Semiconductor Industry Conference

October 20–22, 1986
Hotel Inter-Continental
San Diego, California

Dataquest

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Dataquest

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1986 SEMICONDUCTOR INDUSTRY CONFERENCE
Recovery: Managing the New Industry Structure

October 20–22

Hotel Inter-Continental
San Diego, California

SUNDAY, October 19

4:00 p.m. to 8:00 p.m.	**Registration**	*Tea Lounge*
7:00 p.m. to 9:00 p.m.	**Hosted Cocktails**	*Ballroom C*

MONDAY, October 20

7:30 a.m.	**Buffet Breakfast**	*Pavilion G*
7:30 a.m.	**Registration Continues**	*Pavilion Foyer*
9:00 a.m.	**Welcome Address** Manny Fernandez President Dataquest Incorporated	*Pavilion D, E, & F*
9:15 a.m.	**The New Industry Structure** Howard Bogert Vice President and Director, Semiconductor Industry Group Dataquest Incorporated Robert McGeary Director, Semiconductor Equipment and Materials Service Dataquest Incorporated	*Pavilion D, E, & F*
10:00 a.m.	**U.S. Industry Achievements and Opportunities** Jon E. Cornell Senior Vice President and Sector Executive, Semiconductor Sector Harris Corporation	*Pavilion D, E, & F*
10:30 a.m.	**Coffee Break**	*Pavilion Foyer*
11:00 a.m.	**Wall Street's View of Semiconductors and High Technology** Greg Smith President, Investment Management Group Prudential-Bache Securities	*Pavilion D, E, & F*
11:30 a.m.	**The Future of the Semiconductor Industry: An Inside View** Dr. Robert Noyce Vice Chairman and Vice President Intel Corporation	*Pavilion D, E, & F*
12:00 Noon	**Lunch**	*Pavilion G*
2:00 p.m.	**Semiconductor Applications in a Global Environment** Wilf Corrigan Chairman of the Board LSI Logic Corporation	*Pavilion D, E, & F*
2:30 p.m.	**The Merging of Analog and Digital** James Smaha Executive Vice President and General Manager National Semiconductor Corporation	*Pavilion D, E, & F*
3:00 p.m.	**Break**	*Pavilion Foyer*
3:15 p.m.	**The Evolution and Future of On-time Delivery** Jim Norling Executive Vice President and General Manager, Semiconductor Product Sector Motorola, Inc.	*Pavilion D, E, & F*
3:45 p.m.	**The Role of Technology in the New Industry Structure** Dr. Wilmer Bottoms General Partner Alan Patricof Associates	*Pavilion D, E, & F*
4:15 p.m.	**Adjourn**	
6:00 p.m.	**Buses Leave Hotel for Dinner Cruise**	*Pavilion Entrance*

TUESDAY, October 21

7:30 a.m.	**Buffet Breakfast**	*Pavilion G*
9:00 a.m.	**Service, the Next High-Tech Battleground** Dr. William Davidow General Partner Mohr, Davidow Ventures	*Pavilion D, E, & F*
9:30 a.m.	**Responding to the Competitive Challenge** Fred McClintock Manager, Commodity Management Xerox Corporation	*Pavilion D, E, & F*
10:00 a.m.	**The Revolution in Programmable Logic Devices** Rahul Sud President and Chief Executive Officer Lattice Semiconductor Corporation	*Pavilion D, E, & F*
10:30 a.m.	**Coffee Break**	*Pavilion Foyer*
11:00 a.m.	**ASICs: Their Evolution from a User's Perspective** Prakash Bhalerao Group Manager, ASIC Business Digital Equipment Corporation	*Pavilion D, E, & F*
11:30 a.m.	**Japan's Shift to Creative Research** Sheridan Tatsuno Senior Industry Analyst, Japanese Semiconductor Industry Service Dataquest Incorporated	*Pavilion D, E, & F*
12:00 Noon	**Lunch**	*Pavilion G*
2:00 p.m.	**ASICs, the Real Cost** Wayne Spence Vice President, Semiconductor Group; Manager of ASICs Division Texas Instruments	*Pavilion D, E, & F*
2:30 p.m.	**U.S. and Japanese Manufacturing: What is the Real Difference?** Jim Bagley Senior Vice President Applied Materials, Inc.	*Pavilion D, E, & F*
3:00 p.m.	**Break**	*Pavilion Foyer*
3:15 p.m.	**Industry Challenges Within the New Trade** Andrew A. Procassini President Semiconductor Industry Association	*Pavilion D, E, & F*
3:45 p.m.	**Fab Automation in the U.S.: Bringing the Dream to Reality** Susan Powell Billat Manager, Wafer Fabrication Process Bechtel National, Inc.	*Pavilion D, E, & F*
4:15 p.m.	**Europe's Renewed VLSI Thrust** Gernot Oswald Executive Director, Marketing and Sales, Semiconductor Components Siemens AG	*Pavilion D, E, & F*
4:45 p.m.	**Adjourn**	
6:30 p.m. to 7:30 p.m.	**Cocktails**	*Pavilion I*
7:30 p.m.	**Dinner** **Dinner Address** **Contribution: the New Competition** Jerry Sanders Chairman and Chief Executive Officer Advanced Micro Devices	*Pavilion G*
9:00 p.m.	**Informal Discussion**	*Pavilion C*

WEDNESDAY, October 22

7:30 a.m.	**Buffet Breakfast** .... *Pavilion F*
	FOCUS SESSIONS The first two Focus Sessions will run concurrently with the third. Attendees may join the third session at any time. Coffee service will be available between all sessions.
8:00 a.m. to 9:30 a.m.	**ASIC Focus Session** .... *Pavilion H & I* **Trends in CMOS PLDs** Moderator: Andy Prophet Senior Industry Analyst, Semiconductor Industry Service Dataquest Incorporated ■ Dave Laws Vice President, Marketing Altera Corporation ■ Dane Elliot Manager, Applications Engineering Cypress Semiconductor ■ Wes Patterson Senior Vice President of Marketing Xilinx Corporation ■ Andrew Haines Strategic Marketing Manager, Application-Specific Products VLSI Technology, Incorporated
9:30 a.m. to 12:00 Noon	**Application Markets Focus on Microperipherals for Communication** .... *Pavilion H & I* Moderators: Janet Oncel Industry Analyst, Semiconductor Industry Service Dataquest Incorporated Anthea Stratigos Product Manager, Semiconductor Application Markets Dataquest Incorporated ■ Electronic and Procurement Outlook Anthea Stratigos Product Manager, Semiconductor Application Markets Dataquest Incorporated ■ Data Communications Overview Larry Fullerton Dataquest Consultant ■ Technology Trends and Standards Graham Alcott General Manager, Telecommunications Operations Intel Corporation ■ Impact on Modems Lynn Ditty Product Manager, Communications Products AT&T Technology Systems ■ The Semiconductor Manufacturer's Role Ron Ruebusch Director of Strategic Marketing Advanced Micro Devices

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8:00 a.m. to 12:00 Noon	**Semiconductor Equipment and Materials Service Focus Session**	*Pavilion D & E*
	Semiconductor Fabrication Technology Trends Session Leader: Joseph Grenier Senior Industry Analyst, Semiconductor Equipment and Materials Service Dataquest Incorporated	
8:00 a.m.	**The Changing Environment of Photomask Manufacturing** Travis White Vice President, Materials, Logistics, and Systems LSI Logic Corporation	*Pavilion D & E*
8:30 a.m.	**Lithography in Production through 1992** Aubrey C. Tobey Vice President Micronix	*Pavilion D & E*
9:00 a.m.	**Future Trends in Plasma Etch Processing** Dr. David Wang Director, Advanced Technology Applied Materials, Inc.	*Pavilion D & E*
9:30 a.m.	**Resists for Microlithography** Mary Long Adjunct Lecturer, Microelectronics Laboratory University of Arizona	*Pavilion D & E*
10:00 a.m.	**Coffee Break**	*Pavilion Foyer*
10:30 a.m.	**Trends in Deposition Technology and Equipment** Dr. Klaus Schuegraf Vice President, Director of Technology Tylan	*Pavilion D & E*
11:00 a.m.	**Ion Implantation Equipment Trends** Dr. Andrew Wittkower Consultant	*Pavilion D & E*
11:30 a.m.	**Equipment and Materials: A Perspective from SEMS** Joseph Grenier Senior Industry Analyst, Semiconductor Equipment and Materials Service Dataquest Incorporated Dr. Peggy Wood Research Analyst, Semiconductor Equipment and Materials Service Dataquest Incorporated	*Pavilion D & E*
12:00 Noon	**Lunch**	*Pavilion F*
	Conference Adjourns	

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Final List of Attendees

Advanced Micro Devices, Inc.	Ben Anixter, Vice President, Corporate Marketing W. Curtis Francis, Vice President, Strategic Planning Ron Ruebusch, Director, Strategic Marketing Jerry Sanders, Chairman & Chief Executive Officer
Aerospatiale	Robert Zanotti, Components Engineering Group Manager
Air Products & Chemicals, Inc.	Sen Chen, Marketing Manager
Alan Patricof Associates	Wilmer Bottoms, Senior Vice President Diane Bottoms
Alphagaz	Junichi Imakita, General Manager Electronics Division
Altera Corporation	David Laws, Vice President, Marketing Jean Laws
Aluminum Company of America	James Yates, Technical Director Felicia Yates
American Semicon Equipment Technology	Ralph Miller, Vice President, Marketing Greg Reyes, Chairman Harry Stover, Vice President, Applications
AMRO Bank	Charles Riepe, Senior Vice President, Western Region
ANELVA Corporation	Owen Wilkinson, Marketing Applications Engineer
Anicon, Inc.	Darrel Kinkaid, Vice President, Sales

Apple Computer, Inc.	John Jennings, Purchasing Supervisor Brian Robertson, Supply Base Manager Frank Young, Senior Buyer
Applied Materials, Inc.	James Bagley, Senior Vice President Jean Bagley Gary Bultman, Manager, Strategic Marketing Dennis Hunter, Director, Strategic Marketing David Wang, Director, Advanced Technology
Applied Micro Circuits Corporation	Michael Hollabaugh, Director, Marketing
Arthur Young & Company	Alton Page, Manager
Asea Industries & Electronics	Lars Bodin, President
ASJX Systems Corporation	Wayne Pittenger, President & Chief Executive Officer
ASM Lithography, Inc.	Myrna Van Zanten William Van Zanten, Executive Vice President & General Manager Robert Ward, Sales & Marketing Manager
AT&T	Richard Gilbert, District Manager Linda Cohen, Daniel Lankford
AT&T Bell Laboratories	Glen Cheney, Director, Silicon Device Development James Goldey, Director William Grupen, Department Head Harry Kalvonjian, Department Head Sitoris Kitsopolis, Supervisor Michael Maul, Department Head, IC Customer Service
AT&T Technologies, Inc.	Lynn Ditty, Product Manager, Communications Products Mary Dawn Ditty Thomas Egan, Senior Product Planner, Electronic Components

Ateq Corporation	Douglas Marsh, Vice President, Sales & Marketing Pat Marsh
Austek Microsystems	Jack Balletto, Chief Executive Officer & Managing Director Ron Kasper, Vice President, Sales Paul Lui, Vice President
Bain & Company	John Bergren, Associate Consultant David Woodward, Consultant Norm Wu, Manager
Bank of America	George Bradish, Vice President Mark Verissimo, Vice President
Bank of Boston	Bruce Lipian, Loan Officer Joseph Mannes, Loan Officer
Bechtel Corporation	Susan Billat, Manager, Microelectronics Chris Billat
Bechtel National, Inc.	Curt McGee, Manager, Marketing & Business Development
Berkshire Corporation	George Gilder, Author
Bipolar Integrated Technology, Inc.	Ralph Kaplan, Vice President, Sales
Booz, Allen & Hamilton, Inc	Aydin Koc, Principal
Branson International Plasma Corporation	Rod MacDonald, Vice President, Finance & Administration
Burroughs Corporation	Wally Sanabria, Director, Computer Contracts & Procurement Charles Tague, Manager/IC Marketing
California Devices, Inc.	Martin Harding, Director, Strategic Marketing Douglas Ritchie, President & Chief Executive Officer Anne Ritchie

Calma Company	Van Lewing, Vice President, Marketing Electronics
Capital Management Group	Greg Smith, President
Capital Research Company	Jim Martin, Senior Vice President Richard Yeung, Vice President
Chiyoda International Corporation	William Cummings, Deputy General Manager
Comm Group Consultants	Larry Fullerton, Partner Kathy Fullerton
Crawford Fitting Company	David Simko, Manager, Marketing Resources
Cray Research, Inc.	Kathleen Bernard, Marketing Consultant
Crosspoint Venture Partners	Walter Kortschak, Associate
Cryolab	Burt Lancaster, Vice President, Marketing
Custom Silicon, Inc.	Albert Belle Isle, President
Cypress Semiconductor Corporation	Dane Elliot, Manager, Applications Engineering Lynda Elliot Lowell Turriff, Vice President, Sales & Marketing
Data General Corporation	Jim McHugh, Semiconductor Procurement Consultant
Data I/O	Richard Nyder, Manager, Programmer Marketing
Dataproducts Corporation	Barry Geier, Corporate Purchasing Agent

Dataquest Incorporated	Carol Bender, Conference Assistant Betty Bluford, Administrative Assistant Howard Bogert, Vice President & Director, Semiconductor Industry Group Ronald Bohn, Research Analyst Michael Boss, Industry Analyst Stan Bruederle, Vice President & Director, Semiconductor User Information Service George Burns, Industry Analyst Greg Chagaris, Industrial Marketing Manager Steve Cooper, Industrial Marketing Manager Victor de Dios, Senior Industry Analyst Ralph Dickman, Industrial Marketing Manager Maureen Drobot, Conference Assistant Manny Fernandez, President Patricia Galligan, Research Associate Kelly Gustus, Research Associate John Jackson, National Sales Manager Colleen Kelly, Project Assistant Bryan Lewis, Research Analyst Dennis Lyftogt, Manager, Industrial Marketing Tico Marsh, Conference Assistant Robert McGeary, Director, Semiconductor Equipment & Materials Service
Dataquest Incorporated	Ken McKenzie, Director, Product Marketing Debra McKenzie David Norman, Research Associate Gene Norrett, Vice President & Director, Japanese Semiconductor Industry Service Mary Olsson, Industry Analyst Janet Oncel, Industry Analyst Denise Pacheco, Conference Assistant Jean Page, Account Manager, Strategic Executive Services Jewel Peyton, Director, Corporate Communications Andy Prophet, Senior Industry Analyst John Randall, Manager, Industrial Marketing Mark Reagan, Research Associate James Riley, Senior Vice President, Corporate Consulting Susan Scibetta, Research Analyst Lynn Stern, Conference Coordinator Anthea Stratigos, Product Manager, Semiconductor Applications Markets Sheridan Tatsuno, Senior Industry Analyst

Dataquest Incorporated	Laurie Teixeira, Research Assistant Mel Thomsen, Associate Director, Semiconductor Industry Service Paul van Dillen, Industry Marketing Manager Tom Wang, Associate Director, Asian Services Shali Wang Peggy Wood, Research Analyst Mike Woodward, Vice President, Corporate Finance and Accounting Jan Woodward Fred Zieber, Executive Vice President & General Manager, Technology Operations
Dataquest Japan, Ltd.	Osamu Ohtake, Associate Director
Dataquest UK Limited	Malcolm Penn, Vice President & Director European Operations
Department of Trade and Industry, United Kingdom	Alan Conway, Head of Branch John McAuley
Digital Equipment Corporation	Prakash Bhalerao, Senior Group Manager, Semiconductor Division Ken Brabitz, Program Manager, Advanced Process Development Group
Dimos AG	Willi Bacher, President
Dow Corning Corporation	Kit Kemp, Market Development Specialist
E.I. DuPont de Nemours & Company	Joseph McGonnell, Manager, Advanced Products & Systems Charles Van Soye, Senior Accounts Manager
Electric Power Research Institute	John Cummings, Director, Renewable Resource Systems Department
Electronic Business Magazine	John Kerr, Associate Editor
Electronic Engineering Times	Stan Baker, Semiconductor Editor

Electronic News	Loring Wirbel, Semiconductor Correspondent
Electrotech	Bernard Culverhouse, Marketing Director
Emerson Electric Company	Dale Reynolds, Program Manager Judy Reynolds
Ericsson Information Systems AB	Birger Sundqvist, Manager, Econometrics
Exar Corporation	Shayam Dujari, Marketing Manager Nob Hatta, President
Fairchild Semiconductor Corporation	Francine Plaza, Director of Communications Greg Sheppard, Business Analyst
Ferranti Interdesign, Inc.	Michael Kennett, Vice President, Marketing & Sales
Fidelity Venture Associates, Inc.	Thomas Stephenson, President
Focus Semiconductor Systems, Inc.	Richard Tetschlag, Vice President, Marketing
Ford Microelectronics, Inc.	Harry Nystrom, Worldwide Sales Manager
Ford Motor Company	Eugene Greenstein, Manager, Electronic Technology
Fujitsu Microelectronics, Inc.	Emi Irigashi, Corporate Strategic Planning and Communications
GCA Corporation	Wayne Sayers, Director of Government Relations
GE Intersil, Inc.	Jerry Kiachian, Vice President, Manufacturing
GE Venture Capital	Greg Stapleton, Senior Vice President

GTE Government Systems Corporation	Tony Chernoske, General Manager Steve McGrady, Marketing Analyst
General Instrument Corporation	Robert Pritchard, Corporate Director, Technology
General Instrument Microelectronics, Inc.	Steve Maine, Vice President, Marketing John Ricketts, Vice President, Process Engineering
Genus, Inc.	William Elder, President William Harshbarger, Vice President, Technology Kurt Lightfoot, Vice President, Marketing
Gould, Inc.	Jaime Martorell, Manager Product Planning
Hamilton/Avnet	Bob Gardner, Vice President & General Manager
Harris Corporation	Jon Cornell, Senior Vice President & Sector Executive
Hayes MicroComputer Products, Inc.	Tom Campbell, Commodity Manager Richard Grogean, Purchasing/Vendor Relations, Manager
Hewlett-Packard Company	Robert Santos, Product Marketing Manager Fred Schwettmann, Group General Manager, Circuit Technology Group
Hitachi America, Inc	Elisabeth Blaettermann, Senior Marketing Research Analyst
Hitachi Microsystems International	Kosei Nomiya, President
Hitachi, Ltd.	Hisao Kanamaru, Deputy General Manager
Hoya Electronics Corporation	Donald Frey, Senior Marketing Manager Shoichi Harada, General Manager, Electronic Materials

Hughes Aircraft Company	Richard Belardi, Assistant Division Manager Paul Hart, Senior Scientist Mel Meyers, Manager, Procurement Grant Parker, Assistant Department Manager
Hyundai Electronics America	C.S. Park, Chief Operating Officer
IBM Corporation	John Cahalan, Advisory Engineer Denis Fandel, Senior Business Analyst Cheryl Fandel Basil Harrison, Advisory Engineer David Jacobs, Buiness Analyst Sol Lewin, Senior Engineer John Melgalvis, Advisory Engineer Gerald Parker, Program Manager, Process Technology
ICD Austria	Hubert Gammer, West Coast Director
ICI Americas, Inc.	Richard LaFrance, Project Manager Bill Robson, President & Chief Executive Officer
Ing. C. Olivetti & C., S.p.A.	Tito Conti, Director of Quality, Corporate Staff Giampiero Garelli, Vice President, Corporate Procurement Piero Giannatempo, Director, Electronic Components
Inova Microelectronics Corporation	Kirk MacKenzie, Vice President, Marketing & Sales
Integrated Device Technology, Inc.	Bill Snow, Strategic Marketing Manager
Intel Corporation	Graham Alcott, Director, Telecom Operations Leonard Hills, Manager, Industry Research Don Knowlton, Product Marketing Manager Bruce LeBoss, Manager, Strategic Communications Mark Norwood, Manager, Corporate Market Research Robert Noyce, Vice Chairman & Vice President Mark Varno, Market Research Manager, Microcomputer Albert Yu, Assistant General Manager

InterFirst Venture Corporation	Mark Masur, Vice President
Interface International Corporation	Jerry Mills, Director
International CMOS Technology	Drew Osterman, President
International Microelectronic Products	Peter Hillen, Director, Strategic Marketing
Intersil, Inc.	Paul Gupta, President
Italtel	Gianni Bertolini, Director, Corporate Procurement Mario Tripputi, Advanced Product & Technologies Manager
J. H. Whitney & Company	Harry Marshall, Partner
J.P. Morgan Investment Management	Charles Kimball, Vice President Mary Ann Liberatore
John Hancock Venture Capital	Laurie Thomsen, Associate
LASERPATH	Larry Jordan, Vice President, Sales & Marketing Michael Watts, President & Chief Executive Officer
LM Ericsson Corporation	Bengt Soderberg, Vice President, Corporate Purchasing
LSI Logic Corporation	Wilfred Corrigan, Chairman & Chief Executive Officer Bruce Entin, Vice President, Investor Relations Murray McLachlan, Vice President & Chief Development Officer William O'Meara, Vice President & Chief Marketing Officer Joyce O'Meara Travis White, Vice President, Materials, Logistics & Systems Sharon White

LTX Corporation	Roger Blethen, Vice President R. Scott Higgins, Manager, Investor Relations
Lattice Semiconductor Corporation	Ray Capeze, Executive Vice President Jan Johannessen, Marketing Director Rahul Sud, President & Chief Executive Officer
Lehman Management Company	Larry Phillips, First Vice President
Lex Electronics	Edward Verlander, Corporate Planner
Lex Service, Inc.	Milton Grannatt, Vice President, Planning Christina Iwamura, Planning Manager
Machine Intelligence Corporation	Paul Reagan, President & Chief Executive Officer
Mars Electronics	Michael Massari, Buyer
Matrix Integrated Systems, Inc.	Rick Hazard, Marketing Manager
Mayfield Fund	William Unger, Partner
Meadows Ventures	John Farah, Venture Manager Beth Petronis, Venture Manager
Mellon Bank	J. Garvin Warden, Vice President
Menlo Ventures	Michael Riordan, Associate
Microelectronic Packaging, Inc.	Josef Ref, President & Chief Executive Officer Batya Ref
Micron Technology, Inc.	Warren Wheeler, Manager, New Product Development
Mitsubishi Electronics	Dwain Aidala, Marketing Manager

Mitsubishi International Corporation	Yosuke Mishiro, Manager, Project Coordination
Mitsubishi Semiconductor America, Inc.	Tad Mizoguchi, Executive Vice President/General Manager
Mohr Davidow Ventures	William Davidow, General Partner
Monolithic Memories, Inc.	Joe McDonough, Corporate Marketing Associate Shlomo Waser, Director, Product Planning
Monsanto Electronic Materials Company	Wendy Grossman, Manager, Market Analysis
Motorola, Inc.	Oliver Edwards, Strategic Marketing Memory Manager Bill Jenkins, Vice President & Director, Sector Technology Ron Katchinoski, Director, Marketing Bill Lane, Strategic Marketing Manager, MOS Memory Al Mouton, Telecom Marketing Manager Jim Norling, Executive Vice President & General Manager Wini Schaeffer, Director, Corporate Marketing Development
Mullard, Ltd.	G.A. Allen
Narumi America, Inc.	Larry LaCross, National Sales Manager
National Bureau of Standards	Brian Belanger, Associate Director, Center for Electronics & Electronic Engineering
National Semiconductor Corporation	Fred Horne, Vice President, Customer Specific Products Richard Hunt, Vice President, Computer Industry Marketing James Smaha, Executive Vice President & General Manager, Semiconductor Group Judy Smaha

NCR Corporation	James Van Tassel, Vice President, Microelectronics Division Mary Lou Van Tassel
NEC Electronics USA, Inc.	Doug Finlay, Planning Specialist Jim Kelley, Vice President, Technology Center
NMB Semiconductor Company	Alex Cheng, Director, Engineering Coordination
Northern Telecom, Ltd.	E. Dennis Colbourne, Assistant Vice President, Marketing
Oki Semiconductor	Jerry Crowley, Vice Chairman and Chief Executive Officer
Olin Corporation	William Fu, Marketing Manager
Olin Hunt Specialty Products, Inc.	Joseph Daltner, Director of Marketing
Optical Specialties, Inc.	John Dralla, Product Marketing Manager Craig Williams, Vice President, Marketing
Pacesitter, Inc	Michael Povey, President
Perkin-Elmer Corporation	Thomas Halloran, Assistant General Manager Robert McMenamin, Marketing Products Manager Scott Miller, Assistant Product Manager
Photronic Labs, Inc.	Deno Macricostas, President
Pico Design Inc.	Bernie Aronson, President
Pitney Bowes, Inc.	Michael Swaluk, Director, Advanced Electronic Memory Lynn Swaluk
Plessey Semiconductors	Robert Anslow, Vice President & General Manager Melvyn Larkin, Director, Technology Howard Widdows, Business Planning Manager

Prudential Venture Capital	Mark Rossi, Vice President
Prudential-Bache Securities	Stephen Balog, Systems Vice President, Research George Bristol, Managing Director Elizabeth Dorsey, Junior Analyst Richard Whittington, Vice President, Research Peter Wolfe, Japanese Technology Analyst
Qronos Technology	Mark Brodsky, Product Manager Semiconductor Industry
RCA Corporation	Robert Lenz
Raytheon Corporation	David Deardorf, Vice President & General Manager Martin Geller, Director, Marketing John Shea, Director, Military Specialist Programs
Regis McKenna, Inc.	Chris Halliwell, Vice President, National Accounts
Ricoh Corporation	Kenichi Ichihashi, Vice President, Marketing
Robert Bosch GmbH	Gunter Matthai, Manager, Technical Planning Paula Matthai
Rockwell International Corporation	Armando Geday, Market Research Analyst William Pearce, Director, CAD/CAE Development
SGS Semiconductor Corporation	Richard Pieranunzi, Vice President
Samsung Semiconductor & Telecom Company	Won Yang, Vice President, Finance & Administration
Saratoga Semiconductor	Edward Browder, President

Scudder, Stevens & Clark	George Rockwood, Vice President, Research
Seattle Silicon Technology, Inc.	Sam Brown, Executive Vice President
Security Pacific Capital Corporation	James McElwee, First Vice President
Seeq Technology, Inc.	Mike Villott, Director, Marketing
Semiconductor Industry Association	Ione Ishii, Manager, Statistical Programs Andrew Procassini, President
Semiconductor Microelectronics International	Joseph Curry, Managing Director
Sequoia Capital	Pierre Lamond, Partner
Sharp Electronics Corporation	Vijay Auluck, Product Marketing
Sheldahl, Inc.	Richard Slater, Senior Vice President, Business Development Marilyn Slater
Sherwood Associates	David Sherwood
Shinko Electric America, Inc.	William Cruickshank, Executive Vice President
Siemens AG	Detlef Nuglisch Gernot Oswald, Executive Director, Marketing & Sales
Siemens Capital Corporation	Michael Hyduk, Director
Siemens Components, Incc.	George Fodor, Marketing Director
Sierra Semiconductor Corporation	Lerry Wilson, Account Assistant
Signetics Corporation	Randy Seale, Strategic Business Planning Manager

Silicon Design Labs, Inc.	James Hammock, President
Silicon Systems, Inc.	Gary Kelson, Senior Vice President & Chief Technical Officer
Silicon Valley Group, Inc.	Bruce Donsker, Marketing Manager
Spectrum Semiconductor Inc.	Paul Russo, President & Chief Executive Officer Sally Russo
Sprague Electronics Company	Paul Emerald, Marketing Manager
Stack GmbH	Bernard Hadley, Managing Director
Standard Microsystems Corporation	J. P. Chalmin, Vice President, Sales Gerald Gollub, Executive Vice President
TRW, Inc.	Arthur Branstine, VP & General Manager, LSI Products Division Eric Ressler, Manager, Production Control
Tektronix, Inc.	David Rummler, Strategic Planning Manager
Telic Alcatel	Joseph Heitz, Engineer, Purchasing Department Mr. Lemeunier, Purchasing Engineer
Teradyne, Inc.	Gordon Padwick, Assistant to the General Manager
Texas Instruments, Inc.	Bill Jewell, Market Analyst Wayne Spence, Vice President & Manager, Semiconductor Group Eva Spence Gloria Verbeek, Market Analyst
The Financial Times	Louise Kehoe, West Coast Editor

The Micromanipulator Company	Harry Bauer, Director, Marketing
The Penn Central Corporation	Douglas Barth, Director, Advanced Computer Technologies
The Thomas Group, Inc.	Ron Johns, Associate Philip Thomas, Managing Director
Thomson/Mostek	Mark O'Molesky, General Manager
Thomson Composants	Bernard Levi, Director Research & Development
Toshiba America, Inc.	Allan Cox, Manager, Semicustom IC Marketing Jay Litus, Director, Marketing
Trillium	James Healy, President
Tylan Corporation	Klaus Schuegraf, Vice President & Director, Technology
Ultratech Stepper, Inc.	Jim Nagel, Director, Sales
Union Carbide Corporation	Anthony Keig, Business Research Manager Charles Krichbaum, Manager, Bulk Electronic Gases Thomas Nelson, Process Manager Electronics Bill Schmeh, Region Sales Manager, Electronic Gases Sandy Schmeh Thomas Singman, Marketing Manager, Electronics
Union Venture Corporation	Lee McCracken, Investment Officer
United Microelectronics Corporation	Suj-Dav Lin
United Microtek, Inc.	Sangho Kang, Vice President
United Technologies Microelectronics Center	Robert Cook, Director, Business Development

University of Arizona	Mary Long, Adjunct Lecturer Franklin Long
VLSI Technology, Inc.	Andy Haines, Strategic Marketing Manager, ASIC Henri Jarrat, President & Chief Executive Officer Jim Miller, Vice President, Worldwide Sales & Marketing Nancy Miller
Vitelic Corporation	Jack Ordway, Vice President, Marketing & Sales
Vitesse Electronics Corporation	James Brye, Vice President, Marketing & Sales
Wacker Siltronic Corporation	Vern Meissner, Director, Marketing
Weitek Corporation	Arthur Collmeyer, President Merlyn Collmeyer
Western Digital Corporation	Ken Hallam, Director, Planning Storage Management Products
Xerox Corporation	Fred McClintock, Manager, Commodity Management Seisei Shohara, Manager, Technical Staff James Vesely, Vice President, Microelectronics Center
Xicor, Inc.	Wallace Tchon, Vice President, Strategic Planning
Xilinx	Wes Patterson, Vice President, Marketing
Zoran Corporation	Alan Portnoy, Vice President, Marketing & Sales
ZyMOS Corporation	Dave Guzeman, Vice President, Marketing Haller Moyers, Senior Vice President & Sales
Z	Richard Jacobs, Consultant Andrew Wittkower, Consultant

Semiconductor Industry Conference
October 20 through 22, 1986
San Diego, California

List of Attendees

Dwain Aidala	Mitsubishi Electronics
Graham Alcott	Intel Corporation
John Algeo	Rockwell International Corporation
G.A. Allen	Mullard, Ltd.
Shozo Amano	NEC Electronics USA, Inc.
Robert Anslow	Plessey Semiconductors
John Archer	Union Carbide Corporation
Bernie Aronson	Pico Design Inc.
Vijay Auluck	Sharp Electronics Corporation
Willi Bacher	Dimos AG
James Bagley Jean Bagley	Applied Materials, Inc.
Jack Balletto	Austek Microsystems
Stephen Balog	Prudential-Bache Securities
Douglas Barth	The Penn Central Corporation
Harry Bauer	The Micromanipulator Company
Brian Belanger	National Bureau of Standards
Richard Belardi	Hughes Aircraft Company
Albert Belle Isle	Custom Silicon, Inc.
Carol Bender	Dataquest Incorporated
John Bergren	Bain & Company
Kathleen Bernard	Cray Research, Inc.
Gianni Bertolini	Italtel

Tony Chernoske	GTE Government Systems Corporation
Jim Clymer	Austek Microsystems
E. Dennis Colbourne	Northern Telecom, Ltd.
Arthur Collmeyer Merlyn Collmeyer	Weitek Corporation
Kevin Conlon	Applied Materials, Inc.
Perry Constantine	LSI Logic Corporation
Tito Conti	Ing. C. Olivetti & C., S.p.A.
Alan Conway	Department of Trade and Industry, United Kingdom
Robert Cook	United Technologies Microelectronics
Steve Cooper	Dataquest Incorporated
Jon Cornell Mary Cornell	Harris Corporation
Wilfred Corrigan	LSI Logic Corporation
Allan Cox	Toshiba America, Inc.
Al Crawford	Arthur Young & Company
William Cruickshank	Shinko Electric America, Inc.
Bernard Culverhouse	Electrotech
John Cummings	Electric Power Research Institute
Joseph Curry	Semiconductor Microelectronics International
William Davidow	Mohr Davidow Ventures
David Deardorf	Raytheon Corporation
Victor de Dios	Dataquest Incorporated
Ralph Dickman	Dataquest Incorporated
Lynn Ditty Mary Dawn Ditty	AT&T Technologies, Inc.
Bruce Donsker	Silicon Valley Group, Inc.

Prakash Bhalerao	Digital Equipment Corporation
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Michael Boss	Dataquest Incorporated
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Edward Browder	Saratoga Semiconductor
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Gary Bultman	Applied Materials, Inc.
George Burns	Dataquest Incorporated
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Tom Campbell	Hayes MicroComputer Products, Inc.
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William Elder	Genus, Inc.
Dane Elliot Lynda Elliot	Cypress Semiconductor Corporation
Paul Emerald	Sprague Electronics Company
Craig Ensley	Crystal Semiconductor Corporation
Bruce Entin	LSI Logic Corporation
Denis Fandel Cheryl Fandel	IBM Corporation
John Farah	Meadows Ventures
Manny Fernandez	Dataquest Incorporated
Jim Fiebiger	Thomson/Mostek
Gary Fleeman	INMOS Corporation
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Patricia Galligan	Dataquest Incorporated
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Barry Geier	Dataproducts Corporation
Martin Geller	Raytheon Corporation
Piero Giannatempo	Ing. C. Olivetti & C., S.p.A.
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George Gilder	Berkshire Corporation
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Gerald Gollub	Standard Microsystems Corporation
Roger Goyins	Dow Corning Corporation
Milton Grannatt	Lex Service, Inc.
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Eugene Greenstein	Ford Motor Company
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Wendy Grossman	Monsanto Electronic Materials Company
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James Healy	Trillium
Joseph Heitz	Telic Alcatel
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Thomas Humphrey	Signetics Corporation
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Harry Kalvonjian	AT&T Bell Laboratories
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Don Knowlton	Intel Corporation

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Ed Neubauer	NEC Electronics USA, Inc.
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Joyce O'Meara	LSI Logic Corporation
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Thomas Stephenson	Fidelity Venture Associates, Inc.
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John Wallace	Ford Microelectronics, Inc.
Donna Walters	Los Angeles Times

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Frank Young	Apple Computer, Inc.
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Fred Zieber	Dataquest Incorporated

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James W. Bagley
Senior Vice President
Applied Materials, Inc.

Prakash Bhalerao
Group Manager, ASIC Business
Digital Equipment Corporation

Susan Powell Billat
Manager, Wafer Fabrication Process
Bechtel National, Inc.

Howard Z. Bogert
Vice President
Director, Semiconductor Industry Group
Dataquest Incorporated

Dr. Wilmer Bottoms
General Partner
Alan Patricof Associates

Jon E. Cornell
Senior Vice President and Sector Executive
Semiconductor Sector
Harris Corporation

Wilf Corrigan
Chairman of the Board
LSI Logic Corporation

Dr. William Davidow
General Partner
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Manny Fernandez
President
Dataquest Incorporated

Fred McClintock
Manager, Commodity Management
Xerox Corporation

Robert McGeary
Director
Semiconductor Equipment and Materials Service
Dataquest Incorporated

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Vice Chairman and Vice President
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Investment Management Group
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Vice President, Semiconductor Group
Manager of ASICs Division
Texas Instruments

Rahul Sud
President and Chief Executive Officer
Lattice Semiconductor Corporation

Sheridan Tatsuno
Senior Industry Analyst
Japanese Semiconductor Industry Service
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Focus Session Speakers

ASIC FOCUS SESSION

Dane Elliot
Manager, Applications Engineering
Cypress Semiconductor

Andrew Haines
Strategic Marketing Manager
Application Specific Products
VLSI Technology Incorporated

Dave Laws
Vice President, Marketing
Altera Corporation

Wes Patterson
Senior Vice President of Marketing
Xilinx Corporation

Andrew M. Prophet
Senior Industry Analyst
Semiconductor Industry Service
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APPLICATION MARKETS FOCUS ON MICROPERIPHERALS FOR COMMUNICATION

Graham Alcott
General Manager
Telecommunications Operations
Intel Corporation

Lynn Ditty
Product Manager
Communications Products
AT&T Technology Systems

Larry Fullerton
Dataquest Consultant
Semiconductor Industry Service

Janet Oncel
Industry Analyst
Semiconductor Industry Service
Dataquest Incorporated

Ron Ruebusch
Director, Strategic Marketing
Advanced Micro Devices

Anthea C. Stratigos
Product Manager
Semiconductor Application Markets
Dataquest Incorporated

SEMICONDUCTOR EQUIPMENT AND MATERIALS SERVICE FOCUS SESSION

Mary Long
Adjunct Lecturer
Microelectronics Laboratory
University of Arizona

Robert McGeary
Director
Semiconductor Equipment and Materials Service
Dataquest Incorporated

Dr. Klaus Schuegraf
Vice President
Director of Technology
Tylan Corporation

Aubrey C. Tobey
Vice President
Micronix

Dr. David Wang
Vice President, Technology and Marketing
Applied Deposition Technology
Applied Materials, Inc.

Travis White
Vice President
Materials, Logistics, and Systems
LSI Logic Corporation

Dr. Andrew Wittkower
Consultant

Dr. Peggy Wood
Research Analyst
Semiconductor Equipment and Materials Service
Dataquest Incorporated

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WELCOME ADDRESS

Manny A. Fernandez
President and Chief Executive Officer
Dataquest Incorporated

Mr. Fernandez is the President and CEO of Dataquest. He has been involved in high-technology industries for the past 16 years. Prior to joining Dataquest, Mr. Fernandez was President and CEO of Gavilan Computer Corporation, where he directed that company's efforts in the portable computer marketplace. Before founding Gavilan, he was President and CEO of Zilog, Inc. Zilog grew by more than 500 percent during Mr. Fernandez's tenure, and expanded its facilities to 11 countries. Prior to joining Zilog, Mr. Fernandez was Group Vice President for Fairchild Camera & Instrument Corporation, where he was responsible for three divisions with a combined revenue responsibility of more than $120 million. He began his career as a design engineer, and held several engineering management positions at ITT Semiconductor and Harris Intertype before going to Fairchild. Mr. Fernandez received B.S. and M.S. degrees in Electrical Engineering from the University of Florida.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
October 20-22, 1986
San Diego, California

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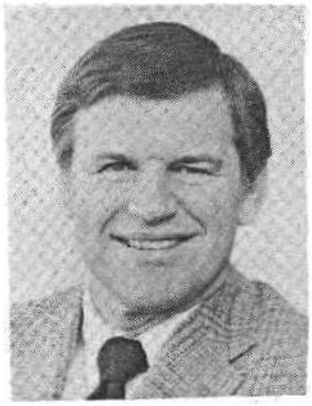
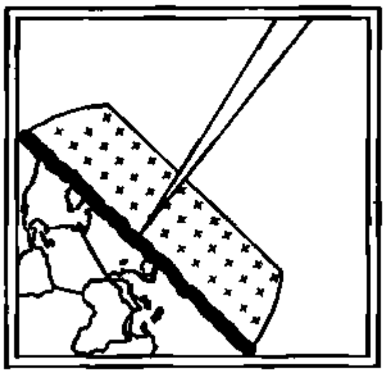
THE NEW INDUSTRY STRUCTURE



Howard Z. Bogert
Vice President
Director, Semiconductor
Industry Group
Dataquest Incorporated

Mr. Bogert is a Vice President of Dataquest and Director of its Semiconductor Industry Group. He is responsible for consulting, publishing, and research activities in semiconductor products, technologies, and suppliers. Prior to assuming his management duties at Dataquest, Mr. Bogert developed the concept of ASICs. Under his direction, Dataquest was the first market research company to follow that market. During his 25 years in electronics, Mr. Bogert has held management positions in market research, product planning, long-range planning, research and development, and engineering. Before coming to Dataquest, he was a Divisional Vice President of Engineering for Rockwell International. Prior to that, he was Director of MOS Development for Siliconix and Manager of Design for AMI. Mr. Bogert holds six patents in the MOS VLSI field, and developed the first MOS circuit to use charge storage. He was also an early contributor to the design of linear integrated circuits. Mr. Bogert received a B.S. degree in Electrical Engineering from Stanford University, an M.S. degree from the University of Maryland, and an M.B.A. degree from the University of Santa Clara.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
October 20-22, 1986
San Diego, California



Recovery: Managing the New Industry Structure

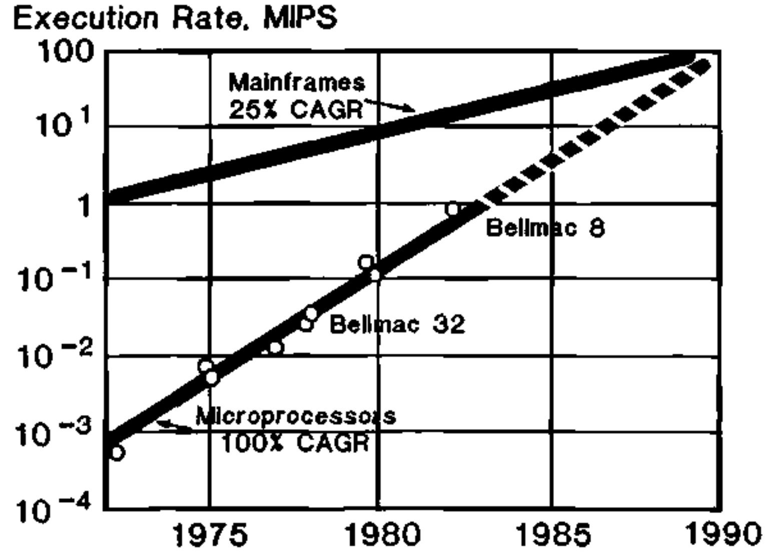
THE NEW INDUSTRY STRUCTURE

HOWARD Z. BOGERT

Vice President and Director
Semiconductor Industry Group
Dataquest Incorporated

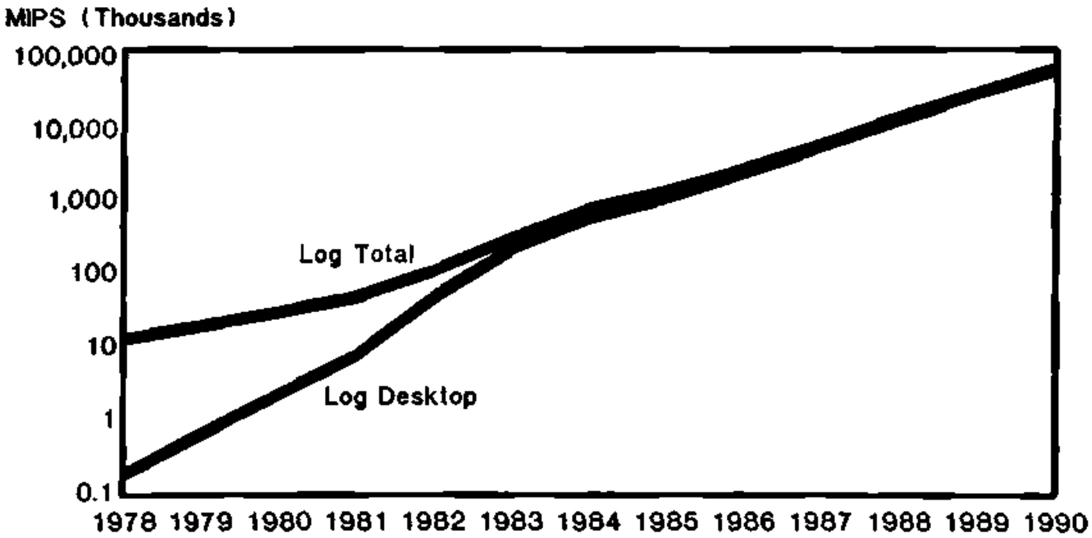
THE SYSTEM IS A CHIP

MICROPROCESSOR AND MAINFRAME CPU PERFORMANCE FORECAST



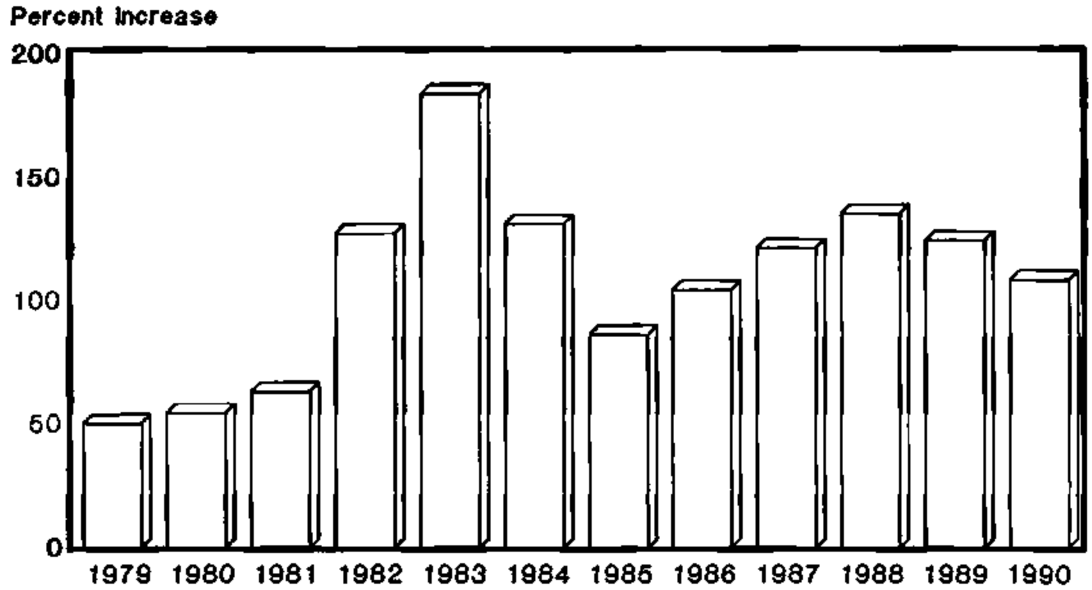
Source: Bernard Murphey
Bell Labs

ESTIMATED MIPS SHIPPED INTO U.S. MARKET



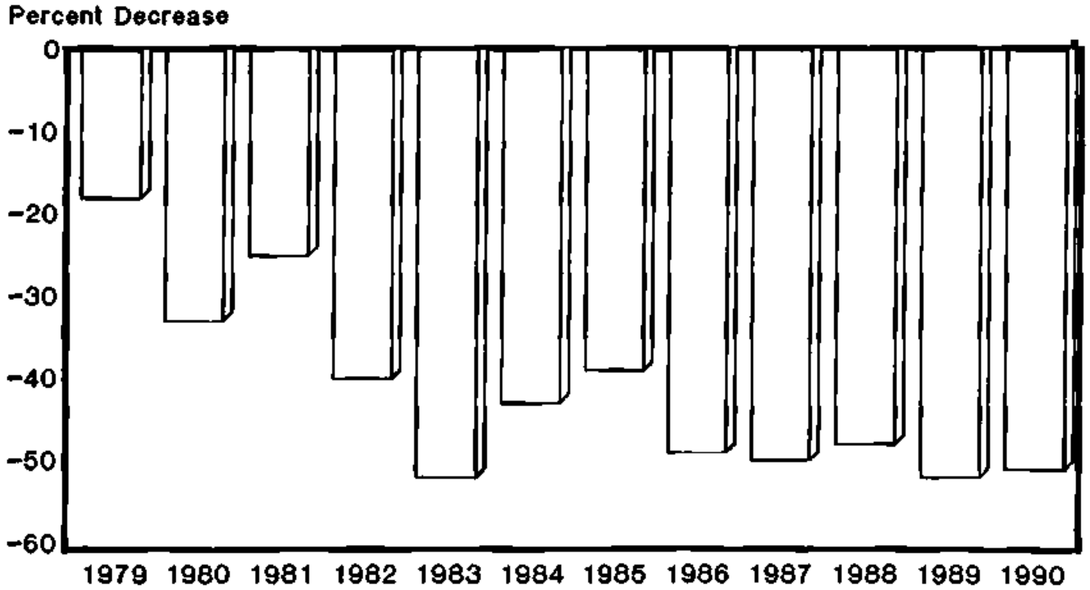
Source: Dataquest

ESTIMATED U.S. MIPS SHIPMENT GROWTH



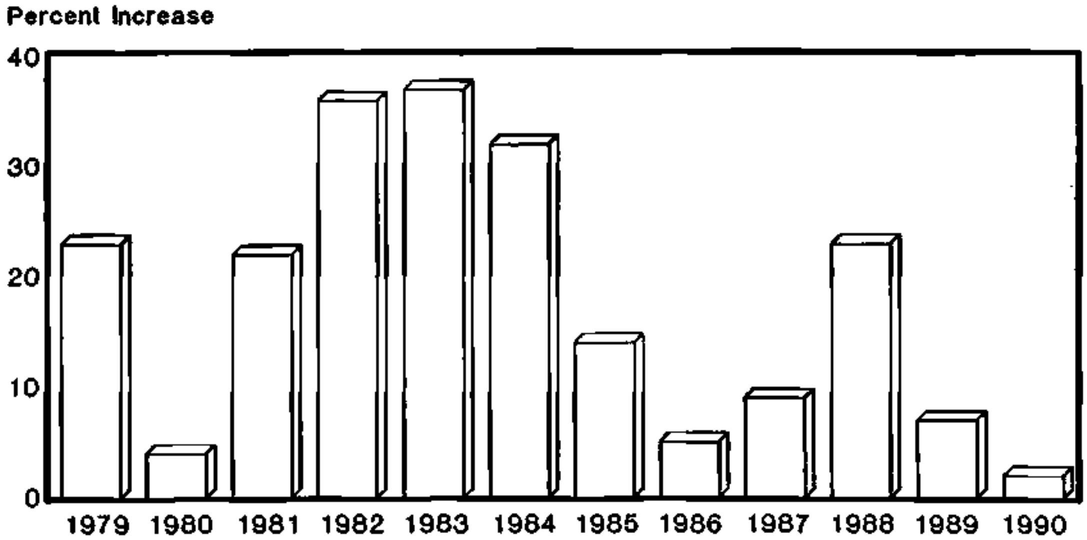
Source: Dataquest

ESTIMATED U.S. MIPS ASP DECREASE



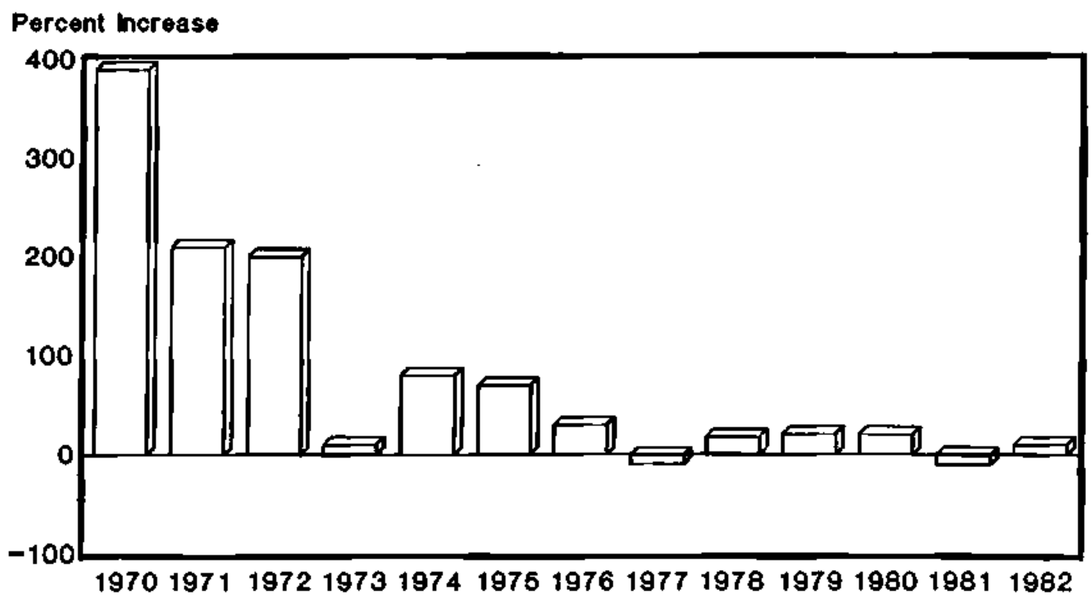
Source: Dataquest

ESTIMATED U.S. COMPUTER MARKET GROWTH



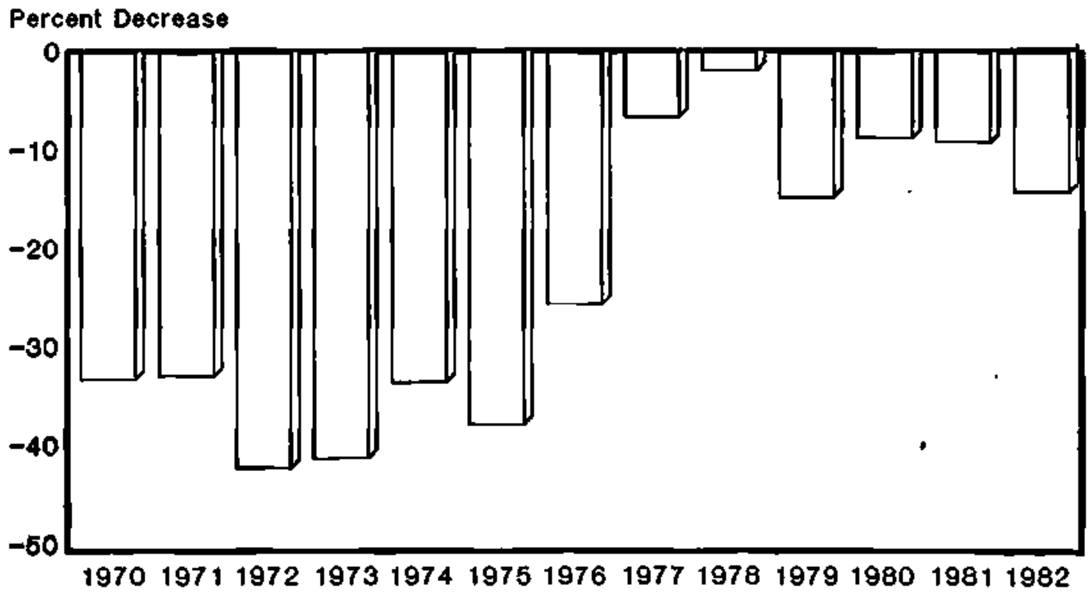
Source: Dataquest

WORLDWIDE CALCULATOR UNIT GROWTH



Source: Dataquest

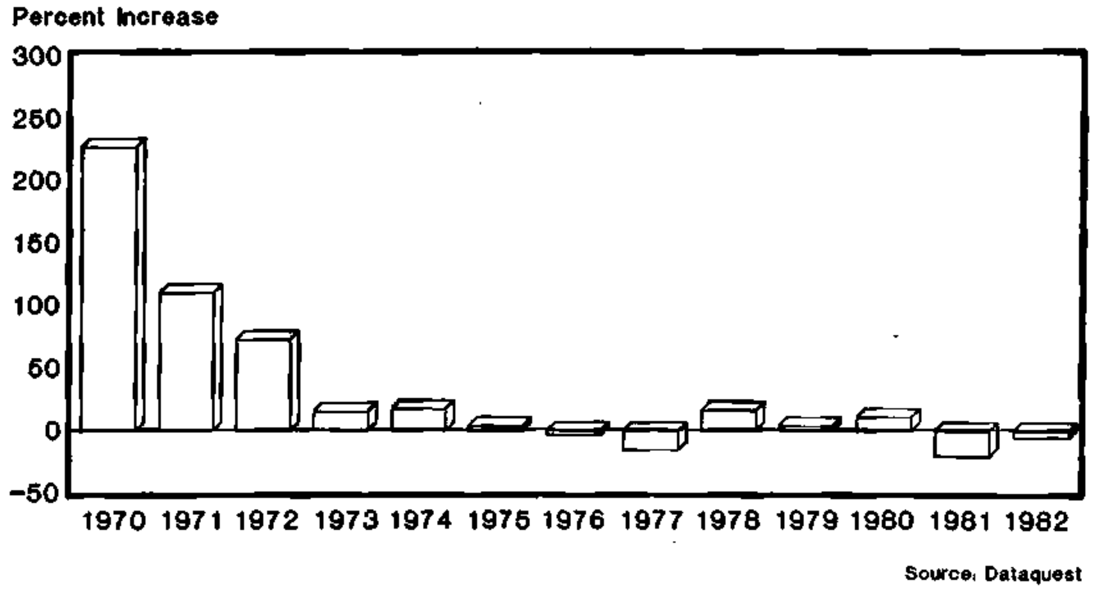
WORLDWIDE CALCULATOR ASP DECREASE



Source: Dataquest

WORLDWIDE CALCULATOR MARKET GROWTH

Percent of Dollars



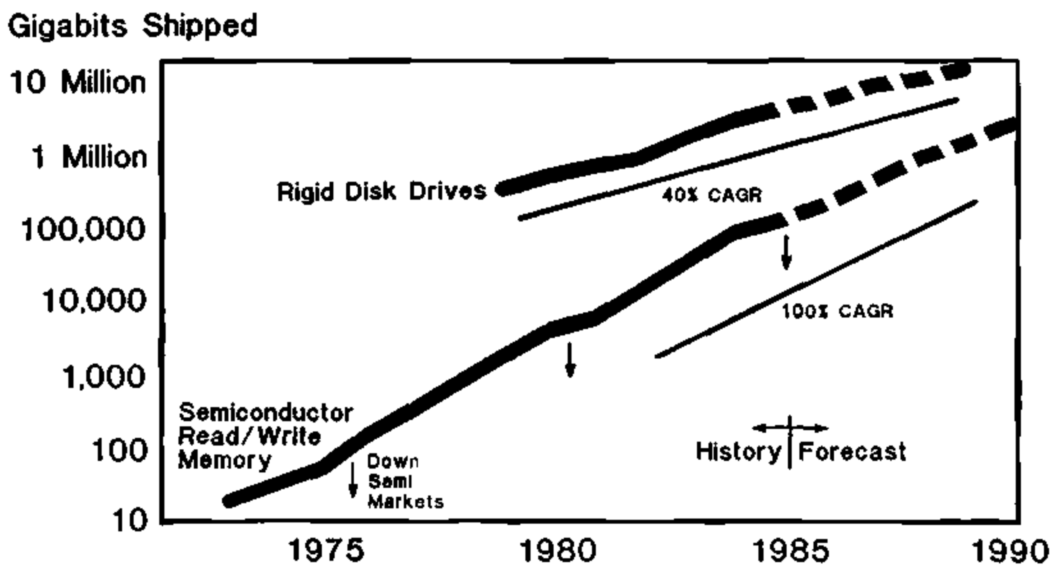
A BILLION-TRANSITOR CHIP WILL BE POSSIBLE BY 1999

COMPUTING POWER OF A BILLION TRANSISTORS

- 128 megabytes RAM
- 1,000 VAX CPUs
- 20 Cray 2 CPUs
- 10 VAXs with memory
- 1/40 Cray 2 with memory

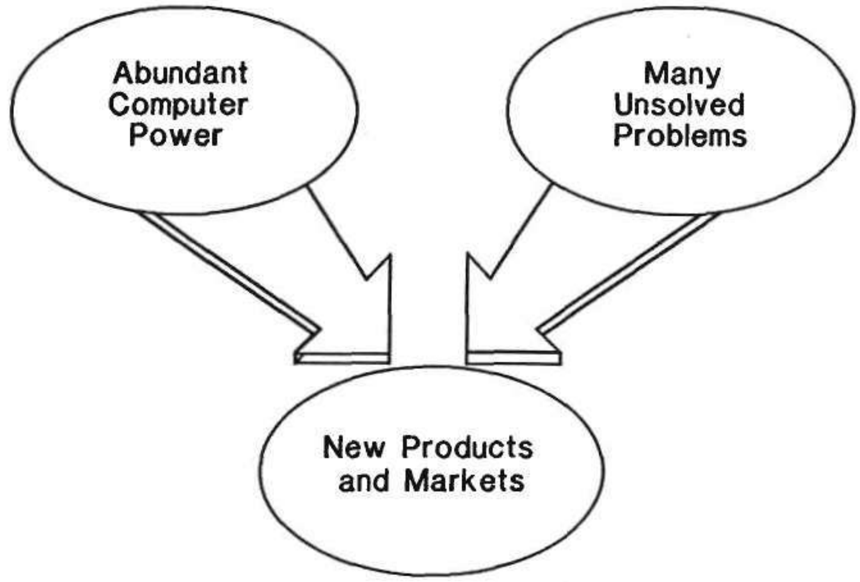
Source: MIPS Computer Systems

ESTIMATED CONSUMPTION COMPARISON OF RIGID DISK AND SEMICONDUCTOR READ/WRITE MEMORY BITS



Source: Dataquest

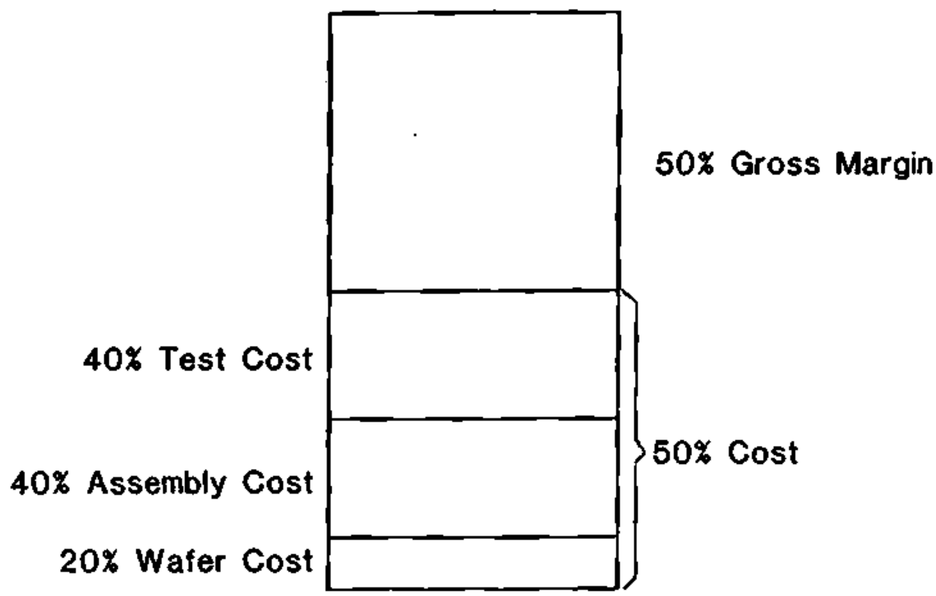
THE AGE OF APPLICATIONS



WHAT DO THESE COMPANIES HAVE IN COMMON?

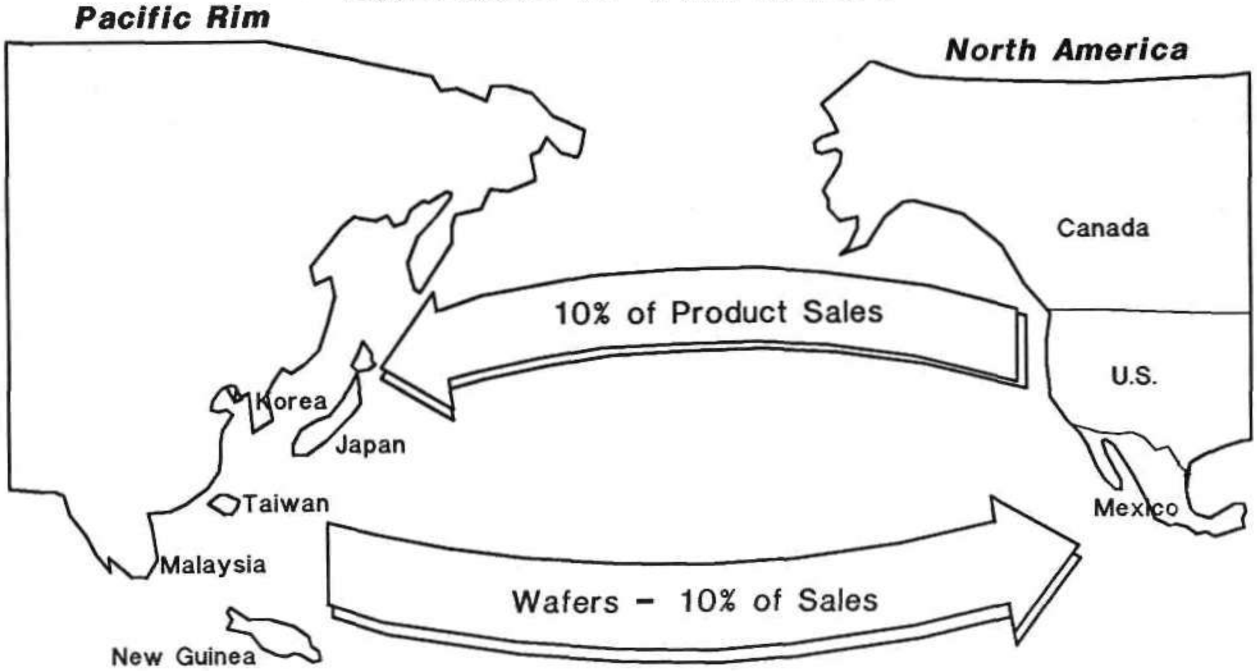
- Weitek
- Vitelic
- Micro Linear
- Wafer Scale Integration
- Altera
- Lattice Semiconductor

FOUNDRY MANUFACTURING COST MODEL



Source: Dataquest

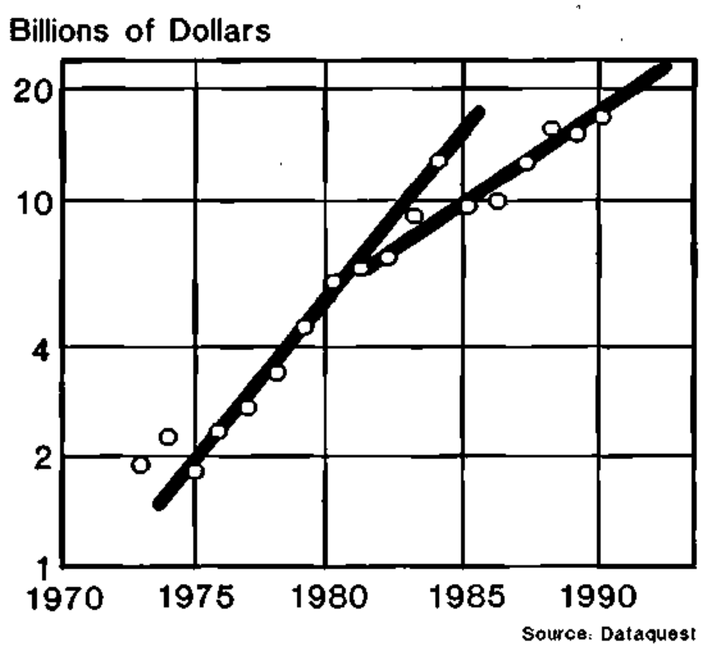
BALANCE OF PAYMENTS



Source: Dataquest

THE KEY:
PROTECTION OF INTELLECTUAL PROPERTY

ESTIMATED NORTH AMERICAN SEMICONDUCTOR CONSUMPTION



ESTIMATED WORLDWIDE SEMICONDUCTOR CONSUMPTION

Percent Change, U.S. Dollars

	1986				
	Quarter				
	1	2	3	4	Year
North America	4.1%	14.4%	(0.3%)	(−1.0%)	6.4%
Japan	11.4%	12.1%	6.3%	(0.4%)	40.6%
Europe	12.1%	9.5%	(0.4%)	2.0%	14.8%
ROW	16.1%	33.3%	7.0%	9.2%	53.9%
Total World	9.3%	14.1%	2.9%	0.7%	23.4%

Source: Dataquest

ESTIMATED WORLDWIDE SEMICONDUCTOR CONSUMPTION

Percent Change, U.S. Dollars

	1986	1987	1988	1989	1990	1991
North America	6.4%	12.0%	32.3%	(5.5%)	10.9%	18.4%
Japan	40.6%	19.4%	20.2%	0.8%	18.8%	20.5%
Europe	14.8%	14.5%	27.4%	4.8%	13.1%	27.9%
ROW	53.9%	37.3%	35.3%	(4.1%)	17.0%	20.8%
Total World	23.4%	17.7%	27.1%	(1.3%)	15.0%	21.1%

Source: Dataquest

CONCLUSIONS

- Surplus computer power will be available for 5 to 10 years
- Long-term semiconductor growth will slow from 18% CAGR to 13% CAGR
- Applications more important than manufacturing
- Protection of inventions is key
- If (or when) innovation slackens, the manufacturers will take over the market

ESTIMATED WORLDWIDE SEMICONDUCTOR CONSUMPTION

Percent Change, U.S. Dollars

	1987				
	Quarter				
	1	2	3	4	Year
North America	(2.0%)	8.0%	7.3%	6.0%	12.0%
Japan	4.1%	5.4%	6.6%	4.2%	19.4%
Europe	3.1%	4.5%	4.0%	6.7%	14.5%
ROW	5.1%	6.9%	5.4%	12.1%	37.3%
Total World	2.0%	6.2%	6.2%	6.1%	17.7%

Source: Dataquest

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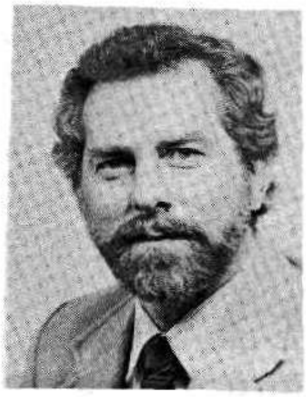
THE NEW INDUSTRY STRUCTURE



Robert E. McGeary
Director
Semiconductor Equipment
and Materials Service
Dataquest Incorporated

Mr. McGeary is Director of Dataquest's Semiconductor Equipment and Materials Service. He was previously a Senior Industry Analyst for Dataquest's Semiconductor Industry Service and was responsible for the Industry and Technology portion of the service. Before joining Dataquest, he was Product Marketing Manager at Applied Materials, Inc., where he managed the worldwide product marketing activities for the Dry Etch Division and managed product support for the European dry etch business. Before that, he worked as Product Marketing Manager at GCA Corporation/IC Systems Group, as an Accelerator Physicist at Lawrence Berkeley Laboratories, as a Nuclear Engineer at Mare Island Naval Shipyard, and as a Reactor Operator at the University of Washington. He received B.S. degrees in Physics and Mathematics from the University of Washington and an M.B.A. degree from St. Mary's College.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
October 20-22, 1986
San Diego, California

**Recovery:
Managing the New
Industry Structure**

FOUNDATIONS OF THE NEW INDUSTRY STRUCTURE

ROBERT McGEARY

Director
Semiconductor Equipment and Materials Service
Dataquest Incorporated

SEMICONDUCTOR CAPITAL SPENDING

Agenda

- Regional production
- Capital spending
- Capacity utilization
- Assumptions
- Conclusions

ESTIMATED REGIONAL SEMICONDUCTOR FABRICATION

(Millions of Dollars)

	1986	1987	1988	CAGR 1985-1990
North America	$16,123	$19,232	$23,767	12.3%
Merchants	12,223	14,599	18,923	
Captives	3,900	4,633	4,844	
Japan	14,292	16,555	21,104	17.7%
Europe	3,753	4,992	6,552	21.8%
ROW	366	541	778	29.7%
Total	$34,534	$41,320	$52,201	15.8%
Growth	21.0%	19.6%	26.3%	

Source: Dataquest

ESTIMATED REGIONAL CAPITAL SPENDING

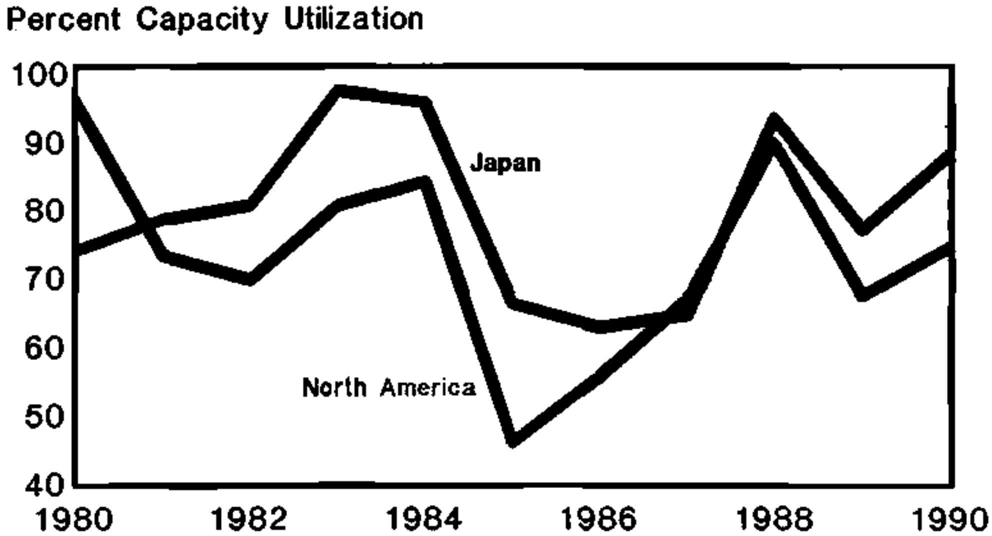
(Millions of Dollars)

	1986	1987	1988	CAGR 1985-1990
North America	$2,561	$2,911	$3,749	5.8%
Japan	3,311	3,241	4,254	7.3%
Europe	655	787	1,062	18.6%
ROW	275	406	606	29.8%
Total	$6,803	$7,344	$9,671	8.8%

Note: Totals may not add due to rounding.

Source: Dataquest

CAPACITY UTILIZATION
U.S. VS. JAPAN



Source: Dataquest

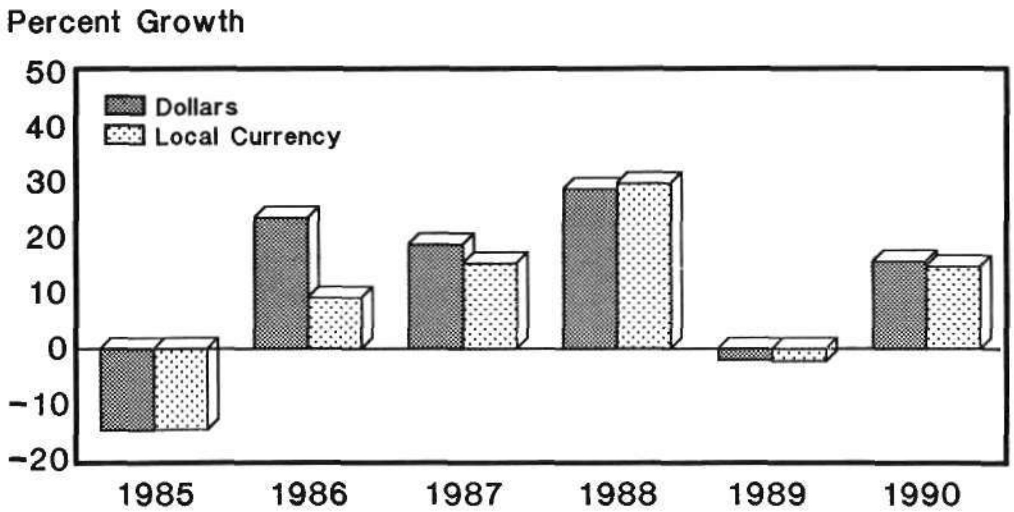
TECHNOLOGY CAPACITY

Product	Technology	Growth
Cellular Radio	>1µm	50%
Robotics	>1µm	28%
LANs	>1µm	12%
Integrated Voice/Data	>1µm	33%
Nonimpact Printers	>1µm	35%
Personal Computers	>1µm	10%
Rigid Disk Drives	>1µm	15%

Source: Dataquest

ESTIMATED SEMICONDUCTOR CONSUMPTION GROWTH

Real vs. Current



Source: Dataquest

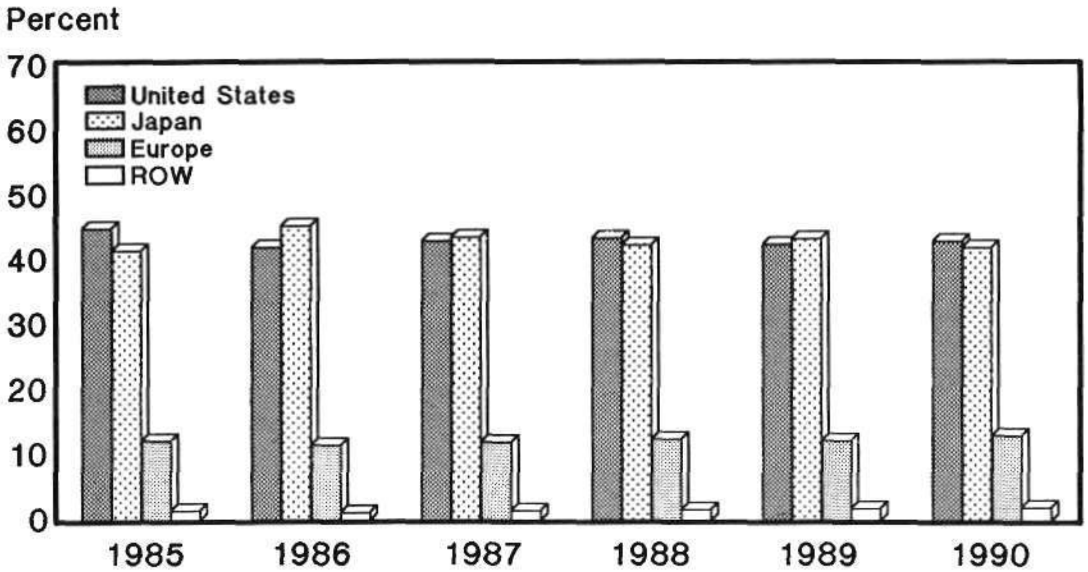
ESTIMATED END-USE GROWTH

1986–1987

Business Computers	6%
Technical Computers	12%
Personal Computers	13%
Telecommunications	12%
Computer Storage	11%
Printers	14%
CAD/CAM	21%
Software	19%

Source: Dataquest

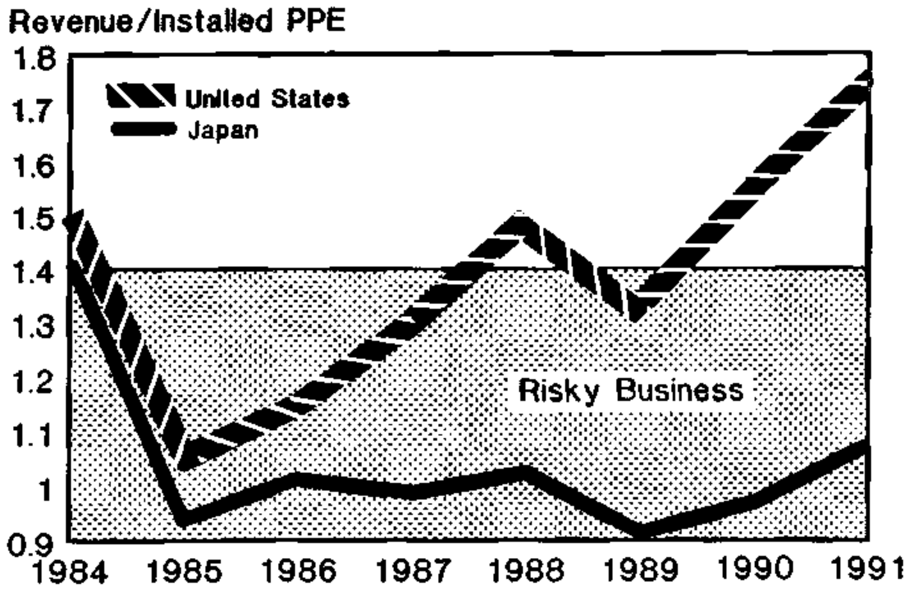
ESTIMATED WORLDWIDE MARKET SHARE - SEMICONDUCTOR COMPANIES



Source: Dataquest

ESTIMATED REVENUE TO CAPITAL RATIO

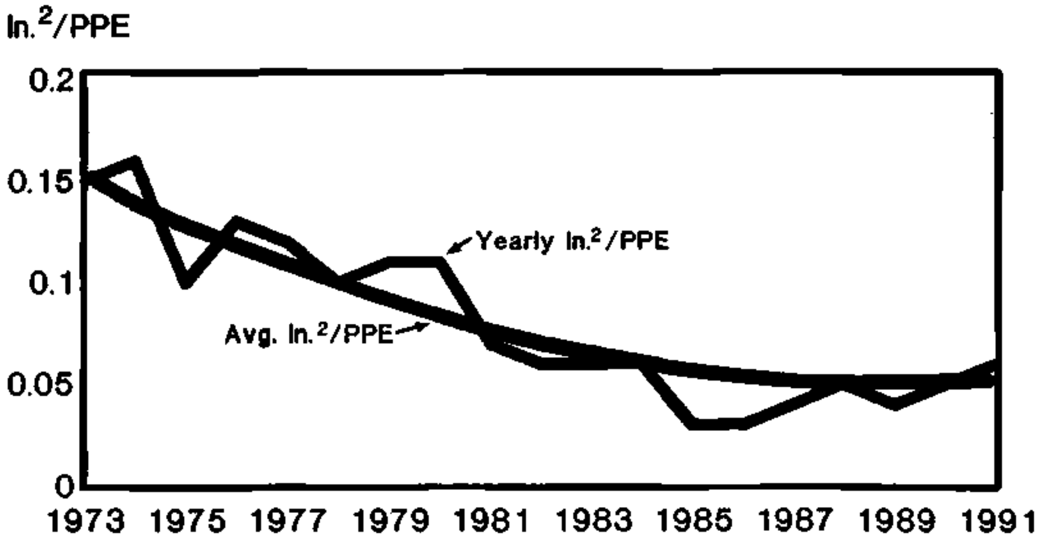
U.S. vs. Japan



Source: Dataquest

ESTIMATED EQUIPMENT PRODUCTIVITY

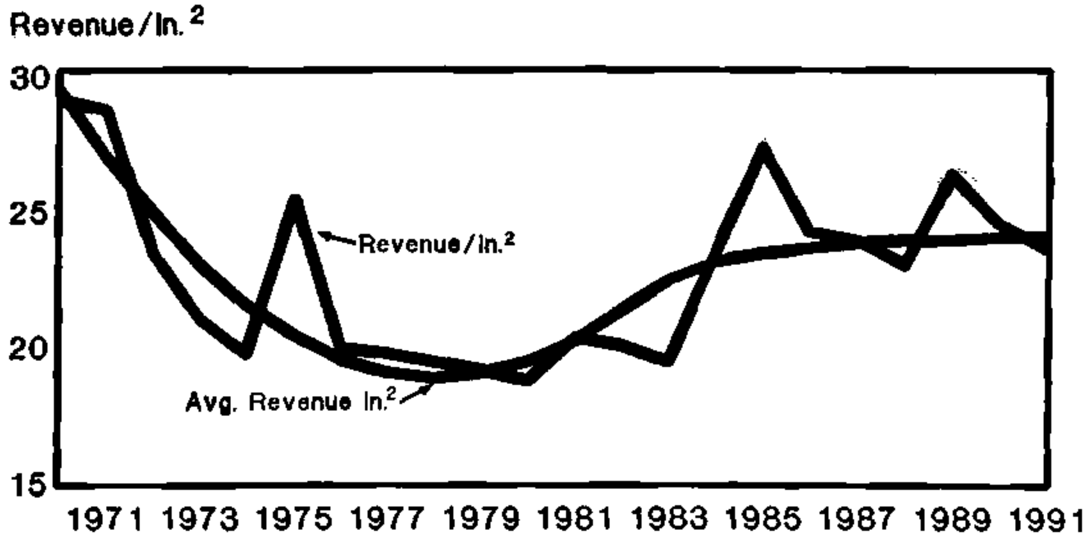
Function of Reliability, Utilization, Throughput



Source: Dataquest

ESTIMATED PROCESS PRODUCTIVITY

Function of Yield, ASP, Die Size



Source: Dataquest

WHY AUTOMATE?
FOR SURVIVAL!!

	Automation	
	Robotics	Software
Yield	Cleanliness	Cycle time
Productivity	Plant management	WIP scheduling

GLOBAL COMPETITION IN SEMICONDUCTORS

- Semiconductor manufacturers: escaping home markets
- Semiconductor market share strategy: where and with whom will capital be spent?
- Equipment and materials vendors: Trojan horse syndrome

ESTIMATED SEMICONDUCTOR GROWTH BY REGION

1985-1990

	Consumption	Production
U.S. region	10%	14%
Japanese region	20%	18%
(in yen)	10%	8%
European region	15%	18%

Source: Dataquest

OFFSHORE SEMICONDUCTOR PRODUCTION AS PERCENT OF COMPANY TOTAL

	1985	1990 (Est.)
North America	10.0%	14.0%
Japan	0.4%	0.9%
Europe	9.0%	18.0%

Source: Dataquest

Survival of
U.S. Industrial Complex

↑

Survival of
U.S. Electronics Industry

↑

Survival of
U.S. Semiconductor Industry

↑

Survival of
U.S. Semiconductor Equipment Companies

↑

Survival of
U.S. Technological Advantage

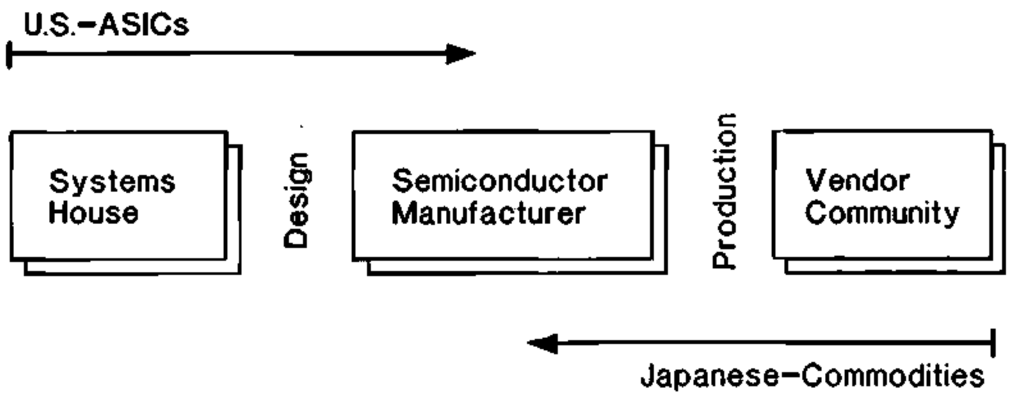
The U.S. has power!

The Japanese are innovative because they have to be!

Jujitsu, karate focus power
→ Efficient use of power through vertical integration

MANUFACTURING PHILOSOPHY

U.S. vs. Japan



Emphasis on design evolves from U.S. lack of vertical integration

THE OPERA IS NOT OVER UNTIL THE FAT LADY SINGS

- Vertical integration through application-specific ICs
- Productivity increases through automation and plant management
- Yield increases through automation and cleanliness

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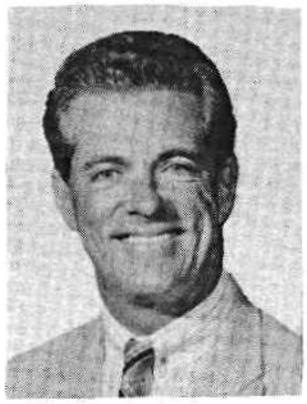
U.S. INDUSTRY--ACHIEVEMENTS AND OPPORTUNITIES



Jon Cornell
Senior Vice President and
Sector Executive
Harris Semiconductor Sector

Mr. Cornell is Senior Vice President and Sector Executive of Harris' Semiconductor Sector. Previously, he was Director of Analog Operations, Vice President of Analog Operations, and the head of Harris' Products Group. He is a member of the Boards of Directors of the Semiconductor Industry Association (SIA) and the Semiconductor Research Corporation. Mr. Cornell received a B.S. degree in Physics from Wichita State University and a master's degree in Electrical Engineering from the University of South Florida in Tampa.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
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(THIS SPEECH WAS NOT AVAILABLE AT TIME OF PUBLICATION)

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WALL STREET'S VIEW OF SEMICONDUCTORS AND HIGH TECHNOLOGY

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Mr. Smith is President of the Capital Managment Group, an Executive Commitee member, and a Director of Prudential-Bache Securities. He is responsible for the Domestic and International Equity and Fixed Income Research Departments, the Strategy Group, Venture Capital, Prudential-Bache Investment Management and Investment Asset, and Quantum. He is also Director of the Prudential-Bache Research Fund. Mr. Smith was previously an Executive Vice President and Director of Research with E.F. Hutton & Co., Inc., where he was in charge of institutional sales and marketing. He received a B.S. degree in Mathematics from the University of Tulsa and an M.S. degree in Mathematics and Economics from Columbia University.

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I realize I'm an unusual speaker at a conference such as this, and if I appear a little bit nervous, it's because I'm not used to talking to this type of audience. But I'm not alone. As I was talking outside the hall a little bit, I saw Manny and I asked Manny, somewhat kiddingly, "What do you think I should talk about?" And he looked stunned and said, "Well, about 25 minutes." So maybe we're all a little uneasy.

Part of the perspective that I should give you is when you look at Wall Street, and you look at our perspective of things, we tend to have a somewhat shorter time horizon which gets shorter and shorter with the volatility in the trading markets. And I think that's a little bit confusing to many of you, but it shouldn't be. It's just basic human nature and Wall Street reflects that. So while it may be somewhat brutal at times, it's very easy to understand. Wall Street rewards accomplishment and accomplishment over time. So lest you think that Wall Street is fickle, this morning I had the opportunity to go out in this little park over here and I noticed that on one of the benches there was an elderly lady--as I get older, elderly gets older, so she was quite advanced in time. She would be what, in New York, we would call a bag lady. I don't know if San Diego admits to such a thing. And next to this bench was this frog, and the frog spoke to the woman and said, "I'm a Texas Oil Man trapped in this frog. If you kiss me I will return to being a Texas Oil Man." And what I would call this bag lady picked up the frog and put it in her pocket. And I couldn't help but be curious about this, so I went over and I said, "I happened to overhear the frog speak to you and I noticed that you didn't kiss the frog, but you put the frog in your pocket." And she said, "Well, you know, Texas Oil Men are a dime a dozen. But a talking frog, well, there's real value." So, these things are human nature. So when Wall Street changes and decides that there's something that's more attractive, there's nothing unusual about that. It's very much part of the way humans are.

To really understand what's been going on in Wall Street and in developments, I have to give you a little bit of very general background and then I'll get more specific. To begin with, in many ways over the past couple years I think it's very clear that we've been thrust into what I would call World War III, which happens to be an economic war, not a military war. We've confronted this grudgingly in looking at our trade statistics and it's becoming more and more clear what the problem is currently. If you look at the exports, the United States, up to about two years ago, had about 20 percent of its exports in general agricultural commodities and there's a lesson to be learned here because the farmer, in retrospect, didn't do anything wrong. The American farmer is just as productive, if not more so, than he was two years ago. But one of the things that happened in the course of the last two or three years is that other people became more productive as a natural course of their development, and what I think is a problem for the farmer and to some extent, a lot of American industry--perhaps including the semiconductor industry--is a lot of the former customers, or potential customers, are now competitors. So we have seen, through no fault of our own, a tremendous surge in developments among countries that are, in the economics world, known as the newly industrialized countries--also known as NICs for short. We most frequently talk about the NICs as being the Pacific Basin or Pacific Rim countries and most people, particularly in the electronics industry, would be familiar with Korea, Taiwan, Hong Kong, and Singapore. But in a general sense, it's not limited to that. Brazil is becoming a major competitor. I think in the not too distant future India, with a population of approximately 750 million people, will increasingly become a competitor in more and more industrialized businesses, including electronics. So it's not so much that we've done something wrong, it's that other countries are getting their political and economic acts together well enough so that in the course of their development, instead of being customers for what we sell, they now compete with us. Or at the very minimum, they are markets that we would have expected historically to sell to, that now no longer are export markets but are supplied by local suppliers. At the same time, in the development of these NICs, we have had to confront an enormous problem with a differential in labor cost. Just to give you a few statistics, I brought along some numbers from our Tokyo research people as we, like most of Wall Street, have become global. In looking at labor statistics at current currency rates, Japan actually, in the technology or the electronics business, actually has higher labor costs than the United States which is somewhat comforting until you look at these four dragons of Taiwan, Hong Kong, Singapore, and Korea, and you see that their labor costs are about one-fifth of either the United States or Japan. So we're really comparing against the wrong competitor in my opinion. I think the NICs are the real competition, and even though labor costs are relatively small relative to the revenue, that kind of differential is so dramatic that it has to have a place in representation in the marketplace. And of course that's true almost regardless of industry. In the auto industry in the United States, full labor costs are about $24.00 an hour. At current exchange rates in Japan, they're pretty close to $20.00 an hour. In Korea, $2.25. That's a tough gap to bridge by being incredibly more productive or more automated or more anything. So what has happened in large measure is a lot of the products, mundane or otherwise, have moved to the low labor costs. And American industry and management has been very efficient. That's spotting the problem and actually finding a way to use it to it's advantage by moving production offshore. Not a closely guarded secret, to be sure, but none the less, a development that has had a clear impact on our trade balance which has affected business. A lot of the customers that made products that you sold to in the States have moved production someplace else. Some of you have figured that out more rapidly than others and moved to share in that business and moved costs offshore, but it's a development that I think has been building for many years, if not a decade, and will continue until these differentials are narrowed. Now, some of you, and maybe all of you, realize that these other countries typically have their currencies tied to the dollar so their currencies haven't adjusted at all against the dollar despite what has happened in Western European and Japanese currencies. While that will help, I'll get to the amount of help, or kind of help, for 1987. It's not really going to make the dramatic change that many economists have promised because they're really not the competition. They will now see how difficult an environment we've been against because our currency appreciated first, and now the Western Europeans and Japanese will see how much fun it is to compete against the NIC countries. And while we will pressure the NIC countries to appreciate their currencies, it will be slow, grudging, and by small amounts compared to the cost differential. In the meantime, look for a very, very difficult export market for the United States, if anything, and imports will grudgingly come down, but instead of coming from Japan they will probably come from other countries as Japan moves their production offshore or someplace substituted. If you go to New York and go to Crazy Eddies you'll see that Samsung and Gold Star--Korean products in televisions and VCRs--have already moved out the Japanese at low price points. Hyundai and the auto market and so on. This is the next wave of competition and it's going to be very, very intense.

I should mention in looking at trade there's another big event coming sometime after the first of the year and that's Gorbochov goes to Japan. Now that's not a movie that I'm sponsoring. The Russians are actually warming up to the Japanese. About five Japanese trade companies have opened offices in Moscow and I think there's going to be some increased political pressure in the trade battle and it's going to come from perhaps the unlikely source of the Japanese. But Gorbochov has made speeches recently indicating that over half of Russia is Asiatic and they should get to know their fellow brethern in Asia more closely, and there _is_ a natural trade fit--Russia has natural resources, Japan has technology and consumer products--and there's a nice, natural trade fit. I wouldn't look for that to accomplish a great deal, but I look for it to become a real issue in terms of psychology and politics in 1987 and that kicks off fairly early in the year. In the meantime, I should mention to you that I think the dollar has stopped its decline against the developed countries--Western Europe and Japan--so there won't be more currency change there. Part of that is a major change in policy. The American administration has decided the dollar's decline is enough, at least against Western Europe and Japan, and they will stop talking down the dollar and I think as we get into 1987, you will see something of a merging of economic outlooks. In 1987, we should see an already weakening Japanese economy slow down to our level or less. Japan's production is slipping; exports and units are declining fairly sharply because of the currency. So their economy will slow, and I believe that in 1987 we will see a slowdown in Europe, particularly in capital spending, primarily because Europe did more or less what we did--that is, they got their capital spending in early in their business cycle, driven in large part in their case by the psychology of inflation of the 70's, and in our case, that plus tax incentives. And in 1987 I think we'll see some of a slowdown in Europe, particularly in capital spending.

One of the other issues that we have to confront in trying to size the problem is this incredible shift that's happened in our economy. Just to use some wide benchmarks: In 1950, the service sector accounted for about 39 percent of our GNP and in 1985 it was about 46 percent of GNP. In 1950, employment in the service sector was 53 percent of all employment, and in 1985 about 74 percent of all employment. And in profits, the service sector took about 36 percent of profits in 1950 and probably two-thirds in 1985. So we've seen a dramatic shift in our economy, and even when economists talk about GNP growing at 3 percent, more and more of that is taken up by the service sector and less by the manufacturing sector. And that really means that the entire production base of the United States, regardless of what part you play in it, has gone from growth cyclical or growth in our definitions of terms, to at best growth cyclical, and in some cases, just plain cyclical. The importance of those labels is in the price you pay for capital. Growth companies get very high valuation; growth cyclicals get quite a bit less. And cyclicals get a tremendously lower valuation. Putting this in perspective, I think, the semiconductor industry has gone from being viewed as growth to growth cyclical. And what that means to you in terms of how Wall Street views the industry is that you've gone from the luxurious position of getting capital when you want it, to you get capital when you can get it. And that means that you have to be more flexible in using debt and equity and it means that you get equity when you can and use debt when you can't. That is a difficult adjustment for an industry that has been viewed as growthy, but I would point out that at various stages in time, almost every industry has gone through this adjustment. It's not all that bad. It just means that you have to operate in a different manner.

I promised some more specifics: In looking at the near term, I predict that the market will go down until some time in November. That's an easy prediction. With the market down 32 today I don't feel that I've gone out on too much of a limb. The problem in a nutshell is that we face a problem with interest rates, and to some extent, a problem that you're very familiar with--earnings--and those have really gotten the stock market in a bind. One of the problems that you should be aware of is that thanks to our federal deficit we have a problem with financing about 28 to 29 billion dollars every 3 months, and in the past year, we have relied very heavily on the Japanese in order to do that. The Japanese have bought six to eight billion dollars of that 27- 28- 29-billion dollars that we issue every quarter. And we need them. And the Japanese, as you are well aware, are excellent traders. In front of every auction--and the next one comes up by the way the first week of November--the Japanese start making sure that people worry about whether they'll buy or not. And they spread a lot of stories about--you'll see it in the Wall Street Journal if you read the Bond Column--some reporter will ask someone from Namura or Daiwa or somewhere, "What's your interest in the upcoming auction?" and the spokesman will say, "Well, gee, I don't know. Our portfolio managers have actually been selling bonds recently." And that's usually good for a couple point corrections in the bond market. That started today, by the way. Japanese were sellers this morning--bond market's down a point. Then they will make sure that, through Namura or someone, they actually sell some bonds, which they will do through somebody that is very visible, like say, Solomon Brothers, who will tell just their 5,000 or 10,000 closest accounts that they have seen the Japanese actually selling bonds recently and that's usually good for another three or four points. And then at the last minute, Namura and Daiwa show up at the auction breathlessly buying bonds and then there's a rally. It's a very good game; they've made a lot of money at it, and that's sort of the point we've reached. Once a quarter where we have to go through this and that's one of the problems that we face, so don't expect any improvement in the bond market or, therefore, interest rates or the price you pay for money. Plus, additionally looking up to 1987, I suspect the bond market is going to be very concerned about the possibility of inflation coming back. The dollar's decline. Some early signs that pricing is bottoming--all are going to have the bond market terribly concerned. Keep in mind that bond investors, through the 70's, that are even worse than venture capitalists--they lost money hand over fist, time and time again. And they are very reluctant to repeat that experience, so the bond market is very jittery about inflation and will be very cautious about assuming that anything good can happen. So bond rates are going to hang up where they are and maybe even move a little bit higher.

We also have the uncertainty over the election coming up, and there's great concern among Wall Street types that the Senate will move to the Democrats, mainly because it changes committees and changes are generally viewed as negative on the Street. As a practical matter, after the initial uncertainty, there are two things to keep in mind. One is that Reagan really doesn't seem to have any more programs he wants done in the remaining two years of his term. So I'm not sure that the change of leadership in the Senate is particularly important. And the other is that to run for the Senate anymore, almost regardless of the place and the country, costs about $10 million dollars. And what that means is that Senators have to take money from everybody and tend to mellow out their positions, except in foreign affairs where, of course, no one knows what they're talking about, and you can get extreme positions on one side or the other. But on domestic issues, they tend to be very similar. And one thing to keep in mind about the election outcome, while you'll see a lot of this in the financial press, it's gotten down to the point where Senators really don't have a problem running on economic issues, because when you think about it, running for Senator means, on average, getting in front of about 100 people in a gymnasium and answering questions about being against deficits, and of course, your Senator is against deficits although he's got a couple of pet projects in the region that he'd like--but if everybody else saw it his way, there wouldn't _be_ a deficit. And, in fact, very quickly an interesting story that's told about the campaign trail is that a Senator in one of these gymnasiums had a reception line, and a guy comes through the reception line and says, "Senator, I think you're a crook," which unsettles the Senator to some extent. And the guy goes back and the Senator can't help but notice that this guy is mixing through the crowd, and then he comes back through the line again and he comes back up, shakes his hand, and says, "Senator, not only are you a crook, but I think you're stupid." Well, this has really got the Senator uneasy, and he can't keep his eyes off this guy as he's back out circulating through the crowd. He comes back up again, and this time he comes up and he says, "Not only are you a crook and stupid, but I don't think you should be re-elected." Well this has REALLY got to the Senator. Now we're getting to the heart of the issue. And the Senator turns to his host and he says, "Who is that guy that keeps coming back up here and saying these insulting things?" And the host says, "Oh don't worry about that guy. He's almost like the village idiot--he doesn't have a thought in his head. All he does is repeat what he hears other people saying." So that's what the Senator is afraid of: Not so much the issues, but what people might say about him. And he's pretty good on his feet in general. So Wall Street will worry about this issue, but it will pass, and by mid November we'll be ready to look at 1987.

1987 I believe will hold some better things in store for us. While I haven't given you much hope on interest rates and tax reform--which I should just mention in passing--does have some negative features for capital spending. One thing that I will say categorically on tax reform is that it will change. There is a classic problem with tax reform. The Treasury believes that they have raised $120 billion over five years from American business. American business, if you read through the newspaper or go to meetings, has got its tax gremlins working very, very hard to make sure that, company by company, they don't pay 120 billion dollars over five years. I'll bet on the tax gremlins on this one. Business won't pay $120 billion dollars which means there will be, in government terms, what's known as a revenue shortfall. Well, revenue shortfall in English means we need to raise taxes so in tax reform a very categoric statement I can make is don't hold your breath on tax reform; it will change as soon as 1987, and I assure you, by 1988 it will change. So let's just watch for the next wrinkle. Somebody is going to have to pay, and I suspect that members of this audience and myself will be included in that lucky group. And in 1987, thanks to the dollar having declined--and it will have some impact--but I think a very important word for 1987 is moderation. Things are going to get moderately better, but not dramatically better. The economy will get moderately better in 1987 and while the overall growth rate won't be a very impressive rate--probably 3 percent or less--there will be a little more of it coming from the industrial sector than has been happening recently or, in quite a few years actually, from the service sector. There will be some inflation in 1987. The dollar's decline is going to permit some price increases and you will start to see more and more pressure by the U.S. government on these NIC countries to allow their currencies to float up. We've already pressured the Koreans and they've allowed us how the Korean Wan is going to float up a little bit. So there will be a less price cutthroat type of environment, but the problem in explaining this and getting the right perspective so that you can plan your businesses is that cutthroat price competition doesn't go back till the pricing pressure is off. It's a little bit of easing of the pressure, so things won't be quite so bad, but it's not the complete reversal, either. So we're going to get some relief in pricing pressures. We'll have some inflation; we will see some economic growth; and that means profits will actually be up next year. One of the big problems for the stock market in the past three or four years is that while there's been great hope and promise of better profits, there's been no delivery. 1987 is the delivery year. And I believe that in looking out to 1987, we will see a modestly better stock market based on better profits, not better valuation, because of dropping interest rates. And here's the good part. The small stocks will rise again. The small stocks have been at a tremendous disadvantage to the currency gains put together by the large companies, and by the real fall off in the industrial sector that in many ways has gone through a recession. And investors turn to the more secure, the more viable returns, of the large multinational companies. Well, that's pretty much run its course, the value exists in the broader market or in the smaller companies, and in 1987, I think that the smaller cap companies will be a good place to be for investors and, therefore, for companies. And undoubtedly, an ideal opportunity to raise capital in smaller stocks after having had a very difficult period of time. So there's hope for 1987. It'll be a moderate year, a good transition year to better times, and hopefully 1988 looks even better after that. But to get the 1988 message, you'll have to invite me back, because I only do one year at a time.

Now we'll take some questions.

Question: How insulated is the Semiconductor industry from corporate raiders--unfriendly takeovers? Is this a reality that must be prepared for?

Answer: Most of the raider mentality, of course, has been based on the ability to take an asset and strip off parts without doing very much to it. And technology industries, because valuations still are so far above book value, tend not to lend themselves to that. Let me tell you that if the environment changes, the people decide they really need to incorporate semiconductors within their corporate environment and there is a market to strip business off, this will happen. I have recently heard more and more companies express the notion that in order to compete looking at three or four years, that they really need their own in-house semiconductor capability. If that really blossoms into convention wisdom, there will be a market. And once that happens, raiders become very much alive. So I wouldn't say that will happen soon, but it's something to keep your eyes on looking a couple years out. I should also mention, tangentially maybe, related to this is that in 1987 we will see in the merger and acquisition activity the interest will be coming from outside the United States. It will come from Japan or from Europe, because they're playing with much cheaper dollars. And they will especially be looking for technology or niche companies from both Europe and Japan, and of course the Japanese are moving more and more production onshore U.S. because of concerns about protectionism and this change in labor costs.

Question: Do you foresee any major changes in the financial structure or environment of the semiconductor industry similar to that occurring in the airline and the network television industries?

Answer: I think in many ways, if I can say this without insulting you, this industry is going to viewed by investors increasingly the way investors look at other growth cyclical businesses. And examples of that is the part that might insult you is that the airline industry, the paper industry, all of which are viewed as growthy except to vulnerable or economic or cyclical downturns, and those are what I would label as growth cyclical industries. And if you'll notice how these business operate, a very recent example, the paper industry is all of a sudden very fashionable because they've been able to show some improvement in operating rates and profits and the stocks move up and what happens? There's an equity offering just as sure as the world. Same in the airline industry. Soon as the stocks move up, United hits the market with an offering. That's part of what I was alluding to: you're going to have to hit the market for capital when the market's ready to give you capital, which may or may not be the time when you particularly think you want it. When I was a young cub analyst I wrote the definitive report on Whirlpool which in one of my 40 page conclusions was that Whirlpool didn't need any capital, that they could self finance. The report was killed because Whirlpool did a $50 million dollar debt deal, and through my embarrassment, I finally asked the management, I said, "I went through all this analysis and I proved you don't need the money." And they said, "Well, your analysis was 100 percent correct; we don't need the money, but we thought the market was right, and when we would need the money the market wouldn't be right, so we borrowed it now." So this goes way back, and that's going to be a way of life, I think, that you have to adjust to.

Question: Does Wall Street see the yen going low in 1987? Possibly down to 130.

Answer: I guess that there's no real consensus in our shop about the yen other than the Japanese obviously want the yen to stabilize around 150 and from there it really depends on what you think's going to happen to the Japanese economy. I have a strong suspicion that the Japanese economy has more problems than are currently perceived. And that the problem is simply that they were able to export with a yen that was priced well below its market, and whether this was the right price or not--because there's so many competitors right on their heels over in the Far East--I suspect that there's a transition period where Japan goes from being viewed as absolutely impossible to compete with to someone that is somewhat vulnerable--maybe a similar transition to what IBM is going through. At any rate, my guess is that the yen is pretty stable. Although there are people looking for 130 on the yen, I think that a year from now it'll be pretty close to 150.

Thank you very much.

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THE FUTURE OF THE SEMICONDUCTOR INDUSTRY; AN INSIDE VIEW

Robert N. Noyce
Vice Chairman of the Board
of Directors
Intel Corporation

Dr. Noyce is a cofounder of Intel Corporation where he presently serves as Vice Chairman of the Board of Directors. He was codeveloper of the silicon-gate MOS process, which enabled Intel to produce the first high-density memory components and the first microprocessor. Prior to forming Intel, he helped found Fairchild Semiconductor Corporation. While at Fairchild, he was responsible for initial development of the firm's silicon mesa and planar transistor product lines. Dr. Noyce also coinvented the integrated circuit. Earlier, he worked at Shockley Semiconductor Laboratory and Philco Corporation. Dr. Noyce graduated from Grinnell College with a B.S. degree in Physics, and was elected to Phi Beta Kappa. He earned a Ph.D. in Physical Electronics at the Massachusetts Institute of Technology.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
October 20-22, 1986
San Diego, California

DATAQUEST SEMICONDUCTOR CONFERENCE

October 20,1986

THE FUTURE OF THE SEMICONDUCTOR INDUSTRY: AN INSIDER'S VIEW

Dr. Robert N. Noyce, Vice Chairman, Intel Corporation

Today I'd like to talk to you about the future of the U.S. semiconductor industry. That's a hot topic lately, considering all the prophecies of doom we've been hearing. And let's face it---fortune tellers have always had a rough time of it. It wasn't too long ago that you could be burned at the stake for looking ahead into the future, so I'd better watch my step.

Anyone can make predictions, but it's another matter to make the right ones. It's like the story of Cassandra, the Trojan princess to whom the gods gave the ability to foretell the future. Unfortunately for her---and the Trojans, for that matter---the gods also determined that although everything she would predict would come true, no one would ever believe her. So when the Trojans dragged the famous wooden horse inside the walls of their city, Cassandra stood on the parapets, tearing at her hair and screaming that all was lost---but no one listened, and Troy was sacked.

Hopefully I won't have as difficult a time getting my point across as Cassandra did. For some time, many of us in the industry have been saying that we should beware of Japanese bearing gifts---gifts like underpriced components, for example. Only recently have the warnings been heard, and only after a great deal of damage has been inflicted.

Our biggest enemy has been the apparent willingness in this country to allow things to reach the point they have. As much as anyone, we have ourselves to blame. We have yet to really address the deficiencies we face. We have lost a big battle, and need to regroup to win the peace.

But now that we're finally getting some of the attention we deserve---that critical mindshare---we should be able to do something to stem the tide. It's like combatting an addiction; the hardest part is admitting you're hooked. After that, you're ready to change and get on with the process. Well, people are facing the hard facts. And now that it's fashionable to jump on the "doomsday bandwagon," I feel it's important to look at the other side of things. I believe that the pendulum will swing back again as equilibrium is re-established.

The essence of my message is this: That which cannot happen, will not happen. The United States cannot continue to consume more than it produces, borrowing heavily to finance imports. We can't survive by service industries alone; along with primary industry, some manufacturing industries must be robust enough to export and pay for the goods we import.

The most likely candidate is the high technology sector, whether it be semiconductors, computers, biotechnology, or whatever. And the reason is quite simple: the leading edge of high technology has become perhaps the greatest resource that this country now possesses. Semiconductors are an example of that national resource. They form the central nervous system of modern industry, from computers and telephones and factory machines to car engines and coffee pots. There is simply too much at stake for us to let the semiconductor industries go the way of the television industry in this country.

There are two major imbalances in the U.S. economy which have affected our industry negatively. First of all, as I mentioned briefly, we consume more than we produce. Because of that, we import more than we export, and we are running unprecedented trade deficits. Second, we ask others in the global community to save for us, and then we turn around and borrow their savings and fall deeper into debt. For a nation that spends more than it earns, borrowing is the only short term answer---but eventually, the debt must be repaid by exports.

There are many indicators of America's weakening position. For example, growth has been a meager annualized 1.2% since 1960, trailing well behind Japan's 5.9%. The rate of return on American manufacturing investment reflects our dismal productivity performance and high cost of capital. Over the past 20 years, investment yields in manufacturing have fallen from 12% to 4%. And the 2% annual growth rate of the standard of living in this country since 1960 leads only Great Britain when compared to that of the major countries in the free world.

It starts to sound as though the prophets of doom have a pretty good argument going. But eventually, the laws of economics decree that these imbalances will even out. The dollar will drop and the yen will rise to restore equilibrium. The more the Japanese export to us, the greater a hole they will dig themselves into. The bottom of that hole represents the declining value of the dollar. Conversely, the goods exported to the U.S. are a growing pile whose top represents the increasing value of the yen. The higher that mound, the deeper the hole gets. And that makes it all the easier for us to start shovelling goods back into the hole and increase our export activity. As the gap widens, it makes it that much more difficult for the Japanese to export to us.

The hole is getting deeper every day. In time, that will drive the yen up to where Japanese goods are too expensive to buy. We can talk until we're blue in the face about the need to enforce our trade agreements with the Japanese, but they will live up to those agreements if they perceive them to be in their best interests. If they continue to drive up the surplus, they will eventually be the instrument of their own undoing.

The Japanese have countered those pressures that increase the value of the yen by loaning their surplus back to us. But as the dollar falls and the Japanese receive fewer yen in return....well, it's simply a bad deal for them, and it can't continue. That is economic reality.

Now, I know what you're thinking: what does this have to do with the plight of the semiconductor industry? The answer is everything. As the scales begin to tip toward a position of balance and we are once again able to increase our exports, those of our industries that are stronger relative to other domestic industries will be the ones doing that exporting. And that is the crux of my argument: OUR INDUSTRY IS STRONGER WHEN COMPARED TO OTHER INDUSTRIES IN OUR COUNTRY. AS LONG AS IT CAN MAINTAIN OR ENHANCE THAT POSITION, IT WILL PROSPER IN THE LONG TERM.

All else being equal, those industries that are less competitive globally will fail before high technology does in this country---we're talking about survival of the fittest here. Although the domestic semiconductor industry must of course compete with its counterparts in the rest of the world, it must also be better than other U.S. industries. And right now, it definitely is.

It all boils down to barriers that prohibit market entry. If you're looking at industries that could go under in this country, look at relatively low technology, low efficiency industries. They're the ones that can be more easily duplicated offshore. It's much easier for an emerging nation to penetrate markets based mainly on high labor content than it is to gain a foothold in high technology, which requires a sophisticated and dedicated infrastructure. It takes a tremendous amount of capital, both physical and intellectual, to successfully straddle the leading edge. And that takes time. Simply put, we have a head start over the rest of the world. It's possible for a nation to make rapid progress when, like Japan, it skews its entire system to succeed in high technology. But I think that's the exception rather than the rule.

American industry spans the spectrum from low tech, low efficiency to high tech, high efficiency. We will still be most vulnerable to imports in the low efficiency sector when the trade balance shifts. The high efficiency industries---of which the semiconductor industry is one---have a relative advantage. They will comprise our exports as the balance shifts. Notice that our waterline, so to speak, will shift up or down the efficiency scale depending on the value of the dollar. But everything ultimately remains relative. The real dividing line to be concerned with here is the vertical axis that separates high and low efficiency industries.

We in the semiconductor industry must maintain that relative advantage over other domestic manufacturing industries. Or as Patton said during World War II: "Make the <u>other</u> S.O.B. die for <u>his</u> country." It all reminds me of the old story about the two guys who are running away from the bear. One of them stops suddenly to put on a pair of running shoes, and the other one turns to him and asks, "Don't you know you can't outrun a bear...?" To which the first guy replies: "You don't understand...all I have to do is outrun you!"

Economic strength has always been measured in large part by <u>natural</u> resources. Raw materials, sources of energy---these were the factors that once dictated what a society's potential was. And that was one of the most significant reasons for the rise of the United States as a world power. We had an abundance of resources to draw from, and our innovative ability and increasing technical skills enabled us to develop the potential of those resources.

And now, we find ourselves at a point in history where our ideas and technology have become even more of a resource than our natural materials. The ability to employ those ideas and technology in our society will ultimately determine the future of our economic well-being. The United States is still unquestionably the science center of the world. Most of the innovations come out of our laboratories, and the initial use of those innovations occurs here at home.

But things aren't going to straighten out without some serious efforts on our part. We've neglected manufacturing over the years---which is ironic, because after World War II we were the unquestioned manufacturing leaders. But now we must learn to produce better, to feed both our consumption needs and those of the world. That's true, of course, across all industries, and not just semiconductors. The U.S. cannot succeed as an economy weighted too heavily toward service industries. We can't survive simply by opening up restaurants or turning out more doctors and lawyers---I only wish we could use them as an export crop!

Better manufacturing capabilities are within our grasp. When we finally realized that the Japanese had gained the edge in semiconductor manufacturing, we started to do something about it. You might remember all the fuss a few years ago surrounding the quality of our semiconductor products when compared to that of the Japanese. There's no question that Japan was better for a while, but we put our minds to it and corrected the problem.

Today, our quality is equal to theirs---people now acknowledge that fact, isolated reports to the contrary. Our industry is taking real steps to improve manufacturing efficiency, productivity, and quality in this country so that we can compete. I know we've made some great strides at Intel over the last few years, and I think that's true at many other domestic semiconductor companies. We've dramatically increased our automation and equipment utilization, and consequently we're running our factories much more efficiently. It's a good start, but we're going to get even better---and that's because we've finally focused our attention on that goal.

If we don't increase our productivity, it will be reflected in a lower standard of living for Americans. Given the status of the "good life" in this country, no one would ever willingly allow that to happen. It would go against the grain of what we've all worked for over the course of many generations. But that reality will be forced upon us unless we increase our productivity.

No matter what course of action we take, there is a short-term problem we'll have to deal with. While I believe there is hope down the road, the next few years promise to be difficult. It takes time to effect the changes that are necessary. Everyone talks about the advantages the Japanese enjoy because of their basic structure---greater savings and lower cost of capital, government backing, and so on. By the time our nation, our government, and our industry are able to make the changes necessary to really stem the tide, the shakeout will have claimed a number of victims. I don't think there's any way around that.

The bad times for our industry will continue until all the excess capacity reaches a state of equilibrium, just as with the import/export balance. We will all do whatever is necessary to survive until that point is reached, but not everyone will succeed. Those that will suffer will be the companies that don't have pockets deep enough to absorb the interim losses. For now, it's like gambler's ruin; you keep doubling your bet until the other guy runs out of money and has to drop out.

I think it would be ludicrous for anyone to suggest that we can go back to the way things were during the infancy of our industry. Things changed quickly then, and new technology was enough to assure a profit. Those days are over. There will be a lot of blood spilled, and a lot of companies scrambling to the safety of niche markets. But those that remain standing will be the stronger because of it.

The stakes are too high for us to fail. I think our government and our people are beginning to realize this. The number of studies concerned with the issue are growing rapidly---the first ones by the government, if you'll remember, were only initiated a few years ago. But I suppose that's understandable; you don't need to worry so much about strategy when you're winning, because you must be doing something right. We won for so long that we simply got spoiled.

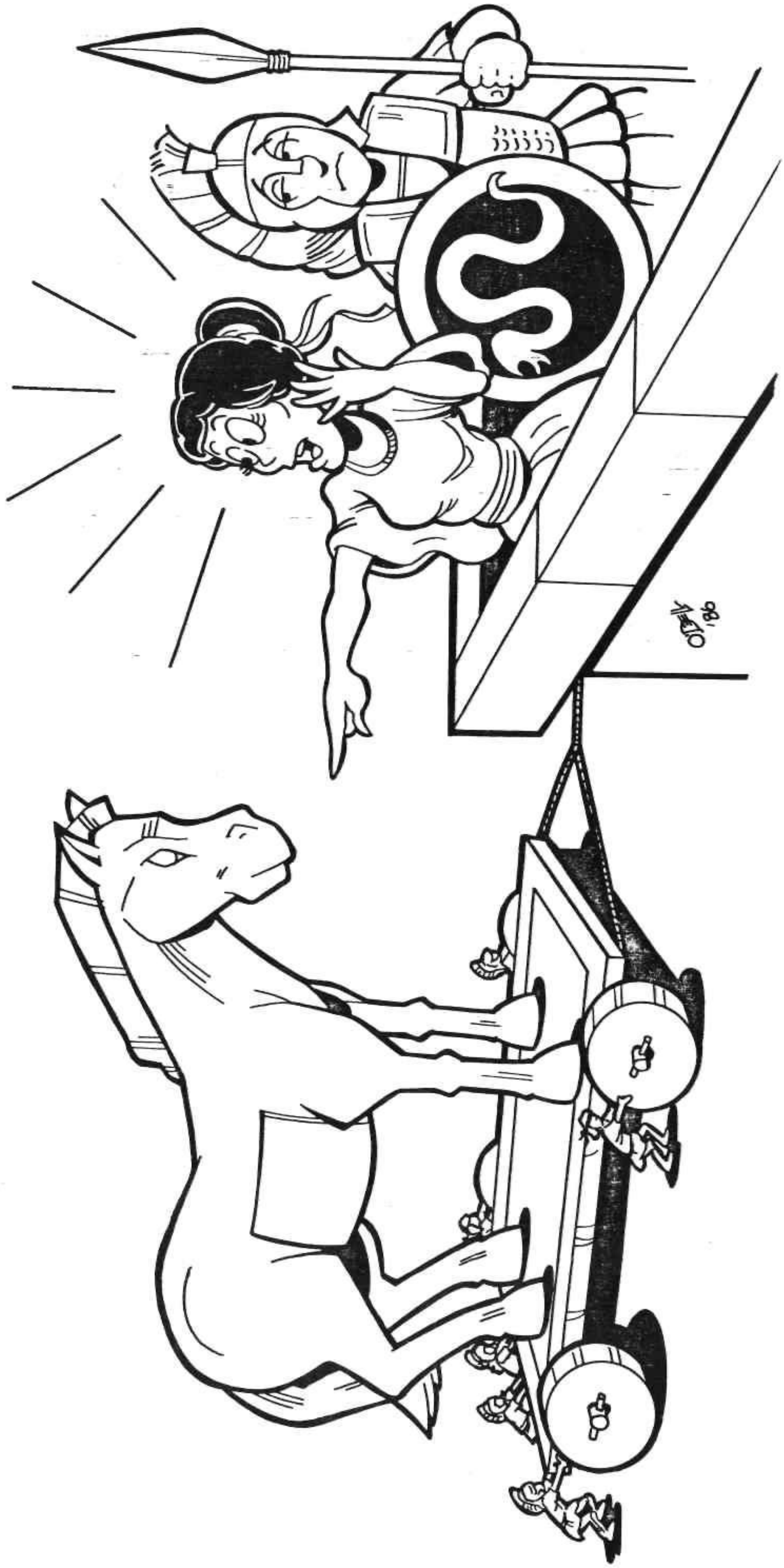
But the problems facing us can be solved. We're already taking many of the actions that are necessary to regain our advantage. Cooperative alliances between our major companies are forming. Projects aimed at the greater good of our society are beginning to gain favor, such as national research based on industrial and economic needs rather than military ends. Our major semiconductor companies are working harder than ever to be the vendors of choice in their respective markets.

So don't immediately throw your lot in with the prophets of doom. It's too easy to play the cynic in the face of current adversity. I predict, contrary to what a lot of people are saying, that by 1991 our domestic semiconductor industry will be strong. Now that the battleflag has been raised, I think we'll finally start to see some results.

The cries of Cassandra are being heard. And while the siege may continue for a while, the tide of the battle is turning in our favor. We will keep the American semiconductor industry vibrant and whole.

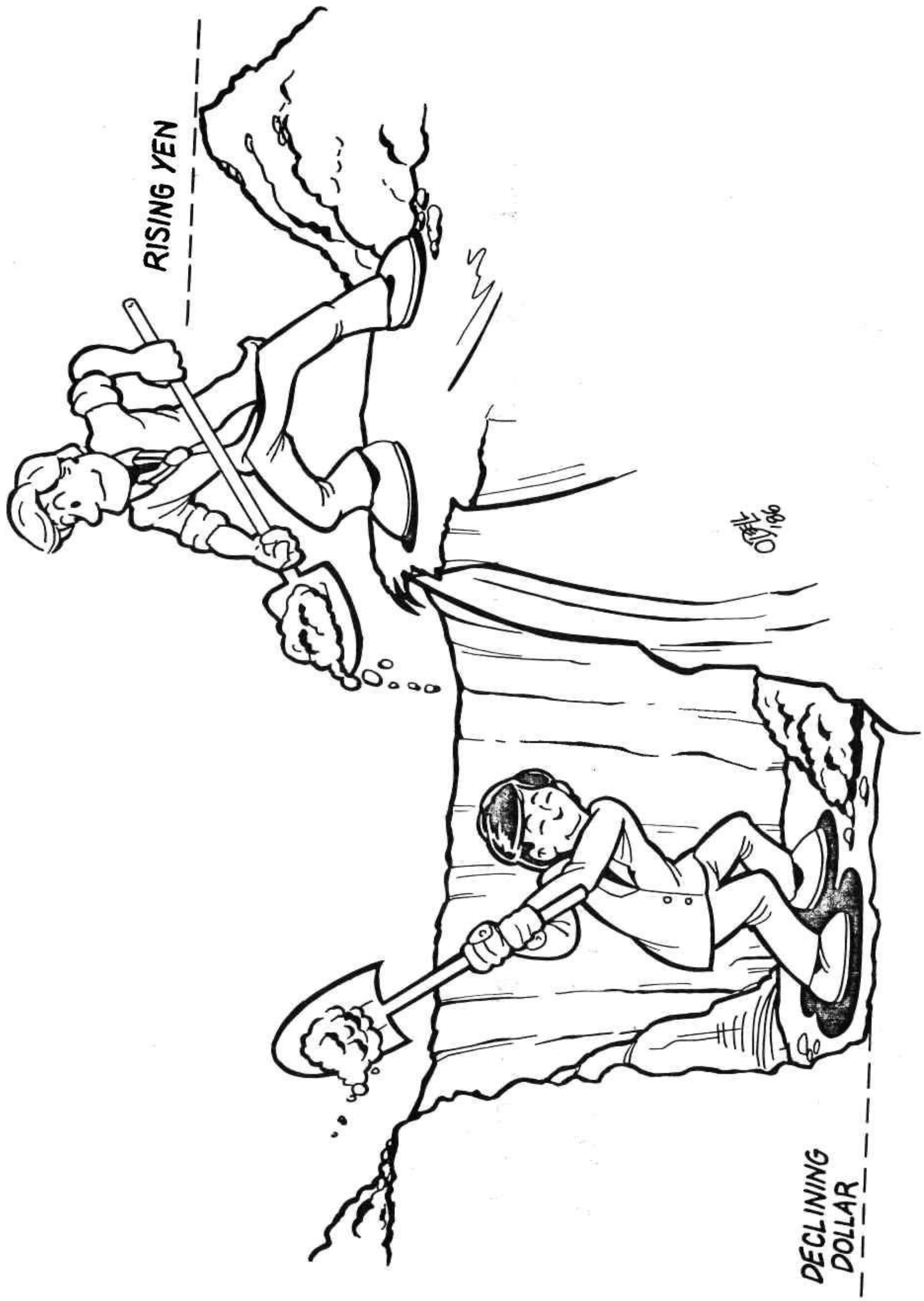
Or, to paraphrase the poet Homer one more time:......we will keep our legacy intact as the place that launched a thousand chips.

Thank you.



Imbalances in the U.S. Economy

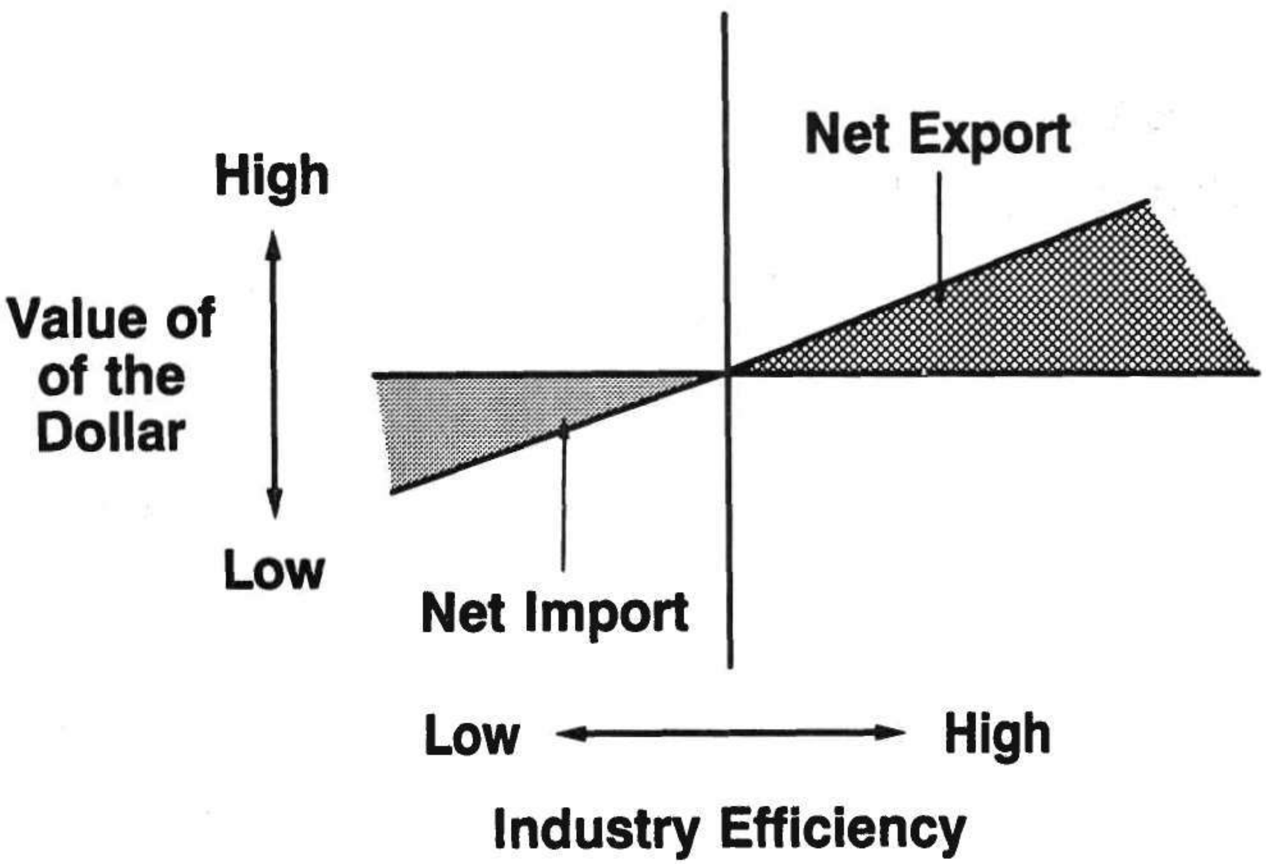
- We Consume More than We Produce
- We Do Not Save ... We Borrow Others' Savings

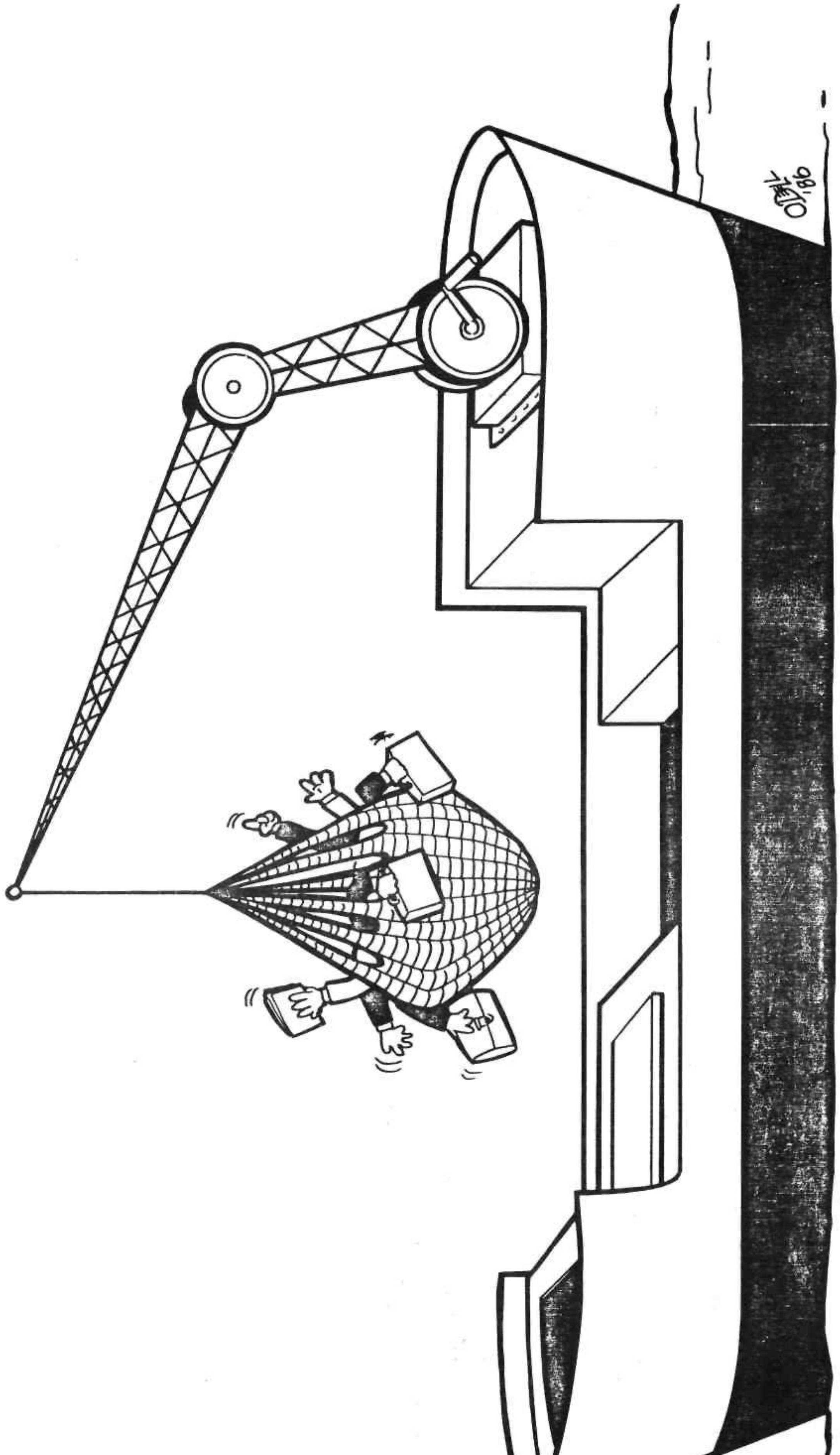

RISING YEN
DECLINING DOLLAR

Economic Relativity

- Trade <u>Will</u> Balance
- Stronger Industries Will Increase Exports as Trade Comes into Balance
- The U.S. Semiconductor Industry Is Strong Compared to Other Domestic Industries

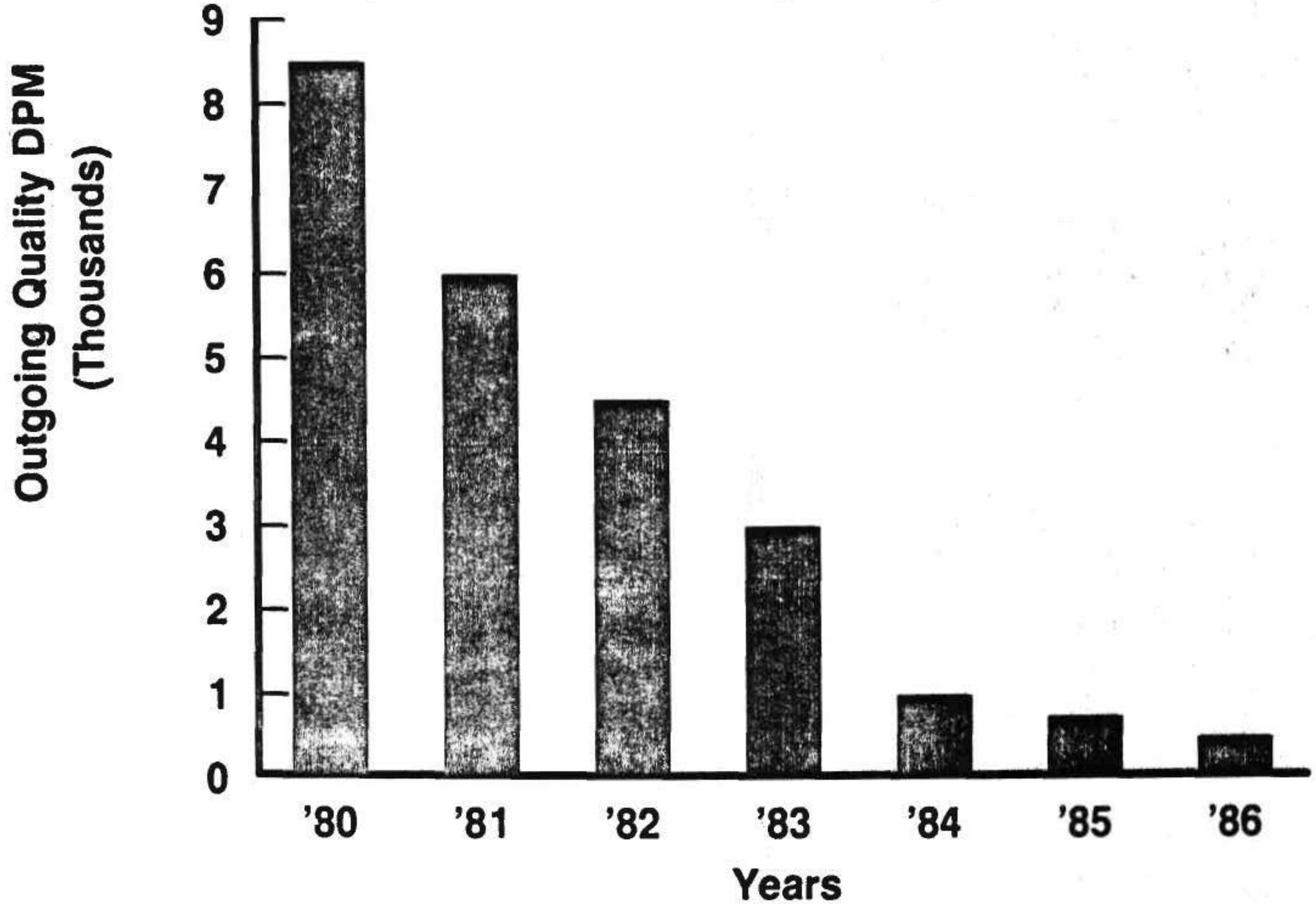
Who Will Export?

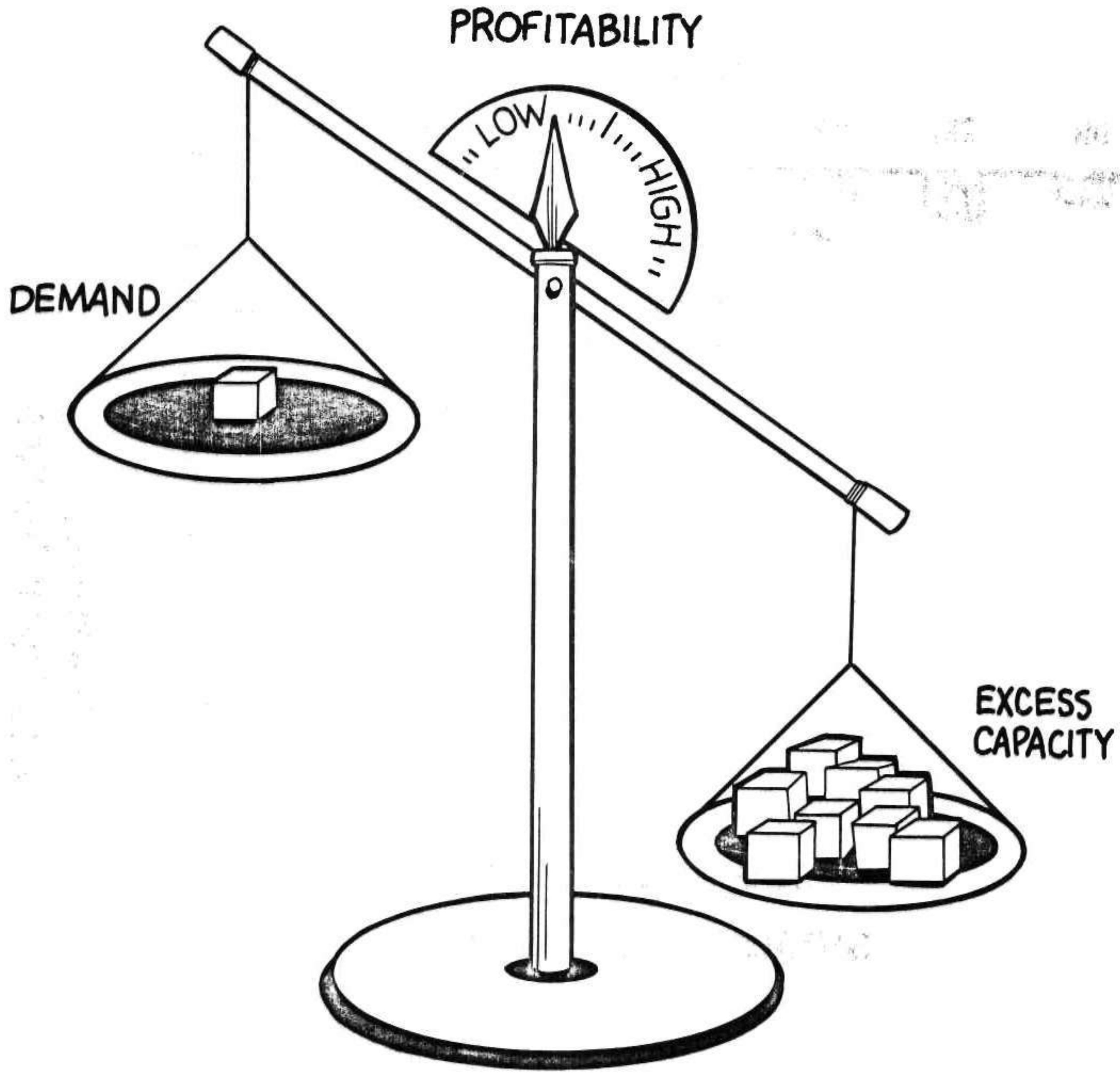




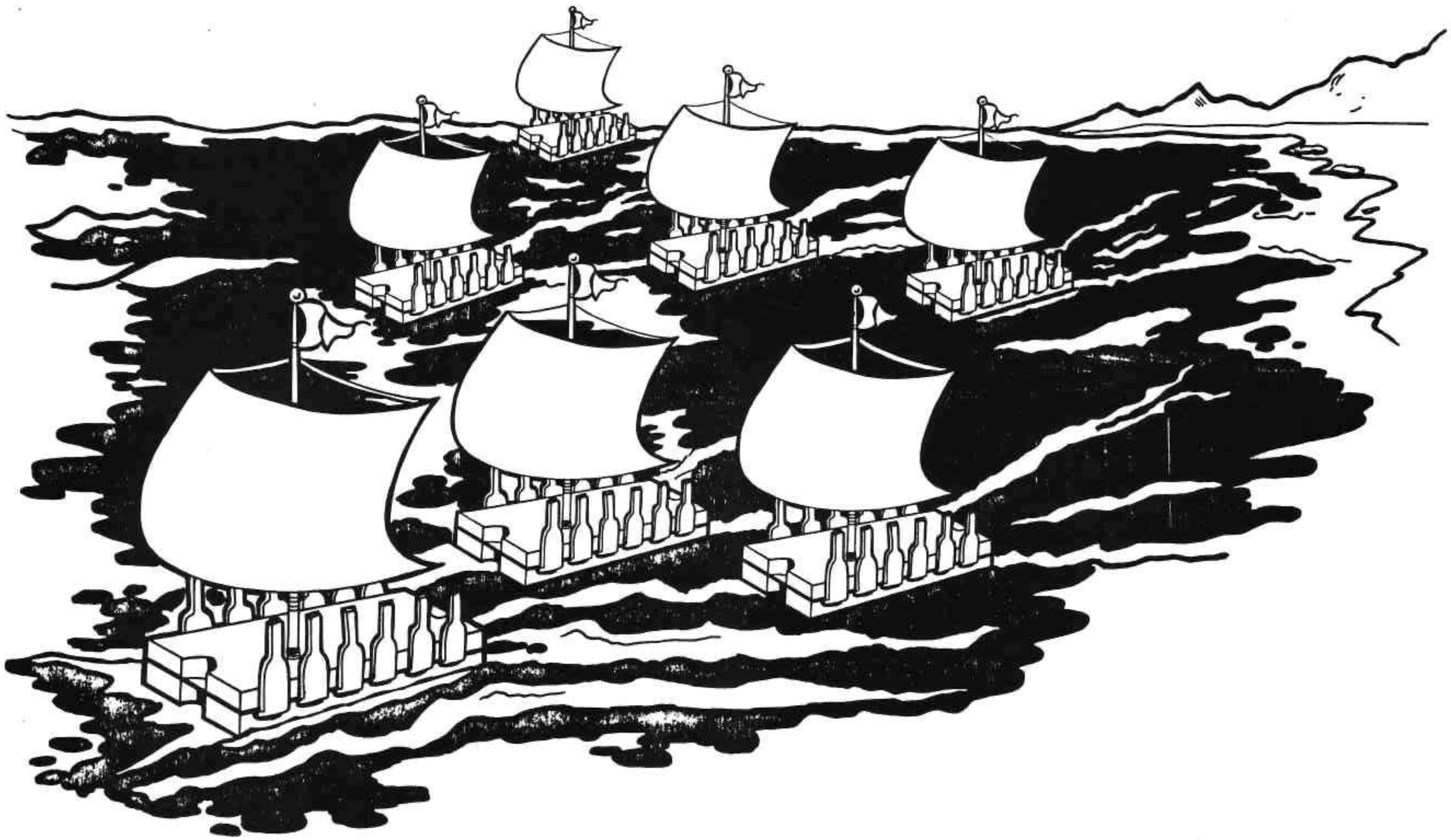
Component DPM Levels

(Customer Perceptions)




PROFITABILITY
LOW
HIGH
DEMAND
EXCESS CAPACITY

The place that launched a thousand chips...



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SEMICONDUCTOR APPLICATIONS IN A GLOBAL ENVIRONMENT

Wilfred J. Corrigan
Chairman and CEO
LSI Logic Corporation

Mr. Corrigan is Chairman and Chief Executive Officer of LSI Logic Corporation. Prior to joining LSI Logic, he was President, Chairman, and Chief Executive Officer of Fairchild Camera and Instrument Corporation. Earlier, he held a series of management positions at Fairchild. Previously, he was Director of Transistor Operations at Motorola Inc.'s Semiconductor Products Division in Phoenix, Arizona. Mr. Corrigan graduated from the Imperial College of Science in London, England, with a B.Sc degree in Chemical Engineering.

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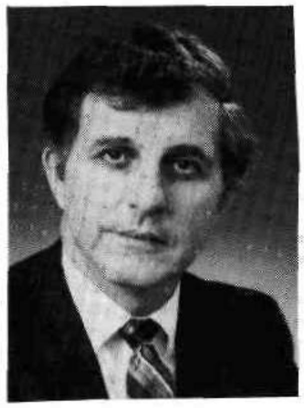
(THIS SPEECH WAS NOT AVAILABLE AT TIME OF PUBLICATION)

THE MERGING OF ANALOG AND DIGITAL



James M. Smaha
Executive Vice President
National Semiconductor
Corporation

Mr. Smaha is Executive Vice President, head of the Semiconductor Group, and a member of the Board of Directors of National Semiconductor Corporation. Previously, he was Vice President and General Manager of National's Semiconductor Division. Other earlier assignments included Vice President of the the Logic Group and Director of Digital Integrated Circuits. Before joining National, Mr. Smaha held management positions in linear and digital bipolar operations at Fairchild Semiconductor. He received a bachelor's degree in Mathematics from the University of Maine.

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October 20-22, 1986
San Diego, California

James M. Smaha

Executive Vice President

Semiconductor Group

National Semiconductor

THE MERGING OF THE DIGITAL AND ANALOG WORLDS

CHALLENGES AND OPPORTUNITIES

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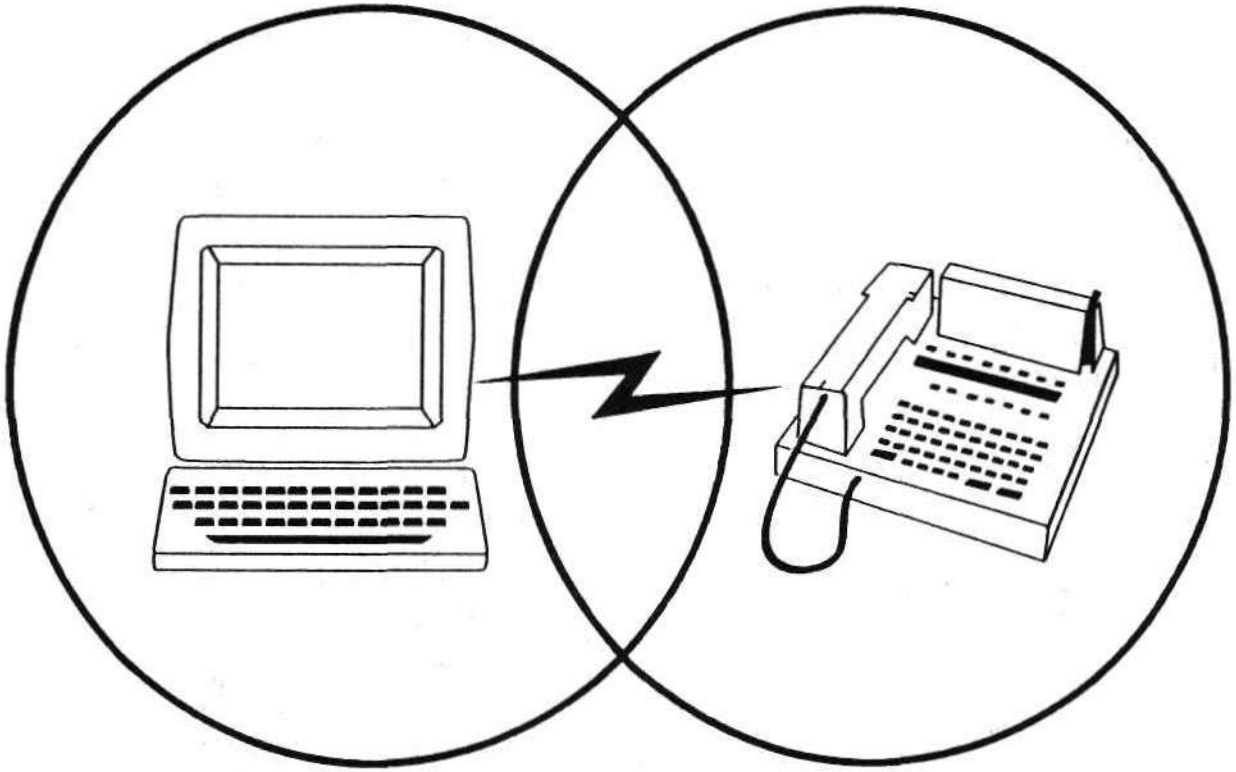
MERGING



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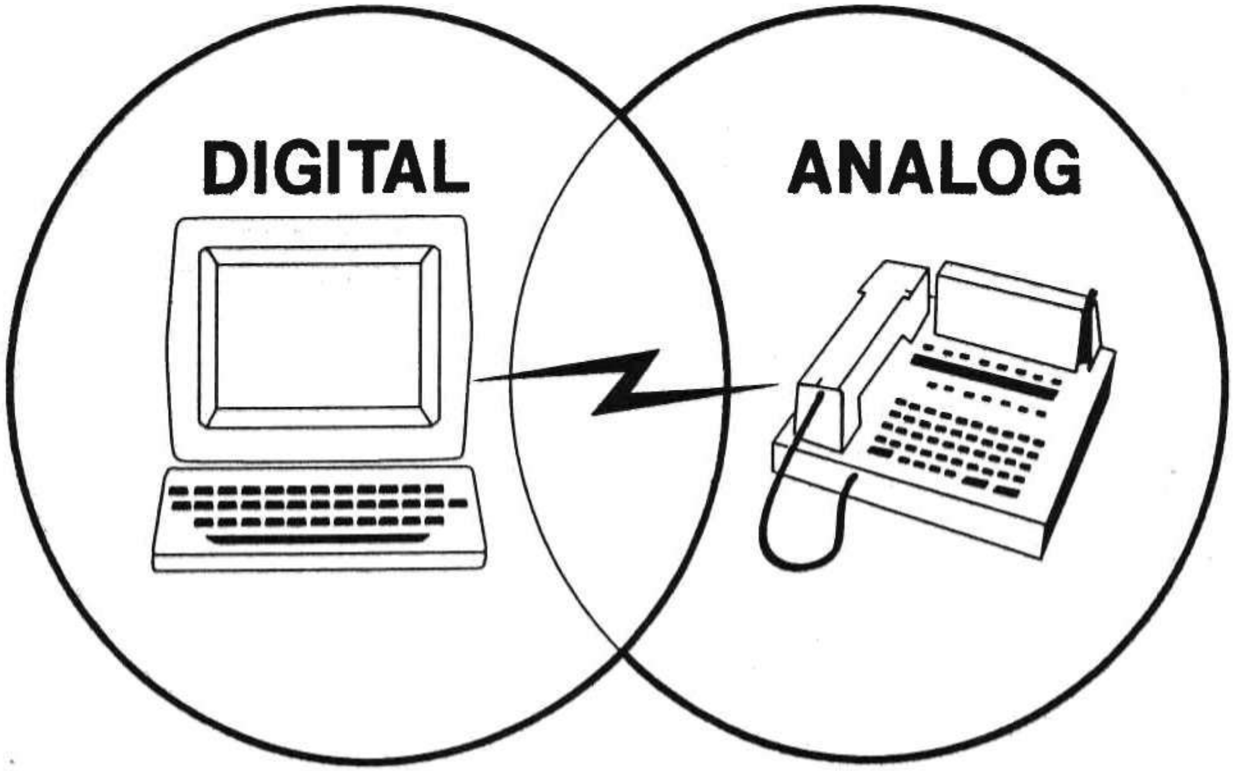
MERGING



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ISSUES IN MERGING

- Nature of merger
- Challenges
- Opportunities

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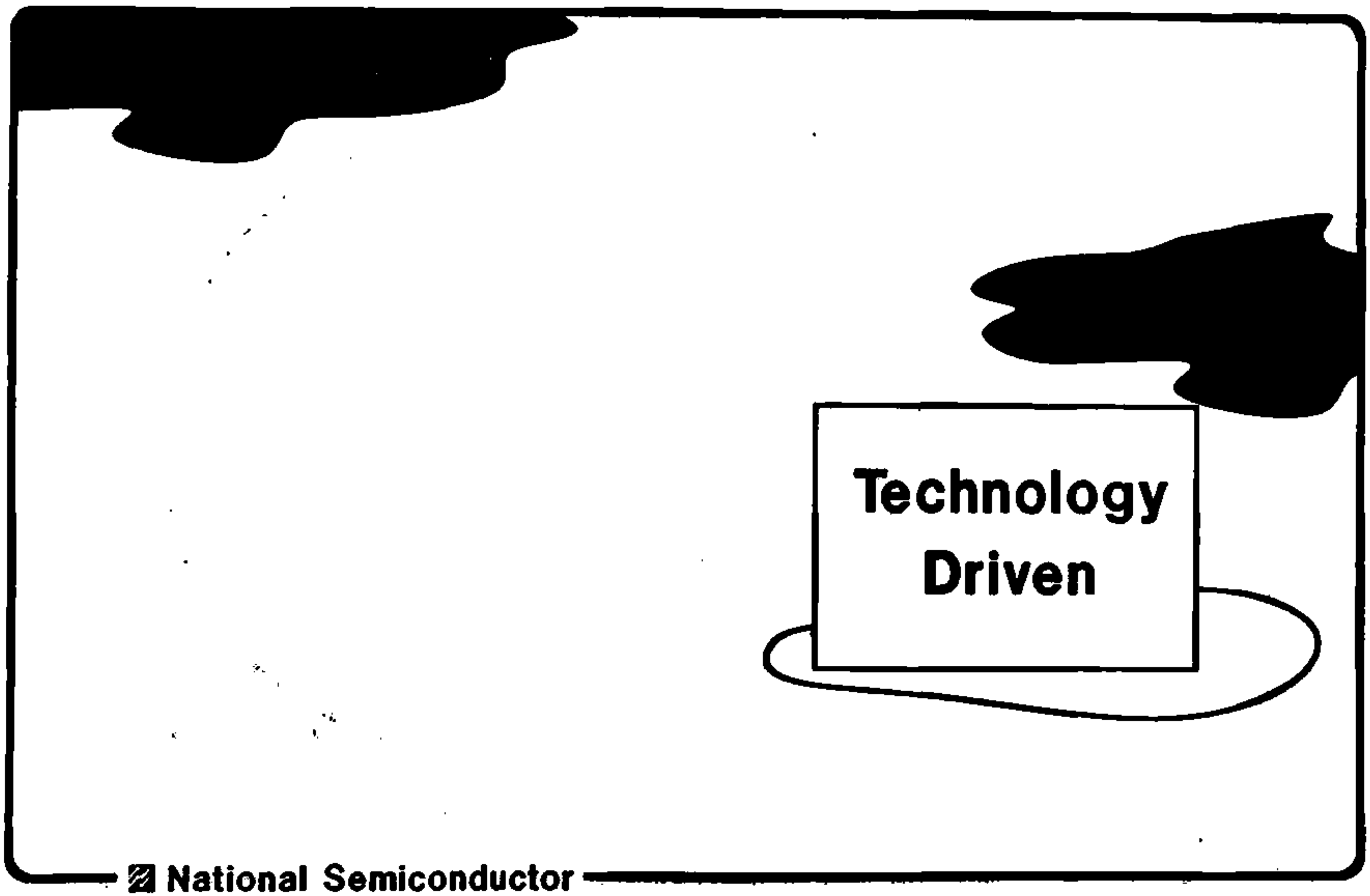
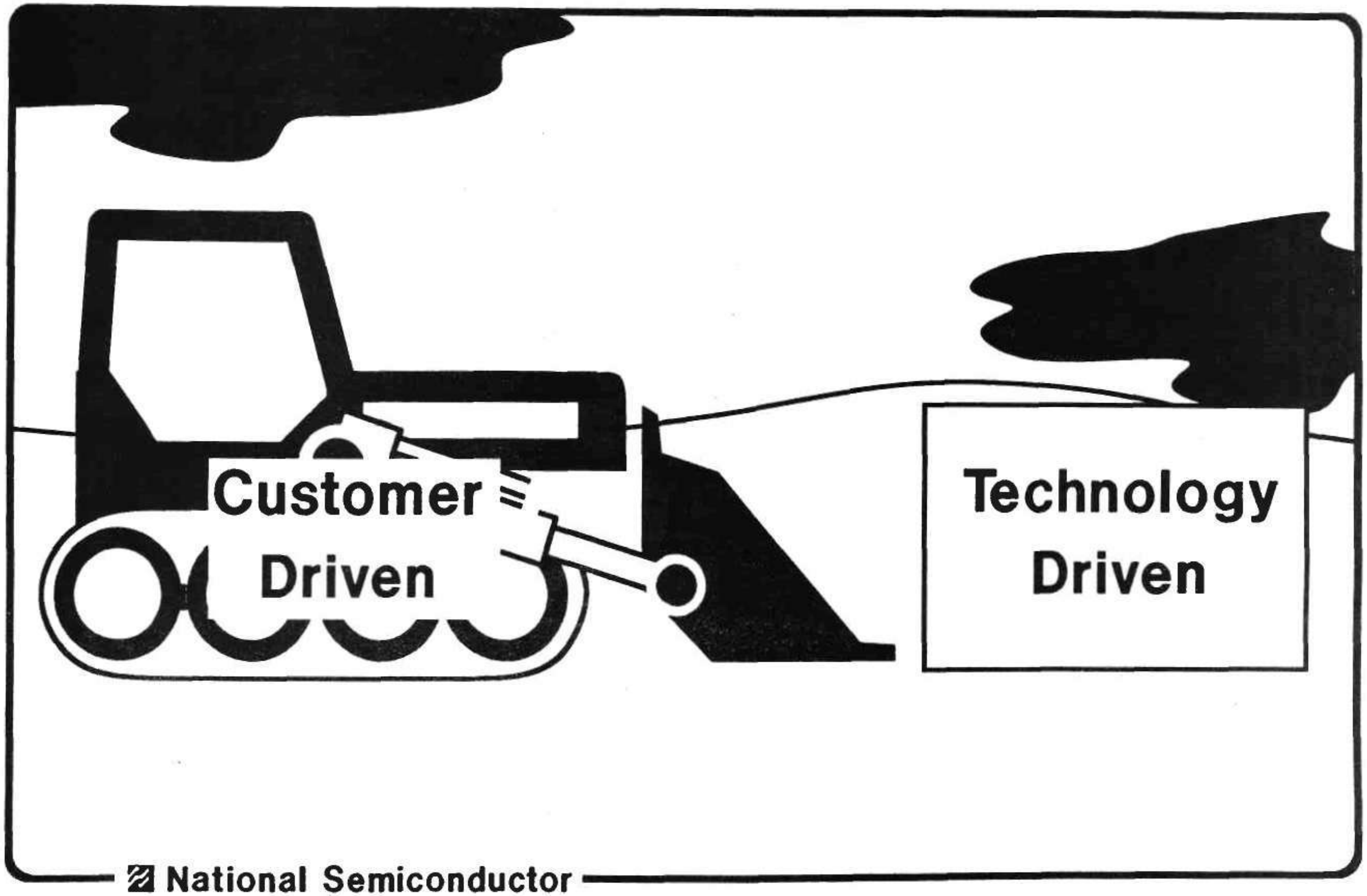

Technology
Driven
National Semiconductor


Customer
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Technology
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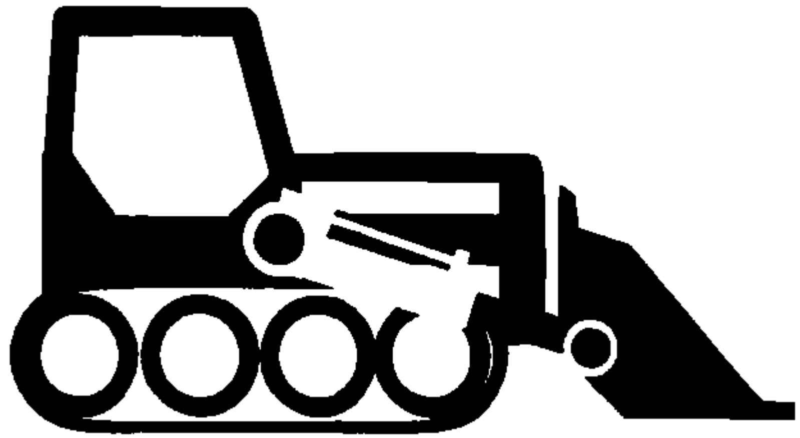
National Semiconductor

Customer Driven



- Complex, proprietary products
- Systems solutions
- Partnerships

National Semiconductor

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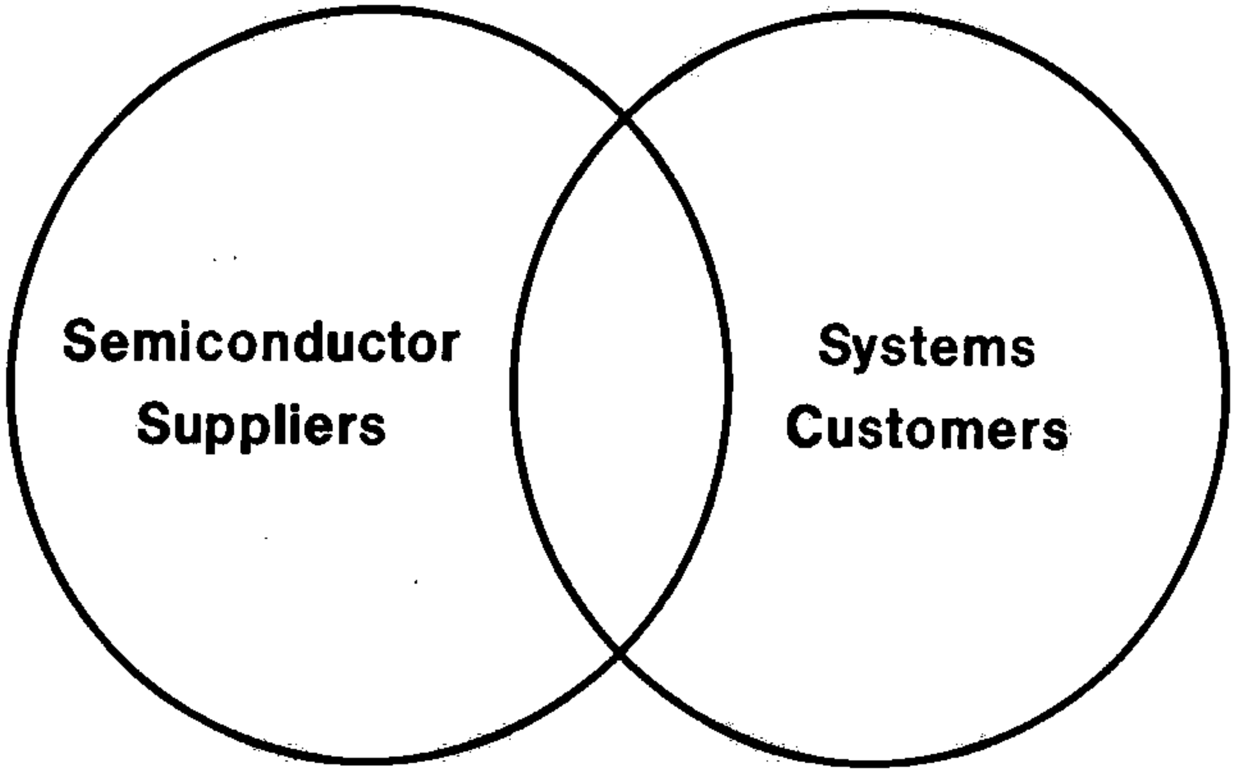
MERGING



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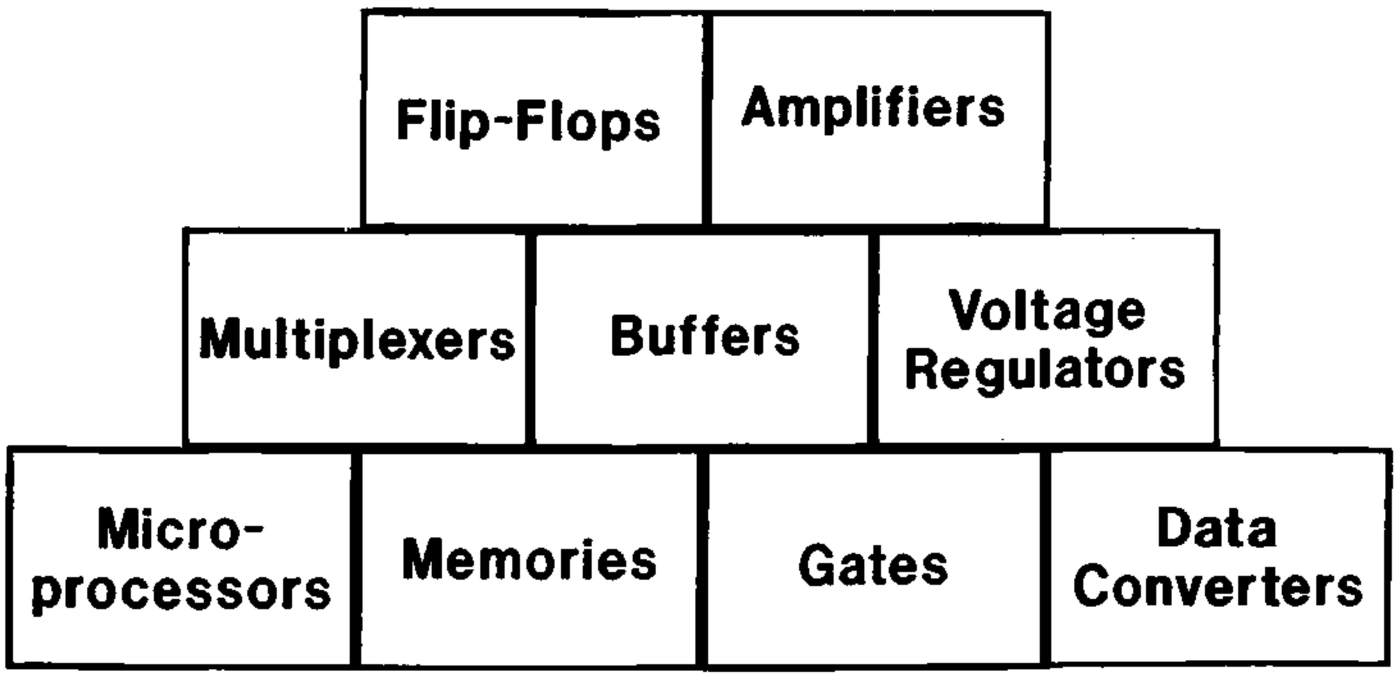
BUILDING BLOCKS



SYSTEMS SOLUTIONS

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ANALOG
REMAINS LINK
TO REAL WORLD

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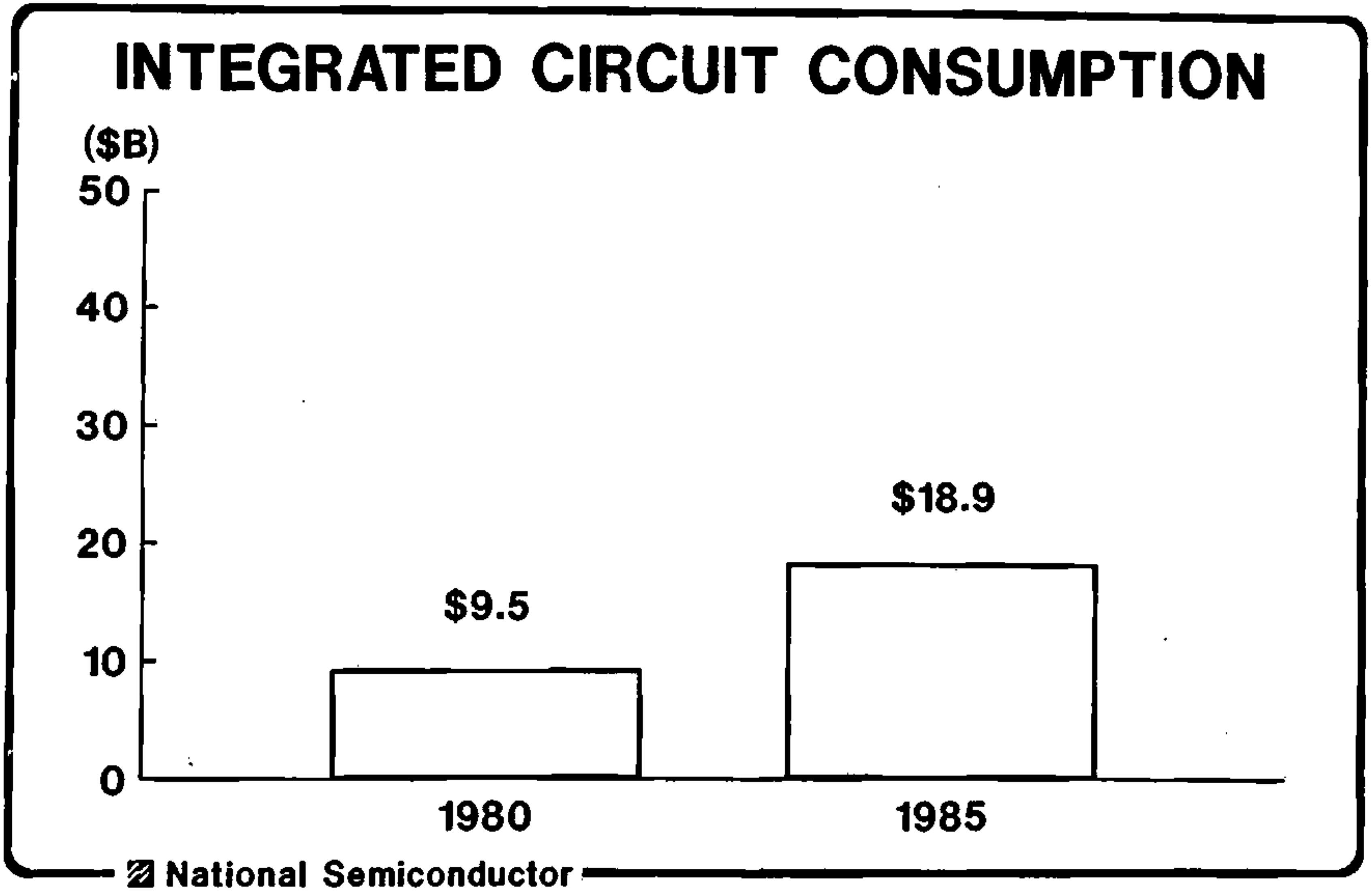
INTEGRATED CIRCUIT CONSUMPTION
($B)
50
40
30
20
10
0
$9.5
$18.9
1980
1985
National Semiconductor

INTEGRATED CIRCUIT CONSUMPTION

Compounded Annual Growth Rate

1980 to 1985	Digital	14.8 Percent
	Analog	14.2 Percent

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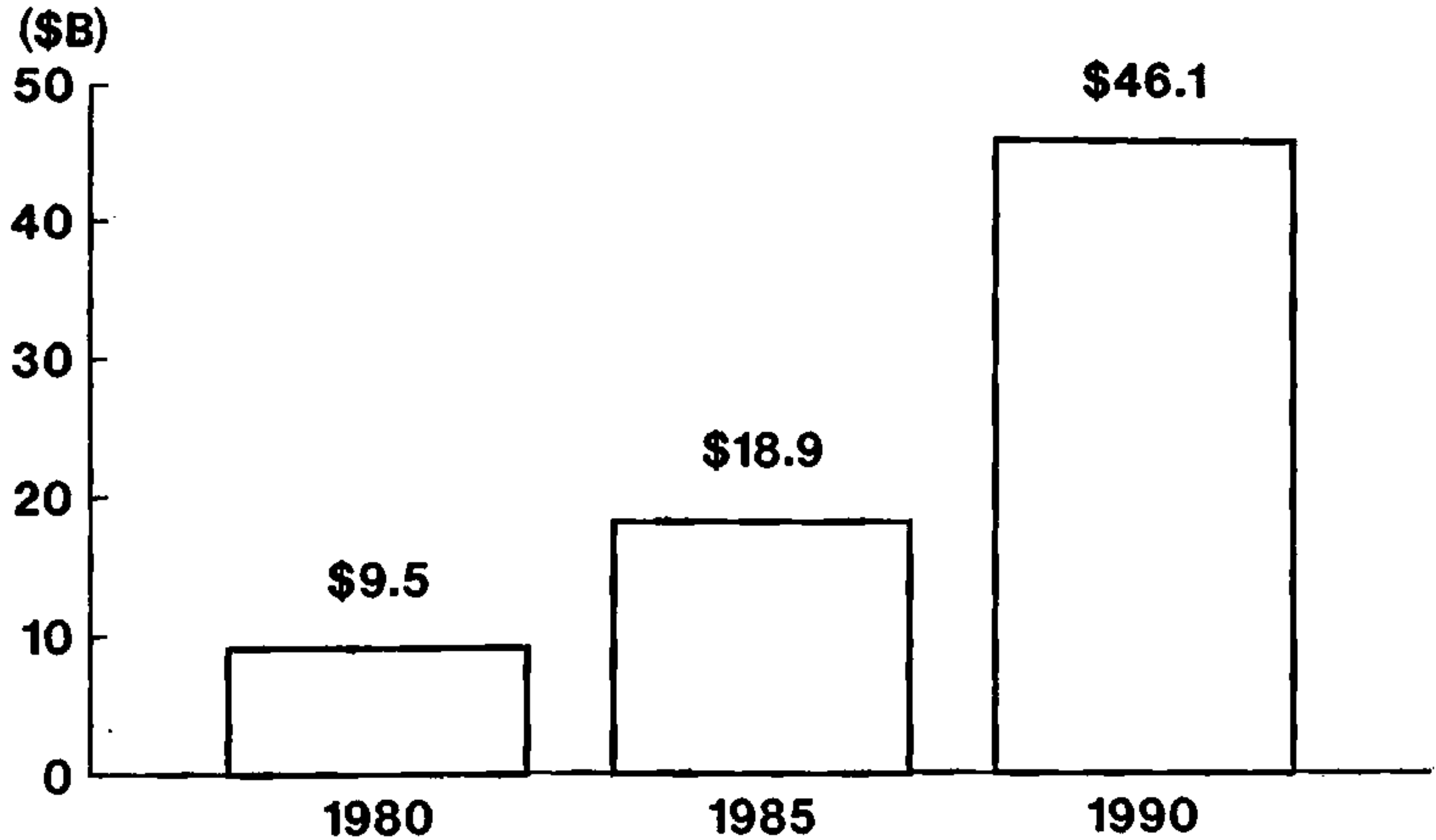
INTEGRATED CIRCUIT CONSUMPTION



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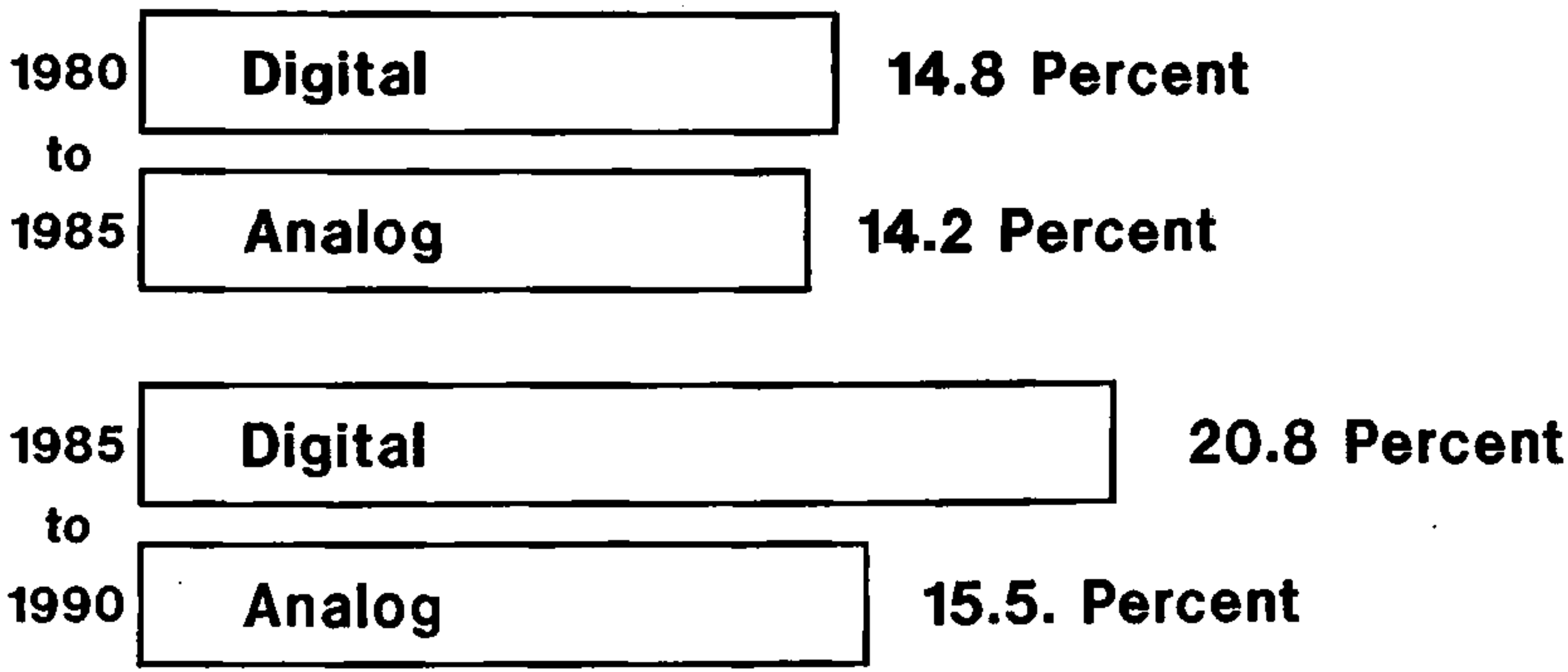
INTEGRATED CIRCUIT CONSUMPTION

Compounded Annual Growth Rate



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TOTAL IC MARKET

1985

Analog	25.3 %
ASICs	24.3 %
Memory	23.7 %
Microprocessor	14.6 %
Other	12.1 %
Total	100.0 %

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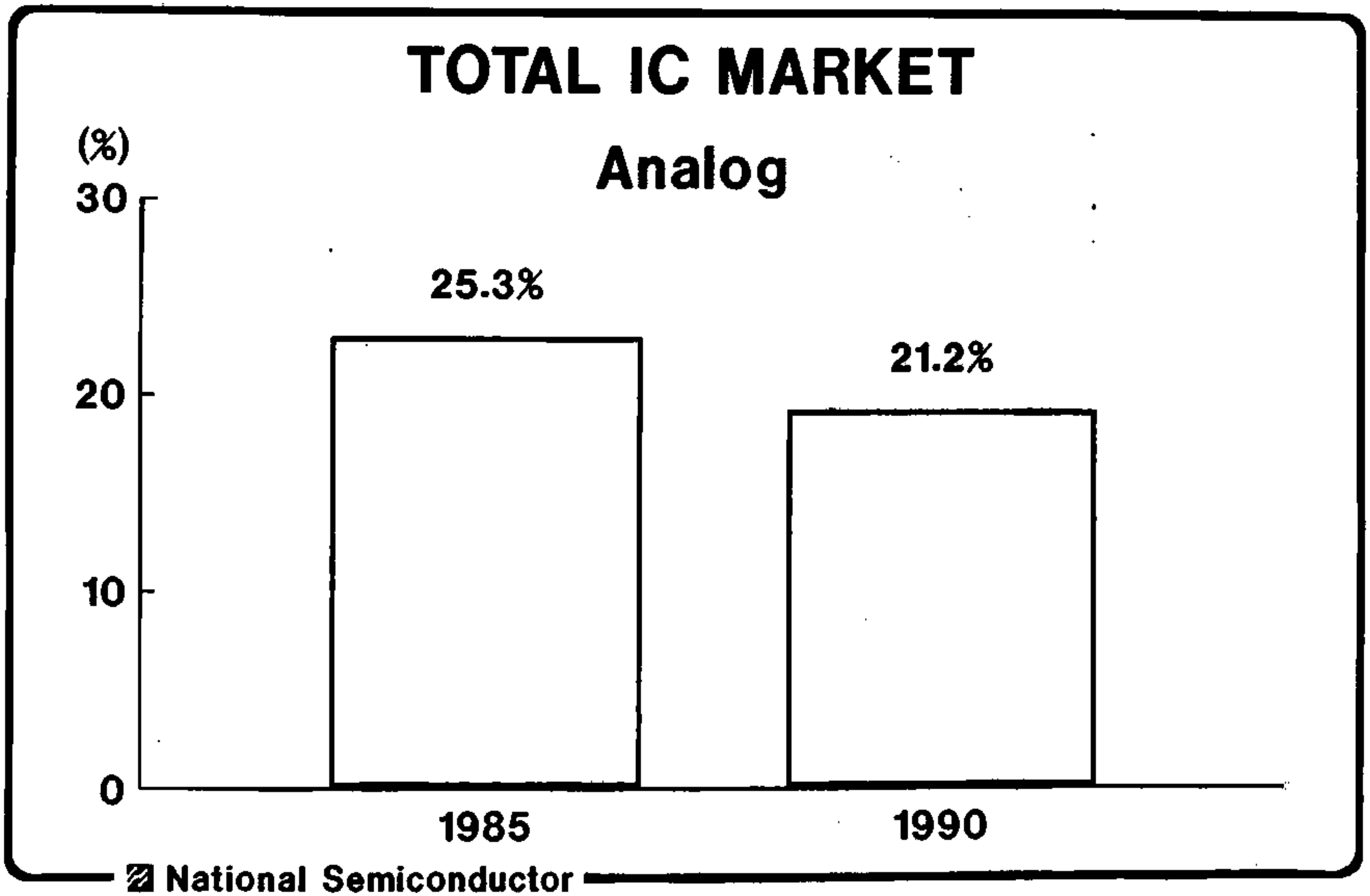
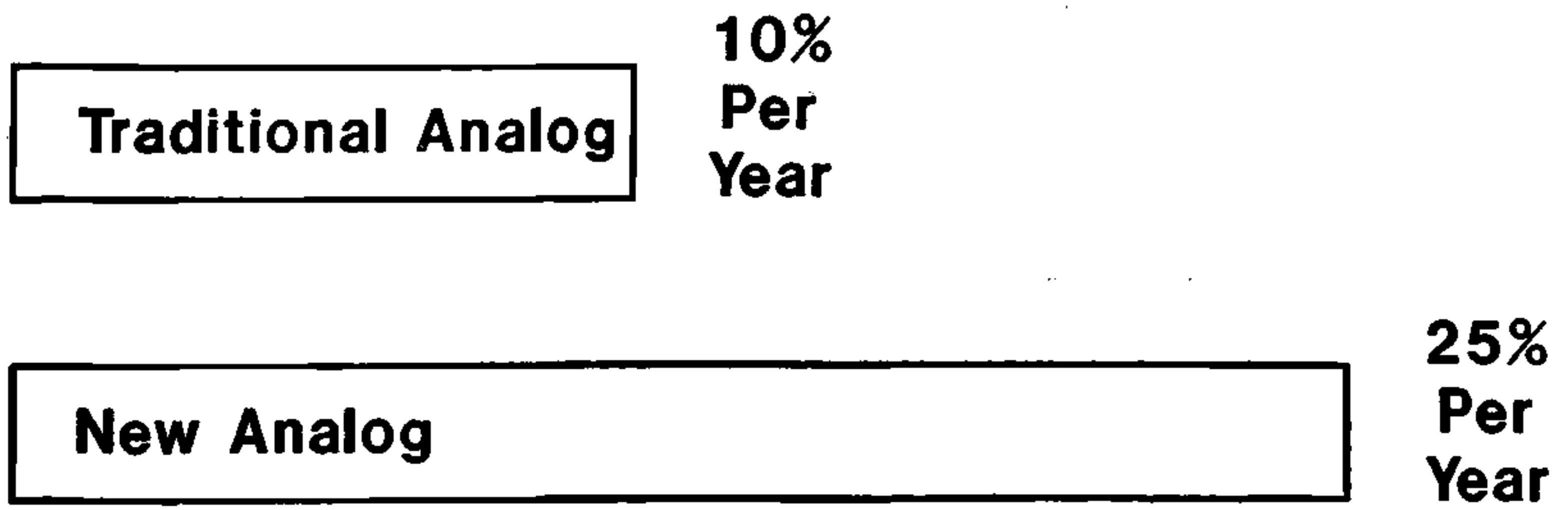

TOTAL IC MARKET
Analog
(%)
30
20
10
0
25.3%
21.2%
1985
1990
National Semiconductor

COMPOUNDED ANNUAL GROWTH RATE

1985 to 1995 (Estimated)



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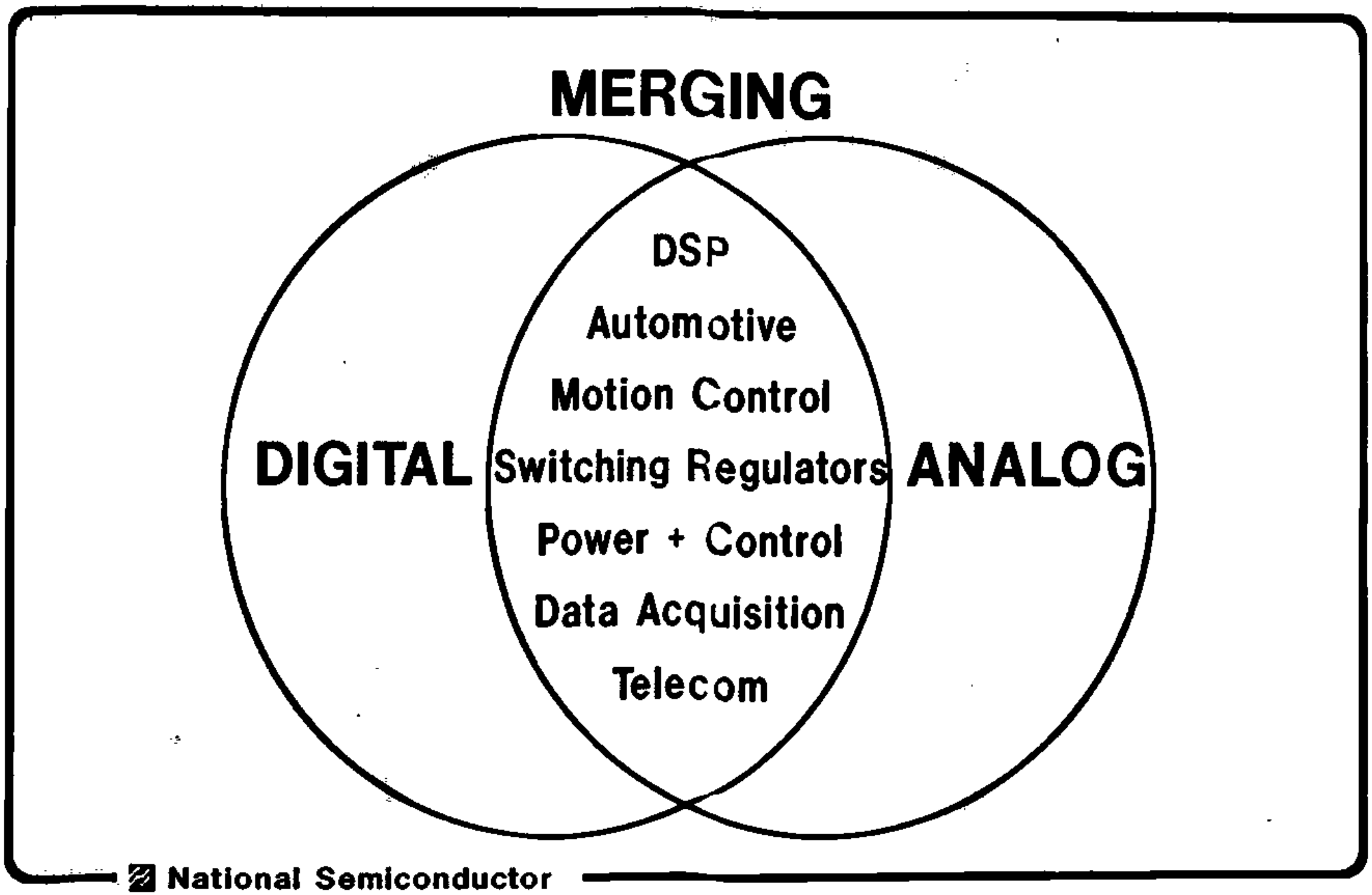
MERGING
DIGITAL
DSP
Automotive
Motion Control
Switching Regulators
Power + Control
Data Acquisition
Telecom
ANALOG
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Challenges for Suppliers

- Development and design
- Process technology
- Test

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1ST

Challenge

Development and Design

- Definition
- Merging technology
- Role and responsibility of designer

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2ND *Challenge*

Process Technology

- **Analog or digital circuit**
- **Bipolar or MOS**

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CMOS

National Semiconductor

M^2CMOS

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MOST BROADLY USED PROCESS

Key point: Within National today, all new, non-memory LSI designs are in M^2CMOS!

- Gate array
- Standard cell
- Telecom (Combo II)
- Advanced interface
- Microprocessor
- Microcontroller
- DSP
- Advanced digital communication

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3RD Challenge

Test

- **Product complexity**
- **Mixed technology**

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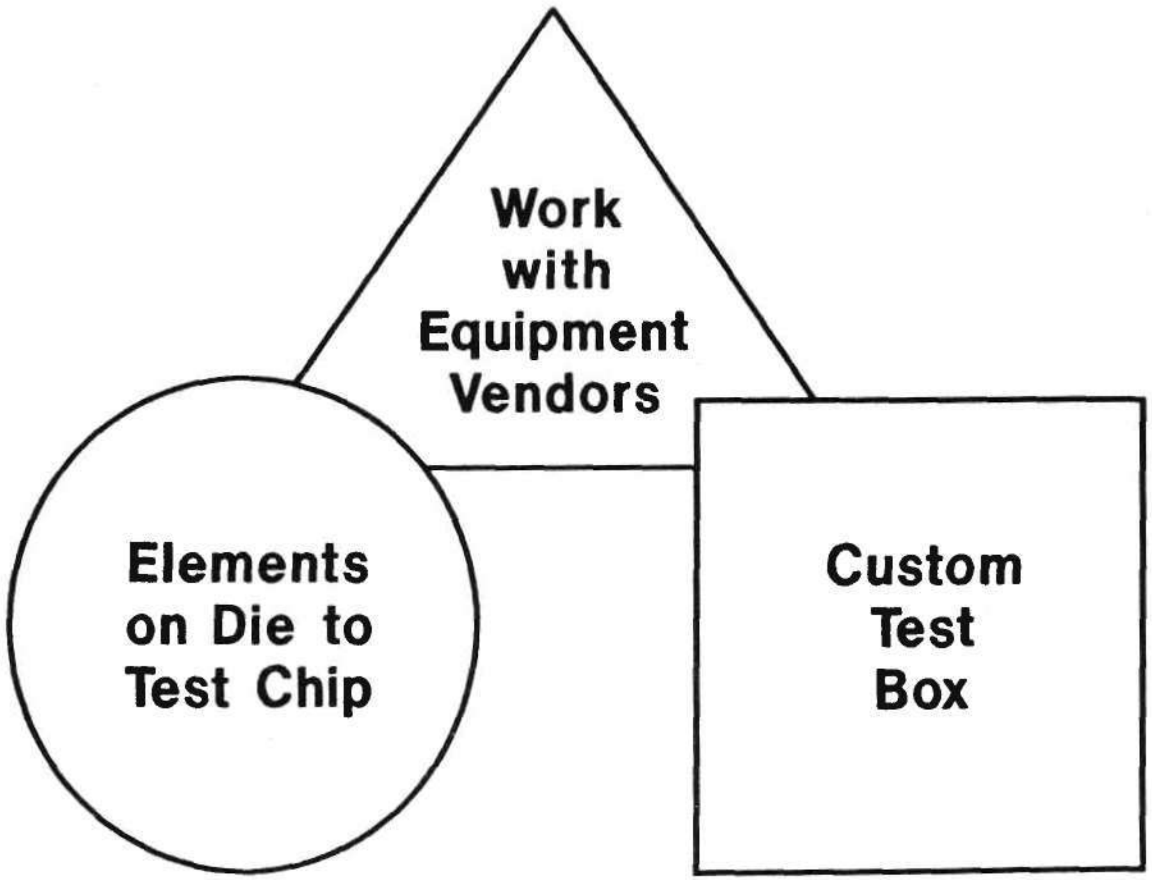
SOLVING THE TEST PROBLEM



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Opportunities for Customers

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Opportunities

- Power, board and cost savings
- Better performance
- Higher quality and reliability

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Advantages for Customers

- Focus on software and applications issues
- Create custom chips/ cell libraries

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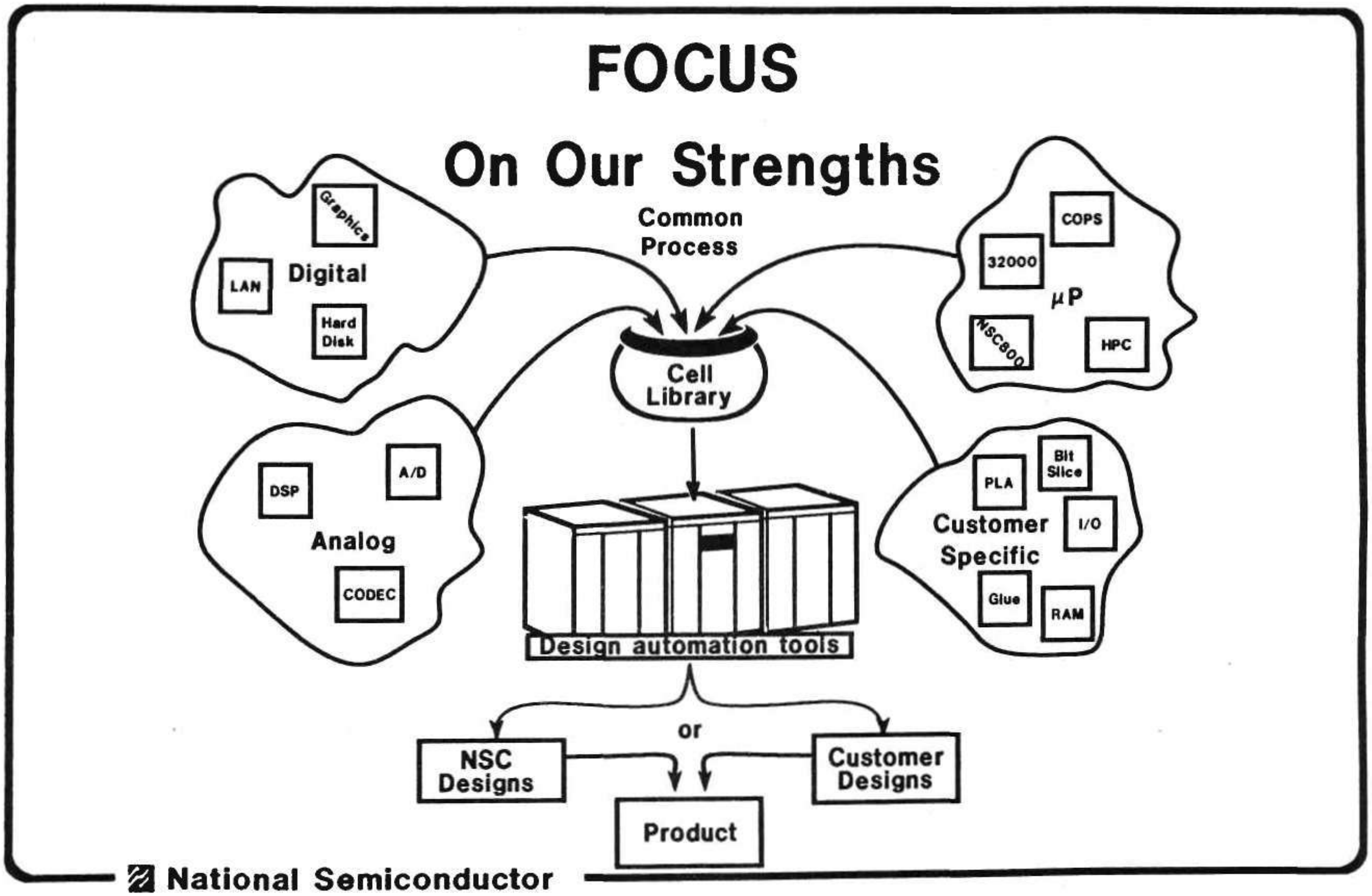
FOCUS
On Our Strengths
Common Process
Digital
Graphics
LAN
Hard Disk
COPS
32000
μP
NSC800
HPC
Cell Library
Analog
DSP
A/D
CODEC
Customer Specific
PLA
Bit Slice
I/O
Glue
RAM
Design automation tools
or
NSC Designs
Customer Designs
Product
National Semiconductor

STANDARD CELL

Phase I: (1985)

- All gate array macros
- Channel router
- G/A S/C migration

Phase II: (Now)

- RAM blocks
- PLA block
- High-current drivers
- Block router
- 16450 UART

STANDARD CELL

Phase III: (2H86)

- 4-bit ALU slice
- Micro-sequencer
- RAM generator
- PLA generator
- Full 7400-series "catalog"
- Core processors
  - COPS II
  - HPC
- First analog functions

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STANDARD CELL

Phase IV: 1987+

- NSC standard LSI circuits
  - e.g., Series 32000
    Ethernet/Cheapernet
    Graphics engine
    DSP
    Disk controller
  - Additional analog functions

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Opportunities for Suppliers

- Leverage designs
- More for R&D dollars
- Advantage to broad-based supplier in customer specific business

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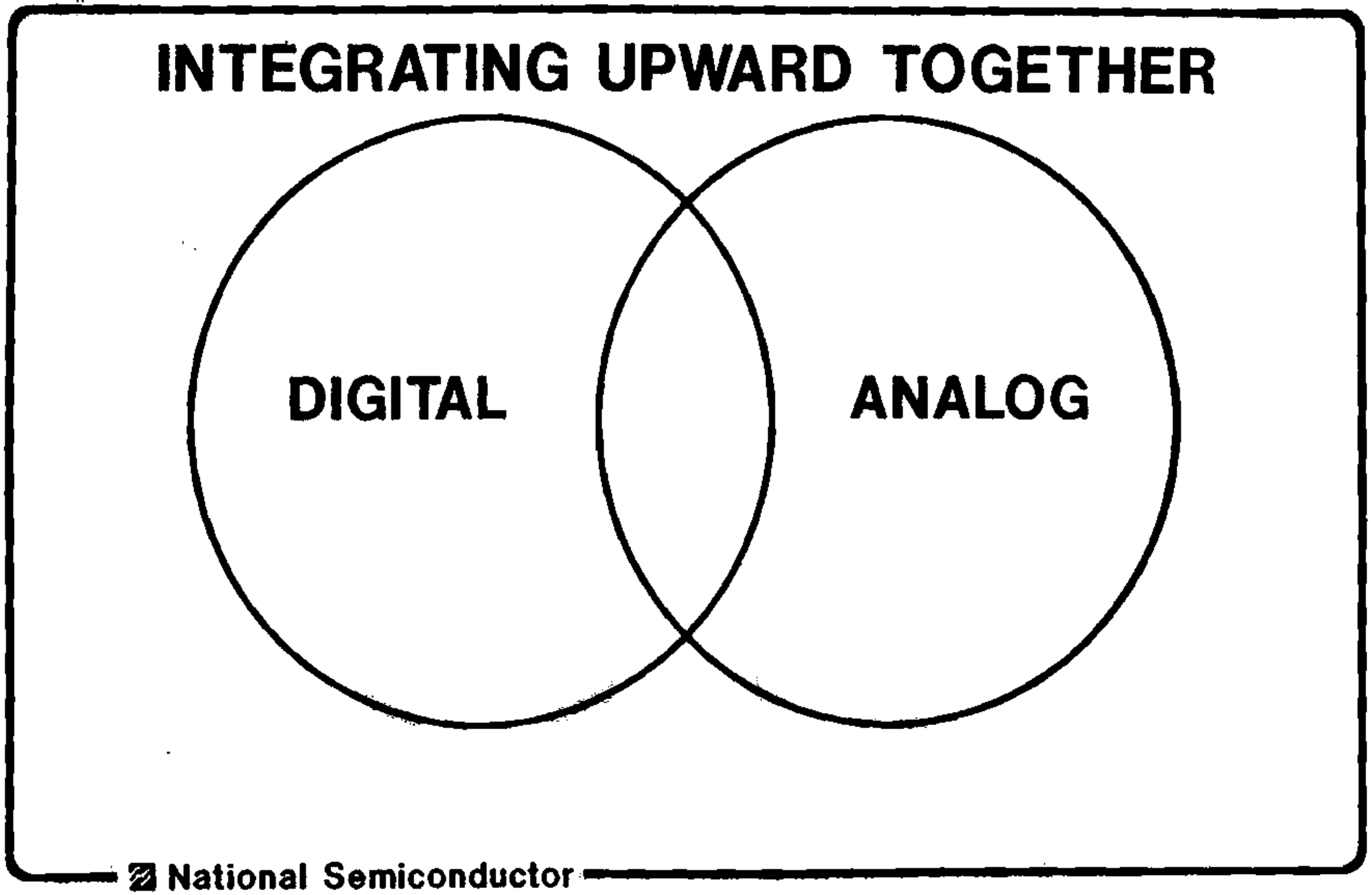
INTEGRATING UPWARD TOGETHER
DIGITAL
ANALOG
National Semiconductor

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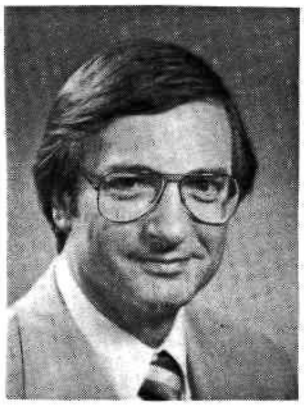
THE EVOLUTION AND FUTURE OF ON-TIME DELIVERY



James A. Norling
Executive Vice President and
General Manager
Semiconductor Products Sector
Motorola, Inc.

Mr. Norling is Executive Vice President and General Manager of the Semiconductor Products Sector of Motorola, Inc. Previously, he was General Manager of Motorola's International Semiconductor Group, and prior to that, he was General Manager of the Power Products Division. In recent years, he has held a variety of other positions at Motorola, including Timepiece Electronics Operations Manager, Bipolar Operations Planning Manager, Power Metal Transistors Operations Manager, and Power Products Director of Operations. Mr. Norling received B.S. and M.S. degrees in Electrical Engineering from the University of Illinois.

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October 20-22, 1986
San Diego, California

Thank you, Stan. When I began preparing my remarks for today it became apparent pretty quickly that limiting this discussion to on-time delivery would be a bit narrow for this subject, and the future of on-time delivery obviously carries with it a fairly substantial change in the future and the way we do business. In fact, there's several of our very important customers in the audience now who have already told me at the coffee break that I deserve whatever I get for raising this subject with them all here! So I'm going to take my chances. It's a topic that gets a lot of discussion and I'd like to give my views. So I've taken the liberty of broadening the scope by changing the title to, "New Realities in Customer Service." And I'd like to offer my views on the rapidly evolving customer service system within which today's stricter on-time delivery requirements are emerging. During the 30 or so years that there's been a commercial semiconductor industry, we've seen customer expectations grow and change. We're now at a point where, in effect, there are three givens to participate in our industry. First, rapidly advancing technology is now required from our industry. Second, continually declining unit costs are expected--or perhaps demanded would be a better term. Third, product quality near or at perfection is expected. These are yesterday's givens. Today a new given is increasingly joining this list: A rapidly changing customer expectation level involving many business elements, generally referred to as service. This term encompasses a broad range of factors, including on-time and just-in-time delivery; guaranteed short lead lines; computer-to-computer communications with customers; and a variety of other service elements related to reducing total costs. What has brought on this change in emphasis on service? Four factors come to mind. First, a maturing of our industry, including the realization that we, as an industry, have not done our homework on service issues in the past. Second, a realization within our industry that service is quickly emerging as the primary competitive differentiator. Third, the increased sensitivity within our customer base to a large group of business issues, which I'll loosely call total cost factors. Fourth, a rapidly developing change in the historical user-supplier relationships which emphasize interdependent working partnerships. Let's review each of these elements, examining where we've been and where we're headed. Just about every marketing textbook ever written has told us that the key elements for success of a business are cost, quality, and service. In the past, we've not really focused on these factors--at least not as much as we should have. For years, we've marketed technology, with geometrically increasing circuit densities providing vastly improved capability. From single discrete transistors twenty-five years, we now approach volume production of 1-Megabit circuits and are designing products with even greater densities. Over time, we've successfully coupled our ever changing technologies with increased manufacturing capability that has allowed continually decreasing unit costs. Much of this cost reduction has come on the shoulders of technology, in the form of more devices per wafer produced. One inch wafers have evolved to 8-inch wafers with a reduction in defect levels giving higher yields and lower costs. While sophisticated automation has allowed additional benefits in quality and cost, we have also aggressively pursued the cost advantages in lower cost countries around the world. A few years ago, some key competitors made our total industry realize, somewhat belatedly, that product quality and reliability were just as important to our success as technology and cost. We're now entering an era of measuring our product quality in parts defective per billion, and we're routinely achieving quality levels that were unheard of only a few short years ago. So to summarize that, we now supply our customers with billions of extremely complex and capable parts with near perfect quality and we charge less and less for them each year. I seriously doubt that any other industry can demonstrate such comparable performance. While we were producing our billions of perfect bits at pennies or less apiece, we lost sight of something. That something was on-time delivery to the customer. Not only did we not deliver when the customer wanted our products, we also did not deliver to our own commitments. I suspect that not too long ago as an industry in total, whether it be early or late, we were shipping less than 50 percent of the time to our own committed dates. This brought upon us some interesting side effects--like excessive inventories held by our customers to buffer our delivery and accuracy, and double ordering by customers to protect their manufacturing rates from our fluctuating performance. Instead of improving our performance, we responded with allocation systems to manage our inflated back log. The reality of this situation is now sinking into both ourselves and our customers. What has happened is rather interesting. Our customers are insisting that we deliver what they order, when we said we would, and sometimes even to their requirements. For awhile we thought that our customers were becoming unreasonable. But soon we realized that they had read their marketing textbooks and they had the right to expect that kind of performance to meet their requirements. We all know the highly competitive nature of our industry, both in terms of the U.S. market place and the world market place. We all strive to introduce the latest technologies, we all continue to seek lower costs, and we've all made advances in product quality. These givens, and now all aspects of service to the customer, are becoming the key competitive differentiators. On time delivery is now achieving given status. By this I mean that each of our firms is now expected by the market place to provide perfect or near perfect delivery to our commitments. And soon we will be expected to perform strictly to our customer's actual short term requirements. Service then is the key competitive issue, but service is far more than just on time delivery. I used the term total cost factors earlier. This needs some definition. Each of us has his own definition of just-in-time. I've chosen to broaden mine to a total cost perspective, including a whole series of issues being raised by our customers--such as: frequent delivery of smaller quantities; certification or ship to stock approaches; guaranteed lead times; very short lead times; consignment of finished goods stocked to the customer's plan; finished goods stock held near the customer's plan; chip inventory dedicated to customers; electronic data interchange; delivery commitments FOB customer's dock; special packaging and labeling requirements such as bar coding. All of these issues are focused on shortening the delivery cycle and reducing our customer's total cost of doing business. Fundamental to all of these issues is the dramatic reduction in what I'll call total cycle time. By this I mean the total time required from the customer's recognition of his need for the item to the incorporation of it into his end product. This definition is intended to cover all of the administrative and manufacturing processes required, as well as all of the intermediate queues. Obviously, this is a very broad area. So focusing on a couple of examples may help to scope the issue. At Motorola, we've concluded that we can take 3 to 5 weeks out of the total cycle time by directly linking our factory information systems to the customer's factory systems. In addition to reducing cycle time, this linkage also can reduce cost and improve overall responsiveness to the customer's needs. A second example is apparent in the area of manufacturing cycle time. By reducing lot sizes and relating those lot sizes to the customer's actual consumption increments, we can plan our production to correspond to the customer's true needs, rather than arbitrary lot sizes established by our manufacturing areas, or arbitrary lot sizes dictated by the customer's ordering practices. These and other new realities force us, as suppliers, to totally rethink the way we do business. For instance, historically we've run our business with large backlogs of actual purchase orders. Today's rapidly changing environment envisions blanket POs with short term releases. We must learn to respond in days or at most, a few weeks. Backlogs, as we've known them, will disappear--to be replaced by forecasts generated both by ourselves and our customers. We now must couple dramatically reduced manufacturing cycle times and the use of forecasts to plan for and respond to customer's short term demands. We must also be flexible enough to handle both unexpected short term orders and to recover on a timely basis if manufacturing problems arise. These, however, are not the only service elements to which we must respond differently. As good as our quality is, we have failures once in awhile. We must learn to give these failures the priority they deserve. Feedback to the customer in weeks is not acceptable. We must respond in hours or several days at the most. If our customers are to have complete confidence in our products, we must stand behind them with near instantaneous capabilities if trouble should occur. Likewise, at the front end of our business relationships, we have design and development cycles that today tend to be ponderously long. As our customer's end product life cycles becomes shorter and shorter, we must respond with substantially reduced design and development cycles. CAD tools are, and will contribute to the needed reductions. But time is not the only issue. We must do it right the first time. Development processes that require multiple passes to work out the bugs will not be competitive. They take valuable time and cost ourselves and our customers dearly. So time is of the essence--whether it be responding to a customer's order, providing him with a new product, or correcting a failure. The capability to quickly make decisions and rapidly fix problems is becoming a way of life.

This brings me to my last point, often spoken about, but I'll take a chance and give my view on it as well. That's the subject of user-supplier relationships. While we add complexity to our products and provide more and faster services, we must be totally attentive to the issue of simplicity. We must do all of these things, and probably more that I haven't mentioned, but me must accomplish these objectives without becoming more difficult to do business with. In fact, we must do the exact opposite and become easier to do business with than we are today. Administrative complexity can't be allowed to get in the way of our objectives. The tendency to impose complex system solutions to our problem must be overridden by finding easier ways to accomplish our and our customer's mutual goals. We then must support these approaches with simplified, highly cost effective systems. I have to point out here that we're dealing with issues that have to be part of a two way street approach. We as suppliers cannot continually give more without getting something in return. These issues should be looked upon as opportunities for both users and suppliers to significantly improve the way we run our businesses. Just in time concepts are based on a lot of common sense, and therefore should improve productivity and reduce cost over time. In fact, implemented properly, JIT will go a long way toward eliminating the demand gyrations in our industry. On the other hand, if JIT is interpreted to be an opportunity to move costs from the user to the supplier, then in the long run, we both fail. Me must find ways to share the problems and share the benefits of these new approaches. A typical example of this scenario is the common attempt by some users to cover up their inability to forecast their business by having their suppliers carry their inventory. Short .term benefits are apparent, but in the longer run, the supplier will pass on the added cost, perhaps becoming less competitive. And the user will delay solving his business problems. In effect, a short term benefit becomes a lose-lose situation. One way to eliminate problems is to forge these often discussed closer partnerships with our customers. Simply stated, suppliers and users must bury their historical adversarial approach to doing business, and in its place develop mutually beneficial long term strategic relationships based on trust, predictability, and commitment. With the goal being competitive advantage in the world market for both of us--the customer and supplier. Why do we need these relationships? I guess I'll cite my own example. I'd suggest that a lot of the craziness in the marketplace during the last three years would have been eased by having more of these trust predictability and commitment relationships. An example of this adversarial relationship in the recent downturn is a few misguided, but highly visible customers who cancelled backlog on vendor A and replaced the demand at the lowest of low prices on vendor B without so much as a conversation. The sad fact is that many semiconductor customers during the 1983-1985 timeframe had little trust in their supplier's ability to meet their needs on schedule, and suppliers had little belief that their customer's demands were real. Motorola, for one, is determined to try to change this pattern by establishing this often discussed closer relationship with customers. These relationships are characterized by constant close interaction in such areas as technology, design and applications support, demand forecasting, electronic ordering and tracking, and continued evolution of just in time delivery, and the elimination of incoming inspection. In short, a total cost perspective. All of this must be supported by active senior management involvement at both parties. The goal of such a relationship, or partnership, is to supply the customer with state-of-the-art product, a stable source of supply, and perfect quality of product and service at a realistic price that reflects total cost and not unit cost. Another reason these types of partnerships are required is the increasing integration of customer systems on silicon. This trend will only accelerate in the future. Geographic proximity, flexibility, and dependability will become increasingly important as customer's reduce their supplier bases and focus their relationships on those vendors who respond to their total needs. The subject of geographic proximity is one that has become increasingly important in recent years with the development of truly global customers having multiple worldwide manufacturing locations. Global sourcing and interrelated multiple country relationships are a fact of life today, and this trend will continue. As suppliers, we must find a way to serve this global customers equally well, regardless of where they're operating their plants. Service imperatives like JIT won't work if we're trying to serve Singapore from San Jose or Phoenix. Strong regional and local capability, with highly coordinated global control, is essential to meet these changing market requirements, and if the product isn't available locally, we must have the means to move it around the planet quickly and at reasonable cost. The trend toward more and more customers limiting the number of suppliers they deal with to a few best in class companies also is very evident. The winners will be those who respond the best from a total cost perspective. Strategic relationships leading to single contracts and a real commitment between user and supplier to work together will assure competitiveness for each in the world market. In these relationships, as I noted earlier, commitment must be a two way street. Design and applications support, predictable delivery, and all the other capabilities a vendor can provide, must be matched by solid commitments for the customer. To be mutually beneficial, the customer's commitment must include the purchase from his supplier partner of higher volume commodity parts as well as the more volatile customer or speciality devices. Just as customers will limit their vendor base, suppliers must carefully choose the customers with whom they can enter into such partnerships. In the long run, we, the suppliers, will only be as successful as our customers and vice versa. Many of our customer's manufacturing operations are undergoing a dramatic change. These customers are developing new innovative and highly beneficial relationships with their suppliers, where the user and supplier are viewed as allies in winning worldwide. The future, then, holds a series of new realities, challenges, and opportunities. Continually increasing product complexity, perfection in quality and reliability, perfection in on time delivery, many more services, and all provided to the customer with declining total cost.

Thank you and may the best team win!

Question: What is the role of electronic distribution in your service system?

Answer: I'll speak for Motorola. Its distributor network continues to have a very major role in its overall route to market. I'm sure it does for most of the suppliers in this room. We've moved to a somewhat similar electronic data interchange procedure with our distributors as well. In fact, it turns out that electronic data interchange that I described that we're now piloting with OEM customers actually got started with our electronic distributors, so we see that ability to exchange order information on a realtime basis as one of the first theories that we've moved into this new type of customer service. So for us it's a very major part of our long term channel to market, and I'd think that was typical, not just for Motorola as well.

Question/Comment: ??? Erickson.....and this is going to be a very unique thing for me. I'll have to thank Jim for having achieved what he is doing now, but you ought to know that it has taken me about ten years--it's taken three generations of general managers of Motorola Semiconductor and at least a dozen defections from Motorola because I've been pestering them all the time. Anyway, you have achieved--topping the list of on time performance--in Europe. The only negative thing of this is, of course, that I'll never be asked to appear in Dataquest anymore because the suppliers have found out what I want. The only thing is, maybe I should have emphasized price instead!

Question: Now that you realize this need for more service, when do you intend to implement this priority, since you are still not giving me what I need currently!

Answer: I'll tell you what. Let me speak first for Motorola, and then I think it wouldn't be that unusual for the industry. I was serious when I said that we've primarily marketed technology and that's been a major, major thrust for us. I guess it wouldn't be fair to say a "new awakening". I think that would be very, very unfair, because many, many suppliers are putting tremendous emphasis on this, but I was serious when I said that as an industry, it was only two years ago when measured--and let me tell you at least what on time means. On time means within a seven day window of when you said it would be there. No partials. Not early. Not late. And I can remember, it wasn't that long ago when I think the industry was probably fifty percent on time by that fairly strict definition. So I guess I feel that we as an industry in total and certainly, at least I'll speak for Motorola, this has been a relatively new set of awakenings for us from an overall priority standpoint and I think I'd have the say honestly that we're just at the beginning on mankind substantial progress on that broad array of service imperatives.

There was a follow up: When you're late in delivering needed product, why do you have a problem in changing the mode of transportation?

I guess I hope we don't, but evidently I must have. Maybe as I'm standing against the wall the person who asked that question could be more direct.

Question: Do your partnership principles apply to your vendors as well as your customers? Please comment.

Answer: The answer is absolutely. I guess maybe it was John Cornell that talked about the fact that the industry overall requires the upstream capability just as much, I guess, as I think I said our success depends on the downstream capability of our customers or their long term success and I would agree with that, and if that's a specific proposal, I guess I'd be happy to entertain it.

Question: How does a blanket order with short term releases work with the continued increase use of ASIC products. We've done this in the ASIC arena, and in fact, have then had call offs on options. As they've come up, or as the need for those options have come up, so we've had somewhat blanket POs with options being call offs between them. Obviously, it requires a little bit different treatment, but I guess philosophically or conceptually, I don't think that it should be a major stumbling block. There are minimum lot sizes which in IC units may be in the thousands and obviously that's not per se been the way I think that we've worked as an ASIC industry overall. I think that there's been a combination of total cost factors to bring those options to the customer. Somebody asked the question of NRE; sometimes it's been NRE, sometimes it's been on a per-unit basis. And sometimes, frankly, it's been on the hopes and dreams of great sounding stories that you guys tell us about how good it's going to be. I know none of my competitors, of course, have done that. What happens to the role of the industrial distributors? I guess same question. I see the distributor world evolving. In fact, distributors moving into the ASIC arena, so I don't think it's a downhill slide based on these service issues.

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THE ROLE OF TECHNOLOGY
IN THE NEW INDUSTRY STRUCTURE

Wilmer R. Bottoms
Senior Vice President
Alan Patricof Associates, Inc.

Dr. Bottoms is Senior Vice President of Alan Patricof Associates, Inc. In addition, he serves on the Boards of Directors of California Devices, Inc., Ion Beam Technologies, Inc., Semiconductor Test Solutions, Inc., and Superwave Technology, Inc. Previously, he was employed by Varian Associates in several managerial positions, most recently as Vice President of Corporate Development. Prior to that, Dr. Bottoms was a Professor of Electrical Engineering at Princeton University. Dr. Bottoms received a B.S. degree in Physics from Huntington College in Montgomery, Alabama, and an M.S. degree in Physics and a Ph.D. in Solid-State Physics from Tulane University.

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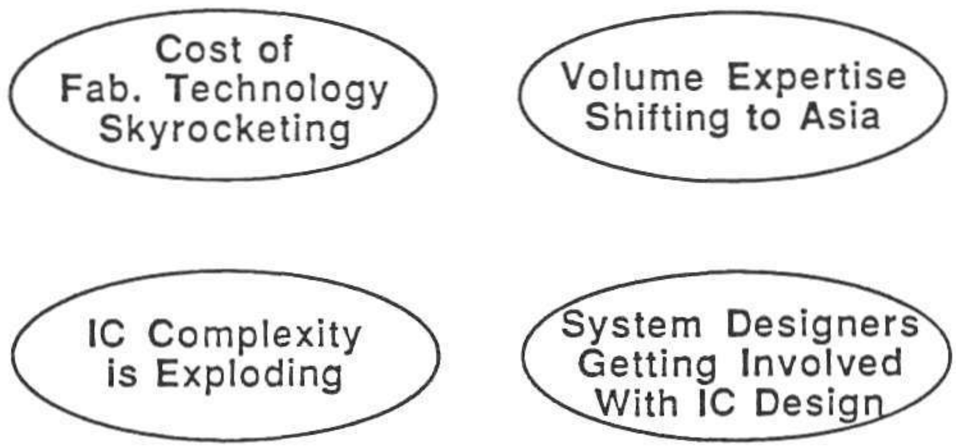
October 20-22, 1986
San Diego, California

GLOBAL FORCES ON THE WORLDWIDE SEMICONDUCTOR INDUSTRY TODAY



WHERE ARE WE TODAY?

- Worldwide over-capacity exists
- Production capacity for volume products has become truly portable
- Japan has a substantial cost of capital advantage
- IC suppliers are selling below cost to maintain marketshare
- Major corporations and countries are subsidizing international competition

THE SEMICONDUCTOR EQUIPMENT INDUSTRY HAS MADE

"STATE-OF-THE-ART" INTEGRATED CIRCUIT MANUFACTURING PORTABLE

International Competitors

Are

Vertically Integrated

	Siemens	Philips	Hitachi	NEC	IBM
Semiconductor materials producer	X	X	X	X	X
Wafer fabrication equipment developer/supplier	X		X	X	X
Significant IC user	X	X	X	X	X

- A recent survey indicated in 1986 23% of Japanese wafer fab equipment will be of U. S. origin

- The same survey projected 0% from the U. S. by 1988

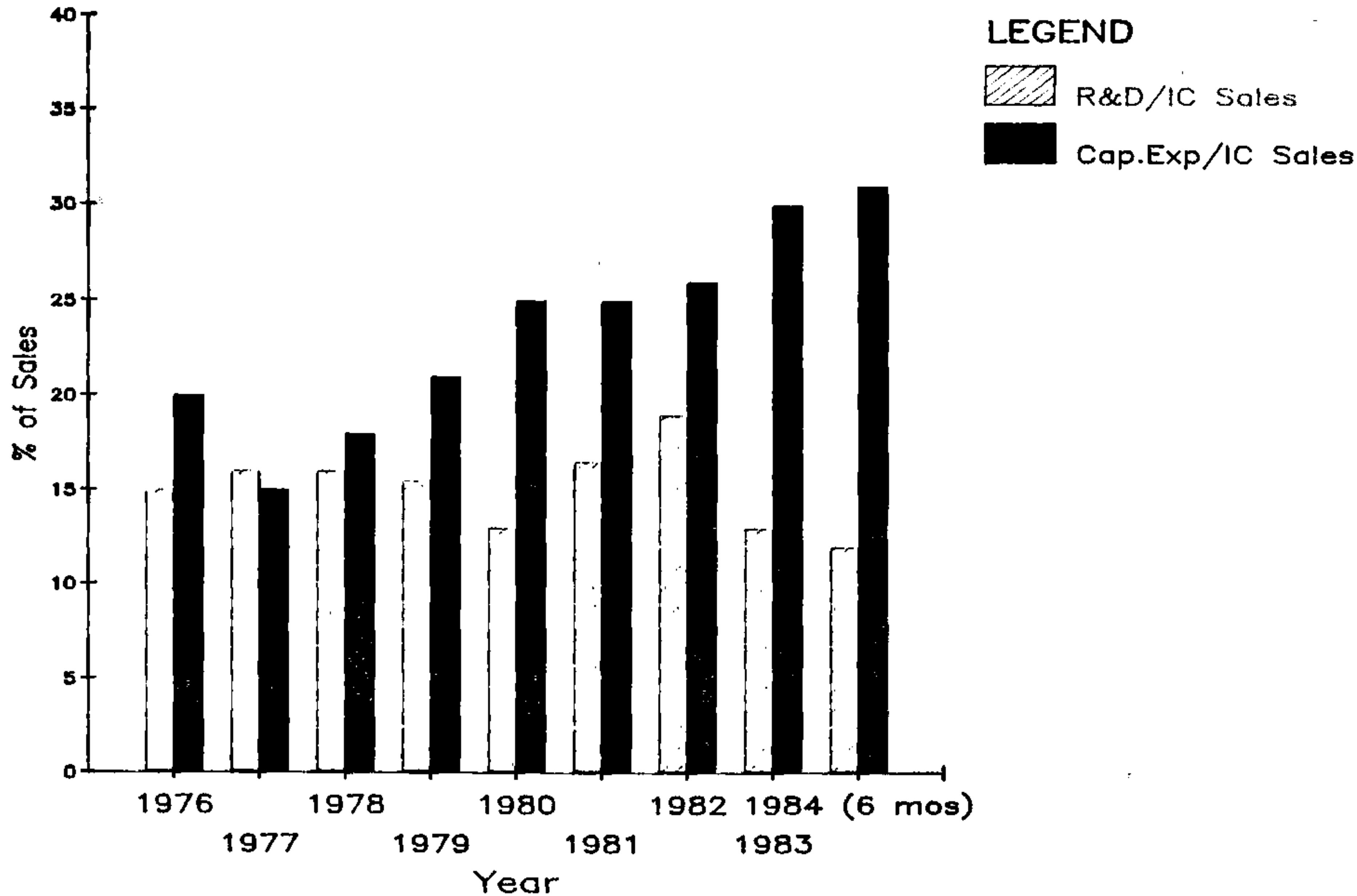
- Hitachi purchased 40% of its semiconductor equipment from internal sources this year

- NEC purchased 60% of its semiconductor equipment from internal sources this year

Overcapacity will continue

Silicon will only be the packaging through which device designers deliver the value added

Japanese Capital & R&D Expenditures as a Percentage of IC Sales



Mitsubishi Saijo Facility

- 200,000 square feet
- More than $300M invested in production equipment
- 650 employees
- Producing 20M drams/month
- Capacity planned to double in 2 increments
  First to be completed in 1987 producing 4MB DRAM

COMMODITY DEVICE SEGMENT

CHARACTERISTICS:

- Products produced in many countries and often subsidized
- Cost per unit is the driving force and are often products sold below real cost
- No sustainable product differentiation is possible
- U. S. will not maintain long term marketshare lead

THERE ARE ONLY TWO ECONOMICALLY VIABLE STRATEGIES FOR SURVIVAL IN INTEGRATED CIRCUIT MANUFACTURING

- Be the lowest cost producer
- Produce lower volume parts where high ASP's are possible

APPLICATIONS SPECIFIC INTEGRATED CIRCUITS SEGMENT

CHARACTERISTICS

- Products produced in close proximity to customers
- Turn around time is the driving force for adequate margins
- Design automation can make ASIC silicon a commodity product
- U. S. will maintain leading marketshare

U. S. BASED PRODUCERS SHOULD CONCENTRATE

ON ASICs WHERE EXCESS PRODUCTION

CAPACITY HAS LESS EFFECT ON ASP'S

This "commodity" characteristic

of high volume devices has caused

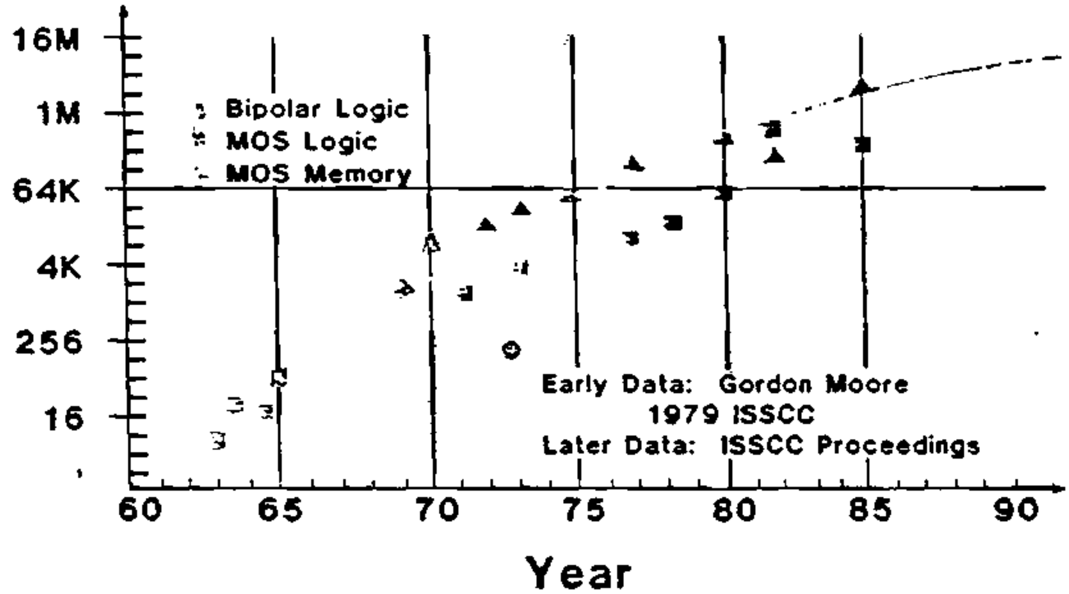
a migration of value added from

device manufacturing to device design

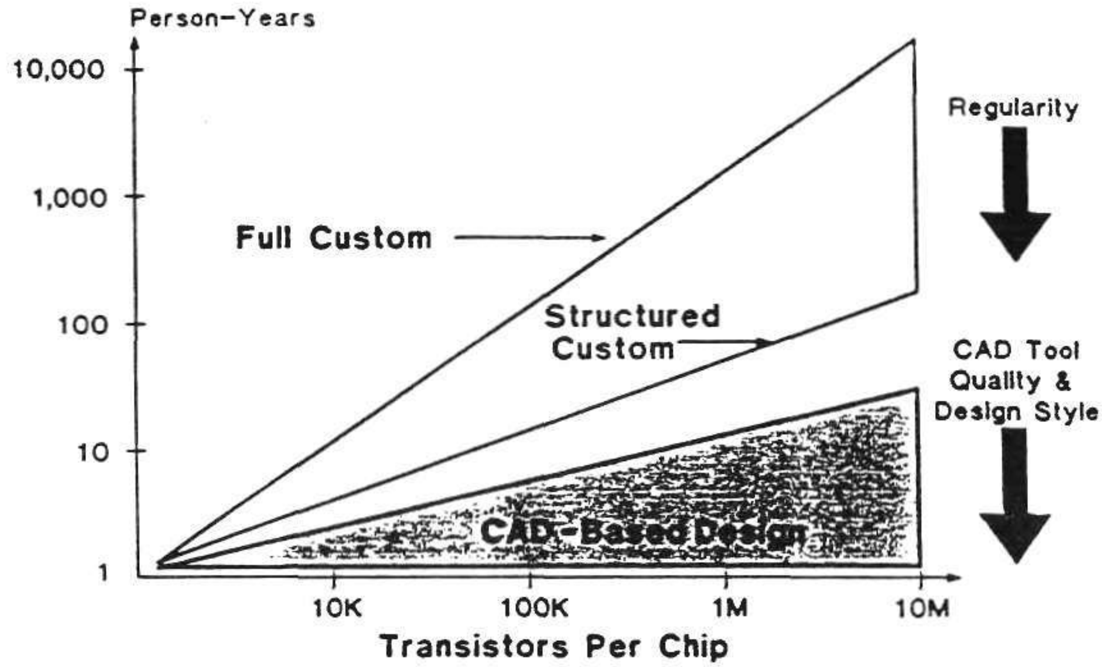
WHERE ARE WE GOING?

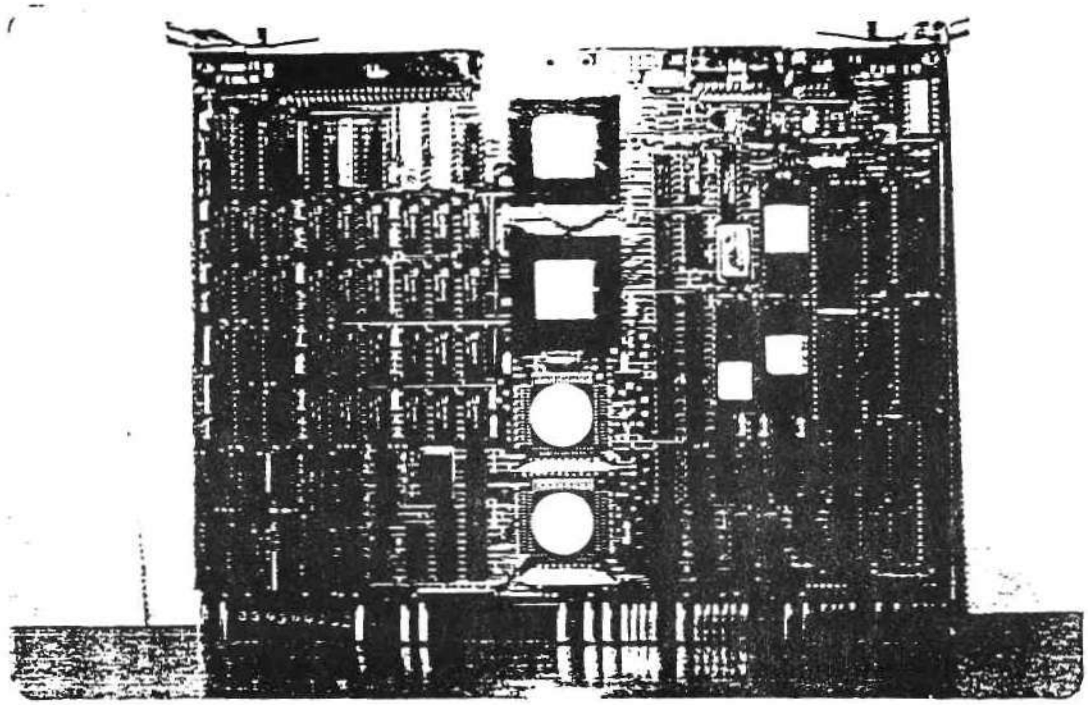
- Designers of High Volume IC's Will Adapt ASIC Design Methods
- Many IC Designers Will Do Design in Software
- Chip Design Will Be At Architectural Level
  - Detail Automated
- System Designers Will Use Complete ASIC Flow Producing Systems on a Chip

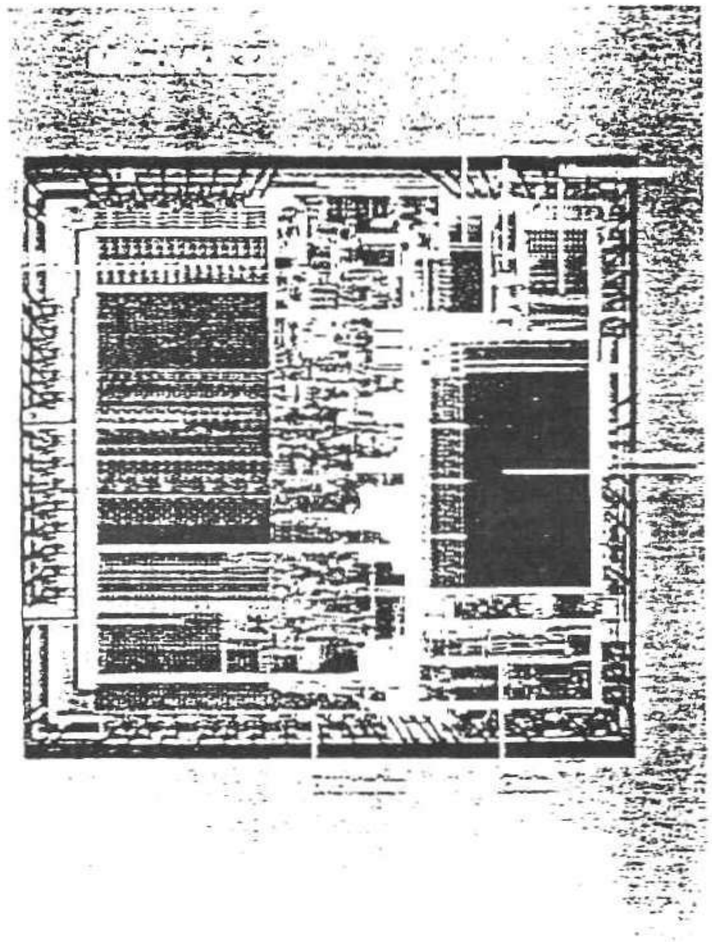
COMPONENTS PER CHIP

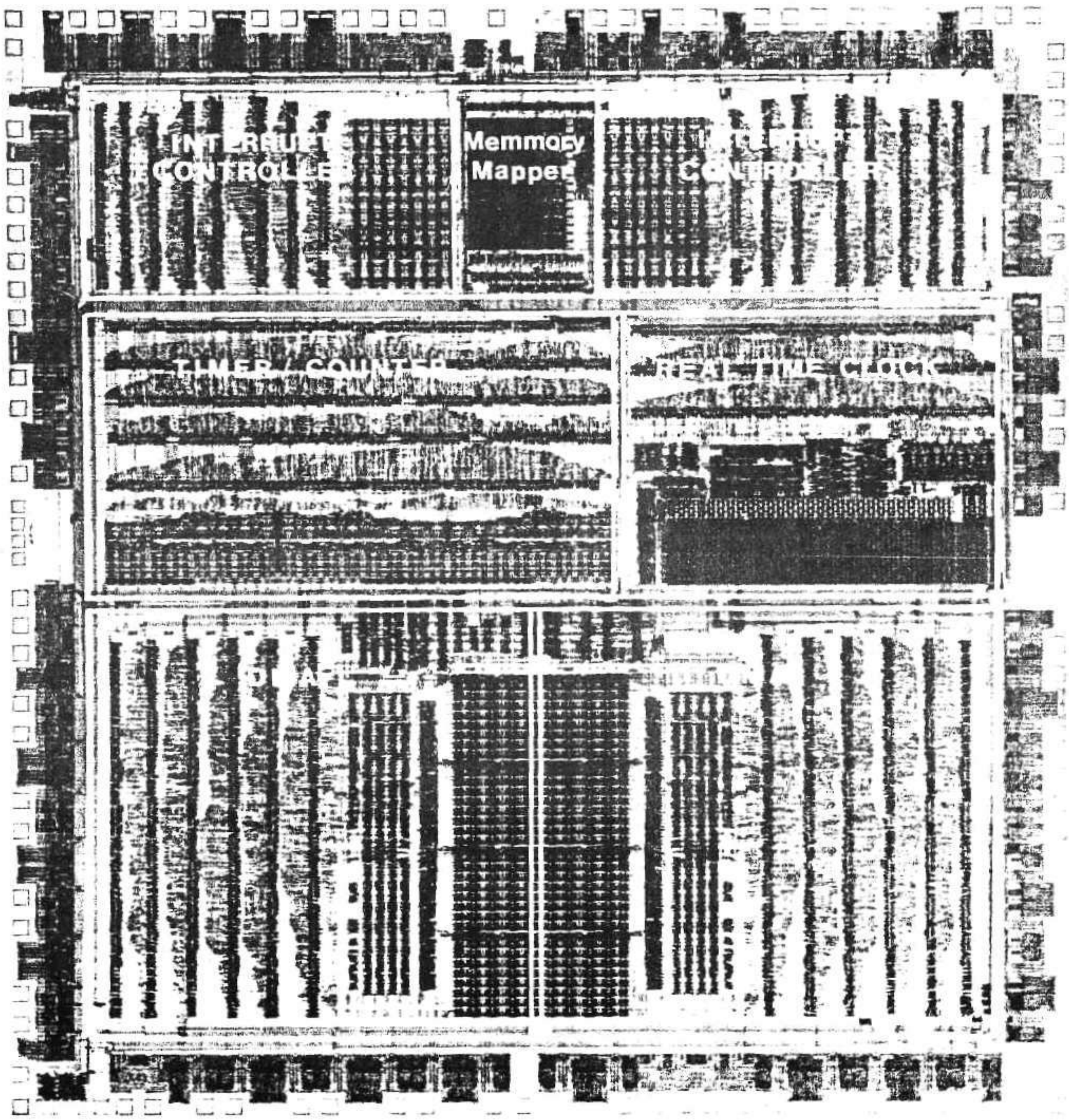


IC DESIGN TIME








Memmory
Mapper

Profit and Growth Opportunities

. High performance devices

. Systems integration

. Quick turn around

High Performance Devices

- Submicron geometrics
- Bipolar—CMOS combinations on Chip
- Digital—Analog combinations on chip

NEW APPROACHES

- Wafer Scale Integration
- 3-D Circuits
- Buried Insulators
- GaAs VLSI
- Optical Interconnection Between Chips
- Optical Interconnection on Chip

Systems Integration

- Systems on a chip
- New packaging technology
- Systems on a board

October 20, 1986

Quick Turn Around

- On chip programmable wiring
- Off chip programmable wiring
- Quick turn ASICs

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SERVICE, THE NEXT HIGH-TECH BATTLEGROUND

William H. Davidow
General Partner
Mohr, Davidow Ventures

Dr. Davidow is general partner of Mohr, Davidow Ventures, a high-technology venture capital firm located in Menlo Park, California. Previously, he was at Intel Corporation, where he ran the firm's microcomputer components and systems business and served as company senior vice president of sales and marketing. Earlier, he worked for General Electric, where he managed an advanced development laboratory, and at Hewlett-Packard, where he led the company's entry into the microcomputer business and where he directed marketing for the Data Products Group. Dr. Davidow graduated Summa Cum Laude from Dartmouth College and received a Ph.D. in Electrical Engineering from Stanford University.

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October 20-22, 1986
San Diego, California

THE COMING SERVICE CRISIS

- 2 -

THREE KEY POINTS

- SERVICE WILL BE NEXT BATTLEGROUND FOR CORPORATE SURVIVAL
- DELIVERING GOOD SERVICE IS A VERY TOUGH JOB
- SERVICE IS PRIMARILY A MARKETING RESPONSIBILITY

THE BROAD VIEW OF SERVICE

FEATURES, ACTS OR INFORMATION WHICH INCREASE THE VALUE OF A PRODUCT

THE INCREASING VALUE OF SERVICE

- KEY TO EFFECTIVE UTILIZATION
- KEY TO PRODUCTIVITY
- TRICKLE DOWN EFFECT
- RISING CUSTOMER EXPECTATION FOR HIGH-TECH PRODUCTS

SIGNIFICANCE OF SERVICE TO HIGH-TECH SUPPLIERS

- KEY TO CUSTOMER SATISFACTION
- INTANGIBLE WAY TO DIFFERENTIATE PRODUCTS
- MAKES HIGH RISK PRODUCTS A SAFE BUY
- ECONOMY OF SCALE SENSITIVE
- DIFFICULT TO DELIVER

SIX BASIC ELEMENTS OF SERVICE

1. SERVICE ORIENTED CULTURE
2. HIGH QUALITY PRODUCT
3. SERVICEABILITY DESIGNED IN
4. SERVICE INFRASTRUCTURE
5. SERVICE ORIENTED STRATEGY
6. MEASUREMENT OF CUSTOMER SATISFACTION

PUTTING GOOD SERVICE IN PLACE IS A VERY TOUGH JOB

- MAY REQUIRE TWO PRODUCT DESIGN CYCLES
- CUSTOMERS ARE STARTING TO APPRECIATE ITS VALUE
- TIME TO START IS NOW

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RESPONDING TO THE COMPETITIVE CHALLENGE

Fred McClintock
Manager, Commodity Management
Reprographic Manufacturing Operations
Xerox Corporation

Mr. McClintock is Manager of Commodity Management in Reprographic Manufacturing Operations (RMO) at Xerox Corporation. He is in charge of worldwide purchasing and materials activities for the Xerox copier and duplicator plants. Previously, as Xerox's Manager of Multinational Procurement, he was in charge of multinational sourcing of all RMO new products and developing RMO procurement strategies. Prior to joining Xerox, Mr. McClintock held purchasing management positions at RCA and Litton. He received a B.S. degree in Mechanical Engineering from the University of Miami.

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XEROX CORPORATION
REPROGRAPHICS
BUSINESS GROUP
MATERIALS MANAGEMENT

"Responding to the Competitive Challenge"

XEROX CORPORATION OVERVIEW :

- 1985 REVENUE $11.8 BILLION
- 102,000 PEOPLE
- WORLD - WIDE OPERATIONS
- BUSINESSES:
  - REPROGRAPHICS (COPIERS & DUPLICATORS)
  - PRINTING SYSTEMS
  - OFFICE AUTOMATION SYSTEMS
  - INSURANCE
  - FINANCIAL SERVICES

REPROGRAPHICS BUSINESS GROUP OVERVIEW:

- REPROGRAPHIC REVENUE OVER 75% OF BUSINESS EQUIPMENT REVENUE
- HEADQUARTERED IN WEBSTER, NEW YORK (NEAR ROCHESTER)
- ELEVEN MANUFACTURING OPERATIONS IN U.S., U.K., HOLLAND, SPAIN, FRANCE, CANADA, MEXICO AND BRAZIL
- AFFILIATE FUJI XEROX OPERATIONS IN JAPAN
- PURCHASING OFFICES IN JAPAN, SINGAPORE, HONG KONG, TAIWAN AND S. KOREA
- STRONG COMPETITION IN MARKET PLACE ACROSS PRODUCT LINES

MISSION:

OUR MISSION IS TO BE THE BEST REPROGRAPHICS SUPPLIER IN THE WORLD, IN TERMS OF:

- CUSTOMER VALUE
  - HIGHEST QUALITY
  - LOWEST COST
- MARKET LEADERSHIP
  - HIGHEST MARKET SHARE
- SHAREHOLDER RETURN
  - PREMIUM RETURN ON ASSETS
- QUALITY OF LIFE FOR OUR EMPLOYEES

REPROGRAPHICS BUSINESS GROUP OVERVIEW:

- REPROGRAPHICS BUSINESS GROUP IS RESPONSIBLE FOR
  - STRATEGY DEVELOPMENT
  - PRODUCT PLANNING
  - TECHNOLOGY DEVELOPMENT
  - PRODUCT DESIGN
  - PRODUCT MANUFACTURING

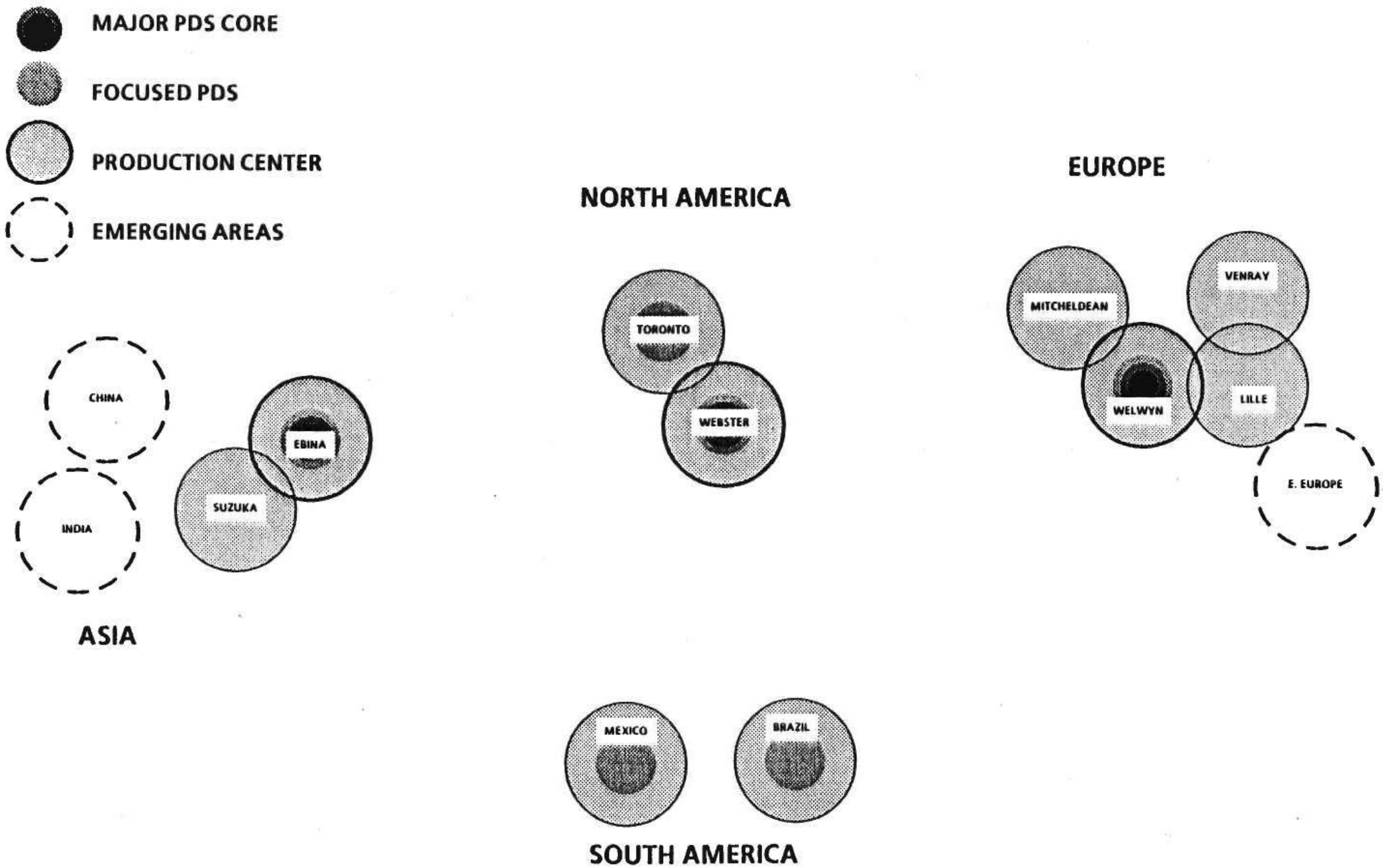
- WE ARE A "PRODUCT DELIVERY" COMPANY

COMPETITIVE POSITION:

"COMPETITIVE BENCHMARKING" STUDIES OF 1980 REVEALED PERFORMANCE GAPS IN THE FOLLOWING:

- PRODUCT QUALITY
- PRODUCT COSTS
- PRODUCT LEAD TIMES
  - NEW PRODUCT INTRODUCTIONS
  - FLEXIBILITY TO MARKET PLACE

REPROGRAPHIC PRODUCT DELIVERY CENTERS:



GEOGRAPHIC VISION:

- MAJOR PRODUCT DELIVERY CENTERS LOCATED IN MAJOR MARKET AREAS
  - FULL RANGE DESIGN AND MANUFACTURING
  - SUPPORTED BY A TIGHTLY INTEGRATED SET OF PRODUCTION CENTERS
  - LOCAL MODEL SUPPLIER NETWORK
- FOCUSED PDS CENTERS IN OTHER DEVELOPED MARKET AREAS
  - A LIMITED SET OF FUNCTIONAL AND PROCESS TECHNOLOGIES
  - ALSO SUPPORTED BY A LOCAL VENDOR BASE
- LOCAL PRODUCTION CENTERS IN EMERGING MARKETS
  - FOCUSED ON NATIONAL INTEGRATION OF PRODUCTS
  - CAPABILITY TO EMERGE AS FOCUSED PRODUCT DELIVERY CENTERS
- WORLD CLASS SUPPLIER BASE AVAILABLE FOR UNIQUE CAPABILITIES
- AN EFFICIENT LOGISTICS SYSTEM WITHIN THE NETWORK
- AN EFFICIENT COMMUNICATIONS NETWORK

ADVANTAGES:

- LOWEST, LANDED TOTAL ACQUISITION COST IN MAJOR MARKETS

- MINIMIZED INVENTORY AND PIPELINES WITH JUST-IN-TIME PRINCIPLES

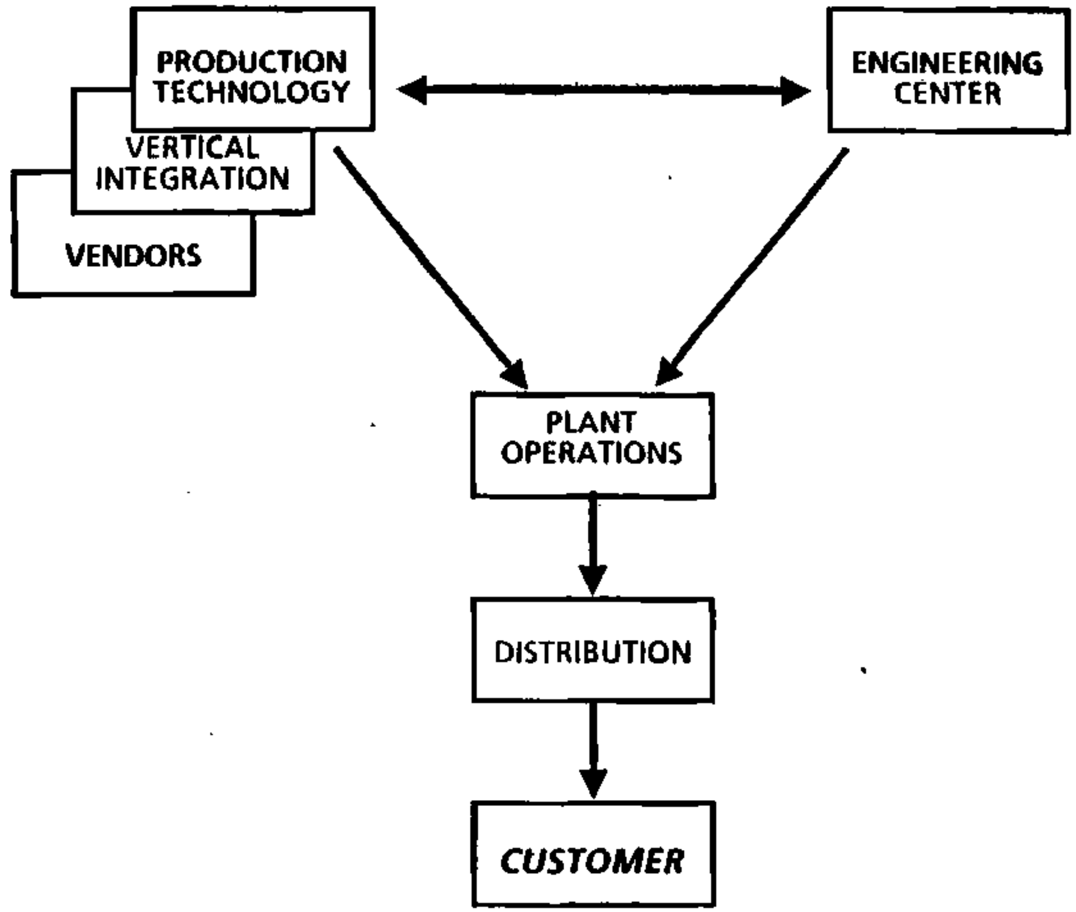
- COMPRESSION OF DESIGN AND PRODUCTION LEADTIMES THROUGH LOCAL NETWORKS AND FLEXIBLE PRODUCTION CENTERS

- BALANCED CAPACITY RISKS THROUGH VENDOR / VERTICAL INTEGRATION STRATEGIES

- "PORTFOLIO" OF PRODUCTION CAPABILITIES TO SUPPORT THE SUPPLY SIDE OPPORTUNITIES FOR CURRENCY FLUCTUATION AND SUPPORT OF MARKET ACCESS REQUIREMENTS

- INTEGRATION OF EMERGING MARKETS INTO A PLANNED EXPORT GROWTH PATTERN

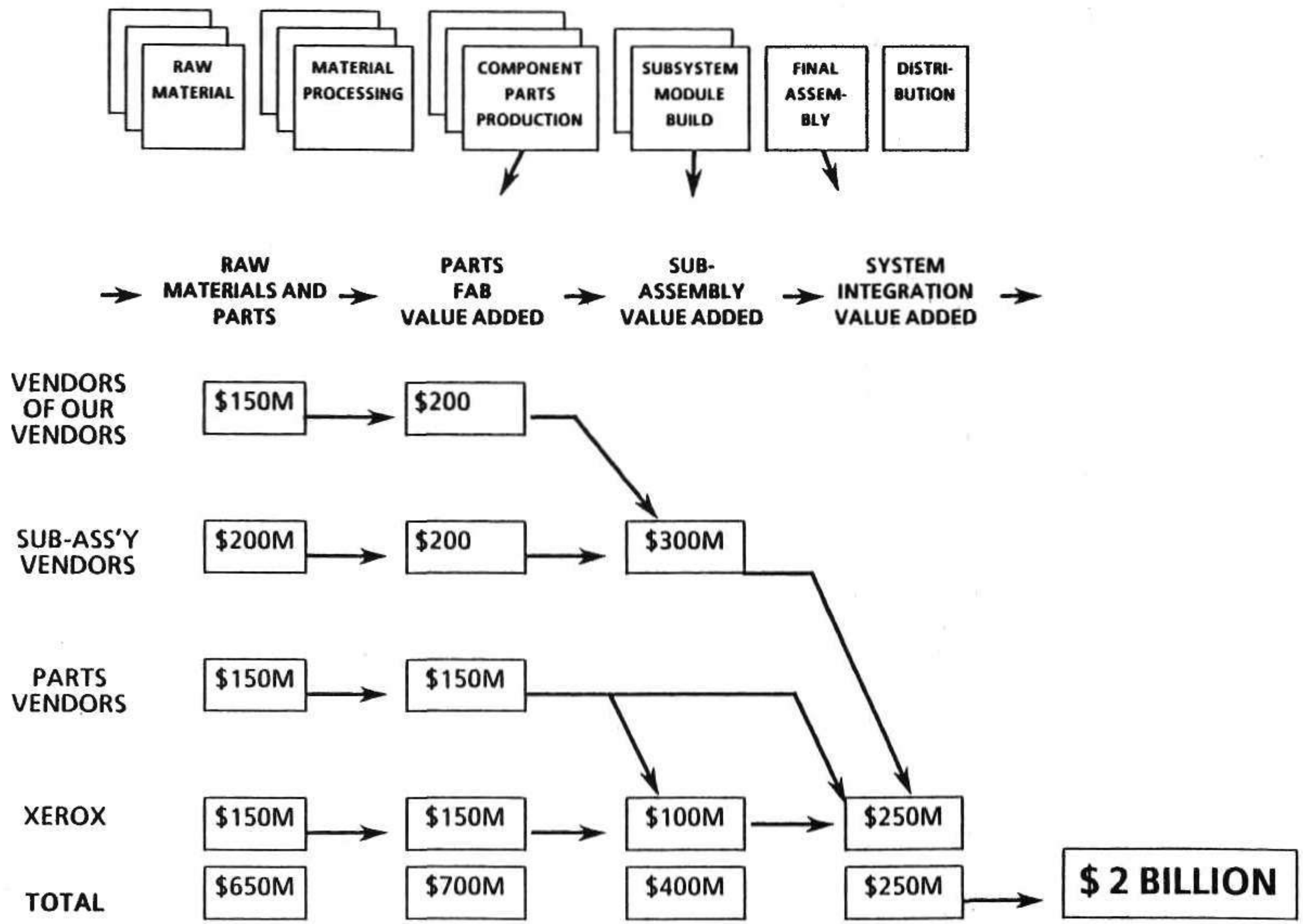
THE PRODUCT DELIVERY SYSTEM:



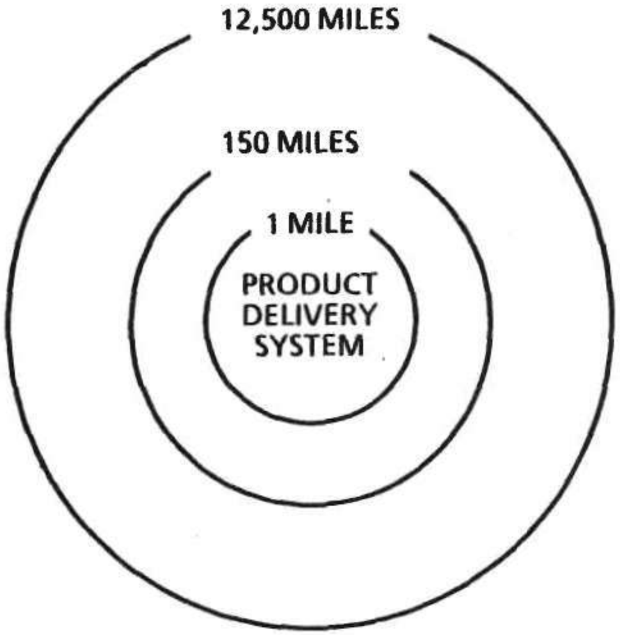
MUST BE OPTIMIZED AS A SYSTEM........

........NOT AS INDEPENDENT FUNCTIONS

XEROX PRODUCTION STAGES:



GEOGRAPHIC VIEW OF THE SYSTEM:



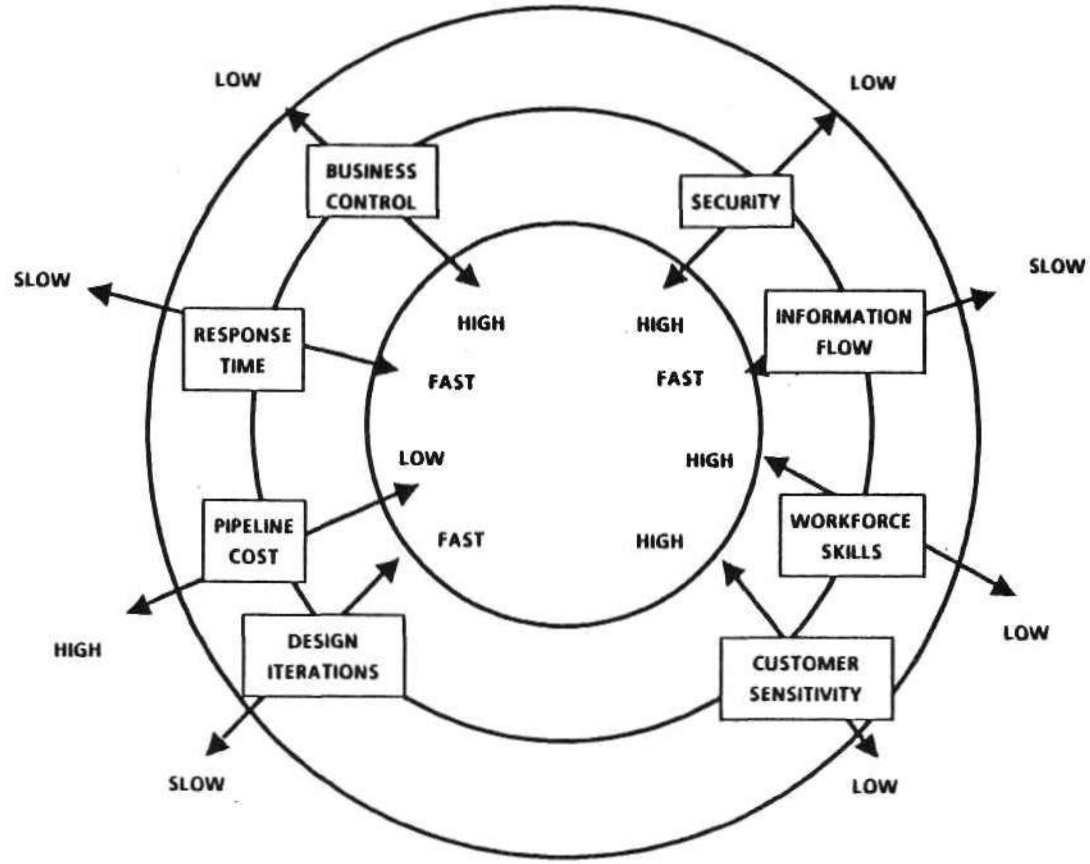
CORE ACTIVITIES	OUTSIDE ACTIVITIES
PROPRIETARY DESIGNS	RAW MATERIALS
PROPRIETARY PROCESSES	CATALOG ITEMS
ENABLING TECHNOLOGIES	WORLD COMMODITIES
MODELS & PROTOTYPES	SIMPLE SUBSYSTEMS
SYSTEM INTEGRATION	
FABRICATION OF BULKY PARTS	

..... GEOGRAPHIC PROXIMITY IS DESIRED STATE

OBJECTIVE IS TO:

- LOCATE THE CORE NEAR THE CUSTOMER FOR RESPONSIVENESS
- SPEED UP INFORMATION TRANSFER AND THE PHYSICAL FLOW OF MATERIAL
- DRAMATICALLY REDUCE LEAD TIMES AND ASSET LEVELS

GEOGRAPHIC DEPENDENCIES:



MOST CRITICAL SUCCESS FACTORS HAVE A DEPENDENCY ON GEOGRAPHIC DISTANCE

A BASIC ENABLER TO OPTIMIZE THE PRODUCT DELIVERY SYSTEM IS THE SELECTION OF THE PATH OF ACQUISITION THROUGH THE SYSTEM

.......THE SOURCING PROCESS

- 13 -

STEPS IN THE SOURCING PROCESS:
- **IDENTIFY CRITICAL SUCCESS FACTORS FOR THE DECISION**
  - **PRIORITIZE THE FACTORS**
    - **SELECT THE SOURCE WITH THE BEST "NATURAL" CHARACTERISTICS**
      - **INVEST TO ALTER UNACCEPTABLE CHARACTERISTICS**

RESPONDING TO THE CHALLENGE:

- JUST IN TIME OFFERS SIGNIFICANT PRODUCTIVITY OPPORTUNITIES
- INTERNAL IMPLEMENTATION OF J.I.T. COMMITTED AND ON GOING
- PURCHASED MATERIAL REPRESENTS 80% OF PRODUCT COST
- SUPPLIERS ARE KEY TO ACHIEVING OUR GOALS
- MATERIALS MANAGEMENT FOCUS ON "PRODUCT DELIVERY" AND INTEGRATES:
    - PRODUCT DESIGN
    - MANUFACTURING
    - SUPPLIERS

IMPLEMENTING JIT - GETTING STARTED:

- SOURCING / SUPPLIER MANAGEMENT - "FEWER BUT BETTER"
- SUPPLIER DEVELOPMENT - "COMMODITY TEAMS"
- QUALITY - "#1 PRIORITY"
- COMPETITIVE BENCHMARKING - "EXPECTATION LEVEL"
- MATERIALS LOGISTICS - "START ELIMINATING WASTE"

SOURCING / SUPPLIER MANAGEMENT:

- SUPPLIER BASE CONSOLIDATION FROM 5,000 TO 300 WORLDWIDE SUPPLIERS
  - CONCENTRATION OF ECONOMIC LEVERAGE
  - MORE STABLE DEMANDS ON SUPPLIERS
  - ABILITY TO FOCUS ON A FEW HIGH POTENTIAL SUPPLIERS
  - SIGNIFICANT REDUCTION IN MATERIAL ACQUISITION COSTS

- EARLY SUPPLIER INVOLVEMENT (ESI)
  - PRODUCT DESIGN PARTICIPATION
  - OPEN SHARING OF BUSINESS AND TECHNICAL INFORMATION

- LONG TERM CONTRACTS
  - TWO TO FIVE YEARS
  - ESI SUPPLIERS - CONTRACT FOR THE LIFE OF THE PART

SUPPLIER DEVELOPMENT:

- "MODEL SUPPLIER" PROGRAM
  - COMMODITY COMPETITIVE BENCHMARKING
  - TRIPS TO JAPAN FOR FIRST HAND OBSERVATION
  - TECHNOLOGY SYMPOSIUM

- SUPPLIER JUST IN TIME (JIT) 1985-86
  - ONE DAY SENIOR MANAGEMENT OVERVIEW
  - THREE DAY SEMINAR
  - IMPLEMENTATION SUPPORT

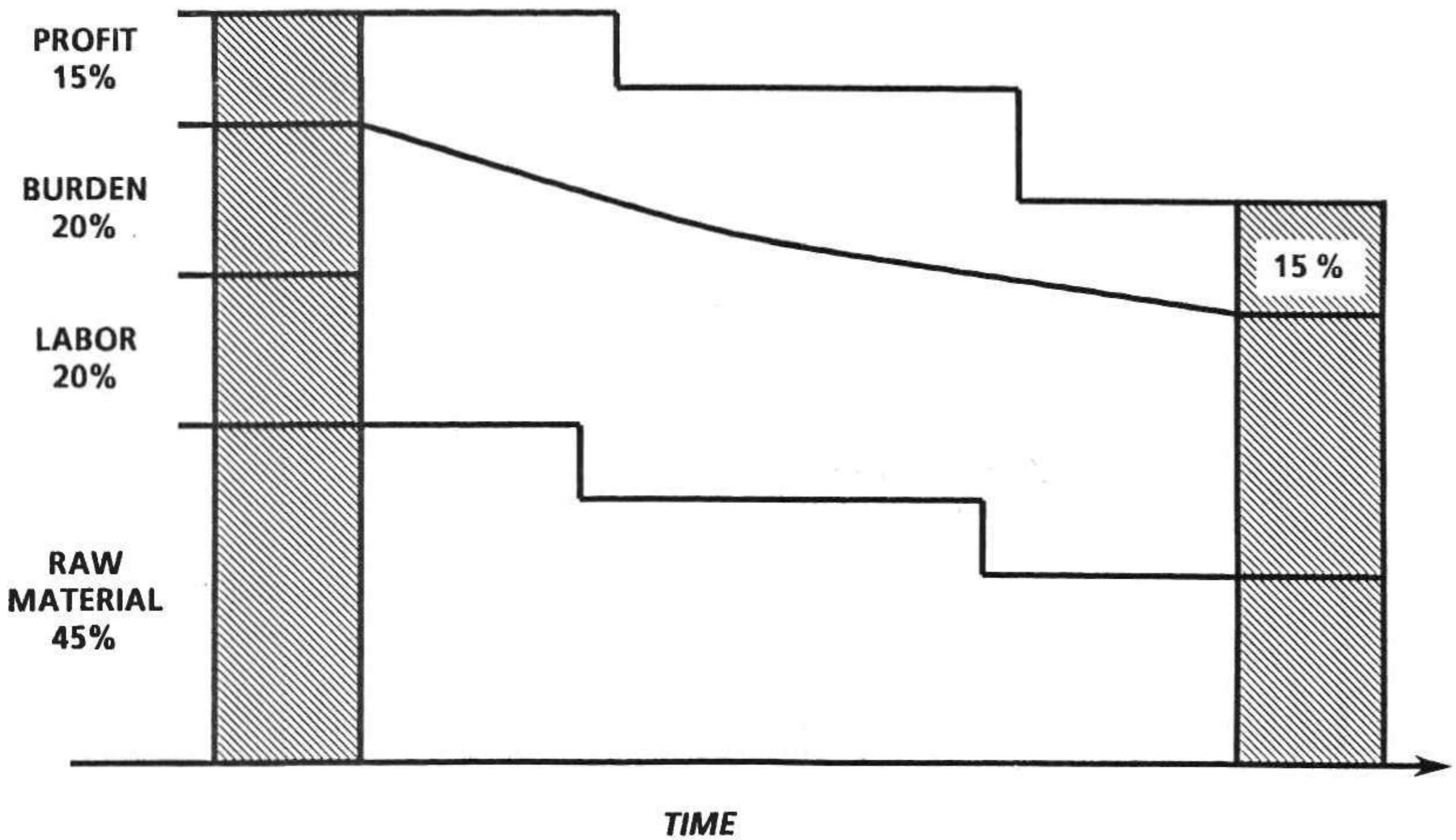
- SUPPLIER TOTAL QUALITY (TQC) 1987-88
  - CONCEPT OF QUALITY
  - DEVELOPING QUALITY POLICY / PRACTICES
  - PROBLEM SOLVING TECHNIQUES
  - QUALITY TOOLS

- COOPERATIVE COSTING - WORK WITH SUPPLIERS TO
  - ESTABLISH AND UNDERSTAND WORLDWIDE PRODUCT AND COMMODITY BENCHMARKS
  - ESTABLISH GOALS AND TARGETS
  - DEVELOP AGGRESSIVE ACTION PLANS TO ACHIEVE TARGETS

JUST-IN-TIME PURCHASING:

COST REDUCTION THROUGH OPERATIONS IMPROVEMENTS...

.....NOT PROFIT ELIMINATION



QUALITY:

- QUALITY MUST BE NUMBER ONE PRIORITY

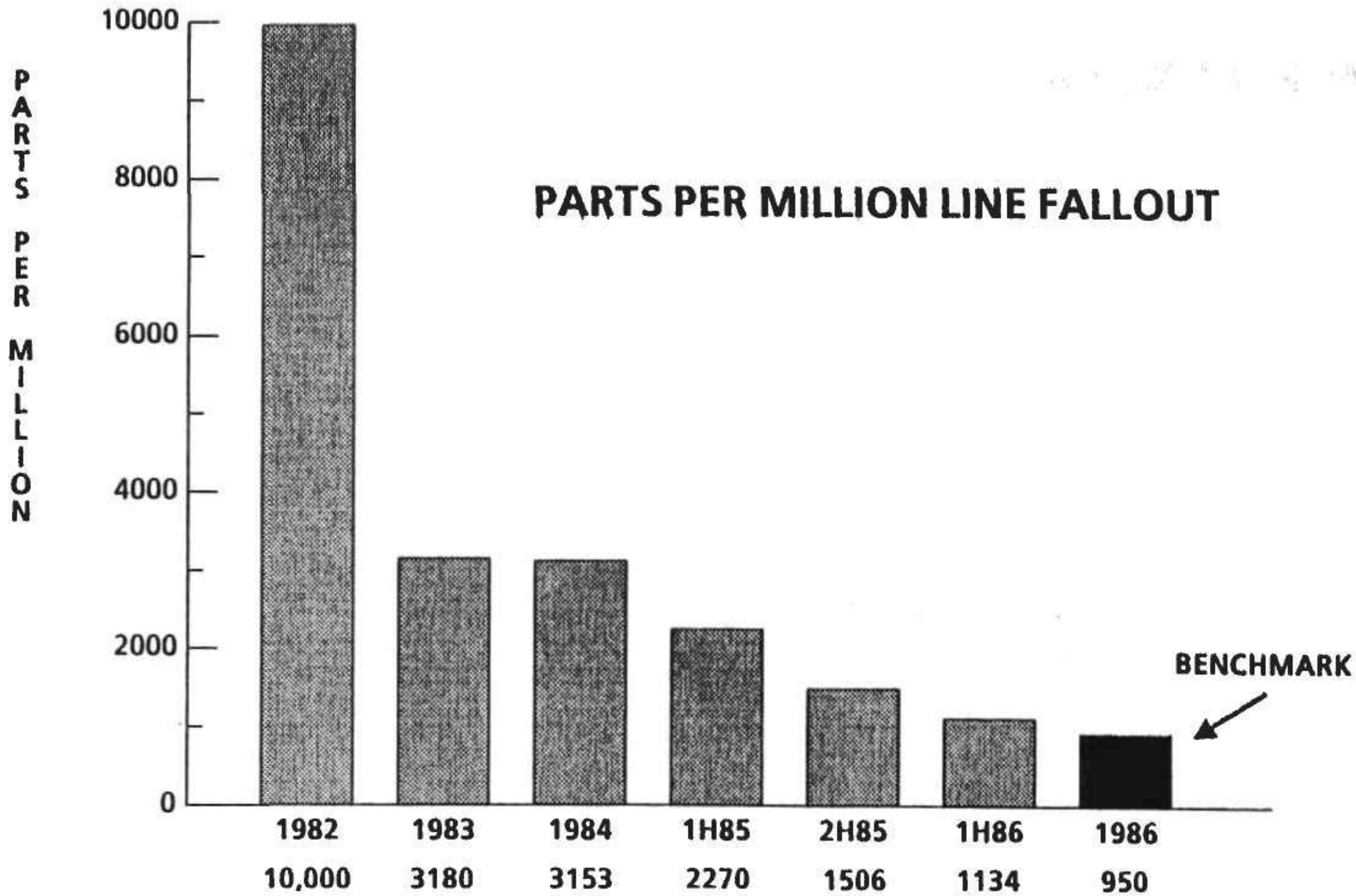
- INSPECTION MUST GIVE WAY TO PREVENTION
  - DEFINE REQUIREMENTS
  - GET THE PROCESS UNDER CONTROL
  - KEEP THE PROCESS UNDER CONTROL

- XEROX CERTIFICATION PROGRAM
  - SUPPLIER EDUCATION 1981-83
  - ON GOING IMPLEMENTATION SUPPORT
  - 95% OF ALL PRODUCTION PARTS ARE CERTIFIED

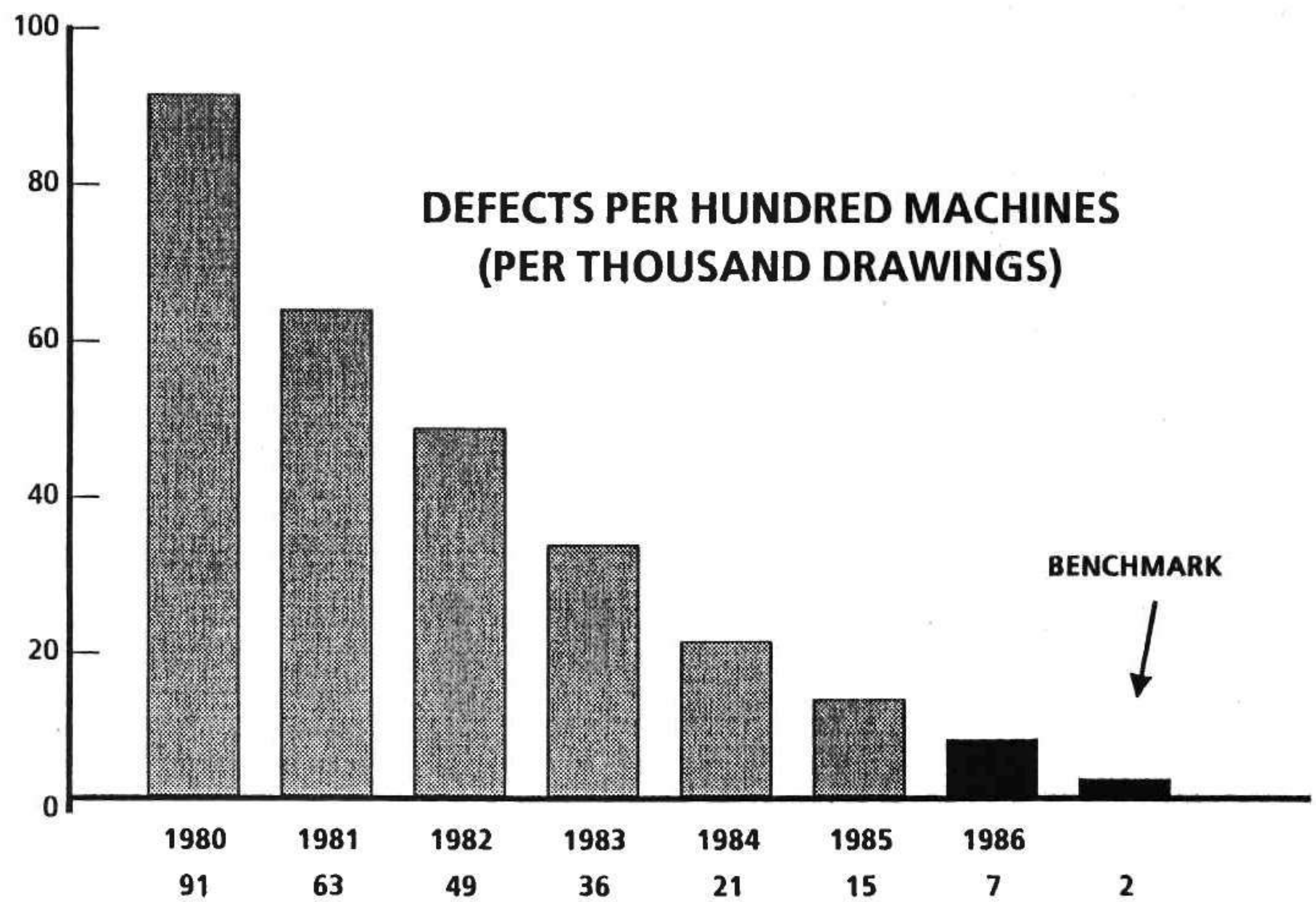
- STATISTICAL PROCESS CONTROL (SPC) RESULTED IN 85% IMPROVEMENT IN SUPPLIER QUALITY -- BUT NOT GOOD ENOUGH

- TOTAL QUALITY CONTROL (T.Q.C.)
  - REQUIRED TO ATTAIN BENCHMARK PERFORMANCE
  - CERTIFICATION OF PARTS MUST GIVE WAY TO CERTIFICATION OF SUPPLIERS

PURCHASED PARTS QUALITY:

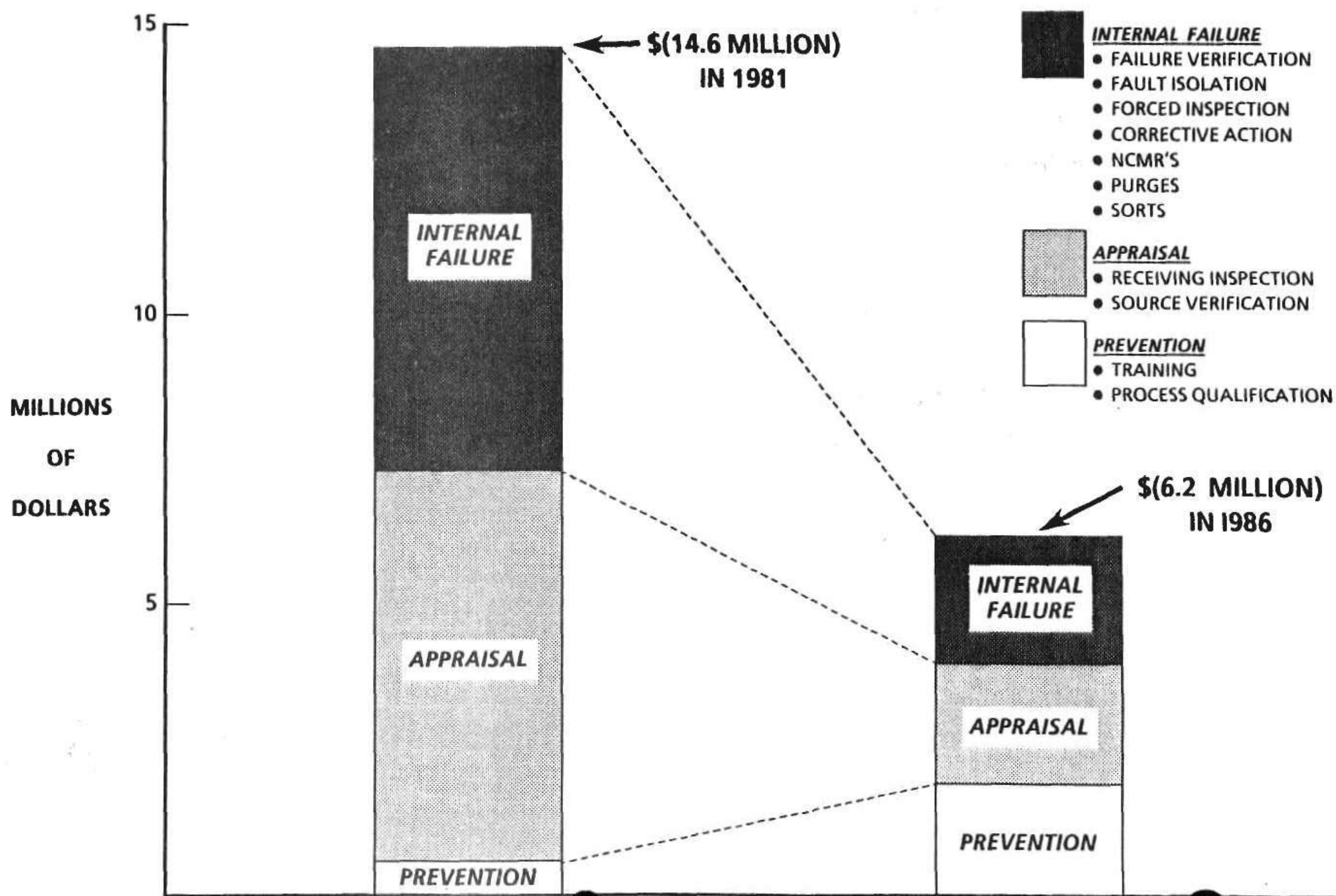


ASSEMBLY QUALITY:



- 21 -

COST OF QUALITY:



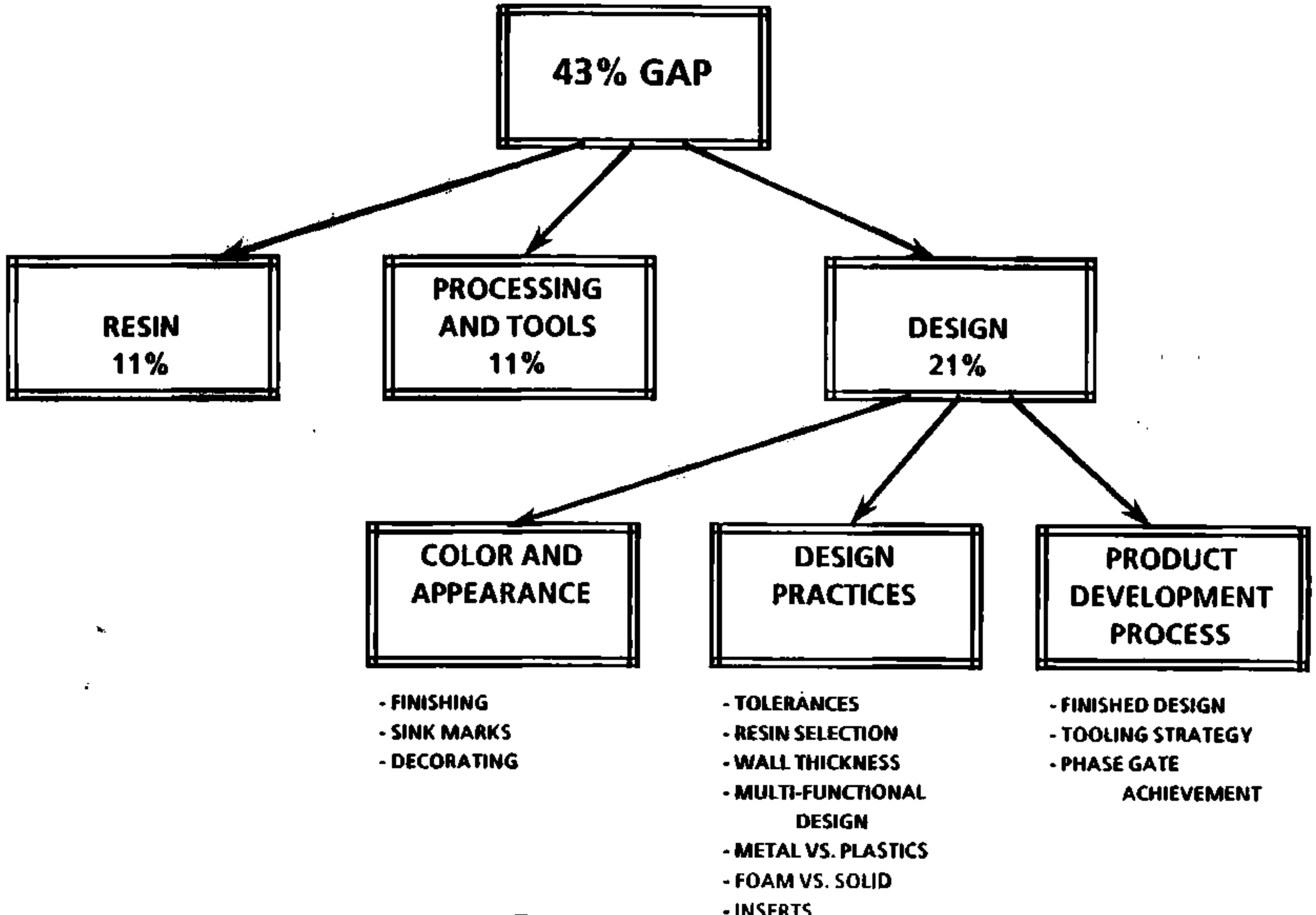
COMPETITIVE BENCHMARKING:

- CONTINUOUS PROCESS OF MEASURING OUR PROCESS, SERVICES & PRACTICES AGAINST THE TOUGHEST COMPETITION AND BEST FUNCTIONAL LEADERS IN THE WORLD

- XEROX COMPETITIVE BENCHMARKING PROCESS PROVIDES FOR:
  - ACCURATE COST ASSESSMENTS BASED UPON TEARDOWNS OF COMPETITIVE PRODUCTS
  - ANNUAL RECALIBRATION & VALIDATION OF BENCHMARK ELEMENTS
  - BENCHMARK ALL MAJOR COSTS OF THE BUSINESS
    - ENGINEERING COST
    - PRODUCT DEVELOPMENT TIME
    - TOOLING COST & LEAD TIME
    - COMMODITIES COSTS (MATERIAL, LABOR)
    - OVERHEAD RATES
    - LEAD TIMES
    - INVENTORY TURNS

- FUJI XEROX PROVIDES AN EXCELLENT WINDOW INTO JAPANESE MANUFACTURING

COMPETITIVE GAP - PLASTICS COMMODITY:



MATERIAL LOGISTICS:

- INVENTORY REDUCTION
  - LEAD TIME REDUCTION
  - MATERIAL RELEASES AT USER LEVEL
  - LOCAL "BUS ROUTE"
  - DEMAND PULL SYSTEMS

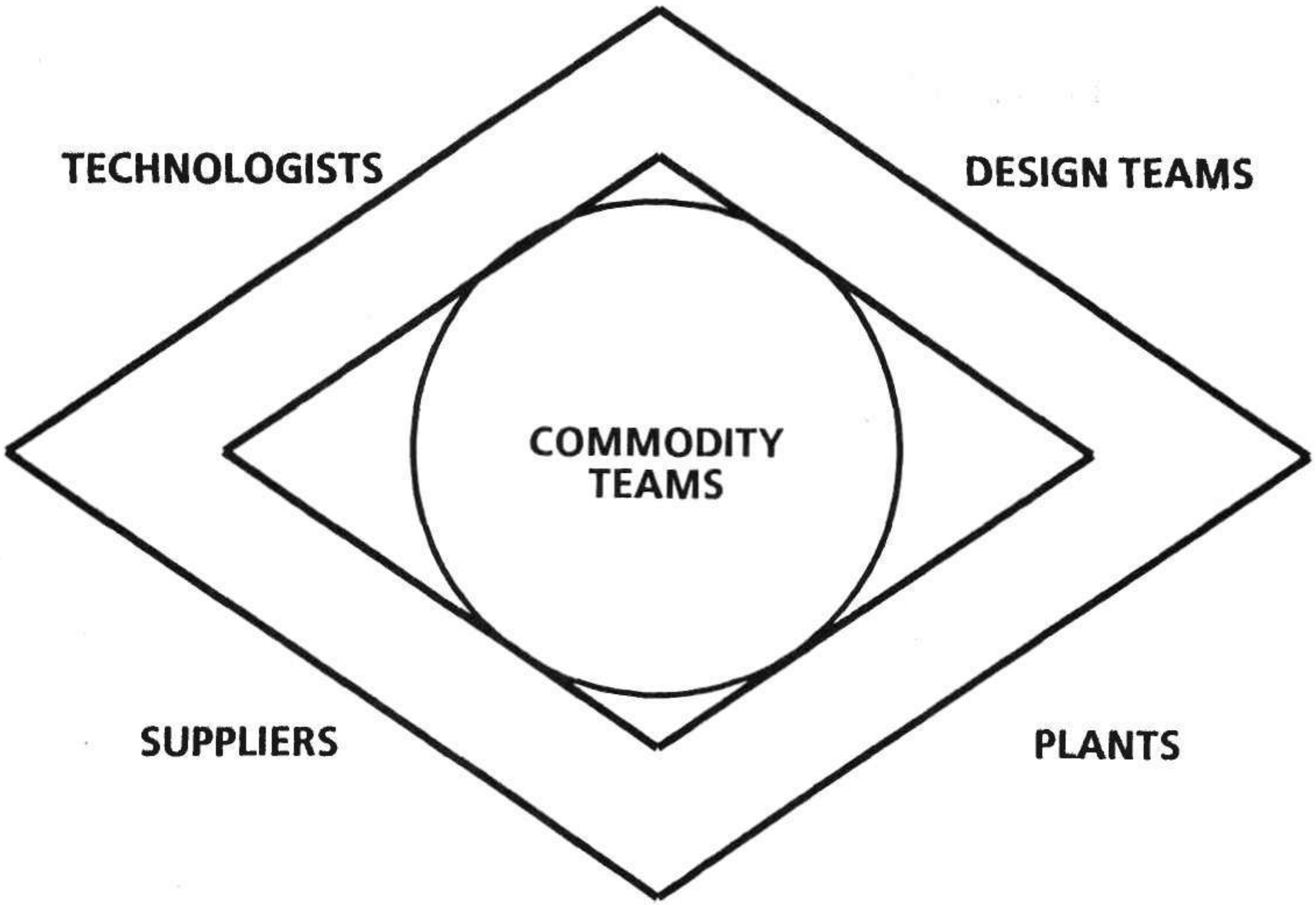
- SUPPLIER ELECTRONIC COMMUNICATION
  - ORDER RELEASES
  - ORDER STATUS
  - INVOICES

- DIRECT SHIPMENT TO POINT OF USE

- FREIGHT CONSOLIDATORS (U.S., EUROPE, FAR EAST)

- RECIRCULATING / REUSABLE PACKAGING

COMMODITY TEAMS:



MANAGE ALL ELEMENTS OF ACQUISITION FOR A PROCESS RELATED SET OF PRODUCTION (e.g. PLASTICS)

- PROCESS TECHNOLOGY
- APPLICATIONS ENGINEERING
- VENDOR BASE MANAGEMENT
- MAKE / BUY AND SOURCING DECISIONS
- DESIGN GUIDELINES
- BENCHMARKING / COST ESTIMATING

SUMMARY:

- COMPETITION FOR ALL OF US IS REAL, TOUGH AND UNRELENTING
- WE WILL NOT SURVIVE WITH "BUSINESS AS USUAL"
- JUST IN TIME PURCHASING OFFERS SIGNIFICANT OPPORTUNITIES FOR PRODUCTIVITY IMPROVEMENTS
- KEY REQUIREMENT TO JUST IN TIME IMPLEMENTATION IS A LONG TERM MUTUALLY BENEFICIAL RELATIONSHIP WITH SUPPLIERS
- THE TURNAROUND AT XEROX HAS STARTED AND WE ARE CONFIDENT OF SUCCESS

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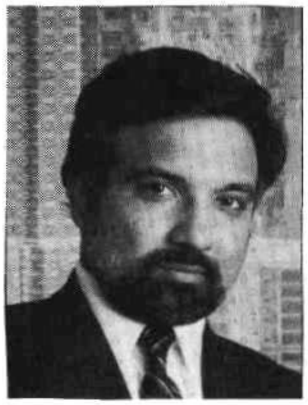
THE REVOLUTION IN PROGRAMMABLE LOGIC DEVICES



Rahul Sud
President and Chief Executive Officer
Lattice Semiconductor Corporation

Mr. Sud is President and Chief Executive Officer of Lattice Semiconductor Corporation. During his 13 years in electronics, Mr. Sud has held management positions encompassing integrated circuit design, development, and manufacturing, as well as marketing and administration. Before founding Lattice, he headed memory component engineering at Intel Corporation. Earlier, he was responsible for the development of the IMS 1400 series of fast 16K static RAMs at Inmos Corporation. He also worked at Signetics Corporation and Harris Semiconductor in development for radiation hard CMOS circuits. Mr. Sud graduated from St. Stephen's College, University of Delhi, in Physics, and from the Alliance Francaise de Delhi. He holds two master's degrees, one in Electrical Engineering from the University of California at Berkeley and one in Physics from the Florida Institute of Technology.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
October 20-22, 1986
San Diego, California

REVOLUTION IN PROGRAMMABLE LOGIC DEVICES

Rahul Sud

President and
Chief Executive Officer

LATTICE SEMICONDUCTOR CORPORATION

DATA QUEST

Semiconductor Industry Conference

October 21, 1986

San Diego, California

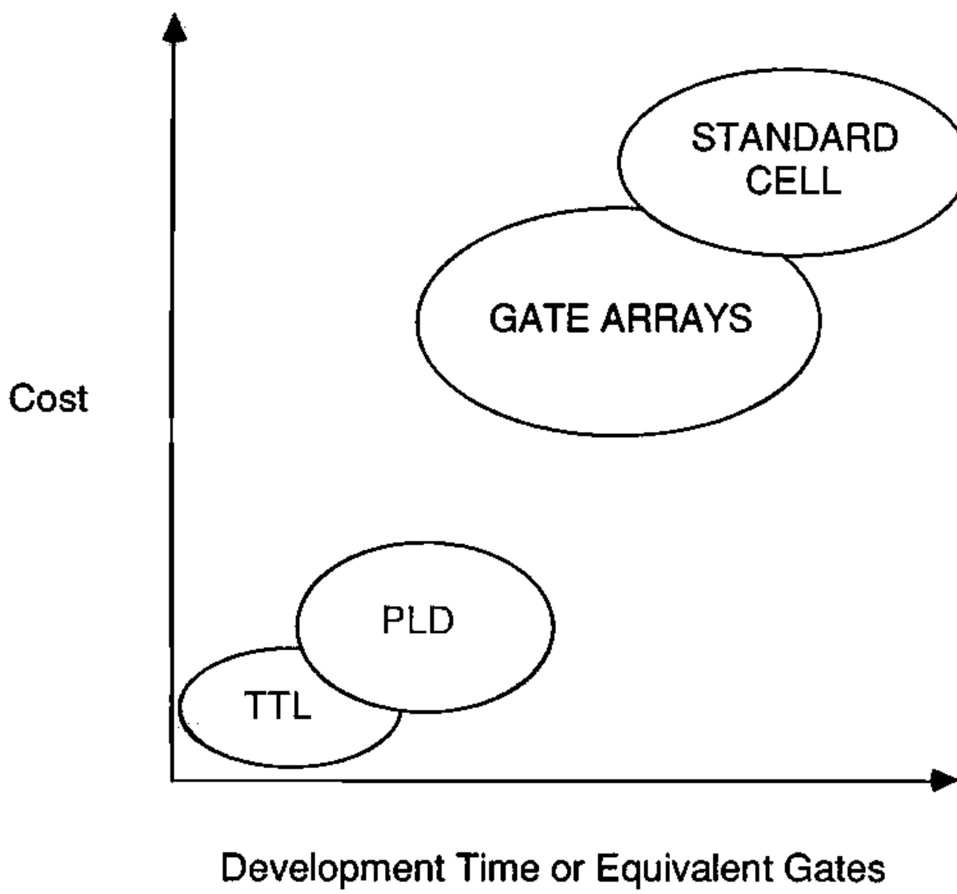
REVOLUTION IN PROGRAMMABLE LOGIC DEVICES

- Market Overview
- Today's Perspective
- Future Trends

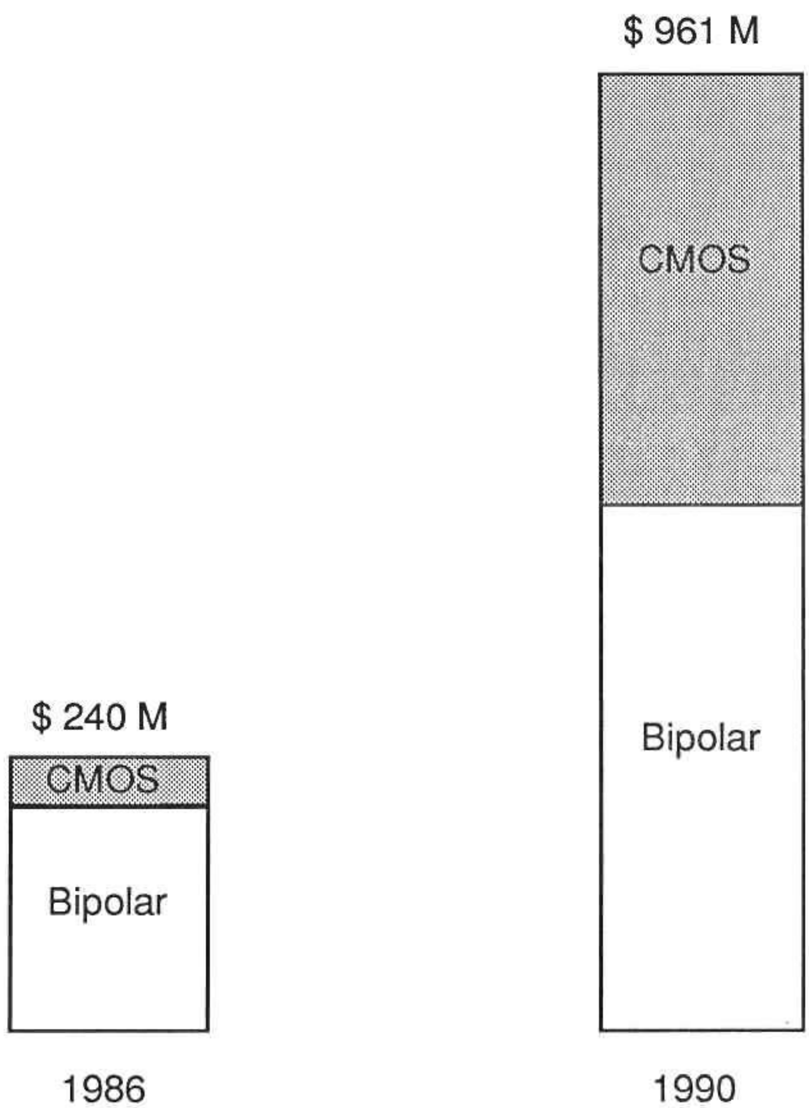
MARKET OVERVIEW

- Logic Alternatives
- Markets
- Device Features
- Technology Options

LOGIC ALTERNATIVES



MARKET SIZE - PLDs



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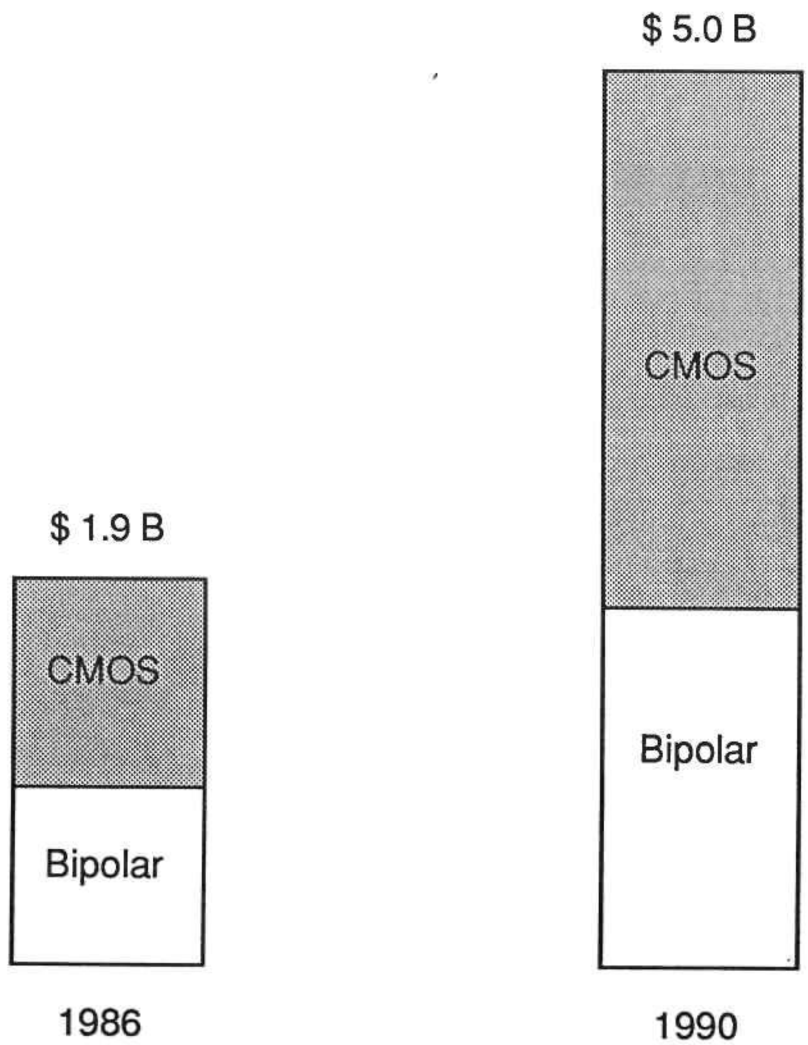
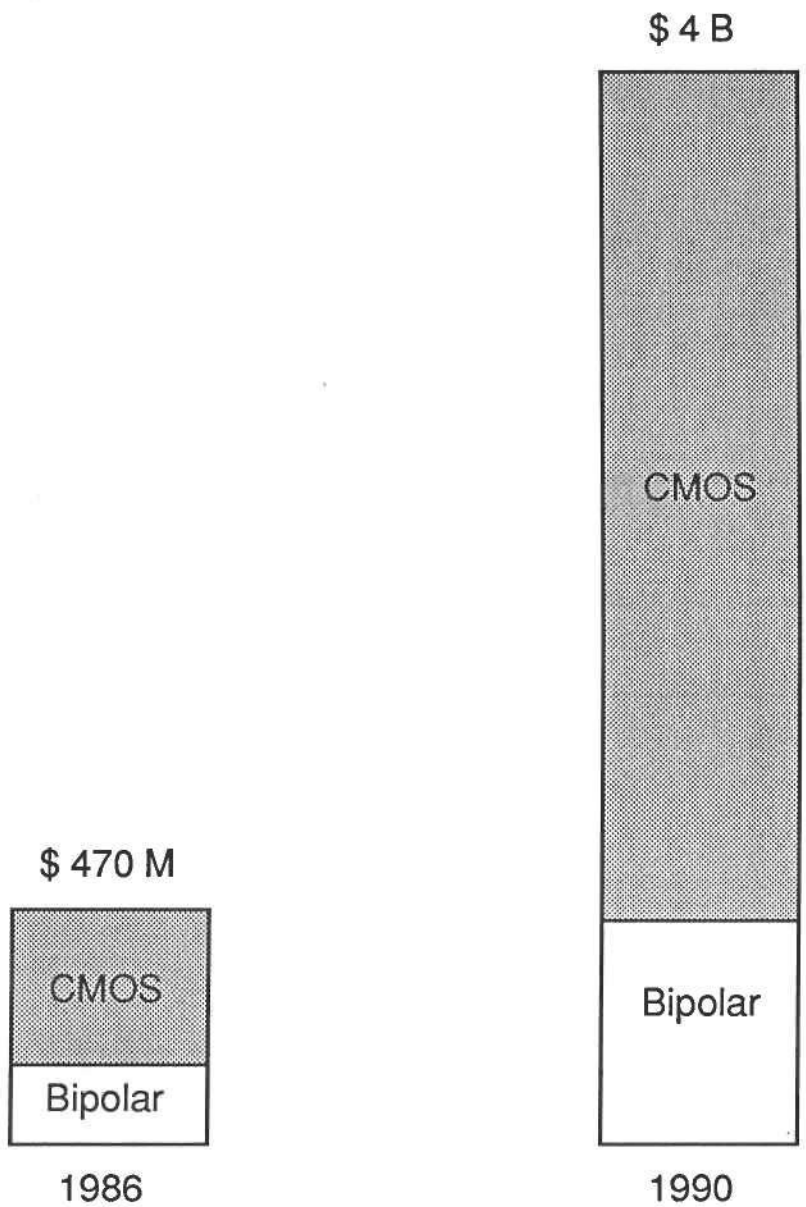
MARKET SIZE - GATE ARRAYS



MARKET SIZE - STANDARD CELL



DEVICE FEATURES

	GATES	INTEGRATION & FLEXIBILITY
• TTL	4 - 50	Low
• PLD	200 - 1800	Medium
• Gate Array	300 - 50,000	High
• Standard Cell	500 - 50,000	High

TECHNOLOGY OPTIONS

	USER PROGRAMMABLE	FIELD RECONFIGURABLE	TECHNOLOGY
• TTL	No	No	---
• PLD	Yes	Yes	Bipolar (OTP) EPROM E^2 PROM
• Gate Array	Yes	No	---
• STD Cell	Yes	Yes	EPROM E^2PROM SRAM

TODAY'S FIELD PROGRAMMABLE PRODUCTS

• PLD	-	Bipolar :	MMI, National, TI, etc.
		EPROM :	Altera, Cypress
		E^2 PROM:	Lattice
• STD Cell	-	SRAM :	Xilinx
		EPROM :	?
		E^2 PROM :	?

TECHNOLOGIES

	USER PROGRAMMABLE	FIELD RECONFIGURABLE	TECHNOLOGY
• TTL	No	No	---
• PLD	Yes	Yes	EPROM E^2 PROM Bipolar
• Gate Array	Yes	No	---
• STD Cell	Yes	Yes	EPROM E^2PROM SRAM

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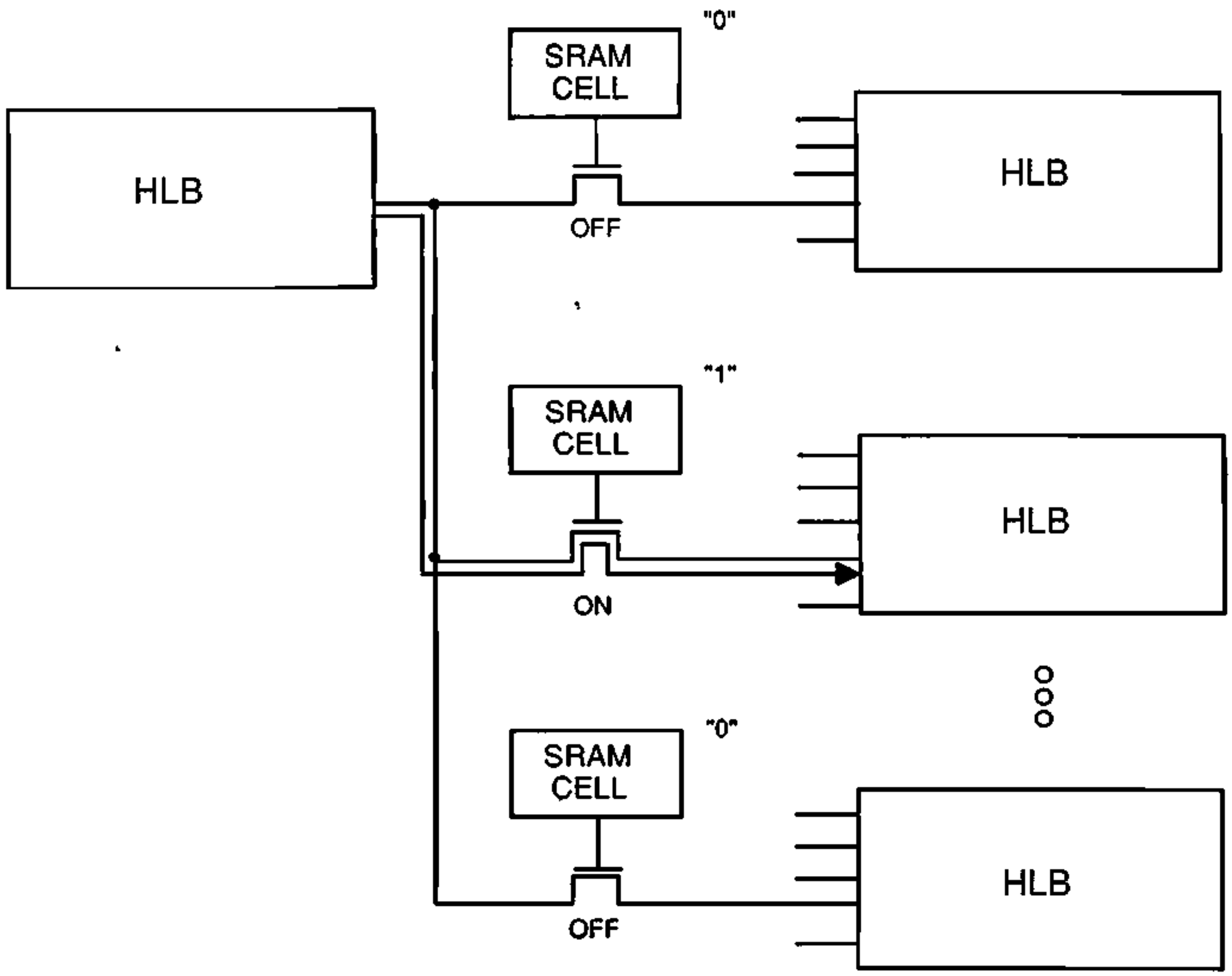
STANDARD CELL + SRAM = YES

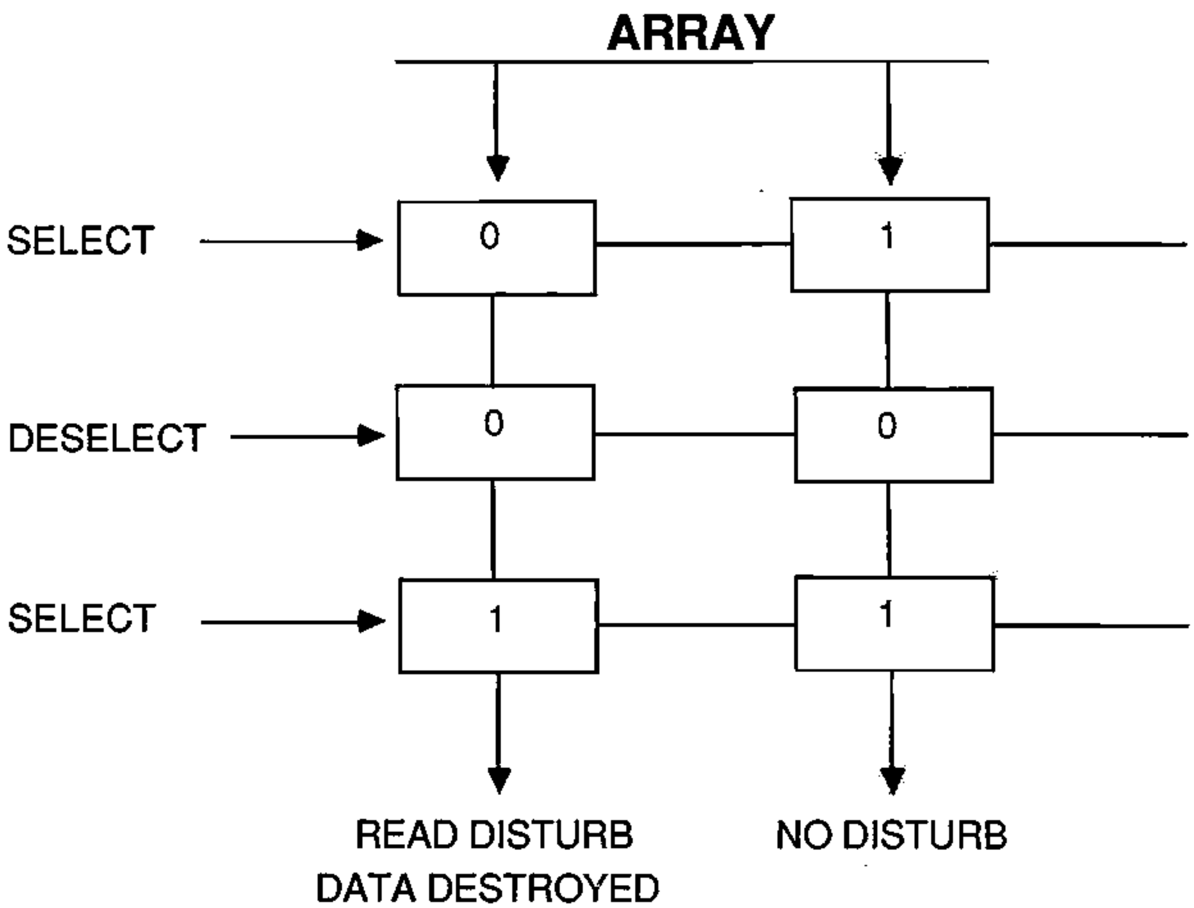
Static RAM Cells can be used to control " transfer gates" to route logic signals.



SRAM CELLS CONTROL SIGNAL ROUTING
(SIGNAL DOES NOT PASS THROUGH CELL)

PLD + SRAM = NO

Static RAM cells do not lend themselves to "array oriented" logic device which require the logic signal to pass through the programmable cell.


ARRAY
SELECT
DESELECT
SELECT
0
1
0
0
1
1
READ DISTURB
DATA DESTROYED
NO DISTURB

USER RECONFIGURABLITY

Only EPROM and E^2 PROM technologies can provide reconfigurability for both PLD and standard cell devices.

SELF ADAPTIVE TECHNOLOGY

or in-system reconfigurable logic

• PLD	E^2 PROM
• STD CELL	SRAM E^2 PROM

IN - SYSTEM RECONFIGURABLE PROGRAMMABLE LOGIC DEVICES

- Standard Cell

- PLD

Only possible with E^2 CMOS™ technology

E^2CMOS is a trademark of Lattice Semiconductor

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E^2 CMOS - THE IDEAL TECHNOLOGY FOR PROGRAMMABLE LOGIC DEVICES

- Testability
- Performance
- Low Power
- In-System Reconfigurable
- Flexibility
- Non-Volatility

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NO OTHER TECHNOLOGY

CAN OFFER ALL THIS

CHALLENGES & TRENDS FOR THE FUTURE

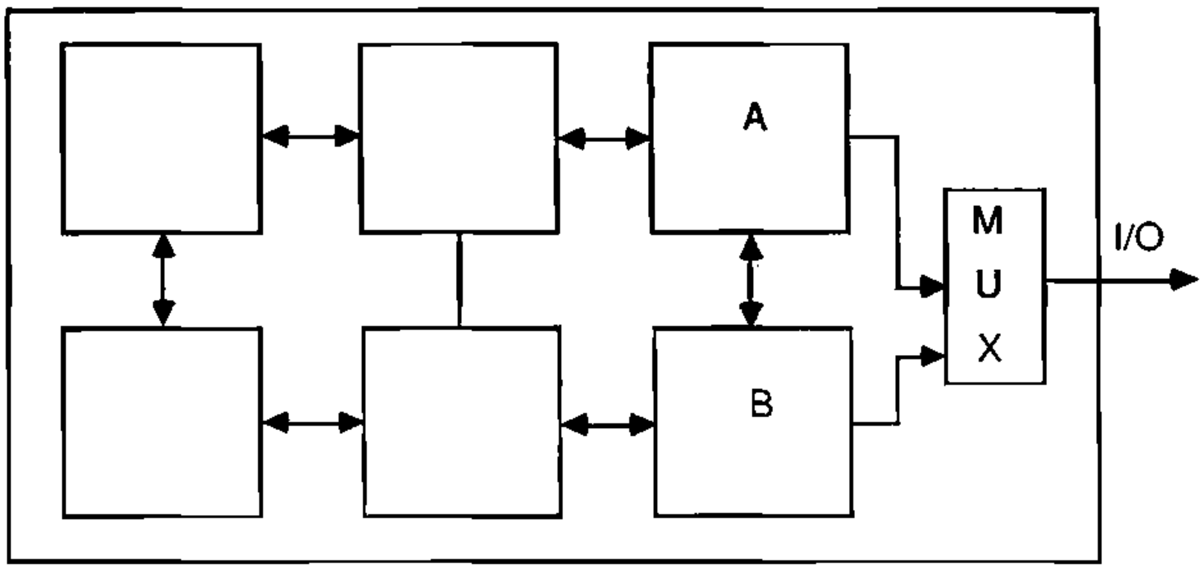
- Applications
- Hardware & Software Development Tools
- Product & Architectures

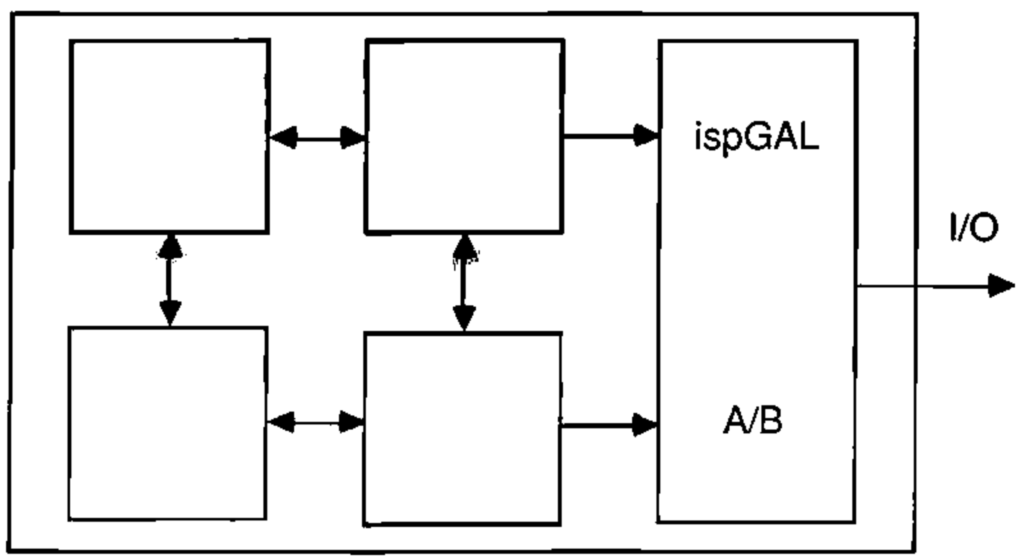
NEW APPLICATIONS

The self adaptive reconfigurable logic technology will open up revolutionary new applications and simplify present ones.

- Robotics
- Industrial Control
- Military - Electronic Warfare
- Hardware/Software anti-piracy interlock
- Electronic Security Systems

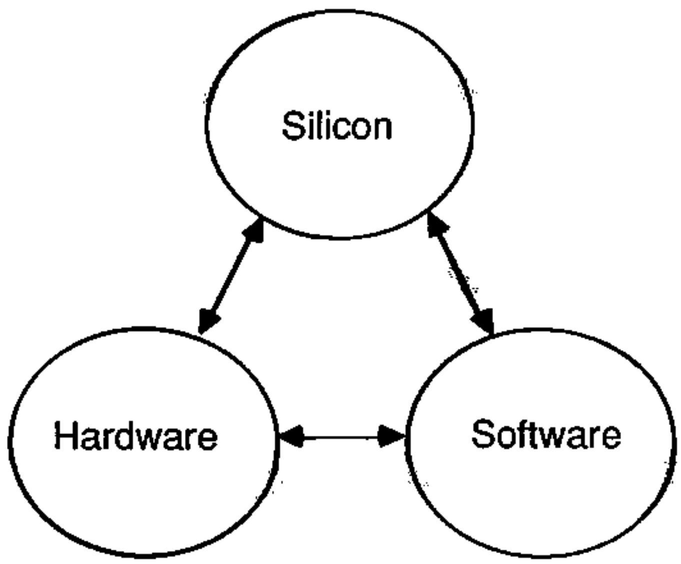
TIME - MULTIPLEXED INTEGRATED FUNCTIONALITY





- 2 FUNCTIONS X 2 DEVICES
- MANY FUNCTIONS X 1 DEVICE

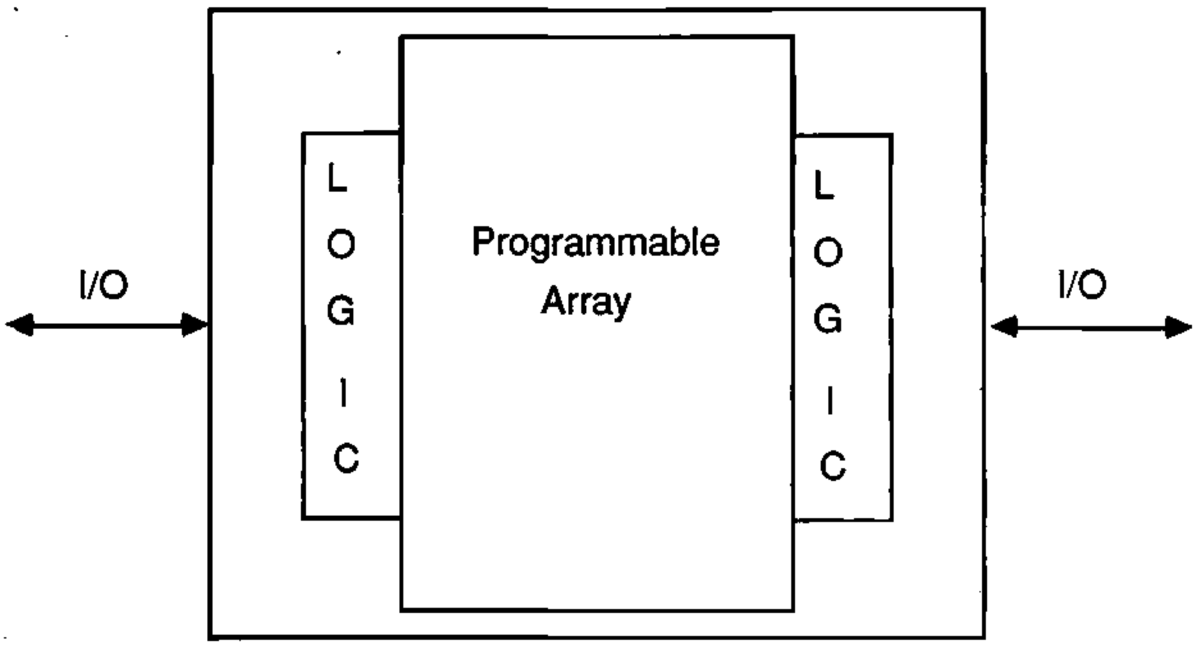
HARDWARE & SOFTWARE DEVELOPMENT TOOLS



New design methodology will be required to take

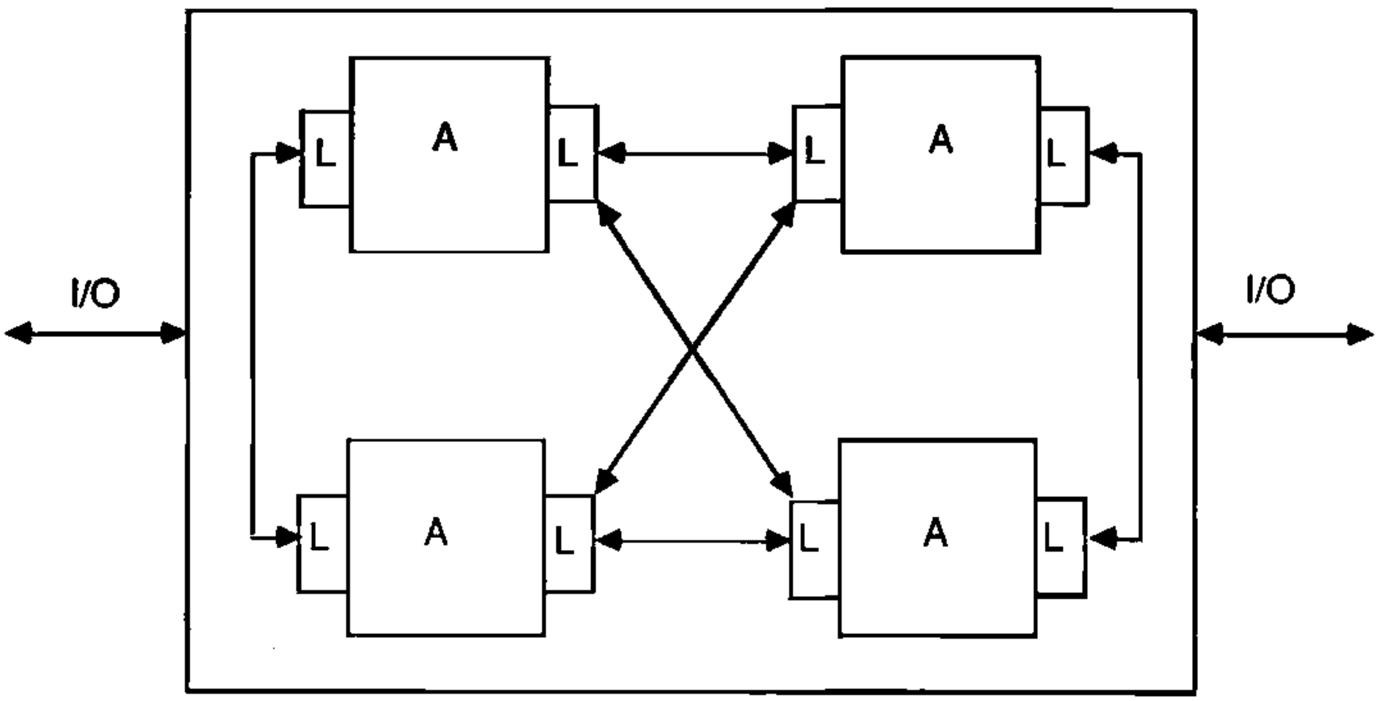
advantage of this new generation of logic products.

PRODUCTS & ARCHITECTURES 1



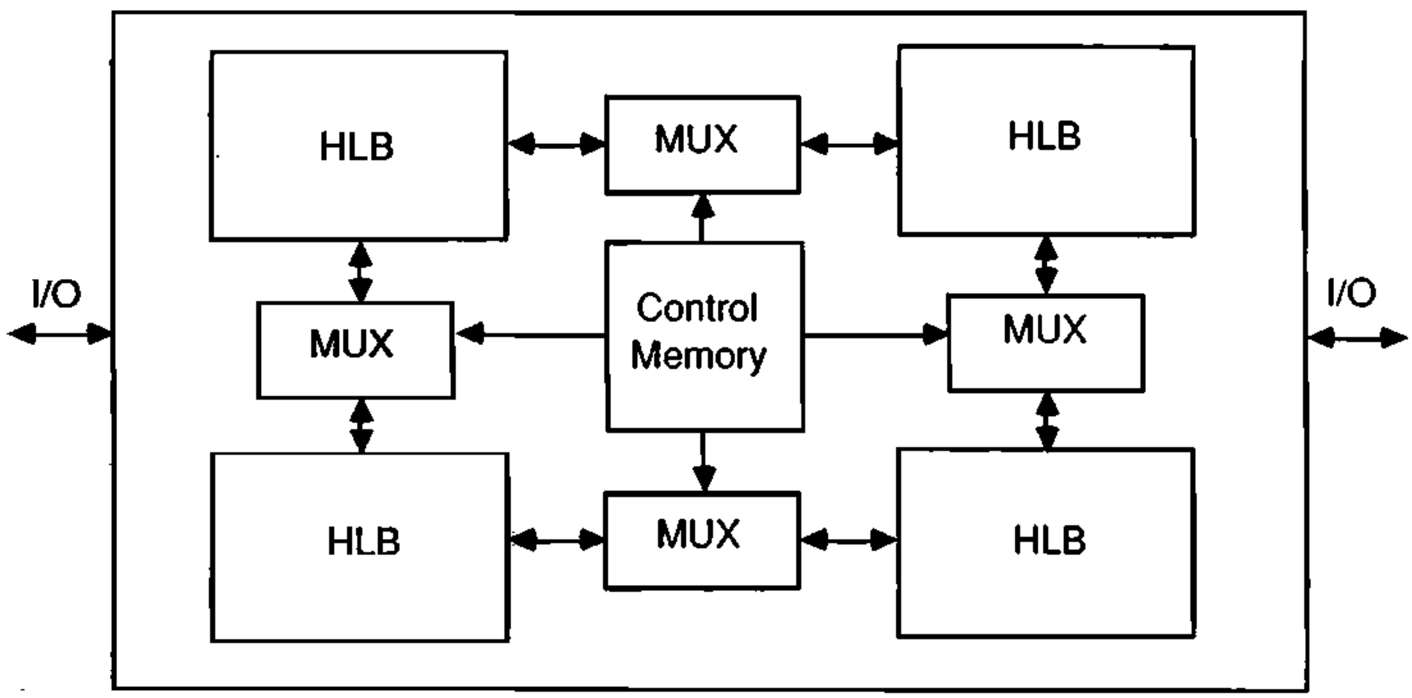
Large Array

PRODUCTS & ARCHITECTURES 2



Distributed Local Arrays

PRODUCTS & ARCHITECTURES 3



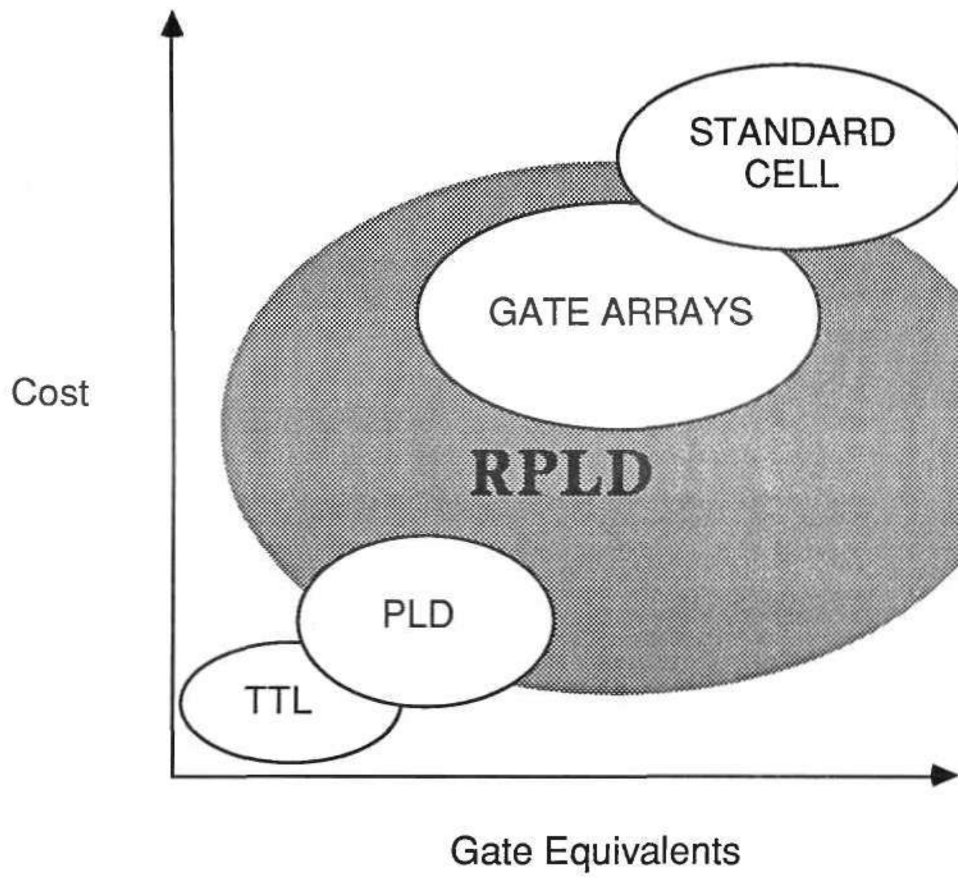
Hardwired Logic Blocks With

Programmable Channel Routing

CHANGING INDUSTRY

All the answers are not clear today, but these revolutionary logic devices are going to change the industry in a significant way.

A NEW MARKET


STANDARD
CELL
GATE ARRAYS
Cost
RPLD
PLD
TTL
Gate Equivalents

RPLD

Reconfigurable

Programmable

Logic

Device

The E^2CMOS revolution will create a new multi-billion dollar logic market within the next 10 years.

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ASICs: THEIR EVOLUTION FROM A USER'S PERSPECTIVE

Prakash Bhalerao
Senior Group Manager
Semiconductor Division
Digital Equipment Corporation

Mr. Bhalerao is a Senior Group Manager in the Semiconductor Division at Digital Equipment Corporation. Previously, he held management positions in market research, product planning and development, and semiconductor technology acquisition and engineering. Five years ago, Mr. Bhalerao founded a group to service the product development engineers within Digital to design their PC boards directly on silicon. This "ASIC Center" is now well recognized throughout the semiconductor vendor community. Earlier, he was a director of custom LSI design and a manager and team leader in Digital's Small System Development Group.

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ASICs: THEIR EVOLUTION

A USER PERSPECTIVE

PRAKASH BHALERAO

ASIC BUSINESS

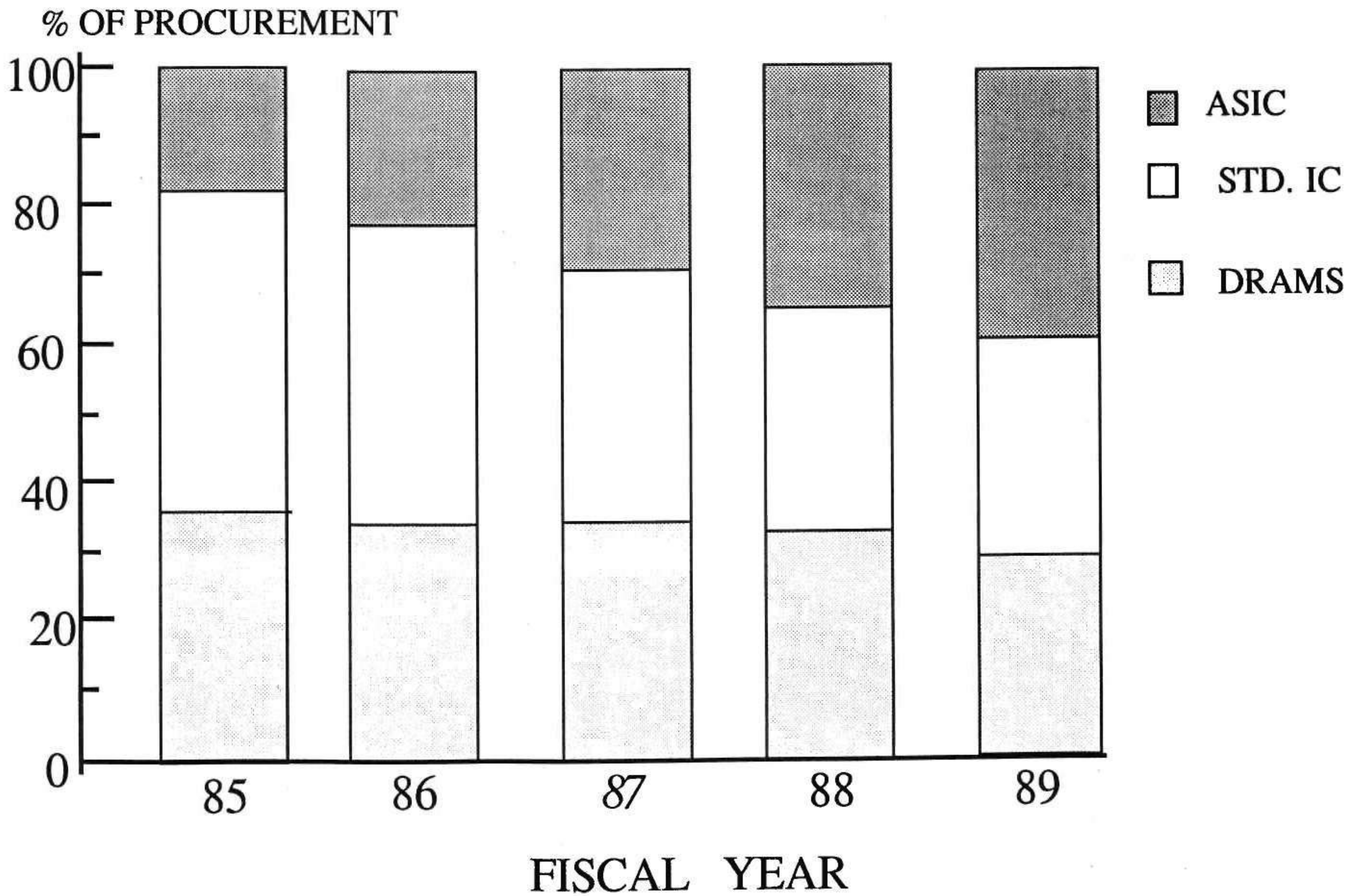
DIGITAL EQUIPMENT CORP.

■ EVERY PRODUCT THAT
DEC WILL DESIGN AND MARKET
WILL HAVE
SEMI CUSTOM IC
DESIGNED INTO IT.

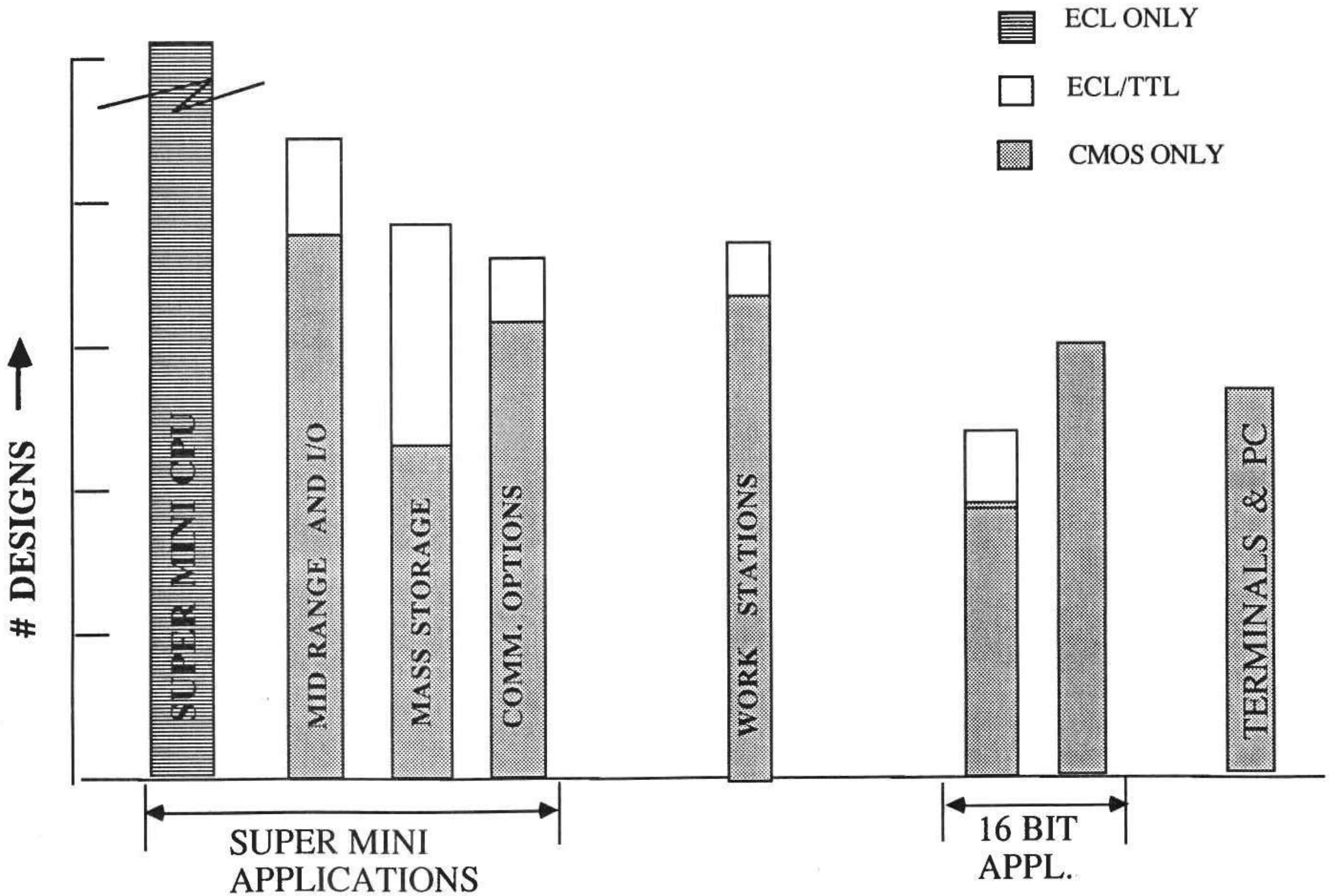
ASIC CENTER

1982

EXTERNAL IC COMMODITY SUMMARY
DIGITAL EQUIPMENT CORPORATION



ASIC DESIGN IN BY MAJOR CATEGORY



■ ASIC CENTER PHILOSOPHY

- PUTTING SILICON DESIGN CAPABILITY INTO THE HANDS OF SYSTEM DESIGNERS

- LOGIC INTENSIVE VS PROCESS INTENSIVE DESIGN METHODOLOGY

ERGONOMIC NEEDS OF 80'S PRODUCTS

CONTROL OF THE DESIGN ENVIRONMENT WITH

" LEVELS OF ABSTRACTION"

PLATFORM AND SUPPLIER INDEPENDENT TOOLS

PREDICTABLE LOGIC AND PERFORMANCE LIBRARIES

■ ■ ■

ALL THE BENEFITS OF MOVING INTERCONNECT
ON SILICON.

QUICK TURN AROUND TIME TO PROTOS

CONTROL OVER THE SUPPLIER BASE IN PENETRATION
ACQ. , SOURCING & PRICING STRATEGIES.

E. D. P. MARKET ASIC VIEW

SUPER MINI & PERIPHERALS.

ECL, ECL/TTL AND H. P. CMOS TECHNOLOGY.

CHARACTERISTICS:

OPTIMAL SILICON INTERCONNECT

SIMULATION DEPENDENT DESIGNS.

Q.B.T.A. AND LAYOUT INTERFACE

CO-DEVELOPMENT OF TECH AND TOOLS

LOW VOLUME, HIGH # OPTION MARKET

MULTI YEAR PROJECTS

SBC'S AND TERMINALS

DOMINANT CMOS TECHNOLOGY

CHARACTERISTICS:

TIME TO MARKET

VERY COST SENSITIVE

MATURE TECHNOLOGY

PROVEN DESIGN TECHNIQUES

DENSITY, POWER DISSIPATION

MID VOLUME LOW # OPTION
MARKET

E. D. P. MARKET ASIC VIEW

SUPER MINI & PERIPHERALS.

ECL, ECL/TTL AND H. P. CMOS TECHNOLOGY.

APPLICATIONS:

CPU KERNELS, (G/A AND COMPILERS)

32 BIT S.B.C'S

HIGH SPEED DISK CONTROLLERS

INTELLIGENT COMM INTERFACES

GRAPHIC SUBSYSTEMS

CLUSTER CONTROLLERS

HIGH SPEED BUS TRANSLATORS

SBC'S AND TERMINALS

DOMINANT CMOS TECHNOLOGY

APPLICATIONS:

16 BIT GP'S AND SBC'S

PC'S AND PERIPHERALS

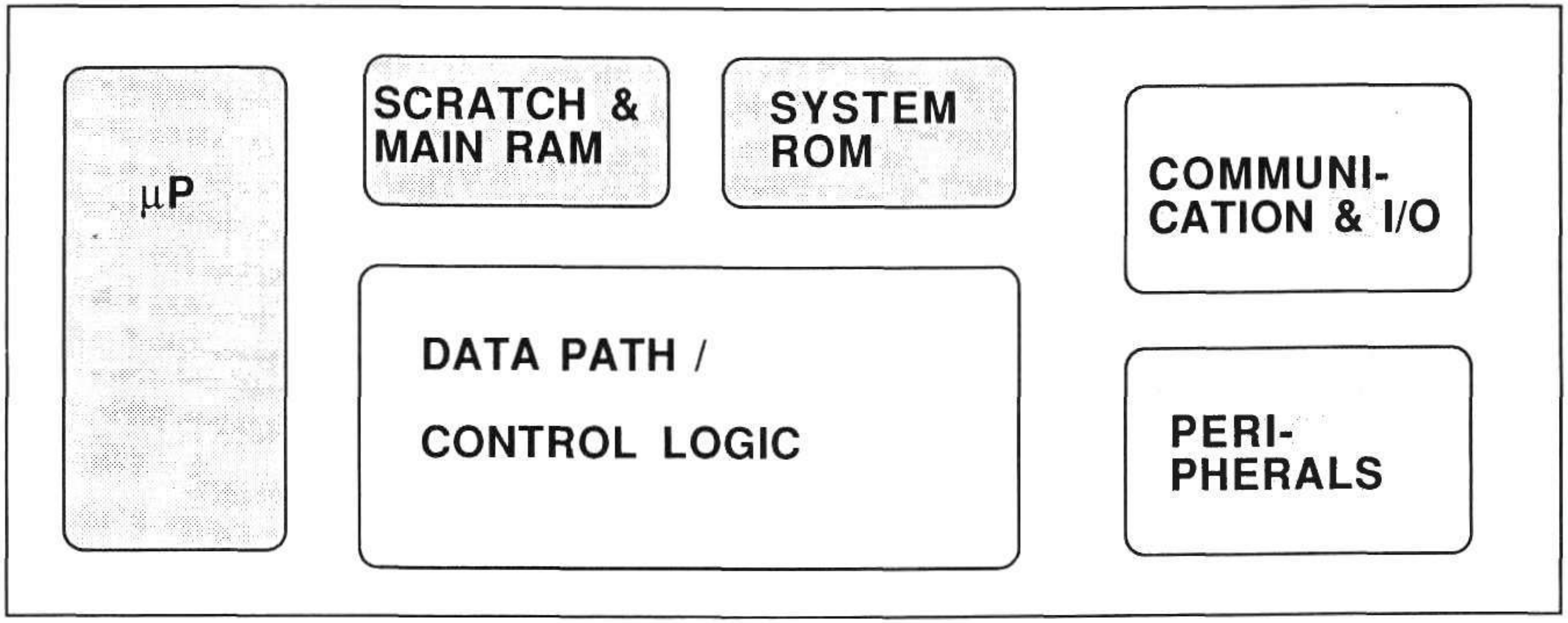
TERMINALS

PRIMARILY USED IN THE REDUCTION OF REAL ESTATE &POWER BUDGET

ASIC DESIGN TREND

FUNCTIONALITIES INTEGRATION

SINGLE BOARD COMPUTER TODAY



μP

- 8 BIT: Z80, 8051, 6800
- 16 BIT: 8086, 80286, 68000
- 32 BIT: 68020, 80386, uVAX

RAM / ROM

- User Configurable

DATA PATH/ CONTROL

- Comb. Logic
- Latches,Muxes
- I/O Buffers

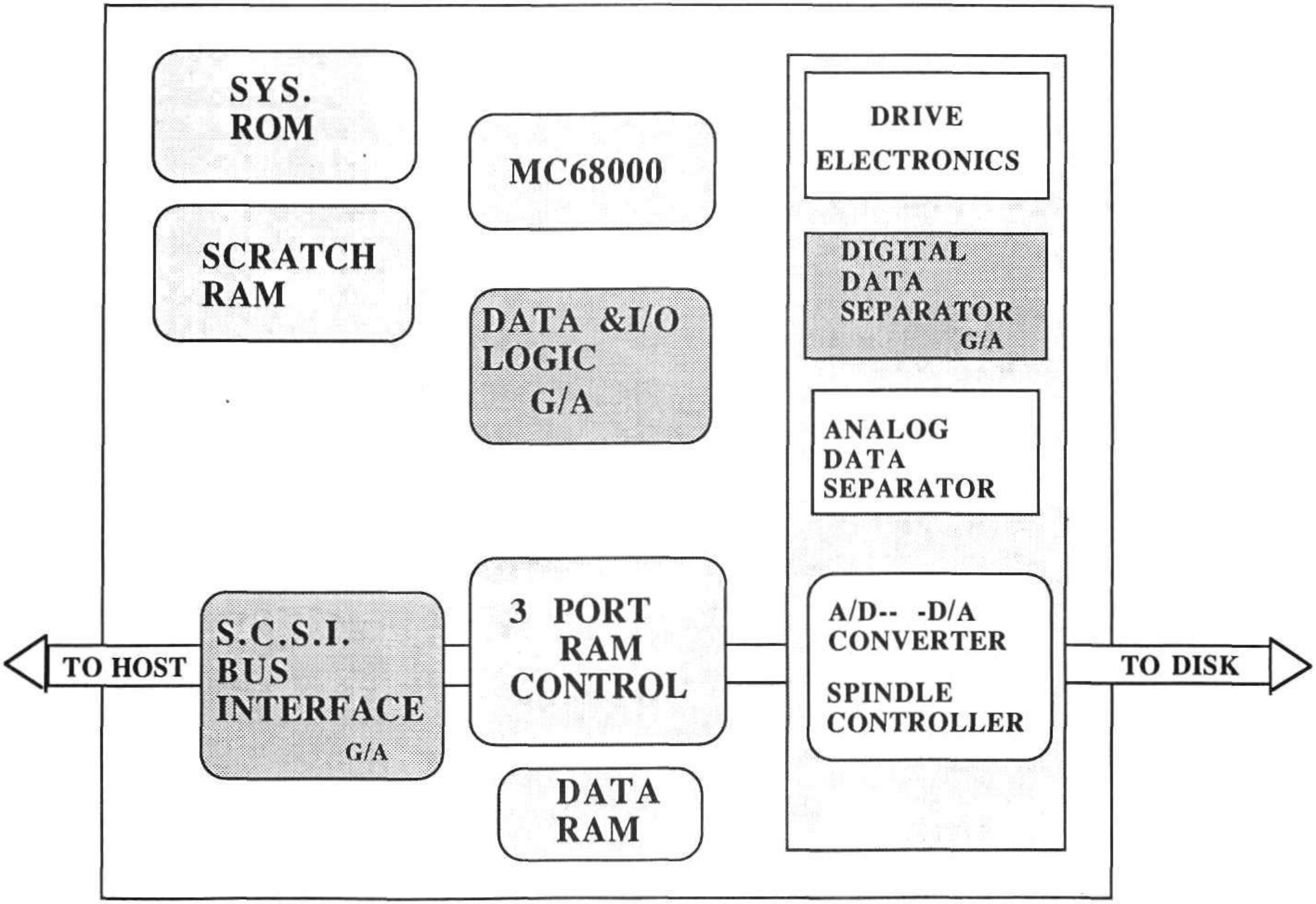
PERIPHERALS

- DMA block
- Interrupt Controller
- Clock Generator
- Peripheral Interfaces

COMM & I/O

- UARTS
- BUS Controller
- .
- ENDEC/SERDES

DISK CONTROLLER MODULE



CMOS GATE ARRAY
SINGLE BOARD COMPUTER MARKET

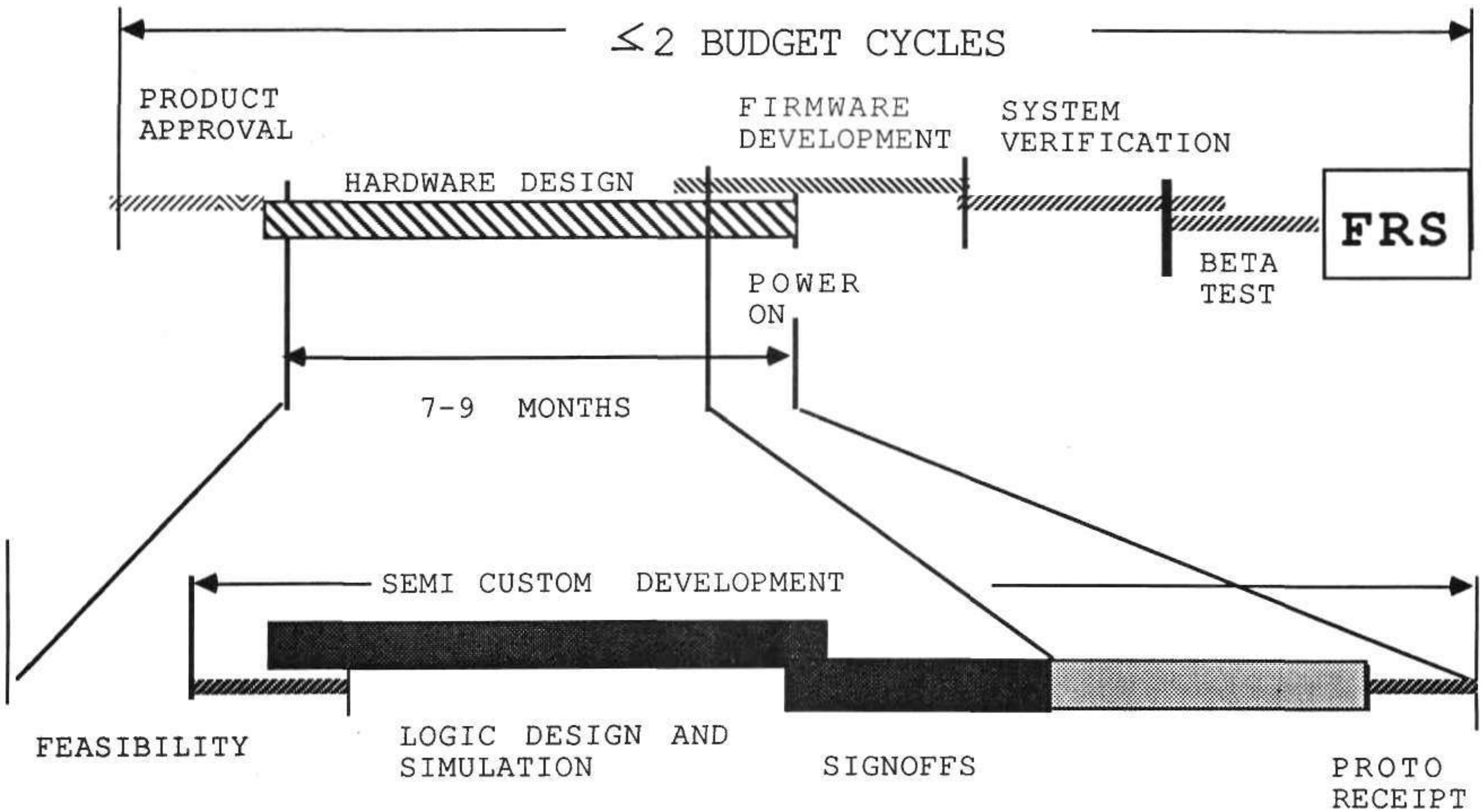
µP @ Clock	Gate Density	Package Pins	Technology[2] CMOS	Application
8 Bit , 4-6 MHz	1.5k - 2.2k	68	3um SLM	PC's, their peripherals Terminal Products
16 Bit , 8-10 MHz	2.2k - 4.2k[1]	84 - 120	3um DLM	16 Bit G.P. mini's , PC's Comm.,Console Applications
32 Bit , 10 MHz	3.2k - 6k[1]	100 - 144	2um DLM	Low-end Workstations, Intelligent Comm Controllers
32 Bit , 20 MHz	4k - 8k[1]	100 - 144	1.5um DLM	H.S. Disk and Bus Controllers,
32 Bit , > 30MHz[3]	6k - 20k[1]	144 - 256	1.2um DLM	High-end Workstations 32 Bit G.P. Superminis

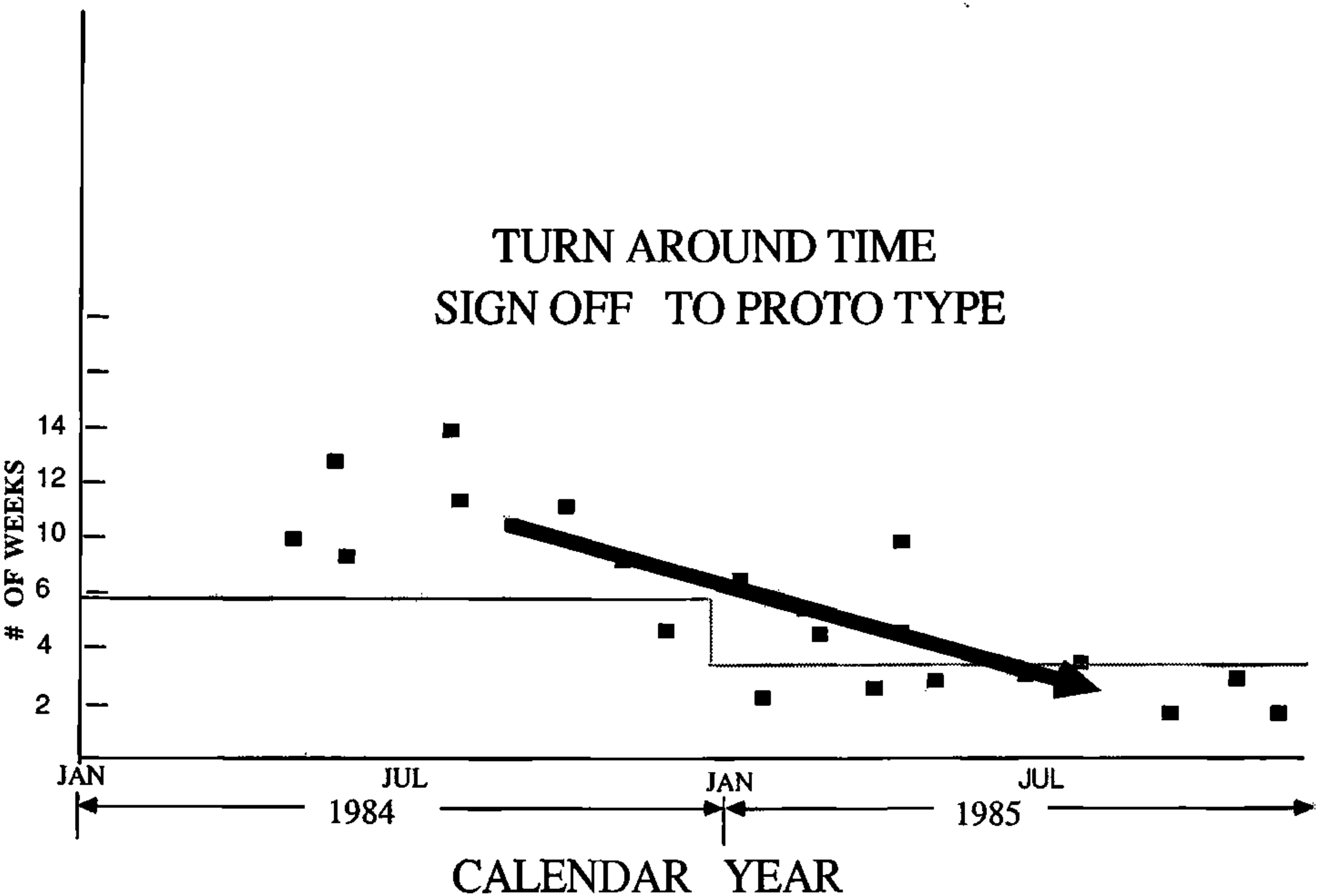
Note : 1. Multiple options

2. I/O Logic speed runs at 1.6-1.8 times the speed of the µP.

3. Estimated.

PRODUCT DEVLOPMENT CYCLE




TURN AROUND TIME
SIGN OFF TO PROTO TYPE
OF WEEKS
14
12
10
6
4
2
JAN
JUL
JAN
JUL
1984
1985
CALENDAR YEAR

- CHANGING FACE OF REVENUE SEGMENTS

  "SILICON" AND "BOXES"

  "SOLUTIONS" STRATEGIES

  INTEGRATION

- STRATEGIC ALLIANCES BETWEEN THE USER AND SUPPLIERS

  OPTIMIZE UNIT COST TO ENSURE SYSTEM COMPETITIVENESS

  LOW VOLUME HIGH COMPLEXITY PRODUCTS

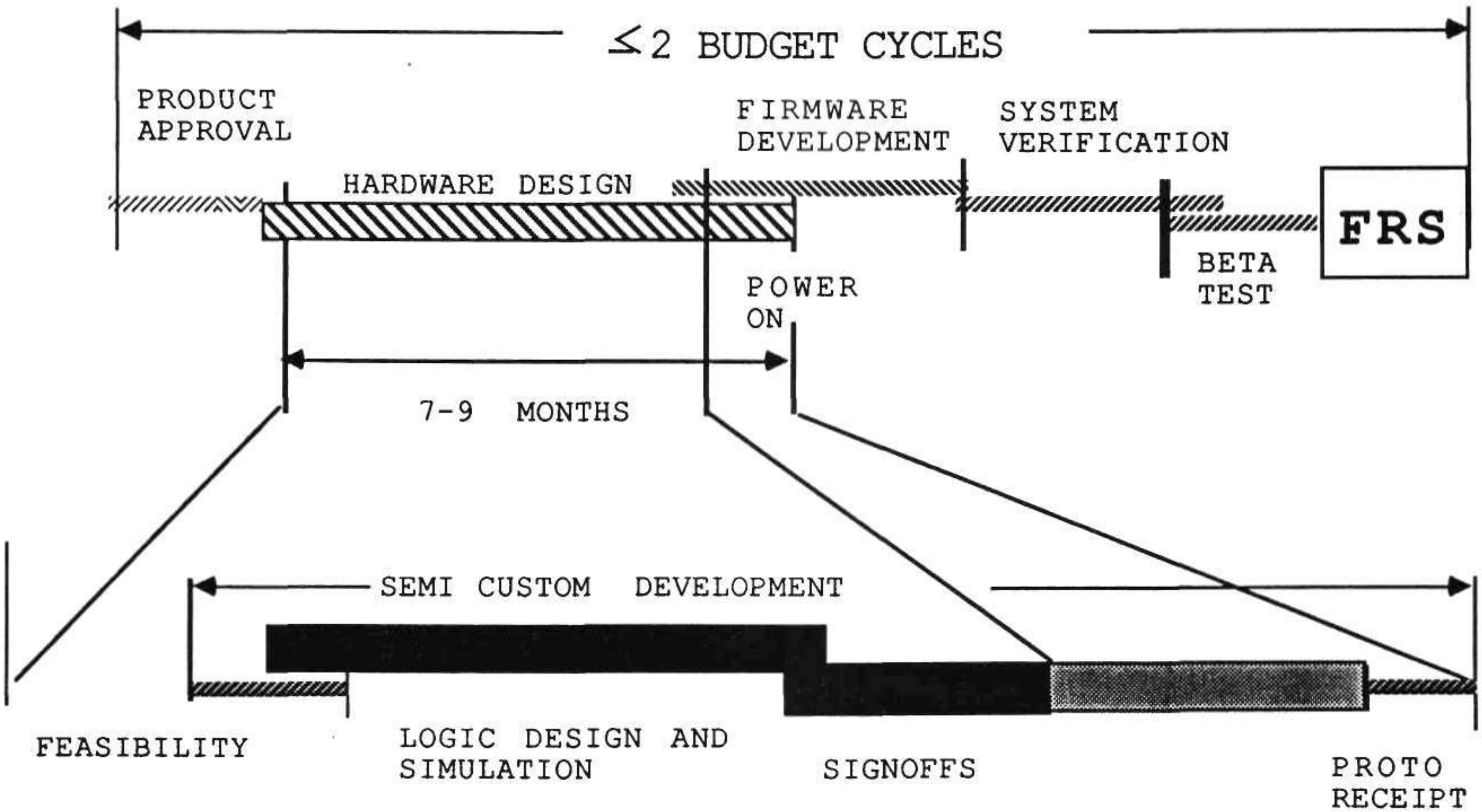
  CROSS POLINATION OF TECHNOLOGIES AND TOOLS

  SERIOUS OPTIMIZATION OF SUPPLIER BASE

  MULTIPLE SOURCING INSURANCE

  PRECEDENCE ESTABLISHED IN BIPOLAR G/A MARKET

PRODUCT DEVLOPMENT CYCLE



EDP INDUSTRY PROVIDES "THE FLY WHEEL" EFFECT TO ASIC TECHNOLOGY

CONTROL OF THE DESIGN ENVIRONMENT WITH LEVELS OF ABSTRACTION

"SILICON BREADBOARDING" TECHNIQUES

FULL INTEGRATION THRU THE SYSTEM DESIGN METHODOLOGY

DENSITY , PERFORMANCE , INTERCONNECT REQUIREMENTS

MASK PROGRAMMABLE VS FULLY PROGRAMMABLE ASICS

ASIC CENTERS WITH IN USER COMMUNITIES

FLEXIBLE MANUFACTURING WITH EOQ = 1

"SUBCONTRACTORS" MANAGEMENT

INVENTORY, AND OBSOLESCENCE STRATEGIES

DISTRIBUTION & MANUF. REPS SELECTION AND SUPPORT

USER CHALLENGES

Dataquest

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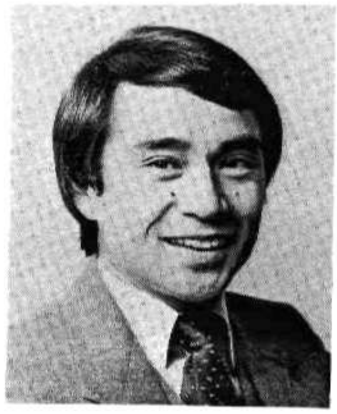
JAPAN'S SHIFT TO CREATIVE RESEARCH



Sheridan M. Tatsuno
Senior Industry Analyst
Japanese Semiconductor
Industry Service
Dataquest Incorporated

Mr. Tatsuno is a Senior Industry Analyst for Dataquest's Japanese Semiconductor Industry Service. He is responsible for analyzing trends in Japanese government policies, procurement, financial markets, industrial financing, subsidized R&D, overall economics, and industrial plant siting. Prior to joining Dataquest, he had seven years of experience in market research, planning and international finance with Bechtel Corporation and Woodward-Clyde Consultants. Mr. Tatsuno received a B.A. degree in Political Science from Yale University and a master's degree in Planning and Policy Analysis from Harvard University's Kennedy School for Government. In addition to these credentials, Mr. Tatsuno is fluent in Japanese, French, and Spanish, and authored a book entitled _The Technopolis Strategy: Japan, High Technology, and the Control of the 21st Century_.

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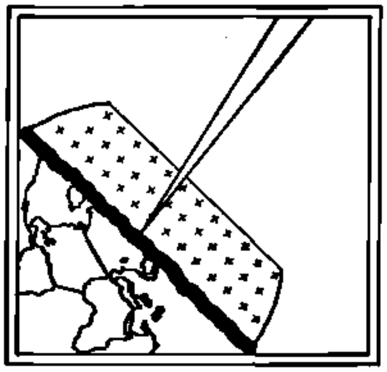
SEMICONDUCTOR INDUSTRY CONFERENCE
October 20-22, 1986
San Diego, California



Recovery: Managing the New Industry Structure

JAPAN'S SHIFT TO CREATIVE RESEARCH

SHERIDAN TATSUNO

Senior Industry Analyst
Japanese Semiconductor Industry Service
Dataquest Incorporated

MYTHS ABOUT JAPAN

#1: Japanese are copycats, not inventors.

#2: Japan is weak in software.

#3: Japan lacks entrepreneurs and start-ups.

#4: Silicon Valley will always be #1.

#5: Japan can't foster creativity.

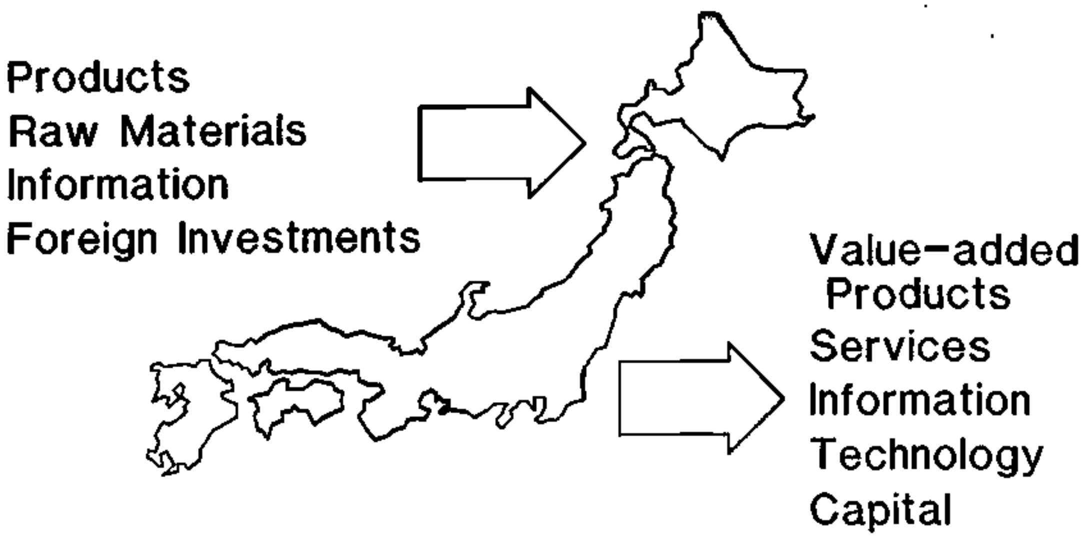
"The next revolutionary advance in technology should come by the beginning of the next century, most probably from Japan."

Dr. Michiyuki Uenohara
Executive Vice President
NEC Corporation

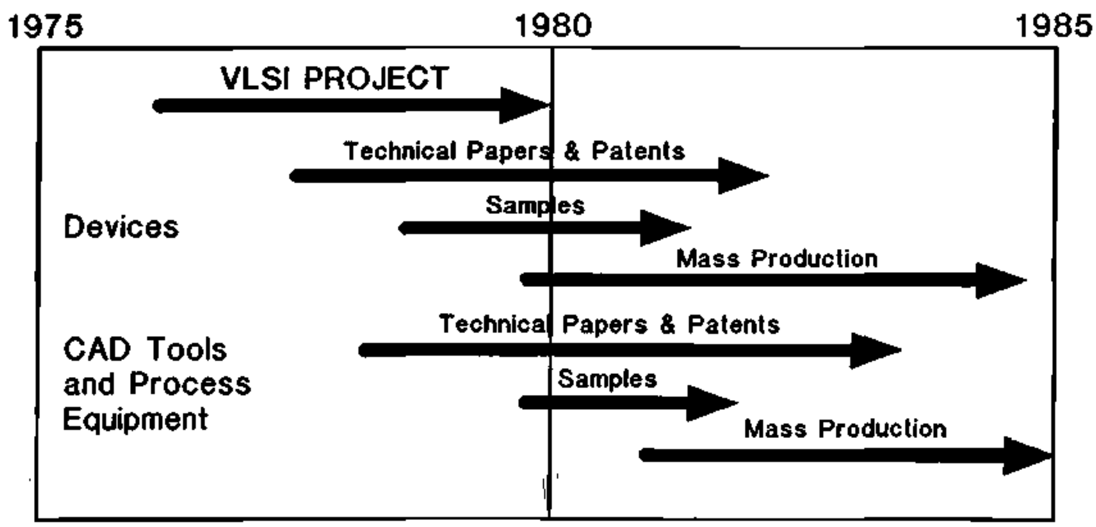
CHALLENGES FACING JAPAN

- Strong yen
- Growing trade friction and protectionism
- "New Japans" emerging
- Aging population
- "My-home-ism"
- Desire for more leisure time

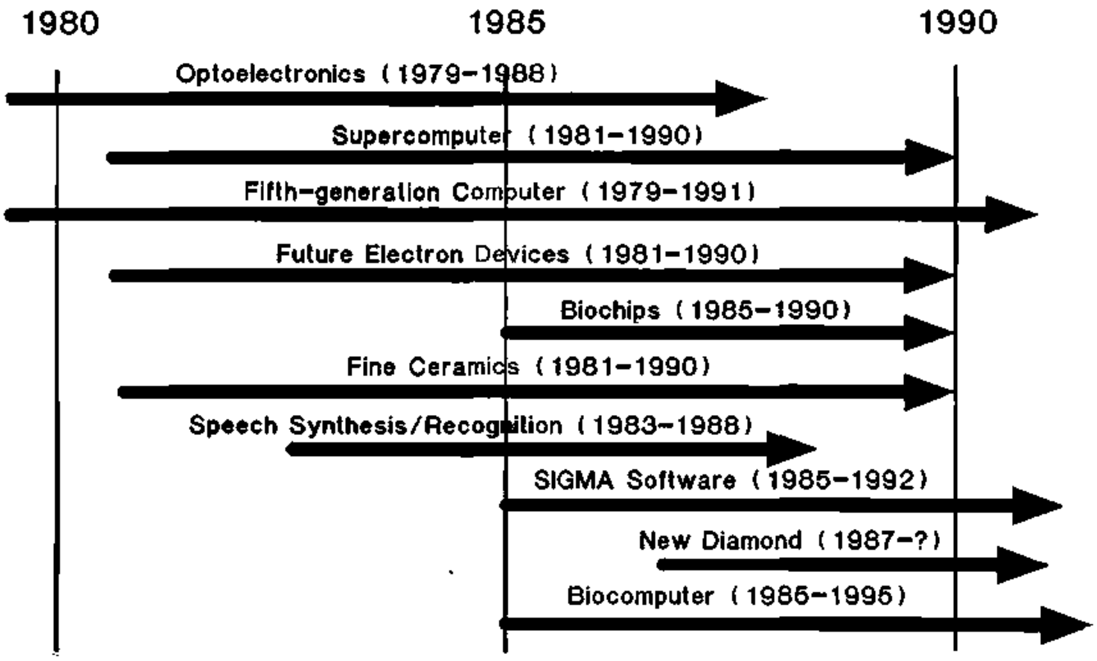
INDUSTRIAL STRATEGY OF "JAPAN TECH"



JAPANESE IC DEVELOPMENT CYCLE



MITI JOINT R&D PROJECTS



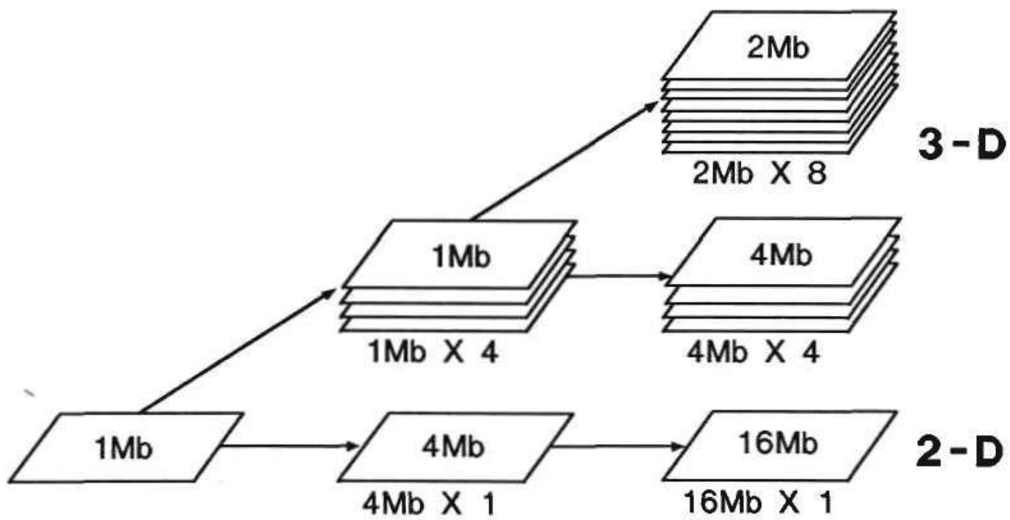
Source: Dataquest

FUTURE ELECTRON DEVICES PROJECT

Themes	81	82	83	84	85	86	87	88	89	90
Superlattices (SL)	PHASE 1 Basic SL Structure New Material System				PHASE 2 Basic Devices			PHASE 3 Integration		
Three-Dimensional ICs (3-D ICs)	PHASE 1 Multilayer Structure Process Technology				PHASE 2 Test Element Group Device Design			PHASE 3 Functional 3-D ICs Basic Technology System Design		
Hardened ICs	PHASE 1 Testing Technique Device, Process Modification			PHASE 2 Test Device		PHASE 3 Integration				

Source: Dataquest

MEGABIT MEMORIES--THE SHIFT TO 3-D ICs



Source: Dataquest

MEGABIT DYNAMIC RAM TRENDS

Sampling Year	Device	Design Rule Start	Design Rule End	Technology
1985	1Mb	1.25	1.00	Steppers (5x)
1987	4Mb	0.80	0.70	Steppers (5x)
1990	16Mb	0.50	0.30	X-ray
1995	64Mb	0.25	0.20	Synchrotron radiation
				E-beam overexposure
				Bias exposure photolitho
1998	256Mb	0.10	0.05	Synchrotron radiation
2000+	1Gb	0.05	0.01	Bioelectronics

Source: Dataquest

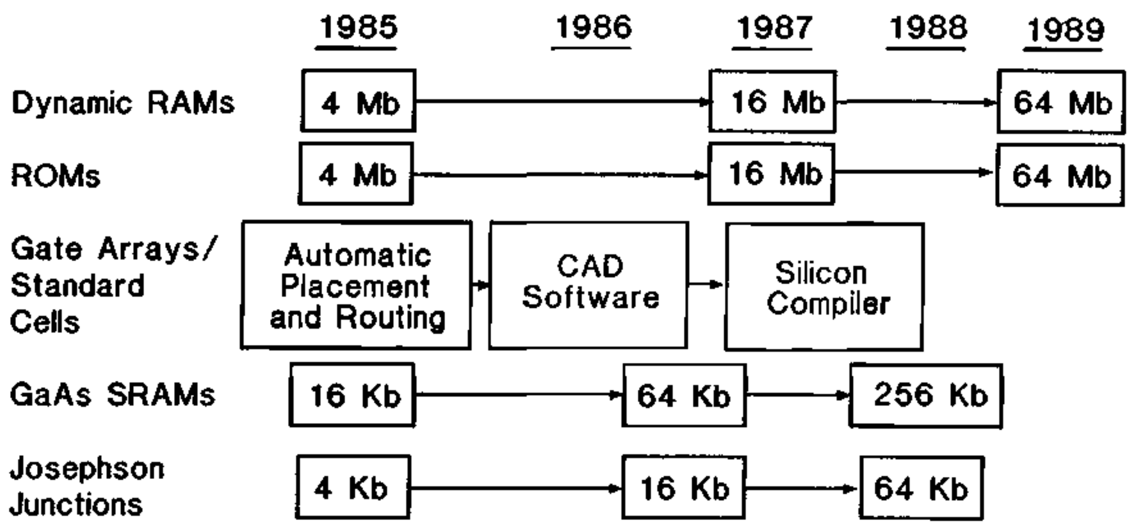
JAPANESE MEGABIT R&D PROJECTS

Start	Group	Type	Goal	$ Millions
1985	NEC/MOE Physics Lab	SOR*	1Mb+	N/A
1986	MITI/13 Companies	SOR	16/64Mb	$65
1986	Sumitomo Heavy	Excimer	16Mb+	N/A
1988	NTT/Hitachi/Toshiba	SOR	64Mb	$42
1989	MITI/Sumitomo Electric	SOR	16Mb	N/A

*SOR = Synchrotron orbital radiation
N/A = Not available

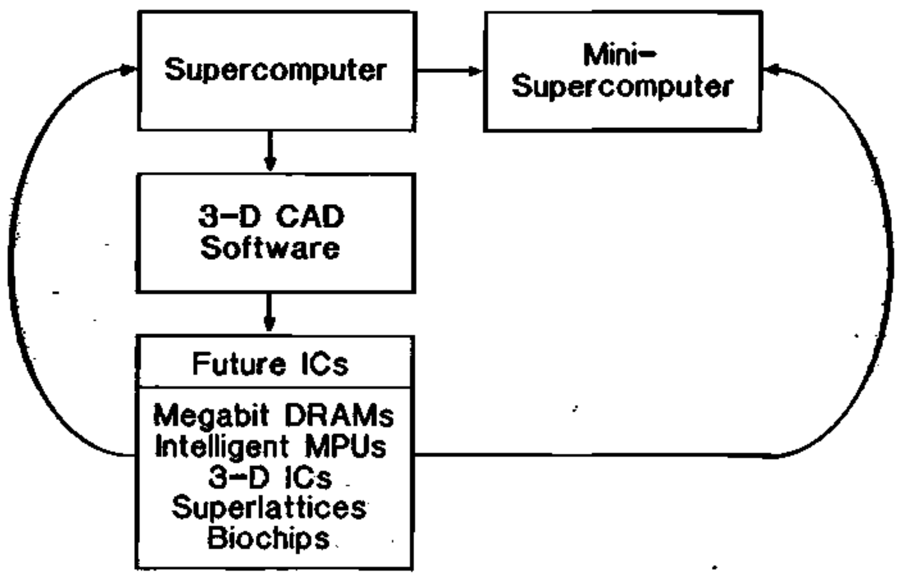
Source: Dataquest

FORECAST OF NTT RESEARCH PAPERS



Source: Dataquest

FUTURE SUPERCOMPUTER CAD TOOLS

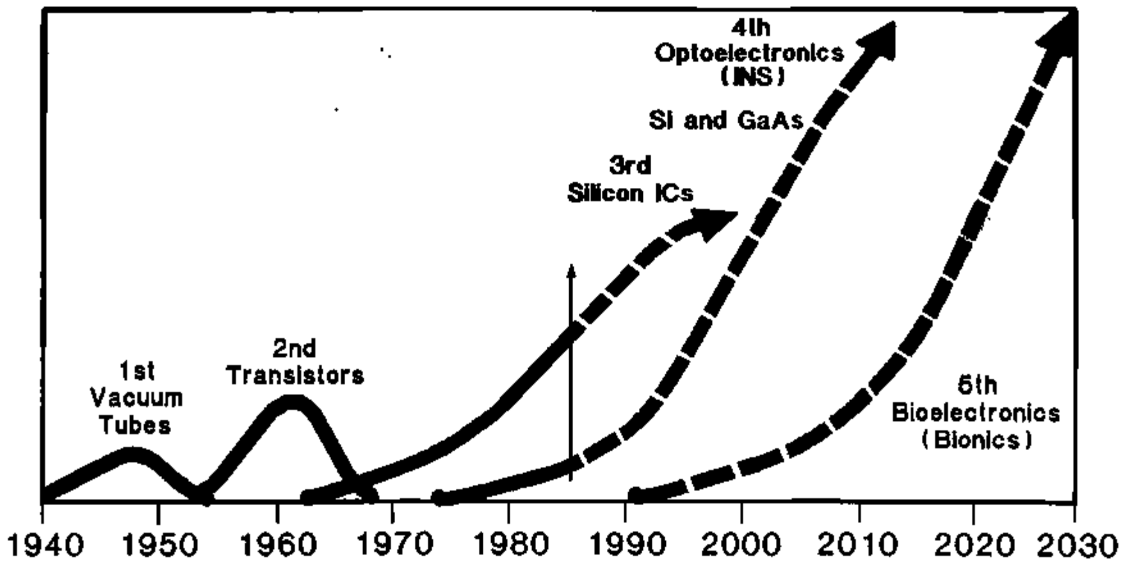


SMART CARDS--THE NEXT PC MARKET?

Start	Group Leader	Application	IC Device
Dec. 1984	Mitsui Bank	Banking and Shopping	64K EPROM with 8-bit MPU
March 1985	Seibu Bank	Medical	16K EEPROM with CPU
May 1985	Sumitomo Bank	Shopping	64K EEPROM with CPU
July 1985	Toyo Trust Bank	Financial Management	64K EPROM with CPU
Aug. 1985	Dai-Ichi Kangyo	Banking	64K EPROM with CPU
Oct. 1985	Sanwa Bank	Shopping	64K EEPROM with CPU
Oct. 1985	Fuji Bank	Corporate Banking	16K EEPROM with CPU
Oct. 1985	Daiwa Bank	Shopping	16K EEPROM with CPU
Oct. 1985	Toshiba	Point-of-Sale	64K EEPROM with CPU

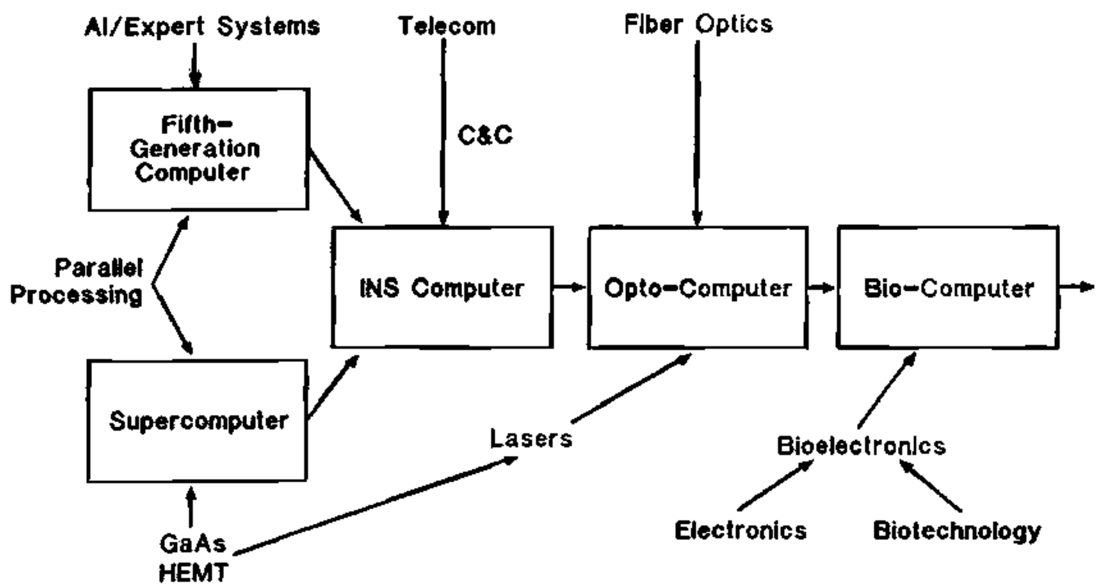
Source: Dataquest

OPTOELECTRONICS: THE NEXT GENERATION



Source: Dataquest

JAPAN'S NEXT-GENERATION COMPUTERS



Source: Dataquest

OPTICAL TECHNOLOGY R&D CORPORATION

- Goal: second-generation OEICs
- $62.5 million budget (1986-1995)
- Applications: optocomputer, optical communications
- Members:
  - Fujikura
  - Fujitsu
  - Furukawa
  - Hitachi
  - Japan Sheet Glass
  - Matsushita
  - Mitsubishi
  - NEC
  - Oki Electric
  - Sanyo
  - Sharp
  - Sumitomo Electric
  - Toshiba

THE SIXTH-GENERATION COMPUTER--
MITI'S BIO-COMPUTER PROJECT

- $40 million funding (1985–1995)
- Mimics human brain functions (pattern recognition, reasoning, and learning)
- Four research areas:
  - New computer architecture
  - Biochip development
  - Neural systems of lower animals
  - Nondestructive, noncontact methods for measuring human brain activity

BIOCHIP RESEARCH

Company	Research Focus
Asahi Chemical	Light-sensitive organic semiconductor
Dojin Chemical	Thin-film biochip substrate
Fujitsu	Biosensors, thin-films, biochips
Hitachi	Biochips, artificial intelligence
Kuraray	Implantable biosensors
MITI	Organic superconductors
Matsushita	Water-soluble photoresist
Mitsubishi	Enzyme biosensors
NEC	Medical biosensors
Sharp	Biochips, biocomputers
Toshiba	Multi-ion biosensors

NEW JAPANESE BASIC RESEARCH LABS

Year	Company	Location	R&D Focus	Facility ($M)
1985	Canon	Atsugi	AI, materials	$ 50.0
1987	Fujitsu	Kawasaki	CAD, ICs, supercomputers	$100.0
1986	Matsushita	Osaka	16Mb DRAMs, ULSI	$100.0
1985	Matsushita	Tokyo	4Mb DRAMs, VLSI	$ 80.0
1986	Mitsubishi	Itami	4Mb DRAMs, X-ray, e-beam	$106.0
1986	MITI/MPT	Tokyo	Electronics, telecom	$ 56.0
1987	NEC	Tsukuba	VLSI, AI, bioelectronics	$ 65.0

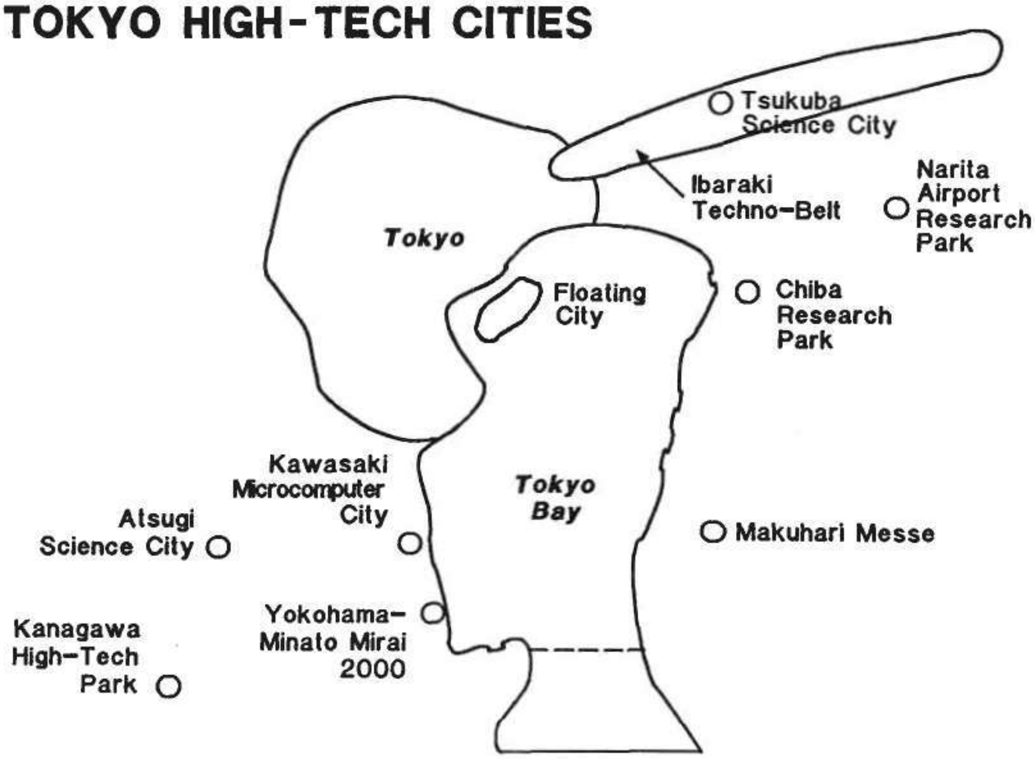
Source: Dataquest

NEW JAPANESE BASIC RESEARCH LABS

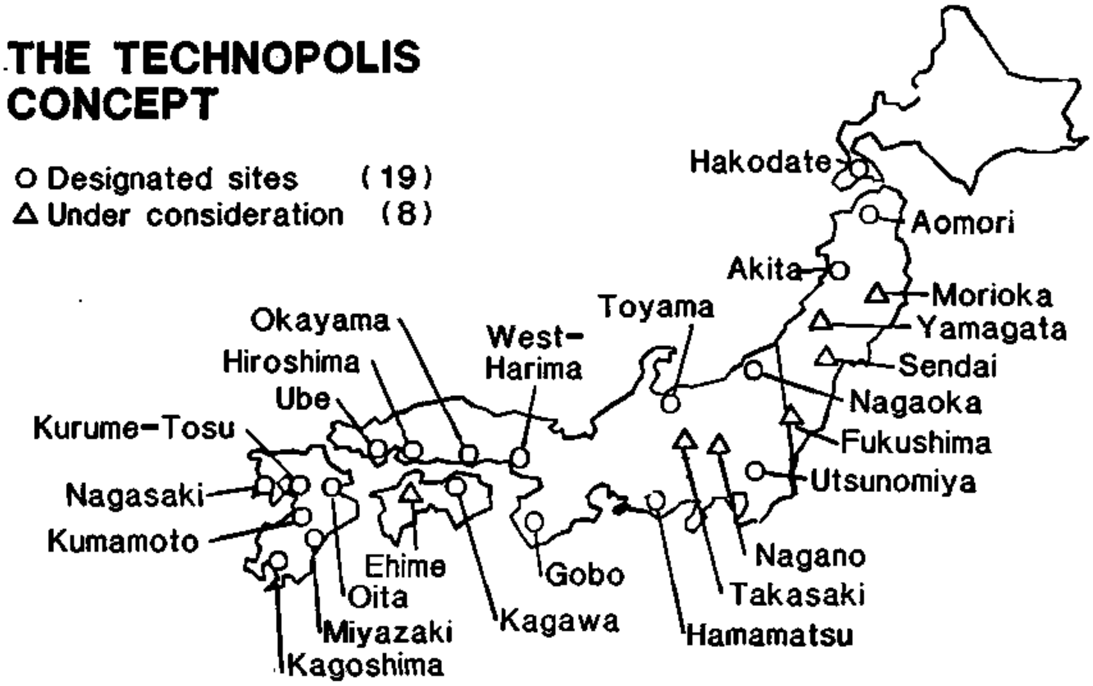
Year	Company	Location	R&D Focus	Facility ($M)
1985	NEC	Sagamihara	32-bit MPU, GaAs, opto	$100.0
1988	NTT/Hitachi, Toshiba	Atsugi	64Mb+ DRAMs, synchrotron radiation	$ 30.0
1985	Oki	Hachioji	1-micron VLSI	$ 46.5
1986	Ricoh	Yokohama	Optoelectronics, materials	$ 60.0
1985	Sanken	Saitama	Semiconductors	$116.0
1985	Sanyo	Tsukuba	Bioelectronics, AI, FA	$ 38.5
1985	Toshiba	Kawasaki	4Mb and 16Mb DRAMs	$110.0
1985	Sumitomo	Yokohama	Bioelectronics, materials, optoelectronics	$147.0

Source: Dataquest

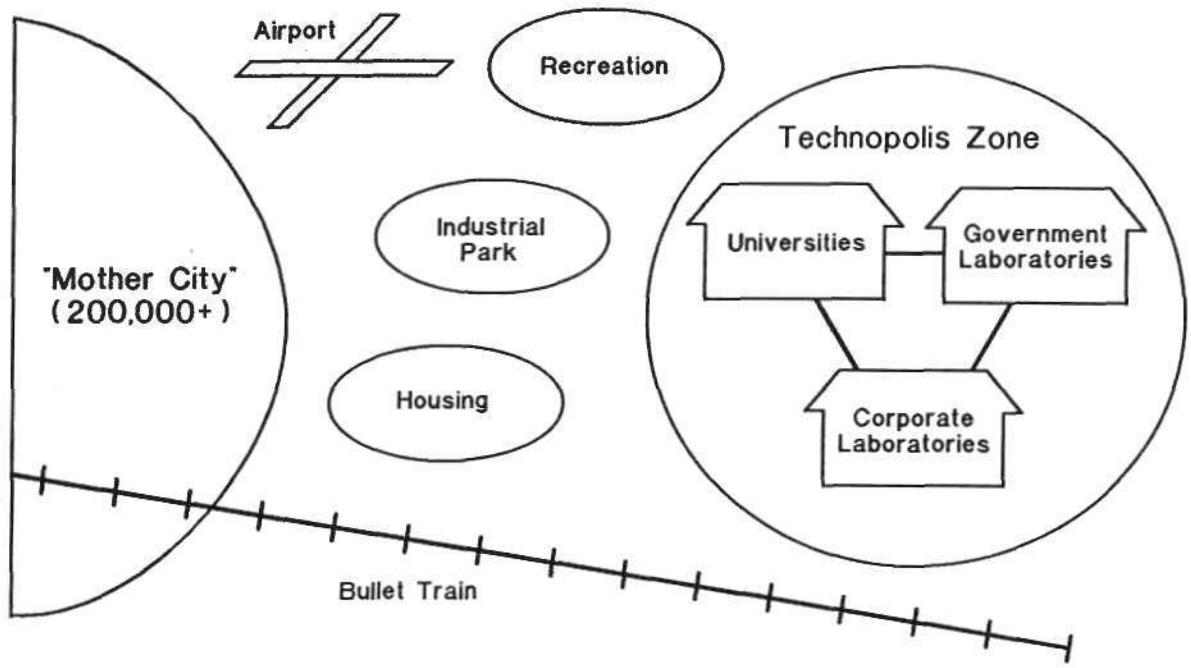
TOKYO HIGH-TECH CITIES

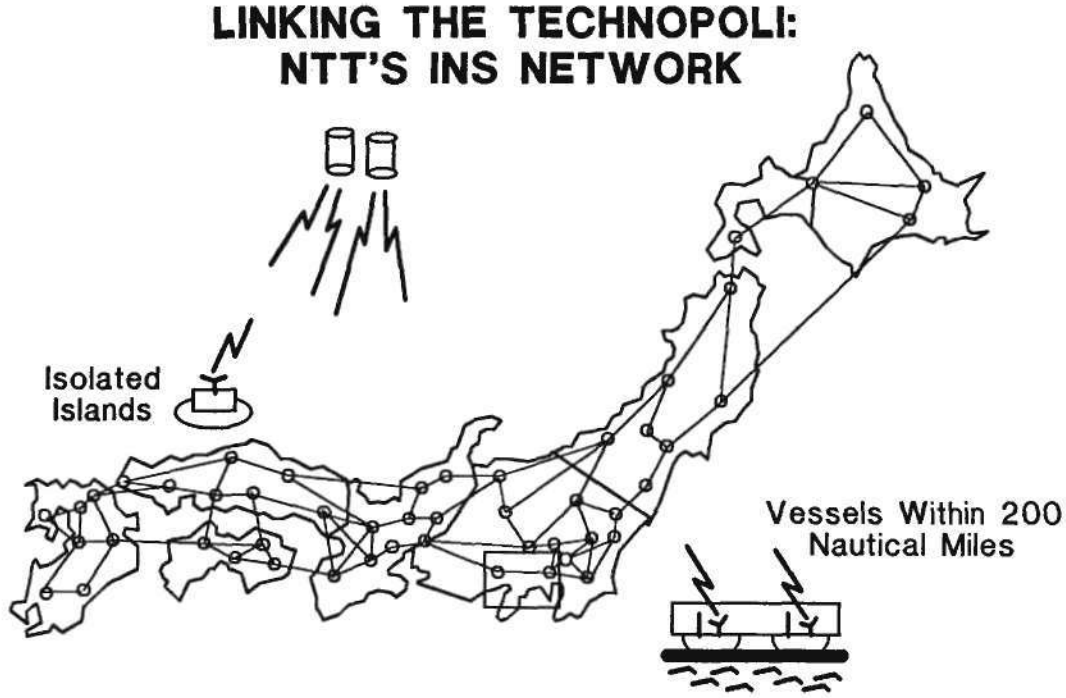


THE TECHNOPOLIS CONCEPT



TECHNOPOLIS CONCEPT




LINKING THE TECHNOPOLI:
NTT'S INS NETWORK
Isolated
Islands
Vessels Within 200
Nautical Miles

POTENTIAL CORPORATE STRATEGIES

- Better monitoring systems
- Long-term planning and investment
- Automated plants and offices
- Retain and retrain employees
- R&D and manufacturing in Japan
- Strategic alliances with Asian companies
- Constant product improvement
- Attention to details and customers

Source: Dataquest

POTENTIAL R&D CONSORTIUMS

- Telecomputing
- Home electronics
- Medical electronics
- Bioelectronics
- Factory automation
- Chemitronics
- IC cards
- Electronic banking ("zaitech")
- Military R&D commercialization
- Regional high-tech development

Table 1

JAPANESE GOVERNMENT SEMICONDUCTOR-RELATED JOINT R&D PROJECTS

DURATION	BUDGET ($M)	AGENCY	PROJECT
1979-86	$112.5	MITI	Optical Measurement & Control Systems
1979-91	375.0	MITI	Fifth Generation Computer
1981-86	11.0	STA	Perfect GaAs Crystals
1981-86	11.0	STA	Nanomechanisms
1981-90	143.7	MITI	Scientific Supercomputer
1981-90	114.0	MITI	Future Electron Devices
1981-90	50.0	MITI	Fine Ceramics
1982-87	10.0	STA	Bioholonics Systems
1983-88	10.0	STA	Bioinformation Transfer
1983-88	n/a	STA	Speech Synthesis and Recognition
1983-90	125.0	MITI	Advanced Robotics (JUPITER)
1984-90	730.0	NTT	Information Network System (INS) Computer
1985-90	n/a	STA	Solid State Surfaces
1985-91	156.3	MITI	Sigma Automated Software Development
1985-90	40.0	MITI	Biochips/Biocomputer
1985-93	n/a	MITI	Next-Generation IC Equipment
1985-88	n/a	Tokyo U.	TRON Project (32-bit MPU)
1985-?	23.5	Kyoto U.	Supercomputer (with Matsushita)
1986-96	93.6	MITI	Synchrotron Orbital Radiation (SOR)
1986-96	62.5	MITI	Optoelectronic ICs (OEICs), optocomputer
1986-96	625.0	MPT/MITI	Automated Translation Telephone
1986-88	n/a	JIRA	Robot Sensors
1986-88	n/a	MPT	High Resolution TV System
1986-?	n/a	Tohoku U.	Automotive Electronics and Materials
1987-?	n/a	MITI	New Diamond Substrates

Legend: MITI = Ministry of International Trade and Industry
MPT = Ministry of Posts and Telecommunications
STA = Science and Technology Agency
NTT = Nippon Telegraph & Telephone (privatized in 1985)
JIRA = Japan Industrial Robot Association

Source: DATAQUEST
July 1986

Dataquest

a company of The Dun & Bradstreet Corporation

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a company of
The Dun & Bradstreet Corporation

ASICs, THE REAL COST

Wayne Spence
Vice President, ASICs Division
Semiconductor Group
Texas Instruments

Mr. Spence is Vice President of the Application-Specific Integrated Circuits Division in Texas Instruments' Semiconductor Group. His previous assignments include engineering and management positions in radiation-hardened integrated circuit design, advanced IC design, photomask/design service systems planning, and design automation. He has contributed to ten patents and has published extensively with respect to semiconductor product design and design automation. Mr. Spence received B.S. and M.S. degrees in Electrical Engineering from Louisiana State University and an M.B.A. degree from the University of Dallas.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
October 20-22, 1986
San Diego, California

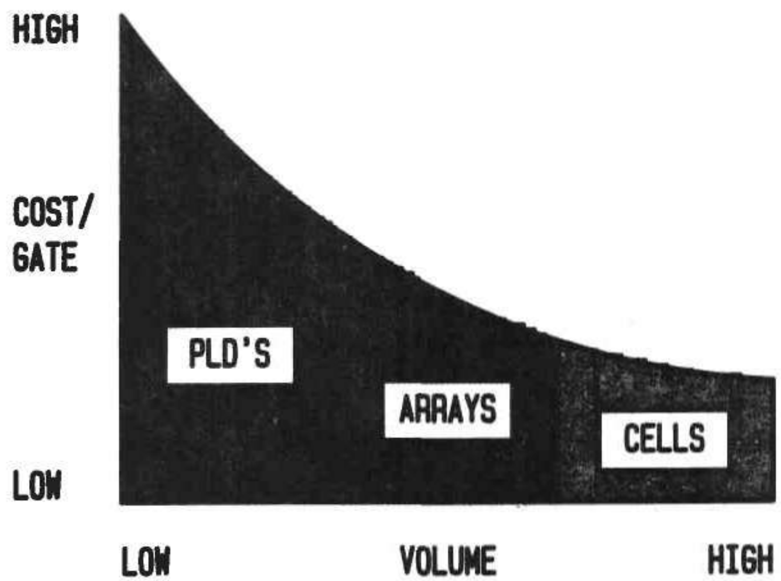
TEXAS INSTRUMENTS

APPLICATION SPECIFIC INTEGRATED CIRCUITS

"THE REAL COST"

H. WAYNE SPENCE
VICE PRESIDENT, SEMICONDUCTOR GROUP
ASIC

ASIC MARKET OVERVIEW



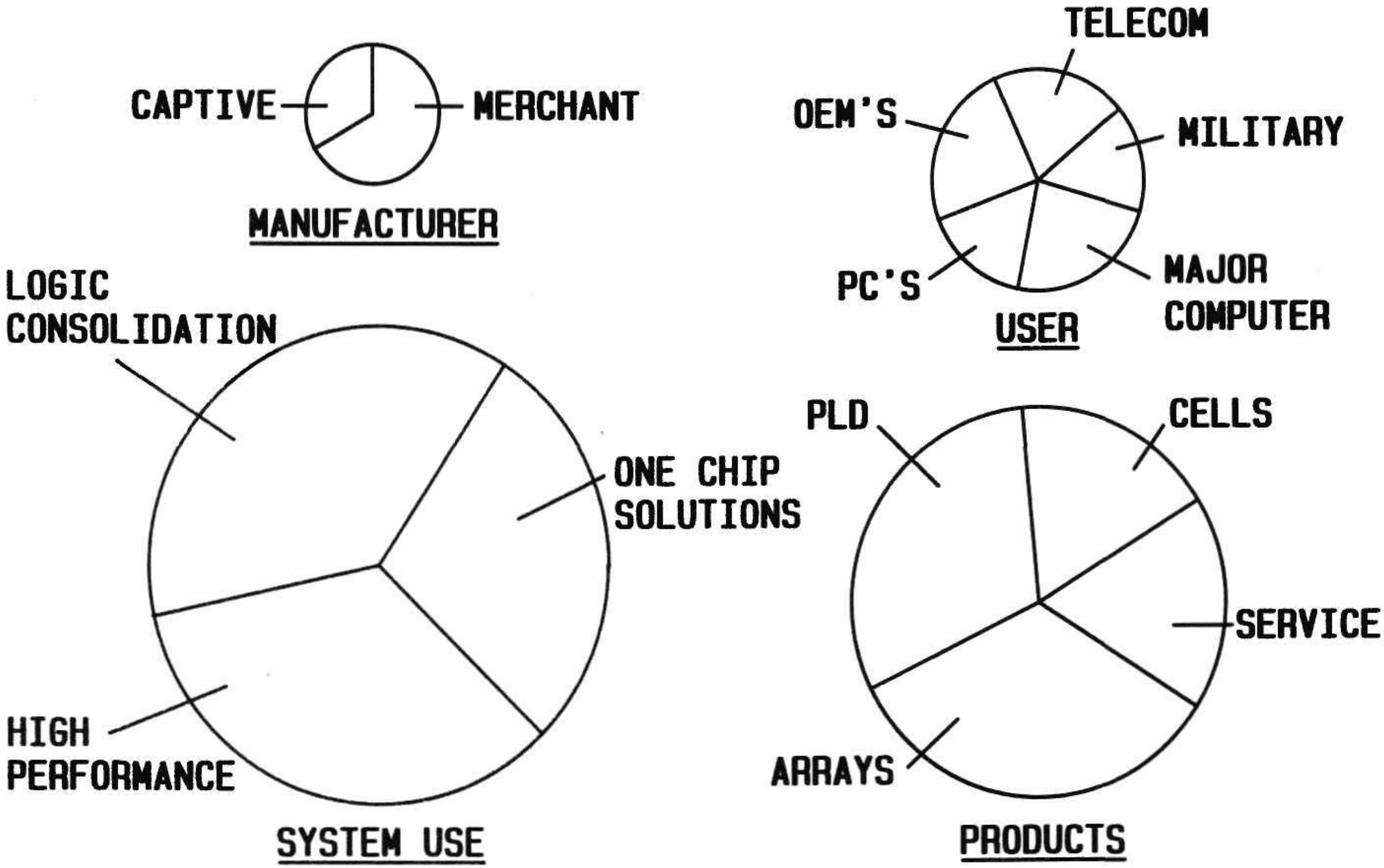
BENEFITS

- LOWER SYSTEM COST
  - HIGHER LEVELS OF INTEGRATION
  - REDUCED BOARD AREA
  - ENHANCED RELIABILITY
- REDUCED TIME-TO-MARKET
- HARDWARE DIFFERENTIATION

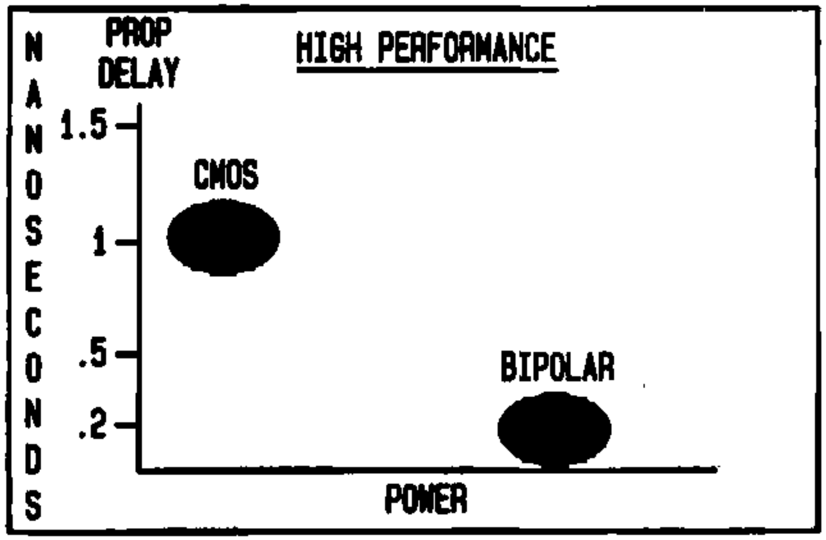
CIRCA 1986

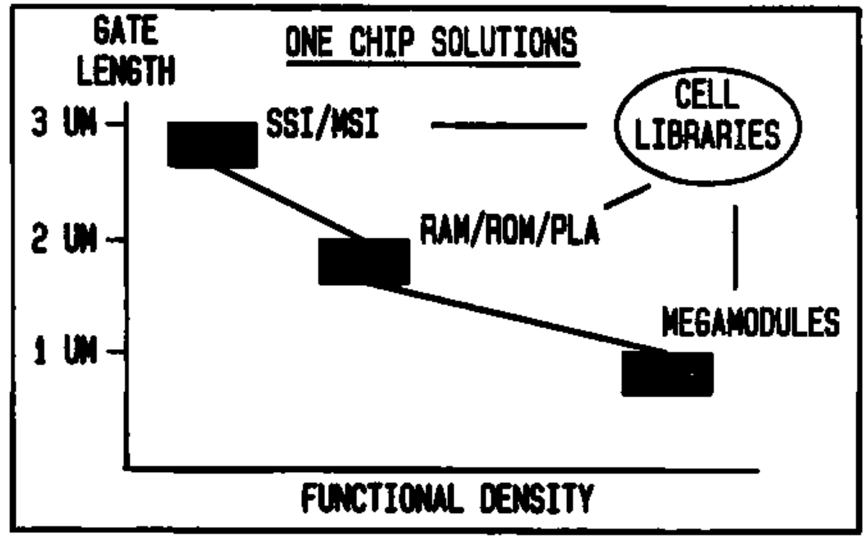
- ENTERING GROWTH SEGMENT OF PRODUCT LIFE CYCLE
- VENDOR BASE SELECTION UNDERWAY - MANUFACTURING KEY SELECTION CRITERIA
- MANY CUSTOMERS ESTABLISHING IN-HOUSE DESIGN CENTERS
- CMOS IS DOMINANT...MOVING RAPIDLY TO ONE MICRON

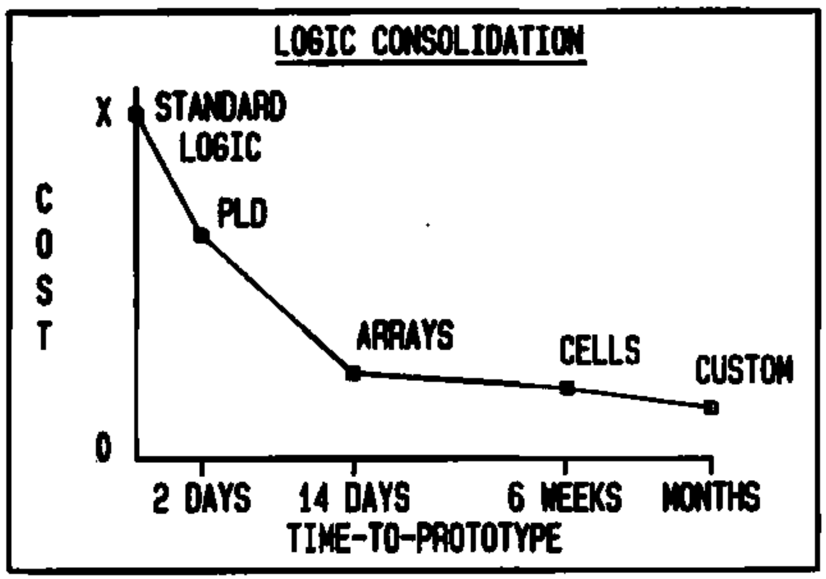
ASIC MARKET SEGMENTATION



ASIC PRODUCT PERFORMANCE

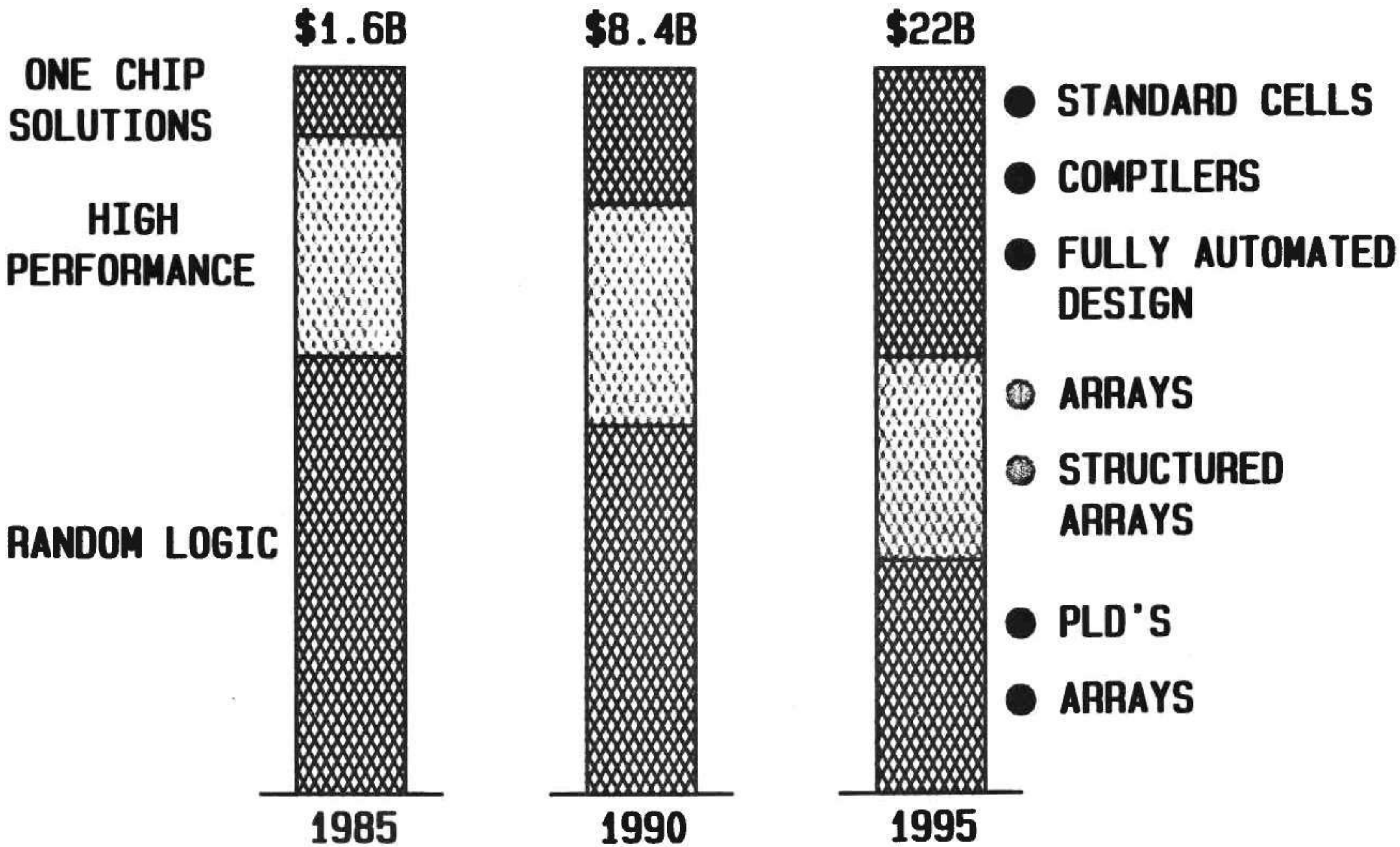






- PERFORMANCE REQUIREMENTS TAKE ON DIFFERENT DIMENSIONS ACCORDING TO MARKET SEGMENTS
- TECHNOLOGY AND SERVICE ARE KEYS TO MEETING PERFORMANCE NEEDS

SYSTEM USE SEGMENTATION



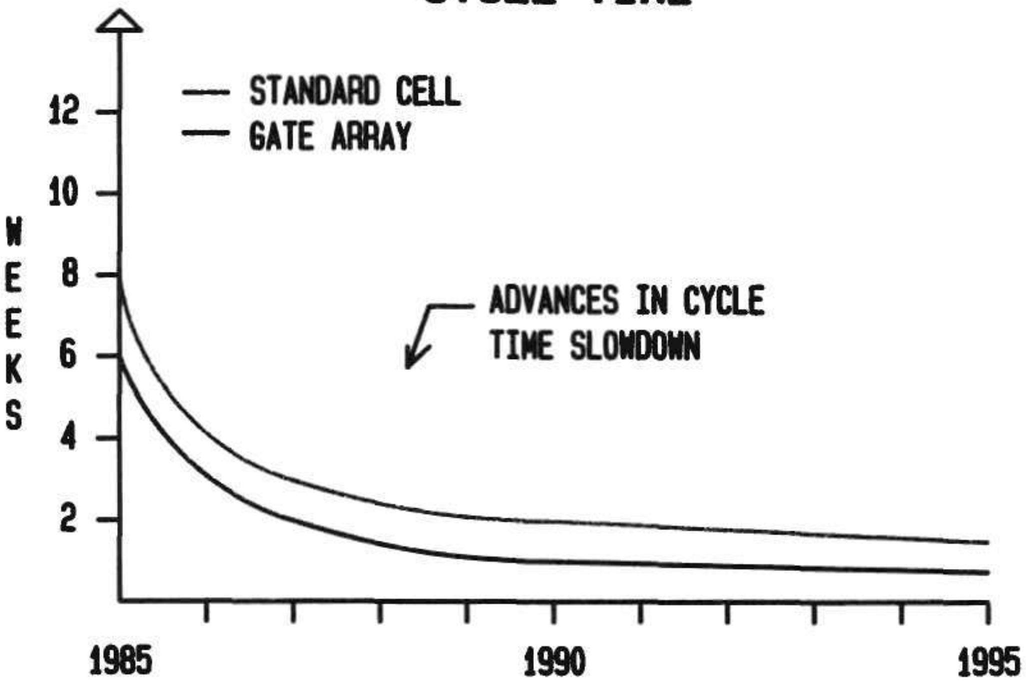
DATAQUEST WORLDWIDE MERCHANT TAM $B

USE OF ASIC PRODUCTS IN SYSTEMS

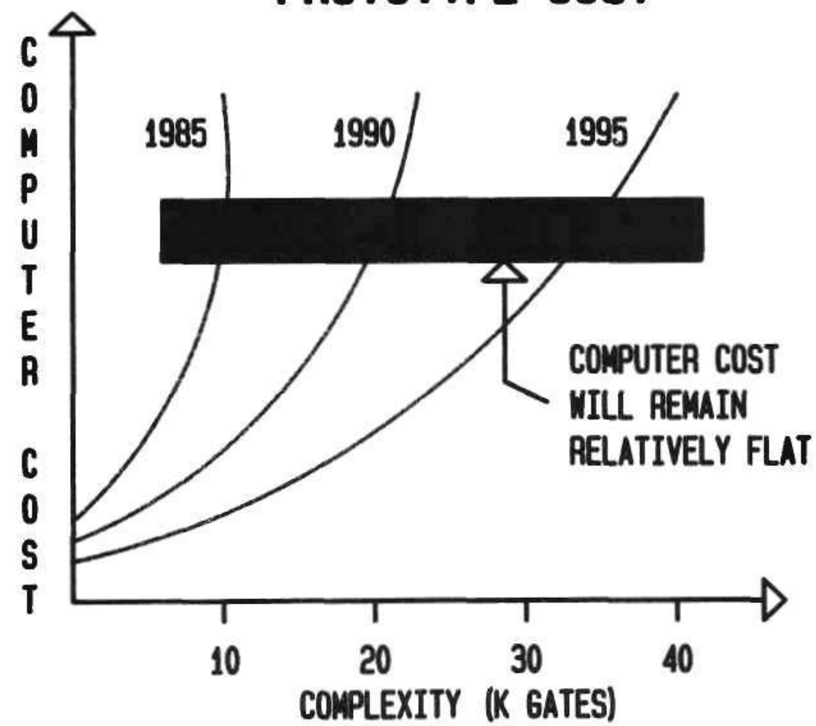
MARKET FOCUS	ELEMENTS	LEVERAGE POINTS
	SYSTEM DESIGN	PRODUCTIVITY
COST & CYCLE TIME	ASIC PROTOTYPE	
	SYSTEM EVALUATION FIX SYSTEM DESIGN	1ST PASS SUCCESS
PRICE	ASIC MANUFACTURING INCOMING TEST REPAIR COST	QUALITY AND RELIABILITY

ASIC PROTOTYPE CYCLE TIME AND COST

CYCLE TIME



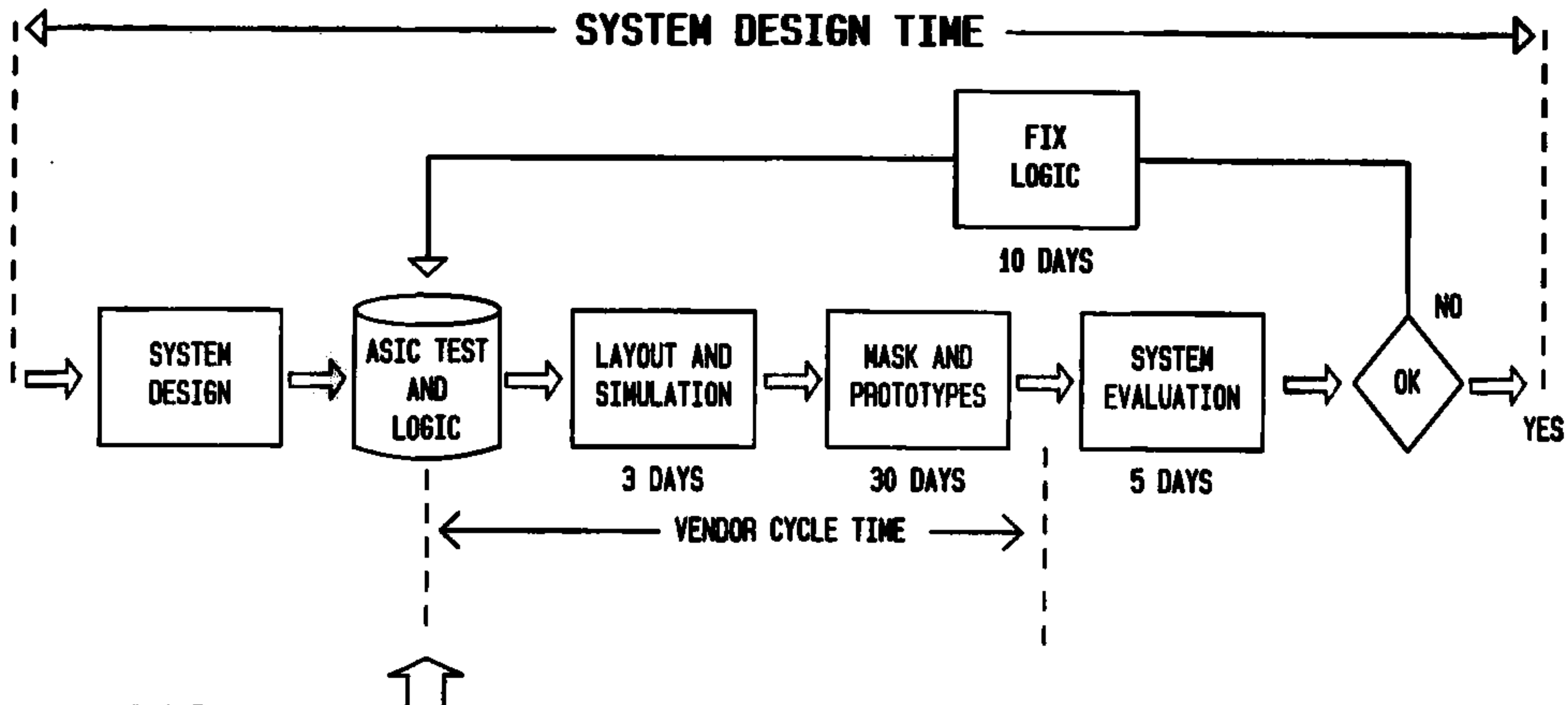
PROTOTYPE COST



- PHYSICAL DESIGN AND VERIFICATION BECOME COMPLETELY AUTOMATED
- PROTOTYPE MAKE-FUNCTION REACHES NEAR THEORETICAL PROCESSING TIME

- COMPUTER RESOURCES ARE DETERMINED BY NUMBER OF ITEMS TO BE CONSIDERED
- PROCESSING COST IMPROVEMENT WILL COME FROM ALGORITHM IMPROVEMENTS AND HARDWARE COST REDUCTIONS
- AVERAGE COMPLEXITY WILL CONTINUE TO GROW

FIRST PASS SUCCESS



AI SOFTWARE

__1986__

- IDENTIFIES AND FIXES PROCEDURAL PROBLEMS SUCH AS UNCONNECTED INPUTS
- IDENTIFIES POOR DESIGN PRACTICES

__1990__

- PARTITION SYSTEM DESIGN
- OPTIMIZE PERFORMANCE

IMPACT OF ERROR

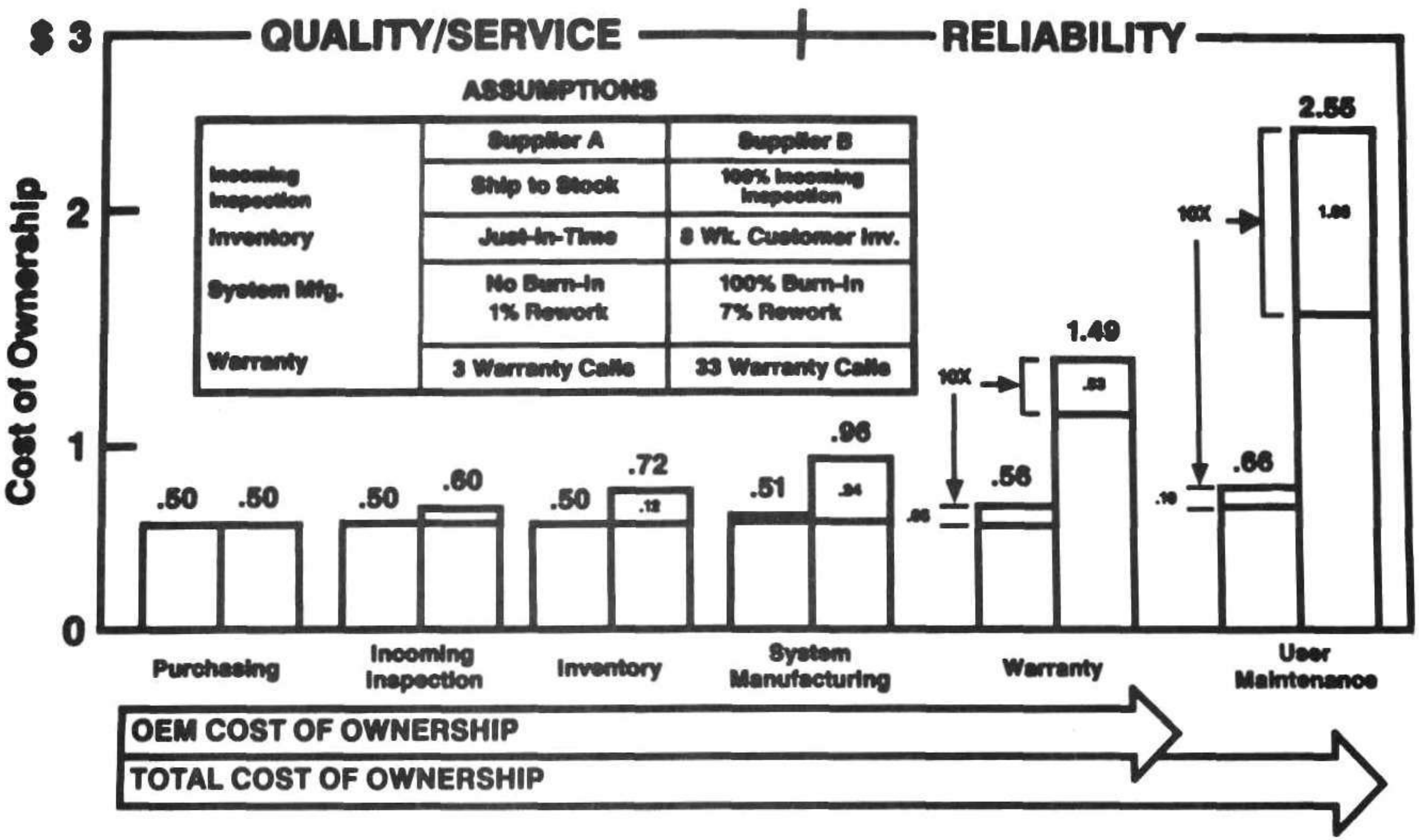
FOUND IN SYSTEM EVALUATION	48 DAYS
FOUND AT START OF VENDOR CYCLE	10 DAYS

COST OF OWNERSHIP EXAMPLE

ASSUMPTIONS

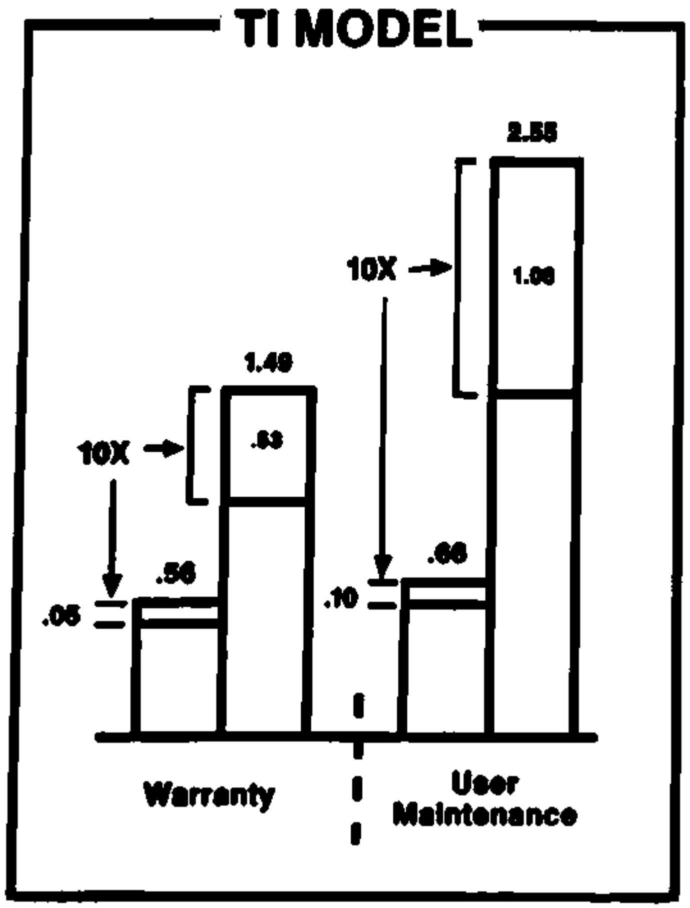
100 PARTS/BOARD-5 BOARDS/SYSTEM-100 SYSTEMS/MONTH		
Purchasing	Supplier A Price = 50¢	Supplier B Price = 50¢
Incoming Inspection	100 PPM Quality Ship to Stock	3,500 PPM 100% Incoming Inspection (10¢/Dev.)
Inventory	Just-In-Time Delivery No Safety Stock	No JIT 8 Wks. Customer Inventory
System Manufacturing	5 Fits Failure Rate No Component Burn-In 1% Board Rework No System Rework	100 FITS 100% Component Burn-In (20¢/Dev.) 7% Board Rework ($50/Board) 1% System Rework ($300/System)
Warranty (One Year)	3 Warranty Calls	33 Warranty Calls ($800/Call)
User Maintenance	2 Times Warranty Cost	2 Times Warranty Cost

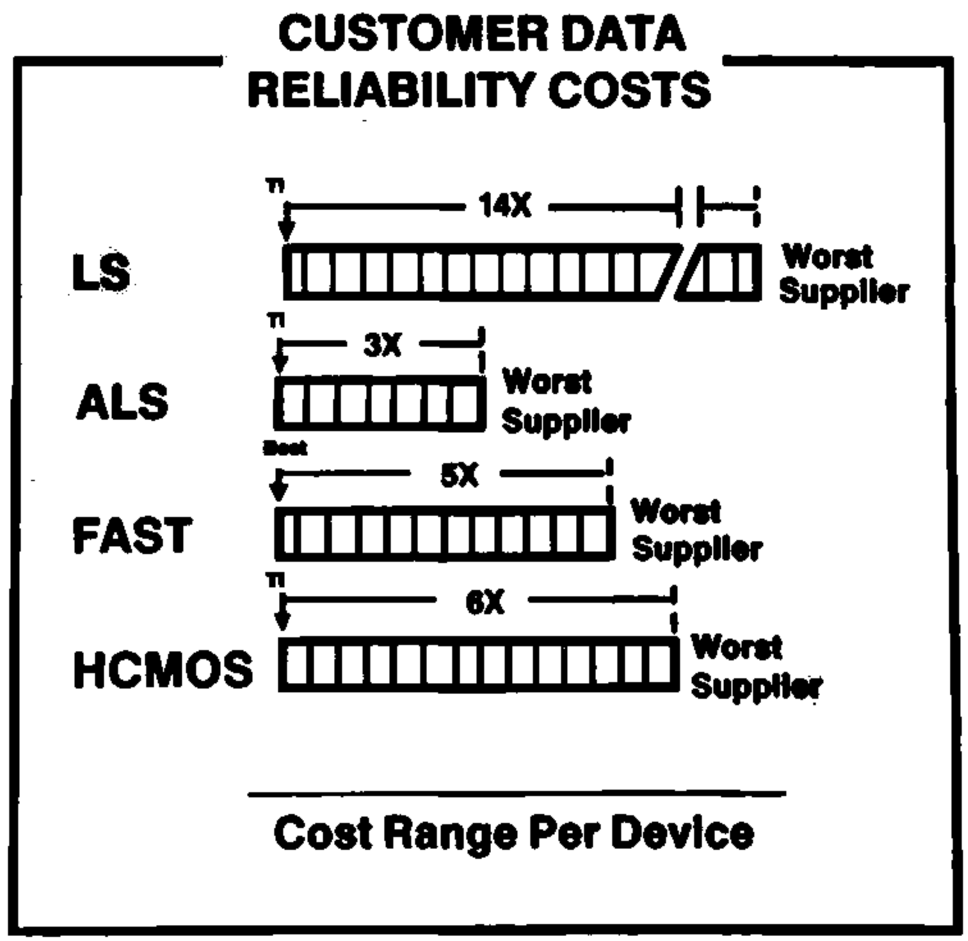
CUSTOMER BENEFIT FROM QUALITY, RELIABILITY AND SERVICE DIFFERENTIATION



	Supplier A	Supplier B
Incoming Inspection	Ship to Stock	100% Incoming Inspection
Inventory	Just-In-Time	8 Wk. Customer Inv.
System Mfg.	No Burn-In 1% Rework	100% Burn-In 7% Rework
Warranty	3 Warranty Calls	33 Warranty Calls

SUPPLIER RELIABILITY COMPARISON





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JAPANESE AND U.S. MANUFACTURING PHILOSOPHIES

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Mr. Bagley is a Senior Vice President of Applied Materials, Inc., and is responsible for operations. Prior to joining Applied Materials, Mr. Bagley spent 16 years at Texas Instruments, Inc., in various engineering and management positions related to the development and manufacture of semiconductor test, assembly, and wafer processing equipment. He received B.S. and M.S. degrees in Electrical Engineering from Mississippi State University.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
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JAPANESE AND U.S. MANUFACTURING

WHAT ARE THE REAL DIFFERENCES?

LAST YEAR, FOR THE FIRST TIME IN THE HISTORY OF THE SEMICONDUCTOR INDUSTRY, THE LARGEST SEMI-CONDUCTOR COMPANY WAS NOT U.S. - IT WAS JAPANESE. (NEC). IN THE UPDATE SECTION, AUGUST 15, 1986 ISSUE OF ELECTRONIC BUSINESS MAGAZINE, I NOTED THAT ICE PREDICTS THAT NEC, HITACHI, AND TOSHIBA, IN THAT ORDER WILL BE THE TOP THREE CHIP MAKERS IN THE WORLD - RELEGATING TI AND MOTOROLA TO NUMBERS 4 AND 5. IN ADDITION, THE ARTICLE STATES THAT THE JAPANESE WILL OUTPRODUCE AND OUTSPEND U.S. PRODUCERS IN TOTAL.

MUCH HAS BEEN WRITTEN DETAILING HOW JAPANESE ACHIEVE SUPERIORITY IN TARGETED INDUSTRIES. MANUFACTURING EXCELLENCE IS HIGH ON THE LIST OF WEAPONS THEY HAVE SUCCESSFULLY EMPLOYED.

FIGURE 1

GENERALLY, JAPANESE PLANTS

1. HAVE HIGHER PRODUCTIVITY
2. HAVE BETTER QUALITY
3. ARE MORE CAPITAL EFFECTIVE - THAT IS THEY UTILIZE CAPITAL EQUIPMENT BETTER AND THEY SPEND LESS CAPITAL PER UNIT OF OUTPUT. FOR EXAMPLE, ONE STUDY SHOWED THAT TOYOTA SPENDS 50% OF THE CAPITAL TO ACHIEVE THE SAME PRODUCTION OUTPUT AS GENERAL MOTORS.
4. NEW PRODUCTS CAN BE INTRODUCED INTO JAPANESE PLANTS AND RAMPED TO HIGHER VOLUMES FASTER, AND IN SEMICONDUCTOR MANUFACTURING THEY ACHIEVE HIGHER YIELDS FASTER.
5. FLEXIBILITY, THAT IS, THE ABILITY TO ACCOMMODATE A WIDE VARIETY OF PRODUCTS SIMULTANEOUSLY OR THE ABILITY TO ACCOMMODATE SIGNIFICANT CHANGES IN PRODUCTION SCHEDULES RAPIDLY, IS LESS THAN U.S. FACTORIES.
6. JAPANESE PLANTS ARE MORE MECHANIZED BUT LESS AUTOMATED.

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7. MECHANIZATION REFERS TO MECHANICALLY ASSISTED, SUCH AS, PICK AND PLACE MATERIAL HANDLING. AUTOMATION IS BROADER AND REFERS TO PROGRAMABILITY OR AUTOMATIC ADAPTABILITY.

FIGURE 2

STEVE WHEELWRIGHT, PROFESSOR OF MANAGEMENT, AT THE STANFORD GRADUATE BUSINESS SCHOOL, HAS VISITED A VARIETY OF U.S. AND JAPANESE MANUFACTURING FACILITIES. SOME OF HIS OBSERVATIONS:

1. JAPANESE AUTO PLANTS ARE ONLY MODESTLY BETTER AUTOMATED THAN U.S. FACTORIES. BOTH FORD AND GENERAL MOTORS HAVE HIGHLY AUTOMATED PLANTS.

2. MAJOR APPLIANCE PLANTS IN JAPAN ARE SOMEWHAT MORE AUTOMATED THAN U.S. PLANTS.

3. THE AVERAGE AGE OF EQUIPMENT IN THE JAPANESE PLANTS IS LESS THAN THE U.S.

4. THE JAPANESE EQUIPMENT LOOKS NEWER BECAUSE IT IS TYPICALLY BETTER MAINTAINED AND OPERATED MORE CONSERVATIVELY THAN IN THE U.S.

5. THE JAPANESE HAVE MORE DEMONSTRATION PLANTS IN WHICH THEY HAVE PUT EVERYTHING TOGETHER AND HAVE BUILT TRULY "LIGHTS OUT" FACTORIES.

FIGURE

ADVANTAGES COMMONLY CITED FOR JAPANESE SUPERIOR PERFORMANCE ARE:

1. THEY HAVE A BETTER EDUCATED WORK FORCE BECAUSE THEY HAVE A HIGHER LITERACY RATE IN JAPAN AND A MORE CHALLENGING ACADEMIC SYSTEM THROUGH THE TEENAGE YEARS.

2. THEY HAVE LESS TURN OVER. THEIR WORKERS ARE MORE LOYAL TO THE COMPANY BECAUSE LIFE TIME EMPLOYMENT PRACTICES AND SOCIETAL PRESSURES DISCOURAGE JOB CHANGES.

3. DESIRABLE EMPLOYEE TRAITS ARE MORE WIDE SPREAD WITHIN SOCIETY AND ARE PASSED ON FROM GENERATION TO GENERATION BECAUSE THE SOCIETY IS HOMOGENEOUS WITH THE SAME HERITAGE, LANGUAGE, RELIGION, ETC. SOME OF THE TRAITS ARE:

4. AN AFFINITY FOR TEAM WORK AND SUBORDINATED INDIVIDUAL GOALS,

5. A SURVIVAL WORK ETHIC, AND

6. AN ORIENTATION FOR DETAIL.

7. LOW COST CAPITAL AND FREEDOM FROM QUARTERLY PROFIT PRESSURE PERMITS MANAGERS TO ADHERE TO A LONG RANGE PLAN IN SPITE OF NEAR TERM FINANCIAL PERTURBATIONS.

8. THE WAGE SCALE IN JAPAN IS LOWER THAN THE U.S. ESPECIALLY FOR ENGINEERING TALENT, AND

9. THE YEN HAS BEEN SIGNIFICANTLY UNDERVALUED.

FIGURE 4

I DON'T BELIEVE THESE ADVANTAGES ARE INHERENT TO JAPAN OR JAPANESE. FIRST THE PERFORMANCE ADVANTAGES OF THE JAPANESE PLANTS ARE NOT CONFINED TO PLANTS LOCATED IN JAPAN.

THE SUCCESSES OF U.S. PLANTS OWNED BY SONY, MATSUSHITA, NUMMI, HONDA AND OTHERS HAVE BEEN WELL DOCUMENTED.

SECOND: MOST OF THESE ADVANTAGES ARE CHANGING WITH TIME OR ARE NOT INHERENT WITH JAPANESE.

- THE U.S. CAN CERTAINLY CLOSE THE LITERACY GAP.

- THE JAPANESE TURNOVER RATE IS INCREASING AND WILL CONTINUE TO INCREASE BUT MAY NEVER REACH CURRENT U.S. LEVELS.

YOUNGER JAPANESE EXHIBIT LESS WILLINGNESS TO WORK AS HARD AS PAST GENERATIONS.

THE ADHERENCE TO A STRATEGY AND LONG RANGE INVESTMENT PLAN IS NO LONGER DISCUSSED WIDELY WITH CREDIBILITY.

THE WAGE SCALE DIFFERENCE IS A TEMPORARY ADVANTAGE THAT IS DECREASING WITH TIME.

THE CURRENT VALUE OF THE YEN HAS TO BE A SIGNIFICANT COST DISADVANTAGE TO THE JAPANESE. JUST ONE YEAR AGO, A YEN VALUED AT 180 TO 200 TO THE DOLLAR WAS THOUGHT NECESSARY TO REACH COST PARITY. MANY PEOPLE BELIEVED THIS DEGREE OF YEN APPRECIATION WAS UNACHIEVABLE. TODAY, THE YEN IS LESS THAN 160 TO THE DOLLAR.

FIGURE 5

THERE ARE SEVERAL DISADVANTAGES THAT JAPANESE COMPANIES MUST OVERCOME THAT ARE SELDOM DISCUSSED.

IT IS MORE DIFFICULT TO MOVE GOODS IN JAPAN. ONE OF THE REASONS THAT JAPANESE SUPPLIERS LOCATE NEAR THEIR MAJOR CUSTOMERS IS THE DIFFICULTY IN MOVING PEOPLE AND GOODS.

THE COST OF TRANSPORTATION, CONSTRUCTION, AND LAND ARE SIGNIFICANTLY HIGHER IN JAPAN THAN IN MOST U.S. LOCATIONS.

THERE ARE FEW CHOICES FOR MANUFACTURING SITES IN JAPAN THAT DO NOT REQUIRE TRANSPORTATION OR PEOPLE RELOCATION HARDSHIPS. QUALITY FACILITIES THAT CAN BE LEASED ARE NOT READILY AVAILABLE.

RELOCATING PEOPLE IS DIFFICULT DUE TO THEIR STRONG TIES TO THEIR FAMILY AND COMMUNITY - AND ALSO THEIR DESIRE TO LIVE IN THE IMMEDIATE TOKYO AREA RESTRICTS YOUR PLANT SITE CHOICES.

LIFE TIME EMPLOYMENT, SENIORITY PAY AND PROMOTION POLICIES, CONSENSUS MANAGEMENT ARE ALL CITED AS JAPANESE ADVANTAGES. IN MY EXPERIENCE, THEY ARE AT BEST NEUTRAL AND PROBABLY A DISADVANTAGE.

FIGURE 6

THE PRINCIPAL REASON FOR JAPANESE MANUFACTURING SUPERIORITY IS ATTITUDINAL NOT ETHNIC, CULTURAL, ENVIRONMENTAL, OR INSTITUTIONAL.

IN JAPAN, SUPERIOR MANUFACTURING CAPABILITY IS VIEWED AS A STRATEGIC WEAPON THAT PROVIDES COST ADVANTAGES THAT CAN LEAD TO MARKET SHARE GAINS THROUGH PRICING.

MANUFACTURING IS A HONORED PROFESSION IN JAPAN AND MOST JAPANESE EXECUTIVES' CAREER PATH HAS BEEN THROUGH THE MANUFACTURING ORGANIZATION.

THE DIFFERENCES IN RESULTS

JAPANESE PLANTS:

1) Have higher productivity
2) Have better quality
3) Are more capital effective
4) Accommodate new product introduction better
5) Are less flexible
6) Are more mechanized
7) Are less automated

FIG. 1

SOME PHYSICAL DIFFERENCES IN U.S. AND JAPANESE FACTORIES

- Japanese plants are only modestly better automated
- The average age of equipment in the Japanese plant is less
- The Japanese have more demonstration "lights-out" factories

FIG. 2

ADVANTAGES CITED FOR JAPANESE PERFORMANCE

- Better educated workforce
- Less turnover
- Desirable employee traits widespread
- Teamwork and subordinated individual goals
- Survival work ethic
- More detail oriented
- Dogged adherence to a long range plan
- Lower wage base - specifically engineers
- Undervalued yen

FIG. 3

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THESE ADVANTAGES ARE NOT FUNDAMENTAL

First: The performance advantages of Japanese plants are not confined to plants located in Japan

Second: Most of these advantages are changing with time or are not inherent with Japanese

FIG. 4

JAPANESE DISADVANTAGES SELDOM DISCUSSED

- Poorer internal transportation system and higher basic cost
- Higher construction cost
- More restrictive building codes
- Higher cost of land
- Fewer choices for manufacturing sites
- Fewer financial options for basic facilities
- Difficulty relocating people
- Difficulty attracting people from the Tokyo area
- Restrictive personnel policies

FIG. 5

JAPANESE ATTITUDE

- Superior manufacturing capability is a strategic weapon
- Manufacturing is on the Japanese executive career path
- The rewards and status for manufacturing managers are equivalent to other functional managers
- The brightest people spend extensive time in manufacturing jobs

FIG. 6

THE REWARDS FOR MANAGING IN MANUACTURING IN JAPAN ARE EQUAL TO JOBS IN OTHER COMPANY FUNCTIONS.

IN JAPAN, THE BRIGHTEST PEOPLE SPEND SIGNIFICANT TIME IN MANUFACTURING JOBS LEARNING MANUFACTURING TECHNOLOGY AND CONTRIBUTING TO ITS DEVELOPMENT AND APPLICATION WITHIN THEIR COMPANIES.

FIGURE 7

THE EXCELLENT JAPANESE ORGANIZATIONS DESIGN FOR MANUFACTURABILITY.

THE JAPANESE APPEAR TO CHARACTERIZE THEIR EQUIPMENT AND PROCESSES TO A GREATER EXTENT AND OPTIMIZE THE PROCESS WINDOW FOR THE CAPABILITY OF THE EQUIPMENT. THE RESULT OF THIS EFFORT IS GREATER EQUIPMENT UTILIZATION.

APPLIED MATERIALS DID AN EXTENSIVE SURVEY OF U.S., EUROPEAN, AND JAPANESE SEMICONDUCTOR MANUFACTURERS ON THEIR UTILIZATION OF CVD EQUIPMENT - PLASMA ENHANCED AND LOW PRESSURE.

THE RESULTS OF THE SURVEY SHOW THAT THEIR GREATER UTILIZATION OF PLASMA ENHANCED CVD EQUIPMENT WAS ALL THE RESULT OF LESS ENGINEERING REQUALIFICATION TIME. THEIR EQUIPMENT WAS RETURNED TO SERVICE FASTER AFTER ROUTINE MAINTENANCE, UNSCHEDULED MAINTENANCE, OR SCHEDULED SHUTDOWNS, APPARENTLY, BECAUSE THEIR SPEC WAS EASIER TO ACHIEVE THAN THEIR U.S. COMPETITORS. THE RESULTS WERE THE SAME REGARDLESS OF THE SOURCE OF THE EQUIPMENT - JAPANESE OR U.S.

FIGURE 8

FOR LOW PRESSURE CVD EQUIPMENT, THE RESULTS WERE SIMILAR WITH THE JAPANESE GETTING AN ADDITIONAL 5 PERCENTAGE POINTS MORE UTILIZATION DUE TO LESS UNSCHEDULED MAINTENANCE. BUT ONCE AGAIN, THE BIG DIFFERENCE WAS ENGINEERING REQUALIFICATION TIME.

FIGURE 9

A SURVEY OF OVER 200 COMPANIES IN THE U.S. AND JAPAN GIVES A VIEW OF DIFFERING STAFFING APPROACHES. THE HEIGHT OF THE BARS INDICATES THE NUMBER OF INDIRECTS BY FUNCTION PER DIRECT WORKER. THE U.S. HAD MORE MANAGERS, ACCOUNTANTS, AND MATERIALS PEOPLE. THE JAPANESE HAD MORE FLOOR SUPERVISORS, HUMAN RESOURCE PEOPLE, AND MANUFACTURING ENGINEERS.

FIGURE 10

A STUDY BY ANDREW WEISS FROM COLUMBIA UNIVERSITY OF FIVE JAPANESE COMPANIES SHOWED THAT ENGINEERING SUPPORT PER DIRECT WORKER WAS MUCH HIGHER IN THESE COMPANIES THAN U.S. COMPANIES. THE ENGINEERING SUPPORT RANGED FROM 4 TO 1 FOR HIGH VOLUME LOW TECHNOLOGY PRODUCTS, SUCH AS RADIOS, TO 1 TO 1 FOR HIGH TECHNOLOGY PRODUCTS, SUCH AS VLSI DEVICES OR SATELLITE COMMUNICATION SYSTEMS.

FIGURE 11

THE CORPORATION MUST DEVELOP THE VIEW THAT MANUFACTURING EXCELLENCE IS A KEY SUCCESS FACTOR AND THEN TAKE ACTIONS THAT SUPPORT MANUFACTURING IMPROVEMENTS.

TOP MANAGEMENT MUST GAIN AN UNDERSTANDING OF THE MANUFACTURING OPERATION AND BECOME INVOLVED IN MANUFACTURING POLICIES AND PHILOSOPHY.

THE ORGANIZATION STRUCTURE, REPORTING LEVELS AND THE REWARD SYSTEM OF A CORPORATION MUST GIVE THE CLEAR MESSAGE THAT A CAREER IN MANUFACTURING IS VALUED AND THAT TOP EXECUTIVES MUST BE WELL SCHOOLED BY EXPERIENCE IN MANUFACTURING ACTIVITIES.

MANUFACTURING MANAGERS SHOULD PARTICIPATE EQUALLY WITH OTHER FUNCTIONAL MANAGERS IN THE DEVELOPMENT OF LONG RANGE PLANS. THEY SHOULD ALSO BE THE MAJOR CONTRIBUTORS IN STRATEGIC MANUFACTURING DECISIONS.

HIRING, TRAINING AND CAREER PATHS FOR MANUFACTURING SHOULD HAVE EQUAL PRIORITY WITH OTHER DISCIPLINES WITHIN A COMPANY.

FIGURE 12

THE MANUFACTURING JOBS SHOULD BE BROADLY DEFINED. THROUGHOUT ALL MANUFACTURING LEVELS IN THE TYPICAL JAPANESE COMPANY, THE JOBS WERE MORE BROADLY DEFINED AND GENERALLY HAD A SCOPE OF RESPONSIBILITY ONE TO TWO LEVELS HIGHER THAN THE CORRESPONDING U.S. TITLE.

IN AND OF THEMSELVES, ORGANIZATIONS, PAY, JOB DESCRIPTIONS ARE NOT GOING TO MAKE THE DIFFERENCE.

GOOD MANAGERS WHO HAVE SPECIFIC MANUFACTURING SKILLS AND WHO HAVE A CHARTER AND MANAGEMENT BACKING TO ACHIEVE EXCELLENCE WILL MAKE THE DIFFERENCE.

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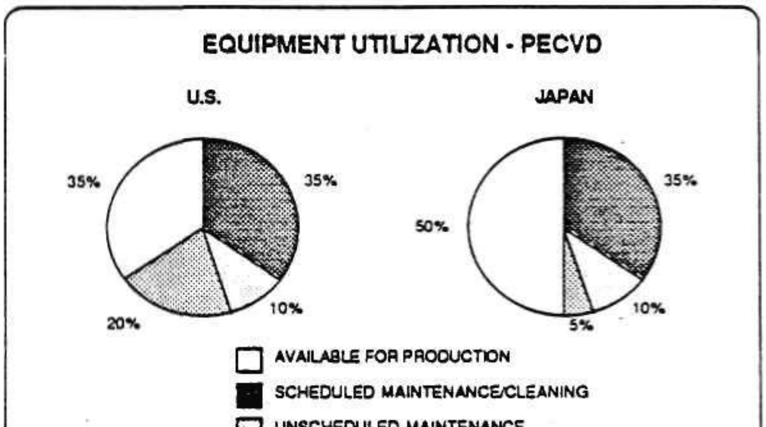

FIG. 7

JWB 10/21/86

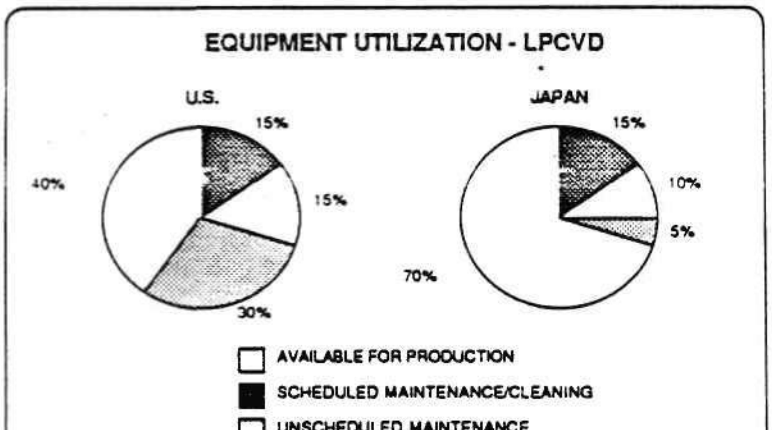

FIG. 8

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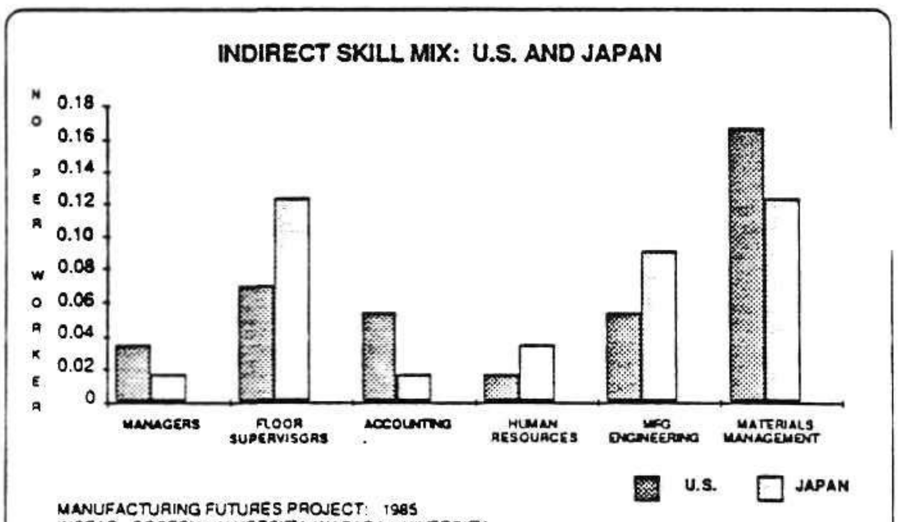

FIG. 9

JWB 10/21/86

RATIO OF PRODUCTION WORKERS TO ENGINEERS

U.S. Company			Greater Than 8 TO 1
Japanese Company	A	Parent	1 TO 1
		Local Subsidiary	8 TO 1
	C	Computer Equipment Div.	1 TO 1
		Industrial Equipment Div.	3 TO 1
	D	Radio Division	4 TO 1
		Computer Equipment Div.	1 TO 1
	E	Plant 1	4 TO 1
		Plant 2	Less than 1 TO 1

"Simple Truths of Japanese Manufacturing"
Andrew Weiss
HARVARD BUSINESS REVIEW July-August, 1984

FIG. 10

MANUFACTURING CITIZENSHIP

Top Management
- Understanding of manufacturing operations
- Involvement in manufacturing policies

Organization structure, reporting levels and reward system that enhances manufacturing

Manufacturing Management
- Input to long range plans
- Involvement in strategic manufacturing decisions

Hiring, training and career paths for manufacturing

FIG. 11

JAPANESE COMPANIES OFFER GREATER JOB RESPONSIBILITY AND BREADTH AT EVERY ORGANIZATIONAL LEVEL

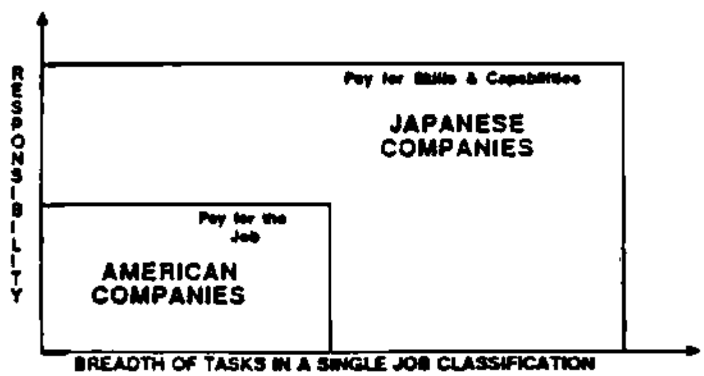

FIG. 12

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INDUSTRY CHALLENGES WITHIN THE NEW TRADE AGREEMENT

Andrew A. Procassini
President
Semiconductor Industry
Association

Mr. Procassini is President of the Semiconductor Industry Association (SIA), the trade organization that represents U.S.-based semiconductor manufacturers. Prior to his appointment as SIA president, Mr. Procassini served semiconductor firms in senior management positions for quality and reliability assurance, operations, sales and marketing, and in the international arena, including residence in Japan and Europe. He has held major posts at Hyundai, Motorola, and Fairchild Semiconductor. He also cofounded and served as President of Micro Circuit Electronics. Mr. Procassini received a bachelor's degree from the University of Michigan and a master's degree in Economics from Arizona State University.

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October 20-22, 1986
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INDUSTRY CHALLENGES WITHIN THE TRADE AGREEMENT

ANDY PROCASSINI
President, Semiconductor Industry Association

SPEECH FOR DATAQUEST
OCTOBER 19-20, 1986

Good afternoon, ladies and gentlemen. The invitation by Dataquest to speak on my subject at this conference is very much appreciated.

There has been a good deal of information, and a great deal of mis-information regarding the U.S.-Japan Semiconductor Trade Agreement. In many cases, it appears that its critics have not even read it.

In the next 20 minutes I would like to discuss the historical circumstances which led up to the filing by the SIA, the terms of the agreement, and the challenges that these terms present to the U.S. semiconductor industry. I will then be happy to answer your questions.

The SIA was founded in March 1977, almost 10 years ago. Its purposes were to, first, address the issues of international trade, especially with respect to Japan, and, secondly, to communicate within and outside the industry on matters of general interest, such as trade statistics, environmental issues, export control, intellectual property, joint research and many other issues.

Many of the issues addressed have been satisfied. The Semiconductor Research Corp. was formed and is operating, the chip protection act was passed, and the World Semiconductor Trade Statistics entity for trade statistics was established. The U.S.-Japan trade agreement was signed on September 2, only about 6 weeks ago.

This historic agreement completed the comprehensive settlement of the Section 301 trade action filed by the Semiconductor Industry Association in July 1985.

Its resolution involved the EPROM and 256K and above DRAM antidumping suits filed by private firms and the Department of Commerce. This agreement is probably the broadest bilateral trade agreement ever signed in this age of global industries. It addresses the issues of market access, dumping and rapid enforcement.

To understand the significance of this agreement to the semiconductor industry; to the broader electronics industries; to the national economy, and to national security, it is necessary to briefly review the history of U.S.-Japan semiconductor trade.

During the 1960's and early 1970's, American firms were not permitted to locate facilities in Japan and were often prohibited from importing products into Japan by the Ministry of International Trade and Industry, also known as MITI. U.S. market share in Japan was about 10% throughout this period, mostly representing parts which Japanese firms did not produce. In fact, in my opinion, state-of-the-art devices produced by American firms were often purchased in order for the Japanese firms to develop their own devices. As purchasers, they were often provided not only with devices, but also device and process information.

In the mid-1970s, MITI removed most of these formal barriers. But at the same time that MITI "liberalized" semiconductor trade by removing formal barriers, it encouraged a market restructuring with the intent to aid reciprocal buying among Japanese electronics firms, and exclude American imports. These measures were described in Japan at the time as "liberalization counter-measures", and were done in an informal and almost secretive manner.

Through the balance of the 1970's and early 1980's, American efforts to penetrate the Japanese market were thwarted by the market structure put in place by MITI's counter liberalization scheme, and the U.S. share in Japan remained at a 10% level. In all other world markets, where semiconductors are purchased on the competitive merits of the products, U.S. producers earned over 50% share of market.

In late 1983, the U.S. and Japanese governments reached an accord on semiconductors in which MITI agreed to encourage the purchase of U.S.-made semiconductors. While there was an initial increase of U.S. share during early 1984, a period of extreme semiconductor shortages, these bright signs faded when the market slowed. U.S. share dropped to below 9% of the Japanese market.

Frustration with MITI's failure to reverse its "counter-liberalization" creation and the lack of an alternative method to access Japan were major reasons for SIA's filing of it's 301 case. In fact, a recent quote by a Japanese executive , no different than 10 years ago during my years in Tokyo, represents the prevailing Japanese customer view, "We buy first within our group, then within Japan, and only as a last resort from foreigners". In other words, if you are a foreign supplier and offered the best delivery, the best price, and the best performance every time, you'd still only get the order sometimes.

Another reason for the SIA 301 case was to stop the Japanese companies from dumping semiconductors in all world markets. Dumping is the persistent and injurious pricing of products below fair market-value by foreign firms. Fair market value is the cost of production, including R&D, and a reasonable profit. Dumping is an unfair trade practice under U.S. law and under the General Agreement on Tariffs and Trade, i. e., GATT. The persistent dumping that is the result of Japanese industrial policy is an effort to force a structural change and not merely a cyclical adjustment to correct for the impacts of the business cycle.

During this recent recession, the U.S. industry was severely injured by Japanese dumping, especially in memory product lines. Japanese dumping caused 256K EPROM prices to drop from $23 in Q1 1985 to $5 a year later. The Department of Commerce investigations in Japan showed that Japanese firms were pricing products at less than half of their cost of manufacture. The result was millions in financial losses for chip producers, and the withdrawal from memory product lines of several U.S. firms.

Chip customers received low prices, in the short term. But here, as elsewhere, there is no free lunch. Intense competition has resulted in a world semiconductor industry characterized by steep but predictable cost declines each year -- a phenomenon that has led to 30% per year price declines for chip customers. The predatory pricing practices by Japanese producers which far exceeded experience curve declines could lead to only one conclusion in the long term -- the elimination of a U.S. supply base and a Japanese oligopoly, with the ability to control prices unchecked and to limit supply of scarce state-of-the-art devices. It does not require a stretch of the imagination to envisage the same impact on segments of the electronics industry other than semiconductors. In fact, the use of dumping and deep pockets as a means to force structural change was aptly defended by a Japanese executive who stated that from a Japanese perspective, when penetrating the market, they cannot afford the "luxury of profits". As Americans, we cannot afford the pain of not making profits.

With this background in mind, let me now take a few minutes to explain the agreement.

The recent agreement has, of course, two elements -- market access and prevention of dumping. I will cover each aspect in turn.

Under the accord, MITI has agreed to encourage Japanese customers to purchase foreign-based semiconductors. Our objective is for U.S. firms to have a position in Japan commensurate with the demonstrated competitiveness of U.S. firms in world markets. The industry's expectation is that, under this agreement, U.S. share in Japan will increase to above 20% by 1991. Access should be broad and wide. It should include the automotive and consumer electronics sectors as well as computer and telecommunications end uses. It should include, as users, small companies as well as the large conglomerates.

The dumping agreements are more complex, since they involve an interplay of the dumping laws and section 301, the Commerce Department and the U.S. Trade Representative's office, and suspension agreements on existing anti-dumping cases and the suspension of SIA's 301 case. Basically, EPROMs and 256K and above DRAMs are covered in the 301 settlement under agreements suspending anti-dumping cases for those products. The Commerce Department has estimated fair market value for each Japanese producer of DRAMs and EPROMs, and those producers have agreed that they will not sell below those values in the

United States. With regard to EPROM and 256K and above DRAM markets outside the United States, and with regard to other products sold outside Japan, MITI has agreed under the 301 accord to monitor prices and costs of Japanese producers and to act to ensure that dumping does not occur. Regarding the Japanese market, MITI has provided assurances that they will not permit activities that undermine the agreement.

I believe the U.S. is well served by the recent semiconductor accord, and not only U.S. semiconductor producers, but U.S. semiconductor customers and U.S. semiconductor equipment manufacturers. I would like to spend a few minutes elaborating on this point.

First, and most importantly, the Japanese electronics industry strategy of predatory dumping did not start with the semiconductor industry, nor will it end with the semiconductor industry. Japanese dumping in televisions has led to the elimination of virtually all American TV production. Dumping in transformers, pagers, cellular telephones--all have occurred. Dumping in semiconductors, the key building block in many end products, is only a prelude to Japanese control in computers, telecommunications, and robotics. The losses sustained by the deep pockets in Japan are not charity contributions to U.S. semiconductor customers. Those Japanese deep pockets would later be refilled by the eventual acquisition of the markets held by the U.S. semiconductor customers through the same types of predatory practices.

The second reason I support this accord is that it is consistent with the free trade principles of the SIA. This agreement is not protectionist: it has no quotas, voluntary or otherwise, and no tariffs to effectively shut out efficient foreign producers. The SIA rejected approaches, such as a uniform price floor set to average Japanese producer costs. This would have prevented U.S. customers from taking advantage of the cost declines from the most efficient Japanese producers; however, under this agreement, if Japanese producers manufacture chips at lower costs than U.S. producers, they can sell them at lower prices than U.S. producers. This agreement focuses on foreign market access and prevention of unfair predatory dumping by foreign producers, not the protection of any non-competitive domestic firms. The basic thought is that the experience curve is still applicable and semiconductor prices will follow the curve. It is only when economic rationale is abandoned, and pricing falls drastically below the curve and persistently remains there, is U.S. law violated.

The third reason I support this agreement is that it is far better than letting the current dumping law take its course, absent an agreement. Had the comprehensive settlement not been signed, the dumping duties on EPROMs and 256K and above DRAMs -- like those on 64K DRAMs -- would have become final; the price increases we have witnessed would have occurred anyway; might have been much higher and the dumper could trade off share of market for dumping duties. In addition, had dumping in third country markets not been addressed, as it was in the trade agreement, the U.S. customer base would certainly have had to purchase chips offshore, long term, to avoid being at a disadvantage against its competitors.

The fourth reason I am in full support of this agreement is that I believe the two governments are committed to fulfilling their agreement. Much has been written about potential loopholes in the agreement. Let me respond by citing two examples where the efforts of the two governments prevented the principles of the agreement from being undermined. The first example is the Department of Commerce's swift action to define EPROMs as including one-time programmable EPROMs, thereby halting an effort by Japanese dumpers to shift to those products after the preliminary duties were announced in the EPROM case. The second example is MITI's reported use of Japan's export control law to prevent a surge of orders on the eve of the accord from being "grand-fathered" out of the agreement. If the governments continue to exercise such resolve, the agreement will work.

My fifth and final reason for support is that the agreement can be rapidly enforced. Quarterly access reviews, 14-day notification of dumping, and reinstatement of the suspended suits are all methods of rapid response.

Let me close with four major challenges which are presented by the agreement.

First, the U.S. semiconductor merchant companies are challenged to make the most of the access opportunities presented by the accord. Under the agreement, the Japanese Government has committed to encourage "foreign-based" (note I did not say U.S.) semiconductor purchases, so if the Korean industry or the European industry were able to produce cheaper, higher quality, or more reliable semiconductors than the U.S. industry, those industries would also benefit from the agreement and to a greater degree than the U.S. industry. Similarly, if any given U.S. company has higher quality and reliability, lower prices, or better technology than its U.S. or foreign competitors, then that firm will benefit from the agreement and the others will not. The access share of market increase is not a given, but would have to be the result of American competitiveness as well as the Japanese newly-agreed willingness to open their markets.

A second challenge for semiconductor manufacturers is to assimilate into the Japanese market. While our challenge under market access is to pursue the Japanese market with vigor, the challenge of assimilation goes beyond increased sales. More U.S. companies will, in time, install manufacturing operations in Japan, both as a mechanism to stay close to the Japanese market, and as a base to facilitate intra-corporate technology transfers between Japan and the United States. The agreement promotes such relationships by its guarantee of Japan's national treatment for investments and access to patents from Japanese Government-sponsored R&D programs.

A third challenge for both U.S. semiconductor merchants and semiconductor users is to monitor the marketplace and report any dumping activities to the U.S. Government. Under the agreement, dumping by Japanese producers should stop in all world markets. As I mentioned before, it is in the interests of both merchants and users to insure that offshore dumping as well as dumping into the U.S. is prevented. The U.S. Government's ability to call for consultations with the Japanese Government to end activities which are inconsistent with Japan's commitments under the agreement, is directly dependent on the U.S. Government's ability to gather data on price anomalies around the globe.

Finally, a fourth challenge for semiconductor merchants, semiconductor users, and semiconductor equipment manufacturers is to work together to strengthen the infrastructure for semiconductor production, and the electronics industry itself, in the United States. Meeting the challenge of manufacturing excellence requires the production of a critical mass of high volume semiconductors to support continued R&D by the equipment vendors. The severe dumping in DRAMs, and the subsequent withdrawal from that product line by many U.S. manufacturers, has had a negative impact beyond the lost sales in DRAMs. Without that high volume product, U.S. equipment producers must turn to less-than-ideal chip products to hone their manufacturing skills. In the long run, this competitive disadvantage will handicap the production of state-of-the-art semiconductors in the U.S. Maintaining the viability of our infrastructure will require a greater degree of cooperation between the semiconductor industry and its upstream suppliers and downstream customers. In fact, it may require a cooperative commercial venture that can be tested in the marketplace, a cooperative ventue of makers, suppliers, users and government. How we meet this last challenge will determine if the U.S. electronics industry retains its position as the world's technological leader.

Let me summarize the general principles upon which the agreement is based:

Greater access to foreign markets, and elimination of persistent predatory practices are necessary for a competitive global electronics and semiconductor market. Any attempts by governments or industries to distort the marketplace by implementing industrial trade policy targeted at American electronic markets are not acceptable. This trade agreement attempts to correct such long-practiced distortions and provides solutions not possible under previously applied laws or agreements. In my opinion, it may become a model for future solutions in other segments of the .ectronics industry.

It's time for the American electronics industry — in toto — to re-energize its expansionary efforts in the global marketplace. That, however, cannot be done unless we first make sure that we are the unquestioned leaders in the United States. That may take structural changes of an economic, social, or political nature. This agreement gives us time to start those permanent changes.

In this case, the trade agreement is not an end at all, it's just the beginning in holding the technological high ground — that-is, the world's semiconductor market leadership.

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FAB AUTOMATION IN THE U.S.: BRINGING THE DREAM TO REALITY

Susan Powell Billat
Manager, Wafer
Microelectronics Group
Bechtel National, Inc.

Ms. Billat is Manager of Bechtel's Microelectronics Group. She is responsible for all aspects of developing the business, negotiating contracts, assembling project teams, overseeing work in progess, client relations, and successful completion of the work. Previously, she held positions at Advanced Micro Devices and Hewlett-Packard in process engineering, advanced bipolar, MOS, and CMOS process development, lithography development, and wafer fab automation. She has authored more than 30 publications in these fields and was responsible for the upgrade of an advanced technology fab to a Class 10 facility. Ms. Billat received B.S. and M.S. degrees in Physics from Georgia Institute of Technology.

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Fab Automation in the U.S.:

Bringing the Dream to Reality

Susan Powell Billat

Bechtel National, Inc.

Dataquest Semiconductor Industry Conference

October 21, 1986

Or, How to Use Automation as a Strategic Weapon

Automation has to start at the planning stages

- Automation and construction account for considerable spending
  - U.S. semiconductor firms spent 10-20% of sales on R&D and 30% of sales on new plants and equipment during the past two years, a slow sales period
  - The full scope and cost of automation need to be seen
- Current facilities have to be upgraded to make competitive parts
  - 80% of Japan's chipmaking capacity can product ICs with circuit lines less than 2 microns wide; U.S capacity is only 35%
  - Since 65% of capacity must be upgraded, this is the opportunity to incorporate the new strategy in automation
- Automation facilitates conceptual design
  - Dynamic simulation demonstrates alternative layouts
  - 3-D CADD assists designers
  - Designing with 3-D dynamic simulation permits incorporation of:
    - Flexibility
    - Phased automation
    - Manufacturability
    - Capacity
    - Aesthetics
    - Safety
  - Iterative simulation provides on-going verification and improvement on original model
- Semiconductor industry can benefit from other industries' use of dynamic simulation
  - Complexity of processes in semiconductor manufacturing delayed its use of dynamic simulation
  - Dynamic simulation is not new: Some automotive companies now will not allow capital purchases without prior factory simulation
  - Application to design of baseball-only park gives case in point

A new organizational structure is required to implement automation

- Current decision makers are Engineering and Information Services - two groups that do not talk to one another
- A new organization needs to be defined, incorporating Facilities and Manufacturing
- Many believe that artificial intelligence is the next step in implementing automation
  - AI is impossible without the involvement of all disciplines
  - AI's earliest practical application is expected to be in diagnostic maintenance
- Personal experiences
  - Fab CIM system that failed
    - IS manager had no fab experience
    - IS engineers outnumbered fab engineers
    - Operators' jobs were made tedious
  - Assembly CIM system that failed
    - Good team
    - Friendly system
    - Good intentions
    - No flexibility negated all the above
  - Fab CIM system that worked
    - IS manager had fab engineering and manufacturing experience
    - All disciplines were committed to the project
    - Operator job functions were made easier
    - In spite of numerous false starts and system inefficiencies

The new corporate structure requires an integrated approach and a new leader, the Chief Information Officer

- "Management's newest star" is needed to implement the new team
- Typical IS Manager profile
  - Accounting oriented
  - Computer bound
  - Isolated from technical and manufacturing functions
- CIO profile
  - Business manager
  - Missionary
  - Visionary
  - Consensus builder
  - Manufacturing or engineering background

For automation to succeed, a new organizational structure that integrates all aspects of factory automation - from simulation through execution - is required.

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EUROPE'S RENEWED VLSI THRUST

Gernot J. Oswald
Executive Director,
Components Group
Siemens AG

Mr. Oswald is in charge of Siemens AG's worldwide semiconductor component sales and marketing and is based in Munich, Germany. He has 24 years of experience in semiconductor components. Previously, he held various management positions at Siemens AG in development, marketing, and sales of discrete semiconductor components, integrated circuits, and microcomputer systems. Mr. Oswald studied Physics in Madrid, Spain, and in Germany. He received an M.A. degree in Theoretical Physics from the Technische Universitaet, Munich, Germany.

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"Europe's Renewed VLSI Thrust"

by Gernot Oswald
SIEMENS AG

Most of Dataquest's Semiconductor Industry Conferences included a section devoted to the situation in Europe. Without any exception the message was either - depending on the condition of the market - "everything is great" or "everything is going to be all right". My honest opinion is that the European Semiconductor Industry was never as sick as most of our friends from overseas thought and was never as great as we tried to believe ourselves. When I gratefully accepted the invitation to speak today about "Europe's Renewed VLSI Thrust", I did so because I am convinced that something is happening in Europe, which is different, new and exiting enough to deserve the interest of even this distinguished audience.

What has changed? What is going to change?

More or less everything: The game, the rules and the players.

<u>VLSI - the changing game</u>

The market

The computer segment is still the largest single market for IC's. Europe's participation in this segment has been very weak. It seems however, that telecommunications, robotics and automobiles will provide the biggest growth opportunities for the next ten years. Europe has a strong and innovative home market in all of these areas.

"Consumption" of Semiconductor Components 1985 (Billions of US$)

	U.S.	W.E.	JPN	ROW	Total
Data Processing	3.7	0.9	2.6	0.4	7.6
Communications	1.4	1.2	0.8	0.2	3.6
Industrial	1.5	1.1	0.8	0.2	3.6
Consumer	0.7	1.0	4.0	0.8	6.5
Military	1.5	0.4	-	0.0	1.9
Transportation	0.8	0.3	0.3	0.1	1.5
	9.6	4.9	8.5	1.7	24.7

Source : Dataquest
Siemens for ROW

The product

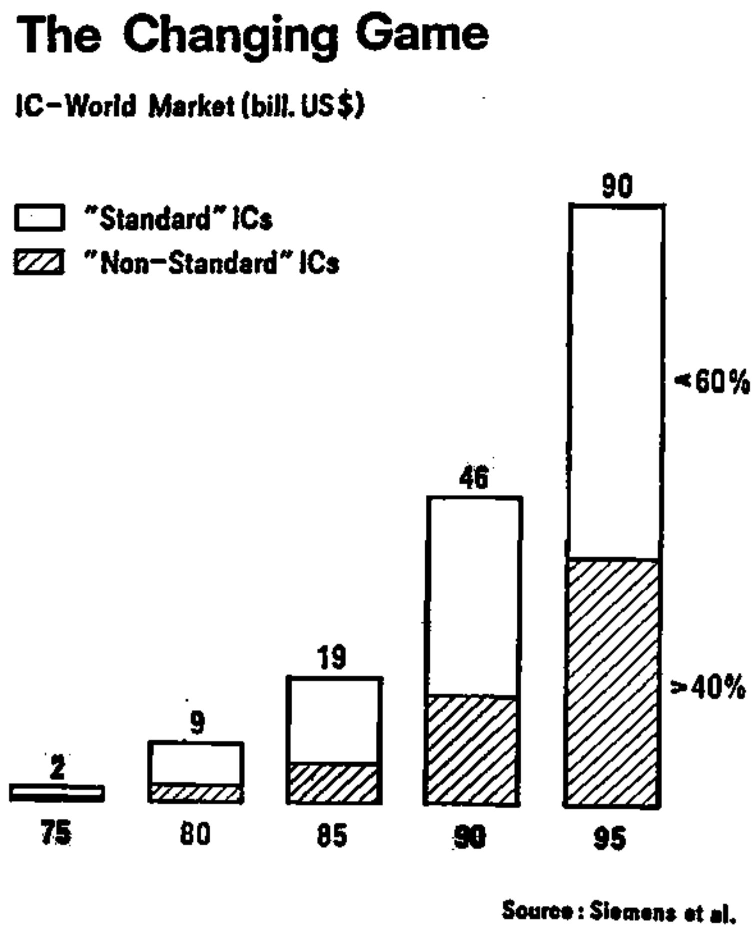
Standard products, like logic families (TTL etc.), memory-circuits and catalog-microcomputer-components have so far dominated the market. American and Japanese companies shared these markets between themselves. Only application oriented products, "non standards" have been supplied by Europe-based companies in any noteworthy amount.

Worldwide Merchant Market Shares 1985

	US-based	Japan-based	Europe-based
Total IC's	49%	39%	10%
Standard Logic	59%	31%	9%
Memory Products	39%	53%	7%
Standard µP/µC	55%	38%	6%
"NON-Standards"	43%	33%	23%

Source: Dataquest, Siemens

The recent worldwide progress in design productivity is shifting the VLSI market strongly towards non-standard IC's.



The customer

The application and customer oriented IC requires both sophisticated procurement methods and close vendor customer relationships. These relationships are becoming more farsighted, engineering driven and selective. It seems that the IC shortage in 1984 has also taught some buyers to distinguish between spot market opportunities and business partnerships. The European business style has always been more long term oriented. Therefore, European companies should benefit from this trend.

The unchanged "basics"

It seems, however, that some basic trends of our industry will not change in the foreseeable future: The compound average growth rate should be around 20 % per year. The competition will continue to be fierce and worldwide despite some protectionistic attempts. Gordon Moore's exponential law of increasing complexity, increasing performance and decreasing cost will be valid for quite sometime.

VLSI - the changing rules

To play in the major league has become pretty expensive. The entrance fee is now hundreds of millions of dollars and the top players are investing Gigabucks each year in the Mega-Chip-Game.

It takes more and more time to get these Gigabucks back, which means that fewer companies will be able to play this game. The winning strategies are being modified. The American product differentiation and the Japanese low cost/high quality approach have to be enriched by design productivity, control of logistics and service. But one of the more important success factors will be the ability to gain and keep customers loyalty.

VLSI - the changing players

The history of our industry in the 70's was written by outstanding American entrepreneurs of extremely different personalities like Gordon Moore, Bob Noyce, Jerry Sanders or Charlie Sporck, to name just a few.

The 80's seem to be the decade of more or less uniform companies, which are all big, all vertically integrated and *all Japanese. They also have great individuals, but these are much less visible. Our industry is becoming the battleground of nations. More and more politicans begin to understand that microelectronics is as important to the economy of industrial countries as electricity is to a modern household. What we used to call the "Rest of World" has joined the race, with the Koreans already becoming "nasty" and the Chinese being just around the corner.*

Even in Europe the majority of lawmakers are finally working hard to get acquainted with the fact that the public opinion about microelectronics has dramatically changed. The discussion about "job killers" is "out". Governments and companies are willing to invest time and money in order to keep this industry alive and able to compete.
New teams of management with international experience have been installed and thousands of young, talented and enthused engineers and scientists have been hired.

What's the score?

Europe is obviously not defeating its American and Asian competitors; but it has the best team ever and will give them a tough time.
The statistics for 1986 will most likely show that Europe

continues to modestly regain market share, both using and producing VLSI products.
In the last three years the number of R+D people has more than doubled and state of the art manufacturing plants have been built.

But there are major constraints to the increased competitiveness of the European IC-industry. The most important reasons for Europe's disadvantageous position compared to Japan and the United states are still the fragmentation of its home market and its efforts, and the limited flexibility of its workforce.

Today, some 40 % of the manufacturing costs of IC's are capital costs. Our overseas competitors run their factories 20 shifts per week. A combination of strange labor rules and the lack of flexibility of unions and politicians limit the usage of our plants to an average of less than 15 shifts per week. The cost disadvantage of this fact alone - assuming everything else to be equal - is 10 % of sales.

We are also working hard to convince our students, that marketing and sales of sophisticated electronic products is an honest and desirable job for an engineer. Most of our universities still simply refuse to entertain this idea.

Summary

The world market for IC's is becoming more and more

- *application oriented*
- *service oriented and*
- *long term oriented.*

This especially suits both the European company culture and large vertically integrated firms in general. The public opinion in Europe about microelectronics has dramatically changed. This has finally created an environment, which attracts outstanding management talent and a surprisingly large number of ambitious and enthused young engineers and scientists.
There is still a tremendous amount of problems to be overcome, but many ot them are homemade. Both the climate for microelectronics and the teams working in the European IC-industry have never been better.
The market is there, the required funding is available - people will make the difference.

"Europe's Renewed VLSI Thrust"

by Gernot Oswald

SIEMENS AG

Question: What has changed?

What is going to change?

Answer: More or less everything:

- The game
- The rules
- The players

The Changing Game

- The market
- The product
- The customer
- The unchanged "basics"

The Changing Game

The market

- Telecom, robotics and automotive become the driving forces
- Europe has strong markets for these products

"Consumption" of Semiconductor Components 1985 (Billions of US$)

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Transportation	0.8	0.3	0.3	0.1	1.5
	9.6	4.9	8.5	1.7	24.7

Source : Dataquest
Siemens for ROW

The Changing Game

The product

- "Non-Standard" ICs gain market share
- Low cost, high quality become "commodities"
- Presales-, application-, aftersales services differentiate the product

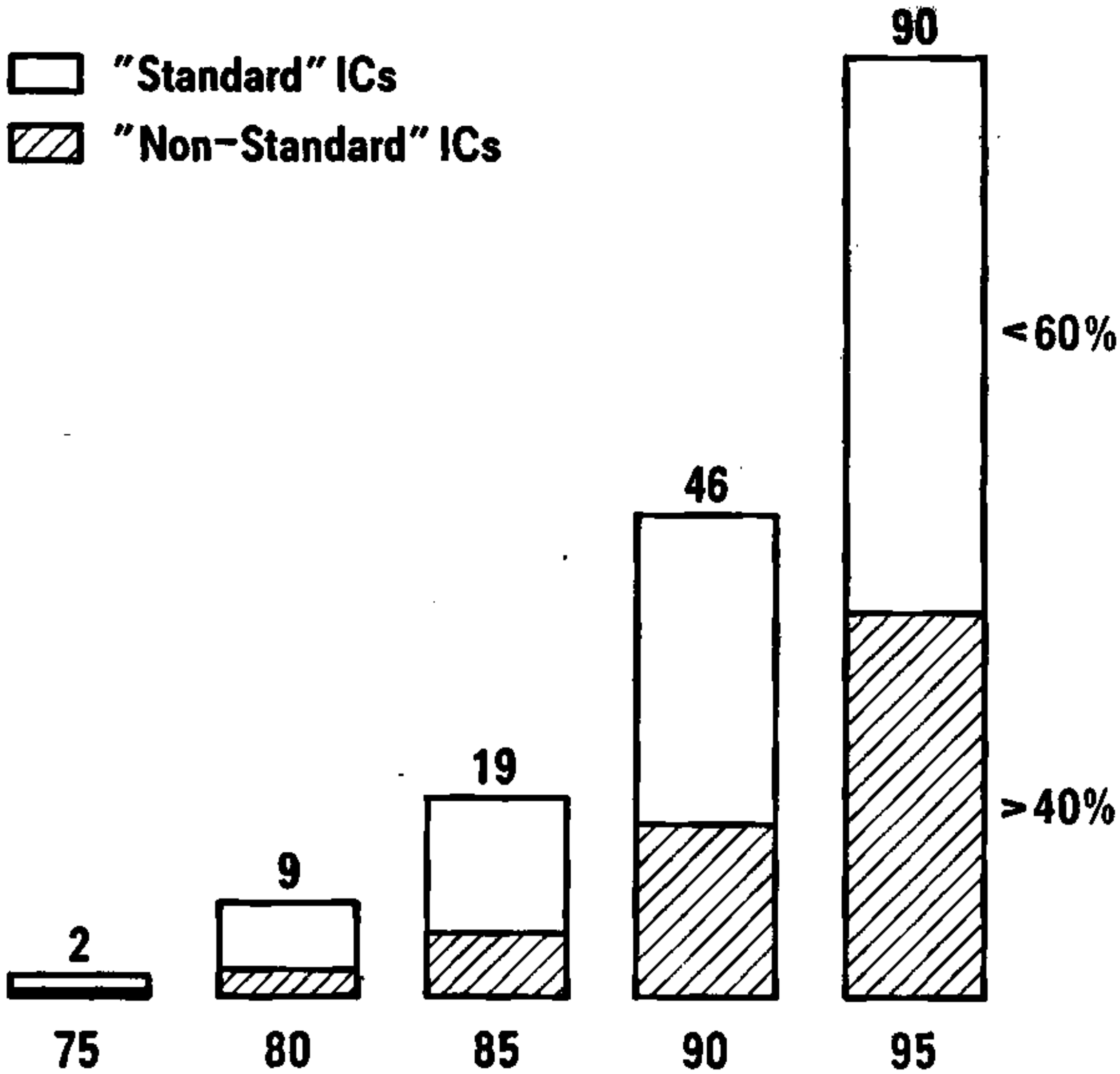
The Changing Game

The product

- "Non-Standard" ICs gain market share
- Low cost, high quality become "commodities"
- Presales-, application-, aftersales services differentiate the product

The Changing Game

IC–World Market (bill. US$)



Source : Siemens et al.

The Changing Game

Definitions

"Standard"- ICs

- Catalog products
- Various Sources
- Many different applications

e.g.: logic series, memory ICs
standard op. amp's, standard μP's

"Non-Standard"- ICs

- Application oriented
- Semicustom ICs
- Custom ICs

Worldwide Merchant Market Shares 1985

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Standard µP/µC	55%	38%	6%
"NON-Standards"	43%	33%	23%

Source : Dataquest , Siemens

The Changing Game

The customer

- Procurement becomes more sophisticated
  - more farsighted
  - more engineering driven
  - more selective
- Long term convergence of computers, telecommunication and consumer products

The Changing Game

The unchanged "basics"

- Increasing complexity
- Increasing speed /performance
- Decreasing cost / price
- Market growth of 20% per year
- Worldwide market / competition

The Changing Rules

- Entrance fee
- Return on investment
- Winning strategies

The Changing Rules

Winning strategies

used to be:

- Product differentiation
- Low production cost
- High quality standards

of growing importance are:

- Design productivity
- Control of logistics and service
- Customer loyalty

The Changing Players

- Vertically intergrated companies
- Multinational firms
- Nations
- "The rest of world"

The Changing Players in Europe

- Management
- Public opinion
- Political environment
- The young people

Barriers

- Fragmented market and efforts
- Protectionism
- The other 50% of our politicians
- Labor
- Marketing

Summary

- The market becomes more favorable
- The money is available
- It is still not easy, but there are no more excuses
- People will make the difference

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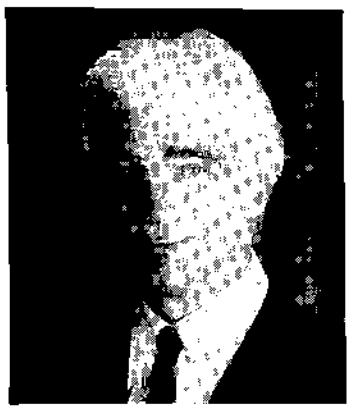
CONTRIBUTION: THE NEW COMPETITION



W.J. Sanders III
Chairman of the Board and Chief Executive Officer
Advanced Micro Devices Inc.

Mr. Sanders is Chairman and Chief Executive Officer of Advanced Micro Devices Inc. and is also cofounder of the company. Before cofounding AMD, Mr. Sanders was Group Director of Marketing Worldwide for the Semiconductor Group of Fairchild Camera and Instrument Corporation. Previous positions at Fairchild included Regional Sales Manager, Area Sales Manager, Department Head, and Director of Marketing. Prior to Fairchild he worked in the engineering department of Douglas Aircraft Co. and in sales and marketing for Motorola Semiconductor. Mr. Sanders is also a cofounder and director of the Semiconductor Industry Association and a cofounder of the Santa Clara County Manufacturing Group, the Semiconductor Research Corporation, and The Microelectronics and Computer Technology Corporation. Mr. Sanders graduated from the University of Illinois College of Engineering with a B.S. degree in Electrical Engineering.

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(THIS SPEECH WAS NOT AVAILABLE AT TIME OF PUBLICATION)

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CMOS PROGRAMMABLE LOGIC DEVICES

A panel session on the strategic role of CMOS PLDs

Wednesday, October 22, 8:00 a.m. to 9:30 a.m.

CMOS programmable logic devices (PLDs) are expected to play a vital role in the growth of the ASIC market for the balance of this decade. Dataquest believes that the emergence of CMOS PLDs could alter the way ASIC products are used. We expect that CMOS and bipolar PLD revenue will exceed $1 billion by 1990 and that the CMOS segment will make up one-half of the market, significantly impacting gate arrays and standard logic.

The companies selected for this CMOS PLD panel are among some of the most innovative and diverse. They represent a new wave of suppliers who offer performance and architectural flexibility that goes far beyond what was available a few years ago. They foresee applications for their product that were once the exclusive domain of the bipolar suppliers. These proponents believe that CMOS PLDs will ultimately challenge all but the fastest applications. Panelists representing these companies will offer their unique perspectives on the role of PLDs and will present their views on the critical issues that will impact the ASIC industry.

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Dane Elliot

Mr. Elliot is Manager of Application Engineering for Cypress Semiconductor. He has 22 years of experience in the industry, including working for Beckman Instruments and Intel Corporation. Mr. Elliot has experience in areas ranging from microprocessors to PLDs and high-speed memory. His perspective covers technical components and system designs with respect to following design issues in silicon. Mr. Elliot has a B.S.E.E. degree from California State Polytechnic University.

Andrew Haines

Mr. Haines is the Strategic Marketing Manager of Application-Specific Products at VLSI Technology, Inc. (VTI). He has worked at VTI for five years, holding a variety of positions in both the ASIC and CAE areas. Prior to joining VTI, Mr. Haines was employed at Intel Corporation as Marketing Manager of Microprocessors. Mr. Haines received a B.S. degree in Physics from the University of Wisconsin.

David A. Laws

Mr. Laws is Vice President of Marketing at Altera Corporation. He has spent more than 22 years in marketing and general management in the semiconductor industry. Prior to joining Altera, Mr. Laws spent 11 years with Advanced Micro Devices, most recently as Vice President. Before that, Mr. Laws was Managing Director of Programmable Logic and Bipolar Gate Array Products for AMD. He has also held marketing positions at Signetics, Litronix, and Fairchild Semiconductor. Mr. Laws received a B.S. degree in Physics from Hull University in Yorkshire, England.

Wes Patterson

Dr. Patterson is a Senior Vice President at Xilinx. Prior to joining Xilinx, he was General Manager of Custom Products for VLSI Technology, Inc. Earlier, he held management and design positions at Motorola and Honeywell. Dr. Patterson received a B.S. degree in Computer Science from Michigan State University and M.S. and Ph.D. degrees in Electrical Engineering from Arizona State University.

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TRENDS IN CMOS PLDs

Andy Prophet
Senior Industry Analyst
Semiconductor Industry Service
Dataquest Incorporated

Mr. Prophet is a Senior Industry Analyst for Dataquest's Semiconductor Industry Service. He is responsible for analyzing the application-specific market environment and future technology trends. Before joining Dataquest, he held a variety of strategic marketing and engineering management positions for 23 years, largely with companies that are active in the application-specific IC market. Mr. Prophet has been responsible for developing major account marketing strategies, managing CAD development, and product line and circuit design management. He received a B.S.E.E. degree from the Illinois Institute of Technology, an M.S.E.E. degree from San Jose State University, and an M.B.A. degree from the University of Santa Clara.

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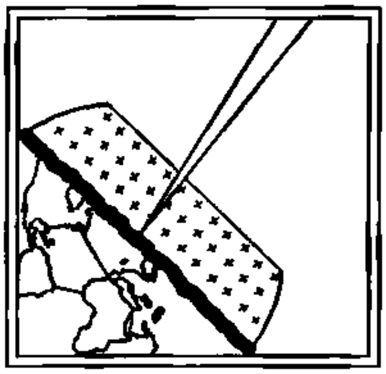


Recovery: Managing the New Industry Structure

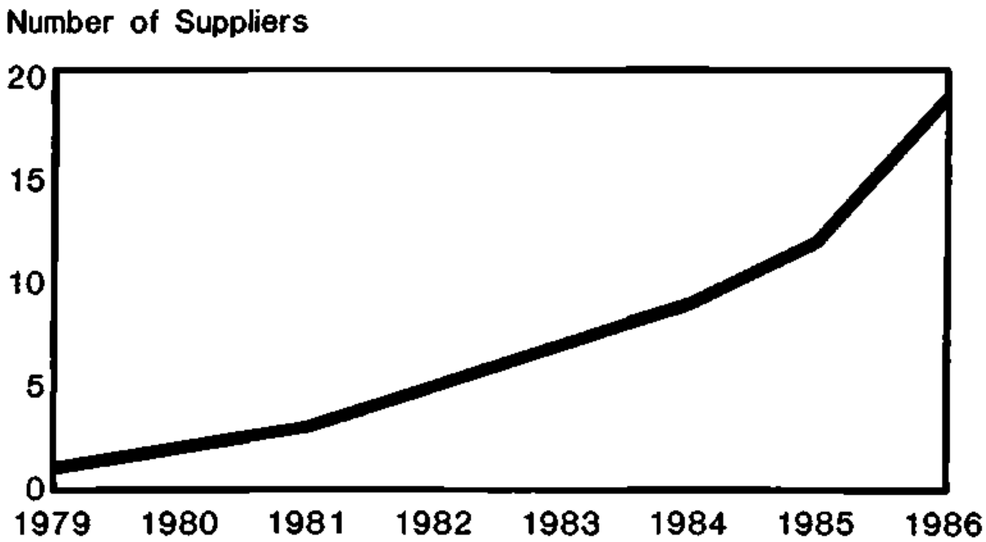
ASIC FOCUS SESSION

Trends in CMOS PLDs

ANDREW M. PROPHET

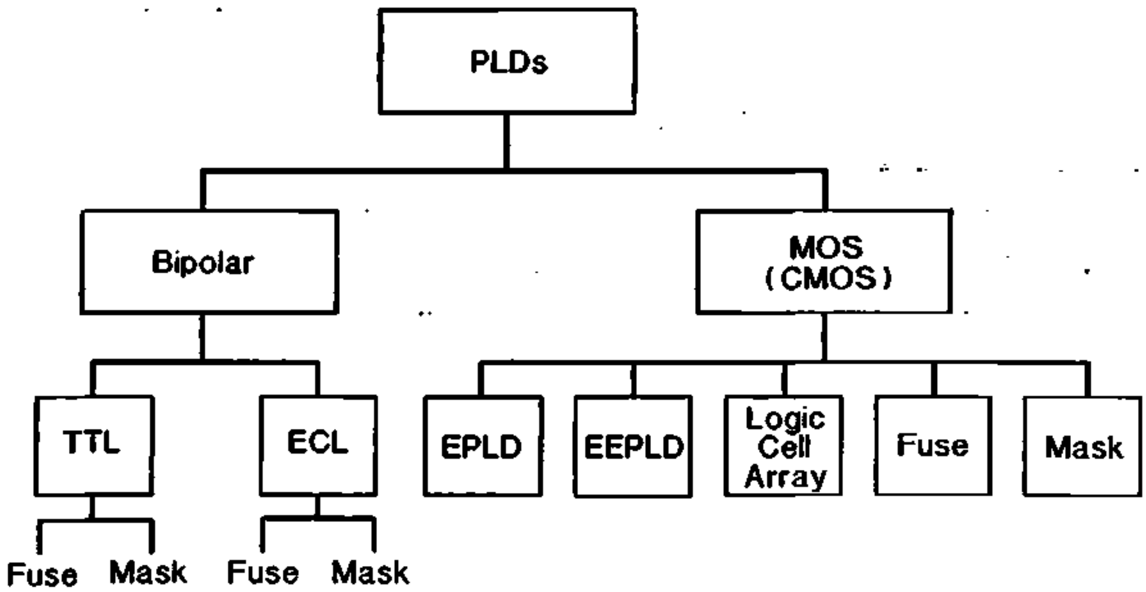
Senior Industry Analyst
Semiconductor Industry Service
Dataquest Incorporated

GROWTH IN PROGRAMMABLE LOGIC SUPPLIERS



Source: Dataquest

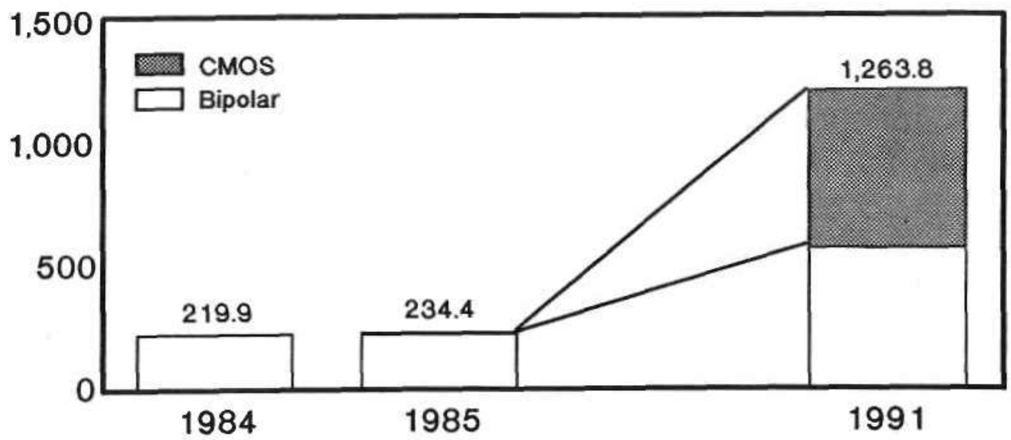
PROGRAMMABLE LOGIC FAMILY TREE



Source: Dataquest

ESTIMATED WORLDWIDE CONSUMPTION OF PROGRAMMABLE LOGIC DEVICES

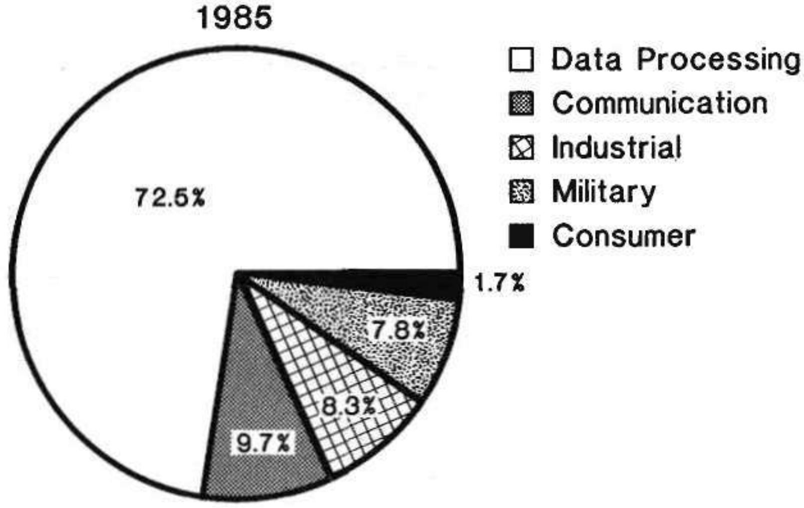
By Technology
(Millions of Dollars)



Source: Dataquest

TOTAL ESTIMATED PROGRAMMABLE LOGIC DEVICE

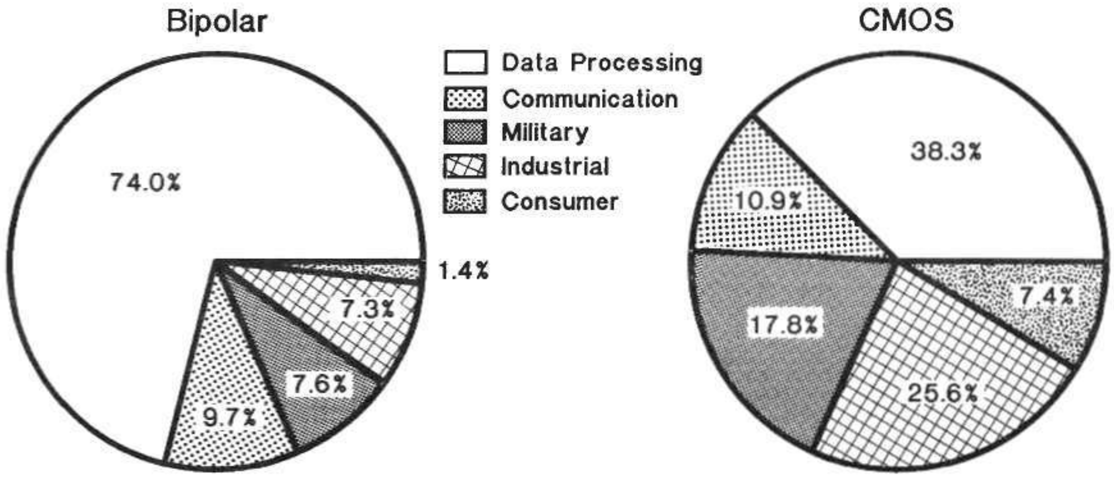
End-Use Consumption



Source: Dataquest

ESTIMATED PROGRAMMABLE LOGIC DEVICE END-USE CONSUMPTION

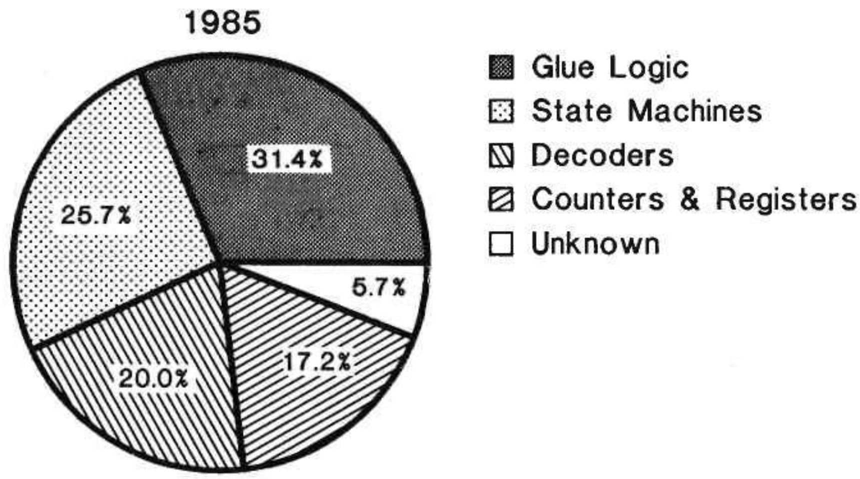
1985



Source: Dataquest

ESTIMATED PLD CONSUMPTION BY APPLICATION

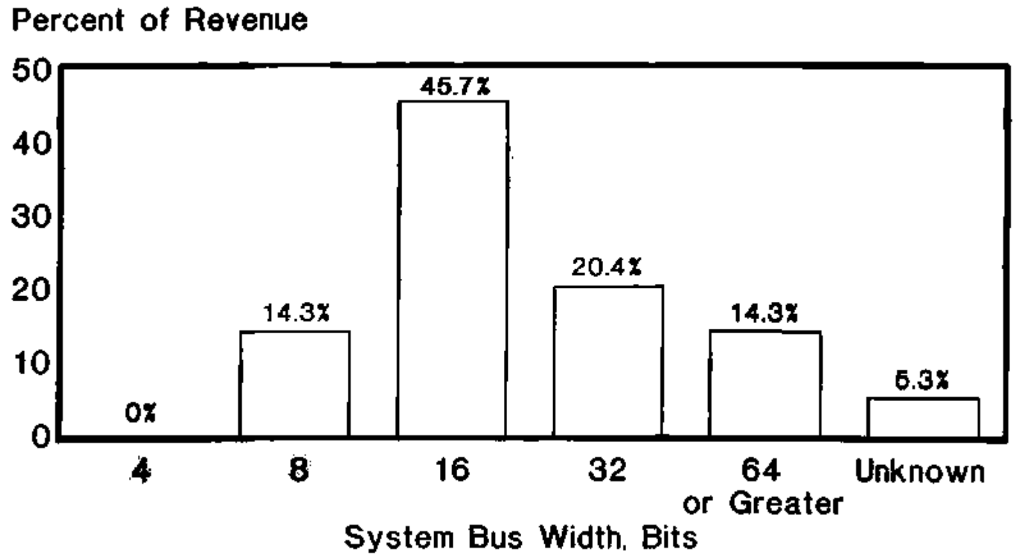
Percent of Revenue



Source: Dataquest

PLD USAGE BY SYSTEM BUS WIDTH

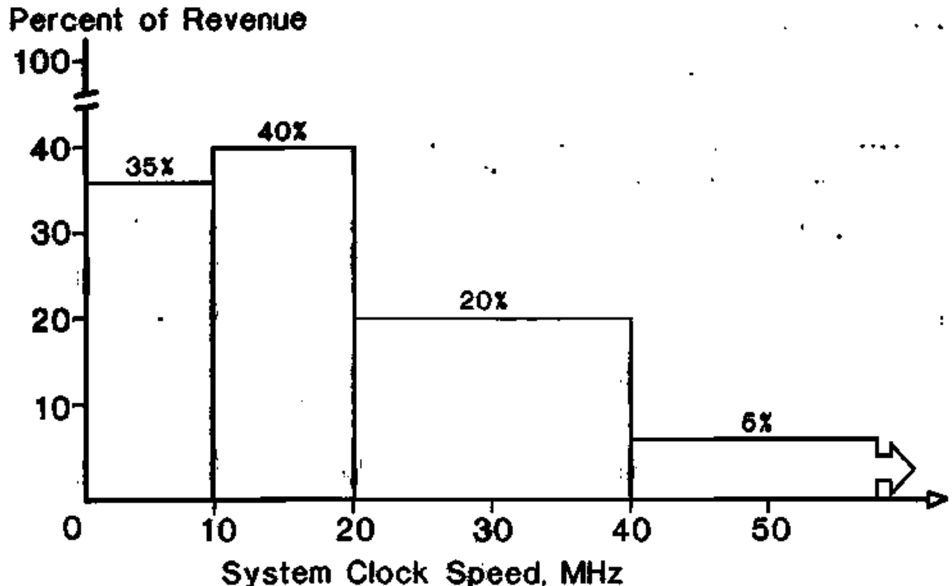
1985



Source: Dataquest

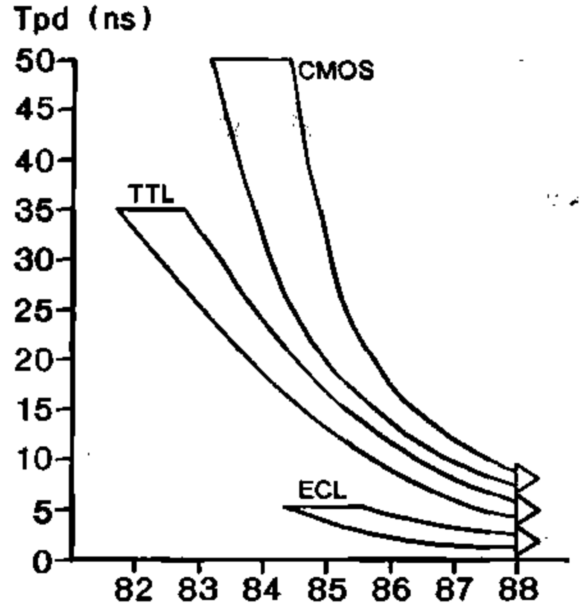
PLD USAGE BY SYSTEM CLOCK SPEED

1985



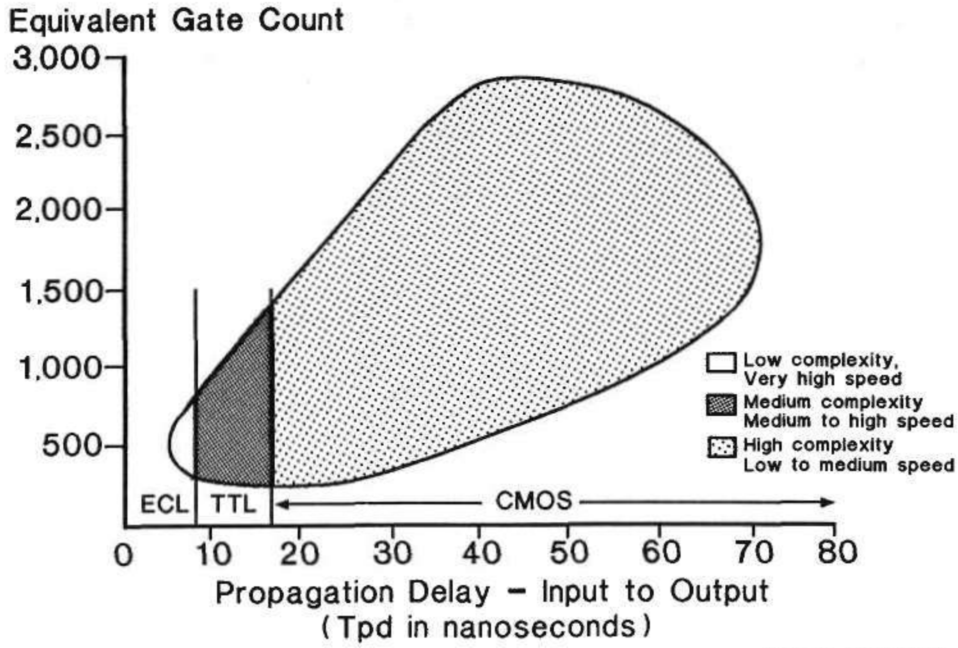
Source: Dataquest

ESTIMATED PLD SPEED TRENDS



Source: Dataquest

PLD GATE COUNT VS. PROPAGATION DELAY



Source: Dataquest

ISSUES

- Critical growth factors?
- Which CMOS technology will win?
- Impact on gate arrays, CBIC, or standard logic?
- Emerging products?
- Most promising architectures?

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CRITICAL FACTORS THAT WILL IMPACT THE GROWTH OF PLDS

DEVELOPMENT OF PRODUCTS OFFERING THE OPTIMUM COMBINATION OF:

- LOGIC DENSITY
- PERFORMANCE
- TOTAL COST/GATE
- EASE OF USE

IN ORDER TO OFFER A USEFUL ALTERNATIVE TO:

- STANDARD TTL/CMOS FAMILIES
- BIPOLAR PLDS
- LOW DENSITY GATE ARRAYS

ALTERA

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DENSITY REQUIREMENTS FOR

VLSI DESIGNS

NUMBER OF GATES/PACKAGE	1986		1988	
LESS THAN 1K	40%	52%*	35%	54%*
1K - 2K	12%		8%	
2K - 5K	18%		11%	
GREATER THAN 5K	30%		45%	

SOURCE: CMP PUBLICATIONS, INC.
CUSTOM/SEMICUSTOM STUDY (QU #8) 7/86

* HIGH DENSITY EPLD COVERAGE

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PERFORMANCE REQUIREMENTS

FOR VLSI DESIGNS

CLOCK SPEED	1986		1988	
Less Than 10 MHz	18%	70%* (Less Than 10 MHz and 10 - 20 MHz)	18%	65%* (Less Than 10 MHz to 20 - 40 MHz)
10 - 20 MHz	26%		24%	
20 - 40 MHz	25%		23%	
Greater Than 40 MHz	31%		35%	

Source: CMP Publications, Inc.
Custom/Semicustom Study (Qu #10) 7/86

* High Density EPLD Coverage

ALTERA

PRODUCTION VOLUMES FOR

ASIC DEVICES

NUMBER OF DEVICES	1985	1988
LESS THAN 1K	56%	47%
1K - 10K	20%	24%
GREATER THAN 10K	24%	29%

ASIC INCLUDES FULL CUSTOM, GATE ARRAYS, STANDARD CELLS, SILICON COMPILERS (EXCLUDES PLDs).

SOURCE: CMP PUBLICATIONS, INC.
CUSTOM/SEMICUSTOM STUDY (QU #5) 7/86

ALTERA

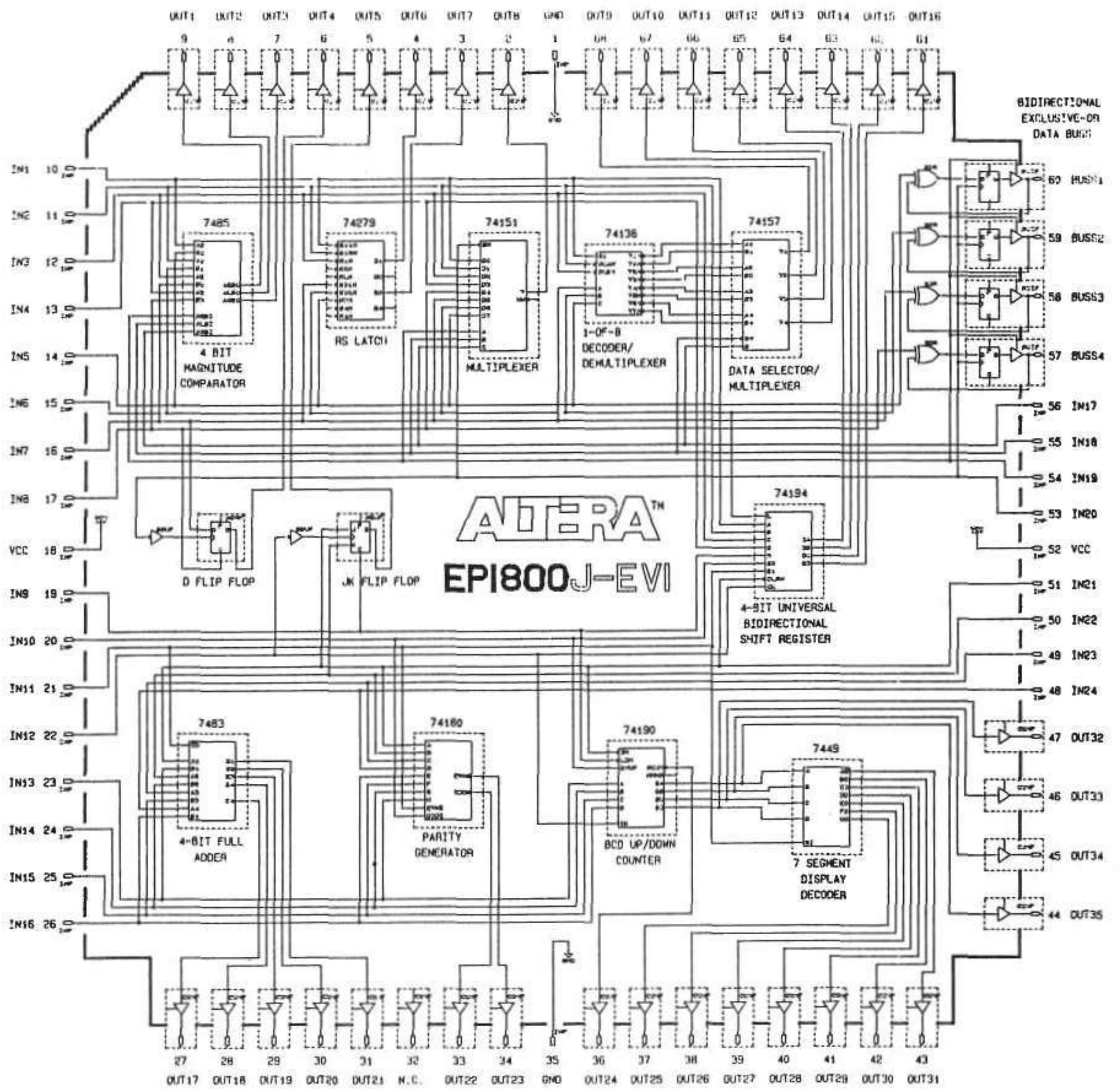
EASE OF USE

- EPLDs CAN BE DESIGNED WITH STANDARD TTL MACROFUNCTIONS
  -- NO MORE BOOLEAN ALGEBRA

- DESIGNS CAN BE COMPILED AND PROGRAMMED IN MINUTES ON IBM PC BASED SYSTEMS
  -- NO NRE, NO LEAD TIME

- FULLY DOCUMENTED AND INTEGRATED WORKING ENVIRONMENT ON THE USER'S DESK
  -- CONTROL YOUR OWN DESTINY

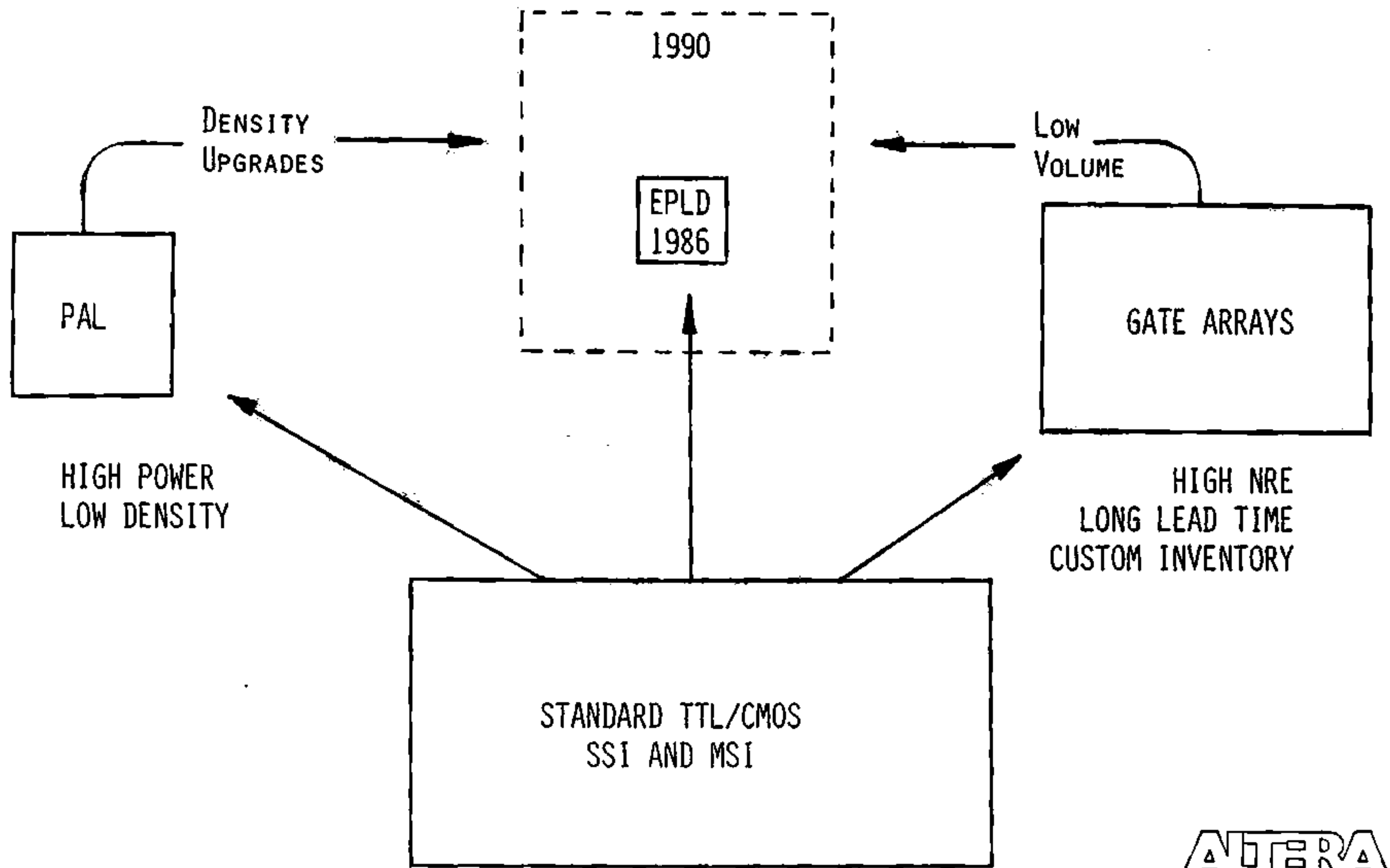
ALTERA



- UP TO 2K GATES
- UP TO 20 MHz
- LESS THAN $20 IN VOLUME

ALTERA

EPLDs, WHERE DO THEY FIT?



ALTERA

NEXT GENERATION PROGRAMMABLE LOGIC

MARKET DEMANDS

TECHNOLOGY OPPORTUNITIES

PRODUCT DIRECTION

MARKET DEMANDS

PRODUCT PERFORMANCE

FASTER Tpd & Tco
HIGHER CLOCK RATES
LOWER POWER

FLEXIBILITY

PROGRAMMABLE ARCHITECTURE
FEWER PRODUCTS IN A FAMILY

HIGHER LEVELS OF INTEGRATION

TECHNOLOGY ADVANTAGE
ARCHITECTURE CHALLANGE
WILL CHALLANGE GATE ARRAYS

SUPPORT TOOLS

ABSTRACT THE PROBLEM
CAD WILL BECOME A NECESSITY
TIMELY PROGRAMMING SUPPORT

TECHNOLOGY OPPORTUNITIES

ECL FOR SPEED
LOW TO MODERATE DENSITY
INVADE LOW END BIPOLAR

BIPOLAR STANDARDS
MODERATE DENSITIES
GOOD PERFORMANCE
CMOS WILL SUPERSEDE

CMOS PERFORMANCE & DENSITY
MODERATE TO HIGH DENSITY
BIPOLAR SPEEDS ARE ON THE WAY
HERE NOW @ HIGHER INTEGRATION

CMOS PRODUCT DIRECTION

FUNCTIONAL PARTITIONING ALONG APPLICATIONS BOUNDRIES

COMBINATORIAL
ASYNCHRONOUS
SYNCHRONOUS

FLEXIBILITY INSIDE PARTITIONS

MACROCELLS
VARIABLE PRODUCT TERMS
UNIVERSAL I/O

HIGHER DENSITIY ARRAY & FUNCTION

>20K CELLS IN ARRAY

CMOS TECHNOLOGY WILL USE:

EPROM FOR CLASSIC ARCHITECTURE
EEPROM FOR NOVEL ARCHITECTURE
DYNAMIC FEATURES FOR LOW POWER

ISSUES

COMMON SOPHISTICATED TOOLS
LEARN ONE/USE MANY
TIMELY PROGRAMMING SUPPORT

TRUE GATE ARRAY ARCHITECTURE
UNRESTRICTED INTERCONNECT

EEPROM ARCHITECTURE
REAL VALUE FOR IN-CIRCUIT
RE-PROGRAMMABILITY

NEW ARCHITECTURES

MEAN

NEW APPLICATIONS

FOR

PROGRAMMABLE LOGIC DEVICES

DATAQUEST
SEMICONDUCTOR INDUSTRY CONFERENCE
October 22, 1986

Wes Patterson
XILINX, INC

XILINX

NEW PLD ARCHITECTURES
NEW PLD APPLICATIONS

DIGITAL LOGIC MARKET GROWTH

($M)	1985	1986	1987	CAGR
SSI/MSI	2478	2506	3028	10.5%
PLD	296	357	455	24.0%
GATE ARRAY	1262	1802	2451	39.4%

SOURCE: DATAQUEST

XILINX

NEW PLD ARCHITECTURES
NEW PLD APPLICATIONS

PLD MARKET LIMITATIONS

o DESPITE DENSITY DISADVANTAGES:

- SSI/MSI MARKET IS STILL 7X PLD MARKET

o DESPITE SEMICUSTOM DISADVANTAGES:

- GATE ARRAY MARKET IS ALREADY 5X PLD MARKET
- GATE ARRAY MARKET IS GROWING FASTER THAN PLD MARKET

o DESPITE PLD ADVANTAGES: DENSITY
USER PROGRAMMABILITY

- CURRENT PLDs SERVE A LIMITED SET OF APPLICATIONS DUE TO ARCHITECTURAL LIMITATIONS

XILINX

NEW PLD ARCHITECTURES
NEW PLD APPLICATIONS

EMERGING PLD ARCHITECTURES

- AND/OR PLANE EXTENSIONS
- APPLICATIONS SPECIFIC PLDs
- ARRAY ARCHITECTURES

NEW PLD ARCHITECTURES
NEW PLD APPLICATIONS

AND/OR PLANE EXTENSIONS

• ALTERA	EP600/EP900	OUTPUT MACRO CELL
• LATTICE	GAL	OUTPUT MACRO CELL
• ALTERA	EP1200/EP1800	AND/OR PARTITION

XILINX

NEW PLD ARCHITECTURES
NEW PLD APPLICATIONS

APPLICATION SPECIFIC PLDs

• AMD	AmPAL23S8	STATE MACHINES
• OTHERS	(unannounced)	BUS CONTROLLER

XILINX

NEW PLD ARCHITECTURES
NEW PLD APPLICATIONS

USER PROGRAMMABLE ARRAY ARCHITECTURES

- XILINX XC2064 PROGRAMMABLE GATE ARRAY

- TOSHIBA TEST CHIP SSI/MSI WITH ARRAY INTERCONNECT

XILINX

NEW PLD ARCHITECTURES
NEW PLD APPLICATIONS

CMOS PLD MARKET SEGMENTATION

PROCESS *vs* ARCHITECTURE

PROCESS

- EPROM
- EEPROM
- SRAM

ARCHITECTURE

- AND/OR PLANE
- APPLICATION SPECIFIC
- ARRAY

XILINX

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E^2 CMOS Programmable Logic

Andrew Haines

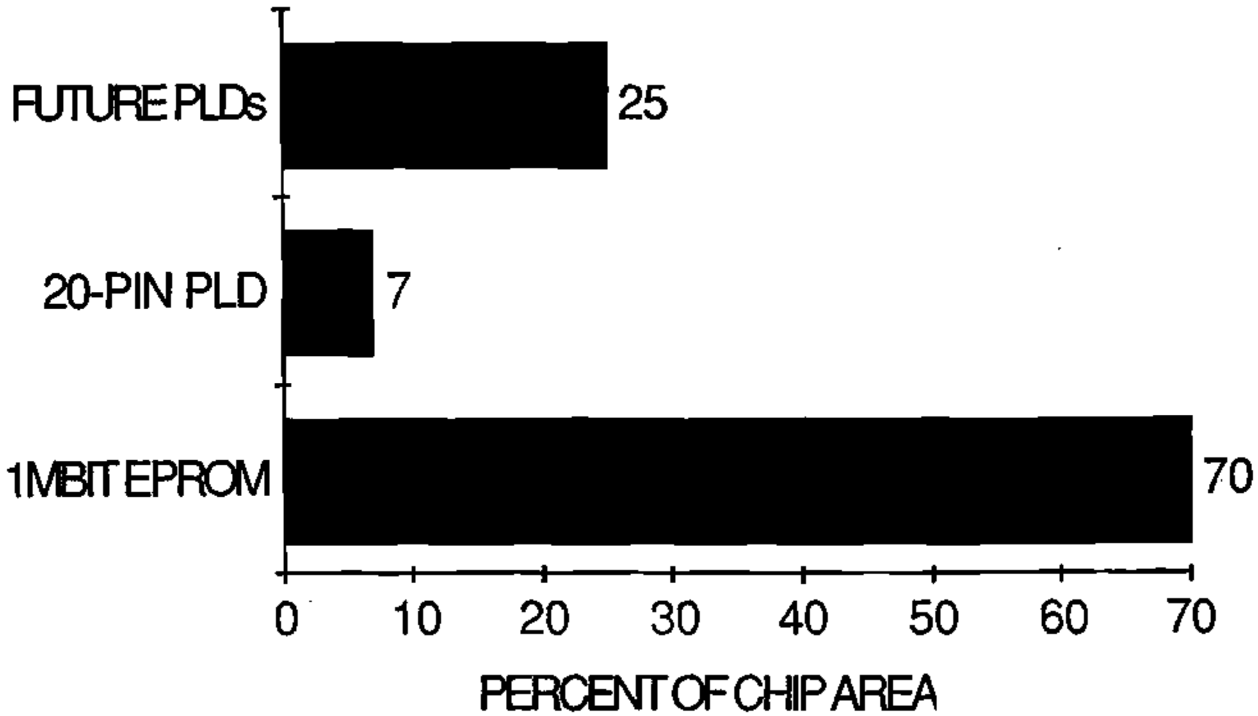
VLSI Technology, Inc.

OVERVIEW

- E^2 VS UV ERASEABLE TECHNOLOGY FOR PLDs
- PLDs AS ASICs
- CONCLUSIONS

VLSI TECHNOLOGY, INC.

CELL ARRAY AREA AS A PERCENT OF CHIP AREA



E^2 VS UV ERASEABLE PLD TECHNOLOGY COMPARISON

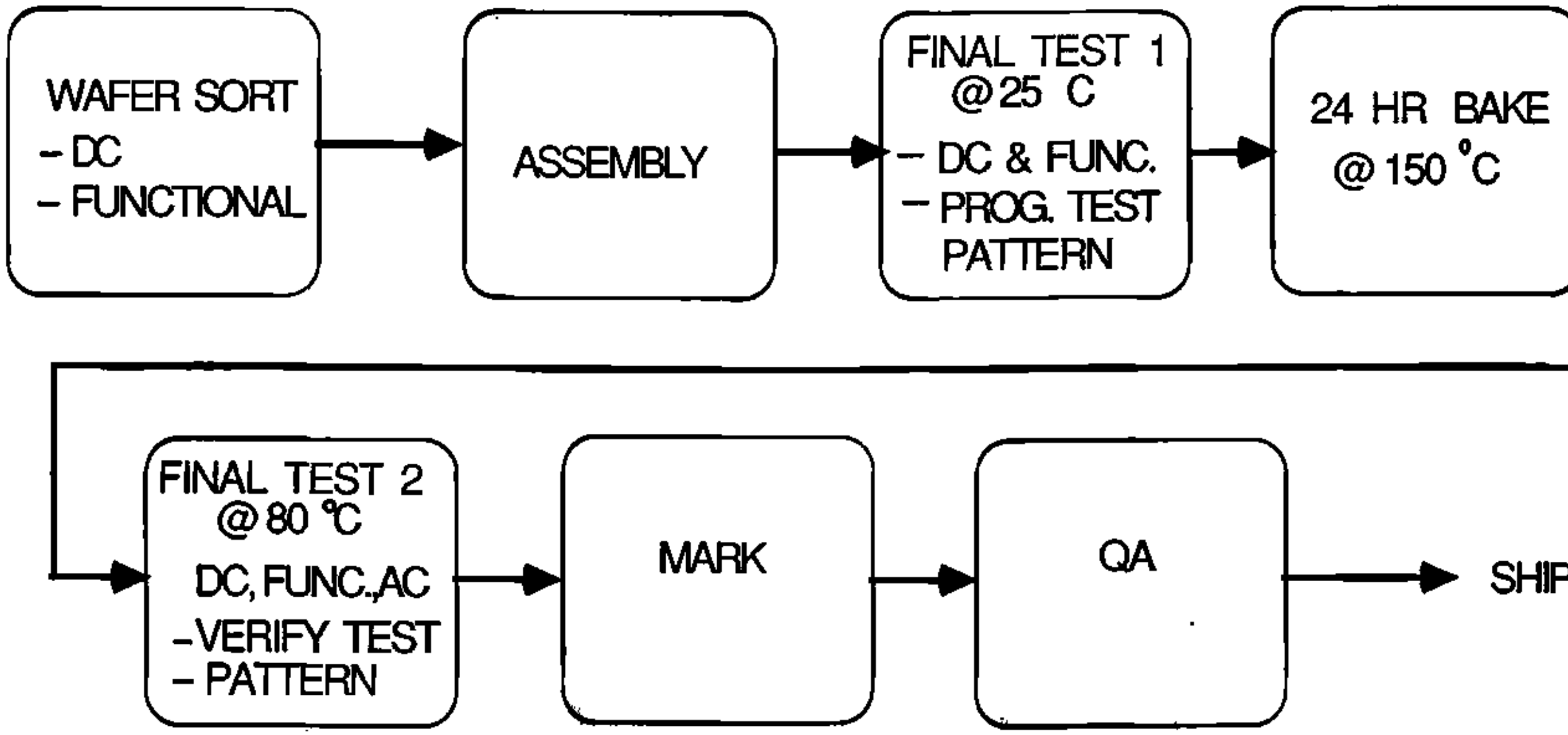
- PERFORMANCE OF E^2 AND UV ERASEABLE IS EQUIVALENT

- RELIABILITY IS NOT A DIFFERENTIATING FACTOR

- REPROGRAMMING FAVORS E^2
  - PROTOTYPING
  - MANUFACTURING
  - IN-CIRCUIT PROGRAMMING

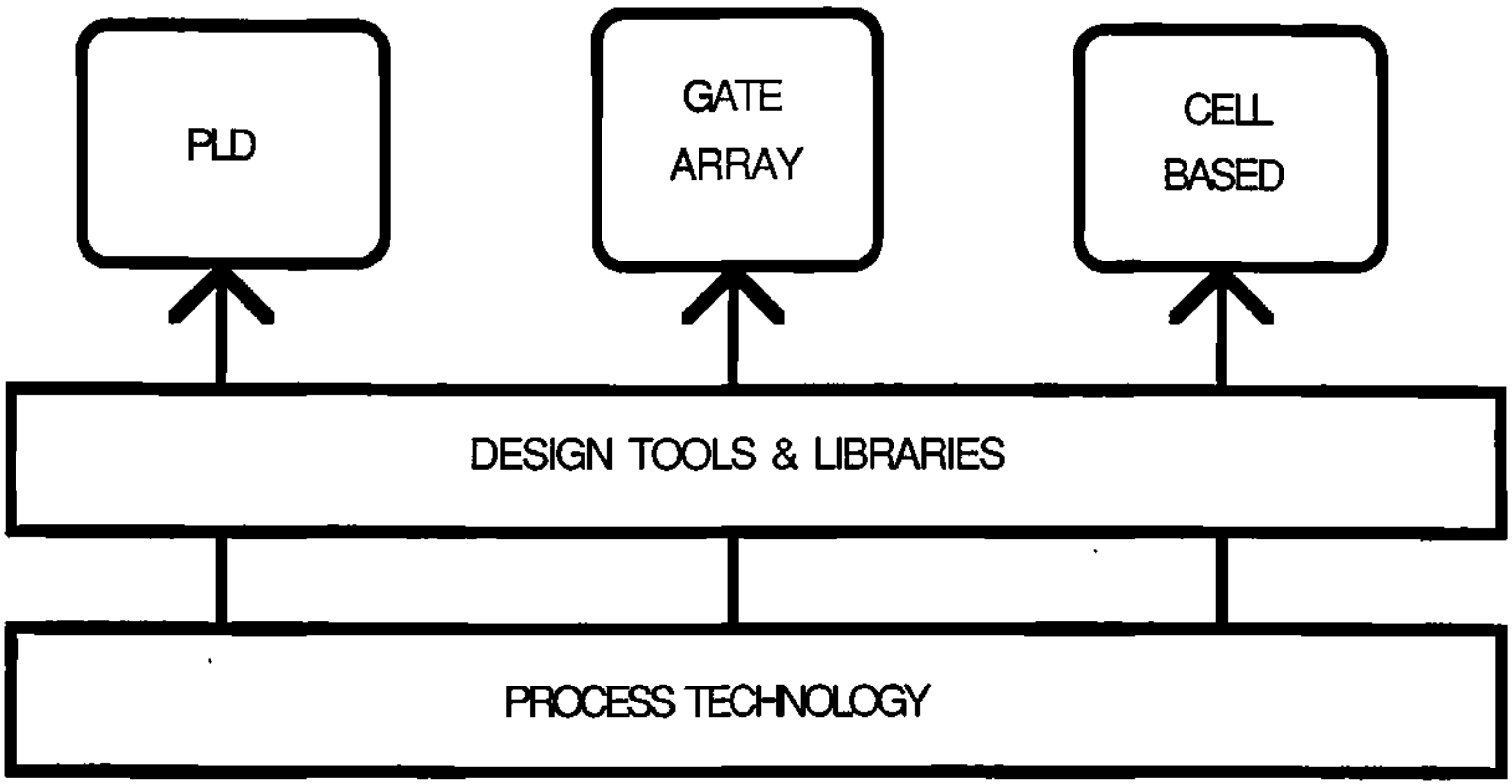
100% TEST FLOW FOR GAL16V8E

- TESTABILITY FAVORS E^2



VLSI TECHNOLOGY, INC.

A SPECTRUM OF ASIC PRODUCTS WITH COMMON DESIGN TOOLS AND TECHNOLOGY



VLSI TECHNOLOGY, INC.

TRENDS IN PLD ARCHITECTURE

- RAPID INCREASE IN HIGH-INTEGRATION ARCHITECTURES
  - MORE FLIP-FLOPS AND FLEXIBILITY
  - APPLICATION FOCUS
  - INCREASING PIN-COUNT

- CONTINUING VARIATIONS OF LOW INTEGRATION ARCHITECTURES

VLSI TECHNOLOGY, INC.

CONCLUSIONS

- E^2 WILL BE THE DOMINANT PLD TECHNOLOGY
- MANUFACTURERS SUPPLYING COMMON TOOLS/LIBRARIES FOR ALL ASIC PRODUCTS WILL HAVE AN ADVANTAGE
- THE APPLICATION OF CMOS TECHNOLOGY HAS USHERED IN A ERA OF EXPLOSIVE PLD MARKET GROWTH

VLSI TECHNOLOGY, INC.

Dataquest

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APPLICATION MARKETS FOCUS ON MICROPERIPHERALS FOR COMMUNICATIONS

An overview of electronic end
equipment with a focus on data communication

Wednesday, October 22, 9:45 a.m. to 12:00 noon

Dataquest's Semiconductor Application Markets service (SAM) believes that total U.S. end equipment will grow more slowly from 1986 through 1990 than it did during the previous five years. However, one area, data communication, is recognized as one of the fastest-growing end-equipment segments and as a new market opportunity for semiconductor manufacturers.

Within the data communication segment, the Integrated Service Digital Network (ISDN) is starting to make an impact. Dataquest expects ISDN to enhance data communication and spur general market growth. We expect some product dislocations as some present equipment functions are taken over by the ISDN network. We believe that ISDN offers unity to an evolving world of computing and communication technologies.

This focus session is composed of semiconductor suppliers, equipment suppliers, and Dataquest analysts. Each company has a unique perspective on the data communication environment. Speakers will present their views on the critical issues that are expected to impact the data communication segment and the ISDN marketplace.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
October 20-22, 1986
San Diego, California

1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 971-9000 Telex 171973 Fax (408) 971-9003

Larry Fullerton

Mr. Fullerton is a General Partner in Comm Group Consultants, and currently serves as a communication component consultant to Dataquest. Previously, he spent three years in advanced telecommunication component product marketing management at Intel. He was also responsible for defining third- and fourth-generation telecom components and generating tactical marketing plans and strategic, long-range product plans. Prior to that, he spent five years consulting in process control and EDP systems, fiber optics, and LANs. Mr. Fullerton received a B.S. degree in Electrical Engineering from Illinois Institute of Technology in Chicago.

Graham Alcott

Mr. Alcott is General Manager of the Telecom Operation at Intel Corporation. This operation is responsible for development and marketing of voice-to-digital conversion circuits, medium-speed modems, and ISDN products. His previous responsibilities during his 12 years with Intel cover manufacturing and marketing positions in support of Intel's microprocessor and microcontroller products. Mr. Alcott received a B.S. degree from Birmingham University in England, an M.S. degree from San Jose State University, and an M.B.A. degree from Santa Clara University.

Lynn E. Ditty

Mr. Ditty is Marketing Manager for Communications ICs at AT&T Technology Systems in Allentown, Pennsylvania. His organization is responsible for product marketing, support, and management of AT&T's line of Catalog Communications Devices. Previously, he has held a variety of engineering and marketing positions at AT&T-TS and AT&T Bell Laboratories in both the transmission equipment division and device division. Mr. Ditty received a B.S. degree in Electrical Engineering from Pennsylvania State University and an M.S. degree in Electrical Engineering at Polytechnic Institute of New York.

Ron Ruebusch

Mr. Ruebusch is Director of Strategic Marketing in the Communications Products Division at Advanced Micro Devices (AMD). His major areas of responsibility include ISDN, analog loop voice products, and data communication products. Before joining AMD, Mr. Ruebusch was a Product Marketing Manager for communications products at Signetics. Prior to Signetics, Mr. Ruebusch worked at Farinon Electric in various marketing and design engineering roles. Mr. Ruebusch received bachelor's and master's degrees in Electrical Engineering and an M.B.A. degree, all from the University of Santa Clara.

APPLICATION MARKET FOCUS: INTRODUCTION TO MICROPERIPHERALS FOR COMMUNICATION

Anthea C. Stratigos
Product Manager
and Industry Analyst
Semiconductor Application
Markets
Dataquest Incorporated

Ms. Stratigos is Product Manager for Dataquest's Semiconductor Application Markets service. She is responsible for managing research on semiconductor consumption based on an end-market segmentation. Primary analysis in this area includes forecasting electronic equipment production, monitoring semiconductor users' electronic equipment revenue, tracking user merchant market semiconductor consumption, analyzing semiconductor company merchant shipments by end market, and examining the semiconductor content of individual types of electronic equipment. Prior to joining Dataquest, Ms. Stratigos worked in Information Development at IBM Corporation's Santa Teresa Laboratory, where she documented software products developed for IBM's mainframe systems. Ms. Stratigos received a B.A. degree in Communication from Stanford University.

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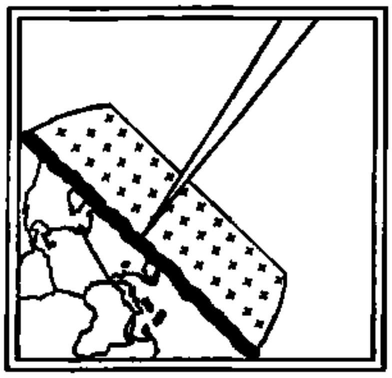

Recovery: Managing the New Industry Structure

APPLICATION MARKETS FOCUS: INTRODUCTION TO MICROPERIPHERALS FOR COMMUNICATION

ANTHEA C. STRATIGOS

Product Manager
Semiconductor Application Markets
Dataquest Incorporated

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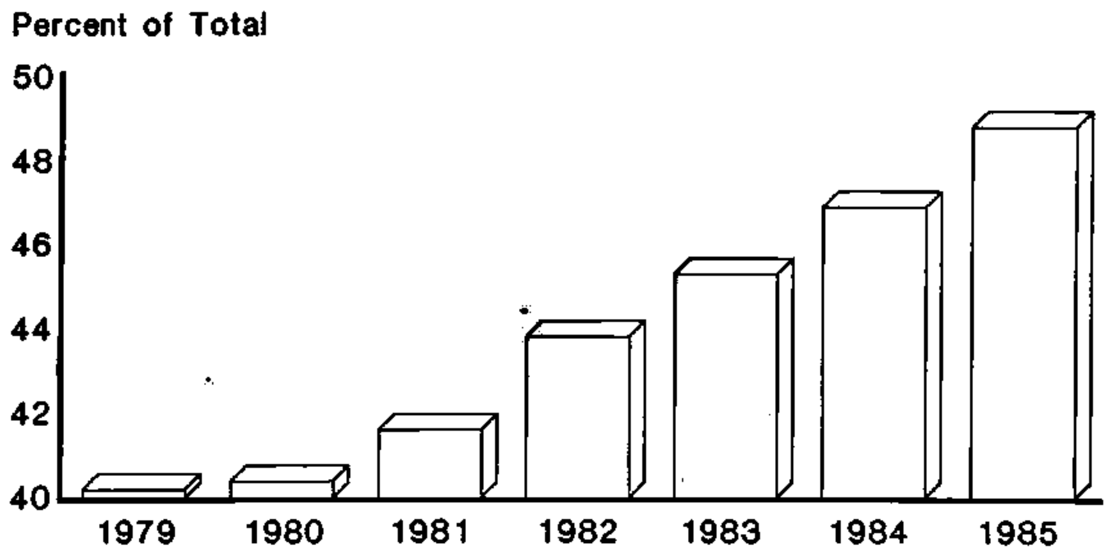
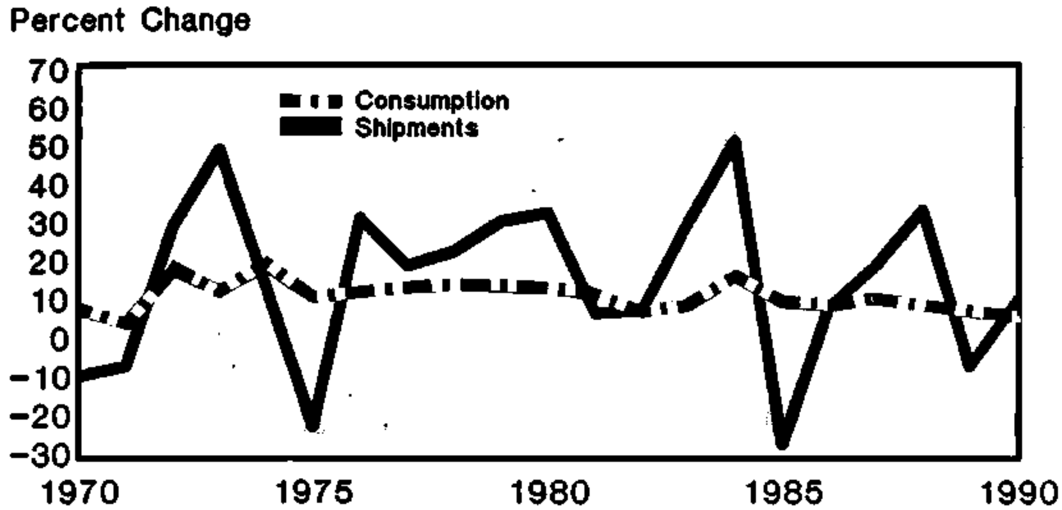
NORTH AMERICAN COMPANY TOTAL REVENUE VS. ELECTRONIC EQUIPMENT REVENUE



Source: Dataquest

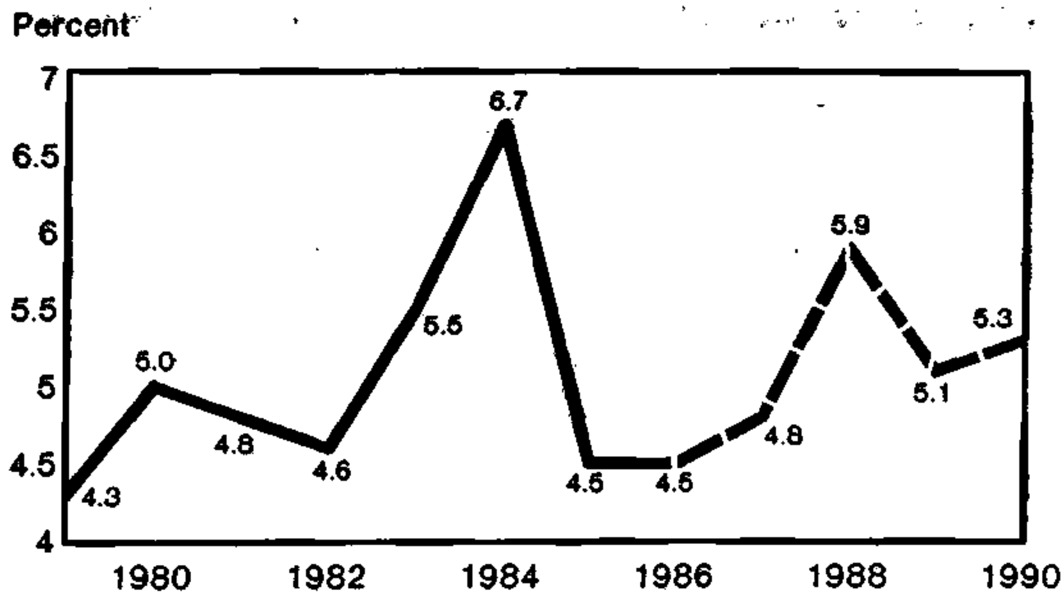
SEMICONDUCTOR CONSUMPTION VS. ELECTRONIC EQUIPMENT SHIPMENTS

North America



Source: Dataquest

A LONG LOOK AT INPUT-OUTPUT RATIOS



Source: Dataquest

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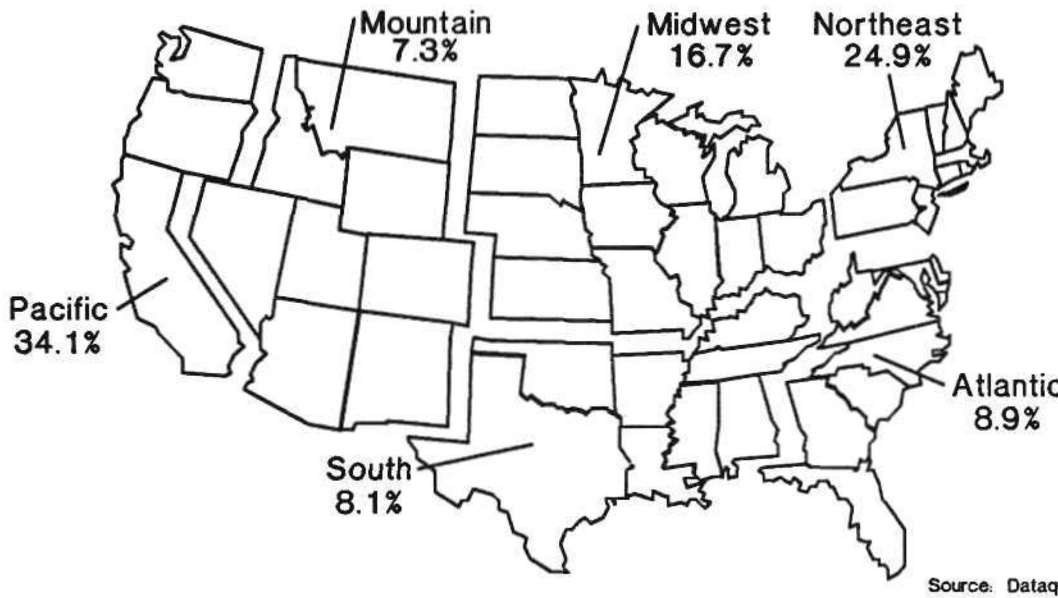
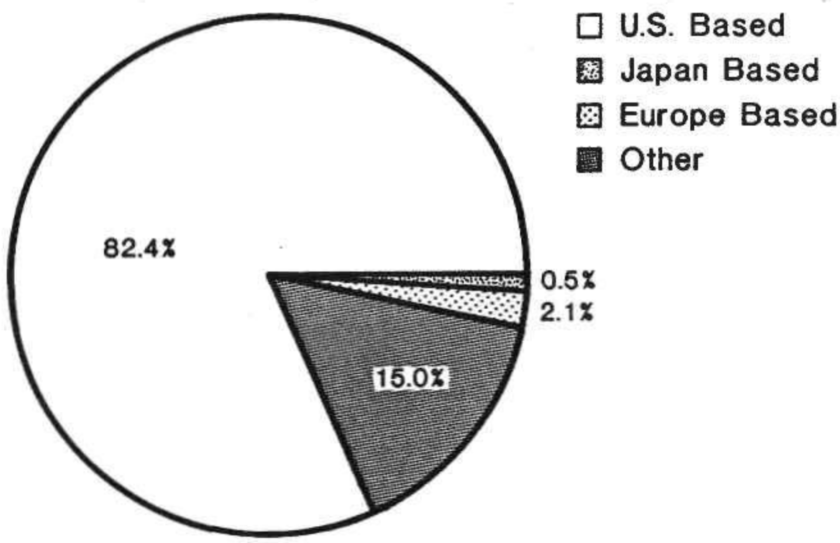
ANNUAL SURVEY
PROCUREMENT LOCATIONS - *ELECTRONIC BUSINESS* 200



Source: Dataquest

REGIONAL SUPPLIER BASE



Source: Dataquest

DISTRIBUTION PURCHASES

Average Percent of Total

Total	13.0%

Purchases by Application Market

Data Processing	10.7%
Communications	8.9%
Industrial	28.2%
Consumer	12.8%
Military	24.8%
Transportation	0.0%

Source: Dataquest

SEMICONDUCTORS PURCHASED OFFSHORE FOR U.S.-BASED EQUIPMENT PRODUCTION

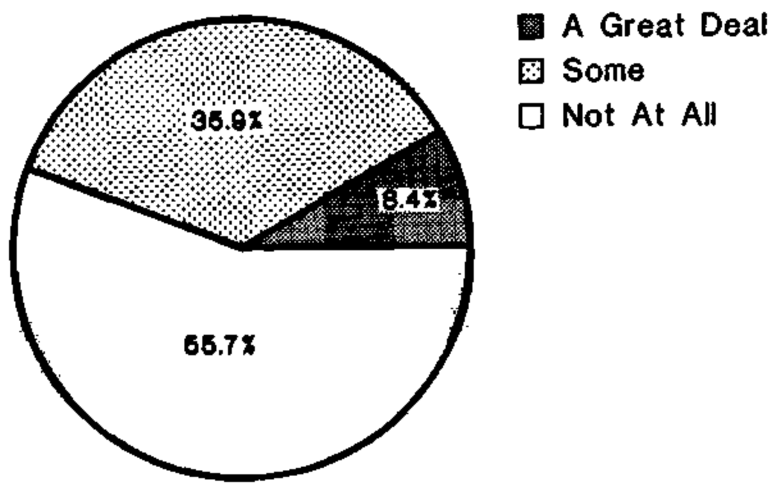
Average Percent of Total

Data Processing	24.8%
Communications	22.0%
Industrial	10.8%
Consumer	45.8%
Military	23.7%
Transportation	29.7%

Source: Dataquest

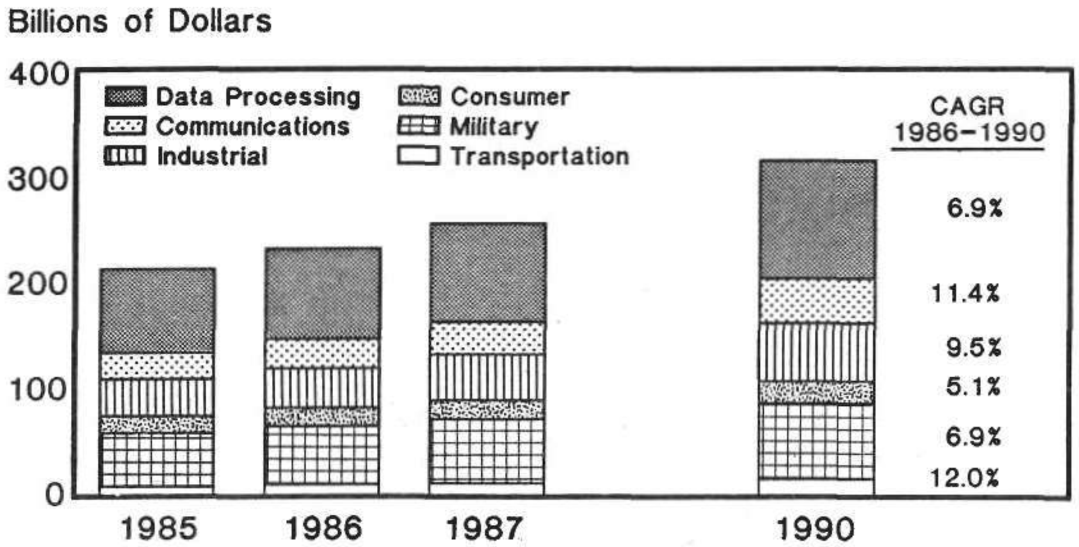
ANTICIPATED SHIFT TO OFFSHORE PRODUCTION

Percent of Total



Source: Dataquest

ESTIMATED NORTH AMERICAN ELECTRONIC EQUIPMENT



Source: Dataquest

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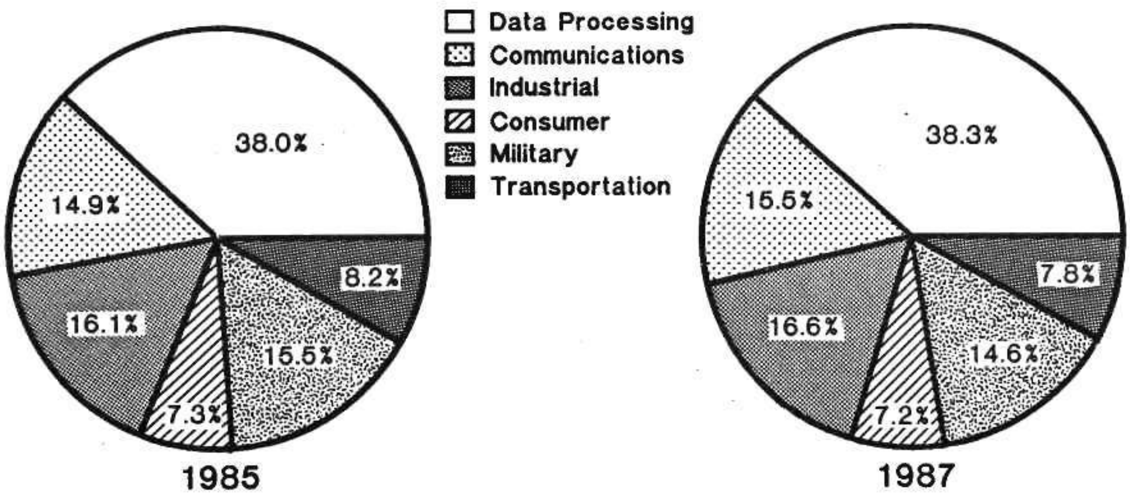
ESTIMATED NORTH AMERICAN SEMICONDUCTOR CONSUMPTION BY APPLICATION MARKET

Percent of Total Dollars



Source: Dataquest

DATAQUEST'S FASTEST-GROWING ELECTRONIC EQUIPMENT MARKETS

Millions of Dollars

	Equipment Type	Estimated Equipment CAGR 1986-1990	Estimated 1986 Equipment Revenue	Estimated 1986 Semiconductor Consumption
1.	Voice Messaging	39.9%	$ 260	$ 13
2.	Integrated Voice/ Data Workstations	38.5%	$ 321	$ 40
3.	Nonimpact Serial Printers	32.6%	$ 968	$ 46
4.	T-1 Multiplexers	29.1%	$ 262	$ 14
5.	Modems	26.2%	$1,288	$120

(Continued)

DATAQUEST'S FASTEST-GROWING ELECTRONIC EQUIPMENT MARKETS

Millions of Dollars

	Equipment Type	Estimated Equipment CAGR 1986–1990	Estimated 1986 Equipment Revenue	Estimated 1986 Semiconductor Consumption
6.	Single-Use Enhanced Computer Systems	24.3%	$ 903	$53
7.	Graphics Terminals	22.8%	$1,000	$68
8.	Private Packet Data Networks	21.7%	$ 279	$16
9.	Cellular Radio/ Telephone	21.6%	$ 670	$33
10.	Robot Systems	20.5%	$ 772	$24

Source: Dataquest

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TOP TELECOMMUNICATIONS SEMICONDUCTOR MARKETS

Millions of Dollars

	Equipment Type	1986 Semiconductor Consumption
1.	PBX	$252.9
2.	Key Telephone Systems	$180.7
3.	Modems	$120.3
4.	Central Office Switching Equipment	$ 98.0
5.	Transmission Carrier Systems	$ 75.3
6.	Local Area Networks	$ 62.0
7.	Transmission Multiplex Equipment	$ 45.1
8.	Integrated Voice/Data Workstations	$ 39.6
9.	Cellular Radio/Telephone	$ 32.7
10.	Centrex	$ 31.2

Source: Dataquest

TOP 10 COMMUNICATIONS EQUIPMENT MANUFACTURERS

Based on Electronic Revenues

AT&T	M/A-Com
GTE	Motorola
Harris	Northern Telecom
IBM	RCA
ITT	Rockwell

Source: Dataquest

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The Dun & Bradstreet Corporation

MICROPERIPHERALS FOR COMMUNICATION: TRENDS AND ISSUES

Janet M. Oncel
Industry Analyst
Semiconductor Industry
Service
Dataquest Incorporated

Ms. Oncel is an Industry Analyst for Dataquest's Semiconductor Industry Service. She is responsible for conducting worldwide semiconductor research on microprocessors, microperipherals, and microcontrollers. Prior to joining Dataquest, Ms. Oncel worked as a Product Planner for Intel Corporation, where she followed memory production from the design stage to customer delivery. Ms. Oncel received a B.S. degree in Marketing from San Jose State University.

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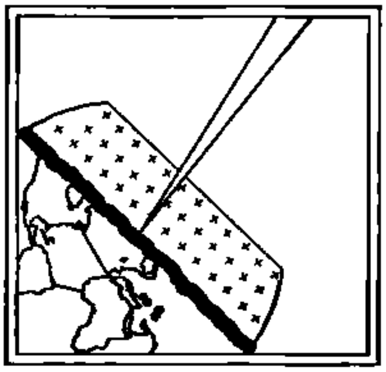

Recovery: Managing the New Industry Structure

APPLICATION MARKETS FOCUS: MICROPERIPHERALS FOR COMMUNICATION

JANET ONCEL

Industry Analyst
Semiconductor Industry Service
Dataquest Incorporated

WHY FOCUS ON DATA COMMUNICATION?

- Fastest-growing end-equipment segment from 1985 through 1990
- New market opportunity for semiconductor manufacturers
- Alliances and standards are evolving

DATA COMMUNICATION FOCUS

- Modems
- LANs
- ISDN

SESSION SPEAKERS

Janet Oncel	Dataquest
Larry Fullerton	Consultant

SESSION SPEAKERS

Janet Oncel	Dataquest
Larry Fullerton	Consultant
Graham Alcott	Intel

SESSION SPEAKERS

Janet Oncel	Dataquest
Larry Fullerton	Consultant
Graham Alcott	Intel
Lynn Ditty	AT&T

SESSION SPEAKERS

Janet Oncel	Dataquest
Larry Fullerton	Consultant
Graham Alcott	Intel
Lynn Ditty	AT&T
Ron Ruebusch	AMD

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ISDN OVERVIEW

Lawrence M. Fullerton
Partner
CGC

ISDN PRODUCT TRENDS

Subscriber Side

- o CMOS
- o 4W/I.430, pt. to pt. and multi drop support
- o 2B + D Service
  - B1/Voice
  - B2/Data
  - D/Signalling
- o HDLC on board transceiver/LAP D for D channel
- o Local mC direct support for call set up/tear down as well as local intelligence.
- o Integration of combo functions in future
- o Power converter availability
- o High density packaging
- o Parallel programming approach, as well as serial

Line Card Side

- o 4W/I.430
- o 2B + D Service
- o CMOS
- o HDLC separate or integrated for signalling flexibility
- o Power controller/transceiver match
- o Serial programming approach
- o High density packaging

EQUIPMENT MANUFACTURERS
ISDN NEEDS

CMOS

- o Low power
- o Standby

System solution costs kept to minimum + $5.00/VLSI analog target

Line card design flexibility

- o Call set up/tear down
  - Local
  - Central
- o D channel packetized data system support

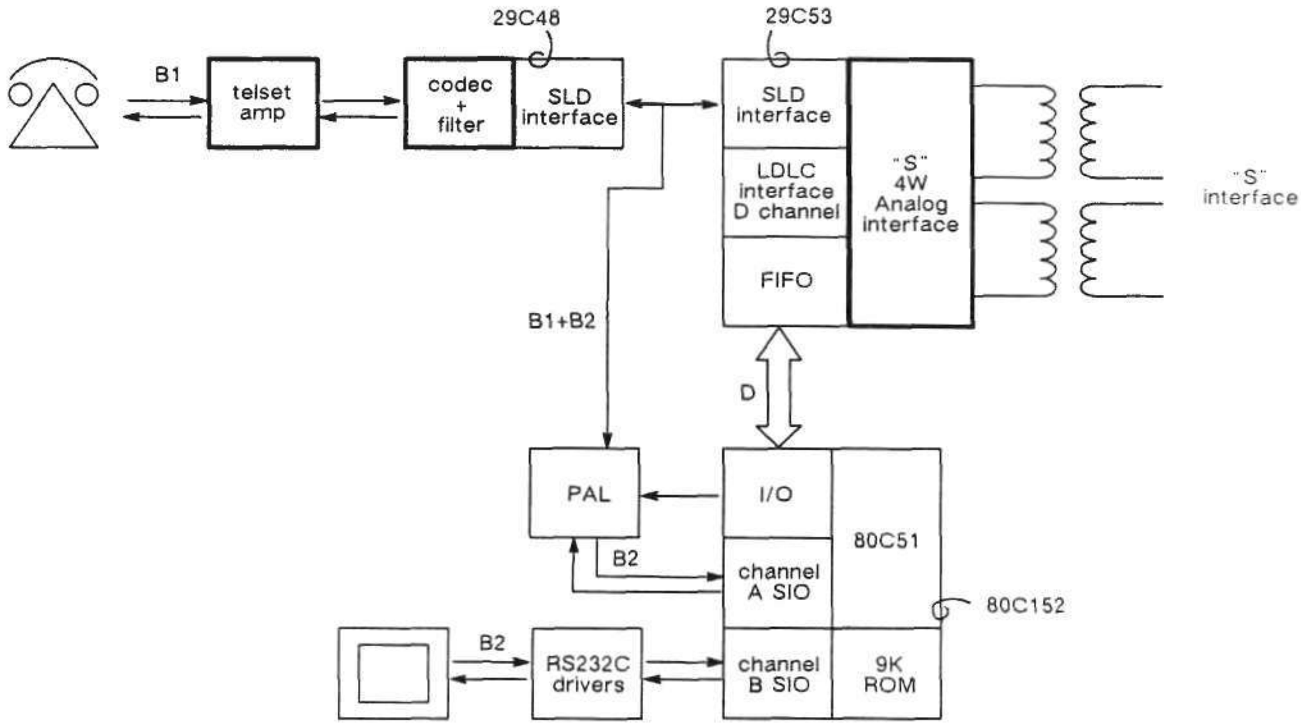
Digital Subscriber

- o Dual channel HDLC/mC or mP
  - D channel
  - B channel/DMI
- o Expandable HDLC private buffer
- o HDLC LAP D software support
- o Total power consumption <450 mw target

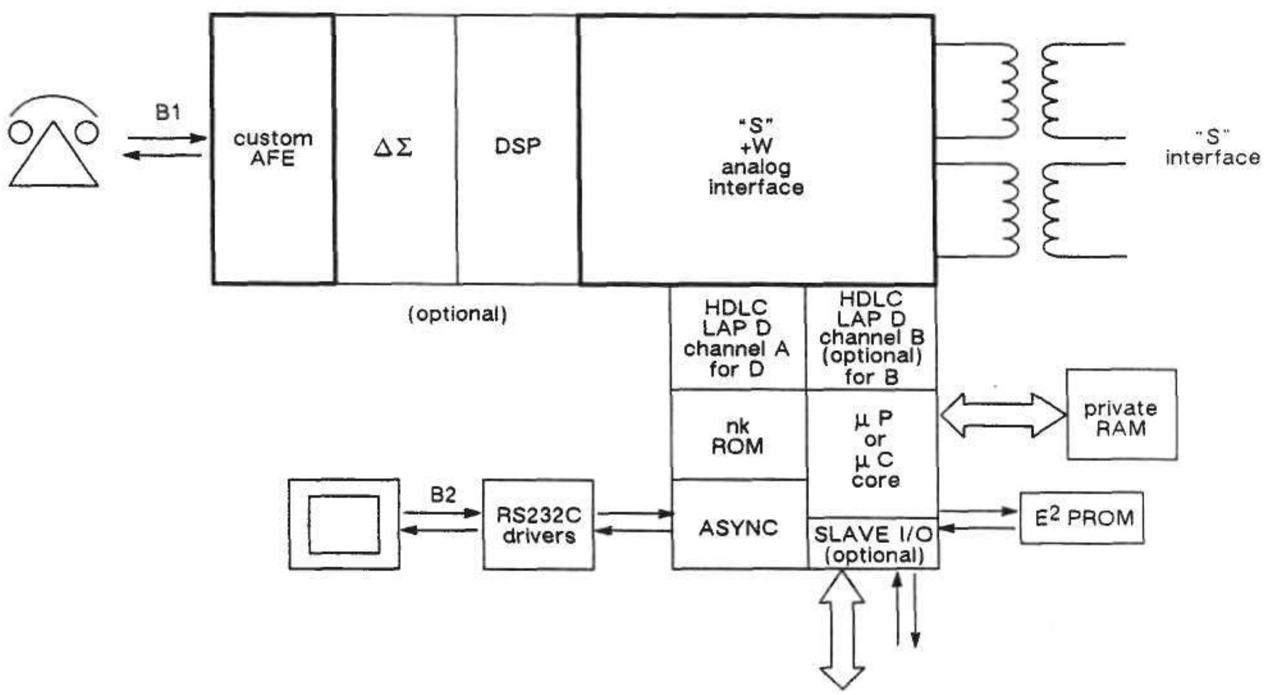
  Combo
  mC or mP
  Transceiver
  Serial I/O
- o Need to power phone with local power removed

Testability

STANDARD



ASIC



CGC

ISDN "S"
TECHNOLOGY IMPACT

Technology	Speed	Next 4 Years	5 -> 10 Years
Modems/Home	< 2.4 kbps	-	+/-
Modems/Office	<19.2 kbps	+	++
DDS	<56 kbps	+	++
ISDN	<64 kbps		
Primary Access	<2.048 mbps	-	-
LAN's	<10 mbps	-	-
Fiber Optics	?	--	--

- not affected by 4W/"S" ISDN
+ affected by 4W/"S" ISDN / 4W will gain ground

ISDN "U"
TECHNOLOGY COMPETITORS

Technology	Next 5 Years	6 -> 15 Years
Modems/Home	++	++
Modems/Office	+	+/-
DDS	+	-
Primary Access	++	+
LAN's	-	-
Fiber Optics	-	++

- Not competitor
+ Competitor

T1D1.3
STATUS

Progress to date

- 2W
- Echo Cancellation
- 2B + D
- Maintenance Channel
- * 2B1Q Transmission Encoding
- Data Scrambling/Descrambling

Open Issues

- Final Bit Rate
- Framing Format
- Receiver Synchronization
- Line Code/Super Frame
- Maintenance Bandwidth/Protocol
- Loop Acquisition Algorithm
- Data Scrambling/Descrambling Algorithm

* Recent, significant development

AMD'S ISDN

Part Number	Product Type	Samples	Fully Functional	Production
79C30	Subscriber side I.430 "S" 4W transceiver + DSP combo + HDLC	Rev 2 Now	100%	1Q87
79C32	Subscriber side I.430 "S" 4W transceiver + HDLC	Rev 2 Now	100%	1Q87
79C31	Line Card side I.430 "S" 4W transceiver + HDLC	Rev 1 Now	100%	1Q87
79C312	Line Card side I4.30 "S" 4W transceiver	Rev 1 Now	100%	1Q87
79C36	Subscriber side power Controller	-	100%	Now
79C38	Line card side power Controller	1/87	--	2Q87
79C33/ TEC	2B + D echo cancelling Biphase 2W Transceiver	3Q87	--	1Q88

Development Support:

- o Evaluation board/Multibus based
- o Evaluation board/PC based
- o Board supports subscribe and line card side development

Future:

- o 2B1Q/T1D1.3 US "U" 2W transceiver
- o 4B3T/European "U" 2W transceiver*
- o HDLC LAP D protocol controller

* Assumes 4B3T does not change to 2B1Q

AT&T's ISDN

Part Number	Product Type	Samples	Fully Functional	Production
T7250A	Subscriber and line card I.430 4W "S" transceiver + HDLC/D channel + timer	Now	100%	1Q87
	Improved register set + CCITT modification	1Q87		2Q87
T7111	HDLC controller/B channel	Now	99%	1Q87

Development Support:

- o Tutor board/1Q87

Future:

- o 2B1Q/T1D1.3 US "U" 2W transceiver

INTEL's ISDN

Part Number	Product Type	Samples	Fully Functional	Production
29C53	Subscriber and line card side I.430 4W transceiver + HDLC	Now	95%	3/87
HDLC LAP B + LAP D	80188 based D channel signalling software, layers 1, 2 and 3	--	--	1/87

Development Support:

- o LEK/line side evaluation card
- o TEK/terminal side evaluation card
- o App notes

Future:

- o IPC/80C51 based mC + 2 HDLC LAP B + LAP D channels

MITEL'S ISDN

Part Number	Product Type	Sample	Fully Functional	Production
MT8930	Subscriber, line card, and NT1 I.430 "S" transceiver + HDLC/D	12/86	--	2Q87
MT8952	HDLC controller/ B channel + C channel access	--	100%	Now
MT8972	2W echo cancellation, 2B + 1D transceiver Maintenance/Overhead (biphase)	--	100%	Now

Development Support:

- o DNIC evaluation board/MT8972, standalone or Apple interface

Future:

- o 2B1Q/T1D1.3 US "U" 2W transceiver
- o SNIC evaluation board/MT8930, IBM PC based
- o MT8930, MT8952, MT8972, MT8994 ISDN evaluation board + crosspoint switch, IBM PC based

MOTOROLA's ISDN

Part Number	Product Type	Samples	Fully Functional	Production
MC145426	UDLT I, subscriber side, TCM 1B + 1D 2W transceiver	--	--	Now
MC145422	UDLT I, line card side, TCM 1B + 1D 2W transceiver	--	--	Now
MC145425	UDLT II, subscibe side, TCM 2B + 2D 2W transceiver	Now	100%	1Q87
MC145421	UDLT II, line card side, TCM 2B + 2D 2W transceiver	Now	100%	1Q87
MC145474	Line card and subscriber, I.430 "S" 4W transceiver (IDL based)	12/86	--	4Q87
MC145488	2 channel, HDLC LAP D controller	3Q87	--	4Q87

Future:

- o Evaluation board
- o HDLC LAP D software support
- o 2B1Q/T1D1.3 US "U" 2W transceiver

NATIONAL's ISDN

Part Number	Product Type	Samples	Fully Functional	Production
TP3400	Subscriber and line card side 2W, TCM based, 2B + D transceiver	1Q87	--	2Q87
TP3420	Subscriber and line card side I.430 4W "5" transeiver	1Q87	--	2Q87
TP3421	Subscriber and line card side I.430 4W "5" transceiver + multiframing	1Q87	--	2Q87
HPC16400	16 bit HDLC controller, 2 channels	1Q87	--	2Q87

Future:

- o TP3410 2B1Q/T1D1.3 US "U" 2W transceiver
- o 4B3T/European "U" 2W transceiver*

* Assumes 4B3T does not change to 2B1Q

SIEMEN's ISDN

Part Number	Product Type	Samples	Fully Functional	Production
PEB2070	HDLC controller, D channel	A3/Now	100%	10/86
PEB2080	Subscriber and line card I.430 4W "S" transceiver (CCITT multiframe bit addition)	A4/Now	100%	2Q87
SAB82520	HDLC controller, 2 channels	A2/Now	100%	10/86
PEB2085	Subscriber and line card I.430 4W "S" transceiver + HDLC	1/87	--	3Q87
PEB2095	Subscriber and line card TCM, 2W 2B+D transceiver	1/87	--	--

Development Support:

- 80188 based, IBM PC compatible 4W "S" transceiver board (3rd party)
- HDLC LAP D level 2 + 3 available (3rd party)
- STU2000 evaluation board

Future:

- PEB2090/4B3T/European "U" 2W transceiver
- 2B1Q/T1D1.3 US "U" 2W transceiver
- Power controller/PEB 2020
- Subscriber and line card TCM, 2W 2B+D transceiver + HDLC/PEB 20950

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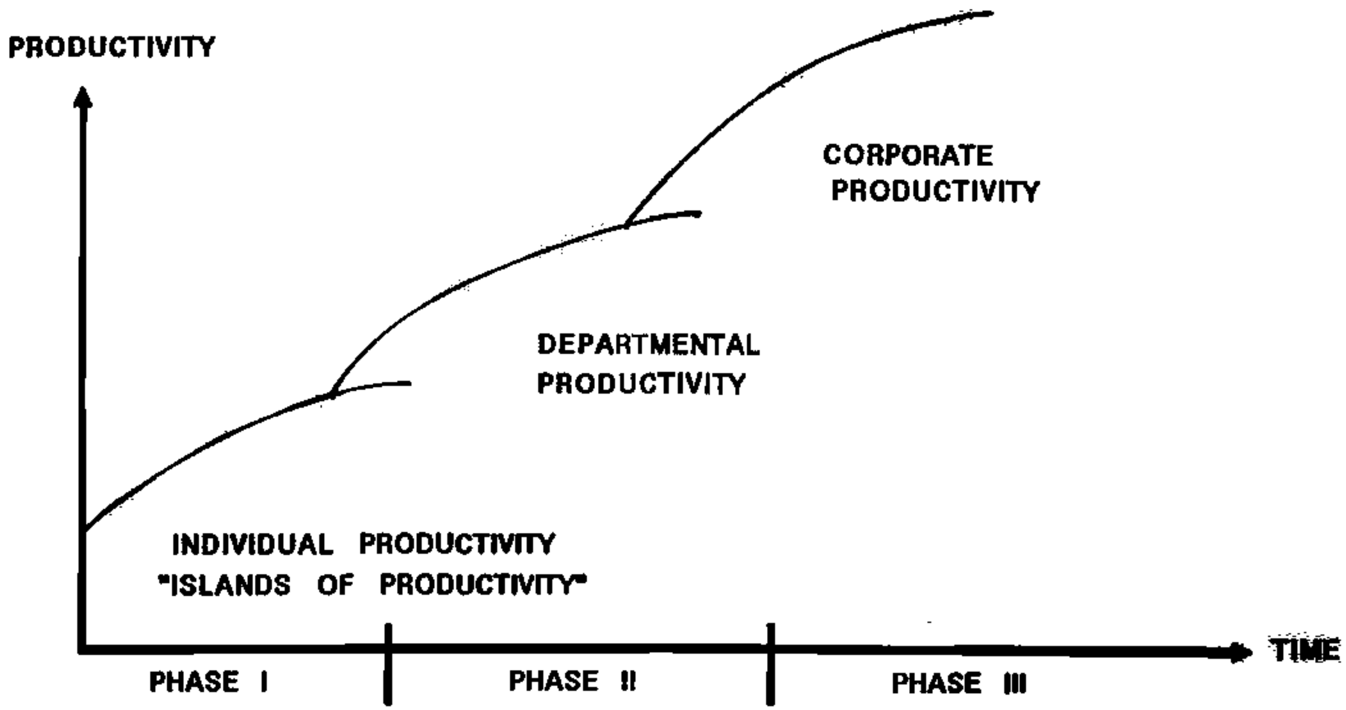
MICROCOMMUNICATIONS:

THE NEXT PRODUCTIVITY BREAKTHROUGH
A MAJOR MARKET EMERGES

GRAHAM ALCOTT

INTEL CORPORATION

PRODUCTIVITY NEEDS

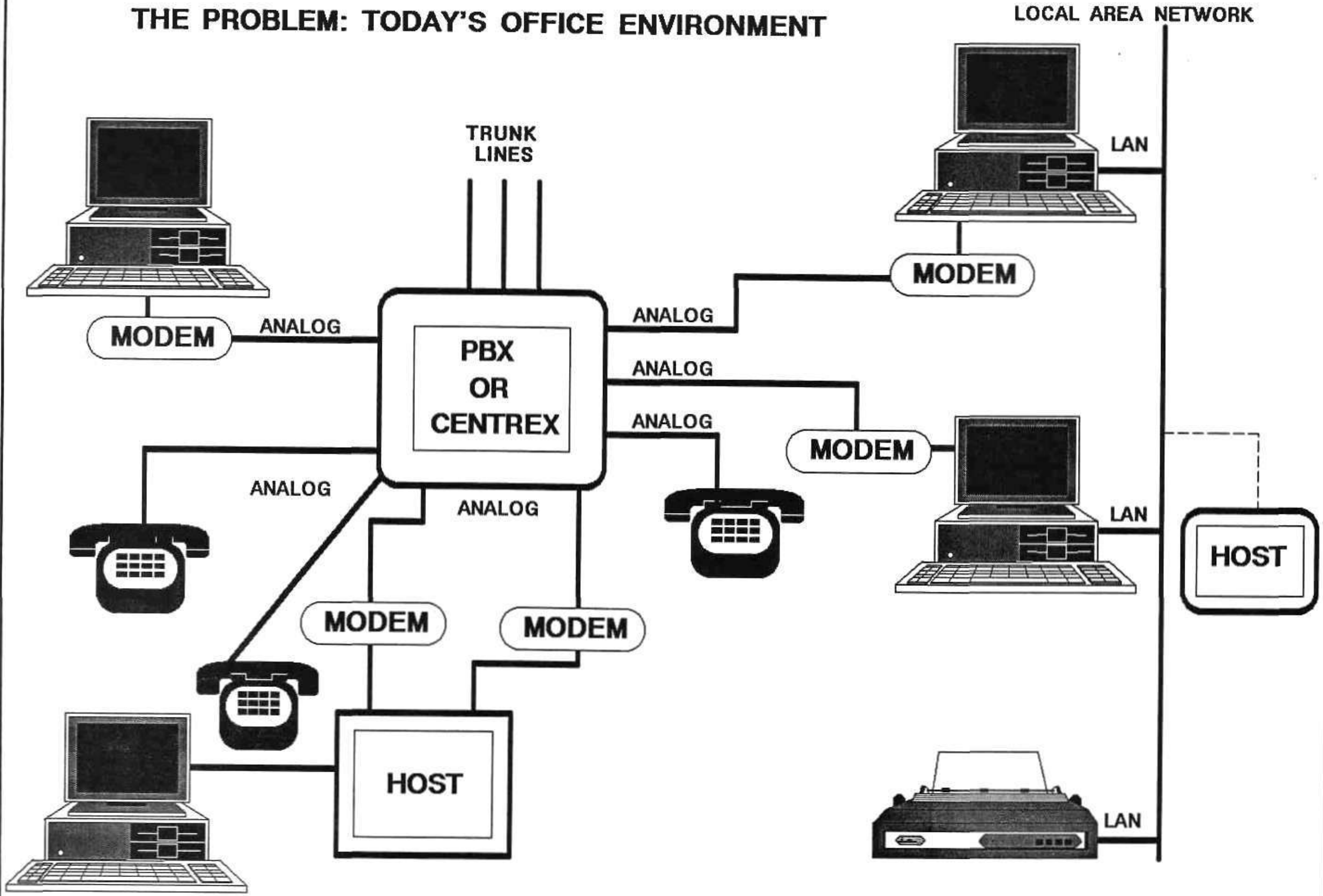


PHASE I – INDIVIDUAL MINICOMPUTERS, WORKSTATIONS

PHASE II – LAN CLUSTERS AND MODEMS

PHASE III – LAN AND ISDN INTER–NETWORKING

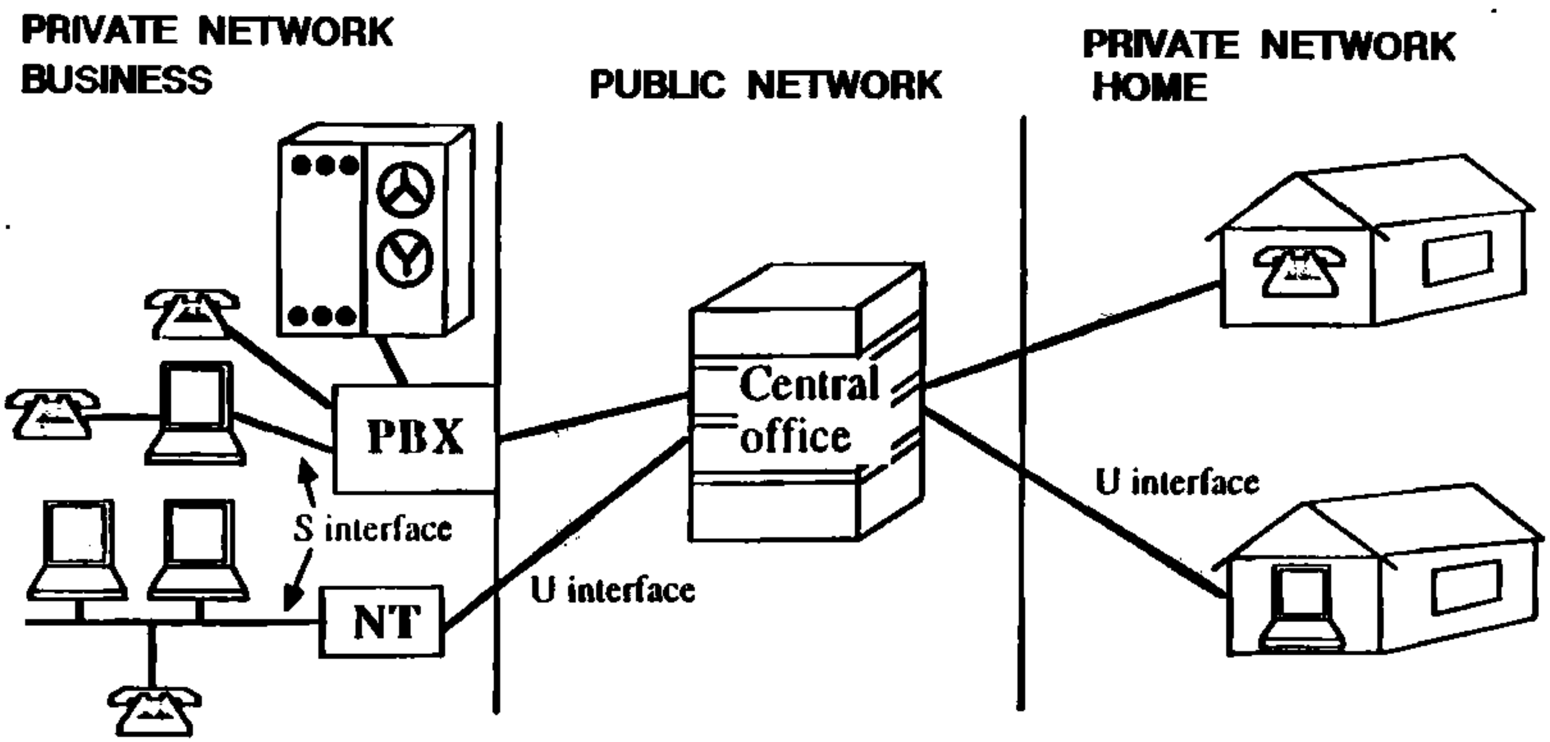
THE PROBLEM: TODAY'S OFFICE ENVIRONMENT



TRENDS IN COST EFFECTIVE MODEM TECHNOLOGY

CURRENT	1200 BPS (212A/V.22)
NEXT 5 YEARS	2400 BPS (V.22 BIS)
FUTURE	9600 BPS (V.32) ?

EVOLVING ISDN NETWORK



- O ADEQUATELY DEFINED CCITT STANDARDS TO ALLOW IMPLEMENTATION
- O T1 COMMITTEE PURSUING STANDARDS COMPLETION
- O LACK OF 'U' INTERFACE SPEC WILL NOT HOLD UP IMPLEMENTATION

ISDN: THE INTEGRATING FACTOR

- O USES THE $500 BILLION INSTALLED TELECOM BASE
- O PROVIDES UNIVERSAL CONNECTIVITY

intel

ISDN AND THE ISO – OSI MODEL

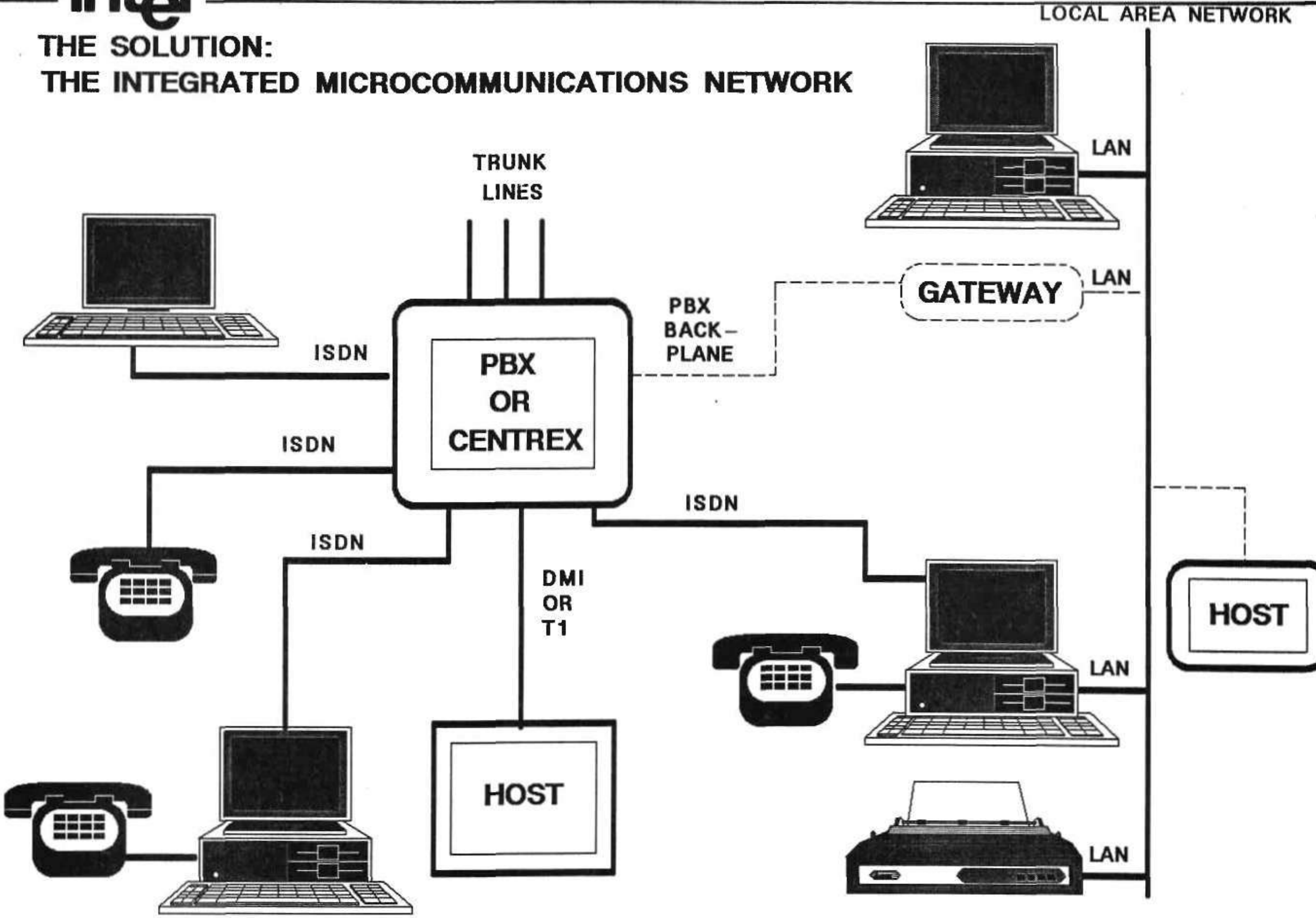
ISO–OSI MODEL	B–CHANNEL	D–CHANNEL	OPENNET/ MAP	OPENNET/ ETHERNET
APPLICATION	NOT SPECIFIED	NOT SPECIFIED	FTAM	NFA
PRESENTATION			MMFS	NFA
SESSION			ISO SESSION	NFA
TRANSPORT			ISO TRANSPORT	ISO TRANSPORT
NETWORK		I–451	ISO NETWORK	ISO NETWORK
LINK		I–441	TOKEN BUS BROADBAND AND BASEBAND	ETHERNET
PHYSICAL	I–430	I–430		ETHERNET

B–CHANNEL / D–CHANNEL: CCITT "S" INTERFACE

MICROCOMMUNICATIONS

intel

THE SOLUTION:
THE INTEGRATED MICROCOMMUNICATIONS NETWORK



- O LANS MACHINE-TO-MACHINE COMMUNICATIONS
- O ISDN - HUMAN-INTERACTING COMMUNICATIONS

ISDN: THE COMMERCIAL SOLUTION

PERFORMANCE	LOW (COST)	HIGH (COST)
HIGH 64000 BPS	ISDN	ANALOG WITH LEASED LINES
LOW 1200 BPS	ANALOG WITH MODEM	N.A.

COST

INTEGRATED VOICE DATA TERMINAL (IVDT)

ISDN S/T TRANSCEIVER 29C53 + VOICE CONVERSION COMBO 29C48 + MICROCOMPUTING 80188 & 82530 = PC CARD

PC CARD +

+

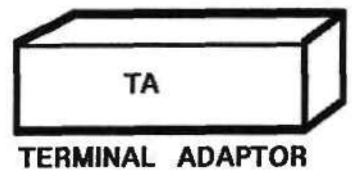
= IVDT

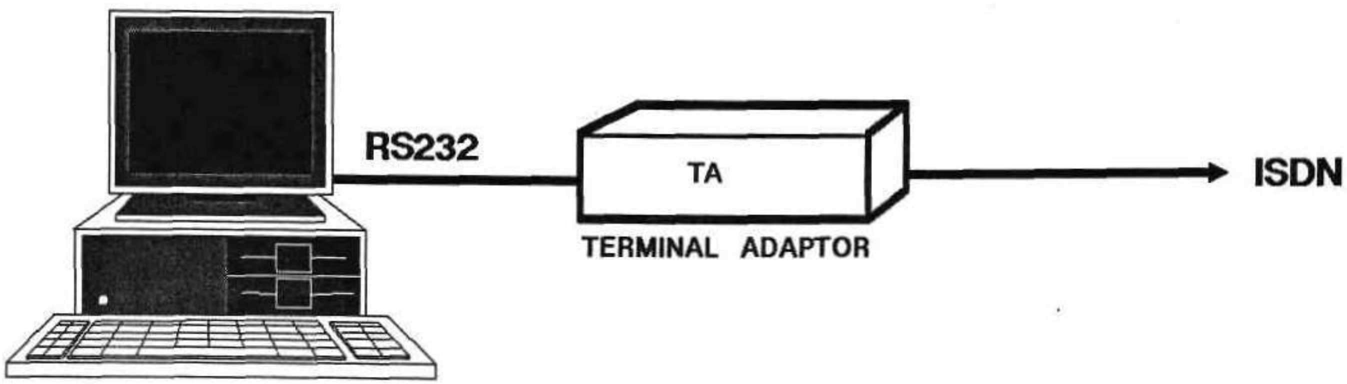
PC UPGRADE TO AN ISDN VOICE AND DATA TERMINAL

PROTECTING THE 16M EXISTING PC INVESTMENT

PIPELINE TO ISDN

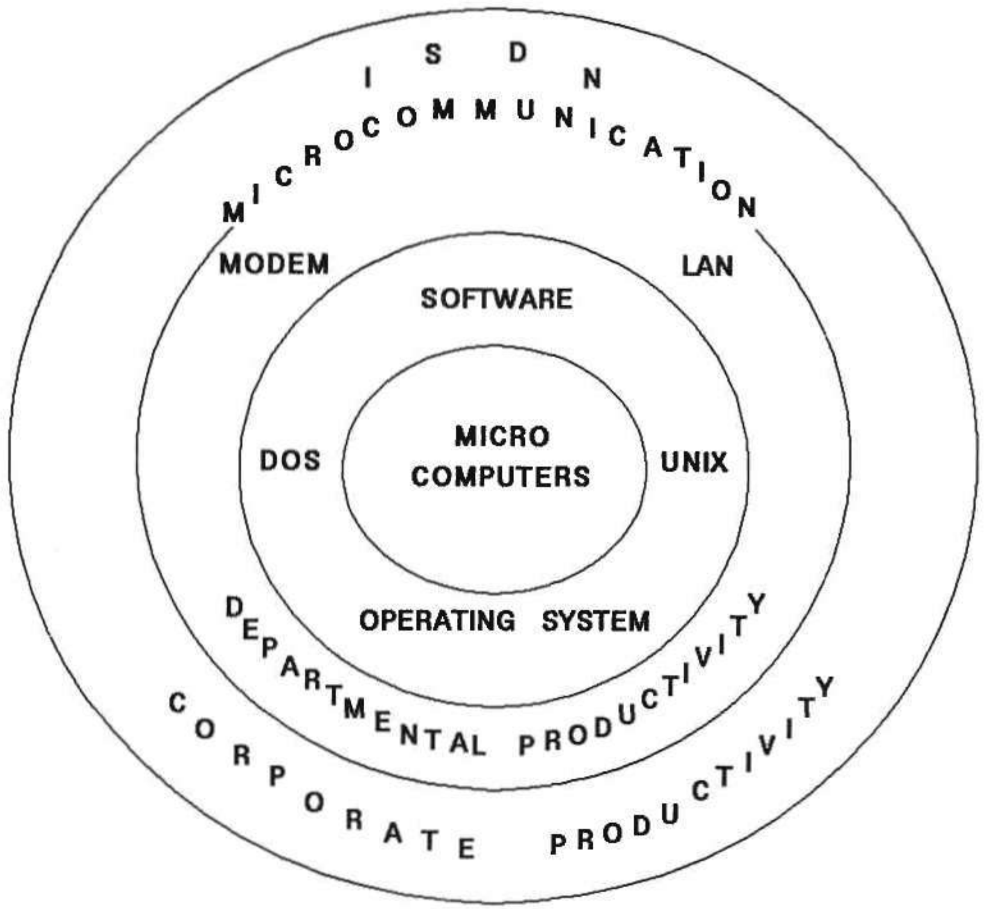
ISDN S/T TRANSCEIVER 29C53 + ISDN PROTOCOL CONTROLLER IPC =





LOW COST ISDN ACCESS FOR ANY TERMINAL

ISDN: THE NEXT PRODUCTIVITY BREAKTHROUGH



AN AT&T-TECHNOLOGIES PERSPECTIVE ON ISDN

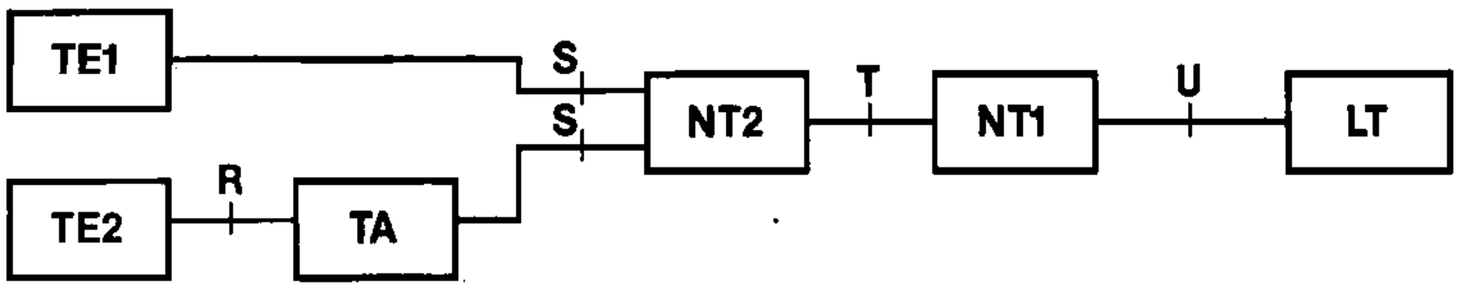
I. Industry Directions and Trends

II. AT&T View and Directions

III. Silicon Prospects

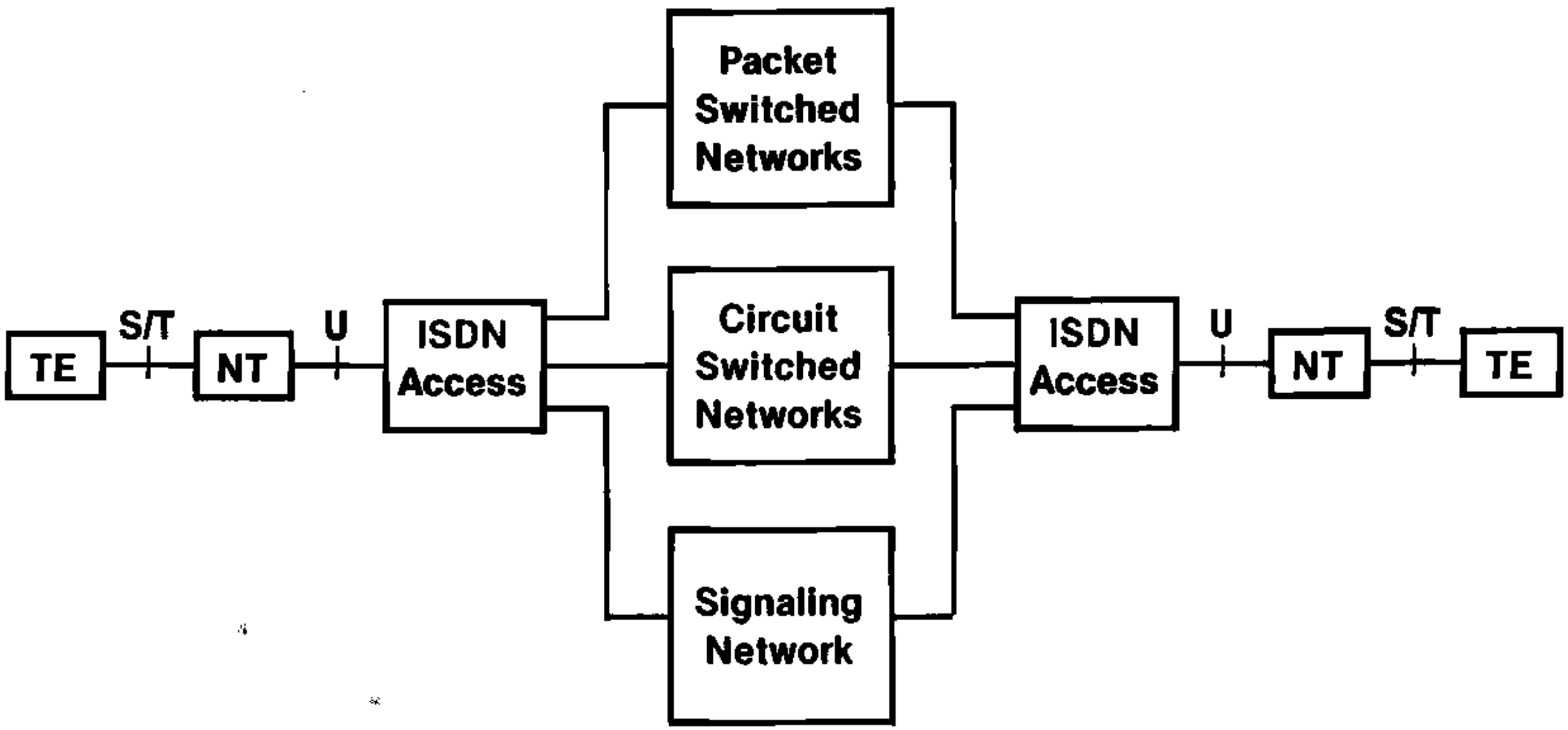
Lynn E. Ditty
Product Manager, Communications Devices
AT&T-TS
Allentown, Pa.

ISDN REFERENCE POINTS AND FUNCTIONAL GROUPINGS



TE1 — Terminal Equipment 1
TE2 — Terminal Equipment 2
TA — Terminal Adapter
NT1 — Network Termination 1
NT2 — Network Termination 2
LT — Line Termination

ISDN NETWORK VISION



ISDN : PRESENT (1986-1988)

- U-Interface basic access field trial support and evaluation
- Pre-standard primary access products primarily serving computer-to-PBX links (DMI)
- Underlying connectivity issues resolved
- Commercial availability and manufacture of a limited number of S or T products
- Terminal adapter market begins to grow

ISDN : SHORT TERM (1989—1993)

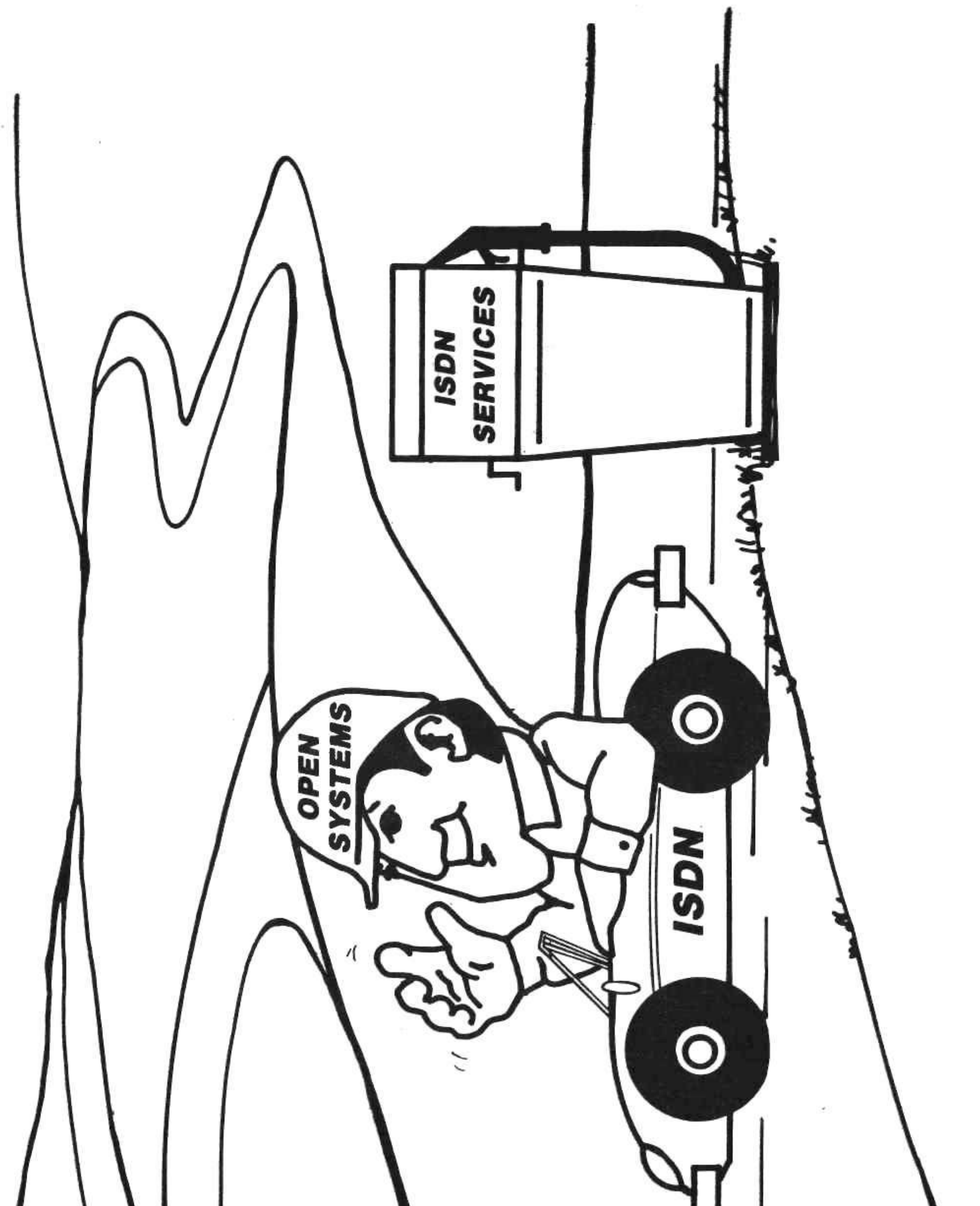
- Commercial availability and manufacture of standard basic and primary U equipment
- ISDN Centrex applications begin to grow
- Variety of S or T terminals are available to interconnect to the network or to PBXs
- Variety of TAs are in production but some are being replaced
- Growth of services

ISDN : LONG TERM (1994—   )

- A wide variety of CPE products are available
- Residence market will begin to grow
- Rapid growth of basic and primary access into "Centrex" environment
- Variety of new services available
- Higher bandwidth channel market will develop
- Multiple uses of existing bandwidth

AT&T PERSPECTIVE

- **Open systems interfaces are a necessity**
- **All vendors who follow ISDN standards should be able to interconnect**


ISDN SERVICES
OPEN SYSTEMS
ISDN

AT&T's CORPORATE COMMITMENTS

- **Standard U, S, T interfaces**
- **Support for existing interfaces**
- **Network-wide support including resources on demand and integrated transport**
- **Centrex solutions**
- **PBX interconnect**
- **Share technology in support of services**

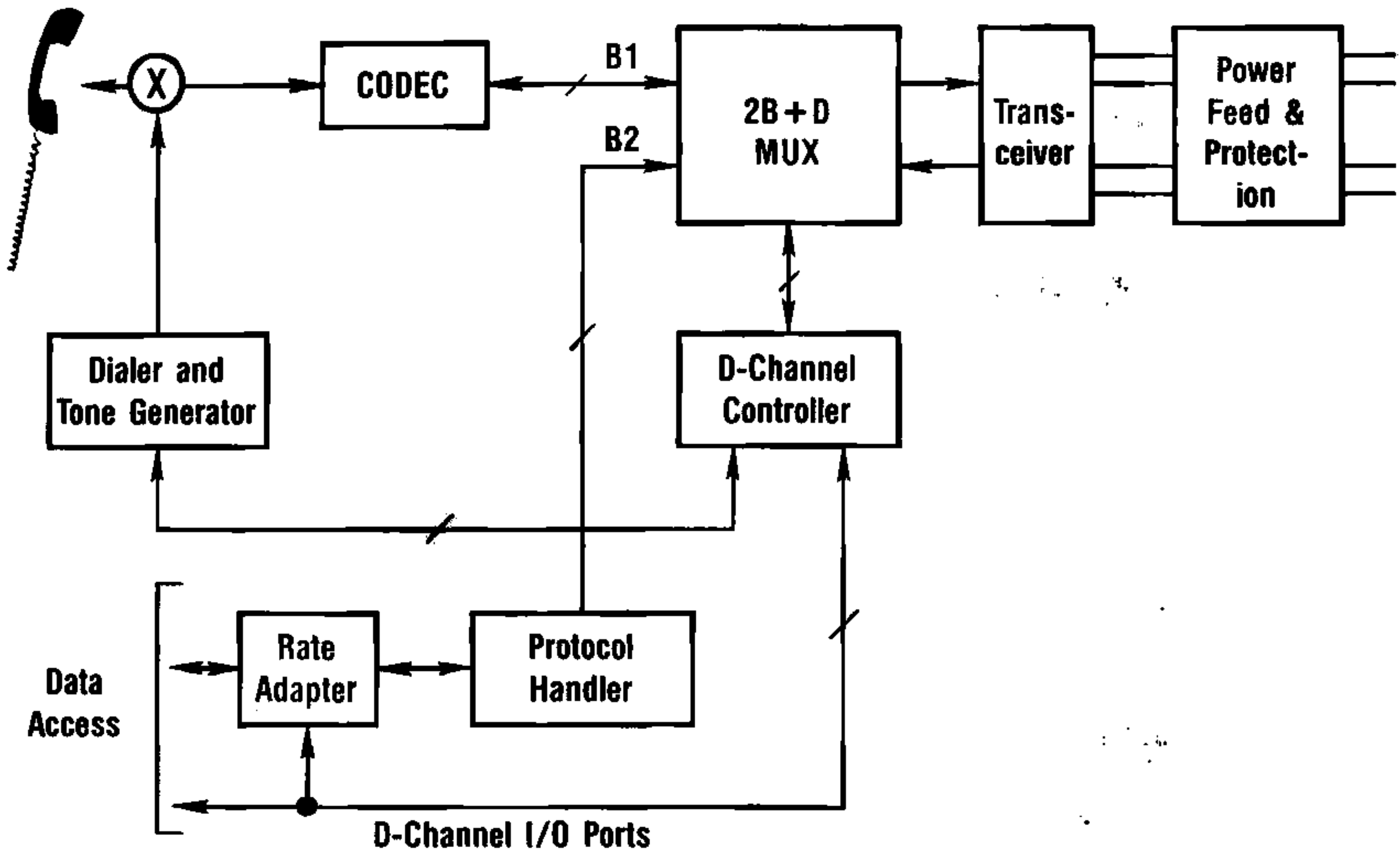
RECENT ACTIVITY

- Public commitment to standards
- Active participation in standards bodies
- Organization of DMI users' group
- Sale of ISDN devices

FACTORS WHICH WILL INFLUENCE ISDN DEVICE MARKET

- High volume market
- Standards not defined
- Loop electronics design is extremely complex
- System architectures important
- Many ISDN terminal building blocks exist today
- A variety of terminals will exist

GENERAL PURPOSE TERMINAL



ISDN FACTORS AND THEIR IMPACT ON DEVICES

FACTOR	IMPACT
• High volume demand	• Low prices, competitive business
• Standards not defined	• Devices must be adaptable, flexible
• Loop electronics design is extremely complex	• Device vendors must have access to telecommunications expertise
• System architecture important	• Device architectures that fit best will win
• Many ISDN building blocks exist today	• Partitioning matters, integrated solutions must be cheap
• A variety of terminals will exist	• A variety of devices will exist

IT IS FAIR TO SAY THAT FOR THOSE SEMICONDUCTOR MANUFACTURERS INTENT ON SUPPLYING THE COMPONENTS THAT ARE SPECIFIC TO THE COMMUNICATIONS INDUSTRY, ISDN IS SEEN AS A MAJOR OPPORTUNITY AND CHALLENGE. THE OPPORTUNITY ARISES FROM THE POTENTIAL SIZE OF THE MARKET. THE CHALLENGE COMES FROM THE PROCESS OF DETERMINING HOW TO MAKE A POSITIVE CONTRIBUTION TO THE IMPLEMENTATION OF A GROUP OF STANDARDS THAT ARE STILL EVOLVING IN THE COMPETITIVE ENVIRONMENT OF TODAY'S WORLD. AT ADVANCED MICRO DEVICES, WE BELIEVE THAT THE SEMICONDUCTOR INDUSTRY CAN MAKE ITS GREATEST CONTRIBUTION TO THE ISDN EVOLUTION BY FOCUSING ON DOING WHAT WE, AS AN INDUSTRY, DO BEST.

SO WHAT IS THE ROLE OF THE SEMICONDUCTOR MANUFACTURER?

THE SEMICONDUCTOR MANUFACTURER BRINGS TWO INTERRELATED, AND IN SOME WAYS, ESSENTIAL, CAPABILITIES TO THE EVOLVING WORLD OF ISDN. THE FIRST IS THE ROLE OF THE PRODUCTIVITY ENGINE. THE SECOND IS THE ROLE OF STANDARDS INSURANCE. LET'S EXAMINE THESE BRIEFLY. FUNDAMENTALLY, THE REASON A SEMICONDUCTOR MANUFACTURER HAS BEEN INCLUDED IN THE PROGRAM FOR THIS CONFERENCE IS IN RECOGNITION OF THE FACT THAT, WITHOUT THE COST REDUCTION POWER OF MODERN SEMICONDUCTOR PROCESSING, NONE OF THE END USERS WOULD BE ABLE TO AFFORD ISDN. THE USER COMMUNITY AND EQUIPMENT MANUFACTURERS HAVE BOTH COME TO THIS REALIZATION. FROM A SEMICONDUCTOR POINT OF VIEW, WE WELCOME THE OPPORTUNITY OF WORKING WITH YOU TO MAKE THE PROMISE OF ISDN A REALITY. PLEASE NOTE I USED THE WORD "WORKING". THIS WAS ON PURPOSE. AS A PRODUCTIVITY ENGINE, THE SEMICONDUCTOR INDUSTRY REDUCES COST THROUGH VLSI COMPONENTS. THE "MAGIC" OF VLSI COST REDUCTION IS BEST DEPICTED BY

AN EXAMPLE EVERYONE IN THE ELECTRONICS INDUSTRY IS FAMILIAR WITH. FIGURE 1 SHOWS THE DRAMATIC DECLINE OF DYNAMIC RAM MARKET PRICES ON A PER BIT BASIS SINCE 1972. THIS REDUCTION DID NOT JUST HAPPEN. IT IS THE DIRECT RESULT OF HUNDREDS OF MILLIONS OF DOLLARS OF INVESTMENT AND THOUSANDS OF MAN YEARS OF EFFORT. IN ADDITION, IT HAS ONLY BEEN ACHIEVED BY THE SLAVISH ADHERENCE TO SOME DEMANDING RULES. BUT, MORE ABOUT THAT LATER.

THE SECOND ROLE MENTIONED WAS ONE OF STANDARDS INSURANCE. WHAT DOES THIS MEAN? AS STANDARDS ARE ADOPTED AND SILICON IMPLEMENTATIONS BEGIN TO ENTER THE MARKET A CONSTITUENCY DEVELOPS THAT SUPPORTS THE CONTINUATION OF THESE STANDARDS. HISTORICALLY, THE READY AVAILABILITY OF INDUSTRY STANDARD DEVICES FROM MERCHANT MARKET SEMICONDUCTOR COMPANIES HAS GREATLY ASSUAGED THE FEARS OF SMALLER EQUIPMENT SUPPLIERS ABOUT THE ABILITY OF THEIR LARGER, VERTICALLY INTEGRATED COMPETITORS TO MANIPULATE THE MARKET. IN ADDITION, USERS HAVE BEEN MORE INCLINED TO COMMIT TO PURCHASE OF "STANDARDIZED" SYSTEMS BECAUSE THE EFFECTIVE LIFETIME OF SUCH EQUIPMENT HAS BEEN MUCH LONGER. FINALLY, WHEN EXPERIENCE HAS INDICATED ADJUSTMENTS WERE NECESSARY IN THE STANDARDS, THE COST IMPACT OF THE CHANGES HAS FORCED A THOROUGH REVIEW OF THE ISSUE BEFORE MODIFICATIONS WERE MADE, THE COMMUNICATIONS INDUSTRY THOROUGHLY UNDERSTANDS THE IMPORTANCE OF BACKWARD COMPATIBILITY.

EARLIER, I STATED THAT THE CONTRIBUTION OF THE SEMICONDUCTOR INDUSTRY TO ISDN WAS TO PROVIDE THE COST REDUCTION VEHICLE TO HELP MAKE ISDN A REALITY. AT AMD, WE HAVE AN OBJECTIVE TO ASSIST IN THE ACHIEVEMENT OF

THIS GOAL BY DEVELOPING HIGHLY INTEGRATED COMPONENTS TO HELP MAKE IT POSSIBLE TO PROVIDE DIGITAL POTS (PLAIN OLD TELEPHONE SERVICE) AT THE SAME PRICE OR CHEAPER THAN ANALOG POTS, AS SOON AS POSSIBLE. WE BELIEVE THIS WILL BE POSSIBLE IN THE NOT TOO DISTANT FUTURE, IF WE FOLLOW THE RULES.

SO WHAT ARE THE RULES?

1. AT THE TIME OF DEVICE DEFINITION, THE CHOICE HAS TO BE MADE TO SELECT A TARGET MANUFACTURING PROCESS THAT HAS THE TIGHTEST PHOTOLITHOGRAPHIC GEOMETRIES POSSIBLE. IN THIS WAY, THE ULTIMATE CHIP AREA (AND THE MATURE MANUFACTURING COST) OF THE DEVICE WILL BE THE SMALLEST POSSIBLE. THIS PROCESS SELECTION, ONCE MADE, HAS SIGNIFICANT IMPLICATIONS ON DEVICE ARCHITECTURE. THIS ISSUE IS BEST SEEN IN FIGURE 2.

TODAY'S STATE OF THE ART PROCESSES FOR LOGIC PRODUCTS HAVE MINIMUM FEATURE SIZES ON THE ORDER OF 1.5 MICRONS. OVER THE LAST NINE YEARS, WE HAVE EXPERIENCED A REDUCTION OF MINIMUM FEATURE SIZE FROM SIX MICRONS TO TODAY'S 1.5 AND THIS REDUCTION IS EXPECTED TO CONTINUE TOWARD 0.8 MICRONS AND LOWER BY 1991. AS FEATURES SIZES SHRINK, THE SILICON AREA INHABITED BY ANY GIVEN TRANSISTOR IS REDUCED BY A FACTOR APPROXIMATELY EQUAL TO THE SQUARE OF THE RATIO OF THE FEATURE SIZE REDUCTION. FOR EXAMPLE, TODAY'S 1.5 MICRON TRANSISTOR OCCUPIES ONE-SIXTEENTH THE AREA OF 1977'S SIX MICRON DEVICE AND 1991'S 0.8 MICRON DEVICE WILL BE ROUGHLY 25% THE SIZE OF TODAY'S. THIS IS THE FUNDAMENTAL PROCESS THAT FEEDS THE SEMICONDUCTOR INDUSTRY'S ABILITY TO REDUCE COST.

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HOWEVER, THIS DEVICE AREA REDUCTION IS NOT FREE. ONE OF THE BIGGEST CHANGES IS IN DEVICE DESIGN. THE MAXIMUM SUPPLY VOLTAGE THAT CAN BE RELIABLY SUPPORTED BY A TRANSISTOR CHANGES AS DEVICE GEOMETRIES SHRINK. AS YOU CAN SEE IN THE FIGURE THERE ARE TWO TRANSITION ZONES. AT ABOUT A TWO MICRON LEVEL IT IS NO LONGER POSSIBLE TO RELIABLY SUPPORT A 10-VOLT (OR +/- 5V) SUPPLY VOLTAGE IN PRODUCTION. BELOW ABOUT 1 MICRON A SIMILAR TRANSITION OCCURS FROM 5V TO 3V.

THESE TRANSITIONS OCCUR BECAUSE AS THE DEVICE GEOMETRIES SHRINK, IT BECOMES IMPOSSIBLE TO MAINTAIN THE INTEGRITY OF THE TRANSISTOR GATE OXIDE IN THE PRESENCE OF THE FIELDS INDUCED BY THE SUPPLY VOLTAGES ACROSS THE OXIDE. THE RESULT IS THAT THE TRANSISTOR THRESHOLD VOLTAGE SHIFTS AND THE DEVICE CAN NO LONGER BE TURNED "ON" OR "OFF" AT THE DESIGNED LEVEL. PROPER OPERATION OF THE CIRCUIT CEASES.

LOGIC CIRCUITS HAVE OPERATED PREDOMINATELY AT +5V SINCE INTEGRATED CIRCUITS WERE INVENTED. IN A FEW YEARS HOWEVER, THIS WILL HAVE TO CHANGE IF WE ARE TO TAKE ADVANTAGE OF THE COST REDUCTION THAT WILL BE POSSIBLE WITH THE STATE OF THE ART IN PROCESSING TECHNOLOGY. TODAY, HOWEVER, THE ANALOG CIRCUITS IN ISDN (AND BY THIS, I MEAN THE VOICE SUPPORTING, CODEC-FILTER CIRCUITS) HAVE TO OPERATE AT +5V ONLY, TO TAKE ADVANTAGE OF TODAY'S PROCESSING CAPABILITIES. FORTUNATELY, AS THE TELEPHONE NETWORK MIGRATES FROM THE ANALOG SUBSCRIBER LOOP TO THE ISDN DIGITAL LOOP, THE CODEC-FILTER FUNCTION MOVES FROM THE SWITCH LINE CARD TO THE TELEPHONE INSTRUMENT ITSELF. THE WIDER ANALOG SIGNAL SWINGS THAT NECESSITATED +/-5V

SUPPLIES IN THE ANALOG LOOP APPLICATION FROM A SIGNAL-TO-NOISE RATIO POINT OF VIEW ARE NO LONGER NECESSARY. ADDITIONALLY, +5V-ONLY CODEC-FILTER DESIGNS MEAN THAT A SINGLE ISDN DIGITAL TELEPHONE CHIP IS POSSIBLE. FURTHERMORE, THE DIFFICULTY OF PROVIDING POWER TO THE TERMINAL IN ORDER TO SUPPORT BASIC POTS IN AN EMERGENCY CONDITION DURING A POWER OUTAGE IS GREATLY SIMPLIFIED, BECAUSE THE VOICE CIRCUITS DO NOT REQUIRE A NEGATIVE SUPPLY VOLTAGE. +5V IS ENOUGH. LASTLY, THE COST OF IMPLEMENTING THE TERMINAL FUNCTION WILL BE OPTIMIZED BECAUSE THE OVERALL SILICON AREA CAN BE MINIMIZED BY THE USE OF THE STATE OF THE ART IN PROCESSING TECHNOLOGY. TO SUMMARIZE THIS FIRST RULE: IN ORDER TO BUILD THE LOWEST COST ISDN TERMINAL, SELECT COMPONENTS MANUFACTURED ON THE SMALLEST GEOMETRY PROCESS AVAILABLE, +5V-ONLY OPERATION IS A GOOD KEY. IF A NEGATIVE SUPPLY VOLTAGE IS REQUIRED ON THE CODEC FUNCTION, YOU'RE LOOKING AT A SOLUTION BASED ON YESTERDAY'S PROCESSING TECHNOLOGY THAT WILL NOT BE COST EFFECTIVE.

2. THE SECOND RULE WE USE IS TO ARCHITECT EACH DEVICE WITH THE HIGHEST LEVEL OF INTEGRATION POSSIBLE. THIS YIELDS SEVERAL BENEFITS RELATING DIRECTLY TO COST.

A. ELIMINATION OF EXTERNAL PASSIVE COMPONENTS

B. REDUCTION IN THE CHIP COUNT NEEDED TO IMPLEMENT THE FUNCTION.

C. REDUCTION IN BOARD AREA, AND

D. FEWER INTERFACE STRUCTURES BETWEEN CHIPS WHICH REDUCES POWER DISSIPATION

AS AN EXAMPLE OF THE LEVEL OF INTEGRATION POSSIBLE, LET'S REFER TO FIGURE 3. THIS IS THE ARCHITECTURE OF THE Am79C30 DIGITAL SUBSCRIBER CONTROLLER. IT IS THE CLOSEST THING TODAY TO A SINGLE CHIP, ISDN TERMINAL DEVICE. IT INCLUDES THE S-INTERFACE TRANSCEIVER, DATA LINK CONTROLLER FOR FORMATTING THE "D" CHANNEL, A MICROPROCESSOR INTERFACE FOR LOCAL CONTROL AND SIGNAL PROCESSING, AND A MAIN AUDIO PROCESSOR FOR HANDLING THE CODEC-FILTER FUNCTION, RING GENERATION, SIDETONE SUPPORT, DTMF GENERATION, AND HANDSET OR LOUDSPEAKER INTERFACE. THIS DEVICE IS 92K SQUARE MILS IN AREA AND CONTAINS OVER 100K TRANSISTORS. IT IS BUILT ON A 1.6 MICRON CMOS PROCESS AND IS THE ONLY DEVICE OF ITS KIND THAT USES A SINGLE +5V SUPPLY.

3. THE THIRD RULE IS THE SELECTION OF A DEVICE ARCHITECTURE THAT WILL ALLOW THE SEMICONDUCTOR MANUFACTURER TO MORE READILY TAKE ADVANTAGE OF FUTURE ADVANCES IN PROCESSING TECHNOLOGY TO REDUCE THE SIZE OF HIS CIRCUITS. WE TALKED ABOUT THE IMPLICATIONS OF SUPPLY VOLTAGE EARLIER. THE TOPIC I AM REFERRING TO NOW IS DIFFERENT FROM THAT. IT IS THE CHOICE OF A FUNCTIONAL IMPLEMENTATION THAT WILL ALLOW THE CIRCUIT AREA TO BE REDUCED MOST QUICKLY AND EASILY. THE LAYMAN'S TERM FOR THIS DIE AREA REDUCTION IS THE "SHRINK". CHIP AREAS ARE REDUCED IN SEVERAL WAYS; REDESIGN, RELAYOUT, AND/OR OPTICAL REDUCTION. IN THE CASE OF REDESIGN, THE DEVICE IS RE-ENGINEERED TO ELIMINATE REDUNDANT CIRCUIT ELEMENTS. IN

RELAYOUT, THE DEVICE IS REDRAWN TO OPTIMIZE THE PHYSICAL LAYOUT, OR TOPOLOGY, OF THE DEVICE. BOTH OF THESE ARE TIME-CONSUMING PROCESSES AND REQUIRE A SIZEABLE ENGINEERING INVESTMENT. IN THE CASE OF OPTICAL REDUCTION, HOWEVER, THE GEOMETRIES OF THE MASKS USED FOR WAFER FABRICATION ARE PROPORTIONATELY REDUCED PHOTOLITHOGRAPHICALLY. THE NEW DEVICE IS THEN MANUFACTURED ON A PROCESS WITH REDUCED GEOMETRIES THAT ARE CONSISTENT WITH ITS NEW REDUCED SIZE.

A 20% LINEAR REDUCTION OF THE DEVICE GEOMETRIES WILL RESULT IN A "SHRUNK" CHIP THAT IS 64% OF ITS ORIGINAL SIZE. THE IMPACT OF THIS PROCESS IS ILLUSTRATED IN FIGURE 4. TODAY'S SIX INCH WAFER HAS 336 POSSIBLE LOCATIONS ON IT IF THE DIE SIZE IS 70K SQUARE MILS OR 45.2 SQUARE MILLIMETERS. A 20% LINEAR REDUCTION OF THE DEVICE GEOMETRIES WILL RESULT IN A NEW DIE SIZE OF ABOUT 45K SQUARE MILS OR 29 SQUARE MILLIMETERS. THE SHRUNK DEVICE WILL SIT ABOUT 550 TIMES ON THE SAME WAFER. THUS, IF THE ORIGINAL DIE COST $1.00, THE NEW DIE WILL COST $0.64. OPTICAL REDUCTION IS MUCH LESS TIME CONSUMING AND MUCH LESS ENGINEERING RESOURCE INTENSIVE THAN REDESIGN OR RELAYOUT.

SO HOW DOES THIS RELATE TO THE ARCHITECTURE OF THE DEVICE?

TO DATE, THE SEMICONDUCTOR INDUSTRY HAS BEEN VERY EFFECTIVE USING OPTICAL REDUCTION TECHNIQUES ON DIGITAL CIRCUITS. MUCH OF THE COST REDUCTION SUCCESS OF THE MICROPROCESSOR IS ATTRIBUTABLE TO THIS. THE ALL DIGITAL PORT CARD CIRCUITS IN AN ISDN SWITCH WILL BENEFIT FROM THE SAME TECHNIQUES. HOWEVER, IN THE COST SENSITIVE TERMINAL APPLICATION, THE

ANALOG VOICE CIRCUITS REQUIRE REDESIGN. ANALOG CIRCUITS, AND PARTICULARLY, SWITCHED CAPACITOR FILTER STRUCTURES, GENERALLY SPEAKING, DON'T SHRINK PHOTOLITHOGRAPHICALLY. HOWEVER, DIGITAL SIGNAL PROCESSING-BASED FILTER ARCHITECTURES, BY THEIR VERY NATURE, ARE PREDOMINATELY DIGITAL. THUS, THERE IS MUCH LESS ANALOG CIRCUITRY TO REDESIGN ON A DSP BASED PRODUCT. IT WILL SHRINK FASTER AND IT WILL PROGRESS DOWN THE COST REDUCTION SLOPE MORE QUICKLY THAN AN ANALOG-ORIENTED SWITCHED-CAPACITOR BASED DESIGN. AT AMD, WE HAVE SUCCESSFULLY DEMONSTRATED THIS SHRINK TECHNIQUE (I.E., PHOTOLITHOGRAPHICALLY REDUCING THE DIGITAL CIRCUITS AND REDESIGNING THE ANALOG PORTIONS) ON SEVERAL OF OUR EXISTING DSP BASED PRODUCTS THAT ARE IN VOLUME PRODUCTION TODAY.

TO SUMMARIZE: THE PRIMARY CONTRIBUTION OF THE SEMICONDUCTOR INDUSTRY TO ISDN AS THAT OF BEING A PRODUCTIVITY ENGINE, COST REDUCTION CAN BE ATTAINED BY APPLYING STATE OF THE ART PROCESSING TECHNOLOGY. CIRCUIT ARCHITECTURES MUST BE CHOSEN THAT ALLOW THE APPLICATION OF TODAY'S LEADING EDGE TECHNOLOGY AS WELL AS THE OPPORTUNITY TO QUICKLY PROGRESS ONWARD IN THE FUTURE AS PROCESS TECHNOLOGY ADVANCES FURTHER.

WITH THE JUDICIOUS APPLICATION OF THESE PRINCIPLES, THE DIGITAL TELEPHONE WILL BECOME LESS EXPENSIVE THAN THE ANALOG PHONE.

AT THE BEGINNING OF THIS PRESENTATION, I SAID THE SEMICONDUCTOR INDUSTRY WELCOMES THE OPPORTUNITY OF WORKING WITH YOU TO MAKE ISDN A REALITY. I HAVE DESCRIBED THE ROLES WE WILL PLAY AND HOW WE WILL PERFORM THEM. BUT THE PART I HAVE DESCRIBED REQUIRES A LOT OF HARD WORK AND LARGE FINANCIAL INVESTMENTS. SO, WHY DO WE IN THE SEMICONDUCTOR INDUSTRY CARE ABOUT ISDN?

THE SEMICONDUCTOR INDUSTRY IS ALWAYS LOOKING FOR NEW GROWTH MARKETS TO FUEL THE 15-25% COMPOUND ANNUAL GROWTH RATES WE HAVE HISTORICALLY ENJOYED AND HOPE TO ENJOY AGAIN SOON IN THE NEAR FUTURE. ISDN HAS THE POTENTIAL TO BECOME A MAJOR GROWTH MARKET. IN FACT, IT HAS THE POTENTIAL OF BEING THE CATALYST THAT WILL RESULT IN A TECHNOLOGICAL REVOLUTION AS SIGNIFICANT TO BUSINESS OPERATIONS AS THE INVENTION OF THE COMPUTER. THIS REVOLUTION WILL BE THE FORCE BEHIND THE CONSUMPTION OF UNPRECEDENTED NUMBERS OF TERMINALS, PC'S, COMPUTERS, PERIPHERALS AND THE COMMUNICATIONS EQUIPMENT THAT WILL LINK THEM ALL TOGETHER. FIGURE 5 HELPS PUT THIS IN PERSPECTIVE. THE WORLDWIDE PABX MARKET IN 1986 WILL BE ABOUT 12 MILLION LINES SHIPPED. THIS NUMBER WILL GROW AT ABOUT AN 8% ANNUAL RATE TO ABOUT 16 MILLION LINES IN 1990. AT THE SAME TIME, THIS GROWTH IS OCCURRING ANOTHER SIGNIFICANT TREND IS WELL UNDERWAY. THE USAGE OF THESE NEW PABX LINES SHIPPED IS INCREASINGLY DATA ORIENTED. AS SHOWN IN FIGURE 6, INDUSTRY SOURCES PROJECT THAT IN 1988, A MINIMUM OF 40% OF THE PABX LINES SHIPPED WILL BE CONFIGURED FOR DATA COMMUNICATION CAPABILITY. THIS STEADILY INCREASING RATE OF INVESTMENT IN DATA COMMUNICATIONS CAPABILITY IS A REFLECTION OF THE OFFICE SYSTEM INTEGRATION THAT IS TAKING PLACE AROUND THE WORLD.

BUT, WHY IS THE PUSH TOWARD OFFICE INTEGRATION OCCURRING? IT IS BASICALLY THE CONFLUENCE OF TWO SETS OF FORCES. FIRST, THE ECONOMIES OF MOST OF THE INDUSTRIALIZED WESTERN COUNTRIES HAVE BEEN EVOLVING INTO WHAT ECONOMIST REFER TO AS POST-INDUSTRIAL SERVICE-ORIENTED ECONOMIES. IN THE U.S., THE EVOLUTION CAN BE SEEN IN THE STATISTICS ON JOB GROWTH. IN 1984, NEW SERVICE JOBS WERE CREATED AT A RATE THAT WAS 10 TIMES GREATER THAN THE CREATION OF MANUFACTURING JOBS. THE STOCK-IN-TRADE OF THE SERVICE WORKER IS THE HANDLING OF INFORMATION, BOTH VOICE AND DATA. SECONDLY, IT HAS VERY RAPIDLY BECOME APPARENT TO MOST COMPANIES THAT WE ARE NOW IN AN AGE CHARACTERIZED BY A WORLDWIDE ECONOMY. MAINTAINING MARKET SHARE AND PROFIT MARGINS TODAY MEANS OUTPERFORMING COMPETITORS FROM ALL OVER THE GLOBE. THIS WORLDWIDE COMPETITION HAS SPURRED CORPORATE MANAGEMENTS TO PRESS FOR PRODUCTIVITY IMPROVEMENTS FROM ALL PARTS OF THEIR ORGANIZATIONS.

IT IS A WIDELY RECOGNIZED FACT THAT WHITE COLLAR OFFICE WORKERS ARE UNDER-CAPITALIZED IN THE WORKPLACE. PRODUCTIVITY GROWTH IN THIS SECTOR HAS GENERALLY LAGGED PRODUCTIVITY GROWTH IN THE ECONOMY AS A WHOLE BY 30-60% OVER A LONG PERIOD OF TIME.

STUDIES SHOW THAT ACHIEVABLE SAVINGS DUE TO IMPROVED OFFICE PRODUCTIVITY IN THE U.S.A. COULD BE AS HIGH AS $100 BILLION PER YEAR. ONE OF THE KEYS TO IMPROVED CORPORATE PERFORMANCE ON A WORLD-WIDE BASIS IS THE INFUSION OF CAPITAL INVESTMENT INTO THE OFFICE ENVIRONMENT. EXAMPLES ARE ALL AROUND US--THE PERSONAL COMPUTER EXPLOSION IN THE WORKPLACE IS ONE OF THE BEST ONES. THE KEY TO THE RESOLUTION OF THE OFFICE PRODUCTIVITY PROBLEM IS COMMUNICATIONS--BOTH VOICE AND DATA.

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IF YOU EXTEND THE TREND SHOWN IN FIGURE 6 A FEW MORE YEARS YOU GET SOME INTERESTING RESULTS. THIS IS SUMMARIZED IN FIGURE 7. THIS EXTENSION INDICATES THAT 60% OF THE PABX LINES SHIPPED WORLDWIDE IN 1990 WILL HAVE A DATA CAPABILITY OR WILL SUPPORT DIGITAL TELEPHONES. UNDER THE ASSUMPTION THAT ISDN IS IN FULL SWING BY THEN, THERE COULD BE 10 MILLION LINES OF ISDN EQUIPMENT SHIPPED THAT YEAR. IF THERE ARE JUST TWO ISDN SPECIFIC INTEGRATED CIRCUIT ON EACH OF THOSE LINES, THE UNIT VOLUME ON PORT-CARD IC'S WILL BE EQUIVALENT TO TWICE THE SIZE OF THE 1984 SHIPMENTS OF 16-BIT MICROPROCESSORS AS REPORTED BY THE SEMICONDUCTOR INDUSTRY ASSOCIATION (SIA).

BUT IN ADDITION TO PORT-CARDS, THERE WILL BE ISDN TERMINALS ALSO. ONE OF THE STRENGTHS OF THE CCITT STANDARDS IS IN THE CONFIGURATION KNOWN AS THE PASSIVE BUS ONTO WHICH UP TO EIGHT ISDN TERMINALS CAN BE CONNECTED. IF ISDN IS IN FULL SWING BY 1990, THERE WILL BE AN AVERAGE OF 2.5 TERMINALS SHIPPED FOR EACH ISDN EQUIPPED PABX LINE WITH 2 ISDN IC'S PER TERMINAL.

IT JUST SO HAPPENS THAT THE TOTAL OF 70 MILLION ISDN SPECIFIC IC'S IN 1990 IS EQUIVALENT TO TWICE THE SIZE OF THE 1985 SIA FORECAST OF 16 BIT MICROPROCESSOR CONSUMPTION IN 1990. THIS ANALYSIS IS BASED ON THE CHIP SET ARCHITECTURE SHOWN IN FIGURE 8 IN WHICH THERE IS ONE ISDN SPECIFIC POWER CHIP AND ONE ISDN SPECIFIC SIGNAL HANDLING DEVICE AT EACH END OF THE 'S' INTERFACE. OBVIOUSLY, IF YOU USE THE LESS INTEGRATED CHIP SETS BEING PROPOSED BY OTHERS, THE NUMBER OF DEVICES GROWS BY A FACTOR OF TWO TO THREE. IN EITHER EVENT, THE POTENTIAL VALUE OF THIS MARKET WILL BE ABOUT $500 MILLION.

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SO, HOW DO WE GET THERE FROM HERE? HOW CAN THIS POTENTIAL BE TURNED INTO REALITY IN THE TIME FRAME MENTIONED? THE FIRST THING TO DO IS TO STEP BACK AND LOOK AT THE WORLD FROM THE USER'S POINT OF VIEW. USERS ARE OVERWHELMED AND DISENCHANTED. THEY ARE OVERWHELMED BY THE RATE OF CHANGE OF TECHNOLOGY. PRODUCT LIFECYCLES HAVE BEEN REDUCED TO SUCH AN EXTENT THAT THE NEXT GENERATION IS ALWAYS JUST AROUND THE CORNER. SINCE INFORMATION PROCESSING AND COMMUNICATIONS EQUIPMENT TODAY ARE GENERALLY VENDOR SPECIFIC AND NOT INTERCHANGEABLE, THE USER HAS AN EXTRA INCENTIVE TO WAIT AND SEE WHAT NEW PRODUCTS WILL BE INTRODUCED WITHIN SIX MONTHS FROM ANY POINT OF TIME. ONCE A COMMITMENT IS MADE, HE IS LOCKED IN. IN THIS WAY, WE HAVE CONDITIONED OUR CUSTOMERS TO POSTPONE THEIR DECISIONS. ONE RESULT OF THIS IS THE TYPE OF ECONOMIC DOWNTURN WE EXPERIENCED IN 1985. THE DISENCHANTMENT EXISTS BECAUSE THE PROMISED LEVEL OF PRODUCTIVITY IMPROVEMENT ADVERTISED FOR THE CURRENT GENERATION OF OFFICE PRODUCTS HAS GENERALLY FAILED TO OCCUR. THE CURRENT GENERATION OF OFFICE PRODUCTS CAN BE CHARACTERIZED AS "POINT PRODUCTS" WITH THE PC AS THE CLASSIC EXAMPLE. AS SALOMON BROTHERS, INC. NOTED AT THEIR 1985 SOUTHEASTERN INVESTMENT CONFERENCE, "THE POINT PRODUCT HAS IMPROVED THE PRODUCTIVITY OF INDIVIDUALS, BUT HAS HAD LITTLE IMPACT ON THE PRODUCTIVITY OF CORPORATIONS. THE TECHNOLOGY THAT FACILITATES THE SHARING OF INFORMATION HAS LAGGED TECHNOLOGY THAT FACILITATES THE CREATION OF INFORMATION. (EMPHASIS ADDED.)

THE RATE OF DEVELOPMENT OF THE LOCAL AREA NETWORK MARKET IS DRAMATICALLY BELOW THE EXPECTATIONS OF JUST A FEW YEARS AGO. HOW DID THIS HAPPEN? IN THE CRITICAL PHASE BETWEEN THE INITIAL ETHERNET PROPOSAL BY XEROX UNTIL COST EFFECTIVE IMPLEMENTATIONS BASED ON ETHERNET-SPECIFIC IC'S COULD HIT THE MARKET, A PLETHORA OF COMPETING STANDARDS WERE CREATED.

ONE OF THE FUNDAMENTAL PROBLEMS IN THE LAN WORLD IS THE STRUCTURE OF THE IEEE 802 COMMITTEE'S DECISION MAKING PROCESS. AS AN INDUSTRY COMMITTEE THERE IS NO REFEREE EXCEPT OTHER COMPETING MEMBERS OF THE SAME INDUSTRY SERVING ON THE COMMITTEE. THUS, WHENEVER TECHNICAL LEADERSHIP IS DISPLAYED BY ONE MEMBER OR GROUP OF MEMBERS ON THE COMMITTEE, THE REST OF THE COMMITTEE IS MOTIVATED TO EITHER DELAY ADOPTION OF THE PROPOSAL UNTIL THEY CAN CATCH UP, OR TO OFFER A COMPETING PROPOSAL. AN "I'LL SCRATCH YOUR BACK IF YOU SCRATCH MINE" LEAST COMMON DENOMINATOR APPROACH GOES INTO EFFECT. MULTIPLE STANDARDS ARE APPROVED SO THAT ALL OF THE COMPETING CAMPS HAVE A ROUGHLY EQUIVALENT MARKET POSITION. THE COMMITTEE DELEGATES CONGRATULATE THEMSELVES AND GO HOME. BUT THE END USERS REMAIN CONFUSED AND POSTPONE PURCHASING COMMITMENTS. THE MARKET FAILS TO DEVELOP TO MEET ITS EXPECTATIONS AND THEN CONFERENCES ARE HELD TO DISCUSS WHY THIS HAS HAPPENED. ISN'T IT OBVIOUS! BY PROPOSING SO MANY STANDARDS, THE RESULT FROM THE USERS' PERSPECTIVE IS THAT THERE REALLY ARE NONE.

SO THE QUESTIONS IS, "WILL ISDN FOLLOW THE SAME PATH AS THE LANS OR CAN A SINGLE SET OF STANDARDS REALLY BE CREATED THAT WILL ALLOW THE MARKET TO DEVELOP RAPIDLY TO THE SIZE MENTIONED EARLIER? ISDN HAS A NUMBER OF SIGNIFICANT STRUCTURAL ADVANTAGES, VIS-A-VIS LAN'S, THAT COULD BE ENOUGH TO CARRY THE DECISION TO A SINGLE APPROACH. LET'S LOOK AT THESE:

1. ISDN HAS A REFEREE IN THE STANDARD MAKING ARENA. THE CCITT IS A GOVERNMENTAL BODY THAT IS GREATLY REMOVED FROM THE TIME TO MARKET LEADERSHIP QUESTIONS THAT HAVE HEAVILY INFLUENCED IEEE 802. THAT'S NOT TO SAY THAT THERE AREN'T COMMERCIAL CONSIDERATIONS PRESENT IN THE PROCESS BECAUSE THERE ARE. HOWEVER, THEIR INFLUENCE IS GREATLY REDUCED AND BALANCED OUT BY THE USERS.

2. USERS ARE ACTIVELY INVOLVED IN THE CCITT ISDN STUDY GROUPS IN THE FORM OF VARIOUS PTT'S. THEIR PRESENCE HELPS TO KEEP THE FOCUS ON ECONOMICALLY VIABLE SOLUTIONS AND UNANIMOUS POSITIONS.

3. IN THE U.S.A. CUSTOMERS ARE GETTING INVOLVED. THIS IS APPARENT IN TWO FORMS. THE FIRST IS PROGRAMS SUCH AS THE GM/EDS PROJECT, AS MENTIONED IN THE TRADE PRESS, IN WHICH A MAJOR USER IS DEMANDING INTER-CHANGEABLE, STANDARDIZED EQUIPMENT FROM ITS POTENTIAL SUPPLIERS. THE SECOND IS THE ACTIVITIES OF THE REGIONAL BELL OPERATING COMPANIES (RBOC'S) IN THE FORM OF FIELD TRIALS AND IN THE T1D1 COMMITTEE. THE FIELD TRIALS ARE INTENDED TO GAIN ACTUAL EXPERIENCE IN THE USAGE OF ISDN BASED EQUIPMENT. THE T1D1 COMMITTEE IS WORKING TOWARD THE ADOPTION OF A U.S. STANDARD FOR CENTRAL OFFICE ISDN IMPLEMENTATIONS.

4. SYSTEM MANUFACTURERS SEEM TO BE RALLYING AROUND THE ADOPTION OF A SINGLE STANDARD. FROM MY POSITION AS A SUPPLIER TO THESE SYSTEM MANUFACTURERS, IT IS ENCOURAGING TO OBSERVE THE CHANGE IN ATTITUDES THAT HAS OCCURRED IN THE LAST TWO TO THREE YEARS. WITH FEW EXCEPTIONS, ATTITUDES OVER THAT TIME PERIOD HAVE CHANGED FROM "ISDN WILL NEVER HAPPEN

AND MY PROPRIETARY APPROACH IS BETTER ANYWAY" TO "WE WILL SUPPORT BOTH THE ISDN STANDARD AND OUR PROPRIETARY APPROACH AND LET OUR CUSTOMERS DECIDE". GIVEN HALF A CHANCE, THE USER'S RESPONSE WILL BE OVERWHELMINGLY ON THE SIDE OF THE STANDARD.

SO THE ANSWER IS STANDARDS. WHY DO WE NEED THEM? MY HYPOTHESIS IS BASED ON THE SUPPOSITION THAT THERE IS MONEY TO BE MADE BY THE RBOC'S AND PTTS THROUGH THE INTRODUCTION OF ISDN SERVICES, BY THE EQUIPMENT MANUFACTURERS IN THE FORM OF GROWING NEW EQUIPMENT SALES AS OLDER GENERATIONS OF PABX AND TERMINAL GEAR IS RETIRED AS WELL AS IN THE NATURAL GROWTH OF THE MARKET, AND, OF COURSE, BY THE SEMICONDUCTOR INDUSTRY IN THE FORM OF SALES TO A NEW AND RAPIDLY GROWING APPLICATION.

AT THE BEGINNING OF THIS PRESENTATION I STATED THAT THE CONTRIBUTION OF THE SEMICONDUCTOR INDUSTRY TO ISDN WAS THE ROLE OF PRODUCTIVITY ENGINE. WE LOOKED AT A NUMBER OF RULES THAT WE USE TO ACHIEVE THE MOST COST EFFECTIVE SILICON IMPLEMENTATIONS OF VARIOUS SYSTEM CIRCUIT FUNCTIONS, BUT THERE IS ONE MORE FUNDAMENTAL RULE THAT NEEDS TO BE MENTIONED. THERE IS NO WAY AROUND IT, THE FUNDAMENTAL PREREQUISITE TO THE COST REDUCTION OF SEMICONDUCTOR COMPONENTS IS VOLUME. THIS IS WHY WE NEED STANDARDS. VOLUME IS THE ENGINE THAT DRIVES THE WHOLE PROCESS.

THE LEARNING CURVE STATES THAT EVERY TIME THE CUMULATIVE SHIPMENTS DOUBLE, THE COST TO MANUFACTURE EACH INDIVIDUAL UNIT REDUCES BY A CERTAIN PERCENTAGE. OUR EXPERIENCE INDICATES THAT THIS PERCENTAGE VARIES OVER A RANGE OF VALUES FROM 10-30%, DEPENDING ON THE TYPE OF CIRCUIT, ITS

COMPLEXITY, AND SO FORTH. WHY DOES THIS HAPPEN? IT'S NOT MAGIC, BUT RATHER THE DIRECT RESULT OF THE WORK I MENTIONED AT THE BEGINNING OF THIS SPEECH.

AS DEMAND FOR A PRODUCT GROWS THERE IS AN INCREASING LEVEL OF ENGINEERING INVESTMENT MADE ON THE PRODUCT. ENGINEERING INVESTMENT IS MADE IN MASK REVISIONS THAT ELIMINATE DESIGN MARGINALITIES THAT LIMIT YIELD OVER THE NORMAL RANGE OF MANUFACTURING TOLERANCE. ENGINEERING INVESTMENT IS MADE IN 'NARROWING' THE RANGE OF EXPECTED VARIATION IN THE MANUFACTURING PROCESS. TEST PROGRAMS ARE IMPROVED TO PROVIDE HIGHER QUALITY AS WELL AS MAKE SURE THAT GOOD PRODUCTS ARE NOT REJECTED BY A FLAW IN THE TEST PROGRAM OR PROCEDURE. SHRINKS ARE PERFORMED TO REDUCE SILICON AREA AND QUALIFIED FOR PRODUCTION AS MENTIONED EARLIER. NEW, LARGER, CLEANER WAFER FABRICATION AREAS THAT PROCESS BIGGER WAFERS WITH BETTER EQUIPMENT THAT CAN RESOLVE FINER GEOMETRIES ARE BROUGHT ON STREAM TO SUPPORT THE SMALLER GEOMETRY PROCESSES MENTIONED EARLIER. (THE REQUIREMENTS OF CLEANER AIR AND MORE PRECISION EQUIPMENT IN THE WAFER FABRICATION AREAS IS THE REASON THAT THE COST OF ONE OF THESE MANUFACTURING MODULES HAS GONE FROM ABOUT $20M FIVE YEARS AGO TO OVER $100M TODAY). IN SUMMARY, THE ONGOING CHALLENGE OF THE LEARNING CURVE CAN BE MET ONLY WITH SIGNIFICANT ONGOING INVESTMENT. THAT INVESTMENT WILL ONLY BE MADE IF THERE IS A RETURN ON THAT INVESTMENT. THE ONLY WAY THAT RETURN CAN OCCUR IS THROUGH VOLUME. THAT IS WHY STANDARDS ARE IMPORTANT.

BUT WHY SHOULD YOU CARE ABOUT ALL OF THIS? YOU COULD CYNICALLY SAY THAT THE DETAILS THAT I HAVE JUST SHARED WITH YOU ARE MY PROBLEM. BUT ARE THEY? I HAVE MADE THE ASSUMPTION THAT THE REASON YOU ARE HERE IS BECAUSE YOUR COMPANY HAS A STAKE IN ISDN AND YOU DO AS WELL.

FRANKLY, WE HAVE A RATHER SIGNIFICANT MUTUALITY OF INTEREST IF YOU STOP TO THINK ABOUT IT, AND DOUBLY SO FOR THOSE OF YOU FROM ORGANIZATIONS THAT ARE NOT VERTICALLY INTEGRATED ENOUGH TO HAVE YOUR OWN STATE OF THE ART SEMICONDUCTOR DESIGN AND MANUFACTURING CAPABILITY. TO PUT IT BLUNTLY, HOW ARE YOU GOING TO COMPETE WITH YOUR VERTICALLY INTEGRATED COMPETITORS WITHOUT A STRONG, VIBRANT AND GROWING GROUP OF MERCHANT MARKET SEMICONDUCTOR SUPPLIERS? EVEN THOSE OF YOU FROM VERTICALLY INTEGRATED ORGANIZATIONS BENEFIT FROM THE INVESTMENT OF THE SEMICONDUCTOR INDUSTRY IN ISDN BECAUSE IT ALLOWS YOU TO FOCUS YOUR R & D MONEY ELSEWHERE IF YOU CHOOSE, IN ORDER TO BE BETTER POSITIONED TO COMPETE WITH VERTICALLY INTEGRATED INTERNATIONAL GIANTS THAT RECEIVE CONSIDERABLE BENEFIT FROM THEIR GOVERNMENTS IN THEIR PROTECTED MARKETS, AS WELL AS THROUGH R & D SUBSIDIZATION.

I HAVE SPOKEN ABOUT THE ENORMOUS ONGOING INVESTMENT NECESSARY TO PROCEED DOWN THE LEARNING CURVE. HOWEVER, THAT IS A SECONDARY CONSIDERATION TO THE LEVEL OF INVESTMENT NEEDED TO ENTER THE RACE. USING THE FOUR DEVICES SHOWN PREVIOUSLY IN FIGURE 8 AS AN EXAMPLE, AT THE TIME OF INSTRUCTION THIS YEAR THESE FOUR DEVICES REPRESENT THE INVESTMENT OF OVER 100 MAN YEARS IN ENGINEERING DEVELOPMENT, IN EXCESS OF AN ADDITIONAL 100 MAN YEARS IN PROCESS DEVELOPMENT AND CIRCUIT ARCHITECTURE DEVELOPMENT, AND A GREATER

THAN $100M INVESTMENT IN EQUIPMENT IN ORDER TO BE ABLE TO MANUFACTURE THEM. FROM THE PERSPECTIVE OF THE USER OF THESE KINDS OF PRODUCTS, YOUR INTEREST IS SERVED IF YOU CAN CONTINUALLY ATTRACT ADDITIONAL SUPPLIERS TO MAKE THAT INVESTMENT TO ENTER THE MARKET.

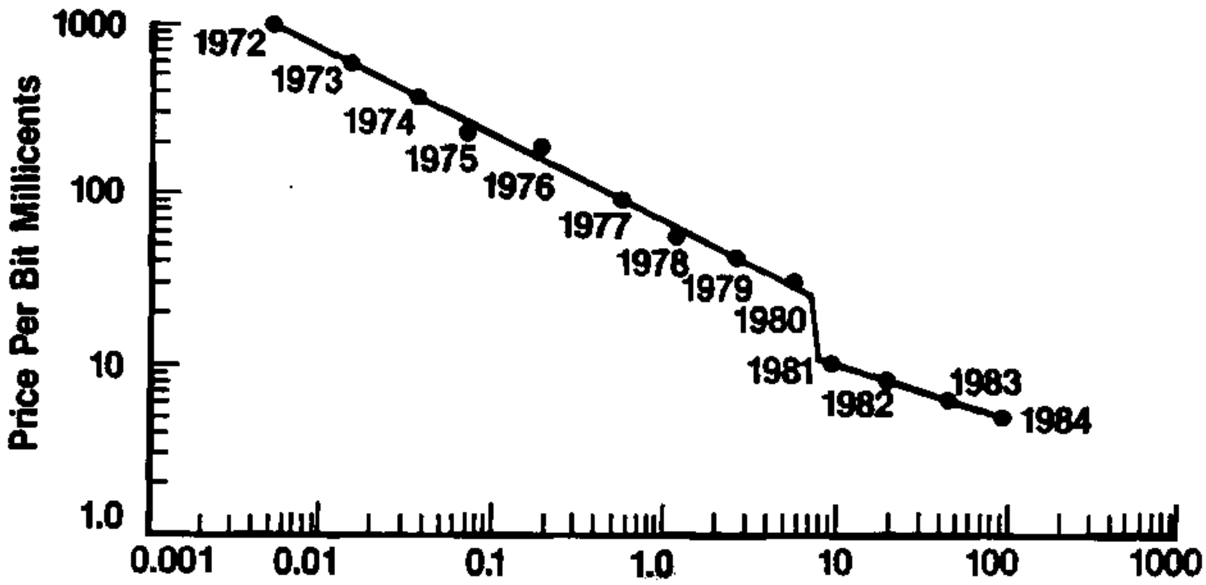
THAT KEEPS INNOVATION FLOWING AND PROVIDES THE COMPETITION THAT KEEPS EVERYONE ON THEIR TOES. HOWEVER, THAT WILL ONLY OCCUR IF THERE IS THE PROSPECT OF AN ADEQUATE RETURN ON THE INVESTMENT. THAT RETURN REQUIRES VOLUME. VOLUME REQUIRES STANDARDS. IN THE ABSENCE OF STANDARDS WE ALL LOSE. LOSING ISN'T FUN AND IT'S CERTAINLY NOT THE STUFF FROM WHICH CAREERS ARE MADE.

IN CONCLUSION, ISDN PRESENTS AN OPPORTUNITY FOR EVERYONE AND EVERY ORGANIZATION REPRESENTED IN THIS ROOM. SEVERAL COMPANIES, AMD AMONG THEM, HAVE MADE SIGNIFICANT INVESTMENTS TOWARD THE REALIZATION OF CCITT ISDN ALREADY. HOWEVER, FOR THE PROMISE OF ISDN TO BE ACHIEVED, ADDITIONAL INVESTMENT WILL BE NEEDED TO FORCE OUR WAY DOWN THE LEARNING CURVE, AND FROM YOUR PERSPECTIVE, NEW INVESTMENT FROM ADDITIONAL PLAYERS NOT CURRENTLY ADDRESSING THE OPPORTUNITY. I'LL SAY IT AGAIN: ONLY VOLUME WILL FILL THIS NEED AND ONLY STANDARDS WILL CREATE THE VOLUME. IF YOU GRASP THAT CCITT ISDN STANDARDS WITH A POSITIVE APPROACH TOWARD MAKING THEM WORK AND PUSH THEM FORWARD TO A RAPID ADOPTION FOR BOTH HARDWARE AND SOFTWARE, THE MARKET WILL FLOURISH AND WE'LL ALL BENEFIT.

THANK YOU

Figure 1

MOS DYNAMIC RAM LEARNING CURVE



Memory Price Per Bit vs Cumulative Volume in Bits x 10^{12}
(Prices are Mid-Year ASPs)

Figure 2

PROCESSING DENSITY TRENDS

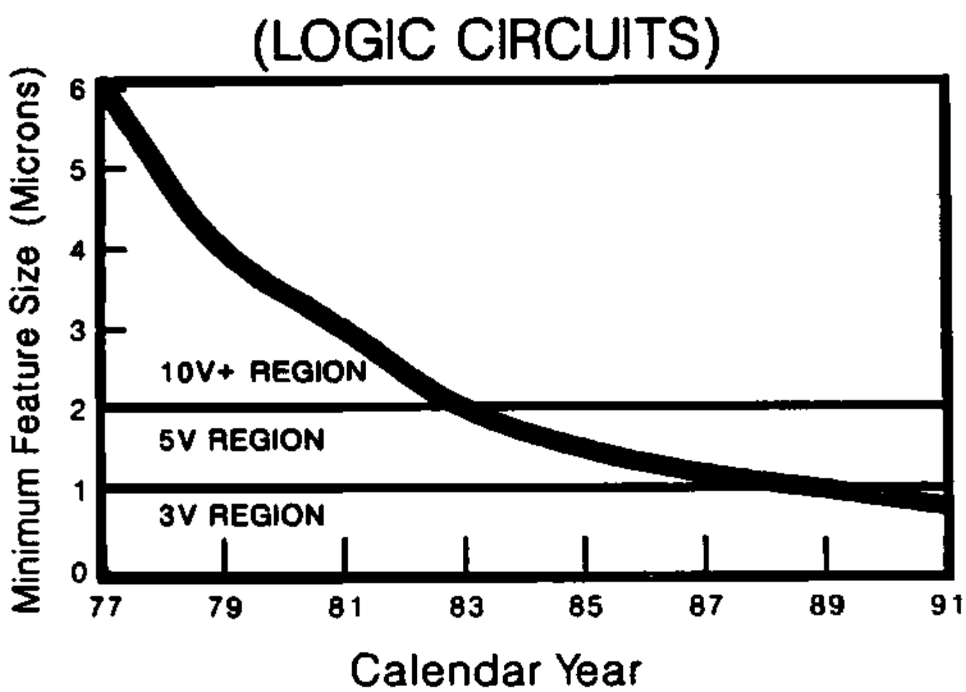


Figure 3

Am79C30 ARCHITECTURE

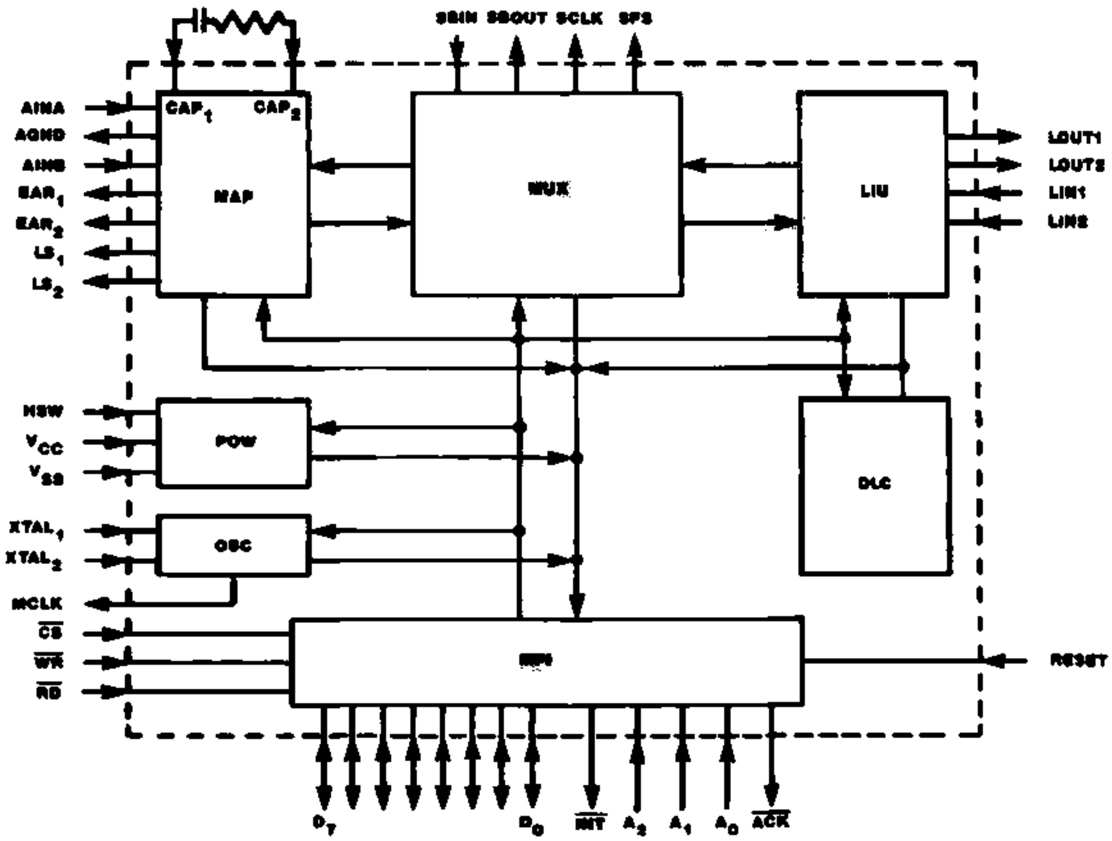
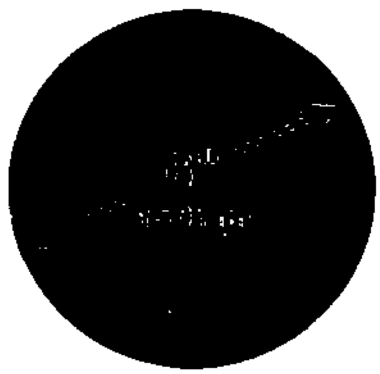


Figure 4

WAFER PROCESSING



DIE SIZE		DPW
mils^2	mm^2	
20000	12.9	1284
30000	19.4	832
40000	25.8	616
50000	32.3	484
60000	38.7	397
70000	45.2	336

Figure 5

ISDN MARKET
PABX MARKET SIZE

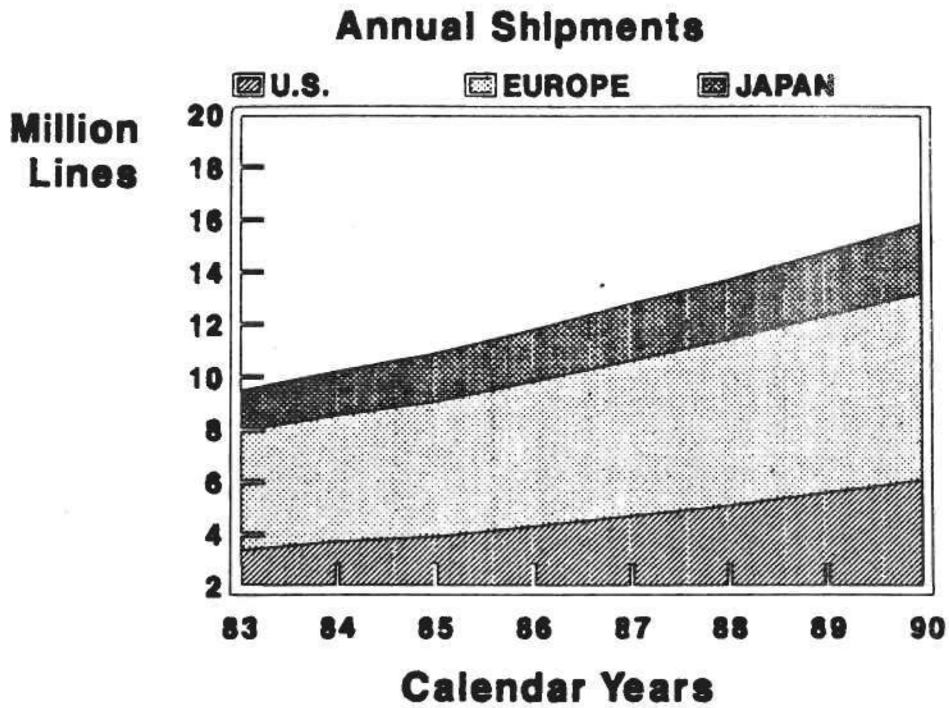


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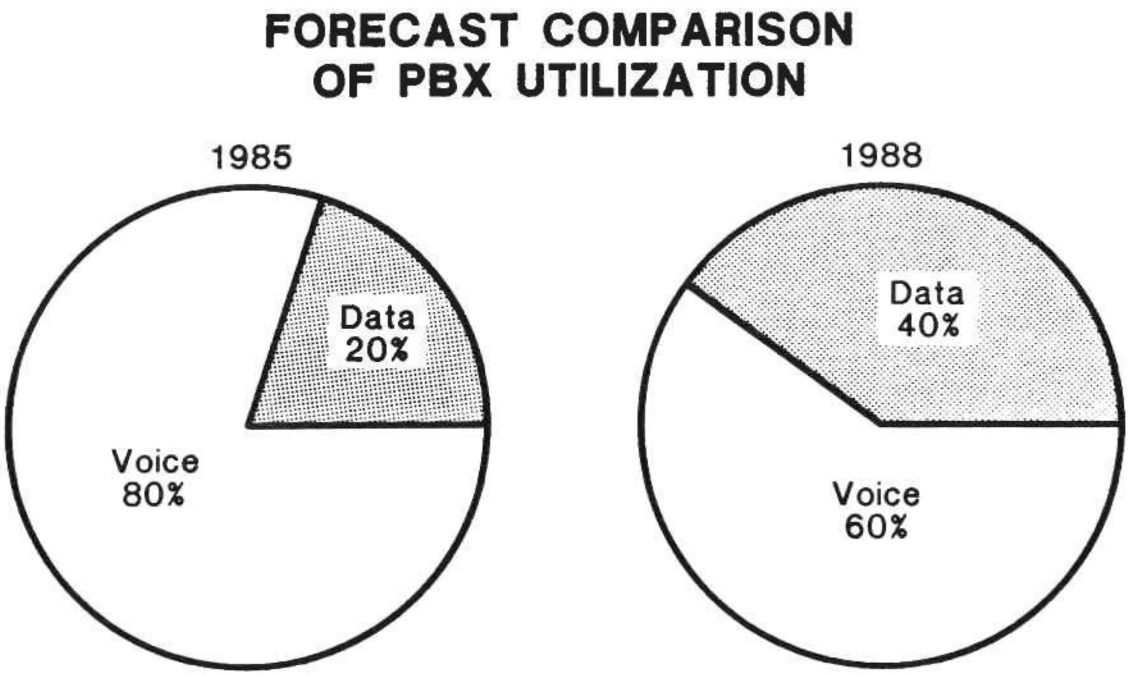
Figure 6



Source: Industry Statistics

Figure 7

ISDN PABX MARKET

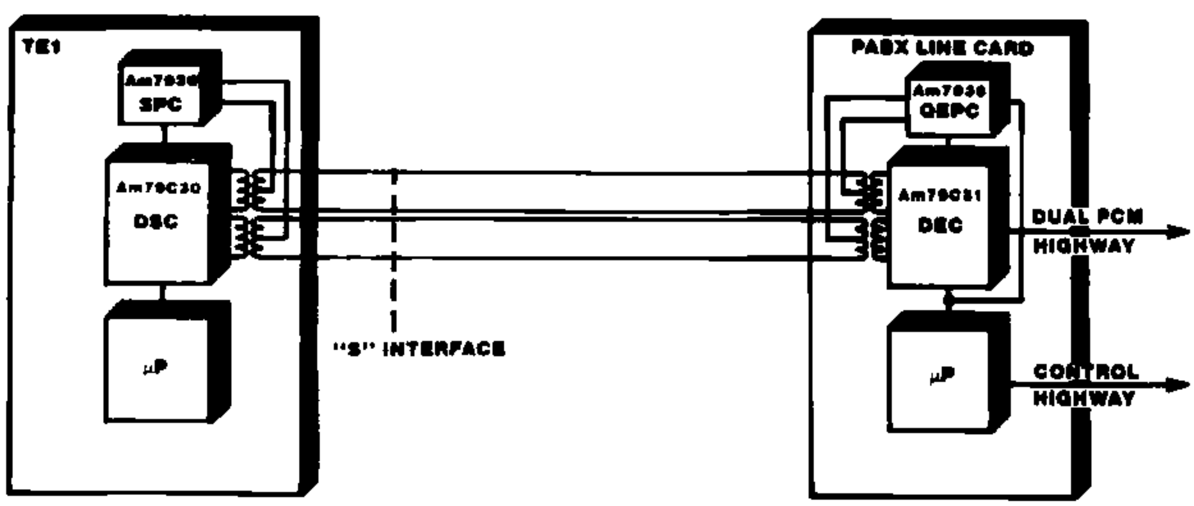
- 60% of PABX lines shipped in 1990 will be ISDN
  ≈20 million units (≈1984 SIA 16-bit μP market)

- There will be ≈2.5 terminals/PABX line
  ≈50 million units in 1990

∴ Total PABX market ≈70M units in 1990

Figure 8

4-WIRE APPLICATIONS



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THE CHANGING ENVIRONMENT OF MASKMAKING

A. Travis White
Vice President
Materials, Logistics,
and Systems
LSI Logic Corporation

Mr. White is Vice President of Materials, Logistics, and Systems for LSI Logic Corporation. He also serves on the Board of Directors for Master Images and is a member of the Executive Technical Advisory Committee for the Semiconductor Industry to the Department of Commerce. Prior to joining LSI, Mr. White was Director of Central Operations at Honeywell's Solid State Product Center in Colorado Springs, Colorado. He has also held various management positions in operations and central operations at Fairchild Semiconductor and Texas Instruments. Mr. White received a B.S. degree in Chemistry and Biological Sciences from the University of Texas at El Paso and has done graduate work in management at the University of Santa Clara.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
October 20-22, 1986
San Diego, California

THE CHANGING ENVIRONMENT OF PHOTOMASK MANUFACTURING

A. Capital Equipment Required and the Associated Cost of that Time Period

1. Total Manufacturing Investment for One Machine in Each Category

	1975	1980	1986
a. Lithography Equipment	Lead Screw Photorepeater	Laser Metered Photorepeater	Electron Beam Exposure System
Total:	$300k	$700k	$3,000k

2. Total Quality Assurance Investment for One Machine in Each Category

	1975	1980	1986
a. Critical Dimension Inspection	Manual Image Shearing	Automatic Video	Automatic Laser
b. Registration Inspection	Optical Overlay	Optical Overlay	Automatic Laser
c. Defect Inspection	2.0 micron capability	1.0 micron capability	.5 micron capability
Total:	$300k	$500k	$2,000k

B. Average Total Selling Price for a Photomask by Time Period

1. Average Total Selling Price of Combined Services*

1975	1980	1986
$700	$1100	$1450

*This is a weighted average selling price based on the following:
   a. product type (e.g., 1x stepper reticles, 1x projection arrays, 5x stepper reticles).
   b. manufacturing method (i.e., electron beam vs. optical photorepeater) and the associated average selling price.

c. non-standard quality assurance requirements associated with unusual or demanding specifications.

In the past each individual photomask represented a unique layer of the integrated circuit. This is changing today for many semiconductor manufacturers. A trend toward creating a single photomask with multiple layers of a device is well under way and could substantially alter the total cost and cycle time of this critical product and service.

THE CHANGING ENVIRONMENT OF PHOTOMASK MANUFACTURING

The American Photomask Manufacturer, the Present

Performance vs. Foreign Competition

Manufacturing Cycle Time

The competitive environment of the semiconductor market place has driven down the cycle time of both manufacturer and supplier/vendor to a point not thought to be attainable a few years ago. In the past, the majority of the American commercial photomask manufacturers quoted a standard cycle time of 10 to 15 working days. Limited capacity and manufacturing capability combined with a voracious market allowed only a minimal improvement into the beginning of the 1980's.

Today that situation is dramatically different. The major American maskmakers have concentrated on reducing the cycle time to as little as 48 hours in some cases. They have accomplished this primarily through installing additional capacity, higher productivity and streamling the entire process from order entry to final shipment. The result is that off-shore foreign competitors are locked out of this rapidly expanding segment of the photomask market.

Product Quality

Like his IC manufacturing customer, the American photomask manufacturer was perceived as a much lower quality supplier than his foreign counterpart until the recent past. However, that gap has virtually disappeared for most of the major consumers of photomasks in the United States. Today, commercial American photomask makers deliver a product that is world class in quality and performance where-ever a user performs sophisticated incoming inspections and judges his vendors in a formal rating and ranking system.

Responding to the American IC Manufacturer's Needs

Along with dramatically reduced cycle time and significant improvements in quality, the American photomask manufacturer has also had to address the challenge of producing geometry sizes and line widths approaching one micron and below. As one scientist puts it, "we are faced with the fundamental granularity of the universe." In addition to incredibly small feature sizes, the IC manufacturers have begun utilizing wafer stepping lithography as a major manufacturing tool resulting in the need for 1x and 5x stepper reticles, a photomask product which can only be manufactured with a multi-million dollar electron beam exposure system. Along with the required investment in manufacturing capability comes an additonal high dollar investment in more sophisticated inspection techniques such as the ability to compare the actual database information to the final photomask product.

The major American commercial photomask manufacturers have responded by expending the capital to install the necessary base of equipment and personnel to meet this expensive and decidedly more complex task on a daily basis for virtually every major IC manufacturer, again essentially shutting out all foreign competition.

The Birth of Partnership

The American photomask manufacturer has evolved into a true participant in the partnership situation so necessary for the success of the American semiconductor industry in the current business environment. In the recent past, all of the successful major independent suppliers of photomasks have forged alliances with either important customers or equipment suppliers resulting in the American photomask industry being a stronger and more cohesive vendor group than ever before.

THE CHANGING ENVIRONMENT OF PHOTOMASK MANUFACTURING

The American Photomask Manufacturer, the Future

The Transition from Optical Lithography to Electron Beam

It is clear to most of the major American IC manufacturers that their current and future photomask needs can be met only by the use of electron beam lithography or some even more advanced exposure system in the future. This will make it necessary for both the IC manufacturer and the photomask maker to reach new levels of sophistication in IC layout, data preparation, and all areas of interface in regard to the specification, order entry, and manufacture of photomask products.

Reducing Cycle Time

Data Transmission

The use of satellite data transmission and other more advanced methods of moving enormous amounts of both primary die data and order information will be developed and brought on line to achieve cycle times of 12 to 24 hours in the future.

Quality, Process Control

Higher internal yields resulting from more advanced process controls at the photomask manufacturer will be necessary to further reduce cycle time and improve the consistency of delivery to the end user. Formalized statistical process control programs are already underway at some of the major independent photomask manufacturers and most already have genuine quality improvement programs implemented which they will continue to refine into the future.

Reduced Inspection

As a matter of course, reduced inspection at both the photomask maker and his customer will come about because of the intense efforts of the maskmaker in regard to higher quality and process control. An audit situation will be the method by which both supplier and customer will judge and maintain vendor quality performance and achieve the desired cycle times for American IC manufacturers to be competitive in the market place of the future.

The Cost

While the portion of the cost of an IC layer that the photomask represents will always be under the pressure of the competitive environment, an increase in price is almost a certainty because of the relationship between cycle time and capacity. To achieve the necessary cycle time of 12 to 24 hours or less, enormous amounts of equipment and personnel must be in place to respond effectively and consistently to the demands of the IC manufacturer who in return is responding to the pressures of his own market place.

Strategic Alliances

The partnerships already formed, as well as those to come, will become more intimate and demand more of both participants in the future. The traditional adversarial relationships of the past will have no place in the intensely competitive world market place of tomorrow. We will be truly global competitors and a responsive infrastructure of vendor and customer will be an absolute necessity for success.

Attitude

The American photomask manufacturer has achieved the results we see today by basically taking an old fashioned "can do" attitude toward the challenges presented to him over the last several years. If he is to maintain that momentum into the future his resolve, dedication, and resourcefulness must not waiver. The challenges to success will be even greater and more relentless and certainly global in scope as we press into the future at an ever accelerating rate.

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LITHOGRAPHY IN PRODUCTION THROUGH 1922

Aubrey C. Tobey
Vice President
Micronix Corporation

Mr. Tobey is Vice President of Micronix Corporation with worldwide responsibility for sales and service. Since 1965, he has been involved in the evolution of microlithography technologies as applied to the manufacture of semiconductor devices and circuits. Prior to joining Micronix, Mr. Tobey was the Vice President of Marketing for the IC Systems Group and a Corporate Vice President of the GCA Corporation. He has authored numerous articles and papers on microlithography and has served on various boards and committees. Prior to joining the semiconductor industry, he was involved in basic and applied research in the fields of fluid dynamics and heat transfer. Mr. Tobey received B.S. and M.S. degrees in Mechanical Engineering.

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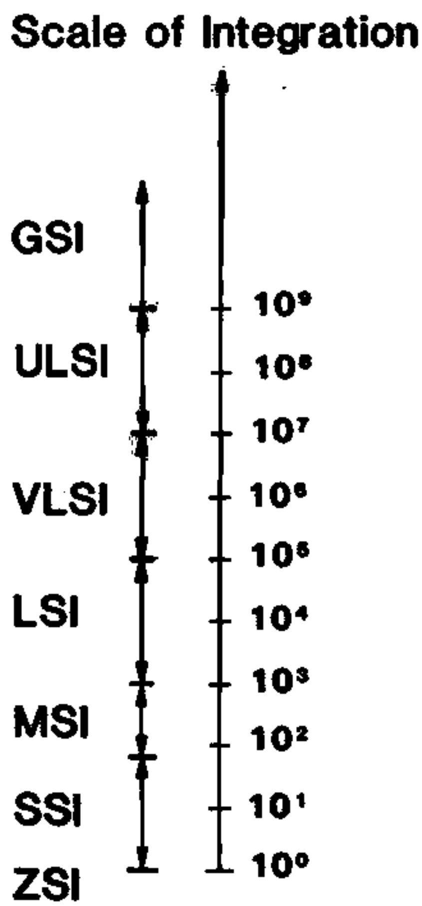
LITHOGRAPHY IN PRODUCTION THROUGH 1992

Aubrey C. Tobey, Vice President

Micronix Corporation
131 Middlesex Tpke., Burlington, MA 01803

FIGURES:



Source: J.D. Meindl

Figure 2

DEVICE FORECAST

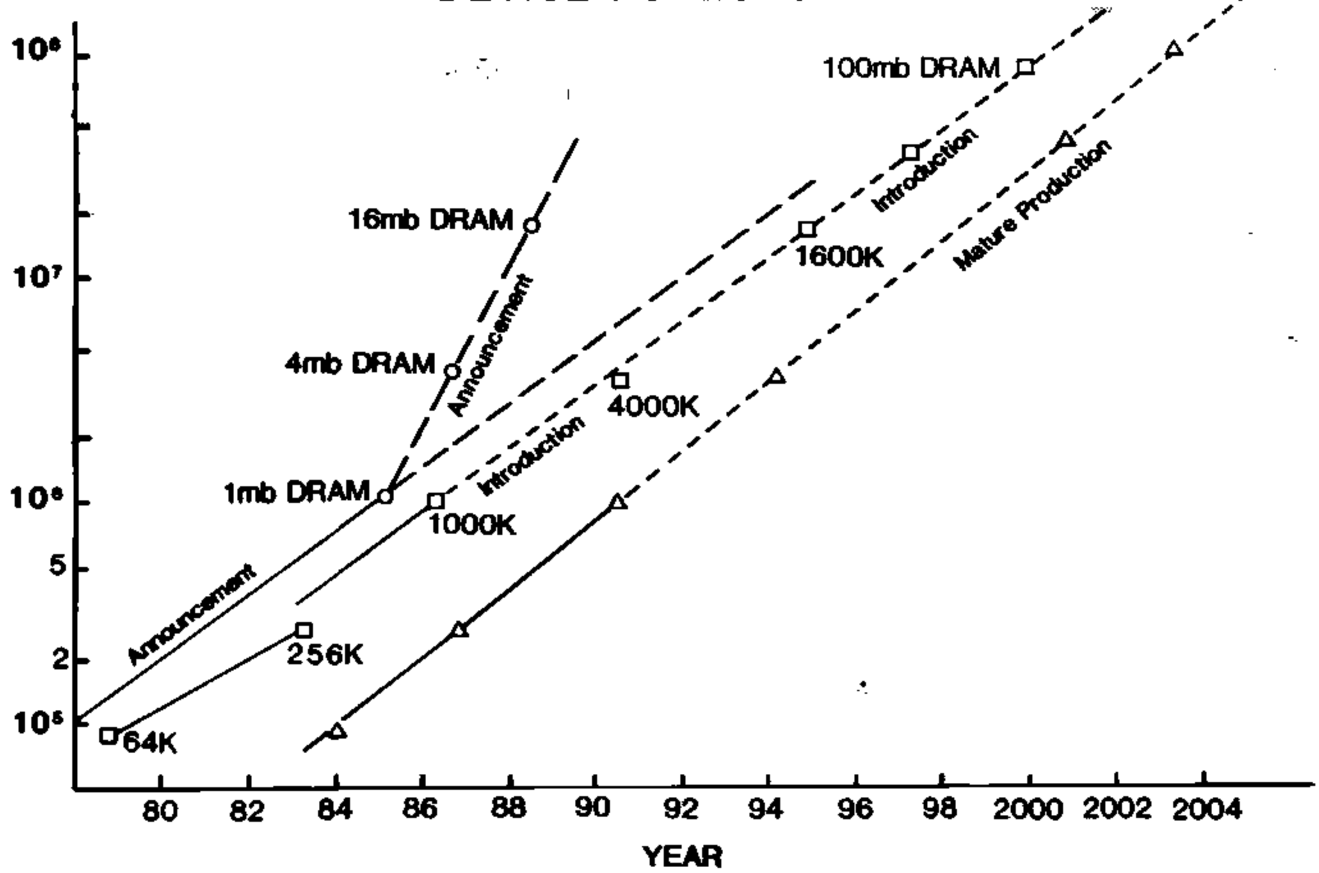
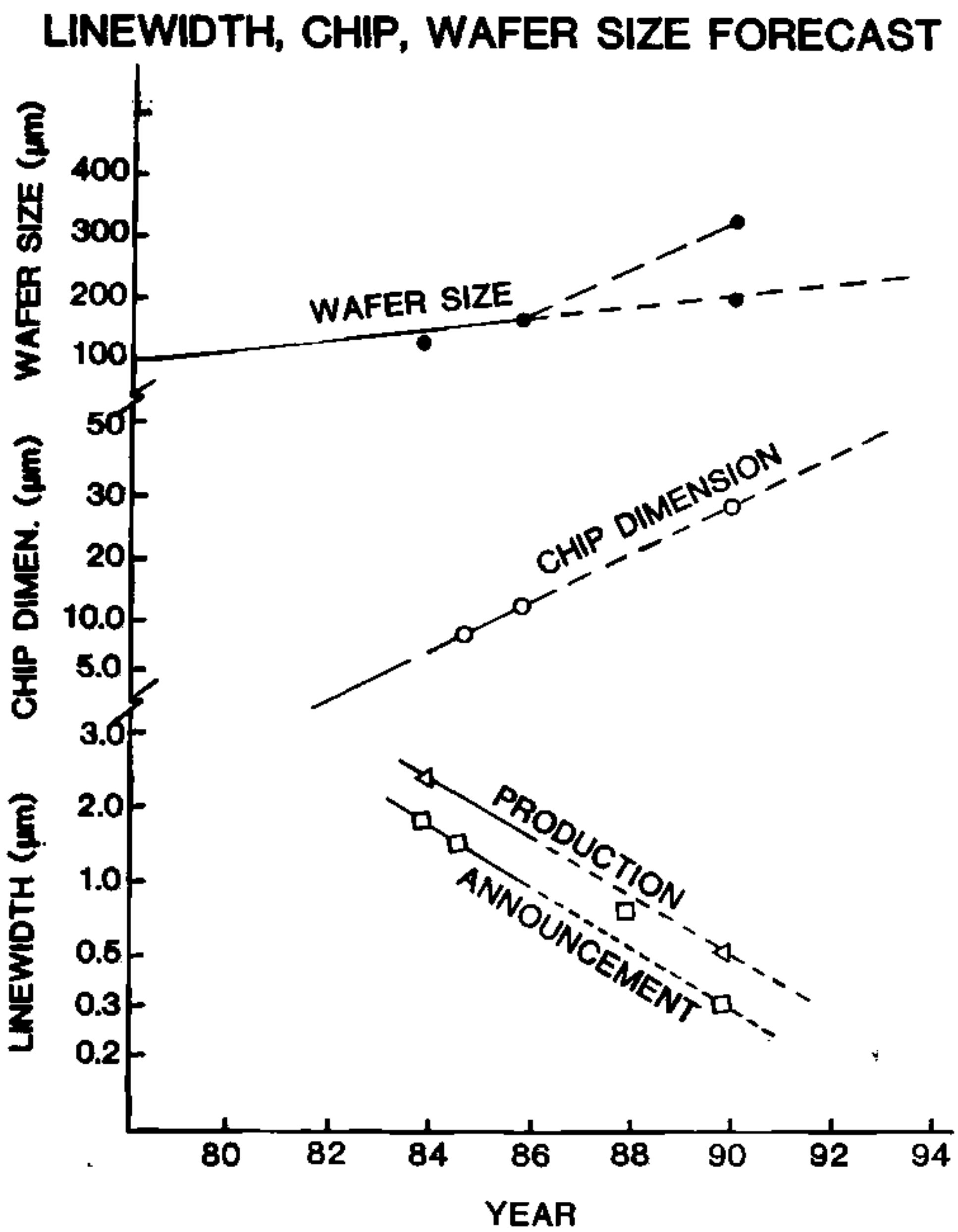
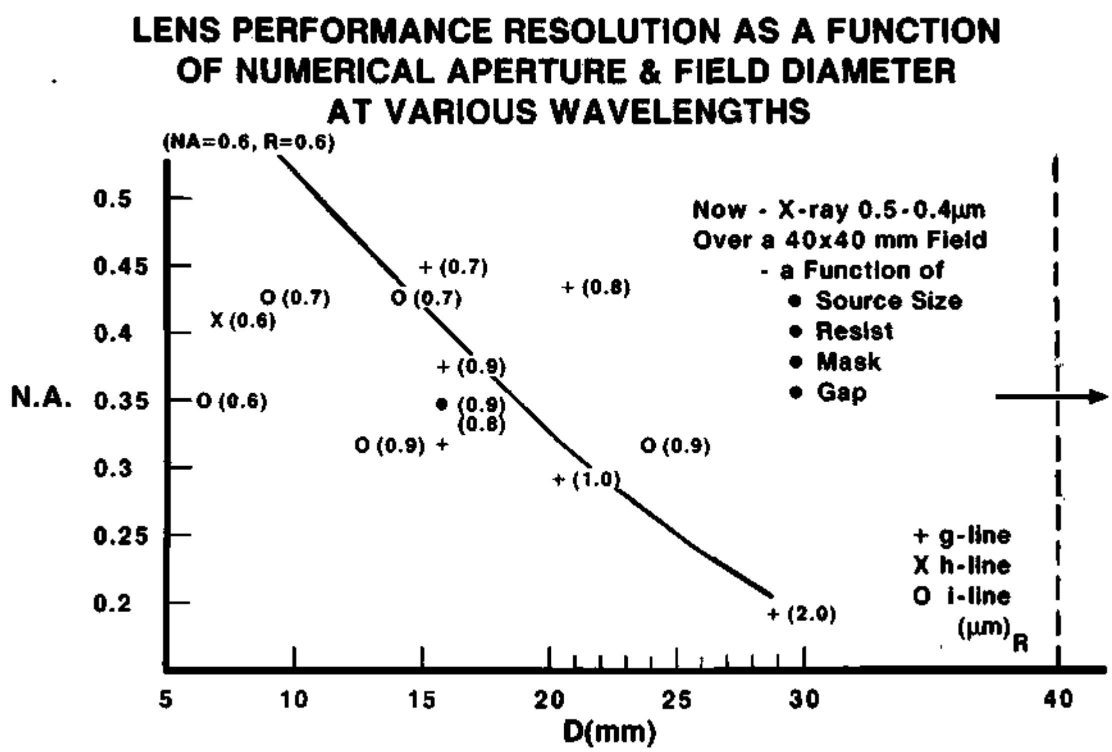
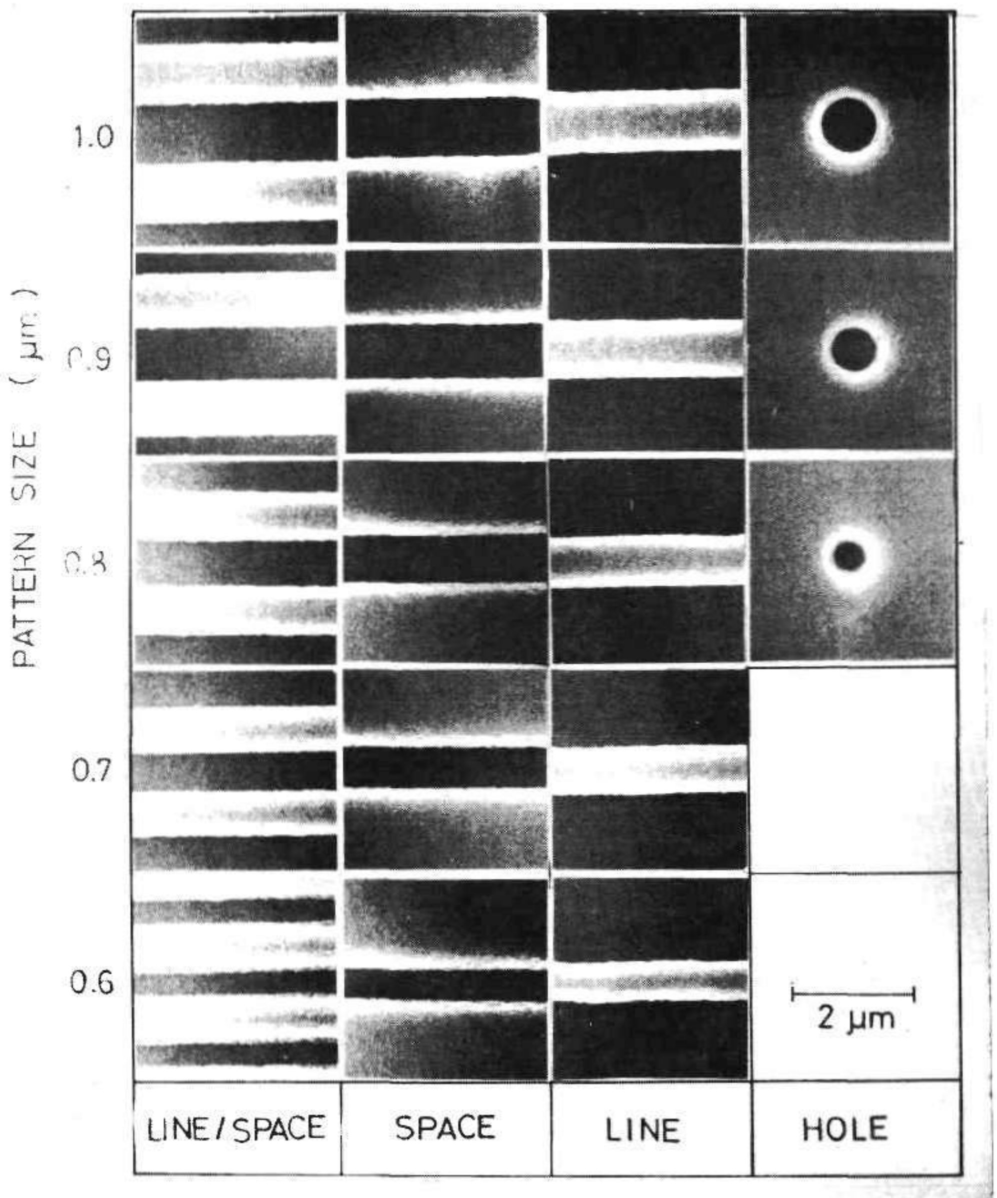


Figure 3



LINEWIDTH, CHIP, WAFER SIZE FORECAST
WAFER SIZE (μm)
CHIP DIMEN. (μm)
LINEWIDTH (μm)
400
300
200
100
50
30
20
10.0
5.0
3.0
2.0
1.0
0.5
0.3
0.2
WAFER SIZE
CHIP DIMENSION
PRODUCTION
ANNOUNCEMENT
80
82
84
86
88
90
92
94
YEAR


LENS PERFORMANCE RESOLUTION AS A FUNCTION
OF NUMERICAL APERTURE & FIELD DIAMETER
AT VARIOUS WAVELENGTHS
(NA=0.6, R=0.6)
N.A.
0.5
0.45
0.4
0.35
0.3
0.25
0.2
+ (0.7)
O (0.7)
O (0.7)
+ (0.8)
X (0.6)
+ (0.9)
O (0.6)
● (0.9)
(0.8)
O (0.9) +
O (0.9)
+ (1.0)
+ (2.0)
Now - X-ray 0.5-0.4μm
Over a 40x40 mm Field
- a Function of
● Source Size
● Resist
● Mask
● Gap
+ g-line
X h-line
O i-line
(μm)R
5
10
15
20
25
30
40
D(mm)


PATTERN SIZE (μm)
1.0
0.9
0.8
0.7
0.6
2 μm
LINE / SPACE
SPACE
LINE
HOLE

MASK PERFORMANCE CRITERIA FOR $\leq$0.5 μm MINIMUM GEOMETRIES

	Needed	Commercial Availability
Flatness (μm)	0.3-0.9	0.3-1.2
Distortion (μm) w/Absorber	<0.1	0.2-0.4
Defects (per cm^2)	0.1-0.3	~ 1.0
Stability	Long Term	Long Term
Transmission (633nm)	40-60%	40-60
Stress (dynes/cm^2)	8×10^8	8×10^8
Youngs Modulus (dynes/cm^2)	2×10^{12}	$\sim 9 \times 10^{11}$

MICRONIX

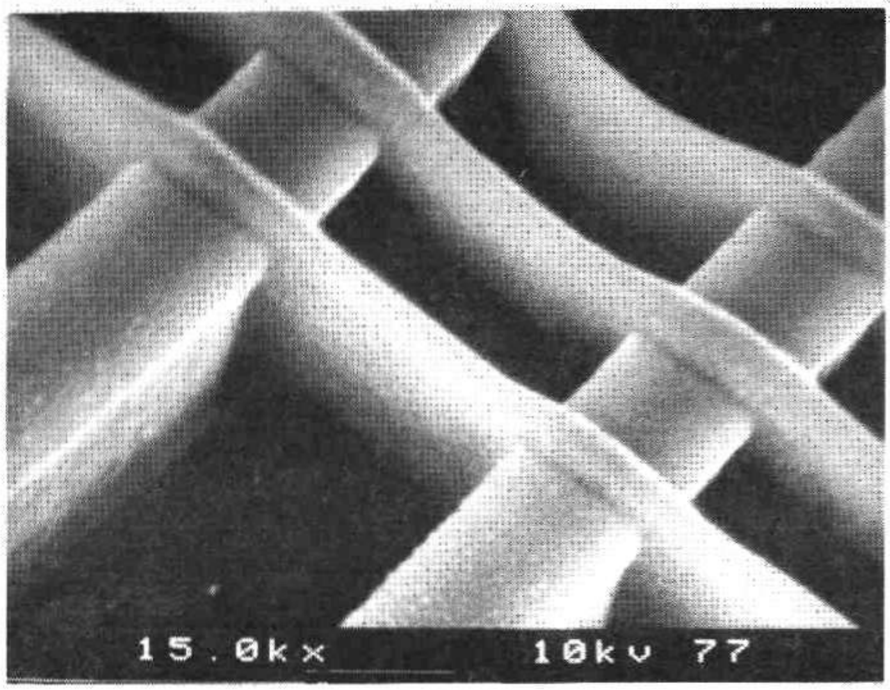


Figure 7(a)

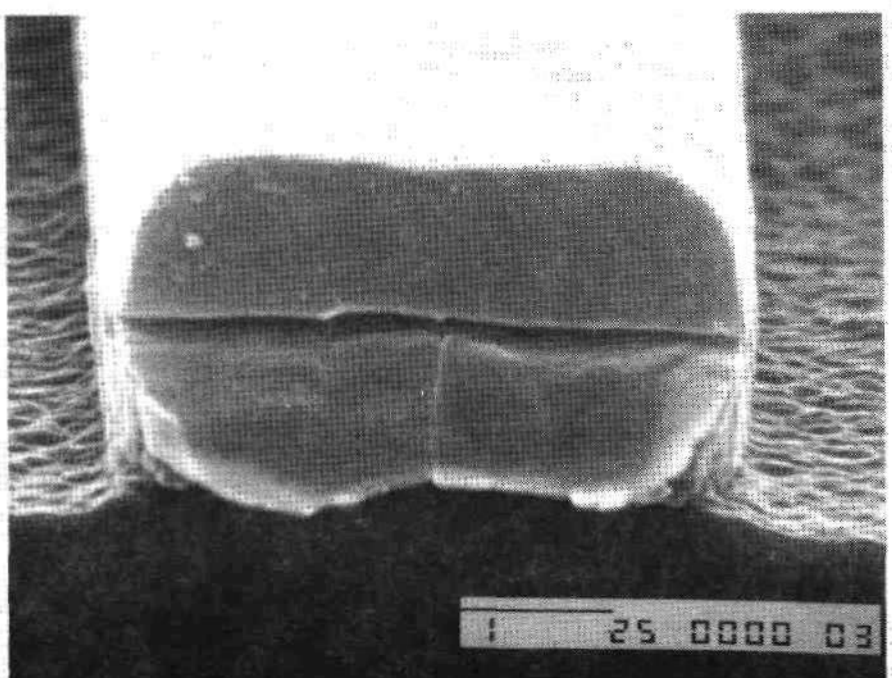
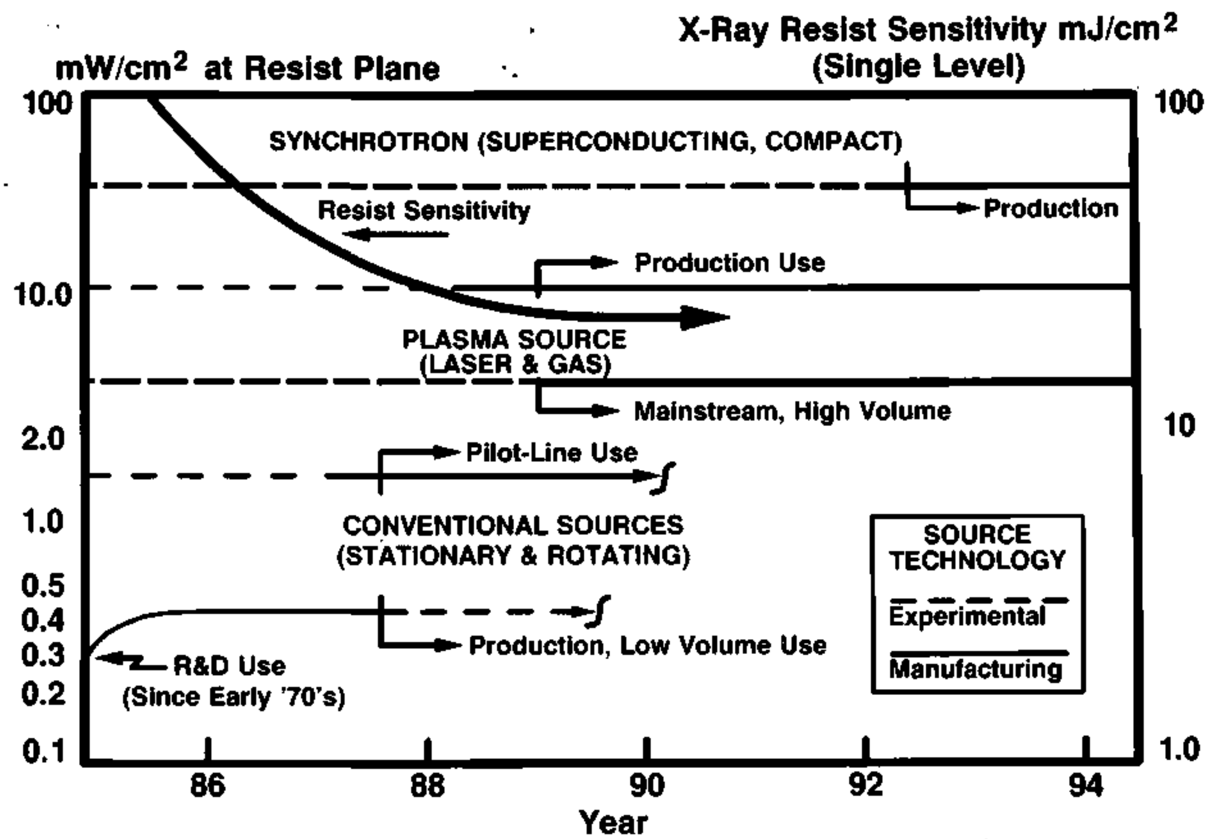


Figure 7(b)


X-Ray Resist Sensitivity mJ/cm2
(Single Level)
mW/cm2 at Resist Plane
100
10.0
2.0
1.0
0.5
0.4
0.3
0.2
0.1
100
10
1.0
SYNCHROTRON (SUPERCONDUCTING, COMPACT)
Production
Resist Sensitivity
Production Use
PLASMA SOURCE
(LASER & GAS)
Mainstream, High Volume
Pilot-Line Use
CONVENTIONAL SOURCES
(STATIONARY & ROTATING)
SOURCE
TECHNOLOGY
Experimental
Manufacturing
Production, Low Volume Use
R&D Use
(Since Early '70's)
86
88
90
92
94
Year

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FUTURE DRY ETCH TRENDS FROM A PROCESSING PERSPECTIVE

Dr. David N.K. Wang
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Dr. Wang is Director of Advanced Technology for Applied Materials, Inc. Before joining Applied Materials, he worked at Bell Laboratories where he did various semiconductor processing work. Dr. Wang received the 1983 Semiconductor International Award for the Advancement of Semiconductor Technology in the Development of the Hexode Type R/E Reactor. He received a Ph.D. degree in Materials Science from the University of California at Berkeley and did research in power metallurgy and high-temperature electroscopy at Lawrence Radiation Laboratory. Dr. Wang holds numerous semiconductor processing patents in the field of plasma etc.

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FUTURE TRENDS IN PLASMA ETCH PROCESSING

David N.K. Wang

Director of Advanced Technology

Applied Materials, Inc.

VLSI technology is making increasing demands on etching equipment and processes. The focus of this presentation is to outline some of the challenges and their impact on etch processing.

The table compares the design rules and structures used in DRAM devices from 64K to 4 megabit (Figure 1). Memory devices are the mainstream of semiconductor industry manufacturing and, thus, represent the most sophisticated technology trends. The design rule for 64K is roughly 2.5-3.0 microns, and for 256K, 1.5-2.0 microns, and 1.0 micron for one megabit. For DRAMs larger than one megabit, submicron lines will be used. Conventional metallization is a single level aluminum. It will become two to three levels as device density increases. The gate oxide, which is the dielectric material underneath the interconnect, started with 500 Angstroms thickness for 64K and will gradually decline to below 100 Angstroms for four megabits. There will also be a structural change in the storage capacitor, from the conventional plate structure into a buried or vertical capacitor. This structure requires etching into the single-crystal silicon substrate.

Figure 2 illustrates some of the VLSI device characteristics. Because we are dealing with one-micron or below, dimensional and profile control are essential. Polycide films, a multilayer gate conductor consisting of a refractory metal silicide over polysilicon, represent some material challenges for both deposition and etch. Structures such as buried capacitors offer an opportunity to dramatically reduce device area while improving performance. Selectivity to the mask is needed for pattern resolution while selectivity to the underlayer allows overetching to remove any residues without destroying the underlayer. Selectivity refers to the ability to etch one material preferentially over another and is specified as an etch rate ratio. Particularly important in selecting, are the mask material and the underlying layers. Last, and equally important, is defect, or particle, control. Even if you can simultaneously meet all the above requirements, you will lose yield if you generate particles on your wafers. As device geometries shrink, the sensitivity to particles goes up exponentially.

In order to accomplish all of this, the trend in etch processing continues to move towards low pressure RIE, multi-step processing, clean chemistries and defect control.

LOW PRESSURE RIE

Pressure is a critical parameter for ion directionality and the characteristic ion energy. If ions are directionally perpendicular to the wafer surface, only the wafer surface is bombarded, not the sidewall; therefore, there will be no reaction or removal of material in the lateral direction. The voltage potential between the plasma and the electrode controls ion energy and directionality. The pressure determines the mean free path of an ion,

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which is defined as the average distance an ion will travel before colliding with another particle.

In a low-pressure environment, there will be a large mean free path, so it is easy to control the directionality of your ions. At high pressure, there will be a shorter mean free path; thus, more collisions of molecules and less directionality (Figure 3).

Low pressure also efficiently removes the etch byproducts so they do not inhibit the progression of the etch process. This is particularly important with smaller geometries, where the reactant species can complete with the etch byproducts, referred to as microloading effect. This causes a variability in etch rate with feature size across the wafer.

This side graphically represents the effects of process pressure when etching small features (Figure 4). For the etching process to proceed, the etch reaction products must be volatile and desorb from the etching surface so that new reactant species can adsorb on the newly exposed surface. Since the only advantage of high pressure operation is high etch rates, one can visualize the problem in confined spaces of 2 microns or less. The crowding of etch byproducts attempting to diffuse out, while the reactant species are attempting to diffuse in, becomes a real problem. This problem does not exist with low pressure etching, even at the sub-micron level, due to moderate etch rates, higher volatility of etch reaction products and a greater mean free path of the individual ions.

The negative impact of low pressure processing is an economic one. Generally lower pressure also reduces the etch rate. Batch systems have some advantage since they process more than one wafer at a time.

MULTI-STEP PROCESSING

Multi-step processing is becoming a necessity on current as well as future devices. The primary advantage is the ability to tailor the process conditions as the etch proceeds. Another advantage is the ability to adjust the chemistries to meet specific film imperfection or for in situ pre- or post-etch treatment.

The most obvious example for a multi-step process is a sandwich structure involving two or more layers. Figure 5 is an example of a polycide etch involving two layers: a polysilicon layer under a silicide layer, plus an interstitial layer that etches differently than either the polysilicon or the silicide. The emphasis will be on profile control of both layers without undercutting either layer. Once again, multi-step processing is essential to completely clear all the silicide material before proceeding to the polysilicon. A three-step process is often necessary to etch the polycide structure vertically without residues and without damaging the underlayer.

Figure 6 shows a 0.8um polycide structure etched over topography. Both layers were etched vertically without any dimensional change.

Single crystal silicon, although a homogenous material, still requires a multi-step process. The difficulty lies in simultaneously controlling a verticle profile, high fidelity mask replication, rounded bottom, no residues and uniform depth control over the entire wafer. With trench capacitors, you may have to open more than a million of them on each device over the entire wafer--and every one must be the same. Other considerations are process repeatability run-to-run, no device damage and reasonable throughput.

A vertical or slightly tapered sidewall is critical. Any bowing in the profile will present serious step coverage problems in subsequent deposition steps. In addition to profile, the shape of the trench bottom must be controlled. Sharp corners cause oxidation-induced stress and gettering sites for heavy metals.

The SEM shown in Figure 8 demonstrates the power of a low pressure system. 1u capacitor holes have been etched into single crystal silicon. Note the smooth sidewalls, tapered profile and rounded bottom.

The disadvantage of multi-step processing is again one of economics. Normally, additional process steps require more overhead time for system stabilization. A batch system can have some advantage since the etch and overhead time is shared evenly over the entire batch.

CLEAN CHEMISTRIES AND DEFECT CONTROL

An additional requirement for future devices will be better defect control. In this competitive market, semiconductor manufacturers must be concerned with the cost per good die, which is the total cost divided by yield. The bottom line will be controlling the number and size of defects in each critical mask level in order to maximize yield. A major source of contamination can be the processing equipment and the processes run in them.

Mechanically induced particulates are generally induced by wafer handling procedures, not from processing. If the wafer must be transported over a relatively long distance, or handled several times, it is almost certain that particles will occur. Turbulence is another important particle contributor as it can disturb existing particles in the system and contaminate the wafer. Load locked systems can be a partial solution to turbulence, but if they are not vented and pumped correctly, turbulence can still occur. To eliminate rough handling the wafer handler must be well designed; and the best design to date is a pick and place system using only edge contact on the wafer, not front side contact. Belts or tracks cannot be tolerated.

Process induced particles can be non-volatile etch products and/or byproducts, or they can be caused by moisture sensitive chemistries reacting with the atmosphere. An example of non-volatile products is the use of fluorocarbon chemistry to etch dielectrics, such as nitride, or oxide. It is desirable for some polymers to develop on the substrate during the overetch to protect the substrate. This polymer, even though organic, is a non-volatile material. If there is an excess of polymer (which in itself can cause contamination on the wafer) it accumulates in the system and can then flake off and cause contamination.

One way to avoid excess polymers is to optimize the chemistry. For example, you can ensure that the proper amount of oxygen has been included to reduce the formation of organic polymers, and there by reduce the accumulation of polymers in the system. Another way is to design the hardware to make removal of the polymers easy to accomplish, either by residual dry etch or by manual operation. Regardless of how its done, the main purpose is to reduce maintenance time and maintain system cleanliness. A clean system naturally reduces contamination.

The problem of moisture sensitive chemistries is a familiar one. When any polycrystylline material such as polysilicon or aluminum is etched, we use silicon tetrachloride or boron trichloride mixed with chlorine. $SiCl_4$ and BCl_3 are both very sensitive to moisture. If the etch system does not have high vacuum, and if moisture sensitive chemistries are exposed during the vent cycle, silicon oxide or boron oxide will be formed. SiO and BO become non-volatile products and another source of particles.

For moisture sensitive chemistries, a high vacuum system, load lock, and temperature control are needed. Whenever silicon or aluminum are etched, silicon chloride or aluminum chloride are generated. These materials are not very volatile, which means that they have relatively low vapor pressures. In order to push them to the exhaust without accumulation in the system, the temperature in the system must be raised so that non-volatile or semi-volatile etch products do not condense.

SIDEWALL-FORMING CHEMISTRIES

What is meant by sidewall protection? If the etching mechanism is predominantly a chemical reaction, then ion bombardment is not very helpful in terms of profile control. Most of the time we rely on a sidewall formation which can isolate the reactive species from the already etched sidewall material to prevent lateral etch and its resulting undercutting. There are two ways to do this: with an inorganic or with an organic chemistry (Figure 9).

1) In a low pressure plasma etch, you would not intentionally select a chemistry which makes a very thick protective sidewall. You might, however, choose an inorganic recombinant mechanism. For example, if pure chlorine is used in aluminum etch, you may get gross undercutting; but if the chlorine is mixed with boron trichloride gas in the appropriate concentration, you can achieve good anisotropy. Boron trichloride decomposes into different grades of boron chloride, which can be adsorbed on the surface of the already-etched profile. Once it is adsorbed there, it will partially recombine with low-grade boron chloride into boron trichloride whenever the reactive chlorine neutrals or free radicals come to the surface. Using this method you can isolate your already-etched profile from the reactive species to gain good anisotropy.

2) The second technique typically applies in a high pressure plasma etch in which an organic sidewall mechanism is relied upon for anisotropy. To do this, the etchant gas must be doped with a polymer forming gas. For example, some processes use $CHCl_3$ or CCl_4 mixed with chlorine or with silicon tetrachloride, forming organic polymers which will start to accumulate on the sidewall. Since this polymer is not in recombinant form, it accumulates thicker and thicker. Later on, this build-up is very difficult to remove and the sidewall can fall onto the substrate once the resist is stripped (Figure 10), since it cannot be satisfactorily stripped away with oxygen. The sidewall is not a pure organic material, it is a mixture of organic material, polymer, and waste etch product, and will certainly cause contamination on your device.

Figure 11 is a diagram showing a post-etch residue resulting from "protective" sidewall chemistry. When etched to end point, all the material will be removed by the plasma etch, but a polymer sidewall will form around the mask and along the etch profile. Vertical steps will also accumulate a sidewall from the protective polymers. Once the sidewall is removed during overetch, you may find some reverse undercutting and a sidewall remaining as a residue. Figure 12 shows a very clear example: aluminum etched over topography using a polymer former as a protective sidewall. As shown, the sidewall does not completely touch the etched profile. It is free standing and can be a very severe contamination source.

<u>Corrosion</u> is another form of contamination that is the result of etch residues. When we discuss corrosion, we always talk about aluminum etch. Since fluorinated chemistry cannot be used to etch aluminum, chlorinated chemistry must be used. The corrosion is produced or induced due to the reaction of residual chloride with moisture when the wafer is exposed to the ambient, after processing. Chloride reacts with any moisture in the ambient to form HCl which will later attack the fresh aluminum and produce aluminum chloride and/or copper chloride. Copper chloride has a much lower vapor pressure than aluminum chloride, so it is even more difficult to remove.

Aluminum is difficult to etch anisotropically if you don't have the right system, and if you must rely on a polymer protective sidewall technique. As the polymer is formed, chlorine species are trapped inside the sidewall and when released will react with moisture, form HCl, and attack the aluminum.

Figure 13 is an example of corrosion due to the aluminum chloride residue and it is safe to say that copper chlorides are even more corrosive.

How do we treat or eliminate corrosion? If you can achieve residue-free etching, you will have solved much of the problem. However, if you have a little bit of residue, or want to ensure that there will be no corrosion in the long-term, there are several alternatives: You may want to try fluoride substitution. We know that aluminum fluoride is somewhat more dynamically stable than aluminum chloride, so if the wafer is treated after etch with some fluorinated species in the chamber before they are exposed to ambient, you may be able to convert a very thin layer of chloride or chloride residue into fluoride compounds, making it inert to moisture. Another method is to deposit a thin organic polymer in situ after etch, which will passivate or isolate your wafer from the ambient. This passivation layer is easily stripped with the photoresist after etching.

Certainly there are many other forms and sources of contamination such as sputter/redeposition, black silicon, incomplete etch or the wafer itself which may be beyond the scope of our talk today.

<u>FUTURE EQUIPMENT TRENDS</u>

There are predominantly two configurations of plasma etch equipment, and they differ essentially in pressure range and electrode configuration. The first configuration, referred to as a planar plasma reactor, consists of two electrodes, usually a single-wafer chamber, and operates a high pressure (0.5-2.0 torr). The electrode size, anode and cathode, are the same, so it is called a symmetrical system. Additionally, the electrodes are closely spaced and operate at a very high power to increase the plasma potential. Inherent in this design are the basic limitations of single-wafer systems. In order to maintain productivity, the system must etch one wafer very fast, often at the expense of other etch requirements.

The other type of etch system is an asymmetrical system, which also has two electrodes, but the cathode is smaller than the electrode. These machines are typically low pressure ($\leq$ 0.1 torr), batch-type systems. Low-pressure systems have a lower concentration of reactants, so are less chemical; i.e., they are more directional but at a lower etch rate. The batch system compensates for the lower etch rate by sharing the process time over a number of wafers.

Single wafer systems now and in the future will focus on performance improvements and rate enhancements to offset the lower etch rates associated with low pressure processing. One approach involves multi-chamber systems while others involve new technologies. Triode, magnitron and ECR are all contenders, each exhibiting its own strengths and weaknesses. At this time there is no clear winner.

Batch RIE trends are focused on its traditional weaknesses; automation and fab integration, plus an additional emphasis on cleanliness.

New generation batch RIE systems are available with full automation, load locked, and designed with a flush-mount clean room interface.

In conclusion, all critical etch processing will continue towards low pressure RIE processing. This will be true regardless of single-wafer or batch configuration. Furthermore, it is anticipated that there will continue to be a role for both configurations on VLSI and ULSI fab lines of the future. The final decisions on which configuration is most applicable will be decided by performance and economic considerations for each specific application.

TRENDS OF DRAM PROCESS TECHNOLOGY

	64K	256K	1 M	4 M
DESIGN RULE (μm)	2.5 ~ 3.0	1.5 ~ 2.0	1 ~ 1.3	0.7 ~ 1.0
OVERLAY (μm)	1 ~ 1.2	0.6 ~ 0.7	0.3 ~ 0.4	0.2 ~ 0.3
Al PITCH (μm)	6.5 ~ 7.5	4.5 ~ 5.5	2.5 ~ 3.0	1.5 ~ 2.0
METALLIZATION	SINGLE LEVEL	SINGLE LEVEL	2 LEVEL	3 LEVEL
GATE OXIDE (Å)	500	350	200	100 ~ 150
GATE CONDUCTOR	POLY SILICON	POLYCIDE (4 ~ 10 Ω/□)	POLYCIDE/ PURE METAL	PURE METAL (<1 Ω/□)
STORAGE CAPACITOR	CONVENTIONAL STRUCTURE	CONVENTIONAL STRUCTURE	BURIED CAPACITOR	BURIED CAPACITOR
DEVICE STRUCTURE	SINGLE DRAIN	DOUBLE DRAIN	DOUBLE DRAIN	DOUBLE DRAIN

248-2

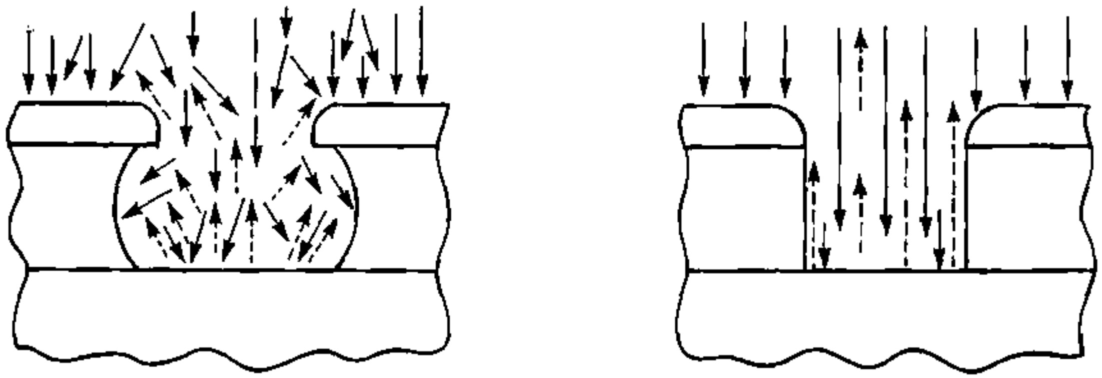
FIGURE 1

VLSI DEVICE CHARACTERISTICS

- DIMENSION/ PROFILE CONTROL
- NEW MATERIALS
- NEW STRUCTURES
- SELECTIVITY
- DEFECT CONTROL

FIGURE 2

INFLUENCE OF PRESSURE ON THE ETCH PROCESS



HIGH PRESSURE
(ION SCATTERING)

- MICROLOADING EFFECT ON SMALL GEOMETRIES
- LINEWIDTH LOSS

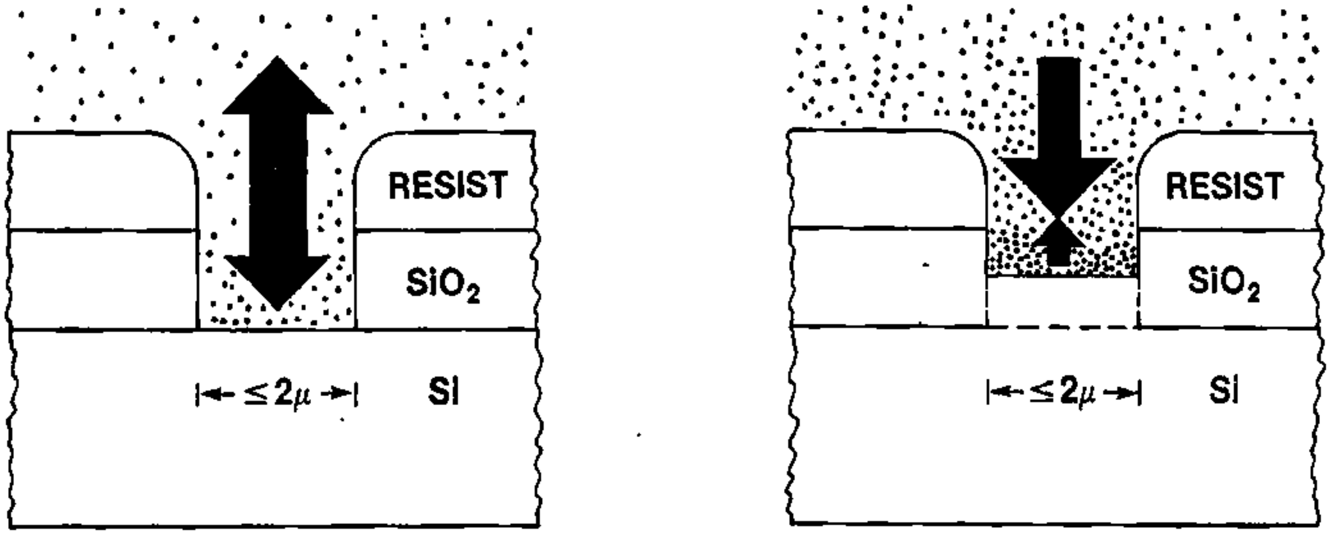
LOW PRESSURE
(DIRECTIONAL ION)

- EFFICIENT REMOVAL OF ETCH BY-PRODUCTS
- PRECISE PATTERN REPLICATION

338-04

FIGURE 3

EFFECTS OF PRESSURE ON NARROW FEATURES (PROXIMITY EFFECT)

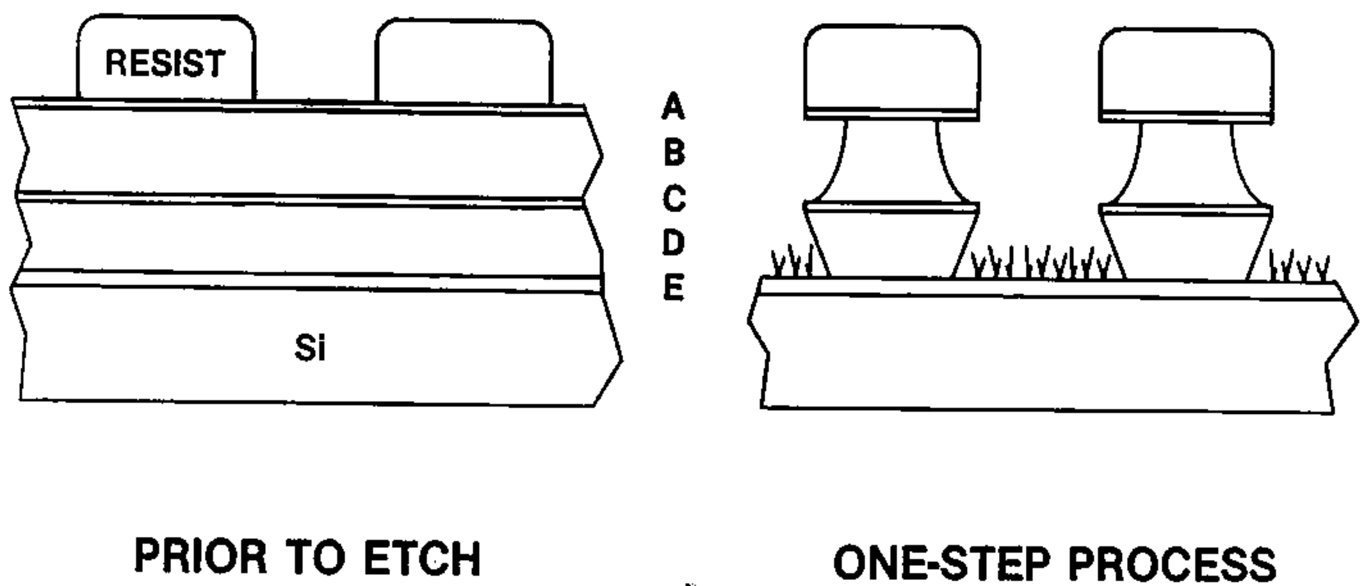


LOW PRESSURE	HIGH PRESSURE
• MODERATE ETCH RATE	• HIGH ETCH RATE (INITIALLY)
• EFFICIENT BY-PRODUCT REMOVAL	• REMOVAL OF BY-PRODUCT IMPEDED
• ETCH PROCEEDS UNIFORMLY	• ETCH STALLED

338-234

FIGURE 4

THE IMPORTANCE OF MULTI-STEP PROCESSSING



338-110

FIGURE 5

0.8 μm POLYCIDE STRUCTURE ETCHED OVER TOPOGRAPHY

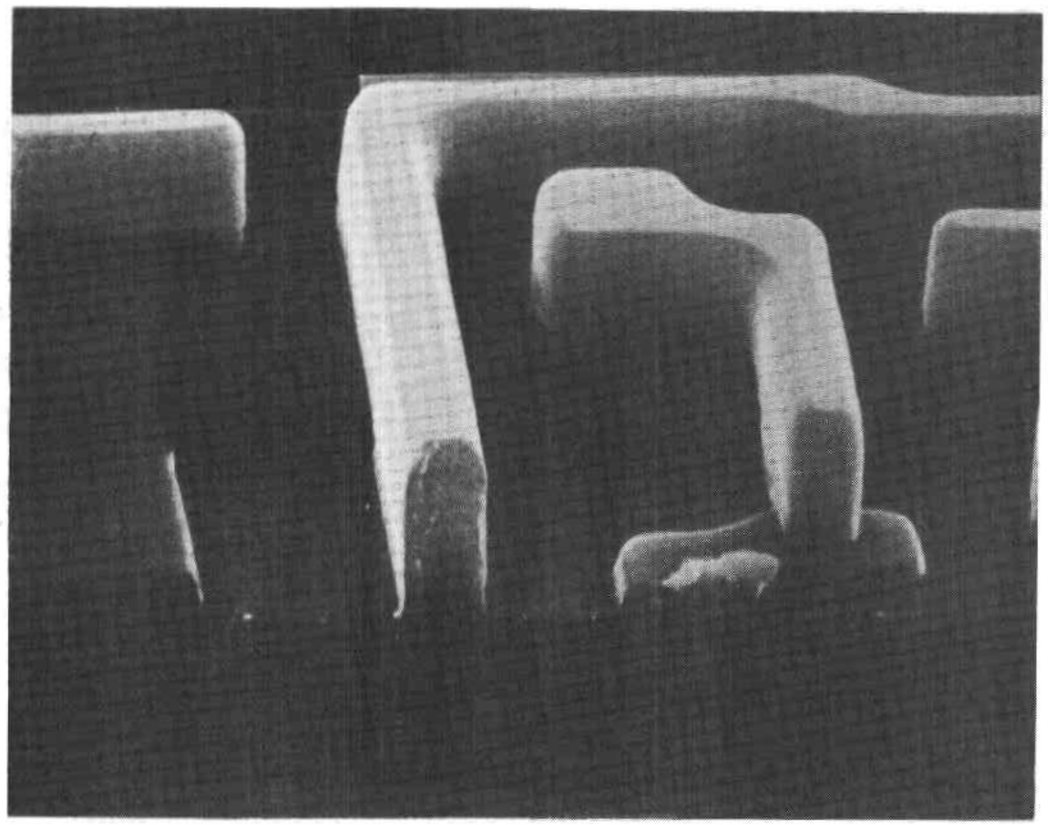


FIGURE 6

581-DW-35

IN SITU MULTIPLE STEP ETCHING FOR SINGLE LAYERS

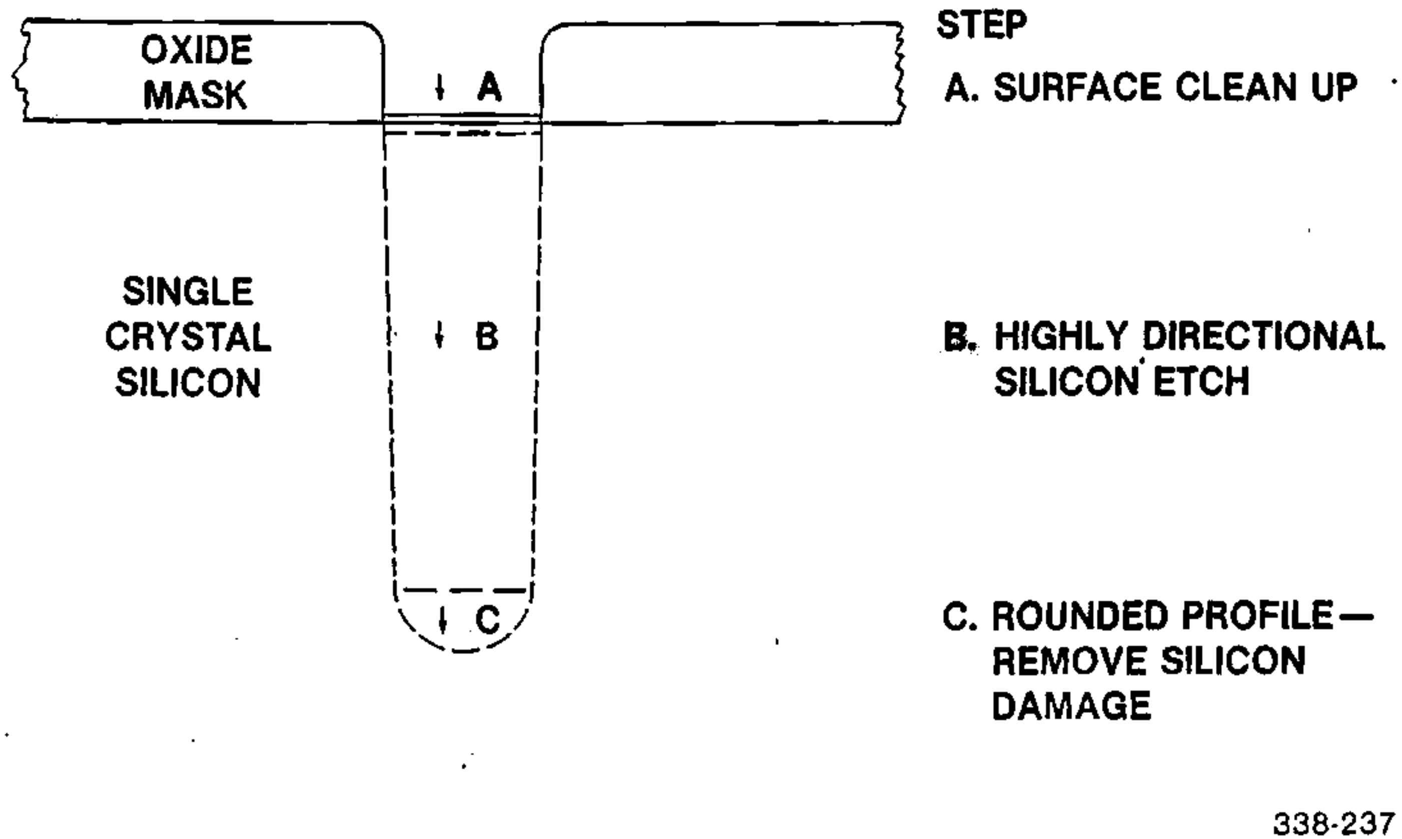
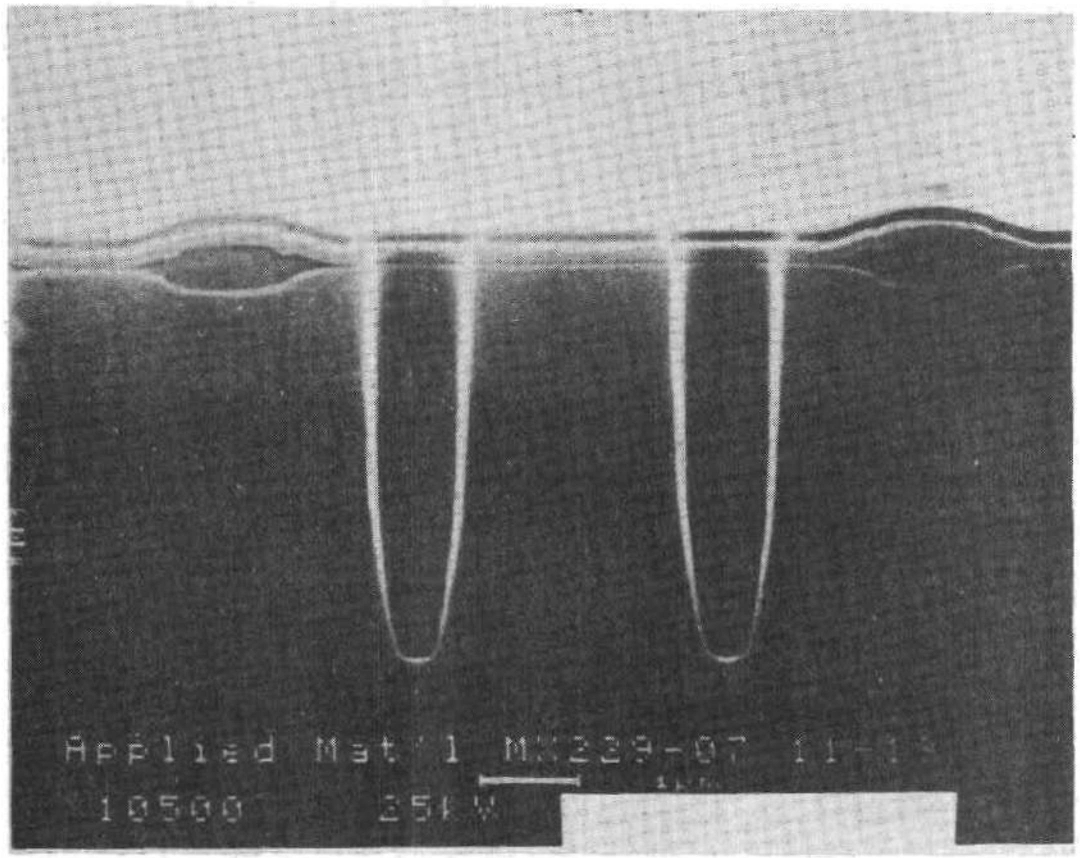


FIGURE 7

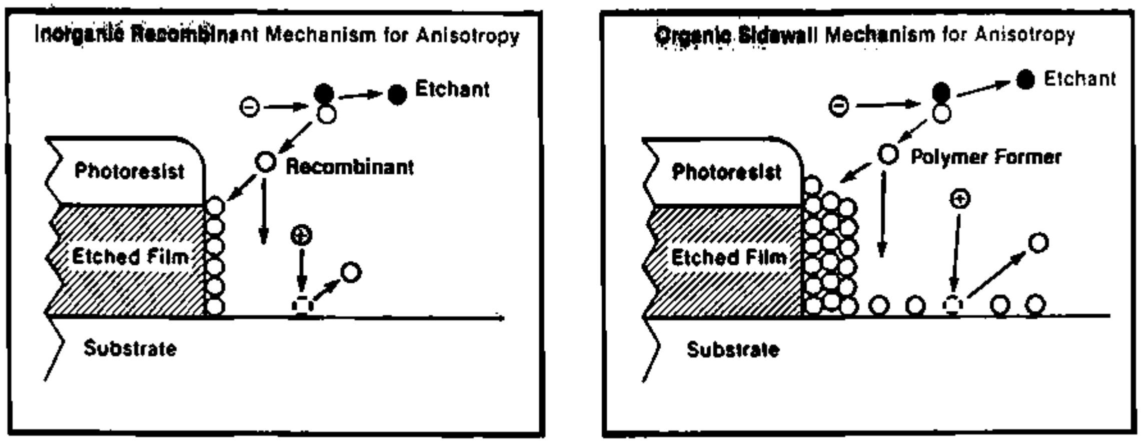
1 μm CAPACITOR HOLES ETCHED IN SINGLE CRYSTAL SILICON



547-06

FIGURE 8

INORGANIC vs ORGANIC MECHANISMS FOR ANISOTROPY

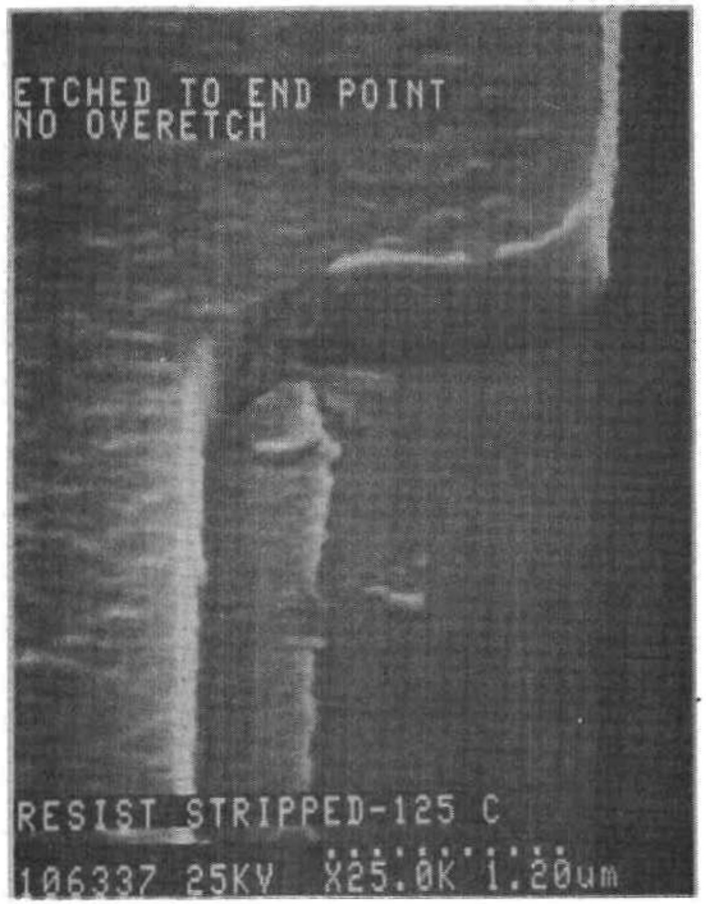


F981MW.11

646-11

FIGURE 9

ORGANIC PROTECTIVE SIDEWALL



581-DW-14

FIGURE 10

Dataquest, a company of The Dun & Bradstreet Corporation / 1290 Ridder Park Drive / San Jose, CA 95131-2398 / (408) 971-9000 / Telex 171973

PROBLEMS ASSOCIATED WITH "PROTECTIVE" SIDEWALL CHEMISTRIES

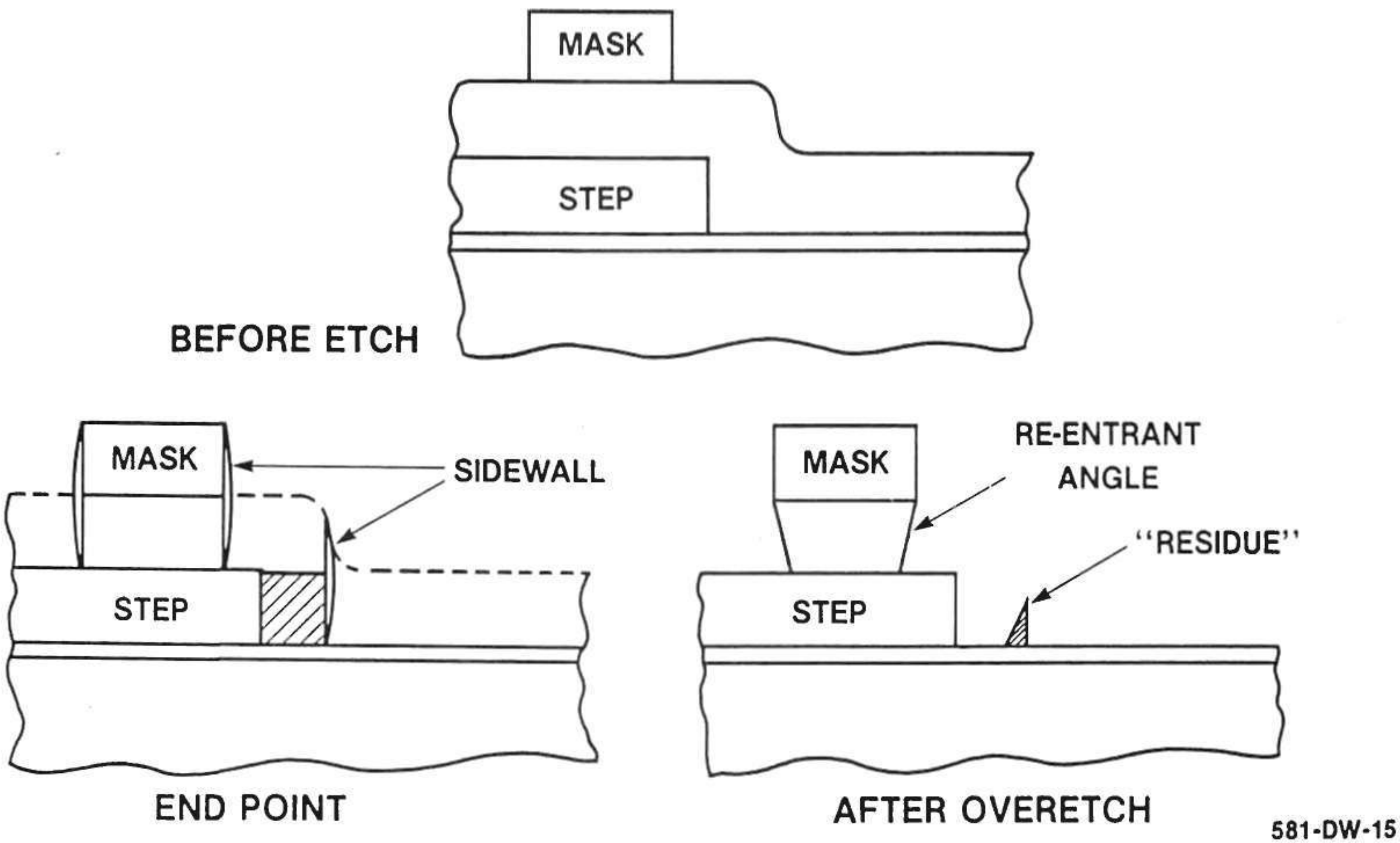


FIGURE 11

POST-ETCH RESIDUE RESULTING FROM "PROTECTIVE" SIDEWALL

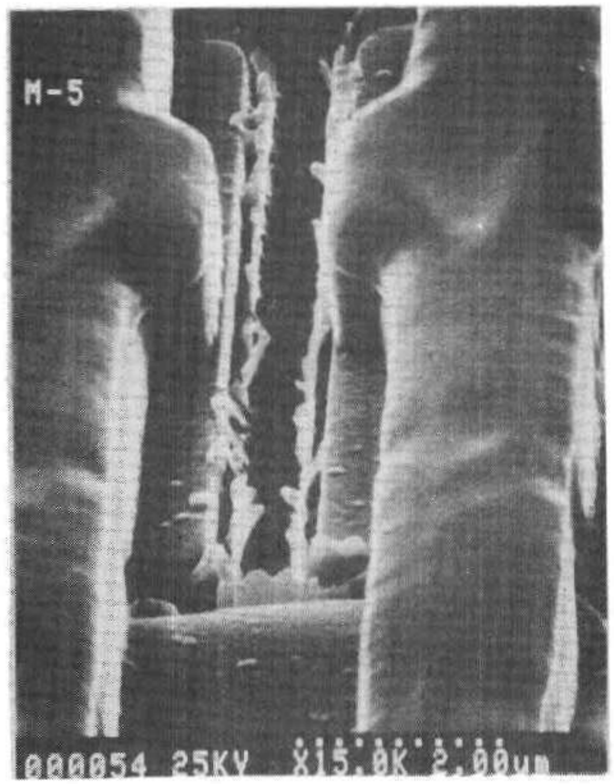
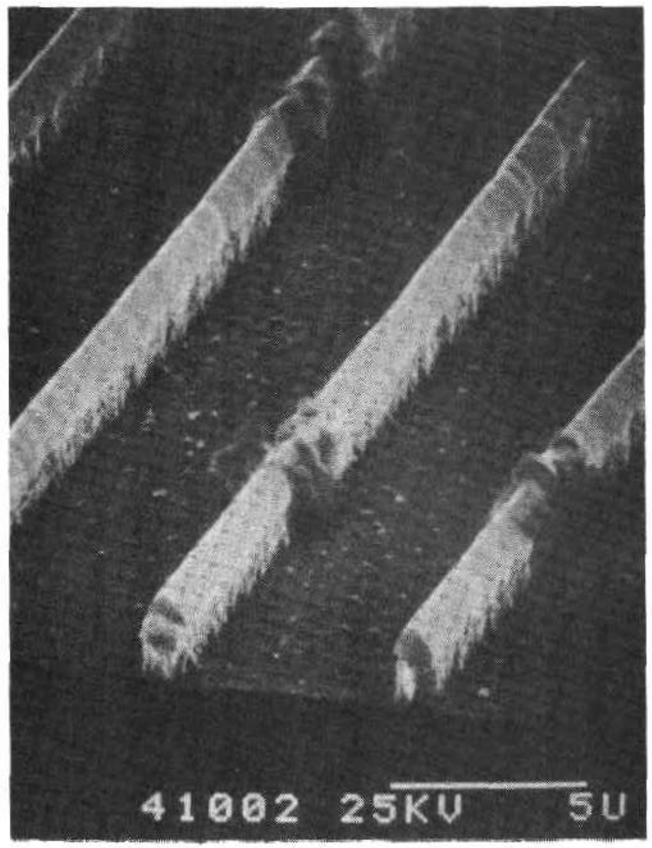


FIGURE 12

581-DW-16

CORROSION DUE TO $AlCl_x$ RESIDUE



F981MW.10

646-18

FIGURE 13

Dataquest

a company of
The Dun & Bradstreet Corporation

RESIST FOR MICROLITHOGRAPHY

Mary L. Long
Adjunct Lecturer
Microelectronics Laboratory
University of Arizona

Mrs. Long is a member of the technical staff of the Microelectronics Laboratory at the University of Arizona and teaches graduate level classes in Microlithography and Optics. She is also an independent consultant with Micro Lithography Ltd. in Tucson, Arizona. Previously, she was a Senior Staff Scientist with KTI Chemicals in Sunnyvale, California, a Senior Engineer at Motorola Semiconductor Group in Phoenix, Arizona, and at a member of the technical staff at Texas Instruments, Inc. Mrs. Long received a B.S. degree in Chemistry from Bishop College and has done graduate work in Solid State Technology and Materials Science at Southern Methodist University.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
October 20-22, 1986
San Diego, California

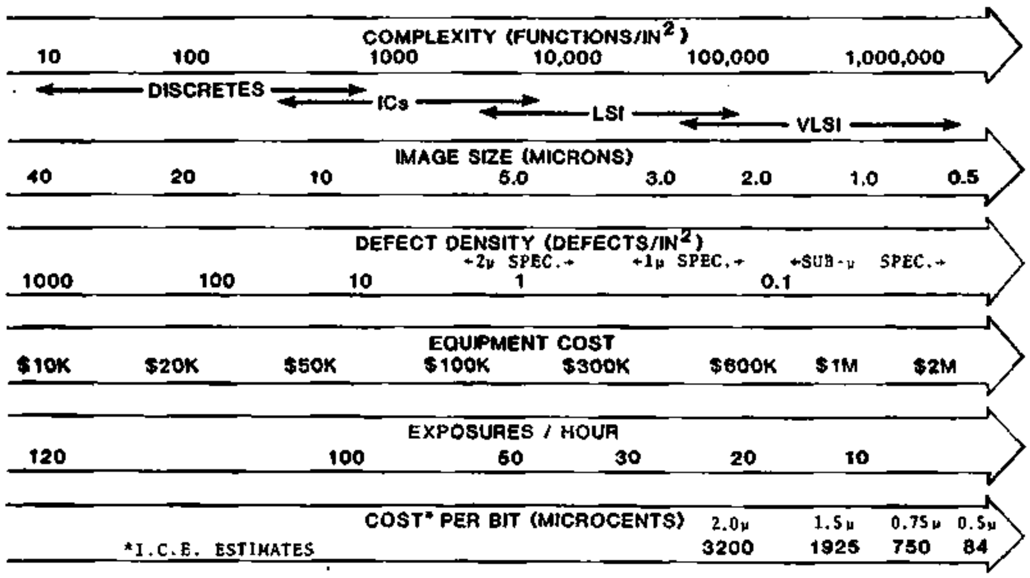
R E S I S T S   F O R   M I C R O L I T H O G R A P H Y

Mary L. Long

Microelectronics Laboratory
University of Arizona

Micro Lithography Ltd.
4040 N. Camino Arco
Tucson, AZ 85718

TRENDS IN MICROLITHOGRAPHY



TECHNOLOGY IMPLEMENTATION GUIDELINES

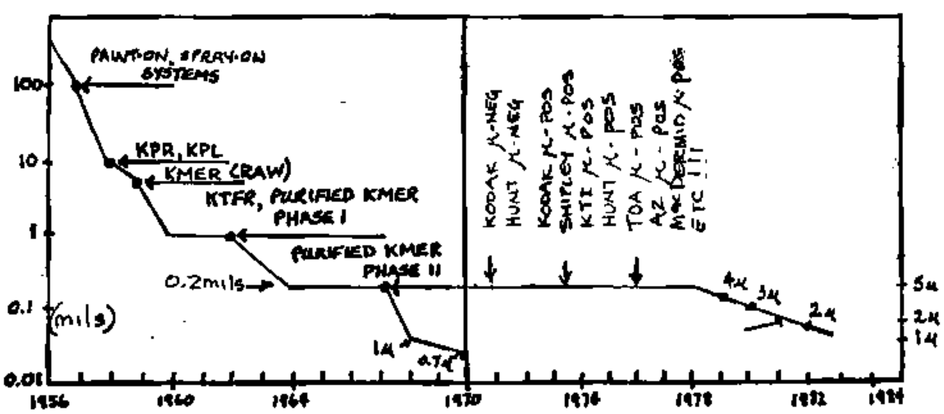
$$ - COST EFFECTIVENESS - $$

-Capital Investment
-Thruput/Yield
-Lifetime

"Microlithography is the pacing technology for VLSI manufacture."

-Rudenberg Associates
(SEMI -ISS, 1985)

RESISTS FOR MICROLITHOGRAPHY - HISTORICAL PERSPECTIVE



WHERE IS VLSI TAKING MICROLITHOGRAPHY?

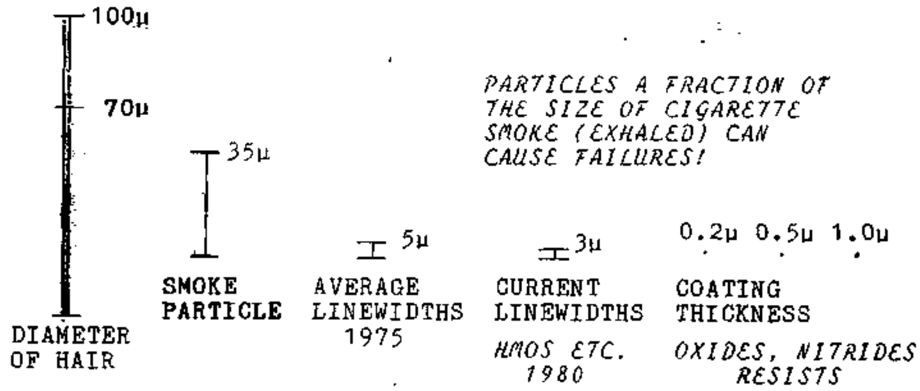
C O N T A M I N A T I O N

CONTAMINATION CONCERNS

-Minimum Image Size (smaller defect spec.)
-Die Size (fewer die per wafer)
-Complexity (less dead space)

"If Manhattan were a microchip, one pothole would stop all traffic"
-McDonnell Douglas ad (1986)

EFFECTS OF CONTAMINATION



STATUS : Contamination Control

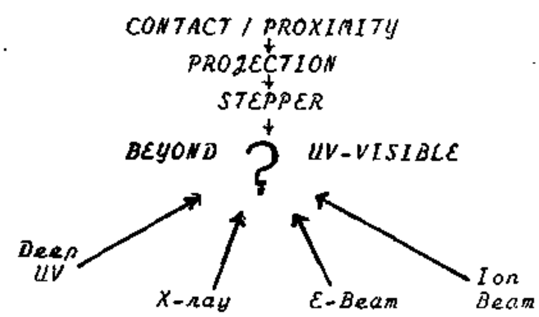
-Resist Filtration
-Substrate Cleanliness
-Processing Techniques
-Environmental Control

CONTAMINATION CONTROL

-<u>Part</u> of integrated team effort to improve yields
-Realistic specifications based on need
-Cost-effective process tuning

R E S I S T A N D I M A G I N G T E C H N O L O G I E S

<u>WAFER IMAGING PROGRESSION</u>



RESOLUTION

<u>Simple</u> resolution is only one of <u>many</u> factors which limit <u>useful</u> resolution.

RESOLUTION LIMITING PROBLEMS

IMAGE FIDELITY

- MTF, Contrast
- Resist Response
- Critical Dimension Control

TOPOGRAPHY

- Step Coverage
- Resist Thickness
- Critical Dimension Control

REGISTRATION

- Alignment
- Distortions
- Thermal Expansion

ETCH CAPABILITY

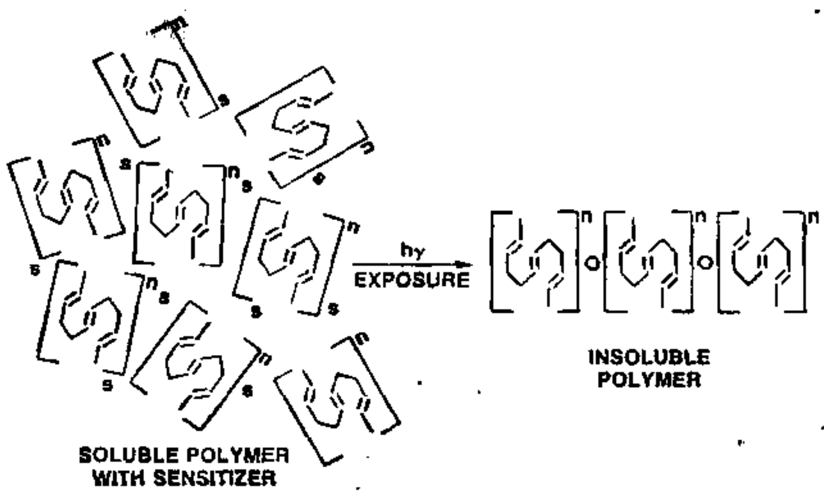
- Lateral Etch
- Resist Performance
- Critical Dimension Control

PHOTORESIST: WHAT IS IT?

- Chemistry
- Properties
- Negative / Positive

CHEMISTRY OF NEGATIVE RESIST

Crosslinking builds molecular weight

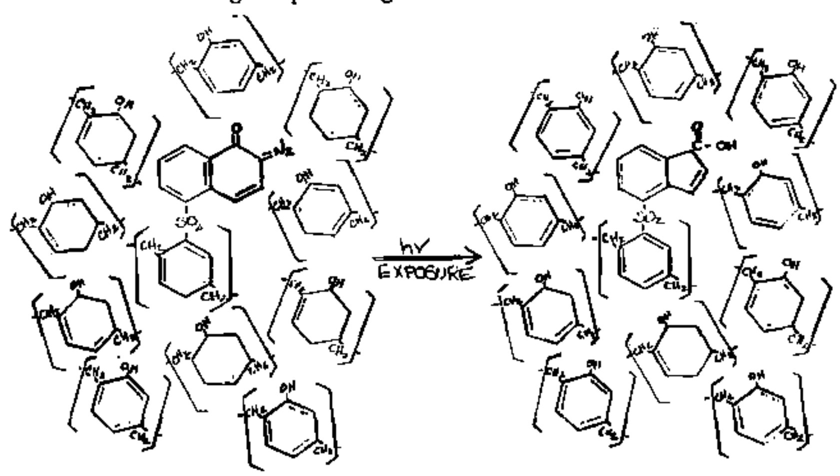


NEGATIVE PHOTORESIST:

- Synthetic Isoprene Polymer
- Elastic, Flexible
- Molecular Weight Changes
- Spectral Sensitivity @ 365 nm

CHEMISTRY OF POSITIVE RESIST

Functional group changes



INSOLUBLE SOLUBLE

POSITIVE PHOTORESIST:

- -Novolac-Type Resin
- -Brittle, Stress Prone
- -Functional Group Changes
- -Spectral Sensitivity @ 405 nm

PHOTORESIST: WHAT DO WE WANT IT TO DO?

IMAGE FIDELITY
- -Resolution
- -Critical Dimensions

ETCH PROTECTION
- -Wet Etch
- -Plasma, RIE, etc.
- -Various Substrates

IMPLANT MASK

LIFT-OFF MASK

MULTILAYER MASK

IMAGE FIDELITY

RESOLUTION
- 1975 - 5μ
- 1980 - 3μ--> 1.5μ
- 1985 - 1.5μ--> submicron

CRITICAL DIMENSIONS
- 1975 - ±0.5μ
- 1980 - ±0.25μ
- 1985 - ±0.1μ

CRITICAL DIMENSION SHIFTING
- 1975 - Negative Resist ← *exposure* →
- 1980 - Positive Resist *limited* →
- 1985 - Positive (VLSI) ↕ *exposure latitude*

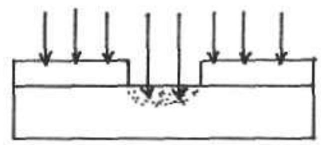
ETCH PROTECTION

WET ETCHANTS
- Lateral Etch, Undercut
- Adhesion, Scumming
- Etch Penetration, Pinholes

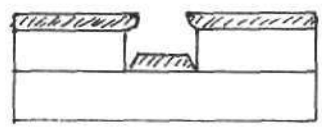
PLASMA, RIE
- Selectivity
- Anisotorpy
- Gas Absorption
- Pitting
- Redeposition

MASKING

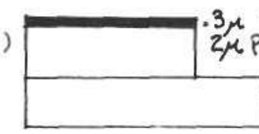
IMPLANT MASK
- Ion Exposure
- Thermal Stability, Removal
- Outgassing
- Thickness vs Resolution



LIFT-OFF MASK
- Edge Profile, Resist Slope
- Thermal Stability
- Scum-free Develop, Clean Lift
- Metal Particulates



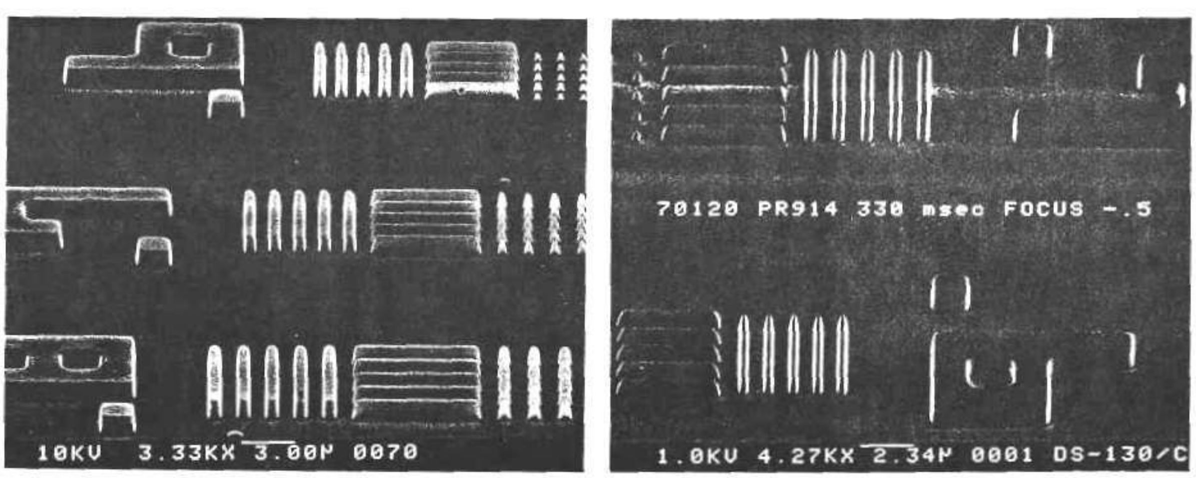
MULTILAYER MASK (PCM)
- High Resolution - (thin, flat resist)
- Interfacial Scum - (processing technique)
- Deep UV Density - (thin positive resists opaque)
- Improved Thruput for Steppers
- Inexpensive DUV Flood Systems
- Critical Dimension Control Over Steps



V L S I   R E S I S T   R E Q U I R E M E N T S

- Higher Resolution
- Tighter Critical Dimension Control
- Harsher Etching Environments
- Fewer Defects

EXAMPLE OF OPTICAL POSITIVE RESIST ON FLAT SURFACE IMAGED BY OPTICAL STEPPER



Thickness: 1.2 micron on oxide
Exposure: Nikon 5x (.42 n.a.), 330 m.s.

Courtesy of MacDermid Inc.

STRATEGIES

Enhancing Current Resist Performance
New Technologies / New Resists

SPECIAL TECHNIQUES TO ENHANCE RESIST PERFORMANCE

ARC (Anti-Reflective Coating)
CEM (Contrast Enhancing Material)
Image Reversal
Stabilization

A R C - ANTI-REFLECTIVE COATING

Under Resist Layer
Reduces Reflection, Scatter
Develops with Positive Resist
"Trenching" Problem

C E M - CONTRAST ENHANCEMENT MATERIAL

On Top of Resist
Bleaches during Exposure to increase threshold
Double or Triple Exposure Time Required
Extra Rinse Step

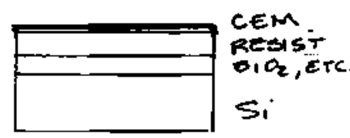


IMAGE REVERSAL

Two Exposures Required
Reversal Bake in Ammonia
Slope Control
Solution to Notching

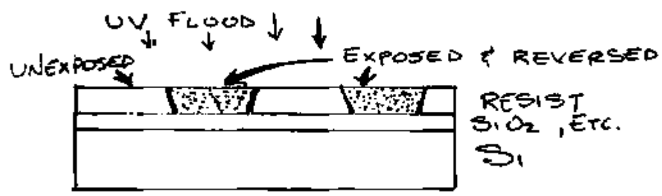


IMAGE STABILIZATION

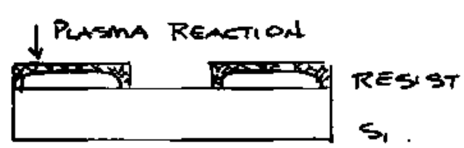
Improve Thermal Stability
Improve Plasma Resistance
Maintain Critical Dimension Control

BULK ACYLATION

Thermal or implant energy
to crosslink resin

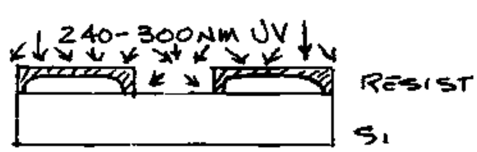
PRIST

Plasma Image Stabilization
Technique
Surface Acylation



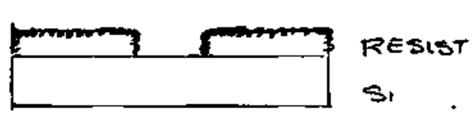
DEEP UV STABILIZATION

Surface Acylation
Mid-range DUV
240-300 nm



CHEMICAL STABILIZATION

Surface Reaction
Chlorobenzene
Liquid "PRIST"



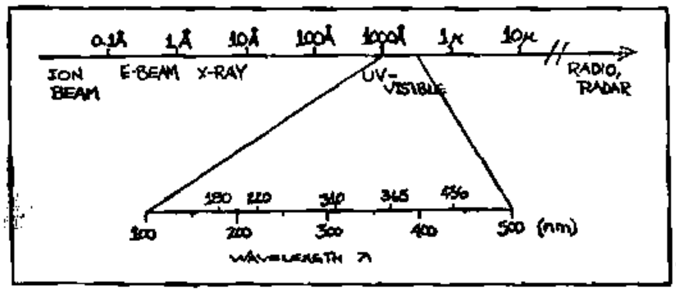
STRATEGIES (II)

NEW TECHNOLOGIES / NEW RESISTS

SHORTER WAVELENGTHS

I-Line (365 nm)
Deep UV (180 - 300 nm)
Laser (249nm, 325nm, ??)

ELECTROMAGNETIC SPECTRUM



OPTICAL RELATIONSHIPS

RESOLUTION $R = \frac{0.61\lambda}{NA}$

DEPTH OF FOCUS $df = \pm \frac{0.61\lambda}{(NA)^2}$

RESOLUTION VS WAVELENGTH

$R = \frac{0.61\ \lambda}{NA}$ if: $\lambda = 436nm$, $R = \frac{0.61}{.35}\ (436) = 0.76\mu$

$\lambda = 365nm$, $R = \frac{0.61}{.35}\ (365) = 0.64\mu$

$\lambda = 220nm$, $R = \frac{0.61}{.35}\ (220) = 0.38\mu$

I-LINE (365nm)

New Stepper Lenses
Theoretical Resolution / Focal Depth
Alignment and Focus Mechanisms
Optimized Resists

DEEP UV (180 - 300nm)

Quartz Optics
Focus and Alignment
Optimized Resists
Resist Aspect Ratio

LASER (single wavelength)

Wavelength (249nm, 325nm, ??)
Strategy
Thruput / Cost
Optimized Resist

BEAM TECHNOLOGIES

E-BEAM
X-RAY
ION BEAM

E-BEAM (Rastor or Vector Scan)

MASK GENERATION
- Flat
- Conductive
- Thin Film

OUTLOOK -
- Fast (compared to pattern generator)
- Resolution, Precision
- Cost Effective

WAFER FABRICATION
- Topography, Step coverage
- Non-conductive
- Dry Etch Requirements
- Beam Scatter, Proximity Effects
- Radiation Damage

OUTLOOK -
- Resolution vs Optical
- Thruput / Cost
- Multilayer Approach

X-RAY

- High Resolution
- X-Ray Sources
- Resist Options
- Mask Fabrication
- Step and Repeat Precision
- Thruput / Cost
- Radiation Damage

ION BEAM (FIB)

- Resolution
- Reduced Scatter
- Improved Resist Options
- Precision Stage and Electronics
- Resist-Free Implant?
- Radiation Damage

NEW TECHNOLOGIES / NEW RESISTS

- Wavelength Specific
- Multilayer
  - Imaging
  - Planarizing
  - Etch Resistance
- GeSe and Other Inorganic Resists
- Polyimides
- Filled Resists

S U M M A R Y   C O M M E N T S

- No Magic
- Integrated Teamwork
- Understand Processes
- Tighten Controls
- Refuse to Accept Low Yields
- Find and Fix Problems
- No Scapegoat!

THANK YOU

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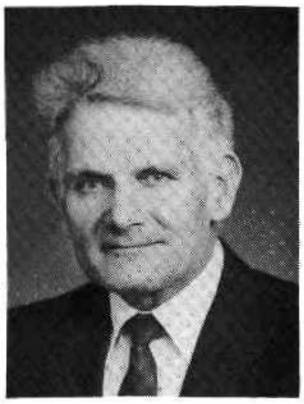
TRENDS IN DEPOSITION TECHNOLOGY AND EQUIPMENT



Klaus K. Schuegraf
Vice President and Director
of Technology
Tylan Corporation

Dr. Schuegraf is Vice President and Director of Technology of Tylan Corporation. During his 33 years in semiconductors, he has held management positions in semiconductor device technology, semiconductor process and equipment development, product planning and market introduction, and research and development. Before joining Tylan, he held managerial positions at Hughes Aircraft Company, TRW, Westinghouse, and IBM. He has also taught integrated circuit technology at UCLA. Dr. Schuegraf received B.S. and M.S. degrees in Physics from the University of Tuebingen, Germany and a Ph.D. in Physics from the Technical University in Stuttgart, Germany.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
October 20-22, 1986
San Diego, California

TRENDS IN DEPOSITION TECHNOLOGY AND EQUIPMENT

- 1 -

KLAUS K. SCHUEGRAF
TYLAN CORP.
CARSON, CA

DEPOSITION TECHNOLOGY

- EPITAXY
- LOW PRESSURE CHEMICAL VAPOR DEPOSITION
- SPUTTERING

DEPOSITION FOR IC FABRICATION

Number of CVD Steps required for IC Fabrication

DEPOSITION	H-CMOS	HMOS	CMOS/NMOS	SCHOTTKY TTL	ECL
POLY Si	2	1-3	1	-	1
EPITAXY	1	-	-	1	1
PSG/Si_3N_4	2-3	1-2	1	2	-
ALUMINUM	1	1-2	1	2	2-3
OTHER METALS	1-2	1	-	1	-
SILICIDES	1-2	0-2	-	-	-
TOTAL DEPOSITION STEPS	8-11	4-10	3	6	4-5

FROM: SEMICONDUCTOR INTERNATIONAL, JAN. '86

TYLAN
Leadership Through Tomorrow's Technology

0021-986-4

EPITAXY ISSUES:

- THROUGHPUT AND COST
- CRYSTAL DEFECTS: SLIP,PARTICLES
- TRANSITION WIDTH
- PATTERN SHIFT
- SENSITIVITY TO OXIDANTS
- DEPOSITION TEMPERATURE

NEW DEVELOPMENTS:

- HOTWALL EPI-REACTOR: BELLJAR/TUBE
- PLASMA ENHANCED EPITAXY
  - LOW TEMPERATURE (650°c)
- PHOTO ENHANCED EPITAXY
  - LOW TEMPERATURE (200°c)

USER EXPECTATIONS:

- SHIFT TO LARGER WAFER SIZE
- FILM THICKNESS & COMPOSITION UNIFORMITY
- REDUCED PARTICLE CONTAMINATION
- AUTOMATION: LOADING PROCESS, TRANSPORT, DATA
- THROUGHPUT
- EQUIPMENT UPTIME

LOW PRESSURE CVD:

FILMS: DEPOSITION OF DIELECTRIC AND CONDUCTIVE FILMS

- SiO_2, DOPED SiO_2
- Si_3N_4
- POLY Si, DOPED AND UNDOPED
- METALS (W, WSi_2, Mo, $MoSi_2$, AL)
- OTHER: BN, OXINITRIDE

PROCESSES: THERMALLY ACTIVATED
PLASMA ENHANCED
PHOTON ENHANCED

EQUIPMENT: HOTWALL - TUBE REACTOR (HORIZONTAL/VERTICAL)
HOTWALL - BELLJAR REACTOR
SINGLE/MULTIWAFER REACTORS

HOTWALL TUBE REACTORS:

ADVANTAGES:

- GOOD ECONOMY: THROUGHPUT, COST
- GOOD FILM UNIFORMITY
- GOOD STEP COVERAGE
- PROVEN EQUIPMENT AND PROCESSES

DISADVANTAGES:

- PARTICULATE GENERATION
- CLEANING AND MAINTENANCE
- REACTANT DEPLETION EFFECTS
- LOADING AND UNLOADING
- NO PLANARIZATION
- COMPLEX REACTION KINETICS (LTO, DOPED POLY, W)

BELLJAR REACTORS:

CHARACTERISTICS:

- GOOD THROUGHPUT
- GOOD UNIFORMITY
- LOWER PARTICULATE GENERATION
- QUICK CLEANING

- 6 -

LIMITATIONS:

- HIGH COST
- EXPENSIVE QUARTZWARE
- AUTOMATED LOADING/UNLOADING
- PLANARIZATION

PROCESS SPECIFIC REACTORS:

CHARACTERISTICS:

- CASSETTE TO CASSETTE LOADING
- SINGLE OR MULTIWAFER PROCESS CHAMBERS
- DEDICATED PROCESSES
- HIGH UNIFORMITY
- LOW PARTICULATE GENERATION
- SELF CLEANING

LIMITATIONS:

- THROUGHPUT
- FAB ACCEPTANCE
- COST

PLASMA ENHANCED CVD REACTORS:

<u>CHARACTERISTICS:</u>

- LOW TEMPERATURE DEPOSITION
- COMPLEX REACTION KINETICS
- DIFFICULT PROCESS FILM CHARACTERISTICS CONTROL
- HIGHER PARTICULATE GENERATION
- COMPLEX AUTOMATED LOADING/UNLOADING

<u>REACTORS:</u>

- TUBE REACTOR:
  - WORKHORSE
  - GOOD THROUGHPUT
- PARALLEL PLATE REACTOR:
  - LIMITED THROUGHPUT
- SINGLE/MULTISTATION REACTOR:
  - CASSETTE/CASSETTE LOADING
  - GOOD UNIFORMITY

CVD FILM APPLICATIONS:

SiO2:

- UNDOPED , DOPED (PSG, BPSG), TEOS
- DIELECTRIC FILMS FOR MULTILAYER INTERCONNECTS
- GLASS REFLOW FOR BETTER STEP COVERAGE
- DEEP TRENCH ISOLATION
- GLASS OVERCOATS (LOW TEMPERATURE: HILLOCKS)
- CAPPING LAYERS
- MASKING LAYERS (ION IMPLANT, DIFFUSION)

ISSUES:

- STRESS CONTROL
- CONFORMALITY
- DOPANT CONTROL
- PLANARIZATION
- DEPOSITION TEMPERATURE

CVD APPLICATIONS:
(CONT.)

METAL FILMS:

REFRACTORY METALS & SILICIDES:

W, WSi_2, Mo, $MoSi_2$, Ti, $TiSi_2$, Ta, $TaSi_2$

- CONTACTS (SMALL GEOMETR CS, $\leqq 2\,\mu m$)
- INTERCONNECTIONS
- SELECTIVE/NON SELECTIVE DEPOSITION

ALUMINUM:

- CONTACTS/INTERCONNECTIONS

ISSUES:

- FILM COMPOSITION
- MINIMUM RESISTIVITY
- ANNEALING
- FILM ADHESION
- SURFACE SPECULARITY
- ELECTRO MIGRATION
- STABILITY

TYLAN

Leadership Through Tomorrow's Technology

CVD APPLICATIONS:
(CONT.)

POLY SILICON: (DOPED/UNDOPED)
- GATE ELECTRODES
- INTERCONNECTIONS
- FIELD ELECTRODES

AMORPHOUS SILICON:
- GATE ELECTRODES
- CONDUCTIVE LAYERS
- PHOTO VOLTAICS

ISSUES:
- DEPOSITION RATES
- GRAIN SIZE CONTROL
- DOPANT CONCENTRATION

CVD FILM APPLICATIONS:
(CONT.)

Si_3N_4:

- SURFACE PASSIVATION (PLASMA ENHANCED CVD)
- OXIDATION MASKS (RECESSED OXIDE ISOLATION)
- GATE DIELECTRIC LAYER

OXYNITRIDES:

- GATE DIELECTRIC LAYERS
- PASSIVATION

ISSUES:

- STRESS CONTROL
- THICKNESS CONTROL (<200A°)

PHOTON-ENHANCED CVD:

EQUIPMENT:

R & D, PILOT LINE. NO PRODUCTION REACTOR COMMERCIAL SYSTEMS AVAILABLE.

DEPOSITED FILMS:

- SiO_2, DOPED AND UNDOPED
- Si_3N_4
- OXYNITRIDES
- AMORPHOUS SILICON
- TUNGSTEN
- SINGLE CRYSTALLINE Si (Si_2H_6)

LPCVD OR SPUTTER DEPOSITION?

ADVANTAGES OF LPCVD:

- ECONOMICS
- UNIFORMITY: THICKNESS/COMPOSITION
- STEP COVERAGE
- GOOD COMPOSITION CONTROL
- PARTICULATES
- MOSTLY DIELECTRIC AND POLY Si
- BATCH PROCESS

ADVANTAGES OF SPUTTERING:

- HIGH DEPOSITION RATES
- SINGLE WAFER PROCESS
- SPECULAR METAL SURFACE
- SAFE PROCESSES
- GOOD ALLOY CONTROL

SPUTTER DEPOSITION:

EQUIPMENT ISSUES:

- UNIFORMITY: ±1...5%
- FILM PURITY AND COMPOSITION
- STEP COVERAGE
- THROUGHPUT: 100 WAFERS PER HOUR
- DEPOSITION RATE: 1 MM/MIN
- SUBSTRATE HEAT DISSIPATION
- TARGET INTEGRITY/COMPOSITION
- MULTILAYER CAPABILITY
- RADIATION DAMAGE
- REPEATABILITY AND CONTROL
- AUTOMATED LOADING: CASSETTE/CASSETTE
- EQUIPMENT UPTIME

SPUTTER DEPOSITION:

PROCESS

- MATERIAL TRANSPORT FROM TARGET TO SUBSTRATE THROUGH ION BOMBARDMENT
- METALS AND DIELECTRIC MATERIALS
- DC-/MAGNETRON-/RF- SPUTTERING

BIAS SPUTTERING:

- ANGULAR DEPENDENCE OF BACK SPUTTER YIELD
- PLANARIZING OF SURFACE TOPOGRAPHY
- SURFACE CONDITIONING/NUCLEATION

PHOTON-ENHANCED CVD:

TECHNOLOGY:

- HIGH ENERGY PHOTONS (UV LIGHT) EXCITES REACTANT GAS
- LOW TEMPERATURE PROCESS
- NO RADIATION/CHARGED PARTICLE DAMAGE
- SENSITIZED/NON-SENSITIZED REACTIONS
- LOW FILM STRESS
- GOOD STEP COVERAGE

PHOTON SOURCES:

- LOW PRESSURE Hg DISCHARGE LAMPS (10-100mW/cm^2)
- EXCIMER LASERS (ArF: 193nm, KrF: 249nm) 3-10 W/cm^2

LPCVD REACTOR PERFORMANCE COMPARISON

REACTOR TYPE	PROCESSES AVAILABLE	THROUGHPUT WAFERS/HOUR	MAX. WAFER SIZE	UNIFOR-MITY	BASE PRICE $	EQUIPMENT SUPPLIERS	COMMENTS
HOTWALL HORIZONTAL TUBE REACTOR	Si_3N_4, PolySi, LTO, HTO, PSG, BPSG, TEOS & Si	~100	150-200mm (6-8")	2-6%	$130.0-150.0) PER TUBE	ACS ASM BRUCE PTL THERMCO TYLAN	DIFFUSION FURNACE TYPE
HOTWALL VERTICAL TUBE REACTOR	Si_3N_4, PolySi, LTO, HTO, PSG, BPSG, TEOS	100	150-200mm (6-"8)	?	$130.0-280.0	DENKO DISCO-SEIER TEMPRESS SVG	VERTICAL FURNACE TYPE
HOTWALL BELLJAR REACTOR	SiO_2, (LTO, HTO), Poly Si, BPSG, Si_3N_4	50-100	150mm (6")	3-6%	$350.0-450.0 100.0	ANICON SEMITHERM	

LPCVD REACTOR PERFORMANCE COMPARISON

REACTOR TYPE	PROCESSES AVAILABLE	THROUGHPUT WAFERS/HOUR	MAX. WAFER SIZE	UNIFOR-MITY	BASE PRICE $	EQUIPMENT SUPPLIER	COMMENTS
PROCESS SPECIFIC REACTORS							
COLDWALL-BATCH	W, $WiSi_2$, SiO_2	30-40	150mm (6")	5%	260.0-320.0	GENUS	8301
COLDWALL-BATCH	LTO/BPSG	70	250mm (10")	2%	460.0	FOCUS	"FORCED CONVECTION"
COLDWALL-SINGLE WAFER PLASMA/THERMAL	POLY SI, W, WSi_2, Si_3N_4, SiO_2, (PSG, BPSG)	10-20	200mm (8")	3-6%	340.0	VARIAN	5101
COLDWALL-BATCH PLASMA/THERMAL	SiO_2, PSG, BPSG	80	200mm (8")	1%	520.0	NOVELLUS	LTP-2
COLDWALL-SINGLE WAFER	SiO_2	30-60	150mm (6")	?	250.0	MTI	"AFTER GLOW"

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ION IMPLANTATION EQUIPMENT TRENDS

Andrew Wittkower
Consultant

Dr. Wittkower is a consultant for the semiconductor industry. Previously, he was Vice President of the Ion Beam Systems Division of Eaton Corporation and a Director of its Japanese joint venture partner, Sumitomo Eaton Nova. Before joining Eaton, he was President of Zymet, which he founded. Prior to that, he was a founder and General Manager of Nova Associates (later acquired by Eaton) and a founder of Extrion Corporation (now Varian/Extrion Division). Dr. Wittkower received a B.Sc. degree in Mathematics and Physics from McGill University in Montreal, Canada, an M.Sc degree from the University of Cambridge, and a Ph.D. degree in Atomic Collision Physics from University College, London.

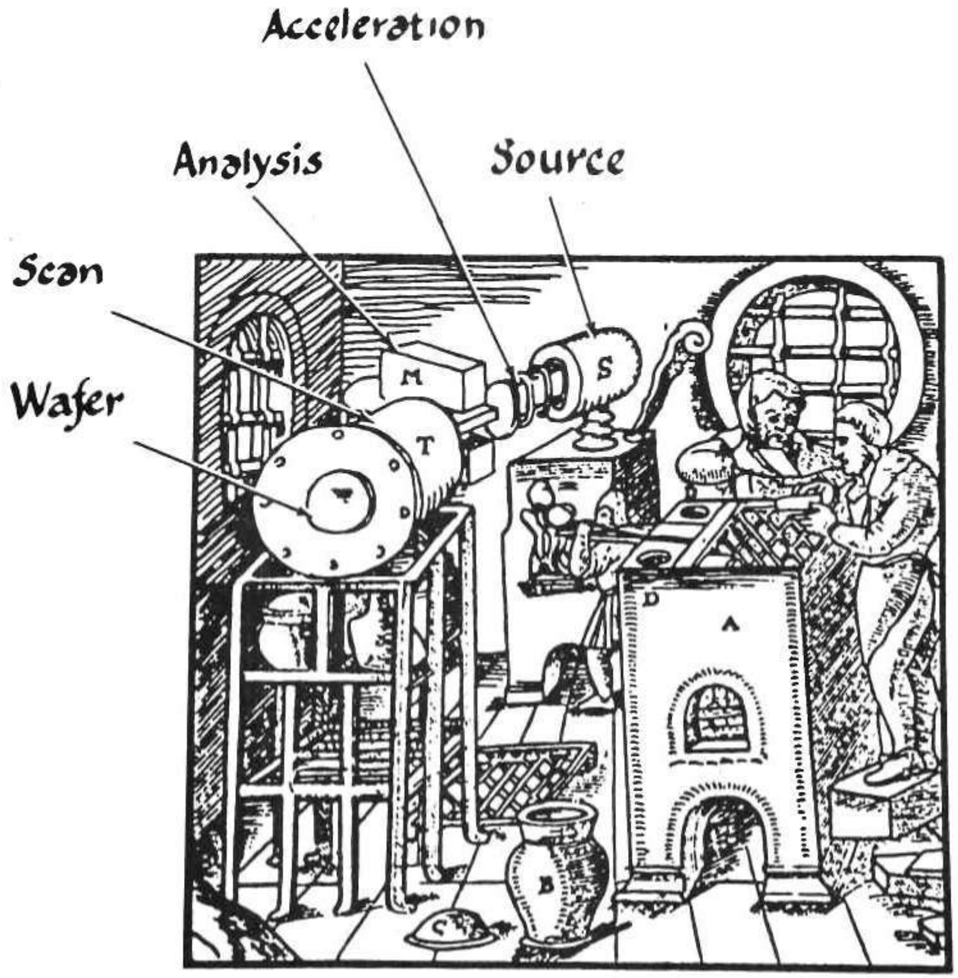
Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
October 20-22, 1986
San Diego, California

ION IMPLANTATION EQUIPMENT TRENDS

BY

Dr. ANDREW WITTKOWER

An Early Ion Implantation System

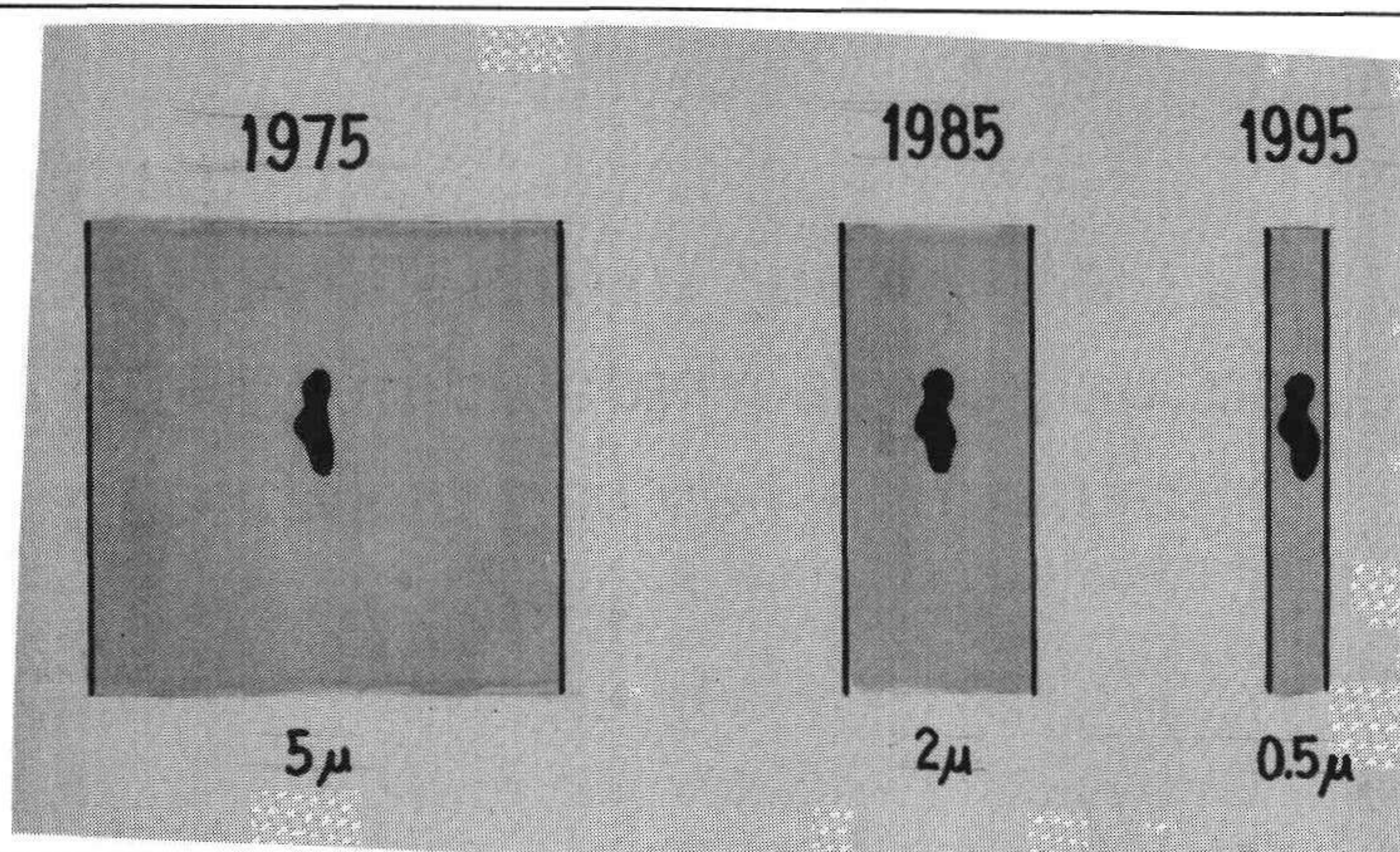


(With Acknowledgments to G. Agricola and Prof. M.W. Thompson)

Changes in Device Requirements Drive Equipment Design Changes in One or More of These Five Elements

Line Width Reduction Means that:

- Particulates Become Increasingly Important
  Both Quantity and Size



Major Device Changes are:

- Line Width Reduction

- Circuit Dimension and Circuit Depth Reduction

- Wafer Size Increase

Particulates Solution

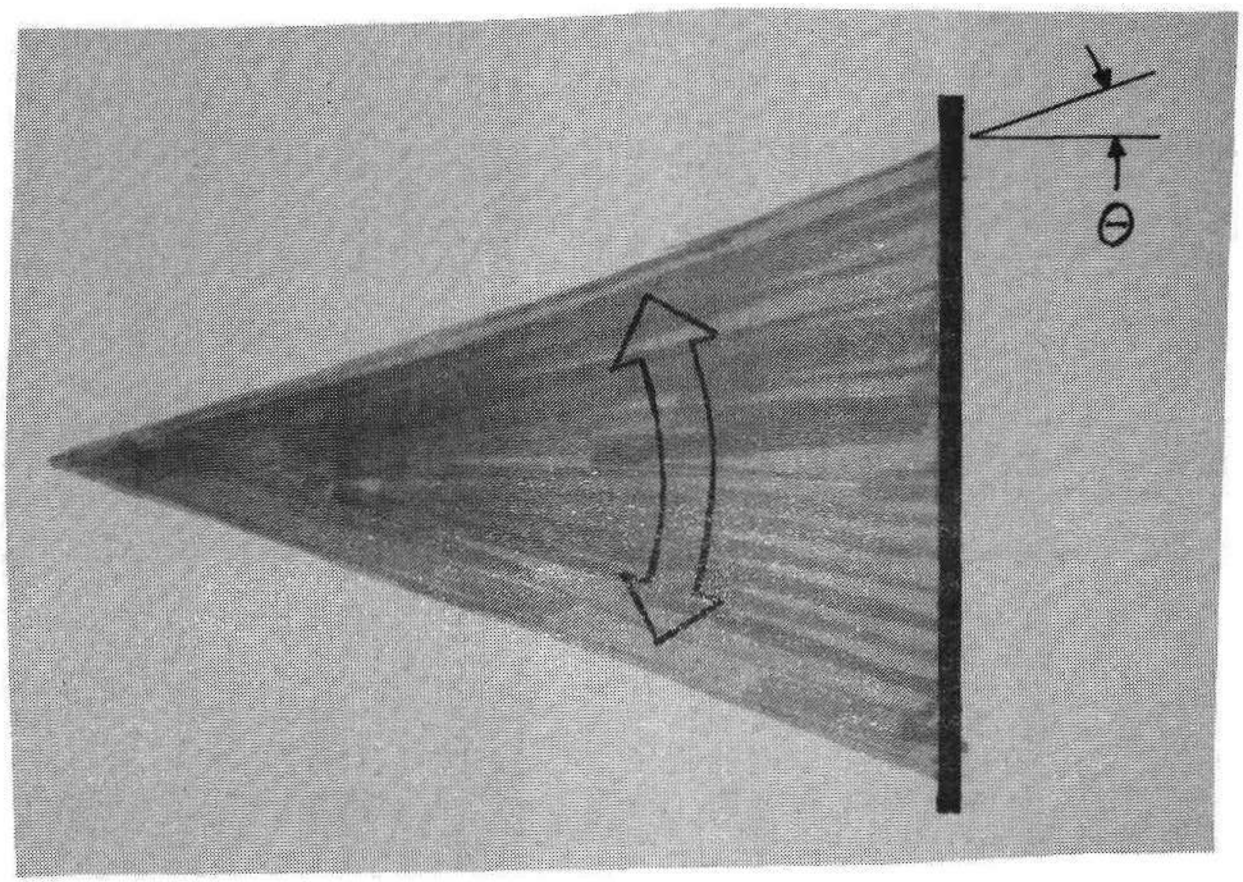
- Cleaner Systems

- Automation

- Robotics

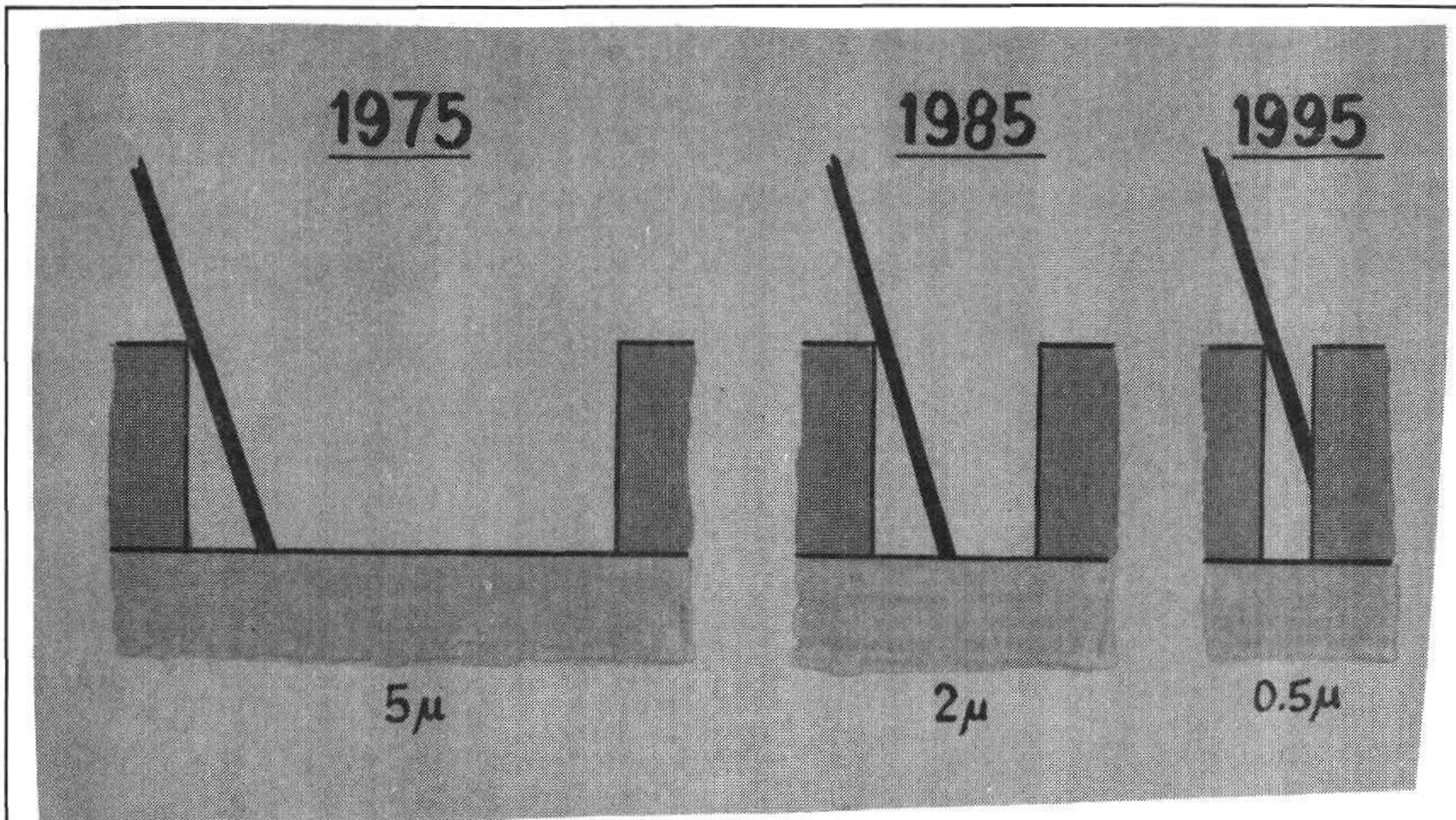
Line Width Reduction Means that:

- The Mask may Shadow the Silicon

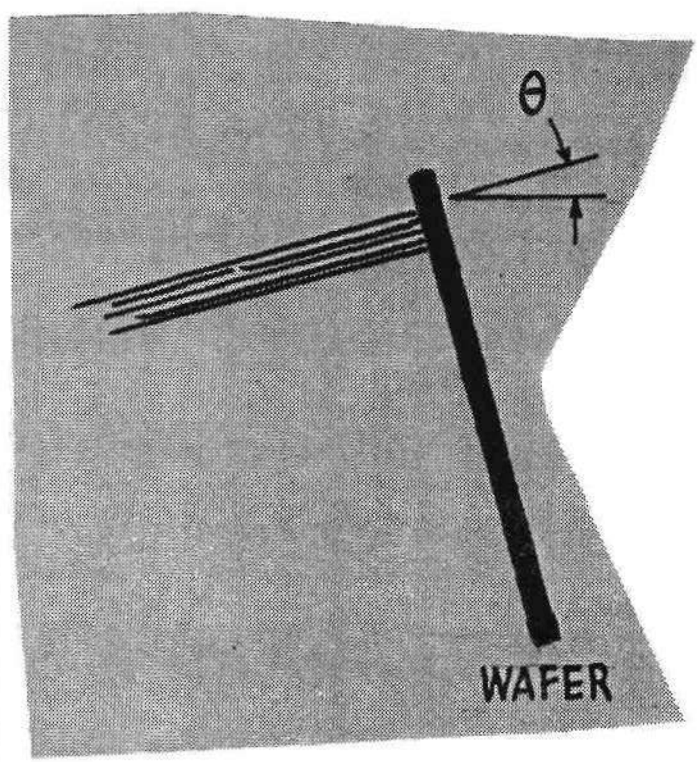


Line Width Reduction Means that:

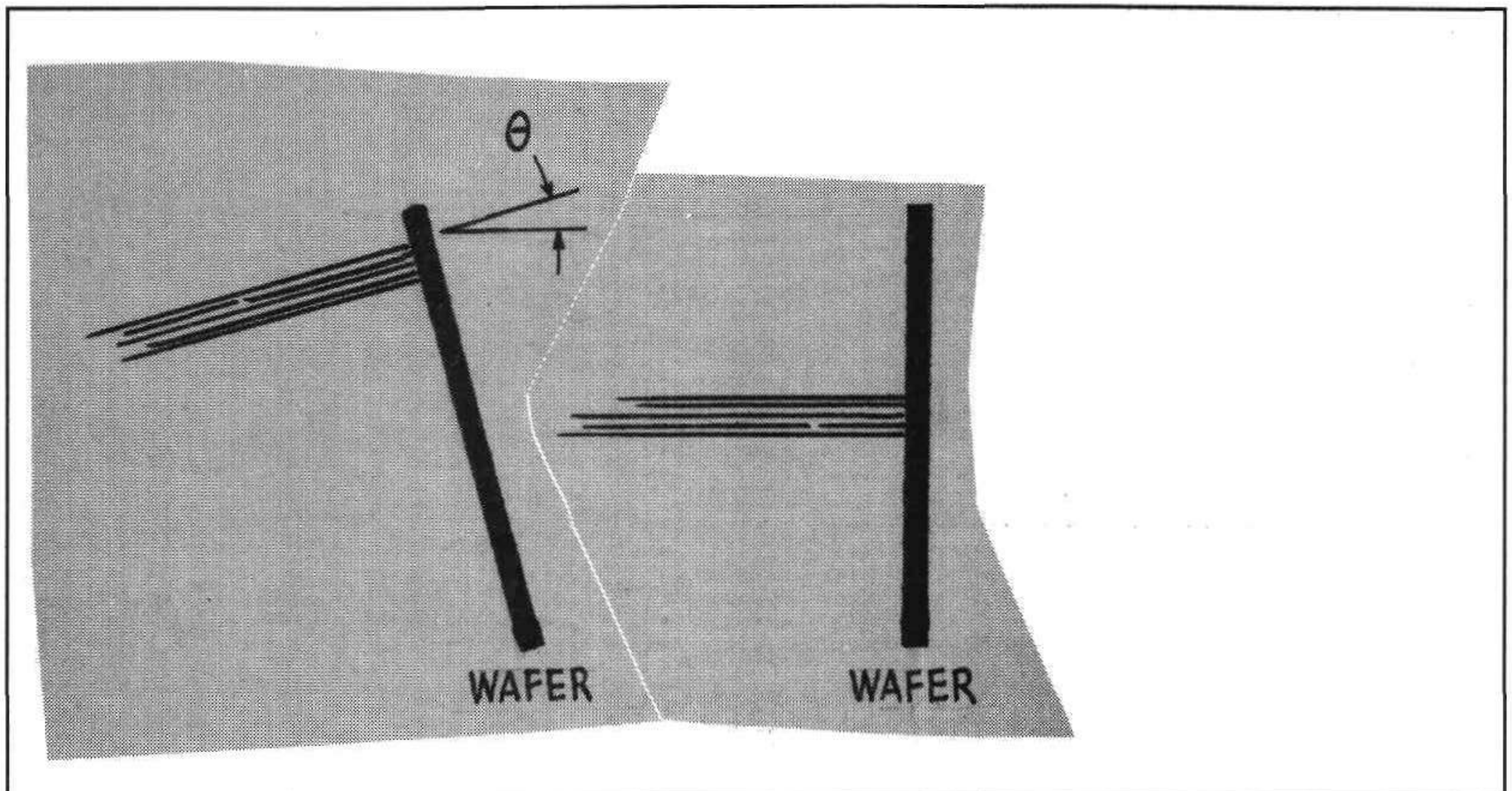
- The Mask may Shadow the Silicon



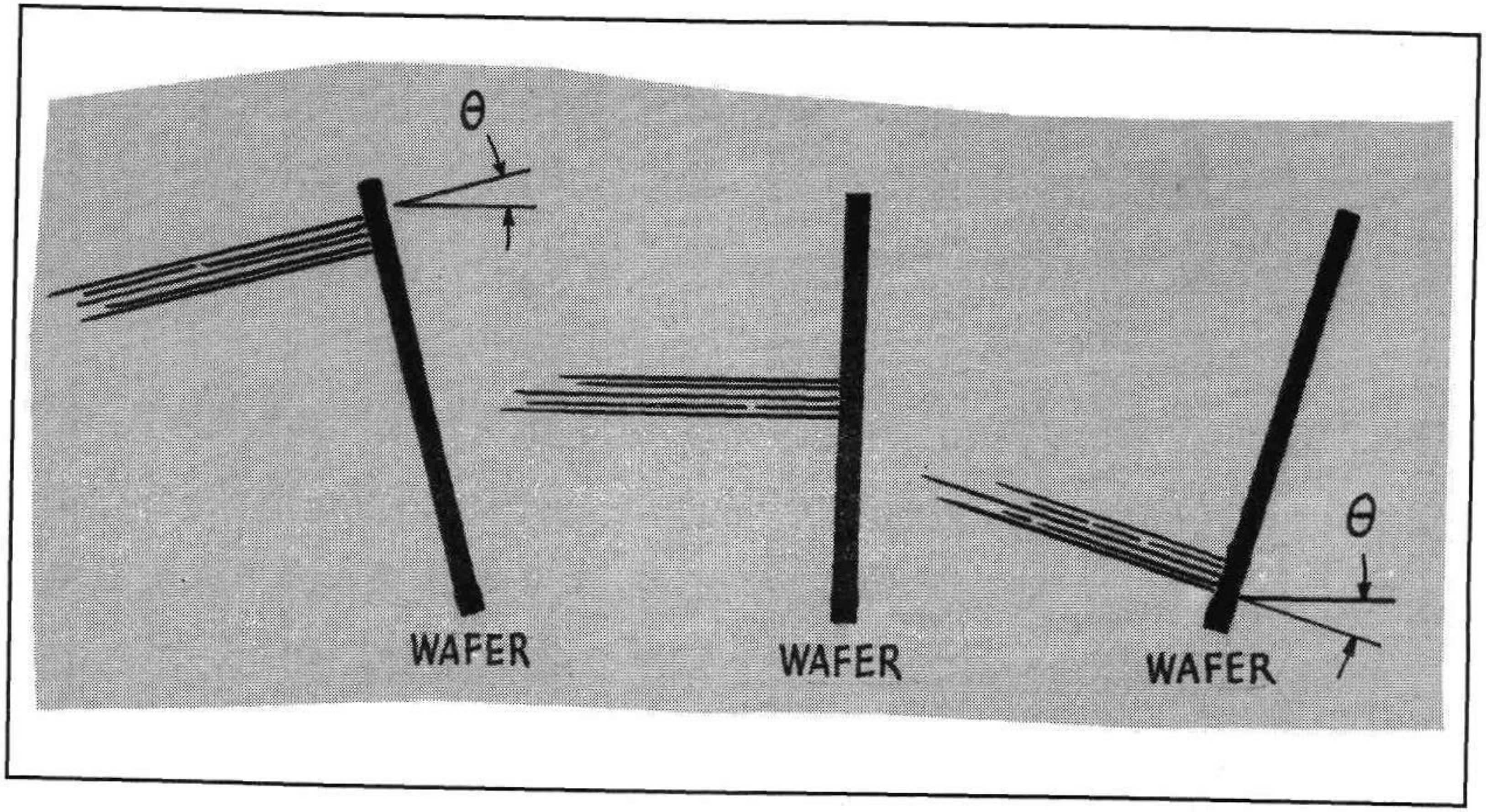
One Engineering Solution to Mask Shadowing is:



One Engineering Solution to Mask Shadowing is:



One Engineering Solution to Mask Shadowing is:



As Line Widths Decrease

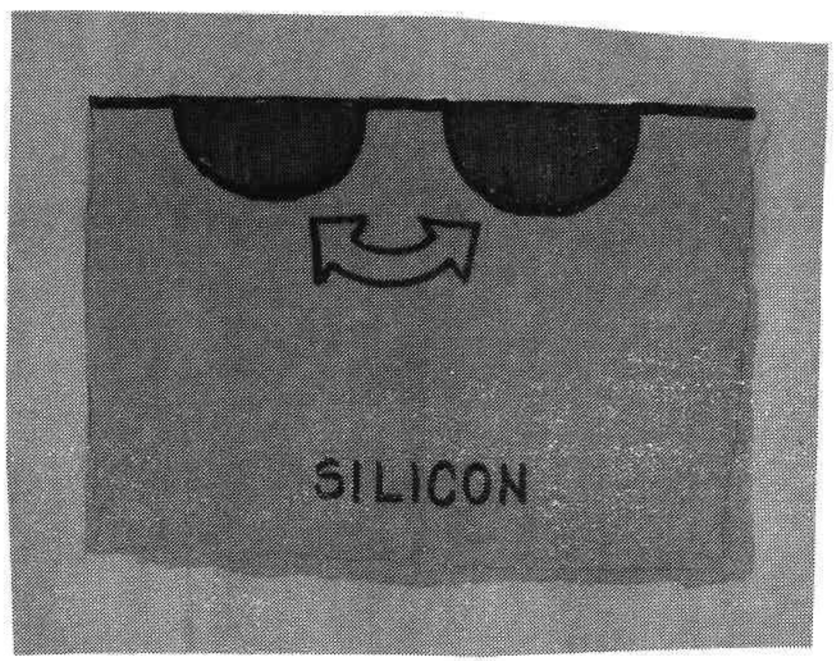
- Circuits get Smaller

- Circuits get Shallower

- Circuits are Placed Closer Together

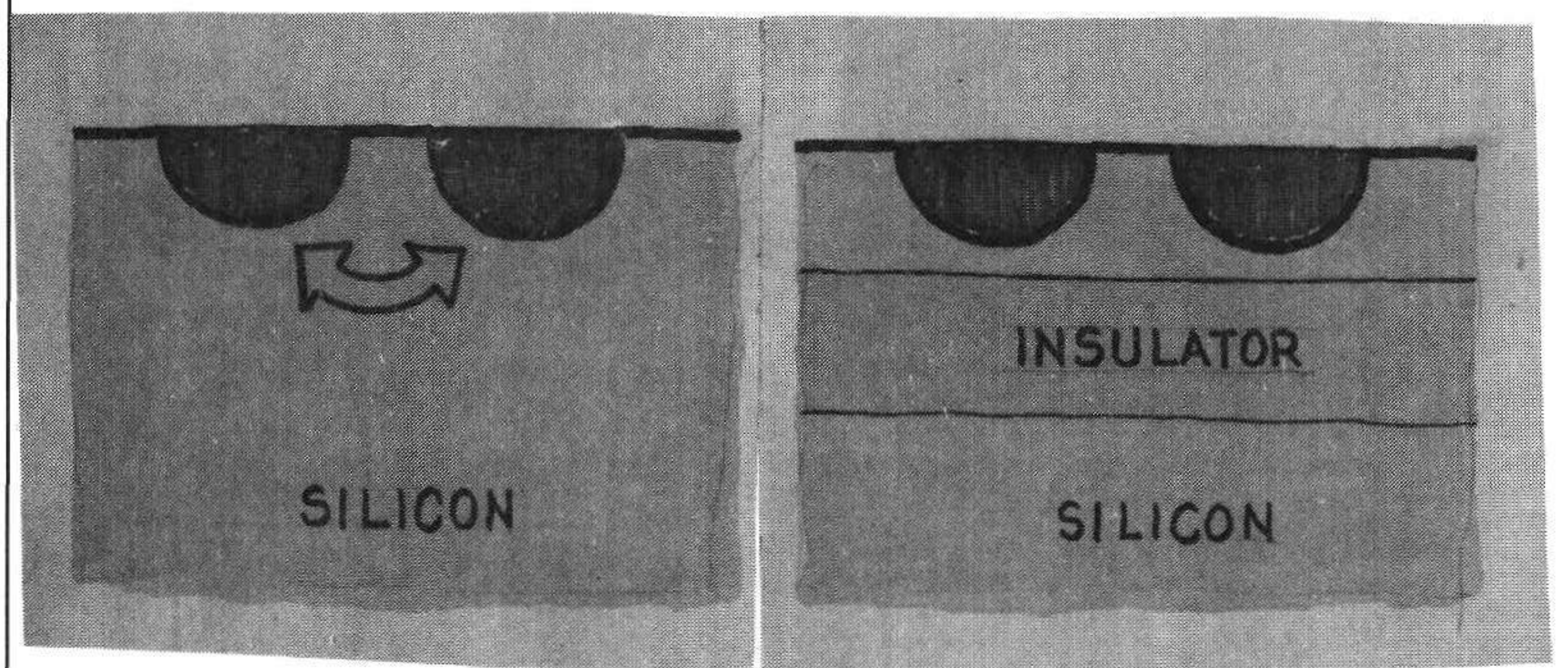
As Line Widths Decrease:

- Circuits are Placed Closer Together

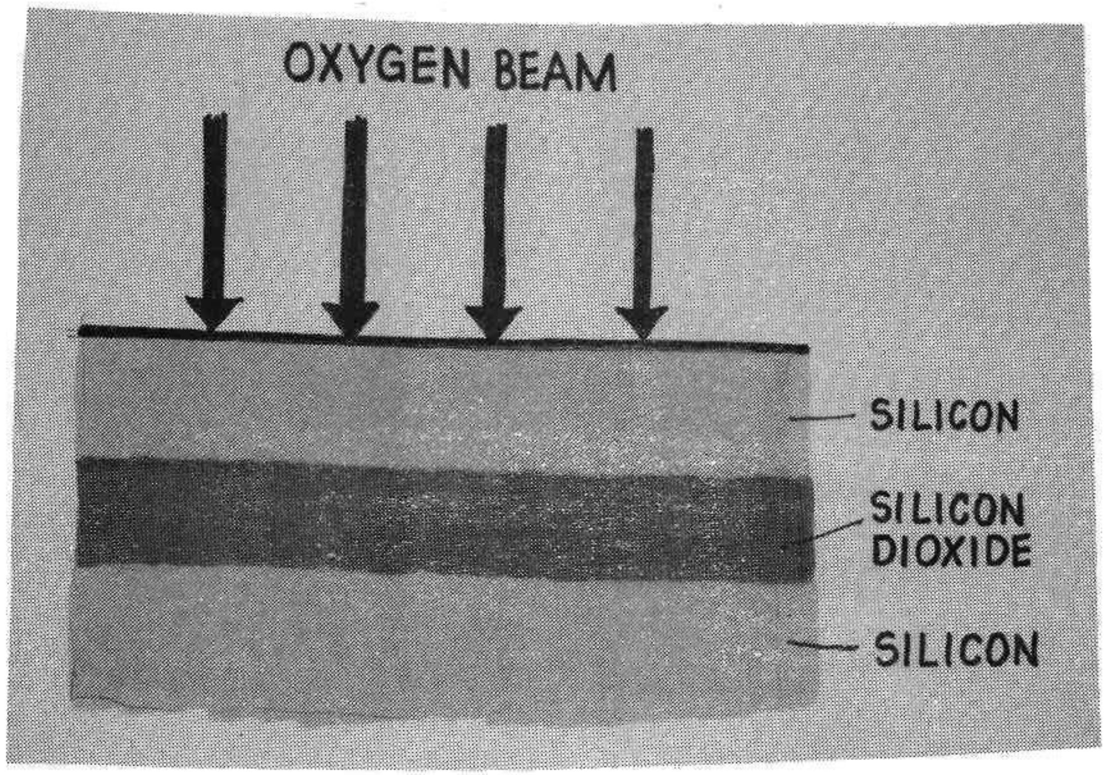


As Line Widths Decrease:

- Circuits are Placed Closer Together

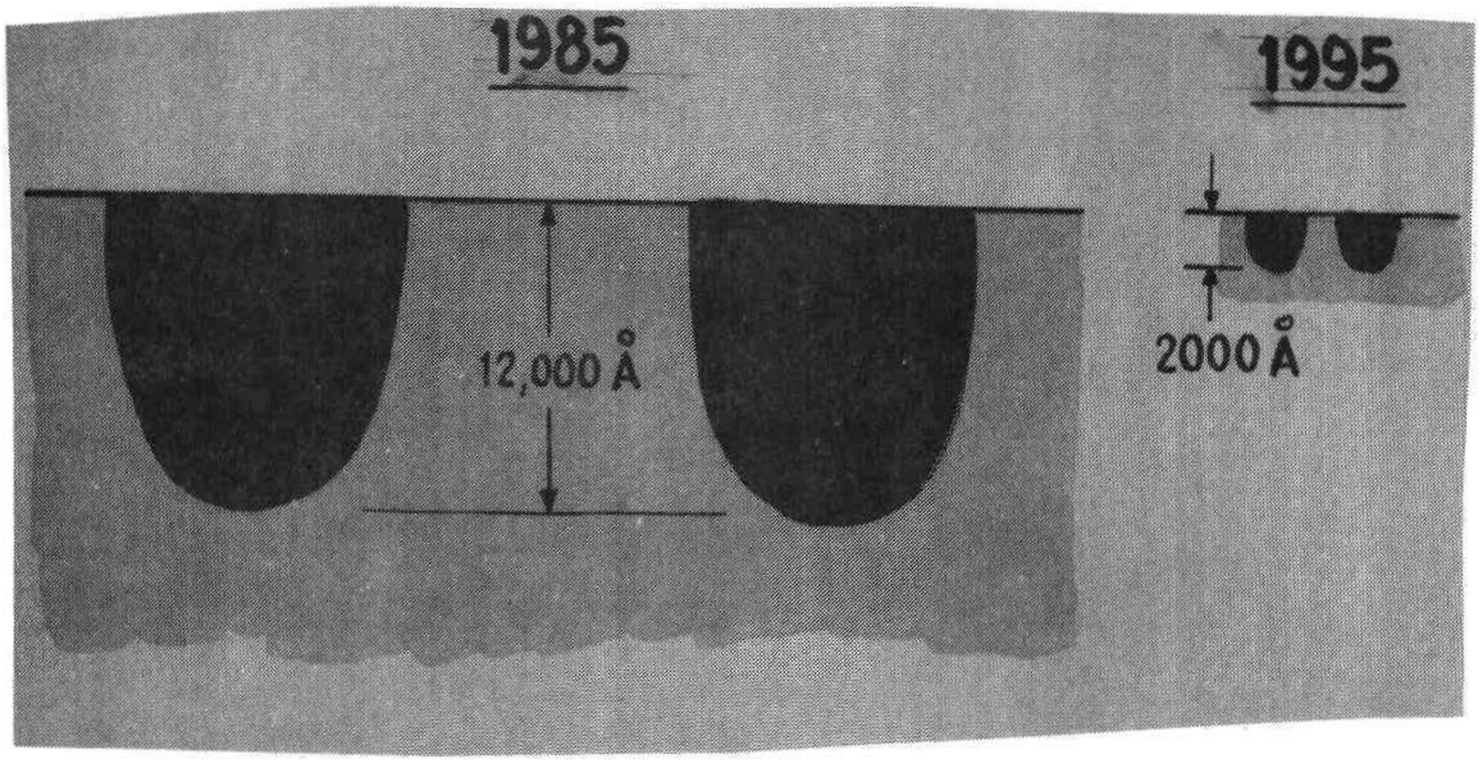


New Ion Implanters Produce a Buried Insulating Layer



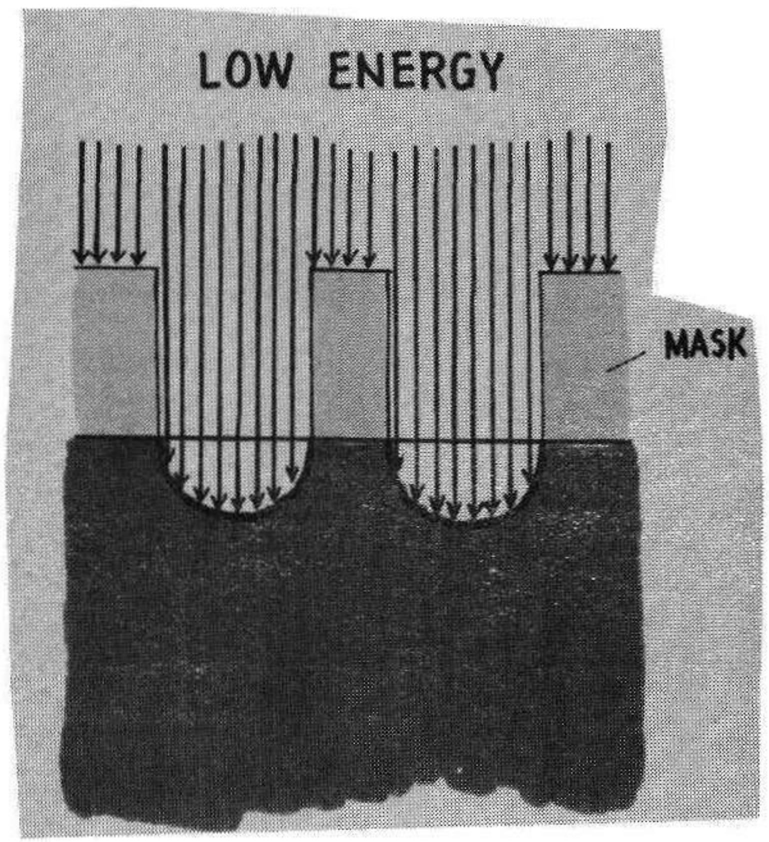
As Line Widths Decrease:

- Circuits get Shallower



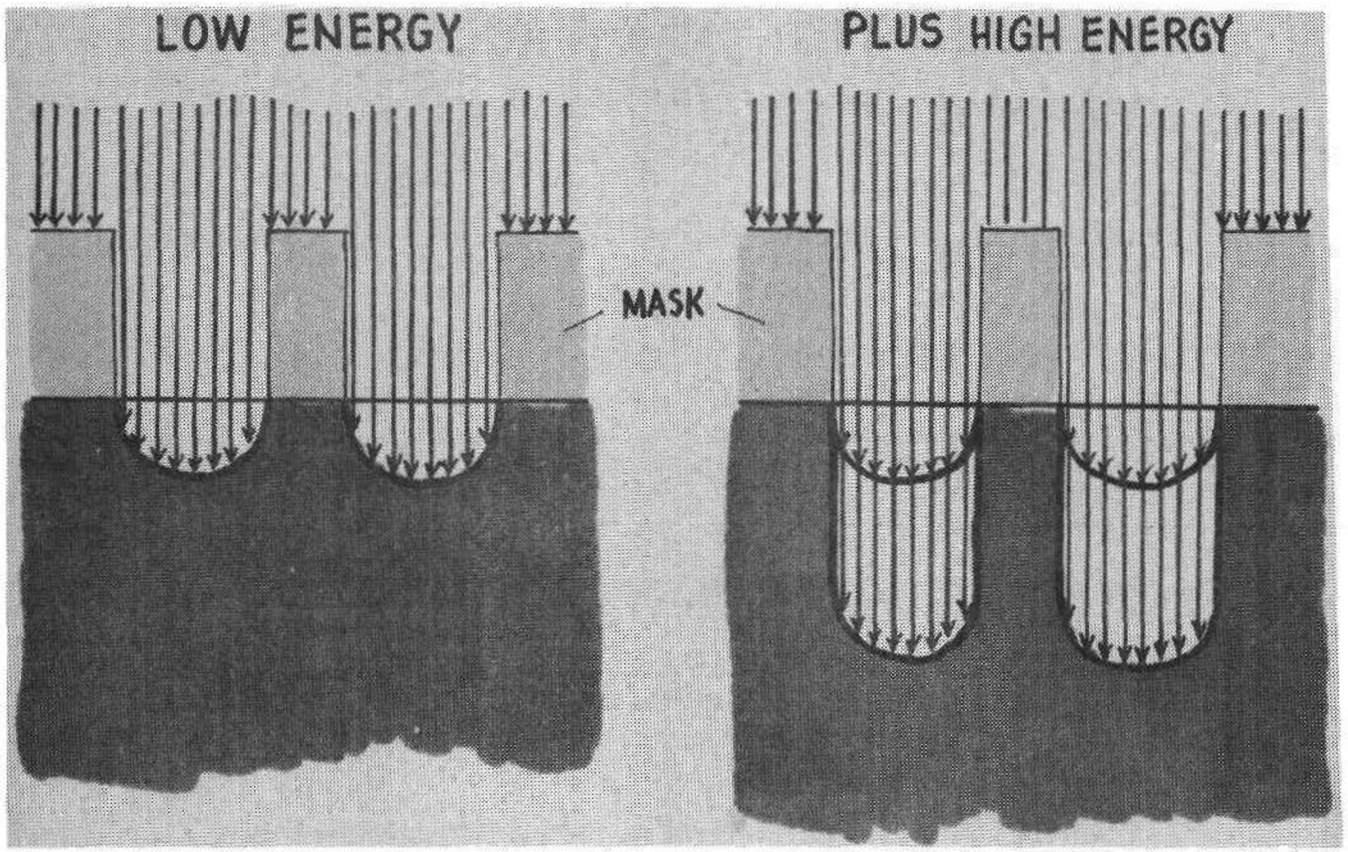
As Circuits get Shallower:

- The Implant Energy Decreases



As Circuits get Shallower:

- Higher Energy Implants may also become useful



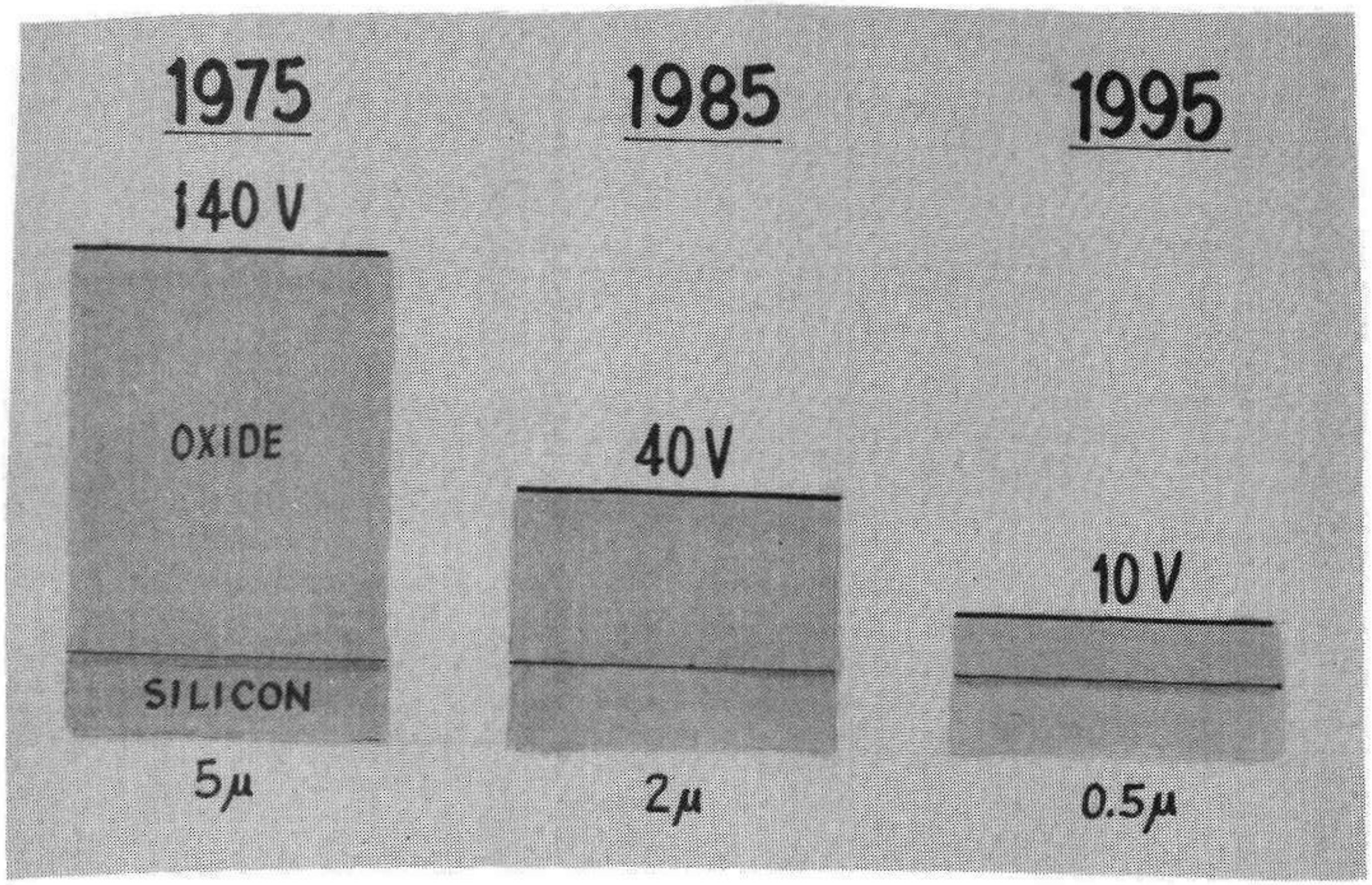
As Line Widths Decrease:

- Circuits get Shallower

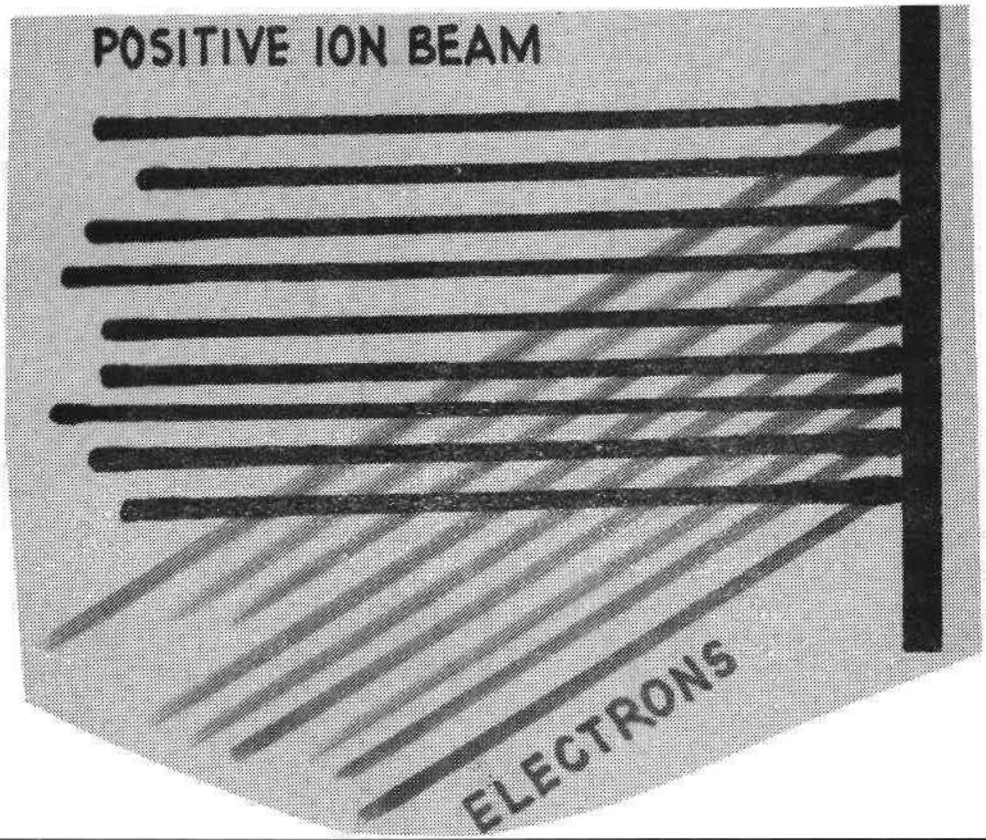
And Thinner Surface Oxides are Used:

- But Ion Beams Cause Surface
  Charging and
  - Thinner Oxides Withstand Lower Voltage

Thinner Oxides Withstand Lower Voltage



The Machine Solution is to Neutralize Surface Charge



As the Wafer Size Doubles (X2)

- The Wafer Area X4

- The Wafer Weight X6

As the Wafer Size Doubles (x2)

- The Wafer Area x4

The Machine Solution is to Increase the Beam Current

Present High Current		Future High Current
10mA	→	40mA

As the Wafer Size Doubles (x2)

- ***The Wafer Weight x6***

The Machine Solution is:

Automation and Robotic Handling

Summary

Device Requirement	Feature	Implantation Solution
Line Width Reduction	• Particulate Reduction • Mask Shadowing	• Automation & Robotic & Cleaner System • Implant Angle Control
Circuit Depth and Size Reduction	• Parasite Effects • Implant Energy Change • Wafer Charging	• Implant Buried Insulating Layer • Lower Energy Systems • Higher Energy Systems • Surface Charge Control
Wafer Size Increase	• Surface Area Increase • Wafer Handling	• Higher Beam Current Systems • Automation & Robotics

Conclusions

- Ion Implantation is to Here to Stay

- Device Requirements are Driving
  Equipment Changes

  Equipment Designers are Responding

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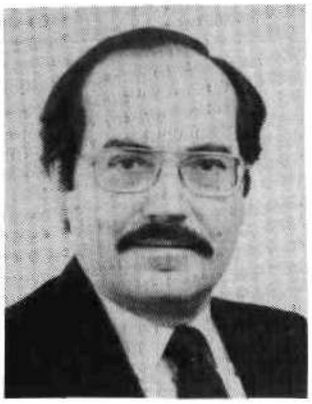
EQUIPMENT AND MATERIALS: A PERSPECTIVE FROM SEMS



Joseph Grenier
Senior Industry Analyst
Semiconductor Equipment and Materials Service
Dataquest Incorporated

Mr. Grenier is a Senior Industry Analyst for Dataquest's Semiconductor Equipment and Materials Service. He is responsible for analyzing the market environment and future technology trends. Prior to joining Dataquest, he was Product Marketing Manager at GCA Corporation, where he managed marketing activities for the reactive ion etch program. He was also International Marketing Manager at GCA, and was responsible for the overseas marketing of wafer processing equipment. Previously, he worked as a Product Manager at Varian Associates/Instrument Division, as a Systems Engineer at the USAF Satellite Test Center, and as a Test Engineer at General Motors' Noise and Vibration Laboratory. Mr. Grenier received a B.S.E.E. degree from the University of Detroit and an M.B.A. degree from the University of Santa Clara.

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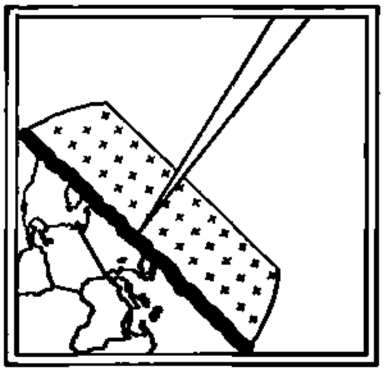


Recovery: Managing the New Industry Structure

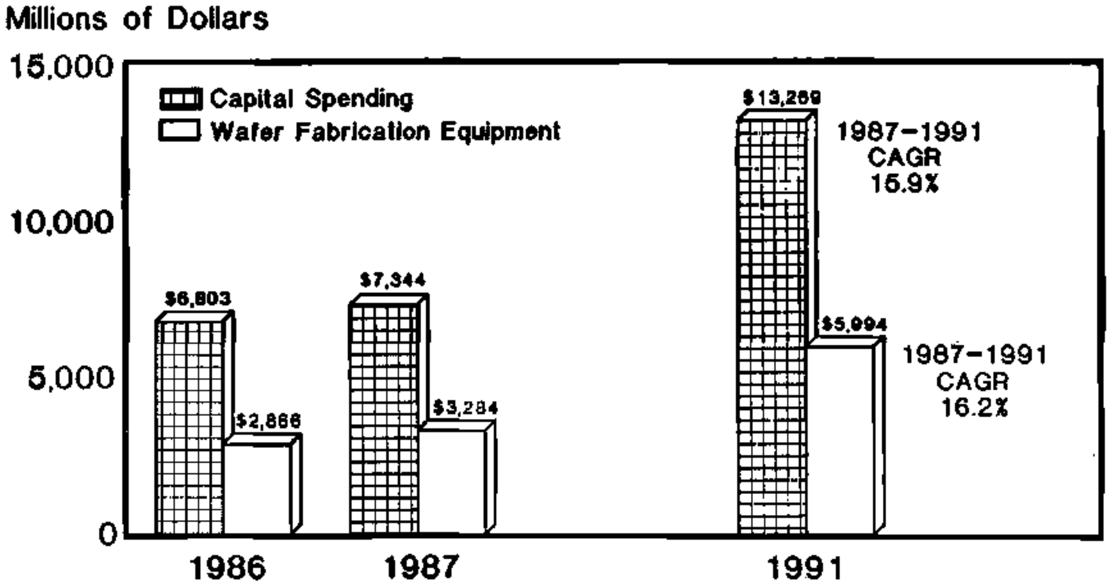
WAFER FABRICATION EQUIPMENT FORECAST

JOSEPH GRENIER
Senior Industry Analyst
Semiconductor Equipment and Materials Service
Dataquest Incorporated

WAFER FABRICATION EQUIPMENT SEGMENTS

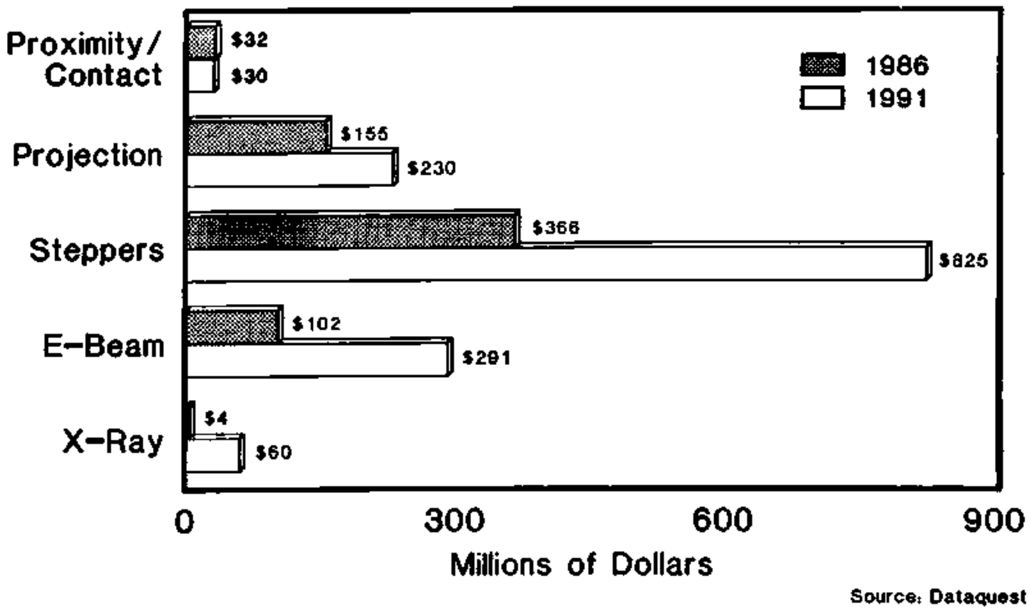
- Lithography
- Automatic Photoresist Equipment
- Etch and Clean
- Deposition
- Ion Implantation
- Rapid Thermal Processing
- Diffusion
- Process Control
- Factory Automation
- Other

ESTIMATED TOTAL SPENDING



Source: Dataquest

ESTIMATED LITHOGRAPHY SALES



ESTIMATED LITHOGRAPHY SALES

(Millions of Dollars)

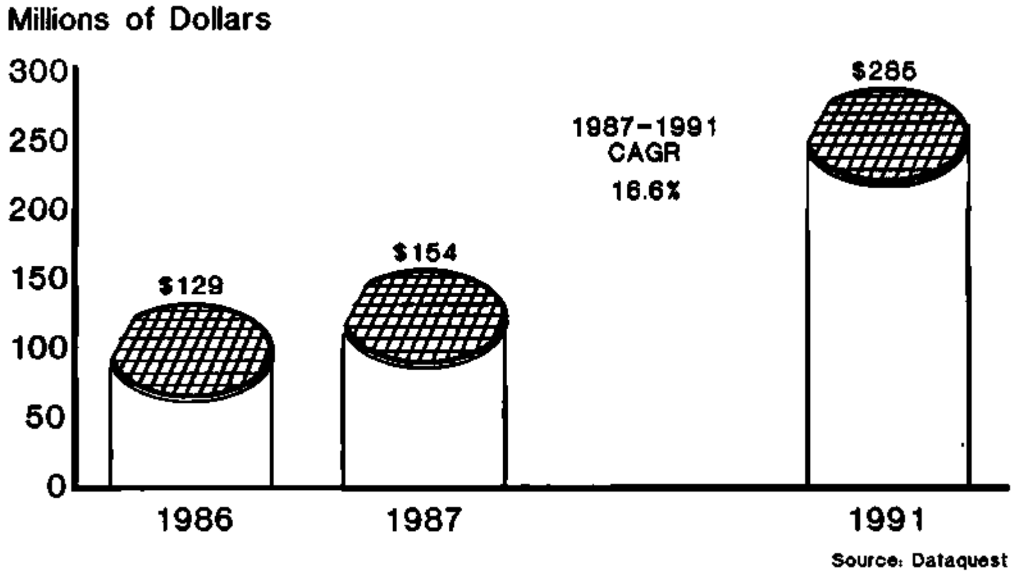
	1986	1987	1991	CAGR (1987-1991)
Proximity/Contact	$ 32	$ 28	$ 30	1.7%
Projection	155	165	230	8.7%
Steppers	366	440	825	17.0%
Direct Write E-Beam	30	50	147	30.9%
Maskmaking E-Beam	72	78	144	16.6%
X-Ray	4	10	60	56.5%
Total	$659	$771	$1,436	16.8%

Source: Dataquest

TRENDS

- Steppers
  - $1,000,000 submicron steppers
  - Intense competition
  - Technology push to 0.5 micron
- E-Beam
  - Direct write for niche markets
  - LPGs may impact maskmaking
- X-Ray
  - X-ray steppers now available
  - German/Japanese working on synchrotrons
- FIB
  - Much effort by the Japanese

ESTIMATED AUTOMATIC PHOTORESIST EQUIPMENT SALES



TRENDS

- Reduce contamination
- Interface to aligners
- Improve communications capability
- Process
  - Spin on glass (SOG)
  - Improve wafer prime

ESTIMATED ETCH AND CLEAN SALES

(Millions of Dollars)

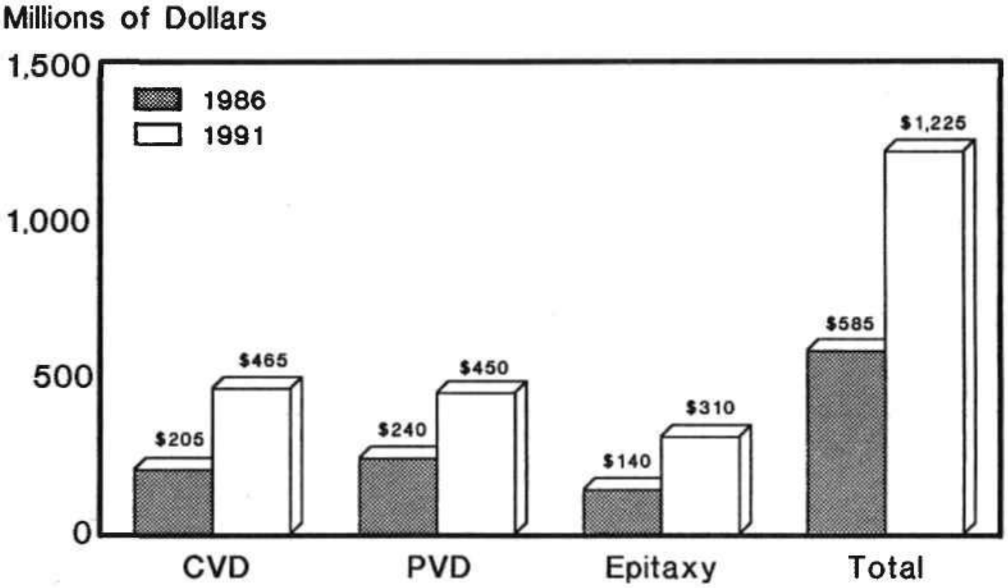
	1986	1987	1991	CAGR 1987-1991
Wet Process	$117	$123	$213	14.7%
Dry Strip	42	45	107	24.2%
Dry Etch	330	361	637	15.3%
Ion Milling	15	16	26	12.9%
Total	$504	$545	$983	15.9%

Source: Dataquest

TRENDS

- Wet process
  - Smart wet process stations with robotics
  - Chemical reprocessors
- Dry strip
  - Emergence of downstream single-wafer strippers
- Dry etch
  - Single-wafer vs. batch machines
  - New processes

ESTIMATED DEPOSITION SALES



Source: Dataquest

ESTIMATED DEPOSITION SALES

(Millions of Dollars)

	1986	1987	1991	CAGR 1987-1991
CVD	$205	$240	$ 465	18.0%
PVD	240	260	450	14.7%
Epitaxy	140	161	310	17.8%
Total	$585	$661	$1,225	16.7%

Source: Dataquest

TRENDS

- CVD
  - Emergence of dedicated CVD reactors
  - Emphasis on interconnection/dielectric processes
- PVD
  - Emphasis on planarization and step coverage
  - Reduction of particulates
- Epitaxy
  - High-throughput reactors for CMOS
  - MBE and MOCVD for III-V devices

ESTIMATED WAFER FABRICATION EQUIPMENT SALES

(Millions of Dollars)

	1986	1987	1991	CAGR 1987-1991
Ion Implantation	$200	$265	$498	17.1%
Rapid Thermal Processing	$ 20	$ 30	$ 95	33.4%
Diffusion	$191	$191	$155	(5.1%)

Source: Dataquest

TRENDS

- Ion implantation
  - High voltage for retrograde wells
  - Low voltage for shallow junctions
  - Low dose growing faster than high dose
- Rapid thermal processing
  - Introduction of new-generation machines
  - Implant anneal, reflow, silicide formation, gate oxide
  - Future – thin film deposition in seconds
- Diffusion
  - Market being eroded by alternative technologies
  - Furnace automation costly
  - Advent of vertical furnace

ESTIMATED WAFER FABRICATION EQUIPMENT SALES

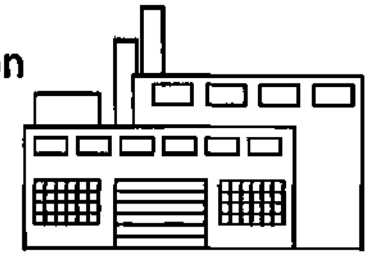
(Millions of Dollars)

	1986	1987	1991	CAGR 1987-1991
Process Control	$403	$463	$857	16.6%
Factory Automation	$ 70	$ 88	$250	29.9%
Other	$105	$116	$210	16.0%

Source: Dataquest

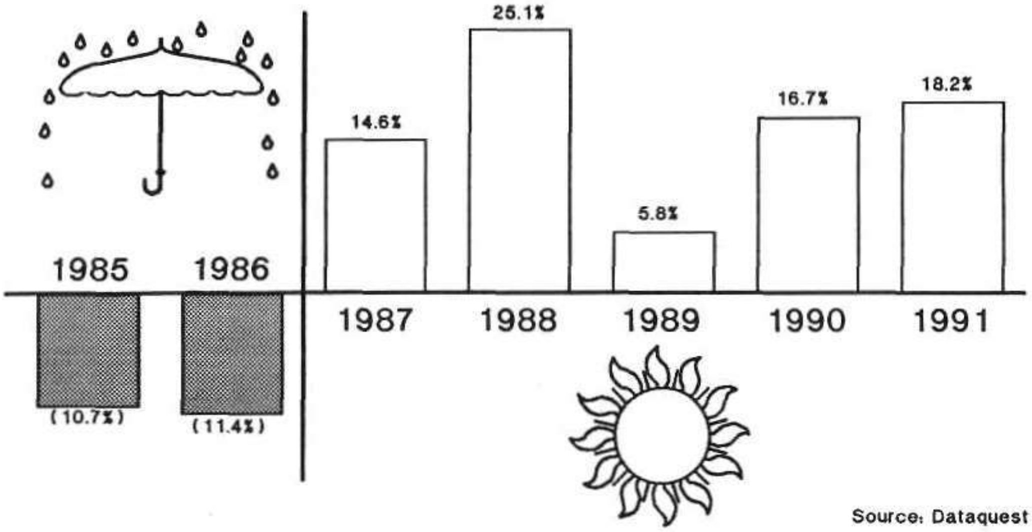
TRENDS

- Process control
  - Automatic wafer inspection
  - Automatic linewidth measurement
  - Necessary for factory automation
- Factory automation
  - No longer an issue – it has to happen!
  - United States lags Japan
  - Mechanization vs. automation



CONCLUSION

ESTIMATED WAFER FABRICATION EQUIPMENT GROWTH



Source: Dataquest

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EQUIPMENT AND MATERIALS:
A PERSPECTIVE FROM SEMS

Dr. Peggy Wood
Research Analyst
Semiconductor Equipment and
Materials Service
Dataquest Incorporated

Ms. Wood is a Research Analyst for Dataquest's Semiconductor Equipment and Materials Service. Her responsibilities include research and analysis of the semiconductor industry with respect to usage of materials in the semiconductor fabrication process and the technology and trends of semiconductor manufacturing automation. Prior to joining Dataquest, Ms. Wood was a postdoctoral research affiliate in the Department of Chemistry at Stanford University. While at Stanford, she supervised the installation of new research facilities and was responsible for the purchase of optical, electronic, and laser equipment. In addition to pursuing her own research in nonlinear chemical dynamics, Ms. Wood taught undergraduate laboratory courses and supervised graduate student research. Ms. Wood received a B.S. degree in Chemistry from California State University at Sacramento and a Ph.D. in Chemistry from Stanford University.

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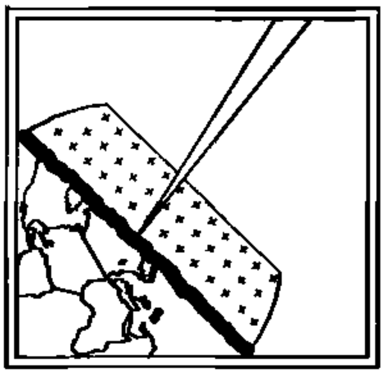
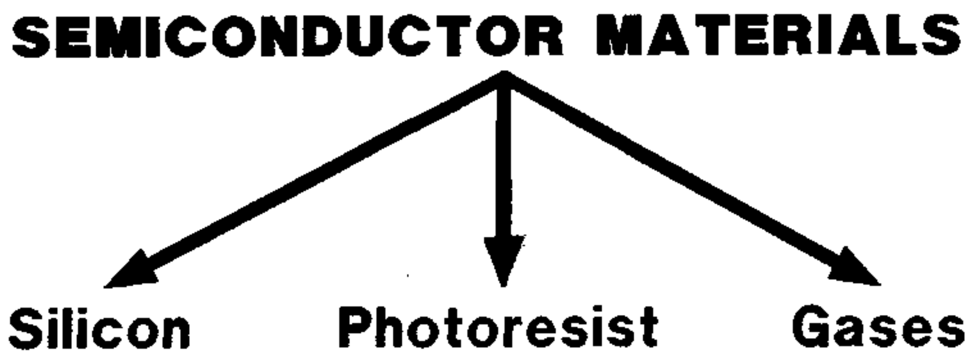


Recovery: Managing the New Industry Structure

WAFER FABRICATION MATERIALS FORECAST

PEGGY MARIE WOOD

Research Analyst
Semiconductor Equipment and Materials Service
Dataquest Incorporated


SEMICONDUCTOR MATERIALS
Silicon
Photoresist
Gases

SILICON MARKET

- Silicon wafers
- Epitaxial wafers

Merchant Silicon Companies	Captive Silicon Producers
Shin Etsu Handotai (SEH)	AT&T
Wacker	IBM
Monsanto	Motorola
Osaka Titanium	Texas Instruments

Source: Dataquest

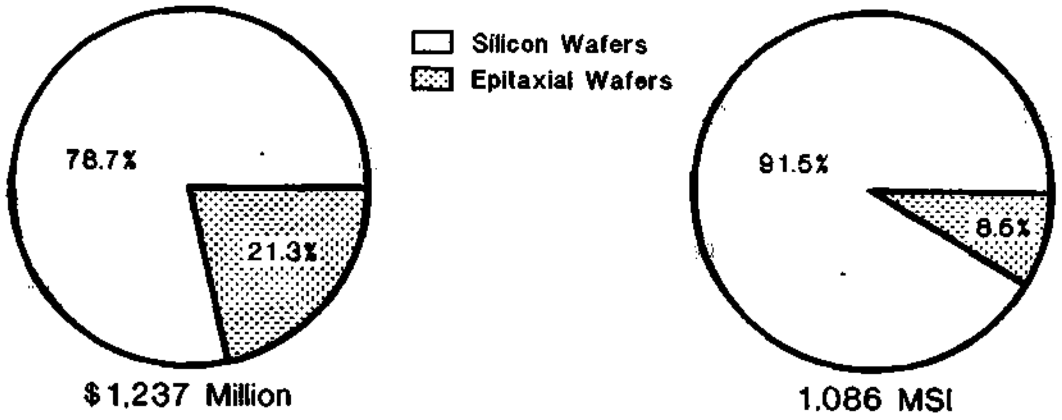
MERCHANT SILICON MARKET, 1985

Million Square Inches (MSI)

Region of Sales	Silicon Wafers	Epitaxial Wafers	Total
United States	327	31	358
Japan	479	51	530
Europe	130	7	137
ROW	58	3	61
Total	994	92	1,086

Source: Dataquest

MERCHANT SILICON MARKET, 1985



ASP – Silicon wafers $0.90–$1.00/square inch
– Epitaxial wafers $2.50–$3.00/square inch

Source: Dataquest

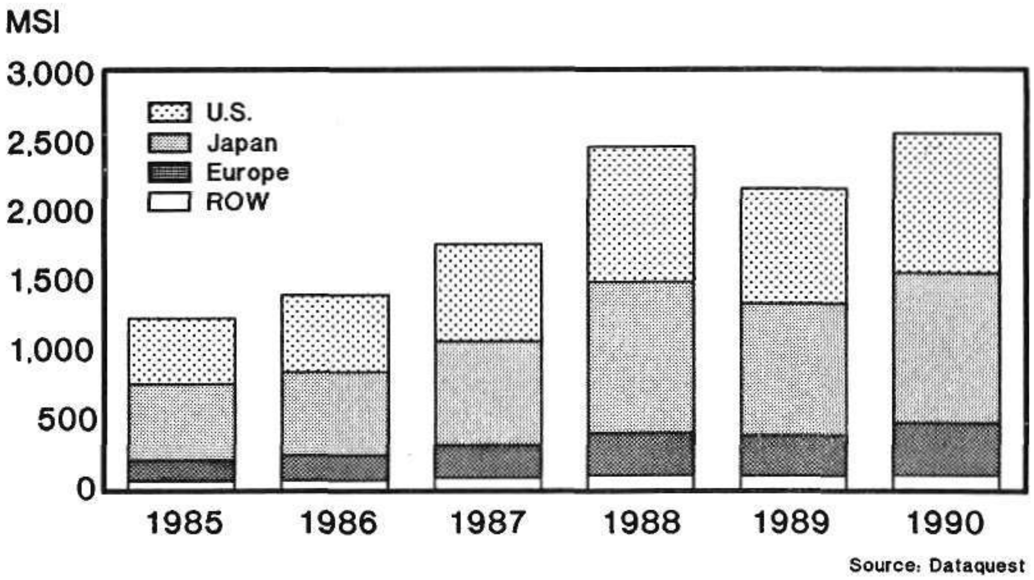
TOTAL SILICON MARKET, 1985

MSI

	U.S.	Japan	Europe	ROW
Merchant Silicon Companies	358	530	137	61
Captive Silicon Producers	120	20	10	--
Total	478	550	147	61

Source: Dataquest

WORLDWIDE SILICON CONSUMPTION FORECAST



WORLDWIDE SILICON CONSUMPTION FORECAST
(Million Square Inches)

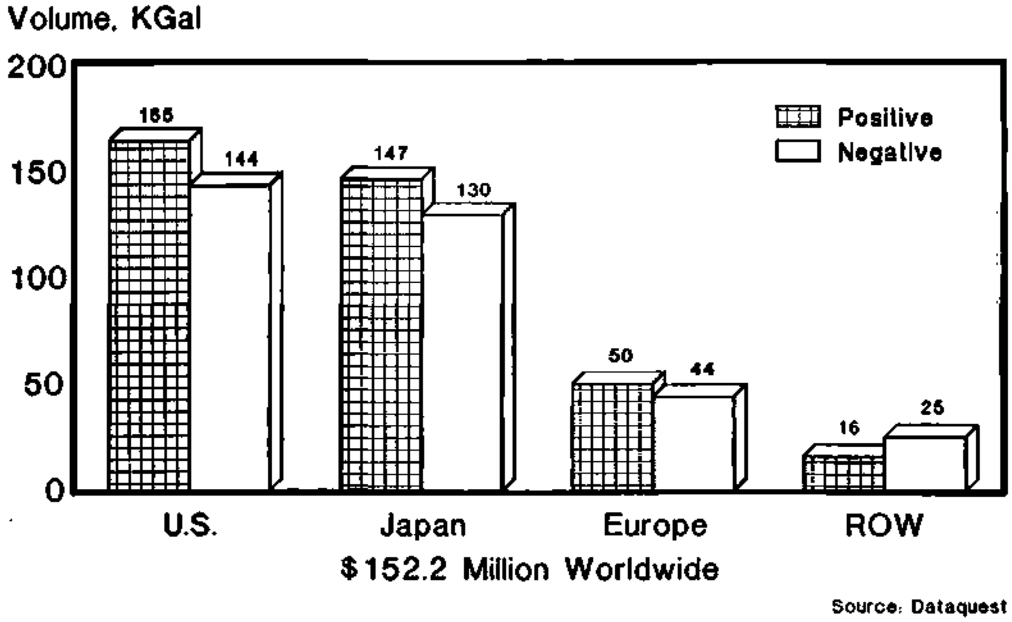
	1985	1986	1987	1988	1989	1990	CAGR 1985-1990
WW Silicon	1236	1404	1770	2477	2172	2573	15.8%
Growth	-21.1%	13.6%	26.1%	39.9%	-12.3%	18.5%	
UNITED STATES	478	560	704	981	837	1014	16.2%
Growth	-32.4%	17.0%	25.8%	39.3%	-14.7%	21.2%	
JAPAN	550	600	750	1093	949	1082	14.5%
Growth	-14.3%	9.1%	25.0%	45.8%	-13.2%	14.0%	
EUROPE	147	177	233	303	294	375	20.6%
Growth	- 4.1%	20.6%	31.7%	30.0%	- 2.8%	27.4%	
ROW	61	67	83	99	91	101	10.7%
Growth	- 3.2%	10.4%	23.1%	19.9%	- 8.0%	10.8%	

SOURCE: Dataquest
September 1986

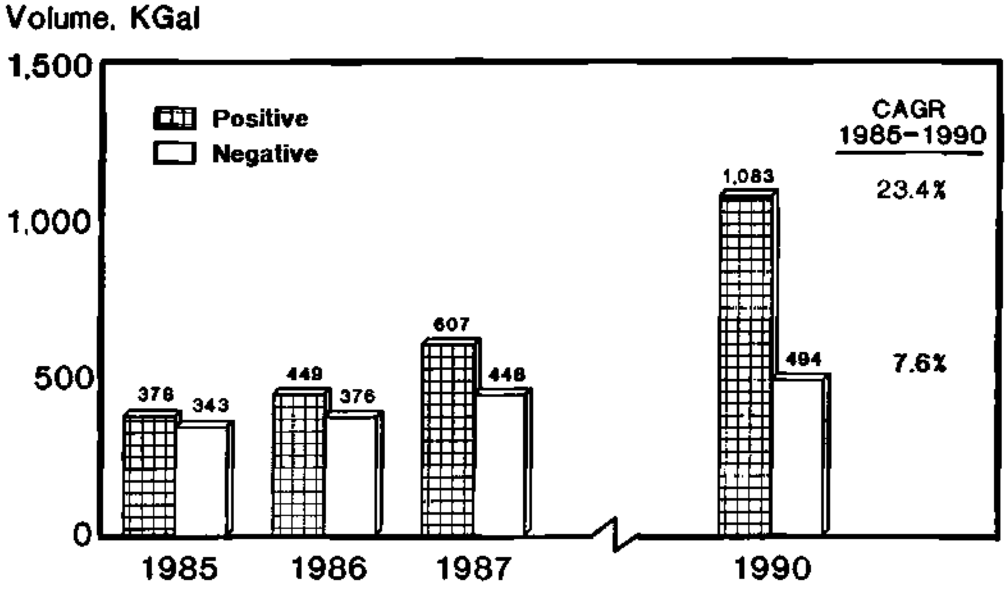
SILICON OUTLOOK

- Decreasing captive silicon production
- Epi wafer market outlook
- Silicon suppliers
  - New entrants and acquisitions

PHOTORESIST MARKET, 1985

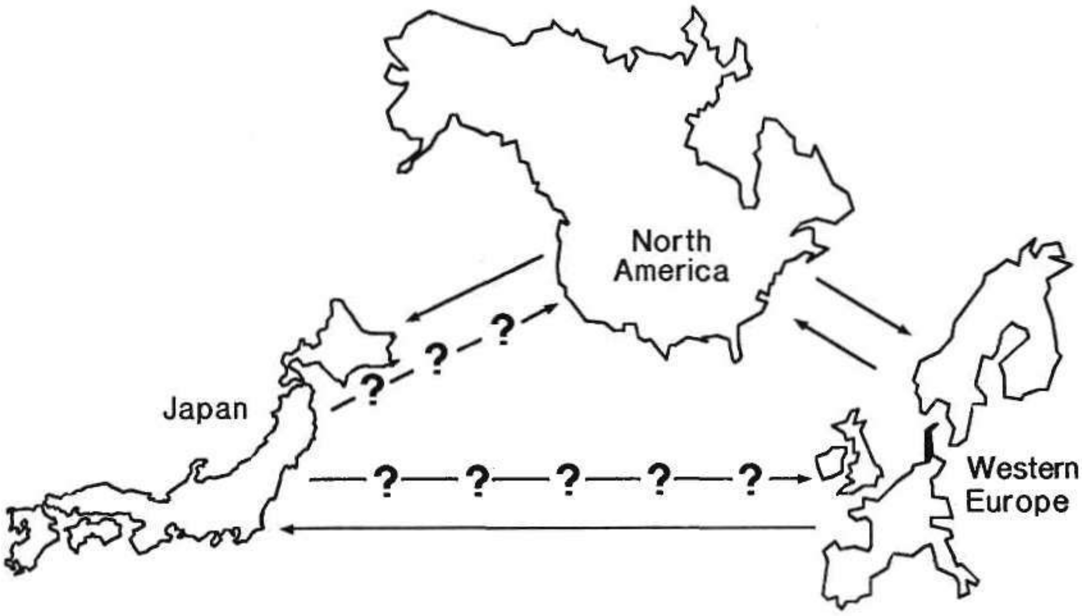


WORLDWIDE PHOTORESIST FORECAST

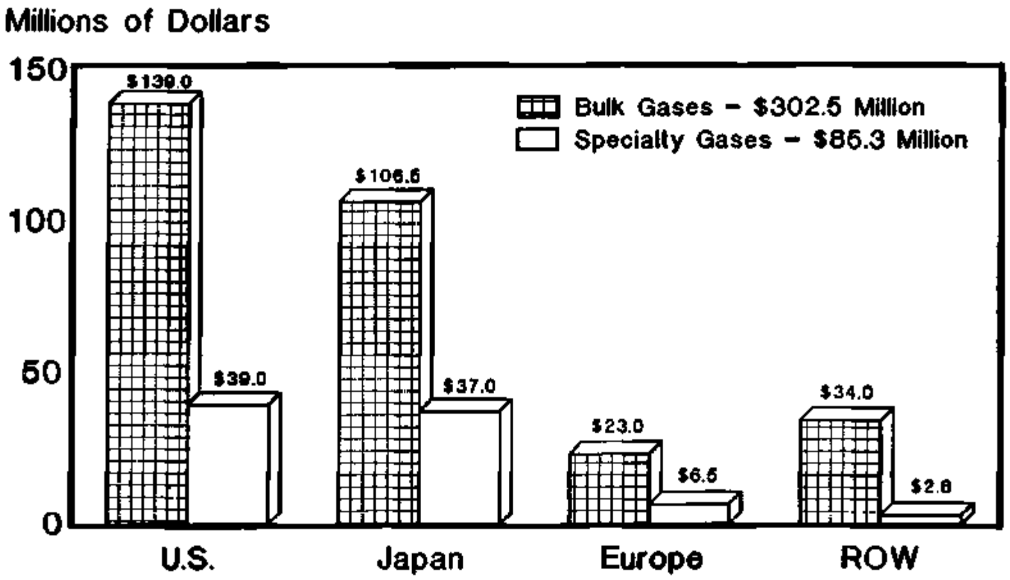


Source: Dataquest

PHOTORESIST OUTLOOK



SEMICONDUCTOR GAS MARKET, 1985



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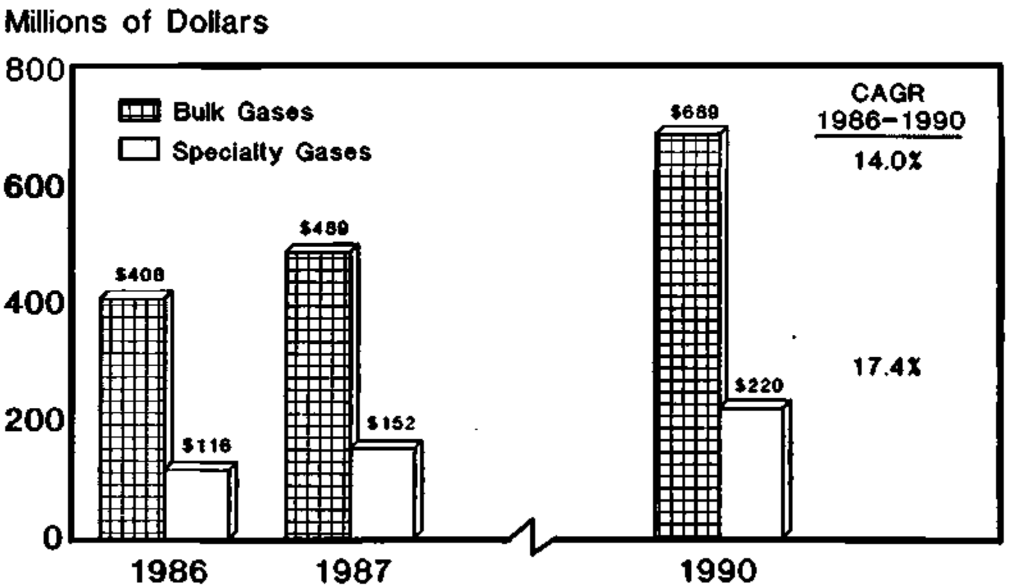
SEMICONDUCTOR GAS FORECAST

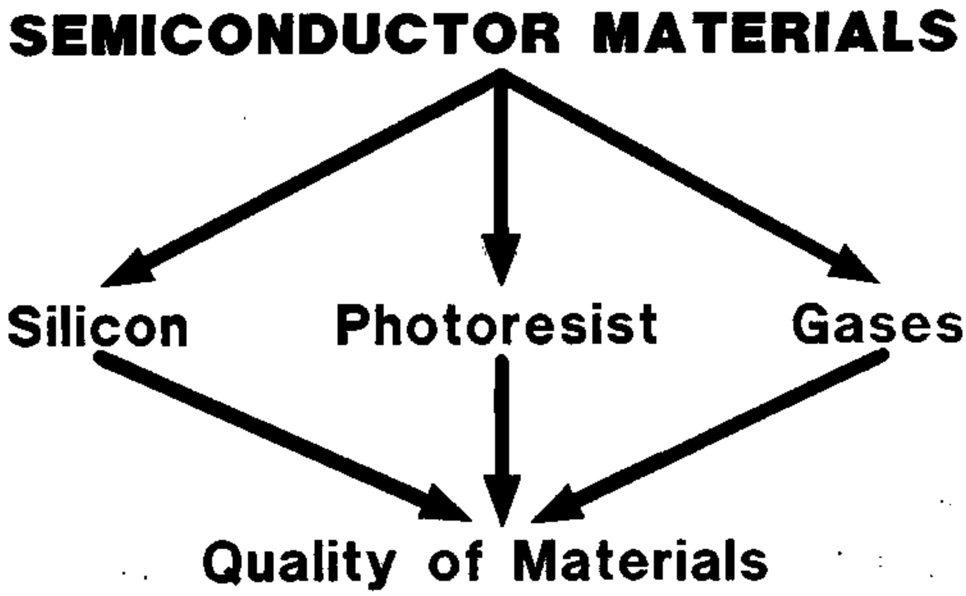


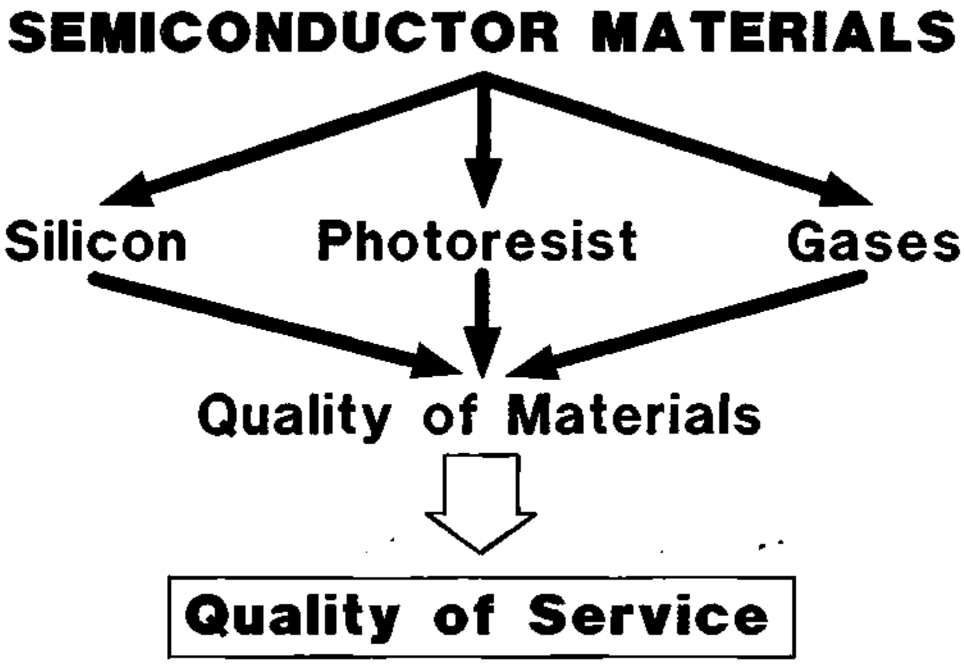
Source: Dataquest

SEMICONDUCTOR GAS OUTLOOK

Bulk and specialty gases – two different markets, two different strategies

- Bulk
  - Nitrogen market stability
  - Long-term contracts
- Specialty
  - Large product mix
  - Multiple suppliers per fab


SEMICONDUCTOR MATERIALS
Silicon
Photoresist
Gases
Quality of Materials


SEMICONDUCTOR MATERIALS
Silicon
Photoresist
Gases
Quality of Materials
Quality of Service