Japanese Semiconductor Industry Service

Volume II
Technology & Government

Dataquest

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Introduction to the Service

The Japanese Semiconductor Industry Service (JSIS) documents, analyzes, and interprets all important aspects of the Japanese semiconductor industry and the Japanese manufacturers that participate in the world markets. The service comprises:

- Three loose-leaf data base binders containing sections that are continuously revised and updated as developments occur or additional information becomes available
- Timely newsletters reporting on significant industry developments--additional binders are provided for these newsletters
- I.C. ASIA, a semimonthly report on the Japanese and Asian integrated circuit industry, and I.C. USA, a semimonthly report on the U.S. integrated circuit industry, focusing on start-ups, strategic alliances, and government activity
- Direct access to research staff in Tokyo and San Jose for background information and questions pertaining to information contained in each volume

The service analyzes, interprets, and reports on the products, markets, and strategies of the major Japanese companies in the semiconductor industry, with a specific focus on the Japanese market. This service also presents valuable information on Japanese government, economy, and industrial policy, and will provide periodic pertinent updates to these subjects. JSIS provides data with which to make strategic decisions. We perform the following functions:

- Track Japanese semiconductor production, inventory, shipments, exports, imports, and consumption for the major products
- Forecast 10-year consumption figures for all semiconductor categories
- Examine and analyze the consumer and industrial electronics end-user markets
- Analyze trends in CAD tools and plant automation
- Analyze trends in strategic alliances

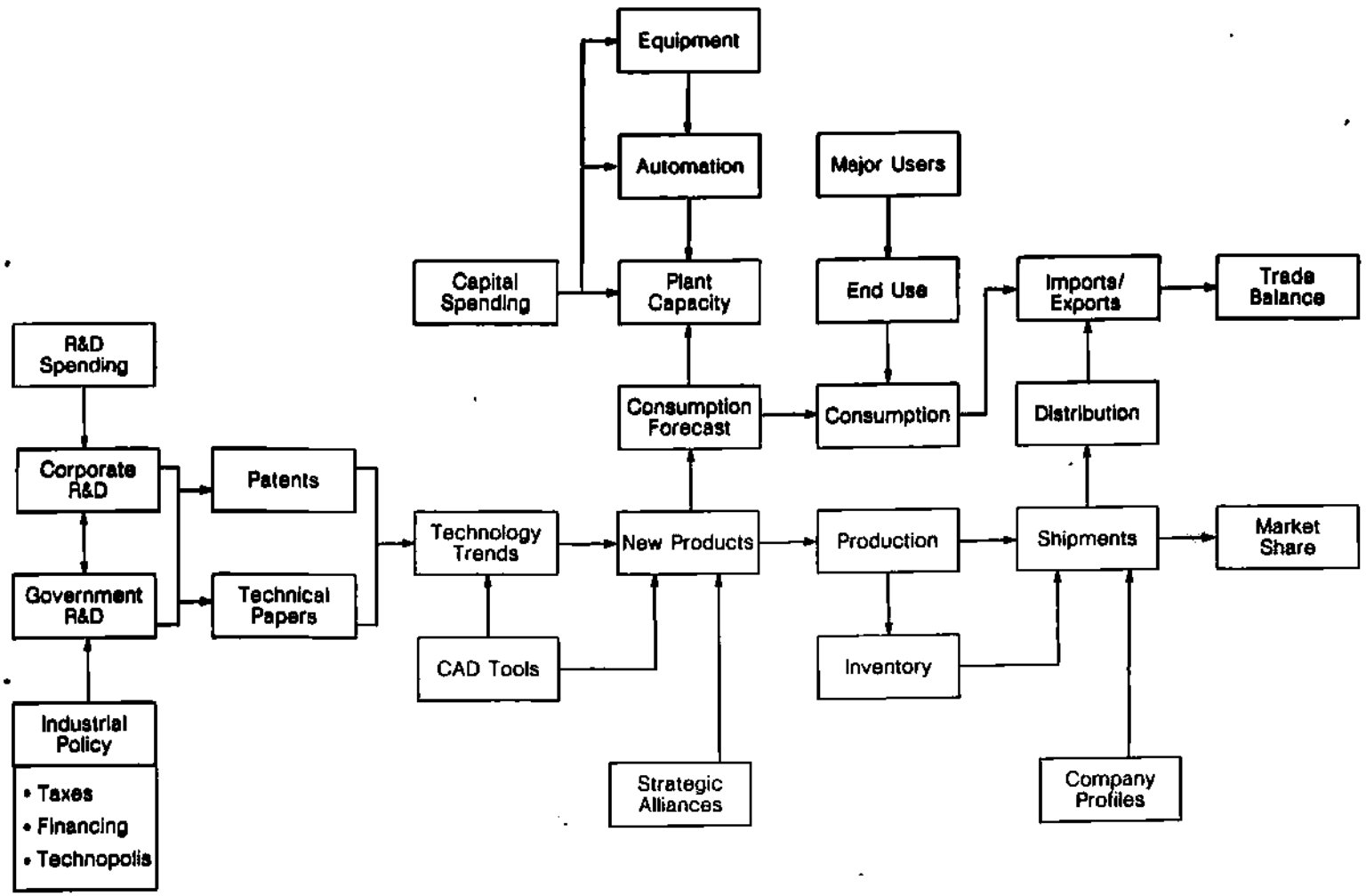
Introduction to the Service

- Monitor Japanese R&D projects and corporate spending for the following areas:
  - Semiconductors
  - Computers
  - Telecommunications
- Issue periodic reports on trends in patent applications and technical papers
- Analyze semiconductor technology trends on a quarterly basis
- Evaluate plant capacity expansion and design center activity
- Profile the major Japanese semiconductor companies, emphasizing their products and strategies
- Analyze the forces affecting the Japanese semiconductor markets
- Investigate the fundamental operation of Japanese industries

Dataquest monitors the Japanese Semiconductor Industry using the system shown in Figure 1. Generally, we observe that R&D projects precede new products by four to eight years; technical papers and patents precede new products by three to four years.

Figure 1

JAPANESE SEMICONDUCTOR INDUSTRY ANALYSIS



Source: Dataquest
April 1987

Introduction to the Service

NEED FOR THE SERVICE

Since 1975, Dataquest's Semiconductor Industry Service has offered comprehensive worldwide market research to semiconductor manufacturers, semiconductor users, and suppliers of semiconductor manufacturing equipment and materials. As individual geographical markets expanded, it became obvious that each of these areas was developing its own unique characteristics. This was especially true of Japan, since it has become a major industrial power and, in fact, has attained the number one position in the world for merchant market semiconductor unit and value production.

Much has been written on the Japanese, but there is no other single detailed, comprehensive, continuously updated and unbiased analytical service in the semiconductor market. With the movement of both finished and unfinished semiconductor products across geographical borders, available industry statistics sources have become less useful. Hence, there is a growing need for the type of data that Dataquest provides through its continuous industry coverage, updated data base, and analyses of observed trends.

SERVICE STRUCTURE AND TERMINOLOGY

Detailed discussions of semiconductor consumption, production, and shipments are broken out in three ways:

- Product technology
- Product function for integrated circuits
- End-user market

Product Technology

Total Semiconductor

- Integrated Circuits
  - Bipolar digital--This category includes all monolithic bipolar digital logic and memory devices.
  - MOS--This includes all monolithic digital MOS memory and logic devices; this total is further divided into PMOS, NMOS, and CMOS.

- Linear--This includes all linear integrated circuits; hybrids manufactured and packaged by the same company are included.

- Discrete
  - Transistors
    - Small-signal transistors--Silicon or germanium transistors with a power dissipation of less than one watt; includes all radio frequency and microwave small-signal transistors, dual transistors, field-effect transistors, and general-purpose bipolar signal transistors
    - Power transistors--Silicon or germanium transistors with a power dissipation of one watt or more; includes radio frequency and microwave power transistors and Darlington power transistors
  - Diodes
    - Small-signal diodes--All diodes rated at less than one ampere; includes microwave diodes, varactor tuning diodes, tunnel diodes, and discrete rectifiers
    - Power diodes--All diodes rated at more than one ampere; includes all discrete rectifiers and assemblies thereof with current ranges of more than one ampere, selenium rectifiers, and other polycrystalline devices
    - Zener diodes--All voltage reference and regulator diodes
  - Thyristors--Includes all unidirectional and bidirectional thyristors
  - Other discrete--Includes all discrete devices not specifically classified above

- Optoelectronics--This group is further divided into LED lamps, LED displays (single- or multidigit), couplers, and other. The "other" category includes photo transistors, photo diodes, photo conductive devices, and infrared lamps. Not included are solar cells, liquid crystal devices and displays, and incandescent lamps and displays.

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Product Function for Integrated Circuits

- Total bipolar digital ICs
  - Memory
  - Logic
- Total MOS digital ICs
  - Memory
  - Micro devices
  - Logic
- Total linear ICs

End-User Market

- Consumer electronics
  - Video
  - Audio
  - Home appliances
- Industrial electronics
  - Computers
  - Commercial peripherals
  - Word processors
  - Communication
  - Industrial
  - Transportation

Introduction to the Service

SERVICE ORGANIZATION

Throughout the JSIS three-ring binders, the terms factory shipments and production are particularly significant when used in conjunction with geographical regions. The term factory shipments refers to devices produced and shipped in a particular region, but the term production refers to the country in which a company has its headquarters. For example, devices produced by an Hitachi subsidiary in the United States would be counted in U.S. factory shipments, but would also be counted as part of the Japanese companies' total production.

Volume I--Markets

Volume I contains specifics of the semiconductor industry both in Japan and overseas. It is divided into the following sections:

- History of the Industry--Discusses the history of the industry, distribution and sales channels to the market, production, and productivity figures
- Production/Consumption--Contains Japanese semiconductor shipments, production, consumption history, and consumption forecasts
- Market Share Estimates--Contains worldwide shares for the major Japanese manufacturers and market shares in Japan for the major Japanese, U.S., European, and Rest of World manufacturers
- Exports/Imports--Analyzes Japanese exports, imports, and balance of trade in the major semiconductor families, particularly emphasizing trade between the United States and Japan
- Market Access--Analyzes history and status of the U.S.-Japan Semiconductor Trade Arrangement; also includes monthly statistics on selected electronic equipment markets in Japan, such as copiers, personal computers, and DAD players
- Semiconductor End Use--Analyzes the major semiconductor products that are used in the consumer and industrial markets and the major subsections of those markets; explores specific application trends such as VTRs, personal computers, robotics, and facsimile machines; examines who buys what and how much
- Distribution--Analyzes trends in Japanese semiconductor sales through distribution; explains who the major distributors are; examines differences between distribution in Japan and the United States

Introduction to the Service

- Electronics Industry--Provides an overview of the Japanese electronics industry, including the increasing part that the electronics industry plays in Japan; includes annual production forecast and history of 50 specific categories of electronic equipment

Volume II--Technology and Government

Volume II of JSIS contains separate sections for each of the following:

- Technology--Discusses major trends in Japanese semiconductor technology
- Strategic Alliances--Analyzes joint venture, licensing, and second-sourcing agreements entered by Japanese semiconductor device and equipment makers
- Start-ups/Newcomers--Reviews trends among semiconductor start-up companies and major Japanese companies entering the industry
- Corporate R&D--Evaluates trends in corporate R&D spending and the opening of new basic research laboratories
- Government R&D--Reviews the major national R&D projects covering semiconductors, computers, and telecommunications
- Industrial Policy--Explores MITI's administrative guidance of industry. Discusses MITI's relationship with the high-technology industries, with details on the growth of specific strategic industries
- INS Program--Describes Nippon Telegraph and Telephone's Information Network System (INS) development plans
- Technopolis Sites--Reviews the 19 high-technology research cities planned by MITI
- Design Centers/ASICs--Analyzes trends among Japanese vendors and design centers
- CAD Tools/Artificial Intelligence--Examines CAD trends and the growing use of expert systems in VLSI
- Plant Capacity--Analyzes plant capacity additions in Japan and lists semiconductor plants, by company

- Economy--Presents macroeconomic statistics on industrial production, capacity utilization, exports, imports, balance of payments, plant and equipment expenditures, wholesale and consumer prices, inventories, and financial data for the major industries

Volume III--Companies

The third volume includes profiles of major Japanese merchant semiconductor companies, including analyses of sales channels, financial structure, and product portfolios. It also includes examinations of factory locations, their technologies, and their organizational structures. Semiconductor revenues for most companies are split by geographical region.

The companies covered include:

- Fuji Electric
- Fujitsu
- Hitachi
- Matsushita
- Mitsubishi
- NEC
- NTT
- Oki
- Rohm
- Sanken
- Sanyo
- Seiko Epson
- Sharp
- Sony
- Toshiba

Introduction to the Service

SERVICE FEATURES AND PROCEDURES

The date of preparation is noted on the bottom of each page of a document. Sections are updated on a regular basis, and filing instructions are sent with the new versions. A complete table of contents is produced on a regular basis to enable you to verify that your binders are current and complete.

Newsletters are published at monthly intervals and should be filed in the Newsletter binder. The newsletters are devoted to current topics of specific Japanese interest and to international industry developments.

The inquiry privilege permits the binderholder to contact Dataquest by mail, fax, telegram, telephone, telex, or in person to request copies of printed material, data, or opinions on topics covered by the Japanese Semiconductor Industry Service staff. The principal information collections are maintained at our San Jose, California, headquarters and, with the exception of confidential or proprietary material, are available to all our subscribers. We also have a research staff in Tokyo that maintains pertinent information on the material contained in the JSIS data base.

Introduction to the Service

DATAQUEST LOCATIONS

The Japanese Semiconductor Industry Service (JSIS) has its headquarters in our San Jose, California, office. Clients in Europe, the United States, or Latin America should address their inquiries to this headquarters office. JSIS also maintains a staff in our Tokyo office; inquiries from subscribers in Japan and Asia should be addressed to our Tokyo office.

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JAPANESE SEMICONDUCTOR INDUSTRY SERVICE STAFF CAPABILITIES

The Dataquest Japanese Semiconductor Industry Service staff has a continuing, long-term commitment to the semiconductor and related electronic industries. The expertise and experience of the worldwide Semiconductor Industry Service staff and access to the resources of other Dataquest high-technology industry groups further enhances the quality of our service.

Introduction to the Service

Members of Dataquest's professional staff are frequent speakers at industry seminars and symposia. We participate in the leading professional societies related to the electronics industry. We maintain contact with a large user base through sophisticated sampling and interviewing techniques. Our staff regularly reviews all important publications related to the semiconductor industry and associated user industries.

SERVICE STAFF

Gene Norrett

Mr. Norrett is Vice President and Director of Dataquest's Semiconductor Industry Group. Mr. Norrett is based in the Dataquest corporate headquarters and directs research staffs in the San Jose and Tokyo offices. Prior to joining Dataquest, Mr. Norrett spent 14 years with the Motorola Semiconductor Group, serving in various marketing and management positions. He was most recently Manager of Market Research, where he was responsible for research analysis of worldwide semiconductor industry trends. In this capacity, he served as the company's representa- tive to the Semiconductor Industry Association and was Chairman of the Association's Trade Statistics Committee. Mr. Norrett has traveled extensively in Japan, Hong Kong, Taiwan, Korea, China, and Europe and has developed an awareness and thorough understanding of their semiconductor markets. His educational background includes a B.A. degree in Mathematics from Temple University and an M.S. degree in Applied Statistics from Villanova University. He has also taken graduate courses in marketing from Arizona State University.

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Osamu Ohtake

Mr. Ohtake is the Tokyo-based Associate Director for Dataquest's Japanese Semiconductor Industry Service and is responsible for strategic research on technologies, markets, products, and manufacturers. Prior to joining Dataquest, Mr. Ohtake worked for 10 years as a reporter and then most recently as Components Group Manager for Dempa Shimbun, a daily electronics industry newspaper published in Japan. He has also authored reports on the Japanese VLSI project and on semiconductor materials and equipment markets. A native of Japan, Mr. Ohtake is a graduate of Tokyo Denki University, specializing in telecommunications.

Sheridan M. Tatsuno

Mr. Tatsuno is a Senior Industry Analyst working for Dataquest's Japanese Semiconductor Industry Service. He is responsible for analyzing trends in Japanese government policies, procurement, financial markets, industrial financing, subsidized R&D, overall economics, and industrial plant siting. Prior to joining Dataquest, he had seven years of experience in market research, planning, and international finance with Bechtel and Woodward-Clyde Consultants. Mr. Tatsuno has a B.A. degree in Political Science from Yale University and a Master's degree in Planning and Policy Analysis from Harvard University's Kennedy School of Government. In addition to these credentials, Mr. Tatsuno is fluent in Japanese, French, and Spanish.

Introduction to the Service

Patricia S. Cox

Mrs. Cox is an Industry Analyst for Dataquest's Japanese Semiconductor Industry Service and Product Manager for the semimonthly I.C. ASIA and I.C. USA newsletters. She is responsible for maintaining Japanese export, import, shipments, production, and consumption data; collecting market share data; performing in-depth company analyses; managing the computerized statistical data base; and performing general research duties. Mrs. Cox has five years of market research experience. Before joining Dataquest, Mrs. Cox was Contract Administrator at a New Jersey management information firm. Mrs. Cox received a Bachelor's degree and a Master's degree from Indiana University.

Kazunori Hayashi

Mr. Hayashi is an Industry Analyst for Dataquest's Japanese Semiconductor Industry Service and is based in Tokyo. He covers the semiconductor equipment and materials area. Among his responsibilities are researching and compiling the JSIS capacity analysis data base and updating the semiconductor equipment and materials data base.

Prior to joining Dataquest, Mr. Hayashi was a co-founder of Innov Japan and Techno System Research Coporation. He has had 12 years experience in the industry. During this time, he has authored publications and performed research and consulting on the Japanese semiconductor equipment industry.

Mr. Hayashi is a graduate of Meiji University in commercial sciences.

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Nagayoshi Nakano

Mr. Nakano is a Research Analyst for Dataquest's Japanese Semiconductor Industry Service and is based in Tokyo. He is responsible for gathering information, researching, analyzing, and compiling the JSIS end-use data base, and providing general research support on the Japanese market. Prior to joining Dataquest, Mr. Nakano worked for six years as a journalist, most recently as associate editor for the foreign correspondent department of Dempa Shimbun, Japan's largest daily electronics industry newspaper. Mr. Nakano is a graduate of Doshisha University, Kyoto, where he majored in English Linguistics.

Hideaki Nemoto

Mr. Nemoto is a Research Associate for Dataquest's Japanese Semiconductor Industry Service and is based in Tokyo. He is responsible for the translation and editing of the Japanese-language I.C. USA newsletter, gathering MITI and Ministry of Finance statistics, handling client inquiries, and providing general research support on the Japanese market.

Prior to joining Dataquest, Mr. Nemoto worked for two years as a foreign correspondent for Dempa Publications, Inc.

Mr. Nemoto is a graduate of Doshisha University.

Introduction to the Service

SUBSCRIPTION TERMS

Basic Terms

The Service begins on the date of the first billing. At that time, the notebook holder receives four service binders containing complete, up-to-date material and copies of all recent newsletters. Additionally, the notebook holder receives I.C. ASIA and I.C. USA binders. For the duration of the subscription, the notebook holder receives a copy of each additional or replacement section of the notebook and each newsletter published. Direct access to service staff may be used for questions related to the Japanese Semiconductor Industry Service.

Add-On Subscriptions

Subsidiaries, divisions, regional offices, majority-owned affiliates, and parent companies of the subscribing organization are eligible for add-on subscriptions at a fraction of the base price for each additional subscription.

Relationship to DATAQUEST's Semiconductor Industry Service

The Japanese Semiconductor Industry Service (JSIS) is intended to complement the existing Semiconductor Industry Service (SIS), and topics of broad general interest such as discussions of technological advances will only be covered to the extent that they specifically affect Japan. These companion services are offered separately as components of Dataquest's international semiconductor industry program.

Base Price and Payment Terms

Industrial clients will be billed for the full price of the service on an annual basis. Dataquest reserves the right to raise its subscription prices to reflect broadened scope or increased costs. Subscribers will be notified in advance of any such price increase.

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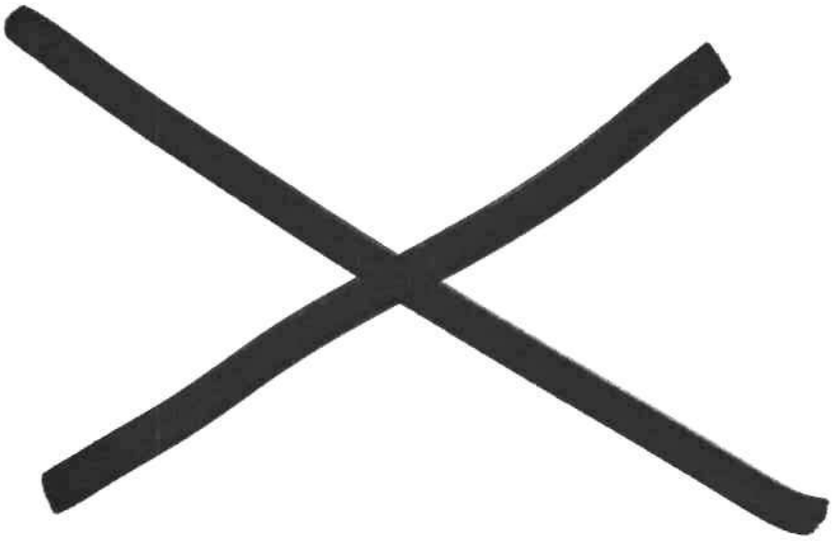

Technology Trends

The following is a list of the material in this section:

- Technology Trends 1st Quarter 1986
- Technology Trends 2nd Quarter 1986
- Technology Trends 3rd Quarter 1986
- Technology Trends--Fourth Quarter 1986
- Technology Trends 1st Quarter 1987
- Technology Trends Second Quarter 1987

NOTE: The arrow symbol indicates the latest documents's location behind this subject tab.

Technology Trends
1st Quarter 1986

SUMMARY

"Science fiction or reality?" Within the last two years, DATAQUEST has observed that many technologies viewed as science fiction in the West, such as bioelectronics, synchrotron radiation, and automated translation systems, are being seriously pursued by Japanese companies in the research laboratory. Whether this situation suggests growing conservatism in western corporate research or differing market perspectives is open to debate, but one thing is clear: Japanese companies view bioelectronics, optoelectronics, and expert systems as commercializable technologies.

Given this growing difference between Japanese and western semiconductor research attitudes and goals, we wonder if U.S. and European companies are prematurely forfeiting future technologies and markets, or whether Japanese industry will look radically different from that in the West in ten years. In the past, Japanese semiconductor makers were heavily consumer-oriented, but are now shifting to industrial applications. In the West, semiconductor research is greatly influenced by military and space programs. With the search for new applications, this divergence in semiconductor technology trends raises major questions about the future competitiveness of Japanese and western manufacturers. In particular, we note the following:

- Will Japanese companies also dominate industrial electronics?
- Will U.S. and European companies retreat to military markets and commercial niche markets?
- Will U.S.-Japanese cooperation in military research channel Japanese technology to U.S. suppliers or lead to Japanese commercialization of U.S. military technology?
- Will western companies maintain R&D spending while investing in manufacturing automation?
- Will western companies establish next-generation research centers to match the 76 basic research laboratories in Japan?

DATAQUEST believes that these types of strategic issues must be addressed now if companies are to retain their international competitiveness in the 1990s.

Technology Trends
1st Quarter 1986

MAJOR TECHNOLOGY TRENDS

During the first quarter of 1986, DATAQUEST observed the following trends in Japanese semiconductor technology:

- Development of small synchrotron radiation machines for 64Mb DRAMs and up (see Table 1)
- Opening of over 30 bioelectronics R&D laboratories to develop biosensors, biochips, photopolymers, and, eventually, biocomputers (see Table 2)
- Formation of corporate R&D consortiums to develop automotive electronics, 32-bit MPUs, supercomputers, diamond substrates, space-grown crystals, and robot sensors
- Commercialization of expert systems developed through MITI's Fifth Generation Computer Project and formation of an electronic dictionary joint program
- Introduction of video RAMs, 4Mb DRAMs, 256K SRAMs, 1Mb EPROMs, 16K ECL RAMs, and 1Mb virtual SRAMs
- Aggressive push into IC cards using cell-based EPROMs and EEPROMs
- Increasing design-in of American 32-bit MPUs and a continuing Japanese push to enter the market by 1987
- Proliferation of digital signal processors (DSPs) for digital stereos, graphics terminals, televisions, and VTRs
- Spinoff of ECL gate arrays, ECL master slice arrays, and GaAs gate arrays from MITI's Supercomputer Project
- Heated competition to develop expert systems for VLSI CAD tools
- Development of 1.3- to 1.5-micron wavelength semiconductor lasers, indium phosphide crystals, and optoelectronic ICs (OEICs) for optical communication and future opto-computers
- Spinoff of ECL-compatible GaAs gate arrays, monolithic microwave ICs (MMICs), and GaAs logic ICs from MITI's Supercomputer Project
- Announcement of a potential breakthrough in Josephson junction technology
- Work on new niobium-based superconducting materials
- Introduction of steppers, direct-write electron beam equipment, and excimer lasers for sub-micron geometries

Table 1

SYNCHROTRON RADIATION (SOR) RESEARCH ACTIVITIES

Company	Activity	Start
NEC/MOE High Physics Lab	Synchrotron for 1Mb+ DRAMs (Tsukuba)	Jan. 1985
NTT/Hitachi/ Toshiba	64Mb+ DRAM synchrotron radiation (Atsugi Lab)	Fall 1987
MITI/Sumitomo Electric	10-meter industrial synchrotron radiation equipment for VLSI research	1989
Sumitomo Heavy Machinery	1-meter diameter synchrotron radiation ring for 16Mb and above	1986

Source: DATAQUEST
May 1986

Table 2

BIOELECTRONICS RESEARCH ACTIVITIES

Company	Activity	Start
Ajinomoto	Biochips, biosensors	1985
Asahi Chemical	Organic semiconductors	1984
Dojin Chemical	Langmuir-Blodgett thin films for biochips	1984
Fuji Electric	Alcohol sensors, glucose sensors (Yokosuka)	1985
Fujitsu	Biosensors, biological data processing functions	1985
Hitachi	Biochips (Tokyo Central Laboratory)	Oct. 1985
Hitachi Works	Biosensors, Langmuir-Blodgett film (Kagoshima)	Feb. 1985
Japan Suisan	Sweetness biosensors	1985
Kao	Biochips	1985
Kirin Brewery	Alcohol biosensors	1985
Kuraray	Implantable biosensors for blood pH monitoring	1984
Kyowa Hakko	Factory Automation and medical biosensors	1985
Kyowa Hakko/ Takeda Chemical	A joint venture to develop biosensors, biochips (other members include Toa Nenryo, Mitsubishi Chemical, and Toray Industries)	1986
Matsushita Elec.	Biochips (Kawasaki)	April 1986
Matsushita Elec./ Hayashibara	Water-soluble photopolymers for VLSI chips	1985
Matsushita Denki	Biosensors, water-soluable photopolymer	1985
Mitsubishi	Nerve functions, biosensors	1985
Mitsui Trading	Biochips	1985
MITI/Tokyo U.	Bioholonics computer (MITI ETL, Tsukuba)	1985
NEC	Nerve functions, biosensors (Tsukuba)	June 1987
Ricoh	Organic semiconductors	1985
Sanyo	Biosensors, biochips (Tsukuba)	Oct. 1985
Sharp	Molecule recognition, vision data processing molecular devices, biochips biocomputers	1985
Sony	Biosensors, optical magnetic storage material	1985
Suntory	Neuro-biology, central nervous systems (Senri)	1986
Tokyo Institute of Technology	Biosensor mass production technology, biosensors (Professor Toyosaka Moriizumi)	1985
Tokyo University	High-polymer membranes using organic monomers	1984
Toray	Biosensors, biochips, molecular memories	1985
Toshiba	Biosensors for measuring chemicals, biochips	1985
Toyo Brewery	Biosensors for food quality analysis machines	1985
Toyobo	Medical and protein measuring biosensors	1985

Source: DATAQUEST
May 1986

Technology Trends
1st Quarter 1986

CORPORATE R&D PROJECTS

In a recent survey, Japanese electronics companies stated that they plan to increase their R&D spending by 20 percent to 30 percent in 1986 to develop new products for the next recovery. Overall, R&D spending of major electronics companies is about 4 percent to 5 percent, up from 3 percent to 4 percent in the past. For semiconductor makers, DATAQUEST estimates that Japanese R&D spending will average about 12 percent to 15 percent of revenue in 1986. We will issue estimates of Japanese semiconductor R&D spending in the Corporate R&D section of our new binder (JSIS, Volume II, Technology and Government) later this year.

Synchrotron Radiation for Megabit DRAMs

DATAQUEST notes growing interest among Japanese companies in synchrotron radiation (SOR) technology to develop 64Mb+ DRAMs. As shown in Table 1, special efforts are being made to downsize SOR equipment in order to expand its market potential.

Bioelectronics Research Blossoms

DATAQUEST observes that more than 20 Japanese electronics companies are engaged in bioelectronics research. As shown in Table 2, the immediate focus is biosensors for medical and factory automation applications. However, biochips and logic systems mimicking nerve systems are being developed for future sixth-generation biocomputers. Unlike in Europe and the United States, where bioelectronics research is conducted primarily for academic or military reasons, Japanese research is aimed at practical commercial uses. (We plan to issue a newsletter reviewing Japanese developments in bioelectronic research.)

In March, a major bioelectronics joint venture was formed by five companies, including Kyowa Hakko, Mitsubishi Chemical, Takeda Chemical, Toa Nenryo, and Toray Industries. The companies will jointly develop biosensors, biochips, bio-pharmaceuticals, bioreactors, and bio-functional membranes. Temporarily called the Protein Engineering Research Institute, the venture is capitalized at ¥300 million ($1.7 million) and is headed by Yoshikazu Ito, president of Toray Industries. The Japan Key Technology Center, jointly owned by MITI and the Ministry of Posts and Telecommunications (MPT), will provide 70 percent of the funds, with the remaining 30 percent equally shared by the participating companies. The company plans to invest ¥30 billion ($176 million) over the next ten years in protein engineering. A ¥5 billion ($29 million) research center will be built in Senri (Osaka prefecture) by late 1987. The venture will include ten more companies. To date, Fujitsu, Kirin Brewery, Nihon DEC, and Showa Denko have already applied for capital participation.

Biocomputing is a hot area of basic research in Japan. MITI and various corporations are currently analyzing the neutral systems of the following organisms to understand simple biological logic circuits:

- NEC's Basic Research Laboratory--1.0mm flatworms
- Mitsubishi Electric's Central Research Laboratory--simple marine organisms
- MITI's Electrotechnical Laboratory--squid

Hitachi-GM Joint R&D Projects

In February, Hitachi and General Motors agreed to an extensive tie-up to pursue joint R&D and production projects in five high-technology areas: automotive parts; semiconductors and other electronics; computers; optical fibers, magnetic materials, and other new materials; and factory automation. GM also agreed to make long-term purchases of electronic control systems produced by Hitachi's Kentucky plant. The two companies will focus on developing new automobile electronics technologies. DATAQUEST notes that Hitachi also participates in a recently formed automotive electronics R&D consortium (see next section). GM also has a joint venture with Toyota, an equity interest in Isuzu Motors and Suzuki Motor, a tie-up with Nissan Motor, and has acquired Lotus (U.K.).

Mitsubishi Group Diamond Film Research Consortium

Five Mitsubishi companies, including Mitsubishi Corporation, Mitsubishi Heavy Industries, Mitsubishi Electric, Mitsubishi Chemical, and Mitsubishi Research Institute, are cooperating to develop thin diamond films in gravity-free conditions. Their goal is to synthesize high-quality diamond structures for use as IC substrates, using a chemical vapor deposition (CVD) process, without encountering heat convection effects. Initial plans call for conducting experiments aboard the U.S. space shuttle.

New Automotive Alloys Research Consortium

Under the sponsorship of Tohoku University's Engineering Department and the Metallurgy Research Association of Sendai City, 25 Japanese companies formed a new research consortium, the Next Generation New Alloys Research Association. The consortium involves eight automobile makers (including Toyota and Nissan), six semiconductor makers (Hitachi, NEC, and others), and eleven materials companies. The group will focus on four areas: amorphous alloys, shaped memory alloys, fine ceramics,

and hydrogen storage alloys. DATAQUEST contacted the MITI office in Sendai City to ascertain whether foreign companies are invited to participate, but no decision has been made yet.

Robot Sensor Joint R&D Program

The Japan Robotics Association recently formed a two-year joint industry/government/university robot sensor R&D program. During 1986, the group will investigate proximity sensors and touch sensors; during 1987, it will study standards and applications. MITI's Machinery Research Laboratory and Electrotechnical Laboratory, Toshiba, Fujitsu, and robot makers will participate in this program.

Sharp Supercomputer Research

Sharp announced that it is developing a non-von Neumann "super personal computer" that will offer word processing, communications, facsimile, and data base functions. The minisupercomputer, which will feature parallel processing architecture, is targeted for release in 1987. DATAQUEST notes that other Japanese companies (besides supercomputer leaders Fujitsu, Hitachi, and NEC) plan to announce mini-supercomputers and mainframe supercomputers in 1987.

NTT Restricts Technical Announcements

DATAQUEST has learned that Nippon Telegraph and Telephone (NTT), which runs the Atsugi Electrical Communication Laboratory (ECL) for semiconductor research, will restrict all technical announcements to the print media and has set tough guidelines for NTT research papers announced at nonacademic conferences. This new policy, adopted since NTT's privatization in April 1985, is a major development since NTT is a world leader in VLSI, fiber optic, and digital communications research. NTT spent ¥170 billion ($1 billion) on research in fiscal 1985.

GOVERNMENT R&D PROJECTS

Science and Technology White Paper

In March, the Nakasone Cabinet approved a Science and Technology Agency (STA) policy proposal to promote more joint government/industry/university cooperation in basic and creative research. The plan calls for expanding national testing laboratories, increasing R&D spending and researcher training, and improving the diffusion of technical

information. Sixteen high-technology fields will be emphasized, including aerospace, electronics, new materials, biotechnology, and health care.

In electronics, the following research targets were identified: optical devices and beams, ion beams, X-ray analysis, ceramic particles, vacuum conditions, synchrotron radiation, bio devices, and new substrates.

Tokyo University TRON Project

Fujitsu, Hitachi, and Mitsubishi are jointly developing MPU technology and operating systems under Professor Ken Sakamura of Tokyo University. In March, Hitachi announced TRON-based operating systems to be used with foreign MPUs in industrial applications. Hitachi has developed a system for Motorola's 68000, Fujitsu has a system for Intel's 80286, and NEC announced a TRON-based operating system for its V Series. TRON-based systems offer 30 percent to 40 percent faster operating speeds in controlling MPUs for robots, motorized equipment, and other industrial machinery. The TRON Project also has the goal of developing 32-bit MPUs by 1987.

Kyoto University Supercomputer Project

Kyoto University's Engineering Department and Matsushita Electric are jointly developing a 2 to 3 GIGAFLOP (billion floating point operations per second) supercomputer utilizing 300 32-bit MPUs and parallel processing architecture. The machine will be unveiled in late 1986 or early 1987. Matsushita has assigned 100 technicians and ¥4 billion ($23.5 million) to the project, which is headed by Assistant Tatsuo Nogi of Kyoto University's Engineering Department.

MITI Optoelectronics Project

MITI's Optoelectronics Project is developing manufacturing technology to evaluate GaAs crystals that will be used to produce optoelectronic ICs (OEICs) for future opto-computers. The goal is to develop defect-free GaAs crystals using epitaxial thin-film technology. MITI is lending equipment worth ¥3.5 billion ($20.6 million) at no cost to companies that are currently receiving consignment funding (itakuhi) to supplement their ¥600 million ($3.5 million) in OEIC research spending. Project participants include Fujitsu, Koga Electric, Matsushita, the Max Planck Institute, Mitsubishi, MITI's Electrotechnical Laboratory, NEC, Oki Electric, Sumitomo Metals, and Toshiba.

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MITI Fifth-Generation Computer Project

MITI's Next Generation Computer Technology Development Association (ICOT) plans to establish an Artificial Intelligence Center to develop practical AI systems. The center will focus on production equipment, printing, CAD/CAM, factory automation, and natural language processing. Members include Hitachi Seiki, Iwanami Publishing, Mitsubishi, NEC, Obunsha, Sanshodo, Sony-Tektronix, Toshiba, and Toyoda Machinery.

Eight computer makers (Fujitsu, Hitachi, Matsushita Electric, Mitsubishi Electric, NEC, Oki Electric, Sharp, and Toshiba) recently formed a joint venture company to develop a 900,000-word electronic dictionary for fifth-generation computers. Four dictionaries will be developed: 300,000 basic words, 600,000 technical terms, a conceptual structure dictionary, and a conceptual description dictionary. Hardware will include workstations and data base machines to enable fifth-generation computers to understand natural languages. The new venture, capitalized at ¥300 million ($1.7 million), was established in April and is located within the New Generation Computer Technology (ICOT) project. The seven-year project is initially budgeted at ¥20 billion ($114 million), but may be expanded to ¥33 billion ($190 million). Participating companies will invest about ¥90 million ($514,000) and the Japanese government's Basic Technology Research Promotion Center will invest about ¥205 million ($1 million).

ICOT has signed an agreement to jointly develop fifth-generation computers and exchange technical information with the Canadian Society for Fifth Generation Research (CSFGR).

DATAQUEST observes that Japanese companies are utilizing expert system and artificial intelligence technology acquired through MITI's Fifth Generation Computer Project. Recently, several companies announced the following applications as shown in Table 3.

MITI Excimer Laser Research

MITI's Electrotechnical Laboratory has developed the world's highest output for a discharge-excitation excimer laser, which generated a 520,000-kilowatt pulse. The previous record of 300,000 kW was set by the U.S. Naval Research Laboratory last year. Future applications for ultraviolet excimer lasers include ultra-large-scale integrated (ULSI) circuits, notably 64Mb DRAMs and higher.

Table 3

COMMERCIAL APPLICATIONS OF EXPERT SYSTEMS IN JAPAN

Company	Application
Mitsubishi	Personal sequential inference (PSI) machine from MITI's Project; 50 PSI computers delivered to the New Generation Computer Technology (ICOT) for evaluation; application for MITI funds to market the computers; developing expert system development tool for the PSI computer
Hitachi/Nishi-Nippon Bank	A joint project to develop a high-speed, compact expert system (an inference machine called Eureka) to assist commercial loan operations
NEC	An Automated Computer Program Generator that automates software development; a minicomputer system utilizing LISP and PROLOG for internal processing and C language for man-machine interface that transforms information input in Japanese language and graphics into a COBOL computer program
Petroleum Corporation	An expert system for excavating undersea oil wells using software (BRAINS) developed by Toyo Joho Systems
System Development Center	A medical treatment expert system (MEDI-NET) utilizing a FACOM-M150F mainframe, PROLOG-based FACOM-Alpha computer, and a nationwide telecommunications network

Source: DATAQUEST
May 1986

Satellite Development Projects

The Ministry of International Trade and Industry (MITI) and the Science and Technology Agency (STA) plan to launch unmanned experimental laboratories in the early 1990s. MITI's plan, supported by the Ministry of Education, involves launching a three-ton laboratory capsule (Free Flyer) on the U.S. space shuttle in 1992 to experiment with proteins, enzymes, and high-purity semiconductor crystal-growing processes. MITI

will allot ¥180 million ($1.0 million) to the project in fiscal 1986. The three-ton STA space lab will be launched by a Japanese rocket, assembled in space, and attached to the U.S. space station. The project was budgeted at ¥32 million ($183,000) in fiscal 1986.

On February 12, the National Space Development Agency (NASDA) launched the BS-2b broadcasting satellite, which will offer two channels. The Japan Broadcasting Company (NHK) may offer pulse code modulation (PCM) audio broadcasting, with future plans for high-definition television and facsimile broadcasting.

The Space Development Corporation, a government corporation, has selected Mitsubishi, NEC, and Toshiba to jointly develop the ETS-VI, its sixth experimental communications satellite. The satellite will weigh two tons and enable satellite-to-satellite communications and communications with moving objects. With a projected budget of ¥40 billion ($230 million), the ETS-VI will be the first satellite using only Japanese technology.

NEW PRODUCTS AND TECHNOLOGY TRENDS

Memory

- Fujitsu--A CMOS 256K SRAM (MB84256); 100/150ns access times; 6.0 x 9.76mm chip; 32K x 8-bit organization; 5.5mW power consumption at standby (standard) or 1.1mW at standby (low-power type); four asynchronous models; sampling at ¥9,800 ($57.65) in lots of 100

  - Three CMOS 1Mb EPROMs; MBM27C1024 with 64K x 16-bit structure, 200/250ns access time, and 40-pin DIP; MBM27C1000/1001 with 128K x 8-bit structure, 200/250ns access times, and 32-pin DIP; MBM27C1028 with 64K x 16-bit/128K x 8-bit, 150/200/250ns access times, and 28-pin DIP or 32-pin LCC; four minutes to write in 1Mb of data; 160mW power dissipation during operation (5 MHz); 550-mW standby power; sampling at ¥12,000 ($70.60)

  - Three 64K ECL RAMs (MBM10490/100490/101490); 1.0-micron design rule; 15/25ns access times; 64K x 1-bit structure integrating 270,000 transistors on a 4.46 x 8.6mm chip; 1.56 watt power consumption for 15ns model and 1.04 watts for 25ns model; I/O compatible with 10K/1000K series; sampling at ¥15,000 ($88.23)

- Two CMOS 64K EEPROMs (MBM28C64/65); 8-bit structure with built-in ECC circuit; 250/350ns access times; sampling at ¥4,000 ($23.53)

- Two low-power 256K PROMs; open collector output chip (MB7111L); a three-state output model (MB7112L); 40mA power consumption; 2.4mA current supply capacity; 35ns; four packages (16-pin ceramic DIP, 16-pin plastic DIP, 20-pad LCC, and 16-pin FPT); 1.8 x 2.5mm chip size; 16 x 12-micron memory cell area; 32K x 8-bit structure

- Two 4K PROMs with power register function; MB7226RA-20L priced at ¥2,000 ($11.76); MB7226RA-25LW priced at ¥3,800 ($22.35)

• Hitachi--A 64K EEPROM (HN58C65) that allows rewriting 8 Kbytes of program in 2.5 seconds; 200ns access time; 20mW power dissipation during operation and 5mW at standby; sampling at ¥4,000 ($23.52 single) and ¥2,500 ($14.70 lots of 1,000) for DIP types; ¥4,500 ($26.47) for small outline package types

- Two CMOS 256K multiport video RAMs featuring built-in serial access memory and shift register; random port linked to RAM and serial port linked to serial access memory (SAM); simultaneous data transfer to CRT and display data rewrite coming from computer; 2.0-micron design rule; 100ns access time for RAM and 40ns minimum cycle time for SAM; 64K x 4-bit RAM structure and 256-word x 4-bit SAM structure; HM53461 priced at ¥1,400 ($8.24) or ¥850 ($5) in lots of 1,000; HM53462 for ¥1,500 ($8.82) or ¥900 ($5.30), respectively

- A CMOS 1Mb pseudo-SRAM (HM658128P/LP); DRAM memory cell and SRAM-like peripheral circuits; 128K x 8-bit structure; sampling from April

- Two CMOS 16K SRAMs; 1.3-micron design rule; 4K x 4-bit structure; 90mA power consumption during operation and 2mA standby; 25ns device (HM6268P) priced at ¥3,000 ($17.64) or ¥2,000 ($11.76) for 1,000-unit lots; 35ns device priced at ¥2,100 ($12.35) and ¥1,400 ($8.24), respectively

- A 1Mb EPROM; 1.2-micron rule; 19.27 square micron memory cell; 26.4 square micron chip; 10 microsecond write-in time; lightly doped drain (LDD) structure

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- Matsushita--A 1Mb video DRAM (MN4700) with 25ns access time and 30ns cycle time; one television field stored on two chips; pipeline method and simple repeat circuit; 256K x 4-bit structure; double-layer polysilicon and double-layer aluminum interconnect; 1.2-micron design rule; 5.88 x 11.20mm chip with 2.2 million elements; 40-pin DIP; 5V power supply; sampling in May at ¥20,000 ($117.65)

- Mitsubishi--Two CMOS 256K SRAMs; M5M5256P with a 1.3-micron rule, 32K x 8-bit structure, and three access times (100/120/150ns) priced at ¥13,000/¥11,000/¥10,000 ($76.47/$64.70/$58.82), respectively; M5M5256P-L low-power consumption model priced at ¥14,000/¥12,000/¥11,000 ($82.35/$70.59/$64.70), respectively

  - Two CMOS 64K SRAMs; 64K x 1-bit and 16K x 4-bit organization; ¥8,000 ($47.06) for 45ns type; ¥7,500 ($44.12) for 55ns type

  - A CMOS 1Mb mask ROM (M5M23C100P), 165mW power dissipation during operation and 550mW at standby; 250ns access time; 1.5-micron design rule; 18-pin DIP; sampling at ¥2,500 ($14.70)

  - A prototype 4Mb DRAM expected by late 1986; sampling from 1988

  - A CMOS 256K video RAM with built-in high-speed I/O functions (M5M4C264); 64K x 4-bit structure; RAM and SAM connected by 1,024 bi-directional bus lines, allowing the SAM to store output data from the RAM at 25 MHz; sampling at ¥1,500 ($8.82)

- NEC--Two high-speed NMOS 256K line memories capable of processing video signals for television sets and VTRs in horizontal scanning line units; complete asynchronous read/write features; three-transistor memory cell; NTSC type with 34ns read/write cycle time (uPD41101C); 28ns for PAL type (uPD41102C); sampling at ¥4,000 ($23.53) since February

  - An NMOS 4Mb DRAM prototype; 95ns access time; 0.8-micron design rule; 9.2 million elements on a 6.2 x 16.0mm chip; an improved trench configuration; transistor and storage electrodes connected within the trench capacitor; high-purity substrate; 0.8-micron diameter, 5.0-micron deep trench capacitor; 2.3 x 4.6-micron memory cell; 8.8 square microns per cell; three-layer wiring of the two-layered polycide and one-layer aluminum wiring and new memory cell structure (buried storage electrode cell); 425mW power consumption; 18-pin DIP; commercialization two to three years away

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- A CMOS 1Mb EPROM (MuPD27C1000D); 0.1mm minimum write-in pulse width allowing user to write in memory in 30 seconds; 64K x 16-bit organization; 500mW standby power; 150mW power dissipation during 5 MHz operation; sampling from March 1986

- A CMOS 256K SRAM with 25ns access time; 1.3-micron gate length; high-performance polyside gate electrode transistors and low-resistance aluminum double layer interconnect technology; 4.7 x 13.37mm chip size; 262,144 word x 1-bit organization; 300 mil, 24-pin DIP; 70mA power dissipation during operation and 2mA at standby; sampling later this year

- A 16K ECL RAM with 4ns access time; 4K x 4-bit structure; 1.25-micron design rule; 120,000 elements on a 5.5 x 4.9mm chip; compatible with ECL-100K Series; 1.6 watt power consumption; 28-pin 400-mil LCC

- A new memory cell technique using an epi-wafer containing boron; 0.8-micron trench method for reducing cell size by half; for use in 4Mb DRAMs and above

- NMB Semiconductor--CMOS 1Mb DRAM sampling; 1.2-micron rule; 1Mb x 1-bit and 256K x 4-bit structures; 10ns read time

- Sharp--A CMOS 64K and 128K EPROM; 256K EPROM expected soon

- Sony--A CMOS 256K SRAM; 30ns access time; NMOS memory cells and CMOS peripherals; 1.4-micron design rule; 50mA power consumption during operation and 2mA at standby; 1.6 million elements on a 6.07 x 10.6mm chip; 10mW power dissipation at 1 MHz during operation and 500 nanowatts at standby; 260,000 memory cells, each with six transistors; sampling from April and mass production from December

  - Two high-speed digital video signal processing memories for television sets and VTRs; CXK1201P with 66/33ns write/read cycle time, 8 x 910 x 2-bit structure, 30 MHz maximum operating frequency, and 28-pin DIP; CXK1202S with 25/25ns write/read cycle time, 1,136 x 8-bit structure; 200mW power consumption, 40 MHz maximum operation frequency, and 28-pin, shrink DIP; sampling at ¥3,000 ($17.65) since February

- Three masked ROM sets for use as Chinese character generators; four NMOS 1.2Mb ROMs that form 7,000 characters on a 24 x 24-dot matrix; 250ns access time; 40-pin ceramic DIP; four-chip set priced at ¥20,000 ($117.65); six 1Mb ROMs for 24 x 24-dot and 16 x 16-dot matrix; 350ns access time; 28-pin ceramic DIL; six-chip set priced at ¥50,000 ($294.12)

- Two high-speed video memories for processing VTR and television digital signals (CXK1201P); non-interlace scanning performed after doubling the horizontal scanning frequency; 1H delay line used for noise reduction, digital filter, time axis compressor, expander, and dropout compensator for VTRs; sampling at ¥3,000 ($17.14)

- Toshiba--A 1Mb virtual SRAM with memory cells structured like a DRAM; built-in refresh circuits; 128K x 8-bit structure; 5.99 x 13.8mm chip size; 3.5 x 8.4-micron cell size; 1.0-micron design rule; twin-well CMOS process, using double layer polysilicon and aluminum interconnect wires; 16mA power consumption during operation and 20mA at standby; 32-pin, 600-mil dual inline

  - Two CMOS 4Mb DRAM prototypes; 4Mb x 1-bit and 1Mb x 4-bit organizations; 8.7 million elements on a 7.84 x 17.48mm chip; 3.0 x 5.8-micron memory cell size; 80ns; trench method; 1.0-micron design rule; 40/80ns access times; 300mW power consumption in operation and 2.5mW in standby; 1.0-micron design rule; commercialization two to three years away

  - Three NMOS 72K SRAMs (TMM2089C); 25/35/45ns access times; 8K x 9-bit structure; 1.5-micron process; shared word line that allows selective operation of memory cell array divided into four segments by a line address decoder and "activated decoder"; 743mW power dissipation during operation and 82.5mW at standby; sampling at ¥12,000 ($70.60) for 25ns device; ¥11,000 ($63.86) for 35ns; ¥10,000 ($57.14) for 45ns device

  - A floating gate method that reduces EPROM memory cell area 40 percent; 1.0-micron gate length; 80 microsecond write-in time

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Application-Specific Memory (ASM)

DATAQUEST observes that Japanese companies are preparing for a "video war" with South Korea and a domestic "IC card battle" in the early 1990s. Research efforts are heating up, with major makers developing video RAMs and line memories, and inserting their EPROMs, EEPROMs, MPUs, and MCUs into standard cell libraries. Special attention is being paid to developing 16K and 64K EEPROM capabilities for IC cards. We will issue special newsletters on the emerging video RAM and IC card developments this summer.

- Dai Nippon Printing--A contract to supply Siemens with 100,000 IC cards incorporating 64K EEPROM; Siemens experimenting with electronic medical records from May, covering height, weight, blood type, blood pressure, and past illnesses; priced at ¥17,000 ($100)

- Hitachi Maxell--An ML series memory IC card; 8K/16K/32K memory types with CMOS SRAMs; 3.5mm thick; 3-year lithium battery

- Japan LSI Card--A plastic molded 256K RAM disk card; 103 x 54 x 3.8mm; 32 grams; 500 Kbps access speed; ¥10,000 ($58.82)

- NEC--A 64K EEPROM for use in IC cards; others planning similar devices include Hitachi, Mitsubishi, and Oki Electric

- Ministry of International Trade and Industry (MITI)--An IC card standards committee report covering future uses, markets, materials, terminals, switching protocols, data formatting, and JIS and ISO standards

- Nippon Printing--An 3.5mm thick IC card (Nissha Card)

- Nippon Telegraph & Telephone (NTT)--An IC card experiment with 19 financial institutions near Yokohama Station, including 7 city banks, 2 regional banks, 2 long-term credit banks, 1 trading company, 5 trust banks, and 2 credit associations

- Omron Tateishi--An automatic teller machine (ATM) that handles IC cards

- Toshiba--An automatic IC card teller machine that can also be used for magnetic cards

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Microprocessors/Microcontrollers

Nikkei Datapro recently conducted a survey on 32-bit MPU applications and reported the following usage among 364 companies: Motorola's MC68020 (used by 42.5 percent of the companies surveyed), Intel's 80386 (21.2 percent), National's 32032 (2.4 percent), and NEC's V70 (1.6 percent). There was no interest in NEC's V60, National's 32332, or Tokyo University's TRON chip. Among the most popular applications:

- Image processing--24.4 percent
- Engineering workstations--18.7 percent
- Robots/NC devices--16.3 percent
- Process controls--8.9 percent
- Measuring instruments--8.1 percent
- Office computers--4.9 percent
- Communications controls--4.1 percent
- Personal computers--2.4 percent
- Medical equipment--2.4 percent
- Super microcomputers--1.6 percent
- Minicomputers--1.6 percent
- Artificial intelligence workstations--0.8 percent
- Peripherals--0.8 percent
- Voice synthesizers--0.8 percent

The following are major new products announced during the first quarter of 1986:

- Fujitsu--Two CMOS 4-bit single-chip MCUs; 256 x 4-bit RAM capacity, 68 I/O ports, 5-bit A/D converter, and 9-bit programmable pulse generator; MB88P551 priced at ¥2,500 ($14.70); 8K x 8-bit ROM capacity; MB88P551 with 8K x 8-bit ROM capacity; MB88P552 with 6K x 8-bit ROM

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- Hitachi/Motorola--A jointly developed CMOS version of Motorola's 68000 MPU (Hitachi HD68MC000/Motorola HC68HC000); 100mW power consumption during operation and 200mW at peak (12.5 MHz); 8/10/12.5 MHz versions; ceramic 68-pin grid array or 64-pin DIL packages

- Matsushita--A CMOS 32-bit MPU with 6 MIPS capability, making it five times as powerful as the 68020; 1.0-micron design rule; 400,000 elements; 25 MHz clock frequency; sampling from fall 1986

- Mitsubishi--A CMOS 16-bit, single-chip MPU; 2-micron rule; 130,000 elements; 500ns command execution time; three-stage pipelining technique; 16 Mbytes of address space; eleven 16-bit registers; 8 Kbytes of built-in ROM; 512 bytes of RAM; 72 basic instructions; 64 I/O ports

- NEC--A proprietary 32-bit MPU (V60 Series) that employs C as its high-level language and a UNIX operating system; CP/M and MS-DOS programs from V20 to V50 Series usable with an emulation mode; 32-bit internal and 16-bit external CMOS MPU; 3.5 MIPs; 16 MHz clock speed; memory management unit, floating-point arithmetic function, six-stage pipeline structure, automatic debugging, and 4 Gbytes of address space; 1.5-micron design rule, two-layer aluminum CMOS process; 375,000 transistors on a 13.9 x 13.8mm chip; sampling at ¥100,000 ($588.23); monthly production of 10,000 units from August; second sourcing likely with Zilog, Sony, and Sharp; a 32/32-bit processor (V70) expected in 1987

  - A peripheral device (MuPD4990C) with a 500 KHz maximum clock input frequency for use in facsimiles, word processors, and computers; priced at ¥400 ($2.35) in lots of 10,000

  - Two 4-bit, single-chip MCUs with built-in controller/drivers for fluorescent display tubes; type with 6 Kbytes of mask ROM priced at ¥1,200 ($7.06); piggy-back type with EPROM priced at ¥15,000 ($88.24)

  - A CMOS 8-bit, single-chip MPU (uP78312); 16-bit internal data processing capabilities; 16 x 16-bit multiplication in 3.2 seconds; 32 x 16-bit multiplication in 8.2 seconds; a successive approximation 8-bit A/D converter; 2-micron process; 8 Kbytes of built-in ROM; 256 Kbytes of built-in RAM; 64 Kbytes of address space; 48 I/O ports; 64-pin shrink DIP, quad, and quad-in-line packages; priced at ¥2,000 ($11.76)

- A CMOS single-chip controller (uPD72015) for Omninet (low-price LAN from Corvus Systems); sampling at ¥20,000 ($117.65) from mid-1986

- NEC/Boeing--A single-chip controller LSI for Boeing's Digital Autonomous Terminal Access Communication (DATAC) System; 1-Mbs data transmission speed; 35mm square CMOS device with more than 10,000 gates

- Oki Electric--A CMOS 8085A-type 8-bit MPU (MSM80C85A-2) produced under an Intel license; 5.0-MHz operation speed; 20mA power dissipation; 40-pin plastic DIN or 44-pin plastic flat package; priced at ¥1,500 ($8.82)

- Rohm--Two flexible disk controllers; IC for read/write functions (BA6580K); drive logic controller (BU9500K); 5V power supply; 750mW power dissipation; commercial device within one year

- Sanyo Electric--A single-chip controller for LCD panels with 640 x 256 dots (LC7980); 10 Mbs data transmission rate; direct interface possible with Intel's 80 family and Motorola's 68 family; LC7980 with 512K dot display capacity; priced at ¥1,500 ($8.82); LC7981 for use with 640 x 128-dot LCD panels; priced at ¥1,000 ($5.88)

  - A CMOS digital servo control MCU (LC7990) for hard disk drive spindle motors; 11-bit resolution speed comparison clock and 1MHz or 2MHz clock signal; 1.5mA current consumption; 22-pin DIP; sampling at ¥700 ($4.11)

Digital Signal Processors (DSPs)

- Fujitsu--A CMOS digital stereo tuning 4-bit MPU (MB88561) incorporating a PLL synthesizer, A/D converter, prescaler, and LCD driver; built-in 192 x 4-bit RAM and 3 Kbytes ROM; 80-pin flat package; priced at ¥980 ($5.76)

- Hitachi--Graphics signal processors; a compression/expansion chip for document images (HD63085Y) that compresses data to one-tenth to one-thirtieth of initial volume; 2-micron CMOS, two-layer aluminum wiring process; 8.3 x 8.2mm chip housed in a 72-pin grid array; a graphics processing chip (HD63084) to eliminate distortion and convert CCD sensor signals to digital form; 5,000 pixels per second; CMOS process; 8-MHz internal processing speed; sampling at ¥7,000 ($41.18)

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- Matsushita--A real-time image signal processor (RISP) with a 20ns instruction execution time; proprietary bipolar Vertically Isolated Self-Aligned Transistor (VIST) technology; 45,000 elements, including RAM memories and four arithmetic functions; 50 million computations per second, including edge detection, noise reduction, contrast emphasis, monochrome graphics, thickening and narrowing lines, and matching patterns; 7.0 x 7.1mm chip size; 5 x 5 picture element register; for use in robots, computer tomographic systems, and OA systems; priced at ¥200,000 to ¥500,000 ($1,176 to $2,941)

- Mitsubishi--A CMOS digital signal processor for improving television picture quality; 100mW power consumption; 40ns cycle time; 88,000 transistors; 2-micron, double-poly CMOS

  - Three color television signal processors; M51346AP for image and voice intermediate frequencies sampling at ¥400 ($2.35); M51308SP for PAL image, color, and deflection signal processing for ¥800 ($4.70); M51309SP for PAL/NTSC/SECAM image, color and deflection signal processing for ¥800 ($4.70); 18-pin package

  - Two hi-fi VCR audio signal processors; a noise reduction IC (M12652P) in a 48-pin dual inline package sampling at ¥800 ($4.70); a frequency modulation/demodulation IC (M51653P) in a 52-pin shrink DIP sampling for ¥1,050 ($6.18)

- NEC--A 32-bit floating-point signal processor (uPD77230) with 6.7 MFLOPS arithmetic capacity; 1.5-micron rule; aluminum double-layered CMOS process; 7.8 x 14.2mm chip size; three-stage instruction; 150ns instruction execution; 2K x 32-bit instruction ROM; 1K x 32-bit data ROM; two-set structured 512 x 32-bit RAM for fast Fourier transformation; sampling at ¥80,000 ($470.60)

  - A real-time clock (uPD4990C) for use in office automation equipment; 10-/30-/60-second interrupt function; sampling for ¥400 ($2.35)

- NEC/Oki Electric--A jointly developed CMOS signal processor (NEC uPD77C20/Oki MSM77C20); NMOS compatible; power consumption reduced by 80 percent; monthly production of 50,000 to 100,000 units

- Oki Electric--A CMOS digital signal processor (MSM6992) with built-in floating-point arithmetic function; 100ns machine cycle; arithmetic power equal to 10 MFLOPS; 2.0-micron design rule; minimum 400mW power dissipation; built-in 1K x 32-bit ROM and 128K x 22-bit x dual-side data RAM; sampling at ¥60,000 ($353)

- Sony/Toshiba--Two jointly developed CD graphics processors; an image synchronized signal generator with 2,000 transistors; a picture element processor with 13,000 circuits; low-power CMOS process

- Tokyo Sanyo--Fifteen VHS VTR image signal processors; four head amplifier ICs; seven brightness signal processors; four color signal processors

- Toshiba--A 32-bit image processor; 50ns operating time; 1.2-micron design rule; CMOS 2-layer aluminum wiring; 170,000 elements on 13.5 x 13.5mm chip; for use in remote sensing, computer tomographics, magnetic resonance imaging, CAD, and medical equipment systems; 20-MHz frequency;

  - Six signal processors for VHS VCR compatible with HQ mode; sampling at ¥2,000 ($11.76)

Application-Specific ICs (ASICs)

- Fujitsu--A 1,520-gate high-electron mobility transistor (HEMT) gate array prototype; 8-bit multiplier with 3.1ns speed at minus 196 degrees centigrade; 1,520 gates arranged in 76 x 20 rows and 72 I/O cells; basic cells of four transistors measuring 132 x 54 microns; plans to develop 3,000-gate array and 16K memory by 1988

  - An ECL gate array incorporating 16K RAM with 2.8ns access time; 1.0-micron design rule; 9.4 x 9.5mm chip with 120,000 elements; 1,248 gates, including 1,120 gates for internal circuit and 128 gates for output circuits; 280ps delay time per gate; RAM organized into four 256-word x 16-bit blocks; 2.8ns data readout time; 4.4 watt power consumption; 64 chips for use in central processing unit of FACOM M-780 ultra-large-scale mainframe from spring 1987

  - Two ECL gate arrays; 3,000 gates (MB125000); 4,500 gates (MB128000); 220ps gate delay time; 500ps standard load; 1.0-micron design rule; oxide film isolation; ECL 10-KHz and TTL-level I/O signal levels; development cost of ¥6.5 million ($38,235) and 1,000-unit price of ¥30,000 ($176) for the MB125000; ¥9.0 million ($52,940) and ¥45,000 ($265) for the MB128000; eight-week turnaround time

  - A 350-gate TTL gate array (MB102000) with built-in circuit for large-current drivers; 48mA driving capacity; development cost of ¥1.5 million ($8,234) and unit prices of ¥650 ($3.82) in 1,000-unit lots

- Hitachi--Two CMOS gate arrays with built-in automatic diagnostic functions (HG62B Series); diagnostic time shortened by 30: 1.8ns gate delay time; 4,032-gate array (HG62B40) priced at ¥2,300 ($13.53); 7,136-gate device (HG62B71) for ¥13,000 ($76.47); 12,000-gate device being developed

- Mitsubishi--An ECL master slice gate array with 17,800 gates; 1.5-micron design rule; three-layer aluminum bipolar process; 39,936 transistors and 53,248 polysilicon resistors on a 11.90 x 11.96mm chip

- NEC--A 3,000-gate GaAs array; developed with MITI's Super-computer Project; 7.5 x 7.4mm chip; basic cell of seven FETs and one diode; 56ps gate delay time, or 186ps with 2mm wiring load; power dissipation one-third of silicon gate arrays; 1.4-micron gate length; 2-micron interconnect wiring of titanium, gold, and white gold; 1.2-GHz maximum toggle frequency; propriety Side Wall Assist Self-Align (SWAT) process; buffered FET logic (BFL) using depression-type FETs for the basic circuits; 26,000 elements; 4.6mW gate power consumption

  - Two ECL gate arrays; 1.4-micron emitter width; 0.7ns gate delay time; 4,000-gate device (uPB6340) of 156 input and 72 output terminals; 5,000-gate device (uPB6350) of 172 input and 80 output terminals; 0.43ns input and 1.32ns output buffer delays; I/O compatible with ECL-100K/ ECL-10KH/TTL; 132-pin and 208-pin grid arrays; 4,000-gate development cost of ¥9.0 million ($52,941) and unit cost of ¥40,000 ($235.29); 5,000-gate costs of ¥10.5 million ($62,765) and ¥50,000 ($294.12), respectively

  - A standard cell library using 1.5-micron CMOS process; 1.4ns internal gate delays; up to 17,000 gates, with plans for 25,000 gates; 256 maximum I/O terminals; 30ns access times for on-chip ROM and 20ns for RAM; development fee for 3,000 gates of ¥10 million ($58,820); price per chip of ¥800 ($4.70); logic simulation and sample shipment from 70 to 105 days

- Oki Electric--A 1.5-micron gate array series (MSM70V000), with arrays ranging from 700 to 10,008 gates; 66 to 172 I/Os; CMOS and TTL compatible; 1.2ns gate delays; clock rates up to 100 MHz; dual-layer metal HCMOS process; 38 macro blocks and 110 functional logic blocks

- Toshiba--CMOS standard cells (TC22SC Series) incorporating 4K RAMs and 16K ROMs; compatible with TC17G Series ultra-high-speed gate arrays; 1.5ns delay times; library of 200 cells and 20 types of master chips from 470 to 10,000 gates; 13 to 18 week turnaround time

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CAD Systems

- Matsushita--An automatic design system for standard cell layout called STELLA (Standard Layout Design Automation System); layout process reduced to one-tenth time of conventional system

- NEC/Anritsu--An in-circuit emulator for the NEC V40/V50 16-bit MPUs; priced at ¥2.4 to ¥2.8 million ($14,118 to $16,470); development under way on an emulator for the 32-bit V60 MPU

  - A VLSI CAD development division within the VLSI Devices Division

- Oki Electric--A portable development system (Ease 51 Mark-II) supporting the 80C51/80C52/80C59; runs either CP/M-80 or PC-DOS on a personal computer; priced at ¥11.8 million ($69,412); Symbolic Debugger, Linker, and macro assembler software for ¥104,500 ($614)

Optoelectronics

- Hitachi--An optoelectronic IC (OEIC) incorporating laser diodes, light wave paths, and optical switch; 1.6 x 1.0mm chip featuring X-shaped wave paths; InGaAs and phosphor used for laser and switch; optical switching speed of 20ns using a current of 15mA; distributed feedback lasers for long distance optical communications; for development of optical exchanges and optical computers

- Hitachi Cable--A high-power linear LED array (LLA) with three to four times higher glow power; for optical printers

- Kyoto Semiconductor--A GaAs double heterostructure LED offering 23.6 percent light-emitting efficiency at 190nm wavelength; high-frequency response at 10-MHz cutoff frequency; 660/750/830/890nm wavelengths; priced from ¥75 to ¥600 ($0.44 to $3.52)

- Kyoto University--An optoelectronic IC (OEIC) developed by Professor Akio Sasaki that combines phototransistors and LEDs in a single structure; thin layers of InP and InGaAsP stacked alternately on an InP substrate to form the four-layer LED; phototransistor built onto LED base by superimposing three layers of InP-type film; for use as a relay for no-noise high-speed signal processing and optical telephone exchanges

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- Matsushita--A laser noise carrier GaAs IC (MEL5005) with 280mW output for use in optical disk systems, CD-ROMs, and communications; 0.87-micron wavelength; 4-pin plastic package; MOCVD production process; sampling from March at ¥500 ($2.94)

- Mitsubishi--A 1.55-micron laser diode that doubles repeaterless transmission distance in optical fibers to 100km; P-type indium phosphor substrate and crescent-shape active layer; 10mA low threshold current; operable up to 115 degrees centigrade; other companies with 1.55-micron lasers include Fujitsu, Hitachi, and NEC

- MITI Optoelectronics Project--A liquid phase Czochralski method that reduces production costs of single crystal indium phosphide (InP) by 90 percent; for the development of optoelectronic ICs

- MITI Electrotechnical Lab--A new optical phenomenon that can be used to develop optical isolators and optoelectronic ICs; propagation of light through a crystal sheet a few microns thick, doped with bismuth; conversion of transverse electromagnetic waves into longitudinal form to prevent light scattering; 100 percent wave-form conversion efficiency

- NEC--A 1.5-micron laser diode (NPL5050A) for optical fiber communications; double channel planar buried heterostructure device with built-in spherical lens for single-mode optical fibers; 30mW peak output; priced at ¥500,000 ($2,941)

  - An optoelectronic IC capable of sending 1.2 Gbs of data through ultra-high-speed long wavelength band fiber optic transmission systems; 1.3-micron transmitting laser integrating three lasers; photodiode and three transistors incorporated into receiver part; indium phosphide (InP) structure; samples in three to four years

  - An AlGaInP semiconductor laser with 689.7nm band continuous visible light output at room temperature; 35mA oscillation threshold current; developed using an improved MOCVD crystal growth method

  - A three-way InGaAs avalanche photodiode (NDL5500); 80 percent signal conversion; a unique selective transversal spreading guardlink architecture; gas-phase one-time growth method; 90V reverse breakdown voltage; priced at ¥350,000 ($2,058)

- A single-chip indium-phosphor optoelectronic IC that allows 12km repeaterless transmission at 1.2 Gbps; 1.3-micron band laser diode, three bipolar transistors, and laser in the transmitter device; a PIN photodiode and three FETs in the receiver device; mass production within three years

- Optoelectronics Research Lab (MITI)--A new technology to produce indium phosphide (InP) single crystal wafers at one-tenth conventional methods

- Sharp--A semiconductor laser (LT090) with 100mW maximum light output; proprietary V-channeled substrate inner stripe (VSIS) structure; a monitor photodiode housed in a high-precision, hermetically sealed package; sampling at ¥200,000 ($1,176)

- Sony--A light-receiving module for infrared remote control systems; receiver amplifier IC and photo diode; 5V power supply; 40-KHz frequency; sampling at ¥500 to ¥575 ($2.91 to $3.38)

- Tokyo Institute of Technology--An optoelectronic device that transmits signals 800 times faster than existing systems; laser diode and optical switching combined onto a single optoelectronic IC; theoretical light switching speed of lps; superlattice structure of different molecular layers to form a multiquantum well structure; 1.5-micron wavelength laser beams emitted; 600-micron length; for use in switching, multiplexing, and signal processing of future opto-computers

- Tokyo University--A prototype optical computer system using ten lenses and optoelectronic devices; data input at three intermediate points and directed using lenses; team headed by Kazuo Hotate of the Interdisciplinary Research Institute

- Tokyo University of Agriculture and Technology--Large single crystals of up to 55 grams created from organic substances for development of future optoelectronic ICs; solvent evaporation technique in which air is passed over an acetone solvent containing dissolved chloronitrobenzene to form huge single crystals in 190 hours; team headed by Assistant Professor Masakuni Matsuoka

- Toshiba--A semiconductor laser for five-wavelength optical transmission system; 0.8- to 1.5-micron wavelength; 1.5-micron pitch; 0.7-micron depth; 0.3-micron structure

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Image Sensors

- Hitachi--A MOS image pickup device employing a horizontal readout (HE98241); 294,000 picture elements (600 x 490); 1.5-micron line width; sensitivity three times and resolution 17 percent greater than conventional MOS devices; vertical smear radically reduced; single 5V power supply; sampling at ¥25,000 ($147)

- NEC--A CCD image sensor incorporating 1.24 million picture elements; 1,280 x 970-element organization, with 960 television line resolution; 12.7 x 9.5mm image pick-up size; 9.9 x 9.8-micron picture element size; 14.5 x 12.0mm chip size; improved LOCOS element isolation method and vertical overflow drain technology to enhance sensitivity and reduce blooming and smear phenomena; 48.2-MHz rapid picture scanning speed; 48dB signal/noise ratio

Gallium Arsenide

- Fujitsu--A 1,520-gate high electron mobility transistor (HEMT) array (see ASIC section for details)

- Matsushita--A 1.6-Gbs GaAs IC for optical communication, using the E-type FET approach; 0.5 watts power dissipation; 1-micron design rule for gate lengths; single 5V power supply; white gold, titanium, and gold combination used for gate; three types of commercial devices--multiplexer, demultiplexer, and recognition system "discriminator"; multiplexer with 378 elements, 1.3 x 1.9mm chip size, and priced at ¥300,000 ($1,765); dumultiplexer with 495 elements, 0.9 x 1.15mm chip size, and priced at ¥100,000 ($588); discrimination recognition system with 96 elements; 0.9 x 1.15mm chip size, and priced at ¥100,000 ($588)

  - A single-chip GaAs noise canceller (MEL5005) using GaAs for the high-frequency oscillation circuit; to reduce noise generated by laser diodes in CD-ROMs and optical file systems; sampling at ¥500 ($2.94)

  - A GaAs wideband, double-balanced mixer IC; 50- to 2,000-MHz zone; signal output five times higher than diode types; nearly zero conversion loss; sampling at ¥300 ($1.76); monthly production of 50,000 units since April

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- Mitsubishi--Three monolithic microwave ICs (MMICs) designed as a medium frequency amplifier for direct broadcast satellites and television receiver only (TVRO); MFG7002 for 0.9 to 1.6 GHz, with a noise index of 2.5dB and a 17dB gain factor; sampling at ¥820 ($4.82); MGF7003 for 0.2 to 1.8 GHz, with 2.5dB noise and 9dB gain, ¥700 ($4.11); MGF7004 for 0.2 to 1.8 GHz, with 3dB noise and 9dB gain, ¥500 ($2.94)

- NEC--Three ECL-compatible GaAs logic ICs; 0.8 to 1.8-volt input/output levels; 5.2-volt power supply; a master/slave D-type flip-flop (MuPG700), a master/slave T-type flip-flop (MuPG701), and three-input, OR/NOR gates (MuPG702); 2-GHz clock frequency; 130ps pulse rise and 120ps decline times; features include 0.8-micron gates, gate electrode of tungsten silicide, GaAs MESFET basic cell, air-bridge interconnect, hermetically sealed 16-pin ceramic package; sampling at ¥48,000 ($282); six more GaAs standard logic ICs by summer 1986

  - A 3,000-gate GaAs array (see ASIC section for details)

- Oki Electric--A technique to layer GaAs circuits on silicon substrates; a dual-stage temperature method used during the MOCVD process that forms an amorphous layer; plans to make power FETs with 1-micron gate lengths

- Sharp--A 1GHz GaAs MESET (LT300) with build-in protection diode; 20dB gain; 14dB noise index; 0.52 x 0.54mm chip in a 2.9 x 1.5 x 1.1mm mini-mold package for automatic mounting machines; sampling at ¥125 ($.73)

- Mitsubishi Metals--Mass production LEC technology for GaAs wafers; from GaAs Perfect Crystal Project headed by Professor Junichi Nishizawa of Tohoku University; arsenide pressure controlled pulling method; 2-inch and 3-inch wafers with under 2,000 defects per square centimeter; for LED, laser diodes, and other optical devices; goal of 1,000 2-inch wafers per month

Josephson Junctions

- Hitachi--A 4-bit x 4-bit multiplier based on a niobium Josephson junction device; 210ps; niobium for upper and lower electrodes; lead for lower electrode; aluminum oxide in barrier layer; 270 elements; 3mW power dissipation; 16 x 16mm chip size; operation up to 11.9 GHz; 1.5-square micron surface; 109 circuits; goal of 3,000-gate, 10ps commercial device by 1988

- MITI Electrotechnical Laboratory--Two sequence circuits for Josephson junction devices; a shift register and a counter that act as a command post in the central processing unit; capable of handling 4 bits of data at a time, with plans for expanding to 8-bits or 16-bits; size reduction one-thirtieth of IBM's design; potential breakthrough for development of practical Josephson junction devices

Standard Logic

- Fujitsu--An ECL gate array incorporating 16K RAM (see ASIC section for details)

- Nippon Precision Circuits--A project to develop ultra-high-speed CMOS logic with a maximum clock frequency over 100 MHz, using molybdenum gate technology developed with Micro Power Systems; ECL speeds achieved with 2.0- to 2.5-micron design rule; plans to develop 1.5-micron design rule

Bipolar Logic

- Mitsubishi--A 17,800-gate ECL masterslice chip; 11.90 x 11.96mm chip incorporating 39,936 transistors and 53,248 polysilicon resistors; 1.5-micron triple aluminum layer process; a prototype 32-bit multiplier equivalent to 10,700 gates; basic cells of three transistors and four resistors

- Toshiba--A bipolar MOSFET (MG25N2CS1) with 1,000V dielectric strength; 25A rated amperage; sampling at ¥15,000 ($88.24); also MG50H2CS1 with 500V dielectric strength sampling at ¥12,000 ($70.59); 1.5-microsecond switching speed; 5V power source

- Tokyo Institute of Technology--A high-speed bipolar transistor with GaAs performance; a heterobonded bipolar transistor (HBT) in which amorphous silicon carbide and two layers of silicon crystal are layered vertically to form the emitter layer; for use in supercomputers and communications equipment; team headed by Professor Seijiro Furukawa

Linear/Analog

- Pioneer--Three custom ICs for large-screen television sets; PA0021/22/12 priced at ¥1,000 ($5.88), ¥700 ($4.12), and ¥800 ($4.70), respectively

- Tokyo Sanyo--An AM stereo decoder IC employing a counter-type pilot signal detection circuit; capable of handling three types of AM stereo broadcasts; sampling at ¥500 ($2.94)

Telecom ICs

- Corvus Systems/NEC--A CMOS single-chip LAN controller (MuPD72015); peripheral for NEC's V series MPUs; 4-Mbs data transmission speed; DMA controller with 24-bit address bus that addresses up to 16 Mbytes of memory space; 1.6-micron design rule; sampling at ¥20,000 ($118)

- NEC--A single-chip, high-speed (4,800-bit-per-second) modem; priced at ¥100,000 ($588), or half of conventional modems

  - Three small power modules for 900-MHz portable car telephones (MC-5848/49/50); sampling at ¥5,000 ($28.60)

  - A high-performance, single-chip CMOS LSI for data communications (uPD72001); 1.6 Mbs; 76mW power consumption; complements V Series MPUs; 8-MHz clock frequency; 1.5-micron rule; 40,000 elements; dual-channel structure; 75mW power consumption during operation and 1mW during standby; 40-pin DIP; sampling at ¥5,000 ($29.42)

- Sanyo Electric--Telephone dialing LSIs; 1.7V to 6V range for pulse operation and 2.5V to 6V for tone operation; 1V minimum for redial memory retention; 22-pin DIP; sampling at ¥400 ($2.35)

- Seiko-Epson--Two model LSIs; a one-chip, 1,200-kbs PSK-modulation CMOS LSI (ST9490C) compatible with the Bell 212A/CCITTV22; a CMOS LSI (ST9420C) that connects modems compatible with the Bell 102/CCITV21

Discretes

- Hitachi--Two high-withstand-voltage, high-current, power MOSPETs and two power FET modules; 120ns diode reverse recovery time; (see I.C. Asia, February 6, p. 6, for details)

- Mitsubishi--A 500-ampere power transistor module (QM500HA-H); 600-volt rating; 2,500 volt dielectric strength; sampling at ¥32,000 ($188)

- MITI Electrotechnical Lab--A single-crystal silicon carbide transistor that can withstand up to 300 degrees centigrade; 1.0 to 2.0-micron silicon carbide film on silicon crystal bases; for future use in nuclear reactor cores and jet engines

New Semiconductor Functions

- Hitachi/Institute of Physical and Chemical Research (Tsukuba Science City)--A new superconductive device, the quantum magnetic flux parametron; 1 nanowatt power consumption; 10ps switching speed; 20dB amplification; 1.8-GHz clock frequency

- MITI Electrotechnical Laboratory--A 3-dimensional XMOS transistor; source, drain, and gate MOS transistors on top and bottom of gates

- Riken/Hitachi--An ultra-high-speed switching element called the Quantum Flux Parametron (QFP) that combines Josephson junction and parametron characteristics; quantum magnetic flux used as the input signal, enabling operation with electrical voltage; power dissipation less than 1/1,000 of that of a Josephson junction; 0.2-nanowatt power consumption; 50ps switching speed; input signal amplified ten times; 1.8-GHz clock frequency

Bioelectronics

- Matsushita Electric/Hayashibara Biochemical--A new water-soluble photopolymer (Contrast Enhanced Lithography) for making 0.6-micron semiconductor circuit patterns; a new photopolymer material produced from "pullulan," a polysugar developed by Hayashibara and a diazo reagent developed by Matsushita; photopolymer produced by Japan Synthetic Rubber on contract basis for Matsushita

- Mitsubishi--A bio-device capable of transmitting electronics using protein molecules (titochrome C molecules extracted from a horse's heart); in protein film fabricated on an aluminum-deposited glass substrate; a fluorescent measuring system to verify the molecular orientation of protein molecules

- National Chemical Laboratory for Industry (Tsukuba)--An organic electroconductive ultra-thin film displaying chemically stable properties; developed using Langmuir-Blodgett method to produce highly ordered, 32-layer membrane structures, each only several molecules thick (0.13-micron thickness); L-B mono- or multilayer amphiphilic molecules spread over a liquid surface, compressed into one-molecule layers, and transferred to glass substrates; headed by researchers Yasujiro Kawabata and Takayoshi Nakamura

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New Processes

- Toshiba--A direct silicon bonding method to create diodes, transistors, and other devices without chemical processing; silicon boards heated in nitrogen gas to 1,000 degrees centigrade; oxide films removed to leave a thin hydrophilic layer; potential reduction in production costs by 40 percent and processing time to two hours; plans to commercialize a MOSFET for motor control parts

Materials

- Matsushita Electric--A garnet single crystal thin film containing bismuth for development of optical isolators; developed using liquid phase epitaxy method

- Nikon--Sputtering target material for 1Mb DRAMs; tungsten silicide material; CVD process utilized to achieve high purity and density

- Science and Technology Agency's (STA) National Research Institute for Metals--A niobium 3-aluminum superconducting strip capable of bearing one 20,000 ampere/square centimeter current load while maintaining superconductivity in a strong 23-tesla magnetic field; niobium titanium, niobium 3-tin, and other alloys limited to 14-tesla; potential for future superconductors and stronger magnets

- Sony--Two new single-crystal silicon technologies; one process produces crystal with 1.4 times higher oxygen density than conventional Czochralski method; a high-speed pulling technology two times faster than both conventional Czochralski and modified Czochralski methods

- Toshiba--An aluminum substrate with ten times the thermal conductivity of conventional substrates; 1,500 to 1,700 degrees centigrade metalizing process

- Tokyo Institute of Technology--An ultra-thin plastic film only one molecule thick for use as an insulating film for GaAs semiconductors; developed using the Langmuir-Blodgett method; a polyamic acid mixed with a long-chain alkyl amine to synthesize a polyimide precursor polymer, which was dripped onto a water surface to produce a monolayer film; film then mixed with acetic anhydride, pyridine, and benzene; joint project group headed by Professor Yoshio Imai

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- University of Tokyo--A single atomic layer metal film developed by Professor Masao Tsuneyama and colleagues; a multilayer structure of copper and molybdenum ultra-thin films stacked alternately on a silicon base; for development of superconductors and powerful, lightweight magnets

Manufacturing Processes

- Sumitomo Heavy--A single magnet synchrotron radiation ring (1-meter diameter) that is smaller than conventional SOR systems; for use in developing VLSIs over 4Mb

- Toshiba--A direct substrate welding technique, eliminating the need for epitaxial growth; P and N substrates directly welded to form PN junction; substrates heated in nitrogen gas at 1,000 degrees centigrade for 80 minutes; 2-hour process; for use in making high dielectric bipolar MOSFETs over 1,000 volts

Manufacturing Equipment

- Anelva--Two sputtering machines for 1Mb and 4Mb DRAMs; multilayer film-forming technology; three sputtering chamber type (ILC-1015i) priced at ¥200 million ($1,176,000); type with one etching chamber and two sputtering chambers (ILC-1015b) priced at ¥180 million ($1,059,000)

- Hitachi--A wafer stepper (RA-101VL) with 0.6-micron resolution for development of 4Mb memories and higher; capable of baking in 10.4 square millimeter circuits in one cycle and handling five-inch wafers; priced at ¥170-180 million ($1.0-1.1 million)

  - Two electron beam direct pattern drawing systems; a mass production machine (HL-600H) priced at ¥1.2 billion ($7.1 million); capable of processing 12 seven-inch wafers in one lot; a low-cost R&D machine (HL-600L) for ¥480 million ($2.8 million); capable of processing one six-inch wafer at a time

- Mitsubishi--A cluster ion-beam evaporating unit (four models) for creating a thin metal film on substrates by evaporation; priced at ¥35 to ¥100 million ($205,880 to $588,235)

  - Mitsubishi/Tokyo Electron--An optical/plasma-assist excimer laser-CVD machine for submicron designs up to 16Mb

- Nikon--A high-precision argon-ion laser lithography unit (LP-3000F) that draws circuit patterns by raster scanning of pixels on printed circuit boards without a master film

  - Two reduction projection lenses for mask aligners; one lens with 20 square mm exposure and 1.2-micron resolution power; the second lens with 5 square mm reduction projection area and 0.6-micron resolution power

- Pioneer--An optical beam soldering system (FS-1010) capable of soldering a four-sided flat package lead; priced at ¥8.8 million ($51,765)

- Sumitomo Metal--An experimental ECR reactive ion shower etcher

Factory Automation

- NEC--A robot system to weld custom VLSIs with legs 0.9mm apart onto printed circuit boards; visual sensor, two robots, and laser projector incorporated into system

Test Equipment

- Ando Electric--A 100-MHz, 512-pin compatible VLSI tester (DIC-9035); maximum 1,024 pins; 500ps timing accuracy; capable of testing ECL, GaAs, multipin gate arrays, 16-bit and 32-bit MPUs, and peripherals; pricing around ¥200 to ¥500 million ($1.2 to $2.9 million)

Packaging

- Ricoh--A chip-on-board (COB) method to mount semiconductor components without package directly onto a printed circuit board; two to four times higher mounting density possible

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SUMMARY

Four major issues--the yen shock, overcapacity, the U.S.-Japan chip agreement, and "Star Wars"--have greatly influenced Japanese semiconductor research in 1986. Dataquest observes that Japanese companies are responding to these events in the following ways:

- Yen shock--Greater emphasis on basic research, access to foreign researchers, and innovative, high-value-added products to stay ahead of emerging Asian companies
- Overcapacity--Foundry agreements and technology exchanges with U.S. vendors, especially start-ups and companies entering the Japanese market
- U.S.-Japan chip agreement--Greater product diversification and closer joint development with users
- "Star Wars"--Much interest in keeping up with U.S. state-of-the-art developments, but continuing concern over U.S. commercialization of Japanese technology developed in the program

JSIS has observed that since 1985 Japanese companies have been rapidly shifting to creative research. Recent events are accelerating this trend, as evidenced by the increased Japanese R&D spending and opening of new research centers. The Ministry of International Trade and Industry (MITI) estimated that R&D spending for the top 12 Japanese vendors was 17 percent in 1985, up from 10.6 percent in 1984. To help companies make the shift, MITI, the Ministry of Posts and Telecommunications (MPT), and the Science and Technology Agency (STA) are organizing new semiconductor R&D projects.

Dataquest believes that there are many research opportunities for European and U.S. semiconductor makers in Japan. Under the new U.S.-Japan chip agreement, foreign companies may be eligible for "national treatment" in Japanese semiconductor R&D projects. Potential areas include:

- MITI and MPT national R&D projects, especially through the joint Japan Key Technology Center
- Exploratory Research for Advanced Technology Organization (ERATO) projects, which operate under STA's Research and Development Corporation of Japan (JRDC)
- Regional R&D consortiums in the 26 emerging technopolises (18 formally designated and 8 being reviewed by MITI)

- Joint R&D in national universities, possibly through university exchange programs

- Nippon Telegraph and Telephone's Atsugi Semiconductor Lab

We believe that companies with Japanese R&D centers or Japanese research partners will have a greater chance for participating in these projects. For our clients' convenience, we will issue a newsletter identifying all of the semiconductor R&D projects.

MAJOR TECHNOLOGY TRENDS

During the second quarter of 1986, Dataquest observed the following trends in Japanese semiconductor technology:

- Japanese government decision to participate in the Strategic Defense Initiative ("Star Wars")

- Early research on small synchrotron orbital radiation (SOR) rings for 16Mb and 64Mb DRAMs (6 projects)

- Plans for new TRON Project operating systems for 32-bit MPUs

- New projects at MITI/MPT's Japan Key Technology Center, including new materials, machine translation, electronic dictionary, fiber optic communications, proteins, aerospace, and Teletopia network

- A new $322 million STA Electronics Research Center planned for the Osaka region

- Formation of MITI-sponsored second-generation optoelectronic IC (OEIC) project for optical computing and optical communications

- MPT plans for a high-resolution television system by 1989

- Advanced work on 4Mb/16Mb video memories and commercialization of 2Mb/4Mb mask ROM kanji generators

- Development of specialized CRT and flexible disk drive controllers and image signal processors

- Automated CAD layout for standard cells
- Increasing commercialization of optoelectronics, GaAs devices, and high-electron mobility transistors (HEMT)
- Introduction of new processing equipment by semiconductor device makers

CORPORATE R&D

Year 2000 Semiconductor Technology Outlook

Nikkei Electronics recently interviewed six Japanese electronics industry leaders to obtain their views of semiconductor developments expected by the year 2000. The following is a summary of their views:

- Kazuhiro Fuchi (MITI's Fifth Generation Computer Project)--Impact of AI on electronics, but no sudden development of natural language processors or AI chips
- Eiryo Takahashi (Oki Electric)--GaAs, HEMT, optoelectronic ICs (OEIC), and AI-based CAD design systems, but no natural language processors
- Kyusuke Oka (Mitsubishi Electronic)--"Humanware" and computer-human interface
- Kyohei Sato (MITI's AIST)--Some progress on biochips
- Kyo Eii (Toshiba)--64Mb DRAMs, system-level ULSI chips, progress on knowledge data processors
- Mizuno (Matsushita)--Home expert systems

32-bit TRON Project

In June, eight Japanese companies (Fujitsu, Hitachi, Matsushita, Mitsubishi, NEC, NTT, Oki Electric, and Toshiba) formed the TRON Council to accelerate the development of proprietary 32-bit MPU technology and several operating systems for next-generation microcomputers. TRON, the

tentative name, stands for "The Real-time Operating Nucleus." The new council is headed by Hitachi's Kazuo Kanahara. In addition, three operating systems capable of handling Japanese and other foreign languages will be developed:

- B-TRON for office automation equipment
- I-TRON for real-time industrial systems
- M-TRON for networking with distributed multiprocessors

Because TRON is coded in C language, it will be hardware (MPU)-tolerant and allow the use of one I-TRON regardless of different MPUs. Since its formation, the project has made some progress:

- NEC, Hitachi, and others have already developed several I-TRON operating systems for 16-bit MPUs, and are focusing on 32-bit versions.
- Mitsubishi, Tokyo Sanyo, and Toshiba have developed 32-bit microcomputers around Intel's 80386.
- Matsushita Electric completed a prototype personal computer design for the B-TRON operating system developed by Tokyo University. The TRON machine, designed around the 80286, is capable of processing the Japanese language, images, graphics, alphanumerics, and sound. System development is slightly behind the I-TRON.

Synchrotron Orbital Radiation (SOR) for Megabit Memories

Development of small-ring SOR equipment has accelerated recently due to intensifying research on 16Mb and 64Mb DRAMs. As shown in Table 1, six SOR projects are under way in Japan.

Table 1

JAPANESE SYNCHROTRON ORBITAL RADIATION RESEARCH

Companies	Research Activity (Location)	Budget	Start
NEC/MOE High Physics Lab	SOR for 1Mb+ DRAMs (Tsukuba)	N/A	Jan. 1985
NTT/Hitachi	64Mb+ DRAM ring (NTT Atsugi Lab)	$42M	Fall 1987
MITI/Sumitomo Electric	4.19-meter diameter SOR for VLSI Research	N/A	1989
Sumitomo Heavy Machinery	1-meter diameter SOR for 16Mb+	N/A	1986
MITI/MPT (13 companies)	Ultrasmall SOR machine in 8 years	$61M	1986
Science & Technology Agency (STA)	Large-scale SOR at Kansai Science & Technology Basic Research Lab (total $322 million equipment)	N/A	1989

N/A = Not Available

Source: Dataquest
October 1986

Software R&D Consortium

Thirty-eight software houses formed the Japan Personal Computer Software Technology Laboratory (JPL) in May to coordinate large-scale R&D projects proposed by MITI. Capitalized at ¥100 million ($645,000), JPL includes Computer Services Kaisha, Konami Industries, Fujitsu BSC, Nippon SE, Pony, and others. Eight hardware companies and four banks will join in the fall.

New Materials R&D Centers

Due to funding from the joint MITI-MPT Japan Key Technology Center and growing industry interest, many new materials R&D centers have been formed in 1986, including those shown in Table 2.

Table 2

MITI/MPT JAPAN KEY TECHNOLOGY CENTER ACTIVITIES

Research Center	Participants	Activities
Fine Ceramics Center	Ceramic makers in Chubu area	Fine ceramic standards and specifications
Japan High Polymer Center	Mitsubishi Chemical Sumitomo Chemical 18 other firms	Engineering plastics and composite materials; assay methods
Japan Metals R&D Center	Nippon Steel 39 other firms	New materials for oil development and light-water nuclear reactors
Metal Surface Research Institute	Nippon Steel Nippon Kokan Kawasaki Steel 14 other firms	Heat- and corrosion-resistant metal surfaces
New Glass Forum	80 glass, chemical, and ceramics firms	High-grade glass
New Material Center	Kansi Economic Federation Osaka Science and Technology Foundation	Assay methods and standards for metal-based industrial materials
Non-Oxide Glass	Nippon Sheet Glass Hoya	Non-oxide glass, infrared transmitting glass, infrared rays in medical fields

Source: Japan Economic Journal
Dataquest
October 1986

GOVERNMENT R&D PROJECTS

During the 1980s, Japanese ministries have organized 26 semiconductor-related joint R&D projects, as shown in Table 3. Dataquest observes that most of these projects are patterned after the highly successful VLSI Project (1976-1980), which developed the 64K DRAM and photolithography equipment.

Table 3

JAPANESE GOVERNMENT SEMICONDUCTOR-RELATED JOINT R&D PROJECTS

Duration	Budget ($M)	Agency	Project
1979-86	$112.5	MITI	Optical Measurement and Control Systems
1979-91	$375.0	MITI	Fifth Generation Computer
1981-86	$ 11.0	STA	Perfect GaAs Crystals
1981-86	$ 11.0	STA	Nanomechanisms
1981-90	$143.7	MITI	Scientific Supercomputer
1981-90	$114.0	MITI	Future Electron Devices
1981-90	$ 50.0	MITI	Fine Ceramics
1982-87	$ 10.0	STA	Bioholonics Systems
1983-88	$ 10.0	STA	Bioinformation Transfer
1983-88	N/A	STA	Speech Synthesis and Recognition
1983-90	$125.0	MITI	Advanced Robotics (Jupiter)
1984-90	$730.0	NTT	Information Network System (INS) Computer
1985-90	N/A	STA	Solid State Surfaces
1985-91	$156.3	MITI	Sigma Automated Software Development
1985-90	$ 40.0	MITI	Biochips/Biocomputer
1985-93	N/A	MITI	Next-Generation IC Equipment
1985-88	N/A	Tokyo U.	TRON Project (32-bit MPU)
1985-N/A	$ 23.5	Kyoto U.	Supercomputer (with Matsushita)
1986-96	$ 93.6	MITI	Synchrotron Orbital Radiation (SOR)
1986-96	$ 62.5	MITI	Optoelectronic ICs (OEICs) for Optocomputers
1986-96	$625.0	MPT/MITI	Automated Translation Telephone
1986-88	N/A	JIRA	Robot Sensors
1986-88	N/A	MPT	High Resolution TV System
1986-N/A	$ 1.9	MPT/MITI	Electronic Dictionary
1986-N/A	N/A	Tohoku U.	Automotive Electronics and Materials
1987-N/A	N/A	MITI	New Diamond Substrates

N/A = Not Available

Legend: MITI = Ministry of International Trade and Industry
MPT = Ministry of Posts and Telecommunications
STA = Science and Technology Agency
NTT = Nippon Telegraph & Telephone (privatized in 1985)
JIRA = Japan Industrial Robot Association

Source: Dataquest
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MITI Research Plans for Fiscal 1986

The Ministry of International Trade and Industry's (MITI) Agency of Industrial Science and Technology (AIST) has framed an R&D plan for fiscal 1986, for 12 categories being promoted by the Research and Development Project of Basic Technology for Future Industries. The project, which began in 1981, includes the following categories: fine ceramics (10 years); high-crystal molecular materials (10 years); optical reactive materials (8 years from 1985), superlattices (10 years); and 3-dimensional ICs (10 years). Fiscal 1986 is the sixth year of research. Project teams will reach the basic test manufacturing and evaluation phase by the end of the fiscal year (March 1987).

MITI/MPT Japan Key Technology Center

The Japan Key Technology Center, jointly formed in 1985 by MITI and the Ministry of Posts and Telecommunications (MPT), allocated ¥2 billion ($12.9 million) in its fiscal 1985 budget for 25 large-scale R&D projects. The projects, which will last 5 to 10 years, include the following:

- Machine translation systems
- Electronic dictionary--Fujitsu, Toshiba, and six other companies in a new research institute
- Fiber optic communications
- Proteins--Mitsubishi Chemical, Kyowa Hakko Kogyo, and six others in new joint company with ¥200 million ($1.3 million) subsidy
- Aerospace--Ishikawajima-Harima Heavy, NEC, and four others in a new joint R&D organization with ¥75 million ($484,000) subsidy
- Teletopia Concept--MPT feasibility study of future urban communications for tourism, industries, and emergencies in 34 test cities

MPT/MITI Electronic Dictionary Project

In May, eight electronics companies formed the Japan Electronic Dictionary Research Center under the auspices of the MITI-MPT Japan Key Technology Center. Capitalized at ¥300 million ($1.9 million), the consortium includes Fujitsu, Hitachi, Matsushita Electric, Mitsubishi Electric, NEC, Oki Electric, Sharp, and Toshiba. The goal is to develop

an electronic dictionary data management system, using up to a hundred 32-bit workstations linked by local area networks (LANs). The consortium will work closely with NTT and MITI's Fifth Generation Computer Project (ICOT).

New STA Electronics Research Center

The Science and Technology Agency (STA) is establishing a new research center, the Kansai Institute of Physical and Chemical Research, in the Osaka (Kansai) area to promote basic research in electronics, new materials, and life sciences. Funded at ¥50 billion ($322 million), the center will be equipped with a synchrotron orbital radiation (SOR) machine for research on megabit DRAMs, new functional elements (3-D ICs and super-lattices), and biomaterials (bioelectronics). Two sites are being considered: the Nishi-Harima Technopolis (Hyogo prefecture) near Kobe, or the Kansai Cultural and Academic City (between Osaka, Kyoto, and Nara).

Data Drive Microprocessor Project

In June, a government-sponsored microprocessor group announced a prototype data drive microprocessor that increases the speed of microprocessors by 100 times. The project, which ended in March 1986, employed parallel processing and asynchronous pipeline processing techniques. The four participating companies, including Matsushita, Mitsubishi Electric, Sanyo, and Sharp, have agreed to cooperate in developing commercial devices. Dataquest observes that these companies are also trying to develop minisupercomputers employing 32-bit microprocessors and parallel processing architectures through Tokyo University's TRON Project.

MITI Optoelectronics Project

In April, MITI announced that it will provide consignment loans (itakuhi) to nine Japanese semiconductor makers to establish a new optoelectronics R&D consortium, the Optical Technology R&D Corporation. The consortium will focus on second-generation optoelectronic ICs (OEICs) for optocomputers and optical communications. Participating groups include MITI's Electrotechnical Laboratory, Oki Electric, Sumitomo Electric, NEC, Hitachi, Fujitsu, Furukawa Electric, Matsushita Electric, Mitsubishi Electric, and others. MITI will loan ¥3.5 billion ($22.6 million) worth of GaAs crystal growth and crystal impurity evaluation equipment. For more details, see our Research Newsletter, "Japan's Push into Optocomputing," dated May 1986.

MITI Fifth Generation Computer Project

The Japanese and U.S. governments have agreed to cooperate on the development of fifth-generation computers. The National Science Foundation and MITI's Institute for New Generation Computer Technology (ICOT) will exchange researchers and technical information beginning in the spring of 1987. Research will focus on inference subsystems and knowledge-based subsystems, which will incorporate next-generation VLSIs. Recently, companies announced new products coming from the project as follows:

- Hitachi announced a relational data base processor for its three 68X Series computers, which compete with IBM's 3090 Sierras. The H-P6085-6 relational data base processor has a data base processing speed reportedly 20 times faster than conventional methods.

- Mitsubishi Electric announced a sequential inference machine, Melcom PSI, which runs on PROLOG and has a speed of 40,000 logical inferences per second (LIPS). The language is ESP (Extended Self-Contained PROLOG) and the operating system is SIMPOS, also developed by ICOT. It is supported by the EXT Kernel expert system support tool, library, and interactive functions. The system includes a 20MB main memory, a 70KB cache memory, two 1MB flexible drives, a 200MB fixed disk, a 17-inch 1,280 x 960 monochrome bit-map display, a kanji printer and programming, and operating systems. The basic system is priced at ¥20 million ($129,000).

MITI Machine Translation Project

The Ministry of International Trade and Industry (MITI) plans to develop a prototype machine translation system by 1988 or 1989, with the goal of commercializing the system between 1992 and 1994. The Japan Electronic Dictionary Research Center was founded this April by eight companies--Fujitsu, Hitachi, Matsushita Electric, Mitsubishi Electric, NEC, Oki Electric, Sharp, and Toshiba (see Technology Trends First Quarter 1986 Section, page 9 for details on consortium). MITI's Institute for New Generation Computer Technology (ICOT) will provide the hardware and operating system. The Cooperative Center for International Information will work with ICOT to develop translation systems for other Asian nations.

Dataquest believes that this project is crucial because machine translation systems will have a major impact on the semiconductor and telecommunications industries. These machines will employ parallel processors, speech recognition and synthesis chips, fast logic, and other next-generation ICs.

U.S. Strategic Defense Initiative (SDI)

Hitachi, Mitsubishi, and NEC could become major participants in Japan's part in the Strategic Defense Initiative ("Star Wars" program) proposed by President Reagan. Recently, a survey was conducted by representatives from 21 Japanese companies and government agencies. Three areas being considered are:

- Hitachi--Directional energy weapons (X-ray and chemical lasers)
- Mitsubishi--Target searching, tracking, and monitoring of their destruction
- NEC--Kinetic energy weapons (electromagnetic missiles)

The Japanese government has committed itself to the SDI program, but is still evaluating its level of research involvement.

MPT High-Resolution Television System

The Ministry of Posts and Telecommunications (MPT) is sponsoring a program to develop by 1989 a high-resolution color television system that is completely compatible with existing broadcast facilities and NTCS receivers. The Extended Definition Television (EDTV) system improves vertical and horizontal resolution by about 60 percent. Although Japan Broadcasting Company (NHK) offers High Definition TV and the United States, Canada, and Europe are developing the Multiplex Analog Component, they have only partial or no compatibility with NTSC systems. Companies currently participating in the EDTV program are Fujitsu General, Hitachi, JVC, Matsushita, Mitsubishi Electric, Pioneer, Sanyo, Sharp, Sony, and Toshiba.

MPT Fiscal 1985 R&D Results

The Ministry of Posts and Telecommunications (MPT) reported success with its R&D work on very wideband transmission, optical fiber cable television, and retransmission for satellite broadcasting. These tests included the following:

- 550-MHz repeat amplifier, coaxial cable, and protector in a six-stage cascade connection, using a maximum frequency of 300 MHz
- Fiber optic multiplex transducer

- 1.3 GHz-repeat amplifier for retransmission of satellite broadcasting with cable television (frequency bands of 70, 250, 470, 770, 1,035, and 1,335 MHz)

Dataquest observes that MPT experiments are stimulating research on optoelectronic ICs (OEICs), semiconductor lasers, and GaAs microwave devices.

NEW PRODUCTS AND TECHNOLOGY TRENDS

Memory

Japanese manufacturers are rapidly introducing 2Mb and 4Mb mask ROMs for kanji character generators, PC software, and other OA applications. Shipments begin in the second half of 1986. Table 4 shows the available models.

Table 4

JAPANESE 2MB and 4MB MASK ROMS

Company	Type	Structure	Process	Access	Design Rule	Sample
Fujitsu	4Mb	x8/x16	CMOS	250ns	N/A	Q3/86
Fujitsu	2Mb	x8	CMOS	150/250ns	N/A	Q3/86
Hitachi	2Mb	x8/x16	CMOS	200ns	1.3 micron	Q1/86
Matsushita	4Mb	x8/x16	NMOS	250ns	1.4 micron	-
Mitsubishi	4Mb	x8/x16	CMOS	250ns	1.2 micron	Q3/86
Mitsubishi	4Mb	x8	CMOS	200ns	1.2 micron	Q4/86
NEC	4Mb	x8/x16	CMOS	250ns	1.0 micron	Q3/86
NEC	2Mb	x8/x16	CMOS	250ns	1.2 micron	Q2/85
NEC	2Mb	x8	CMOS	250ns	1.2 micron	Q3/86
Oki Electric	4Mb	x8/x16	CMOS	150ns	1.2 micron	Q1/87
Ricoh	4Mb	x8/x16	CMOS	150ns	1.2 micron	Q3/86
Ricoh	2Mb	x8/x16	CMOS	150ns	1.2 micron	Q3/86
Toshiba	2Mb	x8	CMOS	200ns	1.5 micron	N/A

N/A = Not Available

Source: Nikkei Electronics
Dataquest
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- Fujitsu--Two 256K SRAMs featuring 55/70ns access times (M881C86); 64K x 4-bit; NMOS memory cells and CMOS peripheral circuits; 1.3-micron process; low-resistance polycide for gate electrode material; ATD circuit to add speed and to lower power consumption; 550mW power consumption during operation and 55mW at standby; 28-pin DIP or 32-pad LCC; sampling at ¥18,000 ($109) for DIP and ¥20,000 ($121) for LCC

  - A 256K SRAM (MB81C81); 45ns access time; 256K x 1-bit; 5.0 x 11.3mm chip; 550mW power consumption during operation and 83mW at standby; 1.3-micron MOS process; polycide material; address transient detector (ATD) circuit; sampling at ¥18,000 ($116)

  - Three 64K ECL RAMs; 1.1W and 730mW power consumption using a decoder circuit; MBM10490 with minus 5.2V service power voltage; MBM100490 with minus 4.5V; MBM101490 with minus 5.2V; 22-pin dual inline and flat package; priced at ¥15,000 ($96.77)

  - An NMOS 72K SRAM (TMM2089C); 35/45/55ns access times; 8K x 9-bit with 1-bit parity for each 8-bit increment; 1.5 micron; shared word line that allows selective operation of memory cell array; activated decoder that allows operation of an eighth of the line address decoder; 743mW power dissipation during operation and 82.5mW at standby; sampling at ¥12,000 ($77.40)

  - A dual port CMOS 16K SRAM for use as a shared memory in microprocessor systems; 2.0-micron design rule; 2K x 8-bit structure; 90ns read-out time; 660mW power consumption during operation; sampling at ¥4,000 ($25.80); monthly production of 100,000 from October

  - Two CMOS 64K EEPROMs (MBM28C64/65) with error-correcting code (EEC) circuit; 50/350ns access times; CMOS for peripheral circuits; 20mA in reading and 40mA in writing

  - A CMOS 256K EPROM (MBM27C256H); 100/120ns access times; 50mA power consumption; 1ms basic pulse width; Intel's fast write-in method; polycide; 28-pin cerdip package; 32-pin LCC; sampling at ¥3,000 ($19.35)

  - Two 1K bipolar PROMs (MB7113L/MB7114L); 35/50ns access times; 40mA power consumption (standard 25mA); three-state output for 7114L; 16-pin DIL ceramic, DIL plastic, and flat plastic packages; 20-pad LCC ceramic package

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- Hitachi--A CMOS 1Mb pseudo-SRAM (HM658128P/LP) featuring DRAM memory cells and SRAM peripheral circuits; 128K x 8-bit; 1.3-micron CMOS process; 120ns access time; 190ns shortest cycle time; 85mA power consumption during operation; 3.6 x 11 square micron memory cell; 4.99 x 14.4mm chip; 32-pin DIP; ¥14,000 ($84.84) to ¥16,000 ($96.97) per unit; sampling at ¥10,000 ($64.50) in 10,000-unit orders; monthly production of 10,000 units by end of 1986

  - A 4Mb bubble memory; 27 x 33 x 7mm and 26 grams (versus 40 x 44 x 9mm and 55 grams for conventional models); 2.0-watt power consumption; priced around ¥46,500 ($300); for use in portable and personal computers, POS terminals, and word processors

  - Two CMOS 1Mb EPROMs (HN27C101 and HN27C301); 1.3-micron Hi-CMOS process; 128K x 8-bit structure; 200ns access time; 150mW power consumption at 5 MHz; 0.6-inch pitch, 32-pin DIP package; sampling at ¥12,000 ($69), or ¥8,000 ($46) for 1,000-unit lots; monthly production of 200,000 to 300,000 by late 1986

  - Two 2Mb CMOS mask ROMs; 64K x 16-bit (HN62302P) and 128K x 8-bit (HN62402P); 40-pin plastic DIP; 50mA power consumption during operation and 20mA at standby; 15.2mm chip; sampling at ¥2,600 ($16.78); ¥1,950 ($12.58) for 1,000-unit lots

  - A CMOS 256K DRAM (HM51256L); 2-micron process; 256K x 1-bit; standby mode added to the substrate bias generation circuit; 200 milli-Angstroms power consumption; 256 cycles/32ms refresh time; 100ns access time

  - A 64K ECL RAM using Hi-BiCMOS technology; 16K x 4-bit; 20ns access time; 500mW power consumption during operation and 350mW at standby; 4.4 x 6.81mm chip size; small LCC package; shipping since June at ¥9,000 ($54.22) each for 10,000-unit lots

  - A CMOS 256K SRAM (HM62256) using 1.3-micron Hi-CMOS process; 32K x 8-bit; 85ns access time; 40mW power consumption during operation at 1Mhz; 15mA power dissipation; 28-pin 600 mil DIP; 1.6 million elements

  - A CMOS 16K SRAM (HM6268P); 1.3-micron Hi-CMOSIII technology; 4K x 4-bit; 25ns access time; 90mA operating power current and 2mA at standby; 4-partitioned memory array mode; sampling at ¥3,000 ($19.35) individually or ¥2,000 ($12.90) each for 1,000-lot orders

- A CMOS 16K EEPROM with 8-bit MCU (HD65901); 2.0-micron process; 5.6 x 5.7mm chip; 114,000 transistors; 24K mask ROM; 128-byte RAM; for use in IC cards, telephones, factory automation, and word processors

- A CMOS 1K EEPROM with 8-bit MCU (HD401220); pulse width modulation method; 2-Kbyte ROM; 32-byte RAM; 10mA power consumption; 28-pin shrink DIP

- An 8K dual port memory (HD63310); 1K x 8-bit; 200/250ns access times; two-surface FIFO; 100mW power consumption; 48-pin plastic DIP; priced at ¥2,700 ($17.42)

• Matsushita--Prototype 4Mb and 16Mb DRAMs using three-dimensional structure; 4Mb DRAM test manufacturing by late 1986 and 16Mb by 1987; volume production by Matsushita Electronics

- A 4Mb DRAM frame memory for video equipment; 0.8-micron design rule; fabricated using trench capacitor technology; memory capable of storing image information for slow motion or freeze frame functions in television sets and VTRs; 9 million elements; 10Mb of memory required to produce quality images in high-definition television sets; development to be announced at ISSCC 1987

- A prototype 16Mb DRAM featuring 0.5-micron design rule; 100-square millimeter chip with 35 million elements capable of storing 64 pages of newspaper data; evaluation samples from 1987

- Two 1Mb video DRAMs (MN411000/1); 1Mb x 1-bit and 256K x 4-bit types; NTSC method color television signals; 30ns cycle time; eight 8-bit shift registers for A/D conversion; four 32K x 8-bit memory cell arrays; for color television sets and home VCRs

• Mitsubishi--Three NMOS 512K EPROMs (M5L27512K); 200ns/250ns/300ns access times; 1.8-micron process; 64K x 8-bits; compatible with Intel 27512; 525mW power consumption during operation and 210mW at standby; 4.6 x 7.48mm chip; 28-pin DIP package; sampling at ¥4,000 ($24.24) per unit; initial production of 100,000 units monthly

- A new memory cell technology for 4Mb DRAMs; double-layer diffusion structured thin capacitor cell; vertical trench cells 1.0 to 1.5-micron in diameter and 3.0 to 4.0-microns deep on a silicon wafer surface; P-layer formed using

boron-injection CVD method; N-layer formed using diffusion furnace; soft error rate reduced tenfold; plans for prototype 4Mb DRAM by late 1986

- Eighteen CMOS 1Mb DRAMs; 256K x 4-bit; 100/120/150ns access times; high-speed page mode or static column mode; 1.2-micron design rule; 4.73 x 13.84mm chip; 330 to 440mW power consumption during operation and 5.5ms at standby

- A digital video line memory; PAL method; 8-bit A/D data conversion; 18,160-bit memory storage; 4-transistor memory cell; 19.5 x 20.0-micron cell; 5.83 x 4.29mm chip

- A video CMOS 256K dual-port memory (M5M4C264); 64K x 4-bit; 120ns access time; 220ns cycle time; 100mA power consumption; 1.7-micron process; 4.86 x 9.14mm chip; 59.2-square-micron memory cell; 24-pin DIP type sampling at ¥1,400 ($9.00); 24-pin ZIP at ¥1,500 ($9.68)

- NEC--A CMOS 64K SRAM (μPD4362C); 45/55/70ns access times; 1.7-micron gate length; 16K x 4-bit; 495mW power consumption during operation and 110mW at standby; 22-pin DIP; ¥5,000 ($32.25) each for 1,000-lot orders

  - Two NMOS 1Mb DRAMs; 1Mb x 1-bit; 120ns access time and 18-pin DIP for page mode (μPD411000); 150ns access time and 26-pin SOJ for nibble mode (μPD411001)

  - A CMOS 16K EEPROM with built-in 8-bit, single-chip MCU; 1K RAM, 32K ROM; 5.43 x 6.06mm chip

  - A large-capacity 256K CMOS FIFO RAM (μPD42532C); high-speed register and control circuit on 7.0 x 8.0mm chip; 1.2-micron CMOS process; 32K x 8-bit; parallel input/output memory; 50ns access time; 100ns cycle time; for use as buffer memory in digital facsimiles, PBXs, disk and magnetic tape control equipment, data transmission/ receiving equipment, and page printers; sampling at ¥10,000 ($64.50)

  - Two FIFO DRAMs (μPD42505C); 50/75ns access times; 660mW power consumption; 300-mil 24-pin DIP; for digital signal processing for facsimiles; 75ns part sampling for ¥5,000 ($32.25)

- Seiko Epson--Two 256K SRAMs; 100/120ns access times; 32K x 8-bit structure; 1.2-micron design rule; 40mA power consumption during operation for standard model and 13mA for low power model; priced at ¥4,000 ($25.80) and ¥5,000 ($32.25), respectively

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- Sharp--Two CMOS 64K EPROMs with 70ns access time; 1.6-micron design rule in cell section; 2.5-micron gate channel in peripheral circuits; bipolar PROM-compatible 24-pin DIP (LH5749J) and standard EPROM-compatible 28-pin DIP (LH5763J); 16-second write-in time; sampling at ¥9,000 ($55)

  - Two CMOS 1Mb DRAMs; 1.2-micron process; 67.5-square-mm chip size; 256K x 4-bit; 300-mil, 20-pin DIP package; static column mode and high-speed serial access mode versions; 100ns access time in random access mode; 30ns in static column mode; 35ns in high-speed serial access mode; sampling in September 1986; volume production from December 1986

  - Two 256K SRAMs (SRM20256LC); 100/120ns access times; CMOS peripheral; 13mA power consumption at 1 MHz; 28-pin 15.2mm plastic DIP; sampling at ¥5,000-¥6,000 ($32.25-$38.70)

  - A 1Mb mask ROM (LH531000); 1.5-micron process; 128K x 8-bits; ion injection system and single-layered polysilicon architecture; 5.55-square-mm chip; 25mA power consumption using automatic power-down method; 250ns access time in normal mode and 100ns in nibble mode; input/output TTL compatible; 28-pin DIP and planned 44-pin QFP; sampling at ¥2,000 ($11.11); volume production of 100,000 units monthly planned

  - A CMOS high-speed line memory (LH5015); 2-micron process; 6.0 x 4.5mm chip size; 60,000 elements; 25ns access time; 28-pin DIP; 90mA power consumption at 14.3 MHz; 40MHz maximum operating frequency; sampling at ¥2,000 ($11.76)

- Toshiba--Sub-micron production plans at its Oita plant from summer 1987; 1Mb DRAMs, 1Mb video RAMs, later 4Mb DRAMs; ¥70 billion ($424 million) three-story clean room for 0.7 to 0.8-micron design rule currently under construction

  - A prototype CMOS 1Mb SRAM capable of storing 130,000 alphanumeric characters; 1.0-micron process; 5.99 x 13.8mm chip; 2.2 million elements; 62ns access time

  - CMOS 1Mb EPROM; 14-second write-in time; 1.2-micron design rule; 150/200ns access times; compatible with 1Mb mask ROM (TC571001D); 158mW power dissipation during operation and 0.53mW at standby; 128K x 8-bit; 6.56 x 6.90mm chip; 32-pin DIP (JEDEC) and 28-pin DIPs compatible with 1M mask ROMs; sampling from June at ¥10,000 ($64.50); volume production from September

- Two 1Mb DRAMs; small outline package J (SOJ) lead type and plastic leaded chip carrier (PLCC) type; monthly production of 1 million units by end of 1986

- A CMOS 2Mb CMOS mask ROM (TC532000P); 1.5-micron process; 200ns access time; sampling at ¥4,000 ($22.86) for 1,000-unit lots; monthly production of 300,000 units from mid-1986

- A 72K SRAM (TMM2089C); 1.5-micron process; 35/45/55ns access time; 8K x 8-bit consisting of 8K x 9-bits with parity bit added for memory; NMOS memory cell with high resistance load; shared word line that operates one of four divided memory cell arrays by row address decoder, and activated decoder that operates one-eighth of row address; 743mW power consumption in operation and 82.5mW at standby; sampling at ¥12,000/¥11,000/¥10,000 ($77.42/$70.97/$64.52), respectively

- Six CMOS video field memories (TC9025F) for VTRs; 6-bit D/A and A/D converter; 10.74-MHz sampling wavelength; four 256K DRAMs; two 64K DRAMs; 120ns cycle time; 10mA power consumption during operation; 67-pin flat package; sampling at ¥1,000 ($6.45) from August

Application-Specific Memory (ASM)

- Dai-Nippon Printing--An IC card with a 16K EEPROM and MCU; sampling from June at ¥3,000 ($18.07) each for 10,000-unit lots, ¥2,000 ($12.05) each for 100,000-unit lots

- Hitachi--Two video RAMs (HM53461/HM53462); 2-micron CMOS process; 100ns RAM access time; 40ns serial access memory cycle time; 120mA power consumption during operation and 5mA in standby; shift register of 256 bits

- Ministry of Posts and Telecommunications (MPT)--Formation of an IC Card Application Association to study consumer needs and card reader environment; focusing on service content, memory management method, and card printing arrangements

Microprocessors/Microcontrollers

- Hitachi--An experimental 32-bit MPU (A132) developed with Tokyo University; object direction language; 1.3-micron CMOS process; 12.0 x 11.6mm chip; 382,000 transistors; 4K EPROM; each unit

connected by two 32-bit bus controllers; 256 x 2 register field; tag architecture; 18 times faster than 68000 at 8MHz

- A single-chip 8-bit MCU (HD65901); 2K built-in EEPROM, 3K mask ROM, and 128-bit RAM; 32-bytes of data rewritable once in the EEPROM; 5.6 x 5.7mm chip; data security function featuring a software key; sampling at ¥5,000 ($30) each in 500-unit orders and ¥1,900 ($11) per unit for 10,000-unit orders; for use in IC cards, numerical controls, and other data storage equipment

- A CMOS 8-bit MCU (HD63701Y) with built-in 16 Kbyte PROM; sampled from April at ¥3,000 ($16.67) per unit for plastic DIP, 1-MHz version; priced at ¥2,300 ($12.78) each for 1,000-unit lots

- A CMOS 8-bit, single-chip MCU (HD401220) with built-in 256-bit EEPROM for use in VCRs and television tuner controllers; two peripheral LSIs (HD63484/63486); sampling from September at ¥1,500 ($8.82) each, or ¥900 ($5.29) per unit for 10,000-unit orders

- Two interface ICs for small hard disk drives (HA16662MP/HA16682MP); priced at ¥1,650 ($10.00) per unit or ¥1,100 ($6.67) in lots of 10,000; two motor drive ICs (HA13441/13442); priced at ¥1,500 ($9.09) and ¥2,100 ($12.73) per unit respectively, or ¥1,000 ($6.06) and ¥1,400 ($8.48) in 10,000-unit lots

- Two CMOS CRT controllers (HD6345F/HD6445F); 2-micron process; 50mW power consumption at 4.5-MHz display action frequency; capable of controlling the display of a 1,280 x 1,024-dot high-resolution CRT; HD6345 with 6800 bus interface; HD6445 with 8080 bus interface; 40-pin plastic DIP; sampling at ¥1,500 ($9.68) and ¥1,800 ($11.61), respectively

- Two CMOS CRT controllers (HD63645F/HD64645F) for 640 x 400-pixel color display; 50mW power consumption at 10MHz; 80-pin plastic flat package; ¥900 ($5.80) each for 1,000-unit orders

- Two CRT controllers (HD63485); 640 x 400-pixel image; up to 64 MHz systems; 2.0-micron Bi-CMOS process; 4.6 x 4.7mm chip (GMIC); 4.8 x 4.8mm (GVAC); 64-pin shrink DIP priced at ¥2,800 ($18.06); 68-pin PLCC priced at ¥3,100 ($20.00)

- A 16-bit peripheral MPU (PIT HD68230) with direct memory access transfer for HD68000; system linked using HD68000 or HD68450 (direct memory access computer) with peripheral equipment; double buffer function; sampling at ¥1,900 ($12.25) or ¥1,300 ($8.39) each in 1,000-lot orders

- Mitsubishi--Nine CMOS 8-bit single-chip MCUs in MELPS740 series; total of 33 models; monthly production of 300,000 units since June

  - Two 8-bit MCUs with built-in 16K EEPROMs (M50747E-SP and M50747E-ES); sampling at ¥2,000 ($15.06) for SP model and ¥3,500 ($21.08) for ES model; initial production of 100,000 units per month

  - Six CMOS single-chip 8-bit MCUs (M50930-FP/M50931-FP); 1K RAM storage (M509320) or 2K storage (M50931); 16K ROM; 4.3-MHz clock; 20mW power consumption at 4 MHz; 80-pin plastic flat package; sampling at ¥1,100 ($7.10) for M50930 and ¥1,900 ($12.25) for M50941

- NEC--An electroluminescent display driver PMOS/NMOS IC for 1000 x 1000-dot panel; 300-320V drain pressure; NMOS transistors and n-well CMOS transistors

- Nippon Gakki (Yamaha)--A series of original MPUs using a static electricity induction transistor (SIT) structure; 16-bit, 24-bit, and 32-bit MPUs combined with Yamaha's ASICs and SIT logic for use in videoprocessing; MPUs incorporated in Yamaha's cell library (Dataquest believes that more Japanese companies will introduce application-specific MPUs using standard cells and, eventually, specialized compiler technology.)

- Oki Electric--A CMOS flexible disk controller (MSM6241RS); software compatible with Western Digital's WD2795/2797; for 8-, 5.25-, and 3.5-inch drives; 100mW power consumption at 8 MHz; 40-pin plastic DIP; 60-pin flat package; sampling at ¥3,000 ($19.35); ¥1,500 ($9.68) per unit for 10,000-lot orders

- Sanyo Electric--A CMOS digital servo control LSI (LC7990) for use in spindle motors of hard disk drives; 1- or 2-MHz clock signal; four motor speed detection signals (120/180/240/360Hz); 22-pin DIP; sampling at ¥700 ($4.50)

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- Sharp--Four V20 and V30 MPU versions second-sourced from NEC and a CMOS 4-bit, one-chip MCU

  - LH70108-5; sample price of ¥3,000 ($18.18); equivalent to NEC's CMOS 16/8-bit MPU (μPD70108-5)

  - LH70108-8; sample price of ¥3,500 ($21.21); equivalent to NEC's CMOS 16/8-bit MPU (μPD70108-8)

  - LH70116-5; sample price of ¥3,200 ($19.39); equivalent to NEC's CMOS 16-bit MPU (μPD70116-5)

  - LH70116-8; sample price of ¥3,700 ($22.42); equivalent to NEC's CMOS 16-bit MPU (μPD70116-8)

  - A CMOS 4-bit, one-chip MCU (SM5G4) with an invertor controller; CMOS silicon gate 2.5-micron process; 5.67-square-mm chip; 64-pin SDIP or 64-pin QFP; 6,144 x 9-bit ROM and 256 x 4-bit RAM; 17.5mW power consumption in operation and 5mW at standby

- Toshiba--Three original 4-bit CMOS MCUs (TMP47C800N); built-in 8K x 8 ROM and 512 x 4 RAM; 1.2-microsecond minimum execution time; 35 eight-bit serial input/output ports switchable to four bits; two 12-bit timers and ports capable of driving 8 LEDs directly; TMP47C440AN and TMP47C441AN with built-in A/D converter; 42-pin DIP; priced at ¥1,000 ($5.56) for TMP47C800N in 10,000-unit lots; ¥600 ($3.33) for TMP47C440AN; ¥650 ($3.61) for TMP47C441AN; piggyback version priced at ¥15,000 ($83.33) for each model

  - A CMOS SOS 16-bit CPU module (T88000) for gas turbine engine control; developed with Ishikawaharima Heavy; MIL-STD-883D; 5004.6 method, Class B; minus 55 to plus 125 degrees centigrade; peak speed of 3,000G; also an 8,000-gate CMOS array and mask ROM

Digital Signal Processors (DSPs)

At the 1986 International Conference on Acoustics, Speech, and Signal Processing, Japanese companies introduced the following DSP chips, as shown in Table 5.

Table 5

JAPANESE DIGITAL SIGNAL PROCESSOR CHIPS

Company	Model	Cycle	Data	Internal Memory	Process
Sony	N/A	75ns	32 x 16 bits	None	CMOS
Matsushita	MN1900	250ns	20-bit	66 x 16-bit RAM 2K x 32-bit ROM	2-micron CMOS
NTT	DSSP	50ns	12+6-bit	512 x 18-bit 4K x 32-bit ROM	1.2-micron CMOS
Oki Electric	MSM6992	100ns	16+6-bit	128 x 22-bit x 2 RAMs 1K x 32-bit ROM	2.0-micron CMOS
NEC	μPD77230	150ns	24+8-bit	256 x 16-bit 1K x 16-bit ROM	1.3 micron CMOS
Mitsubishi	mSP32	150ns	24+8-bit	256 x 16-bit 1K x 16-bit ROM	1.3 micron CMOS

Source: Nikkei Electronics
Dataquest
October 1986

A description of the DSP chips is listed below:

- Hitachi--Two CMOS graphic signal processors; HD63085Y capable of shrinking data by 1/10 to 1/30 according to CCITT facsimile standards; 72-pin PGA; priced at ¥24,000 ($154) each or ¥16,000 ($103) each for 1,000-lot orders; HD63084 capable of converting signals from facsimile CCD line sensors into digital form; 8-MHz internal processing speed; graphic data conversion at 5 mega-pixels per second; 4mW power consumption; 64-pin plastic shrink package; sampling at ¥7,000 ($45.16) each or ¥5,000 ($32.25) each for 1,000-lot orders

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- Mitsubishi--A CMOS digital signal processor for color television receivers; 18K-bit line memory allows simultaneous storage of two scanning lines; built-in filter to separate brightness and color signals; TTL level I/O; 5V power; 450mW power consumption at 17.7 MHz; 40-pin DIP; also for use in VCRs and facsimiles

- NEC--A CMOS signal processor with built-in 32-bit floating-point operations capability (μPD77230); 6.7 million floating-point calculations per second; 47-bit parallel shifter, 55-bit-floating point ALU; 55-bit by eight units working register; 3-stage pipeline structure allows parallel processing; 150ns command execution time; 2K x 32-bit instruction ROM; 1K x 32-bit data ROM; 512K x 32-bit data RAM; 150ns cycle time; 7.8 x 14.2mm chip; 1.5-micron dual layer aluminum CMOS process; 5V power source; 1.5W power consumption; 68-pin PGA; sampling at ¥80,000 ($516); 10,000 chips being produced monthly (see Technology Trends 1st Quarter/1986 section, page 20)

- Nippon Telegraph & Telephone (NTT)--An 18-bit floating-point DSP; 50ns cycle time; 4K x 32-bit command ROM; 512K x 18-bit dual-port data storage; 1.2-micron CMOS process; 9.22 x 9.61mm chip; 280,000 transistors; 64-Kbit/sec codec system also developed; for speech processing

- Oki Electric--A CMOS digital signal processor (MSM6992) with a floating-point arithmetic function; 100ns maximum cycle; 10-MFLOP-per-second capacity; 2-micron silicon CMOS process; 400mW power consumption; 1K x 32-bit built-in ROM and 128K x 22-bit by two-surface data RAM; memories externally expandable to 64K words; priced at ¥60,000 ($387)

- Sony--Three signal processing ICs (CXA1030M/1082M/1083Q) for cellular car telephones; capable of signal processing in line with AMPs (North America standard); sampling at ¥2,000 ($12.12)

- TI Japan--A locally developed CMOS high-performance DSP chip (TMS320C25); 100ns cycle time; 64K masked ROM for storing control program; 8K RAM for temporarily storing computed data; 1.8-micron design rule; for use in modems and voice processing systems

- Tokyo Sanyo--A single-chip signal processor (LA 7650) for NTSC color television sets; 4.5 x 4.6mm chip integrating 1,900 analog circuits and 400 digital gates; 42-pin DIP package; 90mA and 13mA power consumption; 9V and 7.8V power supply; sampling at ¥1,000 ($6.45)

  - A signal processing single-chip IC for NTSC standard color television sets (LA7650); 1,900 analog devices and 400 digital gates on 4.5mm chip sampling from August at ¥1,000 ($5.81)

  - Image signal processing ICs (LA-7300 series); 15 types; VHS method VTR; 3-MHz clock speed; 5V power supply

  - Four-color signal processors; record/playback low-pass filter; clock pulse generator for CCD; ID detector; sub/main converter; 3.58/4.43-MHz VXO; compatible with NTSC, PAL, and SECAM broadcast systems

  - Seven brightness signal processors; video AGC/detect; sub/main pre-emphasis; white/dark clip; FM modulation for recording

Application-Specific ICs (ASICs)

Japanese ASIC makers introduced papers on a variety of gate arrays at the IEEE 1986 Custom Integrated Circuits Conference held in Rochester, New York, in May. Table 6 lists these ASIC devices:

Table 6

JAPANESE GATE ARRAYS ANNOUNCED AT 1986 CICC

Maker	# Gates	Process	Chip Size	Pin Count
Fujitsu	30,000	1.8-micron CMOS	13 x 13mm	256
Mitsubishi	N/A	1.3-micron CMOS	10.2 x 12.7mm	219
NEC	624 to 3,140	Bi-CMOS, 1.6-micron gate	7.6 x 7.3mm	152
NEC	540	1.5-micron bipolar ECL	6.24 x 6.24mm	102

Source: IEEE 1986 CICC
Dataquest
October 1986

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The following are major ASIC announcements made during the second quarter:

- Asahi Chemical--Dissolved capital tie-up with Gould AMI and signed new licensing agreement with Hitachi to secure process technologies for CMOS SRAMs, 4-bit MPUs, gate arrays, and masked ROMs

- NEC--A Bi-CMOS gate array series; 624/124/2248/3140 gates; 0.8ns delay time; TTL-compatible CMOS interface; two NAND-gate MOS transistor; 1.5-micron thick n-type epi layer on a 0-type silicon substrate; 1.6-micron NMOS gate length; 1.8-micron PMOS gate length; 1.5 x 3.0 micron emitter method; ¥2.5 million ($16,130) development cost for 624-gate device; cost range from ¥2.5 million ($15,152) to ¥6 million ($36,364); unit price of ¥700 ($4.50) for 5,000 units

  - Experimental CMOS master slice ASICs employing analog and digital circuits; 2-layer polysilicon; 1- and 2-layer aluminum; parallel processing transistors; NMOS circuit with 2.6-micron channel length; PMOS circuit with 2.8-micron channel length; CAD tool being developed

- Nippon Telegraph and Telephone (NTT)--Three CMOS gate arrays for data flow processing; 3134/3941/4365 gates; 300ns access time; pipeline architecture; 192 and 400 pins

  - A CMOS 4,850-gate array for network switching; 4 x 4 switch; 32-bit data width

- Ricoh--Considering a joint-development project with Monolithic Memories, Inc. (MMI) to avoid patent dispute over Ricoh's electrically programmable logic (EPL)

- Rohm--A CMOS gate array series (BU1200 series); 156 to 3,025 gates; 3ns access time

- Seiko-Epson--A CMOS programmable logic device (SLC2064J) with built-in SRAM; 8 x 8-bit logic microcell; 33-MHz clock speed; equivalent to 1,200-gate array; designed by Xilinx; priced at ¥20,000 ($129); ¥10,000 ($64) each for 10,000-lot orders

- Sharp--Plans to open a custom design center in New Jersey; eventually plans to open a manufacturing plant in the United States

- Toshiba--New ASIC design centers planned for Los Angeles, Chicago, Boca Raton (Florida), and West Germany (two centers) by late 1987; existing centers in Boston, Dallas, and Sunnyvale

  - Prototype CMOS 50,000-gate array family developed with LSI Logic; 0.7ns gate delay; 1.5-micron gate length (PMOS/NMOS); NMOS graded double diffusion drain (GDD); 2-layer aluminum wiring (3 layers optional); 130,000 transistors; 13.3mm square chip; 20-MHz clock frequency

  - Joint development of standard cells with Siemens; Toshiba to provide circuit design and 1.5-micron and 1.2-micron CMOS process; Siemens to provide CAD design software

CAD Systems/Artificial Intelligence

- Fujitsu--A standard cell layout CAD system; ROM, RAM, and PLA compiler developed; wiring algorithm based on Min-Cut method; 2-level wiring; automated wiring for up to 4 memory blocks; 18-second wiring on FACOM M-380 for layout of chip with 2 NAND gate, 2,293 circuits, 4 functional blocks; announced at the IEEE Custom Integrated Circuits Conference, May 1986

  - A VLSI design personal computer CAD system (VIEWCAD); 16-bit PC (FM16-FDII) using 1Mb DRAM chips; ¥1.24 million ($8,000) or ¥100,000 ($645.20) for software only; logic circuit input and simulation; 0.1ns for simulation of 10,000-gate vectorized circuit

- Hitachi--An automatic translation system for consumer-type custom ICs utilizing an artificial intelligence system; designed for conversion of CMOS circuits into custom analog/digital logic circuits; HITACAM mainframe series and LONLI knowledge processing language used for AI system; one- to two-day conversion time; announced at 23rd Design Automation Conference, June 1986

- Matsushita Electronics--A Standard Layout Design Automation System (STELLA) for laying out 3-layer wiring (one polysilicon layer and two metal layers) within one channel; capable of laying out 30,000 gates or 120,000 transistors; 300-gate design within 30 minutes; being used for MN72000 series standard cell models of 2-micron linewidth; plans for 1.5-micron series featuring high-speed operation and low-power CMOS structure

- Mitsubishi Electric--Plans to market its 32-bit AI workstation, Melcom PSI (personal sequential inference) in the United States; extended self-contained PROLOG language (named ESP); priced at ¥20 million ($121,200); developed through MITI's Fifth-Generation Computer Project

- NEC--A VLSI expert system (VILLA) with multilevel operations; design object placed onto template in level 1; circuit rules input into knowledge base in level 2; currently developing design plan for large circuit blocks using heuristic rules

- Sega Enterprise--An AI home computer for computer-aided instruction (CAI) utilizing an NEC V20 MPU; AI language (Sega PROLOG) capable of Japanese language processing and image processing; graphics of child's daily activities drawn by inputting events in normal, everyday language ("Picture Diary"); priced at ¥87,500 ($530); programs priced from ¥4,900 to ¥8,750 ($28 to $50)

- Waseda University--A new computer-aided machinery parts processing and manufacturing system named DREAMS (Drawing Recognizable Automatic Manufacturing System); handwritten plans input into personal computer via a CCD camera and black-and-white picture display readout device; screw forms and curved-line drawings require further development work; project headed by Professor Hiroshi Nakazawa of Waseda's School of Science and Engineering

Optoelectronics

- Fujitsu--An optoelectronic IC (OEIC) prototype that integrates four laser diodes and a drive circuit on a 2 x 4 mm GaAs chip; heterostructure device consisting of alternate layers of AlGaAs and GaAs; four channels consisting of a 0.8-micron wavelength laser, photodiode, three FETs, and one resistor; 24 total elements; designed to couple with a four-channel OEIC consisting of a light-receiving element, four Schottky diodes, and two resistors on a 1.6 x 4.0mm chip; mass production system being planned to fabricate multichannel OEICs

- Hitachi--A distributed feedback laser diode ("6th generation laser") capable of transmitting data three to six times farther than conventional diodes; 1.3-micron device (HL-1341A) featuring a repeaterless transmission distance of 80 to 100km at 1-Gbps speeds; 1.55-micron device (HL-1341A) capable of transmitting data 100 to 200km at 1-Gbps speed; buried heterostructure;

5mW output; sampling at ¥400,000 ($2,424) for 1.3-micron device and ¥500,000 ($2,940) for 1.55-micron device; monthly production of 3,000 units for HL1341A and 1,000 units for HL1541A by March 1987

- Kodenshi--A GaAlAs LED diode (BL-23F) and a photodiode (HII-23F) for plastic optical fibers; 2.54 x 4.7 x 4.7mm size; 2.54mm pitch; BL-23F with 20mA output at 660nm; HPI-23F with 0.4A/W at 450 to 1050nm

- Matsushita--A 280mW GaAs laser diode using a buried twin ridge substrate; 50mW commercial diodes available soon; for use in optical disk systems requiring 25mW write-in and 40mW for data erasing

  - A second harmonic generation (SHG) device using niobic acid lithium crystal for optical laser in 0.4-micron zone; plans for practical use by employing semiconductor lasers and yttrium aluminum garnet (YAG) lasers

- MITI Optoelectronics Joint Research Lab--Optoelectronic IC (OEIC) technologies for transfer to Hamamatsu Photonics K.K. and Toshiba; project focused on key technologies for transmission speeds of more than 1-Gbs/sec

- Mitsubishi--A laser diode with 25mW maximum pulse light output; ML6000 Series; 780nm wavelength; for use as read-write devices for optical disk memory systems or pick-ups in compact disk players; sampling at ¥60,000 ($390)

  - A 1.55-micron band, long wavelength semiconductor laser; 10mA oscillation threshold current at 115 degrees centigrade; antimelt back layer built on InGaAsP active layer; for use in multiplex communication and fiber testers

- NEC--A single-chip optoelectronic IC (OEIC) for light emission and reception; 1.2Gb/sec transmission rate; 1.3-micron band; 7.7dB gain for 12km transmission distance in a single-mode optical fiber; 9.9dB gain for 22km distance; one semiconductor laser and three heterojunction bipolar transistors integrated on a single chip; semi-insulating InP substrate; one Pin photodiode and three indium FETs integrated on receiver IC

- Sanyo--A third-beam laser diode for optical disk systems; one chip integrating two 20mW chips for writing and erasing and one 5mW laser playback integrated on a chip; 810nm wavelength; 70mA for writing and erasing; 50mA for playback; ¥200,000 ($1,290)

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- Sony/Sharp--New standard for laser diodes used in compact disk and video disk players; jointly developed laser diode with 5.6mm diameter generator, 2.0mm lead pin pitch, and 1.35mm base-to-chip distance; 70 percent of CD and video disk markets dominated by both companies; sampling from Sharp at ¥2,500 ($15.15)

- Tokyo Institute of Technology--A new quantum-well structure for future optical computers; capable of integrating 200 to 300 optical switches on a single chip; activation time reduced to one 10-trillionths of a second; single chip with laser diode and optical signal detector; GaInAsP and InP layers of 6 to 8 nanometers alternately stacked; 20 to 30 times more optical switches possible than using lithium niobate; project headed by Professor Yasuharau Suematsu

- Toshiba--Two infrared LEDs for auto-focusing cameras; TLN206 with 14mW output and 250-micrometer spot diameter; TLN216 with 15mW output and 380-micrometer spot diameter; sampling at ¥300 ($1.81) each

  - A five-wavelength multiplex optical transmission system using five integrated semiconductor lasers of distributional feedback architecture; 1.3-micron band wavelength; submicron trenches of 0.7-micron in width and 0.3-micron in depth lined in a row at a 1.5-micron pitch

Image Sensors

- NEC--A half-inch CCD color image sensor for NTSC broadcasting system; 6.75 x 8.0mm; 1.2-micron process; 220,000 picture elements; 8 lux with F1 or F2 lens; 280 X 350 lines; 1mV dark output voltage; sampling at ¥30,000 ($194); monthly production of 100,000; plans for CCD sensor for PAL broadcasting system

- Sharp--An interline transmission CCD sensor (LZ22250G); NTSC-type television signals; 490 x 510 pixels; 2/3-inch optical circuit; p-well structure; 22-pin DIP; sampling at ¥26,000 ($168)

  - A CCD sensor for 2/3-inch NSTC-type black-and-white cameras (LZ22251); 510 x 490 pixels; sampling at ¥21,000 ($135)

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Gallium Arsenide

- Fujitsu--A commercial high-electron mobility transistor (HEMT) to amplify minute signals transmitted from communications satellites (FHR01FH); Ku (12 to 18 GHz) and K (18 to 26.5 GHz) bands; 1mW signal amplified ten times; 1.8dB noise index when amplifying 20-GHz signals; sampling at ¥150,000 to ¥200,000 ($909 to $1,212)

  - A 1,500-gate HEMT array used to build an 8-bit, single-chip multiplier; 3.1ns at minus 196 degrees centigrade; 5.5 x 5.6mm chip; 76 x 20 rows of gates; 72 I/O cells; 2-micron wiring linewidth; one depletion HEMT and three enhancement HEMTs in each gate; three depletion HEMTs and five enhancement HEMTs in each I/O cell; 0.12V threshold voltage for enhancement HEMTs; 1.11V for depletion HEMTs; work under way on 3,000-gate array

- Matsushita--World's first GaAs operation amplifier IC; 200-MHz gain level; 100 times faster than conventional silicon op amp; 18 FETs and 34 diodes on a 0.93 x 1.18mm chip; source-coupled FET logic; 1-micron gate length; for use in noise filters for digital imaging systems; sampling by end of 1986

  - A 280mW output GaAlAs semiconductor laser using a buried twin-ridge substrate (BTRS) structure; 8-layer structure on a p-type GaAs substrate; volume production of 50mW lasers planned

  - A one-chip laser noise canceler GaAs IC (MEL5005) integrating overlapping high-frequency oscillator circuits; 15-dBm oscillation output; 500 to 1,000-MHz frequency; 1.5-micron gate length; 0.7 x 0.45mm chip xsize; 25 FETs and 18 diodes; 4-pin plastic cross package; 475mW power consumption; for use in optical disk filing systems and CD-ROMs; sampling at ¥500 ($3.23)

- Mitsubishi Electric--A 1.55-micron wavelength semiconductor laser capable of oscillation up to 115 degrees centigrade; 10mA threshold current

  - A 1-GHz prescalar with 2.9mA current consumption; 4mA at 1.2-GHz frequency; 128/129 frequency division ratio, dual modular GaAs chip; source-coupled logic circuity with "surface n-plus" layer, slightly recessed FET structure; 1.9-GHz operating frequency at 9.2mA; 5V power supply

- MITI Electrotechnical Lab--A GaAs transistor called an inversion-base bipolar transistor (IBT) capable of speeds greater than HEMT devices; normal base replaced by an inversion layer of high-hole density inside the collector by applying an external negative field; thin films of single crystal GaAs for the base layer of hetero bipolar transistors (HBT) made possible using this simplified layout

- Toshiba--A new method to produce high-purity 3-inch GaAs monocrystals (Super MLEC); 50 to 60 defect-free wafers produced from a single ingot (compared to 10 for conventional methods); magnetic field Czochralski method; intensity of magnetic field tripled to 34,000 gauss to reduce thermal convection of melt during ingot raising; temperature differential within the melt less than 1 degree centigrade; aluminum nitride used for the crucible to prevent carbon mixing into the melt; computer program to control arsenic evaporation during crystal formation; fine ceramic melting pot used; based on 2-inch ingot formation technology from MITI's Optoelectronics Project (1979-1986)

  - A 31-stage GaAs ring oscillator IC; 35ps per gate; 10,000A per square cm emitter current density; 2.0 x 4.0-micron CML inverter circuit; AlGaAs/GaAs heterostructure bipolar transistor technology

  - A microwave amplifier HEMT (S8900); 1.6dB gain at 18 GHz; 0.25-micron gate length; also a 1.3dB gain chip (S8901); sampling at ¥150,000 ($968)

Josephson Junctions

Standard Logic

- Toshiba--A CMOS standard logic series (TC74AC); 3ns delay time; 1.5-micron design rule and dual-layer metal interconnect method; three-layer structure; 10 types with plans for 50 types by spring of 1987; 150-MHz operating frequency at the flip-flop circuit level; 24mA generating power current

Bipolar Logic

- Toshiba--A 32ps heterostructure bipolar transistor featuring GaAs collector layers and AlGaAs emitter layer and base; proprietary self-alignment technology (SAINT); single mask to form the external base layer, base electrode, and emitter electrode; 2-micron emitter width; 0.25-micron interval between emitter and base electrodes; enlarged electrodes used to handle error margins in mask alignment; phosphor ions injected to control horizontal diffusion of magnesium ions; prototype GaAs IC integrating 97 transistors on 0.35 x 1.5mm chip

Linear/Analog

- Fujitsu--An A/D master slice IC (A800) using op amp and analog switch macrocells; 60,000-gate macro; bipolar gate macro in CMOS structure; 16- to 28-pin DIP and SOP; development cost ¥5 million ($32,260); sampling at ¥1,200 ($7.75) from October

- Matsushita--Kits of three modem LSIs for data communications; 1,200-baud class, full-duplex type; meets Bell 212A standard and CCITT V22 international standard; sampling at ¥5,000 ($29.07) per kit

- Mitsubishi--A voltage control type amplifier IC for audio volume control use (M5241L); 36V to minus 18V power supply voltage range; 10-pin SIL resin package; sampling at ¥140 ($0.90); for radio cassette players, stereo decks, and electronic keyboard musical instruments

  - An 8-bit CMOS A/D converter; 1.5-micron process; 30Mb/sec sampling rate; 180mW power consumption at 30 MHz; 60mW at 20 MHz; 3.08 x 2.56mm chip; 10,179 elements

- NEC--A linear power transistor for VHW zone transmitters (2SC3812); 200W at 230 MHz and 280V; sampling at ¥55,000 ($331.88) each

  - Four CMOS 1-chip pulse code modulation (PCM) codecs (μPD9513) family); A/D and D/A converter; 16-pin to 24-pin DIP

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Discretes

- Matsushita--A single-chip Darlington transistor with power transistors connected between the drive stair and output stair; six families (12 models in complementary pairs) ranging from 35W to 100W of maximum collector loss; sampling at ¥150 ($0.90) each for 35W model, and ¥400 ($2.41) each for 100W pair in lots of 100,000 pairs

- Mitsubishi--Six high-current MOSFET modules suitable for 20-KHz to 100-KHz inverter control switching; sampling from ¥7,000 ($40.70) to ¥14,000 ($81.40)

- NEC--Two 500-KHz power supply control ICs capable of directly driving power MOSFETs (PC1094C/G); sampling at ¥300 ($1.67); monthly production of 200,000 units in last half of fiscal 1986 and 600,000 units in first half of fiscal 1987

  - 90 models of semipower, built-in resistance-type transistors capable of 2A collector current; single high-current amplification rate process and low-saturation voltage process used with mesh emitter structures; marketing of devices named "perfect protective transistors"

- Sanken Electric--A power transistor array (SLA4061) with four transistor circuits and high-speed diodes for driving motors and solenoids used in OA equipment; maximum 5W output power; 1.0-1.5V collector saturation voltage; 12-pin single inline package

- Sharp--Two high-input-resistance FET amplifiers; IR9082 with 8-pin DIP; IR9082N with 8-pin SOP; junction FET and bipolar transistors integrated on a single chip; Bi-FET process; sampling at ¥130 ($0.84)

New Semiconductor Functions

- Sharp--A new insulator film for future 3-D ICs; silicon oxynitride film with a thermal expansion coefficient similar to silicon crystals being insulated to prevent warping; film formed by irradiating monosilane, ammonia, and nitrogen oxide gases with ultraviolet rays; six-layer circuits theoretically possible; same thermal expansion as silicon; film formation 3 to 4 times faster than silicon oxide; 1cm-thick layer capable of bearing 7 million volts; developed under MITI's Future Electron Devices Project (1981-1990)

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New Processes

- Kyoto University--A new method (ion cluster beam sputtering) to grow an alumina insulating film on silicon substrate at 100 degrees centigrade; uniform growth achieved by ionizing the material and accelerating the charged particles onto the substrate; for use in organic transistors; project headed by Professor Isao Yamada of Kyoto's Ion Beam Engineering Experimental Laboratory

- Matsushita Electric--Method of joining materials using attraction force of atoms to create firm contact bond (interfacial attraction); oxygen and contaminants removed from surfaces by blowing argon ion gas; for use in semiconductors, and optical and large components used in nuclear fusion reactors and particle accelerators

- Sony--Two new methods for silicon single crystal growth; high oxygen density crystallization to obtain crystals with oxygen concentration 1.4 times that of Czochralski (CZ) process; enhanced version of the silicon single-crystal growth technology magnetic CZ (MCZ) developed by Sony in 1980; also a technology for raising crystals twice as fast as CZ and MCZ process; methods offer low crystal defect rate, high homogeneity, and excellent flatness

- Tokyo Institute of Technology--A new method for growing single-crystal silicon at 200 degrees centrigrade (compared to normal 800 to 1,000 degrees) for 4Mb DRAMs or larger; mercury vapor added to raw mixture and irradiated by low-pressure mercury lamp; electron mobility much lower than that of crystals developed by thermal CVD

Materials

- All megabit DRAM makers--Developing new target materials for 1Mb and 4Mb DRAMs; shifting from aluminum used in 256K to molybdenum for 1Mb DRAMs; developing low-resistance tungsten and titanium for 1Mb, titanium, niobium, and tantalum for 4Mb DRAMs

Manufacturing Processes

- Hitachi--A hybrid beam system for fine pattern ion beam processing; for use in submicron design rules; simultaneous viewing of the operation at the atomic level possible; jointly developed with Toyohashi Institute of Science and Technology; plans for commercialization in two years for 64Mb DRAMs and higher

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- Ishii Tool and Engineering/Oita Prefecture Advanced Technology Development Research Institute/Oita National Technical College--An automated IC assembly system using optical fiber sensors linking nine IC manufacturing stages; assembly time reduced from one hour to three minutes; 48 x 165cm base and 152cm tall; one-tenth the size of existing machines

- Matsushita Electron--0.1-micron pattern drawn using conventional electron beam lithography (20 to 25 kilo accelerator voltage and 0.5 to 1.0-micron thick photoresist); exposure time lengthened two to three times over normal times and special isopropyl alcohol rinse used; plans for use in fabricating X-ray masks using synchrotron orbital radiation (SOR) or high-performance GaAs devices

  - Simulation technology for sub-micron photolithography; photoresist cross section predicted by inputting exposure time, development solution density, resist type and thickness, and 16 other variables; modified version of SAMPLE simulation program developed by University of California at Berkeley; for 0.25-0.50 micron processes

- Mitsubishi--An X-ray exposure technology for 4Mb DRAM production; high-sensitivity, negative-type X-ray resist; successful test manufacturing of 3-micron VLSI

- MITI Electrotechnical Laboratory--An ultra-high precision mask/substrate alignment method using a laser beam and optical sensor; grating pattern engraved on mask and crystal base for alignment; 0.01-micron accuracy; for use in future gigabit DRAMs

Manufacturing Equipment

- Anelva--A low-pressure CVD machine for high-melting-point metal film boring (LCV641); priced at ¥53 million ($319,000) with conveying equipment and ¥39.5 million ($238,000) without conveying equipment

- JEOL Limited--An ion beam lithography system (JIBL 150) for future VLSIs; automated positioning rated at 0.1 micron; capable of ion injection and direct etching on wafer without mask; 1.0-micron design rule possible; 150KV maximum ion accelerator voltage system developed to NEC; priced at ¥1 billion ($6.5 million)

- Japan Steel Works--An experimental high-precision ion beam etcher for 16Mb DRAMs, using the electron cyclotron resonance (ECR) principle; capable of 0.2-micron design rule; orders in late 1986

- Matsushita--Etching and CVD equipment for next-generation VLSIs using technology from Nippon Telegraph and Telephone (NTT); trial runs under way and 10 units ordered

- Mitsubishi Electric--An X-ray lithography system capable of fabricating prototype 4Mb DRAMs with 0.3-micron design rule; polymethyl styrene-based resist with chloride added for increased sensitivity (8 milli-joules per square cm); poor resolution reduced by using computer to control chloride additive and swelling of the resist

  - An opto/plasma assist laser CVD machine using a high-output excimer laser, ultraviolet lamp, and plasma; capable of handling 6-inch wafers; developed jointly with Tokyo Electron (TEL)

- Nippon Telegraph and Telephone (NTT)--A prototype electron beam lithography system (EB60) capable of drawing 0.5-micron patterns; theoretical processing of 16Mb DRAMs at a rate of 20 wafers per hour; plans for in-house use before commercialization

- RHD Inc./Gakei Electric--An InPGaAs single-crystal pulling machine; testing of single-crystal wafers soon; marketing planned within two years

- Sumitomo Electric/MITI Electrotechnical Laboratory--An experimental 4.19-meter synchrotron orbital radiation (SOR) ring for use in ultra-large-scale ICs (ULSIs)

- Sumitomo Heavy--A method to develop 1-meter-diameter synchrotron radiation ring for fabrication of new VLSIs over 4Mb; single magnet approach

Packaging

- Hitachi--Super-high-density printed circuit board for megabit DRAMs featuring 50 layers of interconnect wiring in 4mm wide area; capable of accommodating up to 16Mb DRAMs; 5 to 15 times the mounting density of conventional polyimide boards; new polyimide resin offering low thermal distortion, allowing up to 50 wiring layers and 1.2mm through-hole pitch; for boards up to 64 x 50cm

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- NEC--A robot system to weld custom LSIs 0.9mm apart onto printed circuit boards; system featuring visual sensor, two robots, and laser projector; first robot for picking LSIs from tray; second robot for installation and laser welding of LSIs

- Shin Nippon Steel Chemical--A highly pure synthetic silica for ULSI packaging material; 0.1 parts per billion of uranium and thorium impurities; sol-gel process; for 1Mb and 4Mb DRAMs; new plant for annual production of 300 tons by late 1986

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COMMENTARY

The Optoelectronics Era: Ready or Not, Here It Comes

During the past few years, Dataquest has monitored MITI's Optoelectronics Project (1979 to 1986) and noted a sharp increase in new optical products, applications, and technology developments. On the applications side, 8mm video cameras, CD ROMs, fiber optics, compact disks, and laser printers have already reached the commercialization phase. On the device side, Japanese makers are pushing the performance of semiconductor lasers, CCD and MOS sensors, high-performance LEDs and photodiodes, and optoelectronic ICs. (For details, see the Optoelectronics subsection in each quarterly Technology Trends.) Recently, Japanese companies have organized the following projects that focus on next-generation optoelectronic (photonic) and video imaging technologies:

- MITI's Optocomputer Project (1986 to 1996)--Second-generation optoelectronic ICs (OEICs)
- MITI's Future Electron Devices Project (1979 to 1990)--III-V heterojunction devices and semiconductor lasers
- MPT's High-Resolution Television System (1987 to 1989)--Extended definition color TV system compatible with NTCS receivers
- NTT's Information Network System (1980 to 2000)--Fiber optics, optoelectronic ICs, semiconductor lasers, III-V materials, optical local area networks (LANs), and value-added networks (VANs)
- Japanese Industrial Robot Association's (JIRA) Robot Sensor Project (1986 to 1988)--Proximity and touch sensors
- Science and Technology Agency's (STA) Optical Measurements Technology Development Company--Optical analyzers and coherent light measuring devices
- MITI's Optical Materials Project (1987 to 1996)--Optical materials for high-output lasers and optical fibers
- Japan Key Technology Center's (MITI/MPT) Fiber Optic Communications Project (1985 to 1990 or longer)

Just as the telecommunications industry is making the shift from electrical signals to light, Dataquest believes that the semiconductor and computer technologies will follow suit in the 1990s. The impact of this shift will be enormous, comparable to the dislocations caused by the shift from transistors to silicon ICs.

Currently, U.S. and European universities and technical colleges are producing few graduates with degrees in optical engineering (BSOE/MSOE), and other than those in Japan, few companies are training people in "photonics." The only U.S. effort is the Strategic Defense Initiative (SDI), which is mainly concerned with military applications. The EEC's Research in Advanced Communications in Europe (RACE) Project is focusing on broadband communications, but only incidentally on photonics. Where will future researchers come from? Will the United States, Europe, and Asia fall behind Japan in this critical commercial technology? Dataquest believes that further discussion between the United States, Europe, Japan, and Asia is needed in this area to avoid future trade friction and national security problems.

CORPORATE R&D LABS

32-bit TRON Project

The Japan Electronic Industry Promotion Association is soliciting Japanese and foreign corporations to join the TRON Project, which is developing and standardizing a new operating system for 32-bit MPUs. Headed by Tokyo University Professor Ken Sakamura, the TRON Council has eight member companies: Fujitsu, Hitachi, Matsushita, Mitsubishi Electric, NEC, NTT, Oki Electric, and Toshiba (see Technology Trends, 2nd Quarter 1986, p. 3, for more details). Dataquest plans to issue a service section on the TRON Project soon.

Fifth-Generation Computers

Mitsubishi Electric, which was assigned to develop the personal sequential inference computer for MITI's Fifth-Generation Computer Project, is developing its second artificial intelligence computer. Called PSI-II, the computer will be three times faster, 50 percent cheaper, and have a footprint two-thirds that of its original personal sequential inference computer (PSI-I), which was announced in 1985. The PSI-II computer will use 1Mb DRAMs for its single board, compared with the 256K DRAMs used in eight circuit boards for the PSI-I. It will have an inference speed of 120 kilo logical inferences per second (LIPS). The machine will be priced around ¥10 million ($62,500).

Nippon Telegraph and Telephone, privatized in April 1985, has introduced an AI workstation with a LISP processing capability of 1,000,000 instructions per second. Called ELIS, the computer features a single-chip CPU built on a 20-kilogate LSI. The computer has 8 to 128 Mbytes of main memory, 135 to 540 Mbytes of disk storage capacity, and is two to ten times more powerful than large-scale minicomputers. The computer will sell for ¥10 million ($62,500) domestically and overseas.

IC Cards

Fujitsu, Dai-Ichi Kangyo Bank, and seven other major banks initiated the Mirai (Future) Card Project in the Tokyo metropolitan area in midsummer 1986. The two-year project will involve 1,200 users who will use the cards at 100 hotels, restaurants, department stores, travel agencies, and other businesses in downtown Tokyo. The IC card will allow cashless shopping up to the account balance, from which deductions are made by a computer terminal or ATM and immediately transmitted by public line to a jointly operated Mirai Center. Recently, an IC Card study group of 41 banks and major firms was formed to prepare for full-scale adoption of IC cards in the near future. Dataquest believes that there will be widespread adoption of IC cards in Japan by 1989 to 1990.

Optical Measurement Technology Joint R&D Company

Five Japanese measuring device manufacturers have jointly established the Optical Measurements Technology Development Company (OMTEC) to develop basic technology for measuring coherent light communications. Capitalized at ¥129 million ($806,000), the six-year, ¥4.29 billion ($26.8 million) project is financed by the Basic Technology Research Promotion Center. The project aims to develop an optical synthesizer-sweeper, an optical network analyzer, an optical spectrum analyzer, and other coherent-light measuring devices by March 1992.

The new company, located in Tokyo, is headed by Shozo Yokogawa of the Yokogawa Hokushin Electric Corporation. Participating companies include Advantest, Ando Electric, Anritsu, Iwatsu Electric, and Yokogawa Hokushin.

Automated Translation Systems

Fujitsu and the Electric Power Industry Central Research Institute are jointly developing an automated translation system for documents related to electric power generation. The project will proceed in two phases:

- Phase I (1987)--Develop an English-Japanese automatic translation system based on Fujitsu's Atlas I automated translation system, a dictionary to translate titles, and a more advanced dictionary for detailed documents
- Phase II (1988 to 1990)--Develop an English-Japanese automated translation system based on Fujitsu's Atlas II

Chemitronics

Recently, chemical and synthetic fiber companies have diversified into a new hybrid field, chemitronics, which aims at developing new chemicals and materials for electronic products. Much attention is focused on semiconductor packaging materials, optical fibers and disks, photoresists, and various films. According to a report entitled "Fundamental Vision of the 21st Century Industrial Society," by MITI's Industrial Structure Council, the new materials market will become a ¥58 trillion ($363 billion) industry by the year 2000. Dataquest notes that major Japanese chemical companies are diversifying into the following electronics products and materials:

- Asahi Chemical--Hall elements, dry film resists, optical disks, fine pattern coils, nuclear magnetic resonance CRTs, ICs (with Hitachi), and organic photoconductor drums
- Hitachi Chemical--Power distribution boards and parts, semiconductor parts, insulating sheets and varnish, and electromagnetic wave shielding material
- Mitsubishi Chemical--Organic photoconductors, transparent electroconductive film, color liquid crystal coloring material, floppy and rigid disks, and printed circuit boards
- Shin-Etsu Chemical--Semiconductor wafers and silicon, gadolinium gallium garnet (GGG), synthetic quartz, rare earth magnets, mask substrates, and IC packaging materials

- Teijin--Magnetic film, floppy disks, transparent electro-conductive film, electroconductive fiber, compact disk films

- Toray Industries--Magnetic film, microconnectors, IC film carriers, electron beam resists, transparent electroconductive films, and floppy disks

Recently, many Japanese and foreign chemical companies have established R&D centers in the Tsukuba Industrial Park. We will issue a newsletter on the new Tsukuba plants and R&D centers in the future.

GOVERNMENT R&D PROJECTS

MITI Central Data Processing College

MITI and the Information Technology Promotion Agency plan to establish a central data processing college in fiscal 1987 to alleviate Japan's shortage of computer programmers. The new college will offer year-long courses to groups of 400 computer programming instructors from small technical schools and institutes throughout Japan. Currently, there are 150 data processing technical schools and institutes with 45,000 students throughout Japan, but their average pass rate is only half that of graduates of technical high schools, junior colleges, and universities.

The plans also call for selecting outstanding junior colleges and technical schools as regional data processing branch campuses. These institutions will be provided with advanced computer educational systems free of charge.

MITI Sigma Project

MITI's Sigma Project, a ¥22.8 billion ($152 million) program created to develop computer software by fiscal 1990, entered its second phase in July after releasing the "Vo Document" that officially defines the content of the Sigma operating system. The UNIX-based system, which will be supported by Japanese language code as defined by the Japanese UNIX Council, consists of a basic section, multiwindowing, and graphics. The goal of the Sigma Project is to create a nationwide network system that allows software makers to upgrade their development methods by giving them access to a national software center through inexpensive workstations. Currently, 250 companies are participating in the project; of these, 59 companies were members of the "Vo Document" working committee. The project is supervised by the Information Processing Association (IPA).

In fiscal 1987, the Sigma Center will be opened to provide users with data base and networking services. Fujitsu, Hitachi, and NEC were selected to develop subsystems for the control center. Five subsystems will be designed by the following participants:

- Network (NW)--Nippon Telegraph and Telephone (NTT)
- Data base (DB)--Hitachi
- Demonstration (Demo)--Fujitsu
- Electronic data processing (EDP)--NEC
- Development environment (KK)--Fujitsu

The DARPA Internet Protocol will be used initially as the communications protocol to link Sigma Project workstations with overseas networks, but it will eventually be replaced by the OSI protocol.

MITI Supercomputer Project

Fujitsu, a participant in MITI's Supercomputer Project, has announced a scientific supercomputer (Facom VP-30) priced at two-thirds the price of the VP-50, but with 110 MFLOPS or 80 percent of the maximum computing power. The machine has a maximum 64 megabytes of main memory, a maximum transmission speed of 96 megabytes/second, and can be connected to a maximum of 32 workstations. Fujitsu has also improved its OSIV/MSP operating system for the VP Series, expanding its standalone capabilities for the FACOM VP-30. Monthly rental is ¥30.6 million ($191,250). Recently, Fujitsu installed a VP-400 supercomputer at the Remote Computer Service Division of Recruit Company and has received requests from 20 other firms for the VP-400. Table 1 lists the number of supercomputer orders received by major producers in Japan and elsewhere recently. Currently, U.S. government attention is focused on the few orders for U.S. supercomputers received in Japan. However, we note both countries appear to reflect "buy local" purchasing patterns.

Japan's three supercomputer makers--Fujitsu, Hitachi, and NEC--have introduced the supercomputers shown in Table 2.

Table 1

SUPERCOMPUTER ORDERS RECEIVED BY MAJOR VENDORS
(July 1985 to July 1986)

	From Japan	From Elsewhere	Total
Fujitsu (VP Series)	30	14	44
Hitachi (S-810)	13	0	13
NEC (SX-2 and SX-2)	6	1	7
Cray Research (Cray)	6	134	140
Control Data (Cyber 205)	0	40	40
Total Japanese Orders	49	15	64
Total U.S. Orders	6	174	180

Source: Japan Economic Journal

Table 2

JAPANESE COMMERCIAL SUPERCOMPUTERS

Maker	Date	Model	Speed (Gflops) Announced	Optimal	Megabytes
Fujitsu	1982	VP-100	250	267	128
	1982	VP-200	500	533	256
	1985	VP-50	140	N/A	128
	1985	VP-400	1,140	N/A	256
	1986	VP-30	110	N/A	64
Hitachi	1982	S-810/10	315	400	128
	1982	S-810/20	630	800	256
	1986	S-810/5	160	N/A	128
NEC	1983	SX-1	570	570	128
	1983	SX-2	1,300	1,300	256
	1986	SX-1E	285	N/A	N/A

N/A = Not Available

Source: Dataquest
February 1986

NEC, another participant in MITI's Supercomputer Project, has entered an agreement with Honeywell Information Systems to establish a 50-50 American sales venture, Honeywell-NEC Supercomputers, to market NEC's supercomputer line in the United States. In September 1986, the venture began selling and servicing three NEC supercomputers: SX-1E (285 MFLOPS capability), SX-1 (570 MFLOPS), and SX-2 (1.3 GFLOPS). Its goal is to sell more than 50 supercomputers during the next five years. Dataquest notes that Fujitsu sells its supercomputers through Amdahl. The question is which U.S. maker Hitachi will approach.

MITI/MPT Advanced Communications Systems Project

In July, nine companies established a joint research venture, Space Communications Research, to develop next-generation telecommunications systems. The project will be funded 70 percent by the Basic Technology Research Promotion, a government organization jointly sponsored by MITI and the Ministry of Posts and Telecommunications (MPT). The new venture, budgeted at ¥10 billion ($62.5 million) over the next 10 years, plans to develop 30-meter antenna and switching systems for satellites, solid-state power amplifiers, milliwave transceivers, and 22/27-GHz communications systems. Dataquest observes that many of these systems will use GaAs MESFETS and MMICs. Participating companies include Fujitsu, Hitachi, Japan Broadcasting Company (NHK), KDD, Mitsubishi Electric, NTT, Tokyo Electric Power, Toshiba, and Toyota Motors.

MPT Automated Translation Telephone

The Council for the Promotion of Automated Translation Telephone Systems Development recently issued a report to the Ministry of Posts and Telecommunications outlining the costs and system hardware for automated translation telephones. According to the council, a prototype system with limited language skills can be developed within 15 years at a cost of ¥90 billion ($563 million). The program will have the following development goals:

- 1991--Simulation model with 2,000-word vocabulary and limited grammar and enunciation capabilities
- 1996--Slow automatic translation system with 3,000-word vocabulary and capability of being used as international telephone operators
- 2001--Moderately fast automatic translation system with 10,000-word vocabulary
- 2006+--Ultimate system with 3 million-word vocabulary for handling routine telephone conversations

The translation telephone will feature a TV camera (probably CCD sensor based), monitor, and readout to display the time, day, and country of call destination. The Japanese government plans to cooperate with the United States and European countries to develop the system. Dataquest notes two developments related to the automated translation telephone project:

- In 1986, eight Japanese computer makers formed a joint venture company, the Japan Electronic Dictionary Research Center, to develop a 900,000-word dictionary for fifth-generation computers. The company will be headquartered at MITI's Institute for New Generation Computer Technology (ICOT). (See Technology Trends, 1st Quarter 1986, p. 9, or 2nd Quarter 1986, p. 10).

- The Japan Information Center of Science and Technology (JICST), which launched a four-year project to develop a Japanese-English translation machine, has abandoned the LISP language in favor of C language in order to accelerate the translation speed from 5,000 words per hour to 30,000 words per hour.

MITI Optical Materials Project

In fiscal 1987, MITI will allocate ¥15 billion ($94 million) to an 8- to 10-year project to develop new glass materials for high-output lasers and long-distance optical fibers with low transmission loss. Dataquest observes that this project will support the new Optical Technology R&D Corporation, which will focus on second-generation optoelectronic ICs for optocomputers and optical communications (see Technology Trends, 2nd Quarter 1986, p. 9).

NEW PRODUCTS AND TECHNOLOGY TRENDS

Memory

- Fujitsu--A 4Mb DRAM using three-dimensional stacked capacitance cell structure used in 1Mb DRAMs; 0.8-micron design rule; trench method used by Matsushita, Mitsubishi, NEC, Texas Instruments, and Toshiba; Fujitsu to develop both methods for 4Mb DRAMs

- A 1Mb CMOS DRAM; 1Mbx1 and 256Kx4 structure; high-speed page and nibble mode; 1024-bit serial access mode; 100/120/150ns access times; 180/210/260ns cycle times; 85/75/65mA power consumption during operation; 21.8 square micron NMOS memory cell; 11.85 x 4.19mm chip; plans for four types; CMOS versions also by Hitachi, Mitsubishi, Oki Electric, and TI Japan

- A Hi-BiCMOS 64K ECL RAM (HM10494LCG); 20/25ns access time; 500mW power dissipation during operation; priced at ¥9,000 ($58) in 10,000-unit lots

- Two 16K ECL RAMs (MBM10484A); 10ns maximum address access time and 5ns maximum chip select access time; -5.2 and -4.5 volt power supply models; 4Kx4-bit structure; 1.0-micron design rule; Fujitsu's proprietary U-shaped isolation method (IOP-II); 70,000 elements on a 5.5 x 3.8mm chip; 1.35-watt maximum power consumption for 10K series (MBM10484A-10) and 1.17 watts for 100K series (MBM10048A-10); 28-pin packages, including small outline flat package (SOP), leadless chip carrier (LCC), and 400-mil DIP; sampling at ¥13,000 ($81.25)

- 64K and 72K high-speed SRAMs; 35ns access time; 8Kx8-bit model (MB81C78A) and 8Kx9-bit model (MB81C79A); sampling at ¥5,000 ($31.25) for 35ns model and ¥4,500 ($28.13) for 45ns model; 28-pin DIP or SOP

- Two dual-port NMOS 16K SRAMs (MB8421/MB8422) suitable as common memories in multiprocessing; 120ns access time; left and right ports share the same 16-bit memory cell array; 90ns cycle time; 120mA power consumption during operation; 52-pin shrink DIP package; sampling at ¥4,000 ($25)

- A CMOS 256K SRAM (MB81C81) with a 45/55ns maximum access time; 256Kx1-bit organization; 5.0 x 11.3mm chip; 550mW power consumption during operation and 83mW at standby; 300-mil, 24-pin ceramic DIP package; sampling since November at ¥18,000 ($112.50); plans for a 35ns part by early 1987

- 2K bipolar PROMs; 256x8-bit structure; 25ns maximum access time for MB7118Y; 30ns for MB7118EW; 3-micron design rule; temperature range of -55 to 125°C; 20-pin DIP and LCC; sampling at ¥1,000 ($6.25) for 7118Y and ¥1,500 ($9.38) for 7118EW

- Two 4K bipolar RAMs (MBM10474A-5/7 and MBM10047A-5/7) featuring 1.0-micron rule and U-FOX process (a new technology combining U-shaped isolation technique and a thickened field oxide membrane); work as wired OR circuit in open emitters; ECL I/O interface and internal circuits; 10K and 100K RAM I/O interface types; 5ns access time at -5.2V power voltage and 300mA power current; sampling at ¥8,000 ($50)

- Three 256K CMOS DRAMs with static column mode high-speed operation; 256Kx1-bit (MB81C258) and 64Kx4-bit structure (MB81C466); 4.2 x 9.7mm chip; 100/120/150ns access times, increasing to 45/55/70ns in static column mode; 0.3mA power consumption at standby; 16-pin plastic DIP, 18-pin PLCC (MB81C258), 18-pin plastic DIP and 20-pin ZIP packages; sampling at ¥3,000 ($18.75); volume production of 200,000 to 300,000 monthly since November

- Hitachi--A 64K ECL 10K I/O RAM (HM1049LCG); 16Kx4-bit structure; Hi-BiCMOS process; 20/25ns maximum address access time; 500mW action mode power consumption; highly resistant load NMOS memory cell; Hi-BiCMOS hybrid gate circuit for peripheral circuit; bipolar ECL input/output circuit; 28-pin LCC package; sampling at ¥15,000 ($93.75) or ¥9,000 ($56.25) for 10,000-lot orders

  - A 16K ECL RAM using 1.3-micron Hi-BiCMOS technology; 7ns access time; 350mW power consumption; 16Kx1-bit structure; ECL-level I/O interface; 104-square-micron memory cell; 2.3 x 3.7mm chip

  - Three 1Mb CMOS DRAMs; 100/120/150ns access times; 1Mbx1-bit and 236Kx4-bit structures; 330/275/220mW power consumption during operation; page mode (HM511000), nibble mode (HM5110001), and static column mode (HM511002); 512 refresh cycles/8 microseconds; small outline J-bend (SOJ) package

  - A 16K CMOS static video line memory; 2,048x8-bit structure; five types of access modes: 1H/1H delay mode, time compression/expansion mode, TBC mode, delay line mode; 300-mil package; 28-pin DIP; NTSC and PAL methods; 1.3-micron rule; 28ns cycle time for data input/output

- Matsushita--Three 256K CMOS EPROM (M5M27C256K); 120/150/250ns access times; 4-MHz operating current; 30mA power consumption during operation; 5.43 x 5.41mm chip; silicon channel process; 28-pin, 15.2mm-wide DIP; 120ns-type priced at ¥3,000 ($18.75) and 250ns-type at ¥4,000 ($25)

- Mitsubishi Electric--Three 256K CMOS EPROMs; 120/150/250ns access times; 1.5-micron design rule; 5.43 x 5.41 mm chip, or 6 percent smaller than Mitsubishi's 128K CMOS EPROM; 120ns device priced at ¥3,000 ($18.75)

  - A prototype 4Mb DRAM; 0.8-micron design rule; 9 million transistors on a 5mm-square chip; plans for mass production in 1989

  - A 1K CMOS EEPROM (M34300N-SP) featuring a 4-bit, single-chip MCU (M50720); five D/A converters and one 3-bit A/D converter; for use in television and VTR screens and graphic terminals; 4K x 9-bit mask ROM; 128 x 4-bit RAM; 42-pin shrink DIP; sampling from February 1987

- NEC--Two CMOS video DRAMs (MuPD42505C) capable of reading and storing 5K x 8 bits of information (equal to a single line on an A4 size text) one line at a time; 50/75ns cycle times; 12.48 x 3.6mm chip; high-speed serial access memory with memory cells arranged serially; 50ns write-in, readout cycle; optional features include image data extension or compression, image quality improvement, contour line enhancement, or data transfer speed changes; 660mW power consumption during operation; 300-mil DIP; sampling at ¥7,000 ($43.75) for 50ns device and ¥5,000 ($31.25) for 75ns device

  - A 256K SRAM (uPD43257) featuring two-chip signal selection for memory control and a RAM control system adaptable to battery backup; sampling since August at ¥6,000 ($37.50); monthly production of 200,000 to 300,000 by early 1987

  - A CMOS 256K first-in first out (FIFO) DRAM (MuPD42532C); 32Kx8-bit organization; 1.2-micron process; 7.14 x 8.05mm chip; double buffer structured read-write data register that allows simultaneous read-write operations; 100ns cycle time and 50ns access time; 600-mil, 40-pin device; used as a buffer to facilitate data flow between systems with different processing speeds; one-third to one-fifth the price of equivalent SRAM boards; for G4 facsimiles; sampling at ¥10,000 ($62.50)

  - Three 1Mb CMOS UV EPROMs (MuPD27C1024D); 64K x 16-bit; 150/200/250ns access times; 0.5ms/byte program time; power consumption of 50mA during operation and 100mA at standby

- Two 64K CMOS EEPROMs (MuPD28C64) with 32-byte write-in capability; 250/300ns access times; 8Kx8-bit structure; 50mA power consumption during operation; error correction checking function; 32-byte maximum page write-in mode; for use in musical instruments, programmable controllers, facsimiles, phones, and IC cards; 28-pin 15.2mm ceramic DIP; 250ns type sampling at ¥4,000 ($25)

- Two CMOS 8K EEPROMs featuring error-correction circuits, data polling function, page write mode up to 32 bytes, and error writing protection; sampling at ¥4,000 ($25) for 250ns model and ¥3,600 ($22.50) for 300ns model; target production run of 50,000 monthly

- Six 1Mb CMOS mask ROMs; two 200/250ns, 28-pin devices available commercially (MuPD23C000C/D series); four devices under development: 120ns/28-pin device with output enable (MuPD23C1010C/D), 200ns/28-pin device with page access (MuPD23C1011C/D), 200ns/40-pin device (MuPD23C1024EC/D), and 2-microsec/28-pin with access mask option (MuPD731002C)

- Two 1.2Mb NMOS mask ROMs; 250ns access time; 40-pin; 24 x 24-dot kanji character function (MuPD231200C/D and MuPD2312001C/D)

- Three 2Mb CMOS mask ROMs; two commercially available, including 250ns/40-pin device with 8/16-bit output selection (MuPD23C2000C/D) and 125ns/28-pin device with address/data registers (MuPD732008C/D); one device under development: 250ns/32-pin with JEDEC standard pin layout (MuPD23C2001C/D)

- A 32 x 8-bit FIFO DRAM (MuPD42532C) for G4 facsimile; 40-pin DIP package; 100ns cycle time; 5.6- x 11.3-micron memory cell; 7.14 x 8.05mm chip size

- Seiko--Three CMOS nonvolatile RAMs; 256-bit organized 64x4 (S-2210R); 1K organized 256x4 (S-2212R); 256-bit organized 16x16 (S-2444R); 18-pin DIP for S-2210R/12R; 8-pin DIP for S-2444R

- Sony--Two 256K SRAMs; 100/120ns access times; 32Kx8-bit structure; 40mW power consumption during operation; 28-pin DIP and multiflat pack; sampling at ¥4,000 ($25)

  - Two 64K SRAMs; 8Kx8-bit structure; sampling at ¥1,200 ($7.50) and ¥600 ($3.75) for 70ns and 100ns parts, respectively

- Two 16K SRAMs; 2Kx8-bit and 4Kx4-bit structure; 35ns access time; prices range from ¥1,100 ($6.87) to ¥600 ($3.75)

- Sharp--A 4Mb CMOS mask ROM (LH534000); 512Kx8-bit and 256Kx16-bit organizations; 200ns access time; 50mA power consumption; sampling from December

  - A 2Mb CMOS mask ROM (LH532000); 200ns access time; 1.2-micron design rule and tungsten silicide process; 256Kx8-bit or 128Kx16-bit structures; 35mA power consumption; sampling since October at ¥2,400 ($15)

  - 256K CMOS EPROMs with 32Kx8-bit structure (LH57256J); 128K CMOS EPROMs with 16Kx8-bit structure (LH57128J); 64K CMOS EPROMs with 8Kx8-bit structure (LH5764J); 28-pin DIP; 200/250/300/450ns access times; 165mW power consumption

Memory Modules

- Taiyo Yuden--Multilayered ceramic substrate board for 4Mb to 8Mb memory modules; board can be sintered at 900 to 1,000°C, allowing simultaneous sintering of paste material for resistors, capacitors, and inductors; thermal expansion coefficient same as that of monocrystal silicon, enabling the use of inexpensive copper wiring; 4Mb modules since September and 8Mb modules from December 1986; 8Mb modules sampling at ¥40,000 ($250)

- Toyo Data--An 8-Mbyte VME bus memory board (TVME-220); 72 1Mb DRAMs (TC511000P-12)

- Toyo Telecommunications--A SIP 1Mbx1-bit memory module (TH310009); 1Mb DRAMs in SOJ package (MuPD411000); 1Mbx1-bit structure (Th310008); 64Kx4-bit dual-port DRAM memory (MB81461) and 16Kx16-bit memory (TH3D2564/TH2D2564); ZIP package

IC Cards

- Marubeni Hytech--A memory card with 512K CMOS SRAM and 8Mb mask ROM; 46 x 80mm card; ISO standard 3mm thickness; capable of retaining data for five years in four 64K CMOS SRAM units; 26g weight; sales from October

- Oki Electric--A one-chip CMOS 8-bit MCU with built-in 16K EEPROM for IC cards (MSM61580); 5.0 x 4.5 mm chip; 3 Kbytes of programmable ROM and 512 bytes of ROM; 4.9-MHz clock frequency; 813.8ns execution time; 95-instruction capacity; jointly developed with Catalyst Semiconductor; priced at ¥1,200 ($7.50) in 100,000-lot orders

- Seiko Epson/Toppan Printing/Fujita Corp.--A portable IC card system (IC Card Handy Terminal System) consisting of Seiko Epson's HC-10 portable computer terminal and a small card reader/writer; 16K and 64K EEPROM (plus MCU) cards; Toppan responsible for writing the basic program; Fujitsu planning an experiment at its Tokyo and Chiba construction sites for management of workers' hours, health care, and personnel management

- Toshiba--A Super Smart Card developed with Visa International; one-chip featuring an 8-bit CMOS MCU and 16-Kbyte mask ROM; UART also planned; prototype by summer or fall 1987; ISO standard 0.76mm thickness; magnetic pattern generation circuit

- Towa Electron--Two ISO-standard memory cards; version with 8 Kbytes of EEPROM priced at ¥9,000 ($56.25); version with 32 Kbytes of SRAM priced at ¥12,000 ($75); 160 x 85 x 20 mm size; 1.3mm thickness; reader/writer interface (RS-232-C); 1200- to 19,200-bits/sec transmission; sampling at ¥35,000 ($218)

Microprocessors/Microcontrollers

- Fujitsu--A proprietary high-speed real-time processing 8-bit MPU for ASIC applications; 8-bit external data bus and 16-bit internal bus; 0.33-microsecond minimum instruction execution time; A/D, D/A converters, LCD driver, RAM and ROM peripherals included, with plans for memory, I/O circuits, software, development tools

  - A CMOS 4-bit MCU with 8-bit A/D converter (MB88511); 48-microsecond A/D conversion speed at 6 MHz; four-channel analog input; 4 Kbytes of ROM and 256x4-bit RAM internal memory; 42-pin plastic DIP and shrink DIP or 48-pin flat package; sampling at ¥800 ($5)

  - A CPU core for the CMOS 8-bit flexible MCU series (MB89700 Series); jointly developed by Fujitsu Ltd. and Fujitsu Micon Systems

- An 8-bit video signal A/D converter (MB40578) capable of processing video signals at 30 million samples per second; output compatible in TTL level; 480mW power consumption during operation; parallel comparison-type, bipolar IC technology; for use in digital TVs, VTRs, and medical equipment; 300-mil, 22-pin DIP package; sampling at ¥4,000 ($24.80) since September

- A single-chip, 4-bit MCU (MB88549) incorporating LCD controller and driver circuits; all four models featuring 4 Kbytes of ROM and 256x4 bits of RAM; serial transmission and reception of 8-bit data; 2.86- to 2.0-microsecond minimum command execution time; low-frequency clock generator; sampling at ¥700 ($4.38)

- Two CMOS 4-bit MCUs with built-in A/D converters (high-speed sequential comparison type with 8-bit resolution)

- Hitachi--A CMOS floppy disk controller (HD63265P) featuring an adjustment-free analog VFO circuit and write precompensation circuit; VFO circuit generates a clock for reading drive data from 3- to 8-inch drives; 48-pin DIP package; priced at ¥2,900 ($18.13) each or ¥1,750 ($10.93) in 10,000-lot orders

  - A dual universal serial communications controller (HD68562); second-source product of Signetics; priced at ¥8,500 ($53.13) each or ¥4,900 ($30.63) for 1,000-unit lots

- Matsushita--A digital servo signal LSI processor for VTRs (MN6745) that integrates functions of a servo main, cylinder interface, and capstan interface; sampling at ¥1,000 ($6.25)

  - A single-chip CMOS MCU (MN158452) incorporating 4K ROM, 256-word RAM, a clock frequency divider circuit, an 8-bit preset counter, and an LCD drive circuit; built-in programmer possible for VTR remote control handsets

  - A single-chip, 16-bit MCU (68070) for use in home automation systems; software compatible with Motorola's 68000; jointly developed with Signetics and Philips

- Mitsubishi--An original 16-bit, single-chip CMOS MPU series (M31600M2) and 8-bit series (M50960); production at new Kochi plant

- NEC--A CRT controller (MuPD72022) capable of compressing 640- x 512-line screens into 256x256 format for character display, pop-up menus, and multiwindow displays; 16 colors; 21-MHz bit rate; NTSC and PAL signals

- NTT--A 1-bit pseudo-MIMD (multiple instruction stream/multiple data stream) array processor with 65,536 processing elements; SIMD structure (single instruction stream/multiple data stream); 1.5-micron CMOS process; 104,900 transistors; 100ns machine cycle time

- Oki Electric--World's smallest CMOS 8-bit single-chip with a self-contained 16K CMOS EEPROM; 5.0 x 4.5mm chip; 4.9-MHz clock frequency; 813.8ns execution command time; 3-Kbyte program ROM capacity; 512-byte ROM; internal testing and 95 EEPROM control programs, providing optimum architecture for IC cards

- Rohm--Two CMOS single-chip 4-bit MCU series with 42 devices with internal 512x8-bit ROM and 16x4-bit RAM; 1-MHz version (BU2405L) and 4-MHz version (BU2405); 43 devices with 1024x8-bit ROM and 64x4-bit RAM; 1-MHz version (BU2400) and 4-MHz version (BU2400L)

  - An NMOS single-chip, 8-bit MCU series (BU13870) with internal 2048x8-bit ROM and 64x8-bit RAM; 1 to 4 MHz; 76 devices; TTL-level compatible; 32-bit I/O ports

- Sharp--Two CMOS 8-bit high-speed MPU series; 12-MHz external clock frequency; SM803A/AM/AU models with built-in 4-Kbyte ROMs priced at ¥2,500 ($15.63); LU800AV1/AVM/AVU ROMless types at ¥2,200 ($13.75); 40-pin DIP, 44-pin flat package, and 44-pin PLCC; monthly production targeted at 60,000

Digital Signal Processors (DSPs)

Recently, Japanese companies have developed digital signal processors, focusing on image and video processing. Table 3 lists the fixed-point DSP devices available worldwide.

Color television digital signal processors are also being introduced in Japan, as shown in Table 4.

- Fujitsu--A general-purpose digital signal processor (CS86-22) for Integrated Service Digital Network (ISDN) transmission terminals; 9.3 x 10.2mm device that replaces 100 ICs; 2-micron CMOS process; capable of handling two B channels (64 Kbits/sec) and one D channel (16 Kbits/sec); compact ISDN terminals can be designed by combining new device with an MPU; 9,800-gate CMOS structure capable of outputting voice, image, and data signals and dividing incoming information into separate signals for voice and data; four I/O ports with 384-Kbit/sec transmission capacity of any combination of incoming transmission volumes; 256 Kbytes of RAM, 286 bytes of ROM, and 4,096 bytes of programmable ROM

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- Hitachi--A floating-point DSP chip (HD61811) with instruction ROM changed into RAM; 128- x 16-bit RAM; 512- x 22-bit instruction RAM; 200- x 16-bit data RAM; 250ns machine cycle time; 750mW power consumption; 3-micron CMOS process; 68-pin PGA; sampling at ¥60,000 ($375) or ¥28,000 ($175) for 10,000-unit orders

- Nippon Telegraph and Telephone (NTT)--A 1.56Gb/sec parallel switching DSP LSI; 8-channel I/O; nine parallel shift registers; 1-micron-rule bipolar process (SST-1A); 1,000 gates; 2.5 x 3.1mm chip size; 1.09W power consumption

- Oki Electric--A 22-bit CMOS digital signal processor (M6992) with 20-megaflop arithmetic capability; 2-micron rule; 132-pin package including a 256x22-bit RAM and 1,024x32-bit ROM; 100ns delay time; internal and external memory accessible within one instruction cycle at transfer rate of 10 million words per second

- Sony--Eight LSIs for compact disk players, including three digital signal processors, a servo signal processor, a PWM driver, a 16-bit D/A converter, and a 13-bit D/A converter; pulse number modulation (PNM) method; prices range from ¥400 ($2.50) to ¥3,400 ($22)

- Toshiba--A circuit (TC9019N) for switching image and voice signals; capable of selecting signals from image input terminals for VTRs and video disks, 21-pin analog RGB videotex terminals, and 8-pin digital RGB personal computer terminals; one-fourth the size of discrete circuits; sampling at ¥500 ($3.12)

- Yamaha--An 18-bit signal processing LSI for CD players; capable of processing CD signals at 16 times higher resolution than conventional methods

Table 3

MAJOR FIXED-POINT DIGITAL SIGNAL PROCESSORS

Company	Bits	Cycle	Memory	Instruction	Process	Date
Analog Devices	16	125	None	16x24 ROM	1.5 m CMOS	1986
AT&T Labs	24+8	250	512x32 RAM	512x32 ROM	1.5 m CMOS	N/A
Fujitsu	16	100	128x16 RAM	1Kx24 ROM	2.3 m CMOS	4/83
Hitachi	12+4	250	200x16 RAM 128x16 ROM	512x22 ROM	3.0 m CMOS	5/82
ITT	16	100	440x16 RAM 72x16 ROM	1Kx16 ROM	CMOS	N/A
Matsushita	16/24	250	66x6 RAM	2Kx32 ROM	2 m CMOS Al	11/85
Motorola	24	97.6	256x24 RAM	2Kx24 ROM	1.25 to 1.5 m CMOS	1987
National	16	100	None	None	2.0 m CMOS	1987
NEC	24+8	150	512x32 RAM 1Kx32 ROM	512x32 ROM	1.5 m CMOS	8/86
NTT	12+6	50	512x18 RAM	4Kx32 ROM	1.2 m CMOS	1986
Oki Electric	16+6	100	128x22 RAM	1Kx32 ROM	2.0 m CMOS	5/86
Philips	16	125	128x16 RAM 512x16 ROM	992x40 ROM	2.0 m CMOS	1986/ 1987
Ricoh	16	300	256x16 RAM 128x16 ROM	512x8 ROM	3 m NMOS	1983
Texas Instruments	16	100	256x16 RAM 288x16 ROM	4Kx16 ROM	1.3 m CMOS	8/86
Thomson CSF	16	160	128x16 RAM 512x16 ROM	1280x32 ROM	2.0 m NMOS	1986

N/A = Not Available

Source: Nikkei Electronics
Dataquest
February 1987

Table 4

COLOR TELEVISION DSP DEVICES

Company	Product	Pins	Analog Circuits	Digital Gates	Chip Size	Date
Matsushita	AN5155	150	1,550	150	4.9 x 3.9mm	1/85
Mitsubishi	M51307	52	1,400	43	4.2 x 4.0mm	10/84
Tokyo Sanyo	LA7650	42	1,900	400	4.5 x 4.6mm	6/86
Toshiba	TA7777	64	2,300	250	5.3 x 4.3mm	12/84
Toshiba	TC9019N	42	N/A	N/A	N/A	8/86

N/A = Not Available

Source: Dataquest
February 1987

Application-Specific ICs (ASICs)

- Fujitsu--Japan's first silicon compiler for automatically designing custom ICs, such as RAMs, ROMs, multipliers/adders, and digital signal processors; design time shortened from four months to one day; user designates the number and configuration of bits; compiler capable of handling up to 32x32-bit multiplication/addition chips, 32K RAMs, and 128K ROMs

  - A standard cell library incorporating proprietary 4-bit and 8-bit MPUs

- Hitachi--A Hi-BiCMOS gate array series (HG28 series); 630/864/1008/1326/1800/2550 gates

- NEC--A 3,000-gate GaAs array; 7.5 x 7.4mm chip consisting of 3,000 basic cells forming one diode and seven FETs; 56ps no-load gate delay time, or 180ps with 2mm wiring attached; twice as fast as ECL gate arrays, but one-third the power consumption; plans to commercialize ECL-compatible device; result of MITI's Supercomputer Project

- Oki Electric--A standard cell library incorporating original 4-bit MPUs

- Ricoh--Two CMOS electrically programmable logic (EPLD) series; Group 1 includes four AND-OR/XOR arrays: a 10-input/8-output (10P8-A/B), 12-input/6-output (12P6-A/B), 14-input, 4-output (14P4-A/B), 16-input, 2-output (16P2-A/B); Group 2 includes three arrays: 10-input/6-output (16P8-B), 8-input, 8-foldback, 8-output, 8-register (16RP8-B), 8-output, 6-foldback, 6-register (16RP6-B), and 8-input 4-foldback 4-register (16RP4-B)

- Rohm--A CMOS gate array series (BU1200 Series); 156-3,025 gates; 5V power supply; 3ns gate delay; CMOS/TTL I/O level; DIP, shrink DIP, and quad flat packages; 16-100 pins

- Yamaha--A standard cell library, including RAM, ROM, and analog circuits; YIS-Logic System on a personal CAD for timing simulation, automatic layout programming, and interface

CAD Systems

- Nippon Telegraph and Telephone--An LSI design support system capable of designing logic circuits quickly and cheaply by connecting personal computers to a scientific calculation on-line service called DEMOS-E; NEC PC-9800 series used as system terminal and Data I/O Japan's DASH-2 as software for inputting logic circuits; priced at ¥4.5 million ($28,125)

- Toshiba--An integrated VLSI simulation system designed to handle VLSIs up to 64Mb memories; capable of modeling the device shape and forecasting its electric characteristics after the mask data and fabrication process are input into the computer; device displayed at each fabrication stage, including a layout processor, shape simulator, ion implantation and diffusion simulator; simulation task performed in one to two hours (versus one to two days using single-function simulators); plans for using the system at Toshiba's new Electronic Engineering Center in Kawasaki, Kanagawa prefecture, from March 1987

Optoelectronics

- Citizen Electronics--A LED lamp (CITILED); 3.2 x 2.5mm chip; two LEDs in one-lamp unit

- Fujitsu--A high-speed PIN photodiode ten times faster than conventional photodiodes; 10 billion optical pulses converted into electrical pulses per second; produced using vapor phase epitaxy and argon ion beam etching techniques; N-type layer of doped InP, I-type insulating layer of slightly doped GaInAs, and P-type layer of InP diffused with some zinc; for future optical fiber networks

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- Furukawa Electric--An indium semiconductor laser developed using MOCVD process; indium ring and InGaAs ring layered onto indium substrate; for optical communications

- Hitachi--1.3-micron and 1.55-micron band InGaAs photodiodes; 100- and 300-micron devices for monitoring laser diode output; 3mm device for measuring instruments; 50- to 300-micron devices sampled since September for ¥28,000 ($175); 3mm devices sampling at ¥200,000 ($1,290)

  - A 1.55-micron InGaAsP distributed feedback laser (HL1541) with 5mW output; 1.2 Gbit/sec transmission; 100 to 200km transmission capability

- Kodenshi--A photo interrupter series (Photo Interrupter LG Series) developed using a GaAs LED and photo IC

- Matsushita/Fujitsu--Claims world's first high-output 800-MHz AlGaAs semiconductor laser featuring an optoelectronic IC (OEIC) that consists of a laser diode and noise canceller circuit on a single chip (called a laser noise canceller monolithic chip); 0.35 x 1.2mm device integrating an AlGaAs laser diode, 25 MESFETs, and 18 diodes; 830nm wavelength light with 30mW output during writing and 5mW during reading; U-shaped groove 10 microns deep and 400 microns wide; internal high-frequency circuit designed to reduce noise and data readout errors caused by the reflection of laser light; suitable for pickup subsystems in erasable optical disk systems; commercialization planned within two years

  - A monolithic two-beam GaAlAs laser array for read-write optical disk applications, capable of oscillating two kinds of laser optical output on a single chip; for use in compact optical pickup for optical disk systems

  - An InGaAsP heterostructure laser for optical switching; 1.3-micron wavelength; 13.7mA power current; 200ps (on)/430ps (down time)

  - An ultraviolet lamp annealing (IRTA) method for drawing FETs onto 2-inch gallium substrates to develop 1K/4K/16K GaAs SRAMs

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- Mitsubishi--An AlGa-GaAs semiconductor laser capable of double-wavelength oscillation; 843nm laser beam at 150 mA and 803nm at 890mA, corresponding to the minimum and maximum energy levels of alternately stacked quantum well structure of 48 alternate layers of doped AlAs and GaAs; an inner GaAs light-generating layer (10nm thick by 410nm wide) sandwiched by AlAs layers; light brightness to be enhanced for use in simplifying optical systems in optical disk players, optical sensors, and multiplex wavelength optical communications

- Mitsubishi Corp./Nisshin Steel/Toyo Ink--A method for growing zinc selenide monocrystals for blue LEDs; 26cm long x 5cm-diameter wide crystals grown in one day using Bridgeman method; for use in flat-color televisions and displays, long-distance laser communication systems, and space communications

- NEC--A prototype high-output InP FET for microwave and milliwave communications; InP device 1.5 times the electron speed of available GaAs FETs and superior thermal conductivity; ion implantation method used to form a layer where electron flows within the InP substrate, an AlGaAs crystal in the interface of the layer and the substrate as an insulation gate; extremely stable FET with 8.3dB gain at 12 GHz and 1-micron gate length; commercial device to be developed with submicron gate length; plans for commercial-quality 30- to 40-GHz devices by 1987 for satellite communications systems

  - A crosstalk 15dB, 8 x 8 matrix optical switch; 6.5 to 8.0dB transmission loss; 10 x 64 x 0.8mm device; 2.2mm width electrode; lithium niobate trioxide

  - An experimental 1.55-micron bandwidth, single-mode wavelength semiconductor laser capable of transmitting data 50km+ through quartz optical fibers

  - Two single-mode distributional feedback (DFB) lasers; 8mW output; 1.3-micron band featuring 1.0-Gbps transfer rate and 80 to 100km transmission distance (NDL5600); 1.55-micron band featuring 1.0-Gbps transfer rate, and 100 to 200km transmission; double-channel planar buried heterostructure (DFB-DC-PHB) method; 1.3-micron band (NDL5600) priced at ¥450,000 ($2,813); 1.55-micron band (NDL5650) priced at ¥550,000 ($3,438)

- NTT--An InGaAsP LED capable of transmitting 32 Mbits/second or 800 Kbits/sec of data up to 2km without a repeater; 0.86- x 0.73-micron device

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- Sanken Electric--Two LEDs; a high-brightness GaAlAs LED (SEL1615 series) with 1,000 millicandelas of light at 20mA; a high-density contact mounting type (SEL3000 Series) directly mountable onto a PC board; for use in car stereos and telephone equipment

- Sharp--A low-noise semiconductor laser (LT022PD) driven by a single positive power supply and 5V+ single-power supply laser driver IC (IR30C07/07N); laser priced at ¥2,500 ($15.63) and driver IC at ¥150 ($0.94)

- Showa Electric--Claims world's first ultrasonic sono-coupler (elements that connect digital and analog circuits by ultrasonic waves) for future use in compact disk players and digital audio tape recorders, replacing photocouplers

- Tateishi Electric--A semiconductor laser using spectral pattern processing; 780nm wavelength; 0.01-100m/sec measurement possible

- Toshiba--An ultrasmall semiconductor laser compatible with standard Sharp and Sony models; low noise through use of Toshiba's new ISSS technology (inner stripe square-channel substrate); sampling since September at ¥2,500 ($15.63); other smaller laser makers include Hitachi, Matsushita, and Mitsubishi

  - Two infrared LEDs for camera autofocus use; high output at 1.75W voltage using a spherical lens bound with epoxy resin to the LED; 250-micron spot diameter and 14mW light output for TLN206 model; 380 microns, 15mW with TLN216 model; GaAs active layer sandwiched between GaAlAs layers; sampling at ¥300 ($1.86)

  - Three high-output LEDs featuring a forward current IF of 30mA and light-emitting peak wavelength of 660nm; TO-19 dimensions for TLRC280 model priced at ¥700 ($4.38); TO-92 dimensions for TLRC281 model priced at (¥400 ($2.50); TLRA281 priced at ¥750 ($4.69)

  - An AlGaAs distributed feedback (DFB) semiconductor laser; 767nm wavelength; 270mA current; proprietary VSIS structure; for use in optical disks and measuring equipment

  - A high-conversion efficiency PIN photodiode (TPS721) for use as a light-detecting and light-emitting device for plastic optical fibers; 2.0mm-diameter light detector; 0.4A/W conversion rate possible for 1mm diameter fibers; 200-MHz cutoff frequency; 0.5nA dark current

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Image Sensors

- Hitachi--A MOS-type, PAL method TSL (transversal signal line) solid-state image pickup device to eliminate smear in video cameras to be shipped to Europe; 349,000 (600 x 582) pixels; 576 x 575 effective pixels; vertical and horizontal switching device for each pixel and a common line for horizontal pixels to read out signals horizontally; high resolution of 360 horizontal television lines x 420 vertical lines; high sensitivity of 10 lux; 5V power supply; 5.53-MHz frequency; specialized driver IC (HD62990) provided for sensor; sampling at ¥25,000 ($156.25)

- Matsushita Electronics--A CCD image sensor (MN3656) featuring a 77mm reading width and resolution of 400 lines per inch; a contact-type image sensor for compact facsimile and plain paper copier systems; priced at ¥5,000 ($31.25)

- Sharp--A 2/3-inch CCD image pickup (LZ222506) with sensitivity of 7-lux illumination using Sharp's Shallow Flat P-Well Architecture and color complementary filter; 250,000 pixels and 330-line horizontal resolution; 34 percent aperture rate; 0.02 percent maximum smear; 22-pin DIP package; sampling at ¥26,000 ($162.50)

- Seiko Epson--A contact-type linear image sensor integrating the photosensitive area and scanning circuit on the same glass substrate; for A6- and A4- size facsimiles and image scanners; sampling of A4 size module at ¥60,000 ($375) per unit and ¥10,000 ($62.50) during volume production

- Toshiba--A low-cost, amorphous silicon contact image sensor featuring high sensitivity; one-eighth the size of available sensors; eight picture elements per millimeter; reading speed of 5 to 10 milliseconds per line of A4-size text paper; amorphous silicon layer formed on a glass substrate using plasma chemical vapor deposition method (CVD) and titanium electrodes formed atop the amorphous silicon layer; 1,728 light-receiving elements horizontally arranged on glass surface; 16 elements bundled into groups of 108 common electrodes that are wired across 16 vertical electrodes (versus 54 x 32 electrodes in conventional sensors); sensors could eventually be sold at ¥10,000 ($62.50)

Gallium Arsenide

- Hitachi--Two GaAs MESFET models; ultralow noise version of 1.3dB (2SK779) and low noise version of 1.6dB (2SK780); sampling prices of ¥20,000 ($125) for 2SK779 and ¥5,000 ($31.25) for 2SK780; prices for 10,000-unit lots are ¥10,000 ($62.50) and ¥2,500 ($15.63); sampling since August

- Matsushita--An infrared thermal annual (IRTA) method to anneal ion injection layers of GaAs devices; annealing method effective for unifying the voltage level of GaAs FETs, contributing to higher-density GaAs devices; GaAs device annealed at 1,000°C for 10 seconds; slip-line crystal defects (usually caused by rapid heating and cooling of GaAs substrates) prevented by inserting a dummy wafer between the silicon and GaAs wafers to lessen the sudden temperature change and by placing a guard ring around the substrates; electrical aberrations half of conventional electrical furnace annealing methods; for use in fabricating 4K and 16K GaAs SRAMs

  - Two UHF GaAs amp ICs (GN1030/1031) consisting of a dual-gate GaAs FET and five resistors; bias resistor circuit network; 6-pin DIP package; 1.6dB gain; sampling at ¥150 ($0.93)

- Matsushita Electronics/Matsushita Electric--A GaAs-based RF amplifier IC for the UHF zone (GN1030/1031); priced at ¥150 ($0.94); volume production of 50,000 monthly was planned by late 1986

- Mitsubishi--Mass production of GaAs and AlGaAs membranes using molecular beam epitaxy (MBE); simultaneous growth of seven sheets for one cycle, making it possible to grow GaAs FET wafers in one cycle; round-the-clock operation feasible due to a source airlock mechanism that can fill the molecular beam source without interrupting the vacuum in the growth chamber; for use in producing weak signal and high-output GaAs FETs, and in the future HEMT, GaAs ICs, and optoelectronic ICs

- Mitsubishi Metals--Mass production of GaAs wafer samples using liquid encapsulated Czochralski (LEC) method; arsenic pressure-controlled growth method used to seal the surface of liquid GaAs with a boron oxide sealant and grow crystals in an arsenic vapor; low dislocation rate of less than 2,000 defects per square meter; plans to produce 1,000 units per month

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- NEC--A prototype InP FET for microwave/millimeter waveband width; an InP substrate formed with ion implantation, which is layered with an AlGaAs crystal as an insulating gate using MBE method; 1-micron gate; 83dB power gain at 12 GHz; for use in 30- to 40-GHz range high-power satellite devices

  - A GaAs logic IC series (MuPG700 Series); 120ns access time; three input OR/NOR gates; 2 GHz and above high-speed capability; ECL compatible

  - A GaAs lightly doped drain (LDD) FET; silicon ion implantation in gate electrode area reduced and thinner doped layer; ion doped LDD structure chosen to reduce problems of increased resistance and slower speeds

  - A 3,000-gate GaAs array; 7.5 x 7.4mm chip consisting of 3,000 basic cells forming one diode and seven FETs; 56ps no-load gate delay time; 180ps with 2mm wiring attached, or twice as fast as ECL gate arrays and one-third power consumption; plans for commercializing an ECL-compatible device; result of MITI's Supercomputer Project

  - A GaAs 8x8 matrix LSI switch capable of transmitting 1.6 Gb/sec; 64-bit RAM for output buffer switch control; buffered logic (BFL) for basic switching circuit; SCFL for output buffer; 260/280ps output; 5.1ns access time for 64-bit RAM; 375 gates; 3.0 x 4.0mm chip; 2.4W power consumption; ECL I/O level

- Sumitomo Electric--A method for growing GaAs monocrystals of 20cm length without flaws or lattice defects (twice current methods); plural heaters introduced to the electric cell and computer-controlled system for analyzing specific gravity, buoyancy, and surface tension of the crystal during heating

- Tohoku University/Sendai Semiconductor Research Institute--A GaAs diode capable of emitting a stable 180-GHz signal; produced by growing ultrathin layers of GaAs crystal using liquid phase growth method; maximum 338-GHz signal (10mW) recorded by adopting a pulse mode; potential use in high-frequency semiconductor devices for satellite communications, radar, and data processing

- Toshiba--A heterojunction AlGaAs/GaAs ring oscillator with 35ps delay per gate, developed using a photolithography and ion implantation technology; 97 transistors integrated on a 0.35 x 1.5mm chip; AlGaAs emitter layer and GaAs base layer and collector layer; thin film formed by MBE process; 2-micron emitter electrode width; 0.25-micron gap between emitter and base electrode; 6-micron junction width; simultaneous implantation of magnesium and phosphorus to suppress the diffusion of impurities

Josephson Junctions

- MITI Electrotechnical Laboratory--Claims world's first CPU incorporating Josephson junction device circuits; an arithmetic logic unit (ALU) consisting of four pure niobium Josephson devices separated by thin insulating layers of aluminum oxide; 220ps time from input to output at 50 to 70 milliamperes, and 157ps at 90mA; results of the Josephson Computer Technology Research Laboratory established in 1981 as part of MITI's Supercomputer Project

Standard Logic

Power MOSFETS

- NEC--Eleven power MOSFETs featuring proprietary high withstanding voltage-low ON resistance process; 40 percent lower ON resistance and 20 percent shorter switching time than conventional models; pricing of 20A/250V model ¥500 ($3.23), 18A/450V model ¥650 ($4.19), and 5A/900V model ¥600 ($3.87)

Linear/Analog

- Matsushita--Three noise reduction ICs, including a stereo single-chip peak noise reduction IC for hi-fi VCRs (AN6295N), a dbx noise reduction IC for North American sound multiplex television (AN6293), and a two-channel, single-chip dbx IC for cassette decks

- Mitsubishi--A current driver IC series; 5.0A maximum current at 80V; 0.25 to 0.55V saturation output voltage at the output phase transistor; sampling at ¥130-¥240 ($0.82-$1.50)

- NEC--Five high-speed A/D and D/A converters for consumer electronics equipment using NEC's original CMOS analog process; two 8-bit, 20 megasamples/second, two 6-bit, 20 megasamples/second, and an 8-bit, 50 megasamples/second version

- Rohm--New ICs for telephone speech networks; receiver amplifier with large output, allowing use of either dynamic or ceramic speakers; a single chip (BA6563K) incorporating amplification function and retention muting circuit; also low-cost, compact circuit with a simplified circuit (BA6566F)

- Tokyo Sanyo--Two audio power IC series; one-channel L series and the LP series with protection circuit and muting circuit; oblong substrate structures (39mm high at PC substrate mounting by 105mm wide by 8.5mm thick) to accommodate high pin counts; sampling since October at ¥1,000 to ¥1,500 ($6.25 to $9.38)

Sensors

- Hitachi--A multigas sensor; six types of thick-film sensors for measuring six types of gases; grouped method of data handling

- Toyoda R&D Laboratories (Toyota)--An ion-sensitive FET transistor for measuring sodium ion content in blood samples; silicon dioxide, silicon nitride, and other materials stacked onto a silicon substrate; used for detecting and diagnosing diseases

- Yazaki Machinery--A highly sensitive semiconductor sensor designed to prevent incomplete combustion in various gas heating systems; 3.0 x 4.0 x 1.0mm device; capable of detecting carbon monoxide fumes of 100 parts per million (ppm), or 2,000 to 3,000 ppm in a gas burner environment; temperature resistant up to 900°C; future pricing of ¥1,000 ($6.25); potential use in boilers, stoves, and heaters

Discretes

- Matsushita Electronics--Six one-chip Darlington connection transistors for audio circuits that integrate driver and output power transistors; complementary pairs of PNP and NPN units with 35W, 40W, 45W, 50W, 70W, and 100W collector dissipations; 35W unit sampling at ¥150 ($0.94)

- NEC--Ninety semipower transistor models with built-in resistors capable of handling up to 2-ampere corrector current; 52 NPN models; 38 PNP models

- Sharp--Two field-effect transistor (FET) prototypes using silicon carbide; chemical vapor deposition (CVD) method used to grow high-quality monocrystals; junction-type and insulation gate-type prototypes; bottom layer consisting of boron-doped P-type silicon carbide monocrystals; channel layer of N-type silicon carbide monocrystal without impurities; upper layer of junction-type FET composed of aluminum-doped silicon carbide monocrystal; for use in automobile engine MCUs because of new material's superior qualities against heat and noise

- Toshiba--A MOSFET developed using epitaxial technology; 6 x 6mm chip; 20mm square emitter usable surface; aluminum and imperfect silicon two-level field plate structure

New Semiconductor Functions

- Kyoto University--A superlattice structure containing alternating layers of 200-angstrom-thick amorphous silicon and 40-angstrom-thick silicon carbide to produce an ultrahigh-speed device with electron speeds ten times better than conventional devices

- Mitsubishi Electric--An experimental, large-surface, three-dimensional device without crystal defects, paving the way for 16Mb+ DRAMs; 1.0 x 1.5 x 2.6mm chip; lasers and silicon-on-insulator (SOI) technology used to form silicon single crystals on insulation layer; laser irradiation of 4-inch wafer in 20 minutes, with potential for irradiating 6-inch wafers and developing 10,000-gate arrays on 10 x 9mm chips; new crystal growth front orientation controlled, laser recrystallization process; test manufactured three-layer 256K SRAM and image processor; potential for speeding up operation time of conventional devices by 30 percent

New Processes

- Hitachi/Toyohashi University of Technology--Claims world's first hybrid beam source, capable of emitting either electrons or ions, for future 64Mb DRAMs and three-dimensional ICs; a tungsten metal needle emitter chip with a 0.1- to 0.2-micron tip diameter positioned in a crucible filled with liquid gallium, which serves as the ion source; project sponsored by the Ministry of Education (MOE)

- Matsushita Electronics--A nanometer pattern lithography technology capable of producing 0.1-micron patterns; 0.5- to 10-micron-thick polymethyl methacrylate resist, electron beam of 20 to 25kV accelerated voltage, and isopropyl alcohol rinse used; plans for developing GaAs devices, submicron devices, and X-ray masks using synchrotron orbital radiation (SOR)

- NEC--A high-power excimer laser using krypton fluorine (KrF); 30-watt average output; for use as an exposer for surface treatment of new semiconductor materials

- Nippon Telegraph and Telephone (Atsugi Lab)--A plasma X-ray source for drawing 0.3-micron patterns for memory chips up to 64Mb; 0.9- to 1.4nm wavelength beams ten times stronger than X-rays produced by electron bombardment

- Sanyo Electric--An ultrasensitive positive electron beam resist (SEBR-115) for fabricating 4Mb+ DRAMs; sensitivity made 100 times greater than conventional polymethacrylic acid methyl acrylate (PMMA) resist by converting PMMA into an amorphous material using tetra(n) butyl ammonium perchlorate; 0.75-micron circuit patterns possible; 0.6-microCoulomb per square centimeter sensitivity achieved

- Seiko Instruments and Electronics--A focused ion beam system (SMI-SM) capable of directly drawing, connecting, and cutting submicron metal wiring; priced at ¥100 million ($625,000)

Manufacturing Equipment

- Hitachi--A direct-write electron beam lithography system (EB-F) capable of drawing 0.1-micron lines ten times faster than conventional E-beam systems; strong beam current (0.3 nanoamperes) retained in a special gun that is capable of drawing 0.1-micron patterns on 3- or 4-inch wafers in one hour; electron gun made of titanium-coated tunsten wire; 0.03-micron beam diameter; first system delivered to NTT's Atsugi Semiconductor Research Center; sales from second half of 1987

  - Laser inspection equipment for 6-inch silicon wafers; 0.3-micron positioning accuracy; X-ray microanalyzer

- JEOL Ltd.--An electron beam lithography system (JBX6AIII) capable of drawing up to 0.3-micron lines and handling ten 5-inch masks per hour; 7 x 7-inch mask stage; price ranges from ¥500 million ($3.12 million) to ¥600 million ($3.75 million)

- Matsushita--A holographic wafer stepper with reticle positioning accuracy of less than 0.1 micron, meeting requirements for 0.5-micron design rule used in 16Mb DRAMs; new technology involving laser interference stripes formed between the alignment grids of the reticle and wafer; pair of Fourier conversion lens and a space filter used in optical system

- NEC--A photomask repair system employing laser chemical vapor deposition (CVD) technology (Laser Mask Repair SL454A); a YAG laser used to cover white mask defect spots with a chromic film formed by chrome carbonyl vapor; 25-micron-diameter spots repairable within 30 seconds; system priced at ¥120 million ($750,000)

- Nikon--An electron beam writing machine being developed jointly with Nippon Telegraph and Telephone in NTT's EB60 development project

- Seiko Electronics--An ion beam machine (SMI-3M) capable of laying out and connecting LSI wiring patterns; 0.1-micron beam; ion beam CVD method used; priced at ¥100 million ($625,000) for basic unit

- Seiko Instruments and Electronics--Molecular beam epitaxial equipment capable of using gaseous materials as the molecular beam source; designed for growing single-crystal thin films to develop high-speed ICs and photodiodes; priced at ¥68 million ($425,000)

- Toshiba--A prototype excimer laser photolithographic system capable of drawing 0.35-micron lines and theoretically possible 0.25-micron lines; krypton fluorine excimer laser used to generate 249nm wavelength ultraviolet beam; experiment successful in drawing 5mm-square circuit patterns on 2cm-square wafers; an optical reduction system made of quartz lens for development of future 64Mb DRAMs; commercially viable system possible by late 1987; low production cost advantage over electron beam (one-fourth) and X-ray systems (one-eighth)

Clean Room Automation

- Kawasaki Heavy Industries--A direct-drive robot for clean rooms achieved by altering the AdeptOne, its existing DD robot; adaptable to clean rooms for 1Mb DRAMs; priced at ¥8.0 million to ¥8.5 million ($50,000-$53,125)

- Seiko Instruments and Electronics/Ulvac BTU Corp.--An experimental clean room robot that will be commercialized in the near future

Test Equipment

- Ando Electric--A 40/80-MHz, 256-pin system for high-volume VLSI testing (DIC-8035B); timing accuracy of ±1.6ns for CMOS devices and ±0.7ns for TTL and ECL gate arrays; configured as a basic system or complete tester for custom chips; two-device simultaneous testing and DC measurements; complete debugging of test programs possible

  - An ASIC tester (DIC-9000); testing managed by one 32-bit MPU, while control and communications managed by another; test capability of 512 I/O pins, 100-MHz operation, and 1Mw per pin pattern depth; SUMMIT or PASCAL programming language usable; general-purpose, bipolar, and low-capacitance stations and multiuser function

- Canon--A fully automated wafer prober (AT-800) adaptable to 200mm wafers and capable of processing two cassettes (50 wafer starts) at once; 20 percent smaller footprint than with current 8-inch wafer models

- Hitachi Electronics Engineering--A custom IC test system (HITES-3150) adaptable to large-capacity EPROMs and EEPROMs up to 4Mb and capable of implementing 100 writing function tests at the same time; 10-MHz test speed; priced at ¥100 million ($625,000)

- Minato Electronics--A tester capable of testing PROMs and EEPROMs up to 8Mb (Model 4220); capable of read/write tests, mask ROM read tests, and DC parametric tests; also handles double-chip ROMs, address data multiplex ROMs, 16-bit ROMs, and page ROMs

- Mitsubishi--A laser-based system (MD-2301) for measuring the thickness of the membrane coating of various film types; measurement range of 10 to 500 microns and speed of 100 to 200 meters per minute; 0.1-micron resolution and ±0.5-micron repeatability; priced at ¥5.9 million ($36,900)

- Nikon--A wafer inspection microscope (Optistation-1A) for use with photolithography processes; suitable for custom IC and small-lot quantities; 130kg main body weight; priced at ¥9 million ($56,250)

Materials

- Dai-Nippon Ink and Chemicals--A positive photoresist (DPR-2600) for 4Mb memories capable of 0.6-micron lines; phenolic resin base and quinonediazo compound for sensitizer; priced at ¥120,000 ($750) per gallon

- Institute of Physical and Chemical Research (Riken)/Nippon Oil and Fats Co./Tokyo University of Agriculture and Technology--An organic insulating film displaying a "tunneling effect" for use in high-speed switching devices; an ultrathin film of high-temperature (200°C) resistant polydiester-fumarate (PDF) produced using the Langmuir-Blodgett method

- Matsushita Electric/Hayashibara Biochemical Laboratories--Japan Synthetic Rubber Company commissioned to produce a water-soluble polymer (a combination of an optical bleaching reagent and polysaccharide compounds) to produce 0.6-micron linewidth memories; Japan Synthetic Rubber to be provided with both firms' water-soluble polymer manufacturing technology; polymer applied with photoresist to wafer during exposure process; for future fabrication of 4Mb DRAMs

- Mitsubishi Electric--A silicon-on-insulator (SOI) method using an argon laser for growing defect-free monocrystal silicon; seed crystal formed by cutting off edge of the insulator layer and identifying the ideal optical scanning direction for the argon laser for growing the crystal; defect-free silicon layer grown on a 1.0 to 1.5 x 2.6 mm chip; 20 minutes to grow a monocrystal silicon layer on a 4-inch substrate; for use in commercializing three-dimensional ICs

  - A method for evaluating extreme humidity tolerances of plastic small outline packages (SOPs); capable of protecting devices for 24 hours in 85°C/85 percent humidity environments

- NEC--A new amorphous alloy of tantalum tungsten, silicon, and boron that can endure temperatures up to 1,180°C; ceramic-like properties; ribbons of amorphous alloy produced by heating with hot plasma and cooling through contact with cold copper; 80 percent tantalum and tungsten, 20 percent silicon and boron

  - Silicon-on-insulator (SOI) technology for 1-micron-thick LSIs on 4-inch silicon wafers

- RHD Corp/Nisshin Steel/Toyo Ink Mfg./Mitsubishi Corp.--A ZnSe single crystal for use in flat displays and laser optical communications

- Sanyo Electric--A positive-type electron beam line resist (SEBR-115) using proprietary amorphous technology (Sanyo Electron Beam Resist); suitable for 4Mb devices featuring ultrahigh sensitivity, high resolution, and high stability; conventional resist preparation PMMA (methyl polymethacrylate) made amorphous (noncrystalline) using teta-m-butyl ammonium perchlorate; 0.6 microcoulomb-per-square-centimeter sensitivity; 0.85-micron resolution for 0.5-micron-thick resist; priced at ¥300,000 ($1,875) per liter

- Taiyo Yuden--A new ceramic material produced at 900°C to 1,000°C and a ceramic multilayer substrate that can use copper as wiring material; for use in 256K DRAM, 256K SRAM, and 1Mb DRAM memory modules

Packaging

- NEC--Emboss carrier taping method for PLCC, miniflat, and other surface mount ICs, enabling mounting speed of 0.5 second or less; emboss tape storage capacity of 2,500 ICs; 12mm- and 16mm-wide versions that comply with EIAJ specification RC-1009

- Seiko-Epson--A new mounting method (chip on flexible tape) capable of reducing thickness of liquid crystal displays by 25 percent and manufacturing costs by 20 percent

  - A surface-mount system (MMT-03) with a built-in precision assembling robot for fine-pitching mounting of flat package ICs to printed circuit boards; capable of mounting fine-pitched QFP ICs measuring 0.65 to 0.4mm at rate of five to six seconds per piece and 0.05mm positioning accuracy; priced at ¥20 million ($125,000)

Technology Trends--Fourth Quarter 1986

COMMENTARY

Megabit Memory Devices: The Key to Future Systems

The growing demand for inexpensive, large-capacity storage, especially in video and speech applications, fuels the search for higher-density memory in Japan, despite U.S. semiconductor tariffs and the stagnant domestic economy. Dataquest expects that the MOS memory market to be $12.3 billion in 1991, or 175 percent larger than the market in 1986. Dynamic and static RAMs with submicron geometries, should account for $8.3 billion in 1991, or 68 percent of all MOS memory revenue.

To develop these leading-edge devices and use excess memory capacity, Japanese chip makers are pushing memory technology in four key areas:

- Submicron geometries for megabit memories
- Three-dimensional IC structures
- Hybrid RAM modules
- Silicon disks to replace floppy disks

Megabit memories are becoming increasingly important for video, image, and speech processing. To develop 64Mb and 256Mb memories, the Japanese are developing small synchrotron orbital radiation (SOR) machines capable of writing sub-0.15-micron geometries, as discussed in our Second Quarter 1986 Technology Trends. MITI, MPT, and 13 companies are spending $61 million to develop an ultrasmall (one-meter-diameter) SOR ring.

Concurrently, MITI's Future Electron Devices Project is pursuing three-dimensional ICs as an alternate path to high-density megabit memories and "smart" microprocessors. Trench capacitator cells are already being used in 4-Mbit DRAM prototypes. For 16-Mbit and larger DRAMs, Mitsubishi Electric announced in mid-1986, a large-surface, 3-D device containing laser-recrystallized silicon-on-isolator (SOI) material.

But the search for new mass memory applications is focused on new high-density memory systems. RAM modules (VLSI memory chips mounted onto a single ceramic substrate), which have required expensive, high-temperature-resistant precious metals, are becoming economical due to improvements in interconnection technology. Taiyo Yuden, a ceramic capacitor maker, recently announced a copper replacement for ceramic substrate wiring and a new ceramic multilayer substrate that features low sintering temperatures.

In 1986, Japanese makers also sought to replace floppy disks with silicon disks, also called RAM disks, with up to 2 Mbytes of memory storage. Currently, these standalone systems have battery backup and can be plugged into personal computers. Dataquest believes these systems could replace floppy disks in selected applications if the cost-performance ratio is reduced. We will issue a newsletter on this subject during the summer.

Dataquest believes that there are still many opportunities and technical challenges facing memory device makers. The battle for market share has only begun. The key is to develop memory devices that meet a specific market need, such as IC cards, speech recognition and synthesis, high-density memory storage, or video processing.

CORPORATE R&D PROJECTS

New R&D Centers

Japanese companies are opening new R&D centers overseas because of growing efforts in the United States to restrict technology flows to Japan. As shown in Table 1, automobile and consumer electronics makers have opened several centers in recent years:

Table 1

OVERSEAS JAPANESE R&D CENTERS (1977-1987)

Company	Date	Research Focus	Location
Aisin Seiki	1987	Electronics	Sophia Antipolis, France
Asahi Optical	1985	Optical disks	Englewood, CO
Hitachi	1985	Telephone exchange software	Atlanta, GA
Honda Motors	1984	Electronics, automotive	Los Angeles, CA
Horizon Research	N/A	Computers, software, systems	Waltham, MS
Kanto Electronics	1984	ICs, peripherals	Silicon Valley
Kobe Steel	1986	Electronics	North Carolina
Kyocera	1985	Electronic materials	Vancouver, WA
Matsushita	1986	Electronics	Taiwan; W. Germany
Mitsubishi Electric	1984	Semiconductors	North Carolina
Nakamichi	1984	Nonaudio electronics	Torrance, CA
NEC Electronics	1986	VLSI research for Roseville	Sunnyvale, CA
NEC Information Systems	1982	Software, prototype hardware	Foxboro, MA
Nippon Denso	1986	Automotive electronics	Battle Creek, MI
Nissan Motors	1983	Electronics, automotive	Michigan
Otsuka Pharmaceutical	1985	Cytology, immunology	Maryland
Sony	1984	Optical recording media	Portland, OR
Sumitomo Electric	1983	Optoelectronics	Raleigh, NC
Toyota Motors	1977	Automotive, electronics	Los Angeles, CA
Yaesu Radio	1985	Satellites, radios	California

Source: Dataquest
June 1987

Superconductors

Shin-Etsu Chemical Co. began construction of the world's largest rare-earth refinery plant with an annual capacity of 100 tons at its Takefu, Fukui Prefecture site. The Takefu plant will produce rare elements such as samarium, europium, gadolinium, yttrium, and terbium, which are being used to develop superconductors. The ¥3 billion ($21.4 million) plant, which will refine materials from W.R. Grace & Co. (U.S.) and Molycorp Inc. (Canada), was completed in March 1987. According to the Japan Society of New Metals, Japanese demand for rare elements grew from ¥28 billion ($200 million) in 1984 to ¥32 billion ($228 million) in 1985, and was estimated to be ¥34 billion ($242 million) in 1986.

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TRON Project

In November, 29 companies joined Tokyo University's TRON Project, bringing the total number of companies to 37. Fujitsu, Hitachi, NEC, Mitsubishi, NTT, Oki Electric, and Toshiba are the original 8 members. Alps Electric, Fuji Electric, Sanyo, Sharp, Ikegami Communications, and Yamaha are among the new members. During the symposium, NEC displayed a prototype TRON computer incorporating I-TRON (industrial TRON) in an MS-DOS operating system.

In October 1986, Fujitsu and Hitachi announced that they will use proprietary architectures in the TRON 32-bit microprocessors. The companies announced the plans discussed below.

Fujitsu

- Intel's 8086/186/286--continue second-sourcing and prepare to support the 80386
- CMOS 32-bit TRON MPU (1.0- to 1.3-micron)--develop a proprietary device with Hitachi as part of the TRON Project

Hitachi

- Continue second-sourcing Motorola 8- and 16-bit MPUs
- H Series CMOS 8-bit MPUs (1.3-micron)--market to office automation makers from late 1987
- H Series 16-bit MPUs (1.3-micron)--market to word processor, laser printer, robot, and numerically controlled machine tool makers from July 1987
- H Series CMOS 32-bit MPUs (6 MIPS capability, 32-bit internal and external processing, and 1.0- to 1.3-micron design rule)--market to work station makers in late 1987

GOVERNMENT R&D PROJECTS

MITI Fifth-Generation Computer Project

MITI's Institute for New Generation Computer Technology (ICOT) has begun a program to develop a parallel processing system with 50 to 100 personal sequential inference (PSI) machines. The system will use individual PSIs, not microprocessors. ICOT will develop software to assign individual tasks to each PSI and control the data traffic between PSIs. ICOT's goal is to build a multi-PSI system with 50 machines and expand to 100 PSIs in 1987.

Mitsubishi Electric, the first Japanese company to commercialize ICOT's sequential inference computer, is developing artificial intelligence (AI) software for its Melcom PSI machines. Specifications for these machines are shown in Table 2. Mitsubishi is also organizing projects with PSI users to jointly develop various expert systems for office and factory automation. Mitsubishi America is conducting a survey to identify market demand for automatic diagnostic systems and decision-making systems in the steel, chemical, food processing, and transportation industries.

Table 2

MITSUBISHI'S PERSONAL SEQUENTIAL INFERENCE (PSI) MACHINES

	PSI-1	PSI-II
Highest speed	33K LIPS	100K LIPS
Operating software	KL0	KL0
Processor device	High-speed Schottky TTL	CMOS gate arrays (Am29300 Series)
Cache	4K x 2-bit	4K words
Address width	16M words	64K words
Microinstruction	64-bit width	53-bit width
Processor cycle time	200ns	200ns
Operating systems	SIMPOS	SIMPOS
Programming language	ESP	ESP

Source: Nikkei Electronics

Hitachi has developed a new AI computer language, S-ONLI, that can categorize and manage large knowledge bases by dividing them into smaller increments by function and linking them to perform inference functions efficiently. The program runs 7.5 to 12 times faster than conventional knowledge base systems. Items can be categorized into 10 classifications, each containing 1,000 items. Hitachi plans to commercialize the software and use it in its mainframe computers and workstations.

Hitachi is also developing LISP and PROLOG versions for its Hitac M Series mainframes and Model 2050 workstations. The new languages will allow Hitac mainframe users to build and use AI programs with various data bases developed with existing languages. Hitachi released the new programs at the end of 1986 at a monthly lease price of ¥120,000 ($750) for mainframe applications and ¥400,000 ($2,500).

Mitsubishi Electric introduced its second AI machine (PSI-II) in spring 1987. The new computer will have an inference speed of 120 kilo logical inferences per second (LIPS), three times faster than the PSI-I. The machine, which will cost about ¥10 million ($62,500), will use 1-Mbit DRAMs on a single board.

Nippon Telegraph and Telephone (NTT) introduced an AI workstation, called ELIS, with a LISP processing capability of one million instructions per second. The computer features a single-chip CPU built on a 20 kilogate LSI, a main memory of 8 to 128 Mbytes, and a disk storage capacity of 135 to 540 Mbytes. The computer will be sold domestically and overseas at ¥10 million ($62,500).

MITI Supercomputer Project

In December 1986, Fujitsu announced its VP-30 supercomputer, which costs two-thirds of its V-50 machine. Monthly rental is ¥30.6 million ($191,250). The computer has a 110 MFLOPs capability, 64 Mbytes of main memory, up to 32 channels, and a maximum transfer speed of 96 Mbytes per sec.

MITI New Glass Study Group

In October 1986, MITI formed the New Glass Study Group to investigate basic problems in using glass as a material for future communications, data processing, and optoelectronics applications. The group, which includes 19 scholars and industry representatives, visited the United States in late October and submitted its findings in February 1987.

Ministry of Education TRISTAN Accelerator

In November 1986, the Ministry of Education's High Energy Physical Research Institute succeeded in generating an electron beam with a high energy of 25 billion electron volts, using the large-scale electron-proton collision accelerator (TRISTAN). A beam incidence test using a 1.0mA beam current was conducted, followed by an acceleration test at high-frequency voltage. The institute aims to attain a 30 billion volt electron beam in the future.

MITI/MOE/STA Space Laboratory Project

MITI, the Ministry of Education (MOE), and the Science and Technology Agency (STA) have established the "Free Flyer" Project to launch a 3-ton space laboratory by fiscal 1992. The total project, budgeted at ¥30 billion ($187.5 million), will focus on developing a 3.7-meter diameter, octagonal

laboratory housing eight laboratory modules to conduct space experiments on semiconductors, new materials, and biotechnology. The "Free Flyer" will be launched by Japan's H-2 rocket and recovered by the U.S. space shuttle. The 13 project participants include:

- Mitsubishi Electric--Prime contractor to organize the project and develop the satellite mainframe, lab module storage box, and data processing system
- Nissan Motors--Frame structure
- Toshiba--Power supply system
- NEC--Communication equipment and solar cell paddle
- Mitsubishi Heavy Industries--Propulsion system
- Fujitsu--Ground control system
- Nippon Denso--Coupling section between the "Free Flyer" and the U.S. Space Shuttle
- Nippon Electric Development--Software for lab operations
- Ishikawajima-Harima Heavy--Experimental systems for new materials
- Hitachi--Experimental systems for bioengineering
- Kawasaki Heavy--Ground support systems
- Mitsubishi Precision--Part of satellite position control system
- Sharp--Solar cells

MITI Biochip Project

Research aimed at developing an organic computer (biocomputer) has begun at MITI's Biochip Project. The 10-year project is budgeted at ¥5 billion ($35.7 million) and will be administered by the quasi-governmental R&D Association for Future Electron Devices, which is also developing 3-D ICs, superlattices, and hardened ICs. Eight companies are involved in the research: Fujitsu, Hitachi, Matsushita Electric (an R&D subsidiary), Mitsubishi Chemical, Mitsubishi Electric, NEC, Sanyo Electric, and Sharp. Sumitomo Electric will provide data on biological information processing to a new R&D evaluation committee that will work with the association. The project will explore the information processing nerve mechanisms of lower animals, such as sea hares and nematodes, and study their application to biochips and biocomputer architectures.

Technology Trends--Fourth Quarter 1986

NEW PRODUCTS AND TECHNOLOGY TRENDS

Memory

- Fujitsu--A 10ns, 16K ECL RAM; two types including MBM10484A for -5.2V and MBM10484A for -4.2V power supply; 4Kx4 structure; 1.0-micron design rule; Fujitsu's proprietary U-shaped isolation method (IOP-II); 70,000 elements on a 5.5 x 3.8mm chip; 1.35- and 1.17W power consumption

  - Capacitor cell structure for 4- and 16Mb DRAMs; 4Mb DRAM process featuring 2.4 x 5.3-square-micron cell, 1.0-micron gate length, 1.5 x 2.8mm square chip; 16Mb featuring 0.87 x 1.6-square-micron memory cell and 4.0-micron deep cell

  - A 4Mb CMOS mask ROM (MB834100); 524,288 x 8 and 262,144 x 16 structures; 1.2-micron, single-layer polysilicon gate process; 9.2 x 7.9mm chip size; 250ns access time; 275mW power consumption during operation; 4-pin DIP package; sampling at ¥4,000 ($28.57)

  - A 4K bipolar RAM (MBM10474A-5/7 and MBM10047A-5/7); 1.0-micron design rule; U-shaped isolation technique combined with method to thicken the field oxide membrane (U-FOX process); 5ns access time at -5.2V and 300mA power current; sampling at ¥8,000 ($57)

  - A BICMOS 64K SRAM; 15 to 20ns; I/O level ECL 10K/100K; 70mA operating time; 1.5-micron process; 30mm-square chip; shipping from second half 1987

  - Two 16K bipolar PROMs; 30ns version (MB7118Y) and 35ns version (MB7118EW); sampling at ¥1,000 ($7.14) and ¥1,500 ($10.71) respectively

  - A CMOS 256K SRAM (MB81C81) with 45ns access time; 256Kx1 structure; 5.0 x 11.3mm chip; 300-mil, 24-pin ceramic DIP; 550mW power consumption during operation and 83mW at standby; sampling since November 1986 at ¥18,000 ($112.50); plans for a 35ns device in 1987

  - A 70ns CMOS 256K SRAM (M5M5256AP70); 32Kx8 structure; 1.5-micron design rule; 375mW maximum power dissipation during operation and 2mA at standby

- Hitachi/Kyushu University--A 5-bit Bloch line memory device with memory region of 200 x 400 microns on a 6mm-square GGG substrate; magnetic film with N- and S pole magnetization, and a stripe magnetic region; 1.0- to 0.5-micron-wide magnetized micromemory structure; successful testing of read-write and data-transfer operations; data stored by using the difference in polar directions generated along the domain wall of a magnetic field; plans for a 256Mb device with 1.0 x 0.5-micron cell size, 16 bits per square centimeter, and 6ms readout time within 5 years; basic technology developed by Professor Susumu Konishi of Kyushu University

  - A 64K CMOS EEPROM (HN58C65); metal nitride oxide cell process; 8Kx8 structure; 200ns access time; 32-byte page, byte-write or page-write mode, data polling feature, and read/busy line protection from inadvertent write operations; 28-pin plastic package; 20-microsecond automatic byte-write operation; compatible with Hitachi's NMOS HN58064; priced at ¥2,170 ($13.56)

  - Two SOJ-type 1Mb DRAMs; HB56A18A/B with 1Mx8 structure sampling at ¥39,000 ($278.57) or ¥32,000 ($228.57) for 1,000-unit lots; HB65A19A/B with 1Mb x 9 structure sampling at ¥42,000 ($300) or ¥35,000 ($250) in 1,000-unit lots; 190/200/260ns normal mode; 70/85/105ns high-speed page mode

  - A 1-Mb CMOS SRAM; 35ns access time for 8-bit structure; 1.0-micron rule; 6.4 x 11.6-square-micron memory cell; 8.0 x 13.6 square-millimeter chip

  - A 1Mb BICMOS DRAM; planer-type capacitor memory cells; NMOS gate; BICMOS peripheral circuits; NMOS emitter source; 1.2-micron process

- Matsushita Electron--A 4Mb CMOS mask ROM (MN234000); 200ns maximum access time; 5mW power consumption at standby and 90mW in operation; 5.79 x 11.12 mm chip; NAND multigate method based on a double-layer polysilicon process used; 40-pin DIL or 64-pin flat package; monthly production of 50,000 units since January 1987

- Mitsubishi Electric/NTT--A jointly developed 64K CMOS SRAM for satellite use; can withstand 10 years of use in a hostile space environment; soft error problem solved by lowering the temperature to 900 degrees Celsius during the heat treatment process and using oxidizing and heat treatment methods without hydrogen; latch-up problem solved by using a 300-angstrom-thick oxidized thin film on an epitaxial wafer and adopting a well-source structure; 2-micron CMOS process; 7.9 x 6.6mm chip; 400,000 elements; 150ns access time; 20mA power consumption during operation and 1 microamperes during standby; priced at ¥1 million ($6,250)

- A 64K CMOS SRAM (M5M5187AP Series); 25ns maximum access time; 64Kx1 structure; compatible with M5M5188AP Series (16Kx4); 300-mil, 22-pin standard package; separate I/O pins; double poly, one layer aluminum 1.3-micron CMOS polycide gate process; 3.69 x 6.35mm chip; sampling at ¥4,800 ($30)

- A 1K SRAM RAM (M5M81C55P-2/FP-2); 256Kx8 structure; 40-pin DIP and SOP; sampling at ¥900 ($6.42)

- A test-produced 4Mb DRAM using 0.8-micron design rule; 9 million transistors on 5mm square chip; 4Mx1 or 4Mx4 organization; 1Mb DRAM package used; mass production planned for 1989; 4Mb DRAM prototypes also by NEC and Toshiba

- A CMOS 256K SRAM (M5M5256AP); 32Kx8 structure; 70ns access time; sampling at ¥4,900 to ¥6,400 ($35.00-45.70); also a small-size mold package version (M5M5256FP) priced at ¥5,000 to ¥5,600 ($35.70 to 40.00)

- NEC--A 256K, first-in first-out (FIFO) RAM with CMOS-structure DRAM; 32Kx8 structure (MuPD42532C); one-third to one-fifth the size of equivalent SRAM boards; 1.2-micron design rule; double-buffer-structured, read-write data register that allows simultaneous read-write operation; 100ns cycle time; 50ns access time; 80mA current consumption; 600 mil, 40-pin package; sampling at ¥10,000 ($62.50)

  - A 1Mb CMOS DRAM; page/nibble/static column mode (MuPD421000/421001/421002); 256Kx4 high-speed page/stack column (MuPD424256/424258); 128Kx8 pseudo SRAM (MuPD42128); 80ns RAS access time; 20ns CAS access time; 45ns address access time

  - A 1Mb CMOS UV EPROM family (MuPD27C1000); 150/200/250ns; 0.5ms/byte programming time; 64Kx16 in 40-pin DIP; 128Kx8 in 32-pin DIP; 50mA maximum power dissipation

  - A ditch-type transistor adaptable to 4Mb DRAMs as a new memory cell structure; 0.5-micron deep by 0.8-micron wide ditch; 9.0mm-square transistor surface; 1.0-micron distance between ditch and word circuit

  - Four 16K bipolar PROMs (MuPB431AC/D); 4Kx4-bit; two 25ns parts and two 35ns parts; 150-microsecond/bit write-in time; 300-mil 20-pin ceramic or plastic DIP

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- Oki Electric--A CMOS 4Mb mask ROM with 200ns access time; 260Kx16 and 520Kx8 types; 1.5-micron design rule; volume production in August 1987 at Miyazaki Oki Electric

  - A 256K CMOS SRAM (MSM51256); 32Kx8; 120/150ns; 45mA power dissipation during operation; 1.0-micron process; 28-pin DIP and 32-pin PLCC; shipping from December 1987

  - A CMOS 1Mb EPROM with 120ns access time; 1.5-micron design rule; volume production from August 1987

- Sharp--A 2Mb CMOS mask ROM (LH532000); 200ns access time; 1.2-micron design rule and tungsten silicide process; 256Kx8 or 128Kx16 organization; 35mA power consumption; available since October 1986 at ¥2,400 ($15)

  - A 1Mb DRAM combining NMOS and CMOS technologies; 1.2-micron design rule; mass production of a planar-type from March 1987 and a trench-type from summer 1987 at the Fukuyama Works in Hiroshima Prefecture

  - A 4Mb CMOS mask ROM (LH534000); 512Kx8 and 256Kx16 organization; 200ns access time; 50mA power consumption; available since December 1986

  - Four CMOS EPROMs based on technology licensed from Wafer Scale Integration; 1.2-micron geometries; LH57126J series (128Kb) with 70/90/120ns access times, 70ns sampling at ¥12,000 ($85.71); LH57127J series (128Kb) with 100/120ns access times, 100ns sampling at ¥5,000 ($35.71); LH5749J-55 (64Kb) with 55ns access time sampling at ¥9,000 ($64.29); LH5762J series (64Kb) with 55/70/90-ns access times, 55ns sampling at ¥8,500 ($60.71)

- Sony--A CMOS 1Mb SRAM prototype; 1.0-micron design rule; to be announced at 1987 ISSCC in New York City; plans for a 0.8-micron commodity device

  - A 256K CMOS SRAM (CXK58256P/M); 100/120ns; 40mW power dissipation during operation; 28-pin DIP and flat package;

  - Three 256K CMOS SRAMs (CXK58255P); 32Kx8; 45/55/70ns; 60mA power dissipation during operation; 6.6 x 8.3mm chip size; 10.6 x 13.2-square-micron memory cell; 1.0-micron rule; 28-pin DIP; sampling since April 1987

- Toshiba--Three 256K CMOS pseudo-SRAMs (TC51832P); 85/100/120ns; 32Kx8 structure; address & auto refresh; 140/160/190ns shortest cycle time; 55/45/40mA power dissipation; 28-pin 15.2mm-wide plastic DIP; sampling at ¥1,800-2,500 ($12.85-$17.85)

  - Two 256K CMOS SRAMs (TC55256); 32Kx8; 100/120ns; 70mA power dissipation during operation; 5.7 x 13.3mm-square chip; 7.9 x 21.0-square-micron memory cell; 1.2-micron process; 28-pin DIP and SOP; shipping since June 1987

Application-Specific Standard Products (ASSP)

- Toshiba--A BICMOS panel display driver IC (TD62C932F); 250V, 15-MHz voltage; plus/minus 40mA/250V withstand voltage; high withstand voltage DMOS plus CMOS elements; embedded epitaxial PN bond isolation; ¥2,500 ($17.85)

IC Cards

The Japan Electronic Industry Development Association (JEIDA) has released a standardization proposal for IC cards to encourage the use of two-piece connectors. With such a method, 34 and 68 pins per row would be used in the direct-link bus method, and 20 to 40 pins would be used in the I/O bus mode. Either an 8-bit or 16-bit construction may be used. JEIDA developed a prototype pin and connector in January 1987, and issued card, pin, and connector specifications in March 1987.

- Fujisoku--Three memory cards; 192-Kbyte memory card; 2- to 192-Kbyte SRAM, 32- to 192-Kbyte EPROM; 32- to 192-Kbyte mask ROM; 54 x 86 x 3mm; 38 pins flat package; six ICs; 2016 type 75-mAh battery; priced at ¥3,000 ($21.43) for 8-Kbyte SRAM, ¥7,500 ($53.57) for 32-Kbyte SRAM, ¥14,000 ($121.43) for 192-Kbyte ROM

- Mitsubishi Plastics--Boosting production of IC ROM to 300,000 units annually for use in taxi meters and PC game software; installed IC card system into headquarters for 4,200 employees; 70,000 cards to be distributed to employees within three years for management information data bases, control to high-security sections, and cashless dining hall systems

- Oki Electric--A single-chip, 8-bit MCU (MSM61580) with a built-in 16K EEPROM, 8 Kbytes of programmable ROM, and 512 bytes of ROM; 5.0 x 4.5mm chip; 4.9-MHz clock frequency; 813.8ns execution time; capable of handling up to 95 instructions; priced at ¥1,200 ($7.50) in lots of 100,000; jointly developed with Catalyst Semiconductor of Santa Clara, California

- Toppan Printing/Seiko Epson/Fujita Corporation--A jointly developed portable IC card system (IC Card Handy Terminal System); Seiko Epson HC-10 portable computer terminal and small card reader/writer developed by Seiko Epson and Toppan; system linked by phone to a host computer; two systems, one with 16K EEPROM and one with two 64K EEPROMs; Fujita developing a construction personnel management software package

Microprocessors/Microcontrollers

- Fujitsu/Hitachi--Agreement to jointly develop a CMOS 32-bit MPU and market it by late 1987; TRON architecture (The Real-time Operating Nucleus) and UNIX compatibility planned; 1.0- to 1.3-micron design rule; goal of 700,000 transistors on a 10mm-square chip; 1W power consumption; 6 mips operating speed at 20 MHz; C-language software; support for UNIX and ITRON operating systems; sampling from late 1987

- Fujitsu--A proprietary CMOS 8-bit MPU core for MB89700 Series ASIC applications; core consists of an 8-bit external data bus and 16-bit internal bus; 0.33-microsecond instruction execution time; A/D and D/A converters, LCD drivers, RAMs, ROMs, I/O circuits, and software and development tools to be developed

  - A serial communication control LSI (MB89371); two communication channels on a single chip capable of controlling two lines simultaneously; 44mW power consumption during operation and 275mW in standby mode; sampling at ¥680 ($4.85)

  - A single-chip, CMOS MPU (MB89391) that integrates the peripheral functions of the MBL8086 16-bit MPU and incorporates a clock generator, bus controller, interrupt controller, DMA controller, and timer; 100-pin quad-flat package; maximum of 4-channel DMA transfer; sampling at ¥2,400 ($15)

  - A 4-bit, single-chip MCU (MB88549 series) incorporating circuits for LCD controller and driver; 4 Kbytes of ROM and 256 x 4 bits of RAM; 2.86 to 2.0 microseconds minimum command execution time; can serially transmit or receive 8-bit data; sampling since October 1986 at ¥700 ($4.38)

  - Two CMOS, 4-bit MPU with built-in A/D converters; MB88513 featuring 2 Kbytes of built-in ROM and 192 x 4-bits of RAM; MB88511 featuring 4 Kbytes of ROM and 256 x 4-bits of RAM; 48-microsecond conversion; 8-bit resolution; direct LED-driving capability, power-on reset function, and abnormality detection circuitry; 42-pin DIL package; sampling at ¥650 ($4.62) and ¥800 ($5.71) respectively

- A CMOS interface controller (MB89351); 1.5-Mbps transmission speed; 8-byte FIFO memory; 24-bit wide transcounter; 64-pin plastic DIP; ¥1,800 ($12.85)

- A 5-function, single-chip CMOS 8086 peripheral LSI (MB89391); logic generator and bus controller; 100-pin plastic flat package; sampling at ¥2,400 ($17.14)

- Hitachi--A CMOS 8-bit, single-chip IC (HD401220) with built-in EEPROM for TV and VCR tuner control use; 4.25 x 5.0mm chip; 2.0-micron process; 2K EEPROM, 16K mask ROM, 32 bytes of RAM, 14-bit A/D converter, serial interface, and 20 I/O ports; 28-pin DIL package; priced at ¥900 ($6.42)

  - H series MPUs with original architecture; 1.3-micron CMOS process; 8-, 16-, and 32-bit models; 32-bit MPUs with 32-bit internal and external processing, 20-MHz clock time, and 6 mips

  - A bus-wide, 4-bit CMOS OTP MCU (HD4074008/Hd4074408); 8Kx10 OTP ROM; 512 x 4 RAM; 0.89 microsecond instruction time; ceramic sampling at ¥17,000 ($121.43) since November 1986; plastic type for ¥3,800 ($27.14) since January 1987

  - Two 4-bit, ZTAT MCUs (standard HD4074008 and high dielectric HD4074408)) and pulse controller (LSI HD63140); 0.5 microsecond execution time

  - A dual universal serial communications controller (HD68562); 2-channel, 4Mbps transmission; 5- to 8-bit data length

- Matsushita Electric--A RISP real-time image processor (RISP-II) capable of detecting picture edges, removing picture noise, enhancing contrast, processing binary pattern image data, matching patterns, and enhancing picture quality; 10ns image processing speed; vertically isolated self-aligned transistors (VIST); 20,600 elements; programmable RAM; 3- x 3-pixel image register; ECL I/O level; -5.2V power supply; 1.6W power dissipation; for use in inspecting robots; 30 percent improved peripheral resolution with 4-pole electrode inline electron gun; sampling at ¥250,000 ($1,785)

- Mitsubishi--A RISC processor (Pegasus) for Prolog; 239 KLIPs; 10-MHz clock speed; 40-bit word length; 32-bit address; 72-word register file; 42-type instruction set; 92-pin package planned; 2.0-micron CMOS process; 9 x 9mm-square chip

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- NEC--Five 4-bit, single-chip MCUs incorporating a once-write EPROM for controlling receiving frequencies in digital tuning systems; MuPD17P08/13 with built-in 1.5Kx16 EPROM priced at ¥4,000 ($28.57); MuPD17P16 with built-in 1Kx16 EPROM priced at ¥2,000 ($14.28); MuPD17P19 with built-in 2Kx16 EPROM priced at ¥4,000 ($28.56); MuPD17P20 with built-in 1Kx16 EPROM priced at ¥3,000 ($21.42)

  - Three CMOS, single-chip MCUs with built-in synthesizer for digital tuning systems; PD1717CU priced at ¥1,000 ($7.14); PD1719G priced at ¥1,500 ($10.70); PD1720G priced at ¥800 ($5.70)

  - A 16-bit, single-chip MPU with built-in I-TRON, 2.4 microsecond switching speed; commercialized since spring

  - A CMOS, single-chip MCU with 64 x 8 built-in EEPROM (MuPD1717CU); 2Kx10 mask ROM; 64 x 4 RAM; 40-pin shrink DIP; ¥1,000 ($7.14) in lots of 10,000

  - A CMOS, 16-bit single processor (MuPD77C20A); 0.12W power dissipation; 28-pin plastic DIP; 28-pin ceramic DIP; 44-pin PLCC

  - A hard disk drive control IC (MuPD7262) that conforms to ESDI (enhanced small device interface) standards; NMOS structure; 6.0 x 5.8mm chip that replaces up to 100 ICs; 18 Mbps maximum data transmission speed; 40-pin ceramic DIL package; sampling at ¥10,000 ($71.42)

  - Two V25 family 16-bit MCUs; one model with 16 Kbytes of ROM (MuPD70322) and one without ROM (MuPD70320); architecture differs from V20-V50 family, but design and software compatible; 7.7 x 12.3mm chips; 1.5-micron CMOS process; 255,000 elements; 5- or 8-MHz clock speeds; sampling at ¥8,000 ($50); plans to introduce a V25 device incorporating an I-TRON operating system for industrial equipment and 2.4 microsecond switching capability in 1987

  - A CRT controller IC (PD72022) with built-in, 8-bit MPU; sampling at ¥8,000 ($57.14)

  - A single-chip LSI (PC1095G) for 5.25- and 3.5-inch floppy disk drives; sampling at ¥850 ($6.07)

  - An Ominet LAN protocol I/II CMOS controller (MuPD72105); 8/16-bit CPU; 16-Mbyte memory; 48-pin DIP or 52-pin PLCC

  - A single-chip, hard disk controller (PD7262) based on ESDI specifications; sampling at ¥10,000 ($71.42)

- Mitsubishi--A 48-port, parallel interface (M5M82C255ASP) and 24-port interface (M5M82C55AP-2); 64-pin shrink DIP; sampling at ¥1,500 ($10.70)

- Oki Electric--A CMOS, 8-bit, single-chip MCU with self-contained 16K CMOS EEPROM; 5.0 x 4.5mm chip size; 4.9-MHz clock frequency; 813.8ns execution time; 3-Kbyte program ROM capacity; 512-byte ROM; internal testing, EEPROM control programs; 95 commands usable for IC cards; sampling at ¥5,000 ($35.71)

- Sony--Six MCU models (SPC500 Series); CXP50P48 with built-in, 8-Kbyte PROM, 288-word RAM, sampling at ¥3,000 ($21.43); CXP5058 with 8-Kbyte built-in ROM, 384-word RAM priced at ¥900 ($6.42); CXp5056 with 6-Kbyte ROM priced at ¥800 ($5.70)

Digital Signal Processors (DSP)

- Hitachi--An 8-bit image processor with 2-Kbyte line buffer storage; three parallel I/O ALU ports; 40ns cycle time; 512 x 512 screen image; 1.8-micron BICMOS process

  - Two high-performance, 16-bit CMOS signal processors; 32-bit ALU timing register; 250ns instruction cycle; HD81810 featuring 200 x 16 RAM and 128 x 16 or 512 x 22 ROM; HD61811 featuring 200 x 16 or 512 x 22 RAM

  - A pulse-processing LSI (HD63140); 15 types of MCUs; 16-step memory possible; 16-bit usable registers; 16-bit A/D with 10 channels; 1-Kbyte CMOS SRAM; 2.0-micron CMOS process; 7.3 x 7.2mm chip; 64-pin plastic shrink DIP priced at ¥3,050 ($21.79); 68-pin PlCC priced at ¥3,700 ($26.43)

- Japan Digital Laboratory (JDL)--A vector-to-raster protocol converter (GL Processor) capable of converting Toshiba's P351C and Fujitsu's DPL24C printers into pen plotters; priced at ¥200,000 ($1,290) for Model 15 with 1.5 Mbytes of memory and ¥262,000 ($1,637) for Model 30 with 3 Mbytes of memory

- Matsushita Electric--A 10ns, real-time image signal processor (RISP-II) developed using Matsushita's new Vertically Isolated Self-Aligned Transistor (VIST) technology; 20,600 elements integrated on a single chip; 3- x 3-pixel image register programmable for repeated use in industrial robots, production-line monitoring, medical equipment, and AI; sampling at ¥250,000 ($1,560)

- Mitsubishi--Seven DSP LSIs incorporating the functions of 800 ICs for use in PD-format, professional-use, dual-channel, digital tape recorders; 1.7- to 2.0-micron CMOS process; servo control, editing, digital-signal error correction, recovery, and synchronizing signal oscillation functions offered

- NEC--A single-chip, 4-bit MCU (MuPD17P00) with OTP ROM for radio and TV tuners; MuPD17P19 for FM/AM radios; 2Kx16 OTP, 256 x 4 RAM, LCD driver; 64-pin plastic package; sampling at ¥4,000 ($28.57); FM/AM radio tuner IC (MuPD17P0S/13) sampling for ¥4,000; VTR circuit (MuPD17P16) for ¥2,000 ($14.26); AM radio tuner (MuPD17P20) for ¥3,000 ($21.43)

  - Two CMOS signal processors; a 16-bit type (MuPD7720); 250ns, 512-word ROM, 128-word RAM, 28-pin DIP/44-pin PLCC; a 32-bit type (MuPD77230); 150ns; 512 x 2, 68-pin PGA

  - Two graphics controllers; 256Kx16 type (MuPD7220) featuring 8-MHz clock, 137,000 transistors, 500ns/image speed, 2-micron NMOS process, 4.34 x 4.27mm chip, and 40-pin DIP; 16M x 16-bit type (MuPD72120) with X-Y address, 250ns/16-bit speed, 8-MHz clock, 175,000 transistors, 10.6 x 12.7mm chip, 1.6-micron CMOS, and 132-pin PGA, 88-pin FLP, and 84-pin PLCC

- Sony--Eight LSIs for compact disk players; 3 DSP circuits, a servo signal processor, PWM driver, 16-bit D/A converter, and 13-bit DA converter; priced from ¥400 ($2.50) to ¥3,400 ($21.25)

- Tohoku University--A coordinate conversion processor LSI for robot manipulator controls; 2-micron CMOS process; 14,000 transistors; 16-bit data length; 20-bit internal data processor

Speech Recognition/Synthesis Chips

- Matsushita--A sound generator IC (DN8600) for personal computers; TTL-level compatibility; 24/16mA I/O; 250mW power consumption; BICMOS process; 5.0 x 4.9mm chip; 64-pin flat package; ¥1,500 to 2,000 ($10.70 to 14.30)

- MITI Electrotechnical Laboratory--Simple voice recognition equipment capable of recognizing 220 words with 97.7 percent accuracy; 2,354 standard sound patterns

Application-Specific ICs (ASICs)

Japanese companies are actively opening new design centers overseas, as shown in Table 3:

Table 3

NEW OVERSEAS JAPANESE DESIGN CENTERS

DATE	COMPANY	U.S.	EUROPE
05/87	Matsushita		Singapore
12/86	Oki Electric		Finland Norway Italy Switzerland Denmark
12/86	Ricoh	San Jose, CA	
10/86	Sharp	New Jersey	

Source: Dataquest
June 1987

- Fujitsu--A BICMOS, 2,080-gate array; 3-input NAND; 0.9ns internal gate delay time; 250-microwatt/gate power dissipation at 10 MHz; TTL I/O level; 1.5-micron process; orders from second-half 1987

- Hitachi--A Hi-BICMOS gate array family (HG28 Series); 630/864/1008/1326/1800/2550 gates

- NEC--Two ECL gate array models; 100 and 220ps internal gate delay times under standard load conditions (fan-in and fan-out of 3, 3mm wiring length); 2.1-GHz toggle frequency; power supply voltage of -4.5V or -5.2V; 132- and 72-pin PGA packages; 600-gate model (MuPB6303) featuring 88 inputs and 48 outputs; ¥4.5 million ($32,140) development cost; unit cost of ¥10,900 ($77.86) for 1,000-unit orders; 1,200-gate model (MuPB6312); with 108 inputs and 48 outputs; ¥6.5 million ($46,430) development cost; unit cost of ¥16,000 ($114.30)

- BICMOS, 4-family gate arrays; 600 to 3,100 gates, 0.8ns

- Three ECL gate array families; ECL-2 Series (300-gate/0.5ns, 1200-gate/0.7ns, 2000-gate/0.7ns); ECL-3 Series 3 types (1,200 and 2,000 gates/1.0ns; ECL-3A Series (4,000- and 5,000-gate/ 0.7ns)

- Ricoh--Gate arrays with built-in memories (5GF Series); 2100/2600/ 3200/4500/5800/8200 gates; built-in ROMs from 4K to 16K; built-in RAMs from 2K to 8K; 60ns ROM readout time; 55ns RAM readout time; 2,100-gate array development cost of ¥3 million ($18,750); unit prices of ¥560 ($3.50)

- Sharp--A line of 59 CMOS logic cells for future high-definition TVs; a ¥930,000 ($6,000) high-definition TV prototype possible using 5 LSIs to handle data processing circuits; 0.58ns per gate delay time (compared with 0.7ns for standard ECLs) and power consumption 1/100th that of ECLs

- Toshiba--"Sea of Gates" 50,000-gate array; 1.5-micron HCC-MOS/VLSI process; 0.7ns access time; TC110G Series

CAD Systems

- Hitachi--A CAD system for automatically converting gate-level logic circuits; M200H computer used for 1,500-gate ECL arrays; M680H for 2,000-gate ECL arrays; gate count increased by 0.3 percent, but design time reduced by 50 to 70 percent

  - A logic simulation system (VELVET) using Hitachi's S-810 supercomputer; event-level, gate-level simulation method; 6 vector instruction types; 1/100th the time for input pattern compiler simulation

  - A C-language compiler (HS180VCLV1SF) for 8-bit MPUs (HD64180); VAX-11 using VMS 4.2 operation system; MMU with HD64180 support; 1 Mbyte memory space; ROM-based programming feasible; priced at ¥55,000 ($392.85)

- NEC--A CAD system for standard-cell channel routing, capable of reducing channel length and width; polysilicon 1-layer, 2-layer metal

  - Cybernet system LSI design CAD system for logic simulation using NEC PC-9801; DESIGN PRO II CAD software; 640-Kbyte memory required; DOS Ver 2.1 and above operation system; ¥1.45 million ($10,357) for design input; ¥980,000 ($7,000) for logic simulation

- NTT--An LSI expert CAD system for automatically developing standard cell macrocells; Japanese-language-processing contents; DEC2060 computer used

- Sanyo--A gate array CAD layout system offering memory cells, decoders, and drivers; automatic layout derived from designating bit-word memory structure; 4K RAM and 4,500-gate random logic used to develop 15,000-gate array with same size as current 8,000-gate arrays

- Sharp--A CMOS logic cell for TV-signal-processing LSIs; encoder/decoder using MUSE method; 2-level interconnect; tungsten silicide gate electrodes; 1.2-micron CMOS process; 0.58ns gate delay time; 110- x 180-square-micron cell size; highest operating wavelength 70 MHz and above

- Soliton Systems--Automatic IC design software developed with Silicon Compilers of San Jose, California

- Toshiba--A VLSI-design-integrated simulation system, adaptable up to 0.25-micron geometries and 64Mb DRAMs; 4 types of software including a layout processor, form simulator, an ion implant and diffusion simulator, and device characteristics evaluation simulator; design evaluation within 1 to 2 hours; used at Toshiba's Electronic Engineering Center in Kawasaki, Kanagawa Prefecture since March 1987

Optoelectronics

- Fujitsu--A 1.3-micron LED for single-mode optical-fiber communication; 20km repeaterless transmission successfully tested at a data speed of 600 Mbps; GaAs FET drive circuit and compensation circuit included in the LED

- Hitachi--Five photodiodes; 50/80/100/300 microns and 3mm bandwidths; 100- and 300-micron devices for monitoring laser diode output; 3mm device for measuring instruments; sampling 50 to 300 micron devices for ¥28,000 ($175) since September; 3mm diode to be sampled shortly at ¥200,000 ($1,250)

- KDD--A 1.52-micron InGaAsP/InP direct feedback (DFB) semiconductor laser; optoelectronic IC built onto an InP substrate; 500mA electrical current; 5-micron wide stripe; 670-micron laser length

Technology Trends--Fourth Quarter 1986

- Matsushita Electron--A new laser diode production process that forms a submicron light-generating area, opening the way to developing quantum lasers for communications systems; MOCVD method with a self-alignment process used to grow crystal on a 2-micron reverse-trapezoid "bump" at 54-degree angles on both sides of the bump; an experimental 1-micron stripe GaAlAs semiconductor laser with 15mA threshold current and 1.05 ellipticity; one epitaxial growth operation; plans to commercialize a 0.8-micron stripe laser for short-distance optical communication

  - A blue, light-emitting laser diode developed using a second harmonic generation (SHG) element that reduces the laser wavelength to one-half of its original level; lithium niobate crystal used in the SHG element; 0.83-micron wavelength light generated by combining the SHG element with a laser diode; 25 percent conversion efficiency at 1W output and 1 percent at 40mW; an optical disk with four times the memory density possible by using a 0.415-micron wavelength diode; plans to sample a laser and SHG element on a single chip for future optical storage systems and laser printers

  - World's first AlGaAs optoelectronic IC (OEIC) containing a semiconductor laser, 25 MESFETs, and 18 diodes; 30mW oscillation output and 830nm wavelength; 0.35 x 1.2mm chip; integrated with high-frequency circuit for laser noise reduction; U-shaped groove with 10-micron depth and 400-micron width, and two ridges with 1.5-micron height; 5-micron gap at bottom of groove; liquid-phase, epitaxial growth process; suitable for optical disks

  - A monolithic laser diode integrating a reading laser and a writing laser on a single chip; designed for optical disk systems; more economical optical systems easier to develop due to narrow beam interval

- Mitsubishi Electric--A GaAs variable-waver laser diode that emits two different wavelength signals by changing currents; quantum well layout sandwiching a GaAs center layer with 48 AlAs and GaAs layers doped with impurities and stacked alternately; central GaAs layer 10nm thick and 410nm wide; 843nm light emitted using 150mA current and 803nm light using 190mA; for use in doubling optical disk recording densities and optical communication multiplexing

  - A flush semiconductor laser by MOCVD process, applying self-alignment to crystal growth; reverse semipyramidal structure layered on GaAs substrate at 54-degree angle; submicron stripe possible using MOCVD; test manufactured 1-micron stripe GaAs laser with 15mA threshold current; plans to market 1-micron GaAs laser within 1 to 2 years

Technology Trends--Fourth Quarter 1986

- NEC--A single-frequency, 1.5-micron-band semiconductor laser for 300km optical communications and cable TV transmission

  - A 24-GHz GaAs/AlGaAs multiquantum-well semiconductor laser; GaAs 10nm active layer; AlGaAs 5nm layer; MBE method; amplifier developed using reactive ion etching (RIE)

- RHD (a R&D joint venture of Nisshin Steel, Toyo Ink, and Mitsubishi Corp.)--Bridgeman method for growing zinc selenide for blue LED materials; 26cm-long x 5cm-diameter crystal raised in laboratory; polycrystal ZnSe melted in a crucible using a graphite heater, then seed crystal placed in bottom of pot, slowly rotated, and raised while temperature, rotational speed, and pressure controlled by computer

- Sanyo--A GaAlAs semiconductor laser with 80 percent efficiency; an aluminum composition alteration technology (GRIN-SCH architecture), uses molecular beam epitaxy (MBE) to grow crystals; 880nm wavelength; 95 percent internal quantum efficiency; 40mA oscillating threshold current; for use in short-distance optical communication

- Sharp--A VSIS-structure (V-channeled Substrate Inner Stripe) semiconductor laser; 25mA threshold current at 780nm visible zone; volume production in 1987

- Toshiba--An InGaAlP laser diode for high-vision optical videodisk players using 1,125 scanning lines; 656nm wavelength (versus 780nm for conventional diodes); 0.8-micron beam spot; 1mW output; 40dB image SN ratio; line speed of 15 meters per second; for use as light source in laser printers, point-of-sale systems, and other optical systems

  - A 656nm InGaP semiconductor laser for high-resolution TV videodisks; MOCVD method; InGaAlP ridge-guide structure

  - An ultrahigh-speed GaAsAlAs optoelectronic IC (OEIC) usable in memory and logic circuits; LED and amplification functions; critical for developing optical computers with 100 times the speed of existing supercomputers using 10 parallel processing OEIC devices; 1ns signal-processing capability; 200mW output; no immediate commercialization plans

  - Three high-output LEDs (TLRC281/TLRA280/TLRA281) with forward current IF of 30mA and 660nm wavelength; for use in plastic optical fibers; a high-conversion-efficiency PIN photodiode (TPS721) with 2.0mm light detector for 0.4A/W conversion rate using 1mm diameter fiber

- Tokyo University--A prototype optical computer featuring 10 lenses, 9 LEDs, and 9 light-receiving diodes; theoretically capable of 100 GFLOPs; information processed in a 2-dimensional image, with each numerical value in the matrix expressed by the light intensity, but there are read-out errors since alphanumeric values are represented by light intensity; for use in future image processing

Image Sensors

At the 1986 Electronics Show, Japanese semiconductor makers introduced the following charge-coupled devices (CCD), which are being used in 8mm video cameras and optical readers, as shown in Table 4.

Table 4

JAPANESE CHARGE-COUPLED DEVICE (CCD) ANNOUNCEMENTS

Maker	Model	Method	Pixels	Chip Size	Resolution	Structure
Hitachi	HE98241	2/3"	576 x 485	8.0 x 9.9	380	TSL
Matsushita	MN3731F	2/3"	574 x 499	8.7 x 9.9	380	IT-CCD
Mitsubishi	M50241	1/2"	510 x 489	7.0 x 8.1	320	CSD
NEC	PD3530D	1/2"	512 x 492	8.0 x 6.8	380	IT-CCD
	N/A	1/2"	768 x 492	6.5 x 7.7	380	IT-CCD
Sanyo	LC9915	2/3"	770 x 487	10.8 x 10.4	560	FT-CCD
	LC9931	1/3"	384 x 490	7.6 x 6.2	280	FT-CCD
Sharp	LZ22250	2/3"	530 x 490	8.4 x 10.0	300	IT-CCD
Sony	ICX030AK	1/2"	510 x 492	8.1 x 6.4	330	IT-CCD
	ICX022AK	2/3"	38,000	N/A	N/A	IT-CCD
Toshiba	TCD215C	1/2"	570 x 485	6.5 x 7.7	350	IT-CCD

Note: Interline transfer CCD (IT-CCD)
N/A = Not Available

Source: Nikkei Electronics
Dataquest
June 1987

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- Hitachi--An MOS TSL (horizontal readout) state-state image device for PAL video systems; 600 x 582 pixels; 576 x 575 effective pixels; 360 horizontal TV lines x 420 vertical lines; 10 lux sensitivity; 5V driving power; vertical and horizontal switching device for each pixel; specialized driver IC (HD62990); sampling at ¥25,000 ($178)

- Matsushita Electronics--A CCD image sensor with a reading width of 77mm and resolution of 400 lines per inch (MN3656); contact-type image sensor for compact facsimile and plain-paper copier systems; priced at ¥5,000 ($31.25)

- NEC--A one-half inch color image sensor with 512 horizontal picture elements; sampling for ¥20,000 ($125); initial production of 10,000 units monthly; 100,000 units/month during 1987

- Sanyo Electric--A two-thirds inch image sensor for monochrome applications; 560-line horizontal resolution and 400,000 picture elements; sampling for ¥27,500 ($171.90)

  - An NTSC one-half inch color CCD solid image device with 300,000 picture elements; 280 horizontal TV line resolution; 8.1 x 9.3mm chip; 10 lux minimum intensity using F1 lens; for use in 8mm videocameras

  - Mass production of 802,400-pixel CCDs for solid-state, image-sensing devices for single-unit, videocamera/recorder systems; Sony, NEC, Matsushita, and Toshiba also producing CCDs

- Sony--Two CCD image sensors (ICX030AK/ICX030AL); 7.75mm effective image area for one-half-inch optical systems

- Toshiba--A color image sensor (TCD215C) with 300,00 picture elements on a one-half-inch chip; 1.5 times more sensitive than a 200,000-element sensor; one-half inch monochrome and two-third inch monochrome and color versions; NTSC compliance; 570 horizontal elements; 350 horizontal and vertical TV line resolution; 20-pin ceramic DIP package; sampling for ¥20,000 ($125)

- Yazaki Machinery--A gas sensor for detecting incomplete combustion in heating systems; 3.0 x 4.0 x 1.0mm device consisting of several types of powders, including tin oxide, lanthanum oxide, strontium carbonate, and barium oxide; capable of detecting carbon monoxide fumes of 100 parts per million; priced at ¥1,000 ($6.25)

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Gallium Arsenide

- Fujitsu--Four GaAs prescaler ICs; MB50104/106 for microwave telecommunications; priced at ¥15,000 ($107) and ¥30,000 ($214) respectively; MB50201/202 for portable mobile radio communication systems priced at ¥5,000 ($35) and ¥9,000 ($64) respectively; volume production of 50,000 to 60,000 units monthly since the spring 1987

  - A 6.5-GHz GaAs IC, utilizing a MESFET with 200ms/mm conductance; 0.8-micron gate length; sourced-coupled FET logic (SCFL); 95mA operating current; 14-pin ceramic package; sampling since December 1986 at ¥30,000 ($214.29); 2.3GHz, 1.2- to 1.3-micron device sampling at ¥9,000 ($64.28)

- Matsushita Electric--A GaAs prescaler (MB50106) that converts 6.5-GHz high-frequency signals to less than 1 GHz; 3 times the frequency conversion rate than conventional silicon devices; sampling at ¥30,000 ($187.50) since October 1986

- NEC--A 45-GHz AlGaAs/GaAs heterojunction, bipolar transistor; MBE growth method; 17-GHz toggle frequency

  - A GaAs MMIC series (MuPG100B/101B); 50 to 3 GHz; 3dB noise gain and below for MuPG100B; 1dB for MuPG101B

- Sumitomo Electric--A new method for crystallizing GaAs of 20cm without flaws; plural cell heaters and computer-control system adopted to analyze specific gravity, buoyancy, and surface tension of the crystal while fine-tuning the heat

Josephson Junctions

Superconductors

- Tokyo University--A ceramic material with superconducting properties at 243 degrees Celsius; mixture of barium in a matrix of lanthanum and copper oxide to form a perobskite; for use in future supermagnets for nuclear fusion and linear motor trains; team led by Professor Shoji Tanaka of the University's Engineering Department

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Ballistic Transistors

- Fujitsu--A high-speed, resonance-tunneling, hot-electron transistor (RHET) developed using a AlGaAs/GaAs superlattice structure; 50-angstrom-thick AlGaAs layer sandwiched between layers of 56A thick GaAs; for use as either logic or memory circuits in future supercomputers and AI machines; developed through MITI's Supercomputer Project

- Kyoto University--A hot-electron transistor (HET) made by stacking layers of crystalline GaAs film in a superlattice arrangement; glow discharge technique used to break up silane and ethylane gases with high-frequency electromagnetic waves and deposit thin films of amorphous material on a single-crystal silicon base; superlattice structure of 200-angstrom-thick amorphous silicon and 40-angstrom-thick silicon carbide; team led by Professor Hiroyuki Matsunami of Kyoto University's Engineering Department

- Sharp--Two types of field-effect transistors (FETs) using silicon carbide (SiC), paving the way for MCUs in automobile engines; MOCVD method used to grow high-quality monocrystals; junction-type FET and insulation-type FET; bottom layer of boron-doped, P-type, SiC monocrystals and channel layer of N-type, SiC monocrystals; mutual conductance factor of 40

New Semiconductor Functions

No major announcements

Power ICs

- Hitachi--A 350V MOS power IC; PNP and NPN bipolar transistor; P-channel MOSFET; 325 x 280 square microns

- Matsushita--Fourteen power MOSFET models; 15 and 20A in 400/450/500 withstand voltage; 30 and 50A in 50/60/100/120 withstand voltage

- Tokyo Sanyo--A chopper 5V output power IC series, a 100-KHz switch power series, and two half-bridge, high-output series with 400mW maximum output

Standard Logic

- NEC--High-speed, CMOS, standard logic (MuPD74HC Series); 14/16/20 pin types; 225 and 300 mil flat packages

- Toshiba--Ultrafast, CMOS standard logic (TC74HC00A); 30 percent faster than TC74HC series; 3ns 3-stage gate delay time; 24mA output current; 1.5-micron process with 2-layer metal wiring; 50 models by spring 1988 and 250 models within 2 years

- Sanyo--A bipolar, power IC series for car stereo systems (LA44 series); LA4480 with 4W x 2 output and 12-pin SIP package; 4 models with 12W outputs and 10- to 18-pin packages

  - A Dolby-B circuit hybrid IC (STK2735B); 50-micron minimum linewidth pattern on 2 aluminum substrates connected with flexible wiring

  - Two hybrid IC series for audio equipment power output circuit use (STK4044 series)

Hybrid ICs

- Sanyo--A hybrid IC-driving circuit (STK66000) for dot-matrix printers, allowing replacement of double-sided, printed-through-hole PCBs with single-sided PCBs; 31 x 64 x 8.5mm; 27 pins; sampling at ¥15,000 to ¥20,000 ($107 to $143)

Linear/Analog

- Hitachi--Six digital, audiotape LSIs; 16-bit A/D converter; 3 CMOS types; 3 bipolar types; 48/44.1/32 KHz versions; 860mW power dissipation

- Mitsubishi--A/D and D/A converter ICs for VCR special effects use, such as still picture and slow motion; a high-speed, 6-bit A/D converter IC (M52678P) with built-in clamp-pulse-generation circuit and 250mW power consumption; a high-speed D/A converter (M52679P) with 150mW power consumption; 20- and 18-pin DIL packages; A/D priced at ¥1,000 ($7.14), D/A at ¥400 ($2.85)

Telecom ICs

- Fujitsu--A general-purpose CMOS processor for ISDN terminals; 9,800 gates on a 9.3 x 10.2mm device; capable of sending separate voice, image, and data signals as a single package, and processing and dividing inputs into separate signals for voice and data; 384,000 bps transmission capacity

- Oki Electric--An I-interface ISDN LSI; 2-micron CMOS process; 12,000 gates; 8085 MPU and SRAM; frame-check sequence; 256-Kbyte SRAM; 176-pin PGA; sampling since March 1987

- Rohm--Two speech network ICs featuring dynamic range boosting and speech amplification; BA6563K in 44-pin, quad flat package; BA6566F in 18-pin SOP

Transistors

- Mitsubishi--A monolithic current-driving transistor array to drive motors, relays, and solenoids; increased withstand voltage and low saturation output; 20 and 80V output voltages; 12 models; 4-circuit devices in 16-pin DIL packages and 2-circuit devices in 8-pin SIL packages

- Sanyo--Thirteen models of TO-220 miniflat-packaged power transistor for large current switching

New Processes

- Hitachi--A Bloch line memory with potential for gigabit memory chips; a 6mm square chip of gadolinium-gallium-garnet (GGG), thin layers of magnetic garnet, and polyimide resin coating; gold electrodes; 1 bit stored in device with 0.5- to 1.0-micron width and length, enabling 1Gb device on a 1cm chip; based on idea of Kyushu University's Professor Susumu Konishi

- Tokyo Institute of Technology--A high-polymer material painted onto a base material to produce P- and N-type semiconductors; polyacrylonitryl (PAN) mixed with a copper sulfide solvent for P-type base; cadmium sulfide solvent for N-type device; toxic pollution problems with cadmium sulfide requiring more acceptable material; research team headed by Professor Koichi Yamamoto

Materials

- Japan Synthetic Rubber--Positive electron-beam resist (PFR7700) for 0.8-micron geometries; electron-beam resist MES-E; negative X-ray resist MES-X with 0.4-micron resolution and 1.0-micron coated film thickness

- Matsushita--A new photoresist material using Langmuir and Blodgett technology that allows submicron patterns with excimer laser or X-ray lithography systems; experimental 0.3-micron wide pattern drawn using a 248.3nm excimer beam; experimental 0.4-micron wide pattern using X-ray lithography; 0.1-micron patterns theoretically possible by improving the mask; for use in developing 64Mb DRAMs

- Sanyo Electric--An ultrasensitive, positive electron-beam resist for fabricating 4Mb memories and above (SEBR-115); 100 times the sensitivity of conventional positive-type EB resists used in VLSI fabrication; circuit-pattern, writing resolution of 0.75 micron; conventional polymethacrylic acid methyl acrylate (PAMA) converted into an amorphous material by applying tetrabutyl ammonium perchlorate

- Toshiba--A new, monocrystal material (lithium quadriborate) for surface acoustic wave (SAW) substrates; SAW filters with 3 times the range of conventional filters developed on 3-inch wafers

  - An ultrahigh-resolution photoresist material for 16Mb DRAMs; double-layer type for ultraviolet ray lithography systems; capable of 0.5-micron geometries; a double-layer resist consisting of a nonphotosensitive polymer and photosensitive polymer; possible to develop high-resolution resists for 1Mb using water-soluble organic amines

Manufacturing Processes

- Matsushita--A KrF excimer laser capable of 0.4-micron patterns; 248nm wavelength; 5:1 reduction; 10 x 10mm-square pattern on wafer

- NEC--A high-power excimer laser using kryton flourine (KrF); 30W average output; for use in isotope separation and surface-treating new materials

- Nikon--Success in drawing 0.35-micron linewidth circuits by combining conventional stepper and multilayer resist technologies; adaptable to 64Mb DRAMs

- Osaka University--A mirror for X-ray laser emitters that can reflect with high-efficiency electromagnetic waves; superlattice structure 40- to 200-angstrom-thick consisting of 100 alternating layers of silicon and molybdenum; an electron beam used to vaporize and deposit these thin films on a silicon base; 30 percent reflection factor and surface variations less than 7 angstroms using a precision-control, multilayer, thin-film growing technique; jointly developed by Jojun Yamashita, assistant professor of Osaka University's Faculty of Science, and Professor Yoshiaki Kato of Osaka University's Institute of Laser Engineering

Manufacturing Equipment

- Anelva--A reactive ion etcher (ILD-4031) for up to 4Mb DRAMs; cassette-to-cassette-type, single-wafer processing capability; high-speed and high-etching selectivity; cathode-coupling process permitting etching speed of 6,000 angstroms per minute; polysilicon film or silicon oxide film available; 30 six-inch wafers processed per hour; priced at ¥60 million ($428,570)

  - An inline plasma CVD (ILV-9001), inline sputtering system (ILC-1015) and single, high-speed reactive ion etcher (ILD-4031)

- Fujitsu--An electron-beam VLSI tester capable of reading information at speeds up to 1ns (compared with 10ns for existing testers); electrical voltage on the wiring and electrodes measured by irradiating the circuits with an electron beam and analyzing the secondary electrons generated; 23ps irradiation time; 5ps irradiation cycle; for use in future megabit VLSIs

- Hitachi--An analyzer capable of detecting dust particles with 0.3-micron diameters; wafer surface scanned with helium-neon laser; electronic images of dust particles obtained by scanning electron microscopes (SEMs); X-ray dust particle microanalyzer unit; scanning time of 12 minutes for 5-inch wafers and 22 minutes for 6-inch wafers

  - A stepper for 4Mb DRAMs; 365nm wavelength; one-fifth circuit pattern reduction ratio; Carl Zeiss lens used

  - A mask inspection machine (PD1000) capable of detecting 1-micron particles on masks and reticles; priced at ¥50 to ¥60 million ($357,145 to $428,570)

- Kokusai Electric--A CVD system with 6 reaction tubes (DD-800V) and automatic drive process system (DV-8000)

- Matsushita Electric--A holographic wafer stepper for precision positioning of the reticle over the wafer; positioning accuracy of less than 0.1 micron for use in fabricating 16Mb DRAMs; laser interference stripes formed between the alignment grids of the reticle and wafer; a pair of Fourier conversion lenses and a space filter incorporated into the system

- NEC--A laser CVD system for photomask repair (Laser Maskrepair SL454A); YAG laser employed to irradiate chrome carbonyl vapor to deposit chrome molecules that produce a chemical reaction to cover white, defect spots on a mask with a chromic film; 25-micron-diameter white spots repaired in less than 30 seconds in a single operation; priced at ¥120 million ($750,000)

- An experimental synchrotron orbital radiation (SOR) lithographic system for drawing 0.25-micron geometries for 64Mb DRAMs; successfully tested at the Ministry of Education's High Energy Physics Laboratory that operates a Synchrotron Radiation Facility in the Tsukuba Science City; X-ray beams produced by SOR systems require shorter exposure time than conventional X-ray systems do because of 1,000 time stronger light source; a mirror of silindum used to direct the X-ray beam uniformly onto the wafer; successful drawing of a pattern 3.0-microns high and 0.25-micron thick; capable of processing wafers larger than 20cm square

- Nichicon Capacitor--A gas-injection, plasma, X-ray source system for submicron lithography; developed with NTT for 16Mb DRAMs using 0.5-micron geometries; hollow, cylindrical gas formed by passing high electrical power (100 to 300kA) through a high-speed switching gas valve; 0.3-micron pattern transferred to unit in 13 seconds using FBM-G resist on an exposure area of 30mm square; priced at ¥120 million ($857,143)

- Nikon--A conventional optical stepper with 0.35-micron design rule resolution for 64Mb DRAMs; 436nm wavelength light; 0.6 lens aperture setting; 3 to 4 resist coatings on the silicon substrate

- NTT--A plasma X-ray source for designing megabit memories up to 64Mb with 0.3-micron design rules; 0.9 to 1.4nm wavelength; a strong electric current passed through neon gas in a vacuum chamber to split neon atoms into ions and electrons; 200ns X-ray emissions repeated in this process

- Sony--An automatic, reticle-quality evaluation system (ARQUS-20) built around a CCD sensor featuring 250,000 picture elements; capable of detecting flaws over 0.8 micron; inspection speed of 11 minutes for 1cm square; priced at ¥80 million ($500,000)

- Tokyo Ohka--An ECR etching machine (TSME-5300) adaptable to 4Mb DRAMs; 40 six-inch wafer starts per hour; etching speed 3,000-angstroms per minute

- Toshiba/Tokuda Works--A fully automated reactive ion etching system (HIRRIE-500) designed for sub-0.5-micron design rules for memories up to 64Mb; capable of handling 8 to 10 wafers at a rate of 20 wafers per hour; priced at ¥92 million ($575,000)

- A step-and-repeat exposure system utilizing synchrotron orbital radiation (SOR) technology for 64Mb DRAMs; 0.03-micron alignment precision; vertical wafer alignment system utilized; plans for commercialization in 1990

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Test Equipment

- Advantest--An ultra-LSI test system (T3381) capable of testing 512 pins at 100-MHz rate and 256 pins at 200-MHz rate; also T3319 and T3128 test systems and T7361 analog LSI test system for high-flash A/D converters; parametric test system T6521/6520

- Ando Electric--An ultra-LSI test system (DIC-9035) for 512 pins at 100MHz test rate, compact DIC-8034E/E for 256 pins at 40/20MHz, high-speed parametric system (DIC-8055) for 128-pin ICs, and automatic handler (AHM-645L/646HB/671(HC)/750H)

- Sony Tektronix--An ultra-LSI test system (LT-1000) for ASIC production, an ultra-LSI verification system, and a color, digital analysis system (DAS9200)

Packaging and Interconnection

- Matsushita--A method for raising the thermal properties of IC package resins by reducing impurities

- NEC--Emboss-carrier taping method for PlCC, miniflat, and other surface mount IC; 0.5 second per IC mounted; 2,500 ICs stored per emboss tape reel

- Taiyo Yuden--Copper for ceramic multilayer substrate wiring; substrate of compound alumina-based ceramic sintered at 950 degrees Celsius; thermal expansion coefficient similar to that of mounted silicon chips; 11 RAM modules containing up to 8Mb of DRAM using these low-cost substrates

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COMMENTARY

Japan Enters the Superconductor Race

Caught offguard by the sudden and rapid series of breakthroughs by U.S. and European superconductor researchers, Japanese companies and government ministries are bolstering their capabilities in basic and applied superconductivity research.

In April, the Science and Technology Agency (STA) announced plans to organize a superconductor R&D program involving government, universities, and private industry. Plans include the conversion of the New Superconductive Material Research Committee into a full-fledged corporation and the establishment of a separate Superconductive Material Research Center. The program is tentatively budgeted at ¥10 billion ($71.4 million).

Nonferrous metal firms are also rushing into the rare earth market because of the rapidly growing demand for R&D materials. Major players include Asahi Chemical, Kawasaki Steel, Mitsubishi Chemical, Nippon Steel, Shin-Etsu Chemical, Sumitomo Metal Mining, and Toyo Soda. According to the Japan Society of Newer Metals, Japanese rare earth production in fiscal 1985 totaled 4,390 tons, worth an estimated ¥30 billion ($214.3 million). More than 90 percent of this material went into glass and abrasives. Japan accounts for 60 percent of world rare earth consumption.

JSIS will issue a special report on Japanese superconductor efforts this autumn.

MAJOR TECHNOLOGY TRENDS

During the first quarter of 1987, Dataquest observed the following trends in Japanese semiconductor technology:

- The Management and Coordination Agency reported that Japan's spending on scientific research grew by 12.60 percent to ¥8.89 trillion ($63.5 billion) in fiscal 1985, or 2.77 percent of the GNP, versus ¥25.95 trillion ($185.3 billion) for the United States (2.72 percent).

- MITI added ceramic IC packaging to a list of 15 strategic goods whose exports to communist countries will be controlled by MITI under the Coordinating Committee for Export to Communist Areas (COCOM).

- Japan will finance half of the ¥1 trillion ($7.1 billion), 20-year Human Frontier Science Program designed to promote basic life science research.

- MITI has budgeted the Biochip Project at ¥150 million ($1.1 million) in fiscal 1987.
- MITI is assisting in the formation of two new R&D associations, the New Glass Forum for high-performance glass and the Optomechatronics Association.
- MITI's Sigma Project ordered 50 workstations and Japanese language software from Fujitsu, NEC, and other Japanese makers.
- MITI requested Japan's 26 major audio firms to replace digital-to-digital recording with audio-to-digital recording in digital audio tape (DAT) recorders, as a counterproposal to the recording industry's proposal for a copy code system that prevents recording of compact disk music.
- Japanese semiconductor makers presented 51 papers (44 percent of all papers) at the 34th annual International Solid State Circuits Conference (ISSCC) in New York City, including 4 papers on megabit DRAMs, 5 on fast SRAMs, and 6 on high-density SRAMs (see JSIS newsletter "ISSCC 87."
- IBM Japan joined MITI's Sigma Project for software development.
- NTT's Atsugi Laboratory is installing a synchrotron orbital radiation (SOR) facility for 64Mb and 256Mb DRAM research.

CORPORATE R&D

Japanese semiconductor makers are investing more in basic research because of the yen appreciation and Asian competition. Hitachi, NEC, and Toshiba recently announced plans to strengthen their R&D facilities, as shown in Table 1.

Table 1

R&D STRATEGIES OF MAJOR JAPANESE COMPANIES

Company	R&D Strategy
Hitachi	Build new Saitama Prefecture Basic Research Lab (begin in 1987 and complete in 1989)
NEC	Increase R&D budget (5.3% in 1982, 5.8% in 1983, 6.4% in 1984, 7.7% in 1985, and 8.0% in 1986)
Sanyo	Build new basic research center in the Tsukuba Science City area
Toshiba	Initiate STEP 90 Plan and reduce product development time

Source: Dempa Newspaper
Dataquest
August 1987

GOVERNMENT R&D PROGRAMS

MITI Future Electron Devices Project

MITI's Future Electron Devices Project is making progress on 3-D ICs. Progress has been made in several areas, including basic 3-D device technology and test manufacturing and laser recrystallization of polycrystal crystal for silicon-on-isolation (SOI) layering. The SOI process, in which polycrystal silicon is formed onto an insulation layer by sputtering or chemical vapor deposition (CVD), uses a laser to recrystallize the polycrystal into a single crystal substrate. MITI is also exploring three technologies to supplement this process:

- Smoothing of second- and higher-layer wiring to form silicon oxide evenly on the multilayer wiring on the first layer, using one of three processes: organic polymide base resin, bias sputter, and spin-on-glass (SOG) application
- Turning thin-film polysilicon into single crystals
- High-purity metal gases for CVD equipment to improve thin film characteristics

Optoelectronics R&D Association

In February, the Optical Industry Technology Association formed a working group to investigate the opportunities for an optical information system at Osaka's Flower Exposition in 1990. Approximately ¥4 billion ($28 million) will be invested in the system, which may introduce next-generation ISDN technology to the public, like the Tsukuba Expo 85.

MITI Supercomputer Project

After heated trade discussions, the Japanese government agreed to require all government ministries and universities to announce supercomputer procurement in the government daily publication, Kanpo. Although the "transparency" issue has been resolved, debate continues over the use of extremely low leasing fees to attract potential customers. Dataquest believes that some form of price guideline could be imposed (following the semiconductor precedent) if Japanese companies continue to aggressively price their products.

In January, Cray Research announced shipment of its X-MP/12 supercomputer to Honda Research Labs, following the previous purchase by Nissan Motors. The supercomputer will be used for structural analysis and engine thermal testing.

MITI New Materials Project

In 1980, MITI designated new materials as one of Japan's next-generation industries. Mitsubishi Research Institute estimates that the new industrial materials market will grow from ¥3.6 trillion ($25.7 billion) in 1986 to ¥4.5 trillion ($32.1 billion) in 1995. Of the 1995 market, new functional materials, including silicon monocrystal and photoresists, are forecast to account for ¥4 trillion ($28.6 billion), whereas carbon fiber, super-engineering plastics, and other structural materials are projected to be ¥0.5 trillion ($3.6 billion). Sharp growth is forecast for optoelectronic materials, aramid fibers, and fine ceramics for car engines. Dataquest observes that the Japan Fine Ceramics Center was recently opened in Nagoya City (near Toyota City and MITI's Nagoya Testing Lab), an area traditionally strong in ceramics. We believe that the recent thrust into superconducting ceramics and other new materials will accelerate growth in these fields.

MITI Optical Materials Project

Sanyo Electric and MITI are jointly developing photochemical hole burning (PHB) technology for optical disks with capacities of 10 trillion bits per centimeter. IBM first announced this technology in 1977. In addition to Japan, PHB technology is being researched in the United States, the Soviet Union, and West Germany.

MITI New Glass Forum

In October 1986, MITI sponsored the New Glass Forum, an advisory group to develop a long-term vision for high-performance glass. Led by Kyoto University Professor Sumio Sakka, the group recently estimated that major applications will become a ¥1.62 trillion ($11.6 billion) domestic market by the year 2000, as shown in Table 2. The New Glass Forum, which has 87 member companies, is headed by Tetsuo Suzuki, president of Hoya Corporation.

Table 2

MITI's NEW GLASS FORUM FORECAST*
(Year 2000)

Applications	Yen (Billions)	U.S. Dollars (Millions)
High-transmission optical fiber	¥ 100	$ 714
Fiber optics for laser surgery, laser machining	40	286
Glass lasers	50	357
Optoelectronic ICs (OEICs)	100	714
Thin-film glass memory	150	1,071
Solar cell glass substrates	100	714
Memory disk glass substrates	300	2,143
Flat-display glass substrates	80	571
Photomask plates	260	1,857
Ceramic-glass composites for multilayer PCBs	150	1,071
New high-strength glass	80	571
High-class porous glass	50	357
Artificial human body elements	160	1,143
Total	¥1,620	$11,569

*Exchange rate used: $1 = ¥140

Source: MITI New Glass Forum

Optomechatronics Association

In April, nearly 100 Japanese makers of industrial materials, precision machines, and electronic devices established an R&D association to promote "optomechatronics," the combination of optics, mechanics, and electronics. Canon, Kyocera, Nippon Sheet Glass, and Sharp are heading up the association.

MITI Fifth-Generation Computer Project

By March 1989, MITI's Institute for New Generation Computer Technology (ICOT) plans to develop a 2 mega LIPS (logical inference per second) system by linking 64 PSI-2 (personal sequential inference) computers in parallel. The PSI-2 is a PROLOG machine being developed by Mitsubishi Electric (see "Technology Trends, 2nd Quarter 1986," page 10).

In January, Mitsubishi Electric announced an AI system for its electricity supply routing support system. The system shows power amounts, destinations, and feeder routes used by utility companies, eliminating the need for load-dispatching engineers through the use of an inference-based data base. This system is also compatible with future power-generation programs and capital spending programs. Hitachi and Toshiba are also developing AI systems for utilities companies.

Matsushita is currently developing a SIMD (single instruction stream/ multiple data stream) architecture LISP machine called ATOM with a 64-bit data bus and 32-bit address bus. The machine consists of a data operation unit (DOU) with a 64-bit ALU, 16 Mbytes of memory, 64x8 R and S registers, and controllers; and two structure operation units (SOU) with a 128-bit ALU, 128x8 S register, and 64Kx128 leaf memory.

Hitachi is currently developing a 1 MLIPS PROLOG 32-bit processor for its minicomputer. Within the Warren instruction set, the processor will be capable of list and cross-index processing. The compiler and interpreter will run on UNIX.

MITI Voice Recognition Standard Language

MITI's Institute of Industrial Technology announced plans to establish a standard language format for voice-activated computer input systems. The "Common Voice Data" system, which will consist of a taped library, will be developed by October 1987 and offered free of charge. The plan involves gathering voice patterns from 150 people between the ages of 20 to 60. Each person will vocalize 323 words four times, including 101 Japanese syllables, 9 commonly used foreign syllables, 15 four-digit numbers, 100 geographical names, and 63 functional languages for word processors and banking inquiry systems. The goal is to create a library of 193,000 voice samples. Fujitsu, Hitachi, NEC, Toshiba, Tsukuba University, and Utsunomiya University will collect the voice data. Dataquest believes that this represents a major step toward promoting future voice recognition and synthesis ICs and systems. (See Toshiba three-Chip Voice Recognition Set in the "Voice Recognition" section).

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MITI Future Computing Committee

In January 1987, MITI, six major Japanese computer makers, and eight major computer users formed a committee in the Japan Information Processing Development Corporation to study ways of promoting advanced computer and information systems. Formed at MITI's urging, the group will discuss risk sharing in joint-development projects, software development, maintenance problems, and computer keyboard development. MITI's goal is to promote closer cooperation between users and vendors. The six computer makers include Fujitsu, Hitachi, Mitsubishi, NEC, Oki, and Toshiba; the eight major computer users are Mitsubishi Corp., Nippon Steel, Nomura Securities, Sumitomo Bank, Sumitomo Chemical, Tokyo Electric, Tokyo Marine and Fire Insurance, and Toyota Motors.

MITI Sigma Project

IBM Japan decided to join the Sigma Project, a ¥22.8 billion ($152 million) program launched in April 1985 to develop UNIX-based computer software by fiscal 1990 (see "Technology Trends, 3rd Quarter 1986," page 5). IBM Japan was initially reluctant, but decided to join after the project ordered high-performance personal computers from NEC, Toshiba, and four other Japanese computer makers. Currently, 250 companies are participating in the project, including Japan's Big Six computer companies: Fujitsu, Hitachi, NEC, Toshiba, Mitsubishi, and Oki Electric.

In January, the Sigma Project purchased 50 workstations and Japanese language software from Fujitsu, NEC, and other Japanese makers.

MITI Optical Communications Standardization Plan

In January 1987, MITI and the Optoelectronics Industry and Technology Development Association framed a plan to standardize 33 optical communications products. The products were designated as Japan Industrial Standard (JIS) items from March 1987.

MITI/MPT Electronic Dictionary Project

In January 1987, Sanyo Electric announced a portable electronic dictionary incorporating 35,000 basic Japanese and English words. The PD-1, which measures 209 x 130 x 30mm and weighs 520 grams, converts words entered alphanumerically into Japanese characters. The machine is priced at ¥34,800 ($248) and is supplemented by a 20,000-word Japanese-to-English IC card selling for ¥7,000 ($47).

Sanyo was not one of the original members of the Japanese Electronic Dictionary Research Center, which was formed in May 1986 under the auspices of the MITI-MPT Japan Key Technology Center (see "Technology Trends, 2nd Quarter 1986," page 8). Founding companies include Fujitsu, Hitachi, Matsushita, Mitsubishi, NEC, Oki Electric, Sharp, and Toshiba.

MITI/MPT/NHK High-Definition TV Standards

Japanese ministries are currently working to develop high-definition TV (HDTV) standards. The Ministry of Posts and Telecommunications (MPT) and Japan Broadcasting Corporation (NHK) are formulating a CCIR (International Radio Consultative Committee) standard and developing the Hi-Vision system that was jointly proposed by Japan, the United States, and Canada. In January, MPT held a Hi-Vision broadcasting conference focus, while MITI began a research project to explore nonbroadcasting prospects for Hi-Vision. The Space Agency will launch the BS-3a satellite in mid-1990 for experimental HDTV broadcasting. MPT estimates that the cumulative Hi-Vision market over the next 10 years will total ¥12.0 trillion ($80 billion), including ¥5.3 trillion ($35.3 billion) for receivers and ¥6.7 trillion ($44.7 billion) for VCRs, broadcasting equipment, and other equipment.

JAERI Smart Robot Project

In early 1987, the Japan Atomic Energy Research Institute (JAERI) announced plans to develop intelligent robots for nuclear applications over the next 10 years. The goal is to make robots intelligent enough to understand, judge, and act like human technicians in hostile environments, such as nuclear power plants. The proposed robot system, which will run on JAERI's supercomputer, will feature a superfast calculator, graphic displays, and a relational data base containing maintenance and repair knowledge culled from human workers. Another data base will store equipment shape information. Research will initially focus on software, but will eventually focus on hardware.

MITI/MPT Engine Combustion System Project

In February, the New Combustion System Laboratory was established to conduct basic and applied research on high-efficiency combustion engines for use in the 1990s. The seven-year program, located in Tsukuba Science City, is capitalized at ¥176 million ($1.25 million), of which 70 percent will be provided by the Japan Key Technology Center, an industry/government research institute sponsored by MITI and the Ministry of Posts and Telecommunications (MPT). The remaining 30 percent will be provided by Daihatsu, Diesel Kiki, Hino Motors, Isuzu Motors, Mitsubishi Motors, Mazda, Nippondenso, Nissan, Nissan Diesel Motor, and Toyota. Nippondenso is a major electronics and mechanical parts supplier.

Dataquest observes that 25 Japanese companies formed the Next Generation New Alloys Research Association in early 1986 to develop alloys, shaped memory alloys, fine ceramics, and hydrogen storage alloys for next-generation cars and trucks (see "Technology Trends, 1st Quarter 1986," page 6). Nippondenso, Nissan, Toyota, and other companies are also involved in that project. We believe that both projects will exchange information on next-generation electronic engine controls.

NEW PRODUCTS AND TECHNOLOGY TRENDS

Memory

At the International Solid State Circuits Conference (ISSCC) 1987 in New York City, Japanese semiconductor makers announced the following 4Mb DRAMs, as shown in Table 3:

- Data I/O--A Hi-SUM circuit for G-Series RAM disk board IOS-10
- Fujitsu--A 5ns 64K ECL RAM; 8Kx8 memory organized into two 8Kx4 blocks; 1-micron rule; U-groove separation; 403 square micron memory cell; 76.4 square mm chip; 6.5W power; sampling in 1987
  - A tag memory designed as a cache memory for 32-bit MPUs; 19ns address input-to-output time; 9.5ns tag data input-to-output time; 49K SRAM and 3,500-element logic integrated onto one chip
  - A 250ns 4Mb CMOS mask ROM (MB834100); 524,288 words + 8 words x 8 bits, or 282,144 words + 4 words x 16 bits; 50mW power consumption during operation and 275uW at standby; 4.9 x 9.2mm chip; 1.2-micron process; 40-pin DIL package; EPROM pin compatibility; 20,000-unit monthly production since first half of 1987; priced at ¥4,000 ($28.60)
  - Two 64K CMOS SRAMs; 440mW power consumption during operation and 10mA at standby; 300 mil, 22- to 24-pin DIP, and 22- to 28-pad LCCs; sampling at ¥4,000 ($28.57) for 25ns model and ¥3,200 ($21.33) for 35ns model

Table 3

JAPANESE 4MB DRAMs ANNOUNCED AT ISSCC 1987

Company	Microns	Speed	Process	Cell Size	Chip Size
Fujitsu	0.7um	70ns	N/CMOS	N/A	N/A
Matsushita	0.8um	60ns	CMOS	1.74 x 4.6um	4.54 x 14.8mm
Mitsubishi	0.8um	90ns	CMOS	4.2 x 2.6um	4.85 x 14.9mm
NEC	0.8um	95ns	NMOS	2.3 x 4.6um	6.2 x 16.0mm
Toshiba	1.0um	80ns	CMOS	3.0 x 5.8um	7.84 x 17.48mm
Toshiba	0.9um	60ns	CMOS	N/A	N/A

Source: Dataquest
August 1987

- Hitachi--1Mb/2Mb/4Mb CMOS mask ROMs; 1.3-micron process using the vertical ROM method; 150ns access time for 1Mb model; 200ns for 2Mb and 4Mb models; pricing for 2,000-unit lots; ¥800 ($5.19) each for 1Mb, ¥1,250 ($8.12) each for 2Mb, and ¥2,300 ($14.94) each for 4Mb

  - Three 64K ECL RAMs; 15ns ECL 100K-compatible version (HM100490-15); 12ns ECL 10K-compatible (HM10490-12); 15ns ECL 10K-compatible (HM10490-15); sampling for ¥24,000 ($161.07) in LCC package and ¥14,000 ($93.96) in lots of 10,000

  - Two 1Mb CMOS DRAMs; 100/120/150ns; x8 (20mW) and x9 (23mW) structures

  - An experimental 35ns 1Mb BICMOS DRAM; 450mW power consumption at 60ns cycle time; 1.3-micron rule

  - Two 16K CMOS line memories (HM63021P-28/34); 1Kx2x8 storage; 28/34ns; 1.3-micron process; 250mW power consumption; 28-pin plastic DIP

  - A 256-byte CMOS EEPROM; 2-Kbyte ROM; 32-byte RAM; 20mW power consumption; 28-pin plastic shrink DIP

- Two 1Mb SRAM modules; 128Kx8; 120/150ns; 600-mil wide, 32-pin, 15.2mm-wide DIP; JEDEC pin and signal compatibility with 1Mb DRAMs; HM66203 series with outside decoder priced at ¥18,000 ($126.62) per unit, or ¥14,000 ($90.91) for 10,000-unit lots; HM66204 series with built-in decoder at ¥19,500 ($126.62) and ¥15,500 ($100.65), respectively

- A 42ns 1Mb SRAM; 128x8; compatible with HM66204 1Mb SRAM module (see above); 8 million transistors on a 1mm square chip; 45-micron square memory cell area; 0.8-micron design rule; commercialization from 1988; ISSCC 1987 paper

Matsushita--A 16Mb trench method memory cell with error checking

- An improved version of CMOS 4Mb DRAM introduced at ISSCC 1987; 100ns access time; 250mW to 300mW power consumption; sampling from January 1988 and volume production during fiscal 1989

- Two 4Mb CMOS mask ROMs (MN234000/01); 200ns CMOS (524, 288x8) in 40-pin DIP; 250ns NMOS (262, 144x16) in 64-pin QFP; factory programmed; 20mA current consumption during operation; 1.4-micron double-layer, polysilicon, multigate memory cell structure; 8- or 16-bit operating mode; 90mW power consumption during operating and 50uW during standby; 11.12 x 5.79mm chip; sampling at ¥4,000 ($28.57); 50,000-unit monthly production

- A 3-D 8K SRAM utilizing multilayer monocrystal technology and heat-resistant interconnect wiring; multiple layers formed using a dual argon laser beam to melt islands of polycrystal silicon into monocrystal and form a flat multicrystal heat sink layer in the bottom LSI layer; 4K CMOS memory cell, I/O circuits, decoder, and peripheral circuits connected by tungsten wire on first layer of N-type silicon; 4K CMOS memory on second layer of monocrystal silicon islands; 120ns access time; 7.5 x 8mm; 50,000 elements; 2Kx4 structure; 3-micron design rule; 256-bit 3-D SRAM previously announced

- Four 256K CMOS SRAMs (MN23258); 32Kx8; 70/85/100/120ns; 1.5-micron process; 9.18 x 5.67mm chip; 375mW maximum power consumption and 40mW at 1 MHz; 600-mil, 28-pin DIP; sampling at ¥4,900 to ¥6,500 ($35.00 to $46.42)

- A SOP version of 256K SRAM (M5M5256P series); 100/120/150ns access times; 2mA standby current; sampling at ¥5,000 to ¥5,600 ($35.70 to $39.29)

- Two 1Mb mask ROMs; 131Kx8; 250ns CMOS (MN231000) and 150ns NMOS (MN231001); 28-DIP and SOW-28D

- Two 256K mask ROMs; 32Kx8; 200ns CMOS (MN23258) and NMOS (MN23257); 28-pin DIP

- A 200ns 128K NMOS mask ROM (MN23138); 16Kx8; 28-pin DIP

- A 150ns 64K NMOS mask ROM (MN2364); 8Kx8; 28-pin DIP

• MITI Electrotechnical Lab--Theoretical SOI process for 0.025-micron 1Gb DRAMs and 10ps high-speed logic; new MOS transistor structure

• Mitsubishi--A 64K full CMOS SRAM; radiation hardened for satellites; jointly developed with NTT

- Two 1Mb CMOS EPROMs (MSM27C100K/101K); 1.5-micron CMOS silicon gate process; 150/250ns access times; 263mW power consumption in operation and 6mW at standby; 12.5V write-in voltage; sampling at ¥5,000 ($32.89) for 150ns type, ¥4,000 ($26.32) for 200ns, and ¥3,000 ($19.74) for 250ns; 500,000-unit monthly production

- A 250ns 4Mb ROM (M5M23C400P/FP); 256Kx16 and 512Kx8; 165mW power consumption during operation and 550mW at standby; eight memory cell layers consisting of eight memory transistors; 1.2-micron process; sampling at ¥4,000 ($28.57)

- A GaAs 16K SRAM; adopted self-junction FET structure; 15ns access time; 5.8 x 4.7mm chip; 1W power consumption; announced at ISSCC 1987

- A 480K CMOS field memory (M5M4C500L) that allows a TV or VTR to simultaneously record and play back pictures; 320 x 256 x 6-bit structure; 5.0 x 10.08mm chip; NTSC and PAL method; also capable of storing one TV screen at a time; three chips enabling two programs on one screen, noiseless still images, strobe, and slow-motion images; 28-pin ZIP; sampling at ¥3,000 ($21)

- A 34ns 1Mb CMOS SRAM using triple polysilicon; announced at ISSCC 1987

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- NEC--A general-purpose, 8-Kbyte, single-chip cache memory (MuPD43608R); 1.3-micron CMOS process and aluminum double-layer wiring technology; includes 10Kb dual-port memory and peripheral control circuits; 85ns data output time; 125ns cycle time; 16-byte x 128-set x 4 internal organization; 95 percent hit rate; sampling at ¥80,000 ($519.48); production of 30,000 units monthly in second half of 1987; announced at ISSCC 1987

  - Four 256K SRAM integrated onto a ceramic board (HM66203); decoder connection model priced at ¥18,000 ($128); built-in decoder model at ¥19,500 ($139)

  - Three 256K CMOS SRAMs (MuPD43254C); 35/45/55ns; 64x4; 1.3-micron process; low-resistance, double-layer aluminum interconnection; 300-mil, 24-pin plastic DIP; sampling at ¥10,000 ($62.50)

  - Three 1Mb CMOS DRAMs; high-speed page mode (MuPD421000), nibble mode (MuPD421001), and static column mode (MuPD421002); 1-micron process; trench capacitor memory cell; 300-mil, 18-pin plastic DIP or 20-pin plastic SOJ; 30/100/120ns random access

  - Two 16K ECL RAMs (MuPB10484/MuPB100484); 10/15ns access times; 4Kx4; pnpn memory cells; 23mm square chip; sampling at ¥10,000 ($71) for 10ns version and ¥8,000 ($53) for 15ns version

- NTT--A 16Mb DRAM prototype announced at ISSCC 1987; 0.7-micron process; 40 million transistors; 2Mbx8; 180ns cycle time; 8.9 x 16.6mm chip; 1.5 x 3.5mm memory cell; 5ns access time; high-performance, on-chip error correcting code (ECC) circuit occupying 13 percent of chip area; isolation-merged vertical capacitor (IVEC); 2Mx8 memory cell; 80ns read-in time; 500mW power consumption; low-voltage (3.3V) DRAM circuit enabling 10ns increase in speed over conventional methods; cell array architecture featuring 500mW power consumption; storage capability of 1 million kanji characters or 2 million alphanumeric letters; E-beam process used

- Oki Electric--Two 1Mb DRAMs using a proprietary buried stack capacitor cell technology; 100/120ns; 1.2-micron design rule; 1Mbx1 page and nibble mode, or 256Kx4 page mode; 413mW (100ns part) and 385mW (120ns) power consumption during operation and 28mW at standby; ¥7500 ($50) for 1Mbx1 120ns part in 100-unit lots; ¥8,440 ($56) for 256Kx4 120ns part

  - A pseudovirtual 4Mb CMOS DRAM; 512Kx8; 1.0 micron; 8.75 x 17.07mm; 60/95ns read times; 65mA in operation and 1mA at standby; 1.0-micron rule; 16.8 square micron memory cell; electrostatic capacitance of 44 femto farad; announced at ISSCC 1987

- A general-purpose 4Mb DRAM; 4Mx1 or 1Mx4; 65ns read time; 80mA in operation and 1mA at standby; 0.8-micron process; 5.0 x 14.0 mm chip

- A CMOS 1K EEPROM; 2.5 mmA in operation and 100 uA at standby; 64x16 or 128x8 configurations

- Sample 16K and 64K CMOS EEPROMs and 256-bit, 512-bit, and 1K serial access CMOS EEPROMs; developed with Catalyst Semiconductor

- Three CMOS 256K SRAMs (SRM20256LC/LS/LM); 100/120ns; 32Kx8; TTL compatible; 28-pin DIP, 28-pin shrink DIP; 28-pin MFP (SOP)

- Sharp--A three-layer, 3-D, 64K DRAM using 4-micron geometry; etch-back technology; high-heat withstanding wiring structure; 0.2-micron height for each wafer layer; plans for a multilayer 3-D intelligent image processor by 1990

- Toshiba--A 250ns 4Mb CMOS mask ROM (TC534000P); 512Kx8; 1-micron process; memory cells arranged in superimposed layers; 10ms per byte; power consumption of 20mA in operation and 1uA at standby; 32-pin DIP with pin-arrangement compatibility with 2Mb ROMs and EPROMs; sampling at ¥3,000 ($19.48)

  - A 120ns 4Mb CMOS EPROM; 512Kx8; 10 microseconds per byte to write in information; 0.8-micron design rule; 5.9 x 14.9mm chip; 9 square micron cell area; 10mA power dissipation

  - A 25ns, 1Mb NMOS/CMOS SRAM; 6.86 x 15.37mm chip; NMOS memory cells and CMOS peripheral circuits; 15mA power consumption during operation and 1mA at standby; ISSCC 1987 paper

  - Plans to introduce a 4Mb DRAM, 4Mb EPROM, and 1Mb SRAM in 1988; 0.8- to 0.9-micron minimum process

Application-Specific Memory (ASM)

- Sanyo--A digital-servo LSI (LC7413) with built-in variable slow-control circuity for VCRs; 2-micron CMOS dual-layer aluminum gate process; built-in mask ROM; combined with new bipolar linear IC (LA7117) to form VCR digital-control circuitry; 4.5V to 5.5V voltage; sampling at ¥1,500 ($10.70) and ¥300 ($2.14) for LA7117

- Toshiba--An advanced LSI for consumer remote-control devices, featuring 20 general-purpose components, including MPUs, discretes, LCD drivers, resistors, and capacitors; 64K ROM (8Kx8) for storage of function transmission codes; T9723B for VCRs and compact disk players; T9723A for air conditioners; sampling at ¥800 ($5.70)

Smart Cards

- Dai Nippon Printing/Tokyo Tatsuno--A jointly developed large-capacity IC card system featuring a 128K storage capacity; one 8-bit MPU and 64K EEPROM; 500 systems sold to the Ministry of Construction's Hokuriku Regional Construction Bureau

- Japan Consumer Credit Industry Association/MITI--A joint committee to help heavily indebted credit card users; 86.83 million cards issued in 1985, up 17.6 percent from 1984; 64,000 complaints registered in fiscal 1984

- Sanyo--An English-to-Japanese/Japanese-to-English electronic dictionary on an IC card; 35,000 words in a 4Mb memory card; 20,000 words Japanese-to-English; 209 x 130 x 30mm keyboard and LCD display priced at ¥34,000 ($243); memory card (54 x 86 x 3.8mm) at ¥7,000 ($50)

Microprocessors/Microcontrollers

Table 4 shows the microprocessor papers presented at the 1987 International Solid States Circuits Conference (ISSCC).

Table 4

ISSCC 1987 MICROPROCESSOR TECHNICAL PAPERS

Company	Process	Device	MHz	Chip Size
AT&T	1.75um CMOS	32-bit MPU	16MHz	10.35 x 12.23mm
Digital Equipment	2.00um CMOS	32-bit MPU	25.0	9.7 x 9.4
Digital Equipment	2.00um CMOS	Parallel 2-chip	-	10.4 x 9.4
Fujitsu	1.30um CMOS	Controller	-	4.86 x 8.76
Hitachi	1.30um CMOS	3-chip MPU set	-	12.9 x 12.9
Hitachi	2.00um CMOS	MCU with EEPROM	-	5.6 x 5.7
HP	1.50um NMOS	32-bit MPU	30.0	8.4 x 8.4
HP	1.60um CMOS	32-bit MPU	8.0	8.46 x 8.62
International Micro	2.00um CMOS	16-bit MPU	10/20	10.0 x 10.0
Matsushita	1.00um CMOS	32-bit MPU	12.5	9.74 x 9.45
Mitsubishi	1.30um CMOS	32-bit CPU set	-	8.75 x 11.26
NEC	1.30um CMOS	Cache CPU	-	13.04 x 13.43
NTT	2.00um CMOS	32-bit LISP MPU	-	15.0 x 15.0
Stanford University	2.00um CMOS	32-bit MPU	20.0	8.0 x 8.5
TI	1.25um CMOS	32-bit LISP MPU	-	10.0 x 10.0

Source: ISSCC 1987 Proceedings

- Fujitsu--A cache memory for 32-bit MPUs; 19ns address time; 49K SRAM and 3,500-element logic structure

  - A MIMD parallel processor structure proposed

  - Two data I/O LSIs with six ports of 8-bit parallel I/O (MB89363/MB89363B); 5V single power supply; CMOS process; sampling at ¥600 ($3.70)

  - Two TV displayer controllers (MB88321/MB88322); RGB output; 8-color display; MB88321 with built-in 64K character generator ROM; MB88322 with RAM

  - A CMOS multifunction peripheral LSI (MB39391) for use with MBL8086 16-bit MPUs; interrupt controller, bus controller, clock generator, timer, and DMA controller; 100-pin quad flat package; sampling at ¥2,400 ($17.14)

  - A CMOS 8-bit single-chip MCU (MB89733B); sampling for ¥1,200 ($7.80) and a piggyback type (MB89PV733B) for ¥30,000 ($194.80)

  - A CMOS 8-bit MPU with a CPU core (MB89702) and CPU development tool; 260-byte RAM; 21-bit timer; 128-Kbyte data memory; 40-pin DIP; sampling at ¥800 ($5.70)

  - A 3Gb/sec. GaAs multiprocessor for multiplexer/demultiplexer for optical cable TV and 400Mb/sec. optical LANs; 1.5-micron rule; 24-pin flat package

  - A 1-chip bipolar controller (MB1430/1431) for 1Mb DRAMs; multiplexer and counter peripherals for memory control integrated on same chip; 48-pin plastic DIP; capable of managing 44 1Mb DRAMs; sampling at ¥2,200 ($15.70)

  - A 4-bit, single-chip CMOS MPU (MB88205B) for low-end audio and video equipment; 23 I/O ports; optional pull-down resistors; 1-Kbyte built-in ROM, 128-bit RAM; 28-pin plastic DIP; sampling at ¥300 ($2.15)

- Fujitsu/Hitachi/Mitsubishi--Joint development on a proprietary 32-bit MPU (HF32/300); 20 mips; 4-Kbyte cache memory; supporting UNIX System 5 and ITRON; commercialization in late 1988

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- Hitachi--A single-chip MCU (HD401304) featuring a built-in 256-byte EEPROM, 3.5-Kbyte ROM, an 80-byte RAM, and image display function; sampling at ¥1,500 ($10.07) each for 10,000-unit orders

  - A 32-bit single-chip AI processor for handling Smalltalk80, PROLOG, or LISP; completion of design by late 1987; marketing from 1988

  - A C language compiler MPU (HD64180); VAX-11/VMS-4.2 operation system; Kernigham & Ritchie programming language

  - Two graphic display devices; the HD6345/HD6445 enhanced CRT controller (HRTC-II) featuring 256 x 256-line screen format control at 4.5 MHz clock rate, four split screens, scrolling, two programmable cursors, and dual-port memory access control; HD63645/HD64645 LCD timing controller (LCTC) featuring programmable 2,048 x 1,024-dot screen size, programmable display ratio (1/512 duty cycle), and programmable character font

  - A CMOS floppy disk controller (HD63265) with analog VFO circuit and a CMOS hard disk controller (HD63463)

  - Data conversion and transfer ICs for compact hard disk drives (HD153007/153009); 15-Mbyte/sec. maximum data transfer speed; priced at ¥1,800 ($12.80) in 10,000-unit lots; two seven-code conversion method featuring memory density 1.5 times conventional MFM-type data transfer methods

- Matsushita--TRON 32-bit MPU development planned; also developing a 64-bit MPU with SAE Corporation (United States), integrating 4.5 million transistors on a 2.5cm square chip using 0.8-micron process

- A CMOS 32-bit MPU with on-chip cache memory; announced at ISSCC 1987

  - Joint development of 64-bit MPU with SAE of Dover, Delaware; 10 mips; 50-MHz clock frequency; 2.5cm square chip; scheduled for completion by late 1987

  - An 8-bit CMOS MCU family (PCF84CXX) to be jointly developed with Philips; on-board IIC bus serial communications interface; very high density, low-power SACMOS process (developed by Philips' Swiss subsidiary, Faselec); 28-pin PCF84C21 with 2 Kbytes of ROM and 64 bytes of RAM; PCF84C41 with 4 Kbytes of ROM and 128 bytes of RAM; 10 kHz to 100 kHz

- Mitsubishi--Three CMOS MCUs; 4 Kbytes of ROM/128 bytes of RAM (M50930FP0; 4 Kbytes of ROM/512 bytes of RAM (M50931FP); 8 Kbytes of ROM/512 bytes of RAM (M50932FP)

  - A CMOS 4-bit MCU with built-in character display function (M50436-SP) for voltage synthesizers; 16 characters x 3 lines for color selection; 6 x 7 dots; 64 character types and 4 character sizes; sampling at ¥1,080 ($6.67)

  - An I/O interface LSI (M5M82C255ASP) and four 2K RAMs with built-in I/O port and timer; I/O interface with one general I/O port and two special-purpose ports with 24 I/O lines for transferring data to 8-bit or 16-bit CPUs

- NEC--A CMOS 32-bit MPU (V60 Series/MuPD70616); 1.5-micron aluminum two-layer process; 375,000 transistors; 6-pipelined architecture; floating-point image function; 3.5 mips at 16 MHz; 5V; 68-pin PGA

  - A 32-bit MPU (V70); 20 MHz; 6.6 mips; virtual memory management and fault-tolerant functions; 385,000 transistors; sampling at ¥100,000 ($714); commercial production at a monthly rate of 20,000 units from August 1987

  - A CMOS 32-bit MPU (V80) with 32-bit internal and external architecture; 1.0-micron rule; 700,000 transistors; 10 mips; on-chip cache memory

  - A 16-bit single-chip MPU with built-in I-TRON; 2.4 microsecond switching; commercialization since the spring of 1987

  - An Intelligent String Search Processor (ISSP) with 22K logic gates and 217,600 transistors; 10 million characters per second processing speed; associative memory consisting of four SRAMs; for retrieval of key words where one character differs from the key word in memory

  - Two CMOS 4-bit MCUs with built-in 16K ROM (MuPD75216A) or piggyback type (MuPD75CG216A); priced at ¥1,000 ($6.17) for 75216A and ¥10,000 ($61.73) for 75CG216A

  - A 16-bit single-chip MCU (V25); MuPD70322 with built-in 16K ROM; MuPD70320 without ROM; sampling at ¥8,000 ($49.38); production of 50,000 units monthly since fourth quarter 1986

  - A programmable moving-image MPU with an absolute-value arithmetic circuit, accumulator, and minimum/maximum detector; new parallel-processing system, whereby each component is assigned a processing domain; ISSCC 1987

- Five digital tuning MCUs with built-in OTP ROMs; 1Kx16, 1.5Kx16, or 2Kx16; 64x4 to 256x4 RAM capacities; built-in LCD control/driver and 150-MHz prescalers; 21V write voltage; 52-pin or 64-pin flat package, or 28-pin shrink DIP; priced at ¥2,000 to ¥4,000 ($14.29 to $28.57)

- An ultraviolet motor controller series; 2.0 to 3.3V, 2.0 to 6.0V, and 5V+ to 10V

• Oki Electric--A single-chip CMOS 8-bit MCU with EEPROM (MSM61580); 5.5 x 4.5mm chip; 813.8ns speed; 8-Kbyte program ROM, 512-byte ROM; for IC cards

- A single-chip, 4-bit CMOS MCU (MSC6458) with built-in 24-output optical display driver for audio equipment; 7.4 x 7.2mm chip; 64-pin shrink DIP; ¥800 ($5.70)

• Seiko Epson--Two CMOS 4-bit, one-chip MCU series; SMC6110F series featuring 1Kx12 ROM, 48x4 RAM, and LCD driver; SMC6120F series with 2Kx9 ROM, 96x4 RAM, and LCD driver

- A CMOS 8-bit, single-chip MCU series (SMC8360F); built-in 400- or 800-gate array; 4Kx8 ROM, and 128x8 RAM

• Sony--A 1-Mbyte 2-inch floppy disk controller CMOS LSI (CXD11030)

• Toshiba--A one-chip CMOS controller for remote control handsets; Model T9723A for air conditioners; Model T9723B for VTRs and CD players; 8K ROM; 832-bit data memory; 60-pin miniflat package; sampling at ¥800 ($5.00)

• Yamaha/ASCII--A single-chip CMOS controller for CRT, electroluminescent, plasma, and liquid crystal displays; compatible with IBM's MDA, CGA, and HGC displays

Digital Signal Processors (DSPs)

• Fuji--An 8-bit digital signal converter IC (SLE4520); 0 to 2.6 kHz; 20mA power dissipation; 5.5V; 28-pin DIP; sampling at ¥4,200 ($30)

• Fujitsu--Two video display RGB (red/green/blue) controllers (MB86321/22)

- Hitachi--A document image compression and expansion processor (DICEP) plastic package version; G3/G4 CCITT codes; 0.85 seconds for letter size document; 32-MHz input clock frequency; 125ns machine cycle; 64-Kbyte image address space; 65,536-pixel horizontal resolution; 400Kb/sec. decoding speed

  - An ultrahigh-speed, general-purpose DSP with 50ns sum-of-products computing power; 430,000 elements on 11.5 x 12.9mm chip; 1.3-micron CMOS process; two-layer structure; fixed-point arithmetic mode using a 16-bit multiplier and 32-bit adder/subtractor; 1Kx48 program RAM; 600ns speed to process 3.3 picture elements

- Matsushita--A high-speed, high-efficiency DSP (MN8601); 2-micron double-layer aluminum and double-layer polysilicon CMOS process; 7.52 x 7.24mm chip; 160,000 elements; 100ns cycle time; 256x16x2 set of RAM and 2,048x32 instruction ROM; 100mW power consumption; sampling at ¥5,000 ($33.56); 30,000 units per month

- NEC--A graphic display controller (MuPD72120), a high-end version of the MuPD7220A; sampling at ¥20,000 ($123.46)

  - A 16-bit DSP chip (MuPD77C25) with twice the speed of MuPD7720; sampling April; 122ns instruction cycle time; 2Kx24 instruction ROM; 1Kx16 data ROM; 256x16 data RAM; 28-pin DIP and 44-pin PLCC; ¥5,000 ($35.70)

  - A CMOS 2,048 x 2,048-channel digital switching circuit for connection between two LSI chips; 11.8 x 12.1mm chip; 16.4-MHz clock frequency; 4,000 gates; 2,176 x 17 x 2 SRAM; 50ns cycle time; 16-bit MPU interface; TTL-compatible; 132-pin PGA or 92-pin flat package

  - Four video signal processors (MuPC2312CA/13CA/14CA/15CA) for VHS VCRs; sampling at ¥1,500 ($9.87) for two-head and ¥1,700 ($11.18) for four-head

  - Two 122ns CMOS 16-bit DSP circuits; 1K data ROM; 256-word data RAM; 2K instruction ROM; 28-pin DIP or 44-pin PLCC for surface mounting; MuPD77C25 priced at ¥5,000 ($32.47) per unit for 10,000-unit lots and Mu77P25 at ¥10,000 ($64.94)

- Sharp--A multifunction signal processor (LR3763) for compact disk players; tracking, monitoring, error detection, and correction functions; 1.5-micron CMOS process; 60,000 transistors and circuits; 120mW power consumption; ±5V power supply; sampling at ¥2,500 ($17.85)

- Toshiba--A CMOS chip pair for digital TV; NTSC and PAL method; built-in 1,135 x 8 x 2-line memory; 140,000 transistors; 7.95 x 7.8mm chip; signal-processing chip featuring 55,000 transistors on a 6.67 x 6.55mm chip; real-time processing

Voice Recognition Chips

- Toshiba--Speaker-independent three-chip voice recognition system with 95 percent accuracy, using analog signal processor, a DSP, and system control LSI; 13-word recognition; sampling by late 1987 at ¥10,000 ($6.50)

Application-Specific ICs (ASICs)

The Custom Integrated Circuits Conference (CICC 1987) was held in Portland, Oregon, on May 4 to 7, 1987. Table 5 summarizes the major papers announced at the conference.

Table 5

PAPERS ANNOUNCED AT CICC

Company	Paper
Gigabit Logic	A GaAs standard cell LSI library
Motorola	150,000-gate CMOS channelless gate array; 0.5-micron rule
Toshiba/LSI	130,000-gate CMOS channelless gate array

Source: Dataquest
August 1987

- Ando Electric--A time chart reader (Au-4101) that reduces ASIC turn-around time by one week by converting logic waveform diagrams to pattern data directly readable into CAE/CAD systems; five seconds per chart

- Fujitsu--Eleven ultrahigh-speed CMOS gate arrays (UHB series) and six low-voltage operation models (AVL series); two-layer aluminum CMOS 1.5-micron process; 0.9ns delay time for UHB series; ¥1.8 million ($12,080) development cost; priced at ¥700 ($4.70) each for 10,000- unit lots; development costs of AVL series ¥1.7 million ($11,409); priced at ¥500 ($3.36) each

- Matsushita--An analog cell library, including D/A and A/D converters, operational amplifier, comparator, and analog switch; sales since early 1987

  - A megacell library; 2-micron rule double aluminum CMOS process featuring 4-bit CPU and 4- and 8-bit peripherals; 1,000 transistors on a 4mm square 4-bit CPU; 2,500 to 10,000 transistors on a 4 x 8mm 8-bit CPU peripheral

  - A GaAs gate array series; 200 to 1,000 gates; 1,000-gate model with 0.28ns delay time and 1.5mW per gate power consumption; proprietary pseudo-push/pull FET logic that increases the load-driving circuit capacity; 7,200 FETs, 2,100 diodes, and 3,000 capacitors on 5.15mm square chip; for high-speed computers, optical communications, and measuring instruments; priced at ¥50 ($0.32) per gate, or four to five times ECL prices

- Mitsubishi--An ECL gate array that reduces software error to 1/100 of conventional devices; noise circuit added to reduce error rates (1,000 times when design rule reduced from 2.5 to 1.3 microns)

- NEC--Two ECL gate arrays; 600-gate (MuPB6303); 1,200-gate (MuPB6312); 100ps gate delay; 2.1-GHz toggle frequency; ECL100K- and ECL10KH-compatible

  - A series of 43 gate arrays; 24 CMOS (320 to 20,000 gates); 4 BICMOS (600 to 3,100 gates); 5 TTL (250 to 2,000 gates); 10 ECL (300 to 5,000 gates)

- Ricoh--A high-speed EPLD with 25ns propagation delay time (EPL241); compatible with AMD's 22V10 standard logic; 1.5-micron CMOS process; up to 950 gates; built-in EPROM; 25ns I/O delay time; 30-MHz clock speed; sampling at ¥4,000 ($26.32) for erasable type and ¥3,000 ($19.74) for OTP type

- Seiko Epson--A BICMOS gate array family; 1.2- to 1.5-micron process; 0.6ns to 0.7ns; plans to sell to U.S. military, telecommunications, and measuring applications

  - Four gate array series (SLA6000/600L/7000/700L) comprising 25 models; master slice CMOS gate arrays from 500 to 6,200 gates (SLA6000); high-speed, low-voltage gate arrays from 500 to 6,200 gates (SLA600L); master slice CMOS gate arrays from 2,000 to 9,250 gates (SLA7000)

- Toshiba--A 0.7ns CMOS gate array family (TC110G series) jointly developed with LSI Logic; 15,000 to 50,000 gates; priced 20 percent to 30 percent higher than TC19G series (1ns)

CAD Systems

- Fujitsu--An 80286-based PC VLSI CAD system (VIEWCAD 2000) for gate-level logic simulation up to 20,000 gates; MS-DOS; protect mode; 5-Mbyte memory

- Toshiba--An analog IC layout CAD; circuit data input to generate mask pattern; one-half to one-third the time to design 350 analog circuit TV chip

Optoelectronics

- Hitachi--A DIL semiconductor laser (HL1321DL) containing a laser diode, monitor photodiode, electronic cooling device, and thermistor; 1.3-micron wavelength; 14-pin module; 300-micron-diameter monitor PIN-compound photodiode device; light output stable up to 1.2mW; 300Mb/sec. response speed

- Matsushita--A blue light semiconductor laser using an SHG (second harmonic generator) device; 0.415-micron wavelength; 0.83-micron laser and SHG device; capable of increasing optical disk memory capacity by four times

  - A GaAs optical transmitter IC (OTIC); 163 elements; 1Gb/sec. transmission speed; combined with a high-speed multiplexer/demultiplexer to develop an 8-channel, high-speed, multiplexed optical LAN system

  - A new selenium-zinc-chlorine material for making bright blue LEDs; resistance reduced to one-tenth (0.003 ohm per cm); brightness increased fourfold

- An optical isolator mass production method using liquid phase epitaxy (LPE); one-tenth the cost of conventional methods; crystals for 400- to 800-MHz communications; layers of bismuth, litetium, and gadolinium on gadolinium, gallium, garnet (GGG) substrate

- A 0.82-micron wavelength semiconductor laser; 30nm beam; 128Mb/sec. transmission for NTSC color TV signals; 500m to 10km transmission

- Ministry of Education--Increased R&D on blue LEDs using zinc sulfide, zinc selenide, and other materials; for use in colored displays and large TV screens; Matsushita research on blue LEDs using gallium nitride; installation of MBE and MOCVD equipment at universities being coordinated by Tokyo Institute of Technology Professor Hiroshi Kumamoto; ¥70 billion ($500 million) market in fiscal 1985; research by Matsushita, Nippon Glass, Sanyo, Sumitomo Metal Mining, and Toshiba

- Mitsubishi--A planar-type laser diode that simplifies the process of producing OEICs; a Transverse Junction Stripe (TJS) laser embedded in a GaAs substrate produced using a reduced pressure MOCVD method; a flat layer of GaAs and AlGaAs films on GaAs substrate; one-half to one-third the processing steps of conventional OEIC fabrication methods (liquid phase epitaxy)

  - A surface-light-emitting GaAsAl diffraction lattice junction semiconductor laser for optocomputers; transverse junction stripe (TJS) structure for transverse mode control and distribution feedback structure (DFB) for vertical mode control; continuous oscillation at 867.2nm wavelength; 3mW output vertically from substrate surface

  - A GaAs/AlGaAs direct feedback (DFB) semiconductor laser; 867.2nm wavelength; molecular beam epitaxy method; 30-micron stripe width

  - A dual in-line laser diode (HL1321DL); 1.3-micron wavelength; 14-pin DIL packed module incorporating photodiode monitor and electron refrigeration element; for large-capacity, long-distance optical communication; sampling since March

- Mitsubishi Monsanto Chemical--An epitaxial wafer for infrared LEDs with 50 percent higher output power than GaAs diodes; n-type GaAs layer, p-type GaAs layer, and p-type GaAlAs on an n-type substrate; 940nm wavelength

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- NEC--A visible optoelectronic semiconductor laser using AlGaInP; 678nm oscillation wavelength; 3,000 hours duration at room temperature; 3nm to 5nm light output; heterostructure layer formation technology; 70mA oscillation threshold current; for bar-code readers and laser printers

  - A high-performance, single-frequency 1.5-micron band InGaAsP/InP semiconductor laser for long-distance (300km) optical communications and cable TV transmission; tunable direct feedback (DFB); 5.8nm beam at 720 GHz; continuous wavelength tuning; optical heterodyne transmission featuring 10 to 100 times higher reception sensitivity than direct detection methods

  - A 3.6Gb/sec. communications optoelectronic IC (OEIC); 1.3-micron wavelength light signal receiver element and electronic processing circuit on one chip; InGaAs and GaAs crystals grown alternately on InP substrate using MBE method; commercializa- tion within two years

  - Two photointerrupters coupled with receiving and emitting diodes in one package using ultrathin mold resin; models PS4601/PS4602 insertable into 2.5mm packages

- NTT--A 1.3-micron wavelength InP/InGaAsP direct feedback (DFB) semiconductor laser; 0.02nm/mA small beam width

- Oki Electric--A superhigh-speed optoelectronic IC (GaAs/GaAlAs heterojunction OEIC) for future parallel processing of optical computers; 10x10 chip configuration enabling 100 times faster switching than supercomputers; 1ns switching speed; 200mW signal output capacity; face illumination and optical amplification; four-layer structure with p-type and n-type semiconductors laminated alternately with GaAs and GaAlAs

- Sanyo--Three-beam monolithic laser diode; 20mA write/erase; 50mA read; 20mW output; 100,000 hour life; for rewritable optical disk filing systems; sampling at ¥200,000 ($1,428)

- Sharp--Five ultrasmall semiconductor lasers; 5.6 x 3.5 and 6.5mm leads; LT022PS (60dB) sampling at ¥2,000 ($14.29); LT023MS/PS (80db) sampling at ¥2,300 ($16.43) and ¥2,350 ($16.78), respectively, for use in CD players, CD-ROM drivers, optical videodisk players, and measuring and control equipment

- Sony--Eight 1W AlGaAs laser diodes; 770nm to 840nm wavelengths; MOCVD method; sampling at ¥2.0 million ($14,286) each; for use in medical, dental, communications, and industrial equipment

- Toshiba--10ps optoelectronic IC for future optical computers; four-layer GaAs/GaAlAs structure with p-type and n-type

  - A 656nm output semiconductor laser for laser disks; 0.8-micron beam diameter; for use in high-resolution laser printers and point-of-sale systems; extends high-definition TV (HDTV) picture laser disk playing time from 30 to 45 minutes; no commercialization plans due to lack of international HDTV standards

  - A high-performance triac-type photocoupler to eliminate external mounting of electromagnetic relays and bidirectional thyristors

Image Sensors

- Canon--An 80dB base store image sensor (BASIS) for EOS650/620 autofocusing camera lenses; 5V; 10mW power consumption

- Hitachi--A MOS image sensor for black-and-white TVs; 1/60- to 1/15,750-second shutter speed; 2/3-inch; 320,000 pixels (649 x 491); 8.8 x 6.6mm chip; 1/2-inch being developed

- Matsushita--A solid state 1/2-inch CCD image pickup device with 670 horizontal picture elements; 380,000-element CCD (MN3761) for PAL broadcasting method; 330,000-element CCD (MN3751) for NTSC; sampling at ¥30,000 ($94.80)

- Mitsubishi--Infrared CCD sensor; 260,000 elements; 1.6 x 1.2cm chip; capable of detecting 3.0- to 5.0-micron wavelengths; temperature resolution three times higher than other models; for use in defense equipment and night-vision cameras

- NEC--Two high-sensitivity 1.5-inch CCD image sensors; 250,000 imaging elements; 50 percent reduced power consumption and reduced image smear; MuPD3530D for NTSC system video systems featuring 12 horizontal x 492 vertical imaging elements; MuPD3535D for PAL systems featuring 582 vertical imaging elements; 350-line picture resolution; 0.01 percent smearing; sampling at ¥20,000 ($142.85); 100,000 units monthly from late 1987

- Toshiba--A smear-reducing line address type CCD; 1/2-inch; 300,000 elements; for future high-definition TV/VTR cameras

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Gallium Arsenide

- Hita Electric--A GaAs optical transmitter IC with 1Gb/sec. data-handling capability; 800Mb system for eight-channel multiplex high-speed optical transmission possible by combining device with multiplexer and demultiplexer

- Hitachi--A high-speed FET using lanthanum hexaflouride, which offers high-temperature heat resistance, nonreaction with GaAs materials, and high potential difference with the GaAs substrate; jointly developed with MITI's Optoelectronics Joint Research Laboratory; major step toward 256K GaAs VLSI development

- Mitsubishi--A 15ns 16K GaAs SRAM; 5.8 x 4.7mm chip; 1 watt power; ISSCC 1987 paper

  - Five 14-GHz high-output GaAs FETs (MGFK series); 0.3 to 5.5-watt output; 5.5dB to 8.0dB noise factor; 14.0- to 14.5-GHz frequency range; MBE process technology; sampling at ¥13,500 ($95) to ¥120,000 ($800); for use as signal amplifiers in communications satellites

  - Mass production technology for HEMT GaAs FETs using electron beam epitaxy (MBE) and a proprietary low-noise process; thin films of AlGaAs and other III-V compound materials on a GaAs substrate; 1.5/1.4/1.3dB maximum noise indexes; 10.5dB minimum noise gain level; commercial and industrial use series (MGF4400) sampling at ¥12,000 to ¥45,000 ($85.70 to $321.43); consumer use (MGF4300) at ¥9,000 to ¥30,000 ($64.29 to $214.29)

  - A GaAs microwave monolithic IC (MGF7201) with 2.4-watt output at 28 GHz; electrical power distributing circuits and GaAs FETs on same substrate; eight-cell layout; FETs on GaAs substrate, with hole punched between neighboring FETs to link both sides of substrate surface; eight gates of 0.5 x 100 microns; for satellite communications; commercialization in two years at about ¥400,000 ($2,667)

  - A monolithic microwave IC (MMIC); 30mW output; ¥15,000

- NTT--A heterojunction bipolar transistor (HBT) featuring a sandwich structure of GaAs collectors and AlGaAs base and emitter transistors on a GaAs substrate; 1ps electron flow attained using beryllium impurities and altering aluminum volume; 17.2ps ring oscillator developed using this process

- Sony--Three HEMTs (2SK878-1/2/3) for satellite broadcast receivers and antennas; 1.3-decibel noise factor; microwave signals up to 16 GHz; sampling since February at ¥10,000 ($65.79), ¥8,000 ($52.63), and ¥6,000 ($39.47), respectively

- Toshiba--A 4-bit single-chip GaAs multiplexer and demultiplexer device for optical communications systems; 500 to 700 elements; 2 to 3 GHz; 1.8mm square chip; 28-pin flat package; 0.57W at 2.46 GHz; 1.0-micron gate width; 1.8 x 1.8mm chip; 2 gigabit per second data processing; commercialization within several years

Josephson Junctions

- Fujitsu--A 1ns 16-bit ALU using three Josephson junctions; 8-bit shift register and 16 x 16-bit multiplier; niobium superconducting wire; 9.2ps average gate delay; 1ns chip execution time; 20mW power consumption

Superconductivity

- Furukawa Electric--A commercial superconducting magnet with 14.3 tesla (1 tesla = 10,000 gauss) strength, employing an in-situ method for fabricating the vanadium 3-gallium (V3Ga) coil material; 50mm inner diameter; 360mm outer diameter; 360mm length; two different coils, including a solenoid coil of niobium-titanium superconducting alloy and a pancake coil of V3Ga superconducting material; process invented by MITI's National Metals Research Institute

- Kumamoto University--A ceramic material showing superconductivity at 14 degrees Celsius; requires further verification

- MITI Electrotechnical Laboratory--An oxide substance consisting of lanthanum, strontium, and copper, for which superconductivity occurs at 46 degrees Kelvin (minus 227 degrees Celsius)

- Okazaki National Research Institute (Molecular Science Institute)/ Tohoku University (Research Institute for Iron, Steel, and Other Metals)--A material with superconductivity at 43 degrees Kelvin (minus 230 degrees Celsius)

- STA National Research Institute for Metals--A new ceramic material showing superconductivity at 133 degrees Kelvin; mixture of barrium in a matrix of lanthanum and copper oxide to form a perobskite; headed by Professor Shoji Tanaka

  - A 123K superconductive material consisting of an oxide composed of barium, yttrium, copper, and oxygen in a ratio of 0.6, 0.4, 1.0, and 3.0, respectively; sintered at 1,000 degrees Celsius; 93 degrees Kelvin end-point superconductivity (at which resistance becomes absolute zero)

  - A superconductive wire made of an oxide ceramic composed of lanthanum, strontium, copper, and oxygen; 35K critical temperature; 1,000A/cm square critical current in a magnetic field of 10T

- Tokyo University--An oxide substance with superconductivity at 37 degrees Kelvin (minus 236 degrees Celsius); Professor Kazuo Fueki

  - A substance of barium and oxides of lanthanum and strontium with superconductivity achieved at 35 degrees Kelvin (minus 238 degrees Celsius)

- Toshiba--A ceramic superconductive wire (0.6mm diameter and 20 to 30 meters long) and tape (0.1mm thick, 5mm wide), achieving superconductivity at 87 degrees Kelvin; ceramic material containing yttrium (0.4), barium (0.6), copper, and oxygen (2.3); 30 x 10 x 5mm baked bulk material; superconductivity exhibited at 100 degrees Kelvin and zero electrical resistance at 93.7 degrees Kelvin; critical current density of 101 amperes per square centimeter at 77 degrees Kelvin; research to produce thin-film material to develop superconducting interconnects for semiconductors

Standard Logic

- Hitachi--A 63ps logic circuit using SICOS (sidewall contract structure); NPN and PNP transistors on a single chip; structure; complementary low-power circuit for image processing and data communications; 7.3-GHz frequency divider (1/128) developed using this process

  - A frequency logic IC for automatic controls requiring safety features; on and off functions governed by binary numbers; capable of identifying circuit breakdowns requiring fail-safe operations

- A Hi-BICMOS data transmission IC (HD15307/153009); 2.0-micron rule; sampling since April; ¥3,000 ($21.43) each or ¥1,800 ($12.85) each in 10,000-unit orders

- NEC--High-speed CMOS logic ICs (MuPD74AC series); 2.0-micron process; 3.5ns delay time; 34mA output current; 14- and 20-pin DIP and miniflat packages; sampling at ¥100 ($0.67) per unit for gate model (MuPD74AC00); production of 100,000 units monthly in fiscal 1987 and 500,000 monthly in fiscal 1988

  - ACOS Systems 930/910/830 featuring 1Mb DRAMs, 100ps 1,000-gate logic chips, and 170ps 4,000-gate logic chips

- Sharp--Fifty-nine CMOS logic cell models with 0.58ns gate delay time, including standard cells, function cells, and buffer cells; five chips for high-definition TV DSP; commercialization by 1990

- Toshiba--BICMOS standard logic series (TD74BC); bipolar output parts and CMOS input and logic control functions; 3ns propagation delays; 15mA current at 20 MHz; maximum 64mA electric current driving capacity; series of 50 devices by late 1987

  - A high-speed CMOS logic IC (TC74AC series); quad 2-input NAND gate; 3ns delay time; 150-MHz maximum clock frequency; 0.01uW power consumption; 1.4V/1.4V noise margin

  - A BICMOS 16 x 16-bit multiplier with 7.4ns cycle time; 195ns average gate delay; 400mW power dissipation; 3.3V; 0.6-micron design rule

Linear/Analog

- Epson--A 2.5- to 20-MHz crystal oscillator IC; CMOS outputs; 5ns to 8ns; 10mA power consumption; 14-pin DIP; sampling at ¥1,000 ($7.14)

- NEC--A single-chip linear IC for AM tuners (MuPD1322CA); up-conversion method; RF tuning circuit not required; sampling at ¥600 ($4.03) each; 400,000 units per month

- Sony--A prototype 8-bit A/D converter with 350-MHz clock speed for use in measuring instruments and radars; sampling 300-MHz model (CXA1176K) at ¥270,000 ($1,753) and 200-MHz version (CXA1076K) at ¥180,000 ($1,168)

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Power ICs

- Matsushita/Mitsubishi--A jointly developed control IC for switching power supplies; marketed under own brand names

- Mitsubishi--Four multifunction power supply ICs; M5290P and M5292P for fixed-output power supply; built-in system reset circuits for microcomputer protection; sampling at ¥140 ($0.94) each; M5291P/FP for switching regulators; sampling at ¥90 ($0.60) each

Telecom ICs

- Fujitsu--Bipolar multiplexer and demultiplexer ICs for optical communications; two to four channels of signals processed at 3Gb/sec. rate; 1.5-micron design rule; 50 to 100 gates integrated on 2.6mm square chip; 1.5W power consumption; also for use in optical cable TV and large-scale optical LANs

- Toshiba--Application-specific standard products (ASSP) for high-performance modems and data communications; single-chip devices replacing Z80 MPU, SIO, CTC, PIO, and CGC; 80 percent board space reduction

Discretes

- Matsushita--Three high-resolution chroma output transistors for 100-MHz to 200-MHz video frequency bandwidths (2SC4158/2SC4190/M134L); flat double layer (FDL) structure; 0.46 x 0.46mm chip; priced at ¥200 ($1.30)

- NEC--Cylinder-type leadless glass capsule diodes for surface mounting; 1.4mm diameter x 3.4mm length; 64 regulator diode models

  - A small, 3-pin minimold type transistor and diode; 2.0 x 1.25 x 0.5mm; 40 percent size reduction; 50 percent weight reduction

- Shindengen--Eight 1,200V switching transistors (HFX series); 2SC4230/2SC4237 for 2A, 3A, 6A, and 10A; priced at ¥131 ($0.85) to ¥290 ($1.88) each for 10,000-unit lots; production of 300,00 units monthly, increasing to 1 million units monthly by late 1987

- Tokin--A static induction transistor (SIT) power FET (2SK180 and TS300 Series) designed for induction heaters, high-power ultrasonic generators, wideband amplifiers, and power supplies; 600V to 1,500V carrying capacity; high input impedance level

- Toshiba--Six series of high-speed rectifier diodes for switching frequencies up to 500 kHz; 35ns reverse recovery time; sampling at ¥140 ($0.92) to ¥230 ($15.23)

New Semiconductor Functions

- Matsushita--Test-manufactured, 3-D dual-layer 8K SRAM using two argon lasers to recrystallize polycrystalline silicon onto single crystal silicon; 7.5 x 8.0mm chip; 3.0-micron CMOS process; plans for three-level devices for use in 64Mb+ DRAMs; sponsored by MITI's Future Electron Devices Project

- MITI Electrotechnical Lab--A superlattice Hall device featuring superlattice structure of AlGa and GaAs on GaAs substrate; 12V maximum output at 10,000-gauss magnetic field; Nippondenso studying practical applications

- Tokyo Institute of Technology--A computerized biosensor system for cancer diagnosis; tissue samples react with monoclonal antibodies labeled with fluorescent substance to distinguish malignant cell growth; highly sensitive camera equipped with a biosensor device; Professor Isao Karube

Materials

- MITI--A Basic Materials Industry Symposium held in March to discuss demand expansion for major metals makers

- Osaka University--A diamond film covering for semiconductors and machining tools; diamond material gas ionized into plasma, which is magnet-controlled to achieve the optical state for diamond synthesis; 3cm square area film; diamond film synthesized through electron cyclotron resonance (ECR)

- Toray Silicone--A midlayer material (TSIR series) for three-layer resist used in submicron lithography (0.8 microns or less) for 4Mb and 16Mb DRAMs; sampling at ¥7,500 ($53.57) per 50 cubic cms; radiation resistant

- Toshiba--A new material and technology capable of 0.5-micron processing by using ultraviolet lithography; diazonium salt evaporated thinly on resist; for use in 16Mb+ DRAMs

Manufacturing Processes

- Hitachi--A new technology capable of 0.1-micron geometries by combining electron beam and tele-ultraviolet rays (SPACE process); an ultrathin "skin" formed on surface of photoresist film using a tele-UV ray; E-beam used to draw circuit patterns; 0.1-micron line width and 0.2-micron space width commercially possible using an E-beam system

- Matsushita--A new plasma process (ion shower doping) that allows simpler ion implantation equipment; reduction of prices by one-third to ¥60 million to ¥70 million ($390,000 to $450,000)

  - A deep ultraviolet process capable of developing 0.6-micron geometries with equipment designed for 0.8 microns; pattern irradiated with 250mm to 350nm ultraviolet rays after pattern exposure by a 435nm gamma ray stepper; single-phase positive photoresist used; developed at Matsushita's Kyoto Research Institute

  - A new 16Mb circuit technology featuring a proprietary memory cell process that surrounds each transistor with a trench to allow more space to bury capacitors, reducing space requirements by half; EEC circuit to reduce soft error rates; memory data checking and correction at 16-bit intervals; for image processing in high-definition TVs

  - A new bipolar device manufacturing process technology (SDD-1) that prevents damage during ion implantation and dry etching; 14-GHz maximum cutoff frequency; 72ps propagation delay time; unique dummy pattern process and self-matching double diffusion (SDD) process for polysilicon

- MITI Electrotechnical Lab--A device structure allowing 0.025-micron line widths for eventual use in 1Gb DRAMs and 10ps standard logic; gate electrodes (0.020 micron wide and 0.003 micron thick) layered over source electrode, channel layer, and drain electrode; polycrystal silicon gate electrodes on top and bottom of source and drain

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- Nippondenso--A fine-process technology for automotive ICs; 0.8-micron experimental line widths; for automotive custom ICs produced in Kariya plant, Aichi prefecture

- Nippon Seiko--A pattern generator (LZ-340) that combines the pattern-generate and step-and-repeat functions; maximum exposure surface of 17 x 19 inches (431 x 482mm), with ±0.15-micron alignment; priced at ¥200 million ($1.34 million)

- NTT--Formation of a CVD thin film using synchrotron orbital radiation (SOR); work conducted at Ministry of Education's High Energy Physics Laboratory in Tsukuba Science City; also a 0.01-micron ultrafine etching technology for next-generation ULSIs

- Osaka University--An X-ray exposure method capable of 0.1-micron patterns for 64Mb and 100Mb DRAM production; developed at the laser nuclear fusion research center

- Shinku Yakin--A new thin film technology (gas vapor deposition) that uses a small pipe to spray ultrafine metal particles onto a semiconductor substrate at normal room temperature; system consisting of ultrafine particle generator chamber, carrier pipe, and thin-film forming chamber; 50 percent of the material used in sputtering techniques; for multilayered metal, ceramic, and organic films; potential use in superconductors

- Sony--A new thin-film process technique directly from polycrystal silicon; high-quality films produced at two-thirds the processing steps and cost of monocrystal silicon method; for use in SRAM production

Manufacturing Equipment

- Anelva--A single-wafer plasma CVD machine (ILV-9001) for silicon nitrate film; 30 wafer starts (6 inches) per hour; priced at ¥150 million ($926,000); plans to ship 50 units in three years

- Fuji Electric--An automated chemical station capable of etching, resist film separation, and chemical cleaning for class 10 clean rooms

- Japan Science Association--Development of synchrotron orbital radiation (SOR) technology; silicon compound films using CVD and oxygen etching

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- Matsushita/Nikon--An agreement to jointly develop an i-line stepper and excimer laser capable of 0.8-micron geometries for 16Mb DRAMs; 0.4-micron circuit already designed by Matsushita; Nikon steppers for 4Mb DRAMs available; development at Matsushita's ¥20 billion ($142 million) semiconductor R&D center in Osaka; marketing from 1988

  - A new lithography that enhances stepper resolution by 0.2 micron; less costly and less complicated than multilayer resist method or contrast enhancement lithography; ultraviolet rays applied after a single-layer resist exposed; usable in lithography systems based on excimer lasers or electron beam

- Matsushita--An experimental 248.3nm krypton fluoride (KrF) excimer laser stepper and single-layer photoresist capable of 0.4- to 0.5-micron geometries for 16Mb DRAMs; 15 x 15mm square exposure area using a monochromatic lens; plans for commercial system by 1988 for 16Mb DRAMs

  - A multifunctional chip parts mounting machine (Panasert MPA) with recognition camera capable of mounting 1.6 x 0.8mm chips to 36mm square quad flat packs; ±50-micron accuracy; loading capacity of 40 reels of taped parts

- NEC--A memory repair machine (SL492A) with 10 times higher alignment resolution and 12 times faster than conventional models; YAG laser to cut superfine redundant circuit wiring; 0.5-micron processing accuracy; 0.02-micron positioning resolution; for 4Mb+ DRAMs; priced at ¥130 million ($802,469)

- Nikon--An X-ray lithography machine (SX-5) for 16Mb DRAMs; electron beam-exciting X-ray source (7.1A wavelength); 0.5-micron resolution at large exposure range (29 x 29mm); X-ray power of 0.5mW per square cm; 0.15 micron alignment accuracy; processes six 4-inch wafers per hour; adaptable to 3- to 6-inch wafers; priced at ¥250 million ($1.54 million); five units planned in 1987

  - A high throughput stepper (NSR-1505G4D) for 4Mb DRAMs; 0.45-micron lens opening; 0.75 micron resolution; 15 x 15mm to 17.5 x 12mm exposure area; 700mW per square centimeter exposure power; throughput of 60 5-inch wafers per hour or 50 6-inch wafers per hour; 0.18 micron positioning accuracy

- Nitto Kogyo--A bulk-feeding automatic IC mounting system for use with one-by-one automatic mounting systems; 10,000 chip parts air shot into outlet one at a time; 20 hoppers for each unit

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- Osaka University--An X-ray lithography system capable of fabricating 64Mb to 100Mb VLSIs; 0.1mm-cube target of xenon gas frozen solid with liquid nitrogen irradiated with laser light, which is converted to X-ray beams at 1 million degrees Celsius; 10-watt output X-ray capable of drawing 0.1-micron pattern lines

- Sanyo--An automatic chip mounting machine (TCM-60) that applies bonding agent to two PCBs simultaneously; one-by-one mounting system suitable for 8mm-wide tape and odd-shaped parts on 32mm tape; 0.25 second per part mounting speed

- Sony--A reticle-quality automatic evaluation system (ARQUS-20) capable of detecting defects of more than 0.8 micron; priced at ¥80 million ($493,827); sales by Marubeni Hytech; sales goal of 10 units in 1987

- Sortec/MITI's Institute of Physical & Chemical Research--Joint R&D with 20 companies to develop a large synchrotron orbital radiation (SOR) facility for ultralarge scale integrated (ULSI) circuits and basic physical and biological research; Hitachi Ltd., Kobe Steel, and Sumitomo Heavy involved

- Tokyo Ohka--An ECR etching machine (TSME-5300) adaptable to 4Mb DRAMs; 40 6-inch wafers per hour throughput; 3,000 Angstroms per minute etching speed; cassette-to-cassette transport system; poly-silicon etching evenness of ±1 percent

- Toshiba--A stepper with experimental SOR (synchrotron orbital radiation) source; 0.03-micron alignment accuracy in test wafers; technical breakthrough for 64Mb DRAM development

- Toshiba Ceramics--Development of a high-purity quartz lens for fabricating 64Mb DRAMs using steppers equipped with excimer lasers; 0.193-micron wavelength light region; plans to sample in four to five years

- Yamaha Motor--A high-speed chip mounting system (YM4600S) with 0.9ns mounting time; 1,145 x 960 x 1,246mm dimensions; 8mm or 12mm tape or direct feeder; 46 chip types; one-head system with CRT and controller priced at ¥4.9 million ($35,000)

Test Equipment

- Advantest--A VLSI test system (T3381) capable of testing 512 I/O pins at 100 MHz and 256 I/O pins at 200 MHz in pin multiplex mode; ±500ps timing accuracy; test period of 10ns to 16ms; 125ps resolution; dual user/test processor system; priced at ¥300 million to ¥700 million ($1.85 million to $4.32 million); sales target of 50 systems in 1987; shipments from June 1987

  - An integrated test system (DIC-9035B) for ASIC tests at 200-MHz rate; 512 I/O pin capability; ±300ps calibration; for ECL, GaAs, multibit MPUs, and other high-speed devices; pattern memory of 512 kilowords

  - AVLSI test system (DIC-8034E/E) for multibit MPUs and gate array R&D; 40-MHz test rate (MUX mode); 256 I/O pin capability; serial pattern generator to test scan design devices

  - A LSI tester (DIC-8035B); 80-MHz test rate (MUX mode); 256 I/O pin capability

  - A memory test system (DIC-8046) with 60-MHz test rate for GaAs memories, 16Mb DRAMs, and other high-speed memories; full-scale evaluation of VRAMs, dual-port memories, and ASIC memories

  - A memory test system (DIC-8042) with 40-MHz test rate, capable of parallel testing of 16 high-speed SRAMs, ASIC memories, and 4Mb DRAMs

  - A 20-MHz memory test system (DIC-8020B/E) for 256K and 1Mb DRAMs, and 64K and 256K SRAM mass production

  - A linear IC tester (DIC-8060) for audio/video ICs and A/D devices; 128-pin, 20-MHz (MUX mode) function test

  - An ultrahigh-speed DC tester (DIC-8055) for linear and standard logic ICs; 128-I/O-pin capability; DC/pin architecture

  - An analog LSI testing system (T7361) capable of testing 150-MHz digital pattern rate; priced at ¥70 million ($432,099)

  - Five handlers; AHM-750H for QFPs, PLCCs, and PGAs; AHM-645L for high pin count PLCCs and LCCs; AHM-646 for parallel ZIPs; AHM-633C for 16 parallel DIPs; AHM-671 for -55 to 125 degrees Celsius testing

- Hitachi Electronics Engineering--A wafer surface tester (LSI-5000) for 4Mb memories; capable of inspecting defects (haze and slip line) at 0.16-micron accuracy; priced at ¥28 million to ¥30 million ($172,840 to $185,200); sales target of 70 to 80 units in first year

- Minato Electronics--A memory test system (Model 9600/32) capable of parallel measurements of 32 memories simultaneously

- Sharp--A noncontact, nondestructive trench-etching measurement testing system for 4Mb+ DRAMs; ±0.2-micron measurement accuracy; 40 second measurement time; 0.8 x 5.0-micron trenches can be measured; marketing by Dai-Nippon Screen Manufacturing

- Yokogawa Hewlett-Packard--An analog LSI tester (9480) capable of testing up to 128 MHz; priced at ¥60 million to ¥200 million ($370,370 to $1.23 million); sales target in first year of 50 units worth ¥7 billion ($42.21 million)

Packaging

- Matsushita--An S-mini-type package adaptable to surface-mount devices; for volume production of 71 models of transistors and diodes

  - A chip-on-board (COB) technology; up to 10-micron pitch; 3- to 5-micron thick gold bond on electrode pad; 1,000-hour lifetime at 125 degrees Celsius

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COMMENTARY

The Worldwide Race to Commercialize Superconductors

Although European and U.S. researchers have a slight head start in superconductor research, Japanese companies are throwing significant funding and researchers into the field. Mitsubishi, for example, has formed a team of 220 researchers. According to a recent Japan Economic Journal survey, half of the Japanese researchers interviewed believe a high-temperature superconducting material will be commercially available within one to three years, and that superconductors will be commercialized within five to ten years. Japanese researchers predict that the Japanese superconductor market could reach ¥1 trillion to ¥3 trillion ($6.7 billion to $20.0 billion) by the year 2000. If a room-temperature superconductor is developed, they believe this figure could reach ¥10 trillion ($66.7 billion).

Dataquest observes that superconductive magnetic sensors are already being sampled in Japan, and that a prototype three-terminal switch (phase quantum tunnel device) that requires less electricity than Josephson junctions has been announced by Yokohama National University. Based on these rapid developments, we believe prototype switching devices will be developed within the next two years. Table 1 lists the major government-sponsored superconductivity programs currently proposed.

Table 1

Major Japanese Ministry Superconductivity Programs

Ministry	Program
MITI	International Superconductivity Industry Technology Promotion Center
	Supercomputer Program (Large-Scale Project/Josephson)
	Energy-Generation Technology R&D Program
	Next-Generation Industry Basic Technology R&D System (new materials, devices, and logic)
Science & Technology Agency (STA)	Multi-Core Project
	Superconductive Material Technology Center
	New Superconductive Material Research Association
Education (MOE)	Science Research Financial Assistance Program (¥169 Million/ $1.1 Million)
	Tokyo University Special Research (Professor Shoji Tanaka ¥260 Million/$1.73 Million)

Source: Nikkei Microdevices

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In April, MITI's Agency for Industrial Science Technology (AIST) held a conference to develop industrial technology for superconductive ceramics. The conference was headed by Professor Shoji Tanaka of Tokyo University's Engineering Faculty, the first Japanese researcher to demonstrate an experimental superconductive ceramic, and involved 20 researchers from universities, government agencies, and industry.

In June, the Ministry of Education established a ¥169 billion ($1.13 billion) science research fund to finance high-temperature superconductor research.

Recently, the Science and Technology Agency (STA) announced its new superconductor program, the Multicore Project, for fiscal 1988 (beginning April 1, 1988). Budgeted at ¥2.3 billion ($16.5 million), the project will focus on 15 research cores, as shown in Table 2.

This winter, JSIS will issue a special report on the status of Japanese superconductor research and commercialization plans. For more details, see the section entitled "Superconductivity" that appears later in this service section.

Table 2

STA's Superconductor Multicore Project

Research Core	Millions of Yen	Thousands of Dollars
Superconductivity Theory	¥ 6.0	$ 42.0
Research Data Base	55.3	387.0
Process Exploration	107.0	748.0
Purification Processes	0.0	0.0
Thin-Film Processing	210.1	1,469.0
Single Crystal Processing	31.6	221.0
Lithography Processing	27.2	190.0
Conductor Processing	0.0	0.0
Space Environment Processing	0.0	0.0
High-Field Properties	1,035.2	7,239.0
Crystal Structures	400.3	2,799.0
Chemical Compositions	97.2	680.0
Neutron Irradiation	381.7	2,669.0
Physical and Analysis	0.0	0.0
Total	¥2,351.6	$16,444.0

Source: U.S. State Department

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MAJOR TECHNOLOGY TRENDS

During the second quarter of 1987, Dataquest observed the following trends in Japanese semiconductor technology:

- The Ministry of Finance agreed on two-year tax credits for corporate R&D investments.
- Japanese IC card makers and systems houses are developing a wide variety of new factory automation (FA) and medical applications for IC cards.
- The Japanese government called for a ¥6 trillion ($40 billion) space program to catch up with other nations.
- Japanese carmakers such as Mazda and Nissan are expanding their electronics research centers.
- The Japanese government announced plans to finance half of the ¥1 trillion ($7.1 billion) Human Frontier Program for next-generation life-science research.
- Japan has 107 ASIC design centers, 32 percent more than last year, which explains the fierce price competition ($0.0013 to $0.0016 per gate for 2,000-gate CMOS array in April 1987, or 15 percent less than at the end of 1986).
- Japanese IC vendors Fujitsu, Hitachi, Matsushita, Mitsubishi, and Toshiba introduced prototype 32-bit TRON chips.
- The Japan Optomechatronics Association was formed to develop next-generation video media technology.
- The Institute for New Computer Technology (ICOT) and the AI Center forecast a Japanese AI software market of ¥4.8 trillion ($32 billion) in 1995, of which ¥660 billion ($4.4 billion) will be merchant sales (excluding captive use)—or only 13.8 percent.
- Hitachi is developing an inorganic light-sensitive material for 64Mb+ memories.
- With NTT's 16Mb DRAM announcement, Japanese companies are actively exploring new applications for dense megabit memories, such as voice recognition/synthesis, memory cards, "silicon disks," video memories, and electronic dictionaries.
- NEC announced a prototype 32-bit V80 MPU series.

- Japanese IC makers are actively developing voice recognition/synthesis and graphics chips for next-generation word processors, lap-top PCs, and other office systems.

- Fujitsu announced wafer scale integration technology.

CORPORATE R&D ACTIVITIES

In April, Fujitsu added a second building at its Atsugi Semiconductor Research Laboratory, which is located across the street from NTT's Atsugi Semiconductor Laboratory (which also added a second building recently). The new Fujitsu building has seven floors and a basement, dimensions of 102 x 89 x 31 meters, 4,500 square meters of floor space, and clean rooms in the basement and on the first, second, and third floors. A class 10 superclean room has been installed for high-electron mobility transister (HEMT) and submicron research. Testing is conducted on the fourth through sixth floors. The library, computers, and research offices are located on the seventh floor. The total investment was ¥10 billion ($66.7 million). Researchers in the new building are focusing on submicron devices, HEMT, optoelectronic devices, holographic sensing, and high-speed devices. Fujitsu researchers at Atsugi total 830 people. Fujitsu also created special R&D divisions at its Kawasaki plant near Tokyo and at the Mie plant near Nagoya.

In May, Nissan Motors invested ¥3 billion ($20 million) in an automotive LSI development center at its Yokosuka Central Laboratory in Kanagawa Prefecture. The three-story center has 5,000 square meters of floor space and a clean room (below 0.1-micron dust particles) for submicron ICs using 6-inch wafers. Nissan's top-of-the-line Leopard model uses 142 LSIs and 200 transistors. Hitachi, NEC, and Toshiba have been major suppliers. In fiscal 1986, Nissan consumed about ¥20 billion ($133 million) in semiconductors.

In May, Japan Victor Company (JVC) opened the ¥10 billion ($66.7 million) Kurihama Technology Center. The six-story facility has 13,300 square meters of floor space on a 37,000-square-meter lot. The 500 researchers and support staff will focus on new audio-video, computer, and device technologies, such as new function ICs, new media materials, packaging, and communications systems. A superclean room was built also.

In May, Ricoh opened a ¥3 billion ($20 million) semiconductor design technology center within its Ikeda Plant in Osaka. The 1,900-square-meter center has two floors above ground and one floor underground. A host computer and workstations offer a VLSI design library and an ASIC data base. Five years ago, Ricoh entered the semiconductor merchant market and has opened design centers in Tokyo and Osaka.

In April 1987, Sumitomo Electric opened a new 10,000-meter research facility at its Yokohama Research Center for optoelectronics research. About 70 of the 230 researchers at the center are assigned to the facility, which has a clean room for high-density ICs.

In June 1987, Mazda announced its new Yokohama Research Center for advanced electronics and computer technologies. The ¥500 million ($3.3 million) six-story center, excluding land costs, will have a staff of about 70.

TRON Project

Major Japanese semiconductor makers are planning to commercialize 32-bit MPUs based on the TRON architecture in the near future. Fujitsu, Hitachi, and Mitsubishi are jointly developing the G-Micro series, with plans for sampling in the first half of 1989. Table 3 provides the specifications for the various TRON chips.

- Fujitsu—A 900,000-element, 20-mips processor (32/300)
- Hitachi—A 700,000-transistor, 10-mips processor (32/200)
- Mitsubishi—A 300,000-element, 10-mips processor (32/100)

The low-end devices will be designed for PCs, medium-end devices for workstations, and high-end devices for minicomputers. The three companies are also conducting joint development of microperipherals, TRON architecture, UNIX operating system, and C language.

Table 3

Japanese 32-Bit TRON Chip Specifications

Features	Hitachi, Fujitsu	Matsushita	Mitsubishi	Toshiba
Model	H32/200 F32/300	N/A	M32/100	TX3
Processing Speed	6 mips (20 MHz)	6 mips (20 MHz)	4-5 mips (20 MHz)	8-10 mips (25 MHz)
Clock Speed	20/24 MHz	20 MHz	20/25 MHz	20 MHz
Design Rule (Microns)	1.3/1.0	1.0-1.2	N/A	1.0

(Continued)

Table 3 (Continued)

Japanese 32-Bit TRON Chip Specifications

Features	Hitachi, Fujitsu	Matsushita	Mitsubishi	Toshiba
Process	CMOS	CMOS	CMOS	CMOS
Internal Transistors	700,000	500K-600K	300,000	1,000,000
32-Bit Registers	16	16	16	16
Data/Address Bus Width	32/32	32/32	32/32	32/32
Real Address Space	4GB	4GB	4GB	4GB
Shortest Bus Cycle	2-clock	2-clock	2-clock	2-clock
No. of Pipelines	6	N/A	5	7
On-Chip MMU	Yes	Yes	No	Yes
Cache Memory (Instruction)	1KB	1KB	No	2KB
Cache Memory (Data)	128-byte	512-byte	No	2KB
Ring Storage Method	4-level	4-level	2-level	4-level
Pin Count	135	N/A	130	135
Package Type	PGA	PGA	PGA	PGA
Sampling Date	Late 1987	Future	1988	1989

N/A = Not Available

Source: Nikkei Electronics

Toshiba is developing the TX3 TRON chip with 8- to 10-mips processing capability, and plans to market it in 1988. Matsushita plans to commercialize models in 1988.

Japan Optomechatronics Association

In July, the Japan Optomechatronics Association was established to develop next-generation image media technology. The association president is Mr. Ukita, the Mechanical Research Lab Director at MITI's Agency for Industrial Science and Technology (AIST). Canon, Daikin, Fujitsu, Hoya, NEC, NTT, and Olympus are some of the 101 participating companies. The association is located in the Tokyo area (phone: 0424-75-4051).

In a related matter, Matsushita announced a new high-speed optical computing technology featuring switching speeds of 200ps. Until now, NTT had the fastest circuits at 5ns.

Optoelectronics Research Association

In April, the Optoelectronics Research Association opened the Tsukuba Research Center to pursue basic research in second-generation optoelectronic ICs (OEICs) for future optocomputers. The ¥1 billion ($66.7 million), 10-year project is staffed by 21 researchers from 13 participating companies.

Optical Memory Card R&D Consortium

In June 1987, 21 Japanese companies and institutions formed an optical memory card study group to set interindustry protocols for the laser-memory cards that are being promoted by the Ministry of Health and Welfare for Japan's health insurance program. The consortium is led by Mitsubishi Corp., Kyowa Bank, and Nippon Medical College, and includes IBM Japan, Canon Sales Co., Intec, Seibu Department Stores, Ohbayashi, Shiseido, Dentsu, Toho Mutual Life Insurance, Nippon Shinpan, Honda Motor, Mitsui Trust & Banking, and Bank of Yohohama. The group will begin experiments in 1988 to develop a cross-industry system. Canon Sales will provide cards and readout devices, while IBM Japan and Intec will handle software development and system organization. The study will last until April 1989. Optical card applications include medical record keeping, credit cards, receipts, electronic securities, financial transaction certificates, student identification, and ticketing. Japanese companies are currently studying market segmentation of IC cards and laser (Drexler) cards.

New R&D Centers

Asahi Chemical established a Resin Technology Center at its Kawasaki factory, and plans to spend ¥1.5 billion ($10 million) for construction. In January 1988, the center will be opened to domestic customers for closer cooperation in designing products. It will develop resin applications and technology as well as information services.

Toshiba Corporation completed a Semiconductor System Technology Center in the Technopia Block in Kawasaki, Kanagawa Prefecture. The center is the nucleus of the company's 10 LSI design centers at home and abroad. The 14-story building has 52,000 square meters of floor space, including 60 rooms for design and evaluation. Capital investment totaled ¥23 billion ($165 million). The facility currently houses 1,800 staff members.

In May, Advantest began construction of a research laboratory for basic and applied research in new devices and testers. The three-story, 4,000-square-meter laboratory will opened in April 1988, initially with 20 staff people.

GOVERNMENT R&D PROJECTS

Sortec

In June 1987, Sortec Corp., which was established by the MITI/MPT Japan Key Technology Center and 13 companies, announced plans to build a Tsukuba Research Center in September 1988 to conduct research on SOR (synchrotron orbital radiation). The research center will have two buildings: a research building with 1,200 square meters of floor space and a laboratory work building with 3,300 square meters of space. Construction costs will total approximately ¥2.5 billion ($17.5 million).

MITI Sigma Project

In June, the Information Processing Association (IPA) began installing the Multi-Word System (GMW), developed by Tateishi Electric and other companies, to Sigma workstations. IPA's goal is to develop a Sigma standard software system, Multi-Media Word, capable of handling characters, graphics, and figures.

National R&D Tax Credits

In June, the Ministry and Finance (MOF) and Ministry of Construction (MOC) agreed on special two-year tax credits for corporate R&D expenses. The R&D tax reduction provision, which will total ¥30 billion to ¥50 billion ($200 million to $330 million), was included in the special tax bill in this summer's extraordinary Diet session and will be tentatively implemented by the end of 1987. The measure:

- Increase, the tax-credit rate on lab research expenses from 20 percent to 30 percent of the increase in R&D expenses over a certain level
- Raises the credit ceiling amount from 10 percent to 15 percent of a company's corporate tax

- Permits greater tax breaks for facilities and equipment for new technologies such as bioengineering, new materials, and space development, and allows a 10 percent deduction on the price of new equipment (versus the current 7 percent) from tax amounts

- Credits 5 percent of new facility construction costs against the company's total tax amount (applicable only to nonexport-boosting investments)

MITI Fiscal 1987 Research Budget

In fiscal 1987, MITI's total budget has declined by 16.8 percent to ¥650.6 billion ($4.34 billion). As shown in Table 4, MITI's electronics-related R&D budget has increased 5.5 percent to ¥144.3 billion ($961.8 million). Large-scale project funding was cut 0.5 percent, while funding for the Basic Technology Research Promotion Center and the Fifth Generation Computer Program increased 0.5 percent and 22.0 percent respectively.

Table 4

MITI's Fiscal 1987 Electronics-Related Budget
(Partial List)

Program	FY1986	FY1987	Percent
Human Frontier Science Program	¥ 0	¥ 47	100.0%
Next-Generation Industries Basic Technology	6,350	6,043	(4.8%)
Large-Scale Projects	15,176	15,095	(0.5%)
Basic Technology Research Promotion Center	20,500	25,000	22.0%
Fifth-Generation Computer Program	5,491	5,631	2.5%
Technopolis Promotion Survey Research	0	40	100.0%
Information Technology Promotion Agency	6,142	6,460	5.2%
Other Programs	83,038	86,007	3.6%
Total	¥136,697	¥144,323	5.6%

Source: MITI

Human Frontier Science Program

In June, Prime Minister Nakasone announced at the seven-nation Vienna Summit that Japan will finance half of the ¥1 trillion ($7.1 billion) Human Frontier Science Program, which will promote international cooperation in basic life science research. The project will focus on organic mechanisms, ranging from genetic information to morphogenesis and molecule-level recognition and response systems. Five research objectives will be emphasized: training of engineers, research subsidies, entrustment of studies, international conferences, and data base development. Dataquest notes that MITI recently initiated its Biochip Project to develop sixth-generation biocomputers and biosensor devices.

MITI Sigma Project

Kyoto University developed a Window System GMW, which has powerful Japanese language capability for use in Sigma workstations. The window system was used because of the difficulty of modifying X Window and NeWs. Participating companies began developing character and image functions at the end of August.

MITI Fifth-Generation Computer

In 1988, Fujitsu plans to export AI products, including an expert system development tool (ESHELL), an English-Japanese/Japanese-English translation system (ATLAS), and a back-end LISP machine (FACOM).

MITI Supercomputer Project

In June, NEC announced its SX-J supercomputer with 8 bytes of memory storage. Compared with the SX-1E (285 mflops and ¥4.7 million ($31,333) monthly rental), the SX-J has 210 mflops capability and rents for ¥3.38 million ($22,533). Other specifications include 32KB cache memory, 20KB vector and scalar capacity, eight vector/scalar/register 64-bit units, 128 scalar/vector 64-bit units, four vector image pipelines, one scalar image pipeline, 32MB to 128MB vector processor main memory, 32MB to 64MB control processors, 32 I/O channels, 96MB per second data transmission speed, and 100MB per second HYPER channel.

In July, Hitachi introduced two supercomputers. The S-820 Model 80 with 2-Gflops processing speed, 512x32 vector register, eight image pipelines, and 0.5 GB to 12.0 GB expandable memory storage. The S-820 Model 60 has 256x32 vector register storage, four image pipelines, and 0.5 to 6.0 GB expandable memory storage. Both models feature 25ns 7K vector register RAMs, 4ns machine cycles, fast logic circuits (2000-gate per 200ps and 5,000-gate per 250ps), and 20ns 64K main SRAM.

In July, Sumitomo Corporation and Sopack, a Tokyo venture capital firm, developed a parallel processor for superminicomputers, using conventional PCs and minicomputers. The FAP10 uses 30 CPUs, which enable a computing speed of 10 mflops. The system, priced at ¥2.5 million ($16,600), is designed for computer graphics and measurement instrumentation data. Sumitomo is not part of MITI's Supercomputer Project.

Tsukuba University Supercomputer Project

Tohoku University has begun development of a 2-Gflops supercomputer (PAX-256MA) using 32-bit floating-point MPUs. The CPU core will employ Am29325 floating-point MPUs (8 mflops) in the 68020 CPU core, 4KB of dual-port memories, and 5MB of 32-bit parallel transmission. A DMA transmission control circuit will be used between the floating-point data memory and the Am29325 processors. The machine will use FORTRAN 77 and handle vector processing. The completion goal is 1988. The university previously developed the PAX-128 and PAX-64J machines. Trial production of the PAX-256MA is beginning.

MPT High-Definition TV Funding

In June, the Ministry of Posts and Telecommunications (MPT) completed a study that called for financing 50 percent of high-definition TV development costs incurred by electronics and communications companies. MPT is investigating a ¥45 billion ($300 million) annual funding budget. This program is part of MPT's 20-year, ¥60 trillion ($400 billion) program to promote domestic demand expansion in "high vision" television and VTR industries. Dataquest observes that this program will stimulate research in ISDN circuits, image/video signal processors, semiconductor lasers, and other video-related ICs.

MITI's High-Definition TV Research Group forecasts that the high-definition TV market will reach ¥30 trillion ($200 billion) by the year 2000, of which services will account for ¥4 trillion ($26.7 billion).

MITI New Glass Forum

In June 1987, the New Glass Forum announced plans to develop a PC-based data base on high-performance glass. The 87-member group plans to store about 100,000 cases of information on new glass properties and composition, and the potential for integration information on fine ceramics. The group was formed in October 1986 to investigate new glass applications in future communications, data processing, and optoelectronics.

Space Development Program

In June 1987, the Japanese government advisory Space Development Council issued a report calling for some ¥6 trillion ($40 billion) over the next 15 years to finance space stations and other projects. Japan currently trails far behind the United States and the Soviet Union, but sees aerospace as a major growth market. The report focuses on continuing work on ETS–VI engineering test satellites and H–II rockets, large satellites, large rockets, modules for manned space experiments, and joint development of manned space stations with the United States, Canada, and European nations. The responsibility for communications and broadcasting satellites will be shifted to the private sectors by the late 1990s.

NEW PRODUCTS AND TECHNOLOGY TRENDS

Memory

During 1987, many Japanese semiconductor makers have developed 1Mb field memories for VTRs and televisions. Table 5 lists the major field memories announced to date.

- Asahi Chemical
  - A 1K CMOS EEPROM (AK99C46); 64Kx16; 5V power supply; 3mA power consumption during operation; 1mA at standby; automatic read cycle
- Fujitsu
  - A 1Mb CMOS EPROM (MBM27C1028); 64Kx16 and 128Kx8; 150ns; double–poly gate with stacked single–transistor gate cells; single– or 4–byte programming (Quick Pro algorithm); 30mA operating power consumption; 0.1mA standby power; 5V; 28–pin DIP with transparent lid and 32–pin LCC; directly connectable to 8086/80186; programmable in 15 to 20 minutes
  - A 1Mb CMOS EPROM (MBM27C1001); 32–pin CERDIP; interchangeable with 28–pin 1Mb mask ROM; pin–compatible with 28–pin EPROM; 12.5V programming voltage; 200/250ns versions
  - A 64K CMOS EEPROM (MBM28C65–25); 8Kx8; 250ns; 110mW operating power consumption; 550–microwatt standby power; 5V; 28–pin CERDIP; suitable for rapid turnaround, bit–pattern experiments and low power consumption needs

Table 5

Japanese Megabit Field Memory Chips

Company	Model	Memory Size	Input	Output	Package	Power	Size
Hitachi	HM530 51P	1024 x 256 x 4	60	60	18-pin DIP	40mA	N/A
Matsushita	MN4700 4701	512 x 512 x 4	30ns	30ns	40-pin DIP	150mA	5.88 x 11.22mm
Mitsubishi	M5M4C 500L	320 x 256 x 6	50/60	50/60	28-pin ZIP	20mA	5.0 x 10.08mm
NEC	MuPD 41221C	320 x 700 x 1	70/90	70/90	14-pin DIP	55mA	5.69 x 8.05mm
	N/A	263 x 910 x 4	60	60	28-pin DIP	N/A	N/A
NMB	AAA3081K/2K	2Mb x 2 x 8	13/15 25/30	13/15 25/30	40-pin DIP	900mA	N/A
Nihon TI	TMS4C 1050	(256K+150) x 4-bit	30/60	30/60	16-pin DIP	50mA	12.8 x 4.3mm
Oki	MSM514221	320 x 910 x 4	30	30	24-pin	40mA	N/A
	MSM514222	320 x 1,136 x 4	30	30	SOP	40mA	N/A
	MSM514223	480 x 564 x 4	30	30		40mA	N/A
Sharp	N/A	263 x 720 x 6	60	60	22-pin DIP	70mA	N/A
	N/A	270 x 1,024 x 4	60	60	28-pin DIP	70mA	N/A
Sony	CXK 1205P	265 x 910 x 4	NTSC/ PAL	NTSC	28-pin DIP	60mA	N/A
Toshiba	TC521 000P	512 x 512 x 4	30	30	40-pin DIP	100mA	N/A

Source: Nikkei Electronics

- Three 64K CMOS SRAMs (MB81C71/74/75); 25ns; 440mW current consumption during operation; 64Kx1 and 16Kx4; 1.3-micron process; dual-layer polysilicon; 8.1 x 4.1mm chip; plastic DIPs and LCCs; priced at ¥4,000 ($26.67); 100,000 monthly

- A 16K PROM series (MB7230RA/RS); 2Kx8; 24-pin skinny DIP, 24-pin SOP, and 28-pin LCC packages; DIP sampling at ¥3,500 to ¥5,500 ($23.33 to $36.67)

• Hitachi

- An inorganic light-sensitive material for 64Mb DRAM patterns; 1.5-micron-high x 0.2-micron-wide cylinders drawn on a silicon substrate; hetero-polytungsten material; photolithography, electron beam, and X-ray methods used

- Three ultrahigh-speed bipolar RAMs; 6ns 1K RAM (HM10422CG); 5.5ns 4K RAM (HM2144CG); 13.0ns 16K RAM (HM!040CG); 28-pin LCC package

- A test-manufactured 4Mb CMOS DRAM; 4Mbx1 and 1Mbx4; 80ns; 0.8-micron double-well; two-layer aluminum; 6.38 x 17.38mm chip; 110.9-square-mm chip, with sub-100-square-mm planned; 2.2- x 6.7-square-micron cell; 76ns Row Access Sequence (RAS); 36ns address; 45mA power consumption; 1,024 refresh cycle; 8-bit parallel testing; 350 mil (8.89mm) wide SOJ package; mass production around 1989

- Two 10ns 16K ECL RAMs (HM10484-10/HM100484-10); 1.3-micron BICMOS process; 630mW power consumption; 10484 in 28-pin 400-mil (10.2mm)-wide CERDIP; 100484 in 28-pin 400-mil-wide flat package; 10484 sampling at ¥9,500 ($63.33); 100484 at ¥10,000 ($66.00); also HM10480-10/HM100480-10 models in 20-pin 400-mil-wide CERDIP; sampling at ¥9,000 ($60) and ¥9,500 ($63.33), respectively

- A 64K ECL RAM series; HM100490-15 (ECL 100K) and HM10490-12/15 (10K); 64x1; 2.0-micron to 1.3-micron BICMOS process; 12ns data tramission

- Two 4Mb CMOS mask ROMs; HM62304P (x8) in 32-pin DIP; HM62404P (x8/x16) in 40-pin DIP; 200ns; 0.03mA power consumption during operation

- Three 1Mb CMOS DRAMs; HM511000P/01P/02P (1Mbx1) in 18-pin DIP, SOF, and ZIP; HM514256P (256Kx4) in 20-pin DIP, SOF, ZIP; 80/100/120/150ns; 2mA operating power consumption

- Four 1MB DRAM modules; HB56A18A/18B/19A/19B; 30-pin SIP; 100/120/150ns

- A 1Mb CMOS frame memory (HM53051P) for television and VTRs; 160ns; NTSC method; 32x4 I/O; 1.8Mb per field for two chips; 3.7Mb for four chips; 1.3-micron CMOS; 300-mil 18-pin DIP; sampling since August at ¥4,000 ($26.67)

- Two 1Mb SRAM modules (HM66203/204); 32-pin DIP; 100/120/150ns

- Three 1Mb CMOS EPROMs (HN27C101/301); 170/200/250ns; 50mw operating power consumption; 128Kx8; 5mW standby power; 5V; 32-pin DIP

- A 1Mb CMOS pseudo-SRAM (HM658128P); 256Kx8; 32-pin DIP; 100/120/150ns; 0.2mA during operation

- A 256K CMOS EPROM (HN27C256HG); 70/80ns

- A 1Mb CMOS EPROM (HN27C1024G); 64Kx16; 120/150/250ns

- Three 64K CMOS EEPROMs; 8Kx8; HN58C65FP featuring address, data, C, OE, and WE latches, data protection, 32-byte auto page-rewrite, data polling, and RDY/BUSY signal output

• Matsushita

- An 8Mb mask ROM (MN238000) shallow trench technology with low-layered polysilicon self-aligning NAND multigate cell; two-layered polysilicon process; 200ns; 300mW power consumption during operation and 5 microwatt at standby; storage capacity of 14,000 letters; 1Mbx8 and 512Kx16; sampling at ¥5,000 ($35.71); 42-pin DIP; also 64-pin flat package for 8Mb; monthly production of 20,000 to 30,000 units at Uozu factory from October 1987

- A 16Mb mask ROM (MN2316000) using same process as 8Mb; 2Mbx8 or 1Mbx16; 42-pin plastic DIP or 124-pin flat plastic package; 200ns; 5V; 330mW power consumption and 5 microwatt at standby; TTL compatible; ROM code, ion implantation; storage capacity of 28,000 letters; 16Mb model for ¥10,000 ($71.43)

- Two 4Mb mask ROMs; 200ns CMOS 512Kx8 (MN234000) in 40-pin DIP; 250ns NMOS 256Kx16 (MN234001) in 64-pin quad flat pack

- Four MOS mask ROMs; 1Mb (MN231000/1) 250ns CMOS and 150ns NMOS; 256K (MN23258/57) 200ns CMOS and NMOS; 128K (MN23128) 200ns NMOS; 64K (MN2364) 150ns NMOS; 28-pin DIP or SOW-28D

- A CMOS-type MNOS memory series; MN12C201 (16x16; 8.12mm square chip; MN12C25C (38x16, 5.99mm square and 19x16, 6.75mm square types); sampling at ¥400 ($2.67)

- Mitsubishi
  - A VCR/TV field memory for simultaneous recording and replaying (M5M4C5001); specialized 491, 500-bit DRAM with dedicated address counter for memory refresh; 1.6-micron CMOS process; 20mA operating current; 28-pin ZIP; sampling for ¥3,000 ($20); 100,000 monthly
  - A 4Mb CMOS mask ROM (M5M23C400); 8.33 x 8.66mm chip; 1.2-micron process; eight transistors aligned in a series; 165mW maximum power usage during operation; 550nW at standby; 256Kx16 and 512Kx8; 40-pin plastic DIP and 64-pin flat package; sampling for ¥4,000 ($26.67); produced at Kumamoto Works; 50,000 monthly
  - A 1Mb CMOS EPROM (M5M27C100K); 131Kx8; 1.5-micron process; 150/200/250ns; 12.5V programming voltage; 263mW operating power consumption; 6mW standby power; 5V; 32-pin DIP; sampling at ¥5,000 ($33.33) for 150ns version, ¥4,000 ($26.66) for 200ns, and ¥3,000 ($20) for 250ns
  - A 256K CMOS EPROM (M5M27C256K-12); 32Kx8; 1.5-micron process; 120/150/250ns; sampling at ¥3,000 ($20), ¥2,500 ($16.66), and ¥2,000 ($13.33), respectively; 5.43 x 5.41mm chip; 30mA operating power consumption; 100 microampere standby; 5V; 28-pin CERDIP
- NEC
  - A fluxoid transfer memory for Josephson junction computers utilizing superconductors; 43-micron square storage cell; Josephson junction write gate used instead of a SQUID (superconducting quantum interference device); 1ns read time for a 4K device
  - Three 1Mb CMOS DRAMs; high-speed page mode (MuPD421000), nibble mode (MuPD421001); static column mode (MuPD421002); 1.0-micron process; trench capacitors, dual-layer poly-silicon-silicide-aluminum wiring; 80ns to 120ns; 4.76 x 11.63mm chip; 3.33 x 6.56-micron memory cell; 1Mbx1 structure; 1mA standby current consumption; 300-mil, 18-pin plastic DIP, 26-pin SOJ for surface mounting, and 20-pin VDIP; sampling for ¥12,000 ($80) for 80ns, ¥8,000 ($66.70) for 100ns, and ¥8,000 ($53.30) for 120ns versions
  - 4Mb DRAM technology transferred from central laboratory to divisional level; joint 16Mb DRAM work at central divisions; 64Mb DRAM (using string-search engine) research progressing at central lab
  - Two 4Mb CMOS mask ROMs (MuPD23C4000C/D); 0.9-micron rule; 62mm square chip; 4.2 million elements; storage of 4,000 32 x 32 Kanji characters

- A 256Mb Bloch-line memory; production in two to three years; 2.0-micron process; 20 x 60 micron chip; 14-bit memory storage

- An ECL RAM family (MuPB10400); 10K ECL logic-compatible devices including 256x4, 4Kx1, 1Kx4, 16Kx1, and 4Kx4; 100K ECL-compatible including 256x4, 4Kx1, 1Kx4, 16Kx1, and 4Kx1; CERDIP, ceramic flat package, and LCC; 4.5ns access time

- NEC/ASCII—A 256K frame buffer memory capable of drain and pixel access (MuPD42232CU); plans to add to dual-port memories; 8-bit data bus; 1-bit parallel access; x1/x2/x4/x8 serial port; 40/60ns cycle time; 470mW power consumption; 15.2mm-wide 40-pin shrink DIP sampling for ¥5,000 ($33.33); 220ns read-write cycle type for ¥4,000 ($26.66); 10.2mm SOJ planned; sales since July

• NTT

- Experimental production of 16Mb CMOS DRAM; 8.9 x 16.6mm chip; 40 million transistors and capacitors; 0.7-micron process; polysilicon gate; dual-layer aluminum wiring process; 1.5 x 3.5-micron memory cell; new self-alignment process; thin buried capacitor combining data storage and cell separation functions; 2Mbx8 structure; 80ns access time; 3.3V power source; 500mW power consumption; 180ns cycle time

- Early development of 64Mb DRAM; initial difficulties expected due to limits of silicon processing technology

- A 20K associative memory with AI functions for next-generation computers; associative processor on silicon substrate capable of directly identifying key data from memory storage; 5.3 7.9mm silicon substrate; 1.2-micron pattern; 287,000 transistors; CMOS process; 100ns data output time

• Oki Electric

- A 16K CMOS EEPROM (MSM28C16A); 150ns; floating-gate memory cells; 50mA to 110mA operating power consumption; 0.5mA to 40mA standby power; 10,000 rewrite cycles; 5V; 24-pin plastic DIP

- A 64K CMOS EEPROM (MSM28C64A); 8Kx8; 64K SRAM/64K EPROM-compatible; 32-word/page write-in; 120/150ns access time

- A 4Mb CMOS pseudo/virtual-SRAM; 512Kx8; DRAM refresh control circuit; SRAM pin-compatible; 60ns pseudo-SRAM and 95ns virtual-SRAM access times; 85ns and 120ns cycle times respectively; 1 microampere power consumption; wire bonding; 149.36-square-mm chip and 16.84-square-micron memory cell using 1-micron n-well process; 9.88-square-micron memory cell and 72.5-square-mm chip with 0.8-micron rule used for 4Mb DRAMs

- Seiko–Epson
  - A 256K CMOS SRAM series (SRM20256); TTL–compatible; 28–pin DIP (LC model); 28–pin shrink DIP (LS model); 28–pin MFP/SOP (LM model)
  - A CMOS NVRAM series; two 256K versions: S–2210R (64Kx4) and S–244R (16Kx16); a 1K (256x4) version (S–2212R)
- Sharp
  - A 4Mb CMOS mask ROM (LH534000); 524,288x8 and 262,144x16; 200ns; 15mA power consumption
  - A 64K bipolar PROM (LH5749J); 55/70ns; 8Kx8
  - A 64K CMOS OTP EPROM (LH5762J/LH5749J); 70/90ns
  - A 256K CMOS SRAM (LH522567); 32Kx8; 55/70/90/120/150ns access times; 70mA operating power consumption; 2mA at standby
  - Two 1Mb CMOS DRAMs; static column mode (LH64258) and page mode (LH64259); 100ns; 60mA power consumption; 2mA at standby
- Toshiba
  - A 25ns prototype 1Mb SRAM; NMOS structure and CMOS peripheral cells; 6.86 x 15.37mm chip; 6 million transistors; 0.8–micron process; 5.6 x 9.5–micron memory cell; dual–word wiring structure; automatic power–reducing circuitry; 32–pin DIP and flat packages; production in second half of 1988
  - A 250ns 4Mb CMOS ROM (TC534000P); 8.0 x 7.0mm chip; 1.0–micron process; miniaturized 32–pin DIP; standard JEDEC pin arrangement; 20mA current consumption during operation; 1 microampere at standby; sampling at ¥3,000 ($20.69)
  - A 1Mb DRAM for telephone voice memory (Kiss Phone FF–51MK); 120ns access time; sampling since July; 20–second response message; 10–second message board

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Microprocessors

- Fujitsu
  - A single-chip video signal DRAM controller (MB87045); one field of composite video signal; sampling at ¥800 ($6.95)
  - A CMOS 8-bit MCU (MB89733B); 8KB ROM, 260-byte RAM, 54 I/O ports, three timer channels, interrupt controller circuits, and sequential A/D converter; 64-pin shrink DIP; sampling for ¥1,200 ($8); piggyback version (MB89PV733B) with CMOS EPROM sampling for ¥30,000 ($200)
  - Two peripheral LSIs for Intel 8086/8088 MPUs; MB89393 featuring DMA controller, bus controller, interrupt controller, clock generator, and timer; MB89392 featuring DMA controller, two interrupt controllers, and timer; CMOS process; 100-pin, four-sided flat package; sampling at ¥2,000 ($13.79); 10,000 monthly
  - Two one-chip peripherals (MBL8086/8088) for Intel 8086/8088 and Zilog Z80; four designs of a DMA controller (MB893993 series); ¥2,000 ($13.33)
- Fujitsu/Hitachi
  - A 32-bit TRON MPU; 1.3-micron, 14-layer CMOS process; 650,000 to 700,000 transistors; on-chip cache memory; microprogram memory; 6 mips at 20 MHz; 4GB memory addressable; plans for 25-MHz device within a year; clock pulse generator (CPG), directory memory access controller (DMAC), interrupt request controller (IRC), and floating-point unit (FPU); refined instruction set with RISC speed and CISC complexity; UNIX and C language compatibility; easy expansion into 64-bit MPU
  - A hard disk controller (MB89341); ST506 interface; enhanced small disk interface (ESDI)
  - A small computer system interface (SCSI) protocol controller (MB89352); 2.6MB per second transmission speed; 8-byte FIFO; 24-bit counter; 16MB data transmission; DMA, program, and manual selection methods
- Fujitsu/Hitachi/Mitsubishi
  - Joint development plans for 32-bit TRON CMOS MPUs (G-Micro Series); 700,000-transistor 10-mips processor (32/200) by Hitachi; 900,000-element 20-mips processor (32/300) by Fujitsu; 300,000-element 10-mips processor (32/100) by Mitsubishi; low-end devices for PCs; medium-end for workstations; high-end for minicomputers; also joint MPR development; TRON architecture, UNIX operating system, and C language supported; sampling during first half of 1989

- Fujitsu/Intel
  - A jointly developed ASIC MCU with built-in 16-bit MPU (80186), 8251A peripheral LSI, 16-bit MPU (18677); compatible with external bus interface (80186); Intel production of CMOS types; OEM purchases by Fujitsu at 100,000 annually
  - A multi-function 16-bit MCU (MB89391); five functions including logic generator, bus controller, divide controller, DMA controller, and timer; 8 MHz
- Hitachi
  - A proprietary 16-bit MCU (HD641016 or H16); internal 32 bits; CPU with memory, interface, controller, and timer; real-time response; 2-mips device priced at ¥5,500 ($36.66) in quantities of 10,000 units; 3-mips device planned; 2-mips volume production of 30,000 to 50,000 units monthly from March 1988; 8-bit and 32-bit MPUs planned from early 1988
  - A small hard disk controller IC (HD153007/009); MFM method; 15Mb per second data transmission; SCSI/ESDI interface; sampling at ¥3,000 ($20)
  - An 8-bit CMOS MCU (HD647180X) with 16KB EPROM; built-in 512-byte RAM; sampling since June 1987; 16-bit programmable type; 54 I/O ports; 80-pin flat package; 4 MHz sampling at ¥3,500 ($23.33); 6 MHz at ¥3,850 ($25.66)
  - An 8-bit CMOS MCU (HD401304) with built-in 256-byte EEPROM, 3.5 KB ROM, 80-byte RAM, electronic tuning 14-bit D/A converter, sound and image controller 6-bit D/A converter, remote control receiver functions, and 26 input terminals
- Matsushita—A B-TRON operating system for personal computers; 80286 based; 2MB memory; MS-DOS; 150KB and 180KB operating systems
- Mitsubishi
  - A CMOS single-chip, 4-bit voltage synthesizing MPU (M50436SP); built-in ROM for generating characters on TV screen (3 rows by 16 characters); built-in remote control detection circuity and video signal detection counter; 5,120x8 ROM; 144x8 RAM; 4-MHz clock frequency; 103 basic instructions; five subroutine nesting levels; built-in clock generation circuitry; 1.5ms current consumption when display off, 4.0ms when on; sampling at ¥1,080 ($7.20); 50,000 monthly; for use in TVs, VCRs, and laser disk players

- Four MCUs with system reset circuits (M5290P/5292P); +5V and +/-12V power output; 4.2V current; priced at ¥140 ($.93)

- An 8-bit CMOS parallel processing MPU (M5M80C85AP-2/AFP-2); 2.0-micron rule; 12,000 transistors; 0.8ms instruction cycle; sampling at ¥550 to ¥600 ($3.67 to $4.00)

• NEC

- A high-end V70 CMOS 32-bit MPU (MuPD70632); 1.5-micron two-metal layer process; 14.35 x 14.24mm chip with 385,000 transistors; 32-bit address and data bus; 4GB address space; 6.6 mips peak performance; 40MB per second data transfer rates for multitasking, virtual memory processor, virtual memory management, IEEE-754 floating-point operations, emulation mode; fault tolerant; supports UNIX System V and ITRON (Industrial The Real-time Operating Nucleus); on-chip demand-paged MMU with 4GB virtual space per task; priced at ¥100,000 ($719.42) for 20-MHz version; 132-pin ceramic PGA; 20,000 monthly production from August 1987

- A V60 MPU; 24-bit address bus; 16-bit data bus; 16MB address space; 16 MHz; 3.5-mips processing speed; three clocks; 10.7MB bus transfer rate; 375,000 transistors; 13.92 x 13.80mm chip; 68-pin PGA; sampling since October 1986

- A V60 real-time operating system (RX616), an upgraded version of RX116 for V20 and V50 series; source program priced at ¥5 million ($33,333)

- Development of V80 MPU; 800,000 transistors; 10-mips processing capability; sampling in 1988

- Two CMOS 16-bit MPUs (MuPD70208/216); V40/V50; 68-pin PGA or LCC, 80-pin flat package

- A V25 16-bit CMOS single-chip MCU (MuPD70322); 256-byte RAM, 16KB ROM; two-channel DMA controller; serial interface; timer; 1.5-micron process; 0.4ms instruction cycle at 5 MHz; 84-pin PLCC

- A 16-bit CMOS MPU (MuPD77C25); twice graphics processing capability of MuPD7720; 2Kx24 instruction ROM; 1Kx16 data ROM; 256x16-word data ROM; 122ns instruction cycle; 28-pin DIP or 44-pin PLCC

- A CMOS 4-bit, single-chip MPU (MuPD75216A); 512x4 RAM; four counter/timer channels; fluorescent display driving circuitry; 1.91 and 1.53 microseconds at 4.19 MHz; 122 microseconds at 32.768 KHz; priced at ¥1,000 ($6.67) each for 100,000-unit orders; piggyback version (MuPD75CG216A) for ¥10,000 ($66.67); 200,000 chips monthly, doubling at end of 1987

- A CMOS 4-bit, single-chip MCU (MuPD75308) with built-in LCVD controller/driver; 0.95/1.91/15.3-microsecond at 4.19 MHz; 122ms at 32.768 KHz; 8Kx8 ROM; 512x4 RAM; 80-pin flat package

- An intelligent CRT display processor (MuPD72022); text, graphics, and facsimile display; dual-port RAM interface; 640x540 dots; 5V power; 80-pin flat package and 68-pin PLCC

- A 16-bit character string search processor; 1.6-micron CMOS process; 8.62 x 12.76mm chip; 217,600 transistors; 10 million characters per second

- A 4-bit, one-chip MCU (MuCOM-75X Series); 0.95/1.91/15.3 microseconds at 4.19 MHz; 122ms at 32.768 KHz; 4KB to 16KB program memory size; internal EPROM

- An 8- and 16-bit, one-chip MCU with real-time instruction control; 0.33ms instruction time; 8-bit CPU (MuCOM-78/I); 16-bit CPU (MuCOM-78K/II); three-type family (MuCOM-78K/III); 128-byte to 640-byte RAM, 8KB to 16KB ROM, serial interface, and A/D converter; 8-bit with PROM (MuPD78P112) sampling at ¥3,000 ($20)

- Nissan Motors/Intel--A joint-developed 16-bit MCU for engine controls; plans to use Intel 16-bit MCUs (8096) in 2000cc-class cars in two to three years; Japanese 16-bit MCUs to be used for future models

- Oki Electric—A static version CMOS 16-bit MPU; 5-MHz device 1SM80C86A/88A) priced at ¥2,000 ($14.39) each or ¥1,000 ($7.19) each in 10,000-unit lots; 8-MHz device (MSM80C86A-2/88A-2) priced at ¥2,500 ($17.99) and ¥1,300 ($9.35) respectively; sales of 70,000 to 100,000 monthly

- Sharp

  - Two single MCUs for TV channel selection; LR3790X (50x16 EEPROM, 4Kx9 PROM, 128x4 RAM) sampling for ¥1,700 ($12.14); LR3772X (20x16 EEPROM, 1.8Kx8 ROM, 32x4 RAM) for ¥870 ($6.20); monthly production of 100,000 units each targeted

  - An 8-bit CMOS MCU (SM805); Z8 type; 8K ROM; 15mA power consumption during operation; 8-bit x 4-port output

- Sony--An 8-bit MCU with VTR controller circuit (CXP80116); 16KB ROM; 352-byte RAM; 8-byte FIFO; 500ns instruction time; ¥1,500 ($10); 80-pin flat package

- Tohoku University/Matsushita--A jointly developed, multiple-value logic multiplier LSI; quaternary algorithm computing system; multiple-valued MOS current-mode circuitry; 32x32 multiplier with 24,000 transistors designed using PMOS/CMOS process

- Toshiba

  - Development of TRON 32-bit MPU (TX3) with 8-mips to 10-mips processing capability; sampling in 1988; memory processing unit and cache memory; core processor; internal interface; four-level pipeline; 4 mips to 5 mips at 8 MHz; CMOS process; 200,000 to 300,000 transistors; G-Micro family interface undetermined

  - An 8-bit CMOS MCU (TLCS-90); 0.4-microsecond instruction time at 10 MHz; 256-byte RAM; six-channel 8-bit A/D; one-channel serial interface; 16-bit timer/counter; four 8-bit timers; two-channel stepping motor controller ports; 1MB memory space for DMA functions; 163 basic instructions; 25mA power consumption

Digital Signal Processors (DSPs)

Voice recognition/synthesis technology is attracting intense interest among Japanese companies because of its application to personal computers, telephones, word processors, work stations, and auto electronics. Table 6 lists major Japanese voice recognition systems.

- Citizen Watch—A voice recognition watch employing a CMOS custom LSI, 16K RAM, and three MCUs; 32.768-KHz logic wavelength; more than 80 percent word recognition; priced at ¥10,000 ($66.67)

- Hitachi—A 50ns DSP LSI for general-purpose, multifunction capability; image shrinkage and expansion for use in facsimiles and image recognition by industrial robots; 1Kx48 program RAM; 1.3-micron CMOS process; dual-layer metal; 12.9 x 11.5mm chip; 420,000 elements

- Matsushita—An ultrahigh-speed image processor (RISP-II); 15ns command execution time at 70 MHz; 6.0 x 6.0mm chip; 24,000 elements; proprietary bipolar technology (VIST); 10 times faster than MOS-type image processors; for real-time processing in production line monitoring robots and pattern recognition in medical electronic systems; sampling at ¥250,000 ($1,786)

  - A sample DSP LSI (MN8601); 47 microinstructions; 20 control instructions; 2K built-in ROM; two 256-word data RAMs; 100ns machine cycle; 16-bit parallel interface; 2-micron CMOS; 100mW power consumption; 64-pin shrink DIP; sampling at ¥5,000 ($33.33)

Table 6

Major Japanese Voice Recognition Systems

Company	Activity
ATR	Automated translation phone research lab developing voice and pattern recognition DSP technology for translation phones; 100 simple words with 92.8 percent recognition in experiment with three female speakers
Citizen Watch	Voice recognition watch*
MITI/ETL	Simple voice recognition equipment; 220 words with 97.7 percent accuracy; 2,354 standard sound patterns
NEC	SR-150 Series (35 continuous words, 240 distinct words) DP-3000 (150 simple words/characters, 250 distinct words) SR-2000 Series (phone voice recognition/response system; 16 to 20 simple words) Voice recognition LSI (MuPD7764, MuPD7763) chip set
NTT	ANSER (Voice recognition/response system; 16 simple words); a 16-element parallel processing voice special extraction processor capable of identifying continuous speech of various people**
Ricoh	RV100 (120 simple distinct words, ¥450,000/$3000)
Sharp	Voice recognition word processor (4 sounds per second)
Toshiba	Speaker-independent 3-chip voice recognition system (95 percent accuracy using analog signal processor, DSP, and system control LSI; 13-word recognition; ¥10,000/$66) Voice recognition chip; 50 words; 95 percent accuracy**

*See text on page 23
**See text on page 25

Source: Dataquest
November 1987

- NEC
  - A 256K triple-port graphics buffer (MuPD42232CU); 32Kx8 MOS dynamic memory cells and 128Kx8 data register; 256 types of logic operation circuits; 120ns/40ns models sampling for ¥5,000 ($35.97); 150ns/60ns models for ¥4,000 ($28.78); monthly production of 300,000 by late 1987
  - A 16-bit CMOS signal processor (MuPD77C25) for NC machine tools, CT image processors, industrial robots, and modems; 1.6-micron process; pin- and software-compatible with MuPD7720; 122ns per operation; built-in RAM and ROM; 2Kx24 ROM; 1Kx16 data ROM; 256x16 data RAM; 31-bit fixed floating-point multiplier, 16-bit fixed floating-point ALU; two 16-bit accumulators; 8-bit parallel bus host CPU interface; one-channel I/O serial interface (4 MHz); 5V; 40mA power consumption at 16 MHz; 28-pin DIP and 44-pin PLCC; priced at ¥5,000 ($34.48) for 10,000-unit orders; 100,000 monthly
  - Two color TV signal processors (MuPC1800CA/1810CA); sampling at ¥500 ($3.50) each for 10,000-unit lots; monthly production of 300,000 units by March 1988
- NTT
  - A 16-element parallel processing voice special extraction processor capable of recognizing continuous speech of various people; DSP (TMS32010) and PE (processing element) array structure; vector processing; DSP-based scalar processing; one-dimensional processing element; 42-bit length microinstructions (32-bit PE and 10-bit buffer); 67 mips
  - A 20-MHz+ complex signal processor LSI; 1/2, 3/4/, 7/8 signaling rates; 5.0/4.3/3.4dB noise; 45,000 gates; 164 pins (208-pin PGA) and 234 pins (280-pin PGA); CMOS process; 60-step pass memory LSI (NUFEC TYPE 2)
- Sharp—Rotating head DAT LSIs; 48.0/44.1/32.0 KHz; 16-bit processing; three data conversion, subcode data processing, error correction, 64K external RAM (LR38111/2/3); automatic track-finding DSP (LR38114); drum motor capstone motor DSP (LR3R37); one set priced at ¥100,000 ($666)
- Toshiba—A speech recognition LSI capable of recognizing 50 words; 95 percent accuracy; key 13-word vocabulary; priced at ¥10,000 ($66.67); multiple similarity method previously used in optical character readers and mail-sorting machines

Graphic Display Driver ICs

Dataquest observes a sharp increase in Japanese makers offering low-cost graphic display driver ICs for plasma display panels (PDPs), vacuum fluorescent displays (VFDs), and electroluminescence (EL). Besides Siliconix, Sprague Electric, Supertex, and Texas Instruments, the following Japanese companies have introduced sample chips:

- Asahi Microsystems—A vacuum fluorescent display driver IC (S4543); 60V output current; 25mA operating power consumption; npnx1 and NMOSx1 "totem pole" output circuitry; 40-bitx1; BIMOS process; 64-pin quad flat package

- Fuji Bank/Oki Electric/Toyo—A cash card with 2KB of EEPROM and 7KB program mask ROM; solar power battery; 12-character display; 24-key pad; November 1987 field testing

- Fujitsu

  - A VFD driver IC (FD3205F); 230V output current; 1mA operating power consumption; NMOS and PMOS totem pole output circuits; 32-bitx1; MOS process; 44-pin quad flat package

  - A television display controller (MB88321/322); 8x8 dot matrix; timing control circuit; display memory; character generator; logic generator

- Hitachi—A VFD driver (HA16721MP); 150V maximum current output; 32 output circuits; 1 MHz; 32-bitx1 shift register; BICMOS process; 44-pin minisquare package

- Matsushita Electric/Tohoku University—A 32x32-bit graphics chip; 59ns processing time; 2-micron process; 7.16 x 4.92mm chip; two CMOS graphics circuits, PMOS and NMOS circuits; 23,600 transistors

- NEC

  - A plasma display driver IC (MuPD6337); 200V current output; 300mA operating power consumption; NMOS open drain; 32-bitx1; BIMOS process; 52-pin quad flat package

  - An intelligent display processor (MuPD72022) for text, graphics, and moving display data processing; DRAM refresh; dual-port RAM interface; 640 x 512-dot resolution; CMOS process; 5V; 80-pin flat or 68-PLCC packages

  - 12 on-screen character display LSIs (MuPD61400 Series); CMOS; 4.0 MHz to 7.0 MHz; 5 x 7 dot or 6 x 9 dot; 16-pin DIP or miniflat packages; 18-pin DIP or 20-pin miniflat package for two largest devices

- Oki Electric—A plasma display panel driver IC (MSC1123GS); 60V current output; 220mA operating power consumption; npnx1 open corrector; 32-bitx1; BIMOS process; 60-pin dual flat package

- Seiko Epson—A VFD driver IC (SED2032F); 70V current output; 10mA operating power consumption; NMOS and PMOS totem pole output circuits; 16-bitx2; MOS process; 60-pin quad flat package

- Sharp—A driver IC (LZ1132AM) for EL and plasma display panels; 500V maximum output current; 20mA power consumption during operation; 32 output circuits; open drain PMOS; 4 MHz; 32-bitx1 shift register; 44-pin quad flat package

- Toshiba—A driver IC (TD62C932F) for EL, plasma, and VFD panels; 250V maximum output current; 40mA operating power consumption; two totem-pole NMOS output circuits; 7-MHz clock frequency; 32-bitx1; 44-pin quad flat package

- Yamaha—An MSX personal computer CRT controller (V9938); CAPTAIN videotex processing capability when combined with character transmission display function CRT controller (V99C37) by ASCII Inc.; 400mW power consumption; 100-pin, 4-sided flat package; 84-pin PLCC being studied; sampling since July at ¥10,000 ($66.67)

IC Cards

In early April, 1987 the Electronics Industry Association of Japan (EIAJ) issued a report ("The Impact of IC Cards on the Electronics Industry") forecasting that the Japanese IC card market, which was ¥1.4 billion ($9.3 million) in fiscal 1985, would reach ¥277 billion ($26.4 billion) in fiscal 1995. The overall IC card market, including reader systems, would reach ¥3.977 trillion ($28.4 billion) in fiscal 1995, of which cards would account for only 13 percent. The following are major announcements made during the second quarter of 1987:

- Apex—An IC card management system for coffee percolator sales networks (APEX 500 SUPER BREWER)

- Arimura Giken—An ISO-compatible IC card priced at ¥2,000 ($13.30); Hitachi 16K EEPROM and U.S. 4K EEPROM used; jointly manufacturing and selling with Citizen Watch

- Casio—A world clock IC card (CC120U); ¥3,900 ($26)

- Casio/NTT—A ticket reservation card; 54.0 x 86.0 x 1.8mm; 16-character display; 4-key pad; 8KB SRAM; 4KB program mask ROM; built-in battery; April through September 1986 testing

- Casio/Sumitomo Bank—A company bank card; 54 x 100 x 10mm; 16-character display; 8KB SRAM; 4KB to 6KB program mask ROM; lithium battery; July 1987 testing; November 1987 use

- East Japan Railway Co.—A computerized credit card network using smart cards; plans for a large demonstration involving Japan Railway (JR) riders by late fiscal 1988, allowing cashless purchases of train tickets and payments at JR-group hotels, restaurants, and shops; plans for joint venture with banks and postal authority to build a network of "smart" teller machines in 3,000 stations

- Gakushu Research—An CAI (computer-aided instruction) academic record management system using IC cards; 8KB storage for one student's records for two years

- Iwatani Industries—A numerical-control transmission/storage machine using IC cards (RS-232-C); ISO format; 150/600/4800 bits per second; 256 x 128-dot LCD display panel; 1.8mm-thick 64K EEPROM; type IC card types; ¥17,000 ($113) for programmable card; ¥12,000 ($80) for data card; ¥335,000 ($2,233) for two 40m cards and three 20m cards

- Japan Aviation Electronics Industries—An IC memory card connector (JC20 Series) for office and factory automation

- Japan Electronic Publishing—A 25,000-word Japanese dictionary IC card; 1Mb and 4Mb ROMs; ¥7,000 ($46.70); reader priced at ¥34,800 ($232); 86 x 54 x 3mm card; sales also through Sanyo Electric; plans for laser card and CD-ROM for expanded dictionaries; a joint venture of Japan Coinco, Sanyo Electric, and Toyo Information Systems

- Japan LSI Card—An LSI card reader (C-1600FH) for hand-held computers (HC-40V); ¥98,000 ($653) for reader and 32KB LSI card; ¥198,000 ($1,320) for hand-held computer; ¥75,800 ($505) for cartridge, 8KB card, and BIOS ROM

- Kobe Electric—An automated robot car system (AVH0-5) with an IC card containing factory floor plan to determine shortest routes; supersonic wave sensors

- Mitsubishi Electric—A 512KB memory card for personal computers and POS systems, a 1.2mm-thick 256K SRAM (MF3512-MIEAP01) priced at ¥3,000 to ¥3,500 ($20 to $23), and a high-capacity memory card (MF4512-NIFAP01) with built-in OTP ROM priced at ¥53,000 ($353)

- Mitsubishi Resin—IC card production from fall 1987; 500,000 cards monthly; also connectors and card reader production

- NTT
  - Testing multiple-purpose IC cards in seven banks and three department stores since June; IC card display featuring prepaid money amounts, credit status, medical and health information, bank settlement status for point of sales, and personal identification number; testing by 1,000 NTT employees over the next three years; participants include Sumitomo Bank, Mitsui Bank, Taiyo-Kobe Bank, Kyowa Bank, Bank of Yokohama, and Odakyu, Seibu, and Takashimaya department stores
  - An IC card specialty company in Hiroshima (Chugoku Communication Network, or C-NET) to develop an IC card system network for the financial, distribution, information, and manufacturing industries
- Oki Electric/Fuji Bank—A multipurpose IC bank card featuring a small keyboard and built-in LCD to show bank balances and transactions; for use as cash card and credit card; experimental system in Tokyo from October; regular use from March 1991; 54.00 x 86.00 x 0.76mm card; 8-bit MCU, 7KB ROM, 240-byte RAM, 2KB EEPROM, and LCD driver; 5V power supply
- Ricoh—An electronic note pad (CUVAX-MJ550) featuring a 12mm-thick A4-size pad with keyboard; internal 16-bit MPU; 16KB IC memory data card (5,800 characters); ¥5,800 ($38.67)
- Sanwa Bank/NTT—Distribution of multifunction IC cards to Tokyo and Osaka on an experimental basis from October; three user groups including exclusive Sanwa Bank use, optional use by the bank, and use by nonbank members; JCB, Nippon Shinpan, Daishinpan, Takashimaya, and Hankyu Department Store to produce common IC credit card function; Hitachi and NTT Musashino Lab to jointly develop automatic IC card call facility for storing 50 phone numbers
- Seiko—A world time IC Card; ¥3,500 ($23.33); 24 cities; alarm; daylight saving time
- Tateishi Electric—A home blood pressure measuring system using IC memory cards (Blood Pressure Monitoring System); ¥39,800 ($265); ¥300,000 ($2,000) for personal computer software
- Thanks—A memory card system (IDX Series) for robot cars, component shipment palettes, automated inventory, and other factory automation systems; optical space transmission method
- Token Instruments—A noncontact memory module system (TOKEN) using IC cards for numerical control (NC) factory data
- Tokyo Heavy Machinery—A machine control IC card for apparel production systems (Quick Response Sewing System)

- Toshiba/Visa International—A supercard credit card; 0.54 x 0.86 x 0.76mm card; 16-character display; 20-key pad; 8KB data storage; 16KB program mask ROM; 1988 field testing; 1989 production

- Trio Electronics—A credit card-size voice recorder-playback card (Voice Card) that records up to 32 seconds of music or voice message; 4.8mm thick; for use in Christmas, birthday, and other greeting cards, home and office voice bulletin boards, talking books, and other educational materials; plans to sell 200,000 voice cards in 1987; priced at ¥6,500 ($44.83) from August

- Tsugami—A numerical control (NC) program IC card for a factory automation personal computer terminal (Tsugami NC Mate PSONC Terminal); system price of ¥150,000 ($1,000); also being developed by Hitachi Seiki and Miyano

Application-Specific ICs (ASICs)

- Fujitsu

  - Four mixed ECL/TTL 5ns gate arrays (ETM series); MB183000 (4.5K, 3,000 gates, 10 KHz level); MB193000 (4.5K, 3,000 gates, 100 KHz level); MB182000 (9K, 2,000 gates, 10 KHz level); MB192000 (9K, 2,000 gates, 100 KHz level); nonrecurring cost of ¥5 million ($35,970); models priced at ¥45,000 ($324) to ¥50,000 ($360)

- A BICMOS gate array series (MB210000) combining two bipolar transistors and six CMOS transistors on a single chip; 0.8ns gate delay time; 0.25mW internal gate power consumption; 10 MHz operation; three-input NAND gate for TTL gate array transfer; 430-gate/52-pin, 812/72-pin, 1248/96-pin, and 2160/112-pin devices

  - A very high-speed low-power CMOS gate array (MB680000/AV series); 350/540/850/1,200/1,600/2;000 gates; standard cell package interface; CAD support system; 16- to 100-pin DIP, SH-DIP, SOP, QFP, PGA, LCC, PLCC packages

  - New CMOS gate array series; 11-model UHB series and 6-model AVL series; 0.9ns gate delay time achieved by using two CMOS aluminum layers of 1.5 microns; pin/gate ratio up 40 percent; 330 gates/60 I/O pins to 12,700 gates/220 I/O pins; UHB unit price of ¥700 ($4.67) in 10,000-unit lots; ¥1.8 million ($12,000) development cost; 21-day turnaround; AVL series featuring 1.8-micron thickness for both aluminum layers; priced at ¥500 ($3.33) in 10,000-unit lots

  - An ECL gate array with 9.0K built-in RAM and 1,920 logic gates (ET2009M); an array with 4.5K RAM and 2,880 gates (ET3004M); 220ps internal gate speed; 5ns RAM address access; 5-week logic simulation time; ¥5 million ($33,333) development cost; ¥50,000 ($333) for 500 ET2009M devices; ¥45,000 ($300) for 500 ET3004M devices

- An 8,000-gate CMOS array for 8Mb per second ISDN transmission equipment (Fetex 150)

- A 4,096-gate HEMT gate array for supercomputers; 128x32 array; 0.8-micron process; 4.8 x 6.3mm chip; 17,692 elements

- Hitachi

  - Seven CMOS gate arrays (HG62E Series); 4,309/5,821/7,488/10,760/13,015/18,176 gates; 1.0-micron process; 0.7ns gate delay; 0.55ns for power gate; LOGICIAN and IDEA; I/O pins increased to 4,300 gates/96 pins, 24,000 gates/240 pins; pricing between ¥2,900 ($20.86) for 4,000-gate model and ¥99,000 ($712.23) for 24,000-gate model in 10,000-unit lots

  - A 7,000-gate array with built-in BICMOS 4.6K SRAM; 0.45ns gate delay; 10ns SRAM access time; TTL-compatible; 5V; memory structure of 512x9, 256x18, 128x36

  - An LSI CAD software program (HICE) for converting mask patterns into netlists; S-810 supercomputer used to develop 10,000-transistor MOS memory in 9 hours and simulation in 11 hours

- Matsushita—Two CMOS gate array series; MN53000 featuring 3/15/500/732/1,008/1,547/2,014/3,144/4,104/6,016/8,018/10K/15K/20,064 gates in DIP, SDIP, QFP, SO, and ceramic PGA packages with 16 to 224 pins; MN73000 featuring 50,000 gates, 1.4ns, 5V, 182 basic RAM, ROM, PLA cells, CMOS and TTL compatibility, 8 to 148 pin DIP, SDIP, SO, QFP packages

- Mitsubishi—Two 1.3-micron rule CMOS gate array versions; M6002X featuring alternating internal gate and wiring; 224 to 1,773 gates; M6003X featuring 4,778 to 47,376 gates; VTM system (basic cells laid over all internal gates, enlarging built-in ROM and RAM capacity); gate isolation system; 1.1ns per gate; DIP, shoe-link DIP, QFP, PLCC, and PGA packages

- Sanyo—A 2.3MB per second CD-ROM error correction LSI (LC8950) designed using standard cell method, featuring DSP, controller CPU, and buffer RAM functions; 5V; CMOS process; 9,000 gates; 8.00 x 8.24mm chip; 300mW power consumption during operation; 80-pin quad flat package; sampling at ¥5,000 ($33.33); 200,000 monthly production by late 1988

- Seiko-Epson

  - Two CMOS gate array series; SLA600L featuring 2.0-micron process, eight sizes up to 6,000 gates; 4ns gate delay at 3V; SLA700A featuring 1.5-micron, dual-layer aluminum wiring process, 600 to 1,600 gates, and 1.4ns gate delay; SLA6000 series usable in SLA600L circuit development; for use in portable electronic office machinery, test and measurement instruments, and portable consumer products; plans for third CMOS array series

- Two CMOS logic cell arrays; 1,200 gates (SLC2064J Series); 1,800 gates (SLC2018J Series); 33/50/70-MHz speed cycle time

- Sharp

  - A CMOS standard cell series for high-definition TVs; replacement for 5,000 ECL ICs; 1.2-micron process; low resistance tungsten silicide gates; dual-layer wiring; 0.58ns internal gate delay (versus 0.7ns for ECL chips); 69 models available, including 36 basic cells and 13 functional cells

  - A standard cell CAD program (CERES); cell selected after function and delay time input; length-width (L/W) transistor dimensions; cell revisions possible by changing transistor dimensions; compaction control; master pattern by automatic layout

- Toshiba—A 50,000-gate CMOS array (TC110GC9); 50,000 usable gates of 129,000-gate device; for mainframe computers; jointly developed with LSI Logic's LDS System CAD

- Yamaha—A standard cell library with RAM ROM, analog circuits; YIS-Logic CAD System; personal CAD timing simulation and auto layout program

CAD Systems

- Fujitsu Facom

  - A prototype VLSI expert system to design linear/analog ICs (Fujitsu FIP); development to be completed by end of fiscal 1987 jointly with Nippondenso, an electronics parts affiliate of Toyota Motors; plans to use system to design ICs for car engine controls, windshield wipers, and other systems

  - A logic simulation CAD hardware accelerator for designing up to 4 million gates; 32MB memory; event-driven method logic simulation; 5.3GB per second logic processing speed; 64 basic processors in M-380

- Kyocera—LSI mask pattern design CAD system (CAECO LAYOUT) for transistor layout; one-third to one-sixth the size of existing polygon layout software; 30 percent to 60 percent reduction in data file; GDS-II format; runs on Sun and Apollo workstations; priced at ¥3.9 million to ¥22.0 million ($26,000 to $146,670) in Japan; sales by CAECO, Inc. in the United States

- Mitsubishi—A gate array development expert system (GATEPLEX); yes/no interactive instructions to input number of gates and I/O, input power current, and package; CMOS M60000 Series currently employed; for mainframe computers and TSS terminals

- NEC
  - Three CAD interface methods; circuit diagram interface (74 TTL and NEC logic); electronic work station interface (VISTASL, LOGICIAN, IDEA System, SCALD System, DASH); CAD interface (NEC CAD, TEGAS, HILO, user simulation)
  - A development tool (NV-200) for personal computers (PC-9801) for voice synthesis LSIs (MuPD7755 Series); conversion from analog A/D voice to PROM data
  - Gate array design CAD system offered on NEC's C&C VAN network; logic simulation through design rule checking; inquiries through electronic mail; menu for training services
  - A hard macrocell/standard cell CAD tool; RAM, ROM, and PLA building blocks; program pattern (logic code), aluminum wiring pattern, and master pattern (GDS-II) functions
- Toshiba—A five-year technological agreement with SDA Systems Corp. of the United States to jointly develop CAD software combining Toshiba's semiconductor design technology and SDA's software know-how; Toshiba plans to strengthen VL-CAD using this software, and jointly market CAD software products

Optoelectronics

- Copal Electronics/NHK—An optoisolator using bismuth substitute gadolinium, iron, and garnet; 5mm thickness; bismuth oxide melted and stirred using flux method; for 1.5mm beam diameter and 0.78-1.55-micron band wavelength
- Hitachi
  - A multiquantum well (MQW) semiconductor laser with multilayered oscillation and barrier layers; 30-GHz resonance frequency; undoped GaAs quantum well resonance layer and beryllium-doped GaAlAs barrier layer; two 100A-thick layers formed by molecular beam epitaxy (MBE)
  - A MOS image pickup device (HE98246); 1/60 and 1/15, 750-second shutter speed; sweep-out scanning function; 644 x 491-pixel resolution; 480 TV lines; sampling at ¥25,000 ($167)
  - Laser diodes for CD players, videodisk players, and car stereos (HL7831HG/7832HG); 5.6mm-diameter package; low astigmatism and noise; metallorganic chemical vapor deposition (MOCVD) method; HL7831HG sampling for ¥2,000 ($13.33) or ¥1,600 ($10.67) in lots of 10,000; HL7832HG sampling for ¥2,500 ($16.67) and ¥2,000 ($13.33) respectively

- KDD—Three 1.57–1.58–micron direct–feedback (DFB) semiconductor lasers; two 1.47–micron lasers with 60km optical fiber transmission capability; 0.39 dB/km loss for 1.47–micron lasers; 0.32 dB/km loss for 1.57–micron lasers

- Matsushita

  - A 830nm semiconductor laser; 30/40mW output; captive sampling underway

  - A blue LED featuring low–resistance chlorine oxide; for TV tubes

- Mitsubishi—A GaAsAl/GaAs distributed reflection semiconductor laser for surface light emission; test–manufactured laser with ridge waveguide structure using multiquantum well for active/inactive waveguide path; MBE growth process; 4mW light output; 42mA threshold current during continuous oscillation at 15 degrees Celsius; for future optocomputers

- NEC

  - A 683nm GaInAlP visible light semiconductor laser; 27mW output power; performance equal to helium–neon gas laser; a selective buried mesa structure for sealing light and electrical current in the stripe section; for optical disk systems; plans to commercialize in two years

  - World's first GaAs–on–InP heteromaterial technology for long wavelength OEICs; InP optical device for optical communications integrated with GaAs IC for electronic circuits; 1.3– to 1.55–micron wavelength; molecular ray epitaxial growth technology to growth GaAs crystal on InAs substrate; heteromaterial process technology to develop InP optical device and GaAs IC (MESFET) on single substrate; tested OEIC integrating an InGaAs PIN photodiode, metal semiconductor FET, and load resistor; 3.66GB per second light detection speed

  - A 5.8nm+ continuous wavelength tuning of 1.5–micron wavelength tunable distributed Bragg reflector (DBR) semiconductor laser

- Sanyo—A triple–beam output monolithic laser diode; liquid phase epitaxial (LPE) thin–film single crystal growth method to form GaAlAs thin–film layers on high–purity GaAs substrates; three built–in photodiodes permitting instantaneous voltage adjustment; 830nm oscillation frequency; 20mA output power level; 5mA replay use beam power; 70mA operating current; 200–microampere monitor current; sampling for ¥200,000 ($1,333); for use in erasable optical disks and players

- Sharp—A GaAsAl quantum well semiconductor laser grown on GaAs substrate using MBE method; 145A/square cm threshold current density; 45A–wide quantum well; 490–micron long resonator; 150–micron stripe width; 817nm wavelength; 720 degree Celsius growth temperature; 111 direction surface on crystal

- Sony—Eight 1W semiconductor laser diodes (SLD304V Series); 6W power consumption; MOCVD process capable of forming 70nm layers (versus 1,000nm for liquid phase epitaxy); broad area structure; 100/200/500mW and 1W; 770nm to 840nm range; sampling at ¥300,000 ($2,000) for 100mW models to ¥2 million ($13,300) for 1,000mW models; for use in industrial production equipment, medical devices, and communications equipment

- Toshiba

  - A DFB laser diode (TOLD-312S); 0.1nm spectral width; 1,310nm wavelength; single-mode optical fiber pigtail; 1mW power output; InGaAsP/InP buried hetero-structure for high bit-rate emission; 0.2mW output power version (TOLD-320) priced at ¥56,000 ($400)

  - A power MOSFET driver photocoupler (TLP590/591); sampling since June; 6V output; 6-pin DIP; priced at ¥250 ($1.67)

  - A 650nm to 680nm wavelength semiconductor laser; 105mW pulse operating output; 0.04-micron thick AlGaInP and GaInP layers; MOCVD method

- Toyohashi University—An OEIC prototype; 5.0 x 0.1mm chip; niobium oxide lithium substrate; SAW device and optical guidewave

Image Sensors

- Matsushita—An image sensor using a thrystor shift register; 8 images/mm; 93 x 54mm chip; 5-MHz frequency; 5V power; 20mA power consumption during operation

- Sony

  - A 2/3-inch color CCD image sensor with 380,000 elements; CMOS 1.0-micron rule; interline method; 1/60 to 1/10,000-second shutter speed; ICX022AK for NTSC color cameras sampling at ¥62,000 ($446); CCD image pick-up block (IUO22AK) for ¥70,000 ($504); seven CCD camera peripheral ICs for ¥500 to ¥2,500 ($3.60 to $18.00)

  - A 1.1kg, 8mm video camera using 380,000-element CCD and analog LSI in a 0.5-mm pitch very small quad flat package (VQFP); 90 x 130 x 330 camera; 1.6 x 0.8mm chip

- Toshiba—A 2/3-inch CCD color imaging sensor for televisions and cameras; 380,000 pixels (490 x 768); interline method; 6.6 x 8.8mm chip; 450-line horizontal TV resolution; 13.3 x 11.4-micron image area; 24-pin shrink DIP; sampling at ¥50,000 ($333)

Gallium Arsenide

- Environmental Agency—Development of environmental policy measures for GaAs production; Japanese 1986 GaAs production less than ¥17 billion ($113.3 million), or less than 10 percent of silicon production; 32 GaAs plants nationwide; domestic GaAs consumption of about 4 tons annually; reported issued in late March

- Fujitsu—An experimental 4,000-gate HEMT gate array; 4.1ns multiplication time at room temperature in a 16-bit multiplier; 128 gates x 32 rows and 156 I/O cells; three enhancement-type and one depletion-type HEMT; three input E/D type DCFL NOR circuits; 125 x 100 micron cell; 4.8 x 6.3mm chip; 15 interconnects between each row gate

- Matsushita

  - A GaAlAs semiconductor laser; 50mW output; 780nm zone; 1.5x to 2.0x information density; six layers, including 3-micron n-GaAs contact layer, 7-micron n-GaAlAs cladding layer, 0.04-micron p-GaAlAs active layer; 0.2-micron p-GaAlAs cladding layer; 2.5-micron n-GaAs block layer; 30-micron p-GaAs substrate; sales from early 1988

  - A GaAs monolithic Hall IC; -50 to +150 degrees Celsius; one analog magnetic sensor and two digital magnetic sensors for car electronics; read relay or magnetic resistance devices; analog output (OH450); digital output (OH750); uni-directional output (OH751); sampling at ¥500 ($.33)

- Mitsubishi—A high-output GaAs amplifier IC; 2.45W output at 28-GHz band; for use in ground station amplifiers for satellite communications systems; proprietary source island via hole (SIV) structure for GaAs FET structure; monolithic power distribution synthesis circuitry 70-micron thick gold plate heat sink

- NEC

  - Five 2-GHz GaAs logic ICs; ECL-compatible; four-stage ripple counter (MuPG703B) sampling for ¥40,000 ($287.77); 4:1 multiplexer (MuPG706B) for ¥54,000 ($388.49); 1:4 demultiplexer (MuPG705B) for ¥54,000 ($388.49); D-type flip-flop (MuPG706B) for ¥38,000 ($273.38) and laser diode driver (MuPG707B) for ¥38,000

  - Three microwave GaAs/AlGaAs heterojunction FETs (2SK887/2SK887-1.4/2SK984); 12 GHz; ceramic strip line package

- Sharp—Sample GaAs FETs for 1-GHz UHF zone for cellular phones, communication equipment, and measuring equipment; sampling of SHF zone GaAs FETs for satellite broadcasting expected in March 1988

- Sony
  - Three sample HEMT devices for consumer products; MOCVD process initially developed for laser diodes; 16-GHz frequency; 1.3dB model priced at ¥10,000 ($66.70); 1.5dB at ¥8,000 ($53.30); 1.8dB at ¥6,000 ($40)
  - 12 HEMT devices for telecommunications (2SK676/676H5/677/677H5 Series); 1.0db to 1.4dB maximum noise; n-AlGaAs/GaAs heterostructure grown using MOCVD
- Sumitomo Electric—Mass production of 3-inch GaAs epitaxial wafers; 4-micron deep GaAs epitaxial layer onto GaAs substrate using vapor phase epitaxial growth
- Sumitomo Metal—Development of new process to recycle GaAs scrap material; production since July; 99.99999 percent pure gallium achievable; monthly production goal of 300kg

Josephson Junctions

- NEC—Josephson effect verified at 85K (-188 degrees Celsius) using superconductive barium, yttrium, copper, and oxygen; 1 x 1 x 10mm polycrystal sintered body with 90K critical temperature and critical temperature density of 120A/square cm

Superconductivity

- Asahi Glass—Formation of a special team of 20 researchers to develop superconductive materials and films, especially ceramic compounds for wire rods; nonceramic superconductor work since 1984; researchers shifted from electronics and ceramics sections
- Fujitsu—A yttrium-barium-copper oxide interconnect on aluminum substrate; 159K zero resistance
- Hitachi
  - A prototype optical switch using superconducting material; an amorphous thin film of yttrium-barium-copper oxide formed over magnesium oxide substrate using sputtering process; film baked for two hours in 900- to 950-degree Celsius oxygen environment; superconductivity at 93K and critical temperature at 85K; 3,000A current density at liquid nitrogen temperature; 2-micron thin film with grooves 1.5-microns deep and 5 to 10 microns wide; switching by radiating 0.7- to 0.9-micron wavelength light onto device; 3ps to 5ps switching speed; plans for commercialization in the 1990s

- A SQUID featuring one or two Josephson junctions and an electrode pair connected to a ring; thin-film process; 6,000A per square cm; for use in magnetic resonance image (MRI) sensors in nuclear magnetic resonance (NMR) equipment
- A niobium superconductive coil; 17.2 tesla magnetic output at 4.2K
- A photosensitive superconducting device featuring two thin-film electrodes separated by a superconductive-filled trench; light exposure of trench restricts free flow of excited electrons

- High-Purity Chemistry Laboratory—A yttrium-barium-copper oxide superconductive material with zero resistance at 90K; 25 grams for ¥5,000 to ¥15,000 ($33.33 to $100.00)
- Institute of Chemistry and Physics/Osaka University—A superconductive thin film with zero resistance at 190K
- Kawasaki Steel—A ceramic superconductive material with 410A current density per square cm; yttrium, barium, copper, and other materials; resistance disappears at -178 degrees Celsius; zero resistance at -180 degrees Celsius
- Mitsubishi Electric—A barium-yttrium-copper oxide superconductor; 112A/cm square density at liquid nitrogen temperature; Meissner effect; critical onset temperature 103K; 95K offset temperature
- Mitsubishi Metal
  - Sample shipments of superconductive ceramic-based sputtering targets that enable researchers to form superconductive thin films on surfaces of electronic substrates; superconductivity at -196 degrees Celsius; two types of sputtering targets, including yttrium-barium-copper oxide (superconductivity at 183 degrees C) and lanthanum-strontium-copper-oxide (240 degrees C); 12-inch diameter disk and 5 x 15-inch rectangle backcoated with copper panel; priced at ¥200,000 to ¥300,000 ($1,333 to $1,500)
  - A superconductive ceramic material of barium, yttrium, and copper; 95K (-178 degrees Celsius) critical temperature; 40 x 1mm disk weighing 8 grams; 112A current passed via four terminals
- MITI/ETL—A yttrium-barium-copper oxide superconductive material with zero resistance at 64 degrees Celsius (337K); Meissner effect verified
- MITI/STA—A superconductive power generation R&D project with plans for commercialization in the 1990s; 70,000kw and 200,000kw

- Nagoya University—A yttrium-barium-copper oxide superconductive filament using method similar to synthetic fiber wet spinning production; ceramic material injected into silver pipe 80 microns in diameter and 1m long; 82K critical temperature

- NEC—A SQUID and Josephson circuit using yttrium-barium-copper oxide ceramic; zero resistance at 77K; 1 x 1mm square of 10mm thickness; Josephson effect at 85K

- NEC/Anelva—Three superconductive thin-film sputtering machines (SPF-210S/332S/430S Series) for batch process processing

- NTT—A yttrium-barium-copper oxide (1:2:4.5:8.5 ratio) superconductive single-crystal thin film; 1.8 million Angstroms per square cm at 77K; 1.5cm-square area; 0.6- to 0.7-micron thick strontium titanium oxide (1:1:3 ratio) substrate

- Osaka Science and Technology Center/Osaka University—Recently established to promote information exchanges between public research institutes, companies, and universities in the Kansai (Osaka) area; Osaka University in charge of basic research

- Sanyo—A superconductive material; 100K zero resistance; team consisting of Sanyo's Tsukuba Research Institute, Central Laboratory, and Applied Technology Research Institute; plans to concentrate on superconductive magnet for MRI system for image diagnosis, an energy storage system, and supercomputer

- Sharp—A superconductive magnetic sensor (Super Magneto-Resistor) using yttrium-barium-copper oxide; 83K zero resistance using liquid nitrogen; 1.0 x 7.0 x 0.7mm device; resistance at 10 Gauss

- Sumitomo Electric—A yttrium-barium-copper oxide (1:2:3:7) superconductive crystal thin film; 32,000A/square cm at 60K; 2 x 3 square cm; 0.1- to 1.0-micron thickness

  - A yttrium-barrium-copper oxide superconductive material with zero resistance at 27 degrees Celsius (300K); Meissner effect verified; 7mm diameter by 3mm thick; five samples tested

- Tokyo University—A yttrium-barrium-copper oxide superconductive material with zero resistance at 77K; compound ground and mixed with organic binder to make thick film paste; 10- to 15-micron film screened onto zirconia substrate and fired at 800 to 1,000 degrees Celsius

- Toshiba—A superconductive wire and tape; 93.7K zero resistance temperature; yttrium-barrium-copper oxide material baked in 30 x 10 x 6mm bulk form; 77K critical current density of 191A/square; wire rods with ceramic cores 0.5mm diameter, and 5.0mm-wide x 0.1mm-thick tapes

- Toshiba/Showa Wire & Cable—A copper-covered superconductive 0.6mm-diameter wire and superconductive tape with 0.1mm thickness and 55mm width; superconductivity at 93.5K; zero resistance at 87K; critical current density of 6A/square cm (77K)

- Toshiba/Research Institute of Electric Power Industry—A jointly developed superconductive coil of 500 kVA; copper-nickel alloy wire with 0.112mm diameter containing 15,000 superfine niobium-titanium alloy wires with a 0.45-micron diameter; wire wound on a core with grooves to minimize vibration; 4K temperature required; 0.007 percent power loss

Standard Logic

- Fujitsu

  - A 2-GHz ECL standard logic IC (10K); flip-flop function; OR/NOR gate (150ps internal gate delay; 79mA); exclusive-OR/NOR gate (220ps/79mA); D flip-flop (88mA); price at ¥25,000 ($166); 1-GHz flip-flop (MB810A Series) at ¥3,000 ($20)

  - Multiplexer/demultiplexer; 2 GHz; 263mA/260mA operating current consumption; 1-micron emitter; super self-aligned technology (SAINT) process; 24-pin ceramic flat package

- Matsushita/Tohoku University—A multiple-valued logic multiplier with computing speed 1.4 times faster than CMOS LSIs; quarter algorithm logic system and new multiple-valued MOS current-mode circuitry; 40ns 32 x 32-bit multipler developed featuring 0.5W power consumption and 5.23 x 3.16mm chip; for use in AI, robots, and machine translation systems; commercialization within two to three years

- NEC—High-speed CMOS standard logic (MuPD74HC Series); 14/16/20-pin; 225-mil and 300-mil miniflat packages

- Toshiba

  - A CMOS standard logic IC (TC4S); 2.9 x 1.9 x 1.1 mm package; molding resin; sampling for ¥150 ($1)

  - BICMOS Standard logic ICs (TD74BC series); CMOS I/O control circuits; bipolar output circuit; sampling since August

Ballistic Transistors

- Tohoku Metals—A static induction transistor (SIT) for satellite receivers; twice the radiation hardening of MOSFETs; depression mode difficult to use; work on easier-to-use enhancement mode; original research done by Dr. Junichi Nishizawa at the Semiconductor Research Center in Sendai City

Linear/Analog

- Sony
  - High-frequency A/D converters; 0.6-micron process with ECL structure; 0.3W power consumption for 200-MHz model, and 1.4W for 300-MHz model; sampling at ¥180,000 ($1,240) for 200-MHz version and ¥270,000 ($1,860) for 300-MHz version
  - A flash 8-bit A/D converter series (CX20116/CXA1056P/1016P/1066K); a D/A converter series (8-bit CXA1106P and 10-bit CX20202); an 8-bit A/D converter (CXA1176K) with 120-MHz full-scale input frequency width
- Toshiba—A BICMOS 8-bit D/A converter; 2M samples per second; 0V to 4V output power; 7mA power consumption; 3.56 x 2.64mm chip; 2-micron MOS transistor gate and bipolar transistor emitter; 300-mil (7.62mm) package; 24-pin DIP

Telcom ICs

- Fujitsu—A 3Gb per second multiplexer/demultiplexer device; 1.5-micron bipolar process; processing of two to four channels in optical cable TV and optical LAN systems; 24-pin, flat round package with 7mm diameter

New Semiconductor Functions

- Fujitsu—A wafer scale integration (WSI) technology for FFT processors; 12,000 to 13,000 FFT circuits
- Matsushita—A radiation-hardened LSI for the ERS-1 earth resource survey satellite computer; 1992 launch date planned; plans for AI processor development
- MITI/ETL—A temperature-hardened transistor capable of withstanding 400 degrees Celsuis

Materials

- Mitsubishi Metal—A titanium material with 99.999 percent purity for use in sputtering fine coats on semiconductor substrates for 4Mb+ DRAM development; conventional refinery processes used; details of proprietary process not disclosed

Photoresist

- Sumitomo Chemical—An ultraviolet-type photoresist for 16Mb DRAM mass production; capable of extending 0.6-micron lithography to 0.5-micron process

Manufacturing Processes

- Matsushita
  - An isolation film-forming technology of oxide silicon using optical CVD and spin-on-glass (SOG) methods; adaptable to 16Mb DRAMS and 0.6-micron design rule and aluminum wiring
  - A metal ion beam source for VLSI thin-film manufacturing; 60 x 80mm device that produces a high-density plasma of 10^{12} ions per cubic cm; feeds sputter substance by increasing magnetic field for discharge to 1.2 to 1.6 kilogauss
- NTT—A 0.01-micron process using SOR equipment at the Photon Factory operated by the Ministry of Education's High Energy Physics Laboratory; CVD thin-film process used
- Sumitomo Chemical—A photoresist capable of 0.5-micron process (Sunresist PF9200); single-layer type; designed for 436nm wavelength UV; for 16Mb DRAMS
- Sumitomo Metal—An electron cyclotron resonance (ECR) plasma CVD prototype machine for laying amorphous silicon films

Manufacturing Equipment

- Mitsubishi Electric—An electron beam processing system (EB Microprocessor (MuEBM)) capable of welding, surface treatment, and marking of small precision parts; priced at ¥43 million ($286,700) for continuous differential pressure air exhaust version and ¥32 million ($213,000)
- Nikon—An i-line excimer stepper (NSR-1010i3) for 16Mb DRAMs; 0.5- to 0.35-micron process; 15mm exposure area; current NSR1505G4D for 4Mb DRAMs using 0.5-micron process (0.486-micron wavelength)

- Sumitomo Heavy—Plans to complete SOR machine for 16Mb+ DRAMs by April 1988; commercialization with two to three years; development cost ¥100,000 million to ¥200,000 million ($666,700 to $1.3 billion)

Test and Inspection Equipment

- Ando Electric—A logic simulation machine (AU-4101); timing chart input vector; software/hardware; priced at ¥5 million ($33,333)

- Hitachi—A high-speed electron beam tester that analyzes faults in ASICs and other LSIs; 10 to 20 times faster than metal probe tester and 3 to 5 times faster than conventional E-beam testers; priced at ¥130 million ($866,700); thermoelectric field radiation electron gun and electron optical system capable of measuring LSI waveform with 0.1-micron diameter beam; 10ps time resolution; 10mV voltage resolution in 2-GHz bandwidth

- Mitsubishi Electric—A multilayer LSI probe inspection technology employing ion beam deposition; 0.1-micron beam; tested on lower aluminum layer of ECL gate array; 4 minutes to probe 1.9-micron hole in isolation layer; 10 minutes for 1.0 micron layer

- Toshiba—A silicon wafer impurity inspection machine featuring a three-pole structure oxygen ion method; priced at ¥58 million ($386,7000)

Interconnection

- Sumitomo Electric—A high-purity copper bonding wire for semiconductor device wiring; 99.999 percent purity

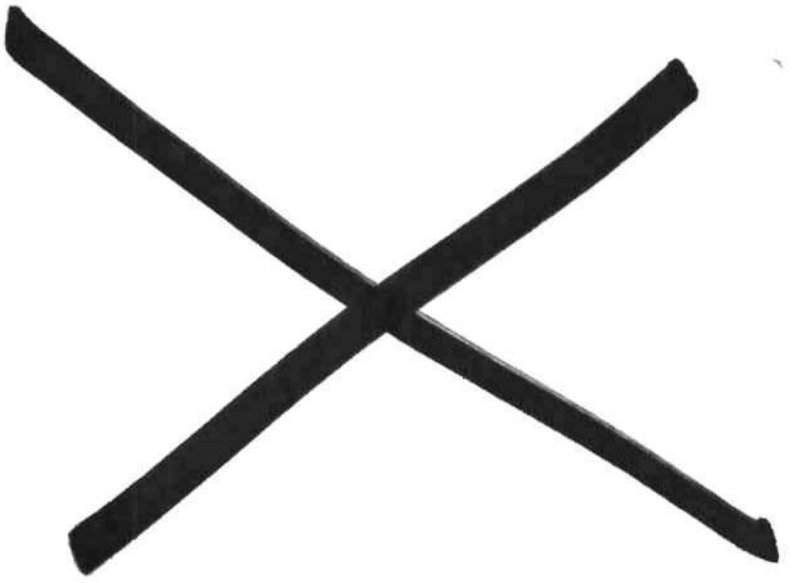
Packaging

- Fujitsu—A 14-pin flat package for 10-GHz to 20-GHz bipolar and GaAs LSIs; 0.3dB loss; 0.4mm ceramic alumina on ceramic substrate; 1.27mm pitch between I/O pins

- Fujitsu/Mitsubishi/Sony—Standards for compact IC packages; four very small outline packages (VSOP) and five very small quad flat packages (VQFP); emboss taping employed with new mounting systems; 1.27mm pitch for SOP; 0.65mm for VSOP; 0.65mm for QFP; 0.5mm for VQFP; 6.4 x 5.0 x 1.2mm package for 16-pin VSOP; 16.0 x 16.0 x 1.4mm for 100-pin VQFP

- Hitachi—A metal bonding wire method for attaching copper to silicon chips

- Mitsubishi—A 44-pin molded flat package for 1/2-inch CCD sensors; 13.2mm square; 7.0 x 8.1mm chip; tested at 85 degrees Celsius and 85 percent humidity
- MITI/ETL—A ceramic packaging survey from January 1988 covering ceramic DIP, dual-line packages, and multilevel packages
- Toshiba—An aluminum-nitride package for VLSIs; 300-pin packages being shipped next spring; heat radiation three times that of conventional aluminum packages; for high-speed bipolar, logic, and GaAs ICs; five-layer wiring; direct pin connection to substrate
- Towa Precision—Japan's first automated ASIC packaging system (Compact Packaging System); priced at ¥18 million ($120,000)



Emerging Technologies

The following is a list of the material in this section:

NOTE: The arrow symbol indicates the latest documents's location behind this subject tab.

Neural Networks

INTRODUCTION

The First Annual IEEE Conference on Neural Networks held in San Diego, California, from June 20 to June 24, 1987, was a huge success. An estimated 1,500 people from a multitude of disciplines and countries were in attendance. Most of the papers at the conference were presented by academics and researchers. Distinguished contributors included Tokyo University's Shun-ichi Amari, Helsinki University's Teuvo Kohonen, Caltech's Carver Meade and John Hopfield, and Stanford's Bernard Widrow.

Based on discussions at the conference, Dataquest expects many of the industrial attendees to begin investigating this field. We estimate that as many as 1,000 of the attendees were new to neural networks. If a fraction of them enter the discipline, it will amount to a substantial expansion of effort.

Most of the commercial firms at the show focused their efforts on providing simulation tools and other support to organizations interested in implementing neural networks in their products. This ready availability of simulators should speed progress considerably. Imagine the progress that could have been made in digital computers if the early workers had available to them, off-the-shelf, the series 7400 TTL family.

This newsletter briefly explains what a neural network is, lists some of the applications discussed at the conference, summarizes the commercial exhibits, and reviews the simulators now becoming available.

Dataquest is implementing a multiclient study of neural networks for a limited number of clients. A brief description of the study is given in the conclusion of this newsletter.

WHY THE EXCITEMENT?

The neural network approach has the potential to solve a class of problems that are difficult or impossible to solve with current digital technology. Although this field is still in its infancy, Dataquest predicts that neural networks will eventually be as significant as the general-purpose digital computer.

There are four reasons for the excitement about neural networks: they can be trained, it appears they can generalize, they can be easily implemented in hardware or software, and they seem more than adequate for most tasks.

It appears that neural networks can be trained by exposing them to stimuli (such as handwriting samples) and giving them the correct response (e.g., "that was an H"). After some training, a properly designed circuit will begin to recognize the handwriting of various individuals reasonably well. Significantly, this can be accomplished with little or no programming.

The neural network will generalize. For instance, it will recognize an "H" written by a second individual, even though it is not precisely like the characters it was trained with. In other words, it can tell when a character appears "pretty much like an H."

Neural networks can be implemented in software or hardware. Most commercial firms are currently building simulators, but the prospect of compiling silicon chips from these same simulators is also being considered.

Finally, both the simulators and hardware can handle networks of much greater complexity than those being described in current research papers. As this "applications gap" closes, some significant commercial products could result.

REVIVAL OF AN OLDER DISCIPLINE

Work on neural networks began as long as 24 years ago. At the conference, Professor Bernard Widrow of Stanford described some of the work he had done on the ADALINE and MADALINE devices in the early 1960s. These neural networks were able to perform crude character and voice recognition and were even applied to weather forecasting.

Early work in this field was minimal, partly because Marvin Minsky (of artificial intelligence fame) showed that some of these networks were not likely to perform useful functions. Recently, John Hopfield of Caltech and others took a fresh point of view, which circumvented some of the limitations pointed out by Minsky. This event was as electrifying to the field of neural networks as the recent discovery of high-temperature superconductors.

ARTIFICIAL NEURONS AND REAL NEURONS

Much work is being done on artificial neurons. An artificial neuron can be a software program or a piece of hardware that simulates the behavior of a biological neuron. These devices simulate only part of the behavior of a real neuron. It is not possible to simulate the entire behavior of a neuron, since its entire behavior is not well understood.

Neural Networks

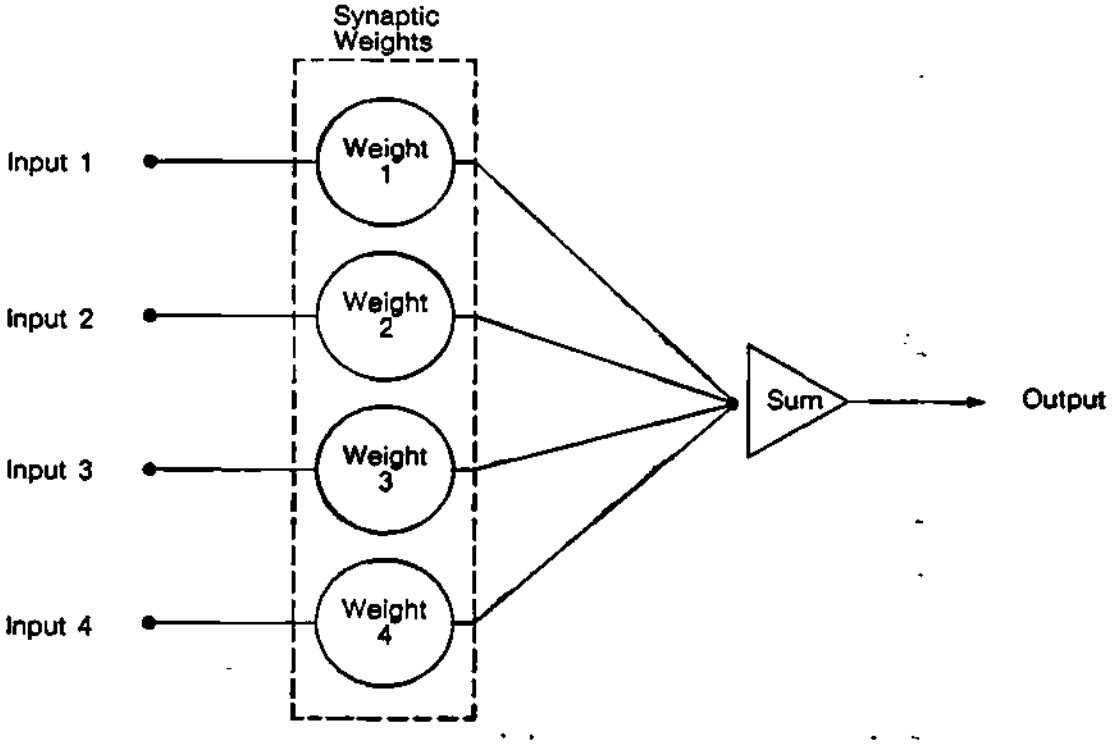
Many papers at the conference dealt with the behavior of real neurons. This work is usually done by researchers from the biological sciences and involves the measurement of electrical signals in living organisms. Several papers presented information about the strings of pulses that appear in real neurons. Some of the patterns in these strings of pulses appear to be repeated on a nonrandom basis. The function of these pulses is unclear; research is continuing.

WHAT IS AN ARTIFICIAL NEURON?

Figure 1 is a diagram of an artificial neuron. This neuron has four inputs and one output. The inputs are connected to a summing unit through a device that applies a synaptic weight. The magnitude of the neuron's output depends on the magnitude of the inputs, as modified by the synaptic weights.

Figure 1

DIAGRAM OF AN ARTIFICIAL NEURON



Source: Dataquest September 1987

A single neuron can make only one decision. For example, the neuron in Figure 1 could be trained to respond positively if two or more inputs were present. Training could be accomplished by giving the neuron a variety of different inputs. For each situation (e.g., three inputs present), the synaptic weights would be modified until the correct output is achieved.

It is not necessary to provide all possible combinations of inputs to train the neuron. Even though it has not been trained on an input pattern, the artificial neuron will give a reasonable output when that pattern is applied. Some believe that this indicates an ability to generalize.

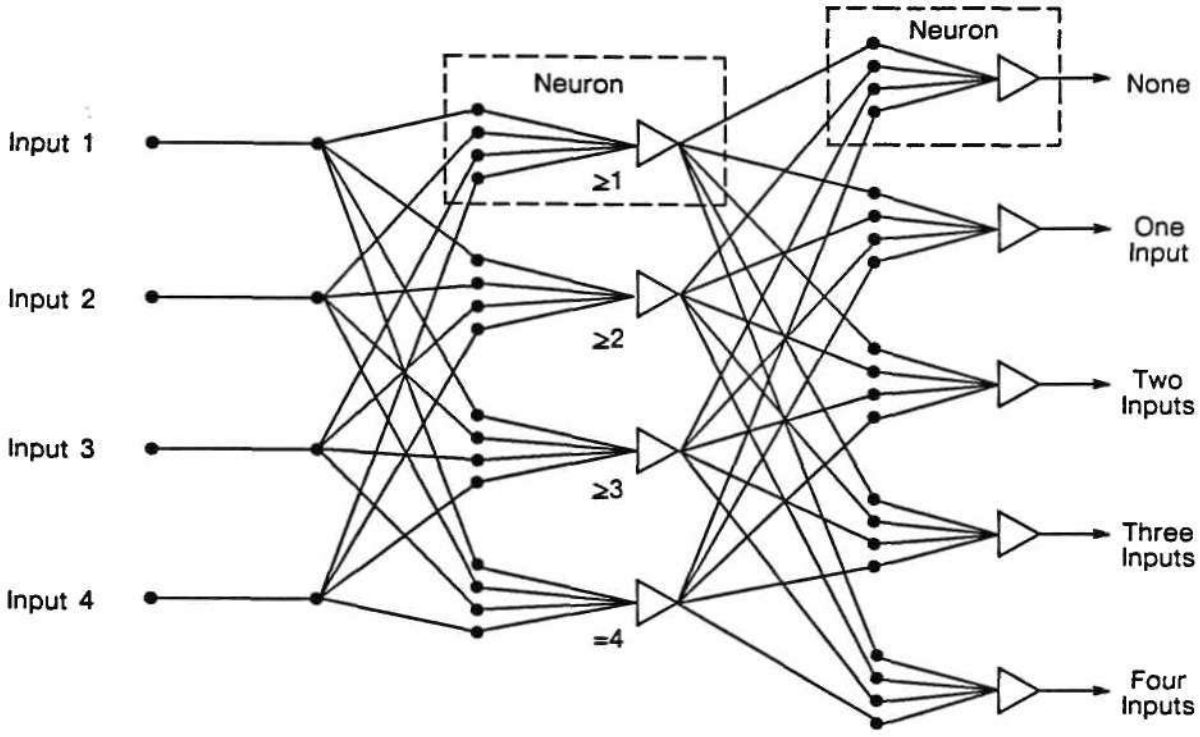
WHAT IS AN ARTIFICIAL NEURAL NETWORK?

An artificial neural network is simply a number of neurons that are interconnected similarly to the illustration in Figure 2. This network has two layers of neurons and might be trained to recognize the exact number of inputs present. The first layer might recognize one or more inputs, two or more inputs, and so on. The second layer looks at the output of the first layer and recognizes exactly one input, exactly two inputs, and so on.

This artificial network is much less complex than a practical network. A practical network for recognizing handwriting might contain hundreds of neurons in the first layer and as many neurons in the second layer as there were different characters to be recognized.

Figure 2

AN ARTIFICIAL NEURAL NETWORK



Source: Dataquest
September 1987

IMPLEMENTATION OF ARTIFICIAL NEURONS

Artificial neurons are implemented in a variety of ways. Hardware researchers use resistive summing networks or optical computers. Simulation and development tools implement the neuron in software. In a resistive network, the resistor that implements the synapse must be varied as the neuron is trained. AT&T has used a resistive ladder driven by an up/down counter to accomplish this. Others have suggested the use of the floating-gate MOS transistor to implement this variable resistor. This device is currently widely used in EPROMs and EEPROMs.

A half-day session was devoted to optical computers. Optical computers represent the inputs to the synapses as a beam of light. The synaptic weights are often represented by a translucent device in which the transmission of light can be changed as the synaptic weights are varied.

Simulators and development tools use a program that simulates the neuron by multiplying the numerical value of the inputs by the value of the synaptic weights. The result is accumulated over all synapses in a storage location that represents the output of the neuron. Simulation thus requires a series of multiply-accumulate operations.

Digital signal processors also require a series of multiply-accumulate operations. Thus, digital signal processing hardware is suitable for simulating neural networks. Texas Instruments demonstrated its explorer artificial intelligence workstation with an Odyssey digital signal processor board as a neural network workstation.

Artificial neurons vary in many other ways. Inputs may be analog or digital, and different synaptic inputs may behave in different ways. In addition, a number of different schemes exist for training the network to reach its optimal synaptic weights. Many papers at the conference discussed the pros and cons of these various techniques.

NETWORK COMPLEXITIES

Most applications presented at the technical sessions or at the exhibits used only tens or hundreds of neurons interconnected in not more than 10 layers. In contrast, current simulators and proposed VLSI chips can implement much more complex networks. Simulators seem able to handle thousands or even millions of neurons. Artificial networks made with VLSI technology appear able to occupy an entire wafer. This is possible because a network with some inoperative neurons can still be successfully trained to perform the desired function. (Widrow, in his speech, described the successful training of a neuron in which 25 percent of the synapses were inoperative.) Today an entire wafer contains a billion transistors. One speaker estimated that it should be possible to implement 50,000 neurons on such a wafer.

Interestingly, available hardware offers much greater levels of complexity than is currently being considered in most research work. The prospect of closing this "applications gap" is cause for much of the excitement in the neural networks field.

Living things have nervous systems that are even more complex. Hopfield estimated that a pigeon's brain has about a billion neurons. The human nervous system is estimated to have between 30 billion and 100 billion

neurons. Thus neural networks show promise of being able to utilize technological advances in computer processing and VLSI fabrication for many years after the applications gap is closed.

APPLICATIONS DESCRIBED AT THE CONFERENCE

Many applications were demonstrated or discussed. Among them were:

- Robotics control--A simulation of paper-tension control in a paper factory was presented by AIWARE Inc. Widrow's presentation described a neural circuit for balancing a broom on its handle.
- Artificial intelligence--Several researchers pointed out that neural networks could generate the rules in a rule-based system by simply observing the behavior of the experts. This would eliminate the need for having a sophisticated programmer formulate the rules.
- Pattern recognition--Two companies had good handwriting analyzers: HNC and Nestor. Other applications included submarine sonar signature analysis and radar signature analysis.
- Vision--Many papers analyzed functions of the eye and proposed systems to duplicate its performance. Carver Meade had a movie of an artificial retina made on a silicon chip. Dr. Meade has reportedly designed 500 neural network chips so far.
- Inspection--A neural network should make a good inspector when tied into a vision system. It should be able to detect gross defects and generalities such as "Is the label on straight?"
- Data base management--It was suggested that a neural network should be good for eliminating duplications in a mailing list. It should be able to recognize that H. Jones is the same person as Howard Jones if the address is the same.
- Data Retrieval--A paper described a software system that used neural networks to generalize a researcher's selection of reference documents and then continue his search based on that generalization.
- Transportation routing--Neural networks should be good for analyzing airline load factors, recommending optimum flight schedules, or solving similar problems.
- Forecasting--Widrow described a weather forecasting system in his talk. This early device used only one neuron. After being trained on several years of weather, it was able to equal the accuracy of the human forecasters.

COMMERCIAL EXHIBITS

A number of firms were represented at the commercial exhibits. In most of these firms the number of individuals involved in neural networks is 25 or less. Many of these companies pursue an OEM sales strategy and focus on helping their customers apply neural networks. A description of some of the exhibits follows.

AIWARE Incorporated, Cleveland, Ohio

This company provides hardware and software for process control. It demonstrated a simulation of paper-tension control in a paper factory.

General Dynamics Electronics, San Diego, California

The company's artificial intelligence center is developing neural network applications in situation assessment and weapon allocation.

HNC (Hecht-Nielsen Neurocomputer Corporation) San Diego, California

This company showed the ANZA board-level neurocomputer operating in an IBM PC AT. Applications on display included a handwriting recognition display for the digits 0-9, working from a graphics tablet (this application used 200 neurons) and a system to recognize human faces working from a TV camera. Often, this system could recognize a face it had memorized, even when that person wore a false mustache.

Human Devices, New York City, New York

Human Devices displayed the Parallon (TM) plug-in board for the PC AT. This board has 8 NEC V20 microcomputers running at 8 megahertz with 32 Kbytes of no wait-state RAM. It should make a high-speed neural simulator.

Meiko Computer, Incorporated, Oakland, California

Meiko displayed a parallel processor using the INMOS transputer.

Nestor, Incorporated, Providence, Rhode Island

Nestor displayed a number of commercial products, including a handwriting recognition system.

Neural Networks

Neural Systems, Incorporated, Vancouver, British Colombia

Neural Systems demonstrated its AWARENESS software running on an AT&T PC 6300.

Neuraltech, Incorporated, Portola Valley, California

Neuraltech described applications in which neural network software was used to enhance an artificial intelligence system. It appears that neural networks make it possible to generate the rules in a rule-based system automatically.

Neuronics, Incorporated, Chicago, Illinois

Neuronics (TM) demonstrated the MACBRAIN (TM), a graphics-oriented neural network simulation system.

SAIC Technology Research, San Diego, California

This company showed a plug-in board for the PC AT that has a 20 mflop, 32-bit floating-point processor. This processor includes 12 Mbytes of on-card memory and processes up to 10 million connections (synapses) per second. It incorporates a triple-address scheme to simultaneously address the synapse input, the synapse weight, and the summing neuron. The computer uses a two-chip, high-speed, floating-point multiplier from Bipolar Integrated Technology.

Texas Instruments, Incorporated, Austin, Texas

Texas Instruments (TI) demonstrated its Explorer artificial intelligence workstation hosting its Odyssey digital signal processing (DSP) board. Odyssey is based on four of TI's TMS 32020 DSP chips. DSP chips have an architecture that makes them excellent simulators of neural networks.

TRW Incorporated, San Diego, California

TRW demonstrated its Mark III neural network system. The demonstration included image processing and radar target recognition.

VERAC Incorporated, San Diego, California

Verac displayed computer simulations of associative memories.

A number of exhibits described newsletters, publications, or training courses in neural networks. The organizations represented included:

ACADEMIC PRESS, Orlando, Florida
LAWRENCE ERLBAUM ASSOCIATES, Hillsdale, New Jersey
MIT PRESS, Cambridge, Massachusetts
NEUROCOMPUTER CONNECTIONS, South Hackensack, New Jersey

SIMULATORS

Simulators were shown by HNC, Human Devices, SAIC, Meiko, Neuronics, Texas Instruments, TRW, and others. Of these, HNC seemed to have the most advanced software. This software makes it easy for the user to specify the network without having to code it, synapse by synapse. A number of networks that differ in architecture are available. The firm hopes to establish its language as an industry standard.

Most of the other devices emphasized hardware and used some sort of parallel processing to implement the basic multiply-accumulate function. Of these, the board supplied by SAIC appeared to be the most powerful, with an ability to simulate up to 10 million synapses per second.

The biological nervous system is a massively parallel interconnection of rather slow electrochemical neurons. Despite the slow neurons, even the fastest multiprocessor has a difficult time keeping pace with a living being.

It's reasonable to assume that a biological nervous system averages 1,000 synapses per neuron. Since these react in about a millisecond, simulators are speed competitive when the number of synapses programmed can all be updated in a millisecond. Thus the SAIC device, at 10 million synapses per second, is equivalent to a biological network with about 10,000 synapses. At 1,000 synapses per neuron, this equates to only 10 neurons.

This example illustrates the potential massive processing power of artificial neural networks. If they are connected like the biological systems, they should be able to operate in parallel effectively, especially since their reaction time is in the microsecond or even the nanosecond range.

Neural Networks

DATAQUEST CONCLUSIONS

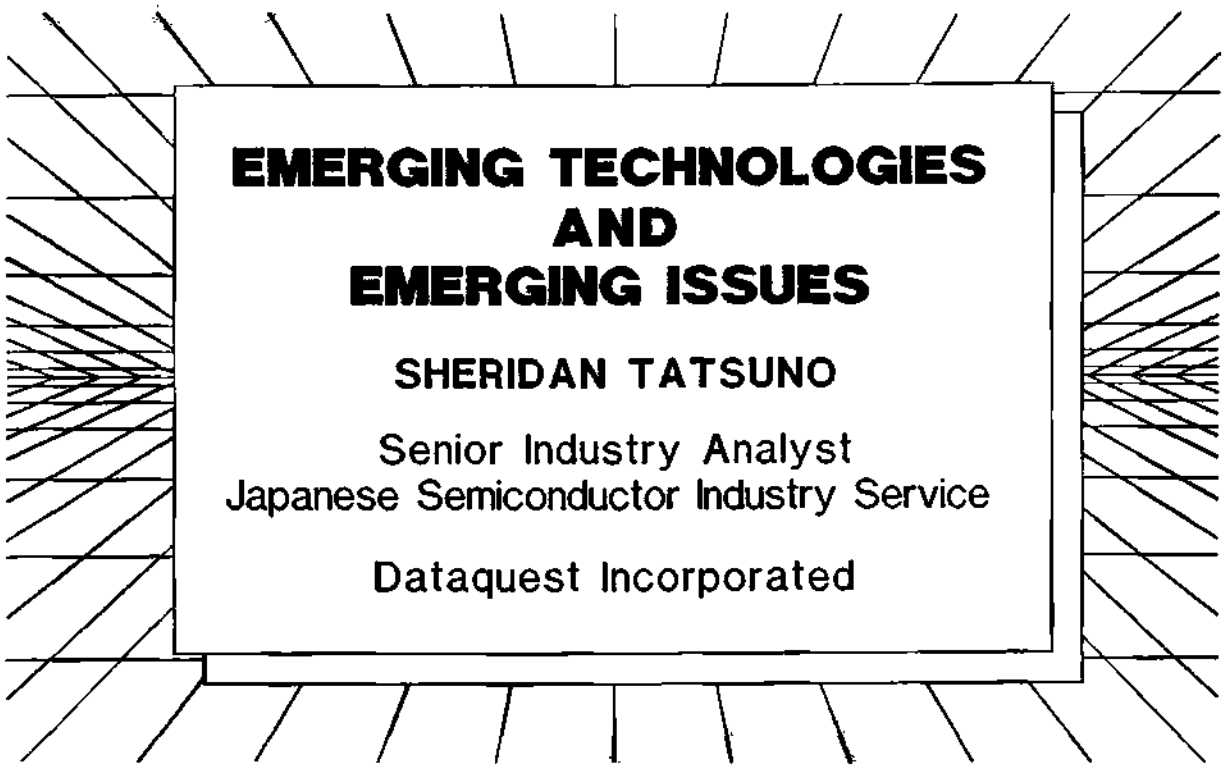
The first IEEE Neural Networks Conference was remarkable for the multidisciplinary nature of its attendees. Included were optical physicists, neural biologists, computer scientists, mathematicians, psychologists, physicists, biologists, neurologists, electronic engineers, and artificial intelligence experts. Those from the life sciences were busy dissecting animal and human nervous systems to see how they work, while physical scientists were building artificial neural models to see whether they could replicate the performance of biological systems. This was the first opportunity that these researchers had to meet at a single conference.

The modern digital computer sprang from attempts to use electronic circuits to emulate the logical functioning of the human mind. Today, the success of that line of investigation is obvious.

Neural networks take the next step--they attempt to emulate the actual functioning of human and animal nervous systems, based on direct experimental observation. Dataquest believes that this research is likely to lead to commercial products as significant as digital computers. Some of the first of these products may appear in the next 3 to 5 years. Progress in this field is expected to continue for at least the next 20 years.

MULTICLIENT STUDY

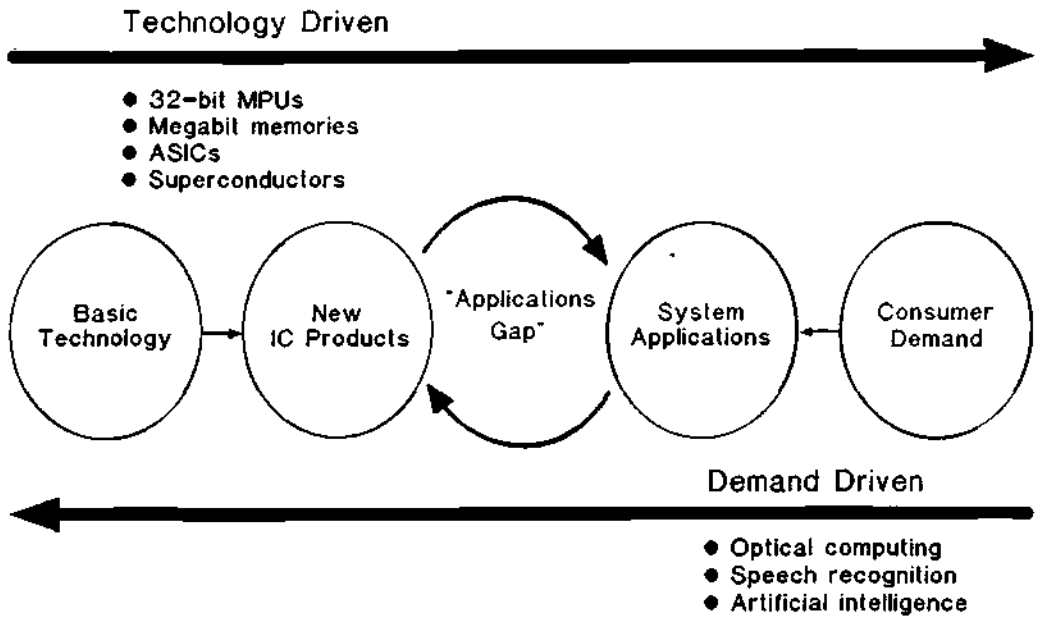
Dataquest is implementing a multiclient study on neural networks, which will be available to a limited number of subscribers. This study will analyze the probable development paths in this field and estimate the potential impact of this technology on markets followed by Dataquest. Subscribers will be advised of the level of involvement (if any) in this technology that might be appropriate for their firms. For further information, please contact Howard Bogert, Vice President at Dataquest, (408) 971-9000.



At Dataquest's special program at Semicon West 1987 in San Mateo, JSIS Senior Industry Analyst, Sheridan Tatsuno, gave a presentation on trends in emerging technologies. A copy of his speech is presented in the following pages.

Emerging Office and Home Systems

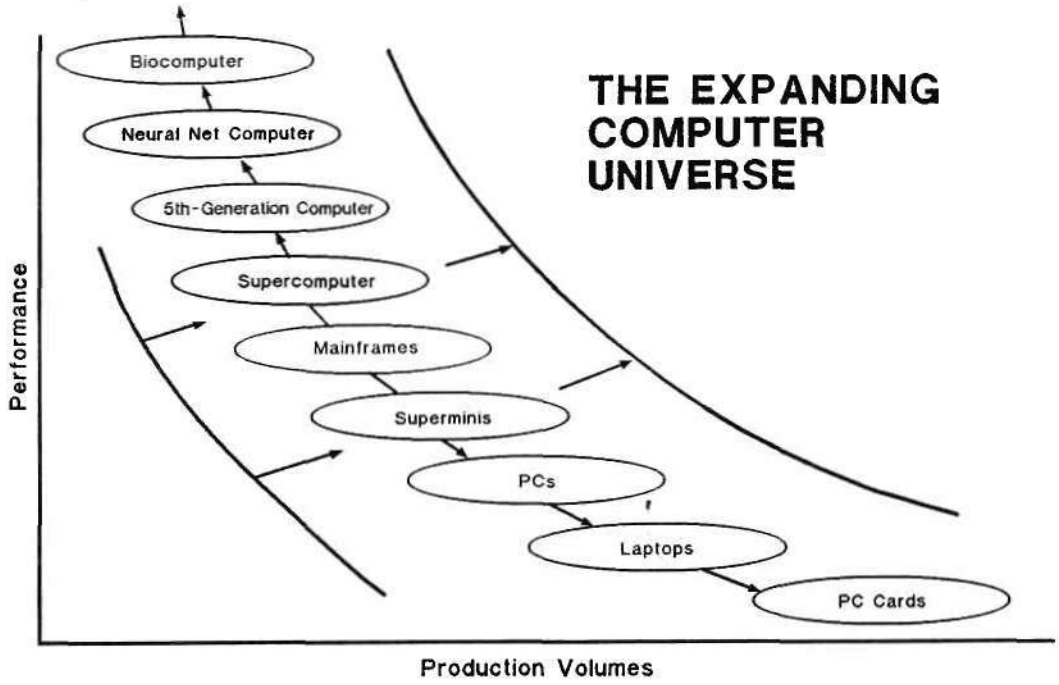
THE TECHNOLOGY VORTEX



Key points to note:

- Emerging technologies are the seeds of the future semiconductor industry, which need to be "watered" (cultivated) by applications engineers and users.
- However, the increasing pace of technological development is creating a growing "applications gap."
- User needs for more powerful, user-friendly systems that employ speech recognition/synthesis, sensing, AI, and optical inputting are growing, but still unsatisfied.
- Semiconductor device and equipment makers must work more closely with systems designers and their customers to provide the products that users need.

Emerging Office and Home Systems

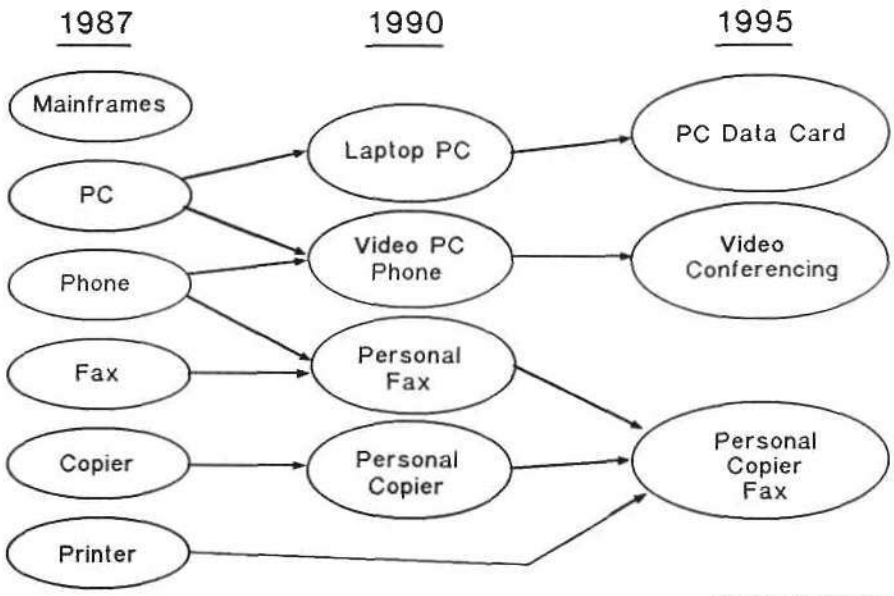


Key points to note:

- During the 1990s, the computer universe will rapidly expand in complexity and production volumes.
- At the high end, computer makers will introduce more powerful supercomputers, minisupers, embedded AI systems (in electronic banking and other areas), parallel computers, neural network architectures, optocomputers, and eventually biocomputers.
- At the low end, laptop PCs will lead to ergonomically-designed, tablet-size PCs and PC cards (smart cards with voice recognition chips). These application-specific low-cost PCs will pervade the office, home, automobile, factory, and entertainment sectors.
- The next successful computer company (like Apple Computer) will introduce a powerful, revolutionary "pocket PC," like the Walkman or Watchman, probably with voice recognition/synthesis capabilities.

Emerging Office and Home Systems

EMERGING OFFICE SYSTEMS



Source: Dataquest

Key points to note:

- Innovative new office technologies will be found in hybrid or dual-use systems that require less space and offer greater performance.
- Japanese companies are already introducing personal facsimiles and copiers.
- Nippon Telegraph and Telephone Co. (NTT) has introduced an experimental video phone that features a television set equipped with a CCD sensor. Eventually, this set could be merged with the office PC to provide videotext and video conversations.
- Prototype "silicon disks" are being developed in Japan to replace floppy disks. These disks could be linked to IC data cards for easy data transfer and security.

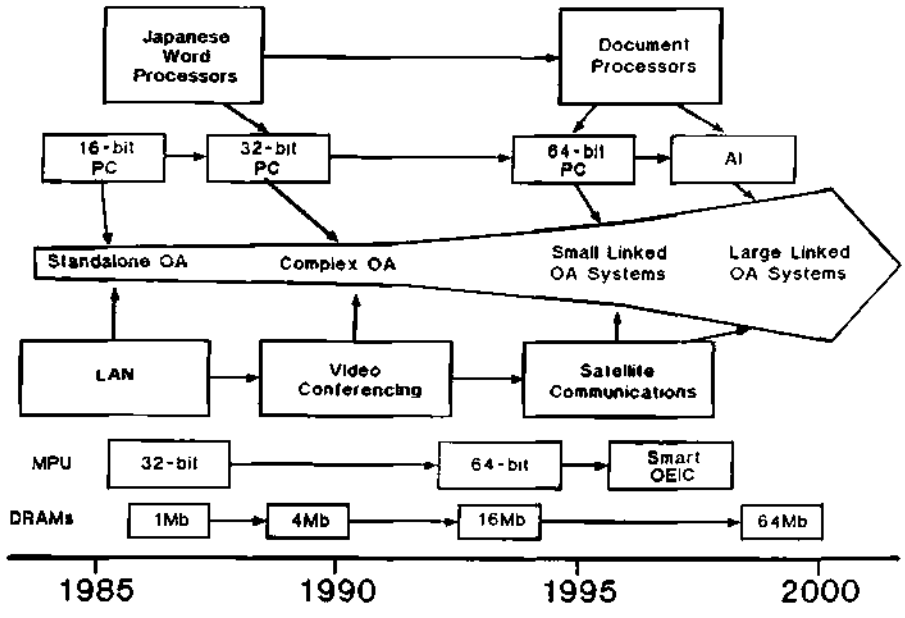
THE OFFICE OF THE FUTURE

Key points to note:

- The office of the future will feature a few dual-use systems:
  - The laptop or tablet PC linked to the telephone for video conversations and data transfer
  - The printer/copier/fax system linked to the telephone and PC, either with wires or remote signal controllers
- The emphasis will be on simplicity, compactness, high performance, data security, and user friendliness.

Emerging Office and Home Systems

OFFICE SYSTEM TRENDS



Source: Dataquest

Key points to note:

- Japan's Ministry of International Trade and Industry (MITI) developed an office systems forecast that is very similar to Dataquest's trend forecast.
- Japanese system designers will make several shifts:
  - From word processing to text processing
  - From 16-bit MPUs to parallel AI processors (64-bit RISC processors) and smart OEICs (MPUs with lasers)
  - From standalone systems to large linked OA systems
  - From local area networks (LANs) to satellite networks
  - From alphanumeric data processing to image and voice processing using megabit memories

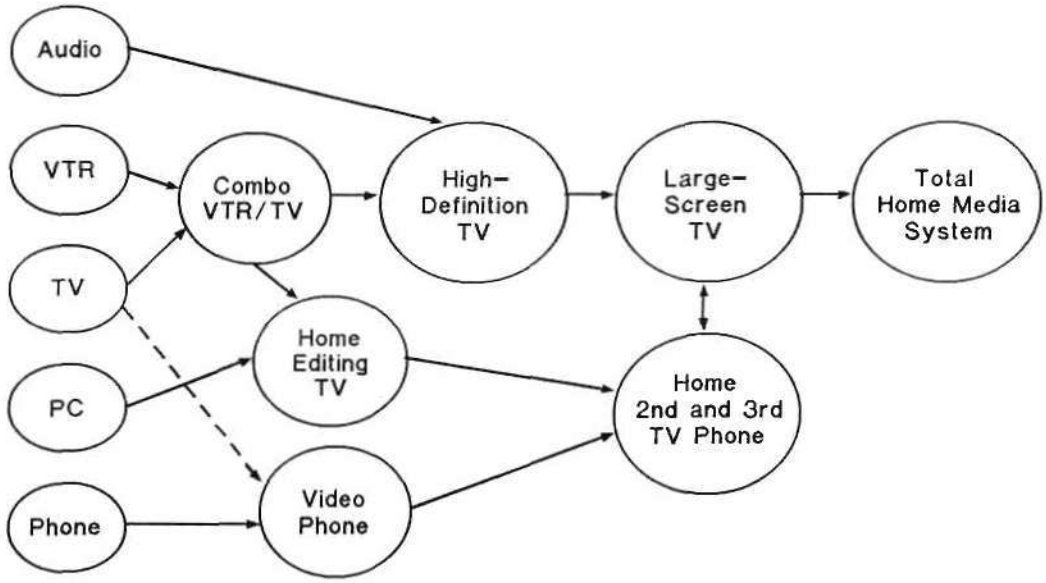
HOT NEW SEMICONDUCTORS FOR THE OFFICE

Emerging Systems	Semiconductors Needed
Laptop PC	"Sea of gates" ASICs Megabit memories (IC cards) Specialized 32-bit MPUs Voice recognition chips
Video PC Phone	CCD sensors Voice recognition chips IC card readers
Personal Fax/Copier	Advanced telecom ICs Printer font ROM cartridges Megabit memory storage

Key points to note:

- What will drive these new OA systems? Advanced semiconductors!
- Emerging office systems will require function-specific ICs (voice, image, parallel processing) as well as user-specific ICs (USICs).
- Except for voice recognition, which still requires a significant amount of research, semiconductor technologies already exist for emerging office systems. The emphasis will be on customizing and pushing the performance of these devices to specific systems.

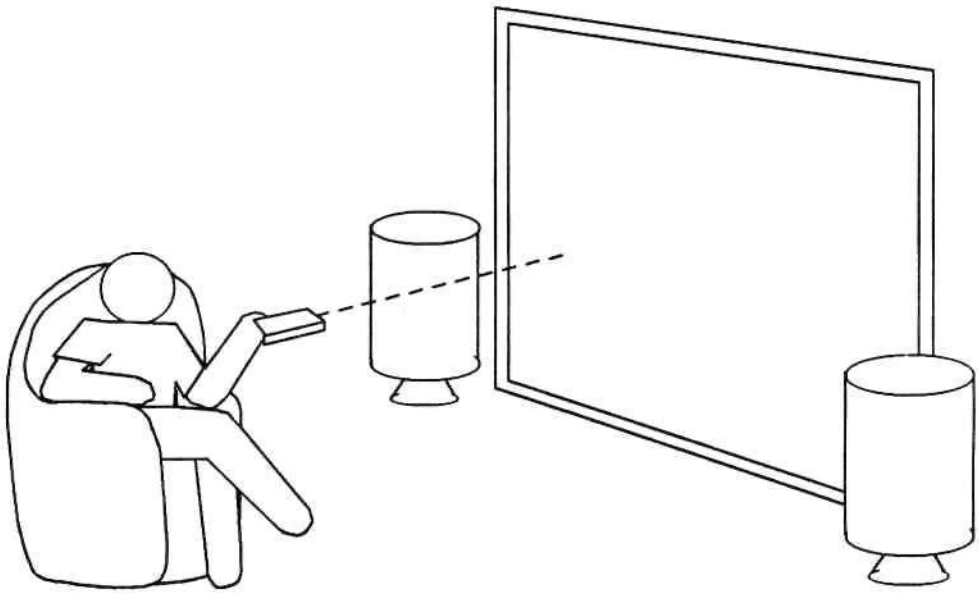
EMERGING HOME ELECTRONICS



Key points to note:

- As in OA systems, home electronic systems are merging into new hybrid systems.
- Japanese video makers are combining televisions and VTRs into one system to stay ahead of South Korean VTR makers.
- Eventually, the PC will be merged with combination television/VTRs to allow home video editing. Large-screen televisions (25 to 45 inches) will be the main entertainment systems, supported by second and third home television/PC sets to allow family members to watch different programs.
- Video phones featuring CCD camera lenses and video recording functions will become inexpensive and feasible for the consumer due to the oversupply of optical fiber capacity.

HOME VIDEO SYSTEM OF THE FUTURE



Key points to note:

- Japanese video companies are developing televisions that use flat CRT, color liquid crystal (LCD), and plasma, electroluminescent display panels. Flat CRTs have the greatest potential because of their display flexibility and brightness.
- Large-screen televisions will feature pulse-code modulation (PCM) digital sound and laser-based interactive remote controllers.
- Video game software makers have already introduced laser toy guns for interactive games.
- Consumer demand for better sound quality, especially for movies and concerts, will push home entertainment system makers to develop better, cheaper systems. We expect home television editing to become a major application of PC computing power.

HOT NEW HOME ELECTRONIC SEMICONDUCTORS

Emerging Systems	Semiconductors Needed
Large-Screen Combo VTR/TV	Video RAMs (4Mb/16Mb/64Mb) 32-bit video processors "Sea of gates" ASICs
Remote Control Handsets	Semiconductor lasers Voice recognition chips 32-bit controllers
Video Phone Sets (Second or Third TVs)	Voice recognition chips Video RAMs CCD sensors Specialized 32-bit video processors

Key points to note:

- Home electronic systems still have a relatively low semiconductor content (under 10 percent of the system price).
- VTRs are known as "IC hogs" in Japan because of their high semiconductor content (15 percent of the total price, or about 120 discrete and IC devices).
- Japanese video makers are using more large ASICs to reduce part counts and adding new features (line memory storage, video processors).
- Semiconductor lasers, CCD sensors, and voice recognition chips are being used to provide interactive programming and greater user friendliness.

FUTURE KEY TECHNOLOGIES

Devices	Applications
Megabit Memories (2-D and 3-D)	Video and voice storage PC data cards Icon generators
Specialized 32-bit MPUs	Video and voice processing Parallel processing Complex system controllers (handsets, PCs)
Optoelectronic ICs (OECs)	Semiconductor laser controllers Optical computing Video transmission processing Sensors
Superconductors	Ultrasupercomputing

Key points to note:

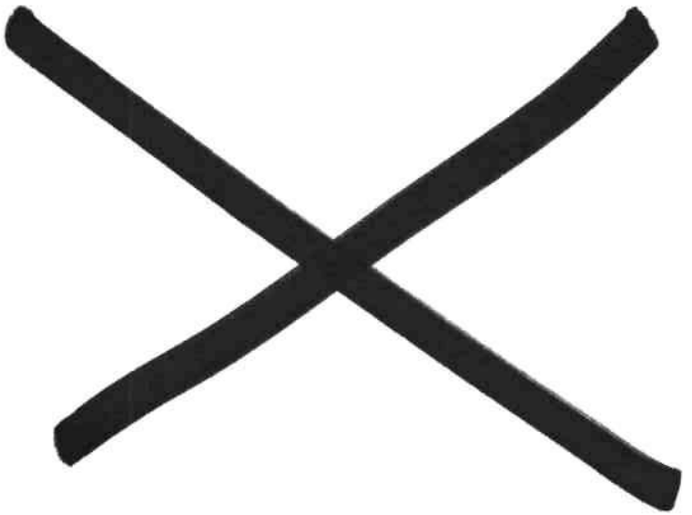
- Video and speech processing will use large amounts of megabit memory capacity. Semiconductor vendors will be pressured by users to rapidly reduce the cost per bit.
- While mainline 32-bit MPUs will be aimed at computing, specialized RISC MPUs will be required for video, automotive, and factory automation systems.
- Japan is pushing aggressively into OEICs, which will be critical for future computer, communications, and entertainment systems.
- Superconductor materials still face technical problems, but will eventually be used for computers, especially interconnection.

MEETING THE COMING TECHNOLOGY EXPLOSION

Service
- Closer vendor–user ties
- Linkage of marketing and after–sales servicing

Design
- 3–dimensional CAD tools
- Stronger applications engineering

Manufacturing
- Flexible modular fabs
- Increased status of manufacturing "researchers"
- Rotation between production and R&D
- Development of proprietary fab equipment



Strategic Alliances

The following is a list of the material in this section:

NOTE: The arrow symbol indicates the latest document(s) correct location behind this subject tab.

1988 Japanese Alliances

SUMMARY

The activity in Japanese semiconductor alliances peaked in 1987 and showed a sharp decline in 1988. As shown in Table 1, Japanese companies entered only 46 alliances in 1988, down from 124 in 1987. This declining activity was due to several factors:

- Japanese companies are busy implementing the alliances entered in 1986 and 1987.
- Foreign companies are increasingly reluctant to license or trade their technologies with Japanese chipmakers, although win–win joint ventures and joint development are still popular.
- There is growing interest in stronger vendor–user relationships as a result of Japan–U.S. talks on market access.

Table 1

Japanese Semiconductor Strategic Alliances (1980–1988)

Industrial Sector	1980	1981	1982	1983	1984	1985	1986	1987	1988
Devices	3	6	10	14	30	54	76	83	35
Equipment & Materials	0	5	12	8	26	17	25	41	11
Total	3	11	22	22	56	71	101	124	46

Source: Dataquest
April 1989

Dataquest believes that strategic alliances are undergoing a major change. Instead of vendor–vendor ties, we are seeing the rise of stronger vendor–user relationships, in which Japanese system houses are working closely with foreign semiconductor makers to design in new chips. These agreements are being driven by two key factors:

- The shift of Japanese system makers toward higher value-added products
- Non–Japanese pressures for greater access to the Japanese market

1988 Japanese Alliances

We observe that most of these vendor–user ties are not announced for strategic reasons. The Users Committee of Foreign Semiconductors, for example, recorded 300 design–ins during the first nine months of 1987, but only a few vendor–user relationships have been made public. (See Table 2.) These agreements are "design–with" alliances that will lead to long–term procurement.

Thus, Dataquest believes that while strategic alliances are declining, vendor–user "design–with" relationships are increasing. Some of these arrangements, such as the Fujitsu–Sun or NEC–MIPS Computer arrangements, have been immensely successful. We think that these arrangements are the wave of the future in Japan.

Table 2

Japanese Design–In of Foreign Semiconductors

User	Foreign Company	Application	IC Product
Hitachi	Intel	VCR	8-bit MPU
JVC	Philips	Televisions	Teletext IC
Matsushita	TI	Microwave oven	8-bit MPU
Mitsubishi	Motorola	VCR	8-bit MPU
Nissan	Intel	Engine control unit	16-bit MPU
Sanyo	Intel	Air conditioner	16-bit MPU
Sony	TI	CD player	Digital filter IC
Toshiba	Motorola	CD player	Motor drive IC
Toyota	Motorola	Engine control unit	8-bit MPU

Source: EIAJ
Users Committee of
Foreign Semiconductors

1988 Alliance Activities

For your convenience, Dataquest has summarized the strategic alliances publicly announced in the English– and Japanese–language press, as shown in Table 3. These alliances are categorized chronologically by device type, with separate categories for CAD tools, equipment, materials, packaging, and interconnection. In addition, each alliance is categorized by type of agreement and briefly summarized by a short description.

1988 Japanese Alliances

Table 3

1988 Japanese Semiconductor Alliances

Date	Japanese Company	Partner	Type	Products
Multiproduct				
05/88	Hitachi	VLSI Technology	2, 8	MPU, CMOS/BiCMOS process; EEPROM, nonvolatile
08/88	Oki Electric	SGS-Thomson	6	CMOS gate arrays; 256K/ 1Mb DRAM modules
10/88	Kawasaki Steel	Harris Corp.	8	Application-specific standard products
Memory				
02/88	NMB	TI	4	1Mb frame memory
04/88	Asahi Chemical	Int'l CMOS	1	32K/64K EPROMs
04/88	Sanyo Electric	Atomel Products	4	High-speed 1Mb EPROMs
07/88	Oki Electric	SGS Thomson	4	256K DRAM assembly
08/88	Oki Electric	Seattle Silicon	8	SRAM module compiler
10/88	NMB	Ramtron	8	4Mb DRAMs
11/88	NEC	Summit Microcir.	1	64K/256K fast SRAMs
12/88	Matsushita	Intel	8	16Mb DRAM process
12/88	Hitachi	TI	8	16Mb DRAM
Microprocessors				
02/88	Mitsubishi	National	3	32-bit MPUs (32000)
04/88	Sanyo Electric	VLSI Technology	3, 4	32-bit ACORN RISC MPUs
04/88	Toshiba	Zoran	4, 8	DSP
04/88	Sanyo Electric	TI	8	Image processors
05/88	Kawasaki Steel	Tomcat Computer	8	PC software interchange
05/88	VM Technology	Mitsui & Co.	9	32-bit MPUs
06/88	Fujitsu	Mizar/Wind River	8	SPARC RISC MPU
09/88	Hitachi	Intel Japan	11	Consumer MCUs
09/88	Matsushita	Sun Microsystems	1	SPARC RISC chip
10/88	Seiko Instruments	Sun Microsystems	1	SPARC RISC chip
ASICs				
03/88	Seiko Epson	S-MOS Systems	8	ASIC R&D center
04/88	Mitsui & Co.	European Silicon Structures (ES2)	3	Quick-turn ASICs
04/88	Oki Electric	iLSi	1, 4	Gate arrays
05/88	Toshiba	Advanced Silicon Corp (ASiC)	4, 8	Software, 6-inch CMOS wafers
08/88	Fuji Electric	Barvon	1, 4	Standard cells
Other Devices				
04/88	Sony	TI Japan	8	Digital audio filter LSI
04/88	Mitsubishi	National	4	High-speed TTLs

(Continued)

1988 Japanese Alliances

Table 3 (Continued)

1988 Japanese Semiconductor Alliances

Date	Japanese Company	Partner	Type	Products
Other Devices (Continued)				
05/88	Fujitsu	NEC	8	Antitank infrared seeker
06/88	Yamaha	Chips & Tech.	6	Chip sets, LSIs
07/88	Hitachi	Mitsubishi	10	EDTV chip sets
08/88	Japan Macnics	Honeywell SPT	3	A/D, D/A converters
08/88	Oki Electric	Seattle Silicon	8	SRAM module compiler
12/88	NEC	Optoelectronics Research Labs	8	Photodiodes
CAD Tools				
03/88	Seiko Epson	Tangent Systems	8	Sea-of-gates gate arrays
05/88	Kawasaki Steel	SDA Systems Other Devices	6, 11	ASIC CAD tools
Equipment				
02/88	Canon/IHI	Ateq	7	Optical reticle engraver
02/88	Nippon Kokan	Nippon Sanso	8	Ultraclean gas piping
05/88	Tokyo Electron	IMS/Mentor	3	Verification systems
Materials				
02/88	Nippon Sanso	Linde	1	Silane gas
02/88	Matsushita	Tosoh	8	E-beam resist
03/88	NTT	Motorola	8	New materials
09/88	Showa Denko	Crystal Special.	3	GaAs wafers
Packaging and Interconnect				
06/88	Nippon Steel Sumitomo 3M	Minnesota Mining	7	Tape automated bonding
07/88	Sumitomo 3M	Indy Electronics Mesa Technology Flextronics	7	Tape automated bonding
Agreement Updates				
01/88	Fujitsu/Hitachi	Mitsubishi	8	TRON chips
02/88	Toshiba	Tangent Systems	8	Gate array CAD
06/88	Kawasaki Steel	LSI Logic	8	ASICs fab
06/88	Toshiba	Motorola	8	1Mb DRAMs
06/88	Toshiba	Siemens/GE	8	Standard cells
09/88	Sony	AMD	8	64K/256K SRAMs
09/88	Hitachi	VLSI Technology	8	SRAMs
10/88	Toshiba	Motorola	8	68020
12/88	Toshiba	VISA Int'l.	8	IC card chips

Source: Dataquest
April 1989

1988 Japanese Alliances

CLASSIFICATION OF AGREEMENTS

Dataquest classifies strategic alliances into 12 major categories:

1. Licensing Agreement—Japanese company receives or issues a license to partner for an upfront fee and/or royalties.

2. Second-Source Agreement—Both companies agree to develop consistent specifications to ensure a second source.

3. Sales Agency Agreement—Japanese company sells partner's products, either as a sales representative or value-added reseller (VAR).

4. Fab Agreement—Japanese company offers fab capacity for partner's product technology.

5. Assembly and Testing Agreement—Japanese company sends or receives devices for assembly and/or testing.

6. Technology Exchange—Both companies exchange technology, which may or may not include a transfer of money.

7. Joint Venture—The two companies form a new joint-venture company to develop, manufacture, and market new products.

8. Joint Development—Both companies jointly agree to develop new products, which may or may not be marketed separately.

9. Investment—Japanese company invests in partner company (less than 50 percent of equity) to secure new technology or access to new markets.

10. Coordination of Standards—Japanese company and partner agree to device standards to ensure compatibility.

11. Procurement Agreement—Japanese company will buy more foreign semiconductors as part of market access program.

12. Other—Joint symposia and programs.

The following paragraphs describe the strategic alliances entered by Japanese semiconductor device and equipment makers in 1988.

1988 Japanese Alliances

Multiproduct

Hitachi and VLSI

In May 1988, Hitachi and VLSI Technology signed a wide-ranging agreement covering cross-licensing, technology exchanges, and joint product development. Initially, Hitachi will provide its new 1-micron and submicron CMOS and BiCMOS process, its electrically programmable and flash nonvolatile memory technologies, and its advanced CMOS process and manufacturing technologies. The goal is to become process-compatible. VLSI will second-source Hitachi's H Series of 8-, 16-, and 32-bit MPUs. The H32 runs the TRON operating system. VLSI will provide its standard-cell CAD tools. The companies will jointly develop MPU peripherals, ASIC memories, and ASIC analog circuits. Hitachi's 8-bit 64180 MCU core and VLSI's 16-bit Acorn RISC may be included.

Oki Electric and SGS-Thomson

In August 1988, Oki Electric renewed its CMOS gate array cross-license contract with SGS-Thomson Electronics. It will now include subcontracting of memory production. Oki will commit production of 256K and 1Mb DRAM modules to SGS-Thomson's Nancy Factory, which will use the same type of production line as Oki's Miyazaki plant.

Kawasaki Steel and Harris

In October 1988, Kawasaki Steel and Harris Corp. agreed jointly to develop and market application-specific standard products (ASSPs) over the next three years. Image processing, industrial control, and telecommunications devices will be the major focus. Kawasaki will market the custom and ASSP devices in Japan and Asia. Harris will produce the devices in Melbourne, Florida, and sell them in Europe and the United States.

Memory

NMB Semiconductor and Texas Instruments (TI)

In February 1988, NMB signed a contract with TI (Dallas) to produce 1Mb frame memory chips, which will allow TI Japan to increase its output of 1Mb DRAMs using advanced trench capacitor technologies for computer and telecommunications customers. NMB's frame memories are based on conventional planar capacitor technology for use in digital TVs, copying, and facsimile machines.

Asahi Chemical and International CMOS Technology

In April 1988, International CMOS Technology licensed Asahi Chemical to manufacture 32K and 64K EPROMs with 35ns to 55ns access times. Production began in the summer of 1988.

1988 Japanese Alliances

Sanyo and Atomel Products

In April 1988, Sanyo Electric signed a foundry contract to produce high-speed 1Mb EPROMs for Atomel Products Corporation (Sunnyvale, California). Sanyo VLSI Engineering will manufacture the 100ns, 256K and 512K CMOS EPROMs, while Sanyo Electric and Atomel will jointly develop 70ns EPROMs.

Oki Electric and SGS-Thomson

In July 1988, Oki Electric entrusted SGS-Thomson Microelectronics with assembly of Oki's 256K DRAMs at the former Thomson Semiconductor's Nancy plant in southern France. The plant will use the same type of production line as Miyazaki Oki Electric. Production began with 256K DRAM modules and will shift to 1Mb DRAM modules.

Oki Electric and Seattle Silicon

In August 1988, Oki Electric and Seattle Silicon signed an agreement to develop jointly a compiler for a process-independent, five-port, static RAM module.

NMB Semiconductor and Ramtron

In October 1988, NMB Semiconductor and Ramtron agreed to develop jointly 4Mb DRAMs. Under the agreement, NMB has access to Ramtron's ferroelectric memory design know-how and advanced materials processing technology. Ramtron's Sheffield Eaton helped NMB with its 256K DRAM design. Ramtron has access to NMB's semiconductor process development and automated fab. The companies will jointly own the codeveloped technology, but NMB will have exclusive rights to the 4Mb DRAM products. NMB is building a $400 million third fab module with a Class 1 clean room in Tateyama that will be used primarily for 4Mb DRAMs.

NEC and Summit Microcircuit

In November 1988, NEC entered a consignment research agreement with Summit Microcircuit of Texas to develop 20ns, 64K and 256K SRAMs. NEC plans sampling from the summer of 1989. Summit is a semiconductor design house established in December 1987 by ex-Inmos researchers.

Matsushita and Intel

In December 1988, Matsushita Electric and Intel signed a contract to exchange 16Mb technical information and pursue joint development of sub-0.5-micron process techniques. Intel sent engineers to Matsushita's Semiconductor Research Center. The project will focus on high-output excimer lasers.

1988 Japanese Alliances

Hitachi and TI

In December 1988, Hitachi entered a major three-year agreement with Texas Instruments to develop jointly 16Mb DRAM production technology. The agreement gives each company access to the other's 16Mb CMOS DRAM technology. A special panel will be formed to handle intellectual property issues. The agreement represents a cost-sharing and risk-sharing strategy for the two companies to remain competitive in the capital-intensive DRAM business. Hitachi has had problems with its modified trench planar capacitor process for 1Mb DRAMs, and will benefit from TI's trench technology. Hitachi offers excellent manufacturing know-how and 16Mb DRAM device technology.

Microprocessors

Mitsubishi and National

In February 1988, Mitsubishi Electronic began importing National's 32-bit MPUs (32000 Series), software, and development systems under a five-year OEM contract.

Sanyo and VLSI

In April 1988, Sanyo Electric agreed to design, manufacture, and market VLSI Technology's 32-bit ACORN RISC chip (VL86C010) and three peripheral circuits, worldwide. The ACORN chip features 12-MHz clock speed, 6-mips performance, and 2.0-micron geometries (5.5mm square die). The peripheral chips include the VL86C110 memory controller, the VL86C310 video controller, and the VL86C410 I/O controller. Sanyo initially will import and sell VLSI's MPUs, and will jointly develop an MPU for control systems within one year. Both companies will work together in marketing and future product planning. VLSI will market MPUs for data processing equipment, while Sanyo will focus on industrial and home appliance systems.

Toshiba and Zoran

In April 1988, Toshiba and Zoran entered into a technology and manufacturing alliance. Zoran entered into a similar alliance with SGS-Thomson in March 1988.

Sanyo and TI

In April 1988, Sanyo Electric and Texas Instruments (Dallas) announced that they are jointly developing image processors and will complete their project by the end of 1988. TI will manufacture the devices and Sanyo will buy them. This project is part of MITI's program to increase market access for foreign suppliers.

1988 Japanese Alliances

Kawasaki Steel and Tomcat Computer

In May 1988, Kawasaki Steel and Tomcat Computer, a Tokyo-based venture firm, jointly developed a chip set for compatible clones of three major personal computers: NEC's PC9800 series, IBM's PC AT, and Toshiba's J3100 series. The 6-chip set is sampling at ¥50,000 ($400) each for orders of 100 sets. Tomcat is producing and selling the chip set. First-year sales are targeted at ¥1 billion ($8 million).

VM Technology and Mitsui & Co.

In May 1988, Mitsui & Co. became the major shareholder in V.M. Technology Corp., a spinoff of Intel Japan's design center. Headed by Masatoshi Shima, VM Technology is developing 32-bit application-specific MPUs compatible with Intel's IAPX86 architecture from the 16-bit 8086 through the 32-bit 80386. The VM8600S virtual MPUs are based on MS/DOS, but will be compatible with Motorola and Zilog MPU architectures.

Fujitsu, Mizar, and Wind River Systems

In June 1988, Fujitsu teamed up with PCB maker Mizar Inc. (St. Paul, Minnesota) and software house Wind River Systems Inc. (Emeryville, California). They agreed to develop a VME bus board around Fujitsu's 25-MHz standard-cell implementation of the Sun SPARC 32-bit RISC MPU (S-25) for industrial and military systems at the chip, board, and box levels. Mizar will provide VME board-level subsystems using Fujitsu S-25 SPARC CPU. Wind River will build development tools for real-time software and its VxWorks real-time operating system. Sun-3 and Sun-4 will be used as development hosts. Initial board-level VME products are targeted for the fall of 1988. Fujitsu's S-25 RISC MPU features 15-mips throughput and comes in a 179-pin plastic PGA.

Hitachi and Intel

In August 1988, Hitachi issued a large order for MCUs from Intel Japan for use in VCRs, room air conditioners, and other consumer goods. This is part of Hitachi's effort to procure more foreign semiconductors and develop "intelligent" consumer products. In 1987, Intel Japan received a large MCU order from Sanyo for room air conditioners.

Matsushita and Sun Microsystems

In September 1988, Matsushita licensed Sun Microsystem's SPARC RISC chip for use in the workstation being developed by Solbourne Computer, Matsushita's Colorado subsidiary. Solbourne will first use the SPARC processor, then Matsushita's own 64-bit SPARC design in a graphics supercomputer.

1988 Japanese Alliances

Seiko Instruments and Sun Microsystems

In October 1988, Seiko Instruments signed an agreement licensing Sun's RISC Scalable Processor Architecture (SPARC) for use in its own workstations. Seiko also signed a three-year, $50 million contract to market the Sun-3, Sun-4, and Sun3861 workstations for use in graphics applications. Sun has also signed 11 other SPARC licensing agreements.

ASICs

Seiko Epson and S-MOS Systems

In March 1988, Seiko Epson and S-MOS Systems decided to open a joint research center in San Jose, California, to develop ASIC software products. Products include simulation software for S-MOS' compiled cell custom service, which is based on Seiko's BiCMOS process technology. S-MOS has developed the Logic Array Design System (LADS) and recently added Tangent's Tangate layout software for sea-of-gates gate arrays. S-MOS sold products worth $45 million in 1987.

Mitsui & Co. and European Silicon Structures (ES2)

In April 1988, Mitsui & Co. signed a sales agreement to design and market ES2's ASIC devices in Japan. Aimed at niche markets, Mitsui expects its ASIC sales to reach about ¥1 billion ($7.6 million) in the near future. ES2 is a joint venture of six European companies, including Philips, Siemens, and GEC.

Oki Electric and iLSi

In April 1988, Oki Electric signed a technology purchase and licensing agreement with Integrated Logic Systems (iLSi) of Colorado Springs for an undisclosed fee. Oki will manufacture and sell gate arrays based on iLSI technology and provide foundry services. iLSi also has agreements with Motorola, Sumitomo, and Yamaha.

Toshiba and Advanced Silicon

In May 1988, Toshiba signed an agreement to provide 6-inch CMOS wafers for Advanced Silicon Corporation (ASiC)—a Dutch start-up company located in Nijmegen—and to develop jointly ASIC software. ASiC also has agreements with Ricoh for silicon compiler wafer fabrication and European sales, and with Goldstar for design-in and Asian sales.

Fuji Electric and Barvon

In August 1988, Barvon BiCMOS Technology of Milpitas, California, agreed to transfer its standard cell technology to Fuji Electric in exchange for cash and a five-year foundry contract. Fuji will supply Barvon with wafers and access to Fuji's

1.5-micron, double-metal, CMOS process; 2-micron, double-metal, silicon gate BiCMOS process; and CMOS-DMOS process. Barvon will provide its cell library design algorithm and CAD software and its technical and training assistance.

Other Devices

Sony and TI Japan

In April 1988, Sony and TI Japan announced a jointly developed IC filter for digital audio equipment. The "8x over sampling" digital filter is designed to remove noise after enhancing the sampling frequency to more than eight times its original level. The digital filter LSI uses CMOS silicon gate and double-layer wiring processes. Sony is handling standard specification and filter coefficient design, while TI Japan handles LSI design and production. TI Japan will produce the device and supply it to Sony under an OEM arrangement. Sony will sell the device as Model CXD1144AP, sampling at ¥2,875 ($23) per device.

Mitsubishi and National

In April 1988, National Semiconductor consigned Mitsubishi Electric to assemble high-speed TTLs in small outline J-lead (SOJ) packages for the Japanese market. Mitsubishi's assembly plant was set up with Kanebo.

Fujitsu and NEC

In May 1988, Fujitsu and NEC jointly supplied infrared seeker electronics to Kawasaki Heavy for use in an antitank missile system.

Yamaha and Chips & Technologies

In June 1988, Yamaha agreed to exchange LSI technologies with Chips & Technologies of San Jose, California. Plans were also made for future joint R&D.

Hitachi and Mitsubishi

In July 1988, Hitachi and Mitsubishi developed LSI chip sets for use in extended definition TV (EDTV), using common system specifications. Sampling began in August 1988. Hitachi offered two chip sets (HA1154NT/HD49404/5/6) and Mitsubishi offered three chip sets (M50570FP/M50571FP/M52002SP).

Japan Macnics and Honeywell SPT

In August 1988, Japan Macnics entered a sales agency agreement to market Honeywell's A/D and D/A converters in Japan.

Oki Electric and Seattle Silicon

In August 1988, Oki Electric signed a joint agreement with Seattle Silicon to develop a compiler for a process-independent, five-port SRAM module.

NEC and Optoelectronics Research Laboratories

In December 1988, NEC's Compound Semiconductor Device Division and Optoelectronics Research Laboratories announced jointly developed InP/InGaAsP/InGaAs avalanche photodiodes (APD) on InP substrates. Yields and bit error rates were improved by adding a guard-ring structure to the planar heterojunction APDs. The devices will be used in 1.0- to 1.6-micron-wavelength optical communications.

CAD Tools

Seiko Epson and Tangent

In March 1988, Seiko Epson signed a joint technology agreement with Tangent Systems of Santa Clara, California. The agreement covers Tangent's Tangate place-and-route software for laying out sea-of-gates gate arrays. Under the agreement, Tangent will customize its Tangate routing and layout software for use in Seiko Epson fabs and design centers. The initial product will be Seiko's SLA 8000 sea-of-gates series gate arrays, which are being marketed by Seiko Epson's U.S. affiliate, S-MOS Systems.

Kawasaki Steel and SDA Systems

In May 1988, Kawasaki Steel signed two multimillion dollar agreements with SDA Systems of San Jose, California: a three-year technology agreement and a corporate purchase agreement. Kawasaki is already using SDA's front-to-back IC design software tools for designing advanced cell libraries for ASICs. SDA also has agreements with SGS/Thomson, NEC, Fujitsu, Hitachi, Mitsubishi, and Toshiba.

Equipment

Canon, Ishikawajima-Harima, and Ateq

In February 1988, Canon Sales Co. and Ishikawajima-Harima Heavy Industries (IHI) formed a joint venture, ICI Technologies Ltd., with Ateq Corp. of Beaverton, Oregon. The new venture will manufacture Ateq's custom optical reticle engraver, the Core-2000. ICI is capitalized at ¥200 million ($1.5 million), with IHI holding 51 percent and the rest split equally between Canon and Ateq. IHI began construction of ICI's plant in eastern Japan. The facility will cost between ¥500 million and ¥600 million ($3.8 million to $4.6 million) and employ 22 people. ICI will sell Ateq's Core-2000 in the Pacific Rim for 10 years.

1988 Japanese Alliances

Nippon Kokan and Nippon Sanso

In February 1988, Nippon Kokan (NKK), Nippon Sanso, and Professor Tadahiro Ohmi of Tohoku University developed a nickel-chromium-molybdenum stainless steel for making a smooth inner surface for gas piping used in chip making. Called "NK Clean Z-Pipe," its low-hydrogen gas emission level makes it suitable for ultrahigh vacuum equipment applications. NKK, which is diversifying into semiconductors, began sampling in May 1988.

Tokyo Electron, Mentor Japan, and Integrated Measurement Systems

In May 1988, Tokyo Electron (TEL) and Mentor Graphics Japan signed a distribution agreement with Integrated Measurement Systems (IMS) of Beaverton, Oregon. TEL and Mentor will market and sell ISM's line of hardware verification systems in Japan, including Logic Master. IMS previously used Marubeni International as a distributor. In August 1987, Mentor and IMS signed a joint marketing agreement for the United States.

Materials

Nippon Sanso and Linde

In February 1988, Nippon Sanso signed an agreement to supply Linde of West Germany with material gases for semiconductor use. The agreement is for silane gas, arsenide, phosphorous, arsine, and other gases.

Matsushita Electric and Tosoh

In February 1988, Matsushita Electric successfully test manufactured a 16Mb DRAM (a 93.85-square-millimeter chip featuring a 0.5-micron process and 65ns access time). The chip uses a conductive electron-beam resist (CER) jointly developed with Tosoh Corporation, a chemical company. The new resist is made of ammonium polystyrene sulfonate and completely solves the electrification problem that occurs with direct-write e-beam.

NTT and Motorola

In March 1988, Nippon Telegraph and Telephone Corporation and Motorola entered an agreement to research jointly new materials for semiconductors.

Showa Denko and Crystal Specialties

In September 1988, Showa Denko signed a marketing and sales agreement with Crystal Specialties International (CSI) for gallium arsenide (GaAs) products. Under the agreement, CSI (a subsidiary of Akzo Electronic Material Co.) will sell Showa Denko's line of semi-insulating GaAs wafers in the United States. Showa Denko will market CSI's line of semiconducting GaAs wafers in Japan.

1988 Japanese Alliances

Packaging and Interconnect

Sumitomo 3M, Nippon Steel, and Minnesota Mining

In July 1988, Sumitomo 3M, Nippon Steel, and Minnesota Mining & Manufacturing (3M) established a joint venture—Japan Interconnection System—to produce tape automated bonding (TAB) tape starting in mid-1989. Capitalized at ¥240 million ($1.8 million), the new venture is funded 34 percent by Sumitomo 3M, 33 percent by Nippon Steel, and 33 percent by 3M.

Also in July, Sumitomo 3M signed a marketing alliance with Indy Electronics, Mesa Technology Corporation, and Flextronics to market printed circuit boards and subassembly IC products using tape-automated bonding (TAB). The three companies will provide very high pin count ICs on PCBs, following JEDEC standards in TAB. Mesa will supply design services and the tape. Indy will supply the inner lead bonding and encapsulation. Flextronics will handle assembly, final test, and burn-in of the boards.

Agreement Updates

Fujitsu, Hitachi, and Mitsubishi

In January 1988, Fujitsu, Hitachi, and Mitsubishi announced a set of TRON chips: Hitachi's 32-bit GMicro200 MPU with 730,000 transistors, Fujitsu's direct memory access controller and two other peripheral LSIs, and Mitsubishi's peripheral chips. In December 1988, they announced the following 32-bit floating-point coprocessors (FPUs): Fujitsu's MB92811, Hitachi's HD648132, and Mitsubishi's M33281GS.

Toshiba and Tangent Systems

In February 1988, Toshiba and Tangent Systems announced a jointly developed series of three CAD systems for designing gate arrays. The top-of-the-line TC110G can handle 50,000-gate layout and wiring.

Kawasaki Steel and LSI Logic

In June 1988, Nihon Semiconductor, a joint manufacturing venture between Kawasaki Steel and LSI Logic, began producing fully metalized, 6-inch, 1.5-micron, CMOS wafers at its Tsukuba facility for direct shipment to customers. The joint manufacturing plant has a Class 1 clean room. Since the fall of 1987, base wafers have been produced in Japan and shipped to LSI Logic in the United States for full metallization. The Tsukuba facility employs 175 people and has space for further plant expansion.

Toshiba and Motorola

In June 1988, Tohoku Semiconductor, the joint venture between Toshiba and Motorola, announced plans to become operational in July. Wafers for 1Mb DRAMs will be produced and shipped to Toshiba and Motorola for assembly and marketing.

1988 Japanese Alliances

Toshiba, Siemens, and GE

In June 1988, Toshiba introduced new CMOS standard cells (TC24SC Series) using the ADVANCELL ASIC library jointly developed with GE and Siemens. The chips use 1.0-micron design rules. The library consists of 166 primitive logic, 84 I/O, and several macro cells. Orders were accepted in the third quarter of 1988.

Sony and AMD

In September 1988, Sony and AMD began sampling SRAMs developed through an agreement signed in the spring of 1987. Sony developed 35ns, 256K SRAMs and AMD designed 25ns, 64K SRAMs using a common 1.2-micron process.

Hitachi and VLSI Technology

In September 1988, VLSI Technology began marketing Hitachi's SRAMs, including 25ns, 64K (x4) and 35ns, 256K (x4) devices, as part of the Hitachi/VLSI Technology agreement. Both companies are working on faster 256K SRAMs.

Toshiba and Motorola

In October 1988, Toshiba began shipping the 68020 32-bit MPU under the Toshiba brand name. Toshiba received manufacturing rights to the 68020 as well as rights to the 68881 floating-point coprocessor and 68851 paged memory management unit as part of its joint venture—Tohoku Semiconductor—with Motorola. The 68030 and 68040 are not part of the agreement.

Toshiba and VISA International

In December 1988, Toshiba announced a multipurpose IC card for VISA International. The VISA SuperSmart Card features 64K memory, a keypad, a 16-digit display, and built-in battery.

1987 Japanese Semiconductor Alliances

The following table lists Japanese semiconductor alliances completed in 1987. Immediately following the table, the section entitled "Classification of Agreements" defines the type of agreement indicated as a number in the "Type" column of the table.

The text provides a discussion of each alliance listed in the table in the same order as the alliance appears in the table.

1987 Japanese Semiconductor Alliances

Date	Japanese Company	Partner	Type*	Products
		Multiproduct		
05/87	Toko	Telefunken	3	Consumer product ICs
07/87	Teksel	Arrow Electronics	7	U.S. product marketing
08/87	Hitachi	Oklahoma University	8	Products or materials
		Memory		
01/87	Mitsubishi	NTT	8	Rad-hard 64K CMOS SRAM
01/87	Asahi Kasei	ICT	1	EEPROMs
02/87	Mitsubishi	National	4	256K DRAMs
02/87	Hitachi	Kyushu University	8	Bloch-line memory
03/87	Oki Electric	Catalyst	2	16K, 64K CMOS EEPROMs; 256, 512, 1K serial access CMOS EEPROMs
04/87	Seiko Epson	VLSI Technology	4	1Mb mask ROMs
04/87	Hitachi	VLSI Technology	4	1Mb mask ROMs
04/87	Mitsubishi	VLSI Technology	4	1Mb mask ROMs
04/87	Sanyo Electric	VLSI Technology	4	1Mb mask ROMs
05/87	Sharp, Fuji Electric	MOSEL	4	4K to 256K SRAMs, dual-port SRAMs
06/87	New Japan Steel	Simtek	9	IC card EEPROMs
06/87	Fujitsu	Signetics	11	Programmable ROMs
06/87	NEC	ASCII Corp.	8	256K graphic buffers
07/87	Mitsubishi	Intel	4	256K, 512K EPROMs
09/87	Yamaha	Programmable Memory Technology	1	EPROMs for voice ASSPs
12/87	NMB Semiconductor	TI	4	1Mb DRAMs
12/87	NMB Semiconductor	Alliance Semiconductor	4, 6	1Mb CMOS DRAMs

(Continued)

1987 Japanese Semiconductor Alliances

1987 Japanese Semiconductor Alliances (Continued)

Date	Japanese Company	Partner	Type*	Products
		Microprocessors		
01/87	Mitsui & Co.	ASCII Corporation	7	Virtual 32-bit MPUs
01/87	Matsushita	SAE	8	64-bit MPUs
02/87	Rohm	Omron Tateishi	8	MOS DSPs
02/87	Matsushita	Philips	2	8-bit CMOS MCUs
04/87	Canon	National	8	32032/332/532s, MPRs, and software
04/87	Canon	Intel	8	32-bit MPUs for printers
04/87	Matsushita	Intel	1	8051s, plus 3 8-bit MCUs
04/87	Hitachi	Fujitsu	8	32-bit TRON MPUs
05/87	Fujitsu	Intel	8	ASIC MCUs with 16-bit MPUs
07/87	NEC	SMC	2	Peripheral controllers
07/87	Mitsui & Co.	Zoran	9	5 percent investment; DSPs
07/87	Nissan Motors	Intel	8	16-bit MCUs (8096)
07/87	Fujitsu	Sun Microsystems	4, 8	32-bit MPUs
10/87	Fujitsu	Intergraph	4	Clipper chip sets
10/87	Kubota	Mips Computer	9	RISC computers and chips
11/87	NEC	Matra-Harris	2	16-bit single-chip MCUs
11/87	Mitsubishi	National	3	32000 MPUs
12/87	Mitsubishi	National	3	32-bit MPUs and software
12/87	Ricoh	Western Design Center	2	65C816 16-bit MPUs
		ASICs		
01/87	Sharp	Altera/WSI	8	Microsequencers
01/87	Ricoh	Advanced Silicon	4	Custom CMOS ICs
02/87	Rohm	Tateishi Electric	4, 8	Semicustom ICs
03/87	Sanyo/Coinco/ Sanwa Bank	Toyo Info Systems	8	Dictionary IC cards
04/87	Arimura Giken	Citizen Watch	4, 8	IC cards
04/87	Arimura Giken	Yamabuki Honeywell	8	IC cards for FA
04/87	Nippon Chemi-con	Hitachi/Sony	4	ASICs
05/87	Yamaha	Western Design Center	7	Standard cells
06/87	Paradise Systems	Gold Star	4	CMOS gate arrays

(Continued)

1987 Japanese Semiconductor Alliances

1987 Japanese Semiconductor Alliances (Continued)

Date	Japanese Company	Partner	Type*	Products
		ASICs (Continued)		
06/87	Oki Electric	Fuji Bank	8	IC cards
06/87	Nihon (Digital Equipment)	LSI Logic	3	ASICs
06/87	Fujitsu	MMI	11	PLDs
09/87	Sanyo	Computerized Information Technologies	8	IC cards
09/87	Toshiba	Silicon Compiler Systems	4, 6	Genesil, CMOS process
10/87	Okura Trading	Xilinx	3	Logic cell arrays
10/87	Mitsui & Co.	European Silicon Structures	7	Direct-write ASICs
11/87	Toppan Printing	ITT Cannon	8	IC memory cards
12/87	Yamaha	Chips & Technologies	9	Design center
12/87	Yamaha	Integrated Logic Systems	1, 4	Gate arrays for foundries
12/87	Kanematsu Semiconductor	Oak Technology	3	ASICs for IBM PS/2 clones
12/87	ADC	VLSI Technology	3	ASICs marketing
		Other Devices		
01/87	Asahi Kasei	Crystal Semiconductor	4, 9	Smart analog ICs
01/87	Toshiba	China Electronics Trading Corp.	4	Color TV LSIs
01/87	Matsushita	A Chinese company	2	Discretes
01/87	Rikei	Adams-Russell	3	GaAs ICs
01/87	Hitachi	Two Chinese companies	1	Linear IC assembly and test
02/87	Mitsubishi	Omron Tateishi	8	Bipolar linear ICs
03/87	Ricoh	Anam Industrial	5	Custom ICs
04/87	Sony	Triquint Semiconductor	3	GaAs ICs, MMICs
04/87	Toyota	Hamamatsu Photonics	9	Optoelectronics
05/87	Kawasaki Steel	Measurement Specialties	8	Sensors, transducers
05/87	Sony	GE Semiconductor	4	A/D converters
06/87	Matsushita	TRW	8	Semiconductor lasers
06/87	Fuji Electric	Barvon	8	Robotic LSI software
09/87	Tokyo Electron	Int'l Rectifier Japan	4, 8	Hybrid ICs

(Continued)

1987 Japanese Semiconductor Alliances

1987 Japanese Semiconductor Alliances (Continued)

Date	Japanese Company	Partner	Type*	Products
		Other Devices (Continued)		
09/87	NTT, Mitsubishi	Battelle	7	Optoelectronic ICs
10/87	Hitachi	Int'l Rectifier	1	Power MOSFETs
12/87	Sanken	Int'l Rectifier	3, 5	Power MOSFETs
12/87	Shin-Etsu Chemical	Brooktree	9	Image processing
12/87	Mitsubishi	Powerex	3	Discretes
12/87	Sony	National	4	Logic products
12/87	Toshiba	SGS Microelettronica	3	Telecom LSIs
		CAD Tools		
05/87	Toshiba	SDA Systems	8	ASICs CAD software
05/87	Nippon Steel	Sun Microsystems	3	CAD workstations
05/87	Fujitsu Facom	Nippondenso	8	Analog IC CAD systems
06/87	Toshiba	Computervision	7	CAD, CAE, CAM
07/87	Fujitsu	Tektronix	8	Gate array work-stations
09/87	Fujitsu, Hitachi, Mitsubishi, NEC, Toshiba	SDA Systems	2	ASICs CAD software
10/87	TEL	Sun Microsystems	3	CAD OEM agreement
10/87	Seiko Instruments	Tangent Systems	1, 3	CAD software
11/87	Toshiba	Viewlogic Systems	8	PC-based CAE software
11/87	Toshiba, Hitachi	FutureNet	8	Simulation library
11/87	Toshiba	Tangent Systems, Motorola	8	Channelless array CAD
		Equipment		
01/87	Sumitomo Corp.	GCA	9	GCA financing
01/87	Plasma Systems	Ming Shen	8	IC ashers
02/87	Tokyo Electron	KLA Instruments	3	IC testers
02/87	Ulvac	Yasukawa Electric	8	Wafer transfer systems
02/87	Toshiba Ceramics	Quartz Int'l	3	Wafer handling systems
03/87	Matsushita	Nikon	8	VLSI steppers
04/87	Nikon	Taiwan Semi Mfg.	3	Steppers
04/87	Niigata Engineering	Machine Technology	7	Photolithography, dry resist, sputtering, CVD

(Continued)

1987 Japanese Semiconductor Alliances

1987 Japanese Semiconductor Alliances (Continued)

Date	Japanese Company	Partner	Type*	Products
		Equipment (Continued)		
04/87	Mitsui & Co.	Denkoh Co.	9	Vertical oxidation, LPCVD
06/87	Mitsubishi	Cadic	3	Custom LSI testers
08/87	Nippon Kokan	Holon	9	Wafer inspection
08/87	Sumitomo Electric	MITI	8	Compact SOR
09/87	Hitachi	Nanometrics	1	Equipment
09/87	Sumitomo Metal	Lam Research	3	ECR and CVD systems
09/87	NTT Technology	MRC	1	ECR technology
09/87	Kokusai Electric	Leybold-Heraeus	3	Etchers, leak detectors
09/87	Kanematsu Semiconductor	Amaya Mfg.	8	Plasma-enhanced CVD
10/87	Dainippon Screen	MRS Technology	1, 3	Stepper for LCD circuits
11/87	Tokki Corp.	NTT	3	ECR plasma CVD machine
11/87	Nippon Sanso	Spire	3	CVD reactors
12/87	Sumisho Electronics	Silicon Valley Group	3	Vertical CVD
12/87	Kobe Steel	Megatest	7	IC testers
12/87	Mitsui & Co.	Shinko Electric, Denko	7	Diffusion furnaces, CVD
		Materials		
02/87	Nippon Steel	Matsuda Precious Metal	7	Bonding wire
04/87	Toray	MacDermid	4	Photoresist
04/87	Sony	Mitsubishi, Fujitsu	10	Joint package standards
06/87	Nippon Steel	Hitachi	4	Silicon wafers
08/87	NTT	Nippon Steel	8	Superconducting ceramics
09/87	Sumitomo Metals	Spire	3	GaAs epi wafers
09/87	Fuji Photo Film	Olin Hunt	7	1Mb DRAM photoresist
		Agreement Updates		
01/87	Tokyo Sanyo	Vitelic	4	High-speed SRAMs
01/87	Sharp	Wafer Scale Integration	4	64K, 128K, 256K CMOS EPROMs

(Continued)

1987 Japanese Semiconductor Alliances (Continued)

Date	Japanese Company	Partner	Type*	Products
		Agreement Updates (Continued)		
02/87	Sony	AMD	8	Atsugi Technology Center
04/87	Toshiba, NEC, Rohm, Sharp	Zilog	2	Z80
04/87	Seiko	Applied Micro	8	BICMOS logic arrays
04/87	Fujitsu	Intel	8	80186-based ASICs
04/87	Toshiba	Motorola	8	4Mb DRAMs
04/87	Japan Radio	Raytheon	7	Revised 1961 agreement
05/87	Toshiba	Visa International	8	IC cards
05/87	Sony	AMD	8	256K SRAMs
06/87	Kawasaki Steel	LSI Logic	7	ASICs fab
06/87	Fuji Electric	Siemens	7	Power MOSFETS
07/87	Kyocera	Vitelic	9	DRAMs and SRAMs
10/87	Seiko Epson	Siliconix	2	Gate arrays
10/87	Sumitomo Metal	Standard Microsystems	7	Standard cells
11/87	Toshiba/Motorola	Tangent Systems	8	Sea-of-gates CAD system
12/87	NMB	National	8	SRAMs, EPROMs
		Agreements Terminated		
01/87	NMB Semiconductor	Lattice Semiconductor	4	16K, 64K SRAMs
01/87	NMB Semiconductor	Inmos	4	256K DRAMs
02/87	Tokyo Electron	Lam Research	7	Auto dry etchers
02/87	Disco Abrasive Systems	Helmut-Seier	7	Wafer polishers
05/87	Sony	Vitelic	8	256K DRAMs
08/87	Itoh Techno-science	Samsung	3	256K DRAMs
12/87	Hitachi	Motorola	2	CMOS OTP 8-bit MCUs

*See section below entitled "Classification of Agreements."

Source: Dataquest
March 1989

1987 Japanese Semiconductor Alliances

CLASSIFICATION OF AGREEMENTS

Dataquest classifies Japanese strategic alliances into 12 categories:

1. Licensing Agreement: A Japanese company receives a license or issues one to a partner for an up-front fee and/or royalties.

2. Second-Source Agreement: Both companies agree to develop consistent specifications to ensure a second source.

3. Sales Agency Agreement: A Japanese company sells its partner's products, acting either as a sales representative or a value-added reseller (VAR).

4. Fab Agreement: A Japanese company offers fab capacity for its partner's product technology.

5. Assembly and Testing Agreement: A Japanese company sends or receives devices for assembly and/or testing.

6. Technology Exchange: Both companies exchange technology, which may or may not include a transfer of money.

7. Joint Venture: Both companies form a new joint-venture company to develop, manufacture, and market new products.

8. Joint Development: Both companies agree to develop new products jointly, which may or may not be marketed separately.

9. Investment: A Japanese company invests in a partner company (less than 50 percent of its stock) to secure new technology or access to new markets.

10. Coordination of Standards: A Japanese company and its partner agree to device standards to ensure compatibility.

11. Procurement Agreement: A Japanese company agrees to buy more foreign semiconductors as part of a market access program.

12. Other

1987 Japanese Semiconductor Alliances

MULTIPRODUCT

Toko and Telefunken

In May 1987, Toko signed a sales agency contract with Telefunken Electronik of West Germany to import and sell prescaler ICs for TVs and cable TV, ICs for AM/FM radios, and FM ICs for car radios. The sales goal was ¥100 million ($714,290) for the initial year.

Teksel and Arrow Electronics

In July 1987, Teksel and Arrow agreed to establish a joint-venture company in Japan to market U.S.-manufactured semiconductors.

Hitachi and Oklahoma University

In August 1987, Hitachi and Oklahoma University signed an agreement to conduct joint research on high-technology products or materials. Research topics were chosen in the fall.

MEMORY

Mitsubishi and NTT

In January 1987, Mitsubishi Electric and Nippon Telegraph and Telephone Corporation (NTT) announced a jointly developed radiation-hardened 64K full CMOS SRAM for satellite use.

Asahi Kasei and ICT

In January 1987, Asahi Kasei received a license to International CMOS Technology's (ICT's) technology and is marketing ICT EEPROMs.

Mitsubishi and National

In February 1987, Mitsubishi agreed to supply 256K DRAMs to National Semiconductor on an OEM basis. At the time, Mitsubishi was producing 7 million 256K DRAMs monthly at its automated Saijo plant.

1987 Japanese Semiconductor Alliances

Hitachi and Kyushu University

In February 1987, Hitachi and Professor Konishi of Kyushu University announced a jointly fabricated prototype of a Bloch-line memory. Hitachi expects practical applications in 1992 or later.

Oki Electric and Catalyst

In March 1987, Oki Electric signed a mutual second-sourcing agreement with Catalyst Semiconductor of Santa Clara, California. The agreement covers 16K and 64K CMOS EEPROMs and 256-bit, 512-bit, and 1K serial access CMOS EEPROMs, which have been jointly developed. Both firms plan to develop 256K, 512K, and 1Mb serial access CMOS EEPROMs in the future. The serial access EEPROM series are pin-compatible with National Semiconductor and General Instruments. The agreement gives Catalyst access to Oki's wafer fabrication facility, giving Catalyst a production capacity of $100 million a year. It also expands a previous agreement signed in July 1986 to develop nonvolatile memories and a 1K serial EEPROM.

Seiko Epson and VLSI Technology

In April 1987, Seiko Epson agreed to produce mask ROMs, mainly 1Mb devices, for VLSI Technology (VTI) of San Jose, California. VTI also has agreements with Hitachi, Mitsubishi, and Sanyo. VTI plans to source 30 percent of its wafers from outside sources, of which two-thirds will be sourced in the United States.

Fuji Electric, Sharp, and MOSEL

In May 1987, MOS Electronics Corp. (MOSEL) of the United States entrusted Sharp and Fuji Electric with production of 4K to 256K SRAMs and dual-port SRAMs. MOSEL's sole Japanese agent, Teksel, markets the products. Sales in the initial year were targeted at ¥100 ($0.72 million) to ¥200 million ($1.44 million).

New Japan Steel and Simtek

In June 1987, New Japan Steel invested $2 million (a 25 percent share) in Simtek, a Colorado Springs, Colorado, start-up company, to acquire pulse-current EEPROM technology for the rapidly growing IC card market. New Japan Steel plans to import EEPROMs. Simtek, formed in January 1986, is a spinoff from Texas Instruments. The company planned to complete a plant in 1987 and began operations in 1988. New Japan Steel has an overall corporate sales goal of ¥4 trillion ($26.7 billion) in 1995, of which ¥800 billion ($5.3 billion) will be electronics and data communications products. The company is planning silicon wafer production and joint ventures with U.S. superminicomputer makers.

1987 Japanese Semiconductor Alliances

Sanyo, Seiko Epson, Hitachi, Mitsubishi, and VLSI Technology

In April 1987, VLSI Technology announced plans to source 1Mb mask ROM wafers from Hitachi, Mitsubishi, Sanyo, and Seiko Epson.

Fujitsu and Signetics

In June 1987, Fujitsu agreed to expand purchases of Signetics' programmable ROMs for its computer group. The decision was made to meet MITI's request for greater market access by foreign makers.

NEC and ASCII Corp.

In June 1987, NEC and ASCII Corp. announced a jointly developed 256K triple-port graphic buffer. The new chip features a 32Kx8 MOS DRAM, 256 logic circuits, and a 128x8 register.

Mitsubishi and Intel

In July 1987, Intel contracted Mitsubishi to produce 256K and 512K EPROMs from August 1987 due to earlier yield problems at Intel. Mitsubishi supplied 200ns and 250ns CMOS parts from its Kumamoto plant, and began shipping approximately 200,000 to 300,000 pieces monthly of its 2 million to 3 million monthly EPROM production. Intel currently receives 8-bit MCUs (8051) from Mitsubishi and 8- and 16-bit MCUs from Sanyo.

Yamaha and Programmable Memory Technology

In September 1987, Programmable Memory Technology of San Jose, California, licensed its EPROM technology to Yamaha, which planned to use it for application-specific standard products (ASSPs) featuring voice and image functions.

NMB Semiconductor and Texas Instruments

In December 1987, NMB Semiconductor entered a one-year fab agreement with Texas Instruments (TI) to produce TI-designed 1Mb DRAMs. NMB supplied 100,000 units per month, which increased to 1 million in March 1988. TI markets the DRAMs in Japan and the United States. The contract is renewed automatically unless either party seeks cancellation.

NMB Semiconductor and Alliance

In December 1987, NMB Semiconductor and Alliance Semiconductor, a DRAM design start-up in San Jose, California, signed a five-year technology exchange. Alliance will provide its family of 1Mb CMOS DRAMs (x1 and x4) with 60ns, 70ns, and 80ns access times, as well as 256K DRAMs. NMB started providing wafers in the second quarter of 1988. Both companies have rights to market the DRAMs independently worldwide.

MICROPROCESSORS

Mitsui & Co. and ASCII Corporation

In January 1987, Mitsui & Co. and ASCII Corporation established a joint venture, VM Technology Corporation, to develop virtual MPUs for use in automobiles, word processors, copy machines, and other products. Annual sales in 1989 are targeted at ¥5 billion ($30.9 million).

Matsushita and SAE

In January 1987, Matsushita Electric announced plans to develop a 64-bit MPU and 64-bit engineering workstation with Solutions are Everything, Inc. (SAE), of Dover, Delaware. Development began in October 1986. The 2.5cm-square MPU will have a 10-mips processing speed and 50-MHz clock frequency.

In December 1987, Matsushita entered the superminicomputer market using SAE's 64-bit MPU. Under the agreement, Matsushita acquired 52 percent of SAE's share and holds management rights, handles superminicomputer production, and holds exclusive sales rights in Japan. Both companies are marketing the product separately. Matsushita reportedly provided $10 million to SAE for joint development of the MPU. SAE was founded in August 1986 by Doug MacGregor, a former Motorola engineer who worked on the MC68010/20.

Rohm and Omron Tateishi

In February 1987, Rohm and Omron Tateishi Electronics formed a partnership in which Tateishi develops MOS ICs for digital signal processing (DSP) using Rohm's technical assistance. Rohm produces the parts. In a separate agreement, Tateishi received bipolar IC design and manufacturing technology from Mitsubishi Electric.

1987 Japanese Semiconductor Alliances

Matsushita and Philips

In February 1987, Matsushita Electronic Corp. (a subsidiary of Matsushita Electronic Industries) signed an alternate sourcing agreement with Philips to jointly manufacture and market the PCF84CXX family of 8-bit CMOS MCUs. The CMOS MCU family features on-board IIC bus serial communication interface and is a worldwide standard for TV receivers, CD players, car radios, and electronic appliances. Philips' Swiss subsidiary, Faselec, will supply the very high-density, low-power CMOS process. Two 28-pin families are covered by the agreement: the PCF84C21 with 2KB ROM and 64-byte RAM, and the PCF84C41 with 4KB ROM and 128-byte RAM. Matsushita, Philips, and Signetics (Philips' U.S. affiliate) have rights to market the devices worldwide. Matsushita began supplying samples in early 1987. Philips is accepting ROM codes.

Canon and National

In April 1987, Canon signed a letter of intent for joint development and specifications definition of the 32032, 32332, 32532, peripherals, and associated software for Canon products, beginning with a laser printer. Canon is using standard National products, but work with National to upgrade software and peripheral circuits for graphic applications. National will produce the 32-bit MPUs. Canon is also working with Energy Conversion Devices (amorphous metals), National Semiconductor (MPUs and software for office machines), Motorola (MPUs for autofocus single lens reflex camera EOS), and Texas Instruments (CCD purchases for still video cameras).

Canon and Intel

In April 1987, Canon agreed with Intel to jointly develop ASICs (80C531) with 8-bit MCU (MCS-51) and other specialized LSIs for copiers and printers. Production consigned to Intel and shipped to Canon at a yearly rate of 10,000 units. Canon is also jointly developing chips with National Semiconductor; Canon raised its purchases of foreign semiconductors to 28 percent in 1987.

Matsushita and Intel

In April 1987, Matsushita Electronics obtained a license from Intel to manufacture four single-chip 8-bit MCUs, including the 8051.

Hitachi and Fujitsu

In April 1987, Hitachi and Fujitsu announced plans to develop two TRON chips by the end of 1987: the 10-mips HF32/200 and the 20-mips HF32/300. Mitsubishi is also participating with the two firms. The chips were announced in January 1988.

1987 Japanese Semiconductor Alliances

Fujitsu and Intel

In May 1987, Fujitsu and Intel Japan announced a jointly developed ASIC microcontroller with a built-in 16-bit MPU (80186). Intel is producing the device for Fujitsu at an annual rate of 100,000 units. The model features low power consumption for office automation use.

NEC and Standard Microsystems

In July 1987, NEC and Standard Microsystems (SMC) of Hauppauge, New York, signed a technology agreement whereby SMC was to second source two NEC NMOS peripheral LSIs: the MuPD7260 hard/floppy disk controllers and the MuPD7262 Enhanced Small Device Interface (ESDI) hard disk controller. NEC is supplying SMIC with circuit data bases, pattern generation tapes, logic and circuit schematics, and test programs. Both companies signed a similar agreement in 1982 for four MCU peripheral LSIs.

Mitsui and Zoran

In July 1987, Mitsui & Co. acquired a 5 percent stake in Zoran of Santa Clara, California, to import Zoran DSPs, for image processing equipment. Mitsui's investment represented $1.5 million of Zoran's $27 million fund raising. Mitsui jointly formed a sales company in the second quarter of 1988 and currently is sampling Zoran chips to seven or eight Japanese customers. The market for Zoran chips is estimated at ¥10 billion ($66 million) for use in computer graphics, telecommunications, measuring instruments, computer axial tomography (CAT) scanners, and other fast-growing image processing applications.

Nissan Motors and Intel

In July 1987, Nissan Motors and Intel announced a jointly developed 16-bit MCU for engine controls. Nissan plans to introduce Intel's 8096 into its 2,000cc-class cars in 1989 or 1990 and to use Japanese 16-bit MCUs in later models. The 8096 device is currently undergoing evaluation.

Fujitsu and Sun Microsystems

In July 1987, Fujitsu announced a 32-bit RISC MPU (SPARC) jointly developed with Sun Microsystems. Fujitsu is manufacturing the SPARC MPU, which drives the Sun-4 workstation being produced under license from Sun. Sun has also licensed SPARC to Cypress and Bipolar Integrated Technology, and is working with Nippon Steel on CAD systems.

1987 Japanese Semiconductor Alliances

Fujitsu and Intergraph

In October 1987, Intergraph acquired Fairchild's Clipper operations and continued Fairchild's agreement to source wafers from Fujitsu for the Clipper set, which was originally signed in October 1986.

Kubota and Mips Computer

In October 1987, Kubota Ltd. invested $25 million, or 20 percent equity share, in Mips Computer Systems Inc. Kubota received exclusive rights to manufacture future Mips RISC computers and MPUs that were under development, and exclusive marketing rights for Mips products in Asia. Kubota plans to build a facility to manufacture RISC MPUs, while Mips Computer focuses on its system business.

NEC and Matra-Harris

In November 1987, NEC and Matra-Harris Semiconducteurs S.A. entered a second-sourcing agreement in which NEC supplied 16-bit, single-chip MCU technology. Matra-Harris produced two models (MuPD78312 and MuPD78310) and marketed them worldwide.

Mitsubishi and National

In November 1987, Mitsubishi agreed to sell National Semiconductor's 32000 MPUs, peripherals, and support tools under Mitsubishi's own label. National hopes that the Mitsubishi connection will open the door for embedded control design wins in Japan.

Mitsubishi and National

In December 1987, Mitsubishi Electric and National Semiconductor signed a five-year OEM contract regarding National's 32-bit MPUs, MPRs, and support software tools. Under the contract, Mitsubishi is importing National's 32000 series for reselling into the Japanese market. National also worked with Canon on a 32532 optimized for laser printer controls, and recently signed an ASIC joint venture with Sierra Semiconductor and Singapore Technology Corp. to form Chartered Semiconductor Pte. Ltd.

Ricoh and Western Design Center

In December 1987, Ricoh signed a second sourcing agreement with Western Design Center (WDC) to produce and market WDC's 65C816 16-bit MPU. Ricoh also accepts orders for standard cell products incorporating the MPU, a CMOS device with 8-MHz clock frequency and 16-bit internal/external buses using a 1.5-micron design

rule. Ricoh is incorporating the MPU as a standard cell device for image processing, voice processing, office automation systems, robots, and numerical controllers, but has no plans to sell the device as an independent MPU. Ricoh is the first Japanese company to use 16-bit MPUs in standard cell chips.

ASICs

Sharp, Altera, and Wafer Scale Integration

In January 1987, Sharp, Altera, and Wafer Scale Integration (WSI) agreed to codevelop a family of standalone microsequencer products with wafers manufactured by Sharp.

Ricoh and Advanced Silicon

In January 1987, Advanced Silicon, of the Netherlands, consigned Ricoh to produce custom CMOS ICs using the Dutch firm's designs. The five-year foundry agreement is focusing on CMOS parts using a 2.0-micron process, with Ricoh producing 1.2-micron products later. Advanced Silicon has branch offices in the United Kingdom, West Germany, and France.

Rohm and Tateishi Electric

In February 1987, Rohm and Tateishi Electric agreed to cooperate in producing semicustom ICs. Tateishi consigned Rohm to produce semicustom MOS ICs using Rohm technology. Devices are initially used in Tateishi equipment, then sold commercially. Earlier, Tateishi received bipolar technology from Mitsubishi Electric.

Sanyo, Coinco, Sanwa Bank, and Toyo Information Systems

In March 1987, the Japan Electronic Publishing Co., a joint venture of Sanyo Electric, Coinco, and Toyo Information Systems, introduced two 25,000-word IC card dictionaries. There are two versions: a card with 4MB memory (¥7,000/$46.67) and another with 1GB memory ($4,800/$32.00). Company ownership includes Toyo Information Systems (20 percent), Sanwa Bank Venture Capital (15 percent), Sanyo Electric (15 percent), Japan Coinco (15 percent), Toyo Information Systems (15 percent), and others (20 percent).

Also in March 1987, Sanyo established the Sanyo VLSI Engineering Company capitalized at ¥400 million ($3.1 million) to conduct joint research and technology exchanges with foreign semiconductor makers.

1987 Japanese Semiconductor Alliances

Arimura Giken and Citizen Watch

In April 1987, Arimura Giken announced an ISO-compatible IC card priced at less than ¥2,000 ($13.30) using 16K EEPROMs from Hitachi and 4K EEPROMs from a U.S. maker. Arimura is manufacturing and selling IC cards in cooperation with Citizen Watch.

Arimura Giken and Yamabuki Honeywell

In April 1987, Arimura and Yamabuki Honeywell announced a joint venture capitalized at ¥156 million ($1.04 million) to develop IC cards for factory automation (FA) systems. Yamabuki is purchasing Arimura IC cards and also marketing them.

Nippon Chemi-con, Sony, and Hitachi

In April 1987, Nippon Chemi-con, a Tokyo manufacturer of aluminum foil electrolytic fixed capacitors, entered the ASIC business. The ASICs were to be produced by Hitachi and Sony. Nippon Chemi-con also sells Hitachi and Sony standard ICs.

Yamaha and Western Design Center

In May 1987, Nippon Gakki (Yamaha) established a partnership with Western Design Center of the United States to strengthen its standard cell business. Yamaha already has introduced Western Design's circuit design technology and developed an IC with a built-in 8-bit MPU (65C02). Yamaha is exporting standard cell ICs, mainly to the United States.

Paradise Systems and Gold Star

In June 1987, Gold Star Semiconductor signed a $1 million contract to supply Paradise Systems with high-speed CMOS gate arrays. Shipments began in July 1987. In 1985, Gold Star signed a second-sourcing agreement with LSI Logic for CMOS gate arrays (7000 Series).

Oki Electric and Fuji Bank

In June 1987, Oki Electric and Fuji Bank jointly developed a new type of IC card, the "visual card," which can be used as a calculator, bankbook/cash card, prepaid card, and credit card. The card is equipped with a solar cell and liquid crystal display. Fuji Bank plans to test the card in Tokyo and commercialize it in fiscal 1990.

1987 Japanese Semiconductor Alliances

Nihon Digital Equipment Corporation and LSI Logic

In June 1987, Nihon Digital Equipment Corp. and LSI Logic announced a cooperative ASIC marketing agreement. Both companies are marketing and providing application support for ASICs using LSI Logic's design system and Digital's VAX minicomputers.

Fujitsu and Monolithic Memories

In June 1987, Fujitsu agreed to purchase more programmable logic devices (PLDs) from Monolithic Memories (MMI) in response to MITI's request for expanded purchases of foreign semiconductors. Under the agreement, Fujitsu aimed at increasing its purchases to ¥200 million ($1.4 million), up tenfold from 1986.

Sanyo and Computerized Information Technologies

In September 1987, Computerized Information Technologies of New York City introduced the credit-card size Manhattan City Key calculator using a Sanyo IC. The $20 to $30 card provides the exact location of various New York City addresses. Cards are sold at Bloomingdale's, Fortunoff, and city boutiques. A local radio program gives away City Keys as prizes.

Toshiba and Silicon Compiler Systems

In September 1987, Toshiba entered an agreement with Silicon Compiler Systems Corp. (SCS) under which Toshiba is providing foundry services for chips using SCS's Genesil IC design system. Toshiba is providing the 1.5-micron CMOS process. Toshiba is SCS's second foundry after Ricoh.

Okura Trading Company and Xilinx

In October 1987, Okura Trading Company signed a sales agency agreement to sell Xilinx's new logic cell array series (XC3000) in Japan. The new series features 2,000 to 9,000 gates using a 1.2-micron CMOS, 2-layer metal process. Xilinx currently sells its XC200 (1,200 and 1,800 gates). Xilinx is jointly developing CMOS programmable gate arrays with Seiko Epson.

Mitsui & Co. and European Silicon Structures

In October 1987, Mitsui & Co. and European Silicon Structures (ES2) formed a partnership that purchased a software and design company called Best to market ES2's products in Japan. ES2 was formed in 1985 to offer fast-turnaround IC-prototyping service using direct-write wafer fab equipment (Perkin-Elmer's Aeble 150); it is

expanding into the United States and Japan. ES2 is offering a 2-micron, 2-layer metal process, and 2 poly layers for advanced analog ASICs. A 1.0-micron process is planned for 1989. Prototyping is done at the Rousset plant in France.

Toppan Printing and ITT Cannon

In November 1987, Toppan Printing and ITT Cannon (Fountain Valley, California) announced plans for joint development of IC memory cards to be called the ITT Cannon STAR Card for use as an alternative to floppy disks, memory cartridges, and internal system memory chips.

Yamaha and Chips & Technologies

In December 1987, Yamaha spun off its semiconductor division at Buena Park, California, and established a development and design firm in the Silicon Valley. Chips & Technologies of San Jose, California, in which Yamaha has a capital interest, is cooperating with Yamaha in marketing semiconductors in the United States. Production will be handled by Yamaha Kagoshima Semiconductor, which was founded in April 1987.

Yamaha and Integrated Logic Systems

In December 1987, Yamaha purchased a license for Integrated Logic Systems' (iLSi's) gate arrays in exchange for royalties and foundry services. iLSI, based in Colorado Springs, Colorado, was formed in August 1983 and specializes in silicon-gate CMOS and software-based design aids. iLSI also has agreements with Motorola, Sumitomo Corporation, and Oki Electric.

Kanematsu Semiconductor and Oak Technology

In December 1987, Kanematsu Semiconductor was named Japanese sales agent of Oak Technology Inc. of Santa Clara, California, to sell Oak's ASICs for IBM PS/2-compatible computers. Kanematsu is also selling BIOS software. VLSI Technology is handling initial chip production.

ADC and VLSI Technology

In December 1987, ADC (a subsidiary of Nippon Chemical Condenser Company) signed an agreement to market VLSI Technology's ASICs in Japan.

OTHER DEVICES

Asahi Kasei and Crystal Semiconductor

In January 1987, Asahi Chemical acquired an 8 percent share in Crystal for about $4 million. Asahi Kasei is manufacturing and marketing Crystal's smart analog IC devices for the Asian market.

Toshiba and China Electronics Trading Corporation

In January 1987, Toshiba agreed to supply TV signal processing ICs and assembly equipment to the China Electronics Trading Corporation under the direct control of the Chinese Ministry of Electronics Industry. The agreement is being reviewed by the Paris-based Coordinating Committee for Export Control (COCOM) for compliance with western defense policies. An LSI assembly with test plant is in Wuxi City, Jiangsu Province, with plans to produce 6 million 4-bit TV signal processors (PAL method) annually.

Matsushita and a Chinese Company

In January 1987, Matsushita Electronics offered discrete semiconductor manufacturing technology and related facilities to an undisclosed Chinese corporation in Dandong, Liaoning Province. Under the ¥400 million ($2.9 million) contract, Matsushita will train 25 Chinese technicians and engineers.

Rikei and Adams-Russell

In January 1987, Rikei Corporation, a Japanese electronics trading company, signed a sales agency contract with Adams-Russell, a U.S. high-frequency semiconductor and application equipment maker in Massachusetts, to sell Adams-Russell's GaAs ICs.

Hitachi and Two Chinese Companies

In January 1987, Hitachi reached a basic five-year agreement with the Chinese government to license its linear IC assembly and testing technology to two companies in Shanghai. The ¥2 billion to ¥3 billion ($14.3 million to $21.4 million) contract must be approved by COCOM.

Mitsubishi Electric and Omron Tateishi

In February 1987, Mitsubishi Electric and Omron Tateishi established a partnership under which Mitsubishi is providing bipolar linear IC design and manufacturing technology for five years. Omron began production in April 1987 at its Mizuguchi Plant

in Shiga Prefecture, beginning with assembly of linear ICs supplied by Mitsubishi's Fukuoka Works. Production in the first year was targeted at ¥500 million ($3.3 million). In phase two, Omron plans to build a ¥5 billion ($33 million) bipolar wafer processing line at the Mizuguchi plant.

Ricoh and Anam

In March 1987, Ricoh entrusted Anam Industrial Co. of South Korea for final custom IC assembly to reduce production costs. Ricoh plans to assign custom IC fabrication to a major semiconductor maker.

Sony and Triquint Semiconductor

In April 1987, Sony agreed to market GaAs ICs produced by Triquint Semiconductor of Beaverton, Oregon, in Japan. Under the agreement, Sony will market 2-GHz GaAs dividers, 2Gb-per-second multiplexer logic ICs, and monolithic microwave ICs (MMICs); take standard cell orders; and provide foundry services. Triquint is a spinoff of Tektronix.

Toyota and Hamamatsu Photonics

In April 1987, Toyota acquired 2 million shares of Hamamatsu Photonics stock for ¥3.8 billion ($29.8 million), making Toyota the second largest shareholder with 8.1 percent stock ownership. By working with Hamamatsu, Toyota plans to enter the optoelectronics field. Hamamatsu is conducting joint optoelectronics research with NTT and Battelle. Toyota is building a new IC plant.

Kawasaki Steel and Measurement Specialties

In May 1987, Kawasaki Steel and Measurement Specialties announced plans to jointly develop sensors and transducers.

Sony and GE Semiconductor

In May 1987, GE Semiconductor's Datel Division began shipment of high-speed A/D converter ICs in the Japanese market. The models (ADC310/303) are supplied by Sony under an OEM agreement.

Matsushita and TRW

In June 1987, Matsushita Electronics and TRW agreed to jointly develop a 0.8-micron wavelength GaAlAs semiconductor laser for space communications for the U.S. National Aeronautics and Space Administration (NASA). Matsushita is now

manufacturing high-powered lasers for installation in TRW machines. NASA plans to introduce a Matsushita 80mW device in 1990. Matsushita is currently supplying semiconductor lasers to Philips for CD players.

Fuji Electric and Barvon

In June 1987, Fuji Electric and Barvon CMOS Technology announced plans to jointly develop software for Fuji's multipurpose LSI for use in robotics. Fuji is selling the LSIs in Japan, and Barvon is handling U.S. sales.

Tokyo Electron and International Rectifier Japan

In September 1987, Tokyo Electron (TEL) and International Rectifier Japan (IRJ) signed an agreement under which TEL is handling circuit design and sales, and IRJ is manufacturing hybrid ICs. The first product is for switching power supplies.

NTT, Mitsubishi, and Battelle

In September 1987, NTT, Mitsubishi, and Battelle Memorial Institute of Columbus, Ohio, established a new optoelectronic IC company, Photonic Integration Research, located at Battelle Institute. The venture is owned 49 percent by NTT, 41 percent by Mitsubishi, and 10 percent by Battelle. President T. Miyashita comes from NTT's Ibaraki Telecommunication Labs' Optical Material Research Lab.

Hitachi and International Rectifier Corp.

In October 1987, International Rectifier Corp. announced a worldwide licensing agreement with Hitachi. International Rectifier is producing MOSFETs at HEXFET America in Riverside, California.

Sanken and International Rectifier Corp.

In December 1987, Sanken Electric and International Rectifier signed an agreement whereby Sanken is packaging and marketing International Rectifier's HEXFET power MOSFETs.

Shin-Etsu Chemical and Brooktree

In December 1987, Shin-Etsu Chemical invested $2 million in Brooktree, a San Diego, California, semiconductor start-up formed in 1981 to develop computer graphics and image processing. Brooktree specializes in D/A, A/D, and mixed-signal data converters. In 1985, Brooktree licensed its technology to Toshiba for consumer digital audio applications, and, in 1986, to Fairchild to develop standard cells.

In a related development, Shintech, the U.S. subsidiary of Shin-Etsu Chemical, acquired a $1 million stake in Ventana Holdings, a San Diego, California, venture capital company, to finance start-ups in biotechnology and electronic materials. Shintech specializes in vinyl chloride resins.

Mitsubishi and Powerex

In December 1987, Mitsubishi Electric began importing discrete devices from Powerex of Youngwood, Pennsylvania, a joint venture between Mitsubishi, Westinghouse, and General Electric.

Sony and National

In December 1987, National entrusted Sony's Nagasaki plant with logic production. Sony recently purchased the Nagasaki plant from Fairchild Japan after National acquired Fairchild Semiconductor. This production agreement, National's first with a Japanese maker, will be expanded to other devices in the future.

Toshiba and SGS Microelettronica

In December 1987, Toshiba agreed to import telecommunication LSIs from SGS Microelettronica for sale in the Japanese market. Toshiba is altering the specifications of the imported LSIs to meet local needs.

CAD TOOLS

Toshiba and SDA Systems

In May 1987, Toshiba and SDA Systems of San Jose, California, formed a five-year technology partnership with Innovative Silicon Technology (IST), an affiliate of SGS, to develop next-generation ASICs circuit-design CAD software. Toshiba, which is paying several million dollars to SDA, is using SDA's CAD software in its VL-CAD system, customizing the Sun-based software, and offering the package to its ASIC customers. SDA is marketing jointly developed products. Toshiba's ¥23 billion ($177 million) Semiconductor System Technology Center in Kawasaki, which has 1,000 workstations and 1,800 designers, serves as headquarters for Toshiba's 10 worldwide design centers.

SDA received equity financing from GE, Harris, L.M. Ericsson, and National. In 1986, SDA signed an $8 million contract to develop ASIC software for Harris. Toshiba also has alliances with LSI Logic and Sun Microsystems.

1987 Japanese Semiconductor Alliances

Nippon Steel and Sun Microsystems

In May 1987, Nippon Steel agreed to market Sun Microsystems engineering workstations on an OEM basis through Concurrent Nippon, a joint venture of Concurrent Computer and Nippon Steel, in order to diversify and expand its product line to super- and personal computers. Sun sold 340 units in 1985 and 940 units in 1986 through Nihon Sun Microsystems K.K. Nippon Steel is loading Sun-3 workstations with software developed in-house and by affiliates. Nippon Steel has software for CAD/CAM and AI.

Fujitsu Facom and Nippondenso

In May 1987, Fujitsu Facom Information Processing Corp., a wholly owned subsidiary of Fujitsu and a leading value-added network (VAN) operator, and Nippondenso, a major auto electrical parts affiliate of Toyota Motors, are jointly developing a prototype expert system to design linear/analog ICs. The system, which reduces design time by 90 percent, is used to design ICs for car engine controls, windshield wipers, and other electronic components.

Toshiba and Computervision

In June 1987, Toshiba and Computervision established a joint venture, Computervision Japan (CVJ), to develop and market CAD/CAE/CAM systems based on Computervision's advanced engineering workstations. Capitalized at ¥750 million ($5.8 million), CVJ is owned 66.5 percent by Computervision and 33.5 percent by Toshiba. Toshiba is manufacturing hardware for the Japanese version of Computervision's workstation, while Computervision is adapting software for use in Japanese equipment.

Fujitsu and Tektronix

In July 1987, Fujitsu signed a technical cooperation pact with Tektronix and Sony Tektronix to jointly develop, manufacture, and sell gate array workstations capable of design to layout.

Fujitsu, Hitachi, Mitsubishi, NEC, Toshiba, and SDA Systems

In September 1987, SDA Systems of San Jose, California, sold its chip design software to five Japanese companies. As mentioned earlier, SDA also signed a five-year technology partnership with Toshiba in May.

1987 Japanese Semiconductor Alliances

Tokyo Electron and Sun Microsystems

In October 1987, TEL signed a $10 million OEM agreement with Sun Microsystem's Japanese subsidiary, Nihon Sun Microsystems. Under the three-year contract, TEL integrated Sun-3 and Sun-4 workstations with hardware and software from Celerity, Convex, GenRad, SDRC, and Vicom. TEL is reselling the systems to the electrical and mechanical CAD markets. TEL also sells Sun workstations in Japan as front-end processors for larger systems, such as distributed networked environments, using Sun's Network File System (NFS) to link systems from different computer vendors.

Seiko Instruments and Tangent Systems

In October 1987, Seiko Instruments paid $2.5 million to license software from Tangent Systems of Santa Clara, California, for sales and distribution in Japan. Under the agreement, Seiko bundles Tangent's cell-based design package (Tancell) and Tansure, a timing analysis and timing-driven layout package, with its own proprietary design software (SX-8000), which it sells with Digital Equipment Corporation computers. Seiko's SX-8000 software is aimed at full-custom designers. Seiko is Japan's largest supplier of design automation systems (more than 200 installations) and the largest Digital OEM. Tangent, which is 50 percent owned by Intergraph, ported its software to Apollo Computer systems earlier in 1987 for sales to Japanese users.

Toshiba and Viewlogic Systems

In November 1987, Toshiba chose Viewlogic Systems as its principal source of PC-based CAE software. Viewlogic and Toshiba have jointly developed a new ASIC design kit. Viewlogic features multiwindowing, integration of schematics and simulation, open architecture, and support of Electronic Design Interchange Format (EDIF). Other recent ASIC-CAE alliances include Motorola-FutureNet, National-Data I/O, and FutureNet-NCR-VLSI Technology-Hitachi.

Toshiba, Hitachi, and FutureNet

In November 1987, FutureNet lined up support from Toshiba, Hitachi, NCR, VLSI Technology, and Gould as part of an extensive simulation library support program called Acculib.

Toshiba, Tangent Systems, and Motorola

In November 1987, Tangent Systems of Santa Clara, California, announced channelless array CAE/CAD software tools developed with Motorola and Toshiba. The place-and-route algorithms were developed for Toshiba's sea-of-gates channelless architecture. The new Tangent physical layout tools boost CAD design to 250,000 usable gates. The Tangent n-layer algorithm allows 70 to 80 percent gate utilization of three-layer metal designs. Four- and five-layer metal designs were added in 1988.

Tangent and Motorola entered an OEM arrangement under which Motorola is selling the CAD tools to its customers. Motorola's ASIC division is using Tangate to place and route CMOS, BICMOS, bipolar, and ECL gate arrays, along with new channelless gate arrays. Toshiba is using the Tangate sea-of-gates layout software to place and route its TC110G gate array series with 5,330 to 129,042 gates. Toshiba sold the layout tool with its new high-end gate array line in 1988. Intergraph owns 50 percent interest in Tangent.

EQUIPMENT

Sumitomo Corporation and GCA

In January 1987, Sumitomo Corporation and Matra S.A. invested a total of $24 million in GCA common stock as part of GCA's restructuring program. GCA plans to raise a total of $72 million in equity, of which $48 million of stock was sold to existing shareholders, employees, and institutional investors.

Plasma Systems and Ming Shen

In January 1987, Plasma Systems Corp. signed a technical cooperation agreement with Ming Shen Enterprises Company, Ltd., a Taiwan gas regulator maker, to produce ashers at Ming Shen's Taiwan plant. Ming Shen is capitalized at NT$1 million ($27,000), shared equally between two partners. The first product is the DES-106-254A asher, a compact tabletop machine capable of processing 50 five-inch wafers per cycle. Ninety percent of the products are exported.

Tokyo Electron and KLA Instruments

In February 1987, TEL provided its IC testers to KLA Instruments on an OEM basis. This large-scale export plan marks TEL's first full-fledged entry into the U.S. and European markets.

Ulvac and Yasukawa Electric

In February 1987, Ulvac and Yasukawa Electric announced jointly developed wafer transfer systems featuring magnetic levitation. Ulvac is using these systems in its semiconductor equipment to avoid particulate contamination on silicon wafers.

1987 Japanese Semiconductor Alliances

Toshiba Ceramics and Quartz International

In February 1987, Toshiba Ceramics began marketing automatic wafer handling systems for diffusion furnaces made by Quartz International of Santa Clara, California. Quartz was purchased by Toshiba Ceramics in 1986. Toshiba Ceramics also began R&D on quartz lenses for future wafer stepper applications.

Matsushita and Nikon

In March 1987, Matsushita Electric and Nikon agreed to jointly develop advanced i-line steppers and excimer lasers for next-generation VLSIs. Matsushita has succeeded in using excimer lasers to draw 0.4-micron geometries. Nikon already sells steppers for 4Mb DRAMs and plans to develop a new stepper for 16Mb DRAMs with Matsushita's ¥20 billion ($140 million) Semiconductor R&D Center in Osaka.

Nikon and Taiwan Semiconductor Manufacturing Corp.

In April 1987, Nikon signed an export contract with Taiwan Semiconductor Manufacturing Corp. to increase its stepper exports.

Niigata Engineering and Machine Technology Inc.

In April 1987, Niigata Engineering (Tokyo) and Machine Technology Inc. (MTI) of Parsippany, New Jersey, established a joint venture in Tokyo to manufacture and market semiconductor equipment. Capitalized at ¥160 million ($1.2 million), the venture is owned 50/50 by the two firms. MTI is supplying photolithography, dry photoresist removal, sputtering, and CVD machines. Their sales goal is ¥5 billion ($38 million) yearly by 1990.

Mitsui & Co. and Denkoh Co.

In April 1987, Mitsui & Co. purchased one-third of the stock of Denkoh Co., which makes vertical oxidation and LPCVD systems. Mitsui is entering the semiconductor equipment field aggressively and has established a Tokyo marketing firm, MBK Microtek.

Mitsubishi and Cadic

In June 1987, Mitsubishi Corporation agreed to market Cadic's custom LSI testers through its subsidiary, M.C. Electronics. Cadic's compact desk-type model is used for testing prototypes and custom LSIs in the last stage of the manufacturing process. The three models are priced between ¥2 million ($13,333) and ¥48 million ($320,000).

1987 Japanese Semiconductor Alliances

Nippon Kokan and Holon

In August 1987, Nippon Kokan (NKK) invested capital in Holon Co., a maker of semiconductor wafer inspection equipment established in 1985. NKK entered the testing equipment market, providing Holon with strong financial, marketing, and personnel support.

Sumitomo Electric and MITI

In August 1987, Sumitomo Electric Industries and MITI's Agency of Industrial Science and Technology announced plans to jointly build a small synchrotron orbital radiation (SOR) machine using superconductors. The Rainbow No. 2 machine has an overall diameter of 3 meters and weighs 20 tons. A completed prototype began test operations in Sumitomo's Tokyo plant. MITI and Sumitomo will produce compact SOR machines in volume so that semiconductor makers can purchase them for their plants.

In April 1988, Sumitomo Heavy began building SOR equipment for its opto technology research building in Tanashi, Tokyo. Equipment costs will reach ¥1 billion to ¥2 billion ($6.8 million to $13.7 million). Experimentation began in 1988.

Hitachi and Nanometrics

In September 1987, Hitachi paid Nanometrics of Sunnyvale, California, $750,000 to use some of its patented technology. Nanometrics entered the licensing agreement to offset a string of quarterly losses.

Sumitomo Metal and Lam Research

In September 1987, Sumitomo Metal signed an exclusive sales agency agreement to import Lam Research's Rainbow plasma etching systems into Japan. In exchange, Lam is marketing Sumitomo Metal's electron cyclotron resonance (ECR) and CVD systems, which were licensed from NTT Technology in North America and Europe in mid-1988. Sumitomo and Lam are planning future joint R&D. Currently, Lam is second in revenue after Applied Materials/TEL, which sold 180 units in Japan during the last six years. No U.S. companies have active ECR programs. In Japan, NTT makes ECR systems for internal use; other Japanese licensees are said to include Anelva, Hitachi, Mitsubishi, and Tokyo Ohka.

NTT Technology and MRC

In September 1987, Materials Research Corp. (MRC) beat Lam Research by entering a technology transfer agreement with NTT Technology, which has developed ECR technology. MRC is licensed to build ECR etch and CVD systems, improve the technology, and sell the systems worldwide. MRC plans to develop a working CVD model

at its advanced lab in Pearl River, New York, and build the machine at its Congers, New York, plant. Dr. Dennis M. Manos, formerly of Princeton's Plasma Physics Lab, is head of ECR research. Mitsubishi, a 25 percent owner of MRC Japan, helped arrange the MRC–NTT deal.

Kokusai Electric and Leybold–Heraeus

In September 1987, Kokusai Electric entered a mutual marketing agreement with Leybold–Heraeus GmbH of West Germany. Kokusai is marketing Leybold's helium–leak detectors in Japan, while Leybold is selling Kokusai's etching equipment in Europe. The association is expanding to other areas.

Kanematsu Semiconductor and Amaya

In September 1987, Kanematsu Semiconductor and Amaya Manufacturing announced a jointly developed plasma–enhanced CVD system (PEC 6000).

Dainippon Screen and MRS Technology

In October 1987, Dainippon Screen Mfg. announced a licensing/sales agency agreement with MRS Technology of the United States to sell MRS steppers for writing circuits for LCD applications. Dainippon injected capital in exchange for licensing rights. The stepper can etch circuits on a 450mm–square chip, double the area of conventional machines, and 1.5 to 2 times faster. Dainippon initially priced the units at ¥200 million each ($1.48 million).

Tokki Corporation and NTT

In November 1987, Tokki Corporation, a factory automation equipment maker, began selling an ECR plasma CVD machine developed using technology from NTT. The machine was initially priced between ¥40 million ($28,000) and ¥100 million ($69,000).

Nippon Sanso and Spire

In November 1987, Nippon Sanso signed a three–year distribution agreement to sell Spire's metal organic CVD (MOCVD) reactors in Japan, with an option to renew. Special emphasisis is being placed on the Model 450, which can handle 5 two– or three–inch wafers per run, and the Model 1000, which can process 20 two–inch wafers or 10 three–inch wafers per run. Sanso, which has been in the MOCVD business since 1982, has ordered 450 reactors for demonstration purposes and provides technical assistance and after–sales service. An R&D center in Kawasaki is being planned. Spire is already selling GaAs wafers in Japan through Sumitomo.

Sumisho Electronics and Silicon Valley Group

In December 1987, Sumisho Electronics signed a sales agency contract with the Silicon Valley Group (SVG) of San Jose, California, to market SVG's vertical thermal reactors in Japan. The equipment was priced between ¥50 million ($37,000) and ¥60 million ($44,000).

Kobe Steel and Megatest

In December 1987, Kobe Steel and Megatest established a joint venture to import IC testing equipment and obtain testing business in Japan. Named Genesis Technology Inc., this venture is capitalized at ¥100 million ($833,000), owned 37.5 percent by Megatest, 32.5 percent by Kobe Steel, 25 percent by Megatest's Japanese exclusive agent, and 5 percent by Shinko Electric, an affiliate of Kobe Steel. Genesis is headquartered in Tokorozawa, Saitama Prefecture. Megatest plans to manufacture testing equipment in Japan within several years for export.

Mitsui & Co., Shinko Electric, and Denko

In December 1987, Mitsui & Co., a trading company), Denko, a small semiconductor equipment company, and Shinko Electric, a heavy electric company, formed a joint venture, Denko Systems, to make vertical–type diffusion furnaces and CVD systems.

MATERIALS

Nippon Steel and Matsuda Precious Metal

In February 1987, Nippon Steel and Matsuda Precious Metal established a joint venture, Nittetsu Micro Metal K.K., to enter the bonding wire/vapor wire business. Capitalized at ¥250 million ($1.62 million), the company is owned 70 percent by Nippon Steel and 30 percent by Matsuda Precious Metal. Production is done at Matsuda Metal's existing factory.

Toray and MacDermid

In April 1987, Toray Industries entered a technical agreement to manufacture the PR900 Series positive photoresists for the United States–based company, MacDermid. The photoresist is a novolac–based positive UV photoresist suitable for 0.6–micron design rules for 4Mb DRAMs. MacDermid has been manufacturing positive photoresists since 1981. Toray will handle production and marketing, and will conduct joint R&D with MacDermid in the future. Toray plans to build a plant within two years and aims at ¥4 billion ($26.7 million) in four years.

1987 Japanese Semiconductor Alliances

Fujitsu, Mitsubishi, and Sony

In April 1987, Fujitsu, Mitsubishi, and Sony agreed on a unified set of standards for nine kinds of small IC packages, including four very small outline packages (VSOP) and five very small quad flat packages (VQFP). The package standards include a 0.65mm-pitch VSOP, 0.65mm-pitch quad flat package (QFP), and 0.50mm-pitch VQFP with a 1.2mm to 1.4mm thickness. The companies are using emboss taping and the latest mounting systems. The packages are ideal for CD players and camcorders. Sampling began in June 1987.

Nippon Steel and Hitachi

In June 1987, Nippon Steel began shipping silicon wafers to Hitachi, based on Hitachi's evaluation of sample wafers in the fall of 1986. Nippon Steel entered the wafer business through Nittetsu Electronics, which Nippon Steel established in June 1985. Nittetsu's silicon wafer plant was completed in June 1987.

NTT and Nippon Steel

In August 1987, NTT and Nippon Steel began a joint project to research new materials, including superconductive ceramics.

Sumitomo Metals and Spire

In September 1987, Sumitomo Metal and Spire of Bedford, Massachusetts, signed an exclusive marketing agreement to develop the market for GaAs epi wafers in Japan. Spire is growing highly specialized GaAs and AlGaAs epi layers on Sumitomo GaAs substrates. Sumitomo is marketing the wafers to its Japanese customers.

Fuji Photo Film and Olin Hunt

In September 1987, Fuji Hunt Electronics Technology (Tokyo), jointly owned by Fuji Photo Film and Olin Hunt, began marketing a photoresist (FH5100) for 1Mb DRAM production.

AGREEMENT UPDATES

Tokyo Sanyo and Vitelic

In January 1987, Tokyo Sanyo began producing high-speed SRAMs for Vitelic on an OEM basis under their agreement signed in October 1986.

1987 Japanese Semiconductor Alliances

Sharp and Wafer Scale

In January 1987, Sharp agreed to supply 55ns 64K, 128K, and 256K CMOS EPROMs for Wafer Scale Integration (WSI) of Fremont, California. Sharp has supplied unfinished CMOS wafers to Wafer Scale since 1984. Their original agreement was expanded in October 1985 to include WSI's 1.6-micron CMOS process.

Sony and AMD

In February 1987, Anthony B. Holbrook of AMD announced that AMD would invest ¥1 billion ($6.6 million) in the Atsugi Technology Center, open a design room, and discuss the mutual supply of products with AMD on an OEM basis.

Seiko and Applied Micro Circuits

In April 1987, Applied Micro Circuits Corp. (AMCC) offered high-performance BICMOS logic arrays (Q12000 Series) combining 1.5-micron bipolar and CMOS technologies, which were developed through a technology exchange program with Seiko that started in 1985. The BICMOS arrays range from 2,100 to 9,072 gates.

Toshiba, NEC, Rohm, Sharp, and Zilog

In April 1987, Zilog decided to limit Z80 second sourcing to NEC, Rohm, Sharp, and Toshiba to prevent excessive competition. Only Toshiba is allowed to use the Z80 in its macrocell configuration. This decision has a major impact on Asahi Chemical, Seiko Epson, Yamaha, and other ASICs newcomers seeking MPU cores for their cell libraries.

Fujitsu and Intel

In April 1987, Fujitsu and Intel Japan announced a jointly developed ASIC MCU with a built-in 16-bit MPU (80186), peripheral LSIs (8251A), and a 16-bit MPU (18677). The devices are compatible with 80186 external bus interfaces. The 18677 employs a 1.5-micron CMOS process. Intel is producing CMOS single-chip MCUs, which Fujitsu initially purchased at a rate of 100,000 units annually.

Toshiba and Motorola

In April 1987, Toshiba began selling Motorola's bipolar logic devices in Japan, as part of their earlier mutual-sourcing agreement.

1987 Japanese Semiconductor Alliances

In May 1987, both companies established a 50/50 joint venture, Tohoku Semiconductor Corporation, to build a production plan with 35,660 square meters of floor space on a 60,334-square-meter tract in the Izumi Parktown Industrial Park in Miyagi Prefecture, and start production of 256K and 1Mb DRAMs, 64K and 256K SRAMs, and 8- and 16-bit MPUs at a monthly rate of 3 million units. Production of 4Mb DRAMs, 1Mb DRAMs, and 32-bit MPUs is planned. The initial investment totaled ¥35 billion ($250 million). The companies are exchanging technical information on memories and MPUs, and joint development of new products. Toshiba is providing MOS memory and logic design and manufacturing technology. Motorola is supplying 8- and 16-bit MPU designs, with plans for exchanging 32-bit MPU designs in the future. Both companies are mutually supplying chips on an OEM basis.

In June 1987, both companies announced plans to add submicron processing lines and begin 4Mb DRAM production in 1989.

In August 1987, Tohoku Semiconductor announced plans to begin 4Mb DRAM production in fiscal 1989 (April 1989-March 1990), a year earlier than originally scheduled, and 32-bit MPUs.

In September 1987, both companies announced plans to expand their mutual OEM agreement to include Toshiba's 1Mb DRAMs and Motorola's 16-bit MPUs. Currently, Toshiba receives Motorola's TTLs. Production of 1Mb DRAMs, 256K SRAMs, and 8- and 16-bit MPUs began in 1988.

Japan Radio and Raytheon

An April 1987, Japan Radio and Raytheon revised their general agreement, which established New Japan Radio (NJR) in 1961. Under the new agreement, each partner must pay license and fees when it produces and markets new products developed by the other. Both partners have global marketing rights. NJR's 1986 sales were ¥15.5 billion ($119 million), of which 80 percent came from bipolar devices and 20 percent from MOS ICs.

Toshiba and Visa International

In May 1987, Toshiba and Visa International completed developing a Supersmart Card. Visa introduced 20 to 30 cards in August, with plans for 15,000 from December 1987 for credit cards. Visa's field experiments are completed.

Sony and AMD

In May 1987, Sony and AMD announced plans for joint development and sales of 20ns 64K SRAMs and 35ns 256K SRAMs using 1.2-micron geometries. Sony currently sells 100ns 64K SRAMs and 45ns 256K SRAMs. Both companies are marketing the products under their own labels.

1987 Japanese Semiconductor Alliances

Kawasaki Steel and LSI Logic

In June 1987, Kawasaki Steel and LSI Logic announced the opening of their new ASICs fab. That same month, LSI Logic opened its Tsukuba design center, which was initially staffed with 20 engineers.

Fuji Electric and Siemens

In June 1987, Fuji Electric and Siemens expanded their cooperative arrangement to promote an international division of labor. Both companies have started a mutual supply of power MOSFETs and share development and production. Fuji is handling 50V to 500V products, while Siemens is handling lower-voltage products. More than 100 models will be commercialized.

Kyocera and Vitelic

In July 1987, Kyocera began importing DRAMs and SRAMs from Vitelic of San Jose, California. Kyocera invested 10 percent of Vitelic's initial capital; Kyocera president Kazuo Inamori sits on the Vitelic board.

Seiko Epson and Siliconix

In October 1987, Siliconix transferred its low-voltage Si6000 and Si7000 digital-only gate array families, second sourced from Seiko Epson, to International Microcircuits Inc. (IMI). IMI supports the Siliconix customer base and work with Siliconix during the transition period. Siliconix laid off 39 of its 2,600 employees and is refocusing its ASICs business to concentrate on mixed A/D arrays and standard cells.

Sumitomo Metal and Standard Microsystems (Toyo Microsystems)

In October 1987, Toyo Microsystems, a joint venture formed in December 1986 and owned by Sumitomo Metal (Osaka) and Standard Microsystems (Hauppauge, New York), began marketing standard cells in Japan.

Toshiba, Motorola, and Tangent Systems

In November, Tangent Systems announced a jointly developed layout system that allows 70 to 80 percent gate utilization of three-layer metal, high-density sea-of-gates arrays. Toshiba is using the CAD tools to place and route its TC110G family of 1.5-micron CMOS gate arrays, ranging from 5,300 to 129,040 gates. Motorola's ASIC division is using it with its MAX family of high-density gate arrays.

NMB and National

In December 1987, NMB Semiconductor and National Semiconductor began joint development of 256K SRAMs, 256K EPROMs, and 512K EPROMs. The chips are being produced by NMB and shipped under National or NMB labels.

AGREEMENTS TERMINATED

NMB Semiconductor and Lattice

In January 1987, NMB Semiconductor dissolved its OEM agreement with Lattice Semiconductor of Portland, Oregon, due to disagreements over technicalities of the agreement. Lattice had supplied 16K and 64K SRAM design technology to NMB in exchange for memory devices. NMB strengthened its ties with National Semiconductor, with whom it is developing 64K SRAMs. Lattice retained Seiko-Epson as its foundry source.

NMB Semiconductor and Inmos

In January 1987, NMB stopped shipments of 256K DRAMs to Inmos due to disagreements over pricing. Inmos, which had arranged to buy 50 percent of NMB's DRAMs, asked for a price reduction to improve its market position. NMB declined, forcing Inmos to withdraw from the 256K DRAM market. Production of 256K DRAMs at Inmos' Colorado Springs, Colorado, plant was suspended in June 1986 when price erosion hurt company earnings. In July 1987, NMB began production of Vitelic's 1Mb CMOS DRAMs.

Tokyo Electron and Lam Research

In February 1987, TEL dissolved its joint venture contract with Lam Research of the United States and bought back all of Lam's share in TEL-Lam, which was formed in July 1983. TEL-Lam changed the company name to TEL Yamanashi Ltd., which is a wholly owned subsidiary of TEL. TEL will continue to manufacture dry etching equipment at TEL Yamanashi.

Disco Abrasive Systems and Helmut-Seier

In February 1987, Disco Abrasive Systems and Helmut-Seier Electronics A.G. of Switzerland dissolved their joint venture, Disco-Seier Japan, which has become Disco's wholly owned subsidiary, Disco Hitech. Disco-Seier U.S.A. changed its name to Helmut-Seier Electronics U.S.A., a Helmut-Seier subsidiary.

Sony and Vitelic

In May 1987, Sony and Vitelic dissolved their technical partnership for 256K DRAMs, originally formed in May 1985, due to the industry slump. The capital association between the two companies will continue.

Itoh Technoscience and Samsung

In August 1987, Itoh Technoscience terminated its 1985 agreement to sell Samsung 256K DRAMs into the Japanese market because of sluggish sales.

Hitachi and Motorola

In December 1987, Hitachi announced plans to phase out its Motorola-based line of CMOS one-time programmable (OTP) 8-bit MCUs and one ROM-based design. The patent cross-licensing agreement was renewed in 1986, but met limited success. The OTP versions of the HD63701V, HD63701X, HD63701Y, HD63705V, and HD63705Z will be phased out by March 31, 1991. The ROM-based HD6305Z will be dropped by March 31, 1990. Customers can migrate to Hitachi's new HHMCS400 ZTAT series and the Zilog-based HD647180 ZTAT series. Motorola plans its own OTPROM series based on the MC68HC11, -HC05, and -HC04 families.

1986 Japanese Alliances

SUMMARY

Corporate marriages are heating up. In 1986, strategic alliances were in vogue as Japanese semiconductor companies scrambled to overcome shrinking domestic sales and export obstacles imposed by the U.S.-Japan Semiconductor Trade Arrangement. With profits down sharply, heavy new investments in capital equipment, R&D, and marketing remained out of the question. Instead, many Japanese companies formed alliances as an efficient way to leverage their corporate assets to enter new markets and develop new products. Teaming up with U.S., European, and other Asian companies, not battling head-on with them, was viewed as one solution to growing trade friction (boeki-masatsu) and the yen shock (endaka).

As shown in Table 1, Japanese semiconductor companies entered a record 101 alliances in 1986, up from 71 in 1985. Dataquest notes that materials companies accounted for 11 of the 101 agreements last year.

Table 1

1986 JAPANESE SEMICONDUCTOR STRATEGIC ALLIANCES

Type	1980	1981	1982	1983	1984	1985	1986
Semiconductor Devices	3	6	10	14	30	54	76
Equipment & Materials	0	5	12	8	26	17	25
Total	3	11	22	22	56	71	101

Source: Dataquest
March 1987

TRENDS

Regional Shifts

As shown in Table 2, Dataquest observes that inter-Japanese alliances are accounting for a rapidly growing share of alliances, especially in the equipment and materials field, suggesting rising technological strength among Japanese companies.

1986 Japanese Alliances

Table 2

JAPANESE SEMICONDUCTOR PARTNERS
BY REGION

Region	1985	1986
United States	50	67
Japan	9	24
Europe	10	8
Asia	2	2
Total	71	101

Source: Dataquest
March 1987

The Shift to Superalliances

A major global trend in 1986 was the rise of "superalliances," such as the Toshiba/Motorola, Fujitsu/Fairchild (which was stopped by the U.S. government), and Sony/AMD, as shown in Table 3. Dataquest believes that these superalliances, especially mutual fab agreements and joint R&D and marketing, will proliferate over the next few years due to excess plant capacity and reduced profits. Currently, both U.S. and Japanese semiconductor makers have excess capacity, but on the wrong side of the Pacific Ocean. Sharing plant capacity, products, and distribution channels will reduce investment costs and give each partner greater access to the other's markets. In light of the growing protectionism and fierce global competition, we believe that loners run the risk of becoming isolated and losing market share.

1986 Japanese Alliances

Table 3

MAJOR JAPANESE GLOBAL ALLIANCES

Japanese Company	Foreign Company	Status
Fujitsu	Fairchild	Joint R&D and marketing
Hitachi	Monsanto Japan	Silicon wafer technology
Oki Electric	Voest Alpine	Joint venture canceled
Matsushita	Intel	Reportedly being negotiated
Matsushita	Philips-Signetics	Equity participation
Mitsubishi	Texas Instruments	Standard logic ICs, possible expansion of agreement
NEC	Zilog	V Series second-sourcing
Ricoh	VLSI Technology Silicon Compilers	Wafer supply Silicon compiler for CMOS
Rohm/Exar	Exel	Takeover
Sanyo	Vitelic	Fab agreement
Seiko Epson	Siliconix Lattice	ASIC wafer supply PLD production
Sharp	RCA	Joint venture canceled
Sony	AMD	Joint development
Toshiba	Motorola	Technology exchange, joint fab

Source: Dataquest
March 1987

Growing Complexity of Alliances

Another trend is the growing complexity and sophistication of Japanese semiconductor alliances. In the early 1980s, licensing and second-sourcing agreements predominated, but we observed a wide variety of agreements in 1986, ranging from fab, assembly, and testing contracts to joint R&D and partial investment, as shown in Table 4. We believe that these alliances reflect the growing sophistication and interdependence of the semiconductor industry, and Japanese efforts to surmount increasing protectionism by joining and investing in foreign companies.

Due to this growing complexity, Dataquest will report strategic alliances using the above categories beginning this year. For reference, we provide definitions for the various categories in Table 5.

Table 4

1986 JAPANESE SEMICONDUCTOR ALLIANCES BY TYPE

Code	Type of Alliance	Number
1	Licensing Agreements	6
2	Second-Source Agreements	10
3	Sales Agency Contracts	21
4	Fabrication Agreements	10
5	Assembly & Testing Agreements	2
6	Technology Exchanges	4
7	Joint Ventures	16
8	Joint R&D	27
9	Investment (less than 50%)	4
10	Common Standards	1
	Total	101

Source: Dataquest
March 1987

Table 5

TYPES OF STRATEGIC ALLIANCES

Class	Type	Explanation
1.	Licensing Agreement	Company A receives a license to Company B's product or process for an upfront fee and/or royalties. a. Company A is permitted to compete in all markets. b. Company A can only use product in-house or sell in restricted markets.
2.	Second-Source Agreement	Both companies agree to develop consistent specifications to ensure a second source.
3.	Sales Agency Agreement	Company A sells Company B's products. a. Product is sold under manufacturer's (Company A) label. b. Product is sold under reseller's (Company B) label.
4.	Fab Agreement	Company A trades product technology for allocated fab capacity at Company B. a. Company A's process is installed at Company B. b. Company A's process is not installed at Company B.
5.	Assembly and Testing Agreement	Company A sends its devices to Company B for assembly and/or testing.
6.	Technology Exchange	Both companies exchange technology, which may or may not include a transfer of money.

(Continued)

Table 5 (Continued)

TYPES OF STRATEGIC ALLIANCES

Class	Type	Explanation
7.	Joint Venture	Both companies agree to a broad-ranging agreement to jointly develop, manufacture, and market new products.
8.	Joint Development	Both companies agree to jointly develop new products, which may or may not be marketed separately.
9.	Investment	Company A invests in Company B (less than 50 percent of stock) to secure new technology or access to new markets.
10.	Joint Standards	Both companies agree to a common set of standards to promote their products as an industry standard.
11.	Other	

Source: Dataquest
March 1987

1986 Japanese Alliances

Greater Product Diversification

In the early 1980s, Dataquest observed many one-way transfers of microprocessor technology from U.S. makers to Japanese second sources, which quickly enabled Japanese companies to dominate the 4-bit and 8-bit MPU markets. We note a shift toward more two-way technology transfers involving a broader range of products in 1986, as shown in Table 6. In particular, there was a sharp jump in multiproduct agreements. We believe that U.S. concern over the "boomerang effect" and growing Japanese technological strength are giving rise to more equitable, two-way technology flows.

Table 6

1986 JAPANESE SEMICONDUCTOR ALLIANCES BY PRODUCT CATEGORY

Product Category	Number
Multiple products	16
Memory	10
Microprocessors	12
Application-specific ICs (ASICs)	22
Standard logic	4
Other devices	12
Equipment	14
Materials	11
Total	101

Source: Dataquest
March 1987

SCORECARD OF JAPANESE ALLIANCES

For convenience, Table 7 lists all the Japanese semiconductor alliances publicly announced in 1986. The type of alliance (see Table 6) is indicated in column four.

1986 Japanese Alliances

Table 7

1986 JAPANESE SEMICONDUCTOR ALLIANCES

Date	Company A	Company B	Type	Products
		Multiproduct		
02/86	Sony	AMD	8	Next-generation ICs
02/86	Tokyo Electron	Nippon Motorola	3A	All products
03/86	Nippon Steel	Philips/ Nippon Chemi-Con	7	Components
04/86	Kowa Denko	SGS-Ates	3A	All products
04/86	Dainichi Contronics	GE	3A	All products
04/86	Yokogawa Hokushin	GE	7	Electronic parts
04/86	Asahi Chemical	Hitachi	7	ASICs, SRAMs, ROMs
06/86	Mareui Trading	Honeywell	3A	DSP, bipolar gate arrays
06/86	Toshiba	Motorola	7	CMOS memories and MPUs
06/86	Ricoh	Hyundai	5	IC assembly
06/86	Seiko Epson	Anam Industrial	5	IC assembly
06/86	Kanematsu Semi.	VTC	3A	Linear bipolar; CMOS dig.
06/86	Kanematsu Semi.	IDT	3A	CMOS SRAMs, logic, DSP
07/86	Oki Electric	Catalyst	8	CMOS 8-bit MCUs and EEPROMs
08/86	Chronix	Matra-Harris	3A	Image processors, etc.
12/86	Asahi Chemical	Crystal/ICT	6	EPROMs, A/D, analog ICs
		Memory		
01/86	Matsushita	NTT	8	Megabit memories
02/86	Seiko Epson	Lattice	2	64K CMOS SRAMs
04/86	Ryoyo	NCR/Japan Macnics	3A	EEPROMs, NVRAMs
05/86	Sharp	MOSel	4	256K CMOS SRAMs
06/86	Mitsubishi	Intel	4	Memories
06/86	MCM Japan	Atmel	3A	CMOS EEPROMs
08/86	Fuji Electric	MOSel	8	CMOS 256K SRAMs
09/86	Sony	Vitelic	4A	CMOS SRAMs
10/86	NMB Semiconductor	National	7	CMOS SRAMs
10/86	Tokyo Sanyo	Vitelic	7	High-speed SRAMs
		Microprocessors		
02/86	Rohm	Zilog	2A	Z8/Z80 8-bit MPUs
02/86	NEC	Boeing	8	CMOS single-chip MCU
02/86	NEC	Oki Electric	8	CMOS signal processor
03/86	NEC	Zilog	2	Z800/Z8000
04/86	NEC	Seiko Epson	2	V Series MPUs
06/86	TRON Project	(8 companies)	8	32-bit MPU system
06/86	Okaya & Co.	Intel Japan	3A	Factory automation MPUs
06/86	Hitachi	Zilog	2	8-bit CMOS MPUs
06/86	Mitsubishi Corp.	Semicon Systems	9	Intel MPUs
07/86	NEC	Sharp	8	V Series peripherals
10/86	Fujitsu	Hitachi	8	TRON 32-bit MPUs and MPRs
12/86	Toshiba	Zilog	2	Z80 MPUs

(Continued)

1986 Japanese Alliances

Table 7 (Continued)

1986 JAPANESE SEMICONDUCTOR ALLIANCES

Date	Company A	Company B	Type	Products
		ASICs		
02/86	Sony	LSI Logic	8	ASICs masks and foundry
02/86	Toshiba	LSI Logic	7	ASICs, CAD system
02/86	Ricoh	Panatech	3	CMOS PLDs and gate arrays
02/86	Ricoh	VLSI Technology	4B	ASICs
03/86	Sharp	RCA/Wafer Scale	8	Macrocells
03/86	Toshiba	GE and Siemens	8	Standard cells
03/86	Toshiba	Laser Path	7	Gate arrays
03/86	Seiko Epson	Siliconix	4A	ASIC wafer supply
03/86	Yokogawa H-P	Hewlett-Packard	8	CAD system for PLDs
04/86	Marubeni Corp.	LSI Logic KK	3A	CMOS gate arrays
05/86	Tokyo Electron	Digi-Systems	3A	CAE workstation
06/86	Mitsubishi	LSI Logic	4	Gate array foundry
06/86	Ricoh	Calif. Micro Dev.	6	ASICs CAD technology
07/86	Ricoh	Silicon Compilers	6	Silicon compiler, CMOS
08/86	Okura & Co.	Xilinx	3A	Logic cell arrays
08/86	Kyocera/Mitsui/ ASCII	Chips and Technologies	7	ASICs for PC clones, ISDN networks and compact disks
10/86	Solitron Systems	Silicon Compilers	3A	Silicon compiler software
10/86	Kanematsu Semi.	Electrical Engineering	3A	IC CAD software
10/86	Seiko Epson	Lattice	4A	Generic array logic (GAL)
11/86	Fujitsu	Arimura Industrial	1B	IC cards
12/86	Sumitomo Metal	Standard Microsys.	7	ASICs
12/86	Sumitomo Corporation	Integrated Logic Systems	1	ASICs design
		Standard Logic		
01/86	Hitachi	Riken	8	Quantum Flux Parametron
07/86	Hitachi	Fairchild	2	Fairchild FACT logic
08/86	Marubeni Hytech	Fairchild	3A	Fairchild TTL and FACT
12/86	Mitsubishi	Texas Instruments	8	High-speed TTL/CMOS logic
		Other Devices		
03/86	Toshiba	Intel	4A	Multibus II interface ICs
05/86	Sony	Sharp	10	Semiconductor lasers
05/86	NEC	Compass Systems	8	LAN ICs
07/86	Chronix	Matra-Harris	3A	Image processors
08/86	NEC	Tokyo Sanyo	2A	Linear ICs for TVs
08/86	Hitachi	Signetics	1	Telecom LSIs
08/86	Teksel	Anadigics	3A	GaAs amplifier ICs
08/86	Matsushita	Philips	2B	LSIs for compact disks
10/86	Rikei	Adams-Russell	2A	GaAs ICs
10/86	Hamamatsu Photonics	City University of New York	8	Optoelectronics
10/86	Oki Electric	Silicon Systems	4B	Single-chip modem LSIs
11/86	Stanley Electric	Kyokuto Trading	7A	Car electronics

(Continued)

1986 Japanese Alliances

Table 7 (Continued)

1986 JAPANESE SEMICONDUCTOR ALLIANCES

Date	Company A	Company B	Type	Products
		Equipment		
01/86	Citizen Watch	Perkin-Elmer	7	Aligners and etchers
01/86	Okano Electric	Factory Automation	3	Surface-mount assembly
05/86	Marubeni Hytech	Ion Beam Technol.	9	Ion beam equipment
05/86	Fuji Electric	Cambridge Instr.	7	MOCVD equipment
05/86	RHD Inc.	Gakei Electric	8	Crystal pulling machine
06/86	NEC	JEOL	8	Focused ion beam machine
06/86	Hitachi	Toyohashi Univer.	8	Hybrid electron/ion beam
07/86	ULVAC ETU	Seiko Instruments	8	Clean room robot
07/86	Hitachi	NTT	8	Direct-write E-beam
08/86	ULVAC Group	Inabata	7	Vacuum equipment
09/86	Napson	Keithley	3A	Wafer measuring equipment
10/86	Mitsubishi Corp.	Nihon MRC	9/3A	Ion etchers, sputterers
10/86	Shinkawa	KLA Instruments	8	IC wire-bonding inspector
12/86	Toshiba	Tokuda Works	8	Reactive ion etcher
		Materials		
01/86	Fujikura	CTS Corp. (U.S.)	8	Metal and conductive paste
02/86	Matsushita Denso	Hayashibara/Japan Compound Gum	4A	Water-soluble photoresist
02/86	Kyocera	Wacker Chemitronic	1A	Polycrystal silicon
06/86	Mitsubishi	Dai Nippon/Hoya/ Toppan/ULVAC	1A	Photomask technology
07/86	Hitachi	Monsanto	6	Wafer technology
08/86	Shinkawa	Superwave Tech.	1A	Epoxy and polyimide process
08/86	Dai Nippon Print.	Perkin-Elmer	8	Photomasks for X-ray
09/86	Mitsubishi Corp.	Nisshin/Toyo Ink	7	Blue LED material
10/86	Asahi Glass	Olin Corp.	7	Hybrid IC substrates
10/86	Mitsubishi Corp.	Nihon MRC	9	Ion etchers and sputterers
11/86	Asahi Denka	Union Carbide	8	Epoxy resins
		Update on Existing Alliances		
02/86	NEC	Corvus	8	1-chip LAN controllers
02/86	Kanematsu Semi.	Anicon	10	CVD system (lawsuit)
05/86	Asahi Chemical	Gould AMI	7A	ASICs (canceled)
07/86	Oki Electric	Voest Alpine	7A	256K DRAMs (canceled)
08/86	NMB Semiconductor	Vitelic	4A	CMOS 1Mb DRAMs
08/86	Sharp	RCA	7	ASICs (dissolved)
08/86	Sharp	TI	10	TI's DRAM technology (lawsuit)
12/86	Fuji Electric	Siemens	9	Sensors, semiconductors

Source: Dataquest
March 1987

1986 Japanese Alliances

THE BOOM IN FOUNDRY ALLIANCES

Dataquest observes that Japanese companies are entering the silicon foundry business due to plant overcapacity and the U.S.-Japan semiconductor agreement, which has limited Japanese exports to the United States. Table 8 lists recent foundry alliances.

Table 8

JAPANESE SILICON FOUNDRY ACTIVITIES
(Publicly Announced)*

Foundry	Buyer	Date	Products
Fuji Electric	Lattice	10/85	64K CMOS SRAMs, logic
Kawasaki Steel	LSI Logic	09/85	ASICs joint venture fab
Mitsubishi Electric	Intel	06/86	Memories
	LSI Logic	06/86	ASICs
NMB Semiconductor	Inmos	06/84	256K CMOS DRAMs
	Vitelic	11/85	1Mb CMOS DRAMs
	National	09/86	CMOS SRAMs (4 types)
	(U.S. maker)	1985	Fast 64K SRAMs
	(Unannounced)	1986	CMOS SRAMs and DRAMs
Oki Electric	Silicon Systems	09/86	Single-chip modem LSIs
Ricoh	VLSI Technology	09/83	64K/128K/256K ROMs, ASIC
	Silicon Compilers	09/86	CMOS custom ICs
Seiko-Epson	Xilinx	12/85	Logic cell arrays
	Lattice	02/86	Fast 64K CMOS SRAMs
	Lattice	09/86	Programmable logic (GAL)
Sharp	Wafer Scale	12/84	64K/256K CMOS EPROMs
	MOSel	05/86	Fast 256K SRAMs
Sony	Vitelic	07/85	Fast CMOS SRAMs
	LSI Logic	02/86	ASICs
Suwa Seikosha	SMOS Systems	12/84	CMOS gate arrays
	AMCC	05/85	CMOS chips
Toshiba	Motorola	09/86	ASICs; 64K/256K DRAMs
	(8 U.S. firms)	1986	Negotiating

*Incomplete listing; most foundry agreements are not publicly announced

Source: Dataquest
March 1987

1986 Japanese Alliances

THE ENTRY OF JAPANESE HEAVY INDUSTRIES

Due to sluggish world markets and the yen shock, Japanese steel, chemical, and metals companies are shifting into high-technology industries. Table 9 lists recent alliances and takeovers of semiconductor companies.

Table 9

SEMICONDUCTOR ACTIVITIES BY HEAVY JAPANESE INDUSTRIES

Japanese Company	IC Manufacturer	Agreement
Asahi Chemical	Crystal Semicon.	$15 million for 8% share
Asahi Chemical	Hitachi	Switched ASICs from Gould AMI to Hitachi
Kawasaki Steel	LSI Logic	ASIC joint venture
Kobe Steel	GCA Laser Div.	100% takeover
Mitsubishi Corporation	Japan MRC	25% investment
Mitsubishi Corporation	Semicon Systems	$1.2 million investment
Mitsubishi Metal	Siltec	$33 million takeover
Nippon Steel	Philips	Electronics joint venture
Sumitomo Corporation	Integrated Logic Systems	Licensing ILSI's ASICs design
Sumitomo Metal	Standard Micro Systems	$13.5 million for 20% share for ASIC joint venture
Toshiba Ceramics	Quartz Int'l.	$11.4 million for 80% share

Source: Dataquest
March 1987

1986 Japanese Alliances

DESCRIPTIONS OF STRATEGIC ALLIANCES

For your convenience, Dataquest provides a short description of each 1986 Japanese semiconductor alliance, categorized by type of alliance, in the following pages. In a forthcoming newsletter, we will analyze major trends in product alliances, process "clustering," and corporate strategies.

Multiproduct

Sony and AMD

In February 1986, Sony and AMD signed a letter of intent to enter into a joint technology development program. The companies plan to develop a common process technology, exchange designs and mask sets, and produce and market those products worldwide. Sony will buy from AMD on an OEM basis. AMD, which spent more than $180 million on semiconductor R&D in 1985 and had 1986 revenue of $629 million, plans to enter consumer markets through this tie-up. Sony, which had semiconductor revenue of $475 million in 1986, also has alliances with Tektronix (CAD workstations), Zilog, Sharp, NEC (V Series MPUs), Monsanto (LEC technology), and Vitelic (CMOS SRAMs).

In July 1986, Advanced Micro Devices (AMD) and Sony Corporation announced that they were negotiating an agreement to jointly develop MOS ICs for consumer electronics equipment. In late 1986, AMD opened a quality assurance center near Sony's Research Center in Atsugi, Japan.

Tokyo Electron and Nippon Motorola

In February 1986, Nippon Motorola and Tokyo Electron (TEL) signed a sales agency contract for Motorola semiconductors and related products. TEL set up a new marketing division to sell these products. Sales in the first year are targeted at ¥5 billion ($26 million). TEL also is the sales agent for AMD, Intel, Fujitsu, and Western Digital. It will be the first trading company to handle both Intel's 8086 and Motorola's 68000.

Nippon Steel, Nippon Chemi-Con, and Philips

In March 1986, the three companies agreed to establish a joint venture in Japan to produce electronic components. NSC Electronic, a wholly owned Nippon Steel subsidiary formed in June 1985 to produce and market semiconductor materials and silicon wafers, will cooperate with the venture.

1986 Japanese Alliances

Kowa Denko and SGS-Ates

In April 1986, Kowa Denko signed a sales agency contract with SGS Semiconductor of Italy to import and sell SGS products in Japan, especially linear ICs. Sales in the first year are targeted at ¥500 million ($2.8 million). SGS also has sales agency contracts with Matsushita Electric Trading and Nihon Teksel.

Dainichi Contronics and GE

In April 1986, General Electric Semiconductor signed a sales agency contract with Dainichi Contronics to handle all products in Japan for GE's Semiconductor Division. The sales goal in the first year is ¥1 billion ($5.6 million); the goal in three years is ¥5 billion ($28.1 million), about half of GE's total Japan sales. Dainichi also handles Intersil products.

Yokogawa Hokushin and GE

In April 1986, Yokogawa Hokushin Electric and General Electric signed a 50/50 joint venture to develop and manufacture electronic parts in Japan.

Asahi Chemical and Hitachi

In April 1986, Asahi Chemical bought out Gould AMI's share in Asahi Microsystems and signed a licensing agreement with Hitachi. Under the agreement, Asahi will market Hitachi's 64K and 256K SRAMs, mask ROMs, and CMOS gate arrays on an OEM basis for two to three years, then produce its own parts. Asahi Chemical is establishing its U.S. and European sales network through sales offices in New York City and Brussels. Asahi will act as AMI's exclusive agent for custom ICs in Asia, while AMI will market Asahi devices in the United States. Asahi Chemical plans to build a semiconductor factory and begin production by mid-1988. Currently, Asahi and Hitachi are jointly developing high-speed SRAMs with 25ns access times.

In 1983, Asahi Chemical and AMI entered the Japanese ASIC market with a first-year sales goal of ¥6 billion ($36 million), but annual sales have only been between ¥2 billion ($12 million) in 1984 and ¥4 billion ($24 million) in 1985, for an estimated total of ¥6.6 billion ($40 million). The two firms opened a joint Tokyo design center and use AMI's fab in the United States.

1986 Japanese Alliances

Maruei Trading and Honeywell

In June 1986, Mareui Trading Co. signed a sales agency contract with the DSP Industry Division of Honeywell to sell Honeywell's products, including bipolar gate arrays, in Japan.

Toshiba and Motorola

In June 1986, Toshiba entered a partnership with Motorola to exchange semiconductor technology. Toshiba will provide CMOS memory process technology in exchange for Motorola's 16-bit MPU technology. Toshiba will also produce semiconductors based on Motorola's specifications and supply them to Motorola on an OEM basis. Toshiba will initially focus on semicustom ICs, which will be manufactured at Iwate Toshiba Electronics. In August, Toshiba began supplying 256K DRAM wafers to Motorola for assembly and sale in the United States.

In December, the two companies formed a joint venture to develop, produce, and sell memories and MPUs. The 50/50 joint venture will be established in early 1987 in Izumi City, Miyagi Prefecture (350km north of Tokyo), where Motorola owns a 60,000-square-meter facility. The ¥35 billion ($219 million) Izumi plant will be jointly operated and equipped with 6-inch wafer lines with a monthly production capacity of 3 million ICs. About 250 workers will be employed at the plant. Production will begin in early 1988. Initially, the plant will produce 256K and 1Mb DRAMs, 64K and 256K SRAMs, and 8-bit and 16-bit MPUs, but eventually it will add 4Mb DRAMs, 1Mb SRAMs, and 32-bit MPUs. Only front-end processing will be done at Izumi. Semifinished MPUs will be sent to Toshiba and the memories to Motorola Korea for final assembly. The firms also agreed to a two-year technology exchange agreement. Toshiba will offer know-how on 4Mb DRAMs, 1Mb SRAMs, and MOS logic processes; Motorola will provide 32-bit MPU technology. Toshiba will also buy 8-, 16-, and eventually 32-bit MPUs from Motorola from 1987 to 1991.

Ricoh and Hyundai Electronics

In June 1986, Ricoh contracted its IC assembly work to Hyundai Electronics in South Korea because of cost advantages resulting from the sharp appreciation of the yen.

Seiko Epson and Anam Industrial

In June 1986, Seiko Epson contracted its IC assembly work to Anam Industrial in South Korea.

1986 Japanese Alliances

Kanematsu Semiconductor and VTC

In June 1986, Kanematsu Semiconductor signed a sales agency contract with VTC of Bloomington, Minnesota, to sell VTC's high-performance linear bipolar and digital CMOS devices. VTC offers CMOS and bipolar gate arrays and standard cells, CMOS silicon compiler services, interface logic, and bipolar semicustom ICs.

Kanematsu Semiconductor and Integrated Device Technology (IDT)

In June 1986, Kanematsu Semiconductor signed a sales agency contract with Integrated Device Technology (IDT) of Santa Clara, California, to sell its high-speed CMOS SRAMs, high-density modules, CMOS logic, bit-slice MPUs, and digital signal processors. Sales of IDT's products are targeted at ¥200 million ($1.2 million) in the first year and ¥1 billion ($5.8 million) in three years. Internix Inc. is IDT's other sales agency in Japan.

Oki Electric and Catalyst Semiconductor

In July 1986, Oki Electric and Catalyst Semiconductor of Santa Clara, California, entered into a partnership for long-term research and development of NVRAMs for ASICs using 16K to 64K CMOS EPROMs and EEPROMs. The products will use Oki's advanced CMOS technology. Terms included a nonexclusive marketing agreement.

In August, Oki announced a CMOS single-chip 8-bit MCU incorporating an EEPROM (MSM61580) for use in IC cards. The 5.0 x 4.5mm chip has a 4.9-MHz clock frequency and was jointly developed with Catalyst. In September 1986, both companies announced a CMOS 8-bit single MCU with a built-in CMOS 16K EEPROM (MSM61580), priced at ¥5,000 ($32.26). Volume production began in December at 50,000 units per month, with plans to increase production to between 200,000 and 500,000 units in May 1987.

Chronix and Matra-Harris

In August 1986, Chronix signed an agency agreement to market semiconductors from Matra-Harris Semiconducteurs in Japan, including image processors jointly developed with Intel. The goal is to sell ¥387.5 million ($2.5 million) worth of devices in two years.

Asahi Chemical, Crystal, and International CMOS Technology

In December 1986, Crystal Semiconductor sold 8 percent of its stock to Asahi Chemical for $15 million over the next five years. Asahi will be the exclusive distributor for Crystal in Asia for three years. Crystal will give Asahi three analog IC masks and receive licensing fees and equity investment. Crystal earlier received $11 million in second-round financing from venture capitalists.

Also in December, Asahi Chemical, Crystal Semiconductor of Austin, Texas, and International CMOS Technology (ICT) of San Jose, California, agreed to a technology exchange covering the design and production of A/D converters and CMOS EEPROMs. Crystal will provide design technology for A/D converters, universal filters, LAN LSIs, and CMOS A/D LSIs, which will be sold throughout Asia. ICT will provide design and production know-how for its CMOS EEPROMs. In April, Asahi Microelectronics switched its ASIC partnership from AMI Gould to Hitachi. ICT has alliances with Hyundai, IMP, and Gould.

Memory

Matsushita and NTT

In January 1986, Matsushita Electric and Nippon Telegraph and Telephone (NTT) signed a technical cooperation agreement to jointly develop 4Mb DRAMs and higher for mainframe computers, optical computers, high-definition television sets, and other consumer electronics. The two companies will share patents and R&D facilities, and will exchange engineers. Currently, Matsushita lags Fujitsu, Hitachi, NEC, and other semiconductor makers that have participated in joint projects with NTT for many years.

Seiko Epson and Lattice

In February 1986, Seiko Epson and Lattice Semiconductor of Beaverton, Oregon, signed a second-source agreement for Lattice's 64K CMOS SRAMs (SR64K4). Seiko Epson will produce the SRAMs and sell them through its U.S. subsidiary, SMOS Systems of San Jose, California. Lattice's 64K SRAM has a 35ns access time and a 16Kx4 organization, and is developed using a 1.1-micron CMOS process (Ultra MOS-I). Seiko Epson's Fujimi plant has the capability of running 35,000 4-inch wafers/month and 15,000 5-inch wafers/month, and plans a new line to run 20,000 6-inch wafers/month. Lattice also produces CMOS EEPROMs, EQ-CMOS programmable logic, and digital signal processors.

Ryoyo Electronics, Japan Macnics, and NCR

In April 1986, NCR signed sales agency contractors with two Japanese electronics distributors, Ryoyo Electronics Corporation and Japan Macnics Corporation, to sell its 64K and 256K EEPROMs, nonvolatile RAMs, and other products in Japan. Sales in the initial year are targeted at ¥400 million ($2.2 million).

1986 Japanese Alliances

Sharp and MOSel

In May 1986, Sharp signed a fab agreement with MOS Electronics (MOSel) of Sunnyvale, California, under which MOSel provides its 256K SRAM design and 1.2-micron CMOS process in exchange for Sharp's foundry capacity. Sharp will provide 256K SRAMs under an OEM contract. MOSel also signed an agreement with Fuji Electric in August 1986.

Mitsubishi and Intel

In June 1986, Mitsubishi Electric agreed to provide foundry work for Intel.

MCM Japan and Atmel

In June 1986, MCM Japan signed a sales agency contract with Atmel of San Jose, California. MCM initially will import Atmel's CMOS EEPROMs (AT28C64). MCM was formed in September 1984 by five former Tokyo Electron Co. members. Atmel was established in November 1984 by former SEEQ employees.

Fuji Electric and MOSel

In August 1986, Fuji Electric and MOS Electronics (MOSel) of Sunnyvale, California, agreed to jointly develop CMOS 256K SRAMs and produce them starting in the second half of 1987. In September 1985, the two companies signed a silicon foundry agreement in which MOSel provided its 1.5- to 2.0-micron CMOS process for 16K and 64K SRAMs for fabrication at Fuji's fab. Fuji has shipped approximately 200,000 to 300,000 units of its 16K and 64K SRAMs to MOSel. Eventually, MOSel plans to use Fuji's Matsumoto fab in Nagano prefecture to produce ASICs.

Sony and Vitelic

In September 1986, Sony and Vitelic replaced their existing agreement to produce 64K and 256K CMOS DRAMs with a new fab contract for CMOS SRAMs because of the greater market potential. Sony currently produces 16K and 256K SRAMs at a monthly rate of 1.4 million units.

NMB and National

In October 1986, NMB Semiconductor established a five-year partnership with National Semiconductor to jointly develop VLSIs, beginning with SRAMs. National has also expressed interest in giving second sourcing rights to NMB for 1Mb and 4Mb DRAMs and EPROMs. NMB will produce the devices at its Tateyama plant in Chiba Prefecture, which National will market through its worldwide sales network. In September,

NMB boosted its production of CMOS 256K DRAMs and 64K SRAMs to 8 million units per month by mid-1987. Line 1 will go into full production (4 million units/month) by spring of 1987. NMB plans to add capacity of 4 million units per month by investing ¥20 billion ($130 million) in Line 2 in early 1987. NMB currently uses Inmos technology to produce CMOS 256K DRAMs and 64K SRAMs, and produces 1Mb DRAMs for Vitelic.

Tokyo Sanyo and Vitelic

In October 1986, Tokyo Sanyo signed a broad agreement with Vitelic of San Jose, California, covering fabrication, technology transfer, and joint development. Sanyo will fabricate high-speed 16K and 64K SRAMs for Vitelic. Read times for the devices are: 25ns for the 16K model and 25/30ns for the 64K model. The SRAMs will be produced at Niigata Sanyo Electric and marketed worldwide through Vitelic's sales network. Vitelic also plans to have Tokyo Sanyo produce 256K SRAMs (25ns access time). The Niigata plant originally was built to produce DRAMs, but switched to SRAMs due to surplus capacity. Small volumes of DRAMs will be produced for Sanyo's in-house use. Vitelic also has agreements with Philips, Sony, Hyundai, NMB Semiconductor, and the Electronic Research and Service Organization (ERSO) of Taiwan.

Microprocessors

Rohm and Zilog

In February 1986, Rohm signed a five-year agreement to second-source Zilog's CMOS and NMOS 8-bit Z80 MPUs, 8-bit Z8 single-chip MCUs, and five Z80 peripheral chips, including a DMA IC controller in Japan and neighboring countries. In early 1986, Zilog was supplying Rohm two MPU products at a monthly rate of 20,000 to 30,000 chips for assembly and testing. Plans call for increasing Zilog's supply to 100,000 chips per month and (Rohm's domestic production) of the Z8000 16-bit MPU. Zilog already produces Z80 chips (ROHMZ80) at a rate of 100,000 chips per month. Zilog and Exar, Rohm's U.S. subsidiary, will organize a joint development system and will exchange engineers.

NEC and Boeing

In February 1986, NEC agreed with Boeing to jointly develop a CMOS single-chip MCU for Boeing's DATAC (Digital Autonomous Terminal Access Communication System), which will be used in next-generation civil aviation aircraft, the 7J7 (Japan's YXX Project). The data system will feature two-way communication and a 1 megabit-per-second transmission speed. The 35mm square CMOS device will have more than 10,000 gates.

1986 Japanese Alliances

NEC and Oki Electric

In February 1986, NEC and Oki Electric announced a jointly developed CMOS version of an NMOS high-performance signal processor currently produced by NEC, with only one-fifth the power consumption of the MuPD7720. NEC began producing the MuPD77C20 and Oki Electric the MSM77C20 since April at a rate of 50,000 to 100,000 chips per month. The new processor is targeted at modems, voice recognition equipment, numerically controlled systems, and robots.

NEC and Zilog

In March 1986, NEC agreed to second-source Zilog's Z800 and Z8000 Series MPUs from mid-1986. Zilog was delayed in developing the two MPUs since it was developing a CMOS version of the Z800 and debugging the Z8000. Zilog is also expanding the Z800 Series MPUs.

NEC and Seiko Epson

In April 1986, NEC signed a second-source agreement with Seiko Epson for the V Series, NEC's original microprocessors. Seiko Epson initially will produce and ship the V20 and V30. NEC already has second-source agreements with Sony, Sharp, and Zilog.

TRON Project

In June 1986, eight Japanese companies (Fujitsu, Hitachi, Matsushita, Mitsubishi, NEC, NTT, Oki Electric, and Toshiba) formed the TRON Council (The Real-Time Operating Nucleus) to accelerate the development of proprietary 32-bit MPU technology and operating systems for next-generation microcomputers. Headed by Hitachi's Kazuo Kanahara, the project will develop three operating systems capable of handling Japanese and other foreign languages: B-TRON for office automation equipment, I-TRON for real-time industrial systems, and M-TRON for networking with distributed multiprocessors. Forty other Japanese companies have been invited to participate in the project.

Okaya & Co. and Intel Japan

In June 1986, Intel Japan signed a sales agency contract with Okaya & Co., a major high-technology distributor, to strengthen its user services in the factory automation market in the Nagoya area.

1986 Japanese Alliances

Hitachi and Zilog

In June 1986, Hitachi and Zilog signed a second-source contract for Hitachi's 8-bit CMOS MPU (HD64180). Under the contract, Zilog will market the Z80-compatible device under Zilog's own label (Z64180). The CMOS device integrates the Z80 MPU, peripheral circuits, and memory management, and is capable of addressing 512 Kbytes of memory. In July, Hitachi shipped its first MPUs to Zilog. Hitachi preserved software compatibility, making the 64180 instruction set a superset of the Z80. There are 12 new instructions, but the HD64180 is not fully hardware compatible with Zilog's Z80 peripherals. The hardware problem will be solved by future parts, the Z180 and HD180.

Mitsubishi Corp. and Semicon Systems

In June 1986, Mitsubishi invested ¥200 million ($1.2 million) in Semicon Systems, a sales agency of Intel Japan. Mitsubishi sent three directors, including a vice president and an auditor, to Semicon Systems, which changed its name to Dia Semicon Systems.

NEC and Sharp

In July 1986, NEC and Sharp agreed to cooperate in developing and producing peripheral LSIs for NEC's original V Series microdevices. NEC will provide its original peripheral LSIs to Sharp on an OEM basis, while Sharp will develop new LSIs for the V Series.

Fujitsu and Hitachi

In October 1986, the two companies announced that they will cooperate in developing a 32-bit MPU and peripheral LSI family based on the TRON architecture. The TRON chip to be jointly developed by the two companies will be 1.0- to 1.3-micron CMOS and will integrate 700,000 transistors. Data processing will operate at 6 mips at 20 MHz; the software is written in C language. The chip will support UNIX and I-TRON operating systems. Sample shipments are planned for late 1987.

Toshiba and Zilog

In December 1986, Toshiba and Zilog signed an extensive agreement giving Toshiba the right to insert the Z80 MPU and peripherals into its standard products and n-well CMOS megacell library (called Super Megacell Integration). Zilog retains the right to second-source any Toshiba-developed products. Both companies seek to develop "quick turn" standard products.

1986 Japanese Alliances

ASICs

Sony and LSI Logic

In February 1986, Sony and LSI Logic jointly agreed to share common specifications for fabrication and design, exchange gate array designs and mask sets, provide cross-foundry services, and jointly work on each other's fab lines.

Toshiba and LSI Logic

In February 1986, Toshiba reached an agreement with LSI Logic to establish wide-ranging cooperation on gate array sales in Japan. Toshiba will support Nihon LSI Logic as a second source, introduce LSI's CAD System (LDS) to its users, and support sales of the system. The two companies will jointly promote advertising activities and hold open technical seminars.

Ricoh and Panatech

In February 1986, Panatech Semiconductor agreed to market Ricoh's CMOS programmable devices and gate arrays as well as thermal printers in the United States. Both companies are closely affiliated since Ricoh acquired 15 percent of Panatech for $500,000 in April 1985. In November 1985, Panatech, Modular Semiconductor, and Ricoh signed a five-year agreement covering CMOS 16K SRAMs and 256K DRAMs.

Ricoh and VLSI Technology

In February 1986, Ricoh and VLSI Technology (VTI) of San Jose, California, strengthened their relationship. Ricoh will produce custom ICs for VTI's new Japanese subsidiary as well as buy custom ICs for use within Ricoh. VTI currently supplies mask ROM to Ricoh on an OEM basis.

Sharp, RCA, and Wafer Scale

In March 1986, Sharp entered a five-year alliance with RCA and Wafer Scale Integration (WSI) to cooperate on manufacturing and technology for high-performance CMOS ICs. (The RCA/Sharp joint venture was dissolved later in 1986 when RCA and GE merged.) Originally, WSI planned to combine its LSI macrocell library with those of RCA and to provide a multisourced advanced cell library. WSI licensed RCA and Sharp to manufacture WSI's high-speed EPROMs and MPUs. In addition, the companies had planned to cooperate on developing next-generation 1.0-micron cell libraries, advanced tools, packaging techniques, high-speed EPROMs, and other high-performance standard products. Sharp is now reconsidering its plans for the U.S. market.

1986 Japanese Alliances

Toshiba, Siemens, and General Electric

In March 1986, Toshiba and Siemens announced their plans to jointly develop standard cells using Toshiba's 1.5- to 1.2-micron CMOS process, and to become each other's second-source. Toshiba provided the standard cell designs, and Siemens the data on its design CAD software. Earlier, in July 1985, Toshiba agreed to supply 1Mb CMOS DRAM technology to Siemens.

In August 1986, this agreement was expanded when General Electric, Siemens, and Toshiba signed a five-year agreement to jointly develop 160 types of standard cells and to become mutual-source suppliers. Under the agreement, the companies will develop common standard cell libraries using Toshiba's 1.5-micron CMOS technology by early 1987, and plans to develop 1.2-micron standard cells. Siemens will supply the CAD software. Third ranked Toshiba had semiconductor revenue of more than $2 billion in 1986; number 16, GE/RCA, sold $459 million, and number 17, Siemens, sold $457 million.

Toshiba and Laser Path

In March 1986, Toshiba and Laser Path signed a joint development, fabrication, and marketing agreement covering Laser Path's gate arrays.

Seiko Epson and Siliconix

In March 1986, Seiko Epson entered an agreement to supply master wafers for gate array products to Siliconix of Santa Clara, California. Seiko Epson will complete 10 of the 14 to 16 wiring layers on Seiko's wafers. Delivery began in the spring of 1986. In the previous November, Siliconix licensed Seiko's 2.0- and 1.5-micron gate array production and CAD technology. Seiko-Epson also produces Xilinx logic cell arrays (LCAs).

Yokogawa H-P and Hewlett-Packard

In March 1986, Yokogawa H-P and Hewlett-Packard announced plans to jointly develop CAD system software for designing programmable logic devices (PLDs) and custom ICs. Three YHP System Lab engineers will be assigned to H-P's Colorado Springs division for 8 to 11 months. YHP's goal was to sell 50 to 60 PLD Development Systems in Japan in 1986.

Marubeni Corporation and LSI Logic

In April 1986, Marubeni Corporation signed a sales agency contract with LSI Logic Japan to enter the ASIC market. Marubeni opened a design center for LSI Logic in July, and is taking charge of part of LSI Logic's circuit design.

1986 Japanese Alliances

Tokyo Electron and Digi-Systems

In May 1986, Tokyo Electron (TEL) signed a marketing agreement to sell Digi-Systems' computer-aided engineering (CAE) workstations in Japan. The Personal Logician is a ¥4 million to ¥5 million ($25,000 to $31,250) workstation.

Mitsubishi and LSI Logic

In June 1986, Mitsubishi Electric agreed to provide foundry services for LSI Logic.

Ricoh and California Micro Devices

In June 1986, Ricoh received CAD technology from California Micro Devices, formerly Custom MOS Arrays (CMA), of Milpitas, California. Ricoh has provided silicon wafers to CMA since 1982, and has jointly developed CMOS gate arrays based on CMA's designs and Ricoh's 1.5-micron wafer process.

Ricoh and Silicon Compilers

In July 1986, Ricoh and Silicon Compilers (SCI) tied up to sell SCI's Genesil silicon compiler in Japan. Ricoh will provide SCI with manufacturing information on its CMOS n-channel ICs, which will be installed in the Genesil compiler for sale into the Japanese market. SCI customers will be able to have Ricoh produce custom ICs designed using Genesil. Soliton Systems will build a Genesil training center at its Shinjuku design center in Tokyo.

Okura & Co. and Xilinx

In August 1986, Okura & Co. signed a sales agency agreement with Xilinx of San Jose, California, to sell logic cell arrays (LCAs) jointly developed by Xilinx and Seiko Epson Corp, which formed their partnership in December 1985. Okura is receiving software for the circuit design. Annual sales are targeted at ¥4 billion to ¥5 billion ($25.3 million to $31.6 million) in the first year. The software was priced at ¥2 million ($12,658) per set.

Kyocera, ASCII, Mitsui & Co., and Chips & Technologies

In August 1986, Chips and Technology (C&T) of Milpitas, California, established a joint venture company capitalized at ¥500 million ($3.16 million) with Kyocera, ASCII Corporation, Mitsui & Co, possibly Yamaha, and one other Japanese company to develop ASICs. Although the investment ratio was not announced, C&T and ASCII are the largest

shareholders with equal shares. Gordon A. Campbell, C&T president, is chairman, and Kazuhiko Nishi, ASCII vice president, is president of the venture. Headquartered in Tokyo, the new venture company opened its doors in October and aims at ¥3 billion ($19 million) sales in the first year and ¥10 billion ($62.5 million) in the fourth year. The venture will design and develop dedicated LSIs for compact disk players, ISDN (Integrated Service Digital Network) equipment, and IBM-compatible personal computers. The LSIs will be supplied to personal computer and telecommunication equipment makers in Japan.

In December, ASCII established two subsidiaries to work with this new joint venture. A new sales company will be established with Mitsui Corp. to market memories for IBM-compatible computers. The R&D firm, Graphics Communications Technology, will specialize in image communications chips. It is financed 70 percent by the Key Technology Research Promotion Center and 11 companies, including Mitsui Corp., Iwasaki Communications, and Okura Electric.

Solitron Systems and Silicon Compilers

In October 1986, Solitron Systems signed a sales agency agreement to market Silicon Compilers' IC design software in Japan.

Kanematsu Semiconductor and Electrical Engineering Software

In October 1986, Kanematsu Semiconductor signed an agreement to market IC design simulation software produced by Electrical Engineering Software. First-year sales are targeted at $640,000 to $1.3 million.

Seiko-Epson and Lattice

In October 1986, Lattice Semiconductor of Beaverton, Oregon, entered a fabrication agreement with Seiko Epson for production of Lattice's programmable logic devices (PLDs), which are called Generic Array Logic (GALs). The devices will be fabricated at Seiko Epson's plant, shipped to Lattice's Oregon plant for inspection and testing, then assembled at Seiko Epson's Korean and Philippine plants. Lattice aims to capture 15 percent of the Japanese PLD market during 1987. In late 1986, Seiko Epson withheld wafer shipments until Lattice received funding to continue its operations.

Fujitsu and Arimura

In November 1986, Fujitsu signed a patent license agreement with Arimura Industrial Laboratories to enter the IC card market. Fujitsu will begin IC card production immediately and initially will target the U.S. market.

1986 Japanese Alliances

Sumitomo Metals and Standard Microsystems

In December 1986, Sumitomo Metal tied up with Toyo Microsystems (TMC), the Japanese subsidiary of Standard Microsystems Corporation (SMC). TMC recently increased its capital to ¥1.1 billion ($6.9 million) to accommodate Sumitomo's 20 percent investment of ¥220 million ($1.35 million). TMC will import and market SMC's ASICs into Japan in the spring of 1987, and will establish a Japanese design center by autumn of 1987. Devices will be produced initially by Sumitomo, but later by another Japanese semiconductor company. Sumitomo Metal will transfer 30 to 50 employees to Toyo, which will have a total investment of $13 million. SMC had $44.5 million in revenue for the year ending February 1986.

Sumitomo and Integrated Logic Systems

In December 1986, Sumitomo Corporation licensed ASIC design technology from Integrated Logic Systems (ILSI) of Colorado Springs, Colorado, in order to enter the semicustom IC market. In addition to receiving royalty payments, ILSI also has the right to use any foundries contracted by Sumitomo for its own production runs.

Standard Logic

Hitachi and Riken

In January 1986, Hitachi and Rikagaku Laboratories (Riken) announced they had jointly developed the Quantum Flux Parametron, an ultrahigh-speed switching element with a 50-picosecond switching speed and 1.8-GHz clock frequency. The new device can operate without electrical voltage and has a power dissipation of one-thousandth of that of a Josephson junction device.

Hitachi and Fairchild

In July 1986, Hitachi signed a five-year agreement to become the first alternate source for Fairchild's FACT (Fairchild Advanced CMOS Technology) logic. Fairchild gave Hitachi its design data base for 20 devices. Hitachi sampled its product in late 1986 and went into full production in early 1987 using Fairchild's trademark. FACT uses Fairchild's silicon-gate p-well process with a 1.3-micron channel length and double-level metal. Hitachi brings high-speed CMOS logic know-how. Fairchild is producing FACT at its South Portland, Maine, plant and will begin production in Nagasaki by mid-1987. Fairchild aims at developing 120 FACT devices by the end of 1987 and to have $500 million in FACT sales by 1990.

1986 Japanese Alliances

Marubeni Hytech and Fairchild

In August 1986, Fairchild named Marubeni Hytech as an agent to sell its fast TTL logic and FACT CMOS logic in Japan. Eventually, Marubeni will also handle gate arrays and standard cell products.

Mitsubishi and Texas Instruments

In December 1986, Mitsubishi Electric and Texas Instruments agreed to mutually supply logic ICs on an OEM basis. TI will supply high-speed bipolar TTLs; Mitsubishi will ship low-power CMOS logic. TI is the world's leading TTL supplier, while Mitsubishi is Japan's second largest TTL supplier after Hitachi (check market shares).

Other Devices

Toshiba and Intel

In March 1986, Toshiba signed a fab and sales contract to provide Intel with two multibus II-compatible interface ICs. The parallel system bus interface IC MPC generates and receives interrupt messages from ICs in a multibus board; it is a CMOS device in a pin-grid array and a 149-pin package. The bit-bus interface IC BBC is capable of two-cable transmission up to 10km; it is a CMOS device in a 64-pin PLCC package. Toshiba, the only BBC producer worldwide, began producing the BBC at a rate of 300,000 chips in April 1986. Toshiba is the only Japanese company making the MPC.

Sony and Sharp

In June 1986, Sony and Sharp announced an agreement on laser diode standards for compact disks, video disk players, and other consumer equipment. The standard involves a new diode incorporating a 5.6mm diameter laser generator, 2.0mm lead pin pitch, and 1.35mm base-to-chip distance. The two firms dominate more than 70 percent of the consumer laser diode market. They produce independently developed ultrasmall laser diodes at a monthly rate of 200,000 units.

NEC and Compass Systems

In May 1986, NEC and Compass Systems announced a jointly developed IC for use in low-cost local area network (LAN) systems.

Chronix and Matra-Harris

In July 1986, Chronix signed a sales agency agreement to market Matra-Harris Semiconducteurs' image processing LSIs in Japan.

1986 Japanese Alliances

NEC and Tokyo Sanyo

In August 1986, NEC and Tokyo Sanyo signed a five-year mutual second-source agreement covering linear ICs for television receivers. Tokyo Sanyo will second-source NEC's television voice multiplex stereo demodulator chip (MuPC1480) and DBX noise reduction decoder (MuPC1481). NEC will second-source Tokyo Sanyo's TV image/voice IF IC (LA7530) and television vertical output amplifier IC (LA7381). Second-source supply of these ICs began in late 1986.

Hitachi and Signetics

In August 1986, Hitachi acquired manufacturing and sales licenses from Signetics for two telecommunication LSI models (HD68562 and HD64941) for transferring data between terminals and mainframe computers. Hitachi aims to strengthen peripheral LSIs for its 16-bit MPUs. Sampling began in August and mass production in November.

Teksel and Anadigics

In August 1986, Teksel signed a sales agency contract with Anadigics of Warren, New Jersey, to sell gallium arsenide ICs. Under the contract, Teksel is responsible for marketing a superwideband amplifier (ADA25001) and an operator amplifier (AOP1510).

Matsushita and Philips

In August 1986, Philips entrusted Matsushita Electronics to produce LSIs for Philips' compact disk players.

Rikei and Adams-Russell

In October 1986, Rikei signed a sales agency agreement to market GaAs ICs and telecommunications equipment components produced by Adams-Russell of Waltham, Massachusetts.

Hamamatsu Photonics and City University of New York

In October 1986, Hamamatsu and City University of New York (CUNY) established a joint Photo-Technology Applications Laboratory (PAL) at CUNY to develop optoelectronic systems and devices.

1986 Japanese Alliances

Oki Electric and Silicon Systems

In October 1986, Oki Electric established a partnership with Silicon Systems of Tustin, California, to produce 1,200-bps, duplex operation, single-chip modem LSIs. Oki will produce and market in Japan six models developed by Silicon Systems. Quantity production, which began in December at a monthly rate of 50,000 units, will be increased to 100,000 units in March 1987.

Stanley Electric and Kyokuto Trading

In November 1986, Stanley Electric formed a joint venture in Battle Creek, Michigan, with Kyokuto Trading Company to produce automotive electronic components. The company is 60 percent owned by Stanley, 30 percent by Kyokuto, and 10 percent by Stanley Electric U.S. Stanley is a major supplier of bright LEDs to Japanese auto makers.

Equipment

Citizen Watch and Perkin-Elmer

In January 1986, Citizen Watch and Perkin-Elmer announced plans to form a joint venture company, Perkin-Elmer Citizen, to manufacture Perkin-Elmer semiconductor processing equipment. The new venture is capitalized at ¥100 million ($625,000), with Perkin-Elmer contributing 60 percent and Citizen Watch 40 percent. The company has its head office in Citizen Watch's plant in Torokozawa City, Saitama prefecture. Initially, the company will produce Perkin-Elmer's step-and-repeat alignment systems and dry-process etching systems. Perkin-Elmer Japan will sell the products throughout Asia. John Suzuki, president of Perkin-Elmer Japan, will also head Perkin-Elmer Japan SA.

Marubeni Hytech and Ion Beam Technology

In April 1986, Marubeni Hytech invested $1.2 million in capital in Ion Beam Technology Corporation (IBT) of the United States, in exchange for 12 percent of IBT's stock. Ichitaro Kimura, president of Marubeni Hytech, was installed as an executive member of IBT. Marubeni plans production of IBT's equipment in Japan within three years.

Fuji Electric and Cambridge Instruments

In May 1986, Fuji Electric and Cambridge Instruments formed a joint venture, Fuji Cambridge Instruments K.K., to market semiconductor equipment, electron microscopes, and other products. Each company contributed half of the ¥300 million ($1.9 million) in capital. The

venture aims to replace gallium arsenide and other crystal-raising equipment and metalized organic chemical vapor deposition (MOCVD) systems with a high-level (20 wafers per batch) wafer processing system. By introducing Cambridge's technology, Fuji will produce single-crystal pulling equipment and MOCVD equipment at its Kawasaki plant in 1987. Cambridge Instruments K.K., formed in August 1983, changed its name to Fuji Cambridge Instruments K.K.

RHD and Gakei Electric

In May 1986, RHD Inc., an R&D firm, and Gakei Electric Works, a high-voltage electric furnace maker, jointly developed an InP/GaAs single-crystal pulling machine. The companies began test manufacturing single-crystal wafers and will market the equipment in two years. RHD may establish a new firm in the future with its three investors: Nisshin Steel Co., Toyo Ink Manufacturing, and Mitsubishi Corporation.

NEC and JEOL

In June 1986, NEC and JEOL announced that they had jointly developed a focusing ion beam machine (JIBL-150) capable of IC circuit pattern writing, resist exposure in the submicron domain, direct etching on wafers, and implanting without using masks. JEOL plans to sell the machine to IC makers and universities as a tool to develop IC manufacturing technology.

Hitachi and Toyohashi University

In June 1986, Hitachi Works and Toyohashi Technology and Science University announced a hybrid electron/ion beam manufacturing equipment prototype jointly developed since 1983 under the auspices of the Ministry of Education's R&D program.

ULVAC BTU and Seiko Instruments

In July 1986, ULVAC BTU and Seiko Instruments & Electronics jointly developed an experimental clean room robot, and plans to commercialize it by early 1987.

Hitachi and Nippon Telegraph & Telephone (NTT)

In July 1986, Hitachi announced a direct-write electron beam machine capable of writing 0.1-micron circuit patterns on a wafer at a rate of one hour per wafer. The machine (EB-F) was jointly developed with NTT's Atsugi Laboratory, which is developing next-generation VLSIs (64Mb DRAMs and 3-D ICs) and ultrahigh-speed gallium arsenide ICs. Hitachi plans to market the machine in the second half of 1987.

1986 Japanese Alliances

ULVAC Group and Inabata

In August 1986, the ULVAC Group, including Vacuum Metallurgical and Inabata & Co., jointly established a sales company called I.H.T. Corporation in Silicon Valley, California, to market electronic materials, including vacuum equipment. The new company is capitalized at ¥400 million ($2.6 million), 70 percent owned by the ULVAC Group and 30 percent by Inabata.

Napson and Keithley Instruments

In September 1986, Napson Corporation signed a sales agency agreement with Keithley Instruments of Cleveland, Ohio, to market Keithley's silicon wafer electrical resistance measuring equipment in Japan. Napson, a Tokyo semiconductor manufacturing and testing equipment maker, hopes to sell 50 systems in 1987.

Mitsubishi Corporation and Nihon MRC

In October 1986, Mitsubishi Corporation announced plans to invest capital in Nihon MRC, a subsidiary of Materials Research Corporation (MRC) of the United States, and to market MRC's semiconductor manufacturing equipment in Japan. Mitsubishi will buy 25 percent of Nihon MRC's total stock, and start selling MRC's ion etching and sputtering equipment through MC Electronics, a sales company established jointly with Mitsubishi Chemical Industries. Mitsubishi will also work with MRC to sell semiconductor materials.

Shinkawa and KLA Instruments

In October 1986, Shinkawa and KLA Instruments announced a jointly developed IC wire bond quality monitor for the Japanese and U.S. markets. The monitor uses three-dimensional image analysis technology to inspect ICs after wire bonding. KLA will handle production, while Shinkawa will handle sales.

Toshiba and Tokuda Works

In December 1986, Toshiba and Tokuda Works announced a jointly developed fully automated reactive ion etching system (HIRRIE-500) that can handle ultranarrow geometries of less than 0.5 microns. The new etcher can process 8-inch to 10-inch wafers at a rate of 20 wafers per hour. Eventually, the system will be used to fabricate memories up to 64Mb. The system, which is priced at ¥92 million ($575,000), will be available in the spring of 1987.

1986 Japanese Alliances

Materials

Fujikura and CTS Corporation

In January 1986, Fujikura and CTS Corporation of Elkhart, Indiana, signed a joint technology agreement to develop porcelainized steel substrates for thick-film hybrids. CTS will share its metal and conductive paste technology with a near-zero sodium content porcelainized steel from Fujikura. CTS supplies prototype thick-film circuits on steel substrates. Near-term applications include automotive electronics and military equipment. In May 1986, the two companies formed a joint venture to manufacture ceramic-processed printed circuit boards.

Matsushita, Hayashibara, and Japan Compound Gum

In February 1986, Matsushita Denso and Hayashibara Biochemical signed a production contract to have Japan Compound Gum produce water-soluble photoresist (WSP), a new material for sub-micron (0.6- to 0.7-micron) patterns required for 4Mb DRAMs and above. The photoresist can be used with i-line and g-line steppers. Japan Compound Gum will supply the photoresist to Matsushita Electronics. Matsushita Denso and Hayashibara, which jointly developed WSP, will supply production technology.

Kyocera and Wacker Chemitronic

In February 1986, Kyocera licensed technology from Wacker Chemitronic GmbH to produce polycrystal silicon ingots for making solar battery cells. Wacker's Silso casting method involves melting metallic silicon material in a casting furnace at 1,500°C. Kyocera currently produces silicon solar cells through its subsidiary, Japan Solar Energy.

Mitsubishi, Dai Nippon, Hoya, Toppan, and ULVAC Coating

In June 1986, Mitsubishi Electric's LSI Development Laboratory provided Dai Nippon Printing, Hoya, Toppan Printing, and ULVAC Coating with photomask manufacturing technology using molybdenum silicide. Contract terms were not disclosed, but the four companies will pay contract fees and royalties based on their production volumes.

Hitachi and Monsanto

In July 1986, Hitachi agreed to share its silicon wafer manufacturing technology with Monsanto. Under the agreement, Monsanto will send wafer engineers to Hitachi to acquire the technology necessary to manufacture products to meet Hitachi's standards. Hitachi will send engineers to the United States as needed. By giving Monsanto its manufacturing technology, Hitachi plans to increase its wafer imports from the United

States. Monsanto, which aims at acquiring 10 percent of silicon wafer starts in Japan, plans to increase silicon wafer production at its Utsunomiya plant in Tochigi prefecture by five times, and to produce 5 million wafers per year by autumn of 1987.

Shinkawa and Superwave Technology

In August 1986, Superwave Technology of Santa Clara, California, licensed its patented process for curing epoxies and polyimides. Superwave will provide documentation on its microwave-assisted curing (MAC) process and several Supertherm-1EC systems, in exchange for royalties. Founded in 1983, Superwave offers the Supertherm-1M for hybrid chips and the automated Supertherm-1EC for in-line applications.

Dai Nippon Printing and Perkin-Elmer

In August 1986, Dai Nippon Printing and Perkin-Elmer announced a joint project to develop photomasks for X-ray lithography systems aimed at the 16Mb and 64Mb memory market.

Mitsubishi Corporation, Nisshin Steel, and Toyo Ink

In September 1986, RHD, an R&D venture formed by Mitsubishi Corporation, Nisshin Steel, and Toyo Ink, developed a Bridgeman method for growing zinc selenide monocrystals, a material for blue LEDs.

Asahi Glass and Olin

In October 1986, Asahi Glass and Olin Corporation (U.S.) established a joint venture, Olin-Asahi Interconnect Technologies, in Stratford, Connecticut, to process and market alumina and ceramic substrates for use in thick-film hybrid ICs. Olin-Asahi is using Asahi's technology. Initially, the substrates are being fired at Asahi's plant, with custom finishing done at Olin-Asahi's Connecticut plant. Olin Interconnect Technologies, another new firm, will market the substrates and ceramic specialties. Production began in November. A U.S. manufacturing complex will be built within two years. Olin and Asahi have operated a joint venture in Japan since 1974 to produce urethane polyol chemicals. The two companies, which invested $800,000 in the venture, have an annual sales target of $30 million within three to four years.

Mitsubishi and Nihon MRC

In October 1986, Mitsubishi Corporation invested in Nihon MRC for 25 percent ownership. Nihon MRC produces ion etchers and sputterers at its Oita plant.

1986 Japanese Alliances

Asahi Denka and Union Carbide

In November 1986, Asahi Denka Industries teamed up with Union Carbide Japan to produce and market an ultraviolet-cured epoxy resin in Japan. Union Carbide, which developed the resin, will import the resin for processing by Asahi Denka. The resin is a sealing agent for electronics equipment.

UPDATE ON EXISTING ALLIANCES

NEC and Corvus

In November 1985, NEC and Corvus Systems of San Jose, California, announced a joint development program to develop single-chip controllers. In February 1986, the two firms announced the world's first CMOS single-chip controller (MuPD72015) for the Omninet local area network (LAN) originated by Corvus. The 1.6-micron device has a 4-Mbps data transmission speed and can address up to 16 Mbytes of memory space because it incorporates a DMA controller with a 24-bit address bus. Mass production began in July 1986 at a rate of 10,000 chips per month.

Kanematsu Semiconductor and Anicon

In February 1986, the two companies reached an out-of-court settlement concerning Anicon's charge that Kanematsu had improperly used information on Anicon's chemical vapor deposition (CVD) system. Kanematsu agreed to pay $25,000 and refrain from selling Anicon-type CVDs for 18 months. (In March 1984, Anicon had dissolved its sole agency contract with Kanematsu and signed a new contract with Sumitomo.)

Asahi Chemical and Gould AMI

In July 1986, Asahi Chemical and Gould AMI canceled plans to build a $100 million CMOS fabrication plant in Japan, due to the semiconductor slump and Gould's $160 million second-quarter write-off.

Oki Electric and Voest Alpine

In July 1986, Oki Electric terminated its talks with Voest Alpine to form a joint VLSI manufacturing venture, due to financial problems at Alpine. (In March 1986, Oki Electric and Voest Alpine of Austria had

resumed negotiations to establish a joint venture in Austria to produce VLSIs, including 256K DRAMs. Negotiation talks began in May 1985, but were called off due to financial problems at Alpine, which elected a new board of directors.)

NMB Semiconductor and Vitelic

In August 1986, NMB Semiconductor began shipping samples of Vitelic's CMOS 1Mb DRAMs, which feature 1.2-micron design rule and a 77ns access time. A 60ns version was sampled in late 1986.

Sharp and RCA

In August 1986, Sharp dissolved its agreement with RCA to establish a joint manufacturing venture for ASICs, DRAMs, 256K SRAMs, high-density EPROMs, EEPROMs, and 32-bit MPUs. The two companies had planned to build a $250 million fabrication plant in Camas, Washington. GE, which bought RCA for $6.2 billion, already runs 2.0-micron CMOS and has a prototype 1.25-micron CMOS line, making the new plant redundant. Sharp is reconsidering its U.S. facility plans. Dataquest notes that Wafer Scale Integration (WSI) of Fremont, California, originally signed up in March 1986 with the RCA/Sharp joint venture, and could be Sharp's new partner.

Sharp and Texas Instruments

In August 1986, Sharp and Texas Instruments reached an out-of-court settlement regarding Sharp's alleged patent violation of TI's DRAM technology. Sharp agreed to pay an undisclosed licensing fee to TI. (Eight other Japanese companies and one Korean company are involved in lawsuits, including Hitachi, NEC, and Toshiba.)

Fuji Electric and Siemens

In December 1986, Fuji Electric and Siemens expanded their existing tie-up in semiconductors, sensors, communications, and factory automation. The two firms will exchange information and products. Fuji Electric will supply sensors and industrial-grade semiconductors; Siemens will provide communications equipment and information systems.

1985 Japanese Alliances

SUMMARY

Marry and conquer! For years, Japanese executives have cemented their business and political ties in Japan through strategically arranged marriages. The nakodo, or professional matchmaker, was the key to this family-style approach to business. Today, Japanese companies are using a similar approach--strategic alliances--to build long-term ties with foreign companies. They are exchanging researchers, sharing technology and plant capacity, and developing new markets with their partners overseas. The emphasis is on building close, family-like relationships. Toshiba's assignment of Dr. Yoshio Nishi to Hewlett-Packard's VLSI Research Lab, Oki Electric's joint venture with Voest Alpine, and the participation of Kyocera's president, Kazuo Inamori, on Vitelic's board are examples of these growing ties.

As shown in Table 1, Japanese companies entered into a record 71 joint ventures and licensing agreements in 1985. Of these, 50 were with U.S. companies, 10 with European companies, 2 with Korean companies, and 9 with other Japanese companies. Significantly, there were 27 joint ventures between Japanese semiconductor makers, more than twice the number in 1984. We believe that stagnant markets, increasing competition, worldwide overcapacity, and growing protectionism are fueling the Japanese push toward joint ventures.

Table 1

JAPANESE SEMICONDUCTOR STRATEGIC ALLIANCES

	1980	1981	1982	1983	1984	1985
Semiconductor Makers						
Joint Ventures	1	1	5	3	11	32
Licensing Agreements	2	5	5	11	19	22
Equipment Manufacturers	0	5	12	8	26	17
	3	11	22	22	56	71

Source: Dataquest
April 1987

THE SEARCH FOR IDEAL PARTNERS

In the past, Japanese strategic alliances were primarily limited to technology transfers and marketing agreements. In 1985, however, we observed a pronounced shift toward more complex and varied agreements. Japanese companies are systematically entering alliances to diversify their product portfolios, exchange technologies, penetrate markets, and utilize excess plant capacity. They are parlaying their strengths--

memory technologies and CMOS wafer processing--in exchange for MPU support systems, CAD systems, and advanced IC designs. Companies like Fuji Electric, NMB Semiconductor, Oki, Ricoh, Seiko, and Sony are using their CMOS processing capabilities as a springboard into technology sharing and joint product development agreements. For many Japanese companies, the ideal partner is a company with leading-edge designs that is seeking low-cost wafer fab capacity.

Japanese semiconductor makers are also mixing their strategies. For example, Hitachi, NEC, and Toshiba are second-sourcing MPUs while jointly designing CAD systems for their proprietary MPUs with other companies. Exar, Seiko, and Sony are investing in or acquiring U.S. start-ups and offering wafer fab capacity. Some companies are simultaneously moving into several new areas. As shown in Table 2, Toshiba was the most active in 1985, signing 12 agreements covering a broad range of products.

The ground swell of strategic alliances has only begun. Because of the growing Japanese interest in Europe, and the coming shakeout in ASIC, CAD, and IC start-up companies, we believe that we will see more strategic alliances between Japanese companies in 1986. As shown in Table 3, there were 10 alliances with European companies in 1985, up from 2 in 1984.

Table 2

1985 JAPANESE STRATEGIC ALLIANCES BY COMPANY

Company	Number	Company	Number
Toshiba	12	Ricoh	3
Hitachi	7	NTT	3
NEC	5	Seiko Group	3
Oki Electric	6	Matsushita	2
Sony	4	Fujitsu	2
Mitsubishi	3	Rohm	2

Source: Dataquest
April 1987

1985 Japanese Alliances

Table 3

1985 JAPANESE STRATEGIC ALLIANCES
BY COUNTRY AND PRODUCT AREA

	United States	Europe	South Korea	Japan	Total
Memory	7	4	-	-	11
Process	3	-	-	-	3
Microprocessors	10	2	-	4	16
ASICs	8	-	-	1	9
Other Devices	9	3	1	2	15
Equipment	13	1	1	2	17
Total	50	10	2	9	71

Source: Dataquest
April 1987

The Rush Toward Product Groupings

We have observed that Japanese companies are forming major product groupings, or "camps," with U.S. and European makers to establish themselves worldwide. The race to find partners before being locked out of these camps is especially fierce. In 1985, we noted the following trends:

- Japanese newcomers are offering CMOS wafer fab capacity in exchange for design technology (NMB Semiconductor/Vitelic, Fuji Electric/Mosel, Seiko Epson/Xilinx/Siliconix, Rohm/Zilog, Kawasaki Steel/Nihon LSI).

- New groupings are being formed around shared product families (Sony/NMB/Vitelic, Oki/Voest/Thomson CSF/Siemens, Fuji/Mosel, Sharp/Wafer Scale Integration, Hitachi/Motorola, NEC/Sharp/Sony/Zilog, Fujitsu/Intel).

- Japanese companies are signing up with Japanese partners, an indication of their growing confidence in domestic technology and willingness to cooperate (Kanebo/Mitsubishi, Matsushita/Hayashibara, NEC with Sharp/Oki/Sony, Casio with NEC/Oki/Hitachi, Mitsubishi/Tokyo Electron).

1985 Japanese Alliances

- Japanese-European alliances are on the rise because of Japanese interest in European markets and creative research (Oki/Thomson CSF, Toshiba/Siemens, Oki/Voest, Hitachi/Thomson CSF, Kobe Steel/Trefimetaux, Toshiba/SGS-Ates, Matsushita/Philips, Canon Sales/CIT-Alcatel).

- Japanese-U.S. alliances are heavily focused on microprocessor second-sourcing (10 alliances), joint ASIC development (8), and equipment joint ventures (13).

- Despite strong rivalry, Japanese-Korean ties are emerging because of cost pressures and the growing U.S.-Korean alliance (Ricoh/Hyundai, Toshiba/Pohang Jonghup Steel, Sharp/Samsung).

Overall, it appears that Japanese companies are using strategic alliances to blunt the wave of protectionism that threatens their overseas markets, an approach pioneered by Japanese automobile makers. We believe that this is the wave of the future in semiconductors. In February, we will issue a service section covering trends in Japanese strategic alliances from 1980 through 1985.

Mergers and Acquisitions--The Opening Gambit?

Although Japanese companies are not noted for actively acquiring new companies, we believe that they will look at struggling U.S. start-ups as possible sources of leading-edge technology. Oki's licensing of Exel's EEPROMs and Exar's subsequent acquisition of Exel are cases in point (see Table 4). On the other hand, U.S. equipment makers are buying out their partners to establish majority-owned Japanese subsidiaries.

Table 4

1985 JAPANESE SEMICONDUCTOR MERGERS AND ACQUISITIONS

Date	Japanese	Foreign	Activity
12/85	Exar (Rohm)	Exel	Exar offer to acquire Exel; Exar to exchange $5.7 million in newly issued stock for common and preferred stock held by Exel shareholders; Exel has 5.7 million shares of stock outstanding; agreement awaiting approval of Exel shareholders
12/85	Midoriya	Materials Research	MRC to buy four-fifths of Midoriya's 20 percent stock in 1986, bringing MRC ownership to 98 percent
10/85	Anelva Corp.	Varian	Varian sold remaining 19 percent share of Anelva to NEC, which now owns Anelva completely, ending 18-year joint venture
05/85	Toshiba	Olivetti	Toshiba bought 20 percent of Olivetti Japan to become stragegic supplier to Olivetti

Source: Dataquest April 1986

1985 Japanese Alliances

Memory Alliances: Trading CMOS DRAMs for New Designs

There were 11 alliances in memory technology (15 percent of all alliances) in 1985. Japanese companies were primarily interested in start-up companies like Exel, Mosel, Vitelic, and Wafer Scale Integration and in large European makers like Siemens, Thomson CSF, and Voest. The hottest technologies were CMOS 256K and 1Mb DRAMs, EEPROMs, and 64K SRAMs. As shown in Table 5, Oki, Toshiba, and Vitelic were the most active companies. An interesting team is being formed by Vitelic (design), NMB Semiconductor (automated CMOS wafer fab), Sony (investor in Vitelic and potential OEM), and Taiwan's Electronic Research and Service Organization (Vitelic's other wafer supplier).

Table 5

1985 JAPANESE MEMORY STRATEGIC ALLIANCES

Date	Japanese	Foreign	Agreement
11/85	NMB Semi-conductor	Vitelic	Vitelic to license CMOS 1Mb DRAM technology for one-third NMB plant capacity; NMB licensing 64K SRAM from another U.S. firm; NMB Class 1 fab to ramp up to 4 million chips monthly by late 1986
10/85	Sony	Vitelic	Sony invested $2 million of $7 million second-round financing package; Sony seat on board; potential technical, production, and OEM ties in future
10/85	Fuji Electric	Mosel	Fuji to produce CMOS 64K SRAMs for Mosel under OEM contract using Mosel's 1.5- to 2.0-micron CMOS process; Fuji to also develop custom CMOS LSIs; $74 million Fuji semiconductor investment in 1985 for plant and technology
10/85	Sharp	Wafer Scale Integration	Expansion of 1984 agreement; WSI's 1.6-micron CMOS technology offered for royalties and plant capacity
09/85	Oki	Thomson CSF	Oki to supply 64K and 256K DRAM technology to Thomson's Marseille plant

(Continued)

1985 Japanese Alliances

Table 5 (Continued)

1985 JAPANESE MEMORY STRATEGIC ALLIANCES

Date	Japanese	Foreign	Agreement
09/85	Toshiba	Siemens	Siemens to second-source Toshiba's CMOS 1Mb DRAM; broad-ranging 7-year agreement to include technology sharing and joint development of new devices; production at Siemens' Furth plant from late 1986; strong impact on Siemens/ Philip 4Mb Mega Project
09/85	Toshiba	Hewlett-Packard	Dr. Yoshio Nishi, manager of Toshiba's 1Mb DRAM team, assigned to head HP's VLSI Research Center for 3 years
07/85	Sony	Vitelic	Joint development of CMOS 256K, 1Mb DRAMs, and 4Mb DRAMs; assembly and testing by Vitelic; Vitelic to buy 5,000 wafers monthly from Taiwan's Electronics Research Service Organization (ERSO); Sony planning 1.5-micron 256K DRAMs; ICs to become 20 to 30 percent of Sony's revenues in future
06/85	Oki	Voest Alpine (Austria)	Joint venture to produce 256K DRAMs, Voest MPUs, and gate arrays; overall deal worth $285 million; venture capitalized at $2 million; 51 percent Oki, 49 percent Voest Alpine; Voest has similar venture with Gould AMI (Austrian Microsystems International)
05/85	Oki	Thomson CSF	Oki to supply VLSI assembly line to new Thomson plant in Maxeville, France, and a wafer fab to line at the Eurotechnique plant in Rousset, France
03/85	Oki	Exel	Oki to produce and market Exel's 16K EEPROMs worldwide

Source: Dataquest
April 1987

1985 Japanese Alliances

CMOS Processes: The Key to the INS Computer

One of the major announcements in 1985 was NTT's decision to work with Motorola and Texas Instruments. As shown in Table 6, both companies will work on CMOS processes and VLSI substrates for the INS computer, artificial intelligence, and satellites. We believe that NTT will sign more agreements in 1986 under its Track III procurement procedures (joint R&D), and possibly open R&D centers in Silicon Valley and Europe. As a result of NTT's privatization and of deregulation of the value-added network (VAN) market, NTT is under pressure to keep ahead of its new rivals in the NTT family--Fujitsu, NEC, Oki, Toshiba, and others. To avoid being sold old technology by the NTT family, NTT is now working with foreign companies and licensing its technology through NTech, its subsidiary. Recently, NTT teamed up with IBM and AT&T to develop joint VANs, a move that upset Japanese computer and telecommunications makers. For U.S. and European companies, the new NTT is one of the best potential partners because of its strong R&D labs and $3.2 billion procurement budget.

Table 6

1985 JAPANESE PROCESS TECHNOLOGY TRANSFERS

Date	Japanese	Foreign	Technology Transferred
11/85	NTT	Motorola, Texas Instruments	2- to 3-year joint development of LSI substrates for INS computer, artificial intelligence, and satellites
10/85	NTT	Texas Instruments	Joint development of buried oxide technique for 1.25-micron CMOS devices with 2-layer metal interconnect; potential TI qualification for DOD's VHSIC Phase I program
02/85	Mitsubishi	Standard Microsystems	Global nonexclusive cross-licensing of each other's semiconductor patents and patent applications; Mitsubishi is sixth Japanese vendor to license SMC coplamos process

Source: Dataquest
April 1987

1985 Japanese Alliances

Microprocessors: Laying the Groundwork

Japanese companies were busy laying the groundwork in 1985 for their assault on microprocessor markets, especially the 32-bit market, in 1987. As shown in Table 7, NEC was the most active, licensing its V Series to Oki, Sharp, Sony, and Zilog. In 1984, NEC teamed up with Digital Research, Hewlett-Packard, Sophia Systems, Tektronix, and Yokogawa to design MPU development support systems. The Sony/Tektronix system, which handles Intel, Motorola, and NEC MPUs, was recently introduced in Japan.

Hitachi is not sitting on its hands. In 1985, it exchanged MPUs with Motorola, Signetics, and Thomson CSF and is developing an MPU development support system with Sophia Systems.

Toshiba is hedging its bets. It signed agreements in 1985 to second-source Intel interface controllers and to develop an operating system with Zilog. In 1984, Toshiba signed agreements with Zilog and Motorola.

Surprisingly, Fujitsu and Mitsubishi have been very quiet. In 1984, Fujitsu negotiated with Intel to take partial charge of 16/32-bit MPU development, but no announcement has yet been made. Mitsubishi may work with Hitachi and NEC on Tokyo University's TRON Project for 32-bit MPUs.

Table 7

1985 JAPANESE MICROPROCESSOR STRATEGIC ALLIANCES

Date	Japanese	Foreign	Agreement
12/85	NEC, Sharp	----	Sharp to 2nd-source NEC V Series (V20/V30); Sony also NEC 2nd-source
12/85	NEC, Oki	----	Announced jointly developed CMOS signal processor (NEC uPd77C20, Oki MSM77C20) for shipment to U.S. in 1986
12/85	Matsushita	Philips	Matsushita to 2nd-source Philips' 68070
11/85	Toshiba	Intel	2nd-sourcing of Intel MOS interface LSIs (bus and interruption controllers)

(Continued)

1985 Japanese Alliances

Table 7 (Continued)

1985 JAPANESE MICROPROCESSOR STRATEGIC ALLIANCES

Date	Japanese	Foreign	Agreement
11/85	Rohm	Zilog	Long-term joint manufacturing and marketing agreement; Zilog MPUs (Z8/Z80) for Rohm's assembly and use (ROHMZ80)
10/85	Hitachi	Motorola	Both firms announced 2-micron HCMOS version of 68000; Hitachi mask sets for Motorola 2nd-sourcing
10/85	NEC	Zilog	NEC negotiating OEM agreement to supply V20/V30
10/85	Hitachi	Thomson CSF	2nd-sourcing of Hitachi's CMOS 8-bit MCU (6300 Series) in exchange for Thomson's telecommunication LSIs
09/85	Toshiba	Zilog	Sales contract for CP/M 8000 operating system for Z80 MPU; Toshiba to market OS with C compiler
09/85	Hitachi	Signetics	Hitachi's CRT controller (63484) for Signetics' data exchange IC (68562)
09/85	Fujitsu	Intel	Extension of 2nd-sourcing of 80286 MPU to include 80186/80188 and 82288 bus controller and 82284 clock generator
08/85	Hitachi	Microtec Research	Microtec to develop macroassembler, utilities, Pascal and C compilers to run on Hitachi's first standalone in-circuit emulator (H180AS01 Adaptive System Emulator) for the HD64180 8-bit CMOS MPU; HD64180 MPU compatible with Z80/8080 family
03/85	Rohm	Fairchild	Fairchild licensed manufacturing and sales rights of its 8-bit one-chip MCU (F3870 series)

(Continued)

1985 Japanese Alliances

Table 7 (Continued)

1985 JAPANESE MICROPROCESSOR STRATEGIC ALLIANCES

Date	Japanese	Foreign	Agreement
02/85	Sony	Tektronix	Tektronix designed MPU development support system for NEC V Series
01/85	NEC, Sony	----	2nd-sourcing of NEC's V20/V30 MPUs
01/85	Hitachi, Sophia Systems	----	Joint manufacturing of MPU development support system for Hitachi proprietary MPUs; joint commercialization of software development tool and program development emulator in late 1985

Source: Dataquest
April 1987

ASICs: The Battle Lines Are Forming

Japanese companies signed nine agreements for application-specific ICs (ASICs) in 1985, as shown in Table 8. Kawasaki Steel, LSI Logic, and Toshiba were clearly the most aggressive. LSI Logic and Toshiba renewed their ties to develop 50,000- to 60,000-gate "Sea of Gates" technology; Kawasaki Steel and Nihon LSI Logic are building a new CMOS plant. In 1984, Kawasaki Steel acquired silicon producer NEK Corporation, of Santa Clara, to obtain wafer processing know-how. The big question is whether LSI Logic will build its ties with Hewlett-Packard through Toshiba's Dr. Nishi.

The Seiko Group and Casio are quietly building ties of their own. Seiko Epson signed agreements with Xilinx and Siliconix, and Suwa Seikosha has ties with start-ups Applied Micro Circuits (AMCC) and SMOS System. Casio, which uses ASICs for its own products, will have Hitachi, NEC, and Oki produce its custom LSIs.

As a result of numerous joint ventures and licensing agreements, six major ASIC camps are forming. As shown in Table 9, these camps include LSI Logic, TI/Fujitsu, Fairchild/VLSI Technology, Gould/AMI, Motorola/National, and Seiko/Honeywell. Not all companies in each camp are related, but they often share mutual ties with other companies in the group.

1985 Japanese Alliances

Table 8

1985 JAPANESE ASIC STRATEGIC ALLIANCES

Date	Japanese	Foreign	Agreement
12/85	Toshiba	LSI Logic	Expansion of agreement for wide-ranging cooperation; Toshiba 2nd-sourcing, joint PR and technical seminars; LSI's CAD system for Toshiba ASIC users
12/85	Ricoh	Western Design Center	WDI's 16-bit CPU core to be input into Ricoh's standard cell library; Ricoh to supply devices through OEM deal
12/85	Seiko Epson	Xilinx	Seiko to produce Xilinx logic cell arrays; sample shipments in spring 1986
11/85	Seiko Epson	Siliconix	Siliconix to license Seiko's 2.0- and 1.5-micron gate array production and CAD technology
11/85	Fujitsu, Toshiba	Chips & Technologies	C&T subcontracting with Fujitsu and Toshiba for CMOS and bipolar arrays
10/85	Toshiba	LSI Logic	Joint development of 50,000-gate "Sea of Gates" for sale in 1986; Toshiba's CMOS process and LSI Logic's logic, simulation, and CAD software
09/85	Kawasaki Steel	LSI Logic	Joint venture company (Nihon LSI) to produce gate arrays and standard cells; 55 percent LSI Logic, 45 percent Kawasaki Steel
05/85	Suwa Seikosha	Applied Micro Circuits	AMCC offering CMOS chips under license from Suwa Seikosha
01/85	Casio, Hitachi, NEC, Oki	----	Casio to design custom LSIs that will be produced by Hitachi, NEC, and Oki

Source: Dataquest
April 1987

1985 Japanese Alliances

Table 9

MAJOR ASIC CAMPS

LSI Logic Camp	Gould/AMI Camp
AMD	Gould/AMI
GE/Intersil	Mostek
LSI Logic	Asahi Chemical
SGS-Ates	Western Micro Technology
RCA	Intergraph Design System
Toshiba	
Mitsubishi	
Sharp	
Chips & Technologies	
California Devices	
Olympus	
Kawasaki Steel	

TI/Fujitsu Camp	Motorola/National Camp
Fujitsu	International Microelectronic Products
MMI	Motorola
Signetics	National Semiconductor
Texas Instruments	GTE Microcircuits
Harris	Plessey
International Computer Ltd.	

Fairchild/VTI Camp	Seiko/Honeywell Camp
Fairchild	SMOS Systems (Seiko)
VLSI Technology	Applied Micro Circuits Corp. (AMCC)
Ricoh	Xilinx
Lattice	Honeywell
Rockwell Custom MOS Arrays	International Microcircuits (IMI)
Western Digital	Siliconix
Altera	Nippon Precision Circuits
Philips	
Silicon Compilers	
Sierra	
Western Design Center	

Other Camps

Intel/Zymos
Oki/Thomson CSF
NEC
Hitachi

Source: Dataquest
April 1987

Other Semiconductor Devices: A Potpourri of Alliances

As shown in Table 10, there were 15 alliances covering a wide variety of other semiconductor devices. Probably the major announcements were Mitsubishi's joint venture with GE and Westinghouse to produce discrete devices, Hitachi's tie-up with Sperry, and Toshiba's joint development of IC cards with VISA International. Toshiba also teamed up with Brooktree, Pohang Jonghup Steel, SGS-Ates, and Sun Microsystems. What distinguishes these alliances are the large number of joint manufacturing and development ventures (9 of the 15 agreements).

Table 10

OTHER JAPANESE SEMICONDUCTOR DEVICE STRATEGIC ALLIANCES IN 1985

Date	Japanese	Foreign	Agreement
12/85	Toshiba	Pohang Jonghup Steel	First major technology transfer with South Korean company (undisclosed)
11/85	Hitachi	Sperry	Technology exchange; joint development effort to study feasibility of using Hitachi's high-speed ICs in Sperry's 1100 system architecture; Hitachi already manufactures Sperry's personal computers
11/85	Kodenshi Corp.	ABM Semicon-ductor	ABM (San Jose, California start-up) to sell 200 Kodenshi optoelectronic ICs in exchange for partial Kodenshi funding
11/85	Toshiba	SGS-Ates	Toshiba 2nd-sourcing of 3 SGS telecom ICs, including CMOS single-chip PCM combo, NMOS modem, and NMOS PCM switching matrix (1st phase); joint development of new telecom ICs (2nd phase); also expansion of 1982 CMOS process contract
11/85	Toshiba	VISA Int'l	Joint development of multipurpose IC card (Super Smart Card) for sale in 1987

(Continued)

1985 Japanese Alliances

Table 10 (Continued)

OTHER JAPANESE SEMICONDUCTOR DEVICE STRATEGIC ALLIANCES IN 1985

Date	Japanese	Foreign	Agreement
10/85	Toshiba	Sun Microsystems	Sun to supply $35 million in CAD workstations to Toshiba; Sun's Network File System software to be added to Toshiba's computers to allow communications with Sun workstations; also technology exchange (undisclosed)
09/85	Toshiba	Brooktree	Licensing of Brooktree's digital/analog converters; Toshiba to use Brooktree chip architecture to design high-resolution D/A converters for consumer digital audio uses
09/85	Toko	Motorola (MC13020P)	Toko to 2nd-source Motorola ICs for AM stereo receiver signal decoders
09/85	Mitsubishi	Westinghouse, GE	Joint venture to produce diodes, power transistors, and thyristors in the U.S.; 45 percent Westinghouse, 45 percent GE, 10 percent Mitsubishi America; $21 million book value; production at 3 plants (Youngwood, PA; Burabo, Puerto Rico; Le Mans, France)
05/85	Kobe Steel	Trefimetaux (France)	Transfer of Kobe's IC lead frame production technology
05/85	Nippon Precision Circuits (Seiko)	Micro Power	Seiko to produce and sell molybdenum ICs and peripheral ICs for Micro Power's modems
05/85	Kanebo, Mitsubishi	----	Joint venture (Kanebo Electronics) to run IC test and assembly plant in Hyogo area; Mitsubishi to supply TTL chips to plant; production from December 1985; Y15 billion ($75 million), 5-year investment

(Continued)

Table 10 (Continued)

OTHER JAPANESE SEMICONDUCTOR DEVICE
STRATEGIC ALLIANCES IN 1985

Date	Japanese	Foreign	Agreement
04/85	Fuji Electric	Thomson	Thomson to second-source Fuji's power modules; Fuji to receive royalties
03/85	Matsushita Hayashi-bara	----	Announced water-soluble photopolymer resist for IC processing by applying bioelectronics technology
01/85	Ricoh	Ixys	Ricoh to license and jointly develop Ixys' MOSFETs and thyristor MOSFETs incorporated in power conversion and motion control applications for home, factory, and office automation products

Source: Dataquest
April 1987

Equipment and Materials: Marriages Still Blooming

Perhaps the least-noticed trend in semiconductors is the proliferation of U.S.-Japanese alliances among equipment and materials manufacturers. Since 1980, we have recorded 68 alliances; almost all are joint ventures. Why the popularity of these alliances? We believe that the entry of strong Japanese competitors and the service-intensive nature of the business demands a Japanese partner for research, low-cost manufacturing, and after-sales servicing. In 1985, we recorded 17 new alliances and one separation, as shown in Table 11. Most of the ventures are developing equipment for 6-inch wafer lines, including etchers, diffusion furnaces, chemical vapor deposition (CVD) equipment, and spin coaters. One interesting agreement is Hyundai's plan to produce 6-inch wafers for Ricoh as a result of the downturn.

1985 Japanese Alliances

Table 11

1985 SEMICONDUCTOR EQUIPMENT AND MATERIALS STRATEGIC ALLIANCES

Date	Japanese	Foreign	Agreement
10/85	Samco International	March Instruments	Samco to produce plasma CVD, MOCVD, and dry stripper equipment in United States at March's Concord, California, plant
10/85	Shinetsu Handotai, Mitsui & Co.	SM Yttrium Canada, Union Oil, Denison Mines	$9 million investment in plant to produce yttrium for use in microwave communications equipment; Denison to run plant; 100-150 metric ton annual plant capacity
10/85	Nippon Kokan	GE	Joint purchase of Great Western silicon factory for $16 million; new GWS Corp.
09/85	Matsushita Denko Co.	----	Developed vertical CVD equipment for thin-film ULSIs
08/85	Tokuda Works	Tylan Corp.	Production of etchers in United States from 1986
07/85	Ricoh	Hyundai	Hyundai to produce 6-inch wafers for Ricoh
06/85	Hugle Electronics	Zeus Corp.	50/50 joint venture to produce Hugle's CVD equipment, cassette cleaners, and probe cards
06/85	Nippon Kokan	GE	Licensing of GE's polycrystal manufacturing technology for Nippon Kokan's Toyama Works
04/85	Kanematsu Semiconductor	Veeco	Kanematsu technical center near Tokyo to develop Veeco ion implanters
04/85	Canon Sales Co.	CIT-Alcatel	Joint venture (Alcantech) capitalized at ¥100 million ($500,000); 50/50 share ownership; assembly and sales of etchers in Japan from 1986

(Continued)

1985 Japanese Alliances

Table 11 (Continued)

1985 SEMICONDUCTOR EQUIPMENT AND MATERIALS STRATEGIC ALLIANCES

Date	Japanese	Foreign	Agreement
03/85	Mitsubishi, Tokyo	----	Codevelopment of electron cyclotron resonance (ECR) plasma etching equipment for 4Mb DRAMs; existing joint venture
03/85	Itoman Kiki Hanbai, Toyomitsu	Plasma Thermo	Joint venture, Plasma Hitech, to sell Plasma's equipment in Japan to top 30 component makers
02/85	Hugle	Atcor	Japanese joint venture to produce 70 to 80 wafer cassette cleaners annually at new plant
02/85	Koyo Lindberg	General Signal	Joint venture to develop automated vertical diffusion furnaces for 6-inch wafers, based on General Signal's manual model; production from fall 1985 at Koyo's Nara plant; Koyo Lindberg owned equally by General Signal and Koyo Seiko
02/85	Toray Industries	Dexter	50/50 joint venture (Toray Hysol Co.) to produce epoxy-resin package materials for ICs and opto-electronics at Toray's Nagoya Works in 1986; capitalized at ¥1.8 billion ($9 million); plant capacity of 6,000 tons annually
02/85	Kanematsu Semicon-ductor	Semiconduc-tor Systems	Semiconductor Systems (San Jose, California) to license its spin coater production technology for 6-inch wafer photoresist coating

(Continued)

Table 11 (Continued)

1985 SEMICONDUCTOR EQUIPMENT AND MATERIALS STRATEGIC ALLIANCES

Date	Japanese	Foreign	Agreement
02/85	Kanematsu Gosho	Perkin-Elmer	Cancellation of agency agreement in Japan to allow opening of Perkin-Elmer Semiconductor Japan to handle sales in Japan; initial staff of 70 to be expanded to 125 by late 1985
01/85	Sumitomo Heavy	Eaton	Expansion of 1983 ion implant agreement to include Optimetrix steppers

Source: Dataquest
April 1987

DATAQUEST CONCLUSIONS

In an era of worldwide overcapacity and growing protectionism, Dataquest believes that the winners in the semiconductor industry will be those companies that judiciously develop strategic alliances to leverage their technologies and conserve their cash. Like all marriages, these alliances will encounter rocky periods once the honeymoon is over, and we expect many alliances to fall apart. But companies that are able to look beyond short-term difficulties and work hard at developing strong relationships have an opportunity to expand their market shares. Those who choose to go it alone run the risk of forfeiting markets and technologies by default. Some companies may choose not to pursue an aggressive strategy, but we believe that they cannot afford to ignore the many options available to them. In the long run, marketing strategy by omission is just as important as strategy by commission.

1984 Japanese Alliances

SUMMARY

"If you can't beat 'em, join 'em." For years, this phrase captured the feeling toward joint ventures and licensing agreements between Japanese and American semiconductor makers. Companies entered agreements largely for defensive reasons in order to secure technology and avoid losing market share.

While these motivations still exist, Dataquest observes a gradual shift in the motivations driving the new ventures and agreements being inked. Recently, mutual licensing agreements have increased because of the rising level of Japanese technology and American concern over the "boomerang effect"--licensing their technology for upfront fees, but losing market share later. Moreover, many companies are entering longer-term agreements to fill in their product lines and to jointly develop new products. The emphasis is on partnership, not rivalry. As of early December, Dataquest recorded 11 joint ventures and 19 licensing agreements between Japanese and non-Japanese semiconductor makers, as well as 16 joint ventures among semiconductor equipment manufacturers who will be covered in a forthcoming newsletter. As shown in Table 1, this is a record for the industry.

Table 1

JAPANESE SEMICONDUCTOR JOINT VENTURES AND LICENSING AGREEMENTS
(1980-1984)

	1980	1981	1982	1983	1984
Semiconductor Makers					
Joint Ventures	1	1	5	3	11
Licensing Agreements	2	5	5	11	19
Equipment Manufacturers	0	5	12	8	16
	3	11	22	22	46

Source: Dataquest
April 1987

1984 Japanese Alliances

JOINT VENTURES--MARRIAGE-MAKING JAPANESE STYLE

Joint ventures are becoming increasingly popular among Japanese and American semiconductor makers seeking long-term development and marketing arrangements as shown in Table 2. In 1984, NEC was the most active in this area, signing agreements with four American companies and one Japanese company for its V Series MPU and LAN controllers, as follows:

- Yokogawa Hewlett-Packard (YHP) will be provided with technical data on the V20 and V30 series, in exchange for the language processing program and emulator for the debugging program.

- Sophia Systems, a Japanese company, will develop a support system for NEC's V Series.

- Tektronix, which already supports nine NEC products, will develop a support system and market the V Series within a year.

- Digital Research will develop modular-type CP/M operating systems for the V20 and V30 series and market them by mid-1985.

- Zilog has signed a five-year contract to second source the V Series, making Zilog the first U.S. second-source supplier of an original Japanese MPU.

- As discussed in our newsletter, "NEC Starts Original MPU Campaign," dated August 8, 1984, we expect NEC to secure a significant share of the Japanese MPU market with its V Series. These joint ventures provide NEC with the development support needed for this marketing effort.

Ricoh, a newcomer to the semiconductor field, is entering joint ventures and licensing agreements to strengthen its product portfolio. In March, Ricoh entered into a partnership with Custom MOS Arrays in which Ricoh will provide CMOS wafer processing technology in exchange for Custom MOS Arrays' gate array design technology. In September, Ricoh joined with Panatec R&D Corporation for joint IC development and sales. In addition, it signed a five-year contract with Panatec R&D Corporation and Modular Semiconductor Corporation to produce and ship Ricoh's sample CMOS 256K DRAMs and 16K SRAMs by late 1984. In May, Ricoh considered a joint venture with Vitelic, a recent Silicon Valley start-up, but cancelled its plans when both parties failed to arrive at an agreement.

1984 Japanese Alliances

Table 2

JAPANESE JOINT VENTURES IN 1984

Date	Japanese Company	Non-Japanese Company	Agreement
March 26	Ricoh	Custom MOS Arrays	CMOS gate array design and wafer production
April 19	NEC	Yokogawa Hewlett-Packard	Joint development of V Series MPU support system
May 1	NEC	Sophia Systems	Joint development of V Series MPU support systems
May 14	NEC	Tektronix	Tektronix marketing of V Series support MPU systems
May 16	Zax Corporation (start-up)	Microtec Research Corporation	Joint development of System Z MPU support systems
May 31	Rhythm Watch	TI Japan	IC assembly and test of TI Japan's ICs
June 3	Toko	Motorola	Read/write amplifiers for flexible disk drives
Sept. 10	Ricoh	Panatec R&D Corporation (U.S.)	Joint development and marketing of ICs
Nov. 2	NEC	Digital Research	Joint marketing of CP/M operating system for V Series
Nov. 15	NEC	Corvus Systems	Joint development of LSI for CMOS single-chip controller
Dec. 7	Sharp	RCA	Design center and wafer fab on West Coast of U.S.--RCA owns 51 percent

Source: Dataquest April 1987

1984 Japanese Alliances

LICENSING AGREEMENTS--FROM MICROPROCESSORS TO GATE ARRAYS

Licensing agreements are the favorite way for Japanese companies to acquire technology, with 19 agreements signed as of early December, as shown in Table 3. Japanese companies are still behind the United States in MPU and MCU technology, so second-sourcing agreements with Intel, Motorola, and Zilog predominated in 1984.

Table 3

JAPANESE LICENSING AGREEMENTS IN 1984

Date	Japanese Company	Non-Japanese Company	Agreement
Jan. 9	Fujitsu	Texas Instruments	Mutual second-sourcing of CMOS and bipolar gate arrays
Feb. 13	Toshiba*	Zilog	Toshiba supplying CMOS 8-bit MPU on OEM basis
Feb. 14	Toshiba	Motorola*	Second sourcing of Motorola 16-bit MPU
Feb. 16	Fujitsu	Intel*	Fujitsu takes partial charge of 16/32-bit MPU development
March 5	Tokyo Sanyo	Intel*	Sanyo captive use of 8086/8088/ 8051
March 9	NEC	Zilog*	Settlement of Z80 patent infringement
March 11	Oki Electric	Intel*	Oki captive use of Intel MPUs, MCUs, and MPR LSIs
April 17	NEC	Zilog	Mutual sourcing of NEC V Series and Zilog Z8000 32-bit MPU
May 7	Hitachi*	AMI	Second sourcing of codecs

(Continued)

1984 Japanese Alliances

Table 3 (Continued)

JAPANESE LICENSING AGREEMENTS IN 1984

Date	Japanese Company	Non-Japanese Company	Agreement
June 12	Oki	Standard Microsystems	Cross-licensing of all patents and patent applications
June 22	NMB Semiconductor (Minebea)	Inmos USA	CMOS 256K DRAM
June 30	Fujitsu*	Monolithic Memories	Second sourcing of Fujitsu TTL gate arrays
July 10	Ricoh*	Rockwell	Ricoh supplying CMOS 64K EPROMs to Rockwell
July 18	Fujitsu	Intel*	Second sourcing of EPROMs, 8-bit, single-chip MCUs, and MPUs
Aug. 29	Sharp*	Samsung	Transfer of 4-bit, single-chip MCU technology to Samsung
Sept. 12	Ricoh	Panatec R&D Corp. and Modular Semiconductor*	Joint development, technical exchange, and mutual sales agreement for 256K DRAMs
Oct. 2	Oki Electric	Thomson CSF	Mutual second sourcing of CMOS gate arrays
Nov. 2	Fujitsu	Intel*	Second sourcing of Intel's 16-bit MPUs and peripherals
Dec. 1	Sony*	Monsanto	Magnetic field Czochralski method

*Company granting license

Source: Dataquest
April 1987

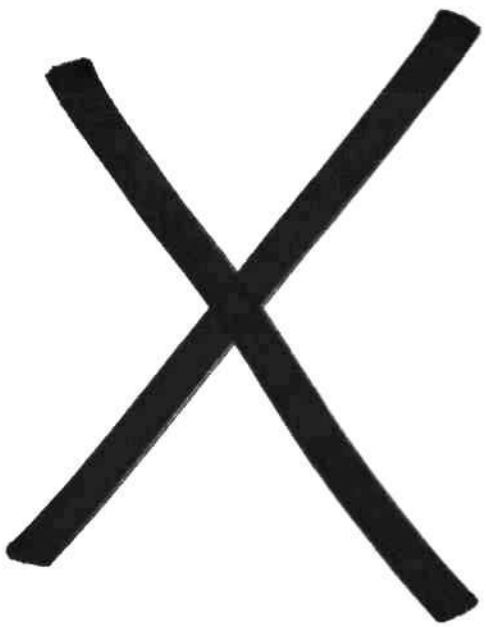
1984 Japanese Alliances

Toshiba, which signed a 10-year cross-licensing agreement in 1982 for Zilog's Z80/Z800/Z8000 families, will supply the CMOS 8-bit Z80C, making Toshiba the first Japanese company to provide MPUs to an American maker on an OEM basis. Toshiba also negotiated a second-source agreement for Motorola's 16-bit MPUs. Motorola previously signed an agreement in 1981 for Hitachi's H-CMOS process.

Fujitsu has signed second-sourcing agreements for its TTL and CMOS gate arrays. In January, Fujitsu agreed to provide its CMOS gate arrays in exchange for Texas Instruments' bipolar gate arrays. (For details, see our newsletter dated January 12, 1984, "Fujitsu and TI Sign Gate Array Second-Source Agreement.") In June, Monolithic Memories agreed to second source Fujitsu's TTL gate arrays (ranging from 240 to 2,000 gates), with shipments to Japan, Europe, and the United States beginning in mid-1985. In February, Fujitsu announced that it will take partial charge in developing Intel's 80286 (16-bit) and 80386 (32-bit) MPUs. In July, Fujitsu announced that it would second source Intel's EPROMs, 8-bit MPUs, and one-chip MCUs. In November, both companies announced that Fujitsu will second source Intel's 16-bit MPUs (80286, 80186); 8-bit bus version of the 80186 (80188); 8-bit, single-chip MCU (8051); clock generator (82284); and bus controller (82288). Intel has also negotiated agreements with NEC, Mitsubishi, Oki Electric, and Tokyo Sanyo.

Oki Electric signed three agreements in 1984. In March, it agreed to produce Intel's MPUs and MCUs only for captive use. In June, Oki signed a worldwide, exclusive cross-licensing agreement with Standard Microsystems Corporation for each company's patents and patent applications. In October, Thomson CSF and Oki Electric entered a mutual licensing agreement in which Thomson CSF will become a second-source supplier of Oki's CMOS gates (3-micron 4,000 gates and 2-micron 10,000 gates) and Oki Electric will supply Thomson's original CMOS gate arrays. The companies will also exchange IC mass production technology. Recently, Thomson CSF opened a design center in Tokyo.

Ricoh has moved aggressively into the semiconductor field. In addition to the joint ventures discussed earlier in this newsletter, Ricoh announced that it would supply CMOS 64K EPROMs to Rockwell International, beginning with 10,000 units a month and gradually increasing. Ricoh currently produces about 500,000 units per month. In September, Ricoh signed a five-year agreement with Panatec R&D Corporation and Modular Semiconductor to produce CMOS 256K DRAMs and 16K SRAMs using Modular's design and processing technology. Ricoh will sample these products in Japan and supply them to its partners by the end of 1984.



Startups/Newcomers

The following is a list of the material in this section:

- Semiconductor Start-Up History 1977-1985
- Semiconductor Start-Up Update First Quarter 1987
- Semiconductor Start-Up Update Second Quarter 1987

NOTE: The arrow symbol indicates the latest documents's location behind this subject tab.

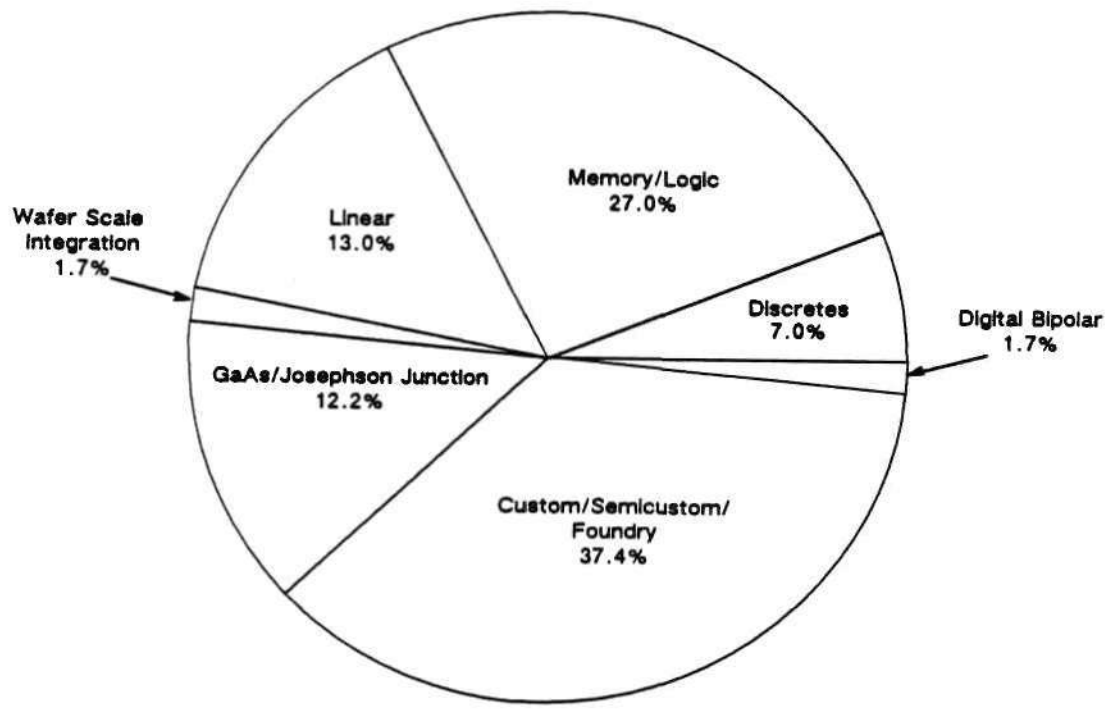
Semiconductor Start-Up History 1977-1985

SUMMARY

The semiconductor industry is a vibrant industry that continues to have dynamic growth. Between 1977 and 1985, DATAQUEST recorded approximately 125 semiconductor manufacturing start-ups. There were 36 start-ups in 1983, 31 start-ups in 1984, and 12 start-ups in 1985. The infusion of venture capital, the increased use of customization, and the growing use of semiconductors in all aspects of daily life have been the driving forces behind the emergence of new companies. As shown in Figure 1, the companies offer a variety of products. We believe the peak of this third wave has passed, but expect a smaller after-wave within the next few years.

Figure 1

SEMICONDUCTOR START-UP PRODUCT LINES
(1977 to 1984)



Source: DATAQUEST
March 1986

Semiconductor Start-Up History 1977-1985

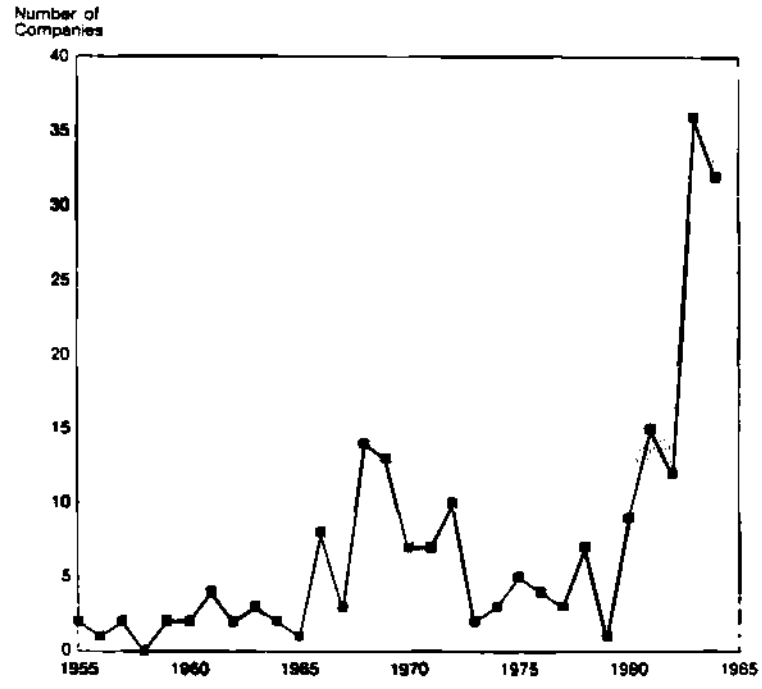
HISTORICAL TRENDS

The heightened start-up activity level in the last few years marked a new phase in the semiconductor industry. As shown in Figure 2, the industry has gone through five distinct periods:

- Establishment of the industry under Bell Labs and Shockley Transistor (1947-1957)
- Domination by Fairchild, which spun off National Semiconductor, Raytheon, Signetics, and other start-ups (1957-1967)
- Boom in start-up companies offering standard products, such as AMD, Intel, and MMI (1968-1974)
- Consolidation of the industry through mergers and acquisitions (1975-1979)
- Shift toward customization and new technologies, such as gate arrays, wafer-scale integration, and gallium arsenide (1980-1984)

Figure 2

HISTORY OF SEMICONDUCTOR START-UPS



Source: DATAQUEST
March 1986

Semiconductor Start-Up History 1977-1985

DATAQUEST believes that the shift toward customization is driven by the strong demand for unique, cost-effective products and the lack of standardized VLSI circuits. In application-specific integrated circuits (ASICs), a category that includes custom circuits, customer-owned tooling, wafer foundries, standard cell circuits, gate arrays, and field-programmable devices, we expect market share to increase significantly. Of the 114 companies that started between 1977 and 1984, 42 were in the ASIC area. This indicates that the move toward ASICs is gaining momentum.

THE DRIVE FOR ORIGINALITY

The availability of venture capital does not totally explain the upswing in start-up activity, since many new companies are internally financed. DATAQUEST believes that technological innovation continues to be the driving force. Several factors contribute to this trend:

- The proliferation of specialized market niches
- Developments in new technologies, such as EEPROMs, wafer-scale integration, gallium arsenide, and specialized chips
- New process technologies and advanced computer-aided design (CAD)
- The availability of silicon foundries
- The entry into the marketplace of Korean and Taiwanese companies with sizable financing

Most of the memory start-ups offer advanced CMOS processes and fine-line geometries in the 1.5- to 3.0-micron range. Larger wafers are also popular. Modern Electrosystems and Tristar Semiconductor use 5-inch wafers, while Exel Microelectronics and Lattice Semiconductor are experimenting with 6-inch wafers. Advances in wafer etching and stepper equipment make these approaches technically feasible.

SILICON VALLEY--THE START-UP CAPITAL

Despite the emergence of high-technology centers throughout the United States and the world, Silicon Valley still leads in the number of semiconductor start-ups. As shown in Table 1, 67 of 114 start-ups since 1977, or 58 percent, were located in Silicon Valley. Table 2 is a complete list of start-ups established between 1977 and 1984.

Semiconductor Start-Up History 1977-1985

Table 1

LOCATION OF SEMICONDUCTOR START-UPS

	1977	1978	1979	1980	1981	1982	1983	1984	1985	Total
Silicon Valley		5	1	5	12	8	21	14	7	73
Southern California				1	2	2	1	1		7
Northwest		1		1	1		3	2		8
Midwest							5	2		7
East Coast	1			1		1	4	2	2	11
Europe						1		4	3	8
Asia	2			1			1	4		8
Canada	—	—	—	—	—	—	1	2	—	3
Total	3	6	1	9	15	12	36	31	12	125

Source: DATAQUEST
March 1986

Table 2

SEMICONDUCTOR START-UPS
(1977 to 1984)

Year	Company	Location	Products
1977	Micro-circuit Eng.	West Palm Beach, FL	ASICs
	A&D Company	Tokyo, Japan	A/D, D/A Converters
	Alpha Electronics	Tokyo, Japan	Precision Resistors
1978	Acrian	Cupertino, CA	RF Power Discretes
	California Devices	San Jose, CA	ASICs
	Micron Technology	Boise, ID	DRAMs
	Universal Semi.	San Jose, CA	ASICs, Foundry
	Xicor	Milpitas, CA	Nonvolatile Memory
	Zymos	Sunnyvale, CA	ASICs
1979	Comdial	Sunnyvale, CA	Foundry
1980	Applied Micro Circuits	Cupertino, CA	ASICs
	Harris Microwave	Milpitas, CA	GaAs, FETs, Logic
	Inmos	Colorado Springs, CO	NMOS Memory
	Insouth Microsystems	Auburn, AL	CMOS ASICs
	Kyoto Semiconductor	Kyoto, Japan	Optoelectronics
	LSI Logic	Milpitas, CA	ASICs
	Silicon Systems	Tustin, CA	ASICs
	Trilogy	Cupertino, CA	CMOS
	VLSI Technology	San Jose, CA	ASICs

(Continued)

Semiconductor Start-Up History 1977-1985

Table 2 (Continued)

SEMICONDUCTOR START-UPS
(1977 to 1984)

Year	Company	Location	Products
1981	Brooktree Corp.	San Diego, CA	D/A Converters
	Cirrus Logic	Milpitas, CA	ASICs
	Gigabit Logic	Newbury Park, CA	GaAs SRAMs
	Integrated Device Tech.	Santa Clara, CA	CMOS SRAMs
	Int'l. Microcircuits	Santa Clara, CA	ASICs
	Int'l. Microelectronic Prod.	San Jose, CA	ASICs
	Linear Technology	Milpitas, CA	Linear
	Panatech Semiconductor	Santa Clara, CA	ASICs, EPLAs
	Seeq Technology	San Jose, CA	Nonvolatile RAMs
	Si-Fab	Scotts Valley, CA	ASICs, Foundry
	Signal Processor Circuits	Salt Lake City, UT	Linear
	Silicon Compilers	San Jose, CA	ASICs
	Telmos	Sunnyvale, CA	CMOS ASICs
	Weitek	Santa Clara, CA	Graphic ICs
	Zytrex	Sunnyvale, CA	CMOS Memory/Logic
1982	Array Devices	San Diego, CA	ASICs
	Array Technology	San Jose, CA	CMOS ASICs
	Barvon Research	Milpitas, CA	ASICs
	Custom MOS Arrays	Milpitas, CA	CMOS ASICs
	Cypress Semiconductor	San Jose, CA	CMOS PALs
	IC Sensors	Sunnyvale, CA	Pressure Sensing ICs
	Isocom	Campbell, CA	GaAs Couplers
	Lattice Logic	Edinburgh, Scotland	ASICs
	Microwave Monolithic	Simi Valley,CA	GaAs MMICs
	Mosaic Systems	Troy, MI	Wafer Scale
	Sensym	Sunnyvale, CA	IC Sensors
	United Microelectronics	Santa Clara, CA	MOS Memory/Micro
1983	Altera Semiconductor	Santa Clara, CA	Erasable PLDs
	Bipolar Integrated Tech.	Beaverton, OR	Bipolar ICs
	Calmos Systems	Kanata, Ontario	CMOS ASICs, MEM, MIC, Logic
	Calogic Corp.	Fremont, CA	DMOS FET Arrays
	Custom Silicon	Lowell, MA	ASICs
	Elantec	Milpitas, CA	High-perf. Linear
	Electronic Technology	Cedar Rapids, IA	CMOS ASICs
	Exel Microelectronics	San Jose, CA	EEPROMs
	Hypress	Elmsford, NY	Josephson Junction
	Inova Microelectronics	Campbell, CA	SRAM Modules, WSI
	Int'l. CMOS Technology	Cupertino, CA	Nonvolatile Memory
	Int'l. Logic Systems	Colorado Springs, CO Santa Clara, CA	CMOS/Bipolar Logic
	Iridian Microwave	Chatsworth, CA	GaAs FETs
	IXYS Corporation	Santa Clara, CA	Power Discretes
	Laser Path	San Jose, CA	CMOS Logic
	Logic Devices	Sunnyvale, CA	CMOS DSP
	Maxim Integrated Prod.	Sunnyvale, CA	CMOS Linear
	Metalogic Corp.	Cambridge, MA	ASICs
	Micro Linear Corp.	San Jose, CA	D/A, A/D, IC Filter

(Continued)

Semiconductor Start-Up History 1977-1985

Table 2 (Continued)

SEMICONDUCTOR START-UPS
(1977 to 1984)

Year	Company	Location	Products
1983 (Cont.)	Microwave Technology	Fremont, CA	GaAs FETs, Amplifier
	Mosel	Sunnyvale, CA	MOS Memory
	Modern Electrosystem	Sunnyvale, CA	NMOS/CMOS Mem./Logic
	Novix	Cupertino, CA	Micros
	Opto Tech.	Msinchu, Taiwan	Discretes
	SMOS Systems	San Jose, CA	CMOS Memory/Logic
	Seattle Silicon	Bellevue, WA	ASICs
	Sierra Semiconductor	San Jose, CA	CMOS ASICs
	Silicon Design Labs	Liberty Corner, NJ	ASICs
	Texet Corp.	Richardson, TX	Power ICs, MOS FETs
	Tristar Semiconductor	Santa Clara, CA	NMOS/CMOS Mem./Logic
	Vatic Systems	Mesa, AZ	ASICs
	Visic	San Jose, CA	HCMOS Memory
	Vitelic	San Jose, CA	HCMOS Memory
	Wafer Scale Integration	Fremont, CA	ASICs
	Xtar Electronics	Elk Grove, IL	Graphics ICs
	Zoran	Sunnyvale, CA	DSP
1984	Anadigics	Morristown, NJ	GaAs A/D Converters
	Array Logic	Cambridge, England	CMOS/Bipolar ASICs
	Atmel Corp.	Milpitas, CA	EEPROMs
	China Ling Lang Micro.	China (Mainland)	ASICs
	Chips & Technologies	Milpitas, CA	ASICs
	Crystal Semiconductor	Austin, TX	Telecom ICs
	Dallas Semiconductor	Dallas, TX	CMOS Memory
	Exmos Semiconductor	Galgary, Alberta	Telecom ICs
	Ikos Systems	Sunnyvale, CA	ASICs
	Inova Microelectronics	Campbell, CA	ASICs
	Integrated Logic Systems	Colorado Springs, CO	ASICs, PLAs
	Integrated Power Semi.	Livingston, Scotland Santa Clara, CA	Linear
	Les Technologies OMVPE	St, Laurent, Quebec	GaAs Buffers
	Micro MOS	Santa Clara, CA	CMOS Memory
	Micron Semiconductor	Lansing, England	Silicon Detectors
	Modular Semiconductor	Santa Clara, CA	CMOS Mem/Micro
	NMB Semiconductor	Tokyo, Japan	CMOS Memory
	Pacific Monolithics	Sunnyvale, CA	GaAs MMICs
	Performance Semiconductor	Cupertino, CA	CMOS Mem./MIC/Logic
	Pivot III-V Corp.	New York, NY	GaAs
	Quasel	Santa Clara, CA	CMOS ASMs
	Silicon Macrosystems	San Jose, CA	CMOS Memory
	STC Components, Ltd.	Paignton, England	GaAs, ASICs, Foundry
	Taisel	Taipai, Taiwan	Hybrids
	Teledyne Mono. Microwave	Mountain View, CA	GaAs Linear
	Topaz Semiconductor	San Jose, CA	DMOS ICs
	Triquint Semiconductor	Beaverton, OR	GaAs ICs
	Vitesse Electronics	Camarillo, CA	GaAS ICs
	VTC Inc.	Minneapolis, MN	High-perf. Bipolar
	Yageo	Taipai, Taiwan	Resistors
	Xilinx	San Jose, CA	CMOS ASICs

Source: DATAQUEST
March 1986

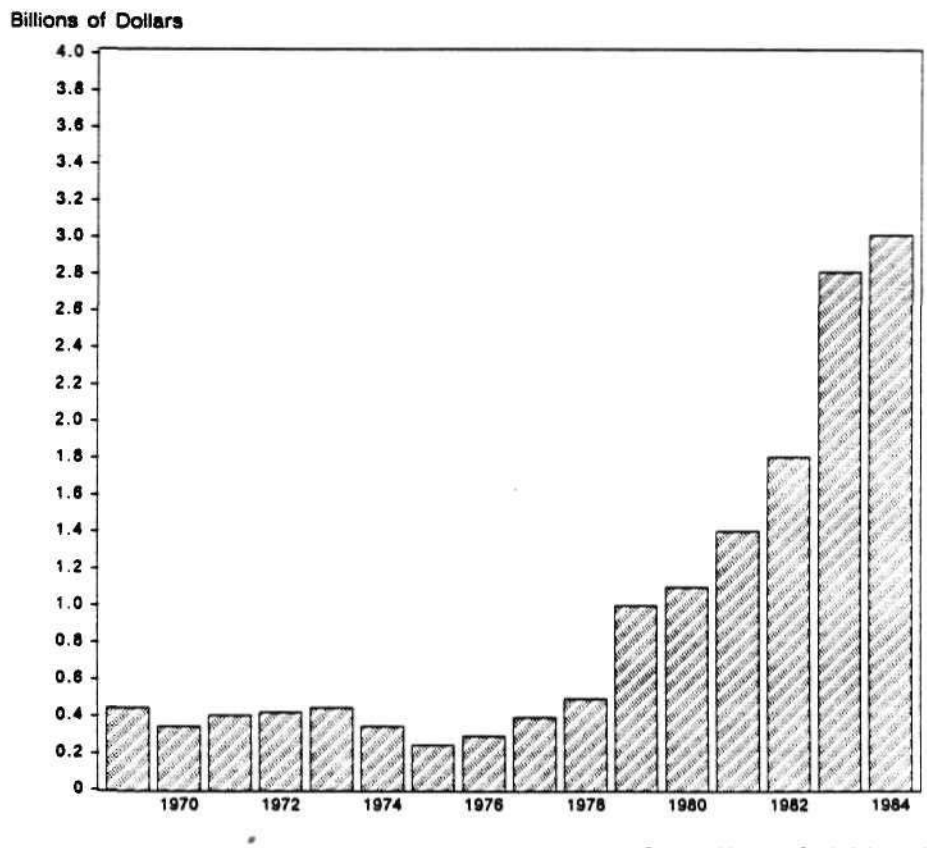
Semiconductor Start-Up History 1977-1985

THE BOOM IN VENTURE CAPITAL

One of the other major reasons for the upswing in start-up activity was the rapid growth of venture capital financing. As shown in Figure 3, the total flow of venture capital funds increased from $450 million in 1969, to more than $3 billion in 1984. Until 1977, most of these funds were invested in existing businesses. Venture capital for start-up companies did not appear in large amounts until the 1978 revision of the capital gains tax law, which lowered the corporate tax rate from 30 percent to 20 percent and the individual tax rate from 50 percent to 20 percent. Since 1978, we have observed an explosion of public offerings, private placements, R&D partnerships, and limited partnerships. The availability of venture capital has tightened, however, with the change in the semiconductor industry climate. New companies are under more pressure to be unique or superior in their product/technology strategies.

Figure 3

FLOW OF VENTURE CAPITAL



Source: Venture Capital Journal

Semiconductor Start-Up History 1977-1985

DEFINITION OF START-UPS

DATAQUEST defines start-ups as semiconductor manufacturers that design and ship finished products under their own labels, whether or not they have in-house wafer fabrication facilities. In the past, we defined start-ups as semiconductor manufacturers with fabrication facilities. With the trend toward customization and the rapidly rising cost of processing equipment, however, we have observed that many recent start-ups use foundries to reduce their up-front costs. They design their custom and semicustom circuits, send the masks to silicon foundries for fabrication, then package the chips in-house. They cannot be considered custom design houses since they offer regular product lines. DATAQUEST believes that as customization increases, we will see more start-ups using a variety of fabrication arrangements.

1985 Start-Ups

In 1985, DATAQUEST recorded 12 new start-up companies, as shown in Table 3. This is a preliminary list, however, since many start-ups formed in 1985 will not publicly announce themselves until 1986 or 1987, when they introduce their first products.

Table 3

1985 SEMICONDUCTOR START-UPS

Company	Location	Products
ABM Semiconductor	San Jose, CA	AlGaAs opto devices
Acumos (old Semi Processes)	San Jose, CA	CMOS gate arrays
Advanced CMOS Devices	Cupertino, CA	CMOS memories
Catalyst	Santa Clara, CA	Nonvolatile memories
Celeritek	San Jose, CA	GaAs FET amps
Clarity Systems (Israel)	Sunnyvale, CA	ASICs
European Silicon Structures	Munich, West Germany	ASICs
Gain Electronics	Princeton, NJ	GaAs ICs
Quodos Ltd.	Cambridge, England	ASICs
Tachonics (Grumman)	Bethpage, NY	GaAs ICs
Unicorn Microelectronics	San Jose, CA	ASICs
Wolfson Microelectronics	Edinburgh, Scotland	ASICs, DSP

Source: DATAQUEST
March 1986

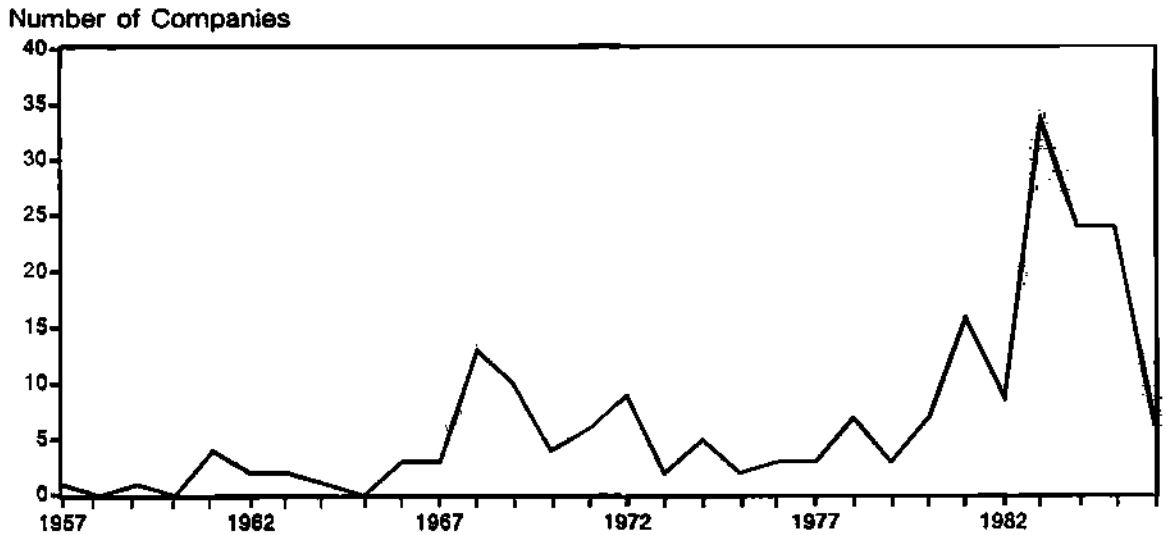
Semiconductor Start-Up Update First Quarter 1987

This is the first in a series of quarterly updates on recent activities of start-up semiconductor companies. This information supplements I.C. Start-Ups 1987, a new Dataquest directory of semiconductor start-ups, which was published in October 1986. The newsletters will include information on new companies formed, initial and additional rounds of financing, significant company announcements, and new alliances.

Figure 1 illustrates the activity in company formation between 1957 and 1986.

Figure 1

FORMATION OF COMPANIES
1957-1986



Source: Dataquest
August 1987

MAJOR DEVELOPMENTS

Start-up activity continues at a strong pace. Seven companies, formed in 1986, have emerged. Dataquest expects the number to grow as companies raise initial financing and complete their initial product offerings.

We have noted also that many of the start-ups are experiencing extraordinary growth. In 1986, Cypress Semiconductor approximately tripled its sales from $18 million in 1985; Samsung and UMC doubled their sales from $95 million and $33 million, respectively, in 1985. Many other companies increased revenue by 25, 30, or 50 percent.

Semiconductor Start-Up Update First Quarter 1987

Major developments for start-up companies include the following:

- Start-up companies have attracted $73.6 million in additional financing since the publishing of I.C. Start-Ups 1987 in October 1986.
- VLSI Technology acquired Visic, Inc.; Custom MOS Arrays and its sister company, California Micro Devices, merged activities.
- Start-ups have expanded with the formation of subsidiaries in Asia and additional manufacturing facilities in the United States and Europe.
- Several start-ups have also announced reorganizations and changes of presidents and CEOs, indicating business expansion.
- Many new alliances have been formed, involving a total of 33 companies.

Table 1 lists the semiconductor companies formed in 1985 and 1986.

Table 1

START-UP COMPANIES

Companies Formed in 1986

Company	Location	Product
Gazelle Microcircuits	Sunnyvale, CA	GaAs digital
Graphics Communications	Japan	Graphics chips
Innovative Silicon Technology	Italy	ASICs
MemTech	Folsom, CA	Bubble memory
Solid State Technologies	San Jose, CA	Bipolar memory
Taiwan Semiconductor Mfg. Corp.	Taiwan	Foundry
Telcom Devices	Newbury Park, CA	GaAs opto

(Continued)

Semiconductor Start-Up Update First Quarter 1987

Table 1 (Continued)

START-UP COMPANIES

Companies Formed in 1985

Company	Location	Product
ABM Semiconductor, Inc.	San Jose, CA	AlGaAs Opto
ACTEL Corporation	Sunnyvale, CA	ASICs
Acumos, Inc.	San Jose, CA	CMOS ASICs
Advanced Linear Devices	Sunnyvale, CA	Linear
American Information Technology	Cupertino, CA	MPUs
Anadigics, Inc.	Warren, NJ	GAas A/D converters
BT&D Technologies, Inc.	United Kingdom	Optoelectronics
Catalyst Semiconductor	Santa Clara, CA	Memory
Chips & Technologies	Milpitas, CA	Micros
Dolphin Integration	Europe	ASICs
European Silicon Structures	West Germany	ASICs
GAIN Electronics	Somerville, NJ	GaAs
Hittite Microwave Corp.	Massachusetts	GaAs
Intercept Microelectronics	San Jose, CA	ASICs
Level One Communications	Folsom, CA	Linear
Orbit Semiconductor	Sunnyvale, CA	Foundry
Sahni Corporation	Sunnyvale, CA	Closed (1986)
Saratoga Semiconductor	Cupertino, CA	Memory
Spectrum Semiconductor	Canada	ASICs
III-V Semiconductor	Arizona	GaAs
Tachonics Corporation	Bethpage, NY	GaAs
Topaz Semiconductor	San Jose, CA	DMOS ICs
Triad Semiconductor Intl.	Colorado	Memory
Wolfson Microelectronics	United Kingdom	ASICs

Source: Dataquest
August 1987

Semiconductor Start-Up Update First Quarter 1987

NEW COMPANIES

American Information Technology

American Information Technology (AIT), a start-up company in Cupertino, California, was formed in 1985. AIT has recently raised additional financing, is in its development stage, and will be releasing information on its activities later this year.

Gazelle Microcircuits, Inc.

Gazelle was founded in the summer of 1986 by ex-GigaBit Logic executives Andy Graham and David McMillan. In January 1987, Jerry Crowley, vice chairman and founder of Oki Semiconductor, left Oki to head the start-up. Gazelle is located in Sunnyvale, California, and was recently financed by Hambrecht & Quist and Kleiner, Perkins, Caufield & Byers. The company also has floated 900,000 shares of preferred stock at $1 a share and currently is putting together another round of financing. Gazelle will concentrate on very high speed digital ICs for military, telecommunications, and EDP applications.

Graphics Communications Technology

Ascii Inc., a Japanese software house, established a graphics start-up called Graphics Communications. Graphics Communications will be 70 percent financed by the joint MITI/MPT (Ministry of Posts & Telecommunications) Key Technology Research Promotion Center and 30 percent by 11 companies, including Iwasaki Communications, Mitsui Corporation, and Okura Electric. Ascii will maintain a 5 percent share in the venture, which will be headed by Ascii vice president, Kazuhiko Nishi.

Innovative Silicon Technology

Innovative Silicon Technology (IST) is a spin-off of SGS that was formed in May 1986 and is headed by Piero Martinotti and others from Motorola. SGS transferred the assets of its ASIC activities to IST, which will use a 1.5-micron, double-layer metal and direct-write on E-beam. It is providing gate arrays in one and one-half weeks and standard cells in two weeks. IST is planning a new R&D facility, fab, and operations, separate from SGS, that will be located northeast of Milan, Italy. Products are expected in 1987.

Semiconductor Start-Up Update First Quarter 1987

MemTech

MemTech was formed to acquire Intel's bubble memory operation. In February 1987, Intel signed the final purchase agreement covering the sale of Intel's magnetics operation to MemTech. The final sale terms provide for the transfer of Intel bubble memory manufacturing and test equipment, inventory, product designs, personnel, and manufacturing and quality specifications to MemTech for an undisclosed price. Operations will remain in Folsom, California.

MemTech is affiliated with Helix Systems & Development, Canoga Park, California, a bubble memory systems manufacturer. MemTech is headed by Richard H. Loeffler, formerly chairman and chief executive of Helix, and William H. Almond, the former head of Eaton's microlithography division. MemTech offers a complete bubble memory product line that includes 1- and 4-megabit bubble memory components and support circuitry, bubble memory boards, subsystems, and a cassette product, all available in a variety of temperature ranges.

Solid State Technologies

Solid State Technologies is a 1986 start-up located in San Jose, California. The company was founded by George W. Brown, presently serving as president, and Marshall Wilder, vice president of operations, both from Advanced Micro Devices. Initially, Solid State Technologies plans to offer high-performance bipolar memory products. It is presently in its developmental stage and will be releasing more information in a few months.

Taiwan Semiconductor Manufacturing Corp.

Taiwan Semiconductor Manufacturing Corp. (TSMC) has been set up as a foundry operation that will produce a wide variety of ICs. Taiwan's Executive Yuan, or legislature, has earmarked monies from its Development Fund for a 48 percent stake in the new company. N.V. Philips will take a 27.5 percent share in the $150 million investment in TSMC.

Chips are now being produced at the company's initial fab, which is capable of producing 10,000 6-inch wafers per month. In the second phase, which will be completed in 1988, it will be able to produce 30,000 1.5-micron, 6-inch wafers per month.

Telcom Devices Corp.

Telcom Devices was formed in early 1986 to offer indium gallium arsenide (InGaAs) photodiodes and indium gallium phosphide (InGaP) light-emitting diodes. Telcom Devices is a subsidiary of Opto Diode Corp. (ODC) and is operating from ODC's facilities in Newbury Park, California. The two companies share clean room and manufacturing space. Larry Perillo, formerly with Rockwell, is director of optoelectronics materials. Telcom Devices started volume production of its first product in May 1986, an InGaAs PIN photodiode for fiber-optic applications.

FINANCING

Table 2 lists by company the funding raised in the fourth quarter of 1986 and the first quarter of 1987.

Table 2

ADDITIONAL START-UP FINANCING

Company	Date	Round	Amount	Sources
Anadigics Inc.	Nov. 1986	2	$10.0M	Century IV Fund; Englehard Corp.; Memorial Drive Fund; Metropolitan Life Insurance Co.
California Devices Inc.	Oct. 1986	3	$ 3.9M	Alan Patricof Assoc.; Partners; Brentwood Assoc.; Dougery, Jones & Wilder; Edelson Technology; Hook Partners; InnoVen Group; John Hancock Ventures; Lambda Fund; Merrill Lynch Venture; Oxford Partners; J.F. Shea & Co.; Xerox
Cirrus Logic Inc.	Nov. 1986	3	$ 4.5M	Brentwood Assoc.; Institutional Venture Partners; Kuwait & Middle East Financial; Nazem & Co.; New Enterprises Assoc.; NY Life Insurance; Robertson, Colman & Stephens; Technology Venture

(Continued)

Table 2 (Continued)

ADDITIONAL START-UP FINANCING

Company	Date	Round	Amount	Sources
Elantec Inc.	Dec. 1986	4	$ 7.8M	Harvard Mgmt.; Cypress Fund; Morgan-Holland; New England Capital; Riksa Trust; Sequoia Capital; St. James Venture Capital Fund; U.S. Venture Partners; CEI; and others
European Silicon Systems	Nov. 1986	Equity	$ 9.0M	Banque International a Luxembourg; European Investment Bank
Krysalis Corp.	Dec. 1986	1	$ 3.0M	Columbine; Crosspoint Venture Partners; Meadows Resources; OSCCO Ventures
Laserpath Corp.	Dec. 1986	2	$ 4.5M	Crosspoint Venture Partners; Emerging Growth Partners; GE Venture Capital; Wolfensen Assoc.
Performance Semiconductor Inc.	Nov. 1986	1	$10.0M	Advanced Technology Ventures; Albion Venture Fund; Asset Mgmt.; Brentwood Assoc.; DSV Partners; Harvard Mgmt.; IAI Venture Partners; North Star Ventures; Northwest Venture Capital; Reynolds Creek Ltd. Partnership; L.F. Rothschild, Unterberg Towbin; Taylor & Turner; U.S. Venture Partners; VenWest Partners
Seeq Technology Inc.	Oct. 1986	Private placement post IPO	$ 6.0M	Bridge Capital; GE Venture Capital; Hillman Ventures; John Hancock; Kleiner, Perkins, Caufield & Byers
Sensym Inc.	Aug. 1986	3	$ 1.5M	Becton & Dickinson

(Continued)

Table 2 (Continued)

ADDITIONAL START-UP FINANCING

Company	Date	Round	Amount	Sources
EVitesse Electronics Corp.	Feb. 1987	2	$10.0M	Sequoia Capital and others
Xilinx Inc.	Jan. 1987	3	$ 3.4M	Fleming Ventures Ltd.; Hambrecht & Quist; Kleiner, Perkins, Caufield & Byers; Interfirst Venture; Interwest Partners; Matrix Partners; Morgan Stanley; Rainier Venture Partners; Security Pacific Venture Capital; J. H. Whitney

Source: Dataquest
August 1987

COMPANY ANNOUNCEMENTS

Acrian Inc.

Acrian Inc. has named Gary Irvine president and chief operating officer. Jack Harris remains as chairman and chief executive. Mr. Irvine, formerly president of EH Electronics, will be responsible for new products and market expansion as well as possible acquisitions by the company.

Adaptec, Inc.

Adaptec announced plans to open a subsidiary in Singapore in the first quarter of 1987 to manufacture surface mount controllers. The new company, called Adaptec Manufacturing (Singapore) Private Ltd., planned to begin pilot production in April and full production in early summer.

Altera Corporation

Altera entered the military market with its EPLDs, offering the first products to meet Class B specifications of MIL-STD-883 Rev. C--the EP310 and EP1210.

Semiconductor Start-Up Update First Quarter 1987

California Devices Inc.

Douglas Ritchie has been elected chairman of the board of CDI in addition to his responsibilities as president and chief executive officer. Wilmer R. Bottoms, the former chairman, has been named vice chairman.

Custom MOS Arrays

Custom MOS Arrays has merged with California Micro Devices (CMD). CMD was incorporated in 1980 to acquire the assets of a thin-film company. No changes in personnel assignments are planned. Handel Jones, formerly president of Custom MOS Arrays, will be the president and chief operating officer of the new combined company.

Cypress Semiconductor Corporation

Cypress announced that it will file a registration statement with the SEC to offer 4,400,000 shares of common stock. The proceeds will be used as working capital and to increase its capital base.

Harris Microwave Semiconductor

Harris Microwave Semiconductor has transferred its CAE tools developed for CMOS digital ASICs in Melbourne, Florida, to its GaAs operation in Milpitas, California. The company has set up a commercial GaAs standard cell operation.

Integrated Device Technology Inc.

Leonard C. Perham, former vice president and general manager of IDT's SRAM Division, has assumed the duties of president and chief operating officer of Integrated Device Technology Inc. John Carey remains as chief executive officer and chairman of the board.

International Microelectronic Products Inc.

Barry Carrington, president, has been promoted to chief executive officer from chief operating officer. Mr. Carrington succeeds George W. Gray, who remains IMP's chairman.

Krysalis Corporation

Franc R.J. deWeeger has joined Krysalis as president and chief executive officer. Joseph T. Evans, who was a Krysalis cofounder and served as the company's president, now becomes vice president of research and engineering. Mr. deWeeger was previously at ASM International, where he served as president since 1984; he remains on the ASM America board of directors. Before that, he spent two years as president of Zilog, Inc.

Lattice Semiconductor Corporation

Lattice announced that Rahul Sud resigned as president and Jay McBride resigned as general manager. C. Norman Winningstad, chairman of the board, is acting CEO. Lattice also announced that Rahul Sud, Jay McBride, S. Robert Breitbarth, and Kishan C. Sud resigned from Lattice's board of directors.

Linear Technology Corporation

LTC has established a Japanese company to strengthen its services to its Japanese customers. The company is called Linear Technology K.K. and is wholly subscribed by the U.S. parent. Robert Swanson has been appointed president, and Atsushi Nakata has been appointed general manager.

LSI Logic Corporation

LSI Logic has reorganized into four strategic business units with separate profit and loss responsibilities. The four units and vice presidents heading them are: Components and Technology, Cy Hannon; Engineering Services, Ven Lee; Software and Computer Services, Jim Koford; and Military/Aerospace, Norm Chanoski. Each of the four vice presidents will report to George Wells; each unit will be supported by decentralized sales, marketing, purchasing, finance, and MIS staff.

LSI Logic also plans to offer part of its European affiliate, LSI Logic Europe, on London's second-tier Unlisted Securities Market (USM). More than 80 percent is owned by the parent company, with the remainder held by local private investors, insurance companies, and other financial interests. The most visible industrial investor in LSI Logic Europe is Sulzer Brothers AG, a Swiss engineering firm.

In West Germany, LSI Logic Europe is building a mass production assembly and test facility in Braunschweig, which will form part of the corporation's worldwide capacity. It should be operational later this year, acting as a subcontractor to the U.S. parent company.

Semiconductor Start-Up Update First Quarter 1987

Micron Technology, Inc.

Micron has placed approximately 3,500,000 shares of common stock with certain foreign institutional investors at a price of $4.375 per share in a private placement assisted by Montgomery Securities.

Samsung Semiconductor Inc.

Samsung announced that it is building a new facility in San Jose, California, which will house its headquarters, R&D operations, and research fab. Included in the new 80,000-square-foot facility will be a 12,000-square-foot fab equipped with 6-inch wafer processing equipment.

Seeq Technology Inc.

Monolithic Memories Inc. purchased a 16 percent equity in Seeq Technology for $4 million. The two companies also have agreed to a four-year joint product and technology program to develop CMOS PLDs. Seeq received MIL-STD-883 Rev. C Class B specifications for its products.

Sierra Semiconductor Corporation

Sierra Semiconductor announced Stephen Forte as president of its new European joint venture, Sierra Semiconductor B.V., formed in June 1986 in the Netherlands.

Silicon Systems Inc.

Stephen E. Cooper, formerly senior vice president and general manager of the Microperipheral Division of Silicon Systems, succeeds Carmelo J. Santoro as president and chief operating officer. Mr. Santoro remains as chairman and chief executive officer.

Telmos Inc., Universal Semiconductor Inc., and Zytrex

Investment Management International Inc. (IMI), the finance group that acquired Zytrex last spring, has acquired Universal Semiconductor and the assets and product rights of Telmos Inc.

Semiconductor Start-Up Update First Quarter 1987

Vitesse Electronics Corp.

The Vitesse Electronics' Integrated Circuit Division raised $10 million and is now an independent company, called Vitesse Semiconductor Corporation. Dr. Louis R. Tomasetta, former president of the IC Division, is president and CEO of the new company. Vitesse Semiconductor will remain in the 70,000-square-foot existing facility and will use the new funding to develop additional products and expand into higher-volume production.

VLSI Technology, Inc.

VLSI Technology's Government Products Division in Phoenix, Arizona, has been certified for production of devices that are fully compliant with MIL-STD-883C.

VLSI Technology completed the acquisition of Visic, Inc. Visic will maintain its own board of directors, which will include members of both Visic and VLSI Technology. Products designed and developed by Visic will be manufactured in the VLSI Technology facility and marketed under the VLSI name.

VLSI Technology's ASIC operation is now a separate division, joining the memory, logic, and government divisions. Former vice president of design and technology, Douglas G. Fairbairn, has been promoted to the new position of vice president and general manager of the new ASIC Division. He will continue to report to both chairman Alex Stein and president Henri Jarrat.

Xicor, Inc.

Xicor announced that it has completed MIL-STD-883C Class B qualification for its X28256 EEPROM device. This qualification affects all versions of the X28256 in the 32-pad leadless chip carriers.

Table 3 lists some recent alliances involving start-up companies.

Table 3

ALLIANCES INVOLVING START-UP COMPANIES

Company	Date	Comments
Altera WaferScale Sharp	Jan. 1987	Altera and WSI agreed to a 5-year technology exchange to develop new user-configurable logic products; Sharp will manufacture the products using WSI's process.
Chips Ascii Corp.	Sept. 1986	Chips & Technologies and Ascii, a major software company in Japan, will start a new company to develop communication products. Chips will design the products; manufacturing will be done by companies in Japan. Chips and Ascii will hold equal shares of the majority interest in the new venture.
Chips NSC	Nov. 1986	National Semiconductor will second source Chips & Technologies CMOS ICs in exchange for fabrication services. National is Chips' first U.S. source.
Cirrus Logic Silicon Systems	Oct. 1986	Cirrus Logic and Silicon Systems will exchange controller and buffer manager functions and mutually second source the ASICs. Both chips will be processed in 2-micron CMOS.
Crystal Asahi Chemical	Jan. 1987	Asahi Chemical acquired an 8 percent share in Crystal Semiconductor for about $4 million. Asahi will provide foundry services in exchange for a license to all of Crystal's existing products and to be its principal distributor in the Far East. Both companies will develop new products.
Custom Silicon NCR	Feb. 1987	NCR has licensed CSi's standard cell library, including 342 TTL macrocells and microcomputer building blocks of up to 5,863 gates. CSi's library was built from NCR's existing library, which CSi licensed.

(Continued)

Table 3 (Continued)

ALLIANCES INVOLVING START-UP COMPANIES

Company	Date	Comments
ES2 N.V. Philips TI	Feb. 1987	Texas Instruments Ltd. of England and Philips International N.V. will offer accelerated prototyping for the SystemCell Library of standard cells in cooperation with ES2. The SystemCell Library is the result of a collaborative relationship between TI and Philips who provide high volume manufacturing and standard prototyping.
ICT Asahi Chemical	Jan. 1987	Asahi Chemical Industry will receive technology from ICT (International CMOS Technology) and will also market its EEPROMs.
IDT VTC, Inc.	Jan. 1987	VTC will second source Integrated Device Technology's FCT product line of TTL-compatible CMOS logic devices.
iLSi Sumitomo Corp.	Dec. 1986	Sumitomo licensed ASIC design technology from Integrated Logic Systems Inc. (iLSi); in addition to royalty payments, iLSi has gained rights to use any foundries Sumitomo uses.
IMP Micro Linear MBB	Aug. 1986	International Microelectronic Products and Micro Linear have agreed to transfer ASIC design know-how to Messerschmitt-Bolkow-Blohm GmbH over a three-year period.
Lattice SGS	Feb. 1987	Lattice Semiconductor signed a technology agreement with SGS Semiconductor, giving SGS a license to second source Lattice's GAL products. SGS will manufacture GAL products for Lattice, and both companies will cooperate on the design of future PLD products.
Seeq MMI	Nov. 1986	Monolithic Memories purchased a 16 percent equity in Seeq for $4 million. The companies also agreed to a 4-year joint product and technology program to develop CMOS PLDs.

(Continued)

Table 3 (Continued)

ALLIANCES INVOLVING START-UP COMPANIES

Company	Date	Comments
Seeq Motorola	Dec. 1986	Seeq and Motorola agreed to work on a multimillion-dollar EEPROM technology project.
XTAR Fairchild	Sept. 1986	Fairchild agreed to second source XTAR's 2-chip set graphic MPU.

Source: Dataquest
August 1987

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Semiconductor Start-Up Update Second Quarter 1987

The second-quarter update on start-up companies includes information on new company formations, acquisitions, and company announcements made in the second quarter. It also includes information on financing raised and agreements made in the first half of 1987.

HIGHLIGHTS

Second-quarter highlights include the following:

- Four companies were formed in 1987.
- European Silicon Structures and Microwave Technology have made acquisitions.
- VTC became a wholly owned subsidiary of Control Data Corporation.
- Approximately $238.3 million was raised in new and additional funding in the first half.
- Twenty-six agreements were signed by start-up companies in the first half.
- Significant management announcements were made.
- International Microelectronic Products went public.
- VLSI Technology broke ground on a 25,000-square-foot wafer fab in Texas.

NEW COMPANIES

GL Micro Devices

GL Micro Devices was formed in February 1987 to develop high-performance, advanced CMOS products. The company was founded by Norman Godinho and Frank Lee, both formerly with Integrated Device Technology. Glenwood Management and El Dorado Ventures participated in $2.4 million seed financing, which was completed in April of this year.

Mr. Godinho served as vice president and general manager of IDT's digital signal processing division, and Mr. Lee was codirector of IDT's corporate research and development group.

Semiconductor Start-Up Update Second Quarter 1987

LOGICSTAR Inc.

LOGICSTAR was formed in 1987 to design, manufacture, and sell high-performance PC AT logic, VLSI graphics, and local area network chips. The company is addressing the PC AT market and is using a VLSI design methodology to bring products to market quickly.

LOGICSTAR was formed by Mark Kaleem, who was formerly president of OSM Computer and Unilogic. Vice president of marketing is Saeed Kazmi, who was formerly with VLSI Technology Inc. in technical sales support.

LOGICSTAR's initial products are a five-chip PC AT chip set that is pin-for-pin compatible with Chips & Technologies' chip set, a monographics controller, a dual-channel NRZI encoder/decoder, and a STARLAN interface chip. Future products will include a VGA chip, PS/2 chip, 386 chip sets, additional data communication chips, and disk controllers.

Foundry services are being provided by companies in the United States and Japan.

Ramax Limited

Ramax Limited is an Australian-based company that is being formed through a $45 million joint venture between Australia's state of Victoria and other investors. A development company owned by the state of Victoria is providing $850,000, for which the state will receive between 7 and 13 percent equity in the company, with the balance in first-round equity coming from both U.S. and Australian investors. The financing should be complete by September 30.

Peter J. Solomon is executive director of Ramax, and Dr. Bruce Godfrey is manager of product and technology development. Dr. Godfrey has been an adjunct assistant professor at the University of Colorado and one of the researchers involved in developing technology the company will be using.

Ramax has licensed high-speed, nonvolatile memory technology using a ferroelectric semiconductor process and a companion technology that uses a thin-film process from Ramtron, an Australian R&D company located in Colorado Springs, Colorado. Ramax acquired a 12 percent stake in Ramtron for $8.0 million and paid $6.9 million in licensing fees.

Initially, the company will produce prototype silicon-based circuits using Ramtron's technology. Future plans include the manufacture of GaAs circuits using the ferroelectric thin-film technology under terms of a license that gives Ramax exclusive worldwide rights to use the Ramtron technology on GaAs.

Semiconductor Start-Up Update Second Quarter 1987

SIMTEK Corporation

On May 15, 1987, Dr. Richard L. Petritz and Dr. Gary F. Derbenwick announced the formation of SIMTEK Corporation, which will develop, manufacture, and market a broad range of advanced semiconductor products. The company will initially focus on new memory components for consumer, commercial, and government markets.

Dr. Petritz, a founder of Mostek and Inmos, will serve as chairman and chief executive officer of the company. Dr. Derbenwick, who was formerly product technology manager at Inmos, will serve as president and chief operating officer.

The initial capitalization for SIMTEK is from Nippon Steel Corporation of Japan, which will own about 20 percent of the company and have a seat on the board. Nippon Steel produced 28 million tons of steel products in 1986, with sales of $15 billion. The investment by Nippon Steel is part of a diversification plan to expand into other business areas.

SIMTEK's headquarters are located in Colorado Springs, Colorado. During the next three months, the company will be conducting studies for its permanent U.S. facilities, which will include a substantial manufacturing capability. The company plans to begin manufacturing within the next 18 months.

MERGERS AND ACQUISITIONS

European Silicon Structures

European Silicon Structures (ES2) is negotiating to acquire Lattice Logic Ltd., an Edinburgh-based silicon compiler software house. ES2 has been marketing Lattice Logic's compilers in Europe since 1985. The merger should give Lattice Logic financial security and the finances to develop software with ES2.

Microwave Technology, Inc.

Microwave Technology, Inc. (MwT), completed the acquisition of Monolithic Microsystems, Inc., of Santa Cruz, California, in June 1987. Monolithic Microsystems makes detector log video amplifiers (DLVAs), logarithmic video amplifiers (LVAs), and threshold detectors, based on its proprietary monolithic silicon LVA ICs. Monolithic Microsystems is manufacturing devices used in various electronic warfare systems and other defense electronic applications.

MwT designs, manufactures, and sells GaAs epitaxial materials, GaAs field-effect transistor devices and monolithic circuits, hybrid microwave ICs, and microwave subassemblies.

Monolithic Microsystems will operate as a wholly owned subsidiary of MwT and will continue its manufacturing operations in its 8,200-square-foot Santa Cruz facility.

VTC, Inc.

VTC has signed a merger agreement under which it will become a wholly owned subsidiary of Control Data Corporation, its largest investor and major customer. The companies declined to disclose the terms of the proposed purchase. Control Data has invested $56 million in VTC since it was founded and holds nonvoting preferred shares in the company that are convertible to 49 percent of the company's voting stock.

The arrangement provides VTC with revenue and financial support. VTC's founders, Thomas E. Hendrickson and John R. Hodgson, will continue to manage the company.

Table 1 lists financing raised by start-up companies in the first half of 1987.

Semiconductor Start-Up Update Second Quarter 1987

Table 1

FINANCING RAISED BY START-UP COMPANIES
FIRST HALF 1987

Company	Month	Round	Amount ($M)	Investors
Dallas Semiconductor	April 1987	3	$ 5.0	Abingworth; Alex Brown & Sons Emerging Growth Stocks; British Petroleum BP Ventures; HLM Partners; Merifin N.V.; New Enterprise Associates; Southwest Enterprise Associates; T. Rowe Price; Threshold Fund; Ventech Partners
Gigabit Logic	May 1987	3	$ 15.0	Analog Devices; Cray Research; Digital Equipment; First Interstate Capital; General Electric Venture; Interfirst Venture; New Enterprises Associates II; Riodan Venture; Union Venture
GL Micro Devices	April 1987	Seed	$ 2.4	Glenwood Management; El Dorado Ventures
International CMOS Technology	June 1987	3	$ 2.0	Undisclosed institutional investors
LSI Logic	April 1987	Eurobond Offer	$125.0	Convertible subordinated debentures offered on London's Unlisted Securities Market
Ramax Limited	June 1987	1	$ 0.8	State of Victoria, Australia

(Continued)

Table 1 (Continued)

FINANCING RAISED BY START-UP COMPANIES
FIRST HALF 1987

Company	Month	Round	Amount ($M)	Investors
Saratoga Semiconductor	March 1987	3	$ 11.5	Initial investors: Berry Cash Southwest Partners; Dougery, Jones & Wilder; Interwest Partners; Matrix Partners; MBW Venture Partners; Merrill, Pickard, Anderson & Eyre; Sierra Ventures; Sigma Partners; Weiss Peck & Greer Venture Partners
			$ 7.6	New investors: Bank of America Capital; HLM Management; John Hancock Venture Capital; New York Life Insurance; Security Pacific Capital; T. Rowe Price Associates
Vitesse Semiconductor	Feb. 1987	2	$ 10.0	Bryan & Edwards; J.H. Whitney; New Enterprises Associates; Oxford Venture Corporation; Robertson, Colman & Stephens; Sequoia Capital; Suez Technology Fund; Walden Capital
VLSI Technology	April 1987	Bond Offer	$ 48.75	Offered convertible subordinated debentures

(Continued)

Table 1 (Continued)

FINANCING RAISED BY START-UP COMPANIES
FIRST HALF 1987

Company	Month	Round	Amount ($M)	Investors
Xilinx	Jan. 1987	3	$ 3.4	Fleming Ventures Ltd.; Hambrecht & Quist; Kleiner, Perkins, Caufield & Byers; Interfirst Venture; Interwest Perkins; Matrix Partners; Morgan Stanley; Rainier Venture Partners; Security Pacific Venture Capital; J.H. Whitney
Zoran	April 1987	4	$ 6.8	Adler & Company; Concorde Partners; Elron Electronics; Grace Ventures Corp.; Kleiner, Perkins, Caufield & Byers; Mitsui & Company; Montgomery Securities; Vista Ventures; Welsh, Anderson & Stowe

Source: Dataquest
August 1987

Table 2 lists agreements start-up companies formed in the first half of 1987.

Table 2

AGREEMENTS WITH START-UP COMPANIES
FIRST HALF 1987

Company	Date	Comments
Altera WaferScale Sharp	Jan. 1987	Altera and WSI agree to a five-year technology exchange focused on developing new user-configurable logic products. Sharp will manufacture the products using WSI's process.
Altera Cypress	June 1987	Cypress Semiconductor Corporation and Altera Corporation announced a five-year technology development agreement focused on new high-performance, high-density, user-configurable logic products. Altera will provide the architecture, circuit design, and software support. Cypress will provide its CMOS process and EPROM device development and manufacturing capacity from its new Austin, Texas fab. The first devices, designated MAX (for Multiple Array Matrix), promise to extend the EPLD density capability up to 5,000 equivalent gates.
Catalyst Oki Electric	March 1987	Catalyst and Oki Electric agreed to a second-source agreement covering a wide range of CMOS EEPROMs. This is another phase of their continuing CMOS memory technology partnership, which was signed in July 1986. The two companies will jointly introduce a 1K serial EEPROM, which will be followed with 256-bit and 512-bit serial EEPROMs, 16K and 64K CMOS EEPROMs, and a 256K CMOS EEPROM that will be introduced at the end of the year.

(Continued)

Table 2 (Continued)

AGREEMENTS WITH START-UP COMPANIES
FIRST HALF 1987

Company	Date	Comments
CDI IST	April 1987	California Devices Inc. (CDI) and Innovative Silicon Technology (IST) have reached an agreement that provides for joint product development and second-sourcing of two families of ASICs using channelless ASIC architectures. The first family will be based on a 2-micron, double-metal layer CMOS and will have a complexity of up to 24,000 gates. The second family, which is slated for introduction in 1988, will be based on 1.5-micron technology and will have more than 100,000 gates.
Crystal Asahi Chemical	Jan. 1987	Asahi Chemical has acquired an 8 percent share in Crystal Semiconductor for about $4 million. Asahi will provide foundry services in exchange for a license to all of Crystal's existing products and for principle distribution rights in the Far East. Both companies will develop new products.
Custom Silicon NCR	Feb. 1987	NCR has licensed CSi's standard cell library, that includes 342 TTL macrocells and micro-computer building blocks of up to 5,863-gates. CSi's library was built from NCR's existing library, which CSi licensed.
Dallas Xecom	May 1987	Dallas Semiconductor Corporation and Xecom Inc. signed a second-source agreement giving both companies marketing rights for several of their existing products. In addition, the companies will cooperate on developing, manufacturing, and marketing future modem-related products--the area of Xecom's expertise. As part of the agreement, Dallas will alternate-source two of Xecom's modem components--the XE1251 and XE1253 modem development kits and the stand-alone XE0002 Data Access Arrangement unit, which is registered by the FCC. Xecom will second-source Dallas' SmartSocket and the SmartWatch families of products.

(Continued)

Table 2 (Continued)

AGREEMENTS WITH START-UP COMPANIES
FIRST HALF 1987

Company	Date	Comments
ES2 N.V. Philips TI	Feb. 1987	Texas Instruments Ltd. of England and Philips International N.V. will offer accelerated prototyping for the SystemCell Library of standard cells in cooperation with ES2. The SystemCell Library is the result of a collaborative relationship between TI and Philips, which provides high-volume manufacturing and standard prototyping.
GigaBit Logic Seattle Silicon WTC	April 1987	GigaBit Logic, Seattle Silicon Corp., and the Washington Technology Center (WTC) announced that a joint design project has resulted in the fabrication of a functional compiler-based GaAs IC design. The design is based on GigaBit's standard cell library and uses Seattle Silicon's Concorde Blue Chip Compiler. WTC provided design and engineering support and will be involved in the packaging and testing of the ICs. The device is equivalent to the 100K ECL 4-bit ALU (100181).
ICT Asahi Chemical	Jan. 1987	Asahi Chemical Industry will receive technology from International CMOS Technology (ICT) and will also market its EEPROMs.
IDT VTC	Jan. 1987	VTC will second-source Integrated Device Technology's FCT product line of TTL-compatible CMOS logic devices.
IST SDA Systems	May 1987	Innovative Silicon Technology Corp. (IST), a wholly owned subsidiary of SGS Corp., signed an agreement with SDA Systems Inc. to develop CAD systems based on SDA technology for use by IST customers.

(Continued)

Table 2 (Continued)

AGREEMENTS WITH START-UP COMPANIES
FIRST HALF 1987

Company	Date	Comments
Lattice SGS	Feb. 1987	Lattice Semiconductor signed a technology agreement with SGS Semiconductor, giving SGS a license to second-source Lattice's Generic Array Logic (GAL) products. SGS will manufacture GAL products for Lattice, and both companies will cooperate on the design of future PLD products.
Lattice National	May 1987	National Semiconductor Corporation made a minority capital investment in Lattice Semiconductor Corporation and licensed its Generic Array Logic (GAL) technology. The five-year agreement includes codevelopment of denser architectures of both standard and in-system programmable GALs, as well as a new line of FPLAs and sequencer devices.
LTC TI	March 1987	Linear Technology Corporation (LTC) and Texas Instruments Inc. (TI) agreed to a five-year alliance for advanced linear ICs. TI will select six products each six months from LTC's line to manufacture and market as TI parts. TI will pay LTC $500,000 and undisclosed royalties on a descending scale for a 10-year period and will directly purchase a number of products for resale. In addition, TI will invest approximately $1 million for warrants to purchase 735,000 shares of LTC stock at $17.50 per share over a four-year period. TI is also free to add the LTC parts to its standard cell library in exchange for specific royalty payments outlined by the agreement. LTC designers are to gain access to TI's CAD system and will also be able to design parts, thereby taking advantage of TI's advanced processes. The two companies plan joint designs in the near future. LTC will be able to situate its own test systems at TI assembly facilities.

(Continued)

Table 2 (Continued)

AGREEMENTS WITH START-UP COMPANIES
FIRST HALF 1987

Company	Date	Comments
LSI Logic Case Technology	March 1987	Case Technology Inc. and LSI Logic have completed a joint development effort that allows LSI Logic's LL5000, LL8000, and LL9000 schematic libraries to be designed on Case Technology's PC-based workstations.
LSI Logic Logic Automation	May 1987	LSI Logic Corporation and Logic Automation Inc. have signed a joint development agreement to make available LSI Logic's LL5000, LL7000, LL8000, and LL9000 channeled gate arrays on Logic Automation's Mentor Graphics workstations.
LSI Logic ASIX Systems	June 1987	LSI Logic Corporation will license design verification software to ASIX Systems Corporation of Fremont.
Samsung Intel	June 1987	Samsung Semiconductor will supply Intel with 64K, 256K, and 1Mb DRAMs, which Intel will sell to its customers in the United States. Shipments will begin from Korea in July.
Tachonics CMD	March 1987	California Micro Devices Corporation (CMD) signed an agreement with Tachonics for the production of gallium arsenide (GaAs) based ICs. Tachonics will manufacture the commercial and military products, and CMD will provide cell design and tools in the 0.5- to 1.0-micron range. Initial products will be a series of GaAs gate arrays with 500 to 2,500 gates and with radiation-hardened capabilities.

(Continued)

Table 2 (Continued)

AGREEMENTS WITH START-UP COMPANIES
FIRST HALF 1987

Company	Date	Comments
TriQuint TRW	June 1987	TRW Components and TriQuint Semiconductor have agreed to jointly supply gallium arsenide devices for space applications. Both companies are working together on procedures for producing Class S-level GaAs components. TriQuint will provide microwave and digital GaAs technology in addition to foundry services.
Vitesse Ford	June 1987	Vitesse Semiconductor Corporation and Ford Microelectronics are close to a second-source agreement involving gallium arsenide (GaAs) IC foundry services. The two companies have an agreement in principle to develop common design rules. Vitesse and Ford each use an enhancement/depletion mode, self-aligned gate technology. Initially, the agreement involves custom and semicustom circuits but may be extended to standard products.
VLSI Technology TCMC	March 1987	VLSI Technology Inc. and Thomson Components-Mostek Corporation (TCMC) have signed a comprehensive agreement for mutual second-sourcing and future new product development in specialized memory products. Each company will provide five existing memory designs for immediate second-sourcing. Both companies will incorporate the devices into megacells for use in their respective ASIC product families and plan to develop future products. Products covered include FIFOs, dual-ported RAMs, cache-tag RAMs, and lithium cell-powered nonvolatile SRAMs.

(Continued)

Table 2 (Continued)

AGREEMENTS WITH START-UP COMPANIES
FIRST HALF 1987

Company	Date	Comments
VLSI Technology Zilog	May 1987	Zilog signed VLSI Technology Inc. as a second source for its Super8 microcontroller. Included in the agreement are the Super8, the Z8038 FIFO I/O interface unit, and the Z8060 FIFO buffer unit and FIFO expander.
VTC Inc. TRW Components	March 1987	VTC and TRW Components International have signed a three-year agreement to cross sample space-quality Class S devices. VTC will supply TRW with unpackaged, high-performance ICs that meet the military Class S specifications. The devices include radiation-hardened CMOS SRAMs and high-speed comparators, op amps, and transceivers that are manufactured with VTC's radiation-hardened bipolar technology. TRW will assemble, test, qualify, and market these devices to customers that require Class S products, including radiation lot qualification where required.
Weitek Hewlett-Packard	May 1987	Weitek Corporation and Hewlett-Packard (HP) have formed a supplier/end-user agreement involving product and manufacturing exchanges. HP will incorporate the Weitek model 2264/65 chip set for high-performance, floating-point computation in current and future HP Precision Architecture computers. HP will also manufacture the chip set using its 1.2-micron CMOS process.

Source: Dataquest
August 1987

Semiconductor Start-Up Update Second Quarter 1987

COMPANY ANNOUNCEMENTS

Altera Corporation

Altera and Monolithic Memories Incorporated (MMI) have settled the patent infringement suit brought against Altera by MMI. Altera agreed to entry of a consent of judgment, and the parties have agreed to license each other under certain patents in the programmable logic field.

Catalyst Semiconductor

Stephen Michael, one-time vice president of GE Semiconductor's Custom Integrated Circuit department, joined Catalyst as executive vice president and chief operations officer. He will have responsibility for all day-to-day operations at Catalyst, reporting directly to B.K. Marya, president and chief executive.

Dallas Semiconductor

Dallas Semiconductor began producing chips in a newly constructed $10 million wafer fabrication facility adjacent to its Dallas headquarters. The Class 1 facility produces CMOS chips with geometries down to 0.7 microns.

GigaBit Logic

GigaBit Logic named president and chief executive John Heightly chairman of the board. Mr. Heightly takes over the chairman's post from Henrich Krabbe, who will remain on GigaBit's board as director. Mr. Krabbe is vice president of new business development for Analog Devices, an investor in GigaBit.

GigaBit Logic announced that Cray Research, Inc., has increased its 1987 order to $5.5 million from $3.2 million. Cray will use the logic and memory device procured under this order to enter the next phase of development of a GaAs-based parallel processor supercomputer.

Integrated Device Technology (IDT)

IDT has established a company in Japan named Integrated Device Technology K.K. It is capitalized at $142,857 and plans to begin contract assembly in Japan, by Japanese semiconductor makers, sometime this year.

International Microelectronic Products (IMP)

IMP made an initial public offering of 6.5 million shares of common stock on June 10, 1987. The company provided 4.5 million shares and 2 million were from certain shareholders. The offering was underwritten by Shearson Lehman Brothers and Montgomery Securities. Proceeds will be used to acquire capital equipment, make leasehold improvements, redeem Series A preferred stock, and provide working capital for general corporate purposes. The company will have about 25 million shares outstanding after the offering.

IXYS Corporation

IXYS has relocated into a new 53,000-square-foot facility in San Jose. The facility, which is six-times larger than its former one, will be occupied by a highly automated assembly line and custom-packaging facility. The automated manufacturing line for commercial products is expected to be operational in eighteen months. IXYS plans to invest $2 million to $3 million in this line over the next two years.

Laserpath

Jim Hively, formerly general manager of Monolithic Memories Inc. semicustom division, has joined Laserpath as president and chief executive officer. Mr. Hively replaces former Laserpath president Michael Watts, who resigned last summer to participate in venture financing. He will report to Laserpath chairman John Mumford.

Lattice Semiconductor Corporation

Lattice filed for Chapter 11 protection to ensure that new funding will be applied only toward financing the company's ongoing operations.

LSI Logic Corporation

LSI Logic announced that it will take its Canadian affiliate, LSI Logic Corporation of Canada Inc., public and offer 4 million newly issued shares. The company plans to raise more than $20 million in the offering.

LSI Logic and Sun Microsystems Inc. announced that they are joining forces to support San Jose State University with the establishment of an ASIC laboratory (ASIC Laboratory Project) at the university. LSI will contribute instructional versions of its LDS-III logic design and verification software and instructional versions of a macrocell library to develop ASICs. Sun Microsystems will donate the SUN-3/160C color workstation and three SUN-3/50 monochrome workstations, as well as the operating system (SunOS) and networking software.

NMB Semiconductor Corporation

William C. Connell, vice president of NMB (USA) Inc., is acting president of NMB Semiconductor. Gary Ater, who was vice president and general manager of U.S. Operations, has left NMB Semiconductor to join Vitelic Corporation as vice president of Sales and Worldwide Marketing.

NMB Semiconductor relocated its domestic headquarters to Garden Grove, California, in April. NMB will share existing facilities with HI-TEK Corporation, another subsidiary company of NMB (USA) Inc. The new location provides additional space for engineering and test and evaluation functions. The existing Santa Clara, California, facility will be maintained as a regional office for the northwestern United States.

The new location is:

11621 Monarch Street
Garden Grove, CA 92641
(714) 897-6272; fax: (714) 891-0895; Telex: 67-8486

Samsung Semiconductor Inc.

Samsung Semiconductor, Goldstar Semiconductor Inc., and Hyundai Electrical Engineering Co. announced that they are preparing to launch full-scale production of a 1Mb DRAM chip jointly developed by the three South Korean firms last year.

Samsung Semiconductor formally opened its national headquarters in San Jose. The new $36 million facility will be used for administration, including sales, marketing, and product support, as well as for chip manufacturing. The company employs 250 people at the site and expects to increase that number to 400 within a year.

Semiconductor Start-Up Update Second Quarter 1987

Silicon Systems Inc.

Chairman Carmelo J. Santoro retook operational control of Silicon Systems in May 1987, after Stephen E. Cooper, president and chief operating officer, and John V. Crosby, senior vice president, resigned.

Mr. Santoro said the reason for the change was to move toward a leaner, more efficient organization to "substantially improve profitability."

Taiwan Semiconductor Manufacturing Company (TSMC)

Dr. Morris Chang, former president and chief executive officer of General Instrument Corporation and president of the Industrial Technology Research Institute (ITRI) in Hsinchu, was made chairman of TSMC. Dr. Chang is also chairman of United Microelectronics Corporation.

Jim Dykes, who set up General Electric Company's Semiconductor Division, will join TSMC as president and chief executive officer.

Stephen L. Pletcher, who had been vice president of sales and marketing for GE Semiconductor, was named director of the new North American and European marketing and sales operation of TSMC.

TSMC, formed in late 1986, has already made its first wafer shipment from its 6-inch CMOS fab line in Hsinchu, Taiwan.

Three-Five Semiconductor Corp.

Three-Five Semiconductor has closed down its gallium arsenide facility in Troy, Michigan, idling about 50 workers.

United Microelectronics Corporation (UMC)

Dr. Morris Chang has been elected chairman of UMC. Dr. Chang is also chairman of the newly established Taiwan Semiconductor Manufacturing Corporation (TSMC) and president of the Industrial Technology Research Institute (ITRI) in Hsinchu. Formerly, Dr. Chang was a vice president at Texas Instruments and president and chief executive officer of General Instrument Corporation.

Vitesse Semiconductor

Vitesse has elected Pierre R. Lamond, cofounder of National Semiconductor and a general partner of Sequoia Capital, as chairman of the board. Mr. Lamond recently organized a $10 million financing of Vitesse and also serves on the boards of Cypress Semiconductor, Convex Computer, and several private companies.

VLSI Technology Inc.

VLSI Technology has broken ground on a 25,000-square-foot 6-inch wafer fabrication facility in San Antonio, Texas. Initially, the plant, equipped with a Class 1 clean room, will fabricate CMOS ASIC devices with minimum feature sizes down to 1.2 microns. The company plans features below 1.0 micron. The facility is expected to begin operation with 100 employees in late 1988.

VLSI Technology Inc.

VLSI Technology sold $48.75 million worth of 7 percent subordinated debentures convertible to common stock in an issue managed by Goldman Sachs & Co., Hambrecht & Quist, and Cowen & Co. VLSI plans to use money to fund new ASIC designs and defray expenses incurred by acquiring Visic Inc. and finance the new fab under construction in San Antonio, Texas.

In April, VLSI Technology repurchased a $7.6 million warrant that had been issued to Bendix Corporation six years ago.

VTC Inc.

VTC announced that it was awarded a $7.5 million contract from Control Data Corp., Government Systems Division, to supply chips for the U.S. Navy's AN/AYK-14(V) standard airborne computer. The contract calls for the production of five VLSI chip types designed with VTC's 1-micron CMOS standard cell library.

Xicor, Inc.

In April 1987, Xicor announced a public offering of 2.1 million shares of common stock at a price of $11.50 with Montgomery Securities and Smith Barney, Harris Upham & Co. Incorporated acting as underwriters. Net proceeds will be used for repayment of a bank debt of approximately $1.5 million and the balance will be added to working capital.

Intel Corporation has terminated a contract worth more than $7 million with Xicor on EEPROM technology and has begun end-of-life procedures on 64K and 256K ICs.

Zoran Corporation

John Ekiss resigned as president and chief executive officer of Zoran. Before joining Zoran in mid-1985, Mr. Ekiss was general manager of Intel's special components division. Terry Martin, vice president of operations, is acting president and chief executive.

ZyMOS Corporation

David Handorf has joined ZyMOS as president and chief executive officer from VLSI Technology Inc., where he was general manager of application-specific memories. He replaces the president's office of Haller Moyers, B.J. Chang, and Alex Young, who were appointed to serve until a successor was named.

New Japanese Research Labs

"Good imitators, but poor inventors." For years, Japanese industry has been strong in manufacturing, but weak in innovative research. However, DATAQUEST believes that this situation is rapidly changing. As shown in Table 1, Japanese electronics makers will open at least 78 basic research laboratories between 1984 and 1988. These laboratories will focus on a wide variety of leading-edge technologies, such as 4Mb and 16Mb DRAMs, 32-bit MPUs, standard cells, 3-dimensional CAD systems, VLSI design expert systems, automotive electronics, telecom ICs, optoelectronics, gallium arsenide, bioelectronics, voice recognition/synthesis, ceramic packaging, diamond substrates, and new materials. Given an average investment of $25 million to $33 million each, we estimate that these laboratories represent a total investment of between $1.9 billion and $2.5 billion.

What impact will these laboratories have on the West? DATAQUEST believes that 1986 will be a major turning point for Japanese industry. We expect an increasing flow of innovative products from Japan within the next few years. To remain internationally competitive, western companies must continue investing heavily in R&D and improve their manufacturing capabilities.

Table 1

NEW JAPANESE ELECTRONICS R&D LABORATORIES (1984-1988)

Company	Research Activities (Location)	Opened	Millions of Dollars
Asahi Chemical	Gate arrays, standard cells (Atsugi)	12/85	$ 25.0
Asahi Optical	Optical disks (Englewood, Colorado)	1985	$ 0.5
Canon	Materials, AI (Atsugi)	02/85	$ 50.0
Data General Japan	Minicomputers (Koda)	12/85	$ 5.0
Dupont Japan	Electronics (Yokohama)	11/86	$ 75.0
Fuji Photo Film	CMOS image sensors	1985	N/A
Fujitsu	CAD, supercomputers, ICs (Kawasaki)	12/87	$100.0
Fujitsu	Mie R&D building postponed	1985	N/A
Fujitsu	Home electronics (main plant)	09/86	$ 17.5
Fujitsu/ Tohoku Digital	HEMT, opto, GaAs center (Sendai)	1985	$ 0.5
Hitachi	64Mb DRAM, biochips (Tokyo Central)	10/85	N/A
Hitachi	Telephone exchange software (Atlanta)	1985	N/A

(Continued)

New Japanese Research Labs

Table 1 (Continued)

NEW JAPANESE ELECTRONICS R&D LABORATORIES (1984-1988)

Company	Research Activities (Location)	Opened	Millions of Dollars
Hitachi Chemical	Electronics (Tsukuba)	1988	N/A
Hitachi Works	Bioelectronics (Kokubu)	02/85	N/A
Hokushin Electric	Ceramic components (Showaza)	02/86	$ 3.5
Honda	Reseach office (California)	09/84	N/A
IBM Japan	Computers, OA, workstations (Daiwa)	07/85	N/A
Japan Automation	CAD/CAM (Fuji)	03/85	$ 15.0
Japan Victor (JVC)	3-micron LSIs (Yamato)	04/85	N/A
JIRA	Laser technology center (Chiba)	1985	$ 1.0
Kanto Electronics	Joint semiconductor R&D (Nagano)	1985	N/A
Kanto Electronics	ICs, peripherals (Silicon Valley)	1984	N/A
Kawasaki Steel	New IC materials (Kawasaki)	03/85	N/A
KDD	Switching, software (Kamifuku-Oka)	02/88	$ 25.0
Kobe Steel	Research office (North Carolina)	09/84	N/A
Konishiroku	New materials (Silicon Valley lab)	03/85	$ 0.3
Kyocera	Electronic materials (Vancouver, WA)	1985	$ 10.0
Kyowa Electric	New materials (Chofu)	09/85	$ 5.0
Matsushita Electric	Submicron 16Mb DRAMs (Kadoma)	10/85	$100.0
Matsushita Electric	Biochips, thin film (Kawasaki)	04/86	$ 3.0
Matsushita Electric	R&D centers (Taiwan & West Germany)	1986	N/A
Matsushita Electronics	4Mb, next-generation ICs (Tokyo)	09/85	$ 80.0
Matsushita Reiki	Electronics (East Osaka)	07/85	$ 10.0
Mazda	Electronics (Yokohama)	1986	N/A
Minolta	Optoelectronics, thin films (Osaka)	11/84	$ 15.0
Mitsubishi Electric	Optical components (Obune)	08/85	$ 15.0
Mitsubishi Electric	Semiconductors (Research Triangle)	1984	N/A
Mitsubishi Electric (Horizon Research)	Computers, systems, software, (Waltham, MA; 35 engineers)	1984	
Mitsubishi Electric	4Mb DRAMs, x-ray, E-beam (Itami)	4/86	$106.0
Mitsubishi Electric	Original CMOS MCUs	1985	N/A
Mitsubishi Electric/ Mitsubishi Kasei	Joint materials research	11/85	$ 1.5
MITI/MPT	Basic technology research center	1986	$ 56.0
MITI/STA	New joint R&D system (Tsukuba)	1985	N/A
MITI/Tokyo University	Bioholonics Computer (Tsukuba)	1985	N/A
Nakamichi	Nonaudio electronics (Torrance, CA)	09/84	N/A
NEC	VLSI, AI, bioelectronics (Tsukuba)	06/87	$ 65.0

(Continued)

New Japanese Research Labs

Table 1 (Continued)

NEW JAPANESE ELECTRONICS R&D LABORATORIES (1984-1988)

Company	Research Activities (Location)	Opened	Millions of Dollars
NEC	32-bit MPU, GaAs, opto (Sagamihara)	1985	$100.0
NEC/MOE Physics Lab	Synchrotron for 1Mb+ DRAMs (Tsukuba)	01/85	N/A
Nippon Denso	Electronics (Aichi Prefecture)	08/89	N/A
Nippon Denso	Auto electronics (Michigan)	1986	N/A
Nissan Motors	Electronics	10/85	$ 8.0
NMB Semiconductor	CMOS DRAMS, EEPROMs (Tateyama)	1985	N/A
NTT/Hitachi/Toshiba	64Mb+ DRAM synchrotron (Atsugi)	1988	$ 30.0
NTT/KDD	Transmission think-tank	1985	$ 0.8
Oki Electric	1-micron VLSI R&D center (Hachioji)	1985	$ 46.5
Oki Electric	CAD, OA, LAN, E-mail (Takasaki)	11/85	$ 25.0
Ono Measuring	Sensors, measuring (Yokohama)	10/89	$ 25.0
Osaka Titanium	VLSI wafers (Saga)	09/85	$ 10.0
Ricoh	Optoelectronics, materials (Yokohama)	04/86	$ 60.0
Sanken Electric	Semiconductors (Saitama)	1985	$116.0
Sanyo	Bioelectronics, AI, FA (Tsukuba)	10/85	$ 38.5
Sharp	0.8- to 1.2-micron VLSI, (Fukuyama)	09/85	N/A
Sony	Optical media (Portland, Oregon)	1984	N/A
Sumitomo Electric	Optical fibers, materials (Raleigh, NC)	1984	N/A
Sumitomo Electric	Bioelectronics, new materials, optical communications (Yokohama)	1985	$147.0
Tamura Works	Semiconductors (Tokyo)	02/85	N/A
Tateishi Electric	Telecommunications (Machida)	03/86	$ 15.0
TDK	Components (Ichikawa)	N/A	N/A
Tokyo Electron (TEL)	Ultra LSI equipment (Nirasaki)	12/85	$ 8.0
Tokyo Sanyo	Semiconductors	02/86	$ 15.0
Toshiba	4 and 16Mb DRAMs (Kawasaki)	04/85	$110.0
Toshiba	ASICs, LANs, CAD (Horikawa)	01/87	$100.0
Toshiba Ceramics	16Mb ceramic substrates	1985	$ 11.6
Toyo Oxygen	IC gas equipment (Kawasaki)	1986	$ 10.0
Toyo Technica	CAD software (Atsugi)	12/84	$ 7.4
Yaesu Musen	Satellites, wireless (California)	1985	N/A
Yaskawa Electric	Robots, factory automation (Okura)	04/86	$ 7.5
Yazaki Industries	Hybrid ICs (Shizuoka)	06/85	N/A

N/A = Not Available

Source: DATAQUEST
May 1986

New Japanese Research Labs

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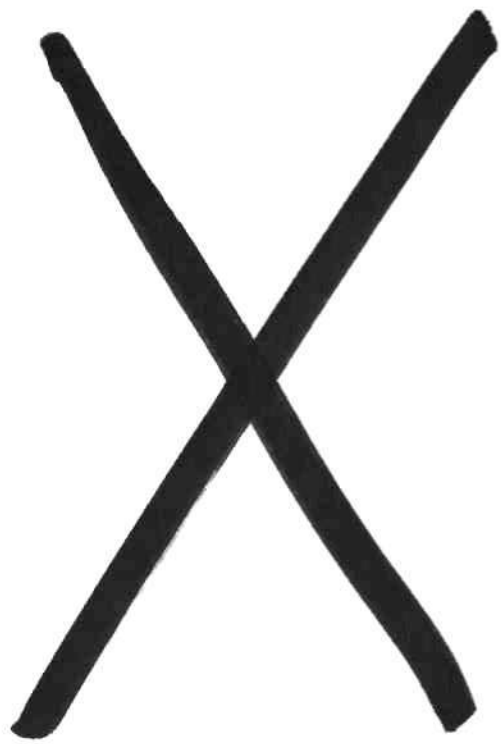


Government R&D

The following is a list of the material in this section:

- Government R&D Projects
- Optoelectronics Project
- Supercomputer Project
- Fifth-Generation Project
- Next-Generation Industries Program
- Future Electron Devices Project
- New Materials Project
- Bioelectronics Project
- Advanced Robotics Project

Government R&D Projects

MITI PROJECT TRENDS

Since 1980, MITI (Ministry of International Trade and Industry) has sponsored more than 30 national high-technology projects, as shown in Table 1. These projects are long-term, ranging from 5 to 10 years, and involve from 10 to 20 companies from the target industry. In recent years, Dataquest has observed the following trends in Japanese national R&D projects:

- Less MITI funding for national projects (about 25 percent), but more government funding (70 percent) for joint MITI-Ministry of Posts and Telecommunications (MPT) projects
- A shift since 1985 from device-oriented research to system-oriented research
- Growing interest in long-term basic research (10 years or more), such as optoelectronic ICs, 3-dimensional ICs, superlattice devices, and gallium arsenide devices and materials
- Joint MITI-MPT research through the Japan Key Technology Center
- Formation of privately-sponsored research consortiums with MITI support (e.g., diamond substrates and space-grown materials)

MITI projects are modeled after the highly successful VLSI project and follow a fairly predictable development schedule. Generally, MITI takes one year to organize the project and assign research responsibilities. Research gets underway during the second year, with patents and papers produced by the beginning of the third year. Due to the fierce competition among Japanese companies, we find it possible to forecast Japanese technology developments with some degree of accuracy. In general, participating companies begin to develop immediately prototype devices for in-house uses and sampling devices for the merchant market 18 to 24 months after the initial papers and patents are introduced. As a result, we anticipate that the current "patent wave" from MITI projects will be followed in the late 1980s by a "new product wave" and a "process wave" of process equipment used to develop these products.

Government R&D Projects

Table 1

MITI'S JOINT R&D PROJECTS
1966-2000

Project	Duration	BUDGET (M)
National Projects		
4th Generation Computer	1979-1983	$ 140.7
5th Generation Computer	1979-1991	$ 375.0
Automated Software Development (Sigma)	1985-1989	$ 156.3
Water Desalination System	1985-1989	$ 1.2
Large-Scale Projects		
Super High-Performance Computer System	1966-1971	$ 62.5
Desulfurization Process	1966-1971	$ 16.3
Olefin Production	1967-1972	$ 6.9
Undersea Remote-Controlled Oil Drilling	1970-1975	$ 28.2
Seawater Desalination	1969-1977	$ 41.9
Electric Car	1971-1977	$ 35.6
Pattern Information Processing System (PIPS)	1971-1980	$ 137.5
Aircraft Jet Engines (Phase 1)	1971-1981	$ 124.4
Automobile Control Technology	1973-1977	$ 45.6
Solid Urban Waste Resource Recycling	1972-1982	$ 78.9
High-Temperature Steelmaking Processes	1973-1980	$ 85.6
Alternative Energy Sources (Sunshine Project)	1974-2000	$1718.7
Asphalt-Based Olefin Production	1975-1981	$ 86.3
Resource Recovery (Phases 1 to 3)	1975-1982	$ 70.6
Aircraft Jet Engines (Phase 3)	1976-1981	$ 81.3
Flexible Manufacturing Systems (FMS)	1977-1984	$ 81.3
Undersea Oil Production System	1978-1984	$ 93.8
767 Wide-Body Jet	1978-1983	$ N/A
Large-Scale Energy Conservation (Moonlight)	1978-2000	$ 386.4
Optical Measurement & Control System	1979-1986	$ 112.5
Turbo-Fan Engine	1980-1988	N/A
Monocarbon (C1) Chemical Technology	1980-1987	$ 93.8
Manganese Nodule Mining System	1981-1989	$ 125.0
Scientific Supercomputing System	1981-1989	$ 143.7
Next-Generation Basic Technologies	1981-1990	$ 649.5
Automated Sewing System	1982-1989	$ 81.3
Speech Synthesis	1983-1988	N/A
Advanced Robotics (JUPITER)	1983-1990	$ 125.0
Resource Exploration Observation System	1985-1990	$ 143.7

(Continued)

Table 1 (Continued)

MITI'S JOINT R&D PROJECTS
1966-2000

Project	Duration	Budget (M)
Large-Scale Projects (Continued)		
Water Recycling (Aqua Renaissance 90)	1985-1991	$ 81.3
Interoperable Databases	1985-1992	$ 125.0
Bioelectronics/Biocomputer	1985-1990	$ 40.0
Optical Reactive Materials	1985-1995	N/A
Next-Generation IC Equipment	1985-1993	N/A
MITI/MPT Joint Projects		
Synchrotron Optical Radiation (SOR)	1986-96	$ 93.6
Optoelectronic ICs & Optocomputers	1986-96	$ 62.5

Notes: Exchange Rate of ¥160 = $1
N/A = Not Available

Source: MITI
Dataquest
June 1986

BUDGET SUMMARY AND SCHEDULE FOR MITI PROJECTS

In fiscal 1986, MITI plans to increase its funding of joint high-technology R&D projects by 5.5 percent, as shown in Table 2. It appears that MITI is accelerating its research on fifth generation computers and computer-aided instruction (CAI), but reducing its supercomputer funding.

Government R&D Projects

Table 2

MITI FISCAL 1985/1986 FUNDING OF HIGH-TECHNOLOGY PROJECTS

Project	FY1985 (M)	FY1986 (M)	
Fifth Generation Computer	¥ 4,779	¥ 5,491	$34.3
Interoperable Data Base System	20	831	5.2
Supercomputer	3,016	2,889	18.1
Future Electron Devices	1,585	1,542	9.6
- Bioelectronic Devices	0	60	0.4
Medical Support System	110	103	0.6
Data Processing Promotion	2,348	1,260	7.9
- Education CAI Software Survey	0	210	1.3
Data Base/Information Provision	12	76	0.5
New Media Community Concept	74	60	0.4
Regional Information "Vision"	0	5	0.1
ASEAN Information "Vision"	0	31	0.2
Int'l Information Cooperation Center	212	239	49.4
Automated Translation System	0	50	0.3
Data Processing Equipment & Systems	13	12	0.1
Information Technology Standards	48	46	0.3
Computer Security	12	11	0.1
Semiconductor Conditions Survey	0	6	0.1
Total	¥12,229	¥12,907	$80.7

Source: Ministry of International Trade and Industry
Dataquest
June 1986

KEY SEMICONDUCTOR R&D PROJECTS

As shown in Table 3, Japanese ministries and universities are pursuing 25 joint R&D projects that will directly affect the semiconductor industry. Dataquest believes that it is imperative for U.S. and European companies to monitor these programs carefully.

Government R&D Projects

Table 3

JAPANESE GOVERNMENT SEMICONDUCTOR-RELATED JOINT R&D PROJECTS

Duration	Project	Budget ($M)
1979-1986	MITI Optical Measurement & Control System	$112.5
1979-1991	MITI Fifth Generation Computer	$375.0
1981-1986	STA Perfect GaAs Crystals	$ 11.0
1981-1986	STA Amorphous Compounds	$ 11.0
1981-1986	STA Nanomechanism	N/A
1981-1990	MITI Supercomputer	$143.7
1981-1990	MITI Future Electron Devices	$114.0
1981-1990	MITI Fine Ceramics	$ 50.0
1982-1987	STA Bioholonics Systems	$ 10.0
1983-1988	STA Bioinformation Transfer	$ 10.0
1983-1988	MITI Speech Synthesis and Recognition	N/A
1983-1990	MITI Advanced Robotics (JUPITER)	$125.0
1984-1990	NIT Information Network System Computer	$730.0
1985-1990	STA Solid State Surfaces	N/A
1985-1991	MITI SIGMA Automated Software Development	$156.3
1985-1990	MITI Biochips/Biocomputer	$ 40.0
1985-1993	MITI Next-Generation IC Equipment	N/A
1985-1988	Tokyo U. TRON Project (32-bit MPU)	N/A
1985-	Kyoto U. Supercomputer/Matsushita	$ 23.5
1986-1996	MITI Synchrotron Orbital Radiation (SOR)	$ 93.6
1986-1996	MITI Optoelectronic ICs/Optocomputer	$ 62.5
1986-1996	MITI/MPT Automated Translation Phone	$625.0
1986-1988	Japan Robot Association Robot Sensors	N/A
1986-	Tohoku U. Automotive Electronics/Ceramics	N/A
1987-	MITI New Diamond Substrates	N/A

Source: Dataquest
June 1986

Notes:
N/A = Not Available
MITI = Ministry of International Trade and Industry
MPT = Ministry of Posts and Telecommunications
STA = Science and Technology Agency
NTT = Nippon Telegraph and Telephone Corporation (formerly a public corporation; privatized in April 1985)

Optoelectronics Project

OPTOELECTRONICS PROJECT (1979-1996)

A major goal of MITI (Ministry of International Trade and Industry) is to develop an optocomputer and optical control system that will use light, rather than electricity, to transfer information. To achieve this goal, the Optical Measurement and Control Systems Project was formed in 1979 to develop optical elements for factory image sensors and data transmission.

The project is sponsored by MITI's National R&D Programs and involves fourteen companies organized into the Engineering Research Association of Optoelectronics Applied Systems. Participating companies include Fujitsu, Furukawa, Hitachi, Matsushita, Mitsubishi, NEC, Oki, Sumitomo Electric, Toshiba, and five smaller companies. In October 1981, the association established the Optoelectronics Joint Research Laboratory within the Fujitsu Laboratory at Atsugi, which works closely with NTT's Atsugi optoelectronic researchers across the street. MITI researchers are assigned to the laboratory, which is under contract to conduct basic research. The project was initially budgeted at ¥18 billion ($112.5 million) and all expenses are covered by MITI consignment payments (itakuhi), which the companies do not have to repay. Patents developed from the project are government property and available to participating companies from MITI's Industrial Technology Promotion Agency.

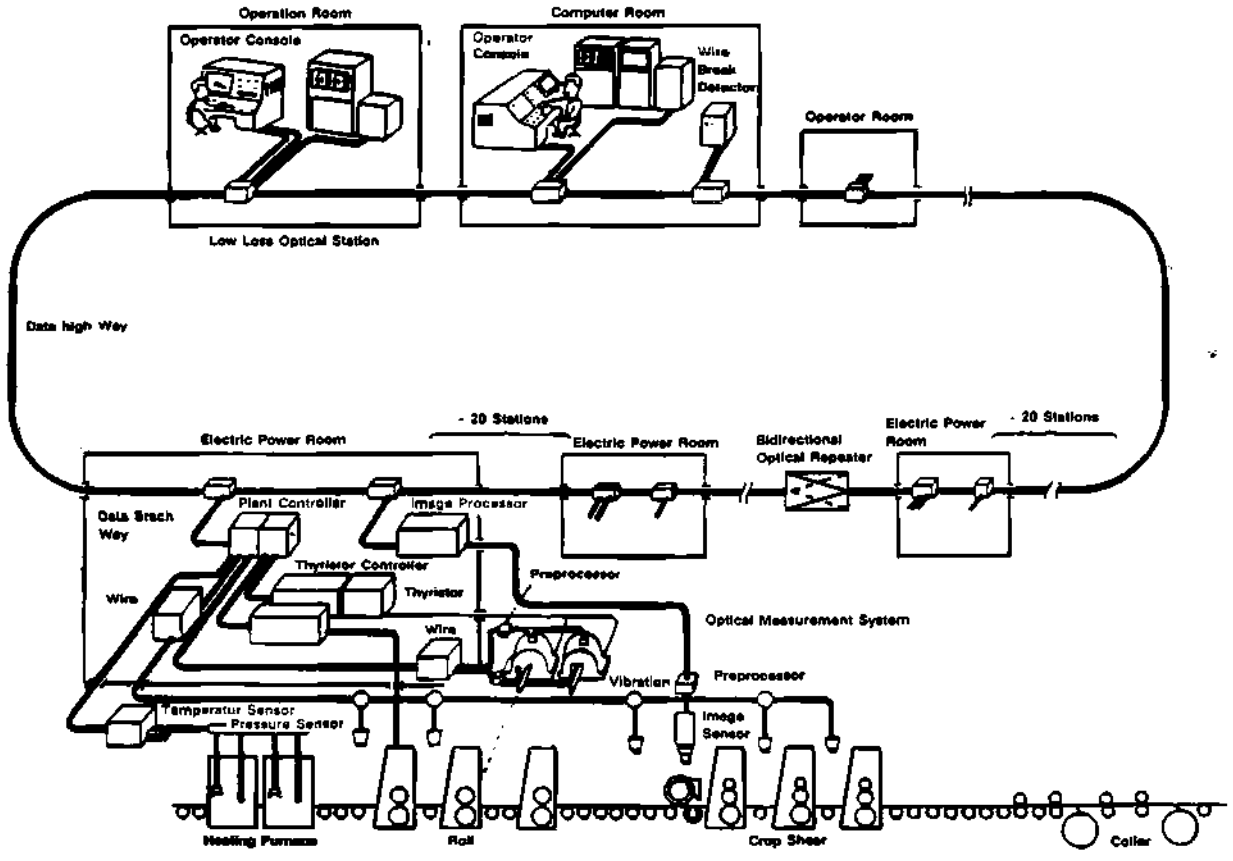
The Optoelectronics Project was divided into two phases: factory optical sensors (1979 to 1986) and optical communication (1986 to 1988). MITI originally planned for only the first phase, but extended the project due to growing interest in NTT's optical fiber-based Information Network System.

During the first phase, experiments on a totally optical system were conducted at a chemical plant in Mizushima (Okayama Prefecture). A model system is shown in Figure 1. Research focused on the following topics:

- High-speed image information system capable of direct measurement, transmission, and multiple monitoring of images too rapid for TV cameras
- Practical system for processing high-quality images of 1,000 x 1,000 pixels or more
- High-speed process information subsystem for collecting and transmitting data from many sensors and actuators
- Compound process information subsystem for simultaneous collection and wavelength multiplexing transmission
- Information management subsystem with 1-Gbs transmission speed or higher

Figure 1

MITI'S MODEL OPTICAL MEASUREMENT AND CONTROL SYSTEM



Source: MITI
DATAQUEST
June 1986

Optoelectronics Project

In addition, work was conducted on optical devices, such as semiconductor lasers and optoelectronic ICs (OEICs), that will permit monitoring and control of industrial and commercial activities in the presence of inflammable gas, adverse weather, and electromagnetic induction. Research targets included:

- Visible light and high-output laser diodes
- Multichannel LSI optical switches
- Direct-image and infrared transmission path fibers
- Temperature, pressure, and flow optical sensors and activators

The first phase has been extremely successful. MITI gained more than 300 patents from work done on the project, which are available to anyone on a fee basis. Japanese semiconductor makers have developed semiconductor lasers, optocouplers, photodiodes, high-output LEDs, single-mode laser diodes, MOS and CMOS charge-coupled device (CCD) sensors, and first-generation optoelectronic ICs (OEICs). These devices are already being used in laser and compact disks (CDs), 8mm movie cameras, optical disk systems, optical communications, factory automation monitoring, remote control systems, car systems, TV animation, laser copiers and printers, point-of-sales terminals, and office LANs. By 1985, over 1,000 optoelectronic systems had been installed in Japan. The project also developed new GaAs epitaxial crystal growth methods for OEICs.

The second phase, focusing on optical communications, began this year. In May, 13 Japanese semiconductor makers announced the formation of the Optical Technology R&D Corporation to develop second- generation OEICs for optocomputers and optical communications. The participating companies include Fujikura, Fujitsu, Hitachi, Koga Electric, Japan Glass, Matsushita, Mitsubishi, NEC, Oki Electric, Sanyo, Sharp, Sumitomo Electric, and Toshiba. Initially capitalized at ¥143 million ($894,000), the R&D venture will receive 70 percent of its funding from the Japanese government and 30 percent from participating companies. The research will run 10 years and is budgeted at ¥10 billion ($62.5 million). About ¥100 million ($625,000) will be invested in a Basic Technology Research Promotion Center. The R&D venture will initially focus on OEICs capable of handling 1-gigabit-per-second (Gbps) optical transmission, with the ultimate goal of developing OEICs capable of 10-Gbps speeds.

MITI is developing manufacturing technology to evaluate GaAs crystals that will be used to produce OEICs. The goal is to develop defect-free GaAs crystals using epitaxial thin-film technology. MITI is lending

Optoelectronics Project

equipment worth ¥3.5 billion ($20.6 million) at no cost to companies that are currently receiving consignment funding (itakuhi), to supplement their ¥600 million ($3.5 million) in OEIC research spending. Project participants include Fujitsu, Koga Electric, Matsushita, the Max Planck Institute, MITI, Mitsubishi, NEC, Oki Electric, Sumitomo Metals, and Toshiba.

Supercomputer Project

NATIONAL SCIENTIFIC COMPUTING PROJECT

In July 1980, MITI (Ministry of International Trade and Industry) announced the National Scientific Computing Project to develop a high-speed computer for scientific and engineering uses. The project goal is to create by 1989 a supercomputer capable of performing 10 billion floating point operations per second (GFLOPS), which will permit complex data processing, such as simulating weather patterns, designing cars and aircraft, and analyzing satellite photos.

In December 1981, six of Japan's top computer makers--Fujitsu, Hitachi, Mitsubishi Electric, NEC, Oki Electric, and Toshiba--organized themselves as the Association for the Development of High-Speed Scientific Computers to work with MITI on the Supercomputer Project, which formally got under way in January 1982. The project is headquartered in MITI's Electrotechnical Laboratory in Tsukuba Science City, but participating companies run parallel efforts in their own research labs.

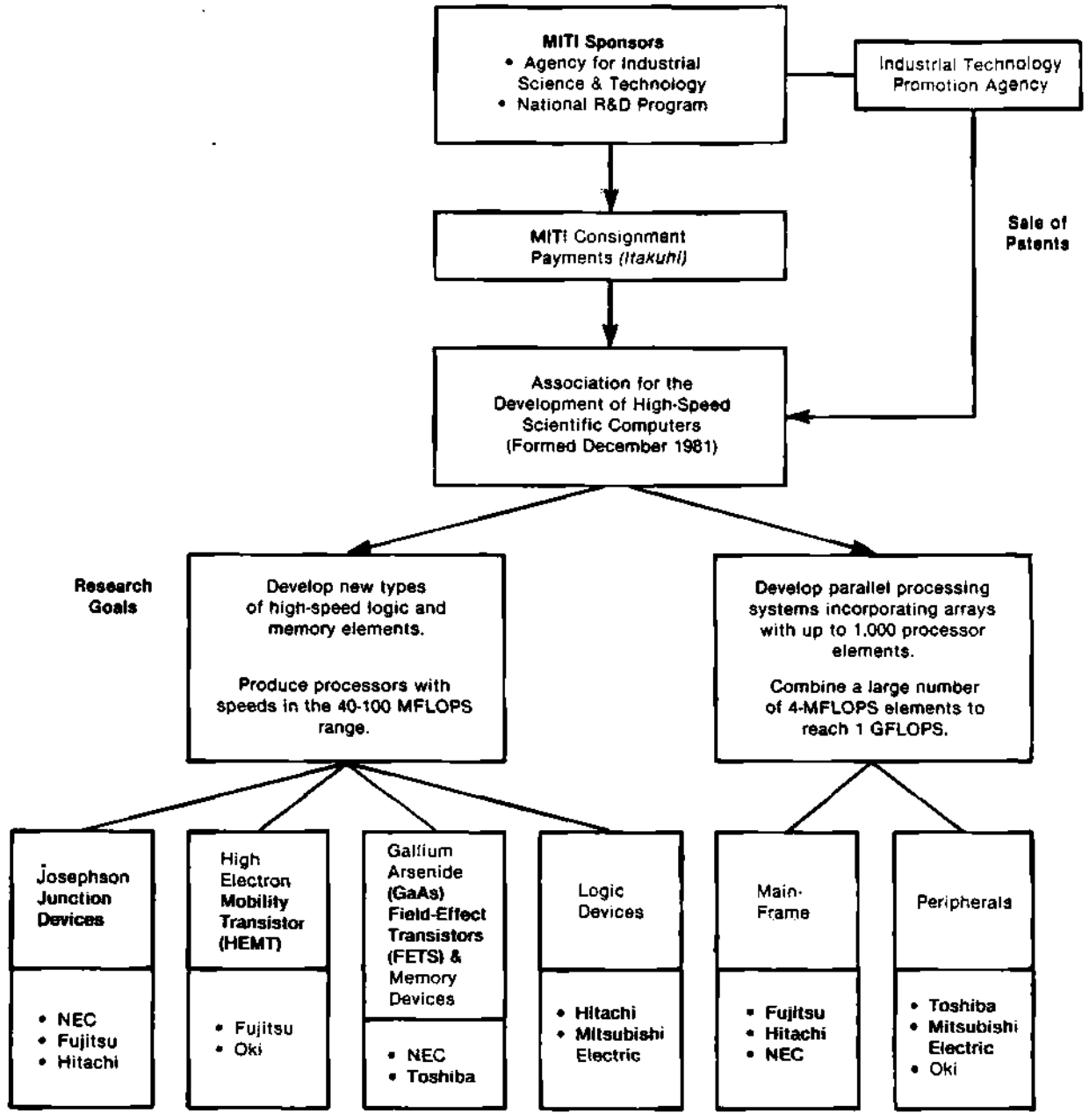
The project, which is scheduled to run from 1981 to 1989, is focusing on six research areas: gallium arsenide field-effect transistors (GaAs FETs) and memory devices, high electron mobility transistors (HEMTs), Josephson junction devices, emitter-coupled logic (ECL) devices, parallel processing mainframe systems, and peripherals. In fiscal 1984, participating companies were given the following assignments: system architecture (Fujitsu), large-capacity high-speed storage (NEC), parallel processor for distributed processing (Mitsubishi, Oki, and Toshiba), software (Hitachi), Josephson junctions (Fujitsu, Hitachi, and NEC), HEMTs (Fujitsu, Oki), and GaAs digital ICs (Mitsubishi, NEC, and Toshiba). Figure 1 shows the project assignments of the participating companies.

The Supercomputer Project has been extremely successful to date. As shown in Table 1, Fujitsu has made significant progress in HEMT and GaAs SRAM technologies for its supercomputer. NEC has also developed a prototype 4K GaAs SRAM (2.4ns), which places it slightly behind Fujitsu (1.7ns) and Hitachi (2.2ns). Nevertheless, NEC has strong architecture capabilities in its latest machine. Matsushita, Oki Electric, and Toshiba have announced GaAs prototypes, which they will probably sell, since they lack supercomputer capabilities. Some work is being done on ballistic transistors, but the research is still in its infancy. Japanese supercomputers will be mostly based on GaAs and HEMT, with Josephson junctions limited to high-end machines for scientific purposes. DATAQUEST believes that these devices are being designed into Japanese machines, initially for in-house use.

Supercomputer Project

Figure 1

THE SUPERCOMPUTER PROJECT (1981-1889)



Source: DATAQUEST
June 1986

Supercomputer Project

Table 1

SEMICONDUCTOR TECHNOLOGY FOR SUPERCOMPUTERS

Date	Company	Announcement
		Gallium Arsenide Digital IC
Q1/84	Fujitsu	4K SRAM with 3ns speed; practical use by 1986
Q1/84	Matsushita	Test manufacturing of direct-coupled FET logic
Q1/84	Oki Electric	8 x 8-bit parallel multiplier
Q1/84	Toshiba	1,000-gate array prescaler for mobile radios
Q1/84	NTT	4K SRAM using self-aligned technology
Q2/84	Matsushita	Heterojunction direct-coupled FET logic (DCFL)
Q2/84	Tokyo U.	High-purity GaAs/GaAlAs FET
Q4/84	NEC	Ultrahigh-speed 12x12-bit parallel multiplier
Q4/84	NEC	4K SRAM for supercomputer cache memory, 2.4ns
Q4/84	Oki Electric	1,000-gate array using superbuffered FET logic
Q1/85	NEC	12 x 12-bit extended parallel multiplier, 4ns
Q1/85	Oki Electric	390ps 1,000-gate array using DCFL FET logic
Q1/85	Toshiba	42ps 2,000-gate array
Q1/85	Oki Electric	14.7ps metal FET (MESFET)
Q1/85	NEC	4K SRAM using source-coupled FET logic
Q2/85	Hitacni	4K SRAM with 2.2ns speed; 16K SRAM by 1986
Q3/85	Fujitsu	4K SRAM with 1.7ns speed
Q3/85	IIT	Silicon-insulator-silicon 3-layer FET
Q3/85	NEC	30ps 3,000-gate logic; 16K SRAM prototype
Q3/85	NEC	5ps GaInAs transistor with 5-atom AlAlAs on GaInAs
		High-Electron-Mobility Transistor (HEMT)
Q1/84	Fujitsu	Test manufacturing of 256-bit HEMT memory
Q1/84	Fujitsu	0.9ns 1K SRAM at minus 196 degrees C
Q3/85	Oki Electric	1,000-element AlGaAs/GaAs "reverse" HEMT
Q3/85	Fujitsu	1ps tunneling hot electron transistor ("chirp" RHET)
		Josephson Junction
Q4/84	Hitachi	20ps superconductive transistor for control terminals
Q4/84	NEC	350ps 4 x 4-bit parallel multiplier with 249 logic gates
Q1/85	NEC	280ps 4 x 4-bit multiplier using dual-rail logic

Source: DATAQUEST
June 1986

Supercomputer Project

The Supercomputer Project has also assisted Japanese computer makers in developing new supercomputers that are competitive with American machines. In fact, NEC recently sold its $20 million SX-2 supercomputer, which has a maximum operating speed of 1.3 GFLOPS, to the Houston Area Research Center, beating Cray Research and IBM in its first encounter in the United States. However, Japanese makers lack the software support available with Cray and Digital Equipment Corporation machines. NEC's supercomputer runs on its own software, unlike those from Fujitsu and Hitachi, which offer IBM compatibility. Another obstacle is that supercomputers run more efficiently using vector processing (manipulation of data arrays) rather than scalar processing (single-element variables). To achieve peak performance speeds, Japanese computer makers must develop compilers to vectorize their programs. Table 2 compares Japanese supercomputers with Cray Research, the U.S. leader.

Table 2

CRAY AND JAPANESE COMMERCIAL SUPERCOMPUTERS

Company	Model	Speed (MFLOPS) Actual	Speed (MFLOPS) Announced	Maximum Memory	Year
Cray (U.S.)	Cray 1	80	160	8	1976
	Cray 1-S	80	160	32	1979
	Cray 1-M	80	250	32	1983
	X-MP-2	400	630	32	1983
	X-MP-48	N/A	1,000	N/A	1985
	Cray 2	N/A	2,000	256	1986
	Cray 3	N/A	1,000	N/A	1986
Fujitsu	VP50	140	N/A	128	1985
	VP100	250	267	128	1983
	VP200	500	553	256	1983
	VP400	1,140	1,000	256	1985
Hitachi	S-810/5	160	N/A	128	1986
	S-810/10	315	400	128	1983
	S-810/20	630	800	256	1983
NEC	SX-1	570	570	128	1983
	SX-1E	285	N/A	N/A	1986
	SX-2	1,300	1,300	256	1985

Note: N/A = Not Available

Source: DATAQUEST
June 1986

Supercomputer Project

MITI's Supercomputer Project has greatly accelerated the pace of Japanese supercomputer development. DATAQUEST observed increased activity in GaAs digital ICs and supercomputers in 1985, as shown in Table 3. We believe that Japanese companies are pursuing the following research in 1986:

- Design of 16K GaAs SRAMs and 32-bit MPU parallel processing architectures into supercomputers by Fujitsu, Hitachi, Matsushita, and NEC
- Announcement of supercomputers over 2 GFLOPS that offer parallel or vector processing from Fujitsu, Hitachi, and Matsushita
- Introduction of entry-level supercomputers (less than 160 MFLOPS) by NEC, Sharp, Sanyo, and other newcomers
- Development of minisupercomputers (less than 100 MFLOPS), possibly with U.S. minisupercomputer start-up companies, for use as VLSI CAD tools

Table 3

1985 JAPANESE SUPERCOMPUTER ACTIVITIES

Company	Announcement
Digital Computer Ltd.	Jointly developed a 60-MFLOP minisupercomputer with Convex Computer Corp. (see discussion in newsletter text)
Fujitsu	Amdahl sold Fujitsu-built 533-FMLOP vector processing supercomputer (Model 1200) to Western Geophysical Company of America; Amdahl offers four Fujitsu supercomputers ranging from 133 MFLOPS to 1.14 GFLOPS under own label (Fujitsu's VP50/100/200/400); Fujitsu has sold 29 VP400 supercomputers (1.14 GFLOPS); prototype 1ps resonance-tunneling hot electron transistor and 1.7ns 4K GaAs SRAM; working on 16K GaAs SRAM
Hitachi	Announced 160 MFLOP entry-level supercomputer (S-810 Model 5) in September 1985; 2.2ns 4K GaAs SRAM prototype; working on 16K GaAs SRAM
MITI	Prototype GaAs complementary FET (SIS-FET), opening the way for future 4Mbyte GaAs DRAMs (see Memory section of the newsletter)

(Continued)

Table 3 (Continued)

1985 JAPANESE SUPERCOMPUTER ACTIVITIES

Company	Announcement
NEC	Sales of 1.3-GFLOP SX-2 supercomputer to Houston Area Research Corporation in January 1986 (fifth SX-2 sold); SX-2 test demonstration before Tokyo press at Fuchu plant in December; new 285-MFLOP SX-1E supercomputer; 2.4ns 4K GaAs SRAM and 30ps 3,000-gate GaAs array prototypes; working on 16K GaAs SRAM; prototype 4 x 4-bit Josephson junction parallel multiplier (280ps and 350ps)
Nissan	Purchased Cray XMP-2 supercomputer for $6 million and motors supporting software for $6 million
NTT	Purchased second Cray supercomputer (XMP-1); first Cray was XMP-2 in August 1984

Source: DATAQUEST
June 1986

Recently, Kyoto University and Matsushita Electric formed their own joint supercomputer R&D project to develop a 2- to 3-GFLOP supercomputer utilizing 300 32-bit microprocessors. Moreover, DATAQUEST observes increased activity to develop minisupercomputers (Personal Crays) with 50- to 60-MFLOPS capabilities for use as engineering CAD workstations. MITI's Supercomputer Project is currently investigating ways to miniaturize current mainframes in order to compete with U.S. minisupercomputer start-ups.

NEC recently sold its $20 million SX-2 supercomputer, which runs at a maximum operating speed of 1.3 GFLOPS, to the Houston Area Research Center (HARC). HARC is a nonprofit research corporation consisting of industry and universities, including Rice University, Texas A&M, the University of Houston-University Park, and the University of Texas. Acording to HARC, the SX-2 offered better price/performance than machines offered by Cray Research and IBM. In December, before a skeptical Tokyo press club at the Fuchu plant, NEC demonstrated that its SX-2 supercomputer can operate at 1.3 GFLOPS, the world's fastest speed. Since then, Cray Research has announced a 1.75-GFLOPS supercomputer.

Supercomputer Project

Hitachi has started marketing its S-810 Model 5 supercomputer, which is capable of performing at up to 160 MFLOPS for complex scientific and technical calculations. It has a main memory capacity of 32 Mbytes. The machine will be leased at ¥40 million ($160,000) per month; sales prices are not yet available. The new computer can be upgraded at the user's site by adding vector processing cards and reinforcing the forced-air cooling system. Hitachi expects to install 80 machines in the next five years.

Digital Computer Ltd. (DCL), a Tokyo systems house, recently developed a small scientific supercomputer with Convex Computer Corporation of Richardson, Texas, for use as a host computer for local area network (LAN) systems. The computer (VP-1) has a processing speed of 60 MFLOPS, which is 25 times faster than Digital's VAX 780, and will cost 50 percent more. DCL will package the supercomputer into a LAN system incorporating DCL workstations. The supercomputer will handle scientific computations, and the workstations will perform interactive processing. The VP-1 supercomputer will cost ¥190 million ($950,000); a LAN system including the VP-1 and 10 workstations will cost ¥240 million ($1.2 million).

Fifth-Generation Project

FIFTH-GENERATION COMPUTER

In April 1982, MITI (Ministry of International Trade and Industry) established the Institute for New Generation Computer Technology (ICOT) to run its Fifth-Generation Computer Project. Headed by Dr. Kazuhiro Fuchi, ICOT's goal is to develop a non-von Neumann computer capable of handling symbols, images, graphics, speech, and other types of nonalphanumeric data. As shown in Figure 1, the fifth-generation computer will offer three unique features:

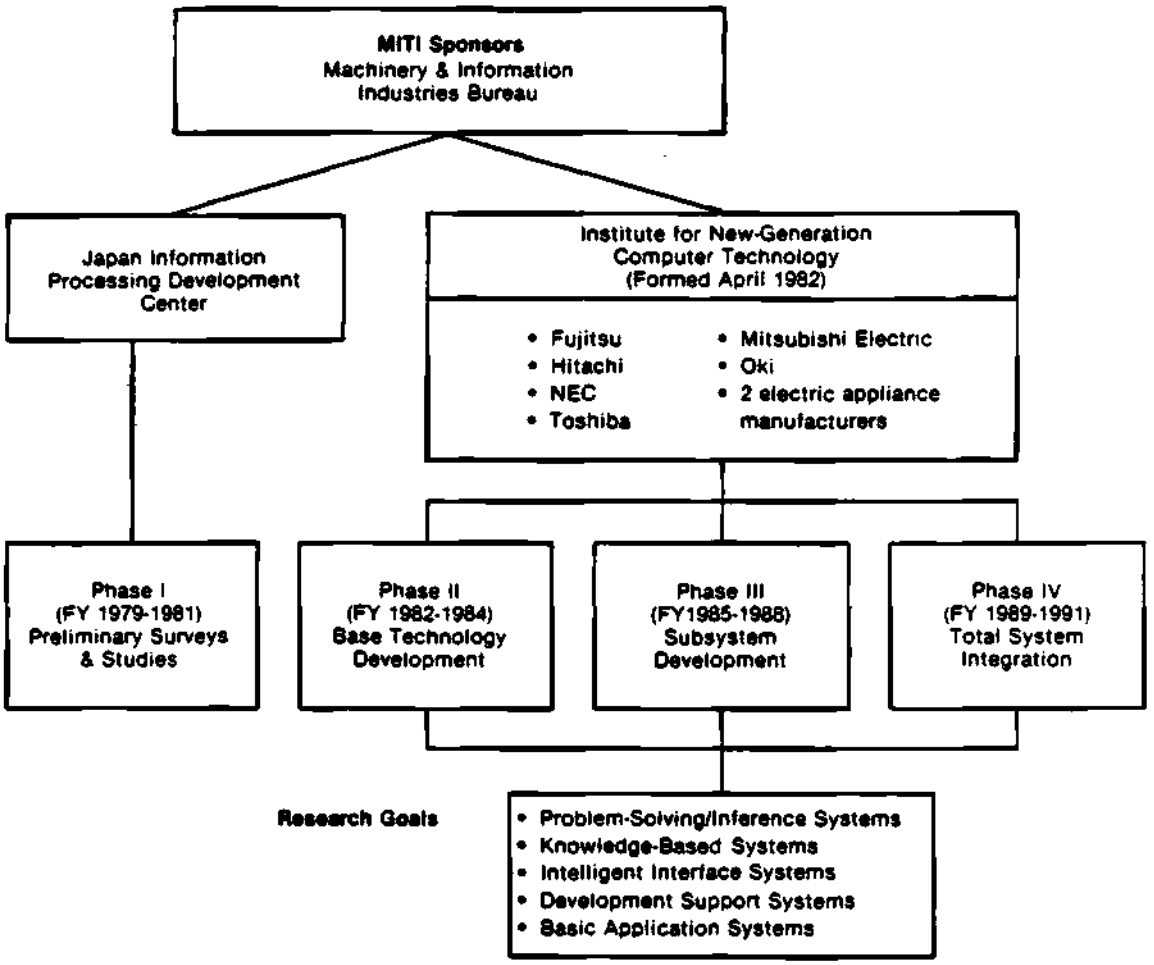
- A vast knowledge base consisting of libraries of images, graphics, voice messages, and other symbolic data represented in the form of "objects," of clusters of attributes, that will be related to other bits of data by links or symbolic references
- A problem-solving and inference system utilizing PROLOG (PROgramming in LOGic) machine language capable of performing one million logic inferences per second (LIPS)
- User-friendly terminals capable of inputting voice, graphic, image, or handwritten data through the use of question-and-answer systems, optical scanners, touch screens, mouse devices, video cameras, phonetic typewriters, and other nontyping means

In addition, ICOT is working on three basic applications for the fifth-generation computer. Japanese-to-English translation software is a major goal because of the linguistic barriers between Japan and the rest of the world. ICOT's aim is to develop a prototype multilingual translation system with a 100,000-word vocabulary and the ability to translate, edit, and print with 90 percent accuracy. A second application will be a consulting system, or small interactive reference library, with information gathering and capacities 100 times greater than existing systems for specialized fields such as medical diagnosis, CAD, and equipment repair. Finally, ICOT plans to introduce nearly automatic software creation with little need for computer literacy on the part of the user. Automatic software generation was originally part of the Fourth-Generation Computer Project (1979-1983), but MITI encountered difficulties with it and transferred it to this project. Other intelligent programming systems will be developed to make software programming faster and easier, including modular programming systems, module management systems, and algorithm banks for problem-solving procedures.

Fifth-Generation Project

Figure 1

THE FIFTH-GENERATION COMPUTER PROJECT (1979-1991)



Source: DATAQUEST
July 1986

Fifth-Generation Project

The fifth-generation computer is being developed in three phases:

- Phase I (fiscal 1982-1984)--ICOT training on PROLOG programming, a single-user sequential PROLOG workstation, and software for expert system applications developed
- Phase II (fiscal 1985-1989)--parallel processing and knowledge-based subsystems to be merged, while work continues on the PROLOG-based inference subsystems
- Phase III (fiscal 1989-1992)--all three subsystems to be merged into a single fifth-generation computer

As shown in Table 1, each company has been given specific task assignments.

Table 1

TASK ASSIGNMENTS OF THE FIFTH-GENERATION PROJECT

Company	Development Responsibility
Hitachi	Hierarchical memory subsystems
Mitsubishi	Terminals (bit-mapped display and mouse)
NEC	Sequential inference machine
NEC/Hitachi/ Fujitsu	Parallel inference and knowledge-based machines
Oki Mitsubishi	Pilot model personal sequential inference computer
Tokyo U.	Parallel inference engine for PROLOG machine
Toshiba	General-purpose parallel computer for knowledge bases and relational data bases; local area network (LAN)

Source: MITI
DATAQUEST
July 1986

Fifth-Generation Project

The Fifth-Generation Computer Project has successfully achieved its Phase I goals, which were relatively modest in scope. In November 1985, ICOT held an international conference that attracted over 1,000 researchers. Kazukiyo Kawanobe of ICOT reported that ICOT had spent ¥8.2 billion ($51.3 million) since 1982 in Phase 1 to develop the following:

- Personal sequential inference (PSI) machine
- Knowledge-based system (parallel relational data base machine and specifications for inference machine interface)
- Basic software system, including:
  - Parallel-type logic programming language
  - Basic specifications for a knowledge programming language
  - Large-scale relational data base management program
  - Japanese proofreader system
  - Advanced syntactic analysis program
  - Experimental semantic analysis program
  - Modular programming system
- Pilot software development tools (sequential logic programming languages and sequential inference machine software)

In fiscal 1985, ICOT began Phase II, a four-year program to develop prototype knowledge-based and inference subsystems.

Computerized natural language translation is another goal of the Fifth-Generation Computer Project. In 1982, MITI began developing machine translation systems to translate Japanese and English scientific and technical papers. Other participating groups include the Electronic Technology Composite Research Institute, the Industrial Technology Institute's Tsukuba Computing Center, the Japan Scientific and Technical Information Center, Kyoto University, and the Scientific and Technical Commission. By 1985, the group developed a Japanese/English system glossary of 10,000 words, 900 grammar analysis rules, and 1,000 conversion/generation rules.

DATAQUEST observes that Japanese companies are already using voice translators with simultaneous readouts for automated teller machines (ATMs) at banks, fish market and stock market bidding, and conferences. In addition, prototype word processing translators with split screens were demonstrated in late 1985.

Fifth-Generation Project

In 1986, ICOT plans to establish an Artificial Intelligence Center to develop practical AI systems. The center will focus on production equipment, printing, CAD/CAM, factory automation, and natural language processing. Members include Hitachi Seiki, Iwanami Publishing, Mitsubishi, NEC, Obunsha, Sanshodo, Sony-Tektronix, Toshiba, and Toyoda Machinery.

DATAQUEST notes that Japanese companies are already applying expert system and AI technology acquired from MITI's Fifth-Generation Computer Project to commercial products. In 1986, several companies announced the applications shown in Table 2.

Table 2

COMMERCIAL APPLICATIONS OF EXPERT SYSTEMS IN JAPAN

Company	Application
Hitachi/Nishi-Nippon Bank	A joint project to develop a high-speed, compact inference machine called Eureka for commercial loan operations
Mitsubishi	50 PSI sequential inference machines delivered to ICOT for evaluation; developing expert system development tool for PSI computers
NEC	An Automated Computer Program Generator that automates software development; a mini-computer system, utilizing LISP and PROLOG for internal processing and C language for man-machine interface, that transforms information in Japanese language and graphics into COBOL
System Development Center	A medical treatment expert system (MEDI-NET) utilizing a FACOM-M150F mainframe, PROLOG-based FACOM-Alpha computer, and a nationwide telecommunications network

Source: DATAQUEST
July 1986

Fifth-Generation Project

Recently, DATAQUEST has observed several developments in fifth-generation computers.

In November 1985, MITI announced that it had developed an experimental non-Von Neumann computer with an operating speed of 3 million floating point operations per second (megaflops), which will form the basic unit for a large supercomputer. According to MITI's Electrotechnical Laboratory, this basic unit will permit development of supercomputers with 50 times the operational speed of existing models.

MITI and the French Ministry of Industrial Reorganization agreed in October 1985 to establish a joint artificial intelligence (AI) R&D program in 1986. The Institute for New General Computer Technology (ICOT) and France's National Information Processing and Automation Institute (INRIA) will exchange researchers and research data.

One of the major criticisms of MITI's Fifth-Generation Project is that small, innovative companies have not been invited to participate. Systran Corporation, a Tokyo software house, is a classic example. In December 1985, Systran won a ¥2 billion ($10 million) order from the U.S. government for its Systran system, which is capable of translating 1.5 million words (6,000 text pages) of Japanese into English in one hour, with 85 percent accuracy. This system approaches MITI's automatic translation goal for 1990. The U.S. government plans to install the system at the Departments of Commerce and Defense and at NASA. Other companies with Japanese-to-English translation machines include Bravis International, Fujitsu, Hitachi, and NEC.

The European Economic Community (EEC) also plans to utilize Japanese-to-English translation machines to collect and monitor Japanese technology trends. EEC representatives visited Bravis International, Fujitsu, Hitachi, and Systran, and will decide on a system by fall. Within three years, the EEC plans to incorporate translation software into its own large-scale computers to translate 50,000 to 70,000 theses from public research laboratories and universities.

Next-Generation Industries Program

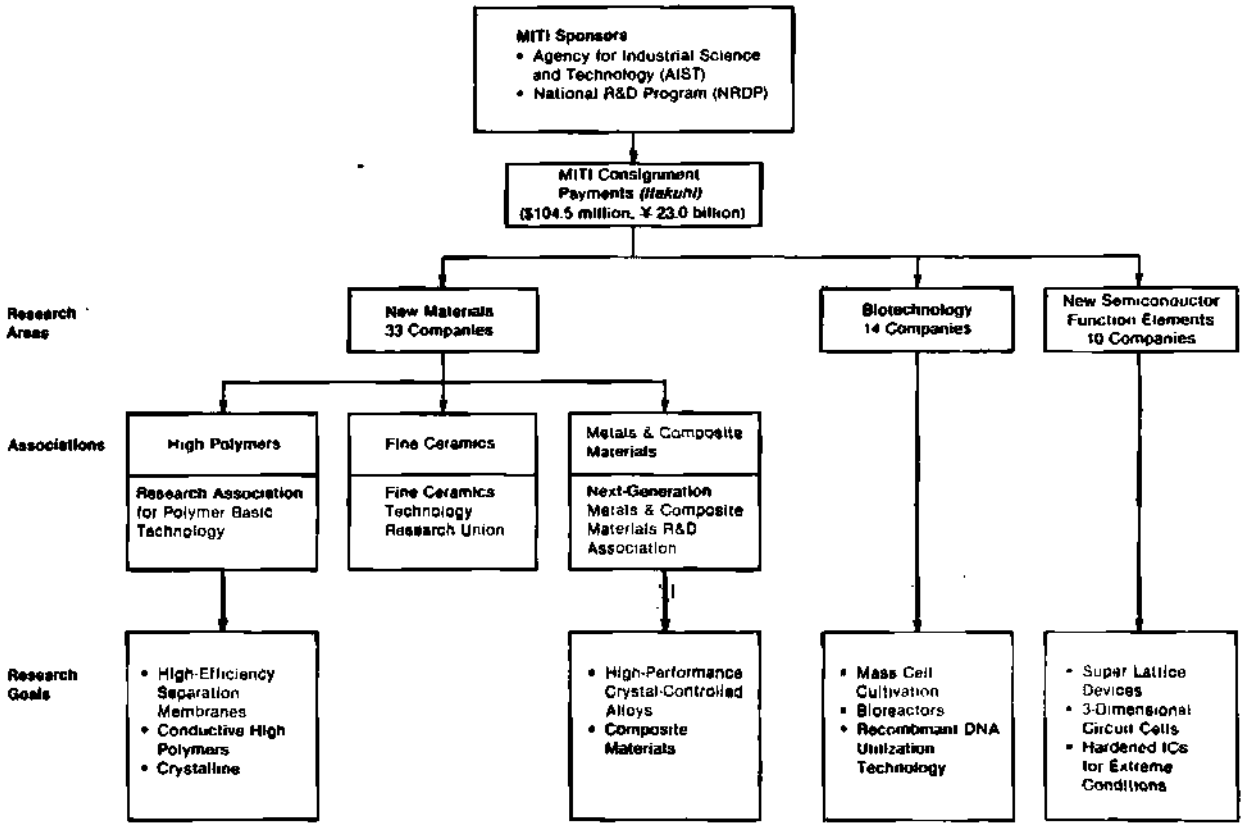
In October 1981, the Long-Term Industrial Technology Planning Committee, a study group of academicians and experts commissioned by MITI (Ministry of International Trade and Industry), issued a report recommending basic research for establishing new industries that are expected to flourish during the 1990s. These industries include biotechnology, aerospace, information processing, alternative energies, and ocean development. Three general fields were chosen by MITI for accelerated development: new materials (high polymers, fine ceramics, and composite materials), biotechnology, and future electron devices (3-dimensional ICs, superlattices, and hardened ICs).

Sponsored by the National R&D Program, the project will run from 1981 to 1990 and consists of 12 research areas. As shown in Figure 1, the 48 participating companies are assigned to five research associations, which are commissioned to conduct basic research. Project expenses are covered by MITI consignment payments (itakuhi), and patents will be made available for licensing from MITI's Industrial Technology Promotion Agency. MITI funding for the project, which averages $40 million annually, is shown in Table 1.

Next-Generation Industries Program

Figure 1

NEXT-GENERATION INDUSTRIES (1981-1990)



Source: MITI
DATAQUEST
June 1986

Next-Generation Industries Program

Table 1

NEXT-GENERATION INDUSTRIES PROJECT FUNDING
(Millions of Dollars)

	FY84	FY85	FY86
New Electron Devices	$ 9.2	$ 9.8	$ 9.7
Superlattice Devices	2.7	2.8	3.3
Three-Dimensional ICs	4.6	5.0	6.0
Hardened ICs	1.9	2.0	0.0
Biochips/Biocomputing*	0.0	0.0	0.4
New Materials	$20.4	$22.4	$22.4
High-Performance Ceramics	5.4	6.0	6.1
Synthetic Membranes	3.3	3.5	3.4
Synthetic Metals	2.1	2.3	2.3
High-Performance Plastics	1.9	1.9	1.8
Advanced Crystalline Alloys	3.6	3.8	3.7
Advanced Composite Materials	4.1	4.5	4.4
Photoreactive Materials*	0.0	0.4	0.7
Biotechnology	$ 7.5	$ 7.9	$ 7.7
Bioreactors	2.8	2.8	2.7
Large-Scale Cultivation	2.4	2.7	2.7
Recombinant DNA	2.3	2.4	2.3
Total	$37.1	$40.1	$39.8

*Initiated in fiscal 1985

Source: MITI
DATAQUEST
June 1986

Future Electron Devices Project

Probably the most important semiconductor project is MITI's Future Electron Devices Project, an eight-year project that focuses on three-dimensional (3-D) ICs, superlattice devices (new crystal structures), and temperature- and radiation-hardened ICs. Silicon-based 3-D ICs were chosen because of their potential for developing megabit DRAMs and other high-density circuits using existing design rules. Superlattice research, which focuses on creating new silicon and III-V compound structures, is aimed at developing semiconductor lasers, GaAs logic, and other ultrafast ICs. According to MITI officials, the project is emphasizing 3-D ICs and superlattices because they believe that Japan has the lead in these fields.

By the end of fiscal 1984, the project had generated 373 technical papers and 282 patents, as shown in Table 1. Because of Japan's lead in 3-D IC technology, MITI and the companies have assigned more than half of their researchers to this field.

The project is organized as shown in Figure 1. A committee of university professors is advising MITI's Agency for Industrial Science and Technology (AIST) on basic research. There are approximatey 300 corporate researchers assigned to the project, divided equally among the three areas. Fourteen companies are organized into the Future Electron Devices R&D Association, which was commissioned by MITI to conduct basic research. The project is budgeted at about $114 million.

Major results of the project to date include:

- MBE for AlGaAs/GaAs--Fujitsu has increased crystal perfection, and decreased alloy clusters (117,000 square cm/v sec at 77 degrees Kelvin).
- MBE for InGaAs/GaSb--Sumitomo has achieved 7,200 square cm/v sec at room temperature.
- MBE for silicon--Hitachi has developed a formation of p-n doping superlattice structures and silicon-nickel electrodes.
- MOCVD for AlGaAs/GaAs--Sony has investigated heterostructure abruptness (32 to 46 angstroms) and developed an impurity high-doping technique that permits high-speed growth.

DATAQUEST believes that the New Functions Project is MITI's VLSI Project for the 1980s. The next major breakthroughs in semiconductor technology will come in the areas of 3-D ICs (e.g., Mitsubishi's 1Mb DRAM with 3-Dimensional stacked capacity cells and Hitachi's 4-bit, 16-level cell storage for the file memory) and III-V compound superlattice devices. We will update you on the latest developments after the project's annual symposium in July.

Future Electron Devices Project

Table 1

PATENTS AND TECHNICAL PAPERS FROM
MITI'S FUTURE ELECTRON DEVICES PROJECT

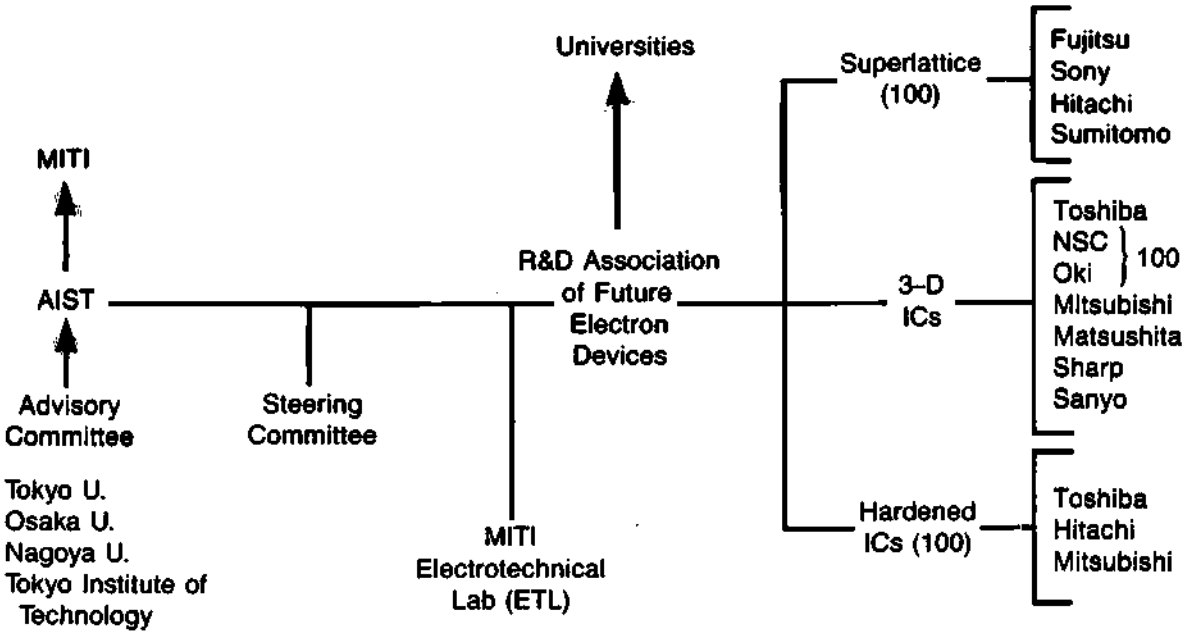
Fiscal Year	Superlattice Devices	3-D ICs	Hardened ICs	Total
		Technical Papers		
1981	1	6	0	7
1982	11	53	18	82
1983	31	86	30	147
1984	33	85	19	137
Total	76	230	67	373
		Patents Pending under Contract		
1981	1	6	1	8
1982	6	64	10	80
1983	16	75	12	103
1984	10	74	7	91
Total	33	219	30	282

Source: DATAQUEST
June 1986

Future Electron Devices Project

Figure 1

MITI'S NEW FUNCTIONS ELEMENT PROJECT



Source: DATAQUEST
MITI New Functions Element Project

As shown in Table 2, Japanese makers are experimenting with silicon-on-isolation (SOI) technology to create buffers between circuit layers and through-wall holes to provide paths for interconnection between layers. Laser recrystallization and laser activation of polysilicon are two popular methods being used to form layers and correct defects in the crystal structure.

Superlattice research is closely linked to III-V heterojunction research in MITI's Optoelectronics Project for semiconductor lasers. In both projects, multiple layers of III-V compounds (GaAs, AlGaAs, GaAlAs, InAsP, etc.) are laid down using molecular beam epitaxy to form superlattice structures. One research focus is GaAs on silicon to take advantage of the high-speed and laser properties of GaAs and the circuit density and low cost of silicon. DATAQUEST believes that MITI is working on GaAs/silicon 3-D ICs for eventually developing intelligent MPUs--microprocessors with built-in lasers for reading and transmitting data.

Future Electron Devices Project

Table 2

FUTURE ELECTRON DEVICE TECHNOLOGY

Date	Company	Technology
		3-D ICs
Q1/84	Fujitsu	2-layer, 3-D CMOS IC using silicon-on-insulator
Q4/84	NEC	Diamond thin-film over silicon
Q4/84	Toshiba	3-D IC production method using silicon substrate
Q1/85	Mitsubishi	3-layer, 3-D IC using laser recrystallization
Q2/85	Fujitsu	1Mb DRAM using 3-D stacked capacitor cells
Q2/85	Mitsubishi	3-D LSI using laser-activated polysilicon
Q2/85	Matsushita	2-layer, 3-D CMOS IC using laser irradiation
Q2/85	Sharp	5-layer poly, 3-D IC for video signal processing
Q3/85	Tokyo U.	3-D IC using amorphous oxidized silicon
Q3/85	Toshiba	3-D IC technology for 4Mb and 16Mb DRAMs
		Superlattices
Q2/84	NEC	10-layer superdoped GaAs/AlGaAs structure, 10ps
Q3/84	MITI	Computer-controlled superlattice crystal growth
Q2/85	MITI	2,200-layer GaAs crystal using molecular beam

Source: DATAQUEST
June 1986

New Materials Project

In 1981, MITI (Ministry of International Trade and Industry) established the Basic New Materials Office to pursue basic research in fine ceramics, new alloys, high-performance polymers, composites, and membranes. As shown in Table 1, there are seven MITI-sponsored projects and three private research projects subsidized by the government, which in several years may be added to the MITI New Materials Project. Total MITI funding is 20 to 30 percent of total project costs, once private sector funds are included.

In March 1985, MITI's Basic Materials Office created the Fundamental Technology Research Center, which will finance up to 70 percent of new materials research whenever two or more companies form a research partnership. For single firms, the Japan Development Bank (JDB) will offer loans repayable at 7 to 8 percent interest if the venture is successful. The new center costs about $50 million, with 50 percent coming from MITI, 25 percent from JDB, and 25 percent from private industry. Two new testing and evaluation centers were also established to develop commercial codes and standards for fine ceramics and new metals.

New Materials Project

Table 1

MITI's NEW MATERIALS PROJECT

Program	Budget (M) (1981-1985)
MITI-Sponsored	
Fine Ceramics	$22.2
Membrane Technology	$13.8
Conductive Polymers	$ 8.3
High-Performance Polymers	$ 7.8
Microcrystalline Alloys	$14.4
Composites	$16.4
Photoreactive Materials (since 1985)	$ 0.5
Subsidized Private Research	
Power Metallurgy Aluminum Alloys, Shape Memory Alloys, and High-Performance & Conductive Alloys	$ 2.0
Oxygen Enrichment Membrane Technology	$21.0
High-Temperature Ceramic Coastings & Corrosion-Resistant Metals	$21.0

Source: MITI
DATAQUEST
June 1986

Bioelectronics Project

BIOELECTRONICS PROJECT (6th Generation Computer)

In fiscal 1986 (beginning April 1986), MITI (Ministry of International Trade and Industry) launched a 10-year, joint R&D project with fourteen companies to develop bioelectronic devices for use in medical equipment, factory robots, and biocomputers. About ¥8 billion ($50 million) will be spent on the project, which will be coordinated with MITI's Biotechnology Project. The project will focus on several themes, including:

- New computer architecture modeled on the human brain
- Study of neural systems of lower animals to develop logic circuits and thin-film materials
- Development of biochips (organic materials for biosensors, logic, and memory circuits)
- Development of nondestructive, noncontact methods for measuring human brain activity

MITI is soliciting the participation of electronic, chemical, and biotechnology companies in the project. DATAQUEST expects participation from many companies involved in bioelectronics research, as shown in Table 1.

MITI is also funding a major bioelectronics joint venture formed in March 1986 by Kyowa Hakko, Mitsubishi Chemical, Takeda Chemical, Toa Nenryo, and Toray Industries to develop biosensors, biochips, bioreactors, biopharmaceuticals, and biofunctional membranes. Temporarily called the Protein Engineering Research Institute, the venture is capitalized at ¥300 million ($1.7 million). The Japan Key Technology Center, jointly owned by MITI and the Ministry of Posts and Telecommunications (MPT), will provide 70 percent of the funds, with the remaining 30 percent shared equally by the participating companies. The company plans to invest ¥30 billion ($176 million) over the next ten years in protein engineering. A ¥5 billion ($29 million) research center will be built in Senri (Osaka prefecture) by late 1987. In addition the venture plans include ten more companies. To date, Fujitsu, Kirin Brewery, Nihon DEC, and Showa Denko have applied for capital participation.

Bioelectronics Project

Table 1

BIOELECTRONICS RESEARCH ACTIVITIES

Company	Research Themes
Ajinomoto	Biochips, biosensors
Asahi Chemical	Organic semiconductors
Dojin Chemical	Langmuir-Bodgett thin films for biochips
Fuji Electric	Alcohol sensors, glucose sensors (Yokosuka)
Fujitsu	Biosensors, biological data processing
Hitachi	Biochips (Tokyo Central Lab)
Hitachi Works	Biosensors, Langmuir-Bodgett film (Kagoshima)
Japan Suisan	Sweetness sensors
Kao	Biochips
Kirin Brewery	Alcohol biosensors
Kuraray	Implantable biosensors for blood pH monitoring
Kyowa Hakko	Factory automation and medical biosensors
Kyowa Hakko & Takeda Chemical	A joint venture to develop biosensors and biochips with Mitsubishi Chemical, Toa Nenryo, and Tora
Matsushita Elec.	Biosensors, biochips (Kawasaki)
Matsushita Elec./ Hayashibara	Water-soluble photopolymers for VLSI chips
Mitsubishi	Nerve functions, biosensors
Mitsui Trading	Biochips
MITI/Tokyo U.	Biocomputer, bioholonics computer (Tsukuba)
NEC	Nerve functions, biosensors (Tsukuba)
Ricoh	Organic semiconductors
Sanyo	Biosensors, biochips (Tsukuba)
Sharp	Molecule recognition, vision data processing molecular devices, biochips, biocomputers
Sony	Biosensors
Suntory	Neurobiology, central nervous systems (Senri)
Tokyo Institute of Technology	Biosensor mass production technology (Professor Toyosaka Moriizumi)
Tokyo University	High-polymer membranes using organic monomers
Toray	Biosensors, biochips, molecular memories
Toshiba	Biosensors for measuring chemicals, biochips
Toyo Brewery	Biosensors for food quality analysis machines
Toyobo	Medical and protein measuring biosensors

Source: DATAQUEST
June 1986

Advanced Robotics Project

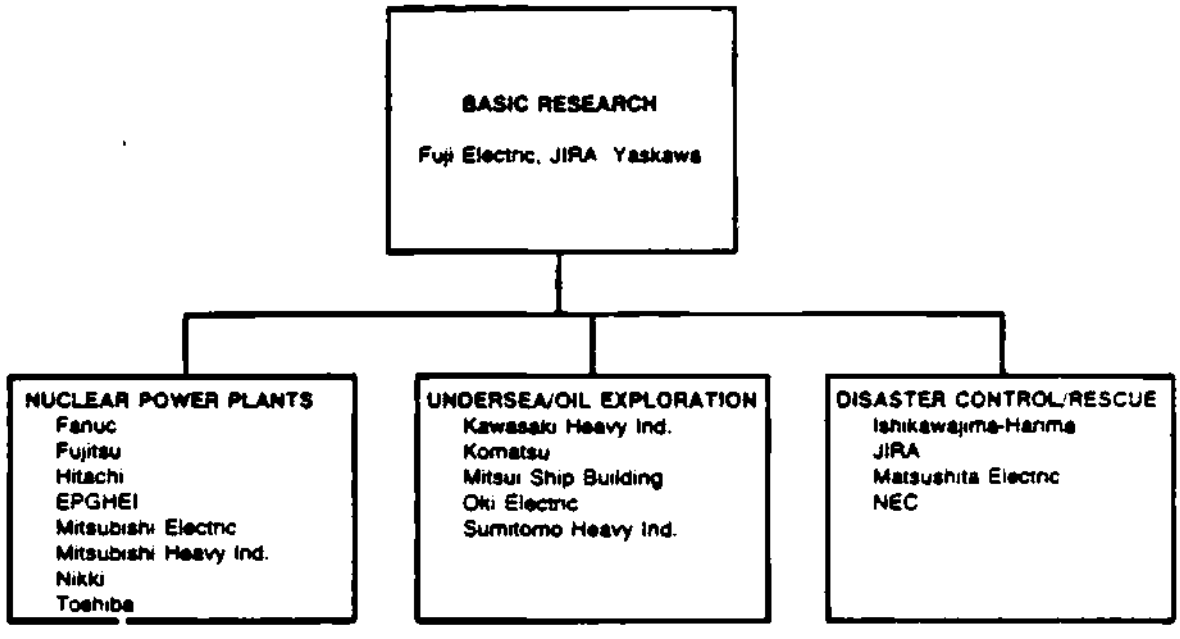
ADVANCED ROBOTICS PROJECT (JUPITER)

In 1983, MITI (Ministry of International Trade and Industry) launched the Advanced Robotics Technology Project, also known as the JUPITER Project, to develop versatile, mobile robots sophisticated enough to replace humans in dangerous environments. The project is scheduled to run for eight years, until the end of fiscal 1990, and currently has a budget of ¥20 billion ($125 million). Headquartered in Tsukuba Science City, the project is being managed by MITI's Agency for Industrial Science and Technology (AIST). Two MITI research laboratories, the Mechanical Engineering Laboratory (MEL) and the Electrotechnical Laboratory (ETL), are participating in the research.

Robotics research is focused on four areas: basic robotics technology, nuclear power plant operations, undersea/oil development operations, disaster control/rescue operations. Figure 1 shows the research assignments of the 19 Japanese companies participating in the project.

Figure 1

PARTICIPANTS IN MITI ADVANCED ROBOTIC RESEARCH



Source: MITI
Dataquest
June 1986

Advanced Robotics Project

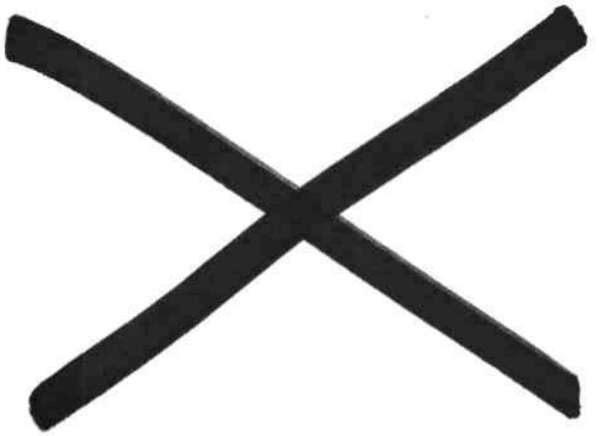
The basic robotics technology component of the project covers a broad range of research areas with practical applications to the other three areas. Specifically, the project focuses on:

- Locomotion--multilegged robots, climbing robots, and wheeled robotics locomotion systems suitable for rugged, unpredictable terrains
- Manipulation--Complex manipulators capable of complicated, multijointed, and multifingered manipulation, and automatic diagnostic technology
- Sensors--Visual, tactile, sound, odor, humidity, and other sensors, robotics navigation systems, and high-speed voice- and pattern-recognition systems
- Kinematics--Low-power-consumption motors, large-torque actuators, and efficient speed reducers using lightweight materials
- Autonomous control--Automatic navigation systems, environment modeling and knowledge representation, vision systems designed for mobile robots, and dynamic suspension systems
- Teleoperation/tele-existence--Human movement and physiological condition-measuring technology, anthropomorphic mechanism design and control technology, data acquisition technology using artificial organs, and tele-existence display technology that gives the operator the sensation of being present at a remote site

In February 1986, MITI and the Japan Robotics Association also established two new joint R&D programs. The first is a two-year program to develop proximity sensors, touch sensors, standards, and commercial applications. MITI, Fujitsu, Toshiba, and robot makers will participate in this program. The second is the establishment of three research groups to investigate direct driver (DD) robot technology, environmental measuring sensors, and robot technology education.

Once these basic technologies have been developed, the participating companies will develop integrated systems, robot language systems, and evaluation methods to adapt them to nuclear power plants, marine development, and disaster operations.

To encourage foreign participation, MITI established the $4 million Robot Center for International Cooperation in 1985. The center plans to promote joint international R&D, to work to establish advanced international robotics standards, and to enter technical licensing and joint venture agreements.



Industrial Policy

The following is a list of the material in this section:

- MITI Organization
- MITI R&D Laboratories
- MITI Industrial Policies

MITI Organization

BACKGROUND

The Ministry of International Trade and Industry (MITI) is a key ministry behind Japan's challenge in high-technology fields. Established in 1949 to direct postwar reconstruction efforts, MITI has evolved into the "general staff" for developing industrial policies (Sangyo seisaku) and promoting foreign trade. During its 37-year history, MITI has gone through five distinct phases, which were reflected in its industrial policies for each period:

- Postwar reconstruction (1949-1960)--Foreign exchange controls, technology importing, export promotion, protection of heavy industries
- High-growth era (1960-1973)--Export promotion, cartelized competition, protection of infant high-technology industries
- Oil shock and environmental crisis (1973-1980)--Energy conservation and alternative energies, pollution controls, consumer regulations, liberalization of tariffs and financial markets
- Shift to high technology (1980-1985)--Joint R&D projects, high-tech infant industry protection, basic research, trade friction intervention
- Regional era (1985-2000)--Technopolis and New Media Community infrastructure development, strengthening of regional testing laboratories, acceleration of next-generation R&D projects

In the early years, MITI was instrumental in creating the policy framework for Japan's economic success. However, because of the oil shock and environmental pollution in the mid-1970s, MITI was severely criticized for mismanaging the Japanese economy and was forced to rethink its industrial policies. Since 1980, MITI has successfully repositioned itself in high technology and regained credibility with the public by offering forward-looking (mae-muki) industrial policies and R&D programs. Working closely with private industry, MITI has laid the foundation for Japan's next-generation industries, such as electronics, biotechnology, new materials, and artificial intelligence.

MITI Organization

OVERALL STRUCTURE

MITI is organized into the Minister's Secretariat, seven bureaus, and five extra-ministerial bureaus, as shown in Figure 1. The key bureaus affecting high-tech industries include:

- International Trade Policy Bureau--Plans and implements Japan's trade policies, conducts surveys on overseas markets, and provides news releases, background information on Japanese industry, and press conferences through the MITI Information Office

- International Economic Affairs Department--Prepares basic policies on international trade and currency for the General Agreement on Tariff and Trade (GATT) negotiations and handles the tariff system

- International Trade Administration Bureau--Organizes expositions and trade fairs, supervises the Japan External Trade Organization (JETRO) branches, inspects import and export transactions, and issues import licenses

- Industry Policy Bureau--Promotes MITI's semiconductor industry policies, oversees business mergers and tie-ups, recommends Japan Development Bank (JDB) loans for plants and equipment, regulates taxes on industry, and handles foreign investments and technical assistance contracts

- Machinery and Information Industries Bureau--Plans and promotes comprehensive policies for electronics and data processing through the following divisions:

  - Electronics Policy--Conducts surveys and plans programs on the use of electronic machinery

  - Data Processing Promotion--Promotes computer use, development of software technology, and data processing service businesses

  - Industrial Electronics--Handles import and export of electronic equipment, electric measuring devices, communications equipment, computers, and semiconductors

  - Electrical Machinery and Consumer Electronics--Handles import and export of home electronic equipment

MITI Organization

- Agency of Industrial Science and Technology (AIST)--Promotes MITI's technology policy of transforming Japan's industrial structure into a "knowledge-intensive" one by operating a system of national R&D projects (including 16 research institutes) and fostering R&D activity in the private sector through subsidies. (AIST is separate from the Science and Technology Agency, which coordinates Japan's overall science and technology policies.) Key divisions include:

  - R&D Utilization Office--Patents MITI's research findings and makes contracts with business firms; handles joint research projects, technical guidance, and research under consignment; promotes computer use by the government; and investigates technical problems

  - Research Administration Office--Coordinates laboratory research programs and conducts joint research projects with private business

  - Planning Division--Plans the national system of laboratories and research institutes and oversees their transfer to the Tsukuba Science City

  - Technology Promotion Division--Grants subsidies and tax preferences to encourage industrial R&D

  - Technology Research and Information Division--Monitors research trends, conducts joint research programs with international organizations, and disseminates information on industrial science and technology

MITI's internal hierarchy differs from that of other ministries in that the Vice Minister, not the Secretariat, is the highest post. The high status accorded the Industrial Policy Bureau is a carryover from the 1960s when the industrial (domestic) faction dominated. Since the 1970s, the international bureaus have taken over. The internal MITI ranking is as follows:

1. Vice Minister
2. Chief, Industrial Policy Bureau
3. Director-General, Natural Resources and Energy Agency
4. Director-General, Medium and Smaller Enterprises Agency
5. Director-General, Patent Agency
6. Chief, International Trade Policy Bureau
7. Chief, Machinery and Information Industries Bureau
8. Chief, Minister's Secretariat
9. Chief, Basic Industries Bureau

10. Chief, Industrial Location and Environmental Protection Bureau
11. Chief, Consumer Goods Industries Bureau
12. Chief, Trade Bureau

MITI gives much authority to its younger officials, who generate most of the new ideas. Many policy proposals originate in informal, late-night brainstorming sessions. These policies are then routed through the MITI organization. Before major policies are approved, the Industrial Structure Council (Sangyo Kozo Shingikai)--MITI's channel to the business community--is consulted for recommendations and advice. The council consists of MITI's old boy network of retired vice ministers and key executives.

The Role of Administrative Guidance

When MITI was reorganized in 1949, it had significant legal powers over Japanese industry. The Foreign Exchange and Foreign Trade Control Law of 1949 empowered MITI to approve foreign currency transactions, joint ventures, licensing agreements, and technology transfers. MITI set limits on foreign exchange allocated to companies operating abroad to reduce Japan's capital outflow and to control the licensing of foreign technologies. MITI has even suggested joint ventures, such as in the case of Sony and Texas Instruments in 1967.

The term "administrative guidance" first appeared in MITI's annual report in 1962. It refers to MITI's authority to issue directives (shiji), requests (yobo), warnings (keikoku), suggestions (kankoku), and encouragement (kansho) to Japanese companies. MITI began to rely more heavily on its "administrative guidance" when it lost much of its legal powers with the passage of the Special Measures Act of 1963. In 1979, MITI's formal authority was further diminished by the revision of the Foreign Exchange and Foreign Trade Control Law of 1949 and liberalization of the financial markets. Currently, MITI cannot restrict foreign exchange transactions; companies only have to notify MITI when they enter a joint venture or licensing agreement. (As a result, DATAQUEST has observed a boom in joint ventures and licensing agreements with foreign companies since 1980.) Thus, MITI is a "lion without legal teeth" that must rely on its influence and credibility (the carrot) to guide Japanese industry.

MITI currently provides "administrative guidance" in several ways, including:

- Issuing broad-ranging policy "visions"
- Conducting surveys and developing industry forecasts

MITI Organization

- Organizing and funding joint R&D projects in sunrise industries
- Offering advice, industry contacts, and financing through government banks
- Developing policies and action plans to reduce trade friction

Ironically, MITI's influence was on the wane in the late 1970s but has been revived by growing foreign protectionism, especially in the area of semiconductors. For example, in response to U.S. dumping margins, MITI recently proposed a three-pronged semiconductor monitoring system that would include:

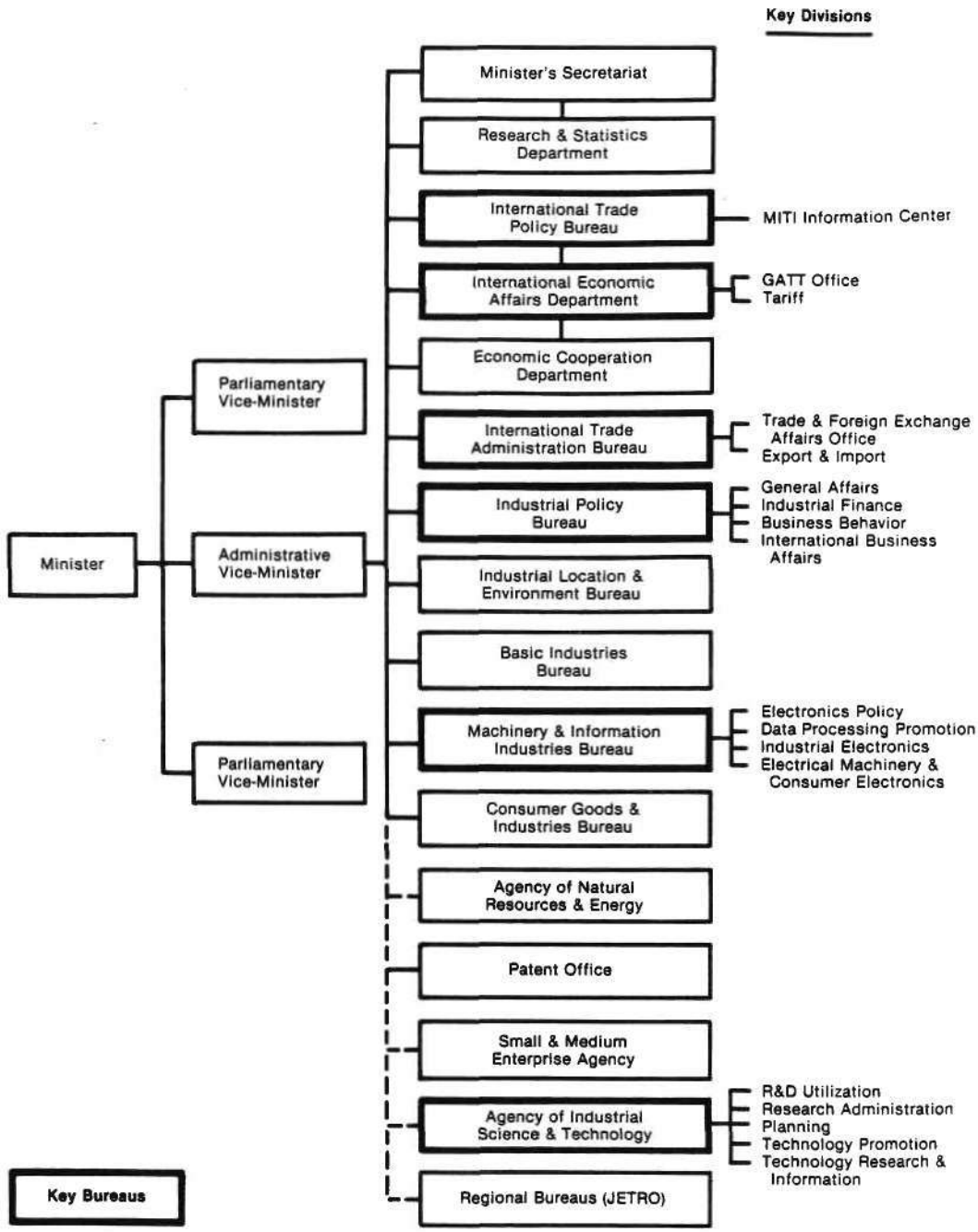
- A quarterly semiconductor production monitoring system that would restrain excessive production
- Establishment of floor prices based on fully load manufacturing cost data supplied to MITI by Japanese semiconductor makers
- Voluntary restraint on excessive shipping of DRAMs and EPROMs through Southeast Asia to avoid U.S. dumping margins

MITI is encouraging Japanese semiconductor makers to support this proposal in order to reduce trade friction with the United States. By offering policy solutions to urgent industry problems, MITI is reasserting its influence over Japanese industry. It appears that reducing trade friction and organizing joint R&D projects are the two major forms of MITI administrative guidance.

MITI Organization

Figure 1

MITI'S ORGANIZATIONAL STRUCTURE



Source: DATAQUEST
July 1986

MITI R&D Laboratories

TSUKUBA SCIENCE CITY LABORATORIES

Tsukuba Science City, nicknamed the "City of Brains," is located about 35 miles northeast of Tokyo. Completed in 1977, Tsukuba has the largest concentrations of researchers in Japan, with more than 11,500 researchers and support staff in fifty national research institutes and two universities.

MITI's Agency for Industrial Science and Technology (AIST), founded in 1948, is a semi-independent organization with the charter of monitoring scientific developments around the world, identifying key technologies for Japanese research, sponsoring research, and encouraging patent and licensing agreements. AIST has 2,640 elite researchers nationwide, or one-fourth of all Japanese government researchers. About 1,855 researchers work at AIST's Tsukuba Research Center, which spent about $130 million for basic research and joint R&D projects in 1984. As shown in Table 1, the center is a complex of nine research laboratories. The largest is the Electrotechnical Laboratory (ETL), where 525 researchers are working on next-generation electronics. However, electronics-related research is also conducted at other MITI laboratories.

REGIONAL TESTING LABORATORIES

In addition to the Tsukuba Research Center, MITI operates industrial development laboratories in each Japanese region, as shown in Table 2. These laboratories act as "technology transfer agents" to speed the diffusion of technology from MITI's national R&D projects to regional industries, and work closely with local companies to upgrade their technological levels. In general, MITI's Tsukuba Research Center pursues generic basic research at the national level, while the regional laboratories explore local industry-specific applications research. For example, MITI's Kyushu lab is developing ways to utilize high technology to boost the productivity of the region's traditional coal, ceramics, and textile industries.

MITI R&D Laboratories

Table 1

MITI RESEARCH LABORATORIES IN THE TSUKUBA SCIENCE CITY

Laboratory	Research Themes (Number of Researchers)
National Metrology Research Lab	Measurement standards, lasers, X-rays (137)
Mechanical Engineering Laboratory	Robotics, bionics, medical & biological engineering, optical measuring, wind-energy conversion, high-precision controls, energy storage, undersea production, aids for the physically handicapped (213)
National Chemical Lab	Coal liquefaction, aluminum smelting, super-conductive materials, hydrogen energy, fine chemicals, heat storage, gene technology, pollution prevention, synthetic membranes (289)
Fermentation Research Institute	New enzymes, recombinant DNA, bioreactors, micro-organism industrial processes, industrial waste water treatment, cell fusion, biomass energy generation, photosynthesis hydrogen production (61)
Polymer & Textiles Research Institute	Computer-designed apparel, new plastics and polymers, 3-D fabrics, bioreactors, artificial kidneys, bio-engineering, chemical absorbents, synthetic fibers, IC lithography (100)
Geological Survey of Japan	Energy & mineral surveys, earthquake prediction, undersea development, geothermal energy, deep sea mining, industrial pollution (218)
Electrotechnical Laboratory	Supercomputers, optoelectronics, microelectronics, intelligent robots, speech processing, energy conservation, new materials, space development, nuclear power, pollution control, superconducting magnets, lasers (525)

(Continued)

MITI R&D Laboratories

Table 1 (Continued)

MITI RESEARCH LABORATORIES IN THE TSUKUBA SCIENCE CITY

Laboratory	Research Themes (Number of Researchers)
Industrial Products Research Institute	Sensors, speech synthesizers, visual aids for the blind, computer-aided design (CAD), ergonomics, bionics, carbon fibers, composite materials (103)
Pollution & Resources Research Institute	New mining and mineral process technologies, coal liquefaction, geothermal energy, energy conservation, pollution control, industrial safety (209)

Total Researchers: 1,855

Source: Ministry of International Trade and Industry
DATAQUEST
June 1986

MITI R&D Laboratories

Table 2

MITI's INDUSTRIAL DEVELOPMENT LABORATORIES

Region	No. Staff	FY 1984 Budget	Major Research Activities
Hokkaido	104	¥1.3B ($5.5M)	Coal uses, waste disposal, pollution controls, energy conservation (Sunshine Project), biomass, plant automation
Tohoku	57	0.5B ($2.2M)	Materials, mineral resources, energy conservation (Sunshine Project)
Nagoya	268	2.8B ($11.6M)	Energy, oil pressure uses, production machinery, measuring equipment, metal alloys, electronics, radiography, inorganic materials, biomedical and health care equipment
Osaka	238	2.7B ($11.2M)	Ceramics, inorganic and compound materials, housing materials, pollution control, housing materials, new energy
Chugoku	54	0.8B ($3.3M)	Inland Sea hydrologic studies, marine environment protection, production machinery
Shikoku	46	0.5B ($2.2M)	Thermal energy, marine development, organic & inorganic chemistry, biochemical pulps, nuclear power safety, laser equipment, metal ion separation
Kyushu	94	0.9B ($3.8M)	Coal uses, energy generation and conservation (Sunshine & Moonlight Projects), carbon ceramics, textiles, pollution control
Total	861	¥9.5B ($40.1M)	

Source: Ministry of International Trade and Industry
DATAQUEST
June 1986

MITI Industrial Policies

VISIONS FOR THE 1980s

In 1980, MITI (Ministry of International Trade and Industry) issued its famous "Visions for the 1980s," which called for promoting basic research in next-generation industries, such as electronics, new materials, artificial intelligence, and biotechnology. Based on its earlier "Visions for the 1970s," which emphasized Japan's emergence as an information-intensive society, the 1980 Visions exhorted industry leaders to make a shift from imitation to innovation. Rather than copying and improving existing products and manufacturing processes, MITI encouraged industry to pursue new materials and creative products and designs. MITI's goals are essentially twofold: to eliminate Japan's "copycat" image and to promote higher-value-added products. If quality was Japan's industrial slogan for the 1950s and 1960s, creativity has become its rallying cry for the 1980s and 1990s.

Contrary to popular belief, MITI's "Visions for the 1980s" was not a predetermined policy, but evolved in response to major challenges facing Japan in the late 1970s, including:

- The vulnerability of Japan's energy- and materials-intensive heavy industries to the 1973 and 1979 oil shocks and recessions
- The emergence of newly industrialized countries (NICs) in Asia, such as Malaysia, Singapore, South Korea, and Taiwan
- The shift from heavy industries to high-technology product and service industries
- Growing trade friction with the West and criticism of Japan's "copycat" mentality
- An informal technology boycott against Japan because of the "boomerang effect" (being bombarded by Japanese products developed from western technology)
- Growing confidence among Japanese companies that have achieved technological parity with the West

To accelerate the shift to high technology, MITI identified 14 industries for rapid development during the 1980s and 1990s: aircraft, space, optics, biotechnology, medical electronics, industrial robots, ICs, computers, word processors, metal-based new materials, fine ceramics, medicine and medical supplies, industrial machinery, and software. These technologies are intended to become the drivers of Japan's economic growth in the twenty-first century. Unlike previous

"targeting" policies, MITI's Visions is more of a gunshot approach. MITI is spreading its limited funds over a wider range of technologies and requiring greater corporate investments.

Initially, Japanese companies viewed MITI's Visions as just another policy statement, but growing worldwide protectionism, U.S. dumping margins, the rapid yen appreciation, and U.S. calls for cutbacks in Japanese capital spending have convinced Japanese government and corporate leaders that they cannot afford to pursue "business as usual." As a result, Japanese makers are diversifying their product lines and boosting R&D spending. A recent MITI survey estimated that R&D spending among the top 12 Japanese semiconductor makers averaged 17 percent of semiconductor revenue in 1985, up from 11 percent in 1984. Part of this increase was due to a smaller revenue base, but absolute R&D spending also grew. Increasingly, MITI and Japanese companies see the development of creative, proprietary technologies as essential for keeping ahead of South Korea and as "bargaining chips" in negotiations with foreign companies.

MITI INDUSTRIAL POLICIES FOR THE 1980s

During the 1980s, MITI has developed an array of "take-lead" industrial policies to maintain Japan's international competitiveness. Unlike its previous interventionist method of guiding industry, MITI's new policies emphasize private investments and collaborative research. They are designed to take advantage of the major trends changing Japanese society: internationalization, aging of the population, liberalization of tariffs and financial markets, regionalization, and a growing desire for innovation and creativity. Instead of using the stick, MITI now uses the carrot--joint R&D projects and funding--to encourage industries to shift to high technology. MITI's new role is that of catalyst, strategist, cultivator, advisor, and negotiator.

What are MITI's key high-technology industrial policies for the 1980s? The following is a summary of MITI's main thrust.

Joint Research and Development

- Parallel-Track Joint R&D Projects--Since 1980, MITI has formed more than 30 national high-technology R&D projects with private industry (see section 3.4); more than 10 projects focus on semiconductors.

MITI Industrial Policies

- Sale of MITI Patents--In July 1984, MITI began licensing patent rights from its projects to private industry in order to generate new revenue; in October 1984, the Japan Industrial Technology Promotion Association went to the United States and Canada to license 30 MITI patents in ceramics, electronics, mechatronics, and biotechnology.

- New High Technology University--In July 1984, MITI announced its support of a new private university in Tsukuba Science City to train high-technology engineers and scientists; the Ministry of Education is also encouraging joint university-industry R&D.

- Opening of MITI Labs--In 1985, MITI opened its laboratories in Tsukuba Science City to Japanese companies for the first time; companies may use MITI equipment or bring in their own.

- Joint Research Centers--In 1985, MITI and the Ministry of Posts and Telecommunications (MPT) established the Japan Key Technology Center for joint research and will establish 28 joint R&D projects.

- International Cooperation--Since 1982, MITI has actively promoted cooperation with foreign nations in high-technology fields to reduce trade friction and avoid a technology boycott by western nations (see Section 3.3 for details).

Financial Incentives

- Tax Breaks for High-Technology Industries--Accelerated depreciation is allowed.

- Industrial Financing for New Plants--The Japan Development Bank (JDB) and Hokkaido-Tohoku Development Bank offer 7.3 percent loans for building new plants in Japan's technopolis zones.

- Japan Export-Import Bank Loans--In 1984, MITI established a special finance program to offer 6.0 to 6.5 percent loans to companies opening R&D facilities overseas.

- New Media Loan Program--In 1984, MITI and MPT established a loan program to encourage local governments to introduce new media infrastructure, such as cable TV, on-line data bases, and videotex.

MITI Industrial Policies

Infrastructure Development

- Industrial Location Promotion--MITI maintains an on-line data base of over 2,000 industrial parks throughout Japan and a monthly listing of plant siting in each prefecture.

- Technopolis Program--In 1980, MITI announced the Technopolis Concept, an ambitious program to develop 19 "Silicon Valleys" throughout Japan; in 1986 this number will be expanded to 26.

- New Media Community Program--With the convergence of computer telecommunications, MITI is encouraging cities to test experimental telecommunications networks and services; the Ministry of Posts and Telecommunications (MPT) is promoting an identical program known as the Teletopia Concept.

- Commuter Airport Program--With the Ministry of Construction, MITI is promoting the construction of commuter airports throughout Japan to link the technopolises to Tokyo and Osaka.

MITI POLICIES FOR FISCAL 1986

Due to growing trade friction and worldwide protectionism, MITI is emphasizing greater internationalization of the Japanese economy. Specifically, MITI is promoting reduced reliance on exports, expansion of domestic demand, promotion of foreign imports and investments in Japan, adjustments in Japanese investments abroad, collaborative R&D and researcher exchanges, and improved information exchanges. In addition, MITI supports accelerated high-technology development, venture business activity, alternative energy development, and a larger role for the private sector.

During fiscal 1986 (April 1986 to March 1987), MITI has allocated the following budgets to each major policy thrust, as shown in Table 1.

MITI Industrial Policies

Table 1

MITI's FISCAL 1986 INDUSTRIAL POLICY BUDGET ALLOCATIONS

Policy	Program	$Millions
Internationalization	New Industrial Society (Silver-Polis) Plan	$90.6
	Economic Revitalization Center	42.5
Import Promotion	Import Promotion Activities	7.1
	Venture Business Import Sales Promotion	0.7
	Import Promotion/External Investment System (JDB)	62.5
International Cooperation	International High-Tech Association (survey)	0.1
	International Joint R&D Activities	0.3
	International Robotics Center	15.9
	Solar Power Battery System	44.6
	Foreign Researcher Invitation Program (Japan Trust)	n/a
	Japan Trade Promotion	13.1
	ASEAN Cooperation	0.2
Technology Development	Next-Generation Industries R&D	40.8
	Large Scale Industrial Technology R&D	96.4
	New Energy R&D (Sunshine Project)	269.2
	Energy Conservation (Moonlight Project)	76.2
	Basic Technology Research Center	200.0
	Commercial Jet Engine Development (V2500)	25.0
	Commercial Jet Development (YXX)	4.5
	International Jet Joint R&D Fund (JDB loans)	43.8
	5th Generation Computer	28.1
	Interoperable Database System	5.3
	Supercomputer	18.3
Technology Development	Data Processing Reliability Improvement (JDB loan)	68.8
	New Materials	22.4
	Advanced Production System	0.1
	Biotechnology	7.6
	Bioindustry Measures	0.8
	Govt/Private Joint R&D System	1.4
	Key Regional Technology Development	1.6
Data Processing	Data Processing Promotion Association	1.4
	Data Processing Training Activities	6.3
	Data Base/Information Services	0.7
	Computer/Communications System Promotion	46.9
	Basic Data Base Development Foundation	46.9
	Software Program Development Promotion	32.5
	Software Program - Japan Development Bank loans	1.9

(Continued)

Table 1 (Continued)

MITI's FISCAL 1986 INDUSTRIAL POLICY BUDGET ALLOCATIONS

Policy	Program	$Millions
Data Processing (Continued)	Interoperable Data Base	5.3
	Computer Reliability	68.8
	Computer Promotion Fund - JDB loans	406.3
	Model Community Information System	0.4
	New Media Community Concept (Basic R&D Center)	93.8
	Regional Information Promotion (Tohoku Bank loans)	12.5
Venture Business	Venture Business Promotion	8.3
	Venture Business Import Promotion	0.7
	Software Promotion	1.3
	Information Network Promotion	2.3
	High-tech/Information Equipment Leasing	62.5
	Information Advisor System	2.8
	Venture Business Information Promotion	220.6
	Venture Business Structural Improvement Loans	806.3
	Other programs	15.9

Source: MITI
DATAQUEST
June 1986

Overcapacity/Depressed Industries Policies

MITI has played a central role in reducing overcapacity among Japanese industries. Through the early 1970s, its major policy tool was the recession cartel, which called for short-term production cutbacks to avoid costly price wars. However, after the 1973 oil crisis and the 1974 to 1975 recession, MITI concluded that these adjustment measures were inadequate to cope with industries hit by high energy costs, such as aluminum, paper, and petrochemicals, or loss of long-term competitiveness, such as textiles and shipbuilding.

In May 1978, the Japanese Diet passed MITI's proposed Law on Temporary Measures for the Stabilization of Specific Depressed Industries, which granted troubled industries antitrust immunity to reduce surplus capacity in line with restructuring plans developed by MITI and its advisory group, the Industrial Structure Council. Under the law, a "depressed industry" was defined as an industry in which most of its companies were losing money. Two-thirds of these depressed industries agreed to join MITI's program. MITI forecast industry supply and demand, and the amount of industry capacity and surplus plant and

equipment that had to be decommissioned. Six industries with fourteen products reduced their capacity about 95 percent under the 1978 law: shipbuilding, steel (ferrosilicon and electric furnace steel), nonferrous metals (primarily aluminum), chemicals (ammonia, area, and phosphoric acid), paper (corrugated cardboard), and textiles (four synthetic fibers, cotton, and wool yarn).

Reluctant to give up its enormous powers over Japan's declining industries, MITI proposed an extension of the 1978 law, arguing that its restructuring program had been delayed. In May 1983, the Japanese Diet renewed the depressed industries law for another five years. Called the Law on Temporary Measures for Structural Adjustment of Specific Industries, the new law not only calls for the contraction of industry capacity, but also industry rationalization (reorganization) and modernization. Declining industries were encouraged to enter joint purchasing, production, sales, storage, transportation, and distribution ventures through mergers. Cooperative R&D, energy and raw material cost reductions, product quality improvements, and new product and process technologies were also emphasized. MITI must secure antitrust clearance from the Japanese Federal Trade Commission before approving industry tie-ups. However, Japan's Anti-Monopoly Law exempts the joint disposal of surplus plants and equipment.

The Ministry of Finance also grants four types of financial assistance to declining industries:

- A loan guarantee fund to facilitate the scrapping of plants and equipment that had been pledged as collateral for bank loans.
- Japan Development Bank (JDB) low-cost loans for the disposal of excess capacity, introduction of new technologies, and installation of efficient plants and equipment.
- Ten-year tax write-off of scrapped equipment losses and 18 percent depreciation allowance on the first year of approved investments
- A 50 percent government subsidy for approved R&D projects

Although MITI's depressed industries law softens the blows of demand cutbacks and overcapacity, DATAQUEST observes that the law has stirred significant debate in Japan. Some critics argue that free market competition is much more efficient than government intervention and subsidies to cut back excess capacity. MITI's powers give inefficient manufacturers an extended life and force others to reduce efficient plants. On the other hand, MITI intervention offers an orderly contraction of industry when the only genuine alternative is a heated

export battle. The irony is that, although U.S. officials dislike MITI's restructuring plans, trade pressures have forced MITI to act on behalf of Japanese industry. Protectionist sentiment in Washington, D.C., has resurrected the old MITI.

Import Promotion Policies

U.S. pressure to open Japanese markets has also endowed MITI with growing influence over Japanese import policies. In October 1983, Prime Minister Yasuhiro Nakasone announced that Japan would "move beyond market opening measures into the realm of active import promotion." This new strategy involves a variety of new MITI policy tools: the promotion of foreign investment and plant siting in Japan's new technopolis regions, low-interest import financing by the Japan Development Bank and Export-Import Bank, short-term yen loans for importers, revised standards and certification systems, improved distribution systems for imported products, and more business information from the Japan External Trade Organization (JETRO), MITI's overseas promotion arm. However, DATAQUEST believes that while these are positive, market-opening gestures, they amount to selective import promotion since the importing of certain agricultural products and high-value-added products is still strictly controlled.

In 1985, due to growing trade friction with the United States, MITI called a meeting of 60 top Japanese executives to request them to submit "Affirmative Procurement Plans." These plans would list products that the company needed to procure externally and its dollar commitment to buying U.S. products. Although not legally enforceable, MITI officials urged Japanese companies to participate to avoid protectionist legislation. Since then, Hitachi, NEC, and other top electronics companies have announced their procurement plans.

In May 1986, as part of the Market Opening Sector Specific (MOSS) talks, the Japanese government tentatively agreed to the following market-opening measures:

- A doubling in the U.S. share of the Japanese semiconductor market from 10 percent to 20 percent within five years
- A system to monitor prices of Japanese chip exports to prevent dumping
- Suspension of several lawsuits pending against Japanese semiconductor makers for alleged unfair trade practices

MITI Industrial Policies

DATAQUEST believes that MITI will play an increasingly active role in administering this program and coordinating overcapacity, trade friction, dumping, and import promotion issues. For MITI bureaucrats, long ignored by Japanese electronics makers, these trade issues give MITI a renewed sense of mission and purpose.

MITI'S LONG-RANGE PLANS

Japan's Shift to Creative Research

This year, the Japanese government is accelerating its push into creative basic research. In March, the Nakasone Cabinet approved a Science and Technology Agency (STA) proposal to promote more government-industry-university cooperation in basic research. The plan calls for expanding national testing laboratories, increasing R&D spending and researcher training, and improving the diffusion of technical information. Sixteen high-technology fields will be emphasized, including aerospace, electronics, new materials, biotechnology, and health care. The proposal has also targeted the following electronics research: optical devices and beams, ion beams, X-ray analysis, ceramic particles, vacuum conditions, synchrotron orbital radiation (SOR) for megabit memories, biochips, and new substrates. DATAQUEST believes research in these fields will be long-term (10 years), with initial commercialization beginning in the early 1990s.

Venture Capital and Venture Business Promotion

Since World War II, MITI's policies have been oriented to large corporations, but in recent years MITI has also promoted small and medium-size businesses (venture businesses). In 1975, MITI established the Venture Enterprise Corporation (VEC) to lend up to $400,000 to venture businesses for R&D purposes at 4 percent interest from a commercial bank, with VEC guaranteeing 80 percent of the loan for up to eight years. By 1984, VEC had guaranteed over 200 loans worth about $27 million, but most entrepreneurs shied away to avoid the paperwork and MITI interference. Without regulatory powers, MITI had little influence in directing venture capital companies to high-technology start-ups.

Since 1982, Japan has experienced a second "benchaa boomu" (venture capital boom) because of the rapid growth of high-technology industries and consumer demand for custom products. Moreover, investment funds are shifting away from declining heavy industries. In November 1983, the

MITI Industrial Policies

Ministry of Finance approved the creation of three American-style over-the-counter (OTC) markets at the Tokyo, Osaka, and Nagoya exchanges. The new rules require a net worth of about $850,000 and pretax profits of more than 4 cents a share for listing.

During this second venture boom, MITI is downplaying its interventionist role and emphasizing market incentives, as shown in Figure 1. In February 1984, MITI and the Small Business Agency announced a "venture business" subsidy program consisting of four financing systems:

- A new Small Business Finance Bank program that will issue loans of up to $1.5 million at 8.1 percent for 15 years
- An R&D subsidy program to finance half the development costs for new ceramics, biotechnology, and mechatronics
- Subsidies to 18 venture business cooperatives engaged in new ceramic research projects
- Subsidies to local industrial testing stations for purchasing mainframe computers

MITI is also proposing several laws to promote small businesses. The Small Businesses' New Technology Promotion Law would grant a buildup of investment loss reserves and preferential tax treatment for businesses selected by local governments as high-technology ventures. The Small Business Credit Insurance Law would allow venture businesses to obtain unsecured loans. MITI officials are considering four criteria for qualifying firms for tax incentives:

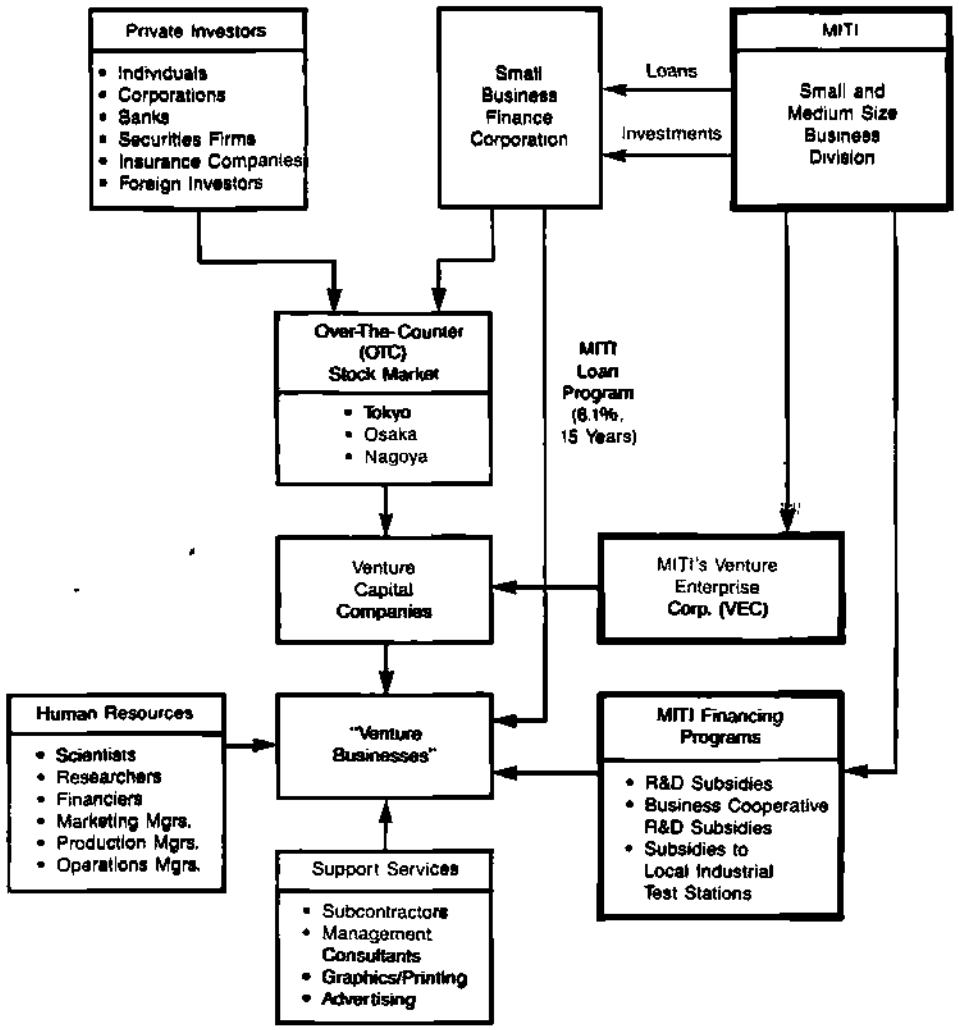
- Research in electronics, mechatronics, new materials, biotechnology, or computer software
- R&D spending of more than 3 percent of total sales
- Founded or moved into the high-technology field within the last 10 years
- Plan to be listed on OTC stock exchanges

MITI is also encouraging the Japanese Fair Trade Commission to remove its ban on the assignment of venture capital executives to start-up companies to strengthen the management of these firms.

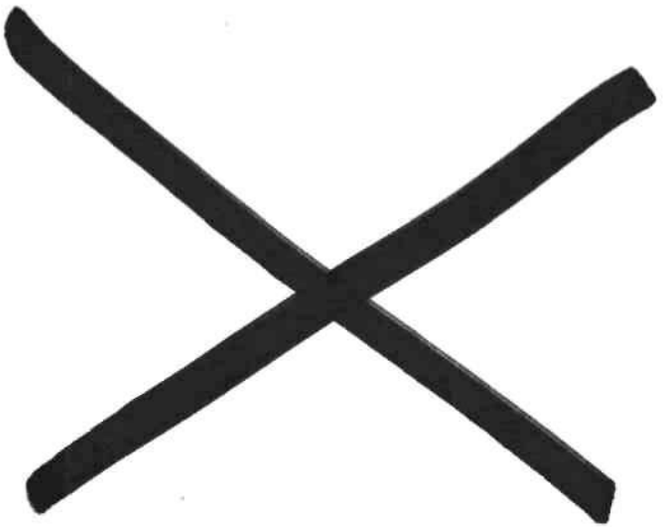
MITI Industrial Policies

Figure 1

MITI'S VENTURE BUSINESS PROMOTION ACTIVITIES



Source: DATAQUEST
June 1986



INS Program

NTT's INFORMATION NETWORK SYSTEM (INS)

NTT's idea for an advanced integrated services digital network (ISDN) originated in 1979, when Executive Vice President Yasusada Kitahara introduced the Information Network System (INS) concept at the Third World Telecommunications Forum of the Telecommunication Union (ITU) in Geneva. In his book, Information Network System--Telecommunications in the 21st Century, Dr. Kitahara argued that the merger of computers and communications would allow more information to be transmitted at a lower cost. His idea was to integrate separate local area networks (LANs) into a single, nationwide digital communications network that would consist of optical fiber trunk lines and satellites. Initial estimates placed the INS program cost at about ¥20 trillion ($100 billion), but this figure could rise to ¥30 trillion ($150 billion) over time.

Dr. Kitahara was an influential executive within NTT, and his INS concept appealed to NTT's officials who were concerned about the company's growing financial problems. DATAQUEST believes that INS was part of Dr. Kitahara's campaign to become the next NTT president. However, Mr. Shinto was brought in from outside NTT and quickly adopted the INS concept.

INS is a telephone company's dream: it will require all 44 million Japanese businesses and households currently hooked to NTT subscriber lines to buy new digital telephones. Moreover, INS will generate new revenues by allowing NTT to lease its circuits and offer high value-added network (VAN) services. If properly implemented, INS could be the key to NTT's financial solvency.

However, INS' high price tag will be a major obstacle. Although NTT is initially financing INS through depreciation on its existing assets, NTT will eventually have to raise more financing to complete the program. Because of the national budget deficit, government funding is out of the question. But the privatization of British Telecom demonstrates that NTT can become a private company and issue stock to finance the INS program. Thus, NTT privatization is essential to the success of INS.

Basic Concept

The INS program envisions linking Japanese businesses and households through a nationwide network of optical fiber cables, backed by direct broadcast satellites (DBS) and communication satellites. The all-digital system will unify all telephone, telex, data, videotex, facsimile, and information processing systems into a single network. Unlike existing

INS Program

telecommunications systems, INS will offer advanced computing to process, store, and transmit voice and video information. As proposed by Dr. Kitahara, INS consists of several basic concepts:

- Digitalization--NTT will gradually shift its entire telecommunications network from analog to digital by 1995; this began in 1979 with NTT's digital switching exchange.

- Integrated optical fiber/satellite network--Given Japan's numerous islands, heavy maritime traffic, and frequent floods, earthquakes, and other natural disasters, the INS network must have back-up satellites to support its main optical fiber trunk lines.

- Merger of computers and communications--The INS network will utilize the latest in computer and telecommunications technologies, symbolized by the INS Computer, which will merge supercomputer and fifth-generation computer technologies with the INS network.

- Video transmission--INS will emphasize new video communications technologies, such as sketch phones, videoconferencing, videotex, and video response systems (VRS).

- Machine-to-machine links--New systems will be designed with more computers and automatic remote control systems to link different communication systems and terminals.

- Enhanced communications processing--New functions such as temporary storage, media or size conversion, automatic language translation, message retrieval, and distributed supercomputing will be offered.

- Multistage star network embodying high-usage circuits--The INS network will be a multistage star consisting of 64 Kb/s circuit switching, high-speed circuit switching, packet switching, and leased lines at its core, and local switches at its periphery.

- Bit-based tariff system--NTT is investigating the possibility of charging system users according to the amount of digital information transmitted, not distance or time. NTT is still undecided because of the difficulties of raising local rates.

NTT's basic goal is to shift Japan's telecommunication system from voice-oriented analog communications to video-oriented digital communications, which parallels current market trends and advanced research

on the fifth-generation computer. Although based on CCITT's concept of an Integrated Services Digital Network (ISDN), INS will offer several unique features:

- Stored program control (SPC) technology as an intermediate step toward a fully digitalized system
- Bit-based tariff structure
- Greater emphasis on broadband capabilities (video processing)
- Advanced communications processing utilizing the INS computer
- Difference in channel interface standards

CCITT Standards

In the INS network, both user information and signals will be transmitted through the user-network interface. Two approaches have been adopted by NTT:

- Channel-associated signaling (Y interface)

  B (64 Kb/s) + D (4 Kb/s) and
  B (16 Kb/s) + D (4 Kb/s) = 88 Kb/s

  (B: information channel, D: signal channel)

- Common channel signaling system--CCITT (I interface)

  2 x B (64 Kb/s) + D (16 Kb/s) = 144 Kb/s

Although the CCITT standard (I interface) is more highly functional, it is less cost effective. Initially, NTT planned to begin INS service using the Y interface, then integrate the I interface when CCITT standards are determined. Besides cost considerations, DATAQUEST believes that NTT chose the Y interface to reduce transmission costs and control entry by foreign manufacturers.

In December 1985, NTT decided to postpone INS service until July 1986 due to problems arising from the differing standards. Because the Ministry of Posts and Telecommunications (MPT) is reluctant to begin INS service before CCITT announces ISDN specifications, MPT recently established study groups to investigate digital network service. On January 9, 1986, NTT announced that it will use both the Y interface (88 Kb/s) and CCITT's I interface (144 Kb/s) for the INS program.

INS Program

To standardize various protocols for INS services, NTT has developed an INS Protocol Reference Model (INSP-RM) based on the Reference Model for Open Systems Interconnection (OSI-RM) developed by ISO and CCITT. NTT rejected the OSI-RM because it was too general and abstract for practical implementation. To date, NTT has developed the following INS higher-layer protocols:

- Message handling systems (conformance with CCITT)
- Japanese character teletex (conformance)
- Mixed-mode teletex (conformance)
- Videotex (almost in conformance with OSI-RM)
- G4 facsimile (conformance)
- Higher-layer protocols of Data Communication Network Architecture (physical, data link, network, and transport conformance)
- Telewriting (under study)

NTT plans to develop an INSP-RM version 2 that will conform with OSI-RM wherever possible to avoid redundancy and ensure interconnection between INS protocols.

INS Development Schedule

NTT's goal is to develop the INS network by 1995. The program involves three development phases, as shown in Figure 1:

- Phase 1 (1979-1984)--Merging of individual digital communication networks for telephone, data, and facsimile into an integrated service digital network (ISDN) and laying of optical fiber cable trunk lines
- Phase 2 (1985-1990)--Introduction of communications processing (information storage and media conversion); expansion of system into regional cities and rural areas
- Phase 3 (1991-1995)--Establishment of an integrated network architecture and distributed information processing; unification of DDX and facsimile networks

INS Program

During the first phase (1979-1984), NTT began digitalizing its nationwide network, as shown in Table 1. Circuit switching, which began in December 1979, integrates digital transmission technology and time division switching with a stored program control (SPC), and links terminals. In contrast, packet switching service, begun in July 1980, uses a local office store-and-forward switching system to hold and transmit information in "packets," paving the way for a bit-based tariff system. Digital switching was extended to local and long distance calls in 1982 and 1983, forming the basis for the nationwide INS program.

As shown in Table 2, NTT has laid the foundations for its INS network. In 1984, NTT completed installing the 2,400km Japan Transverse 400-Mbs optical fiber trunk line that runs from Hokkaido in the north to Kagoshima City in the south (see Figure 2). CAPTAIN videotex service began in Tokyo and Osaka, and a model INS system began operations in the suburb of Mitaka-Musashino. In 1985, NTT's networks in Tokyo, Osaka, and Nagoya were digitalized, and a commercial INS system was opened at the Tsukuba Science City in time for the Tsukuba Expo 85.

Figure 1

INS DEVELOPMENT PHASES

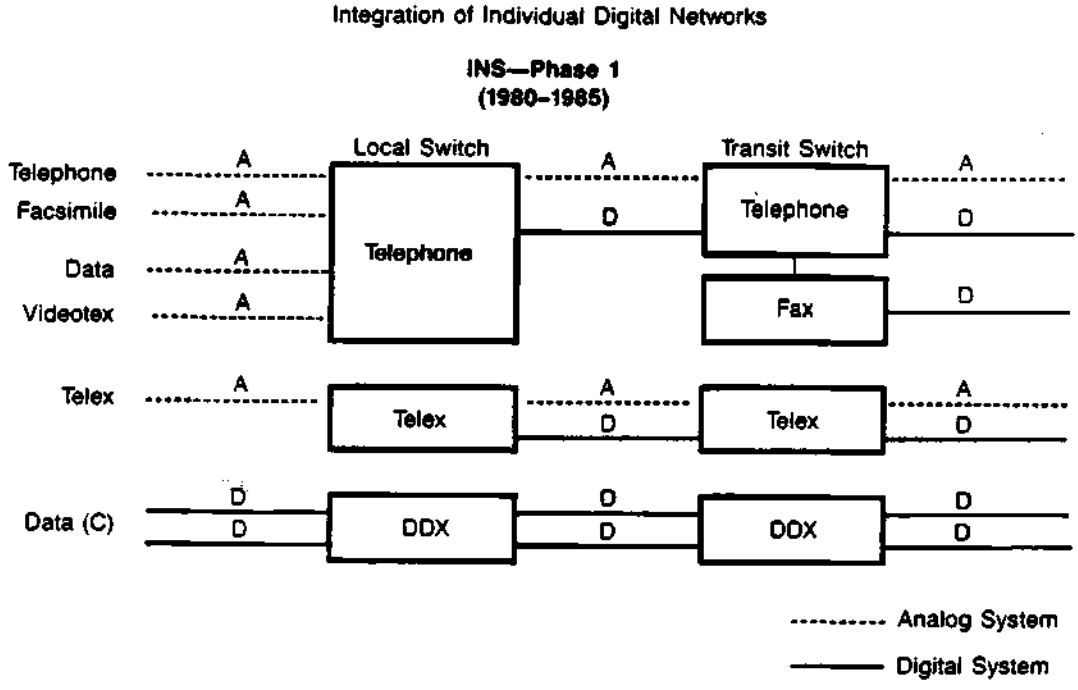


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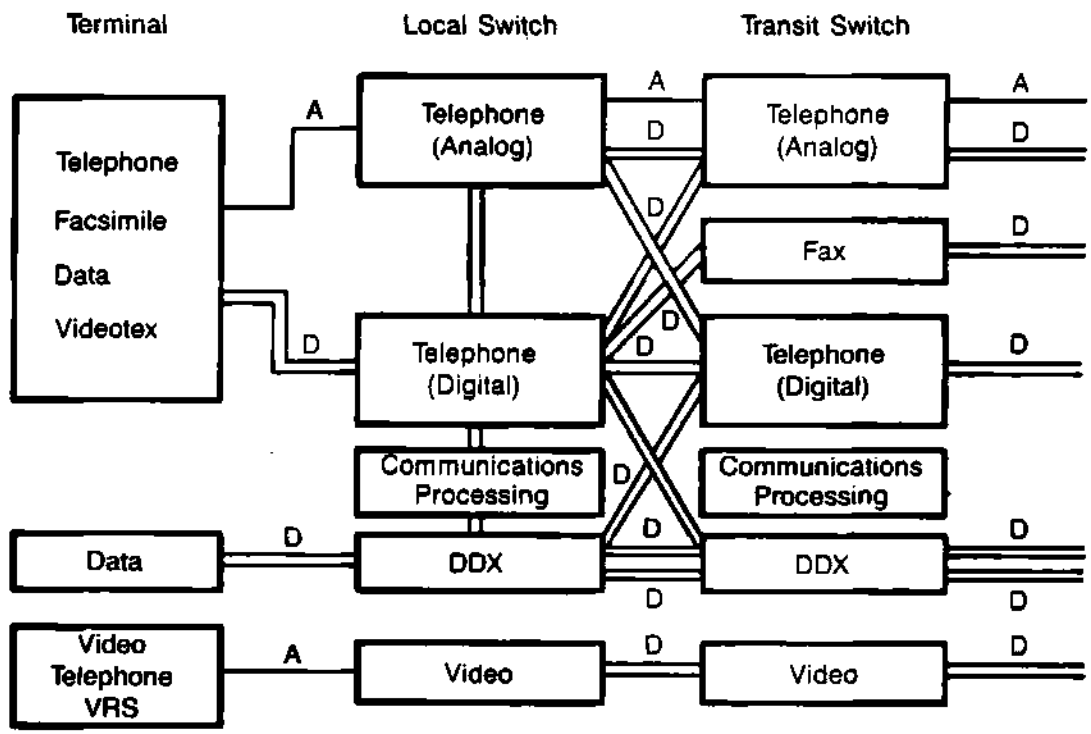
Figure 1 (Continued)

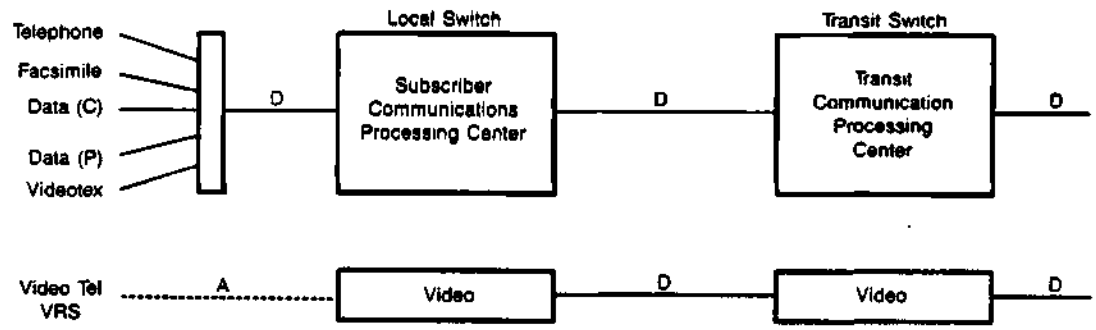
INS DEVELOPMENT PHASES

INS—Phase 2
(1985–1990)

Incorporation of Communications Processing



INS—Phase 3
(1990–1995)



Source: DATAQUEST
April 1986

INS Program

Table 1

NTT'S DIGITALIZATION PROGRAM

Year	System
1979	Circuit switching service
1980	Packet switching service
1981	Facsimile service
1982	D-60 digital switching (long distance)
1983	D-70 digital switching (local calls)
1983	16 major optical fiber lines; 16 digital exchanges
1984	Japan Transverse trunk line; 84 digital exchanges
1984	CAPTAIN videotex service in Tokyo and Osaka

Source: DATAQUEST
April 1986

Table 2

INS DEVELOPMENT SCHEDULE

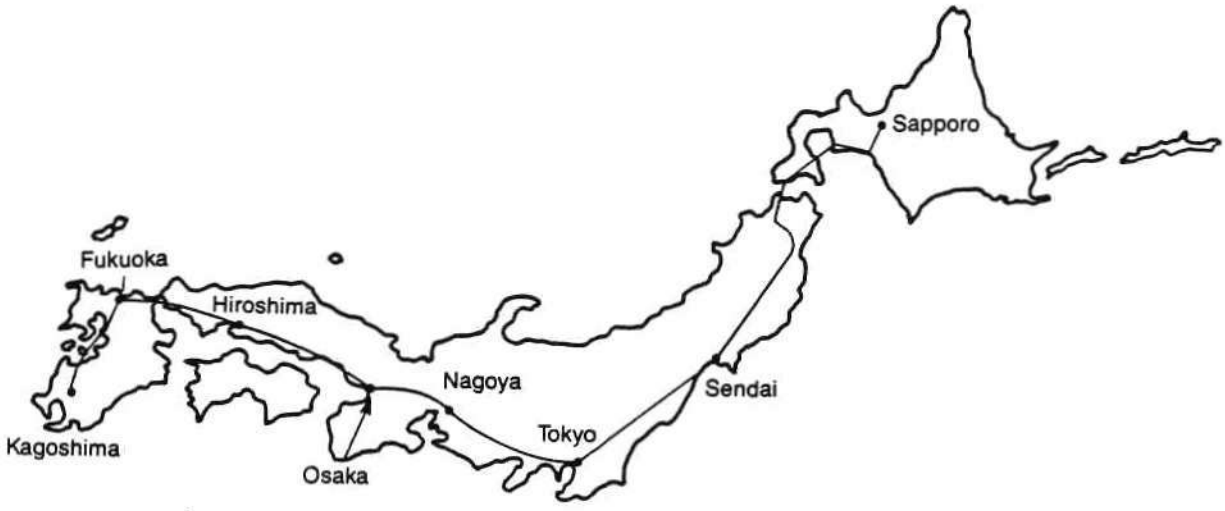
Year	Development Activity
1984-86	Mitaka model INS system
1985	Network digitalization between Tokyo, Osaka, Nagoya
1985	Commercial INS system at Tsukuba Science City
1985	Medical Information Service Company (CAPTAIN system)
1985	Testing of nationwide personal computer network
1986	Video response system (VRS) service
1986-87	INS expansion to prefectural capitals
1987	1.6-Gbs optical fiber trunk line in Tokyo-Osaka corridor
1988-90	INS expansion to midsize cities (over 100,000)
1990	Prototype INS Computer for communications processing
1990	Bit-based tariff structure
1995	Completion of nationwide INS network

Source: NTT
DATAQUEST
April 1986

INS Program

Figure 2

JAPAN TRANSVERSE TRUNK LINE



Source: DATAQUEST
April 1986

In October 1985, NTT began testing a nationwide personal computer communication network for homes and offices. The link connects the phone network with the public digital packet exchange network, and provides phone messaging and interactive computer services, such as banking and ticket reservations. Fees are ¥400 ($2) for 3 minutes, one-tenth that of regular digital data exchange charges. Because system compatibility is a major obstacle, MPT has established standards for PC communications equipment.

In November 1985, NTT established a subsidiary, the Japan Medical Information Company, with four banks and five NTT subsidiaries to provide medical information nationwide through the CAPTAIN system. The system will use the expert advice of 65 doctors to provide diagnostic services for 700 illnesses.

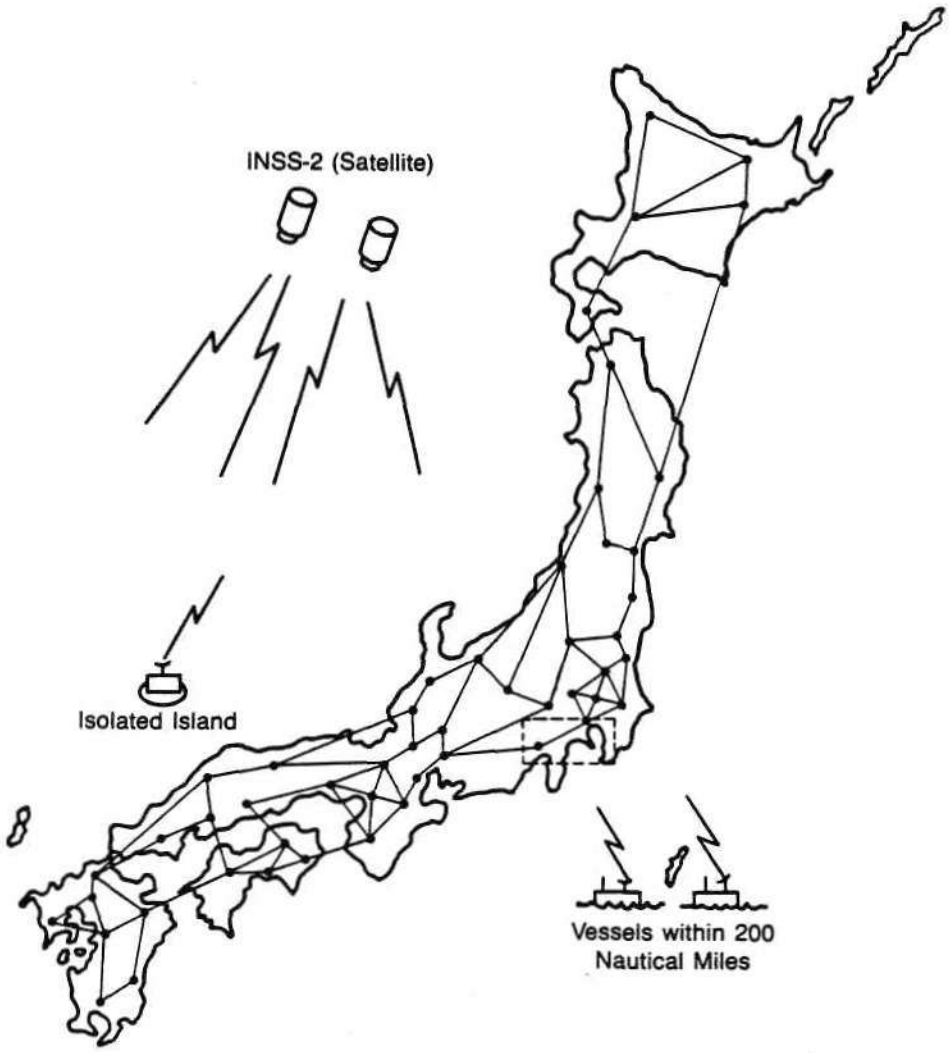
In 1986, NTT will introduce a video response service (VRS) designed for use in tourism, real estate, and medicine. The service, which utilizes the optical fiber network, can handle still pictures, photos, and image data bases. A maximum of 250,000 still pictures and images in 300 cassettes can be handled by one center linked to 255 terminals by 31 lines. Monthly fees will run about ¥100,000-¥150,000 ($500-$750).

INS Program

In 1986, NTT will expand the INS system to the prefectural capitals and medium-size cities throughout Japan. In 1987, NTT plans to begin laying a 1.6-Gbs optical fiber trunk cable between Tokyo and Osaka. By 1990, a prototype INS Computer will be tested in Tokyo and eventually be used for high-level communications processing. By 1995--the goal for completing INS--NTT plans to have installed INS computers throughout Japan as distributed processing centers, as shown in Figure 3.

Figure 3

FUTURE INS NETWORK



• Distributed INS Computer Processing Centers

Source: DATAQUEST
April 1986

NTT Investments

To establish the foundation for INS, NTT has invested heavily in new facilities and research. Under President Shinto, capital investments have been used mainly to digitalize NTT's network and replace existing circuits with optical fibers in preparation for INS. Capital spending has grown in absolute terms, but declined as a percentage of total revenues. As shown in Table 3, capital spending reached a peak of 43.2 percent of total revenues in 1980, dropping to 36.2 percent in 1985, while R&D spending grew from 2.0 percent to 2.7 percent.

Research, one of NTT's strong cards, is being accelerated to give NTT an edge over its domestic competitors in the VAN market and to generate new revenues from licensing agreements. Currently, NTT has nine research divisions that were recently reorganized within its four laboratories--Musashino Electrical Communication Laboratory (ECL), Yokosuka ECL, Ibaraki ECL, and Atsugi ECL. NTT is planning to open an R&D center in California's Silicon Valley to conduct joint R&D under Track III procurement and may open an R&D center in Europe in the future.

Table 3

NTT CAPITAL AND R&D SPENDING
(Billions of Yen)

	Fiscal Year					
	1980	1981	1982	1983	1984	1985
Total Revenues	¥3,855.6	¥4,006.3	¥4,167.1	¥4,344.3	¥4,552.4	¥4,756.2
Capital Spending	¥1,666.4	¥1,709.0	¥1,752.3	¥1,743.2	¥1,682.1	¥1,722.6
% of Revenues	43.2%	42.7%	42.1%	40.1%	36.9%	36.2%
INS Investment	-	-	-	-	¥ 380.0	¥ 480.0
% of Capital Spending	-	-	-	-	22.6%	27.9%
R&D Spending	¥ 75.5	¥ 80.2	¥ 88.5	¥ 93.9	¥ 93.9	¥ 126.6
% of Revenues	2.0%	2.0%	2.1%	2.2%	2.1%	2.7%
Combined R&D and Investment Spending	45.2%	44.7%	44.2%	42.3%	39.0%	38.9%

Source: NTT
DATAQUEST
April 1986

INS Program

Optical Fiber Construction

In January 1985, NTT finished installing the 3,300km Japan Transverse fiber-optic trunk line from Hokkaido in the north to Kagoshima in southern Kyushu. The 400-Mbs cable, begun in March 1983, uses paired cable connection to accommodate 5,760 channels. Testing began in February 1985 and operations in April 1985.

NTT plans to experiment with a 1.6-gigabit/second optical fiber prototype system, dubbed F-1.6G, in early 1986. The 120km cable will link Tokyo and Kofu and utilize new high-performance 1.3-micron laser diodes and noise-minimizing light receptors.

Satellite Program

Satellites are considered an extremely important component of the INS program because of their critical role during floods, earthquakes, typhoons, and other natural disasters that regularly affect Japan. As shown in Table 4, NTT plans to launch two types of satellites: communications satellites (CS) for commercial use and direct broadcasting satellites (DBS) for home use.

In February 1983, the National Space Development Agency launched CS-2a, Japan's sixth stationary satellite, for use as the main communications vehicle. During the transponders' idle time, NTT is conducting various experiments, including transmission of newspaper pages, cable TV transmission, electronic mail, videoconferencing, data transmission, and high-speed facsimile communications. The backup CS-2b was launched in August 1983.

In 1988, CS-3a and CS-3b will be launched to handle increased communications traffic. The Japan Satellite Broadcasting Company, a new venture capitalized at ¥7.3 billion ($36.5 million) by 189 investors, will lease the single commercial transponder. Twelve companies will provide high-definition TV entertainment and news reporting and pulse-code modulation (PCM) radio broadcasting. CS-4 is expected to expand NTT's capacity tenfold.

Kokusai Denshin Denwa (KDD), NTT's international affiliate, recently formed the International Satellite Communications Society Inc. (ISCS) to study the international satellite communications business and share information among its 10 co-founders (Anritsu, Fujitsu, Furuno, Hitachi, Japan Radio, Mitsubishi, NEC, Oki, Sharp, and Toshiba). ISCS has a budget of ¥50 million ($200,000), of which KDD contributed ¥40 million ($160,000).

Table 4

NTT'S SATELLITE PROGRAM

Year	Satellite	Number of Circuits	Features
		Communication Satellites	
Feb. 1983	CS-2a	4,000	Time division multiplex access; 350 kg; 8 transponders (6 in 20-30 GHz range)
Aug. 1984	CS-2b	4,000	Time division multiplex access; 350 kg; 8 transponders (6 in 20-30 GHz range)
Early 1988	CS-3a	20,000-25,000	Complement to ground units
Summer 1988	CS-3b	20,000-25,000	Complement to ground units
1993	CS-4	100,000-200,000	Marine radio; mobile communications; 20-GHz band transmitting; 30-GHz band receiving; 64-Kbs conversion
		Direct Broadcasting Satellites	
1978	BS-1		First experimental satellite for 1-meter-diameter antennas
Feb. 1984	BS-2a		2 of 3 transponders failed to work; originally for TV transmission to 440,000 subscribers in remote areas and high-rise buildings
Feb. 1986	BS-2b		Back up satellite. Two of three transponders failed to work; originally for TV transmission to 440,000 subscribers in remote areas and high-rise buildings
Feb. 1989	BS-3a		Wider broadcasting operations planned; 4-color TV channels

Source: DATAQUEST
April 1986

INS Program

In the area of direct broadcast satellites, Japan has been less successful. In February 1984, NASDA launched the BS-2a broadcast satellite, but two of the three transponders (supplied by Thomson CSF as a subcontractor of Toshiba) failed to operate. NASDA is debating whether to use Toshiba, which has developed its own transponders, or NEC, which has strong DBS technology through its work with Intelsat. Due to the failure of BS-2a, the launching of the backup BS-2b will be delayed to January or February 1986 and BS-3a to February 1989. Japan Broadcasting Corporation (NHK) plans to use BS-2b to test its high-definition TV and facsimile broadcasting, and a consortium of broadcasters plan to share one channel. However, Japanese broadcasters and antenna vendors are waiting for the operation of the large-capacity BS-3a in February 1989.

INS Computer

By 1990, NTT plans to spend $730 million to develop an advanced computer with information processing capabilities for the INS network. The INS Computer will combine fifth-generation computer (parallel processing, expert systems, and artificial intelligence) and supercomputer (ultrafast circuits) technologies. As shown in Figure 4, the INS Computer will form the information and communication nodes of the INS network. During Phase 2, a central INS Computer will be installed at the NTT headquarters. During Phase 3, multiple INS Computers will provide distributed communications processing throughout Japan.

Although most western media coverage has focused on MITI's Fifth-Generation Computer project, DATAQUEST believes that the INS Computer Project is more significant because of NTT's large research budget and its plans for actually developing and using the computer. MITI's project is more theoretical and oriented toward basic research.

Based on NTT descriptions, DATAQUEST believes the INS Computer will offer the following features:

- Fifth-generation computer technology
  - Knowledge base
  - Learning and knowledge acquisition
  - Inference mechanism
  - Natural language processing (automatic translation)
  - Visual and audio information processing

INS Program

- Speech recognition and syntnesis
- Automatic software production and testing

- Supercomputer technology
  - High-speed logic ICs (GaAs, Josepnson junctions, ballistic transistors)
  - Parallel processing (16-bit and 32-bit microprocessors, multiprocessors)

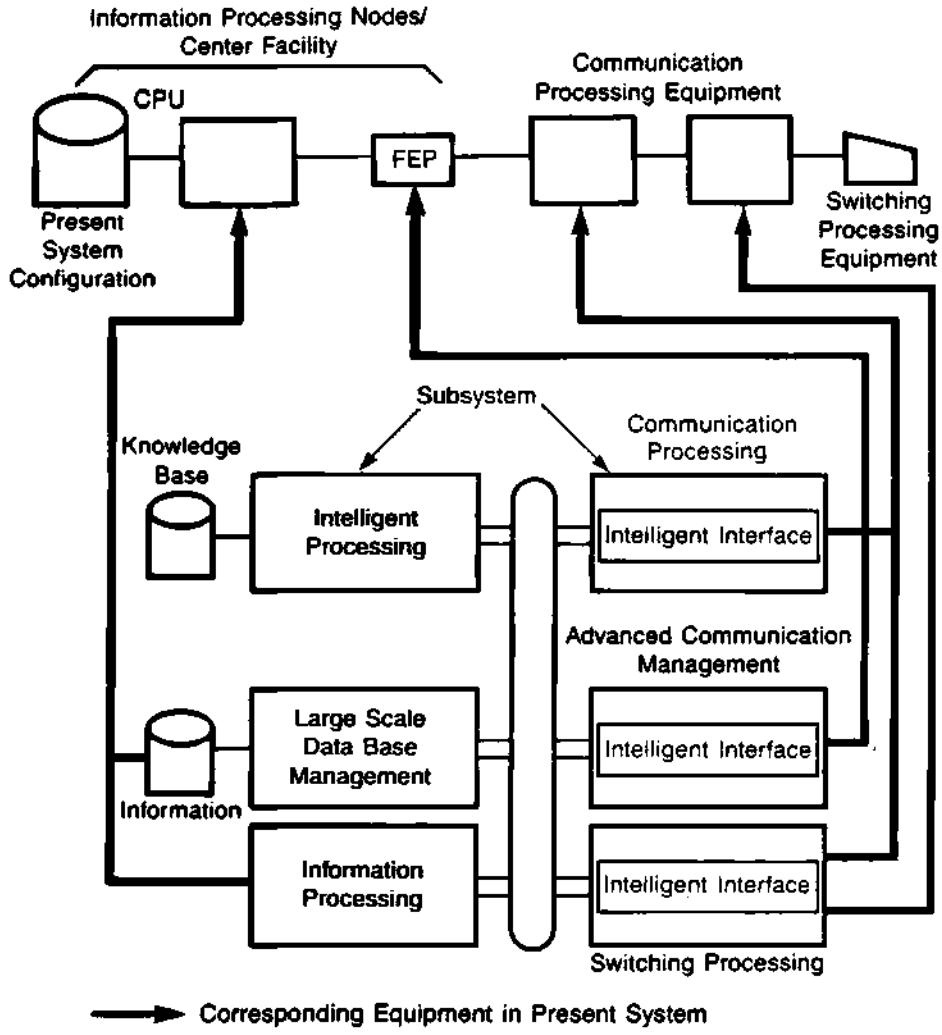
- Optoelectronics technology
  - Megabit memory video processing (4/16/64 megabit)
  - Optical transmission (semiconductor lasers and opto-electronic ICs)
  - Video processing (CCD sensors, wafer scale video chips)

The INS Computer will merge communications and computer technologies into an image- and video-oriented system witn the potential for automated voice translation and information processing. When implemented, the INS Computer will free Japan from the constraints of alphanumeric data entry and voice communications and build on its strength in video technology.

INS Program

Figure 4

CONCEPTS OF INS COMPUTERS



Source: NTT
DATAQUEST
April 1986

Technology Transfer

The following is a list of the material in this section:

- Technology Tranfer--Conceptual Framework
- Japanese Technology Transfer Method
- Technology Transfer--Japanese Corporate Methods
- → Technology Transfer--Japanese R&D Consortia Methods

NOTE: The arrow symbol indicates the latest document's location behind this subject tab.

Technology Transfer--Conceptual Framework

INTRODUCTION

During the last few years, global competition and rapid technological development have forced governments and companies to accelerate the flow of technology from their laboratories to the marketplace. Technology transfer, once a topic of academic discussion, is now a matter of serious national and corporate debate. Dataquest observes that each region has its own set of concerns:

- North America—Retaining international competitiveness with Japan and emerging Asian nations
- Japan—Staying ahead of cost-competitive Asian countries, overcoming the "technology boycott" by Western nations, and developing its own basic research capability
- Europe—Reviving its "national champions" by organizing joint R&D projects, commercializing its technology rapidly, and retaining technological parity with Japan and the United States
- Asia—Absorbing new technologies from Japan, Europe, and the United States and moving rapidly up the technology ladder to higher-value-added products

Technology transfer has become such an important topic of national policy that the U.S. Congress, for example, passed the Technology Transfer Act of 1986, and the president issued an executive order mandating the development of technology transfer programs at all federal laboratories and universities receiving federal funds. Recently, major R&D consortia such as the Semiconductor Research Corporation (SRC), Microelectronics and Computer Technology Corporation (MCC), and Semiconductor Manufacturing Technology Corporation (SEMATECH), have initiated studies to develop technology transfer programs. Japanese companies and government projects are developing new technology transfer methods to improve their own international competitiveness.

To assist Dataquest clients, the Japanese Semiconductor Industry Service (JSIS) provides this conceptual framework and practical how-to information on Japanese technology transfer practices. For further information and discussion, JSIS clients are encouraged to use their inquiry privilege.

Technology Transfer--Conceptual Framework

DEFINITIONS

As shown in Figure 1, Dataquest uses the term "technology transfer" to describe the flow of basic scientific and applied industrial research results to marketable products and services. The following are definitions for terms used in this section:

- Technology—A learned set of technical, financial, and labor and management methods and skills employed to achieve a practical purpose
- Technology Transfer—The consciously planned acquisition, dissemination, and utilization of existing skills, techniques, or know-how to develop new products and services
  - Technology Flow—The unimpeded diffusion of technology that occurs naturally via commercial publications, programs, communications media, and human interaction
- Manufacturability—The design of a product to make it easier and cheaper to make, usually by reducing the number of parts and using simpler fabrication operations
- Commercialization—The transfer of basic scientific and applied industrial research from the laboratory to the marketplace

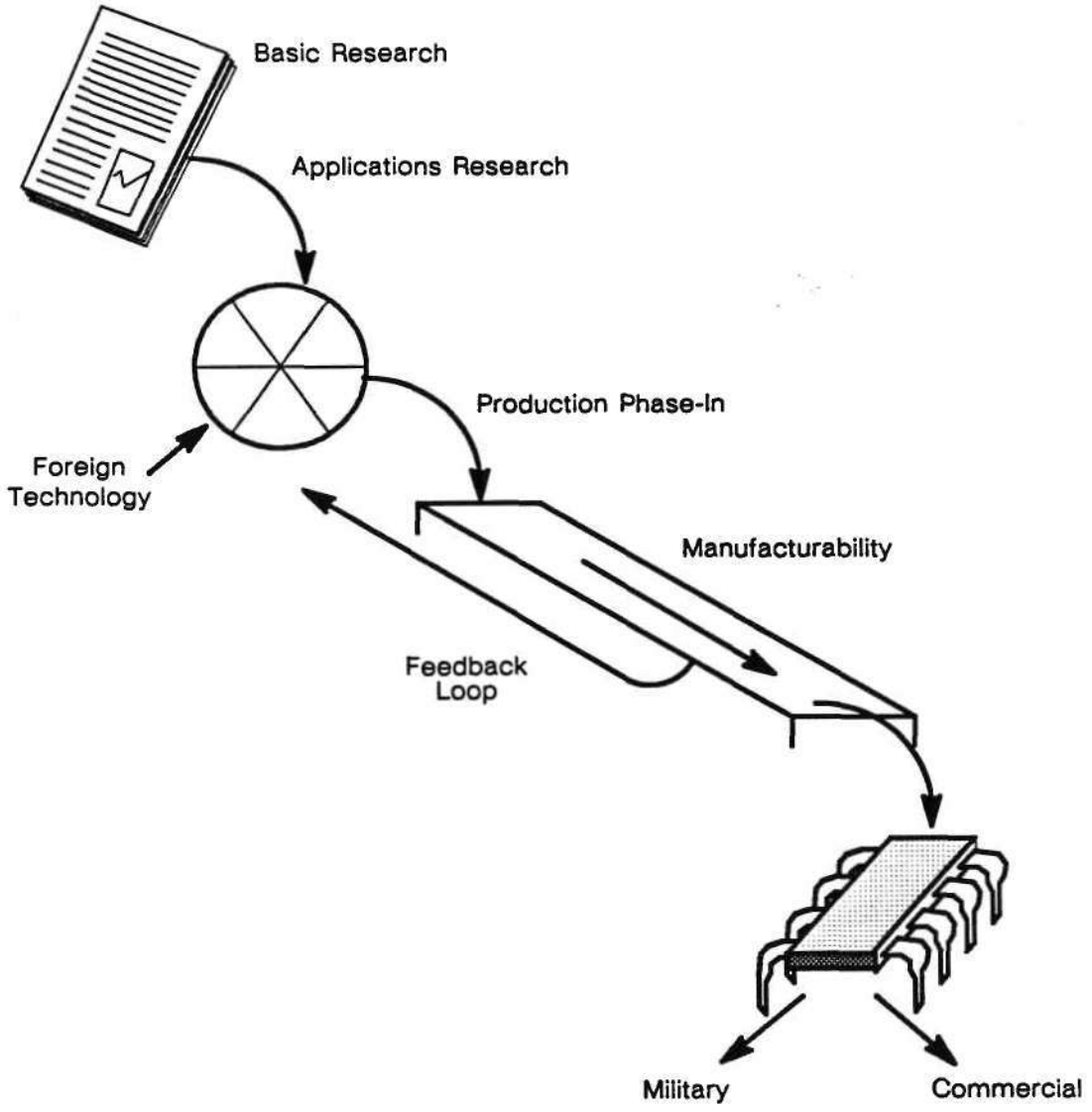
Technology is not limited to knowledge embodied in tangible products, tools, and software ("hard" artifacts), but encompasses the broader range of intangible human skills, values, and abilities surrounding that knowledge ("soft" capabilities). Consequently, technology is most effectively transferred through constant, informal, person-to-person interactions, not only through one-way transfers of paper documents, tapes, or other fixed media. Japanese companies believe that people, not paper, are the most effective carriers of technology and knowledge. They emphasize teamwork and job rotation as the primary vehicles of technology transfer.

Dataquest observes that technology is most rapidly transferred when people and organizations are highly receptive to new ideas and change. Transfers cannot be forced when the recipients are uninterested, unprepared, or unwilling (the "not invented here" syndrome). Motivation, open-mindedness, and intellectual curiosity play key roles in the technology transfer process.

Technology Transfer--Conceptual Framework

Figure 1

Technology Transfer—A Conceptual Approach



Source: Dataquest March 1988

Technology Transfer--Conceptual Framework

DRIVING FORCES BEHIND JAPAN'S TECHNOLOGY ACQUISITION MENTALITY

If motivations and attitudes are paramount, what are the major driving forces behind Japan's well-known "acquisition mentality"—its openness to gathering and adapting new ideas--and its success in rapidly transferring technology? Dataquest believes that the following factors are central to understanding Japan's commercial successes:

- Sheer economic necessity—The need to develop Japan's only natural resource—the human brain—because of overpopulation and a lack of natural resources
- Fierce domestic competition—The need to find and utilize the best technology around the world in order to survive financially in the hypercompetitive Japanese market (reflected in the "one-upsmanship mentality" of topping one's competitors to become number one, or in the college "entrance exam hell")
- Geographic isolation—The need to overcome natural barriers to the free exchange of ideas, knowledge, and technology
- Little immigration—No natural "brain gain" of new ideas and technology (unlike Europe, Asia, and the United States) due to rigid Japanese immigration laws
- "Catch-up" mentality—The compulsion to catch up in science and technology since Japan's opening to the West during the Meiji Period (1868-1911)
- Inferiority complex—The deep-seated belief that Japanese science and technology is not as advanced as Western technology (However, this is rapidly changing among Japanese researchers in areas where Japan has attained technological superiority, such as DRAMs.)
- Weak scientific base—The inadequacy of Japanese basic research facilities and funding (which the Japanese government and corporations are now trying to rectify)
- "Not-reinventing-the-wheel" mentality—The belief that Japan should focus on adopting, improving, and refining new technologies instead of wasting its limited human and financial resources and time on reinventing technologies
- Receptivity to foreign ideas—The esteem historically given to foreign ideas (but not necessarily domestic ideas) as a way to stay at the forefront of technological development
- Deep reverence for learning—The traditional belief among Japanese, based in Confucianism and Buddhism, in constantly learning and improving oneself through study

- Uniqueness myth—The widely held myth that Japanese are somehow unique and that all foreign ideas and technology must be thoroughly adapted to avoid creating serious domestic, social, economic, or political problems

- Strong national commitment—Ongoing support and encouragement from the national government, in the form of policy "visions" and national R&D projects, to strengthen Japan's scientific and technological base

- Technology "boycott" on Japan—The belief among many Japanese that foreigners are deliberately stopping or slowing the flow of technology to Japan because of the country's competitiveness (reflected in intellectual property and patent suits, and the closure of programs and laboratories to Japanese researchers)

Given these circumstances, Japanese organizations view technology transfer and rapid commercialization as critical for their economic survival. They have invested much time and money refining their technology transfer methods in the postwar era.

JAPAN IN A GLOBAL CONTEXT

Japanese technology transfer has traditionally been viewed as the importing of foreign technology by means of copying, licensing, reverse engineering, and marketing intelligence. Dataquest believes this stereotype of Japan as "copycat" is simplistic and outdated because it ignores the complex transfers of domestic technology within Japan itself. Figure 2 provides a more balanced view of Japanese technology transfers within the rapidly changing global context listed below:

- International transfers to and from Japan via foreign study missions, licensing, technology exchanges, and strategic alliances

- National R&D programs involving major corporations (san), universities (gaku), and government laboratories (kan)

- Regional transfers involving the transfer of national R&D results to regional government testing laboratories, universities, and local consortia

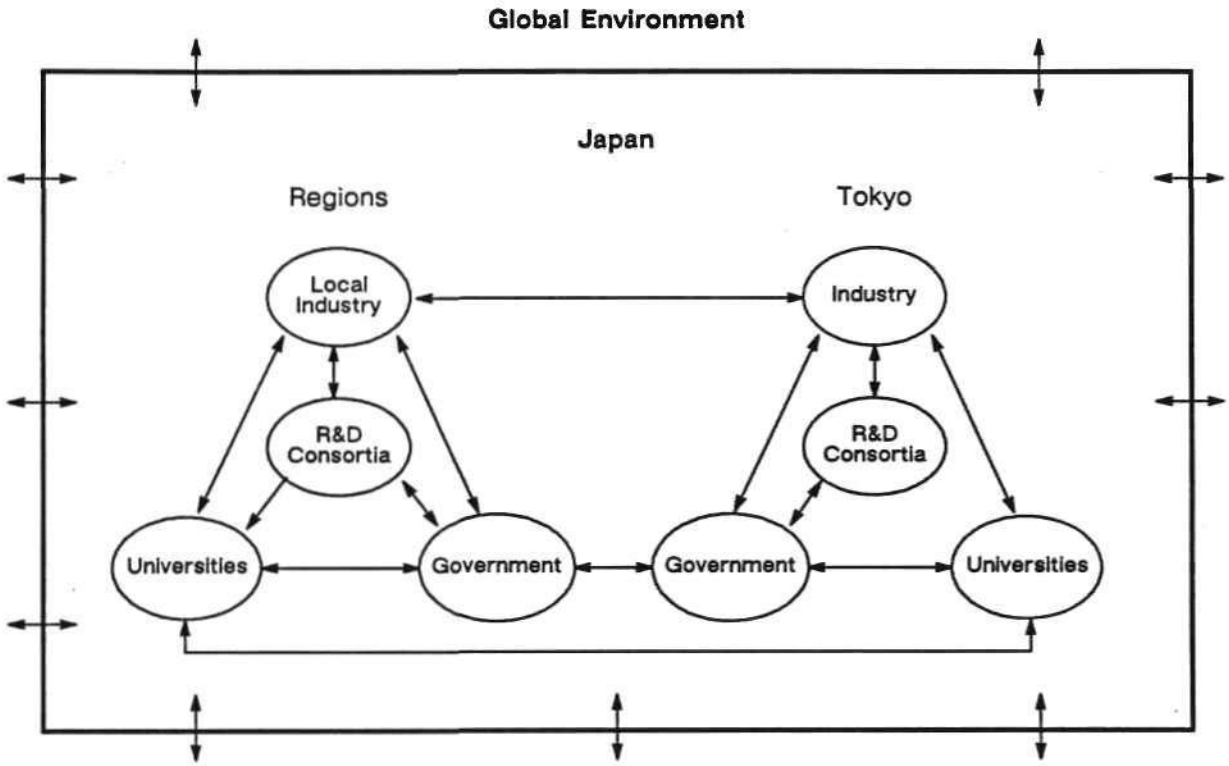
- Regional consortia involving the local government, university, and corporate researchers (the technopolis, teletopia, new media community, techno-net, and other regional programs)

- Small business development to upgrade the technological level of small and medium-size businesses

Technology Transfer--Conceptual Framework

Figure 2

Japan Technology Transfer Flows



Source: Dataquest March 1988

During the postwar era, Japan emphasized international transfers as its major source of new technology. Today, there is greater emphasis on creating a high-tech infrastructure, such as national R&D programs, regional high-tech programs, and venture business consortia, linked by an integrated information network. The Japanese government's goal is to create a "techno-state" (gijutsu rikkoku) of regional R&D centers.

As the twenty-first century approaches, Dataquest observes that Japan's focus is rapidly shifting from absorbing, copying, and improving foreign technologies to creating, cultivating, and licensing its own technologies. Creativity and innovation have become Japan's rallying cry. In this light, the Japanese technology transfer methods discussed in this section reflect Japan's previous obsession with catching up with the West. Now that Japan has attained technological parity in many fields, we believe Japanese organizations will modify these methods to encourage greater creativity and innovation.

Japanese Technology Transfer Method

OVERVIEW

Japanese are prodigious information gatherers and voracious readers, but little has been written about their specific methods of acquiring and transferring technology. Through years of experience with our Japanese semiconductor clients, Dataquest has identified technology transfer methods commonly used by Japanese organization. As shown in Table 1, these methods are listed by phase in the transfer process, but they are used flexibly throughout the process. In general, the Japanese value rapid, flexible methods that involve a high degree of interaction among multidisciplinary teams. The following is a short description of the dynamics of the Japanese technology transfer process.

Table 1

Japanese Technology Transfer Methods

Transfer Phase	Japanese Transfer Methods
Monitoring	Data base networking (technical papers and patents)
	Random global search
	Domestic and overseas sabbaticals
	Research societies (kenkyukai)
	Professional associations
	Symposiums and seminars
	Roundtable discussions (zadankai)
	"Old-boy" network (drinking, eating, golf)
Planning	Long-term industry "visions"
	Alternative scenario forecasting
	Technology trees (road mapping)
	Seeds/needs analyses
	Group brainstorming ("lotus blossom" approach)
Organizing	Informal study groups (benkyokai)
	Industry R&D associations (kenkyu kaihatsu kyokai)
	Advisory councils (zunokai)
	Parallel-track R&D groups
	National R&D projects
Acquisition	Directed global search
	Overseas study missions
	Technology licensing and bartering
	Joint ventures and R&D (strategic alliances)
	Procurement R&D and design-in

(Continued)

Japanese Technology Transfer Method

Table 1 (Continued)

Japanese Technology Transfer Methods

Transfer Phase	Japanese Transfer Methods
Dissemination	Post-trip debriefings, trip reports, and articles
	*Broad job descriptions and job rotations
	*Close R&D/plant linkage
	Intense cross-training and on-the-job training
Utilization	Spiral/feedback approach
	Generic process spin-offs
	Ad hoc new product groups
Evaluation	User feedback surveys
	In-house technology transfer analyses

*Methods not easily transferable to the United States, Europe, and Asia due to different labor practices and attitudes.

Source: Dataquest
March 1988

DYNAMICS OF THE JAPANESE TECHNOLOGY TRANSFER PROCESS

Japanese organizations transfer technology efficiently because of their global information-gathering network, their high concentration in a few cities (more than 80 percent of all researchers are located in Tokyo and Osaka), and their ability to mobilize people rapidly. Using superconductors, neural networks, and optocomputing as examples, Dataquest observes that Japanese organizations transfer technology as described in the following sections.

Monitoring Process

Worldwide developments are constantly monitored through a variety of formal and informal channels:

- Formal networks—These networks include Japan External Trade Organization (JETRO), embassy and consulate officers, trading companies, offshore R&D centers and plants, employees on overseas sabbaticals, foreign correspondents, and on-line data bases. Leading experts are contacted and visited.

Japanese Technology Transfer Methods

- Informal networks—Frequent phone calls, meetings, and evening drinking and eating with colleagues and visitors are accepted practices.

- Seminars and symposiums—Leading Japanese and foreign visitors are invited to speak on state-of-the-art developments in their fields.

Due to their massive information-gathering network, the Japanese are usually much more knowledgeable about major global developments than their foreign commercial counterparts, who tend to be highly focused and follow only developments in the West. Large Japanese organizations regularly conduct global searches for the best technologies and ideas available around the world.

Planning Process

Industry associations or advisory councils meet when an emerging trend develops, to analyze long-term scenarios, alternative options, technology road maps, and demand-supply forecasts. Broad-ranging surveys (chosa) are conducted to identify key issues, trends, and industry needs.

Organizing Process

Based on the recommendations of industry advisory councils, the Japanese government establishes national R&D projects or assigns emerging technologies to existing projects (e.g., biodevices to MITI's Future Electron Devices Project in 1987). Industry groups form new R&D associations, such as the New Glass Forum, to analyze new technologies and applications. Since 1985, the Ministry of International Trade and Industry (MITI) and the Ministry of Posts and Telecommunications (MPT) have jointly sponsored the Japan Key Technology Center, which provides seed financing to risky next-generation technologies.

Responding to Breakthroughs

When breakthroughs such as IBM Zurich's superconductor announcement are made, university research teams (e.g., under Tokyo University's Professor Shoji Tanaka), informal study groups (kenkyukai), and overseas study missions are mobilized within a few days to discuss key trends and issues, gather information, and develop research strategies. Research associations are established shortly thereafter. Government ministries jointly sponsor research centers, such as MITI's International Superconductivity Research Center.

Acquisition Process

Study missions are sent overseas repeatedly to attend key conferences (such as the optocomputing and neural net conferences in California during 1987) and visit leading research centers to determine Japan's level of competitiveness, study research trends,

and identify commercial opportunities. Companies then license, invest, or enter into strategic alliances with leading Japanese and foreign makers to market and acquire the technology (e.g., the current trend in VLSI CAD tools). Occasionally, joint ventures are pursued, such as the Toshiba–Motorola venture. Increasingly, Japanese companies are consigning basic research (itaku-kenkyu) to Japanese professors, who are assisted by employees assigned by the company.

Dissemination Process

Trip reports and articles are immediately circulated among researchers and published in industry journals within one to three months of the overseas trip. Multi-disciplinary teams are quickly formed (e.g., Mitsubishi's 220-person superconductor team) and trained on the job to investigate commercial applications. Joint R&D/plant teams determine manufacturing time frames and issues. Industrial newspapers and magazines compete to publish technical series on emerging trends. Publishers consign experts to write books, which are published within three to six months of breakthroughs. For example, there were more than 40 books in Japanese on supercomputer technologies and business by late 1987.

Utilization Process

Product champions are encouraged to form multidisciplinary teams of product and system designers, software programmers, plant operations, engineers, sales and marketing staff, and distributors to identify product opportunities, development schedules, and marketing requirements. Flexible groups of five people (the traditional (gonin-gumi) and repeated feedback loops are used until a marketable product is developed. Managers find whatever financial, technical, and marketing resources are needed to hit a "tight product window," which is usually less than three months for consumer products. (See the section below entitled "Corporate Methods" for details.)

Evaluation Process

Japanese companies constantly experiment with products and evaluate their acceptance through surveys of customers, salespeople, distributors, and subcontractors. In-house technology transfer analyses are conducted to determine the reasons for success or failure, and ways to improve the product or service.

Unlike many Western companies that drop unsuccessful products, Japanese companies often go back to the laboratory and marketing division to determine ways to improve a product. New technical and marketing approaches are developed, and the product goes through another cycle. A product can go through this process many times (sometimes as many as 20) until either the product champion quits or the product either succeeds or is dropped.

Japanese Technology Transfer Methods

The technology transfer process described above is only generic in nature, and does not reflect the numerous differences among Japanese organizations. The key point to remember is that the Japanese technology transfer process is highly flexible, dynamic, multidisciplinary, interactive, and iterative. The Japanese do not believe that perfection can be attained on the first try. Constant striving and improvements (kaizen) are essential to successfully transferring and commercializing any technology. Indeed, problems and setbacks are viewed as opportunities. In the hotly competitive Japanese market, this dogged perseverance in the face of adversity is crucial for corporate survival. It can be summed up in a popular Japanese saying: "Knocked down seven times, back up eight times."

JAPANESE TECHNOLOGY TRANSFER METHODS

The preceding section describes the dynamics of the Japanese technology transfer process; this section describes the actual transfer methods used by Japanese organizations, as listed in Table 1.

Monitoring Methods

Data Base Networking

The Japanese government and industry associations are jointly developing on-line data bases for technical papers and patents. Regional technology centers are being linked to these on-line data bases. Major semiconductor makers maintain in-house patent monitoring divisions staffed by technical and legally trained experts. Overseas Japanese electronics and trading companies maintain instantaneous monitoring using modems, fax machines, telex, telephones, and on-line data bases.

Random Global Search

Japanese organizations continually send study mission overseas to conferences, trade shows, government agencies, universities, and other key sources to glean valuable bits of information not available in the press. Generally, these exploratory investigations are open-ended and conducted during planned business trips. Often, the Japanese have no preconceived goal or interest in mind but are "just looking around."

Domestic and Overseas Sabbaticals

Major organizations send promising young researchers to Japanese or foreign universities for one to three years to monitor the environment and research an emerging field. Usually, they are enrolled in graduate programs or assigned to a professor familiar with the organization.

Japanese Technology Transfer Methods

Research Societies

Being group-oriented, Japanese researchers often form small study groups (benkyokai), research societies (kenkyukai), or academic societies (gakkai) to discuss issues and trends with colleagues. These groups meet frequently to exchange papers and publish their own journals.

Professional Associations

Japanese traditionally identify themselves as members of companies, not professions. However, this is changing among younger engineers and software programmers (e.g., UNIX programmers) who are more independent and share the latest developments.

Symposiums and Seminars

Japanese organizations are always sponsoring symposiums and roundtable discussions (zadankai) to discuss the latest trends and developments. Many of these are covered by the news media and published in trade journals.

"Old-Boy" Network

Probably the fastest way to learn about any new development in Japan is to eat, drink, or play golf with Japanese friends and colleagues. The Japanese "grapevine" is extremely efficient. As the saying goes: "There are no secrets in Tokyo." Once you have established a long-term relationship, Japanese managers are surprisingly frank and open.

Planning Methods

Long-Term Industry Visions

Japanese ministries, especially MITI, frequently develop long-term industry goals and forecasts in collaboration with industry, academia, labor, and the media. These visions are rallying points for cooperative research and government funding, but have no legal force.

Alternative Scenarios

Japanese organizations routinely examine the relative merits/demerits, tradeoffs, costs, and requirements of alternative industry scenarios in their planning. Analyses of these situations are used to identify the critical technologies to develop or acquire (e.g., memory chips in the late 1970s).

Japanese Technology Transfer Methods

Technology Trees

Alternative technology paths frequently are depicted graphically through the use of technology trees, which show the evolution of new processes, applications, and market opportunities (e.g., telecommunication technologies). These are similar to technology "road maps," but tend to be less directional and more evolutionary in approach.

Seeds/Needs Analyses

Due to their concern for commercial markets, Japanese organizations temper their forecasting of technology "seeds" with market "needs" analyses, which often uncover new market opportunities. Plant managers request in-house economics teams to conduct these analyses before committing any fab investments.

Group Brainstorming

Japanese believe that "two heads are better than one." Groups often sit around, especially in the evening, dreaming up new products, applications, and market strategies. The Japan Productivity Center uses a "lotus blossom" format to encourage divergent thinking; in these sessions, new applications are considered for "seed" products or technologies.

Organizing Methods

Informal Study Groups

Unlike ongoing research societies, ad hoc study group (benkyokai) are quickly formed whenever a new trend or development emerges. These groups usually are centered around the "old-boy" network of research colleagues, drinking partners, and former college classmates.

Industry R&D Associations

When MITI advisory councils identify a new technology trend, quasi-public industry R&D associations (kenkyu kaihatsu kyokai or kenkyukai) are established to conduct surveys (chosa), analyze trends, prepare forecasts, and conduct joint research with research laboratories. Recent groups include:

- Next-Generation Automotive Information Systems Project (third quarter 1987)
- Japan Optomechatronics Association (second quarter 1987)
- Optical Memory Card R&D Consortium (second quarter 1987)
- New Glass Forum (first quarter 1987)

Japanese Technology Transfer Methods

Advisory Councils

MITI and other government ministries usually seek expert advice on emerging trends from industry, university, labor, and media sources through advisory councils (zunokai). These opinion leaders carry significant clout and influence the direction of government funding and R&D associations. MITI's Technopolis '90 Committee is an example of this type of council.

Parallel-Track R&D Groups

Given their competitiveness and risk aversion, Japanese organizations often create competing parallel-track R&D groups to avoid running into technological dead ends. MITI's Fifth Generation Computer Project and its Supercomputer Project, for example, are both working on parallel processing architectures. However, the most heated competition is between companies, and between MITI and NTT laboratories. Despite the competition, the groups usually participate in each other's seminars and meetings to exchange ideas and papers.

National R&D Projects

Probably the favorite method for transferring technology is government sponsorship of joint R&D projects, such as MITI's Future Electron Devices Project. These projects are necessary to break down the normal barriers between competing companies. To encourage cooperation, these projects usually focus on generic technologies that are three years or more from commercialization. Dataquest has identified more than 30 semiconductor-related R&D projects.

Acquisition Methods

Directed Global Search

Once a technology is identified or a breakthrough occurs, Japanese organizations send teams to local universities and government laboratories and send study teams overseas to attend conferences, companies, universities, and national laboratories. Repeated visits to different leading centers are made until the Japanese feel they understand the technology.

Overseas Study Missions

Unlike in the West, where overseas trips are considered luxuries, Japanese organizations believe that study missions are essential to maintain technological parity. These groups usually consist of R&D association members who are focused on a specific area, such as neural nets or optocomputing.

Japanese Technology Transfer Methods

Technology Licensing and Bartering

In the past, Japanese semiconductor companies acquired much of their technology through one-way licensing agreements. As their technological level rises and foreign companies become reluctant to share their technology, Japanese companies are beginning to trade their technology with partners, such as the December 1987 agreement signed by NMB Semiconductor and Alliance Semiconductor for 1Mb DRAMs. Dataquest believes that bartering will become a major transfer method in the future.

Joint Ventures and Joint R&D

For technical and political reasons, more Japanese companies are entering joint ventures with foreign companies to exchange technology, such as the Toshiba-Motorola venture and the Matsushita-SAE Systems joint research on 64-bit MPUs. Dataquest observes a rapid increase in these types of alliances. (See the section entitled "Strategic Alliances" for future information on this subject.)

Procurement Research and Design-In

As large vertically integrated companies, Japanese companies regularly use components procurement as a way to uncover competitor strengths, secure new technologies, and direct supplier investments. Through their qualification process, Japanese companies usually investigate the manufacturing capabilities of their suppliers and transmit the information to their components divisions. Thus, procurement is a major source of competitive information.

Dissemination Methods

Debriefings and Trip Reports

Japanese researchers are trained to brief their colleagues and write detailed trip reports on significant developments observed. For overseas study missions, these notes are published in soft-cover reports with macroeconomic data, business trend analysis, and summaries of group discussions and conclusions. Major trend analyses are often published in monthly industry journals (Electronics and Denshi Kogyo Geppo, or Electronics Industry Monthly).

Broad Job Descriptions/Job Rotations

Japanese organizations value well-rounded generalists who are flexible, easy to train, and cooperative team players. Unlike U.S. companies, which seek highly-trained specialists and rely heavily on paper documents, large Japanese semiconductor companies rotate their engineers (shanai koryu or internal transfer) to transfer know-how from division to division. (For a detailed description of this process, see the section entitled "Corporate Methods.")

Japanese Technology Transfer Methods

Close R&D/Plant Linkage

Given their emphasis on manufacturing, Japanese semiconductor companies locate their R&D centers near their fab lines and encourage flexible, free-flowing, and constant informal communication between R&D and manufacturing. Production engineers are gradually phased into new product development from the beginning. (See "Corporate Methods" for more details.)

Intense Cross-Training and On-the-Job Training

Since Japanese semiconductor engineers receive theoretical training in college, companies provide highly structured on-the-job training during the first few years under the guidance of senior engineers. Engineers are also expected to master all aspects of their job, not just design or marketing. This cross-training enables Japanese companies to transfer their "corporate memory" throughout the company.

Utilization Methods

Spiral/Feedback Loop

A key method used by Japanese companies is to recycle product failures back to R&D, manufacturing, and marketing for new ideas and constant improvements. Product champions are selected (or volunteer) to take products from R&D to sales and distribution. Product teams are assigned to the product and withdrawn as needed during the development cycle. (See "Corporate Methods" for more details.)

Generic Process Spin-Offs

Based on the concept of technology trees or road maps, Japanese companies emphasize control over process evolution, which is viewed as an ongoing source of spin-off products and services. This process orientation ensures product continuity and enables Japanese companies to develop products quickly.

New Product Groups

New product development groups of three to five employees often meet informally to identify and discuss commercial applications for acquired technologies. Unlike the earlier planning and organizing groups, these groups incorporate ideas gathered while developing another product (adaptive R&D). If the plant manager approves their product plan, this group often champions the product to marketing distribution.

Japanese Technology Transfer Methods

Evaluation Methods

User Feedback Surveys

Japanese companies constantly conduct surveys with internal user divisions and outside customers to refine and improve their products. These surveys are not just product evaluations. Much technology and many ideas about potential areas of research are uncovered during this process.

In-House Technology Transfer Analyses

Major Japanese companies conduct in-house evaluations of product success and failures to identify areas of improvement. Frequently, these evaluations will identify necessary research or synergies with existing technologies (fusion or hybrid technologies). Japanese groups usually accept responsibility for failures, and tend to view problems as challenges and opportunities. (See "Corporate Methods" for details.)

Technology Transfer--Japanese Corporate Methods

OVERVIEW

Japanese companies are renowned for their ability to rapidly transfer new technologies into marketable products and services. How do they accomplish this process so efficiently? What popular methods are used by leading Japanese semiconductor companies? To answer these questions, Dataquest interviewed managers at the top three worldwide semiconductor companies: NEC, Toshiba, and Hitachi, with 1987 semiconductor revenue of $3.2 billion, $2.9 billion, and $2.8 billion, respectively. This section summarizes our findings with analyses of the following topics:

- Corporate philosophy
- Corporate organization
- Technology acquisition
- Internal communication
- Personnel training and job rotation
- Factory-centered product development
- Product development process
- Case study: Toshiba's laptop personal computer

Although each company has a distinct corporate style of its own, we observed common methods used by all three companies. The following section attempts to distill these methods.

CORPORATE PHILOSOPHY

Corporate philosophy plays a very important role in Japanese companies because of their commitment to building high-quality products and to employee teamwork. In our interviews, each company emphasized a different aspect of technology transfer. Hitachi managers mentioned factory-centered product planning, whereas Toshiba seeks constant product feedback and refinement and NEC places a high priority on strong horizontal communication among employees. Despite their differences, the three companies share a philosophy about technology transfer that encompasses the following areas and principles:

- Monitoring and acquisition
  - Constantly survey global markets for emerging technologies, applications, and market needs

Technology Transfer--Japanese Corporate Methods

- Seek and develop the best technology in the world (technology "seeds")
- Pursue related technologies that can be combined to develop totally new technologies and products (fusion technologies)

- Product development
  - Adapt new technologies to meet specific market needs (seeds/needs analysis)
  - Get new products to the market quickly (three- to six-month market window)
  - Be flexible; do not analyze a product to death or expect perfection the first time
  - Constantly improve (kaizen) products and their underlying technology and manufacturing processes, which are always seen as imperfect or unfinished (mikansei)
  - Encourage teams of frontline workers to champion new product ideas and provide adequate corporate support
  - Promote cross-fertilization of ideas by rotating people (internal transfers or shanai koryu) and involving multidisciplinary teams at different phases of the product development cycle
  - Fund research at universities, corporate R&D centers, or national laboratories to develop new product technologies (itakuhi-kenkyu)

- Manufacturing
  - Involve factory engineers from the beginning to improve product manufacturability and reduce production costs
  - Encourage constant communication among marketing, research, and the factory during the manufacturing process; if possible, locate these functions nearby or at the plant
  - Give manufacturing managers the power to decide on product plans and to cancel unmanufacturable or unmarketable products
  - Set zero-defect goals and determine manufacturing improvements required to meet those goals
  - Run pilot R&D lines separate from main production lines to qualify new processes and products; allow production engineers to try new ideas during slack periods

Technology Transfer--Japanese Corporate Methods

- Marketing and distribution
  - Rotate engineers through marketing and distribution to acquire "a feel for the market"
  - Solicit feedback from customers, marketing divisions, and distributors and quickly incorporate their suggestions into new products
  - Provide strong after-sales service as a vehicle for hands-on marketing research
- Overall management
  - Keep management interference to a minimum (Managers should build harmony and teamwork by orchestrating, not controlling, people.)
  - Build teamwork by rewarding groups, not individuals, for product successes
  - Train generalists who have a broad understanding of research, manufacturing, sales, and marketing
  - Rotate employees and build multidisciplinary product teams (Technology is best transferred by people, not paper.)
  - Do not be afraid of making mistakes—rather, learn from errors and failures; apply those lessons in succeeding efforts
  - Persevere despite short-term setbacks and failures

Dataquest believes that the application of these principles is largely responsible for the Japanese companies' effectiveness in transferring technology quickly to the marketplace. This approach is not specific to Japanese companies, but is practiced by leading semiconductor companies worldwide. However, top Japanese semiconductor companies are particularly adept at implementing these principles on a daily basis.

Table 1 summarizes the major differences in management philosophy that Dataquest observes between top U.S. and Japanese semiconductor companies. The U.S. approach is particularly effective for developing highly sophisticated semiconductors, whereas the Japanese approach is efficient for developing manufacturable devices quickly.

In short, the Japanese corporate philosophy regarding technology transfer can be summarized in a few words: commitment, curiosity, open-mindedness, hard work, perseverance, constant improvements (kaizen), teamwork, and total dedication to excellent quality, service, and customer needs.

Technology Transfer--Japanese Corporate Methods

Table 1

United States–Japan Comparison of Semiconductor Company Management Approaches

United States	Japan
Research-oriented	Manufacturing-oriented
Rigid specialists	Rotating generalists
Not-invented-here (NIH) syndrome	Global search
R&D/fab gap	Integrated R&D/fab/sales
Linear development	Feedback approach
Sophisticated designs	Manufacturable designs
Short-term, bottom-line orientation	Long-term, manufacturing-refinement orientation
Document transfers	People transfers

Source: Dataquest
March 1988

CORPORATE ORGANIZATION

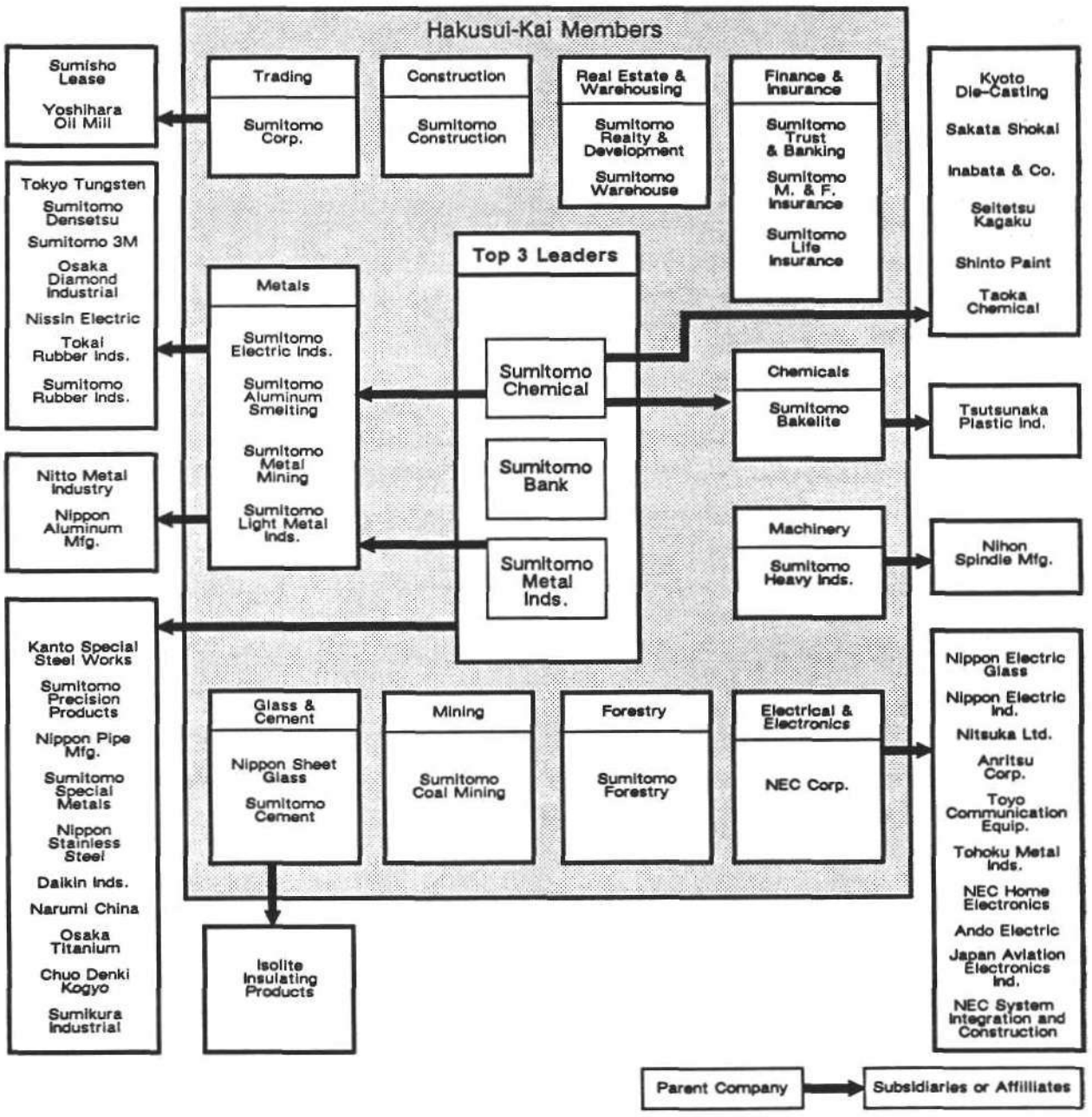
Top Japanese semiconductor companies can take advantage of their organizations to rapidly transfer technology. First, they are vertically integrated companies related to larger industrial groups (keiretsu). An example of this type of relationship is NEC's position in the Sumitomo Group, as depicted in Figure 1. This vertical integration enables these companies to:

- Obtain long-term bank financing to develop risky technologies and products ("patient money")
- Share new technologies with related keiretsu companies
- Jointly develop semiconductors with system designers from their captive users
- Leverage the research, product development, marketing, and distribution capabilities of other affiliates

Second, Japanese semiconductor companies conduct much of their research at the factory level. As shown in Figure 2, applied R&D centers are located at the plant site or nearby to promote a constant exchange of ideas and technology. In contrast, many U.S. and European companies locate their R&D centers and production lines far apart, thereby inhibiting communication and smooth technology transfers. Geographical separation also contributes to an adversarial "we versus they" attitude. However, as Japanese companies globalize their operations, we believe that they will encounter a similar R&D/fab gap. Several Japanese semiconductor companies are already opening R&D centers offshore near their plant sites to tailor products to the local market and analyze customer feedback.

Figure 1

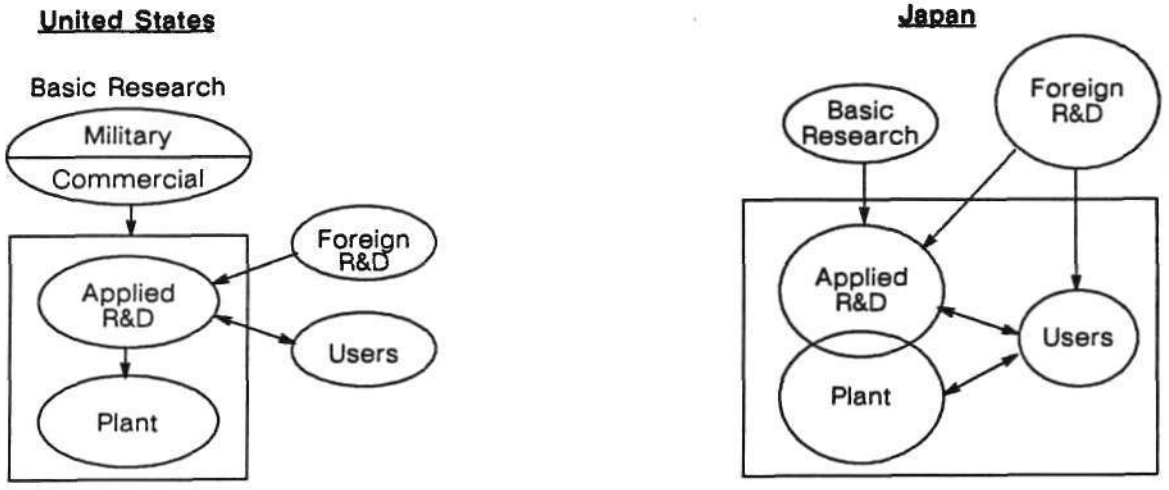
Sumitomo Group



Source: Industrial Groupings in Japan 1986/1987
Dodwell Marketing Consultants
Dataquest
March 1988

Figure 2

U.S.-Japan Comparison of Corporate Technology Transfer



Source: Dataquest March 1988

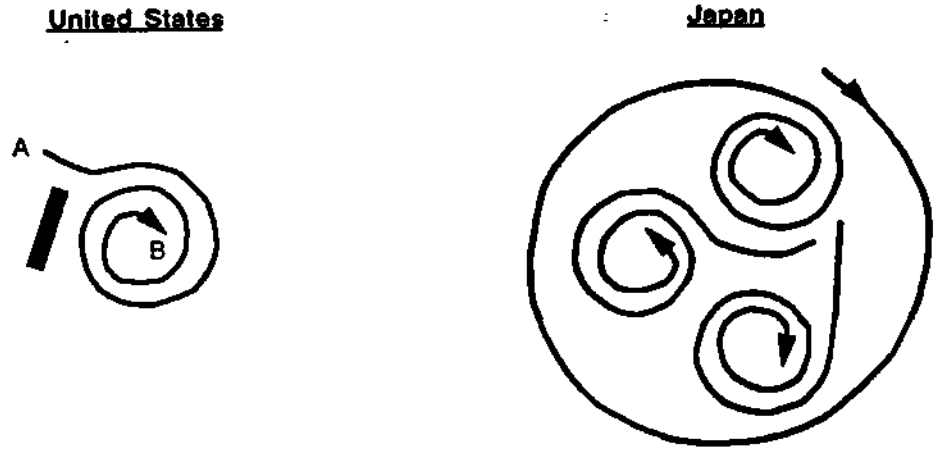
TECHNOLOGY ACQUISITION

Japanese companies gather information in a way that is very different from the methods of most U.S. or European companies. As shown in Figure 3, U.S. companies often have specific product goals in mind when they gather information. Their search tends to be narrow and highly focused, making them vulnerable to being blindsided, as in the case of the well-known VLSI project.

In contrast, Japanese semiconductor companies usually conduct a global search to identify emerging markets and technologies. Their approach is often random, indirect, and exploratory in nature, making it costly and time-consuming. However, once an opportunity is identified, these companies quickly mobilize people and assign them to promising areas. Not only do they avoid being blindsided, but they often uncover various technologies that can be combined into a new product. Large, well-financed U.S. and European companies are similar to their Japanese counterparts, but are usually not as exhaustive in their global searches. Japanese companies leave few stones unturned.

Figure 3

U.S.–Japan Comparison of Corporate Technology Search Approaches



Source: Dataquest March 1988

INTERNAL COMMUNICATION

Top Japanese semiconductor companies are organized for very flexible communication. As shown in Table 2 and Figure 4, large U.S. semiconductor companies tend to be paramilitary command-style organizations in which managers exert strong control over internal communication and decision making. Aggressive, domineering managers are highly valued. Jobs are specialized, and communication between research and manufacturing must go through the proper channels—usually the managers. Because of employee turnover and rigid job definitions, technology transfers must be formalized and documented. Engineers are discouraged from straying from their areas of expertise. As a result, this top–down, compartmentalized structure slows down technology transfers.

In contrast, top Japanese semiconductor companies are fluid network organizations in which teams of employees are encouraged to consult employees in other corporate divisions to resolve problems before they occur. Informal, ad hoc communication is highly valued and encouraged through open offices, frequent meetings, R&D at the plant site, and evenings out together.

Technology Transfer--Japanese Corporate Methods

According to NEC's Dr. Hiroe Osafune, the ideal Japanese manager is "invisible." He is deeply knowledgeable about all aspects of the company but does not second-guess his team. His role is to build company harmony and orchestrate the activities among teams. This bottom-up approach to management allows Japanese employees to solve problems quickly and efficiently.

Table 2

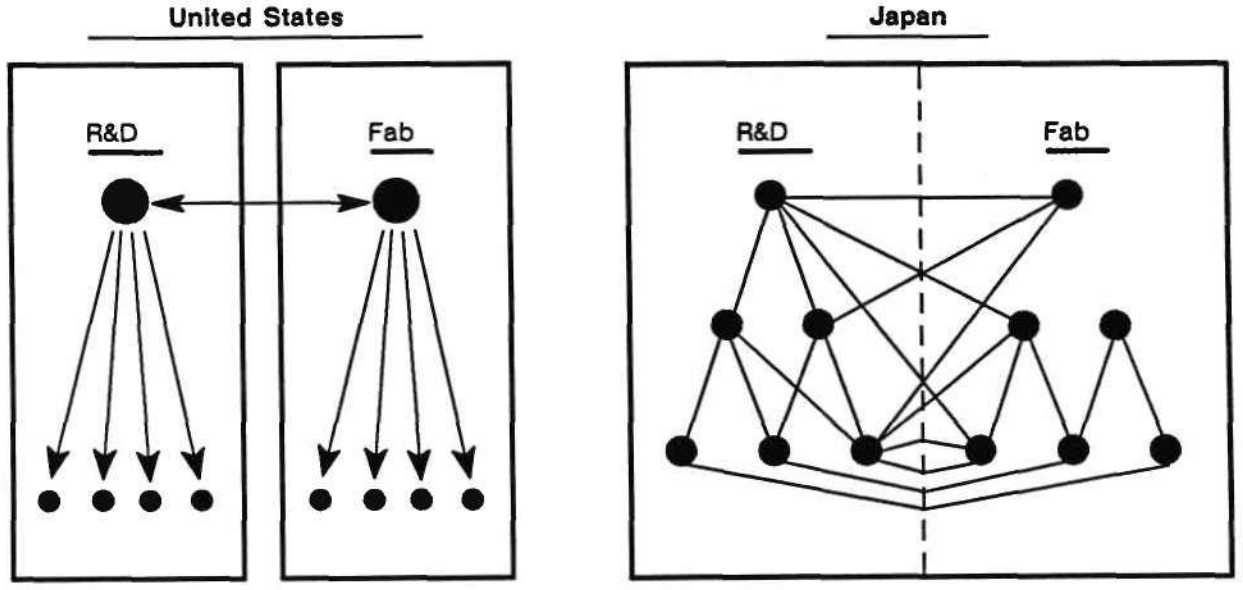
U.S.-Japan Comparison of Internal Communication in Large Semiconductor Companies

United States	Japan
Formal	Informal
Top-down command	Bottom-up
Job specialization	Job rotation
Command-style communication	Multilevel communication
Document transfers	Discussions

Source: Dataquest
March 1988

Figure 4

U.S.-Japan Comparison of Internal Communication in Large Semiconductor Companies



Source: Dataquest March 1988

PERSONNEL TRAINING AND JOB ROTATION

Top Japanese semiconductor companies believe that technology is best transferred by people, not paper documents. They emphasize training and job rotation as vehicles for upgrading and transferring their technology base. Their goal is to train well-rounded employees who are knowledgeable about all aspects of their business. Although some employees may specialize in a particular field, they rarely rise to top management levels. Unlike U.S. executives, who usually have research or marketing backgrounds, all Japanese semiconductor executives have manufacturing experience. Thus, these Japanese semiconductor executives are attuned to product development and manufacturability.

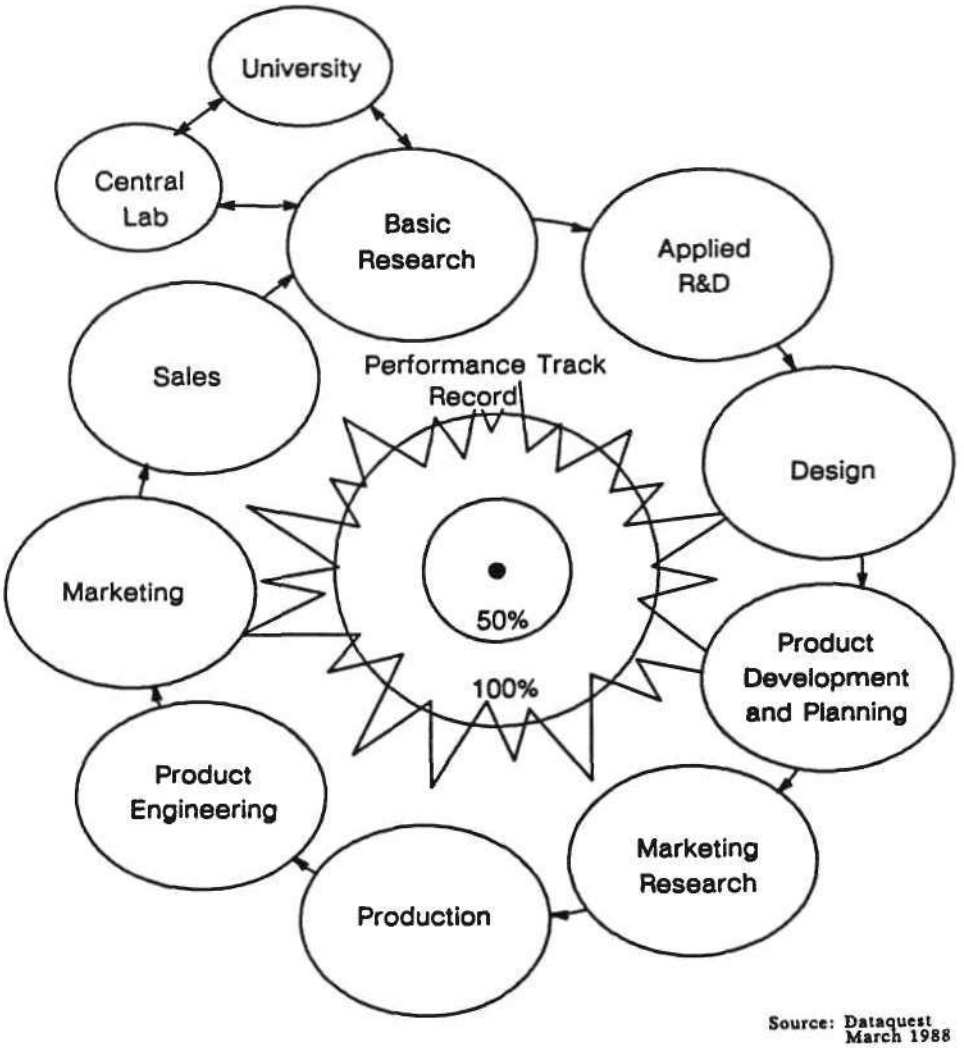
Technology Transfer--Japanese Corporate Methods

The following job-rotation approaches are commonly used by top Japanese semiconductor companies to transfer technology:

- Career development consisting of two- to three-year assignments through different divisions, as shown in Figure 5
- Short-term assignments to assist other divisions in developing products
- Assignments to follow a product from basic research, to sales and distribution, then back to research to make product refinements
- Two- to three-year sabbaticals to Japanese or foreign universities to conduct basic research

Figure 5

Japanese Job-Rotation Approach



Source: Dataquest March 1988

FACTORY-CENTERED PRODUCT DEVELOPMENT

Japanese semiconductor product development is much more factory-centered than U.S. or European approaches. As shown in Figure 6, the Japanese semiconductor plant is the key profit/loss (P/L) center, where the responsibility for product development lies with business units (sekkei-bu). The Japanese plant manager is responsible for the following:

- Deciding research targets and funding levels for products manufactured at the plant
- Conducting seeds/needs analyses in cooperation with other corporate research centers (kenkyujo) and research societies (gakkai)
- Providing consignment funding (itakuhi) to university professors for theoretical and experimental research
- Preparing a long-range plan (kacho-kessai) and semiannual plant production forecasts of major products to be manufactured
- Approving product development plans
- Funding internal production evaluation (recommendation system, or hyosho seido)
- Ensuring smooth cooperation among the plant divisions and outside groups

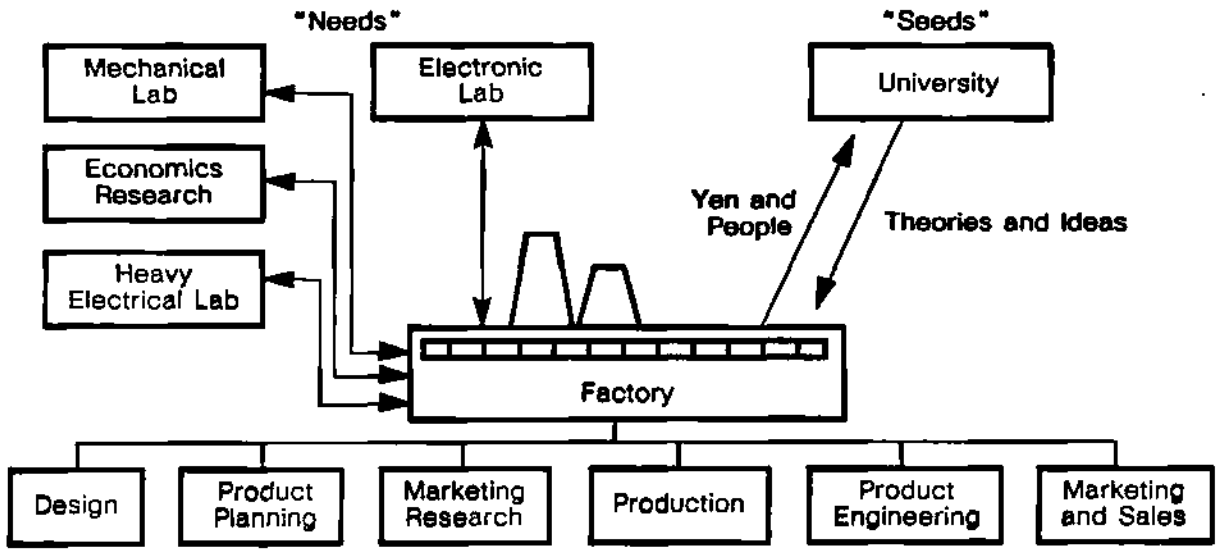
Product development plans are decided in the following two ways:

- For major products that require special research (tokubetsu kenkyu) funding, plant meetings are conducted twice a year. Decisions are made by the plant manager and his business unit.
- For current projects for less ambitious products, plant meetings are held frequently, but they are not often scheduled. Product decisions are made by the plant manager.

Within the factory, the product planning group usually has the most power over new product development. It recommends research directions, prepares product development plans, and negotiates the plans with the plant manager and his business units. By investing so much decision-making power and profit responsibility at the plant level, Japanese semiconductor plant managers are very concerned about manufacturability and rapid product development. If a product is poorly designed or unmarketable, plant revenue and employee bonuses suffer, providing a strong incentive for cooperation and market responsiveness.

Figure 6

Japanese Plant-Level Technology Transfer



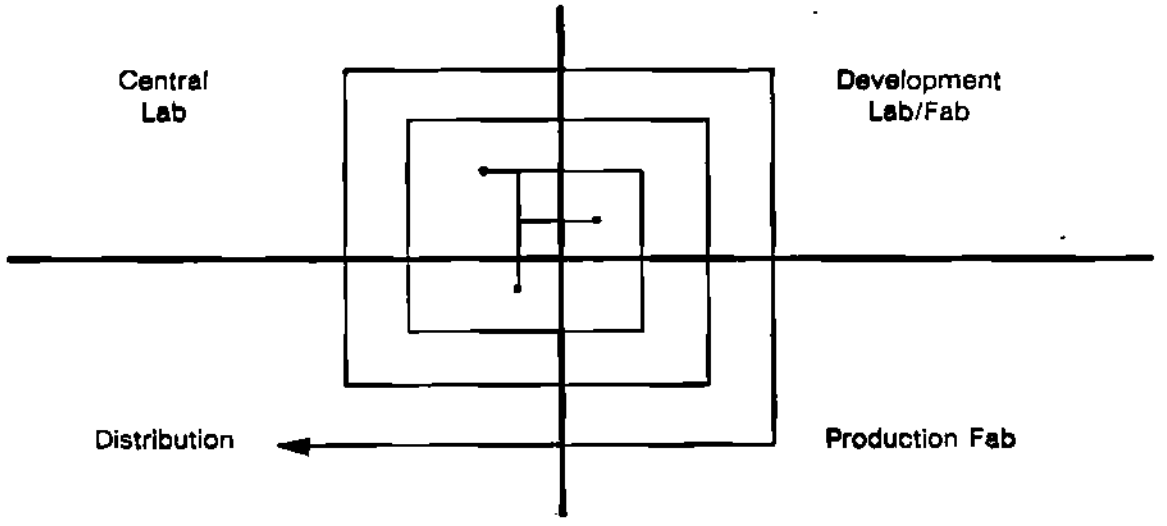
Source: Dataquest March 1988

PRODUCT DEVELOPMENT PROCESS

How do Japanese semiconductor companies incorporate new technologies into products and services so quickly? How do they manage the product development process? Based on our discussions with NEC, Hitachi, and Toshiba, we have observed that Japanese semiconductor companies view product development as a cyclical feedback process. As shown in Figure 7, Toshiba uses a spiral approach in which new products are refined through numerous feedback loops. All three companies emphasize that new product ideas emerge from all areas of the company, not just research. In fact, many of the best ideas come from manufacturing, sales, marketing, and distributors. Moreover, new products are never finished (mikansei), but are constantly improved (kaizen).

Figure 7

Japanese Spiral Approach



Source: Dataquest March 1988

The following paragraphs provide a generic description of the Japanese product development cycle based on the methods of NEC, Toshiba, and Hitachi.

Product Planning

The spiral approach is implemented in the following way:

- An employee or group conceives a new product idea and forms an informal study group (benkyokai) to sketch out a plan. The initial investigation covers the following:
  - Market needs
  - Technology requirements
  - Initial product designs
  - Market size and growth forecasts
- The team members survey other divisions to identify their interest and receptiveness, and to acquire technology, ideas, or resources for the new product.

- The team coordinator submits the product development proposal to the plant manager or product planning manager who reviews and approves or disapproves. If rejected, the team revises the proposal and resubmits.

Product Development

Product development takes place as follows:

- If approved, the plant manager or development planning manager assigns employees with the required skills or knowledge to the development team. Employees are rotated through the team as needed. Other corporate divisions are involved as follows:
  - Corporate research centers provide the required basic and applied technologies and seeds/needs analysis.
  - Plant engineers offer ideas to improve manufacturability of the product.
- The overseeing manager allocates funds for consignment research (itaku-kenkyu) by university professors or corporate research centers. This research is jointly conducted with the product team.
- Production engineers are gradually phased into the product development team from the beginning (see Figure 8) to ensure manufacturability, prepare production schedules, and transfer know-how from the outgoing engineers.
  - Product engineering varies in length from two months for simple products to four years for complex systems. Products are often routed back through research and marketing for refinement.

Manufacturing

At the manufacturing stage, the following steps occur:

- Prototype products are test-manufactured on a pilot production line to eliminate design and process flaws. Samples are test-marketed with other company (captive) divisions and major accounts. If serious problems are encountered, the product goes back to product development or applied research.
- If test manufacturing goes well, the plant manager works with the product development team and plant business units to prepare a production schedule.
- Product design engineers are gradually replaced by production engineers, who are trained thoroughly about the product by the outgoing design engineers. The companies conduct intensive training, rather than just provide a handoff of product specifications. This is a key technology transfer point in Japanese manufacturing.

- Sales and marketing engineers are gradually phased into the product development team to coordinate marketing and production schedules.

- Production is gradually ramped up. If the product sells well, the plant manager and his business units allocate more funding for progressively larger-scale production.

Marketing and Distribution

Marketing and distribution involve the following:

- The plant manager and his business units coordinate product marketing with corporate marketing divisions and distributors. Delivery schedules and pricing are negotiated.

- Members of the product development team work with marketing, sales, and distribution teams to conduct user surveys (chosa) to identify product flaws and areas for refinement (kaizen). Ideas for new products or applications are conveyed back to the plant.

- Product refinements or new product ideas are proposed by the development team as follow-on products in a product series.

In this process, Dataquest believes that the key to Japan's success in technology transfer is the gradual phase-in of production engineers from the beginning of product development, as shown in Figure 8. Their presence enables Japanese semiconductor makers to accomplish the following:

- Ensure the manufacturability of new products and, thus, reduce production costs

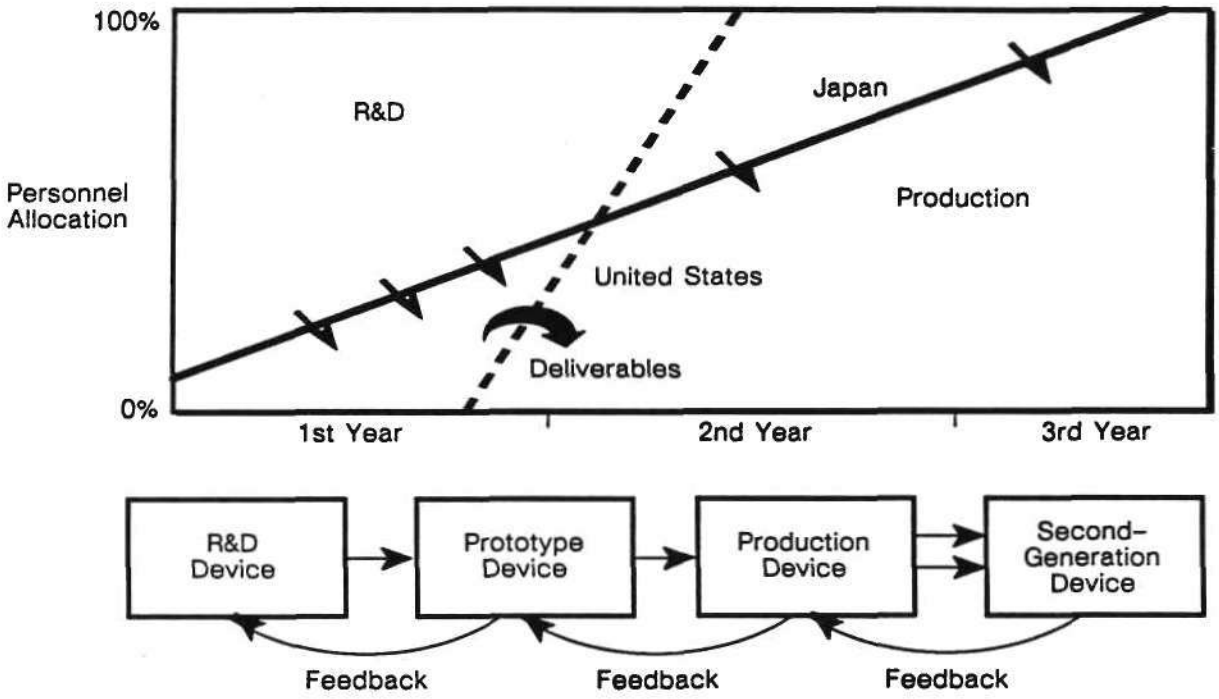
- Transfer know-how efficiently from the outgoing product designers to incoming manufacturing engineers

- Reduce the amount of paperwork and time required to transfer product technologies

- Smooth the transition from product development to manufacturing

Figure 8

Japanese Production Phase-in Approach



Source: Dataquest March 1988

CASE STUDY: TOSHIBA'S LAPTOP PERSONAL COMPUTER

An example of successful Japanese technology transfer is Toshiba's first word processor (now the Toshiba laptop PC), which was developed in the early 1980s. As shown in Figure 9, Toshiba uses the spiral approach to evaluate new product successes and failures. In this case, Toshiba's word processor was developed through the following process:

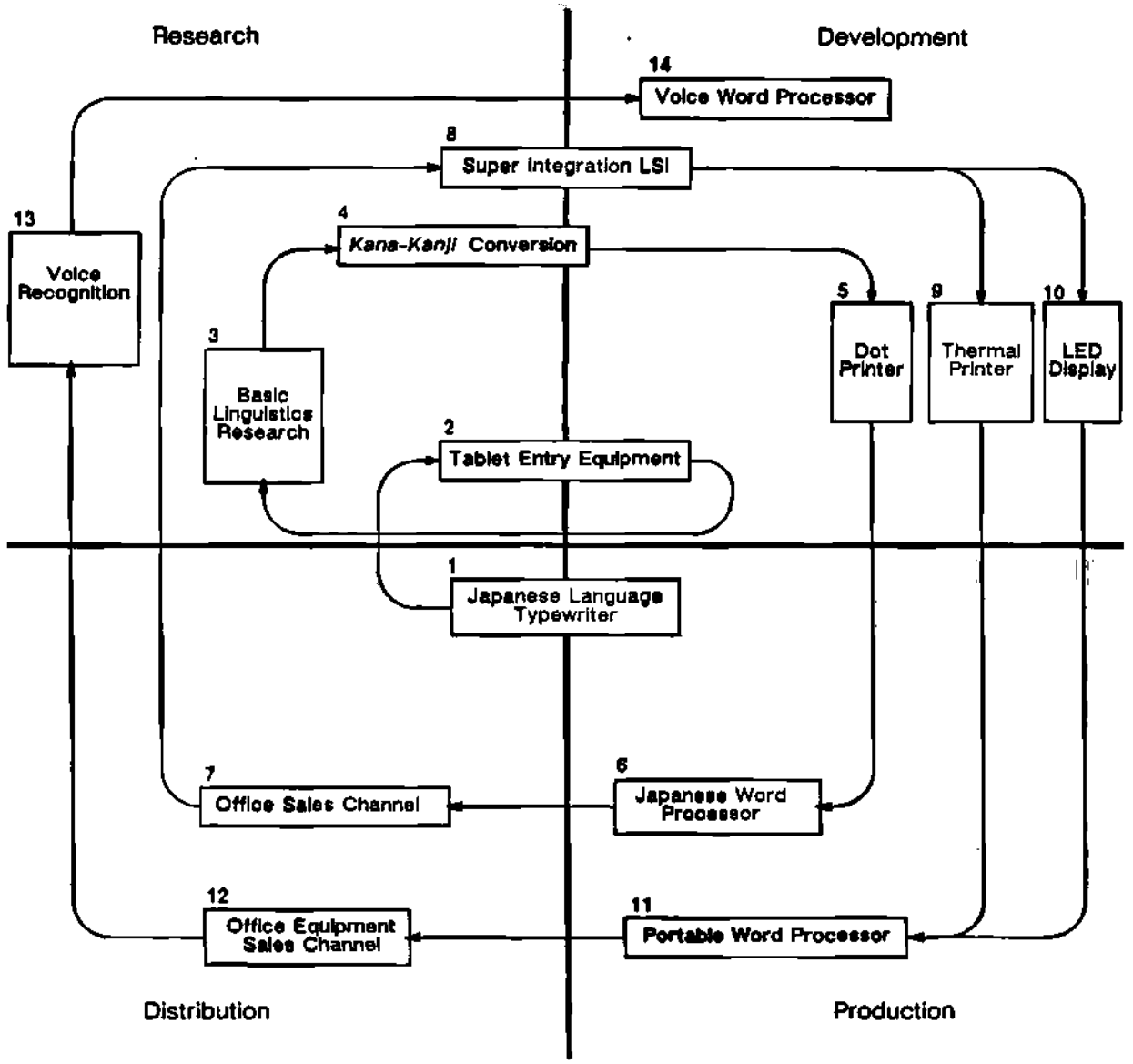
- The need for a Japanese-language word processor capable of handling 3,000 Japanese characters (kanji and kana) was identified.
- The first tablet-method input method was developed in 1968, but it failed to meet market needs.

Technology Transfer--Japanese Corporate Methods

- Toshiba assigned a researcher to a Japanese university to conduct basic linguistics research.
- Toshiba informally funded under-the-table research on kana-kanji conversion methods for 10 years.
- The development of the dot matrix printer in 1978 made Japanese word processors feasible.
- Toshiba developed a Japanese word processor that automatically converted phonetic kana letters into ideographic kanji characters.
- Based on sales in the office distribution channels, Toshiba decided to quickly develop LSIs to meet market demand for smaller, lighter word processors.
- Progress in VLSI manufacturing technology during the early 1980s stimulated research for smaller word processors.
- Thermal printers were developed, making small word processors practical in the office.
- Second-generation LCD displays were developed.
- Portable word processors were developed using VLSI chips, thermal printers, and LCD displays. Because of reduced costs and size, word processors became popular in the office and home.
- Toshiba sold its portable word processor through the office equipment and home appliance distribution channels, capturing sales in this rapidly growing market.
- However, Toshiba does not consider its technical innovation to be complete. The company currently is developing basic voice recognition technology.
- In the future, Toshiba plans to sell voice-activated word processors, for both Japanese and foreign languages.

Figure 9

Spiral Development of Toshiba's Japanese-Language Word Processor



Note: Product champion follows the technology throughout the entire cycle.

Source: Toshiba

Technology Transfer--Japanese Corporate Methods

Toshiba's successful laptop PC is an example of Japanese technology transfer at its best. Dataquest observes that Toshiba, in its search for new product ideas and markets, took the following key steps:

- Identified a market need (Japanese-language word processor)
- Assigned a full-time researcher to work with a university professor on a consignment research (itakuhi-kenkyu) project to develop the basic technology (kana-kanji conversion)
- Tested early models in the marketplace, surveyed customer and distributor responses, then developed the appropriate technology (LSIs for smaller, compact word processors)
- Sought and incorporated new technologies developed in other divisions of the company (e.g., thermal printers, LCD displays, and VLSI)
- Sold the product through various channels (office and home market distribution)
- Sought (and continues to seek) constant improvements (kaizen) to the existing laptop PC, such as ergonomically designed TRON keyboards, ROM program cards, memory storage cards, and voice recognition

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Technology Transfer— Japanese R&D Consortia Methods

OVERVIEW

Since the famous VLSI Project of the late 1970s, the Japanese semiconductor industry has refined its technology transfer methods in collaboration with universities and the national government. This section reviews the technology transfer methods used in the VLSI Project, which is the prototype for current Japanese R&D consortia. Since the VLSI Project, results from the Future Electron Devices Project and formation of the Japan Key Technology Center have led to refinements in the R&D consortium approach.

This section is divided according to the following topics:

- The VLSI Project
- Comparison of major R&D consortia
- Current Japanese semiconductor R&D consortia
- Transferability of Japanese methods
- Implications for Sematech

The VLSI Project

Project Organization

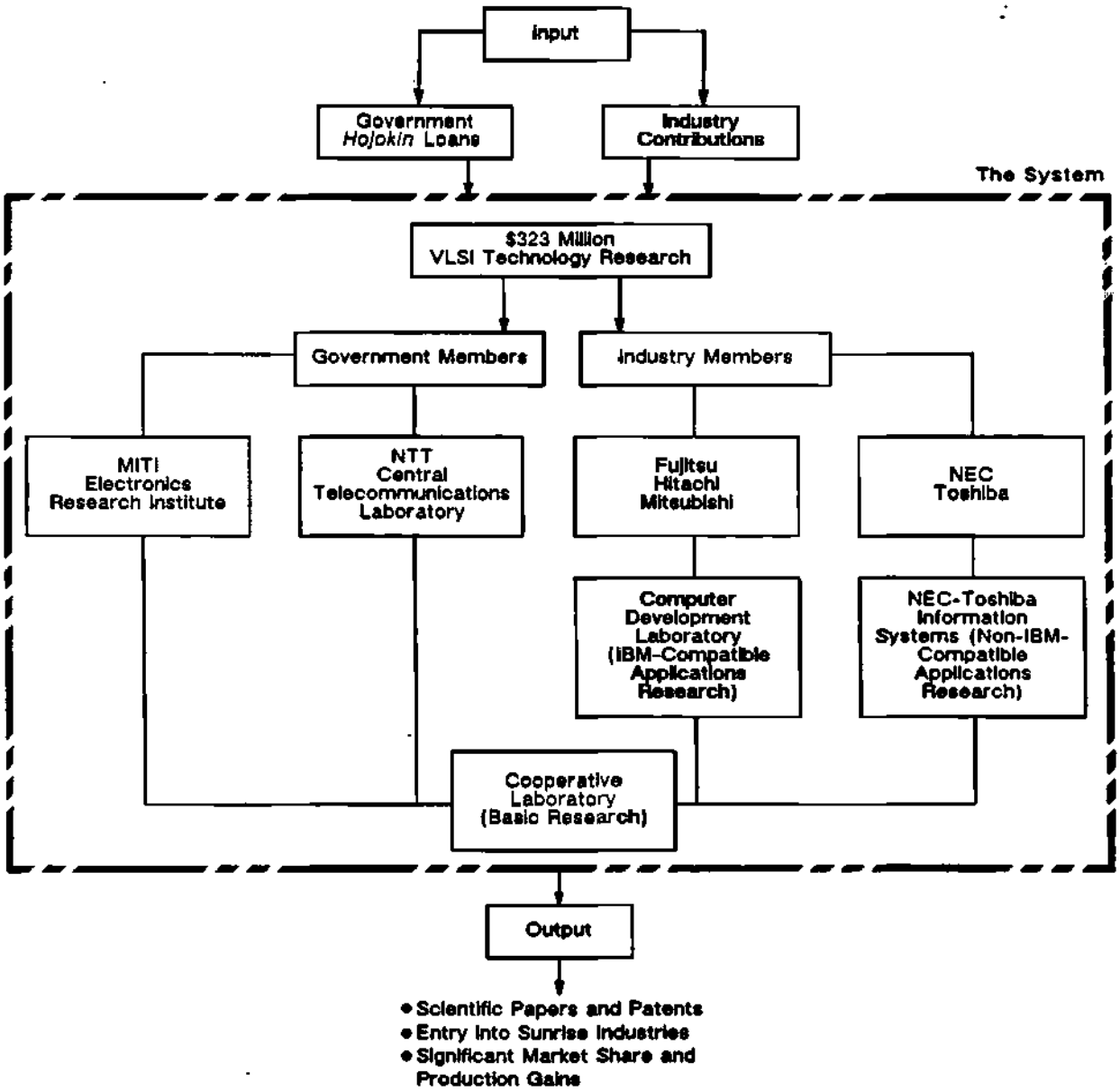
In March 1976, the Ministry of International Trade and Industry (MITI) and Nippon Telegraph and Telephone (NTT) formed the VLSI Technology Research Association with Japanese semiconductor companies. The four-year project was budgeted at ¥70 billion (about $300 million at the 1979 exchange rate of ¥220/$1) and consisted of four cooperating groups, as shown in Figure 1. The project goal was to develop basic VLSI technology and manufacturing techniques that would enable participating companies to do the following:

- Build VLSI chips (64K DRAM or equivalent) by the end of the project in 1979
- Commercialize 1Mb DRAMs or their equivalents by 1985

Technology Transfer—
Japanese R&D Consortia Methods

Figure 1

Organization of the VLSI Project



Source: Japan Agency of Science and Technology

Technology Transfer—
Japanese R&D Consortia Methods

Originally, MITI targeted 1Mb DRAMs, but the participating companies preferred the simpler 64K DRAMs that could be commercialized more quickly. According to Dr. Yoshio Nishi of Toshiba, the following six research areas were targeted for development:

- LSI process techniques and equipment
- Submicron process technology
  - Submicron lithography (optical, electron beam, and X-ray)
  - Submicron etching (dry processes)
  - Submicron thermal processes
  - Interconnection and metallization
- Logic and memory devices
  - High-density MOS memory and logic
  - High-speed bipolar memory and logic
- Materials
  - Low-defect, large-diameter silicon wafer substrates
  - High-performance epitaxy
  - Ultraclean processing
- Improved design and testing
  - Computer-aided design (CAD) for logic/circuit/layout
  - Design verification
  - Highly automated testing techniques and equipment
- Packaging—high density and high speed

Basic research was conducted at the Cooperative Laboratory of the VLSI Association, located at NEC's facilities, while the NEC-Toshiba Information Systems Laboratory and the Computer Development Laboratory handled applied research. By March 1977, there were 300 researchers involved, 100 of whom were assigned to the Cooperative Laboratory. The participating firms allocated the R&D tasks and shared the results. Basic research findings were given to the applied research laboratories, one focusing on IBM-compatible technologies and the other on non-IBM-compatible technologies, for product development. The VLSI Association coordinated the overall program and encouraged information sharing among government agencies and participating firms.

Technology Transfer—
Japanese R&D Consortia Methods

Project funding came from two sources. MITI provided interest-free conditional loans (hojokin), which were repayable when participating firms derived profit from the VLSI technologies. These loans were matched by contributions from the participating firms as shown in Table 1.

Table 1

VLSI Project Funding

	Billions of Yen	Millions of Dollars
MITI Interest-Free Loans	¥30.8	$132
Corporate Contributions	39.2	168
Total	¥70.0	$300

Source: Dataquest
April 1988

Between 1976 and 1979, approximately $300 million in hojokin loans and corporate funds was spent on the VLSI project. A major portion of the funds was used to purchase U.S. production and test equipment. Foreign imports (mostly U.S.) accounted for about 70 to 80 percent of the Japanese test equipment market in 1976 and 1977.

Technology Transfer Methods

During its early phase, the VLSI Project encountered a number of serious obstacles to the free flow of information. To increase the transfer of technology, the project coordinators (Masato Nebashi and Dr. Yasuo Tarui of MITI) implemented the following measures:

- Limited the joint lab to 100 researchers to maintain a more open, informal environment
- Handpicked the 100 researchers assigned to the joint lab in order to obtain top-flight personnel
- Took small groups of researchers out in the evening to break the ice (which turned out to be very effective)
- Involved semiconductor equipment makers to promote closer device-equipment vendor ties
- Rotated researchers from the participating companies throughout the project

- Held regular technical meetings to promote strong intercompany/university/government lab interaction

- Reported regularly on the number of technical papers contributed by participating companies, as well as on the patents filed

The objective was to break down the barriers between these extremely competitive companies and to encourage them to share information. Despite popular opinion, the VLSI Project was the first occasion on which semiconductor researchers had worked together, so creating a cooperative environment was a major challenge. But the project managers realized that informal, people-oriented methods would be the only way that the project could succeed.

The Project Results

The VLSI Project attests to the effectiveness of a well-managed R&D consortium. Dataquest has observed dramatic results in the following four areas:

- Major technological achievements—The participating companies developed a variety of new equipment systems and device prototypes that were later commercialized, as shown in Table 2. In addition, technology road maps were laid out for future corporate research, as shown in Figure 2.

- Scientific papers and patents—By 1980, more than 1,000 new VLSI patent applications were filed. Moreover, the number of research papers presented at the IEEE International Solid-State Circuits Conference doubled from 9 papers in 1976 to 23 papers in 1981, as shown in Table 3. By 1987, the number of papers more than doubled to 50.

- Entry of Japanese DRAM makers—As shown in Figure 3, Japanese companies rapidly entered the market for 16K to 1Mb DRAMs. By the first quarter of 1979, Fujitsu had begun limited production of 64K DRAMs, while Hitachi and Mitsubishi were circulating samples. They were soon joined by NEC, Oki, and Toshiba. By the second quarter of 1981, all six major manufacturers had begun commercial production.

- Japanese production and market share—Despite a worldwide recession, Japanese memory makers captured 30 percent of the worldwide 16K DRAM market and 64 percent of the 64K DRAM market by the end of 1982. All major Japanese 64K DRAM makers quickly moved into 256K DRAMs in late 1983, where they controlled 80 percent of the worldwide market in late 1987, and into 1Mb DRAMs, where they controlled 91 percent of the market.

Technology Transfer—
Japanese R&D Consortia Methods

Table 2

Major Achievements of the VLSI Project

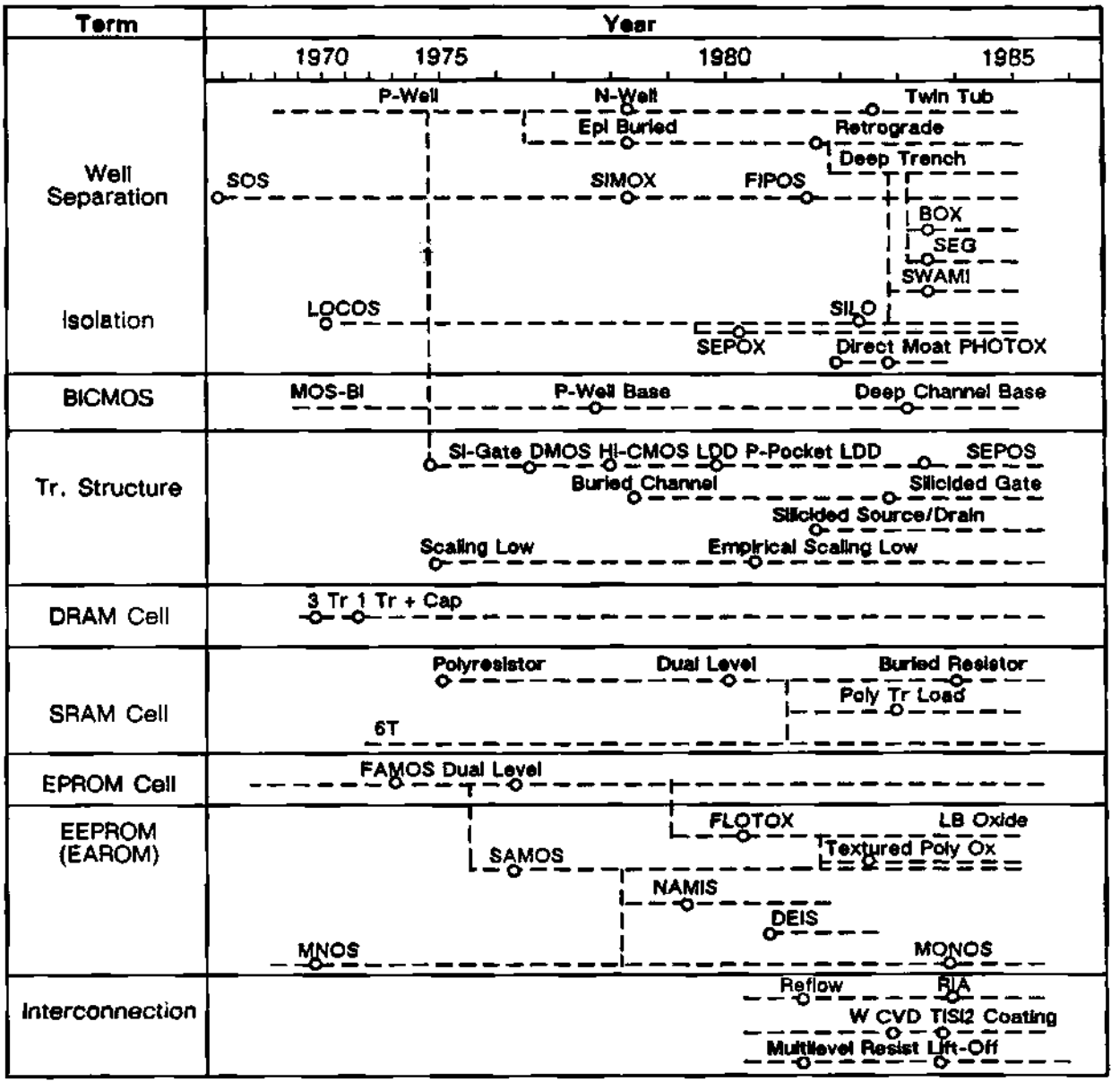
Equipment Technologies	Device Technologies
Electron beam raster scan system	64K and 256K DRAM prototypes
Electron beam projection beam system	16K and 64K SRAM prototypes
X-ray lithography system	10,000-gate, 16-bit MPU
Single wafer multichambered plasma etching system	2-micron process verified through VLSI chip fabrication
Laser scan failure analysis tester	Submicron process feasibility and unit process research
Infrared scanning microscope for water temperature measurement	CAD capability for logic/circuit/ pattern/test pattern
Quadruplicate self-aligned stacked high-capacitance cell	
Submicron device physics/reliability	

Source: Toshiba
Dataquest
April 1988

Technology Transfer—
Japanese R&D Consortia Methods

Figure 2

VLSI Project Technology Road Map



Source: Toshiba
Dataquest
April 1988

Technology Transfer—
Japanese R&D Consortia Methods

Table 3

Number of Technical Papers Presented at IEEE International Solid-State Circuits Conference

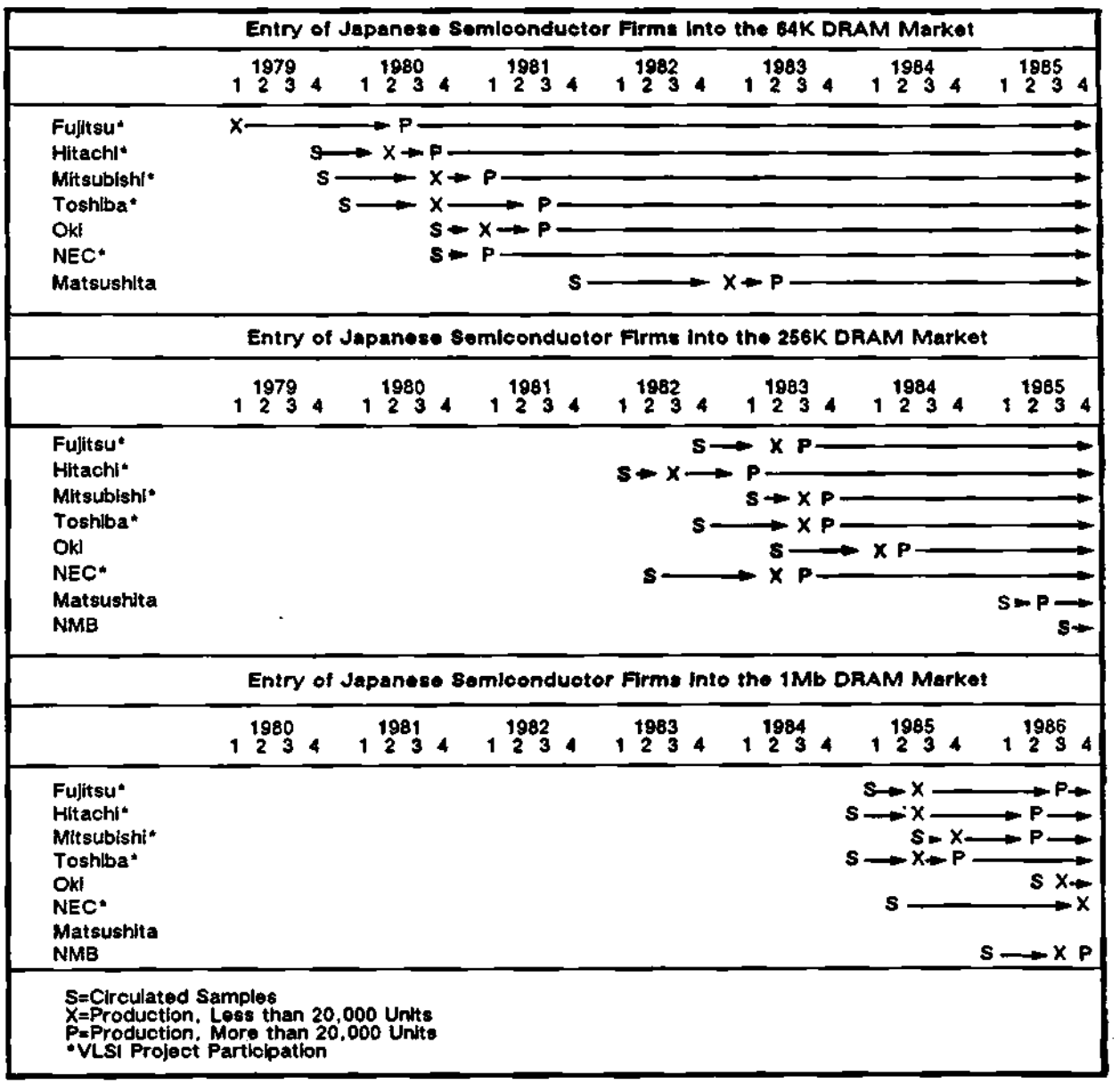
Private Firms	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987
NEC	1	3	4	4	5	4	6	7	6	8	8	5
Hitachi	1	1	3	5	6	6	4	3	8	14	6	15
Toshiba	4	3	1	1	3	2	5	4	11	9	6	8
Fujitsu	1	2	1	0	4	2	3	11	4	4	2	6
Sharp	0	0	1	0	0	1	1	1	0	1	0	0
Matsushita	2	0	0	2	3	0	1	2	4	3	3	2
Mitsubishi	0	1	1	1	1	1	2	3	1	4	6	6
Sanyo	0	1	0	0	0	0	0	0	0	0	0	0
Oki	0	0		1		1	0	0	2	1	1	1
Sony	0	0	1	—	1	4	1	2	3	2	1	3
Subtotal	9	10	13	14	23	21	23	33	39	46	33	46
Government Agencies												
Nippon Telegraph and Telephone (NTT)	0	3	3	6	4	2	7	3	4	2	5	4
VLSI Cooperative Laboratory	0	1	0	1	1	0	0	0	0	0	0	0
MITI Electronic Technology Laboratory	0	1	0	0	0	0	0	0	0	0	0	0
Control Research Laboratory	0	2	0	0	0	0	0	0	0	0	0	0
Tohuku University	0	1	0	0	1	0	0	0	0	1	0	0
Subtotal	0	8	3	7	6	2	7	3	4	3	5	4
Total	9	18	16	21	29	23	30	36	43	49	38	50

Source: Dataquest
April 1988

Technology Transfer—
Japanese R&D Consortia Methods

Figure 3

Entry of Japanese Semiconductor Firms into the DRAM Market



Source: Dataquest April 1988

Technology Transfer— Japanese R&D Consortia Methods

Lessons Learned

In retrospect, the VLSI Project was a spectacular success for a variety of reasons, not only because of astute project management but also because of market timing and competitor activities. Dataquest believes that the following reasons were significant:

- Project organization
  - VLSI Project funding reduced basic R&D costs and risks for participating firms.
  - VLSI Project members were eligible for low-cost loans, special depreciation and tax benefits, and increased access to bank financing.
  - The project lab was limited to 100 handpicked researchers to facilitate open communication and top-level research.
  - Applications research was focused along narrow product lines.
  - The joint lab supported basic technological research but encouraged open communication by leaving actual prototyping and applied research to the participating companies.
- Technology transfer
  - Regular meetings and informal evenings out broke down corporate barriers.
  - Equipment makers were involved in the project.
  - Competition among researchers to contribute the best technical papers was encouraged and recognized by publication of their work at the IEEE Solid-State Circuits Conference.
  - Technical papers were distributed and discussed at regular project meetings.
  - Technology road maps were developed to provide a framework for future corporate research investments.
- Japanese industrial structure
  - Semiconductor divisions within each company were cross-subsidized by other divisions and not expected to be profit/loss centers.
  - Semiconductor makers received long-term financing from their industrial group's (keiretsu) banking affiliates.

Technology Transfer— Japanese R&D Consortia Methods

  - NTT and the vertically integrated electronics firms provided a huge captive market for domestic ICs.

  - "Buy Japanese" purchasing policies among major users, complex distribution networks, and other nontariff barriers protected Japanese vendors from direct foreign competition.

- Market timing

  - American manufacturers reduced their production capacities by laying off workers and cutting back on investments in plants and equipment during the 1974–1975 recession, whereas the Japanese maintained their staffs and increased R&D spending.

  - Several U.S. companies reduced their presence in the Japanese market during the 1974–1975 recession to reduce their operating losses.

  - Key U.S. firms de-emphasized the 16K and 64K DRAM markets or entered these markets too late.

  - Like the Japanese, U.S. manufacturers of 64K DRAMs initially experienced quality and yield problems, but took longer to solve them (until Hewlett-Packard publicly announced problems with U.S. memory quality and yields).

  - Hewlett-Packard and IBM surprised manufacturers by buying on the open market, turning to Japanese firms when quality U.S. products were unavailable.

The effectiveness of the VLSI Project was accentuated by the lack of preparedness on the part of U.S. memory makers. Good management as well as good luck were responsible for their success in the 64K DRAM market.

The VLSI Project provided the technological foundation for improved competitiveness but did not ensure that companies would actually use the technology or develop strong marketing, manufacturing, and distribution strategies to commercialize products quickly. However, by bringing companies together, the project stimulated strong competition among the makers.

Technology Transfer—
Japanese R&D Consortia Methods

Comparison of Major R&D Consortia

The VLSI Project is the prototype for many semiconductor R&D consortia on both sides of the Pacific, but there are many differences among these projects, as shown in Table 4. The key points to note include the following:

- VLSI Project coordinators realized that CAD tools and production equipment were critical elements, so all Japanese projects involve equipment and CAD researchers.
- Research cooperation was difficult to achieve for the VLSI Project because of intense competition during the commercialization phase (3 to 4 years prior to sampling); current Japanese projects are longer term (8 to 10 years) and focus more on basic technologies.
- Due to fiscal austerity and management difficulties, current Japanese projects are smaller (about 60 assigned researchers), and most research occurs at the corporate laboratories.
- Japanese government funding has been reduced for most projects from 40 percent in the VLSI Project to 25 percent for the Supercomputer and Future Electron Devices projects.
- In 1985, MITI and the Ministry of Posts and Telecommunications (MPT) established the Japan Key Technology Center to fund long-term, high-risk research such as SORTEC.
- MITI projects now include more Japanese companies than the VLSI Project, but much fewer than Sematech.
- Sematech is an example of the "big project" approach of the U.S. government; not only are the technical goals ambitious, but coordinating more than 1,000 researchers will be a major organizational challenge.

In general, the Japanese government prefers many small R&D consortia to explore a variety of leading-edge technologies, while the United States likes spectacular, large-scale programs like MCC or Sematech. Moreover, the U.S. government is heading toward more funding involvement, while the Japanese government is reducing its relative share due to budget constraints and the growing financial strength of major corporations.

Technology Transfer—
Japanese R&D Consortia Methods

Table 4

Semiconductor Project Comparison

	VLSI	Supercomputer*	Future Electronic Devices	SORTEC	Sematech
Goal	64K litho. CAD	GaAs/HEMT ECL supercomputer	3-D ICs superlattice biodevices	SOR 64Mb 0.20um	16Mb SRAM 0.35um
Duration	1976-1979 (4 years)	1981-1989 (9 years)	1981-1990 (10 years)	1986-1995 (10 years)	1988-1993 (6 years)
Budget	$325M	$100M	$114M	$106M	$1,500M
Government	40%	Approx. 25%	25%	70%	40%
Corporate	60%	Approx. 75%	75%	30%	60%
Companies	5	6	14	13	>100
Assigned Researchers	100	Approx. 60	Approx. 60	40-50	700-800
Total Researchers	300	Approx. 300	300	Approx. 200	>1,000

Source: Dataquest
April 1988

Transferability of Japanese Methods

Based on the Japanese experience, several key lessons can be drawn for R&D consortia and intercompany technology transfers, as follows:

- National R&D projects
  - Small consortia (<300 researchers)
  - Small core teams (<100 researchers per technology)
  - Frequent technical meetings (<20 researchers)

Technology Transfer— Japanese R&D Consortia Methods

- Leveraged corporate labs
- Organized into three phases

- Intracompany transfers
  - Feedback/spiral approach
  - Job rotation that leads to promotions
  - Factory centered
  - Flexible generalists
  - Production team phased in
  - People oriented, not document oriented

Dataquest believes that national R&D consortia should be kept relatively small (less than 300 total researchers and 100 assigned researchers) to maintain the informal give-and-take environment necessary for effective technology transfer. R&D projects should be divided into three phases: basic research, applied research, and commercialization. To obtain the maximum cooperation from participating companies, collaborative research should focus on the first two phases.

Cooperation from the participating companies is essential for the success of R&D consortia. Instead of "designing-in" management inefficiencies, companies must modify their management policies to allow more flexibility at the research and manufacturing levels. If the goal is manufacturability, fab employees should be given more status, authority, pay, and benefits, and companies must pursue a factory-centered approach to research and development. Manufacturing "researchers" must be flexible engineering generalists who are phased into the early stages of product development.

Semiconductor companies need to become more people oriented, not document oriented. Emphasis should be given to technology transfer by training and rotating people through manufacturing, not just through the delivery of specifications. Ultimately, each researcher must become a product champion who is willing to build and work with teams, from product design to final distribution. R&D consortia can then act as "seedbeds" for emerging technology that can be applied quickly to new product ideas and production.

Implications for Sematech

To test the transferability of the Japanese experience, what are the implications for Sematech? What Japanese technology transfer methods can be applied to a different setting? How would Sematech be organized if it were a Japanese R&D consortium?

Technology Transfer— Japanese R&D Consortia Methods

Table 5 summarizes the major challenges facing Sematech as an organization. Dataquest notes that Japanese R&D consortia face similar challenges, except for the military use requirement. Sematech's major challenge is its massive scale. To transfer technology rapidly, it must break the organization into smaller, competing groups. Moreover, to take advantage of entrepreneurship, it needs to involve smaller companies, either through procurement agreements or horizontally integrated R&D consortia of smaller companies clustered around a Sematech member.

Table 5

Application of Japanese Technology Transfer Methods to Sematech

Challenges	Proposals
Big company domination	Involve smaller companies
Mass production only	Develop ASIC/ASSP fab
Huge organization	Establish two or more competing groups
Pentagon vs. commercial users	Parallel divisions and commercialization unit
Throwaway wafers	Sell wafers to start-ups (antitrust?)
Closed U.S. consortium	Joint R&D unit with foreign companies
	Foreign technology-monitoring division
Fab/R&D gap	Integrated fab/R&D
	Rotate engineers
Best brains withheld	New promotion system

Source: Dataquest
April 1988

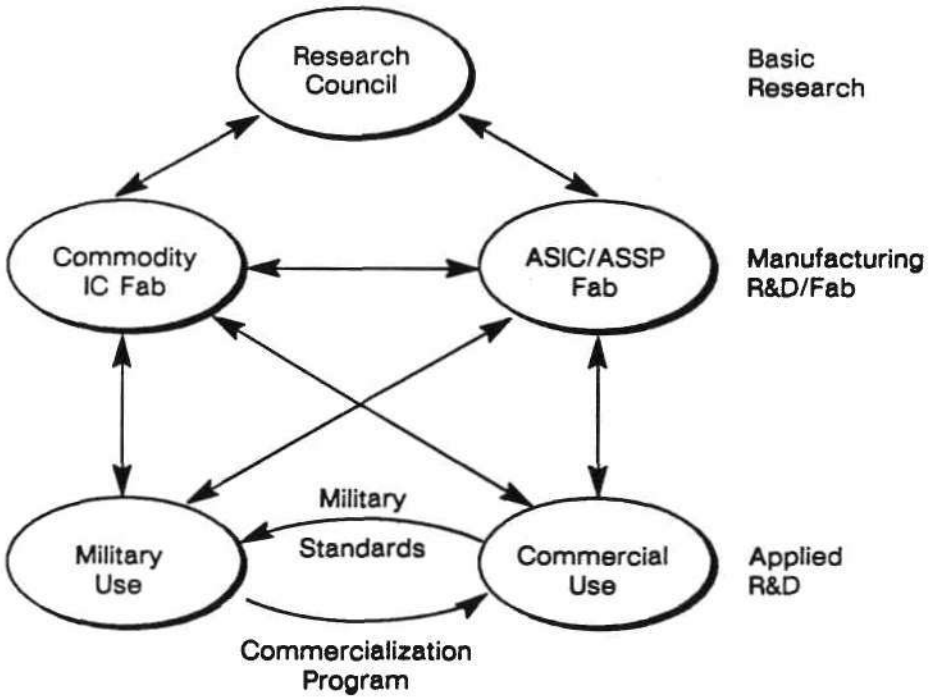
Figure 4 shows how Sematech might be organized to increase the transfer of technology from commodity semiconductors (DRAMs and SRAMs) to application-specific ICs and standard products (ASICs and ASSPs). Such an organization would emphasize strong R&D/manufacturing interaction and a commercialization/military standards program to develop crossover technologies. Multidisciplinary teams and rotating engineers would be an efficient way to transfer technology.

Figure 5 illustrates the type of engineer-rotation system that Sematech could institute to maximize the cross-fertilization of ideas among consortium researchers. Engineers would be professionally evaluated according to their performance in four major areas of proficiency. Those excelling in all four areas would become candidates for fast-track promotion to top management upon returning to their respective companies.

Technology Transfer—
Japanese R&D Consortia Methods

Figure 4

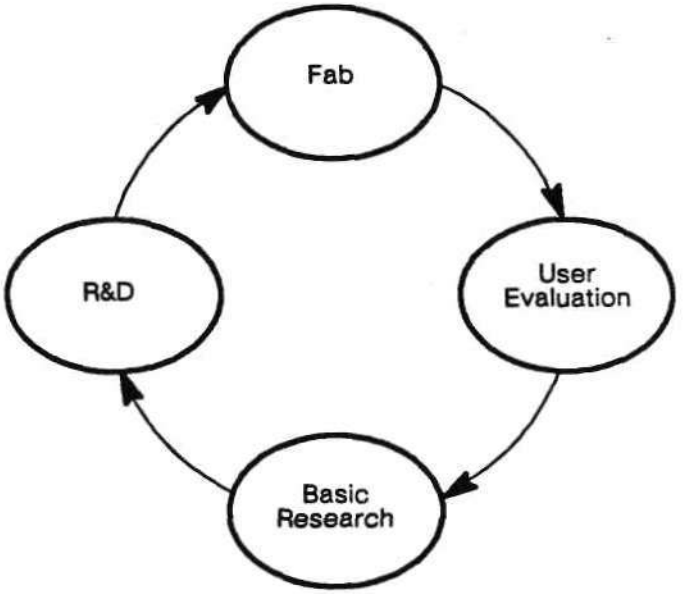
Proposed Sematech Organization



Source: Dataquest April 1988

Figure 5

Potential Sematech Engineer–Rotation System



Rank	Engineer Rankings
1	★★★★ All Four Areas
2	★★★ Three Areas
3	★★ Two Areas
4	★ One Area

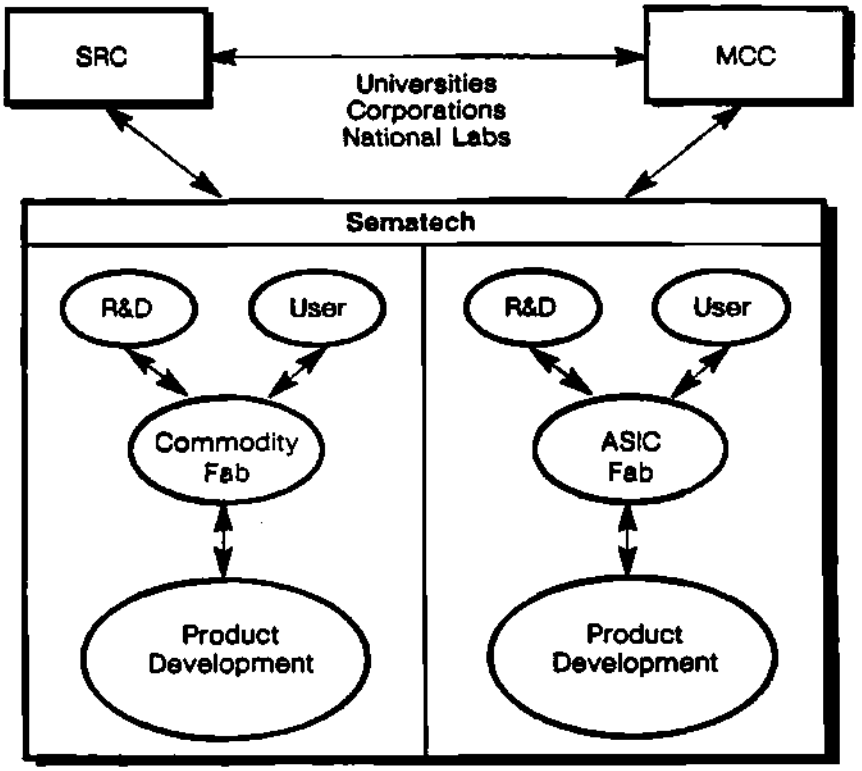
Source: Dataquest
April 1988

Figure 6 depicts the potential interaction of Sematech with other U.S. R&D consortia, such as the Semiconductor Research Corporation (SRC) and Microelectronics and Computer Technology Corporation (MCC). Like Japanese national R&D projects, Sematech participants could hold frequent technical meetings and programs to transfer research results. Researchers should be encouraged to step across organizational boundaries to pursue face–to–face discussions with other researchers.

Technology Transfer—
Japanese R&D Consortia Methods

Figure 6

Sematech Interface



Source: Dataquest
April 1988

Clearly, there are obstacles to developing this type of technology transfer model, but Dataquest believes that it can be achieved despite cultural differences between the United States and Japan. The key to the success of any consortium is not the sophistication of the technology but the flexibility of the management.

Plant Capacity

The following is a list of the material in this section:

NOTE: The arrow symbol indicates the latest documents's location behind this subject tab.

Worldwide Capital Spending Forecast

INTRODUCTION

The capital equipment industry has just experienced its worst downturn in history. In 1986, worldwide capital spending, including captive spending, declined 30 percent. Dataquest believes that the capital equipment industry can now look forward to growth in four out of the next five years. This growth, however, will not be as strong as it has been in the past. We believe that future growth will be slower for two reasons: first, the growth of semiconductor consumption and production will be slower; second, a dollar's worth of capital equipment will be more productive than it has been in the past.

1986: MARKET CRASH

Japan's capital expenditures fell from ¥793 billion in 1985 to ¥293 billion in 1986, a 63 percent drop during calendar 1986. Expressed in dollars, the decline, although severe, was not quite as precipitous. The 1985 figure of $3.3 billion dropped to $1.7 billion in 1986, or 47 percent.

This severe decline in Japanese capital spending is due to major shocks that have hit the Japanese economy in general and the semiconductor industry in particular. These changes include:

- Sluggish exports due to trade friction with Japan's leading trading partners, including the United States and Europe
- Sharply reduced profits and even some layoffs
- Excess capacity and declining domestic prices caused by growing competition from new entrants into the commodity DRAM market, especially from Pacific Rim countries
- The yen shock, which has raised production costs by more than 50 percent within the last year

Spending by merchant semiconductor manufacturers in North America also experienced a severe decline, from $2.3 billion in 1985 to $1.6 billion in 1986, a full 28 percent.

Capital spending by captive semiconductor manufacturers also fell in 1986, from $1.0 billion in 1985 to $0.9 billion in 1986, or 12 percent.

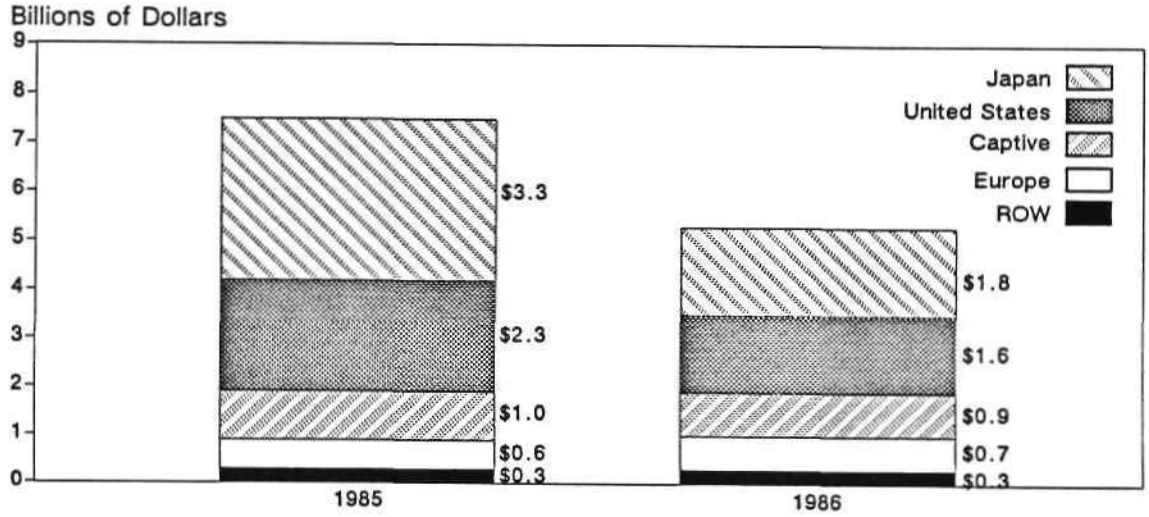
Europe and the rest of the world (ROW) were the two 1986 capital spending bright spots. Measured in dollars, spending in Europe increased 12 percent, from $600 million in 1985 to $670 million in 1986. Many equipment companies have reported sales either even with 1985 or higher. However, measured in local currency units, capital spending, even in Europe, experienced an 11 percent decline in 1986.

Spending in ROW (especially in Korea, Taiwan, Hong Kong, Thailand, and Singapore) was the only unalloyed bright spot in 1986; it grew 25 percent. However, ROW represented only 5 percent of the market for property, plant, and equipment (PPE) in 1986.

Figure 1 summarizes the 1986 market for capital spending in dollars. On a worldwide basis, capital spending declined 30 percent--from 1985's $7.5 billion to $5.3 billion in 1986.

Figure 1

MARKET CRASH



Source: Dataquest
September 1987

1987 AND BEYOND: THE FORECAST

Except in Japan, we expect 1987 to be a year of recovery for the capital equipment industry. We look forward to a 10 percent increase in capital spending worldwide. The main force behind this increase is the continuing recovery of the semiconductor industry itself. Semiconductor manufacturers contacted by Dataquest in April and May were markedly more confident about their business than they were in January. Semiconductor companies are firm about their capital spending plans and in some cases have increased their plans markedly since the first of the year. We believe that semiconductor production will increase 10 percent worldwide in 1987.

Worldwide Capital Spending Forecast

When measured in dollars, capital spending in Japan will decline another 4 percent, to $1.7 billion. When measured in yen, the decline sounds even more painful: 11 percent. The reasons for this downward trend are the continuing uncertainty about exchange rates, overcapacity, low or nonexistent profit levels, and continuing trade friction.

Table 1 presents a regional breakdown of capital spending in 1987 versus 1986.

Table 1

ESTIMATED REGIONAL CAPITAL SPENDING
(Millions of Dollars)

	1986	1987	Percent Change
North America	$1,640	$1,812	10%
Japan	1,754	1,688	(4%)
Europe	670	764	14%
ROW	275	406	48%
Captive	920	1,104	20%
Total	$5,260	$5,774	10%

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
September 1987

1987 and Beyond: Highlights

As semiconductor consumption and production continue to expand in 1988, capacity utilization levels will rise. We therefore expect capital spending, including Japan's, to increase again in 1988. However, since we believe that semiconductor consumption and production will not grow in 1989, we expect a pause in capital spending growth that year. After 1989, however, we expect a renewed growth in capital spending (see Table 2). Also, after 1989, we expect a significant proportion of capital spending to be technology driven as a new generation of devices such as the 4Mb DRAM begins to go into production.

European capital spending will reach $1.7 billion by 1992, which represents a compound annual growth rate (CAGR) of 17 percent between 1986 and 1992.

Worldwide Capital Spending Forecast

Table 2

ESTIMATED CAPITAL SPENDING

	1982	1983	1984	1985	1986
North America	$1,212	$1,452	$3,051	$2,291	$1,640
Japan	921	1,698	3,578	3,332	1,754
Europe	315	350	630	600	670
ROW	45	91	201	220	275
Captive	501	542	965	1,045	920
Worldwide Capital Spending	$2,994	$4,133	$8,424	$7,488	$5,260
Percent Change		38%	104%	(11%)	(30%)

	1987	1988	1989	1990	1991	1992
North America	$1,812	$2,428	$2,292	$2,727	$ 3,436	$ 4,285
Japan	1,688	2,026	2,330	3,495	4,893	6,543
Europe	764	953	965	1,125	1,405	1,728
ROW	406	606	648	810	969	1,135
Captive	1,104	1,309	1,244	1,294	1,527	1,852
Worldwide Capital Spending	$5,774	$7,322	$7,478	$9,451	$12,230	$15,543
Percent Change	10%	27%	2%	26%	29%	27%

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
September 1987

ROW capital spending will grow at a CAGR of 27 percent between 1986 and 1992, to $1.1 billion.

Captive manufacturers such as IBM and AT&T are a major market for semiconductor equipment. Captives accounted for 35 percent of total North American capital spending in 1986. We expect spending by the captives to increase 20 percent in 1987 and to grow to $1.8 billion in 1992.

Worldwide Capital Spending Forecast

Merchant capital spending in North America will grow at a slower rate than in the past--a 17 percent CAGR from 1986 to 1992. Because of this slower growth rate and the severity of the recent decline in capital spending, merchant capital spending will not reach its 1984 level of over $3 billion again until 1991.

Individual company capital spending in North America is shown in Table 3.

Table 3

NORTH AMERICAN COMPANY CAPITAL SPENDING

	1975	1976	1977	1978	1979	1980	1981
AMD	$ 1	$ 6	$ 10	$ 20	$ 39	$ 49	$ 58
Analog Devices	2	4	7	12	10	19	16
Fairchild	20	36	15	23	58	83	140
General Electric							
Harris						45	45
Intel	11	32	46	104	97	156	157
Thomson-Mostek	3	10	24	19	42	85	98
Motorola	21	33	43	72	159	177	184
National	17	26	31	51	84	116	105
Others	56	94	105	177	333	318	285
Philips-Signetics	4	10	19				
Texas Instruments	35	62	88	122	251	300	145
Subtotal of Domestic Company Spending	$170	$312	$388	$599	$1,073	$1,348	$1,233
Non-U.S.-Owned Company Spending in United States							
NEC	-	-	-	-	-	-	-
Philips-Signetics	-	-	-	$ 40	$ 50	$ 90	$ 115
Siemens	-	-	-	-	-	-	-
Thomson-Mostek	-	-	-	-	-	-	-
Total North American Capital Spending	$170	$312	$388	$639	$1,123	$1,438	$1,348
Percent Change		84%	24%	65%	76%	28%	(6%)

(Continued)

Table 3 (Continued)

NORTH AMERICAN COMPANY CAPITAL SPENDING

	1982	1983	1984	1985	1986	1987
AMD	$ 67	$ 111	$ 237	$ 172	$ 55	$ 120
Analog Devices	19	24	58	62	37	50
Fairchild	156	125	195	135	135	68
General Electric		64	107	81	50	50
Harris	35	25	50	50	40	30
Intel	138	146	388	214	150	225
Thomson-Mostek	47	78	123			
Motorola	160	174	412	330	250	338
National	82	120	300	184	117	100
Others	311	293	567	703	494	451
Philips-Signetics						
Texas Instruments	140	232	472	281	213	230
Subtotal of Domestic Company Spending	$1,155	$1,392	$2,908	$2,213	$1,541	$1,660
Non-U.S.-Owned Company Spending in United States						
NEC					$ 10	$ 12
Philips-Signetics	$ 55	$ 58	$ 133	$ 50	60	100
Siemens					20	15
Thomson-Mostek				39	9	25
Total North American Capital Spending	$1,210	$1,450	$3,041	$2,302	$1,640	$1,812
Percent Change	(10%)	20%	110%	(24%)	(29%)	(11%)

Source: Dataquest
September 1987

A Burst of Spending in Japan after 1987

We expect Japanese capital spending to recover somewhat in 1988, increasing from $1.69 billion in 1987 to $2.0 billion in 1988, or 20 percent. After 1988, we expect Japanese capital spending to increase at a rate much faster than the worldwide average. This is because the

Worldwide Capital Spending Forecast

$6.9 billion of capital put on-stream in 1984 and 1985 will be nearing the end of its productive life and will have to be replaced. This 1984-1985 equipment will represent more than 50 percent of the Japanese installed base through the remainder of this decade.

As a consequence of the aging of a significant part of the Japanese installed base, we expect Japanese capital spending to increase 15 percent in 1989 when the worldwide market for capital goods will be flat; we also expect that in 1990 and 1991, Japanese capital spending will increase by 50 percent and 40 percent, respectively.

Table 4 shows individual Japanese company spending on a calendar year basis.

Table 4

JAPANESE MERCHANT COMPANY CAPITAL SPENDING
(Calendar Years, Millions of Dollars)

	1976	1977	1978	1979	1980	1981
Fuji Electric	0	0	0	0	0	0
Fujitsu	$ 3	$ 22	$ 48	$ 64	$110	$145
Hitachi	20	22	43	59	93	149
Japan Semiconductor	0	0	0	0	0	0
Matsushita	10	11	19	41	88	86
Mitsubishi	17	22	19	41	35	59
NEC	34	37	67	105	132	172
NJRC	0	0	0	0	0	0
NMB	0	0	0	0	0	0
Oki	10	15	10	14	53	54
Rohm	0	0	0	0	0	0
Sanken Electric	0	0	0	0	0	0
Sanyo	7	7	7	18	35	54
Sharp	0	0	7	37	37	43
Shindengen	0	0	0	0	0	0
Seiko Epson	0	0	0	0	0	0
Sony	0	0	0	0	0	0
Toshiba	14	19	24	37	48	72
Others	0	0	0	0	0	0
Total	$115	$156	$242	$416	$632	$834

(Continued)

Table 4 (Continued)

JAPANESE MERCHANT COMPANY CAPITAL SPENDING
(Calendar Years, Millions of Dollars)

	1982	1983	1984	1985	1986
Fuji Electric	$ 16	$ 26	$ 51	$ 50	$ 30
Fujitsu	141	226	485	303	96
Hitachi	145	264	506	387	132
Japan Semiconductor	0	0	0	0	30
Matsushita	36	89	371	366	144
Mitsubishi	80	132	274	261	120
NEC	169	247	544	517	180
NJRC	8	9	17	21	30
NMB	0	0	59	59	0
Oki	44	47	110	109	60
Rohm	8	13	25	38	48
Sanken Electric	8	13	25	25	24
Sanyo	40	51	135	197	108
Sharp	32	68	110	151	132
Shindengen	4	4	13	13	18
Seiko Epson	20	38	76	34	30
Sony	20	38	59	151	96
Toshiba	113	366	574	517	389
Others	36	68	143	134	90
Total	$921	$1,698	$3,578	$3,332	$1,754

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
September 1987

A SLOWER LONG-TERM GROWTH

As shown in Table 2, we expect healthy growth during four out of the next five years. This growth, however, will not be as robust as it has been in the past. For the period from 1985 to 1992, the worldwide CAGR is 11 percent; for the period from 1980 to 1985 it was 27 percent.

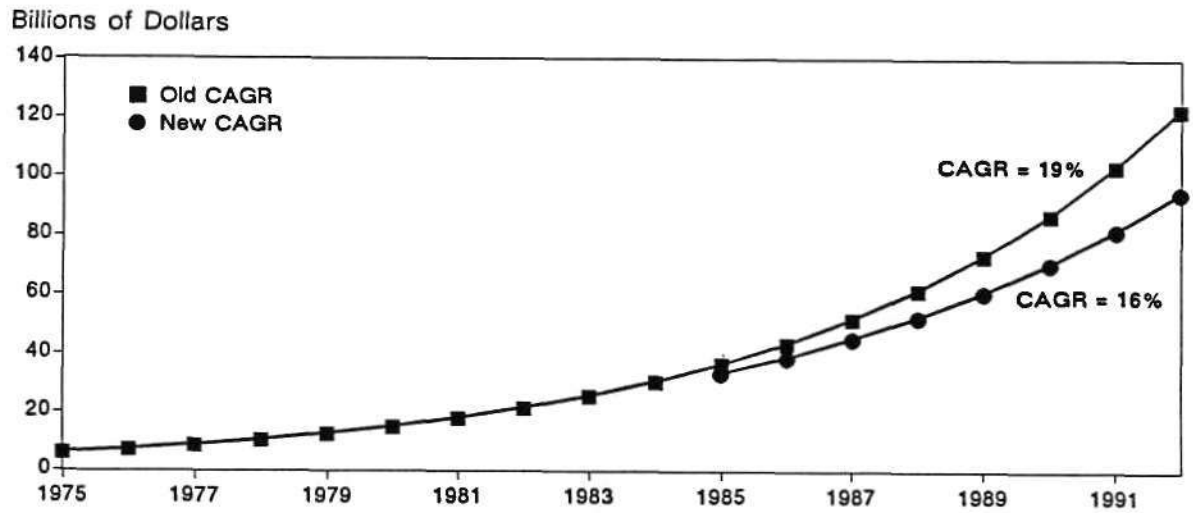
The CAGR of capital spending has slowed down for two reasons: first, the CAGR of the semiconductor industry itself has slowed; second, the productivity of capital has begun to increase.

Worldwide Capital Spending Forecast

From 1975 to 1985, worldwide merchant semiconductor production has grown at a 19 percent CAGR. Dataquest now expects semiconductor production to grow at a slower rate of 16 percent. This new, lower, long-term growth rate is due to the absence of a new "hoola-hoop" such as the PC to drive the industry as it did in 1982 through 1984. It is also due to the success of the industry. Because semiconductors are now found throughout the economy, they will increasingly be influenced by the secular trends of the economy. The effect of this new, slower growth rate will be that the market for semiconductors will be $28 billion less in 1992 than it would have been (see Figure 2). For equipment makers this means $5 billion fewer revenue dollars in 1992 than if the CAGR had remained constant.

Figure 2

A SLOWER WORLDWIDE MERCHANT CAGR
(The Old and the New)

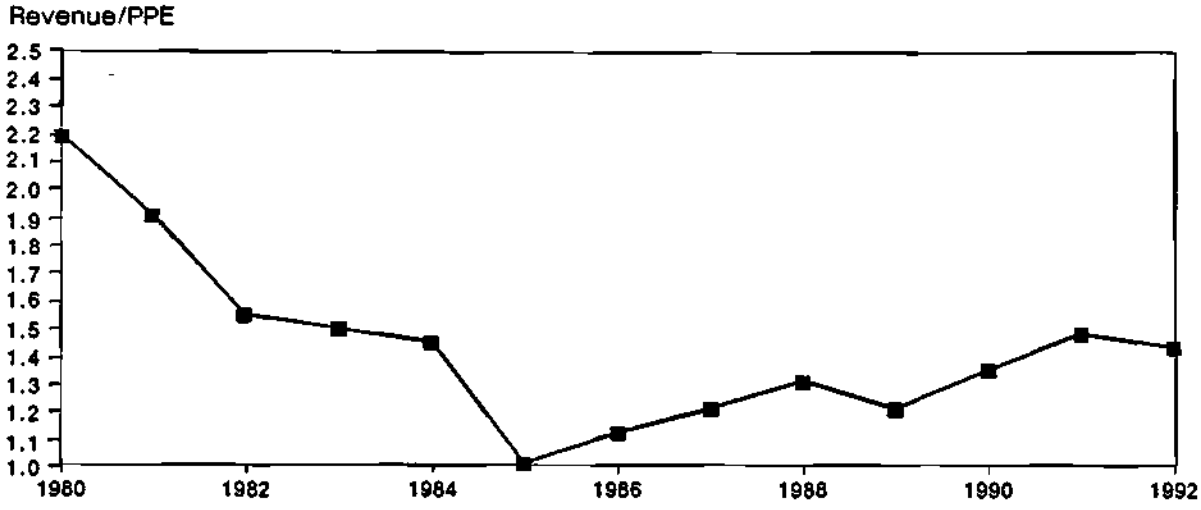


Source: Dataquest
September 1987

As mentioned above, the second reason for the slowdown in the capital spending CAGR is the increasing productivity of capital. Capital productivity is the amount of revenue that is generated with a given installed PPE base. Historically, this ratio has declined (see Figure 3). We believe, however, that capital productivity has begun to rise and will continue to do so. There are several reasons for this. Computer-integrated manufacturing (CIM) will allow manufacturers to schedule many different product mixes and maintain line balance while increasing equipment utilization. (We estimate that equipment utilization is presently in the neighborhood of 40 percent.) Manufacturers will increase their yields because automation will remove people from clean rooms. Lower particulate from semiconductor equipment and materials will also increase yields.

Figure 3

REVENUE/PPE
WORLDWIDE INSTALLED BASE



Source: Dataquest
September 1987

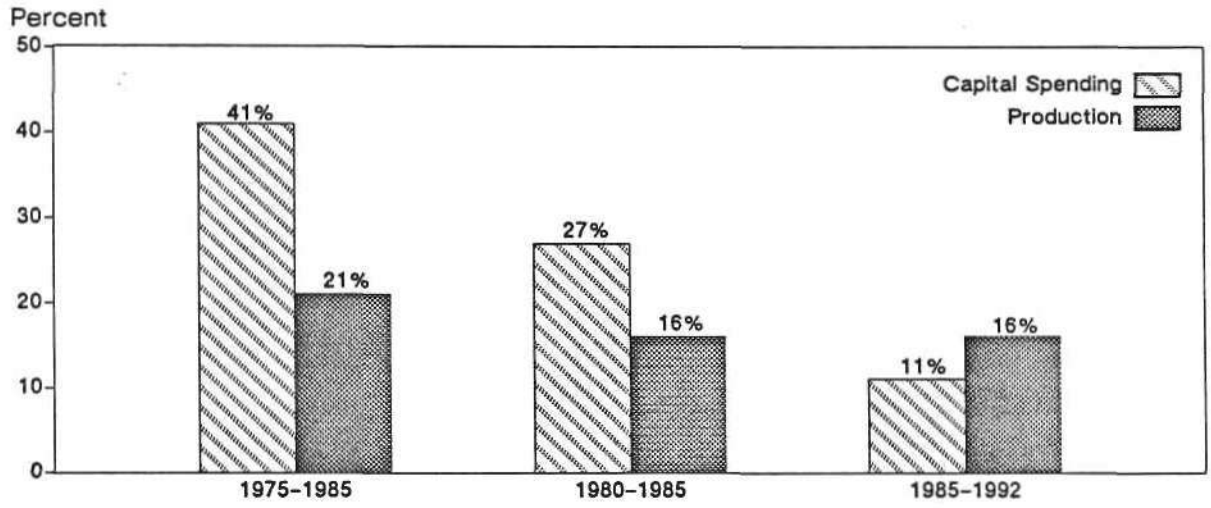
Figure 4 shows the effects of both the slowdown of semiconductor production and of increasing capital productivity. For the first period, from 1975 to 1985, worldwide capital spending grew at a CAGR of 41 percent; worldwide semiconductor production, including captives, grew at a CAGR of 21 percent. From 1980 to 1985, however, both capital spending and production CAGRs had fallen; the CAGR of capital spending fell more. From 1985 to 1992, we expect that the capital spending CAGR will fall below that of semiconductor production. Growth will occur, but it will be slower than it has been in the past.

CONCLUSION

Although growth will be slower for the capital equipment industry than it has been in the past, there will be growth--and that is an improvement over the last two years. Moreover, the growth will be relatively sustained: we expect healthy growth in four out of the next five years. Semiconductor manufacturers will spend first to increase capacity and then to introduce new manufacturing technology. We expect that the CAGR of the semiconductor equipment industry from 1985 to 1992 will be 11 percent, about four times the growth rate of the U.S. economy, and almost 50 percent higher than the growth rate for the electronics industry in the United States. Although less so than in the past, the semiconductor capital equipment industry is still a growth industry.

Figure 4

DECLINING CAGR
CAPITAL SPENDING VERSUS PRODUCTION



Source: Dataquest
September 1987

Plant Robotics

SUMMARY

The semiconductor industry is being squeezed between two major pressures to adopt advanced automation technology: the market pressure to remain competitive with highly automated Japanese companies, and the push to develop increasingly sophisticated products that require more stringent controls for factory cleanliness. The consensus is that humans must be removed entirely from certain process areas, and possibly the entire fabrication process, to achieve the cleanliness required to manufacture advanced VLSI integrated circuits. There is considerable debate as to the best approach to automating a semiconductor facility. Some of the options include:

- Aisles or tunnels of automation with robots interfacing into the clean tunnels
- Teleoperation in which equipment is controlled from outside the clean room
- Individual work cells where similar types of equipment are clustered together
- A "lights out" factory in which operator-free machines work around the clock, even in darkness

In this section, DATAQUEST examines the issues surrounding robotics automation in the semiconductor industry. Researchers from two DATAQUEST industry sectors, the Robotics Industry Service and the Semiconductor Equipment and Materials Service, combined efforts to explore the following topics:

- Market forces driving the adoption of robots
- Semiconductor manufacturers using robotics
- Channels of distribution and implementation
- Approach to semiconductor automation--United States versus Japan
- Clean room requirements and certification for robots
- Robot vendors--their products, prices, and applications
- Market opportunities and directions for development
- DATAQUEST analysis

Due to the highly competitive nature of the semiconductor industry, there is an unusually high degree of confidentiality surrounding the automation efforts of this industry.

Plant Robotics

MARKET FORCES DRIVING THE ADOPTION OF ROBOTS

Robots are used in place of humans to interface with process equipment in the clean room. Robots are used in two ways:

- Within a piece of process equipment
- To transfer wafers and/or cassettes between various pieces of process equipment

In some cases, robot systems provide process control feedback into the computer control system.

The major driving forces behind the use of robots include:

- Reducing the number of people present in a fab to lower the defect density, ultimately resulting in increased yields
- Achieving process consistency
  - When the human element is removed, processes are more tightly controlled.
  - Statistical process data collected will show less distribution about the mean.
- Reducing cycle time--perhaps the most significant benefit of automating the factory
  - Cycle time is the time it takes for a batch of wafers to be completely processed; each time a batch is processed, the yields for that process increase because the factory is climbing up the learning curve.
  - If a company's cycle time is less than its competitors', this means that the company is climbing up the learning curve faster and is obtaining higher yields than its competitors--which directly results in a price and market leadership position.
- Achieving shorter product life cycles
  - This motivates manufacturers to be the first to market with new product designs.
  - Robots are particularly advantageous when dealing with leading-edge technology, such as larger and more expensive wafers that must be handled individually rather than in cassettes.

- Making advances in micron/submicron technology with finer circuit lines
  - These advances mandate ultraclean, human-free environments to avoid contamination from ever-decreasing sizes of particulates.
  - New robot models designed for the clean room meet and surpass current Class 10 specifications, and some achieve or approach Class 1 requirements.

SEMICONDUCTOR MANUFACTURERS USING ROBOTICS

The companies currently involved in the automation of semiconductor manufacturing generally are larger, have greater financial resources, manufacture high-volume products, and produce many product designs. These companies include Fairchild, IBM, Mostek, Motorola, National Semiconductor, and Texas Instruments. Initial applications are the most costly, due to engineering design expenses; subsequent applications capitalize on the experience generated from earlier installations, which brings the costs down. Therefore, the multiple system users can make the most cost-effective use of investments in new automation technology.

In many cases, robotic automation is included in the plans for new facilities where the proper emphasis can be given to overall process flow in the facility design and where the location of equipment affects the air flow and cleanliness levels. Robots are also finding their way into existing fabs one at a time, especially as they are incorporated into the process equipment by original equipment manufacturers (OEMs) or by the semiconductor companies themselves.

CHANNELS OF DISTRIBUTION AND IMPLEMENTATION

Distribution of robotic equipment for semiconductor use in the United States differs from distribution in Japan. The following are some of the paths robotic equipment takes to market in the United States:

- Robot vendors provide direct sales and do complete systems installation. This may include clean rooms established by vendors specifically for design and testing of systems prior to sale.

Plant Robotics

- Robot vendors contract with OEM semiconductor equipment companies to integrate their robots with semiconductor process equipment. A significant number of robot vendors have established or are now negotiating OEM contracts with process equipment suppliers, and DATAQUEST believes that this trend will continue. Robot integration into packaged systems with process equipment is a particularly effective distribution method, as the equipment suppliers have more knowledge of and experience in the semiconductor industry than do most robot manufacturers.

- Systems integrators--companies that integrate robots with other equipment to create functional automated systems--are a major link between robot manufacturers and end users. A number of systems integrators in the United States specialize in electronics applications, and their customers include semiconductor companies. As the new clean room robots become available, these systems integrators are expanding their custom automation services to include semiconductor applications.

APPROACH TO SEMICONDUCTOR AUTOMATION--UNITED STATES VS. JAPAN

Japan is significantly more advanced in the use of robotics in semiconductor production. While the United States takes small, tentative steps to investigate robot capabilities, Japan strides ahead with factory-wide automation of production facilities. A notable example is the new Mitsubishi factory, for which there is no comparable facility in the United States.

Mitsubishi Electric Corporation completed its Saijo semiconductor factory in early 1984. It is a fully automated front- and back-end facility dedicated to the production of 64K DRAMS. It uses automated guided-vehicle systems (AGVSs) that are optically guided to carry cassettes and transfer them to main I/O stations; then robots transfer the cassettes to the processing equipment. The entire wafer fabrication production sequence proceeds without operators ever handling the wafers. All phases of assembly and test, including encapsulation and burn-in, are fully automated. Mitsubishi built its own robots and AGVSs for the factory and even wrote the factory-automation software.

Japan differs from the United States in its reliance on internal resources. There are two reasons for this: it is cost effective to use equipment that was produced internally, and resources from outside suppliers are not as plentiful in Japan. U.S. semiconductor companies turn to vendors and systems integrators because the semiconductor

corporations generally do not produce automation equipment. This has resulted in U.S. vendor strengths and breadth of offerings, since equipment vendors have specialized in their efforts to supply the needs of the U.S. semiconductor industry. In fact, North American vendors such as Hewlett-Packard, Consilium, and I. P. Sharp (a Canadian company) are beginning to supply Japanese companies with factory-automation software. They are exploiting the niche of Japanese semiconductor companies that provide consumer products and, therefore, do not have the internal software expertise to develop their own software, in contrast to the computer producers that do.

In Japan, the automated semiconductor manufacturers are generally part of horizontally and vertically integrated megacorporations that provide a wide range of products other than semiconductors. As a result, systems integration of semiconductor production is often performed in-house, using company-built robots, AGVSs, computers, process equipment, and factory-automation software. Since the semiconductor companies have many resources, there are relatively few Japanese companies providing equipment, software, or systems integration. This is in direct contrast to the United States, where semiconductor companies have limited internal resources for automation compared with the Japanese. U.S. semiconductor companies rely on equipment suppliers and third-party vendors/integrators to meet their automation requirements.

The differences in distribution channels have profound cost implications for installed systems. A company that provides all, or nearly all, equipment and systems integration in-house is able to keep costs to a minimum. A company that purchases robot-integrated process equipment from an OEM vendor is paying the profit margins on the individual pieces of equipment from various suppliers, plus the systems markup. For example, a robot is sold to an OEM for $40,000 to $60,000, which includes the vendor margin. It is combined with a wet bench costing $30,000 to $50,000, again including margin. With controls and software, the integrated product may sell for $125,000 to $155,000.

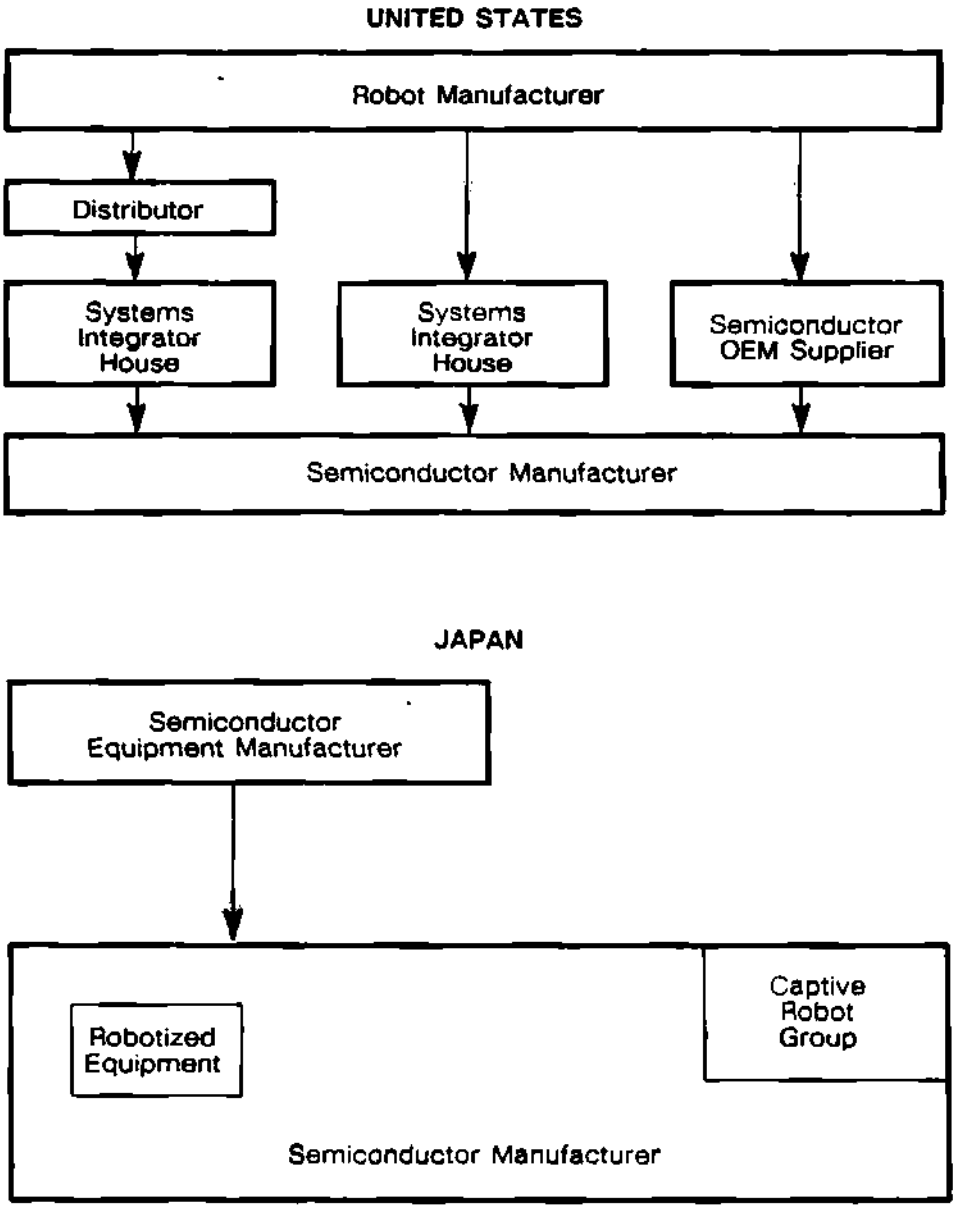
Figure 1 shows the different channels utilized to deliver robotic products to the semiconductor companies in the United States, and in Japan.

Table 1 summarizes the following information for eleven major robot manufacturers in the United States currently supplying robots to the semiconductor industry: products, prices, distribution channels, and customers.

Plant Robotics

Figure 1

ROBOT DISTRIBUTION CHANNELS
UNITED STATES VERSUS JAPAN



Source: DATAQUEST
June 1986

Table 1

ROBOTICS PRODUCTS, DISTRIBUTION, AND USERS IN THE SEMICONDUCTOR INDUSTRY

U.S. Robotics Vendors	Products	Approximate Price Range	OEMs/Systems Integrators (Non-Inclusive)	Semiconductor Manufacturers (Non-Inclusive)
Adept Technology	AdeptOne Adept Vision	$40,000 $17,000	OEM: Perkin-Elmer Systems integrators that handle electronics: Gelzer Systems, UAS Automation Systems, Wes-Tech Automation Systems, Western Technologies	Confidential
American Robot	Modified Merlin Series: MR-6240, MR-6540, MR-6260	Base price: $65,000	Dynamac subsidiary: systems house with focus on electronics industry Daikin licensee: Japanese market	Currently in labs, not yet in production
GCA Corporation	XR-6050 Gantry; Factory control systems	Varies with system	Currently negotiating with OEMs; GCA does own systems integration using GCA or other robots, GCA semiconductor equipment	International CMOS Technology; GCA IC Systems Group (corporate division); others confidential
GMF Robotics	A-101, A-201 A-301	$33,000 $40,000	OEMs not available	Confidential
Intelledex	605-S or 605-T (post or table) Intellevue 200 Computer Vision System	$48,000 $14,500	Flexible Manufacturing Systems, PSI, CVC Products	National Semiconductor, Delco Electronics
Microbot	Alpha II WaferMover System	$14,000 $16,200	Machine Technology, Inc., Seiltec, Optoscan	Texas Instruments (Texas, W. Germany), Harris Semiconductor, IBM, Motorola, Xerox
Panasonic	Pana Robo Clean Room Robot V-1C	$65,000	Bagaard Engineering, Noel J. Brown, Automation Tooling Systems	Confidential
Precision Robots, Inc.	PRI-1000 (wafers) PRI-2000 (cassettes)	$30,000 to $60,000 systems	Materials Research Corp., Tetron, Santa Clara Plastics, BTU	National Semiconductor, Intel (worldwide), SGS (Italy)
Seiko Instruments USA	RT-3000 RT-2000 XY-3000 XY-2000	$32,850 $34,000 $33,850 $32,850	Automation Tooling Systems, Datum Industries, Dick Schuff & Co., Intelmatec Corp.	GTE, Intel, Motorola, Northern Telecom, RCA-Sharp, Sperry, Westinghouse
Unimation	Clean Room PUMA 560 w/VAL-Plus control sys. w/VAL-II control system	 $48,000 $53,000	VEECO (PUMA integrated on Automated Guided Vehicle System); negotiating with OEMs; also use systems integrators, distributors, direct sales force	Confidential
United States Robots	Maker 110	$45,000	OEMs: Semifab; Poly-Flow; WES, Inc.; Systems Integrators: Penrep Ltd., Durham Technology Group, Contamination Control and Devices	Harris Communications, Intel, Mostek, Motorola, Texas Instruments (Texas)

Source: DATAQUEST
June 1986

CLEAN ROOM REQUIREMENTS AND CERTIFICATION FOR ROBOTS

Clean Room Requirements for Robots

Of the 60 U.S.-based robot manufacturers, only a handful are focusing on clean room robots, with the majority of robots entering the market between 1984 and 1985. By definition, robots are multifunctional, reprogrammable devices able to perform a variety of tasks. Therefore, robots used in semiconductor applications are largely standard robots modified to meet clean room requirements. They are capable of performing other tasks, however, particularly material handling in the electronics industry. Some have required a year or more of redesign and structural modification to achieve clean room standards. They nevertheless remain general-purpose robots rather than special-purpose designs limited to use in semiconductor applications.

The following are possible steps in modifying a robot to achieve the required clean room specifications:

- Rotary joints are enclosed with ferrofluid seals to prevent particles from escaping from the moving parts.
- External surfaces are made of nonshedding bare metal or painted with a nonflaking paint, epoxy, or polyurethane.
- Lubricants are not exposed or have a very low vapor pressure.
- Motors are brushless to minimize particulate generation.
- Negative-pressure air is pulled through the inside of the robot, or bellows surrounding the robot, and filtered as exhausted.
- A clean suit of fray-resistant material is tailored to the robot.
- End effectors are designed using contaminant-free material, such as stainless steel.

In most of the front-end operations, robots are not required to have high speeds but to move smoothly to avoid generating particles or breakage from water movement inside the cassettes. The trend is toward higher communications capability to integrate a robot into an automated factory control system. Robots interface with material feeders, processing equipment, safety controls, and host computer systems for complete process tracking and control. The communications and integration needs, as well as the complexity of some tasks requiring

decision making by the robot, mean that it must be programmed in a high-level language. High robot uptime and mean time between failure (MTBF) are important to keep humans out of the fab as much as possible.

Back-end operations need more speed and precision for assembly and test applications. Cleanliness is less stringent, and robots used in other electronics industry applications are often used.

Clean Room Certification

U.S. government guidelines specify the standards for Class 100 clean room environments. The stricter Class 10 and Class 1 environments are de facto standards currently specified and recognized by the semiconductor industry, but they are not as yet (and may not become) official government standards. Some robot manufacturers do not claim class certification beyond Class 100, but prefer to publish the results of testing by third parties. Testing is performed by four major means:

- Robot vendors use an internal clean room where systems are developed and tested prior to delivery to customers.
- Process equipment suppliers, OEM vendors or systems integrators, integrate the robots with their equipment and then sell custom automation solutions to customers.
- Independent engineering firms or semiconductor consultants, such as Dryden Engineering or the Institute for Microcontamination Control, perform the testing.
- Semiconductor manufacturers, the users of the equipment, certify the systems in their own environment; this includes robot supplier corporations that test their automation products in semiconductor divisions within the corporation.

All systems eventually have to meet standards within each installation, where the unique layout of equipment influences air flow and particulate control and where human traffic affects the level of cleanliness that can be achieved overall.

ROBOT VENDORS--THEIR PRODUCTS, PRICES, AND APPLICATIONS

Table 2 gives a brief description of leading robotic products, features, and specialization. For further detail, a list of the robot manufacturers, OEMs, and systems integrators is presented in Appendix A at the end of this newsletter.

Table 2

PRODUCT/APPLICATION CHART: ROBOT VENDORS

Company	Products/Applications	Advantages Stated*	Comments
Adept Technology	AdeptOne assembly robot used predominantly in back-end assembly and test. SCARA (assembly) configuration, 13-lb. payload, 32-in. reach. Sample applications: component testing of SIPs, DIPs; load/unload wire bonder; palletize components of molding machines; test station conveyor tending; lead frame alignment in ceramic chip assembly; load/unload lead frame equipment. 10-20 back-end installations; fab applications confidential.	Speed, precision. Looking at applications requiring these characteristics. Uses sophisticated control system, VAL-II, with process control capability.	Currently in early stages of supplying semiconductor industry. Evaluating needs to develop solutions.
American Robot	Turnkey systems integration. 6-axis articulated-arm robots. Models: MR-6240, MR-6260, MR-6540 have work envelopes ranging 40 in.-60 in., payload 20-50 lbs. Targeted to handle heavy quartz boats and large wafers. Equipment targeted: Diffusion furnace and other equipment load/unload; conveyor unload; DIP handler in test area. Work cell approach: Clean Wafer Cassette Handling work cell includes robot system, controller, linear conveyor, to link with wafer processing equipment. Some confidential installation in R&D laboratories.	Heavier payload and extended-reach capabilities. High level communication with host computer system; SECS-II. Subsidiary Dynamac Inc. emphasizes design of complete automated factories for electronics industry.	New products to reach market in early 1986 for light assembly and material handling; applicable to back-end assembly and test.
GCA Corporation	Turnkey systems integration. XR-Series gantry robots modified for clean room; XR-6050 has 50-lb. payload. Emphasis on total CIM. Performs analysis; designs factory control system; then provides total system of robots, hardware, and software. CIMcell product skips hierarchy channels to communicate directly to host computer. All systems designed to order, not off the shelf. Can upgrade semiconductor equipment to communicate on factory level; GCA systems communicate with process equipment from any vendor. Teleoperation technology provides human control of robots to perform nonstandard, unprogrammed work--such as equipment repair--without human entry into clean room. Installations include several large contracts for whole factory automation.	GCA is leading producer of stepper equipment. In-house experience base with GCA IC Systems Group, which tests and uses the automated systems. Emphasis on factory control and communication.	Clean room material handling system debuted at Semicon West in May, 1985.

(Continued)

Table 2 (Continued)

PRODUCT/APPLICATION CHART: ROBOT VENDORS

Company	Products/Applications	Advantages Stated*	Comments
GMF Robotics	Turnkey systems integration. E-301 is a Class 10 robot, approaching Class 1, uses patented design sealed linear joints. Three to five axes, with a 33-lb. payload in a 3-axis configuration. E-101 and E-201 offer different envelope sizes, are Class 100, and can convert to Class 10. Targeted to handle wafers and cassettes. Twelve installations.	Provides systems or units. Develops and tests systems in an in-house clean room. SECS-II	GMF is just entering clean room market with first product demonstration at Robots 9, June 1985. E-301 will be available on production floor in December 1985. Within GMF Electronics Business Segment, half of efforts are devoted to robots for clean room use.
Intelledex	Turnkey systems integration. Articulated, 6-axis Model 605 can be post, table, or track mounted. Sealed rotary joint, tactile sensors. Applications: predominantly cassette, also wafer handling; lead frame loading. Developed wet chemical processing system for 6 in. wafers in cooperation with Flourocarbon, which makes wafer cleaning systems and particulate detection equipment. Offers 7 systems where robot on track operates Megasonic Cleaning Systems and Superclean 1600 Rinser/Dryers in Class 10 room. System oversees recipe selection; monitors fluid levels, temperatures, and timing decisions. IntelleVue 200 Computer Vision System: aligns wafers for probing by test equipment; process control--assures ink jet defect marker functions and reads characters for part tracking.	Emphasizes smooth motions to avoid contact contamination. High-level communications ability for interface with sensors, process equipment, and process tracking and control. SECS-II, IEEE-488.	Company specialization in 2 markets: semiconductor manufacturing and electronic industry. Starting distribution in Europe.
Microbot	WaferMover: turnkey, standardized systems for wafer handling. Consists of Alpha II robot with 5-axis articulated arm, various vacuum pickups to allow handling of different size wafers, microcomputer control, peripheral equipment. Alpha II system is Class 1. Optional accessory Robot Clean Suit tested to more stringent level of Class 1. Applications: Automates transfers into and out of coater, developer, and aligner; picks wafers out of cassettes, sorts, and takes to inspection systems, then refiles into cassettes. Communicates between equipment.	Pre-engineered package solutions allow faster installation, less risk to user due to proven technology. Two-year use history in fabs. Reliability: 4,500+ hours MTBF; 500 hour stress test at 130 degrees F for whole system	Lowest-cost robot systems available on market.

(Continued)

Table 2 (Continued)

PRODUCT/APPLICATION CHART: ROBOT VENDORS

Company	Products/Applications	Advantages Stated*	Comments
Panasonic	Pana Robo V-IC Clean Room Robot, 6-axis articulated arm with 11-lb. payload; Class 10. Applications in wafer fab and wafer coating processes. Robot transfers wafers between cleaning baths; loads/unloads sputtering equipment. Installations: Nearly 25 in the U.S. since June 6, 1985 announcement to provide robots for semiconductor industry.	High precision, smooth motion to avoid contact contamination, high speed (80 in./second). Clean room testing performed by independent labs and by in-house tests in Japan and in U.S.	Panasonic Industrial Company is a division of Matsushita Electric Corporation of America, which has extensive experience base in electronics, notably in Japan.
Precision Robots, Inc.	Turnkey systems integration. PRI-1000 and PRI-2000 series used for handling wafers, cassettes, wafers mounted to film frames, quartz boats. Articulated arm with up to 6 axes, 10-lb. payload (higher available). Tactile sensor, vacuum pickup. Application in 5 major areas: sputtering, CVD, diffusion, epitaxy, wet chemical processing. Class 10. Nonvolatile computer memory system used to maintain lot identities, communicates with central computer. More than 50 installations to semiconductor manufacturers worldwide.	Reliability, high (98 percent) up-time; MTBF over 1,000 hours. Unique arm structure and mechanical linkage allows precise, smooth linear motion for moving wafers in and out of boats.	Internationally marketed, installations in Japan and Europe. Supplies products to electronics industry, with more than 80 percent of focus on clean rooms.
Seiko	Primary model used is RT-3000 modified for clean room, including negative air pressure system. Also smaller RT-2000. Both cylindrical-coordinate, 4-axis, with payloads of 5.5 to 11 lbs. Two Cartesian models, XY-2000 and XY-3000, featuring high accuracy and repeatability levels. Applications: lead frame handling--robot picks lead frames from cassette, palletizes them for die bonding. Other uses in die/wire bonding area. Turnkey systems available through large network of distributors.	XY-series are accurate to .0008 inch and repeatable to .0002 inch, and can be downloaded directly from host computer. Seiko has extensive experience base in electronics industry.	Developing new clean room products cooperatively with users. Anticipate product announcements in near future.
Unimation	Turnkey systems integration Clean Room PUMA 560, a 6-axis articulated arm with significant internal changes and parts built for low particle emission: negative air pressure, sealed motors, particulate exhaust air filter. Major OEM contract with VEECO Integrated Automation, Inc., which integrates PUMA arm on top of mobile Automated Guided Vehicle System (AGVS). Applications: wafer or cassette equipment handling; furnace, other loading. Several proprietary applications.	High level control and factory integration capability; uses sophisticated controller--VAL-II; SECS-II. Clean room compatibility tested by VEECO in Class 10 room. Unimation publishes the test results.	Internationally marketed. Entered clean room market at beginning of 1985. Anticipate new product announcements toward end of 1985.

(Continued)

Table 2 (Continued)

PRODUCT/APPLICATION CHART: ROBOT VENDORS

Company	Products/Applications	Advantages Stated*	Comments
United States Robots	Turnkey systems integration. Maker 110 is a spherical-coordinate, 5-axis robot designed for clean room; payload more than 5 lbs. Class 10. Control/communications, work process tracking ability using SECS-II and ASCII interface for monitoring/control by PC, mini, or mainframe. Used almost exclusively for semiconductor industry. Applications emphasize work cell approach: wet bench work cell, dry etch, furnace and rinser/dryer loading. Current focus is work cells, working on full factory systems automation. 30-40 installations after 1 year in the market.	Passed clean room testing and certification by Texas Instruments, Dallas. Targets two major markets: semiconductor front end is 65-70 percent of company focus; electronics industry material handling 30-35 percent.	Internationally marketed. Intends to provide capability to automate all front-end processes.

*All Companies stated that their products meet stringent cleanliness standards; therefore, cleanliness will be assumed for all companies although not listed.

Source: Company Literature
DATAQUEST
June 1986

Several additional vendors offer mobile transport vehicles or wafer transport systems.

Flexible Manufacturing Systems has introduced a computer-integrated manufacturing system that has navigation, equipment docking, and robotic-arm transfer capabilities. The system components are: a mobile robotic vehicle for materials transfer and transport; an intelligent work-in-process station that provides local storage of cassettes and wafers; a workstation interface that includes a docking module and operator interface; a computer system with communications network, including SECS (Semiconductor Equipment Communications Standards) link; and software for monitoring and control.

Veeco Integrated Automation, Inc., has a Robotic Wafer Fabrication Automation System that uses an automated guided vehicle equipped with a robotic arm to transport wafers from station to station. The system consists of the vehicle, WIP station, and central control computer. The robot arm inserts and removes loaded cassettes from production equipment, stores wafers, and controls wafer inventories. It communicates with the central computer (MICROVAX) via an IR link.

Nacom offers the Namtrak Wafer Cassette Transporter, which includes elevators with load/unload stations and an interlocking track to transport wafers in a clean environment. A pneumatically controlled transfer mechanism loads and unloads cassettes from the transfer tunnel. The tunnel is an enclosed Class 10 environment that allows wafers to be transported between processing equipment and clean rooms. An optional elevator system allows wafers to be moved at ceiling level, thus allowing maximum floor space utilization.

Additional companies that provide this type of conveyor/track equipment system for moving cassettes include: Programmation, Shuttleworth Systems, and Translogic.

MARKET OPPORTUNITIES AND DIRECTIONS FOR DEVELOPMENT

The current state of automation in the United States is work cell automation--or islands of automation--where a robot is combined with a process machine, fixturing, and a controller that oversees the activities of that particular process. The next level of opportunity involves linking together the individual islands so that entire production lines run without human operators. This includes the transfer of wafers within and between processes and control by a central computer system. Recent development efforts and new products focus on mobile equipment that services multiple machines and locations to maximize the use of the equipment.

Plant Robotics

Specific robot directions for development may include machine assisting: correcting minor malfunctions and jamming, alcohol wipedown and equipment cleaning, and routine maintenance. In addition to targeting these operations for robots, GCA Corporation offers teleoperation equipment originally developed for use in the nuclear industry. It allows a human operator outside the clean room to manipulate robotic equipment with manual control, while receiving sensory feedback as if operating the equipment directly. This method can be used to perform a nonstandard assist or repair without entering the clean environment or shutting down a process.

DATAQUEST ANALYSIS

The semiconductor industry is a very new area for robotics penetration, and Japan is ahead of the United States in adopting robots. The use of robotics in the U.S. semiconductor industry is in its embryonic stages. In the United States, there are no fully automated facilities. Rather, U.S. manufacturers have taken the approach of automating the work cell area first; then they will connect the various work cells together in a fully automated factory. The robots that are in use today in U.S. fabs are being used in the work cell areas of wet benches, photolithography, diffusion, and ion implantation, but even in these areas the use of robotics is limited. It is likely that the majority of currently installed robots are being investigated in R&D laboratories, where the semiconductor manufacturers test and evaluate new methods and equipment prior to using them in production.

The whole semiconductor industry takes a different approach from other industries to justification of robots. While cost is important, DATAQUEST believes it to be second in emphasis to yield improvement, reduced cycle time, and process control. The purpose of reducing the human work force is not only to save labor costs, but primarily to improve cleanliness of the environment and therefore increase product yields. Higher product yields result in lower IC product costs, which are required for a semiconductor manufacturer to remain competitive in the world market.

U.S. semiconductor manufacturers are just starting up the learning curve of adopting advanced manufacturing technology. The companies that act quickly to fully automate their factories will realize significant competitive gains. DATAQUEST sees the U.S. robot vendors responding appropriately to meet the needs of the semiconductor industry. They are making the effort to work closely with semiconductor manufacturers and OEM equipment suppliers to develop products best suited for use in the

fabs. The robot vendors are positioning themselves to supply the domestic market and also to sieze opportunities overseas where certain market segments lack competitive products. However, it is not up to the robot vendors to drive the market. That responsibility lies with the semiconductor manufacturers, who must fully automate their factories or lose their competitive position in the world market.

Appendix A

Robot Manufacturers

The following companies can provide further infomation and specific product details:

Adept Technology
1212 Bordeaux Drive
Sunnyvale, CA 94089
(408) 747-0111

American Robot Corporation
121 Industry Drive
Pittsburgh, PA 15275
(412) 787-3000

GCA Corporation
Industrial Systems Group
One Energy Center
Naperville, IL 60566
(312) 369-2110

GMF Robotics
5600 New King Street
Troy, MI 48098-2696
(313) 641-4201

Intelledex
4575 S. W. Research Way
Corvallis, OR 97333-1098
(503) 758-4700

Microbot
453-H Ravendale Drive
Mountain View, CA 94043
(415) 968-8911

Panasonic Industrial Company
Industrial Equipment Division
One Panasonic Way
Secaucus, NJ 07094
(201) 392-4979

Precision Robots, Inc.
6 Cummings Park
Woburn, MA 01801
(617) 938-1338

Seiko Instruments USA
Robotics/Automation Division
2990 W. Lomita Blvd.
Torrance, CA 90505
(213) 530-8777

Unimation Incorporated
Shelter Rock Lane
Danbury, CT 06810
(203) 796-1188

United States Robots
650 Park Avenue
King of Prussia, PA 19406
(215) 768-9210

Appendix B

Systems Integrators and OEM Equipment Suppliers

The following companies can provide further information on integration of robot systems, as well as specific product details:

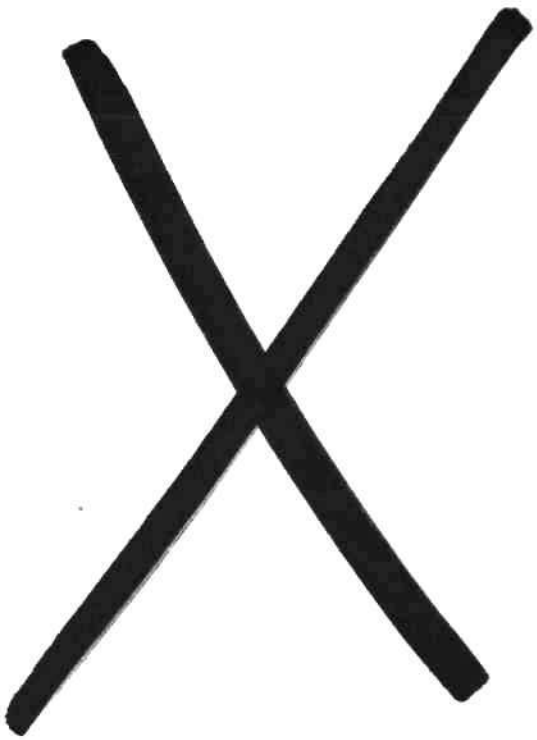
Systems Integrators/ OEM Equipment Suppliers	Robot Manufacturers Represented (Non-Inclusive)
Mr. Joe Nava Vice President, Marketing Flexible Manufacturing Systems, Inc. 16780 Lark Avenue Los Gatos, CA 95030-2315 (408) 395-2777	Intelledex
Mr. Rick Heim, Vice President Machine Technology, Inc. 641 River Oaks Parkway San Jose, CA 95134 (408) 942-0800	Microbot
Solitec, Inc. 1715 Wyatt Drive Santa Clara, CA 95054 (408) 980-1355	Microbot
Optoscan Corporation 1250 Charleston Road Mountain View, CA 94043 (415) 961-9451	Microbot
Mr. Roger Awad, Marketing Manager Automation Tooling Systems (ATS) 101 Trillium Drive Kitchener, Ontario CANADA N2E 1W8 (519) 893-7541	Panasonic, Seiko
Mr. Bill Reiersgaard Bagaard Automation 725 S. E. Lincoln Portland, OR 97214 (503) 233-8246	Panasonic, Seiko

Plant Robotics

Systems Integrators/ OEM Equipment Suppliers	Robot Manufacturers Represented (Non-Inclusive)
Mr. Bill Salvesen, President Datum Industries, Inc. 15 Grand Avenue Palisades Park, NJ 07650 (201) 943-8870	Seiko
Mr. Dick Schuff, President Dick Schuff & Company 2432 W. Peoria Avenue, Suite 1076 Phoenix, AZ 85029 (602) 997-0206	Seiko
Mr. Minoru (Red) Akagawa, President Intelmatec Corporation 28300 Industrial Blvd., Unit H Hayward, CA 94545 (415) 887-8703	Seiko
Mr. Eric Waeldchen, Manager Keller Technology Corporation 2320 Military Road Tonawanda, NY 14150 (716) 693-3840	Seiko
WES, Inc. P.O. Box 800 Brandywine Court Lafayette, NJ 07848 (201) 579-1998	United States Robots
Contamination Control & Devices, Inc. 510 Market Loop West Dundee, IL 60118 (312) 428-5105	United States Robots
Penrep Limited 790 Lucerne Drive Sunnyvale, CA 94086 (408) 733-7176	United States Robots
Durham Technology Group, Inc. 2300 Cypress Point East Austin, TX 78746 (512) 328-0402	United States Robots

Plant Robotics

Systems Integrators/ OEM Equipment Suppliers	Robot Manufacturers Represented (Non-Inclusive)
Semifab, Inc. 307 Fallon Road Hollister, CA 95023 (408) 637-8101	United States Robots
Veeco Integrated Automation, Inc. 10355 Brockwood Road Dallas, TX 75238 (214) 349-8482	Unimation



Design Centers/ASICs

The following is a list of the material on this section:

NOTE: The arrow symbol indicates the latest documents's location behind this subject tab.

Gate Array Suppliers

EXECUTIVE SUMMARY

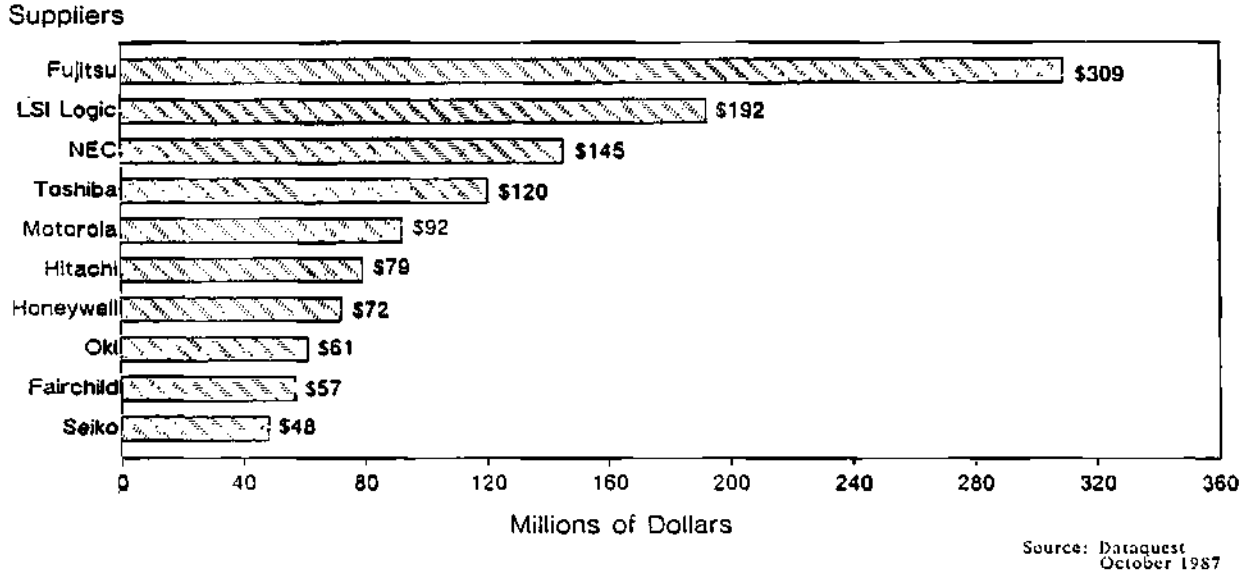
Semiconductor users undoubtedly face bewildering situations when it comes to selecting suppliers for specific component types. This is especially true with gate arrays. Changes in market conditions and the profile of a supplier base can translate into confusion when the time arrives for negotiation and commitment.

Dataquest has projected the $1.8 billion gate array market of 1986 to exceed $7.8 billion by 1992. Today, there are in excess of 100 merchant gate array suppliers. Fierce competition in the North American market has caused nonrecurring engineering charges (NRE) as well as device pricing to decline to the point where most suppliers sacrifice profits for market share.

Dataquest believes that large, broad-based IC suppliers will dominate the mainstream gate array market and force the small suppliers to be acquired, to move to niche markets, or to move out of the market altogether. Figure 1 shows that three out of the top five 1986 gate array suppliers are large, broad-based Japanese companies. Toshiba had a large number of designs go to production and went from eighth position in 1985 to fourth in 1986.

Figure 1

Estimated Worldwide Gate Array Shipments
Top 10 Suppliers—Total



Source: Dataquest
October 1987

Gate Array Suppliers

During 1986, worldwide MOS gate array consumption increased 49 percent compared to 1985, while bipolar gate array consumption rose 23 percent. North American companies shipped 46 percent of the total worldwide gate arrays while Japanese companies shipped 45 percent. However, Japanese companies had 43 percent of their shipment revenue generated from intracompany sales (sales to internal divisions) while North American companies only had 11 percent intracompany sales. The yen-to-dollar exchange rate also increased the market share of Japanese companies by changing from 238 in 1985 to 167 in 1986. This newsletter will address the following key areas:

- Preliminary 1986 company shipment estimates
- Technology forecast
- Design starts
- Merchant revenue versus intracompany revenue
- NRE and device pricing
- Regional trends

PRELIMINARY 1986 GATE ARRAY RESULTS

Dataquest Definitions

Dataquest defines the commonly used terms as follows:

- Gate arrays—These are digital or linear/digital integrated circuits containing a configuration of uncommitted elements customized by interconnecting one or more routing layers.
- NRE—These are nonrecurring engineering charges or simply the cost of developing the array.
- Intracompany revenue—When an IC manufacturer takes a product line, which was developed and produced for internal consumption, to the merchant market, the revenue associated with this internal consumption is called intracompany revenue; the revenue from sales to outside companies is called merchant revenue.
- Dataquest gate array shipments—The shipment revenue equals the estimated production revenue plus intracompany revenue plus NRE revenue.

Gate Array Suppliers

Total Gate Arrays

As Figure 1 indicates, Fujitsu is the leader in total gate array revenue. Fujitsu is number two in MOS gate arrays and number one in bipolar arrays as shown in Tables 1 and 2, respectively. However, one must consider that a large portion of Fujitsu's revenue comes from sales to its own divisions. LSI Logic came in number two in total gate arrays with an exclusive MOS product line. NEC remains in third place with a healthy 54 percent increase in 1986 sales over 1985. Toshiba is climbing the top 10 supplier roster at a rapid rate, going from number eight in 1985 to number four in 1986. The next six suppliers are in a close race for market share. The top 10 suppliers in 1986 shared 65 percent of the total available market (TAM). During 1985, the top 10 suppliers shared 61 percent of the TAM. This comparison shows that the top 10 suppliers are gaining market share at the expense of the smaller suppliers.

However, it should be noted that even as the dedicated gate array suppliers are battling for valuable market share, there are other vendors whose primary business is either specialty arrays or another ASIC technology in addition to gate arrays. For example, Laserpath Corp. provides one-day quick turnaround of gate arrays, and VLSI Technology Inc. (VTI) is primarily a cell-based design company but can also do MOS gate arrays with its sophisticated design tools.

Table 1

Estimated 1986 Worldwide Gate Array Shipment Revenue—MOS (Millions of Dollars)

1985 Rank	1986 Rank	Company	1985 Revenue	1986 Revenue
1	1	LSI Logic	$140.0	$192.0
2	2	Fujitsu	101.3	145.0
4	3	Toshiba	45.6	120.0
3	4	NEC	49.0	72.0
7	5	Oki	28.0	49.0
5	6	Sieko	33.8	48.0
6	7	Hitachi	29.1	45.0
8	8	Gould AMI	25.0	27.0
22	9	Honeywell	7.0	27.0
9	10	Hughes	19.2	22.0
Total			$478.0	$747.0

Source: Dataquest
October 1987

Gate Array Suppliers

Table 2

Estimated 1986 Worldwide Gate Array
Shipment Revenue—Bipolar
(Millions of Dollars)

1985 Rank	1986 Rank	Company	1985 Revenue	1986 Revenue
1	1	Fujitsu	$120.1	$164.0
2	2	Motorola	68.4	82.6
3	3	NEC	45.0	73.0
5	4	Fairchild	39.8	47.7
4	5	Honeywell	42.0	45.0
6	6	Ferranti Electronics	29.0	38.0
7	7	Hitachi	29.0	34.0
10	8	Siemens	23.4	26.0
8	9	Signetics	28.8	26.0
9	10	Texas Instruments	27.5	24.7
Total			$453.0	$561.0

Source: Dataquest
October 1987

MOS Gate Arrays

As Table 1 indicates, LSI Logic maintained its number one position in MOS gate arrays with a 37 percent growth in 1986 over 1985. However, Toshiba had a large number of designs go to production and it increased sales by an estimated 163 percent. Fujitsu captured many new designs in 1986 and remains in second place. Oki is gaining market share by capturing lower-density designs with high-production volumes. Four of the top 5 MOS suppliers are Japanese companies. The top 10 MOS suppliers accounted for 69 percent of the total 1986 MOS market, compared to 66 percent in 1985.

Bipolar Gate Arrays

The ECL market continues to flourish while the TTL market fades. Mainframe computers are large consumers of ECL arrays. Fujitsu, Motorola, NEC, Fairchild, and Honeywell are the key suppliers to the mainframe manufacturers. These top 5 ECL suppliers shared 74 percent of the $412 million 1986 ECL market. AMCC is also a supplier of ECL arrays and had sales of 24 million dollars mainly in the military and industrial markets. Ferranti Interdesign and Exar dominate the North American linear

and mixed linear/digital array markets. It is interesting to note that only 2 of the top 5 bipolar array suppliers shown in Table 2 are Japanese companies. The top 10 bipolar suppliers shared 78 percent of the total 1986 bipolar market, compared to 77 percent in 1985. This is a capital-intensive mature market dominated by large IC suppliers.

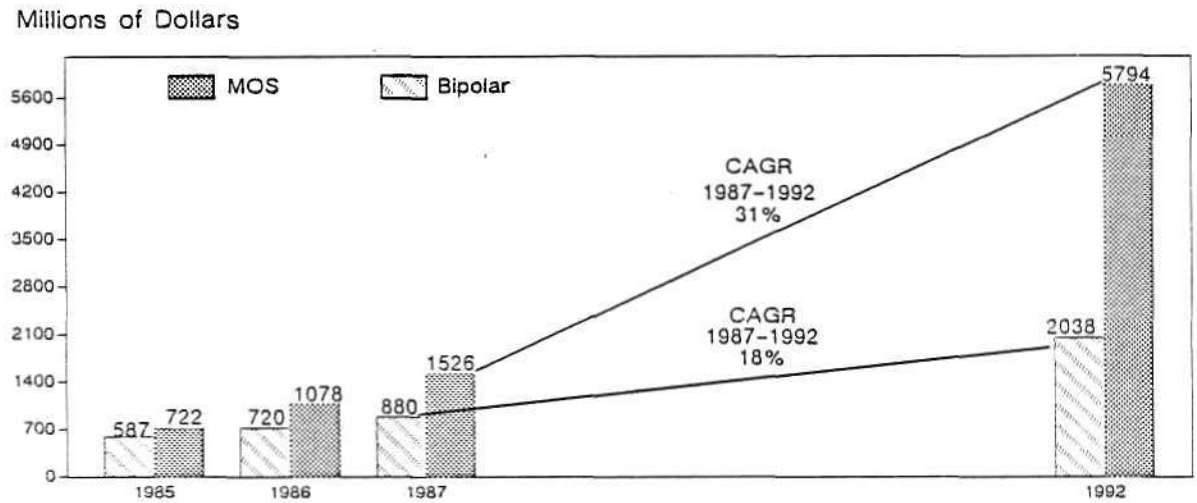
GATE ARRAY SUPPLIERS POSITION FOR FUTURE GROWTH

The worldwide gate array market is expected to increase from $1.8 billion in 1986 to $7.8 billion by 1992. Figure 2 illustrates that by 1992 the MOS market will dominate with a $5.8 billion market followed by the $2 billion bipolar market. The compounded annual growth rates from 1987 through 1992 for the MOS and bipolar gate array markets shown in Table 3 are 31 percent and 18 percent, respectively.

During 1986, the MOS portion of the gate array market increased 49 percent compared to 1985, while the bipolar market experienced a more modest 23 percent growth. Most of the bipolar growth was attributed to ECL arrays with a 32 percent rise in 1986 consumption compared to 1985. Please remember that shipments and consumption include NRE, intracompany, and production. The yen-per-dollar exchange rate applied in 1985 was 238 and 167 in 1986.

Figure 2

Estimated Worldwide Gate Array Consumption by Technology



Source: Dataquest
October 1987

Gate Array Suppliers

Table 3

Estimated Worldwide Gate Array Consumption
by Technology
(Millions of Dollars)

	1985	1986	1987	1988	1989	1990	1991	1992
Total	1,308.5	1,797.8	2,406.5	3,163.9	3,773.6	4,851.2	6,175.4	7,832.2
Total MOS	721.6	1,078.0	1,526.4	2,102.0	2,563.9	3,406.3	4,459.0	5,793.9
MOS Digital	704.1	1,057.0	1,500.9	2,071.3	2,527.0	3,360.9	4,402.8	5,723.6
MOS Linear	17.5	21.0	25.4	30.7	36.9	45.4	56.3	70.3
Total Bipolar	586.9	719.8	880.2	1,061.9	1,209.7	1,444.9	1,716.4	2,038.3
Bipolar Digital	516.9	646.8	801.3	977.5	1,120.3	1,351.3	1,618.7	1,937.7
TTL	135.9	154.1	169.5	178.0	176.2	172.7	164.0	150.9
ECL	313.6	412.6	540.5	697.3	836.7	1,071.0	1,349.4	1,686.8
Other	67.4	80.1	91.3	102.3	107.4	107.4	105.2	100.0
Bipolar Linear	70.0	73.0	78.8	84.4	89.4	93.9	97.6	100.6

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
October 1987

Most gate array suppliers are currently sacrificing today's profits for increased market share. During 1986, device pricing as well as NRE charges decreased in CMOS gate arrays to the point where most suppliers experienced small profits or even losses. Suppliers want to gain as much market share as possible so that they will be able to capitalize on the $7.8 billion market in 1992. NRE charges and device pricing will be addressed later in this newsletter.

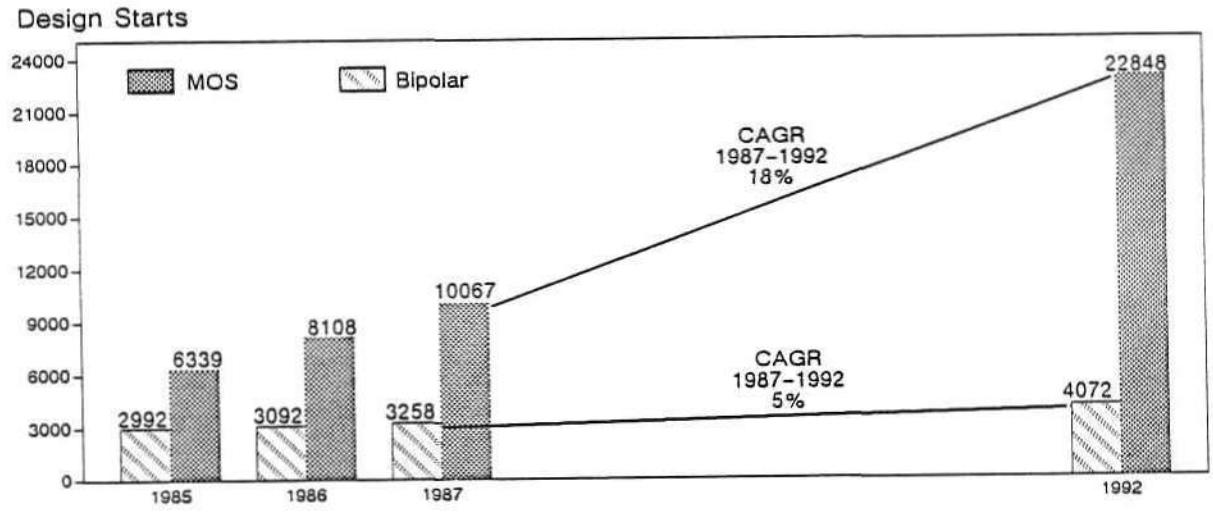
DESIGN STARTS DETERMINE FUTURE GROWTH

Design starts are a leading indicator of future gate array revenue. Figure 3 illustrates that there were 11,200 total design starts in 1986 and we expect 26,920 total design starts in 1992. During 1986, MOS gate array design starts grew an estimated 28 percent compared to 1985, while bipolar design starts grew only 3 percent. This low growth rate in bipolar arrays can be attributed to the fact that TTL designs are being phased out while the number of ECL designs are increasing. Dataquest analysis indicates that designs captured in 1986 will take an average of 6 to 12 months to reach the production phase. Thus, a high number of designs in 1986 will result in high production revenue in 1987. However, the percentage of designs that ultimately reach production phase can vary widely. Our analysis indicates that the percentage of designs that go to production for the industry ranges from 30 percent during a depressed semiconductor economy to 70 percent in a thriving semiconductor economy.

Gate Array Suppliers

Figure 3

Estimated Worldwide Gate Array Design Starts by Technology



Source: Dataquest
October 1987

Table 4 shows the number of designs captured in 1985 and 1986 by companies from each region. During 1986, North American companies experienced a 22 percent increase in MOS designs and an 11 percent decrease in bipolar designs. Part of the decline in bipolar designs can be attributed to the shift from TTL designs to ECL designs. However, Japanese companies grew 37 percent in MOS designs while increasing 22 percent in bipolar designs, which indicates that Japanese companies will gain market share in both the MOS and bipolar gate array markets during the next two years.

Table 4

Estimated Worldwide Gate Array Design Starts
by Region

	1985	1986
Worldwide Total	9,331	11,200
MOS	6,339	8,108
Bipolar	2,992	3,092
North American Companies	4,924	5,439
MOS	3,184	3,885
Bipolar	1,740	1,554
Japanese Companies	3,297	4,389
MOS	2,429	3,334
Bipolar	868	1,055
Western European Companies	1,041	1,272
MOS	657	789
Bipolar	384	483
ROW	69	100
MOS	69	100
Bipolar	0	0

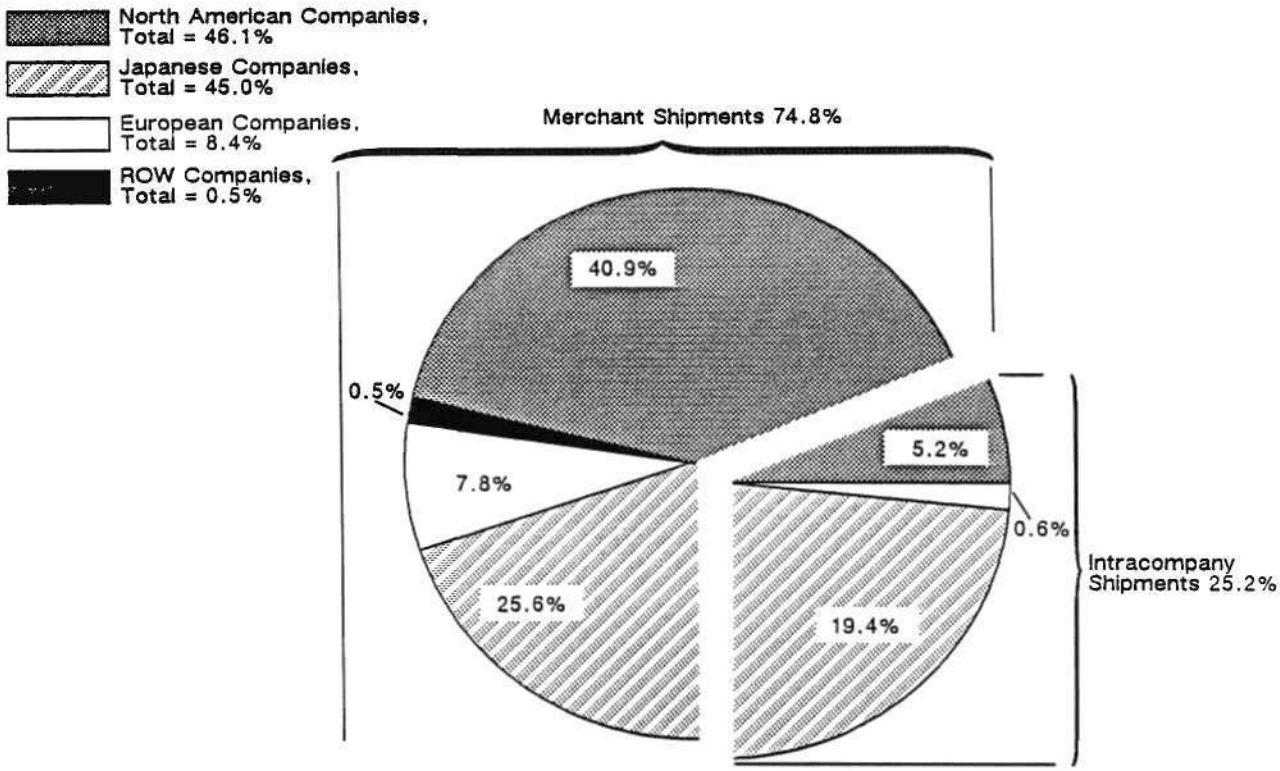
Source: Dataquest
October 1987

MERCHANT REVENUE VERSUS INTRACOMPANY REVENUE

It is important to examine the source of revenue when exploring regional trends. There was 25.2 percent intracompany revenue in the total 1986 worldwide gate array market as shown in Figure 4. Japanese companies had 43 percent of their 1986 worldwide revenue generated from sales to internal divisions compared to only 11 percent for North American companies. During 1986, Japanese companies had 77 percent of the $453 million intracompany market and 35 percent of the $1,345 million merchant market. North American companies had 21 percent of the intracompany market and 55 percent of the merchant market. Intracompany markets are less volatile and less vulnerable to outside competition. However, Figure 4 shows that the combined intracompany and merchant revenue for North American companies and Japanese companies is 46.1 percent and 45 percent, respectively.

Figure 4

Estimated 1986 Intracompany and Merchant Worldwide Shipments by Region



Source: Dataquest October 1987

MARKET TRENDS

Fierce competition from the more than 100 gate array suppliers produced the following trends:

- Amortized or low NRE pricing
- Declining device pricing
- Increased offshore manufacturing and consumption

Gate Array Suppliers

NRE Pricing

Suppliers are experimenting with different NRE strategies. Some suppliers try to minimize the up-front NRE charge and amortize the cost of the design over production volume. This can be risky since some designs never go to production. Japanese companies in Japan charge low or zero NRE and require a production order. At the other extreme is the supplier that charges NRE and production cost separately, making each part self-reliant. Between these extremes are various combinations of NRE and production charges that may not represent the true cost of either part. In today's North American market, an increasing number of companies are offering NRE below cost and amortizing the cost of the design over the production volume.

Pricing on NRE for low-density CMOS arrays declined drastically in 1986. During 1985, 1,500-gate CMOS devices had a typical NRE charge of $25,000 to $30,000. In late 1986, these same devices had an average NRE charge of $15,000 to $20,000. This can be attributed to the competitive environment brought about by the 60 to 70 suppliers offering comparable products.

Device Pricing

The price per device is difficult to estimate because prices vary widely due to technology, gate count, and packaging configurations. Thus, a CMOS 2,000-gate device may sell for as low as $3 in high quantities, while an ECL 2,500-gate device may sell for $170. A better way to monitor gate array pricing is on a price-per-gate basis. For benchmarking purposes, users should refer to the quarterly pricing data in the SUIS "Industry Trends" volume.

The most popular gate arrays (CMOS, 2,000 gates, die only, in quantities of thousands) took a sharp price-per-gate drop from between $0.01 and $0.012 in 1984, to between $0.002 and $0.004 in 1985. During 1986, the price per gate for these same devices fell to between $0.001 and $0.003. Higher gate count CMOS devices took a much smaller drop annually. The price per gate for ECL gate arrays only took an estimated 15 percent drop annually. Price decreases did occur in gate arrays, but not equally across all product lines.

Few suppliers can make a profit with pricing at $0.001 per gate.

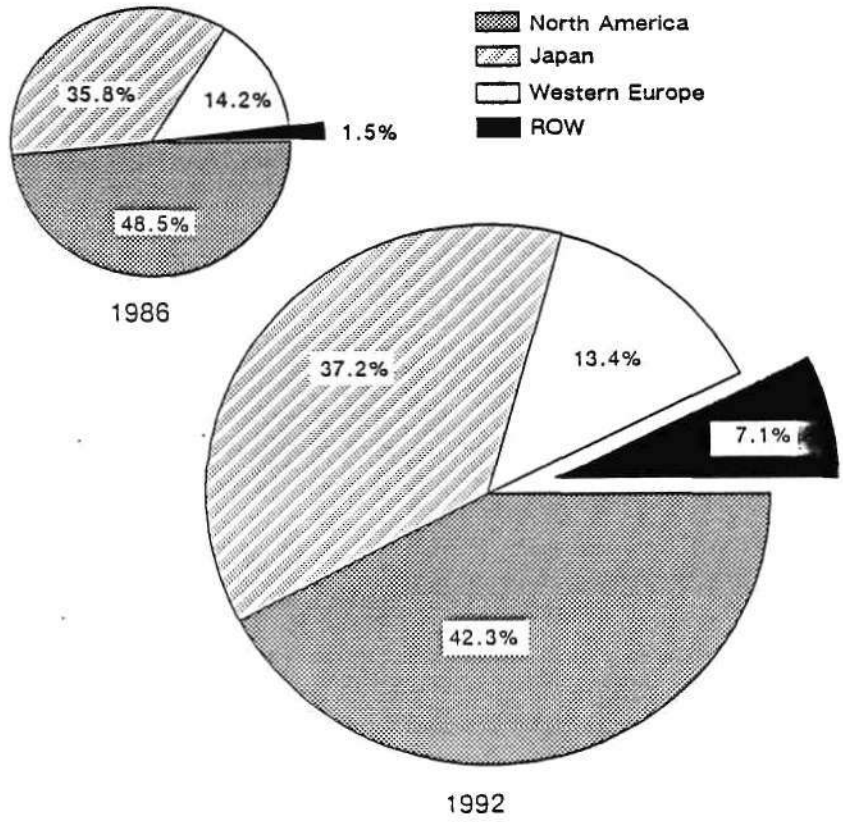
Offshore Manufacturing

The escalating value of the yen against other currencies is having a major impact on system manufacturers. This is especially true for those companies that make consumer electronics. In the highly competitive consumer electronics market, building the product at the lowest possible cost can make the difference between success or failure. We see a strong shift of system manufacturing to the Asian Pacific basin. This is true for Japanese system companies as well as North American companies. Dataquest has noted in other publications that there is an increasing demand for all types of semiconductors

in Korea, Taiwan, Hong Kong, and Singapore. The Japanese Ministry of Finance reported that in 1986, Japan exported 498 million ICs to the United States while also exporting 444 million units to Korea, 442 million to Taiwan, and 481 million to Hong Kong. The trend in gate arrays is no different. Figure 5 illustrates that Dataquest expects the consumption of gate arrays in Rest of World (ROW) to increase from 1.5 percent in 1986 to 7.1 percent in 1992.

Figure 5

Estimated Worldwide Gate Array Consumption by Region



Source: Dataquest
October 1987

Gate Array Suppliers

DATAQUEST CONCLUSIONS

Suppliers need to position their design wins to capitalize on their strengths while avoiding major competition. We expect Japanese companies in the North American market to continue focusing on capturing lower-density, high-volume CMOS gate array designs as well as high-density ECL designs. North American companies are expected to focus more on capturing high-density CMOS designs and the full range of ECL designs. The gate array market is now dominated by large IC suppliers. The data suggest that Japanese companies will gain market share in both the MOS and bipolar gate array markets over the next two years. We expect 1987 to be the year of truth for the small gate array suppliers. They must decide which path to take: move to a niche market, look to be acquired, or retreat from the market altogether.

Food for Thought

In summary, being careful means understanding all of the subtle nuances involved in these market evolutions. Indeed, your requirements as users may mean seeking the best combination of price, technology, and supplier market position (or the importance of alternate sourcing). Here then, are several primary issues to consider:

- Prices have been decreasing and are forecast to continue dropping. NRE charges are also decreasing and some suppliers may eliminate them to draw business.
- Due to the competition, the gate array market is undergoing changes that will force realignments among surviving suppliers.
- ASIC vendors that are either special service companies or do gate arrays in addition to other design approaches should be considered.
- CMOS technology will be the process of choice in mainstream suppliers' portfolios.
- Japanese companies are serious about doing business. They will compete aggressively since they are broad-based suppliers and are targeting this market.

1987 Custom Integrated Circuit Conference

OVERVIEW

With a conference as large and diverse as the 1987 Custom Integrated Circuits Conference (CICC), there is a temptation to evoke images of a flagship and an armada of great ships searching the seas for new worlds. At the head of the fleet is the flagship, which represents the essence of the fleet. Following is a vast convoy of ships, each representative of the remarkable diversity of ASIC technology. There are ships that specialize in CAD tools, ships that specialize in certain ASIC products, and ships that specialize in certain technologies. The flagship is like the CICC in that it represents all that is ASICs.

This event continues to attract over 1000 attendees and offers the ASIC technical community the best place to learn and to exchange views. CICC has been an annual event for nine years; over those years it has grown to represent some of the best ideas from around the world. Table 1 shows a steady growth in the number of papers presented across the industry, academic, and government communities. This year was no exception. There were 14 countries represented, 360 papers were submitted, and 170 papers were accepted. The technical committee continues to experiment with new ways to disseminate new information. For example, this year there was an informal evening session on emerging products.

The intent of this newsletter is not to detail all that goes on at the CICC, but to highlight five important topics that remain after adjournment:

- The changes in regional representation
- The technical innovations
- The characterization of cells
- The current state of the Electronic Design Interchange Format (EDIF)
- The emergence of quick ASIC

Table 1

CICC PAPERS BY INSTITUTION

	1984	1985	1986	1987
Industry	101	89	112	138
Academic	19	25	42	34
Government	1	2	2	8
Total*	121	116	156	180

*Totals exceed actual number of papers due to coauthors' overlapping in the categories.

Source: Dataquest
September 1987

SHIFT IN REGIONAL REPRESENTATION

Table 2 shows the international flavor of the conference and suggests some important trends. While the total number of papers continues to grow, it is particularly noteworthy that the number of Japanese participants nearly doubled. Toshiba and Hitachi each published seven papers, followed by three papers from Fujistu and three from NEC. But unlike their North American or European counterparts, the Japanese suppliers are concentrating on different areas. It is also noteworthy that these companies are focusing on testing, fault grading, and simulation (an area that has been considered the Achilles heel of ASIC).

It is widely known that ASIC products are not tested as thoroughly as standard products. This is largely because developing complete fault coverage has been time-consuming and very expensive. Also, most ASIC chips are not sold in unit volumes that match most standard products. Therefore, one must conclude that ASIC cannot support the effort required to achieve higher fault coverage. We believe that the Japanese ASIC suppliers are particularly sensitive to this issue. This is not to say that the North American or European suppliers have ignored testing problems; rather, they have concentrated on other design problems. Dataquest believes that the sharp increase in the number of Japanese papers reflects a strategic thrust in the this area. We believe that Japanese companies, over the next three years, will try to differentiate their product by offering more thoroughly tested product.

Table 2

CICC PAPERS BY COUNTRY OF ORIGIN

Region	1984	1985	1986	1987
North America	97	87	114	122
Europe	7	17	23	27
Japan	14	11	12	22
Rest of World	3	1	1	1
Total*	121	116	150	172

*Totals exceed actual number of papers due to coauthors' overlapping in the categories.

Source: Dataquest
September 1987

TECHNOLOGICAL INNOVATIONS

Because of the diversity of this conference, it is difficult to single out specific papers that reflect the state of the art. Nevertheless, two papers stand out. The first was a gate array paper from Motorola. This paper reported on the design of a 0.5-micron CMOS 150,000-gate channelless gate array. Funded under a VISIC contract, the 350-millimeter die represents one of the largest gate arrays yet. It uses three-layer metal and platinum silide; the lithography was done using a direct-write E-beam system. While a working part is not available, the Motorola team expects to have parts by the end of 1987 or early 1988.

The second paper discussed a wafer-scale 170,000-gate fast fourier transform processor on a four-inch wafer. Fujitsu Laboratories developed the processor using a 2.3-micron process and configurable building blocks. The implementation has 750 input and output pads and includes built-in test circuitry.

CHARACTERIZATION AND COMPILERS

The sessions on cell characterization and compilers were well attended. Developing cells for a cell-based IC (CBIC) library is a challenge that most designers welcome, but the tedious task of characterizing each cell is time-consuming and expensive. Furthermore, as new applications are encountered more cells must be added to the library. So it must seem to the engineer who is charged with this task that characterization is an endless task. Most engineers that we talked to were looking for ways to expedite the characterization process. They were especially concerned with the characterization as it related to silicon compilers. Picking the proper parameters to characterize was highest priority. We believe that herein are the seeds for a new niche market. Providing CAD tools that accelerate characterization may be the next "boutique" CAD market. From the CAD suppliers' point of view, the challenge is how to expand existing products to support characterization or to develop standalone systems.

EDIF CONTINUES TO LANGUISH

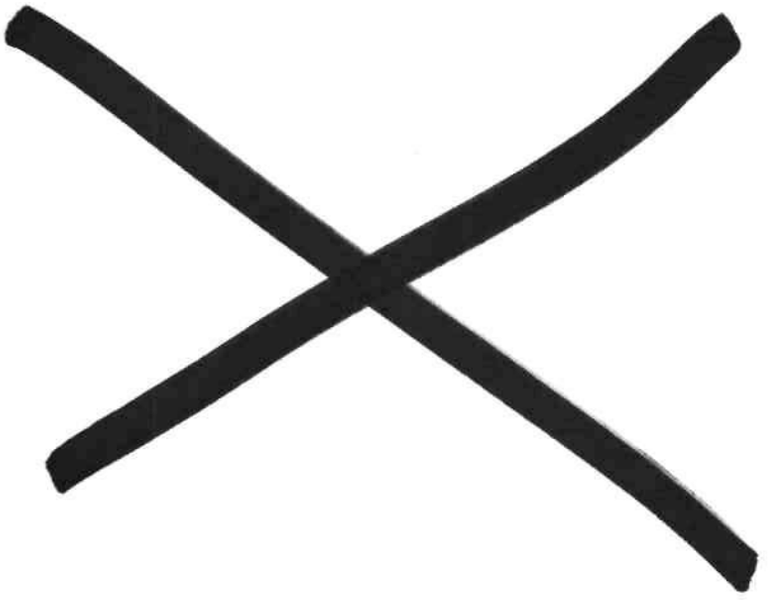
Each year the ASIC community comes to the CICC to hear how important it is to have industry-wide standard CAD interface and each year it continues to receive only lip service from ASIC suppliers. For nearly four years the Electronic Design Interchange Format (EDIF) has been hailed as just what the users and suppliers need: a standardized method of exchanging ASIC data. But unfortunately, very few of the major ASIC suppliers support a standard. We believe that this is largely because they perceive EDIF as a threat. This threat stems from competition between large and small ASIC suppliers. First, most of the young, less-established suppliers have nothing to lose and everything to gain by endorsing EDIF. EDIF can be considered as a vehicle that lowers the barriers to entry into a market. Thus many large ASIC suppliers view EDIF with mixed feelings. They would like an industry standard, but at the same time they perceive the standard as a disguised threat to their market position. The result is that EDIF receives the full support of most emerging companies and a few major companies, but only partial endorsement from the remaining major suppliers. What is needed to give EDIF universal endorsement? The answer is the user. Only strong and persistent endorsement by the user community will make EDIF a real standard. Dataquest strongly encourages its user clients to seriously consider this standard.

QUICK ASIC REVISITED

For some time, Dataquest has been monitoring the emerging quick ASIC market. This latent market was defined in a March 1986 newsletter as any product that could be delivered in less than two weeks at a very nominal cost. CICC 1987 devoted a session to this emerging market. Two products were PLDs and two were laser-based. Xilinx presented a paper on a RAM-based PLD and Intel's paper discussed a bus-oriented PLD. In the laser category, VLSI Technology (in conjunction with Elron) presented a paper on laser etching of gate arrays; Laser Path presented an informal paper on its gate array. It was also learned that Texas Instruments is planning to launch a family of 1.2-micron CMOS quick-turn gate arrays that could be delivered in two weeks. All five products received rapt attention from the user community. We believe that users want to reduce the time and perceived cost to produce all quick ASIC products.

NEXT YEAR WILL BE TEN YEARS!

Next year the CICC returns to Rochester, New York, for its tenth anniversary. The flagship has come a long way. What events will unfold in the next 10 years? Will we see a billion-transistor ASIC? Will silicon compilers fulfill their destiny? Will we see custom chips manufactured on a desktop? No one can be certain, but the voyage will certainly be exciting, challenging, frustrating, and very rewarding.



CAD Tools/AI

SUMMARY

DATAQUEST recently completed its first annual CAD/CAM end-user survey in Japan. The purpose of the survey was to gain insight from users currently using CAD/CAM systems. The survey questions closely paralleled those asked in DATAQUEST's U.S. survey administered early in 1985 (see DATAQUEST's CCIS newsletter No. 84 entitled, "1985 CAD/CAM User Survey Results") and was designed to detect similarities and differences in the two geographical regions.

DATAQUEST surveyed end users using products from the following CAD/CAM vendors in Japan:

- C. Itoh Data Systems (U.S. affiliation: Calma)
- Cadam
- Fujitsu
- Marubeni Hytech (U.S. affiliation: Applicon, Ecad, Zycad)
- Mentor Graphics
- NEC
- Sekio Instruments & Electronics (U.S. affiliation: Daisy Systems, McAuto, Zuken)
- Technodia (U.S. affiliation: Valid Logic)
- Tokyo Electron (U.S. affiliation: Computervision)
- Toshiba

In 1984, these ten vendors accounted for $441 million in Japanese CAD/CAM revenue (60 percent of total 1984 Japanese CAD/CAM revenue) and 3,685 installed 1984 total workstations shipped in Japan (48 percent of total installed Japanese workstations).

The 1,200 questionnaires were mailed to the CAD/CAM system managers at these installations (sites), and 397 (33 percent) were returned and used in compiling the results. The sum of the workstations at these sites totaled 4,644 units.

CAD Tools/AI

SURVEY FOCUS

DATAQUEST chose the following five major issues as the focus of this survey:

- Survey demographics--By industry classification, by type of applications, and by system usage
- Penetration--Number of workstations installed, percentage of trained users, trained users per workstation, number of engineers and draftsmen per site, engineers and draftsmen per workstation, the use of standalone workstations, and the use of color workstations
- Personal computer use in CAD/CAM
- Pricing expectations for workstations relative to the following parameters: main memory, disk storage, screen resolution, screen size, and preference for either color or monochrome screen
- Solids modeling in CAD/CAM

SURVEY DEMOGRAPHICS

Industry Classification

Those surveyed were asked to identify the one industry classification from the following list that best described the type business in which their company was engaged:

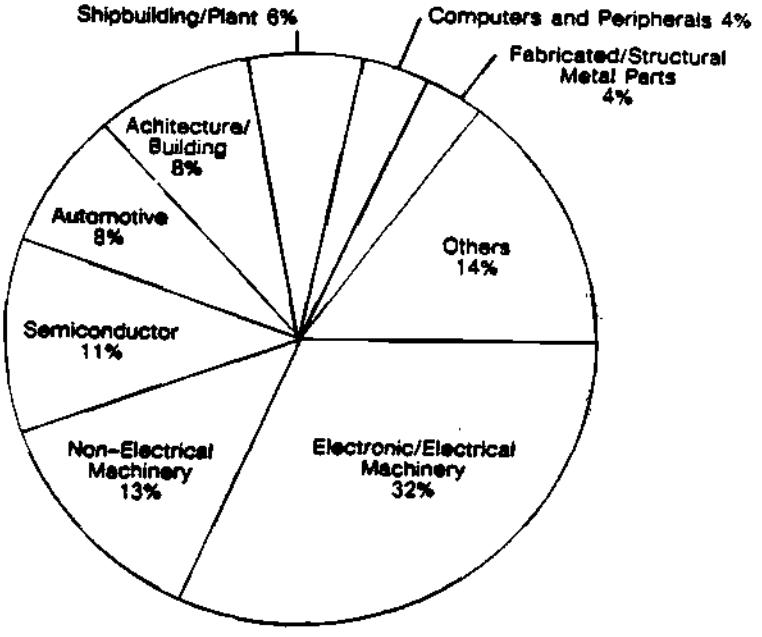
- Aerospace
- Architecture/building
- Automotive
- Chemical and allied products
- Computers and peripherals
- Electrical/electronic machinery, equipment, and supplies
- Fabricated/structural metal parts

- Iron and steel
- Mapping
- Metalworking
- Semiconductor
- Shipbuilding/plant
- Telecommunications
- Transportation (other than aerospace and automotive)
- Other (to be specified)

The distribution of respondents for each industry is shown in Figure 1. Electrical/electronic machinery, equipment, and supplies was the largest response group with nearly one-third of all responses.

Figure 1

INDUSTRY CLASSIFICATION
(Percent of Respondents)



Source: DATAQUEST February 1986

The only major difference in the CAD/CAM industrial distribution between Japan and the United States is the aerospace industry. The U.S. aerospace industry has been one of the largest and most aggressive groups to implement CAD/CAM technology. Without any appreciable number of companies in this area, Japan obviously does not have this market opportunity.

Applications

Those surveyed were asked to check all applications from the following list that were being performed at their site:

- Architecture, engineering, and construction/2D (AEC/2D)
- Architecture, engineering, and construction/3D (AEC/3D)
- Mechanical/2D (MECH/2D)
- Mechanical/3D (MECH/3D)
- Computer-aided manufacturing (CAM)
- Printed circuit board physical layout (PCB)
- Integrated circuit physical layout (IC)
- Electronic design automation (EDA/CAE)
- Technical publications (T-Pubs)
- Mapping

The distribution of respondents for each application is shown in Figure 2. Table 1 shows the respondents for each application by industry. As expected, mechanical applications dominate, with more than 60 percent of the respondents indicating that they perform some mechanical CAD/CAM work. The distribution illustrated in Figure 2 closely parallels the U.S. application distribution.

Figures 3 and 4 segment 2D and 3D usage for mechanical and AEC applications, respectively. Surprisingly, the use of 3D in AEC (52.7 percent) and mechanical (55.9 percent) was nearly equal. Nevertheless, DATAQUEST believes that 2D applications such as drafting still dominate when measuring the total elapsed time spent on a CAD/CAM workstation.

Figure 2

APPLICATIONS
(Percent of Respondents)

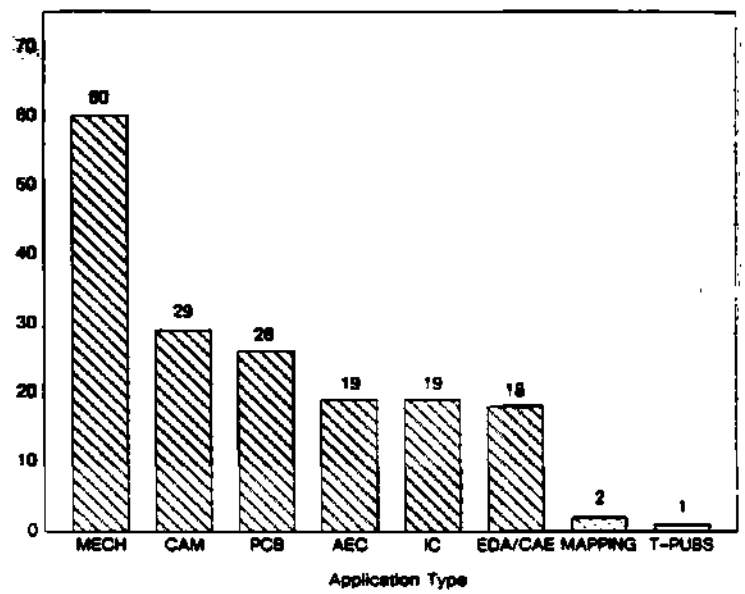


Table 1

APPLICATIONS BY INDUSTRY
(Percent of Respondents within Each Industry)

Industry	AEC	CAM	MECH	PCB	IC	EDA/CAE	T-Pubs	Mapping
Architecture/Building	87%	3%	20%	0%	0%	0%	0%	0%
Computers and Peripherals	0%	25%	63%	50%	25%	44%	0%	0%
Electrical/Electronic Machinery	7%	37%	43%	53%	21%	23%	2%	0%
Fabricated/Structural Metal Parts	6%	63%	81%	6%	0%	0%	0%	0%
Non-Electrical Machinery	10%	22%	72%	14%	2%	2%	0%	0%
Semiconductor	0%	14%	10%	7%	74%	55%	0%	0%
Shipbuilding/Plant	76%	32%	72%	0%	0%	0%	0%	0%
Transportation including Aerospace & Automotive	2%	35%	72%	19%	5%	12%	0%	0%
Others	28%	28%	57%	21%	19%	13%	2%	11%

Source: DATAQUEST
February 1986

Figure 3

MECHANICAL APPLICATION USAGE

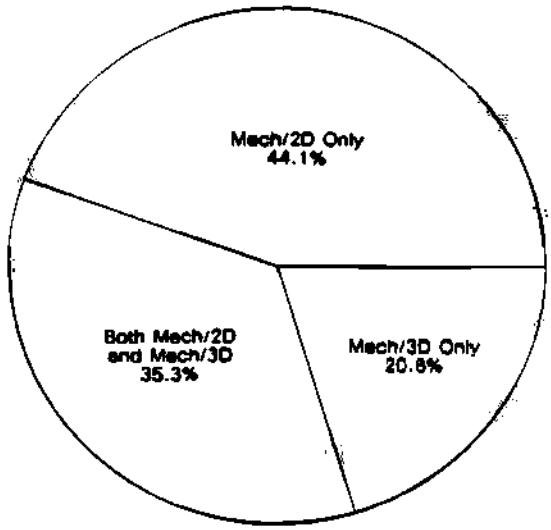
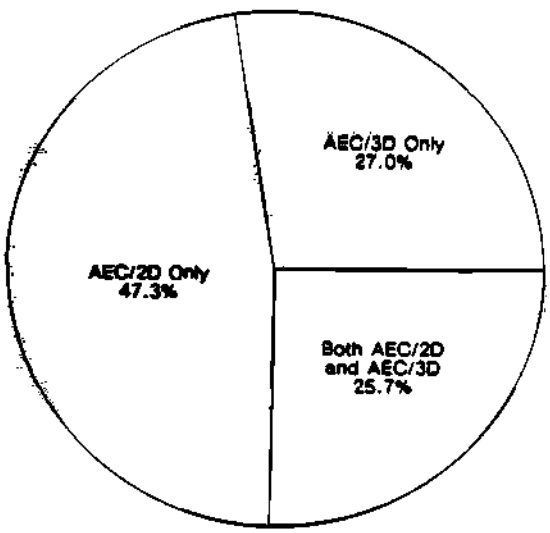


Figure 4

AEC APPLICATION USAGE



Source: DATAQUEST
February 1986

System Usage

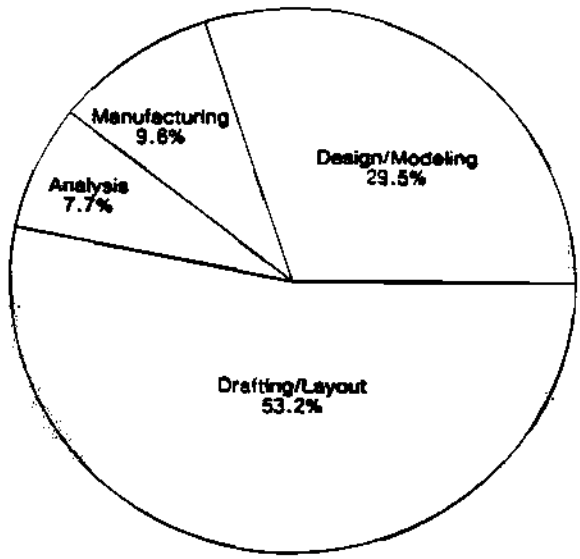
Respondents were asked to indicate system usage percentages among the four following system functions:

- Drafting/layout
- Design/modeling
- Analysis
- Manufacturing

Figure 5 breaks out the system usage categories across all respondents. Across the aggregate of respondents, drafting/layout represents an average of 53.2 percent of system usage followed by design/modeling (29.5 percent), manufacturing (9.6 percent), and analysis (7.7 percent). This usage mix is nearly identical to what was found among surveyed users in the United States. This is not unusual because a high percentage of Japanese CAD/CAM products are U.S.-sourced, and usage is highly dependent on system capabilities.

Figure 5

SYSTEM USAGE
(Averages)



Source: DATAQUEST
February 1986

PENETRATION

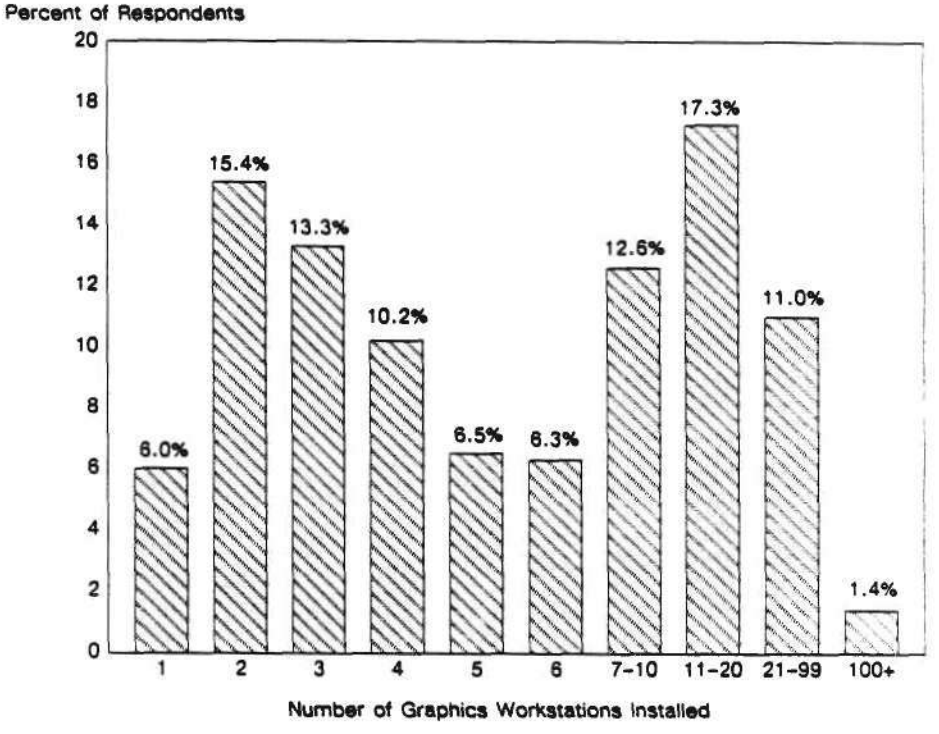
Number of Graphics Workstations Installed

Survey respondents were asked to indicate the number of graphics workstations they had installed at each site. The distribution of respondents by number of workstations installed is illustrated in Figure 6. Greater than half of all CAD/CAM workstations are installed at sites with five workstations or less. The largest single distribution (17.3 percent) is found at sites with between 11 and 20 workstations.

Table 2 lists the average number of graphics workstations installed, by industry. The semiconductor and transportation companies have the largest average number of graphics workstations installed (16) while companies in the fabricated structural/metal parts group had the smallest average number of installed workstations (6).

Figure 6

GRAPHICS WORKSTATIONS INSTALLED
(Distribution of Respondents)



Source: DATAQUEST
February 1986

Table 2

CAD/CAM WORKSTATIONS INSTALLED, BY INDUSTRY

Industry	Average Number
Semiconductor	16
Transportation including Aerospace & Automotive	16
Shipbuilding/Plant	13
Electrical/Electronic Machinery	12
Non-Electrical Machinery	12
Architecture/Building	7
Computers and Peripherals	7
Fabricated/Structural Metal Parts	6
Others	13
Industry Average	12

Source: DATAQUEST
February 1986

Trained Users/Workstation

DATAQUEST also asked survey respondents to indicate how many trained engineers and draftsmen share a single CAD/CAM workstation. The average number of users per workstation across the aggregate of respondents was 3.6. The distribution of respondents for the number of users per workstation is shown in Figure 7.

Table 3 lists the average number of trained users per workstation, by industry. The semiconductor industry has the highest number of users per workstation (4.3) while the fabricated/structural metal parts industry has the fewest number of users per workstation (2.3).

Figure 7

TRAINED USERS PER GRAPHICS WORKSTATION

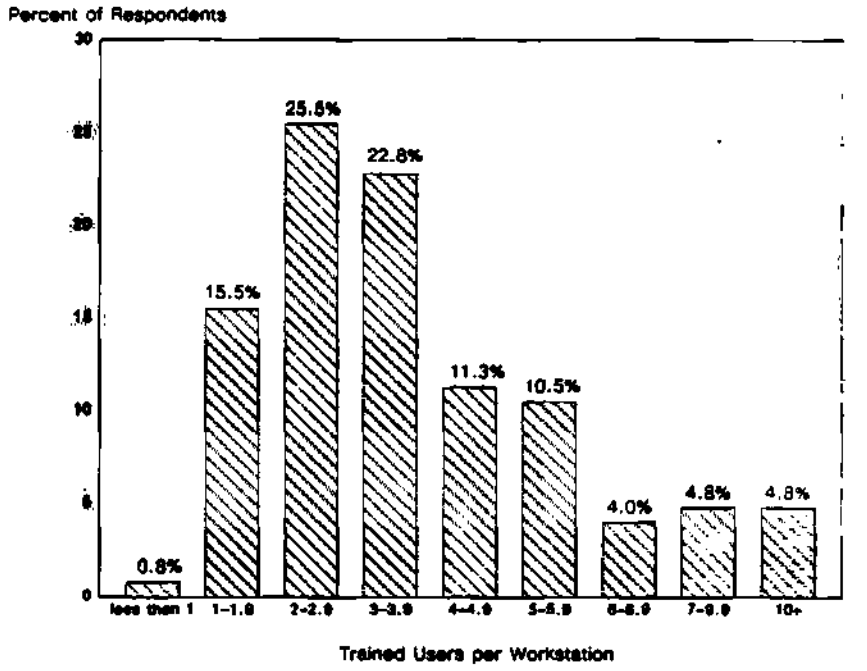


Table 3

TRAINED USERS PER INSTALLED WORKSTATION, BY INDUSTRY

Industry	Average Number
Semiconductor	4.3
Architectural/Building	4.1
Shipbuilding/Plant	3.9
Electrical/Electronic Machinery	3.6
Non-Electrical Machinery	3.5
Computers and Peripherals	3.4
Transportation Including Aerospace & Automotive	3.0
Fabricated/Structural Metal Parts	2.3
Others	3.2
Industry Average	3.6

Source: DATAQUEST
February 1986

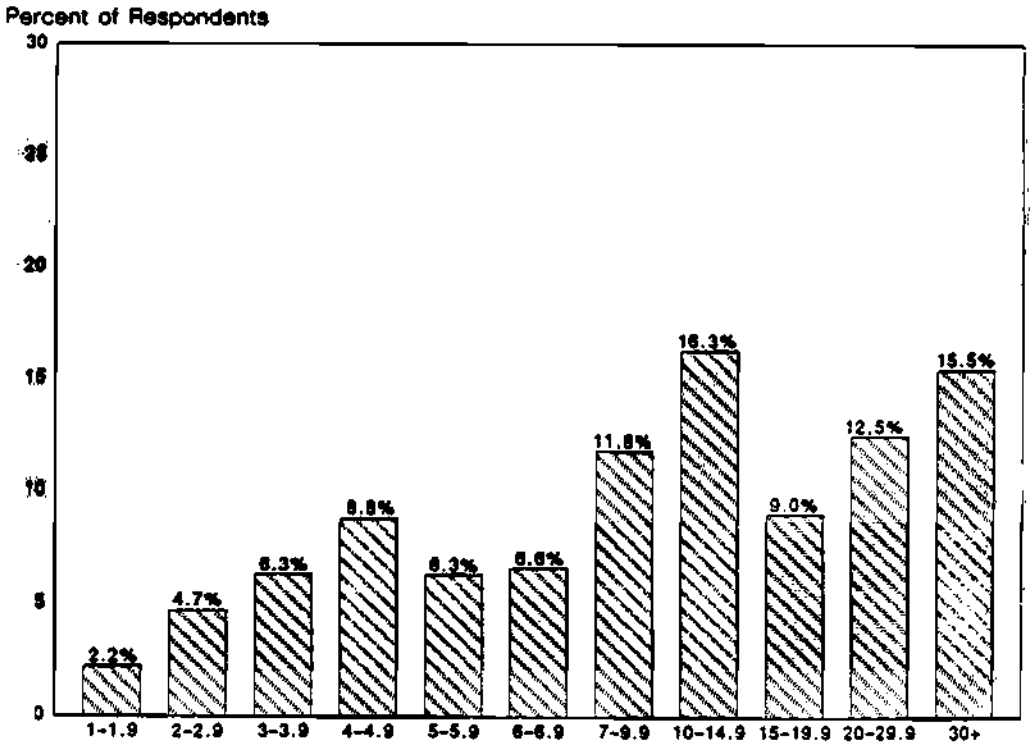
Engineers and Draftsmen/Workstation Penetration

DATAQUEST asked survey respondents to indicate the total number of engineers and draftsmen (trained and untrained) per workstation at their site. The average number of engineers and draftsmen per workstation across the aggregate of respondents was 18. Figure 8 illustrates workstation distribution by the number of engineers and draftsmen.

Table 4 lists the average number of engineers and draftsmen per workstation and the corresponding market penetration by industry. The fabricated/structural metal parts industry has the highest penetration of workstations (12.5 percent) while the architectural/building industry has the lowest (2.6 percent). DATAQUEST believes that the Japanese architectural/building industry has a much lower level of market penetration (2.6 percent) than the U.S. architectural/building industry (6.0 percent).

Figure 8

TOTAL ENGINEERS AND DRAFTSMEN PER GRAPHICS WORKSTATION
(Percent Distribution)



Source: DATAQUEST
February 1986

Table 4

AVERAGE OF ENGINEERS AND DRAFTSMEN PER WORKSTATION INSTALLED BY INDUSTRY

Industry	Average	Percent Penetration
Fabricated/Structural Metal Parts	9	12.5%
Semiconductor	10	10.0%
Computers and Peripherals	10	10.0%
Transportation Including Aerospace & Automotive	11	9.1%
Non-Electrical Machinery	15	6.7%
Shipbuilding/Plant	20	5.0%
Electrical/Electronic Machinery	21	4.8%
Architectural/Building	38	2.6%
Others	19	5.3%
Industry Average		6.0%

Source: DATAQUEST
February 1986

Use of Standalone Workstations

Those surveyed were asked to indicate how many standalone 32-bit engineering workstations versus host-dependent, shared-logic workstations they have installed. Figure 9 illustrates the split between these two system architectures. Figure 9 does not account for the use of personal computers. Standalone workstations account for only 10.6 percent of all installed workstations. However, DATAQUEST believes that this number will rise dramatically in the future since the new 32-bit, workstation-based systems (e.g., Apollo, Sun, MicroVAX) are just now beginning to gain favor in the Japanese market.

Table 5 shows the percentage of standalone workstations out of all workstations installed by industry. The semiconductor and computer industries account for approximately 50 percent of the installed standalone 32-bit workstation population.

Figure 9

HOST-DEPENDENT VERSUS STANDALONE GRAPHICS WORKSTATIONS

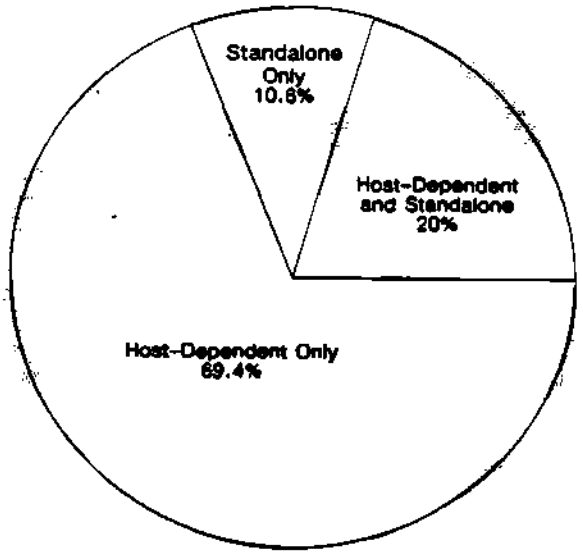


Table 5

STANDALONE GRAPHICS WORKSTATIONS INSTALLED, BY INDUSTRY
(Percent of Standalone Workstations)

Industry	Standalone Workstations
Semiconductor	25%
Computers and Peripherals	25%
Non-Electrical Machinery	15%
Shipbuilding/Plant	12%
Fabricated/Structural Metal Parts	12%
Electrical/Electronic Machinery	7%
Transportation Including Aerospace and Automotive	7%
Architectural/Building	2%
Others	6%
Industry Average	11%

Source: DATAQUEST
February 1986

Use of Color Workstations

Those surveyed were asked to indicate how many color workstations were installed as a percentage of all workstations at each site. The survey revealed that 42 percent of all workstations installed were color units. This compares quite closely to the 40 percent figure in the United States.

Table 6 shows the percentage of color workstations installed by industry. The semiconductor industry has the highest percentage of installed color workstations (64 percent), while the shipbuilding/plant design industry has the lowest (24 percent).

Table 6

COLOR WORKSTATIONS INSTALLED, BY INDUSTRY

Industry	Color Workstations
Semiconductor	64%
Fabricated/Structural Metal Parts	53%
Transportation Including Aerospace & Automotive	51%
Architecture/Structural	46%
Electrical/Electronic Machinery	44%
Computers and Peripherals	41%
Non-Electrical Machinery	27%
Shipbuilding/Plant	24%
Others	31%
Industry Average	42%

Source: DATAQUEST
February 1986

USE OF PERSONAL COMPUTERS IN CAD/CAM

Those surveyed were asked to indicate how many personal computers used for CAD/CAM were installed at each site. Additionally, they were asked who used the personal computers and whether or not they were networked. For those who did not have any personal computer-based CAD/CAM, we asked whether or not they had plans to use personal computers for CAD/CAM in the future.

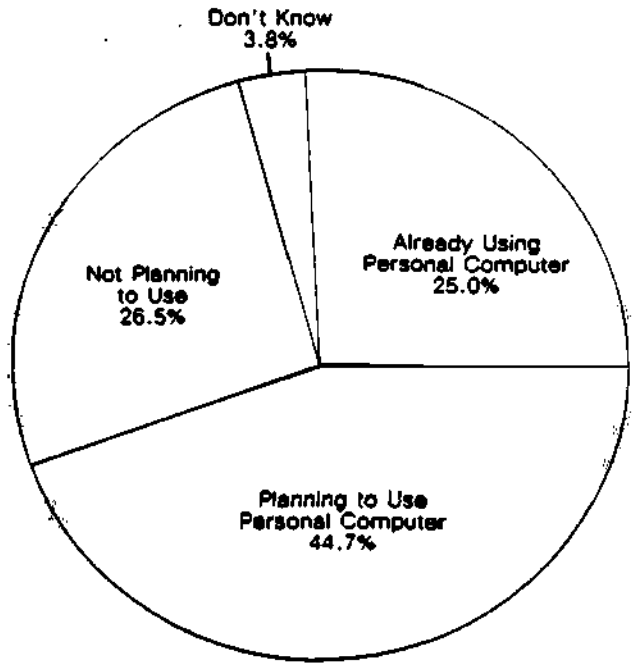
As Figure 10 illustrates, the findings indicate that 25.0 percent of the respondents are using personal computer-based CAD/CAM systems and an additional 44.7 percent are planning to use personal computers for CAD/CAM in the future. The 44.7 percent that plan to use personal computers in the future is much higher than the 30 percent who plan to use personal computers in the United States, which we found in our previous U.S. survey.

Figure 11 illustrates the types of professionals using personal computer-based CAD/CAM. Only 30.3 percent of the respondents indicated that engineers are using personal computers compared to more than 50 percent of those surveyed in the United States.

Table 7 lists our respondents' answers to personal computer use, by industry. The semiconductor industry leads all industry groups with a 90 percent approval rating for using personal computers. The fabricated/structural metal parts industry is least favorable toward personal computer-based CAD/CAM, with only a 50 percent approval rating.

Figure 10

PERSONAL COMPUTER USE IN CAD/CAM



Source: DATAQUEST
February 1986

Figure 11

ACTUAL PERSONAL COMPUTER USERS

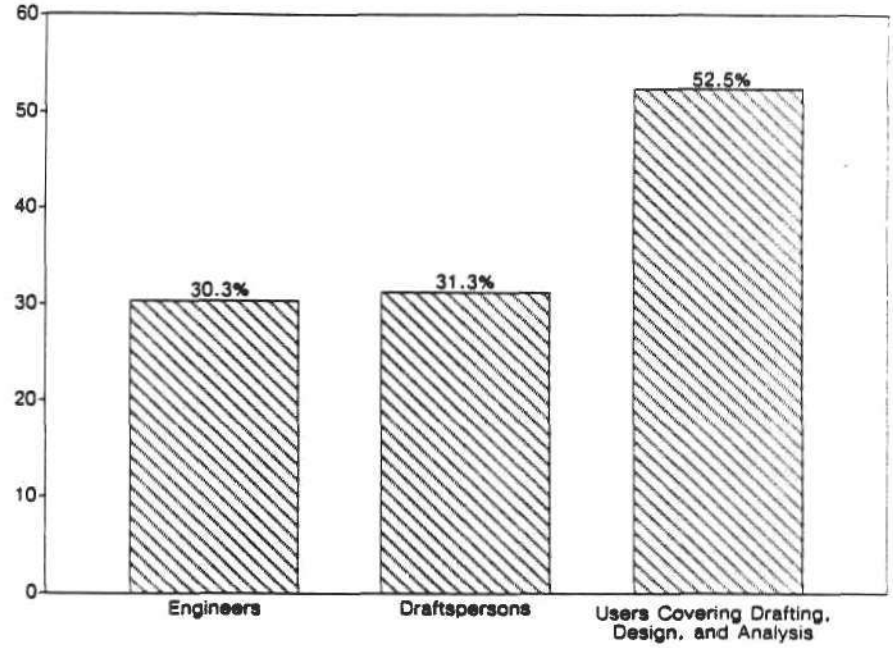


Table 7

PERSONAL COMPUTER USE, BY INDUSTRY
(Percent of Respondents)

Industry	Planning to Use	Already Using	Total
Semiconductor	43%	45%	90%
Shipbuilding/Plant	56%	32%	88%
Architecture/Building	55%	28%	83%
Electrical/Electronic Machinery	48%	25%	73%
Computers and Peripherals	41%	29%	70%
Non-Electrical Machinery	41%	14%	55%
Transportation Including Aerospace & Automotive	37%	14%	51%
Fabricated/Structural Metal Parts	44%	6%	50%
Others	34%	30%	64%

Source: DATAQUEST
February 1986

PRICING EXPECTATIONS FOR WORKSTATIONS

Those surveyed were asked to indicate the graphics workstation unit price from the following price levels that would enable them to install one workstation on every engineer's desk:

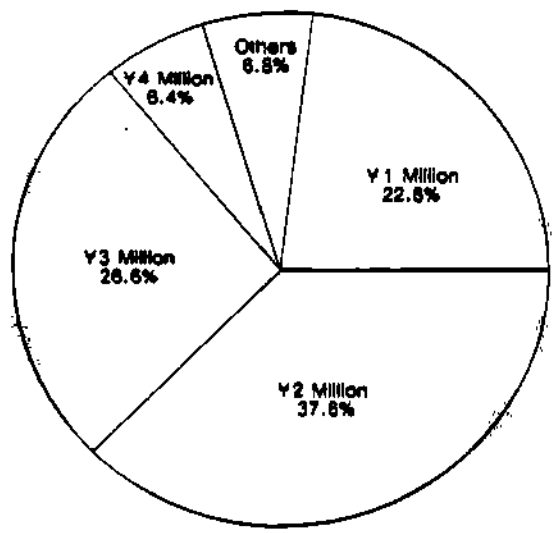
- ¥1 million ($4,200)
- ¥2 million ($8,400)
- ¥3 million ($12,600)
- ¥4 million ($16,800)
- Others (to be specified)

The findings revealed that 64 percent of those who responded wish to pay ¥2 million or less, with 37.6 percent of the respondents indicating ¥2 million as the ideal price. Figure 12 illustrates workstation price levels across the aggregate of respondents.

Respondents also indicated what an acceptable workstation configuration would be at the price level they indicated. Nearly 70 percent of all respondents indicated that color was necessary.

Figure 12

IDEAL PRICE FOR A WORKSTATION ON EVERY ENGINEER'S DESK



Source: DATAQUEST
February 1986

Figure 13 reveals the acceptable main memory capacity levels selected from the following memory capacity levels at ¥2 million:

- 0.5 Mbyte
- 1.0 Mbytes
- 2.0 Mbytes
- Others (to be specified)

Figure 14 reveals acceptable disk storage levels selected from the following disk storage levels at ¥2 million:

- 10 Mbytes
- 20 Mbytes
- 50 Mbytes
- 100 Mbytes
- Others (to be specified)

Figure 15 reveals acceptable screen resolution selected from the following resolution levels at ¥2 million:

- 512 x 512
- 640 x 512
- 1,024 x 1,024
- 1,280 x 1,024
- Others (to be specified)

Figure 16 reveals acceptable screen size selected from the following size levels at ¥2 million:

- 14 inch
- 17 inch
- 19 inch
- Others (to be specified)

Figure 13

ACCEPTABLE MAIN MEMORY AT ¥2 MILLION

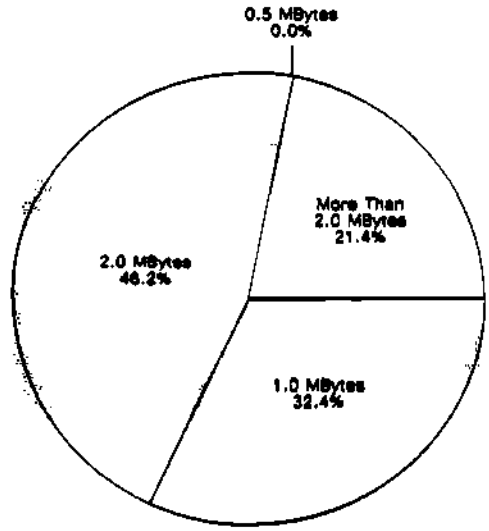
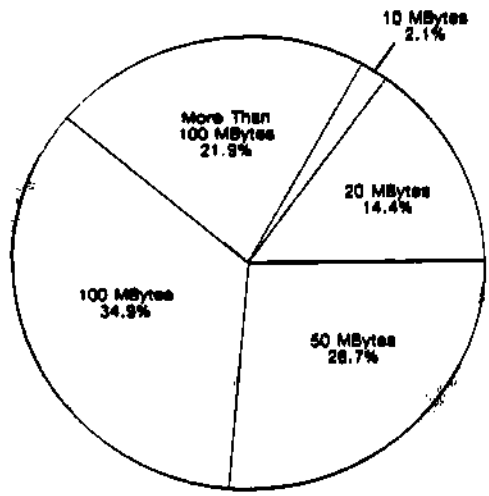


Figure 14

ACCEPTABLE DISK STORAGE AT ¥2 MILLION



Source: DATAQUEST
February 1986

Figure 15

ACCEPTABLE SCREEN RESOLUTION AT ¥2 MILLION

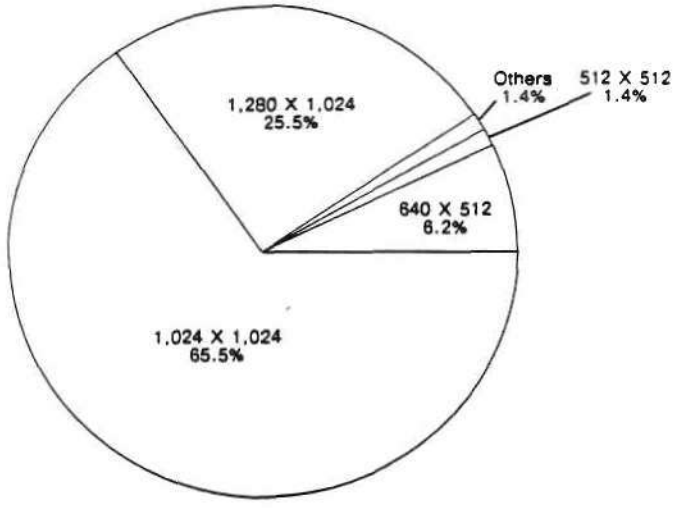
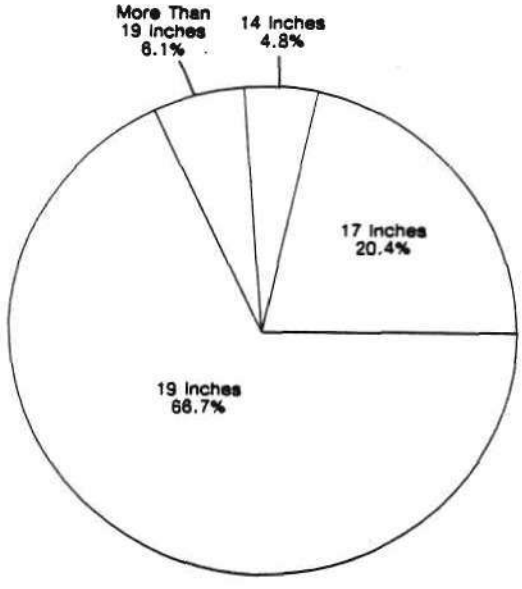


Figure 16

ACCEPTABLE SCREEN SIZE AT ¥2 MILLION



Source: DATAQUEST
February 1986

The most frequent responses given for each of the features yields the following configuration:

Main Memory	2.0 Mbytes
Disk Storage	100 Mbytes
Screen Resolution	1,024 x 1,024
Screen Size	19 inch
Color or Monochrome	Color

SOLIDS MODELING USE

Those surveyed were asked to indicate their solids modeling usage. Only 10.8 percent of the respondents are currently using, and only 42.4 percent are planning to use, solids modeling. This usage is much lower than the 25 percent who are now using, and the 37 percent who plan to use, solids in the United States.

Figure 17 illustrates the overall distribution of respondents for solids modeling use, while Table 8 breaks out the responses for solids modeling use, by industry. Table 8 indicates some significant market opportunities for filling the solids modeling void in the fabricated/structural metal parts, non-electrical machinery, and shipbuilding/plant industries.

Those currently using solids modeling indicated that they were using it on their sites for the following usages:

- CAD
- CAM

As illustrated in Figure 18, more than 70 percent of the respondents indicated that they are using solids modeling for CAD applications only.

Figure 17

SOLIDS MODELING USE IN CAD/CAM

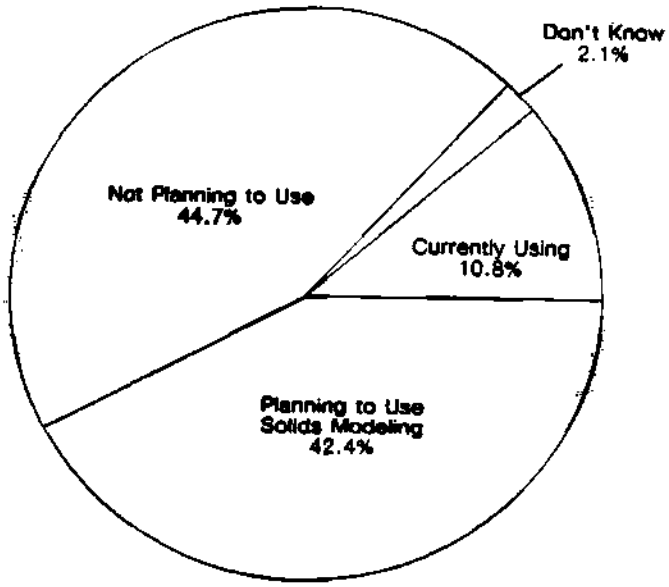


Table 8

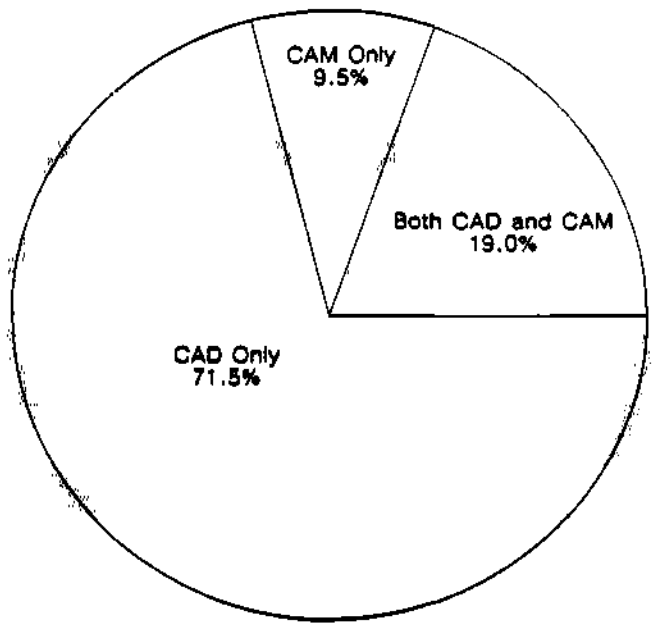
SOLIDS MODELING USE, BY INDUSTRY
(Percent of Respondents)

Industry	Planning to Use	Already Using	Total
Transportation Including Aerospace & Automotive	53%	21%	74%
Architecture/Building	46%	21%	67%
Fabricated/Structural Metal Parts	63%	0%	63%
Non-Electrical Machinery	57%	4%	61%
Shipbuilding/Plant	49%	4%	53%
Electrical/Electronic Machinery	41%	7%	48%
Computers and Peripherals	35%	12%	47%
Semiconductor	17%	21%	38%
Others	35%	9%	44%

Source: DATAQUEST
February 1986

Figure 18

SOLIDS MODELING USAGE



Source: DATAQUEST
February 1986

DATAQUEST CONCLUSIONS

- The 33 percent survey return of the questionnaires is a very high return rate. DATAQUEST believes that end users like to participate in sharing their thoughts and expectations to help vendors develop more cost-effective and efficient products.

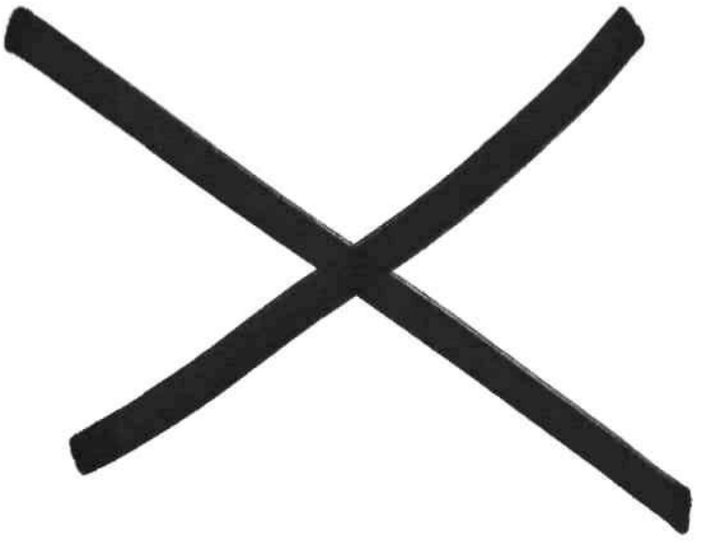
- The application and usage mix of CAD/CAM systems by Japanese and U.S. respondents is nearly identical. Because a good deal of the Japanese systems are U.S.-based products, this is not totally surprising.

- The Japanese semiconductor industry appears to be the most progressive industry group in terms of accepting CAD/CAM technology. This group leads in average number of workstations installed (16), average number of trained users per workstation (4.3), standalone workstation installation percentage (25 percent), percentage of color workstation usage (64 percent), and most favorable feelings toward using personal computers (90 percent).

CAD Tools/AI

- Standalone workstations and personal computers are beginning to play an important role in Japan. Although respondents indicated that standalone and personal computer usage was quite low, DATAQUEST believes that these two architectures will soon dominate new CAD/CAM systems shipments.

- Overall Japanese market penetration (6 percent) is still very low. DATAQUEST expects that the Japanese market will grow at or above that of the United States over the next five years.



Economic Data and Outlook

OVERVIEW

The 1986 world economy is heading into its fourth year of expansion. For most countries, this year will see moderate growth with inflation rates remaining near current levels.

The economic expansion slowed during 1985 and this year will see further deceleration. The slower growth reflects moderate increases in the United States and Japan, while Europe is expected to see gains comparable with last year's. Most other countries, especially in the Pacific Basin, are likely to experience less growth than that of the past couple of years, as smaller increases are seen in the export markets.

Inflation is not the major concern it was a couple of years ago, largely due to weak commodity prices and lower energy costs. In fact, the inflation rates in many countries are currently less than half what they were a few years ago.

These disinflationary forces are a mixed blessing for the world economy. Commodity prices, in inflation-adjusted terms, are at their lowest point in nearly 30 years. And the economies of the Third World countries, which produce and depend upon these exports, continue to suffer as their incomes fall. The industrialized nations reap most of the benefits of these lower prices, and will continue to do so.

With the prospects of increased employment and consumer spending in the United States, imports, which fueled much of the recent economic growth among the other major industrial nations, will continue on their upward trend through this year and probably next. Although moderating, these imports will continue to give additional strength to the global export markets and most economies.

THE UNITED STATES

Buoyed by gains in the service sectors, the U.S. economy is improving and should enjoy a modest growth of 3 percent during 1986. An additional one million jobs are expected to be created this year, putting total employment at a record of more than 108 million. How long the rejuvenated expansion will last depends on consumer spending and efforts to cut the federal deficit.

Consumers remain confident, short-term interest rates are at their lowest level since the late 1970s, and inflation will be held in check by stable food prices and falling energy costs. Inventories are lean and the value of the dollar is dropping. Thus, there are few signs of the forces that typically lead to a recession.

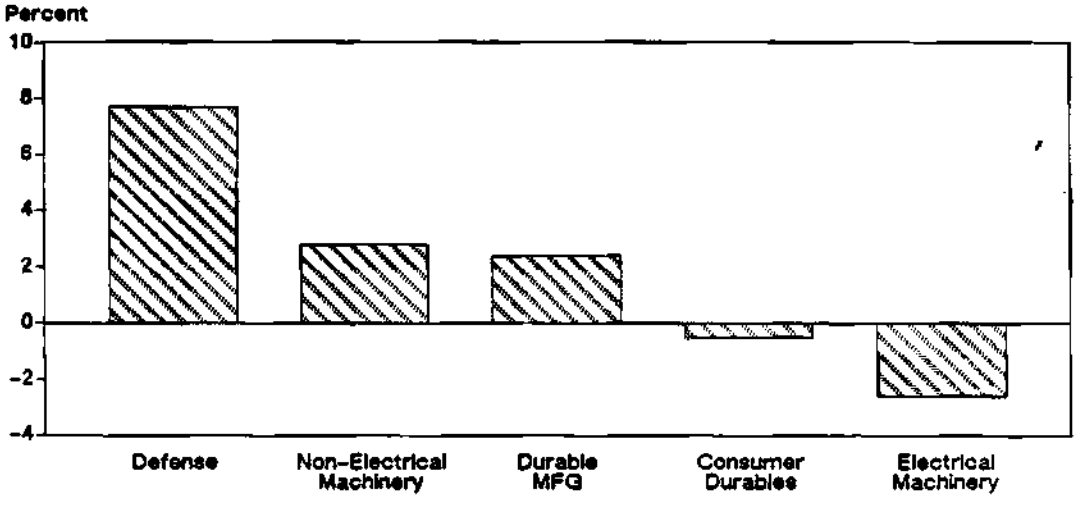
Economic Data and Outlook

There have been significant structural changes in the U.S. economy. The historical strengths, first agriculture and then heavy industry, remain depressed and are no longer the driving forces. The unevenness that marked this recovery continues to hasten the transition from a manufacturing to a service economy.

Figure 1 shows an example of the uneven growth in production in several major U.S. industrial sectors during 1985.

Figure 1

INDUSTRIAL PRODUCTION GROWTH
(1985 versus 1984)



Source: U.S. Department of Commerce

Employment in the durable goods industries has declined by over one million people in the past few years. Overall, the growth of high-technology industries has not generated enough new jobs to offset the losses in the heavy industry sectors. The strong dollar made U.S.-manufactured goods and agricultural products less competitive, and foreign competition has steadily reduced the markets for these products at home and abroad. The resulting huge trade deficit has forced major shifts in the employment structure.

Economic Data and Outlook

Defense spending has become increasingly important to manufacturing. An estimated 15 percent of the employment gains seen in the past three years are directly or indirectly due to defense spending. Pentagon spending will continue to fuel growth for at least the next couple of years.

While consumer spending will increase, low savings and high indebtedness will temper the buyers' enthusiasm. The degree of the improvements during 1986 and 1987 are clouded by other major uncertainties: the budget deficit, the dollar, and capital investment.

Business Fixed Investment

U.S. business will barely boost capital spending for new plant and equipment this year. Companies are cautiously waiting for clearer economic signals and a better understanding of the tax reforms, particularly for investment tax credits and accelerated depreciation. Most of the recent surveys were taken before the improved fourth quarter business conditions were known; however, a one or two quarter uptick will not change the long-range picture.

Manufacturing already has sufficient capacity. Factory utilization is near 80 percent, which means that there is little pressure to expand. In most areas, commercial structures are in oversupply and vacancy rates are increasing. The only bright spot is the continuing need to modernize and increase productivity. This will provide a modest increase in equipment purchases this year.

Imports have grabbed a record share of U.S. markets, and domestic manufacturers have not participated as fully in this expansion as they have in previous recoveries. The declining dollar will make imports less attractive, but no significant impact is seen before late 1986 or early 1987.

Capital spending is a major risk in this year's economic picture. Another 10 to 15 percent drop in the value of the dollar will probably be necessary to alter the trade balance enough to increase capacity requirements this year, and such a decrease seems unlikely.

Fiscal and Monetary Policy

Fiscal Policy

The administration's tax-reform plan is expected to shift a big chunk of the nation's tax burden from individuals to business, largely by eliminating the investment tax credit and trimming the accelerated depreciations that were enacted in 1981.

Economic Data and Outlook

The administration's long-running, laissez-faire economic policy is beginning to stem the tide of protectionist legislation in Congress. The Group of Five's agreement (finance ministers of the five leading industrialized nations) to a U.S. plan to lower the value of the dollar brought an end to the administration's nonintervention policy in the currency markets.

The White House and Congress have made little progress in cutting the budget deficit. As a result, the U.S. will continue to rely on foreign capital inflows to finance the deficit, which will continue upward pressure on long-term interest rates.

Monetary Policy

The Federal Reserve Board has indicated that it does not want short-term interest rates to rise much above their recent levels. The Federal Reserve Board can be expected to continue accommodating the credit needs of a moderate economic expansion, maintain steady interest rates, and try to nudge the dollar lower.

The falling dollar will boost U.S. inflation no matter what the Federal Reserve Board does. Sooner or later, prices of imports will climb, and competing U.S. manufacturers will follow suit by raising prices. However, for most of this year, inflation is not likely to quicken enough to force the Federal Reserve Board into major restraints on the growth of money and credit.

The composition of the Federal Reserve Board is changing, as new members are appointed. There are also indications that Chairman Volcker may feel that it is time to leave the Board. His departure would undoubtedly change the outlook for long-range monetary policy, probably more towards the expansionary side.

Deficits

Trade Deficit

While the falling dollar has made headlines, the trade deficit will not go away soon. Even if the dollar's value continues to drop, changes will be slow. The 1986 trade deficit will stay in the $130 billion range and continue to put pressure on U.S. manufacturers.

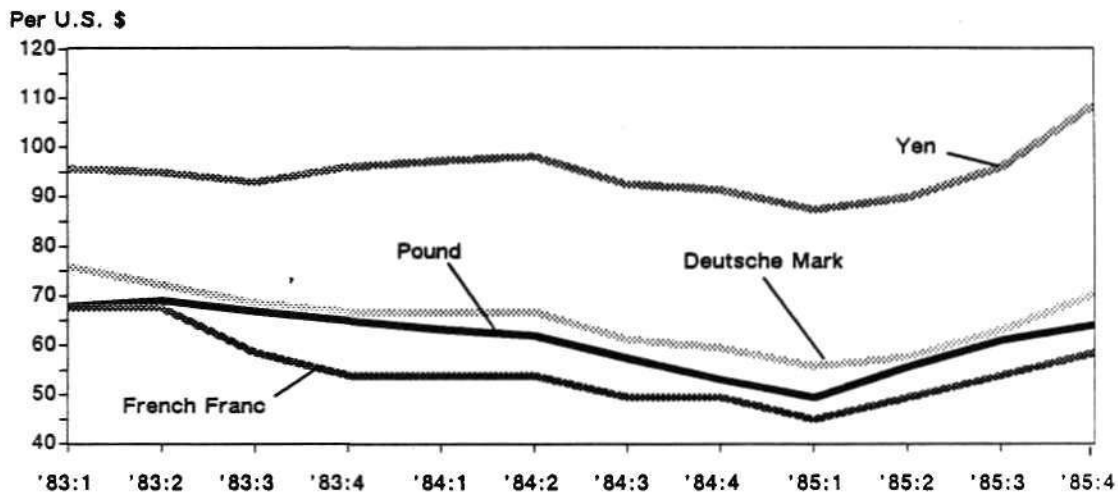
Protectionist pressure has been building on Capitol Hill since the 1974 through 1975 recession. The continuing decline of the U.S. industrial sector and the deepening agricultural crisis will keep strong bipartisan pressure on the White House, as both houses of Congress escalate passage of trade bills.

The bottom line on trade: imports will start to decline and exports show some improvement by midyear; but do not look for major progress on the trade deficit until 1987.

Figure 2 shows the recent trends for the other major currencies. In dollar terms, the Yen increased about 20 percent during 1985 and is currently above its 1980 value. The European currencies floated nearly in parallel, but, compared to the Yen, are still well below the average 1980 value.

Figure 2

MAJOR CURRENCIES



Index: 1980 = $100

Source: International Monetary Fund
Wall Street Journal

Federal Deficit

Although a step in the right direction, the Gramm-Rudman measure, which is supposed to balance the federal budget by 1991, will have a limited effect on 1986 through 1987 government spending.

Many business economists are pessimistic about the likelihood for short-range success of the deficit-cutting amendment. It's an open question how the legislation will work, where the spending restrictions will come from, and how much federal outlay will be cut. A simple fact of the budget is that 40 percent is currently off-limits to reductions.

Economic Data and Outlook

The administration's projected deficit of $172 billion for the current fiscal year looks too low, since it is based upon a 4 percent real GNP growth this year. Even with the recently approved spending cuts, the budget deficit for fiscal 1986 will likely approach $180 billion to $190 billion and could be $20 billion to $30 billion higher if the economy grows by less than 3 percent. In either case, the 1986 shortfall will not be a significant improvement over that of last year.

DATAQUEST's forecast for the 1986 through 1987 U.S. economy is presented in Tables 1 and 2.

Table 1

ESTIMATED QUARTERLY U.S. ECONOMIC INDICATORS
(Billions of Dollars, Seasonally Adjusted at Annual Rates)

	Quarterly							
	85:1	85:2	85:3	85:4*	86:1*	86:2*	86:3*	86:4*
GNP	$3,810.6	$3,853.1	$3,916.1	$3,969.0	$4,028.3	$4,098.7	$4,178.1	$4,264.5
Real GNP ($ 1972)	$1,663.5	$1,670.3	$1,686.9	$1,699.4	$1,710.4	$1,724.1	$1,737.4	$1,751.0
Percent Change	0.3	1.6	4.0	3.0	2.6	3.2	3.1	3.1
GNP Deflator (1972 = 100)	229.1	230.7	232.1	233.6	235.5	237.7	240.5	243.5
Percent Change	5.3	2.8	2.5	2.4	3.4	3.8	4.7	5.1
Real Final Sales	$1,644.4	$1,662.0	$1,689.0	$1,696.4	$1,707.4	$1,721.1	$1,734.4	$1,748.0
Percent Change	-0.3	4.3	6.5	1.8	2.6	3.2	3.1	3.1
Savings Rate (Percent)	4.5	5.1	2.7	3.0	4.0	4.5	5.0	5.0
Real Disposable Income	$1,181.9	$1,205.3	$1,192.1	$1,205.3	$1,214.4	$1,224.1	$1,233.6	$1,243.2
Percent Change	-2.3	8.0	-4.4	4.5	3.0	3.2	3.1	3.1
Real Consumption Spending	$1,089.1	$1,102.1	$1,116.5	$1,124.5	$1,130.9	$1,137.9	$1,146.7	$1,155.7
Percent Change	5.1	4.8	5.3	2.9	1.6	3.2	3.1	3.1
Unemployment Rate (Percent)	7.3	7.3	7.1	7.1	7.0	7.1	7.2	7.2
Wholesale Prices (1967 = 100)	309.1	309.4	307.3	309.0	310.8	312.6	314.3	316.1
Percent Change	-1.0	0.4	-2.7	2.2	2.3	2.3	2.2	2.3
Consumer Prices (1967 = 100)	317.4	321.2	323.6	325.5	328.1	331.6	335.5	339.7
Percent Change	2.5	4.8	3.0	2.4	3.2	4.3	4.7	5.0
Industrial Production (1967 = 100)	123.8	124.2	124.7	125.0	125.8	126.6	128.0	129.0
Percent Change	2.3	1.3	1.6	1.0	2.6	2.6	4.4	3.1
Business Fixed Investment ($ 1972)	$ 213.0	$ 220.3	$ 218.2	$ 218.7	$ 219.1	$ 219.6	$ 220.0	$ 220.7
Percent Change	-1.5	13.9	-3.8	0.9	0.7	0.9	0.7	1.3
Private Housing Starts (Millions)	1.79	1.70	1.66	1.70	1.70	1.65	1.70	1.70
Money Supply (M1)	$ 568.0	$ 583.0	$ 605.0	$ 618.0	$ 627.0	$ 635.0	$ 643.0	$ 650.0
Percent Change	10.3	10.3	15.3	8.9	5.9	5.1	5.1	4.4
3-Month Treasury Bills (Rate: Percent)	8.2	7.5	7.1	7.1	7.0	7.1	7.1	7.2
U.S. Population (Millions)	238.0	238.4	238.8	239.2	239.6	240.0	240.4	240.8
Percent Change	0.8	0.7	0.7	0.7	0.7	0.7	0.7	0.7
Per Capita Real GNP	$6,989.0	$7,006.0	$7,064.0	$7,104.0	$7,138.0	$7,184.0	$7,227.0	$7,271.0
Percent Change	-0.6	1.0	3.3	2.3	1.9	2.6	2.4	2.4

*DATAQUEST estimate

Source: U.S. Department of Labor
U.S. Department of Commerce
Federal Reserve Board
DATAQUEST
March 1986

Economic Data and Outlook

Table 2

ESTIMATED U.S. ECONOMIC INDICATORS, 1980-1987
(Billions of Dollars, Seasonally Adjusted at Annual Rates)

	1980	1981	1982	1983	1984	1985*	1986*	1987*
GNP	$2,632.0	$2,954.0	$3,069.0	$3,305.0	$3,663.0	$3,887.0	$4,142.0	$4,436.0
Real GNP ($ 1972)	$1,475.0	$1,514.0	$1,480.0	$1,535.0	$1,639.0	$1,679.0	$1,730.0	$1,773.0
Percent Change	-0.3	2.6	-2.2	3.7	6.8	2.4	3.0	2.5
GNP Deflator (1972 = 100)	178.6	195.1	207.3	215.4	223.4	231.4	240.3	250.2
Percent Change	9.2	9.3	6.2	3.9	3.7	3.6	3.9	4.1
Real Final Sales	$1,479.0	$1,506.0	$1,490.0	$1,538.0	$1,615.0	$1,673.0	$1,727.0	$1,774.0
Percent Change	0.5	1.8	-1.1	3.2	5.0	3.6	3.3	2.7
Savings Rate (Percent)	6.0	6.6	5.8	5.0	6.1	3.8	4.6	4.8
Real Disposable Income	$1,022.0	$1,055.0	$1,058.0	$1,095.0	$1,169.0	$1,196.0	$1,229.0	$1,260.0
Percent Change	0.6	3.2	0.3	3.5	6.8	2.3	2.7	2.5
Real Consumption Spending	$ 931.0	$ 957.0	$ 963.0	$1,009.0	$1,062.0	$1,108.0	$1,142.0	$1,170.0
Percent Change	0.3	2.8	0.6	4.8	5.3	5.3	3.1	2.4
Unemployment Rate (Percent)	7.1	7.6	9.7	9.6	7.5	7.2	7.1	7.4
Wholesale Prices (1967 = 100)	268.8	293.4	299.3	303.1	310.3	308.7	314.3	323.0
Percent Change	14.1	9.2	2.0	1.3	2.4	-0.5	1.8	2.8
Consumer Prices (1967 = 100)	246.8	272.4	289.1	298.4	311.1	321.9	334.6	349.7
Percent Change	13.5	10.4	6.1	3.2	4.3	3.5	3.9	4.5
Industrial Production (1967 = 100)	108.6	111.0	103.1	109.2	121.8	124.4	127.4	129.9
Percent Change	-1.9	2.2	-7.1	5.9	11.6	2.1	2.4	2.0
Business Fixed Investment ($ 1972)	$ 161.1	$ 174.4	$ 166.1	$ 171.0	$ 204.9	$ 217.6	$ 219.9	$ 223.1
Percent Change	-5.2	8.2	-4.7	3.0	19.8	6.2	1.1	1.5
Private Housing Starts (Millions)	1.30	1.10	1.06	1.70	1.75	1.71	1.69	1.55
Money Supply (M1)	$ 398.0	$ 430.0	$ 459.0	$ 510.0	$ 545.0	$ 593.0	$ 639.0	$ 670.0
Percent Change	7.0	8.0	6.6	11.1	6.9	8.9	7.6	5.0
3-Month Treasury Bills (Rate: Percent)	11.6	14.1	10.7	8.6	9.6	7.5	7.1	7.4
U.S. Population (Millions)	227.7	229.9	232.1	234.5	236.7	238.6	240.2	241.9
Percent Change	1.2	0.9	1.0	1.0	0.9	0.8	0.7	0.7
Per Capita Real GNP	$6,475.0	$6,589.0	$6,378.0	$6,543.0	$6,925.0	$7,040.0	$7,205.0	$7,331.0
Percent Change	-1.5	1.8	-3.2	2.6	5.8	1.7	2.3	1.7

*DATAQUEST estimate

Source: U.S. Department of Labor
U.S. Department of Commerce
Federal Reserve Board
DATAQUEST
March 1986

INTERNATIONAL

Western Europe is progressing on its path of modest expansion and is expected to see at least a 2 percent real growth in 1986. European export markets improved during the last half of 1985 and should see continued increases this year.

Economic Data and Outlook

The declining dollar will have its effect on European exports, but not to the extent seen in many countries; the extensive trade within the Common Market is less sensitive to other currency changes.

Unemployment remains the most persistent problem in Europe. The current expansion has not been sufficient to create jobs as fast as new entries into the labor markets. Unemployment rates are stuck at nearly the same high levels they were three years ago and real relief is not yet in sight. It will be several years before groups entering the labor market are smaller and unemployment rates can be reduced.

Economic expansion elsewhere will also be only moderate. With exports slowing, most countries will have to look to increased domestic demands to spur growth in 1986 and beyond; but, most governments are continuing their austere fiscal policies because of their concern over budget deficits, thus restricting their growth.

As the dollar seeks a lower value and long-term export contracts are renegotiated, exporters to the United States will struggle to hold on to their newly established markets. Many are expected to trim their margins to maintain market share by holding the dollar prices steady and cutting prices in their own currencies.

A different consequence is seen for countries that are competing with Japan in the export markets, particularly in the mid- to low-end consumer goods. The stronger Yen is likely to make their products more competitive and allow them to maintain or even increase their shares of the world markets, at the expense of Japanese products.

Oil is priced in dollars on most international markets; thus energy costs will see further declines and help moderate inflation in most countries. At the same time, this compounds the problems of the export-dependent oil producers. They will fare the poorest in the next few years and can only look ahead to future stronger expansion in the industrialized world.

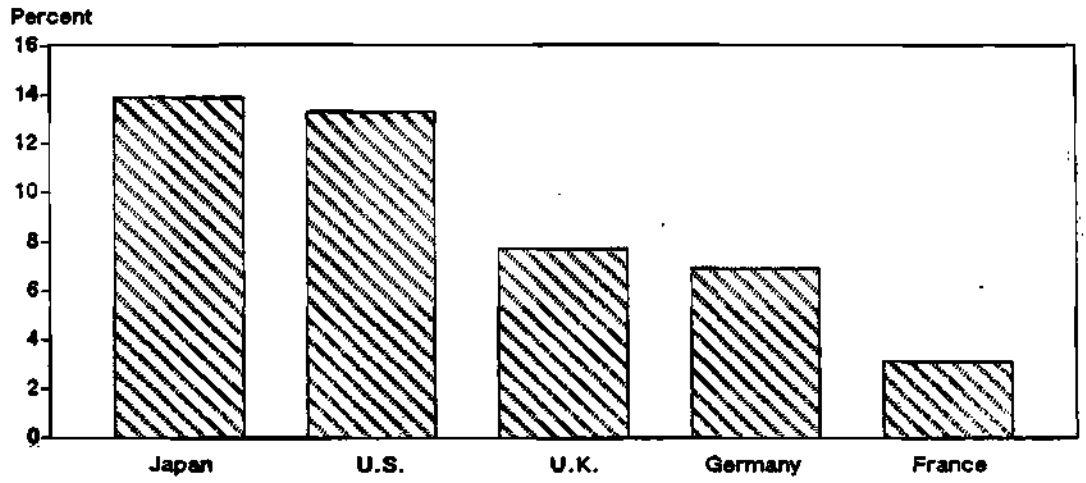
The real economic growth of the five major industrialized countries from 1982 to 1985 is shown in Figure 3.

DATAQUEST's forecasts for France, Japan, the United Kingdom, and West Germany are presented in Tables 3 through 6. Table 7 shows the 1983, 1984, and 1985 month-end selling prices for bank transfers.

Economic Data and Outlook

Figure 3

REAL ECONOMIC GROWTH
(1982 through 1985)



Source: International Monetary Fund
DATAQUEST
March 1986

Table 3

ESTIMATED FRENCH ECONOMIC INDICATORS
(Billions of French Francs, Seasonally Adjusted at Annual Rates)

	Yearly						Quarterly				Yearly	
	1979	1980	1981	1982	1983	1984	85:1*	85:4*	86:1*	86:2*	1985*	1986*
GDP	FF2,442.3	FF2,765.3	FF3,086.4	FF3,569.3	FF3,934.9	FF4,281.2	FF4,600.4	FF4,679.6	FF4,755.9	FF4,839.7	FF4,564.7	FF4,881.2
Real GDP (FF 1975)	FF1,690.4	FF1,708.1	FF1,712.1	FF1,746.8	FF1,759.6	FF1,787.1	FF1,806.9	FF1,811.7	FF1,819.4	FF1,827.7	FF1,804.8	FF1,832.0
Percent Change	3.3	1.0	0.2	2.0	0.7	1.6	1.2	1.1	1.7	1.8	1.0	1.5
GDP Deflator (1975 = 100)	144.5	161.9	180.2	204.3	223.6	239.6	254.6	258.3	261.4	264.8	252.9	266.5
Percent Change	10.4	12.1	11.3	13.4	9.4	7.1	5.6	5.9	4.8	5.2	5.6	5.3
Industrial Production (1975 = 100)	118.0	115.7	113.1	112.5	113.6	114.8	115.7	116.5	116.7	117.0	115.5	117.1
Percent Change	5.2	-2.0	-2.3	-0.5	1.0	1.0	3.5	2.8	0.7	1.0	0.6	1.4
Fixed Capital Formation	FF 524.6	FF 601.1	FF 659.2	FF 742.1	FF 778.7	FF 808.3	FF 839.3	FF 846.0	FF 852.0	FF 858.5	FF 835.5	FF 861.7
Percent Change	14.3	14.6	9.7	12.6	4.9	3.8	3.6	3.2	2.8	3.1	3.4	3.1
Wholesale Prices (1975 = 100)	134.0	145.8	161.8	179.8	200.0	226.0	241.7	244.8	248.0	251.4	240.4	253.1
Percent Change	13.3	8.8	11.0	11.1	11.3	13.0	5.1	5.2	5.3	5.5	6.4	5.3
Consumer Prices (1975 = 100)	144.4	164.3	185.7	207.9	227.6	245.1	262.4	265.8	269.3	273.1	260.3	275.0
Percent Change	10.7	13.8	13.0	12.0	9.5	7.7	5.5	5.2	5.3	5.7	6.2	5.6
Money Supply (M1)	FF 599.0	FF 638.0	FF 741.0	FF 817.0	FF 919.0	FF1,002.0	FF1,053.0	FF1,071.0	FF1,086.0	FF1,102.0	FF1,071.0	FF1,135.0
Percent Change	11.8	6.5	16.1	10.3	12.5	9.0	6.8	6.8	5.7	6.0	6.9	6.0
Official Discount Rate (Rate: Percent)	9.5	9.5	9.5	9.5	9.5	9.5	9.5	9.5	9.5	9.5	9.5	9.5
Exchange Rate (US$/FF)	$0.24	$0.24	$0.18	$0.15	$0.13	$0.12	$0.12	$0.13	$0.13	$0.13	$0.11	$0.13

*DATAQUEST estimate

Source: International Monetary Fund
DATAQUEST
March 1986

Table 4

ESTIMATED JAPANESE ECONOMIC INDICATORS
(Trillions of Yen, Seasonally Adjusted at Annual Rates)

	Yearly						Quarterly				Yearly	
	1979	1980	1981	1982	1983	1984	85:3*	85:4*	86:1*	86:2*	1985*	1986*
GNP	¥218.9	¥235.8	¥252.0	¥264.9	¥275.2	¥292.8	¥312.1	¥315.7	¥319.5	¥323.8	¥311.2	¥326.5
Real GNP (¥ 1975)	¥180.1	¥188.7	¥196.2	¥202.8	¥209.6	¥221.7	¥232.1	¥233.3	¥234.9	¥236.7	¥230.9	¥237.8
Percent Change	5.2	4.8	4.0	3.4	3.4	5.7	2.4	2.1	2.8	3.1	4.2	3.0
GNP Deflator (1975 = 100)	121.6	125.0	128.8	130.6	131.0	132.0	134.5	135.3	136.0	136.8	134.2	137.3
Percent Change	2.6	2.8	3.1	1.3	0.3	0.8	2.1	2.4	2.1	2.4	1.6	2.3
Industrial Production (1975 = 100)	136.0	142.4	143.8	144.4	149.3	165.9	175.0	176.6	177.8	179.2	174.4	180.0
Percent Change	7.3	4.7	0.9	0.4	3.5	11.1	-0.4	3.7	2.7	3.2	5.1	3.2
Fixed Capital Formation	¥ 70.2	¥ 75.4	¥ 78.4	¥ 80.3	¥ 79.3	¥ 84.5	¥ 84.8	¥ 85.1	¥ 85.3	¥ 85.5	¥ 85.1	¥ 86.0
Percent Change	12.6	7.4	4.0	2.4	-1.2	6.5	1.4	1.4	0.9	0.9	0.8	1.1
Wholesale Prices (1975 = 100)	112.0	132.0	133.8	136.2	133.1	132.8	131.2	131.4	131.9	132.5	132.2	132.9
Percent Change	7.3	17.8	1.4	1.8	-2.2	-0.2	-4.4	0.7	1.5	1.8	-0.5	0.5
Consumer Prices (1975 = 100)	127.0	188.2	143.9	147.7	150.4	153.8	157.2	158.0	158.7	159.6	156.9	160.7
Percent Change	3.6	48.2	-23.5	2.6	1.8	2.3	0.7	2.0	1.8	2.3	2.0	2.4
Money Supply (M1)	¥ 66.9	¥ 65.6	¥ 72.1	¥ 76.2	¥ 81.0	¥ 81.2	¥ 85.1	¥ 85.8	¥ 87.1	¥ 88.7	¥ 85.8	¥ 91.7
Percent Change	3.2	-1.9	9.9	5.7	6.3	0.2	1.7	3.3	6.1	7.4	5.7	6.9
Official Discount Rate (Rate: Percent)	6.3	7.3	6.1	5.5	5.4	5.0	5.0	5.0	5.0	5.0	5.0	5.0
Exchange Rate (¥/US$)	¥219.0	¥226.0	¥220.0	¥249.0	¥237.0	¥237.0	¥234.0	¥207.0	¥202.0	¥203.0	¥237.0	¥205.0

*DATAQUEST estimate

Source: International Monetary Fund
DATAQUEST
March 1986

Table 5

ESTIMATED U.K. ECONOMIC INDICATORS
(Billions of £, Seasonally Adjusted at Annual Rates)

	Yearly						Quarterly				Yearly	
	1979	1980	1981	1982	1983	1984	85:3*	85:4*	86:1*	86:2*	1985*	1986*
GNP	£194.5	£227.5	£252.7	£276.9	£300.6	£318.3	£344.1	£348.6	£354.4	£360.7	£342.6	£365.8
Real GNP (£ 1975)	£114.6	£112.0	£110.9	£113.7	£117.3	£119.2	£122.1	£122.7	£123.5	£124.3	£122.4	£124.9
Percent Change	2.1	-2.3	-1.0	2.6	3.1	1.6	1.3	2.0	2.6	2.6	2.7	2.0
GNP Deflator (1975 = 100)	169.6	203.2	225.8	243.4	256.2	267.0	281.8	284.1	287.0	290.2	279.9	293.0
Percent Change	15.1	19.8	11.1	7.8	5.3	4.2	2.9	3.3	4.1	4.5	4.8	4.8
Industrial Production (1975 = 100)	110.7	103.5	100.0	102.0	105.4	106.5	110.5	111.5	112.2	113.0	110.6	113.4
Percent Change	3.8	-6.5	-3.3	1.9	3.4	1.0	-3.7	3.7	2.5	2.9	3.9	2.6
Fixed Capital Formation	£ 34.8	£ 39.2	£ 39.1	£ 45.8	£ 49.1	£ 55.0	£ 56.5	£ 58.0	£ 59.1	£ 60.3	£ 58.3	£ 61.1
Percent Change	16.6	12.7	-0.4	17.2	7.3	12.0	13.4	10.8	7.7	8.2	6.0	4.7
Wholesale Prices (1975 = 100)	195.0	222.4	243.6	262.4	276.8	293.7	311.8	313.8	317.9	322.5	309.9	325.4
Percent Change	10.9	14.0	9.5	7.7	5.5	6.1	2.3	2.6	5.3	5.8	5.5	5.0
Consumer Prices (1975 = 100)	189.8	223.8	250.4	272.0	284.4	298.6	319.4	323.0	326.7	331.0	317.2	333.6
Percent Change	13.5	17.9	11.8	8.6	4.6	5.0	1.1	4.5	4.6	5.3	6.2	5.1
Money Supply (M1)	£ 29.5	£ 30.5	£ 35.7	£ 40.1	£ 44.7	£ 51.7	£ 58.0	£ 59.0	£ 60.2	£ 61.6	£ 59.0	£ 64.9
Percent Change	9.1	3.5	17.0	12.4	11.4	15.7	10.8	7.0	8.2	9.4	14.1	10.0
Treasury Bills (Rate: Percent)	13.0	15.1	13.0	11.5	9.6	9.3	11.9	11.9	11.5	11.0	12.0	10.8
Exchange Rate (US$/£)	$ 2.12	$ 2.24	$ 2.03	$ 1.75	$ 1.52	$ 1.34	$ 1.38	$ 1.45	$ 1.43	$ 1.41	$ 1.30	$ 1.40

*DATAQUEST estimate

Source: International Monetary Fund
DATAQUEST
March 1986

Table 6

ESTIMATED WEST GERMAN ECONOMIC INDICATORS
(Billions of DM, Seasonally Adjusted at Annual Rates)

	Yearly						Quarterly				Yearly	
	1979	1980	1981	1982	1983	1984	85:3*	85:4*	86:1*	86:2*	1985*	1986*
GNP	DM1,395.3	DM1,485.7	DM1,545.1	DM1,599.9	DM1,673.7	DM1,749.9	DM1,852.2	DM1,883.3	DM1,901.7	DM1,921.9	DM1,835.1	DM1,930.8
Real GNP (DM 1975)	DM1,210.1	DM1,233.4	DM1,231.2	DM1,218.4	DM1,234.5	DM1,266.0	DM1,310.8	DM1,322.8	DM1,327.8	DM1,333.8	DM1,302.1	DM1,336.1
Percent Change	4.0	1.9	-0.2	-1.0	1.3	2.6	3.6	3.5	1.8	1.8	2.8	2.6
GNP Deflator (1975 = 100)	115.3	120.5	125.5	131.3	135.6	138.1	141.3	142.4	143.3	144.2	140.9	144.7
Percent Change	4.0	4.5	4.2	4.6	3.3	1.9	2.6	3.0	2.6	2.5	2.0	2.7
Industrial Production (1975 = 100)	118.5	118.5	115.8	111.9	112.8	116.7	121.5	122.6	123.1	124.0	120.8	124.5
Percent Change	5.3	0.0	-2.3	-3.3	0.8	3.4	3.0	3.6	1.6	2.9	3.5	3.1
Fixed Capital Formation	DM 304.8	DM 337.9	DM 338.2	DM 330.7	DM 346.5	DM 357.4	DM 361.0	DM 363.5	DM 365.4	DM 366.8	DM 359.2	DM 367.0
Percent Change	14.3	10.9	0.1	-2.2	4.8	3.1	3.8	2.8	2.1	1.5	0.5	2.2
Wholesale Prices (1975 = 100)	113.0	121.5	131.0	138.6	140.7	144.7	148.1	149.1	150.1	151.5	148.2	152.5
Percent Change	4.8	7.5	7.8	5.9	1.5	2.9	-0.3	2.7	2.7	3.7	2.4	2.9
Consumer Prices (1975 = 100)	115.4	121.8	129.5	136.1	140.7	144.2	147.7	148.1	149.0	149.9	147.5	151.2
Percent Change	4.1	5.5	6.3	5.1	3.4	2.4	0.3	1.1	2.4	2.4	2.3	2.5
Money Supply (M1)	DM 226.0	DM 235.1	DM 231.5	DM 248.1	DM 269.1	DM 285.3	DM 289.0	DM 293.0	DM 296.1	DM 298.7	DM 293.0	DM 303.4
Percent Change	3.0	4.0	-1.5	7.2	8.5	6.0	4.4	5.6	4.3	3.5	2.7	3.5
Official Discount Rate (Rate: Percent)	6.0	7.5	7.5	6.8	4.0	4.4	4.0	4.0	4.0	4.0	4.3	4.0
Exchange Rate (US$/DM)	$ 0.55	$ 0.55	$ 0.44	$ 0.41	$ 0.39	$ 0.35	$ 0.35	$ 0.39	$ 0.40	$ 0.41	$ 0.34	$ 0.42

*DATAQUEST estimate

Source: International Monetary Fund
DATAQUEST
March 1986

Table 7

MONTH-END SELLING PRICES FOR BANK TRANSFERS
(Expressed in U.S. Dollars)

Year	Month	Canada (US$/Can$)	France (US$/FF)	Japan (US$/¥)	United Kingdom US$/£	W. Germany (US$/DM)
1983	January	0.8087	0.1430	0.004171	1.5240	0.4056
	February	0.8141	0.1452	0.004190	1.5125	0.4105
	March	0.8104	0.1375	0.004187	1.4840	0.4119
	April	0.8159	0.1355	0.004204	1.5600	0.4063
	May	0.8131	0.1318	0.004183	1.6050	0.3956
	June	0.8147	0.1308	0.004170	1.5275	0.3931
	July	0.8105	0.1252	0.004118	1.5155	0.3769
	August	0.8196	0.1239	0.004070	1.4990	0.3729
	September	0.8116	0.1251	0.004240	1.4995	0.3802
	October	0.8114	0.1248	0.004276	1.4958	0.3803
	November	0.8074	0.1223	0.004310	1.4685	0.3724
	December	0.8038	0.1200	0.004320	1.4525	0.3676
	Average	0.8201	0.1304	0.004203	1.5120	0.3894
1984	January	0.8005	0.1161	0.004261	1.4018	0.3551
	February	0.7993	0.1244	0.004287	1.4890	0.3836
	March	0.7835	0.1253	0.004466	1.4390	0.3858
	April	0.7786	0.1198	0.004405	1.3980	0.3671
	May	0.7726	0.1193	0.004319	1.3865	0.3662
	June	0.7580	0.1172	0.004213	1.3570	0.3596
	July	0.7606	0.1126	0.004066	1.3085	0.3456
	August	0.7589	0.1062	0.004045	1.2335	0.3254
	September	0.7588	0.1064	0.004053	1.2345	0.3259
	October	0.7608	0.1076	0.004070	1.2201	0.3302
	November	0.7553	0.1054	0.004043	1.1980	0.3223
	December	0.7576	0.1039	0.003978	1.1592	0.3175
	Average	0.7704	0.1137	0.004184	1.3188	0.3487
1985	January	0.7533	0.1034	0.003930	1.1305	0.3156
	February	0.7194	0.0977	0.003840	1.0720	0.2978
	March	0.7305	0.1048	0.003955	1.2295	0.3198
	April	0.7320	0.1063	0.003976	1.2440	0.3227
	May	0.7285	0.1073	0.003982	1.2890	0.3277

(Continued)

Table 7 (Continued)

MONTH-END SELLING PRICES FOR BANK TRANSFERS
(Expressed in U.S. Dollars)

Year	Month	Canada (US$/Can$)	France (US$/FF)	Japan (US$/¥)	United Kingdom US$/£	W. Germany (US$/DM)
	June	0.7359	0.1083	0.004027	1.3095	0.3299
	July	0.7386	0.1171	0.004234	1.4135	0.3580
	August	0.7326	0.1166	0.004188	1.3915	0.3556
	September	0.7279	0.1225	0.004626	1.4075	0.3726
	October	0.7319	0.1255	0.004729	1.4430	0.3826
	November	0.7199	0.1301	0.004907	1.4925	0.3967
	December	0.7153	0.1333	0.004996	1.4520	0.4090
	Average	0.7305	0.1144	0.004283	1.3229	0.3490

Source: The Wall Street Journal
DATAQUEST
May 1986

France

French output is expected to rise 1 to 2 percent in 1986, about the same growth as in 1985. The French recovery has been the lowest of the major industrialized countries and unemployment is staying at 10 to 11 percent, a consequence of the government's fiscal austerity.

Most of its industries are still only marginally profitable and the investment outlook remains fragile. The continued expansion within Europe will give rise to a modest increase in France's net exports, and a small cut in the personal income taxes will help to boost consumer spending this year.

More than elsewhere in Europe, French government policy will continue to focus on inflation. President Mitterrand's 3-year-old program of economic austerity has just begun to produce some positive results and consumer and wholesale price increases are about half what they were three years ago. However, investment and industrial output have not increased proportionately with those of their neighbors.

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The 1986 French budget is the most austere in many years and will prevent any real increase in government spending. The Socialists seem prepared to suffer the consequences of these austerity programs in the hope that it will allow them to claim credit for a return to healthier economic growth by 1987.

Japan

Sluggish exports and less than expected domestic demand slowed the Japanese economy in the last half of 1985. Official forecasts still envision economic growth of 4 percent in 1986, but private estimates are in the 1 to 3 percent range, based upon the increasing prospects that the yen will stabilize in the ¥200 to the U.S. dollar range.

Domestic consumption is expected to increase no more than last year's 2 to 3 percent gain. Japanese plans to stimulate domestic demand will not kick in fast enough to make up for slower export growth.

The Nakasone government has been driving interest rates to the highest level in years to strengthen the Yen against the U.S. dollar (per the Group of Five's agreement); however, this monetary policy will eventually depress domestic demand. A stronger Yen will reduce prices of basic materials and energy, which will keep inflation in the 2 percent range this year.

Private capital spending plans for 1986 are showing signs of slowing, as lower exports will require smaller capacity increases. Overseas sales and profits will be pinched, but Japanese companies will take steps to protect their shares of the export markets. Thus, their large trade surpluses will not disappear, even if the Yen drops further.

The United Kingdom

Britain is in its fifth year of economic expansion, the longest since World War II. GNP should rise 2 percent in real terms in 1986 compared to an estimated 2 to 3 percent last year. Possible tax cuts would boost consumer spending this year, but are not expected to show any dramatic improvements.

U.K. unemployment in excess of 13 percent, the highest of any major industrialized country, remains the country's central concern. It continues to put pressure on the government to increase spending.

The government has been pursuing relatively expansive fiscal and monetary policies; however, interest rates are high. Industry is pleading for lower rates; but, the Thatcher government continues to stress holding down inflation and is not expected to ease credit by much.

Business optimism for 1986 is waning. Businesses expect slower growth due to climbing wage costs and declining competitiveness in the export markets. The British Pound's strength relative to other European currencies is expected to handicap sales abroad.

West Germany

The West German outlook for 1986 is improving. Most firms expect business to increase at about the same rate in 1986 as it did in 1985. Real GNP is expected to increase 2.6 percent in 1986 compared to an estimated 2 to 3 percent gain last year.

The economy saw an upturn in the second half of 1985, with both external and domestic demands gaining ground. Exports and capital investment led the business upturn. Prospects for better earnings and sales coupled with steadier labor costs are expected to keep West German plant and equipment investment headed up through 1986.

Domestic demand is still lagging, but as a result of cuts in the personal income tax rates, consumer spending should increase 2.5 percent in 1986 versus only 1 percent in 1985. For the first time in years, new jobs are being created; however, the unemployment rate stays in the 8 to 9 percent range, with little change expected.

Long-term growth continues to hinge mostly on exports. West Germany will not be hurt as much as Japan by a cheaper dollar, because more of West Germany's trade is with Europe than with the United States, and a higher valued Yen may increase their competitiveness in the export markets for high-end industrial products.

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