Copyrighted material

The Birth and Passing of Minicomputers:
From A Digital Equipment Corp. (DEC) Perspective

1957-1998. 41 yrs., 4 generations:
transistor, IC, VLSI, clusters - winner take all

How computer classes form…and die.

Not dealing with technology =change = disruption

Gordon Bell

11 October 2006

On History…

1. "God alone knows the future, but only an historian can alter the past." -- Ambrose Bierce
2. "A historian who would convey the truth must lie. Often he must enlarge the truth by diameters, otherwise his reader would not be able to see it."--Mark Twain
3. "The past is malleable and flexible, changing as our recollection interprets and re-explains what has happened." -- Peter Berger
4. "History, a distillation of rumour." -- Thomas Carlyle
5. "Anyone who believes you can't change history has never tried to write his memoirs." _-David Ben Gurion
6. "No harm's done to history by making it something someone would want to read." -- David McCullough
7. "History is the present. That's why every generation writes it anew. But what most people think of as history is its end product, myth." -- E.L. Doctorow
8. "People always seemed to know half of history, and to get it confused with the other half." -- Jane Haddam
9. "All history becomes subjective; in other words there is properly no history, only biography." -- Ralph Waldo Emerson

Digital's Trials by Technology…
With time, "high" tech becomes a commodity.

"DEC found guilty of violating Moore's Law …" –gbell

1. Designing and building first transistor circuits. 1957-1965
2. Transition to integrated circuits & modulo 8 bits 1965-1975
3. Design with VLSI; *manufacturing VLSI* *1975-2002*
4. Design of "clusters" as the ultimate computer 1983- ????
5. *Quadruple whammy c1983 – "killer" micros, UNIX: PC, Workstations, CMOS AND UNIX , as "standards" Anyone can manufacturer computers in their dorm! "You mean to say, our new ECL mainframe is not equal to our latest CMOS chip?" –Ken Olsen c1990*
6. *Fail to exploit: networks, WWW, printers, clusters…*

http://research.microsoft.com/users/gbell/Digital/DECMuseum.htm

1. Bell's Law that opens the page and is on my page and Wikipedia. I will open with a bit about laws.
2. Computer, October 1984 that gives the coming and going of the 100 mini companies. 1984 was the time of transition to micros. Startups used UNIX and micros that had performance competitive with minis. Also note my article in Science on "Multis" is important because it became the standard g0t computers.
3. Listing of Minicomputer companies 1960-1984 and super-minicomputer and mini-supercomputer companies 1984-1995.
4. Digital 41 Year History CD published 30 April, 1998 with key events and timeline... with photos and facts about machines (alpha to PDP-1), module, the mill, and people! A nice reference with time, bullets, and photos.
5. COMPUTER ENGINEERING Bell, C. G., C. Mudge, J. McNamara,, Digital Press 1978 has the origin of DEC from the circuits that came from MIT Lincoln Laboratory. It has the story of how the PDP-5 was created as a component. PDP-5 begot the PDP-8 that was the "classic" or archetypical mini. The same story can be told about micros as components.
6. The Bell Appendix for Edgar H. Schein's book "DEC is Dead, Long Live DEC" Berett-Koehler Publishers, San Francisco, 2003. The appendix describes Bell's view of What Happened such that Digital was first sold to Compaq in 1998 and then to HP in 2002. Digital aka DEC was only 41 years old. It has some technology, but it is management too. I am not a fan of Christian's use of DEC as the poster child to illustrate Innovator's Dilemma or disruptive technology…
7. Note the VAX Strategy, similar to the IBM 360 plan, and then Sun's "All the wood behind one arrow".
8. Note the transition to distributed computing and the Ethernet presentation. The complete Ethernet Announcement by Bell (Digital), Noyce (Intel), and Liddle (Xerox) slides and script (PDF 7MB) was made in New York City on February 10, 1982 by the DIX group, followed by announcements in Amsterdam, and London. Note my presentation included: *"the network becomes the system"*... Can you recall a similar mantra that SUN Microsystems later appropriated?
9. See the three articles on the PDP-11 on "the address space problem":

a. Bell, C. G… and W. Wulf, "A New Architecture for Mini-Computers -- The DEC PDP-11, SJCC, pp. 657-675 (1970).
b. What we learned from the PDP-11, published by myself and Bill Strecker in 1975.
c. Retrospective on the PDP-11 Bill Strecker with a retrospective about VAX and Alpha, 1995.

10. Family Tree of Digital's Computers Poster created in 1980, shows the evolution of all of all computer models and times they were introduced since 1960… my favorite way to represent history

Bob Supnik has simulators for the DEC machines Papers on Simulation and Historic Systems. Searching for specific machines and people usually get a lot more than you want or need. E.g. http://www.pdp8.org/, www.pdp11.org www.pdp10.org, www.vax.org are sites about specific minis including simulators.http://en.wikipedia.org/wiki/Digital_Equipment_Corporation lists all the machine families.

The 41 year life and trials of Digital Equipment Corp. aka DEC

- **1960: Birth of DEC from MIT Lincoln Lab… its evolution**
- 1965-1984+?: Birth and death of the minicomputer industry built with LSI to be replaced by multiple, microprocessors
- Theory: Bell's Law (of Computer Classes)
- 1978: VAX and the VAX Strategy to become number 2
- 1985-: PCs, workstations, "killer micros" and standards take on all comers
- The DEC Organization and Culture... What happened?
- Summary…

Digital's aka DEC's Origin and Plan …

1957: Ken Olsen, Harlan Anderson, Stan Olsen -- leave MIT's Lincoln Laboratory as transistor circuit and computer designers; collect $70K from American Research and Development –VC

Business plan: design, manufacture, sell logic modules… and eventually use the earnings and modules for building computers

See also www.computerhistory.org

http://research.microsoft.com/users/gbell/Digital/DECMuseum.htm

Movie celebrating the PDP-1 Birth, Spacewar, etc.
http://www.computerhistory.org/events/index.php?id=1142978073

Some Financial & Size, Dates, Factoids

1957: Founded @ $70K. 5 Mhz logic modules. Profitable 1st yr @$94K. 60p. Ken Olsen, CEO & Ben Gurley, PDP-1 @$14K

1959: Memory test equipment using system modules;

1960: 1st. PDP-1 delivery to BBN;

1964: $1.8M R&D, 1/6 of revenue

1965: $15M. PDP-5 (the Mini), PDP-6 (Timesharing); 1966: $23M;

1971: $147M. PDP-11; 1972: 7.8Kp, $200M; 1977: **$1B** 38Kp;

1978: VAX & VAX Strategy; 1979: $1.8b; 1980: 200KC, $2B;

1982: VAX Clusters.$4B, 369KC, 67Kp, Fortune 137th; 1984: $5B,

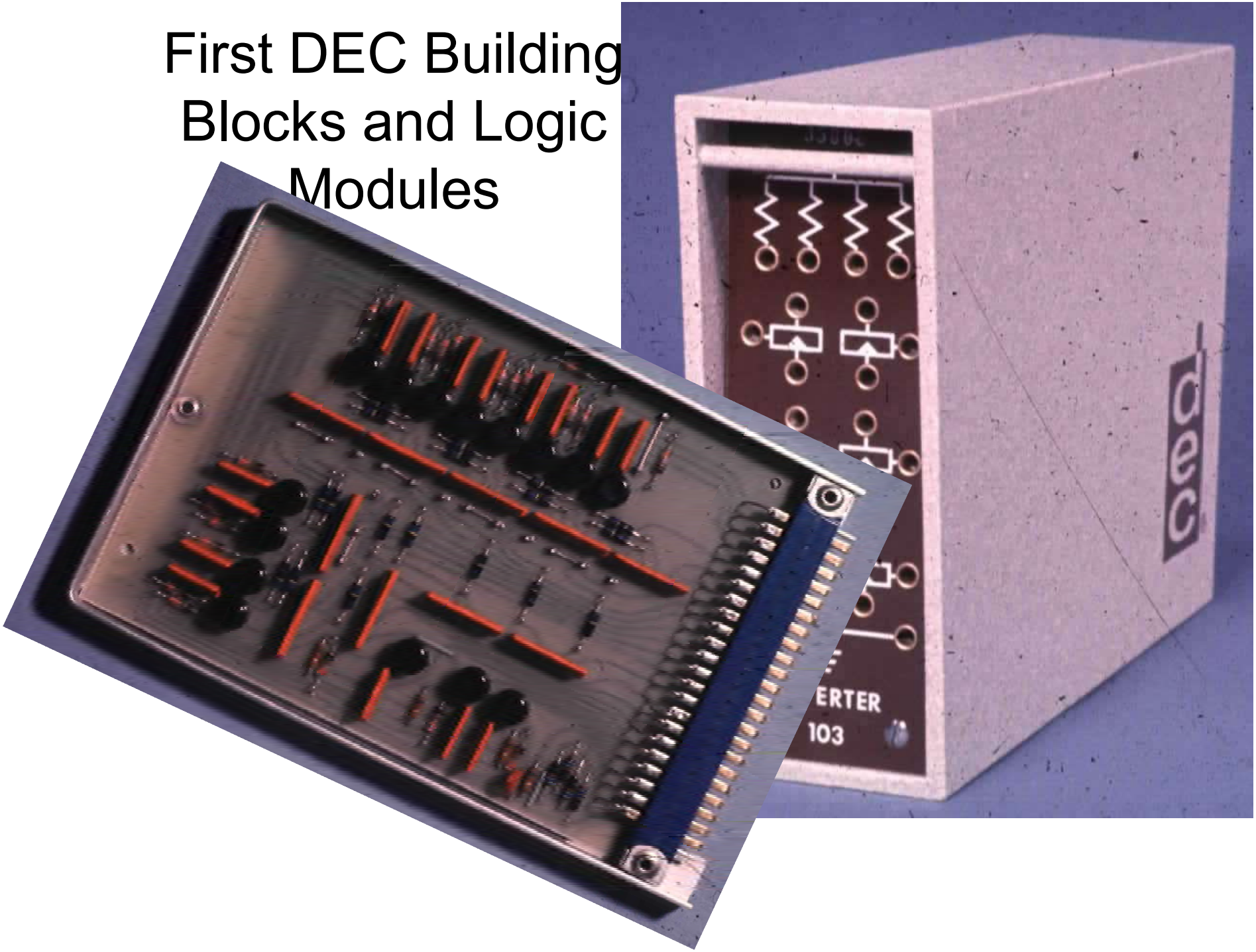
1988 120Kp largest in MA&NH; 62 countries, 475 sales offices $11.4B revenue, $1.3 billion in net profits, market cap $23.9 billion (10th in US), Fortune 38. NUMBER 2!

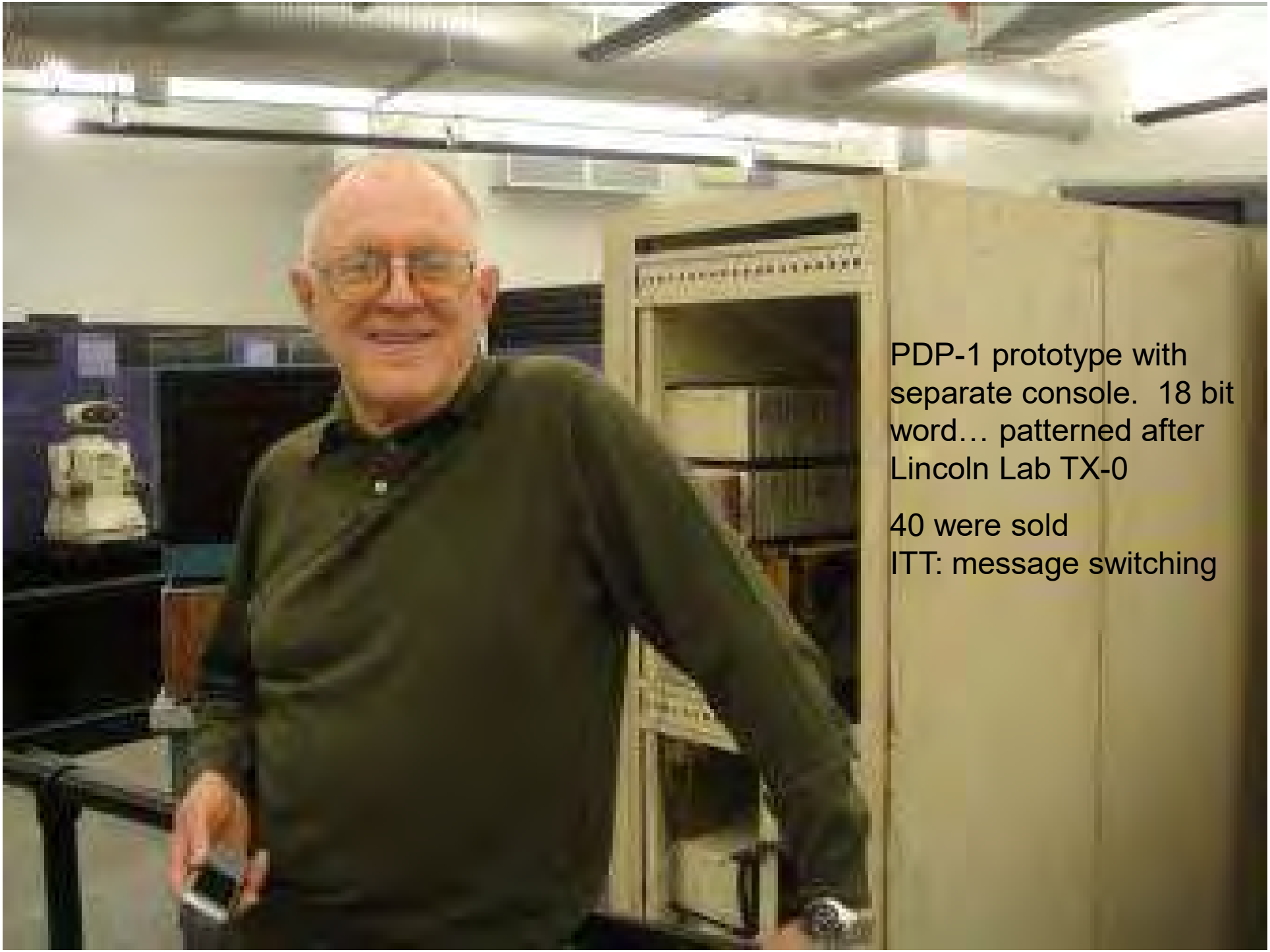
1992: Alpha, Bob Palmer, former VP DEC Semis, appointed CEO

1998: Compaq Acquires DEC @ age 41. All except Palmer lose!

2002: HP acquires Compaq.

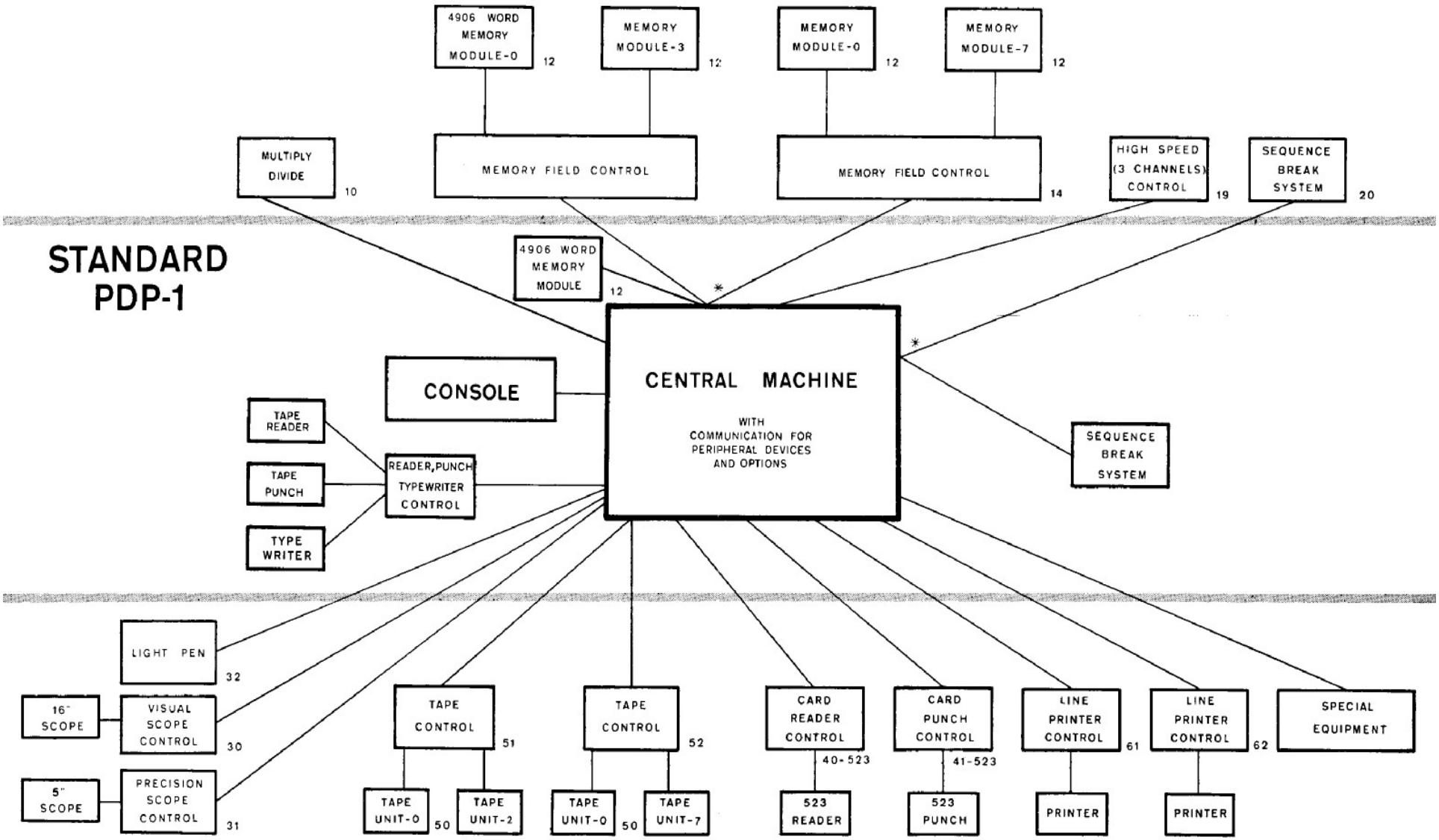
First DEC Building Blocks and Logic Modules





PDP-1 prototype with separate console. 18 bit word… patterned after Lincoln Lab TX-0

40 were sold
ITT: message switching



INPUT-OUTPUT OPTIONS

NOTE:

OUTER NUMBERS DENOTE OPTION TYPES

* ONLY ONE OPTION MAY BE CONNECTED FOR A MACHINE

PDP-5

Initial design was for data collection for an experimental reactor in Canada… A/D, I/O bus, 12-bit word

GROUP 1 OPERATE MICROINSTRUCTIONS

Mnemonic Symbol	Octal Code	Event Time	Operation
nop	7000	—	No operation. Causes a 12 μsec program delay.
iac	7001	3	Index AC. C(AC) +1 => C(AC)
ral	7004	2	Rotate the C(AC) and the C(L) left one place. $C(AC)_i \Rightarrow C(AC)_{i-1}$ $C(L) \Rightarrow C(AC)_{11}$ $C(AC)_0 \Rightarrow C(L)$
rtl	7006	2, 3	Rotate two left.

MEMORY REFERENCE INSTRUCTIONS

Mnemonic Symbol	Operation Code	Time (μsec)	Operation
and Y	0	18	Logical AND. The AND operation is performed between the C(Y) and the C(AC). $C(Y)_i \wedge C(AC)_i \Rightarrow C(AC)_i$.
tad Y	1	18	Twos complement add. The C(Y) are added to the C(AC) in twos complement arithmetic. C(Y) + C(AC) => C(AC).
isz Y	2	18	Index and skip if zero. The C(Y) are incremented by one in twos complement arithmetic. If the resultant C(Y) = 0, the next instruction is skipped. C(Y) + 1 => C(Y). If result = 0, C(PC) + 1 => C(PC).
dca Y	3	18	Deposit and clear AC. The C(AC) are deposited in core memory location Y and the AC is cleared. C(AC) => C(Y), then 0 => C(AC).
jms Y	4	24	Jump to subroutine. The C(PC) are deposited in core memory location Y. The next instruction is taken from location Y+1. C(PC) + 1 => C(Y) Y + 1 => C(PC)
jmp Y	5	12	Jump to Y. The C(PC) are set to address Y. The next instruction is taken from core memory location Y. Y => C(PC).

GROUP 2 OPERATE MICROINSTRUCTIONS

Mnemonic Symbol	Octal Code	Event Time	Operation
hlt	7402	3	Halt. Stops the program.
osr	7404	3	OR with Switch Register C(SR) V C(AC) = > (CAC)
skp	7410	1	Skip, unconditional. C(PC) + 1 = > C(PC)
snl	7420	1	Skip on non-zero L. If C(L) = 1, then C(PC) + 1 = > C(PC)
szl	7430	1	Skip on zero L. If C(L) = 0, then C(PC) + 1 = > C(PC)
sza	7440	1	Skip on zero AC. If C(AC) = 0, then C(PC) + 1 = > C(PC)
sna	7450	1	Skip on non-zero AC. If C(AC) ≠ 0, then C(PC) +1 = > C(PC)
sma	7500	1	Skip on minus AC. If $C(AC)_0 = 1$, then C(PC) + 1 => C(PC)
spa	7510	1	Skip on positive AC. If $C(AC)_0 = 0$, then C(PC) + 1 => C(PC)
cla	7600	2	Clear AC 0 = > C(AC)

A computer that grows with you

Latest machine is designed to serve 128 terminals at once, and to have subsystems added as required. Called the PDP-6, it's made by company that serves mainly scientists

Business Week, March 1964 (recall 4/7/1964)

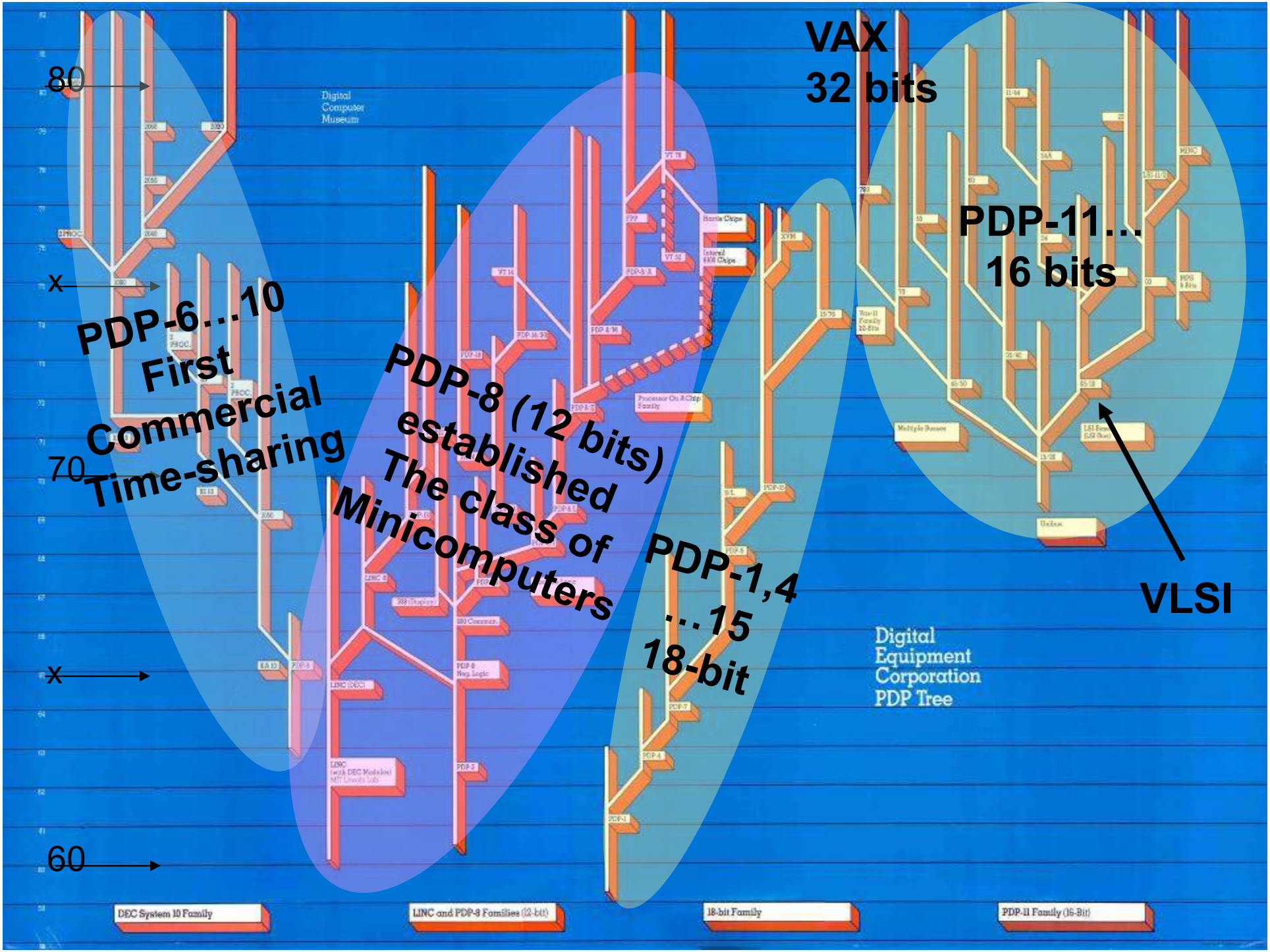
A very small company this week unveiled a computer that, in some respects, is the biggest ever.

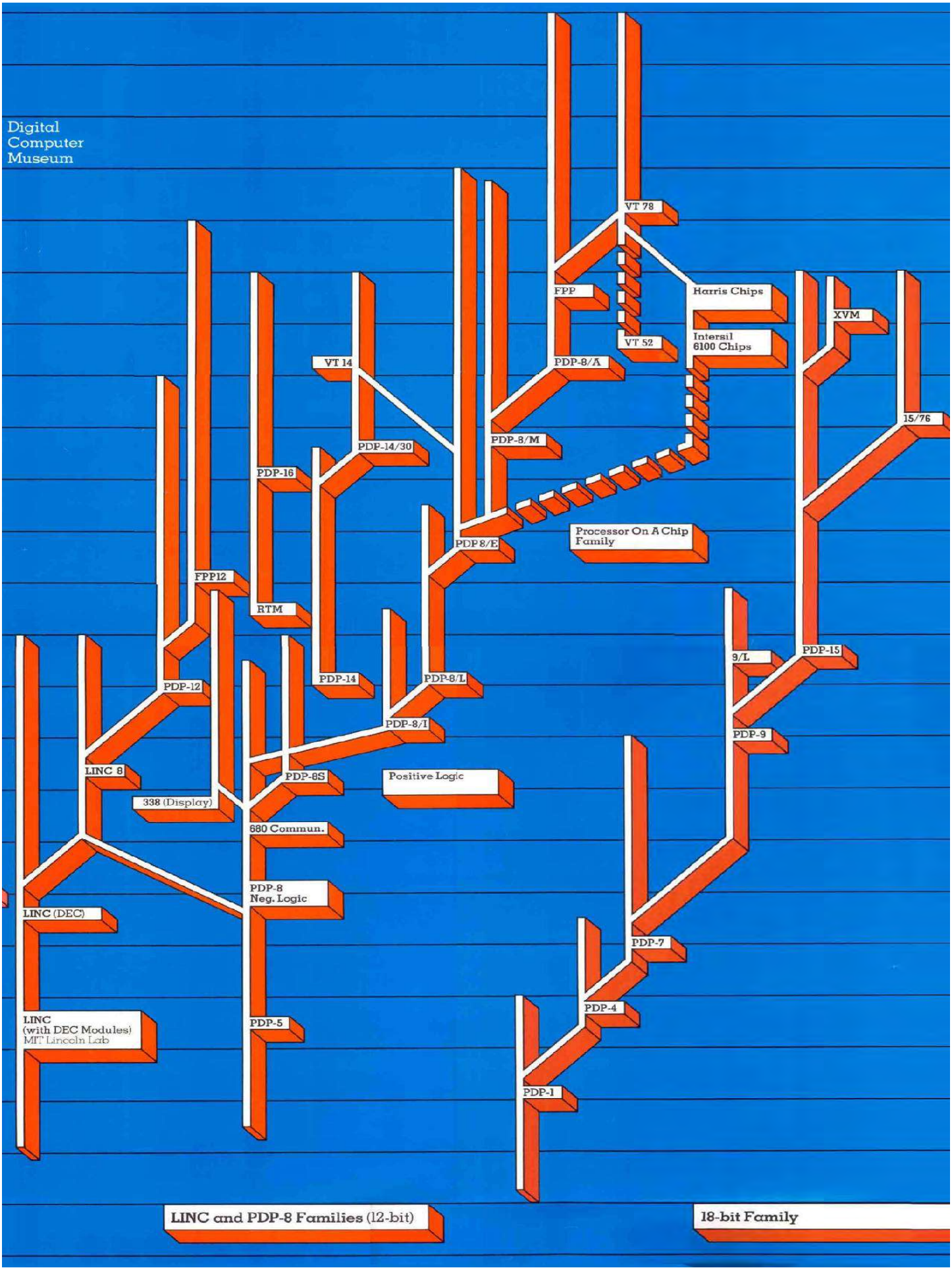
Digital Equipment Corp., of Maynard, Mass., put the machine together. It's called the PDP-6, and it costs $2-million if you want all the available bells and whistles. And these are considerable, particularly its outsized central memory with a capacity of 262,000 words (compared with 64,000 in the larger IBM scientific computers), which, among other things, allows the PDP-6 to serve up to 128 input-output stations simultaneously.

Most computers are designed to work one problem after another, very fast. What's unusual about the PDP-6 is that it is designed to work on a whole lot of problems at once, though at moderate speed. Digital Equipment believes it is the first commercially available computer to offer time-sharing and multi-processing as standard features—a concept that for years has fascinated computer experts at MIT [BW Feb. 1'64,54], as well as DEC's scientist executives.


VAX 11/780

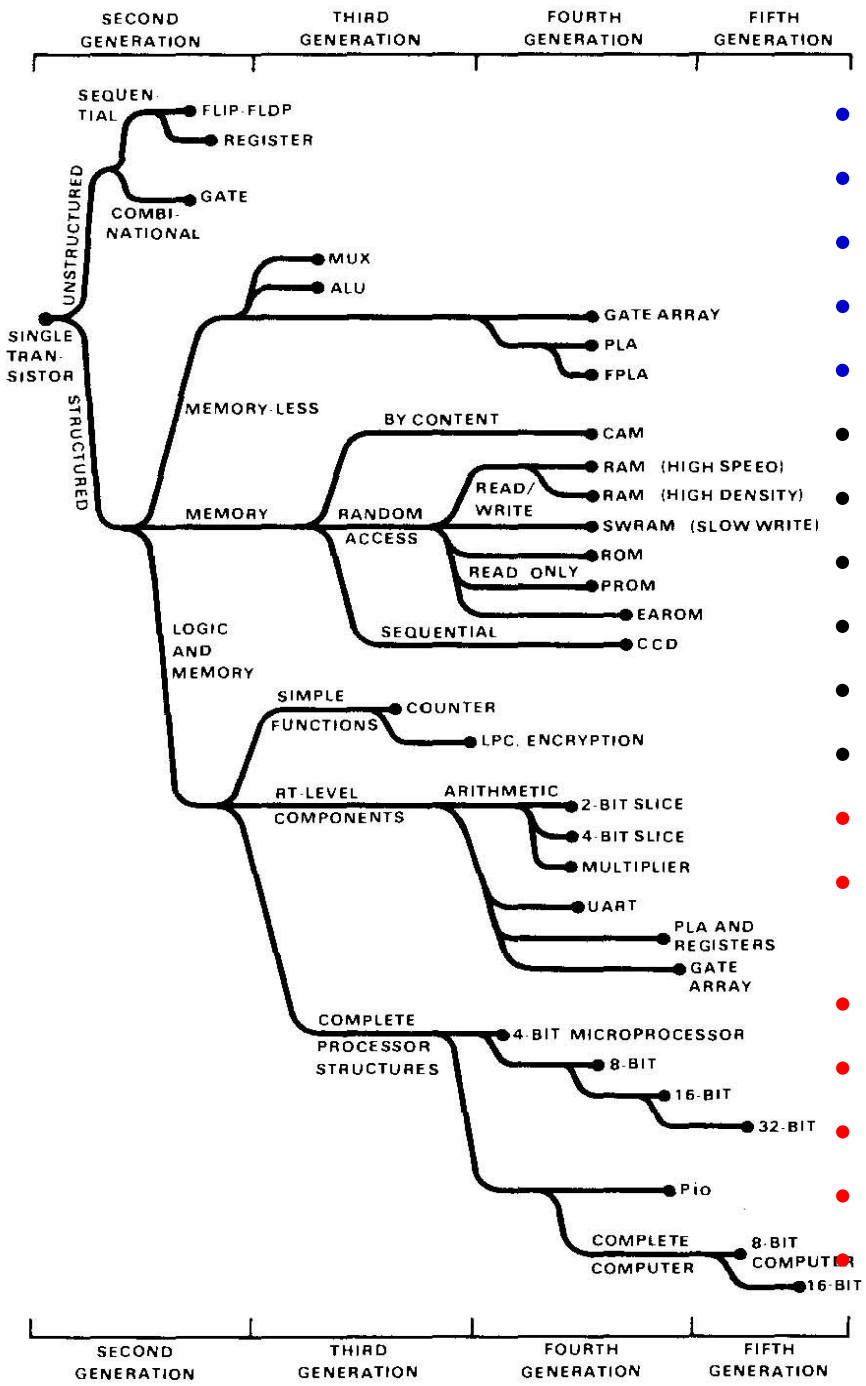

KL10


80
x
70
x
60
PDP-6…10
First
Commercial
Time-sharing
PDP-8 (12 bits)
established
The class of
Minicomputers
PDP-1,4
…15
18-bit
VAX
32 bits
PDP-11…
16 bits
VLSI
Digital
Equipment
Corporation
PDP Tree
Digital
Computer
Museum
DEC System 10 Family
LINC and PDP-8 Families (12-bit)
18-bit Family
PDP-11 Family (16-Bit)


Digital
Computer
Museum
VT 78
FPP
Harris Chips
XVM
VT 52
Intersil
6100 Chips
VT 14
PDP-8/A
15/76
PDP-14/30
PDP-8/M
PDP-16
Processor On A Chip
Family
PDP 8/E
FPP12
RTM
9/L
PDP-15
PDP-12
PDP-14
PDP-8/L
PDP-8/I
PDP-9
LINC 8
PDP-8S
Positive Logic
338 (Display)
680 Commun.
PDP-8
Neg. Logic
LINC (DEC)
PDP-7
PDP-4
LINC
(with DEC Modules)
MIT Lincoln Lab
PDP-5
PDP-1
LINC and PDP-8 Families (12-bit)
18-bit Family

The 41 year life and trials of Digital Equipment Corp. aka DEC

- 1960: Birth of DEC from MIT Lincoln Lab… its evolution
- **1965-1984+?: Birth and death of the minicomputer industry**
  Shift to 8 bit word with introduction of the IBM System 360.
- Theory: Bell's Law (of Computer Classes)
- 1978: VAX and the VAX Strategy to become number 2
- 1985-: PCs, workstations, "killer micros" and standards take on all comers
- The DEC Organization and Culture... What happened?
- Summary…



Tech/Computer Generations

- 1947 Transistor
- 1958 IC
- 1971 4004 Microprocessor
- 1960 1st Trans. Comp.; 64' 8bits
- 1979-83 Ethernet/LANs (DIX)
- 1966 1st IC Computers
- 1965-85+ Mini era (100 companies)
- 1975 1st Micro- computers
- 1981,4 IBM PC, MAC; u's & UNIX
- 1988 – *clusters* = ***the computer***
- 1992 – WWW; 1000s of micros
- 1960 DEC *PDP-1*
- *1965 DEC PDP-5 (mini archetype); DEC PDP-6 (timesharing)*
- 1970, 75 DEC *PDP-11*, LSI-11
- 1978; 84; 92 DEC *VAX; uVAX, Alpha*
- 1982 DEC PCs
- 1983 DEC *VAX Clusters..VAX stratgy*
- 1992 *DEC Altavista*

Minicomputer definitions c1970, 71 with introduction of PDP-11

	primary memory (words)	*(1970 kilodollars)*	*(bits)*
micro	8 K	~ 5	8 ~ 12
mini	32 K	5 ~ 10	12 ~ 16
midi	65 ~ 128 K	10 ~ 20	16 ~ 24

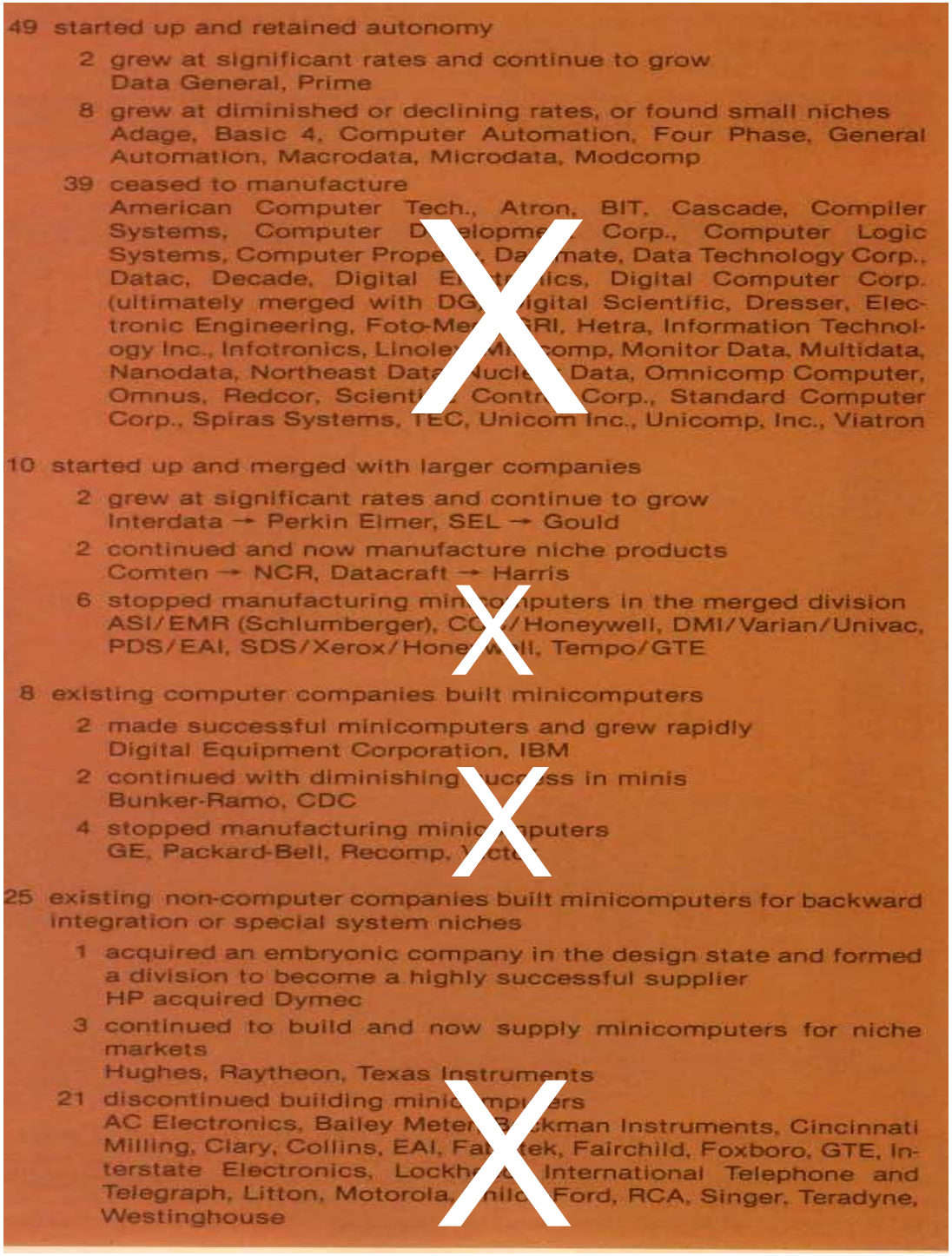
Minicomputers (for minimal computers) are a state of mind; the current logic technology, …, are combined into a package which has the smallest cost. Almost the sole design goal is to make the cost low; …. Alternatively stated: the hardware-software tradeoffs for minicomputer design have, in the past, favored software.

HARDWARE CHARACTERISTICS

Minicomputer may be classified at least two ways:

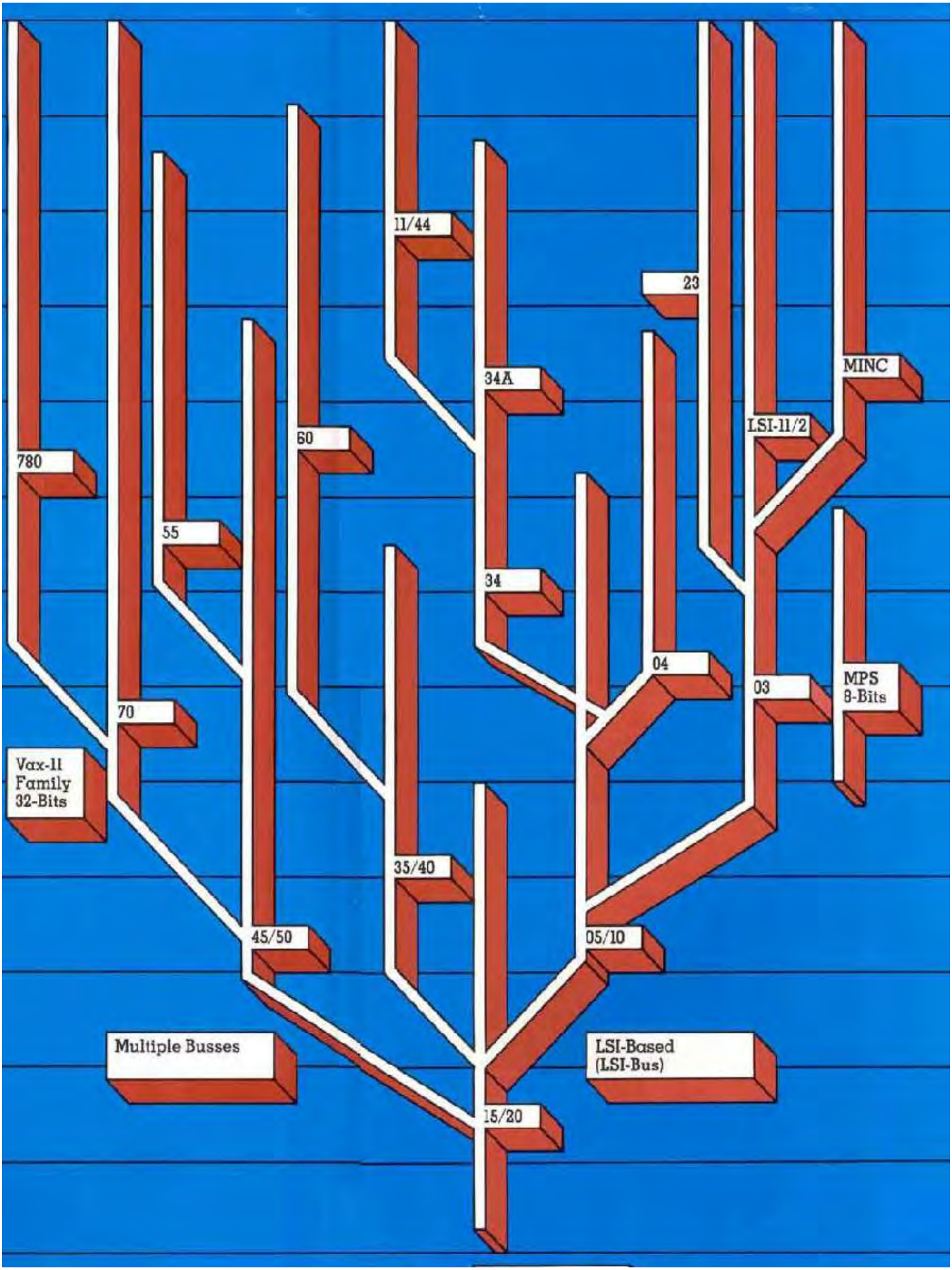
I. It is the minimum computer (or very near it) that can be built with the state of the art technology.

2. It is that computer that can be purchased for a given, relatively minimal, fixed cost (e.g., $10K in 1970).



91 Minicomputer companies 1984

DG, DEC, HP, IBM…
survived by 1990


11/44
23
34A
MINC
LSI-11/2
60
780
55
34
04
MPS
8-Bits
03
70
Vax-11
Family
32-Bits
35/40
45/50
05/10
Multiple Busses
LSI-Based
(LSI-Bus)
15/20

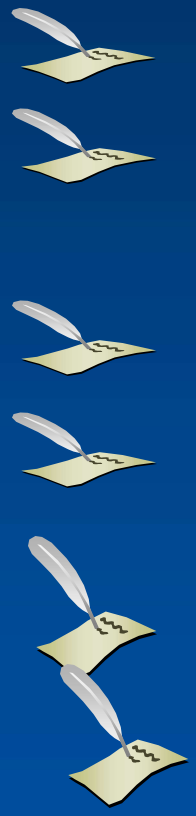
The 41 year life and trials of Digital Equipment Corp. aka DEC

- 1960: Birth of DEC from MIT Lincoln Lab… its evolution
- 1965-1984+?: Birth and death of the minicomputer industry
- **Theory: Bell's Law (of Computer Classes)**
- 1978: VAX and the VAX Strategy to become number 2
- 1985-: PCs, workstations, "killer micros" and standards take on all comers
- The DEC Organization and Culture... What happened?
- Summary…

Bell's Law of Computer Classes & their Formation

the Quest… to move or encode the entire world into cyberspace

Economics-based laws determine the market



- Demand: doubles as price declines by 20%
- Learning curves: 10-15% cost decline with 2X units that enable Moore's Law and other hardware technology evolution
- Bill's Law for the economics of PC *software*
- Nathan's Laws of Software -- the virtuous circle
- Metcalfe's Law of the "value of a network"
- Computer classes form and evolve just like modes of transportation, restaurants, etc.

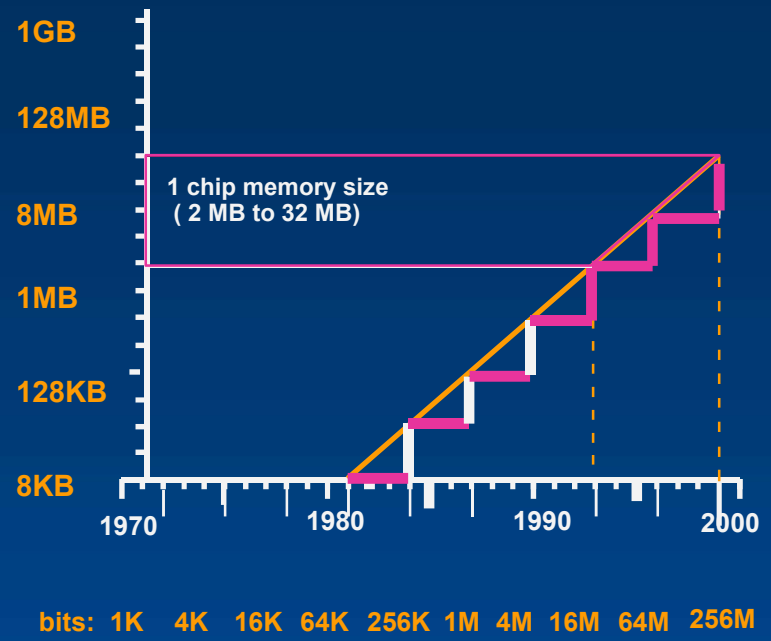
Software Economics: Bill's Law

$$\text{Price} = \frac{\text{Fixed\_cost}}{\text{Units}} + \text{Marginal\_cost}$$

- Bill Joy's law (Sun): NO software for <100,000 platforms
  @$10 million engineering expense, $1,000 price
- Bill Gate's law: NO software for <1,000,000 platforms
  @$10M engineering expense, $100 price
- Examples:
  - UNIX versus Windows NT: $3,500 versus $500
  - Oracle versus SQL-Server: $100,000 versus $6,000
  - No spreadsheet or presentation pack on UNIX/VMS/...
  - Commoditization of base software and hardware

The Virtuous Economic Cycle that drives the PC industry

Moore's First Law



- Transistor density doubles every 18 months
  60% increase per year
  - Chip density transistors/die
  - Micro processor speeds
- Exponential growth:
  - The past does not matter
  - 10x here, 10x there … means REAL change
- PC costs decline faster than any other platform
  - Volume and learning curves
  - PCs are the building bricks of all future systems

Computer components must all evolve at the same rate

- Amdahl's law: one instruction per second requires one byte of memory and one bit per second of I/O
- Storage evolved at 60%; after 1995: 100
- Processor performance evolved at 60%.
  - Clock Performance flat >1995 until multi-cores
  - Multi processors.
  - Graphics Processing Unit to exploit parallelism
- Wide Area Network speed evolved at >60%
- Local Area Network speed evolved 26-60%
- Grove's Law: Plain Old Telephone Service (POTS) thwarts speed, evolving at 14%!

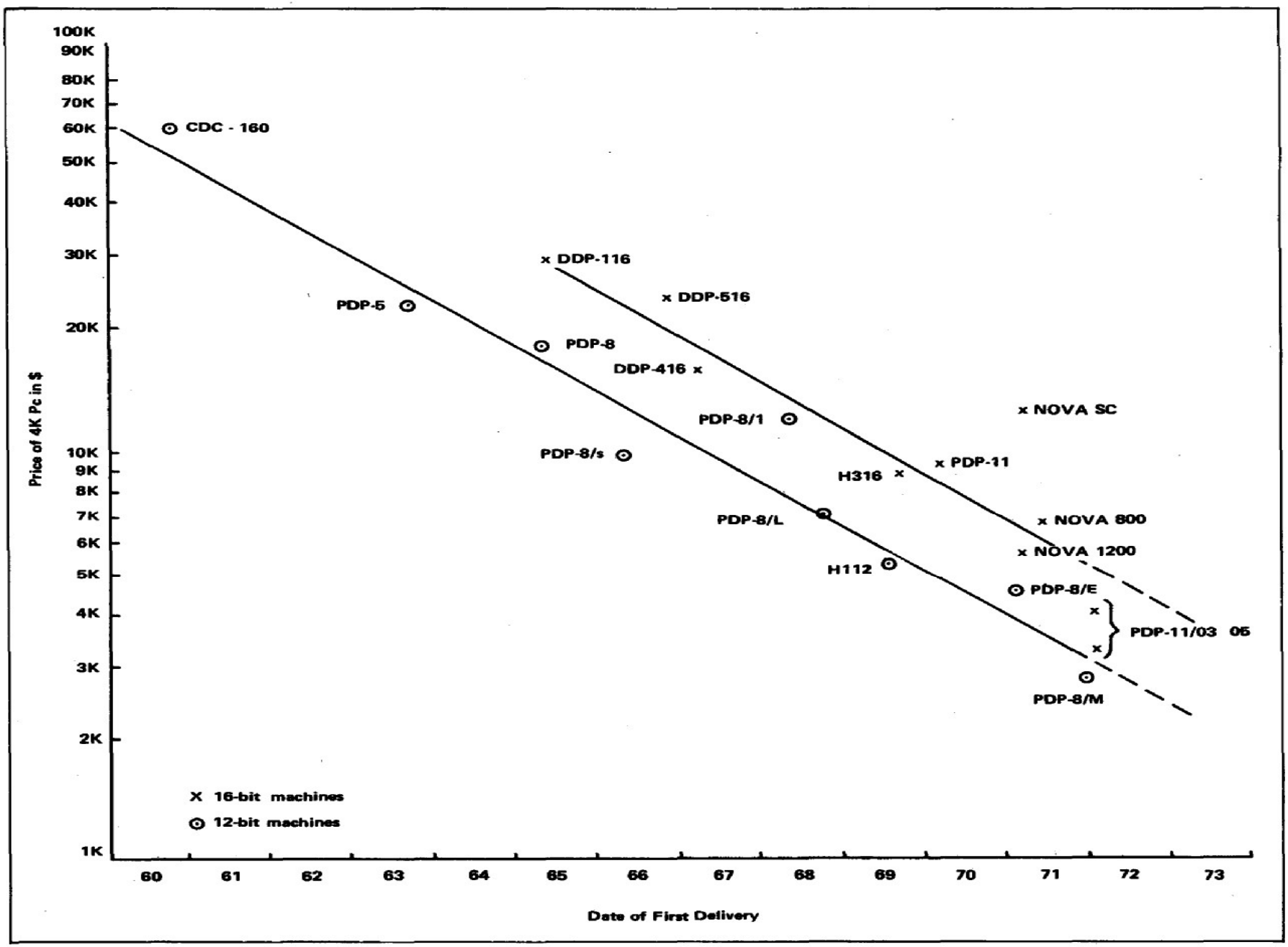
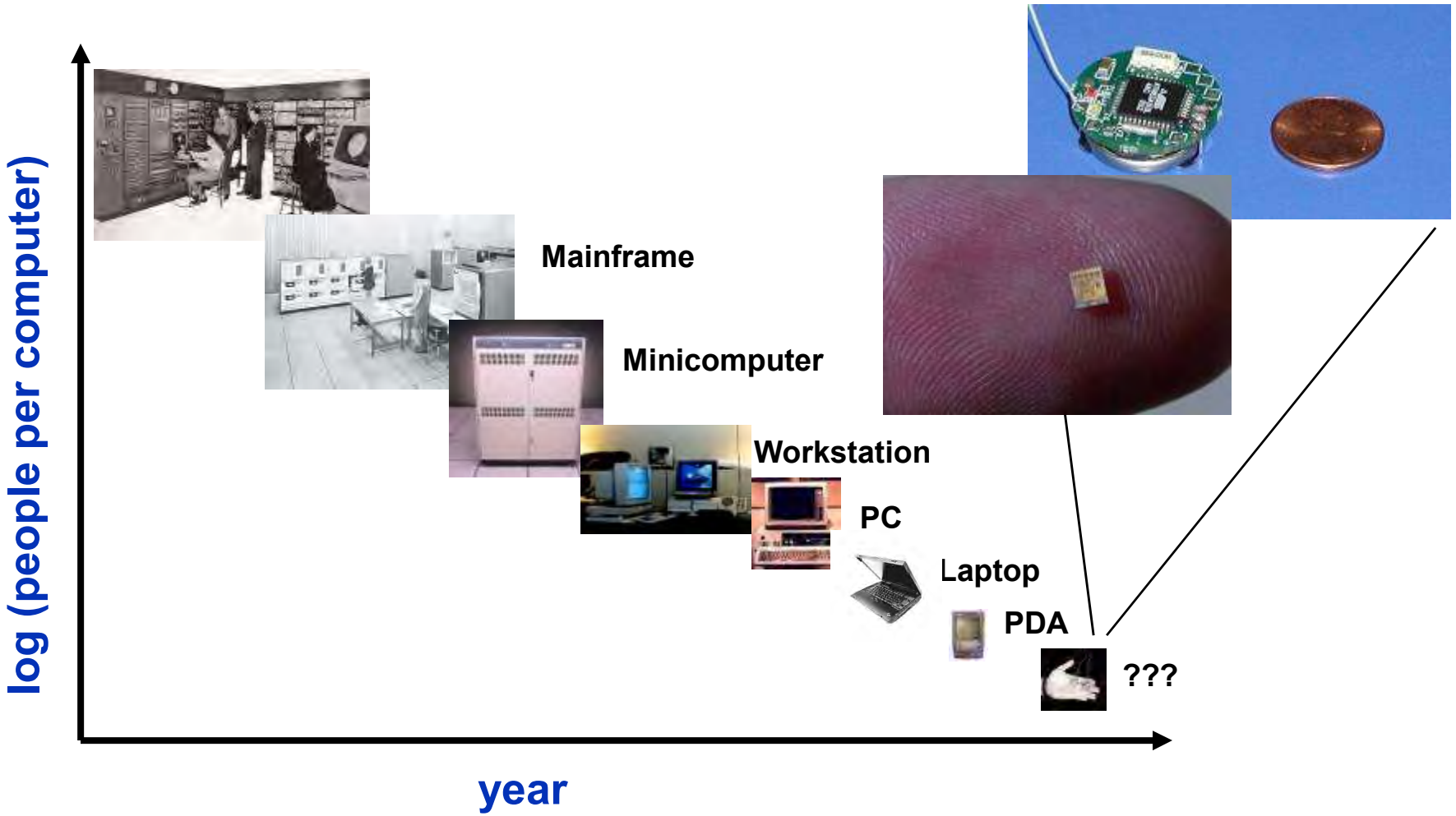
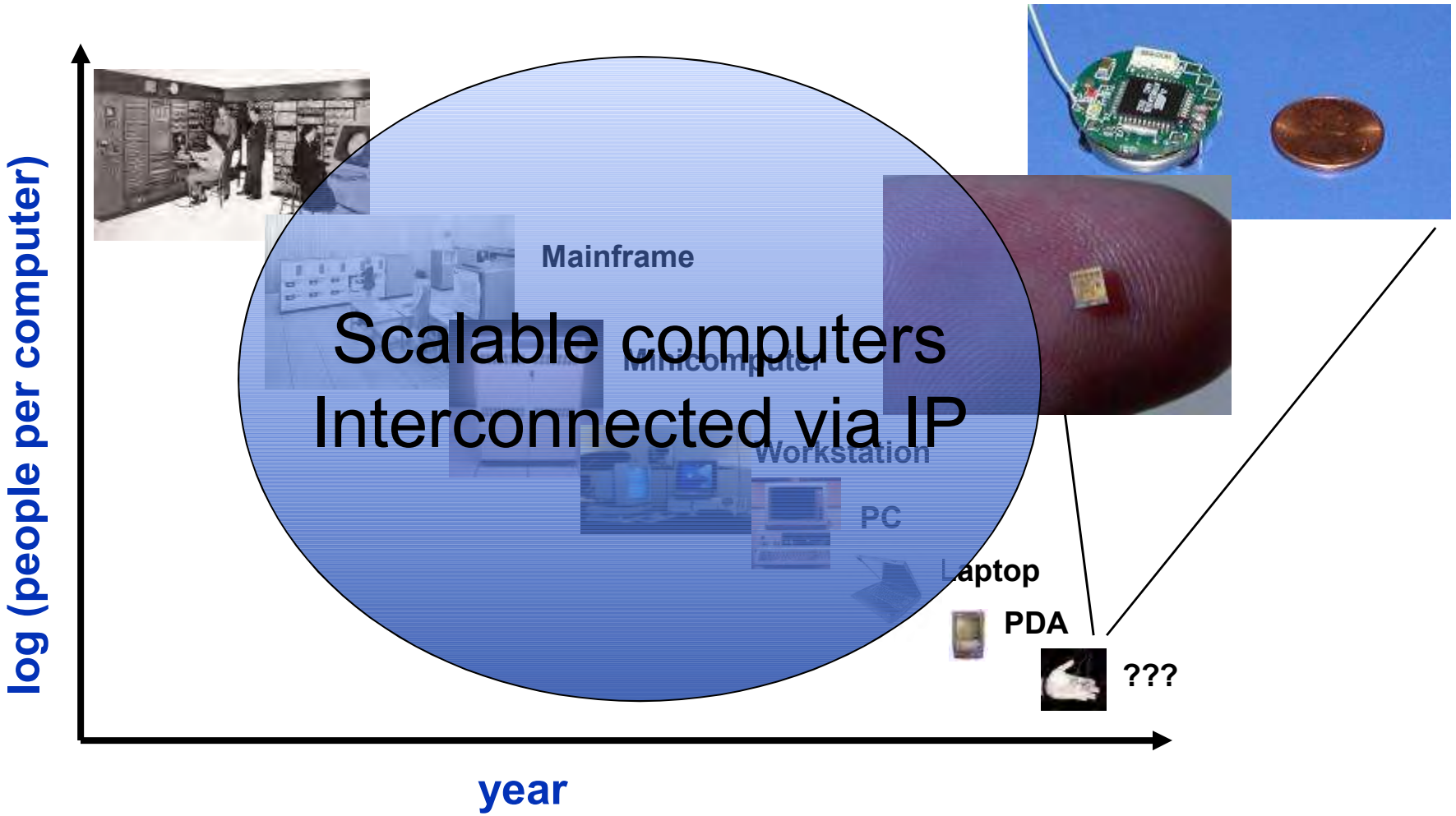


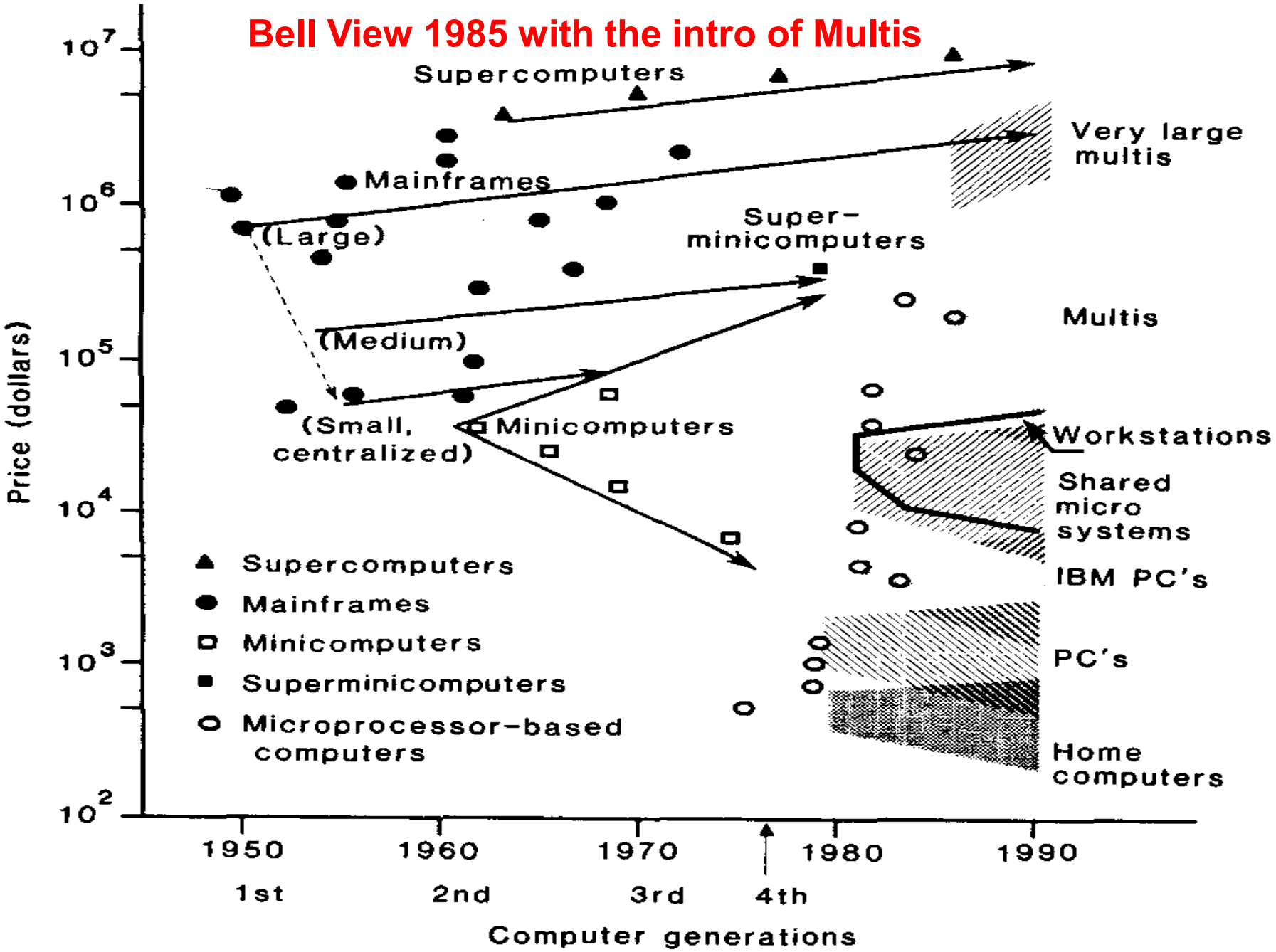
Fig. 1. Plot of cost of 12 and 16 bit machines, based on 4K Pc's, beginning in 1960 and extended through 1970. (Data taken from House and Henzel, 1971, courtesy of Computer Design Magazine.)

The classes, sans phones, 2006



The classes, sans phones, 2006




Bell View 1985 with the intro of Multis
Price (dollars)
10^7
10^6
10^5
10^4
10^3
10^2
Supercomputers
Very large multis
Mainframes
(Large)
Super-minicomputers
Multis
(Medium)
(Small, centralized)
Minicomputers
Workstations
Shared micro systems
IBM PC's
PC's
Home computers
Supercomputers
Mainframes
Minicomputers
Superminicomputers
Microprocessor-based computers
1950
1960
1970
1980
1990
1st
2nd
3rd
4th
Computer generations

How Will Future Computers Be Built?

Thesis: SNAP: Scalable Networks and Platforms

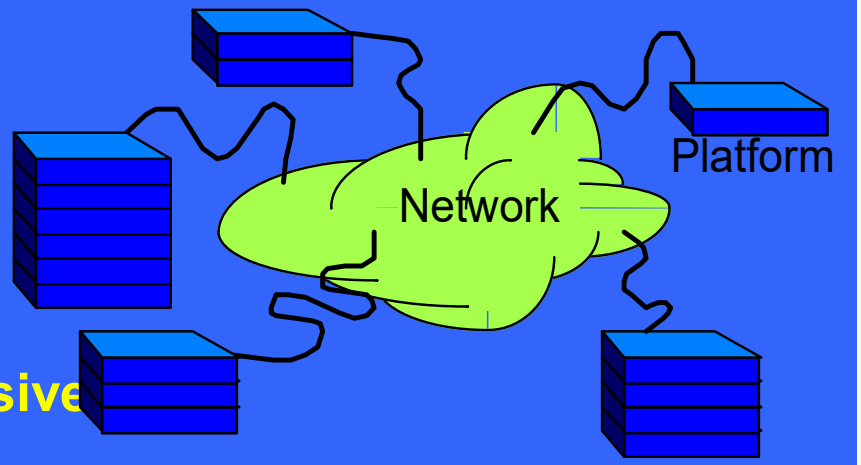
- upsize from desktop to world-scale computer
- based on a few standard components

Because:

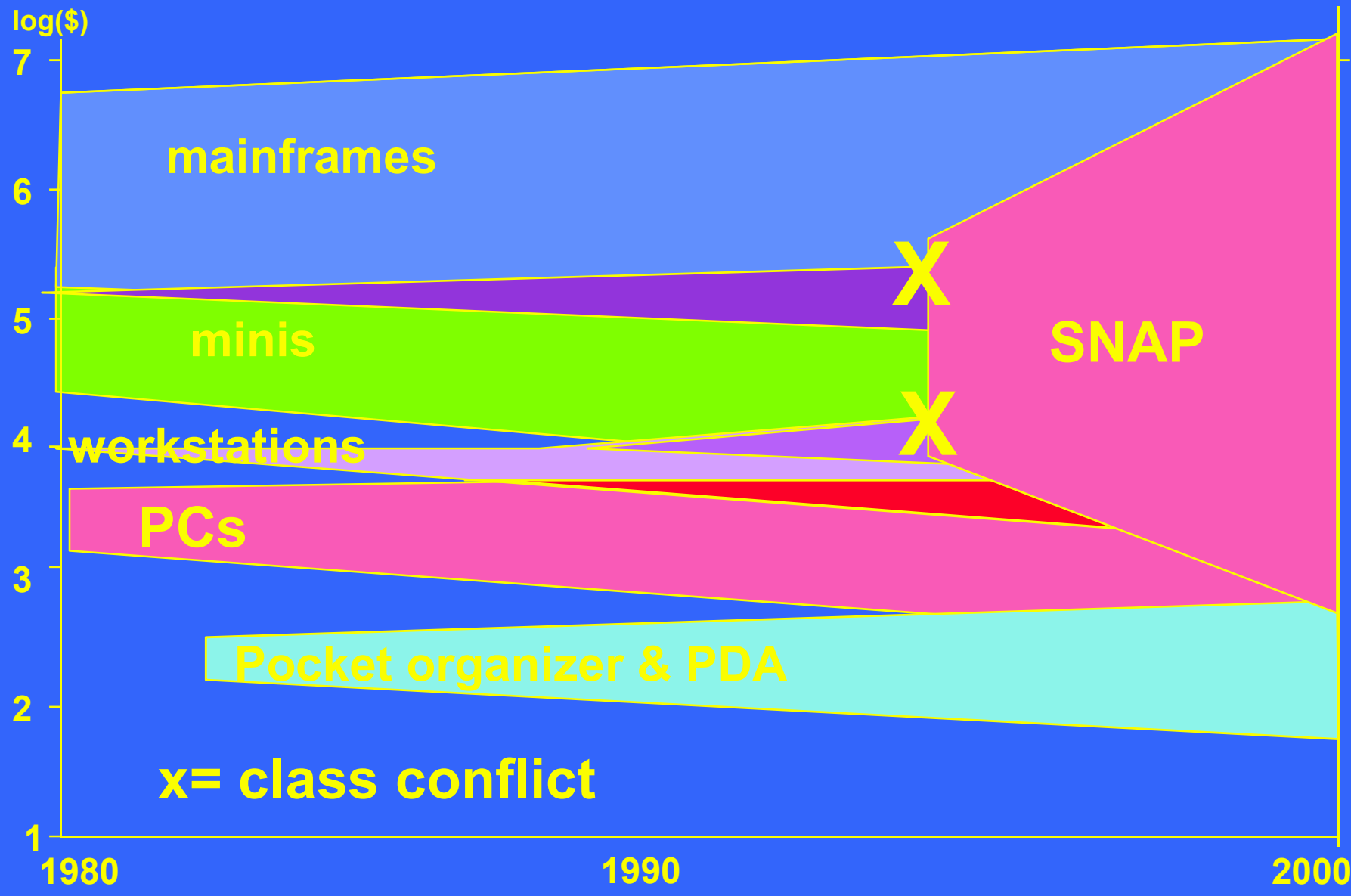
- Moore's law: exponential progress
- Standardization & commoditization
- Stratification and competition

When: Sooner than you think!

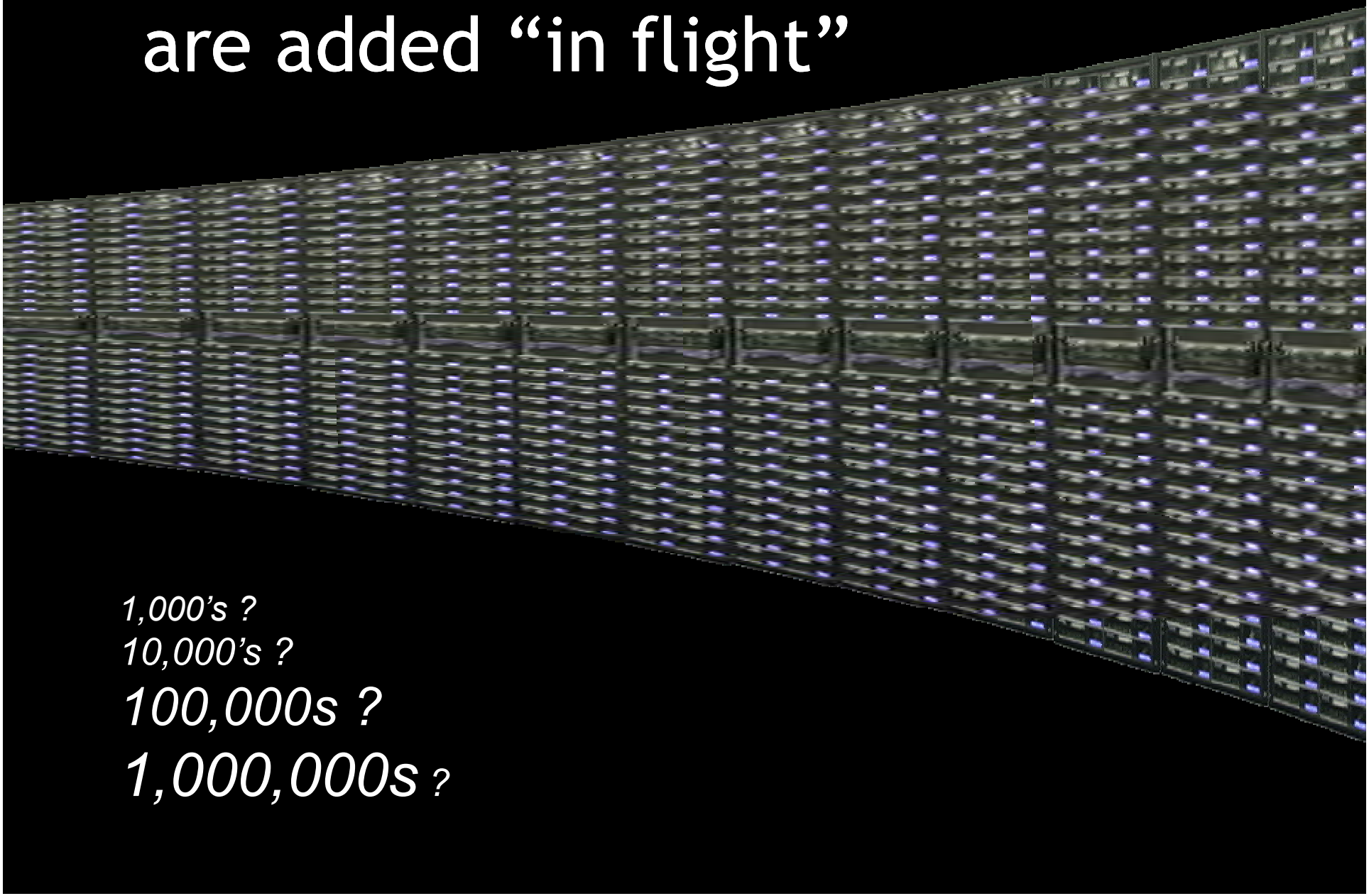
- massive standardization gives massive
- economic forces are enormous



Class conflict with SNAP



Large servers… new services are added “in flight”



1,000’s ?
10,000’s ?
100,000s ?
1,000,000s ?

Bell's Law of Computer Classes

Hardware technology improvements i.e. Moore's Law for semis,… disks, enable two evolutionary paths(t) for computers:

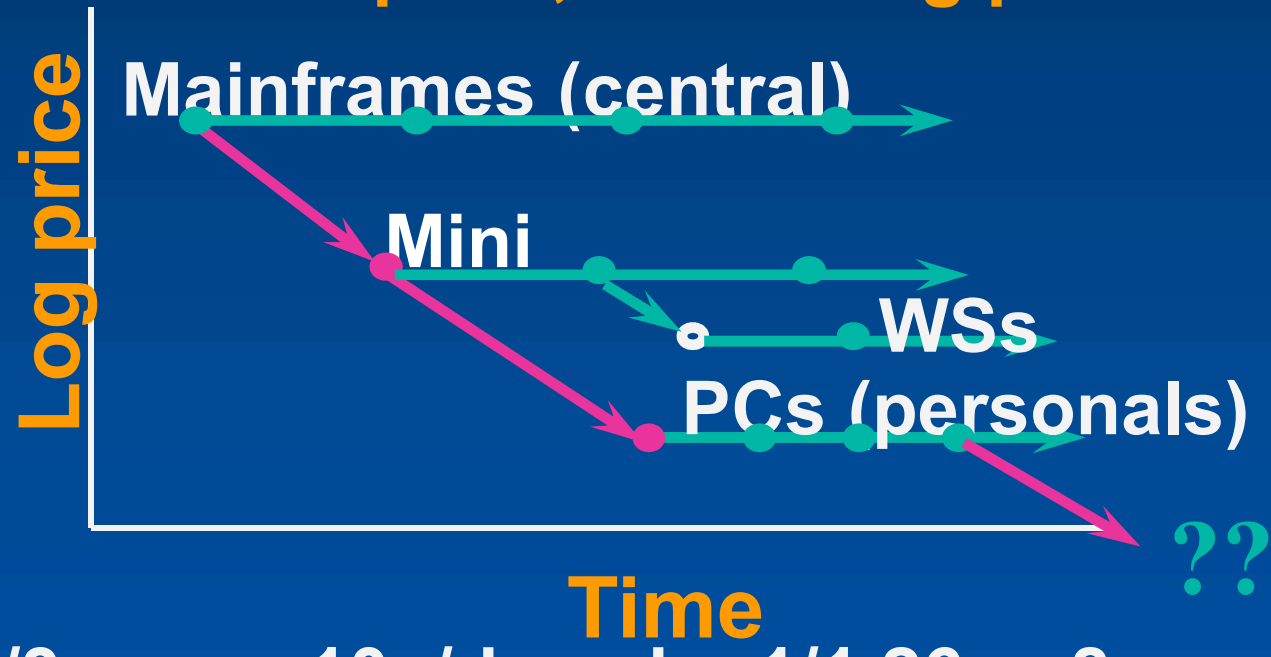
1. constant price, increasing performance

2. Constant or decreasing performance, decreasing cost by a factor O(10)X
.. leading to new structures or a new computer class!

Bell's Law of Computer Classes

Technology enables two evolutionary paths:

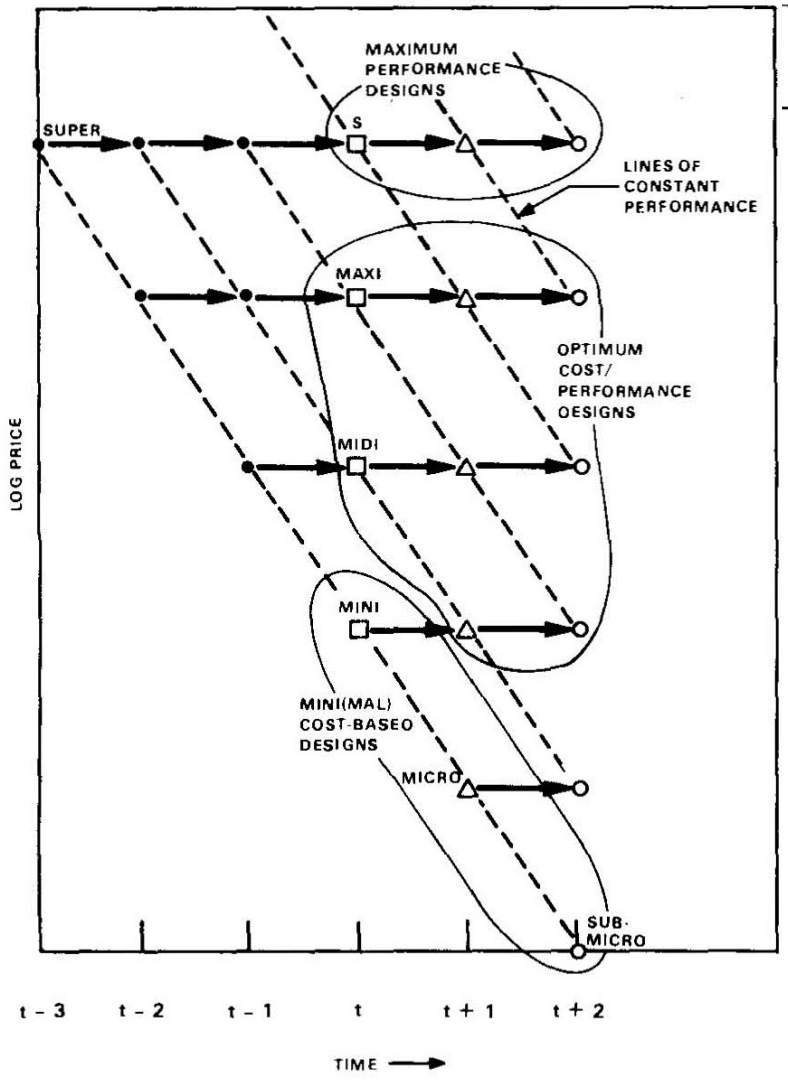
1. constant performance, decreasing cost
2. constant price, increasing performance



1.26 = 2x/3 yrs -- 10x/decade; 1/1.26 = .8

1.6 = 4x/3 yrs --100x/decade; 1/1.6 = .62

Conspiracies: Why old companies can't create new computer classes



Introduction (*generation*)	Time t	t + 1	t + 1	t + 1
Design style	Base case	Constant price/ increased performance	Constant performance/ decreased price	Constant performance/ decreased price
Application	Base	Base	Base	New base
Computer price	1	1	0.5	0.5
Operating costs (range)	2–4	2–4	2–4	1–2
Total cost	3–5	3–5	2.5–4.5	1.5–2.5
Performance (and improvement)	1	2	1	1
Improvement (in total cost)	1	1	0.83–0.9	0.5
Performance/price (computer only and improvement)	1	2	2	2
Performance/ total cost	0.33–0.2	0.66–0.4	0.4–0.22	0.66–0.4
Improvement (in performance/total cost)	1	2	1.21–1.1	2

Price, performance, and class of various goods & services

Computer price = $10 x 10 $^{class\#}$

Computer weight = .05 x 10 $^{class\#}$

Car price = $6K x 1.5 $^{class\ \#}$

Transportation artifact prices =
k x $10 ^{type} (shoes,...cars,... trains,... ICBMs)

French Restaurants(t='95) =
f(ambiance, location) x $25 x 1.5 ^{stars}

Platform, Interface, & Network Computer Class Enablers

Platform	"The Computer" Mainframe	Mini & Timesharing	PC/WS	Web browser,
Interface	tube, core, drum, tape, batch O/S	SSI-MSI, disk, timeshare O/S	micro, floppy, disk, bit-map display, mouse, dist'd O/S	PC, scalable servers,
	direct > batch	terminals via commands	WIMP	Web, HTML
Network		POTS	LAN	Internet

Bell's Law of Computer Classes… Every Decade a new class emerges

- Every decade a new, lower (1/10) cost class of computers emerge to cover cyberspace with a
  - New computing platform
  - New Interface to humans or a part of physical world
  - New networking and/or interconnect structure
  - New classes --> new apps --> new industries
- The classes… a decade in price every decade

60s	$millions	mainframes
80s	$10K	workstations & PCs; MICROs
70s	$10K-100K	minis
90s	$1K	PCs
00s	$100s	PDAs & cellphones
10s	$10	SFF& CPSDs, sensors, motes

Bell's Nine Computer Price Tiers

1$:	embeddables e.g. greeting card
10$:	wrist watch & wallet computers
100$:	pocket/ palm computers
1,000$:	portable computers
10,000$:	personal computers (desktop)
100,000$:	departmental computers (closet)
1,000,000$:	site computers (glass house)
10,000,000$:	regional computers (glass castle)
100,000,000$:	national centers

Super server: costs more than $100,000
"Mainframe": costs more than $1 million
an array of processors, disks, tapes, comm ports

Copyrighted material

Pyramid of networked - computing, communicating, and storage devices

Computer Industry 1982

Computing Laws

Law of Dis-integration: forming A Horizontal Computer Industry

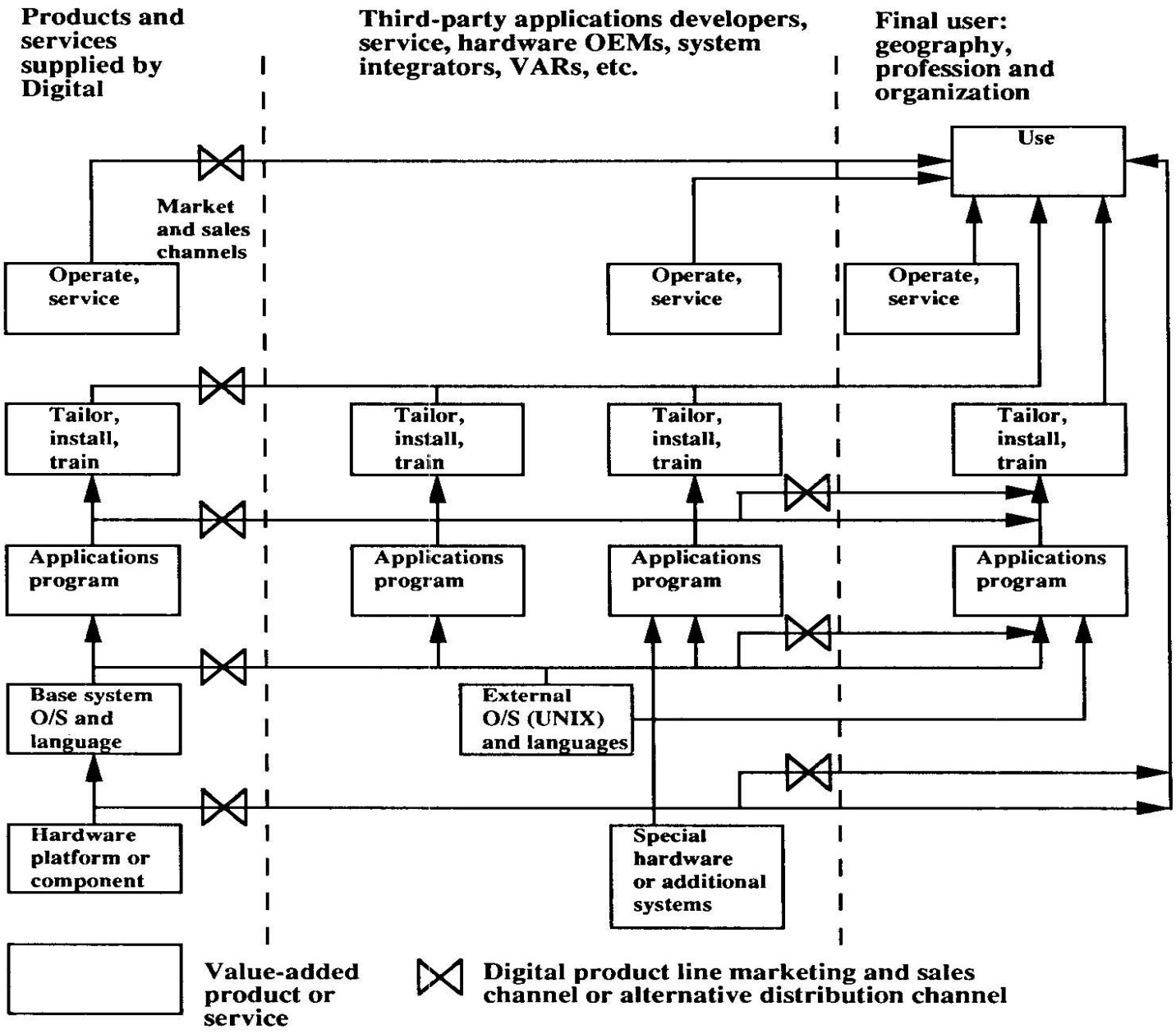
- Horizontal integration is new structure
- Each layer picks best from lower layer
- All layers run //
- Desktop (C/S) market
  - 1991: 50%
  - 1995: 75%

Function	Example
Operation	AT&T
Integration	EDS
Applications	SAP
Middleware	Oracle
Baseware	Microsoft
Systems	Compaq
Silicon & Oxide	Intel & Seagate

Courtesy Andy Grove

Computing Laws

Structure of industry around DEC c1982

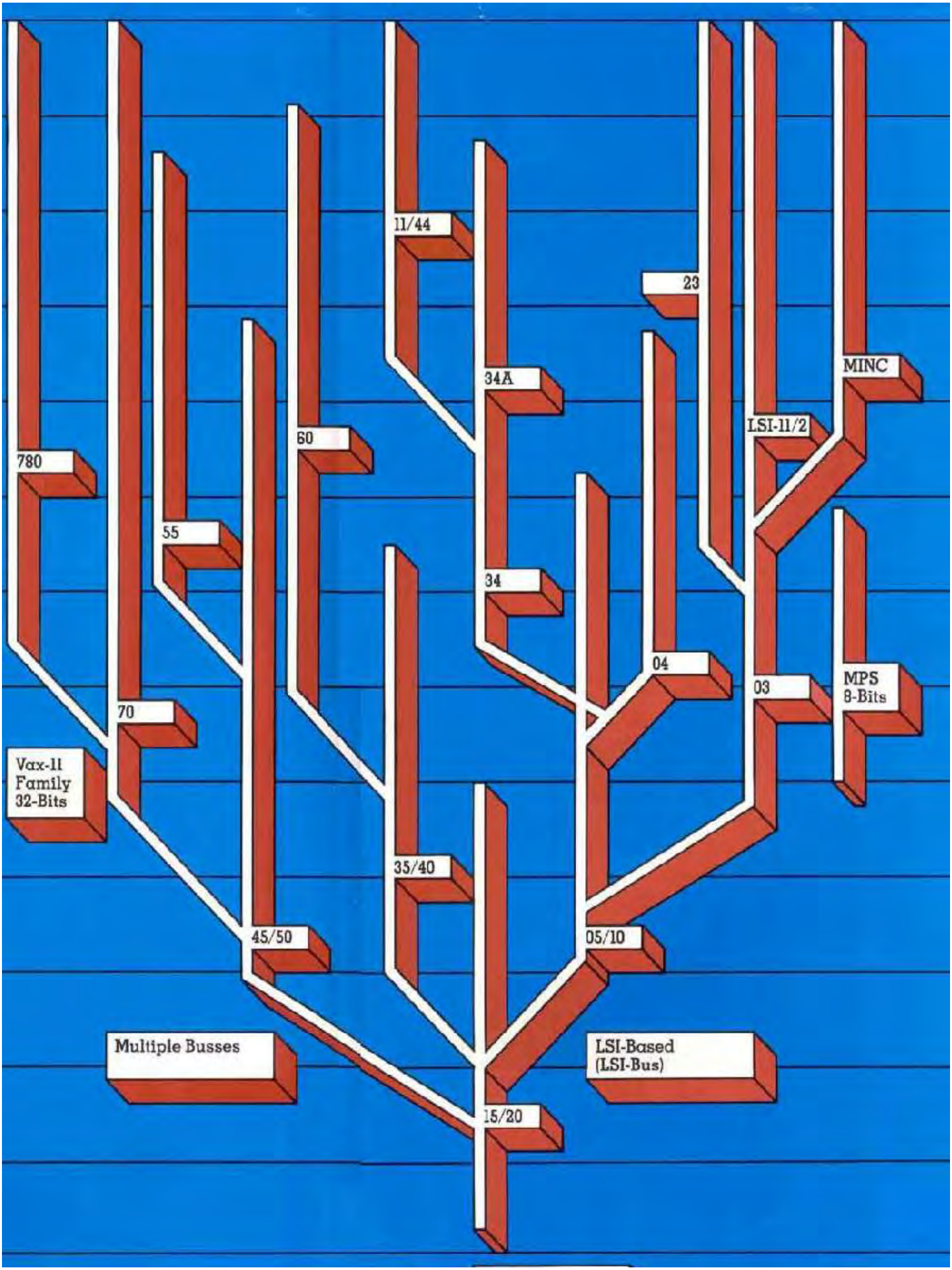


Bell's Law of Computer Classes & their Formation

End

The 41 year life and trials of Digital Equipment Corp. aka DEC

- 1960: Birth of DEC from MIT Lincoln Lab… its evolution
- 1965-1984+?: Birth and death of the minicomputer industry
- Theory: Bell's Law (of Computer Classes)
- **1978: VAX and the VAX Strategy to become number 2**
- 1985-: PCs, workstations, "killer micros" and standards take on all comers
- The DEC Organization and Culture... What happened?
- Summary…

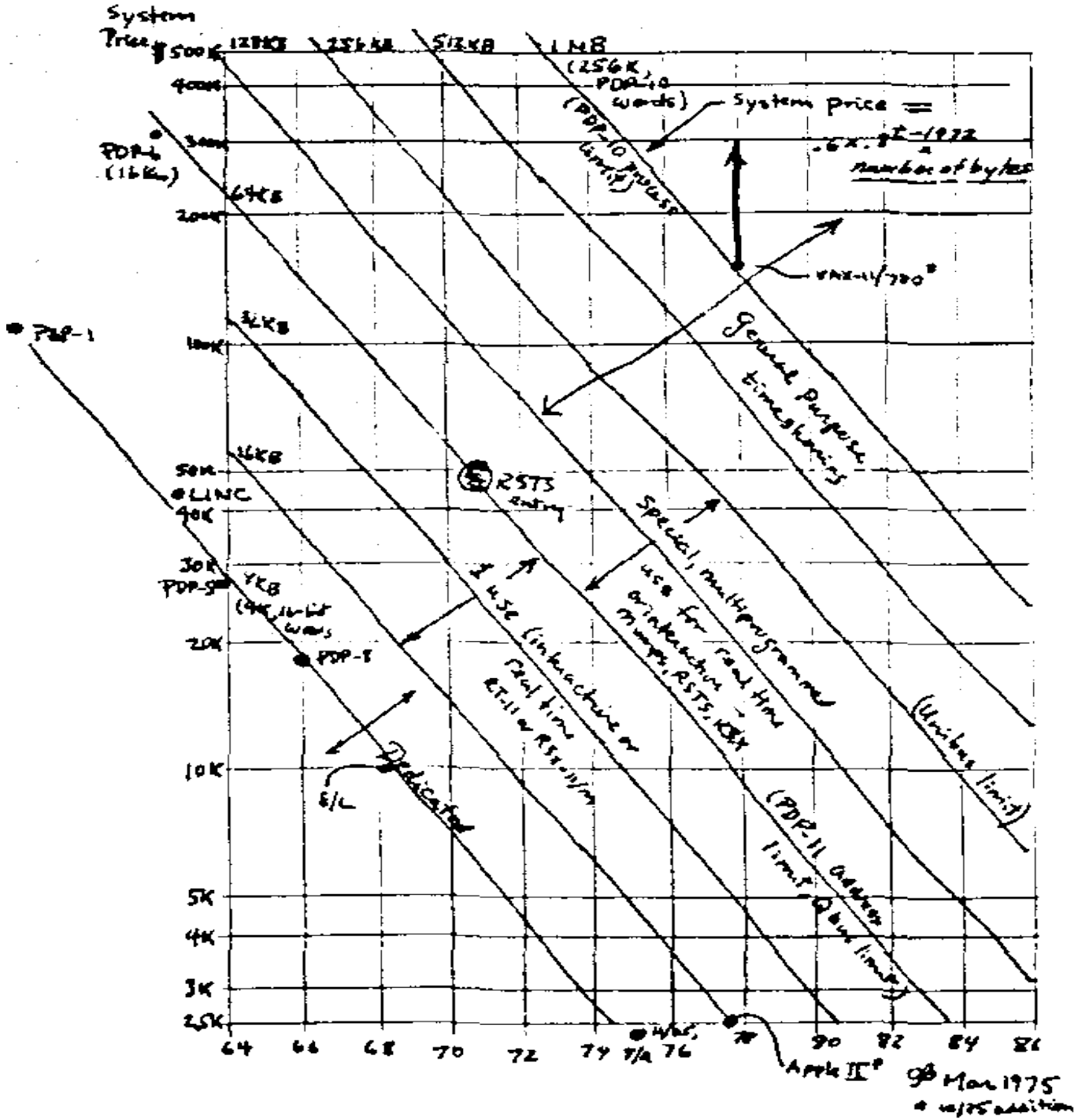

11/44
23
34A
MINC
LSI-11/2
60
780
55
34
04
MPS
8-Bits
03
70
Vax-11
Family
32-Bits
35/40
45/50
05/10
Multiple Busses
LSI-Based
(LSI-Bus)
15/20

VAX-A Bluebook 1 April 1975
Bell, Cutler, Hastings, Lary, Rothman, Strecker

Had we the foresight, it was clear the pure, 16-bit 11 was born to have a short, happy, prolific, profitable life. In 1969, an address of 16-18 bits, and a system size being sold of 13-15 bits, left only 3 bits of address growth left. At the constant-price historical memory growth rates of 26 to 41 percent per year, only 6 to 9 years of comfortable lifetime is allowed, bringing it to 1975-1978.

"There is only one mistake that can be made in a computer design that is difficult to recover from – not providing enough address bits for memory addressing and memory management. The PDP-11 followed the unbroken tradition of nearly every known computer.

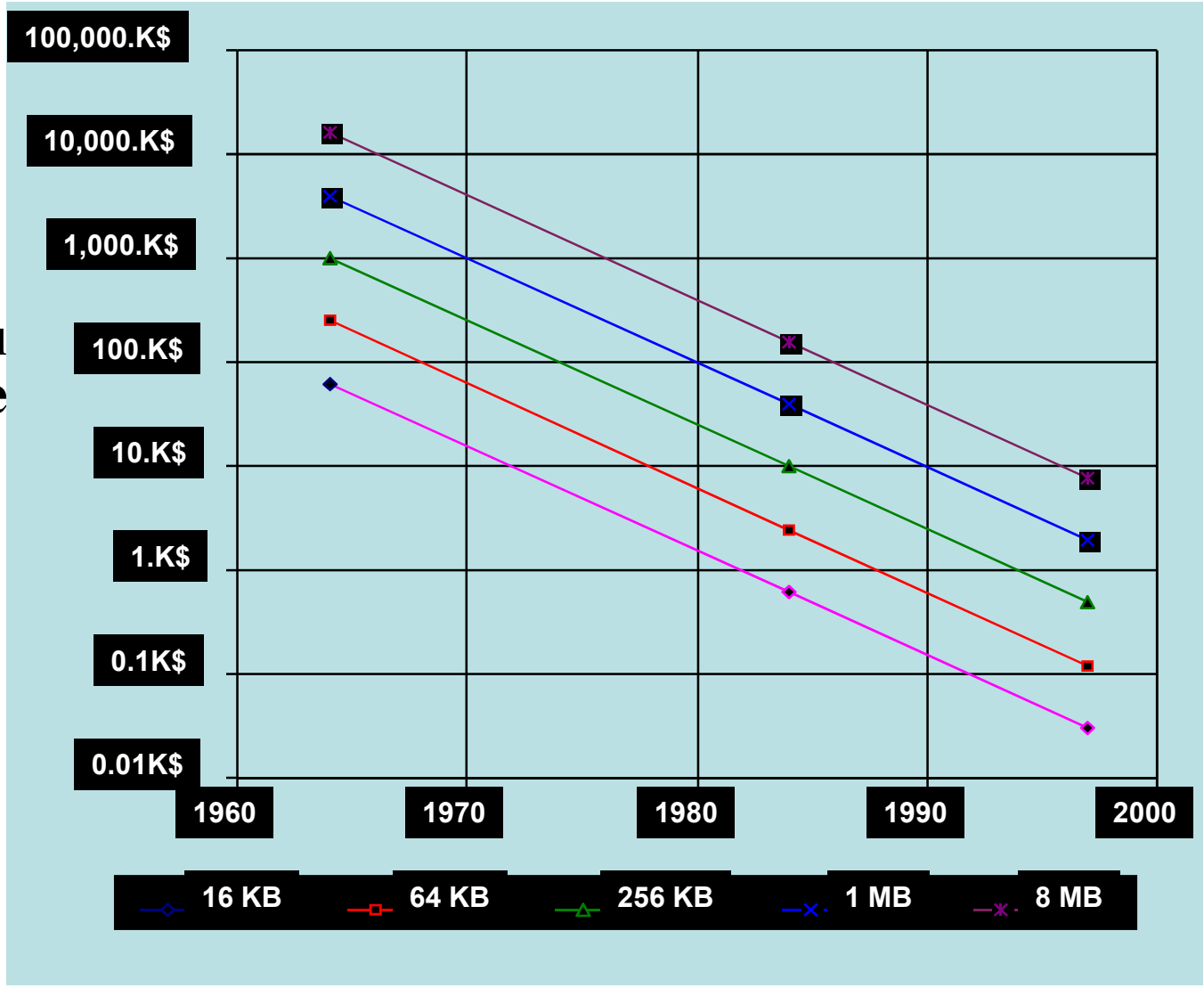
VAX Planning Model



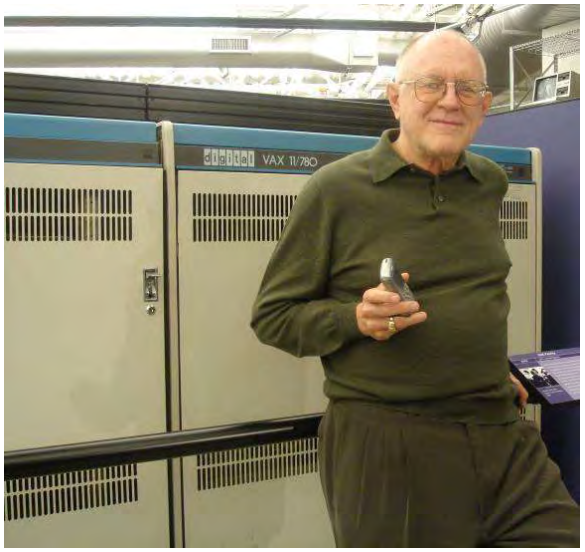
Gordon Bell's 1975 VAX Planning Model... I Didn't Believe It!

System Price = 5 x 3 x .04 x memory size/ 1.26 $^{(t-1972)}$ K$

- **5x: Memory is 20% of cost**
  3x: DEC marku
  .04x: $ per byte
- **Didn't believe: the projection $500 machine**
- **Couldn't comprehend implications**



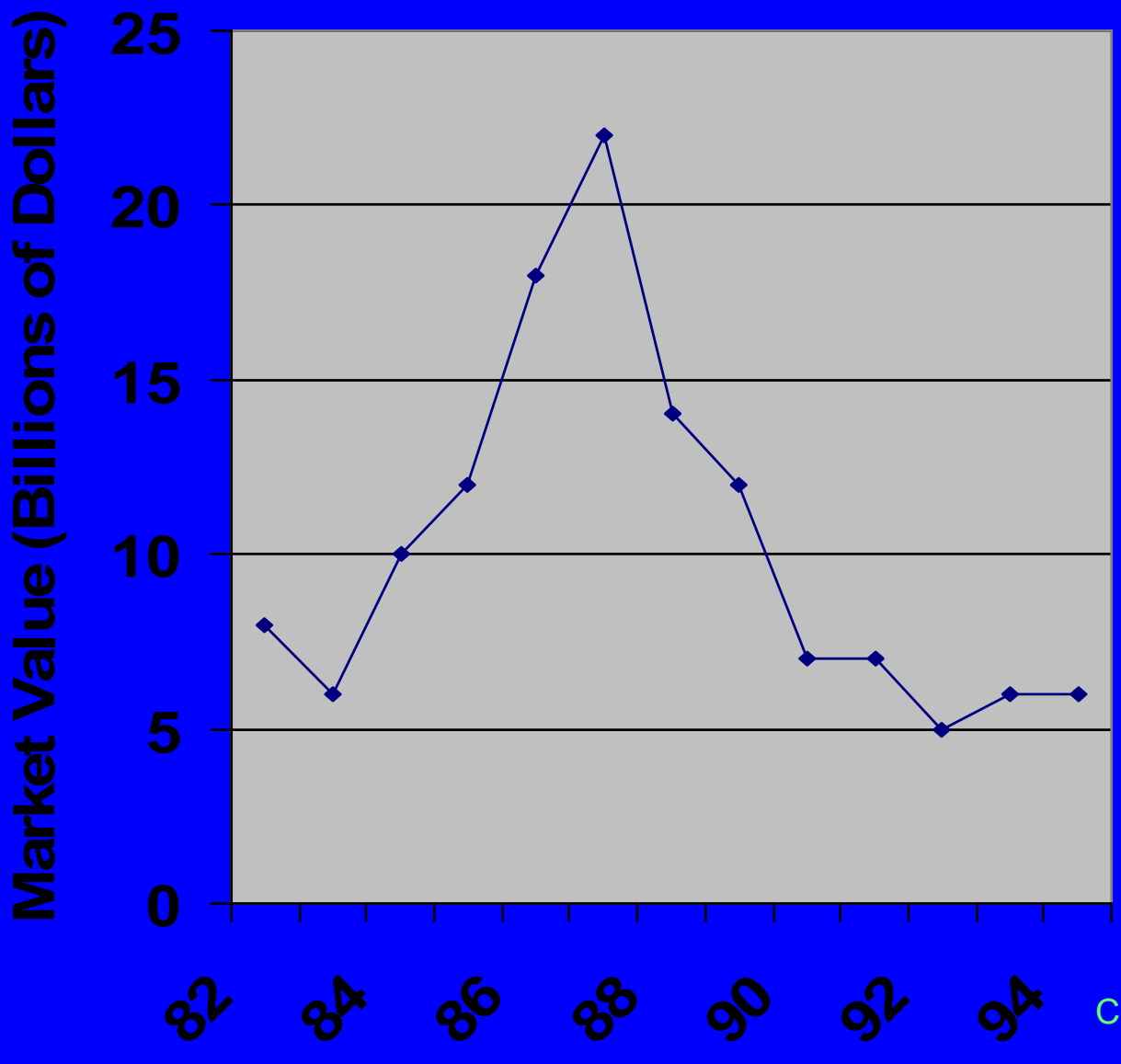
VAX/VMS Strategy (c1978)



…a homogeneous, distributed-computing system, where users interface, store information, & compute without reprogramming or extra work:

- via a cluster of large computers *using CI*,
- at local minis, workstations, & PC clusters,
- with interfaces to industry standard systems,
- interconnected via LANs *(Ethernet agreement was essential)*, Campus Area, & WANs

DEC Value Migration



Source: CDI Value Growth Database

Courtesy Pete DeLisi

The 41 year life and trials of Digital Equipment Corp. aka DEC

- 1960: Birth of DEC from MIT Lincoln Lab… its evolution
- 1965-1984+?: Birth and death of the minicomputer industry
- Theory: Bell's Law (of Computer Classes)
- 1978: VAX and the VAX Strategy to become number 2
- **1985-: "killer micros" enable PCs, workstations, and standards to take on all comers**
- The DEC Organization and Culture... What happened?
- Summary…

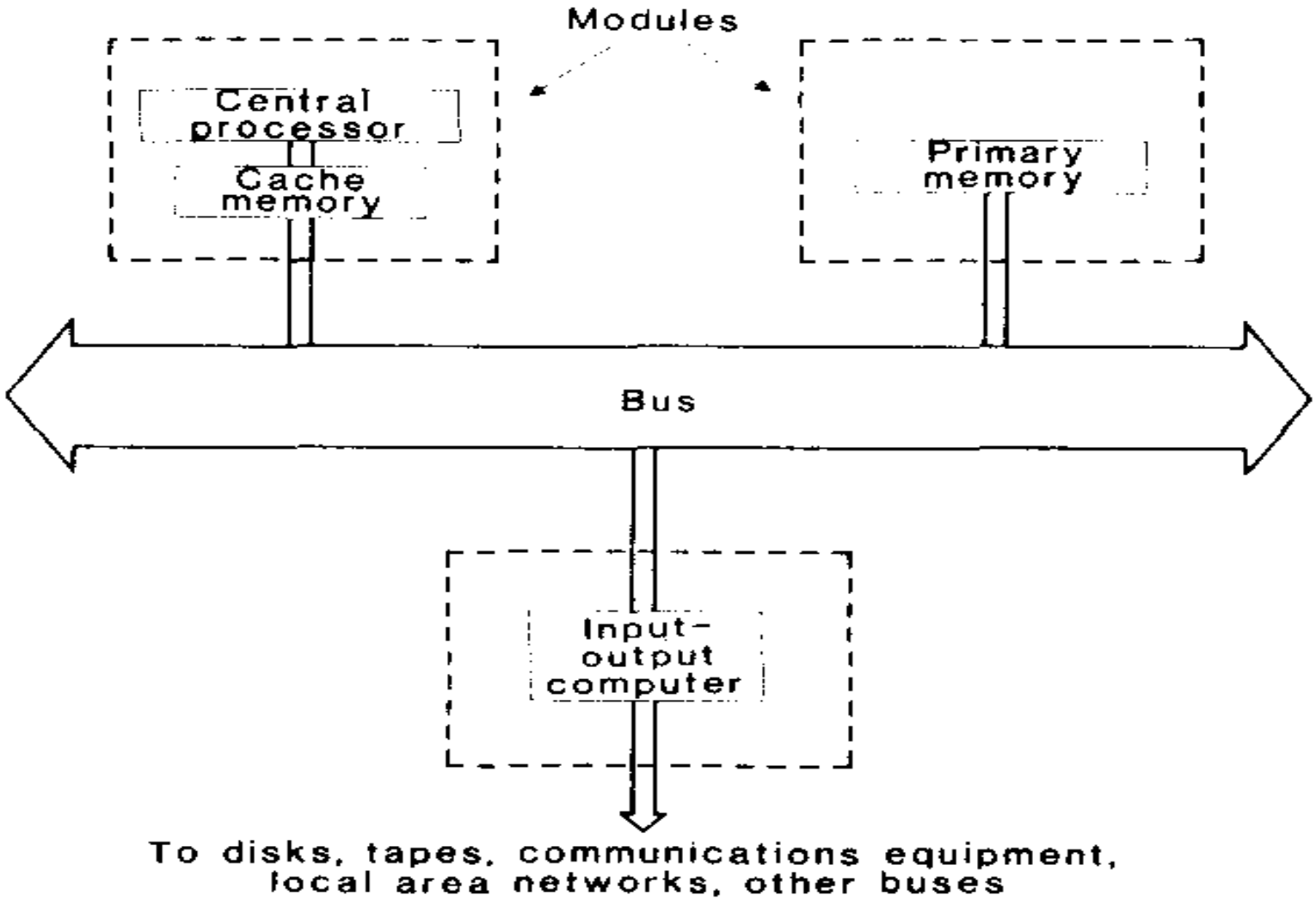
Motorola 68K, UNIX License, PC Standard:
Anyone can manufacture computers

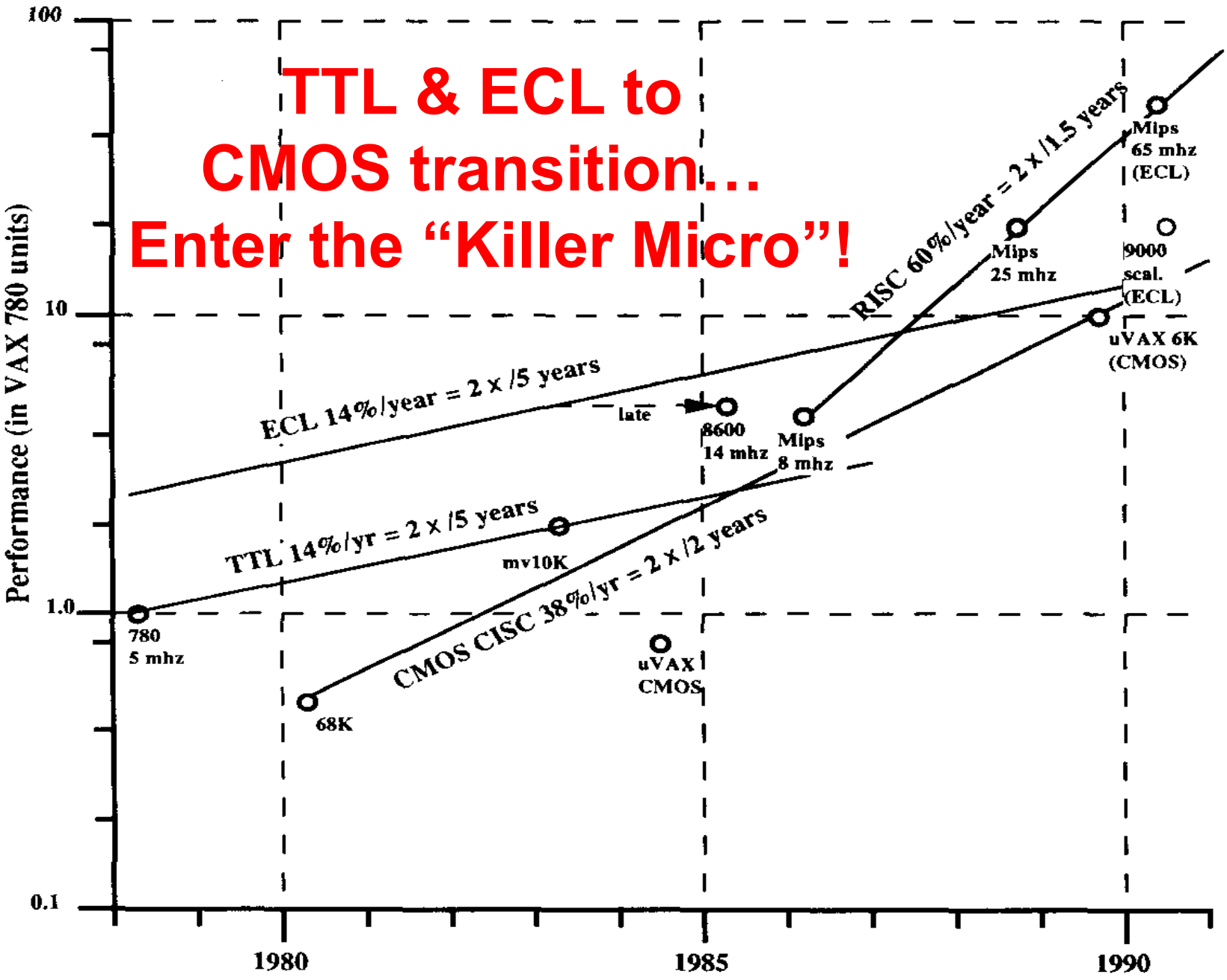
```
procedure  Entrepreneur_Venture_Cycle
    begin
    while  Frustration > Reward {Push
        from Old_co} and
    Greed > Fear {Pull to New
        company} do
    begin
    get (PC, spreadsheet);
    IF System_Company then
        write  (Beat_Vax_Plan)
        ELSE
        write (Plan)_
            New_Company
    get (Venture_capital);
        {from Old_Venture_Co}
    exit {job};
        start (New_Company);
end
```

get (UNIX License, developers)

```
get (Vax, development_tools);
build (product); sell (product);
sell (New_Company);
    {@ 100 × sales}
venture_funds : = Co._Sale
start (New_Venture_Co.);
end
```

Multis: Multiple, shared memory Microprocessors (Bell, Science 4/25/1985)




TTL & ECL to
CMOS transition…
Enter the "Killer Micro"!
Performance (in VAX 780 units)
100
10
1.0
0.1
1980
1985
1990
ECL 14%/year = 2 x /5 years
TTL 14%/yr = 2 x /5 years
CMOS CISC 38%/yr = 2 x /2 years
RISC 60%/year = 2 x /1.5 years
780
5 mhz
mv10K
68K
late
8600
14 mhz
uVAX
CMOS
Mips
8 mhz
Mips
25 mhz
Mips
65 mhz
(ECL)
9000
scal.
(ECL)
uVAX 6K
(CMOS)

The Challenge: Dealing with technology *transitions* and any ensuing standards

Technology = Change = Disruption

- 1957: Vacuum tube to Transistor circuits (high bar)
- 1965: Transistors to ICs… 100 mini companies
- 1971: 8 bit Microprocessor >> master VLSI;
  1981: IBM PC >> failure to embrace, only extend
- 1983: VLSI overtakes TTL AND ECL>> 9000 fail
- 1984+?+: UNIX and 32-bit micros >> standards fail
  "Either make the standard, or follow the standard.
  If you fail to set the standard, you get to do it twice."
- 1992: WWW Altavista, servers, clients. Mrkt'ng fail.

Digital's Trials by Technology…
With time, high tech becomes a commodity.

"DEC found guilty of violating Moore's Law …" –gbell

1. Designing and building first transistor circuits. 1957-1965
2. Transition to integrated circuits & modulo 8 bits 1965-1975
3. Design with VLSI; *manufacturing VLSI* *1975-2002*
4. Design of "clusters" as the ultimate computer 1983- ????
5. *Quadruple whammy c1983 – "killer" micros, UNIX: PC, Workstations, CMOS AND UNIX , as "standards" Anyone can manufacturer computers in their dorm! "You mean to say, our new ECL mainframe is not equal to our latest CMOS chip?" –Ken Olsen c1990*
6. *Fail to exploit: networks, WWW, printers, clusters…*

Kampas' Pros & Cons products

- Leading 12, 16, 32-bit minis & OS's
- Leading video terminals
-Leading printing terminals (LA-xx), first desktop lasers
- First www products
- Leading OEM business
- Leading office software
- Effective divisional structure

- MicroVAX II (M68000 + 8yrs)
- VAX 8600 (8 years after 780)
- VAX 9000 was unsuccessful >$1B investment (1990)
- RISC/Alpha (via MIPS; 6 years after Sun/HP)
- Never fully endorsed Unix Olsen: "snake oil"
-Late to TCP/IP from OSI
- Late to IBM-compatible PC -(Rainbow, Pro, DECmate)
- Failed to divisionalize
- Failed at low cost capability

-In the end: SEVEN Platforms VAX, X86, MIPS and Unixes

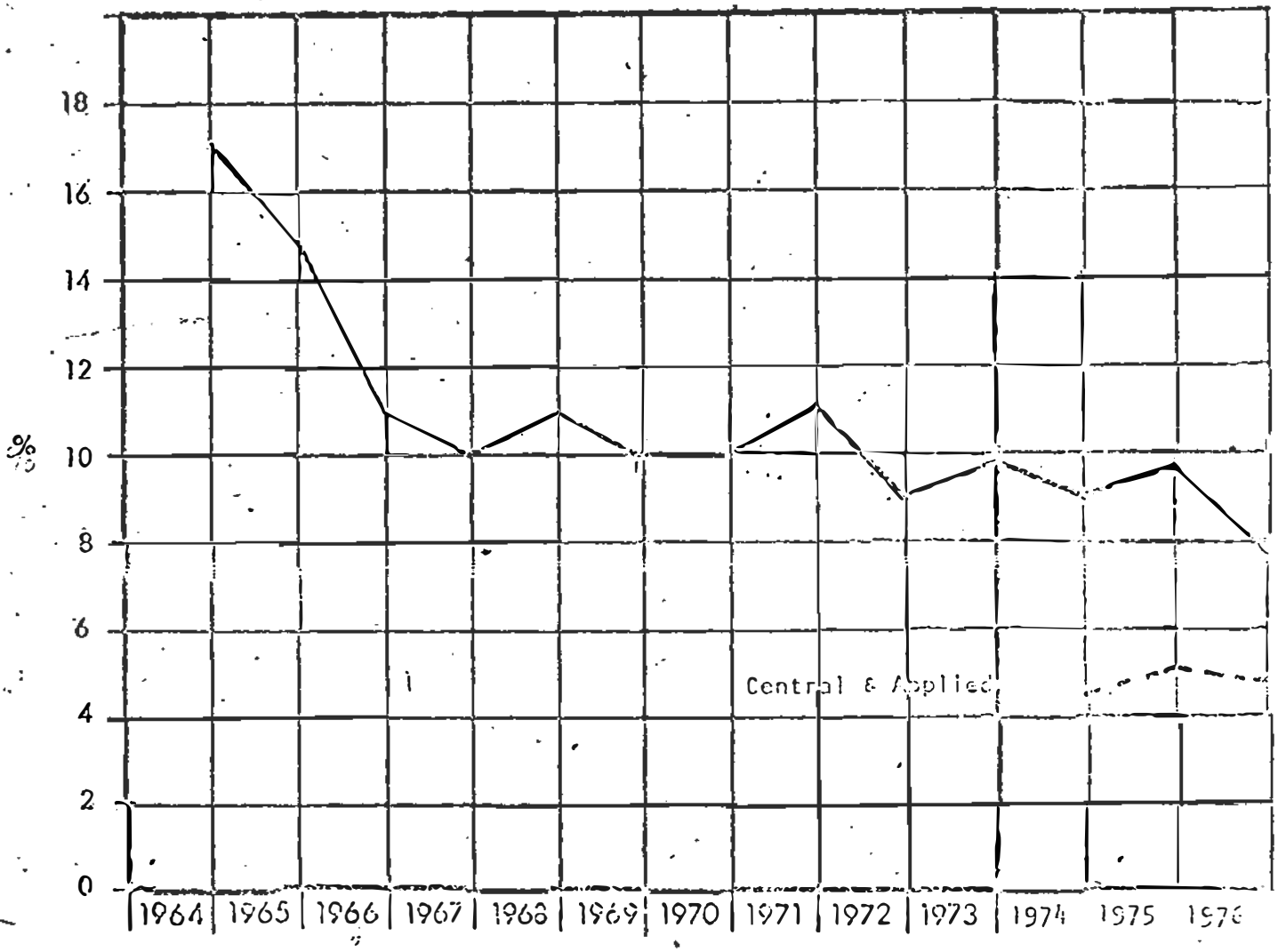
Copyrighted material

The 41 year life and trials of Digital Equipment Corp. aka DEC

- 1960: Birth of DEC from MIT Lincoln Lab… its evolution
- 1965-1984+?: Birth and death of the minicomputer industry
- Theory: Bell's Law (of Computer Classes)
- 1978: VAX and the VAX Strategy to become number 2
- 1985-: PCs, workstations, "killer micros" and standards take on all comers
- **The DEC Organization and Culture... What happened?**
- Summary…

- Stories
  - PDP-1; ITT Store & Forward Switch… UART
  - PDP-6 from PDP-3. Compiler
  - PDP-5 how it was created & PDP-8
  - PDP-11 at CMU
  - VAX and VAX Strategy… address bit problem
  - Ethernet DIX, Liddle,

Copyrighted material

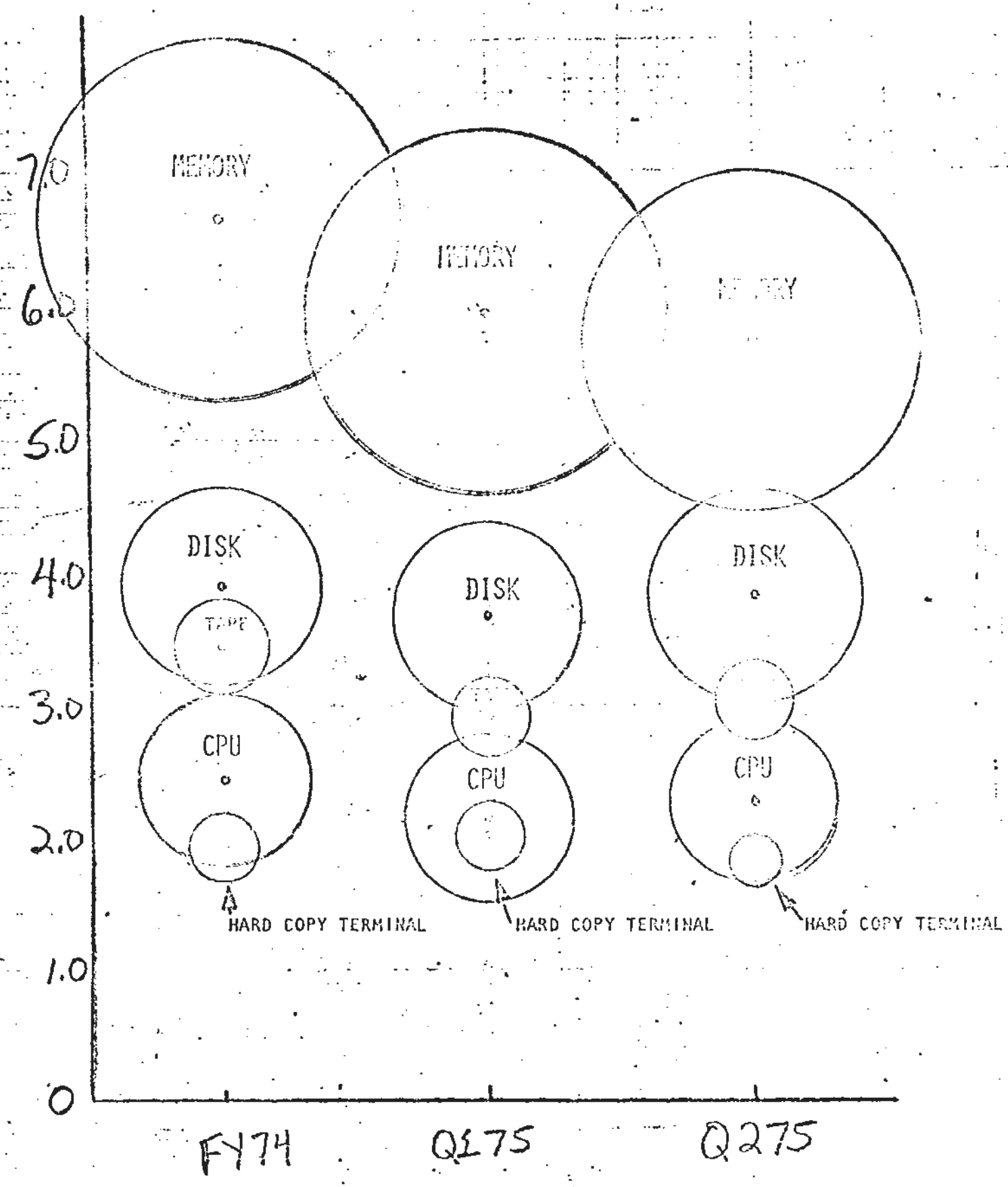


RESEARCH & ENGINEERING AS A % OF NET SALES

Figure I

Phil Leut
8/13/73
8/10/74
3/25/75

10/72 KNO-SLIDE 2

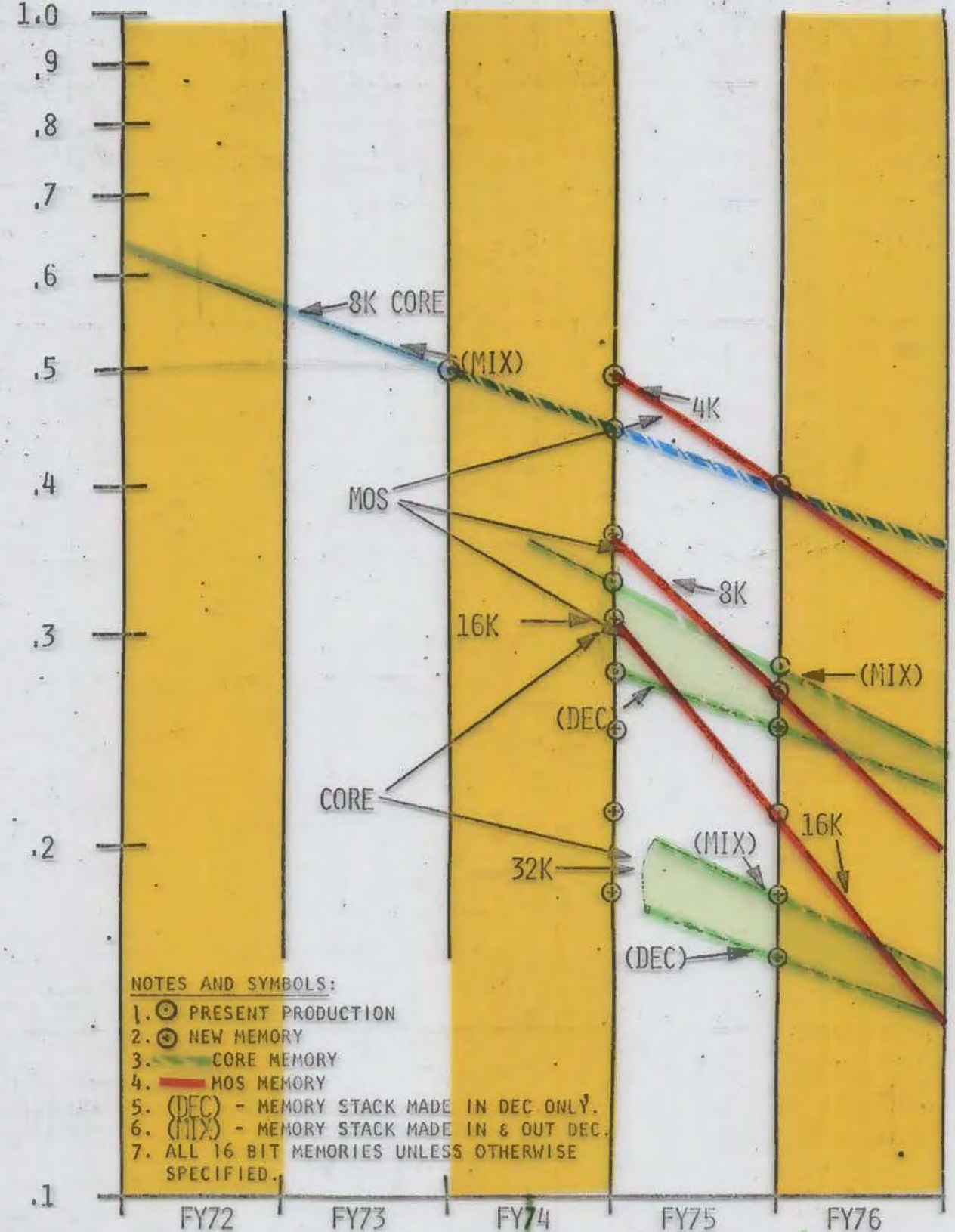


GROSS MARK UP & SALES ANALYSIS

Phil Laut
6/11/75

PDP-11

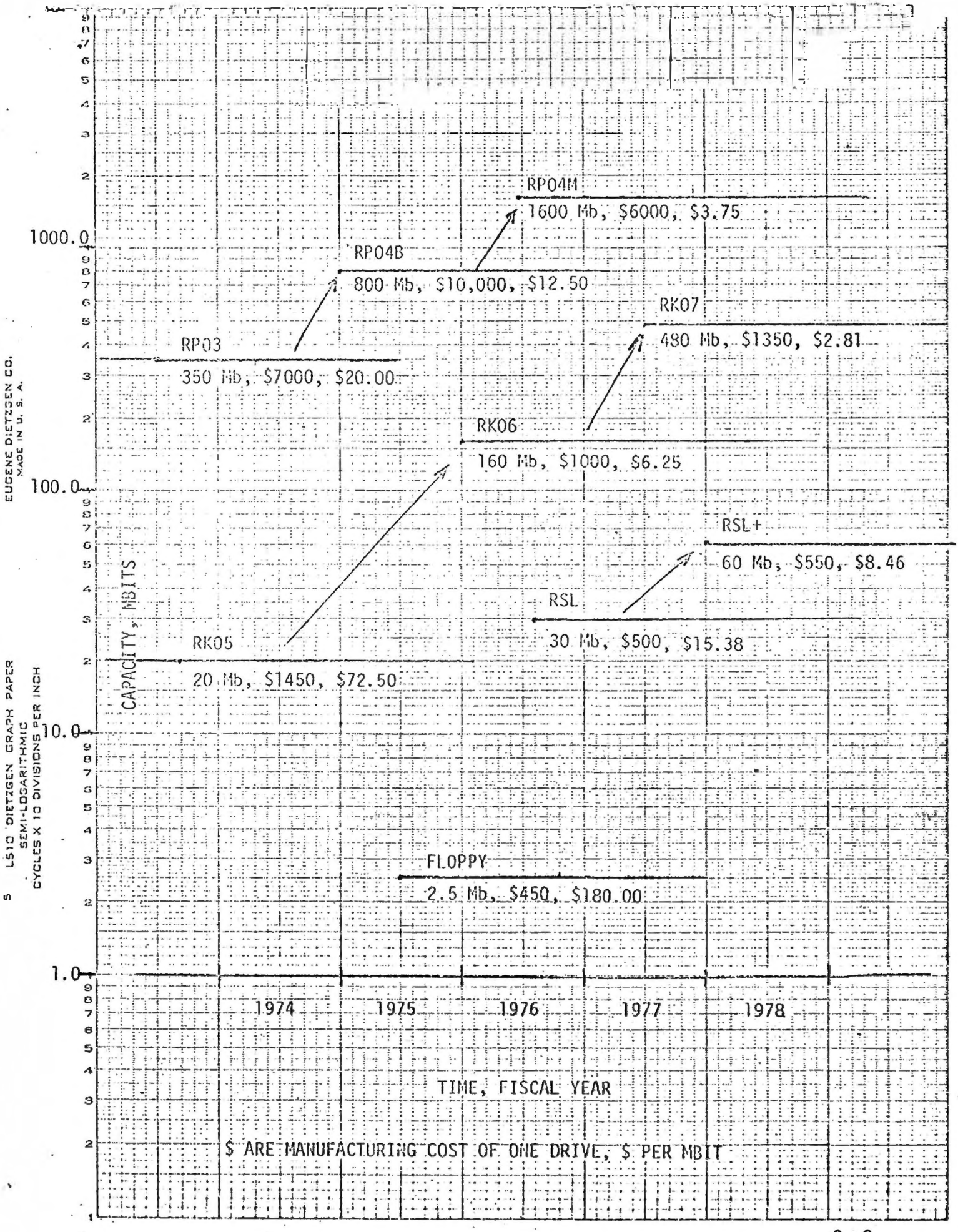
COST/BIT (¢) VS TIME



NOTES AND SYMBOLS:

1. ⊙ PRESENT PRODUCTION
2. ⊙ NEW MEMORY
3. CORE MEMORY
4. MOS MEMORY
5. (DEC) - MEMORY STACK MADE IN DEC ONLY.
6. (MIX) - MEMORY STACK MADE IN & OUT DEC.
7. ALL 16 BIT MEMORIES UNLESS OTHERWISE SPECIFIED.

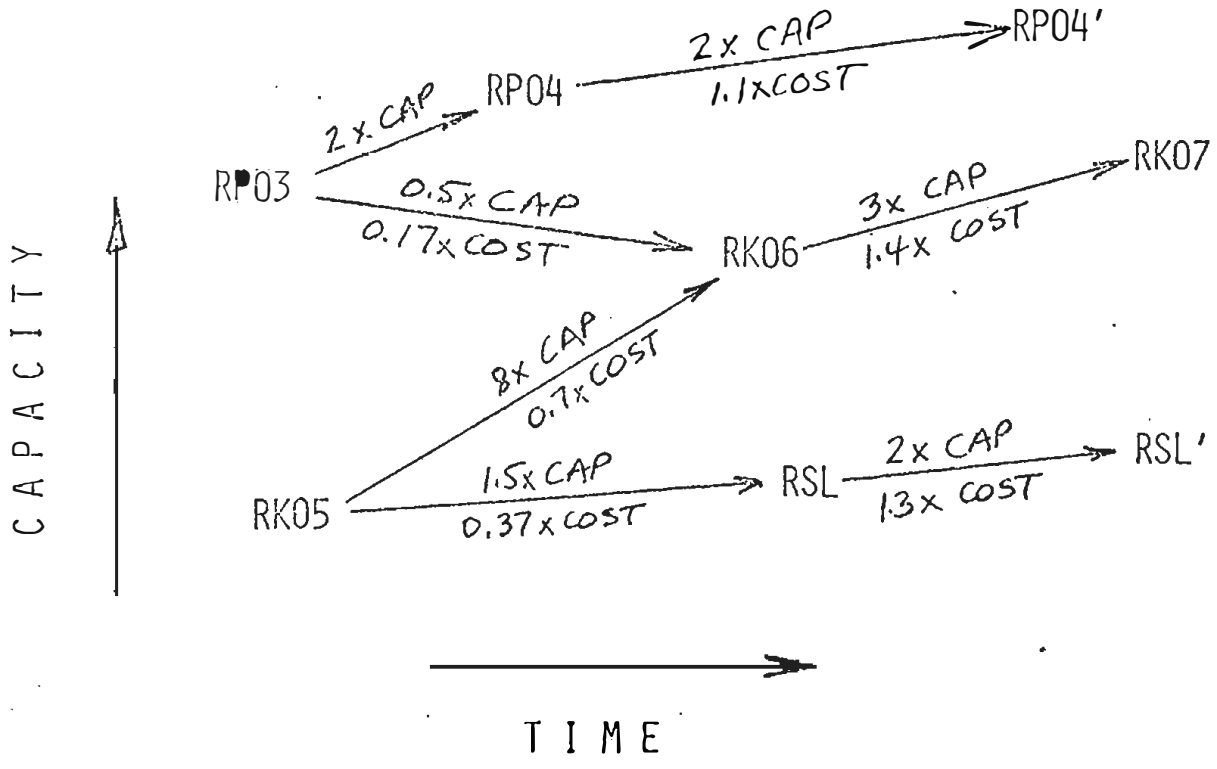
GB/DEC Projection Dec. 73


RP04M
1600 Mb, $6000, $3.75
RP04B
800 Mb, $10,000, $12.50
RK07
480 Mb, $1350, $2.81
RP03
350 Mb, $7000, $20.00
RK06
160 Mb, $1000, $6.25
RSL+
60 Mb, $550, $8.46
RSL
30 Mb, $500, $15.38
RK05
20 Mb, $1450, $72.50
FLOPPY
2.5 Mb, $450, $180.00
1000.0
100.0
10.0
1.0
CAPACITY, MBITS
1974
1975
1976
1977
1978
TIME, FISCAL YEAR
$ ARE MANUFACTURING COST OF ONE DRIVE, $ PER MBIT
EUGENE DIETZGEN CO.
MADE IN U. S. A.
5 L510 DIETZGEN GRAPH PAPER
SEMI-LOGARITHMIC
CYCLES X 10 DIVISIONS PER INCH
NO. 340

G. S.
11/28/73

CUSTOMER GROWTH

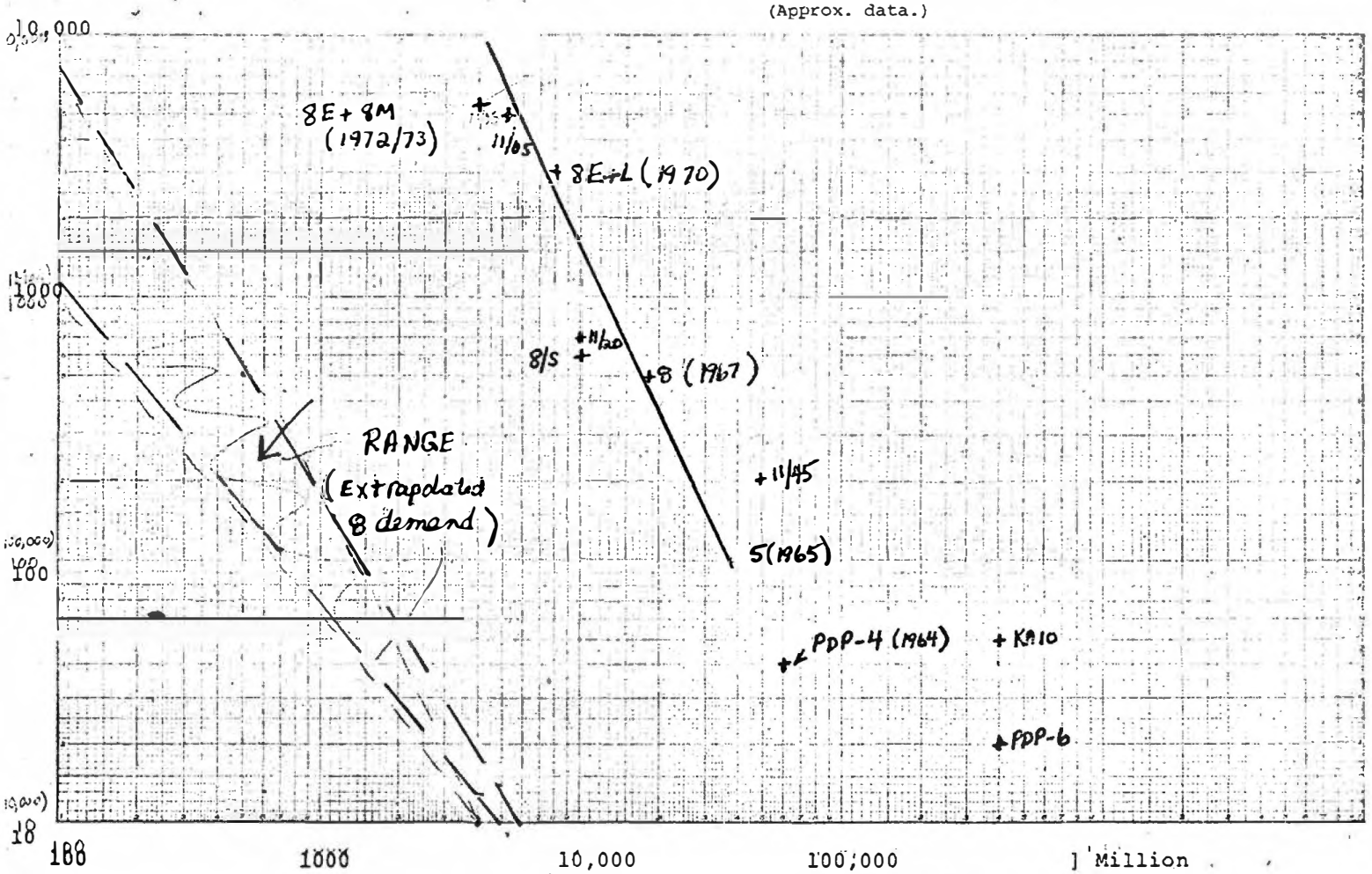
DEC MOVING HEAD/ REMOVEABLE MEDIA DISKS



ALTERNATIVES: 1. CONSTANT COST, INCREASED CAPACITY

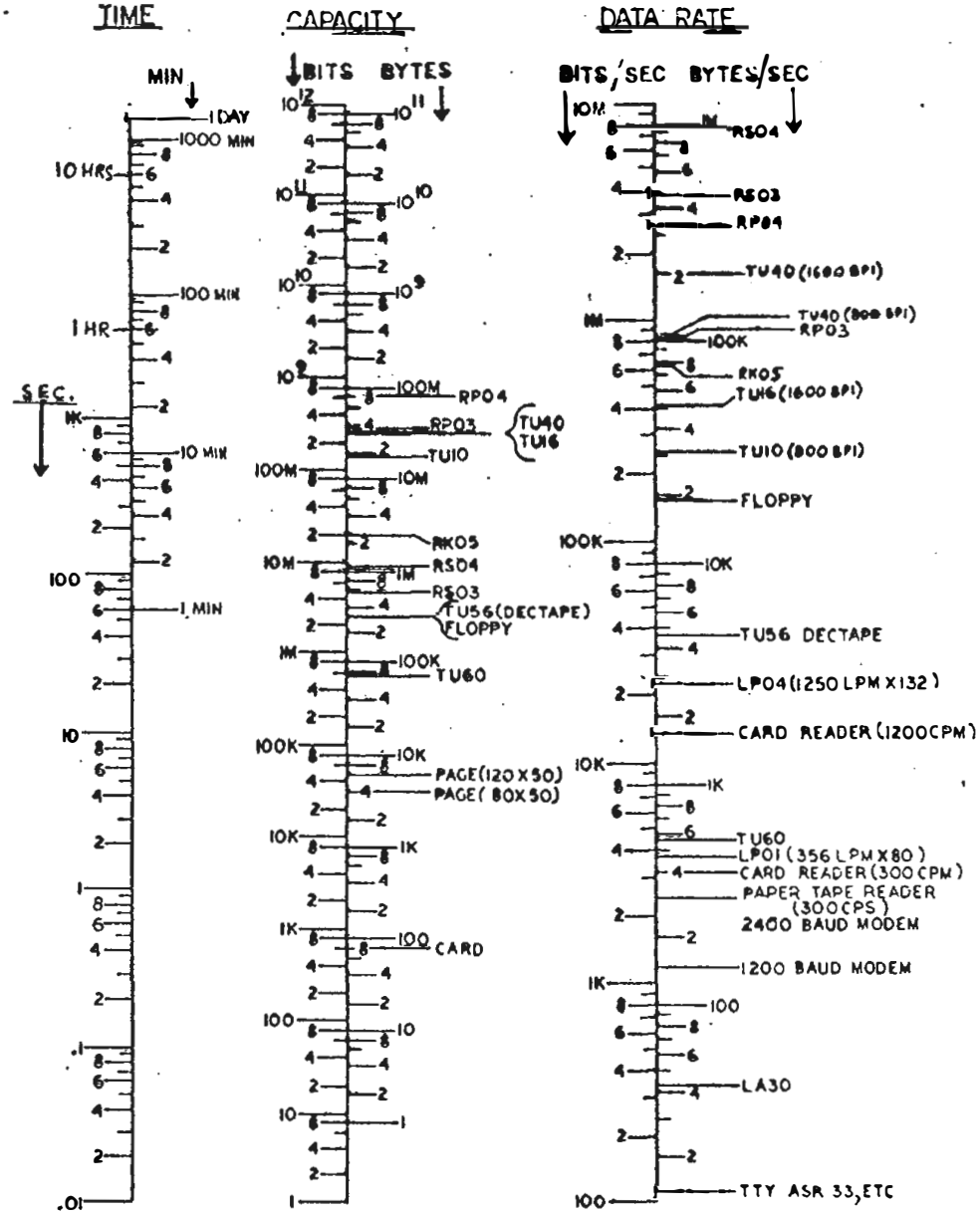
2. DECREASED COST, CONSTANT CAPACITY

(1st year--after start-up transient.) Figure 3 DEMAND FOR VARIOUS PRICED COMPUTERS
(Approx. data.)



8/8/73 gp

DATA TRANSFER TIME BETWEEN DIFFERENT MEDIA



NOTES:

1. Products are marked at average data rate.
2. Average data rate (disks) = $\frac{\text{Formatted Track Capacity}}{\text{Access Time to Index + Rotation Time}}$
3. Average data rate (rest of divices) = Nominal Data Rate x $\frac{\text{Length of Data Field}}{\text{Length of Block}}$

   (Block includes, as appropriate, gaps, header, CRC, head and bottom of page, margin etc.
4. Tape block sizes:
   - TU10 & TU16 - 1024 (16 bit) words
   - TU40 - 4096 (36 bit) words
   - TU56 & TU60 - 256 (16 bit) words

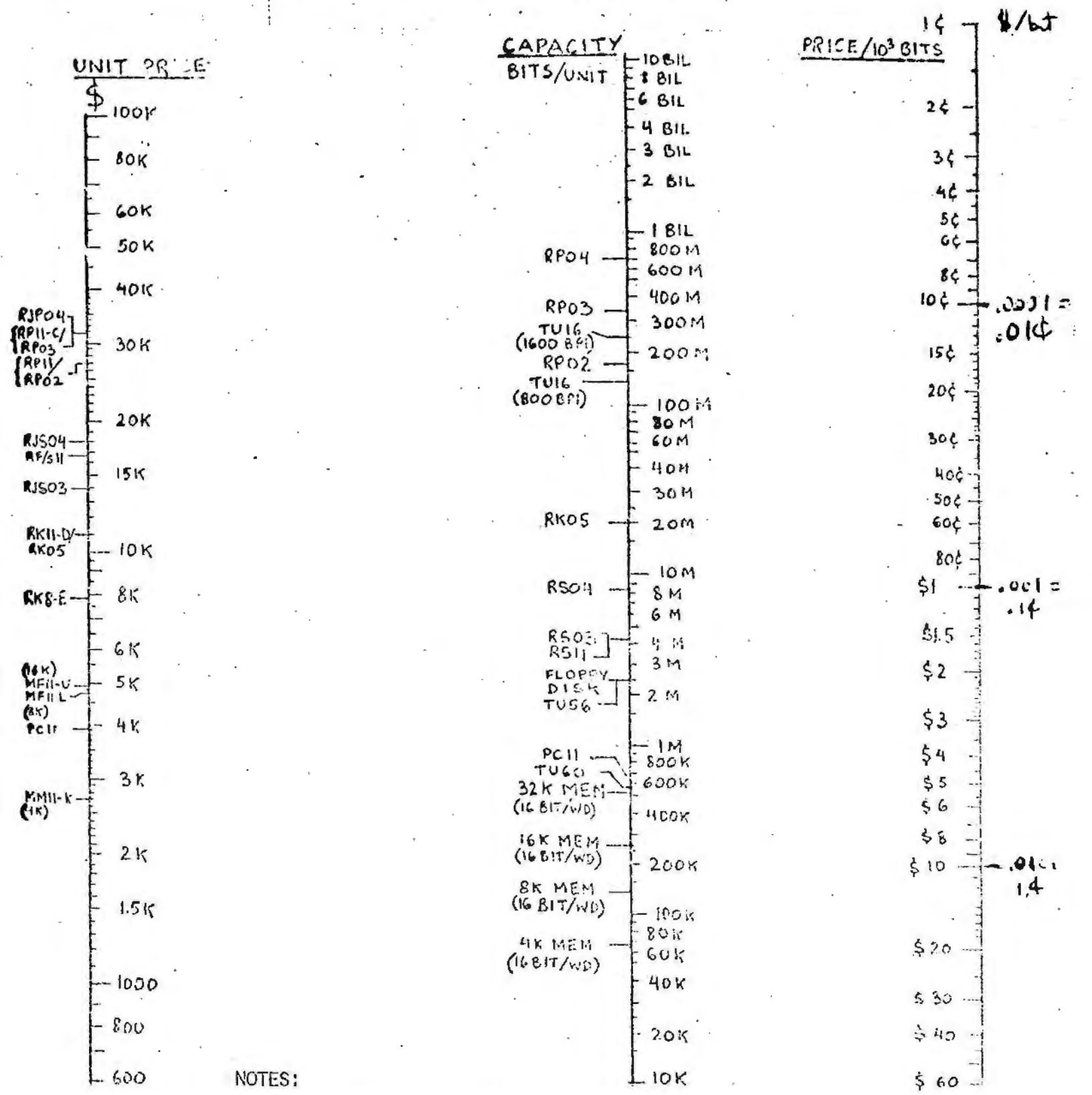
   Data rates for small blocks:
   - TU10 - 256 (16 bit wds) - 160kbit/s
   - TU16 - 256 (16 bit wds) - 224kbit/s
   - TU40 (1600bpi) - 256 (36 bit wds)- 1.06Mbit/s

HOW TO USE:

Example: to determine time to transfer the contents of RK05 cartridge to TU16 tape reel, locate TU16 on "data rate" scale and RK05 on "capacity" scale. Extend straight line between them to "time" scale. Time to transfer data about 4.2 seconds (excluding disk and tape mounting time.)

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

DATA STORAGE COSTS



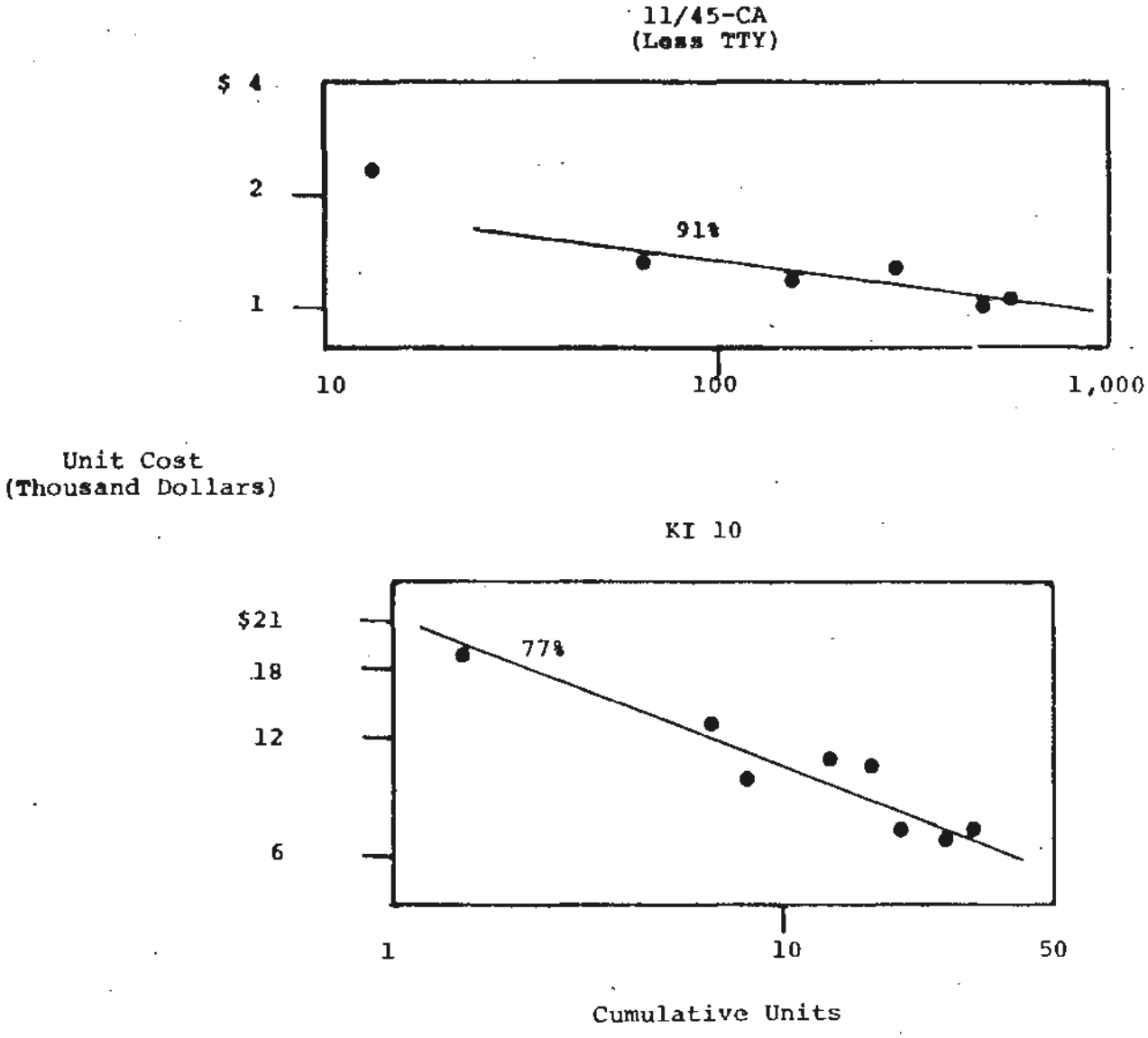
NOTES:

1. ALL UNIT PRICES SHOWN INCLUDE 1 STORAGE MODULE (E.G. DISK DRIVE) + INTERFACE TO I/O BUS (E.G. CONTROLLER).
2. CAPACITY OF UNITS SHOWN ARE FORMATTED.
3. PRICE SCALE IS ON A BASIS OF 1000 BITS

A. SHARON 12/74

EXHIBIT 3

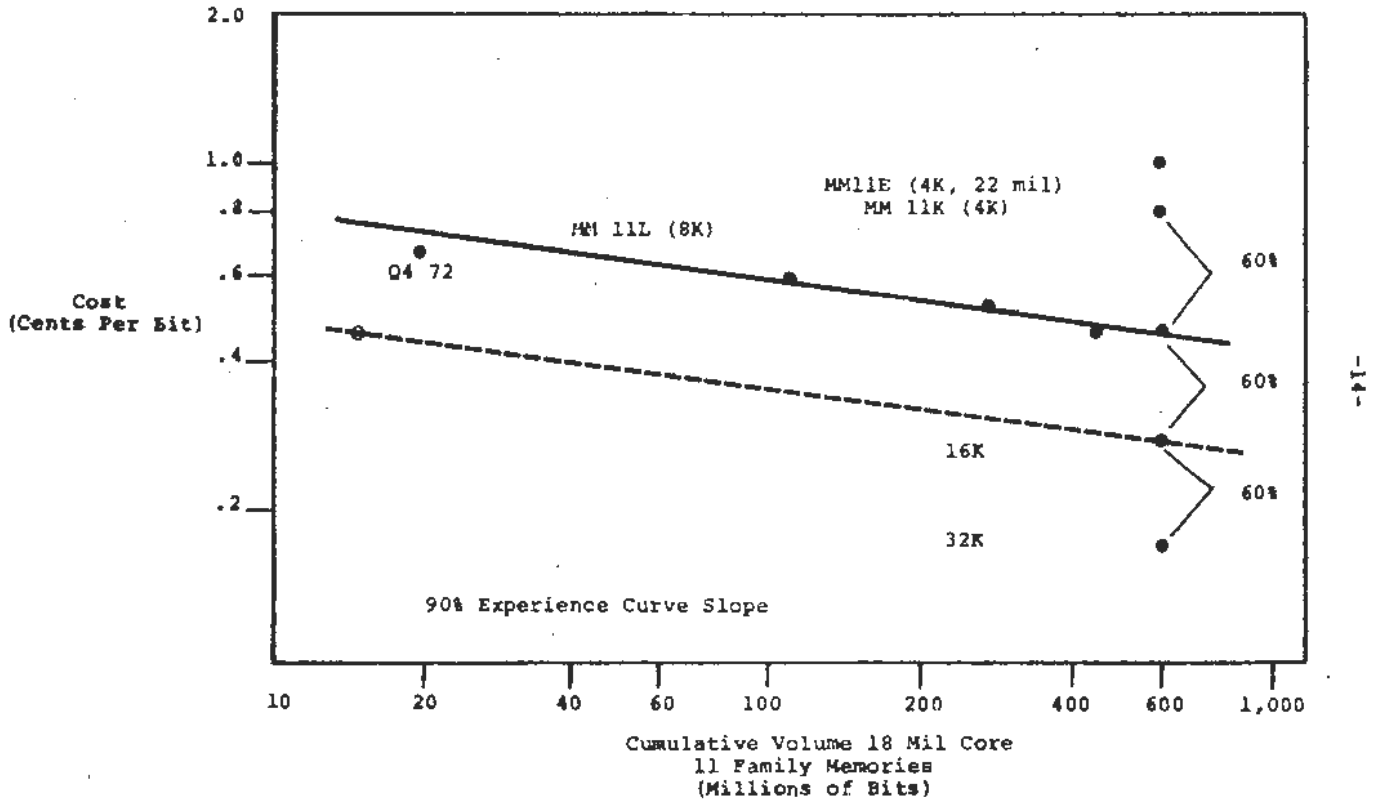
PRODUCT SPECIFIC COSTS



Source: Pink Book Data

EXHIBIT 9

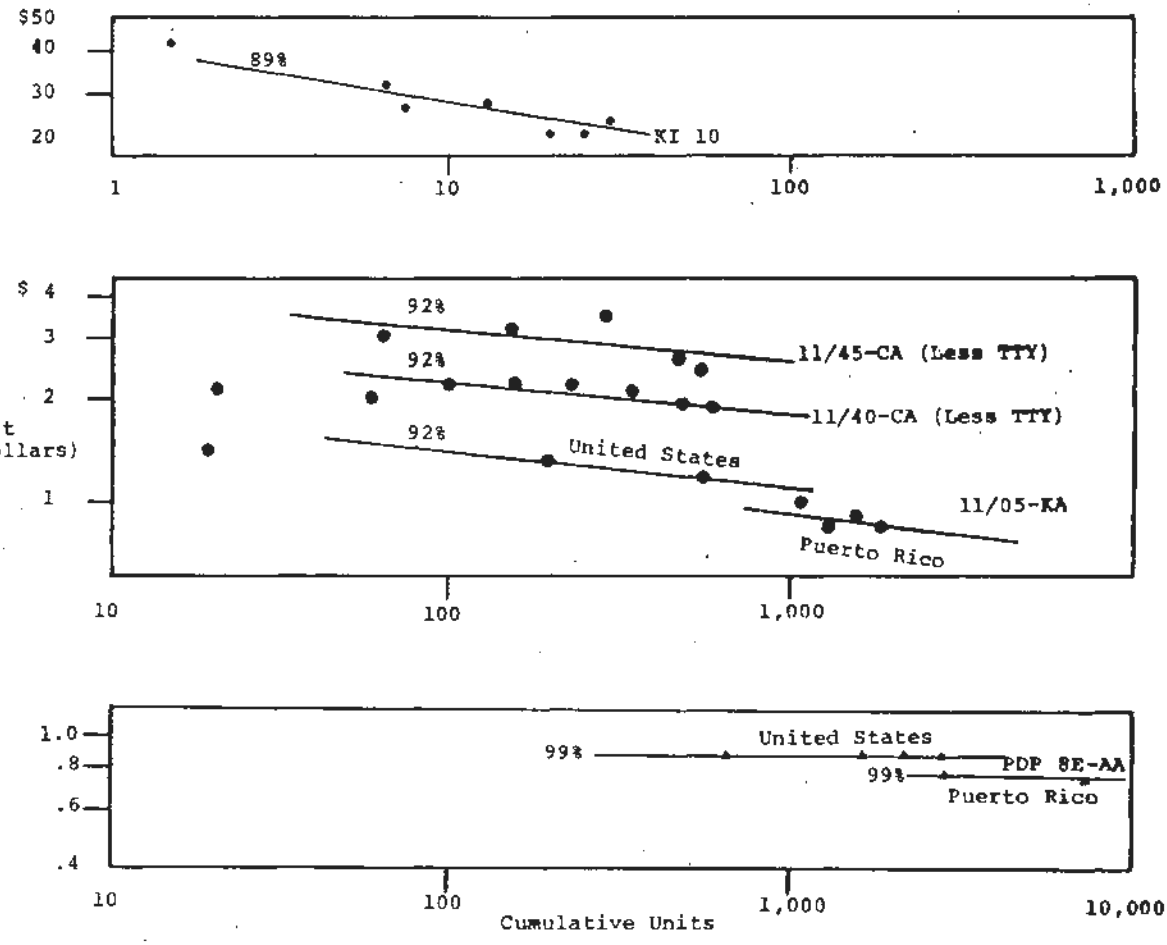
MEMORY TECHNOLOGY AND COSTS



Source: Pink Book Data and estimates from Phil Laut

EXHIBIT 1

CPUs
VALUE ADDED



Source: Pink Book Data

IMPLEMENTATION

OFFICE OF DEVELOPMENT

CLAYTON - SYSTEMS

8, 11, FUTURE SYSTEMS, INTERNAL MARKETING, PLANNING, 11-FIDELITY AND SYSTEMS

PUFFER - COMPUTER COMPONENTS AND SERVICES

TAPES, DISKS, PRINTING DEVICES, PACKAGING, POWER, SEMICONDUCTOR COMPONENTS, AND SERVICES

PORTNER - SOFTWARE PRODUCTS

SOFTWARE SUPPORT, SOFTWARE PRODUCTS (FOR ALL SYSTEMS) APPLICATIONS, DIAGNOSTICS/ MANUFACTURING, ADVANCED DEVELOPMENT AND CONSULTING, COMPUTATIONAL FACILITIES

LAUT

LEMAIRE

G.Bell
3/74

ENGINEERING ORGANIZATIONAL CHANGE

0. ESTABLISH PRODUCT DEVELOPMENT BUSINESS

1. INTEGRATE PLANNING AND DEVELOPMENT WITH HARDWARE-SOFTWARE

2. PLAN OF OPTIONS SYNCHRONIZED WITH SYSTEMS AND SOFTWARE

3. PRODUCT MANAGER ALIGNMENT WITH PRODUCTS--ROLES EXPANDED

4. INCREASED CAREER DEVELOPMENT

G.Bell
3/74

COMPATIBILITY AND STANDARDS: GOALS

SOFTWARE (ALL MACHINES)

- COMMAND LANGUAGE FOR (INTERACTIVE AND BATCH)
- SCIENTIFIC SUBROUTINE PACKAGES
- LANGUAGES (ALGOL, APL, BASIC, BLISS, COBOL-73, FOCAL, FORTRAN, MACRO (SYNTAX), PL/1...
- UTILITIES (PIP, ET AL)
- EDITORS (TECO--NOW, NEW LINE-ORIENTED)
- FILES
- COMMUNICATIONS PROTOCOL FOR MESSAGES (DDCMP)
- COMMON FRONT END MACHINES FOR 10 AND 11
- MONITOR INTERFACE FOR PDP-11's

G.Bell
3/74

PROFESSIONAL ENVIRONMENT GOALS

- THE PERSON WHO DOES THE PLAN, DOES.
- CONTINUED EDUCATION (INCLUDING MANAGEMENT TRACT)
- MEASURES FOR ALL
- ENCOURAGE PRODUCTS--AND IF USEFUL, PAPERS AND PATENTS

G.Bell
3/74

SIGNIFICANT MANUFACTURE OF PRODUCTS GOALS

- SIGNIFICANT SUPPLIER < $200K
- ATTEMPT TO BRIDGE GAP TO 10...AGAIN
- INCREASED DEVELOPMENTS AT LOW END (60% ALLOCATION)
- INCLUDING SEPARATED PERIPHERALS
- TWO PRODUCT TYPES
  - OEM TYPE: COST ORIENTED
  - SYSTEM TYPE: HIGH PERFORMANCE AND RELIABILITY
- DIRECTLY COUPLED SYSTEMS (NON-BATCH)
  - .TO HUMAN, INTERACTIVE USER
  - .TO PROCESS
  - .TO OTHER COMPUTERS
- ECOLOGICALLY CLEANER
  - .LESS POWER
  - .LESS PAPER, CARDS
  - .SUBSTITUTE INFORMATION FOR TRANSPORTATION

G.Bell
3/74

COMPATIBILITY AND STANDARDS: BENEFITS

- MOBILITY AMONG OUR MACHINES
- USERS DO NOT HAVE TO RE-LEARN TO BUY (WE OBSOLETE OUR EQUIPMENT--NOT OUR CUSTOMERS)
- OUR OWN LEARNING IS PRESERVED
- FEWER MANUALS, SPARE PARTS, AND INVENTORY
- WE CAN BUILD NETWORKS
- WE CAN WORK ON MORE CAPABILITIES FOR USERS INSTEAD OF BASIC SYSTEM
- WE CAN WORK ON LOWER COST AND/OR BETTER PRODUCTS INSTEAD OF LOW LEVEL RE-INVENTIONS

G.Bell
3/74

COMPATIBILITY AND STANDARDS: GOALS

HARDWARE (ALL MACHINES)

- STANDARD BUSSES FOR COMMON PERIPHERALS
  - 20MA AND EIA SERIAL LINES
  - UNIBUS FOR LOWER SPEED I/O
  - MASSBUS FOR STORAGE DEVICES (EG. RP, RS, TU16+, RK06+
  - NEW SERIAL, MULTIDROP 0.5 MHZ LINE FOR LOW COST, REMOTE PERIPHERALS

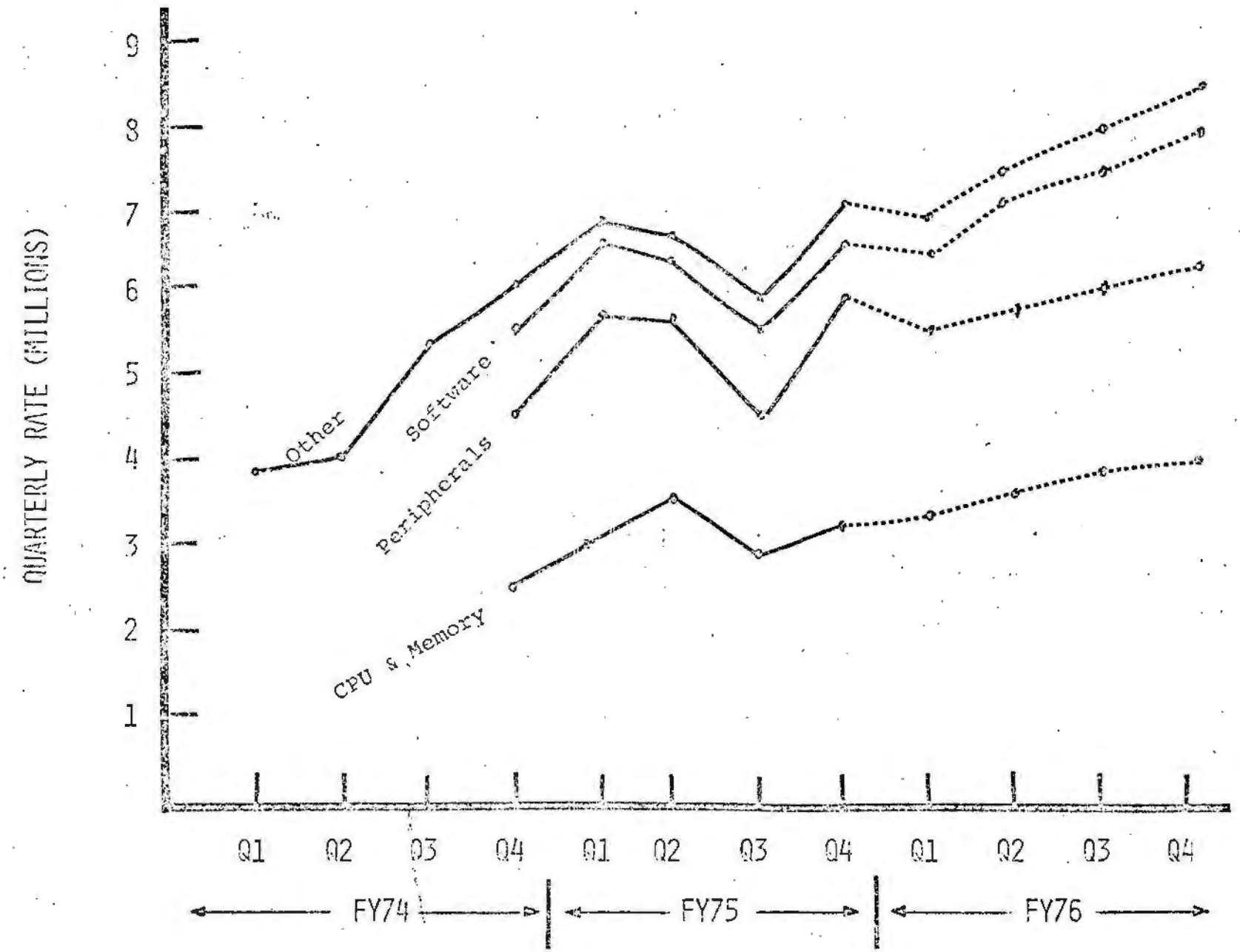
HARDWARE (COMPONENTS)

- PARTS (IC'S, CAPACITORS, ETC.)
- CABINETS, BOXES, POWER SUPPLIES
- MORE SYSTEMS BY PROGRAMMING--NOT LOGIC DESIGN

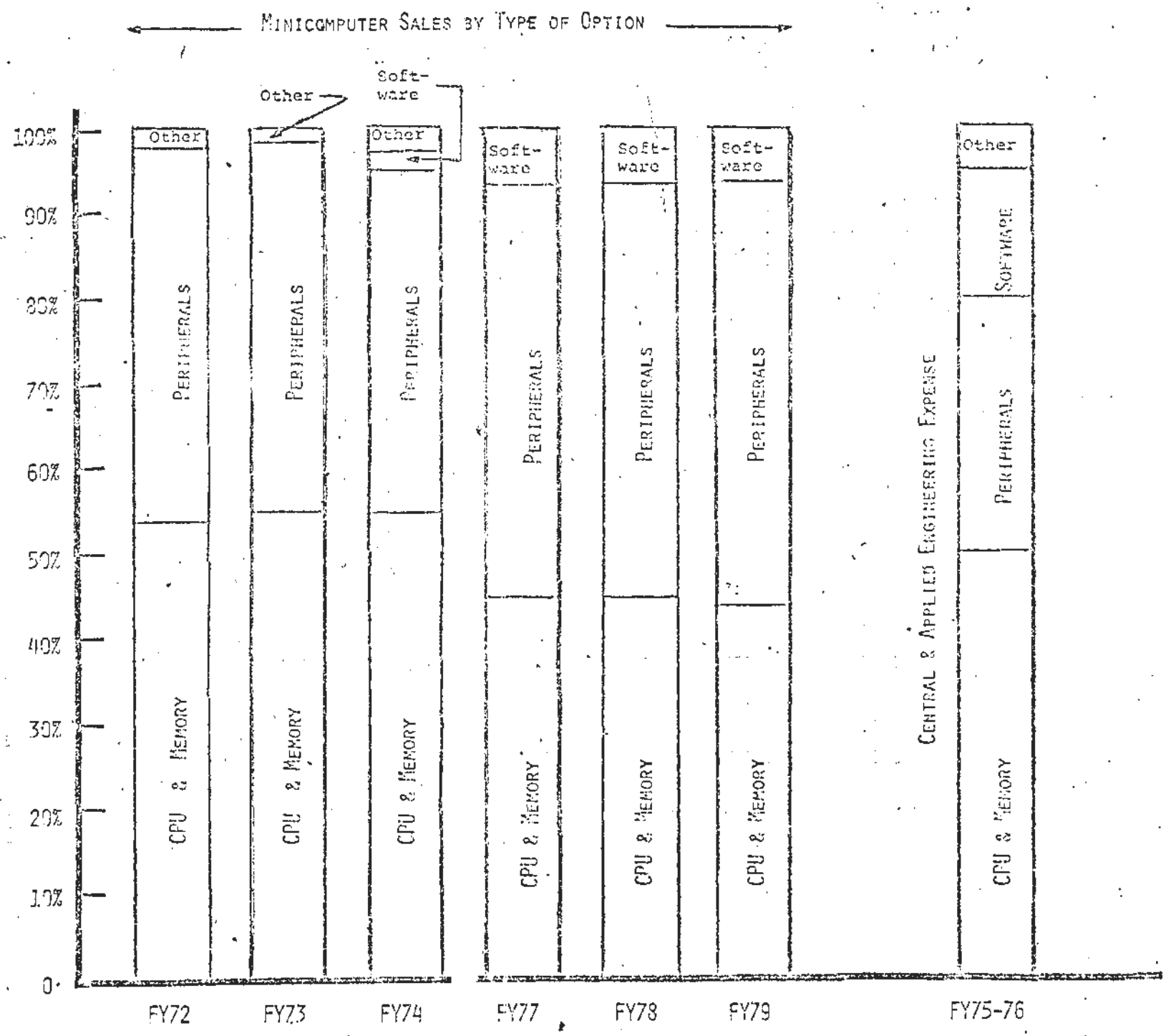
G.Bell
3/74

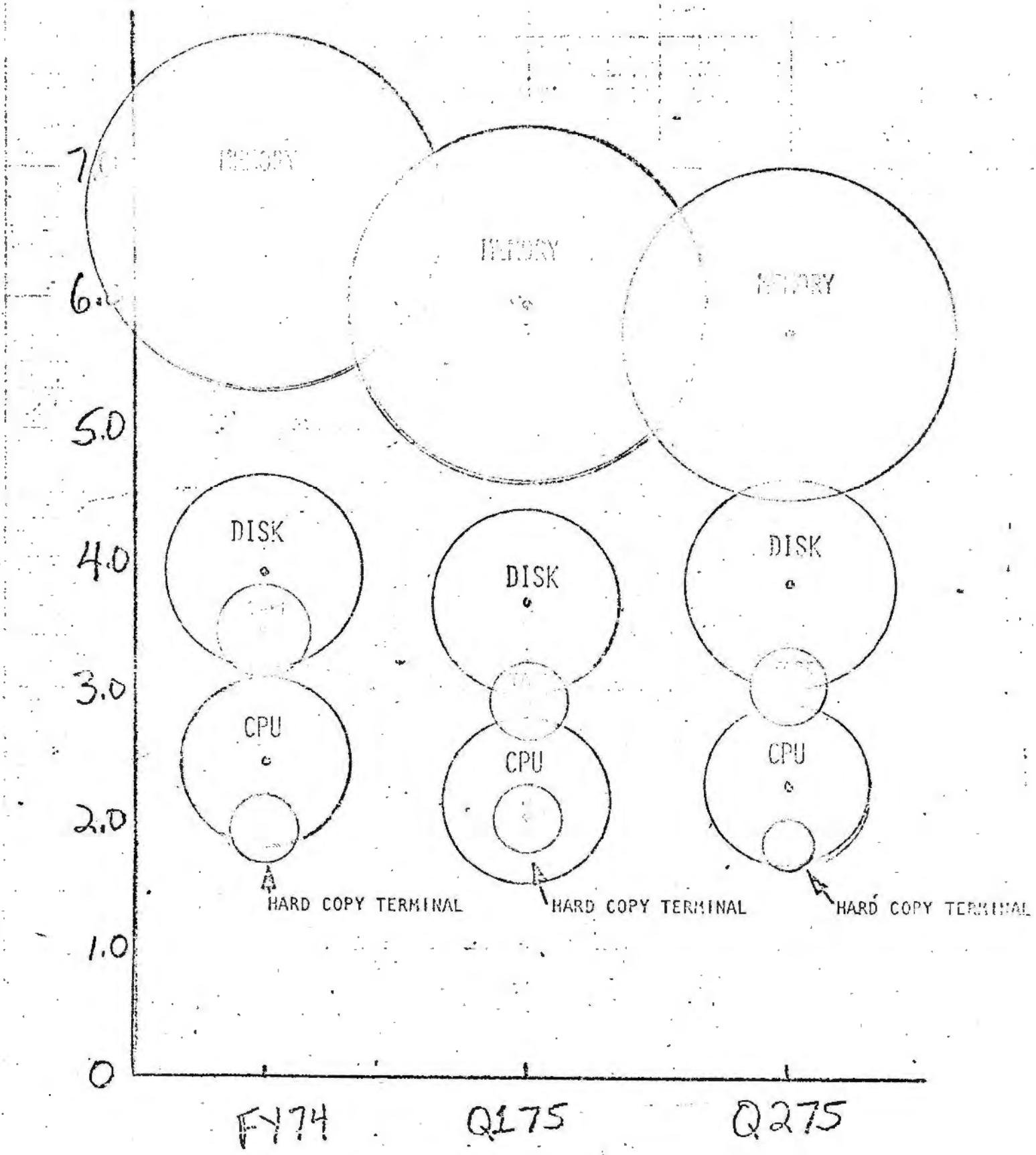
HOW ARE WE GOING TO DECREASE TECHNOLOGY (IBM) LEAD?

- NOVEL ORGANIZATION OF ELECTRONICS/SYSTEMS.
- COPY. HARD. WE'RE AWAY. BOTH LIMITED BY NATURAL LAWS.
- REDUCE DELAY TIMES - HARD DUE TO SEGMENTED CO.
- BUYOUT PEOPLE (ONLY FAST WAY)
  - END UP TRACKING PROBLEMS.
- BUYOUT PRODUCTS.
- FASTER DECISIONS.
- HIRE ADVANCED DEVELOPMENT PEOPLE - NOT DEVELOPMENT PEOPLE.



Phil Laut
9/30/75


MINICOMPUTER SALES BY TYPE OF OPTION
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0
Other
Soft-ware
CPU & MEMORY
PERIPHERALS
SOFTWARE
CENTRAL & APPLIED ENGINEERING EXPENSE
FY72
FY73
FY74
FY77
FY78
FY79
FY75-76



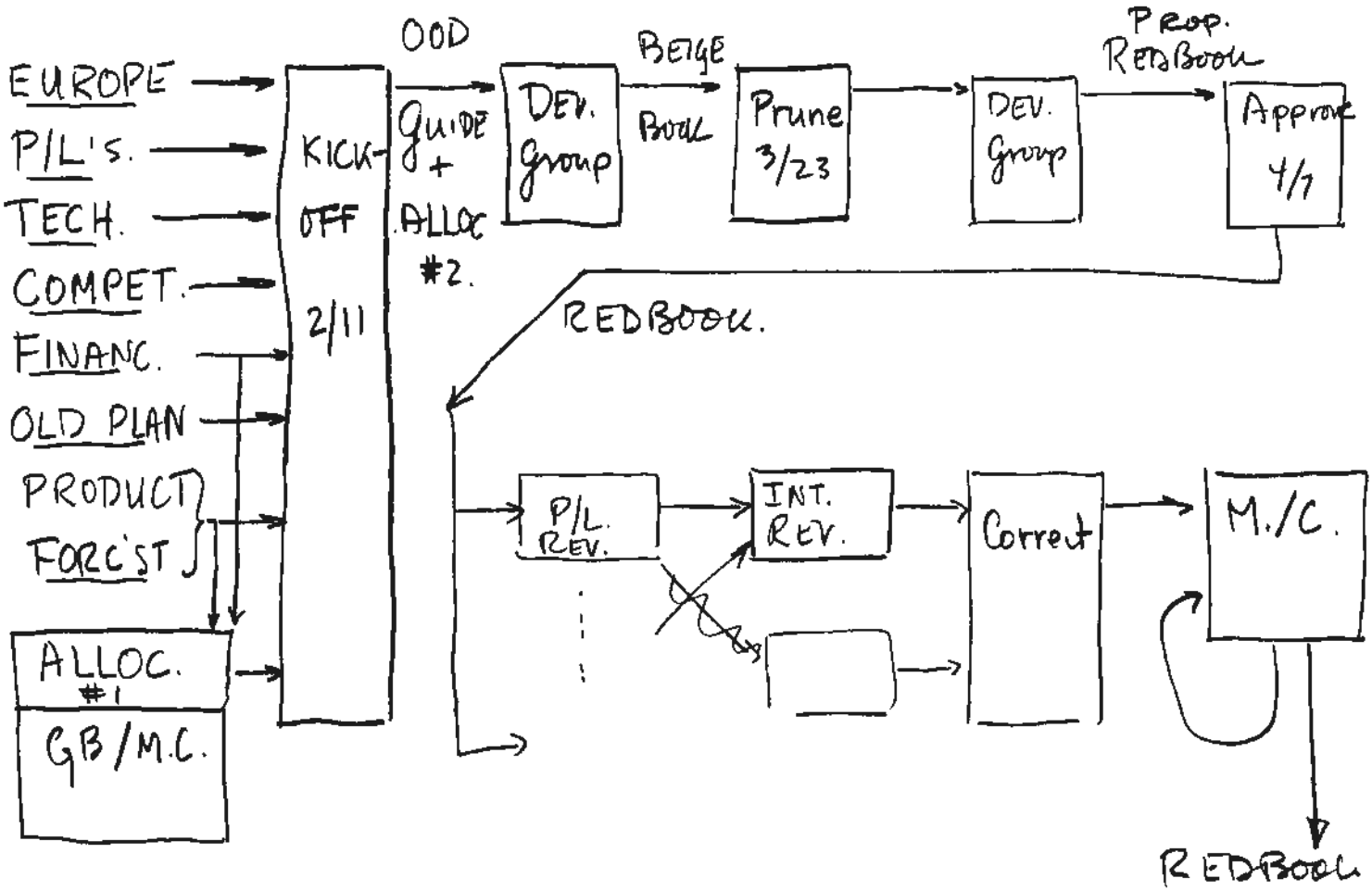
GROSS MARK UP & SALES ANALYSIS

Phil Laut
6/11/75

	Phase	Semi Annual Approval
0	PRE-PLAN	2p. Plan → OOD → PL/MC Info.
1	DESIGN	Φ1 Bus. Plan → PSG (Opinion) → OOD → PL/MC Info.
2	PROTO BLD/ DEBUG.	Φ2 Bus/Mfg. Plan → PSG (OPINION) → OOD (INFO) → M/E Appr. →
3	PROD. ST.-UP	PRICE PR. → PLM/MC Approve.
4	SUPPORT	· Prod. Mgr. Changes → OOD (INFO) → PLM/MC Approve

PRODUCT PLAN/Approval Process.

2/28/76.
SB.



8-QTR. ROLLING REDBOOK. PROCESS.

(EACH 2 QTR'S).

GB 2/28/76.

OOD (Cent. Eng.).

GB

- Pecuniary (PL), Place, Prod. K.
- Personnel (M.A.)
- LSI & Elect. Mems. (HL)
- Comm.
- Terminals, Disk, Tape, PS, Eng. Svc., CAB.
- HDW. Systems
- SOFTWARE
- 10 Eng.

FY. 77-78 STRATEGY ISSUES

- Increase Focus on Tech./Fut.
- Growth In Comm. Mkt.
- Customer Migration (Comp./Std)
  - Nets & mP
  - Systems Orientation
  - Disks
    - Low End.

digital

INTEROFFICE MEMORANDUM

TO: OOD
Staff

LOC/MAIL STOP

Slides for Europe

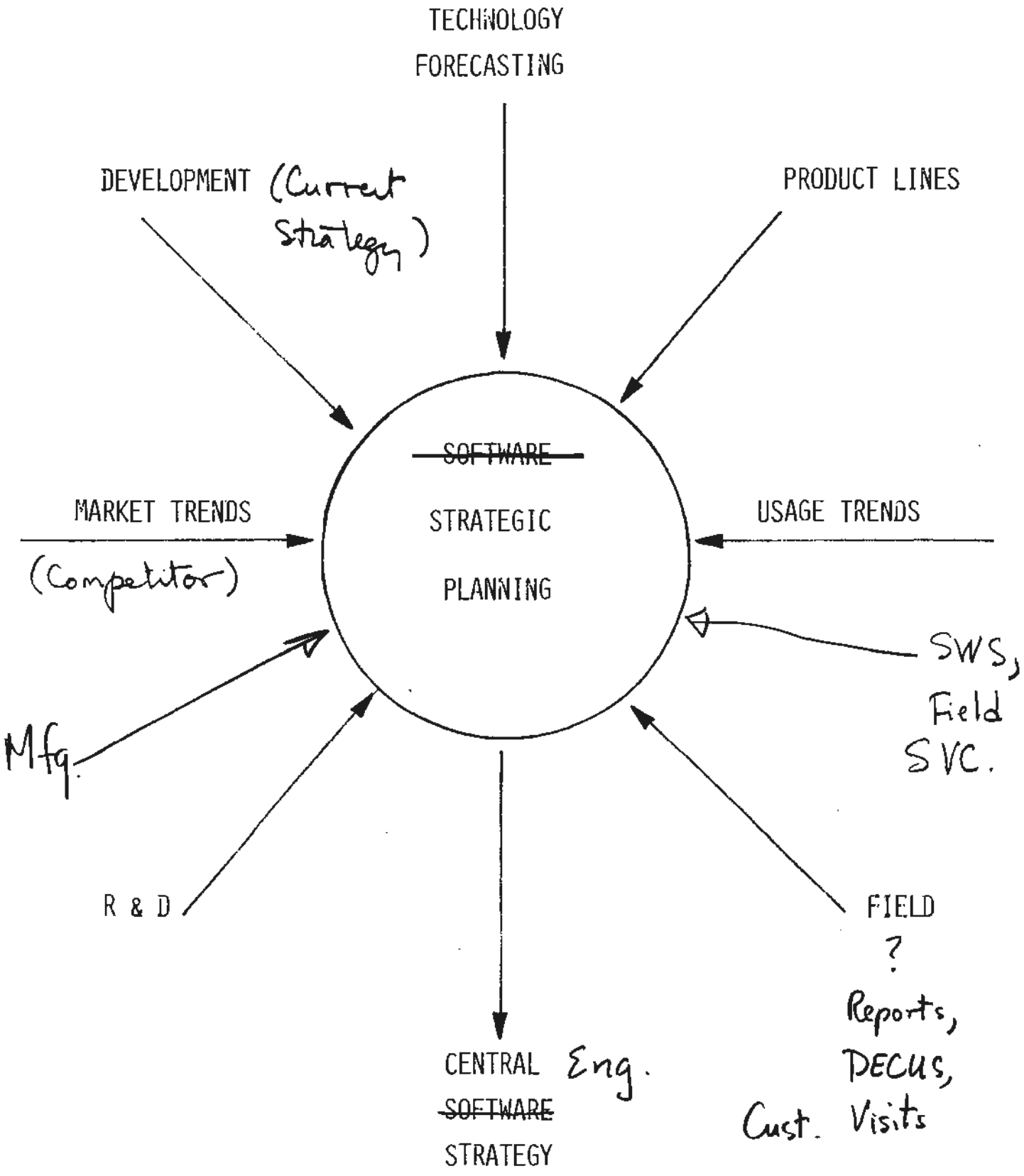
DATE: December 19, 1975
FROM: Larry Portner
DEPT:
EXT:
LOC/MAIL STOP:

SUBJ:

DEC 29 1975

The attached slides were used to address the North American District Software Services Managers in Atlanta last month. I thought you or your groups might like to see them.

gm
attachment


TECHNOLOGY
FORECASTING
DEVELOPMENT (Current Strategy)
PRODUCT LINES
~~SOFTWARE~~
STRATEGIC
PLANNING
MARKET TRENDS
(Competitor)
USAGE TRENDS
SWS, Field SVC.
Mfg.
R & D
FIELD
?
Reports, DECUS, Cust. Visits
CENTRAL Eng.
~~SOFTWARE~~
STRATEGY

SIGNIFICANT FACTORS IN OUR PLANNING

- RAPID GROWTH IN "COMMERCIAL" ORIENTATION OF OUR BUSINESS.

- SHIFT TO LESS TECHNICALLY SOPHISTICATED CUSTOMERS.

- TECHNOLOGY DRIVING DOWN COST FOR GIVEN LEVEL OF PERFORMANCE @ 30% YEAR.

- INCREASE IN PRODUCT FUNCTIONALITY, DECREASE IN CUSTOMER SOPHISTICATION MEANS DRAMATIC INCREASE IN PRODUCT COMPLEXITY.

- SHIFT TO SYSTEMS ORIENTATION - MORE FOCUS ON "TOTAL SYSTEM" PERFORMANCE, CAPABILITY.

- INFLATION DRIVES UP SUPPORT COSTS.

- MORE FOCUS ON APPLICATIONS ORIENTATION.

OUR PRIMARY FOCUS IN NEW SOFTWARE PRODUCT ENGINEERING IS ON

S U P P O R T A B I L I T Y

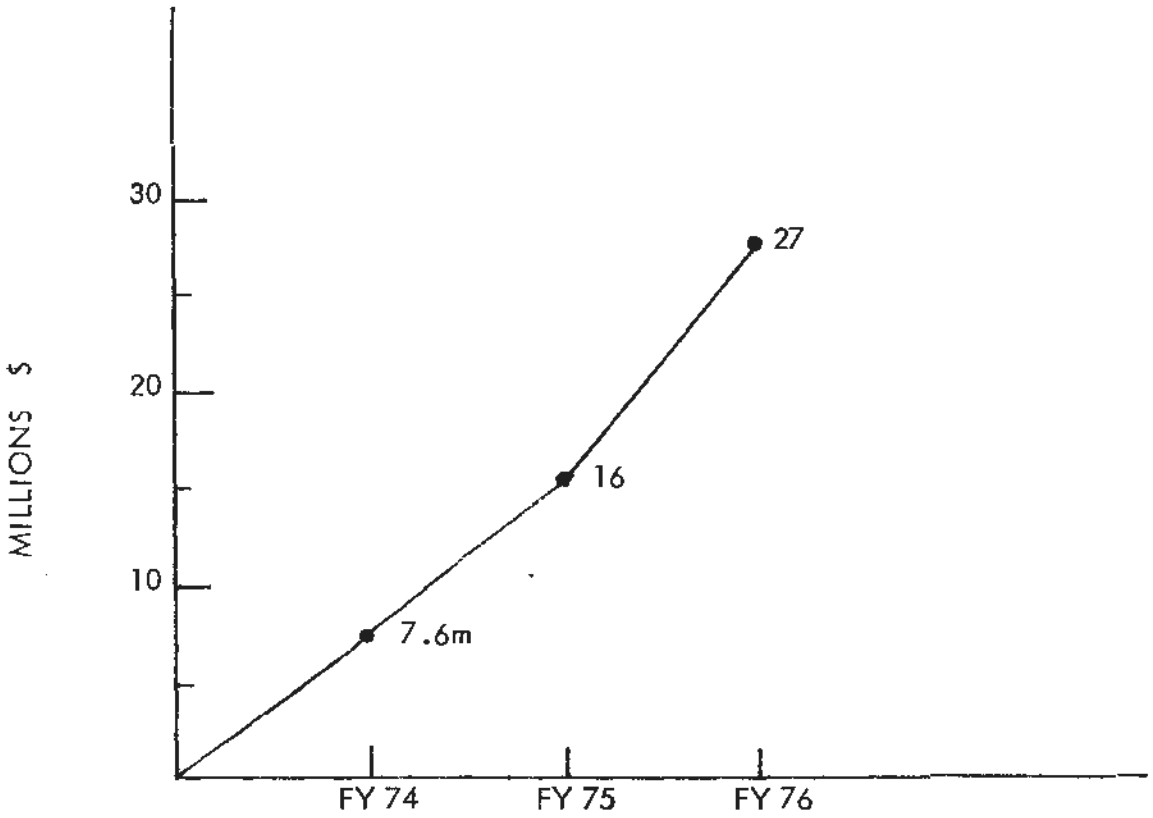
WE ARE DESIGNING FOR:

- EASE OF INSTALLATION
- EASY "PATCHING"
- ABILITY TO DO PARTIAL (COMPONENT) UPDATES
- FAULT TOLERANCE
- INCREASE WRITER-PROGRAMMER RATIO FROM 1-5 TO 1-3
- SIGNIFICANTLY INCREASED INVOLVEMENT OF SWS
    - MAINTENANCE PRODUCT MANAGEMENT
    - SUPPORTABILITY PLANNING ON NEW PRODUCTS
    - PHASE REVIEW SYSTEM
    - THE PRODUCT TEAM
        - PRODUCT MANAGER
        - PRODUCT SUPPORT MANAGER
        - SOFTWARE ENGINEERING MANAGER

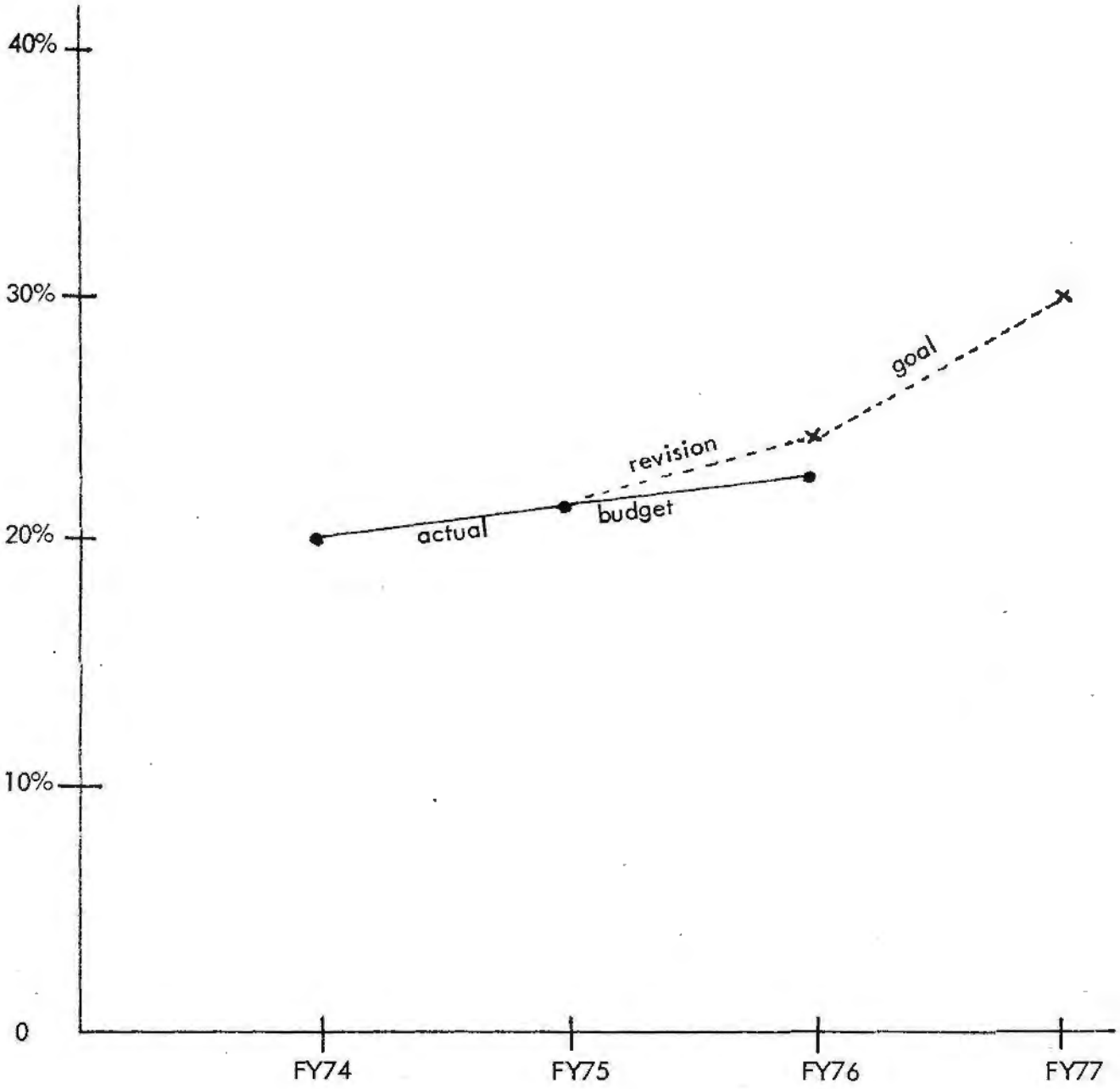
BUSINESS ISSUES

- SHOULD WE (CAN WE) MAKE A PROFIT ON SOFTWARE?
- ARE THE SELLING HASSLES BECAUSE SOFTWARE "HAS NO INTRINSIC VALUE" OR BECAUSE OUR POLICIES ARE POOR?
- ARE THE SELLING HASSLES INCREASING, OR MODERATING?
- DOES SELLING SOFTWARE PUT US AT A COMPETITIVE DISADVANTAGE?
- COULD WE SELL MORE PRODUCTS OVERALL IF WE BUNDLED SOFTWARE BACK IN?
- HOW IS OUR SOFTWARE IMAGE WHEN WE APPROACH NEW CUSTOMERS? DOES IT HELP US OR HURT US?

SOFTWARE LICENSE REVENUE



SOFTWARE SPENDING AS A % OF TOTAL ENGINEERING



CHANGES OVER THE PAST YEAR

1. ADDED AN ADVANCED DEVELOPMENT GROUP TO THE RESEARCH GROUP.

2. FULL-TIME STANDARDS ACTIVITY.

3. DEVELOPMENT METHODS GROUP.

4. APPLICATIONS GROUP.

5. FULL-TIME MANAGER FOR MAINTENANCE.

6. PRODUCT MANAGEMENT GROUP.

7. SOFTWARE QUALITY MANAGEMENT FUNCTION.

8. R.A.S. PROGRAM

- USER ENVIRONMENT TEST PROGRAMS
- DIAGNOSTIC PROGRAM GENERATION
- ON-LINE DIAGNOSTICS UNDER MAJOR OPERATING SYSTEMS
- ERROR LOGGING

9. ACTIVE PDP-10/PDP-11 DIALOGUE ON LANGUAGE COMPATIBILITY, COMMAND LANGUAGES.

10. FOCUS ON THE DEVELOPMENT PROCESS FOR BUILDING COMPLEX PRODUCTS.

11. "KEY ~~MAN~~ Person" HIRING PROGRAM; "HIRE ONLY THE BEST".

12. SOFTWARE FAMILY STRATEGIES AND PLANS.

KEY ELEMENTS OF OUR SOFTWARE STRATEGY

- A Leadership Product Set in Every Major DEC Market
- Retain Leadership in Time-Sharing and Interactive Computing
- Provide the Customer Clear Easy Growth Opportunities (the "FAMILY" Concept)
    - Across Mainframes
    - Within the Software Families
- Exploit DEC's Rich Product Set Thru Networks
- Increased Commercial Orientation
    - RAS
    - Human Engineering
    - Documentation
    - File Systems
    - Coordinated Utilities
    - Terminal Support
- Increased Applications Orientation - Reduce the Customer's Cost for Developing his Applications.

MAJOR NEW PRODUCTS

IAS

BASIC+II

FMS-11

DBMS-11

TPM-11

RSTS/FORTRAN IV

COBOL UPGRADE

RSTS/E V6B

NETWORKS

- Interprocessor Link
- Terminal Support
- Better IBM Support Via FE

FRONT END

- Work with RSTS, RSX, IAS, DEC-10, DEC-20
- Vehicle for Most Sophisticated Communications Support in Big Systems in Future

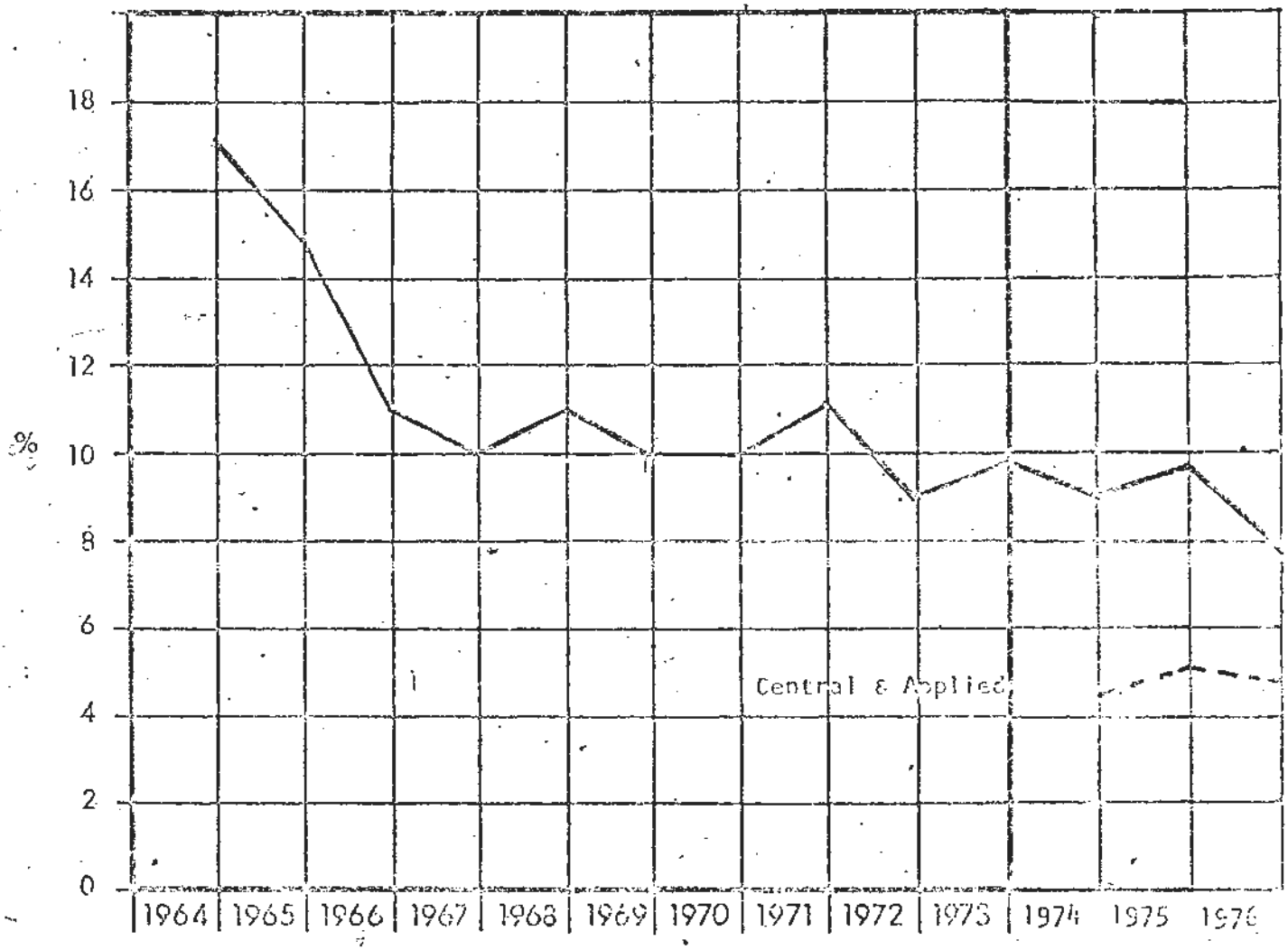
RT-11 UPGRADE

APL

- RSTS/E
- RT-11

MESSAGES

- DON'T LET US DO DUMB THINGS!
- A SIGNIFICANT PORTION OF SDC PROBLEMS START WITH BAD ORDERS.
- THE MONTHLY REPORTS ARE WORTH THEIR WEIGHT IN DIAMONDS, DON'T LET THEM STOP.
- CONTINUE TO EDUCATE THE SALESFORCE ON SOFTWARE; IN FIVE YEARS IT MAY BE WHERE MOST OF OUR PROFIT COMES FROM.
- RECOGNIZE NEW PRODUCT OPPORTUNITIES AND FEED THEM BACK!
- INVITE US (THE DEVELOPERS, THE PRODUCT MANAGERS) TO YOUR MEETINGS; WE NEED TO DEVELOP A BETTER UNDERSTANDING OF HOW OUR PRODUCTS RELATE TO SELLING, SUPPORT AND CUSTOMERS.

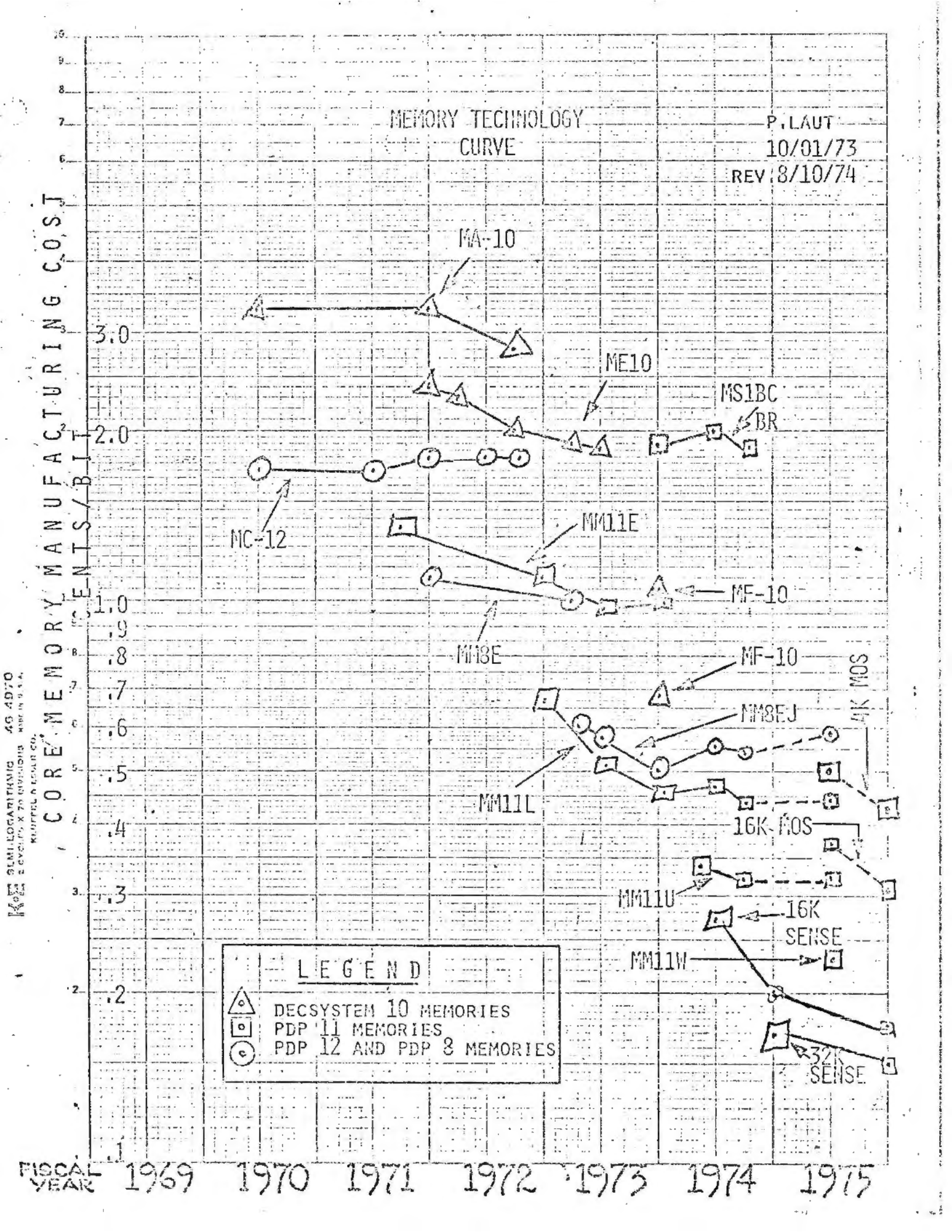


RESEARCH & ENGINEERING AS A % OF NET SALES

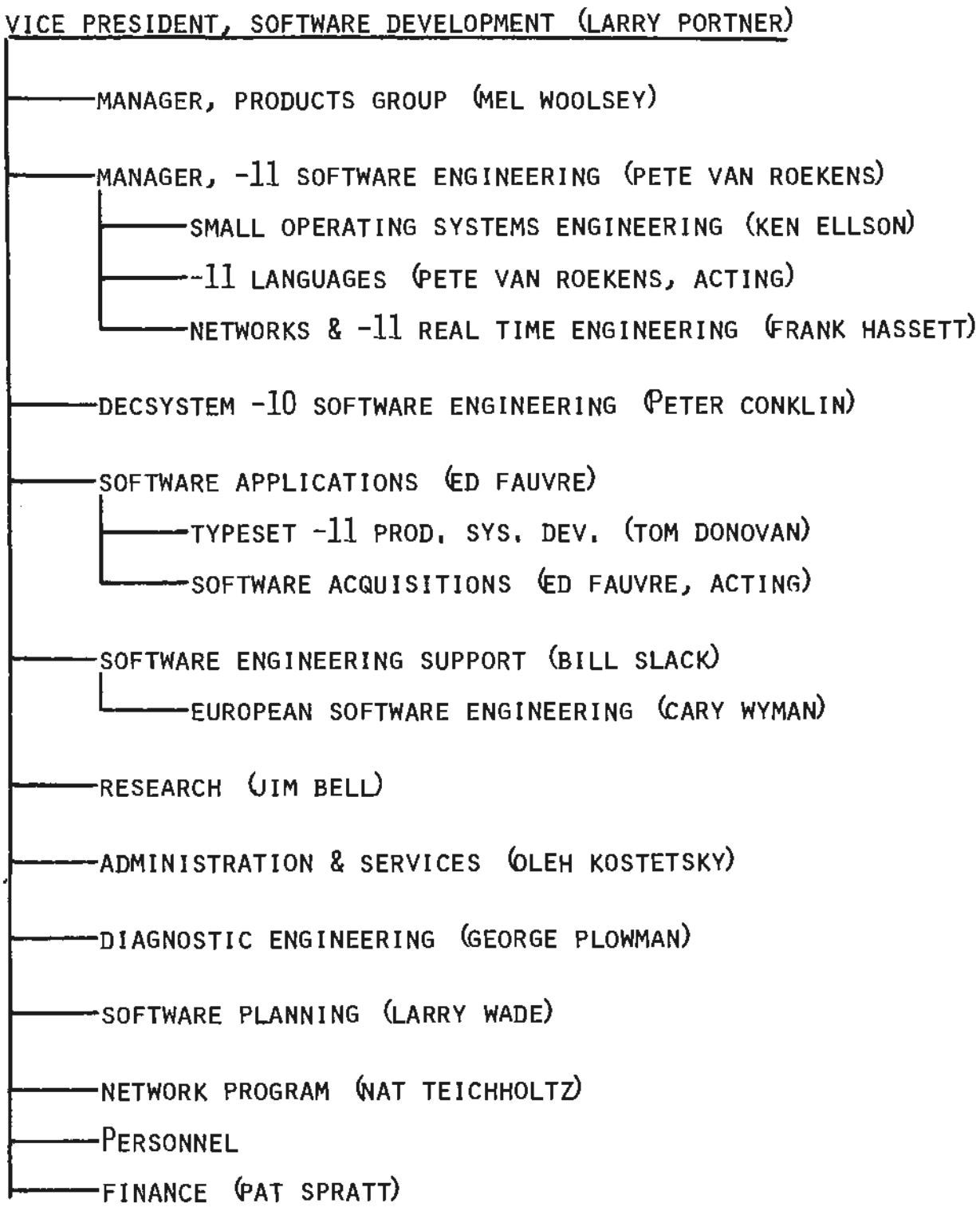
Figure 1

Phil Laut
8/13/73
8/10/74
3/25/75

10/72 KHO-SI [illegible] 2

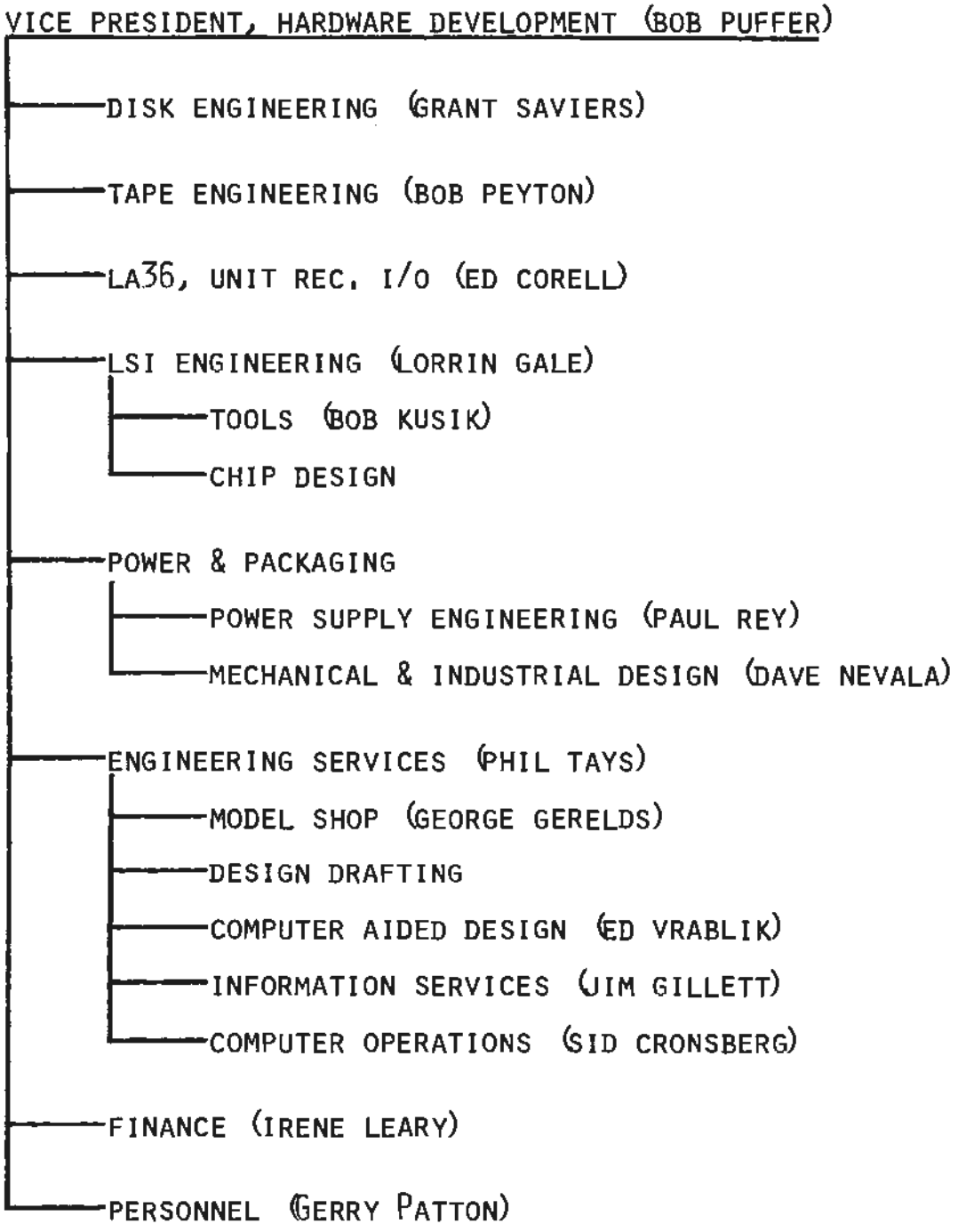

MEMORY TECHNOLOGY CURVE
P. LAUT
10/01/73
REV 8/10/74
CORE MEMORY MANUFACTURING COST
CENTS/BIT
MA-10
ME10
MS1BC
BR
MC-12
MM11E
MF-10
MM8E
MF-10
MM8EJ
4K MOS
MM11L
16K MOS
MM11U
16K
SENSE
MM11W
32K
SENSE
LEGEND
DECSYSTEM 10 MEMORIES
PDP 11 MEMORIES
PDP 12 AND PDP 8 MEMORIES
FISCAL YEAR
1969
1970
1971
1972
1973
1974
1975

SOFTWARE DEVELOPMENT



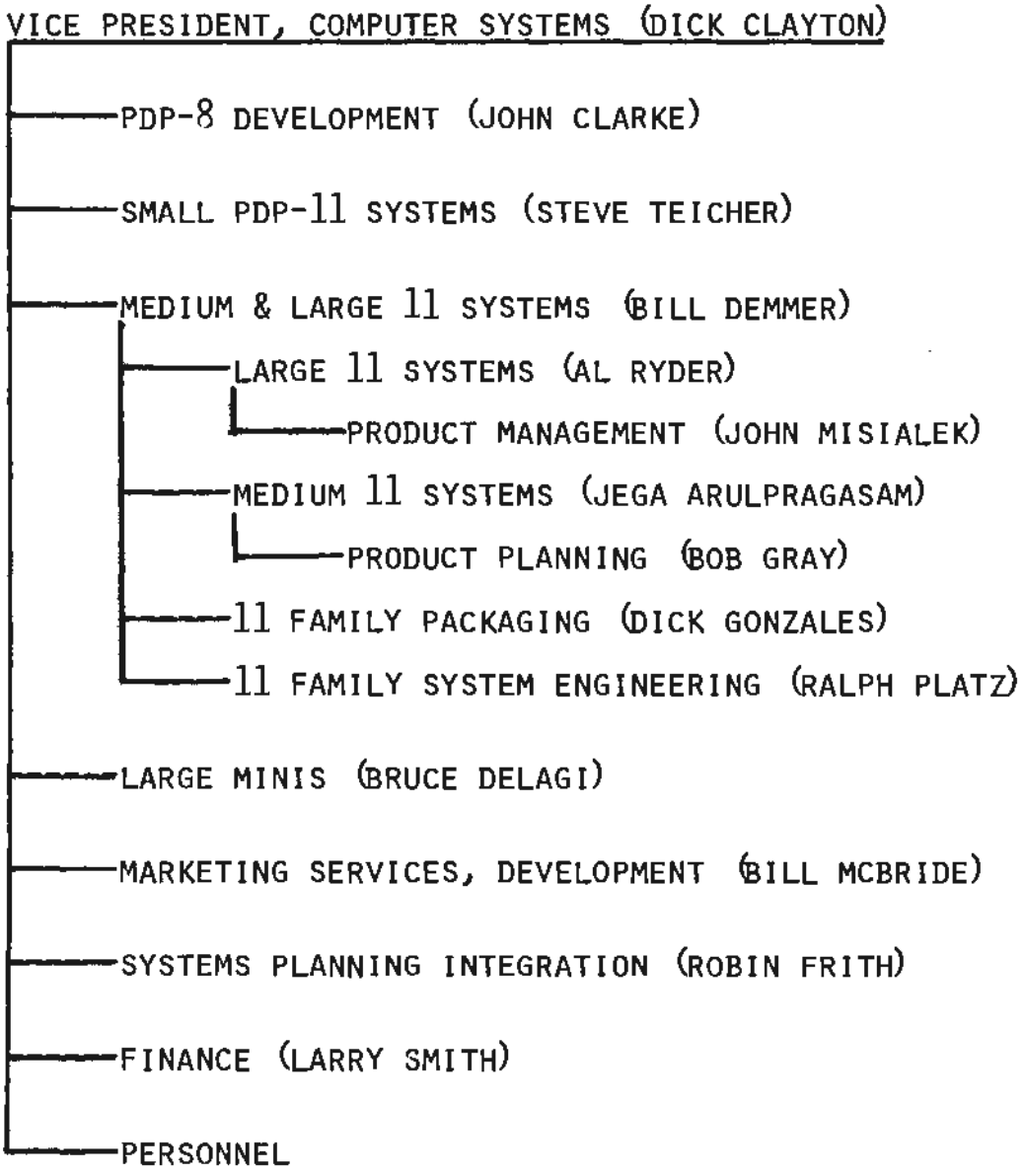
7/74
GB

HARDWARE DEVELOPMENT



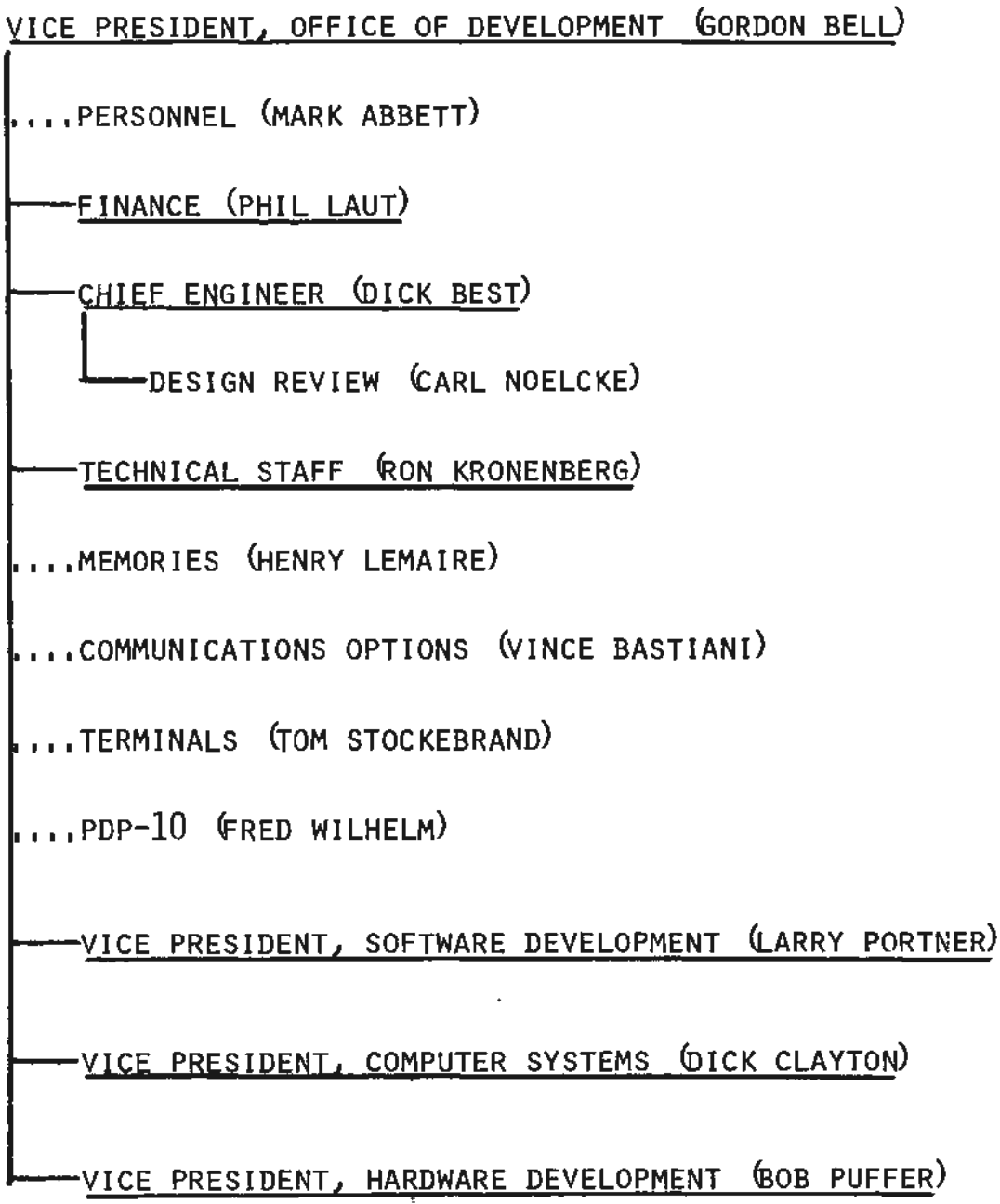
7/74
GB

COMPUTER SYSTEMS

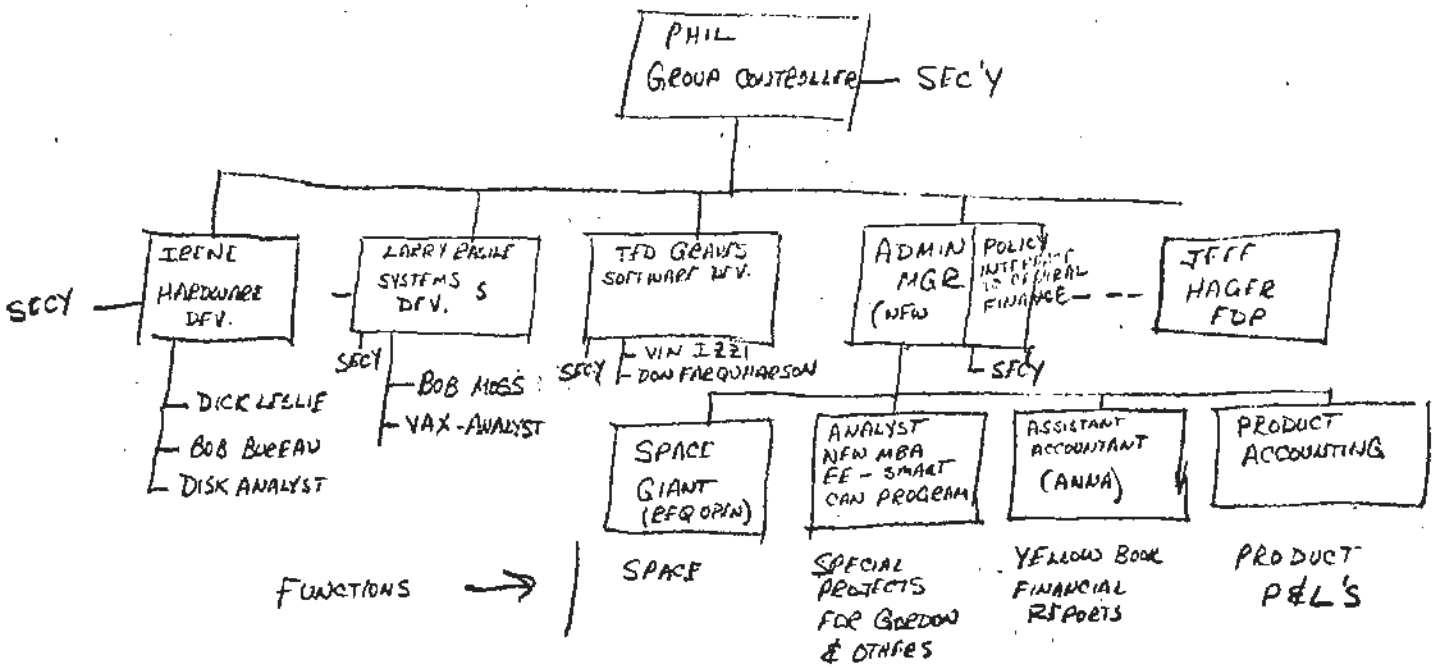


7/74
GB

OFFICE OF DEVELOPMENT



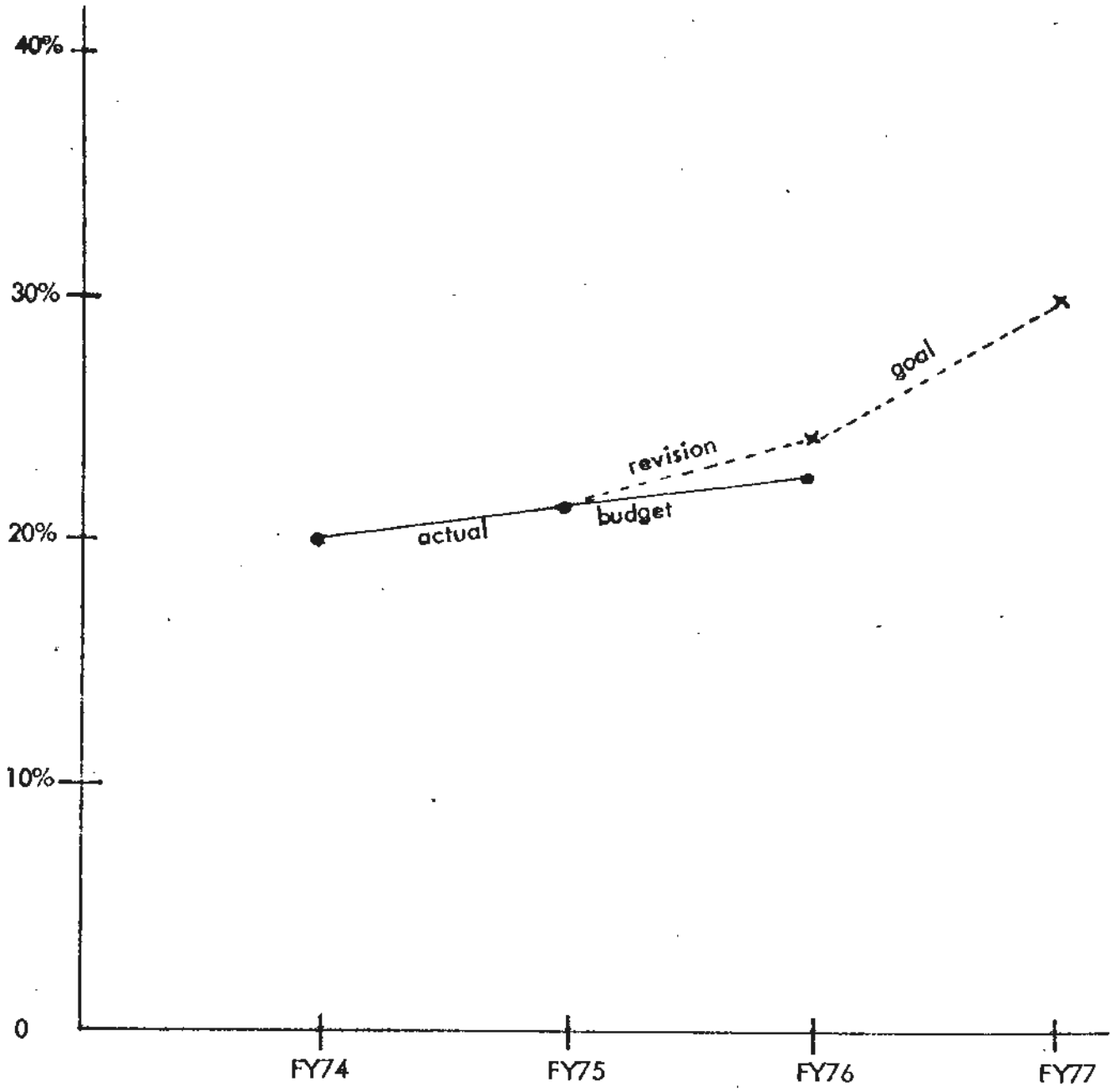
7/74
GB


PHIL
GROUP CONTROLLER
SEC'Y
IRENE
HARDWARE DEV.
SECY
DICK LESLIE
BOB BUREAU
DISK ANALYST
LARRY PAULL
SYSTEMS S DEV.
SECY
BOB MOSS
VAX-ANALYST
TED GEARS
SOFTWARE DEV.
SECY
VIN IZZI
DON FARQUHARSON
ADMIN MGR.
(NEW
POLICY
SECY
JEFF
HAGER
FOR
SPACE
GIANT
(EEQ OPN)
ANALYST
NEW MBA
EE - SMART
CAN PROGRAM
ASSISTANT
ACCOUNTANT
(ANNA)
PRODUCT
ACCOUNTING
FUNCTIONS
SPACE
SPECIAL
PROJECTS
FOR GORDON
& OTHERS
YELLOW BOOK
FINANCIAL
REPORTS
PRODUCT
P&L'S

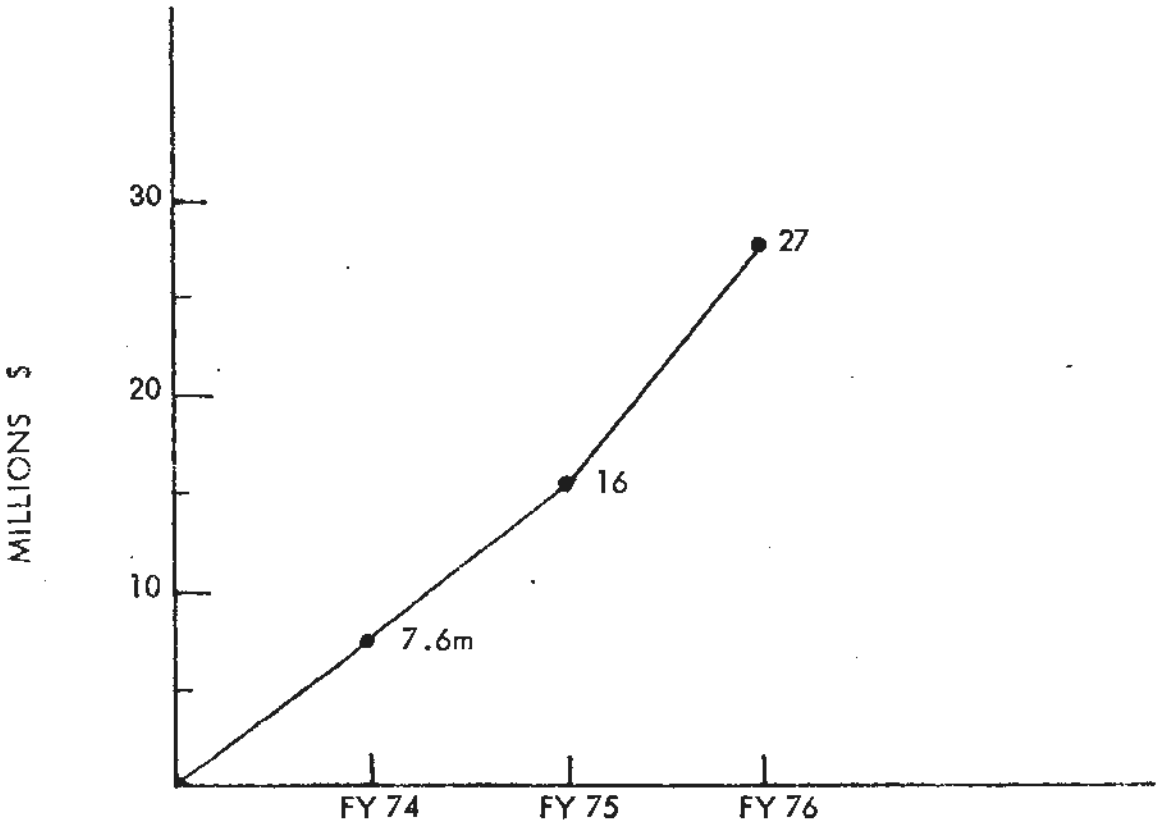
MESSAGES

- DON'T LET US DO DUMB THINGS!
- A SIGNIFICANT PORTION OF SDC PROBLEMS START WITH BAD ORDERS.
- THE MONTHLY REPORTS ARE WORTH THEIR WEIGHT IN DIAMONDS, DON'T LET THEM STOP.
- CONTINUE TO EDUCATE THE SALESFORCE ON SOFTWARE; IN FIVE YEARS IT MAY BE WHERE MOST OF OUR PROFIT COMES FROM.
- RECOGNIZE NEW PRODUCT OPPORTUNITIES AND FEED THEM BACK!
- INVITE US (THE DEVELOPERS, THE PRODUCT MANAGERS) TO YOUR MEETINGS; WE NEED TO DEVELOP A BETTER UNDERSTANDING OF HOW OUR PRODUCTS RELATE TO SELLING, SUPPORT AND CUSTOMERS.

SOFTWARE SPENDING AS A % OF TOTAL ENGINEERING



SOFTWARE LICENSE REVENUE



OUR PRIMARY FOCUS IN NEW SOFTWARE PRODUCT ENGINEERING IS ON

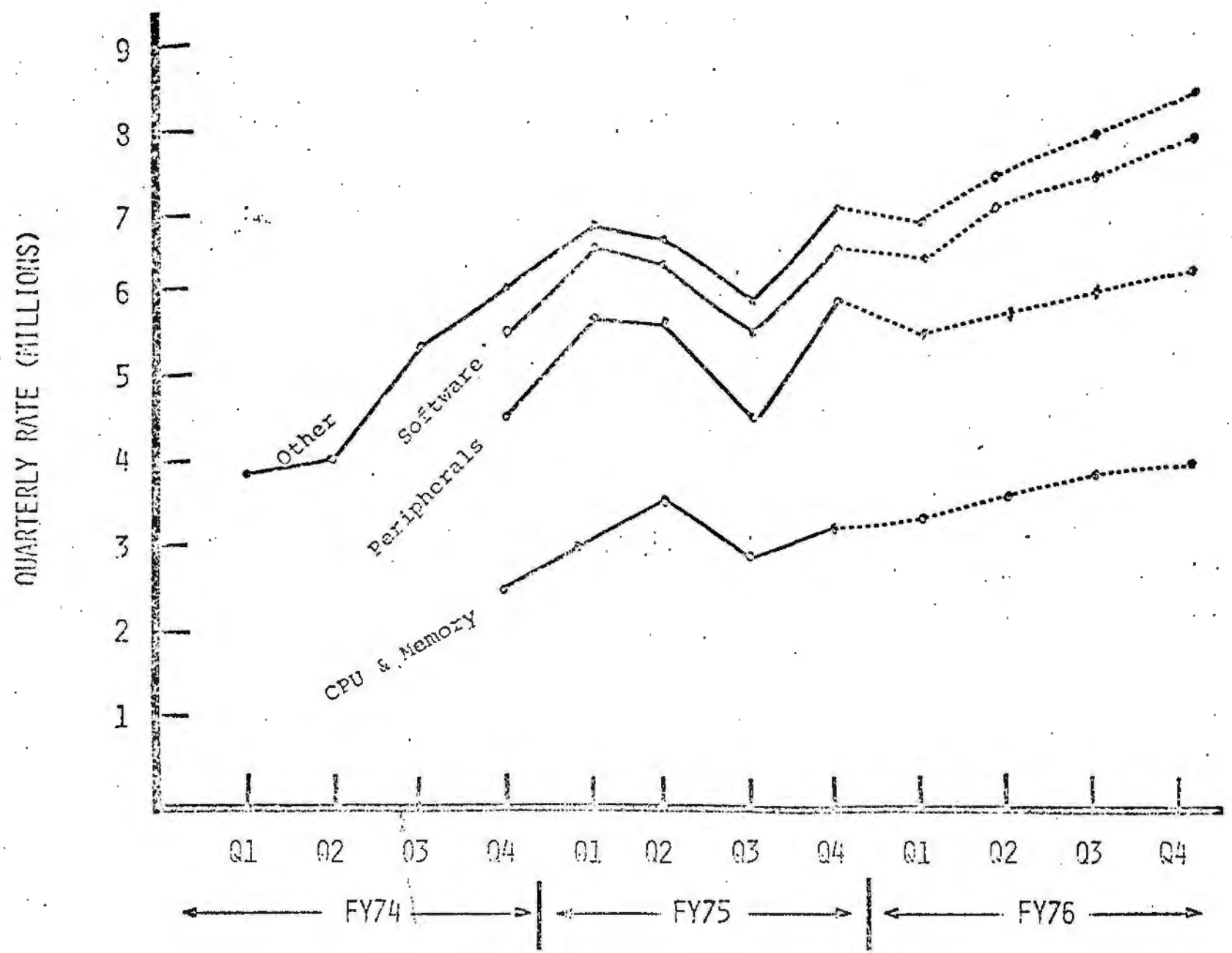
S U P P O R T A B I L I T Y

WE ARE DESIGNING FOR:

- EASE OF INSTALLATION
- EASY "PATCHING"
- ABILITY TO DO PARTIAL (COMPONENT) UPDATES
- FAULT TOLERANCE
- INCREASE WRITER-PROGRAMMER RATIO FROM 1-5 TO 1-3
- SIGNIFICANTLY INCREASED INVOLVEMENT OF SWS
    - MAINTENANCE PRODUCT MANAGEMENT
    - SUPPORTABILITY PLANNING ON NEW PRODUCTS
    - PHASE REVIEW SYSTEM
    - THE PRODUCT TEAM
        - PRODUCT MANAGER
          PRODUCT SUPPORT MANAGER
          SOFTWARE ENGINEERING MANAGER

BUSINESS ISSUES

- SHOULD WE (CAN WE) MAKE A PROFIT ON SOFTWARE?
- ARE THE SELLING HASSLES BECAUSE SOFTWARE "HAS NO INTRINSIC VALUE" OR BECAUSE OUR POLICIES ARE POOR?
- ARE THE SELLING HASSLES INCREASING, OR MODERATING?
- DOES SELLING SOFTWARE PUT US AT A COMPETITIVE DISADVANTAGE?
- COULD WE SELL MORE PRODUCTS OVERALL IF WE BUNDLED SOFTWARE BACK IN?
- HOW IS OUR SOFTWARE IMAGE WHEN WE APPROACH NEW CUSTOMERS? DOES IT HELP US OR HURT US?



Phil Laut
9/30/75

FY. 77-78 STRATEGY ISSUES

- Increase Focus on Tech./Fut.
- Growth In Comm. Mkt.
- Customer Migration (Comp./Std)
  - Nets & mP
  - Systems Orientation
  - Disks
    - Low End.

SIGNIFICANT FACTORS IN OUR PLANNING

- RAPID GROWTH IN "COMMERCIAL" ORIENTATION OF OUR BUSINESS.

- SHIFT TO LESS TECHNICALLY SOPHISTICATED CUSTOMERS.

- TECHNOLOGY DRIVING DOWN COST FOR GIVEN LEVEL OF PERFORMANCE @ 30% YEAR.

- INCREASE IN PRODUCT FUNCTIONALITY, DECREASE IN CUSTOMER SOPHISTICATION MEANS DRAMATIC INCREASE IN PRODUCT COMPLEXITY.

- SHIFT TO SYSTEMS ORIENTATION - MORE FOCUS ON "TOTAL SYSTEM" PERFORMANCE, CAPABILITY.

- INFLATION DRIVES UP SUPPORT COSTS.

- MORE FOCUS ON APPLICATIONS ORIENTATION.

KEY ELEMENTS OF OUR SOFTWARE STRATEGY

- A Leadership Product Set in Every Major DEC Market
- Retain Leadership in Time-Sharing and Interactive Computing
- Provide the Customer Clear Easy Growth Opportunities (the "FAMILY" Concept)
    - Across Mainframes
    - Within the Software Families
- Exploit DEC's Rich Product Set Thru Networks
- Increased Commercial Orientation
    - RAS
    - Human Engineering
    - Documentation
    - File Systems
    - Coordinated Utilities
    - Terminal Support
- Increased Applications Orientation - Reduce the Customer's Cost for Developing his Applications.

CHANGES OVER THE PAST YEAR

1. ADDED AN ADVANCED DEVELOPMENT GROUP TO THE RESEARCH GROUP.

2. FULL-TIME STANDARDS ACTIVITY.

3. DEVELOPMENT METHODS GROUP.

4. APPLICATIONS GROUP.

5. FULL-TIME MANAGER FOR MAINTENANCE.

6. PRODUCT MANAGEMENT GROUP.

7. SOFTWARE QUALITY MANAGEMENT FUNCTION.

8. R.A.S. PROGRAM

- USER ENVIRONMENT TEST PROGRAMS.
- DIAGNOSTIC PROGRAM GENERATION
- ON-LINE DIAGNOSTICS UNDER MAJOR OPERATING SYSTEMS
- ERROR LOGGING

9. ACTIVE PDP-10/PDP-11 DIALOGUE ON LANGUAGE COMPATIBILITY, COMMAND LANGUAGES.

10. FOCUS ON THE DEVELOPMENT PROCESS FOR BUILDING COMPLEX PRODUCTS.

11. "KEY ~~MAN~~ Person" HIRING PROGRAM; "HIRE ONLY THE BEST".

12. SOFTWARE FAMILY STRATEGIES AND PLANS.

MAJOR NEW PRODUCTS

IAS

BASIC+II

FMS-11

DBMS-11

TPM-11

RSTS/FORTRAN IV

COBOL UPGRADE

RSTS/E V6B

NETWORKS

- Interprocessor Link
- Terminal Support
- Better IBM Support Via FE

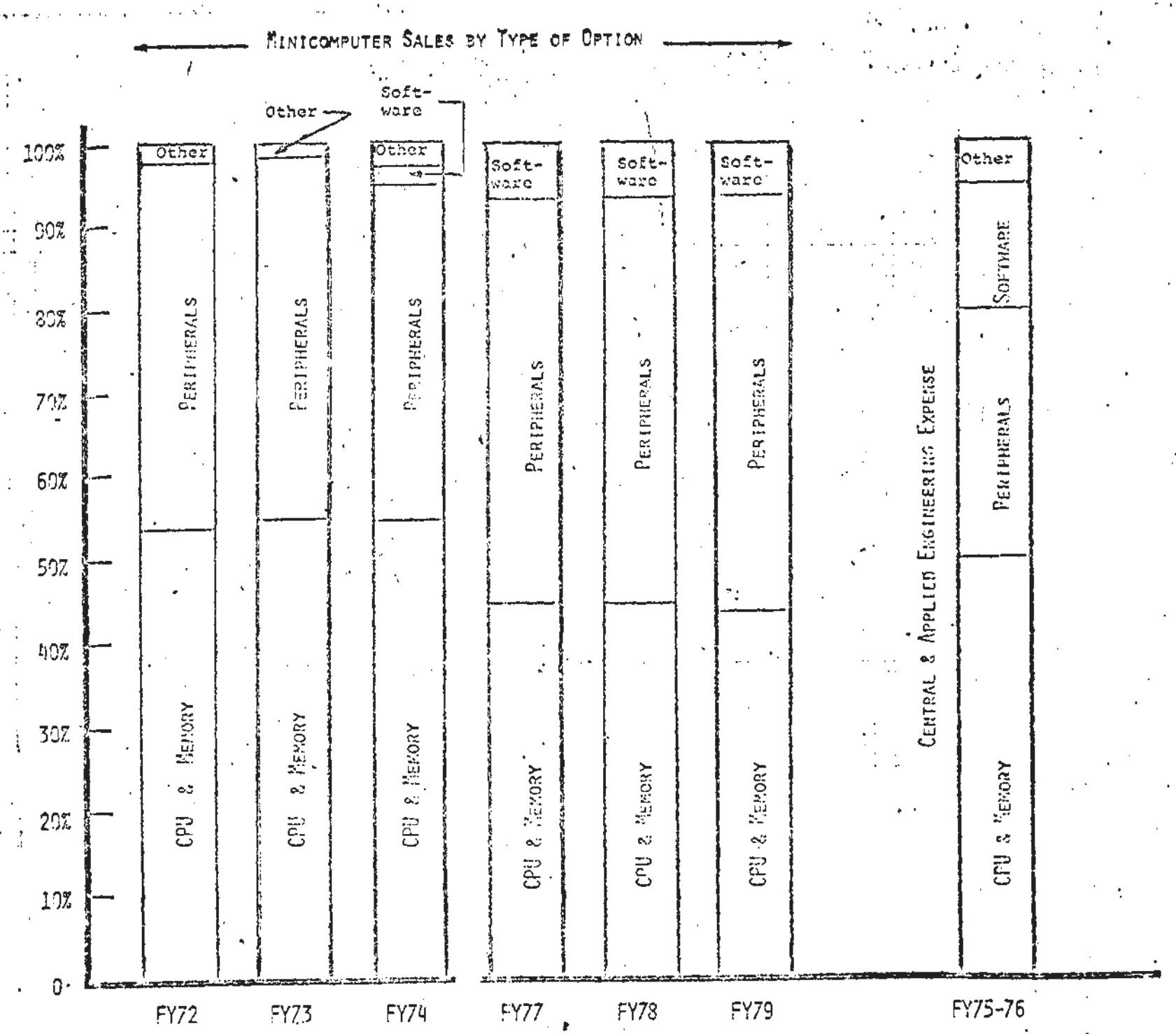
FRONT END

- Work with RSTS, RSX, IAS, DEC-10, DEC-20
- Vehicle for Most Sophisticated Communications Support in Big Systems in Future

RT-11 UPGRADE

APL

- RSTS/E
- RT-11



INDUSTRY TRENDS IN COMPUTER TECHNOLOGY

1. Business trends: Five Year Forecast

   Computers much cheaper
   Easier to use
   Personal computers common
   Reliability dramatically better
   Software, service income

2. Technological developments

   Microprocessors
   Memory prices
   Mass storage
   Floppy disks
   Optical technology

3. Architecture trends

   Storage hierarchy
   Address spaces
   Multiprocessing

4. Operating systems trend

   Why OS at all?
   Kernel approach
   Modularity
   Human interface

5. Compiler and language trends

   Why languages survive
   Multiple level interpreters
   Compiling microcode
   Language trends

Jim Bell
1 December 1975

BUSINESS TRENDS: Five Year Forecast

Computers will be much cheaper: Equivalents of today's machines will cost 2/3 less

- Price; performance
- New applications; sophistication
- Substituting information for energy, for mechanics

Computers will be easier to use

- Manufacturer supplied software will be bigger and have more function
- Memories will be bigger: 64K bit RAM chips, 256K ROM, bubbles
- Languages will be ultra-high level, often specialized, more redundant, better human engineered
- Non-standard IO (graphics, speech, transducers) will be quite common
- Non-numeric and semi-numeric applications will predominate: POS, EFTS, office, factory, $40B government paperwork
- Virtual, transparent facilities; even over nets

Personal computers will be common

- Data capture, hand held, desk top, also maxis
- New distribution methods
- Portable partly because of power supply costs
- Why personals: privacy, protection, comm costs
- Not all personal: distributed data bases and programs

Software and hardware reliability will be dramatically better

- Implies ease of use-- cf. calculator failure rates
- Software and hardware redundancy
- Service free? Remote diagnosis, self diagnosis, user service, deferable service
- More self-testing of software
- Availability not reliability (cf. telephone system)

Software and service income will be increasingly important

- Value added: hardware vs. software, micros, our expertise
- Functional pricing: IBM, per line compiled, transaction, rental/service environment
- Maximizing income via software pricing: hardware families, breadth of user base. Functional?
- Sales vs. service revenues as function of growth rate

TECHNOLOGICAL DEVELOPMENTS

Microprocessors

- Really here
- Stand-alone
- Distributed intelligence
- Many cooperating

Memory prices

- 4K
- 16K
- LARAM
- CCD
- Bubbles
- Screen-door
- Last gasp theory
- Computers (i.e. software) will have more function

Mass storage

- Ultra-large 3 or 4 yrs. off says CDC
- Cheaper, more capacity
- Archival storage
- Distributed data bases

Floppy disks

- Real costs--peripherals next focus
- Random access--systems device
- Capacity
- Cost

ARCHITECTURE

Storage hierarchy

- Locality, working set, statistical
- Cache accepted
- Paging coming for minis (Prime)
- Disks/drums/tape
- Saltzer model; Strecker program
- Honeycomb memory (IBM)

Address spaces

- Large physical--but less still cheaper
- Larger virtual
- Segmentation, paging--understood
- Mapping, protection--still tough

Multiprocessing

- Front-ends
- Controllers
- Vector--ganged lawnmower, languages
- I boxes sharing E box (IBM)
- Multi-streaming
- Symmetric multiprocessing
- Thruput & Availability

Optical technology

- Memories
- Busing
- Optical readers, matrix readers

OPERATING SYSTEMS

Why OS at all?

- Multiplexing vs. function
- Former invisible--less future need?
- Stand-alone (Hansen)

Kernel approach

- Large OS, small resident kernel
- Only kernel involute
- Universal kernel possible?

Modularity

- Sharable--e.g., device drivers
- How broken up matters
- Logical versus physical, decoupling

Human interface

- Smart terminals--line scanning, editing
- Language, graphics (prompting factor of 4)
- Unsophisticated users predominate
- Speech IO, training by doing
- Transparency--virtual memory, processors, network

COMPILER AND LANGUAGE

Why languages survive

- FORTRAN, COBOL--inertia
- BASIC--momentum, many students
- PL/I--sponsorship
- APL--aggregates
- PASCAL--fits current theories

Multiple level interpreters

- BASIC
- How many levels
- Which levels (Burroughs, SAAB/Univac)

Compiling microcode

- PL/M (Intel)
- Optimizing (parallelism, timings)

Language trends

- Ultra-high level, more layers on onion
- Special purpose--including systems
- Control structures are key
- Data: separate physical vs. logical structures

GENERAL GROWTH TRENDS AND ORGANIZATION SOLUTIONS

1. LOWER LEVEL OF INTEGRATION $\Rightarrow$ LSI FOR COST

   $\Rightarrow$ LSI FOR PERFORMANCE

2. HIGHER LEVEL OF INTEGRATION $\Rightarrow$ APPLICATIONS

3. MORE (CLEAR) CHARTER SEGMENTATION (I.E. IN FACTORY/ MARKET/PRODUCT) $\Rightarrow$ BETTER CENTRALIZED

   PLAN, ROLL-UP, CLEAR STANDARDS, GOALS, AND PLAN TESTING/TRACKING $\Rightarrow$ STAFF AND TOOLS!

4. MANUFACTURING $\Rightarrow$ FOCUSED VERSUS DEFOCUSED FACTORY?

GB
11/6/75

DEC-EXTERNAL-GROUP INTERFACES

1. TECHNOLOGY ⇒ GENERALLY ORGANIZE TO "MONITOR AND BUY"
   (AD HOC NOW)

   SEMICONDUCTORS ⇒ MORE DESIGNS OUTSIDE

   MAGNETICS ⇒ CATCH-UP!

   NEW DEVICES ⇒ ?

   PROGRAMS ⇒ SET TO STIMULATE THIS MARKET AND SUPPLY

   PATENTS BUYOUT

2. EXTERNAL STANDARDS ⇒ ?? GROUP CENTRALIZED

   SAFETY (UL, CSA, VDE)

   EMI

   INFORMATION PROCESSING (ANSII, ISO, CCITT)

   INTERFACES OF HARDWARE (NBS, CBEMA, GSA)

   LEGAL

3. CUSTOMER (HOW/DOES HE USE OUR MACHINES?)

4. Competitors – who evaluates?

GB
11/6/75

TRAINING

GENERAL BUSINESS ($, MARKET, PLANNING, SCHEDULING, RESOURCE ALLOCATION)

MARKETING AND P/L AWARENESS ⟹ ROTATION THROUGH P/L'S

(ESPECIALLY IMPORTANT AS OUR BUILDERS DRIFT AWAY FROM BEING USERS).

ALSO, TAKE ON P/L CONTRACTS IN CE

TECHNICAL

EVENTUAL RETRAED (WITH SLOWER GROWTH)

HARDWARE PEOPLE LEARN MORE SOFTWARE

NEW SKILLS FOR BOTH LOWER LEVEL INTEGRATION

HIGHER LEVEL OF INTEGRATION REQUIRES INDUSTRY ORIENTATION (E.G. BANKING, MANUFACTURING)

PEOPLE ⟹ LESS-ORIENTATION

MANUFACTURING SKILLS

GB
11/75

INTRA-ENGINEERING INTERFACES

(AND GROUP PROBLEMS)

ADV. DEV.

GETTING ACCEPTANCE OF VARIOUS PRODUCTS (TECHNOLOGY TRANSFER)

ESTABLISHING THIS FUNCTION IN VARIOUS GROUPS.

DEVELOPMENT

BETTER SYSTEMS FOCUS

HARDWARE/SOFTWARE CO-LOCATION

H/S CONTROL EXPERIMENT (VAX) HIGHLY MATRIXED

ARCHITECTURE CONTROL AND PLAN $\Longrightarrow$ WHERE??

BETTER DISKS $\Longrightarrow$ PEOPLE

BETTER DISKS AND MEM SUB-SYSTEM $\Longrightarrow$ NEED SYSTEM PEOPLE

LOW END PRODUCT PLETHORA $\Longrightarrow$ IN FUNCTION

HIGH END PLAN $\Longrightarrow$

SUPPORT

SEE MANUFACTURING

GB (CAN HE) (DOES HE WANT) TO "RUN" SUCH AN ORGANIZATION?

GB
11/6/75

THE DEVELOPMENT ORGANIZATION 1980

Assumptions:

Total Revenue

FY	74 75	76	77	78	79	80	81
9/6	420(27) 535(39)	745(27)	950(26)	1197(26)	1508(26)	1900	
NOR	~~420(27)~~	700	1,000	1,200	1,450	1,750	2,100

By Size

Syst > $100K	200 (29)	250	300	360	420 (24) ↓	400
Syst $25K - $100K	200 (28)	300	300	320	320 (18) ↓	400
Syst $ 5K - $ 25K	70 (10)	100	130	150	200 (11) =	250
Prods. $1K - $ 5K	60 (10)	100	150	200	240 (14) ↑	300
Prods. < $1K	20 (3)	30	50	70	120 (7) ↑	200
Services	150 (21)	220	270	350	450 (26) ↑	550
TOTAL	700	1,000	1,200	1,450	1,750	2,100

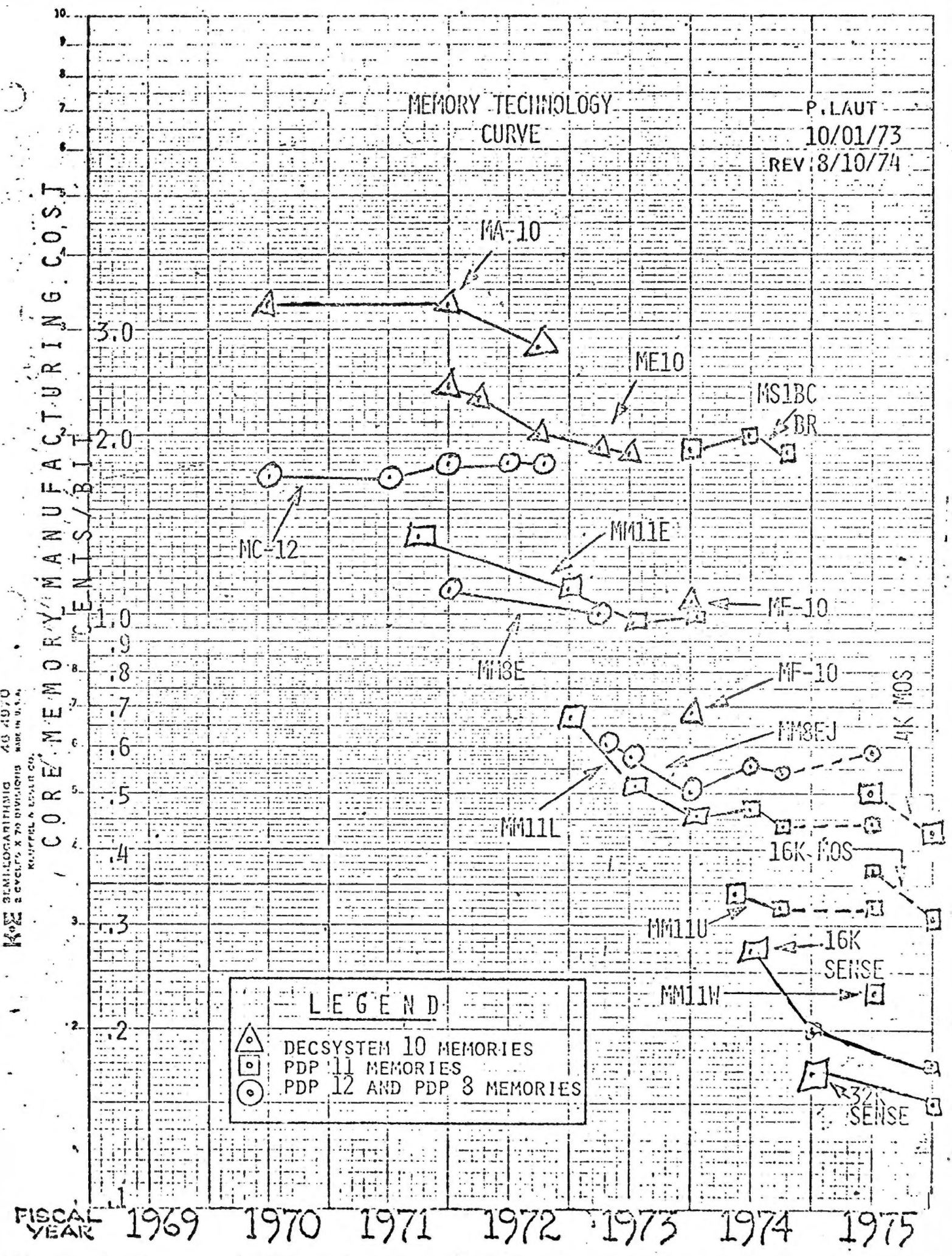
By Syst Family

DEC 10	80 (11)	120	170	200	250 (14) ↑	250
VAX	Ø 0	Ø	50	150	300 (17) ↑	400
11 UNIBUS	330 (49)	480	460	410	300 (17) ↓	300
Sub-UNIBUS	20 3	50	100	170	250 (14) ↑	350
PDP-8	50 6.6	30	20	20	10 (1) ↓	10
Components & Terminals (not systems)	50 6.6	80	100	120	150 (8.5) ↑	200
Other	20 3	20	30	30	40 2	40
Services	150 21	220	270	350	450 26 ↑	550
TOTAL	700	1,000	1,200	1,450	1,750	2,100

People 1220(6) 1305 (15) 1511 (19) 1.7~1.9 (19) 2~2.3 (19) 2.4~2.7

Space 240 (16) 280 (21) 340 (17) 400

R.J. Clayton
11/6/75


MEMORY TECHNOLOGY CURVE
P. LAUT
10/01/73
REV: 8/10/74
CORE MEMORY MANUFACTURING COST CENTS/BIT
FISCAL YEAR
1969
1970
1971
1972
1973
1974
1975
10.
9
8
7
6
5
4
3.0
2.0
1.0
.9
.8
.7
.6
.5
.4
.3
.2
.1
MA-10
ME10
MS1BC
BR
MC-12
MM11E
MF-10
MM8E
MF-10
MOS
MM8EJ
4K
MM11L
16K MOS
MM11U
16K
SENSE
MM11W
32K
SENSE
LEGEND
DECSYSTEM 10 MEMORIES
PDP 11 MEMORIES
PDP 12 AND PDP 8 MEMORIES

What Does a Technology Company Look Like? (A look at Microsoft and Digital aka DEC)

Gordon Bell

Perspective from the depths of Microsoft Research

Three part comparison with MSFT

- Observations on high tech organization cultures based on my experience at Digital aka DEC, Microsoft, and various high tech startups
  - Is it scalable?
  - Built productively on appropriate technology?

Microsoft Secrets

Cusumano and Selby

1. Organizing and managing the company
   - Find smart people who know technology & business
     Hiring pool, interviews, turn-over…
2. Managing creative people and technical skills
   - Small teams, overlapping functional specialists
3. Compete with products and standards *NOT brand Bodies!*
   - Pioneer and orchestrate mass markets… try many
4. Defining products and development processes
   - Focus creativity on evolution and fixing resources
5. Develop and ship products
   - Do it in parallel, synchronize and stabilize
6. Build a learning organization
   - Improve through continuous self-critiquing, feedback, and sharing
7. **Attack the future…** ***be or be in, the mainstream… home, games, SAAS/SAS (SW as Services),***

Microsoft

- Product and process. Architecture for // development
- HBR Article: Architecture, interfaces, int/ext developers
  - Growing, increasingly valuable platform
- Small teams, interconnect with sync
- One development site w/ research. Large capital expenditures.
- Common language. Common development environment. …whole company tests (we eat our own dog food)
- No single point of developer failure
- Managers who create technology, make technical decisions
- Quick decision making re. business etc. issues
- Feedback from users…e.g. *Do you want to send this to MS?*
- Learn from the past…v3 is great
- *Try things, don't give up…* be prepared to fail vod, webtv, …
- *An understanding and appreciation for the individual… stock*
- Research!

DEC Cultural Beliefs (Ed Schein ms.) unconscious, shared, tacit assumptions

1. “Rational & Active Problem Solving”
2. Giving People Freedom Will Make Them Responsible
3. Responsibility means Being on Top of One’s Job, and owning one’s own Problems. (He who plans, does.)
4. “Truth through Conflict” and “Buy-In”
5. Internal Competition and “Let the Market Decide”
6. Management by Passion, but Work should be Fun and Enjoyable. Benign Manipulation or Controlled Chaos
7. Perpetual Learning
8. Loyalty and Life Time Employment
9. *Moral commitment to customers*

Digital according to Schein

- Individualism
- Truth through conflict
- Personal responsibility
- Engineering arrogance
- Market competition…let it decide
- Paternalistic commitment to people
- Organizational idealism
- Moral commitment to customers

Digital-gb 1

- **Great responsibility, freedom, and trust in the individual.**
  - **"Do the right thing." Open door-email. *Scalability is a problem.***
  - **Paternalistic organization.**
- **"He who proposes, does." Very little was top-down**
  - **Product managers are part of the product (conflict at low level)**
  - **Small, responsible teams. Make their own schedules.**
  - **CDC: Cray left, machines obsolete, ETA had no legacy, Price (CE0) thought top decides, bottom executes**
- **Conflict is good. Came from starting from M.I.T. Data decides**
- **OK to have competing and overlapping technology/projects/products, *but know when to cut them! When DEC started down, it had almost 10 platforms***

Digital gb-2

- **Focus on Customer. Let them decide the strategy.**
- **Profit is essential …all products were measured**
- **“Either make the standard or follow it, if you fail to make the standard you get to do it twice.” IBM PC versus 3**
- **“Make what you can sell, not what you can buy.” Therefore: sell everything you make.” semi**
- **Wilkes: “Stay in the mainstream”… SOS, ECL**
- **Beware of complex structures. Buyer-seller relationships versus matrix**

DEC: Schein View of What's Learned

"1. Don't judge a company by its public face.

2. A culture of innovation does not scale up; "functional familiarity" and "truth through debate" are lost with size; "do the right thing" becomes dysfunctional; managerial sense of responsibility changes with age and maturity; buy-in becomes superficial agreement.

3. If a culture of innovation only works at a certain small size, the organization must either find a way to break away small units that continue to innovate or abandon innovation as a strategic priority.

4. A culture that breeds success and growth over a considerable time becomes stable and embedded even if it contains dysfunctional elements; changing the culture means changing key people who are the culture carriers

5. Cultures are sometimes stronger than organizations

6. A successful technical vision will eventually create its own competition and, therefore, changes in technology and in the market conditions; dominant designs will emerge and commoditization will occur.

7. Successful growth based on a technical vision will hide business problems and inefficiencies until an economic crisis reveals them or until the business gene is switched on; recognition of those problems will not necessarily produce remedial action.

8. If a growing business lacks the business gene, the Board must act to introduce that gene.

9. If you try to do everything, you may end up not doing anything very well.

10. How the market evolves may not reflect either the best technology or the most obvious logic.

11. A technical vision that is right for its time can blind you to technical evolution

12. The value of "listening to your customers" depends upon which customers you choose to listen to.

13. The type of Governance System an organization uses must evolve as the organization matures

14. The events and forces act in unison"

A Puzzling Question

What would cause one of the industrial stars of the 20th century, ***and one of the first truly digital economy companies,*** *at the very zenith of its success, to begin a precipitous decline that would eventually result in its demise?*

Courtesy Pete DeLisi

Why did Digital fail (GB)

- **The top 3-5 execs didn't understand computing**
  - Moore's Law, Standards and their effect
  - Platforms and their support
  - Levels of integration, make-buy, and ISVs
  - Competitor metrics: it simply got "out of control"
- Destroyed its marketing organization, requiring a complex matrixed organization, but lacking ISVs
- Didn't exploit: printing (e.g. HP), networking (e.g. Cisco), the Web, and UNIX
- Did: ECL mainframe, non-compatible PC, too many platforms, semi-fabs without partnerships

Manufacturing has never been DEC's strength as a high overhead, bureaucratic, slow-moving, conservative old boy network organization. It is slow to get products to the marketplace with a low degree of automation. Cost reduction consists of going overseas to low cost producers to buy out from Tandy. DEC will be unable to compete with Japanese producers in the future years. It had a strong Taiwan group.

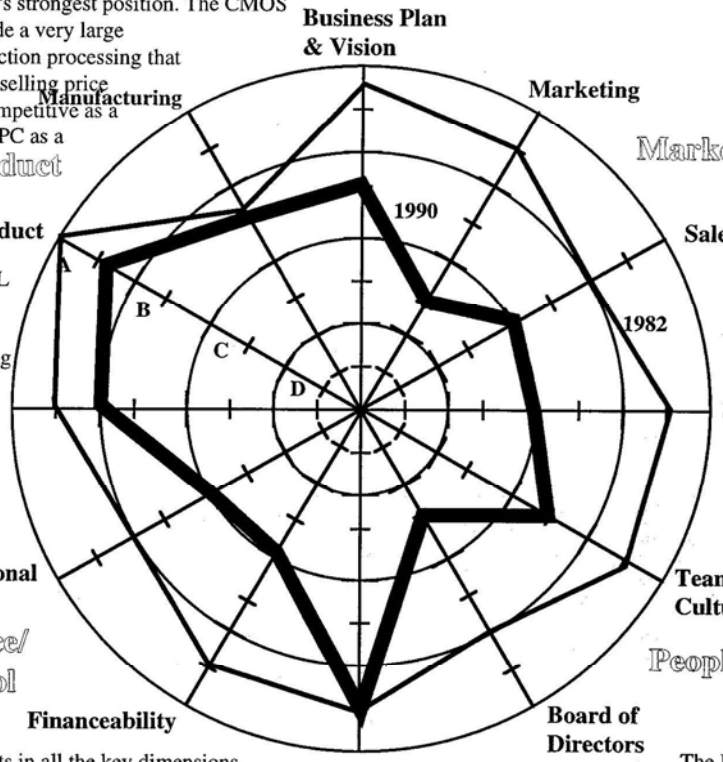
Products overall are not bad. Communication is DEC's strongest position. The CMOS VAX micros have saved DEC. DEC should have made a very large multiprocessor with 20-50 microprocessor for transaction processing that would have betat IBM, Tandem, etc. and kept higher selling price and margins. The ECL 9000 is not especially cost-competitive as a mainframe. Unlike HP, DEC failed to respond to the PC as a standard that sits on every desk.
The product flaw is there are TOO MANY!

Engineering and technology have been DEC's past strengths, especially in architecture, networking, software, semiconductuctors and large disks. The ECL 9000 took too many resources, robbing the company of potential gains elsewhere. DEC spends more on R&D than any other mfg. outside of IBM. Engineering failed to build a competitive workstation or PC, and hence is disproportionally higher than it should be. Strength in termals and low cost systems were not used to get competitive products in the PC and small server product space. DEC missed key products, technologies, and cost-reductions.

Control seems very poor... namely the company seems unable to do what it says it's going to do. The greatest source of poor control is in productivity, when it started buying more from outside and failed to downsize.

Every customer, employee, and stockholder is concerned witht DEC's strategy or Vision. Is it simply: we provide every possible platform, you choose and find the Application software?

Marketing is the number two problem. It has completely lost the communication between customer application segments (e.g. ECAD, insurance office, semiconductor manufacturer) and the product planning. As such it has no way to decide what to get for applications software or what platforms to recommend. The vast array of products with no market means the customer has to decide.



Sales is led by a non-salesman, such an organization is flawed Until DEC puts the field organization on a commission plan where the salesmen are really forced to produce, the sales folks will probably spend more time concerned about politics than customers and selling. Distribution of computing is moving from the 100K salesman. to the retail level.

KHO is clearly a legend. Recent performance is poor and he has no suitable successor. He now shares the CEO slot with someone with less stature. It is ironic that someone who failed in products and controlling manufactuing cost is COO. His failure is simply not being the CEO and seeing to it that he has a quality team and organization.

Is the top level team fundamentally weak without a representation of the marketing, sales, and a disconnect of the product builders? In the early 1980s, the Operations Committee was extremely strong. The problem then was that the team was not lead by KHO to resolve and find a product direction that would be successful in personal computing. The result, IBM walked away with it .... Compaq formed, etc. Similar stories can be told about worstations, minisupers, and RISC.

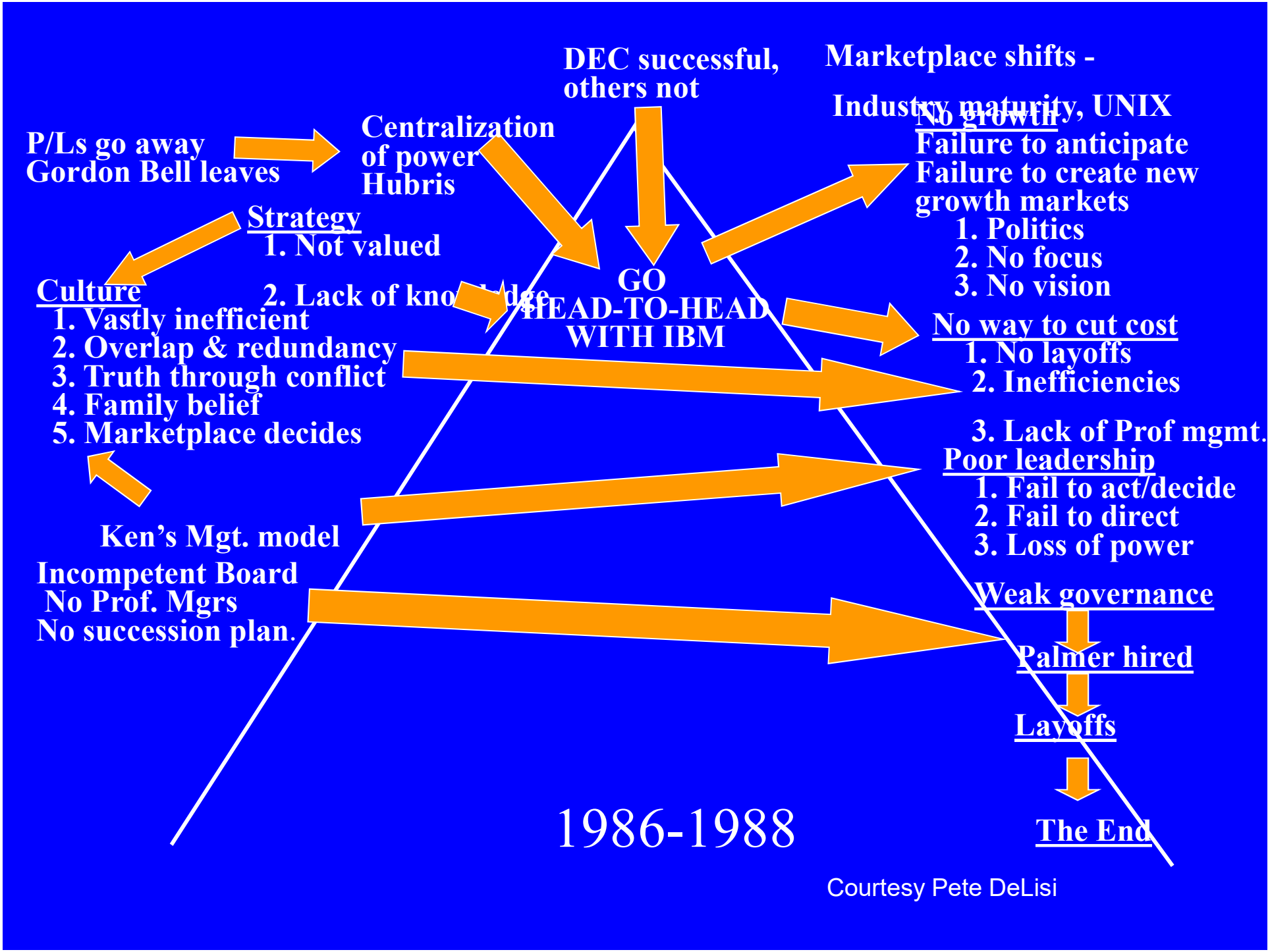
Financeability will not continue without improvements in all the key dimensions, together with a vision for the company of how it is to respond to the key exogeneous pressures: demand for commodity standards which put enormous pressure on the expense lines; lower cost systems that yield exceptional price per MIPS and do the work of yesteryear's systems that cost 10X the price.
DEC has to position itself so as to not look like a losing mini company such as DG, HP, WANG, Prime or a traditional mainframe company such as Unisys, CDC, Bull.

DEC missed 3 major market segments: PCs, Workstations, and minisupers, all of which ate into minis. It missed RISC as a technology. Betting on the company in the 1990s is unwise given the overall situartion in the markct and in all other dimensions.

DEC has a healthy cash position, but this will evaporate quickly with loss.
The question is what is the true balance sheet of the company, given that an appreciable amount is in real estate and factory?

The Board is considerably weaker with the loss of General. Doriot who is probably the only person that Ken could talk with or listen to. Everett is the only board member who has an understanding of computers. Although the board members are ok,and have been connected, all are retired and are not in touch with the issues of the 1980s vis a vis computation. The average PC user (a few 10 millions of them) is in better touch with computing than the board, top level team, and the CEO.

Bell-Mason Diagnostic Relational Graph With A Plot of Gordon Bell's Evaluatation of Digital Equipment Corp. 11/90



Courtesy Pete DeLisi

Digital's Trials by Technology…
With time, high tech becomes a commodity.

"DEC found guilty of violating Moore's Law …" –gbell

1. Designing and building first transistor circuits. 1957-1965
2. Transition to integrated circuits & modulo 8 bits 1965-1975
3. Design with VLSI; *manufacturing VLSI* *1975-2002*
4. Design of "clusters" as the ultimate computer 1983- ????
5. *Quadruple whammy c1983 – "killer" micros, UNIX: PC, Workstations, CMOS AND UNIX , as "standards" Anyone can manufacturer computers in their dorm! "You mean to say, our new ECL mainframe is not equal to our latest CMOS chip?" –Ken Olsen c1990*
6. *Fail to exploit: networks, WWW, printers, clusters…*

Paul Kampas' View of the Computer Industry and DEC Failure

Copyrighted material

Due to copyright considerations, pages161-167 of this PDF are not available online.

These pages contain graphics and charts by Paul Kampas analyzing DEC's decline.

For questions about access to this material, please contact the Computer History Museum: http://www.computerhistory.org/collections/requests/

The End

****
* d i g i t a l *
****

TO: ENG STAFF:
JACK SMITH

DATE: MON 15 FEB 1982 6:55 AM EST
FROM: GORDON BELL
DEPT: ENG STAFF
EXT: 223-2236
LOC/MAIL STOP: ML12-1/A51

SUBJECT: TASK FORCES, COMMITTEES; NOD; C-I T/F; PRODUCTIVITY REV.

I just read the minutes of two meetings of a task force called Customer Installability. It is not a task force it is a sewing circle consisting of 21 people! If there weren't 3 people there who I know have real work to do and have done good work, I would ask that we simply dismiss the whole group.

The minutes contain no real information on the subject. We already have a spec on what CI is, and we have to do some work on products to get it. This is not the work of a committee.

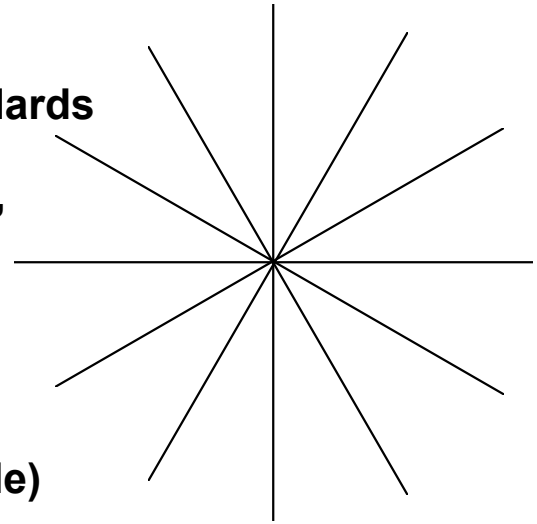
My point, I would like you to come forward with a list of the various committees and task forces, etc that are working within your group during the productivity review. I don't want to look at them, but I expect you to have, and I want to know that you understand what's going on in your area.

I believe 1/2 of these people could be let go from DEC today and our productivity would take a sharp rise. If this is the case, I would like to have their names and since we have the reputation for never firing anyone we can put them in a new group I propose we start called NOD (No Output Division) where they won't take time from people who have real work to do.
PS
I'm quite serious about NOD. Since it is so difficult to get rid of people, I want to make us at least not have them mixed in with the workers and suck up good people's time.

15-FEB-82 06:55:06 S 31987 BURT

NOD: No Output Division

The Technology Balance Sheet



Plan with:
Schedule of
Milestones &
Resources

Eng. Specs:
User view (e.g., data sheets,
manuals) and Features, Functions,
Benefit (FFB)
Eng. view (e.g., product structure,
how to design)

Quality Design
Methods/Processes

External (industry),
internal, & other standards

Manufacturing Specs.
(i.e. How to
Produce Product)

Indigenous (i.e., skills,tools,
& technical know how)
& exogenous technology
base (e.g., patents)

Chief Technical Officer
(Eng. VP)

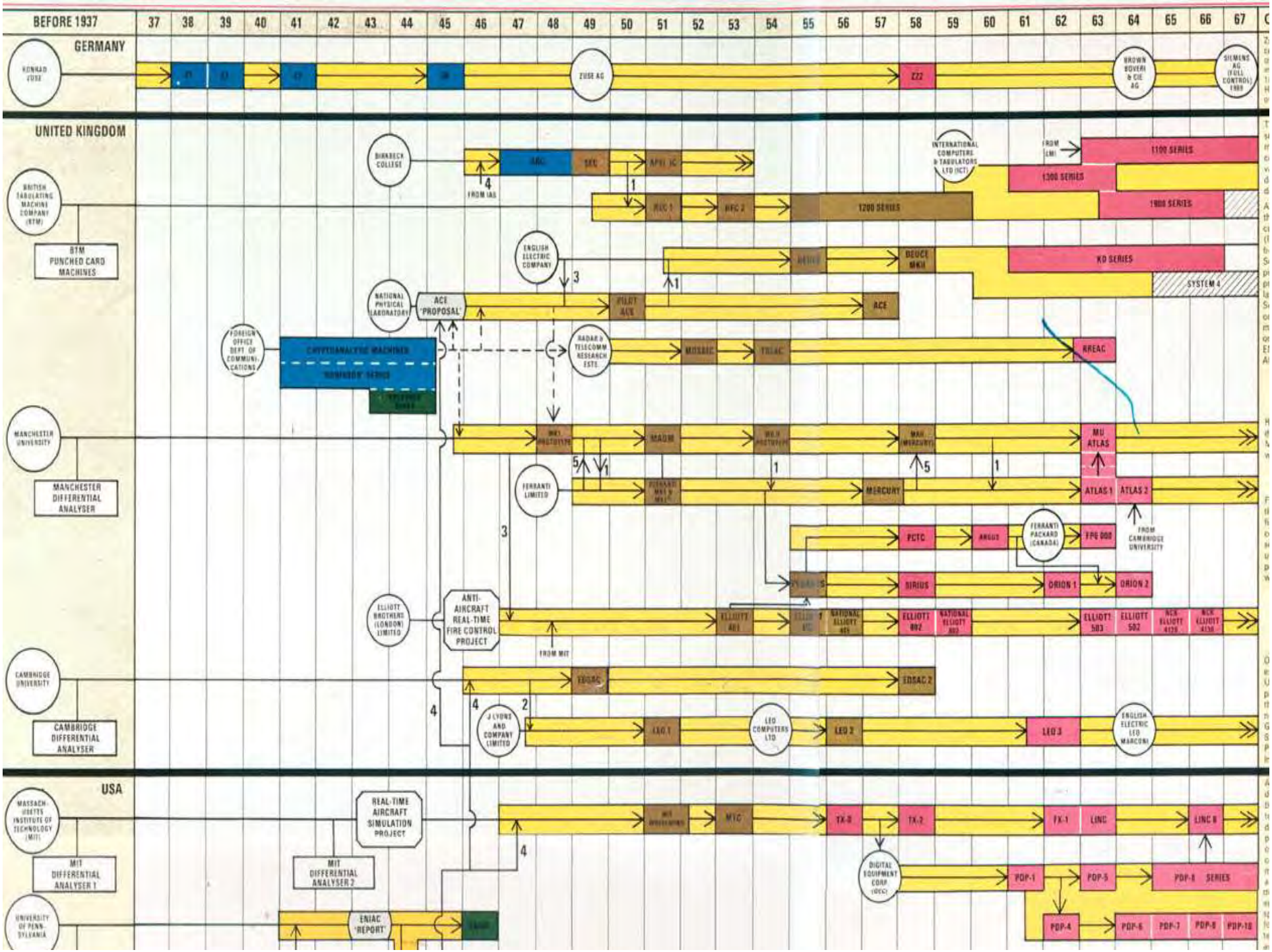
Operational Management
(ability to fulfil plans-
specs, resources, schedule)

Team, Product Architect,
Engineering Culture

Technology Advisory Board

Technology
Future --
Financeability

$s
(Cash / Budget)


BEFORE 1937
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
GERMANY
KONRAD ZUSE
ZUSE AG
Z22
BROWN BOVERI & CIE AG
SIEMENS AG (FULL CONTROL) 1969
UNITED KINGDOM
BIRKBECK COLLEGE
FROM IAS
INTERNATIONAL COMPUTERS & TABULATORS LTD (ICT)
FROM LMI
1100 SERIES
1300 SERIES
1900 SERIES
BRITISH TABULATING MACHINE COMPANY (BTM)
BTM PUNCHED CARD MACHINES
1200 SERIES
ENGLISH ELECTRIC COMPANY
DEUCE
MK II
KDF SERIES
SYSTEM 4
NATIONAL PHYSICAL LABORATORY
ACE 'PROPOSAL'
PILOT ACE
ACE
FOREIGN OFFICE DEPT OF COMMUNICATIONS
CRYPTANALYTIC MACHINES
'HOWARD' SERIES
RADAR & TELECOMM RESEARCH ESTS.
MOSAIC
TRIAC
KREAC
MANCHESTER UNIVERSITY
MANCHESTER DIFFERENTIAL ANALYSER
MADM
MU ATLAS
FERRANTI LIMITED
MERCURY
ATLAS 1
ATLAS 2
FROM CAMBRIDGE UNIVERSITY
PEGASUS
PEGASUS 2
FERRANTI PACKARD (CANADA)
FPE 000
PEGASUS
PEGASUS 2
PCTC
ARGUS
SIRIUS
ORION 1
ORION 2
ELLIOTT BROTHERS (LONDON) LIMITED
ANTI-AIRCRAFT REAL-TIME FIRE CONTROL PROJECT
FROM MIT
ELLIOTT 401
ELLIOTT 402
ELLIOTT 503
ELLIOTT 502
CAMBRIDGE UNIVERSITY
CAMBRIDGE DIFFERENTIAL ANALYSER
EDSAC
EDSAC 2
J LYONS AND COMPANY LIMITED
LEO I
LEO COMPUTERS LTD
LEO 2
LEO 3
ENGLISH ELECTRIC LEO MARCONI
USA
MASSACHUSETTS INSTITUTE OF TECHNOLOGY (MIT)
MIT DIFFERENTIAL ANALYSER 1
REAL-TIME AIRCRAFT SIMULATION PROJECT
MIT DIFFERENTIAL ANALYSER 2
WHIRLWIND I
MTC
TX-0
TX-2
DIGITAL EQUIPMENT CORP. (DEC)
PDP-1
PDP-5
PDP-8 SERIES
LINC
LINC 8
UNIVERSITY OF PENNSYLVANIA
ENIAC 'REPORT'
ENIAC
PDP-4
PDP-6
PDP-7
PDP-8
PDP-10

Gordon's Personal View of The Early Days of Digital…

DECWorld, 16 June 2001

Gordon Bell

gbell@microsoft.com

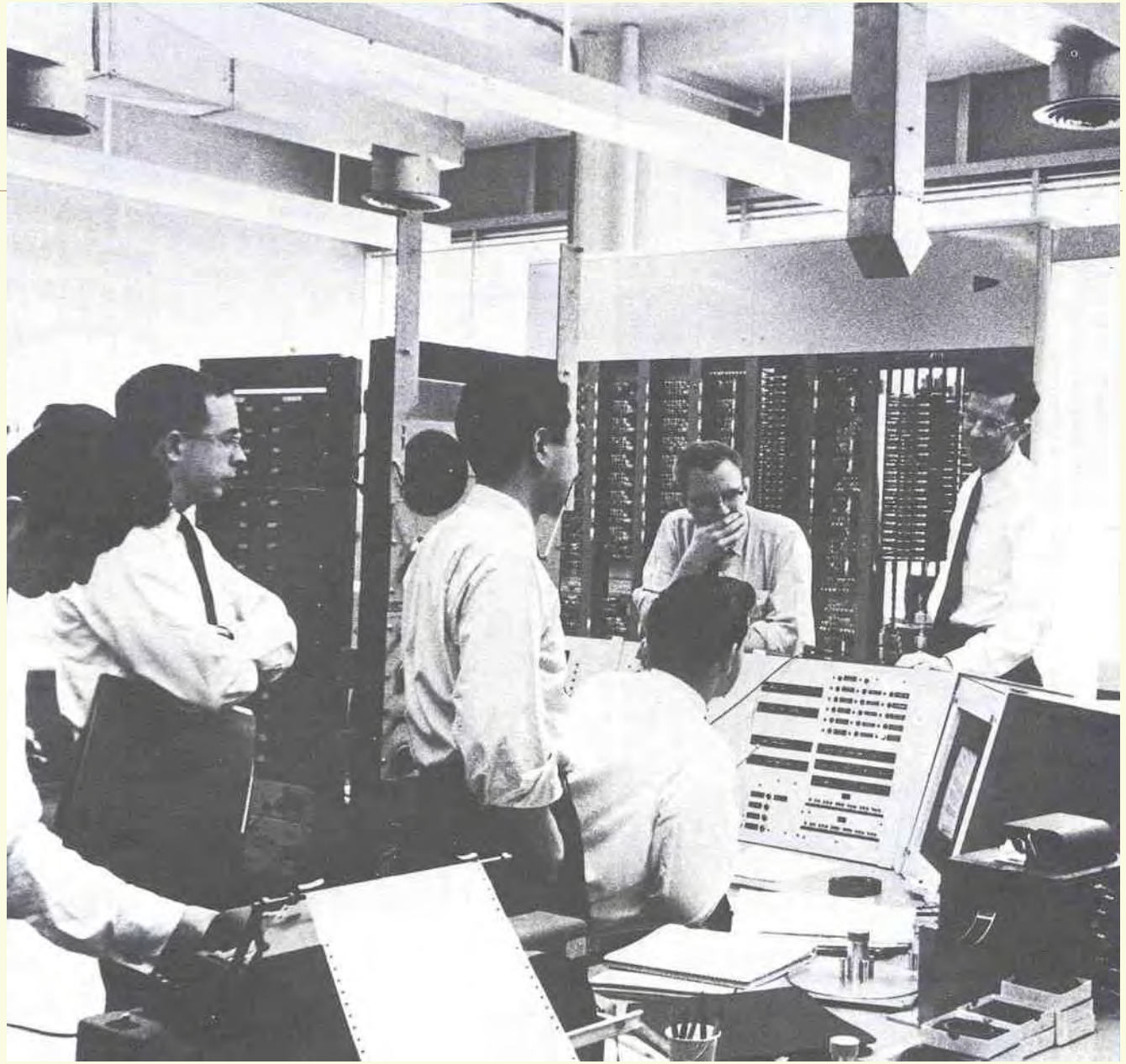
http://www.research.microsoft.com/~gbell

Whirlwind c1953 … 1st generation, 16-bit word; 4 KB memory; 8 K drum

Whirlwind begot TX-O/TX-2 begot DEC PDP-1
Real time, first compiler, ECAD, text editor

SAGE (Semi-Automatic Ground Environment) Operator Console

MIT Speech group with TX-0, c1959.

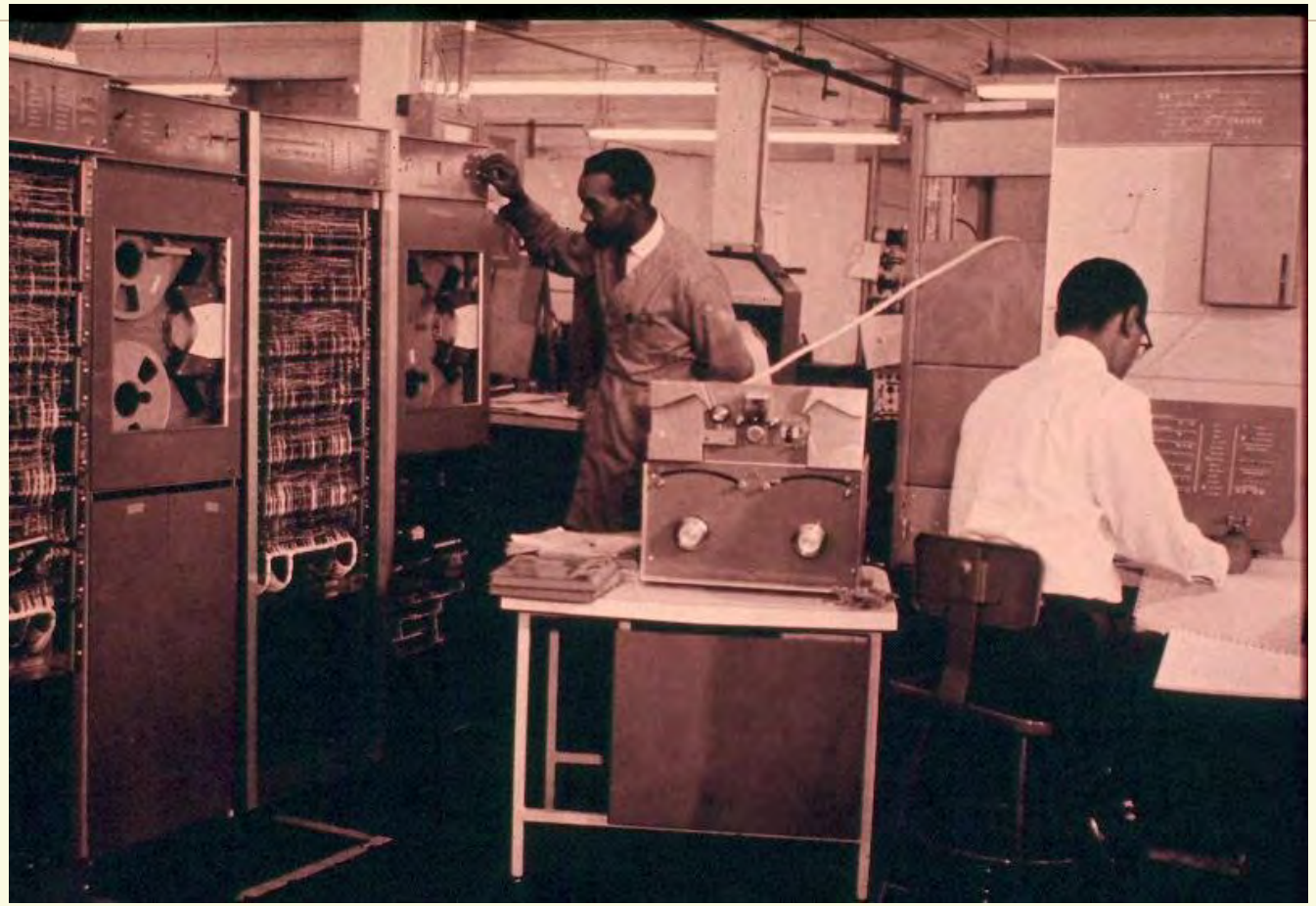


DEC PDP-1 c1961

DEC PDP-1
c1961
Being tested
Building ?

PDP-1 Production Line c 1962

Livermore Labs machine: they bought one of everything in our virtual catalog



PDP-4

Wes Clark & LINC c1962: Personal computers for bio-medical research

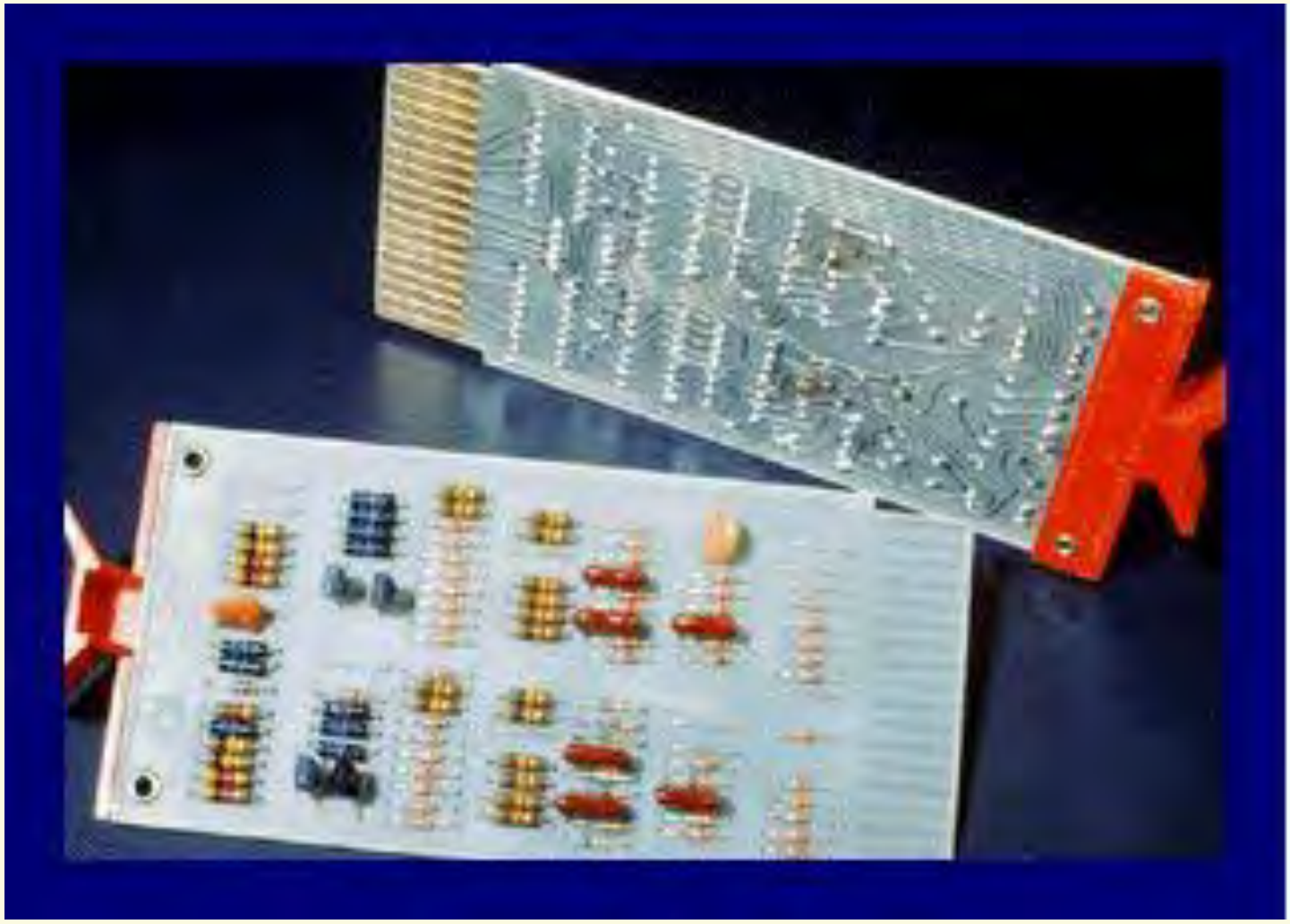
PDP-5 c1964: PDP-8 predecessor

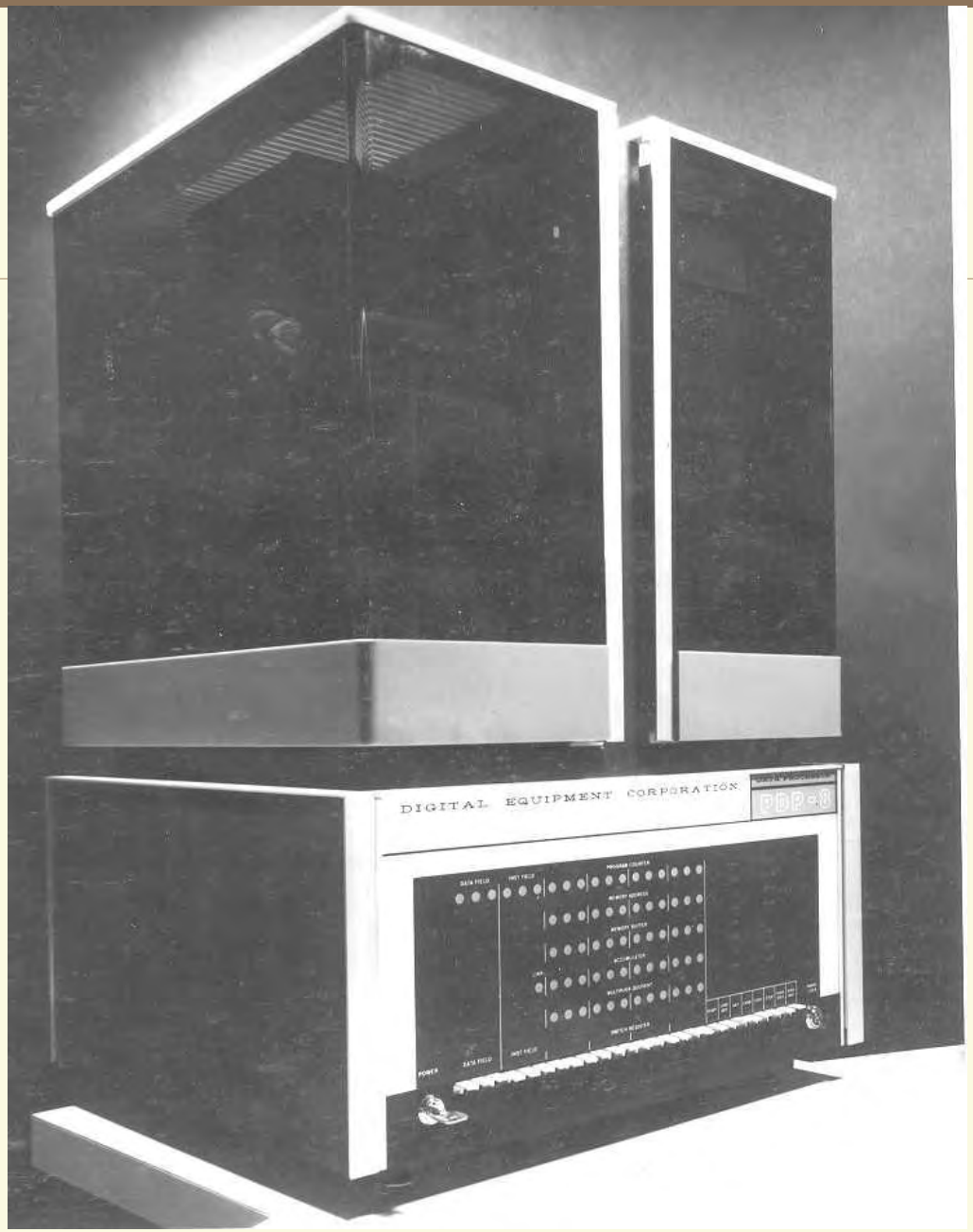
Process control, real time experiments. Fortran ran in 4 K, 12 bit words

PDP- 5:

as
pulse
height
analyzer

PDP-8 Modules

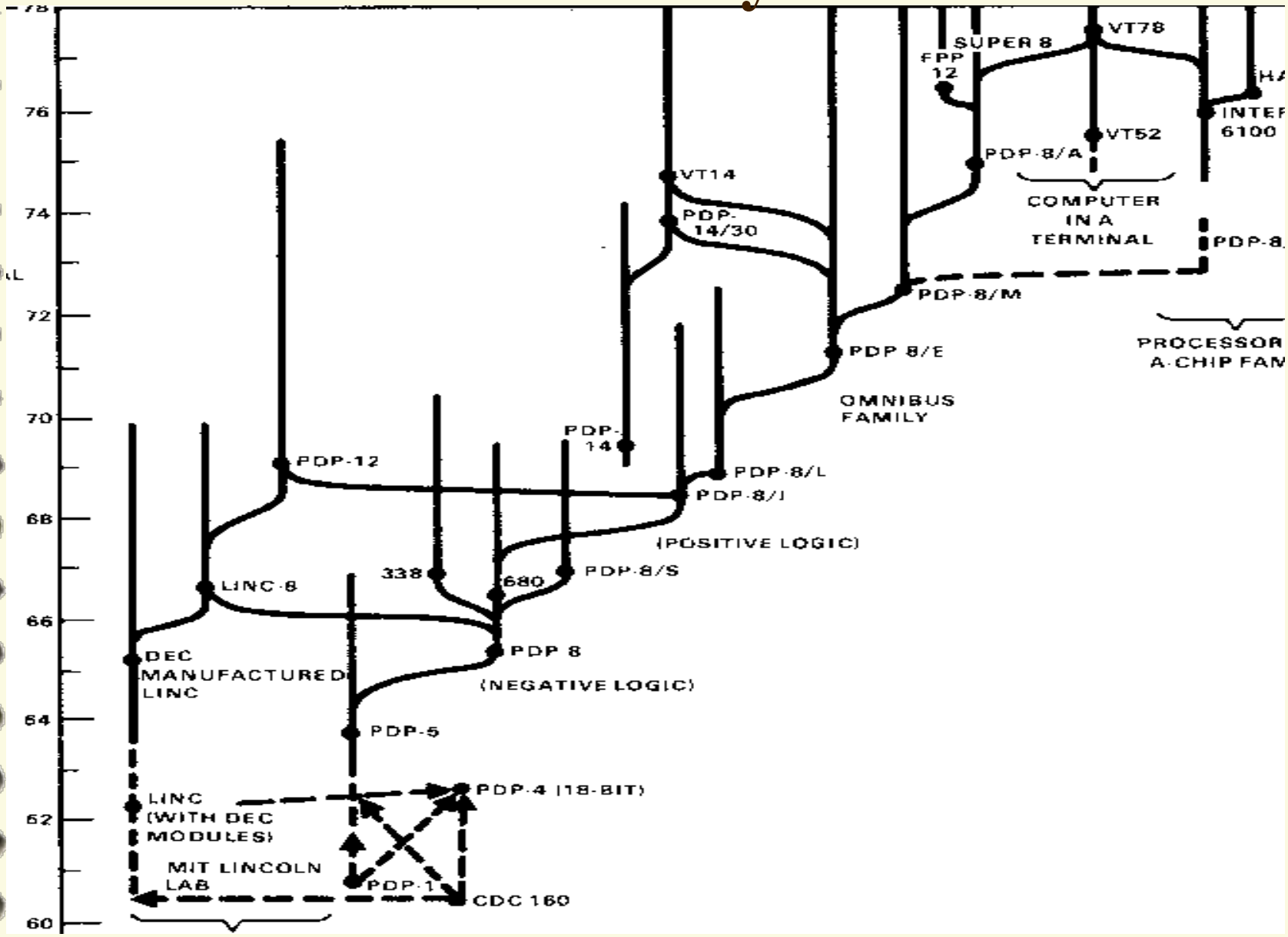




PDP-8: first mini

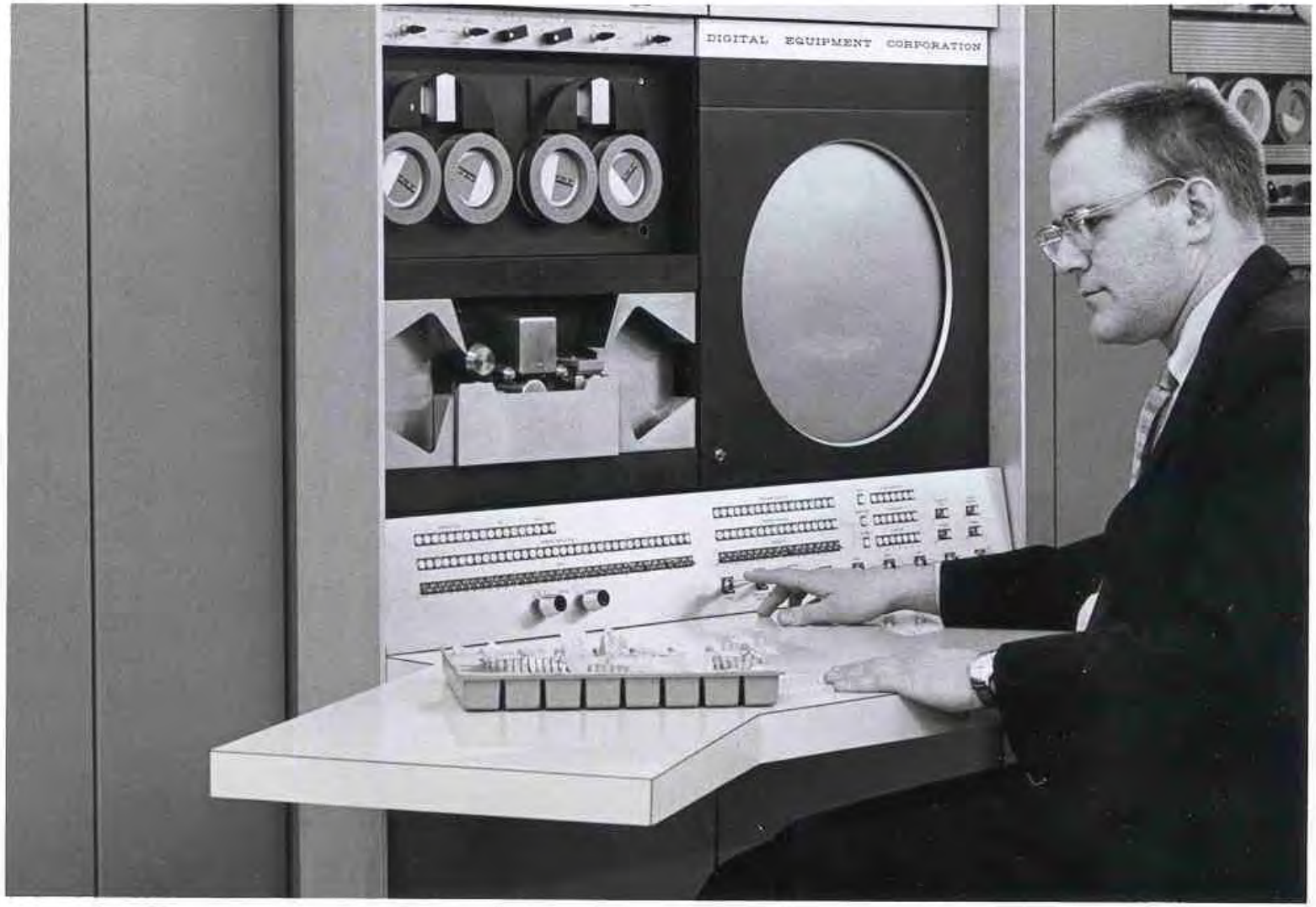
First OEM computer.
OS/8 (from timesharing) begot RT-11 begot CPM

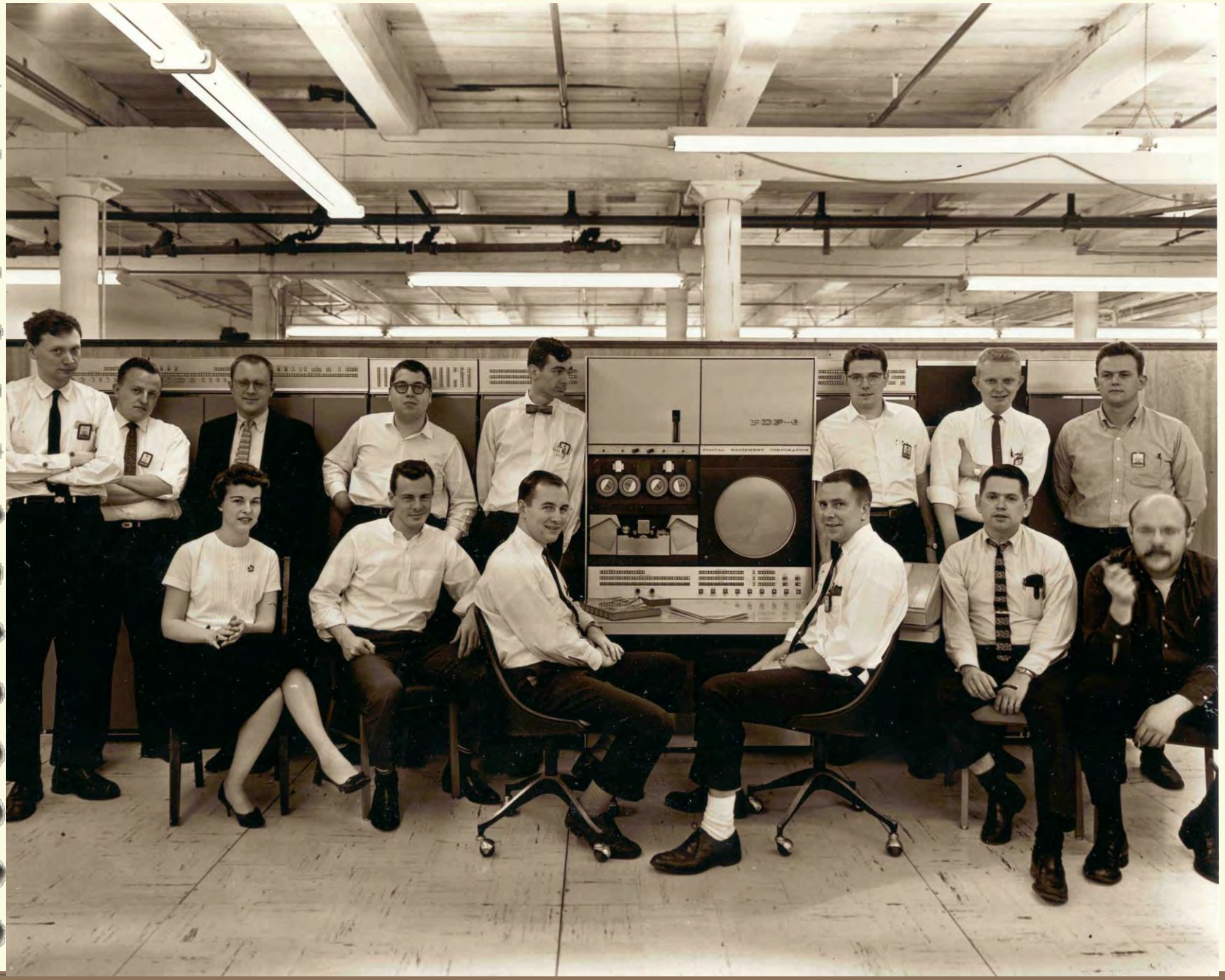
PDP-8 and Linc Family Tree



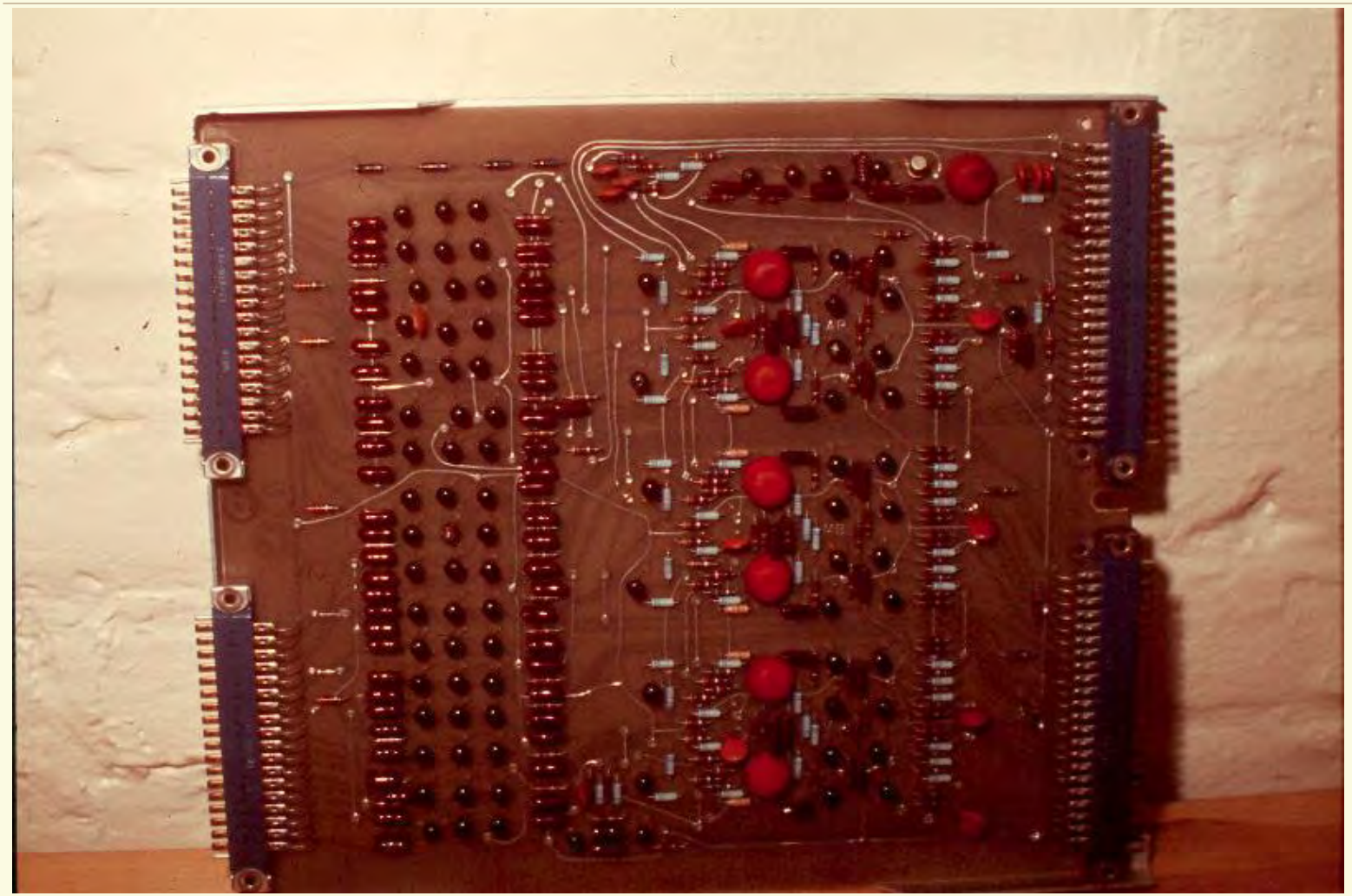
Timesharing: giving everyone their own, low cost, personal computer

PDP-6 with GB at the console

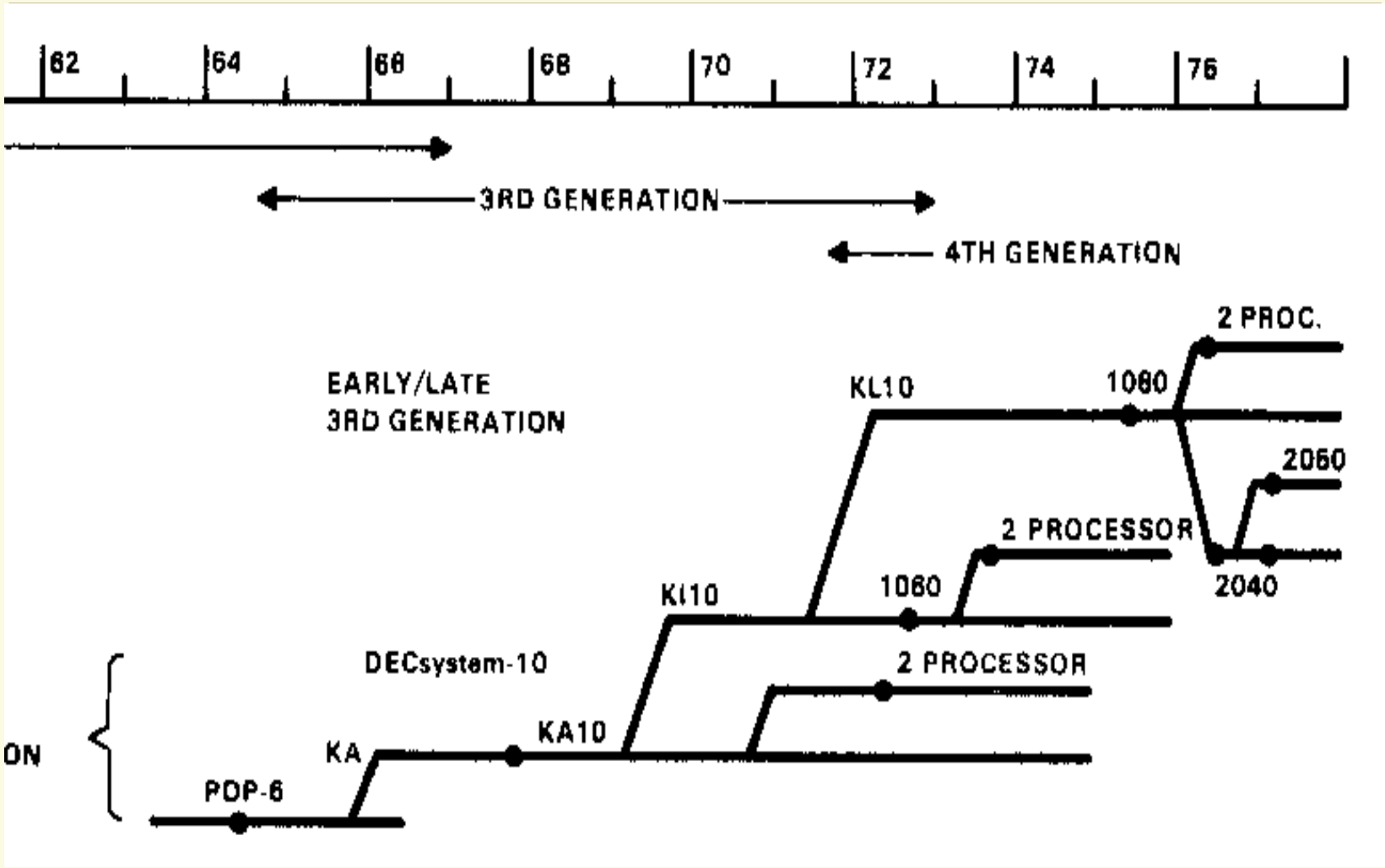



PDP-8
DIGITAL EQUIPMENT CORPORATION

Gordon's Packaging Folly: double sided connectors for PDP-6

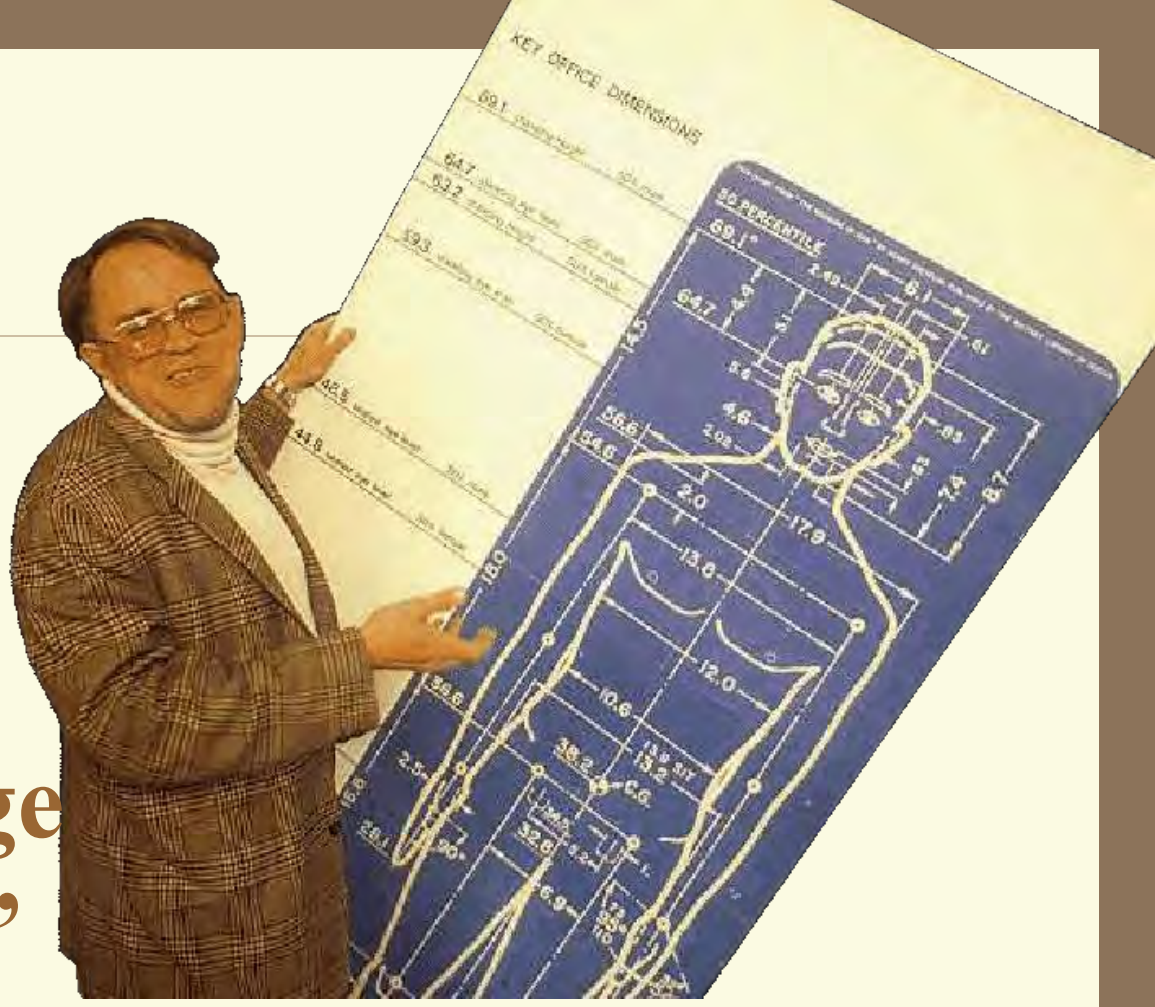


PDP-6/10/ DECsystem 10/20 family tree



Minis and timesharing contributions

- Editors, calculators, interactive debuggers, interpreters, including mail and chat from timesharing
- Minis established embedded computers, importance of I/O to interconnect anything
- SpaceWar demonstrated interactive graphics and settled lots of later law suits
- OEM Distribution and marketing model… Harlan Anderson, after Tecumseh
- SCO's all-in-one module and computer handbooks…

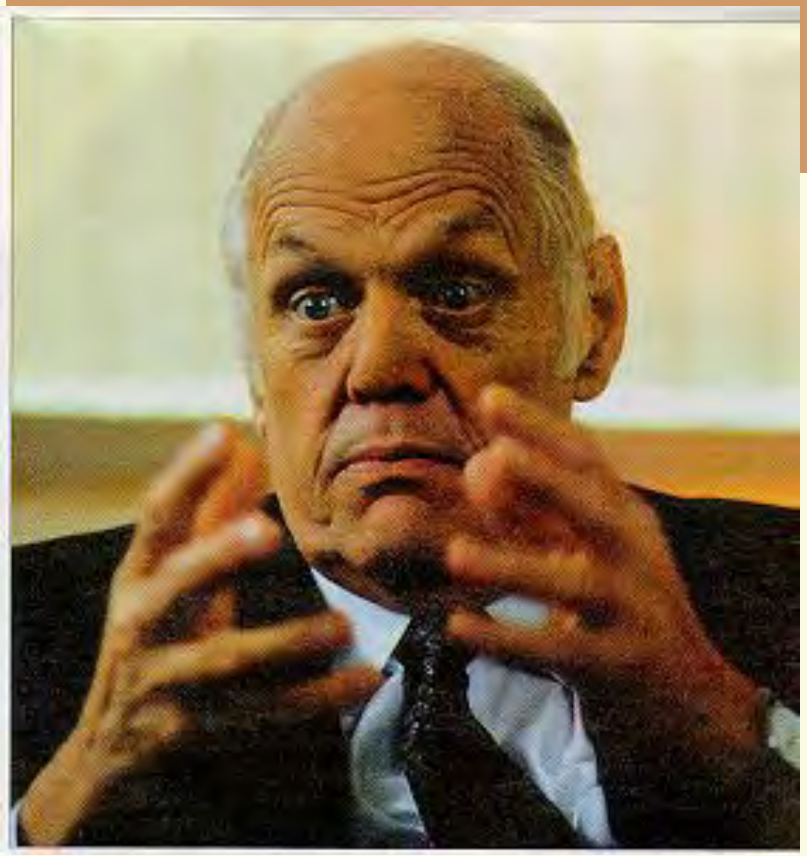


Equating yourself to the average "user/buyer" is risky . . . unless you're an average user like me. G. Bell

Why didn't Digital lead personal computers?

That's another story…

There is no reason anyone would want a computer in their home.



Ken Olsen
President, Chairman and founder of Digital, 1977

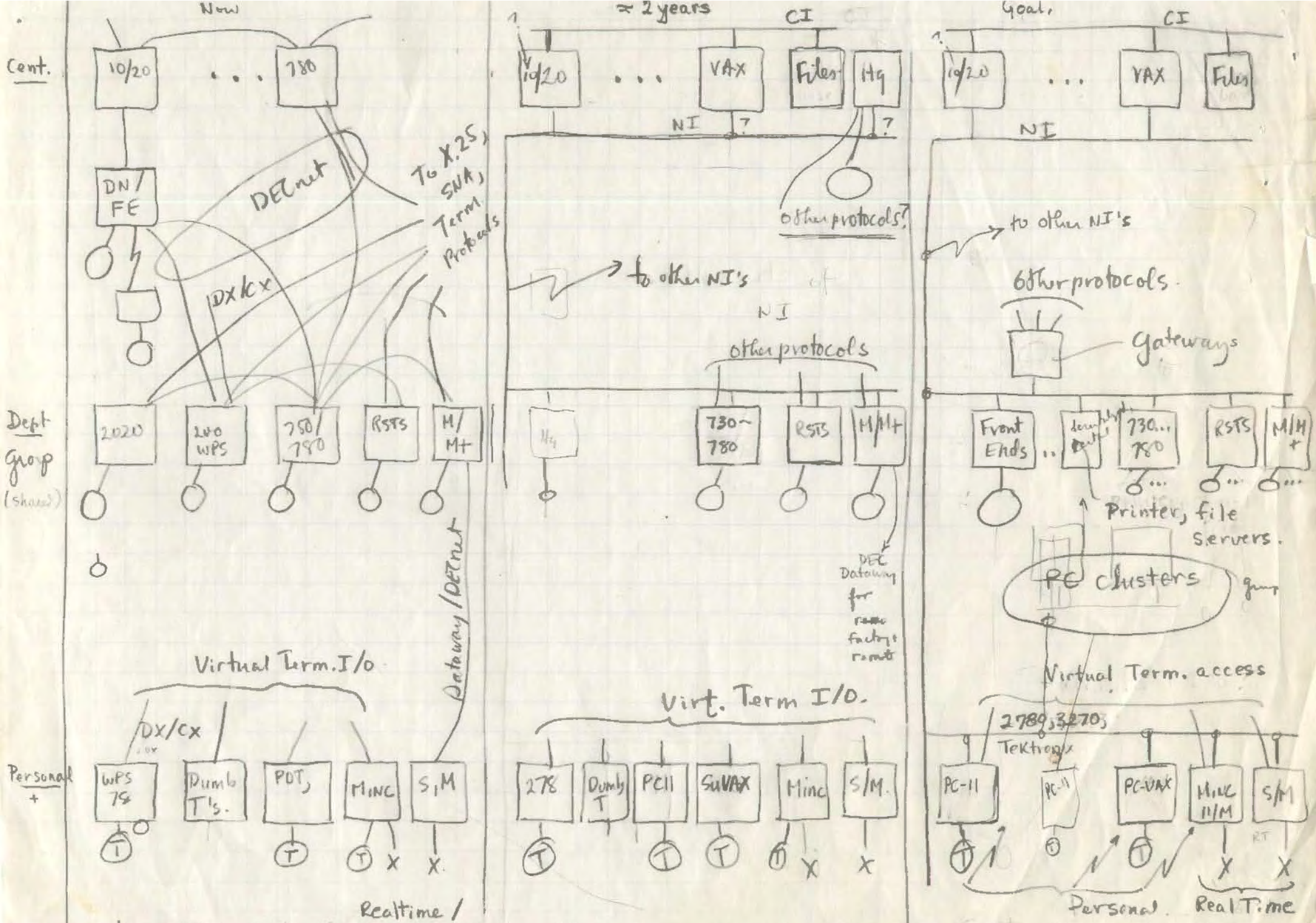
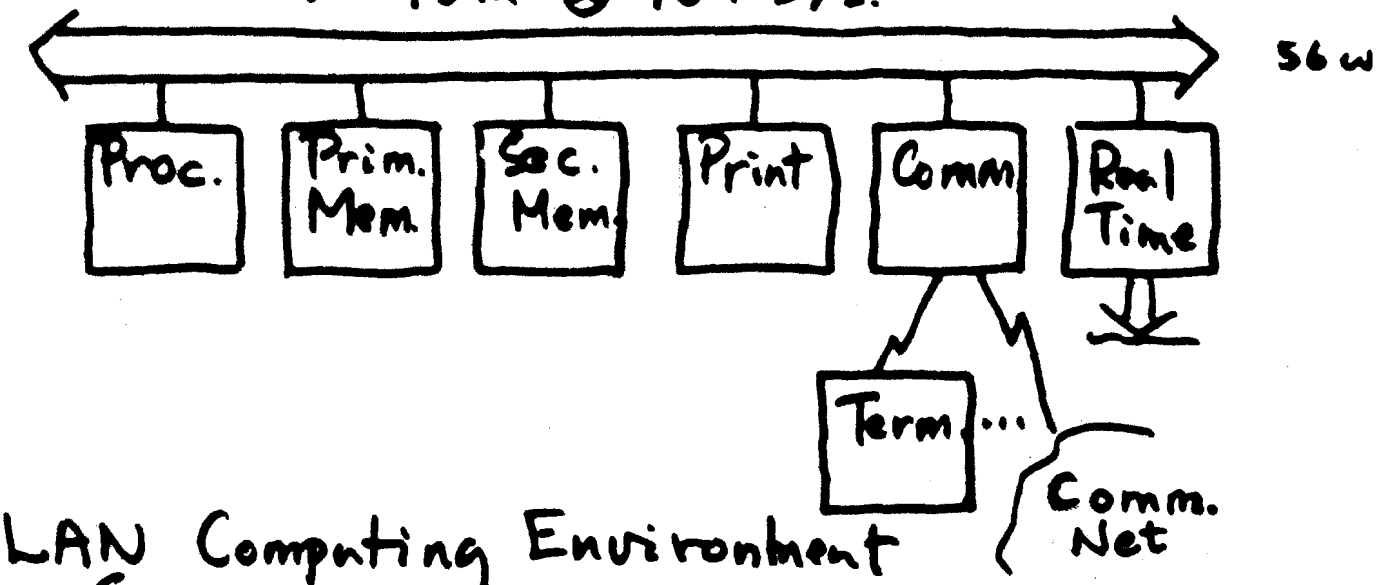


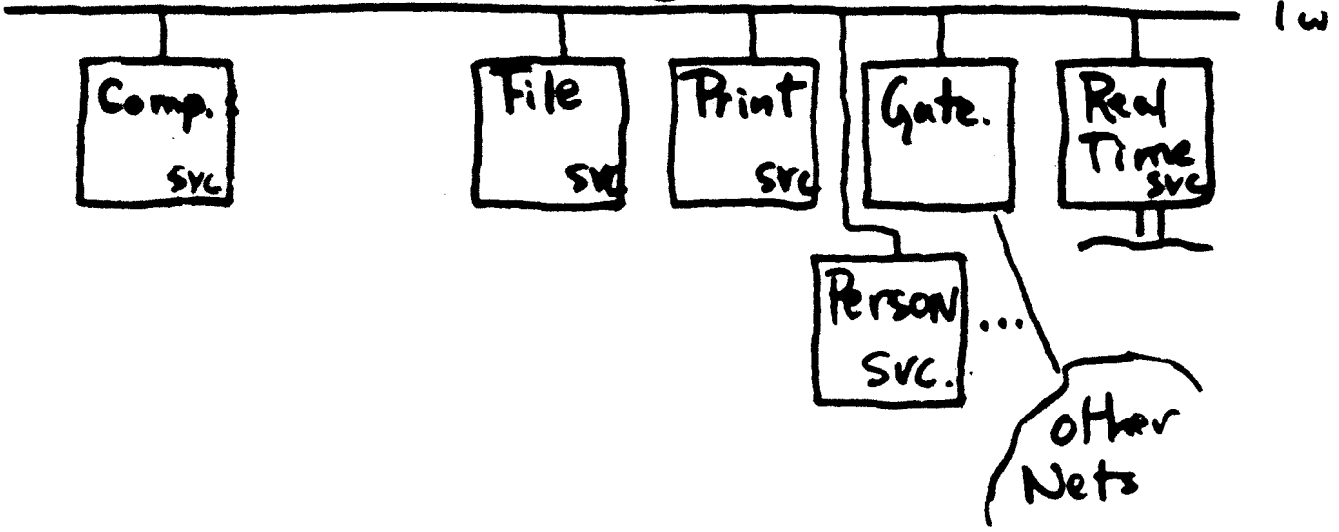
Fig GAE Galactic Architecture Evolution

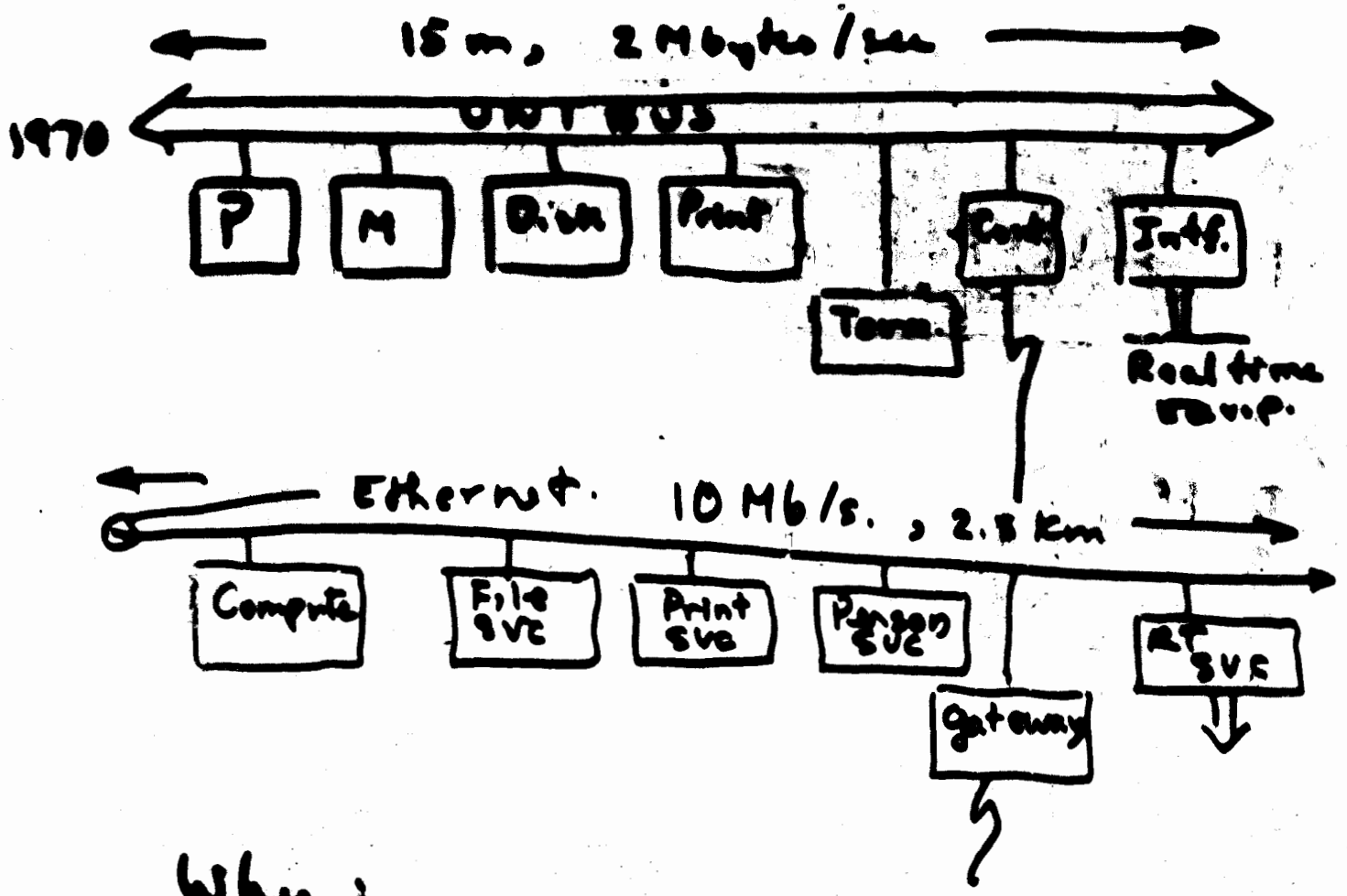
10/13/80
GB

Single Computer ~ Circa 1970, 80...
(Unibus) 15m @ 16 Mb/s.



LAN Computing Environment
(Ethernet) 2.5 Km. @ 10 Mb/s.





Why:

Ethernet's The Unibus of the 5th Generation.

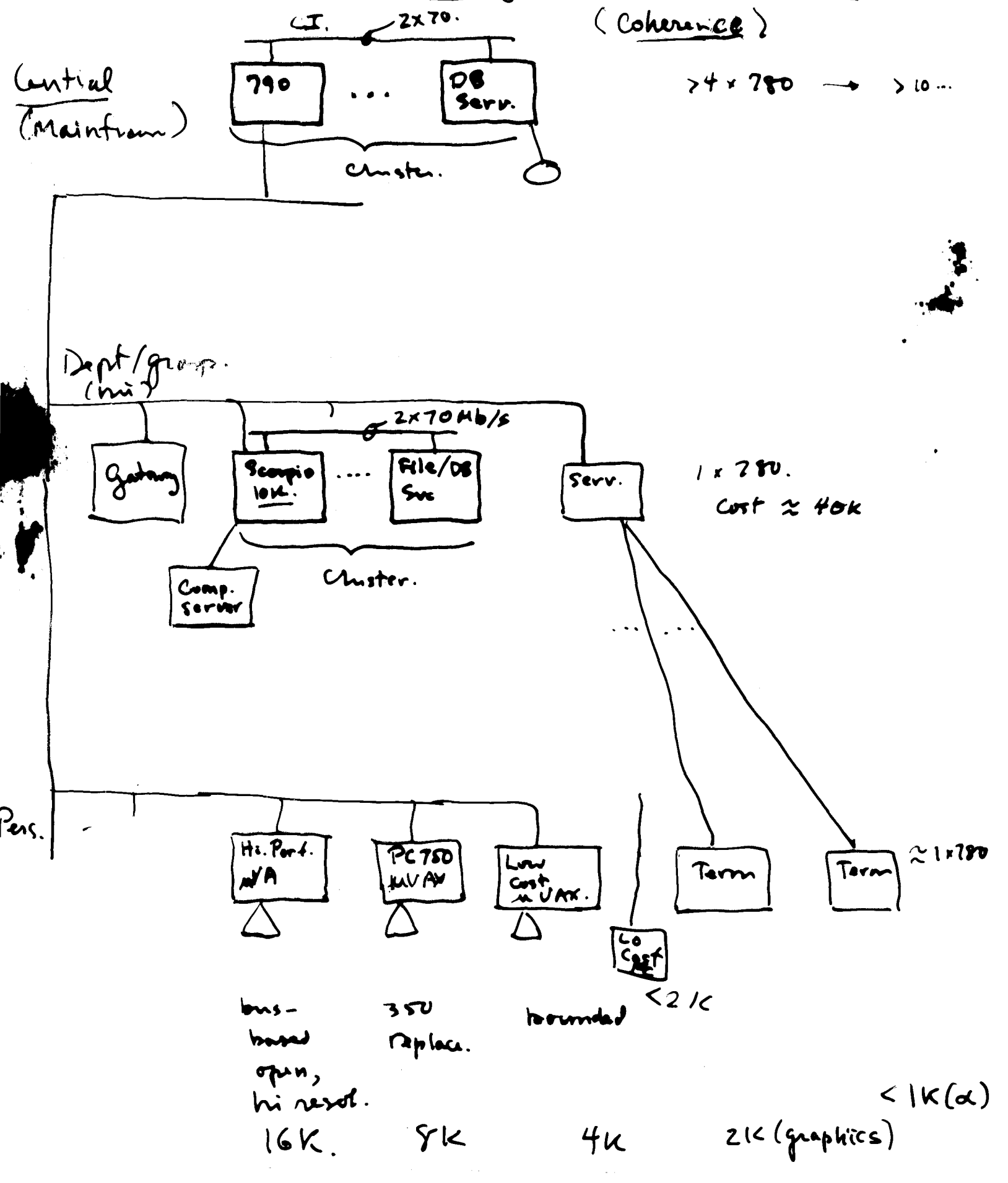
- standard
- passive.
- high speed.

- I/C Computers
- I/C Term.-to Computers
- Forms fully distributed Clusters.

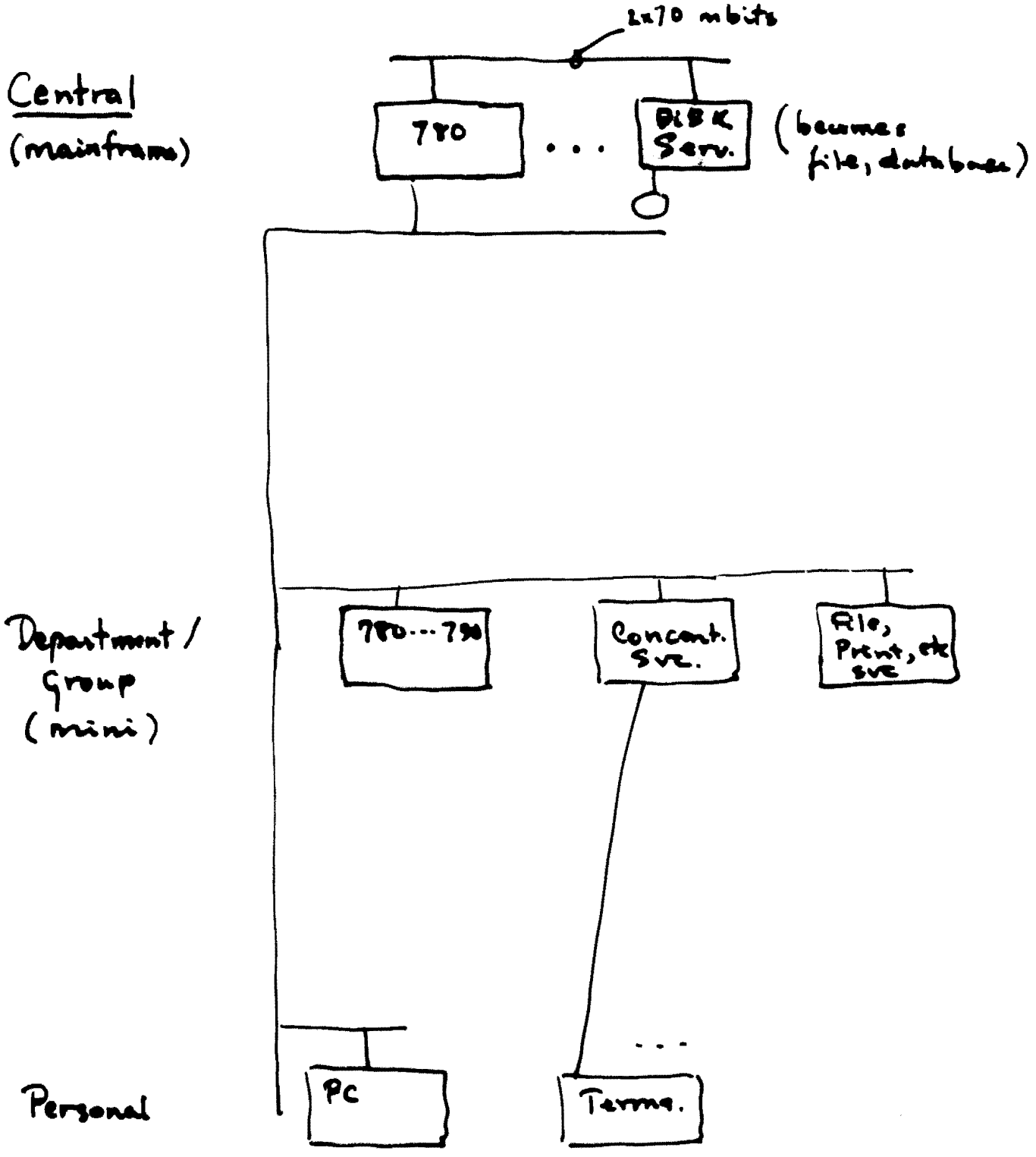
+2 yrs.

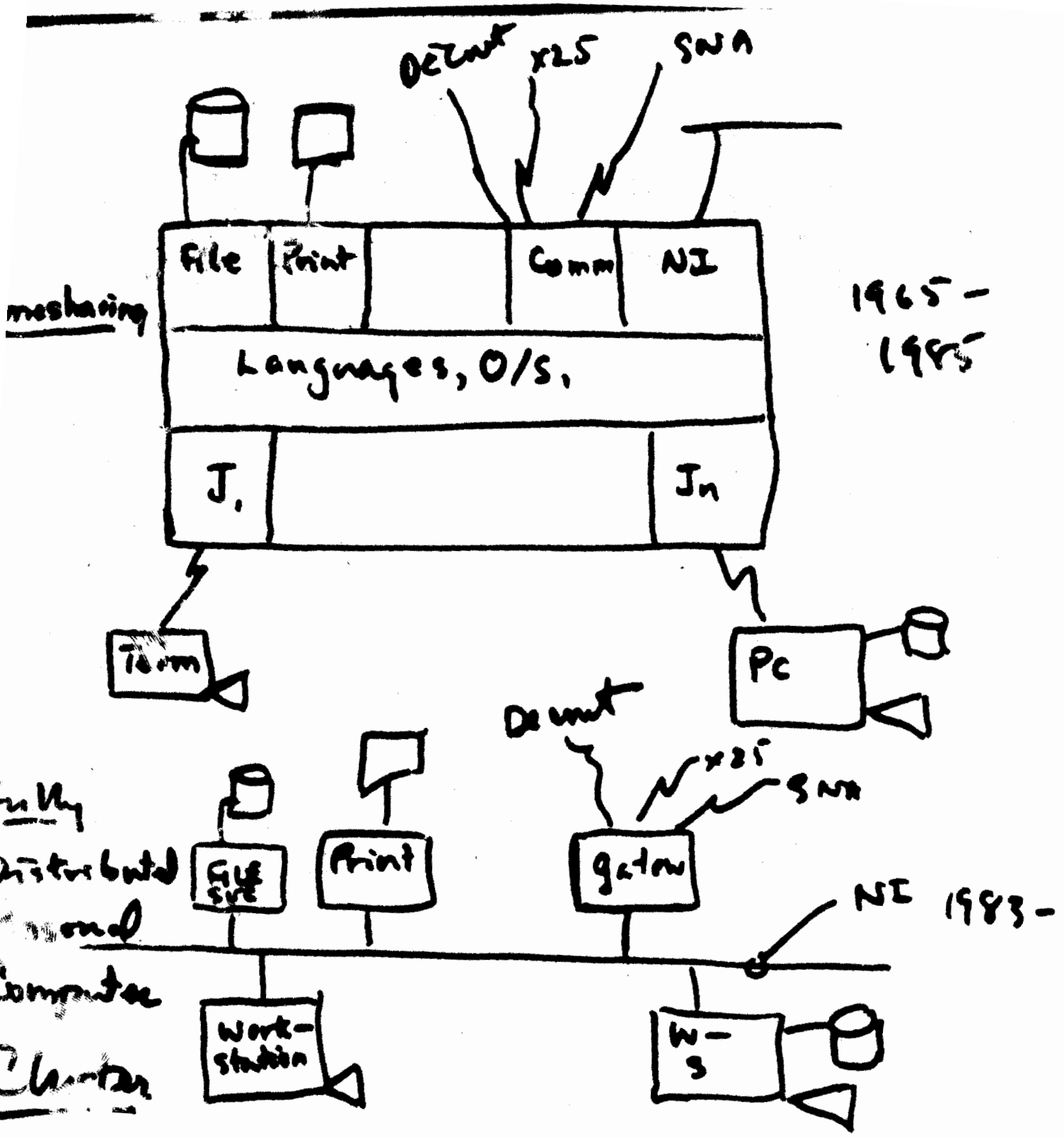
Homogeneous Architecture.

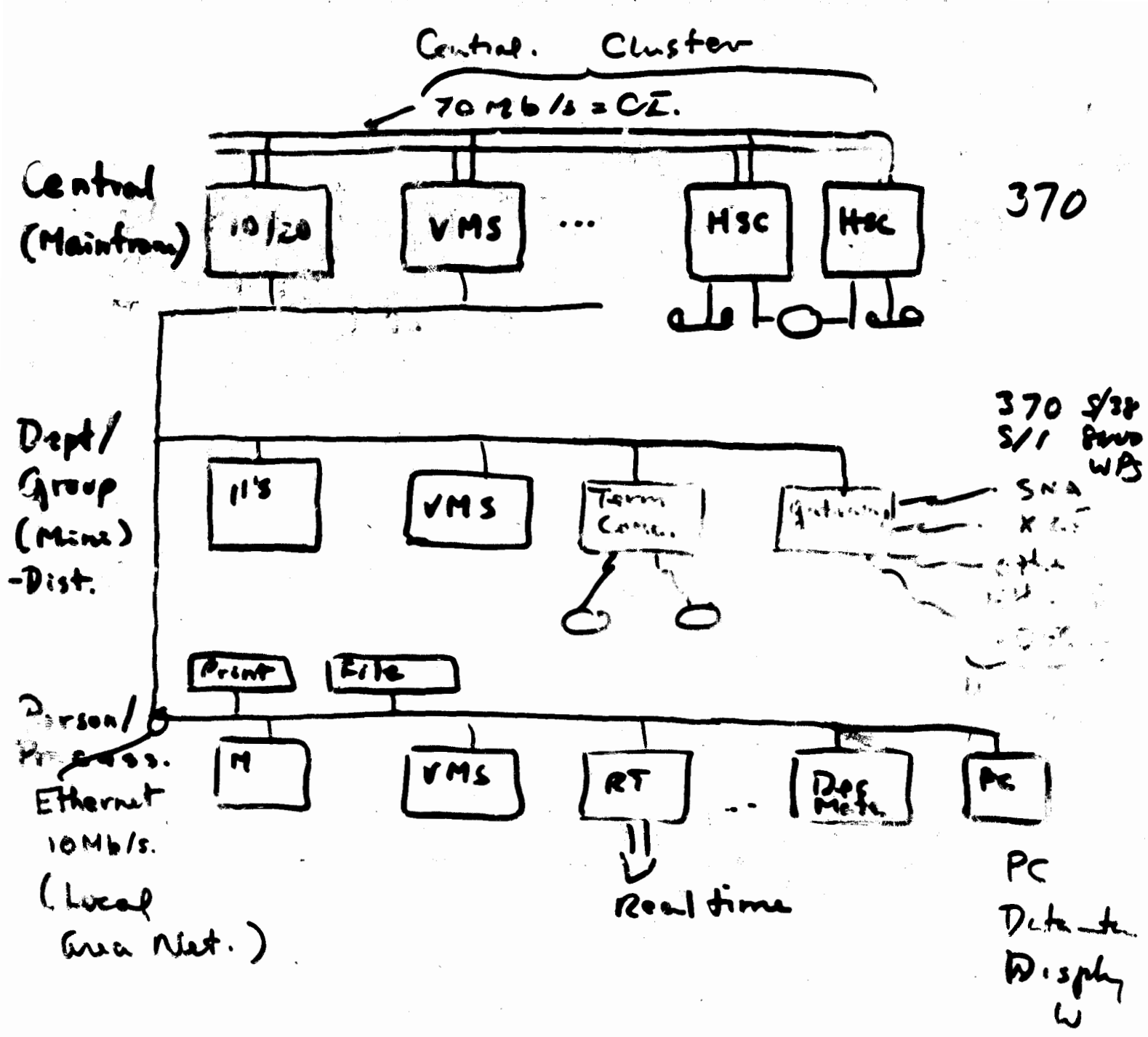
(Coherence)



now.


2x70 mbits
Central
(mainframe)
780
...
BIBK Serv.
(beamer file, database)
Department / Group (mini)
780 ... 790
Concent. Svr.
File, Print, etc svr
Personal
PC
Terms.
...


DECnet
X25
SNA
File
Print
Comm
NI
Languages, O/S,
J1
Jn
Term
Pc
1965-
1985
Decnet
X25
SNA
File Sys
Print
gatew
NI
1983-
Work-station
W-S

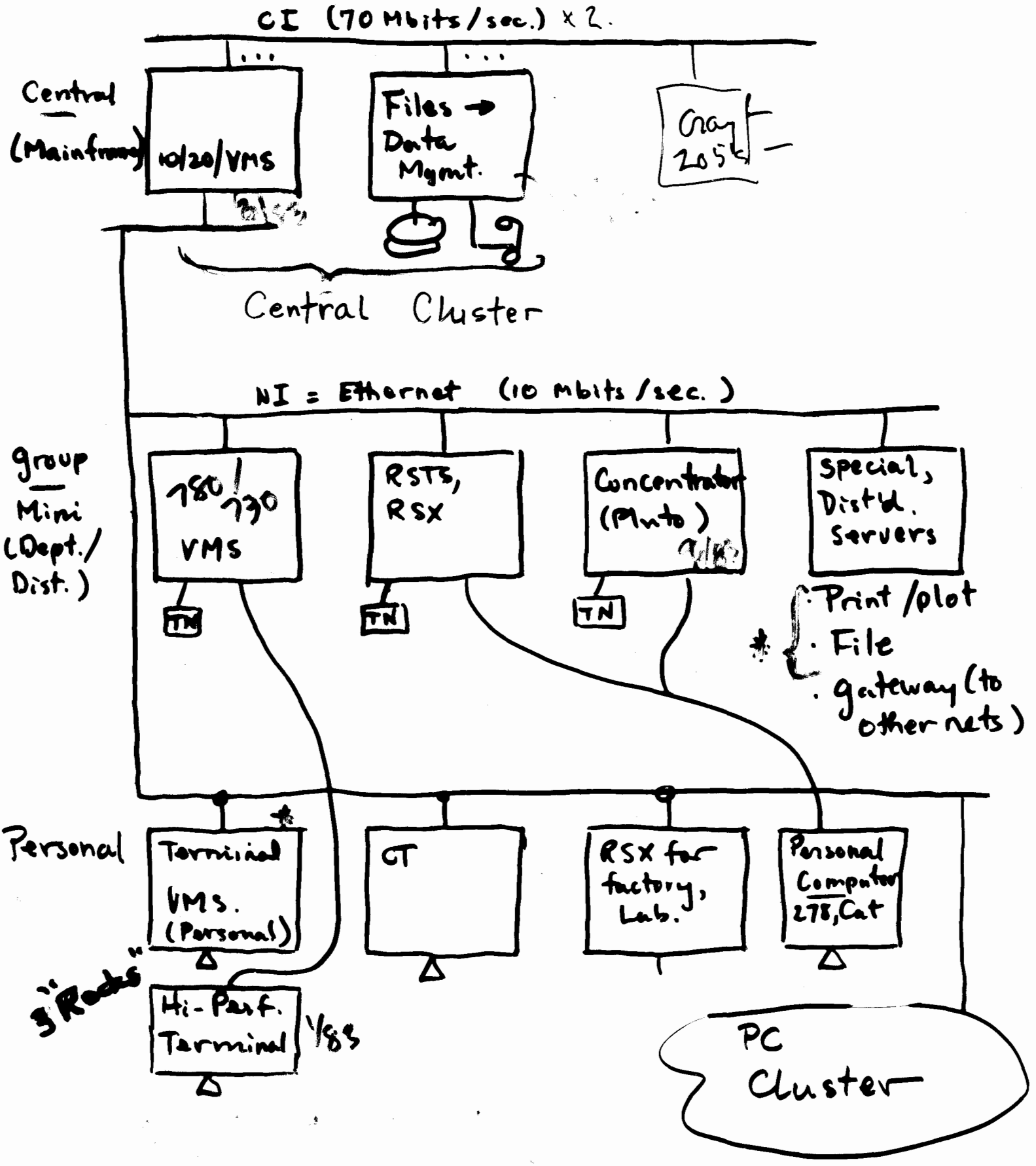

Central. Cluster
70 Mb/s = CI.
Central (Mainframe)
10/20
VMS
...
HSC
HSC
370
370 S/32 S/1 Apollo WS
Dept/ Group (Mini) -Dist.
11's
VMS
Term Conn.
SNA
X.25
Print
File
Person/ Process.
M
VMS
RT
Dec Mate
PC
Ethernet 10Mb/s. (Local Area Net.)
Real time
PC Data-to Display

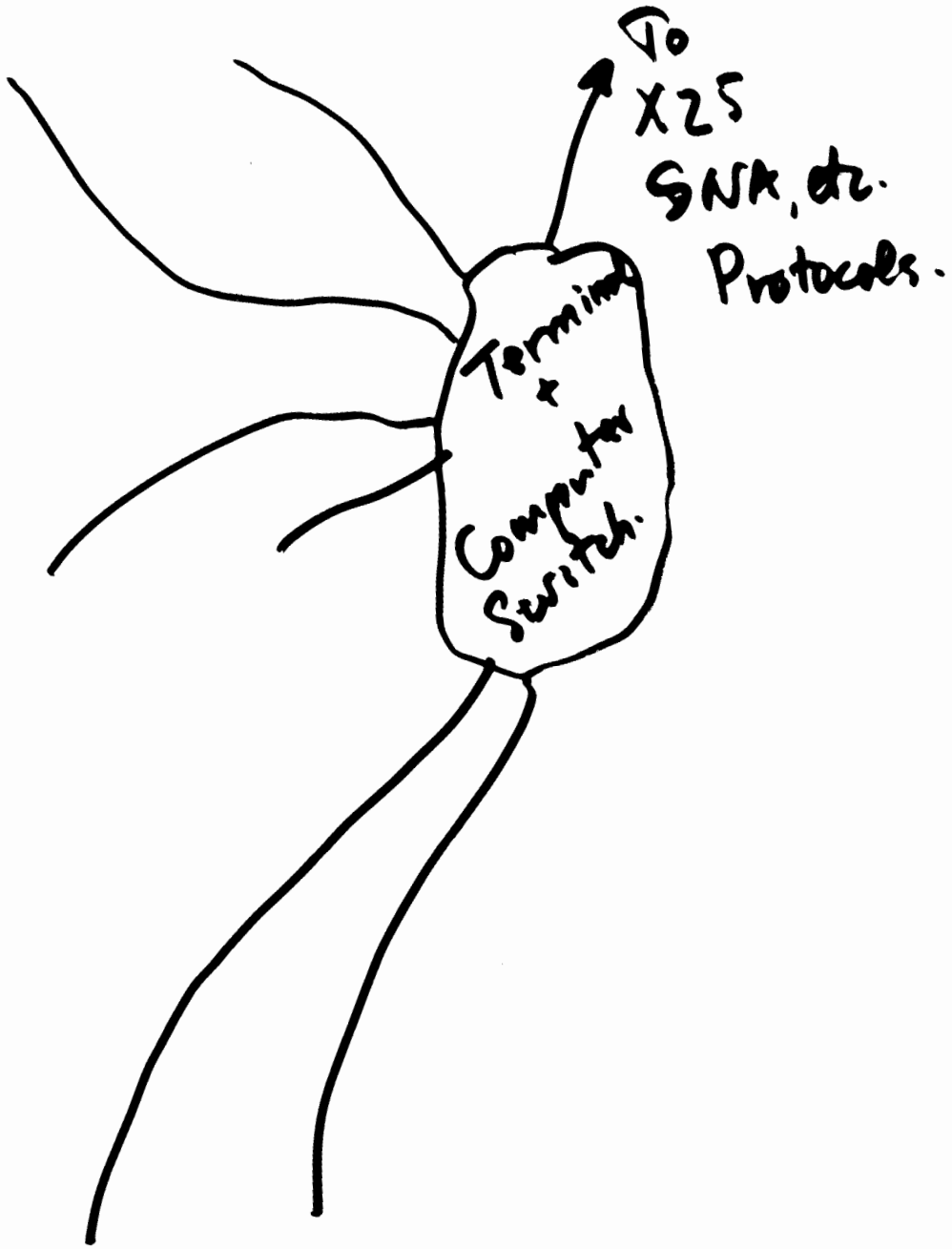
DEC'S PRODUCT STRATEGY

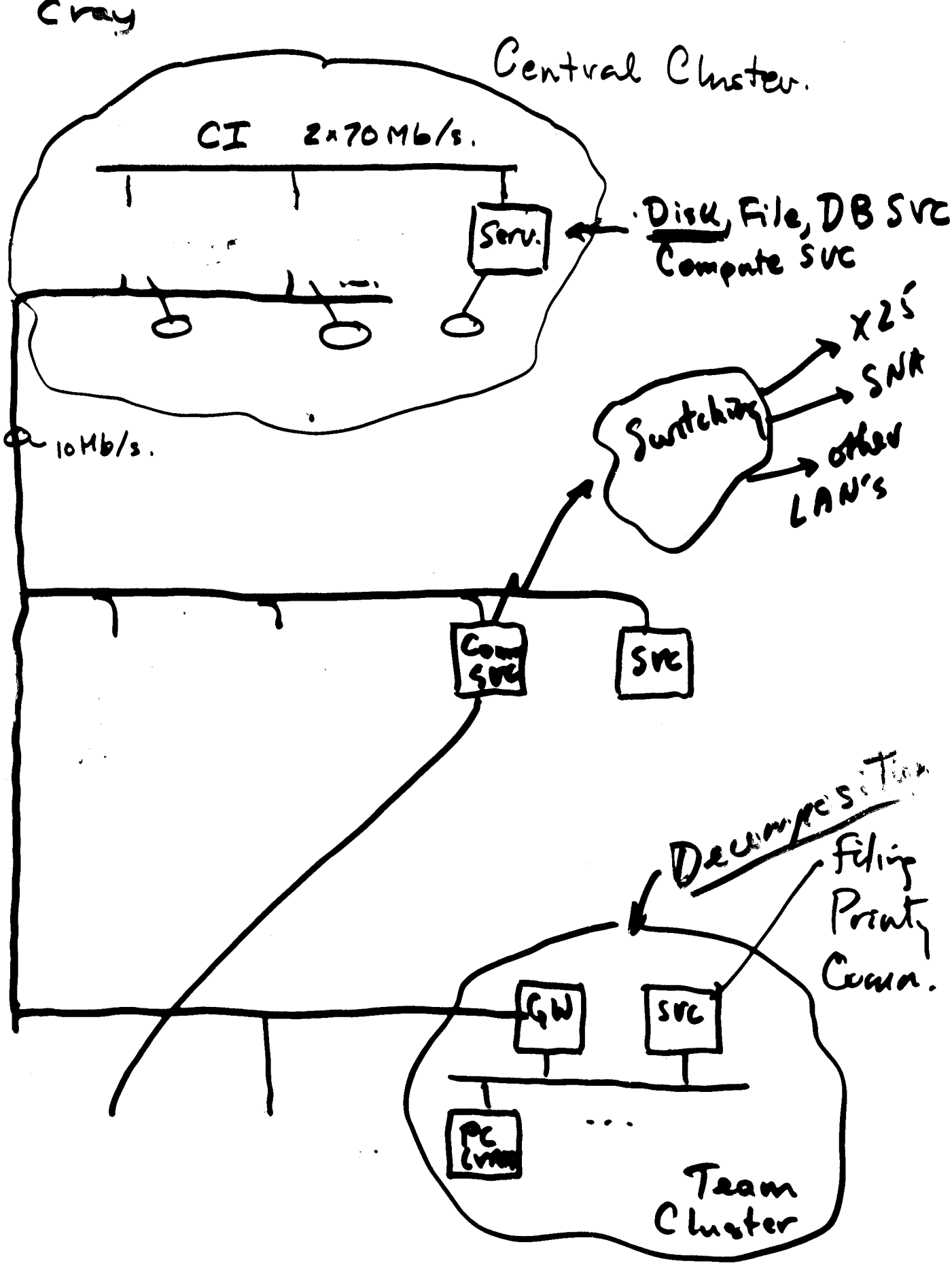
PROVIDE A SET OF HOMOGENEOUS DISTRIBUTED COMPUTING SYSTEM PRODUCTS SO A USER CAN INTERFACE, STORE INFORMATION AND COMPUTE, WITHOUT RE-PROGRAMMING OR EXTRA WORK FOR THE FOLLOWING COMPUTER SYSTEM SIZES AND STYLES:

- AS A SINGLE USER, PERSONAL COMPUTER WITHIN A TERMINAL, AND EVOLVING TO PC CLUSTERS AND PC NETWORKS;
- AT A SMALL, LOCAL SHARED, DEPARTMENTAL COMPUTER SYSTEM, AND
- VIA A CLUSTER OF LARGE CENTRAL COMPUTERS
- WITH INTERFACING TO OTHER SYSTEMS FOR REAL TIME PROCESSING; AND
- ALL INTERCONNECTED VIA ETHERNET AND WIDE AREA NETWORKS

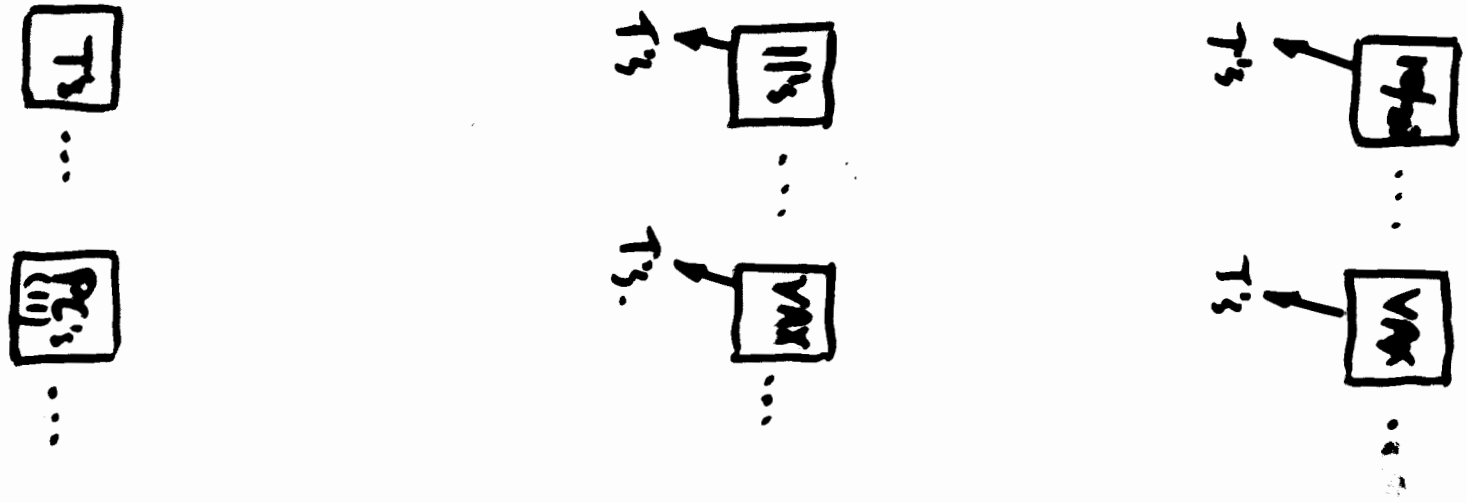
1984 Distributed Computing 3/82




To
X25
SNA, etc.
Protocols.
Terminal
+
Computer
Switch.


Cray
Central Cluster.
CI 2×70 Mb/s.
Serv.
Disk, File, DB SVC
Compute SVC
X25
SNA
other LAN's
Switching
10Mb/s.
Com SVC
SVC
Decompression
Filing
Print
Comm.
GW
SVC
PC LAN
...
Team Cluster

Person Team/group/Dept Central Regi



What functions:

1. Obvious — storage filing, archiving, fast access — Database

Communication

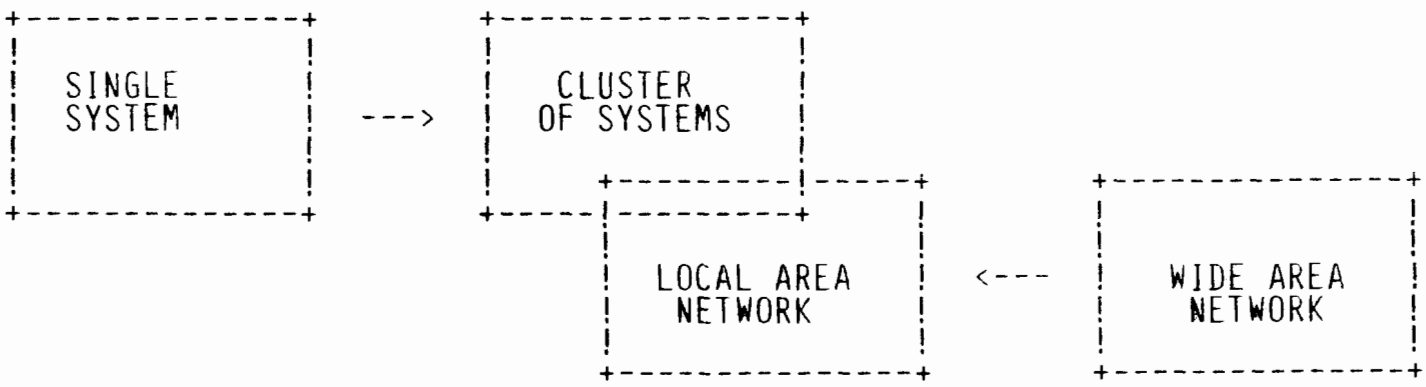
- all the protocols.
  all the networks — ARPA
  Csnet
  mail systems
  local processing — mainframes.

- Processing
  special purpose

- T.X

- T. human
  - print/plot
  - ~~et~~ visual
  - voice

DEFINITIONS



CLUSTER:

- AGGREGATE OF HOMOGENEOUS SYSTEMS (EXAMPLES : VMS CLUSTER TOPS20 CLUSTER , P/OS CLUSTER).
- HIGH SPEED INTERCONNECT. HIGH CONNECTIVITY. SYSTEMS WITHIN MACHINE ROOM OR OFFICE AREA.
- EXTENSION OF LOW-LEVEL 'OS SERVICES' ACROSS SYSTEMS VIA SCA-BASED PROTOCOLS. IN PARTICULAR A COMMON FILE SYSTEM.

LAN:

- AGGREGATE OF HETEROGENEOUS SYSTEMS (EXAMPLES : CT-VAX LAN, CT-20 LAN).
- HIGH SPEED INTERCONNECT. HIGH CONNECTIVITY. SYSTEMS WITHIN OFFICE AREA OR BUILDING.
- HIGH-LEVEL DNA-BASED SERVICES (I.E., SERVERS) VIA APPLICATION LEVEL PROTOCOLS.

WAN:

- INTERCONNECTED HETEROGENEOUS SYSTEMS AND HETEROGENEOUS NETWORKS.
- LOWER SPEED INTERCONNECT. LOWER CONNECTIVITY. WIDE GEOGRAPHICAL DISPERSION.
- COMMUNICATION SERVICES BETWEEN AUTONOMOUS SYSTEMS VIA DNA AND WITH OTHER NETWORKS VIA X.25/SNA/ETC. GATEWAYS.

PROBLEM STATEMENT

1. NO ONE OWNS THE PROBLEM OF INTEROPERABILITY OF CT's , VAX's AND 20's. SPECIFICALLY:

   - "CT - VAX" LOCAL AREA NETWORK
   - "VAX WORKSTATION - VAX" LOCAL AREA NETWORK
   - "CT - 20" LOCAL AREA NETWORK

2. LACK OF PRODUCT ORIENTED THINKING IN THE LOCAL AREA NETWORK SPACE.

   THERE IS MORE TO LOCAL AREA NETWORKS THAN THE NI AND DECNET-IV.

3. CLUSTER PRODUCTS (E.G., VMS , TOPS20 , P/OS) - RESPONSIBILTY OF INDIVIDUAL OPERATING SYSTEM GROUPS.

   WAN PRODUCTS (E.G., DECNET , GATEWAYS) - RESPONSIBILITY OF THE DISTRIBUTED SYSTEMS GROUP.

   LAN PRODUCTS (E.G., P/OS-VMS , WS-VMS) - NO ONE HAS PRODUCT OWNERSHIP.

PROPOSED SOLUTION

1. ORGANIZATIONAL RECOMMENDATION

   - CREATE A "LAN PRODUCTS GROUP" WITH PRODUCT OWNERSHIP & PRODUCT MARKETING RESPONSIBILITY FOR DISTRIBUTED SYSTEMS AND LOCAL AREA NETWORK PRODUCTS.

   - THIS GROUP SHOULD BE PART OF THE DISTRBUTED SYSTEMS ORGANIZATION UNDER BERNIE LACROUTE.

   - THIS GROUP WILL INCLUDE SOME PEOPLE CURRENTLY IN THE WORKSTATION ADVANCED DEVELOPMENT GROUP (AL LOPEZ) AND THE DISTRIBUTED COMPUTING GROUP (FRED ENGEL) BOTH UNDER RON CRISS.

   - THE PEOPLE CURRENTLY WORKING ON THE WORKSTATION TERMINAL SOFTWARE, SYSTEMS DISPLAY ARCHITECTURE, AND HUMAN FACTORS SHOULD BECOME PART OF BILL KEATING'S TERMINAL SW GROUP.

2. INITIAL ORIENTATION OF GROUP SHOULD BE TOWARDS SHORT-TERM PRODUCTS. WE HAVE THE COMPONENTS BUT NO LOCAL AREA NETWORK PRODUCT.

3. INITIAL PRODUCT FOCUS OF THIS GROUP (IN PRIORITY ORDER) :

- CT-VAX LAN
- WS-VAX LAN

4. FUNCTIONALITY FOCUS WITHIN ABOVE PRODUCT SPACES.

HIGH PRIORITY :

- PRINT SERVER
- SECURITY (AUTHENTICATION/AUTHORIZATION/ACCESS CONTROL)
- SYSTEM MANAGEMENT IN DISTRIBUTED ENVIRONMENT

LOWER PRIORITY :

- NAMING
- FILE SERVER
- MESSAGE TRANSPORT
- REMOTE PROCEDURE CALL

OPEN ISSUES

1. NO AGREEMENT ON A COMMON SESSION LAYER INTERFACE TO SCA AND DNA (ACROSS ALL SYSTEMS AND INTERCONNECTS).

2. NO PLANS FOR VMS AND TOPS20 CLUSTERS TO SHARE CI AND HSCs.

3. THE "LOCAL AREA TERMINAL (LAT)" PROTOCOL PROVIDES A CHEAP AND EFFECTIVE MEANS OF CONNECTING TERMINALS TO HOSTS.

   NO CLEAR PRODUCT PLANS FOR THE PLUTO JR. BASED LAT CONCENTRATOR.

4. FORSEE SIGNIFICANT OVERLAP AMONG CT-16 , CT-32 AND VAX WORKSTATION IN FY84-85 TIMEFRAME.

   PRODUCT COMPATIBILITY AND ORGANIZATIONAL CHARTER ISSUES NOT BEING ADDRESSED.

To: Bruce Stewart, Bob Travis, Gilmore, Lyle, Dickson
BJ, Daley, Buzz Brooks, Vlach, D. Stannard
+ Lee

Slides of MK Talk on □A/OOF/
WPS/LEMS

5/23/80
GBell

A PROFESSION BASED SYSTEM

(FOR LARGE ORGANIZATIONS)

- IS A HIERARCHY OF COMPUTERS (INCLUDING PERSONALS?)

- PROVIDES BENEFIT NOW THROUGH GENERIC CAPABILITIES FOR TEXT, FILING AND COMMUNICATIONS

- REQUIRES ATTENTION TO HUMAN ENGINEERING, AND COST OF CAPABILITY (INCLUDING OWNERSHIP)

OFFICE OF FUTURE (OOF)

USE OF EQUIPMENT WHICH ALLOW A DRASTIC RESTRUCTURING OF OFFICE WORK, AMONG A DIFFERENT COMPOSITE WORK FORCE.

PARAPHRASING THE APRIL 80 COOPERS AND LYBRAND NEWSLETTER: "A SECRETARY USES THE EQUIPMENT, IT'S OA; AND IF WE ALL USE IT, IT'S OOF".

OFFICE AUTOMATION - OA - EVOLUTIONARY USE OF WORD PROCESSING AND ELECTRONIC MAIL EQUIPMENT TO IMPROVE OFFICE PRODUCTIVITY, WHERE:

1. WORD PROCESSING EQUIPMENT, EVOLVING TO USER TYPESETTING REPLACES, TYPEWRITERS, SNOPAKE, AND COPIERS.

2. ELECTRONIC MAIL REPLACES COPIERS AND POST PEOPLE, FAX, TWX/TELEX AND INTRA-ORGANIZATION ELECTRONIC TORN TAPE MESSAGE SWITCHES.

3. COMMON CARRIER PACKETNETS EVOLVE FOR INTER-ORGANIZATIONAL MESSAGE AND DATA SWITCHING.

4. ELECTRONIC FILING REPLACES PAPER FILES.

5. DIRECT SOURCE FORMS ENTRY AND TRANSMISSION REPLACES MODERN KEYPUNCH.

6. LOCALIZED LIST PROCESSING FOR REPORTS REPLACES CENTRAL, DATA PROCESSING.

FUNCTIONAL LEVELS OF A PBS ROOT (HARDWARE, OS, LANGUAGES, NETWORKING AND DATA BASES)

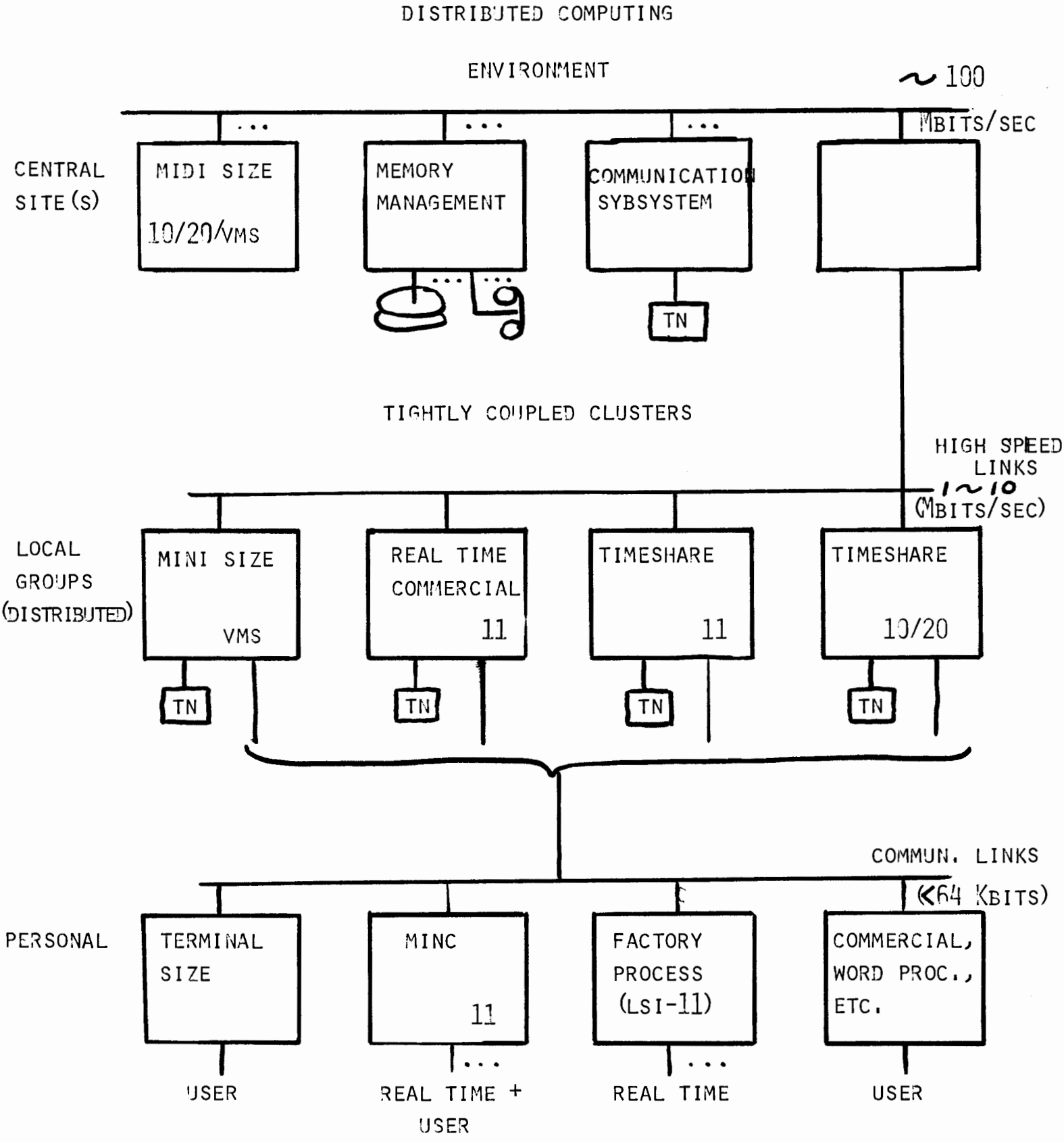
GENERIC MODULES FOR COMMUNICATIONS WITHIN AN ORGANIZATION

- TEXT AND GRAPHICS PROCESSING AND "USER TYPESETTING"
- FILING CABINETS FOR TEXT, MESSAGES, FORMS, ETC.
- ELECTRONIC MAIL AND COMPUTER CONFERENCING
- OFFICE PROCEDURES AND FORMS PROCESSING
- INTERFACE TO NON-COMPUTER COMMUNICATIONS (FAX, OCR, INTERFACE TO OTHER ORGANIZATIONS, TWX, TYPESETTERS, TELEPHONE)

GENERAL PROFESSIONAL DISCIPLINE MODULES (E.G. ENG.)

DEPARTMENTAL PROFESSIONAL DISCIPLINE (E.G. ELEC. ENG.)

COMPARTMENTAL PROFESSIONAL DISCIPLINE (E.G. RF CKT. DESIGN)



TN = TERMINAL NETWORK--CONNECTS SIMPLE TERMINALS, GATEWAY TO OTHER NETWORKS, MOST PERIPHERALS, AND PERSONAL COMPUTERS, AND PROCESS COMPUTERS

LARGE, CENTRALLY OPERATED FACILITIES PROVIDE:

LARGE, SHARED DATA BASES AT LOWEST COST/BYTE (THROUGH ECONOMY OF SCALE OF LARGE DISKS)

ARCHIVAL OF PERSONAL FILES

PROGRAMS FOR SPECIAL NON-COMPUTER OWNER COMMUNITIES

VERY HIGH PERFORMANCE PROCESSING

COMMUNICATIONS AMONG THE ENTIRE COMMUNITY AND GATEWAYS TO INTERNETS AND PACKETNETS

COMMUNICATIONS ORIENTED SERVICES (E.G. MAIL, TELECONFERENCING)?

SPECIAL FACILITIES SUCH AS TYPESETTING

GROUP CENTERED COMPUTERS PROVIDE:

RELATIVELY COST-EFFECTIVE FILE STORAGE FOR ITS COMMUNITY

FACILITIES BEST MATCHED TO COMMUNITY

RELATIVELY HIGH PERFORMANCE PROCESSING

COST-EFFECTIVENESS THROUGH GROUP SUPPORTED PROGRAMS

PERSONAL COMPUTERS PROVIDE:

PERSONAL DATA BASES AND SECURITY

FAST RESPONSE TO RELATIVELY COMPLEX REQUESTS (E.G. EDITING)

PROGRAM ENVIRONMENT FOR ENTERING AND GETTING INTO PRODUCTION

USER VIEW GOALS

LIVE AND WORK ON THE MACHINE

CONSISTENCY AND COMPATIBILITY ACROSS KEYBOARDS, SYNTAX/SEMANTICS, FILES, COMMUNICATIONS...PERMITTING TRUE DP HOMOGENETS AND HETEROGENETS

"CAMERA INSTRUCTION BOOK-LIKE" MANUALS PERSONALIZABLE WITHOUT PROGRAMMING CONTEXT DEPENDENT EDITING FOR TEST, TYPESETTING, MAIL, FILE CABINET, PICTURES FORMS, TABLES, ETC.

IMPLEMENTATION DESIGN GOALS

NO ASSEMBLY LANGUAGE PROGRAMMING

CONSISTENCY AND COMPATIBILITY FOR FORMING DP HOMOGENETS AND HETEROGENETS

ALL PROGRAMS DRIVEN FROM: FILES, TERMINALS, TEXT, ANY OTHER PROGRAM USING VARIOUS PROGRAM MODELS (TP, PIPES, SINGLE PROCESS, AND NETWORK)

BUILT IN FOREIGN LANGUAGES

TYPED DATA FOR FILES, FORMS AND PROGRAMS

COST OF CAPABILITY UNDERSTANDING

PERSONAL OR SHARED?

GIVEN: ECONOMY OF SCALE, EXCEPT DISKS AND SWITCHING DISAPPEARING. ALL MEMBERS OF HIERARCHY ARE NEEDED.

STRATEGY: MOVE FROM GENERAL TO SPECIFIC AND PERSONAL

PROBLEMS: DISTRIBUTING AND SHARING PROGRAMS, PROGRAMMING AND DATA. USING.

PBS (1985) GENERIC CAPABILITIES:

WPS: FULL PAGE, VOICE INPUT, GRAPHICS, PROFESSION DEPENDENT. ARCHIVES ANY PART AND ALL DOCUMENTS.

USER-TYPESETTING: YES

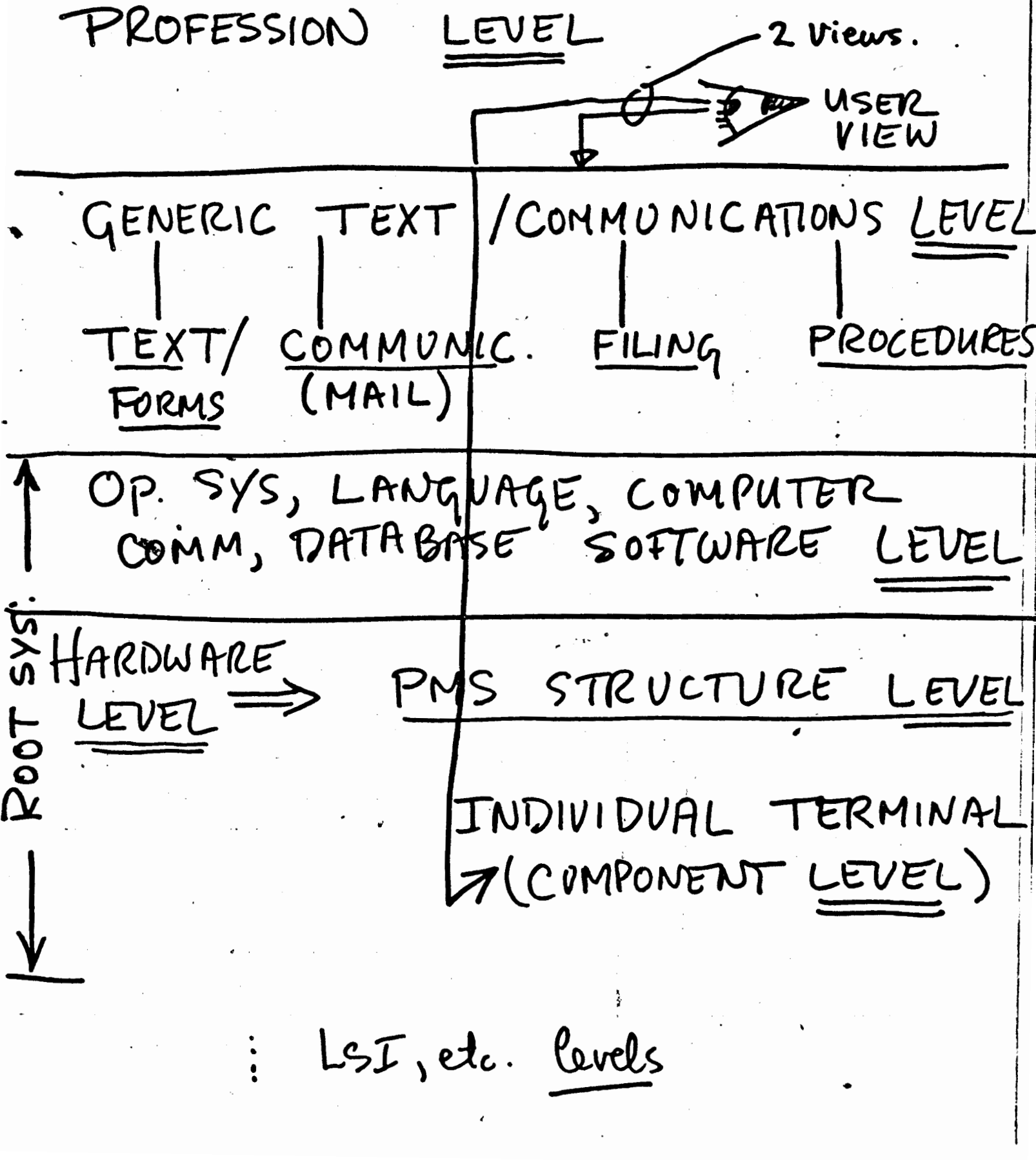
FILE CABINET: RETRIEVE BY MULTIPLE KEYWORD. SEARCH FOR CONTENT.

MAIL SYSTEMS: VOICE. COMPUTER CONFERENCING WITH PERSONAL VIDEO CONFERENCING IN SIGHT.

COMMUNICATIONS: INTERNETS, PACKETNETS, AND NON-COMPUTER NETS (E.G. PHONE, FAX, TWX, OCR FOR OLD DOCUMENTS).

OFFICE PROCEDURES: NUMEROUS

OA - SUBSET OF A PROFESSION - BASED SYSTEM



PHYSICAL STRUCTURE PARAMETERS

- COST (PURCHASABILITY, MAINT., ETC.), PERFORMANCE, RELIABILITY

- SECURITY, ATTITUDES ABOUT SHARING

- AESTHETICS/APPEARANCE

- ENVIRONMENTAL ADAPTABILITY

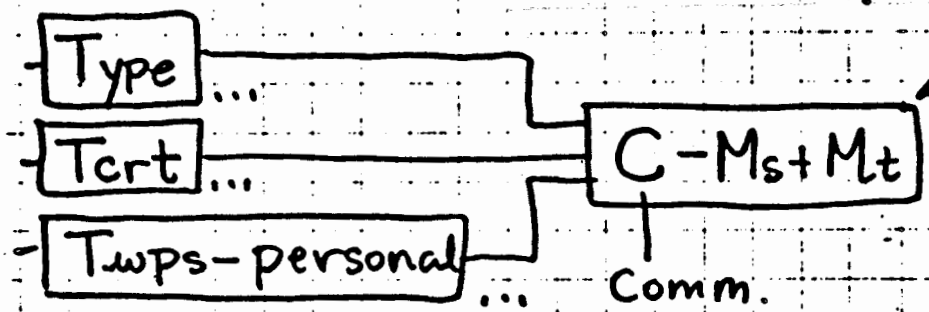
  (1). UNOBSTRUSIVE

  (2). DOMINATES & BECOMES (CREATES) THE ENVIR. (EG. WORK SPACE, NOISE, LIGHTING, FILING, DOCUMENTS, PHONE

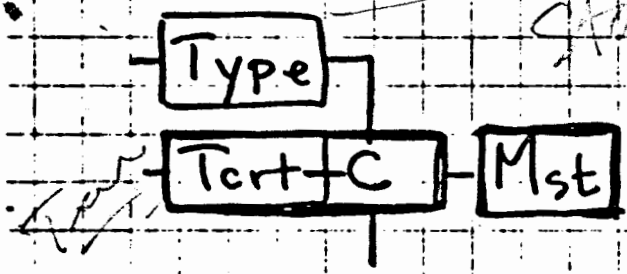
- COMMUNICATION WITH: OTHERS, OTHER WPS, DP,...

PHYSICAL STRUCTURES ALTERNATIVES

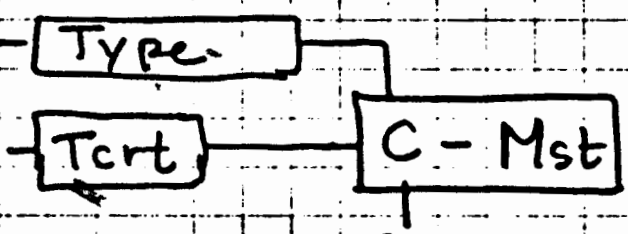
- SHARED: CENTRAL AND GROUP



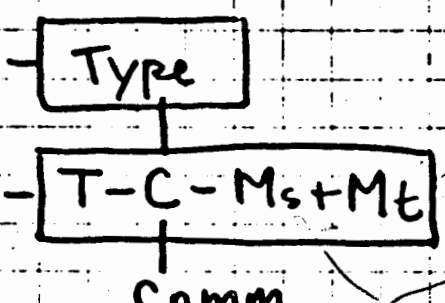
- PERSONAL:



IN DESK AND TERMINAL I.
(E.g. VT 78, 278)

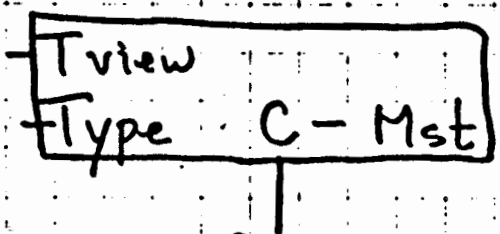


IN Mass. Storage II.
(PDT)



IN Terminal. III.

IN Typewriter IV.



5/20/80

PRIME OA 5/80

WP

TEXT CREATION & EDITING

FILING & RETRIEVAL

BOILERPLATE LIB.

LIST PROC.

ADV. FEATURES:
PROOFING, HYPHENATE, TRANSLATE

MGMT COMM. & SUPPORT

EMAIL
CREATE NOTES & MEMOS
DIST.
ANNOTATE
ACK. & SECURITY CODES

CORRESP. MGMT
FILE, RETRIEVE, ARCHIVE
FILE CODES & REPORTS

MGMT SUPPORT
INTRAY, CALENDAR, SCHEDULING, TICKLER FILE, TELEPHONE LOG

MGMT INFO.
QUERIES, REPORTS, MODELLING, APPL.

COMPATIBILITY

EDITING SYNTAX

- WPS, EMS, FORMS TEXT, COMMANDS, USER TYPESET

FILES

- PERSONAL & SHARED WPS
- EMS
- INTERFACE TO DATA IN SYSTEM W/O CONVERSION (I.E. PROGRAMS)

COMMUNICATIONS

- DECNET ETC. VIA SYSTEM CALLS

PERFORMANCE/USE UNDERSTANDING

1981 GOALS

GENERIC LEVEL TEXT/COMMUNICATIONS PRODUCT INTRODUCTION

- PLAN, SPECIFY, DESIGN AND UNDERSTAND (I.E. MASTER) THIS LEVEL FOR NEXT 5 YEARS → ADDRESS PRODUCTIVITY (COST TO USE)
- DECNET COMMUNICATIONS WITH VIRTUAL TERMINALS AND COMMON PROTOCOLS VIA STANDARD SYSTEMS
- HIGH QUALITY, COMPATIBLE WPS BASE
  - STABILIZE THE 2XX MULTI-USER SYSTEM?
  - BUILD A FIRM BASE FOR 278 AND ENHANCE IT
  - BUILD A MULTI-USER BASE ON WPS COMPATIBLE EDT FOR RSTS AND VMS
  - BUILD A SINGLE USER 11 SYSTEM ON SAME EDITOR
  - LIST PROCESSING, SORT AND MATH.
  - GRAPHICS (PROTO)
  - DICTIONARY AND SPELLING (PROTO)

(WPS FILING ON ALL SYSTEMS)
(WPS COMM. " " ")

GB1.S4.13
5/23/80

- USER TYPESETTING BREADBOARD
- USER FORMS CREATION AND EDITING (VS LISTS?)
- FILING
  - PUT DOCUMENT HOLDER FOR 278 ON 11/M, RSTS AND VMS
  - MAIL
  - BASE FOR FORMS HOLDER
  - RELATIONAL
- QUERY BY FORMS (PROTO) USING CATS AND FORMS EDITOR
- VOICE MESSAGE STORAGE (PROTO)
- ELECTRONIC MAIL (EMS' COMPATIBLE WITH WPS) - TEST AT DEC
  - VMS (AND POSSIBLY RSTS)
  - VOICE READ MAIL (PROTO)
  - FORMS SIGNATURE ROUTING AND APPROVAL (PROTO)
- OFFICE PROCEDURES (PROTO)
  - TICKLER, SCHEDULING, PHONE MANAGEMENT

A PROFESSION BASED SYSTEM
(FOR LARGE ORGANIZATIONS)

- IS A HIERARCHY OF COMPUTERS (INCLUDING PERSONALS?)

- PROVIDES BENEFIT NOW THROUGH GENERIC CAPABILITIES FOR TEXT, FILING AND COMMUNICATIONS

- REQUIRES ATTENTION TO HUMAN ENGINEERING, AND COST OF CAPABILITY (INCLUDING OWNERSHIP)

OFFICE AUTOMATION - OA - EVOLUTIONARY USE OF WORD PROCESSING AND ELECTRONIC MAIL EQUIPMENT TO IMPROVE OFFICE PRODUCTIVITY, WHERE:

1. WORD PROCESSING EQUIPMENT, EVOLVING TO USER TYPESETTING REPLACES, TYPEWRITERS, SNOPAKE, AND COPIERS.

2. ELECTRONIC MAIL REPLACES COPIERS AND POST PEOPLE, FAX, TWX/TELEX AND INTRA-ORGANIZATION ELECTRONIC TORN TAPE MESSAGE SWITCHES.

3. COMMON CARRIER PACKETNETS EVOLVE FOR INTER-ORGANIZATIONAL MESSAGE AND DATA SWITCHING.

4. ELECTRONIC FILING REPLACES PAPER FILES.

5. DIRECT SOURCE FORMS ENTRY AND TRANSMISSION REPLACES MODERN KEYPUNCH.

6. LOCALIZED LIST PROCESSING FOR REPORTS REPLACES CENTRAL, DATA PROCESSING.

DISTRIBUTED PROCESSING MATCHES COMPUTER SYSTEMS TO NEEDS ON A GEOGRAPHICAL OR ORGANIZATIONAL BASIS, AND INTERCONNECTS INDIVIDUAL COMPUTER SYSTEMS INTO A SINGLE NETWORK.

THE OBJECTIVES OF DISTRIBUTED PROCESSING ARE:

1. TO ALLOW EFFECTIVE MATCHING OF RESOURCES TO NEEDS.

2. TO ALLOW BOTH LOCAL AUTONOMY AND CENTRAL CONTROL OF THE VARIOUS DISTRIBUTED PARTS.

3. TO PROVIDE AN EVOLVING, OPEN ENDED SYSTEM SO THAT THE DEVELOPMENT OF DISTRIBUTED PARTS CAN PROCEED AT THEIR OWN PACE IN A QUASI INDEPENDENT FASHION.

4. TO ALLOW PURCHASE AND INSTALLATION OF COMPUTER IN THE MOST TIMELY, COST-EFFECTIVE WAY, TAKING ADVANTAGE OF REDUCED (WITH TIME) HARDWARE COSTS.

5. TO BUILD ON AND COMMUNICATE WITH EXISTING, MORE CENTRAL SYSTEMS, FULLY DISPERSED SYSTEMS, AND EMERGING PERSONAL COMPUTERS.

6. TO PROVIDE COMPUTING, CONTROL AND STORAGE OF INFORMATION NEAREST THE NEED.

DISTRIBUTED PROCESSING IS THE MATCHING OF COMPUTER RESOURCES TO NEEDS- ON A GEOGRAPHICAL OR ORGANIZATIONAL BASIS - AND THE INTERCONNECTION OF THESE RESOURCES TO FORM A SINGLE, COST-EFFECTIVE SYSTEM.

THE OBJECTIVES OF THIS STRATEGY FOR BUYING AND USING COMPUTERS ARE TO REDUCE DATA PROCESSING COSTS, INCREASE PRODUCTIVITY AND IMPROVE ORGANIZATIONAL EFFICIENCY.

TACTICALLY, DISTRIBUTED PROCESSING MAKES IT POSSIBLE TO:

- CONTROL COSTS BY MATCHING COMPUTER PROCUREMENT TO ACTUAL NEEDS.

- DECOUPLE OR CENTRALIZE SYSTEM DEVELOPMENT.

- CENTRALIZE OR DECENTRALIZE ADMINISTRATIVE CONTROLS.

- MATCH PROCESSING CAPABILITIES, CONTROL AND STORAGE OF INFORMATION ON THE MOST COST-EFFECTIVE BASIS.

- COMMUNICATION WITH THE EXISTING CENTRALIZED SYSTEMS, WITH FULLY DISPERSED SYSTEMS, AND WITH COMPUTER WORK-STATIONS AND PERSONAL COMPUTERS AS THEY EMERGE AT EVERY LEVEL OF THE ORGANIZATION.

- MANAGE OPEN-ENDED GROWTH.

FUNCTIONAL LEVELS OF A PBS ROOT (HARDWARE, OS, LANGUAGES, NETWORKING AND DATA BASES)

GENERIC MODULES FOR COMMUNICATIONS WITHIN AN ORGANIZATION

- TEXT AND GRAPHICS PROCESSING AND "USER TYPESETTING"
- FILING CABINETS FOR TEXT, MESSAGES, FORMS, ETC.
- ELECTRONIC MAIL AND COMPUTER CONFERENCING
- OFFICE PROCEDURES AND FORMS PROCESSING
- INTERFACE TO NON-COMPUTER COMMUNICATIONS (FAX, OCR, INTERFACE TO OTHER ORGANIZATIONS, TWX, TYPESETTERS, TELEPHONE)

GENERAL PROFESSIONAL DISCIPLINE MODULES (E.G. ENG.)

DEPARTMENTAL PROFESSIONAL DISCIPLINE (E.G. ELEC. ENG.)

COMPARTMENTAL PROFESSIONAL DISCIPLINE (E.G. RF CKT. DESIGN)

OFFICE OF FUTURE (OOF)

USE OF EQUIPMENT WHICH ALLOW A DRASTIC RESTRUCTURING OF OFFICE WORK, AMONG A DIFFERENT COMPOSITE WORK FORCE.

PARAPHRASING THE APRIL 80 COOPERS AND LYBRAND NEWSLETTER: "A SECRETARY USES THE EQUIPMENT, IT'S OA; AND IF WE ALL USE IT, IT'S OOF".

LARGE, CENTRALLY OPERATED FACILITIES PROVIDE:

LARGE, SHARED DATA BASES AT LOWEST COST/BYTE (THROUGH ECONOMY OF SCALE OF LARGE DISKS)

ARCHIVAL OF PERSONAL FILES

PROGRAMS FOR SPECIAL NON-COMPUTER OWNER COMMUNITIES

VERY HIGH PERFORMANCE PROCESSING

COMMUNICATIONS AMONG THE ENTIRE COMMUNITY AND GATEWAYS TO INTERNETS AND PACKETNETS

COMMUNICATIONS ORIENTED SERVICES (E.G. MAIL, TELECONFERENCING)?

SPECIAL FACILITIES SUCH AS TYPESETTING

GROUP CENTERED COMPUTERS PROVIDE:

RELATIVELY COST-EFFECTIVE FILE STORAGE FOR ITS COMMUNITY

FACILITIES BEST MATCHED TO COMMUNITY

RELATIVELY HIGH PERFORMANCE PROCESSING

COST-EFFECTIVENESS THROUGH GROUP SUPPORTED PROGRAMS

PERSONAL COMPUTERS PROVIDE:

PERSONAL DATA BASES AND SECURITY

FAST RESPONSE TO RELATIVELY COMPLEX REQUESTS (E.G. EDITING)

PROGRAM ENVIRONMENT FOR ENTERING AND GETTING INTO PRODUCTION

PHYSICAL SYSTEM

CLOSETABLE OR IN A DESK IF QUIET ENOUGH

Pc + Mp (1 Mbyte) + Ms (100 Mbyte; FIXED)...NOTE 1 FILE CABINET = 32 Mbytes

2 - 4 X T.CRT(1 PAGE B/W, OR COLOR)
WITH ABILITY TO REMOTE AT REDUCED BANDWIDTH

T(LETTER QUALITY AND SCREEN PRINTER)

T(TELEPHONE DIALER, PHONE ANSWERER, VOICE OUTPUT)

L(SYSTEMS OF THE SAME TYPE) FOR:
COMMUNICATION, EXECUTING OTHER PROGRAMS, TELE- AND COMPUTER-CONFERENCING, ETC.

L(CENTRAL SYSTEM) FOR:
- FILING, PRINTING, TYPESETTING, AND SLIDE MAKING
- DISTRIBUTION OF DOCUMENTS TO PEOPLE NOT ON SYSTEM
- ACCEPTANCE OF DOCUMENTS FROM PEOPLE NOT ON SYSTEM
- EMS'S, AND OTHER SYSTEMS

T(VIDEO AND VOICE I/O) - LARGE SCREEN FOR TELECONFERENCING)

STRUCTURE OF PROFESSION MODULES AND USE DEPENDENCIES

USE IS A FUNCTION OF THE PRODUCT OF:

PROFESSIONAL DISCIPLINE/PROJECT DISCIPLINE
ORGANIZATION (BUYER, SELLER, KNOWLEDGE SELLER, CONTROLLER/GOV'T)

PERSON'S ROLE:

MKT.-, MFG.- TECH- GATEKEEPER, IDEA GENERATOR/CREATIVE SCIENTIST, ENTREPENEUR, COACH/SPONSOR, PROBLEM SOLVER

(...NOTE VARYING DEGREE OF COMMUNICATION, ANALYSIS, NEED TO ACCESS AND PRESENT DATA IN EACH ROLE

POSITION IN ORGANIZATION HIERARCHY

TIME OF FISCAL YEAR AND OTHER PROCESSES (E.G. PLANNING)

TIME OF TRANSACTION (PROCESS STATE)

E.G. PROJECT (PROPOSAL, DESIGN, ANNOUNCEMENT, DEATH) ETC.

USER VIEW GOALS

LIVE AND WORK ON THE MACHINE

CONSISTENCY AND COMPATIBILITY ACROSS KEYBOARDS, SYNTAX/SEMANTICS, FILES, COMMUNICATIONS...PERMITTING TRUE DP HOMOGENETS AND HETEROGENETS

"CAMERA INSTRUCTION BOOK-LIKE" MANUALS PERSONALIZABLE WITHOUT PROGRAMMING CONTEXT DEPENDENT EDITING FOR TEST, TYPESETTING, MAIL, FILE CABINET, PICTURES FORMS, TABLES, ETC.

IMPLEMENTATION DESIGN GOALS

NO ASSEMBLY LANGUAGE PROGRAMMING

CONSISTENCY AND COMPATIBILITY FOR FORMING DP HOMOGENETS AND HETEROGENETS

ALL PROGRAMS DRIVEN FROM: FILES, TERMINALS, TEXT, ANY OTHER PROGRAM USING VARIOUS PROGRAM MODELS (TP, PIPES, SINGLE PROCESS, AND NETWORK)

BUILT IN FOREIGN LANGUAGES

TYPED DATA FOR FILES, FORMS AND PROGRAMS

COST OF CAPABILITY UNDERSTANDING

PERSONAL OR SHARED?

GIVEN: ECONOMY OF SCALE, EXCEPT DISKS AND SWITCHING DISAPPEARING. ALL MEMBERS OF HIERARCHY ARE NEEDED.

STRATEGY: MOVE FROM GENERAL TO SPECIFIC AND PERSONAL

PROBLEMS: DISTRIBUTING AND SHARING PROGRAMS, PROGRAMMING AND DATA. USING.

PBS (1985) GENERIC CAPABILITIES:

WPS: FULL PAGE, VOICE INPUT, GRAPHICS, PROFESSION DEPENDENT. ARCHIVES ANY PART AND ALL DOCUMENTS.

USER-TYPESETTING: YES

FILE CABINET: RETRIEVE BY MULTIPLE KEYWORD. SEARCH FOR CONTENT.

MAIL SYSTEMS: VOICE. COMPUTER CONFERENCING WITH PERSONAL VIDEO CONFERENCING IN SIGHT.

COMMUNICATIONS: INTERNETS, PACKETNETS, AND NON-COMPUTER NETS (E.G. PHONE, FAX, TWX, OCR FOR OLD DOCUMENTS).

OFFICE PROCEDURES: NUMEROUS

A PROFESSION BASED SYSTEM
(FOR LARGE ORGANIZATIONS)

- IS A HIERARCHY OF COMPUTERS (INCLUDING PERSONALS?)

- PROVIDES BENEFIT NOW THROUGH GENERIC CAPABILITIES FOR TEXT, FILING AND COMMUNICATIONS

- REQUIRES ATTENTION TO HUMAN ENGINEERING, AND COST OF CAPABILITY (INCLUDING OWNERSHIP)

OFFICE AUTOMATION - OA - EVOLUTIONARY USE OF WORD PROCESSING AND ELECTRONIC MAIL EQUIPMENT TO IMPROVE OFFICE PRODUCTIVITY, WHERE:

1. WORD PROCESSING EQUIPMENT, EVOLVING TO USER TYPESETTING REPLACES, TYPEWRITERS, SNOPAKE, AND COPIERS.

2. ELECTRONIC MAIL REPLACES COPIERS AND POST PEOPLE, FAX, TWX/TELEX AND INTRA-ORGANIZATION ELECTRONIC TORN TAPE MESSAGE SWITCHES.

3. COMMON CARRIER PACKETNETS EVOLVE FOR INTER-ORGANIZATIONAL MESSAGE AND DATA SWITCHING.

4. ELECTRONIC FILING REPLACES PAPER FILES.

5. DIRECT SOURCE FORMS ENTRY AND TRANSMISSION REPLACES MODERN KEYPUNCH.

6. LOCALIZED LIST PROCESSING FOR REPORTS REPLACES CENTRAL, DATA PROCESSING.

DISTRIBUTED PROCESSING MATCHES COMPUTER SYSTEMS TO NEEDS ON A GEOGRAPHICAL OR ORGANIZATIONAL BASIS, AND INTERCONNECTS INDIVIDUAL COMPUTER SYSTEMS INTO A SINGLE NETWORK.

THE OBJECTIVES OF DISTRIBUTED PROCESSING ARE:

1. TO ALLOW EFFECTIVE MATCHING OF RESOURCES TO NEEDS.

2. TO ALLOW BOTH LOCAL AUTONOMY AND CENTRAL CONTROL OF THE VARIOUS DISTRIBUTED PARTS.

3. TO PROVIDE AN EVOLVING, OPEN ENDED SYSTEM SO THAT THE DEVELOPMENT OF DISTRIBUTED PARTS CAN PROCEED AT THEIR OWN PACE IN A QUASI INDEPENDENT FASHION.

4. TO ALLOW PURCHASE AND INSTALLATION OF COMPUTER IN THE MOST TIMELY, COST-EFFECTIVE WAY, TAKING ADVANTAGE OF REDUCED (WITH TIME) HARDWARE COSTS.

5. TO BUILD ON AND COMMUNICATE WITH EXISTING, MORE CENTRAL SYSTEMS, FULLY DISPERSED SYSTEMS, AND EMERGING PERSONAL COMPUTERS.

6. TO PROVIDE COMPUTING, CONTROL AND STORAGE OF INFORMATION NEAREST THE NEED.

DISTRIBUTED PROCESSING IS THE MATCHING OF COMPUTER RESOURCES TO NEEDS- ON A GEOGRAPHICAL OR ORGANIZATIONAL BASIS - AND THE INTERCONNECTION OF THESE RESOURCES TO FORM A SINGLE, COST-EFFECTIVE SYSTEM.

THE OBJECTIVES OF THIS STRATEGY FOR BUYING AND USING COMPUTERS ARE TO REDUCE DATA PROCESSING COSTS, INCREASE PRODUCTIVITY AND IMPROVE ORGANIZATIONAL EFFICIENCY.

TACTICALLY, DISTRIBUTED PROCESSING MAKES IT POSSIBLE TO:

- CONTROL COSTS BY MATCHING COMPUTER PROCUREMENT TO ACTUAL NEEDS.

- DECOUPLE OR CENTRALIZE SYSTEM DEVELOPMENT.

- CENTRALIZE OR DECENTRALIZE ADMINISTRATIVE CONTROLS.

- MATCH PROCESSING CAPABILITIES, CONTROL AND STORAGE OF INFORMATION ON THE MOST COST-EFFECTIVE BASIS.

- COMMUNICATION WITH THE EXISTING CENTRALIZED SYSTEMS, WITH FULLY DISPERSED SYSTEMS, AND WITH COMPUTER WORK-STATIONS AND PERSONAL COMPUTERS AS THEY EMERGE AT EVERY LEVEL OF THE ORGANIZATION.

- MANAGE OPEN-ENDED GROWTH.

FUNCTIONAL LEVELS OF A PBS ROOT (HARDWARE, OS, LANGUAGES, NETWORKING AND DATA BASES)

GENERIC MODULES FOR COMMUNICATIONS WITHIN AN ORGANIZATION

- TEXT AND GRAPHICS PROCESSING AND "USER TYPESETTING"
- FILING CABINETS FOR TEXT, MESSAGES, FORMS, ETC.
- ELECTRONIC MAIL AND COMPUTER CONFERENCING
- OFFICE PROCEDURES AND FORMS PROCESSING
- INTERFACE TO NON-COMPUTER COMMUNICATIONS (FAX, OCR, INTERFACE TO OTHER ORGANIZATIONS, TWX, TYPESETTERS, TELEPHONE)

GENERAL PROFESSIONAL DISCIPLINE MODULES (E.G. ENG.)

DEPARTMENTAL PROFESSIONAL DISCIPLINE (E.G. ELEC. ENG.)

COMPARTMENTAL PROFESSIONAL DISCIPLINE (E.G. RF CKT. DESIGN)

OFFICE OF FUTURE (OOF)

USE OF EQUIPMENT WHICH ALLOW A DRASTIC RESTRUCTURING OF OFFICE WORK, AMONG A DIFFERENT COMPOSITE WORK FORCE.

PARAPHRASING THE APRIL 80 COOPERS AND LYBRAND NEWSLETTER: "A SECRETARY USES THE EQUIPMENT, IT'S OA; AND IF WE ALL USE IT, IT'S OOF".

LARGE, CENTRALLY OPERATED FACILITIES PROVIDE:

LARGE, SHARED DATA BASES AT LOWEST COST/BYTE (THROUGH ECONOMY OF SCALE OF LARGE DISKS)

ARCHIVAL OF PERSONAL FILES

PROGRAMS FOR SPECIAL NON-COMPUTER OWNER COMMUNITIES

VERY HIGH PERFORMANCE PROCESSING

COMMUNICATIONS AMONG THE ENTIRE COMMUNITY AND GATEWAYS TO INTERNETS AND PACKETNETS

COMMUNICATIONS ORIENTED SERVICES (E.G. MAIL, TELECONFERENCING)?

SPECIAL FACILITIES SUCH AS TYPESETTING

GROUP CENTERED COMPUTERS PROVIDE:

RELATIVELY COST-EFFECTIVE FILE STORAGE FOR ITS COMMUNITY

FACILITIES BEST MATCHED TO COMMUNITY

RELATIVELY HIGH PERFORMANCE PROCESSING

COST-EFFECTIVENESS THROUGH GROUP SUPPORTED PROGRAMS

PERSONAL COMPUTERS PROVIDE:

PERSONAL DATA BASES AND SECURITY

FAST RESPONSE TO RELATIVELY COMPLEX REQUESTS (E.G. EDITING)

PROGRAM ENVIRONMENT FOR ENTERING AND GETTING INTO PRODUCTION

PHYSICAL SYSTEM

CLOSETABLE OR IN A DESK IF QUIET ENOUGH

Pc + Mp (1 Mbyte) + Ms (100 Mbyte; FIXED)...NOTE 1 FILE CABINET = 32 Mbytes

2 - 4 X T.-CRT(1 PAGE B/W, OR COLOR)
WITH ABILITY TO REMOTE AT REDUCED BANDWIDTH

T(LETTER QUALITY AND SCREEN PRINTER)

T(TELEPHONE DIALER, PHONE ANSWERER, VOICE OUTPUT)

L(SYSTEMS OF THE SAME TYPE) FOR:
COMMUNICATION, EXECUTING OTHER PROGRAMS, TELE- AND COMPUTER-CONFERENCING, ETC.

L(CENTRAL SYSTEM) FOR:

- FILING, PRINTING, TYPESETTING, AND SLIDE MAKING
- DISTRIBUTION OF DOCUMENTS TO PEOPLE NOT ON SYSTEM
- ACCEPTANCE OF DOCUMENTS FROM PEOPLE NOT ON SYSTEM
- EMS'S, AND OTHER SYSTEMS

T(VIDEO AND VOICE I/O) - LARGE SCREEN FOR TELECONFERENCING)

STRUCTURE OF PROFESSION MODULES AND USE DEPENDENCIES

USE IS A FUNCTION OF THE PRODUCT OF:

PROFESSIONAL DISCIPLINE/PROJECT DISCIPLINE
ORGANIZATION (BUYER, SELLER, KNOWLEDGE SELLER, CONTROLLER/GOV'T)

PERSON'S ROLE:

MKT.-, MFG.- TECH- GATEKEEPER, IDEA GENERATOR/CREATIVE SCIENTIST, ENTREPENEUR, COACH/SPONSOR, PROBLEM SOLVER

(...NOTE VARYING DEGREE OF COMMUNICATION, ANALYSIS, NEED TO ACCESS AND PRESENT DATA IN EACH ROLE

POSITION IN ORGANIZATION HIERARCHY

TIME OF FISCAL YEAR AND OTHER PROCESSES (E.G. PLANNING)

TIME OF TRANSACTION (PROCESS STATE)

E.G. PROJECT (PROPOSAL, DESIGN, ANNOUNCEMENT, DEATH) ETC.

USER VIEW GOALS

LIVE AND WORK ON THE MACHINE

CONSISTENCY AND COMPATIBILITY ACROSS KEYBOARDS, SYNTAX/SEMANTICS, FILES, COMMUNICATIONS...PERMITTING TRUE DP HOMOGENETS AND HETEROGENETS

"CAMERA INSTRUCTION BOOK-LIKE" MANUALS PERSONALIZABLE WITHOUT PROGRAMMING CONTEXT DEPENDENT EDITING FOR TEST, TYPESETTING, MAIL, FILE CABINET, PICTURES FORMS, TABLES, ETC.

IMPLEMENTATION DESIGN GOALS

NO ASSEMBLY LANGUAGE PROGRAMMING

CONSISTENCY AND COMPATIBILITY FOR FORMING DP HOMOGENETS AND HETEROGENETS

ALL PROGRAMS DRIVEN FROM: FILES, TERMINALS, TEXT, ANY OTHER PROGRAM USING VARIOUS PROGRAM MODELS (TP, PIPES, SINGLE PROCESS, AND NETWORK)

BUILT IN FOREIGN LANGUAGES

TYPED DATA FOR FILES, FORMS AND PROGRAMS

COST OF CAPABILITY UNDERSTANDING

PERSONAL OR SHARED?

GIVEN: ECONOMY OF SCALE, EXCEPT DISKS AND SWITCHING DISAPPEARING. ALL MEMBERS OF HIERARCHY ARE NEEDED.

STRATEGY: MOVE FROM GENERAL TO SPECIFIC AND PERSONAL

PROBLEMS: DISTRIBUTING AND SHARING PROGRAMS, PROGRAMMING AND DATA. USING.

PBS (1985) GENERIC CAPABILITIES:

WPS: FULL PAGE, VOICE INPUT, GRAPHICS, PROFESSION DEPENDENT. ARCHIVES ANY PART AND ALL DOCUMENTS.

USER-TYPESETTING: YES

FILE CABINET: RETRIEVE BY MULTIPLE KEYWORD. SEARCH FOR CONTENT.

MAIL SYSTEMS: VOICE. COMPUTER CONFERENCING WITH PERSONAL VIDEO CONFERENCING IN SIGHT.

COMMUNICATIONS: INTERNETS, PACKETNETS, AND NON-COMPUTER NETS (E.G. PHONE, FAX, TWX, OCR FOR OLD DOCUMENTS).

OFFICE PROCEDURES: NUMEROUS

Slides

Order

RC - 1/77 ?

1) CPU

2) Message

3) System overview

4) Hdwr system overview

5) CPU Family

6) Future " CPU product

7) " Family (system size vs time)

8) Tie # to cost perf

9) Cost Perf

10) Tech Drive

11) Devel Process

12) Repeat 6

13) CPU Gen strategy

14) CPU STRATEGIES

15 Tech "

16 Arch "

17 Mfg "

18. Key Tactic Risk

19 Repeat 7 ✓

20 Repeat 2

CENTRAL PROCESSORS

DIGITAL'S

"CORPORATE JEWELS"

MESSAGE

DEC CPU (SYSTEM) STRATEGY IS HEAVILY FOCUSED ON THE PDP-11

THE STRATEGY EXPANDS THE PRESENT BASE UPWARD AND DOWNWARD OVER TIME.

THE CPU STRATEGY IS DRIVEN BY:

- MEMORY TECHNOLOGY
- SEMICONDUCTOR TECHNOLOTY

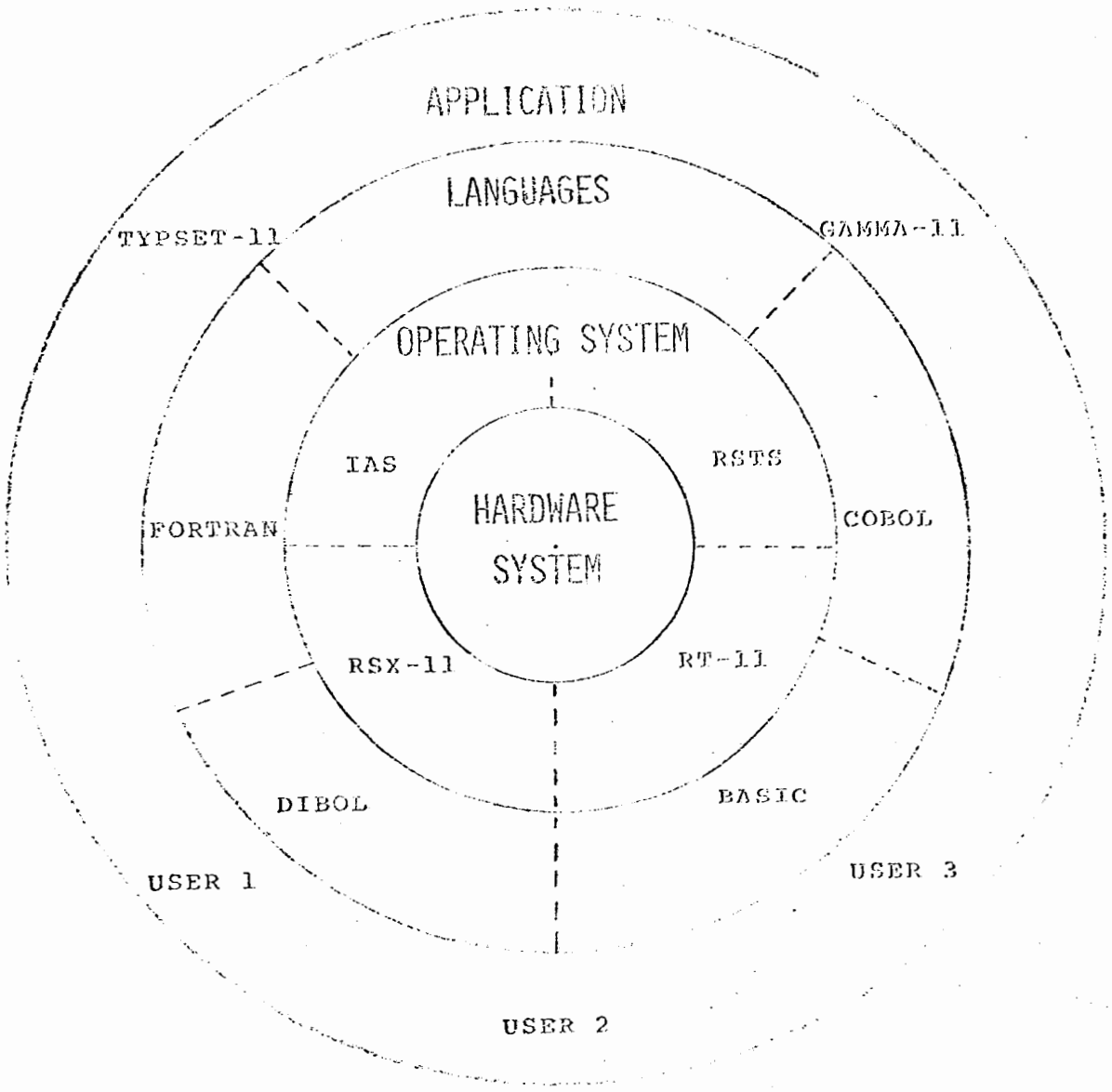
} IMPLEMENTATION

THE CPU STRATEGY GENERALLY ENCOMPASSES:

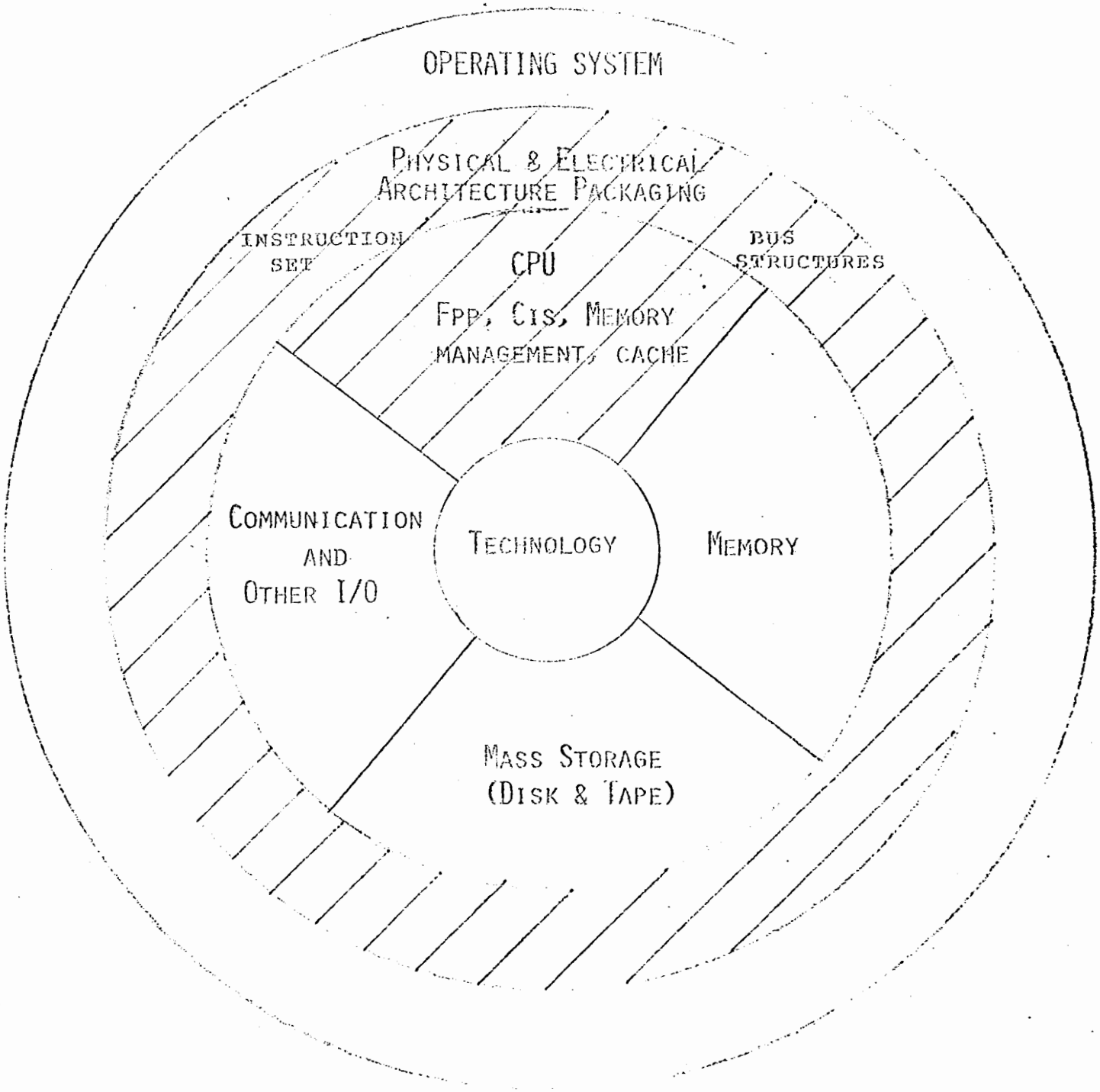
- HARDWARE INSTRUCTION SET
- ELECTRICAL & PHYSICAL BUS STRUCTURES
- MECHANICAL PACKAGING STRUCTURES.

} SYSTEM ARCHITECTURE

COMPUTER SYSTEM OVERVIEW

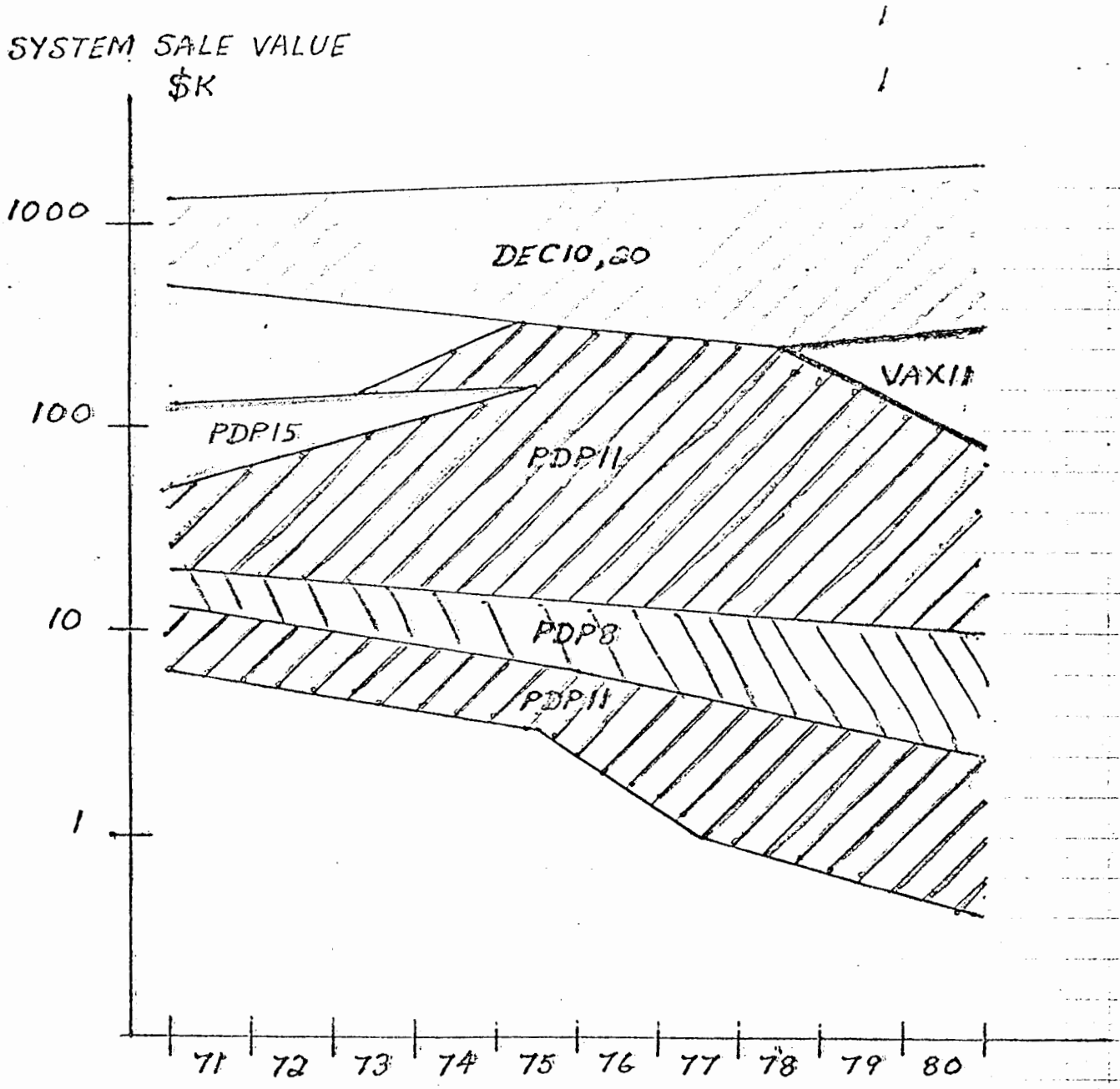


HARDWARE SYSTEM OVERVIEW



DIGITAL EQUIPMENT CORP

SYSTEM SALES VALUE vs TIME



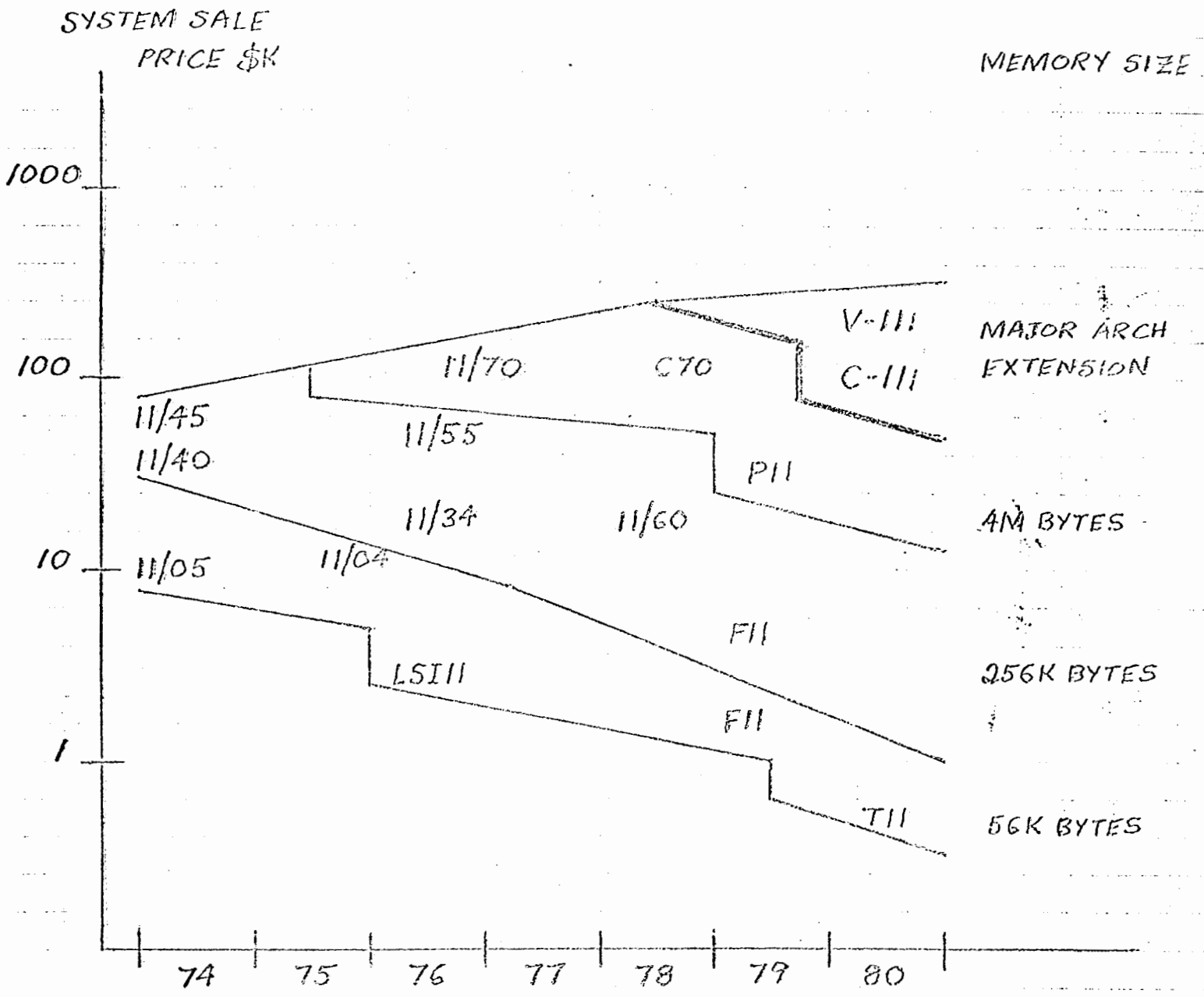
FUTURE CPU PRODUCT STRATEGY

V 11	MAJOR ARCH.EXT. TO 11, SCI. FIRST	FY78
C 11	2ND IMPLEMENTATION USING NEW TECHNOLOGY	FY79
C 70	COMMERCIAL ENHANCEMENT TO 11/70	FY78
P 11	PHYSICAL MEMORY ADDRESS EXT. BEYOND 256K BYTES FOR 60 AND 34	FY79
F 11*	NEW NMOS 11 CHIP SET THAT IMPLEMENTS MOST 11/34 & 11/60 FUNCTIONS AT VERY LOW COST.	FY79
T 11*	SINGLE CHIP 11 USING ~~MICROPROCESSOR~~ INDUSTRY BUS	FY79
VT78	PDP-8 SYSTEM IN VT52	FY78
DK/KRYPTON	PACKAGING ARCHITECTURE FOR SMALL 11 SYSTEM	FY78

*CHIP LEVEL, A NUMBER OF BOARD AND BOX LEVEL VERSIONS CAN BE EXPECTED.

PDP11 FAMILY

SYSTEM SIZE vs TIME

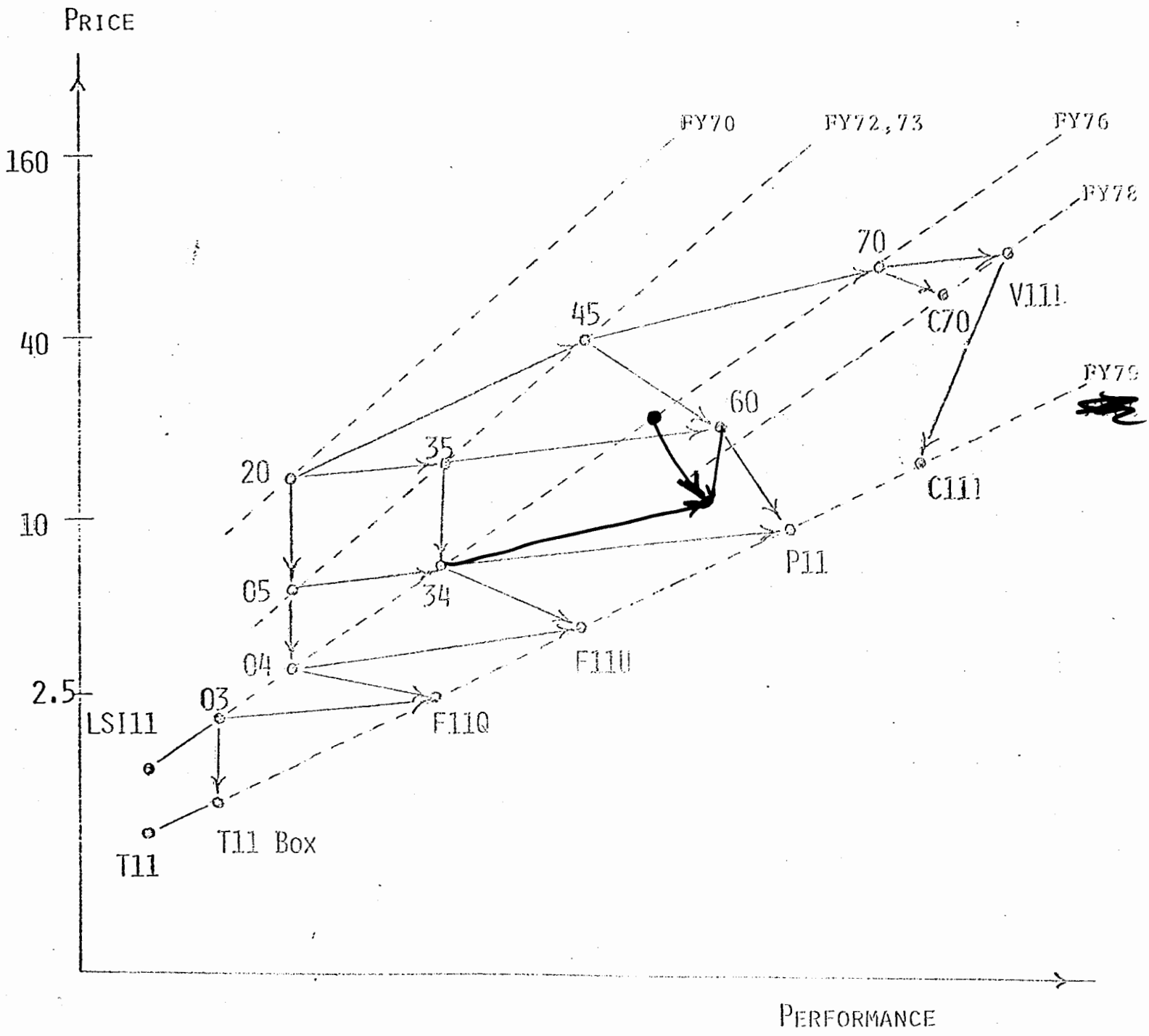


Cost Of System vs Time Valid Only If Cost Performance Is Competitive!

CPU - Hardware System Metrics

Execution Speed
Bus Speed (I/O)
Instruction Set (CIS, FPP)
Packaging (Size Weight)
RAMP
Memory Size
Disk Size

PDP11 CENTRAL PROCESSOR FAMILY EVOLUTION



TECHNICAL DRIVE:

Comes From Semiconductors.

Goal: Contain Technical Change At Lowest Architecture
Yielding Good Cost Performance At User Level.

Role of Architecture is Crucial:

Chips
Boards (backplane Bus)
Cables (long Buses)
Protocols

IF: Technical Change Rate Slow and
Architecture Remains Fixed

THEN: Product Is Result Of Cumulative Historic Investment.

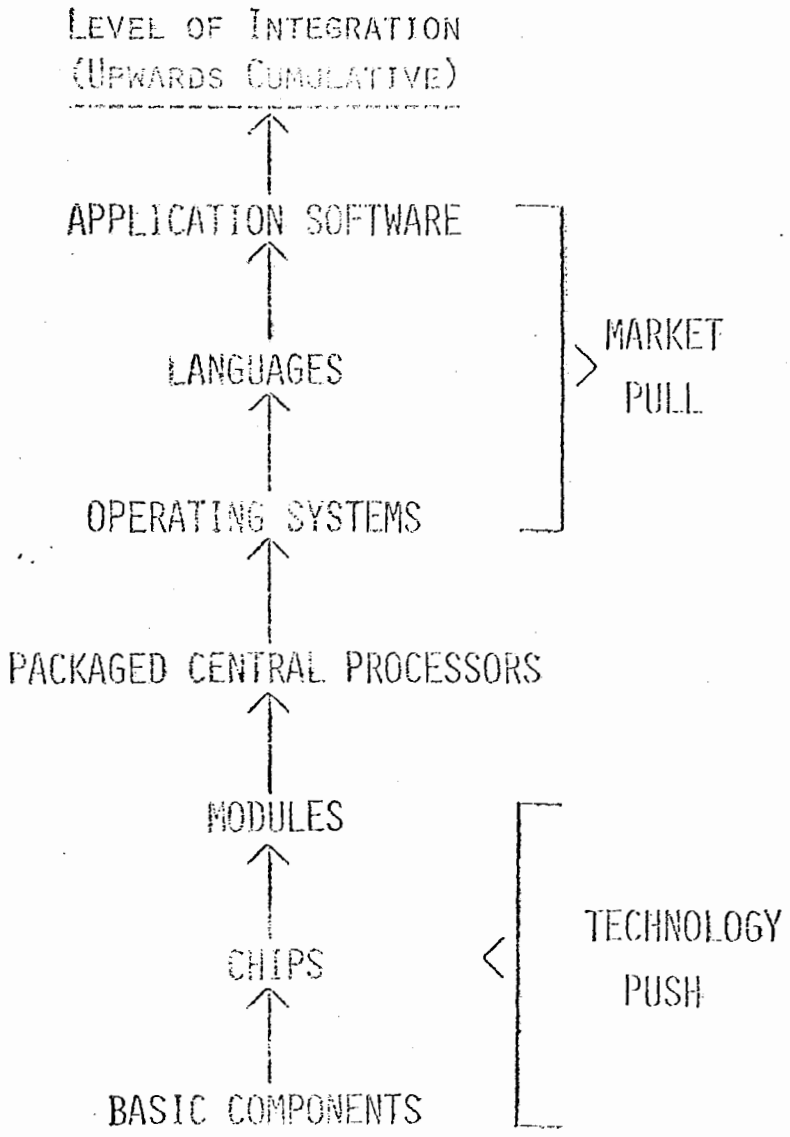
i.e.) Fortran vs Memory Matrix.

Examples:

Unibus	old
11 Instruction Set	old
Magic Backplane	old
P11	New
V111 Instruction Architecture	New
F11 Chip Architecture	New
Low End Package	New

DEVELOPMENT PROCESS

GOOD ARCHITECTURE ALLOWS YOU TO KEEP TECHNOLOGY CHANGE AS LOW AS POSSIBLE.



GENERAL STRATEGIES

- MORE INTERNAL COMPLEXITY YIELDS EXTERNALLY SIMPLER PRODUCTS.
- TRACK MEMORY SIZE (PRICE) CHANGE.
- ADD SEMI TECHNOLOGY TO CPU'S.
- HOLD ARCHITECTURE BOUNDARIES TO MINIMIZE AMOUNT OF SYSTEM TO CHANGE.
- RETAIN ADAPTABILITY TO TRACK EVOLVING TECHNOLOGY WITH MINIMIZING PAIN.

BASIC CPU AND SYSTEM STRATEGIES

VAX (V111, C111)

- EXPAND 11 ARCHITECTURE UPWARD

11 FAMILY (MID RANGE)

- COMMERCIAL FOCUS
- PHYSICAL ADDRESS EXTENSION
- RAMP
- COST PERFORMANCE

LOW END

- NEW HIGH PERFORMANCE CHIP SET — F11
- NEW TINY CHIP — T11
- PACKAGING ARCHITECTURE — DK KRYPTON
- UPWARD SOFTWARE MIGRATION

PDP-8

- CLEVER, AGGRESSIVE, FOCUS ON EXISTING BASE
- KEEP 11 HONEST
- USE OTHERS' DEVELOPMENTS

DEC 20

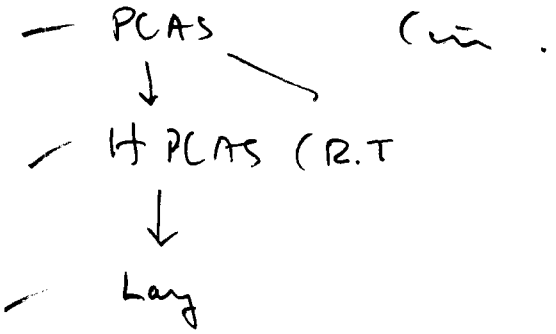
- SOFTWARE ENHANCEMENT
- MANUFACTURING COST REDUCTION
- BACKUP TO VAX
- VAX WILL DOMINATE VAX IN 8 YEARS

TECHNICAL TACTICS

NMOS	LOW END
MOS MEMORY	ALL
CUSTOM LSI	MID RANGE 11
GATE ARRAY	C111, LATER MID 11
COMMERCIAL INST	ALL
CMOS (EXTERNAL)	8
FIBER OPTICS	11 MID RANGE

ARCHITECTURE TACTICS

CACHE	ALL PRODUCTS EXCEPT LOW
COMMERCIAL INSTRUCTION	ALL EXCEPT 8
~~BIG PHYSICAL MEMORY~~	~~ALL~~ mid 11 (11/70 ARCHTIECTURE)
MULTIPROCESSORS	HIGH 11 FIRST



PACKAGING TACTICS

UNIFIED LOW END PACKAGED ARCHITECTURE	VT100 AND KRYPTON (TERMINAL PROCESSOR)
MAGIC BACKPLANES	MID-11, LSI-11
CORPORATE CABINET	MID-11, VAX
STANDARDS COMPLIANCE	WORLD WIDE, ALL PRODUCTS

KEY RISKS

GENERAL:

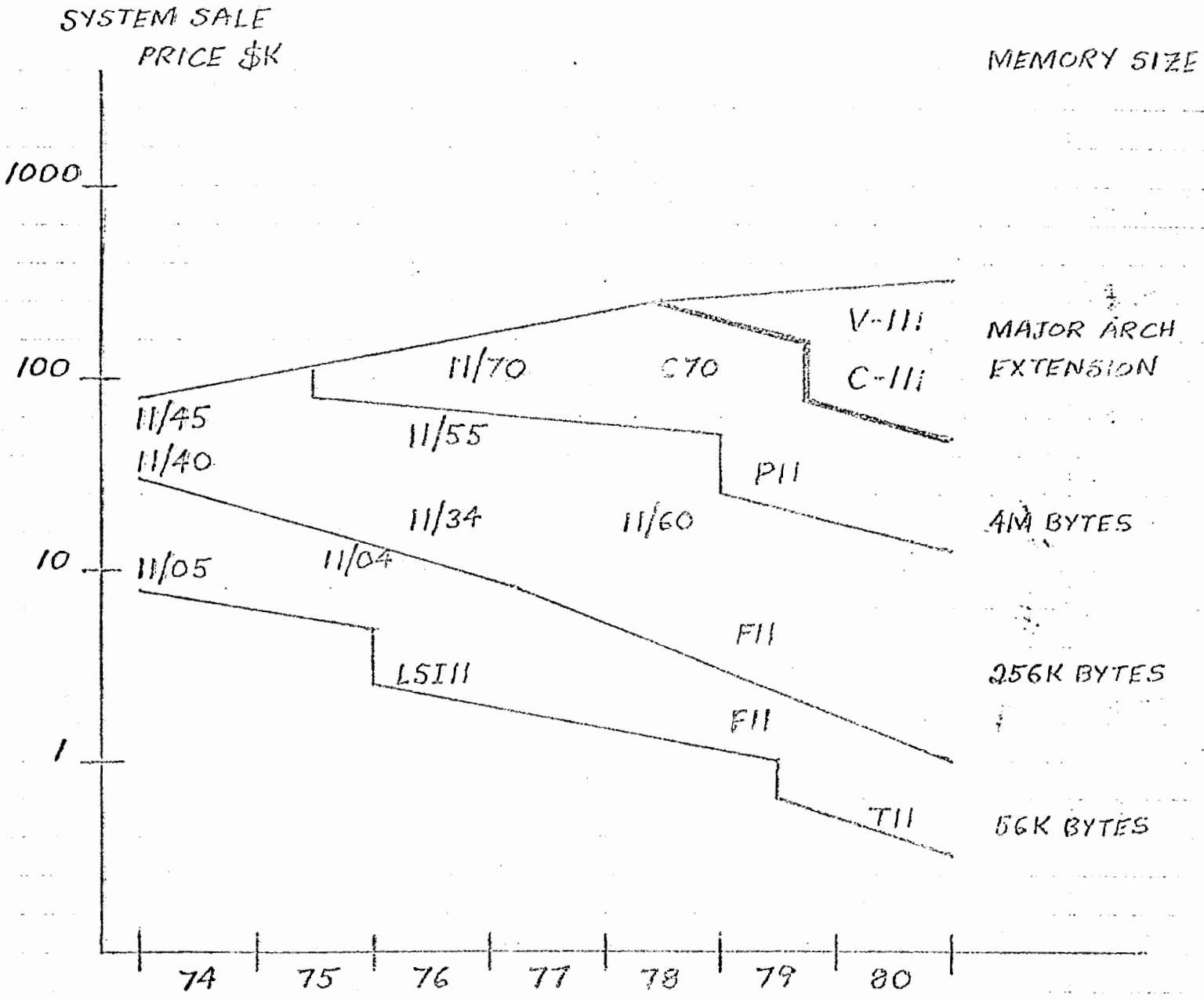
- COST PERFORMANCE REMAINS COMPETITIVE ACROSS RANGE OF MAJOR VALUE (LEADING SELECTIVELY).
- ARCHITECTURES EVOLVE RAPIDLY ENOUGH TO TRACK TECHNOLOGY, BUT NOT SO FAST AS TO LOSE CUMULATIVE SOFTWARE INVESTMENT.
- FAIL TO MANAGE 20-V111-11 FAMILY OVERLAP.

SPECIFIC TACTICAL RISKS

- WE STUMBLE WITH VAX SCHEDULE, ARCHITECTURE, COST OF LATER SYSTEMS.
- WE ARE LATE WITH COMMERCIAL ENHANCEMENTS TO LARGER 11 FAMILY SYSTEMS.
- F-11 IS TOO HARD TO PRODUCE.
- WE FAIL TO MEET OUR SEMICONDUCTOR GOALS ON NMOS (T11) OR GATE ARRAY DESIGN (2ND VAX).
- BUBBLES COME VERY FAST (LESS THAN 24 MONTHS).
- MAJOR MULTI CPU ARCHITECTURE BEYOND NETWORKS.

PDP11 FAMILY

SYSTEM SIZE vs TIME



MESSAGE

DEC CPU (SYSTEM) STRATEGY IS HEAVILY FOCUSED ON THE PDP-11

THE STRATEGY EXPANDS THE PRESENT BASE UPWARD AND DOWNWARD OVER TIME.

THE CPU STRATEGY IS DRIVEN BY:

- MEMORY TECHNOLOGY
- SEMICONDUCTOR TECHNOLOTY

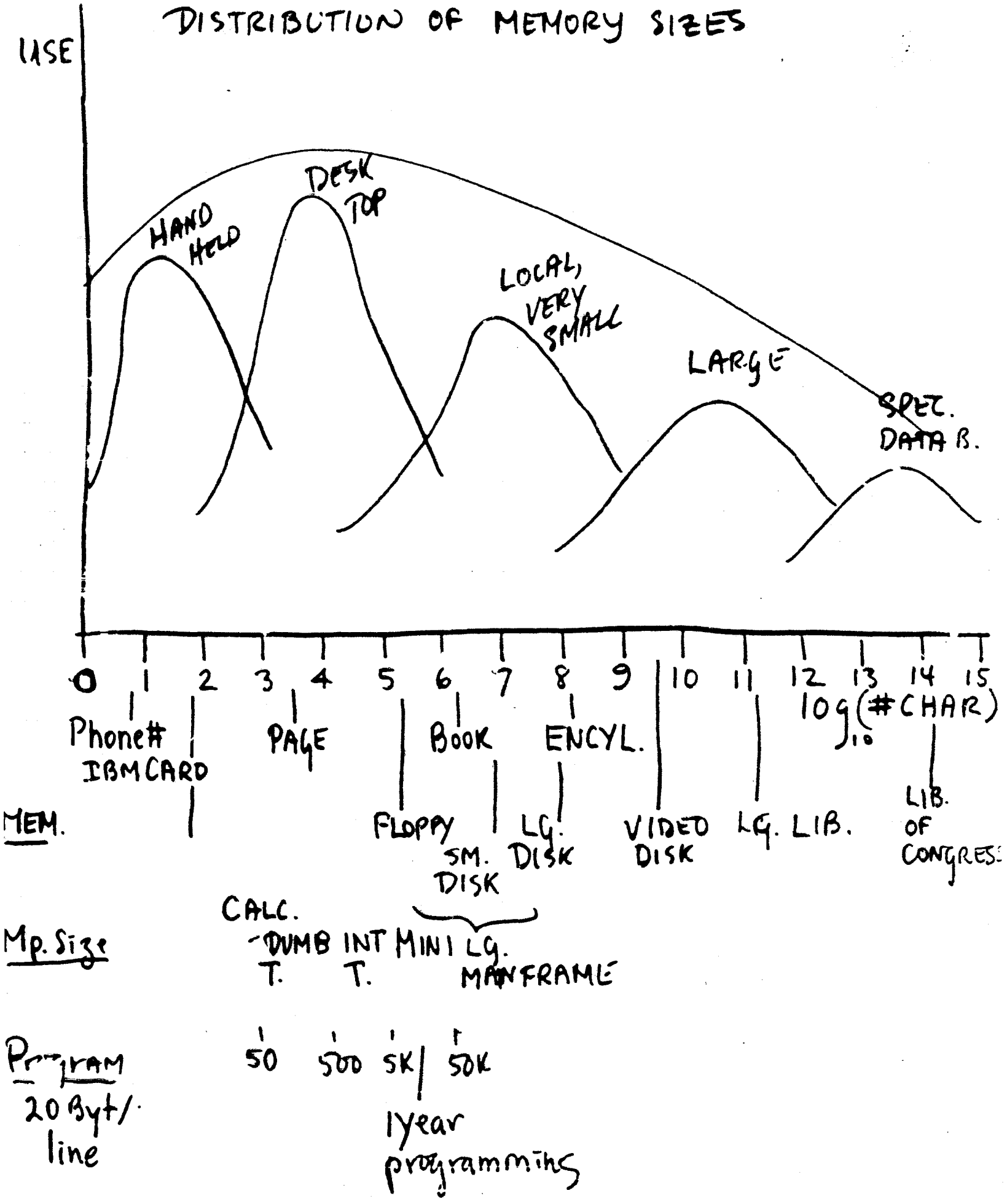
} IMPLEMENTATION

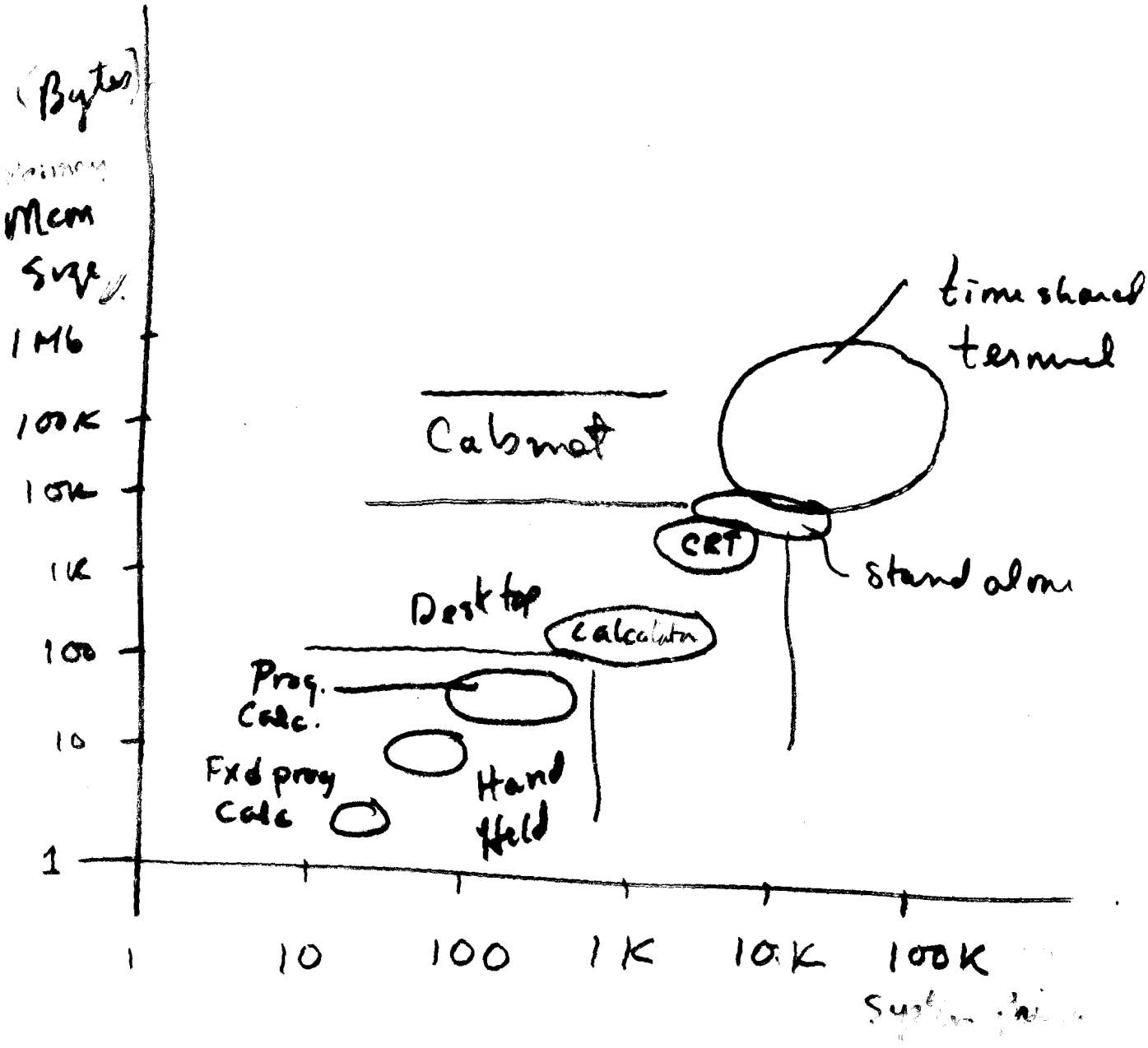
THE CPU STRATEGY GENERALLY ENCOMPASSES:

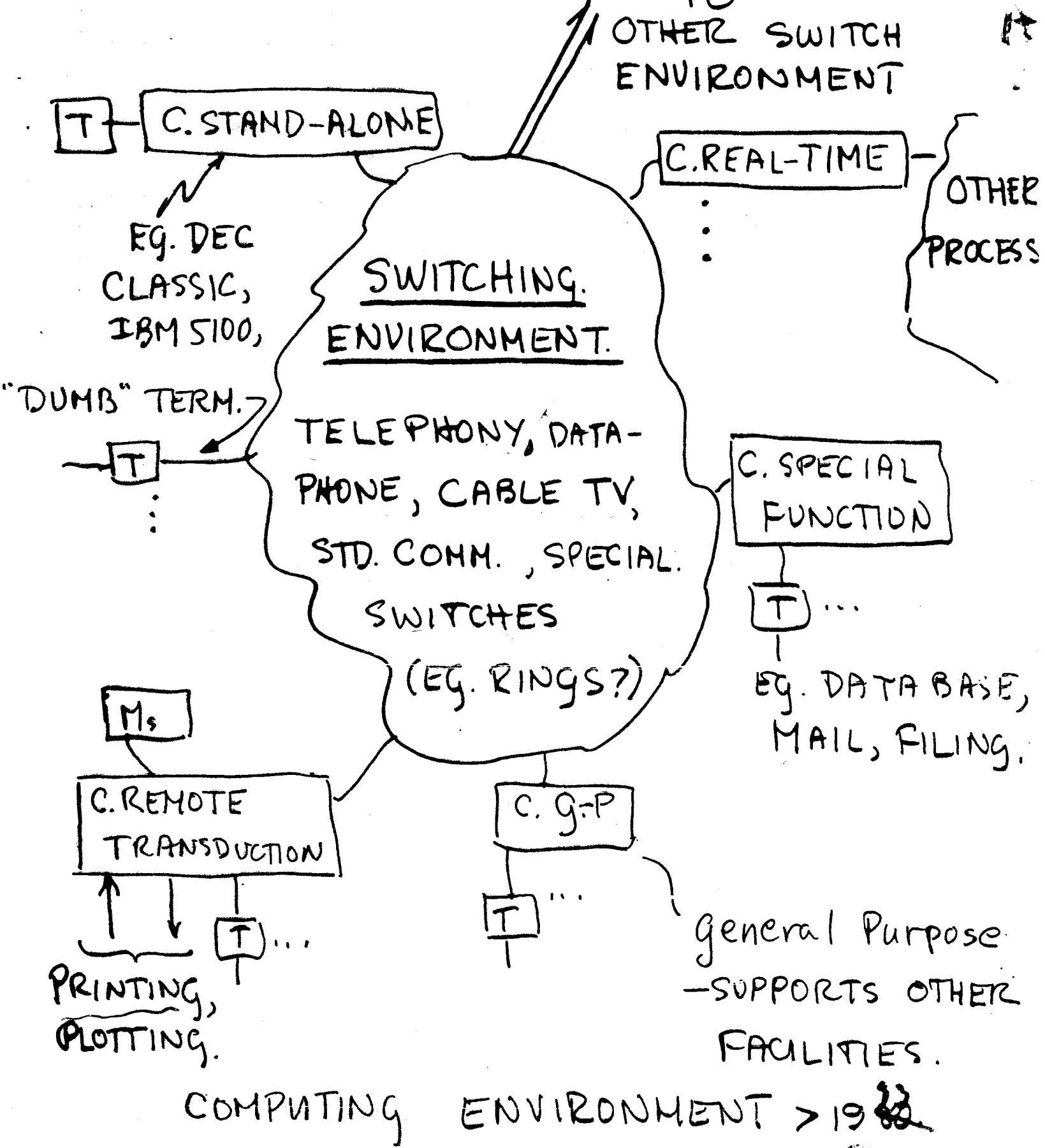
- HARDWARE INSTRUCTION SET
- ELECTRICAL & PHYSICAL BUS STRUCTURES
- MECHANICAL PACKAGING STRUCTURES.

} SYSTEM ARCHITECTURE

DISTRIBUTION OF MEMORY SIZES



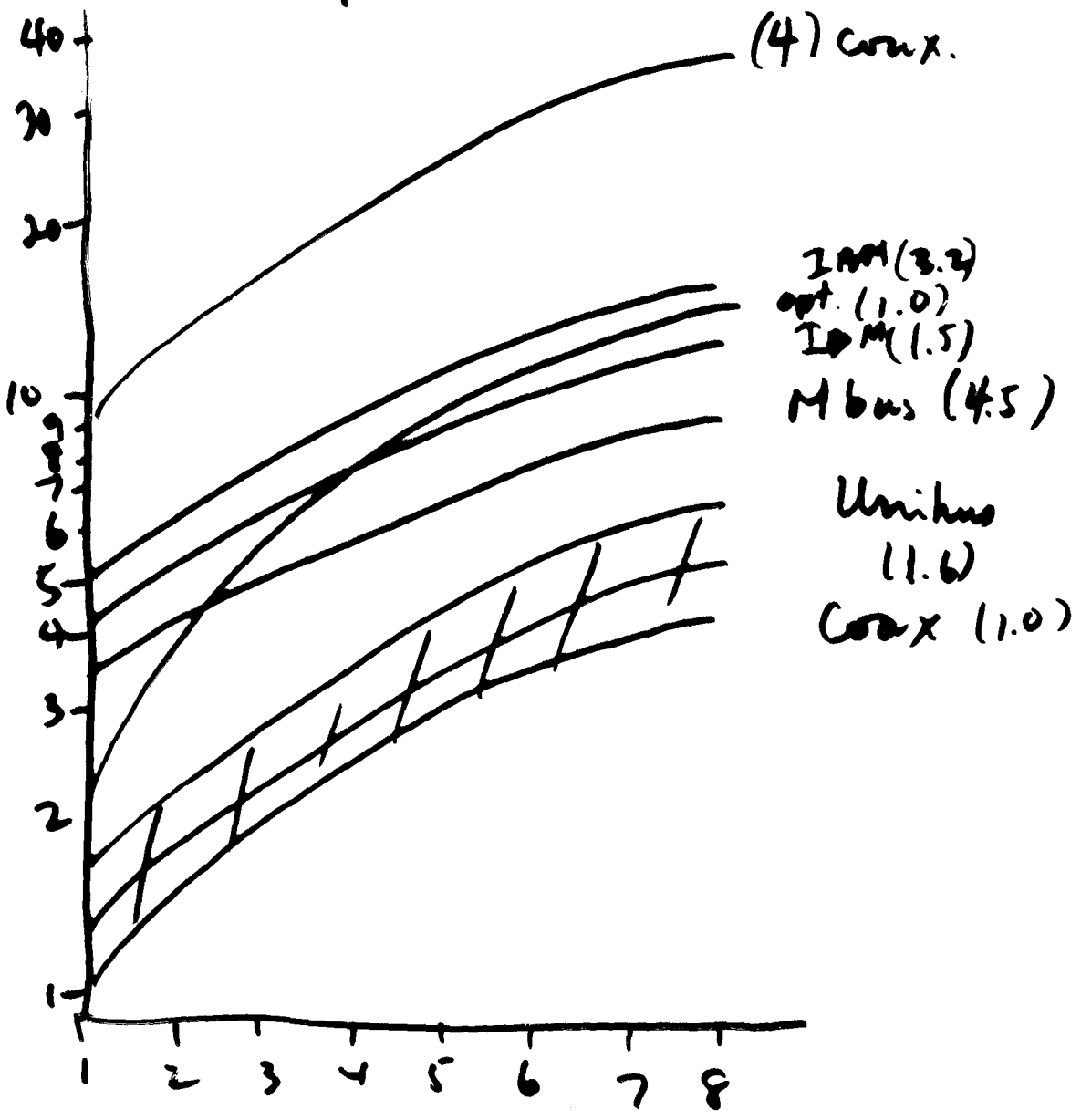

(Bytes)
Mem Size
1MB
100K
10K
1K
100
10
1
Cabinet
time shared terminal
CRT
stand alone
Desktop
Calculator
Prog. Calc.
Fxd prog Calc
Hand Held
1
10
100
1K
10K
100K

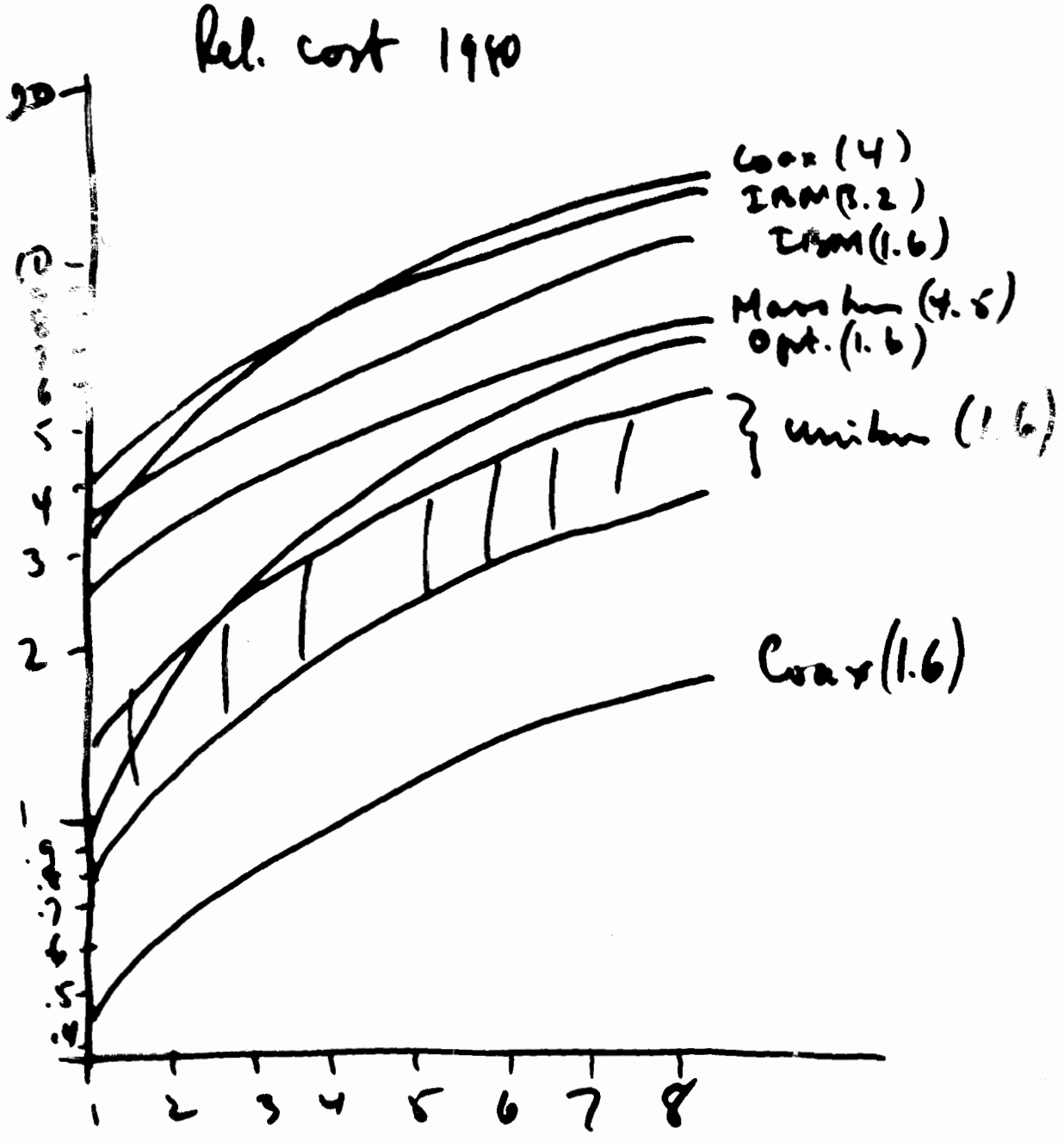


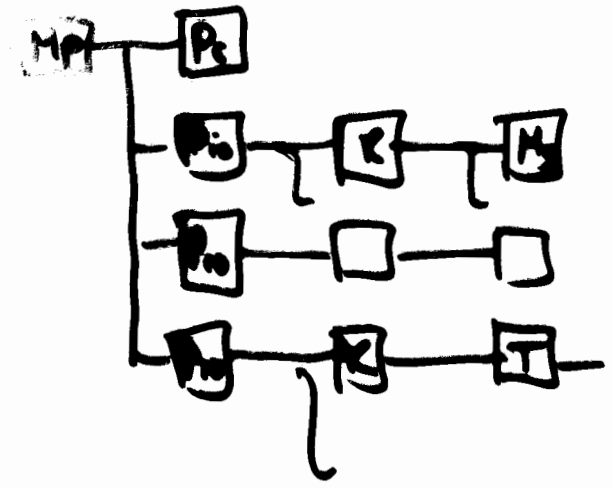
COMPUTING ENVIRONMENT > 19~~82~~

(12)

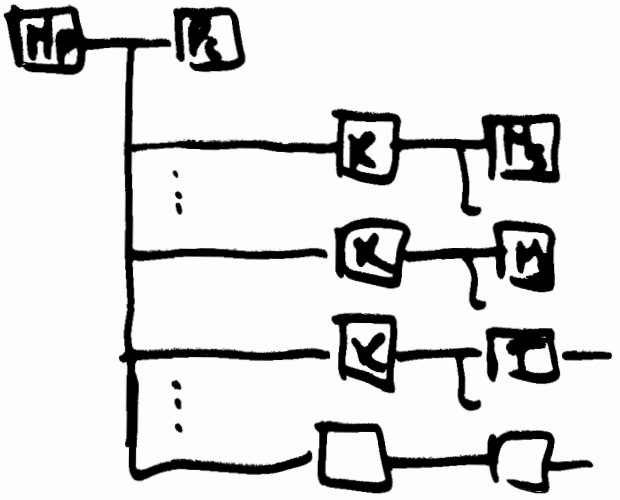
Rel. cost of interfaces
1977



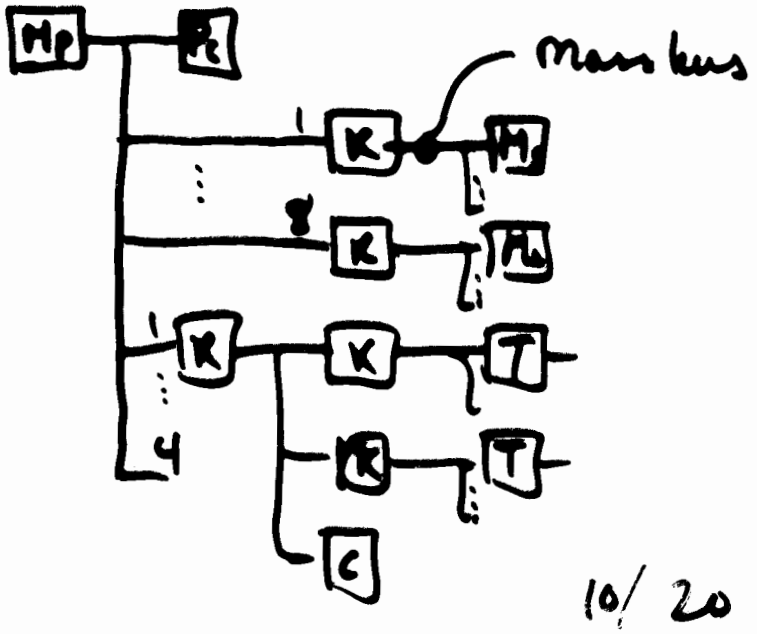

Rel. cost 1980
20
10
6
5
4
3
2
1
.5
.4
1 2 3 4 5 6 7 8
Coax (4)
IAM (3.2)
IAM (1.6)
Mono (4.5)
Opt. (1.6)
Mono (1.6)
Coax (1.6)



360 / 370



11



10/ 20

GROSCH'S LAW COULD HOLD

ASSUME:

PERFORMANCE = MEMORY-DATA-RATE X MEMORY-SIZE

MEMORY-SIZE $\approx$ 4K/25 X PRICE (IN $)

MEMORY-DATA-RATE $\approx$ 2M/25 X PRICE (IN $)

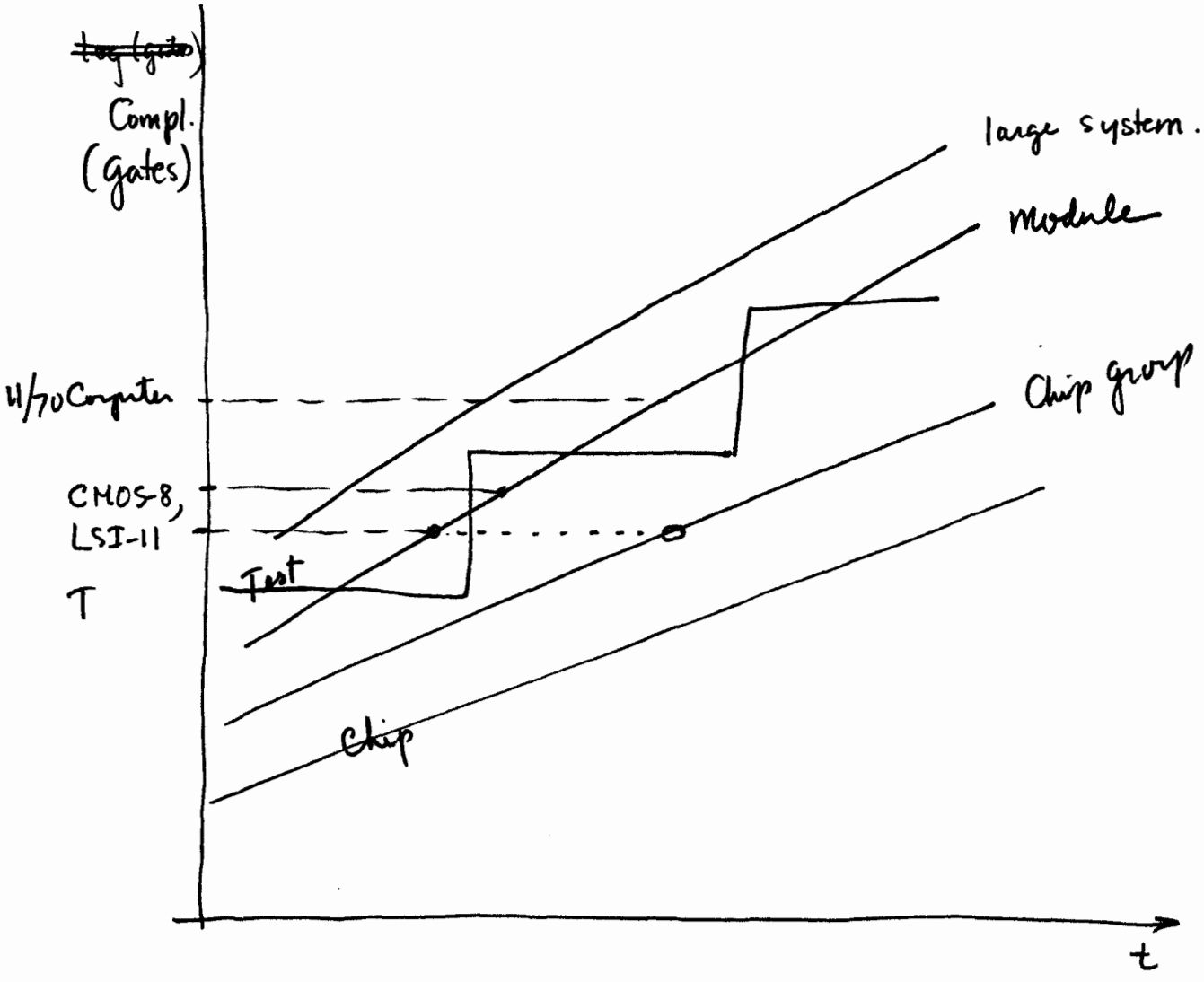
PERFORMANCE = (8 X 10^9/625) X $PRICE^2$

LAW HOLDS IF PROCESSING IS ADDED FOR EACH 4K CHIP...TO FULLY OCCUPY ACCESSES.

LAW HOLDS IF COST OF PROCESSOR = 0 OR $\approx$ MEMORY SIZE.

1. BY LARGE PROCESSOR
2. BY FULLY INTERCONNECTED, DISTRIBUTED PROCESSOR
3. TOTALLY SEPARATED MACHINES

ALSO NOTE A STRAIGHT LINE IS A REASONABLE APPROXIMATION TO A SQUARE LAW OVER AN ORDER-OF-MAGNITUDE RANGE.


~~log (gate)~~
Compl.
(gates)
large system.
module
Chip group
H/P0 Computer
CMOS-8,
LSI-11
T
Test
Chip
t

	Cray1	Amdahl V6	TT9900	COMET
Tech.	ECL	ECL Gate A.	NMOS	Bipolar
Year ↑	1.5	3	20	10?
Delay ↓	72	74	76	79
MIPS	80	16	0.2	1.0
Total Gates	600K	150K	10K	4.8K
Comps (ICs)	300K	2K	4	120
MIPS/IC	266	8,000	50,000	8,333
Comps/80 MIPS	300K	10K	1.6K	9.6K
Total Gates 80 Mip sys	600K	750K	4.0M	3.84M
# of Pc's	1	5	400	80

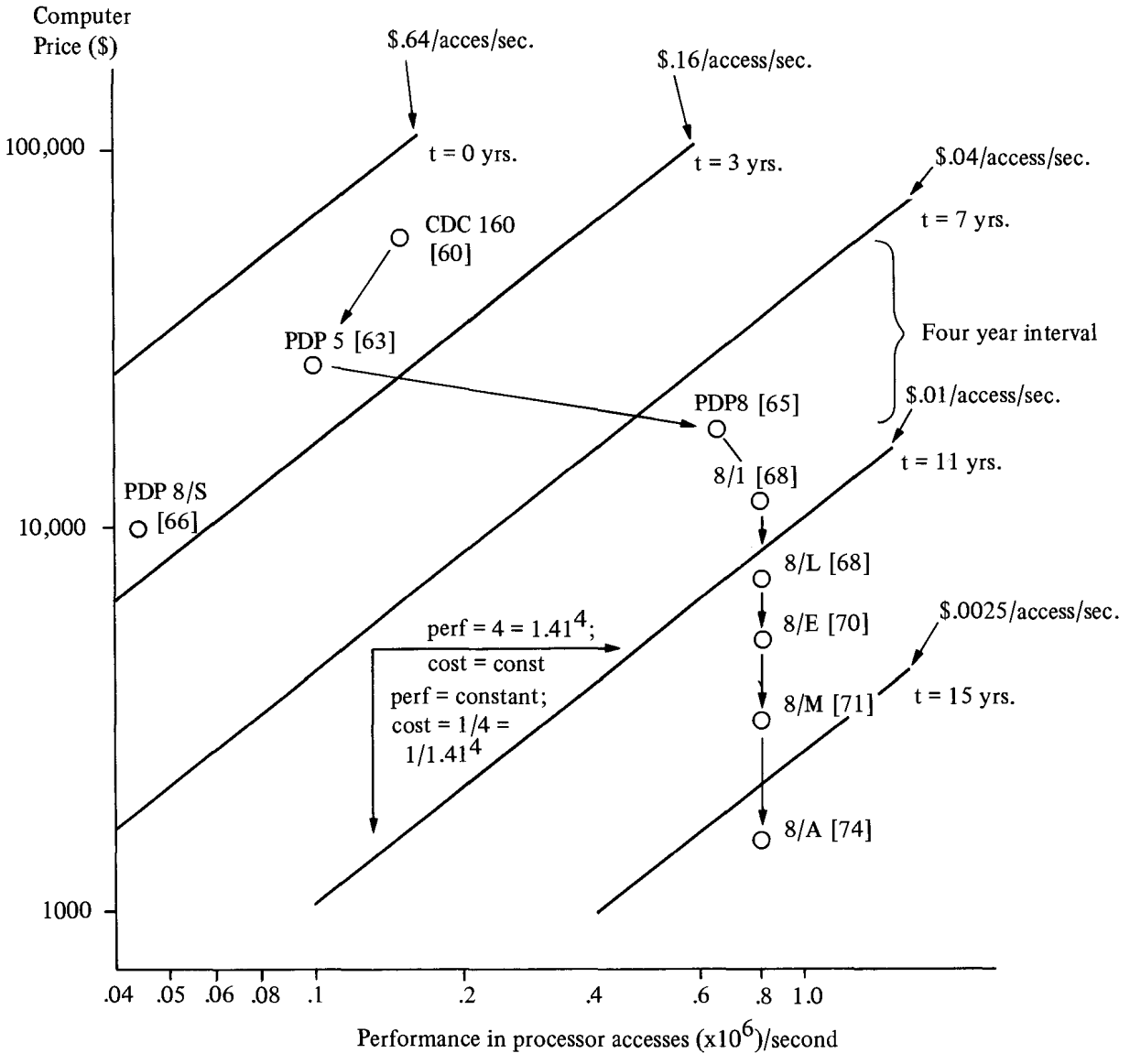
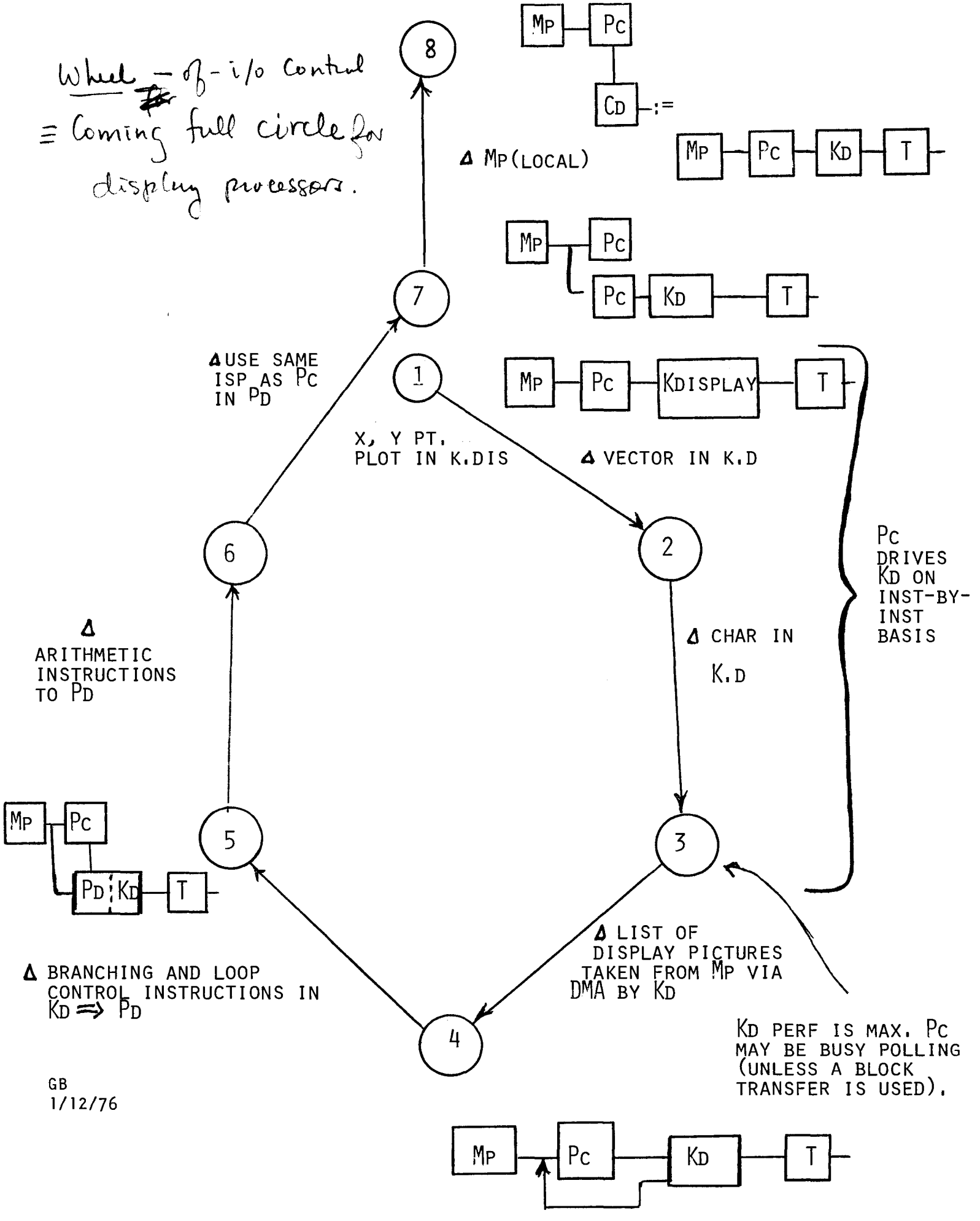


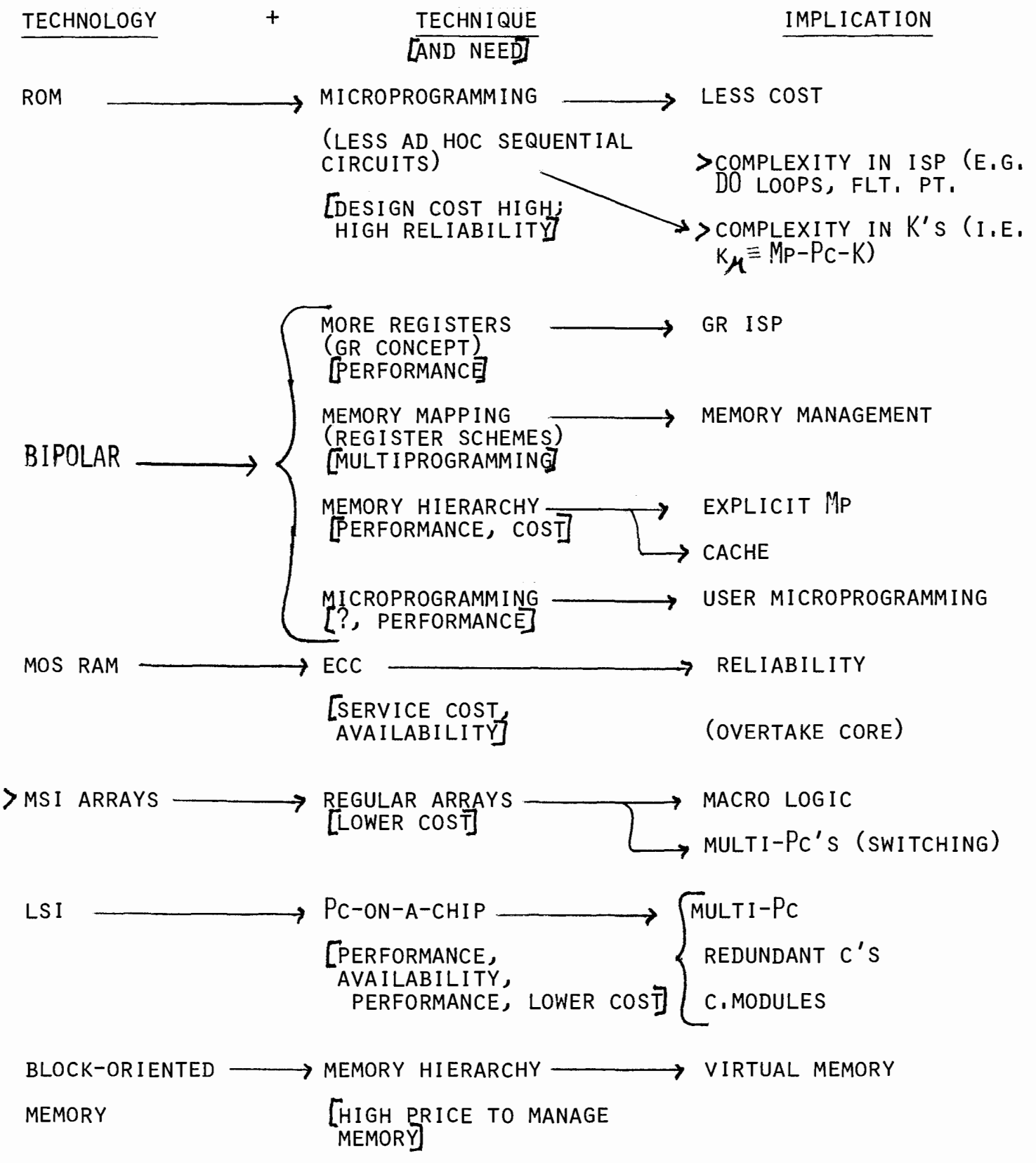
Figure 3 Minicomputer price vs. performance for various technologies. Lines of constant cost/performance ($/access/sec.) are plotted for each four year's (factor of $4 = 1.41^4$) assuming improvement of 41% per year.

Wheel of i/o Control
≡ Coming full circle for display processors.



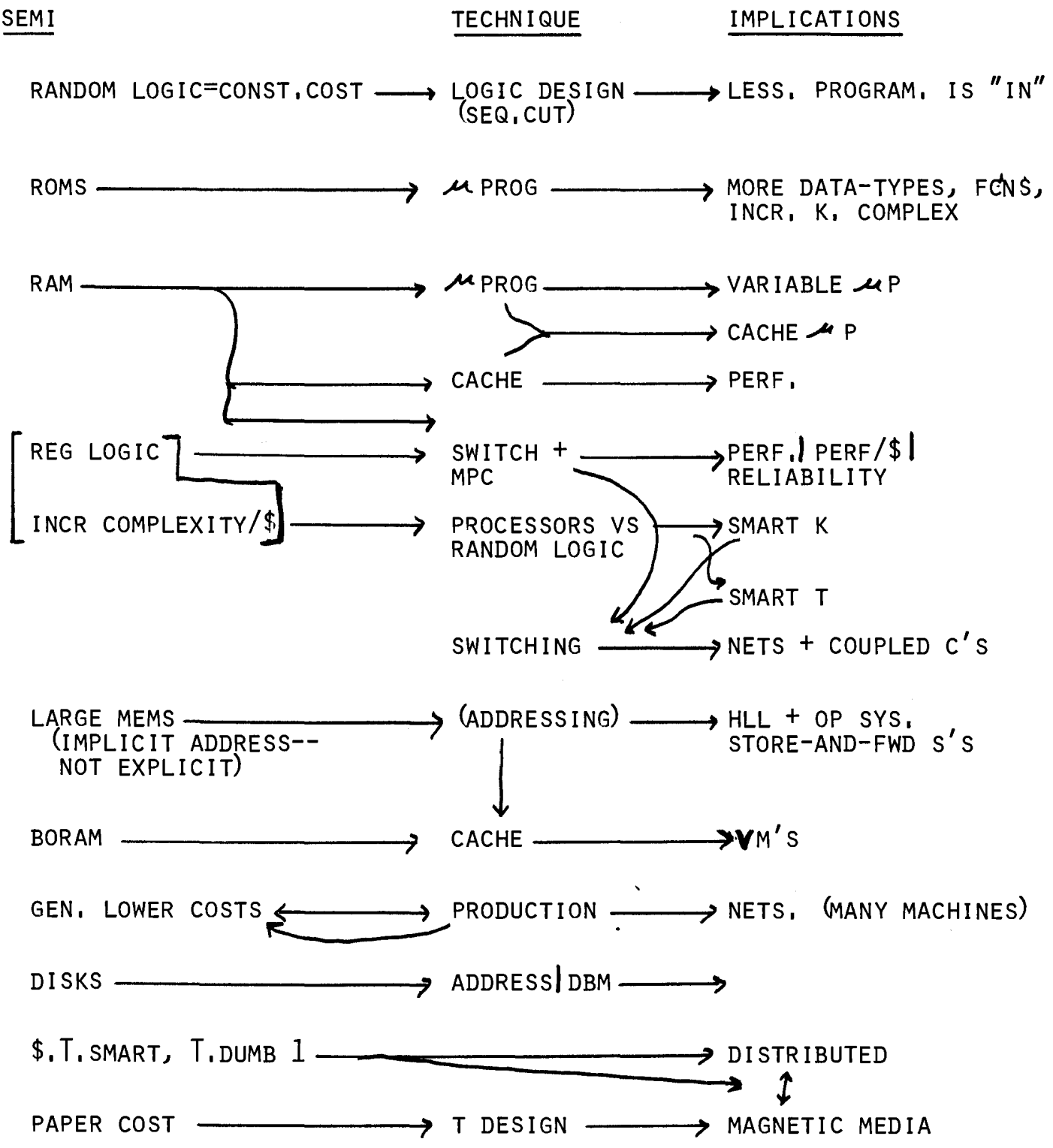
GB
1/12/76

TECHNOLOGY IMPLICATIONS



GB
1/12/75

TECHNOLOGY

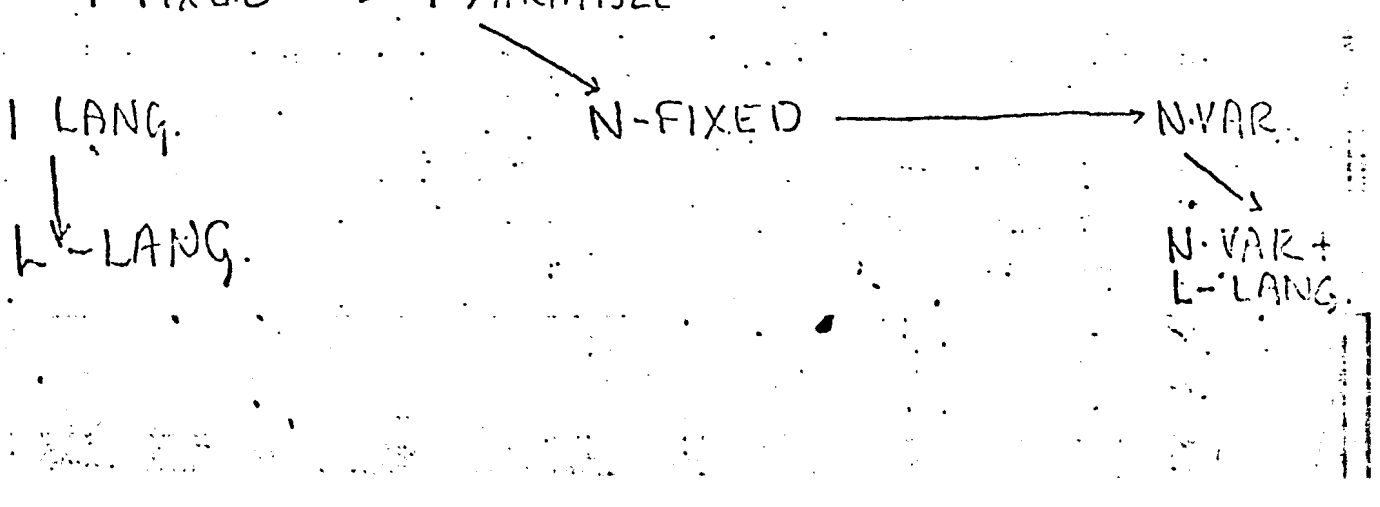


GB
2/7/75

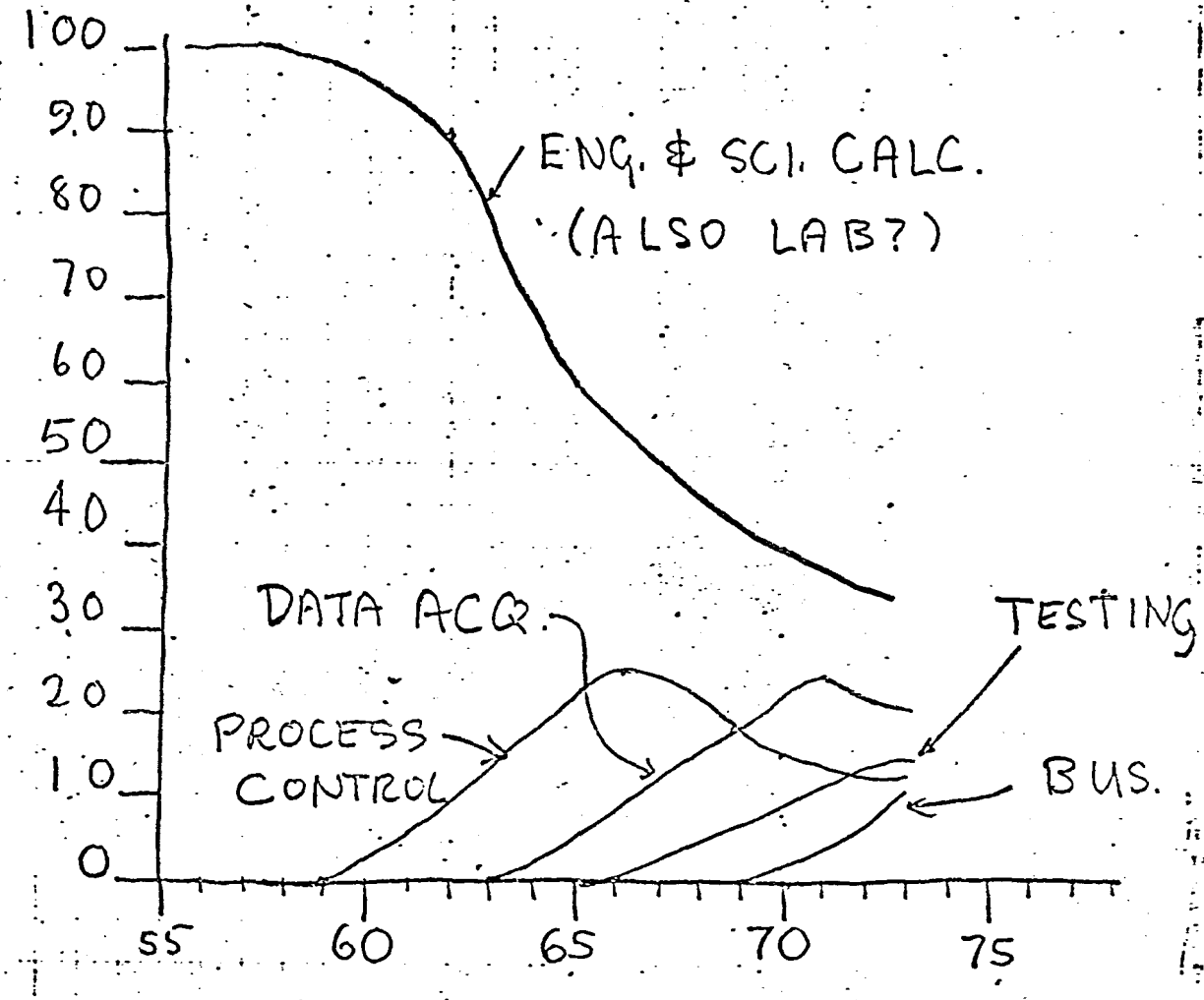
LANGUAGE/OP. SYSTEM. STRUCTURE DIMENS.

- FUNCTION ~ SCHEDULING ~ URGENCY:
  - BATCH — DON'T CARE 0 → ∞ SEC.
  - INTERACTIVE — STOCHASTIC 2 - 10 SEC.
  - REAL TIME — DEMAND .100μ - 1 SEC (GUARANTEED RESP.)
- # PERFORMING FUNCTION: 1 OR N JOBS [SUB-STRUCTURE 1 OR M PROCESSES/J.]
- DEDICATEDNESS: FIXED OR VARIABLE ~ UNCERTAINTY (PROGRAMMABILITY)
- LANGUAGE GENERALITY
  - 1, FIXED.
  - MULTIPLE, FIXED
  - MACHINE + ABILITY TO ADD MORE

INCREASING {PERFORMANCE / RESOURCE} NEEDS



Send Hus



M. PHISTER ESTIMATE OF MINICOMPUTER APPLICATIONS.

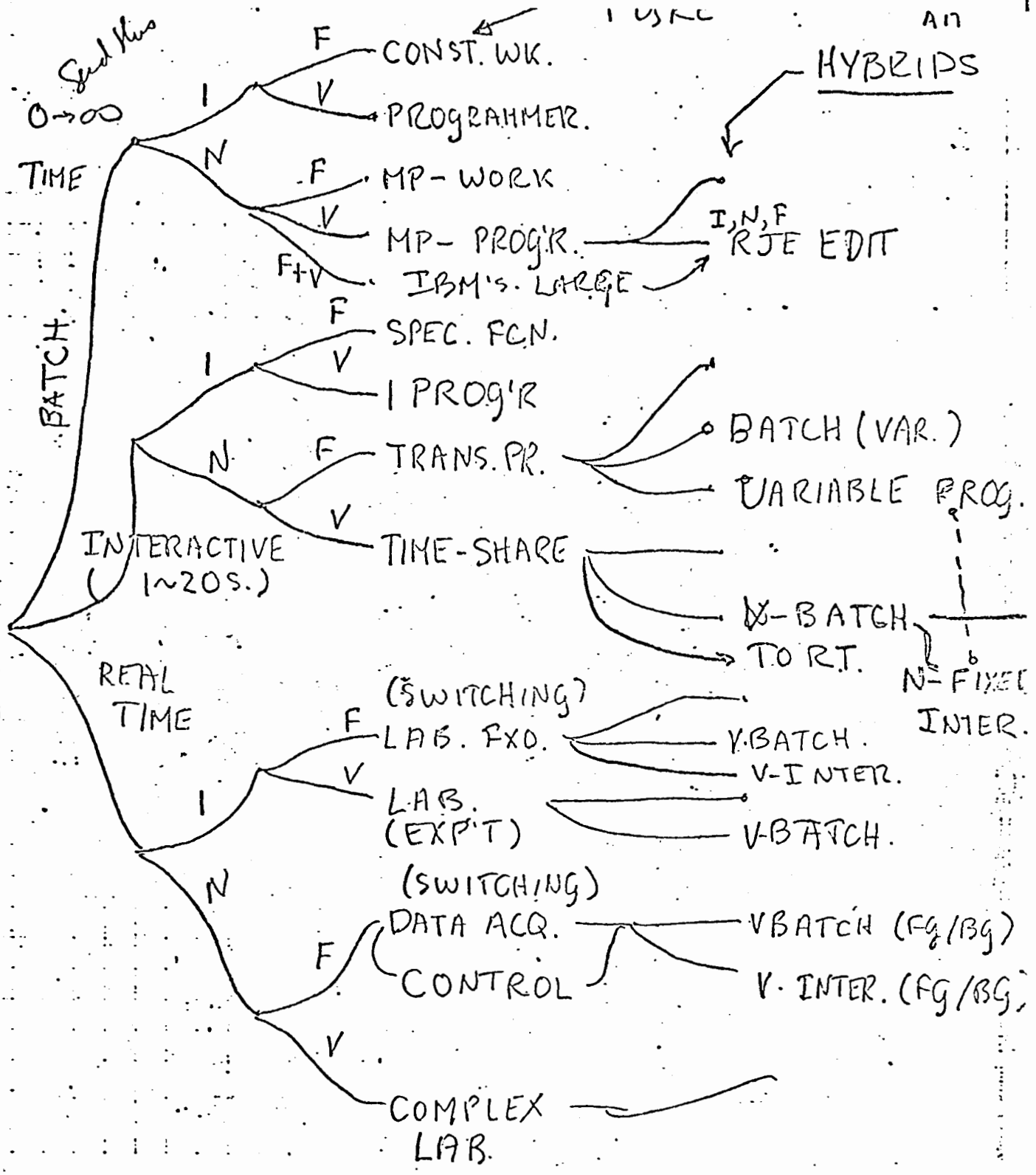
Send Hive

DEC's MKT SEGMENTATION.

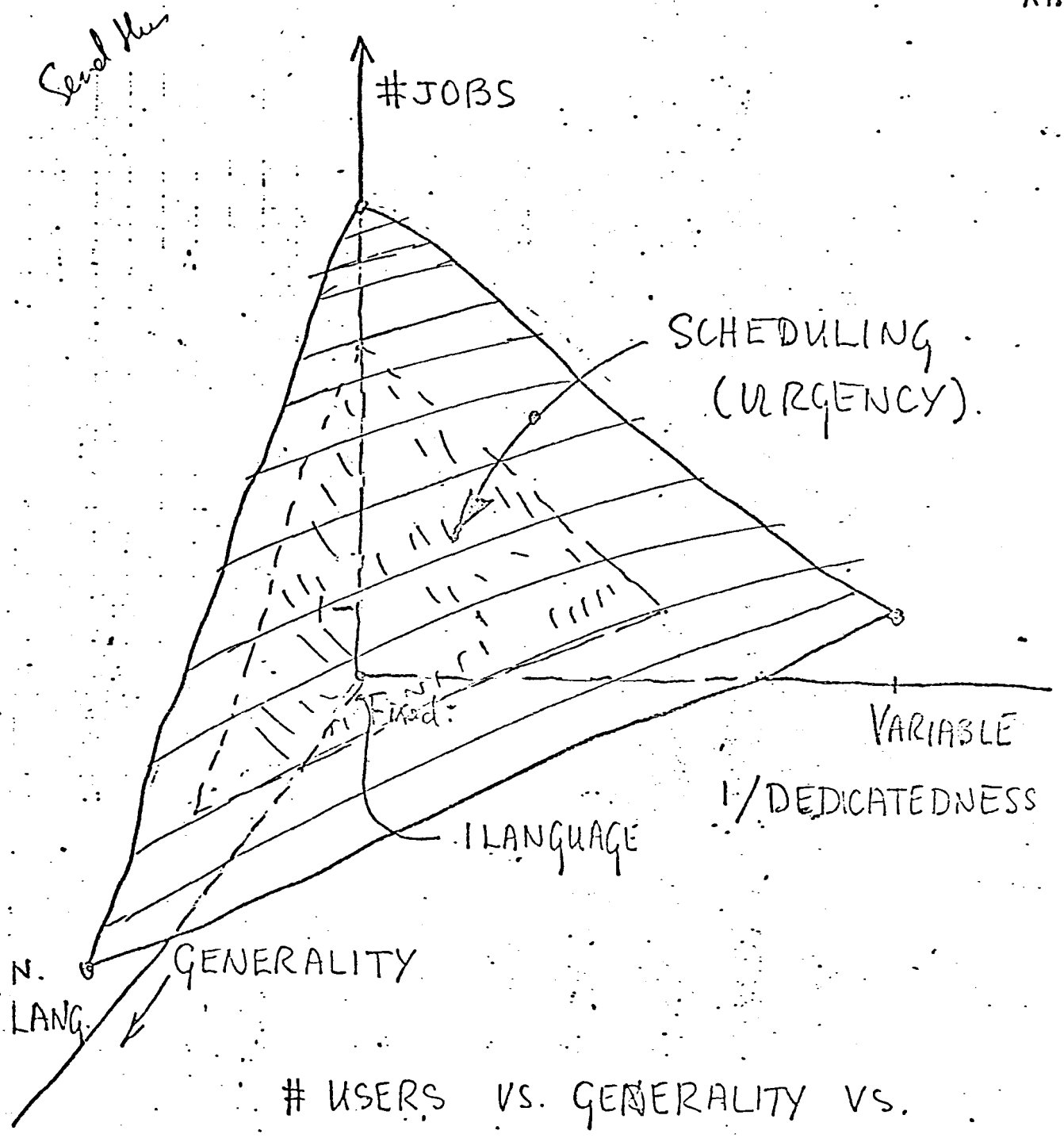
BASICS { OEM – IRON COMPONENTS/SYSTEMS
DCG – COMPONENTS (BOARD LEVEL)

END USE {
- EDUCATION.
- ENG. COMPUTATION
- INDUSTRIAL.
- BUSINESS.
- LABORATORY.
- COMMUNICATIONS.

TURN-KEY { TYPESETTING.

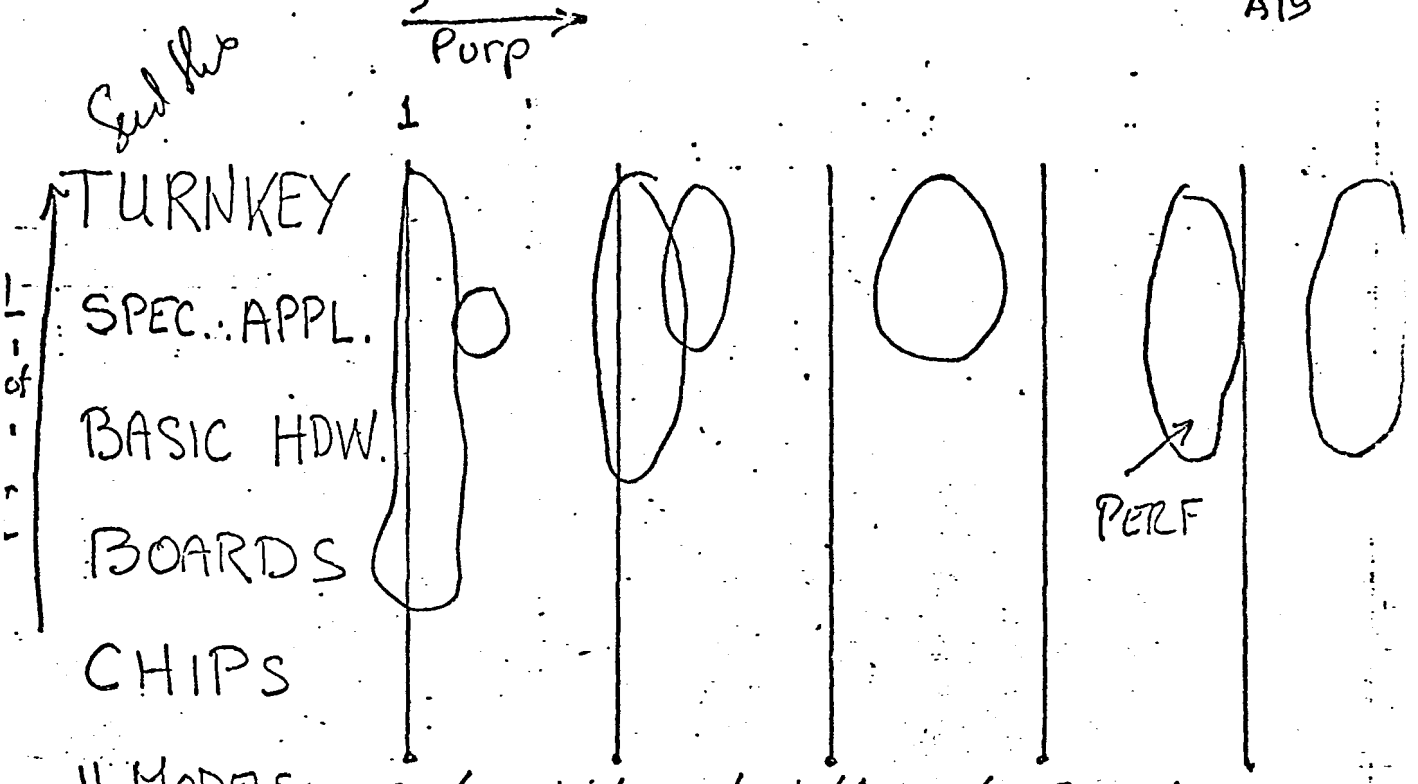


TAXONOMY OF SYSTEM STRUCTURES



USERS VS. GENERALITY VS. 1/DEDICATEDNESS FOR VARIOUS FUNCTIONAL SYSTEMS (IE. SCHEDULE URGENCY)

GB.
2/13/76



11 MODELS: 03 / 04 / 05 / 34 / 40 / 45 / 70

PRICE	.6-10	2-20	10-50	30-150	50-250
PERF. (Basic)	1	2	4	10	20
Perf. (Sci)	3	1	5	40	70
Perf ~ Price^2	1	4	25	225	625
Perf ~ Price^1	1	2	5	15	25
Mem. Size	(1) 4K-28KW		-128KW (32)		(256) 1Mw

ANCESTRY

- MINICOMPUTER ANCESTRY BEGAN WITH EDSAC.
- AEROSPACE COMPUTERS CLAIMED ANTECEDANTS.
- MINICOMPUTERS (FOR MINIMAL COMPUTERS) ARE A STATE OF MIND; THE CURRENT LOGIC TECHNOLOGY, THE CHARACTERISTICS FOUND IN LARGER COMPUTERS, COMBINED INTO A PACKAGE WHICH HAS THE COST.
- ALMOST THE SOLE GOAL IS TO MAKE THE COST LOW.
- THE HARDWARE-SOFTWARE TRADEOFFS FOR MINICOMPUTER DESIGN FAVORED SOFTWARE.

GB
1/19/76

G. Bell, Minicomputer Architecture and Design
IEEE Conference, Spring 1971

BASIC PROBLEMS IN DEFINING (CHARACTERIZING)

(MINI) COMPUTERS

TECHNOLOGY CHANGES RAPIDLY--HENCE, PRICE AND SIZE FOR CONSTANT FUNCTION DECREASES RAPIDLY.

LIFETIME (AGES) VARY AMONG COMPARISONS

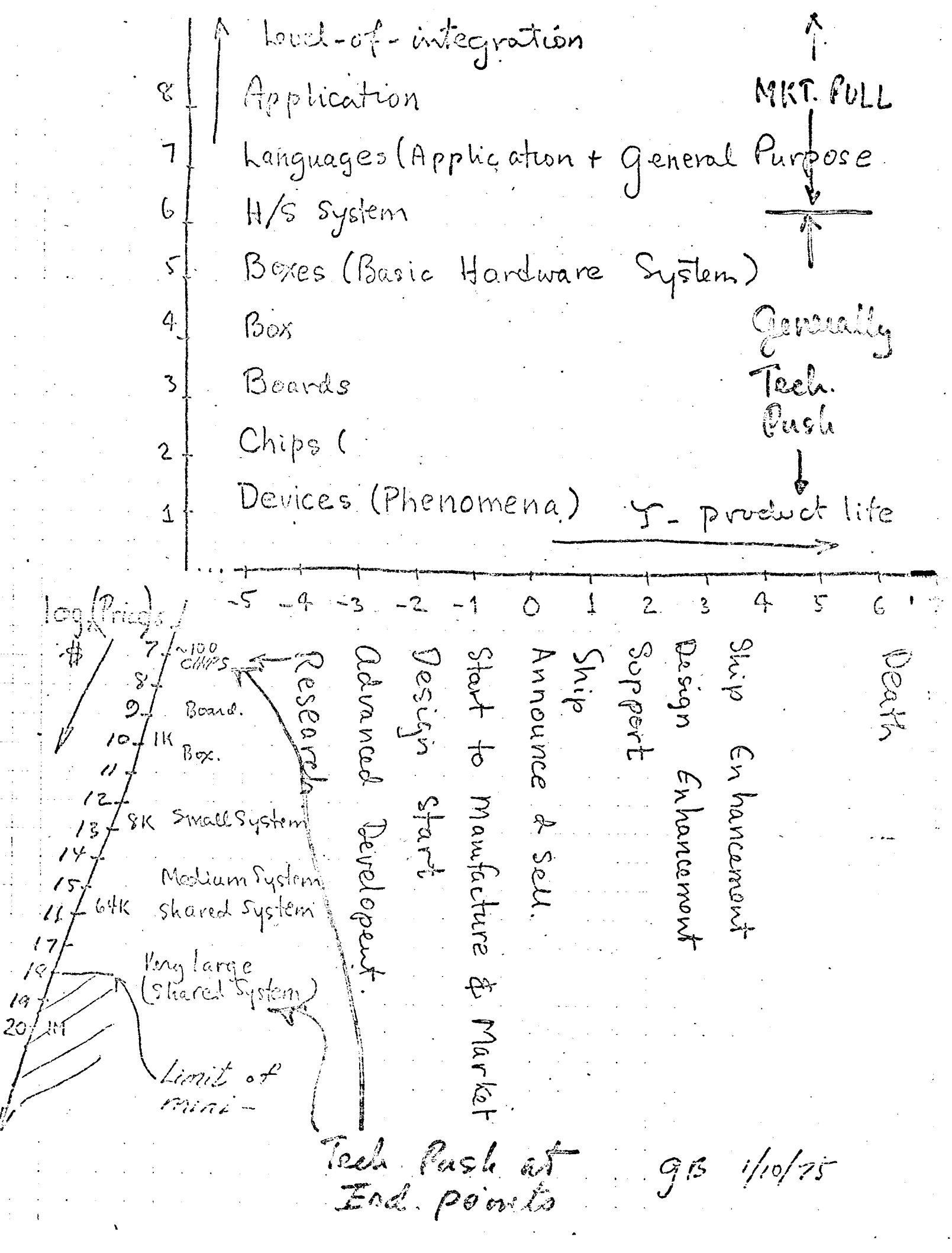
THE CONFIGURATIONS VARY WITH APPLICATION--MAKING $ FOR SYSTEM A POOR MEASURE.

MINI ANCESTRY INCLUDES: CONTROL, COMPUTATION, AND DATA PROCESSING.

WIDE IMPLEMENTATION RANGE ($ AND PERFORMANCE)

LEVELS-OF-INTEGRATION, MARKUPS AND MARKETING VARY

GB
1/26/76


level-of-integration
8 Application
7 Languages (Application + General Purpose
6 H/S System
5 Boxes (Basic Hardware System)
4 Box
3 Boards
2 Chips (
1 Devices (Phenomena)
MKT. PULL
Generally Tech. Push
Y - product life
-5 -4 -3 -2 -1 0 1 2 3 4 5 6 7
log (Price)
$
~100 CHIPS
Board.
1K Box.
8K Small System
Medium System
64K shared system
Very large (Shared System)
1M
Limit of mini-
Research
Advanced Development
Design Start
Start to Manufacture & Market
Announce & Sell.
Ship
Support
Design Enhancement
Ship Enhancement
Death
Tech Push at End points
GS 1/10/75

EVOLUTION OF IO CONTROL IN COMPUTERS

CONTROL, K EVOLUTION	COMPUTER CONTROL & PROCESSING FUNCTION
K, SIMPLE	Pc (WITH EMBEDDED K)
K (1 INSTRUCTION WITH INTERRUPTS)	Pc (INTERRUPTS & IO PROGRAM)
K (>1 INSTRUCTION)	PcIO (1 INSTRUCTION AT INTERRUPT)
K-P-Mp (LOCAL) CIO	Pc + nPIO (CHANNELS)
	mPcIO
	Pc + P. SPECIAL (E.G. P. DISPLAY)
	CIO (SEPARATE COMPUTER WITH Mp (LOCAL) FOR IO CONTROL)

GB
1/12/76

LEE `69

R = RATIO OF t.slow / t.fast.

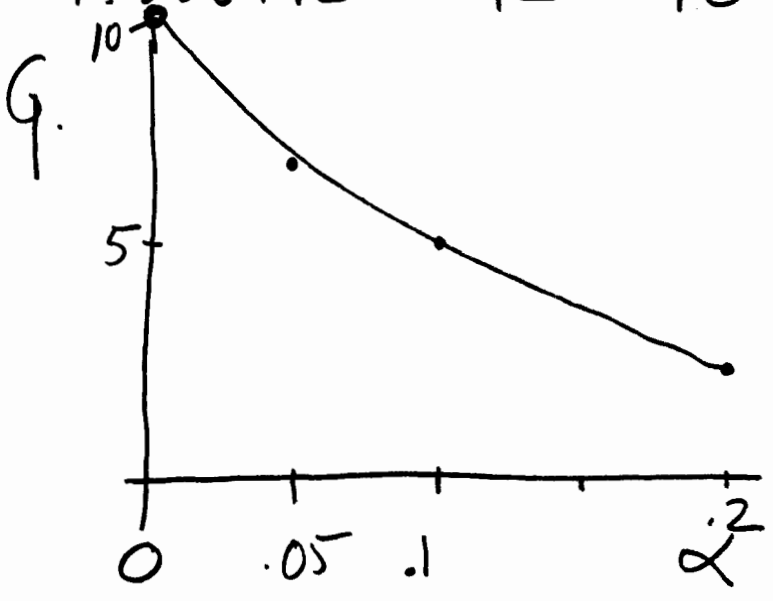
$$t(\text{No } M_c) = R \cdot a$$

$$t.(\text{cache}) = a + mR$$

$$\text{GAIN} = \frac{Ra}{a+mR} = \frac{R}{1+\frac{m}{a}R} = \frac{R}{1+\alpha R}$$

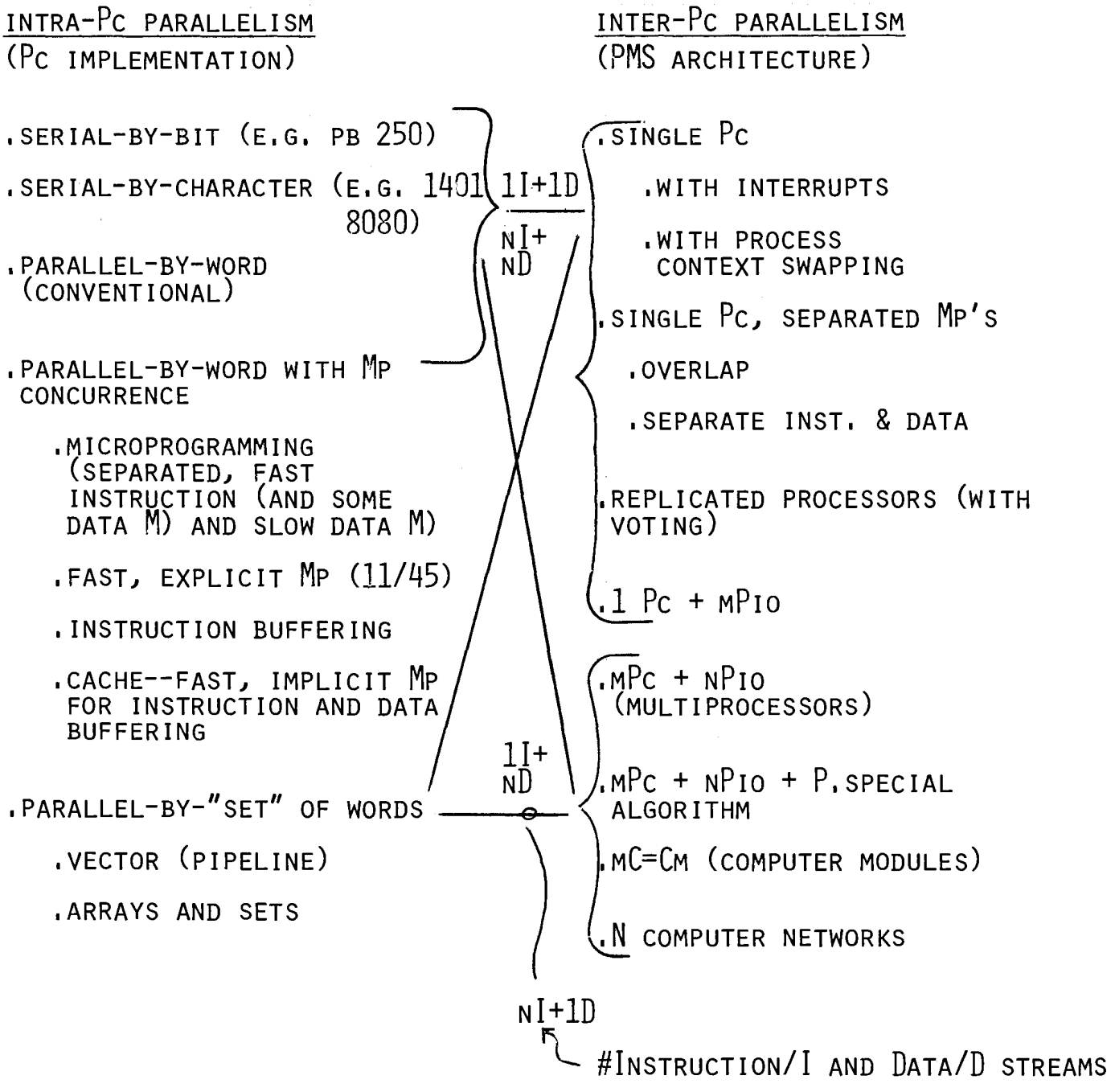
$$\frac{m}{a} = \alpha = \text{MISS RATIO.}$$

ASSUME $R = 10$



PMS-STRUCTURE DIMENSION

(FROM BELL & NEWELL)



GB
1/12/76

SEMICONDUCTOR TECHNOLOGY

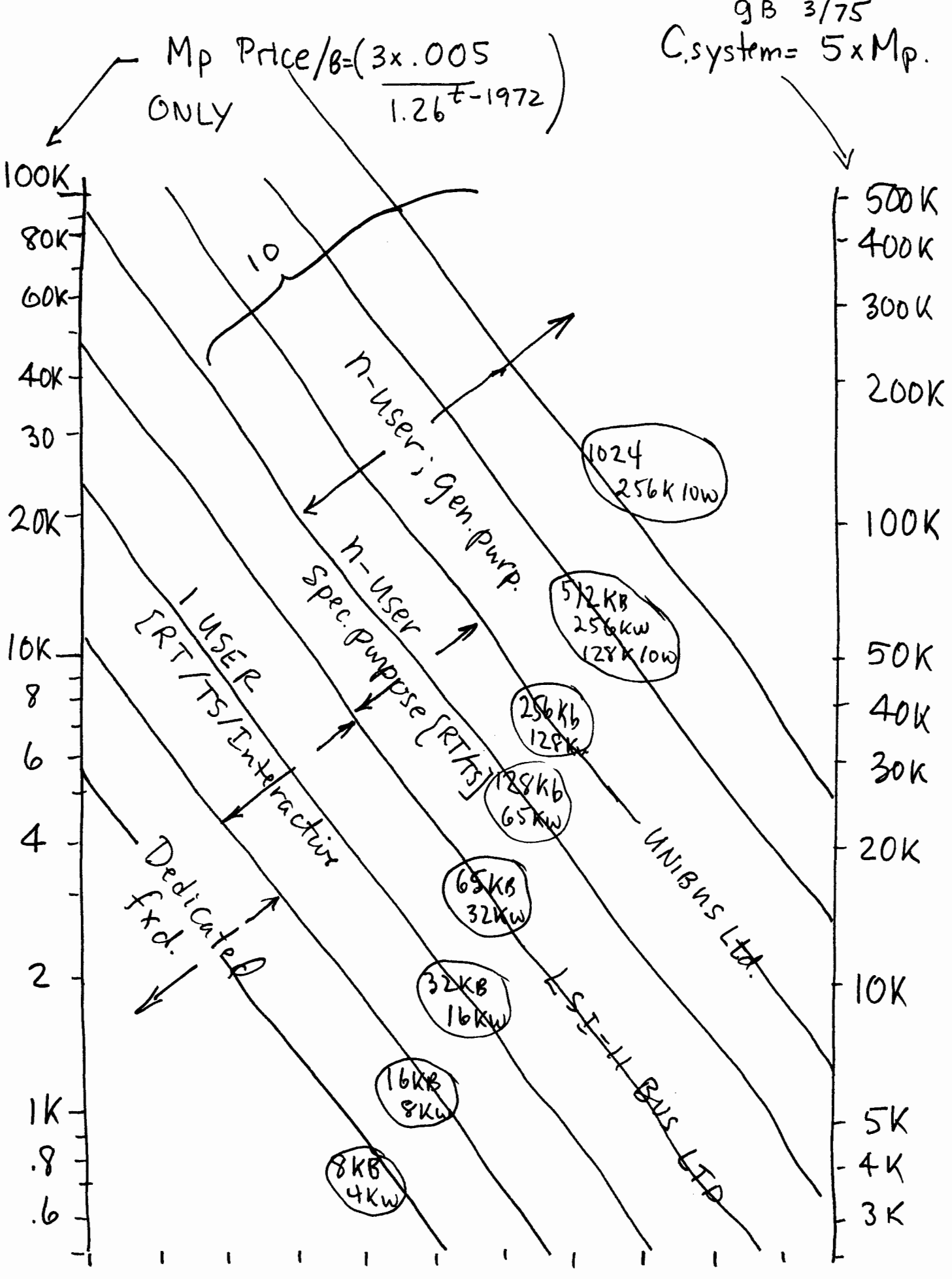
bits/die = $2^{(t-1962)}$

Bipolar read-write	lags by two years
Bipolar read-only	lags by one year
MOS read-write	--
MOS read-only	leads by one year
Production volumes	lags by 1-2 year

Technology	# Bits	Availability
Bipolar read-write	16	1969-1970
	64	1971-1972
	1,024	1975-1976
MOS Read-Write	16,384	1977-1978
Bipolar read-only	256	1971-1972
	1,024	1974-1975
	2,048	1975-1976

OTHER TECHNOLOGY

Disks (40)
Cores (30)
Terminals (25)
Magnetic tape performance (29)
Packaging and power (-3)


gB 3/75
Mp Price/B=(3x.005 / 1.26^t-1972)
ONLY
C.system= 5xMp.
100K
80K
60K
40K
30
20K
10K
8
6
4
2
1K
.8
.6
500K
400K
300K
200K
100K
50K
40K
30K
20K
10K
5K
4K
3K
10
n-user; gen. pwrp.
n-user
Spec. pwrpse [RT/TS]
1 USER
[RT/TS/Interactive
Dedicated
fxd.
1024
256K 10W
512KB
256KW
128K 10W
256KB
128KW
128KB
65KW
64KB
32KW
32KB
16KW
16KB
8KW
8KB
4KW
UNIBUS Ltd.
LSI-11 BUS LTD

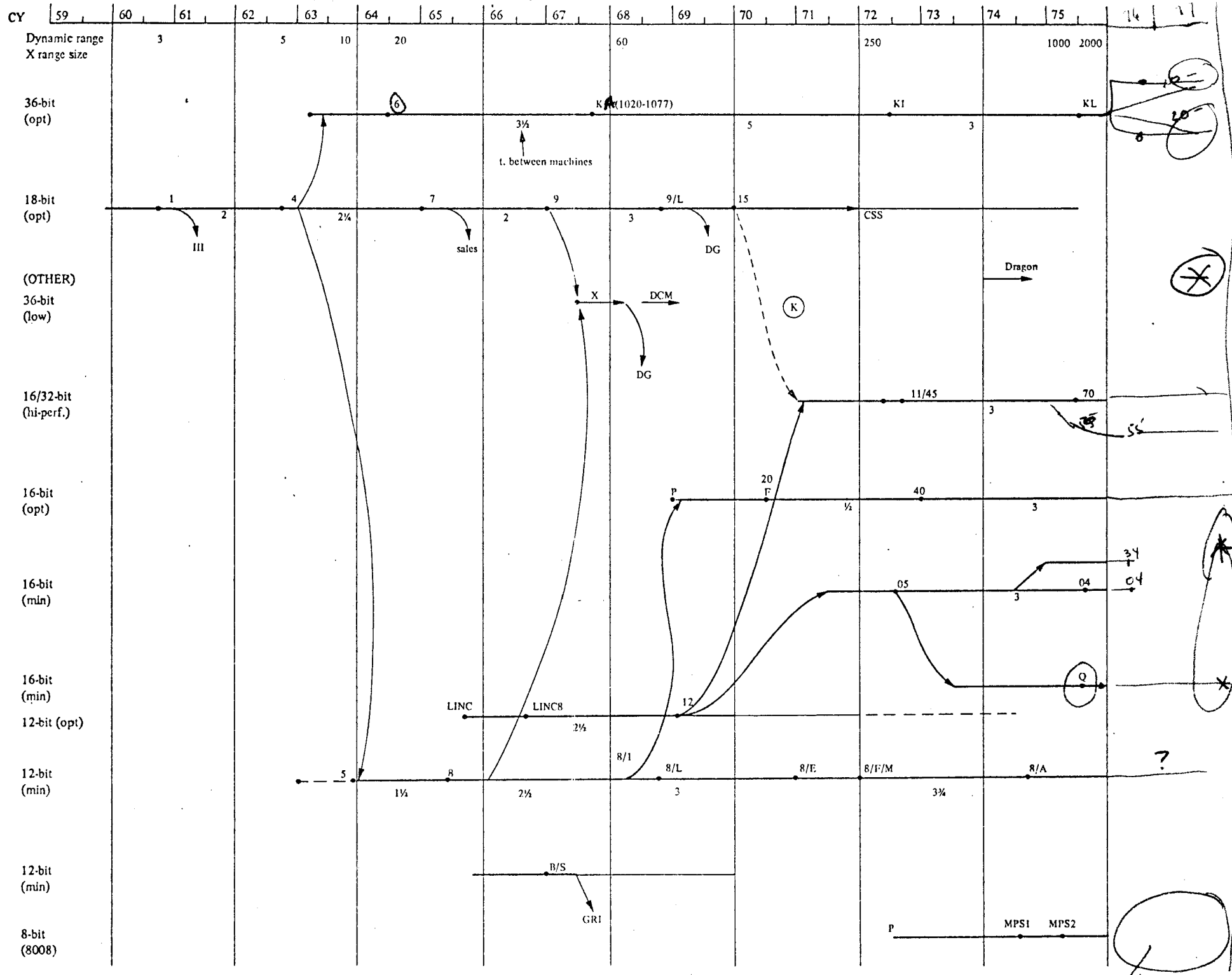


FIG. DECMACHINES. DEC MACHINES PROJECTS VS. TIME

MEM. SIZE Depends On Use.

STRUCTURE	SIZE	USE	
DEDICATED (FXD 1 USE)	16KB	Interactive. eg. POS, T	SPEC. Purp., Fxd
	4 ~ 8 KB	RT - scope, traffic, Cnto.	
PROGRAMMABLE (1 USE)	16KB - 65	Interactive - RT11	Small Scale, General.
		RT - RSX-11/M,S	
DEDICATED N-USER	65 ~ 256	INteractive - MUMPS, RSTS	Spec. Purp.
		RT RSX-11/D/M	
PROGRAM. N-USER	128K-1024K	Interactive - IAS, TOPS 10, RSTS	Compl. General
		RT	

Human Interface

Mechanical (other) Process Interface.

GB 3/75

Model	First Delivery	ROM	RAM	Machine time (n.s.)	Word length microword	# microwords	Single Prec. Flpt.	Simple arith. perf	Mp	Innovations
03 LSI-11	6/75	11.2K + PLA NMOS; 150ns	13 w NMOS; 75ns	350	22	1024	3.2	perf. 1.5	MOS (Core)	LSI - 4 chips; ODT; MAINT., FLT. PT.
04	9/75	256; 1K; 2K 50ns	4x16; 50ns	260	38	249	1.6	2.3	Mos/ Core	SIZE; ODT; MAINT./ TEST
05	6/72	256; 1K 50ns	4x16	137, 314, 630	40	249	1.4	2.1	CORE	SIZE
20	6/70	—	4x4.	—	—	—	—	—	"	ISP; UNIBUS.
34	9/75	See 04	4x16	200, 260	48	470	2.2	3	See04	SIZE; MODULARITY
40	1/73	See 05	4x16	140, 200, 300	56	256	6	2.8	Core	GP Emulation, Fl. PT.
45/	6/72		256 (MAPPING)	150	64	256	13	3.8	"	FASTEST FP/ MEM MGMT. TTL/S
55	6/72 176		256 Bipolar 1K. "	150	64	256	90	~~19.6~~ 35	Bipolar	Bipolar
70	3/75		1K CACHE	150	64	256	85	31	Core	Cache; Systems-Orient.
3001	9/75		?	170	32	512			—	Emulation.
C/D	74			?	?				—	~~WCS~~ Writeable Control Store

Machine	t.~	Word length	# words μ-code	# Hex boards	#IC's - Pc	WHET stones 1/2-Prec.	Simple Arithmetic
03 ~~(LSI-11~~	350	22	1024	1/2	61	3.2 / 1.4 ~~(1.0)~~	1.5 (1.0)
04	260	38	249	1	137	1.6 / 1.7	2.3
05	137,314,630	40	249	2	203	1.4 / 1.6	2.1
20	-?	-	-	6	523	-	-
34	200,260	48	470	2	231	2.2 / 2.3	3.0
40	140,200,300	56	256	5	417	6 / 3.6	2.8
3001	170	32	512	1	122	—	-
45	150	64	256		697	13 / 46	3.8
45 Nos	..	..	..			35 / 124	19.6
45 Bip	..	..	..			90 / 320	35
11/70	150	64	256			85 / 300	31
Cal Data	?					—	

03 LSI-11	6/75	11.2K + PLA NMOS; 150ns	13W NMOS; 75ns	MOS (Core)	LSI - 4 chips; ODT; MAINT., FLT. PT.
04	9/75	256; 1K; 2K 50ns	4x16; 50ns	MOS/ Core	SIZE; ODT; MAINT./ TEST
05	6/72	256; 1K 50ns	4x16	CORE	SIZE
20	6/70	—	4x4.	"	ISP; UNIBUS.
34	9/75	See 04	4x16	See04	SIZE; MODULARITY
40	1/73	See 05	4x16	Core	GP Emulation, Fl. PT.
45/	6/72		256 (MAPPING)	"	~~FASTEST~~ FP/ MEM MGMT. TTL/S
55	6/72 176		256. Bipolar 1K. "	Bipolar	Bipolar
70	3/75		1K CACHE	Core	Cache; Systems-Orient.
3001	9/75			—	Emulation.
C/D	74			—	WCS.

Machine	t.~	word length	# words u-code	# Hex boards	#IC's - Pc	WHET 1/2-Prec.	Simple Arith
03 (LSI-11	350	22	1024	1/2	61	3.2 / 1.4 (1.0)	1.5(4.0)
04	260	38	249	1	137	1.6 / 1.7	2.3
05	137,314,630	40	249	2	203	1.4 / 1.6	2.1
20	—?	-	-	6	523	-	-
34	200,260	48	470	2	231	2.2 / 2.3	3.0
40	140,200,300	56	256	5	417	6 / 3.6	2.8
3001	170	32	512	?	122	—	-
45	150	64	256		697	13 / 46	3.8
45 Nos	..	..	..			35 / 124	19.6
45 Bip	..	..	..			90 / 320	35
11/70	150					85 / 300	31
Cal Data	?					—	

whet [Rel] (S.P.)	
3, 2 1. ~~6~~ ~~2~~ 1.6	
- 2. ~~2~~ 3.0	

$$\text{BITS/DIE} = 2^{t-1962}$$

Bipolar	r/w	- 2 yr
"	rom	- 1 yr.
MOS	R/W	—
"	rom	+ 1
Production		- 1 ~ - 2 yr

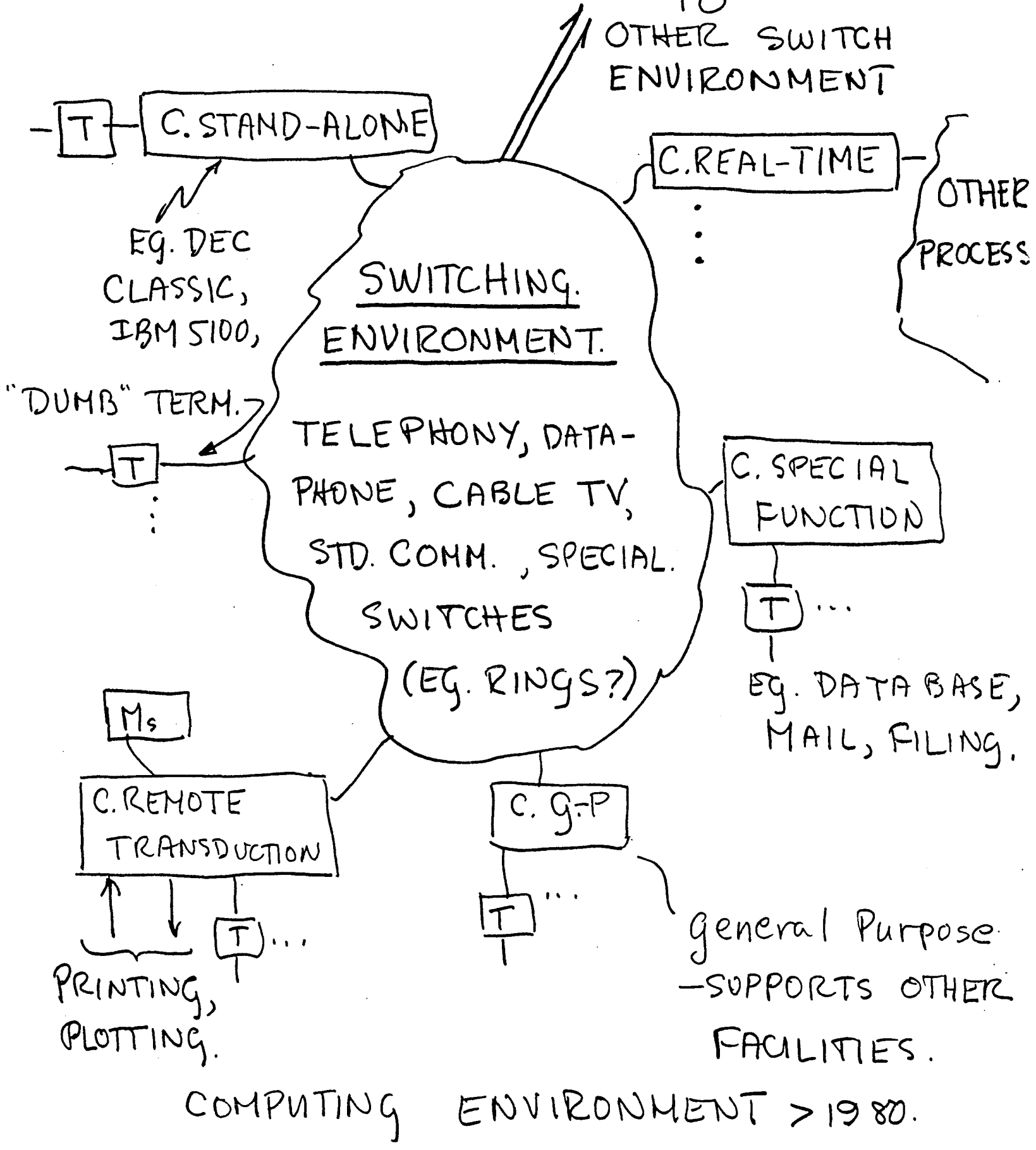
Bipolar	r/w	16	69 - 70
		64	71 - 72
		1024	75 - 76
MOS	r/w	16K	77 - 78
Bipolar	ro	256	71 - 72
		1024	74 - 75
		2048	75 - 76

COSTS (1975)

	K/YEAR	$/HR @ 2400 HR.
HUMAN	0, 5, 10, 20, 40	0, 2, 4, 8, 16
COMPUTER	1.2 ~ 2.5	.5 ~ 1.
T	.25 ~ .75	.1 ~ .4
SERVICE	.05	.02
POWER	.005 ~ .01	.002 ~ .004
LINE (COMM.)	0 ~ 2.4	0 ~ 2
PAPER	0 ~ .1	1/3 ~ .10
SPACE	.05 ~ .1	.02 ~ .04

1967	PRICE(K$)	WL	Mp.Size	$/BIT x100	MIPS × WL	MIPS (REAL)	PERF/ COST
8	10(1)	12(1)	.05 (1)	20	.3(1) (1)	.002(1)	30
6600	3K(300)	60(5)	8Mb(160)	38	3(10) (50)	3(1500)	1
1975							
11	1(1)	16(1)	4KW(1)	1.6	.3(1) (1)	.04(1)	300
LARGE	10^4 (10^4)	64(4)	1MW (10^3)	16	100(10K)(40K)	100(2500)	10

LARGE & SMALL MACHINES
1967 & 1975



COMPUTING ENVIRONMENT > 1980.

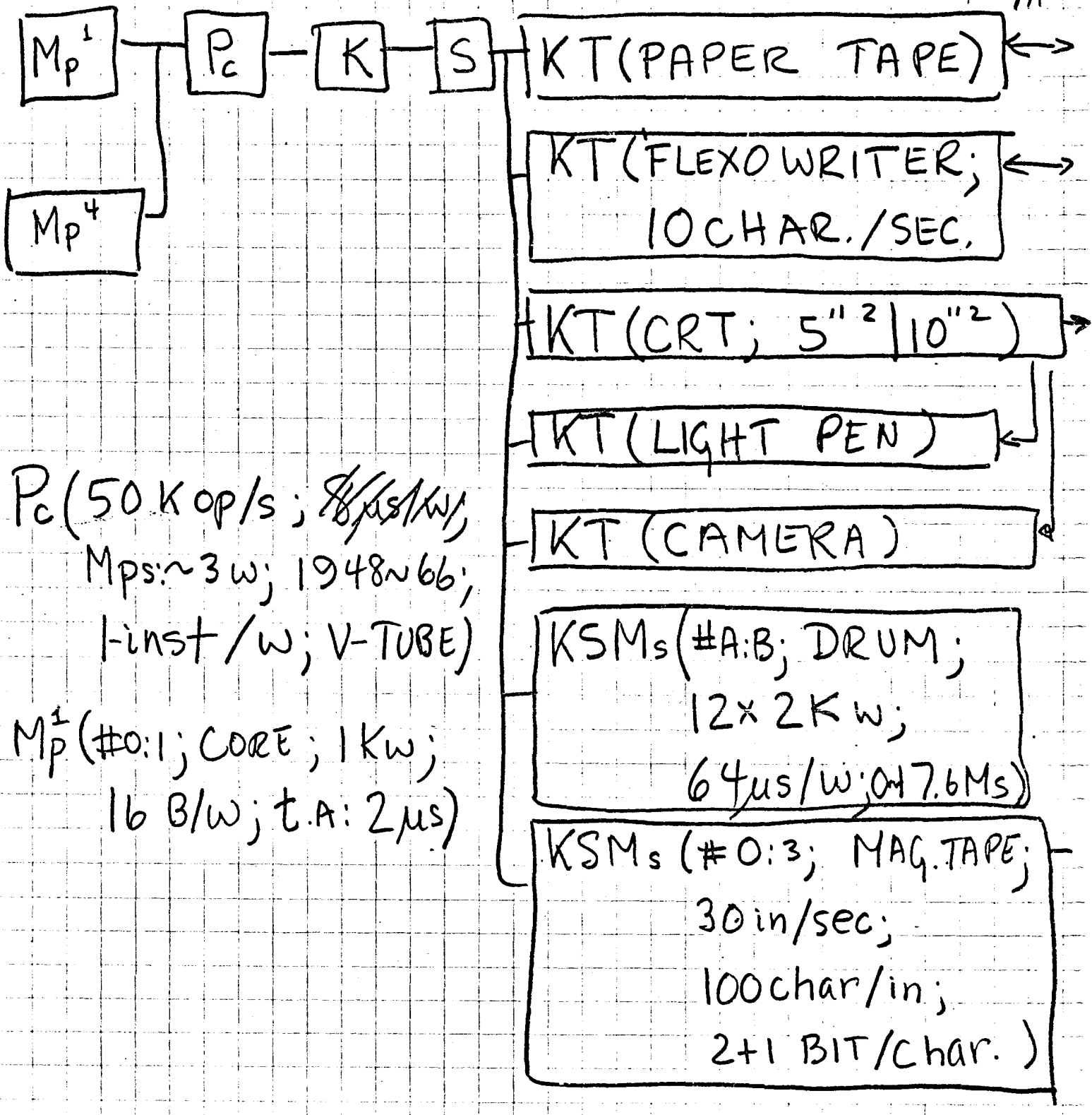
	SMALL (DECENTRAL.)	LARGE (CENTRAL)
PERF.	• > AVG.	• >> PEAK. • > Mp. PEAK.
COST	• EC. THROUGH PROD.	• ONLY DISK EC. OF SCALE
	• f (COMM. COSTS, UTILIZATION).	
	• PRODUCTION LIMITED	• DESIGN LIMITED
	• OVHD HIDDEN — USER IS SYSTEMS PROGRAMMER	
USE	• SMALL (OR 0) DATA BASE	• LARGE DATA BASE
	• FIXED, WELL-DEFINED COMPUTATION (EG. TEXT, CAI, STAT. CALC.)	• FULLY GEN. PURP.
SECURITY	• PRIVATE	• EASY TO SHARE, BREAK.
RELIABLE	• DIST.	• CENT + COMM.

C. SYSTEMS PROBLEMS

- CHARACTERIZING COMPUTATION
- ISP SELECTION/DESIGN
- USER ARCHITECTURE
  BASIC MACHINE SELECTION, CONFIG's
- MANUFACTURER ARCHITECTURE
  MODELS, CORRECT CONFIGS, PERF
- MEMORY HIERARCHY MODEL
- OP. SYS. SPECIFICATION, DESIGN, MODELING
- BUS (SWITCH) SPECIFICATIONS.
- STANDARDS FOR PORTABILITY.
  (LANGUAGES, PROTOCOLS, LOW-LEVEL PRIM.)
- UTILIZATION OF MULTIPROCESSORS.
- COMPUTER MODULES.
- COMPUTERS THAT WON'T FAIL.

SYSTEM COSTS

	PURCHASE (K$)	COST/USER/YR
DESK CALC.	5	1.3
IBM 5100	17	4.4
DEC CLASSIC	10	3
SMALL (8) USER	50	2.8
MID (32) USER	100	1.4
LARGE GP-MINI (20/50)	250	2.2~5.5
DEC 10	750	6
50 USER LARGE	3000	20



P_c(50 Kop/s; ~~8μs/w~~;
Mps: ~3w; 1948 ~66;
1-inst/w; V-TUBE)

M_p^1(#0:1; CORE; 1Kw;
16 B/w; t.A: 2μs)

MIT WHIRL WIND I BLOCK
(PMS) DIAGRAM.

Feustel 1973 - Tagged Arch.

Arith: Int, Real., Long Int., Long Real, Complex, long Compler, Mixed

Structure: Vector, Matrix, Matrix (Arith.) Sparse Vector.

Structures: Q, double/single linked List, Stack,

Process: Semaphore, Event, Message, Interrupt-Of., I-d.

Procedures: Proc, Name of Var, formal, Label, Reference to, Paramete-Set

Undefined, Garbage

Machine State and Instructions

File

CHAR, BOOLEAN

BALANCING P_c — M_p — I/O (BUSSES)

BUS OPTIMALITY (AMDAHL'S CONST's)

1 Byte of Mp = 1-$\dot{i}$/sec (use 2)

1 Bit of (i/o) = 1-$\dot{i}$/sec

---

1 $\dot{i}$ = 3~5 bytes of accessing.

1 $\dot{i}$ = 4~6 bytes with i/o.

UNIBUS $\approx$ 2 Mbytes/sec.

$\approx$ 1/2 ~ 1/3 MEGA.-INST./SEC.

~~LIMITED~~ VIA BUS.

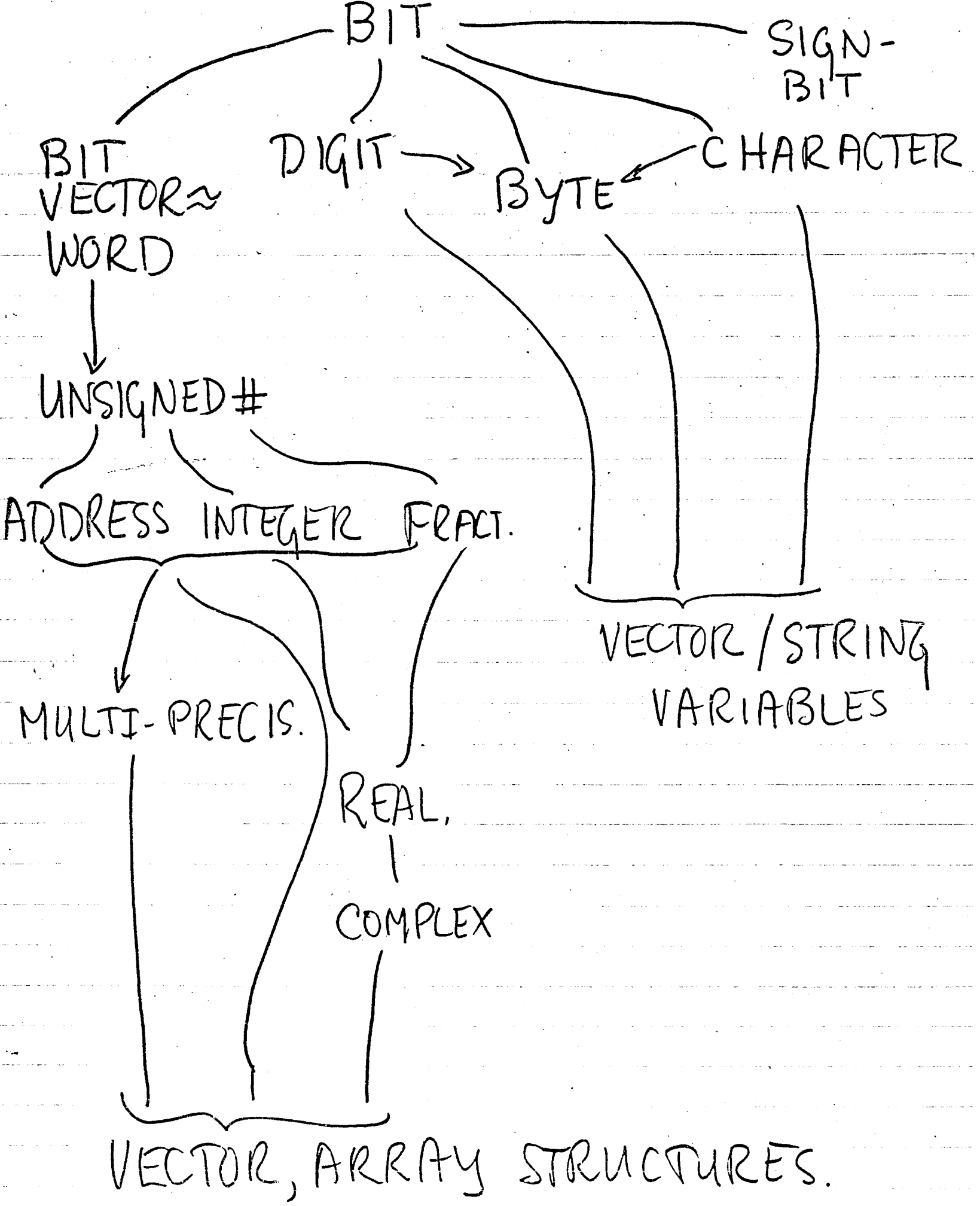
1/2 ~ 1/3 MEGA BYTES ARE REQ'D

UNIBUS = 1/4 MEGA BYTES.

11/70 $\approx$ 2 Mbytes. $\Rightarrow$ 2 Mips.

CACHE ACTS TO REDUCE BW.

R.22 DOM17


BIT
SIGN-BIT
BIT VECTOR≈ WORD
DIGIT
BYTE
CHARACTER
UNSIGNED #
ADDRESS
INTEGER
FRACT.
VECTOR / STRING VARIABLES
MULTI-PRECIS.
REAL,
COMPLEX
VECTOR, ARRAY STRUCTURES.

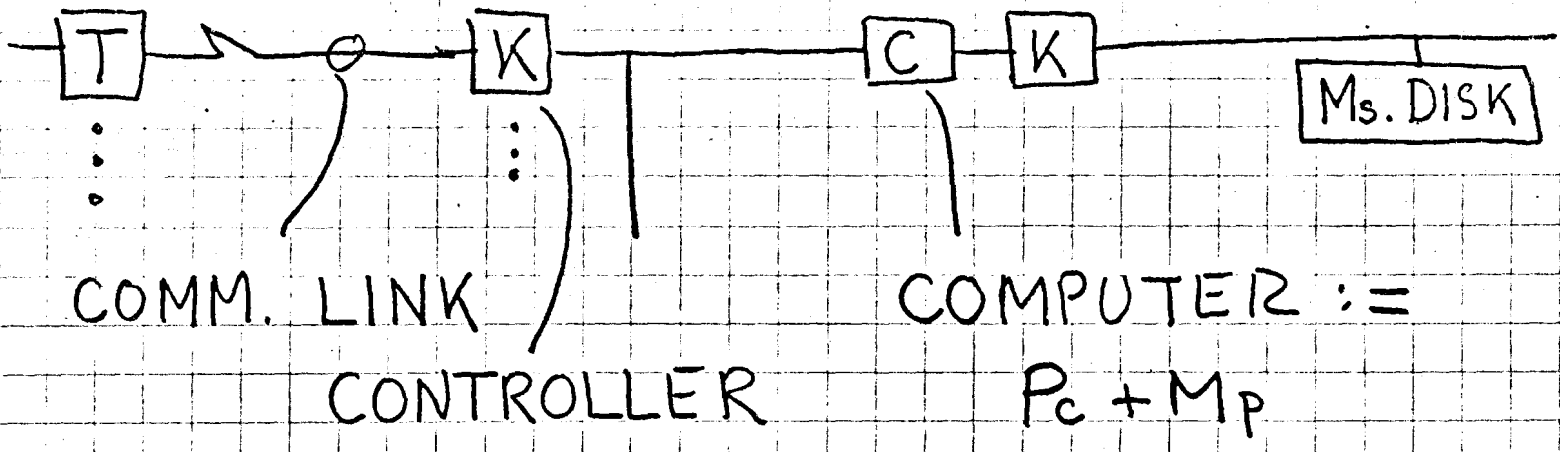


FIG1. BASIC COMPUTER, 1 SITE (MULTIPLE TERMINALS) - ACCESS TO DATA BASE

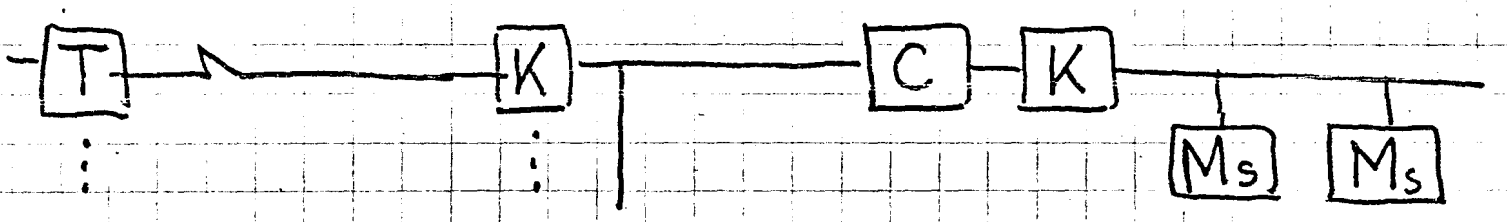
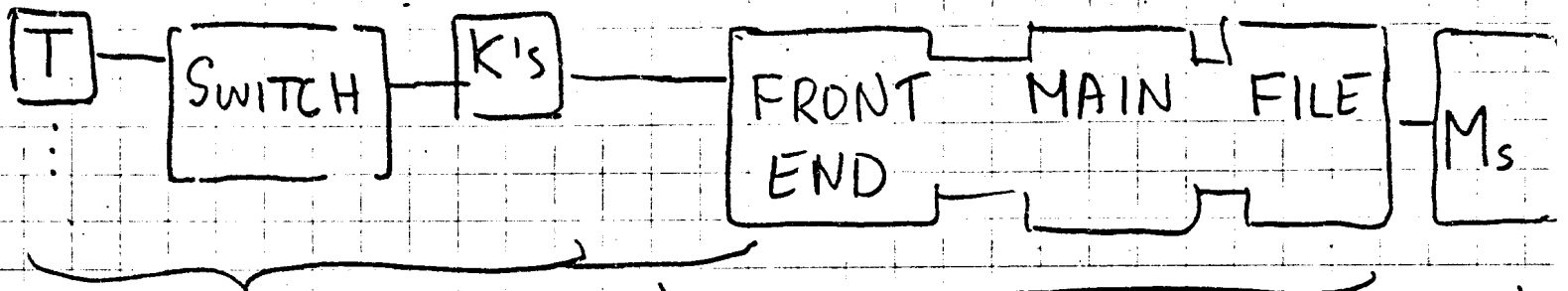


FIG2. BASIC C, 1 SITE, REDUNDANT DISK.



T-K-C

Cfe-Cm-CM's

C-Ms.

PROBLEM INTERCONNECTION

STRUCTURE

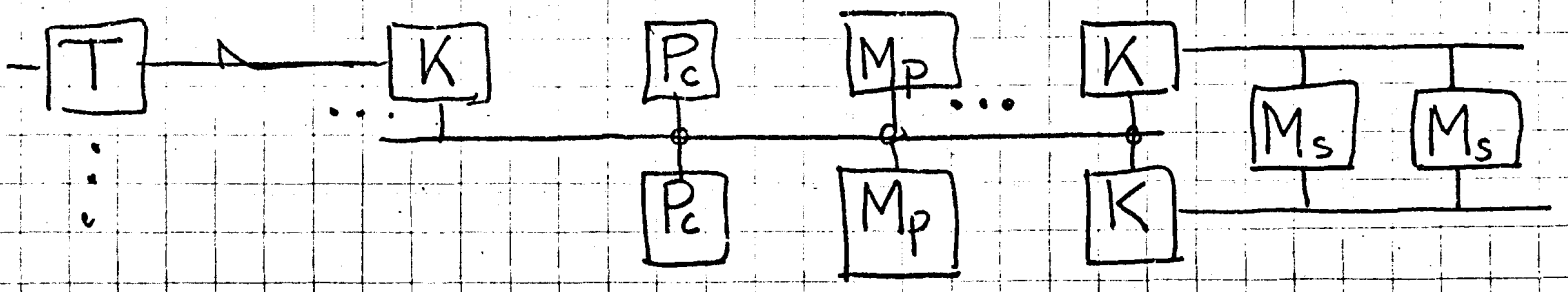


FIG 3. 1 C, 1 SITE WITH N+1 (REDUNDANT) RUNNING COMPONENT

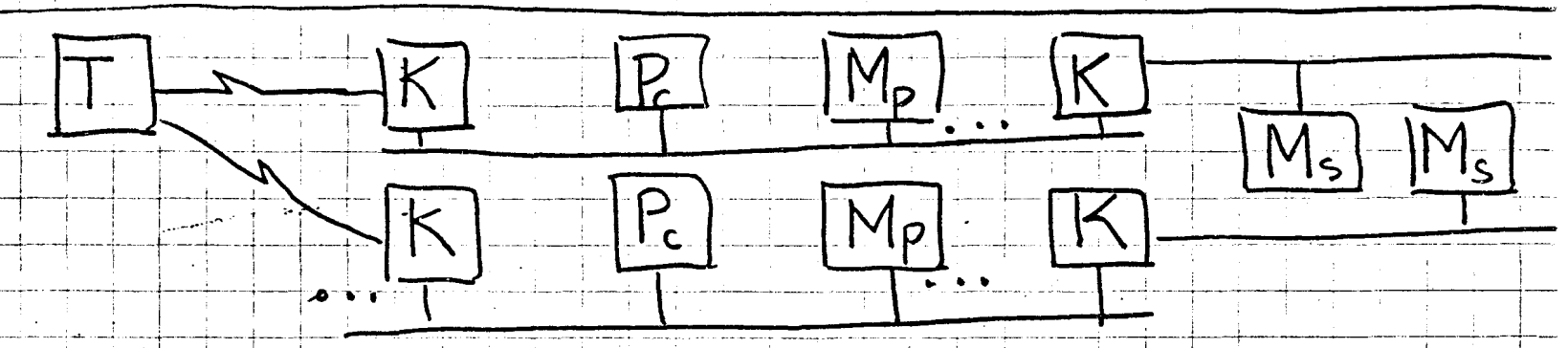


FIG 3A. 2C, 1 SITE WITH COMPLETE REDUNDANCY.

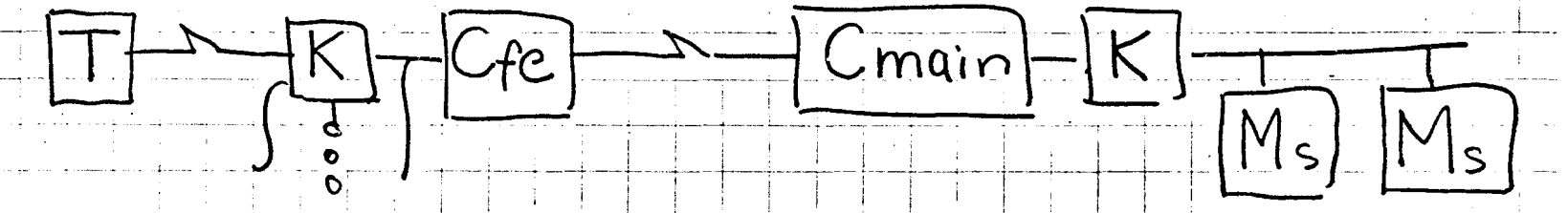


FIG 4. N := Cfe + Cmain ;
1 OR 2 SITES.

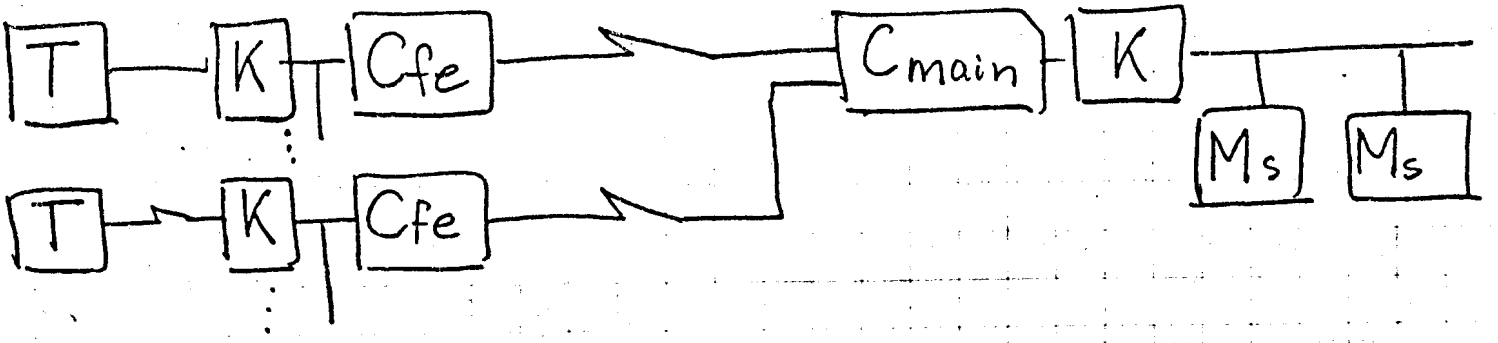


FIG 5. N := 2Cfe + Cmain ; 1, 2 or 3 SITES

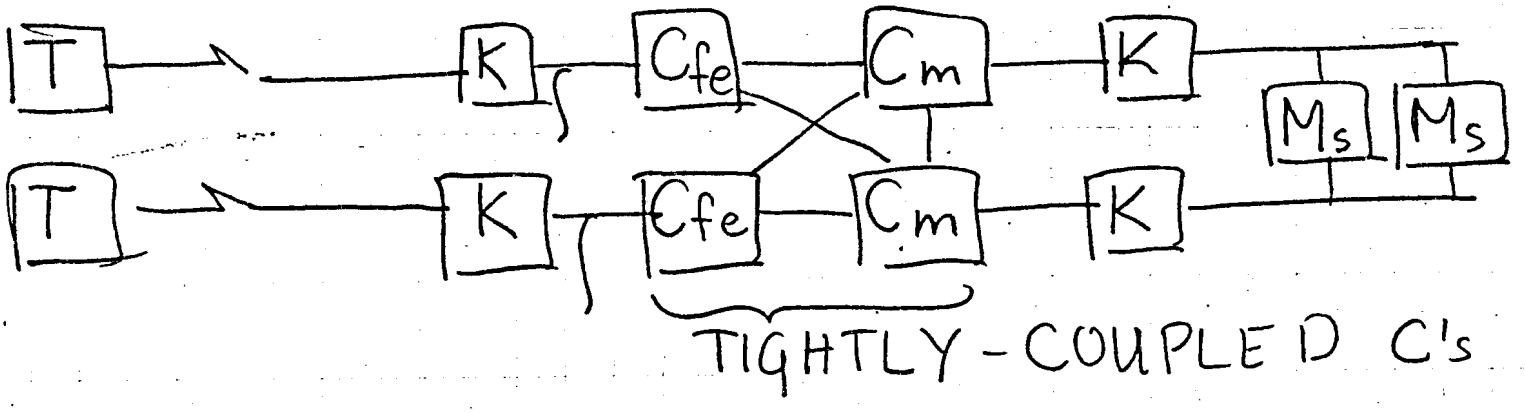


FIG. 13 Cm Structure, 1 SITE

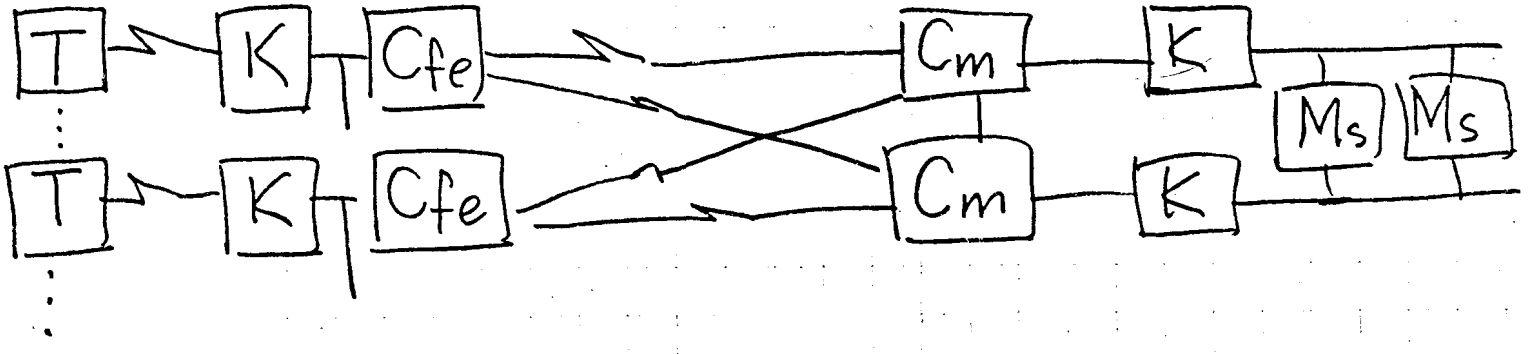


FIG. 12. N-Cm Structure ; 1~3 SITES

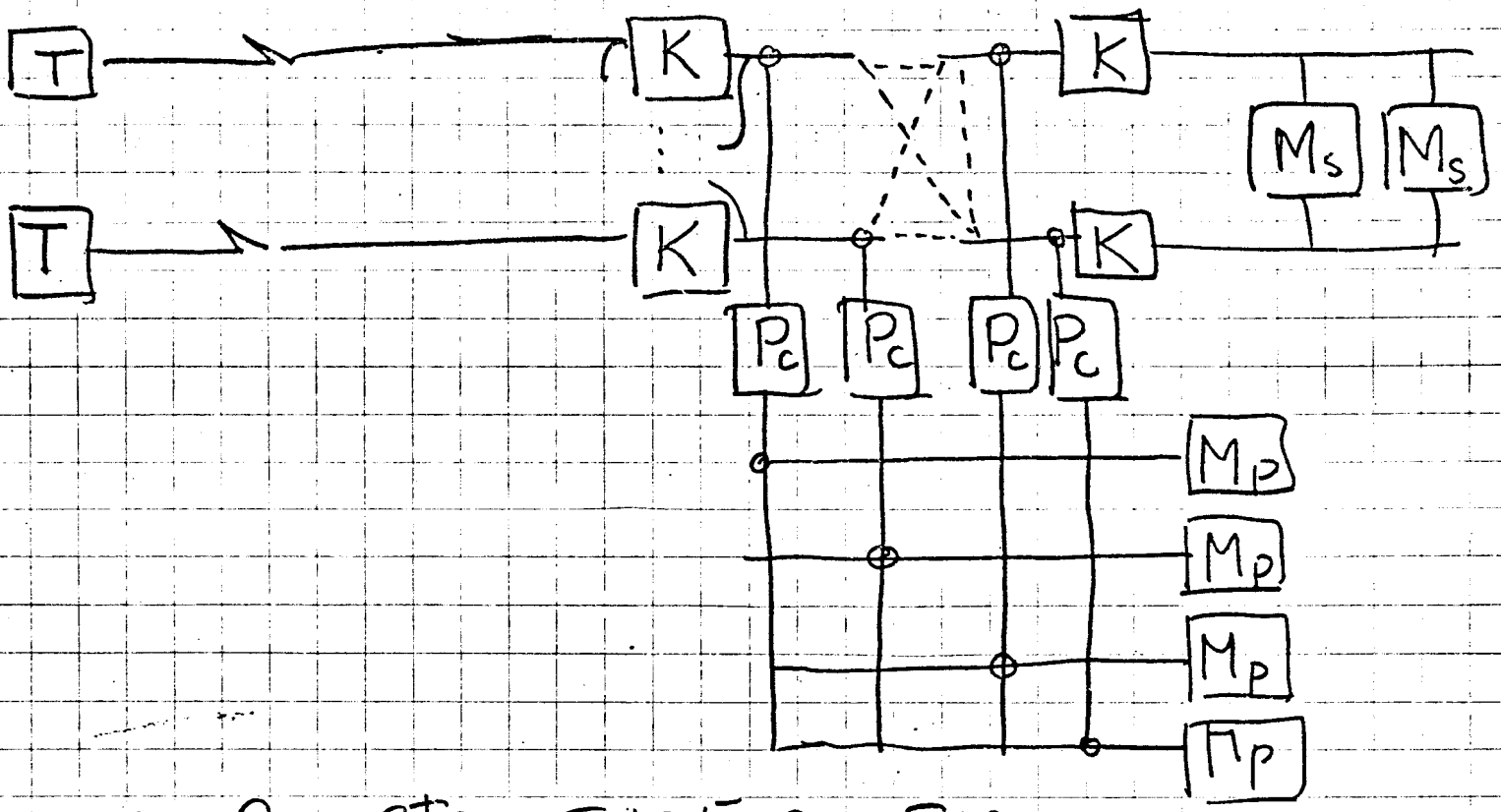


FIG 14. Cm STRUCTURE ≈ FIG 13.

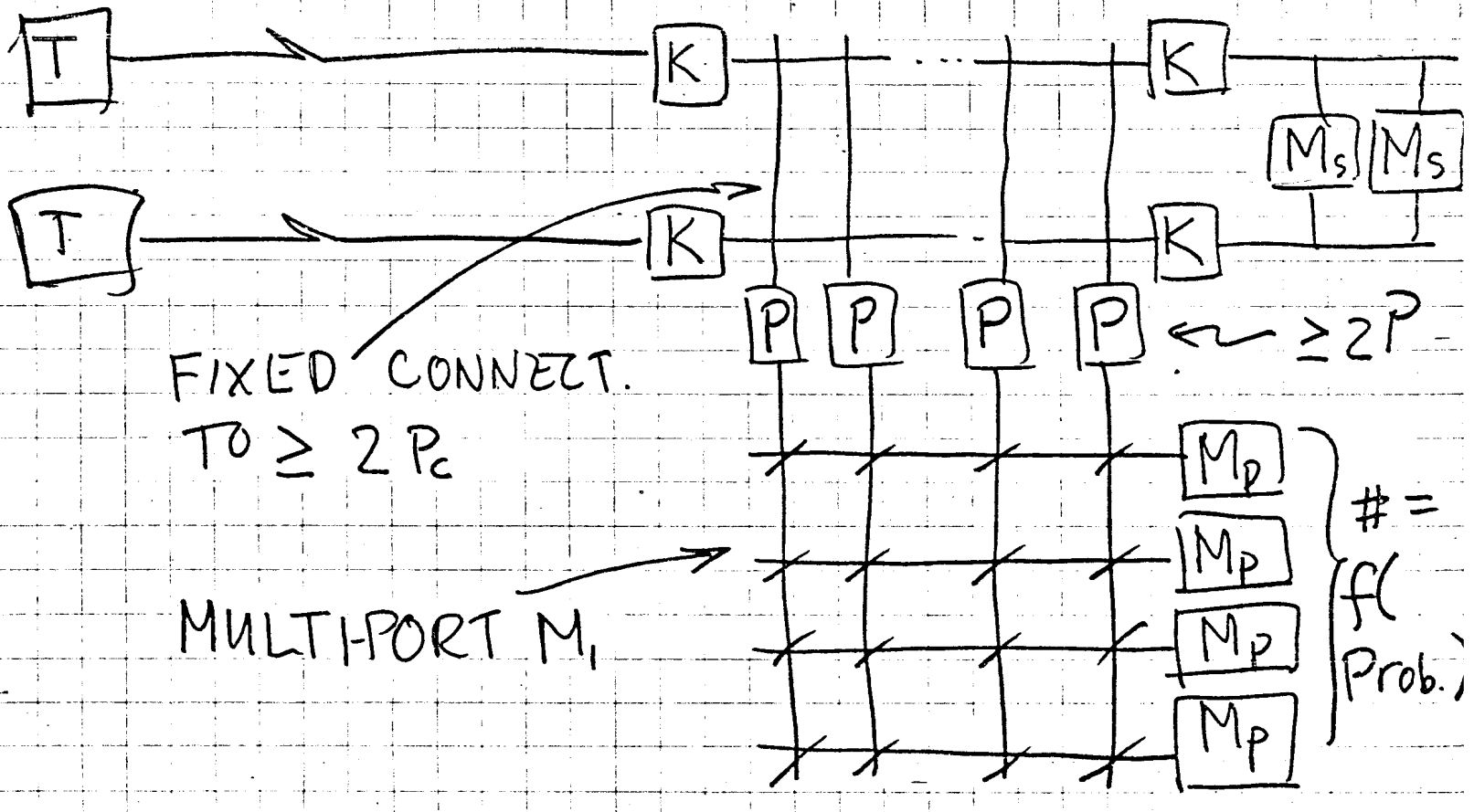


FIG 15 Pc (MULTIPROCESSOR)

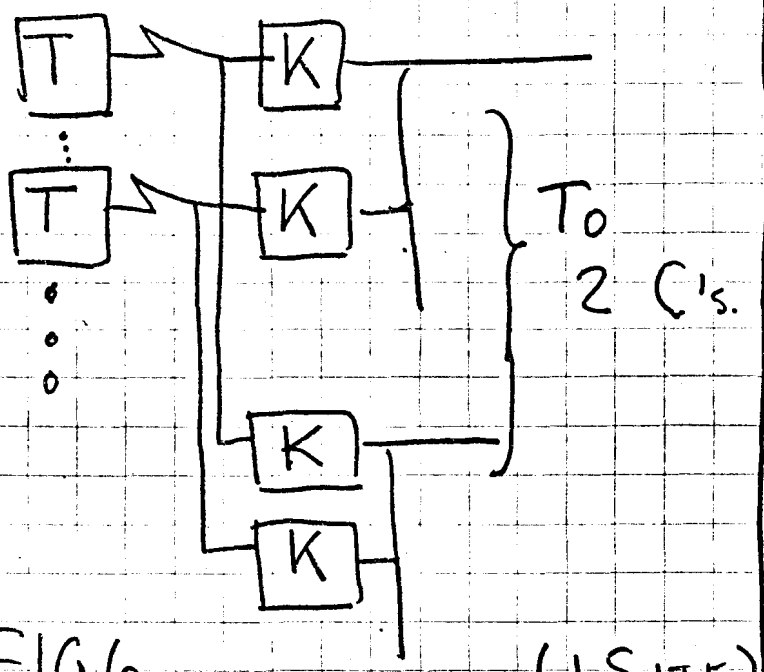


FIG 6. (1 SITE)

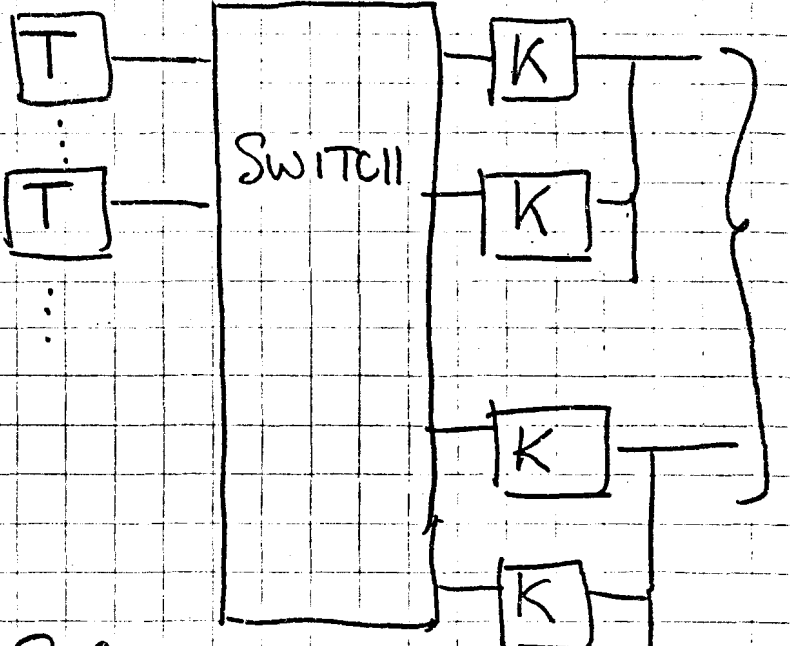


FIG 7.

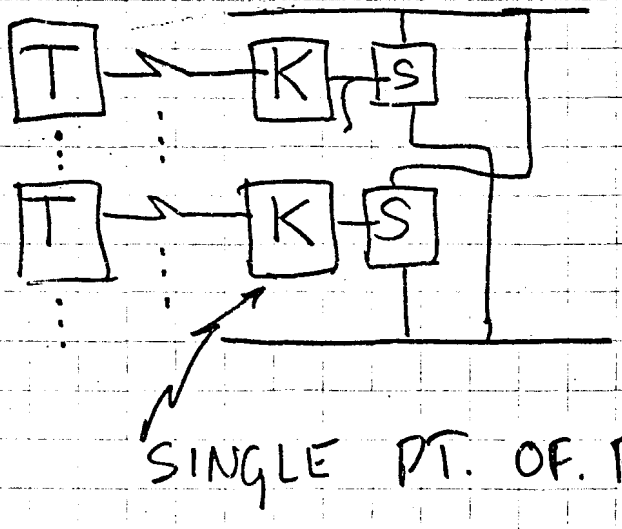


FIG 9. S. DUPLEX. 1 SITE

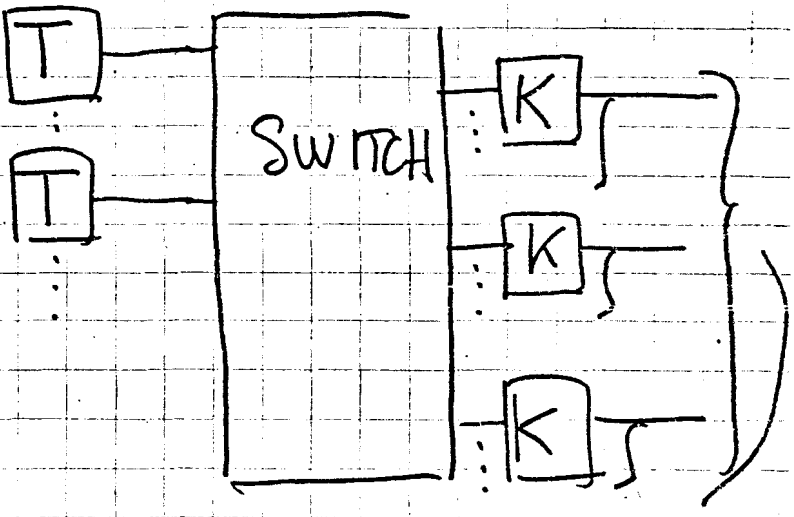


FIG 8.

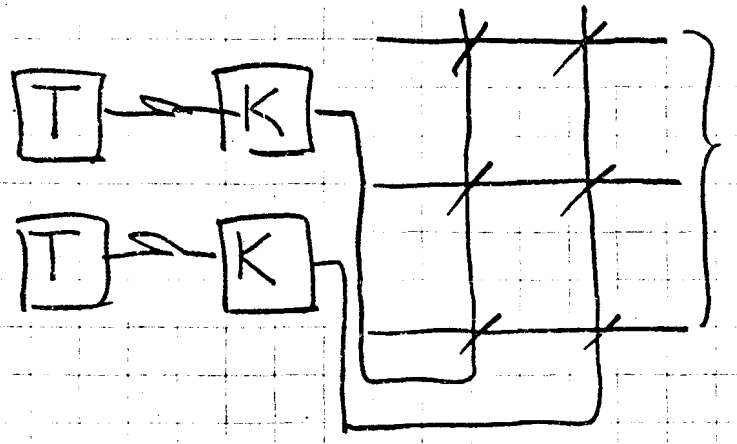


Fig. 10.
S. TRIPLEX S. 1 SITE

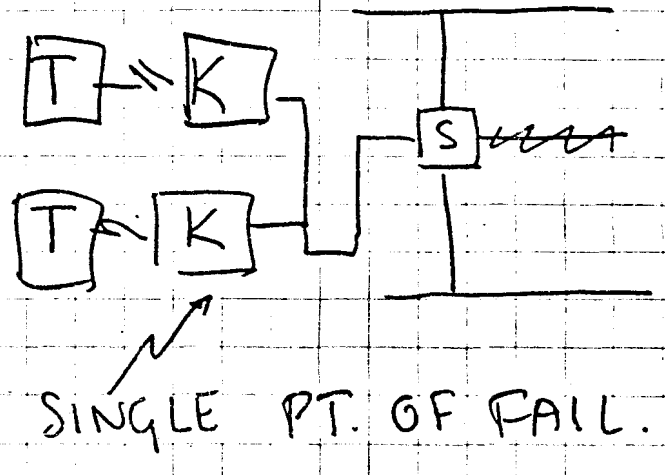
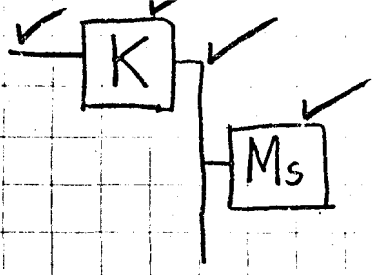
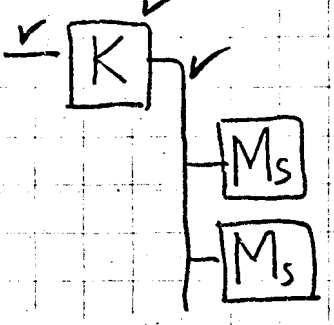


FIG 11.

1 SITE



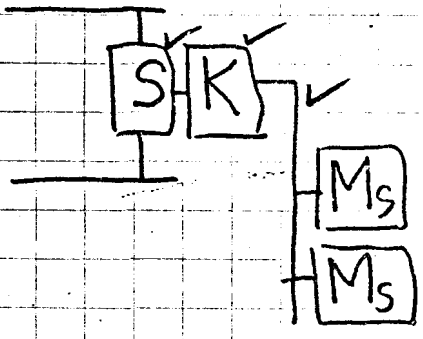
BASIC NEED



+ BACKUP DISK.

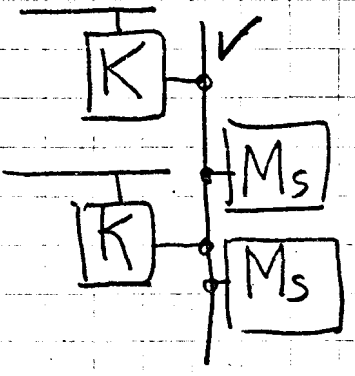
↙ PT. OF FAILURE

1C STRUCTURES



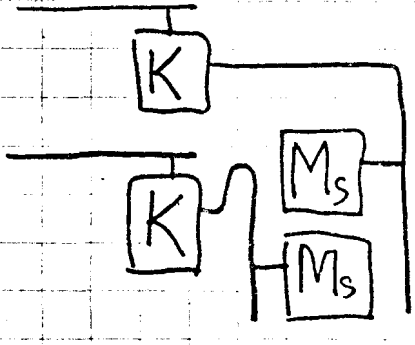
+ BACKUP C

2C (I.E. BACKUP)

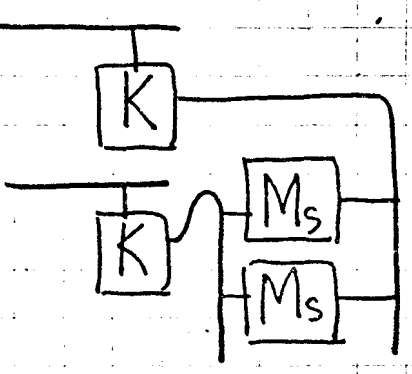


+ BACKUP K.

(NO OFFLINE REPAIR)



(FAILURE OF IC - DISABLES PATH TO 1 DISK)



+ 2 PORT Ms. - WITH OFFLINE REPAIR

2C - NO SINGLE PT. OF FAILURE

BALANCING $P_c - M_p - I/O$ (BUSSES)

BUS OPTIMALITY (AMDAHL'S CONST's)

1 Byte of Mp = 1-i/sec (use 2)

1 Bit of (i/o) = 1-i/sec

---

1 i = 3~5 bytes of accessing.

1 i = 4~6 bytes with i/o.

UNIBUS ≈ 2 Mbytes/sec.

≈ 1/2 ~ 1/3 MEGA.-INST./SEC.

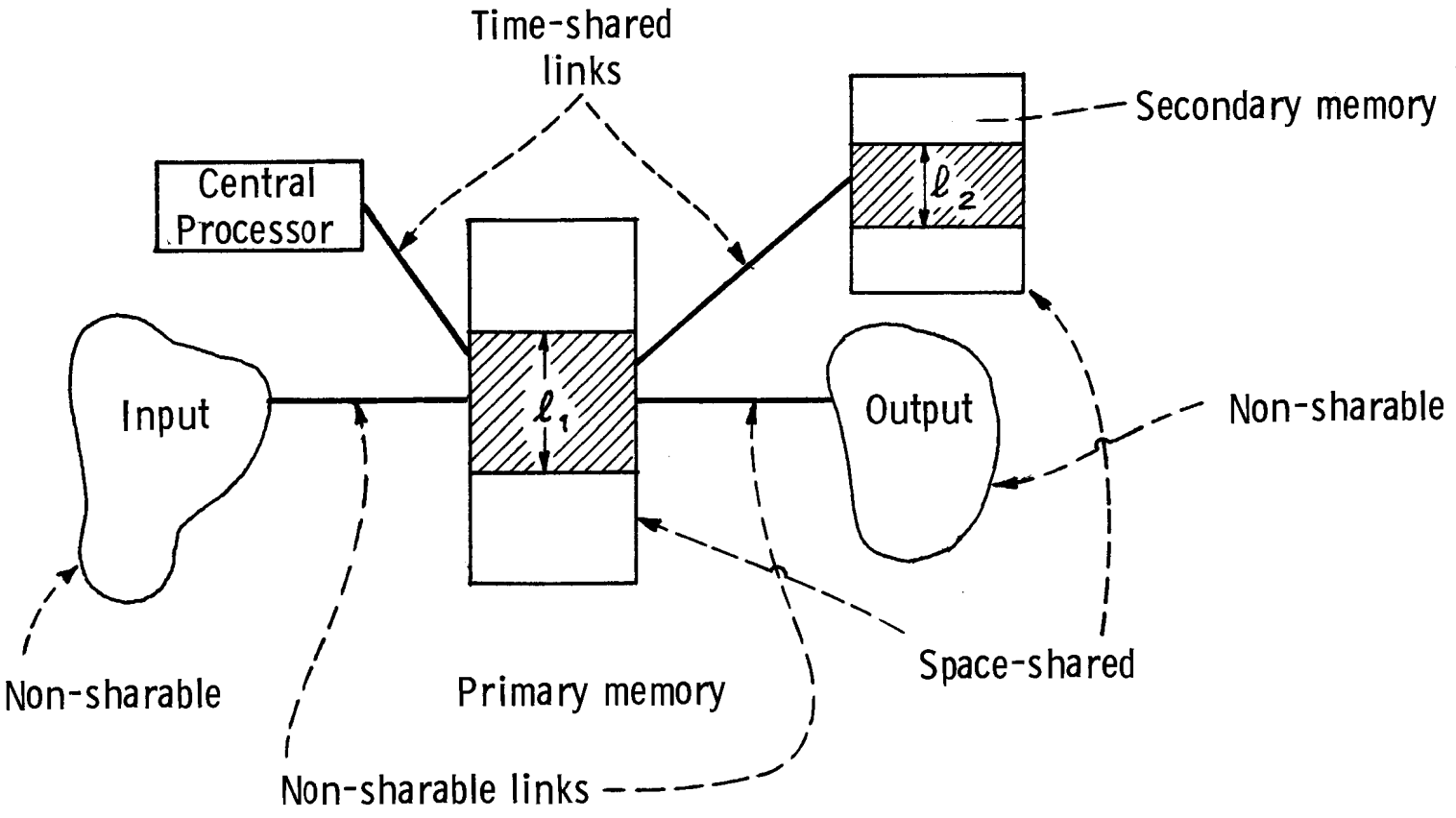
~~LIMITED~~ VIA BUS.

1/2 ~ 1/3 MEGA BYTES ARE REQ'D

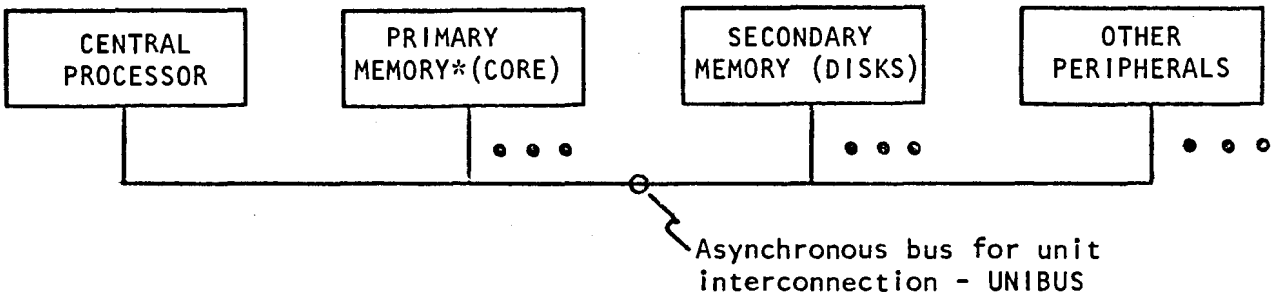
UNIBUS = 1/4 MEGA BYTES.

11/70 ≈ 2 Mbytes. ⇒ 2 Mips.

CACHE Acts TO REDUCE BW.



Multiprogram Fortran Machine Structure



* MOS can alternatively be used as desired.

Figure 1 PDP-11 Structure for the interconnection of options

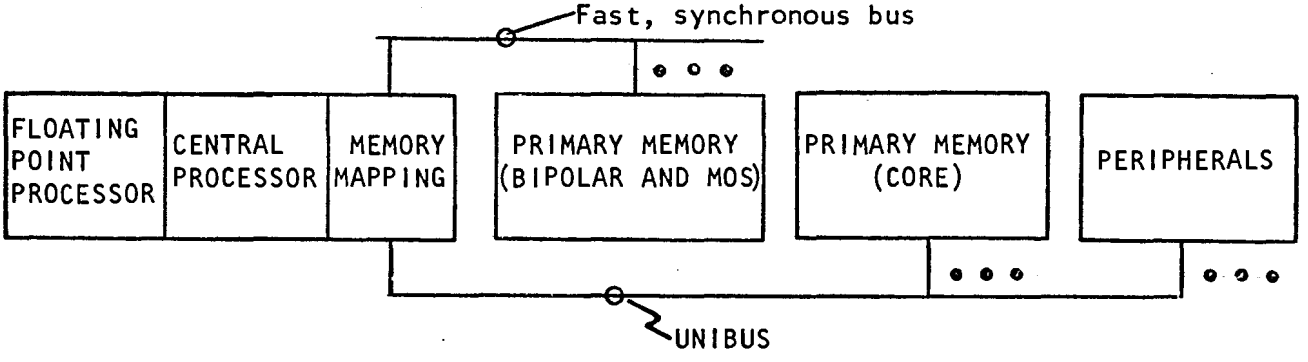


Figure 2 PDP-11/45 Structure adapted for faster memory

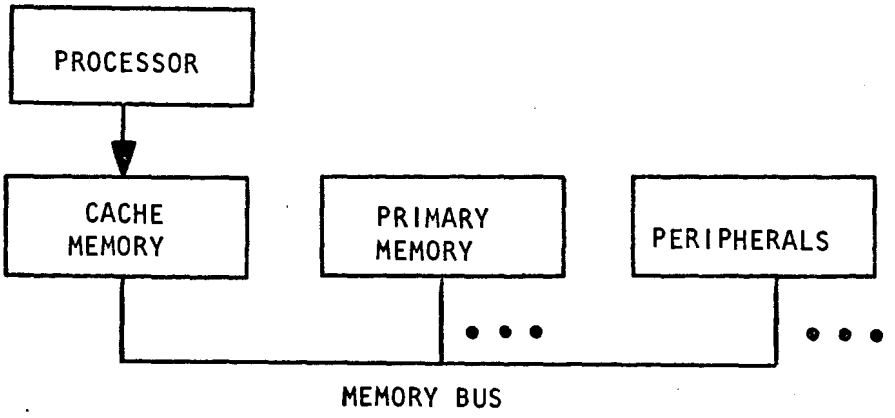


Figure 8 Computer system with Cache memory

Single Bus

+ Simplicity

+ Flex. For > # of Structures
  ⇒ (Parallelism; Reliability; Perf. via. Good Comm.)

M+ Peripheral Bus

+ Possibility For > Parallelism

+ Less Components / Bus ⇒ Reliab.

LARGE - SMALL COMPARISON

Circa 1967	Cost	WL	Mp Size	Mp.size/ $ bits/$	MIPS	MIPS x WL	REAL(MIPS)	P/C (MIPS/M$)
8	10^4(1)	12 (1)	$5x10^4$(1)	5	$.3x10^6$(1)	(1)	10^3(1)	30
6600	$3x10^6$(300)	60 (5)	$8x10^6$(160)	2 2/3	$3x10^6$(10)	(50)	$3x10^6$(3000)	1
Circa 1975								
Brd	10^3(1)	16 (1)	$4x10^3$w(1)	64	.3 (1)	-		100
8600	10^7(10^4)	64 (4)	$1x10^6$w(10^3)	6.4	100(10^4)	-		10

SOME OBSERVATIONS

1. Performance: low end is about the same. High end up 10∼30. Gap 10 ⟶ 300 (30)
2. Cost : low end is cheaper by x 10. High end up x 3. Gap 300 ⟶ 10,000 (30)
3. Mp. size no economy of scale.

GB
2/7/75

PMS-Level Computer Architecture

BASIC Problem: Specifying Load

User: Buying (Selecting);
Balancing (#M, P, T);
Designing Structures (Front Ends, mP, closely Coupled, Nets)

Manufactures:
New design Structures;
Reliable, - PRESENT INTERFACE

Objective Fcn: Price,
Availability, Performance,
Size (Space & Power)

MINI APPLICATION ORIGINS

CONTROL (LOGGING, RECORDING, CONTROL — EG. LGP-30, RW-)

SMALL SCALE COMP. (LGP-30)

SMALL SCALE EDP (1401)

LAB. CONTROL + PROCESSING (EG. PDP-'S).

SWITCHING ↗

G.P. SHARED (EG. PDP-1)

[HOW USED vs. WHAT FOR]

INDUSTRIAL

- T — TRANSDUCTION (DATA LOGGING)
- T + MEMORY — (RECORDING)
- T + M + K — (CONTROL)

- SWITCHING.
- S + MEMORY (ACCESS to DATA B.)

EDP

- T + D (DATA PROCESSING) — REPORTS
- T + D + P (PROCESSING)
- T + D + P + M (ACCESS TO DATA B.)

SCI.

- D - COMPUTATION
- T + D + M - DATA RECORDING.
- T + D + M + P - ON Line Control + Proc.

P - Processor (eg. Cent., i/o)

M - Memory (eg. Core, Disk)

S - Switch (eg. Bus)

L - Link (eg. Comm. Intf

K - Control (i.e. FSM)

T - Transducer (eg. Terminal)

D - Data-operation

C := $(M_p + P_c)$ - Computer

Examples of PMS Use

P(function: central)

P(central \ c)

P(c)

P.c

Pc

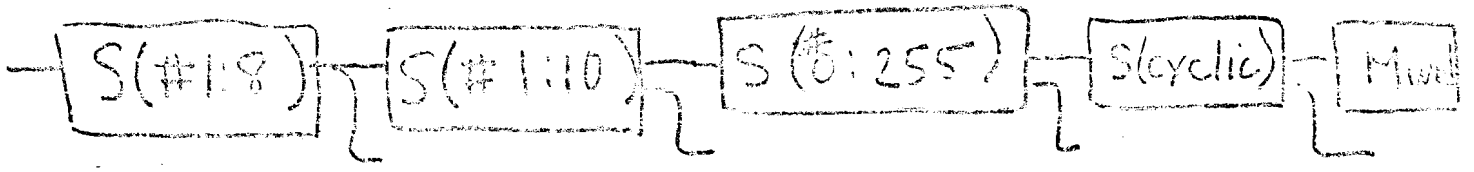
M(function: primary \ p |
secondary \ s | tertiary \ t)

Mp | Ms | Mt

M := M.simple | SM

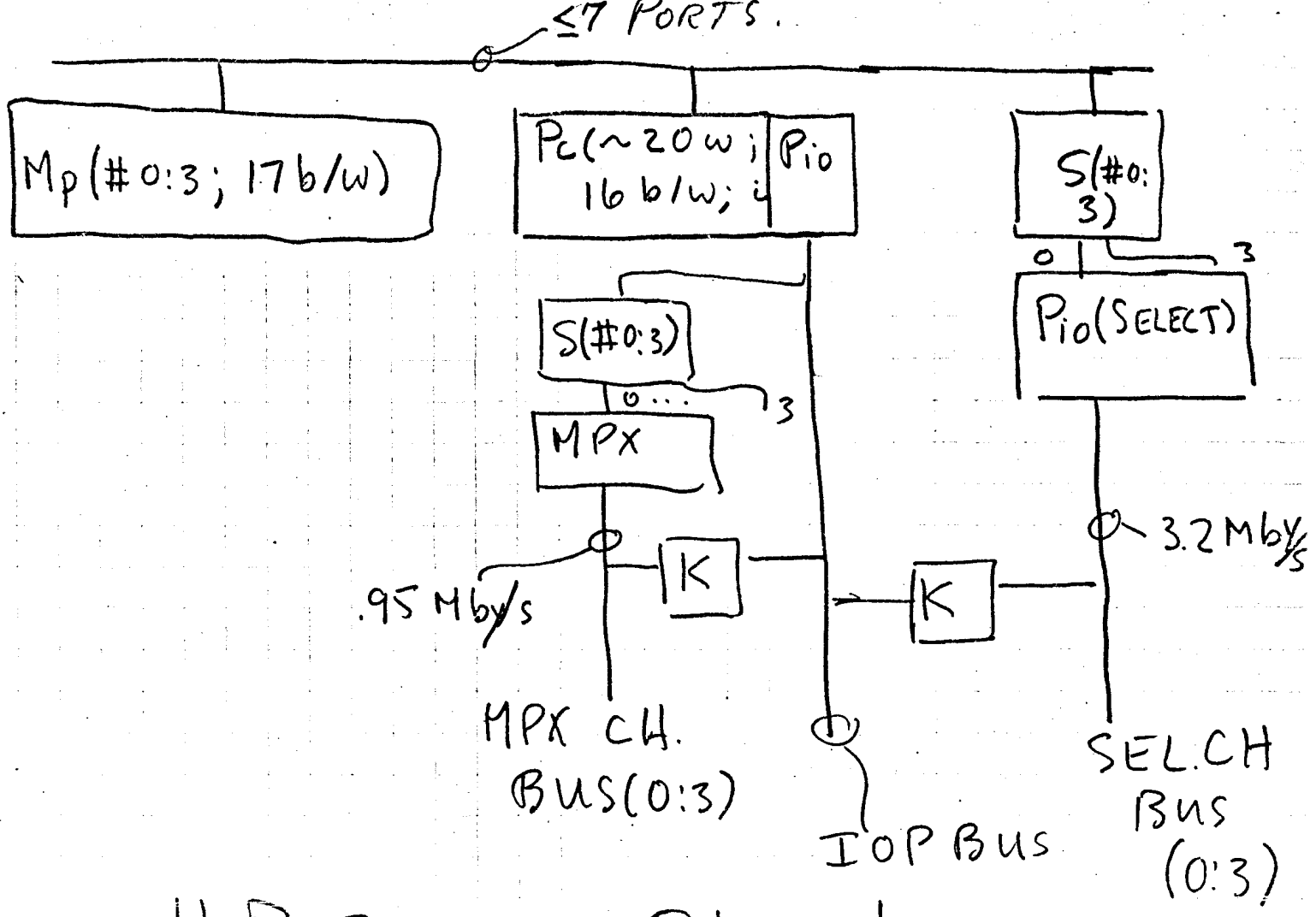
eg.

M(disk sub-system) :=

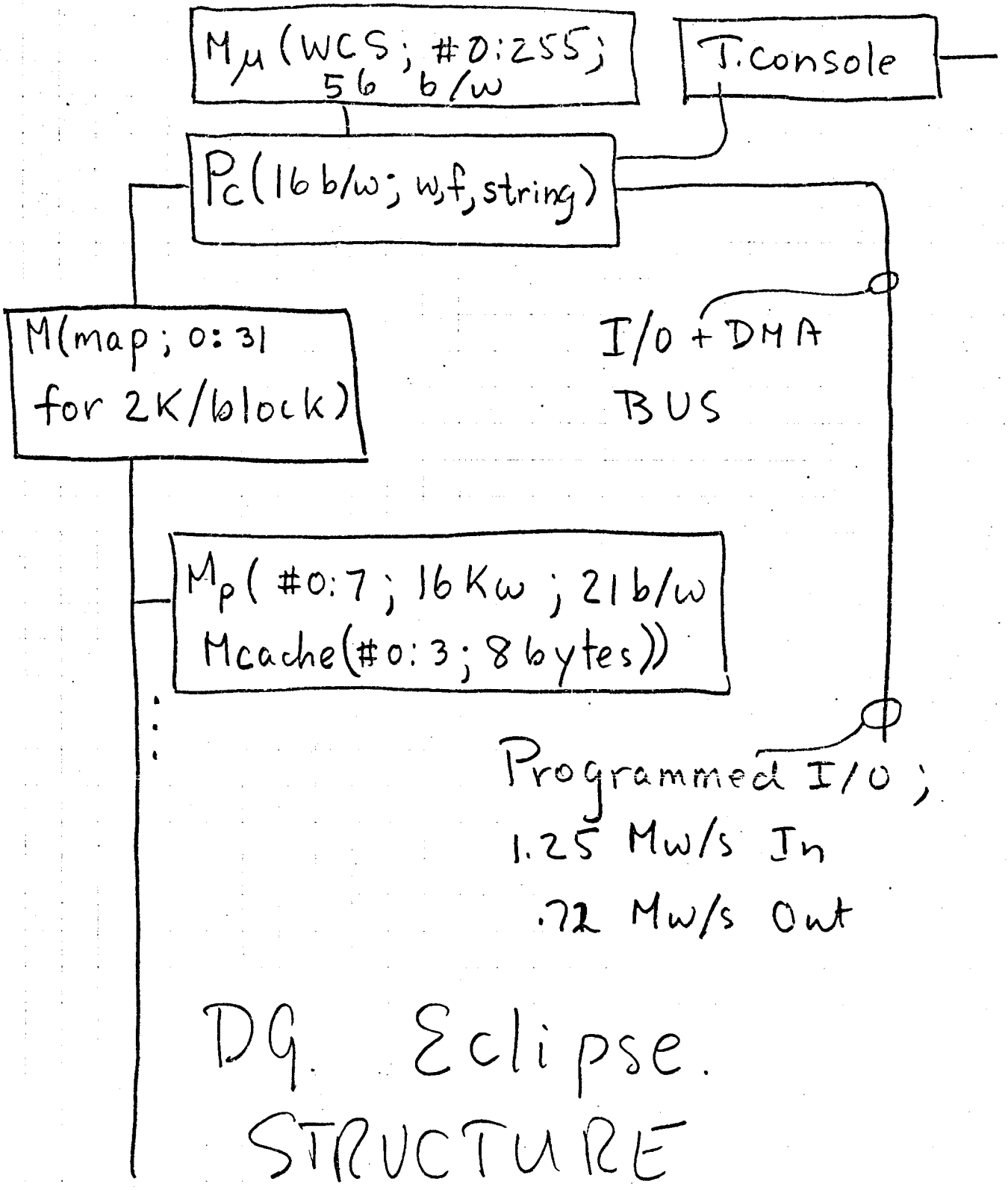


CONFIG.	Perf.	PRICE			PERF/PRICE (NORMAL.)		
		S	M	L	S	M	L
CORE	1	5	10	35	1	1	1
MOS	2	5	10	35	2	2	2
CACHE	5	10	15	40	2.5	3.3	4.3

PERF., PRICE & PERF/PRICE
FOR CACHE-BASED, ETC.
PDP-8's.



HP 3000 Structure.



DG. Eclipse.
STRUCTURE

1. Production (Learning)

$E_n = k\, n^d$ = Eff. of nth unit

(Learning consts.)

---

2. Technology Forecasting

$T(t) = k\, e^{ct}$ = Technology at t

---

3. Technology Progress Fcn.

$T_n = a \cdot n^b$

[b = 2.5 for Computers]

$T_n = T(t)$ if $i = e^{\%\, t}$

BASIC DESIGNS.

1. **STATUS - QUO**

   ALL Costs $\approx k$

   ↳ (COMPUTER, SALES, Operations)

2. **MINI(MIZE) COST**

   Perf $\approx$ function $\approx k$.

   Decrease cost... accelerate learning + demand.

3. **BUILD "SUPER" COMPUTER**

4. **BUILD SUBSET**

   (Eg. CALCULATOR).

TABLE 2 - CHARACTERISTICS GENERIC TO MINICOMPUTERS

IMPLIMENTATIONS TRACK TECHNOLOGY CLOSELY.

INTERNAL CENTRAL PROCESSOR

BASE ADDRESSING; ADEQUATE INTERRUPT RESPONSE TIME; POWER ON-OFF INTERRUPT

STRUCTURAL

VERY LITTLE HARD COPY I/O, SECONDARY MEMORY; OBVIOUS STRUCTURE (ALLOWING EASY INTERFACING); DIRECT MEMORY ACCESS--ENCOURAGES PMS ARCHITECTURE + DESIGN.

USES (DEDICATED)

CONTROL (E.G., PLANT, INSTRUMENT); COMMUNICATIONS (E.G., MESSAGE SWITCH); LARGER COMPUTER (E.G., TERMINALS, FILES, HARD COPY)

SOFTWARE

SMALL GENERAL PURPOSE MONITOR; LANGUAGES: PRIMITIVE ASSEMBLER, BASIC, FORTRAN; SPECIALIZED DEDICATED USE PACKAGES (E.G., TYPESETTING, INSTRUMENT TESTING, PROCESS)

APPROACHABLE--FIT COMPUTER TO PROBLEM VS...

TABLE 1 - CHARACTERISTICS DERIVED FROM LARGER COMPUTERS

INTERNAL CENTRAL PROCESSOR

INDIRECT ADDRESSING; INTERRUPTS; INDEX REGISTERS; MULTIPLE, GENERAL PURPOSE REGISTERS; BASE AND/OR PAGE ADDRESSING; FLOATING POINT DATA-TYPES*; PAGING, SEGMENTATION, AND INTERPROCESS COMMUNICATION*

STRUCTURAL

SPECIALIZED PROCESSORS; MULTIPROCESSORS*

IMPLEMENTATION

MICROPROGRAMMING*; LOOKAHEAD*; CACHE*;

SOFTWARE

COMPILERS: FORTRAN; TIME-SHARING MONITORS*

*NOT EXTENSIVELY USED, BUT USE LIKELY TO INCREASE.

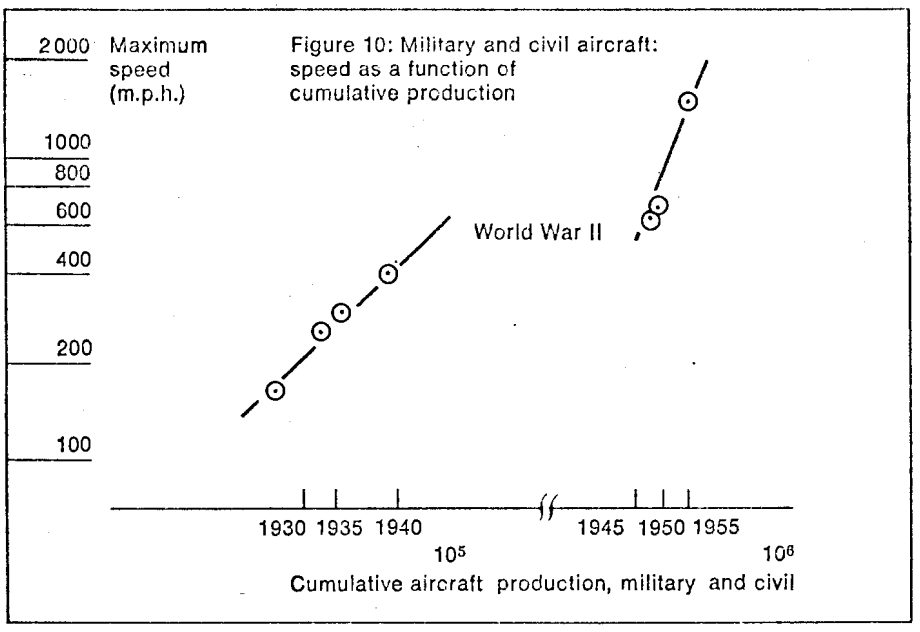


Figure 10: Military and civil aircraft: speed as a function of cumulative production

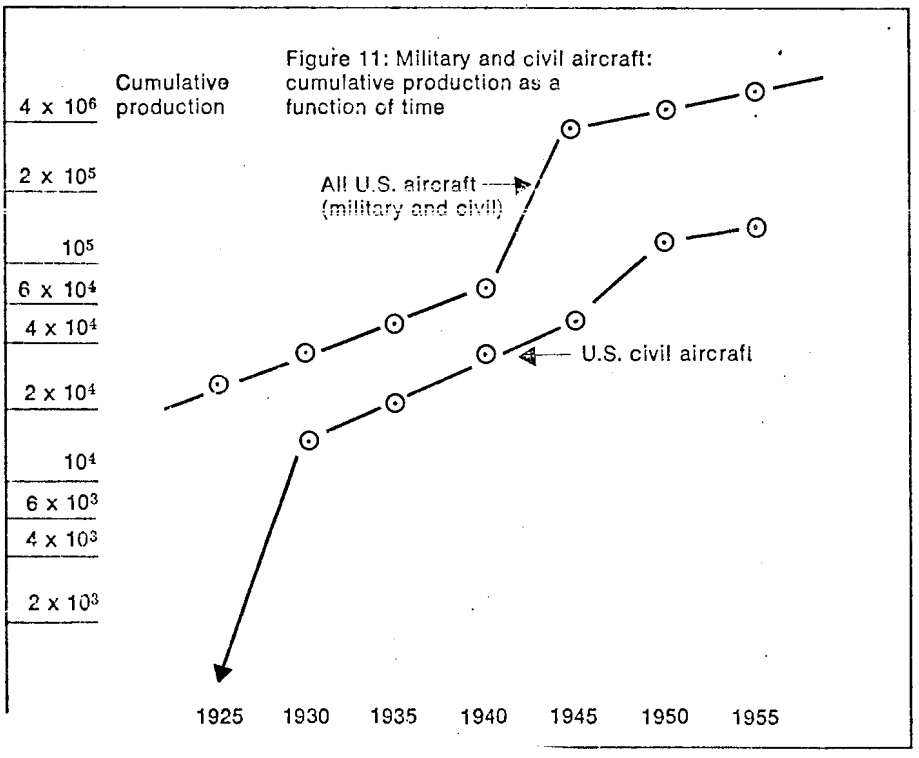


Figure 11: Military and civil aircraft: cumulative production as a function of time

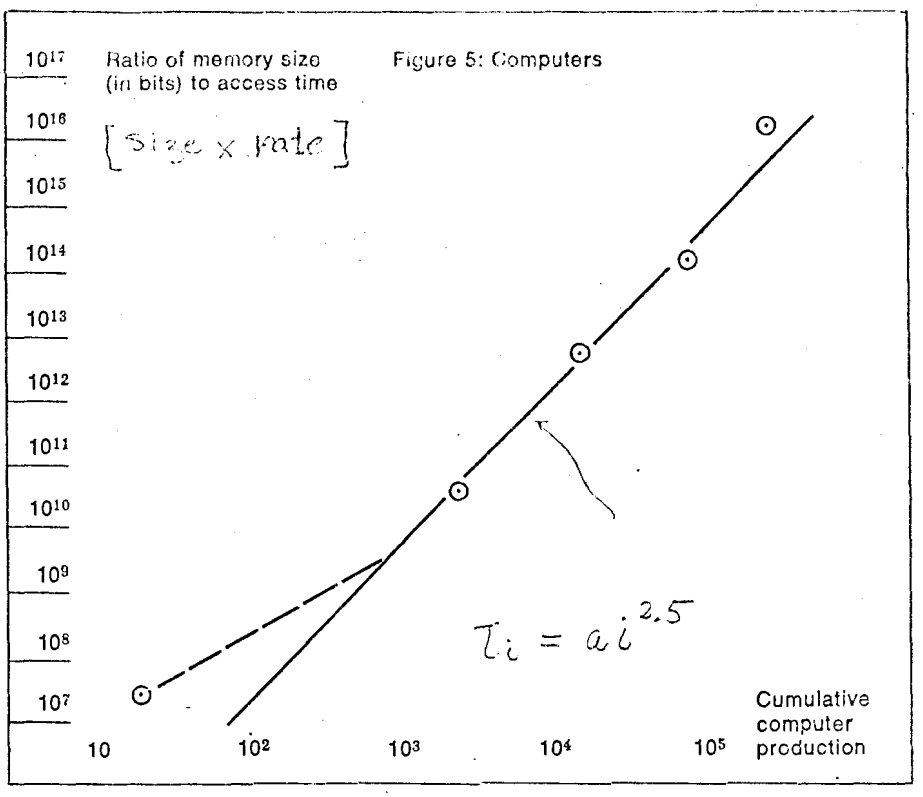


Figure 5: Computers
Ratio of memory size (in bits) to access time
[size x rate]
10^{17}
10^{16}
10^{15}
10^{14}
10^{13}
10^{12}
10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
$T_i = a i^{2.5}$
10
10^2
10^3
10^4
10^5
Cumulative computer production

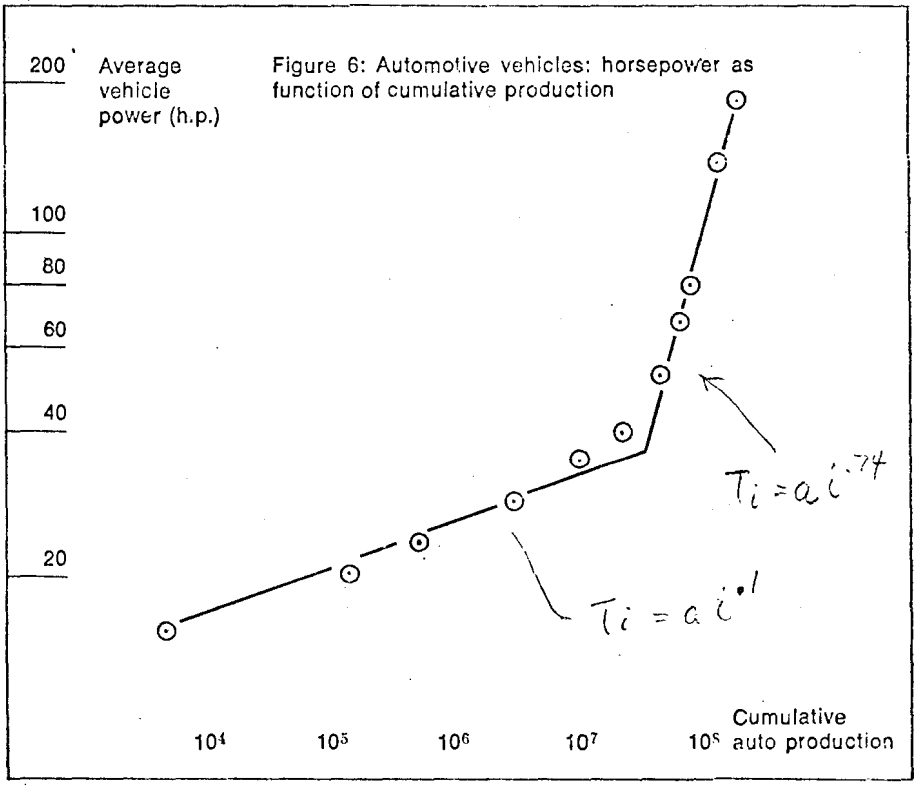


Figure 6: Automotive vehicles: horsepower as function of cumulative production
Average vehicle power (h.p.)
200
100
80
60
40
20
$T_i = a i^{.74}$
$T_i = a i^{.1}$
10^4
10^5
10^6
10^7
10^8
Cumulative auto production

FM: BELL, CADY, MCFARLAND, DELAGI, O'LOUGHLIN, NOONAN, WULF
AFIPS SJCC 1970, P657, "A NEW ARCHITECTURE FOR MINI-COMPUTERS--
THE DEC PDP-11"

NAME	MP.SIZE	PC+BASIC MP PRICE	WORD LENGTH (BITS)	PC.STATE (WORDS)	DATA-TYPES
MICRO	8K	~5K	8-12	2	(1~2) WORD = BYTE - INTEGER = BOOLEANS
MINI	32K	(5-10)K	12-16	2-4	(3) + ADDRESSES, VECTORS (INDEX)
MIDI	65-128K	(10-20)K	16-24	4-16	+ DOUBLE INTEGERS + FLOATING POINT
: : MAXI					

ALL ARE: 5-10 MHZ CLOCK; TTL; MSI
T.CYCLE .7~2 μSEC.
FIXED TO A SPECIFIC, SINGLE TASK.

GB
1/19/76

MINICOMPUTERS: A STATE OF MIND

IANN M. BARRON

"THE MINICOMPUTER IS AN ATTITUDE OF MIND. IT IS NOT USEFUL TO DEFINE IT IN TERMS OF PRICE OR CAPABILITY BECAUSE THESE CHANGE WITH THE TECHNOLOGY. THE DIFFERENCE...LIES IN MARKETING PHILOSOPHY. THE MINICOMPUTER COMPANY IS SELLING A MANUFACTURED PRODUCT WHEREAS THE CONVENTIONAL COMPUTER COMPANY IS SELLING A SERVICE, AND SERVICES COST MONEY.

H. COX

MINICOMPUTER: A GENERAL PURPOSE COMPUTER IN WHICH INPUT AND OUTPUT TRANSFERS ARE OF SINGLE WORDS (OR PART WORDS) FROM REGISTERS, EACH TRANSFER COMMANDED BY AN INSTRUCTION IN THE PROGRAM. THE OTHER MAIN CLASS OF COMPUTERS HAS NO COMMON NAME AND IS DISTINGUISHED BY INPUT AND OUTPUT TRANSFERS BEING OF BLOCKS OF WORDS (OR PART WORDS) THAT ARE CARRIED OUT AUTOMONOUSLY FROM STORE, THE PROGRAM SETTING UP BLOCKS AND INITIATING THE TRANSFER OF BLOCKS.

THE DIFFERENCE IS SIMILAR TO TUNGSTEN OR FLUORESCENT LAMPS AND ORDINARY LAMPS, VIZ: LOWER EFFICIENCY... OR HIGHER OVER-HEADS. FLUORESCENTS ARE UNDOUBTABLY MORE EFFICIENT FOR BUSINESS LIGHTING, BUT HAVE A MINIMAL SHARE OF THE CHRISTMAS TREE LIGHTS MARKET.

ab 1/19/76

MINICOMPUTER SOFTWARE

FROM A SALES PITCH BY JR, CG BELL FOR IFIPS BOOK (CONFERENCE)

ON MINICOMPUTER SOFTWARE

"READ THIS BOOK AND FIND OUT WHY SOME OF THE MOST EXPERIENCED, KNOWLEDGEABLE PEOPLE FEEL THAT:

- A MINICOMPUTER IS NOT JUST A SCALED DOWN LARGE COMPUTER.
- THE LIMITED SIZE OF MINICOMPUTERS CAN ACTUALLY BE AN ASSET.
- ONE OF THE KEY BARRIERS TO MINICOMPUTER USE IS PSYCHOLOGICAL.
- STANDARDIZED LANGUAGES ARE MORE IMPORTANT THAN BETTER LANGUAGES.
- PORTABILITY OF PROGRAMMERS IS AS VITAL AS PORTABILITY OF PROGRAMS.
- MINICOMPUTERS ARE FOR THOSE APPLICATIONS NOT FEASIBLE WITH MAXICOMPUTERS--COST, RESPONSE TIME, HUMAN INTERFACE, ULTRA-RELIABILITY.
- TO MINICOMPUTER USERS, OLD TECHNICAL PAPERS ARE MORE VALUABLE THAN NEWER ONES.
- MINICOMPUTER SOFTWARE IS SHAPED PRIMARILY BY APPLICATIONS, YET FORCES EVERY PROGRAMMER TO BE A SYSTEMS PROGRAMMER."

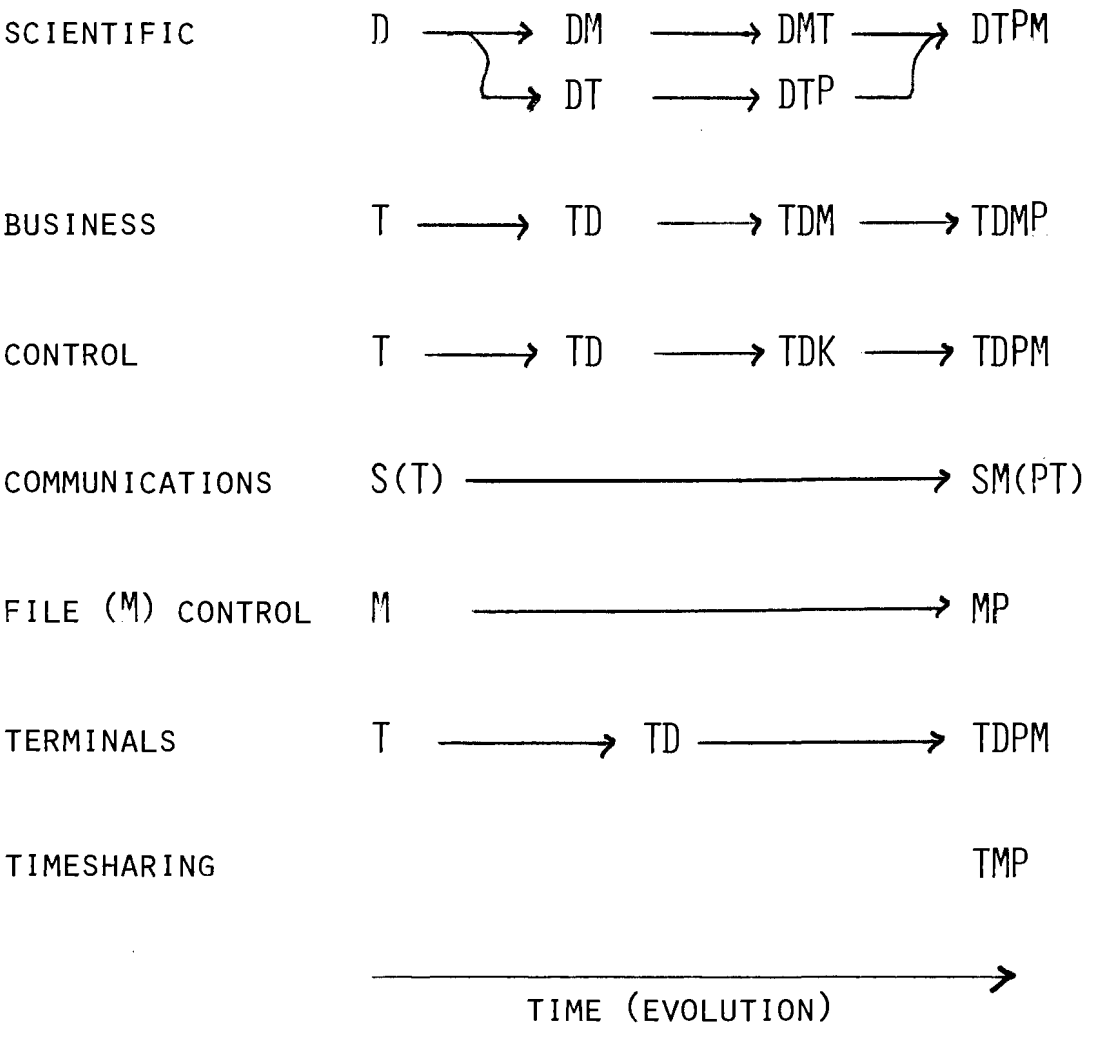
DIFFERENCES: DEDICATEDNESS (E.G. OPERATING SYSTEM)

SIZE CONSTRAINT (ALTHOUGH COST/BIT IS CHEAPER AND MP SIZE IS INCREASING)

ISSUES OF CONFERENCE: PROGRAMMING LANGUAGES (STRUCTURED-TYPE), PRODUCTIVITY, PORTABILITY, USER MICROPROGRAMMABILITY

GB
1/19/76

COMPUTER-SPACE (FUNCTION DIMENSION)



GB
1/12/76

COMPUTING EUROPE (6 NOV 1975)

" WHEN IS A MINICOMPUTER NOT A MINICOMPUTER?
SURELY IT IS TIME THE INDUSTRY FACED THE PROBLEM OF EVOLVING A STANDARD DEFINITION.

1. ANNOUNCEMENTS FROM MINICOMPUTER COMPANIES AREN'T, BY DEFINITION, MINIS.

2. DATAPRO RESEARCH CORPORATION
...THE WHOLE CLASS OF STORED-PROGRAM DIGITAL COMPUTERS WHICH ARE SUITABLE FOR GENERAL-PURPOSE APPLICATIONS AND ARE PRICED BELOW $50,000.

3. ELECTRICAL RESEARCH ASSOCIATION (1972)
...A COMPUTER...WHICH MAY BE PURCHASED FOR LESS THAN $40,000 IN THE FOLLOWING MINIMUM CONFIGURATION: Pc, Mp (256~8K WORDS), T.CONSOLE, T(TELEPRINTER + PAPERTAPE READER AND PUNCH), POWER SUPPLIES (ETC.); SOFTWARE...WITH BOOTSTRAP AND BINARY LOADER.

4. BARNES IN SPL INTERNATIONAL MINICOMPUTER FORUM 1975

...HARD TO SAY PRECISELY BECAUSE OF BROAD SPECTRUM OF SIZE, PERFORMANCE, BUT USUALLY A RELATIVELY INEXPENSIVE, SMALL SCALE COMPUTER WITH A WORD LENGTH OF 16 BITS OR LESS WHICH CAN OPERATE IN AN OFFICE ENVIRONMENT WITH NO AIR CONDITIONING, NO FALSE FLOORS AND NO SPECIAL POWER SUPPLIES.

5. DEC (UK) MINIMAL CONFIGURATION COST OF < £ 20K AND CAPABLE WITHIN THE MINIMUM OF TAKING A HIGH LEVEL LANGUAGE (E.G. FORTRAN, BASIC).

6. VARIAN--THE DEFINING CRITERIA IS THAT THE ACTUAL PHYSICAL EQUIPMENT SHOULD BE PACKING MAINFRAME CAPABILITY INTO A PHYSICALLY SMALLER CABINET.

7. HP(UK)--SMALL GP-C WHICH IS FREQUENTLY THE MOST COST-EFFECTIVE SOLUTION TO A WIDE VARIETY OF APPLICATIONS IN BUSINESS, SCIENCE, AND EDUCATION."

GB
1/12/76

LANGUAGE / OP. SYSTEM. STRUCTURE DIMENS.

- FUNCTION ~ SCHEDULING ~ URGENCY:
  - BATCH — DON'T CARE 0 → ∞ SEC.
  - INTERACTIVE — STOCHASTIC 2 - 10 SEC.
  - REAL TIME — DEMAND .100μ - 1 SEC. (GUARANTEED RESP.)

- # PERFORMING FUNCTION: 1 OR N. JOBS [SUB-STRUCTURE 1 OR M PROCESSES/J.]

- ° DEDICATEDNESS: FIXED OR VARIABLE ~ UNCERTAINTY (PROGRAMMABILITY)

- LANGUAGE GENERALITY.
  - 1 , FIXED.
  - MULTIPLE, FIXED
  - MACHINE + ABILITY TO ADD MORE

INCREASING {PERFORMANCE / RESOURCE} NEEDS

1 - FIXED → 1 - VARIABLE → N - FIXED → N - VAR → N - VAR + L - LANG.

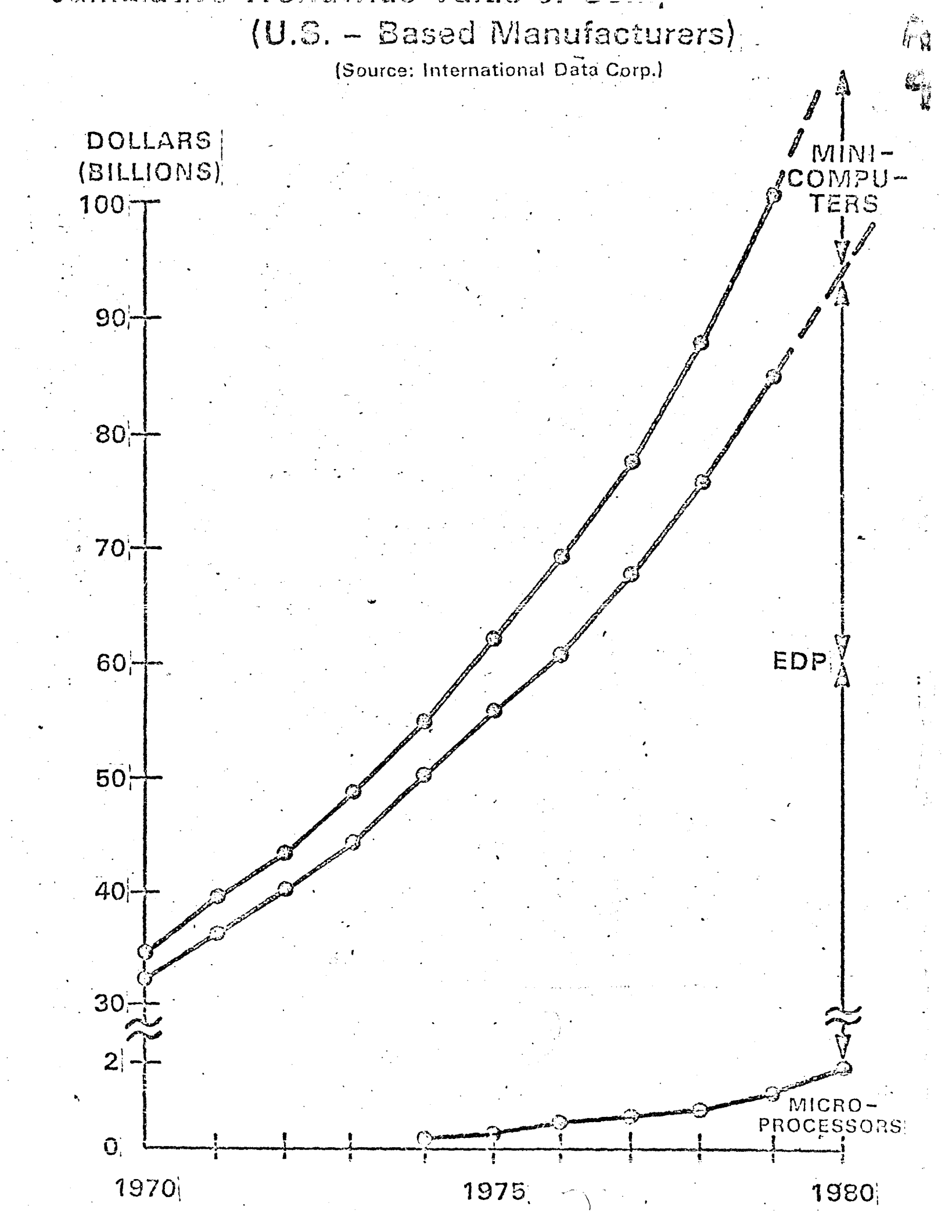
1 LANG. → L - LANG.

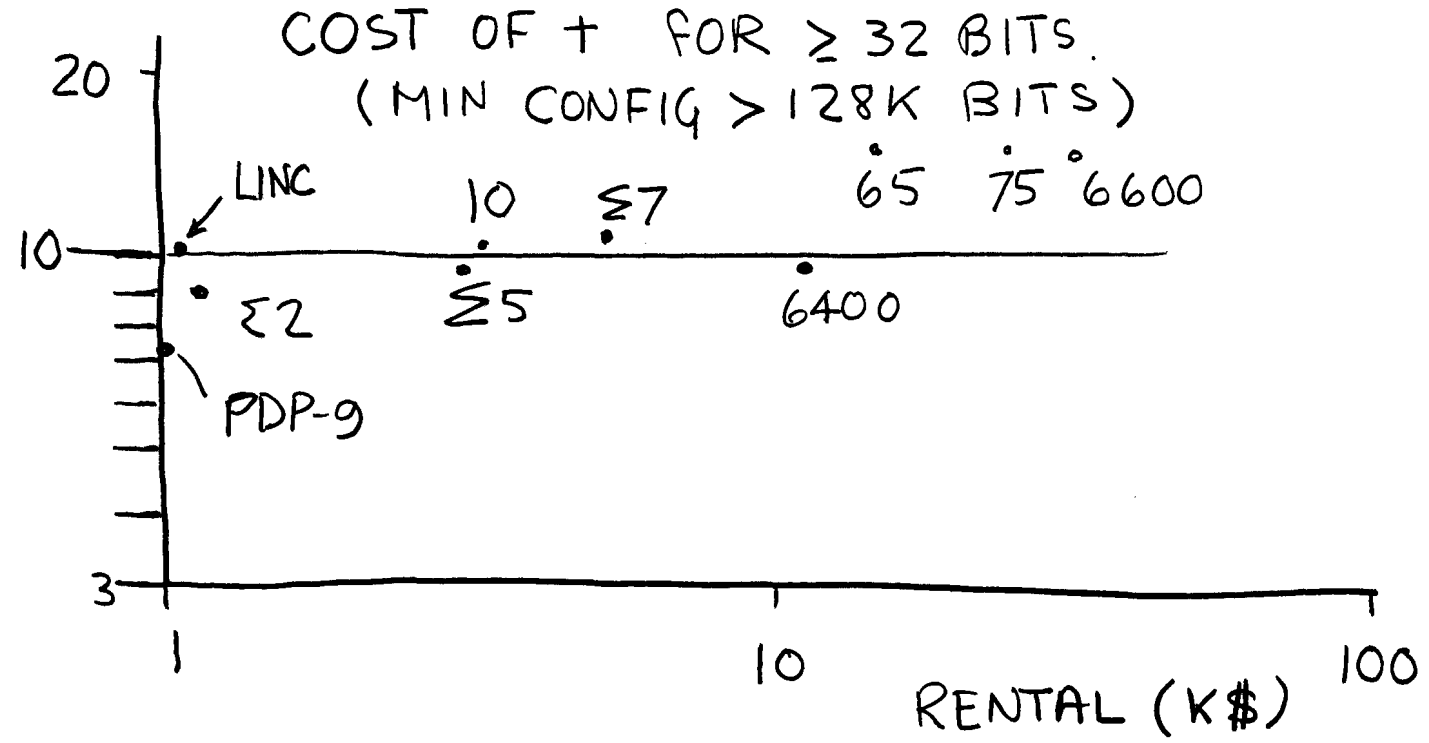
MARKET SEGMENTATION SCHEMES

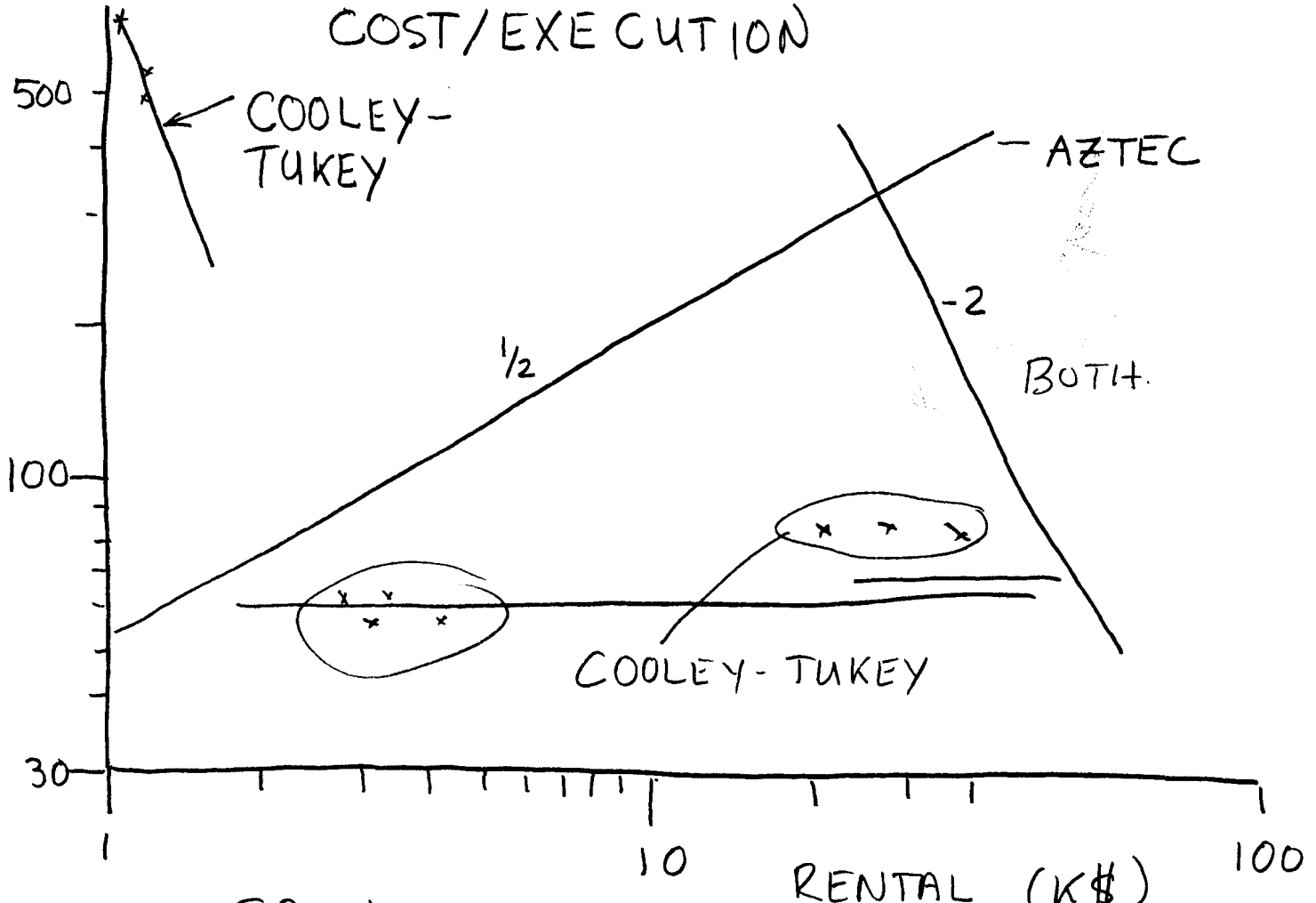
- LEVEL OF INTEGRATION (I.E. WHO DOES WHAT?)
  - ≃↓
- HOW DISTRIBUTED. / WHERE DIST.
- APPLICATIONS:
  - STRUCTURE (M, P, T, S-REQ'D).
  - LANGUAGES
- LANG. / OP. SYS. STRUCTURE DIMENS. (SEE NEXT FIG.).
- PRICE
- BASIC PERF. (≃ P. STRUCTURE)

(U.S. – Based Manufacturers)

(Source: International Data Corp.)



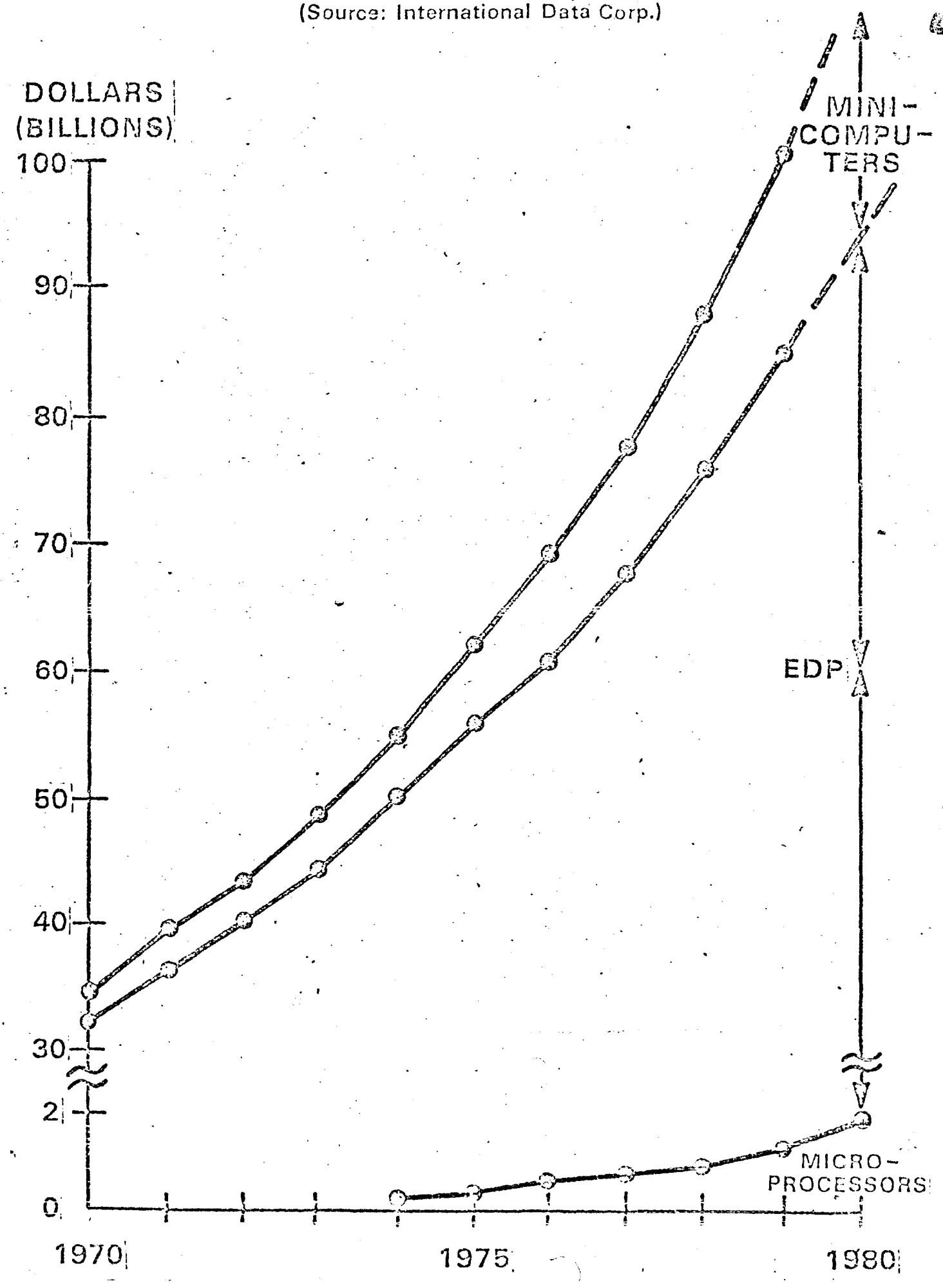




ECONOMY OF SPECIALIZATION (COX-1969)

Annual Worldwide Value of Computers Installed
(U.S. – Based Manufacturers)

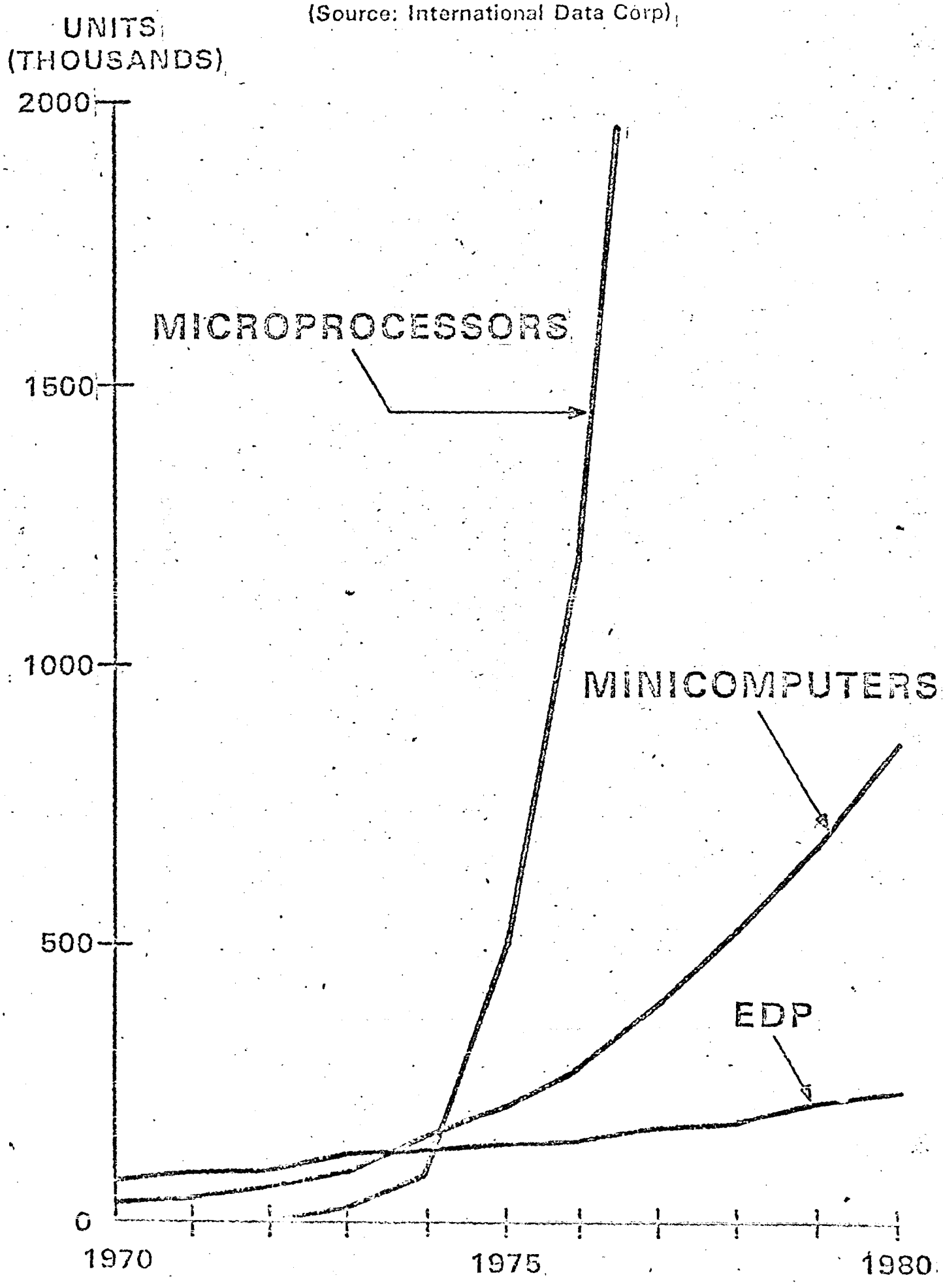
(Source: International Data Corp.)



Computers Installed Worldwide

By U.S. – Based Manufacturers

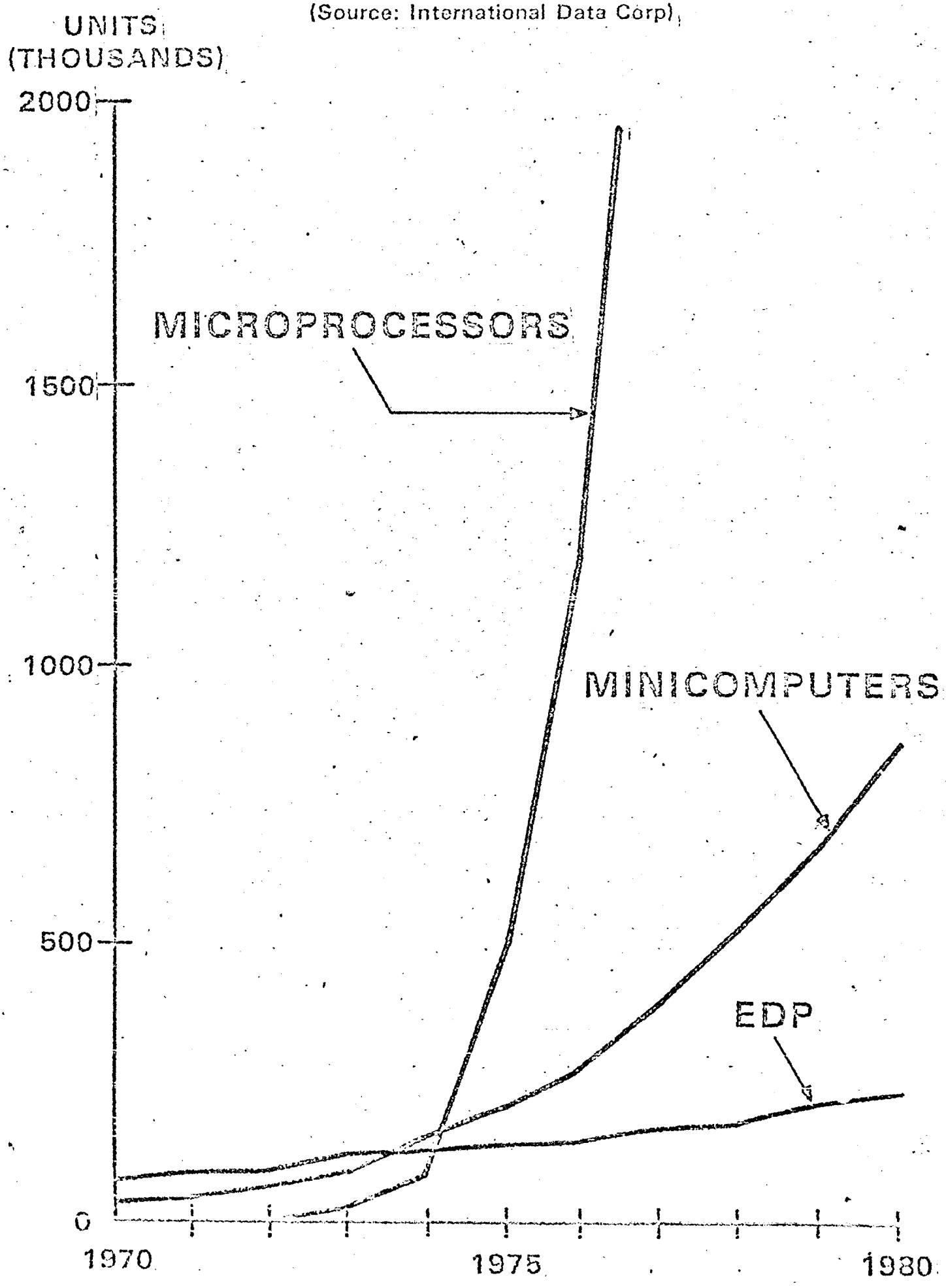
(Source: International Data Corp)



Computers Installed Worldwide

By U.S. – Based Manufacturers

(Source: International Data Corp)



A MARKET MACHINE CLASS SEGM.

I. 8-12 bits Board ~ Box Predef.
↖ μprocessor Language

II. 8~12 Mini Similar to PDP-8.

III 11/05 – 11/40 (2K – 50K)
Boxes ~ systems.

IV. 16~32 bits 11/45 ~ 11/70
Interdata 8/32.

SIZE PARTITION

1. μP (Integrated Into Peripherals
2. Modules destined to OEMs
3. μ or Mini Cap. of Nets
4. " Spec. Processing
5. MINI SPEC. Pkg.
6. " COMPLEX Net. Comp.
7. " Use by NOVICE
8. " Top of Range
9. " , but Integ. to Nets.

⇒

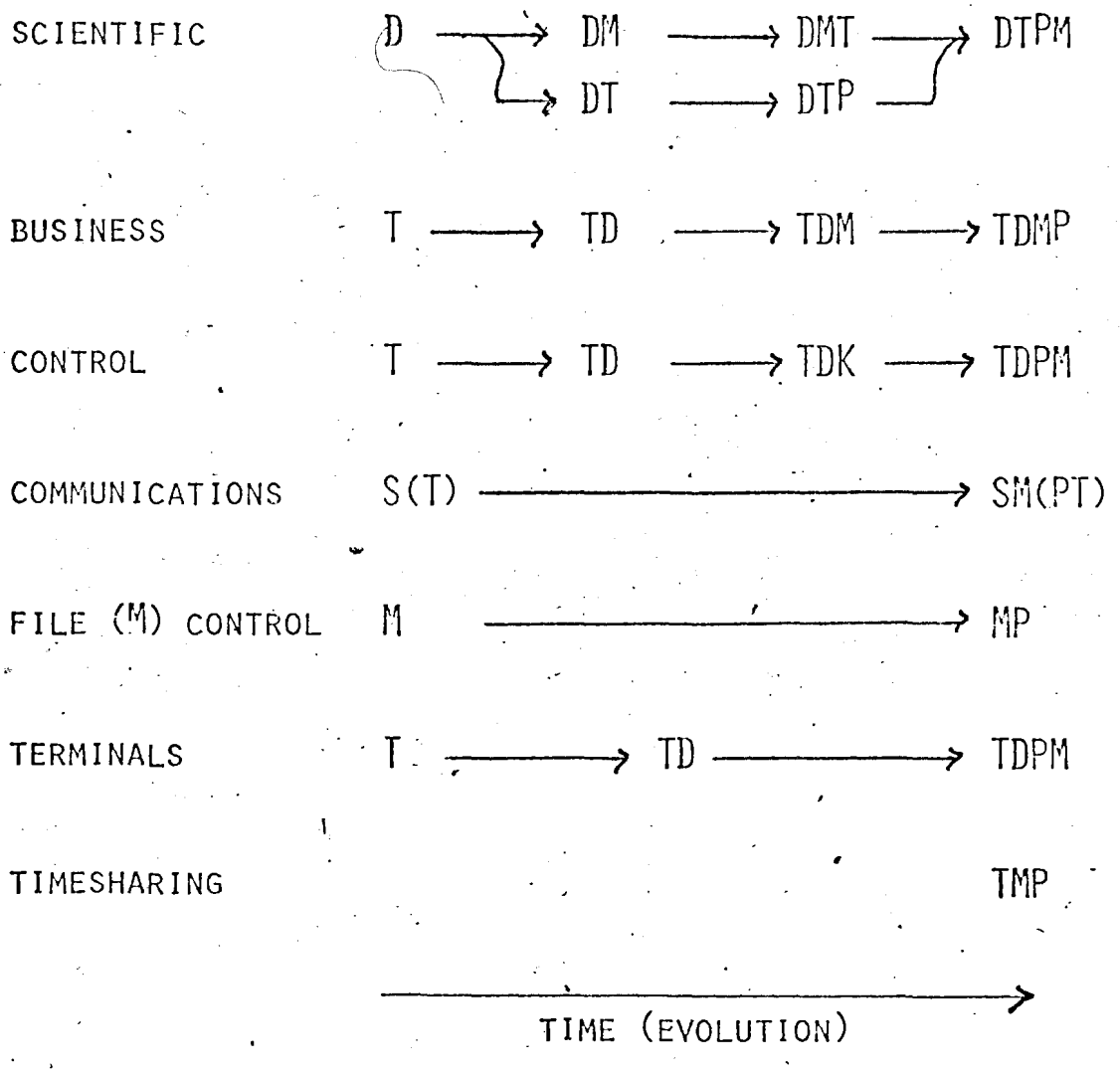
- MICRO − Weak, Var. Compx., FUNCT. Spec.
- " + Avg., Weak. Comp., Multi Pc
- MINI − GOOD, COMPAT., COMPLEX
- " + HIGH, WK. COMP., MULTI-Pc, GP.

Perf.	ARCH.	°SPEC.	COMPAT.	COMPX.

A: MARKET SEGMENTATION A14

COMMUNICATIONS	S, K, M.
EDP SUPPORT	T
BUS. DATA PROC.	D, TD, TDM
SPEC. DATA & WORD PROC.	TM.
IND. AUTOMATION	T, K, KM.
SPEC. DATA ACQ.	TM.
LAB & COMPUT.	DM, TM, ..
INSTRUCTIONAL.	T, TM., TDM.

COMPUTER-SPACE (FUNCTION DIMENSION)

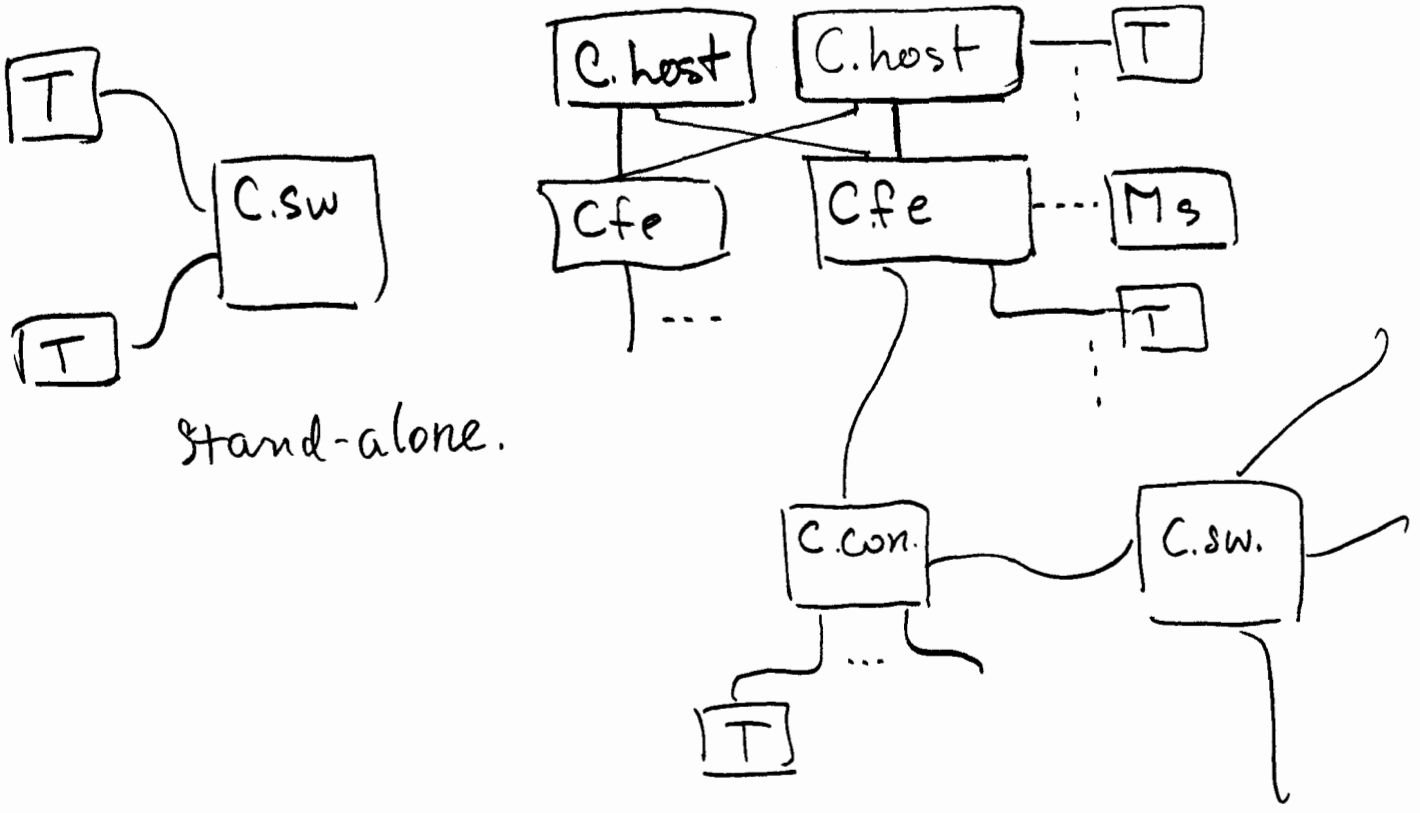


GB
1/12/76

COMMUNICATIONS

FRONT END
CONCENTRATOR
MESSAGE SWITCH.

PABX.
MONIT. / CONTROL CENT. OFF.



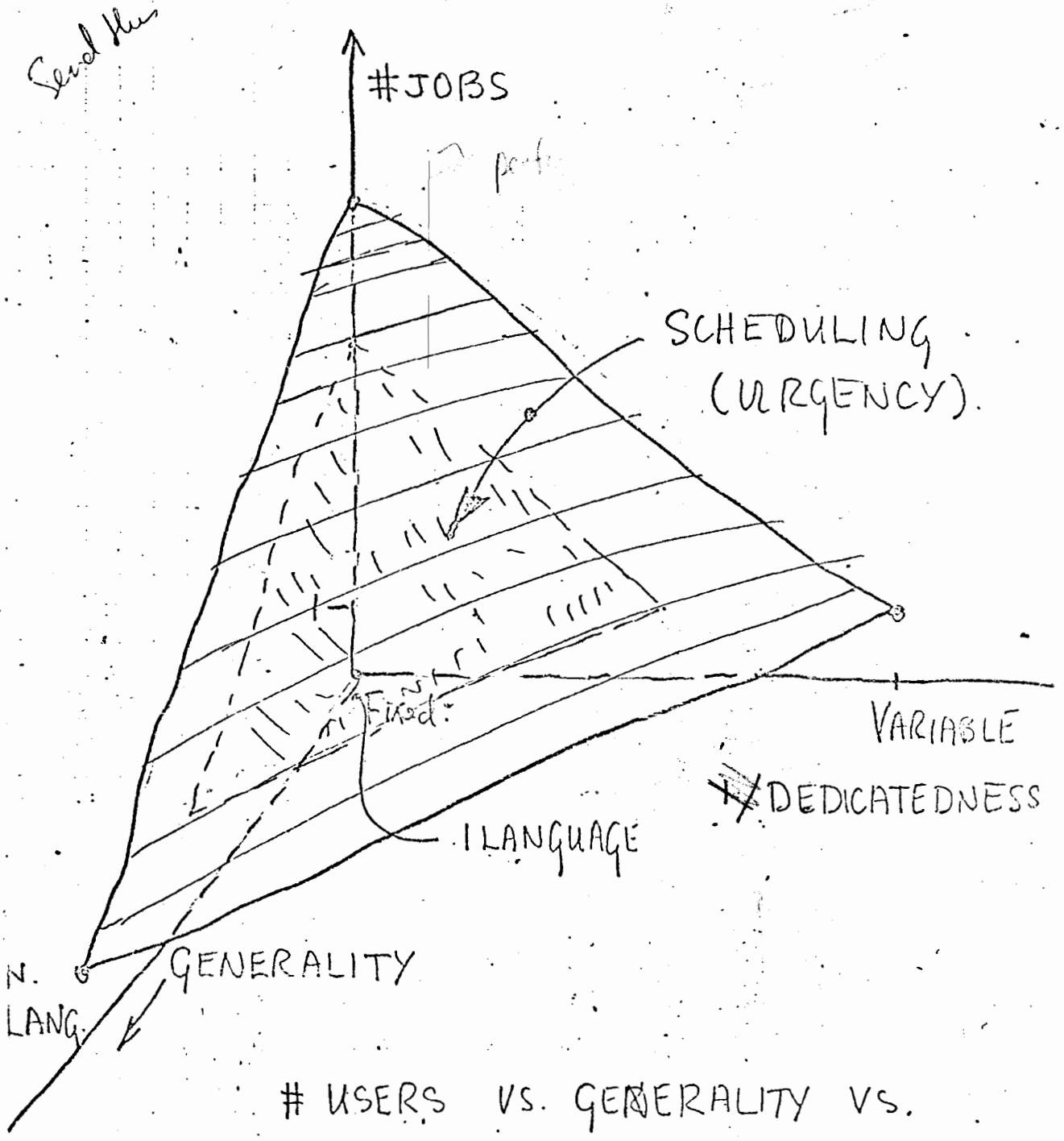
DEC's MKT SEGMENTATION.

BASICS
- OEM – IRON COMPONENTS/SYSTEMS
- DCG – COMPONENTS (BOARD LEVEL)

END USE
- EDUCATION.
- ENG. COMPUTATION
- INDUSTRIAL.
- BUSINESS.
- LABORATORY.
- COMMUNICATIONS.

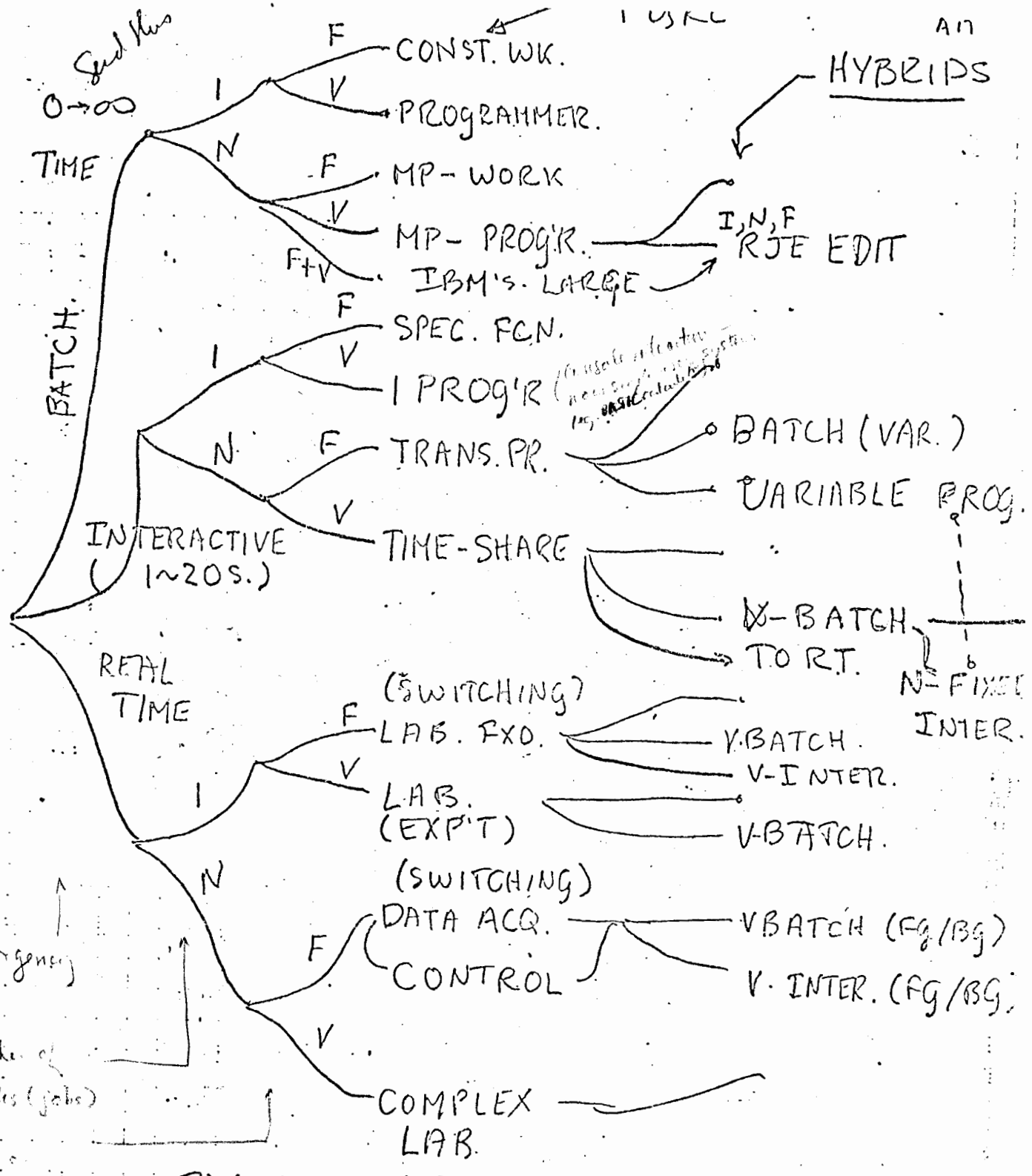
TURN-KEY
- TYPESETTING.

Fig 4

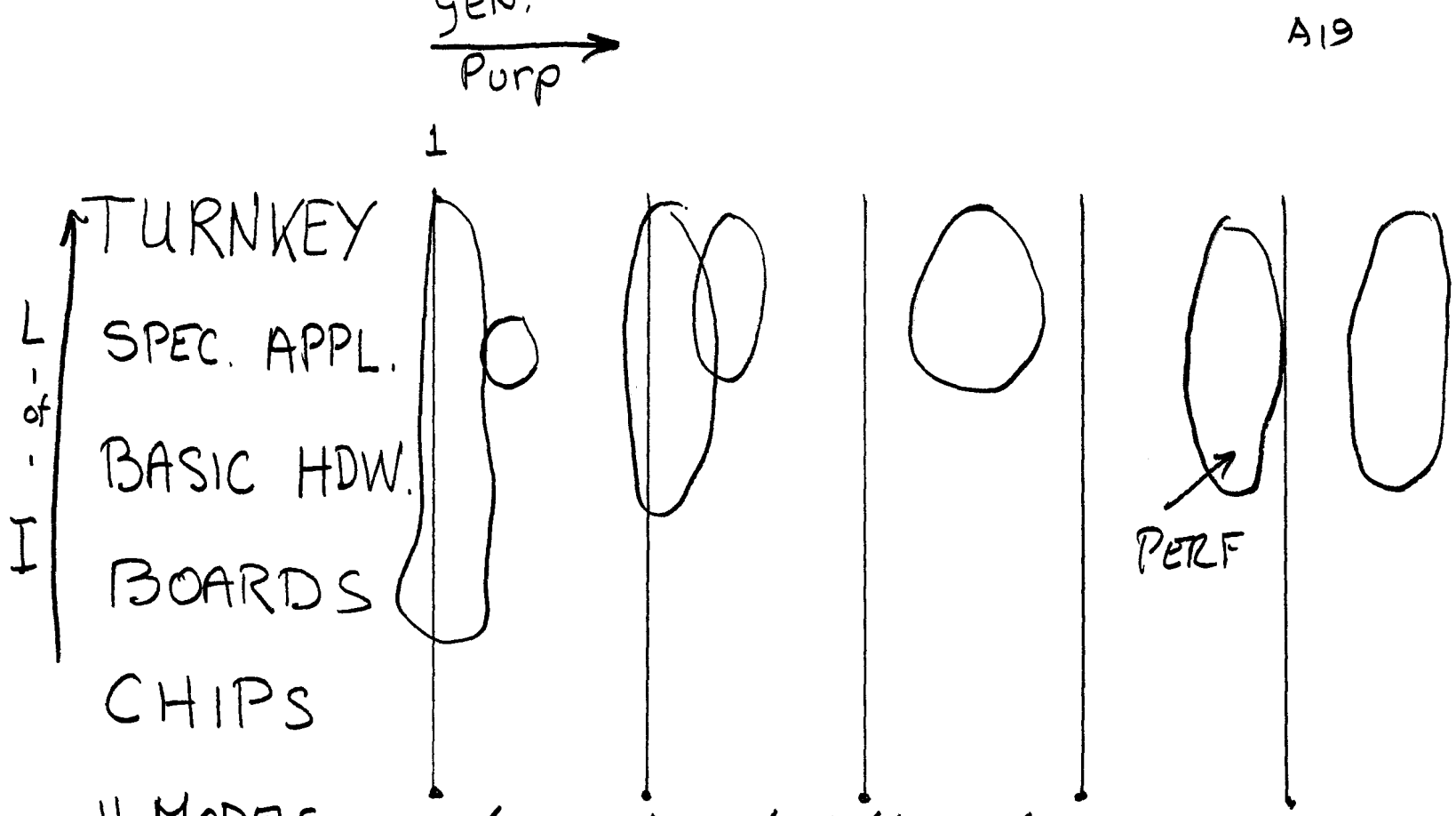


USERS VS. GENERALITY VS. DEDICATEDNESS FOR VARIOUS FUNCTIONAL SYSTEMS (IE. SCHEDULE URGENCY)

GB.
2/13/76

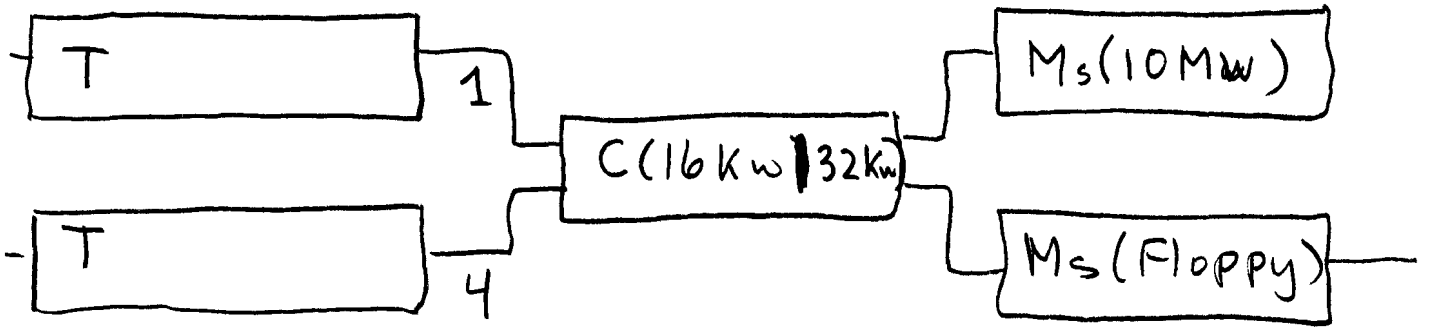


TAXONOMY OF SYSTEM STRUCTURES

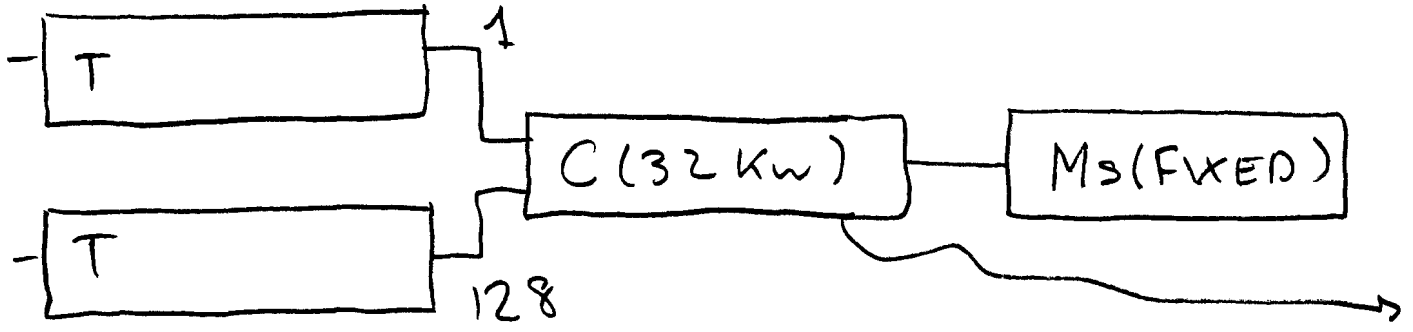


11 MODELS:	03	04	05	34	40	45	70
PRICE	.6-10		2-20		10-50	30-150	50-250
PERF. (Basic)	1		2		4	10	20
Perf. (Sci)	3		1		5	40	70
Perf ~ Price^2	1		4		25	225	625
Perf ~ Price$^{\frac{1}{2}}$	1		2		5	15	25
Mem. Size	(1) 4K-28Kw				-128Kw (32)		(256) 1Mw

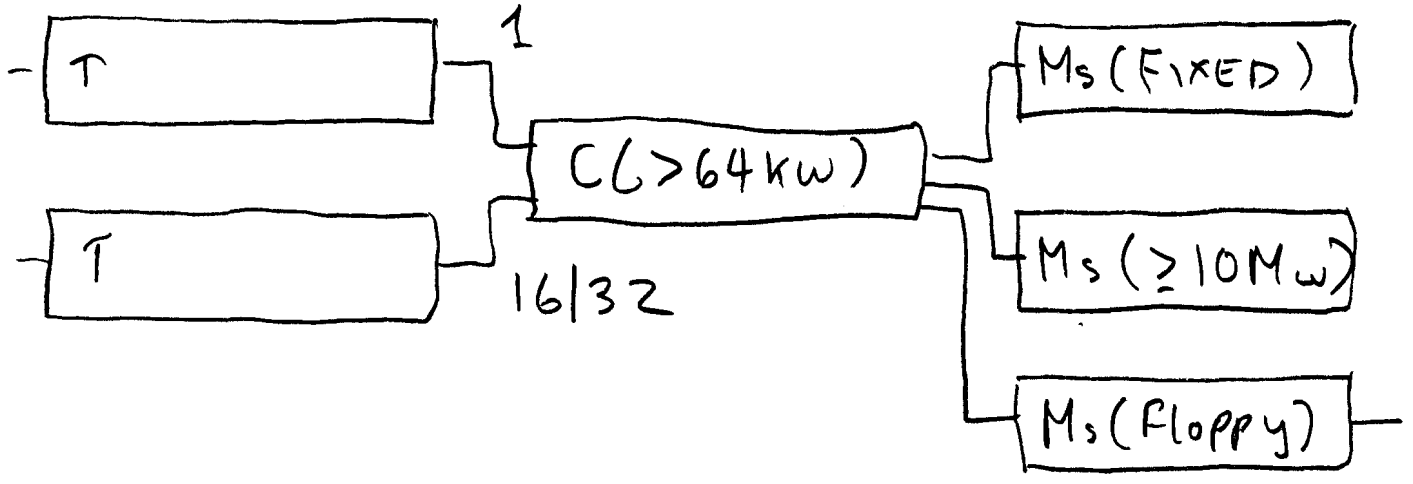
1 USER; FIXED OR VAR. USE



1~4|8 USER; ~~V~~RIABLE | FIXED USE



128 USER; FIXED FUNCTION (EG. CONCENT., MESSAGE SWITCH).



16|32 USER; VAR ~~FIXED~~; I|L LANGUAGES.

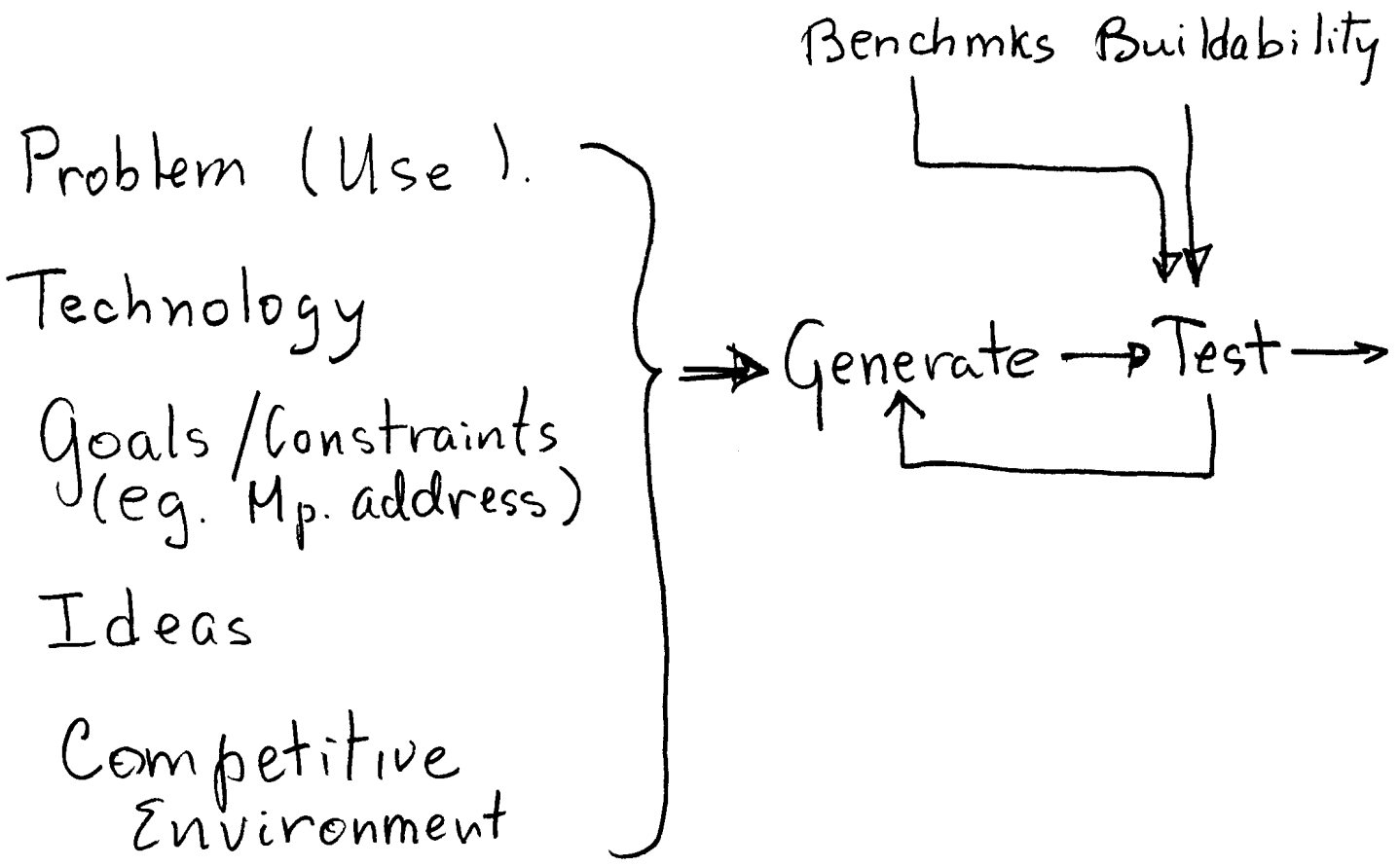
The Instruction-set Processor (ISP): 41

- Language for specifying Algorithms
- Supports all "Outer-level" Machines:
  - Applications (spec. languages, inter-comm.)
  - Languages (Higher level-type as we know)
  - Operating-Systems.

Control of i/o, Secondary memory
Scheduling & Resource alloc. (MP)
Parallelism (co-operating seq. process.)
Inter-process Comm. (interrupts.)

Data-types & Corresponding Oper's.
Procedures & Control
Access of Data. Structures
Compilers & Interpreters

Sharing and ... Protecting data
Inter-process Comm.



- ISP. size (i.e. Goodness) ≈ Required Data-types.
- # bits to encode algorithm = 1:3
- Performance ≈ Speed × # bits

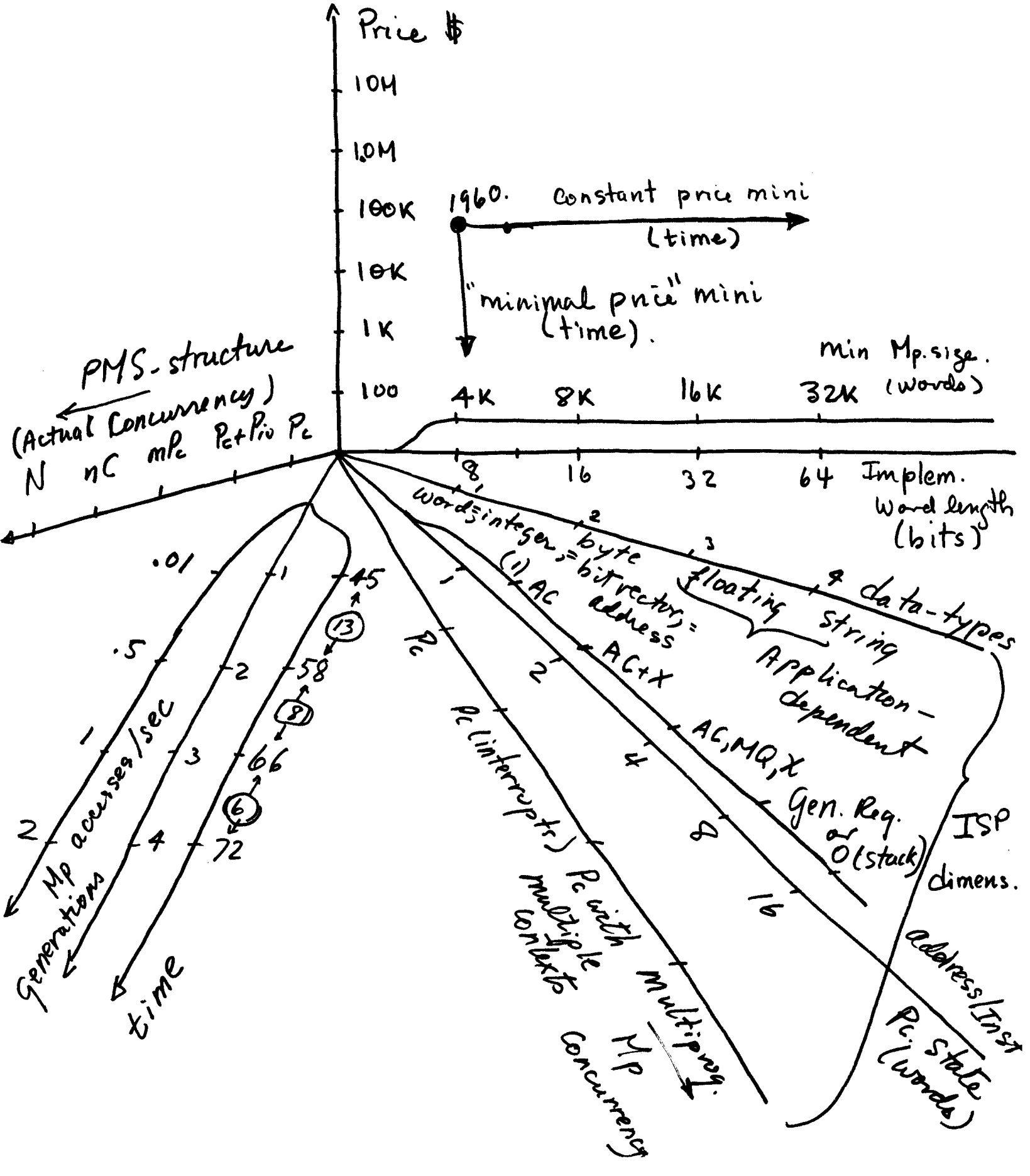
Mini ISP vs "Other"

Emphasis on mini(mum):

- Encoding
- # of registers (Pc. state)
- Inter-process switching
- Sharing.
- Fewest data-types → Flt. / String.

GB 1/10/76.
43

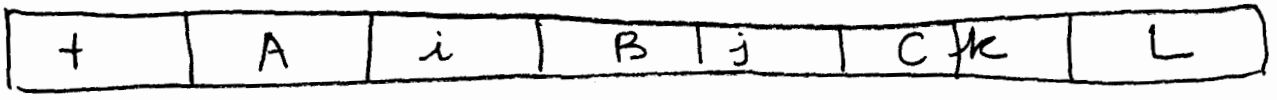
Basic hardware-oriented C-space dimensions (emphasis on mini)



Instructions specify how to access and 24
Operate on Mem. Space & what to do next

- Accessing: Primary Memory → Orthogonal.
  : Processor State → Orthogonal.
  ↑ Vectors.
- Data-types ⇐⇒ Data-operators
  - Completeness
  - f(problem)
- Processor-state & Operators ⇒ # addresses / Instruction
- Memory Management ~~for Multi-programs~~
  - of physical memory.
  - for multi-programs / processes
  - Intercommunication (implied)
  - Sharing and/or protection (req'd.)

Instruction:



$A[i] \leftarrow B[j] + C[k]$; goto L

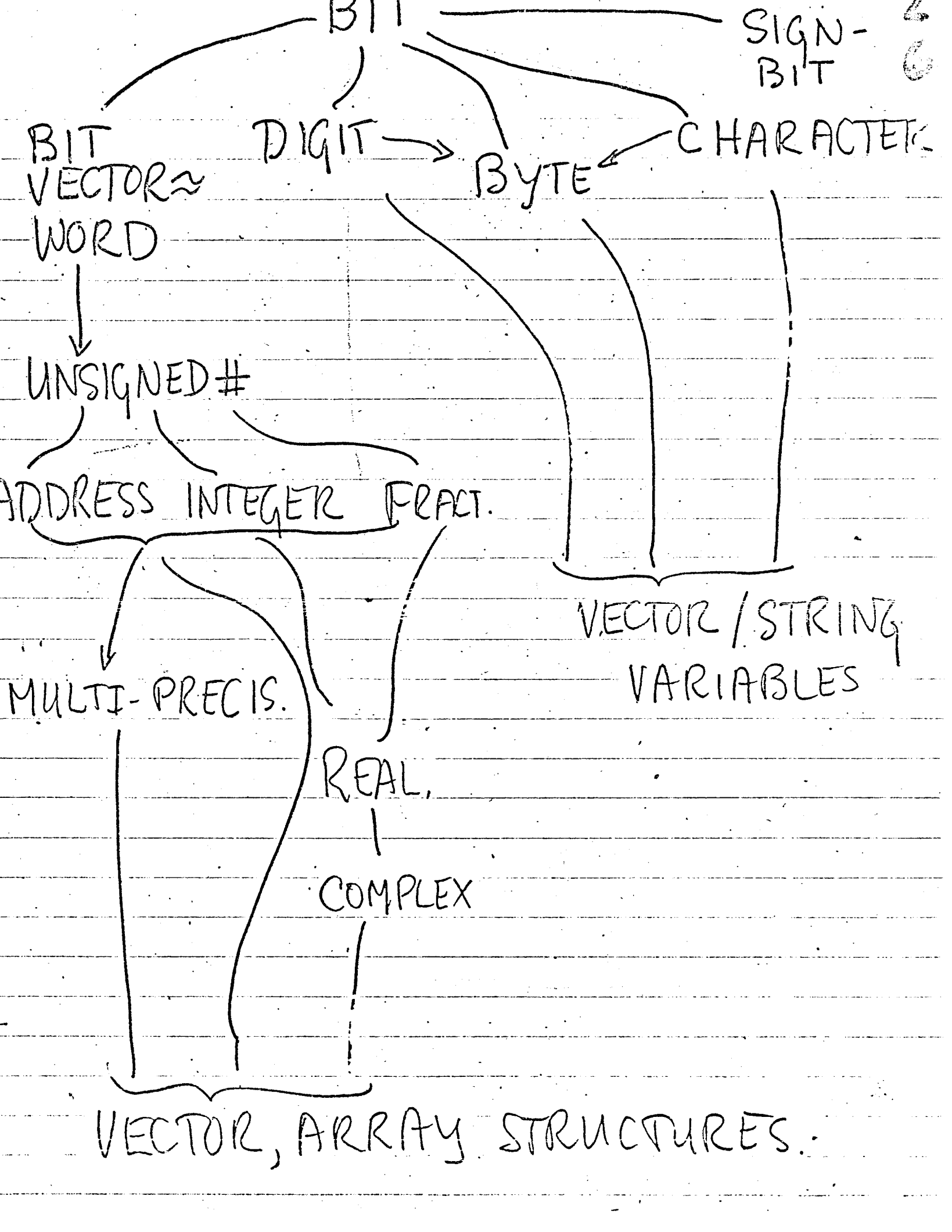
Access : Related to data-type

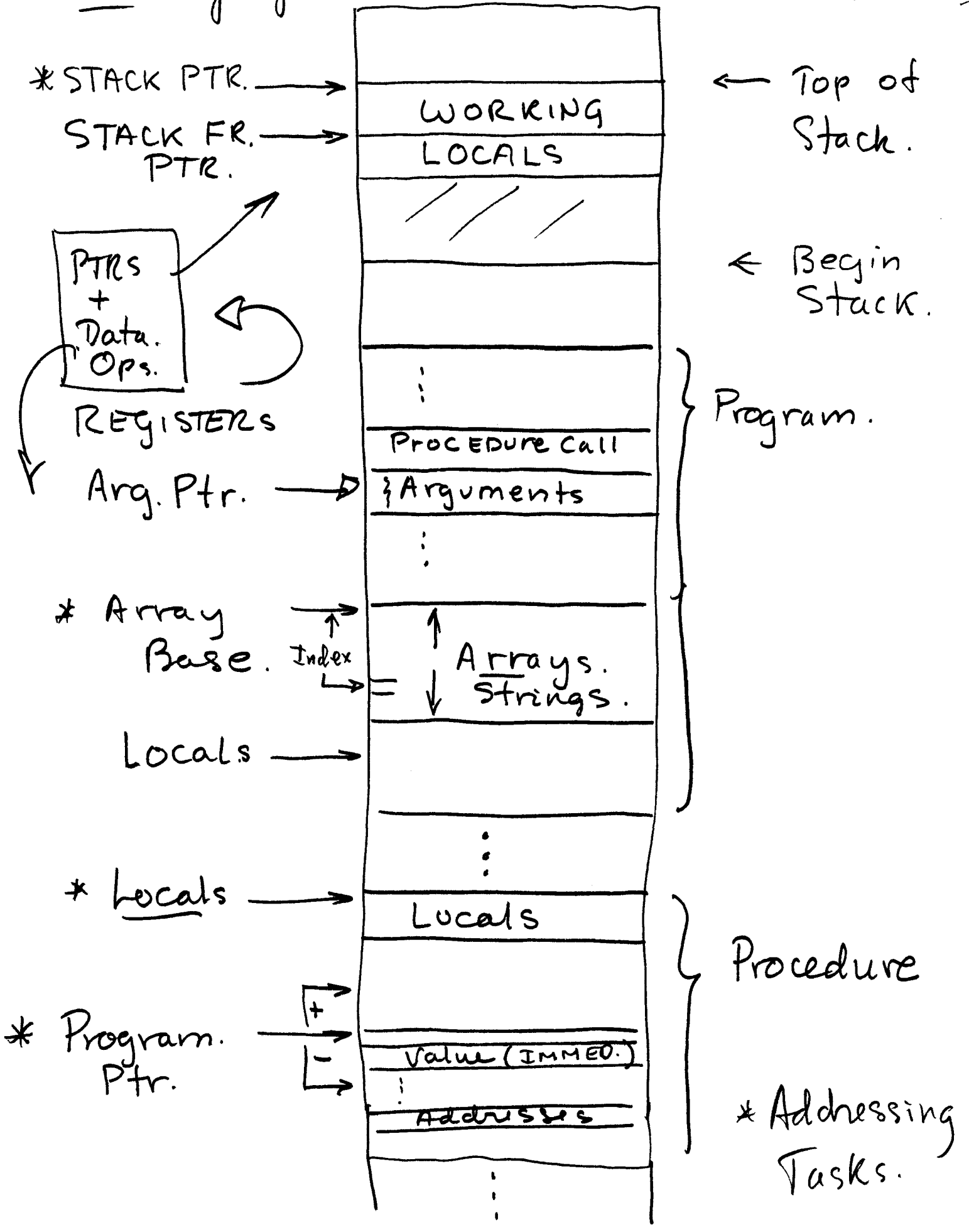
bit, digit, byte (character), field, word(s), multiple lower levels (ie. strings & vectors)

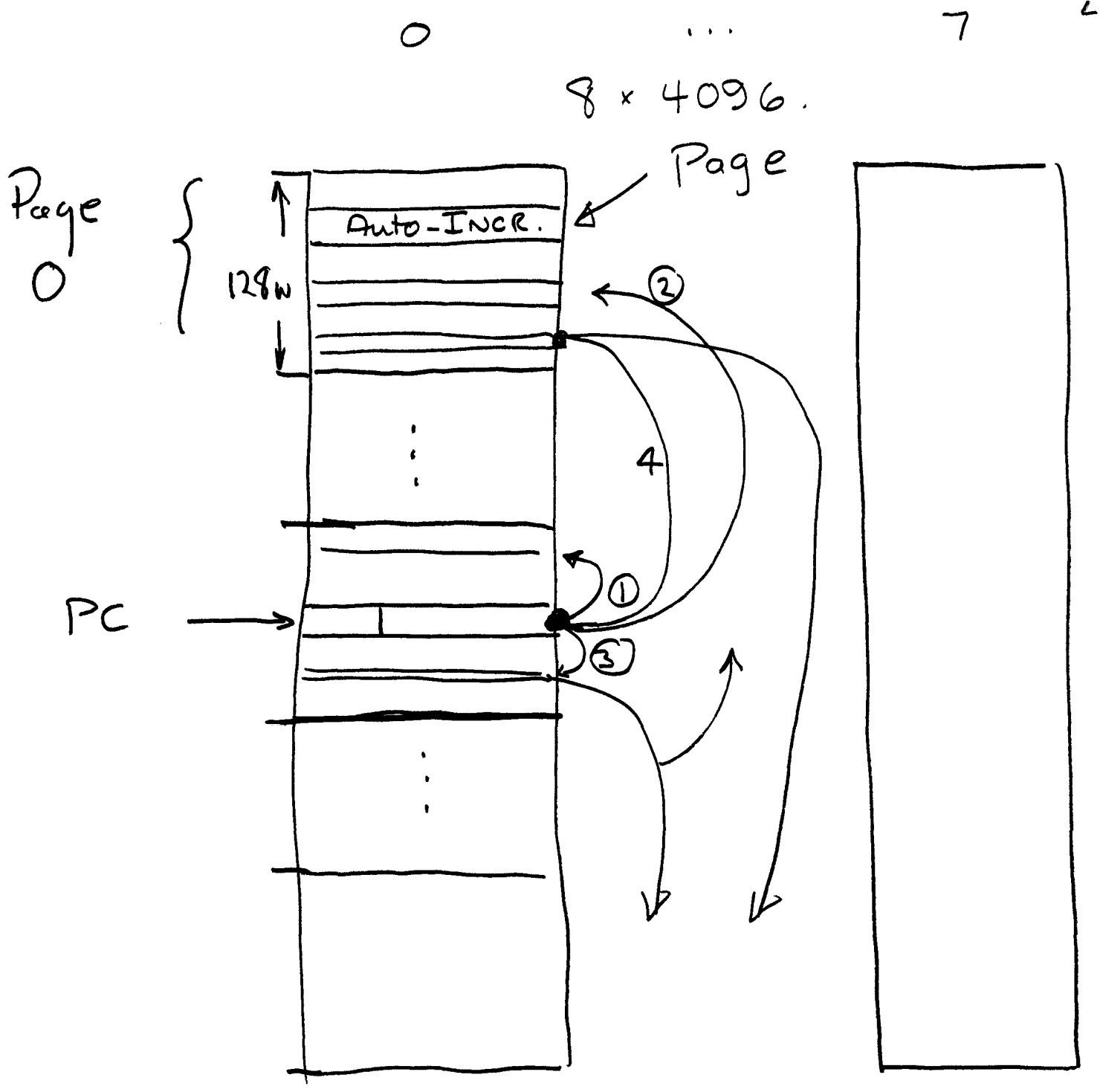
Access : Based on Accessors Mechanisms

- Indexing for Vectors, Arrays, strings
- Bases for program entities:
  Locals, Procedure parameters, Stacks, Queues, Array bases. Arguements

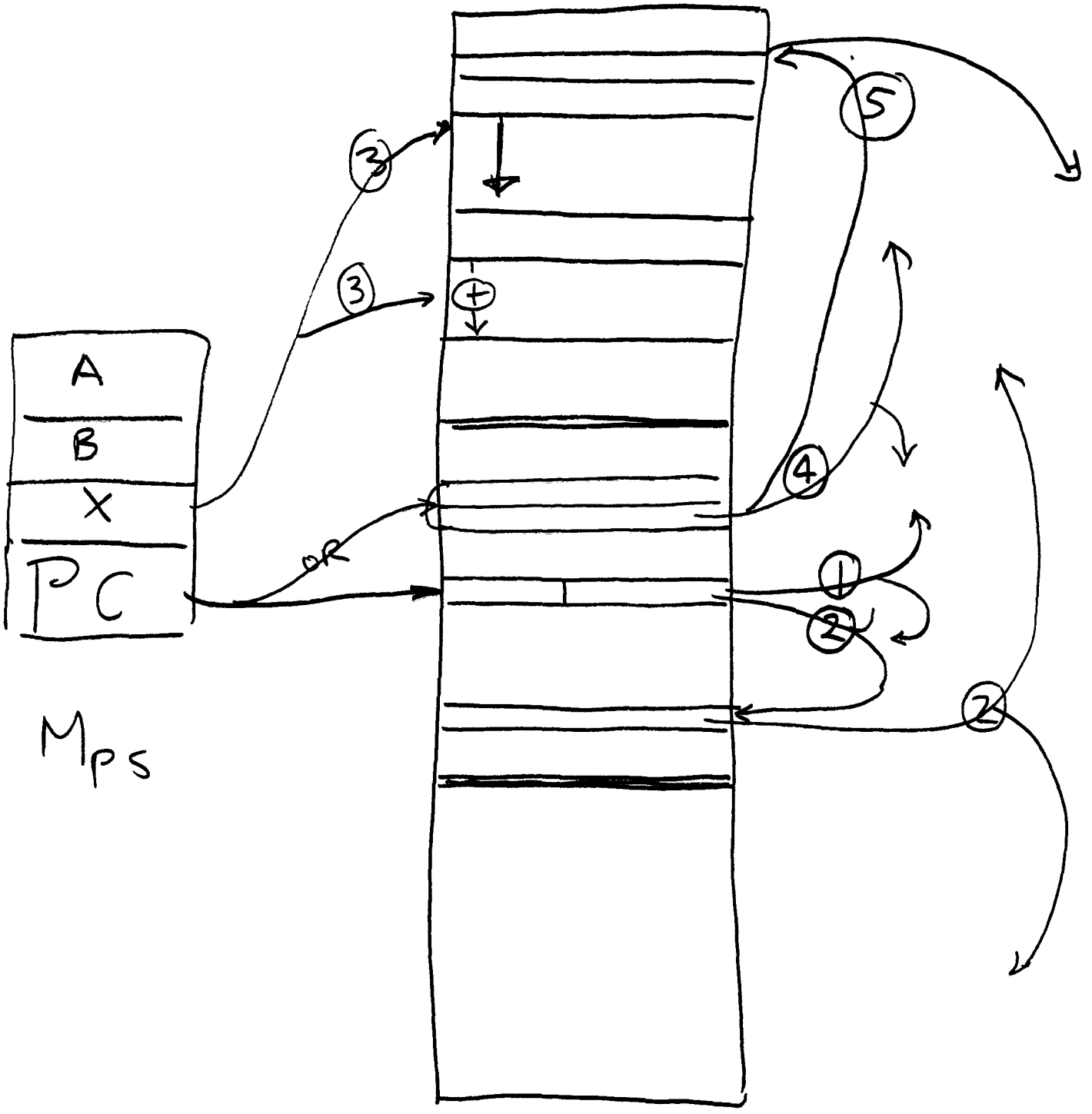
Many problems arise due to mapping into linear address-space.


BIT
SIGN-BIT
BIT VECTOR≈ WORD
DIGIT
BYTE
CHARACTER
UNSIGNED #
ADDRESS
INTEGER
FRACT.
VECTOR / STRING VARIABLES
MULTI-PRECIS.
REAL
COMPLEX
VECTOR, ARRAY STRUCTURES.


* STACK PTR.
STACK FR. PTR.
WORKING
LOCALS
← Top of Stack.
← Begin Stack.
PTRs + Data. Ops.
REGISTERS
PROCEDURE CALL
Arg. Ptr.
Arguments
Program.
* Array Base.
Index
Arrays. Strings.
Locals
* Locals
Locals
Procedure
* Program. Ptr.
+
-
Value (IMMED.)
Address
* Addressing Tasks.



PDP-8.

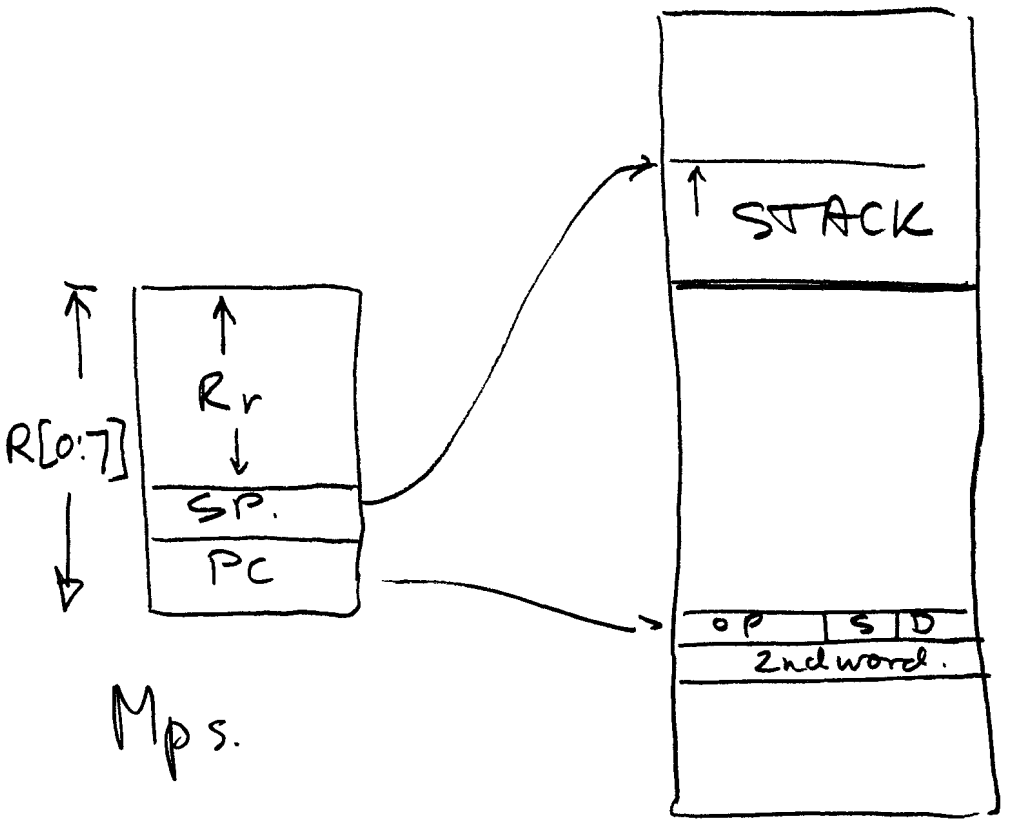


M_{PS}

$M_P = 2^{15}$

HP 2100

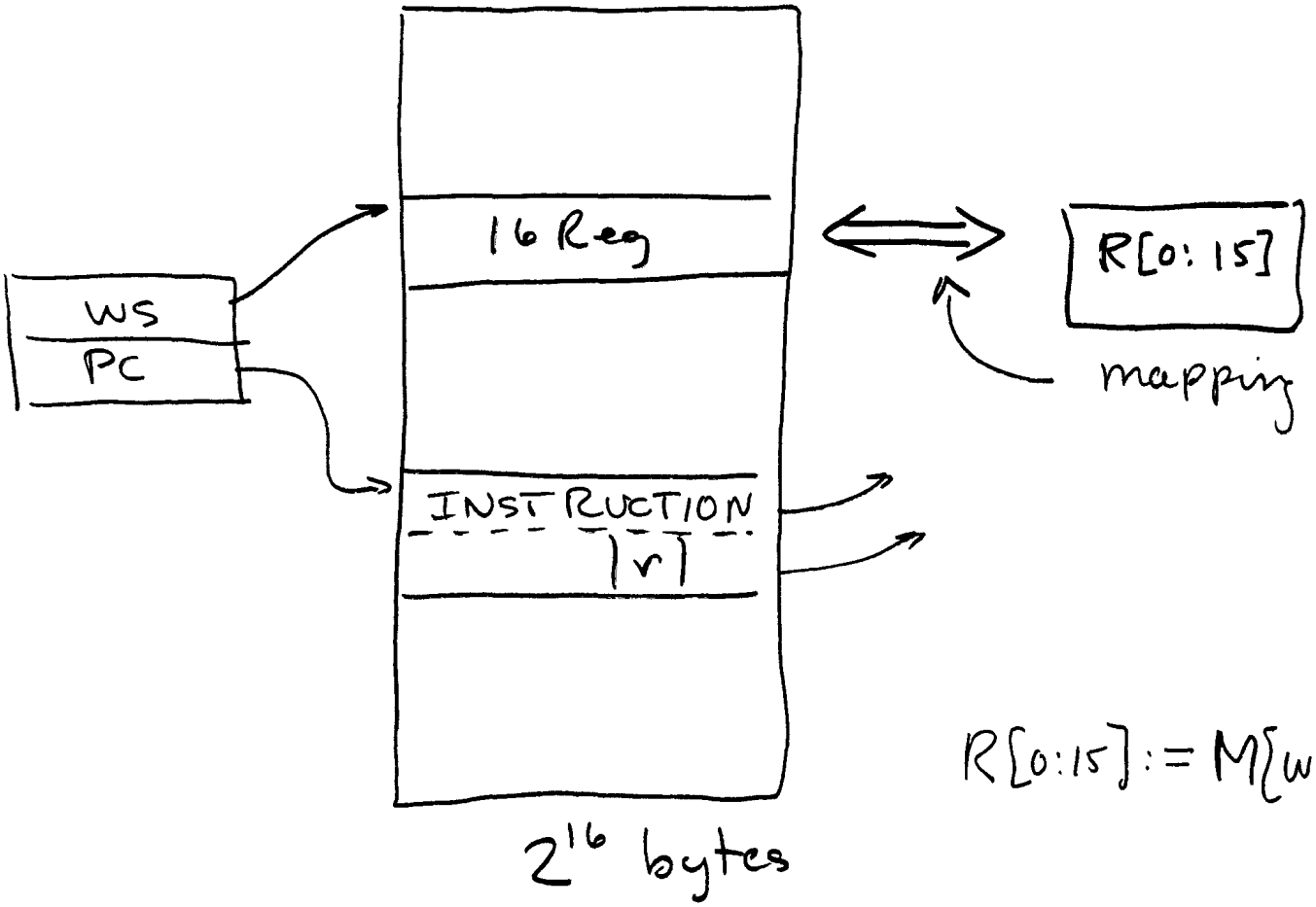
PDP-11 Addressing



for Source / Dest gives 8×8 Access Modes.

Reg.	R[r] - directs.	0
pop	M[R[r]] ; next R[r] ← R[r] + ai	1 note immediate too
push	R[r] ← R[r] - ai ; M[R[r]]	2
	M[2nd word + R[r]]	3 Indexed OR BASE Relative if R[r] = PC
	M[R[r]] indirects	4
≡ (	M[M[Rr]] ; R[r] ← R[r] + ai	5 indirect. stack. Pop
	M[M[PC]]	direct absolute
	R[r] ← R[r] - ai ; M[M[Rr]]	6 indirect push
↱	M[M[2nd word + R[r]]]	7 ind. indexed
↳	M[M[2nd word + PC]]	ind. relative

TI — 9900 Addressing.



$R[0:15] := M[WS:WS+15]$

Register.	R[r]
" indirect	M[R[r]] := M[M[ws+r]]
" " auto	M[R[r]]; next R[r] ← R[r]+2
Symbolic direct	M[M[PC+2]]
Indexed address.	M[R[r] + M[PC+2]]
Immediate	M[PC+2]
PC Relative	PC + disp
PC " +	<R[r] + disp> bit addr.

Data-types / Data-Ops

integers.
doubles
real
:
Complex

} { $x \leftarrow y \; f \; z$ } 2 or 3 Operands

} {
+
− and inv.?
×
/ and inv?
mod.
> ≥ = < ≤ ≠ } Compare part.
+ trigs, etc.
}

note } address.
2 if 0 implied

{ Booleans - 1 bit
Boolean word (vector)
fields

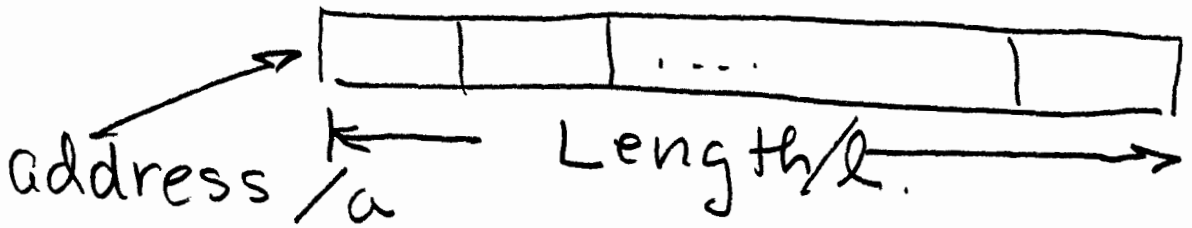
{ 2 or 3 Operands
$x \leftarrow y \; f \; z$.

} { 16 ops }

Strings 2/3 ops.

Arithmetic
Compare.
moves.
translate
Search.

Accessing Data-types (eg. strings)



Length Spec.

fixed (eg. 10 d.)

variable, but in instruction (worst)

tag.
- eat head or tail by count or mark flag. 360. 1401.
- another parameter. d(a, l).
- descriptor with a, l.

global register

Program it... not built in... Someone will

Feustel 1973 - Tagged Arch.

Arith: Int, Real., Long Int., Long Real, Complex, long Compler, Mixed

Structure: Vector, Matrix, Matrix (Arith.) Sparse Vector.

Structures: Q, double/single linked List, Stack,

Process: Semaphore, Event, message, Interrupt-of., I-d.

Procedures: Proc, Name of Var, formal, Label, Reference to, Parameter-list

Undefined; Garbage

Machine State and Instructions

File

CHAR, BOOLEAN

Number of Registers = Proc. State

≈ Addresses / Inst.

→ Lots – Explicit binding (B5500 → HP3000)
= 0 addresses / instruction.

1 or 2 = No permanent assignment, much flexibility, compute everything.
4 = Too Few. Too Much to do.
} ≈

→ >4 (able to be assigned) = Working Arithmetic Temporary in loops.
Access to Program data str.:
(Stack, Locals, arguments) → Base.
Access to User Data Structure
(arrays, strings) – Index
– Base
Global data (bits).

>8 Lots to remember if assembly lang.
" to store.

Appendix 1

DEC PDP-8 ISP Description

```
Pc State
    AC<0:11>                                    Accumulator
    L                                           Link bit/AC extension for overflow and carry
    PC<0:11>                                    Program Counter
    Run                                         1 when Pc is interpreting instructions or "running"
    Interrupt_state                             1 when Pc can be interrupted; under programmed control
    IO_pulse_1; IO_pulse_2; IO_pulse_4          IO pulses to IO devices

Mp State
Extended memory is not included.
    M[0:7777_8]<0:11>
        Page_0[0:177_8]<0:11> := M[0:177_8]<0:11>       special array of directly addressed memory registers
        Auto_index[0:7]<0:11> := Page_0[10_8:17_8]<0:11>  special array when addressed indirectly,is incremented by 1

Pc Console State
Keys for start, stop, continue, examine (load from memory), and deposit (store in memory) are not included.
    Data switches<0:11>                         data entered via console

Instruction Format
    instruction/i<0:11>
        op<0:2>             := i<0:2>           op code
        indirect_bit/ib     := i<3>             0, direct; 1 indirect memory reference
        page_0_bit/p        := i<4>             0 selects page 0; 1 selects this page
        page_address<0:6>   := i<5:11>
        this_page<0:4>      := PC'<0:4>
        PC'<0:11>           := (PC<0:11> -1)
        IO_select<0:5>      := i<3:8>           selects a T or Ms device
        io_p1_bit           := i<11>            these 3 bits control the selective generation of -3 volts,
        io_p2_bit           := i<10>             0.4 μs pulses to I/O devices
        io_p4_bit           := i<9>
        sma                 := i<5>             μ bit for skip on minus AC, operate 2 group
        sza                 := i<6>             μ bit for skip on zero AC
        snl                 := i<7>.            μ bit for skip on non zero Link

Effective Address Calculation Process
    z<0:11> := (                                effective
        ¬ib → z";
        ib ∧ (10_8 ≤ z" ≤ 17_8) → (M[z"] ← M[z"] + 1; next);    auto indexing
        ib → M[z"])
    z'<0:11> := (¬ ib → z"; ib → M[z"])
    z"<0:11> := (page_0_bit → this_page□page_address;       direct address
                 ¬page_0_bit → 0□page_address)
```

μ *microcoded instruction or instruction bit(s) within an instruction*

APPENDIX 1 DEC PDP-8 ISP DESCRIPTION (Continued)

```
Instruction Interpretation Process
   Run^Λ ¬ (Interrupt_request Λ Interrupt_state) → (          no interrupt interpreter
      instruction ← M[PC]; PC ← PC + 1; next                 fetch
      instruction_execution);                                execute
   Run Λ Interrupt_request Λ Interrupt_state → (              interrupt interpreter
      M[0] ← PC; Interrupt_state ← 0; PC ← 1)

Instruction Set and Instruction Execution Process
   Instruction_execution := (
      and (:= op = 0) → (AC ← AC Λ M[z]);                    logical and
      tad (:= op = 1) → (L□AC ← L□AC + M[z]);                two's complement add
      isz (:= op = 2) → (M[z'] ← M[z] + 1; next              index and skip if zero
                         (M[z'] = 0') → (PC ← PC + 1));
      dca (:= op = 3) → (M[z] ← AC; AC ← 0);                 deposit and clear AC
      jms (:= op = 4) → (M[z] ← PC; next PC ← z + 1);        jump to subroutine
      jmp (:= op = 5) → (PC ← z);                            jump
      iot (:= op = 6) → (                                    μ in out transfer, microprogrammed to generate up to 3 pulses
         io_p1_bit → IO_pulse_1 ← 1; next                     to an io device addressed by IO_select
         io_p2_bit → IO_pulse_2 ← 1; next
         io_p4_bit → IO_pulse_4 ← 1);
      opr (:= op = 7) → Operate_execution                    the operate instruction is defined below
                  )                                          end Instruction execution

Operate Instruction Set
The microprogrammed operate instructions: operate group 1, operate group 2, and extended arithmetic are defined as a separate
 instruction set.
   Operate_execution := (
      cla (:= i<4> = 1) → (AC ← 0);                          clear AC. Common to all operate instructions.
      opr_1 (:= i<3> = 0) → (                                operate group 1
         cll (:= i<5> = 1) → (L ← 0); next                   μ clear link
         cma (:= i<6> = 1) → (AC ← ¬ AC);                    μ complement AC
         cml (:= i<7> = 1) → (L ← ¬ L); next                 μ complement L
         iac (:= i<11> = 1) → (L□AC ← L□AC + 1); next        μ increment AC
         ral (:= i<8:10> = 2) → (L□AC ← L□AC × 2 {rotate});  μ rotate left
         rtl (:= i<8:10> = 3) → (L□AC ← L□AC × 2^2 {rotate}); μ rotate twice left
         rar (:= i<8:10> = 4) → (L□AC ← L□AC / 2 {rotate});  μ rotate right
         rtr (:= i<8:10> = 5) → (L□AC ← L□AC / 2^2 {rotate})); μ rotate twice right
      opr_2 (:= i<3,11> = 10) → (                            operate group 2
         skip condition ⊕ (i<8> = 1) → (PC ← PC + 1); next   μ AC,L skip test
            skip condition := ((sma Λ (AC < 0)) ∨ (sza Λ (AC = 0)) ∨ (snl Λ L))
         osr (:= i<9> = 1) → (AC ← AC ∨ Data switches);      μ "or" switches
         hlt (:= i<10> = 1) → (Run ← 0));                    μ halt or stop
      EAE (:= i<3,11> = 11) → EAE_instruction_execution).    optional EAE description
```

Pc State

AC<0:11>

L

PC<0:11>

Run

Interrupt␣state

IO␣pulse␣1; IO␣pulse␣2; IO␣pulse␣4

Mp State
Extended memory is not included.

M[0:7777_8]<0:11>

Page␣0[0:177_8]<0:11> := M[0:177_8]<0:11>

Auto␣index[0:7]<0:11> := Page␣0[10_8:17_8]<0:11>

Pc Console State
Keys for start, stop, continue, examine (load from memory

Data switches<0:11>

Instruction Format

```
instruction/i<0:11>
    op<0:2>                 := i<0:2>
    indirect␣bit/ib         := i<3>
    page␣0␣bit/p            := i<4>
    page␣address<0:6>       := i<5:11>
    this␣page<0:4>          := PC'<0:4>
    PC'<0:11>               := (PC<0:11> -1)
    IO␣select<0:5>          := i<3:8>
    io␣p1␣bit               := i<11>
    io␣p2␣bit               := i<10>
    io␣p4␣bit               := i<9>
    sma                     := i<5>
    sza                     := i<6>
    snl                     := i<7>
```

Effective Address Calculation Process

```
z<0:11> := (
    ¬ib → z'';
    ib ∧ (10₈ ≤ z'' ≤ 17₈) → (M[z''] ← M[z''] + 1; next);
    ib → M[z''])
z'<0:11> := (¬ ib → z''; ib → M[z''])
z''<0:11> := (page␣0␣bit → this␣page□page␣address;
              ¬page␣0␣bit → 0□page␣address)
```

μ *microcoded instruction or instruction bit(s) within an ins*

Instruction Interpretation Process

```
Run ∧ ¬ (!Interrupt_request ∧ Interrupt_state) → (
    instruction ← M[PC]; PC ← PC + 1; next
    instruction_execution);
Run ∧ Interrupt_request ∧ Interrupt_state → (
    M[0] ← PC; Interrupt_state ← 0; PC ← 1)
```

Instruction Set and Instruction Execution Process

```
Instruction_execution := (
    and (:= op = 0) → (AC ← AC ∧ M[z]);
    tad (:= op = 1) → (L□AC ← L□AC + M[z]);
    isz (:= op = 2) → (M[z'] ← M[z] + 1; next
                       (M[z'] = 0) → (PC ← PC + 1));
    dca (:= op = 3) → (M[z] ← AC; AC ← 0);
    jms (:= op = 4) → (M[z] ← PC; next PC ← z + 1);
    jmp (:= op = 5) → (PC ← z);
    iot (:= op = 6) → (
        io_p1_bit → IO_pulse_1 ← 1; next
        io_p2_bit → IO_pulse_2 ← 1; next
        io_p4_bit → IO_pulse_4 ← 1);
    opr (:= op = 7) → Operate_execution
```

Operate Instruction Set
The microprogrammed operate instructions: operate group 1, operate instruction set.

```
Operate_execution := (
    cla (:= i<4> = 1) → (AC ← 0);
    opr_1 (:= i<3> = 0) → (
        cll (:= i<5> = 1) → (L ← 0); next
        cma (:= i<6> = 1) → (AC ← ¬ AC);
        cml (:= i<7> = 1) → (L ← ¬ L); next
        iac (:= i<11> = 1) → (L□AC ← L□AC + 1); next
        ral (:= i<8:10> = 2) → (L□AC ← L□AC x 2 {rotate});
        rtl (:= i<8:10> = 3) → (L□AC ← L□AC x 2^2 {rotate});
        rar (:= i<8:10> = 4) → (L□AC ← L□AC / 2 {rotate});
        rtr (:= i<8:10> = 5) → (L□AC ← L□AC / 2^2 {rotate}));
    opr_2 (:= i<3,11> = 10) → (
        skip condition ⊕ (i<8> = 1) → (PC ← PC + 1); next
            skip condition := ((sma ∧ (AC < 0)) ∨ (sza ∧ (AC = 0))
        osr (:= i<9> = 1) → (AC ← AC ∨ Data switches);
        hlt (:= i<10> = 1) → (Run ← 0));
    FAE (:= i<3,11> = 11) → EAF_instruction_execution)
```

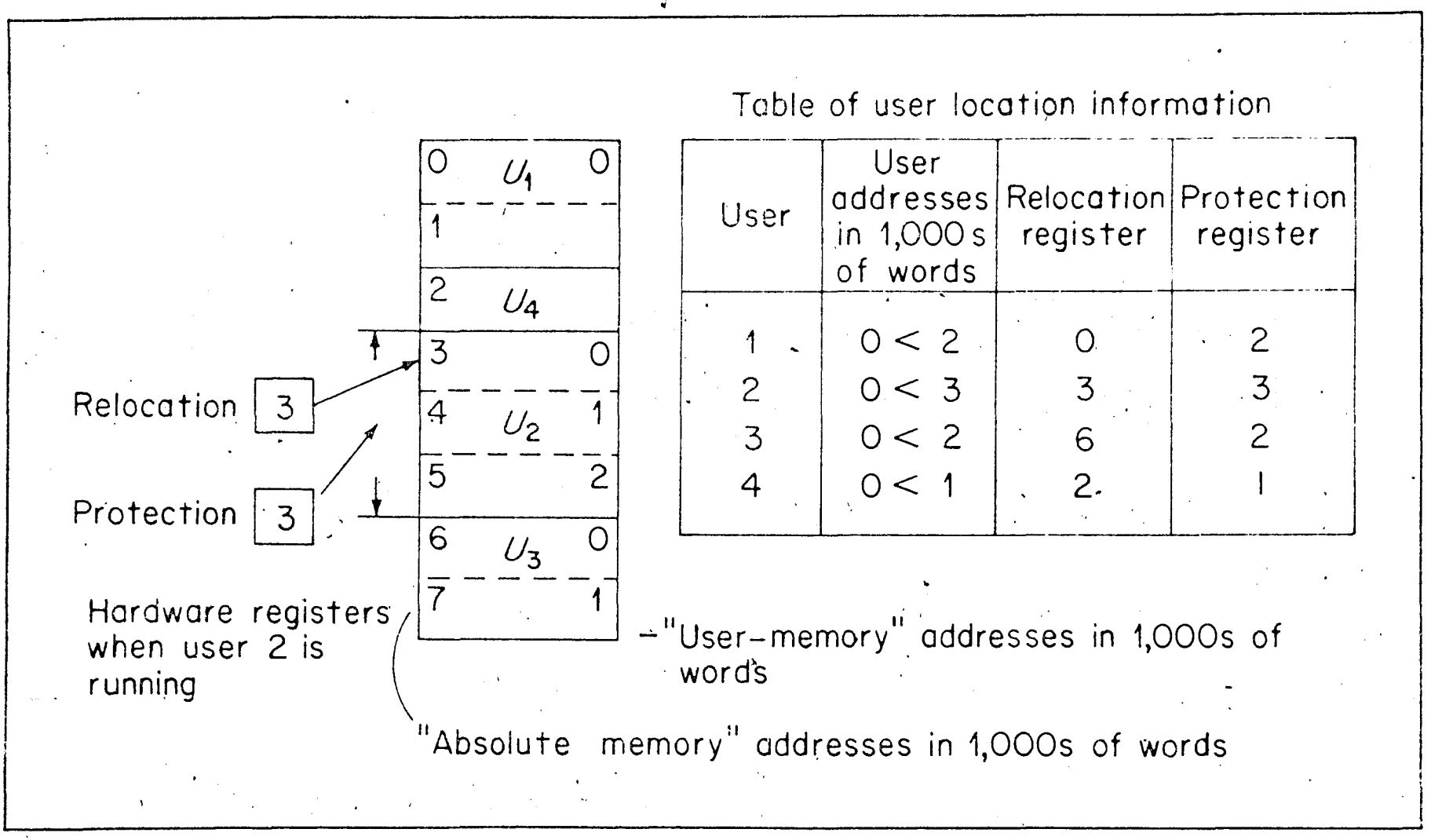


Fig. 15. Memory allocation using a boundary (relocation and protection) register.

MEMORY MANAGEMENT.

- By Program.
- By: Cells, Pages, Memory
- 1, 2, or N Regions and with.
  Relocation (Base + Protection)

→ Paging

- SEGMENTATION (AND/-) PAGING

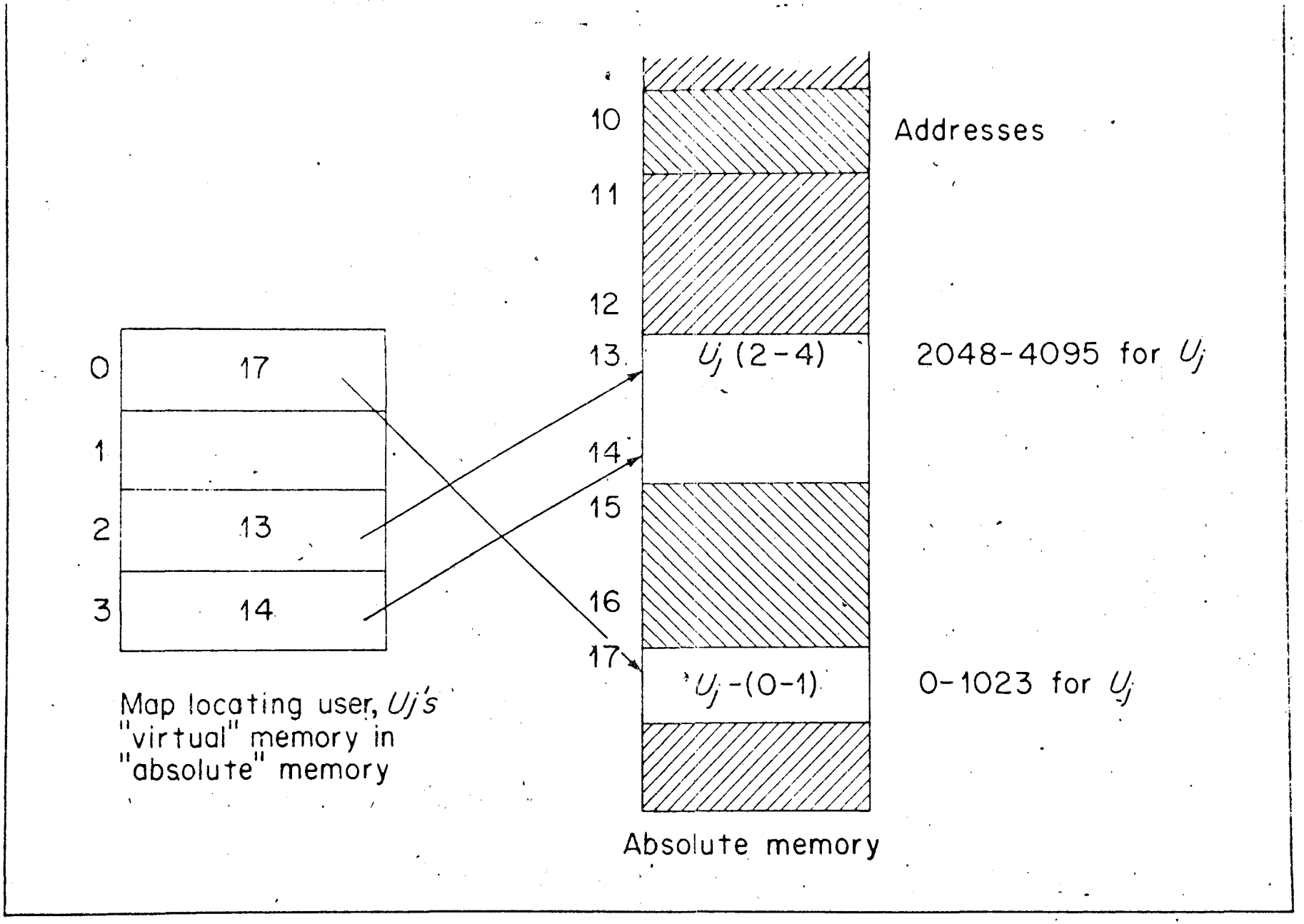


Fig. 16. Memory allocation using a page allocation map.

PARALLELISM: BASIS FOR MULTI-PC's

STATIC (I.E. RELIABLE)

- INDEPENDENT PARTITIONS: — DYNAMIC STOCKROOM.
- FUNCTIONAL SEPERATION - FRONT/BACK END / PRE-PROC. /

- INDEPENDENT
  - JOBS (T/S)
  - PROCESSES (TRANSACTION PROC.)
  - BATCH STREAMS
- SET PARALLELISM (PROC. CONT)
- ARRAYS, VECTORS
- GENERALLY CONCURRENT PROCESSES.

BASIC RATIONALE FOR m P's

USER
- PERFORMANCE
- Δ PERFORMANCE AND RANGE
- AVAILABILITY VIA REDUNDANCY

MFG.
- COST (BETTER SPARES, MANUFACTURING)
- LESS DESIGNS

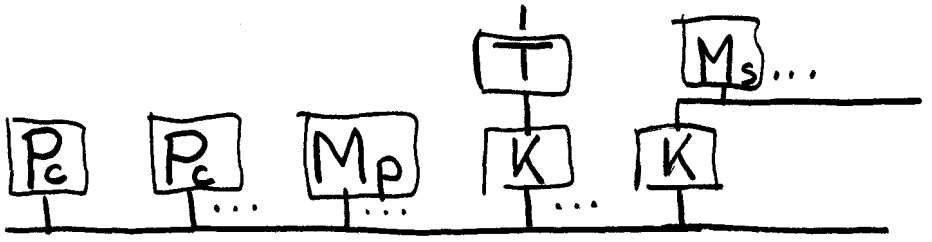
BASIC IRRATIONALE FOR m P's.

- NO-PROGRAMS
- HIGH DEV. RISK.
- UNIPROCESSORS ARE MORE COST/EFF.
- BETTER PLAN

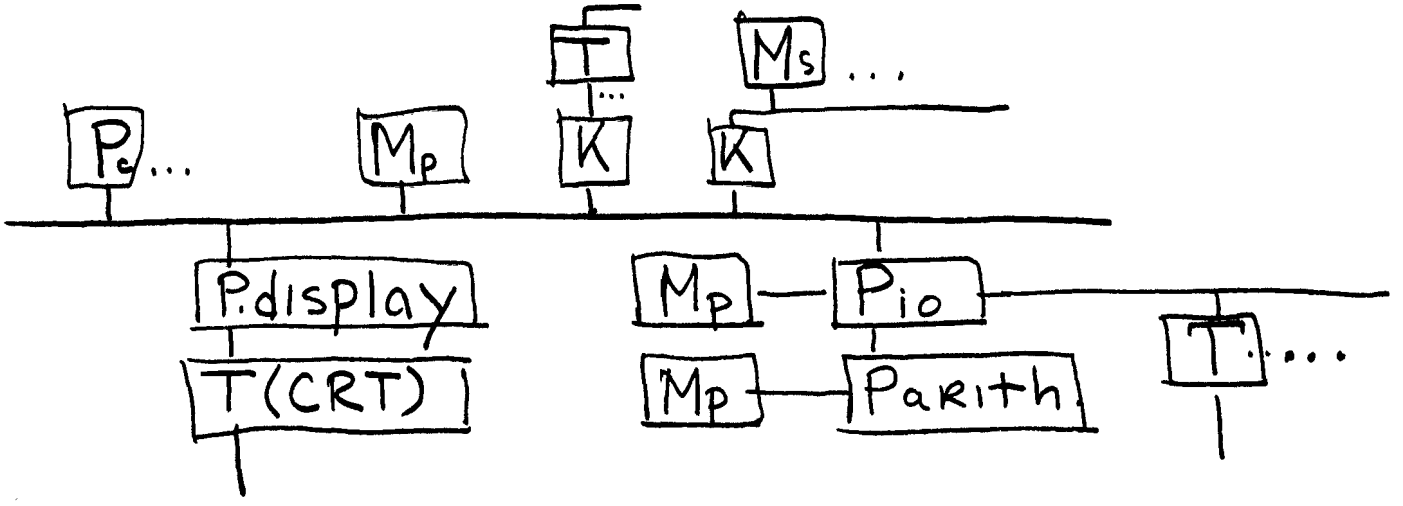
$$\#\frac{\text{ACCESSES}}{\text{SEC}} = \frac{m}{t_c}\left(1-\left(1-\frac{1}{m}\right)^P\right)$$

$$= \frac{m}{t_c}\left(1-1/e\right) \quad \text{for } m=\infty \text{ and } P=m.$$

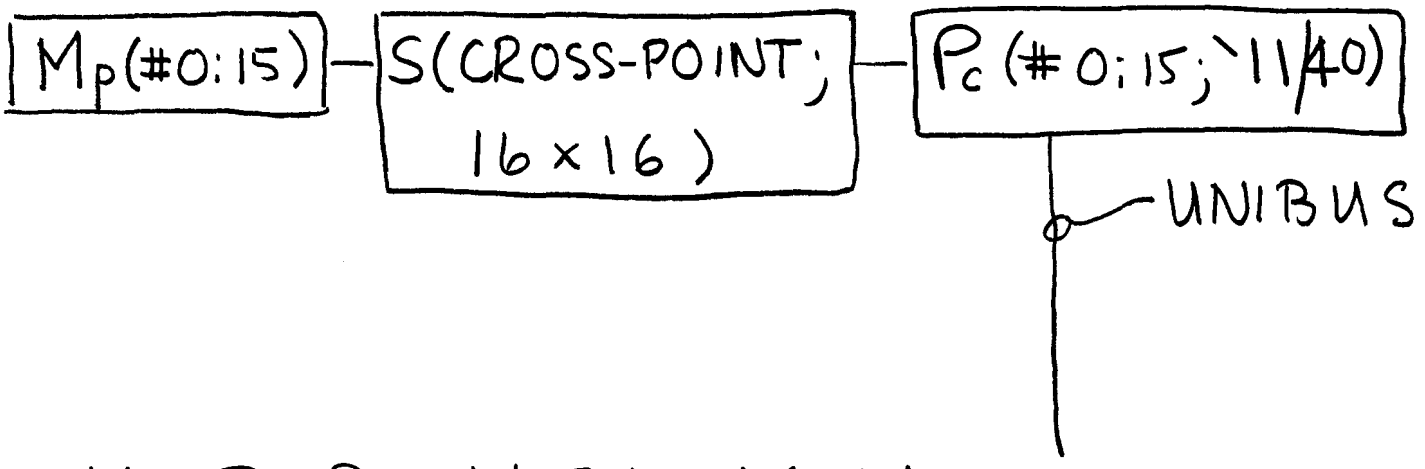
$$= \frac{m}{t_c} \times .67.$$



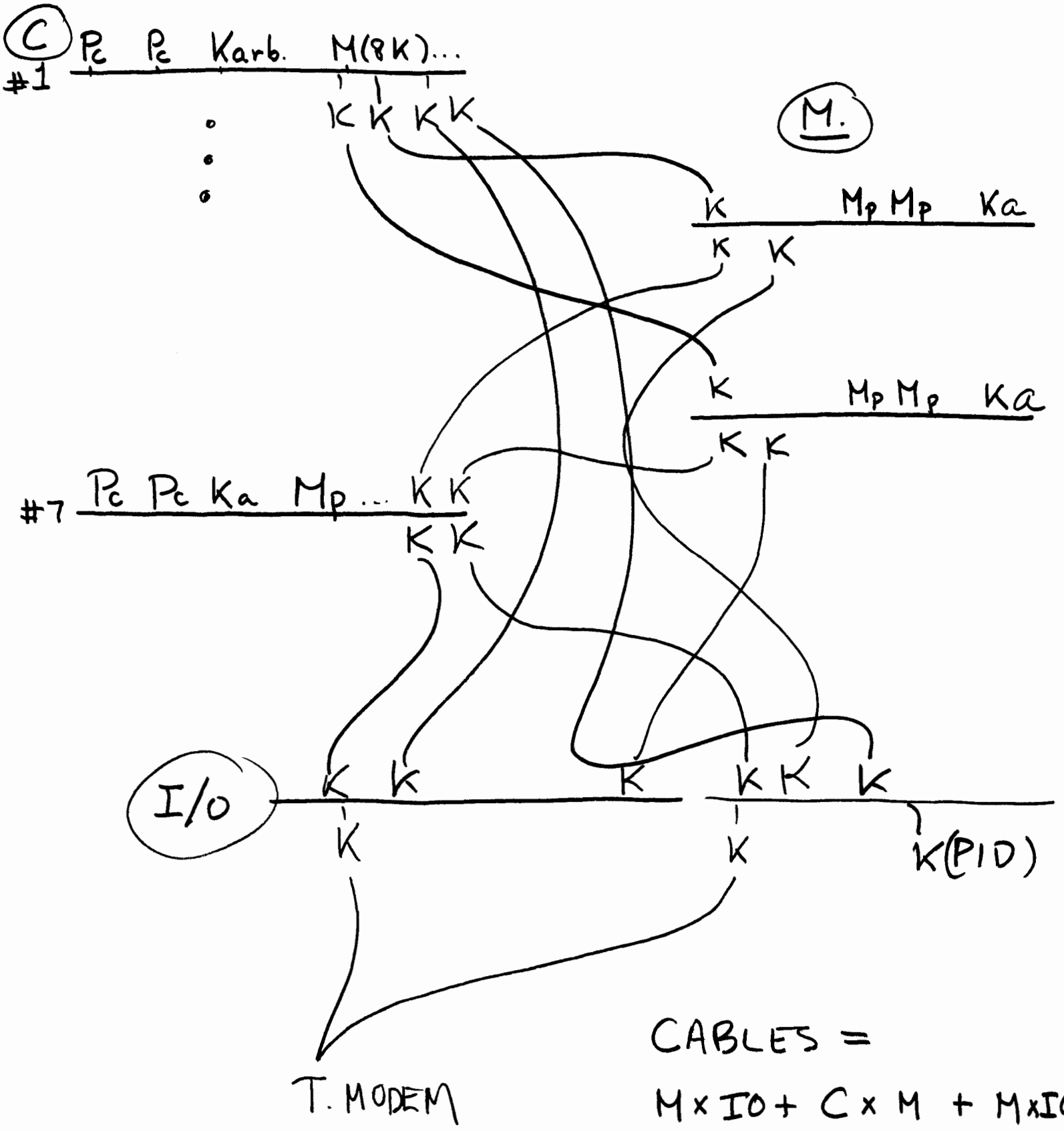
MULTI- Pc USING 1 BUS



MULTI- SPECIAL Pc, 1 BUS



MULTI-Pc WITH 16 Mp's.



CABLES =

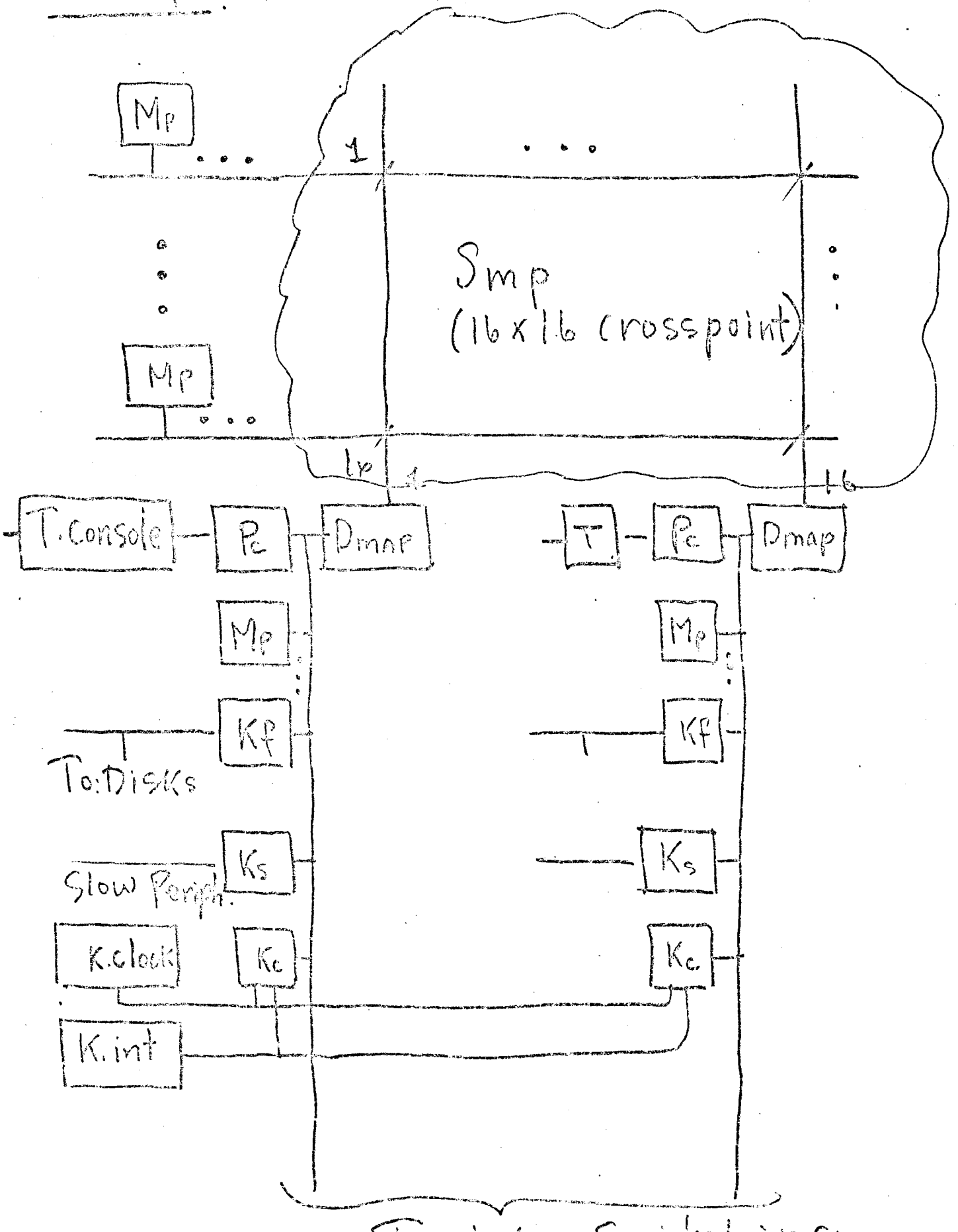
M x IO + C x M + M x IO

2 x 2 + 7 x 2 + 2 x 2

= 22

PLURIBUS SYSTEM. (BBN)

C.mmp


Mp
Mp
1
16
Smp
(16x16 crosspoint)
T.Console
Pc
Dmap
T
Pc
Dmap
Mp
Mp
Kf
Kf
To:Disks
Ks
Ks
Slow Perph.
K.clock
Kc
Kc
K.int
To i/o Switching.

DEFINITIONS

N-Computer Networks - Computers loosely coupled via Comm. L's.

mC Computer Modules - Tightly coupled C's... possibly sharing M_p.

mP - Multi-procesor Computer - A number of processors sharing a common, M_p.

STRUCTURES

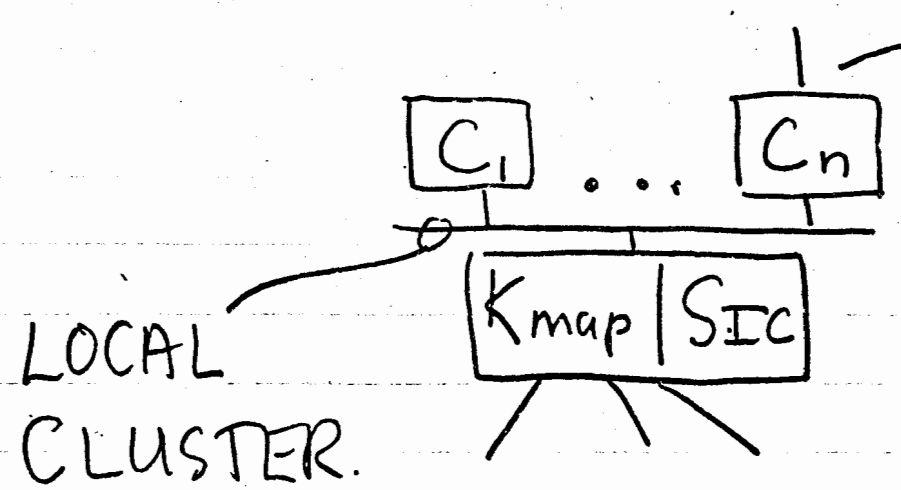
1. MULTI-PROCESSOR - mP
2. COMPUTER MODULES - Cm
3. NETWORKS.

PROBLEM / OBJECTIVE FCN

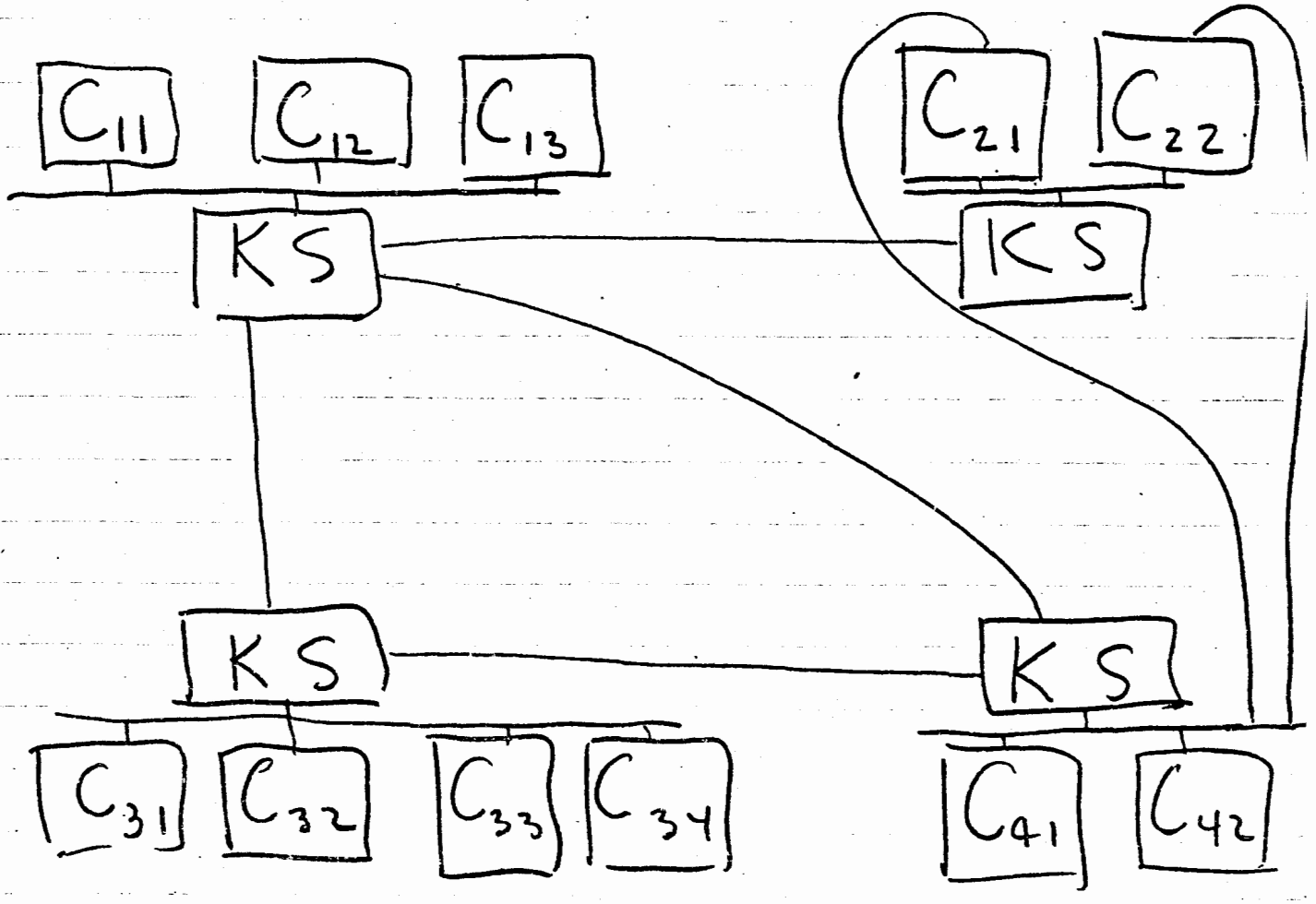
1. LOCATION OF "WORK"; PEOPLE
2. REQ. FOR P_c, M_p, M_s, AVAILABILITY.

TRADEOFFS

	+	− (and Cost)
mP	LESS M_p, L, MORE P_c AVAIL; CONFG. TO MAINTAIN	SMp; INTEGRAL SYSTEM.
Cm	FUNCTIONAL ISOLATION	M_p, Links, P_c (ABILITY TO MATCH/MOVE WORK)
N	LESS FCN. ISOLATE. COMM. LINKS.	SAME AS Cm ~~(LINKS MORE)~~

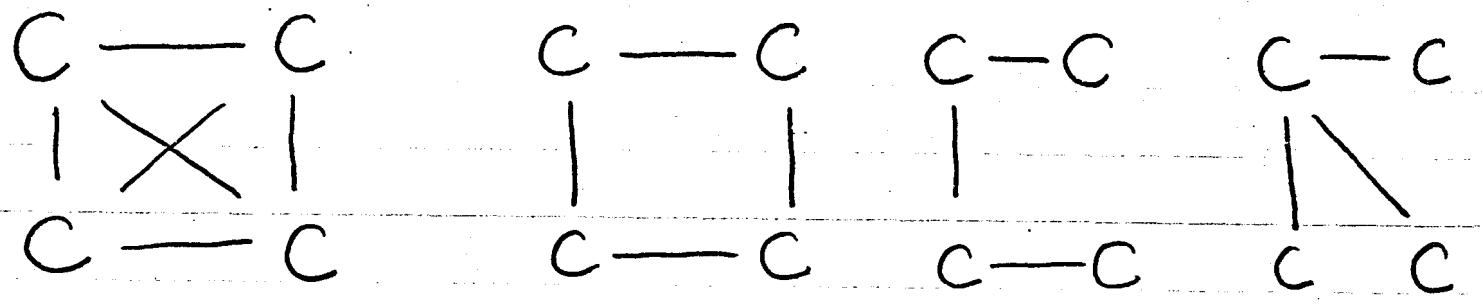


mC CLUSTER STRUCTURE
(Computer Module).



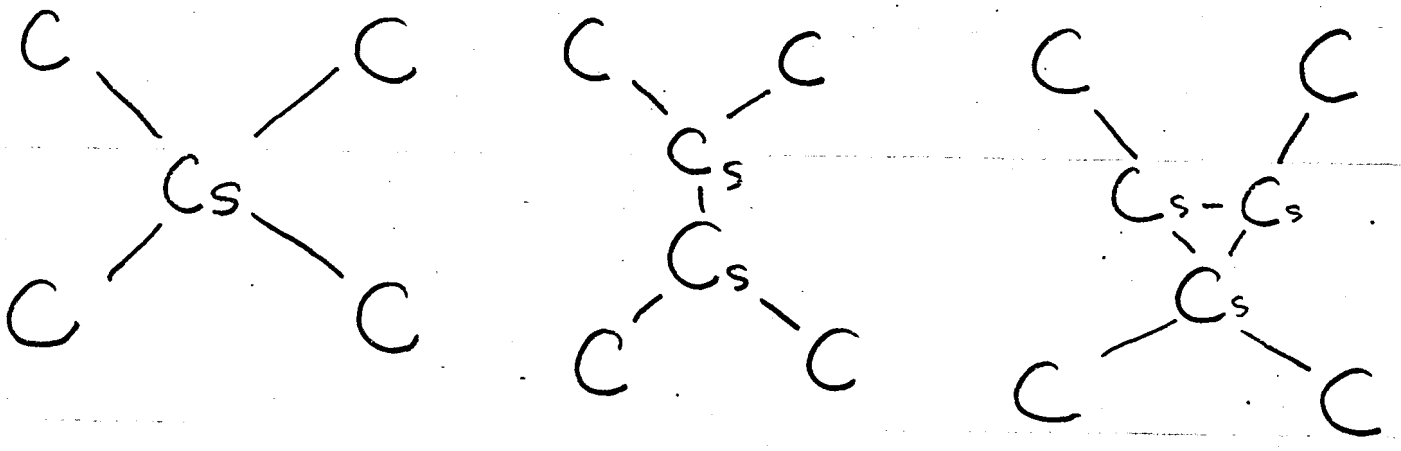
mC Problem Structure

DIRECT INTERCONNECT

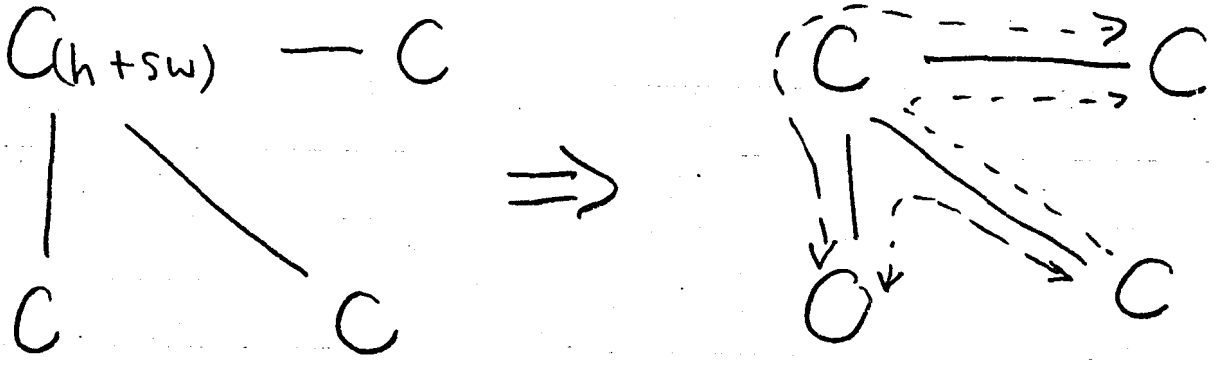


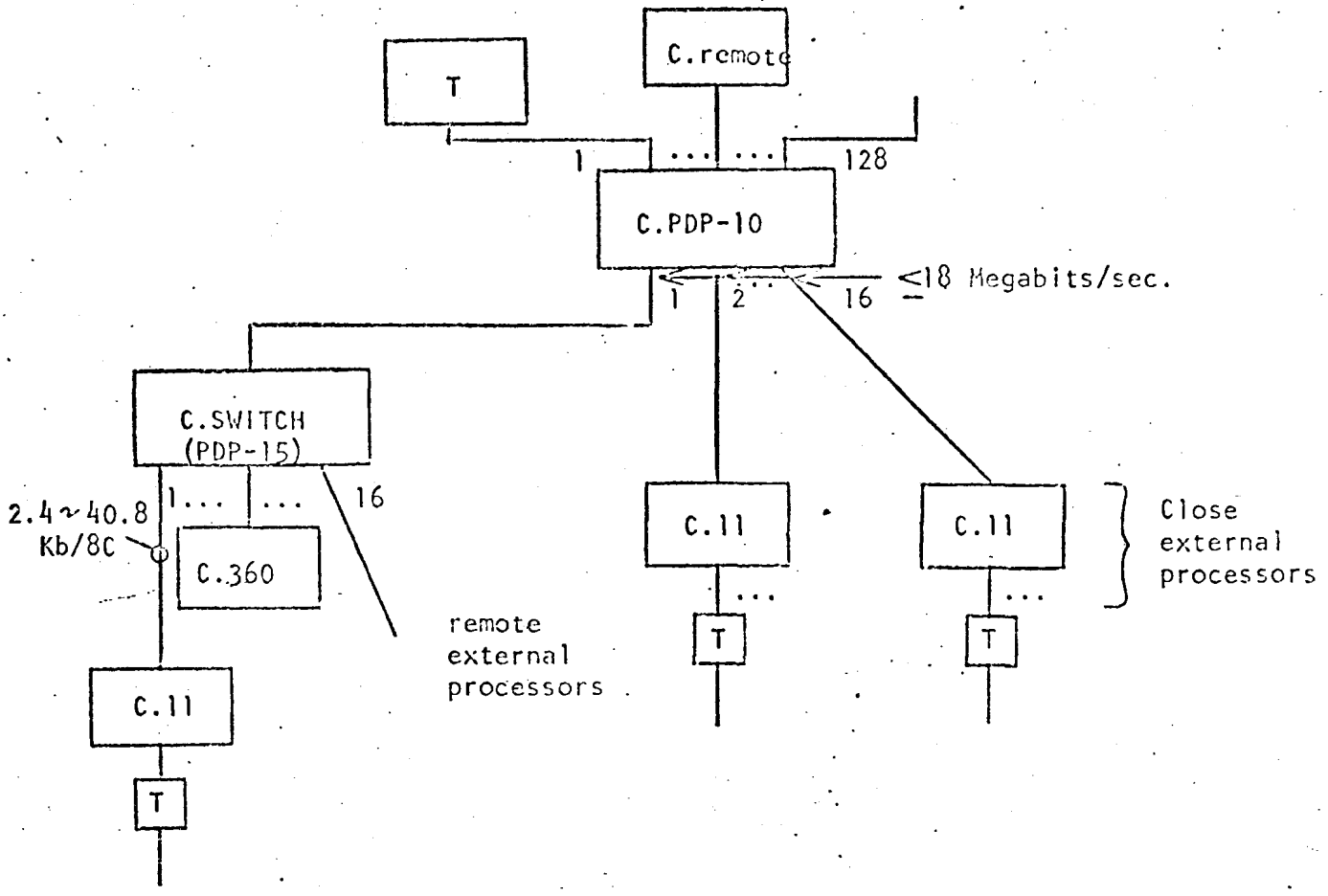
EXHAUSTIVE RING CHAIN STAR

S/F NETS W/ Csw's.



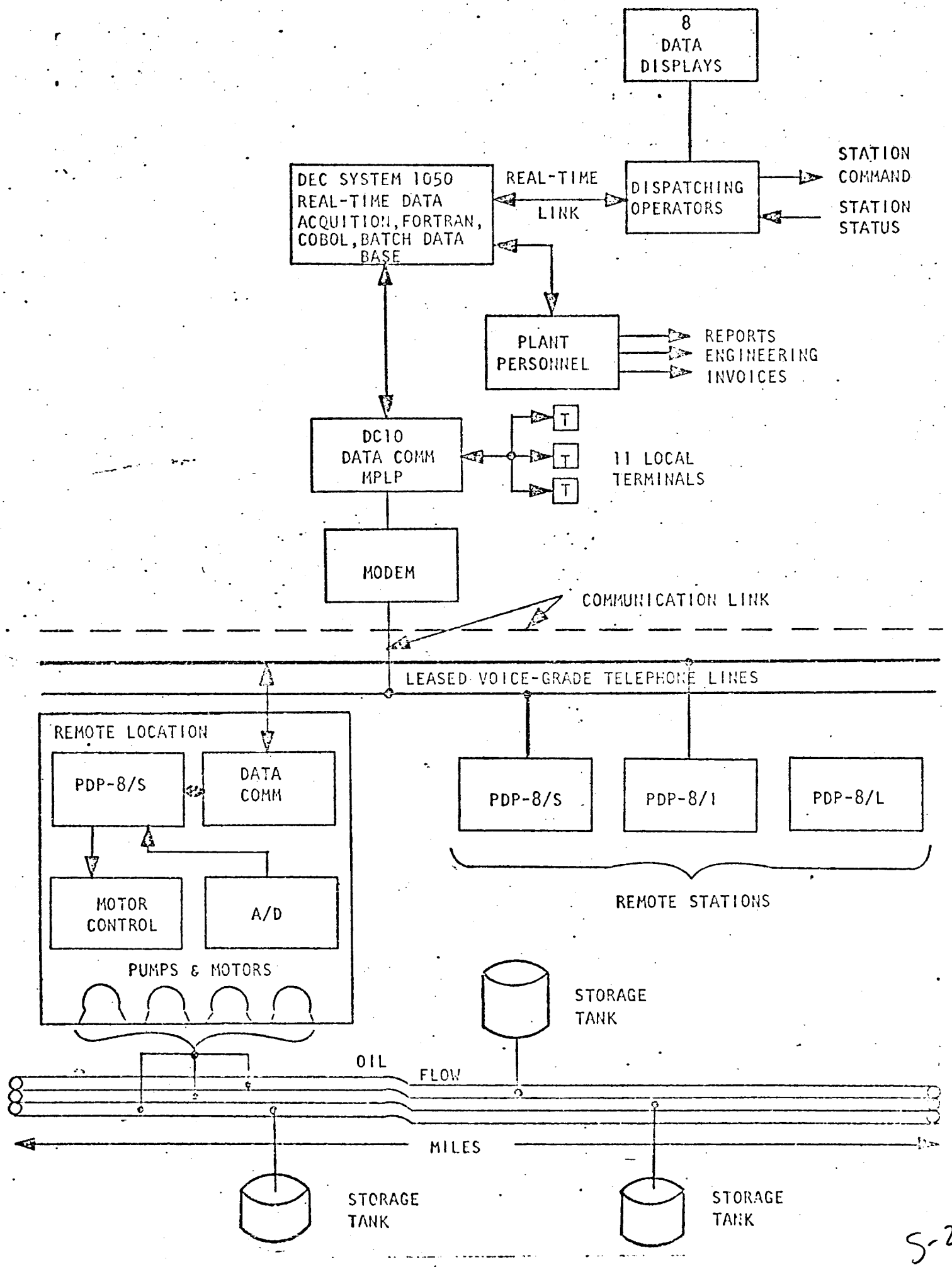
Hybrid.

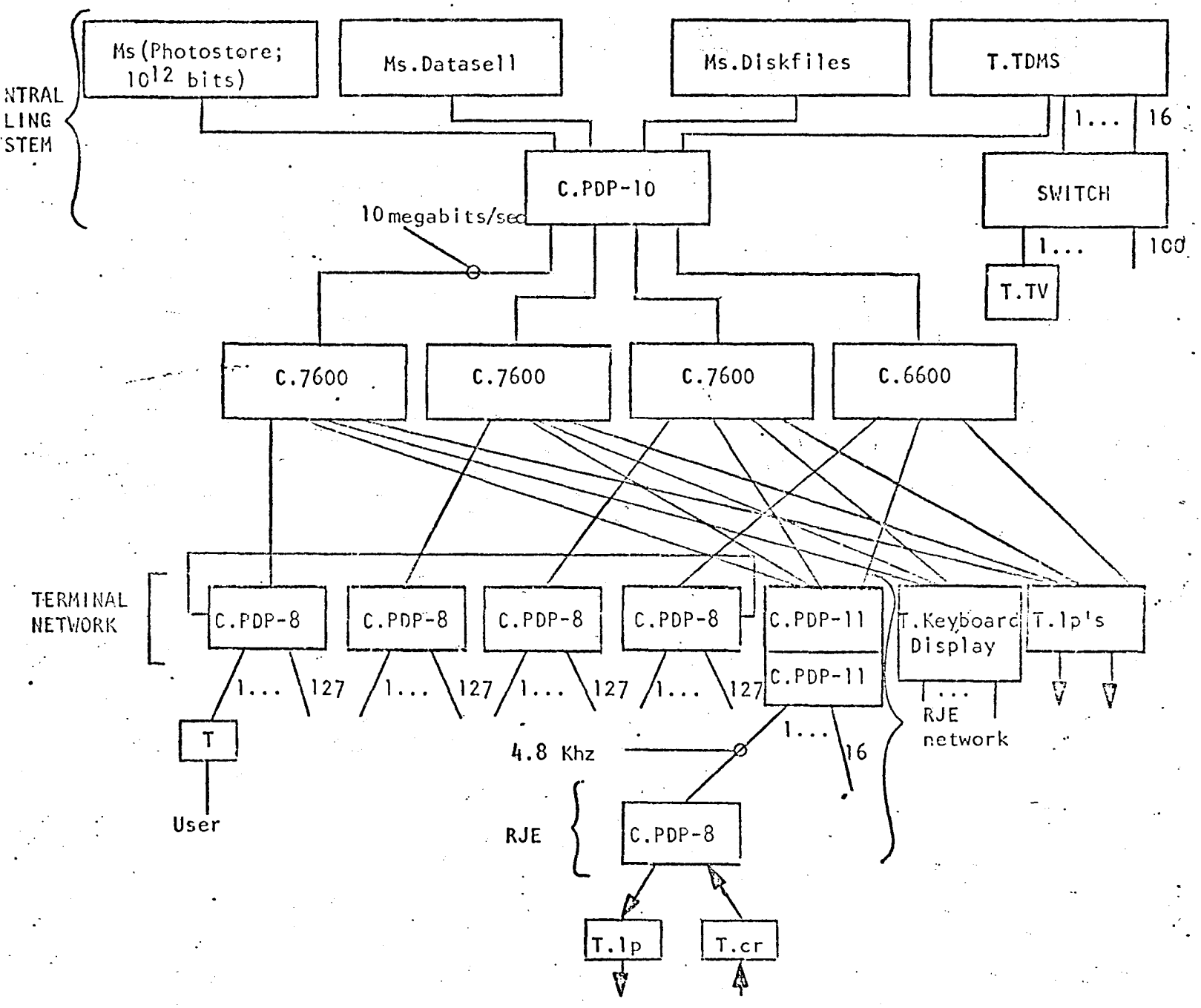




C.PDP-10	Single or dual processor DECsystem 10 with TOPS 10 monitor.
C.11	PDP-11 Model 40 or 45 with RSX-11D monitor
C.remote	Any computer connected via standard asynchronous communications Link at 110, 300, 1200 or 2000 b/s.
C.360	Appears to a 360 or 370 as a HASP 2780 RJE Terminal

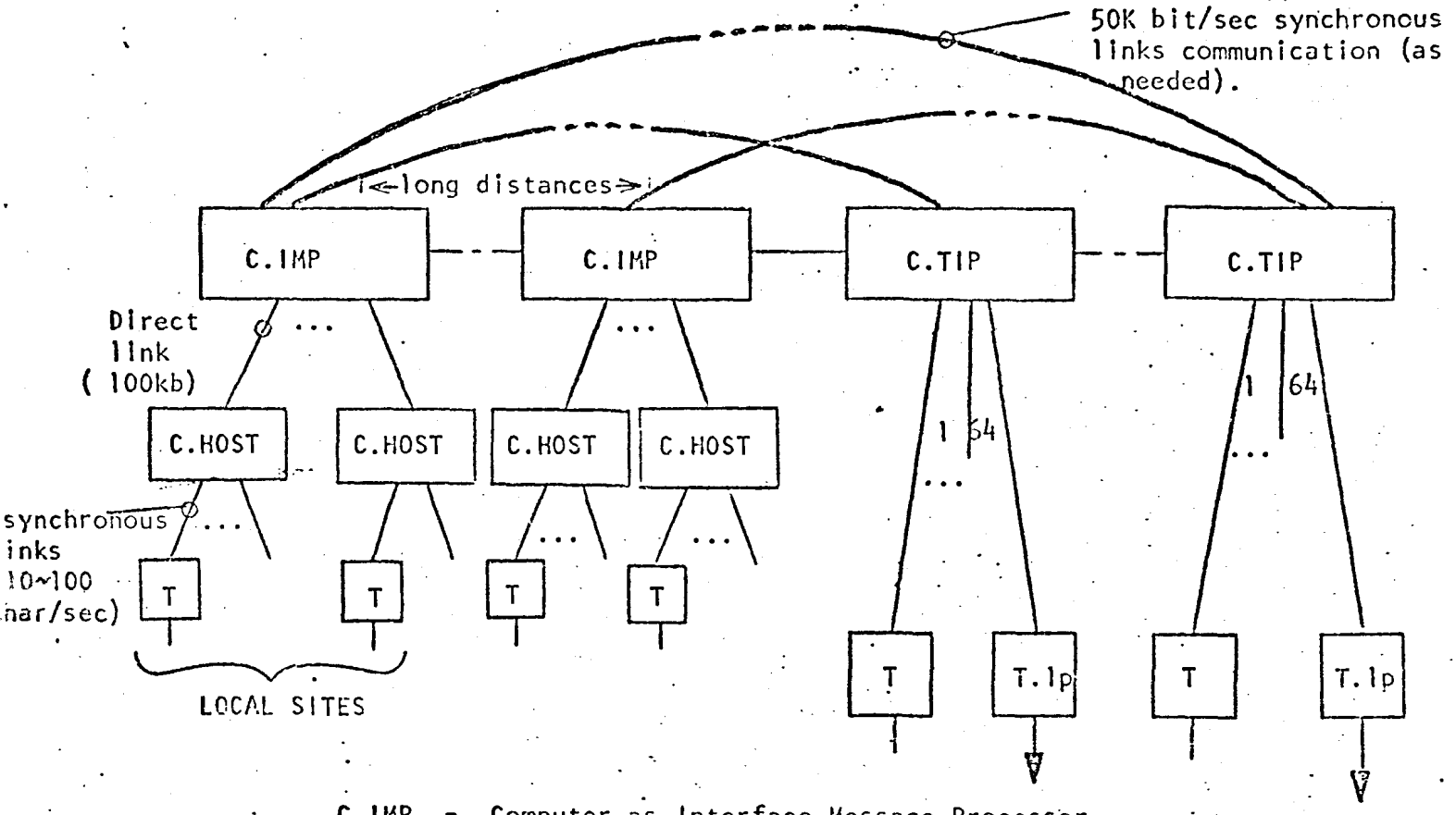
FIGURE 2. DEC LABORATORY INTERCONNECTION PROGRAMMING SYSTEM


8
DATA
DISPLAYS
DEC SYSTEM 1050
REAL-TIME DATA
ACQUITION, FORTRAN,
COBOL, BATCH DATA
BASE
REAL-TIME
LINK
DISPATCHING
OPERATORS
STATION
COMMAND
STATION
STATUS
PLANT
PERSONNEL
REPORTS
ENGINEERING
INVOICES
DC10
DATA COMM
MPLP
T
T
T
11 LOCAL
TERMINALS
MODEM
COMMUNICATION LINK
LEASED VOICE-GRADE TELEPHONE LINES
REMOTE LOCATION
PDP-8/S
DATA
COMM
MOTOR
CONTROL
A/D
PUMPS & MOTORS
PDP-8/S
PDP-8/I
PDP-8/L
REMOTE STATIONS
STORAGE
TANK
OIL
FLOW
MILES
STORAGE
TANK
STORAGE
TANK



T - Teletype; T.lp - line printer; T.cr - card reader; T.tv - television display
T.TDMS - Television Display Monitor System

FIGURE 4. STRUCTURE OF LLL OCTOPUS NETWORK

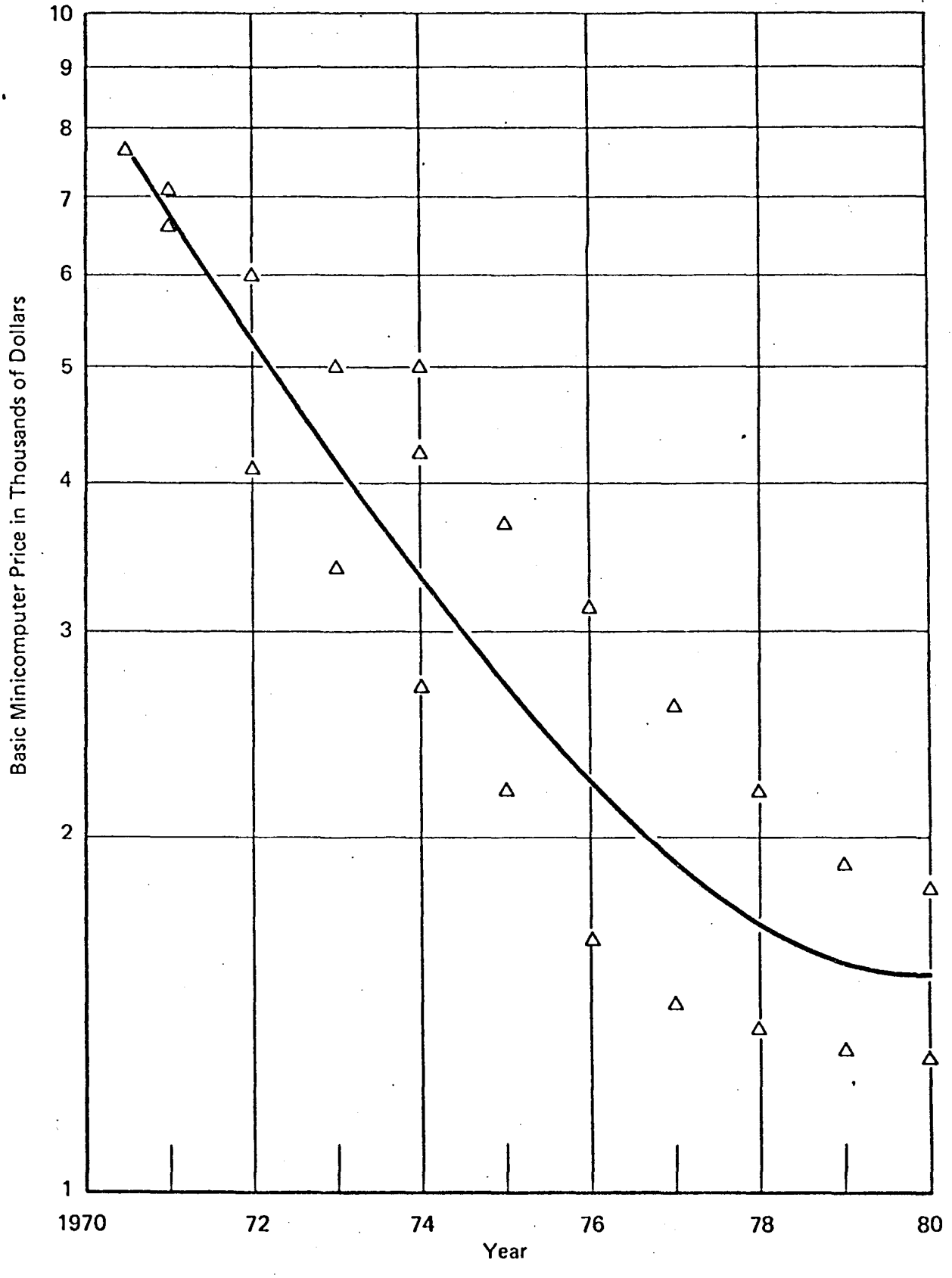


C.IMP - Computer as Interface Message Processor (stores and forwards messages).
C.TIP - Computer as Terminal Interface Processor (moves and forwards messages).
C.HOST Computer - Host (e.g. PDP-10, 360/91).
T - Terminal to user (e.g. Teletype, Execuport).
T.lp - Terminal - Line printer.

FIGURE 5. INTERCONNECTION STRUCTURE OF ARPA NETWORK

Figure 3-2

CLASS II AND III MINICOMPUTER PRICE TRENDS



DataQuest

Figure 3-4

TYPICAL MINICOMPUTER PRODUCT LIFE CYCLE

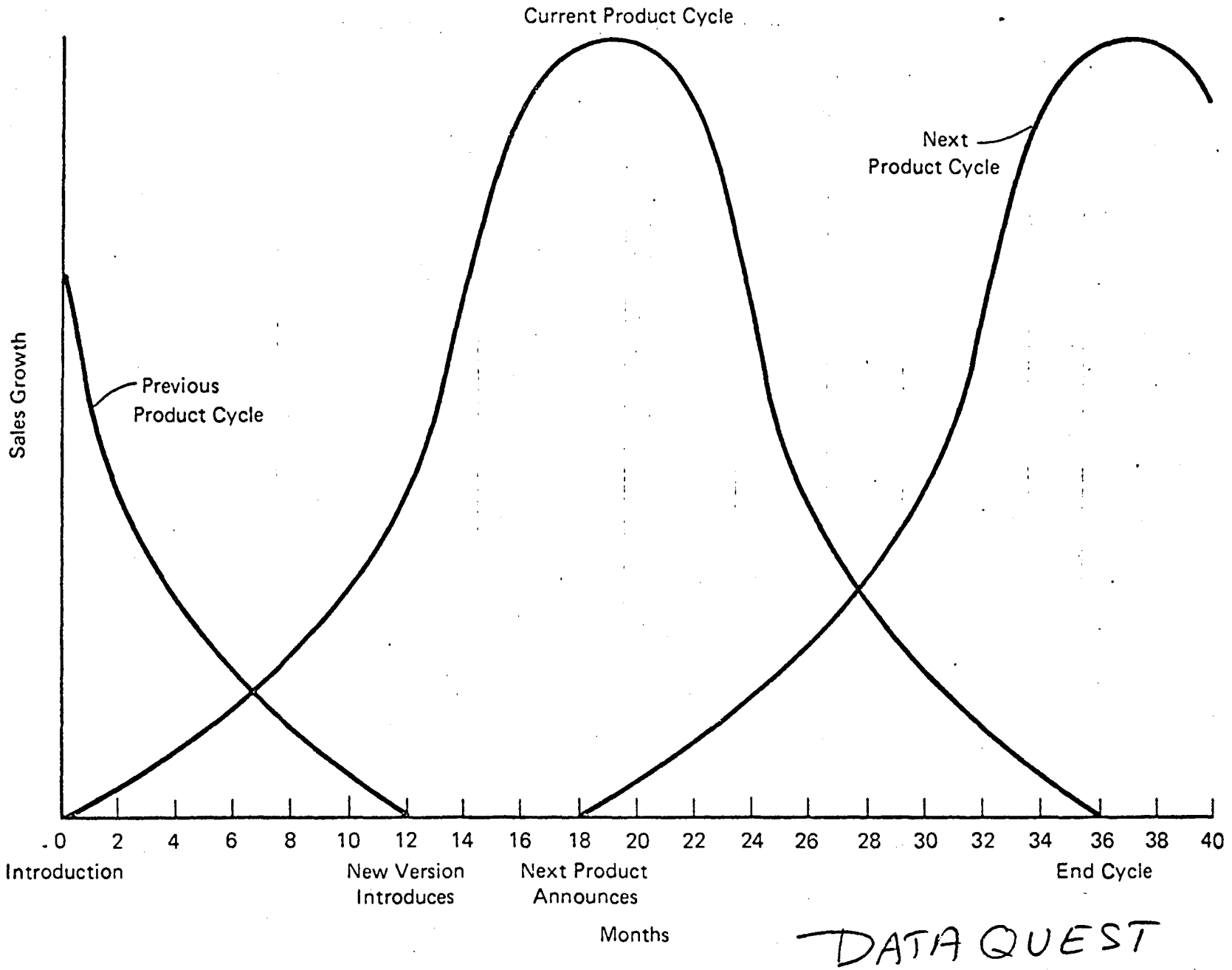
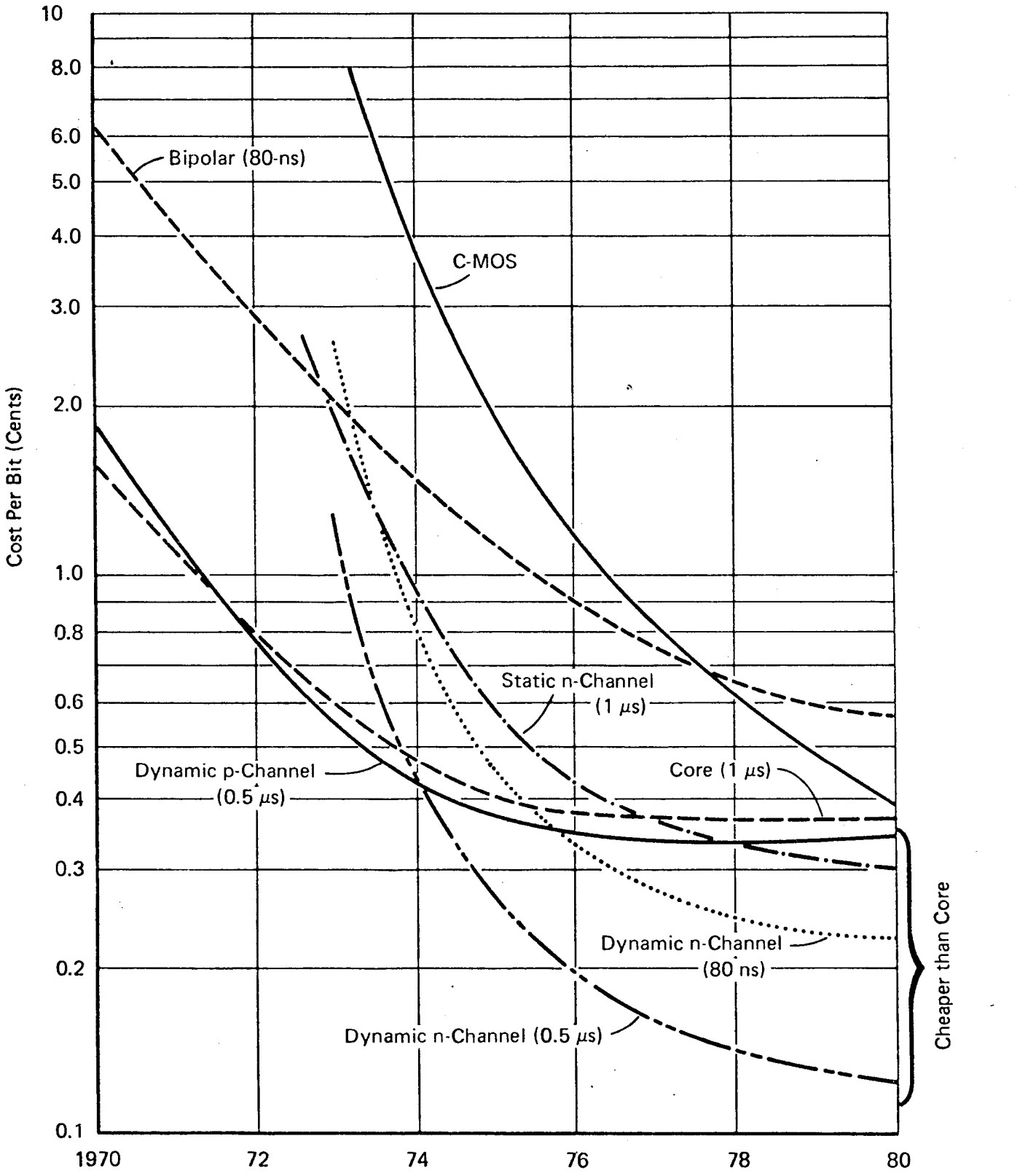


Figure 6-5

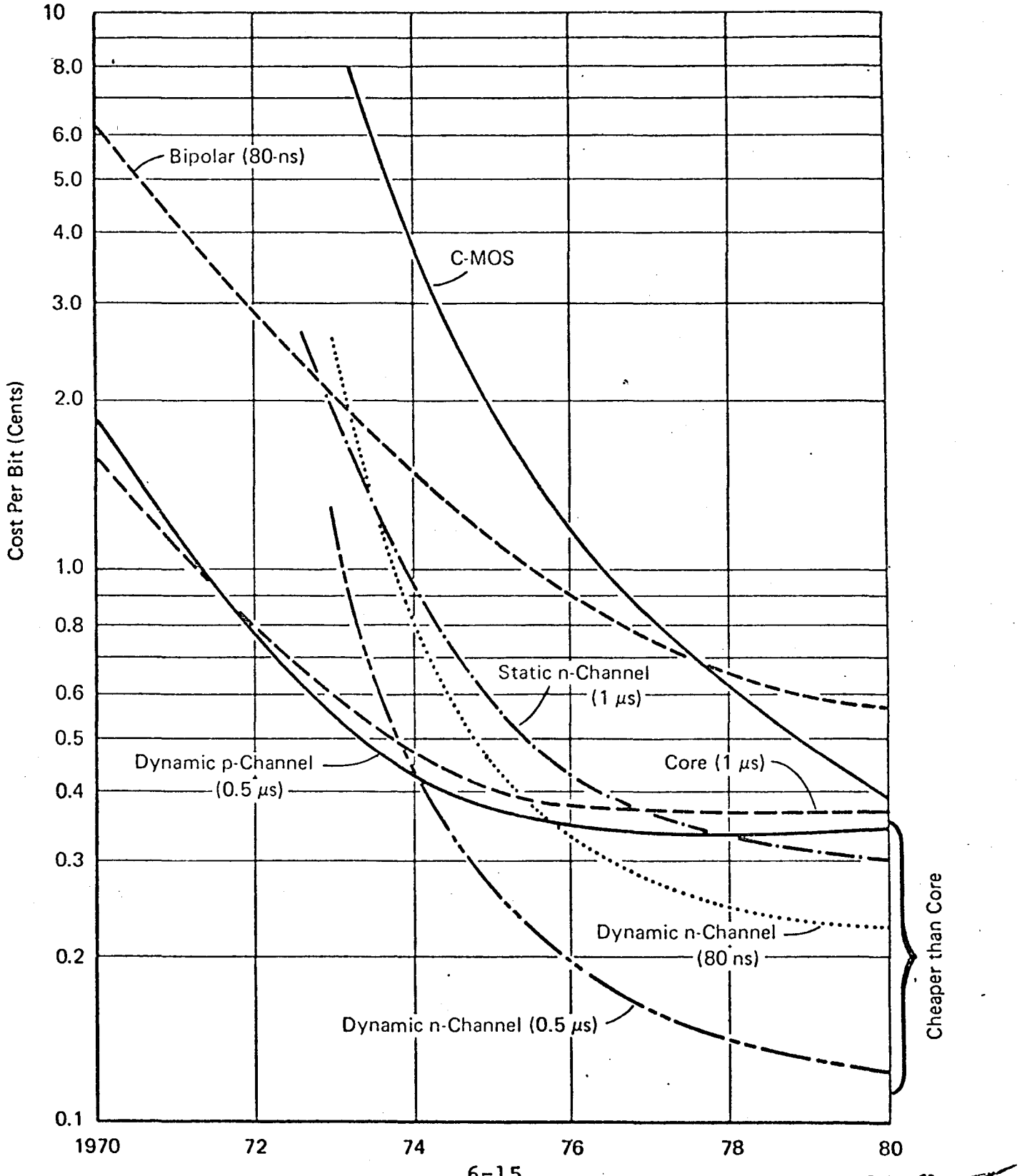
MEMORY SYSTEM COST PER BIT
FOR VARIOUS TECHNOLOGIES



DATA QUEST

Figure 6-5

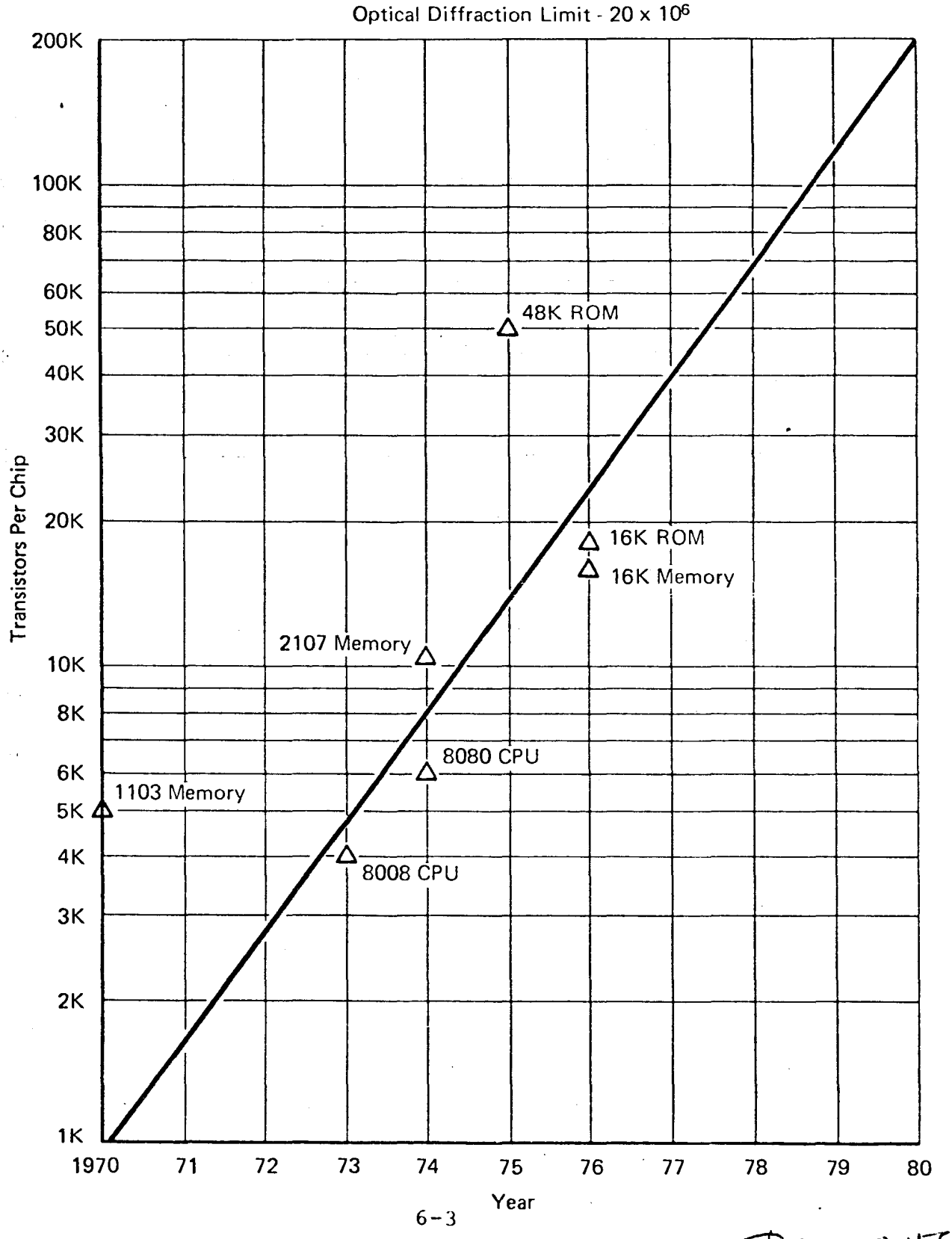
MEMORY SYSTEM COST PER BIT
FOR VARIOUS TECHNOLOGIES



DATA QUEST

Figure 6-1

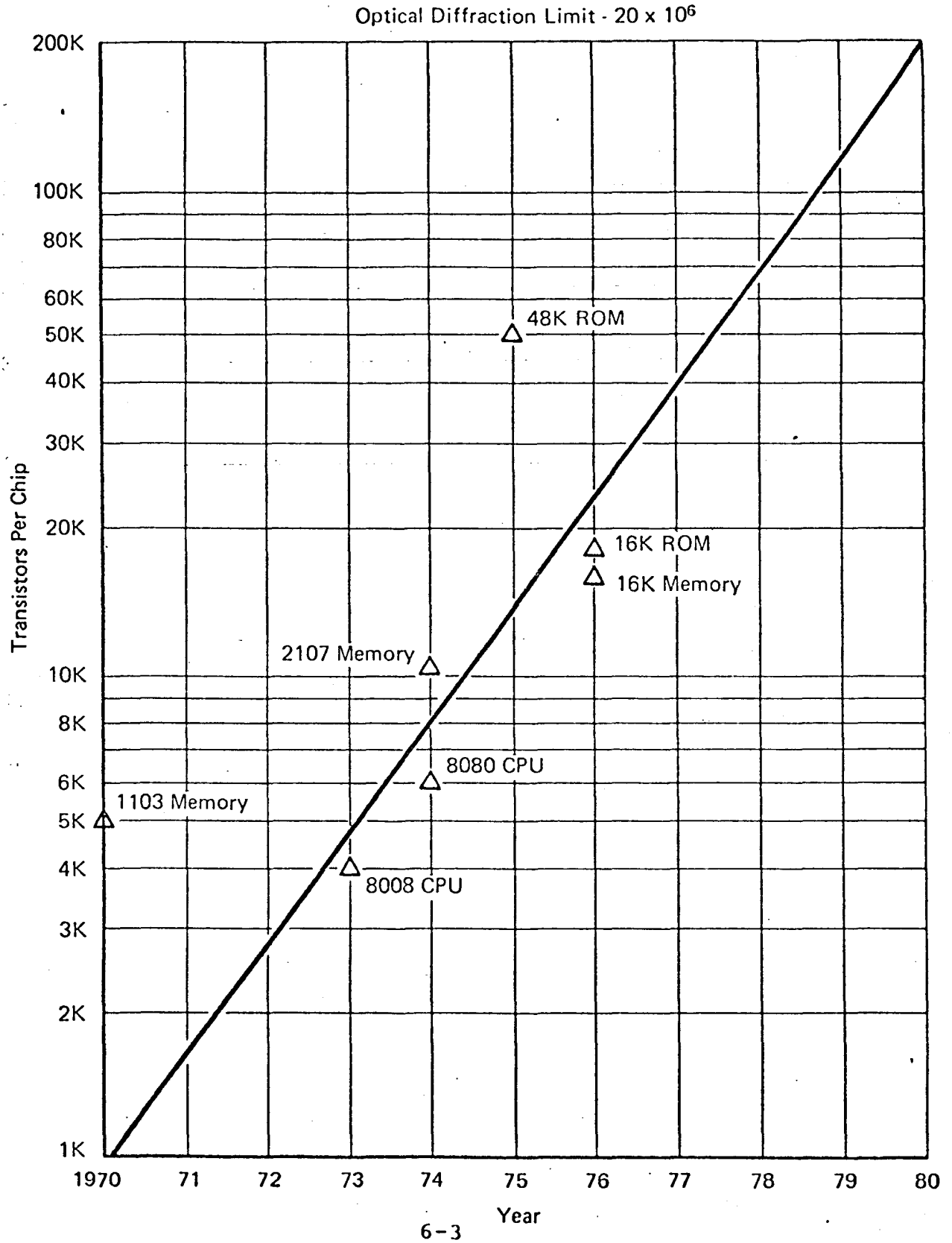
TRENDS IN COMPONENT COMPLEXITY



DATAQUEST

Figure 6-1

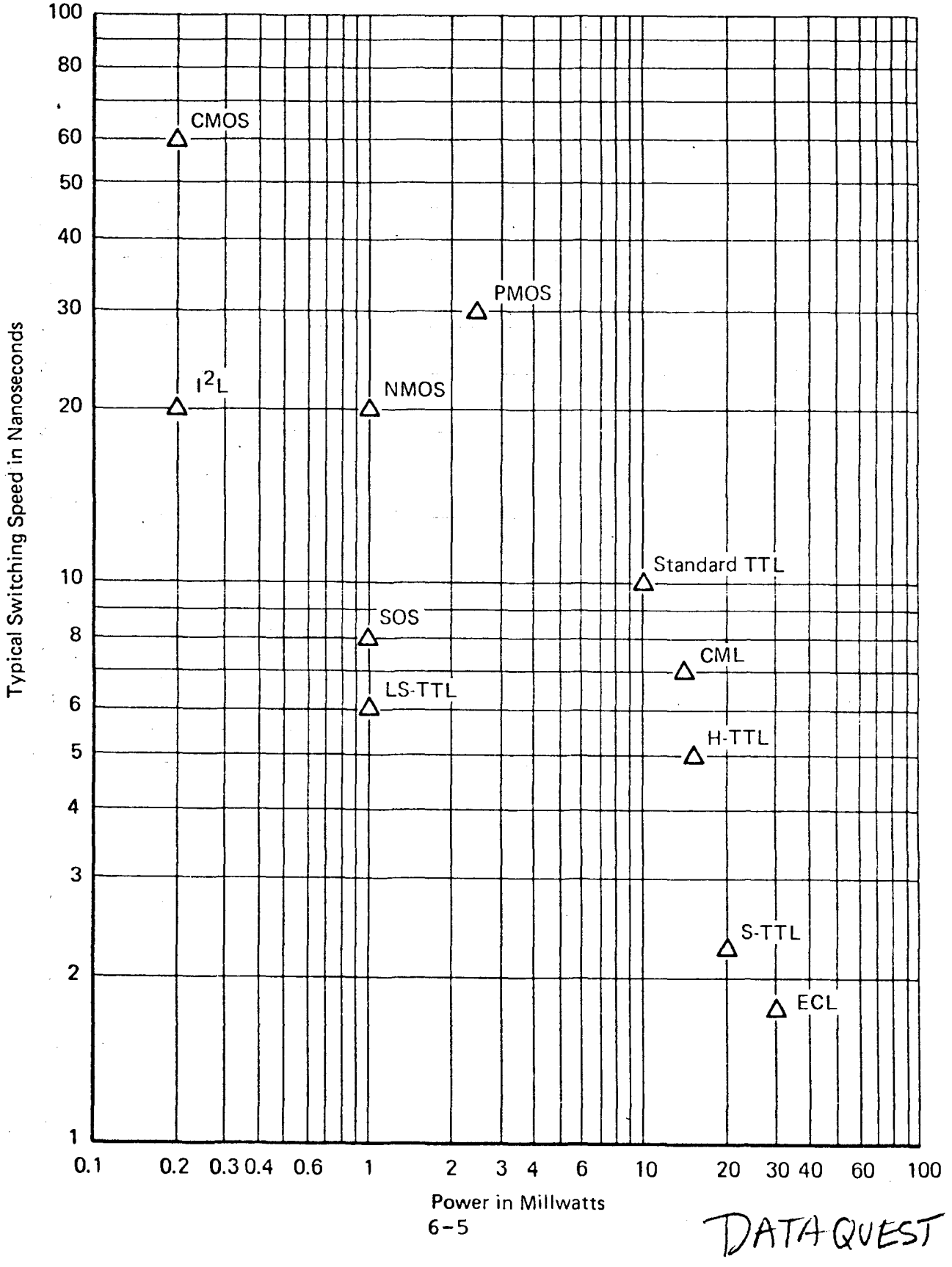
TRENDS IN COMPONENT COMPLEXITY



DATAQUEST

Figure 6-2

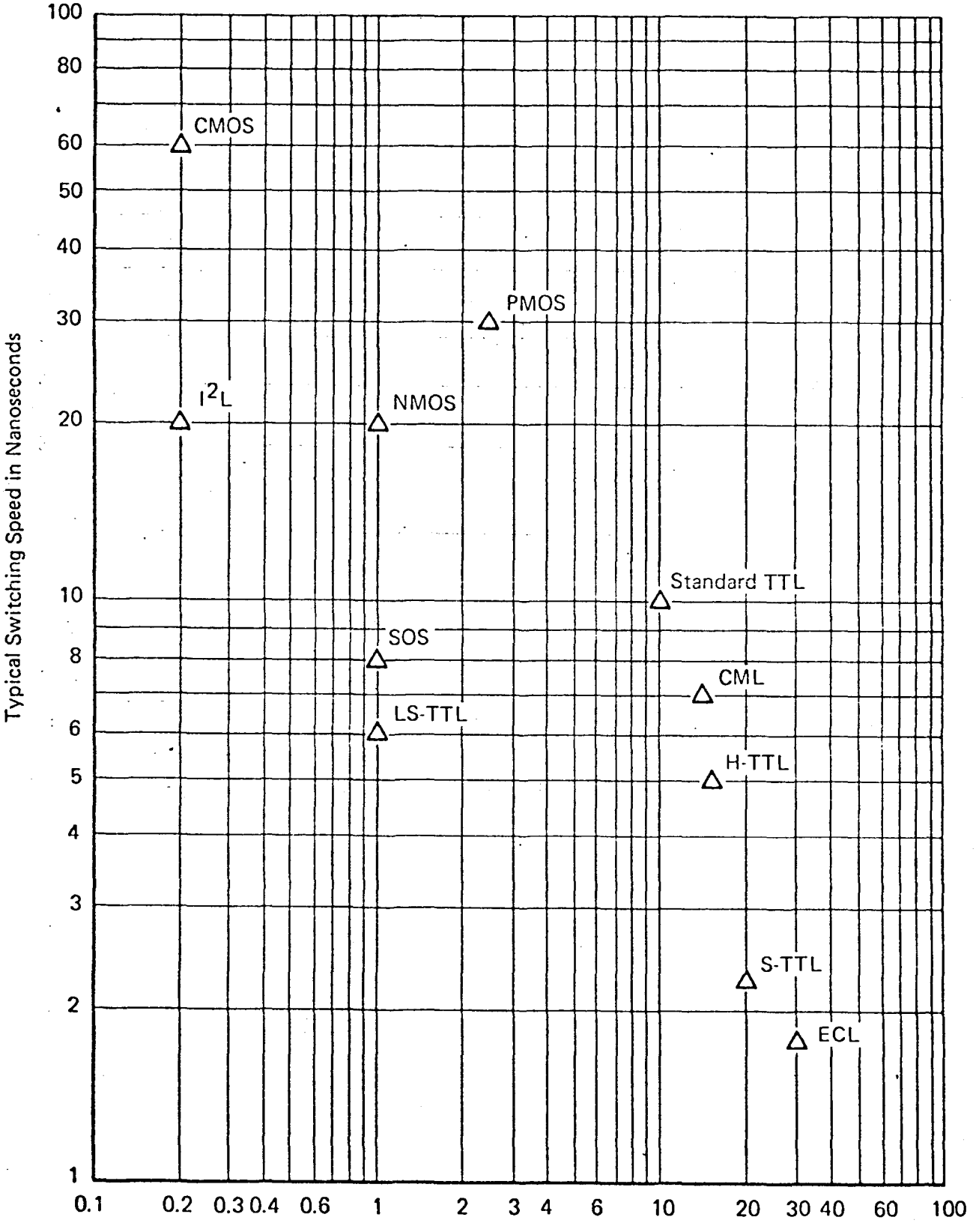
SPEED-POWER PERFORMANCE BY TECHNOLOGY



DATA QUEST

Figure 6-2

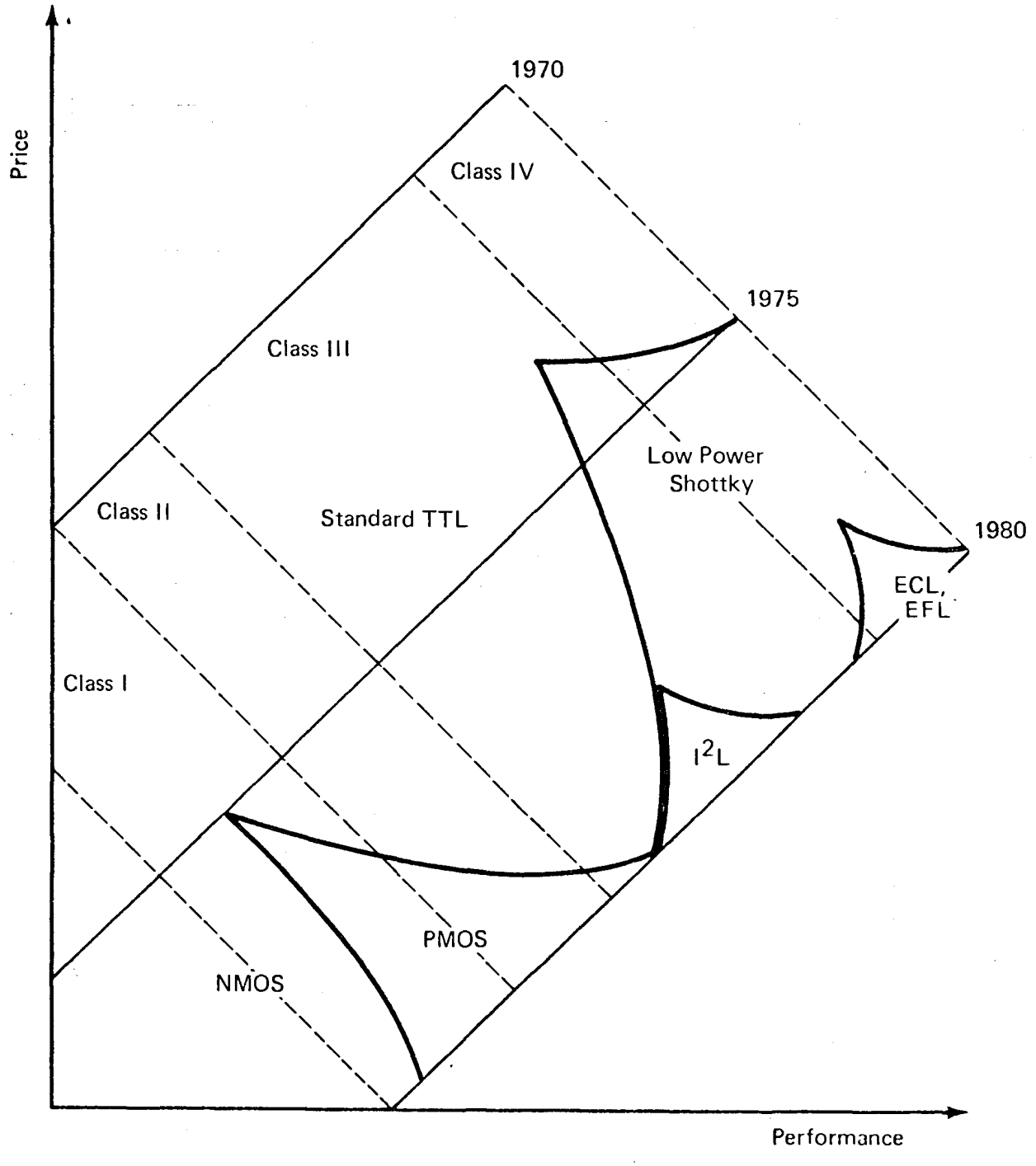
SPEED-POWER PERFORMANCE BY TECHNOLOGY



DATA QUEST

Figure 6-3

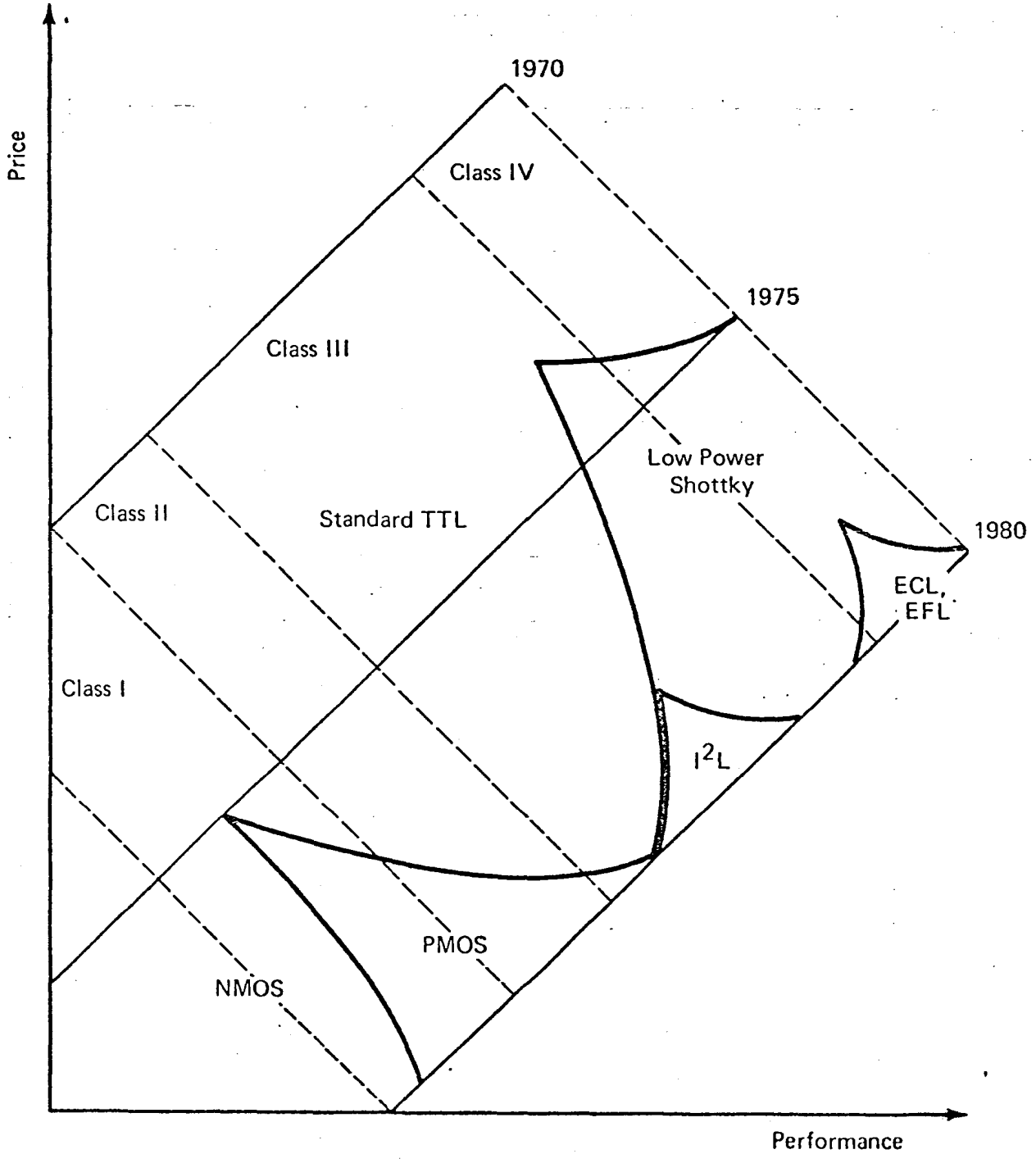
MINICOMPUTER LOGIC FAMILIES
IMPLEMENTATION PROJECTIONS



DATAQUEST

Figure 6-3

MINICOMPUTER LOGIC FAMILIES
IMPLEMENTATION PROJECTIONS



DATAQUEST

Figure 3-2

CLASS II AND III MINICOMPUTER PRICE TRENDS

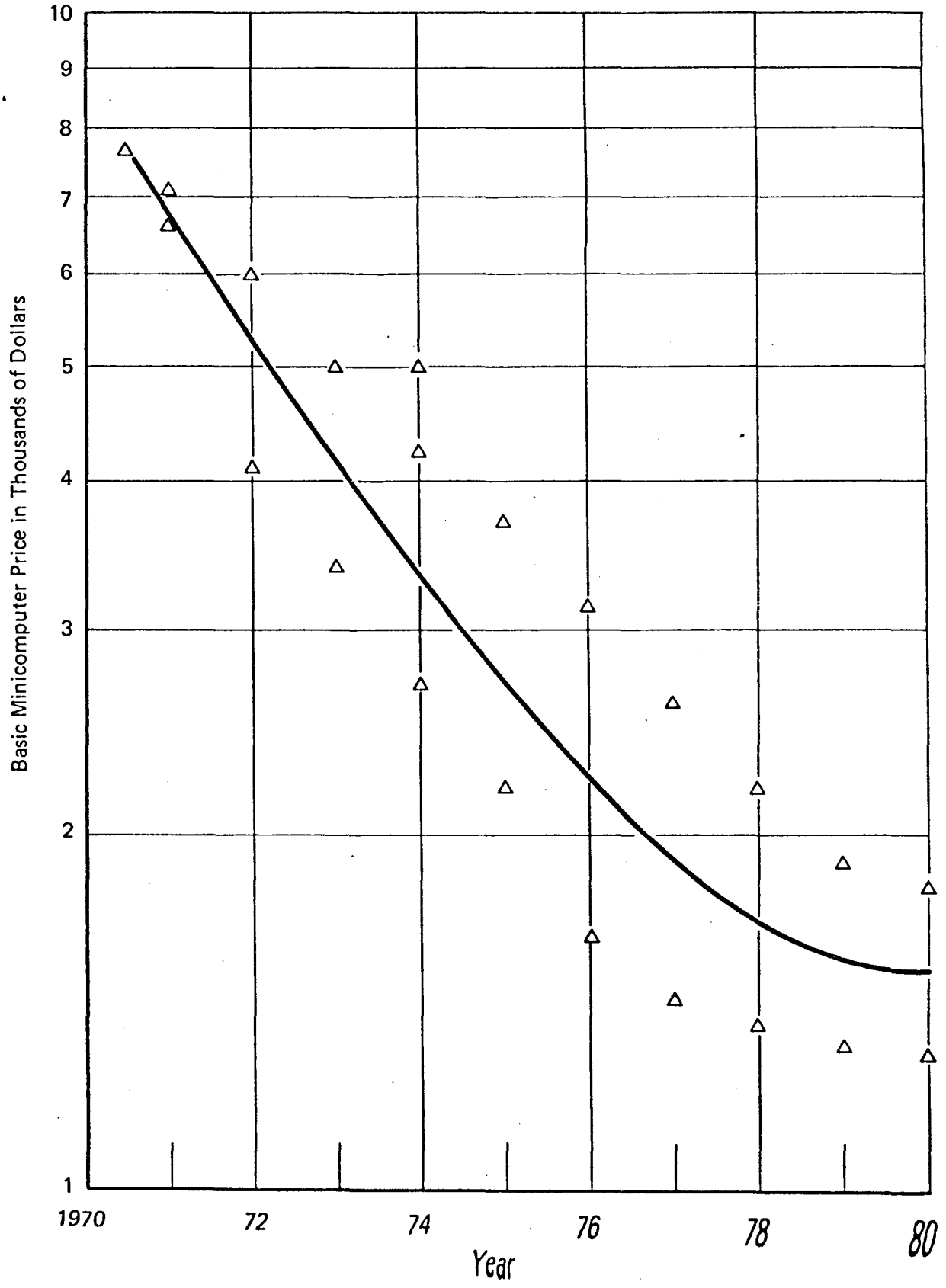
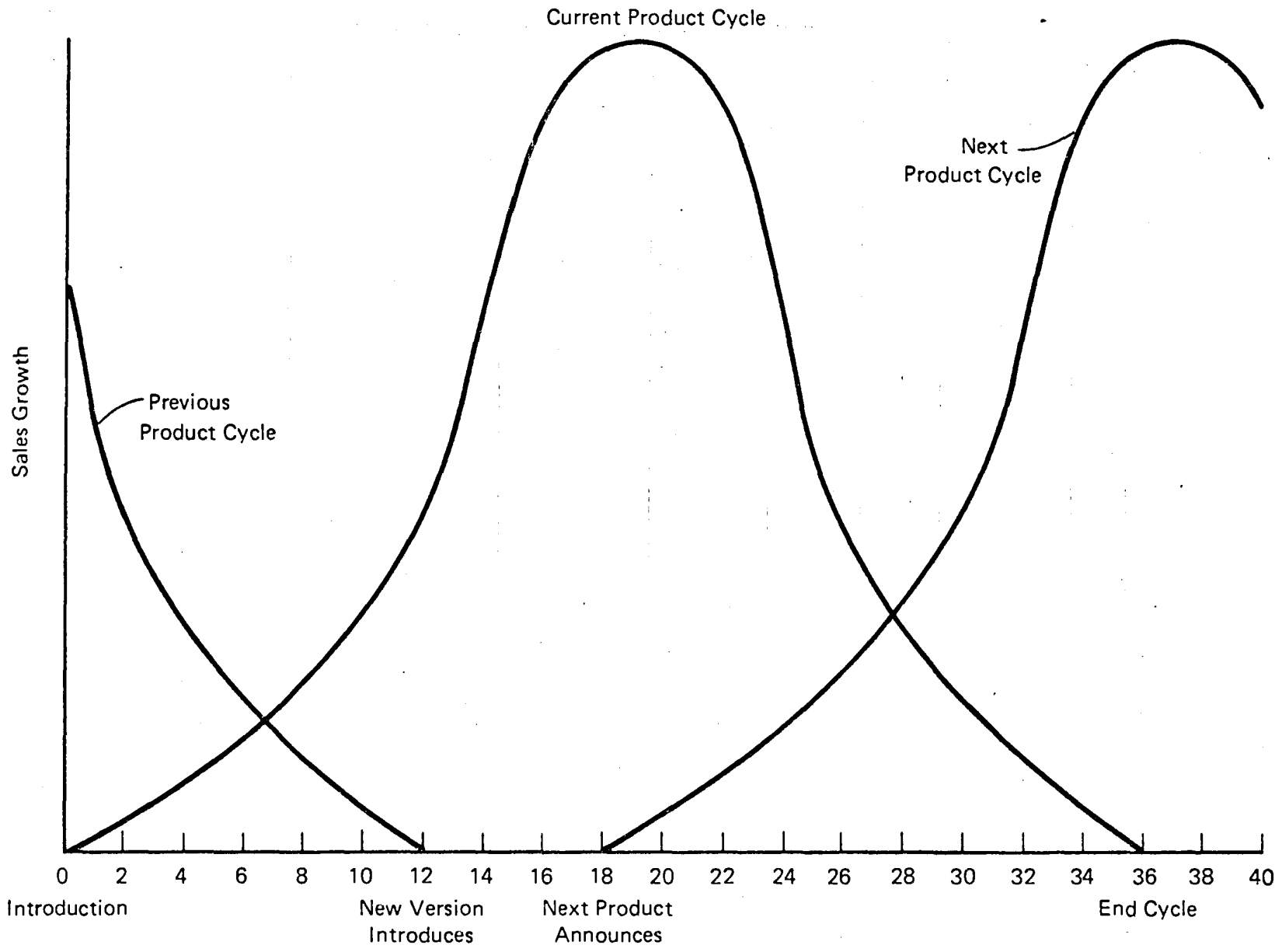


Figure 3-4

TYPICAL MINICOMPUTER PRODUCT LIFE CYCLE



DATA QUEST

DISK TECHNOLOGY 1975

	PRICE (K$)	SIZE (MB)	C/B (¢/B)	ACCESS T.
FLEX.	3	2.5	.12	1 SEC.
1 PLAT.	6	30	.02	50 Ms.
3-5 "	12	160	.0075	↓
10 "	25	800	.003	20 Ms.

	MB/PLATTER	YRS (AT 41% YR)
1.	30	~~43~~
3	53	1+
5	80	0

YEARLY IMPROVEMENTS IN TECHNOLOGY (1975)

- SEMICONDUCTORS
  - DENSITY 2^{t-1962}
    = 60 ~ 80 %/yr (CONSERVATIVE)

- DISKS (62-74) - DENSITY = 41%/yr.
- CORE PRICE IMPROVE 30%/yr.
- TAPE (52-73) - 23%/yr DENSITY
  29%/yr. DATA-RT
- POWER, PACKAGING ~ 0
- MINIS - 31% IMPROVE IN PRICE (SINCE '60)
- TERMINALS - YES.

SMALL (I.E. MICROS/MINIS) VS. "LARGE"

- THERE ISN'T A FUNDAMENTAL DIFFERENCE IN MACHINE & SYSTEM CAPABILITY BETWEEN SMALL & LARGE COMPUTERS
→ EXCEPT PRICE.

→ THERE'S DIFFERENCES IN DEDICATEDNESS (USE) & BUNDLED-IN SERVICES (HELP).

WILL SMALL COMPUTERS EVOLVE:

→ ALONG TRADITIONAL LINES (>COMPLEX. ≈ CONST. PRICE)?
AND/OR
→ ALONG P-on-a-Chip (MUCH LOWER PRICE) #(≤ COMPLEXITY) IN AN INTERCONNECTED FASHION?

GB 3/76

A Course of Study in C. Hdw. Arch.

Computer — Dec. 75

✓2 - Intro & Meta-rep. (Levels, text, Languages,)

✓5 - Data Repr. (formats, Vectors, ...)

✓5 - Inst. + Addressng (what, name space, op's)

✓6 - Interpretation + Control (μ-prog)

8 - M - hierarchies (refs, Components, ...)

✓4 - Protection & Hdw. Aids to Supervisors

5 - P. Special (channels ... μP.

✓4 - mC, (mP, performance, Nets)

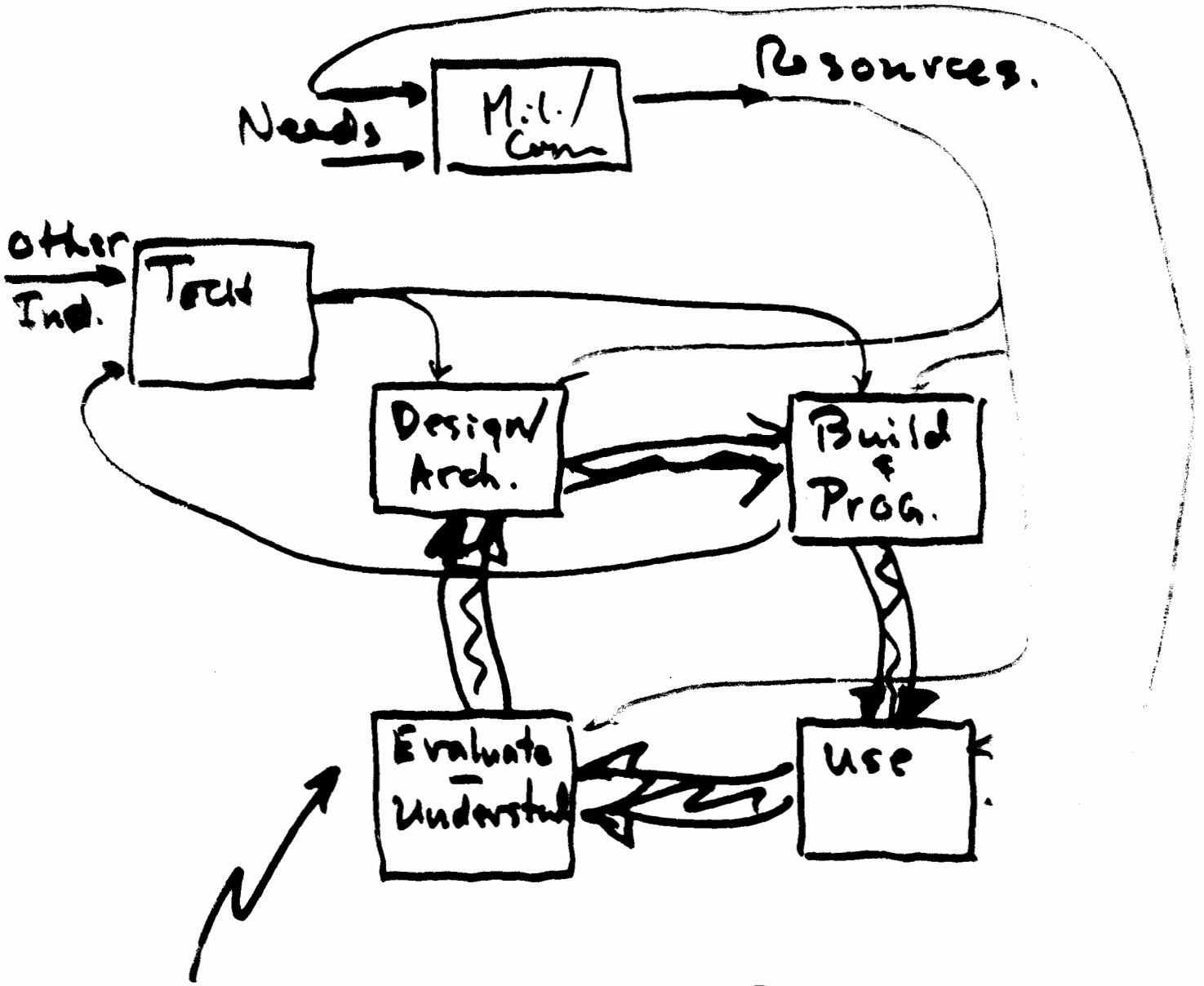
9 - Performance Evaluation

✓5 - Reliability

6 - Design Eval.

59

Computer Generations Model.



1 Cycle = 1 Generation ~ 5~10 years.

Technology + Structure + Need → Use.

SIXTH GENERATION

- WILL BEGIN IN ROUGHLY 6 YEARS

TECHNOLOGY

- TRULY COST AND HIGH PERFORMANCE HARDWARE
- INSTALLED LAN'S AND HIGH BANDWIDTH WAN'S
- VOICE AND PICTURES

NEED

- INFORMATION OVERLOAD, PRIVACY AND PRODUCTIVITY

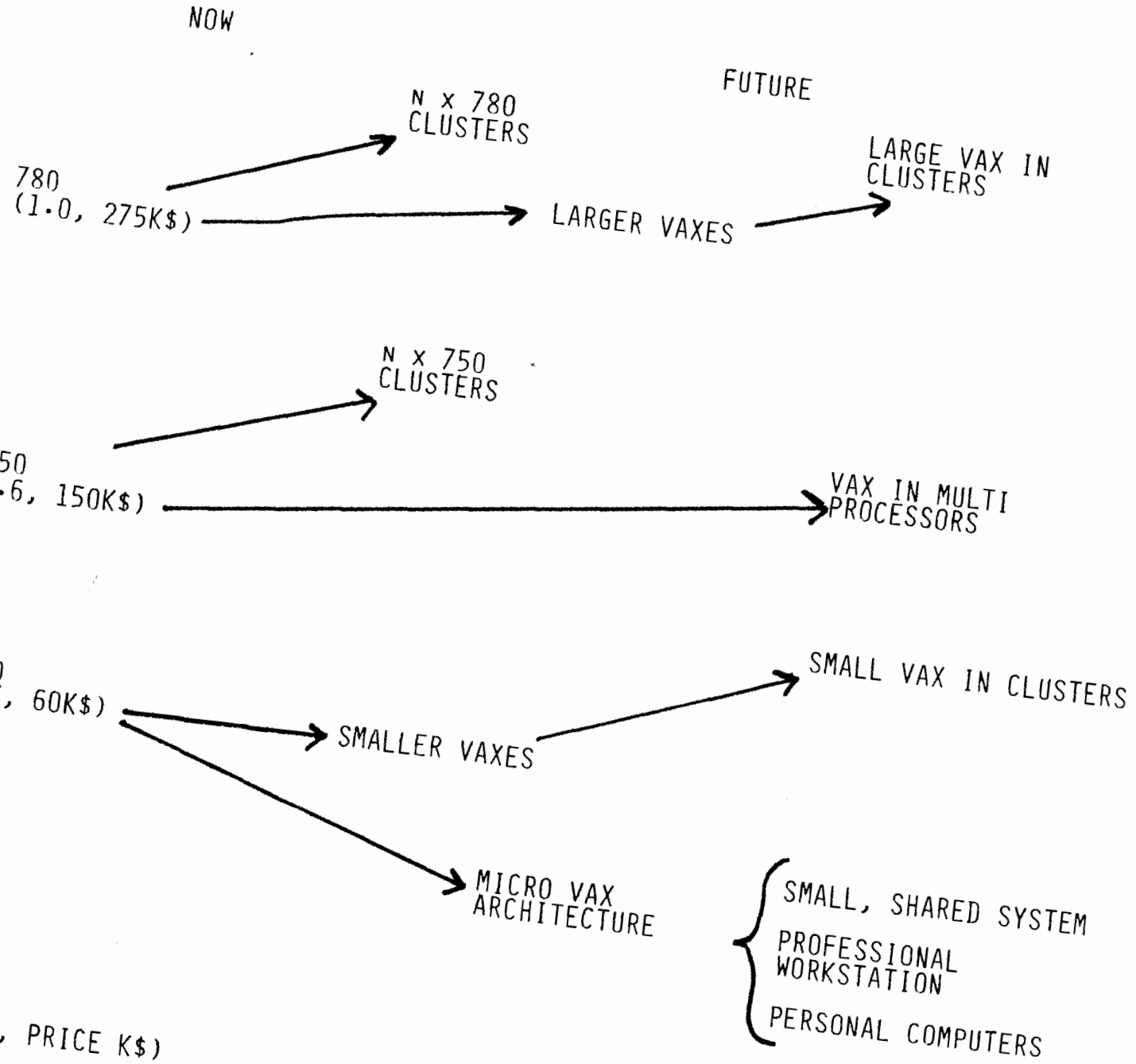
STRUCTURE

- KNOWLEDGE BASED SYSTEMS INCLUDING VARIOUS EXPERT SYSTEMS
- INTENSIVE COMMUNICATION OF ALL FORMS OF PEOPLE UNDERSTOOD DATA

USE

- SIGNIFICANT SUBSTITUTION OF COMPUTERS FOR OTHER INFORMATION PROCESSORS

EVOLUTION OF VAX FAMILY



(PERF, PRICE K$)

PERF: 780 = 1.0

EVOLUTION IN CENTRAL COMPUTING

LET'S DEFINE CLUSTERS

- AGGREGATION OF HOMOGENEOUS SINGLE AND MULTIUSER SYSTEMS (E.G., VAX/VMS, VAX/UNIX, DECSYSTEM 20, ALTOS, XEROX STAR)

- BEHAVING AS A SINGLE, MULTIPLE ACCESS SYSTEM (USUALLY SHARING A COMMON FILE SYSTEM)

- HIGH SPEED INTERCONNECT (10-100 MBITS/SEC) WITH HIGH CONNECTIVITY AMONG SYSTEMS

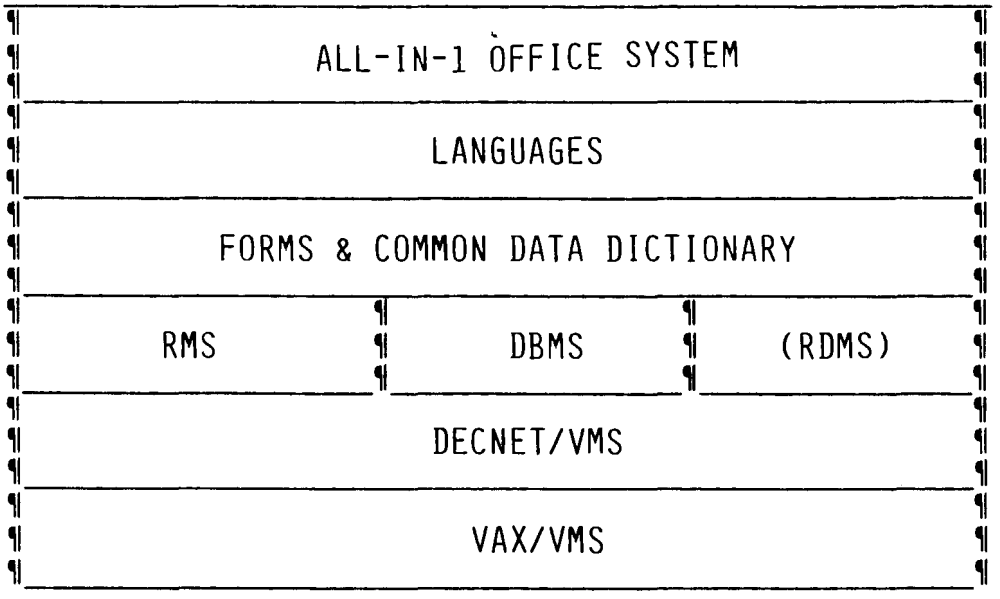
- SYSTEMS LOCATED IN A SINGLE MACHINE ROOM OR OFFICE AREA

- EXTENSION OF LOW LEVEL O/S SERVICES (FILE, PRINT/PLOT) VIA RELIABLE INTERSYSTEM MESSAGE BASED "PROCEDURE ORIENTED" PROTOCOL

WIDE AREA NETWORK DEFINITION
(WAN)

- AGGREGATE OF HETEROGENEOUS SYSTEMS AND NETWORKS
- PURPOSE IS TO CONNECT SYSTEMS ACROSS A WIDE AREA
- RELATIVELY LOW SPEED INTERCONNECT (4-64KB/SEC) ... 128KB/SEC
  LOW CONNECTIVITY (PABX, CIRCUIT AND PACKET SWITCHES)
  SYSTEMS LOCATED IN DIFFERENT REGIONS
- COMMUNICATION SERVICES BETWEEN AUTONOMOUS SYSTEMS VIA
  DECNET AND GATEWAYS TO OTHER NETWORKS (X.25/SNA...)

VAX INFORMATION ARCHITECTURE
(VIA)



COMPUTER GENERATIONS

- o A CONCURRENCE OF:
  - TECHNOLOGY
  - NEED
  - USE
  - STRUCTURE
- o GENERATION UNDER DEVELOPMENT TODAY IS THE FIFTH

GENERATION	NEED	USE	STRUCTURE
I. ELECTRONIC (MAGNETIC) 1945	DEFENSE	WAR MACHINE CONTROL	EDVAC, IAS WHIRLWIND, IBM 605
II. TRANSISTORS 1958	SPACE/SCIENCE	AIR DEFENSE AND CONTROL ENGR. AND SCIENTIFIC EDUCATION	TX-0, IBM 7090 ATLAS, STRETCH
III. INTEGRATED CIRCUITS 1966	TRANSPORTATION FLOW CONTROL AND WELFARE	PROCESS CONTROL AND SOCIAL ACCOUNTING	PDP-8, IBM 360 PDP-6, CDC 6600
IV. LSI 1972	ECONOMIC MODELS AND REAL TIME CONTROL	INTERACTIVE COMPUTING COMPUTERS FOR LOGIC	INTEL 4004, 8008, PDP-11 (RSTS) CRAY 1

FIFTH GENERATION

TECHNOLOGY

VLSI INCLUDING MEMORIES, LAN (CSMA/CD),
WINCHESTER DISKS AND HIGH RESOLUTION DISPLAYS

NEED

COMMUNICATIONS AMONG PEOPLE AND PROLIFERATING
COMPUTERS

STRUCTURE

- OFFICE AND HOME COMPUTING
- ? WHICH BUILDS THE BASIS FOR THE SIXTH GENERATION

ETHERNET: THE UNIBUS OF FIFTH GENERATION BECAUSE IT IS THE STANDARD TO INTERCONNECT COMPUTERS AND FORM A FULLY DISTRIBUTED SYSTEM

HOMOGENEOUS DISTRIBUTED COMPUTING APPROACH

(STRATEGIC TARGET FOR '85)

- ADOPT A SINGLE VAX-11/VMS ARCHITECTURE

- IMPLEMENT A WIDE RANGE OF PRODUCTS COVERING THE FOLLOWING COMPUTING "STYLES"

  - PERSONAL COMPUTING
  - TIMESHARED DEPARTMENTAL COMPUTING
  - CENTRAL COMPUTING

- INTERCONNECT THESE IN A HOMOGENEOUS NETWORK INCLUDING PERSONAL COMPUTING CLUSTERS

- BUILD CRITICAL AND UNIQUE APPLICATIONS

HOMOGENEOUS DISTRIBUTED COMPUTING APPROACH

(STRATEGIC TARGET FOR '85)

- ADOPT A SINGLE VAX-11/VMS ARCHITECTURE

- IMPLEMENT A WIDE RANGE OF PRODUCTS COVERING THE FOLLOWING COMPUTING "STYLES"
  - PERSONAL COMPUTING
  - TIMESHARED DEPARTMENTAL COMPUTING
  - CENTRAL COMPUTING

- INTERCONNECT THESE IN A HOMOGENEOUS NETWORK INCLUDING PERSONAL COMPUTING CLUSTERS
  Central-site
  Personal Computers.
- BUILD CRITICAL AND UNIQUE APPLICATIONS
  - Commercial
    - Data management
    - Transaction Processing
    - Office
  - Technical: Engineering, Lab., Factory
- Follow-on hardware & point products
  10/20
  PC's & WPS

DEC'S PRODUCT STRATEGY

PROVIDE A SET OF HOMOGENEOUS DISTRIBUTED COMPUTING SYSTEM PRODUCTS SO A USER CAN INTERFACE, STORE INFORMATION AND COMPUTE, WITHOUT RE-PROGRAMMING OR EXTRA WORK FOR THE FOLLOWING COMPUTER SYSTEM SIZES AND STYLES:

- AS A SINGLE USER, PERSONAL COMPUTER WITHIN A TERMINAL, AND EVOLVING TO PC CLUSTERS AND PC NETWORKS;
- AT A SMALL, LOCAL SHARED, DEPARTMENTAL COMPUTER SYSTEM, AND
- VIA A CLUSTER OF LARGE CENTRAL COMPUTERS
- WITH INTERFACING TO OTHER SYSTEMS FOR REAL TIME PROCESSING; AND
- ALL INTERCONNECTED VIA ETHERNET AND WIDE AREA NETWORKS

WHY THIS ARCHITECTURE?

- CUSTOMER INVESTMENT PROTECTED
  - DATA
  - PROGRAMMING
  - TRAINING
- HIGHEST FLEXIBILITY/COMPATIBILITY IN THE INDUSTRY
  - $50 CHIPS TO SEVERAL M$ CENTRALIZED CLUSTERS
- FEWEST SYSTEMS NEEDED TO SPAN RANGE, RESULTING IN
  - LOWER COST
  - HIGHER QUALITY
  - HIGHER RELIABILITY
- CLEAR DIRECTION LETS CUSTOMERS DEVELOP EFFECTIVE/FLEXIBLE PLANS
- FOCUS RESULTS IN RICHEST SET OF S/W TOOLS AND APPLICATIONS

CONTRAST BETWEEN VAX & CONVENTIONAL MAINFRAME

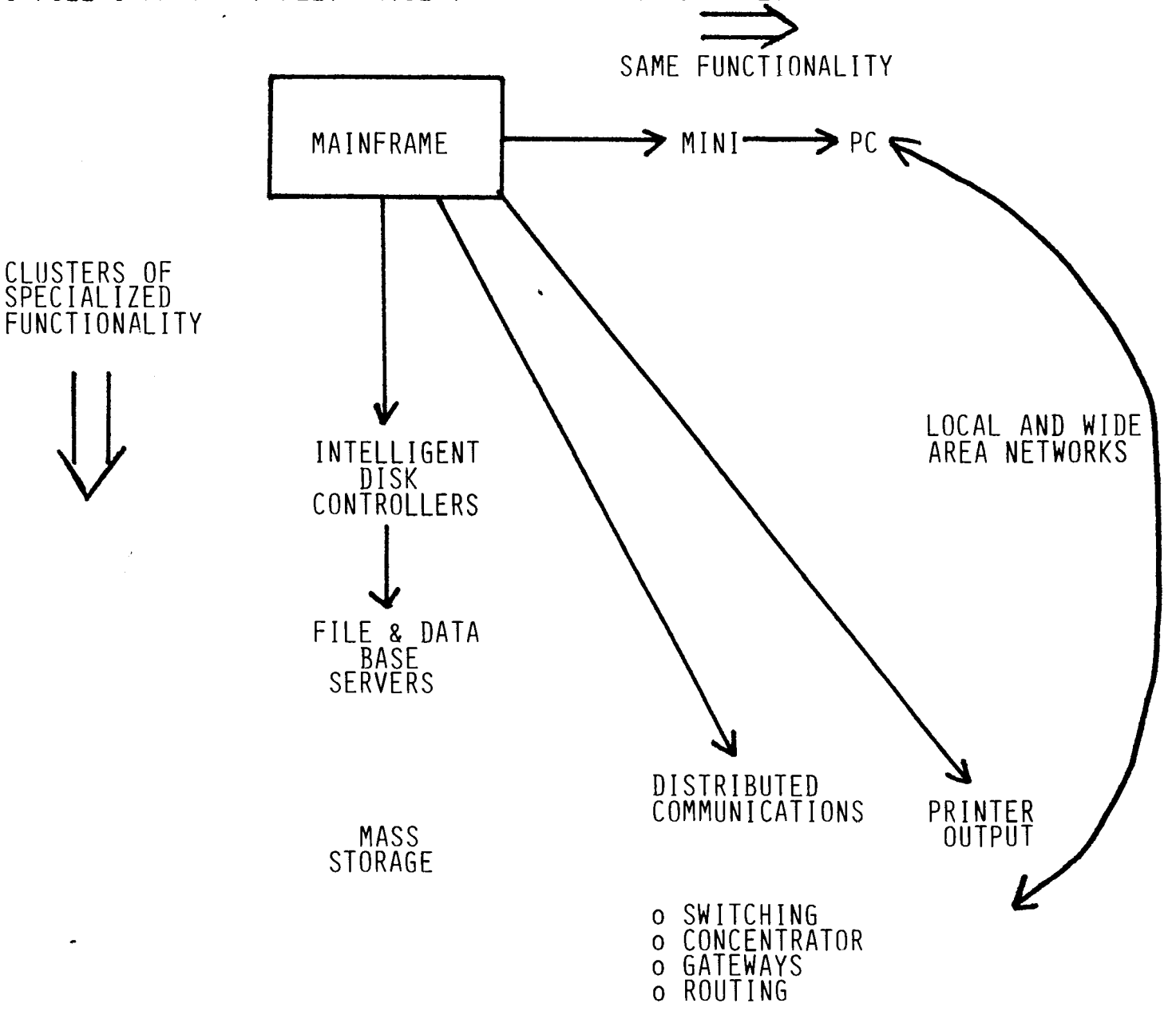
- NO CHANNELS!
- 1 OPERATING SYSTEM WITH ALL LAYERED PRODUCTS AVAILABLE
- LAYERED S/W TOOLS MORE FULLY INTEGRATED
  EXAMPLE: OFFICE AUTOMATION SYSTEM (ALL-IN-1)
- SUPERSET COMPATIBILITY WITH PDP-11 BASED DEPARTMENTAL SYSTEMS AND PC'S
- BUILT TO BE OPERATOR-LESS
- COVER A WIDER RANGE OF USE (COMPUTING STYLES) FROM PC TO MAINFRAME

EVOLUTION OF MAJOR COMPUTING STYLES

CENTRAL	MAINFRAME	CENTRAL CLUSTERS
DEPARTMENTAL/ GROUP	GENERAL PURPOSE	LOCAL AREA NETS OF: - GENERAL PURPOSE MINI'S - DEPARTMENTAL SERVERS - DEPARTMENTAL CLUSTERS OF PC'S
	MINI	- SUPER MICRO (YESTERDAY'S $100K MINI FOR $10K)
PERSONAL	DUMB TERMINAL INTELLIGENT TERMINAL TO SHARED SYSTEM	PERSONAL COMPUTING CLUSTERS

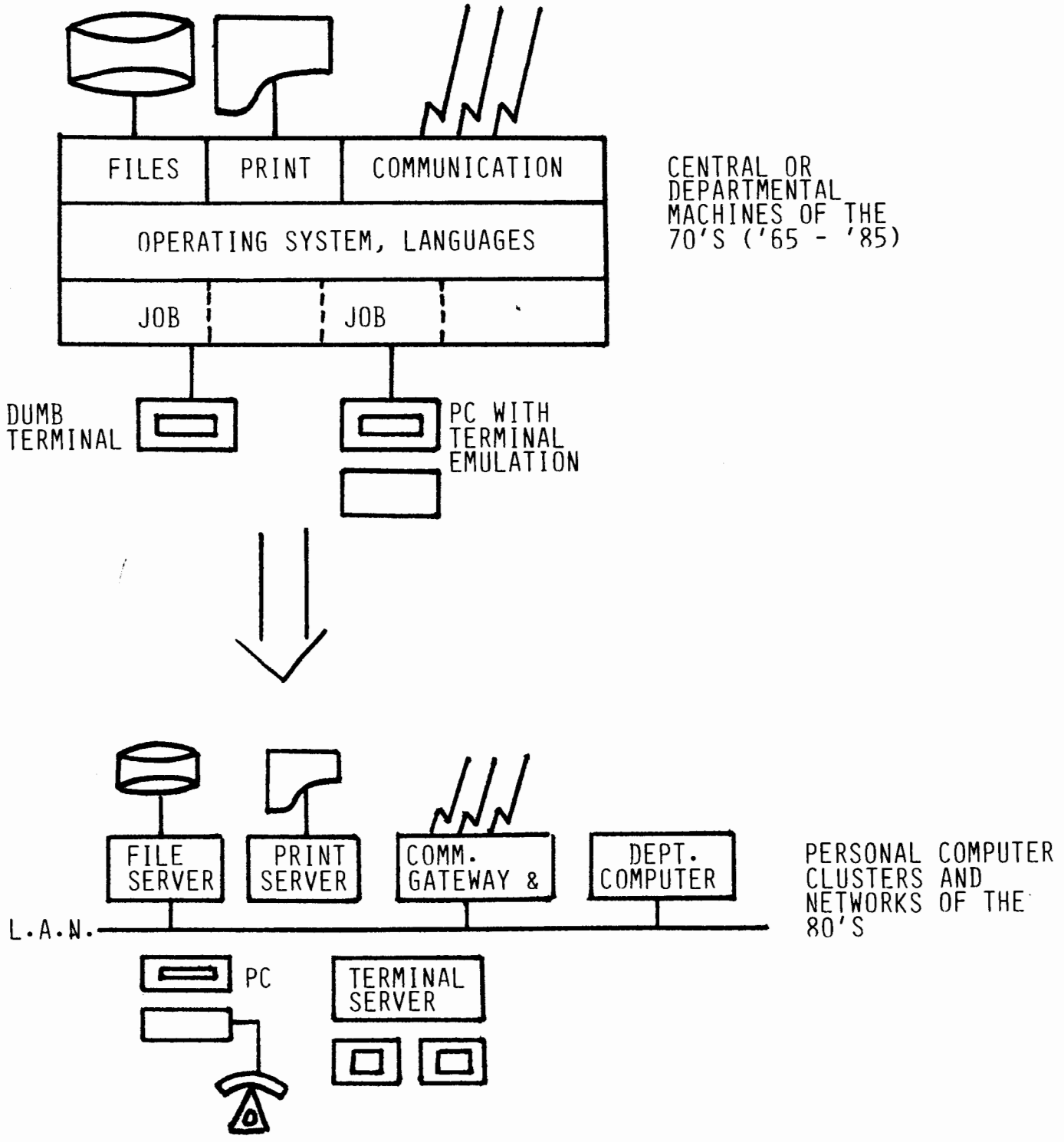
KEY EVOLUTIONARY TRENDS

- THE TWO SEPARATE TRENDS ARE VISIBLE TODAY
- FULL IMPACT NOT FELT UNTIL THE TWO ARE TIED TOGETHER



- WHEN LINKED, THEY'RE THE BASIS FOR THE NEXT GENERATION OF COMPUTING ARCHITECTURE
- CLUSTERS ARE AN ALTERNATAIVE TO LARGER SYSTEMS

KEY EVOLUTIONARY TRENDS



LOCAL AREA NETWORK DEFINITION
(LAN)

- AGGREGATION OF HETEROGENEOUS SYSTEMS
  (E.G., VAX/VMS-PC-TOPS 20-UNIX; GATEWAYS TO OTHERS)

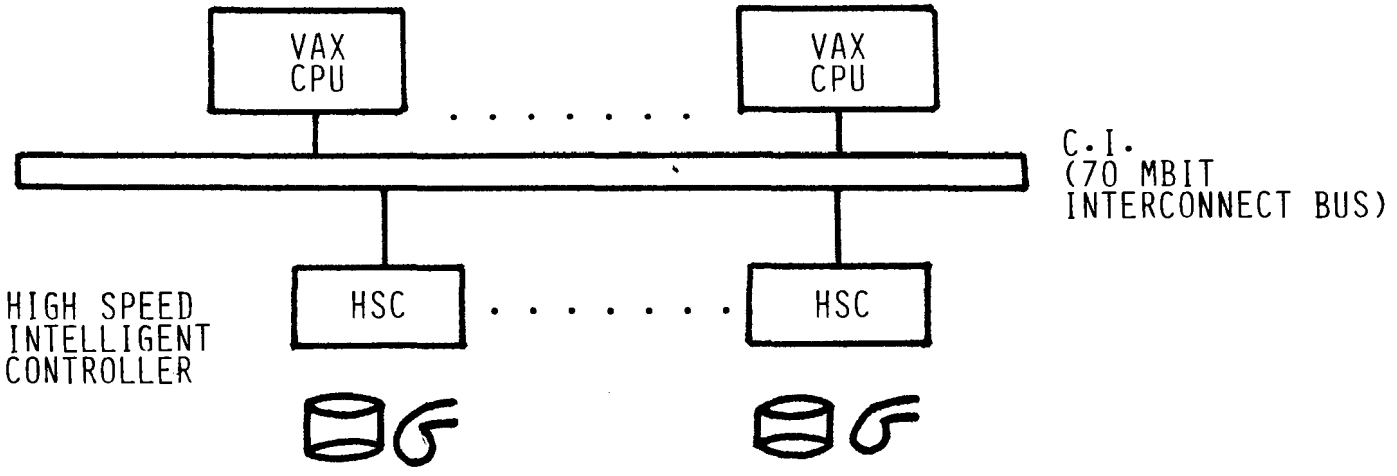
- PURPOSE IS TO CONNECT A NETWORK OF AUTONOMOUS SYSTEMS
  (MESSAGE, FILE, PROCESS, TERMINAL INTERCOMMUNICATION)

- RELATIVELY HIGH SPEED INTERCONNECT (1-30 MBITS/SEC)
  HIGH CONNECTIVITY AMONG SYSTEMS (AND CLUSTERS)
  SYSTEMS LOCATED IN AN OFFICE AREA, BUILDING, OR CAMPUS

- BASED ON ISO 7 LAYER NETWORK PROTOCOLS (APPLICATION)

TYPICAL DEC CLUSTER

(1983-1984)



- EITHER LARGE VAX OR DECSYSTEM 20 CPU'S
- SHARED DATA ACCESS

TYPICAL LARGE CLUSTER CAPACITY

	1983-1984	1984-1985
MIPS	8-->30*	30
BYTES X 10^9	80	160

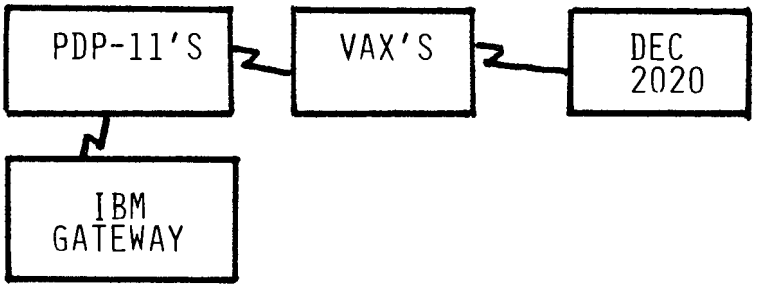
KEY NEW PRODUCTS IMPROVING CLUSTER CAPACITY

* - LARGE VAX (4 MIPS, LATE 1984)

- 900 MB 9" WINCHESTER DISKS (1985)

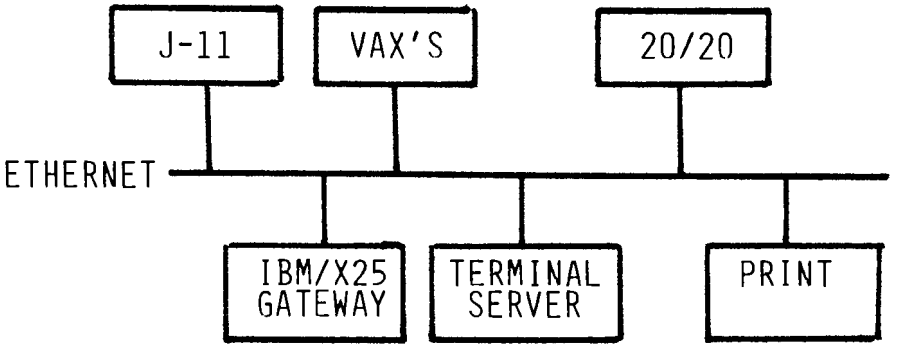
EVOLUTION OF DEPARTMENTAL COMPUTING

TODAY



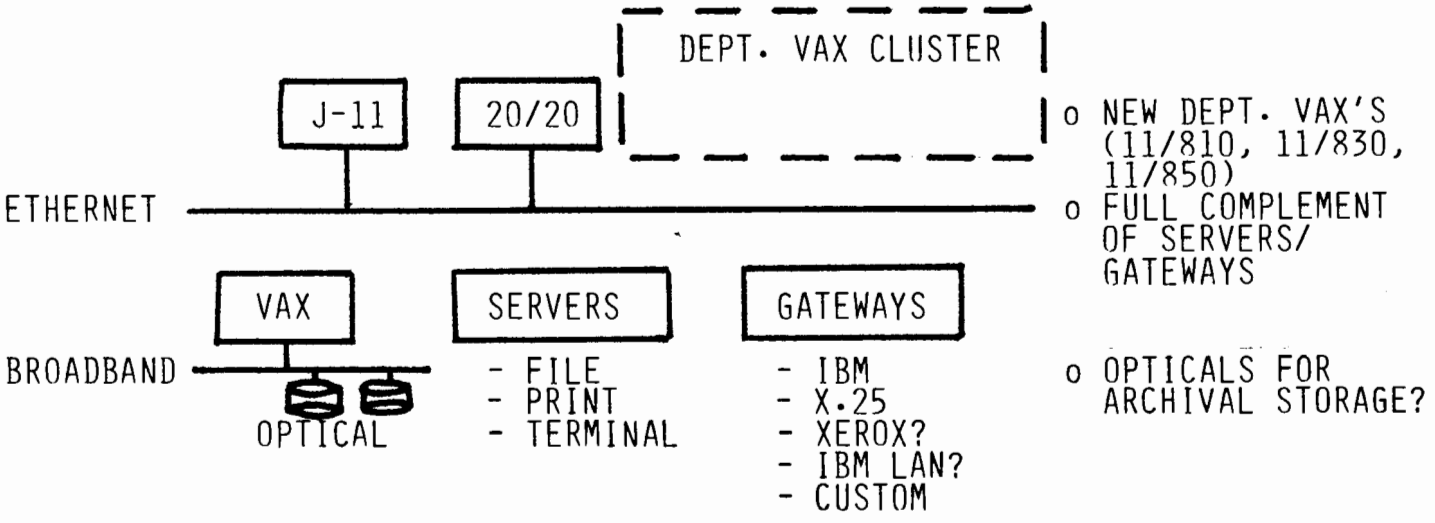
- o HETEROGENEOUS NETS
- o FLEXIBLE NET ARCHITECTURE (DECNET)
- o INITIAL GATEWAYS
- o COMM. SPEED <1M BIT/SEC

1983-1984



- o HETEROGENOUS "VIRTUAL TERMINALS"
- o ETHERNET (10M BITS/SEC)
- o VLSI PDP-11'S
- o MORE GATEWAYS
- o MORE SERVERS

1985


DEPT. VAX CLUSTER
J-11
20/20
ETHERNET
VAX
SERVERS
GATEWAYS
BROADBAND
OPTICAL
- FILE
- PRINT
- TERMINAL
- IBM
- X.25
- XEROX?
- IBM LAN?
- CUSTOM
o NEW DEPT. VAX'S (11/810, 11/830, 11/850)
o FULL COMPLEMENT OF SERVERS/ GATEWAYS
o OPTICALS FOR ARCHIVAL STORAGE?

EVOLUTION OF PERSONAL COMPUTING

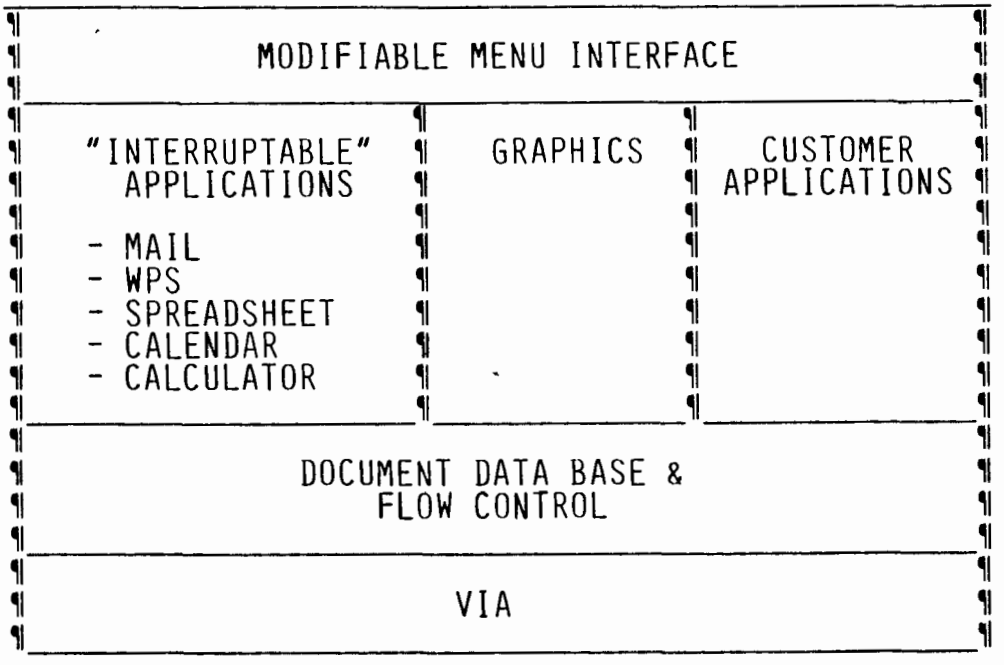
TODAY	1983-1984	1985
COMPATIBLE 16 BIT PC -->	PC CLUSTERS -->	COMPATIBLE 32 BIT PC
• PDP-11 BASED	• LOW COST "SMALL ETHERNET" FOR CLUSTERS	• μ VAX
• COMPATIBLE FILES, TOOLS, LANGUAGE	• DIRECT ETHERNET CONNECT	• VMS COMPATIBLE
• TELEPHONE MANAGEMENT	• FILE, PRINT, COMM. SERVERS	• 16 BIT PC'S FIELD UPGRADEABLE (?)
• BITMAP GRAPHICS (GREYSCALE & COLOR)	• VLSI PDP-11 CPU (.5 MIPS)	
• "STEREO COMPONENT" APPROACH		
• INTERNATIONALIZED		
• WINCHESTERS		
• DUMB TERMINAL EMULATION		

EVOLUTION OF PERSONAL COMPUTING
"DUMB" TERMINALS

- EVERY TERMINAL WILL BECOME A COMPUTING TERMINAL!

TODAY		1983		1984
UBIQUITOUS DUMB TERMINAL	----->	16 BIT PDP-11 STANDARD IN TERMINAL	----->	TERMINALS HANG ON ETHERNET
- VT100 INDUSTRY STANDARD		- PC KEYBOARD, MONITOR		- ACCESS TO ETHERNET DIRECTLY
		- MEDIUM RESOLUTION GRAPHICS		- ACCESS VIA TERMINAL SERVER
		- EMULATES OTHER TERMINALS		- TELEPHONE AND VOICE MANAGEMENT

ALL-IN-1 ARCHITECTURE



TRENDS IN GRAPHICS

- PROLIFERATION OF QUALITY GRAPHICS CAPABLE TERMINALS & PC WILL MAKE GRAPHICS COMMONPLACE IN NEXT TWO YEARS.

- SIGNIFICANT INCREASE IN PROFESSION-SPECIFIC APPLICATIONS AND LEVEL OF INTEGRATION IN OFFICE SYSTEMS.

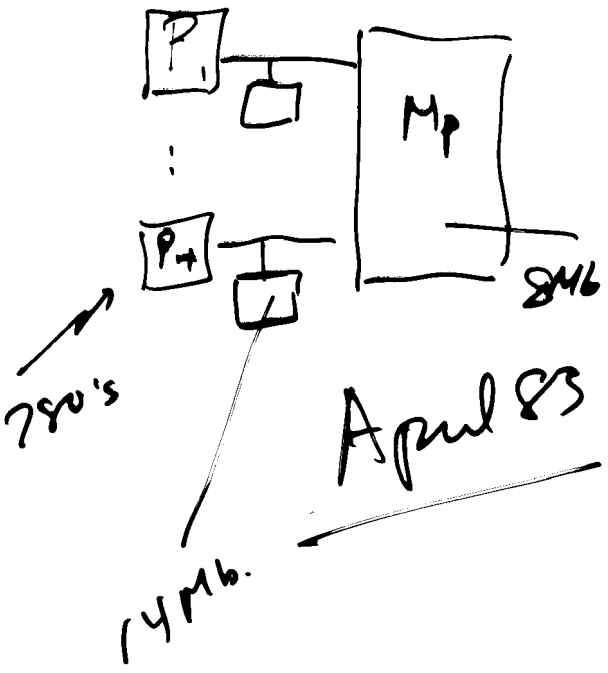
EXAMPLE: CURRENT ALL-IN-1 GRAPHICS

PRODUCT	USE	INTEGRATION
DECPLOT	DECISION SUPPORT MANAGEMENT SUMMARY	- CODASYL, ISAM DB'S - DUNN CAMERA & GRAPHICS PRINTER
DECSLIDE	PRESENTATION GRAPHICS	- IMAGE LIBRARY - LASER PRINTER
FINGRAPH	FINANCIAL MANAGEMENT (OPERATING RESULTS)	- "ACCOUNTING" APPLICATIONS - PRESENTATION COLOR MONITORS
EMPIRE	COMPLEX MODELING / DECISION SUPPORT	- DEPT. DB - PC-BASED GRAPHICS

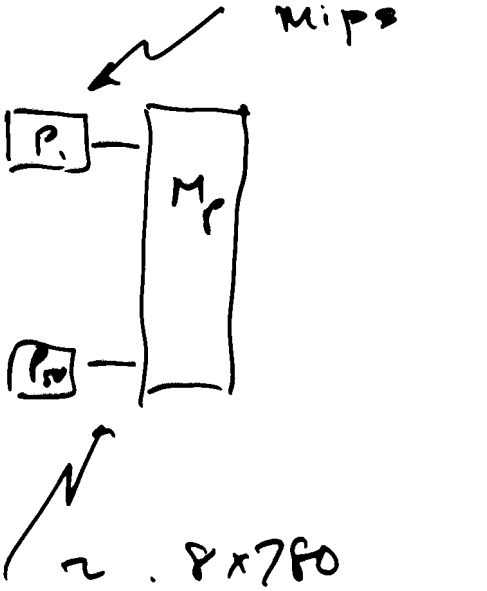
DATA MANAGEMENT TRENDS

- RAPIDLY EXPANDING USE OF RELATIONAL SYSTEMS WITHIN NEXT TWO YEARS
- INTEGRATION OF MULTIPLE DB TECHNIQUES THROUGH SINGLE, EASY-TO-USE, INTERFACES (2-5 YEARS)
- EXTENSION OF DATA TYPES TO INCLUDE TEXT, VOICE, IMAGE (2-5 YEARS)
- DISTRIBUTION TO CLUSTER SERVERS (NOW) FOLLOWED BY "DATABASE" SERVERS (3-5 YEARS)
- ROBUST DISTRIBUTED COMMON DATA DICTIONARIES (2-3 YEARS)

now.



April 85



~ . 8×780

(40×780)

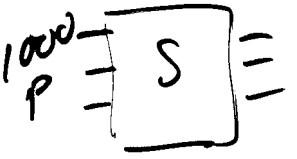
$250K

Sun ① →

② S1

③ Dataflow.

④ Cray n P.

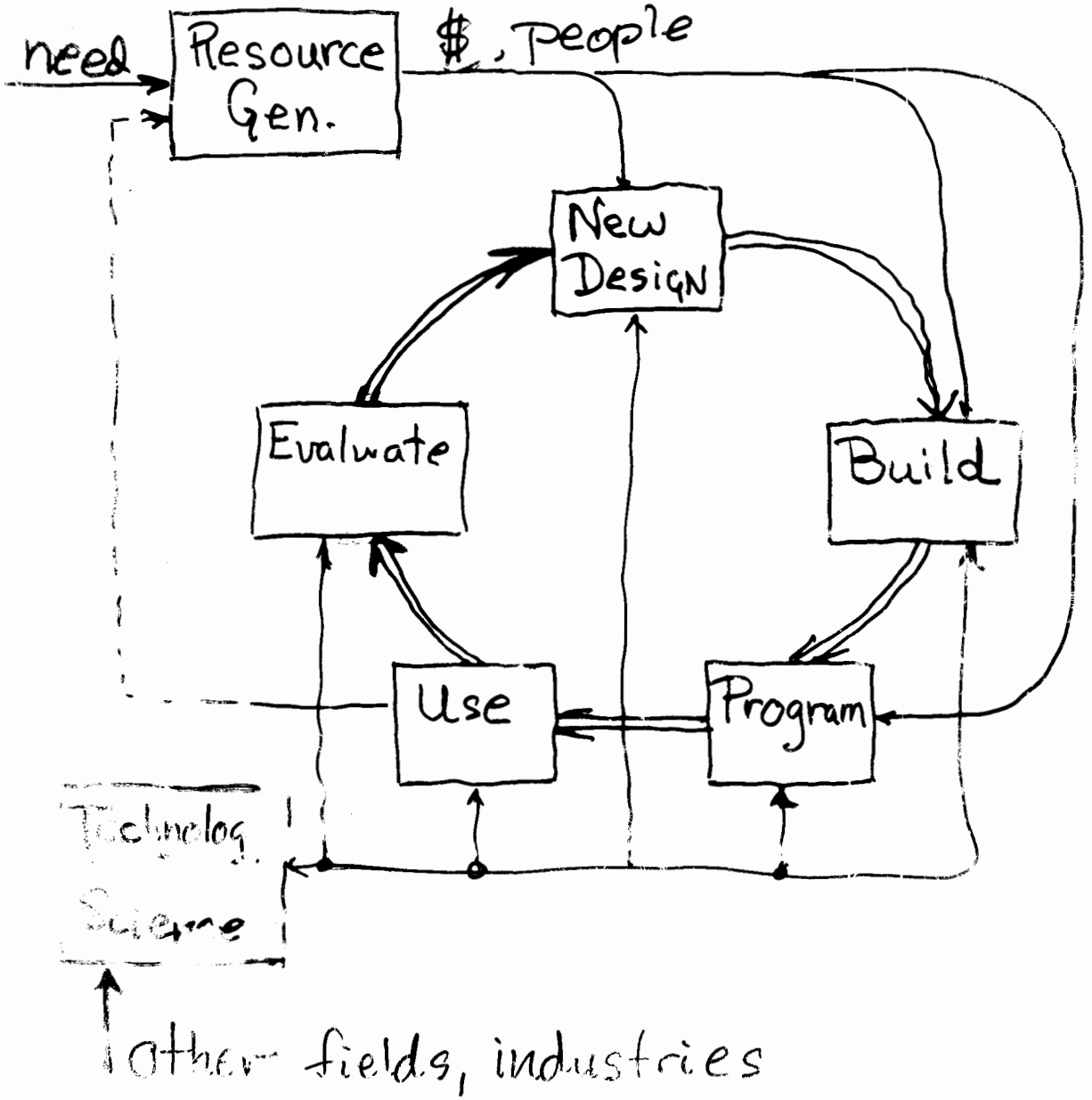


780 — $\frac{1}{40}$ × Cray 1

$\frac{\text{Cray}}{250K} = \frac{40}{10M.}$

Computer Generations Cycle:

Revolutionary? Evolutionary?



A GENERATION IS THE CONVERGENCE OF:

- NEED (EG. THREAT OF ANNIHILATION, GREED)

  FREEING RESOURCES – (also Frustration w/ [illegible]

- TECHNOLOGY AND SCIENCE

  THAT PROVIDE FOR BUILDING MACHINES

- New- ORGANIZATIONS TO BUILD NEW COMPUTING STRUCTURES

- USE TO CONFIRM A GENERATION (AFTER THE FACT)

```
procedure Entrepreneur_Venture_Cycle
                    trust > Reward And
while Greed > Fear do
    begin
    get PC Lotus 1-2-3
    write (business_plan);
                    VC, old VC Co.
    Get (funds);
    Exit {job}; start (New_company);
    Build (product);
    Sell (product);
    Sell (New_company); {@ 100 x Net Sales}
    funds := funds + company_value;
    Start (New_venture_company);
    end;
```

"If a computer understands English,
it must be Japanese."

-Alan Perlis

WHAT IS THE FIFTH GENERATION?

- PR ... ALSO A CREATIVE DREAM ... VISION
- TO ENGAGE US (CRITICS, COMPETITORS)
- TO LEARN TO DO RESEARCH [illegible] Better
- TO LEARN KNOWLEDGE ENGINEERING AND OTHER AI-BASED TECHNIQUES
- TO GET BY-PRODUCTS FROM FAR-OUT GOALS
- TO REPEAT SUCCESS IN SEMIS AND SUPERCOMPUTERS
- TO INCREASE PARALLELISM
- TO DETRACT US FURTHER FROM ENGINEERING & MANUFACTURING. (By believing in the magic of revolution.)

FIFTH GENERATION

TECHNOLOGY

VLSI INCLUDING MEMORIES, LAN (CSMA/CD),
WINCHESTER DISKS AND HIGH RESOLUTION DISPLAYS

NEED

COMMUNICATIONS AMONG PEOPLE AND PROLIFERATING
COMPUTERS

STRUCTURE

- OFFICE AND HOME COMPUTING
- ? WHICH BUILDS THE BASIS FOR THE SIXTH GENERATION

ETHERNET: THE UNIBUS OF FIFTH GENERATION BECAUSE IT IS THE
(i.e. LANs) STANDARD TO INTERCONNECT COMPUTERS AND FORM A FULLY
DISTRIBUTED SYSTEM

THE NEXT GENERATION: EVOLUTIONARY VIEW

- EVOLUTIONARY USE. WIDESPREAD ELECTRONIC MAIL.

  ELECTRONIC-BASED LOGIC TO ENCODE KNOWLEDGE

- NEED TO HAVE INFORMATION AT "FINGERTIPS" – Simple expertise based on facts
  (IN THE SYSTEM AND NOT IN PAPERS AND BOOKS)

- EVOLUTIONARY TECHNOLOGY WITH LARGER.

  DISTRIBUTED MEMORIES — VLSIzation!
  BETTER COMMUNICATION ?
- NEW COMPANIES. BUILD WITH EVOLVING TECHNOLOGY

THE NEXT GENERATION: REVOLUTIONARY VIEW

- REVOLUTIONARY USE DEPENDING ON VOICE AND NATURAL LANGUAGE COMMUNICATION
- GREATER COMMUNICATION AND PRODUCTIVITY NEEDS INCLUDING ROBOTICS, SPEECH AND NATURAL LANGUAGE,

Deep EXPERT SYSTEMS FOR COMPLEXITY AND PRODUCTIVITY, Creativity, Programs that learn.

- ROBOTICS, AND ARTIFICIAL INTELLIGENCE,

FAST-WANS, ULTRA- AND VLSI AND PARALLELISM

- AVANT GARDE ORGANIZATIONAL COOPERATION BETWEEN RESEARCHERS AND INDUSTRY

MICROPROCESSOR-BASED COMPUTER PRODUCTS

ON A DESK (PERSONAL COMPUTERS)

SMART TELEPHONES

TERMINALS

HOME (AND GAME)

PORTABLE PC'S

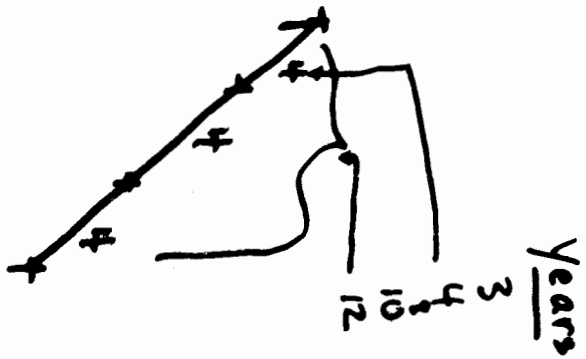
WORD PROCESSORS

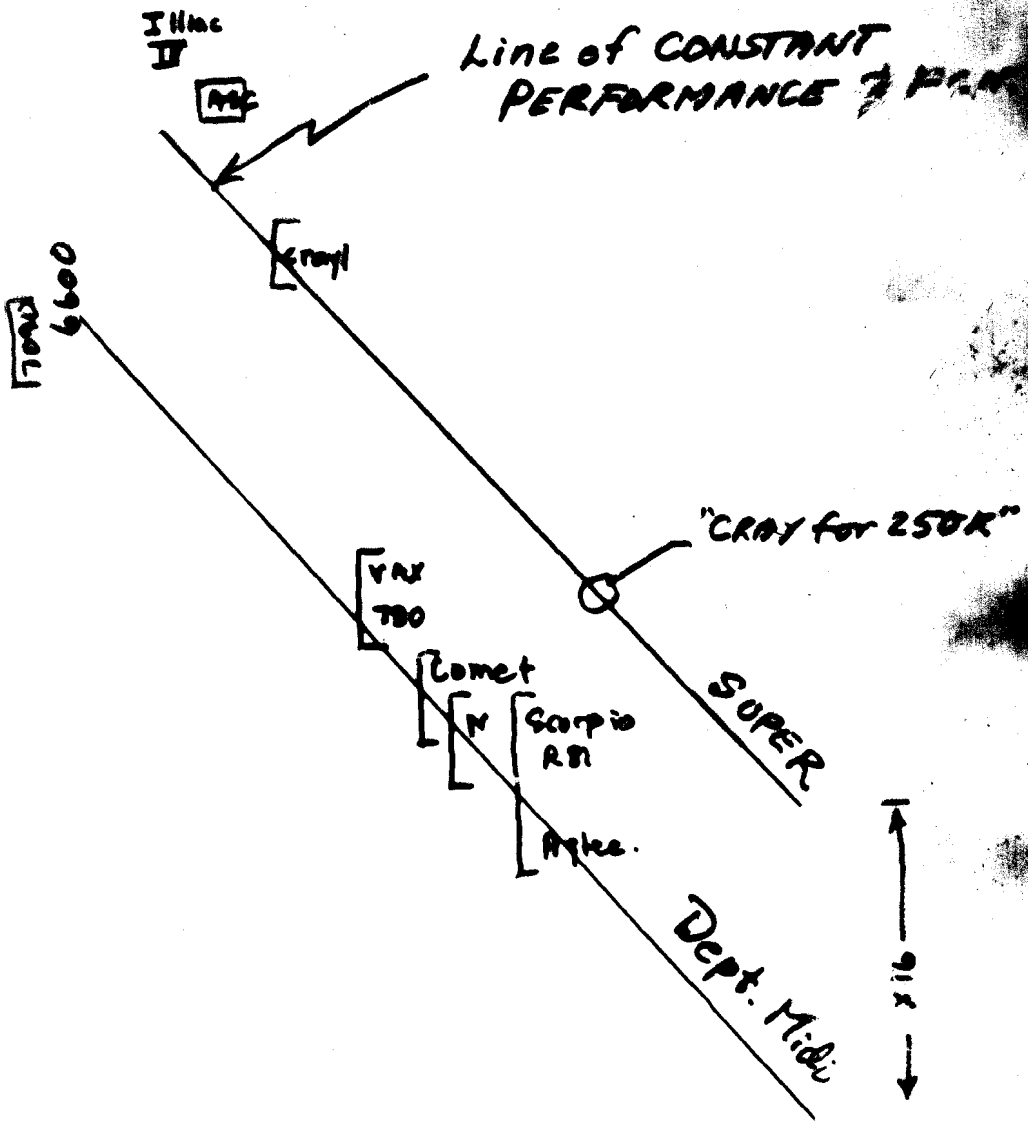
PC'S

WORKSTATIONS

Run shoes | Bicycle | Moped | Motor-cycle | Car | Bus | Train ⟶

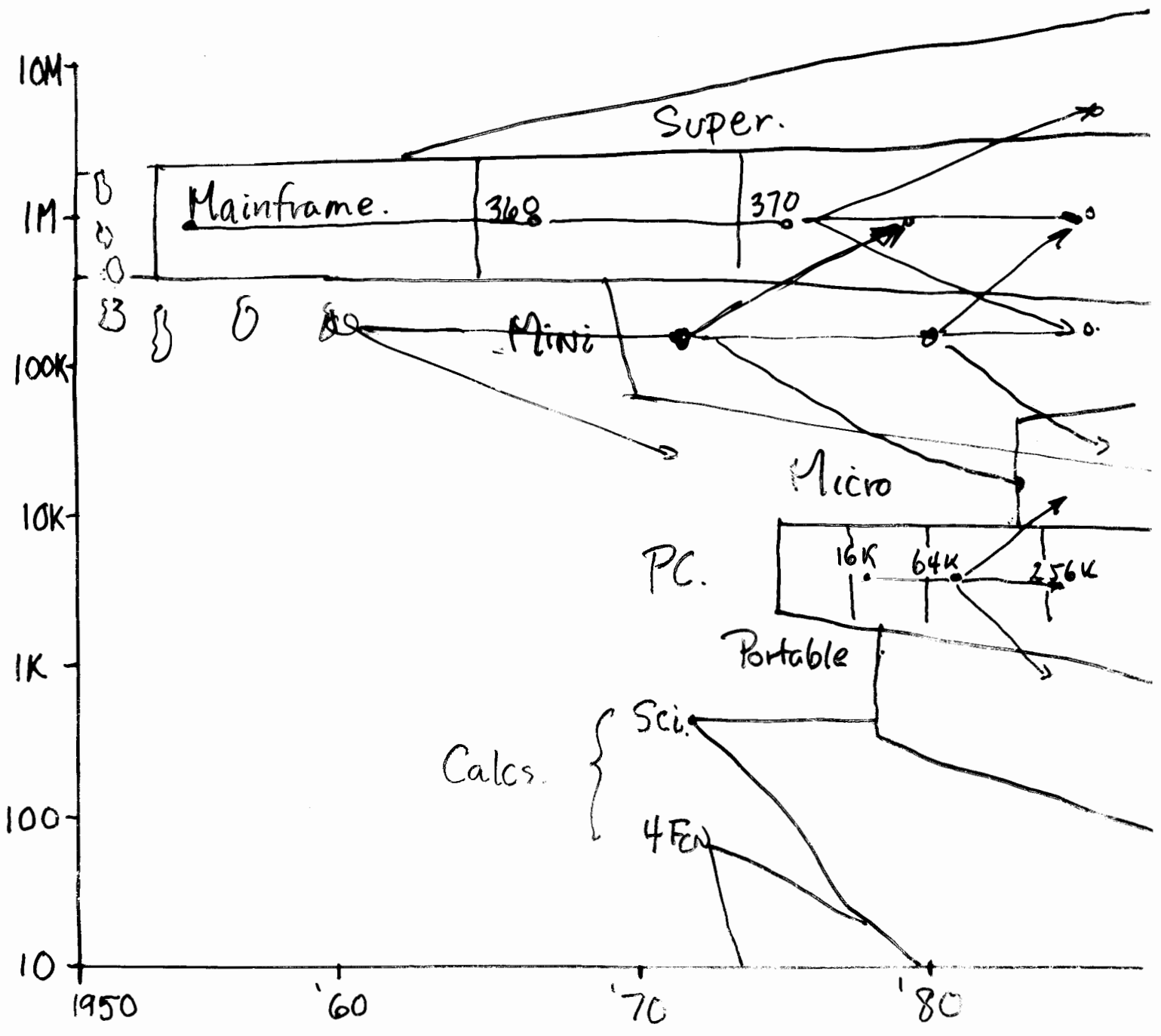
Small plane | Turbo. | Small Jet | 707 | DC10




IHmc II
Line of CONSTANT PERFORMANCE
"CRAY for 250K"
SUPER
Dept. Midi
9 x
6600
VAX 780
Comet
Scorpio R11
Apollo.

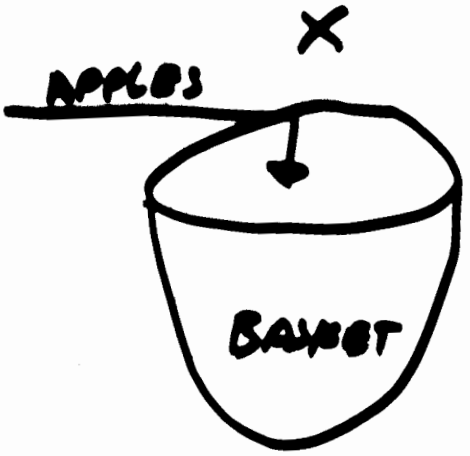
IBM
o-KL.
PDP-L
PDP-1
RSTS
LINC
PDP-8
D 315
Shared VAX
A III
CT
PVAX
A II
Department. Mini
TSS
PERSONAL
TTES
HP35
Prog. Calc
Personalized to telephones, tv, appliances, cars, instruments, books, etc.
SCI Calc.
4004

Digital Products
Household
Personal (portable)
Personal (mixed)
Personal (desk)
Home Ent.
Tom. Desk-bound
Cabinet(s)
Room
Physical Space (sq. feet)
Bldg.
'85
'90
50
60
70
80
90
2000
Year
2c. vtube
2c trans.
3c. IC
4c. LSI
5c VLSI
6c ULSI
7c.
Generation

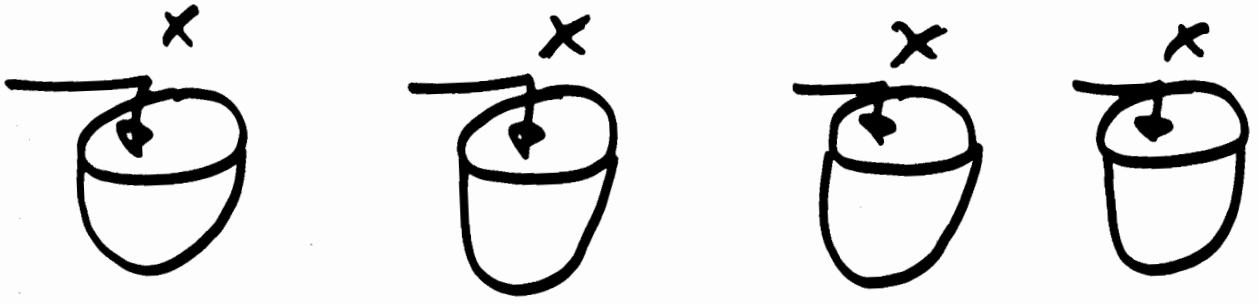

10M
1M
100K
10K
1K
100
10
1950
'60
'70
'80
Super.
Mainframe.
360
370
Mini
Micro
PC.
16K
64K
256K
Portable
Calcs.
Sci.
4 Fcn

MINICOMPUTER COMPANY LESSONS

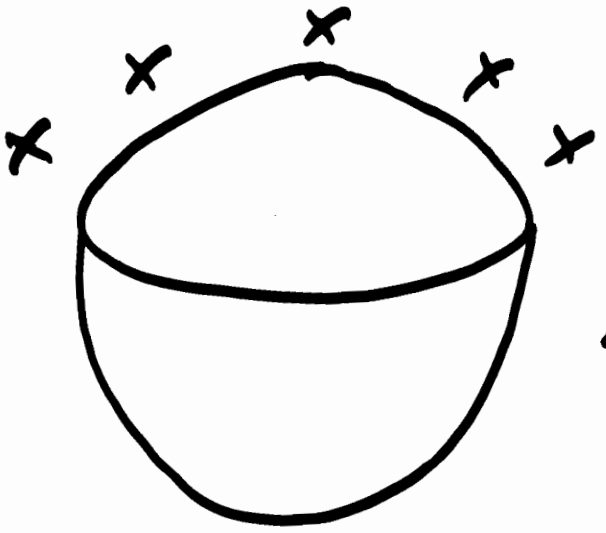
1. NEARLY 25% SURVIVED
2. ONLY 8% REALLY WON
3. ONLY 2% OF STARTUPS RETAINED AUTONOMY
4. MERGING WAS TRIED BY 10%
5. BUT ONLY 1/3 OF MERGERS WERE SUCCESSFUL
6. BEING A COMPUTER SUPPLIER DIDN'T HELP:
   ONLY DEC AND IBM MADE THE TRANSITION!
7. IBM ALWAYS WINS... EVENTUALLY
   (SYSTEM 3... SERIES 1)



UNIPROCESSOR



MULTICOMPUTER



MULTIPROCESSOR

PARALLEL
PROCESSING

The Current Generation:

- microprocessor (VLSI) based;
- Product Segmented industries
- Stratified* by Levels-of-integration
- Driven by Entrepreneurial Energy released by Venture Capital.

* Standards define the Strata

LEVELS-OF-INTEGRATION: THE STRATA

EARTH: IRON, SAND,...

SILICON WAFER: Bipolar → MOS → CMOS

STANDARD CHIP: MICROS, MICRO-PERIPHERALS, MEMORIES

8080 → Z80 → 8086+ → 68,000 (32-bit)
(4K) (16K) (64K) (256K).

BOARD: BUSES FOR PERFORMANCE, APPLICATIONS...

S100 → Multibus → PC Bus ---

ELECTROMECHANICAL: DISKS, I/O, POWER, ENCLOSURES...

8" → 5" → 3" Floppy
5" — Winch

OPERATING SYSTEM: COMMUNICATIONS, DATABASES, I/O... Processes

CP/M → MS/DOS → UNIX

LANGUAGE: INCLUDING APPLICATION LANGUAGES

Basic → C

GENERIC APPLICATION: WORD PROCESSING...

eg. Visicalc → Lotus 1-2-3

DISCIPLINE/PROFESSION SPECIFIC APPLICATION:

The Technology: hi, med, or low tech?

MICROCOMPUTER-BASED COMPANIES

BASIC INDUSTRIES	MICROCOMPUTER COMPANIES
POWER SUPPLIES	OPTIONAL
PACKAGING	OPTIONAL
SEMICONDUCTORS (MICROS, MEMORY, PERIPHERALS)	-
CRT'S AND TERMINALS	-
DISKS AND TAPES	-
BOARD OPTIONS	OPTIONAL
UNIX & DIAGNOSTICS	OPTIONAL
LANGUAGES & DATABASES	OPTIONAL
LAN'S / COMMUNICATION	OPTIONAL
APPLICATIONS	OPTIONAL
	SYSTEM INTEGRATION

ON DECLARING AND REACHING THE FIFTH GENERATION BY 1990

Gordon Bell

Chief Technical Officer
Encore Computer Corporation
and
Member of the Board of Directors
The Computer Museum, Boston Massachusetts

Wellesley Hills, Massachusetts, U.S.A.

This last month was marked by two significant events leading to the Fifth Generation: the Association of Computing Machinery's Fifth Generation Conference in San Francisco, and International Conference of Fifth Generation Computer Systems in Tokyo. The world's first international Computer Museum opened in Boston to record and help interpret the information processing generations.

As a person interested in the past and future history of computing, I have marked computer generations as the convergence of these factors:

- need (eg. threat of physical or industrial annihilation) freeing resources;
- technology and science that provide ideast for building the machines (whether physical computers or languages or applications machines);
- organizations that build the new structures; and
- user to confirm a generation (after the fact).

Each generation has a repetitive and cyclic pattern, followed by a new generation. A generation takes at least two trips around a three to four year cycle which has these stages: the understanding of past results and the application of a new technology to the design a new structure; followed by the actual architecture and design; followed by construction and manufacture. System software further accelerates the cycle in much the same way that an electron is accelerated in a cyclotron. Finally, the system is used and evaluated in order to form the basis of going around again.

The first two generations were marked by clear technology breakpoints in 1950 and 1960 utilizing vacuum tubes and transistors (invented in 1949) which allowed Fortran and Cobol to be developed, and widespread commercial and scientific use to occur. The third generation was declared by IBM to be the System 360, announced in April 1964, but is more accurately placed as 1970 when a new industry of small computers formed to build minicomputers, using the integrated circuit which had been invented in 1959. Reliable, multiprogrammed operating systems emerged for timesharing and real time system, permiting widescale interactive computing and small computers began to be embedded in other systems for control, communication, processing and memory. The first, single chip microprocessor was introduced in 1971.

The fourth generation may be marked as 1978-81 when VLSI

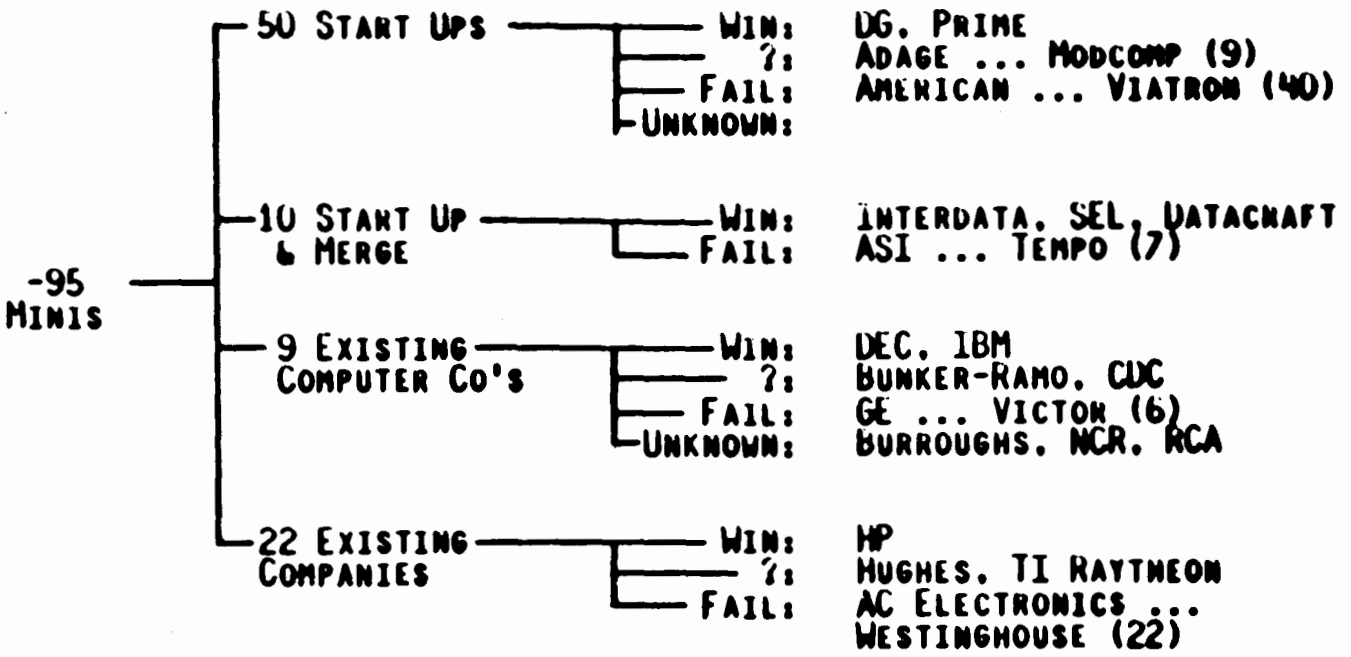
MAINFRAME TECHNOLOGY (1950, 1960)

BASIC INDUSTRIES	MAINFRAME COMPANIES
DISCRETE COMPONENTS	
TUBES, TRANSISTORS	PLUG-IN UNITS
MEMORIES	MEMORIES
	PERIPHERALS
	LANGUAGES
	APPLICATIONS
	SYSTEM INTEGRATION

MINICOMPUTER TECHNOLOGY (CIRCA 1970)

BASIC INDUSTRIES	MINICOMPUTER COMPANIES
POWER SUPPLIES	OPTIONAL
PACKAGING	ESSENTIAL
CORE MEMORY	OPTIONAL
SEMICONDUCTORS (MSI)	CPU AND MEMORIES
DISKS AND TAPES	PERIPHERAL CONTROLLERS
TERMINALS	-
	OPERATING SYSTEMS
	LANGUAGES
APPLICATIONS	OPTIONAL
	SYSTEM INTEGRATION

TABLE OF U.S. MINICOMPUTER COMPANIES (CIRCA 1970)



THE NEXT GENERATION WILL BE EVOLUTIONARY

- FUJITSU AND HITACHI HAVE RUN THE LIVERMORE KERNELS AT >2 x THE CRAY xmP USING EVOLUTION:
  - 25 YEAR OLD LANGUAGE - FORTRAN
  - 20 YEAR OLD ARCHITECTURE - 360/370
  - 25 YEAR OLD CIRCUITS AND SEMIS--ECL

COMPETING FOR THE NEXT GENERATION

. TURBULENCE DUE TO GENERATION TRANSITION

- NEW INDUSTRIES/PRODUCTS WITH MICRO

- VENTURE CAPITAL <--> ENTREPRENEURIAL ENERGY
  MANY, REDUNDANT, SHORT-TERM PRODUCTS
  THEREFORE, MUCH SHAKEOUT AND LOST EFFORT

- Gulf
  - Engineering ⟷ Science
    - Computer Science ≅ Software Eng.
      - Artifial Intelligence — Knowledge Eng.

GENERAL FACTORS IN COMPETING WITH JAPAN

- P = I x E (INTELLIGENCE, ENERGY)
- SOCIETAL VALUES
  - MEDICINE, LAW, POLITICS, ... , BUSINESS
  - SCIENCE, ENGINEERING, ... , MANUFACTURING
- TECHNOLOGICAL INFRASTRUCTURE
  - MATERIALS (SEMICONDUCTORS, MAGNETICS, ...
  - MECHANISMS
  - MANUFACTURING (CONTROL, ROBOTICS, ...
- MANAGEMENT - ESPECIALLY ENGINEERING AND MANUFACTURING
- QUALITY also – large, lithurgic Corps.
- LONG TERM VERSUS SHORT TERM

Trivial, Low-tech products

- JAPAN HAS DECIDED HOW TO ACCESS WORLD SOFTWARE

PROBLEMS IN RESEARCHING THE NEXT GENERATION

- RESEARCH ON THE NEXT GENERATION IS HARD
  - THERE ARE NO PROTOTYPES
  - UNIVERSITIES AND INDUSTRY ARE BOTH ILL-EQUIPPED!
  - LACK OF GOALS CREATES LOTS OF POOR PROJECTS
  - LOTS OF FUNDING - FEW PEOPLE.
    THEREFORE, TURBULENCE AND LOST EFFORT
  - LOTS OF POORLY STAFFED, SUB-CRITICAL PROJECTS
  - LARGE PROJECTS - LACK OF MANAGEMENT

- JAPAN Seems to know how to Couple to "World Research" (Versus European / U.S. Industries)

CRITICAL EXTENSIONS TO UNIX

. PERFORMANCE & RELIABILITY & SECURITY

. VIRTUAL MEMORY

. APPLICATIONS: REAL TIME, TRANSACTION PROCESSING, ETC.

. MODERN HUMAN INTERFACE. EVENTUALLY ~~EGA~~ WINDOWING, GRAPHICS

. MULTIPROCESSING

. WIDE AREA NETWORKS

. LOCAL AREA NETWORKS (LAN) AND CLUSTERS (LANC)

The Challenge

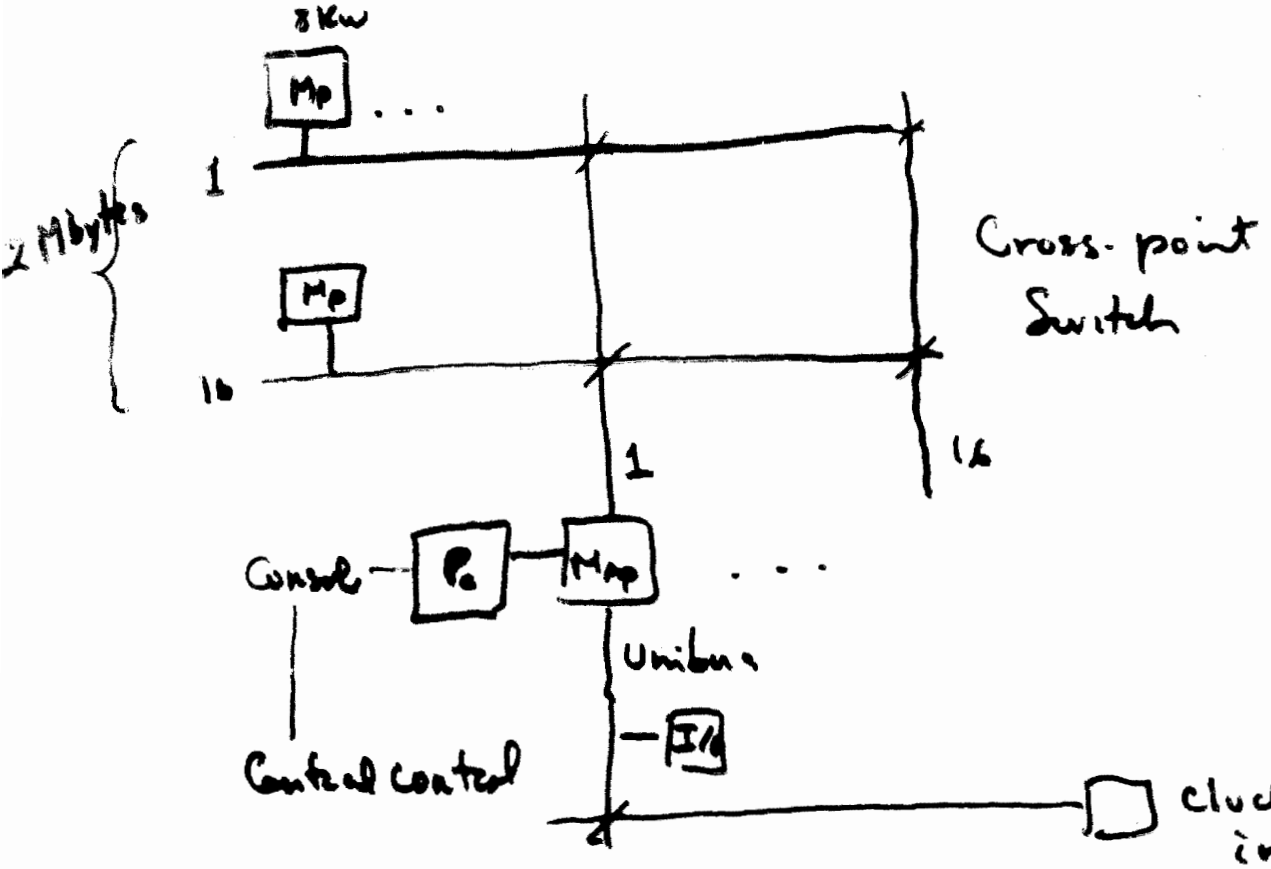
- UNIX... but
- Standards permit faster evolution and building on each other's work.
- Standards permit the Strata to form and ultimate entrepreneurism — Small is Beautiful
- Creativity abounds —
  - Trilogy
  - Macintosh
  - Silicon Graphics
  - CAD/CAM Companies.
- Next Generation of VLSIzation.
- Interest in Manufacturing — including Components

C.mmp 16 P_c Multiprocessor (1 O/S) 1972

pp. 7

1/40

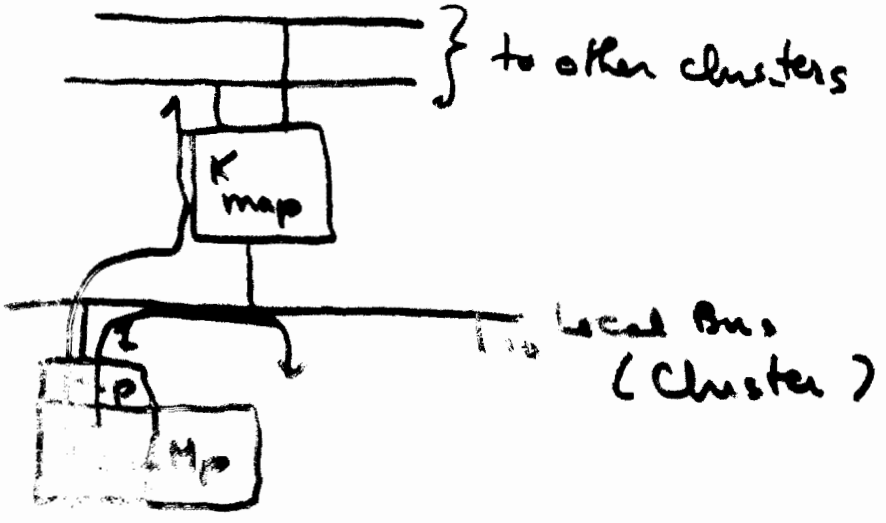
with WCS



C.M* - Computer Modules - 1974 10 P_c

1979 50 P_c

P_c = LSI-11



Data/Program

- Local - [illegible]
- Within Cluster
- Across Cluster (12 μs/[illegible])

SELECTED UNIVERSITY-BASED COMPUTERS

MACHINE	FIRST USE	CONCEPT-USE	USE	USE/LIFE
HARVARD MARK I - IBM ASCC	8/44	7	15	.7
IBM SSEC	1/48	-	4.5	.6
ENIAC	6/46	4	9	.7
MIT WHIRLWIND	6/50	5.5	9	.6
MIT/LINCOLN LAB TX-0	57	3	8	.8
EDSAC	5/49	2.5	8	
Mark I	6/48	1.5*,**	6*	

* Proto ** Ferranti Version 2/51 - 4

Machine	First Use	Concept-Use	Use	Use/Life
ILLIAC I	9/52	4	10	.7
ILLIAC II	6/65	5.5	3	.3
ILLIAC IV	11/75	12	6.5	.3
CMU C.mmp	5/75	5	6	.7
CMU Cm*	9/76	4	>6	>.6
TEXAS TRAC	83	7	>1	>.1

STANDARDS

SPECIFIES INTERCONNECTION OF TWO (OR MORE) MORE PARTS

VANITY: EXISTS WITHIN A SINGLE COMPANY

DE FACTO: ORIGIN IS A SINGLE COMPANY, EVERYONE FOLLOWS

...SOME STANDARDS ORGANIZATION MAY BLESS I

INDUSTRY: EXISTS WITHIN A SINGLE COMPANY (IBM)

NATIONAL: (EG. ANSI, VDE, ISA)

FEDERAL: (EG. NBS)

INTERNATIONAL: (EG. ISO, IFIP, ECMA, CCITT)

PROFESSIONAL ORGANIZATION: (EG. IEEE, ASME)

CONSIDERATIONS FOR FUTURE COMPCON ON STANDARDS

KINDS OF STANDARDS THAT DON'T CONSTRAIN CREATIVITY.

YET ARE ESSENTIAL TO PROVIDE A PATHWAY FOR THE FUTURE

NATURE OF GOALS AND CONSTRAINTS FOR FUTURE STANDARDS

ROLES OF VARIOUS ORGANIZATIONS: MANUFACTURERS, USERS,

STANDARDS BODIES, PROFESSIONAL ORGS., ACADEMIA

TIMING IN RESEARCH, PRODUCT, AND USE LIFE CYCLE

MAINTAINING, EVOLVING AND DISCARDING STANDARDS

ECONOMICS OF SINGLE AND MULTIPLE STANDARDS

A PRODUCT SEGMENTED INDUSTRY, ORGANIZED BY

LEVELS OF INTEGRATION WHICH FORM STRATA*.

FUELED BY ENTREPRENEURIAL ENERGY

RELEASED BY VENTURE CAPITAL FUNDS

SOFTWARE FORMS NEW PRODUCTS AND USES

SYSTEMS ARE DELIVERED IN MANY DIFFERENT WAYS

*STANDARDS DEFINE THE STRATA

GUIDELINES FOR STANDARDS

SPONSORED... NOT JUST A COMMITTEE OR COMMITTEES

REAL (IMPLEMENTABLE AND TESTABLE)

PRECISE, UNDERSTANDABLE AND APPLICABLE

FEW, NOT ALL POSSIBLE ONES FOR A GIVEN FUNCTION

TIMELESS, AND

EXTENDABLE IN A RESPONSIVE FASHION

LEVELS OF INTEGRATION: THE STRATA

SILICON WAFER:

STANDARD CHIP: MICROS, MICRO-PERIPHERALS, MEMORIES

BOARD: BUSES FOR PERFORMANCE, APPLICATIONS...

ELECTROMECHANICAL: DISKS, I/O, POWER, ENCLOSURES...

OPERATING SYSTEM: COMMUNICATIONS, DATABASES, I/O...

LANGUAGE: INCLUDING APPLICATION LANGUAGES

GENERIC APPLICATION: WORD PROCESSING...

DISCIPLINE/PROFESSION SPECIFIC APPLICATION:

```
procedure VENTURE_CAPITAL_ENTREPRENEURIAL_ENERGY_CYCLE

    begin
    while greed and not fear do
    write (business plan);
    get (venture funds);
    exit (job); start (new company);
    build (product); sell (product);
    sell (company); (for 100 times sales)
    venture funds := venture funds + sale_liquidity;
    end
```

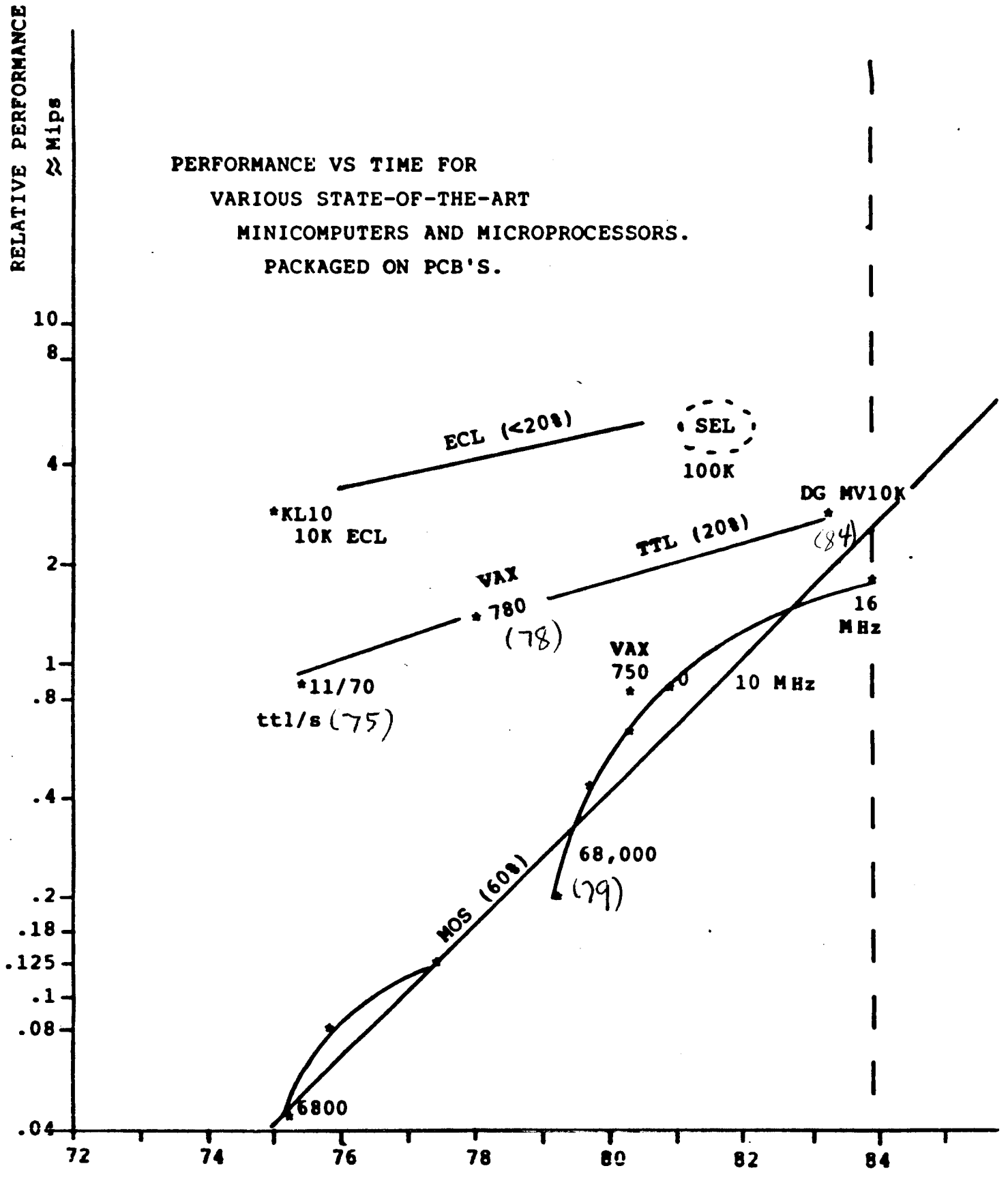
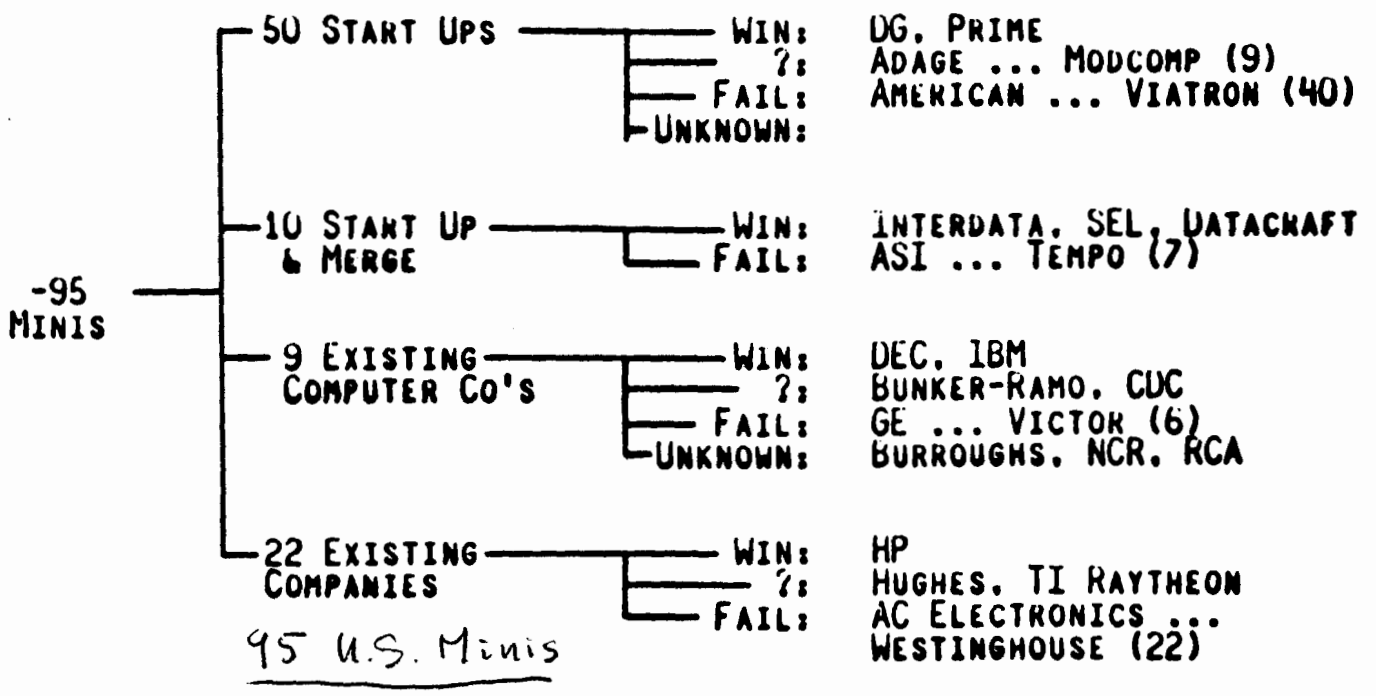

RELATIVE PERFORMANCE
≈Mips
PERFORMANCE VS TIME FOR
VARIOUS STATE-OF-THE-ART
MINICOMPUTERS AND MICROPROCESSORS.
PACKAGED ON PCB'S.
10
8
4
2
1
.8
.4
.2
.18
.125
.1
.08
.04
72
74
76
78
80
82
84
ECL (<20K)
SEL
100K
*KL10
10K ECL
DG MV10K
(84)
TTL (20K)
VAX
* 780
(78)
16
MHz
VAX
750
10 MHz
*11/70
ttl/s (75)
68,000
(79)
MOS (60K)
6800

TABLE OF U.S. MINICOMPUTER COMPANIES (CIRCA 1970)



MICROPROCESSOR-BASED COMPUTER PRODUCTS

On a Desk (Personal Computers)

- Smart Telephones
- Terminals
- Home (and game)
- Portable PC's
- Word Processors
- PC's
- Workstations

"IF A COMPUTER UNDERSTANDS ENGLISH.
IT MUST BE JAPANESE."

-ALAN PERLIS

MICROPROCESSOR-BASED COMPUTER PRODUCTS

THE DESK (DEPARTMENTAL AND GROUP-LEVEL COMPUTERS)

- SUPER MICRO / small micro
- CLUSTERED, FUNCTIONAL MULTIPROCESSOR
- SYMMETRIC MULTIPROCESSOR
- HIGH-AVAILABILITY
  - SINGLE COMPUTER VIA VOTING
  - MULTIPROCESSOR (N+1) REDUNDANCY
  - MULTI-COMPUTER CLUSTERS

A GENERATION IS THE CONVERGENCE OF:

-NEED (EG. THREAT OF ANNIHILATION, GREED) FREEING RESOURCES

-TECHNOLOGY AND SCIENCE THAT PROVIDE FOR BUILDING MACHINES

-ORGANIZATIONS THAT BUILD NEW COMPUTING STRUCTURES

-USE TO CONFIRM A GENERATION (AFTER THE FACT).

THE FOURTH GENERATION

-EVOLUTIONARY USE BASED ON TRADITIONAL WORD AND DATA PROCESSING, MACHINE-AIDED ENGINEERING AND MANUFACTURING, AND EMBEDDED COMPUTING

-MASSIVE INTER-COMMUNICATIONS AND PRODUCTIVITY NEEDS TO INCREASE USE

-WELL-DEVELOPED TECHNOLOGIES, INCLUDING POWERFUL VLSI MICROPROCESSORS, LANS, MAGNETICS, DISPLAYS AND STANDARD SOFTWARE

-NEW ORGANIZATIONS TO BUILD NEW COMPUTER STRUCTURES, BUT

-NEW USES THAT EVOLVE FROM GREATER ACCESS WON'T BE APPARENT FOR AT LEAST A DECADE

THE NEXT GENERATION: EVOLUTIONARY VIEW

-EVOLUTIONARY USE WITH WIDESPREAD ELECTRONIC MAIL AND ELECTRONIC-BASED LOGIC TO ENCODE KNOWLEDGE (EG. CAD/CAM)

-NEED TO HAVE INFORMATION AT "FINGERTIPS" (IN THE SYSTEM AND NOT IN PAPERS AND BOOKS)

-EVOLUTIONARY TECHNOLOGY WITH LARGER, DISTRIBUTED MEMORIES

-NEW COMPANIES TO BUILD WITH EVOLVING TECHNOLOGIES

THE NEXT GENERATION: REVOLUTIONARY VIEW

-REVOLUTIONARY USE DEPENDING ON VOICE AND NATURAL LANGUAGE COMMUNICATION

-SOPHISTICATED INTER-COMMUNICATION AND PRODUCTIVITY NEEDS INCLUDING EXPERT SYSTEMS TO HANDLE COMPLEXITY AND IMPROVE PRODUCTIVITY

-ROBOTICS, AND ARTIFICAL INTELLIGENCE, FAST-WANS TO SERVE LANS, BASED ON U- AND VLSI AND PARALLELISM TECHNOLOGIES

-AVANT GARDE ORGANIZATIONAL CO-OPERATION BETWEEN RESEARCHERS AND INDUSTRY TO PIONEER NEW COMPUTER STRUCTURES

MINICOMPUTER COMPANY LESSONS

1. NEARLY 25% SURVIVED

2. ONLY 8% REALLY WON

3. ONLY 2% OF STARTUPS RETAINED AUTONOMY

4. MERGING WAS TRIED BY 10%

5. BUT ONLY 1/3 OF MERGERS WERE SUCCESSFUL

6. BEING A COMPUTER SUPPLIER DIDN'T HELP:
   ONLY DEC AND IBM MADE THE TRANSITION TO MINIS!

7. IBM ALWAYS WINS . . . EVENTUALLY
   (SYSTEM 3 ... SERIES 1)

MINICOMPUTER TECHNOLOGY (CIRCA 1970)

BASIC INDUSTRIES	MINICOMPUTER COMPANIES
POWER SUPPLIES	OPTIONAL
PACKAGING	ESSENTIAL
CORE MEMORY	OPTIONAL
SEMICONDUCTORS (MSI)	CPU AND MEMORIES
DISKS AND TAPES	PERIPHERAL CONTROLLERS
TERMINALS	-
	OPERATING SYSTEMS
	LANGUAGES
	APPLICATIONS
	SYSTEM INTEGRATION

MICROCOMPUTER-BASED COMPANIES

BASIC INDUSTRIES	MICROCOMPUTER COMPANIES
POWER SUPPLIES	OPTIONAL
PACKAGING	OPTIONAL
SEMICONDUCTORS (MICROS, MEMORY, PERIPHERALS)	-
CRT'S AND TERMINALS	-
DISKS AND TAPES	-
BOARD OPTIONS	OPTIONAL
UNIX & DIAGNOSTICS	OPTIONAL
LANGUAGES & DATABASES	OPTIONAL
LAN'S AND COMMUNICATION	OPTIONAL
APPLICATIONS	OPTIONAL
	SYSTEM INTEGRATION

PARALLEL COMPUTING

NETWORK - WITH LAN OR WAN INTERCONNECT

CLUSTER - WITH LAN INTERCONNECT

FUNCTIONAL - ONE PROCESSOR PER FUNCTION

CLOSE AREA NET CLUSTER - HIGH SPEED INTERCONNECT

TIMESHARING - ONE PROCESSOR PER USER

PARTITIONED - ONE PROCESSOR PER PROCESS

TRANSACTION PROCESSING - PROCESSOR PER TRANSACTION STEP

FAULT-TOLERANT - DIFFERENT PROCESSORS ASSIGNED PER STEP
WITH REDUNDANT COMPUTATION

CONCURRENT-TASK - PARALLEL PROCESSING OF A TASK BY
PARTITIONING FOR INDEPENDENT DATA

PIPELINED-TASK - PARALLEL PROCESSING OF A TASK

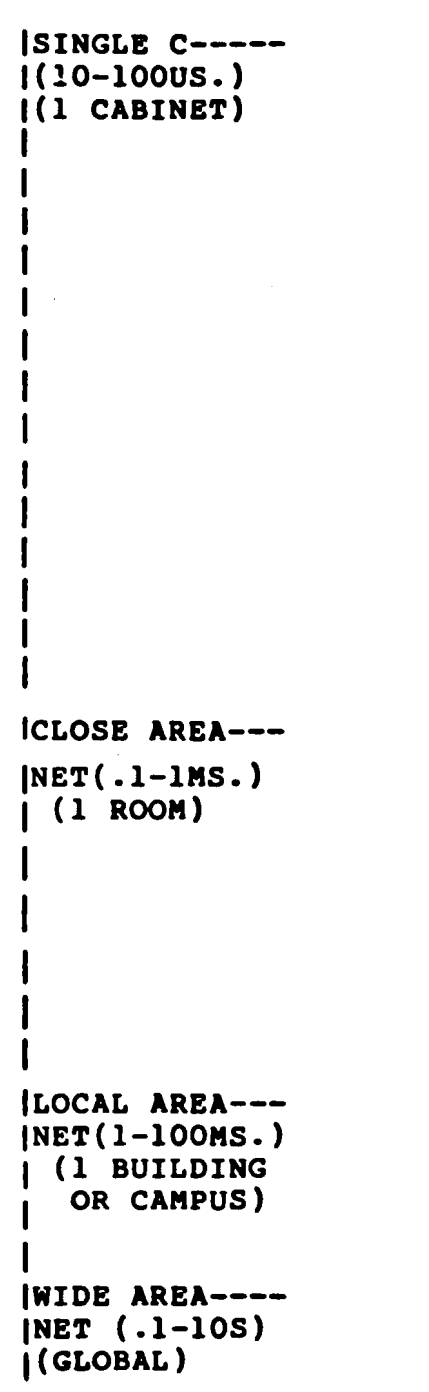
PARALLEL PROCESSING - PROCESSORS WORK ON A SINGLE TASK

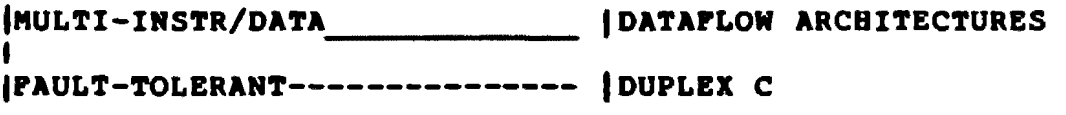
SELECTED UNIVERSITY-BASED COMPUTERS

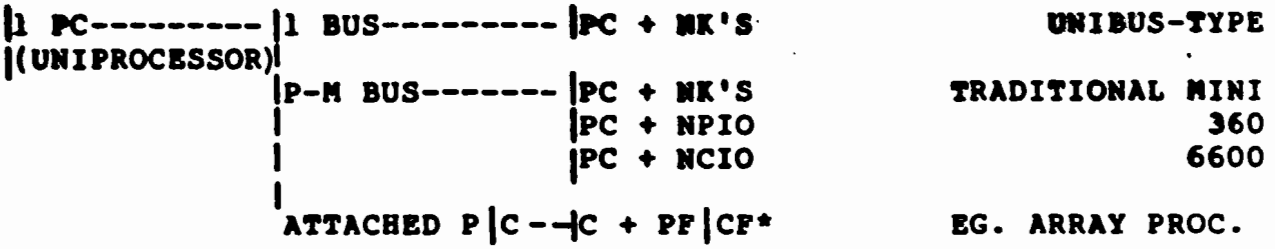
Machine	First Use	Concept-Use	Use	Use Life
Harvard Mark I - IBM ASCC	8/44	7	15	.7
IBM SSEC	1/48	-	4.5	.6
ENIAC	6/46	4	9	.7
MIT Whirlwind	6/50	5.5	9	.6
MIT/Lincoln Lab TX-0	57	3	8	.8

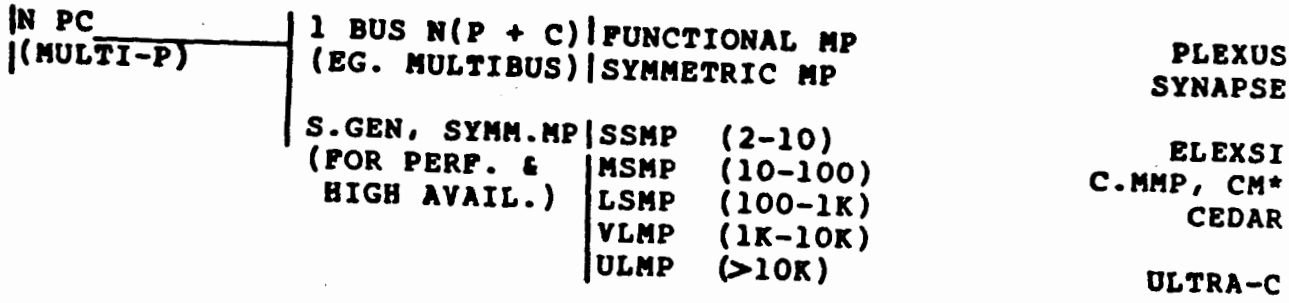
Machine	First Use	Concept-Use	Use	Use Life
ILLIAC I	9/52	4	10	.7
ILLIAC II	6/65	5.5	3	.3
ILLIAC IV	11/75	12	6.5	.3
CMU C.mmp	5/75	5	6	.7
CMU Cm*	9/76	4	>6	>.6
TEXAS TRAC	83	7	>1	>.1

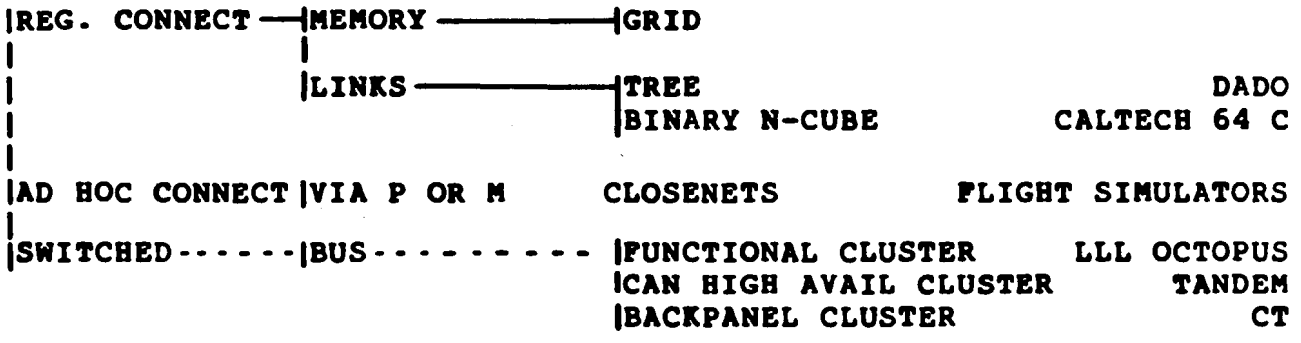
COMPUTER TYPE TAXONOMY

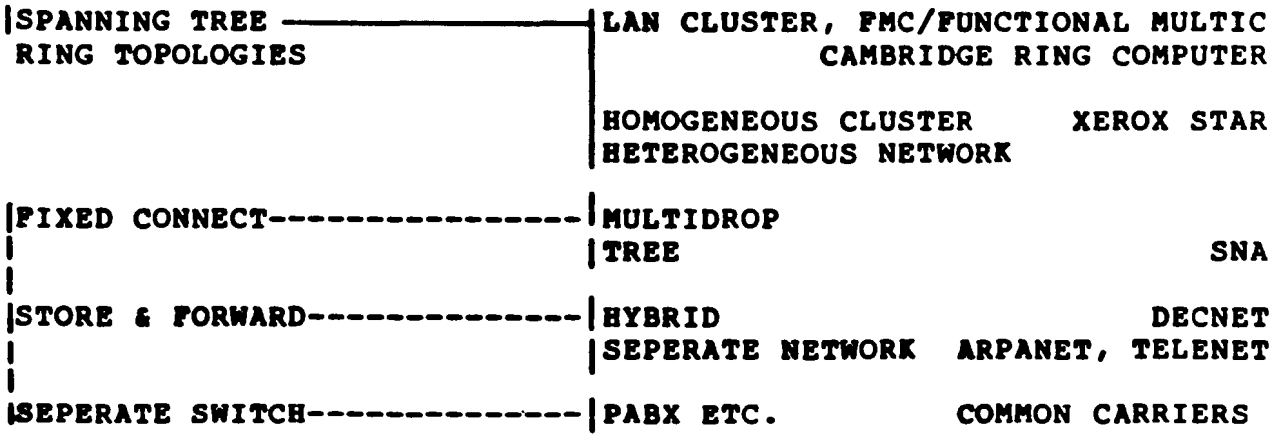



MULTI-INSTR/DATA
DATAFLOW ARCHITECTURES
FAULT-TOLERANT
DUPLEX C


1 PC
(UNIPROCESSOR)
1 BUS
PC + MK'S
UNIBUS-TYPE
P-M BUS
PC + MK'S
TRADITIONAL MINI
PC + NPIO
360
PC + NCIO
6600
ATTACHED P
C
C + PF
CF*
EG. ARRAY PROC.


N PC
(MULTI-P)
1 BUS N(P + C)
(EG. MULTIBUS)
FUNCTIONAL MP
SYMMETRIC MP
PLEXUS
SYNAPSE
S.GEN, SYMM.MP
(FOR PERF. &
HIGH AVAIL.)
SSMP (2-10)
MSMP (10-100)
LSMP (100-1K)
VLMP (1K-10K)
ULMP (>10K)
ELEXSI
C.MMP, CM*
CEDAR
ULTRA-C


REG. CONNECT
MEMORY
GRID
LINKS
TREE
BINARY N-CUBE
DADO
CALTECH 64 C
AD HOC CONNECT
VIA P OR M
CLOSENETS
FLIGHT SIMULATORS
SWITCHED
BUS
FUNCTIONAL CLUSTER
LLL OCTOPUS
CAN HIGH AVAIL CLUSTER
TANDEM
BACKPANEL CLUSTER
CT


SPANNING TREE
RING TOPOLOGIES
LAN CLUSTER, FMC/FUNCTIONAL MULTIC
CAMBRIDGE RING COMPUTER
HOMOGENEOUS CLUSTER
XEROX STAR
HETEROGENEOUS NETWORK
FIXED CONNECT
MULTIDROP
TREE
SNA
STORE & FORWARD
HYBRID
DECNET
SEPERATE NETWORK
ARPANET, TELENET
SEPERATE SWITCH
PABX ETC.
COMMON CARRIERS

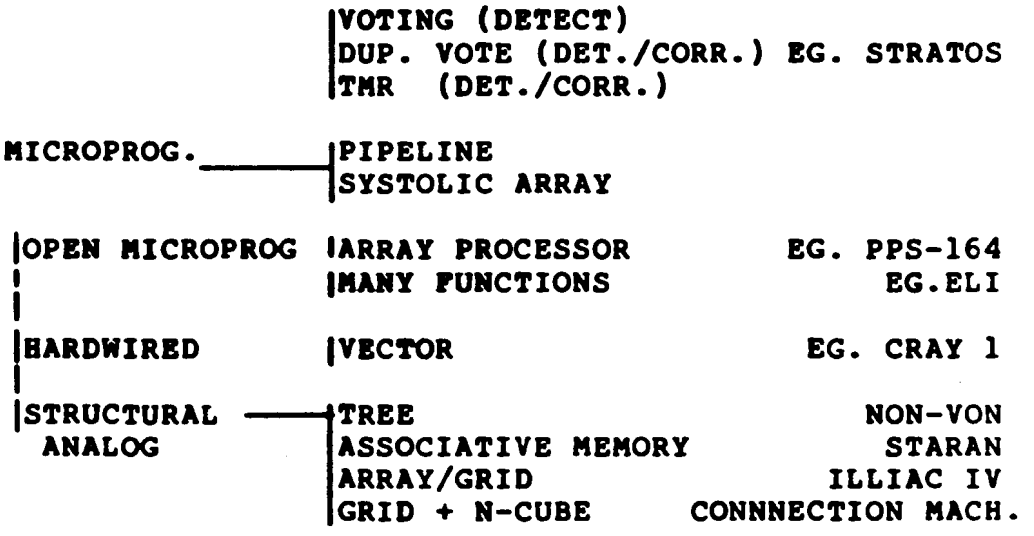
PROCESSOR-TYPE TAXONOMY

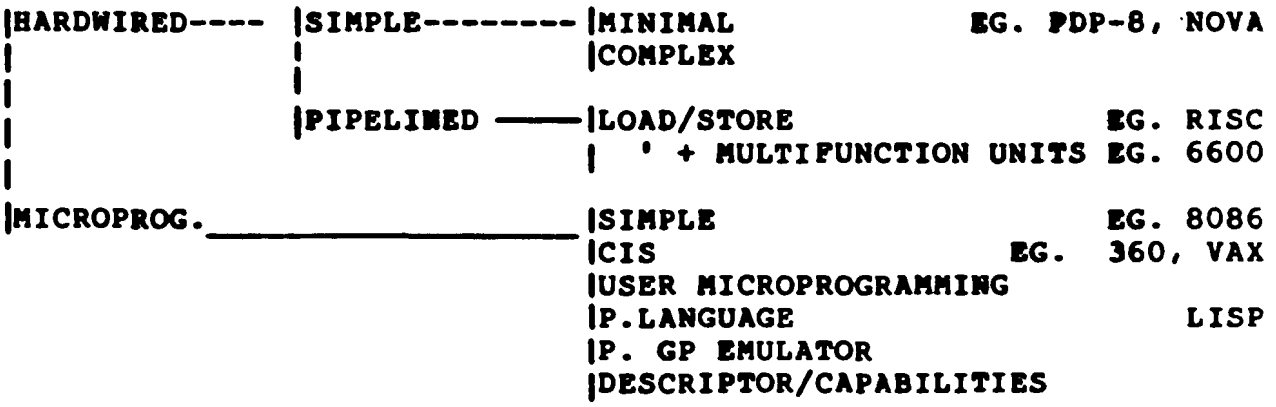
SINGLE INSTR-
SINGLE DATA

SINGLE INSTRUCTION————————————————
SINGLE DATA, HIGH AVAILABILITY

SINGLE OPER., MULTI DATA--

SINGLE INSTRUCTION,-------
MULTI-DATA


VOTING (DETECT)
DUP. VOTE (DET./CORR.) EG. STRATOS
TMR (DET./CORR.)
MICROPROG.
PIPELINE
SYSTOLIC ARRAY
OPEN MICROPROG
ARRAY PROCESSOR
EG. PPS-164
MANY FUNCTIONS
EG.ELI
HARDWIRED
VECTOR
EG. CRAY 1
STRUCTURAL ANALOG
TREE
NON-VON
ASSOCIATIVE MEMORY
STARAN
ARRAY/GRID
ILLIAC IV
GRID + N-CUBE
CONNNECTION MACH.


HARDWIRED
SIMPLE
MINIMAL
EG. PDP-8, NOVA
COMPLEX
PIPELINED
LOAD/STORE
EG. RISC
' + MULTIFUNCTION UNITS
EG. 6600
MICROPROG.
SIMPLE
EG. 8086
CIS
EG. 360, VAX
USER MICROPROGRAMMING
P.LANGUAGE
LISP
P. GP EMULATOR
DESCRIPTOR/CAPABILITIES

MINICOMPUTER COMPANY LESSONS

1. Nearly 25% survived
2. Only 8% really won
3. Only 2% of startups retained autonomy
4. Merging was tried by 10%
5. But only 1/3 of mergers were successful
6. Being a computer supplier didn't help:
   Only DEC and IBM made the transition to minis!
7. IBM always wins... eventually

(System 3... Series 1)

MINICOMPUTER TECHNOLOGY (CIRCA 1970)

Basic Industries	Minicomputer Companies
	Optional
Power Supplies	
Packaging	Essential
Core Memory	
Semiconductors (MSI)	Optional
Disks and Tapes	CPU and Memories
Terminals	Peripheral Controllers
	-
	Operating Systems
	Languages
	Applications
	System Integration

MICROCOMPUTER-BASED COMPANIES

Basic Industries	Microcomputer Companies
Power Supplies	Optional
Packaging	Optional
Semiconductors (micros, memory, peripherals)	-
CRT's and Terminals	-
Disks and Tapes	-
Board Options	Optional
UNIX & Diagnostics	Optional
Languages & Databases	Optional
LAN'S and Communication	Optional
Applications	Optional
	System Integration

MICROPROCESSOR-BASED COMPUTER PRODUCTS

On a Desk (Personal Computers)

Smart Telephones
Terminals
Home (and game)
Portable PC's
Word Processors
PC's
Workstations

SL.MI

The Desk (Departmental and Group-Level Computers)

- Micro
- Super-micro
- Clustered, functional multiprocessor
- Symmetric multiprocessor
- High-availability
  - Single computer via voting
  - Multiprocessor (n+1) redundancy
  - Multi-computer clusters

PARALLEL COMPUTING

NETWORK - WITH LAN OR WAN INTERCONECT
CLUSTER - WITH LAN INTERCONECT
FUNCTIONAL - ONE PROCESSOR PER FUNCTION
CLOSE AREA NET CLUSTER - HIGH SPEED INTERCONNECT
TIMESHARING - ONE PROCESSOR PER USER
PARTITIONED - ONE PROCESSOR PER PROCESS
TRANSACTION PROCESSING - PROCESSOR PER TRANSACTION STEP
FAULT-TOLERANT - DIFFERENT PROCESSORS ASSIGNED PER STEP WITH REDUNDANT COMPUTATION
CONCURRENT-TASK - PARALLEL PROCESSING OF A TASK BY PARTITIONING FOR INDEPENDENT DATA
PIPELINED-TASK - PARALLEL PROCESSING OF A TASK
PARALLEL PROCESSING - PROCESSORS WORK ON A SINGLE TASK

"If a computer understands English,
it must be Japanese."
-Alan Perlis

A GENERATION IS THE CONVERGENCE OF:

- NEED (EG. THREAT OF ANNIHILATION, GREED) FREEING RESOURCES
- TECHNOLOGY AND SCIENCE THAT PROVIDE FOR BUILDING MACHINES
- ORGANIZATIONS THAT BUILD NEW COMPUTING STRUCTURES

- USE TO CONFIRM A GENERATION (AFTER THE FACT).

THE FOURTH GENERATION

- EVOLUTIONARY USE BASED ON TRADITIONAL WORD AND DATA PROCESSING, MACHINE-AIDED ENGINEERING AND MANUFACTURING, AND EMBEDDED COMPUTING
- MASSIVE INTER-COMMUNICATIONS AND PRODUCTIVITY NEEDS TO INCREASE USE
- WELL-DEVELOPED TECHNOLOGIES, INCLUDING POWERFUL VLSI MICROPROCESSORS, LANS, MAGNETICS, DISPLAYS AND STANDARD SOFTWARE
- NEW ORGANIZATIONS TO BUILD NEW COMPUTER STRUCTURES, BUT
- NEW USES THAT EVOLVE WON'T BE APPARENT UNTIL A DECADE

THE NEXT GENERATION: REVOLUTIONARY VIEW

- REVOLUTIONARY USE DEPENDING ON VOICE AND NATURAL LANGUAGE COMMUNICATION
- SOPHISTICATED INTER-COMMUNICATION AND PRODUCTIVITY NEEDS INCLUDING ROBOTICS, SPEECH AND NATURAL LANGUAGE, EXPERT SYSTEMS TO HANDLE COMPLEXITY AND IMPROVE PRODUCTIVITY
- ROBOTICS, AND ARTIFICAL INTELLIGENCE, FAST-WANS TO SERVE LANS, BASED ON U- AND VLSI AND PARALLELISM TECHNOLOGIES
- AVANT GARDE ORGANIZATIONAL CO-OPERATION BETWEEN RESEARCHERS AND INDUSTRY TO PIONEER NEW COMPUTER STRUCTURES

THE NEXT GENERATION: EVOLUTIONARY VIEW

- EVOLUTIONARY USE WITH WIDESPREAD ELECTRONIC MAIL AND ELECTRONIC-BASED LOGIC TO ENCODE KNOWLEDGE (EG. CAD/CAM)
- NEED TO HAVE INFORMATION AT "FINGERTIPS" (IN THE SYSTEM AND NOT IN PAPERS AND BOOKS)
- EVOLUTIONARY TECHNOLOGY WITH LARGER, DISTRIBUTED MEMORIES
- NEW COMPANIES TO BUILD WITH EVOLVING TECHNOLOGIES

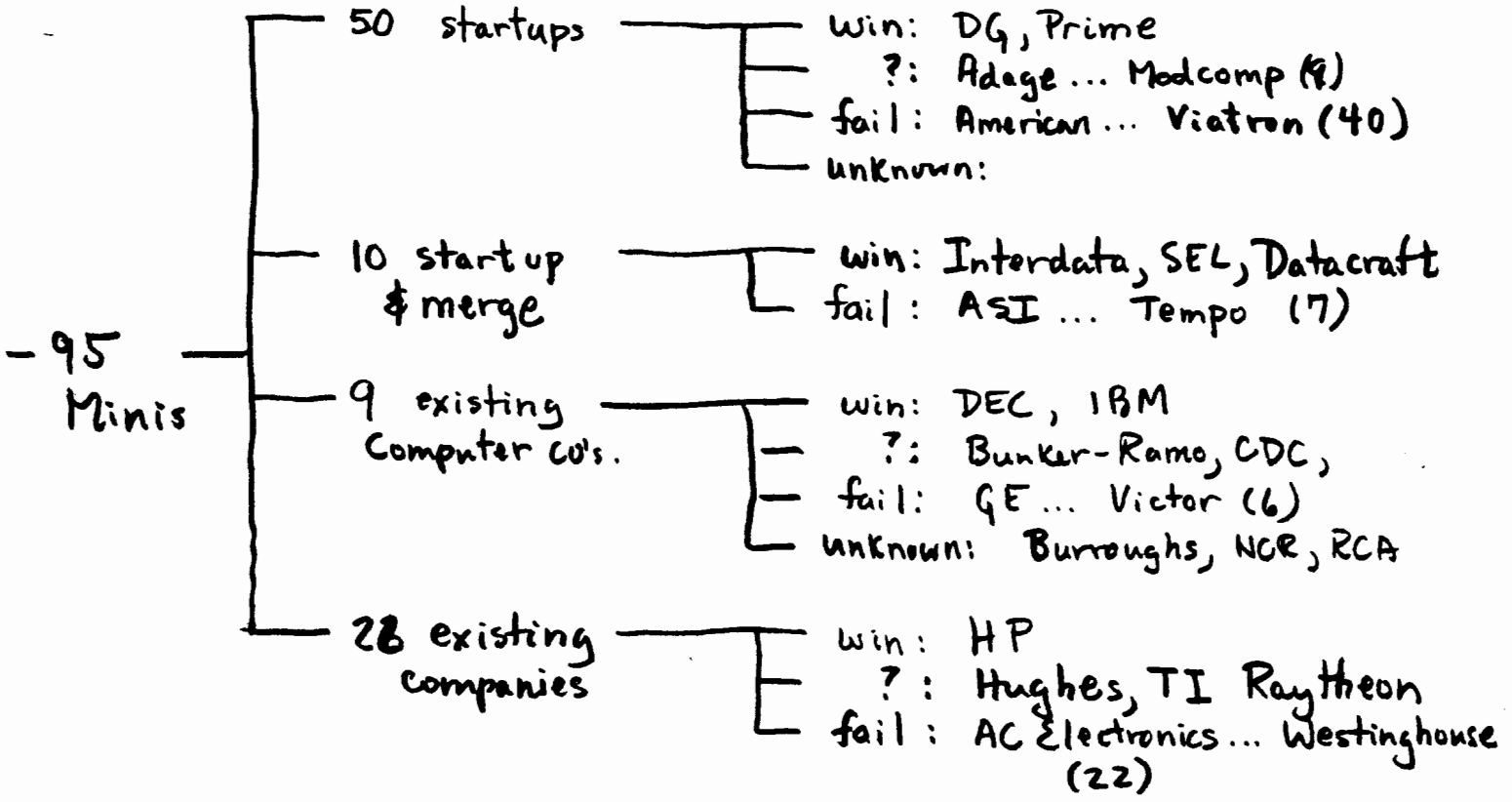
Two Slides

Selected University-Based Computers

Machine	First Use	Concept-Product-Use	Use	Use to Obsol. Life	Results (in addition to engineering and scientific training)
Harvard MarkI = IBM ASCC	8/44	7	5	15	.7	Use.
IBM SSEC	1/48	-	2.5	4.5	.6	Use,
ENIAC	6/46	4	3	9	.7	Use. stored program, Electronic Computer
MIT Whirlwind	6/50	5.5	3.5	9	.6	Use, circuits, core memory, real time and interactive computation, proto for SAGe system
ILLIAC I	9/52	4	3	10	.7	Use, proto for 6 others
MIT/Lincoln Lab TX-0	57	3	2	8	.8	Use, transistor circuits, large core memory
ILLIAC II	6/63	5.5	2	3	.3	Asynchronous logic, design too conservative
ILLIAC IV	11/75	12	8.5~10.5	6.5	.3	Use, parallelism (algorithms), accelerate bipolar memory develop. stimulated competitive approaches
CMU C.mmp	5/75	5	4.5	6	.7	Parallelism, Intel 432 proto
CMU Cm*	9/76	4	2	>6	>.6	Parallelism, Multibus-type structures.
TEXAS TRAC	83	7	5	>1	>.1	-

TA-CH
1/4/84

Table of U.S. Minicomputer Companies (Circa 1970)



extra shots to show BOLDED text.

PARALLEL COMPUTING

NETWORK - with LAN or WAN interconect
CLUSTER - with LAN interconect
FUNCTIONAL - one processor per function
CLOSE AREA NET CLUSTER - high speed interconnect
TIMESHARING - one processor per user
PARTITIONED - one processor per process
TRANSACTION PROCESSING - processor per transaction step
FAULT-TOLERANT - different processors assigned per step with redundant computation
CONCURRENT-TASK - parallel processing of a task by partitioning for independent data
PIPELINED-TASK - parallel processing of a task
PARALLEL PROCESSING - processors work on a single task

"If a computer understands English,
it must be Japanese."
-Alan Perlis

THE FOURTH GENERATION

- **Evolutionary use** based on traditional word and data processing, machine-aided engineering and manufacturing, and embedded computing
- **massive inter-communications** and **productivity needs** to increase use
- **well-developed technologies,** including powerful VLSI microprocessors, LANs, magnetics, displays and standard software
- **new organizations** to build new computer structures, but

- **new uses** that evolve from greater access won't be apparent for at least a decade

---

THE NEXT GENERATION: REVOLUTIONARY VIEW

- **Revolutionary use** depending on voice and natural language communication
- **sophisticated inter-communication and productivity needs** including robotics, speech and natural language, expert systems to handle complexity and improve productivity
- **robotics,** and **artifical intelligence,** fast-WANs to serve LANs, based on **U- and VLSI and parallelism** technologies
- **avant garde organizational co-operation between researchers and industry** to pioneer new computer structures

THE NEXT GENERATION: EVOLUTIONARY VIEW

- **Evolutionary use** with widespread **electronic mail** and **electronic-based logic** to encode knowledge (eg. CAD/CAM)
- **need to have information at "fingertips"** (in the system and not in papers and books)
- **evolutionary technology** with larger, distributed memories
- **new companies** to build with evolving technologies

A **GENERATION** is the convergence of:

- **need** (eg. threat of annihilation, greed) freeing resources
- **technology and science** that provide for building machines
- **organizations** that build new **computing structures**

- **use** to confirm a generation (after the fact).

PARALLEL COMPUTING

NETWORK - with LAN or WAN interconect
CLUSTER - with LAN interconect
FUNCTIONAL - one processor per function
CLOSE AREA NET CLUSTER - high speed interconnect
TIMESHARING - one processor per user
PARTITIONED - one processor per process
TRANSACTION PROCESSING - processor per transaction step
FAULT-TOLERANT - different processors assigned per step with redundant computation
CONCURRENT-TASK - parallel processing of a task by partitioning for independent data
PIPELINED-TASK - parallel processing of a task
PARALLEL PROCESSING - processors work on a single task

"If a computer understands English,
it must be Japanese."
-Alan Perlis

THE FOURTH GENERATION

- **Evolutionary use** based on traditional word and data processing, machine-aided engineering and manufacturing, and embedded computing
- **massive inter-communications** and **productivity needs** to increase use
- **well-developed technologies,** including powerful VLSI microprocessors, LANs, magnetics, displays and standard software
- **new organizations** to build new computer structures, but

- **new uses** that evolve from greater access won't be apparent for at least a decade

---

THE NEXT GENERATION: REVOLUTIONARY VIEW

- Revolutionary use depending on voice and natural language communication
- sophisticated inter-communication and productivity needs including robotics, speech and natural language,
expert systems to handle complexity and improve productivity
- robotics, and artifical intelligence,
fast-WANs to serve LANs,
based on U- and VLSI and parallelism technologies
- avant garde organizational co-operation
between researchers and industry to pioneer new computer structures

---

THE NEXT GENERATION: EVOLUTIONARY VIEW

- Evolutionary use with widespread electronic mail and electronic-based logic to encode knowledge (eg. CAD/CAM)
- need to have information at "fingertips" (in the system and not in papers and books)
- evolutionary technology with larger, distributed memories
- new companies to build with evolving technologies

A GENERATION is the convergence of:

- need (eg. threat of annihilation, greed) freeing resources
- technology and science that provide for building machines
- organizations that build new computing structures

- use to confirm a generation (after the fact).

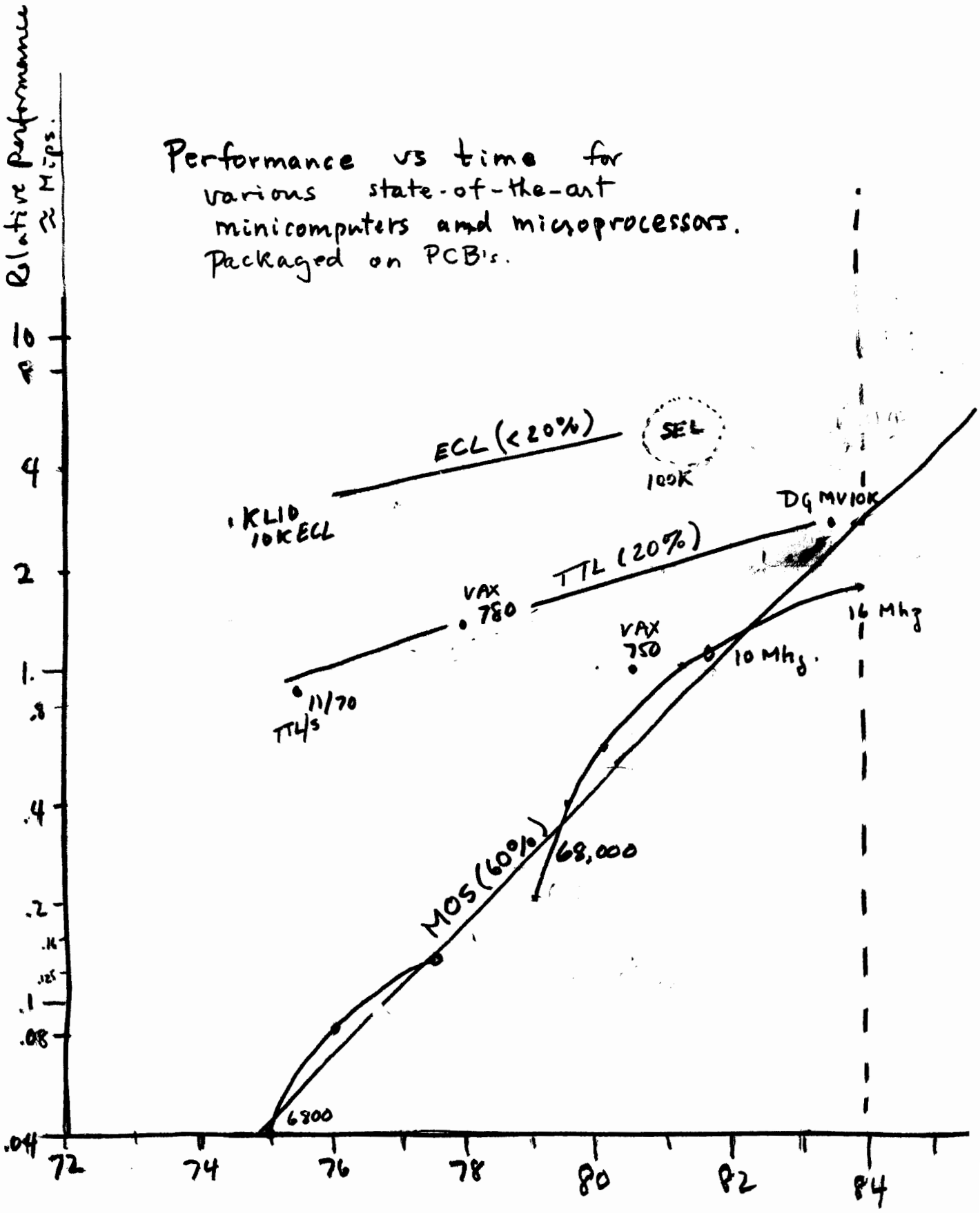
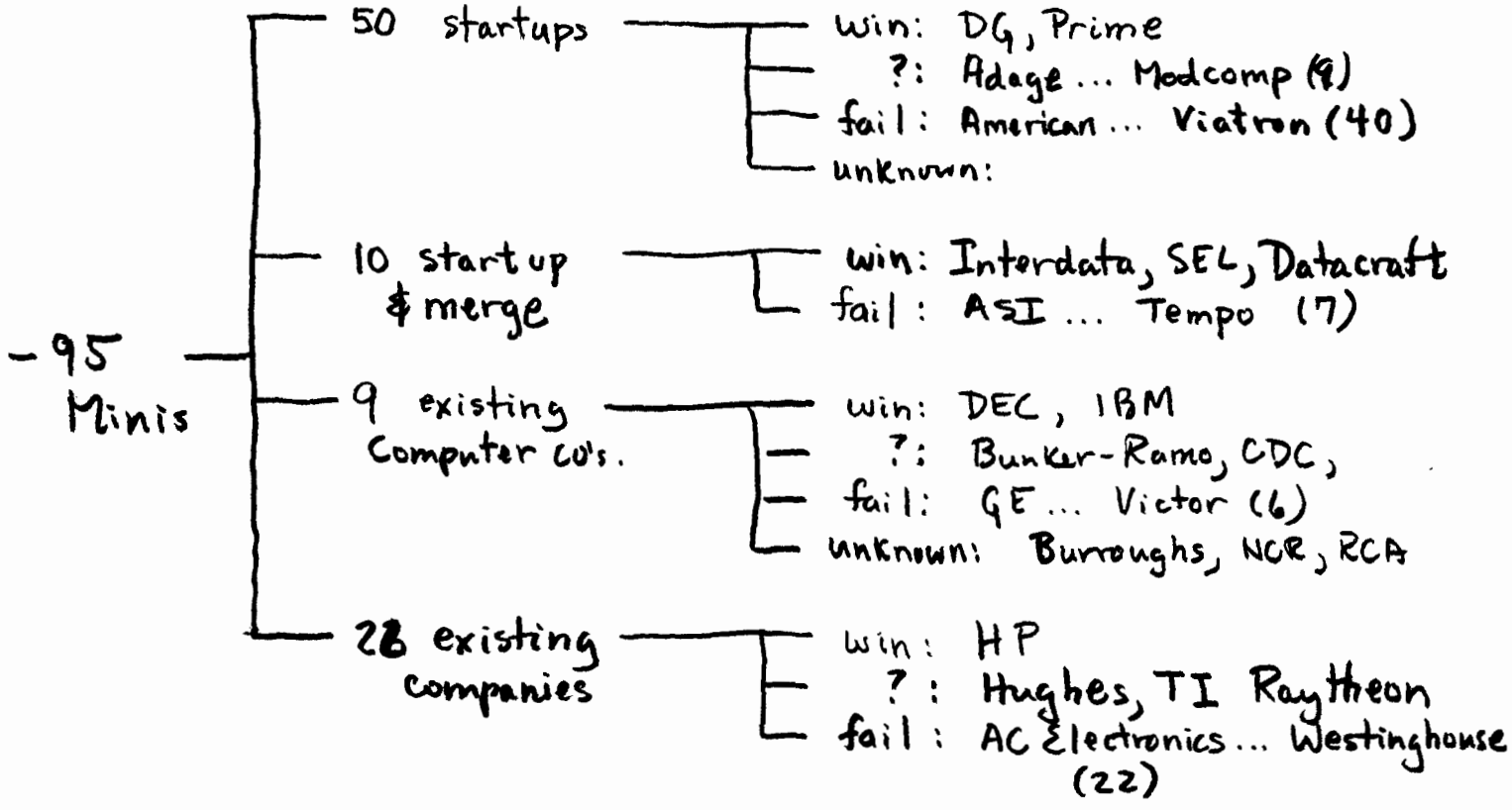

Performance vs time for various state-of-the-art minicomputers and microprocessors. Packaged on PCB's.
Relative Performance
≈ M.I.P.S.
10
4
2
1.
.8
.4
.2
.1
.08
.04
72
74
76
78
80
82
84
ECL (<20%)
SEL
100K
KL10
10K ECL
DG MV10K
TTL (20%)
VAX
780
VAX
750
11/70
TTL's
16 Mhz
10 Mhz
MOS (60%)
68,000
6800

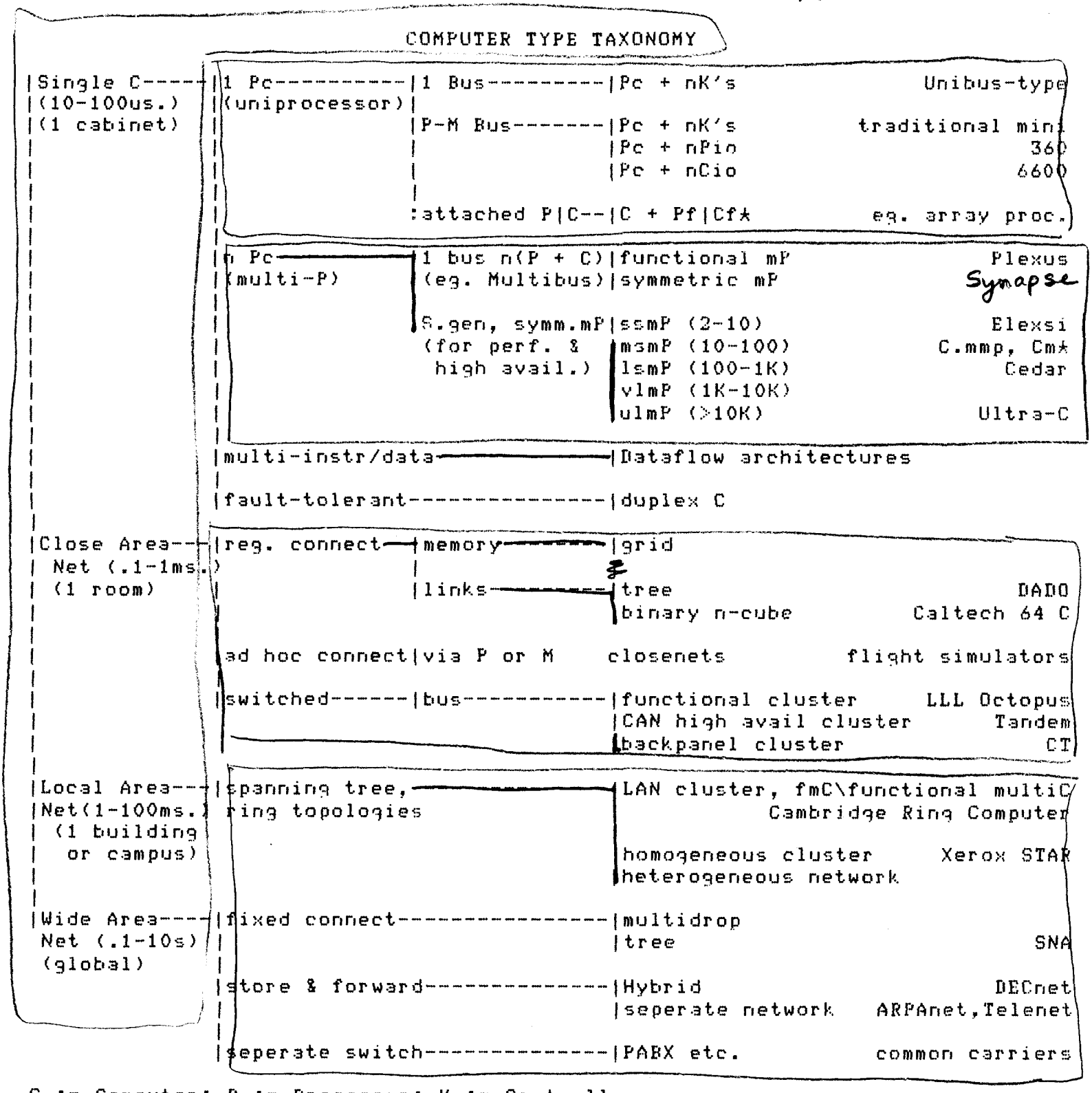
Table of U.S. Minicomputer Companies (Circa 1970)



5 slides

The pen drawn lines should be different than the others.

COMPUTER TYPE TAXONOMY

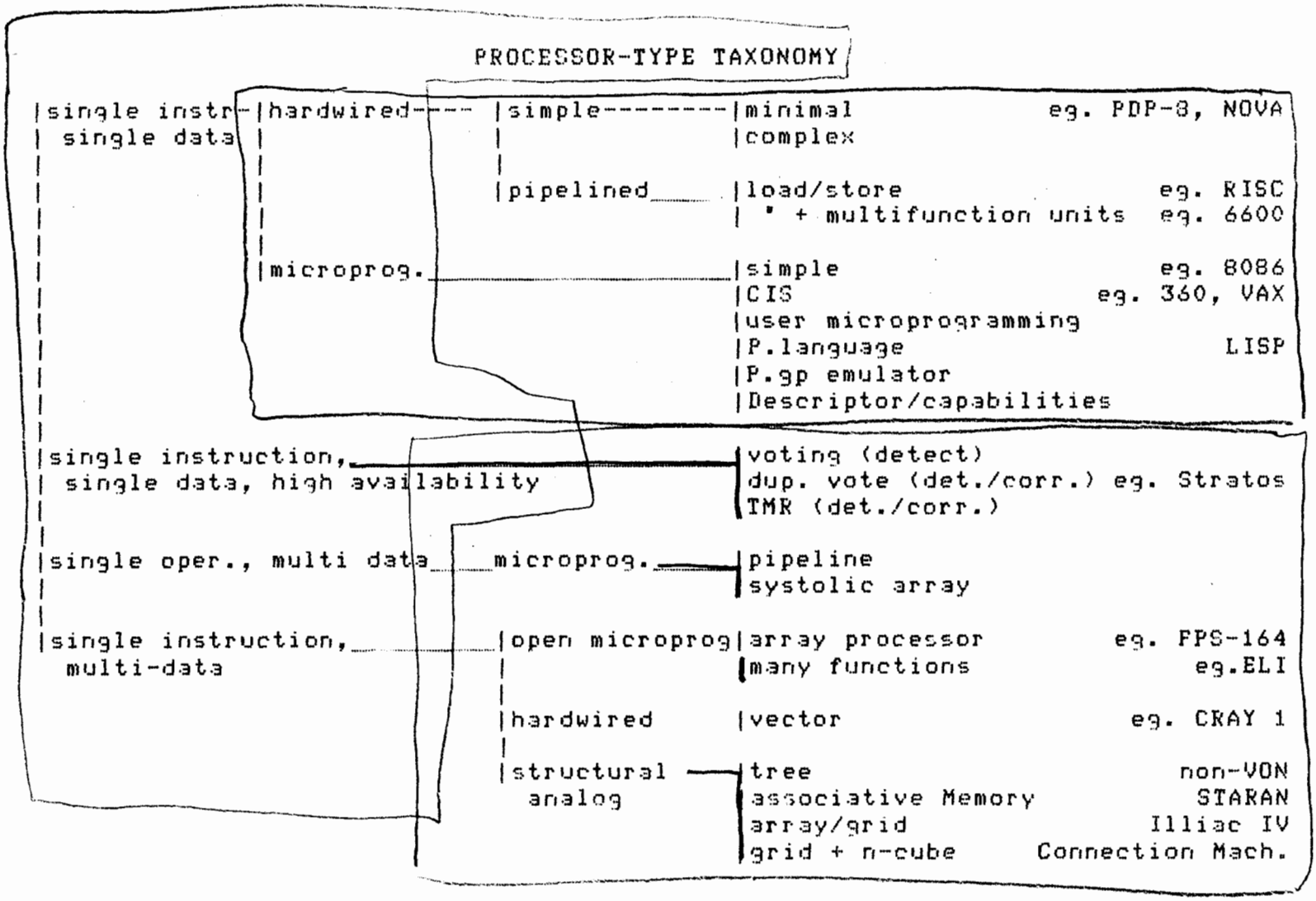


C := Computer; P := Processor; K := Controller
Cluster := collection of C's acting as a single C
(interprocessor communication times) determine parallel processing grain
*function := arithmetic, array processor, signal processor, communication (front end), database (back end), display, simulation

gBell
1/8/84

3 slides

PROCESSOR-TYPE TAXONOMY



GBell
1/8/84

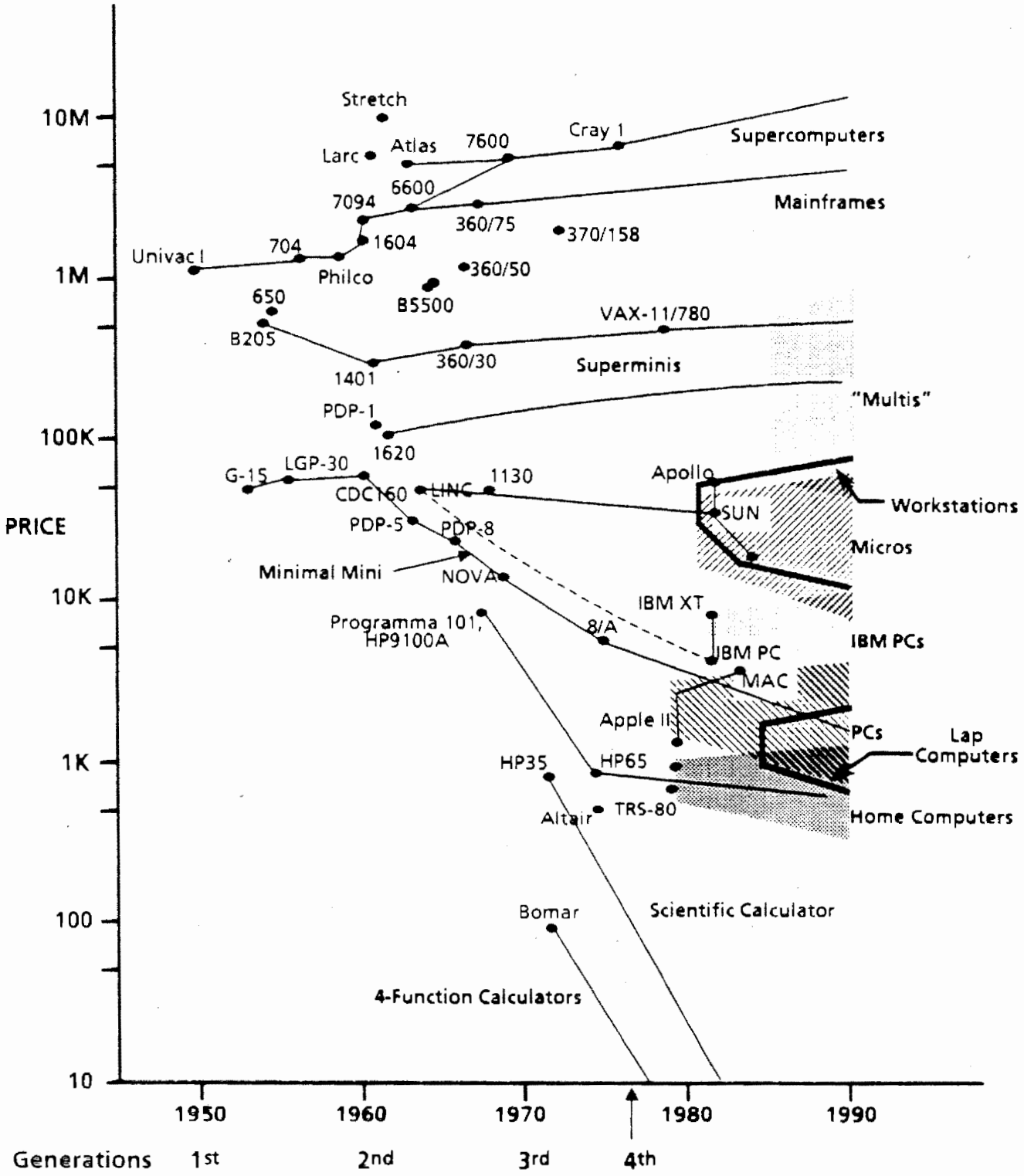
Two Slides

Selected University-Based Computers

Machine	First Use	Concept-Use	Project-Use	Use	Use Life	Results (in addition to engineering and scientific training)
Harvard MarkI = IBM ASCC	8/44	7	5	15	.7	Use,
IBM SSEC	1/48	-	2.5	4.5	.6	Use,
ENIAC	6/46	4	3	9	.7	Use, stored program, Electronic Computer
MIT Whirlwind	6/50	5.5	3.5	9	.6	Use, circuits, core memory, real time and interactive computation, proto for SAGe system
ILLIAC I	9/52	4	3	10	.7	Use, proto for 6 others
MIT/Lincoln Lab TX-0	5/57	3	2	8	.8	Use, transistor circuits, large core memory
ILLIAC II	6/63	5.5	2	3	.3	Asynchronous logic design too conservative
ILLIAC IV	11/75	12	8.5-10.5	6.5	.3	Use, Parallelism (algorithms), accelerate bipolar memory develop, stimulated competitive approaches
CMU C.mmp	5/75	5	4.5	6	.7	Parallelism, Intel 432 proto
CMU Cm*	9/76	4	2	>6	>.6	Parallelism, Multibus-type structures,
TEXAS TRAC	83	7	5	>1	>.1	-

1/4/84

Computer System Price Classes versus Time



DEPARTMENTAL AND GROUP-LEVEL COMPUTERS

MICRO — Corvus.

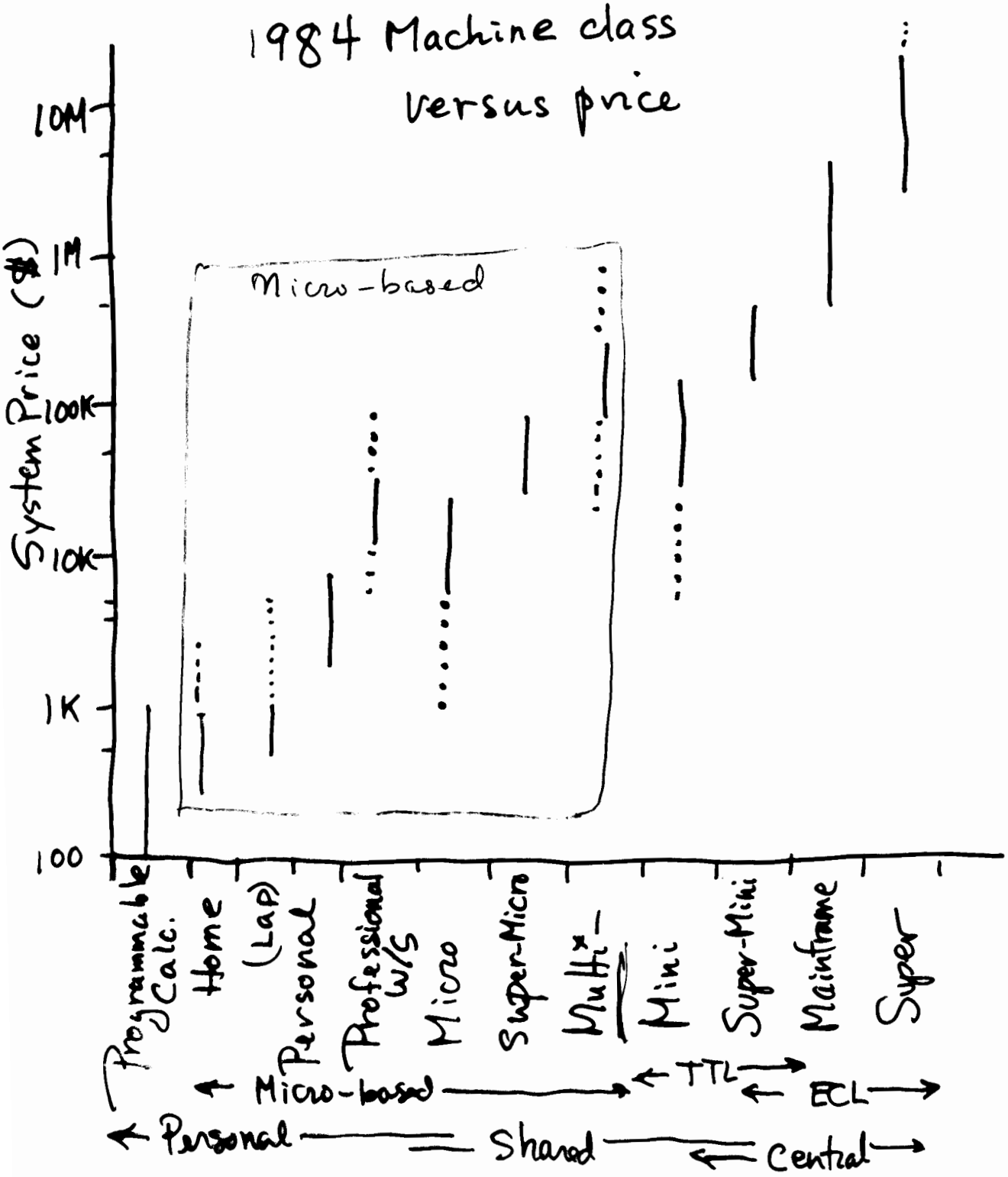
SUPER-MICRO — Angle M - CRDS

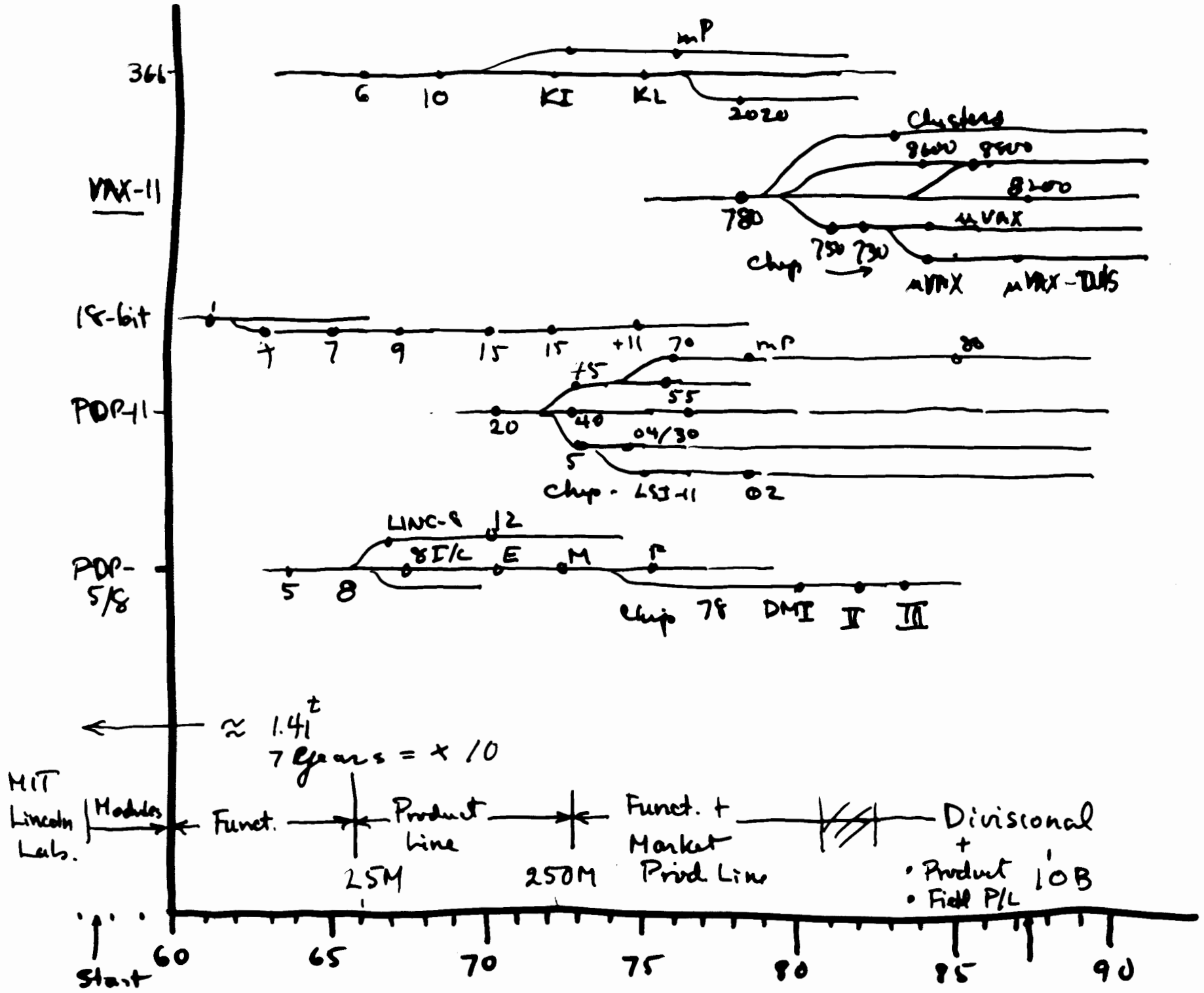
CLUSTERED. FUNCTIONAL MULTIPROCESSOR — Plexus.

SYMMETRIC MULTIPROCESSOR

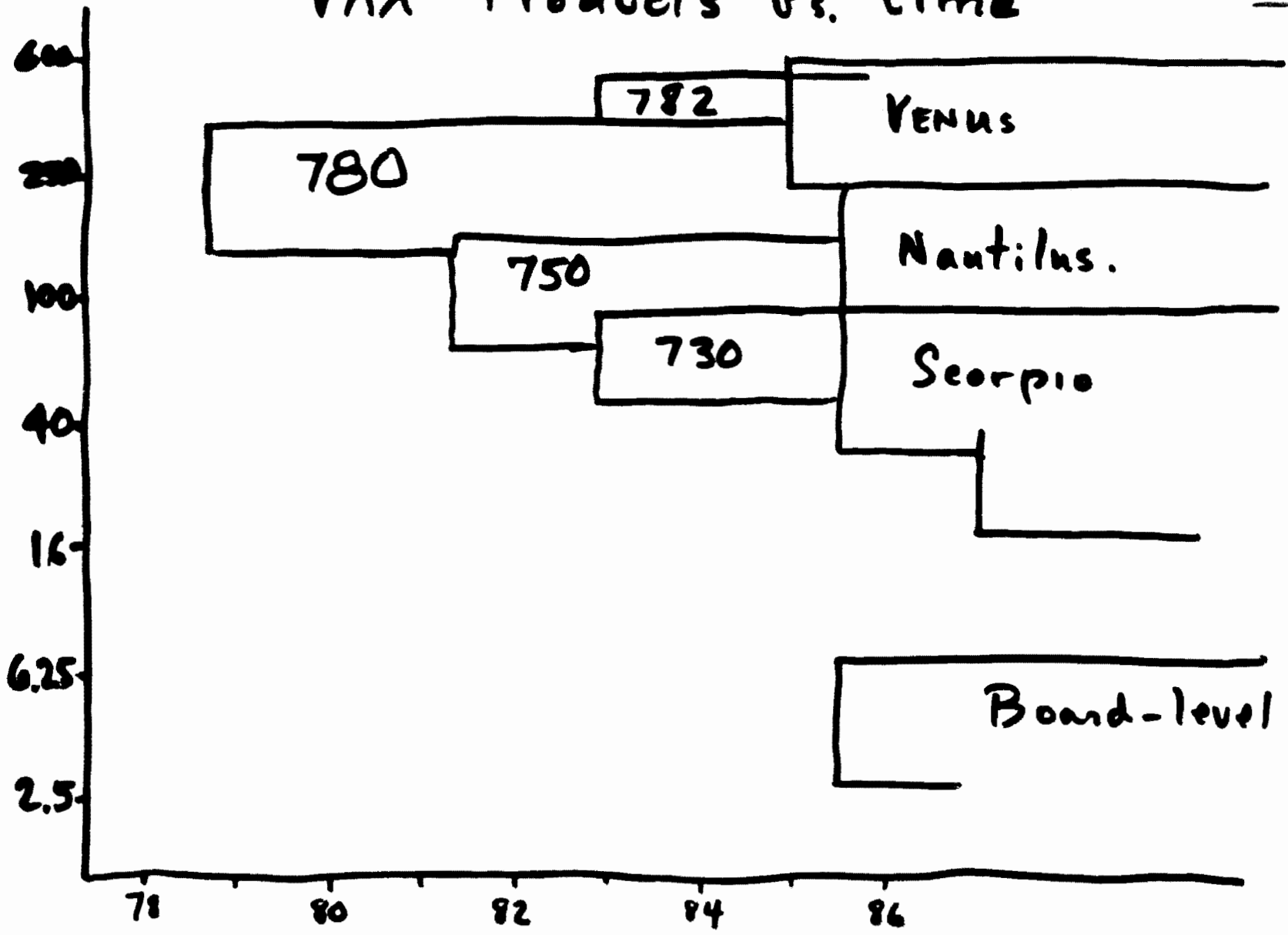
HIGH-AVAILABILITY

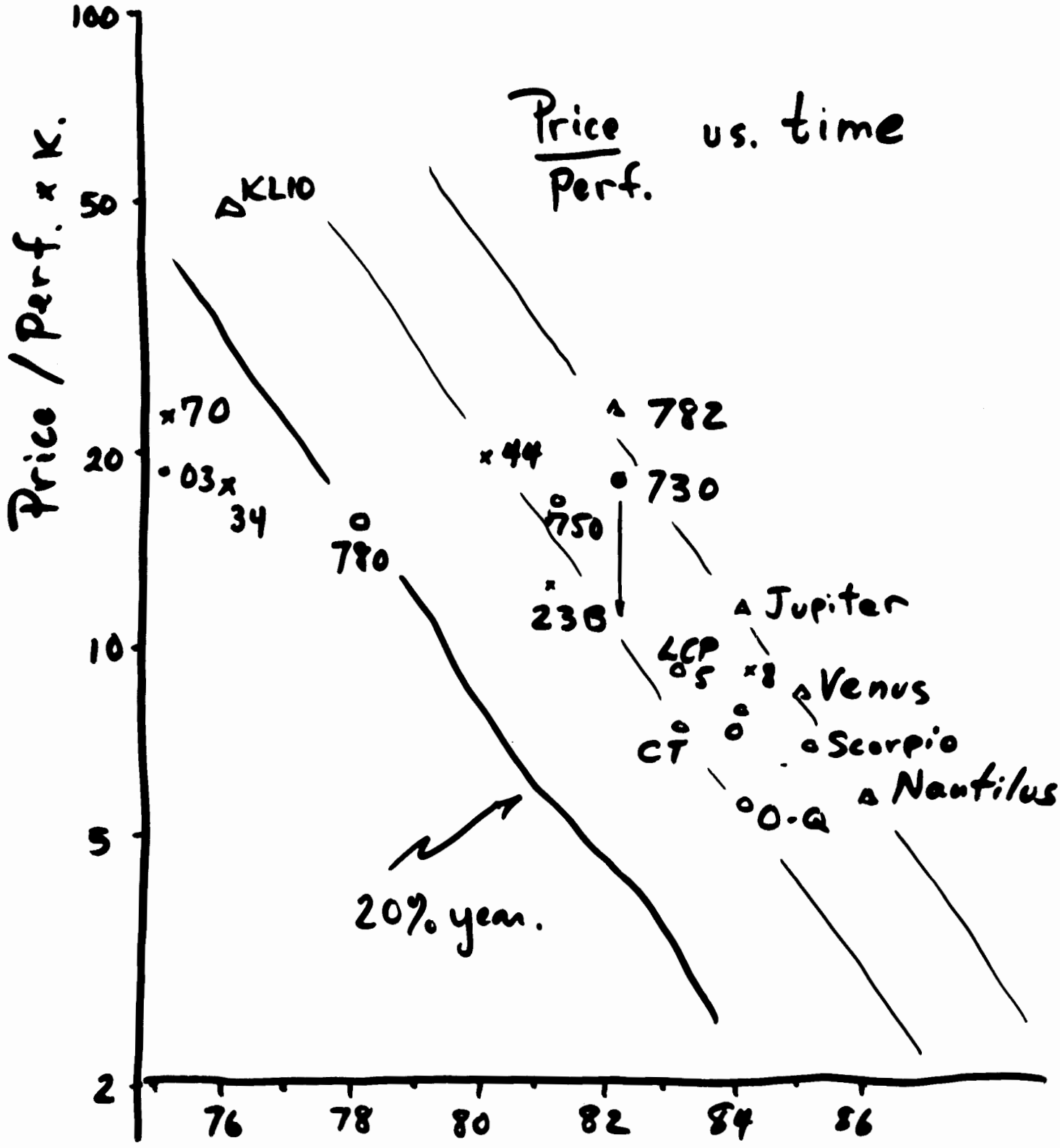
- SINGLE COMPUTER VIA VOTING
- MULTIPROCESSOR (N+1) REDUNDANCY
- MULTI-COMPUTER CLUSTERS


1984 Machine class versus price
System Price ($)
10M
1M
100K
10K
1K
100
Micro-based
Programmable Calc.
Home
(Lap) Personal
Professional W/S
Micro
Super-Micro
Multi-
Mini
Super-Mini
Mainframe
Super
← Micro-based
TTL
ECL
← Personal
Shared
Central


mP
360
6
10
KI
KL
2020
Clusters
8600
8500
8200
VAX-11
780
µVAX
Chip
750
730
µVAX
µVAX-DUS
16-bit
4
7
9
15
15
+11
70
mP
80
75
55
PDP-11
20
40
04/30
5
Chip - LSI-11
02
LINC-8
12
8I/C
E
M
F
PDP-5/8
5
8
Chip
78
DMI
II
III
≈ 1.41^t
7 years = x 10
MIT Lincoln Labs.
Modules
Funct.
Product Line
Funct. + Market Prod Line
Divisional + • Product • Field P/L
25M
250M
1 OB
Start
60
65
70
75
80
85
90

VAX Products vs. time




Price / Perf. x K.
100
50
20
10
5
2
76
78
80
82
84
86
Price / Perf. us. time
KL10
x70
•03
x34
780
x44
782
730
750
238
Jupiter
LCP
05
x8
Venus
CT
Scorpio
Nautilus
O-Q
20% year.

VAX-11

GENERAL GOALS/CONSTRAINTS

GO.1 MINIMIZE MP.SIZE (PROGRAMS) BY ENCODING & OPERATIONS (BIND IN HARDWARE)

[VAX ISP SHOULD HAVE $\leq$ MP.SIZE (OF PDP-11) WHILE PROVIDING 32-BIT VIRTUAL ADDRESS)

GO.2 MINIMIZE PROCESSING TIME FOR COMMON FUNCTION (E.G. MEMORY MANAGEMENT, PROCEDURE CALL, CONTEXT SWITCH)

GO.3 MINIMIZE COST OF EXTENSIONS

GO.4 BUILD GENERAL VS. SPECIFIC MECHANISMS

GO.5 MINIMUM PROGRAMMING TIME

GO.6 PROVIDE A MACHINE IN WHICH THERE IS MORE PROGRAM SHARING THAN WITH ANY OTHER MACHINE

G.BELL
4/28/75

VAX Design Goals & Constraints

1. Maximal compatibility with PDP-11 (given significant extension of virtual address space)

2. High bit efficiency

3. Easy exploitation of instruction set by HLL processors

4. System level architecture tailored to needs of planned O/S

5. Extensibility

6. Range

> Program sharing among all languages

INSTRUCTION FORMAT DESIGN CRITERIA

1. ALL OPERATORS SHOULD HAVE THE "NATURAL" NUMBER OF OPERANDS

2. ALL OPERANDS SHOULD HAVE THE SAME SPECIFICATION GENERALITY

3. ADDRESSING MODES SHOULD REFLECT MEASURED PROGRAM BEHAVIOR DATA:

    A. LITERALS SHORT

    B. DISPLACEMENTS SHORT

    C. TRUE INDEXING NEEDED

OPERATOR SET DESIGN CRITERIA

1. REGULAR AND CONSISTENT TREATMENT

   OF OPERATORS ACROSS DATA TYPES.

2. AVOIDANCE OF INSTRUCTIONS UNLIKELY

   TO BE GENERATED BY A COMPILER

3. INCLUSION OF SEVERAL FORMS OF

   COMMON OPERATORS; E.G.

INCL	A	A = A + 1
ADDL2	A,B	B = A + B(I)
ADDL3	A,B,C	C = A + B

4. REPLACEMENT OF COMMON INSTRUCTION SEQUENCES

   WITH SINGLE INSTRUCTIONS :

   E.G. LOOP CONTROL, PROCEDURE CALLING,

   SUBSCRIPT CALCULATION

USER-LEVEL COMPATIBILITY

C8 NO APPARENT CUSTOMER TRAINING FOR 11VAX.

Constant ← RSX-11/M.

G9 RUN 16 BIT USER MODE MACHINES DEFINED BY OPERATING SYSTEMS (E.G. RSX-11) INTERFACE.

G10 THE 11VAX USER MODE ENVIRONMENT WILL BE A PROPER SUBSET, ALBEIT ONE WHICH REQUIRES REASSEMBLY OF THE 11, 16-BIT USER MODE INTERFACE.

G11 THE SYSTEM SOFTWARE WILL SUPPORT EXISTING TASKS WITH NEW (OR MODIFIED) TASKS WHICH USE EXTENDED ADDRESSING AND OTHER NEW FEATURES.

C12 HARDWARE PERIPHERAL COMPATIBILITY WITH CURRENT 11'S. — Unibus

G12 MINIMIZE EXCLUDED HARDWARE FEATURES.

G.Bell
4/28/75

MARKET SPECIFIC ENVIRONMENT GOALS/CONSTRAINTS

G5 SIGNIFICANTLY IMPROVE REAL TIME RESPONSE.

G6 ENHANCE MACHINE ISP FOR OUR VARIED MARKETS.

G7 IMPROVE RAS OVER CURRENT STRUCTURES.

RAM → Rel., Avail, Maint.

G.Bell
4/28/75

11 VAX ARCHITECTURE GOALS/CONSTRAINTS

C1 EXTEND THE USER VA TO AT LEAST 24-BITS

G2 LONG LIFE EXPECTANCY, WITH AN IMPLEMENTATION NOW AND IN 1980

G3 COMPATIBILITY ACROSS A RANGE OF 1000:1.

G4 PROGRAMS WRITTEN ON A LARGE MEMORY MACHINE SHALL RUN ON SMALL MEMORY MACHINES PROVIDED THE OPTIONS AND FILE SPACE ARE ADEQUATE... AND VICE VERSA.

G.Bell
4/28/75

DEC INTERNAL GOALS/CONSTRAINTS

G13 EXISTING PRIVILEGED PROGRAMS (OPERATING SYSTEMS) SHOULD RUN WITH MINIMAL MODIFICATIONS.

NG14 EXISTING OPERATING SYSTEMS WILL BE RECODED TO PROVIDE ONLY 11 (16-BIT) USER MODE ENVIRONMENT.

G15 PHASEOVER FROM 11 TO 11VAX MUST BE MINIMIZED.

G16 MAXIMIZE THE RUNNABLE DIAGNOSTICS WITH NO REASSEMBLY.

G.Bell
4/28/75

Ken + rat ✓ The Museum's organized in 2 ways:
+ extra copy
· time (Table 1.4)
· a taxonomy of information processing elements (Table 2).
It goes from class to specie.

TABLE 1. THE GENERATIONS

note 2 classes (memory + Calculators) are broken down.
Gozinta

PRE-COMPUTER GENERATIONS

TECHNOLOGY	MANUAL	CRAFT 1620	MECHANICAL 1810	ELECTRO-MECHANICAL 1900
MACHINE	ABACUS	TABLES GUNTER'S RULE	PLANIMETER JACQUARD LOOM	HOLLERITH CENSUS MACHINE, FRIDEN CALCULATOR
NEED	TAXES	TRADE EXPLORATION	INDUSTRIAL LAND DIVISION	CENSUS BUSINESS
USE	COUNTING	ARITHMETIC NAVIGATION	SURVEYING WEAVING	SORTING ACCOUNTING

COMPUTER GENERATIONS

TECHNOLOGY	ELECTRONIC 1950	TRANSISTOR 1960
MACHINES	WHIRLWIND UNIVAC 1 ERA 1101	CDC 160, IBM 7090, IBM 1401 PDP-1
NEED	DEFENSE WEATHER PREDICTION	SPACE SCIENCE
USE	FIRING TABLES WEATHER FORECASTING MANAGEMENT	SIMULATION TRAINING PROGRAMMERS ACCOUNTING

DCM004.58

TABLE 2. COMPARISON OF MUSEUM TAXONOMY AND PMS

MUSEUM TAXONOMY CLASS - CODE	CODE - PMS
MEMORIES - M	M - MEMORIES
CONTROLS - K	K - CONTROLS
TRANSDUCERS - T	T - TRANSDUCERS
LINKS & SWITCHES - S	S - SWITCHES
	L - LINKS
CALCULATORS - D	D - DATA OPERATION
	P - PROCESSOR
DIGITAL COMPUTER - C	C - COMPUTER
ROBOTICS - R	

TABLE 3. (IN PROCESS)

CRITERIA USED IN DIFFERENTIATING ORDERS, FAMILIES, AND GENUS.

CLASS	ORDER (TECHNOLOGY)	FAMILY	GENUS
MEMORY	MACHINE INTERFACE	STORAGE MATERIAL	STRUCTURE OF ACCESS MOVEMENT
CONTROLS	*	DEGREE OF COMPLEXITY	*
TRANSDUCERS	*	PHENOMENA/MATERIAL	*
LINKS & SWITCHES	*	DEGREE OF COMPLEXITY	*
CALCULA	ANALOG OR DIGITAL	DEGREE OF COMPLEXITY	STRUCTURE
DIGITAL COMPUTERS	*	*	*
ROBOTICS	*	*	*

* - TO BE DETERMINED.

CLASS CALCULATOR

ORDER	FAMILY -COMPLEXITY	GENUS -STRUCTURE	SPECIES
ANALOG	SINGLE PART	DRAWING INSTRUMENTS	PROTRACTOR, PEN ETC.
	2-3 PART	FIXED RULE	PROPORTIONAL RULES
		GUNTER RULE	GUNTER RULE
		SECTOR	SECTORS
		SLIDE RULE	STRAIGHT, CIRCULAR,
		SPIRAL, LOG-LOG	
		LEVEL REFERENCE	GUNNERY LEVEL
		INTEGRATOR	MILEAGE READER
	MULTIPLE PART	DRAWING INSTRUMENTS	PANTOGRAPH
		LEVEL REFERENCE	QUADRANT, SEXTANT ETC
		INTEGRATOR	PLANIMETER, ETC.
	COMPLEX	LEVEL REFERENCE	AUTO-PILOT
		EQUATION SOLVER	HARMONIC ANALYZER ETC
			TIDE PREDICTOR, ETC
	PROGRAMMABLE	DIFF. ANALYZER	BUSH, HARTREE
		ANALOG COMPUTER	GENL PRECISION, ETC.

Class Calculator

DIGITAL	SINGLE REGISTER	STONE, BEAD	COUNTING TABLE, ABACUS, SOROBAN, ETC
		PASCAL WHEEL	PASCAL WHEEL, STRIP, KEYED WHEEL "COMPTOMETER"
	TWO REGISTER	TAB INDICATOR KEYED WHEELS	BURROUGHS
	3-4 REGISTER	STEPPED WHEEL	LEIBNIZ, ARITHMOMETERS AUTOMATIC STEPPED WHEEL
		ROTARY	BALDWIN, ODHNER, CURTA, ETC.
		MOTOR-DRIVEN WH. BATTERY ELECTRONIC	MONROE, FRIDEN ETC "POCKET" CALCS.
	COMPLEX	TABULATOR	HOLLERITH CENSUS, POWERS-SAMAS
		EQUATION-SOLVER	ABC MACHINE, POCKET CALCULATORS,
		RELAY CALCULATORS	BELL LABS I DIFFERENCE ENGINES
	PROGRAMMABLE	RELAY CALCULATORS	BELL LABS II-IV, Z3-4
		ANALYTIC ENGINE	BABBAGE, HARVARD MKS
		TABULATOR	HOLLERITH, POWERS, ETC
		PLUG-BOARD	ENIAC
		BATTERY ELECTRONIC	POCKET

CLASS MEMORY

ORDER -INTERFACE	FAMILY -TECHNOLOGY	GENUS -STRUCTURE OF ACCESS	SPECIES
NON-MECH.	PHYSICAL STATE	FIXED-PERMANENT	STONE MARKS, NAPIERS
		FIXED-ERASABLE	QUIPU, BEADS, ABACUS
WRITABLE OR READABLE	PAPER	FIXED	
		LINEAR	SCROLL
		CYCLIC	ROLODEX
		RANDOM	BOOK
	MECH. STABLE	FIXED	SWITCHES
		LINEAR	PIANO ROLL
		CYCLIC	DRUM, DISK
		RANDOM	CARD
			MOVABLE NOMOGRAPH
	CHEM. STABLE	LINEAR	MICROFILM
		RANDOM	MICROFICHE, VIDEODISC
	MAGNETIC	RANDOM	ROPE
	ELECTRIC CHARGE	RANDOM	CAPACITOR
	ELECTRONIC	RANDOM	DIODE, SEMICON. ROM

CCars Mem...

WRITABLE & READABLE	MECH. STABLE	FIXED	CALCULATOR REGISTERS
		RANDOM	ZUSE MEMORY
	WAVE STORAGE	CYCLIC	MERCURY, OPTICAL, & MAGNETO-STRICTIVE
	ELECTRIC CHARGE	CYCLIC	ATANASOFF DRUM
		RANDOM	WILLIAMS TUBE, SELECTRON CAPACITOR, SEMICOND.
	MAGNETIC FLUX	LINEAR	TAPE, WIRE
		LINEAR-CYCLIC	DATACELL
		CYCLIC	FIXED-HEAD DISK, DRUM
		CYCLIC-LINEAR	DISK
		RANDOM	CORE, DISK
	ELECTRONIC STABLE	FIXED	FLIP/FLOP, RELAYS, STEPPING SWITCHES
		RANDOM	SEMICONDUSTOR ARRAY, RELAY ARRAY
	CHEMICALLY STABLE	LINEAR	PHOTO STORE

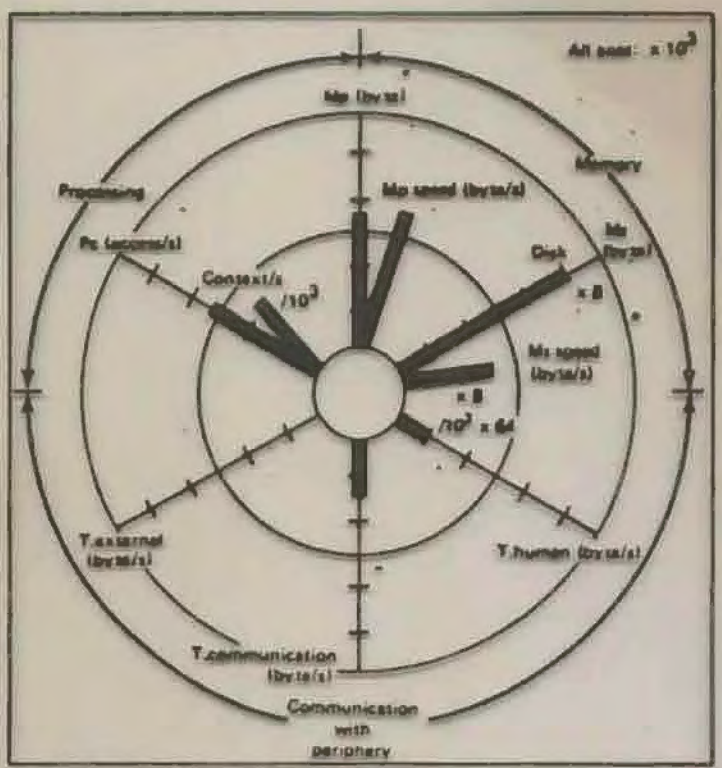


Fig. 2. A representative Kiviat graph.

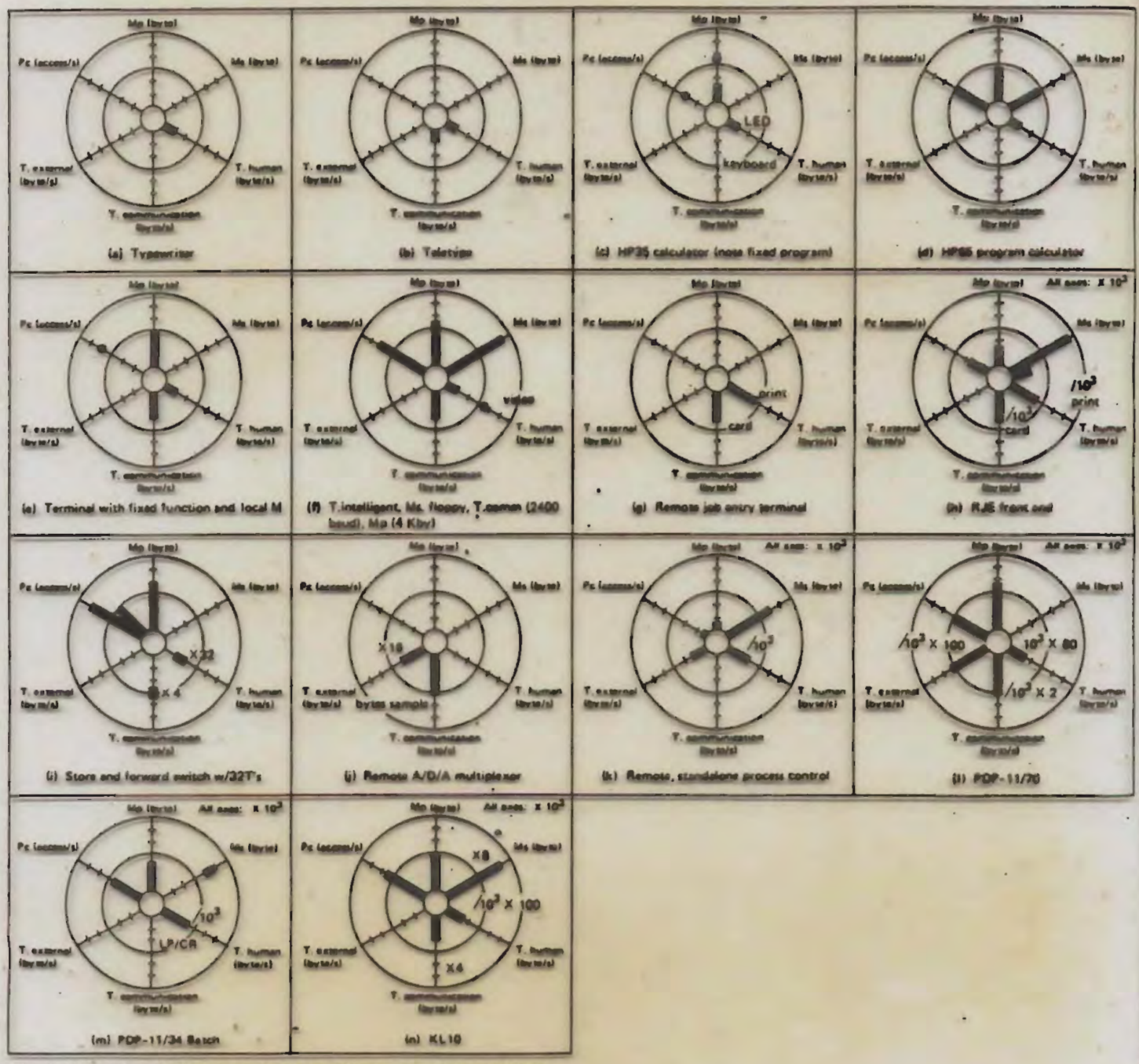


Fig. 4. Examples of Kiviat graphs for various computing systems.

time

- The CM Uses a "standard", cyclic Technology Evolution Model ⇒ TIME
  - Technology Generations (after the fact)
    - Need
    - Structure
    - Use (after the fact)

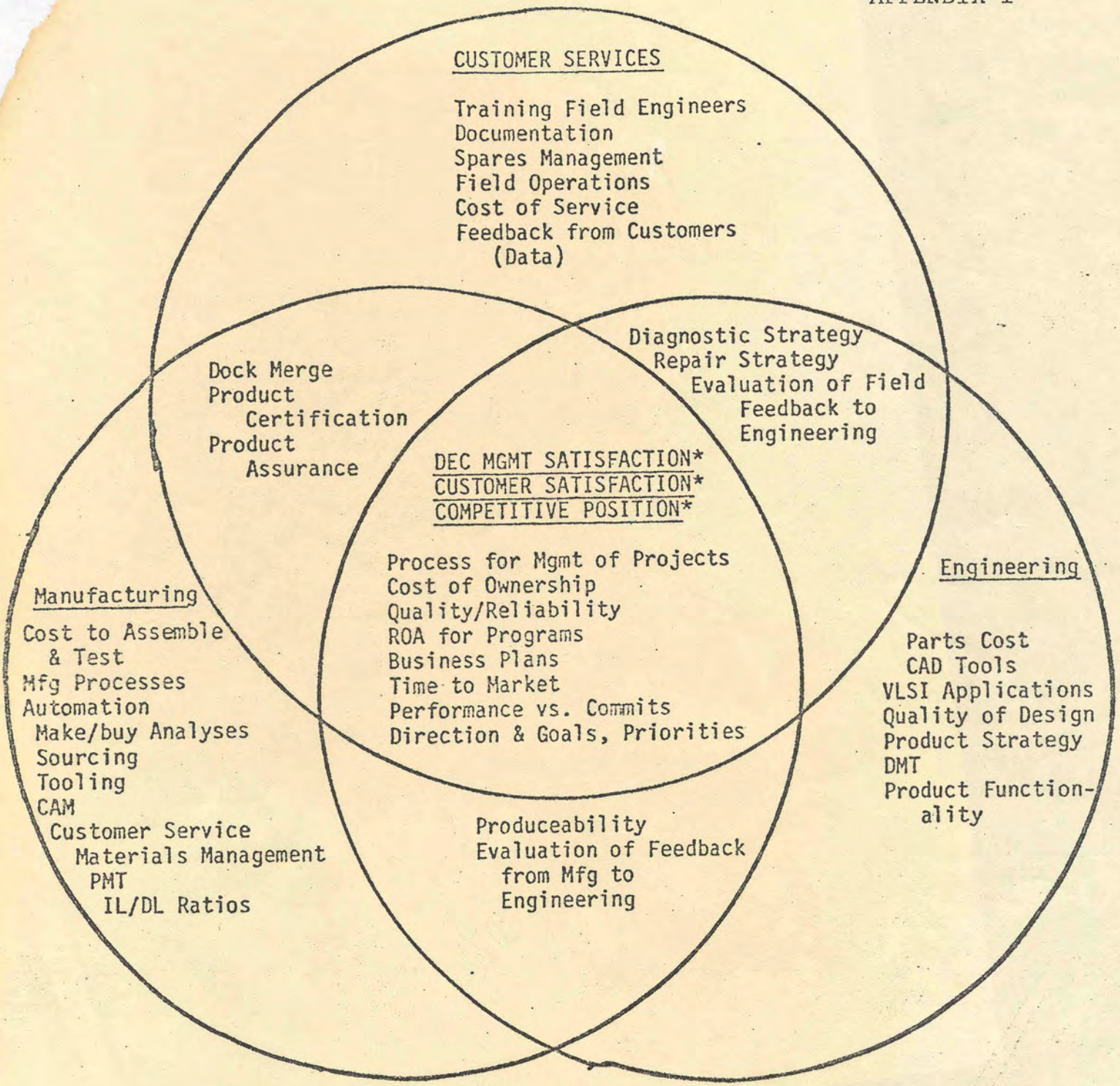
Function
- Why & When was it formed?
- How was it formed?

- Hardware (and Software) are classified according to their information processing function.

  The functions are those by Bell & Newell. These form the taxonomic Classes.
  - What does it do?
  - How does it do it?
- Many resultant Classes (eg. C's, P's) and species are classified in trees

ENGINEERING, MANUFACTURING AND CUSTOMER SERVICES INTER-RELATIONSHIPS:
SORTING OUT THE WORK THAT NEEDS TO BE DONE

APPENDIX 1



* PRIMARY GOALS

DWB
2/12/82

MARKET SEGMENTATION SCHEMES

- LEVEL OF INTEGRATION (I.E. WHO DOES WHAT?)
  - ≈
- HOW DISTRIBUTED. / WHERE DIST.
- APPLICATIONS:
  - STRUCTURE (M, P, T, S-REQ'D).
  - LANGUAGES
- LANG. / OP. SYS. STRUCTURE DIMENS. (SEE NEXT FIG.).
- PRICE
- BASIC PERF. (≈ P. STRUCTURE)

OVERALL

ORGANIZATIONS

RESULTS

TECHNOLOGY PROVIDES:
- ↑ PERF
- ↓ PRICE (/UNIT)
- ↑ PERF./PRICE

MARKET ALTS.

MINI- + OTHER COMPUTER LEVELS-OF-INTEGRATION

TECHNOLOGY AND DESIGNERS

BASIC DRIVES FOR PERF.

PROCESS

LEARNING CURVES / TECH. PROG.

INTERACTION ... E.G. DEC SEMICONDUCTOR / MAGNETIC STORAGE TECH.

IMPLIC. ABOUT FUTURE COMPUTERS

MARKETPLACE (USE)

SEG. DIMENSIONS
- FUNCTION
- STRUCTURE
- USE

RELEVANT COMPUTER DIMENSIONS

RANGE OF MACHINES

Organization ☆

MACHINES

SOFTWARE DIMENSIONS
- OP. SYS. (URGENCY)
- LANGUAGE
- DEDICATEDNESS (OF USE)

TAXONOMY

TOTAL ENVIR.
- SMALL VS. LARGE
- BASIC COSTS

MACHINE COST BASED ON MEM. HIERARCY.

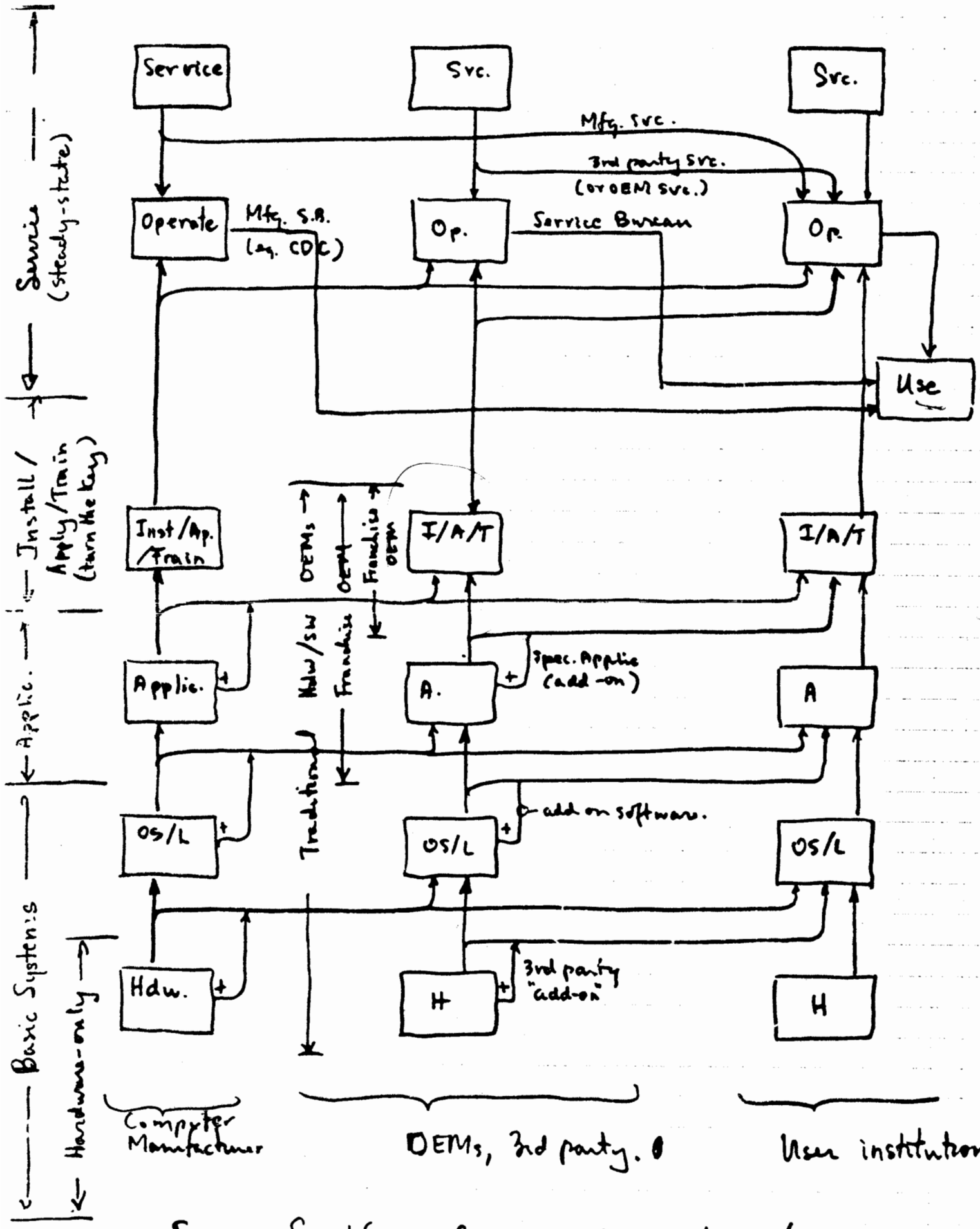
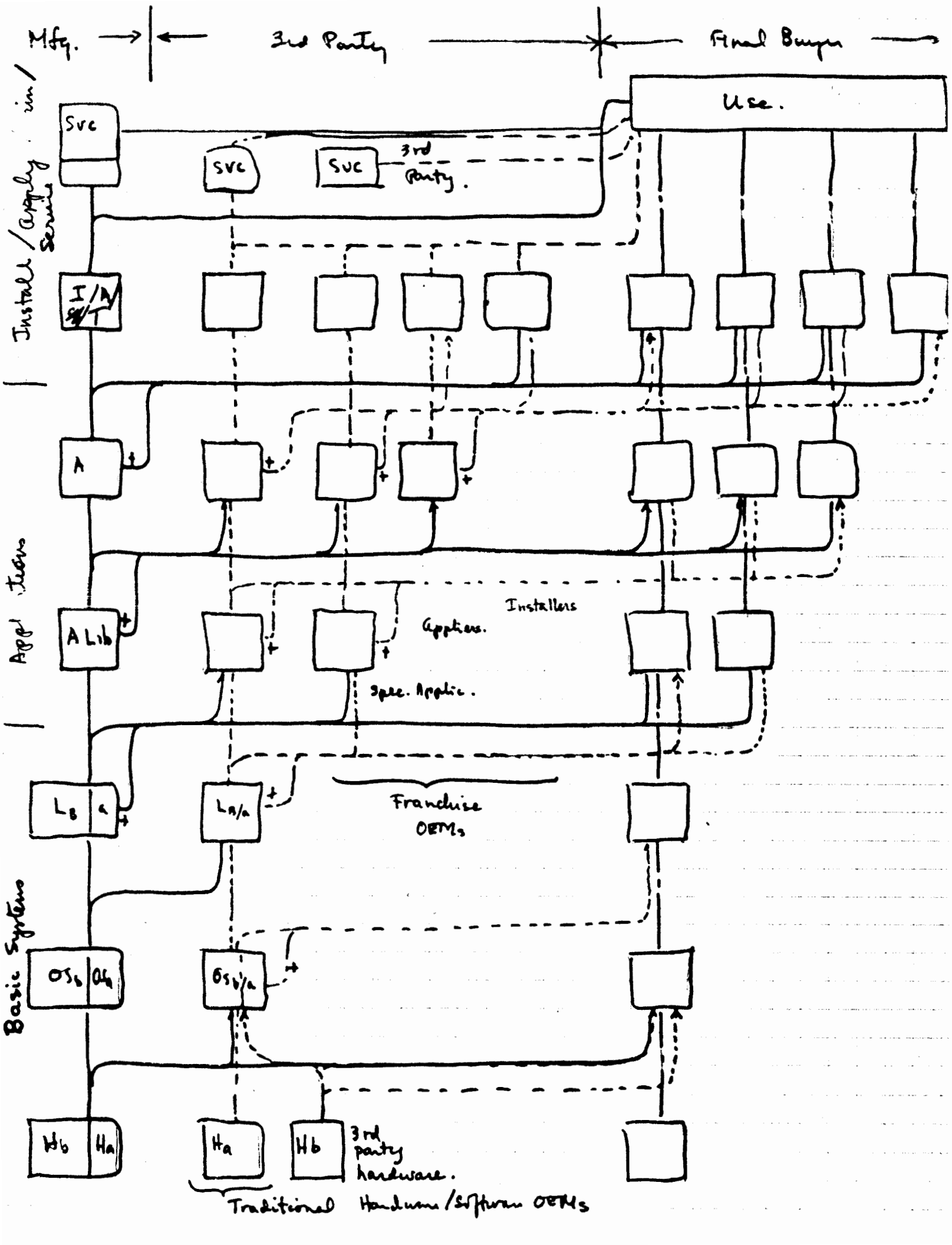


Fig. ~~Simplified~~ Channels of distribution & and service for computer systems (simplified)


Mfg.
3rd Party
Final Buyer
User.
Svc
SVC
SUC
3rd Party.
Install / apply service
I/A S/T
A
A Lib
Appl Items
Installers
Applics.
Spec. Applic.
L_B a
$L_{a/a}$
Franchise OEMs
Basic Systems
OS_b O_a
$OS_{b/a}$
Hb Ha
Ha
Hb
3rd party hardware.
Traditional Hardware/Software OEMs

MARKET SEGMENTATION DIMENSIONS

PRODUCT

- FUNCTION
- DISCIPLINE/ENVIRONMENT Based FUNCTIONS
- STRUCTURE I.E. PMS (V.S. FUNCTION)
- PERFORMANCE
  - HARDWARE
  - OP. SYS.
  - LANGUAGE
  - USE GENERALITY
- RELIABILITY, MAIL., MAINTAINABILITY

DIST. CHANNEL

- PRICE (UNIT/SALE)
- TERMS/CONDITIONS/SVC.)
- RENT VS. BUY
- SELLING (Catalog)
- 3rd Parties.

USER

- GEOGRAPHY
- STD. IND. CODE
- GENERIC ACTIVITY
- INTELLECT. DISC.
- DEMOGRAPHIC
- ORGANIZ. STR (SIZE, OWNERSHIP, CENTRALITY, GEO. CENT., DIV. VS FCN, DECIS. MAK,
- USER CAPABILITY
  - PRODUCER - Applic. Part./Cap. Level of I
- COST, RISK, BENEFIT
- APPLIC. TECH / REAL TIME
- SHARED VS DIST
- APPLIC. PROB. LOC.

FUNCTIONAL SEGMENTATION

- EDP
- SCI (BATCH, T/S FOR COMP
- INDUSTRIAL CONTROL (DISC/CONT)

- BUSINESS
- SCIENTIFIC
- CONTROL
- COMMUNICATIONS
- FILE
- TERMINAL
- T/S.

- COMMERCIAL
- SCIENTIFIC, ENG., DESIGN BASED
- MANUFACTURING.
- COMMUNICATIONS
- NETWORK (E.G. RAILROAD) CONTROL
- EDUCATION (CAI)
- HOME-BASED.

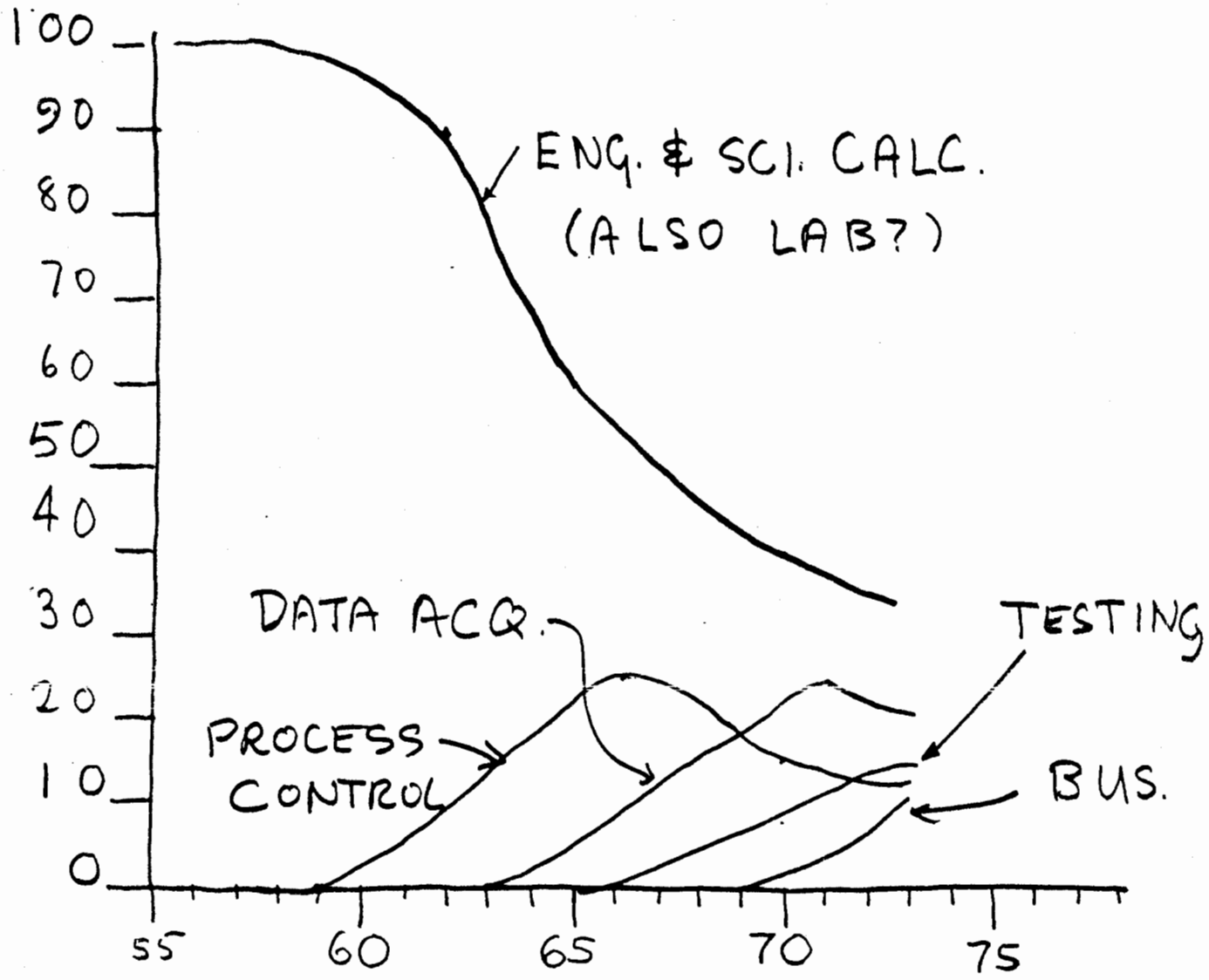
CONVENTIONAL

B/N (1971)

B (1977)

A THANKS TO IMPLEMENTATION AM

COMMUNICATIONS	S, K, M.
EDP SUPPORT	T
BUS. DATA PROC.	D, TD, TDM
SPEC. DATA & WORD PROC.	TM.
IND. AUTOMATION	T, K, KM.
SPEC. DATA ACQ.	TM.
LAB & COMPUT.	DM, TM, ..
INSTRUCTIONAL.	T, TM., TDM.



M. PHISTER ESTIMATE OF
MINICOMPUTER APPLICATIONS.

PMS STRUCTURE BASED FUNCTIONS

C

- BUSINESS
- SCIENTIFIC
- MANUFACTURING CONTROL (PEOPLE)
- MANUFACTURING CONTROL (R.T.)
- NET. TRANSPORT. CONTROL
- EDUCATION
- HOME

M

DATA BASE

S

- CONTROL OF COMM.
- FRONT END
- STORE/FORWARD
  - COMM.
  - C-C.

T

- PERSONAL stand alone (Calcs, fixed fcn Calcs, Prog. Calcs)
- Personal C-based
  - Dumb
  - Text
  - Fxd FCN
  - Programmable
- PERSONAL RJE
- SHARED
- SPEECH i/O.
- SENSOR-BASE

DEC's MKT SEGMENTATION.

BASICS
- OEM - IRON COMPONENTS/SYSTEMS
- DCG - COMPONENTS (BOARD LEVEL)

END USE
- EDUCATION.
- ENG. COMPUTATION
- INDUSTRIAL.
- BUSINESS.
- LABORATORY.
- COMMUNICATIONS.
- Medical.

TURN-KEY
- TYPESETTING.

Generic — Word Processing Terminals

Product-based — 8, 10, 15

SIZE PARTITION

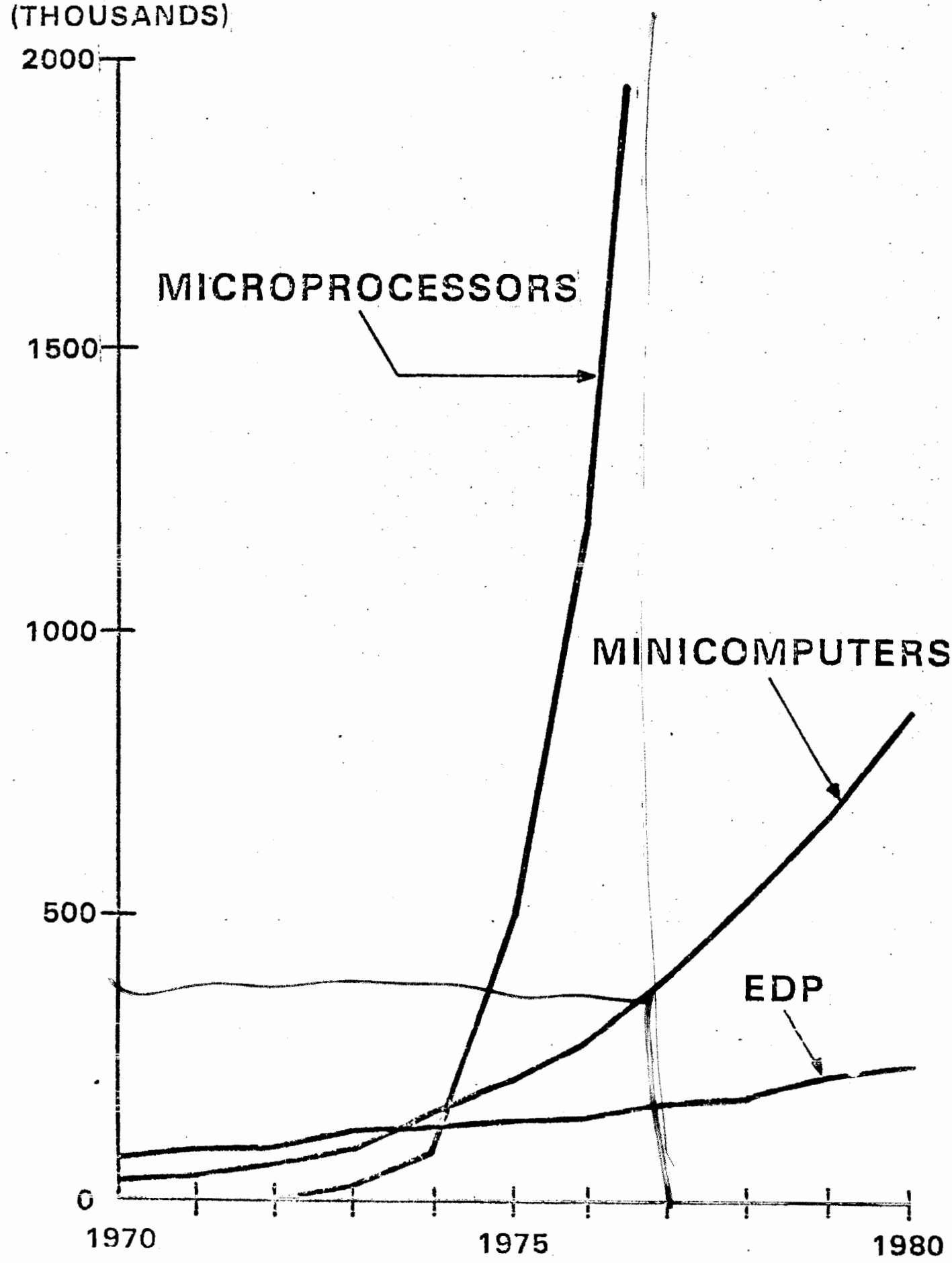
1. ~~Micro~~ µP (Integrated Into Peripherals
2. Modules destined to OEMs
3. ~~Micro~~ or Mini Cap. of Nets
4. " Spec. Processing
5. MINI SPEC. Pkg.
6. " COMPLEX Net. Comp.
7. " Use by NOVICE
8. " Top of Range
9. " " , but Integ. to Nets.

- MICRO − Weak, Var. Compx., FUNCT. Spec.
- " + Avg., Weak. Comp., Multi Pc
- MINI − GOOD, COMPAT., COMPLEX
- " + HIGH, WK. COMP., MULTI-Pc, GP.

Perf. | ARCH. | °SPEC. | COMPAT. | COMPX.

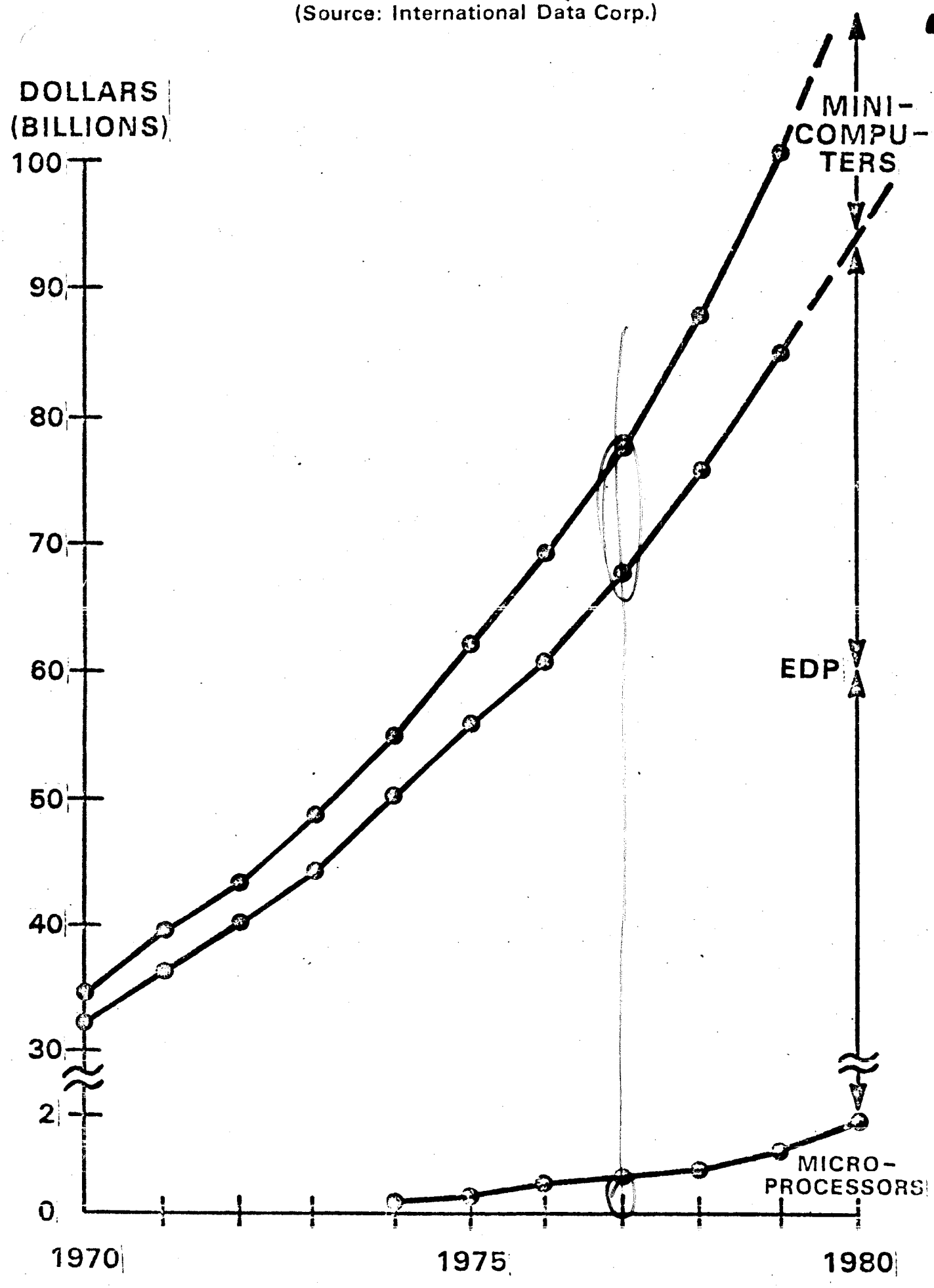
Cumulative Computers Installed Worldwide By U.S. – Based Manufacturers

(Source: International Data Corp)



Cumulative Worldwide Value of Computers Installed
(U.S. – Based Manufacturers)

(Source: International Data Corp.)



MINI APPLICATION ORIGINS

CONTROL (LOGGING, RECORDING, CONTROL — EG. LGP-30, RW-)

SMALL SCALE COMP. (LGP-30)

SMALL SCALE EDP (1401)

LAB. CONTROL + PROCESSING (EG. PDP-'s).

SWITCHING ↗

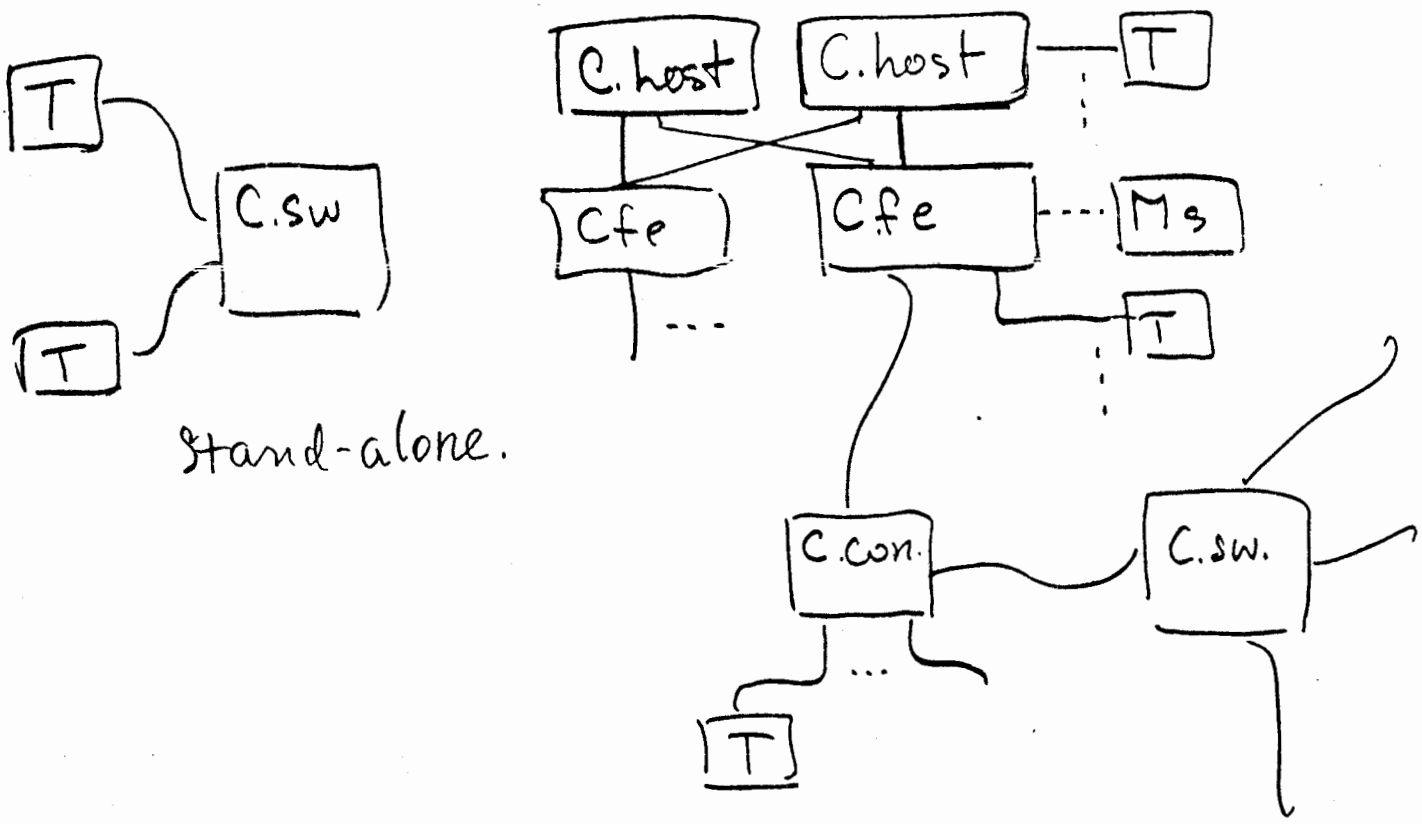
G.P. SHARED (EG. PDP-1)

[HOW USED vs. WHAT FOR]

COMMUNICATIONS

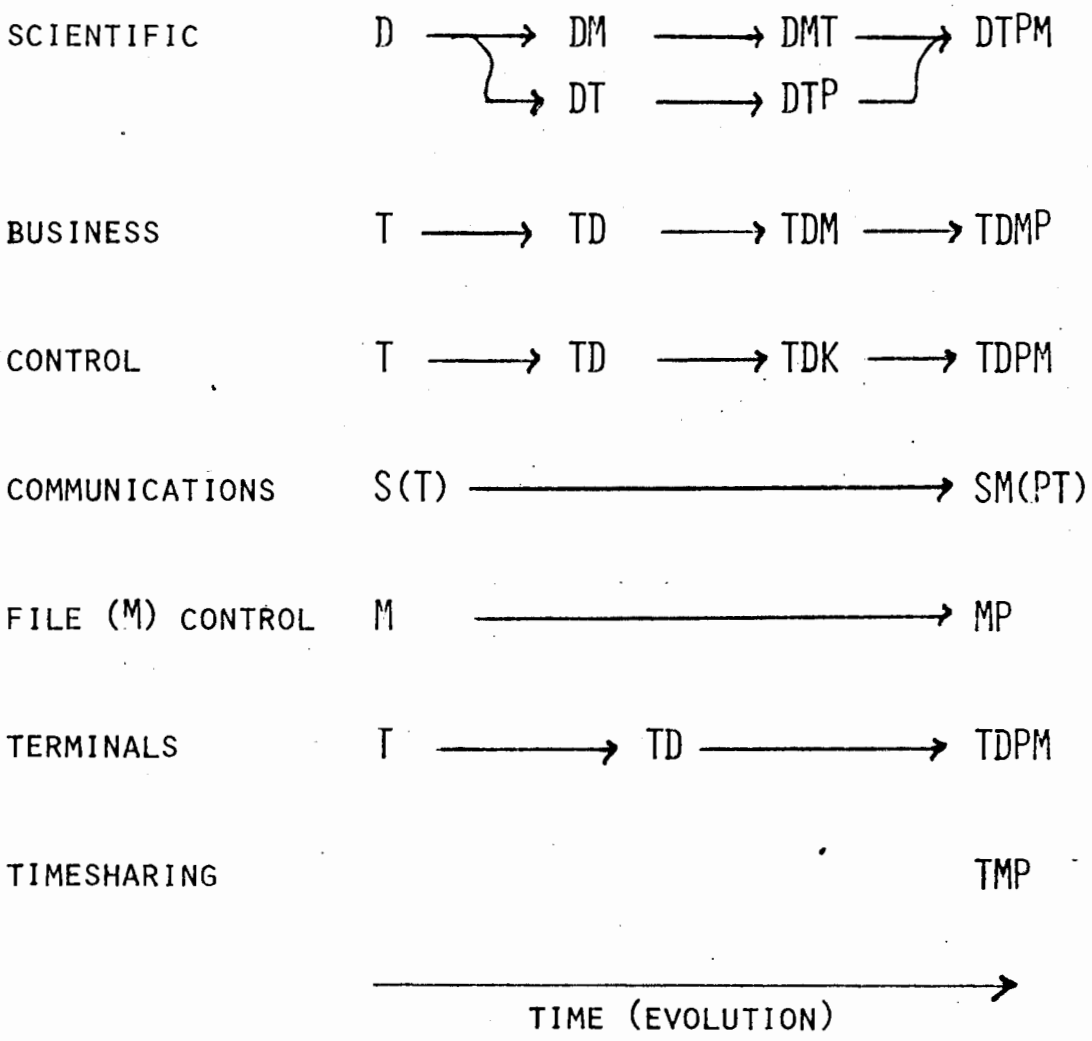
FRONT END
CONCENTRATOR
MESSAGE SWITCH.

PABX.
MONIT./CONTROL CENT. OFF.



A
1 4
A

COMPUTER-SPACE (FUNCTION DIMENSION)



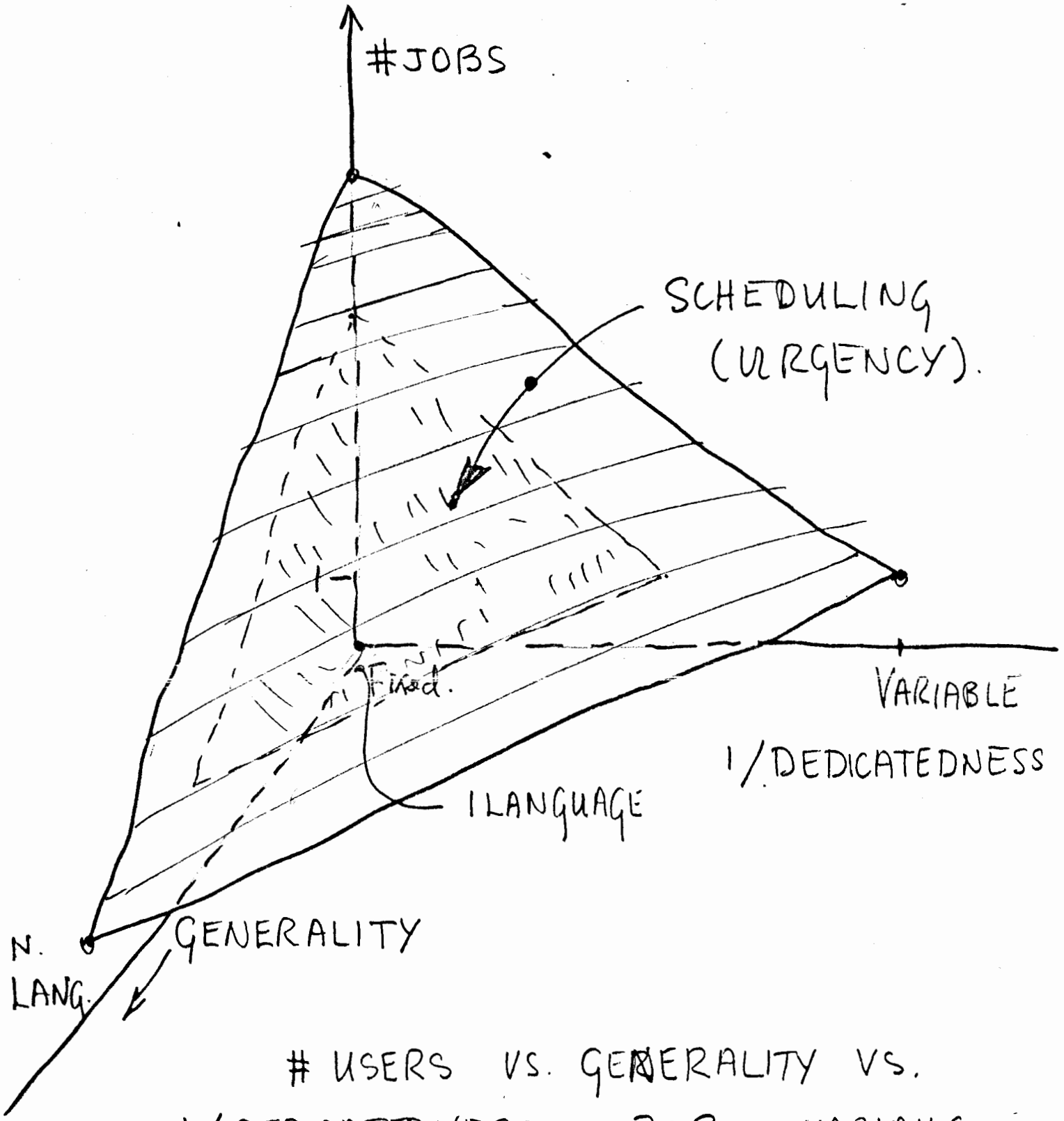
GB
1/12/76

STANDARD INDUSTRIAL CLASSIFICATION

- AGRICULTURAL, FORESTRY, FISHING
- MINING
- MANUFACTURING
- CONSTRUCTION
- TRANSPORTATION, COMM., ELEC., GAS, SANIT. SVC.
- WHOLESALE
- RETAIL
- FINANCE, INSURANCE, REAL ESTATE
- SERVICES
- PUBLIC ADMIN.

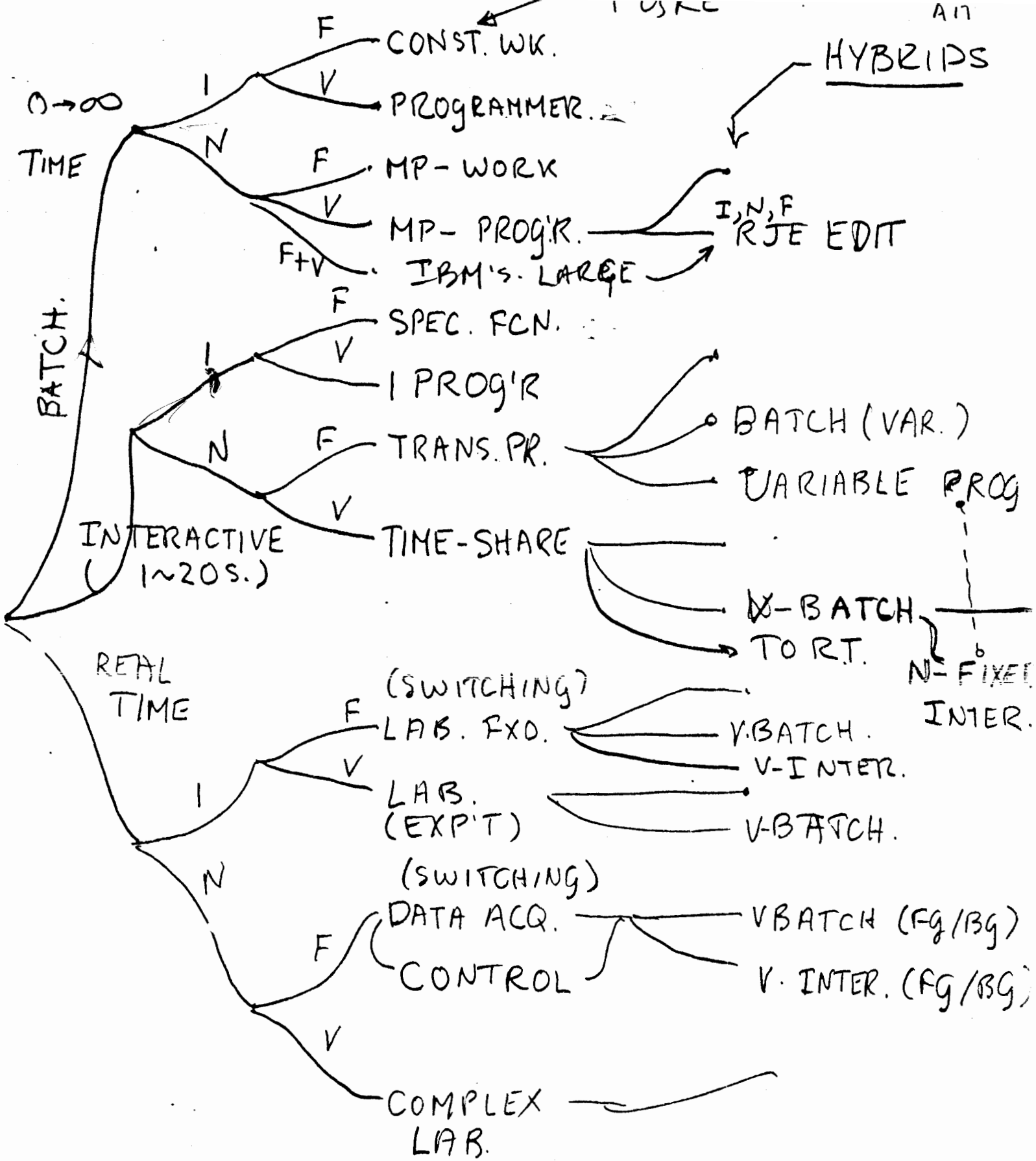
ACM APPLICATION CLASSIFICATION

- NAT. SCI.
- ENG.
- SOC/BEH. SCI
- HUMANITIES
- MANAGEMENT DP
- AI
- INFO. RET.
- REAL TIME
- MISC.



USERS VS. GENERALITY VS. 1/DEDICATEDNESS FOR VARIOUS FUNCTIONAL SYSTEMS (I.E. SCHEDULE URGENCY).

GB
2/13/76



TAXONOMY OF SYSTEM STRUCTURES

LANGUAGE / OP. SYSTEM. STRUCTURE DIMENS.

FUNCTION ~ SCHEDULING ~ URGENCY:

· BATCH	– DON'T CARE	0 → ∞ SEC.
· INTERACTIVE	– STOCHASTIC	2 – 10 SEC.
· REAL TIME	– DEMAND (GUARANTEED RESP.)	100μ – 1 SEC.

Trans. Proc.

PERFORMING FUNCTION: 1 OR N. JOBS

[SUB-STRUCTURE 1 OR M PROCESSES/J.]

° DEDICATEDNESS: FIXED OR VARIABLE

~ UNCERTAINTY (PROGRAMMABILITY)

LANGUAGE GENERALITY.

- 1, FIXED.
- MULTIPLE, FIXED
- MACHINE + ABILITY TO ADD MORE

INCREASING {PERFORMANCE / RESOURCE} NEEDS

1-FIXED → 1-VARIABLE → N-FIXED → N-VAR → N-VAR + L-LANG.

1 LANG. → L-LANG.

INDUSTRIAL (Control).

t
- TRANSDUCTION - (DATA LOGGING)
- T + MEMORY (RECORDING)
- T + M + K (CONTROL)

- SWITCHING.
- S + MEMORY (ACCESS to DATA

E D P
- T + D (DATA PROCESSING) - REPORTS
- T + D + P (PROCESSING)
- T + D + P + M (ACCESS TO DATA

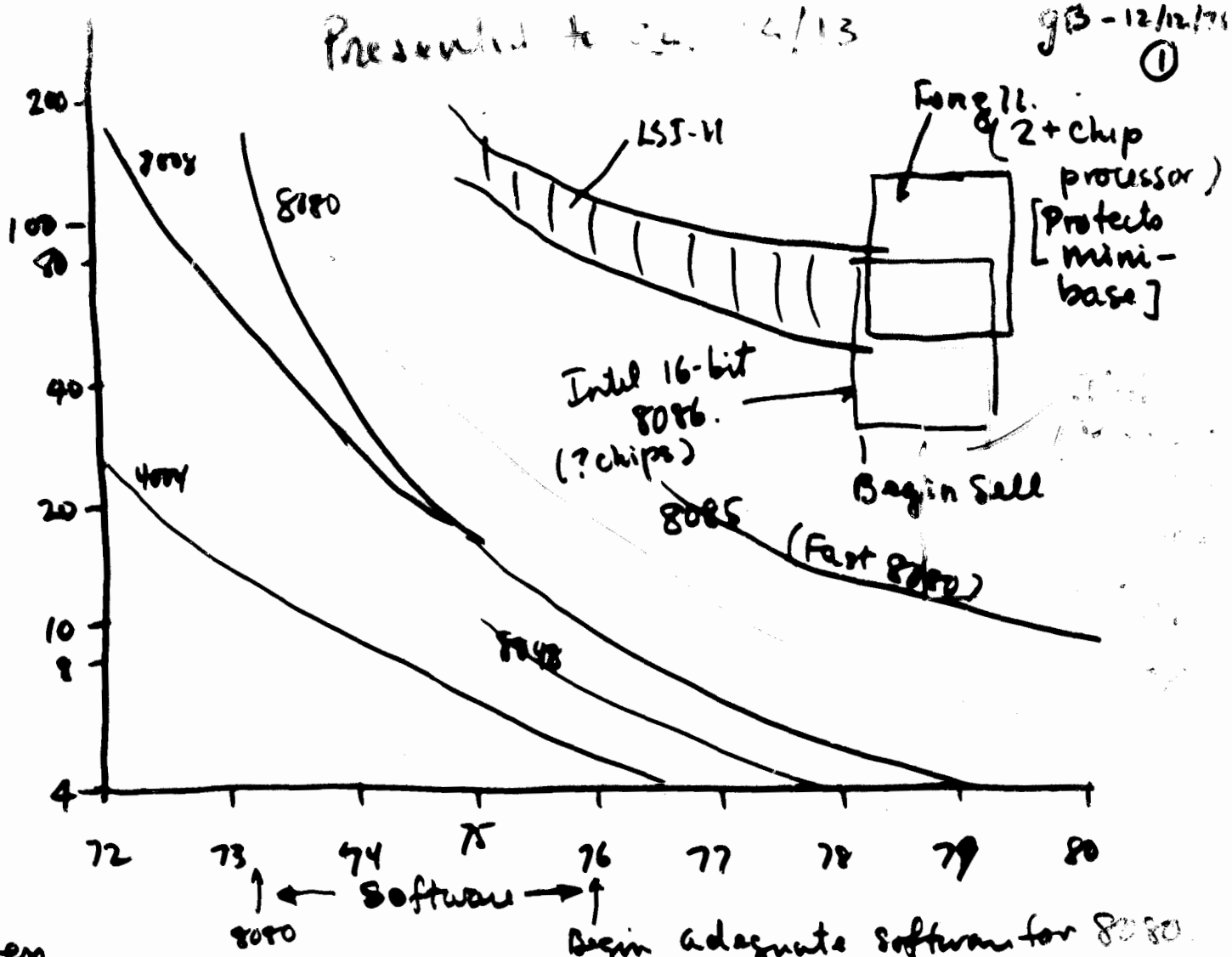
T + M — OFFICE

Sci.
- D - COMPUTATION
- T + D + M - DATA RECORDING.
- T + D + M + P - ON Line Control + Proc.

Presented to [illegible] 4/13

gB - 12/12/74

①



Given

INTEL Currently dominates* Micro. Mkt (Below Mini) at Board & Chip level w/ 8080

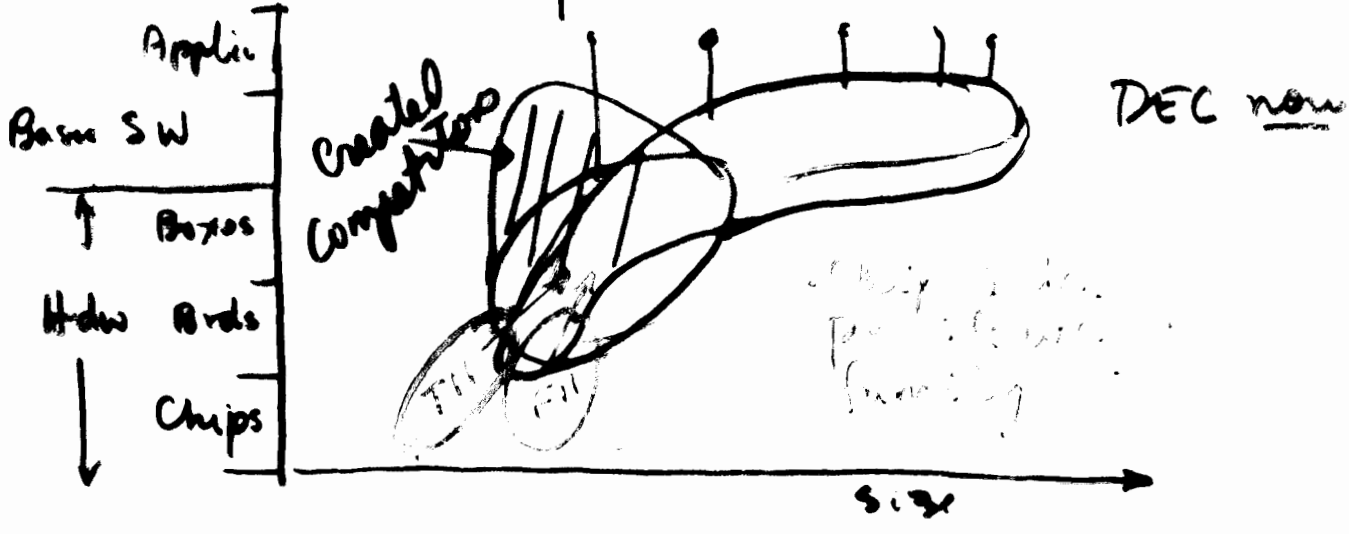
*(The 8080 outsells (3:1), lots of Sources; +on per

The 8086 as a 16-bit Mini (with 20-bit address) in 12-18 months <u>could be</u> significantly better than the 11! (Hence would become the standard Mini in 12~18 mot 3 years.

GB 12/12/76
②

Dilema

1. Let INTEL Become the standard, but hope it won't. It will take a long time to affect us since many small vendors have to buy it and form C. Systems with it. (It may be possible to build an 11/70 class machine with 10-20 Processors)
2. Take advantage of 11's as the current standard mini — especially since world wants a standard. (the military effort). and attempt to make the 11 the standard instead of INTEL. This will create systems competitors, but we will be in no worse position than 1 ... and should be in a better position.

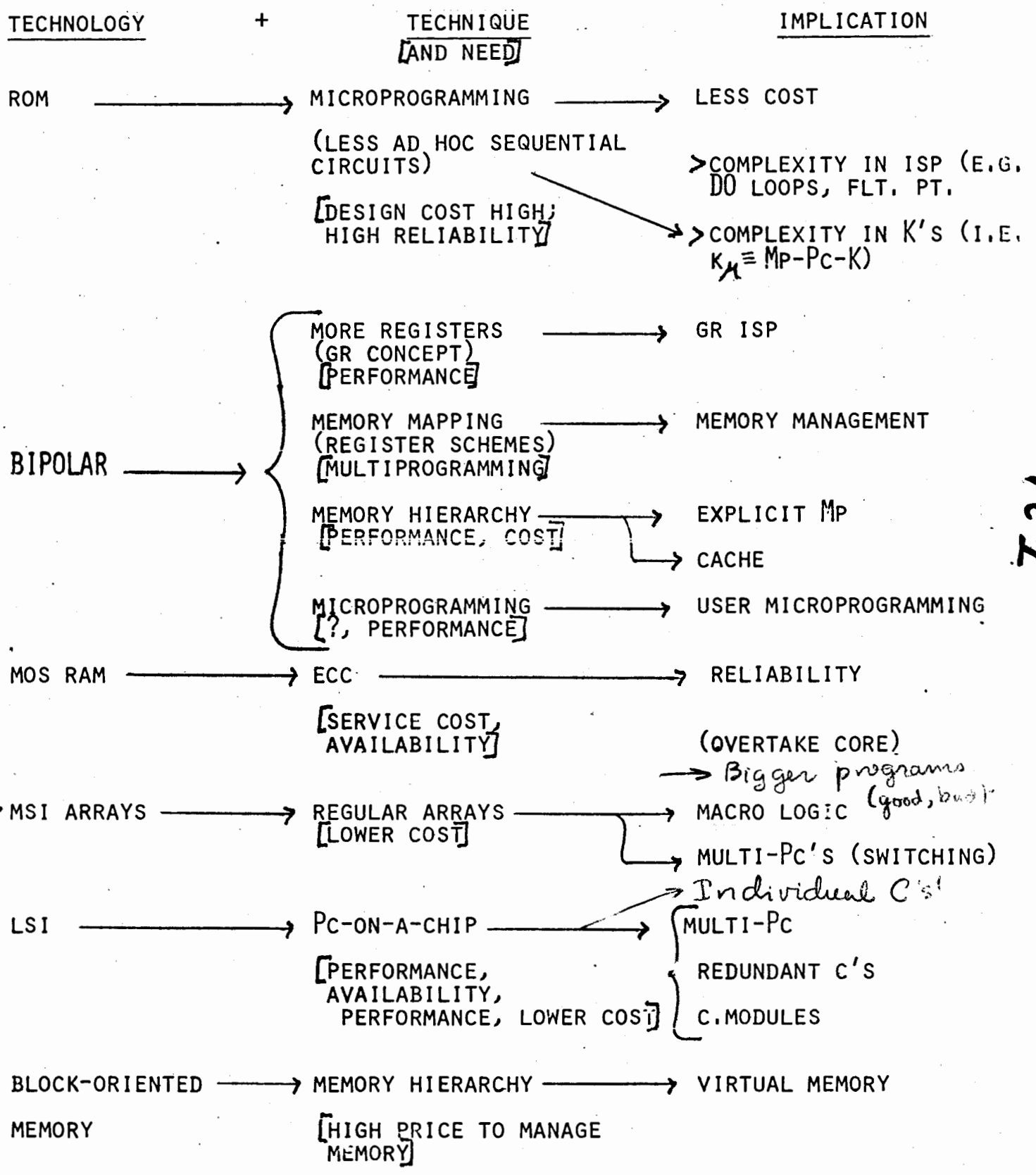


I want to talk with outside vendors ③
(eg. Fairchild, Motorola, TI?, Intel??)
about supplying (designing & building)
Chips which they would sell on Open Mkt!

Because: (or can we obtain quickly)

1. We don't have adequate Eng. resources to get both T-11 & F-11 ... and we may not have adequate resources to get F11 in time.
2. Our MOS technology is 1~3 years behind and we will be lucky to stay there.
3. The Eng. resources must also include Special i/o Chips, which we don't have.
4. It isn't clear that we want in Chips Sales business due to low profitability, high cost to lean business, and need to sell Chips with memories and i/o... which we do not have!!
5. Our current customers want Chips!
6. This is a small part (but important in future) and I don't feel we'll adequately work it strategically!

TECHNOLOGY IMPLICATIONS



T-21

GB
1/12/75

YEARLY IMPROVEMENTS IN TECHNOLOGY (1975)

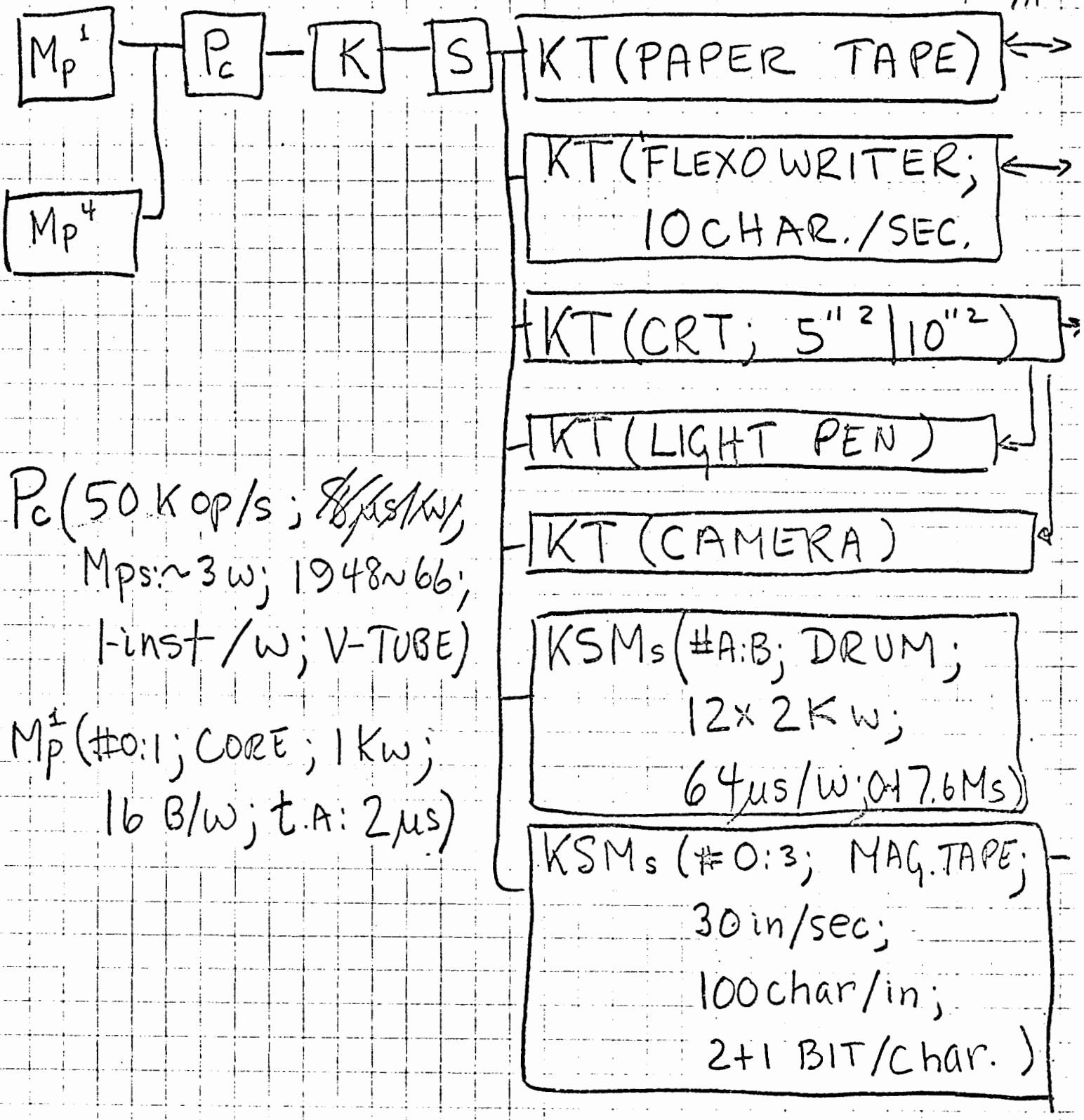
- SEMICONDUCTORS
  - DENSITY 2^{t-1962}
  - = 60 ~ 80 %/yr (CONSERVATIVE)

- DISKS (62-74) - DENSITY = 41%/yr.
- CORE PRICE IMPROVE 30%/yr.
- TAPE (52-73) - 23%/yr DENSITY
  29%/yr. DATA-RATE
- POWER, PACKAGING ~ 0
- MINIS - 31% IMPROVE IN PRICE (SINCE '60)
- TERMINALS - YES.

DISK TECHNOLOGY 1975

	PRICE (K$)	SIZE (MB)	C/B (¢/B)	ACCESS T.
FLEX.	3	2.5	.12	1 SEC.
1 PLAT.	6	30	.02	50 Ms.
3-5 "	12	160	.0075	↓
10 "	25	800	.003	20 Ms.

	MB/PLATTER	YRS (AT 41% YR)
1.	30	~~43~~
3	53	1+
5	80	0



MIT WHIRL WIND I BLOCK (PMS) DIAGRAM.

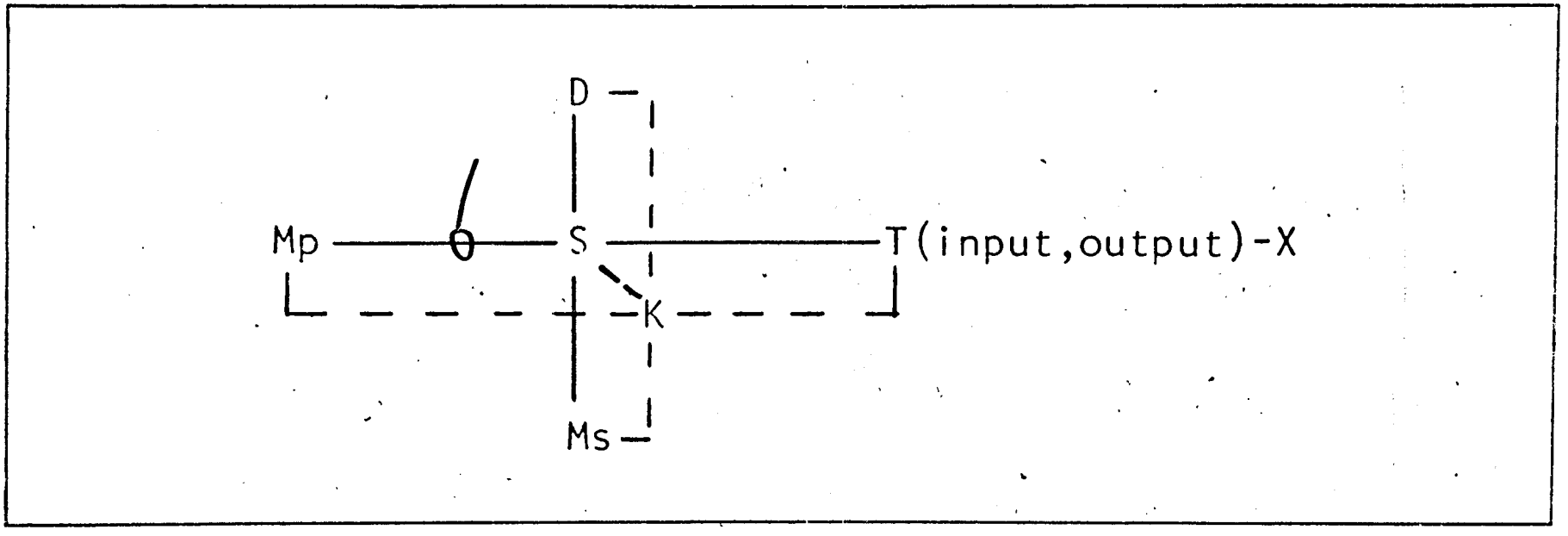


Fig. 6. Early computer model (with Ms and S) PMS diagram.

Infotech Agenda
11/22/76

BASIC DESIGNS.

1. STATUS-QUO

ALL Costs ≈ k

↳ (COMPUTER, SALES, Operations)

2. MINI(MIZE) COST

Perf ≈ function ≈ k.

Decrease cost... accelerate learning + demand.

3. BUILD "SUPER" COMPUTER

4. BUILD SUBSET

(Eg. CALCULATOR).

A Course of Study in C. Hdw. Arch.

Computer — Dec. 75

✓2 - Intro & Meta-rep. (Levels, text, Languages,)

✓5 - Data Repr. (formats, Vectors, ...)

✓5 - Inst. + Addressng (what, name space, op's)

✓6 - Interpretation + Control (μ-prog)

8 - M - hierarchies (refs, Components, ...)

4 - Protection & Hdw. Aids to Supervisors

5 - P. Special (channels ... μP.

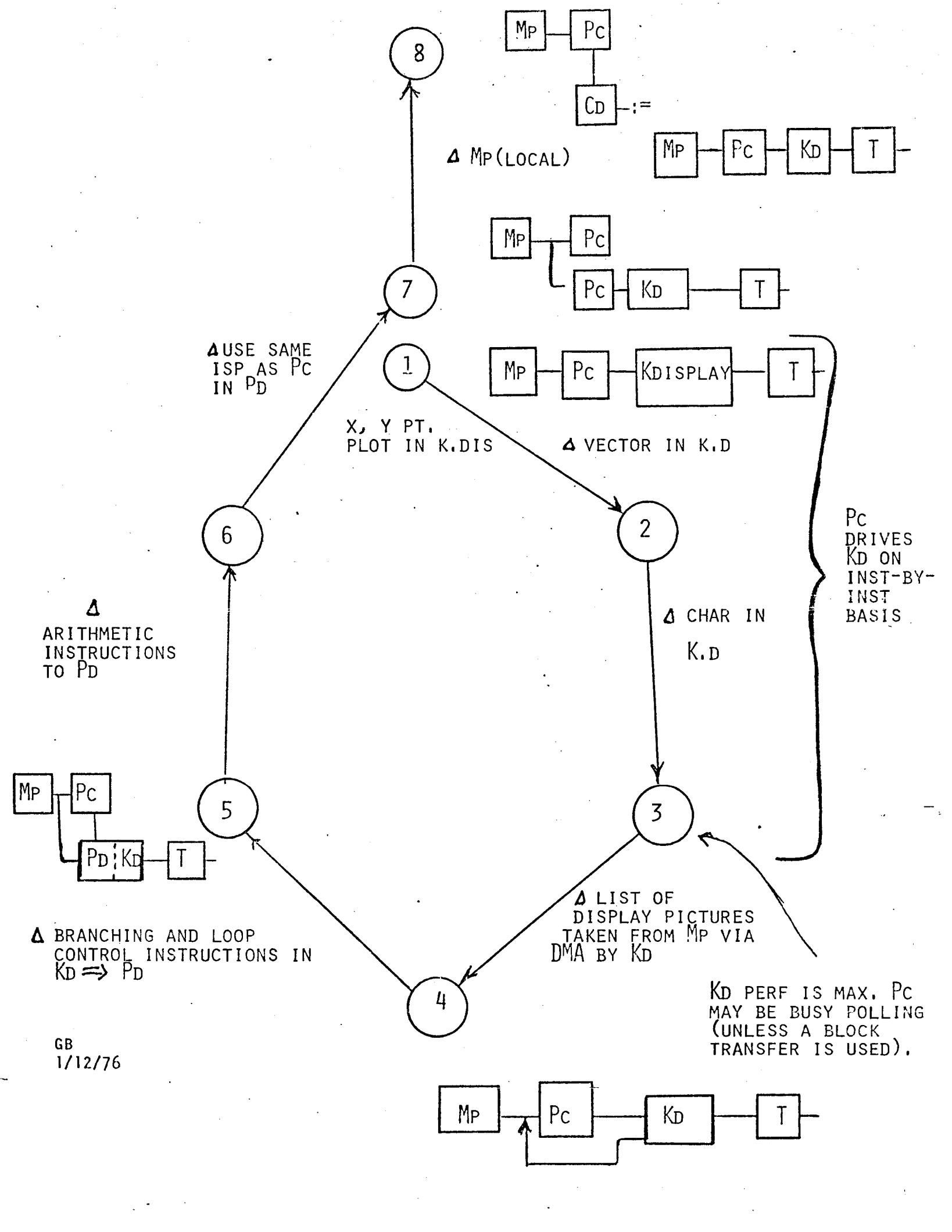
✓4 - mC, (mP, performance, Nets)

9 - Performance Evaluation

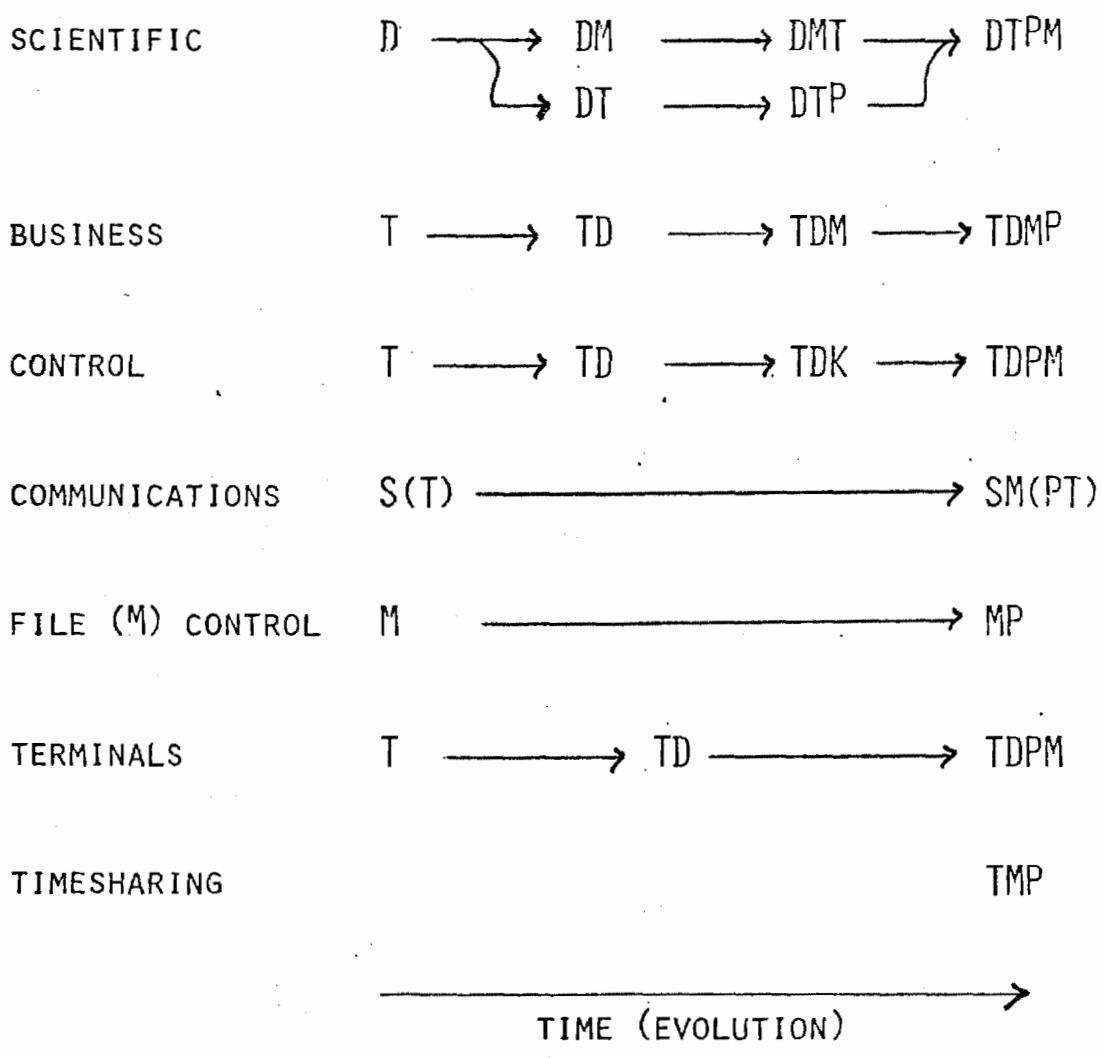
✓5 - Reliability

6 - Design Eval.

59


8
MP
PC
CD
:=
Δ MP(LOCAL)
MP
PC
KD
T
MP
PC
PC
KD
T
7
ΔUSE SAME ISP AS PC IN PD
1
MP
PC
KDISPLAY
T
X, Y PT. PLOT IN K.DIS
Δ VECTOR IN K.D
6
2
PC DRIVES KD ON INST-BY-INST BASIS
Δ ARITHMETIC INSTRUCTIONS TO PD
Δ CHAR IN K.D
MP
PC
PD
KD
T
5
3
Δ LIST OF DISPLAY PICTURES TAKEN FROM MP VIA DMA BY KD
Δ BRANCHING AND LOOP CONTROL INSTRUCTIONS IN KD ⟹ PD
4
KD PERF IS MAX. PC MAY BE BUSY POLLING (UNLESS A BLOCK TRANSFER IS USED).
GB
1/12/76
MP
PC
KD
T

COMPUTER-SPACE (FUNCTION DIMENSION)



GB
1/12/76

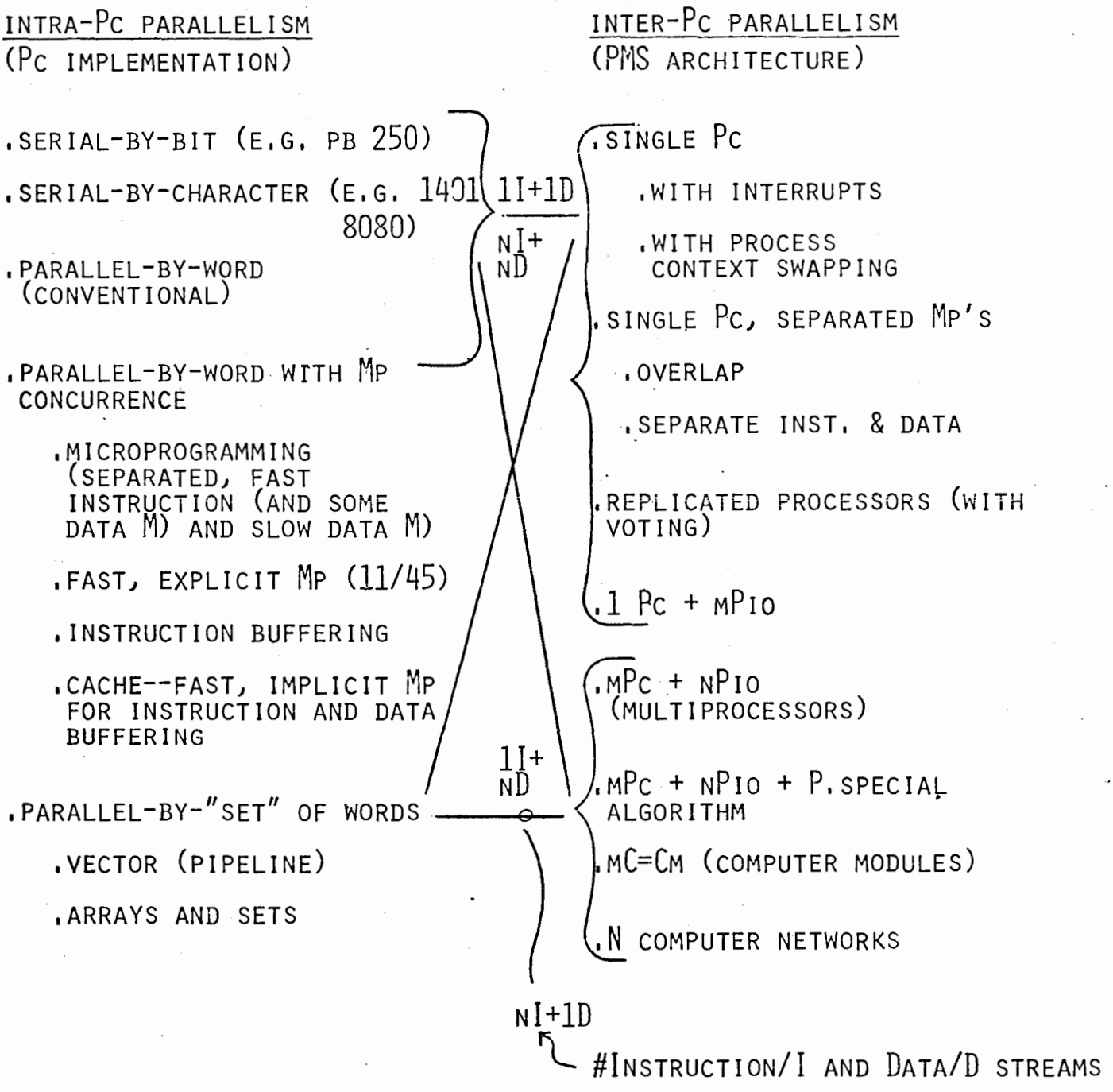
EVOLUTION OF IO CONTROL IN COMPUTERS

CONTROL, K EVOLUTION	COMPUTER CONTROL & PROCESSING FUNCTION
K. SIMPLE	Pc (WITH EMBEDDED K)
K (1 INSTRUCTION WITH INTERRUPTS)	Pc (INTERRUPTS & IO PROGRAM)
K (>1 INSTRUCTION)	PcIO (1 INSTRUCTION AT INTERRUPT)
K-P$_4$-MP (LOCAL) CIO	Pc + nPIO (CHANNELS)
	mPcIO
	Pc + P. SPECIAL (E.G. P. DISPLAY)
	CIO (SEPARATE COMPUTER WITH MP (LOCAL) FOR IO CONTROL)

GB
1/12/76

PMS-STRUCTURE DIMENSION

(FROM BELL & NEWELL)



GB
1/12/76

COMPUTING EUROPE (6 Nov 1975)

" WHEN IS A MINICOMPUTER NOT A MINICOMPUTER?
SURELY IT IS TIME THE INDUSTRY FACED THE PROBLEM OF EVOLVING A STANDARD DEFINITION.

1. ANNOUNCEMENTS FROM MINICOMPUTER COMPANIES AREN'T, BY DEFINITION, MINIS.

2. DATAPRO RESEARCH CORPORATION
...THE WHOLE CLASS OF STORED-PROGRAM DIGITAL COMPUTERS WHICH ARE SUITABLE FOR GENERAL-PURPOSE APPLICATIONS AND ARE PRICED BELOW $50,000.

3. ELECTRICAL RESEARCH ASSOCIATION (1972)
...A COMPUTER...WHICH MAY BE PURCHASED FOR LESS THAN $40,000 IN THE FOLLOWING MINIMUM CONFIGURATION: Pc, Mp (256~8K WORDS), T.CONSOLE, T(TELEPRINTER + PAPERTAPE READER AND PUNCH), POWER SUPPLIES (ETC.); SOFTWARE...WITH BOOTSTRAP AND BINARY LOADER.

4. BARNES IN SPL INTERNATIONAL MINICOMPUTER FORUM 1975

...HARD TO SAY PRECISELY BECAUSE OF BROAD SPECTRUM OF SIZE, PERFORMANCE, BUT USUALLY A RELATIVELY INEXPENSIVE, SMALL SCALE COMPUTER WITH A WORD LENGTH OF 16 BITS OR LESS WHICH CAN OPERATE IN AN OFFICE ENVIRONMENT WITH NO AIR CONDITIONING, NO FALSE FLOORS AND NO SPECIAL POWER SUPPLIES.

5. DEC (UK) MINIMAL CONFIGURATION COST OF < £ 20K AND CAPABLE WITHIN THE MINIMUM OF TAKING A HIGH LEVEL LANGUAGE (E.G. FORTRAN, BASIC).

6. VARIAN--THE DEFINING CRITERIA IS THAT THE ACTUAL PHYSICAL EQUIPMENT SHOULD BE PACKING MAINFRAME CAPABILITY INTO A PHYSICALLY SMALLER CABINET.

7. HP(UK)--SMALL GP-C WHICH IS FREQUENTLY THE MOST COST-EFFECTIVE SOLUTION TO A WIDE VARIETY OF APPLICATIONS IN BUSINESS, SCIENCE, AND EDUCATION."

GB
1/12/76

TECHNOLOGY IMPLICATIONS

TECHNOLOGY	+ TECHNIQUE [AND NEED]	IMPLICATION
ROM	MICROPROGRAMMING	LESS COST
	(LESS AD HOC SEQUENTIAL CIRCUITS) [DESIGN COST HIGH; HIGH RELIABILITY]	> COMPLEXITY IN ISP (E.G. DO LOOPS, FLT. PT. > COMPLEXITY IN K'S (I.E. $K_\mu \equiv M_P - P_C - K$)
BIPOLAR	MORE REGISTERS (GR CONCEPT) [PERFORMANCE]	GR ISP
	MEMORY MAPPING (REGISTER SCHEMES) [MULTIPROGRAMMING]	MEMORY MANAGEMENT
	MEMORY HIERARCHY [PERFORMANCE, COST]	EXPLICIT M_P CACHE
	MICROPROGRAMMING [?, PERFORMANCE]	USER MICROPROGRAMMING
MOS RAM	ECC [SERVICE COST, AVAILABILITY]	RELIABILITY (OVERTAKE CORE)
> MSI ARRAYS	REGULAR ARRAYS [LOWER COST]	MACRO LOGIC MULTI-P_C'S (SWITCHING)
LSI	P_C-ON-A-CHIP [PERFORMANCE, AVAILABILITY, PERFORMANCE, LOWER COST]	MULTI-P_C REDUNDANT C'S C.MODULES
BLOCK-ORIENTED MEMORY	MEMORY HIERARCHY [HIGH PRICE TO MANAGE MEMORY]	VIRTUAL MEMORY

GB
1/12/75

Larry Wade's slides 3/75

SUMMARY

- FUNDAMENTALLY A BUSINESS DECISION
- NO RESOURCES TO DO BOTH
- IBM FS COMPETITION
  - HEAD ON?
  - SEGMENT THE MARKET?
  - TECH. / ARCH. QUALITY?
- ORGANIZATION LIMITED
- SUPPORT ISSUES
  - MARKET READY?
  - CAN WE SELL / SUPPORT?
- PLANNING ENVIRONMENT

32 BIT STRATEGY

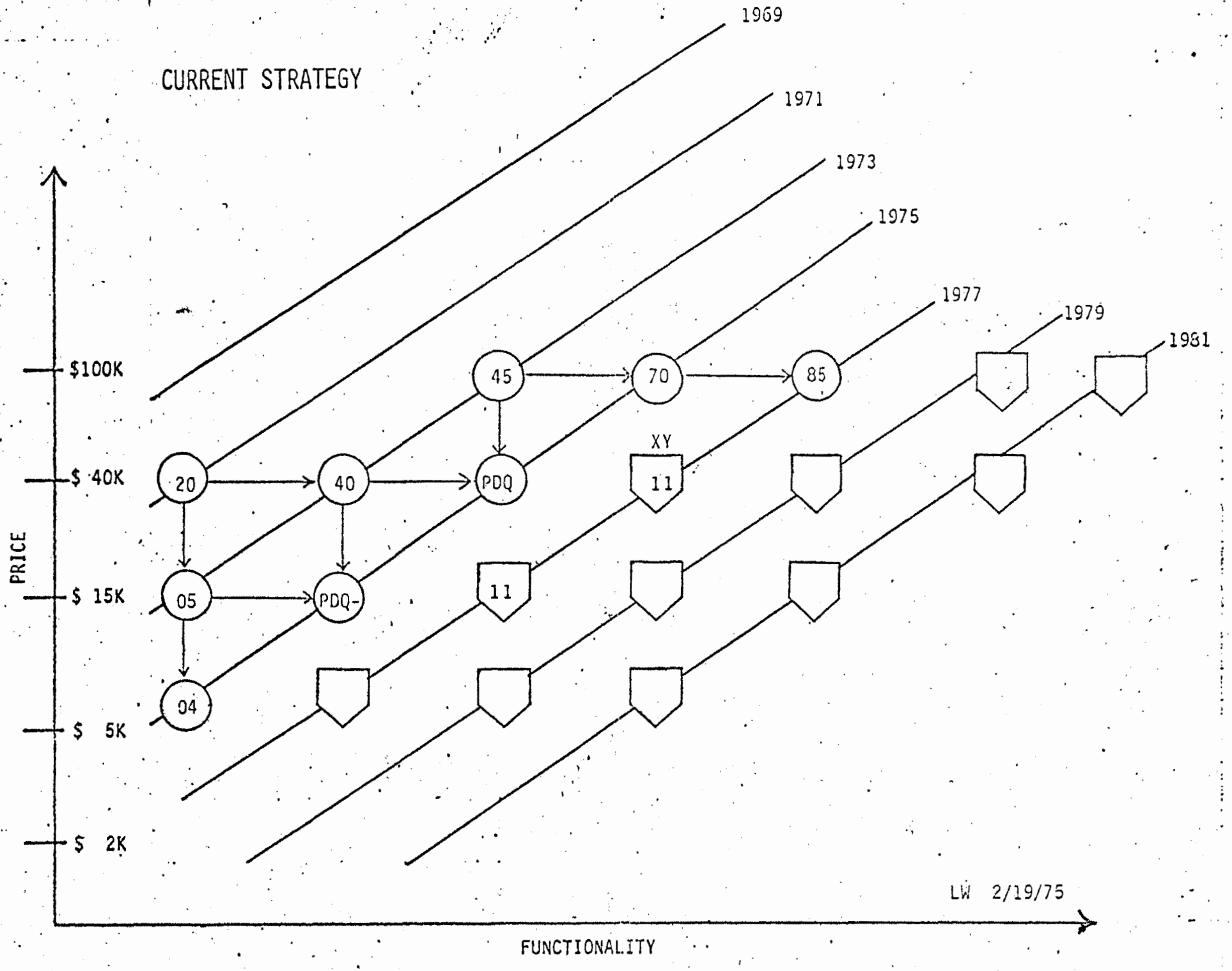
ARGUMENTS FOR

- PERCEIVED 11 COMPATIBILITY
- SOLVES VIRT. ADDRESS PROBLEM
- MODERN ARCHITECTURE
- UNIFIES 10-11 RANGE
- 11 COMPATIBILITY MODE
- SOME SOFTWARE CONVERTS

32 BIT STRATEGY

ARGUMENTS AGAINST

- LITTLE REAL COMPATIBILITY
- COSTLY
- INSTRUCTION SET DOESN'T MATTER TO END USERS
- NO SUBSTANTIAL PROPOSALS
- LARGE SOFTWARE COSTS
- MAKES UNICORN A DEC-10 PROD.
- FUTURE DEC-10 COMPETITOR
- IBM "FS" COMPETITOR


CURRENT STRATEGY
1969
1971
1973
1975
1977
1979
1981
$100K
$ 40K
$ 15K
$ 5K
$ 2K
PRICE
20
40
PDQ
45
70
85
05
PDQ-
04
11
XY
11
LW 2/19/75
FUNCTIONALITY

10 BASED STRATEGY

PRO	CON
LOTS OF SOFTWARE	18 BIT VA LIMITATION
COMPATIBLE UPWARDS	PDP-11 INCOMPATIBILITY
UNIFIES THE COMPANY	1962 ARCHITECTURE
NEAT	ALL EGGS IN ONE BASKET
TECHNOLOGICALLY ADVANCED	CURTAILS PDP-11 SOFTWARE
DEFERS VA PROBLEM	LEAVES PDP-11 VULNERABLE
	LARGE SOFTWARE EFFORT - LOW END

32 BIT STRATEGY

PRO	CON
PERCEIVED PDP-11 COMPATIBILITY	COSTLY ENDEAVOR
SOLVES VA PROBLEM	NO SOLID PROPOSALS
MODERN ARCHITECTURE	LARGE SOFTWARE COSTS
MULTIPROCESSOR DESIGNED IN	MAKES UNICORN A DEC-10 PRODUCT
UNIFIES 10-11 MARKETS	LITTLE REAL COMPATIBILITY
BACKWARD COMPATIBILITY MODE	EVENTUALLY A DEC-10 COMPETITOR
SOME SOFTWARE CONVERTS	

MAJOR ASSUMPTIONS

- PDP-11 ARCHITECTURE IS MATURE/LIMITED
- REPLACEMENT APPEARS IN 3 YEARS
- ALTERNATIVES ARE:
  - A. COVER 11 RANGE WITH 10 ARCHITECTURE
  - B. DEVELOP NEW ARCHITECTURE
  - C. SPLIT BETWEEN 10 & 11
  - D. DO BOTH 10 AND NEW ARCHITECUTRE
- SOFTWARE STRATEGY ASSUMES "B"

  NEW ARCHITECTURE

  RESEMBLES PDP-11

  PDP-11 COMPATIBILITY MODE

  NOT BINARY COMPATIBLE

  PERCEIVED AS 32 BIT PDP-11

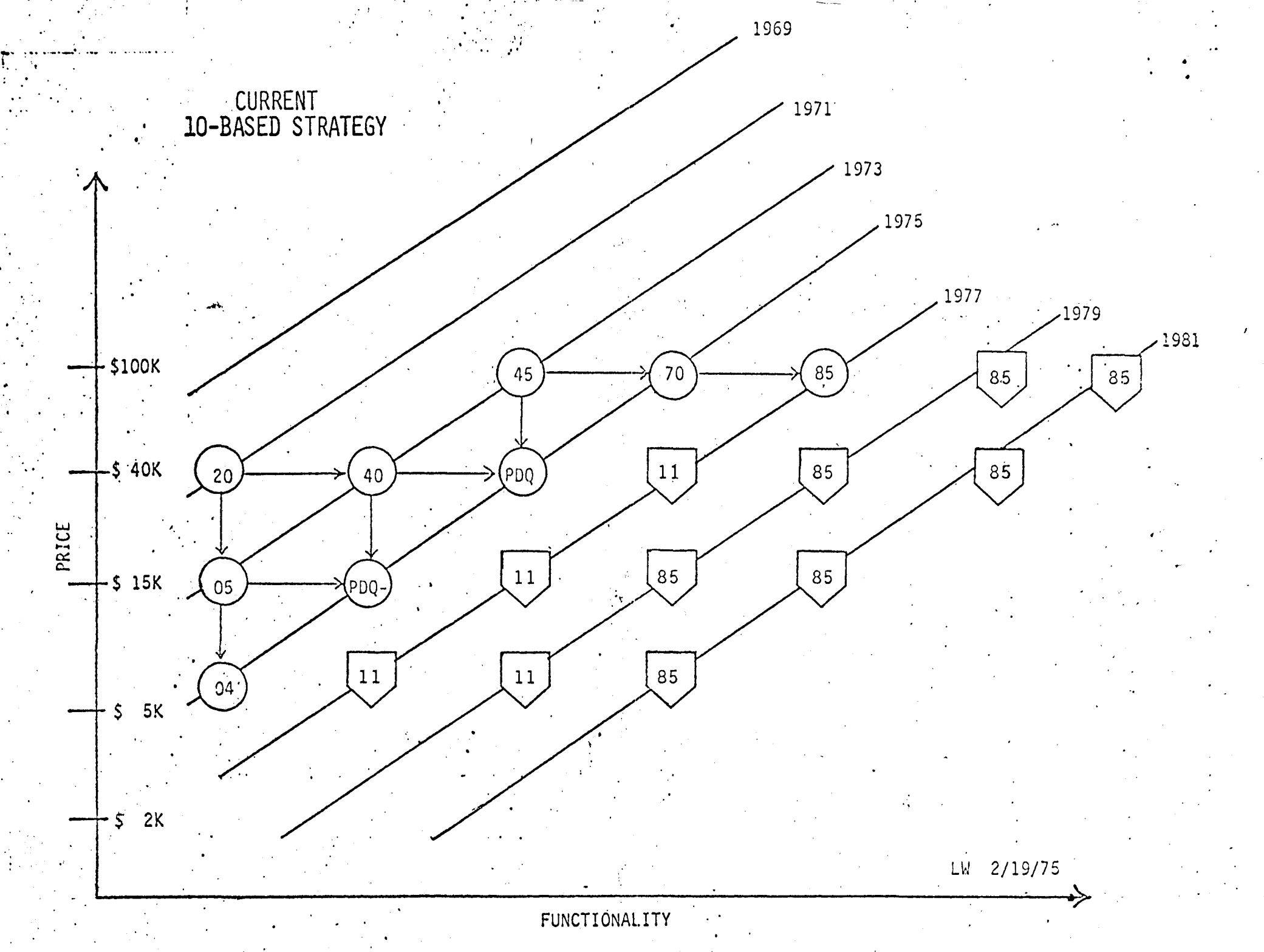
10 STRATEGY
ARGUMENTS AGAINST

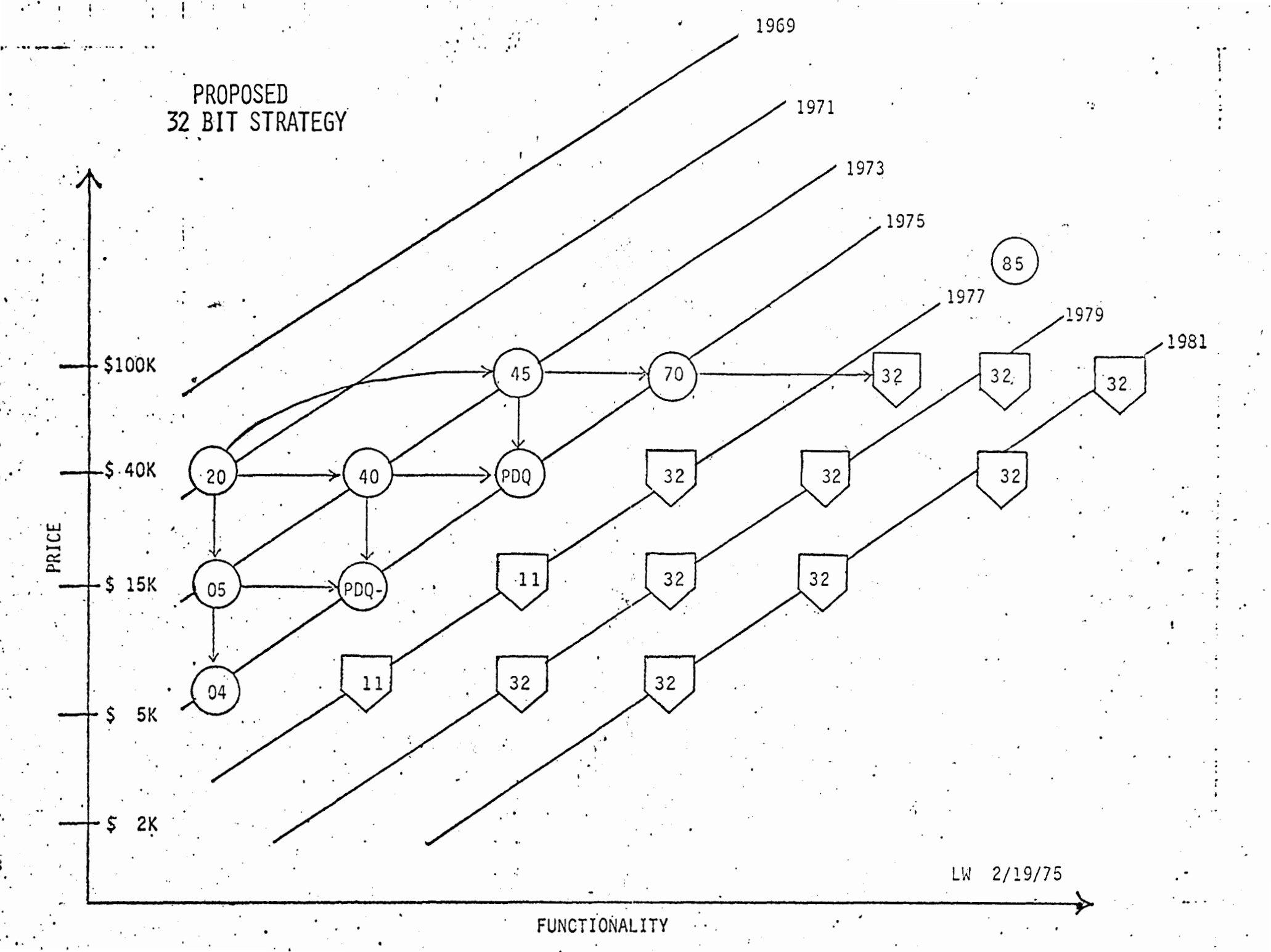
- LEAVES 11 VULNERABLE TO 32 BIT THREAT
- DONE AT EXPENSE OF 11
- PDP-11 INCOMPATIBLE
- SOFT. NOT APPROPRIATE FOR LOW END MARKETS
- VIRTUAL ADDRESS LIMITATION
- ALL EGGS IN 10 BASKET
- 1962 ARCHITECTURE
- LARGE FUTURE SOFT. EFFORT

IO STRATEGY

ARGUMENTS FOR

- PRICE/PERF. LEADER
- ANSWERS 32 BIT THREAT
- LOTS OF SOFT. NOW
- PIGGYBACK ON NEW IO SOFT.
- HIGH END COMPATIBLE
- UNIFIES THE COMPANY
- DEFERS VIRT. ADDR. PROBLEM
- IMPORTANT LEARNING VEHICLE FOR IO & II ENGR.


CURRENT
10-BASED STRATEGY
1969
1971
1973
1975
1977
1979
1981
$100K
$ 40K
$ 15K
$ 5K
$ 2K
PRICE
20
40
PDQ
45
70
85
05
PDQ-
04
11
85
LW 2/19/75
FUNCTIONALITY


PROPOSED
32 BIT STRATEGY
1969
1971
1973
1975
1977
1979
1981
$100K
$ 40K
$ 15K
$ 5K
$ 2K
PRICE
20
40
PDQ
45
70
32
85
05
PDQ-
11
32
04
LW 2/19/75
FUNCTIONALITY

SINGLE USER

- PROVIDE LOWEST-PRICE SYSTEM
- "GO-DEC" - "GROW-DEC"
- RT-11 CLASSIC SYSTEM
- LSI-11 SUPPORT VIA RT/FLOPPY
- RSX-11D/RT-11 ENVIRONMENT
- REDUCE SERVICE COSTS/SUPPORT HIGH VOLUME

REAL TIME

- LSI-11 SUPPORT
  - TRIMMED RSX-11S (NOT RSX-11A)
  - RSX-11M FOR PROGRAM DEVELOPMENT
- SUBSTRATEGY IMPLICATIONS
  - RT-11 ENVIRONMENT
  - FILES IMPROVEMENTS
  - NETWORKS SUPPORT
- IMPROVE IAS PERFORMANCE
  - ADD BASIC-PLUS

TIME SHARING

- RSTS/E V7
  - . FILES-11 VERSION OF V6
  - . CLEAN UP BASIC-PLUS
  - . NETWORK SUPPORT
- SWITCH EMPHASIS TO TRANSACTION-PROCESSING
- DON'T DO FULL FAMILY

TRANSACTION PROCESSING

- DOMINANT MARKET PRESSURE
- MOVES US INTO COMMERCIAL APPLICATIONS
- INVOLVES
  - . NETWORKS
  - . DATA MANAGEMENT
  - . LANGUAGES
  - . UTILITIES
  - . OPERATING SYSTEMS
  - . HARDWARE
- TREAT IT AS ADVANCED DEVELOPMENT
  - . NOT A PRODUCT
  - . A THROW-AWAY

LANGUAGES

SCIENTIFIC

- CLEAN UP BASICs
- MORE HARDWARE SUPPORT
- PRODUCTIVITY AIDS
- ANTICIPATE NEW ANSI
- ANTICIPATE APL

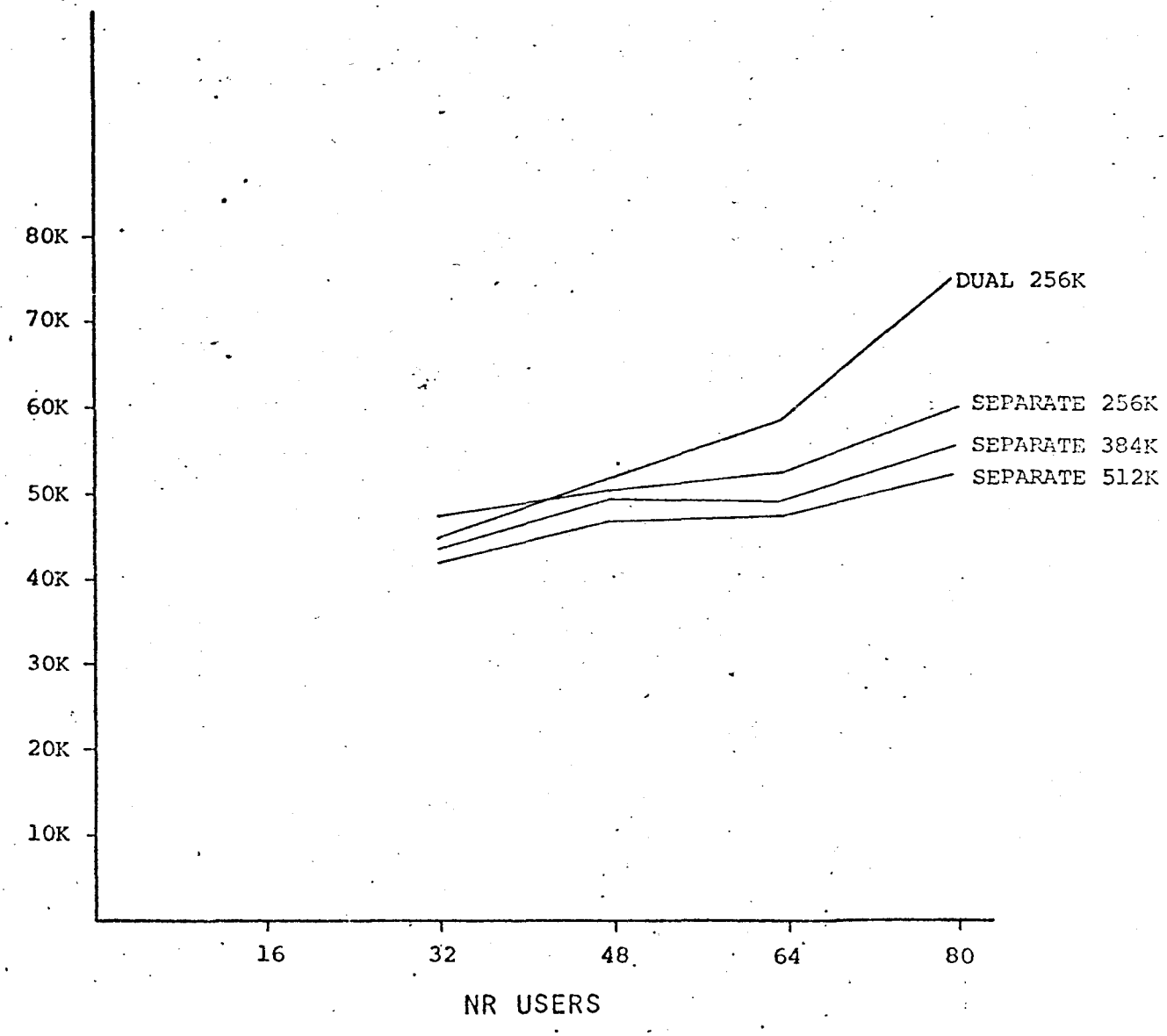
COMMERCIAL

- NEED ONE FOR ON-LINE APPLICATIONS
- REOPEN PL/1
- EVOLVE COBOL (INDEXED I/O)
- MINI-COBOL

CATALOG NO.15-1006-4
MADE IN U.S.A.

R+

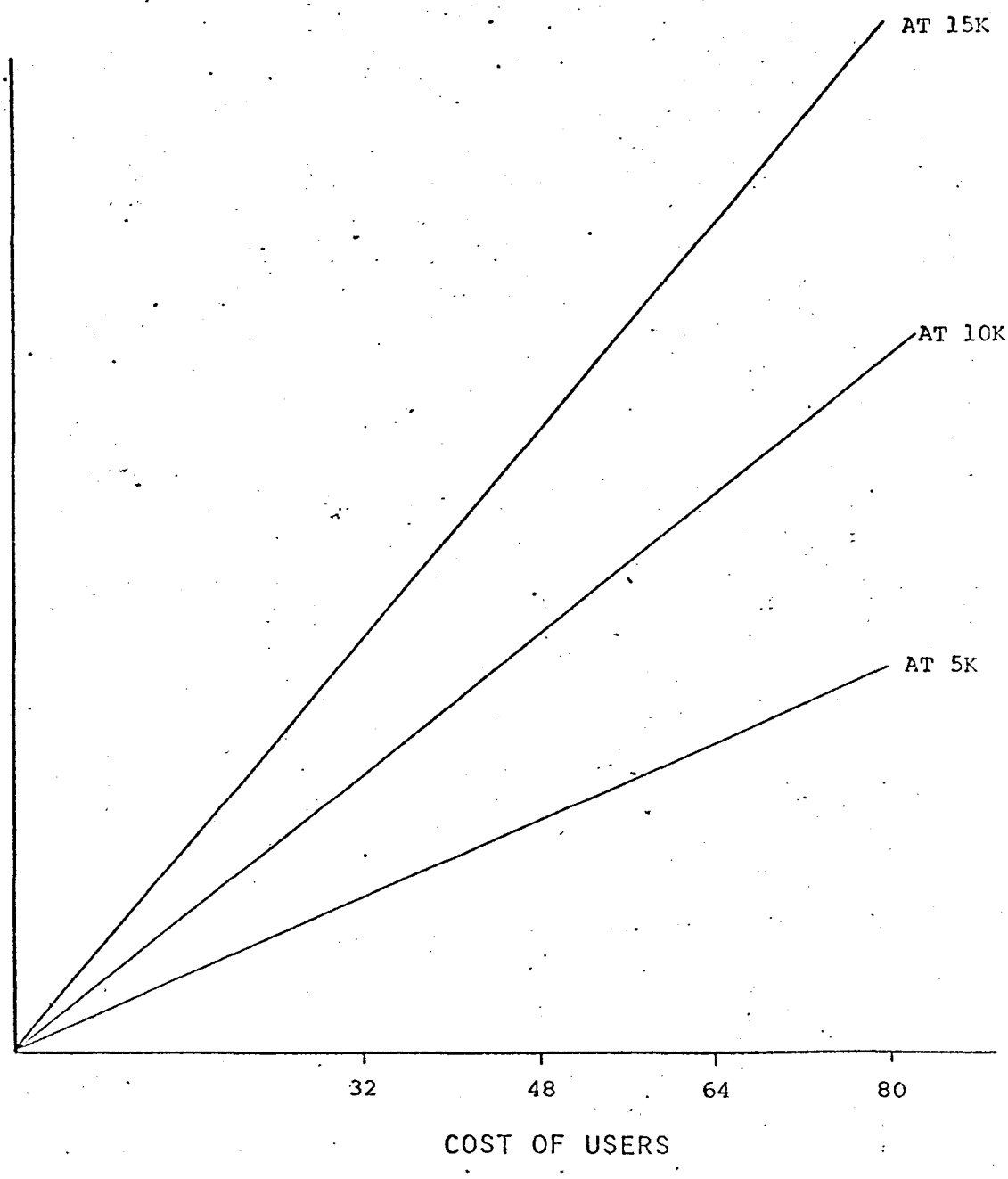
COST/EFFECTIVENESS



COMP CENTER COST
PLUS USERS AT 15K

NOTES

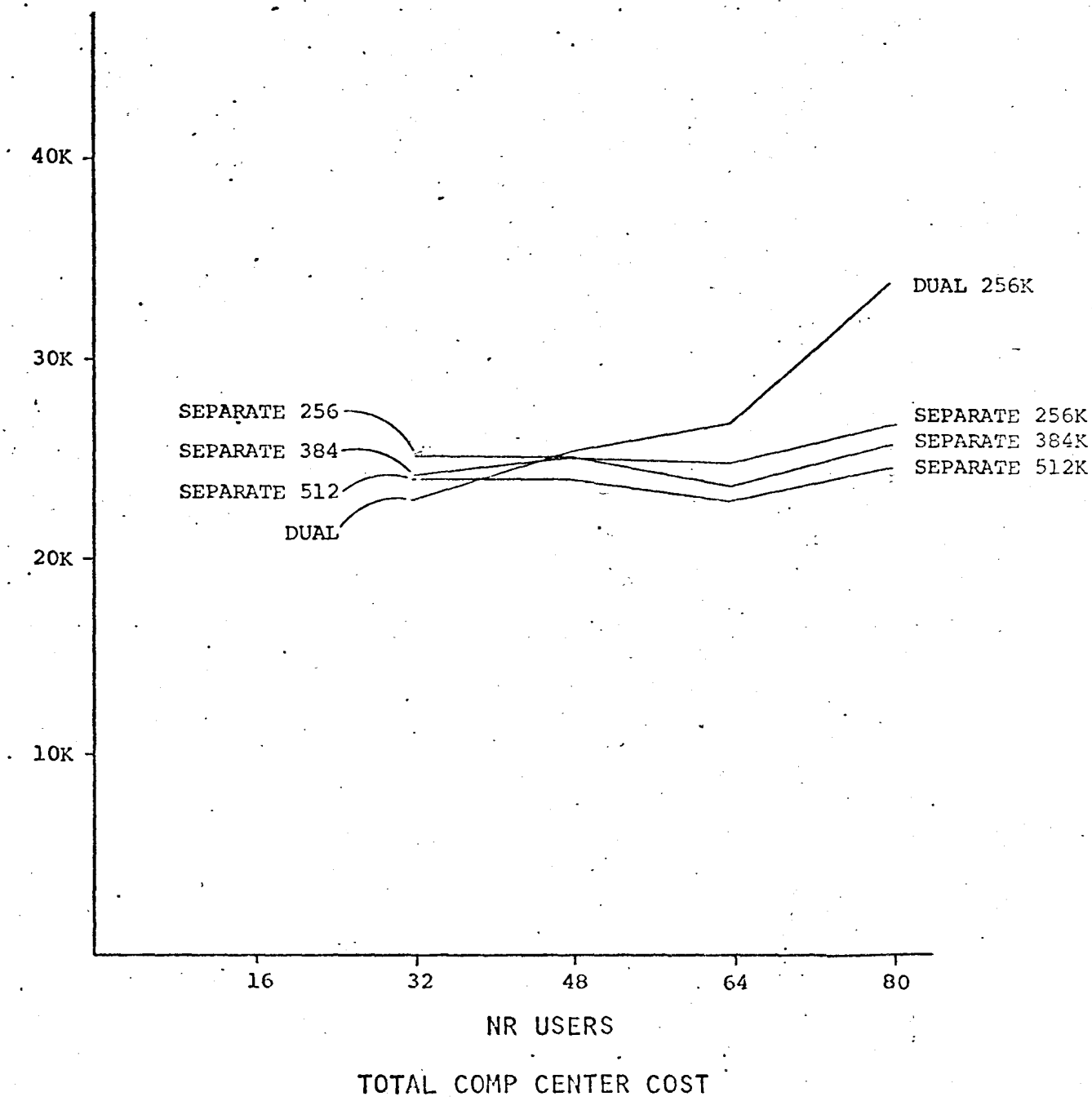
CATALOG NO.15-1006-4
MADE IN U.S.A.



NOTES

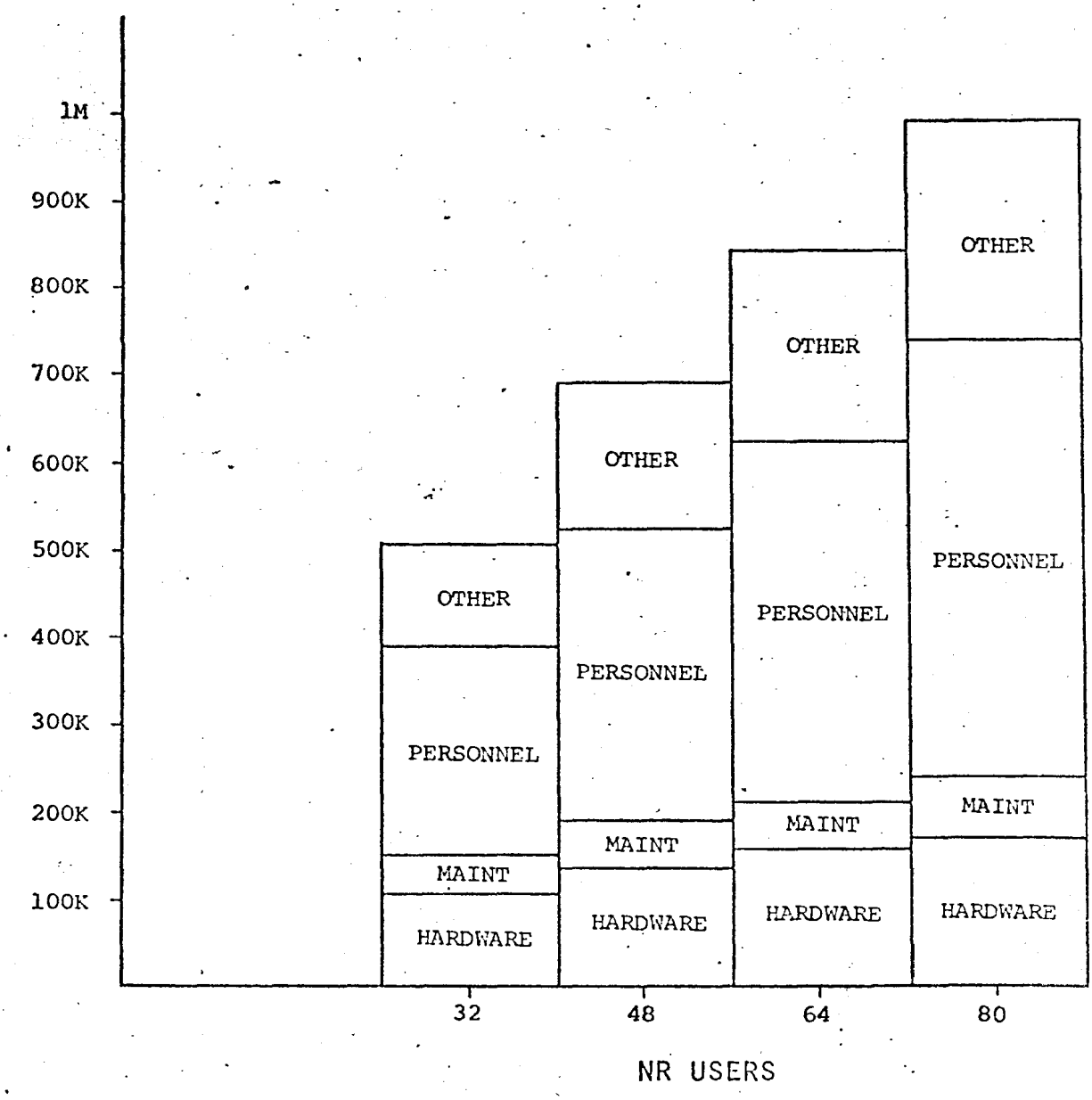
JBJECT ----------

COST/EFFECTIVENESS



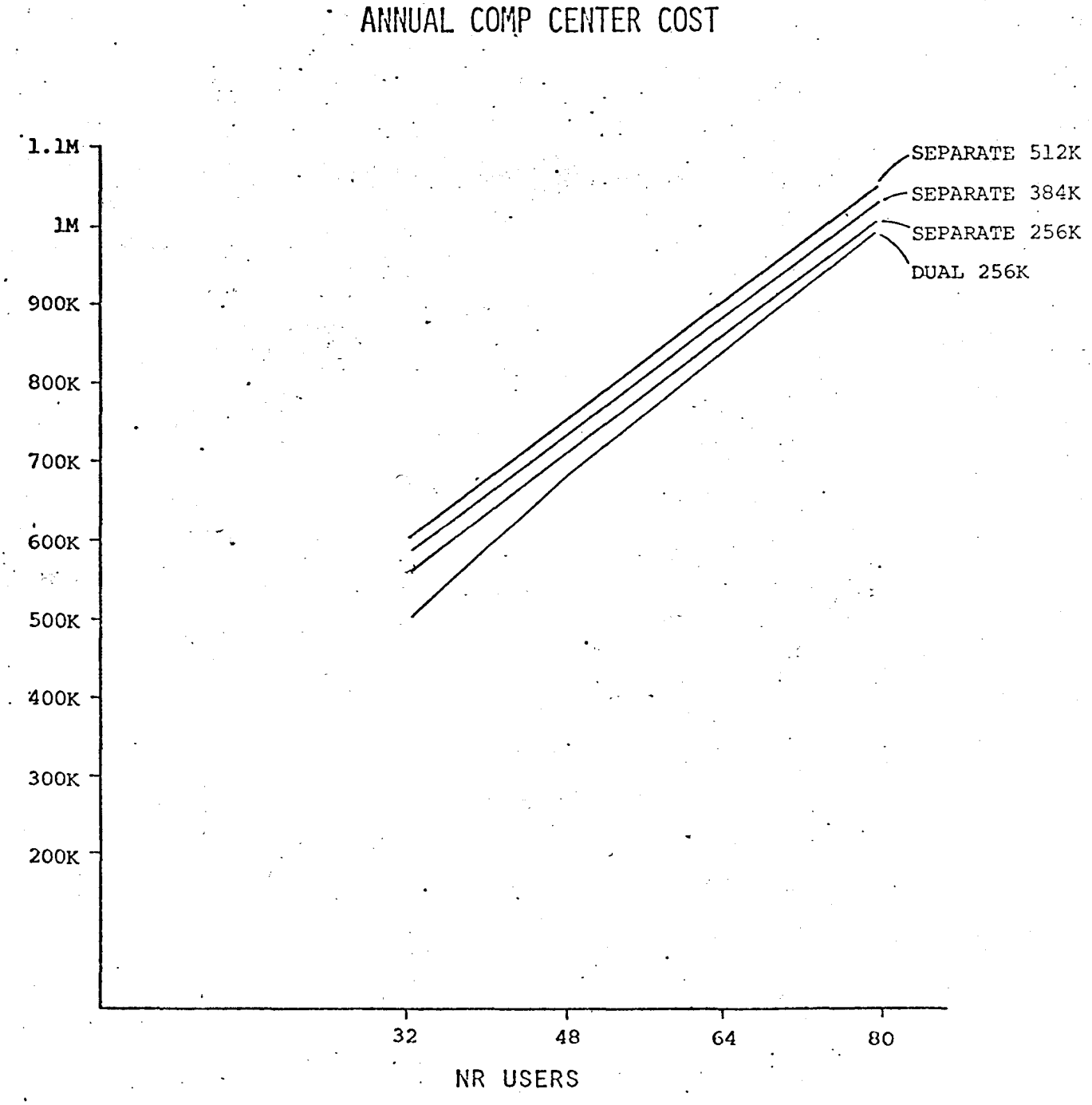
NOTES

COMP CENTER COST COMPONENTS



DUAL PROCESSOR 256K

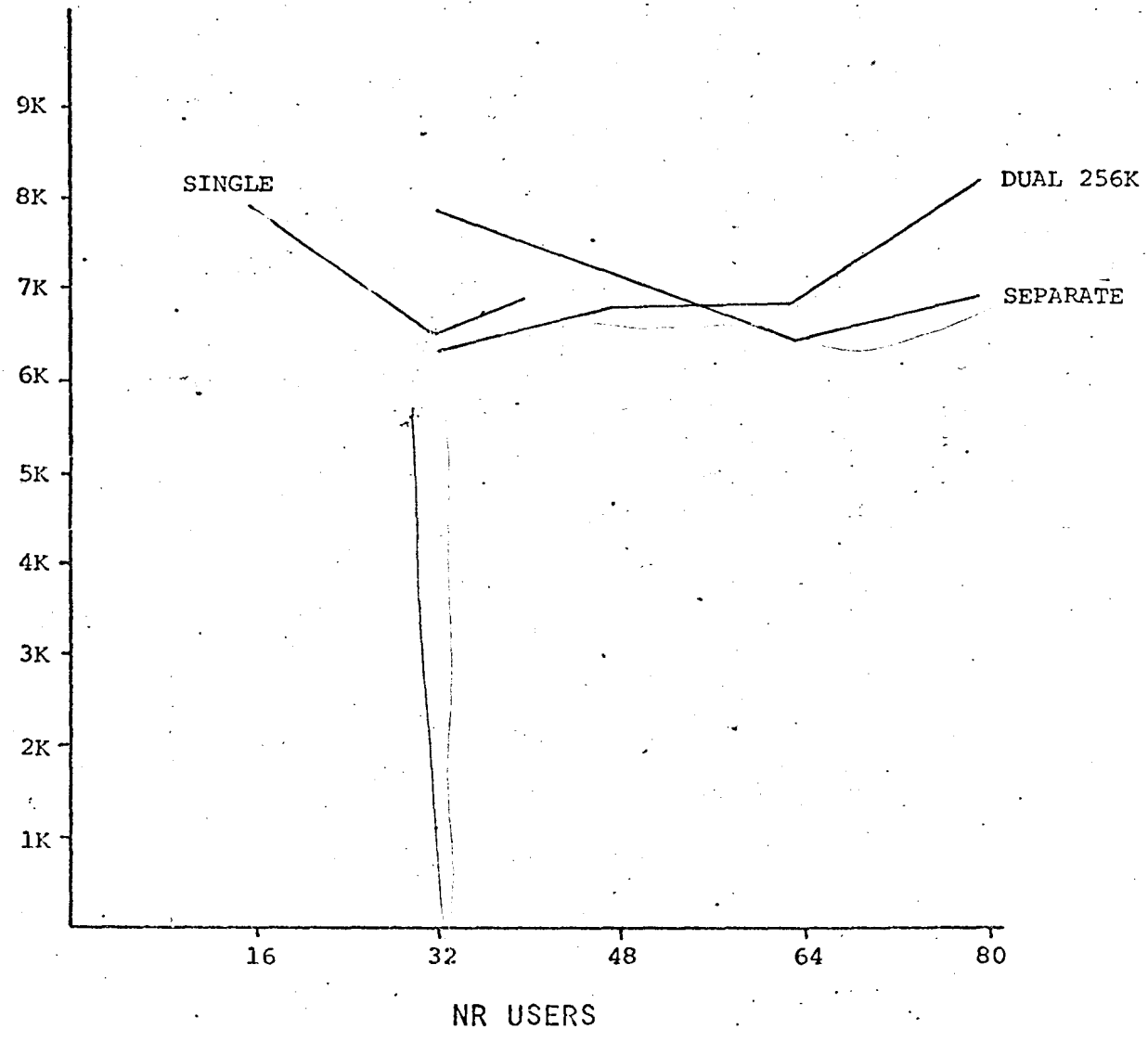
3M CENTER • ST. PAUL, MINNESOTA 55101
CATALOG NO.15-1006-4
MADE IN U.S.A.



NOTES

UBJECT ----------

COST/EFFECTIVENESS



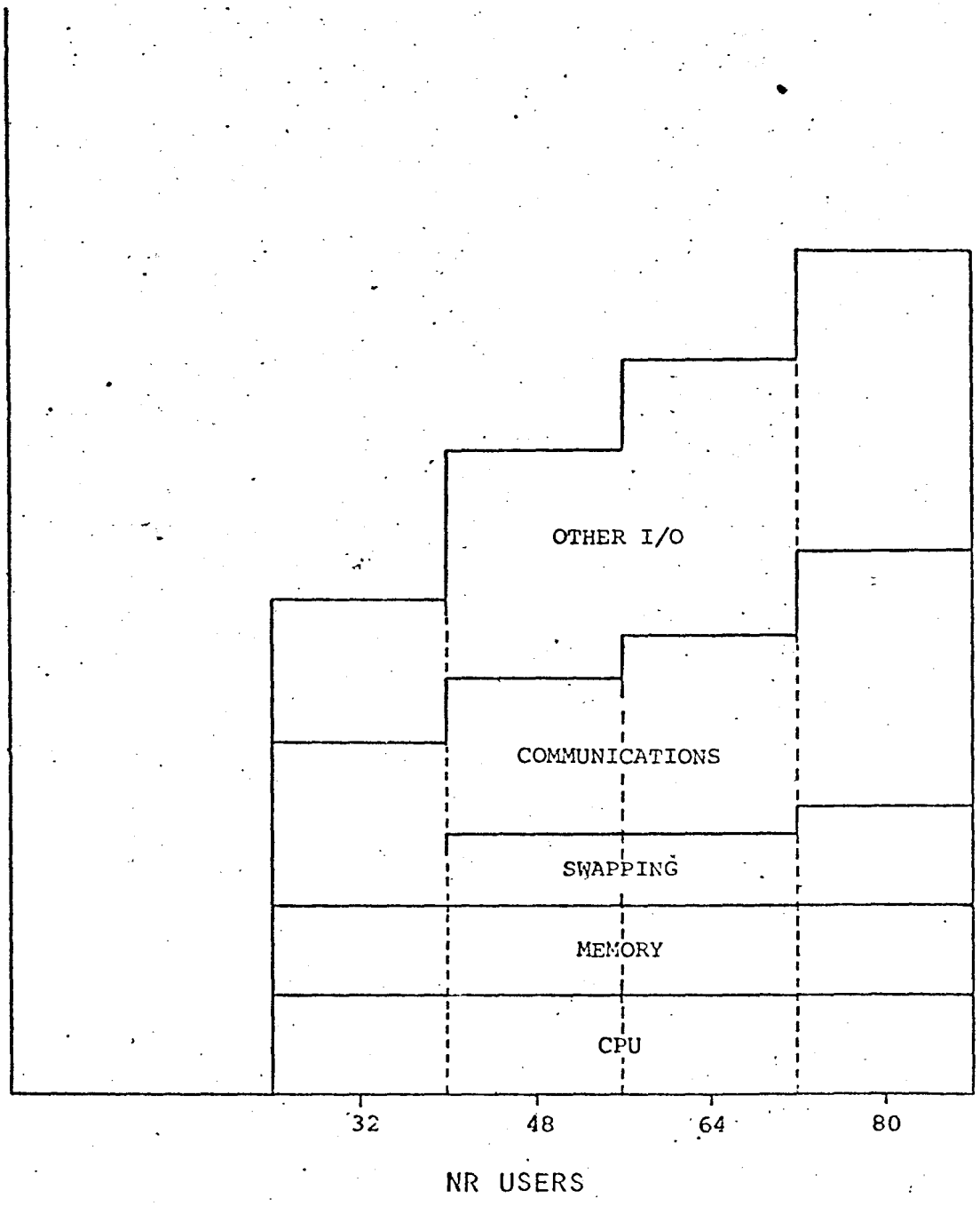
- SYSTEM COST ONLY -

NOTES

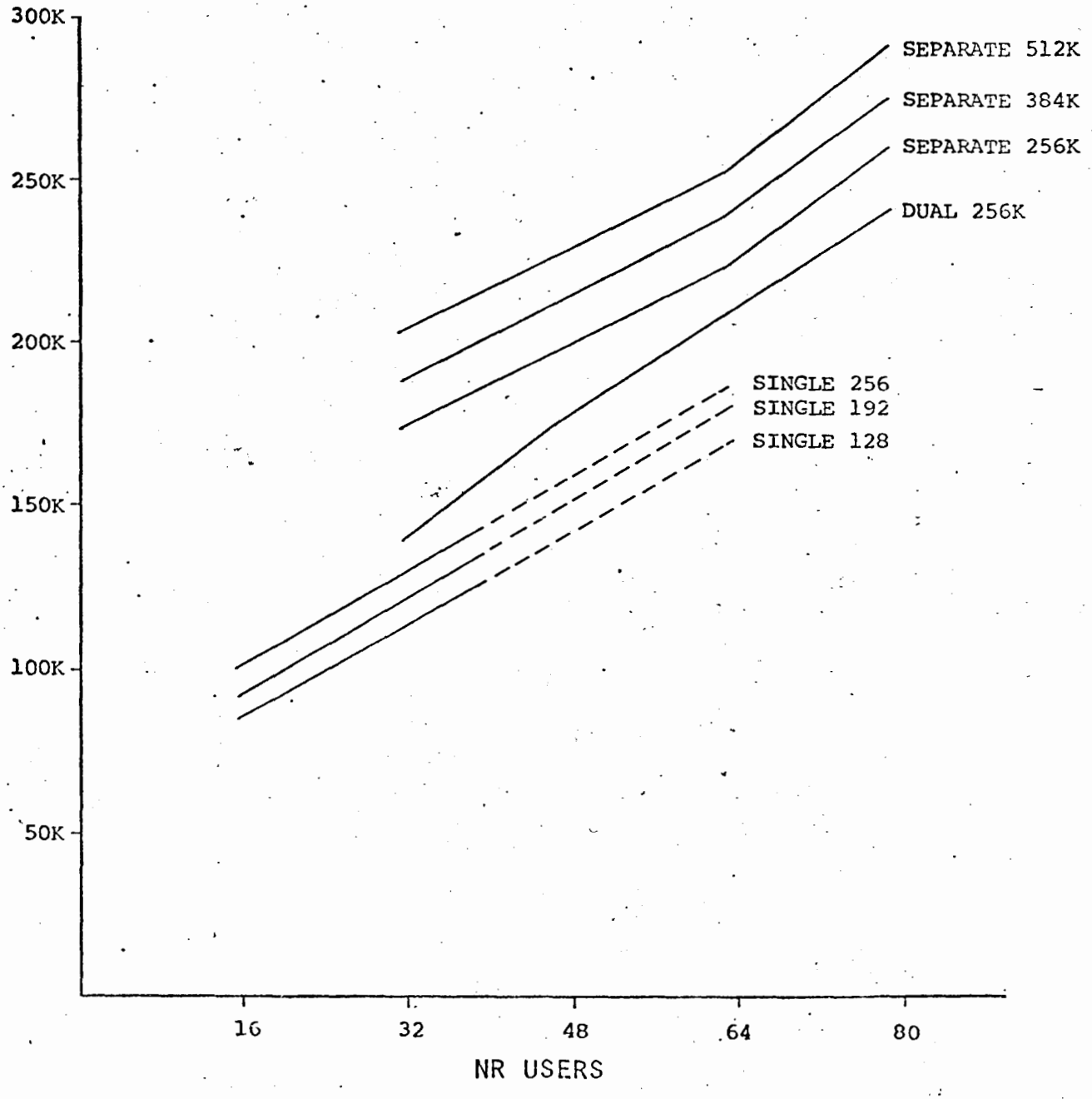
CATALOG NO.15-1006-4
MADE IN U.S.A.

COMPONENTS OF ANNUAL SYSTEM COST

256K DUAL CPU SYSTEM

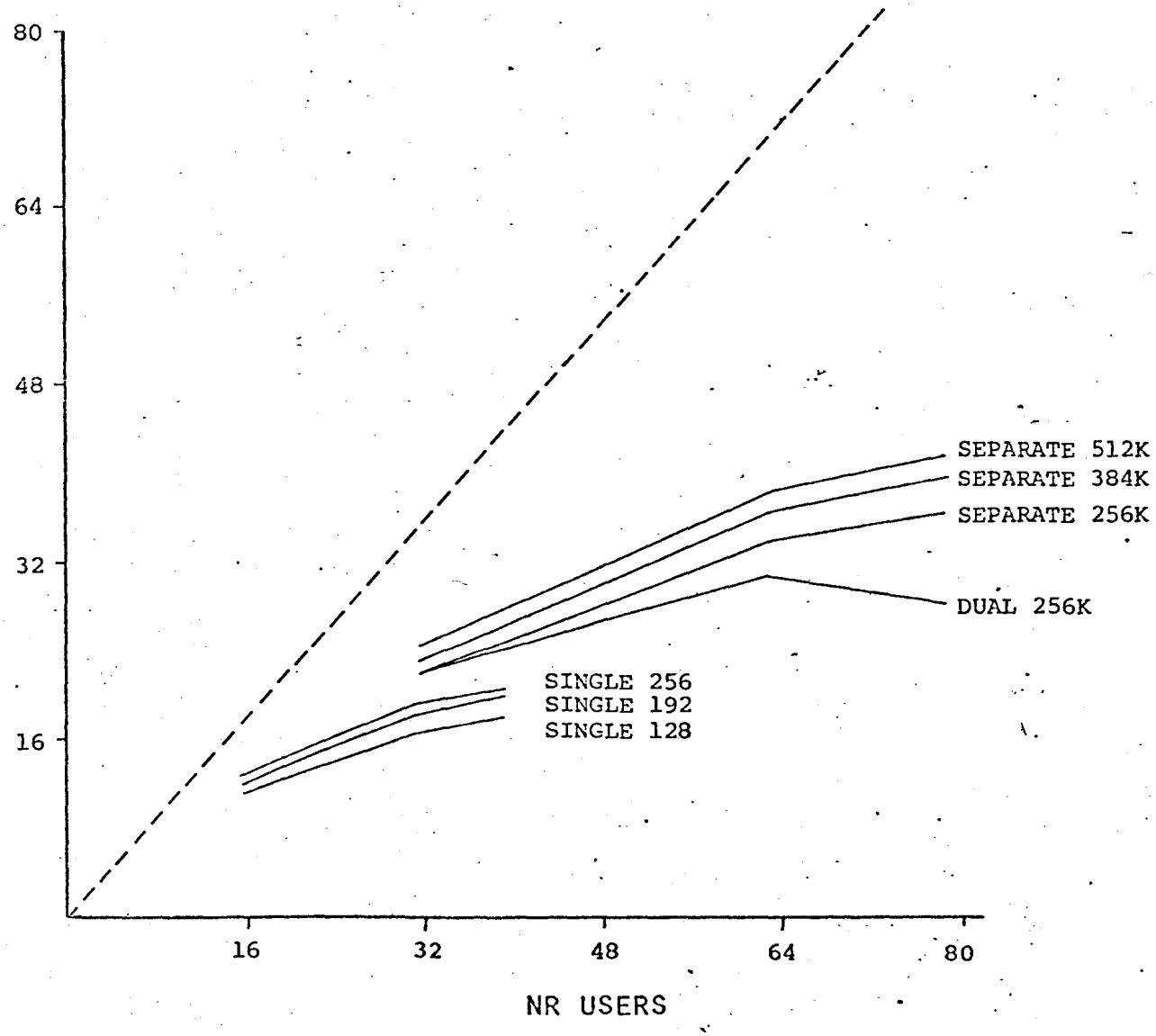


NOTES


ANNUAL SYSTEM COST
300K
250K
200K
150K
100K
50K
SEPARATE 512K
SEPARATE 384K
SEPARATE 256K
DUAL 256K
SINGLE 256
SINGLE 192
SINGLE 128
16
32
48
64
80
NR USERS

NOTES

"EFFECTIVENESS" INDEX



NOTES

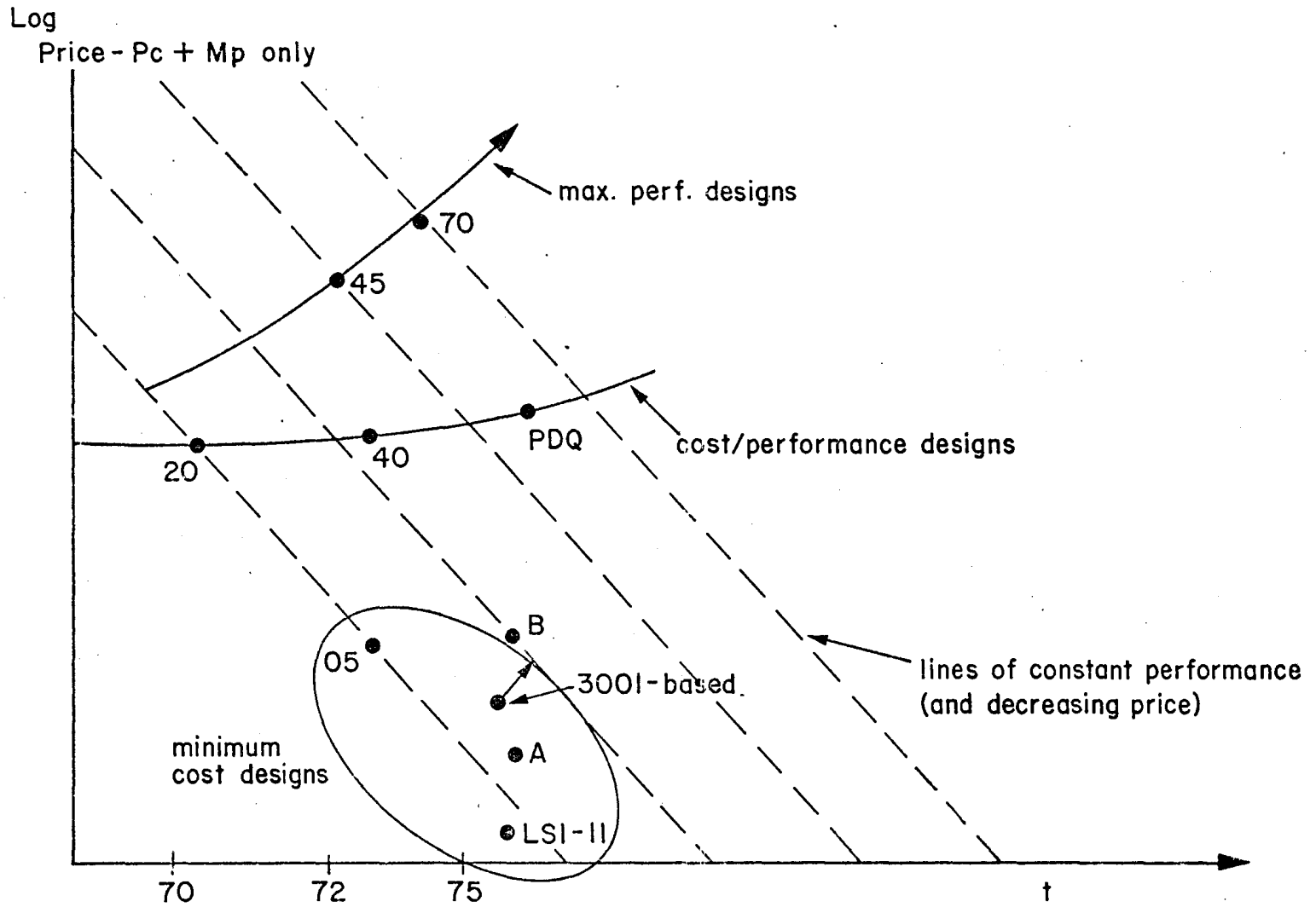
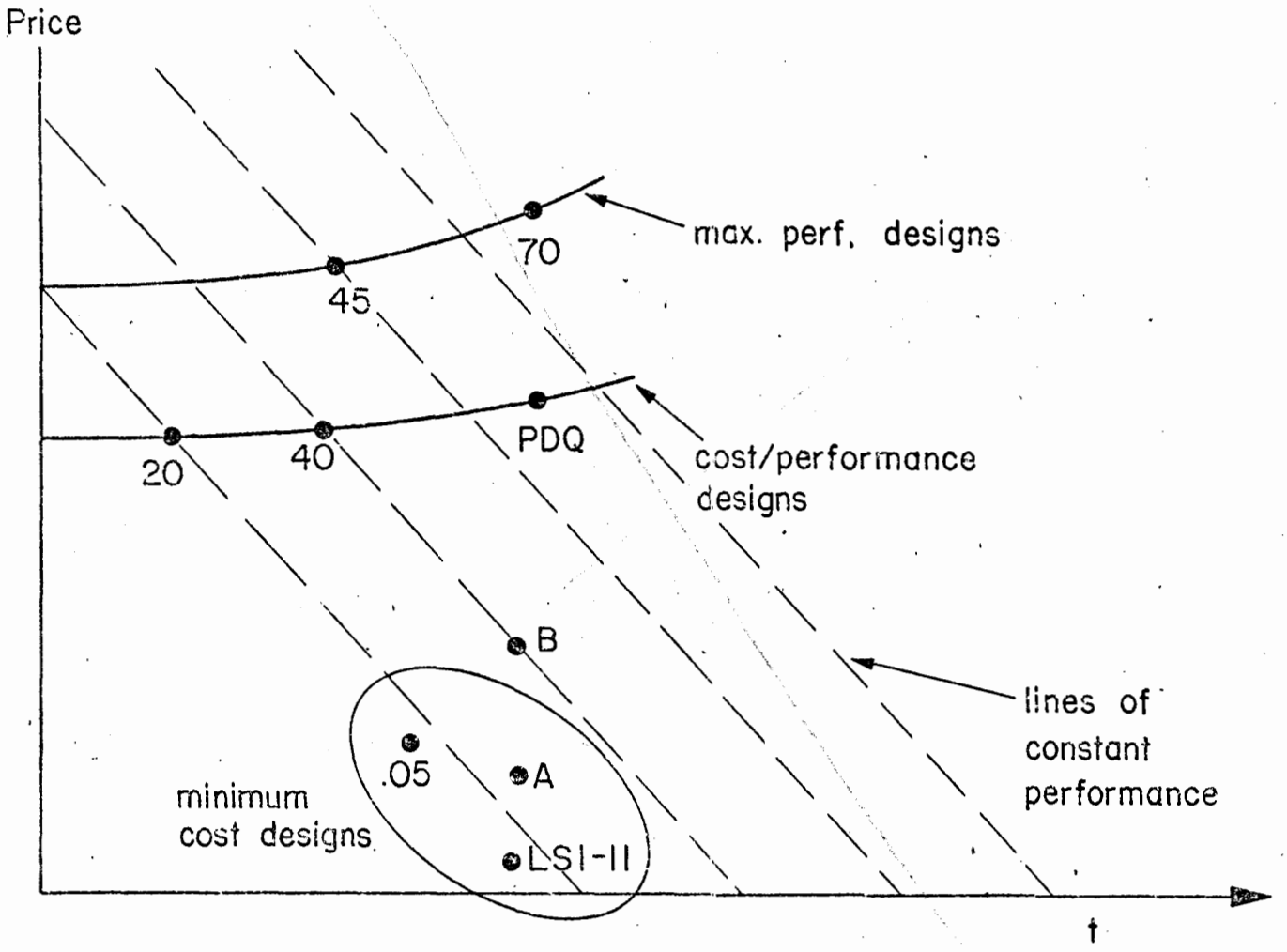


Fig. MODELS PDP-11 MODELS PRICE VERSUS TIME WITH LINES OF CONSTANT PERFORMANCE

Figure Models PDP-11 MODELS PRICE VERSUS TIME WITH LINES OF CONSTANT PERFORMANCE



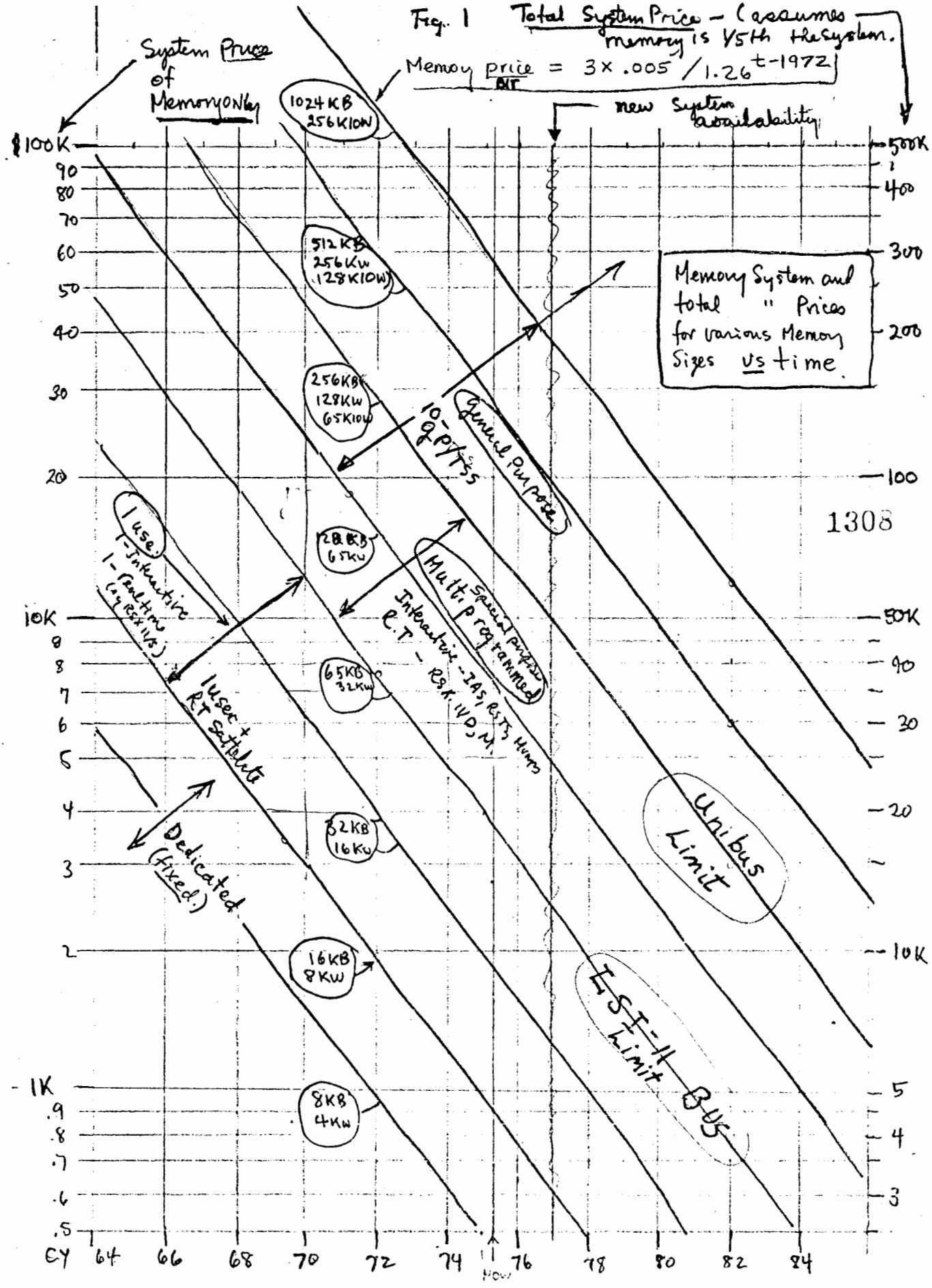


Fig. 1 Total System Price – (assumes memory is 1/5th the system.
Memory price = 3 × .005 / 1.26^(t-1972)
System Price of Memory Only
new System availability
Memory System and total " Prices for various Memory Sizes vs time.
1024 KB 256 K10W
512 KB 256 Kw 128 K10W
256 KB 128 Kw 65 K10W
128 KB 65 Kw
64 KB 32 Kw
32 KB 16 Kw
16 KB 8 Kw
8 KB 4 Kw
General Purpose
10-99 PDP's
Special Purpose Multi Programmed Interactive - RSX, RSTS, Hams C.T. - RSX, VDM
1 user T-Interactive I-(Batch or Interactive (e.g. RSX11S))
1 user + RT Satellite
Dedicated (fixed)
Unibus Limit
LSI-11 Limit Bus
$100K
90
80
70
60
50
40
30
20
10K
9
8
7
6
5
4
3
2
1K
.9
.8
.7
.6
.5
500K
400
300
200
100
50K
40
30
20
10K
5
4
3
CY 64 66 68 70 72 74 NOW 76 78 80 82 84
1308

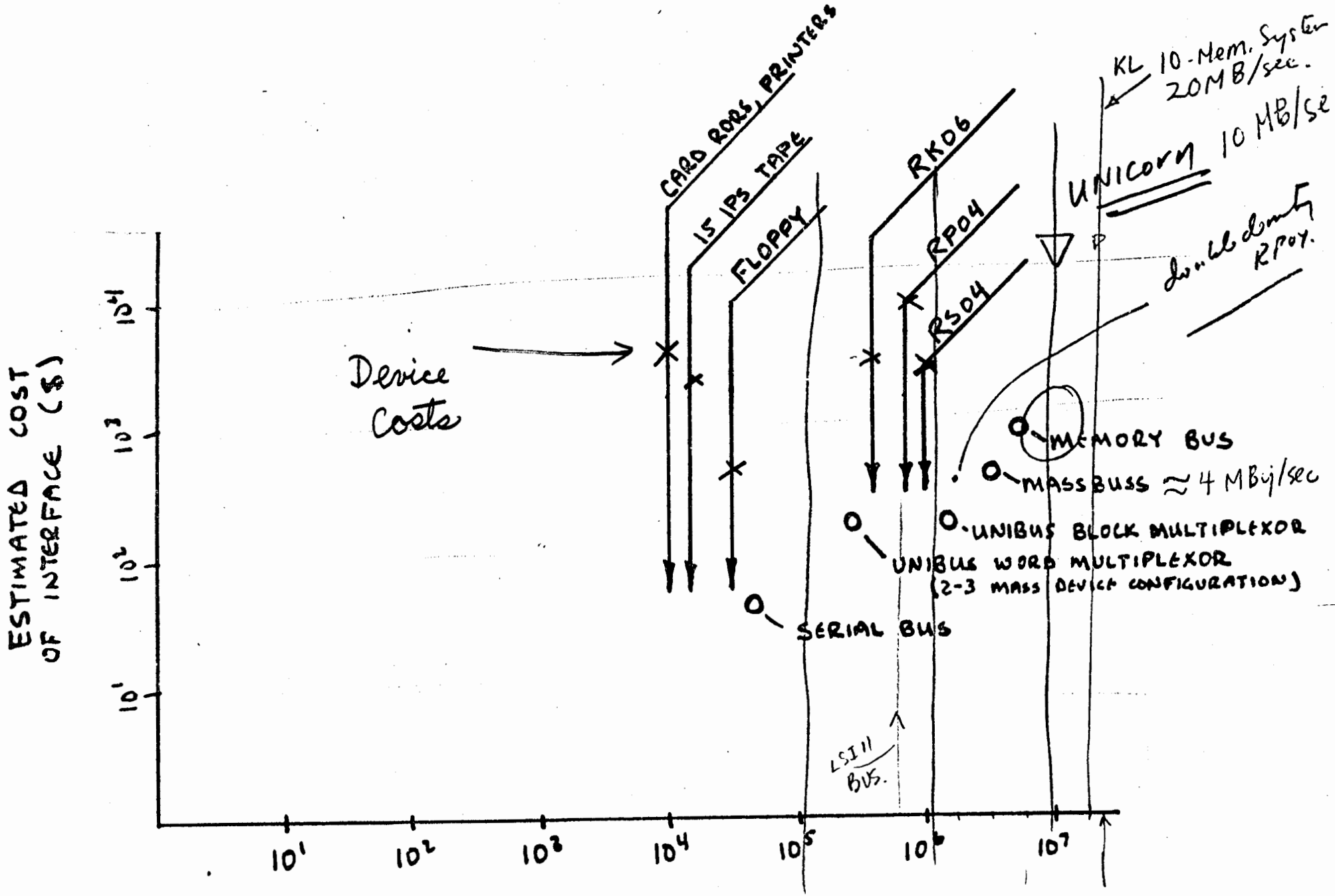


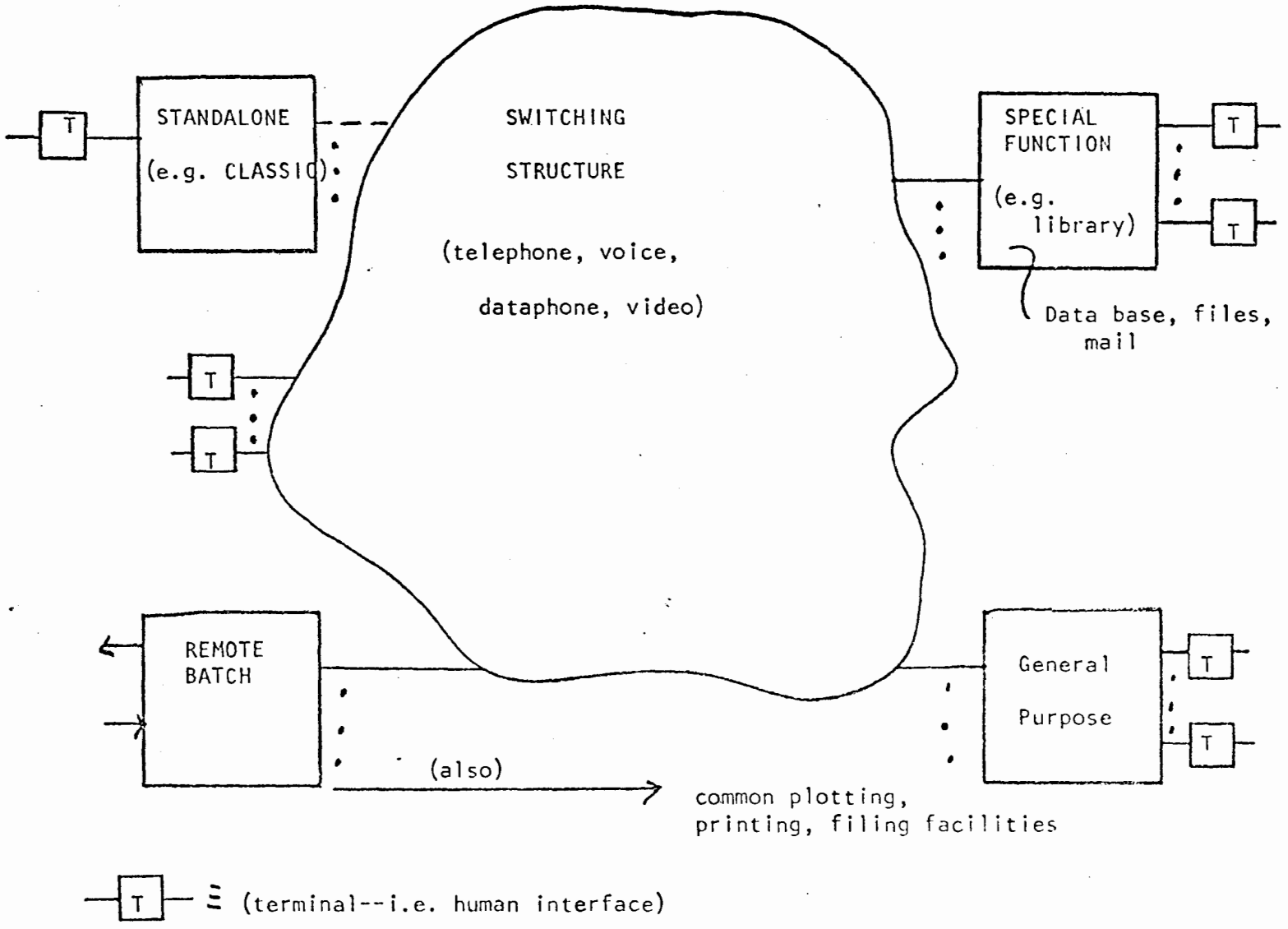
Fig 2.

Fig 2

D Nelson

1303

FIGURE 3 GENERAL STRUCTURE OF COMPUTATION FACILITIES



GB
5/8/75

TABLE 1 DISK TECHNOLOGY (1975)

DISK CONFIGURATION	PRICE (Roughly)	CAPACITY (Bits)	COST/ BIT	ACCESS TIME
Flexible (floppy)	3	2.5	1.2	1 s
1 Platter	6	30.0	.2	50 ms
3 - 5 Platters	12	160.0	.075	50 ms
10 Platters	24	800.0	.03	20 ms

GB
5/8/75

TABLE 2 YEARLY IMPROVEMENTS FOR VARIOUS COMPUTER TECHNOLOGY COMPONENTS

Technology Indicator	% Improvement
Semiconductor density	60 - 80
Semiconductor memory density (bits/chip--leading edge)	100 (1962 - 1974)
Magnetic recording density (disks)	41 (1962 - 1975)
Core (price)	30
Terminals	25
Magnetic tape (density) (data-rate)	23 (1952 - 1973) 29
Power Supply (cost/watt)	-3
Packaging (cost/in↑3)	-3
Minicomputers	31 (1960-1975)

GB
5/8/75

Table 3--SYSTEM STRUCTURE, MEMORY SIZE, AND RESULTANT USE

Structure	Memory Range	Function (use)	
Dedicated (fixed-] use)	16KB (4KB - 8KB)	Unteractive--e.g. POS Real time--e.g. scope, traffic control, automobile	Special purpose, Fixed
Programmable (1 user)	16KB - 65KB	Interactive--RT11 Real time--RSX11S,M	Small scale, generality
Dedicated (multiprogrammed n-users)	65KB - 256KB	Interactive--MUMPS, Trans. Process n RSTS Real time--RSX-11M, D	Special purpose
Programmable (multiprogrammed n-users)	128KB - 1024KB	Interactive--IAS, TOPS 10, RSTS Real time--RSX-11D	Generality

There are many implications of the 4 categories of structure and the 2-sub categories as to the operating system, its overall system structure, etc.

GB
3/24/75

TABLE 4 LARGE AND SMALL COMPUTERS 1967 AND 1975

Circa 1967	COST	WL	Mp Size	Bits/$	MIPS	MIPS X WL	REAL (MIPS)	P/C (MIPS/M$)
8	10^4(1)	12 (1)	$5X10^4$(1)	5	$.3X10^6$(1)	(1)	10^3(1)	30
6600	$3X10^6$(300)	60 (5)	$8X10^6$(160)	2 2/3	$3X10^6$(10)	(50)	$3X10^6$(3000)	1
Circa 1975								
BRD	10^3(1)	16 (1)	$4X10^3$w(1)	64	.3 (1)			100
Large	10^7(10^4)	64 (4)	$1X10^6$w(10^3)	6.4	100 (10^4)			10

Some Observations:

1. Performance: small is about the same. Large up 10~30.
2. Cost: small is cheaper by X10. Large up X3.
3. Mp. size no economy of scale.

GB
5/8/75

TABLE 5 OPERATING COSTS FOR COMPUTING

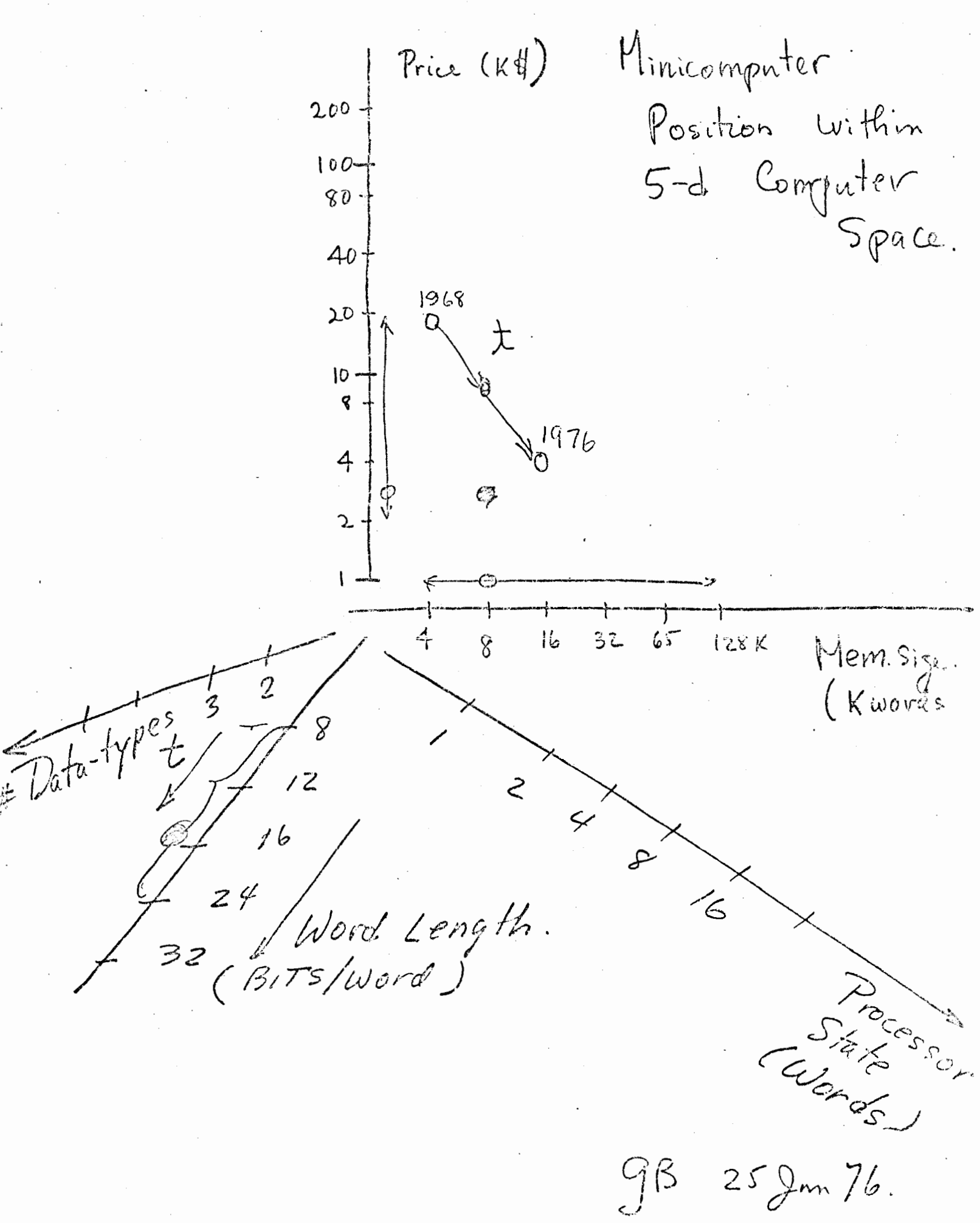
(1K)	COST/Year	COST/HR. @ 2400 HR.
Human	0, 5, 10, 20, 40	0, 2, 4, 8, 16
Computer	1.2 ~ 2.5	.5 ~ 1.
Terminal	.25 ~ .75	.1 ~ .4
Service	.05	.02
Power	.005 ~ .01	.002 ~ .004
Line	0 ~ 2.4	0 ~ 2.
Paper	0 ~ .1	1/3¢ ~ 3¢
Space	.05 ~ .1	.02 ~ .04

GB
5/8/75

TABLE 6 CHARACTERISTIC DIFFERENCES OF SMALL (decentralized) VERSUS LARGE (central) FOR COMPUTATION

Attribute	Small (Decentral)	Large (Central)
Performance	Greater average.	Greater peak Large memory (programs)
Cost	Economies through production. Lower, given a terminal is is needed for a system. f(COMM line, terminal, and memory costs).	Economy of scale for disk.
	Production limited.	Design limited.
	Overhead of maintenance on individual (hidden)	Explicit, central maintenance costs.
Use	Small (or 0) data bases.	Large, shared data base.
	Fixed, (well-defined) computation.	General (undefined) computation.
Non-use	Programming where tasks are unbounded.	Defined, bounded tasks.
Security	Private	Public

GB
5/8/75


Minicomputer
Position within
5-d Computer
Space.
Price (K$)
200
100
80
40
20
10
8
4
2
1
1968
1976
t
4
8
16
32
65
128K
Mem. Size
(Kwords)
Data-types
t
3
2
8
12
16
24
32
Word Length.
(BITS/word)
1
2
4
8
16
Processor
State
(words)

GB 25 Jan 76.

1. Production (Learning)

$E_n = k\, n^d$ = Eff. of nth unit

(Learning consts.)

---

2. Technology Forecasting

$T(t) = k\, e^{ct}$ = Technology at t

---

3. Technology Progress Fcn.

$T_n = a \cdot n^b$

[$b = 2.5$ for Computers]

$T_n = T(t)$ if $i = e^{\%_b t}$

BASIC PROBLEMS IN DEFINING (CHARACTERIZING)

(MINI) COMPUTERS

TECHNOLOGY CHANGES RAPIDLY--HENCE, PRICE AND SIZE FOR CONSTANT FUNCTION DECREASES RAPIDLY.

LIFETIME (AGES) VARY AMONG COMPARISONS

THE CONFIGURATIONS VARY WITH APPLICATION--MAKING $ FOR SYSTEM A POOR MEASURE.

MINI ANCESTRY INCLUDES: CONTROL, COMPUTATION, AND DATA PROCESSING.

WIDE IMPLEMENTATION RANGE ($ AND PERFORMANCE)

LEVELS-OF-INTEGRATION, MARKUPS AND MARKETING VARY

GB
1/26/76

Single Bus

+ Simplicity

+ Flex. for > # of structures ⇒ (parallelism; reliability; perf. via good comm.)

Mpt Peripheral Bus

+ Possibility for > parallelism

+ Less components/bus ⇒ Reliab.

LARGE - SMALL COMPARISON

Circa 1967	Cost	WL	Mp Size	Mp.size/ $ bits/$	MIPS	MIPS x WL	REAL(MIPS)	P/C (MIPS/M$)
8	10^4(1)	12 (1)	$5x10^4$(1)	5	$.3x10^6$(1)	(1)	10^3(1)	30
6600	$3x10^6$(300)	60 (5)	$8x10^6$(160)	2 2/3	$3x10^6$(10)	(50)	$3x10^6$(3000)	1
Circa 1975								
Brd	10^3(1)	16 (1)	$4x10^3$w(1)	64	.3 (1)	-		100
8600	10^7(10^4)	64 (4)	$1x10^6$w(10^3)	6.4	100(10^4)	-		10

SOME OBSERVATIONS

1. Performance: low end is about the same. High end up 10~30. Gap 10 ⟶ 300 (30)
2. Cost : low end is cheaper by x 10. High end up x 3. Gap 300 ⟶ 10,000 (30)
3. Mp. size no economy of scale.

GB
2/7/75

PMS-Level Computer Architecture

Basic Problem: Specifying Load

User: Buying (Selecting);
Balancing (#M, P, T);
Designing Structures (Front Ends, mP, closely Coupled, Nets)

Manufactures:
New design structures;
Reliable, - Present Interface

Objective Fcn: Price,
Availability, Performance,
Size (space & Power)

MINI APPLICATION ORIGINS

CONTROL (LOGGING, RECORDING, CONTROL — EG. LGP-30, RW-)

SMALL SCALE COMP. (LGP-30)

SMALL SCALE EDP (1401)

LAB. CONTROL + PROCESSING (EG. PDP-'s).

SWITCHING ↗

G.P. SHARED (EG. PDP-1)

[HOW USED vs. WHAT FOR]

INDUSTRIAL

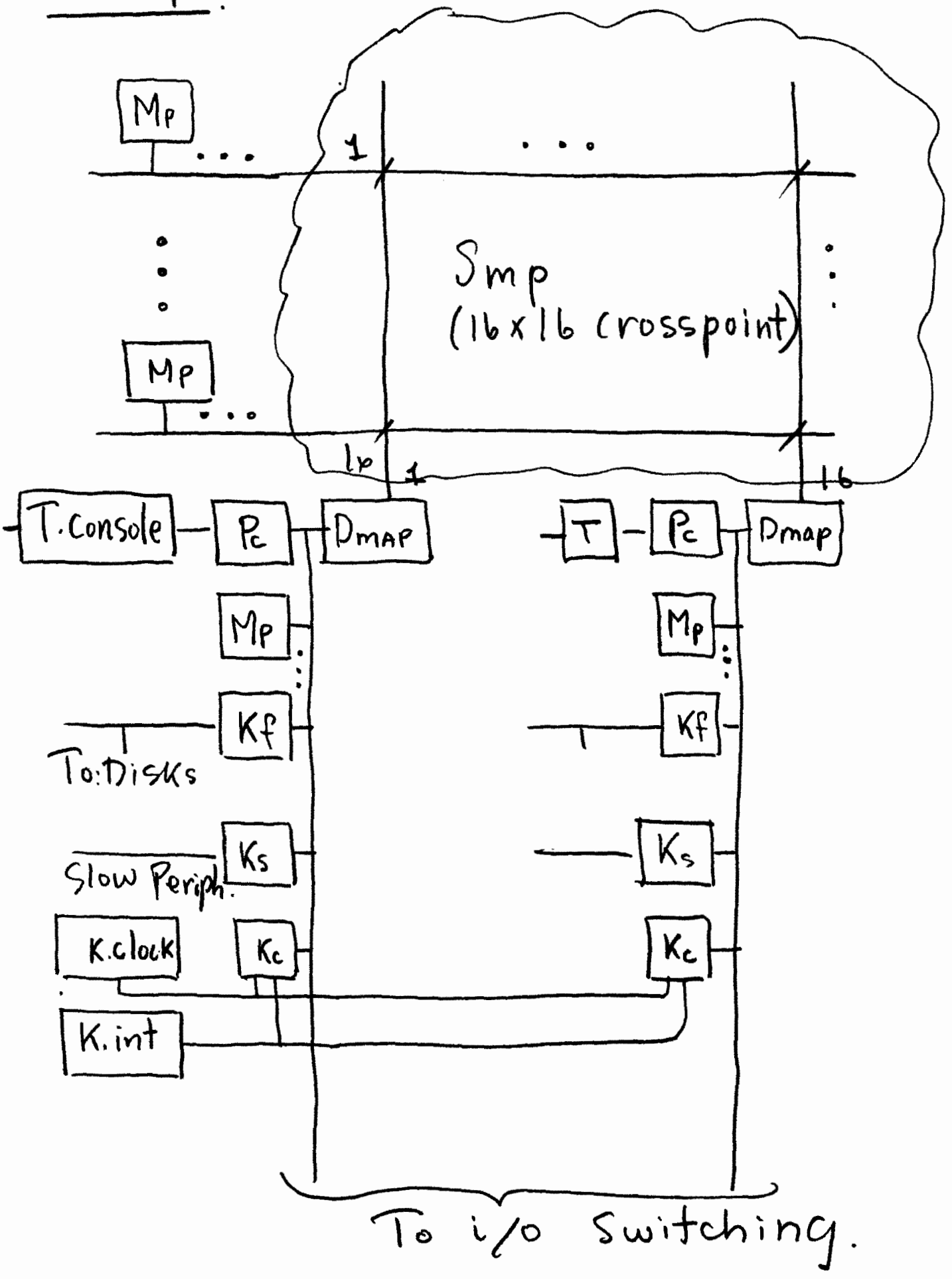
t
- T RANSDUCTION (DATA LOGGING)
- T + MEMORY (RECORDING)
- T + M + K (CONTROL)

- SWITCHING.
- S + MEMORY (ACCESS to DATA B.)

E D P
- T + D (DATA PROCESSING) — REPORTS
- T + D + P (PROCESSING)
- T + D + P + M (ACCESS TO DATA B.)

S c i.
- D - COMPUTATION
- T + D + M - DATA RECORDING.
- T + D + M + P - ON Line Control + Proc.

C.mmp


Mp
1
Smp
(16x16 crosspoint)
Mp
16
1
T.Console
Pc
Dmap
T
Pc
Dmap
Mp
Mp
Kf
Kf
To:Disks
Ks
Ks
Slow Periph.
K.clock
Kc
Kc
K.int
To i/o Switching.

P- Processor (eg. Cent., i/o)

M - Memory (eg. Core, Disk)

S - Switch (eg. Bus)

L - Link (eg. Comm. Intf.)

K - Control (i.e. FSM)

T - Transducer (eg. Terminal)

D - Data-operation

C := (M_p + P_c) - Computer

Examples of PMS Use

P(function: central)

P(central \c)

P(c)

P.c

Pc

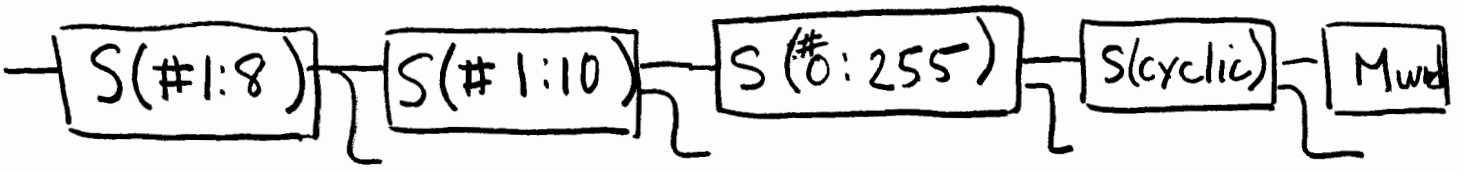
M(function: primary \p |
secondary \s | tertiary \t)

Mp | Ms | Mt

M := M.simple | SM

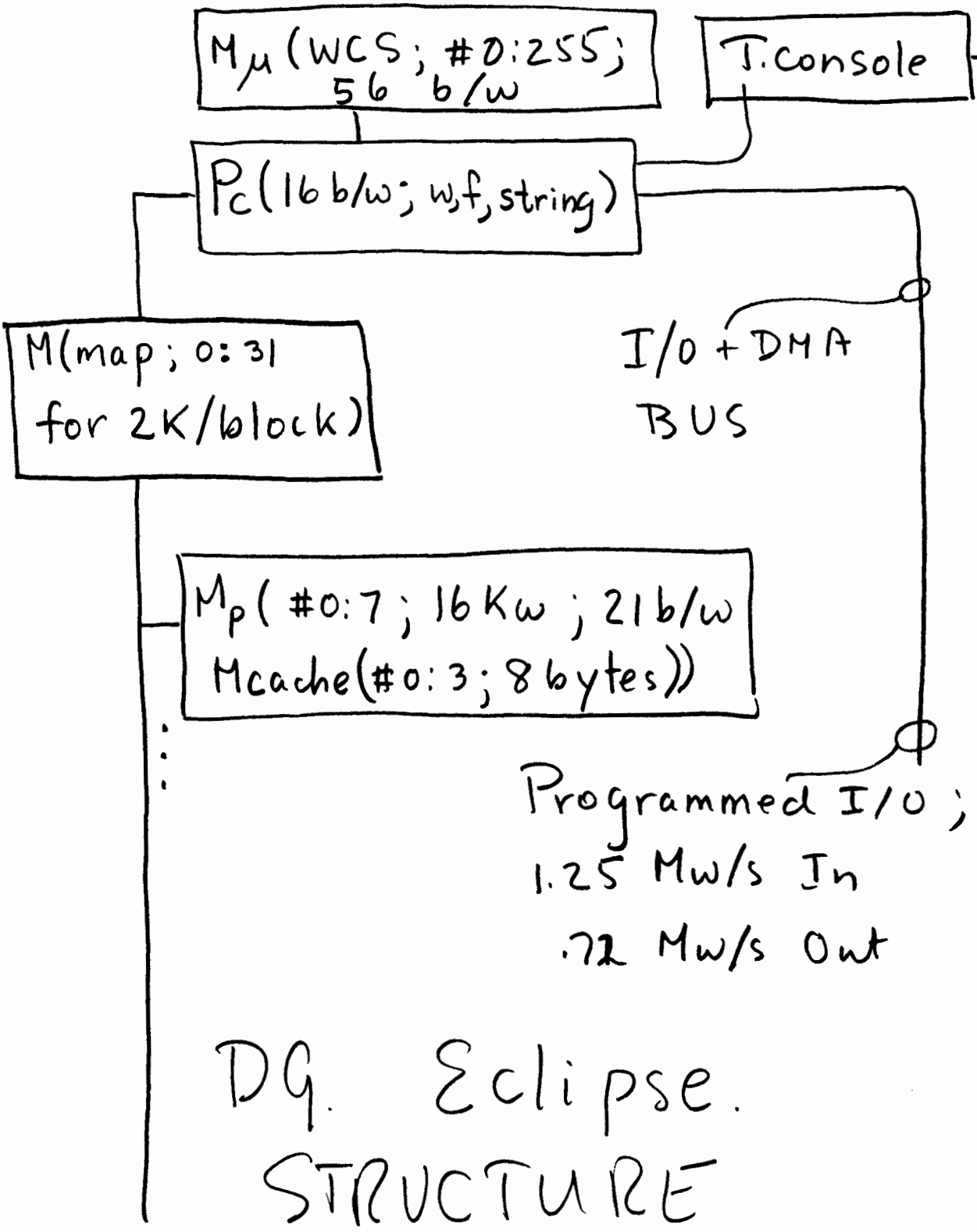
eg.

M(disk sub-system) :=

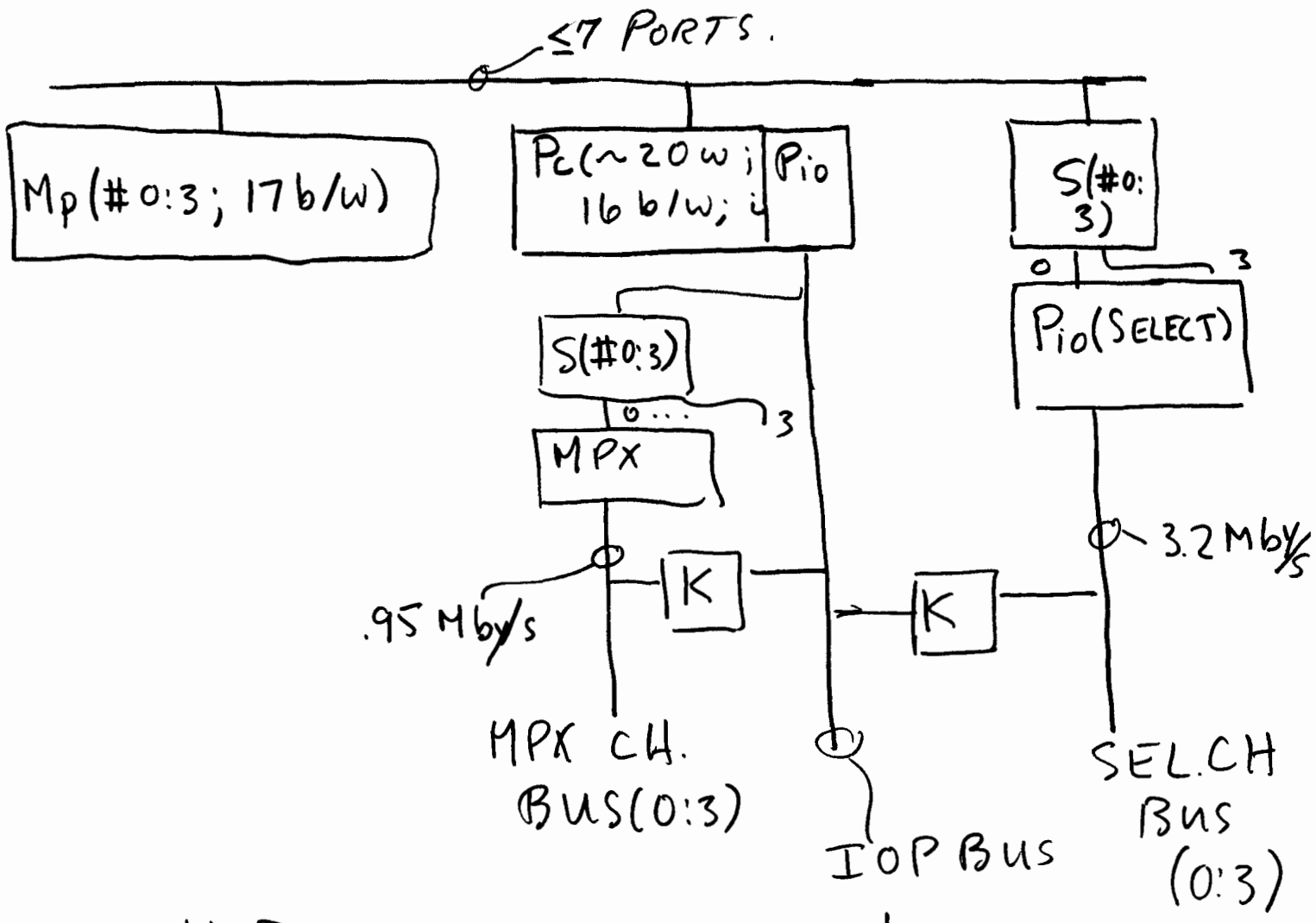


CONFIG.	Perf.	PRICE			PERF/PRICE (NORMAL.)		
		S	M	L	S	M	L
CORE	1	5	10	35	1	1	1
MOS	2	5	10	35	2	2	2
CACHE	5	10	15	40	2.5	3.3	4.3

PERF., PRICE & PERF/PRICE for CACHE-BASED, ETC. PDP-8's.



DG. Eclipse.
STRUCTURE



HP 3000 Structure.

BASIC RATIONALE FOR m P's

USER
- PERFORMANCE
- Δ PERFORMANCE AND RANGE
- AVAILABILITY VIA REDUNDANCY

MFG.
- COST (BETTER SPARES, MANUFACTURING)
- LESS DESIGNS

BASIC IRRATIONALE FOR m P's.

- NO-PROGRAMS
- HIGH DEV. RISK.
- UNIPROCESSORS ARE MORE COST/EFF.
- BETTER PLAN

$$\#\frac{\text{ACCESSES}}{\text{SEC}} = \frac{m}{t_c}\left(1-\left(1-\frac{1}{m}\right)^{P}\right)$$

$$= \frac{m}{t_c}\left(1-1/e\right) \quad \text{for } m=\infty \text{ and } P=m.$$

$$= \frac{m}{t_c} \times .67.$$

PARALLELISM: BASIS FOR MULTI-PC's

STATIC (I.E. RELIABLE)

- INDEPENDENT PARTITIONS: — DYNAMIC STOCKROOM.
- FUNCTIONAL SEPERATION - FRONT/BACK END / PRE-PROC. /

- INDEPENDENT
  - JOBS (T/S)
  - PROCESSES (TRANSACTION PROC.)
  - BATCH STREAMS
- SET PARALLELISM (PROC. CONT)
- ARRAYS, VECTORS
- GENERALLY CONCURRENT PROCESSES.

BALANCING $P_c - M_p - I/O$ (BUSSES)

BUS OPTIMALITY (AMDAHL'S CONST's)

1 Byte of Mp = 1-i/sec (use 2)

1 Bit of (i/o) = 1-i/sec

---

1 i = 3~5 bytes of accessing.

1 i = 4~6 bytes with i/o.

UNIBUS ≈ 2 Mbytes/sec.

≈ 1/2 ~ 1/3 · MEGA.-INST./SEC.

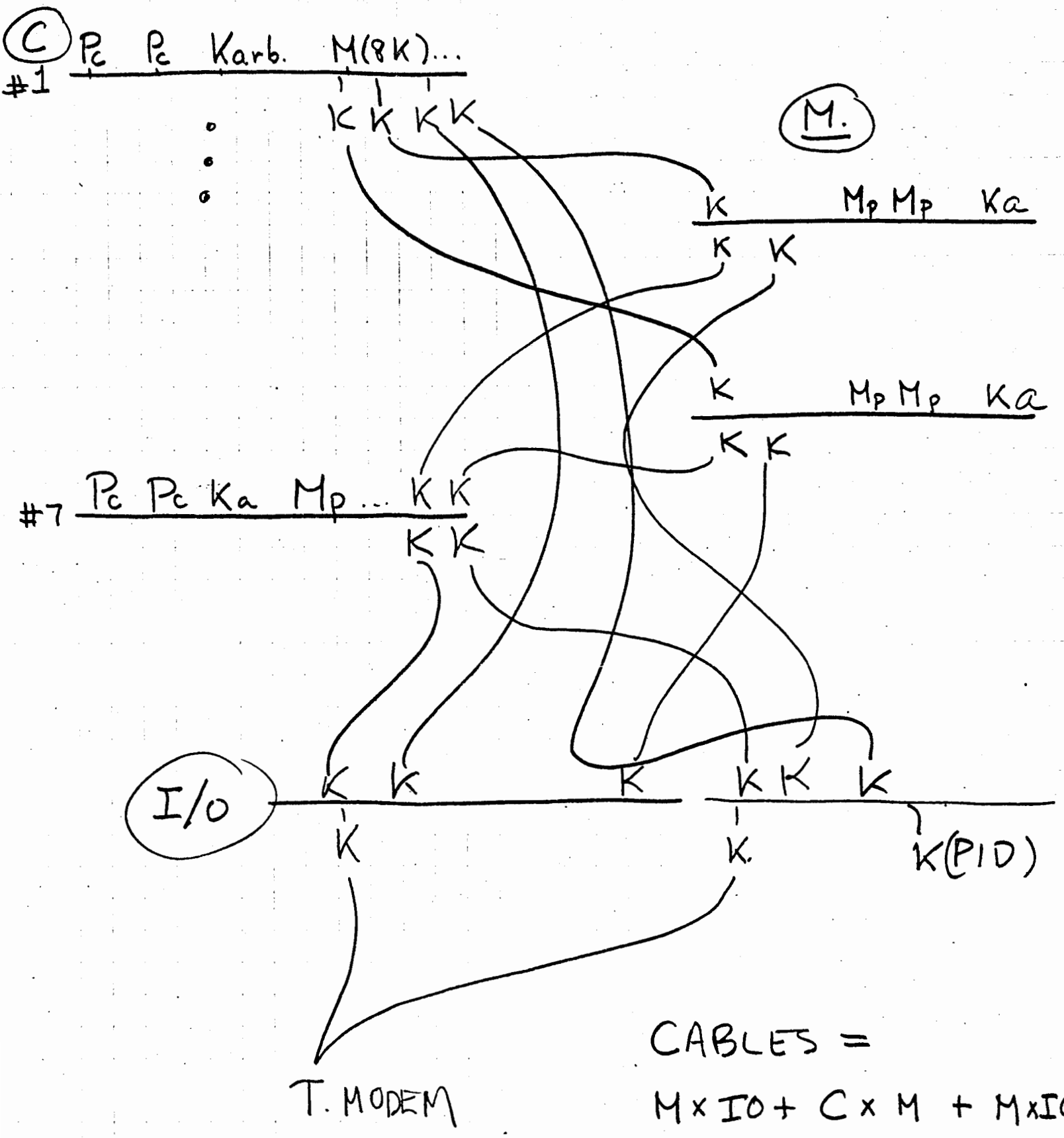
~~(IMPLIED~~ VIA BUS.

∴ 1/2 ~ 1/3 MEGA BYTES ARE REQ'D

UNIBUS = 1/4 MEGA BYTES.

11/70 ≈ 2 Mbytes. ⇒ 2 Mips.

CACHE Acts TO REDUCE BW.



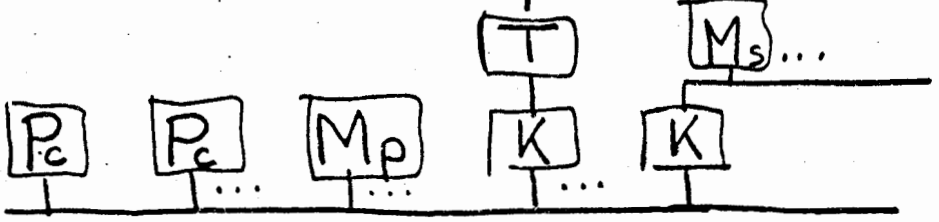
CABLES =

$M \times IO + C \times M + M \times IO$

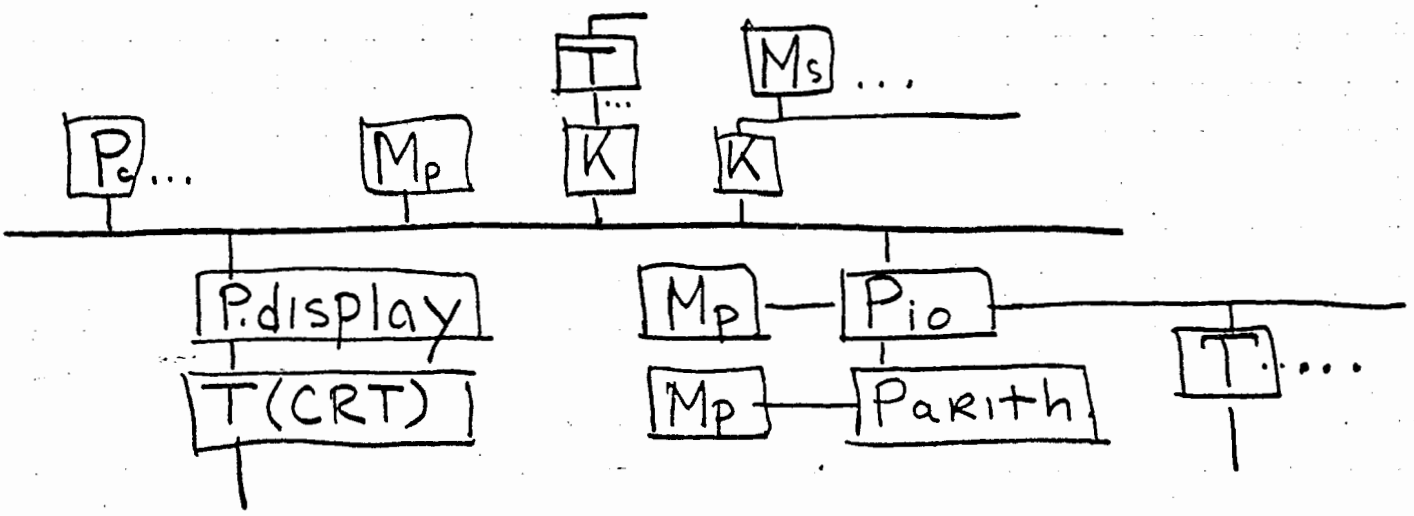
$2 \times 2 + 7 \times 2 + 2 \times 8$

$= 22$

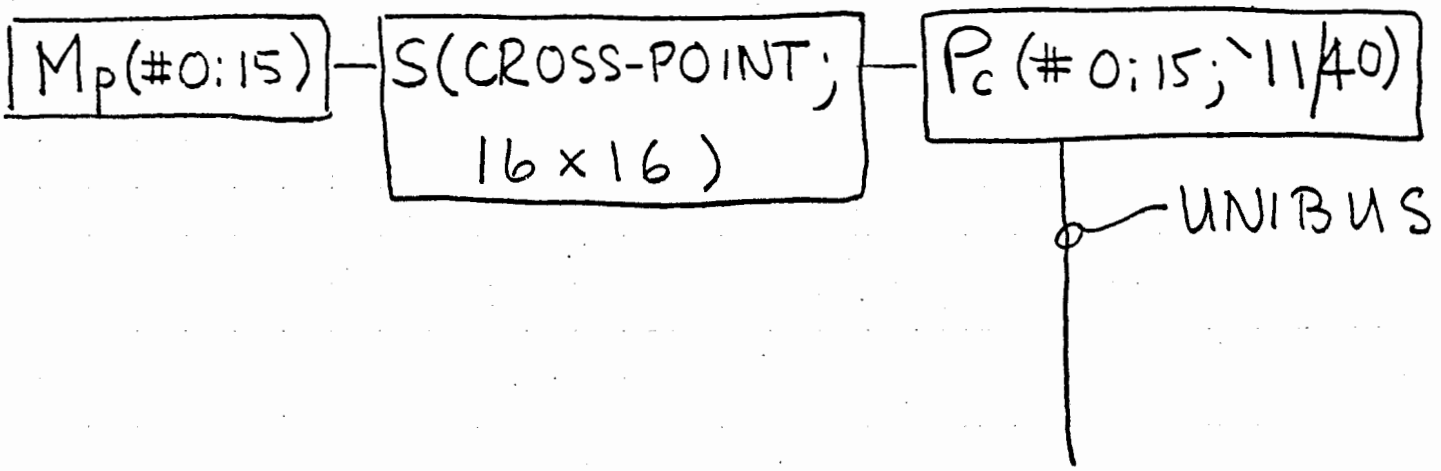
PLURIBUS SYSTEM. (BBN)



MULTI- Pc USING 1 BUS

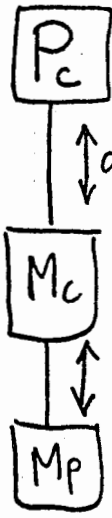


MULTI- SPECIAL Pc , 1 BUS



MULTI-Pc WITH 16 Mp's.

LEE '69



R = RATIO OF t.slow / t.fast.

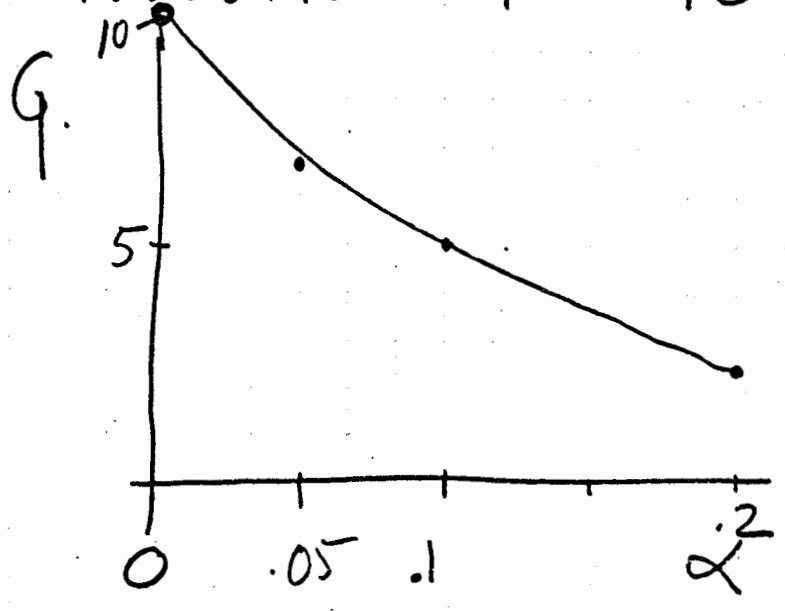
$$t(\text{No } M_c) = R \cdot a$$

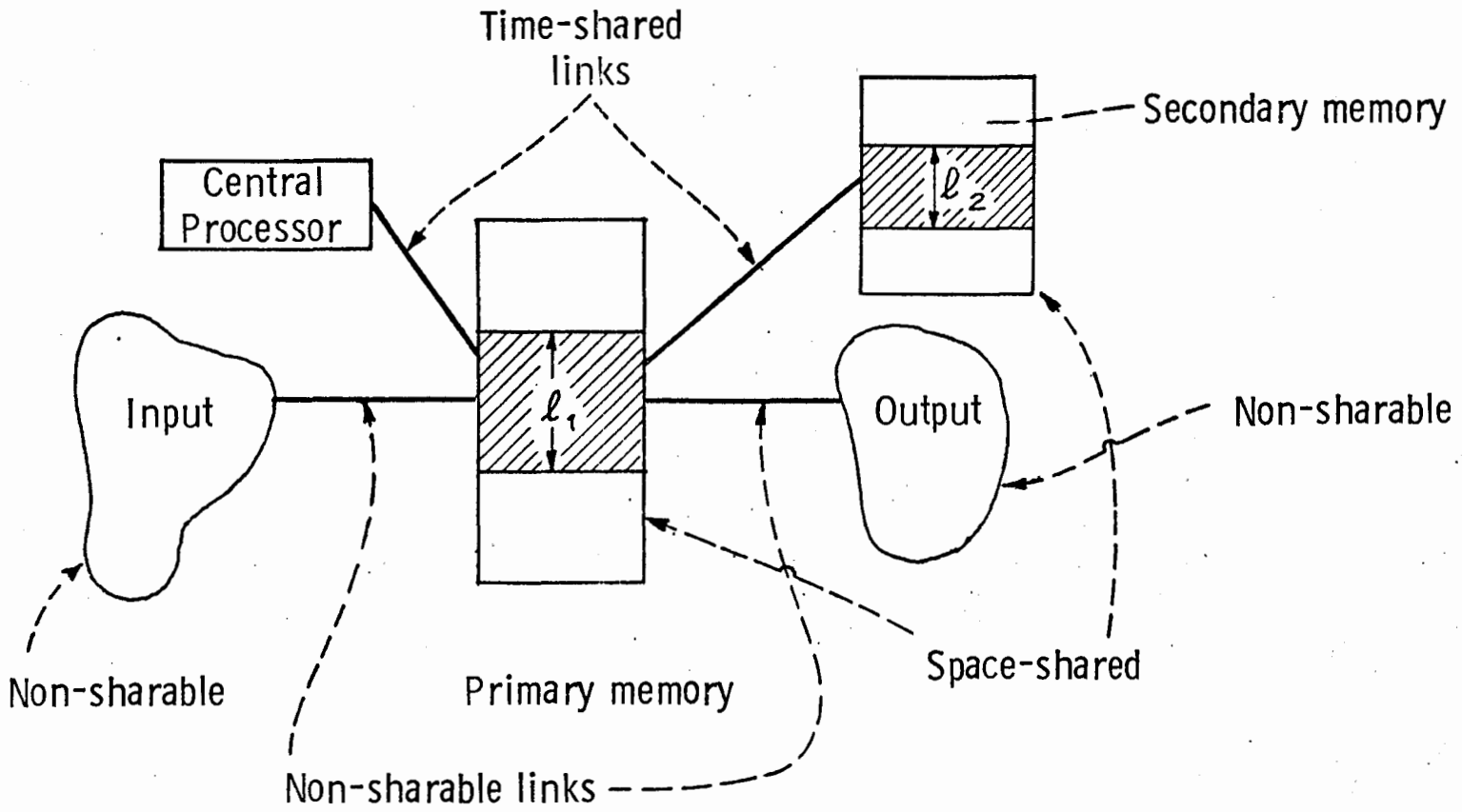
$$t(\text{cache}) = a + mR$$

$$\text{GAIN} = \frac{Ra}{a+mR} = \frac{R}{1+\frac{m}{a}R} = \frac{R}{1+\alpha R}$$

$$\frac{m}{a} = \alpha = \text{MISS RATIO}.$$

ASSUME $R = 10$





· Multiprogram Fortran Machine Structure

MEMORY SYSTEM CHARACTERISTICS

1. LOW ACCESS TIME (FAST)
2. LARGE CAPACITY
3. LOW COST

MEMORY HIERARCHIES

A MEMORY HIERARCHY IS A MEMORY SYSTEM WHICH IS BUILT OUT OF A NUMBER OF MEMORY TECHNOLOGIES WHICH ARE COORDINATED IN USE SO AS TO REALIZE A SET OF MEMORY SYSTEM CHARACTERISTICS AVAILABLE IN ANY SINGLE MEMORY TECHNOLOGY.

L O C A L I T Y

OVER REASONABLE TIME PERIODS A PROGRAM TENDS TO REFERENCE ONLY A SMALL SUBSET OF THE ADDRESS SPACE IT CAN POTENTIALLY ADDRESS.

MEMORY TECHNOLOGY EXAMPLES

1. GENERAL REGISTERS
2. CACHE
3. MAIN MEMORY
4. EXTENDED MAIN MEMORY
5. MAGNETIC DOMAIN/CCD SHIFT REGISTER
6. FIXED HEAD DISK
7. MOVING HEAD DISK
8. TAPE
9. ARCHIVAL MEMORY

FASTER ACCESS ↑

LOWER COST ↓

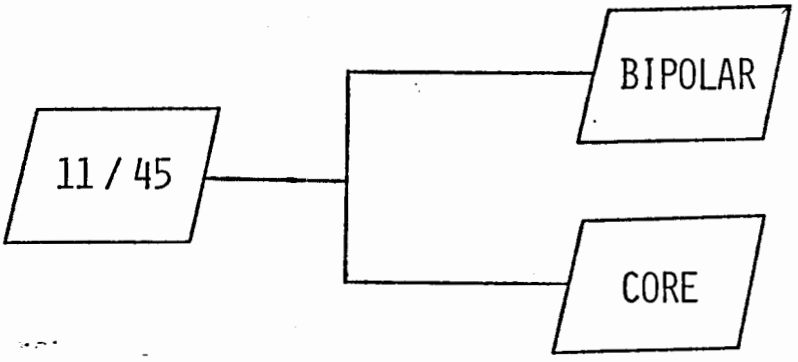
M E M O R Y H I E R A R C H Y

O P E R A T I O N

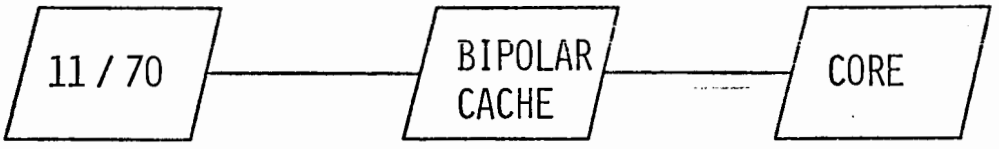
1. TRANSPARENT
    A. CACHE
    B. DEMAND PAGING TO USER

2. NON-TRANSPARENT
    A. OVERLAYING
    B. FILE SYSTEMS
    C. DEMAND PAGING TO SYSTEM

EXAMPLE



NON - TRANSPARENT



TRANSPARENT

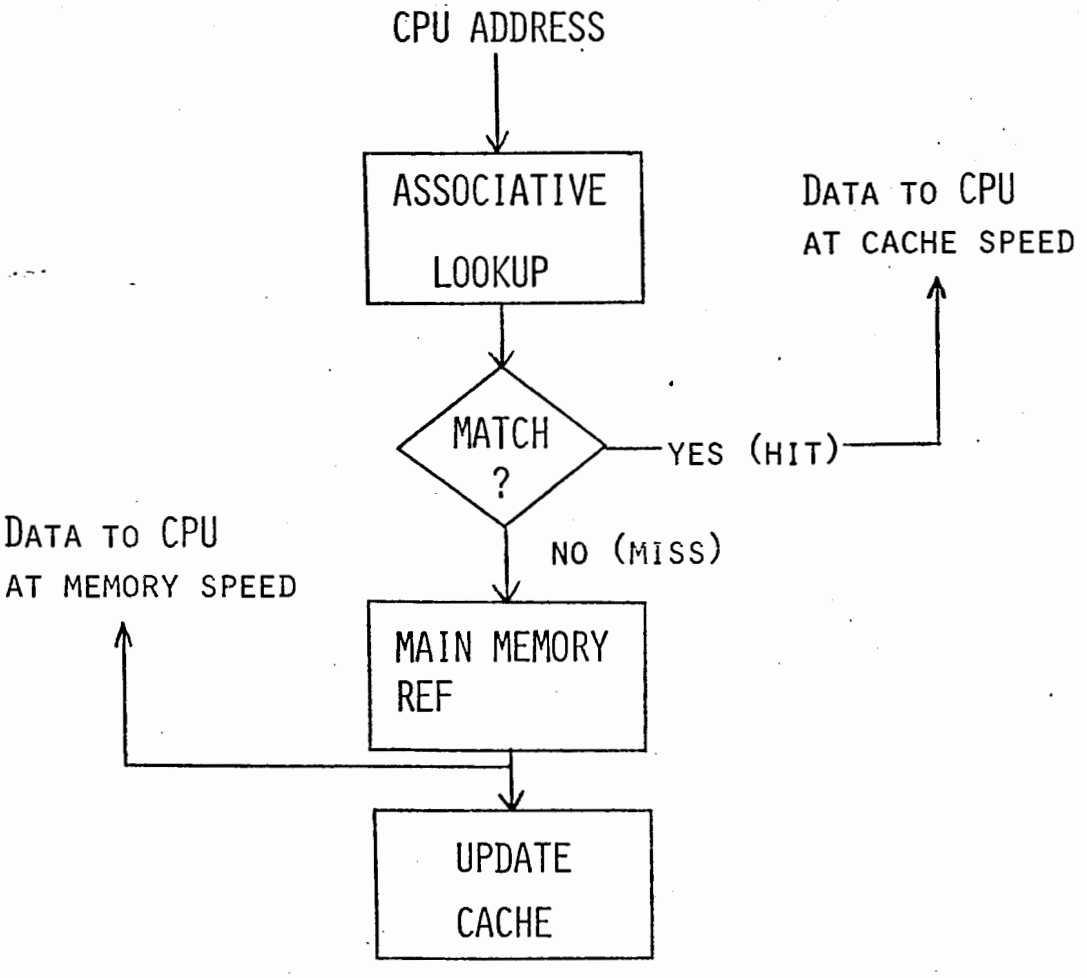
C A C H E

1. ASSOCIATIVE MEMORY WHICH STORES ADDRESS--
   DATA PAIRS

2. ASSOCIATION IS DONE ON ADDRESS

CACHE OPERATION

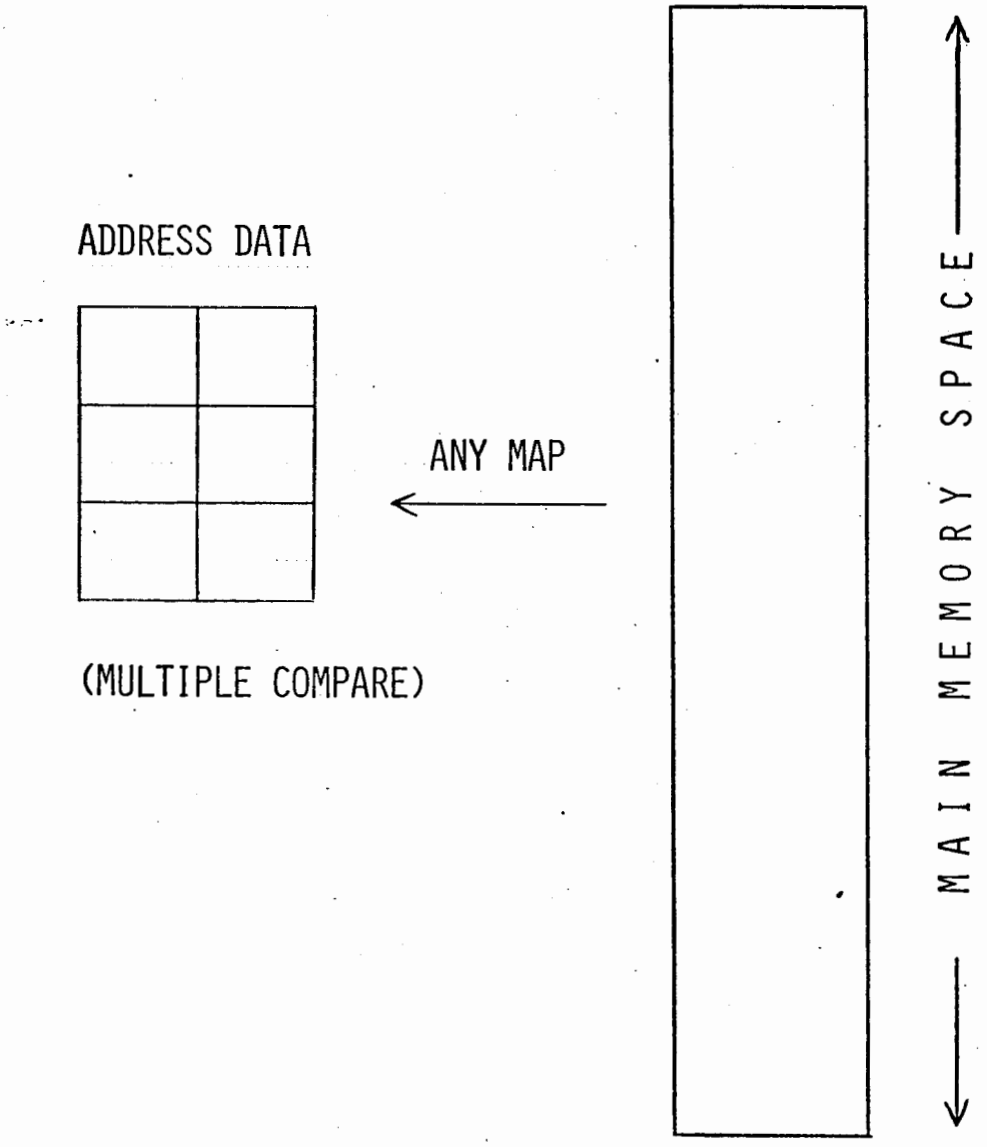
(CPU READ)



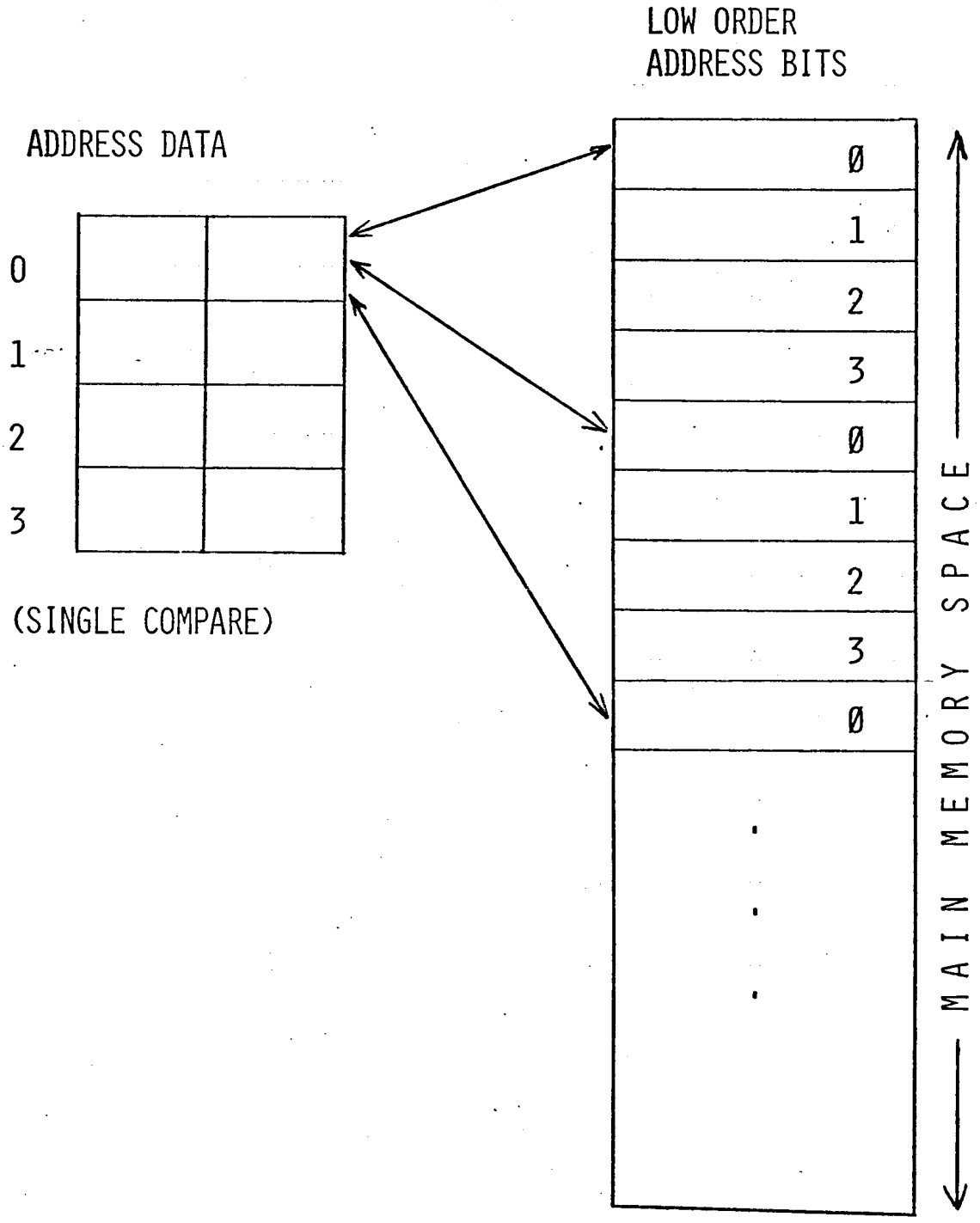
CACHE PARAMETERS

1. CACHE SIZE
2. ASSOCIATIVITY
3. BLOCK SIZE
4. REPLACEMENT ALGORITHM
5. WRITE ALGORITHM
6. ALLOCATION SIZE
7. ALLOCATION BY REFERENCE TYPE

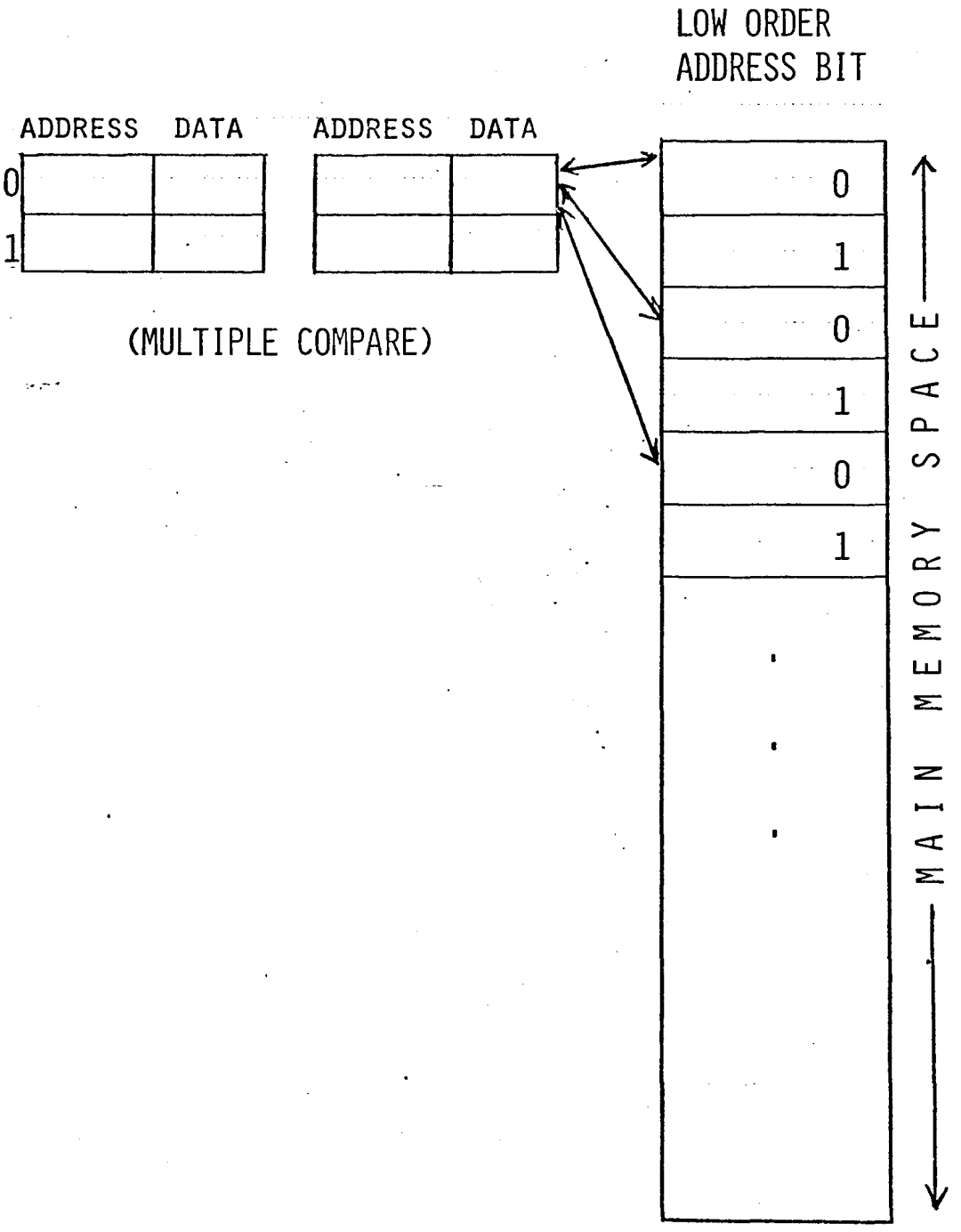
FULLY ASSOCIATIVE



DIRECT MAP


LOW ORDER
ADDRESS BITS
ADDRESS DATA
0
1
2
3
(SINGLE COMPARE)
Ø
1
2
3
Ø
1
2
3
Ø
MAIN MEMORY SPACE

SET ASSOCIATIVE



BLOCK SIZE

1. (USUALLY) UNIT OF DATA EXCHANGED BETWEEN MAIN MEMORY AND CACHE

2. (USUALLY) UNIT OF CACHE ALLOCATION

3. OFTEN LARGER THAN ONE WORD TO ACHIEVE INSTRUCTION AND DATA "PREFETCH"

REPLACEMENT ALGORITHM

(APPLICABLE ONLY TO SET AND FULLY ASSOCIATIVE)

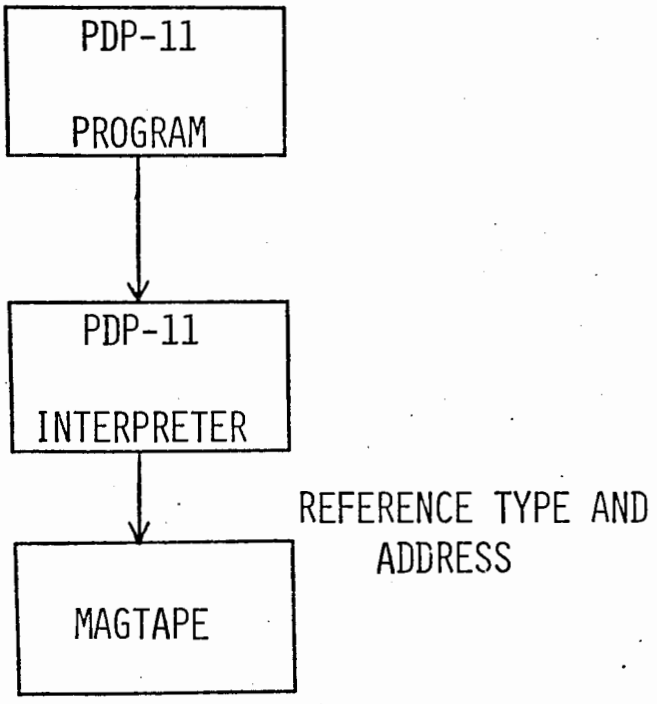
1. LRU
2. FIFO
3. RANDOM

W R I T E A L G O R I T H M

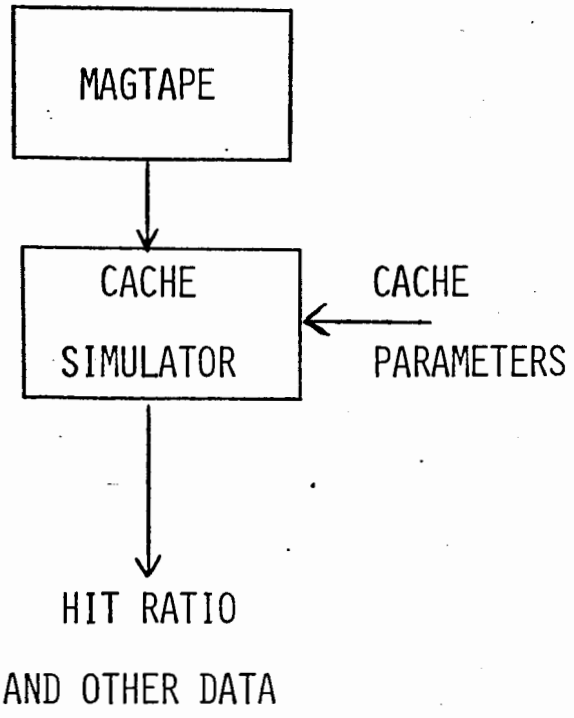
1. WRITEBACK -- CACHE ONLY IS UPDATED ON WRITE HITS. MAIN MEMORY UPDATED ONLY ON REPLACEMENT OF CACHE BLOCK WHICH HAS BEEN WRITTEN INTO.

2. WRITE THRU -- MAIN MEMORY UPDATED ON ALL WRITES.

S I M U L A T I O N -- I



S I M U L A T I O N -- II



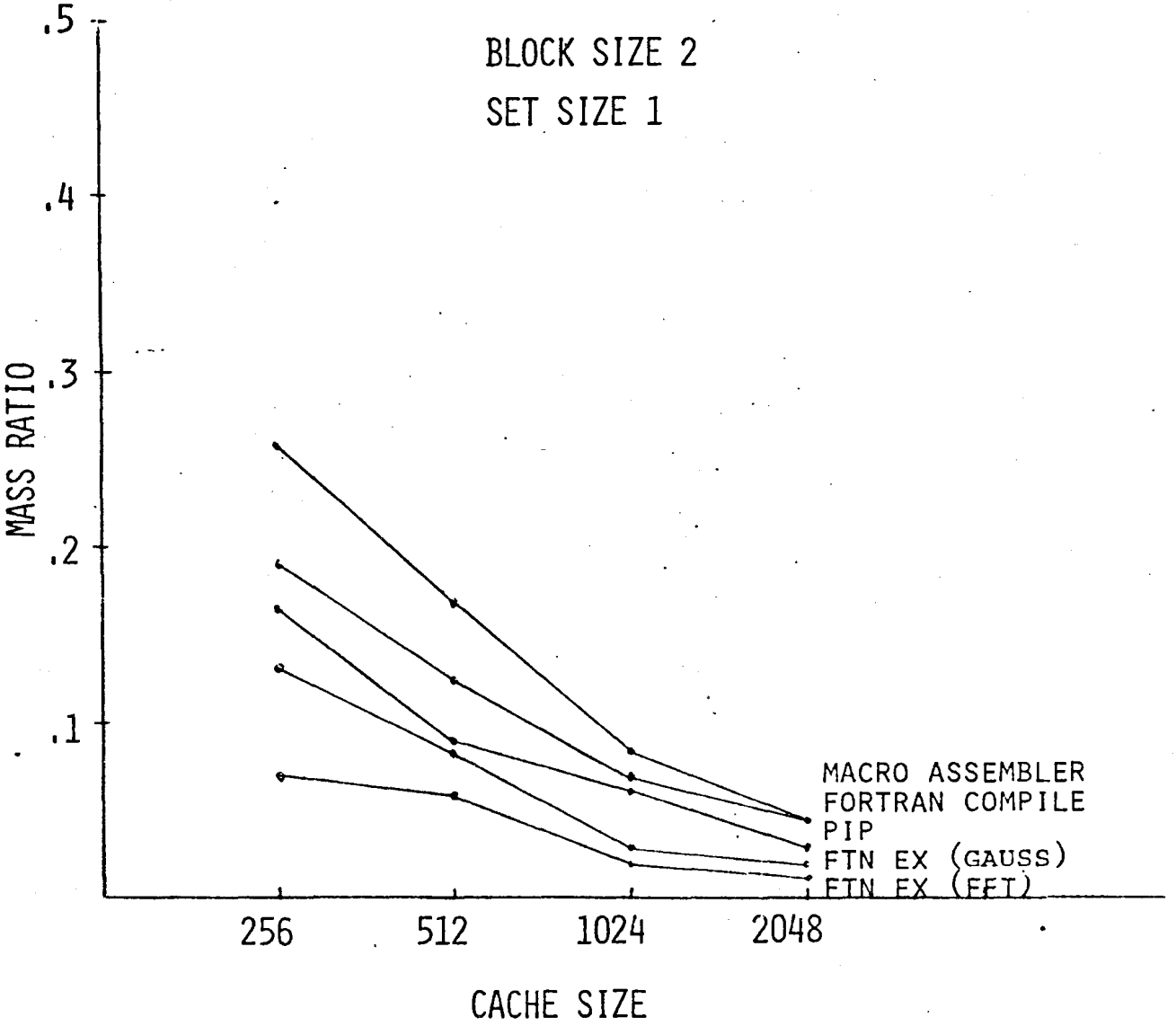


FIG. 2. EFFECT OF CACHE SIZE ON MISS RATIO

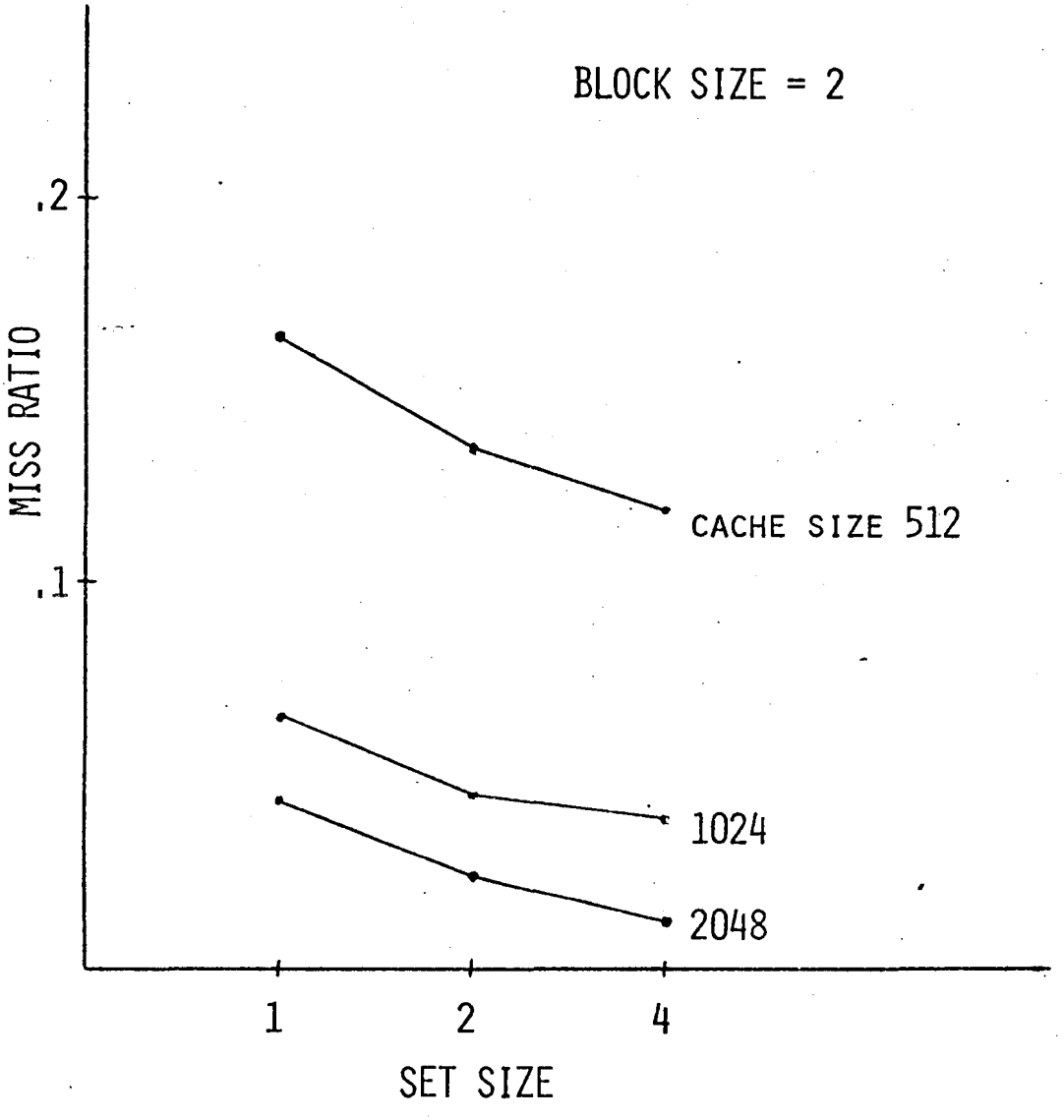


FIG. 3. EFFECT OF SET SIZE ON MISS RATIO

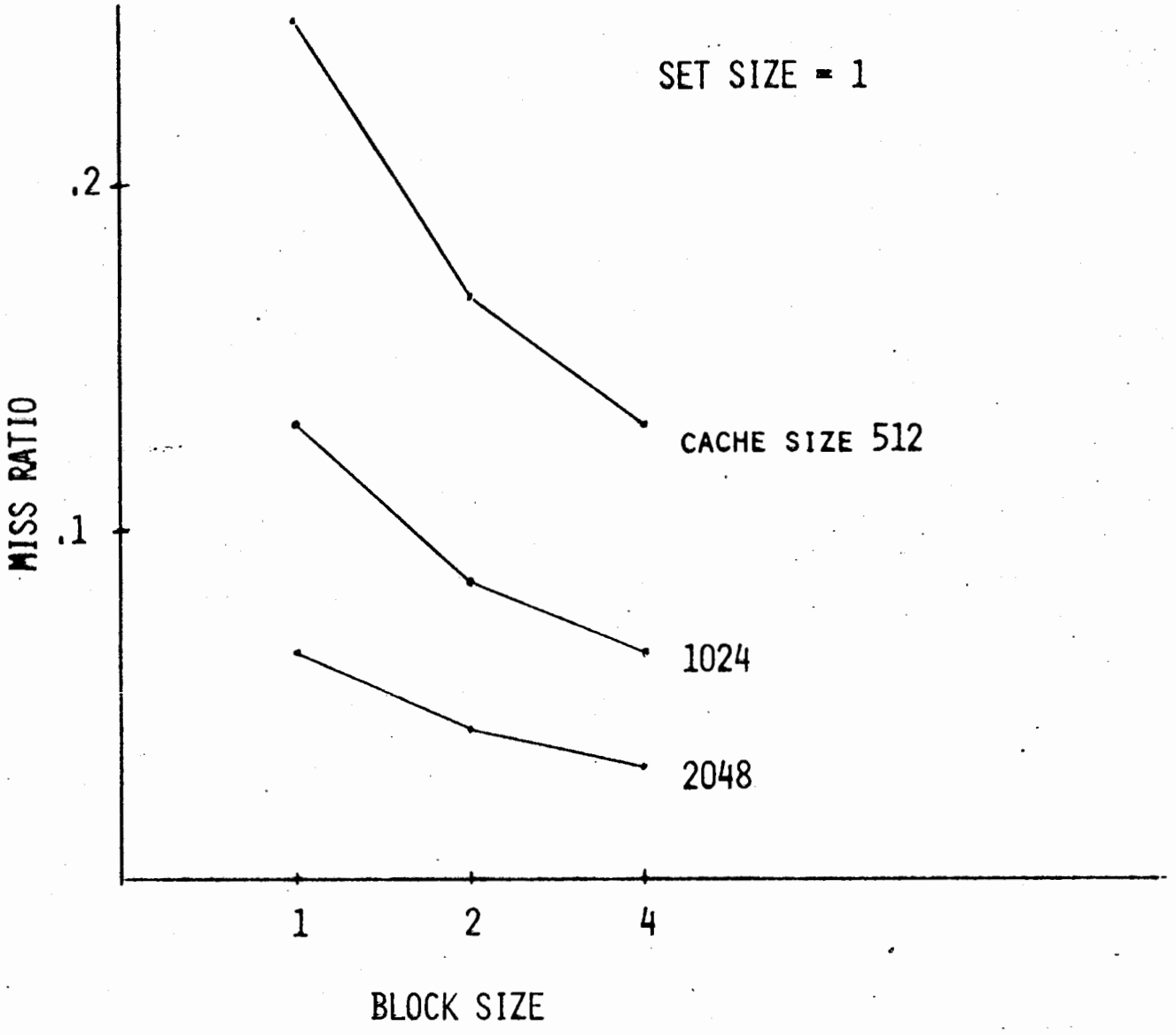


FIG. 4. EFFECT OF BLOCK SIZE ON MISS RATIO

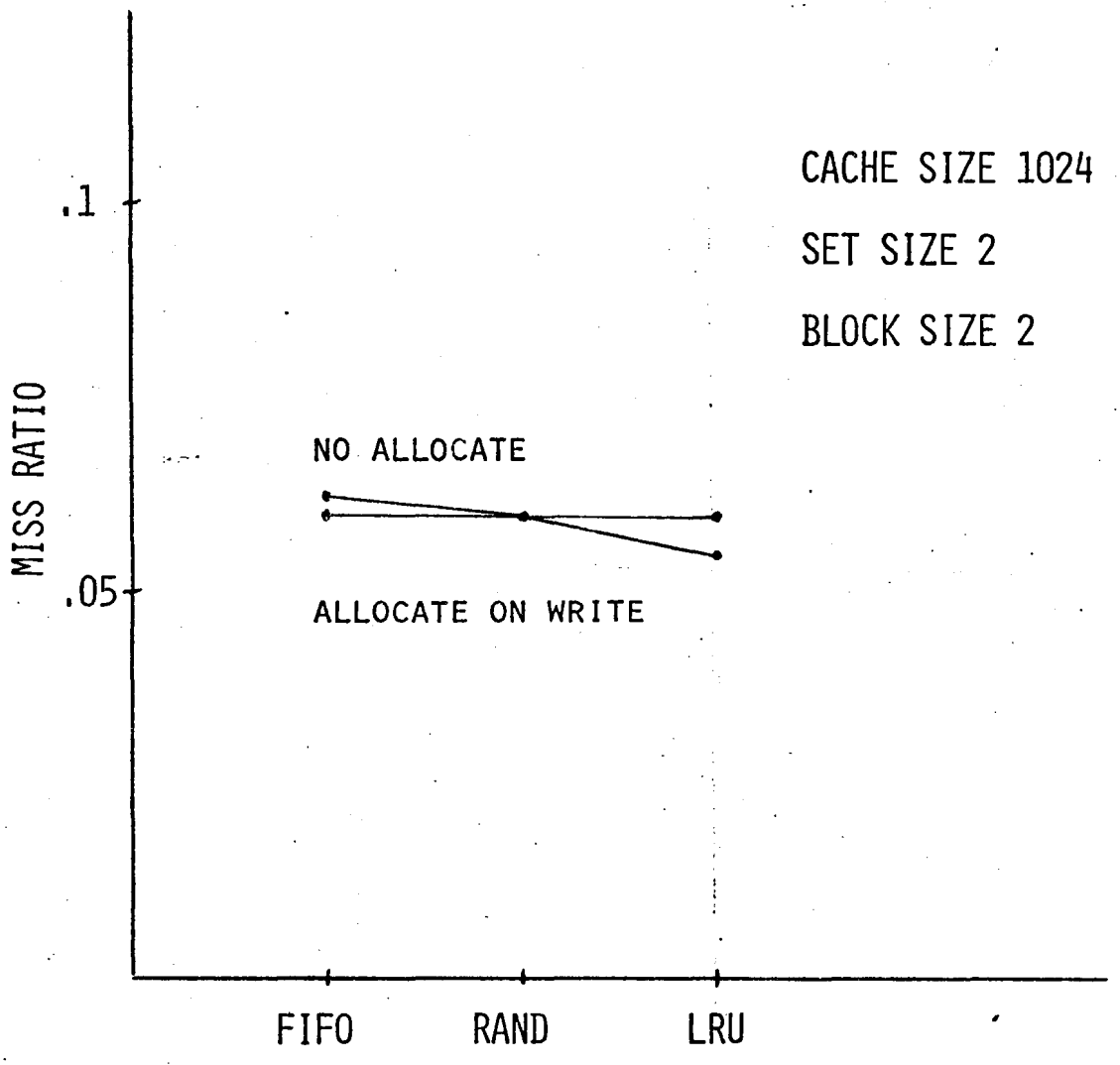


FIG. 5. EFFECT OF REPLACEMENT ALGORITHM AND WRITE ALLOCATION ON MISS RATIO

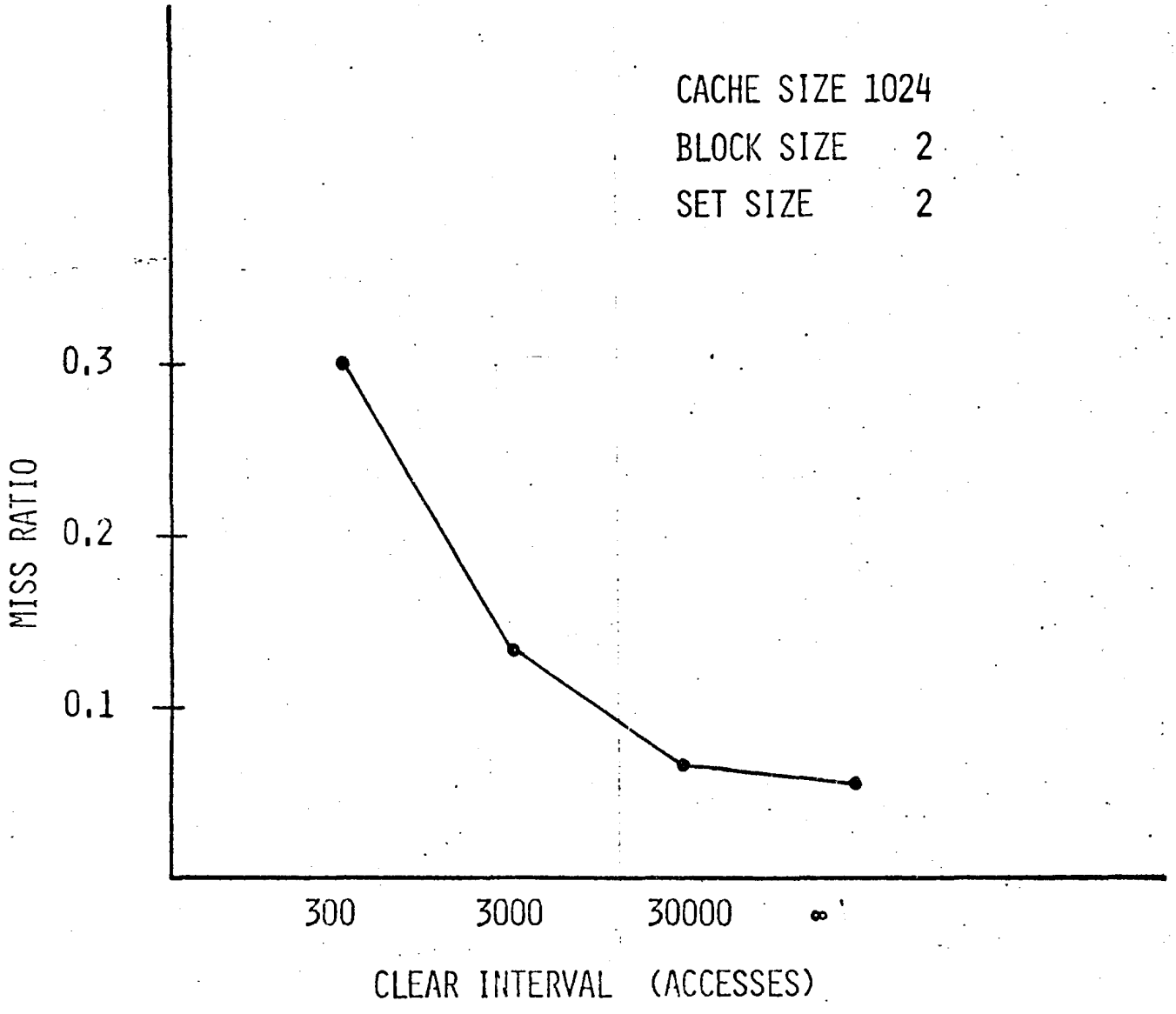


FIG. 6. EFFECT OF CLEAR INTERVAL ON MISS RATIO

RESULTS

1. ORDER OF IMPORTANCE

   A. CACHE SIZE

   B. BLOCK SIZE

   C. SET SIZE

2. REPLACEMENT ALGORITHM NOT IMPORTANT

3. WRITE ALGORITHM IMPORTANT--BUT SYSTEM LEVEL DECISION

11/70 C A C H E

1. 1024 WORDS

2. SET ASSOCIATIVE--SET SIZE TWO

3. BLOCK SIZE TWO

4. RANDOM REPLACEMENT ALGORITHM

5. WRITE-THRU

11/70 CACHE PERFORMANCE

TYPICAL HIT RATIO

(READS) 95%

TYPICAL WRITE RATIO

10%

$\Longrightarrow \sim$ 15% CPU REFERENCES RESULT IN MAIN MEMORY REFERENCES

Feustel 1973 - Tagged Arch.

Arith: Int, Real., Long Int., Long Real, Complex, long Compler, Mixed

Structure: Vector, Matrix, Matrix (Arith.) Sparse Vector.

Structures: Q, double/single linked List, Stack,

Process: Semaphore, Event, Message, Interrupt-of., I-d.

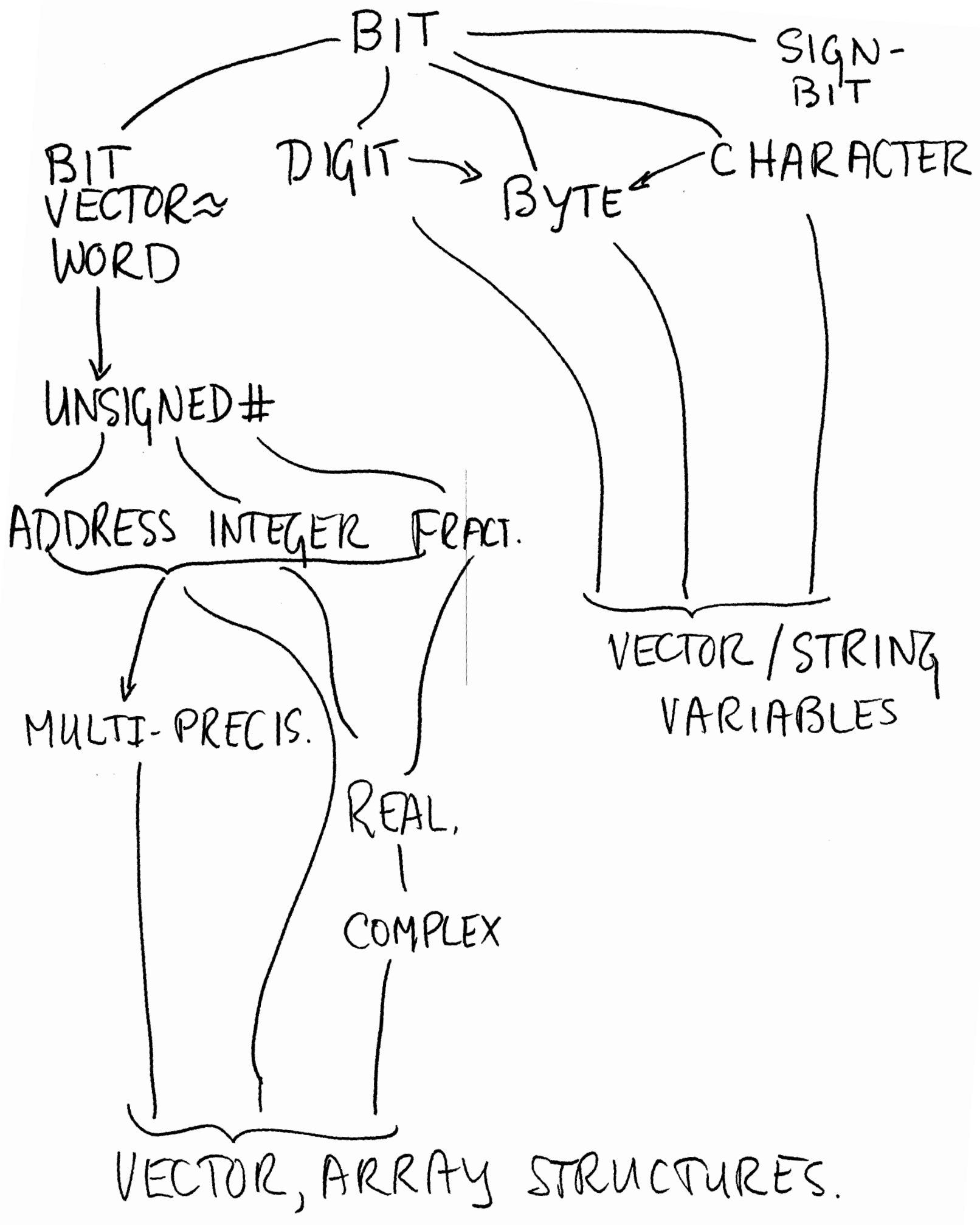
Procedures: Proc, Name of Var, formal, Label, Reference to, Paramete-Set

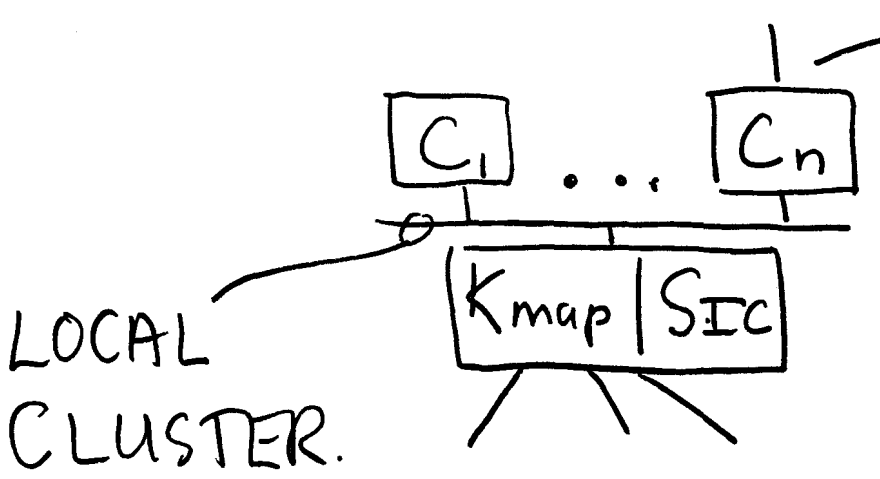
Undefined, Garbage

Machine State and Instructions

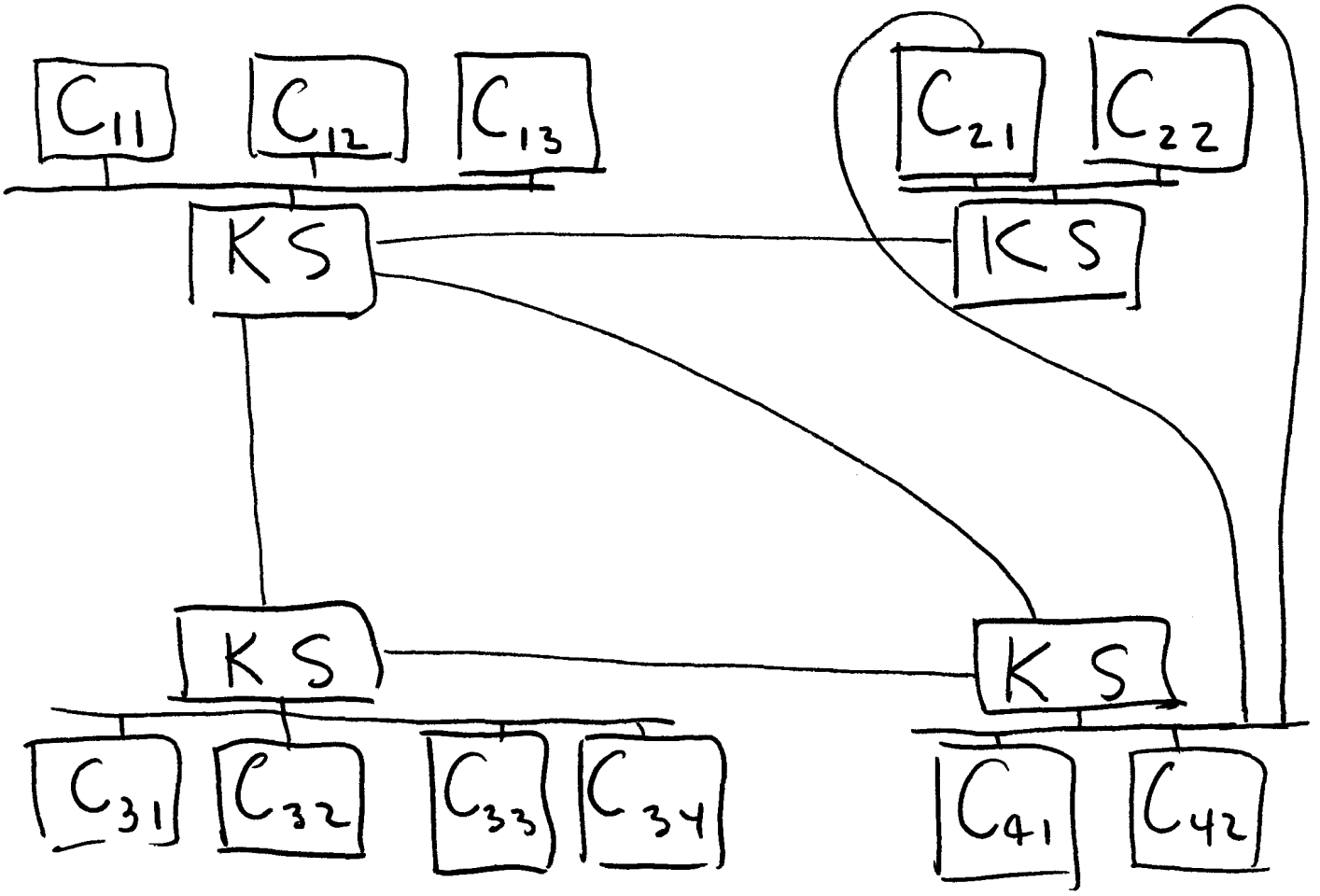
File

CHAR, BOOLEAN


BIT
SIGN-
BIT
BIT
VECTOR≈
WORD
DIGIT
BYTE
CHARACTER
UNSIGNED#
ADDRESS
INTEGER
FRACT.
VECTOR / STRING
VARIABLES
MULTI-PRECIS.
REAL,
COMPLEX
VECTOR, ARRAY STRUCTURES.



mC CLUSTER STRUCTURE
(Computer Module).



mC Problem Structure

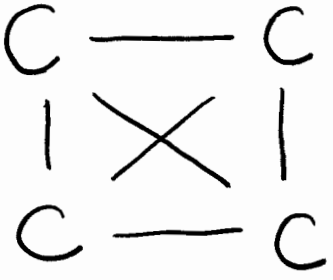
DEFINITIONS

N-Computer Networks - Computers loosely coupled via Comm. L's.

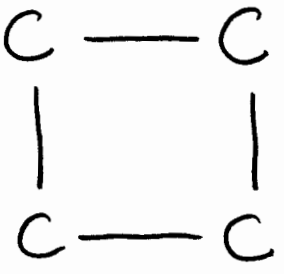
nCm Computer Modules - Tightly coupled C's... possibly sharing Mp.

mP- Multi-procesor Computer- A number of processors sharing a common, Mp.

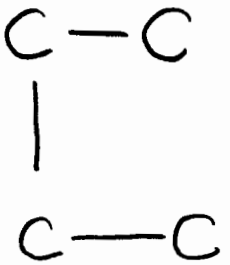
DIRECT INTERCONNECT



EXHAUSTIVE



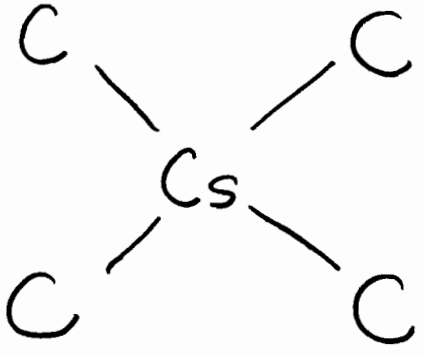
RING

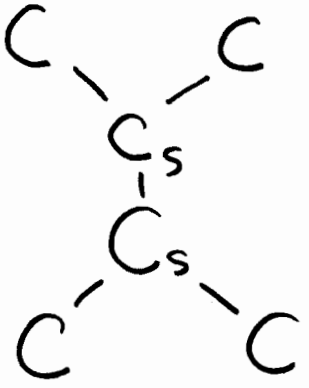


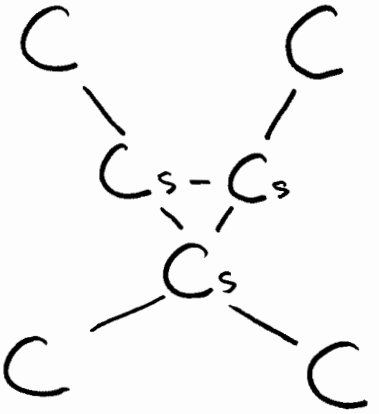
CHAIN

STAR

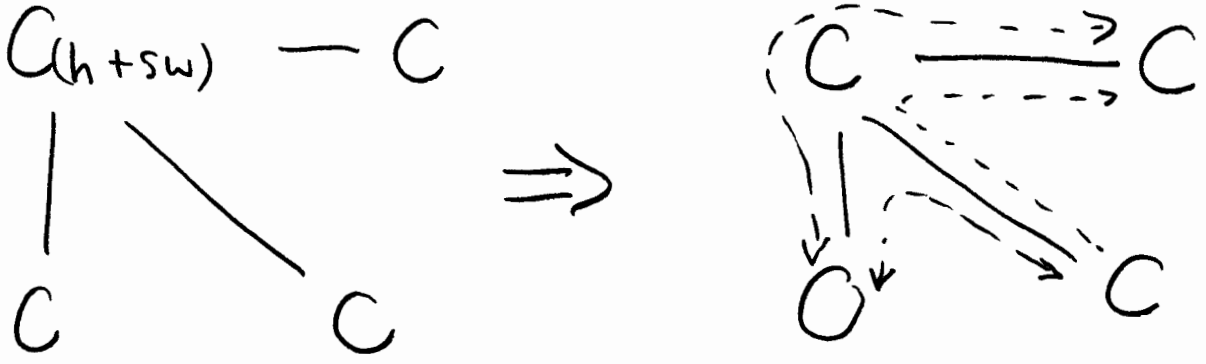
S/F NETS W/ $C_{sw's}$.







Hybrid.



YEARLY IMPROVEMENTS IN TECHNOLOGY (1975)

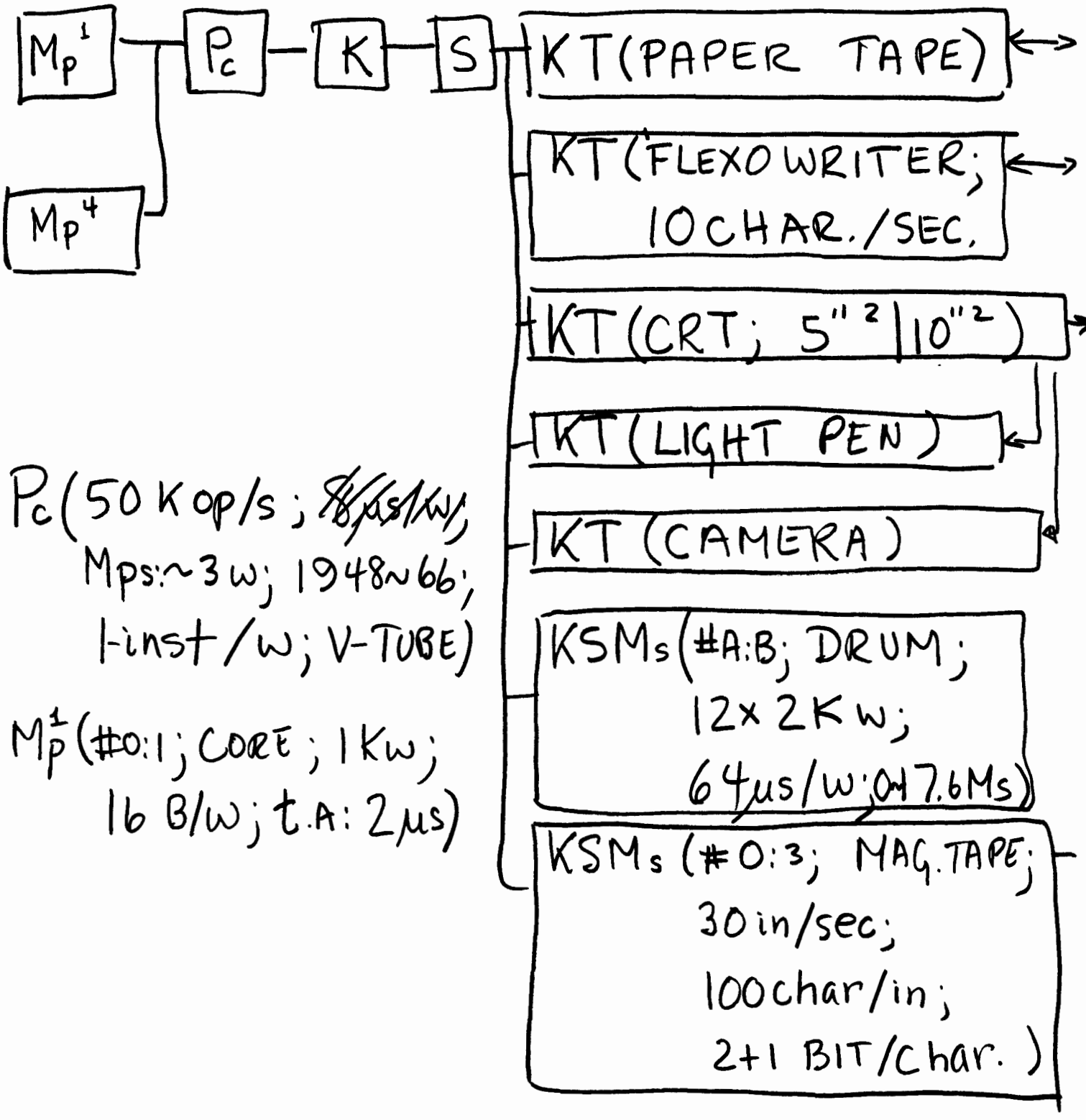
- SEMICONDUCTORS
  - DENSITY 2^{t-1962}
    = 60 ~ 80 %/yr (CONSERVATIVE)

- DISKS (62-74) - DENSITY = 41%/yr.
- CORE PRICE IMPROVE 30%/yr.
- TAPE (52-73) - 23%/yr DENSITY
  29%/yr. DATA-RT
- POWER, PACKAGING ~ 0
- MINIS - 31% IMPROVE IN PRICE (SINCE '60)
- TERMINALS - YES.

DISK TECHNOLOGY 1975

	PRICE (K$)	SIZE (MB)	C/B (¢/B)	ACCESS T.
FLEX.	3	2.5	.12	1 SEC
1 PLAT.	6	30	.02	50 Ms.
3-5 "	12	160	.0075	↓
10 "	25	800	.003	20 Ms.

	MB/PLATTEER	YRS (AT 41% YR)
1	30	~~4~~3
3	53	1+
5	80	0



MIT WHIRL WIND I BLOCK (PMS) DIAGRAM.

STRUCTURES

1. MULTI-PROCESSOR - mP
2. COMPUTER MODULES - Cm
3. NETWORKS.

PROBLEM / OBJECTIVE FCN

1. LOCATION OF "WORK"; PEOPLE
2. REQ. FOR P_c, M_p, M_s, AVAILABILITY.

TRADEOFFS

	+	- (and COST)
mP	LESS M_p, L, MORE P_c AVAIL; CONFG. TO MAINTAIN	SMp; INTEGRAL SYSTEM.
Cm	FUNCTIONAL ISOLATION	M_p, LINKS, P_c (ABILITY TO MATCH/MOVE WORK)
N	LESS FCN. ISOLATE. COMM. LINKS.	SAME AS Cm ~~(LINKS MORE)~~

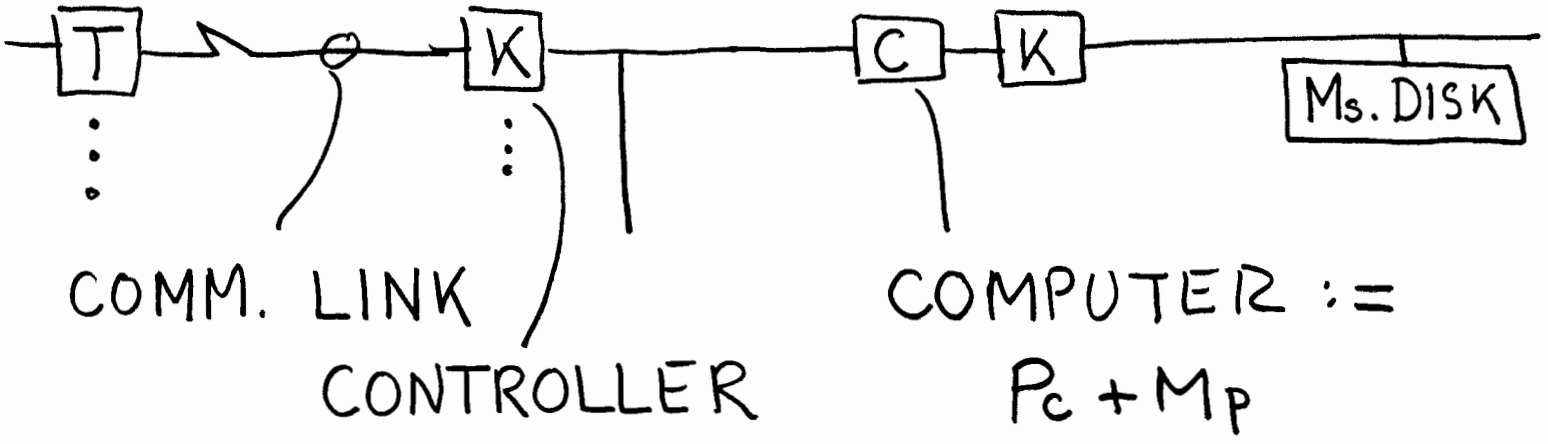


FIG1. BASIC COMPUTER, 1 SITE (MULTIPLE TERMINALS) - ACCESS TO DATA BASE

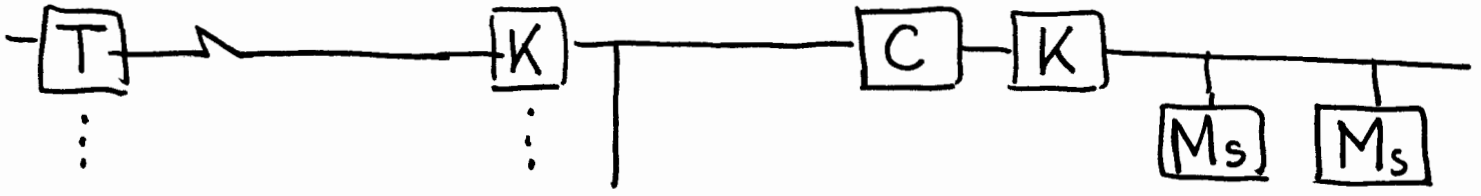
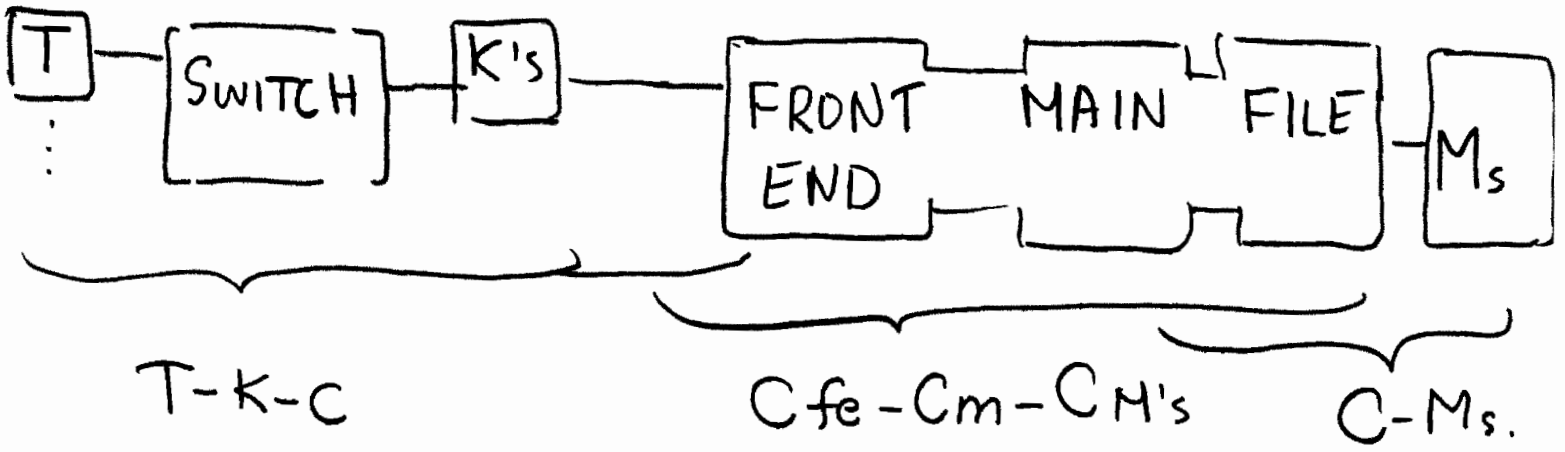


FIG2. BASIC C, 1 SITE, REDUNDANT DISK.



PROBLEM INTERCONNECTION

STRUCTURE

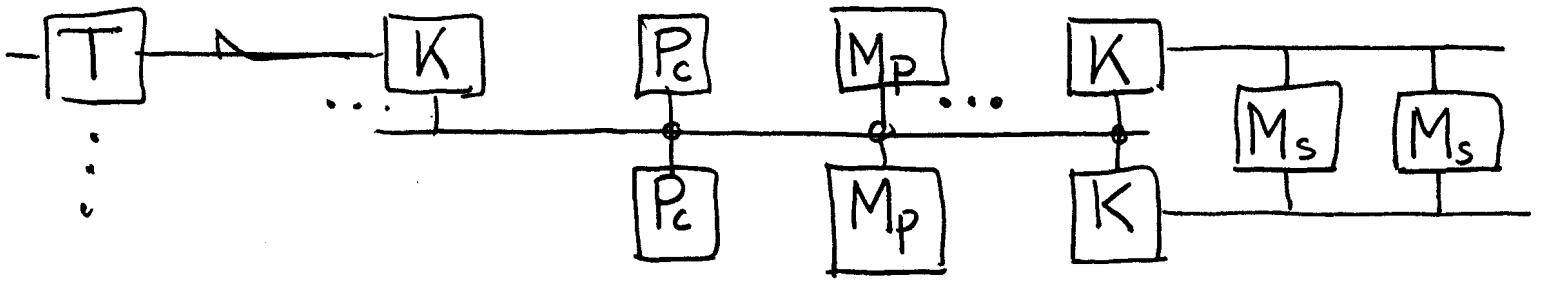


FIG 3. 1 C, 1 SITE WITH N+1 (REDUNDANT) RUNNING COMPONENT

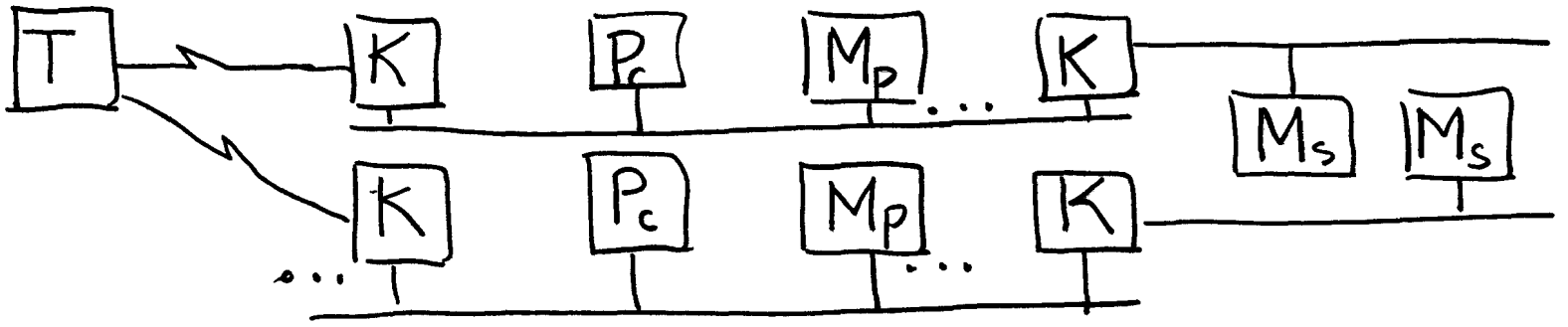


FIG 3A. 2C, 1 SITE WITH COMPLETE REDUNDANCY.

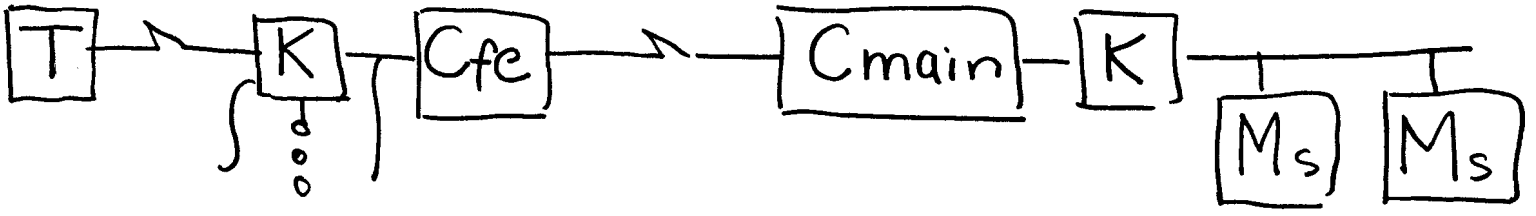


FIG4. N := Cfe + Cmain;
1 OR 2 SITES.

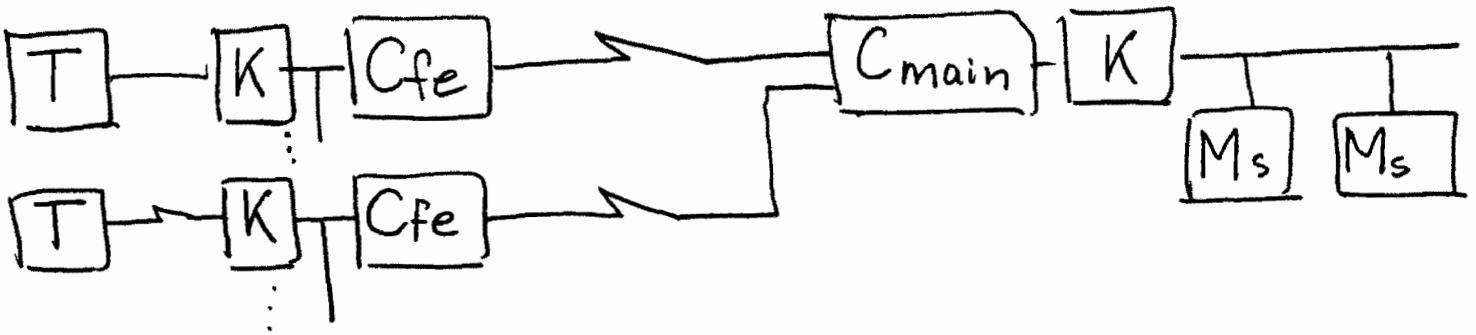


FIG 5. N := 2Cfe + Cmain ; 1, 2 or 3 SITES

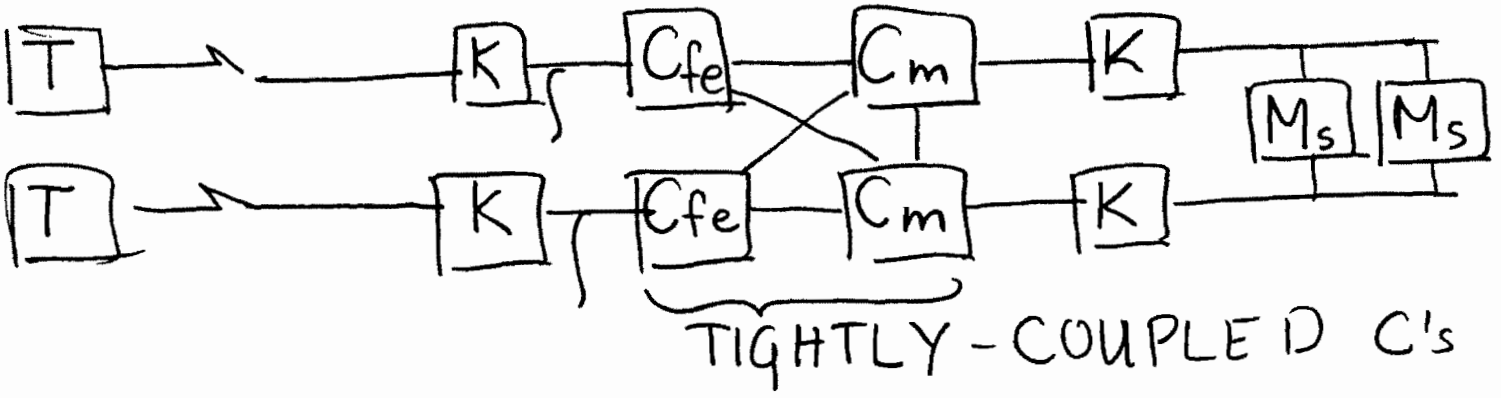


FIG. 13 Cm Structure, 1 SITE

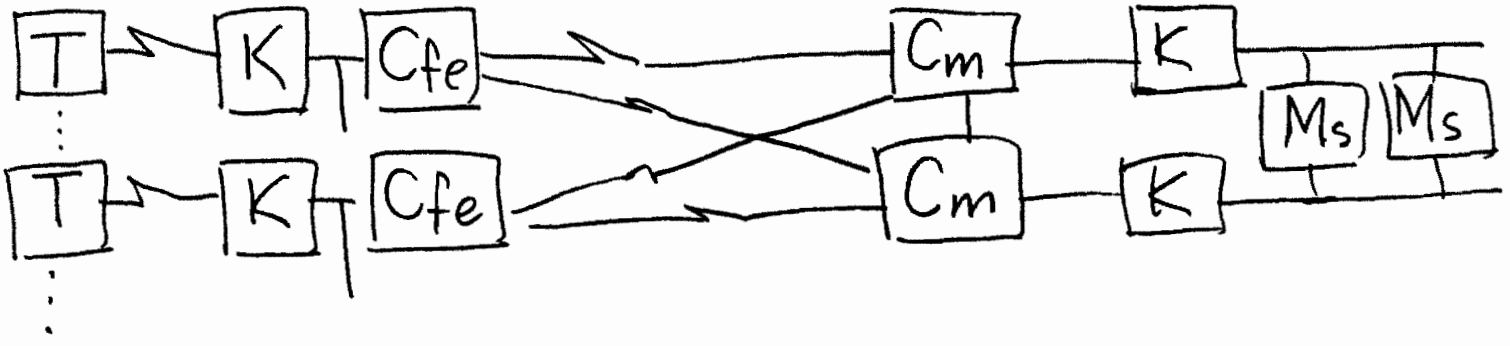


FIG. 12. N-Cm Structure ; 1~3 SITES

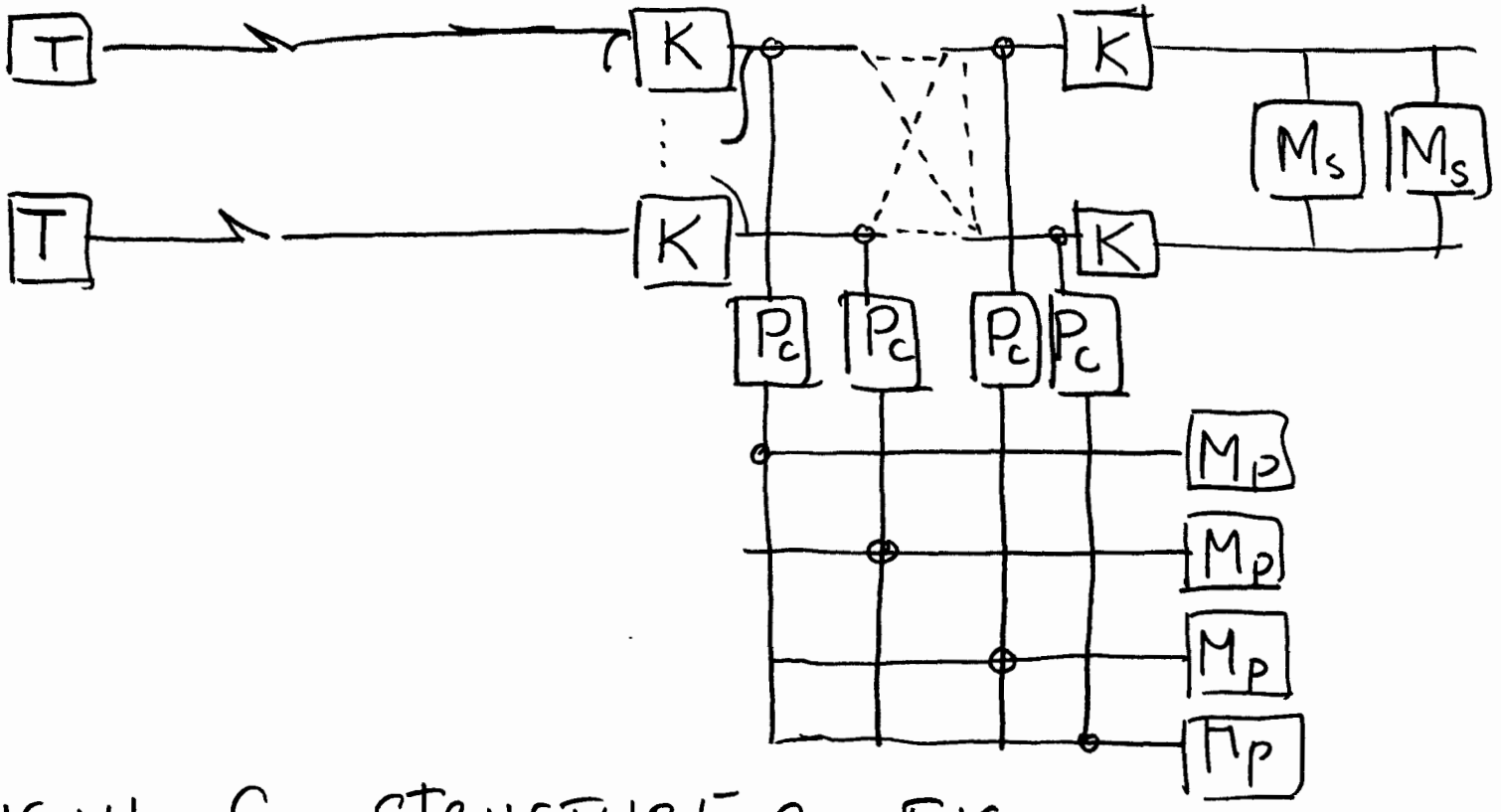


FIG 14. Cm STRUCTURE ≈ FIG 13.

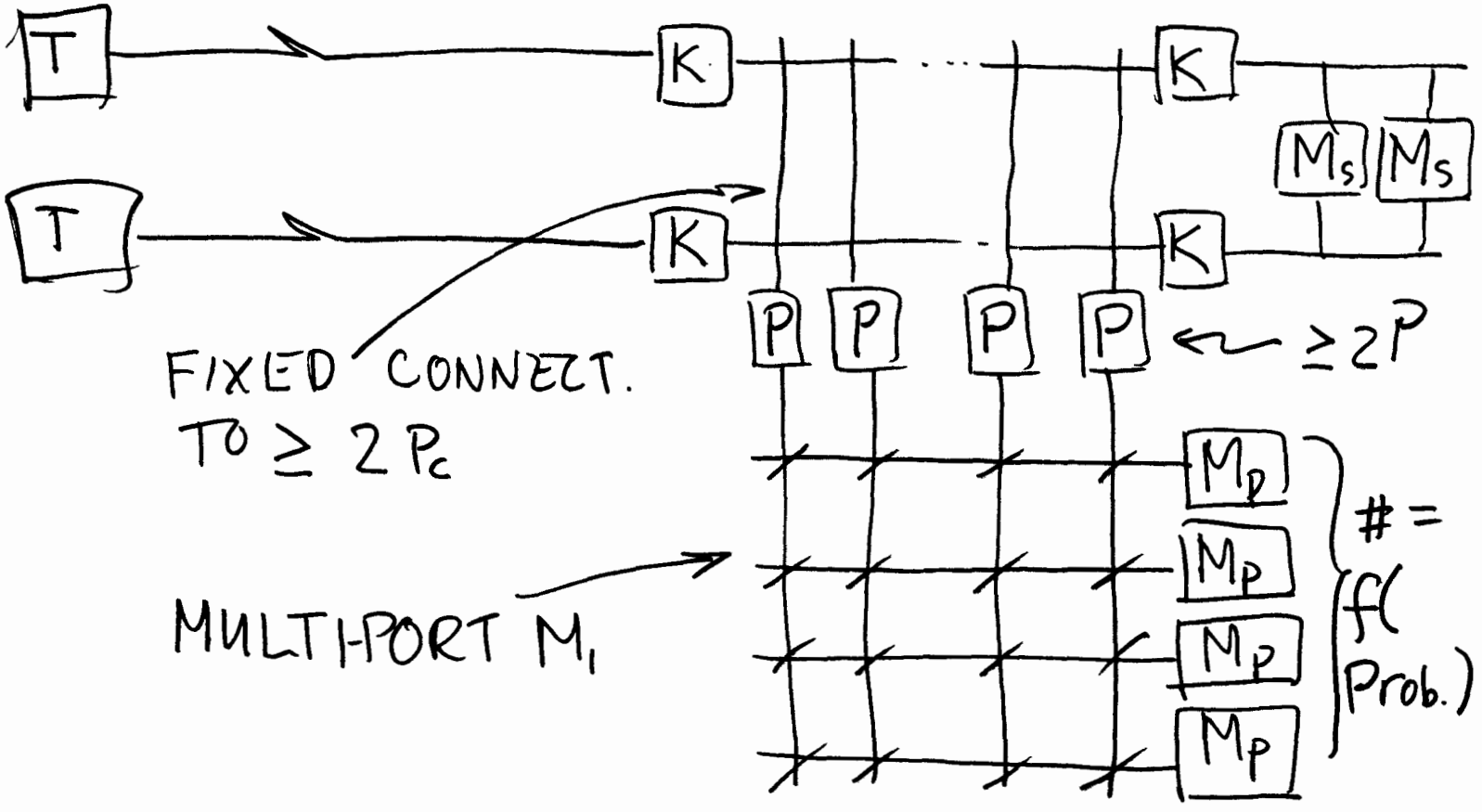


FIG 15 4 Pc (MULTIPROCESSOR)

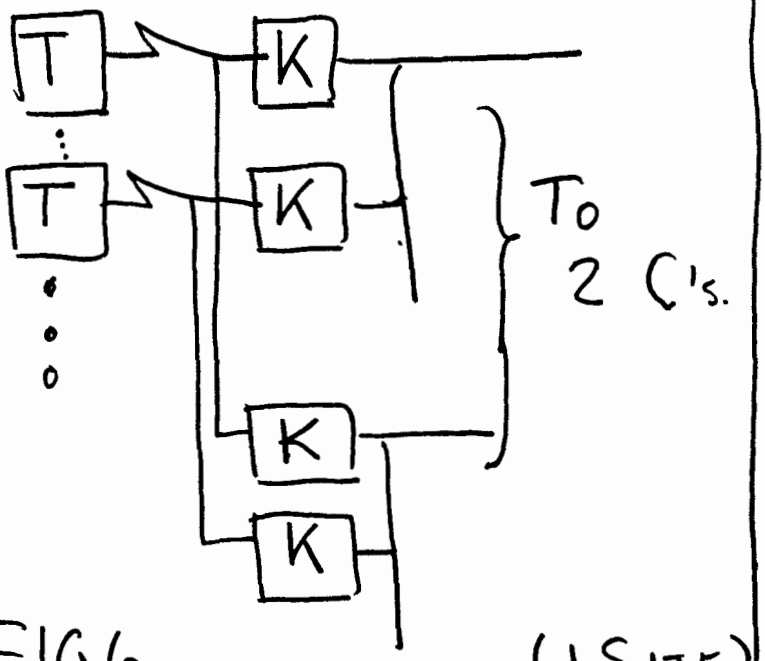


FIG 6. (1 SITE)

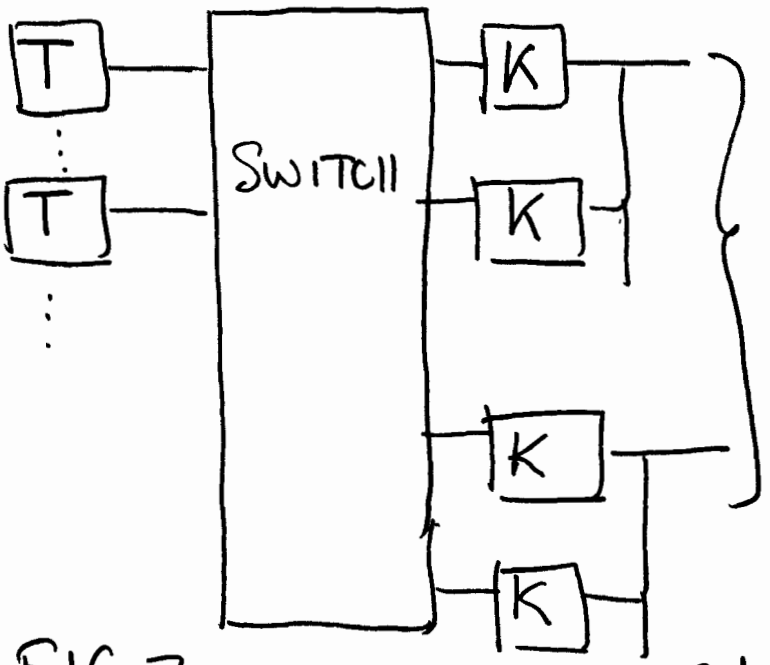


FIG 7.

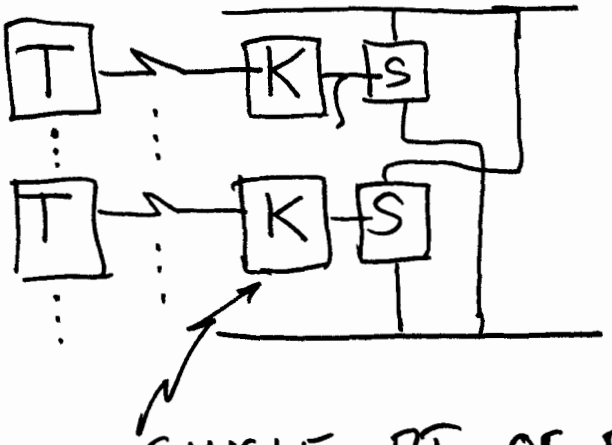


FIG 9. S. DUPLEX. 1 SITE

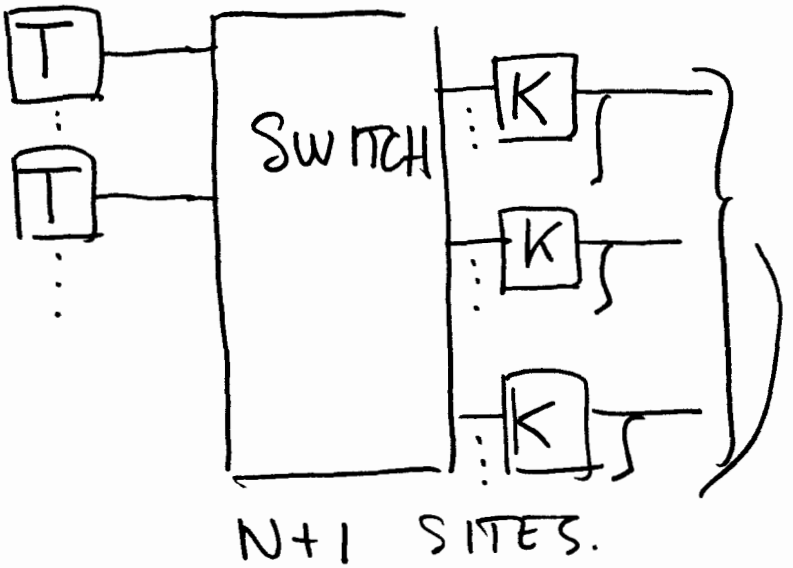


FIG 8.

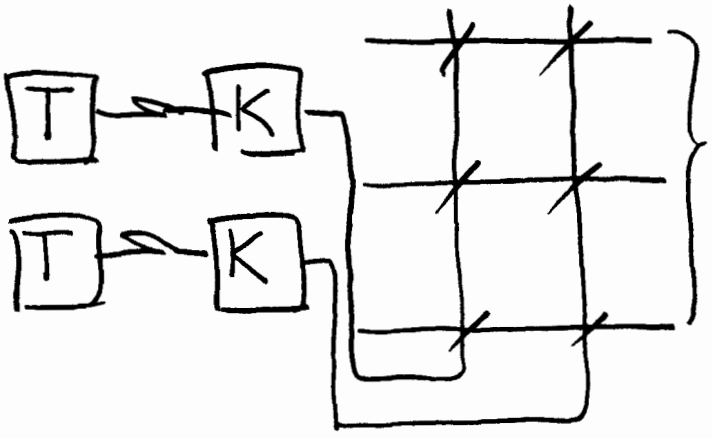


Fig. 10.
S. TRIPLEX S. 1 SITE

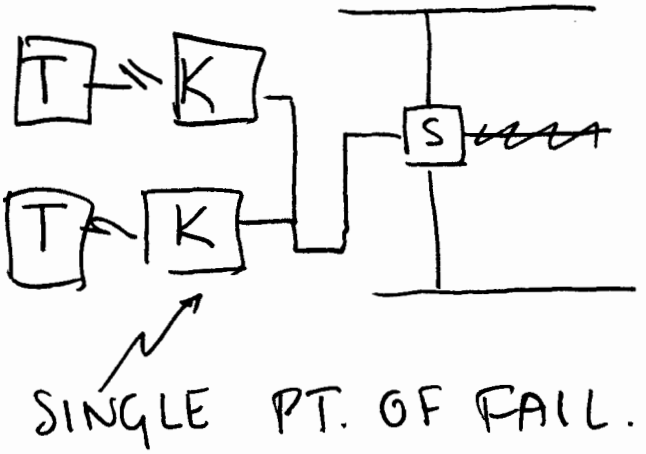
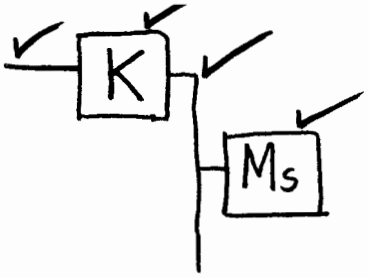
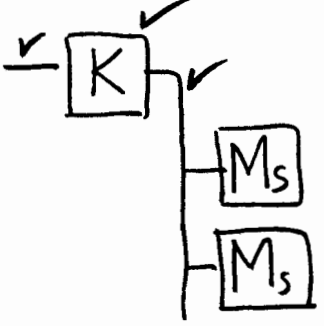


FIG 11.

1 SITE



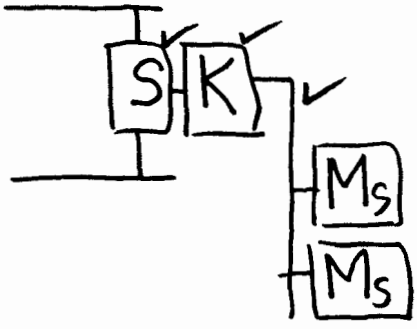
BASIC NEED



+ BACKUP DISK.

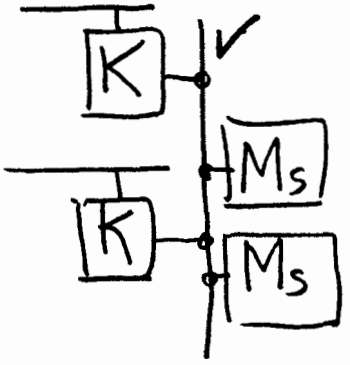
↙ PT. OF FAILURE

1C STRUCTURES



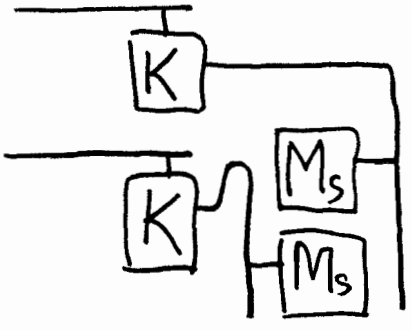
+ BACKUP C

2C (I.E. BACKUP)

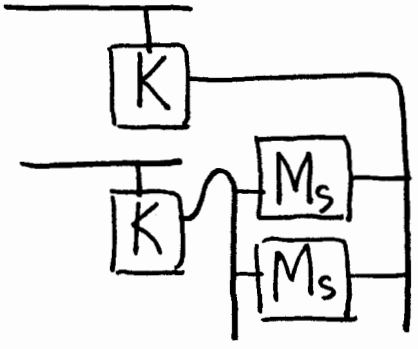


+ BACKUP K.

(NO OFFLINE REPAIR)



(FAILURE OF IC - DISABLES PATH TO 1 DISK)



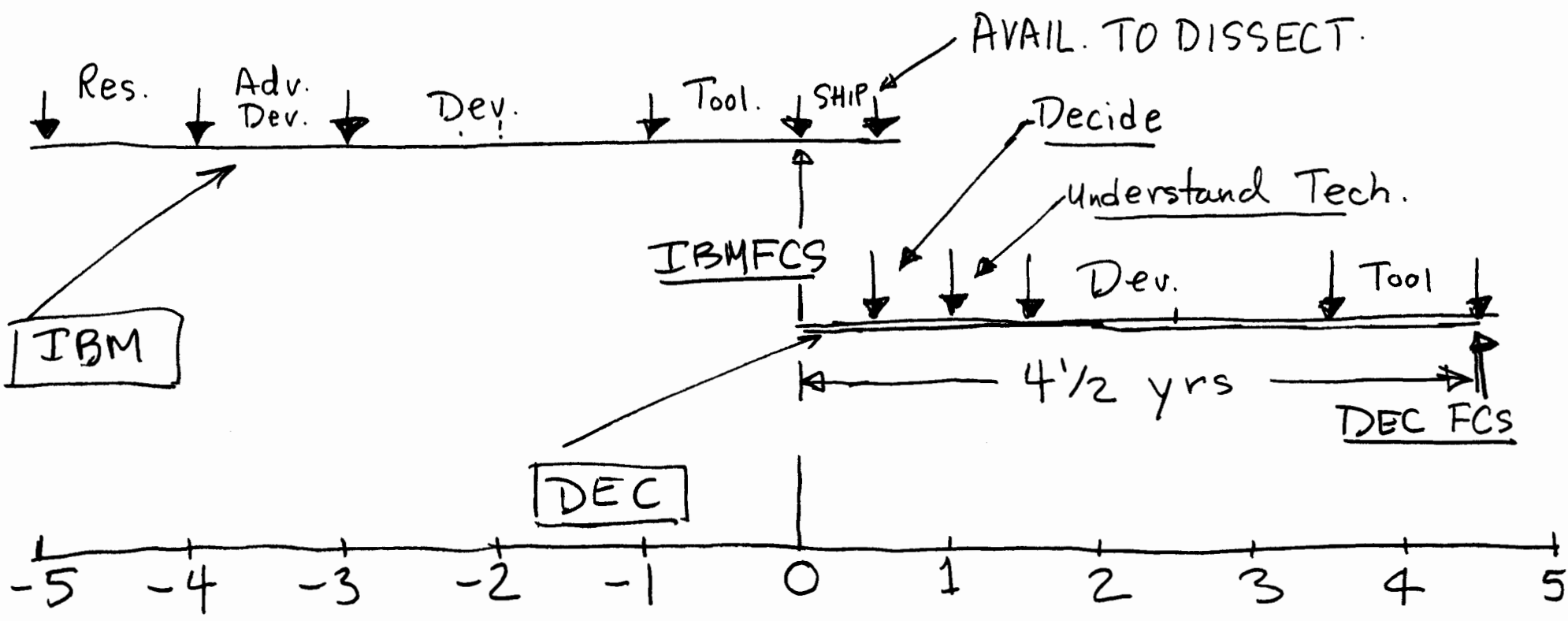
+ 2 PORT Ms. - WITH OFFLINE REPAIR

2C - NO SINGLE PT. OF FAILURE

How {Can / Are} We {Going To} Decrease Technology (IBM) Lead?

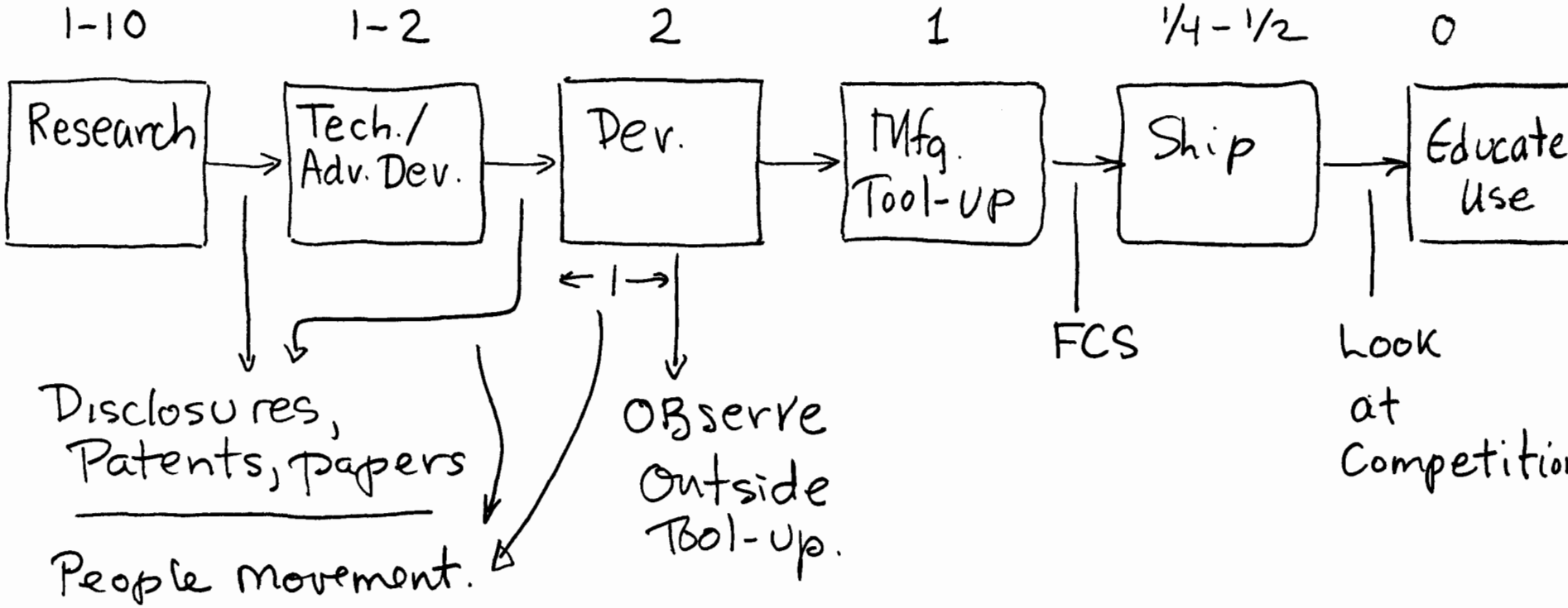
- Novel Organization of Electronics/ Systems
- Copy. Hard. We're away. Both Limited By Nat. Laws.
- Reduce Delay times — Hard Due to Segmented Co.
- Buyout People (only fast way) — Endup tracking. Problems
- Buyout Products.
- Faster Decisions
- Hire Adv. Dev. People — NOT Dev. People.

GB
2/1/76



TIMES FOR IBM / DEC DISKS.

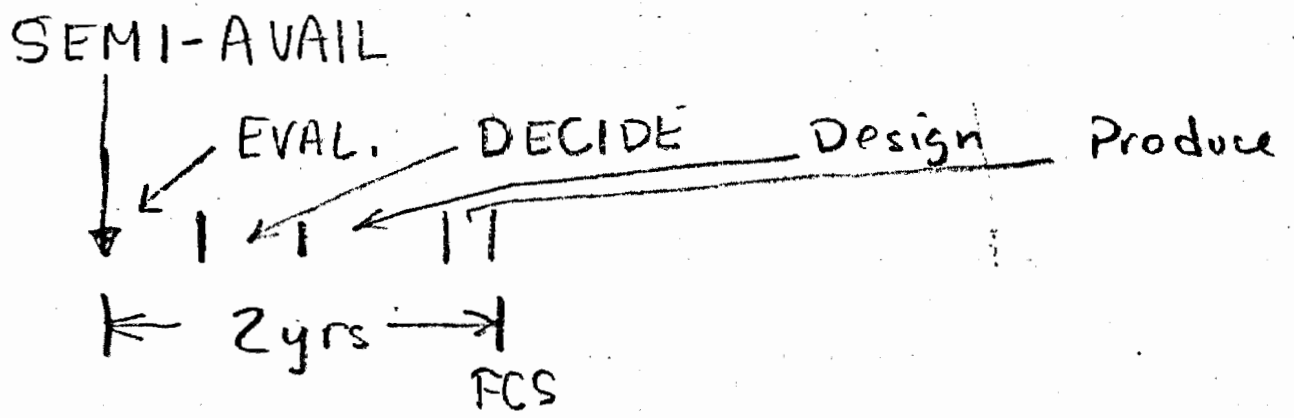
GB
2/1/76.

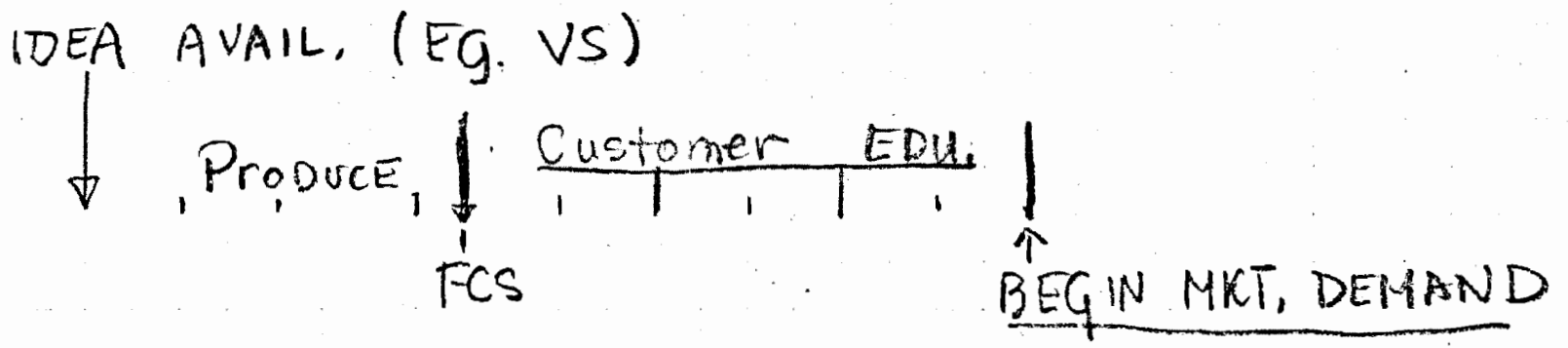


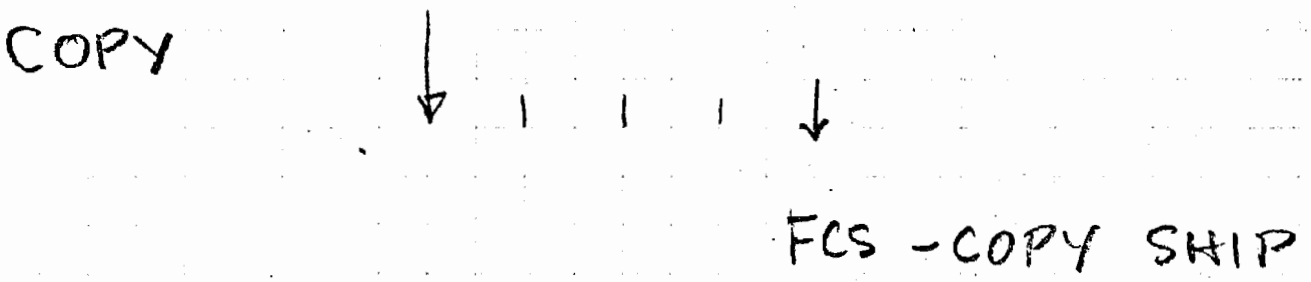
DISK R+D PROCESS.

(IBM).

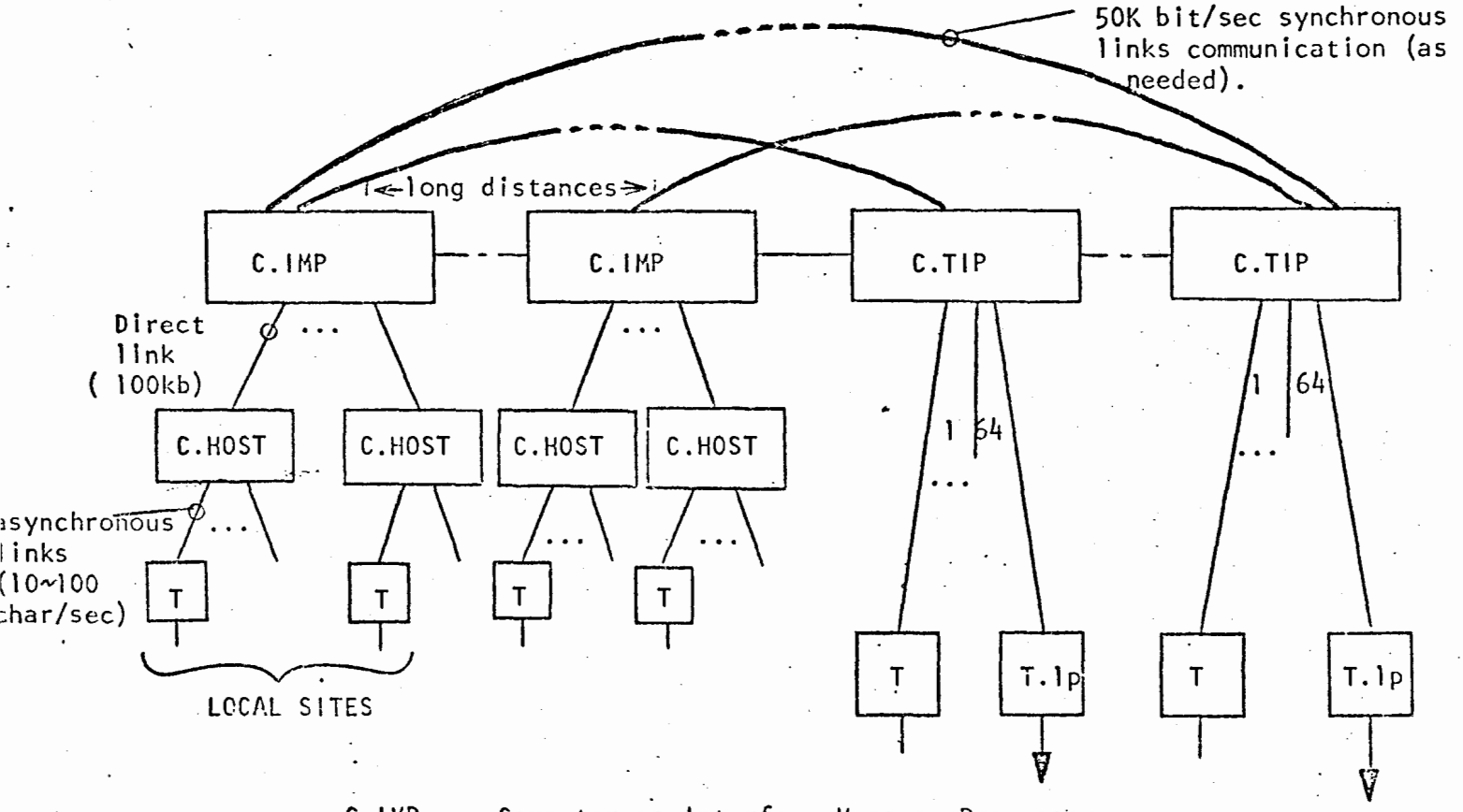
GB
2/1/76


SEMI-AVAIL
EVAL.
DECIDE
Design
Produce
2yrs
FCS


IDEA AVAIL. (EG. VS)
PRODUCE,
Customer EDU.
FCS
BEGIN MKT. DEMAND

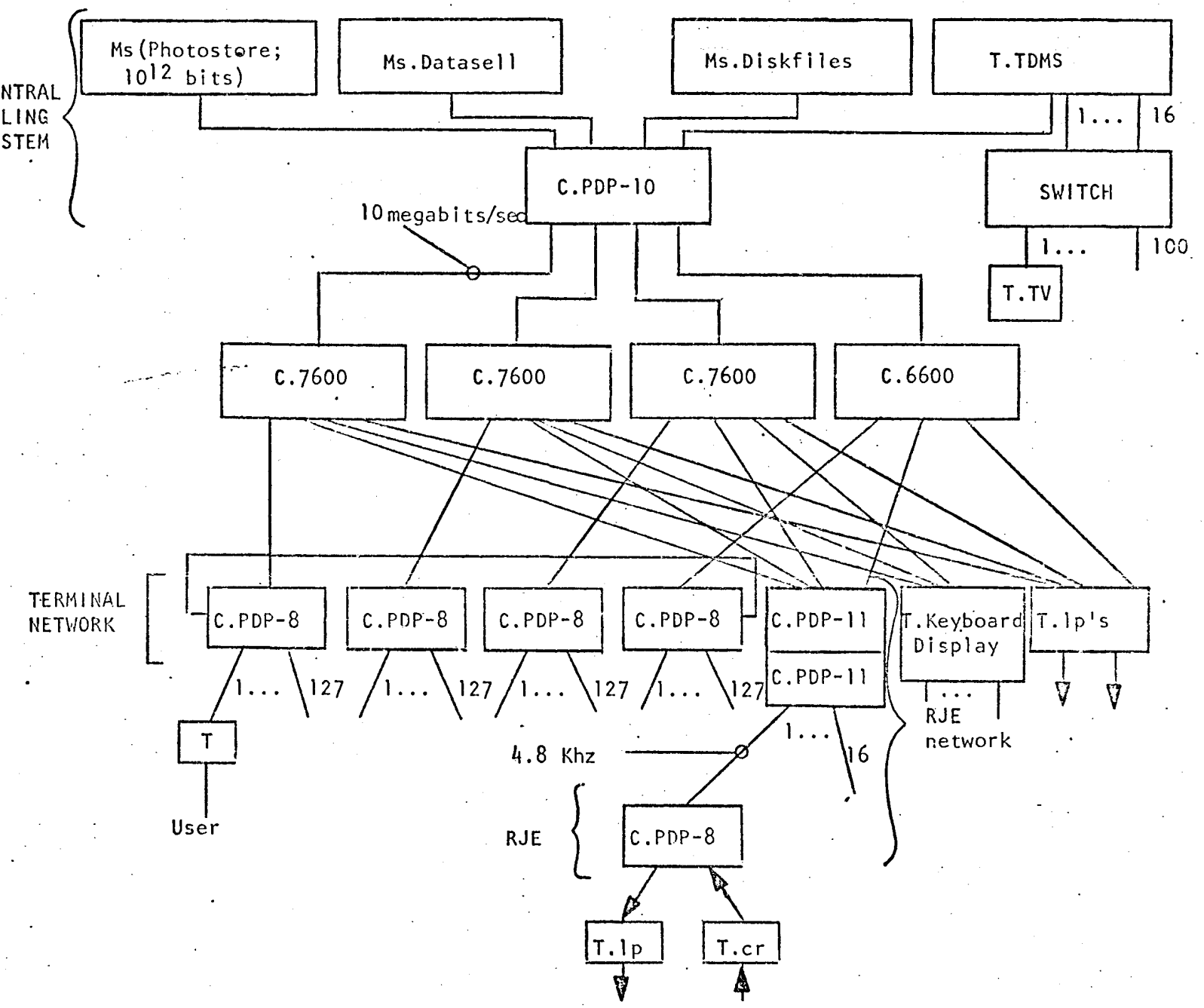

COPY
FCS - COPY SHIP

GB 2/2/76



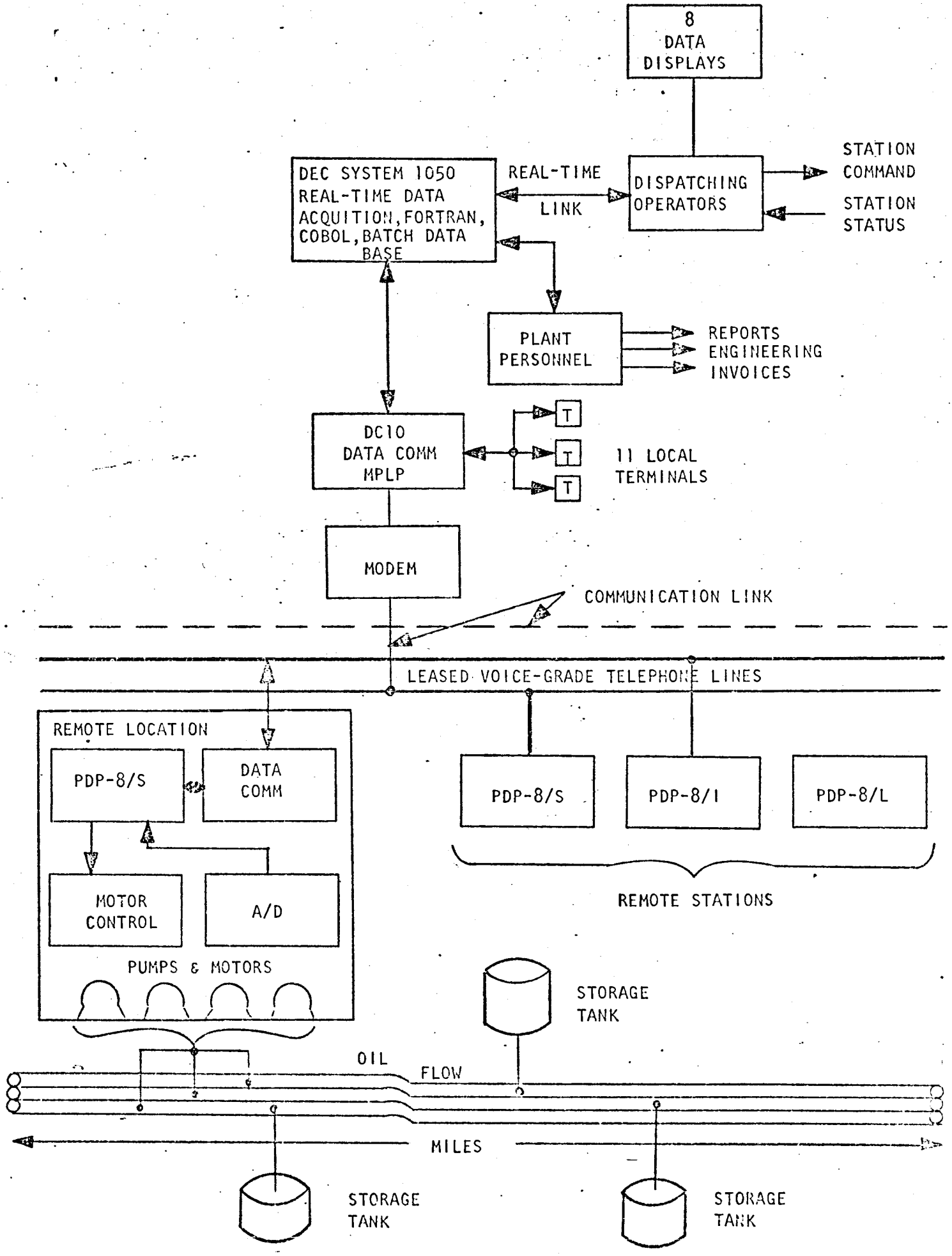
C.IMP - Computer as Interface Message Processor (stores and forwards messages).
C.TIP - Computer as Terminal Interface Processor (moves and forwards messages).
C.HOST Computer - Host (e.g. PDP-10, 360/91).
T - Terminal to user (e.g. Teletype, Execuport).
T.lp - Terminal - Line printer.

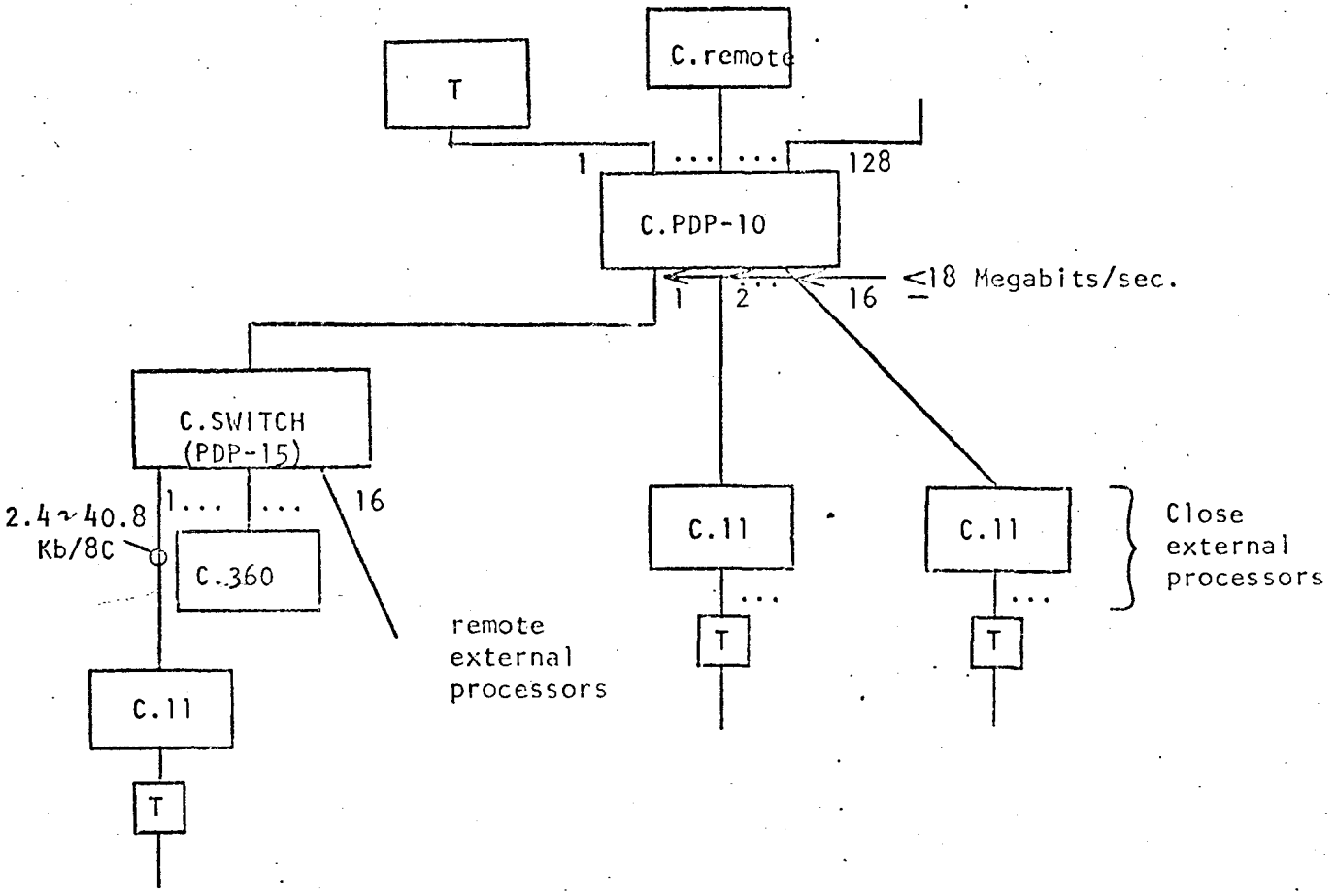
FIGURE 5. INTERCONNECTION STRUCTURE OF ARPA NETWORK



T - Teletype; T.lp - line printer; T.cr - card reader; T.tv - television display
T.TDMS - Television Display Monitor System

FIGURE 4. STRUCTURE OF LLL OCTOPUS NETWORK


8
DATA
DISPLAYS
DEC SYSTEM 1050
REAL-TIME DATA
ACQUITION, FORTRAN,
COBOL, BATCH DATA
BASE
REAL-TIME
LINK
DISPATCHING
OPERATORS
STATION
COMMAND
STATION
STATUS
PLANT
PERSONNEL
REPORTS
ENGINEERING
INVOICES
DC10
DATA COMM
MPLP
T
T
T
11 LOCAL
TERMINALS
MODEM
COMMUNICATION LINK
LEASED VOICE-GRADE TELEPHONE LINES
REMOTE LOCATION
PDP-8/S
DATA
COMM
MOTOR
CONTROL
A/D
PUMPS & MOTORS
PDP-8/S
PDP-8/I
PDP-8/L
REMOTE STATIONS
STORAGE
TANK
OIL
FLOW
MILES
STORAGE
TANK
STORAGE
TANK



C.PDP-10	Single or dual processor DECsystem 10 with TOPS 10 monitor.
C.11	PDP-11 Model 40 or 45 with RSX-11D monitor
C.remote	Any computer connected via standard asynchronous communications Link at 110, 300, 1200 or 2000 b/s.
C.360	Appears to a 360 or 370 as a HASP 2780 RJE Terminal

FIGURE 2. DEC LABORATORY INTERCONNECTION PROGRAMMING SYSTEM

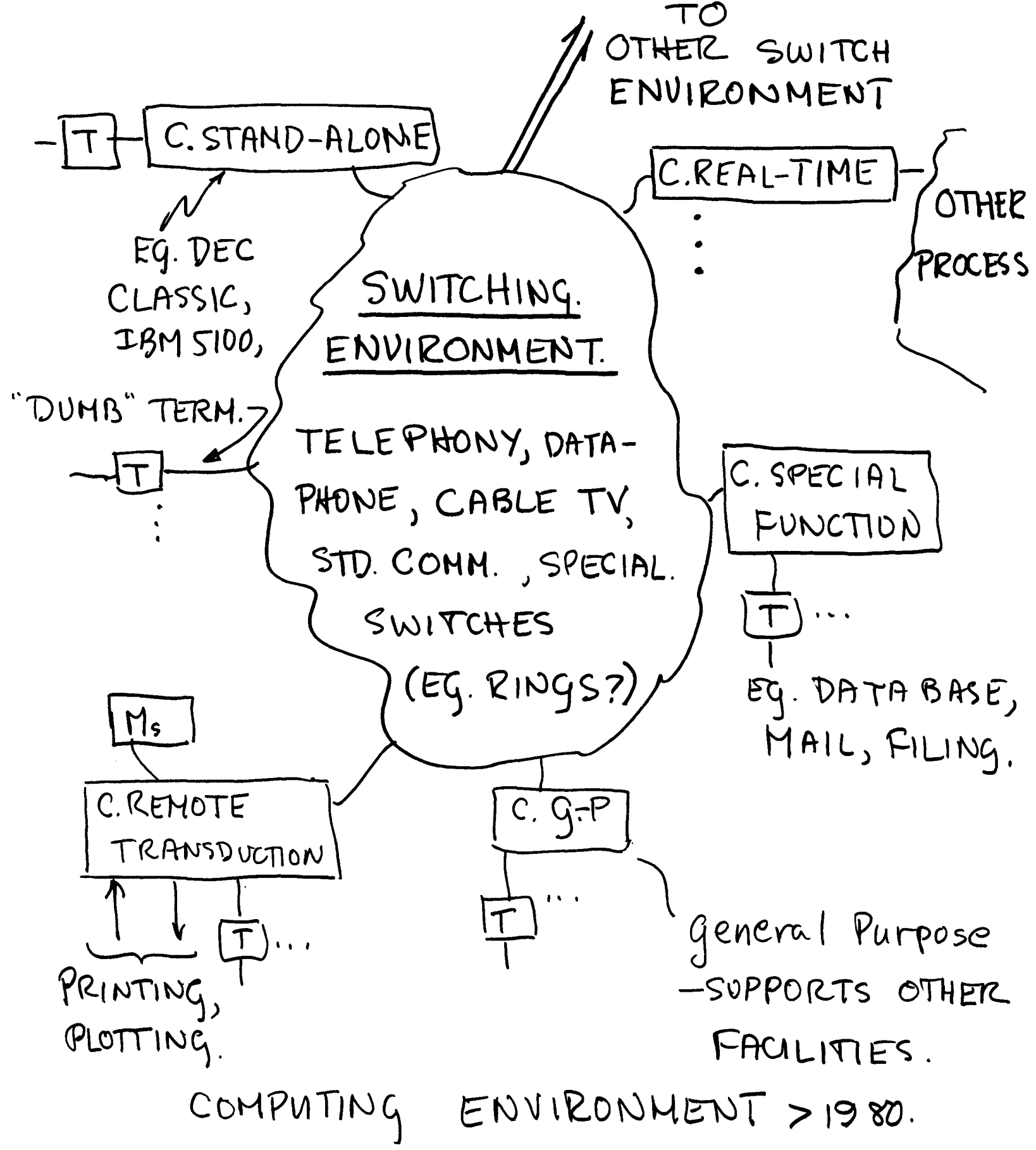
COSTS (1975)

	K/YEAR	#/HR @ 2400 HR.
HUMAN	0, 5, 10, 20, 40	0, 2, 4, 8, 16
COMPUTER	1.2 ~ 2.5	.5 ~ 1.
T	.25 ~ .75	.1 ~ .4
SERVICE	.05	.02
POWER	.005 ~ .01	.002 ~ .004
LINE (COMM.)	0 ~ 2.4	0 ~ 2
PAPER	0 ~ .1	1/3 ~ .10
SPACE	.05 ~ .1	.02 ~ .04

2/9/76

1967	PRICE(K$)	WL	Mp.Size	$/BIT ×100	MIPS × WL	MIPS (REAL)	PERF/ COST
8	10(1)	12(1)	.05 (1)	20	.3(1) (1)	.002(1)	30
6600	3K(300)	60(5)	8Mb(160)	38	3(10) (50)	3(1500)	1
1975							
11	1(1)	16(1)	4Kw (1)	1.6	.3(1) (1)	.04(1)	300
LARGE	10^4 (10^4)	64(4)	1Mw (10^3)	16	100(10K)(40K)	100(2500)	10

LARGE & SMALL MACHINES
1967 & 1975



COMPUTING ENVIRONMENT > 1980.

	SMALL (DECENTRAL.)	LARGE (CENTRAL)
PERF.	• > AVG.	• >>PEAK. • > M_p. PEAK.
COST	• EC. THROUGH PROD.	• ONLY DISK EC. OF SCALE
	• f (COMM. COSTS, UTILIZATION).	
	• PRODUCTION LIMITED	• DESIGN LIMITED
	• OVHD HIDDEN — USER IS SYSTEMS PROGRAMMER	
USE	• SMALL (OR 0) DATA BASE	• LARGE DATA BASE
	• FIXED, WELL-DEFINED COMPUTATION (EG. TEXT, CAI, STAT. CALC.)	• FULLY GEN. PURP.
SECURITY	• PRIVATE	• EASY TO SHARE, BREAK.
RELIABLE	• DIST.	• CENT + COMM.

C. SYSTEMS PROBLEMS

- CHARACTERIZING COMPUTATION
- ISP SELECTION/DESIGN
- USER ARCHITECTURE
  BASIC MACHINE SELECTION, CONFIG's
- MANUFACTURER ARCHITECTURE
  MODELS, CORRECT CONFIGS, PERF
- MEMORY HIERARCHY MODEL
- OP. SYS. SPECIFICATION, DESIGN, MODELING
- BUS (SWITCH) SPECIFICATIONS.
- STANDARDS FOR PORTABILITY.
  (LANGUAGES, PROTOCOLS, LOW-LEVEL PRIM.)
- UTILIZATION OF MULTIPROCESSORS.
- COMPUTER MODULES.
- COMPUTERS THAT WON'T FAIL.

SYSTEM COSTS

	PURCHASE (K$)	COST/USER/YR
DESK CALC.	5	1.3
IBM 5100	17	4.4
DEC CLASSIC	10	3
SMALL (8) USER	50	2.8
MID (32) USER	100	1.4
LARGE GP-MINI (20/50)	250	2.2~5.5
DEC 10	750	6
50 USER LARGE	3000	20

PARALLELISM: BASIS FOR MULTI-PC's

- INDEPENDENT PARTITIONS: — DYNAMIC STOCKROOM. ← STATIC (I.E. RELIABLE)
- FUNCTIONAL SEPERATION — FRONT/BACK END / PRE-PROC. /

- INDEPENDENT
  - JOBS (T/S)
  - PROCESSES (TRANSACTION PROC.,
  - BATCH. STREAMS
- SET PARALLELISM (PROC. CONT)
- ARRAYS, VECTORS
- GENERALLY CONCURRENT PROCESSES.

BASIC RATIONALE FOR m P's

USER
- PERFORMANCE
- Δ PERFORMANCE AND RANGE
- AVAILABILITY VIA REDUNDANCY

MFG.
- COST (BETTER SPARES, MANUFACTURING, LESS DESIGNS

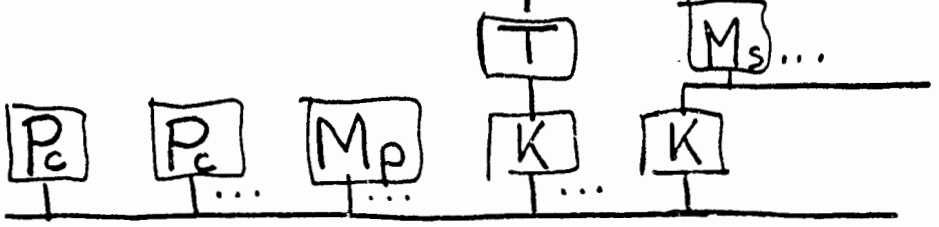
BASIC IRRATIONALE FOR m P's

- NO-PROGRAMS
- HIGH DEV. RISK.
- UNIPROCESSORS ARE MORE COST/EFF.
- BETTER PLAN

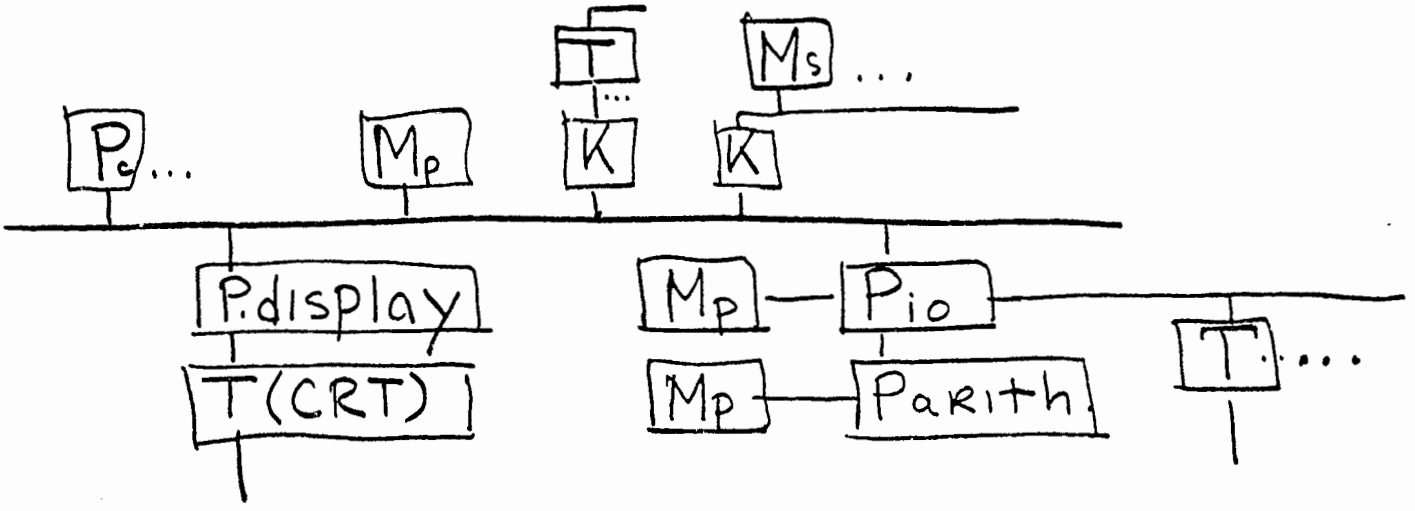
$$\#\frac{\text{ACCESSES}}{\text{SEC}} = \frac{m}{t_c}\left(1-\left(1-\frac{1}{m}\right)^P\right)$$

$$= \frac{m}{t_c}\left(1-1/e\right) \quad \text{for } m=\infty \text{ and } P=m.$$

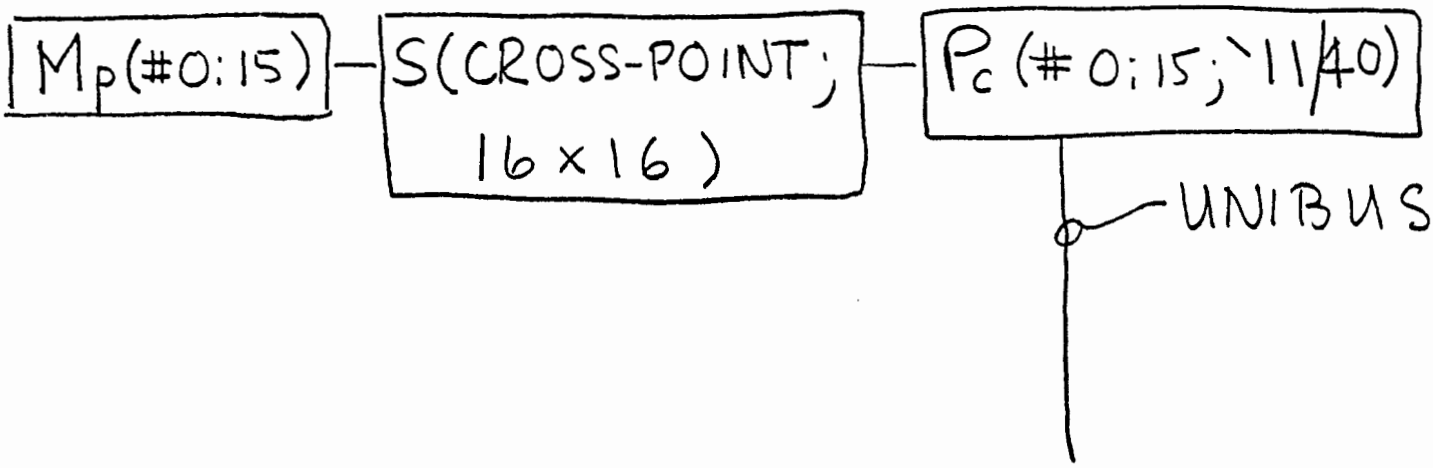
$$= \frac{m}{t_c} \times .67.$$



MULTI- Pc USING 1 BUS



MULTI- SPECIAL Pc , 1 BUS



MULTI-Pc WITH 16 Mp's.

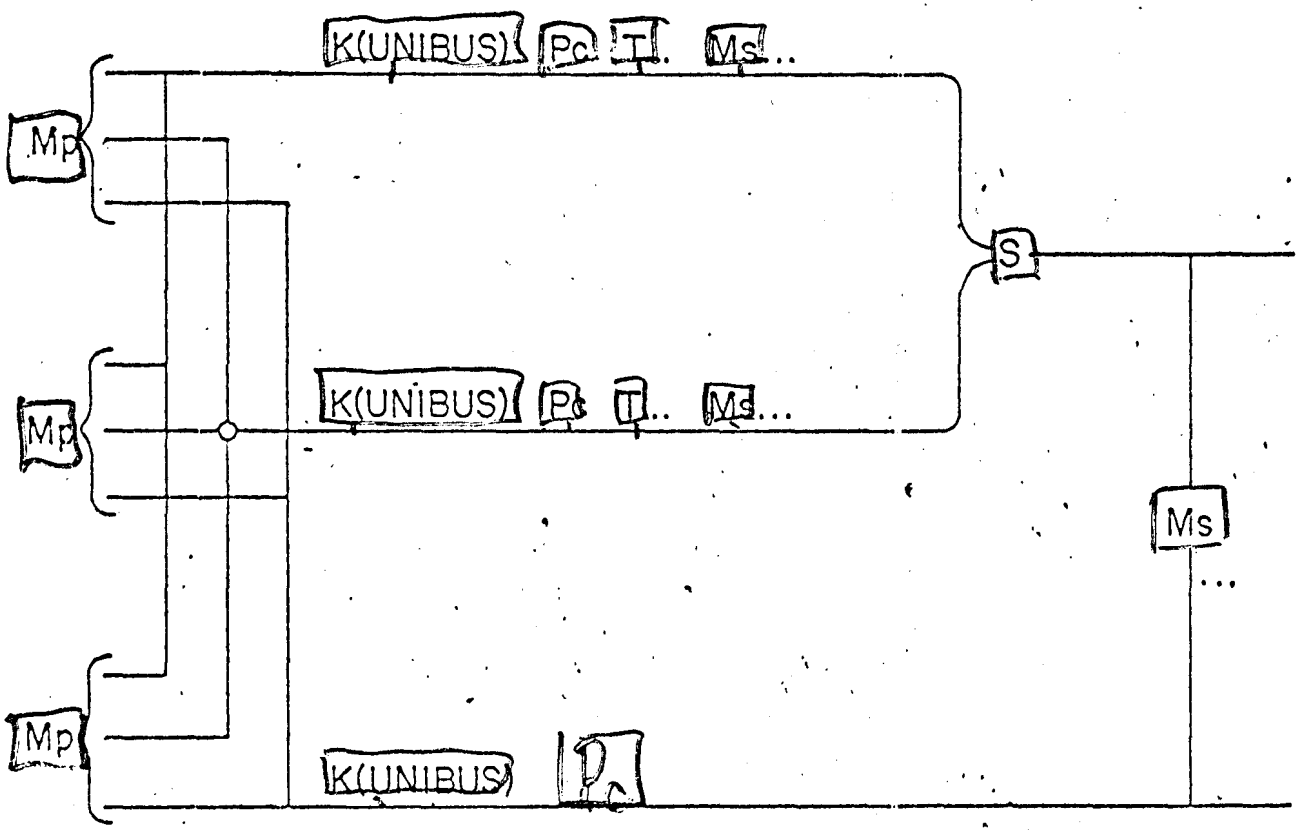
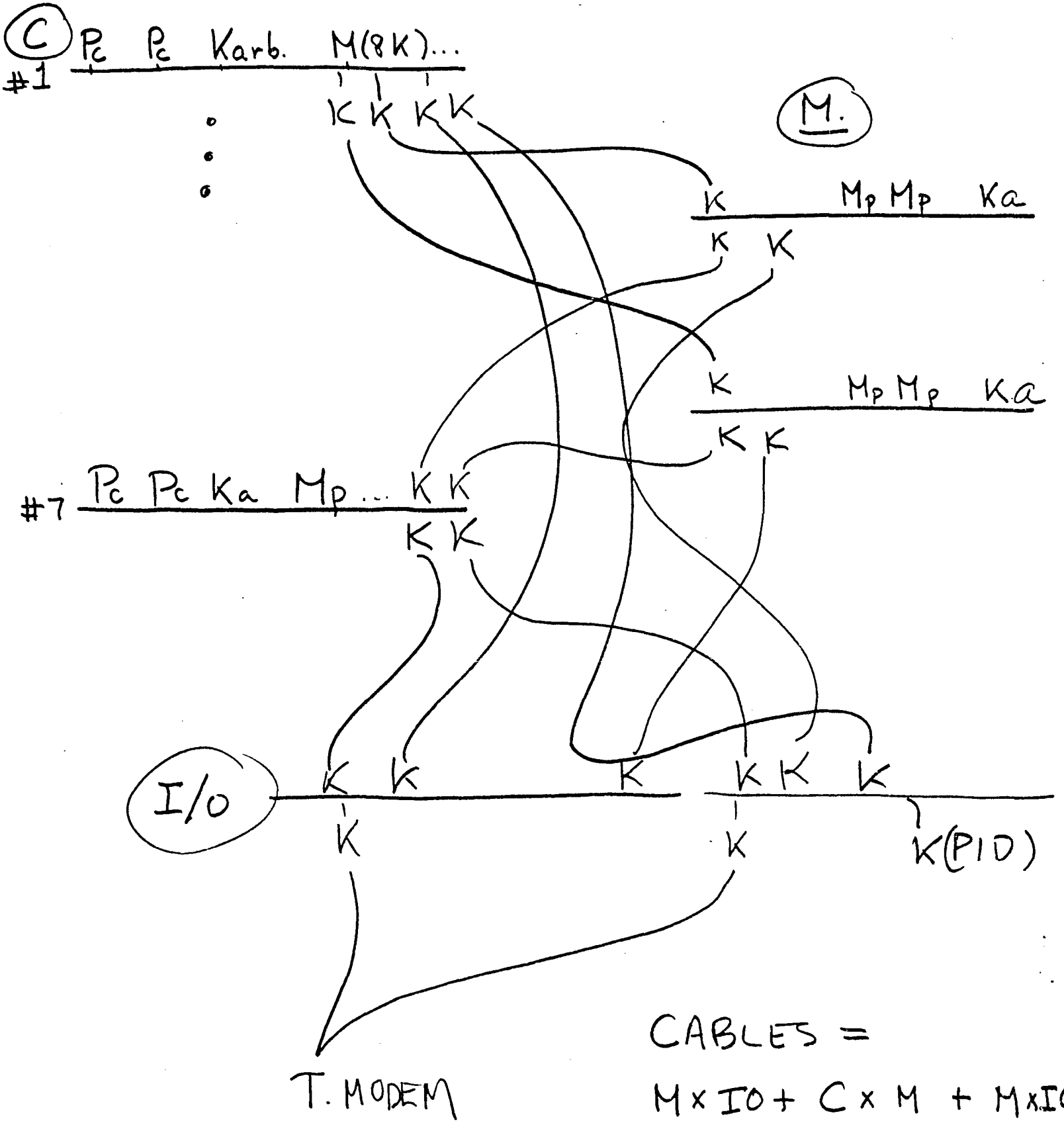


FIGURE DP USE OF DUAL Pc MULTIPROCESSOR SYSTEM WITH PROCESSOR-LESS UNIBUS FOR I/O DATA TRANSMISSION (FROM BELL ET AL, 1970)



CABLES =

M x IO + C x M + M x IC

2 x 2 + 7 x 2 + 2 x 8

= 22

PLURIBUS SYSTEM. (BBN)

#PC	Mp	PC.Perf	PC.PRICE	Price/Perf	Sys Price	Price/Perf
1	.6	1	1	1	3.	1
2	1.15	1.85	1.23	.66	3.23	.58
3	1.42	2.4	1.47	.61	3.47	.48
40		2.25	1.35	.6	3.35	.49

C.mmp

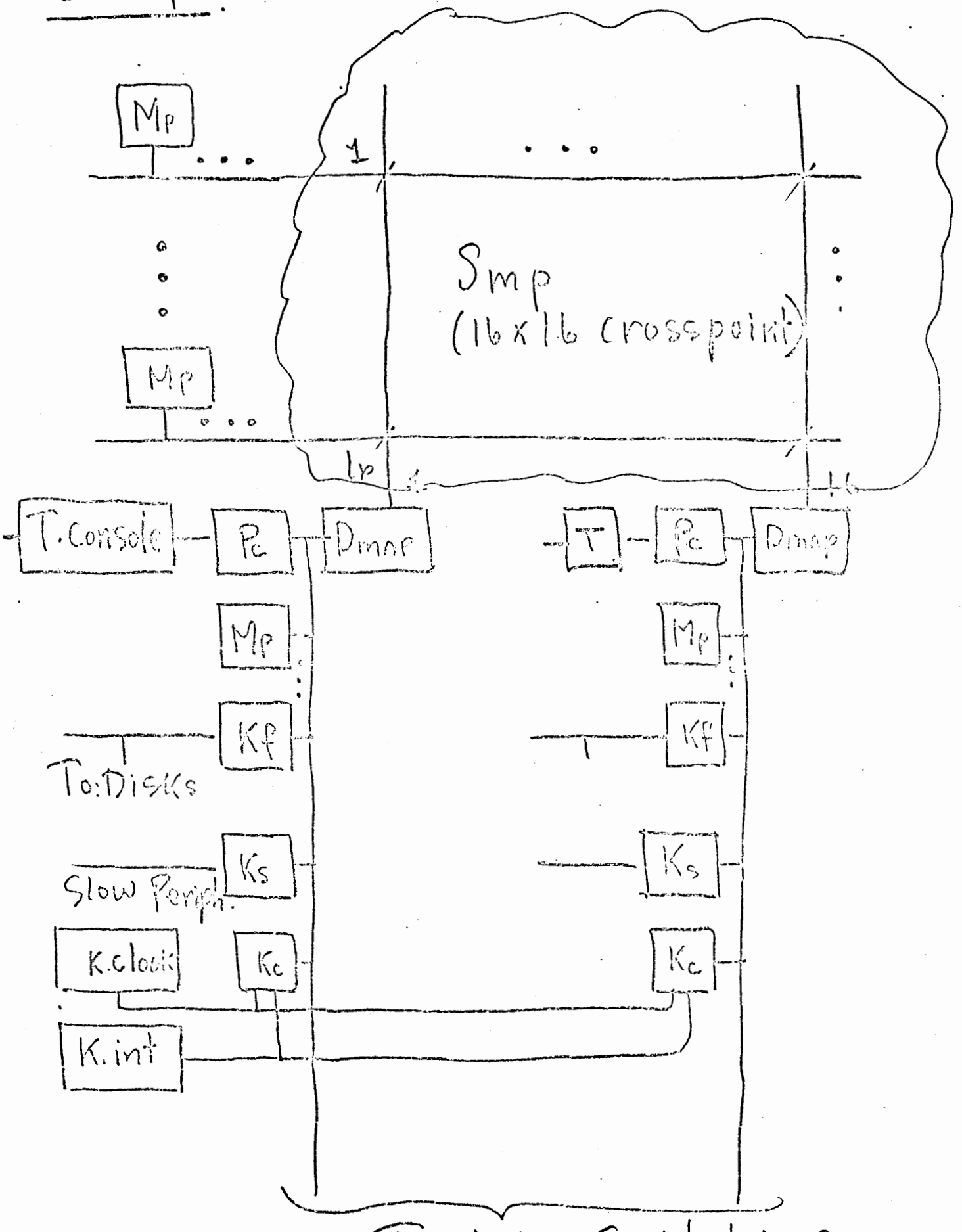

Mp
Mp
1
16
Smp
(16x16 crosspoint)
Lp
T.Console
Pc
Dmap
T
Pc
Dmap
Mp
Mp
Kf
Kf
To:Disks
Ks
Ks
Slow Perph.
K.clock
Kc
Kc
K.int
To i/o Switching.

Fig. 4b. Performance vs Pc's for 8 Mp; Pc(#2; tp: 450 ns)

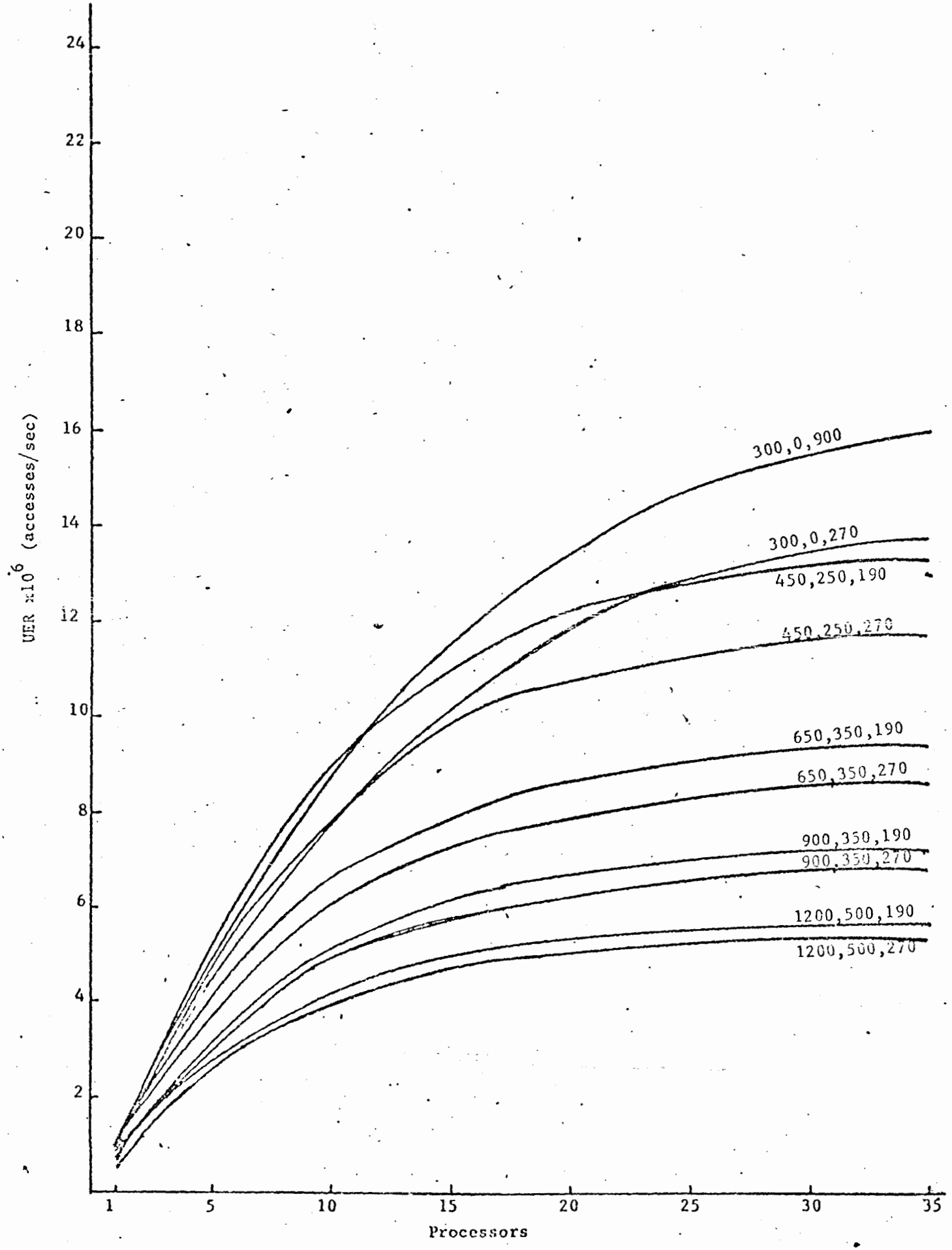
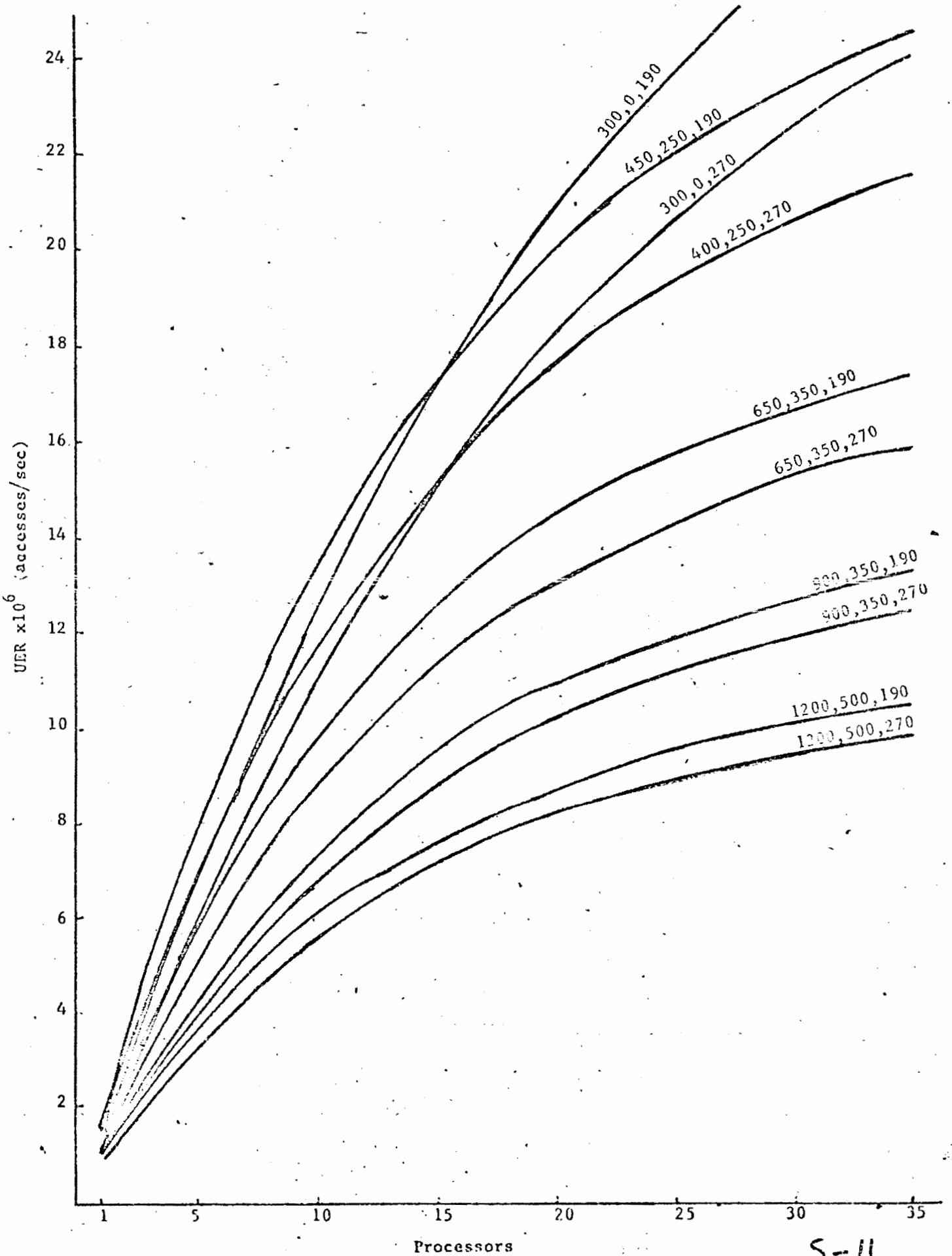
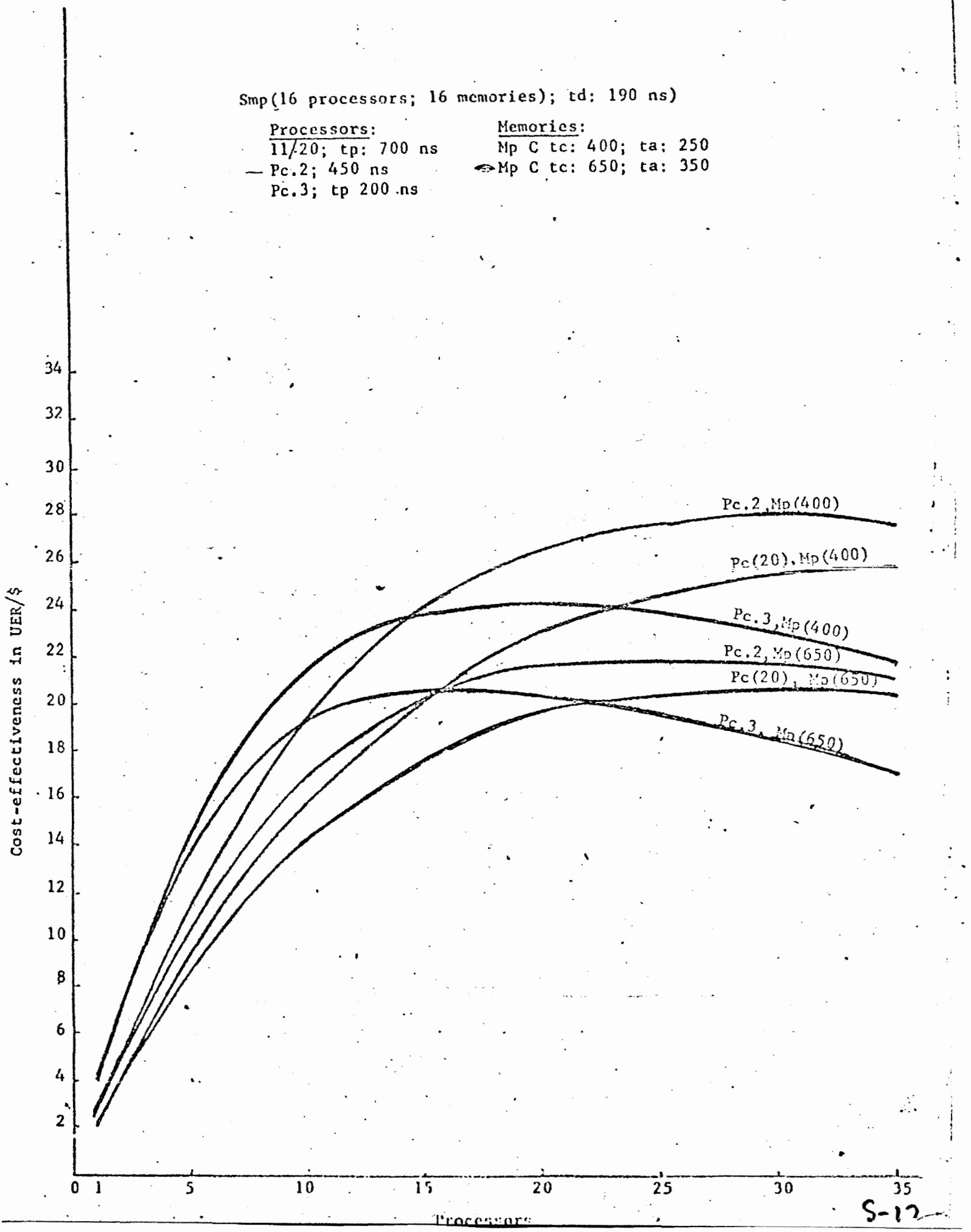


Fig. 4f. Performance vs Pc's for 16 mp



S-11

Fig. 5. Cost effectiveness (UER/$) vs Pc's.



DEFINITIONS

N-Computer Networks - Computers loosely coupled via Comm. L's.

CM-Computer Modules - Tightly coupled C's... possibly sharing Mp.

mP- Multi-procesor Computer- A number of processors sharing a common, Mp.

STRUCTURES

1. MULTI-PROCESSOR - mP
2. COMPUTER MODULES - Cm
3. NETWORKS.

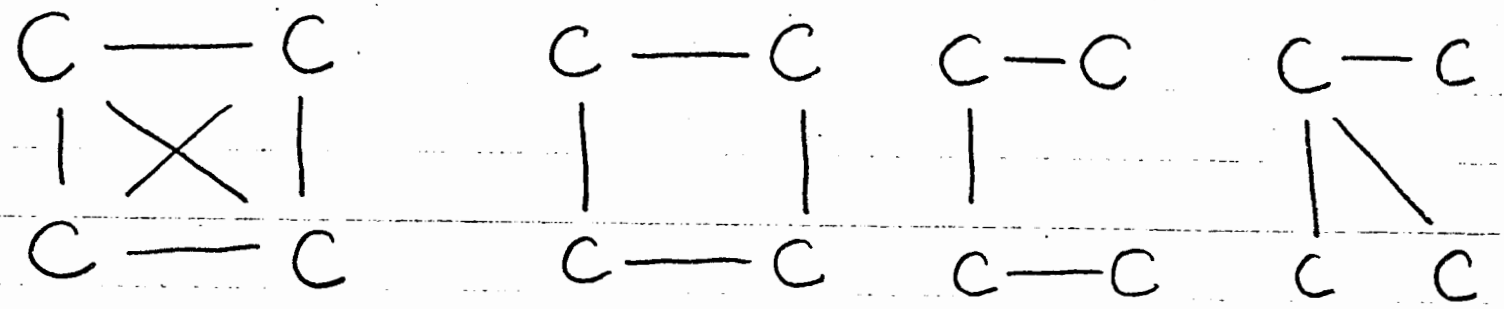
PROBLEM / OBJECTIVE FCN

1. LOCATION OF "WORK"; PEOPLE
2. REQ. FOR P_c, M_p, M_s, AVAILABILITY.

TRADEOFFS

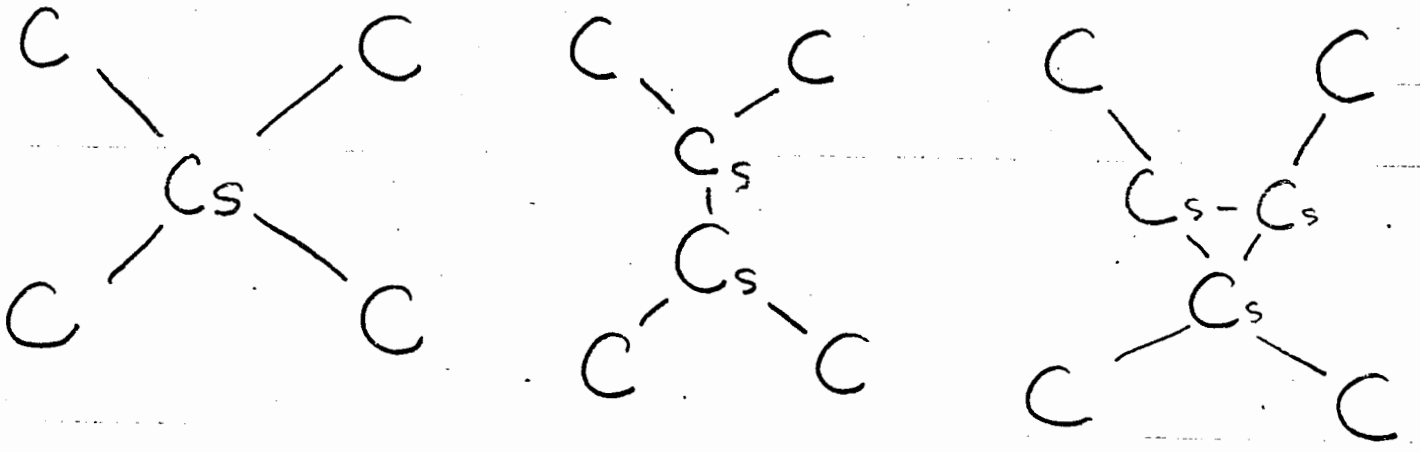
	+	− (and COST)
mP	LESS M_p, L, MORE P_c AVAIL; CONFG. TO MAINTAIN	SM_p; INTEGRAL SYSTEM.
Cm	FUNCTIONAL ISOLATION	M_p, Links, P_c (ABILITY TO MATCH/MOVE WORK)
N	LESS FCN. ISOLATE. COMM. LINKS.	SAME AS Cm ~~(LINKS MORE)~~

DIRECT INTERCONNECT

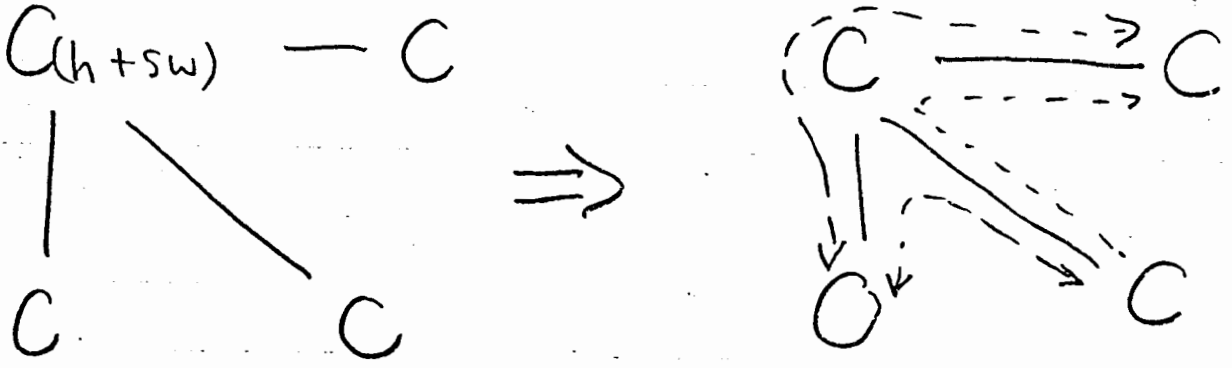


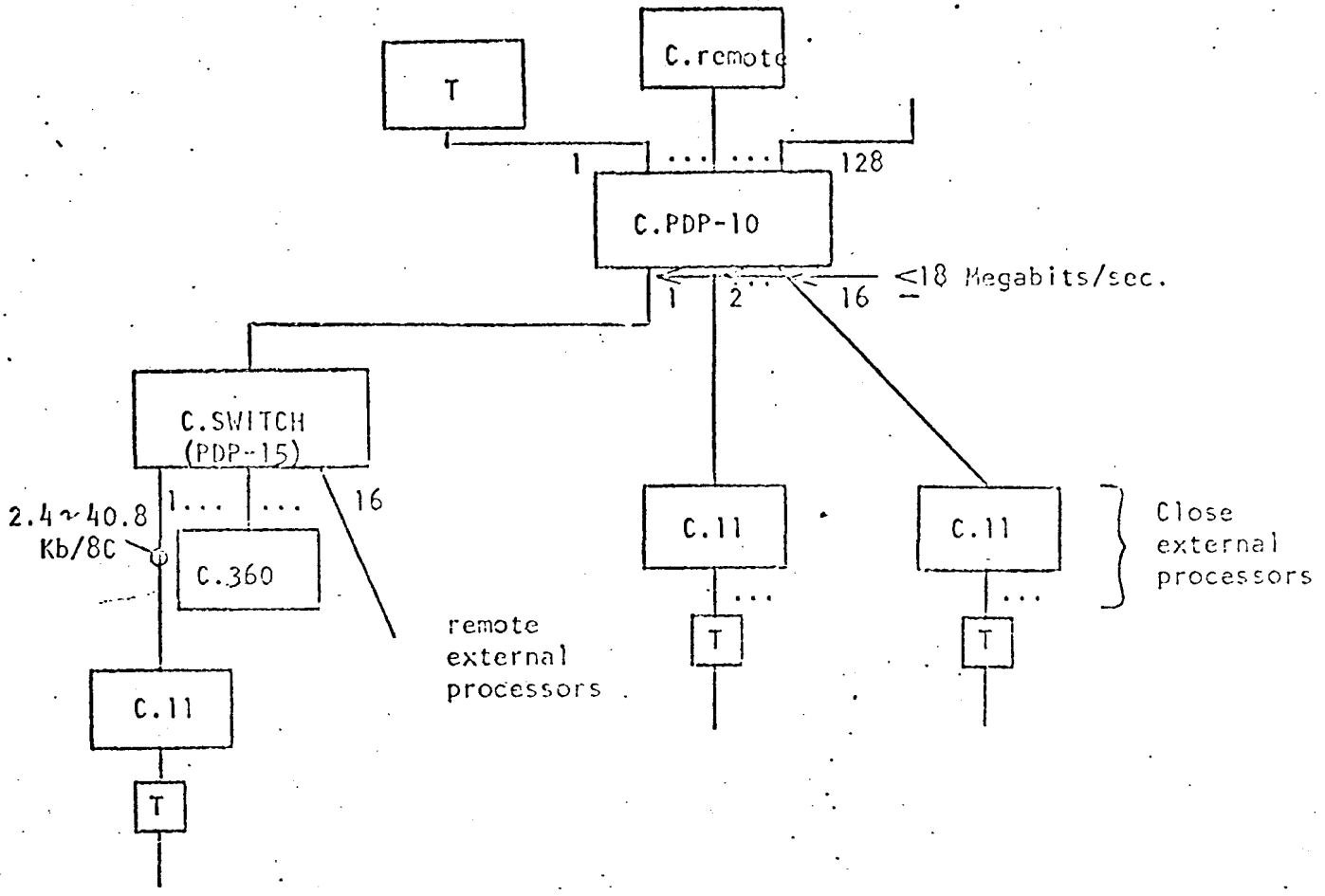
EXHAUSTIVE RING CHAIN STAR

S/F NETS W/ Csw's.



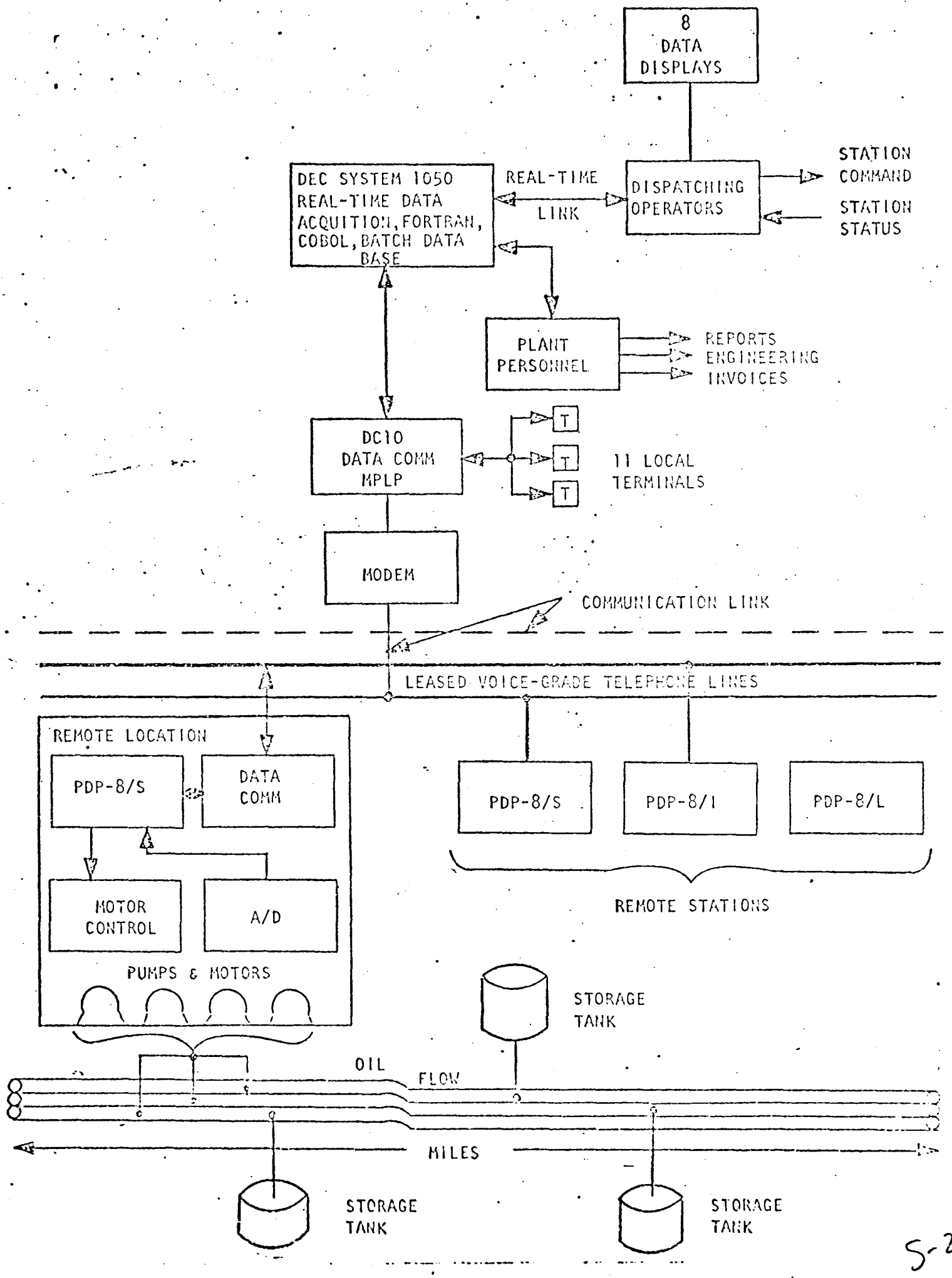
Hybrid.

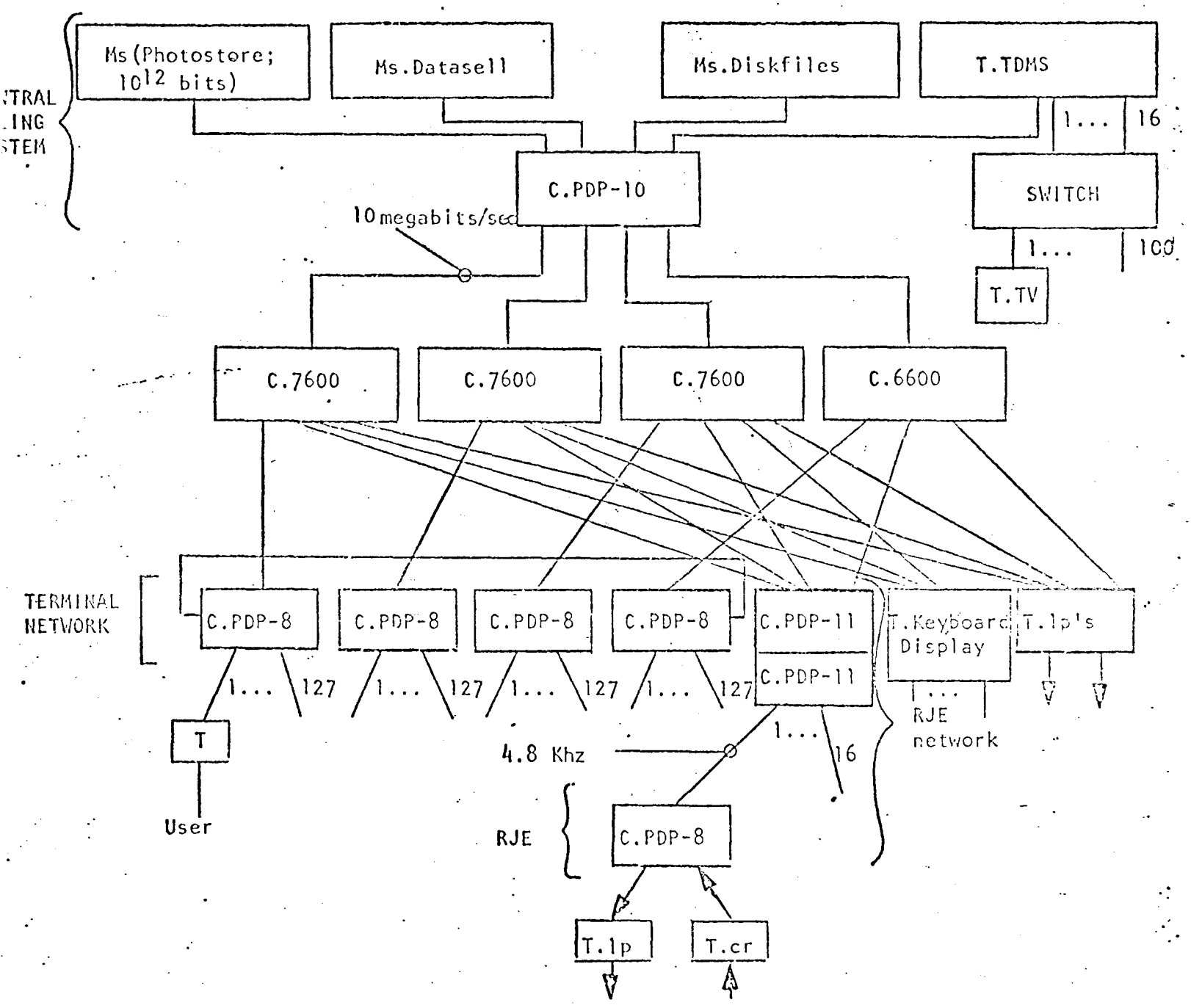




C.PDP-10	Single or dual processor DECsystem 10 with TOPS 10 monitor.
C.11	PDP-11 Model 40 or 45 with RSX-11D monitor
C.remote	Any computer connected via standard asynchronous communications Link at 110, 300, 1200 or 2000 b/s.
C.360	Appears to a 360 or 370 as a HASP 2780 RJE Terminal

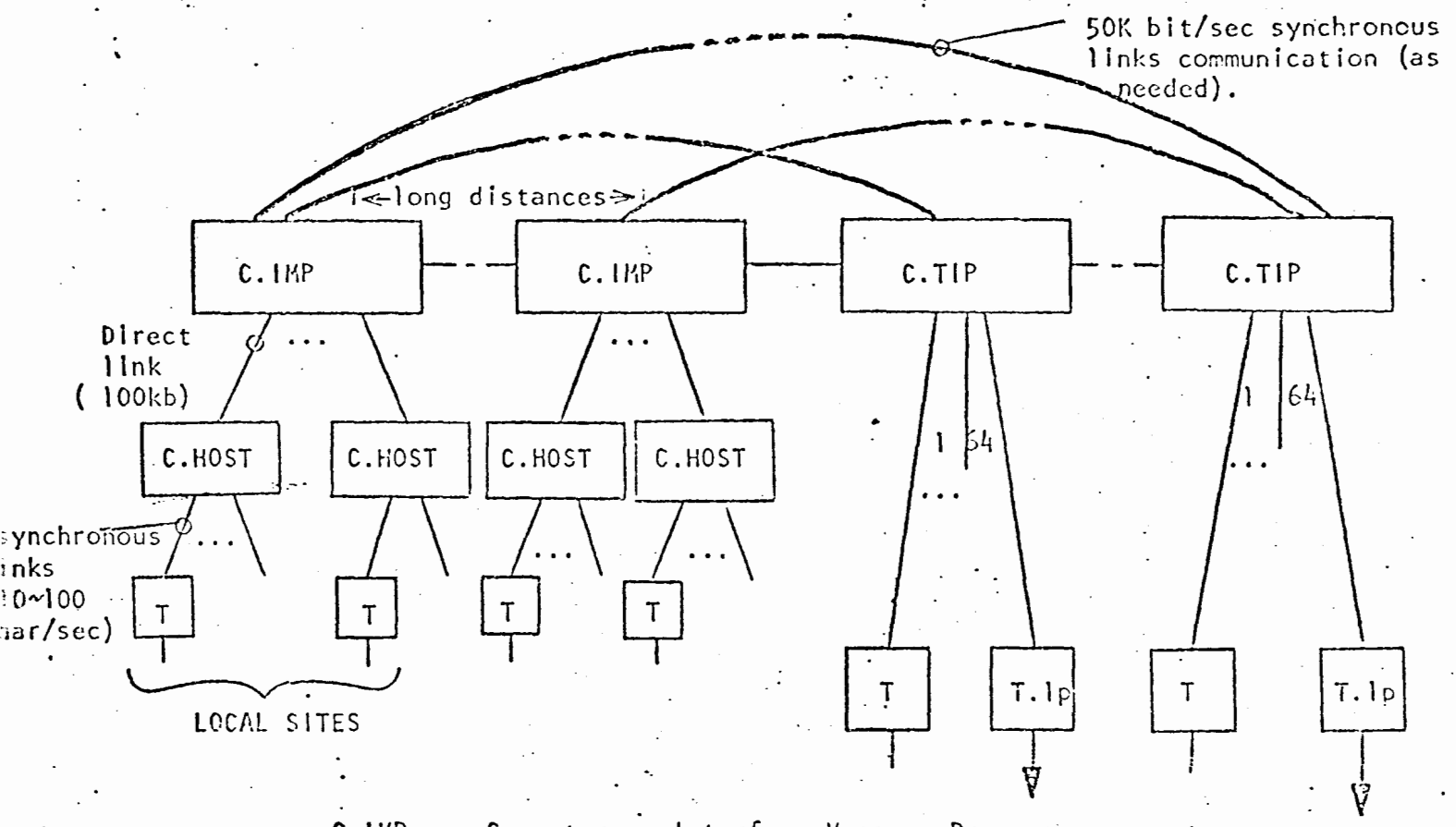
FIGURE 2. DEC LABORATORY INTERCONNECTION PROGRAMMING SYSTEM


8
DATA
DISPLAYS
DEC SYSTEM 1050
REAL-TIME DATA
ACQUITION, FORTRAN,
COBOL, BATCH DATA
BASE
REAL-TIME
LINK
DISPATCHING
OPERATORS
STATION
COMMAND
STATION
STATUS
PLANT
PERSONNEL
REPORTS
ENGINEERING
INVOICES
DC10
DATA COMM
MPLP
T
T
T
11 LOCAL
TERMINALS
MODEM
COMMUNICATION LINK
LEASED VOICE-GRADE TELEPHONE LINES
REMOTE LOCATION
PDP-8/S
DATA
COMM
MOTOR
CONTROL
A/D
PUMPS & MOTORS
PDP-8/S
PDP-8/I
PDP-8/L
REMOTE STATIONS
STORAGE
TANK
OIL
FLOW
MILES
STORAGE
TANK
STORAGE
TANK



T - Teletype; T.lp - line printer; T.cr - card reader; T.tv - television display
T.TDMS - Television Display Monitor System

FIGURE 4. STRUCTURE OF LLL OCTOPUS NETWORK



C.IMP - Computer as Interface Message Processor (stores and forwards messages).
C.TIP - Computer as Terminal Interface Processor (moves and forwards messages).
C.HOST Computer - Host (e.g. PDP-10, 360/91).
T - Terminal to user (e.g. Teletype, Execuport).
T.lp - Terminal - Line printer.

FIGURE 5. INTERCONNECTION STRUCTURE OF ARPA NETWORK

TABLE PARAMETERS OF LARGE AND SMALL COMPUTERS 1967 AND 1975

ACTUAL AND (RELATIVE)

1967	COST (K$)	WL	Mp.Size	$/bitx100	MIPS	MIPS X WL	REAL (MIPS)	PERF/COST (MIPS/MS)
8	10(1)	12 (1)	.05Mb(1)	20	.3 (1)	(1)	.002 (1)	30
6600	3K(300)	60 (5)	8Mb(160)	38	3(10)	(50)	3 (1500)	1
1975								
LSI-11	1(1)	16 (1)	4Kw(1)	1.6	.3 (1)	(1)	.04 (1)	300
Large	10K(10^4)	64 (4)	1Mw(10^3)	16	100 (10K)	(40K)	100(2500)	10

Some Observations:

1. Performance: small is about the same, except for floating point. Large up 30.
2. Cost: small is cheaper by X10. Large up X3.
3. Mp.size no economy of scale.

GB
9/5/75

ENGINEERING FORECAST FOR RS1011 FH DISK — PREPARED ON 24-APR-74

Project No: 10-000 Proposal Date: 01-Jun-73 Approved: Products Committee 01-Oct-73

Product Manager: John Discus Project Engineer: Hy Density

Description: 10 megaword FH disk, 1ms avg access, 1us xfer rate

Goals: Improve performance of VIROS, RSX, RSTS Operating Systems

Requested by: Disk Steering Group; Software Engineering

HISTORY:	START DESIGN	OPERATE PROTO	LIMITED RELEASE	PUBLIC ANNOUNCE	FIRST CUST. SHIP	PRICE ($/UNIT)	MFG. COST ($/UNIT)	COMMENTS
01-Jun-73	Jul 73	Jul 74	Dec 74	Jan 75	Mar 75	$22,500	$1,500	Original Plan
01-Oct-73	Jul 73	Jul 74	Dec 74	Jan 75	Mar 75	$22,500	$3,000*	2ms avg access
01-Apr-74	Jul 73	Oct 74*	Mar 75*	Apr 75*	May 75*	$22,500	$5,000*	New price, sched

PRODUCT LINE	FORECAST DATE	FY74 Q4	FY75 Q1	Q2	Q3	Q4	FY76 Q1	Q2	Q3	Q4	FY77 Q1	Q2	Q3	Q4	FY78 Q1	Q2	Q3	Q4	FORECASTER
DECsys-10	01-Oct-73				5	20	25	30	30	35	40	40	45	45	45	45	50	50	J. Leng
	01-Apr-74				0	25	25	30	30	35	40	40	45	45	45	45	50	50	J. Leng
LDP-11/45	01-Oct-73				2	4	6	6	7	7	6	7	8	9	7	7	6	10	L. Data
	01-Apr-74				0	10	3	3	8	1	9	1	1	2	4	1	1	8	Anna Log
IND-11	01-Oct-73						2	2	2	4	3	3	3	5	4	4	4	6	R.T. Exec
	01-Apr-74							2	2	4	3	3	3	5	4	4	4	6	R.T. Exec
TOTAL	01-Oct-73				7	24	33	38	39	46	49	50	56	59	56	56	60	66	TOTAL
	01-Apr-74				0	35	28	35	40	40	52	44	49	52	53	50	55	64	TOTAL

FIGURE 3 SAMPLE FORMAT FOR PRODUCT PLAN CHARTS

/ale

FIGURE 2 TECHNOLOGY/PRODUCT PLANNING AND PRODUCT BUDGETARY PROCESS

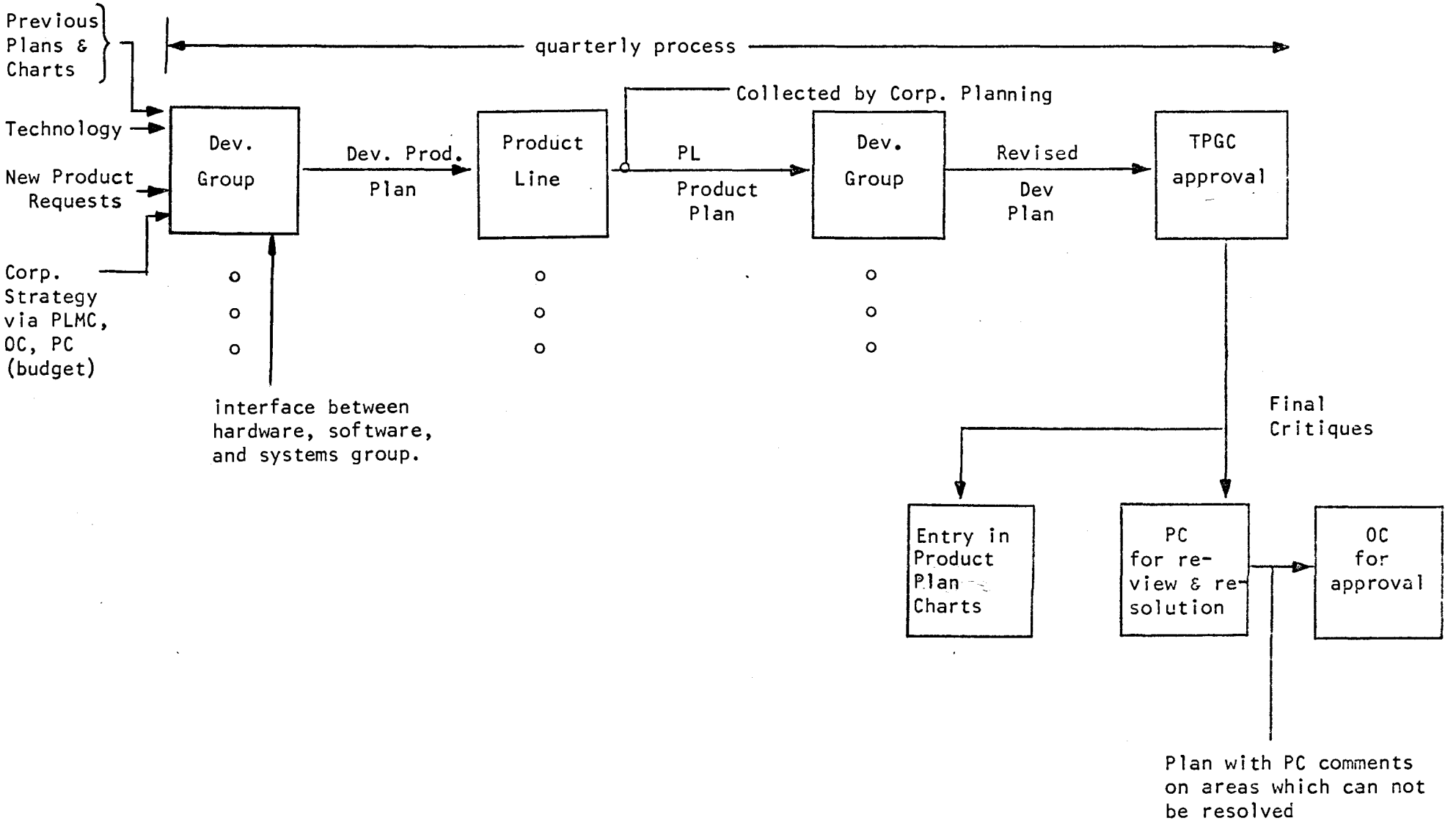


FIGURE 1

DEVELOPMENT PROCESS
(Function of Time)

PRODUCT PHASE	ACTIVITIES (AND GATE TO NEXT PHASE)	BUSINESS PLAN PHASES
Preconcept	Request to study by PC, PLM, Dev. Mgr., etc.	
	--Development Manager approves--	
Study (1/4-1/2 year)	PRODUCT MANAGER APPOINTMENT	
	--TPGC approves--	
Proposal (1/4-1/2 year)		Original Business Plan Development with sales projection.
	--TPGC recommends; PLMC reviews; PC approves--	
Design and Tool (1-2 years)	Design Reviews by Eng. Committee Mfg./Eng. Committee reviews Mfg. Plan	Manufacturing part Support part (training & service) Sales part
	--TPGC recommends; PC revies; PLMC approves--	
Produce, Sell Support (2-3 years)	--TPGC recommends; PC approves--	--Rejuvenation plan (redesign)
	--TPGC recommdns; PLMC approves--	
Rejuvenate (1-2 year)		Traditionalize plan.
	--TPGC recommends; PLMC approves--	
Traditionalize (? years)		
	--TPL Manager recommends; PLMC approves--	
Death (4 1/2 - 8 yrs)		

APPENDIX B

TECHNOLOGY/PRODUCTS STEERING COMMITTEES & SEMI-ANNUAL WOODS MEETINGS MEMBERSHIP

			PRODUCT LINES										HARDWARE ENGINEERING								SOFTWARE						
SUBJECT	CHAIRMAN	DATES-WOODS MTG	Component	OEM	CSS	IPG	DCM	BUS	TYPE	LAB	COMP	DECsys-10	Tape	Disk	Memory	Terminal	11-Small	11-Med/Lg	8	10	Eng	Sup	Mfg.	Diag.	Field Ser.	Sales	Off. of Dev.
8 Systems	Clarke	08/28/74																									
		03/12/75	X	X		X		X					X	X	X	X	X		X		X	X	X	X	X	X	X
11-Small & RT Op. Sys	Teicher/ Thissell	06/26/74																									
		01/22/75	X	X		X		X	X	X	X		X	X	X	X	X	X	X		X	X	X	X	X	X	X
11 Med & Large	Demmer	07/24/74																									
		02/05/75	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X
DECsys-10	Wilhelm	10/16/74																									
		04/16/75										X	X	X	X	X		X		X	X	X	X	X	X	X	X
Terminals (LA,VT,LR)	Corell/ Stockebrand	08/14/74																									
		02/19/74	X	X	X	X	X	X	X	X	X	X				X		X			X		X	X	X	X	X
Graphic Term.	Hallo/ Holman	09/25/74																									
		03/26/75			X	X	X	X	X	X	X	X					X	X					X	X	X	X	X
Networks & Comm	Stackpole/ Bastiani	10/23/74																									
		04/23/75		X	X	X	X			X	X	X						X		X	X	X		X	X		X
Disk	Saviers	05/22/74																									
		11/06/74																									
		06/11/75	X	X	X	X	X	X	X	X	X	X		X			X	X	X	X			X	X	X	X	X
Tape	Peyton	05/22/74																									
		11/20/74																									
		06/11/75	X	X	X	X	X	X	X	X	X	X	X				X	X	X	X			X	X	X	X	X
Core & MOS	Lemaire	05/29/74																									
		11/20/74																									
		05/21/75	X	X		X	X			X	X	X			X		X	X	X	X			X		X	X	X
PS & PKG & Modules	Rey/Nevala /Moffa	06/12/74																									
		12/18/74																									
		06/25/75	X	X						X		X		X		X	X	X	X						X		X
LSI	Gale	07/10/74																									
		01/08/75											X	X	X	X	X	X	X	X							X
R & D	J. Bell	07/10/74																									
		01/08/75											X	X	X	X	X	X	X	X							X
Diagnostics	Plowman	09/18/74																									
		04/30/75											X	X	X	X	X	X	X	X	X	X	X	X	X	X	
MFG. Test	O'Connor	12/11/74											X	X	X	X	X	X	X	X	X	X	X	X	X	X	

NOTE: WOODS MEETINGS INVITATIONS SHOULD ALSO BE EXTENDED TO OPERATIONS COMMITTEE AND PRODUCT LINE MANAGERS

A. Sharon
04/24/74

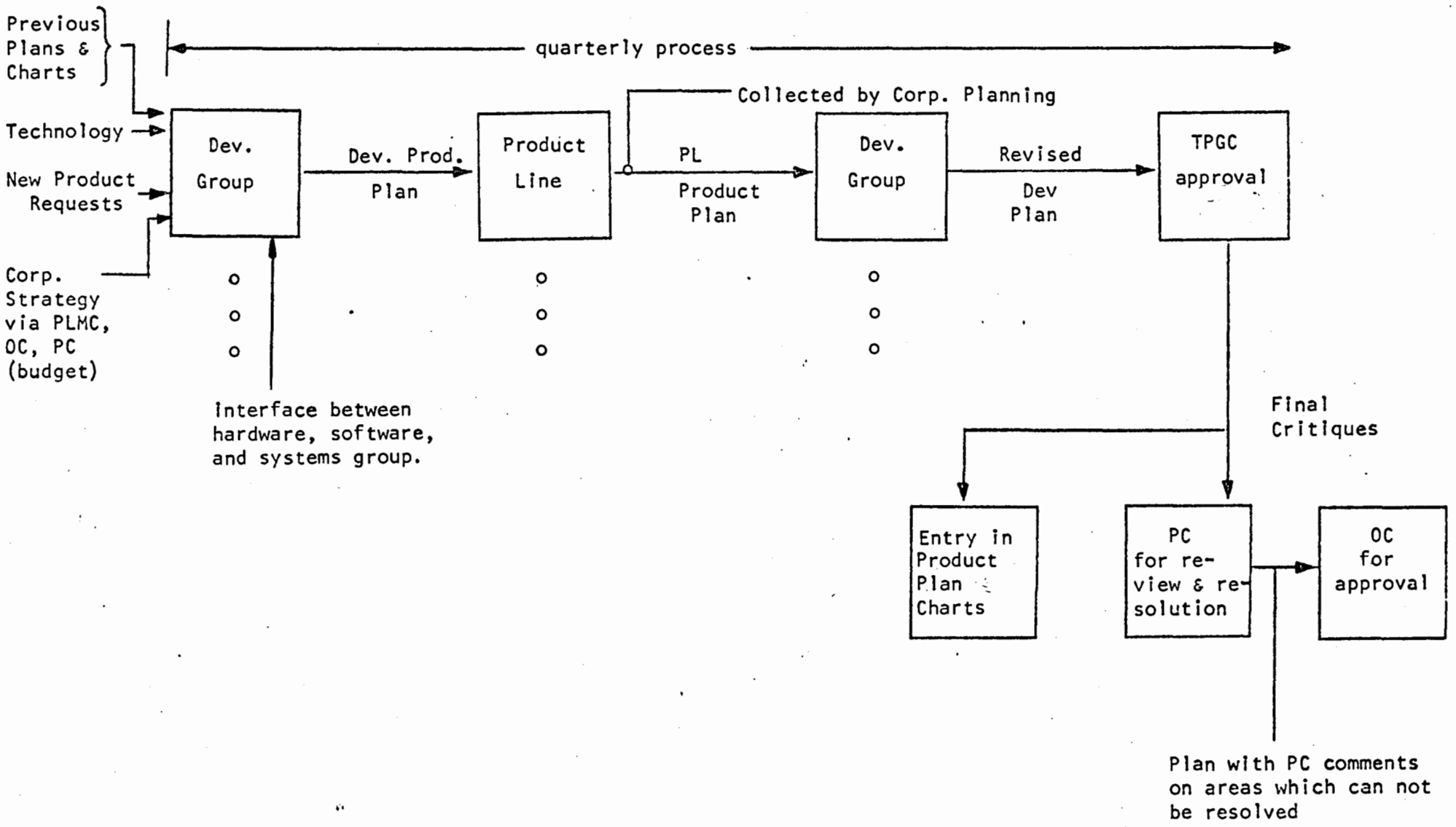
GB
5/74

FIGURE 1

DEVELOPMENT PROCESS
(Function of Time)

PRODUCT PHASE	ACTIVITIES (AND GATE TO NEXT PHASE)	BUSINESS PLAN PHASES
Preconcept	Request to study by PC, PLM, Dev. Mgr., etc.	
	--Development Manager approves--	
Study (1/4-1/2 year)	PRODUCT MANAGER APPOINTMENT	
	--TPGC approves--	
Proposal (1/4-1/2 year)		Original Business Plan Development with sales projection.
	--TPGC recommends; PLMC reviews; PC approves--	
Design and Tool (1-2 years)	Design Reviews by Eng. Committee Mfg./Eng. Committee reviews Mfg. Plan	Manufacturing part Support part (training & service) Sales part
	--TPGC recommends; PC revies; PLMC approves--	
Produce, Sell Support (2-3 years)	--TPGC recommends; PC approves--	--Rejuvenation plan (redesign)
	--TPGC recommdns; PLMC approves--	
Rejuvenate (1-2 year)		Traditionalize plan.
	--TPGC recommends; PLMC approves--	
Traditionalize (? years)		
	--TPL Manager recommends; PLMC approves--	
Death (4 1/2 - 8 yrs)		

FIGURE 2 TECHNOLOGY/PRODUCT PLANNING AND PRODUCT BUDGETARY PROCESS



ENGINEERING FORECAST FOR RS1011 FH DISK PREPARED ON 24-APR-74

Project No: 10-000 Proposal Date: 01-Jun-73 Approved: Products Committee 01-Oct-73

Product Manager: John Discus Project Engineer: Hy Density

Description: 10 megaword FH disk, 1ms avg access, 1us xfer rate

Goals: Improve performance of VIROS, RSX, RSTS Operating Systems

Requested by: Disk Steering Group; Software Engineering

HISTORY:	START DESIGN	OPERATE PROTO	LIMITED RELEASE	PUBLIC ANNOUNCE	FIRST CUST. SHIP	PRICE ($/UNIT)	MFG. COST ($/UNIT)	COMMENTS
01-Jun-73	Jul 73	Jul 74	Dec 74	Jan 75	Mar 75	$22,500	$1,500	Original Plan
01-Oct-73	Jul 73	Jul 74	Dec 74	Jan 75	Mar 75	$22,500	$3,000*	2ms avg access
01-Apr-74	Jul 73	Oct 74*	Mar 75*	Apr 75*	May 75*	$22,500	$5,000*	New price, sched

PRODUCT LINE	FORECAST DATE	FY74 Q4	FY75 Q1	FY75 Q2	FY75 Q3	FY75 Q4	FY76 Q1	FY76 Q2	FY76 Q3	FY76 Q4	FY77 Q1	FY77 Q2	FY77 Q3	FY77 Q4	FY78 Q1	FY78 Q2	FY78 Q3	FY78 Q4	FORECASTER
DECsys-10	01-Oct-73				5	20	25	30	30	35	40	40	45	45	45	45	50	50	J. Leng
	01-Apr-74				0	25	25	30	30	35	40	40	45	45	45	45	50	50	J. Leng
LDP-11/45	01-Oct-73				2	4	6	6	7	7	6	7	8	9	7	7	6	10	L. Data
	01-Apr-74				0	10	3	3	8	1	9	1	1	2	4	1	1	8	Anna Log
IND-11	01-Oct-73						2	2	2	4	3	3	3	5	4	4	4	6	R.T. Exec
	01-Apr-74							2	2	4	3	3	3	5	4	4	4	6	R.T. Exec
TOTAL	01-Oct-73				7	24	33	38	39	46	49	50	56	59	56	56	60	66	TOTAL
	01-Apr-74				0	35	28	35	40	40	52	44	49	52	53	50	55	64	TOTAL

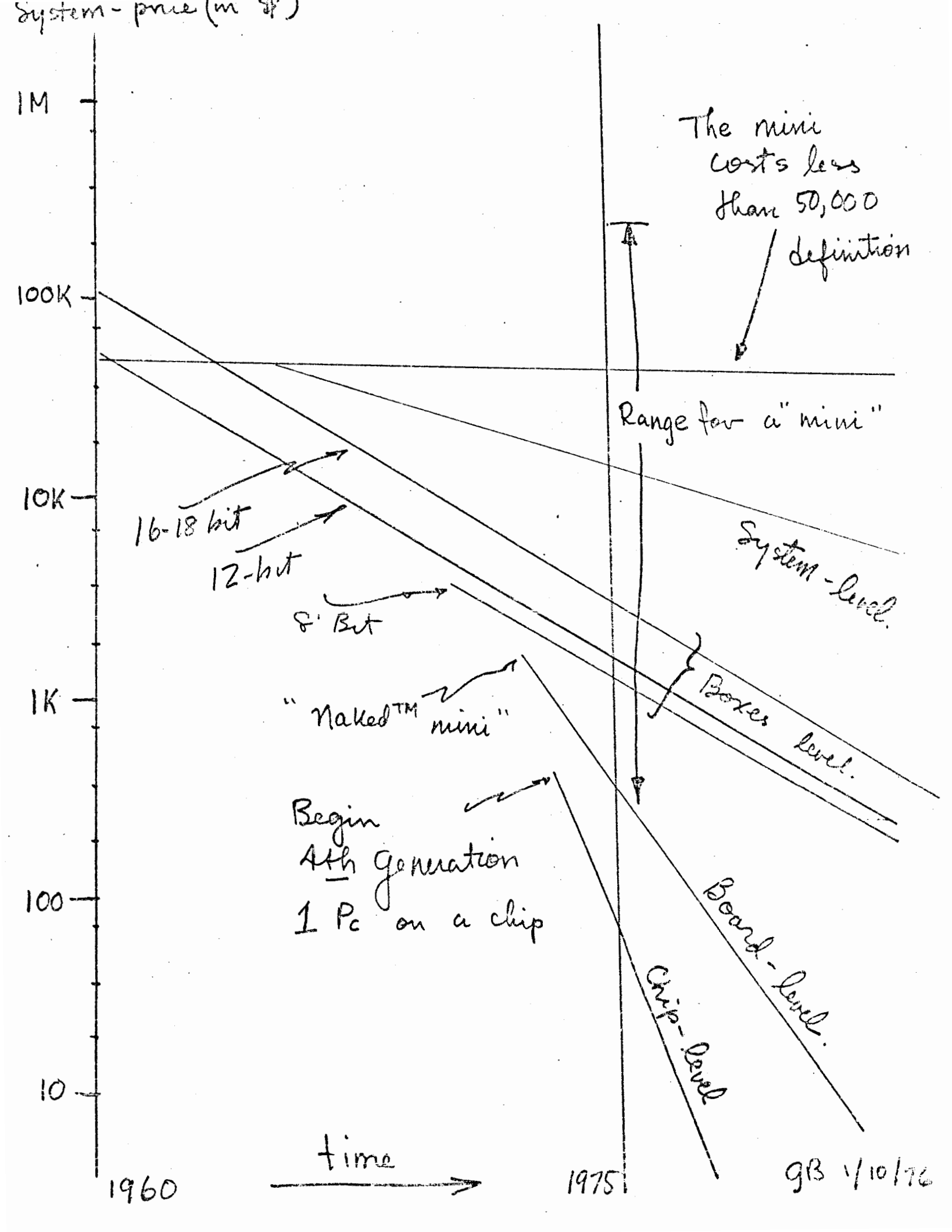
FIGURE 3 SAMPLE FORMAT FOR PRODUCT PLAN CHARTS

/ale

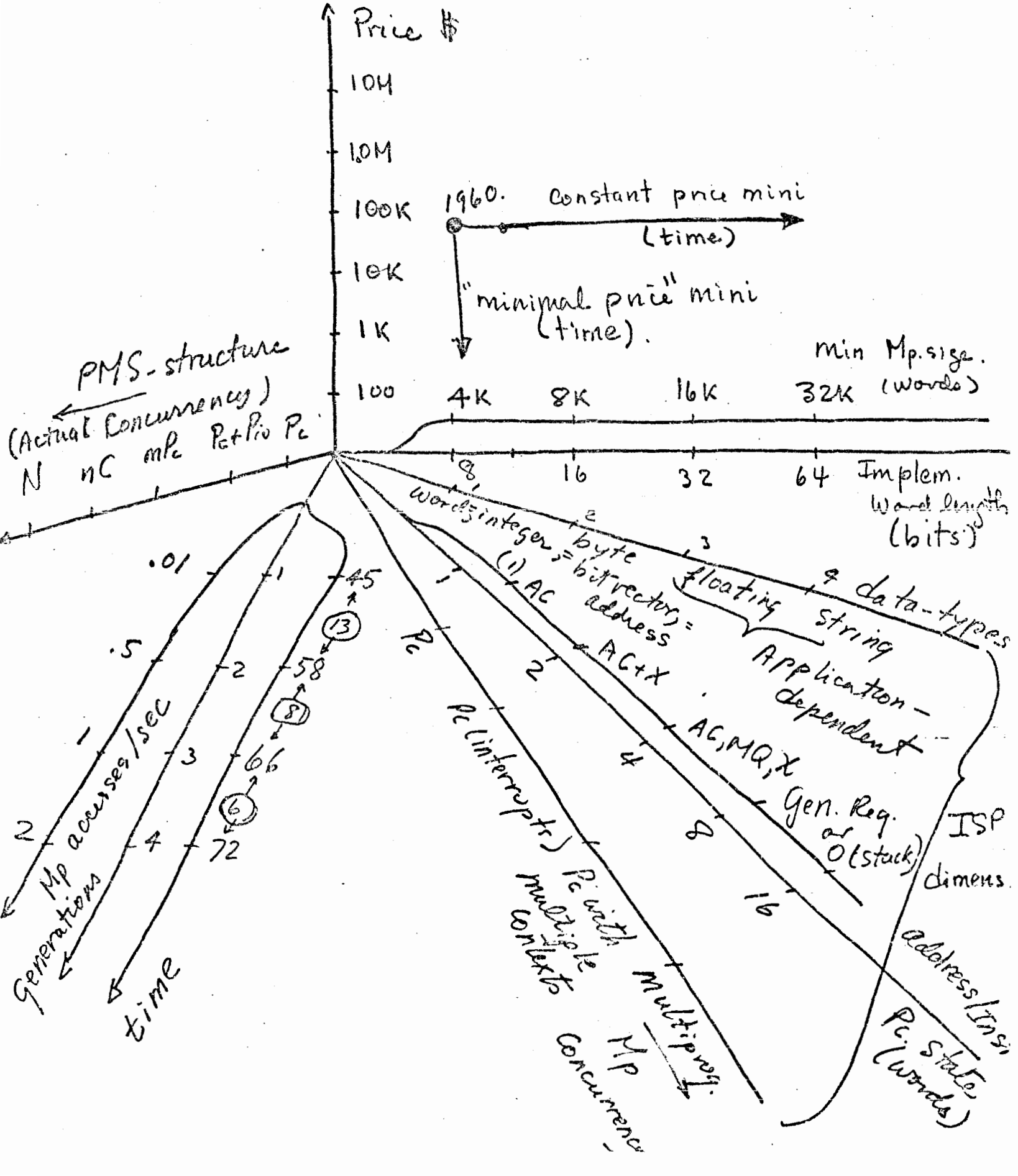
FIGURE 1

DEVELOPMENT PROCESS
(Function of Time)

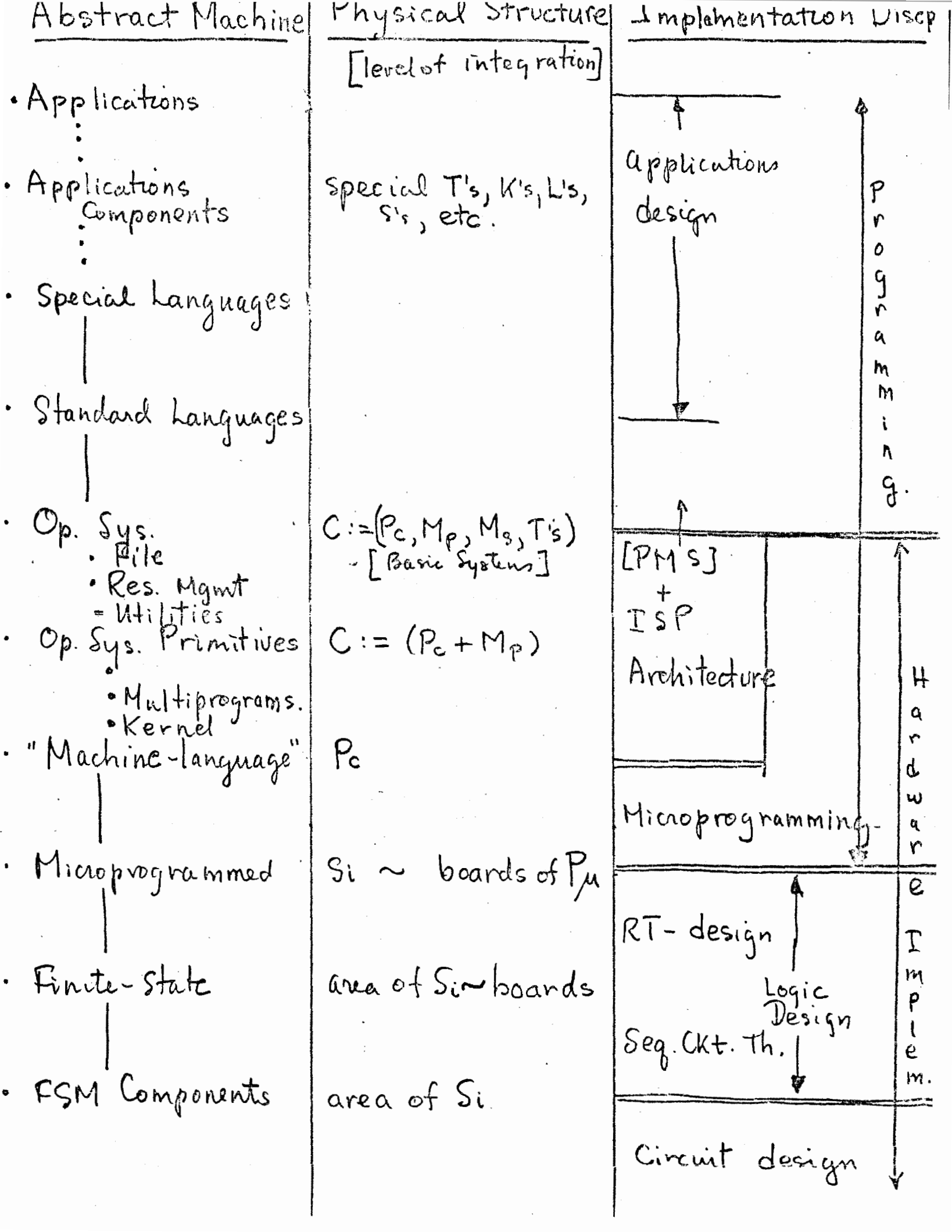
PRODUCT PHASE	ACTIVITIES (AND GATE TO NEXT PHASE)	BUSINESS PLAN PHASES
Preconcept	Request to study by PC, PLM, Dev. Mgr., etc.	
	--Development Manager approves--	
Study (1/4-1/2 year)	PRODUCT MANAGER APPOINTMENT	
	--TPGC approves--	
Proposal (1/4-1/2 year)		Original Business Plan Development with sales projection.
	--TPGC recommends; PLMC reviews; PC approves--	
Design and Tool (1-2 years)	Design Reviews by Eng. Committee Mfg./Eng. Committee reviews Mfg. Plan	Manufacturing part Support part (training & service) Sales part
	--TPGC recommends; PC revies; PLMC approves--	
Produce, Sell Support (2-3 years)	--TPGC recommends; PC approves--	--Rejuvenation plan (redesign)
	--TPGC recommdns; PLMC approves--	
Rejuvenate (1-2 year)		Traditionalize plan.
	--TPGC recommends; PLMC approves--	
Traditionalize (? years)		
	--TPL Manager recommends; PLMC approves--	
Death (4 1/2 - 8 yrs)		

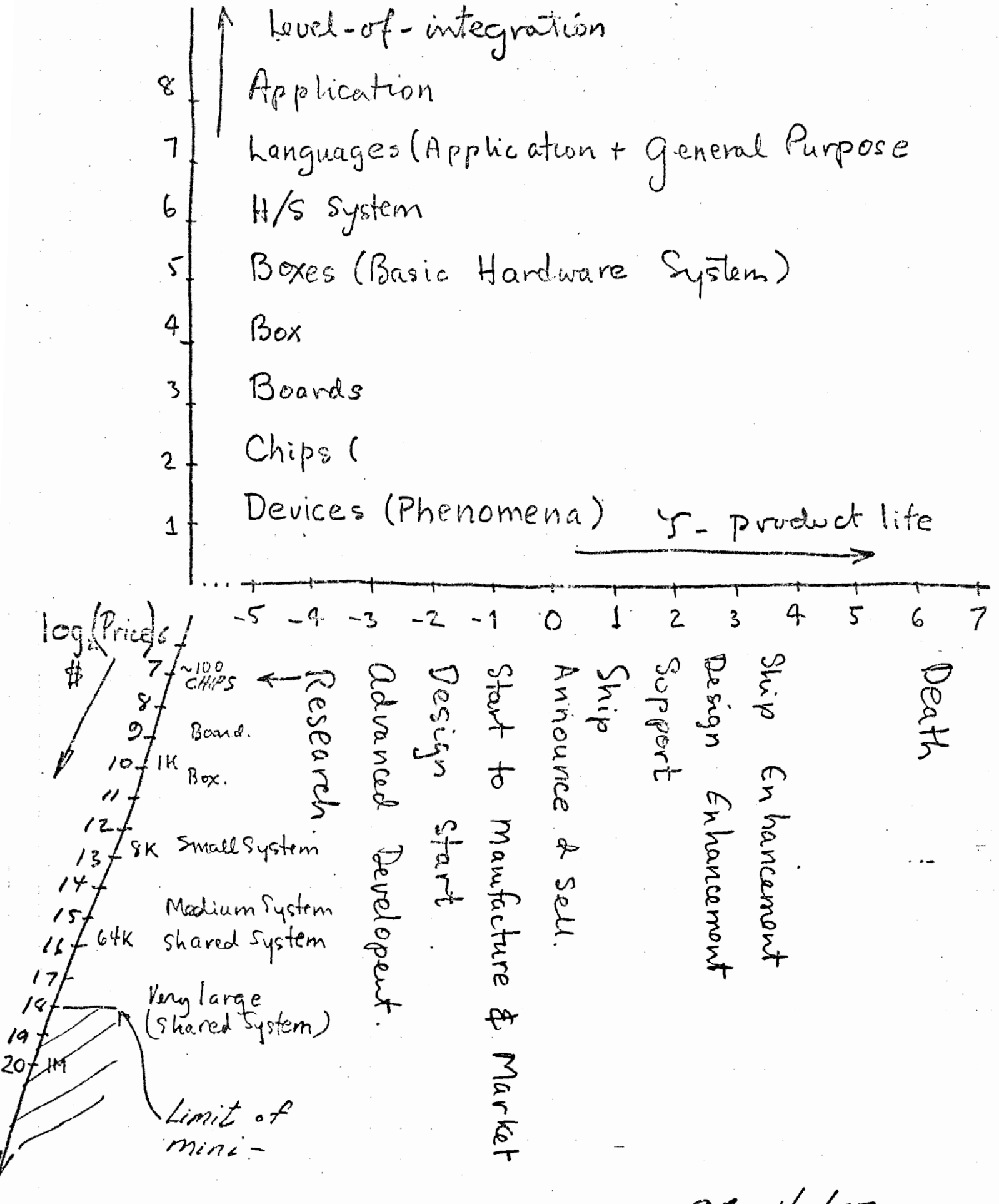

System - price (in $)
1M
100K
10K
1K
100
10
The mini costs less than 50,000 definition
Range for a "mini"
16-18 bit
12-bit
8 Bit
"Naked™ mini"
Begin 4th Generation 1 Pc on a chip
System - level
Boxes level
Board - level
Chip - level
time
1960
1975
GB 1/10/76

Basic hardware-oriented C-space dimensions (emphasis on mini)

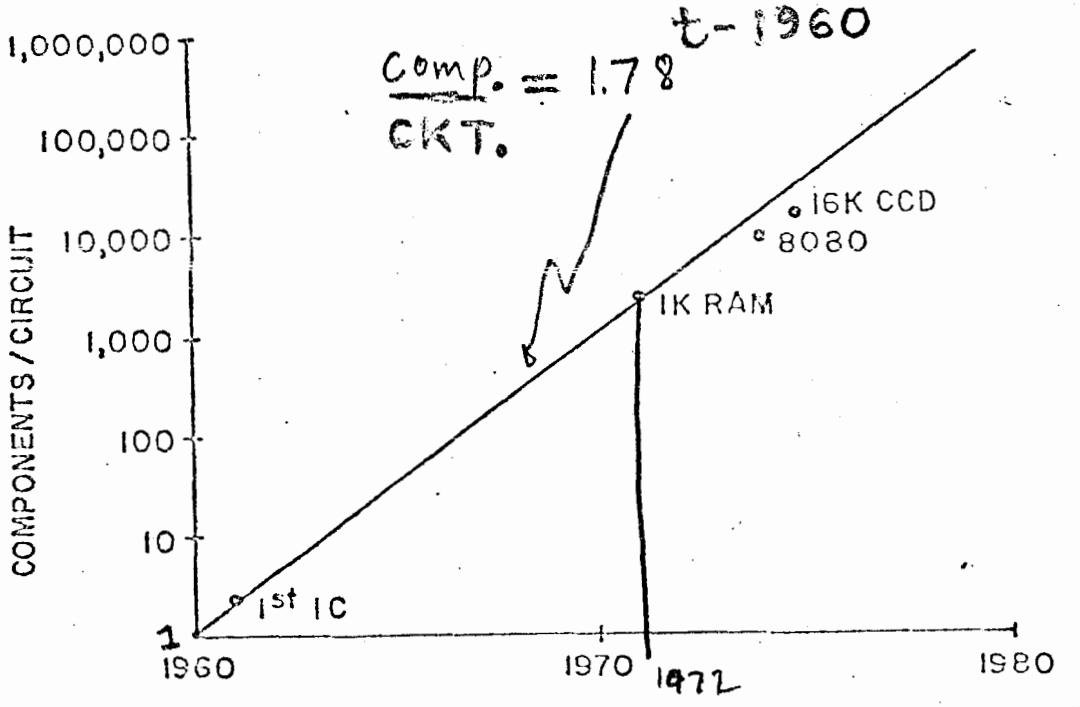


Mini - level of Integration.	Very small - (Micro)
8	8
7 Language.	7
6 H/S System	6 H/s system.
5 Σ Boxes	5 - (non-existent)
4 - Boxes := Σ Brds	4 - Box.
3 - Board	3 - Board = $P_c + M_p$
2 Chip	2 - Chip


Abstract Machine
Physical Structure
[level of integration]
Implementation Disc
• Applications
• Applications Components
• Special Languages
• Standard Languages
• Op. Sys.
• File
• Res. Mgmt
• Utilities
• Op. Sys. Primitives
• Multiprograms.
• Kernel
• "Machine-language"
• Microprogrammed
• Finite-State
• FSM Components
special T's, K's, L's, S's, etc.
C := (Pc, Mp, Ms, T's)
- [Basic Systems]
C := (Pc + Mp)
Pc
Si ~ boards of Pμ
area of Si ~ boards
area of Si
Applications design
Programming.
[PMS] + ISP Architecture
Microprogramming
RT - design
Logic Design
Seq. Ckt. Th.
Circuit design
Hardware Implem.


Level-of-integration
8 Application
7 Languages (Application + General Purpose
6 H/S System
5 Boxes (Basic Hardware System)
4 Box
3 Boards
2 Chips (
1 Devices (Phenomena)
Y- product life
-5 -4 -3 -2 -1 0 1 2 3 4 5 6 7
log2(Price $)
7 ~100 CHIPS
8
9 Board.
10 1K Box.
11
12
13 8K Small System
14
15 Medium System
16 64K Shared System
17
18 Very large (Shared System)
19
20 1M
Limit of mini-
Research.
Advanced Development.
Design start
Start to manufacture & Market
Announce & sell.
Ship
Support
Design Enhancement
Ship Enhancement
Death

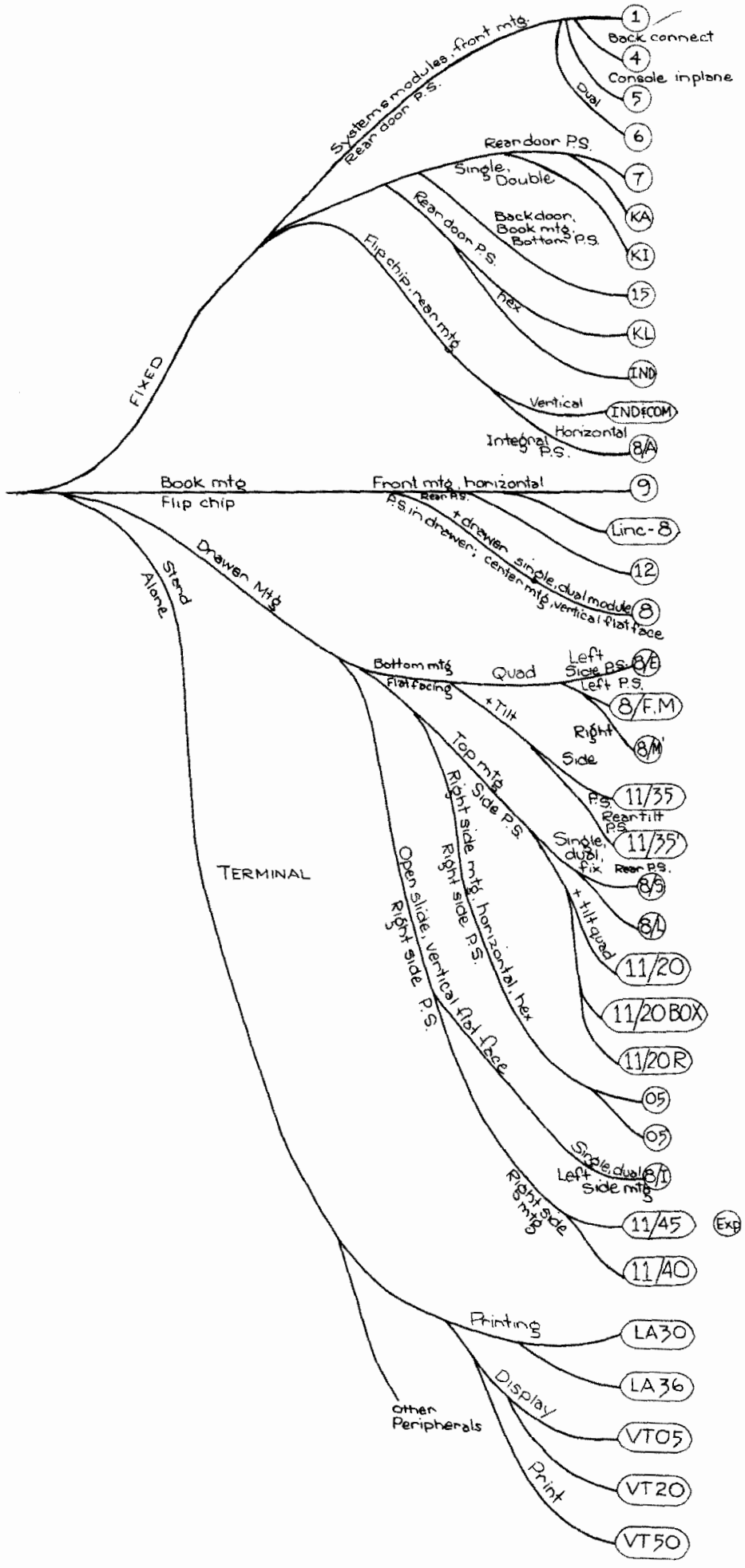
gis 1/10/75



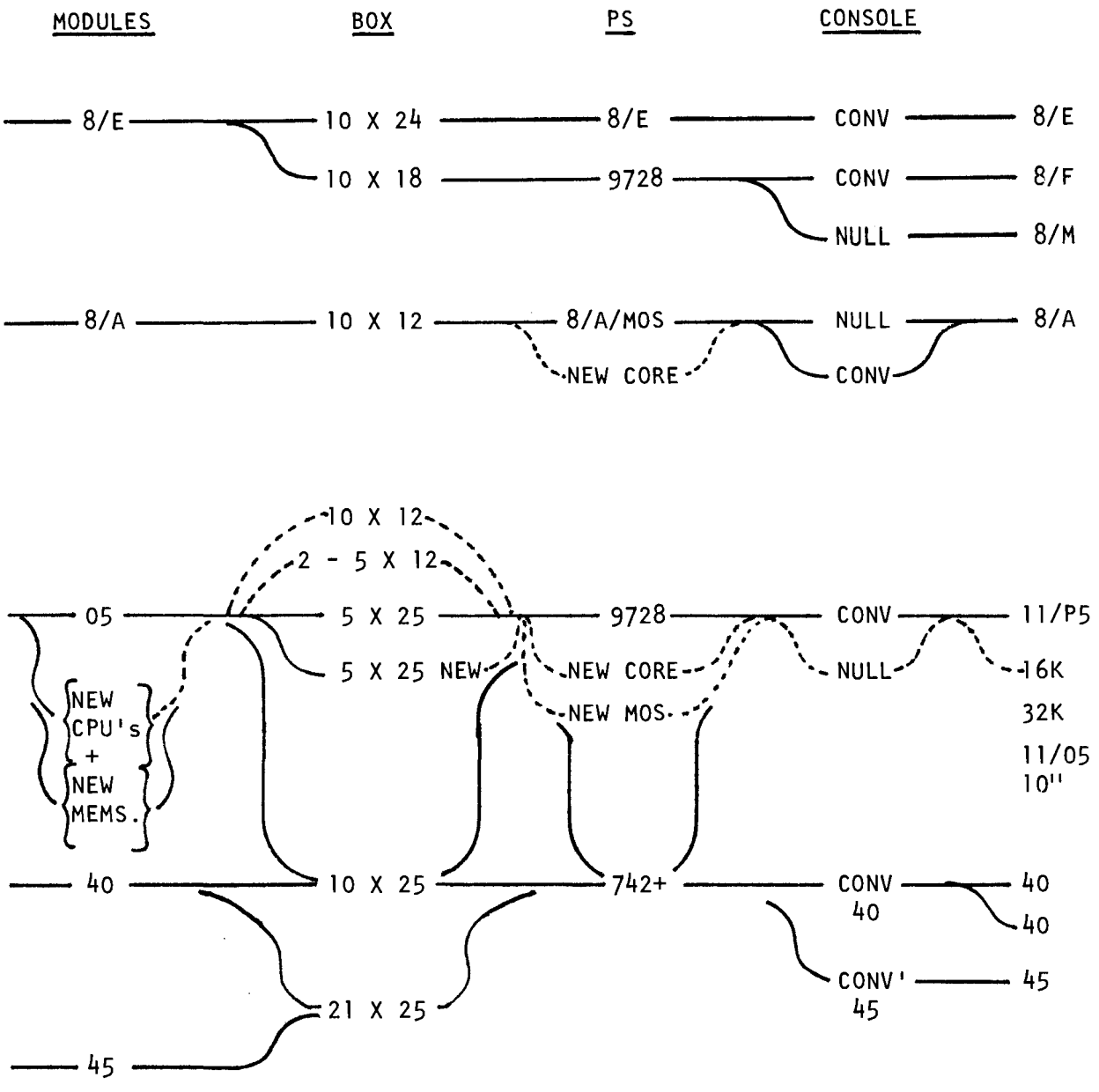
COMPLEXITY OF INTEGRATED CIRCUITS CONTINUES TO INCREASE, NEARLY DOUBLE EVERY YEAR.

(Bell) # bits/die = 2^{t-1962}.

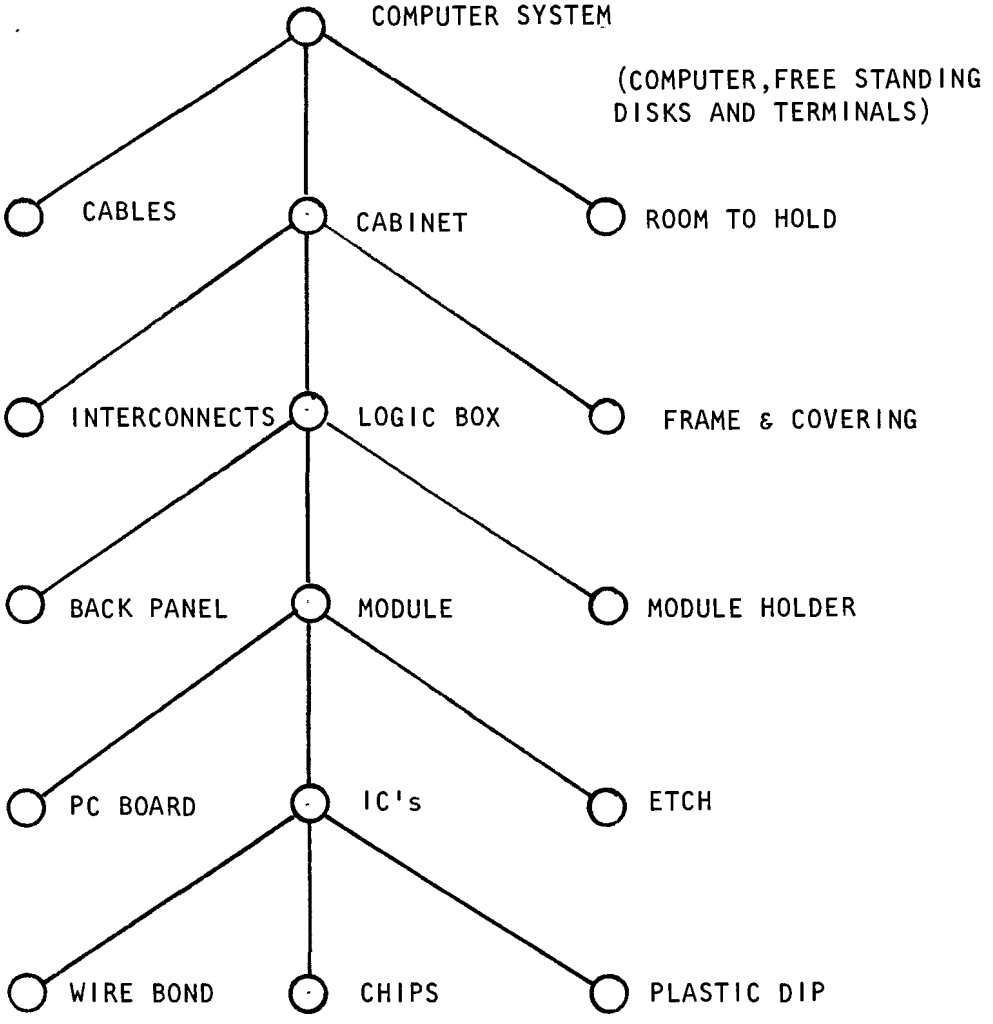
Noyce 10/75



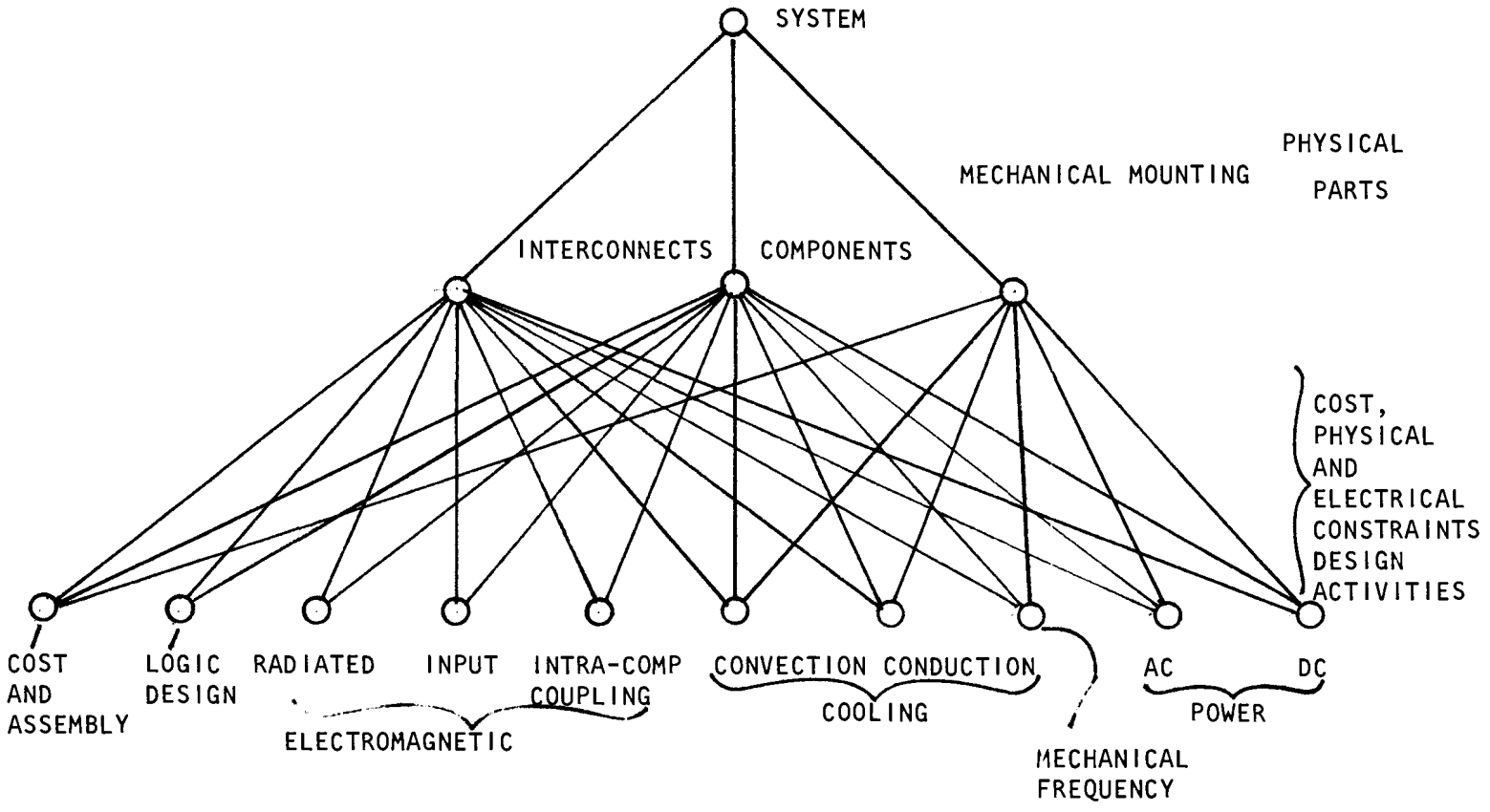
DEC COMPUTER PACKAGING GENEALOGY



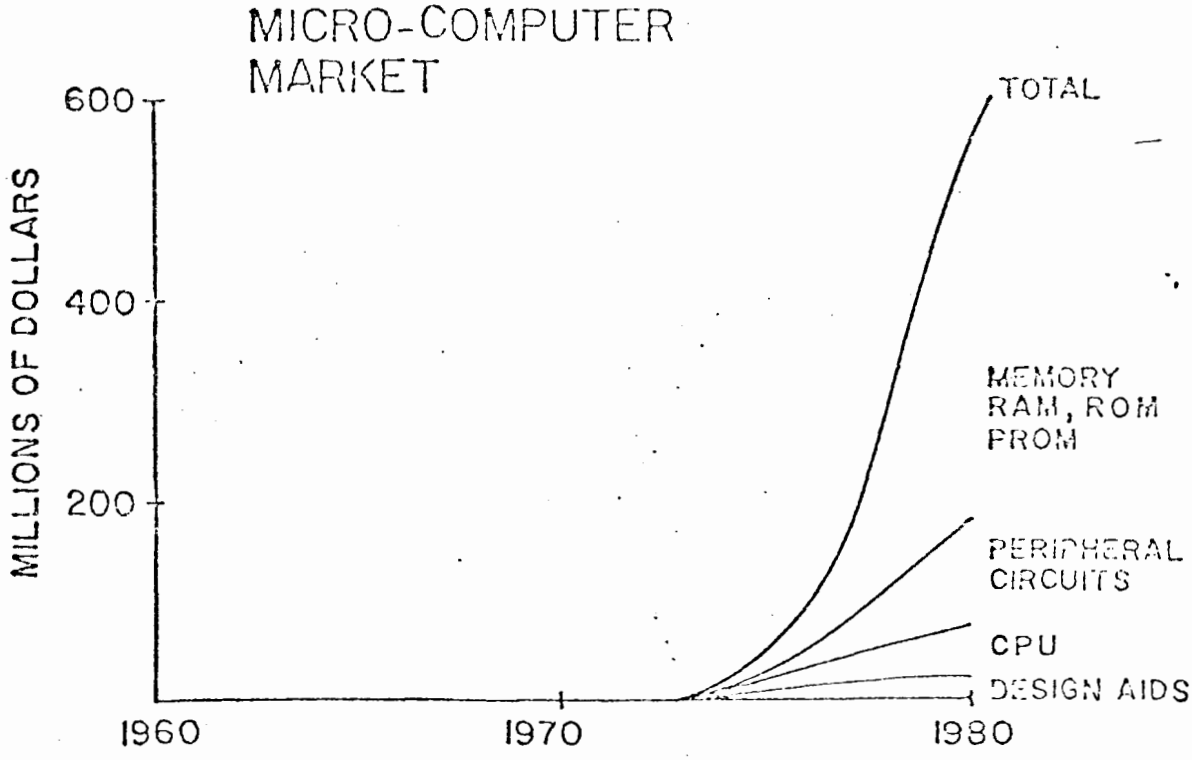
PROCESSOR, PACKAGE, PS, CONSOLES FOR 8 AND 11's



COMPUTER SYSTEM HIERARCHY OF PHYSICAL COMPONENTS, THEIR INTERCONNECTION AND MOUNTING

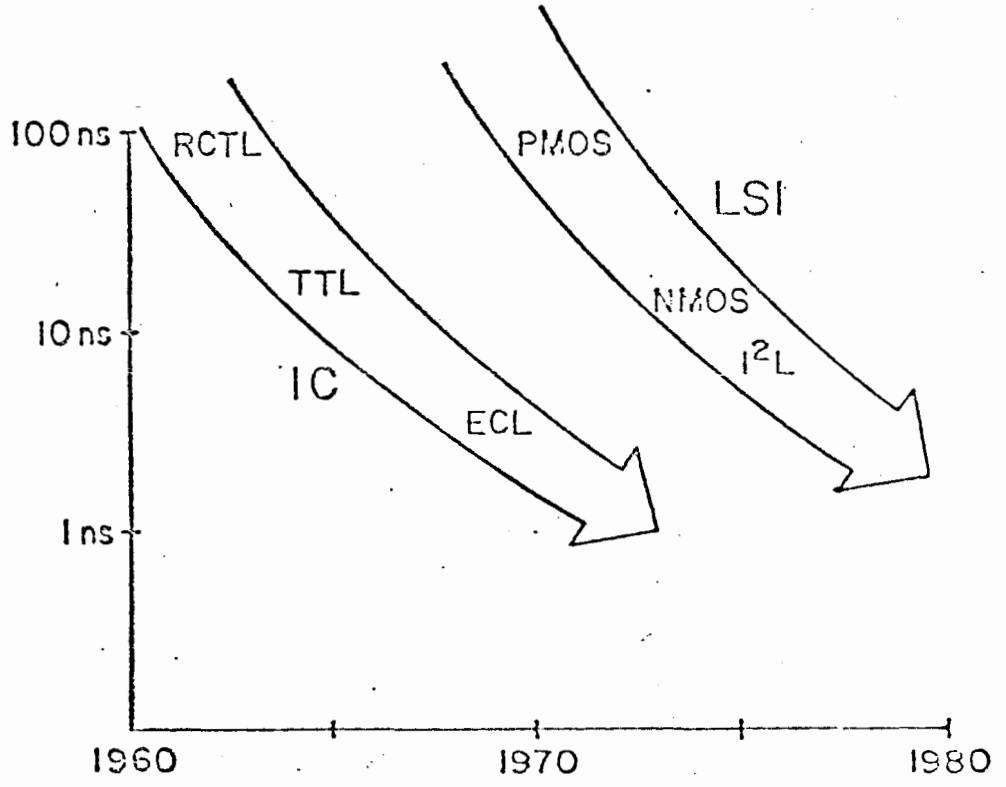


RELATIONSHIP OF PHYSICAL PARTS TO OTHER DESIGN ACTIVITIES



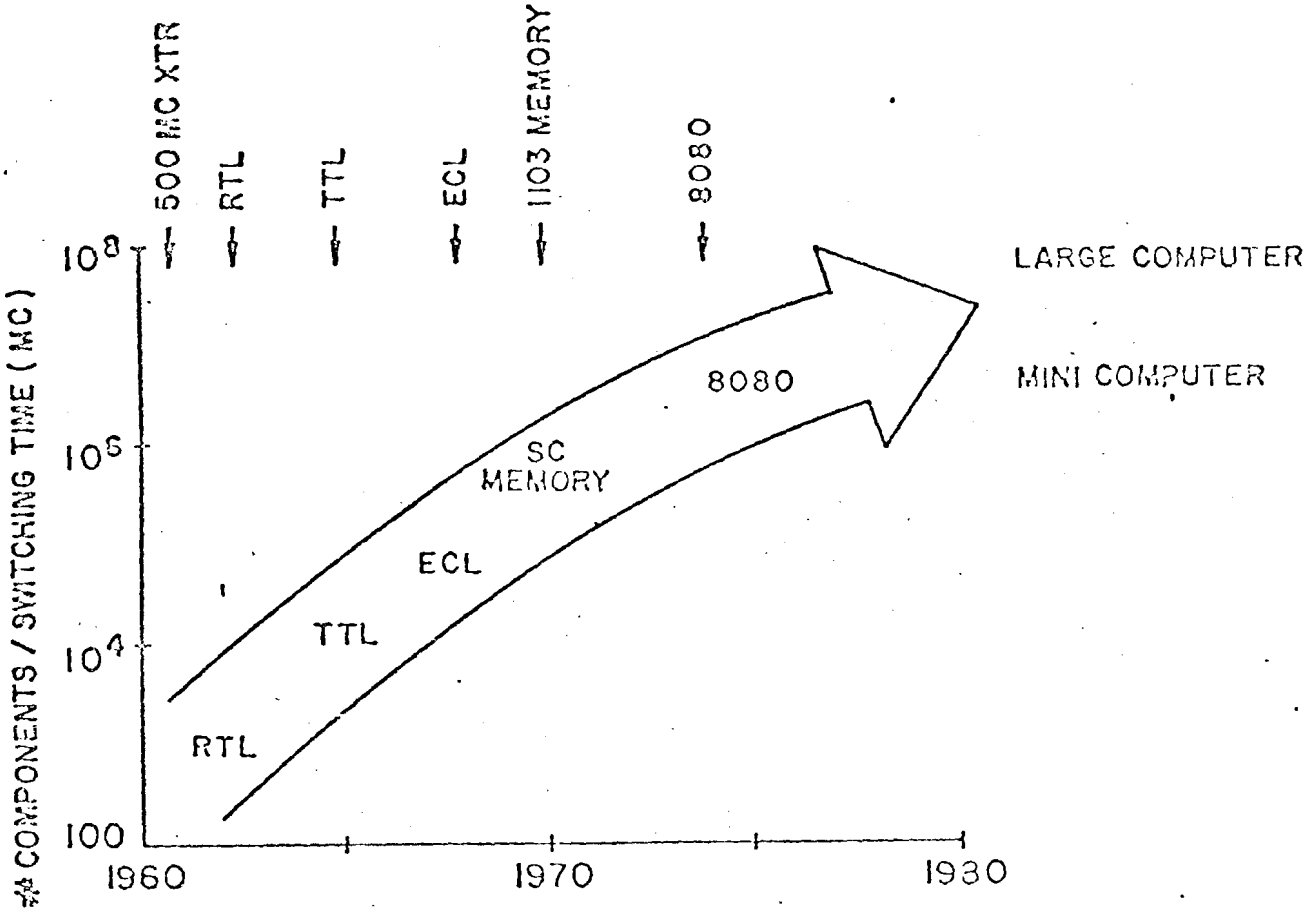
THE μCOMP MARKET IS JUST BEGINNING TO DEVELOP, IT INCLUDES MUCH MORE THAN THE CPU.

Noyce 10/75



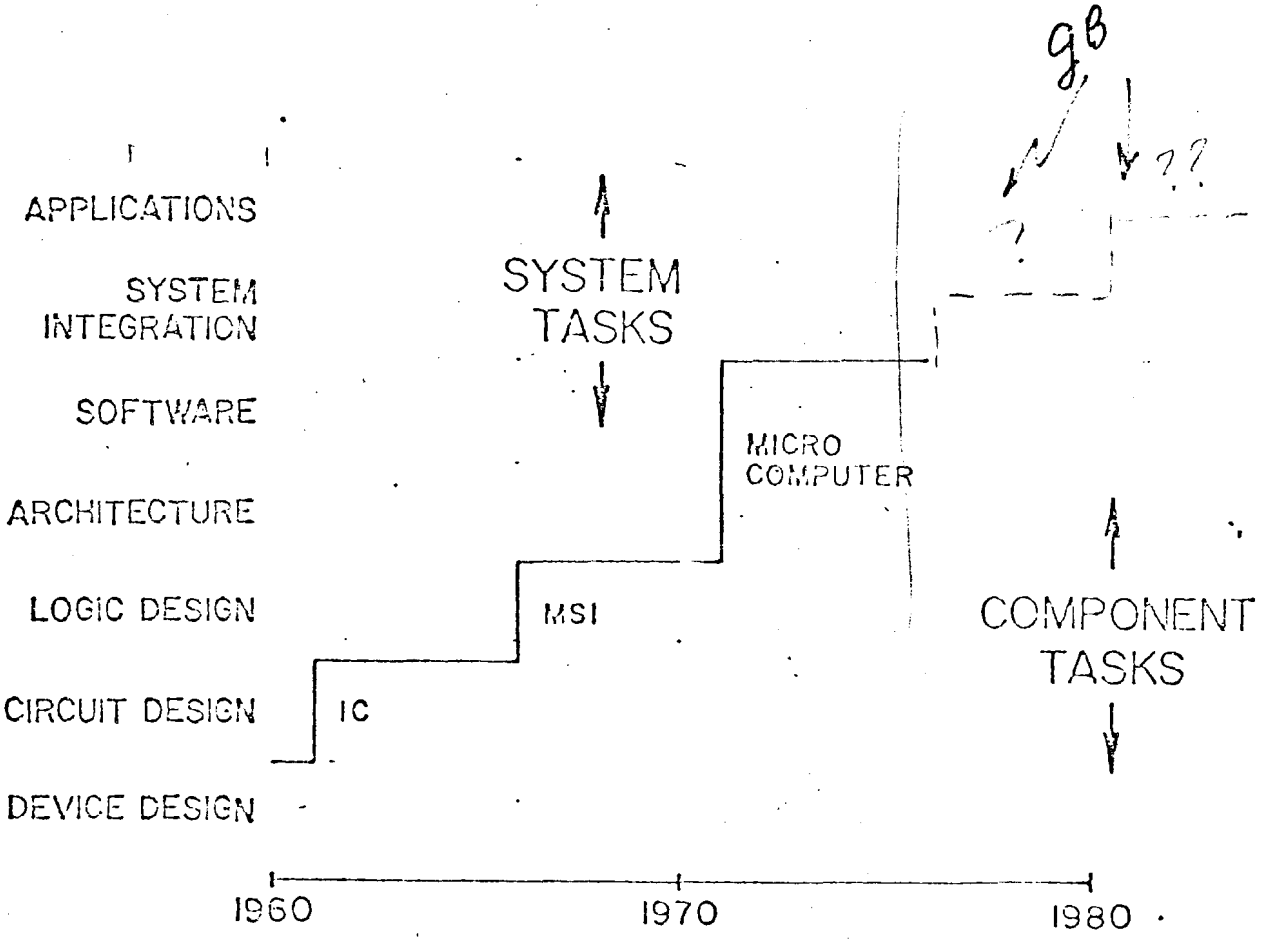
AFTER INTRODUCTION, THE PERFORMANCE OF IC'S IMPROVED RAPIDLY. THE SAME IS TRUE OF LSI.

Noyce 10/75



BY 1980 THE SPEED COMPLEXITY OF THE MICRO-COMPUTER WILL BE COMPARABLE TO THAT OF TODAY'S LARGE CPU'S.

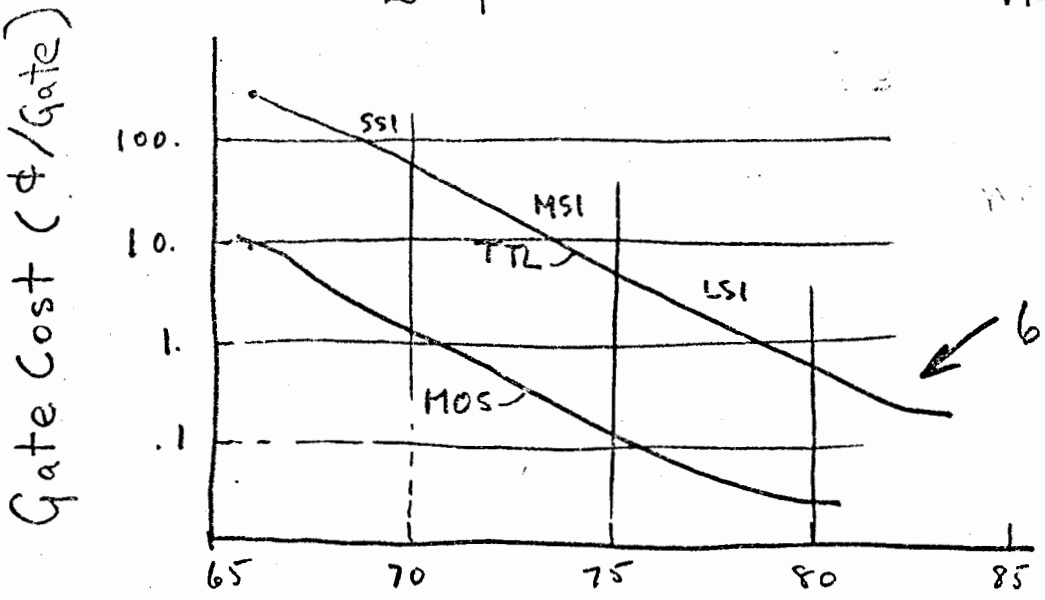
Noyce 10/75



EACH CHANGE OF LEVEL OF INTEGRATION HAS FORCED THE COMPONENT SUPPLIER TO ASSUME ADDITIONAL RESPONSIBILITIES.

Noyce 10/75

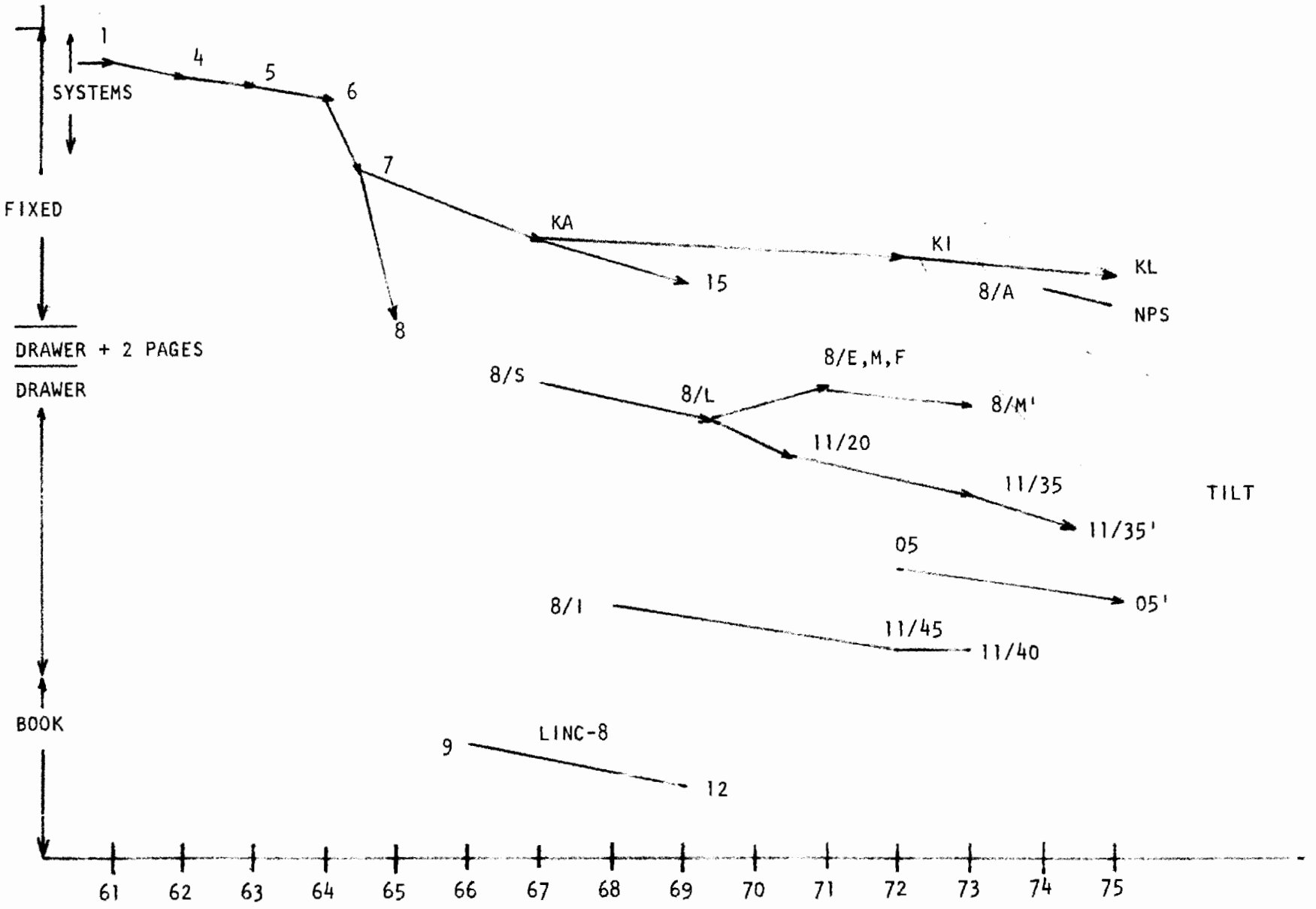
LOGIC COST VS. TIME



note
60% improvement/year

Nussbaum, BTL, 1975

(Head of Switchy Ckts. Dept.)



TIME LINE OF COMPUTER PACKAGES

TABLE 2 - CHARACTERISTICS GENERIC TO MINICOMPUTERS

IMPLIMENTATIONS TRACK TECHNOLOGY CLOSELY.

INTERNAL CENTRAL PROCESSOR

BASE ADDRESSING; ADEQUATE INTERRUPT RESPONSE TIME; POWER ON-OFF INTERRUPT

STRUCTURAL

VERY LITTLE HARD COPY I/O, SECONDARY MEMORY; OBVIOUS STRUCTURE (ALLOWING EASY INTERFACING); DIRECT MEMORY ACCESS--ENCOURAGES PMS ARCHITECTURE + DESIGN.

USES (DEDICATED)

CONTROL (E.G., PLANT, INSTRUMENT); COMMUNICATIONS (E.G., MESSAGE SWITCH); LARGER COMPUTER (E.G., TERMINALS, FILES, HARD COPY)

SOFTWARE

SMALL GENERAL PURPOSE MONITOR; LANGUAGES: PRIMITIVE ASSEMBLER, BASIC, FORTRAN; SPECIALIZED DEDICATED USE PACKAGES (E.G., TYPESETTING, INSTRUMENT TESTING, PROCESS)

APPROACHABLE--FIT COMPUTER TO PROBLEM VS...

ANCESTRY

- MINICOMPUTER ANCESTRY BEGAN WITH EDSAC.
- AEROSPACE COMPUTERS CLAIMED ANTECEDANTS.
- MINICOMPUTERS (FOR MINIMAL COMPUTERS) ARE A STATE OF MIND; THE CURRENT LOGIC TECHNOLOGY, THE CHARACTERISTICS FOUND IN LARGER COMPUTERS, COMBINED INTO A PACKAGE WHICH HAS THE COST.
- ALMOST THE SOLE GOAL IS TO MAKE THE COST LOW.
- THE HARDWARE-SOFTWARE TRADEOFFS FOR MINICOMPUTER DESIGN FAVORED SOFTWARE.

GB
1/19/76

G. Bell, Minicomputer Architecture and Design
IEEE Conference, Spring 1971

TABLE 1 - CHARACTERISTICS DERIVED FROM LARGER COMPUTERS

INTERNAL CENTRAL PROCESSOR

INDIRECT ADDRESSING; INTERRUPTS; INDEX REGISTERS; MULTIPLE, GENERAL PURPOSE REGISTERS; BASE AND/OR PAGE ADDRESSING; FLOATING POINT DATA-TYPES*; PAGING, SEGMENTATION, AND INTERPROCESS COMMUNICATION*

STRUCTURAL

SPECIALIZED PROCESSORS; MULTIPROCESSORS*

IMPLEMENTATION

MICROPROGRAMMING*; LOOKAHEAD*; CACHE*;

SOFTWARE

COMPILERS: FORTRAN; TIME-SHARING MONITORS*

*NOT EXTENSIVELY USED, BUT USE LIKELY TO INCREASE.

FM: BELL, CADY, MCFARLAND, DELAGI, O'LOUGHLIN, NOONAN, WULF

AFIPS SJCC 1970, P657, "A NEW ARCHITECTURE FOR MINI-COMPUTERS--THE DEC PDP-11"

NAME	MP.SIZE	Pc+BASIC MP PRICE	WORD LENGTH (BITS)	Pc.STATE (WORDS)	DATA-TYPES
MICRO	8K	~5K	8-12	2	(1~2) WORD = BYTE - INTEGER = BOOLEANS
MINI	32K	(5-10)K	12-16	2-4	(3) + ADDRESSES, VECTORS (INDEX)
MIDI	65-128K	(10-20)K	16-24	4-16	+ DOUBLE INTEGERS + FLOATING POINT
.					
.					
.					
MAXI					

ALL ARE: 5-10 MHZ CLOCK; TTL; MSI
T.CYCLE .7~2 μSEC.
FIXED TO A SPECIFIC, SINGLE TASK.

GB
1/19/76

MINICOMPUTER SOFTWARE

FROM A SALES PITCH BY JR, CG BELL FOR IFIPS BOOK (CONFERENCE)

ON MINICOMPUTER SOFTWARE

"READ THIS BOOK AND FIND OUT WHY SOME OF THE MOST EXPERIENCED, KNOWLEDGEABLE PEOPLE FEEL THAT:

- A MINICOMPUTER IS NOT JUST A SCALED DOWN LARGE COMPUTER.
- THE LIMITED SIZE OF MINICOMPUTERS CAN ACTUALLY BE AN ASSET.
- ONE OF THE KEY BARRIERS TO MINICOMPUTER USE IS PSYCHOLOGICAL.
- STANDARDIZED LANGUAGES ARE MORE IMPORTANT THAN BETTER LANGUAGES.
- PORTABILITY OF PROGRAMMERS IS AS VITAL AS PORTABILITY OF PROGRAMS.
- MINICOMPUTERS ARE FOR THOSE APPLICATIONS NOT FEASIBLE WITH MAXICOMPUTERS--COST, RESPONSE TIME, HUMAN INTERFACE, ULTRA-RELIABILITY.
- TO MINICOMPUTER USERS, OLD TECHNICAL PAPERS ARE MORE VALUABLE THAN NEWER ONES.
- MINICOMPUTER SOFTWARE IS SHAPED PRIMARILY BY APPLICATIONS, YET FORCES EVERY PROGRAMMER TO BE A SYSTEMS PROGRAMMER."

DIFFERENCES: DEDICATEDNESS (E.G. OPERATING SYSTEM)

SIZE CONSTRAINT (ALTHOUGH COST/BIT IS CHEAPER AND MP SIZE IS INCREASING)

ISSUES OF CONFERENCE: PROGRAMMING LANGUAGES (STRUCTURED-TYPE),

PRODUCTIVITY, PORTABILITY, USER

MICROPROGRAMMABILITY

GB
1/19/76

MINICOMPUTERS: A STATE OF MIND

IANN M. BARRON

"THE MINICOMPUTER IS AN ATTITUDE OF MIND. IT IS NOT USEFUL TO DEFINE IT IN TERMS OF PRICE OR CAPABILITY BECAUSE THESE CHANGE WITH THE TECHNOLOGY. THE DIFFERENCE...LIES IN MARKETING PHILOSOPHY. THE MINICOMPUTER COMPANY IS SELLING A MANUFACTURED PRODUCT WHEREAS THE CONVENTIONAL COMPUTER COMPANY IS SELLING A SERVICE, AND SERVICES COST MONEY.

H. COX

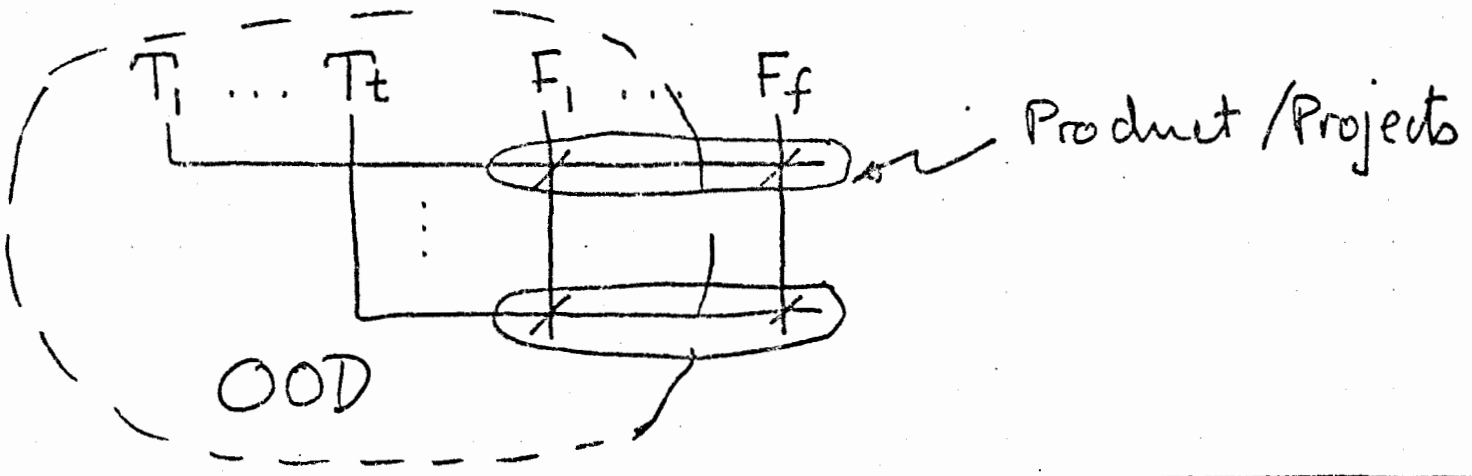
MINICOMPUTER: A GENERAL PURPOSE COMPUTER IN WHICH INPUT AND OUTPUT TRANSFERS ARE OF SINGLE WORDS (OR PART WORDS) FROM REGISTERS, EACH TRANSFER COMMANDED BY AN INSTRUCTION IN THE PROGRAM. THE OTHER MAIN CLASS OF COMPUTERS HAS NO COMMON NAME AND IS DISTINGUISHED BY INPUT AND OUTPUT TRANSFERS BEING OF BLOCKS OF WORDS (OR PART WORDS) THAT ARE CARRIED OUT AUTOMONOUSLY FROM STORE, THE PROGRAM SETTING UP BLOCKS AND INITIATING THE TRANSFER OF BLOCKS.

THE DIFFERENCE IS SIMILAR TO TUNGSTEN OR FLUORESCENT LAMPS AND ORDINARY LAMPS, VIZ: LOWER EFFICIENCY... OR HIGHER OVER-HEADS. FLUORESCENTS ARE UNDOUBTABLY MORE EFFICIENT FOR BUSINESS LIGHTING, BUT HAVE A MINIMAL SHARE OF THE CHRISTMAS TREE LIGHTS MARKET.

qb 1/19/76

How Are We Organized? [PEOPLE] gB May 9, 197

- Functionally by skills (eg. drafting) and by technology (eg. disk mem.) with Matrix mgmt. via Technology using Skills



How do we Measure Output?

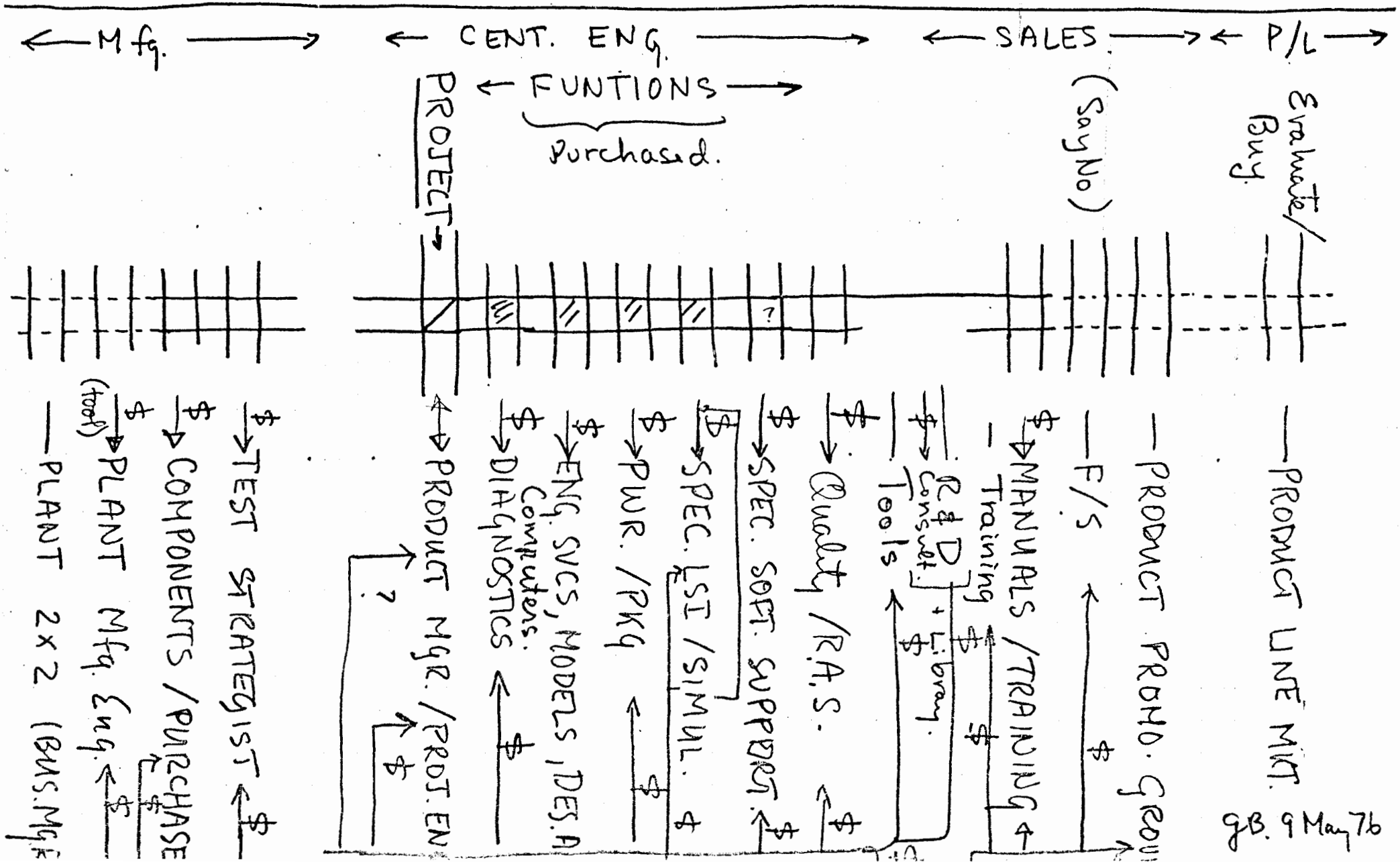
- Mostly by "success" of product ≈ NOR!
  - Schedule
  - $. develop and $. cost
  - Performance of Product (eg. reliability, function, ... ,
  - Rarely as / agreement.
  -
- Gut feel
  - Truly useful • Does it feel good? (Weak link)
  - Adds evaluation dimension
  - Doesn't lose Sales for Other Systems.

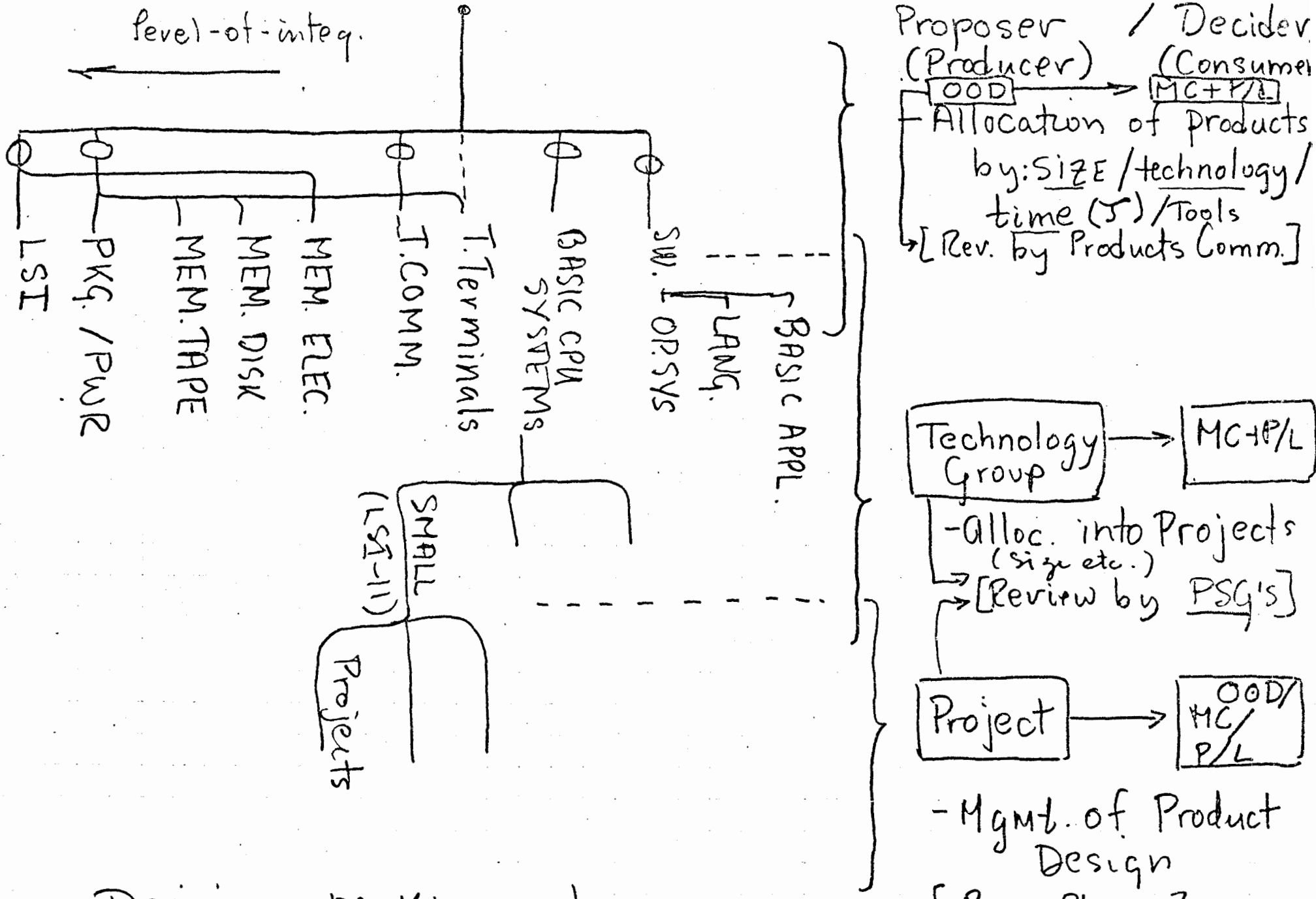
Project MATRIX

Projects are formed from Matrix of Functional / Product Skills.

(Matrixed person has: 2 bosses, lives with project, skill orientation)

and Many functions are outside Central Eng.



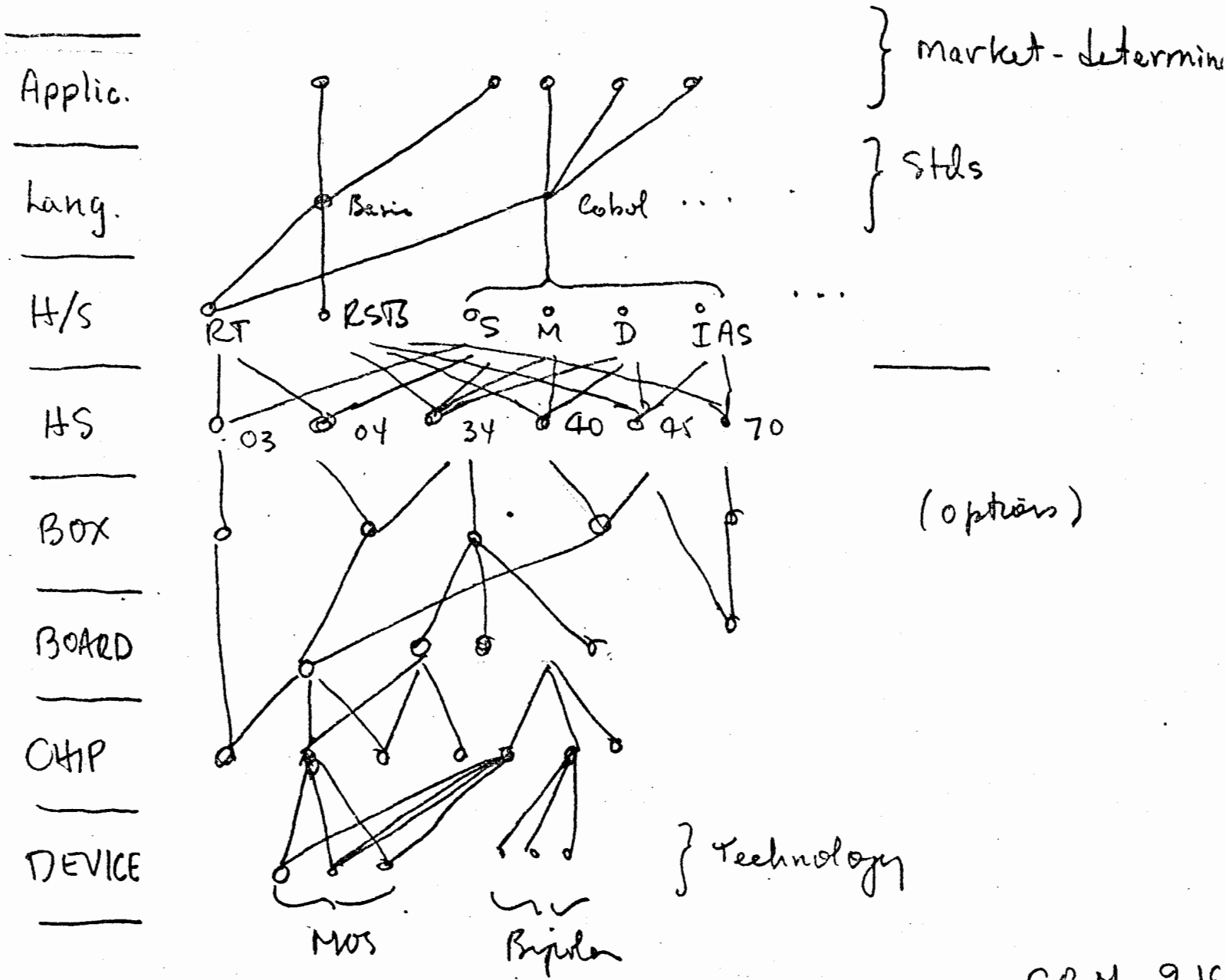


Decision-making at 3-levels of OOD (OOD-Technology Area-Project)

AR Mar 9 1971

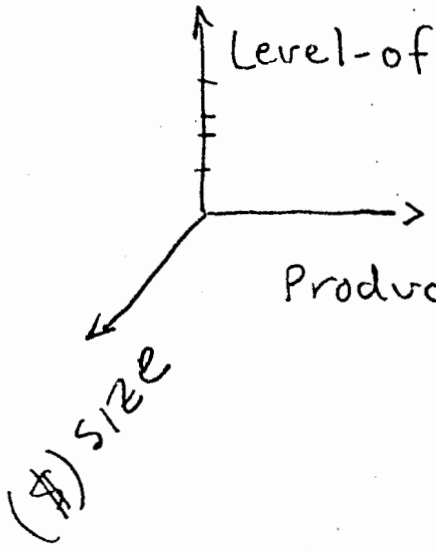
THE PRODUCT: Allocate Resources in size, life cycle (T), level-of-inte

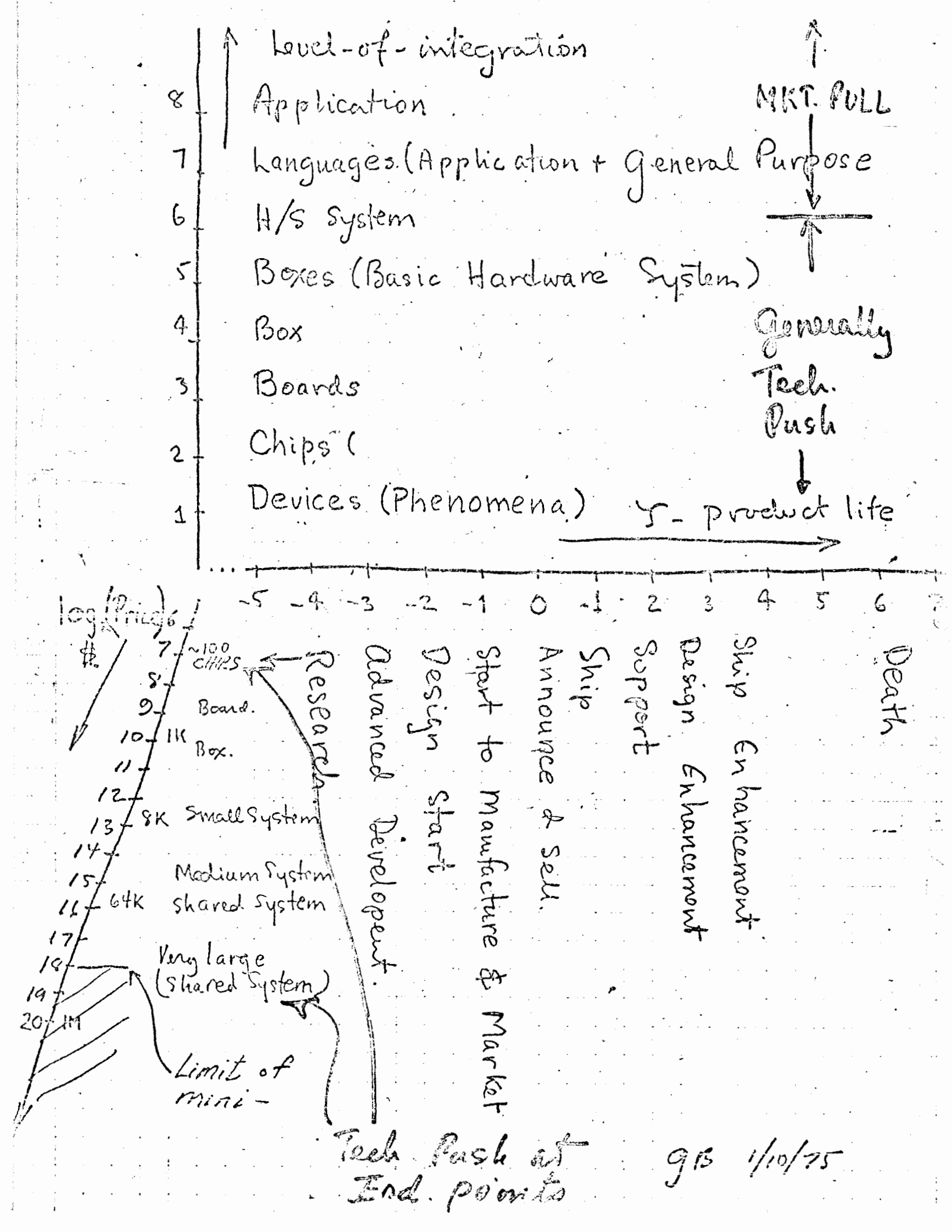
Computer System Development IS A Network (NOT JUST A Tree-structured HIERARCHY) OF 8 DISTINCT LEVELS. (IN ESSENCE, A PROJECT MAY DEPEND ON 1 OR MORE SUB PROJECTS AND A PROJECT MAY AFFECT SEVERAL SUCCESSOR PROJECT



GB Mar 9.19

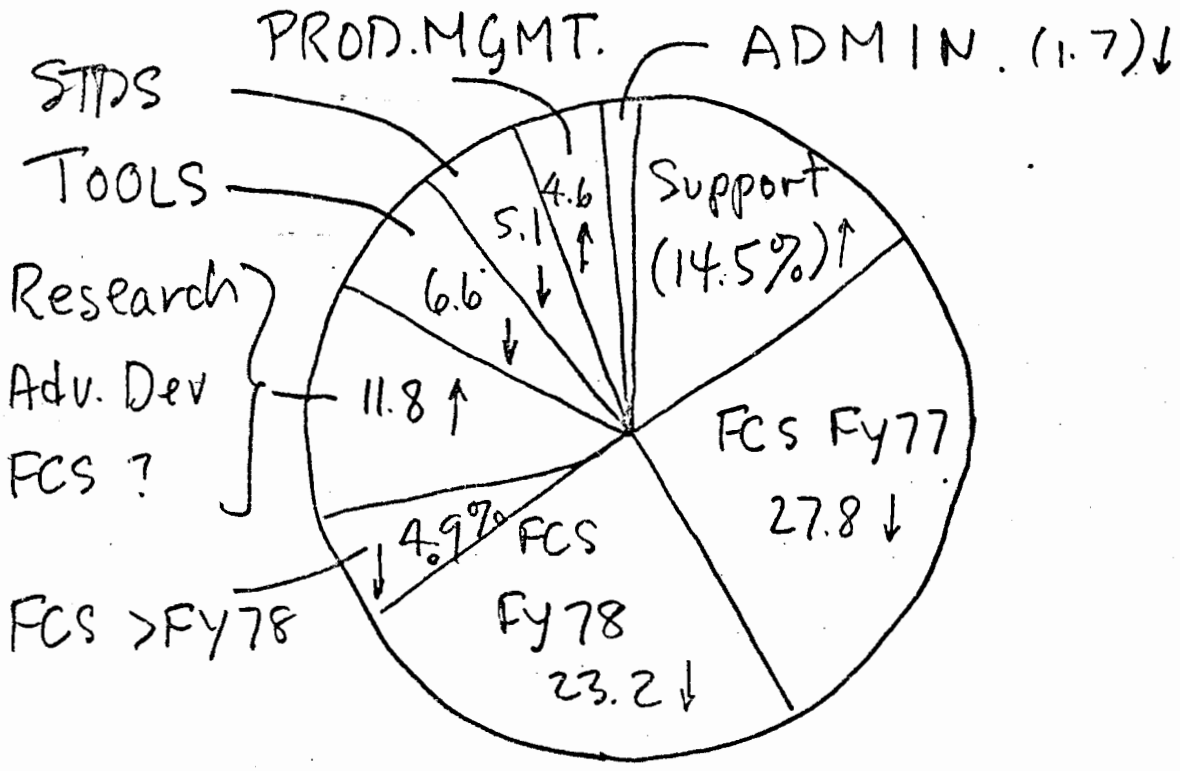
OOD MGMT IS FUNDAMENTALLY RESOURCE ALLOCATION IN SPACE



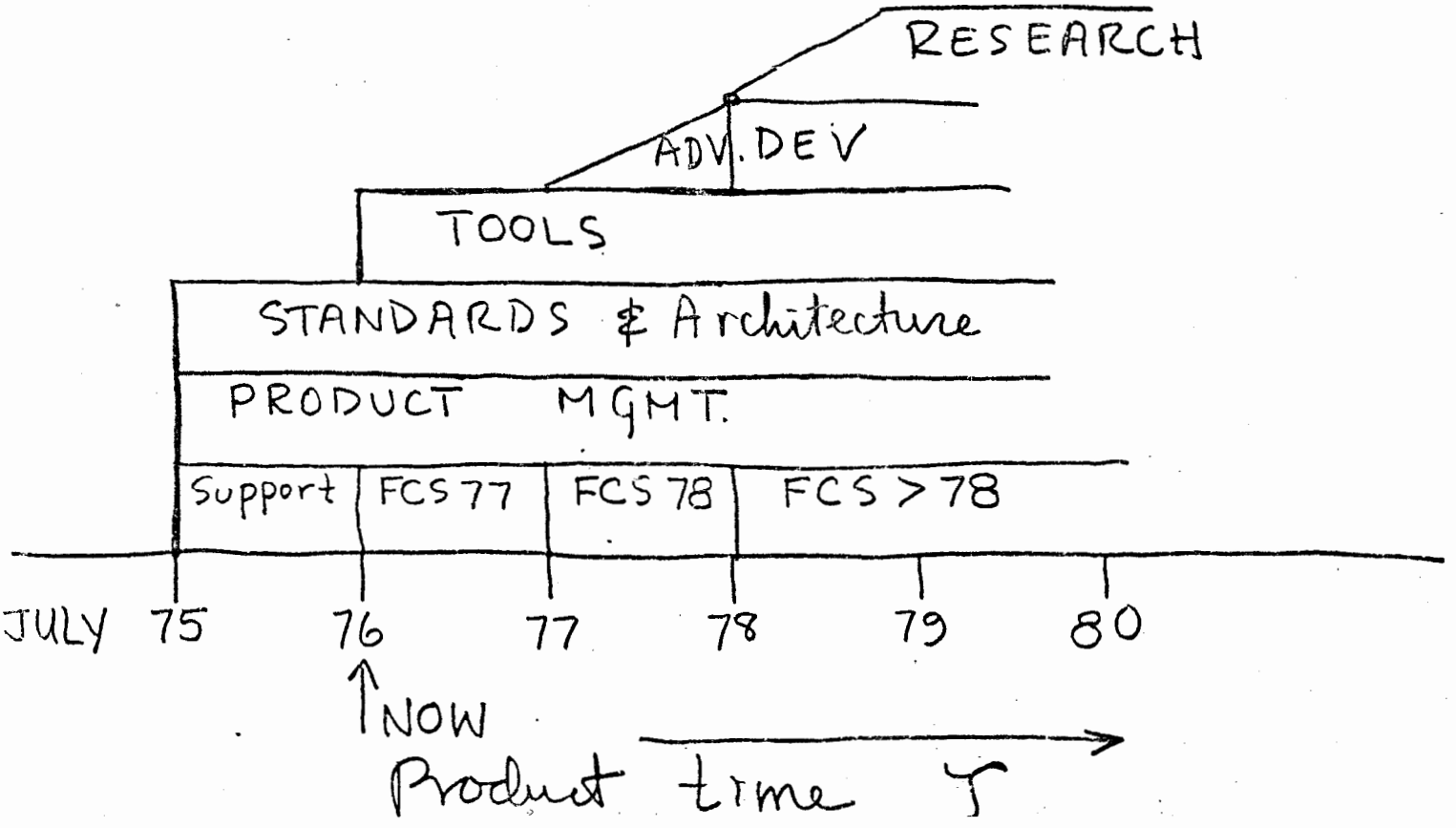

Level-of-integration
8 Application
7 Languages (Application + General Purpose
6 H/S System
5 Boxes (Basic Hardware System)
4 Box
3 Boards
2 Chips (
1 Devices (Phenomena)
MKT. PULL
Generally Tech. Push
Y - product life
-5 -4 -3 -2 -1 0 1 2 3 4 5 6
log (Price)
#
7 ~100 CHIPS
8
9 Board.
10 1K Box.
11
12
13 8K Small System
14
15 Medium System
16 64K shared system
17
18 Very large (Shared System)
19
20 1M
Limit of mini-
Research
Advanced Development
Design start
Start to Manufacture & Market
Announce & sell
Ship
Support
Design Enhancement
Ship Enhancement
Death
Tech Push at End points
gis 1/10/75

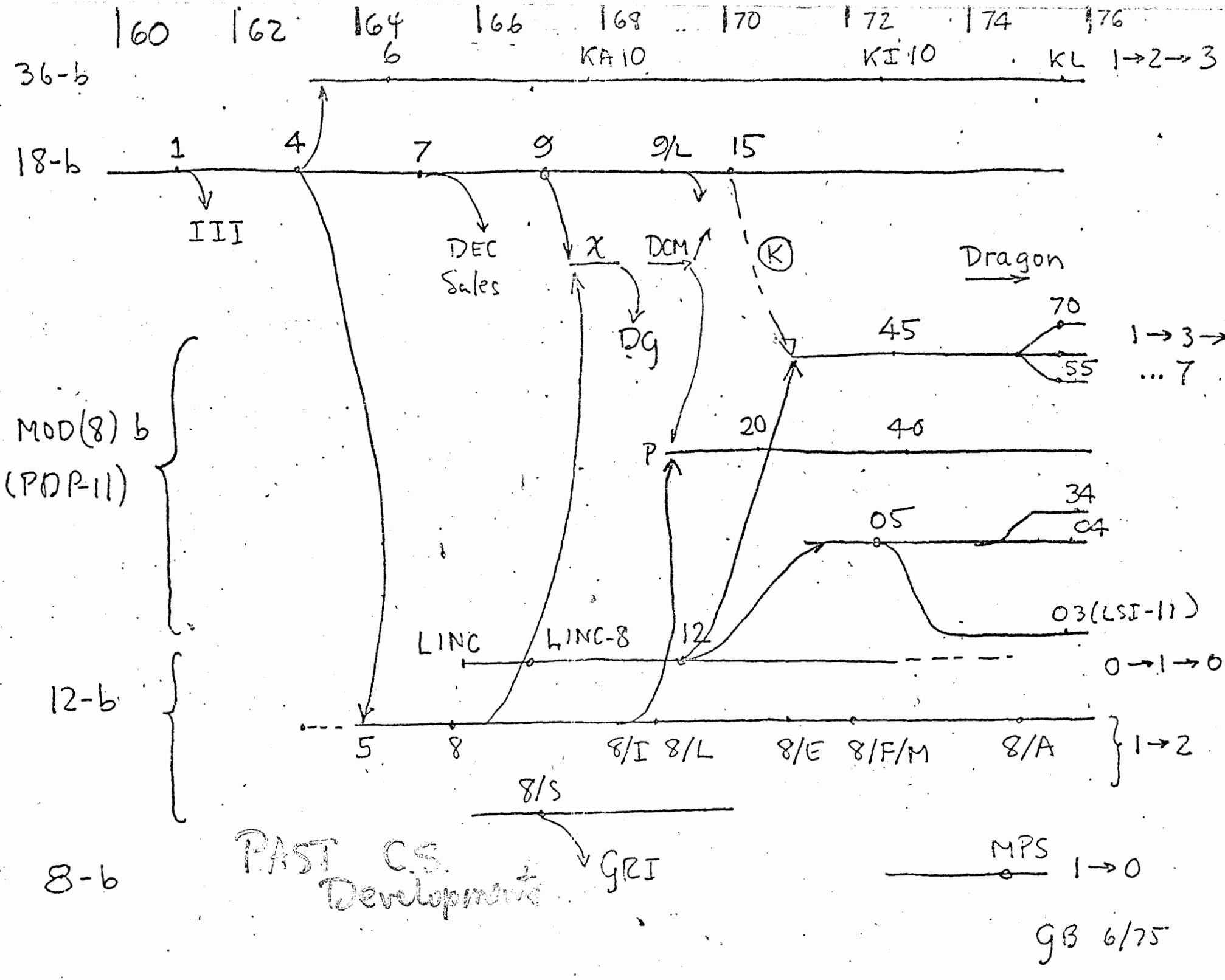
Resources Measurement Categories qB in time (T) dimension.

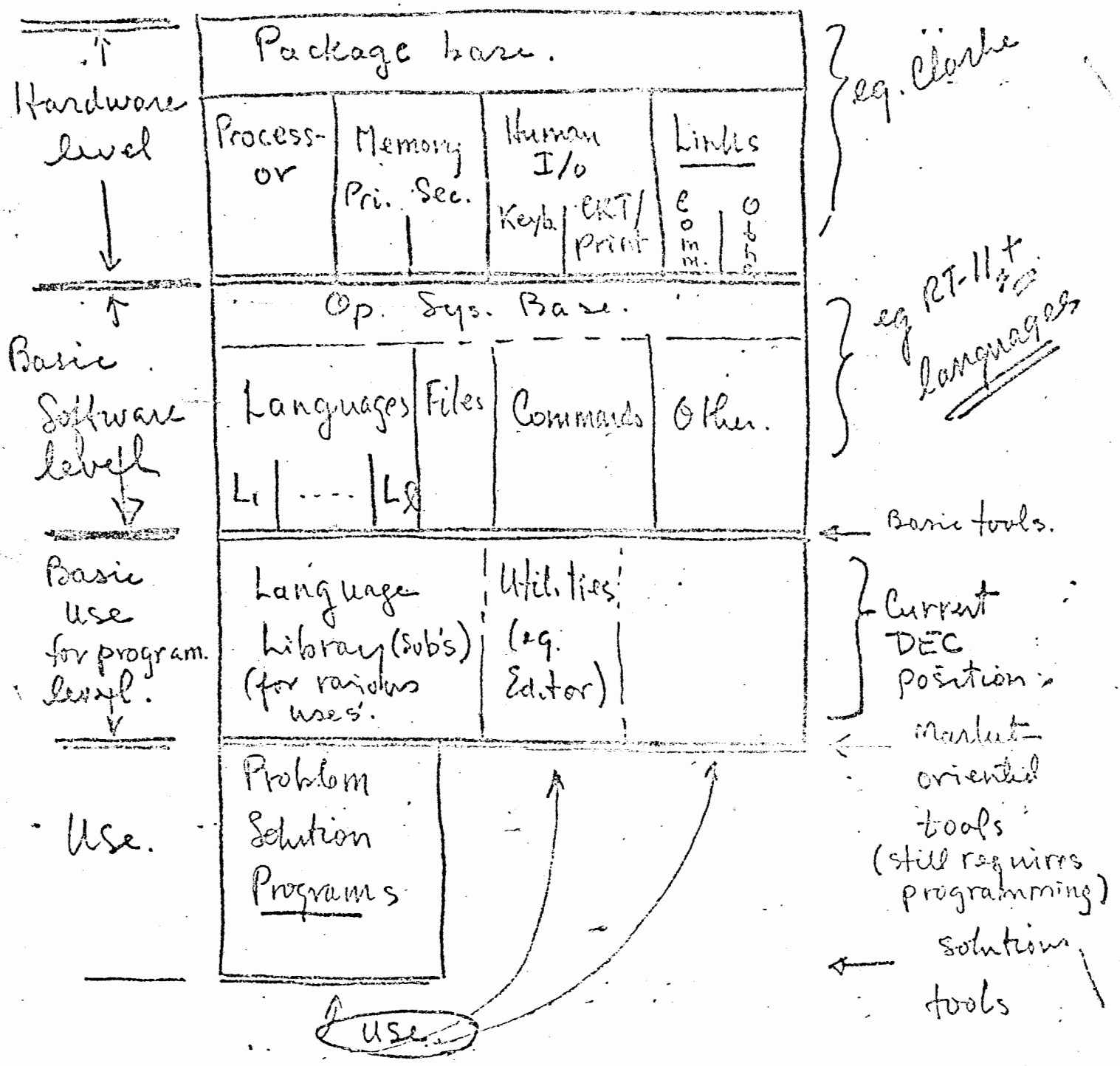
May 9, 197



FY·77 Budget. (Trend FY78)




|60 |62 |64 |66 |68 |70 |72 |74 |76
6
KA10
KI10
KL 1→2→3
36-b
18-b
1
4
7
9
9/L
15
III
DEC
Sales
X
DCM
K
Dragon
DG
70
45
55
1→3→
... 7
MOD(8) b
(PDP-11)
20
40
P
34
05
04
03(LSI-11)
LINC
LINC-8
12
0→1→0
12-b
5
8
8/I
8/L
8/E
8/F/M
8/A
1→2
8/S
GRI
MPS
1→0
8-b
PAST C.S. Development
GB 6/75



Levels of Machines - Partitioning

gb 21 Sept 1978

PROCESS

TIME-YEARS (3)

multi-disciplin

PROCESS	SOFTWARE (OS, LANGUAGES)	CPU (LARGE)	DISK
basic idea → RESEARCH	0-20	1-10	1-10
→ DISCLOSURE PATENTS			
proto { TECHNOLOGY ADVANCED DEVELOPMENT	1/2-2	1-2	1-2
→ PEOPLE (ISS, MRX)			
(schedulable) DEVELOPMENT	1-2	1-2	> 2
→ TOOL-UP			
TEST, TOOL & DMT	1/4-1/2	1/2-1	1
→ FCS			
SHIP	1/4-1/2	1/4-1/2	1/4-1/2
EDUCATE & USE	1/2-5	1/2	0

1/4 - 2

ANNOUNCE MKT DEMAND

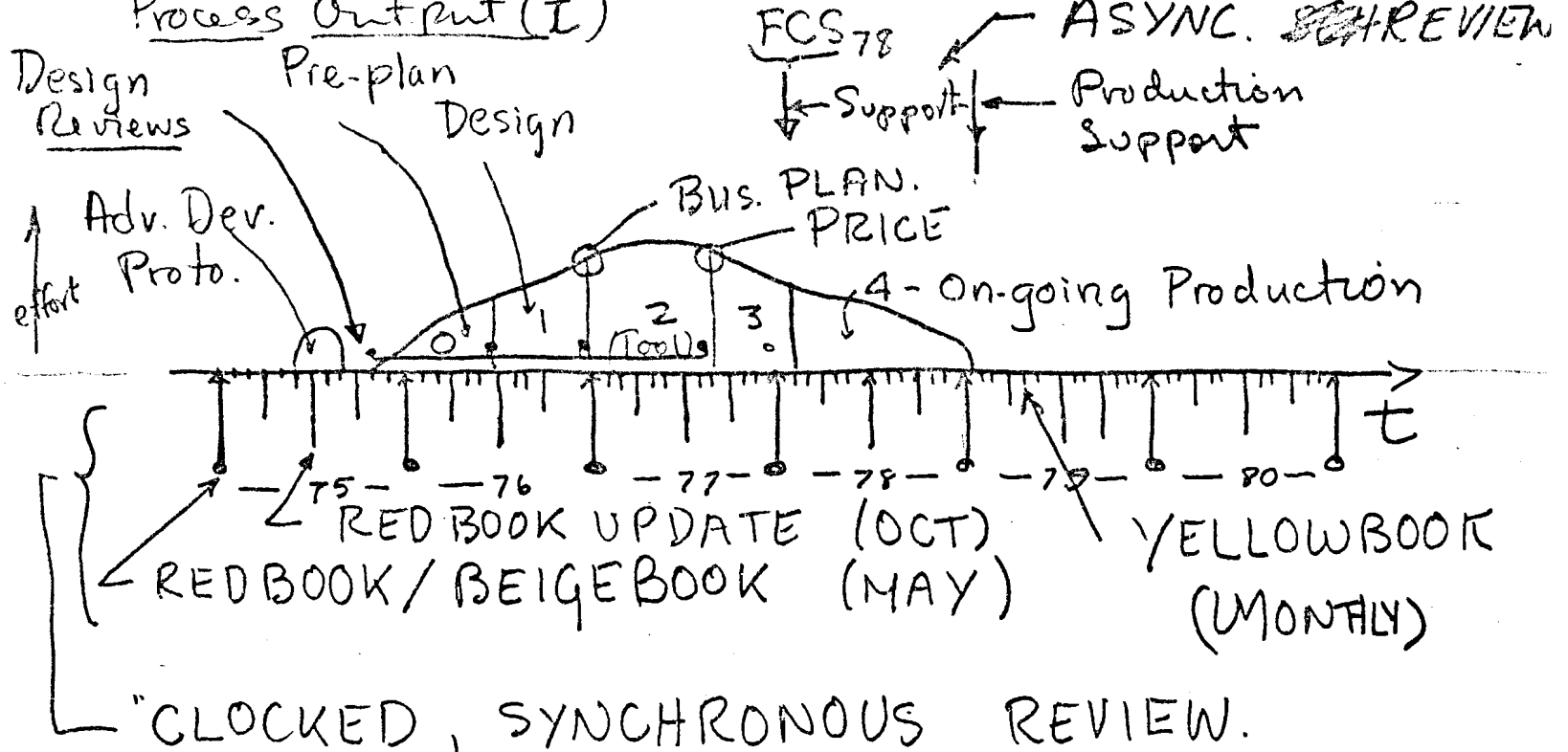
1 ~ 2

ANNOUNCE MKT DEMAND

Commod.

MKT DEMAND

Education / [illegible]
(mkt)



Project Effort vs. time.

Reviews:

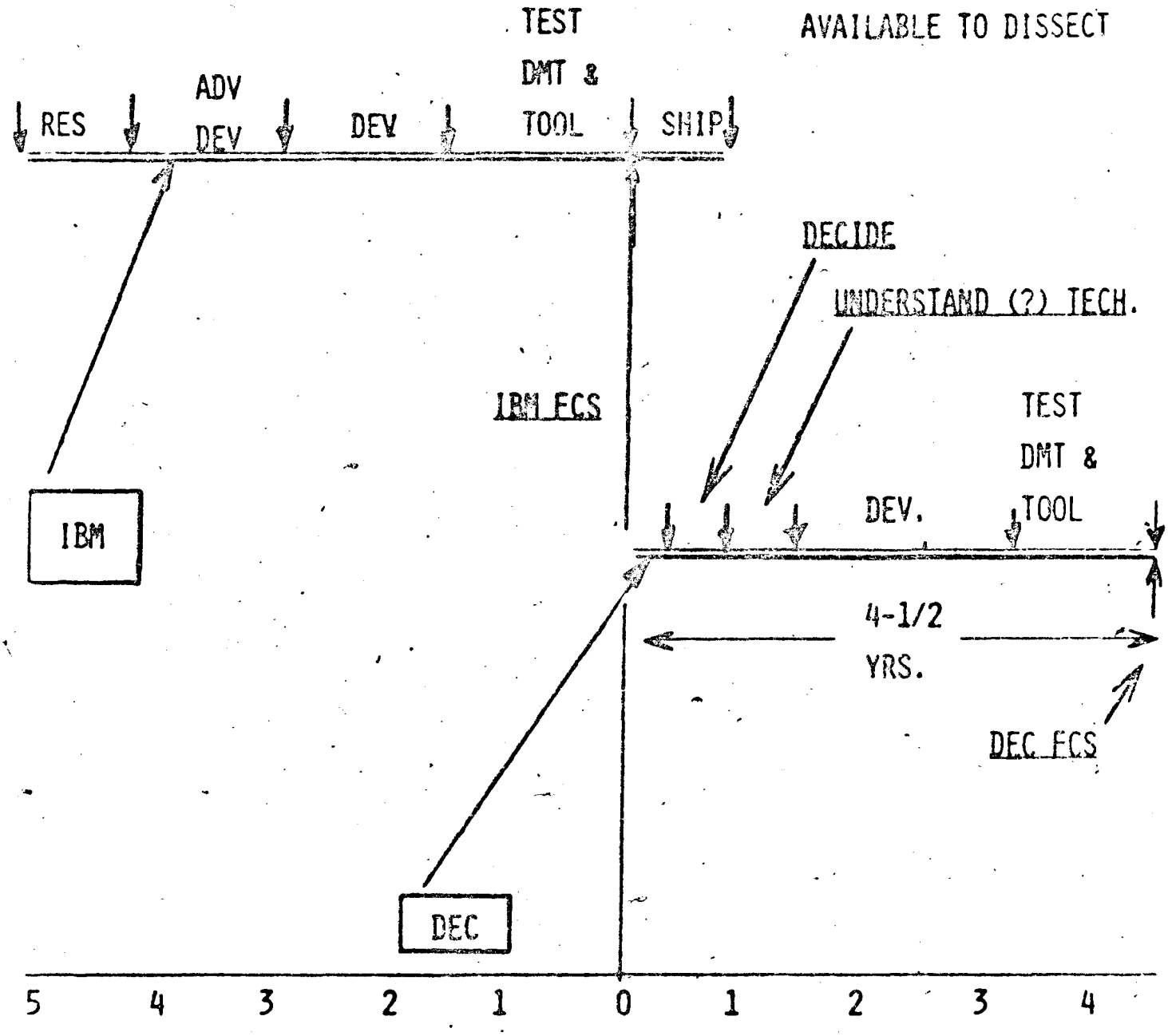
SYNCHRONOUS

- Redbook
- Redbook update
- Yellow Book (status update)

Asynchronous (Project Based)

- Prototype (Adv. Dev.). {Idea Generation}.
- Prel. Plan. {alternatives to select from}.
- Design Reviews (Measures/monitors Project)
- Business Plans (Reviews)
  - 2 page (to go into design)
  - To go ahead
  - To produce
  - To build/sell.
- PSG monitor

gb May 9. 1976



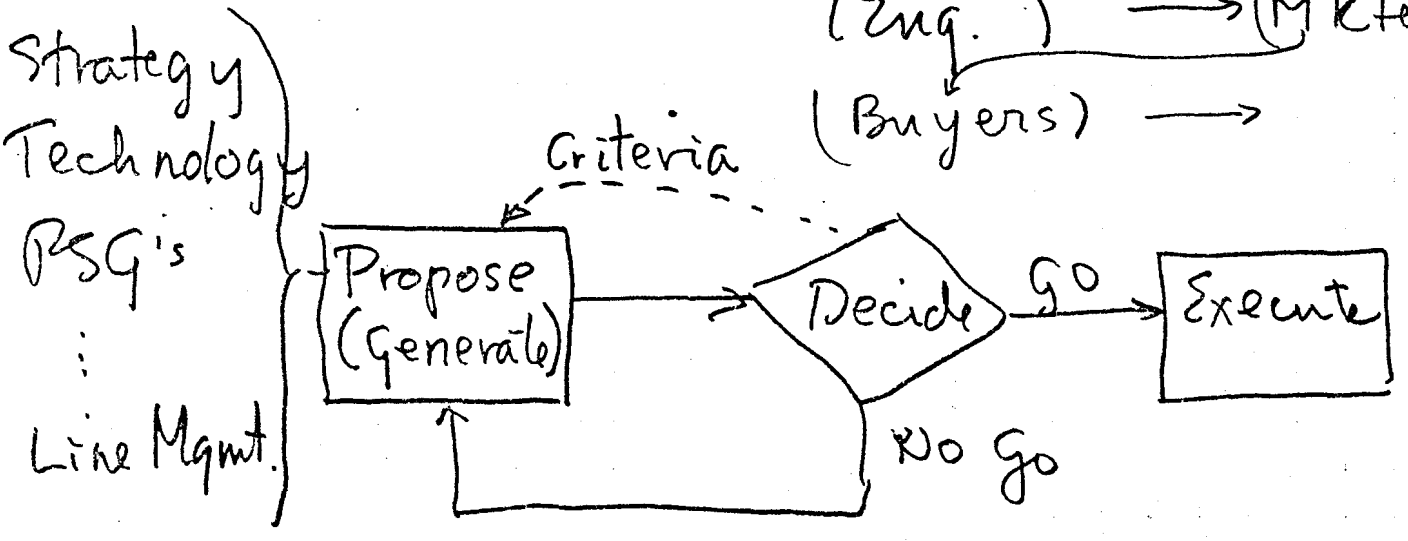
TIMES FOR IBM/DEC DISKS

DECISION-MAKING WITHIN OOD

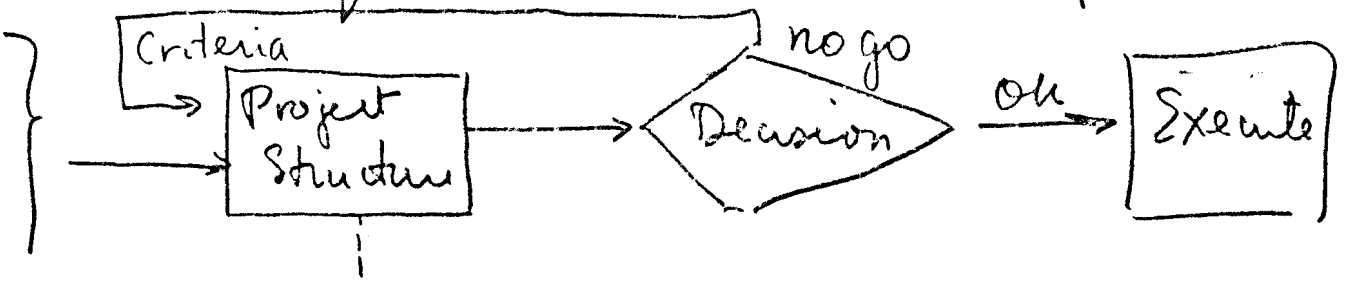
GB
May 9, 1976

- Fundamentally no substitute for Hi-Q. Person(s)
- Basically decisions are made according to Model set forth by Ken and Op. Comm.
- Carry forward notion of a (decision) process & attempt to form structures (Organize) such that: Individuals can propose and have decided such that individuals are responsible to do.
  (i.e. he who plans, does).

- Process requires: Producers → Consumers
  (generators) → (Testors)
  (Designers) → (Evaluators)
  (Eng.) → (MKters)
  (Buyers) → →



(General) Techniques for Decision-making May 9, 1976



Inputs (Comm.) ——→ monitor fcn.

- 5 year strategic plans, (Budget allocation)
  Redbook... ; Meetings
  DEC Stds. / Policies / processes (eg. approval process).
  DEC Goals (roi program).
  Competitive ideas
  Technology base: R&D; Idea; Invention
  → Market Requirement (need). PSG.
  Specify Action ... i.e. Tell 'em. + Manage

STRUCTURE / MANAGE {Team, Task force, Committee, Indiv.

Organiz. Engineering. / Matrix / Move People (skills)
Educate / Train
Consultants. Or Get 1 or 2 Good People.

Monitor
Yellow books, Redbooks, PSG's.

Decision
Specify Problem, Goals, Constraints, Evaluation Criteria

(tradeoffs)

Problems in Decision-making

GB 9 May 72

We are significantly Market driven (via PSG's, MKters, etc.).
As we get larger, it is harder to Recover from poor MKT-based (Persons) ~~D&R~~ Recommendations vs. Tech. risk.

Examples:

→ Don't write down Goals, etc. hence instability
→ Don't move out far enough (mP)
→ Don't understand new mkt. (LSI-11)
→ Don't understand Systems we'll Sell (eg. Size on 11/70)
→ Don't understand changing mkt. (optimize R-R vs. Real Performance).
→ "Mill Around", No Clear decision/Test (CIS).
→ Overall the developers want to be heros ... i.e. building anything is OK. and avoids risk of Project Cancel. (eg. Unicorn
→ Don't understand risk of a fully peopled company. Mfg. ... F/s. — hence minimum product cost, max. user (etc.) Cost.

CONTROL (DECISIONS) VIA FUNDING gB 9 May 72

- PROJECT DIRECT (Hdw., SOFT, Hdw+ Soft.)
  Memory (electronic, disk, tape), Comm., terminals, CPU's, Operating Systems, Languages.

- PROJECT SUPPORT (Fully purchased Services)
  Drafting, Model shops, Consulting, Computers, EDP.

- PROJECT SUPPORT WITH TECHNOLOGY BASE
  LSI, PKG., POWER, DIGGNOSTICS, QUALITY
  - Purchasing, Components, testing, tool-up
  - Manuals, Training.

- Open loop
  Tools, Standards, Research, Adv. Dev.
  Library, Program Library.
  Field Service, Software Support, Training.

LARGE - SMALL COMPARISON

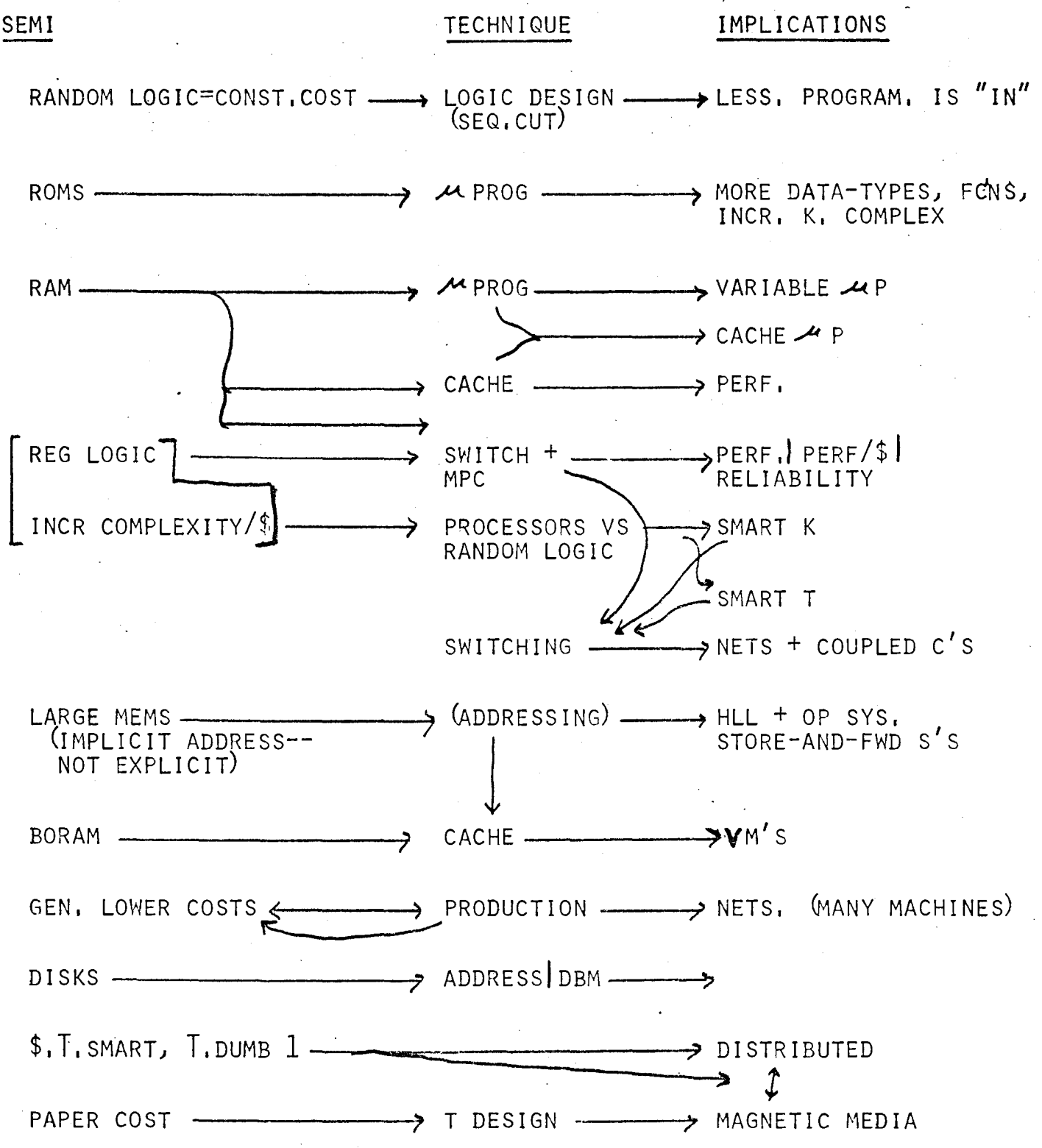
Circa 1967	Cost	WL	Mp Size	Mp.size/ $ bits/$	MIPS	MIPS x WL	REAL(MIPS)	P/C (MIPS/M$)
8	10^4(1)	12 (1)	$5x10^4$(1)	5	$.3x10^6$(1)	(1)	10^3(1)	30
6600	$3x10^6$(300)	60 (5)	$8x10^6$(160)	2 2/3	$3x10^6$(10)	(50)	$3x10^6$(3000)	1
Circa 1975								
Brd	10^3(1)	16 (1)	$4x10^3$w(1)	64	.3 (1)	-		100
8600	10^7(10^4)	64 (4)	$1x10^6$w(10^3)	6.4	100(10^4)	-		10

SOME OBSERVATIONS

1. Performance: low end is about the same. High end up 10∼30. Gap 10 ⟶ 300 (30)
2. Cost : low end is cheaper by x 10. High end up x 3. Gap 300 ⟶ 10,000 (30)
3. Mp. size no economy of scale.

GB
2/7/75

TECHNOLOGY



GB
2/7/75

PRICE PERFORMANCE IN 8 FAMILY

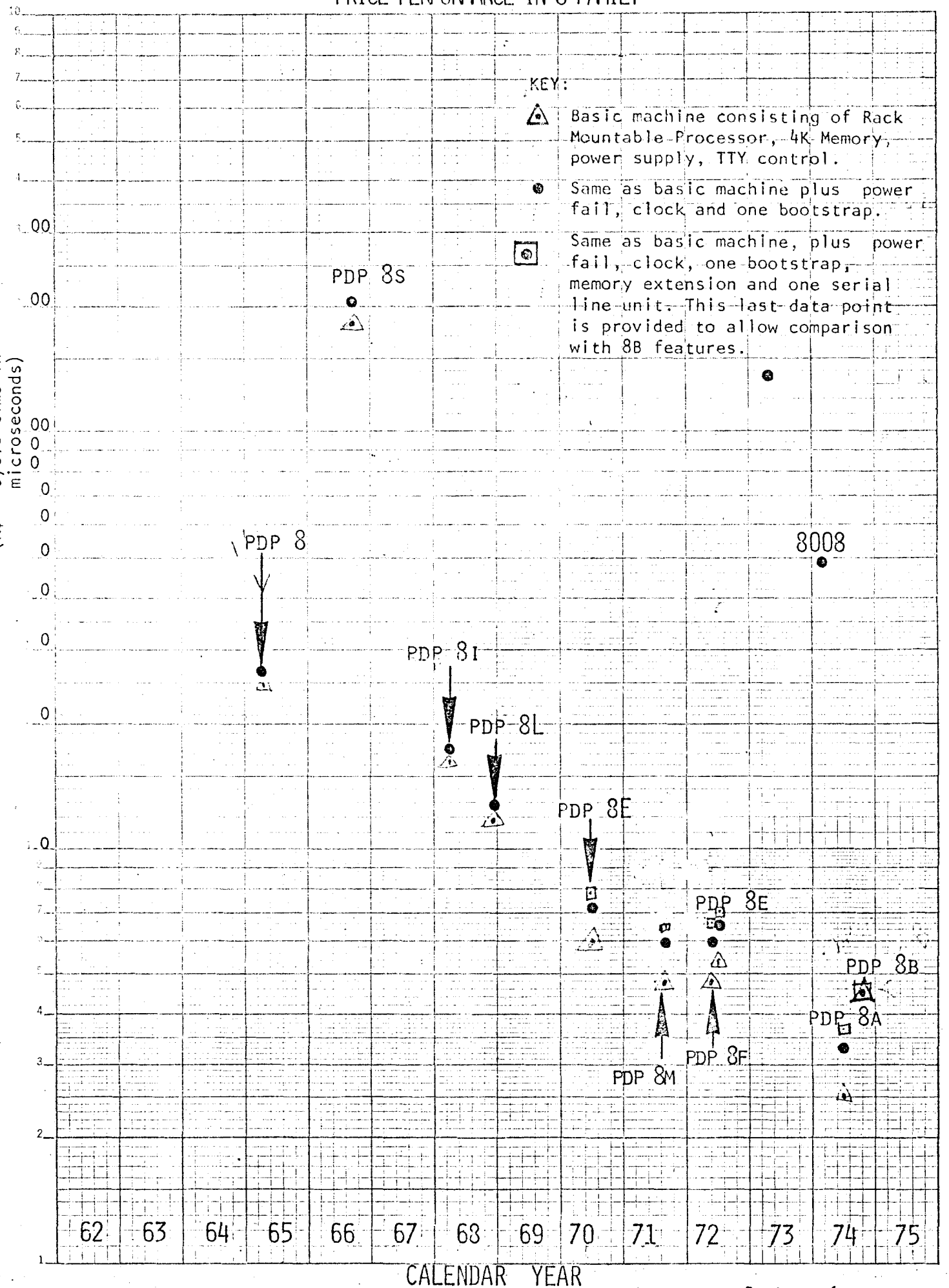
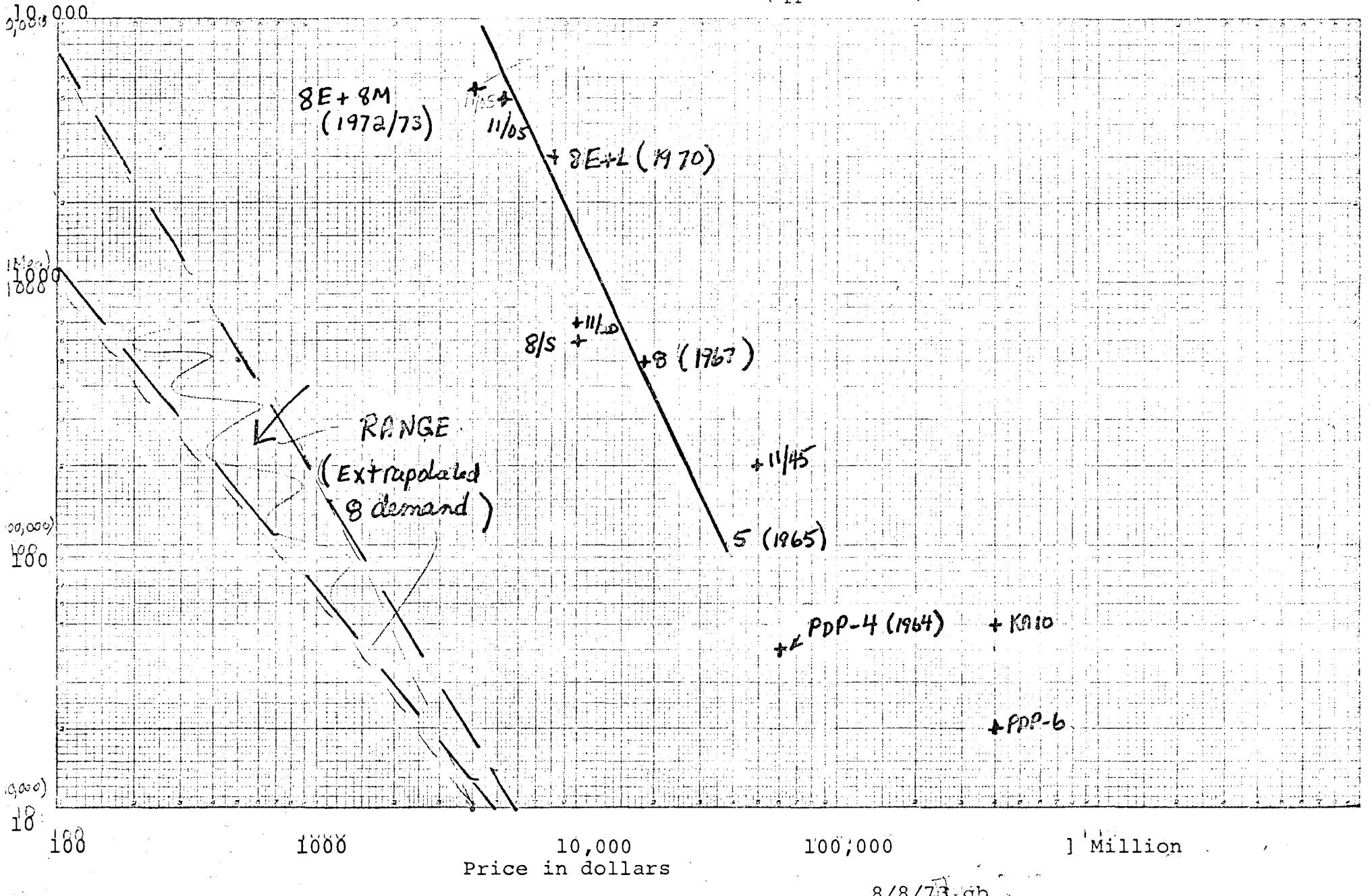


FIGURE 2

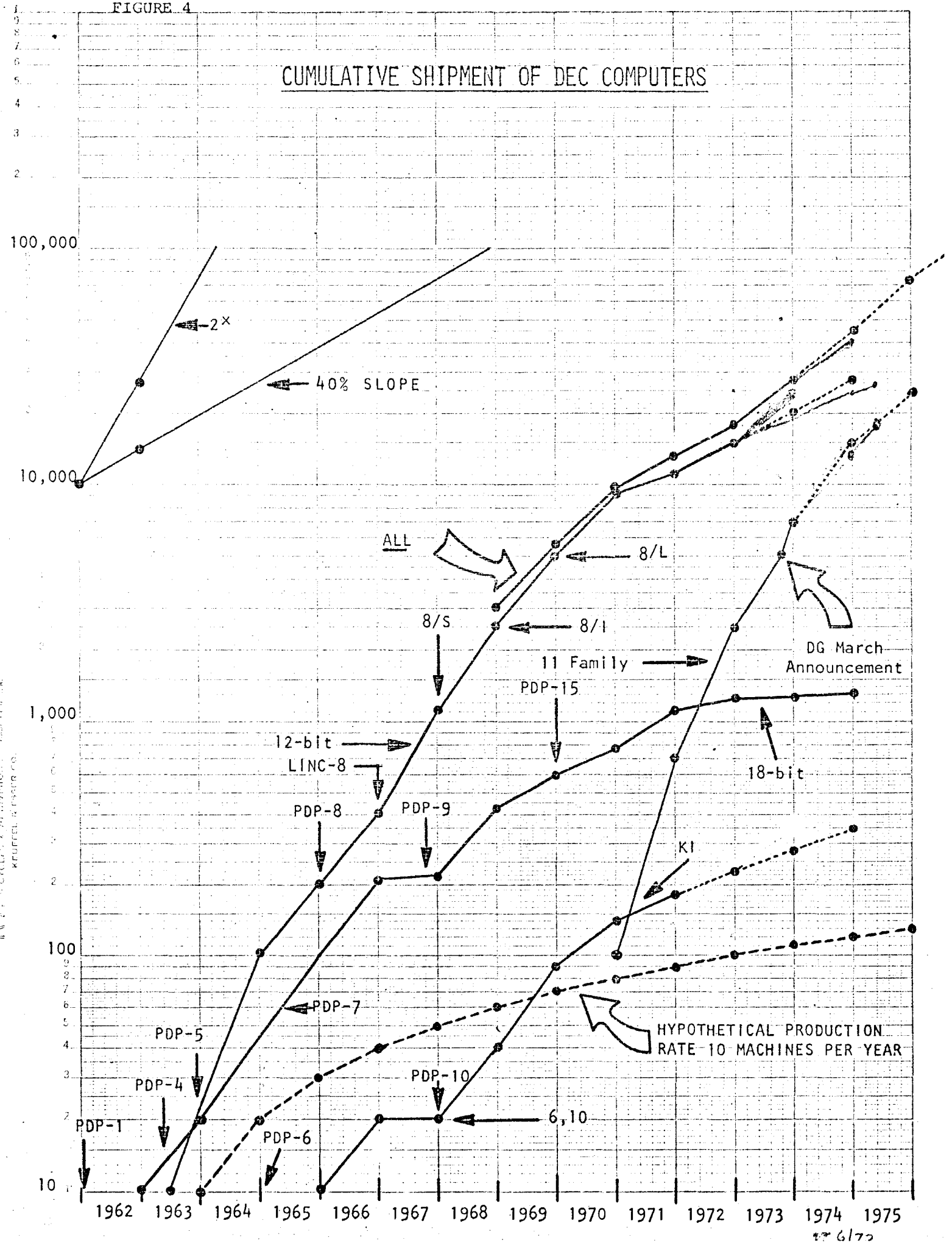
P. Laut 6-22-73

(1st year--after start-up transient.) Figure 3 DEMAND FOR VARIOUS PRICED COMPUTERS
(Approx. data.)



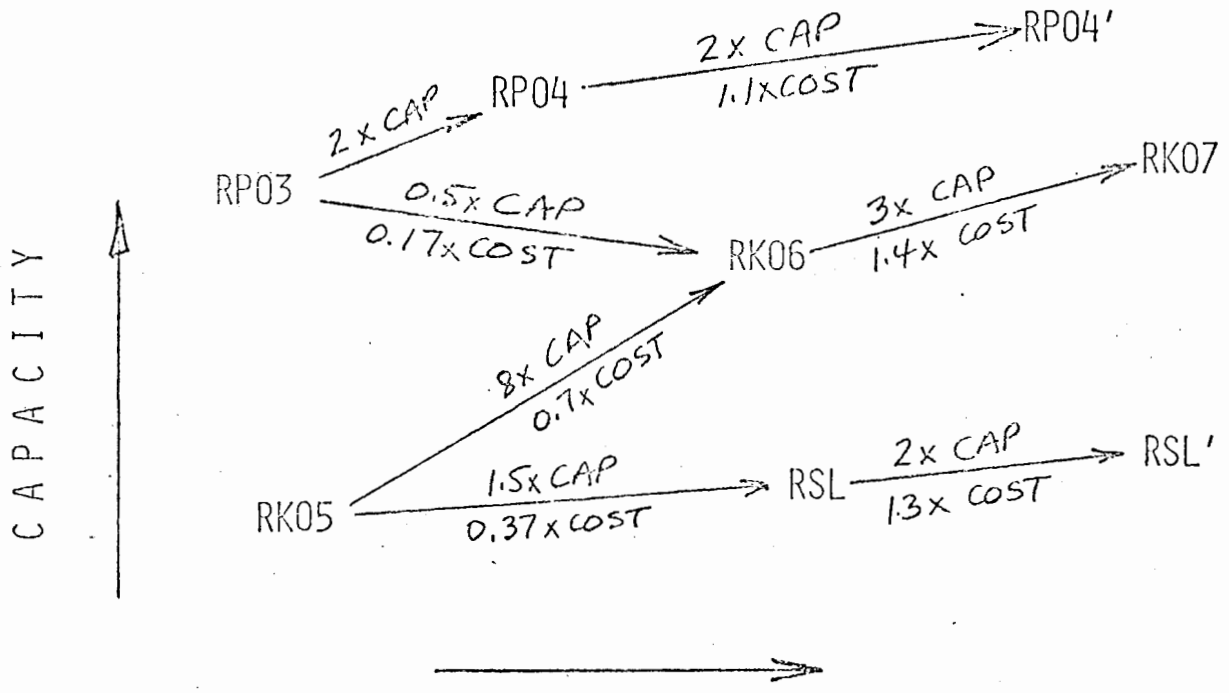
8/8/73 gb

FIGURE 4



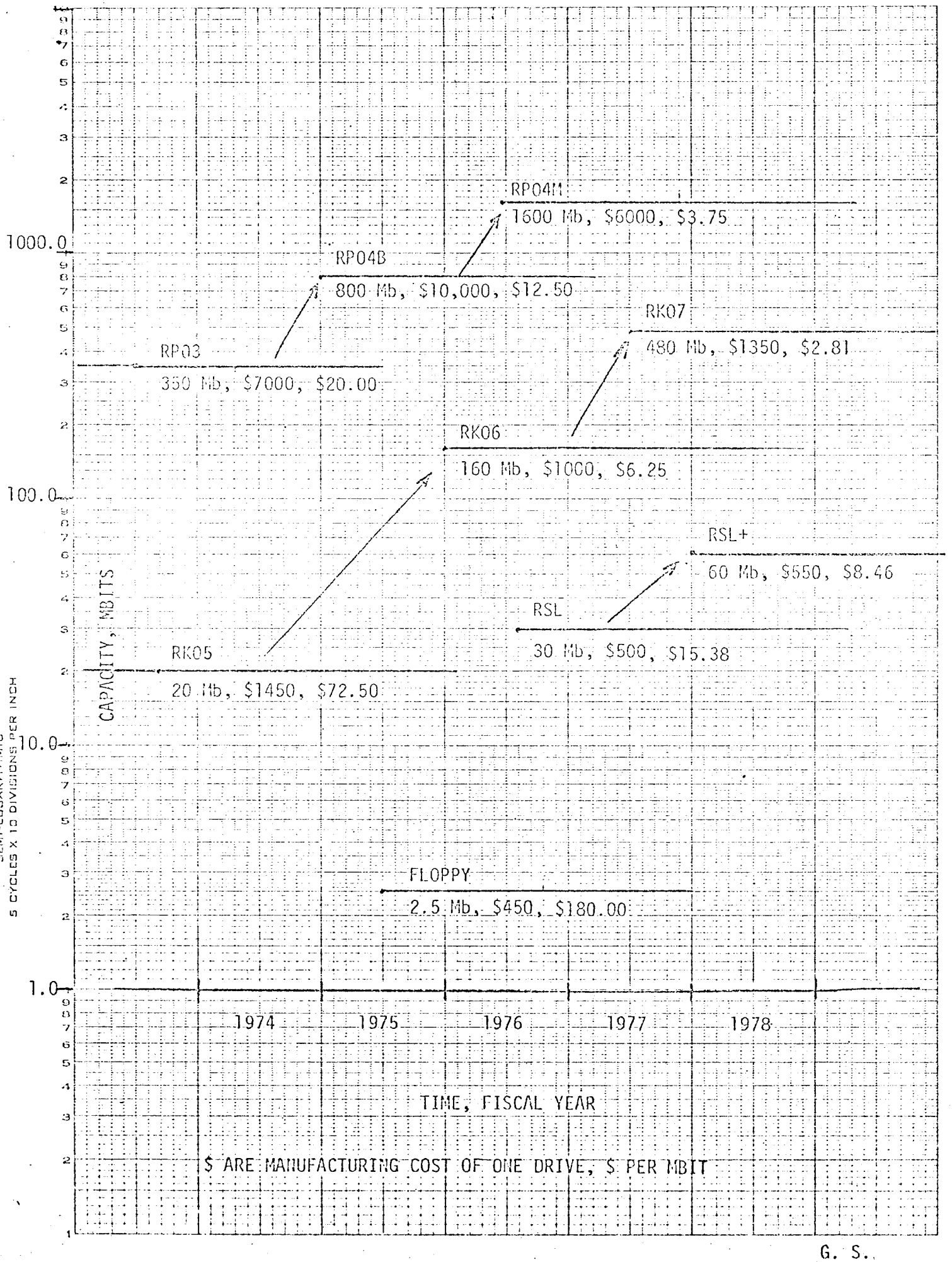
CUSTOMER GROWTH

DEC MOVING HEAD/ REMOVEABLE MEDIA DISKS



ALTERNATIVES: 1. CONSTANT COST, INCREASED CAPACITY

2. DECREASED COST, CONSTANT CAPACITY



G. S.
11/28/73

22x34

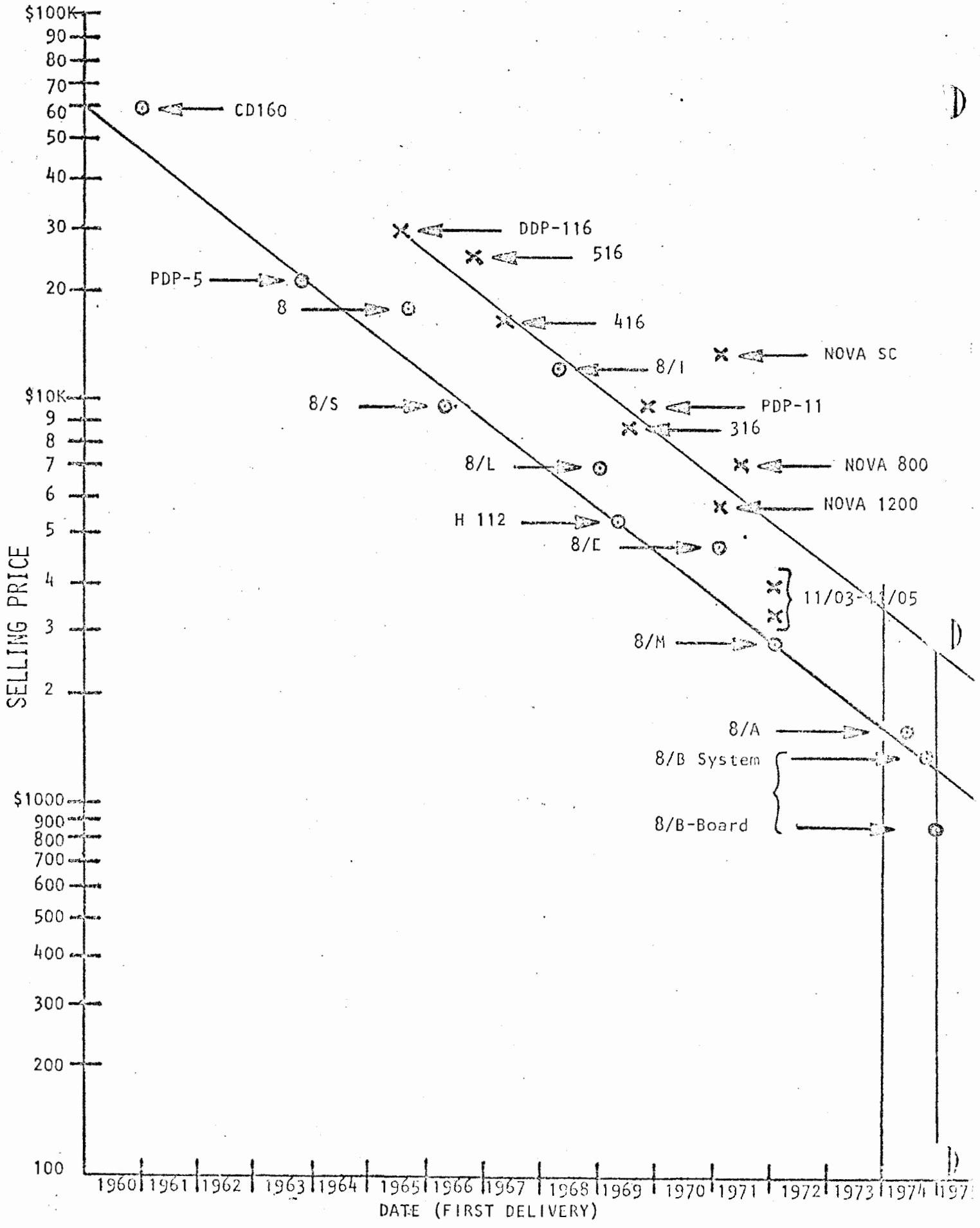


FIGURE 1 SELLING PRICE VERSUS FIRST DELIVERY DATE FOR MINICOMPUTERS

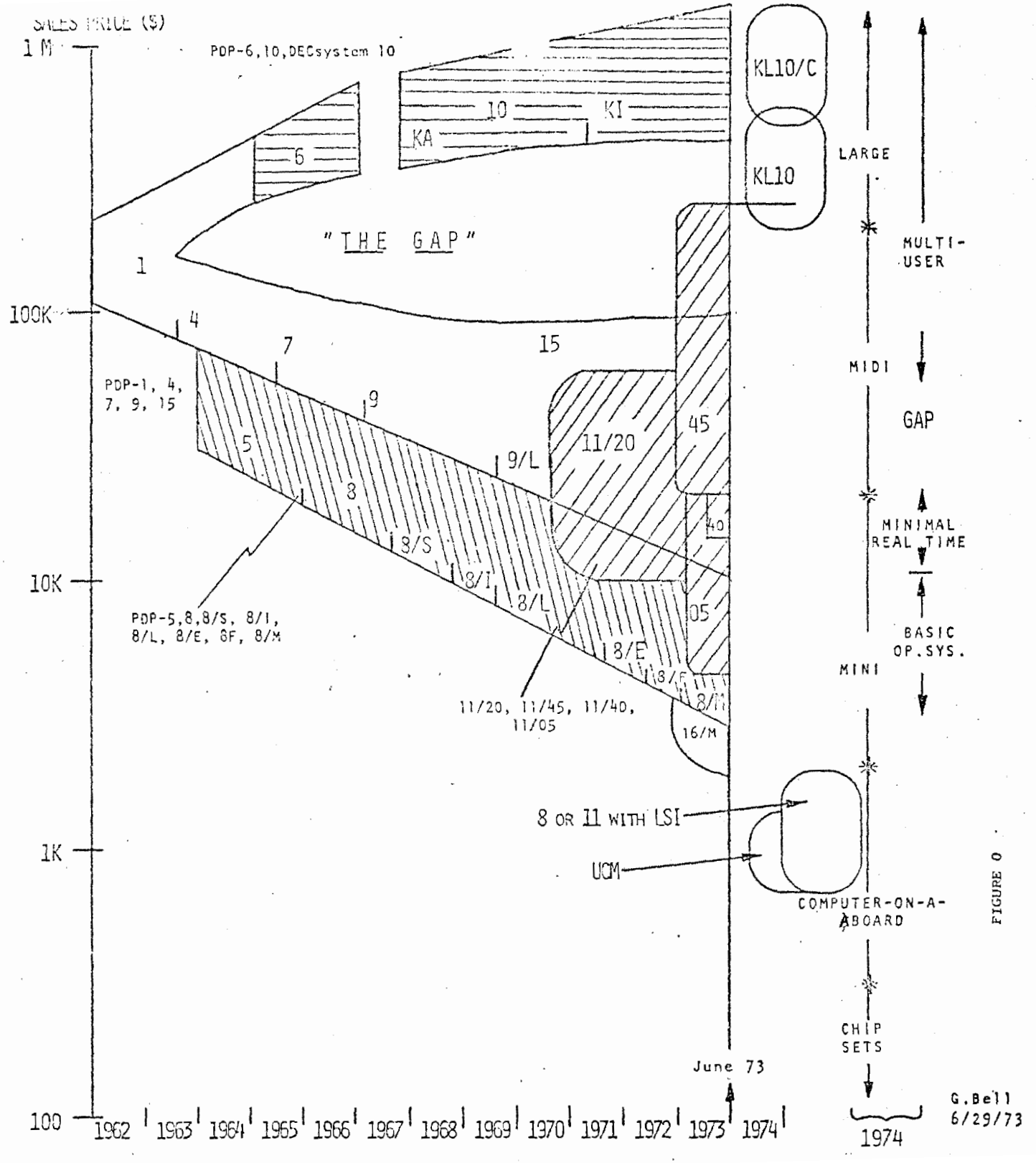

SALES PRICE ($)
1 M
100K
10K
1K
100
PDP-6,10,DECsystem 10
KL10/C
KL10
10
KI
KA
6
"THE GAP"
1
4
7
15
PDP-1, 4, 7, 9, 15
9
5
8
9/L
11/20
45
40
8/S
8/I
8/L
05
8/E
8/F
8/M
16/M
PDP-5,8,8/S, 8/I, 8/L, 8/E, 8F, 8/M
11/20, 11/45, 11/40, 11/05
8 OR 11 WITH LSI
UCM
COMPUTER-ON-A-BOARD
CHIP SETS
June 73
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1974
LARGE
MULTI-USER
MIDI
GAP
MINIMAL REAL TIME
BASIC OP.SYS.
MINI
G.Bell 6/29/73

FIGURE 0

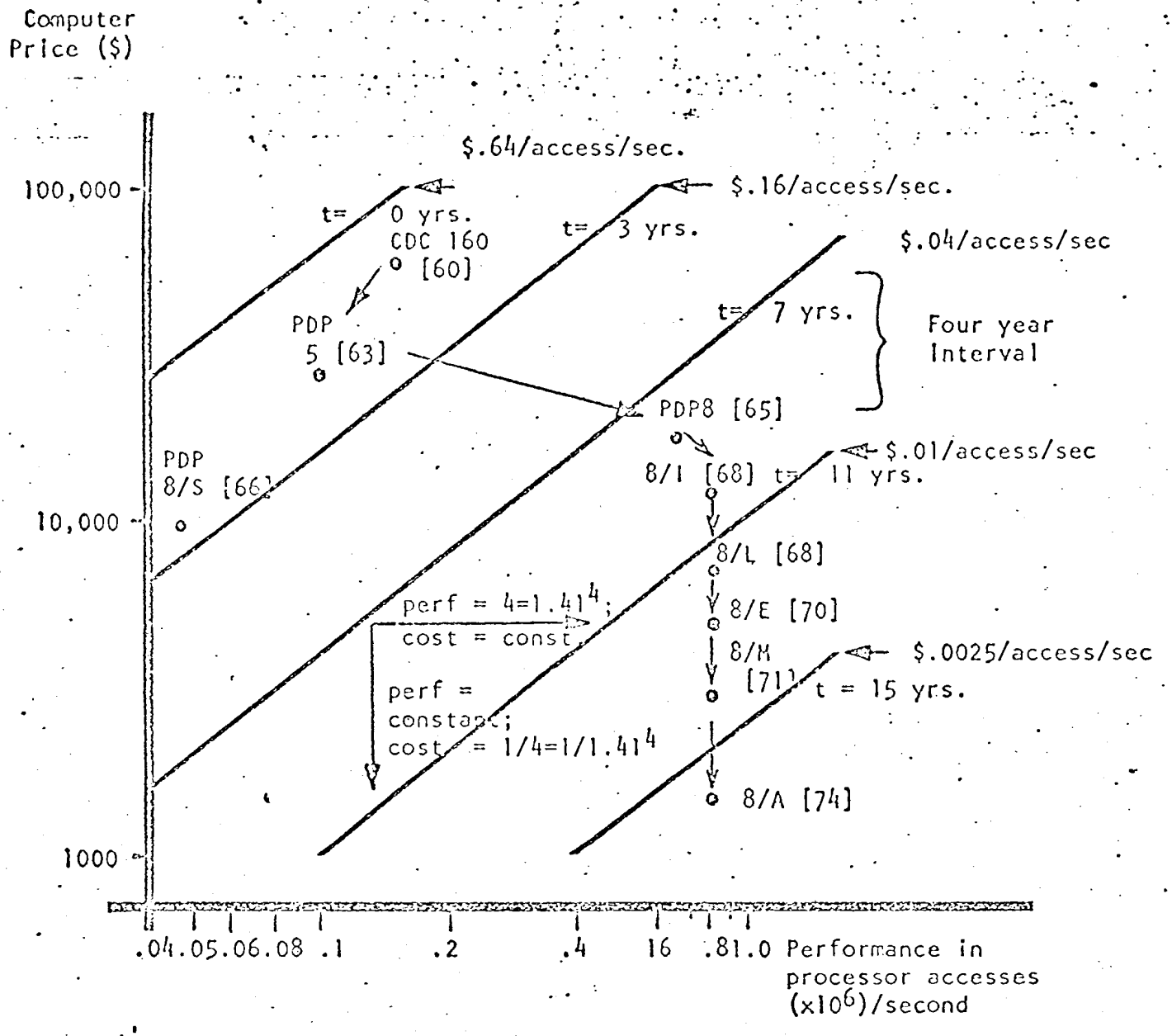
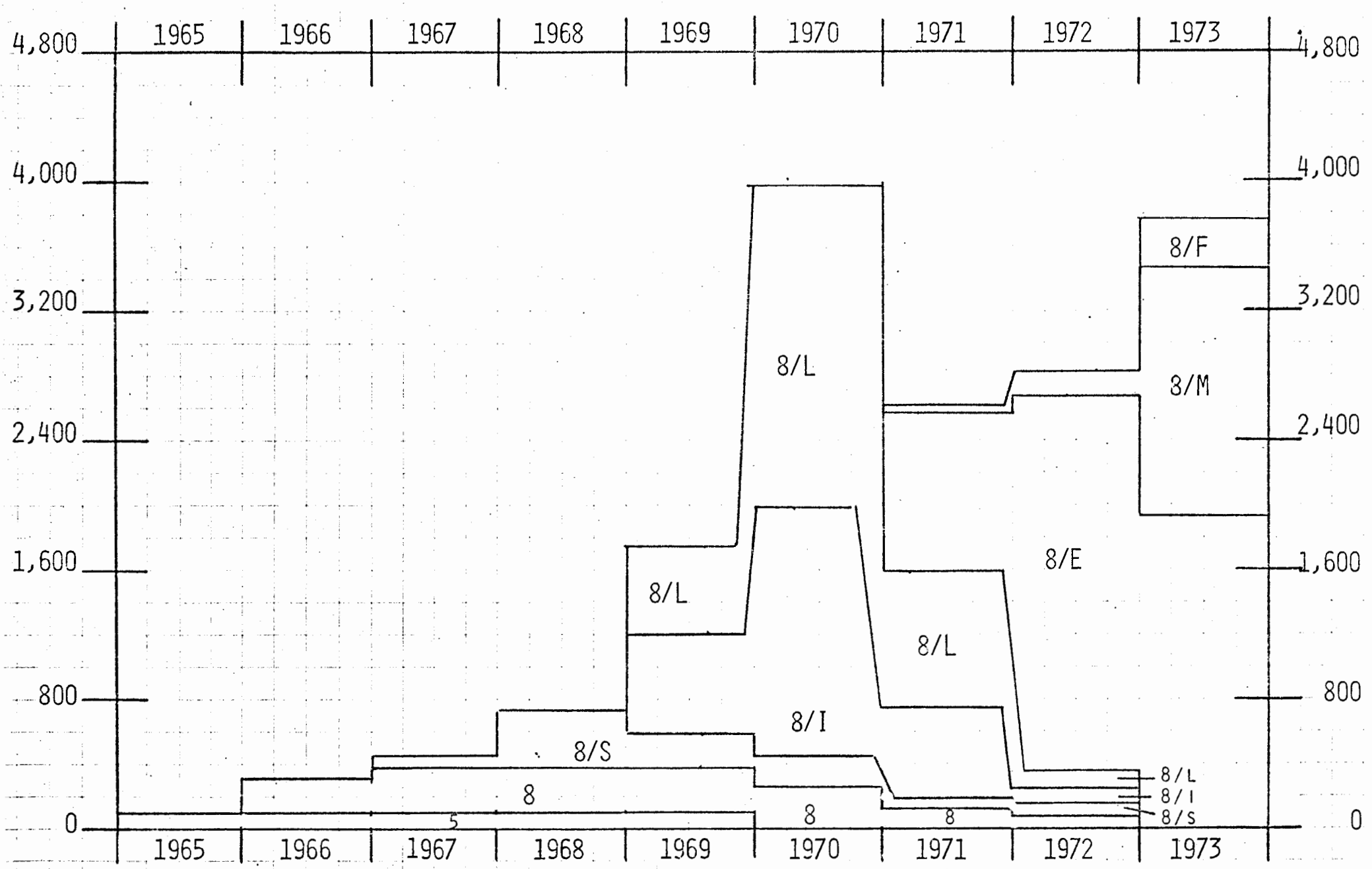
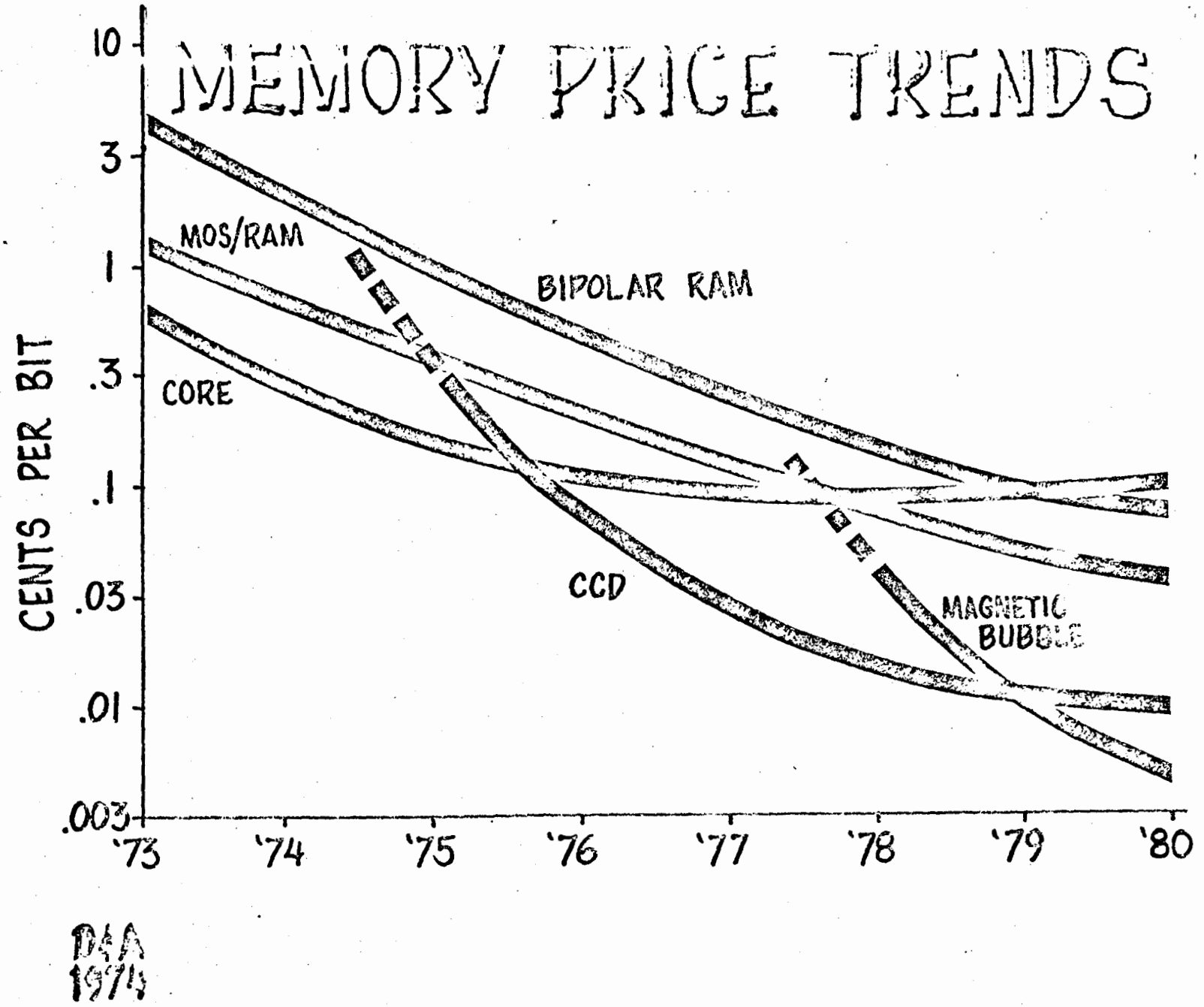


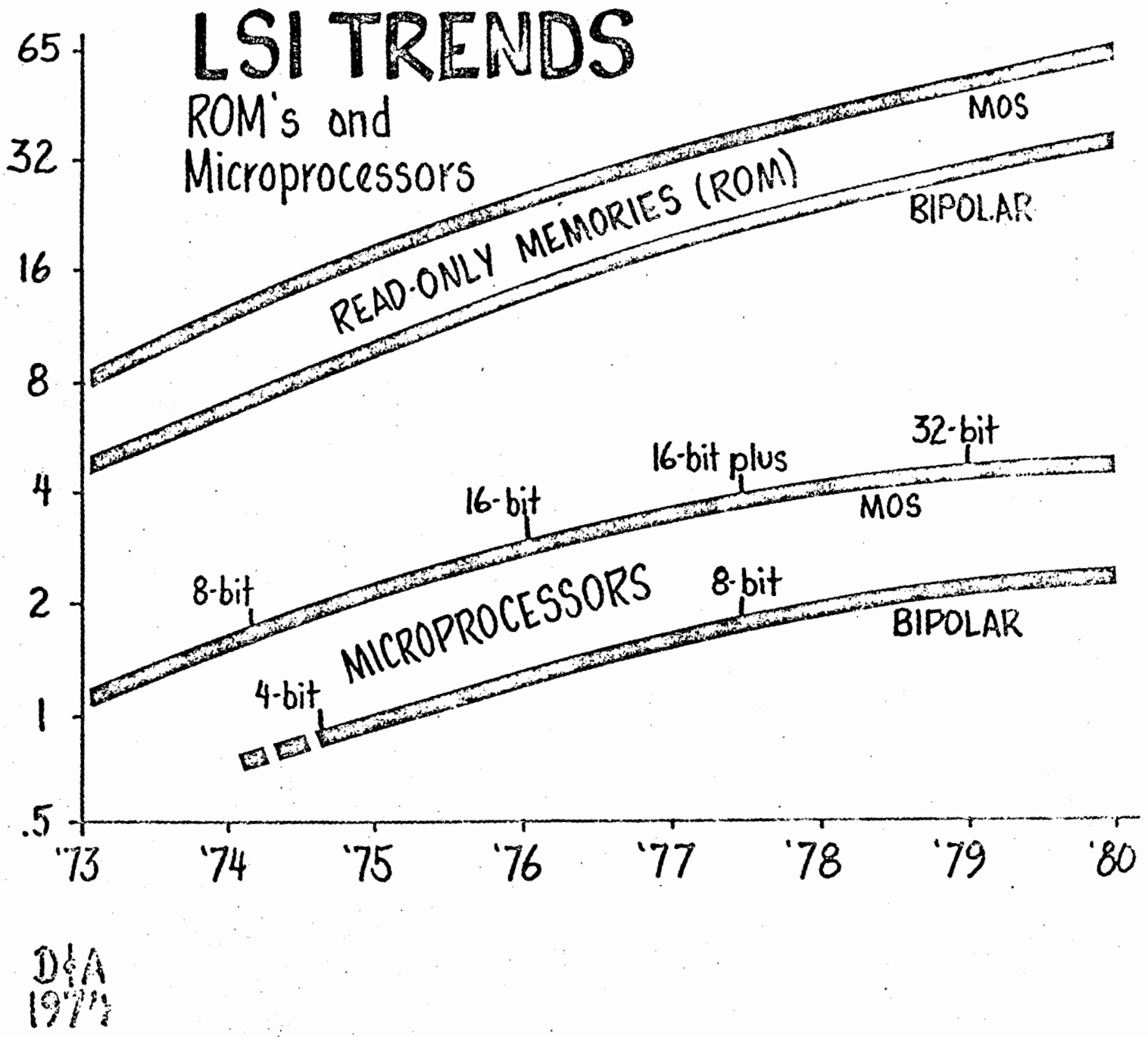
FIGURE 3 MINICOMPUTER PRICE VS PERFORMANCE FOR VARIOUS TECHNOLOGIES. LINES OF CONSTANT COST/PERFORMANCE ($/ACCESS/SEC) ARE PLOTTED FOR EACH FOUR YEAR'S (FACTOR OF 4 = 1.41^4) ASSUMING IMPROVEMENT OF 41% PER YEAR

FIGURE 5 PDP-8



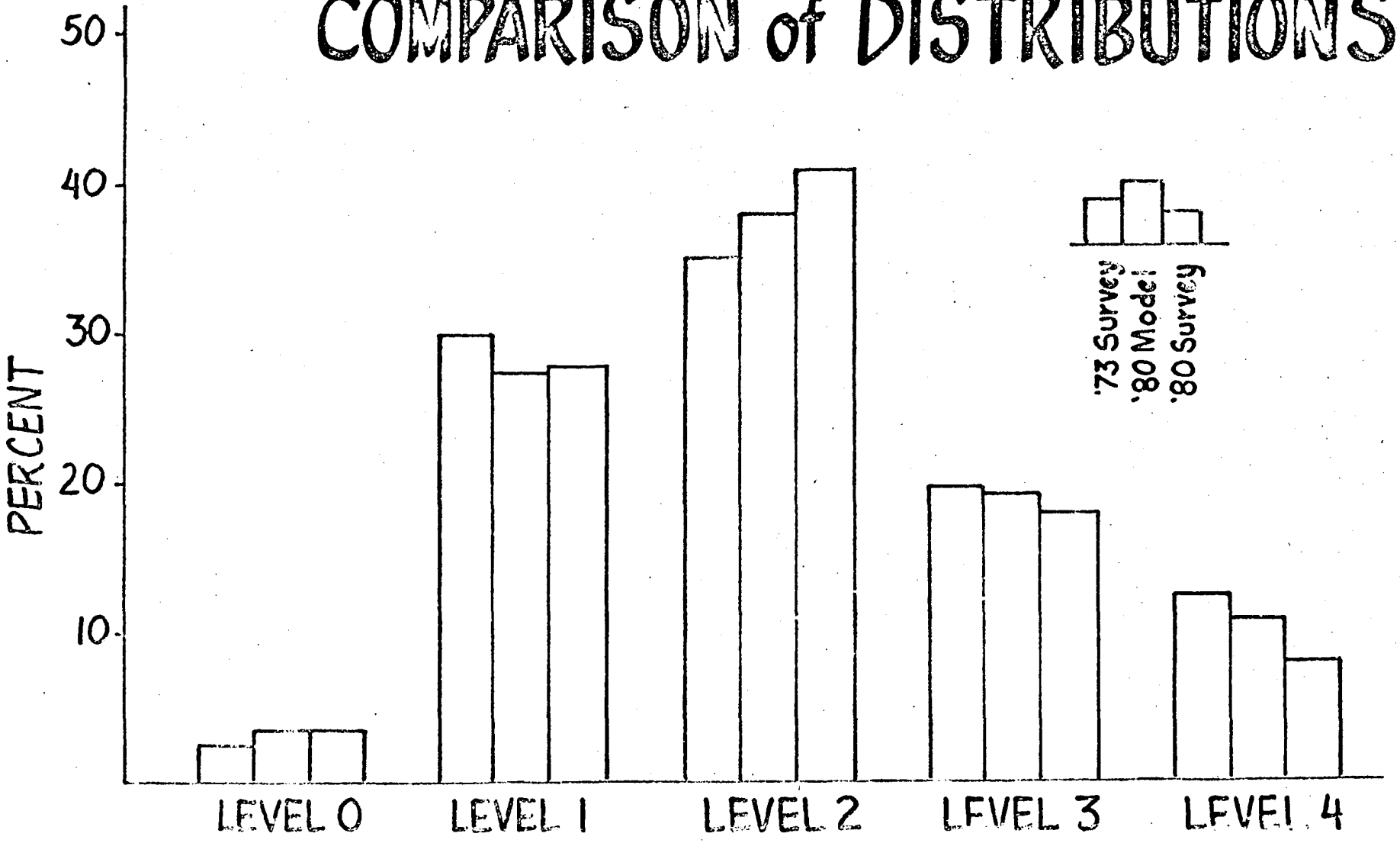

MEMORY PRICE TRENDS
CENTS PER BIT
10
3
1
.3
.1
.03
.01
.003
'73
'74
'75
'76
'77
'78
'79
'80
MOS/RAM
BIPOLAR RAM
CORE
CCD
MAGNETIC BUBBLE

DAA
1974


LSI TRENDS
ROM's and
Microprocessors
65
32
16
8
4
2
1
.5
'73
'74
'75
'76
'77
'78
'79
'80
READ-ONLY MEMORIES (ROM)
MOS
BIPOLAR
MICROPROCESSORS
4-bit
8-bit
16-bit
16-bit plus
32-bit
MOS
8-bit
BIPOLAR

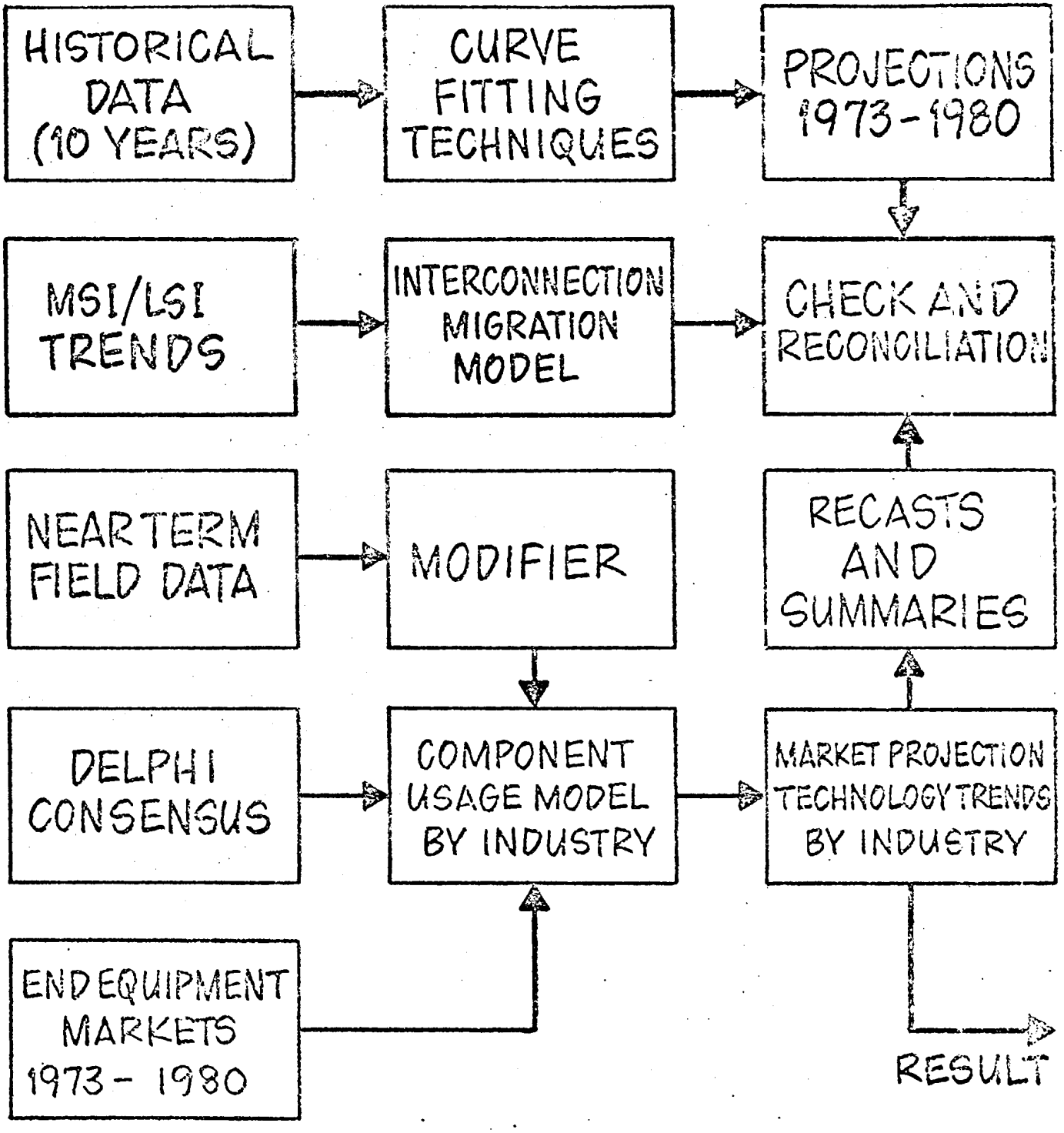
D&A
1974

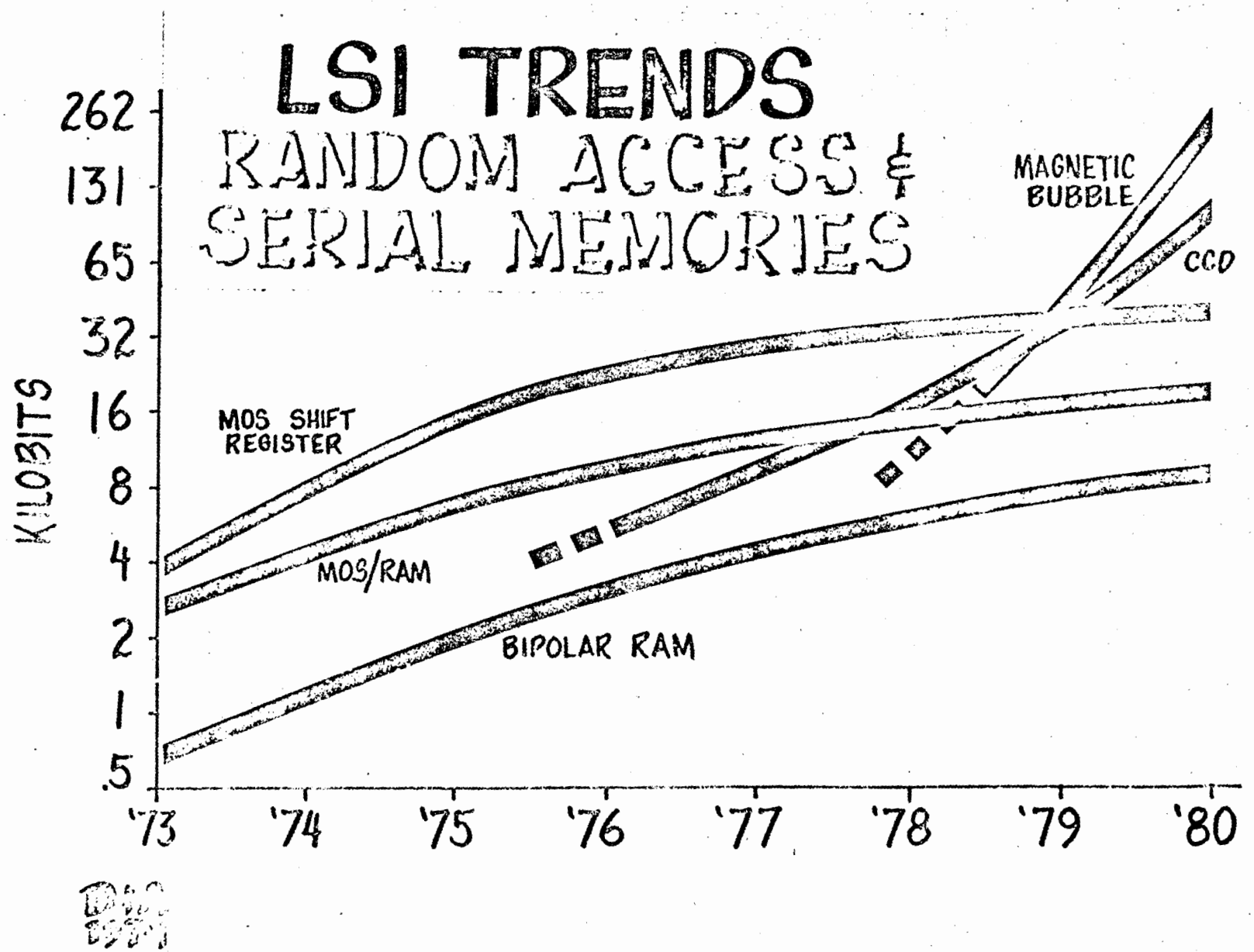
COMPARISON of DISTRIBUTIONS



DLA
1979

FORECAST METHODOLOGY




LSI TRENDS
RANDOM ACCESS &
SERIAL MEMORIES
KILOBITS
262
131
65
32
16
8
4
2
1
.5
'73
'74
'75
'76
'77
'78
'79
'80
MOS SHIFT REGISTER
MOS/RAM
BIPOLAR RAM
MAGNETIC BUBBLE
CCD

PACKAGING LEVELS

LEVEL 0 — Metalization on the Chip

LEVEL 1 — IC Package • Ceramic Substrate
• Lead Frame • Thin or Thick Film

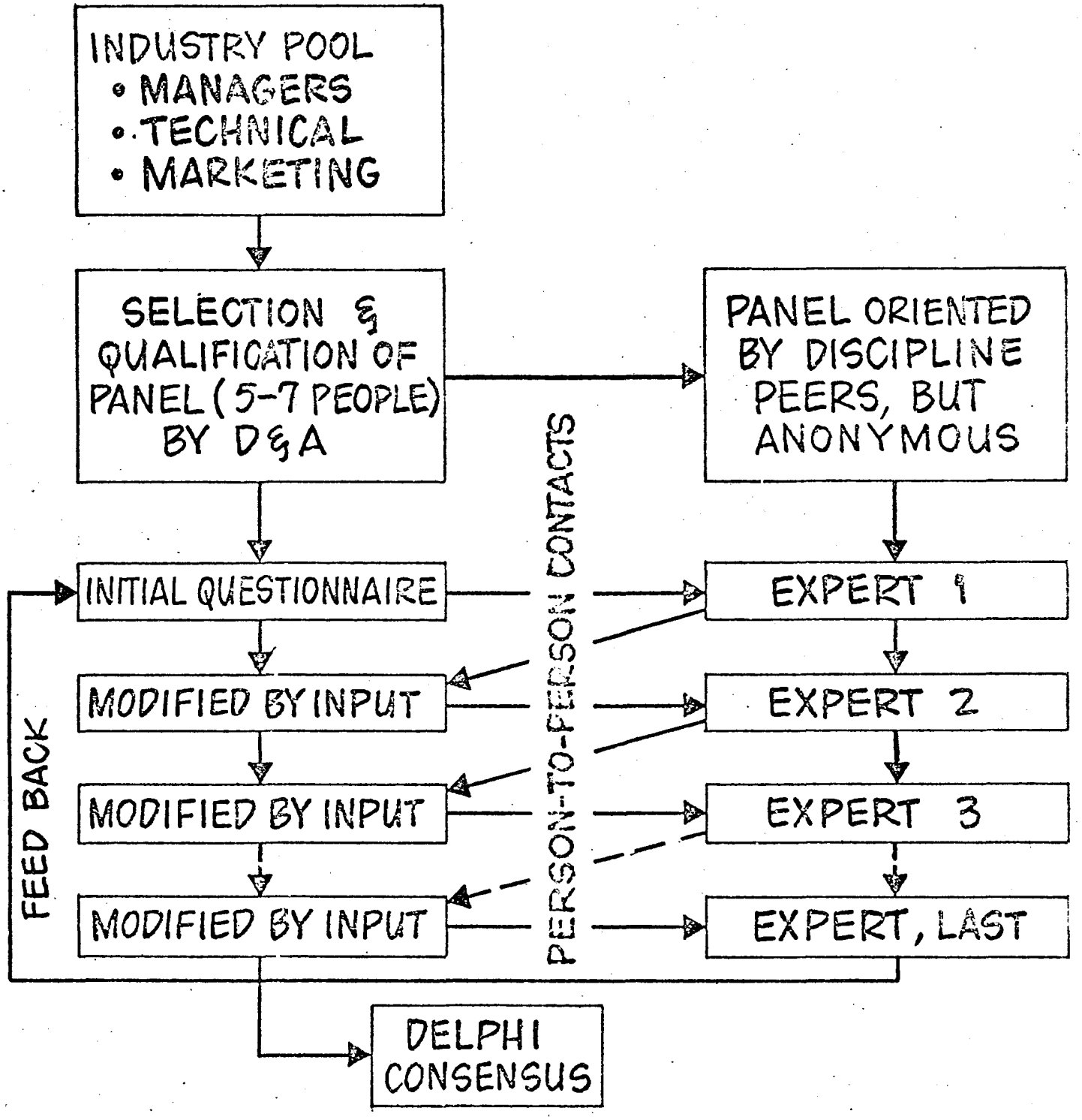
LEVEL 2 — Printed Circuit Board • IC Socket
• Flexible Circuit

LEVEL 3 — Motherboard • Backplane
• Wire Wrap™ • Socket Board

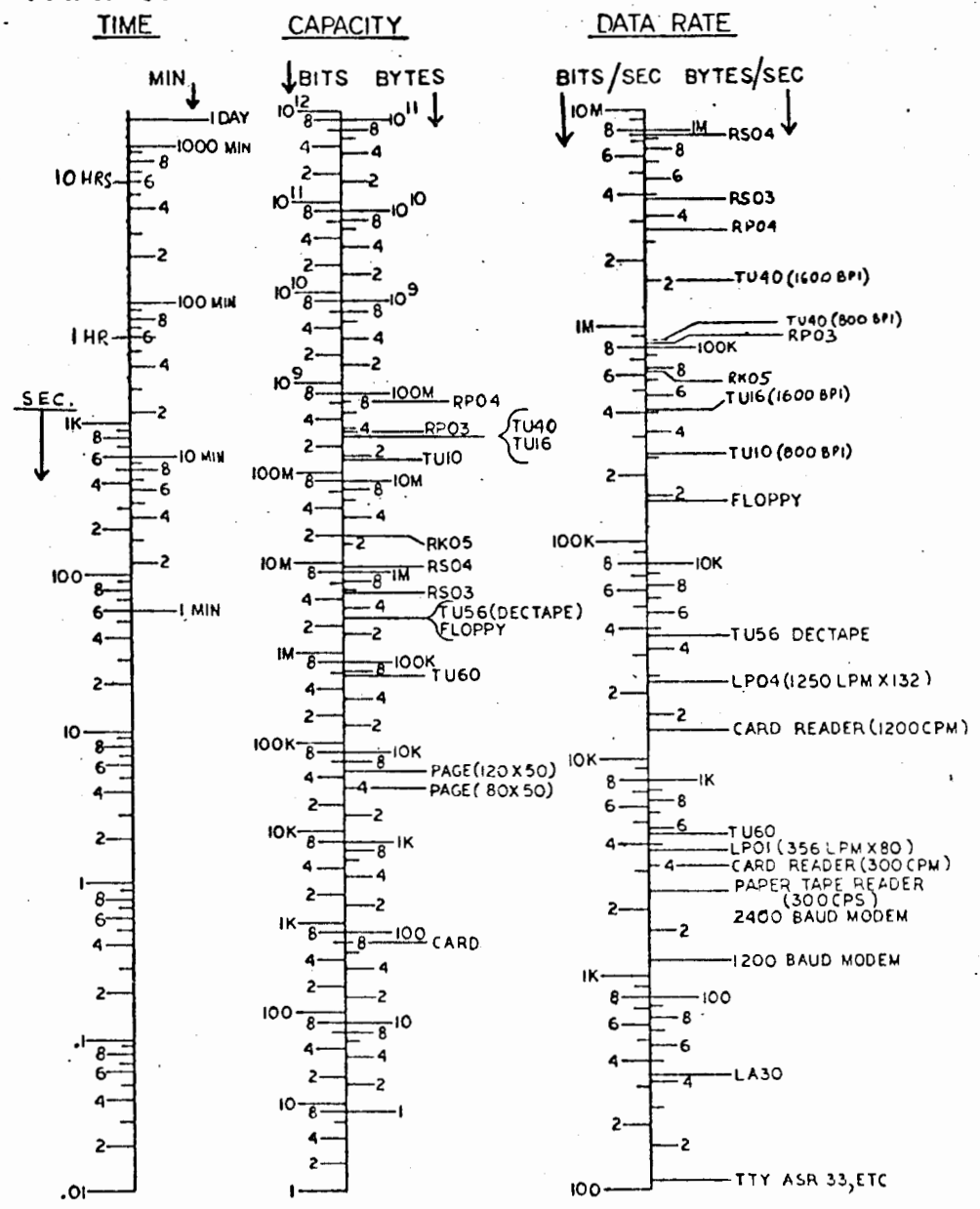
LEVEL 4 — Connector • External Cable

D&A
1974

DELPHI TECHNIQUE
AS MODIFIED BY D&A



DATA TRANSFER TIME BETWEEN DIFFERENT MEDIA



NOTES:

1. Products are marked at average data rate.
2. Average data rate (disks) = $\frac{\text{Formatted Track Capacity}}{\text{Access Time to Index + Rotation Time}}$
3. Average data rate (rest of divices) = Nominal Data Rate x $\frac{\text{Length of Data Field}}{\text{Length of Block}}$

   (Block includes, as appropriate, gaps, header, CRC, head and bottom of page, margin etc.
4. Tape block sizes:
   - TU10 & TU16 - 1024 (16 bit) words
   - TU40 - 4096 (36 bit) words
   - TU56 & TU60 - 256 (16 bit) words

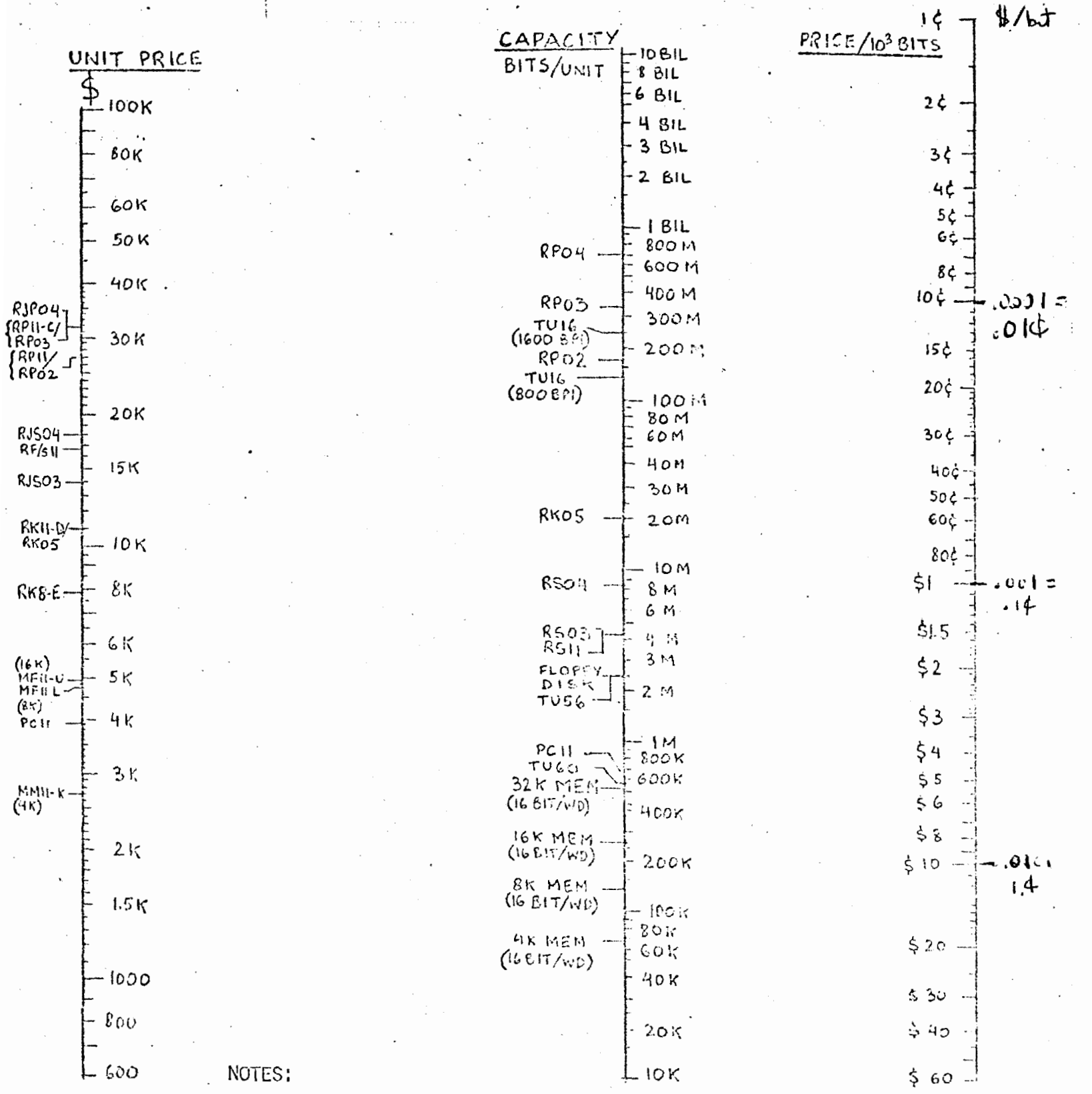
   Data rates for small blocks:
   - TU10 - 256 (16 bit wds) - 160kbit/s
   - TU16 - 256 (16 bit wds) - 224kbit/s
   - TU40 (1600bpl) - 256 (36 bit wds)- 1.06Mbit/s

HOW TO USE:

Example: to determine time to transfer the contents of RK05 cartridge to TU16 tape reel, locate TU16 on "data rate" scale and RK05 on "capacity" scale. Extend straight line between them to "time" scale. Time to transfer data about 4.2 seconds (excluding disk and tape mounting time.)

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

DATA STORAGE COSTS



NOTES:

1. ALL UNIT PRICES SHOWN INCLUDE 1 STORAGE MODULE (E.G. DISK DRIVE) + INTERFACE TO I/O BUS (E.G. CONTROLLER).
2. CAPACITY OF UNITS SHOWN ARE FORMATTED.
3. PRICE SCALE IS ON A BASIS OF 1000 BITS

A. SHARON 12/79

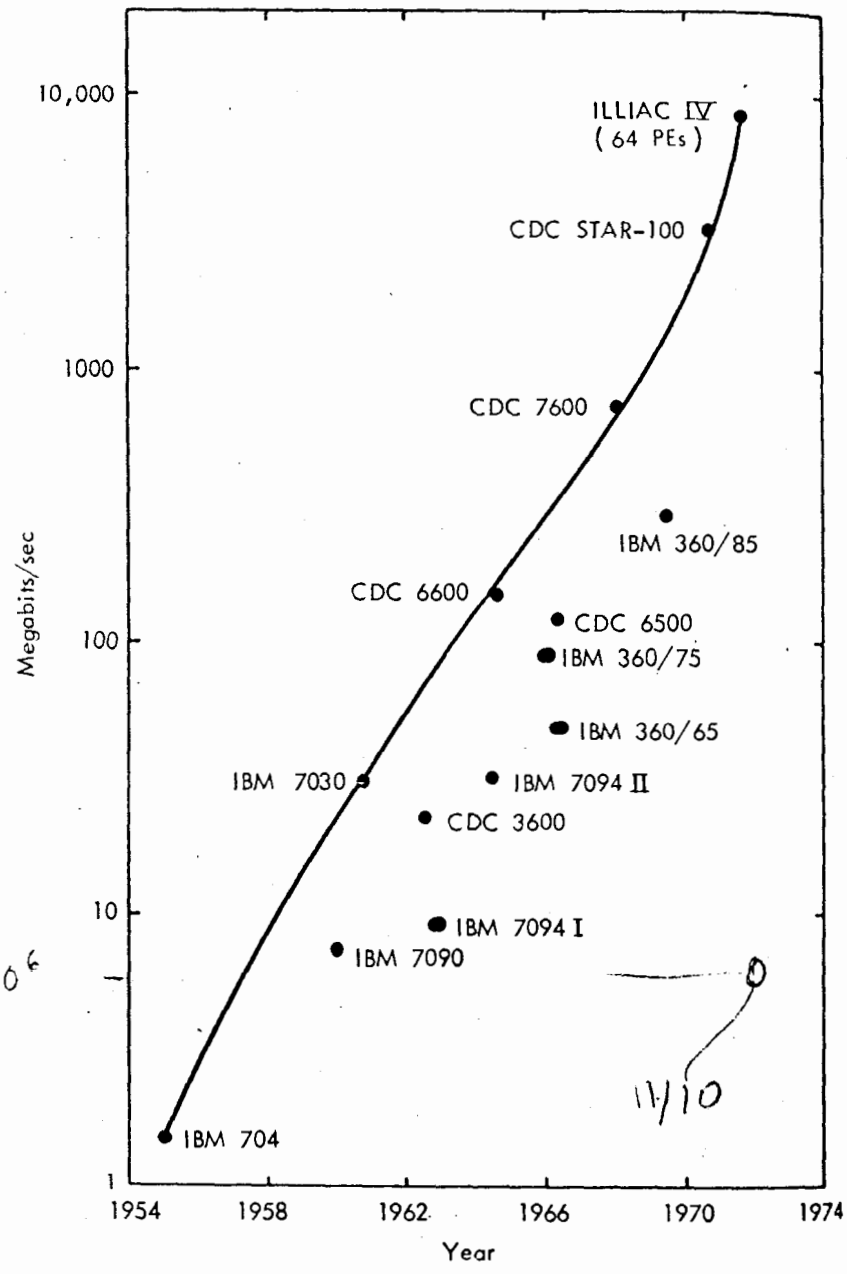


FIGURE 2. DATA-PROCESSING RATES FOR GENERAL-APPLICATION COMPUTE

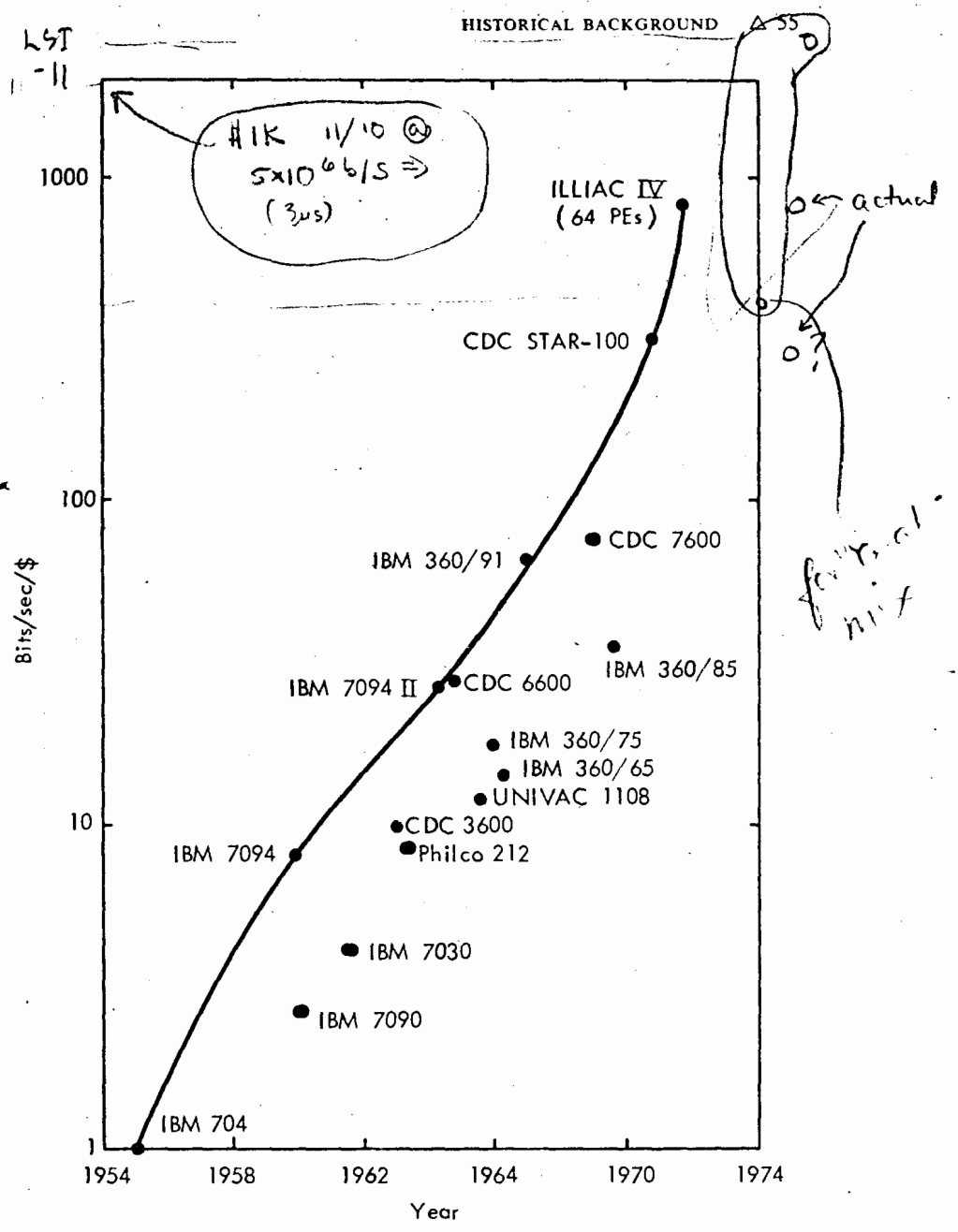


FIGURE 3. COST EFFECTIVENESS OF GENERAL-APPLICATION COMPUTER HARDWARE.

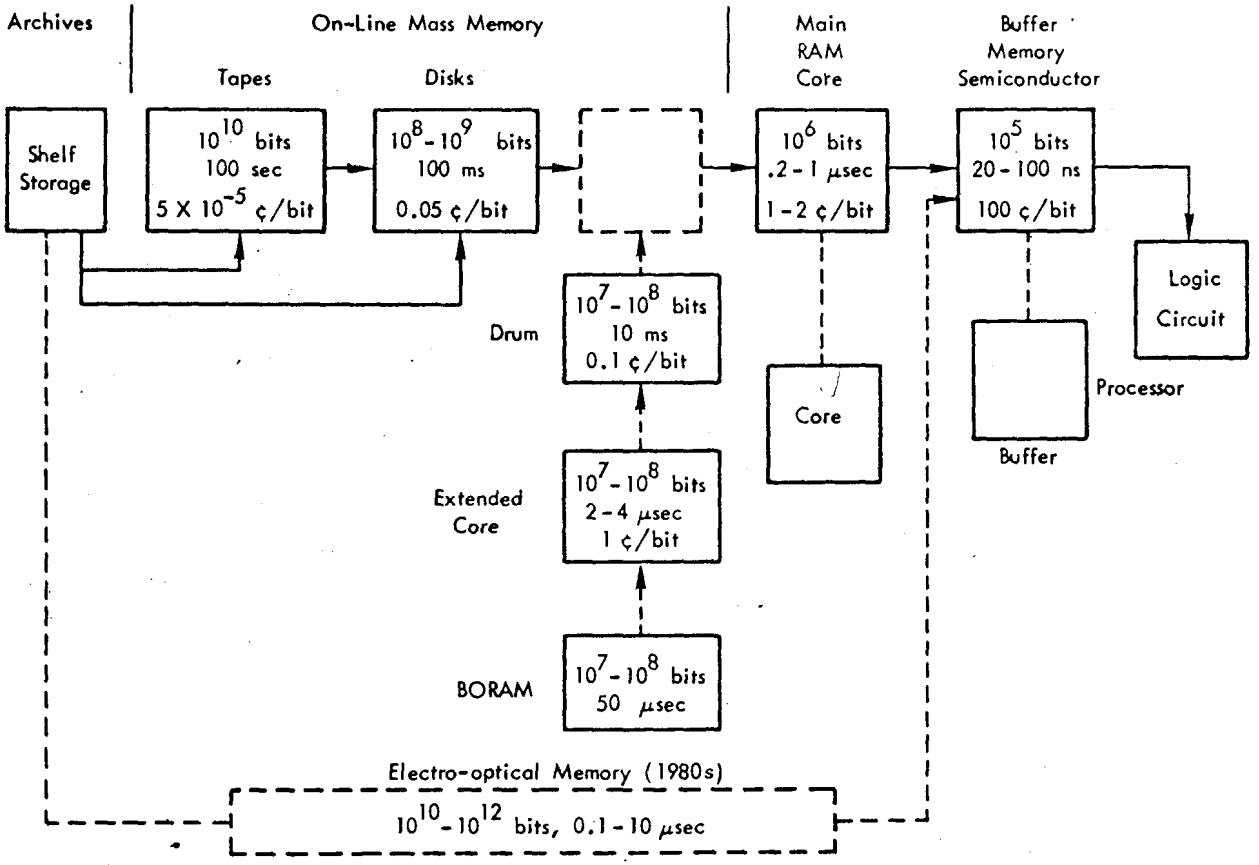


FIGURE 4. TYPICAL MEMORY HIERARCHY, 1971–1975.

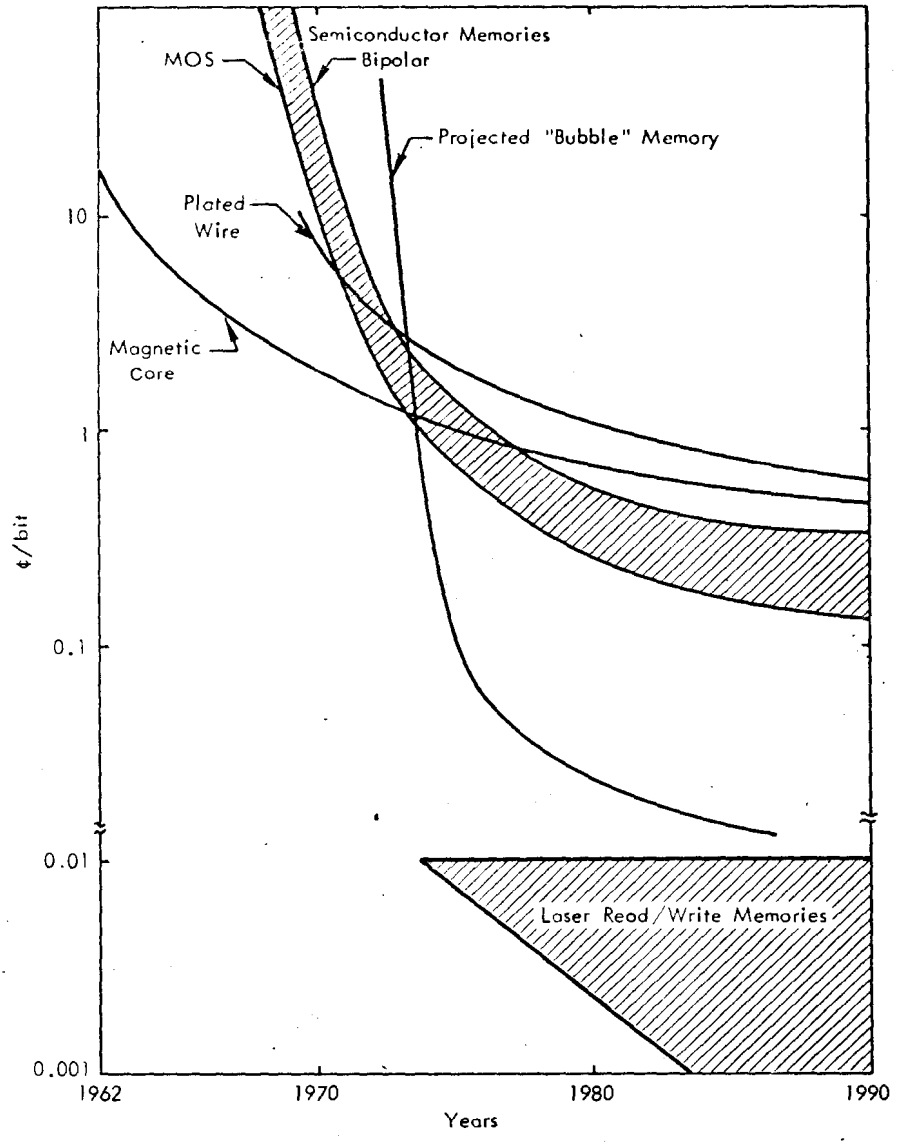


FIGURE 5. PROJECTIONS OF RANDOM-ACCESS MEMORY COST.

Projections of the memory capacity, cycle time, and cost into the 1980s are summarized in Tables 3 and 4 and in Figure 5. The supporting analyses are presented in Chapter IX.

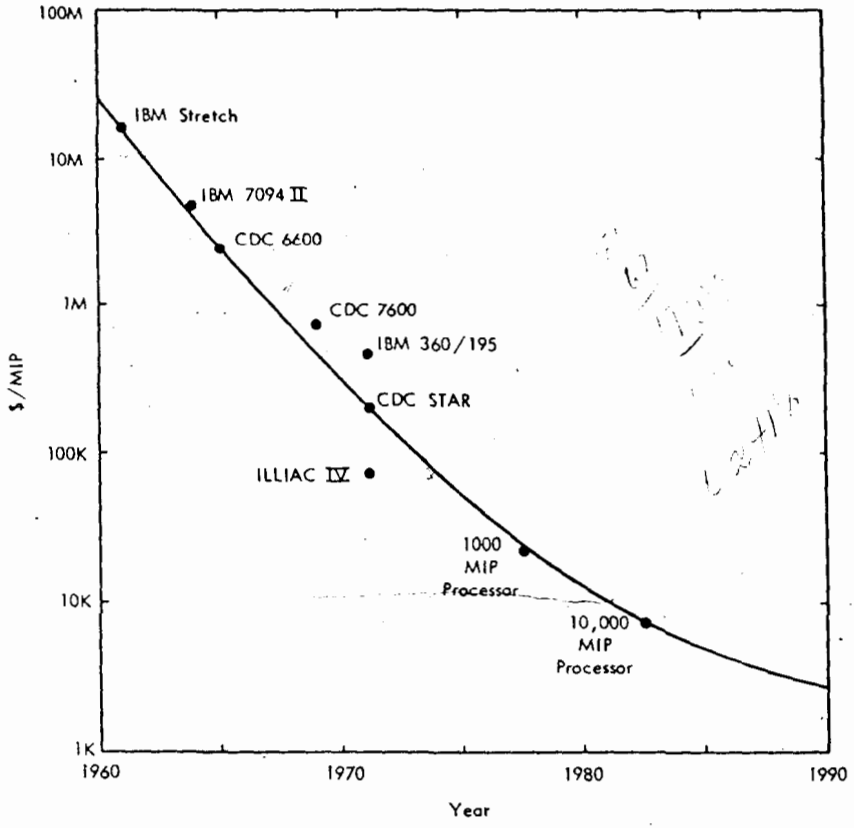


FIGURE 8. COST PROJECTIONS FOR HIGH-PERFORMANCE GENERAL-APPLICATION COMPUTERS.

lining features of future systems will be driven and controlled by software. In many instances these additional software burdens can be avoided through hardware implementation in the architectural design. An example is the IBM 360/195 pipeline computer in which hardware implementation has significantly reduced the software requirements because the pipeline characteristics are transparent to the user.

ARRAY PROCESSOR

An array processor (parallel processor) is characterized by a single instruction stream and multiple data streams. The principal features are:

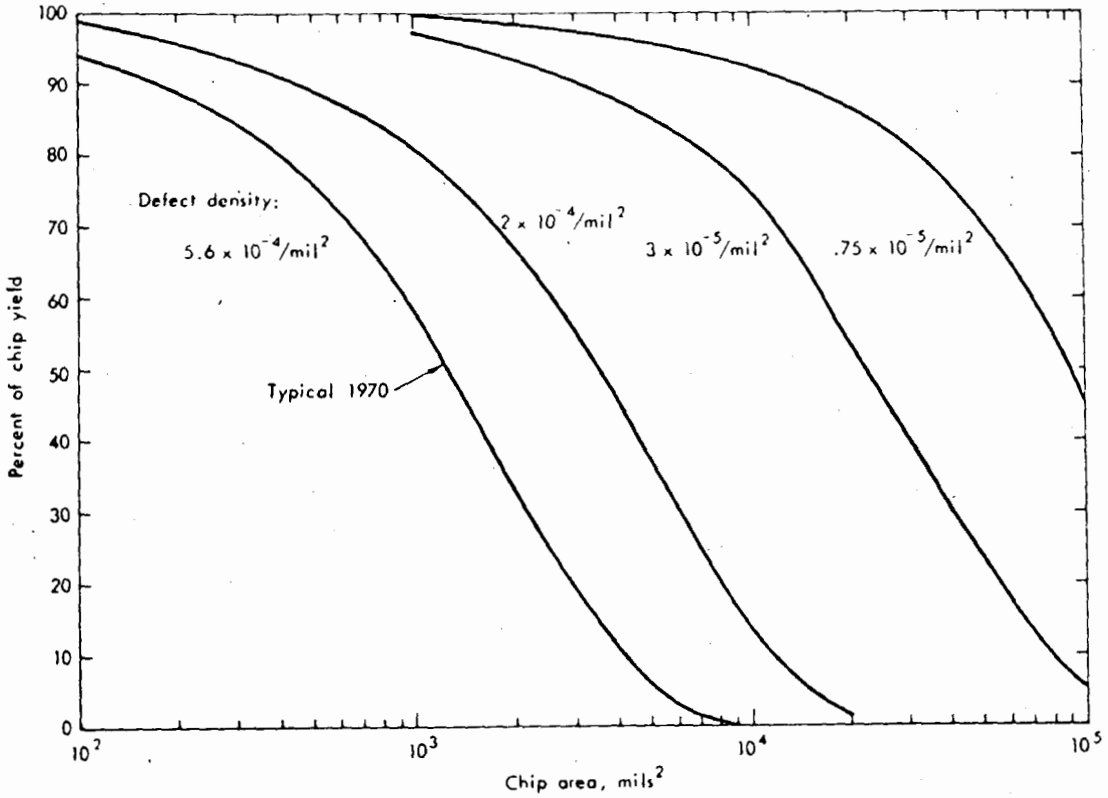


FIGURE 22. EXPECTED CHIP YIELDS VS. CHIP AREA SYSTEMS.

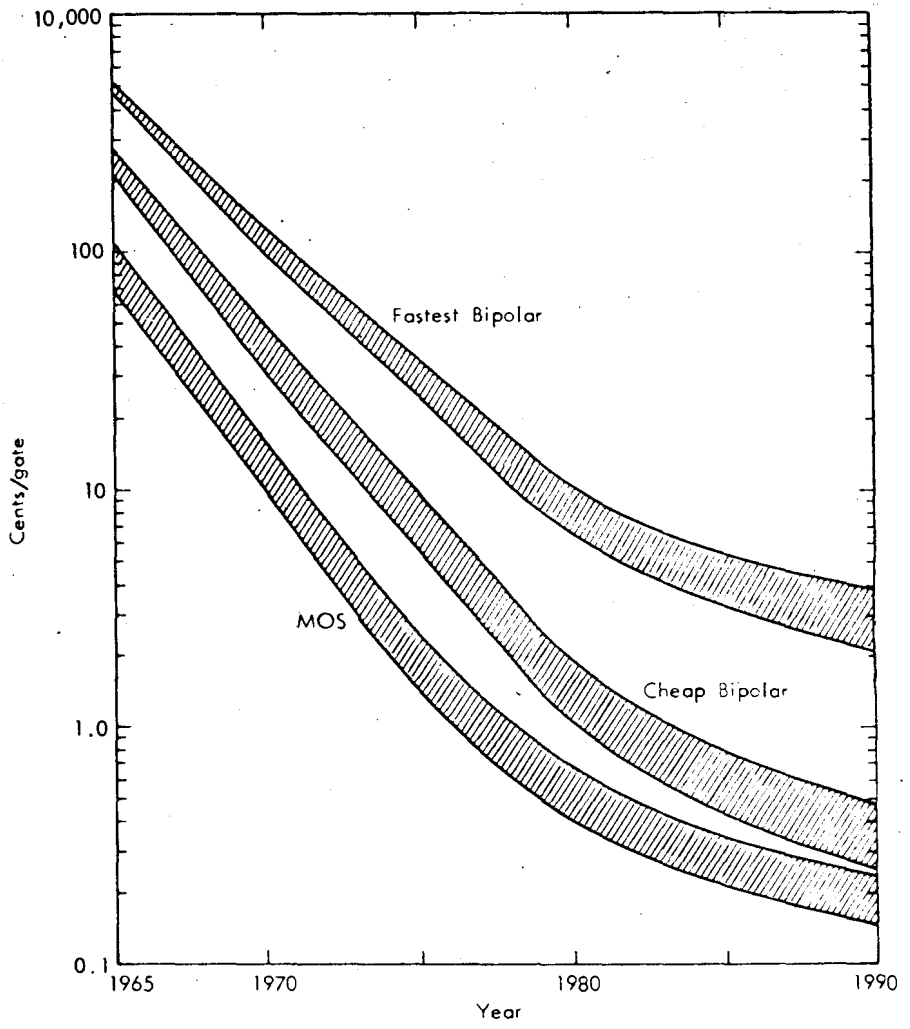


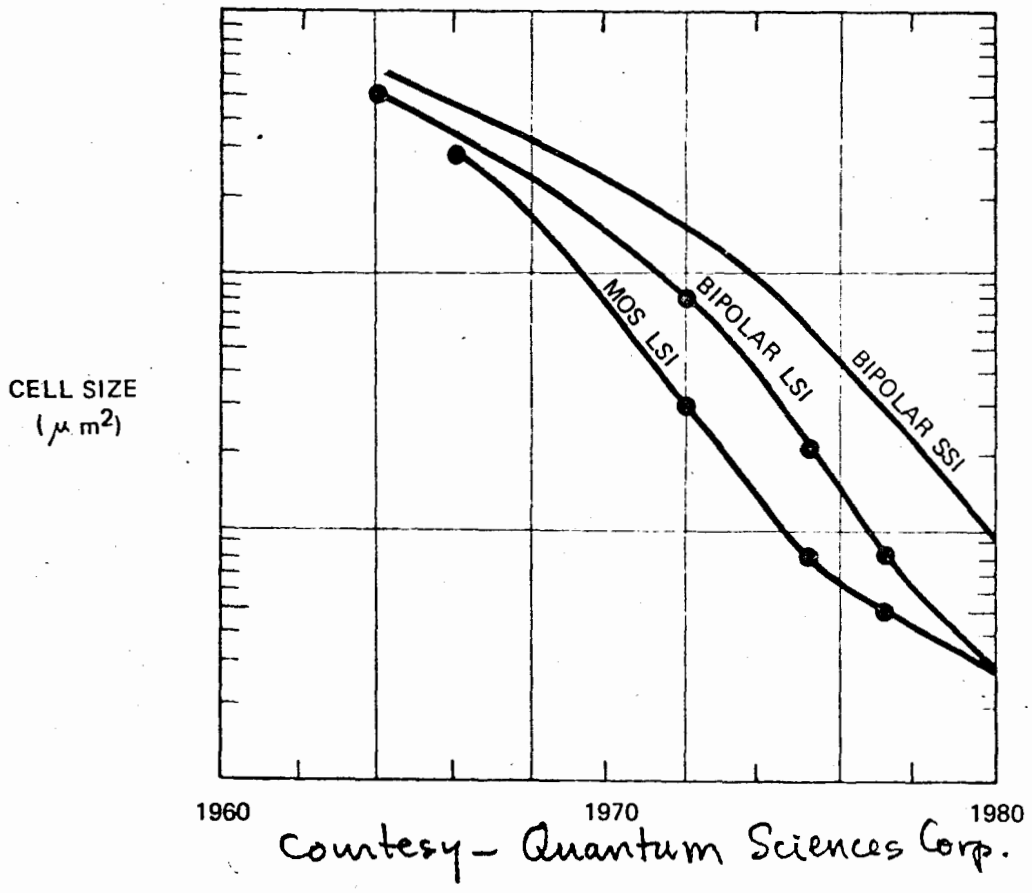
FIGURE 23. PROJECTED COSTS OF SEMICONDUCTOR LOGIC CIRCUITS.

the relatively benign operating environments associated with general-purpose commercial computers. The custom-designed logic circuits that may be required for CC computer applications are likely to cost much more.

Bipolar Transistors. A bipolar transistor is the "conventional" transistor, manufactured of silicon or germanium crystalline material, whose

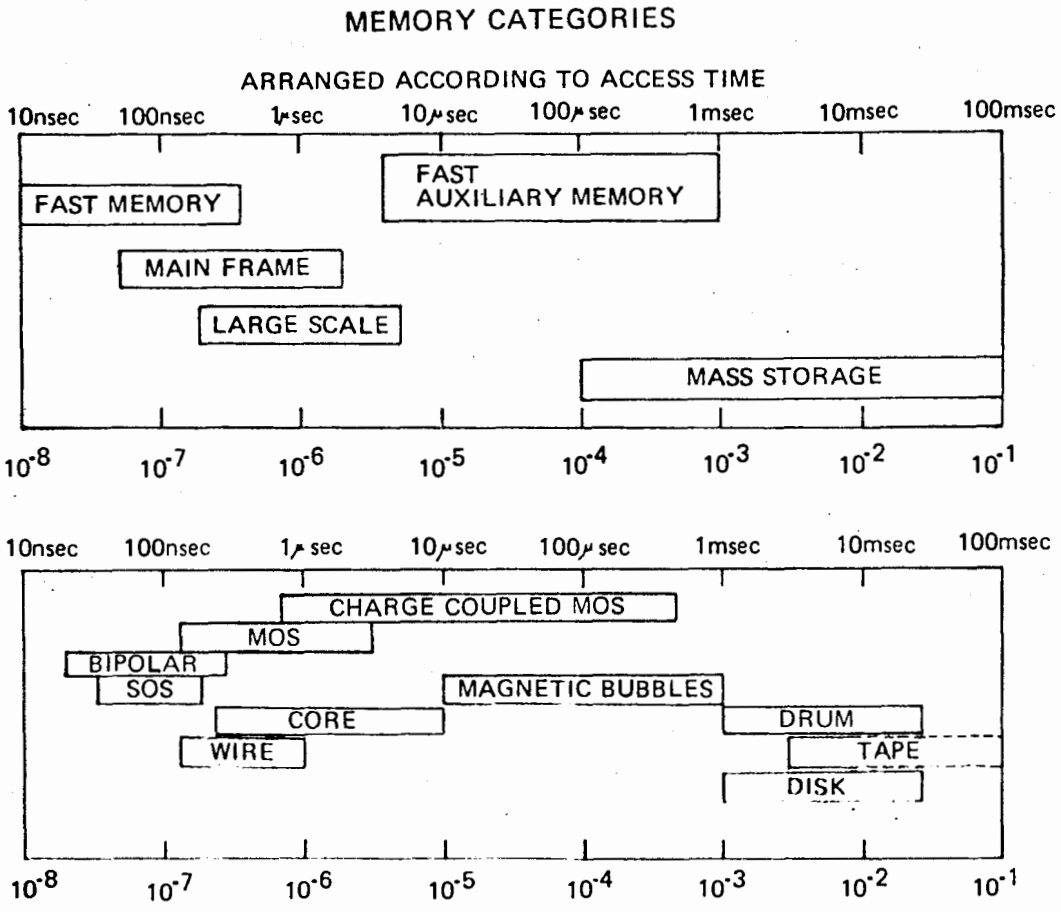
FIGURE 9

IC TECHNOLOGY DEVELOPMENT



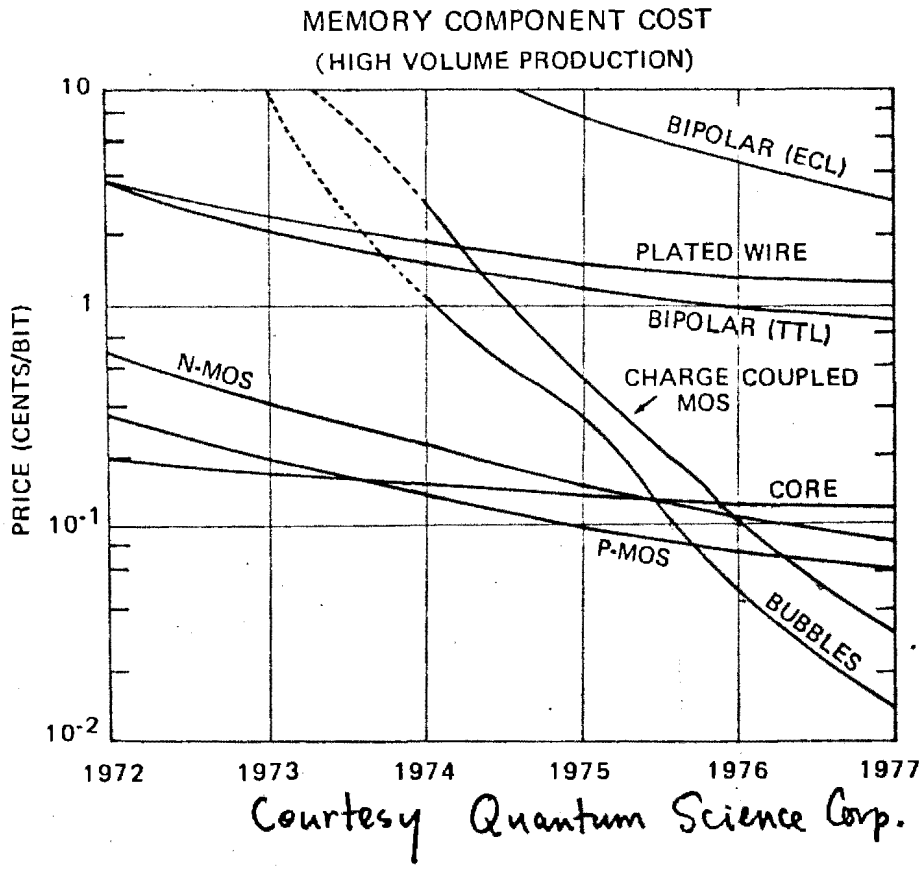
Courtesy – Quantum Sciences Corp.

FIGURE 12



Courtesy Quantum - Science Corp.

FIGURE 13



Courtesy Quantum Science Corp.

FIGURE 14

SPEED–DENSITY RELATIONSHIP OF LSI TECHNOLOGIES

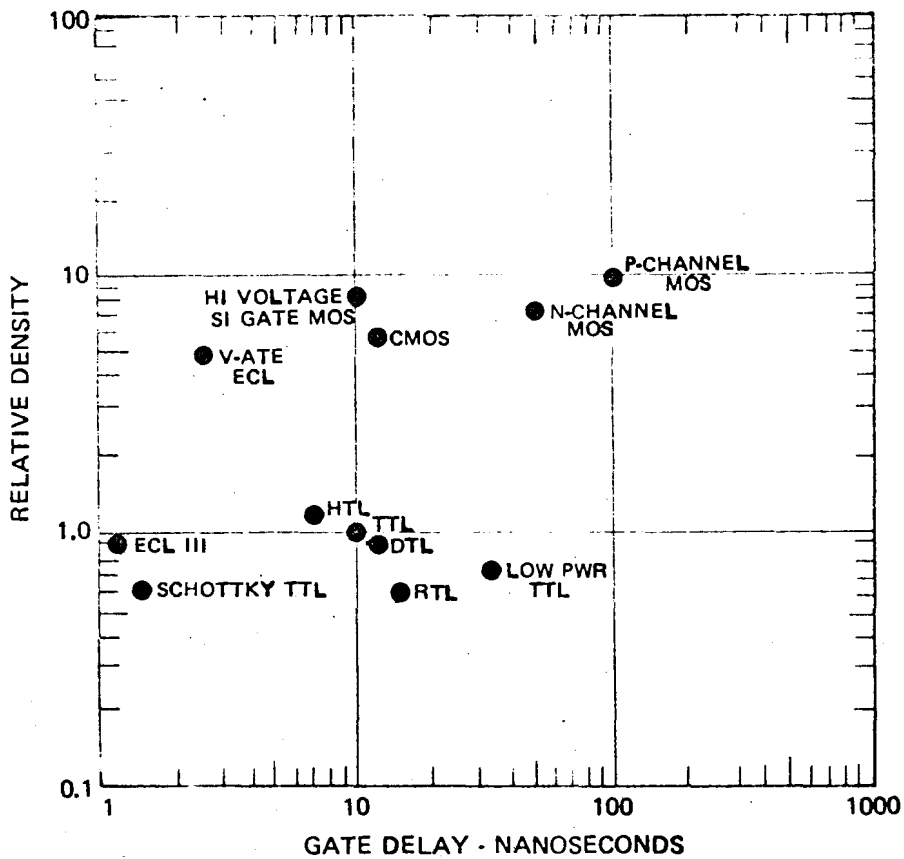
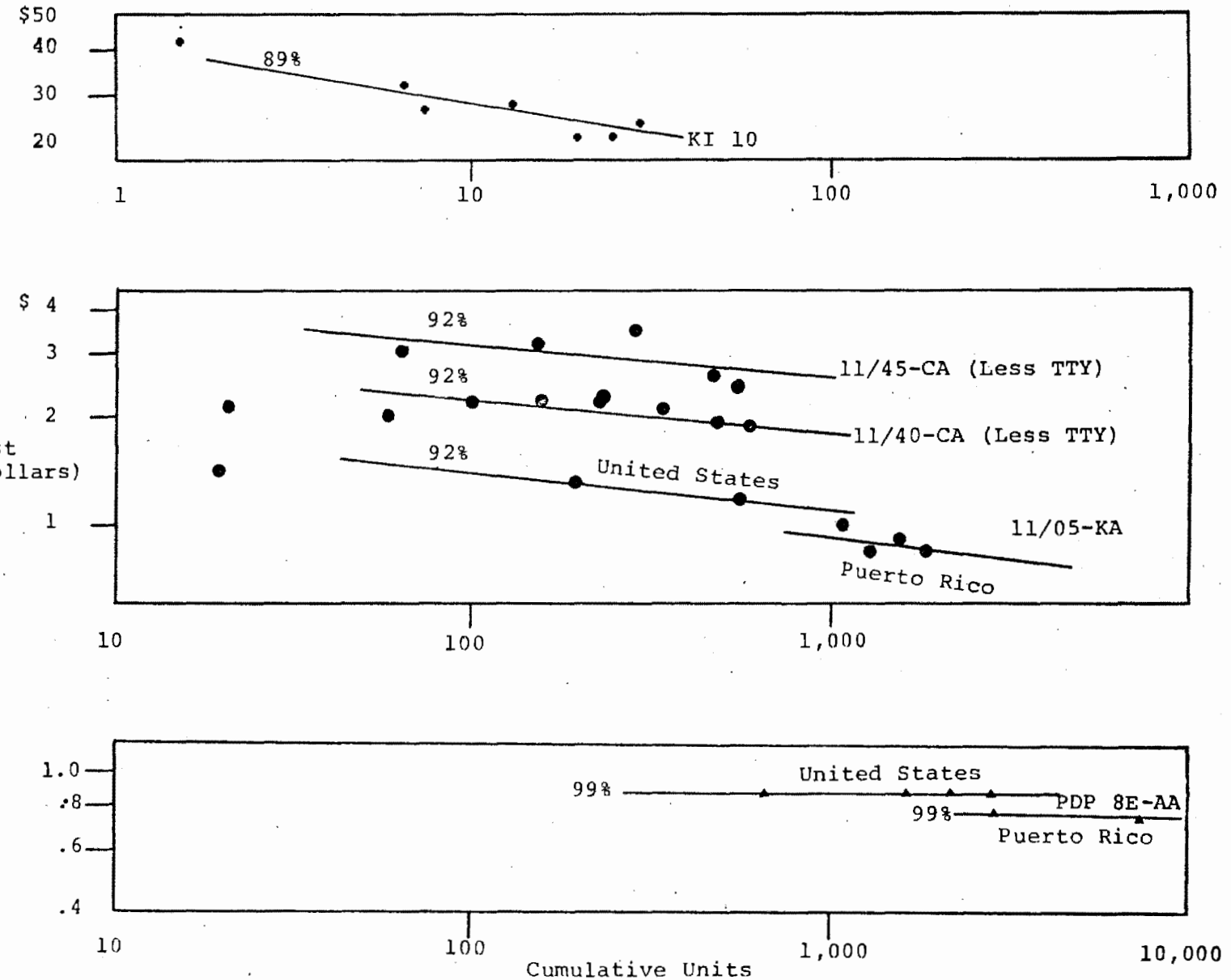


EXHIBIT 1

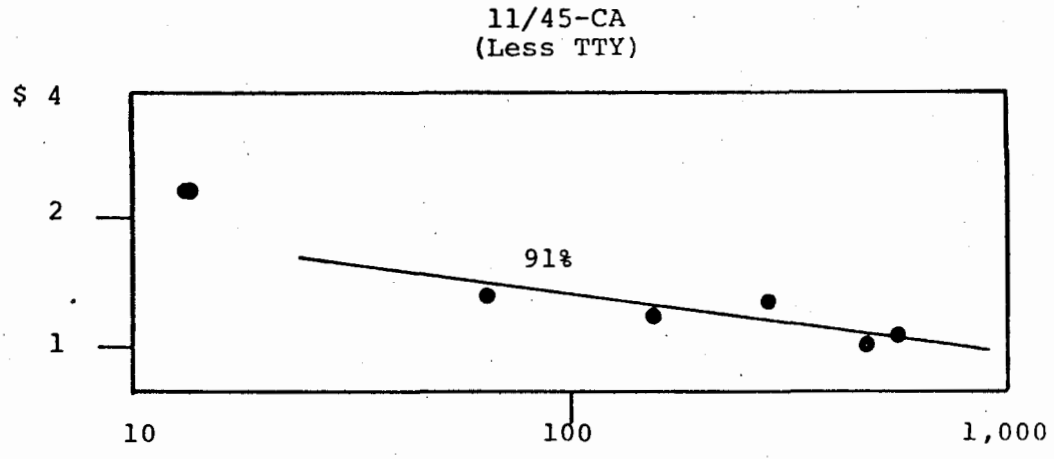
CPUs
VALUE ADDED



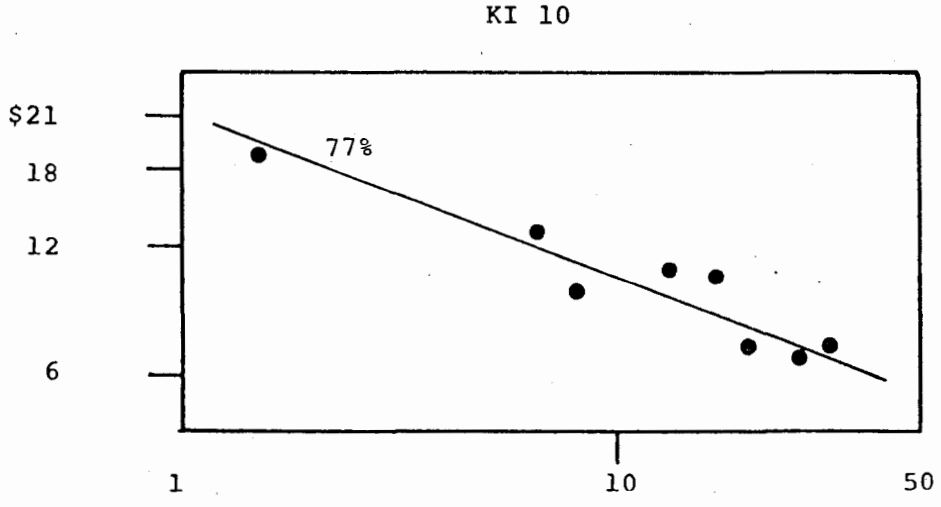
Source: Pink Book Data

EXHIBIT 3

PRODUCT SPECIFIC COSTS



Unit Cost
(Thousand Dollars)

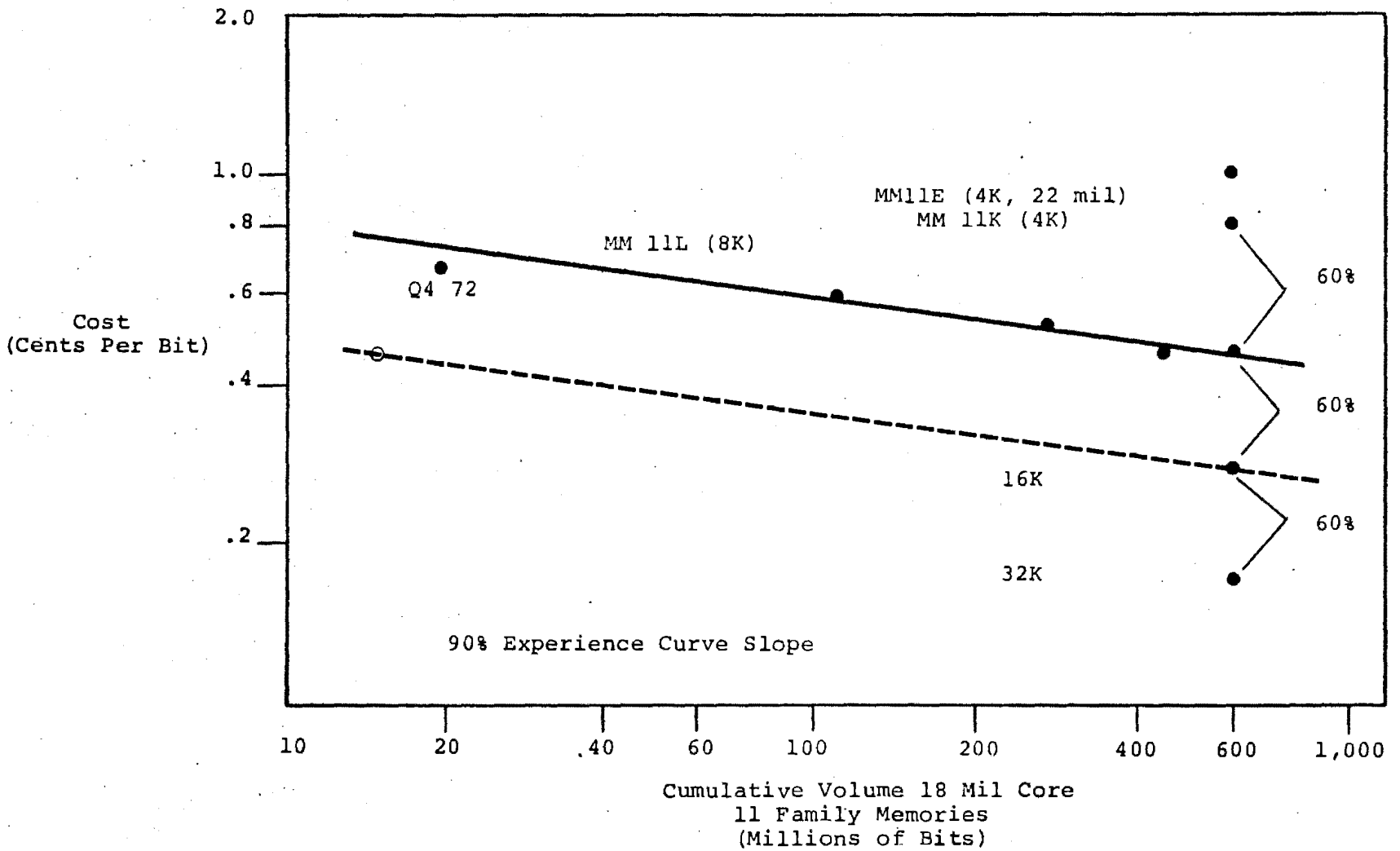


Cumulative Units

Source: Pink Book Data

EXHIBIT 9

MEMORY TECHNOLOGY AND COSTS



Source: Pink Book Data and estimates from Phil Laut

CATEGORY - (1.) PATTERN RECOGNITION EQUIPMENT

EVENT	Goal	Desirability	Feasibility	Timing
a. Optical character reading (OCR) will accelerate the phasing out of key-punched data inputs.	S	7	7	72 / 74 / 77
b. Page readers will replace key-punching for data input in conjunction with magnetic tape recorders.	N/A	5	7	72 / 74 / 77
c. Faster and more reliable document readers will be available at 10,000 characters per second.	N/A	5	5	72 / 77 / 81
d. Techniques for computer reading of print and handwritten print will have been developed. No current or envisaged system is adequate.	N/A	5	3	72 / 75 / 85
e. Computer recognition of 3-D objects will permit automatic processing and understanding of photos, TV and motion picture film.	N/A	5	5	74 / 80 / 90
f. Optical character readers capable of automatically reading multifont characters (i.e., greater than 20 fonts) will be available.	N/A	5	9	72 / 74 / 77
g. Commercially available pattern recognition equipment for input of graphic data (bar charts, diagrams, etc.).	M	5	5	75 / 80 / 85
h. Low cost OCR reader (less than $20,000).	S	8	8	70 / 72 / 74
i. Pattern reader used commercially in medical field analysis (hospitals).	N/A	9	9	71 / 73 / 75
j. Pattern reader for recognition of spoken words with limited vocabulary.	N/A	5	5	74 / 80 / 90
k. Pattern reader for recognition of spoken words with little vocabulary limitations.	N/A	5	2	80 / 85 / 95
l. Remote scanning will be commercially available.	S	8	8	70 / 71 / 72
m. OCR will be a major technique for the transmission of digital data.	N/A	5	8	72 / 74 / 76
n. Adaptive recognition techniques will be implemented into the pattern recognition equipment.	N/A	5	5	78 / 81

CATEGORY - 1. PATTERN RECOGNITION EQUIPMENT (Cont'd.)

	EVENT	Goal	Desirability	Feasibility	Timing
o.	Some form of computer voice input will be available.	M	5	5	74 80 85
p.	OCR will play an active role in the computer storage of present documentation files for library, books, journals, abstracts, files, indices, etc.	S	8	8	72 74 78
q.	Reading of U. S. mail will be basically by OCR (Zip code and address).	L	8	8	80 85 90
r.	On-line interpretation of reconnaissance photographic data.	M	8	8	75 80 85
s.	Techniques for reading of script will have been developed.	N/A	5	5	77 79 80 84
t.	Techniques for reliable reading of printed alphanumeric characters will have been developed.	N/A	8	8	70 72 75
u.	Very reliable OCR equipment capable of reading hand printed numerics will be developed.	N/A	8	8	72 74 76
v.	Moderately slow low-cost OCR transmittal equipment will be developed.	N/A	8	8	69 71 73
w.	A larger selection of reliable multifont OCR equipment will become available.	N/A	5	8	73 76 79
x.	Faster (2,000 documents/min.) small document readers with sorting capabilities will be developed.	N/A	5	5	70 73 75
y.	Techniques for machine reading of general print will have been developed (for books, newspapers, etc.)	M	7	8	72 75 95
z.	Techniques for machine reading of script will have been developed. (Requires memories of very large capacity for storing of context.)	L	7	5	75 80 2000
aa.	Optical page readers will use spelling, grammar, and context to check individual characters.	N/A	8	8	71 75 80

CATEGORY - PATTERN RECOGNITION EQUIPMENT (Cont'd.)

EVENT	Goal	Desirability	Feasibility	Timing
bb. Recognition of line drawings and perhaps more sophisticated input material will be possible.	N/A	5	5	80 — 85 — 90
cc. Personal characteristics such as fingerprints, facial features, etc. will be useful for identification.	N/A	5	5	85 — 90 — 2000
dd. Techniques for on-line handprint and script entry using graphic input devices and small (less than $10 K) computers with simple programs will be available.	S	5	5	69 — 70 — 75
ee. Speech recognition devices capable of recognizing dozens of speakers using the systems.	N/A	6	5	73 — 77 — 83
ff. Reception and encoding of spoken data limited to data identifiers and numerical data will be possible.	N/A	6	5	70 — 75 — 80
gg. For spoken input, computers will identify a few tens of words.	N/A	5	6	70 — 75 — 80
hh. For spoken input, computer vocabulary will be many hundreds of words, and computer will interpret simple sentences.	S	9	5	70 — 72 — 75
ii. Computer will use for both spoken input and audio output the extent of vocabulary and the idiomatic usage as does an educated person.	L	7	3	75 — 80 — 2000
jj. Spoken reply to digital input.	N/A	5	7	68 — 70 — 72
kk. Spoken input will be recoded and reconstituted for verification.	N/A	5	5	70 — 74 — 78
ll. Natural syntax and symbols including motion pictures will be accepted, but not recognized, by computers.	L	5	3	76 — 82 — 90
mm. Some form of voice input and output will be in common use.	S	9	4	71 — 74 — 78
nn. Need for facsimile and OCR (Optical Character Readers) may be eliminated by use of dual-mode documents containing both digital, machine-readable, high density codes and conventional man-readable printing.	N/A	2	6	71 — 73 — 77

CATEGORY - 4. DATA COMMUNICATIONS EQUIPMENT

EVENT	Goal	Desirability	Feasibility	Timing
a. "Smart" terminals will be developed to permit most of the computing and processing to be done in the terminal (going over a communications line to a larger computer only when necessary) to minimize communications costs.	N/A	8	8	68 — 69 — 70
b. Teleprinters will substantially replace line printers.	N/A	6	7	73 — 75 — 80
c. Teleprinters will commonly be supplanted by CRT's (cathode ray tubes).	N/A	2	7	72 — 75 — 80
d. Practical application of optical electronic communication and computer equipment will be feasible.	N/A	5	5	73 — 78 — 85
e. I/O data communication terminals will become more versatile at higher speeds and lower costs by sharing common control electronics within geographical clusters.	S	6	6	71 — 73 — 76
f. Automated circuit switch control of private data networks.	N/A	8	8	68 — 70 — 72
g. Interconnection of private and public switched voiceband networks.	S	5	6	70 — 71 — 73
h. Small scale computer time-sharing systems operating within each major local dial area will become common to avoid toll charges for transmission between terminals and computer.	N/A	8	8	69 — 71 — 73
i. Increased multiple processing capabilities of computers will permit general purpose computers to perform message collection, editing and forwarding on a part-time basis.	N/A	5	8	70 — 73 — 75
j. Modem speeds of:				
(1) 7200 bps data transmission reliably performed on voice grade (nominal 3kHz) lines.	S	7	8	69 — 70 — 72
(2) 9600 bps data transmission reliably performed on voice grade lines.	S	6	5	69 — 71 — 73
(3) 12,000 bps data transmission reliably performed on voice grade lines.	S	6	5	71 — 72 — 75

CALL... Y - 5. GRAPHIC DATA SYSTEMS AND DEVICES (Cont'd.)

EVENT	Goal	Desirability	Feasibility	Timing
l. An inespensive alphanumeric terminal (with limited graphic capability) will revolutionize this field at about $1K per terminal.	M	8	6	72 — 75 — 78
m. Standard television sets will come into substantial use as I/O terminals.	S	8	8	70 — 72 — 75
n. Development of low-cost, high-resolution, direct view storage CRT.	N/A	8	7	70 — 72 — 74
o. Development of low-cost scan converters.	N/A	7	6	70 — 73 — 75
p. Development of solid-state X-Y-Z displays of integral memory..	N/A	5	6	72 — 74 — 76
q. A solid state, thin, large screen display device will be in general use as a TV display.	L	5	4	75 — 83 — 90
r. A solid state vidicon will be available.	N/A	8	6	69 — 70 — 71
s. A 3-color vidicon will be available, leading to relatively inexpensive color cameras.	N/A	8	7	71 — 72 — 75
t. Inexpensive, high sensitivity vidicons for low light level applications will be available.	N/A	5	8	70 — 72 — 75
u. Electron beam recording devices will be available.	N/A	7	7	69 — 72 — 75
v. Page-size, dry-process hard copy CRT output device will be available.	S	9	8	69 — 71 — 73
w. TV-raster I/O devices will be a replacement for many direct CRT displays because of capability for accepting both digital and video (background data from optical storage) inputs.	S	6	7	70 — 72 — 73
x. Non-electromechanical, hard copy X-Y recording equipment for use as an analog or digital computer peripheral equipment with the following general characteristics:	M	5	5	74 — 76 — 80
Large screen (plotting areas of up to 6' x 10') High speed (writing speeds of 100 inches/sec or greater) High accuracy (0.05% to 0.005% of full scale)				

CATEGORY - 5. GRAPHIC DATA SYSTEMS AND DEVICES (Cont'd.)

EVENT	Goal	Desirability	Feasibility	Timing
hh. A color display, 1024 x 1024 resolution, low cost-$1-10K including storage, will be available.	S	9	5	70 / 71 / 73
ii. A hardware display generator which can draw curves, lines, points, and characters with edge clipping, fast and accurately will be available at a low cost ($1-5K).	N/A	8	5	69 / 70 / 73
jj. A hardware picture generator which can generate a raster scan in color given the specifications of all the homogeneous areas will be available.	N/A	8	5	70 / 72 / 74
kk. LSI technology will permit the inclusion of many special purpose processing functions in display generators thus saving central machine time (e.g., 3-D transformations).	N/A	5	8	70 / 72 / 74
ll. The plasma panel will be perfected to provide a low cost, flat, easily driven, high resolution color display with selective write, intensity storage and read-out capacity.	N/A	5	8	69 / 70 / 72
mm. High resolution (750-1000 line) TV refreshed from an analog or digital mass storage device (e.g., disc) either in clusters or individually will provide low cost, high performance graphics consoles.	N/A	5	8	69 / 70 / 72
nn. Wall displays 4' to 12' square with resolution of at least 40 lines/inch and color will be feasible. 40 x 48 1440	N/A	8	5	71 / 73 / 75
oo. Development of flat panel, digitally addressed displays with inherent storage and selective erasure.	N/A	8	7	69 / 70 / 72
pp. Development of dynamic real-time large screen displays.	S	8	5	70 / 72 / 74
qq. Development of low cost remote graphic terminals.	S	7	7	71 / 74 / 76
rr. Development of sophisticated man-machine interface consoles with high speed and high resolution graphic input and graphic output at reasonable cost for applications such as design automation.	N/A	9	9	69 / 70 / 72

CATEGORY - 5. GRAPHIC DATA SYSTEMS AND DEVICES (Cont'd.)

EVENT	Goal	Desirability	Feasibility	Timing
ss. Reliable high resolution opaque scanner with 4-times the resolution presently available.	N/A	5	5	70 — 72 — 75
tt. Holographic techniques may compete with and/or supersede the use of TV consoles for man/machine interface.	N/A	3	3	77 — 80 — 84
uu. Telephone couples soft copy capability can be commonly used for information retrieval and presented to the individual viewer.	N/A	5	6	73 — 75 — 75
vv. Personal terminals which "simulate" routine activities of employees in functional departments (e.g., personnel, contract administration, pricing, etc.) so as to increase productivity of administrative work.	N/A	8	8	70 — 72 — 75
ww. Graphics capabilities will assume tremendous importance.	S	5	8	69 — 72 — 75

CATEGORY - 6. MEMORY SYSTEMS AND MAGNETIC RECORDERS (Cont'd.)

	EVENT	Goal	Desirability	Feasibility	Timing
p.	Use of LSI for small CAM memories in computers.	S	5	7	69 / 70 / 72
q.	Majority or at least equal use of anisotropic permalloy memories (films, plated wire) for computer main frame memory.	N/A	5	6	73 / 75 / 80
r.	Widespread use of LSI for computer memories.	M	6	5	72 / 76 / 79
s.	Erasable mass storage units of 10^{10} bit capacity will have access times less than 10 milli-seconds and cost .1 millicent per bit.	M	9	5	73 / 76 / 79
t.	Erasable mass storage units of 10^{13} bits capacity will have access times of less than 1 sec. and cost less than .1 mill/bit.	N/A	6	5	74 / 77 / 80
u.	Methods for utilizing close to the theoretically maximum density of magnetic material will be found, in an economical, realiable system.	N/A	5	3	80 / 85 / 87
v.	Radical new memory structures which grow new paths when stimulated electrically will be in use.	N/A	5	5	78 / 83 / 90
w.	Main memory storage will average 100-300 NS for 4th generation computers.	N/A	7	7	71 / 74 / 76
x.	Scratch pad memories will average 100 NS for 4th generation computers.	N/A	7	7	71 / 73 / 75
y.	Submicrosecond core memories will be available of 10 million (10^7 bits), costing 2.5 to 3 cents/bit.	N/A	5	5	70 / 73 / 75
z.	Both planar thin film and plated wires will gain industry acceptance, but ferrite cores will continue as the primary main memory storage element for 5-6 years.	N/A	5	4	72 / 74 / 76
aa.	Holographic techniques will be utilized to store digital, or possibly even alpha-numeric information, as a main storage element in a computer.	N/A	8	5	70 / 73 / 75
bb.	Cost reductions on cores, plate and wire or thin film for main storage will make it possible to provide lots of fast storage capacity. This will simplify the software convolutions of "virtual memory" and "paging" and make time sharing more economic than now.	S	6	4	71 / 73 / 75

CATEGORY - 6. MEMORY SYSTEMS AND MAGNETIC RECORDERS (Cont'd.)

	EVENT	Goal	Desirability	Feasibility	Timing
cc.	High-speed ROM (Read Only Memory) Systems less than 100 nsec. cycle times	N/A	7	7	69 → 72, 70
dd.	Combined ROM and erasable memory systems in one physical unit sharing electronics.	N/A	5	5	68 → 69, 68
ee.	Large scale associative content addressable memory systems.	S	6	4	70 → 74, 72
ff.	Use of laser beam recording on magnetic media for wide band analogue and higher speed digital recording (50 megabit/sec.); increasing packing density by 10; reducing cost by a factor of 10; improving access time by a factor of 10.	N/A	7	4	71 → 75, 73
gg.	Use of magnetic film memory coupled to IC to produce high-speed, low power, low cost RAM.	N/A	5	5	71 → 78, 73
hh.	Use of optical techniques for CAM.	N/A	4	4	72 → 79, 76
ii.	On-line memories with very high data reliability, access time of 5_3 seconds, capacities in excess of 10^{12} bits and cost of less than 10^{-3} cents/bit.	N/A	9	8	69 → 72, 70
jj.	Semiconductor "cache" memories will extend the lifetime of ferrite core memories.	N/A	8	8	69 → 73, 71
kk.	Disc paks will take over a major portion of the magnetic tape market due to increased reliability and performance.	N/A	8	5	70 → 76, 73
ll.	Thin-film memories with cycle times of 250-400 NS will be available in stores of 10^5-10^6 bits.	N/A	6	4	69 → 71, 70
mm.	Major semiconductor suppliers will not enter the computer business with LSI CPU's and memories. They will recognize that main memory and control processor has tended to be a smaller and smaller portion of the total computer system as the history of the art develops. The software requirements will be considered too monumental.	N/A	5	5	70 → 75, 72

CATEGORY - 11. SOFTWARE

EVENT	Goal	Desirability	Feasibility	Timing
a. There will be a sequence of small languages relating small groups of people to machines, and groups of machines. This comment is based on the promise that, for example, there is no need to force physicists to talk the same language as biologists.	N/A	5	5	69 / 75 / 80
b. Compiler-compilers which will include front and back end languages (permitting code optimization) will be the normal technique for producing compilers.	N/A	5	5	69 / 71 / 73
c. Machine indexing of both textual and pictorial data.	N/A	5	4	72 / 76 / 80
d. Compilers will provide an object program as good as a hand-coded program	S	6	6	70 / 72 / 74
e. Programs will become more modular. Combinations of program packages can be made to solve specific problems.	N/A	5	5	72 / 74 / 77
f. Natural English language for file inquiry and updating.	N/A	8	4	74 / 76 / 85
g. A universal computer language will have evolved through automated communication.	N/A	2	3	85 / 95 / 2050
h. Modular technologies will be utilized in industrial research and development efforts. In other words, programs will be developed in theory and placed on tape. Combinations of machines and computers will be utilized to determine the practicality of various combinations in an effort to accomplish the objective of the program.	M	6	4	74 / 76 / 80
i. Sub-routine libraries will become more general, i.e., library routines more like generators than fixed procedures.	N/A	8	8	69 / 70 / 71
j. For new, more exotic application, software cost will substantially increase. Conventional business and scientific application can make greater use of software systems supplied by the hardware manufacturer as part of the library package.	S	4	6	70 / 73 / 76

CATEGORY - 13. SYSTEMS AND APPLICATIONS (Cont'd.)

	EVENT	Goal	Desirability	Feasibility	Timing
ff.	Touch Tone input to remote microfilm Retrieval Systems and graphic print out.	S	5	6	69 — 71 — 73
gg.	Improved software for micro-digital recording of facsimile of printed or typed material, in the range of 100-1 reduction.	N/A	8	5	70 — 73 — 78
hh.	Drafting will be reduced to a set of codes which may be transmitted as easy as data. The engineer or the draftsman would compose a drawing in this new language and it would become as easily understood and recognizable as our present simplified drafting practices.	N/A	8	6	71 — 73 — 75
ii.	Information banks will be established on the basis of professions, types of equipment, technologies, special fields of interest, etc. They will do their searching on computer controlled basis; however, it is likely that microfilm will play a significant part in it, either as the information store or as the means of delivery of the information.	N/A	3	5	75 — 76 — 85
jj.	Instead of buying books and going to libraries for information, a student will be issued a reader and complete sets of microfilm with his entire course of study and all of the associated reading materials. The cost would be sufficiently low that the convenience to him would be worth the cost. The ability of microfilm to be distributed quickly and easily and updated would make it possible for additional materials to be handed out easily and quickly to be added to the collection in case the art is advancing or additional materials become available.	N/A	5	7	72 — 75 — 80
kk.	Use of microforms in the home will be accelerated by merchandising in color microfiche catalogues read on home TV viewers.	N/A	5	5	72 — 78
ll.	Computer generated tapes for playback on inexpensive audio video equipment will be prevalent.	N/A	5	5	76 — 81 — 87
mm.	Digitized voice/analog transmission between central offices and switching centers to facilitate time-division multiplexing, encryption and switching.	S	5	5	71 — 76

CATEGORY - 13. SYSTEMS AND APPLICATIONS (Cont'd.)

	EVENT	Goal	Desirability	Feasibility	Timing
nn.	Full blown time-sharing systems which provide multi-programming capability and remote terminal servicing will be available.	S	9	7	70 72 74
oo.	There will be substantial use of the on-line time-sharing computer systems which will facilitate the purchase of computing services at a reasonable price. Line costs will still be high, resulting in system costs which will prevent widespread use for some time.	S	8	6	69 70 71
pp.	Use of simulation to determine design of information storage and retrieval systems.	N/A	5	5	69 71 72
qq.	Modular, dynamically changeable command structures in on-line systems for rapid construction of easier man-machine interfaces which are particularized to individual users.	N/A	8	8	70 72 74
rr.	Man-machine capabilities to allow a user to examine in greater detail, at various levels, the output results of Management Information reports. With this would also come the opportunity to experiment more with overall results by causing changes in variables used in projecting from the bases established by using this stored information. The result would be a greater understanding by the user of the methods used to derive the information and what variables cause changes in what areas.	S	6	6	70 74 77
ss.	Management not making use of management information and control systems which are real-time current awareness call up systems will not be able to perform competitively.	N/A	5	6	70 72 75
tt.	Program restructurable systems.	S	6	5	70 72 74
uu.	User programmed systems without programmers. Programmer only used to program firmware.	N/A	4	6	73 75 77
vv.	Due to cost considerations, there will be an upsurge of remote batch processing systems which will have a depressing effect on interactive time-sharing systems.	N/A	2	1	69 71 72

CATEGORY - 13. SYSTEMS AND APPLICATIONS (Cont'd.)

	EVENT	Goal	Desirability	Feasibility	Timing
cccc.	Development of more powerful capabilities in man-machine areas which lead, instruct and assist the user in obtaining desired results primarily via the use of CRT consoles in on-line, real-time situations.	S	7	7	70 — 75 — 77
dddd.	Personal terminals which "simulate" routine activities of employees in functional departments (e.g., personnel, contract administration, pricing, etc.) so as to increase productivity of administrative work.	M	6	4	74 — 76 — 80
eeee.	90% of the documentation required to manufacture an electronically based product will be computer generated in an acceptable format. Complete electrical documentation from logic designer at a terminal.	M	7	7	70 — 75 — 80
ffff.	Micro-electronic and medical technologies will reach the point where it will be possible to directly stimulate (by implantation or other means) the appropriate areas of the human brain in order to produce sights and sounds as an aid to the blind or deaf.	L	5	3	85 — 90 — 2000
gggg.	The need for higher speed systems will continue to grow. Such systems will be designed and built.	N/A	5	5	69 — 72 — 75
hhhh.	The use of computers in the educational process will expand rapidly and significantly.	S	8	8	69 — 72 — 75
iiii.	Powerful capability will exist for modeling computer programs and computer systems such that predictions of "goodness" of computer hardware and software systems can be made reliably.	N/A	8	5	69 — 72 — 80
jjjj.	Computers will receive signals from radar sets, physical experiments, sensors, etc., and begin to organize them into meaningful structures.	N/A	8	5	73 — 75 — 77
kkkk.	A major increase in the use of small central processors suitable for procurement by individuals to perform such functions as climate and lighting control in the home, systematic information retrieval from various sources such as stock brokers, banks and retailers and scheduling of such functions as maintenance, budgeting and medical care.	M	7	6	72 — 78 — 84

... is the "standard" to Interconnect:

(Servers)

Processing

- General Purpose, numerical; Symbolic
- particular system simulation

- **Memory**
  - files, archiving, database

- **T.** (Communications)
  - protocols to conventional Computers,
  - to all networks & mail systems
  - including voice, fax,

- T. human
  - Images & ability to print/plot
  - voice
  - Human, mechanical actions

- T. real time (to non-computer / non-human)
  - Scientific and manufacturing instruments

Local Area Network

- Aggregation of heterogeneous systems
- Purpose: form net from autonomous
  (message, file, process, term. intercomm.)
- Relatively hi speed (1~30 Mb/s)
  High connectivity
  Systems located in an area, building, Campus
- Based on ISO 7-layer protocols.

Wide Area Network

- Aggregation of heterogeneous Systems and networks
- Purpose : intercommunication of Systems
- Relatively low speed (4 ~ 64 Kb/s)
  Low Connectivity (PABX, Circuit, packet)
  Systems Located in different regions
  Comm. Services are network oriented
  (DECnet and gateways to others (X25, SNA, ..

CLUSTER

- Aggregation of homogeneous systems
- Behaving as a single, Multi-access System
- High speed interconnect (10 ~ 100 Mb/s)
  High connectivity
  Systems located in a room or area.
- Evolution from low-level Op./Sys.
  Service to provide common
  files, print/plot, communication, etc.
- Via "Procedure Call" protocols.

1600 - 1800	3 PC	MANUAL
1800 - 1890	2 PC	MECHANICA
1890 - 1950	1 PC	ELECTRO - MECH.
1950 - 1960	1 ✓	ELECTRONIC
1960 - 1972	2 ✓	TRANSISTOR
≈ 1968	3 ✓	I/C
	4 ✓	VLSI
	5	ULSI
	6	Optical
	7	PARTICLE

LARGE, APPLIED MULTIPROCESSORS FOR INCREASED PARALLEL COMPUTING

NETWORKS

WIDE AREA NETWORK - SPATIAL PARALLELISM

LOCAL AREA NETWORK - MORE TIGHTLY COUPLED, SPATIAL PARALLELISM

LOCAL AREA NETWORK CLUSTER - ALL PROCESSORS OPERATE AS A SINGLE SYSTEM

CLOSE AREA CLUSTER - HIGH RELIABLITY / HIGH PERFORMANCE - SINGLE SYSTEM

SINGLE COMPUTER SHARING A COMMON MEMORY

FUNCTIONAL MULTIPROCESSOR COMPUTER - ONE PROCESSOR PER FUNCTIO (E. G. I/O)

TIMESHARING - ONE PROCESSOR PER USER

PARTIONED OR TRANSACTION PROCESSING - ONE PROCESSOR PER PROCESS OR STEP

FAULT-TOLERANT

- DIFFERENT PROCESSORS ASSIGNED PER STEP WITH REDUNDANT PROCESSING

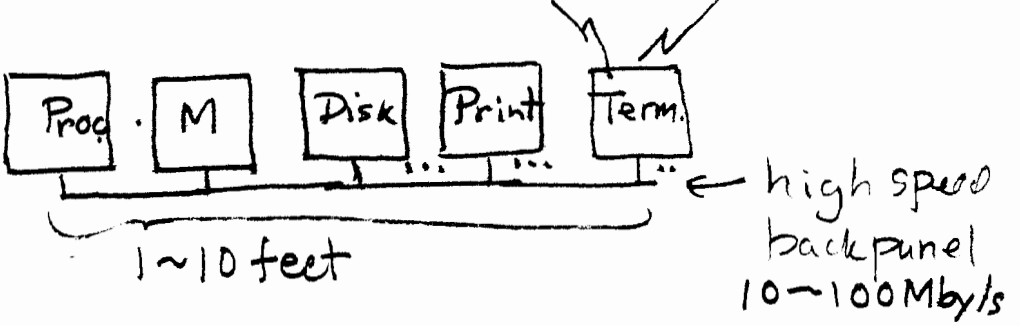
PARALLEL PROCESSING (MULTIPLE PROCESSORS PER JOB)

CONCURRENT-TASK - MULTIPLE PROCESSORS OPERATE ON PARTIONED, INDEPENDENT DATA

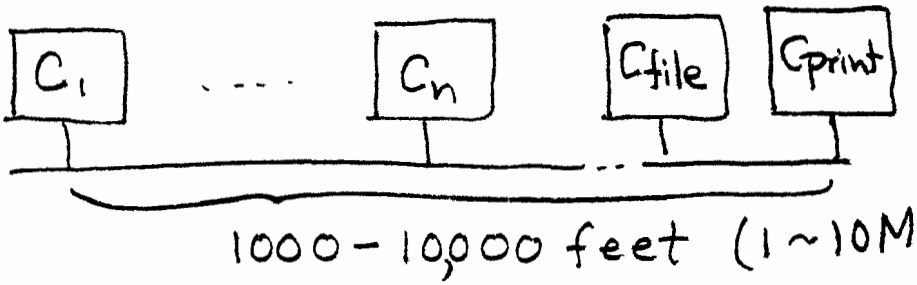
PIPELINED-TASK - PARALLEL PROCESSING OF A SINGLE TASK IN PIPELINE FASHION

GENERAL PURPOSE PARALLEL PROCESSING - DYNAMIC ASSIGNMENT OF PROCESSORS

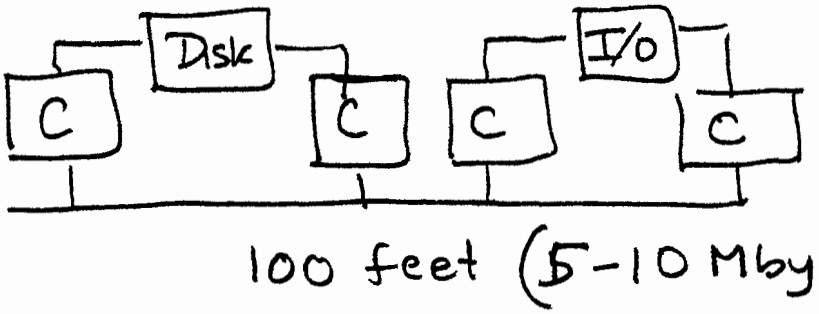
Multiprogrammed Computer (C)



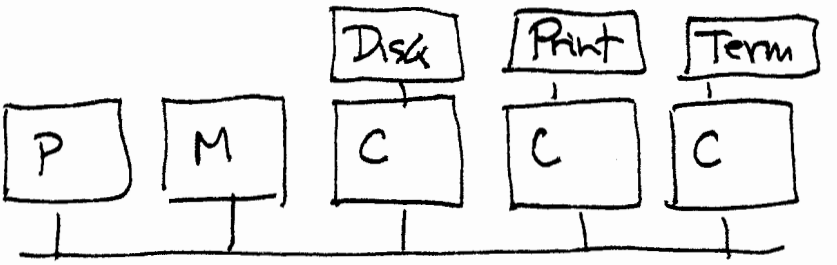
Local Area Net Computer Cluster



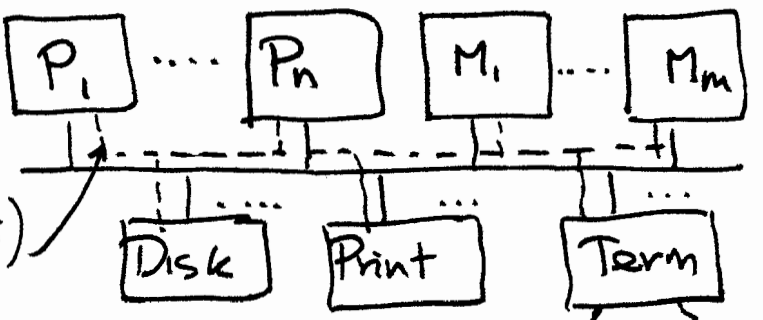
High Availability Cluster (eg Tandem)



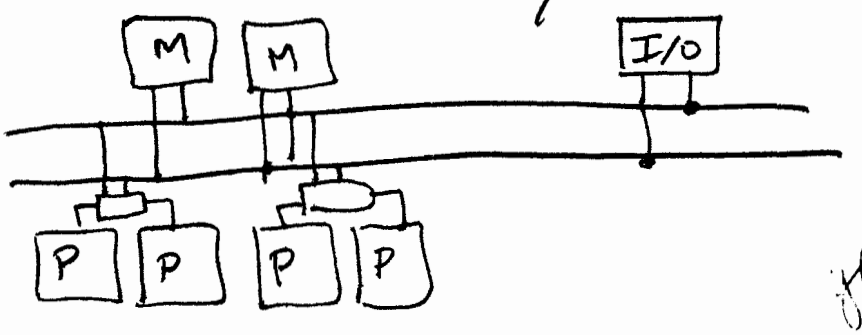
Functional Multiprocessor (eg. Plexus)



Symmetrical Multiprocessor (----- Fault-Tolerant)

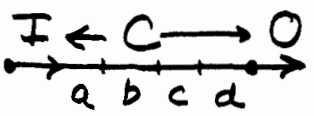


Voting Fault-Tolerant Computer (eg. STRATUS)

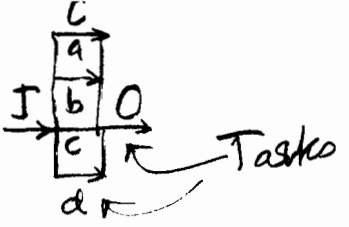


jfb 4/18/84

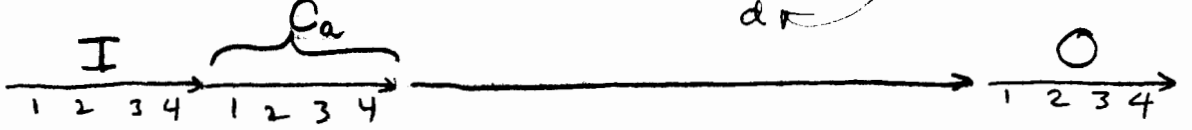
Pipelineable Work.



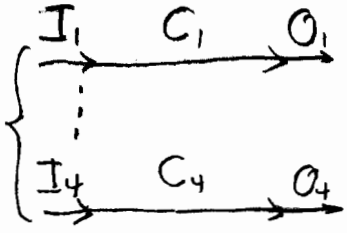
Also



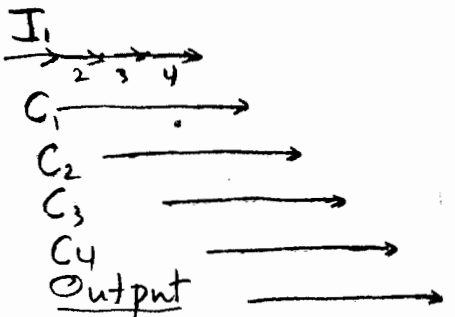
Multiprog. (4 jobs, 1 proc.)



LAN. 1 Computer/job

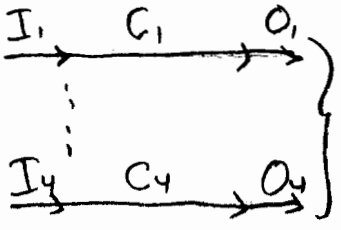


≡

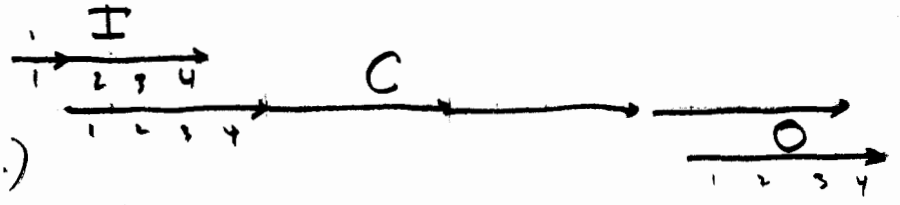


LAN with single input, output.

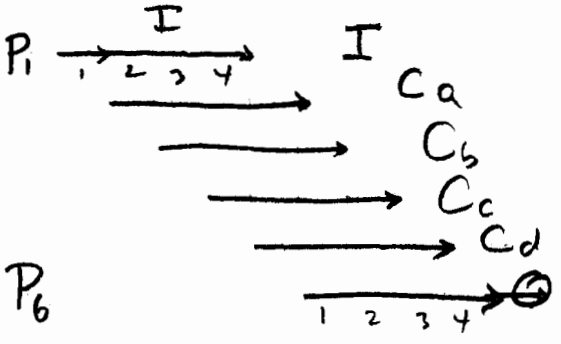
Timesharing One Processor Per user



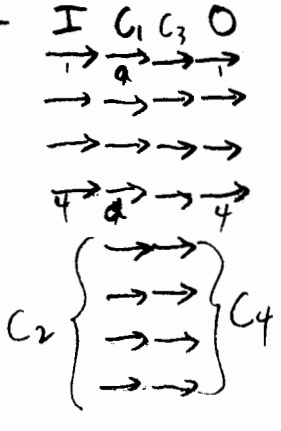
Functional Multiproc. (1 Arith. Proc.)



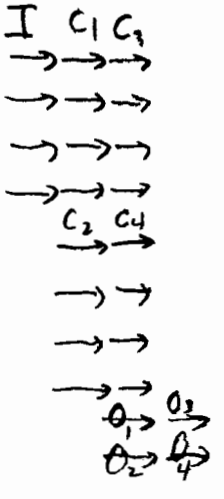
Trans. Proc. (1 proc/Step)



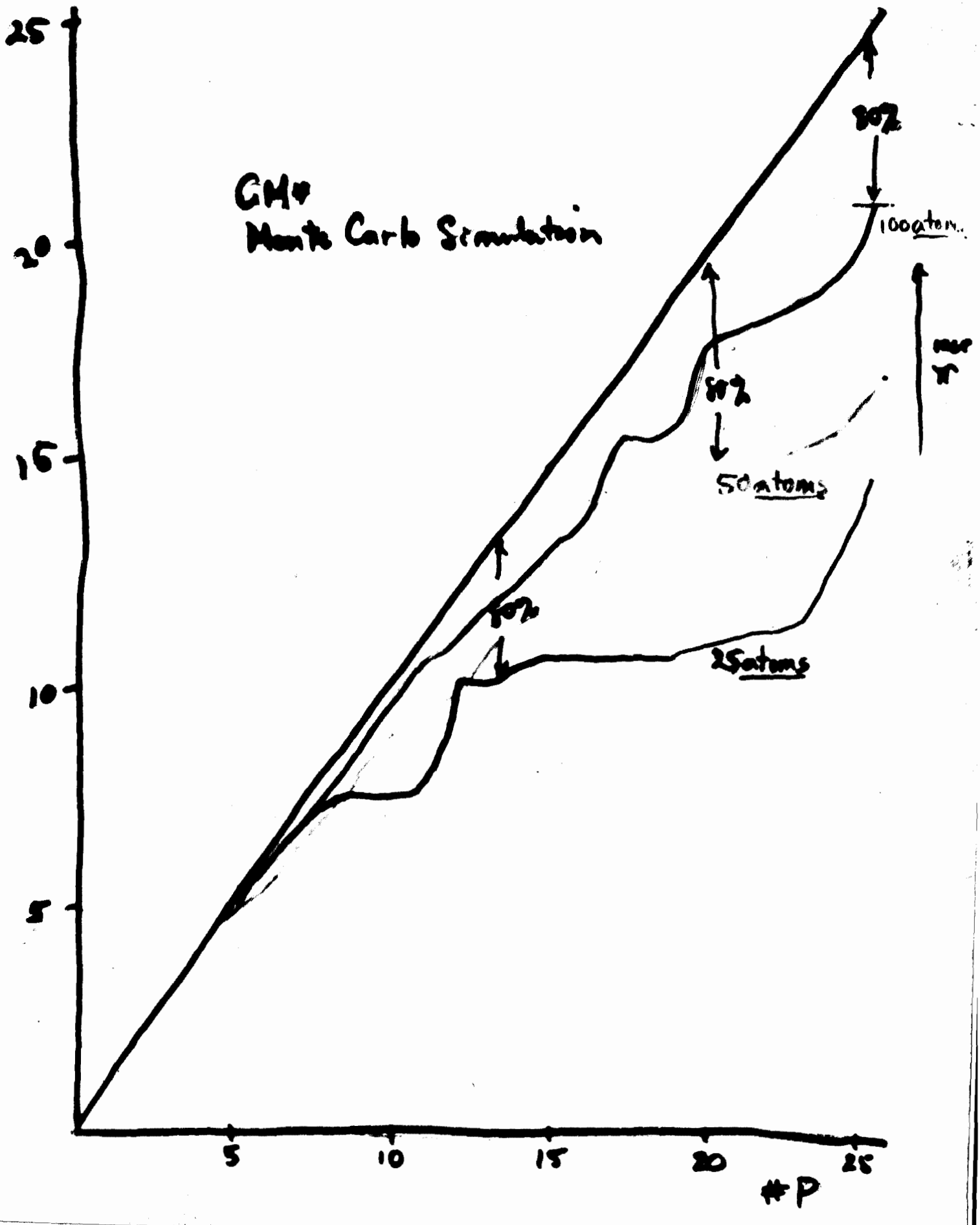
Concurrent Task 3 Proc.



Concurrent Task 10 Proc.



gb 4/18/84

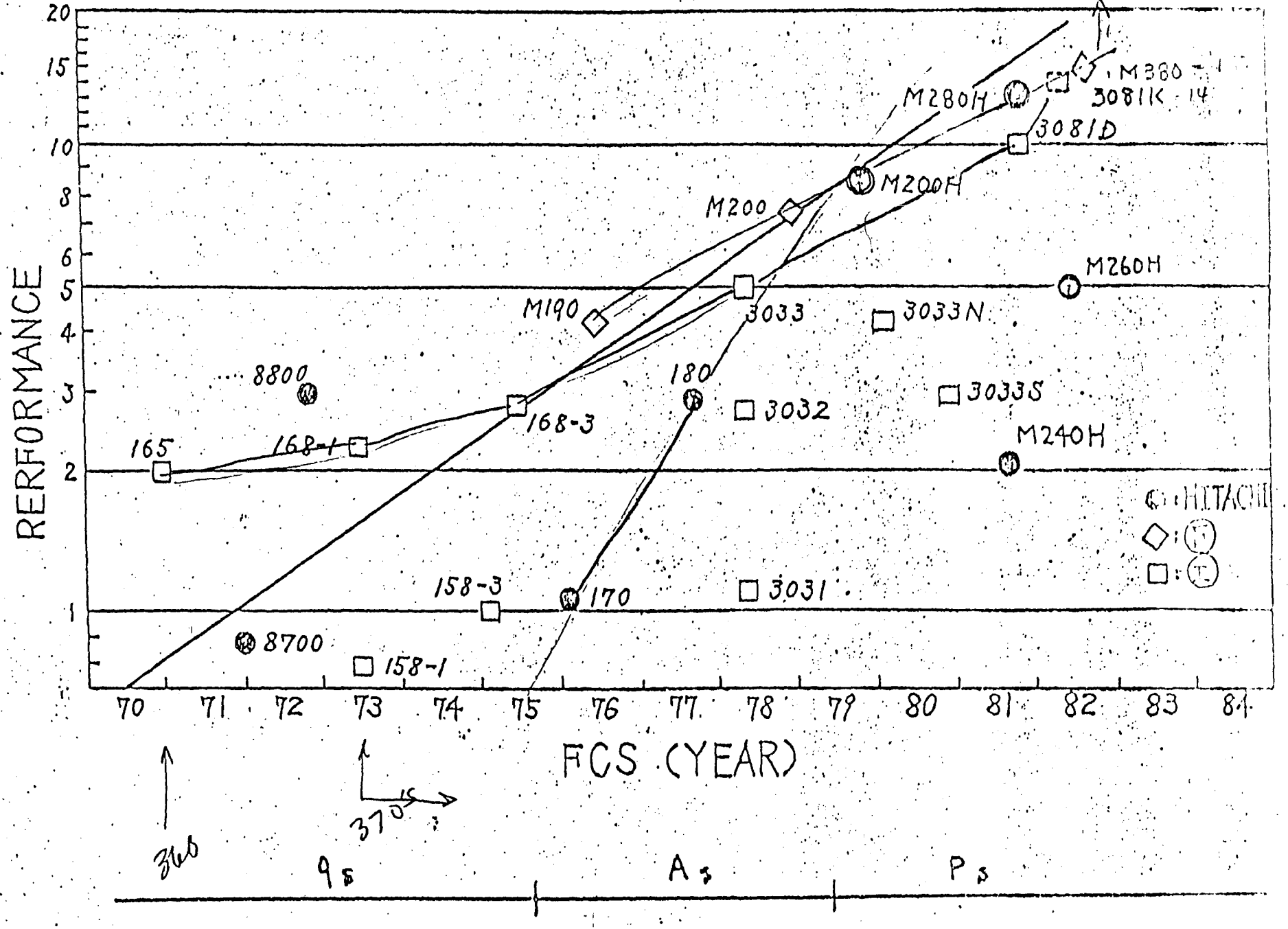

25
20
15
10
5
5
10
15
20
25
#P
CMP
Monte Carlo Simulation
100 atoms
50 atoms
25 atoms

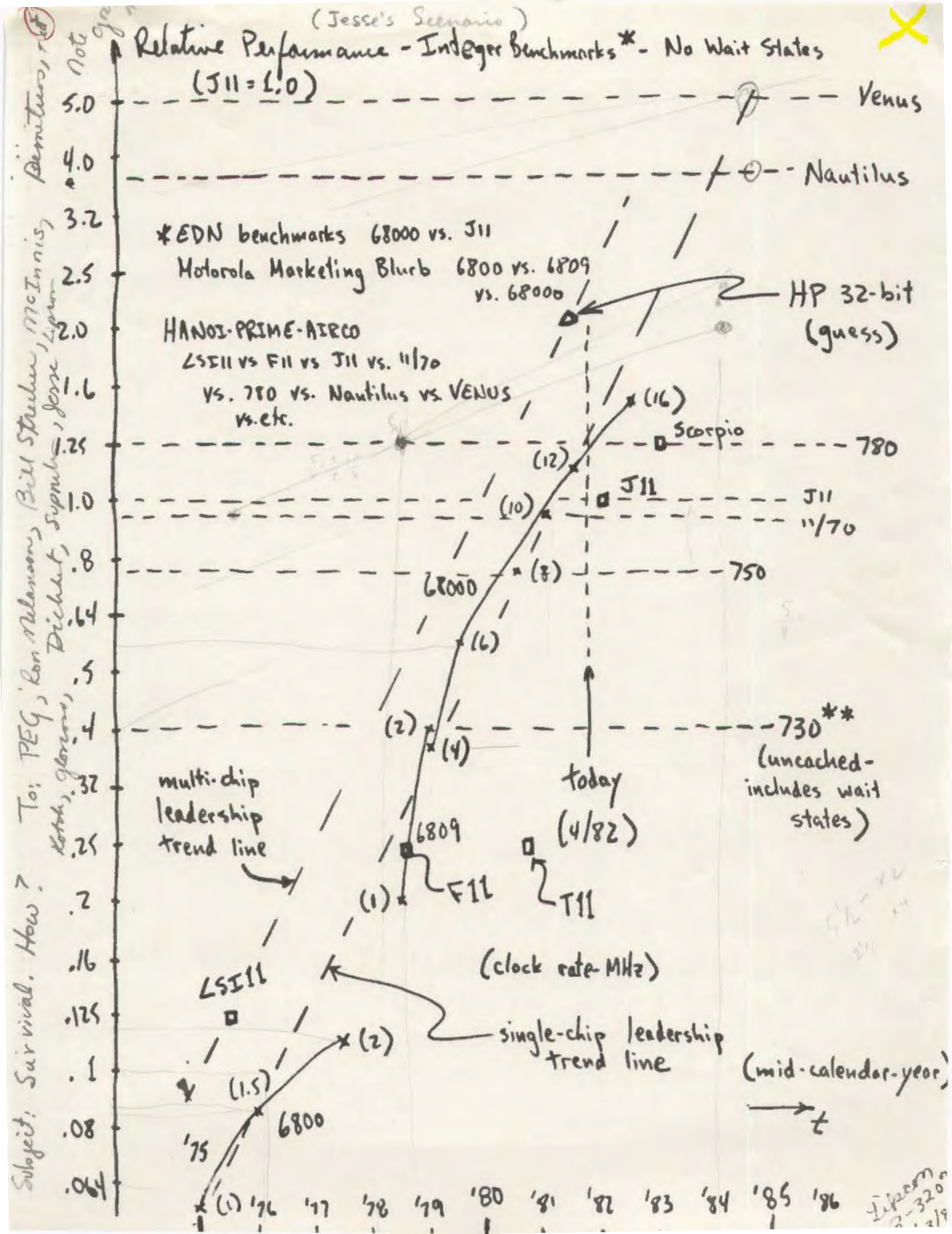
→ Operations Committee, PEG

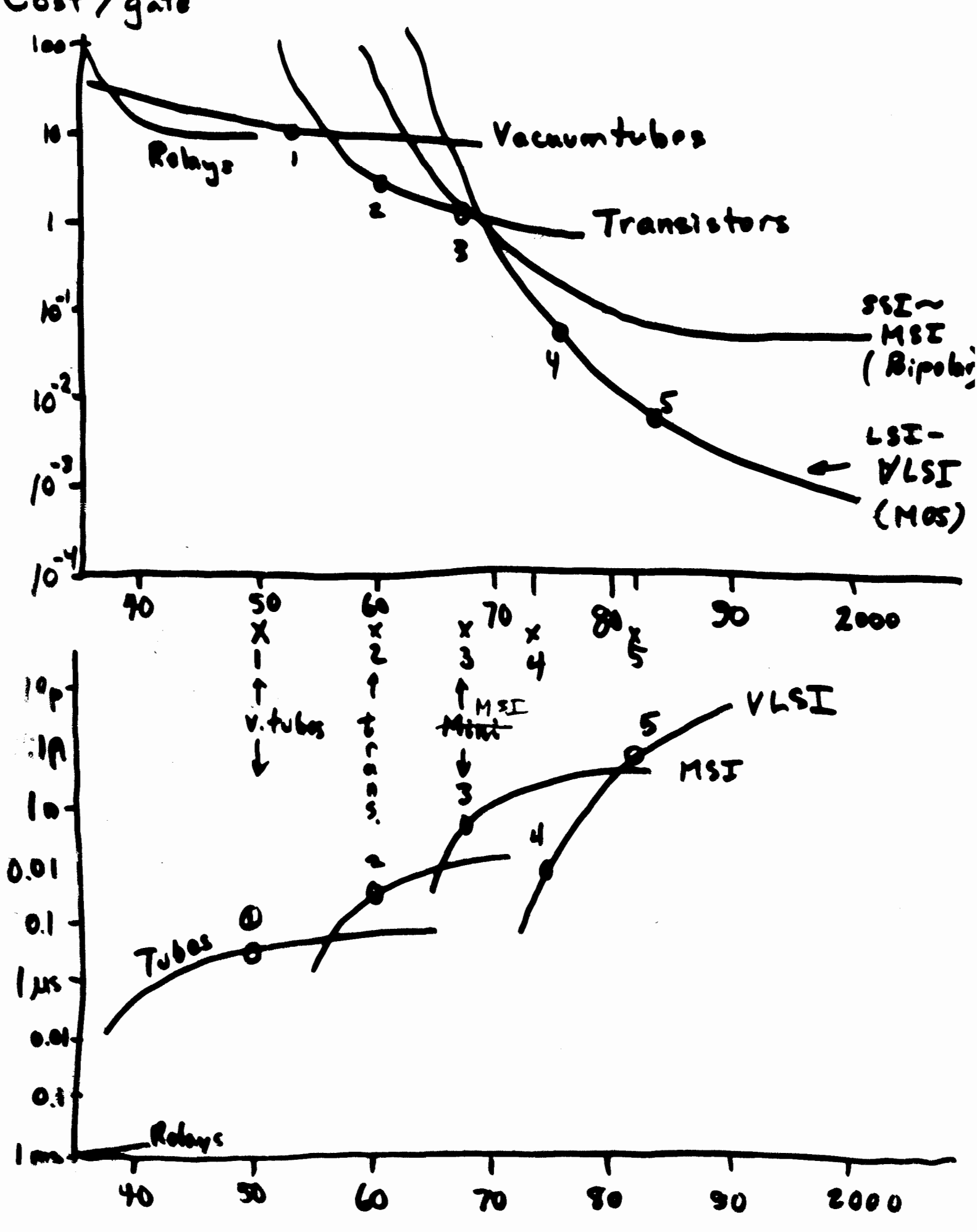
Gordon

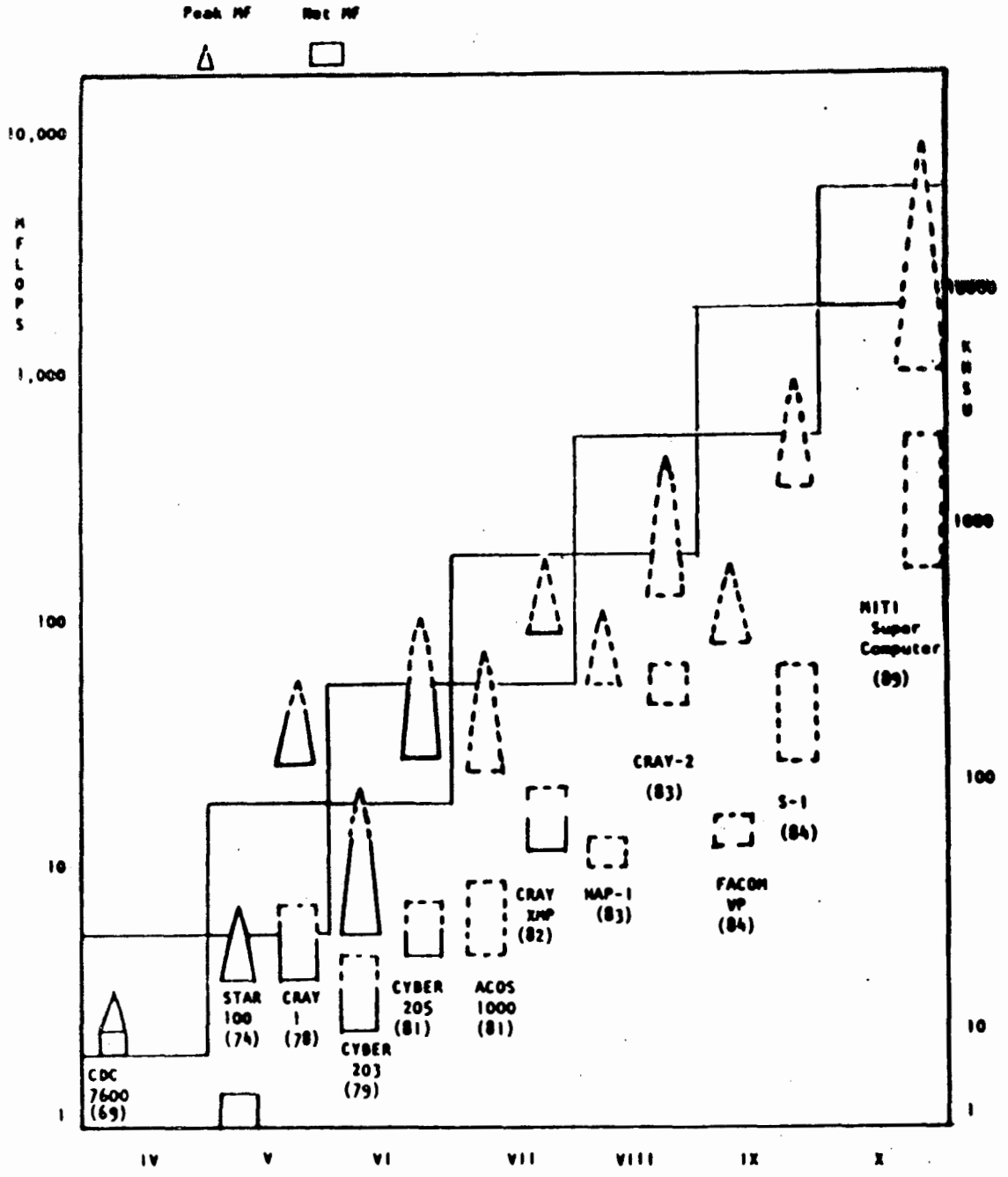
next

TRENDS OF LARGE CPU (plotted by Hitachi)

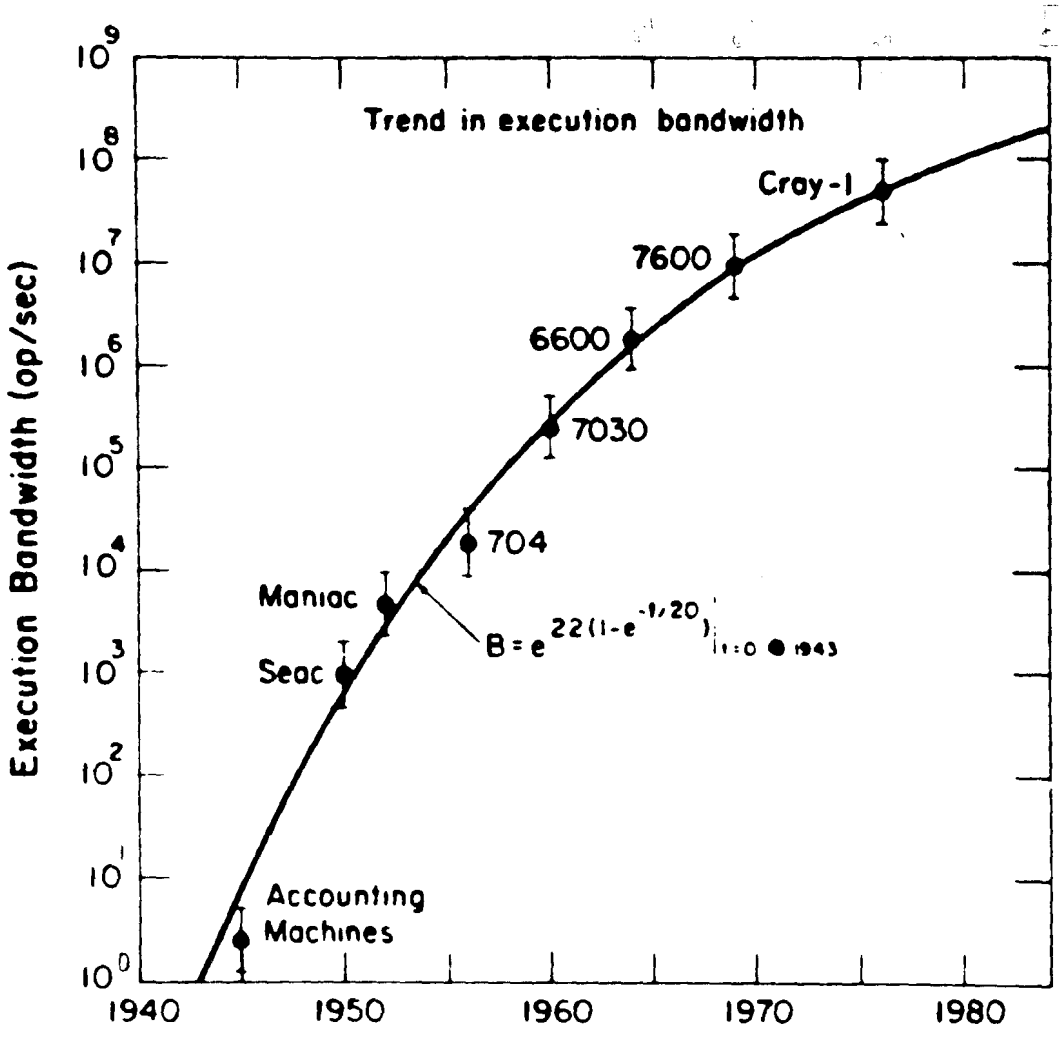



(Jesse's Scenario)
Relative Performance - Integer Benchmarks* - No Wait States
(J11 = 1.0)
Venus
Nautilus
*EDN benchmarks 68000 vs. J11
Motorola Marketing Blurb 6800 vs. 6809 vs. 68000
HP 32-bit (guess)
HANOI-PRIME-AIRCO
LSI11 vs F11 vs J11 vs. 11/70 vs. 780 vs. Nautilus vs VENUS vs. etc.
Scorpio
780
J11
11/70
68000
750
730**
(uncached - includes wait states)
multi-chip leadership trend line
today (4/82)
6809
F11
T11
(clock rate-MHz)
LSI11
single-chip leadership trend line
(mid-calendar-year)
t
6800
'75
'76
'77
'78
'79
'80
'81
'82
'83
'84
'85
'86
5.0
4.0
3.2
2.5
2.0
1.6
1.25
1.0
.8
.64
.5
.4
.32
.25
.2
.16
.125
.1
.08
.064
(1)
(2)
(4)
(6)
(8)
(10)
(12)
(16)
(1.5)
(2)


Cost / gate
100
10
1
10^{-1}
10^{-2}
10^{-3}
10^{-4}
Relays
Vacuum tubes
Transistors
SSI~MSI (Bipolar)
LSI-VLSI (MOS)
1
2
3
4
5
40
50
60
70
80
90
2000
x 1 ↑ v.tubes ↓
x 2 ↑ trans. ↓ 2
x 3 ↑ MSI Mini ↓ 3
x 4
x 5
10^{0}
1 μs
0.01
0.1
1 μs
0.01
0.1
1 ms
VLSI
MSI
Tubes
Relays
4
5
40
50
60
70
80
90
2000


Peak MF
Rec MF
10,000
1,000
100
10
1
MFLOPS
KMSU
10000
1000
100
10
1
CDC 7600 (69)
STAR 100 (74)
CRAY 1 (78)
CYBER 203 (79)
CYBER 205 (81)
ACOS 1000 (81)
CRAY X/MP (82)
HAP-1 (83)
CRAY-2 (83)
FACOM VP (84)
S-1 (84)
NITI Super Computer (89)
IV
V
VI
VII
VIII
IX
X

EXECUTION BANDWIDTH OF HIGH-PERFORMANCE COMPUTERS
OVER THE PAST 25 YEARS



REF: B. L. BUZBEE, ET.AL., "DOE RESEARCH IN UTILIZATION OF HIGH-PERFORMANCE COMPUTERS," LOS ALAMOS REPORT LA-8609-MS

PERFORMANCE RESULTS TO DATE

Nat Goodman

Nov 12 1985

Single stream:

We run like a Vax 750 with decent compilers but no FPA.

For example, here's how we compare on linpack vs. a Vax 750. Within each category, the entries are listed from fastest to slowest.

		Ratio	MFLOPS	Time	Unit

The numbers for a Vax 750 without FPA are:

		Ratio	MFLOPS	Time	Unit
VMS	Double	218	.057	12.1	35.1
Mmax	Double	298	.041	16.7	48.7
Unix	Double	422	.029	23.7	69.0
VMS	Single	138	.089	7.71	22.5
Unix	Single	204	.060	11.4	33.3
Mmax	Single	233	.052	13.1	38.1

Multiple streams:

We get almost linear speed-up when running many CPU bound jobs in parallel.

For example, running 20 incarnations of the Sieve of Erastothenes gives a speed-up of 19.7. This is within 2% of linear.

Compiles are also remarkably linear. Compiling 8 copies of a 10,000-line program gave a speed-up of 7.56. Compiling 8 copies of a 1000 line program gave a speed-up of 6.25.

Another type of program is one in which the problems are independent, but some synchronization is needed to assign problems to processors. For example, Lusk and Overbeek's "grid" program gives the speed-ups shown below.

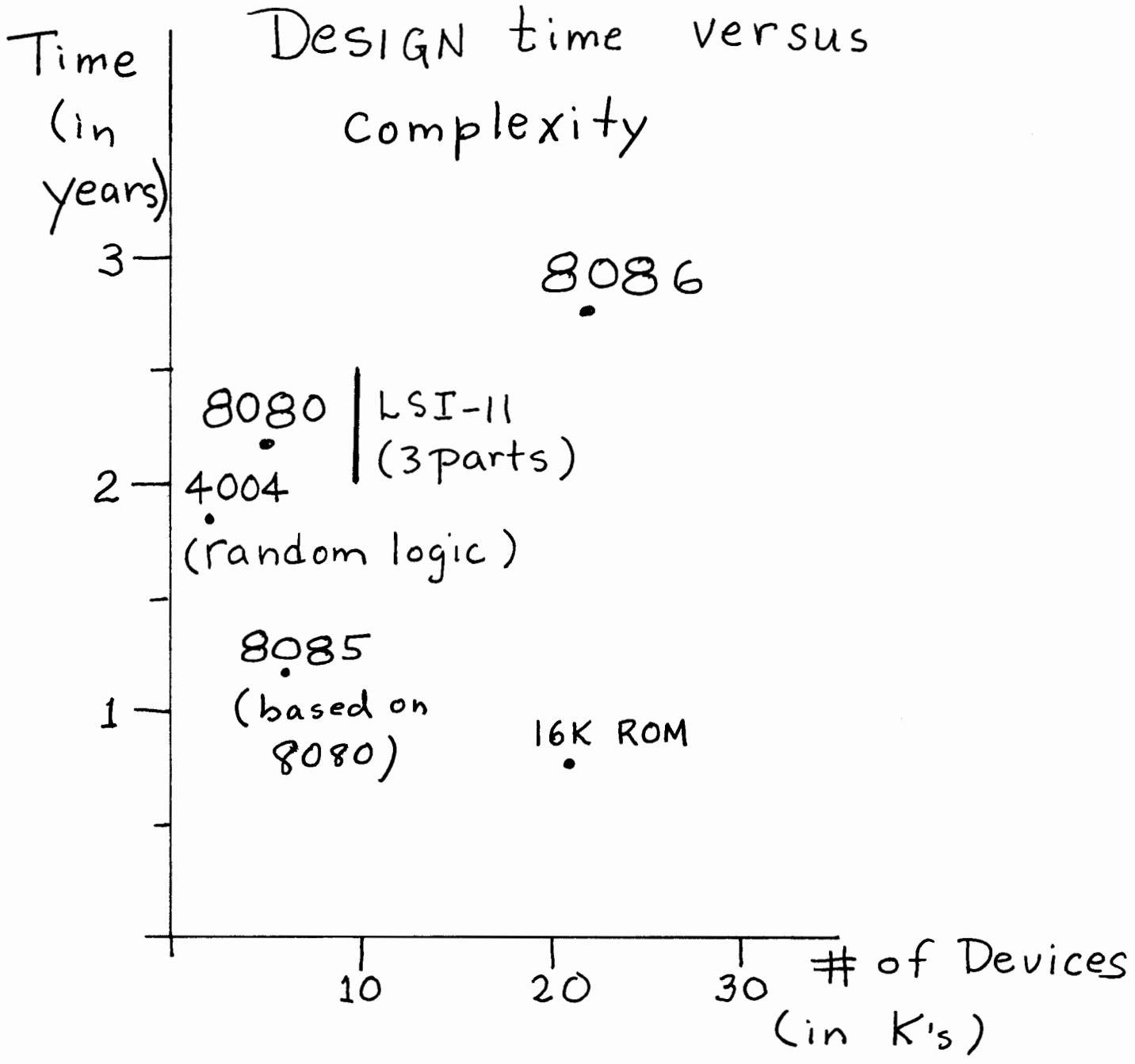
Processors	Speed-up
1	1.00
2	1.90
4	3.86
8	7.56
10	9.72
15	14.34
20	19.17

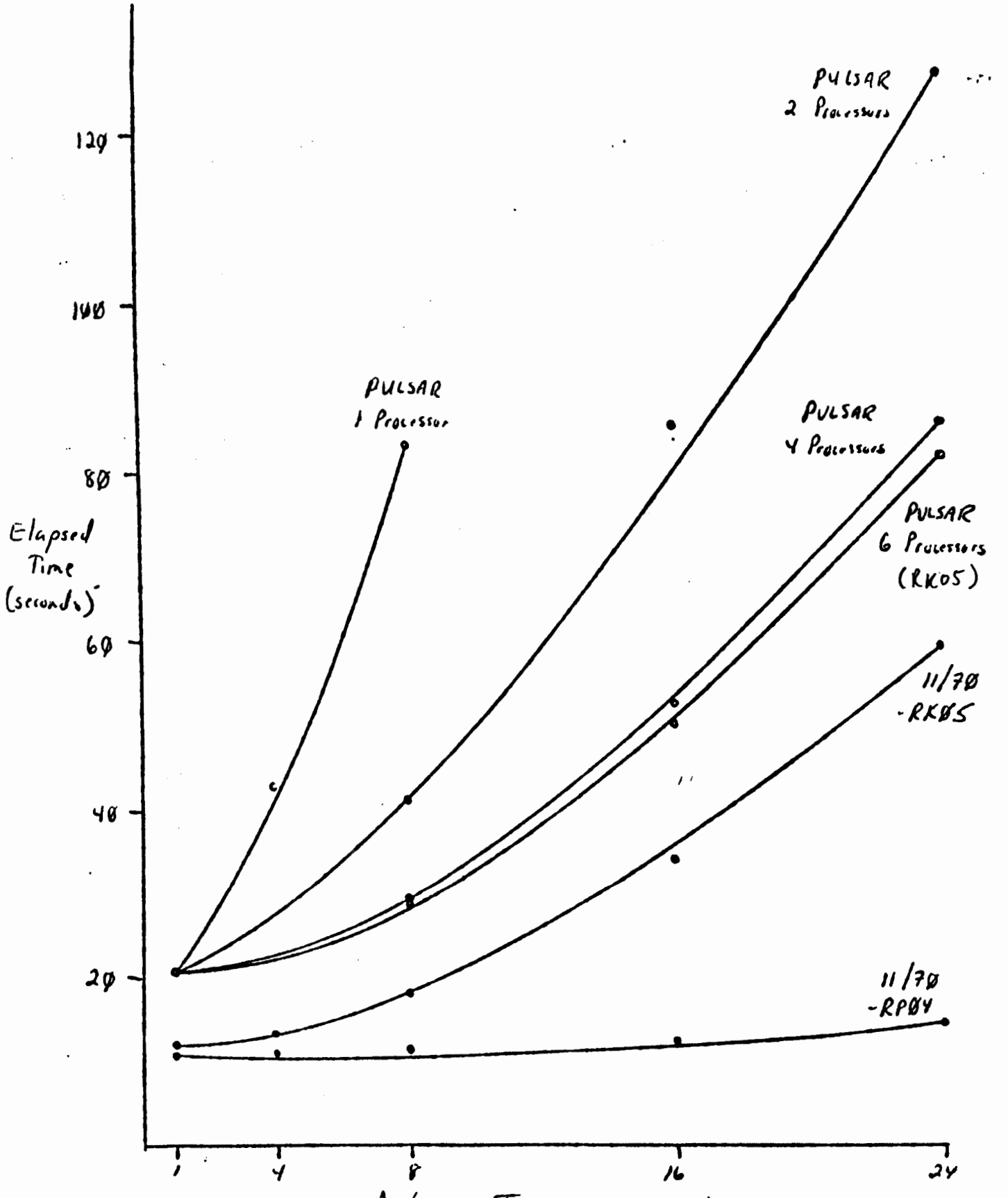
On realistic parallel programs, we're seeing speed-ups between 13-14 (for 20 processors). I expect the speed-up to improve. The programs we're now running were developed for 8 processor systems. When we throw these programs on a 20 processor system, new bottlenecks show up. One program improved 30% after one week's

tuning on our system.

To help with this tuning, we provide a free running, microsecond timer that can be accessed via a memory reference, and a special lock call that returns the number of microseconds spent waiting for the lock.

A customer used these tools to analyze a program that shows 13 speed-up. He found that the program spends about 1/3 of its time waiting for one specific lock! The customer is currently tuning his algorithm to reduce this contention.


Design time versus complexity
Time (in years)
3
2
1
8086
8080
LSI-11 (3 parts)
4004
(random logic)
8085
(based on 8080)
16K ROM
10
20
30
# of Devices (in K's)

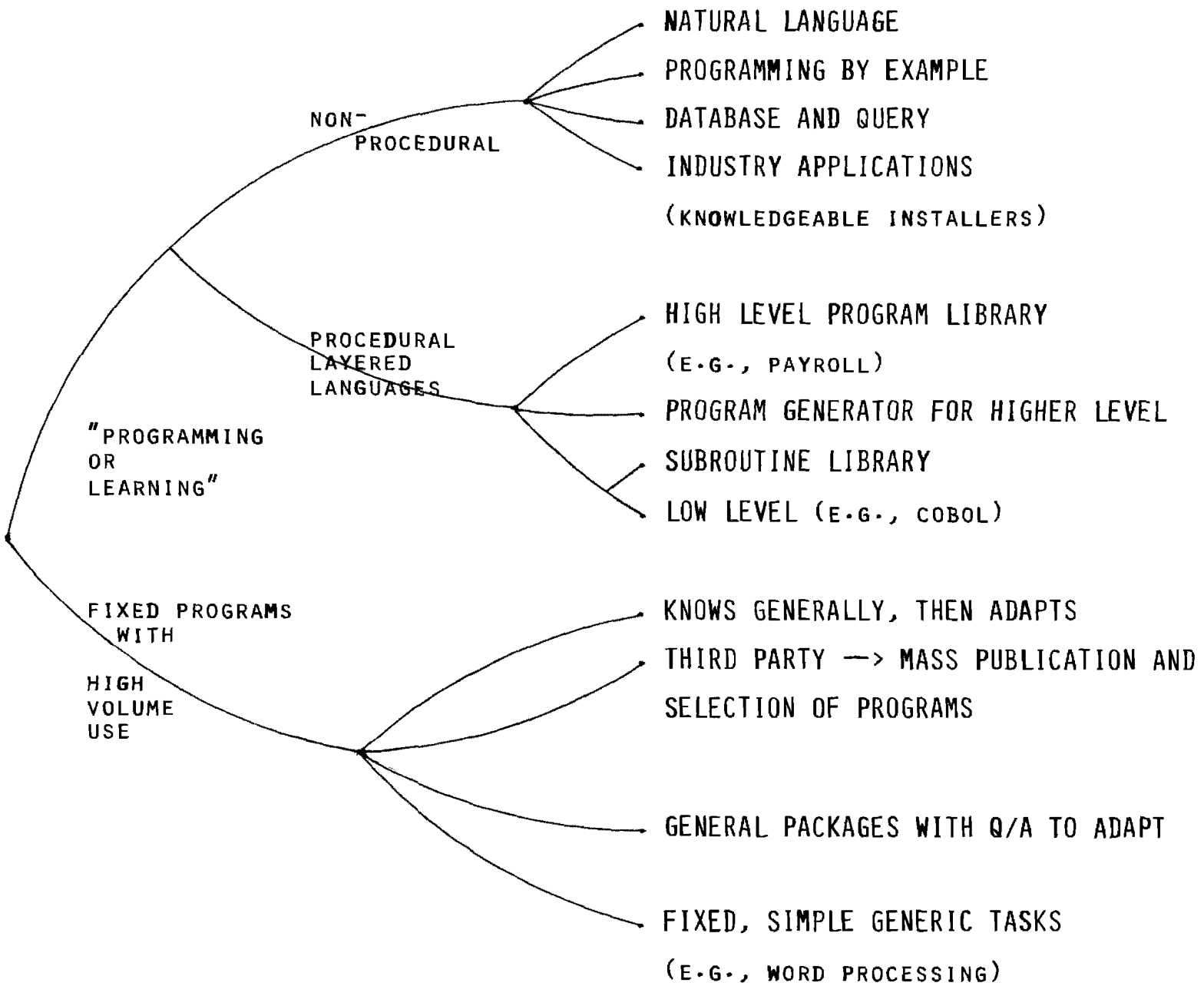


PULSAR - 11/70 Comparison
Workload W2

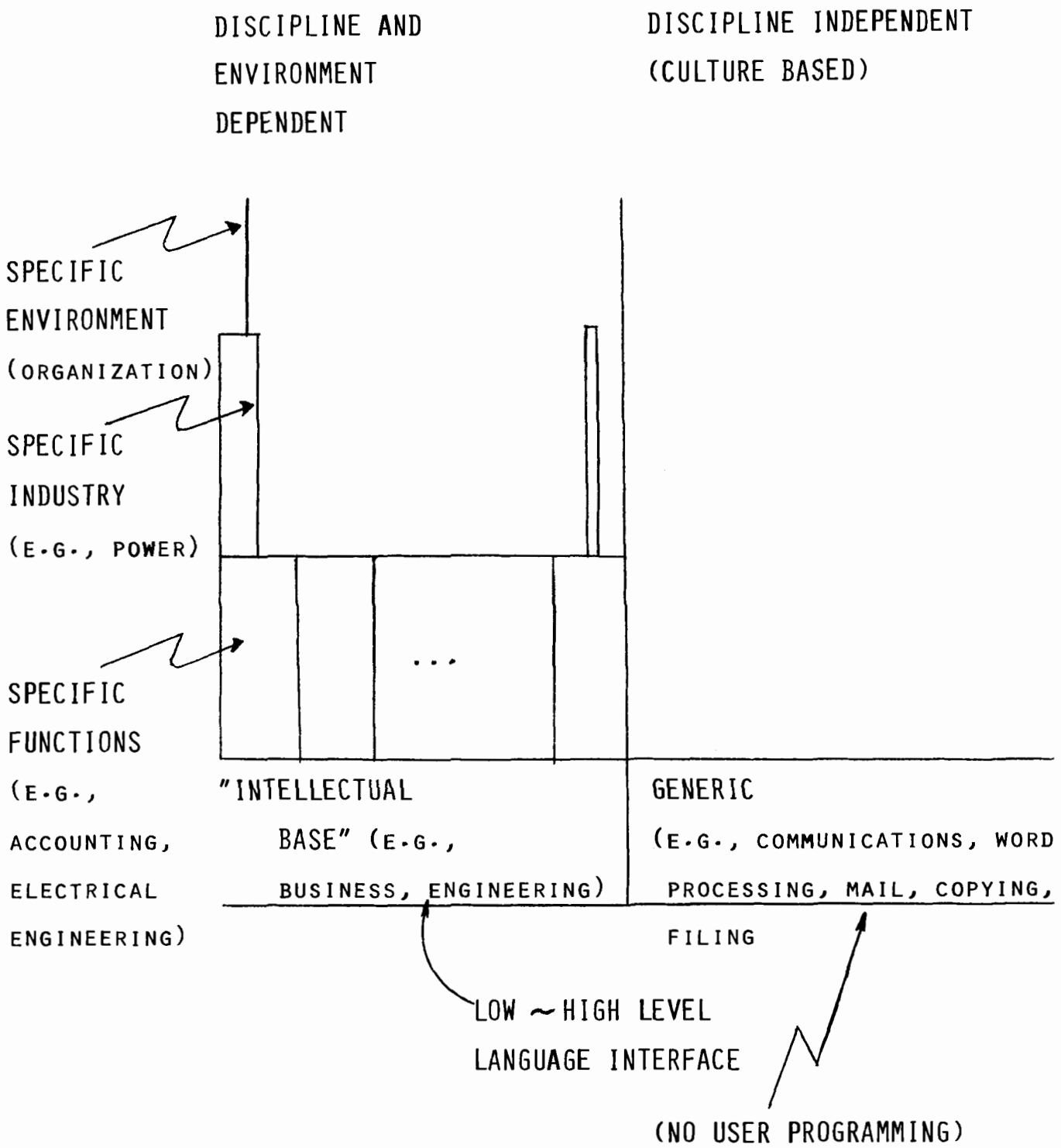
APPLICATIONS PROGRAMS POSSIBILITIES

KEY TO USE?

WILL PROGRAMS BE STANDARDIZED, TAILORED, SELF-INSTALLING AND ENVIRONMENT ADAPTING?



G.BELL, 2/7/79
SLIDES/31



LAYERS OF (PROGRAMMING) LANGUAGES WITHIN A DISCIPLINE AND ENVIRONMENT

G.BELL, 2/7/79
SLIDES/32

INDUSTRIES INVOLVED IN (INCREASED) INFORMATION PROCESSING

SEMICONDUCTOR

- DIRECT
- ADD-ON AND EMULATION OF CONVENTIONAL COMPUTERS
- INDIRECT TO ALL INDUSTRIES

COMPUTER

- MAINFRAME
- MINI

(TERMINAL NETS)

- PERSONAL COMPUTERS
- SERVICES

COMMUNICATION

- NEW PHONE-BASED
- ACS
- OTHER SERVICES NETWORKS

OFFICE EQUIPMENT

- TYPEWRITERS —> WORD PROCESSING
- FAX —> COMMUNICATING XEROX

TV-BASED CONSUMER ELECTRONICS

- GAMES —> PERSONAL COMPUTERS
- CATV AS COMMUNICATIONS

THEME

COMPUTERS ONLY SUPPLEMENT (AND SUPPLANT)
OTHER INFORMATION PROCESSING* SYSTEMS

*INCLUDING TRANSMISSION, TRANSDUCTION, STORAGE, SWICHING AND PROCESSING (CONTROL)

THE POSSIBILITIES ARE NEARLY LIMITLESS

BUT

SYSTEMS CHANGE MORE SLOWLY THAN WE THINK (PREDICT)

LIMITS TO MICROSTRUCTURES

THE TECHNOLOGY PROCESS TO BUILD IT (E.G., INSTRUMENTS AND ROBOTS)

DESIGNERS AND COMPUTER AIDED DESIGN

IDEAS FOR NEW STRUCTURES

LACK OF STANDARDS -- TOO MANY STANDARDS

ALGORITHMS FOR EFFECTIVE USE

EDUCATION OF INTERDISCIPLINARY ENGINEERS AND SCIENTISTS TO APPLY

MARKET SIZE AND USEFUL APPLICATIONS

COMPETITION FROM THE JAPANESE

SOME STANDARDS QUESTIONS
(GOVERNMENT'S, AT&T, DEFACTO)

MUST WE HAVE MORE LOW LEVEL STANDARDS (CHARACTER SET, FLOATING POINT)?

WILL DEFACTO STANDARDS EVOLVE THAT ARE SIMPLY THE 370 AND A SEMICONDUCTOR CHIP?

HOW MUCH NETWORKING CAN BE DONE WITHOUT FULLY HOMOGENEOUS MACHINES? (I.E., CAN USERS STAND IT?)

HOW MUCH NETWORKING CAN BE DONE WITHOUT COMMON LANGUAGES AND A COMPLETE NETWORK ARCHITECTURE? (WILL GATEWAYS WORK EFFICIENTLY ENOUGH?)

WILL A "CHANNEL-LEVEL" INTERFACE CONSTRAIN PRICE OR INHIBIT FURTHER EVOLUTION OF BACK END PROCESSING?

CAN WE KEEP TRACK OF THE DATA? (WILL DB'S OR DB STANDARDS HELP?)

PAPER COSTS (LAST 10 YEARS)

MAIL	INCREASING AT 10%/YEAR COSTS ~ $30 MBYTES TO TRANSMIT, 1979)
BOOKS	INCREASING AT 7%/YEAR
PERIODICALS	INCREASING AT 11%/YEAR COSTS $1 ~ 20/MBYTE (1979)
SHELVES	INCREASING 7%/YEAR (WITH INFLATION)
CATALOGING	$4/ITEM (1979)

HUMAN INFORMATION PROCESSING IS IMPROVING A FEW $/YEAR, WHILE COSTS ARE INCREASING

G.BELL, 2/13/79
SLIDES/39

COMMUNICATIONS COSTS

VAGUE, ALTHOUGH FORECASTS INDICATE COSTS HALVING BY 1985.

(THE NUMBER OF LINES IS NOT INCREASING AS RAPIDLY AS TOTAL OPERATING COMPANY REVENUES. THEREFORE, THE COST/LINE IS INCREASING!)

MODEM COSTS

1973 - 9.6 KB MODEM COST $9.6K
1979 - 9.6 KB MODEM COST $4.5K

} 12%/YEAR REDUCTION

YEAR	DATA-RATE (KBIT)	COST/MBIT
1960	2.4	$1.00
1963	40.3	.42
1964	50	.33
1976	56 (DDS)	.11

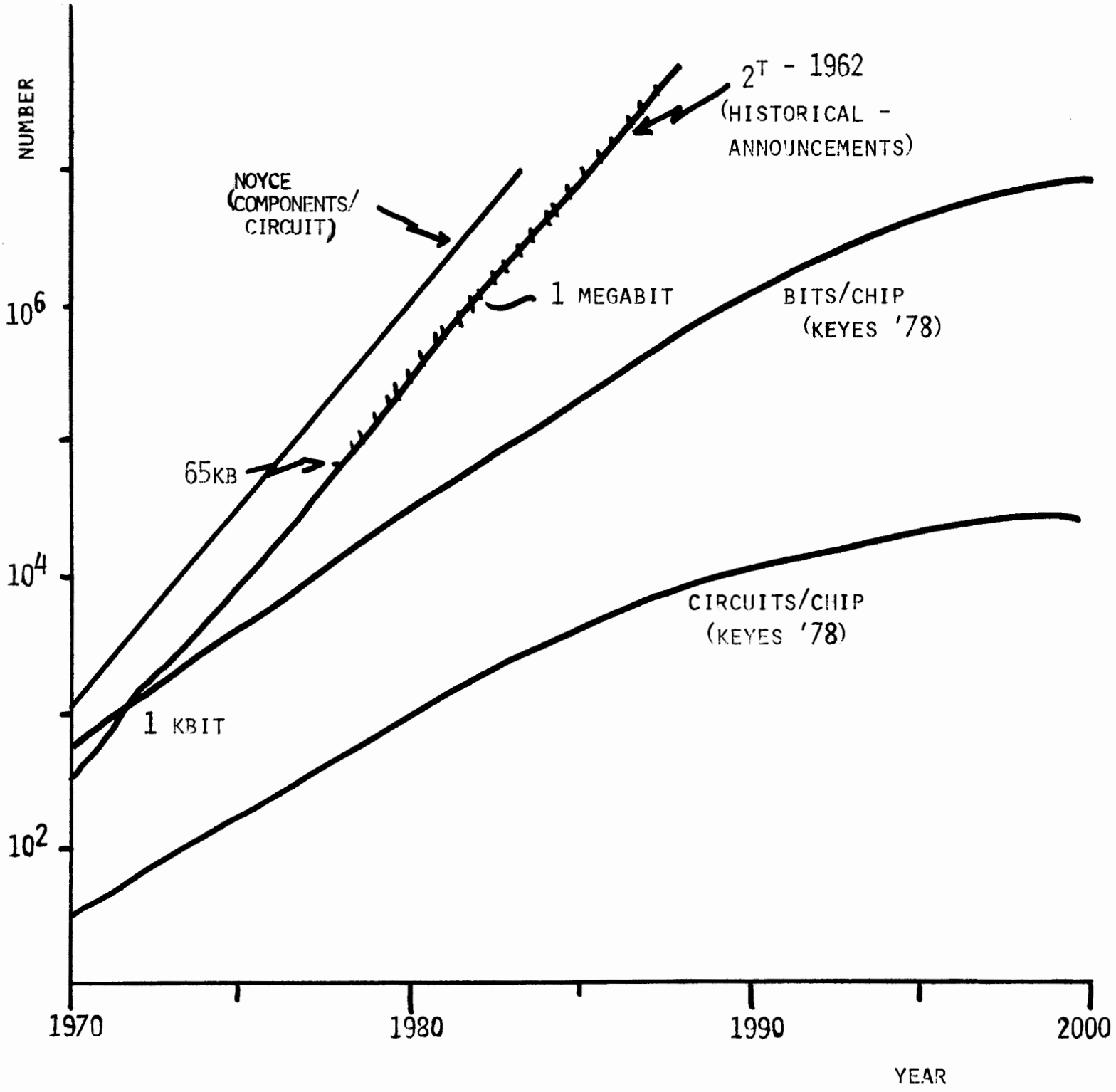
13%/YEAR REDUCTION

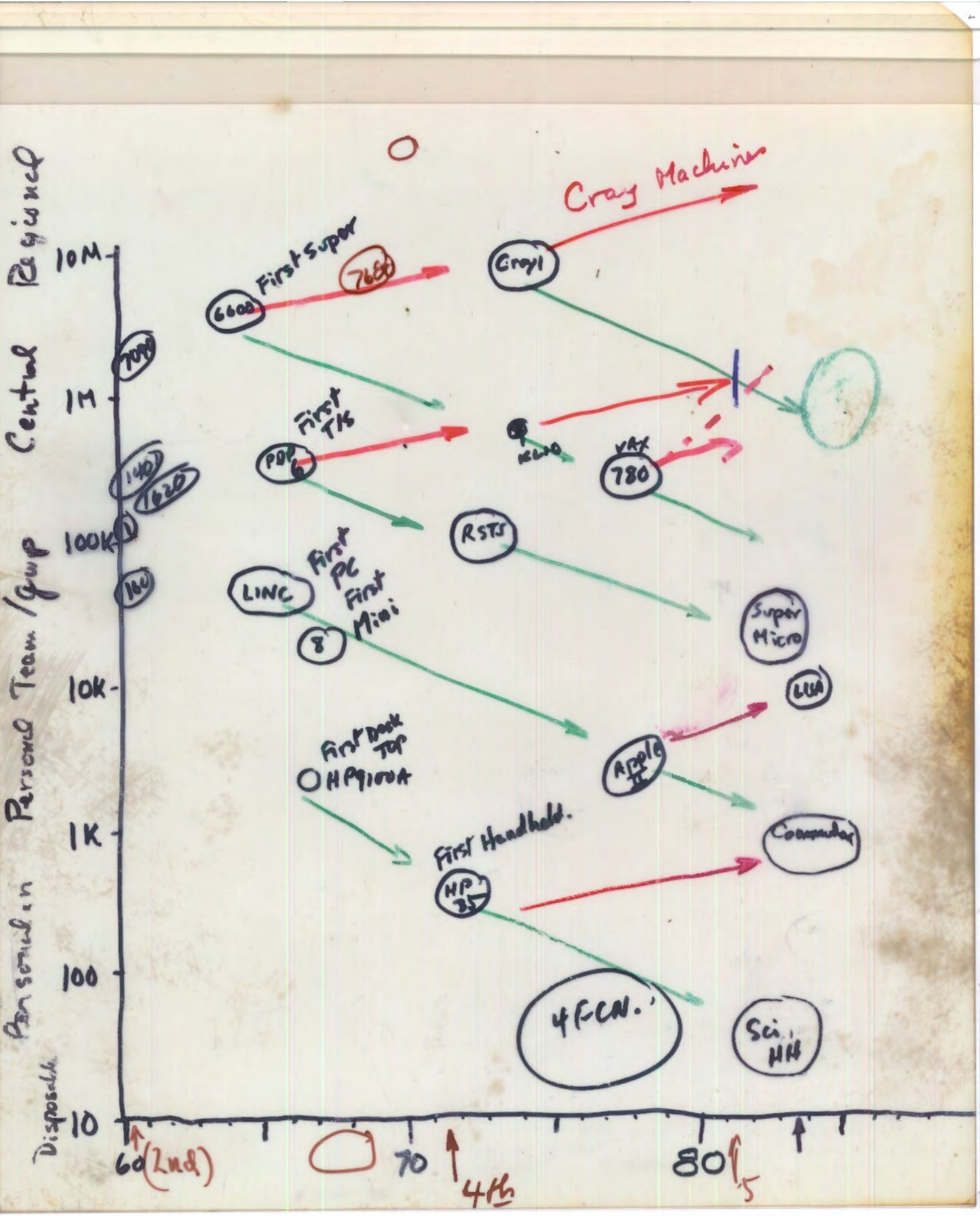
COST* FOR VARIOUS MAIL SYSTEMS

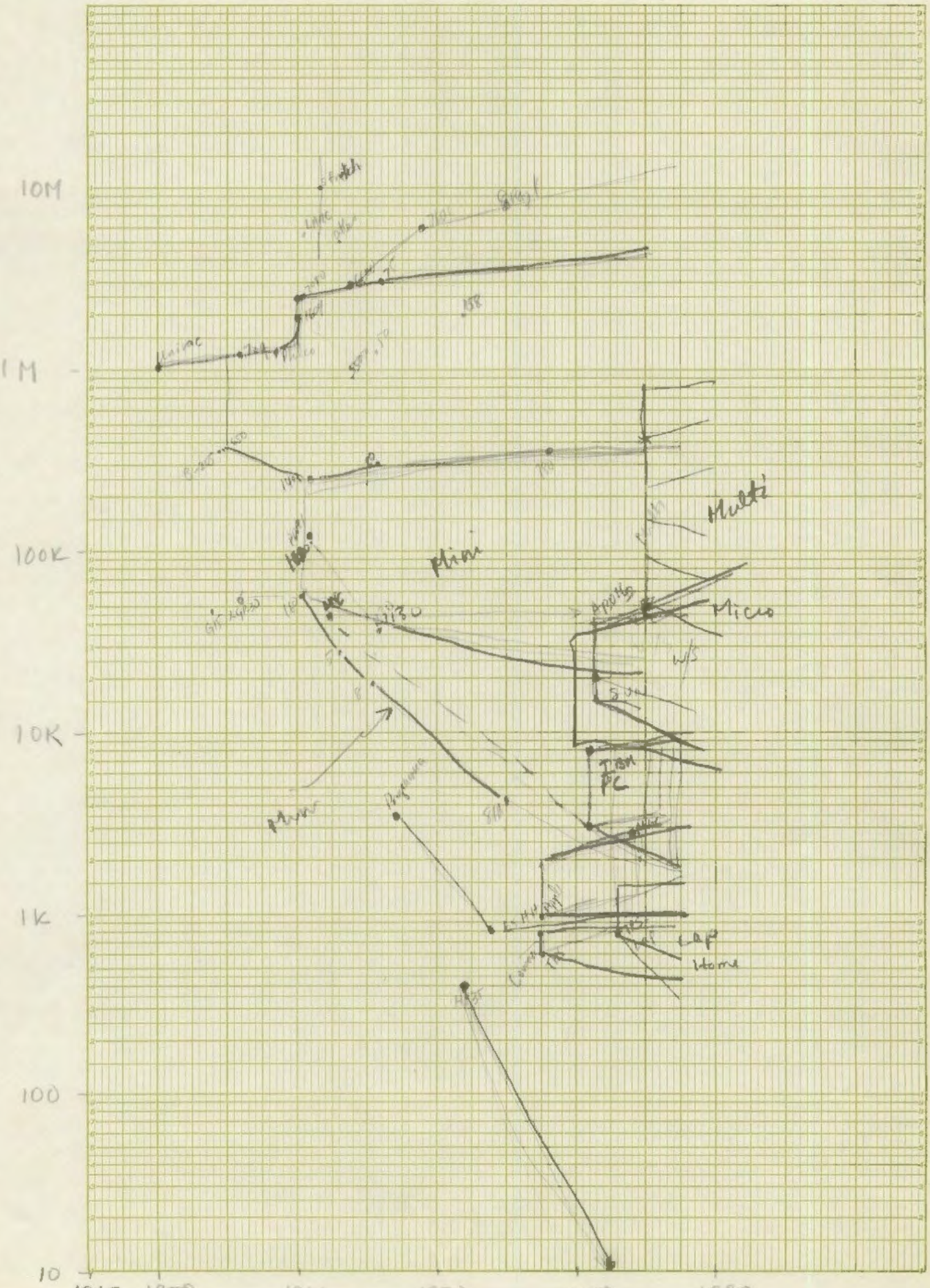
	TRANSMISSION	LABOR
POST	.16	4.06
TELEX	1.75	4.69 ~ 5.31
FAX	1.60	4.44 ~ 4.81
PHONE (3 MIN)	.75	3.82 ~ 4.50
COMPUTER	.27 ~ .98	2.25 ~ 3.76

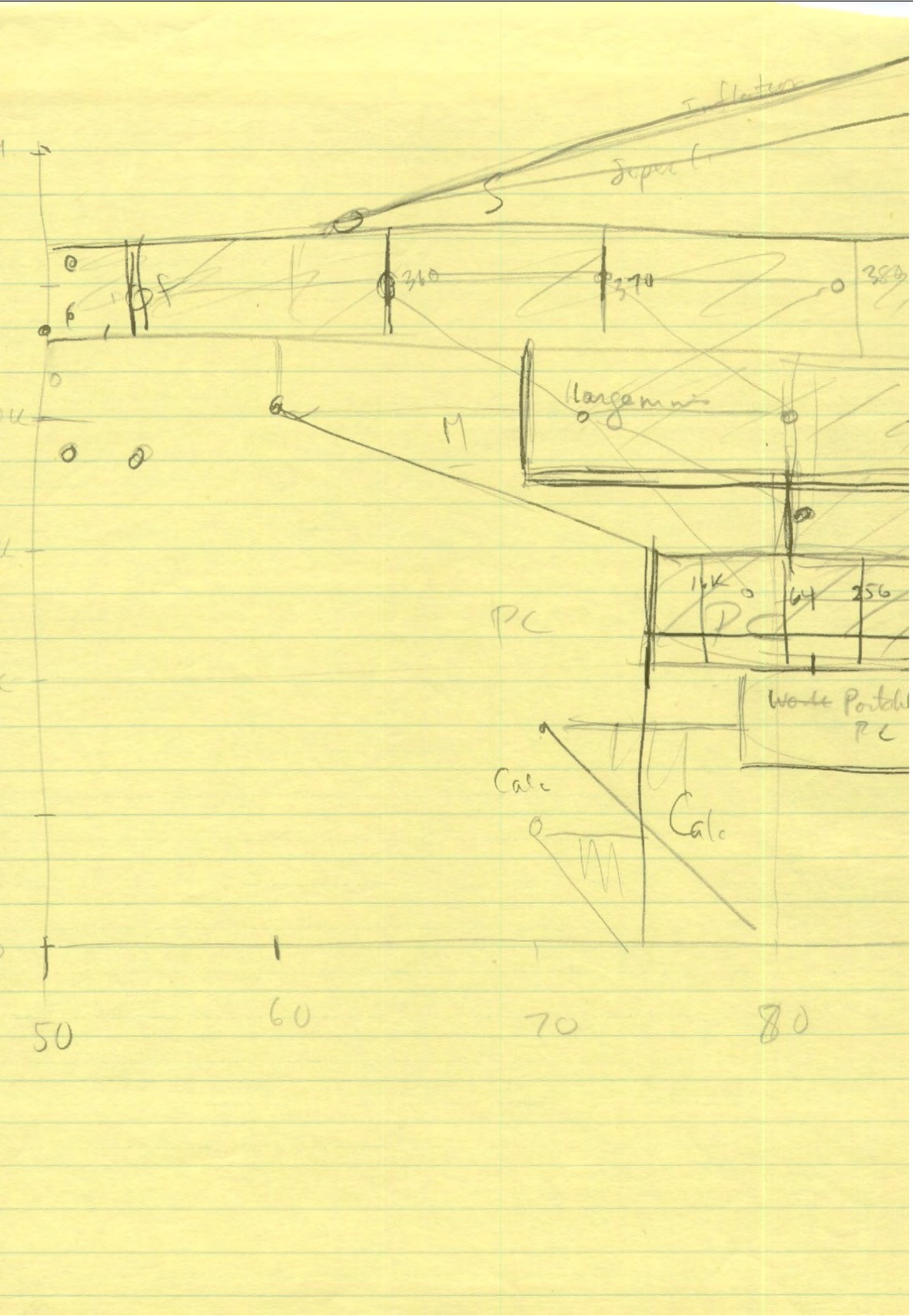
G·BELL, 2/13/79
SLIDES/38

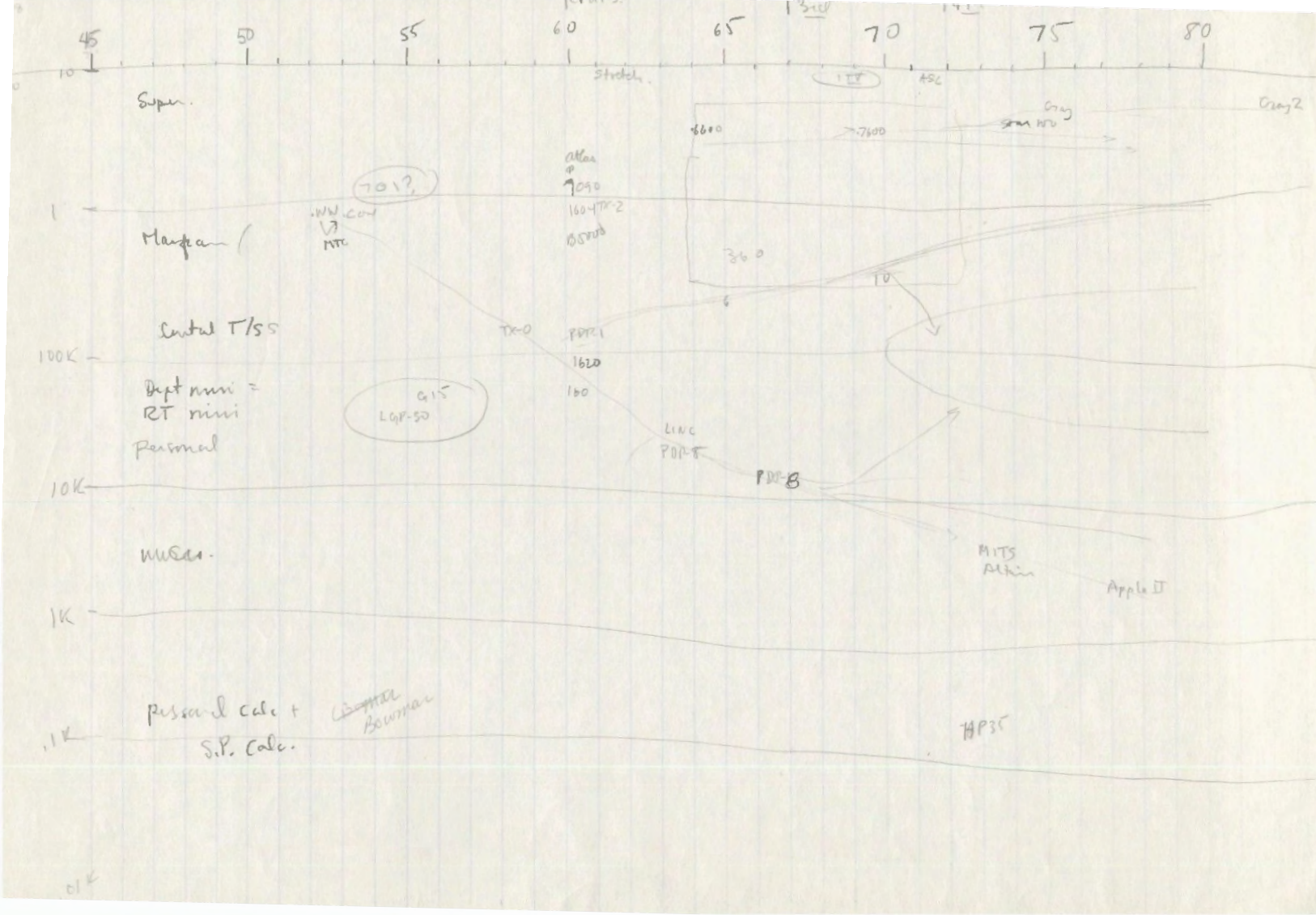
*SRI STUDY, 1978

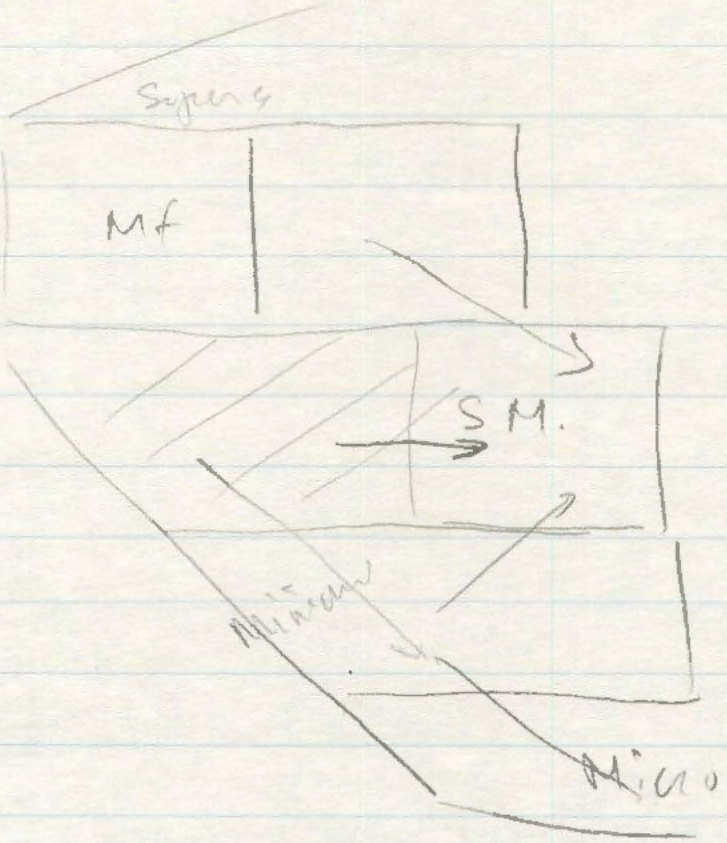

NUMBER
10^6
10^4
10^2
2^T - 1962
(HISTORICAL - ANNOUNCEMENTS)
NOYCE (COMPONENTS/ CIRCUIT)
1 MEGABIT
BITS/CHIP (KEYES '78)
65KB
CIRCUITS/CHIP (KEYES '78)
1 KBIT
1970
1980
1990
2000
YEAR

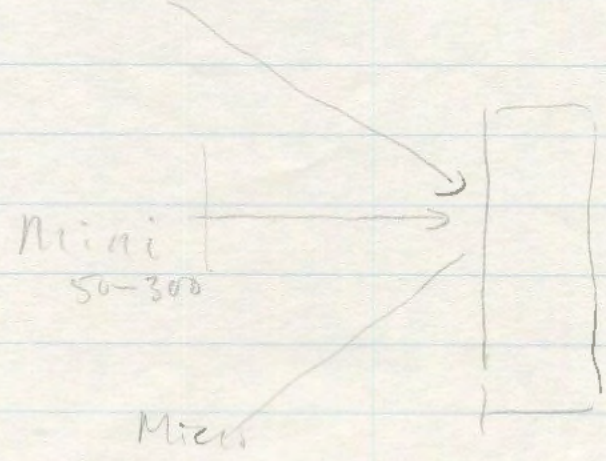

Cray Machines
First super
6600
7600
Cray1
Personal Computer Mainframe Supercomputer
10M
1M
100K
10K
1K
100
10
7090
1401
1620
160
First TK
PDP 8
RSTS
VAX 780
First PC
First Mini
LINC 8
Super Micro
LISA
First Desk Top
HP9100A
Apple II
First Handheld.
HP 35
Commodore
4 FCN.
Sci. HH
60 (2nd)
70
4th
80
5


10M
1M
100K
10K
1K
100
10
1945
1950
1960
1970
1980
1990
Multi
Micro
LAP
Home


340
370
64
256
PC
Calc
50
60
70
80


45
50
55
60
65
70
75
80
Stretch.
ITT
ASC
Super.
Cray2
6600
7600
Cray
STAR MD
Atlas
Manpac
701?
.WW.COM
NYU
1604/TX-2
B5500
360
10
6
Central T/SS
TX-0
PDP-1
1620
100K
Dept mini =
RT mini
Personal
G15
LGP-30
LINC
PDP-8
PDP-8
10K
MITS
Altair
Apple II
micro.
1K
Personal Calc +
S.P. Calc.
Bowman
HP35
.1K
01K


Super
Mf
SM.
Micro


Mini
50-300
Micro

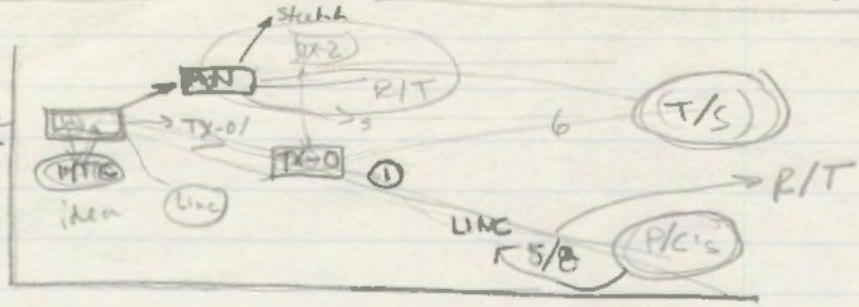
ANFSQ52V

L-1

Clark.

MTC

whirlwind, ANFSQ7, TX-0, TX-2, PDP-1, LINC, PDP-5/8, 6

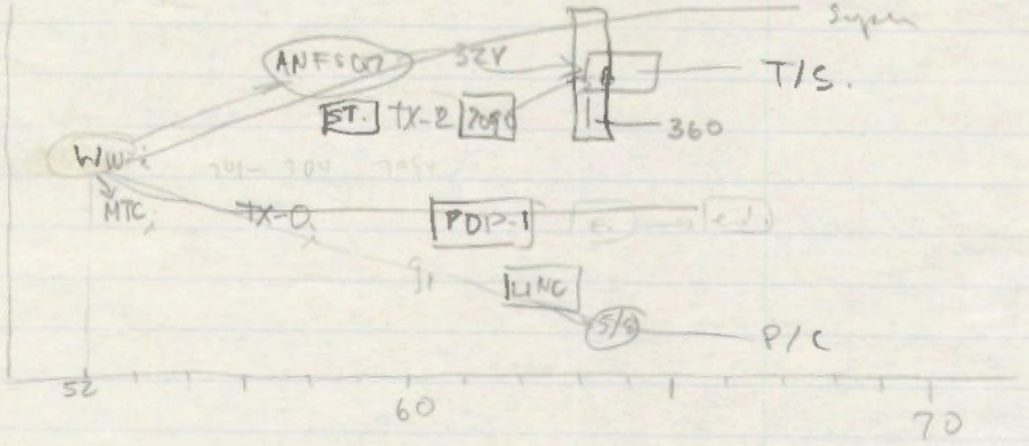


· Stretch
7090

Root of both real time & interactive. (T/S & P/C)

R/T

conflict between - arch + implementation - Ken left because of Clark

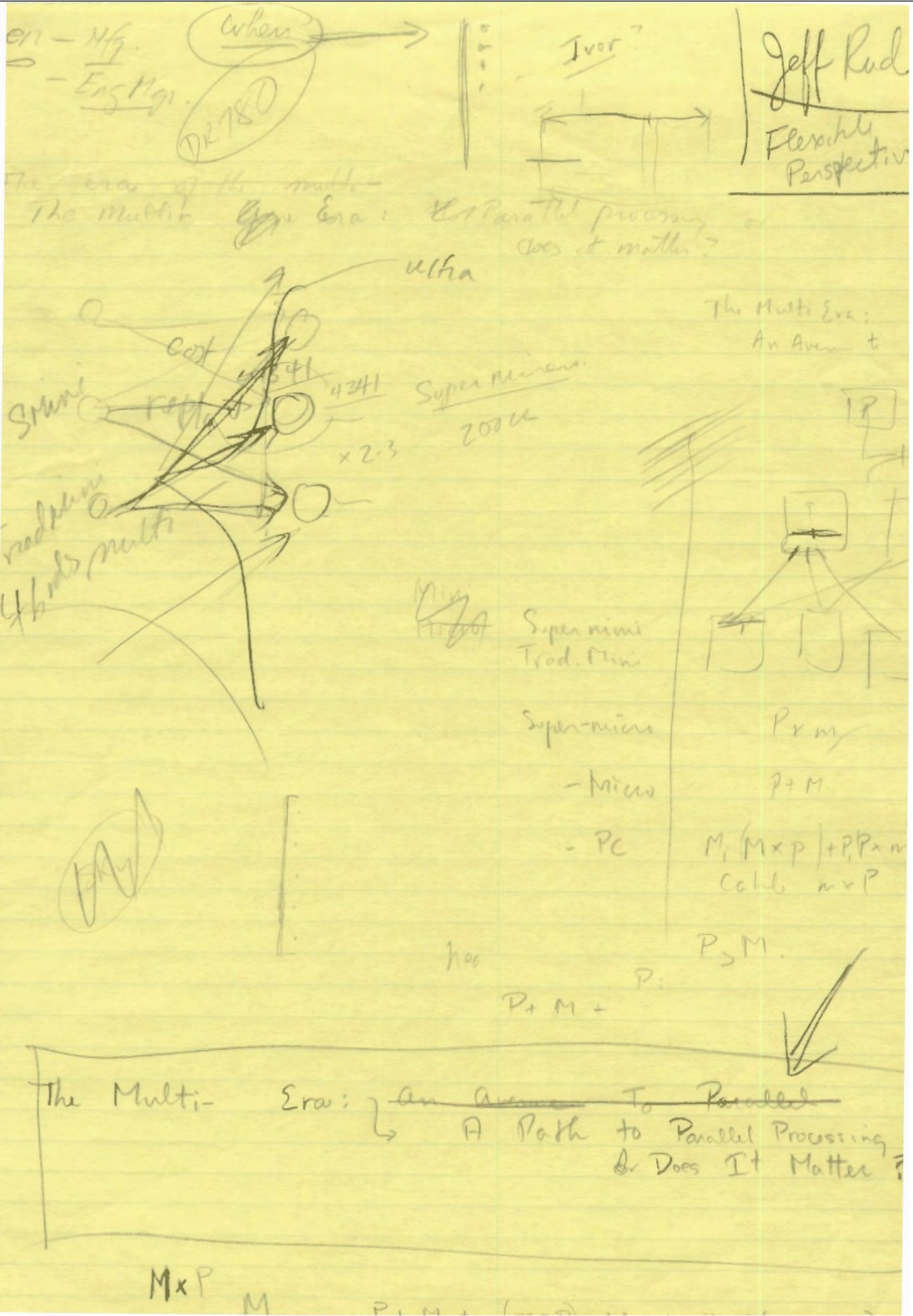


701 → 704 → 70

Search for smallest
" largest ... array!

(Ideas)
· mount — ww, TX-0, TX-2, LINC, MTC, JVA., 7030, 70
· Begin — 1, LINC-8, 701, 5
· maint — 704 — 709Y
· ending. — PDP-8.,

360 - 1
370


Ivor?
Jeff Rud
Flexible
Perspectiv
The Multi Era: A Parallel process
does it matter?
ultra
cost
Super micro
200K
×2.3
Trad. Mini
The Multi Era:
An Aven
P
T
Super mini
Trad. Mini
Super-micro
P x M
- Micro
P + M
- PC
M (M × P) + P P
Calls n × P
P > M.
P + M +
The Multi- Era: A Path to Parallel Processing
Or Does It Matter?
M x P

Timeshare – SS – Prog. MAC. Exciting.
Univ. can do it. THALE population, NO COMITS

Dev. R&D only possible at certain times in certain times. pre-C, late 60's, now (less)

Language Results – algol-60 – Rigid
wanted Algol-W | "genius can't be controlled"
"genius can't control themselves"

→ all SW projects tend to be escaled till they can't be done! – wanted
→ Hoare Tony lecture

→ Retreat to try & control SW projects ... still work at it

CAP – ·–T.S. would get bigger + maint. a prob, + rugged + modifiable
mammoth TS is – need a way to build this (still need
bad + Inc. interest in security + privacy. friendly

Fabry → Hw capabilities
Build HW then SW.
Start in 70

May not nec. believe in it
Res. to obtain Knowledge!
Built it. It was complex! (out of scale?)
Cap II → reduce complexity.

Dataflow – too much belief ... bought, +

Pers. Experiences in OS Research

→ Early days –
Intervening period (30 yrs)
Not successful projects
→ How to chose research projects to remain in Mainstream
· R ⟷ D comply with corporate, short time
· If you are to influence, then look 10 years
How chosen?
· Interesting when it comes to fruition
· It must be possible! It must be too easy.

Must look into future?
① What's going to happen? extrapolation
② What is future going to be like? → constraints
3 KAD – no rooms like down
Model = / Views / Statement of future.

Fail '61 → Tunnel diode ~~Ge~~ C
goto pair –
Model I – would get faster, but diodes would get faster at same rate!
Transistors – No one worked on diode
U. of IM. / Carlyle

Fail Make a C on magnetic core switches!
add diodes, add transistors .., throw away cores and replace with transistors

T

- Early 70's • Micros (Didn't go ahead with a mP/0) Each C knew not tenacles.
  74 - Pair for voice Sold it.
→ Networks •
→ Cambridge Ring — built on Dept. funds, worked to easy.
- very wide bw / very low cost /
- Ethernet = same view of future.

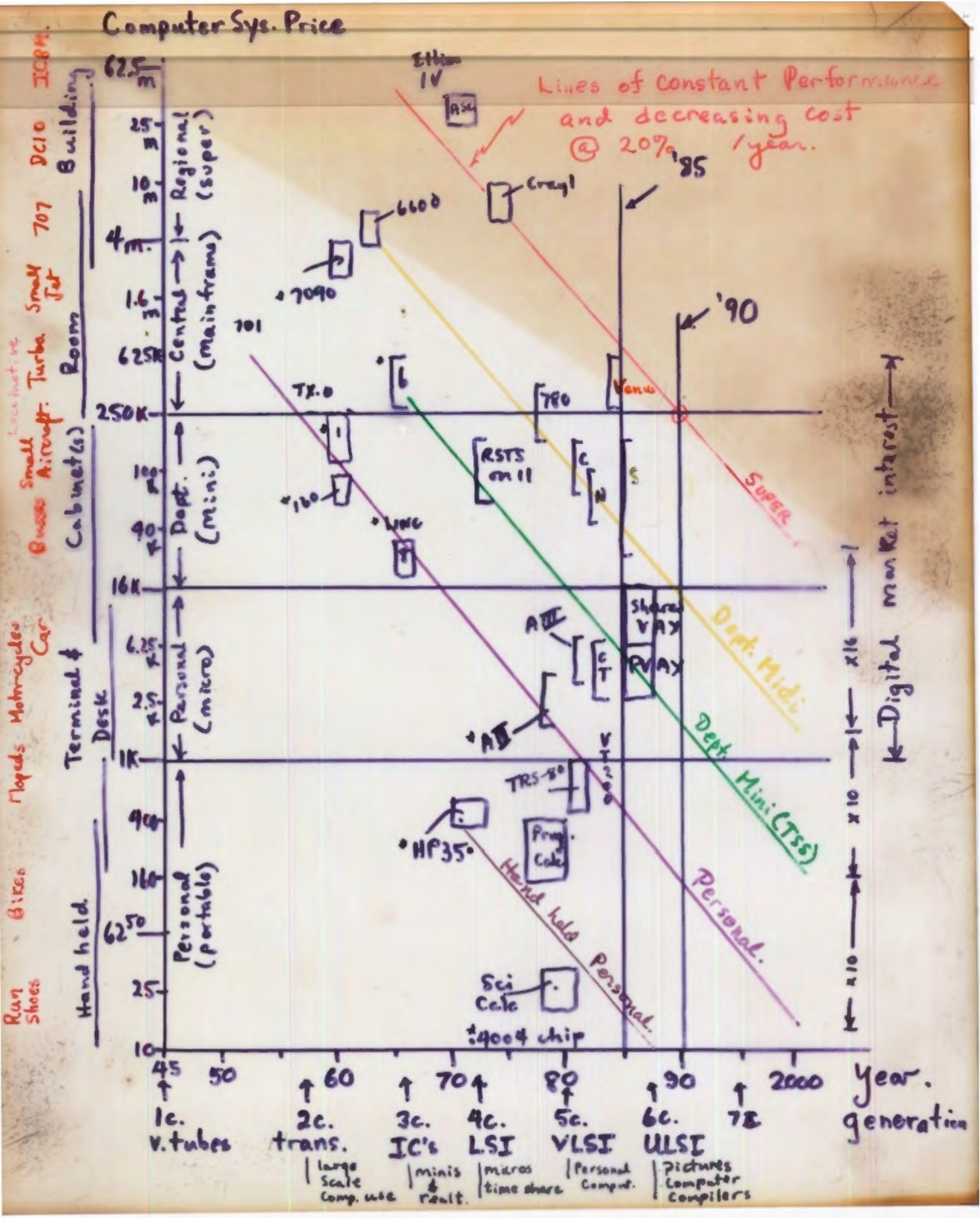
Conference on subject.
Way to look at Dist. computing.
⇒ Whole new style of C. Servic!

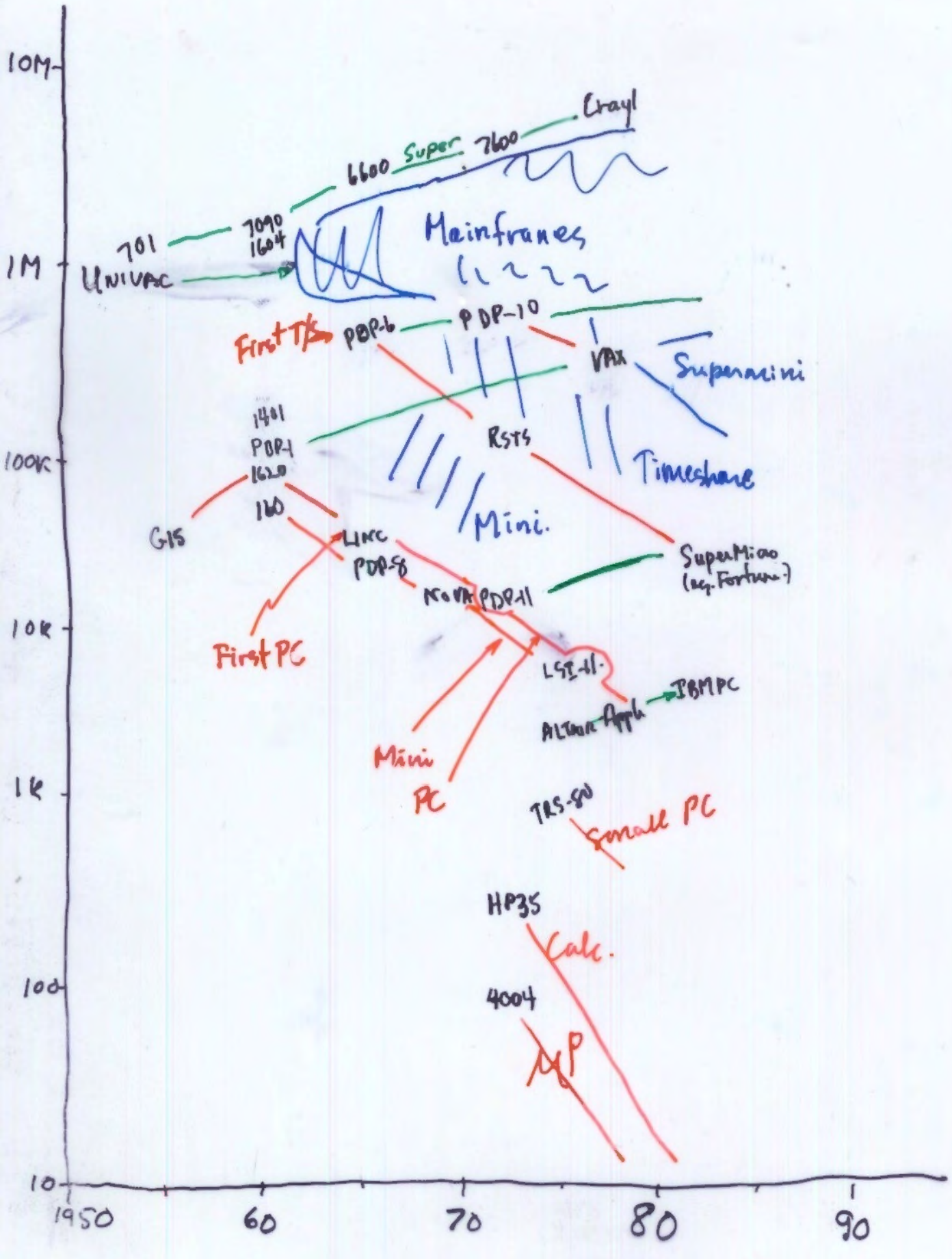
Can pretend that somthy will be true! Released energy for research.
Xerox pretended that powerful PC were low cost. gave to people. Developed User Server concept, Spectacularly succesful among CS Community.
People began to believe this...
& Existence escalated expectations!
Unis believed that there was a whole area of res. on PC's... not research.
Cambridge → Built up a thought to me 2 C's when 1 was enough.
Reliability →

- Authentication server
- Relax constraints → let's dream

NAME
Co./Address
IEEE MEMBER

SEPT 23, 1981 - WORK SECTION + COMPUTER


Computer Sys. Price
Lines of constant Performance and decreasing cost @ 20%/year.
'85
'90
Super
Dept. Midi
Dept. Mini (TSS)
Personal
Hand held Personal
Digital market interest
x16
x10
x10
Year.
generation
45
50
60
70
80
90
2000
1c. v. tubes
2c. trans.
3c. IC's
4c. LSI
5c. VLSI
6c. ULSI
7c
large scale Comp. use
minis & realt.
micros time share
Personal Comput.
pictures Computer Compilers
Hand held
Terminal & Desk
Personal (portable)
Personal (micro)
Cabinet(s)
Dept. (mini)
Central → Regional (super)
Room
Building
625
250
16K
1K
62.5
25
10
4
1.6
.625
.25
.16
.04
.01
Ethos IV
ASC
Cray1
6600
7090
701
TX.0
PDP
Venus
RSTS on 11
VAX
PMAX
ATT
TRS-80
HP35
Prog. Calc
Sci Calc
4004 chip
Run shoes
Bikes
Bicycles
Motorcycles
Car
Buses
Small Aircraft
Turbo
Locomotive
Small Car
707
DC10
ICBM


10M
1M
100K
10K
1K
100
10
1950
60
70
80
90
Cray!
6600
Super
7600
701
UNIVAC
7090
1604
Mainframes
First T/S
PDP-6
PDP-10
VAX
Supernini
1401
PDP-1
1620
160
RSTS
Timeshare
G15
Mini.
LINC
PDP-8
SuperMicro
(eg. Fortune)
PDP-11
First PC
LSI-11
IBM PC
Mini
PC
TRS-80
Small PC
HP35
Calc.
4004
μP

COMPUTER GENERATIONS

- o A CONCURRENCE OF:
  - TECHNOLOGY
  - NEED
  - USE
  - STRUCTURE
- o GENERATION UNDER DEVELOPMENT TODAY IS THE FIFTH

GENERATION	NEED	USE	STRUCTURE
I. ELECTRONIC (MAGNETIC) 1945	DEFENSE	WAR MACHINE CONTROL	EDVAC, IAS WHIRLWIND, IBM 605
II. TRANSISTORS 1958	SPACE/SCIENCE	AIR DEFENSE AND CONTROL ENGR. AND SCIENTIFIC EDUCATION	TX-0, IBM 7090 ATLAS, STRETCH
III. INTEGRATED CIRCUITS 1966	TRANSPORTATION FLOW CONTROL AND WELFARE	PROCESS CONTROL AND SOCIAL ACCOUNTING	PDP-8, IBM 360 PDP-6, CDC 6600
IV. LSI 1972	ECONOMIC MODELS AND REAL TIME CONTROL	INTERACTIVE COMPUTING COMPUTERS FOR LOGIC	INTEL 4004, 8008, PDP-11 (RSTS) CRAY 1

The administrator from the previous example wants a file system on a cartridge disk. Cylsize is 2 x 8 x 2 = 32. The administrator inserts a blank disk in the drive enters the following commands. The system administrator's input is in boldface, the computers responses in roman.

```
# /etc/iv /dev/fp@1@ /usr/lib/iv.work/pd.offline
# /etc/mkfs /dev/fp@11 9776 1 32
```

Mounting a File System

Every file system must be mounted in order to be used; this gives the file system a place in the CTIX file hierarchy. The **mount** command mounts a file system:

/etc/mount /dev/fp@d p dir r

where

d indicates the disk, as in the **mkfs** command.

p indicates the slice, as in the **mkfs** command.

dir is the name of an empty directory. Subsequent references to dir will actually be to the root directory of the newly mounted file system; this gives user normal access to any files on that file system.

This directory can be on the root file system or it can be on another mounted file system. But the directory's file system must be already mounted.

r controls access to the file system. If r is **-r**, the file system is mounted read-only: files in the file system can be read, subject to normal permission rules, but cannot be modified, created, or deleted. If r is missing, the file system is mounted read-write: all files in the file system can be read, modified, created, or deleted, subject to normal permission rules.

Without any arguments:

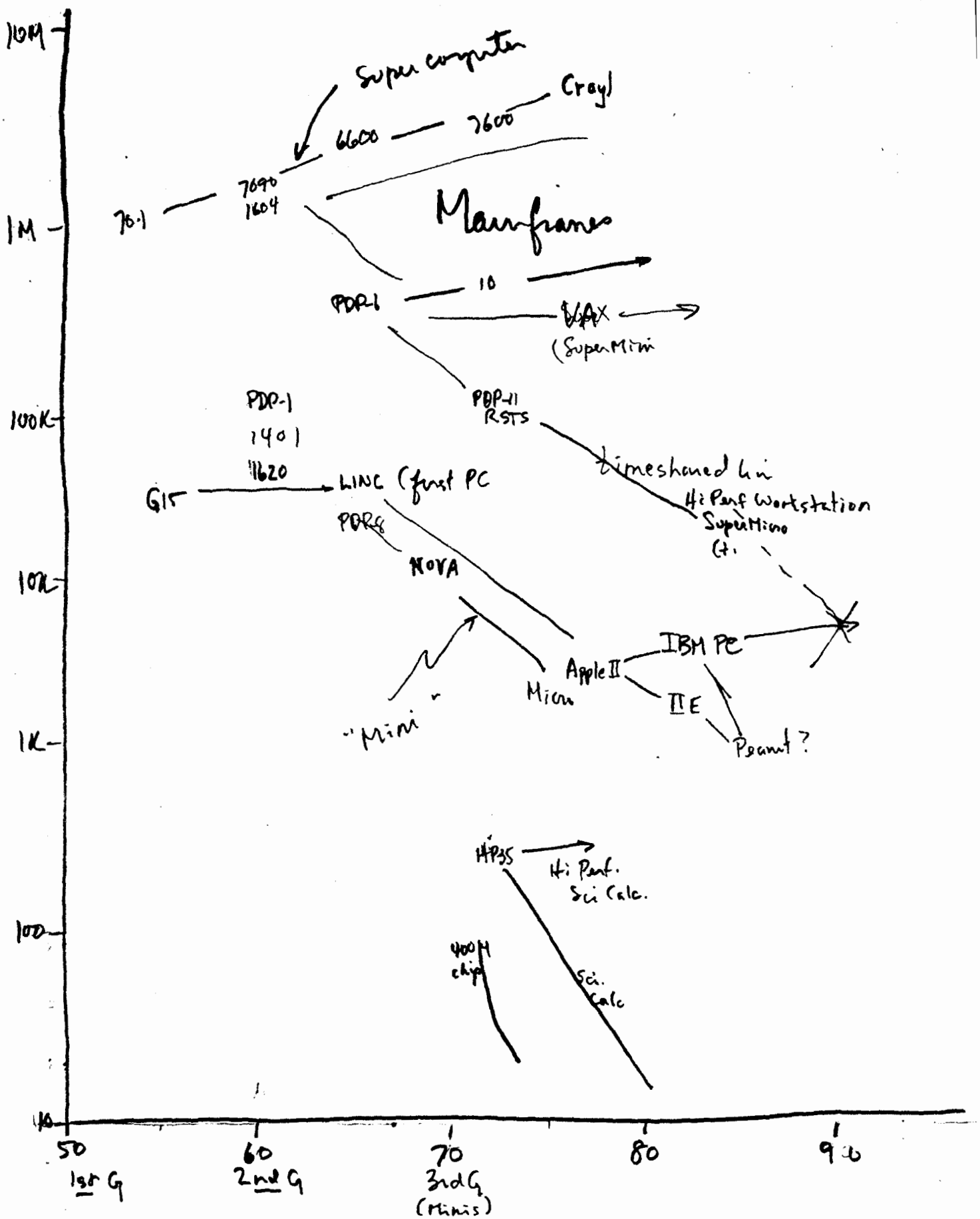
/etc/mount

the program displays a list of currently mounted file systems.

A **umount** undoes a **mount**:

/etc/umount /dev/fp@dp

where


10M
1M
100K
10K
1K
100
10
Super computer
Cray1
6600
7600
7090
1604
Mainframes
10
PDP-1
VAX
(SuperMini
PDP-11
RSTS
PDP-1
1401
1620
GIT
LINC (first PC
timeshared Lin
Hi Perf Workstation
SuperMicro
PDP8
NOVA
Apple II
IBM PC
IIE
Peanut?
HP35
Hi Perf.
Sci Calc.
400M
chip
Sci.
Calc
50
1st G
60
2nd G
70
3rd G
(Minis)
80
90

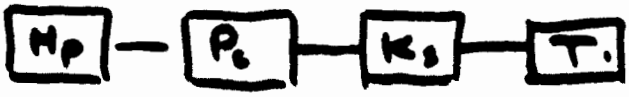
Some Lessons

- Understand before building
- operate on (naive - simple - elegant - general - kludge) spectrum.
- Watch out for Conway's law —
  - "People build C's like their Org's."

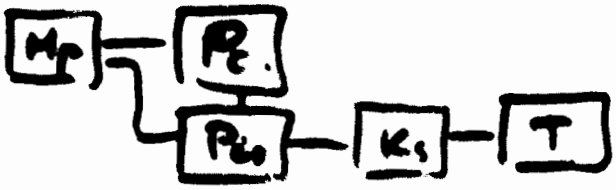
eg. UNIBUS, SNA, ARPAnet,

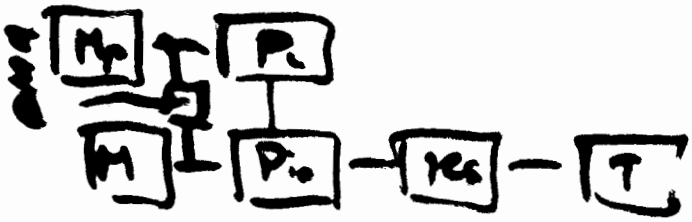
- Conway's Law "turns" Wheel of Reincarnation

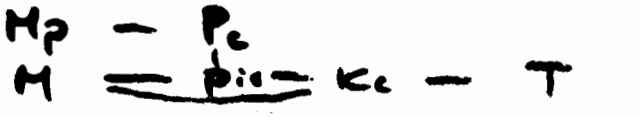
in Graphics, Communication, Database, ... Computation etc.

1. 

2. 

3. 

4. 

5. 

To: Bruce Stewart, Bob Travis, Gilmore, Tyle, Dickson, BJ, Daley, Buzz Brooks, Vlach, D. Stanwood + Ret

Slides of MK Talk on OA/OOF/WPS/E-15

Copy to Corben, Steele, Fuller

Delagi + Ref

Fiji

Gosden

5/28/...

GBell

A PROFESSION BASED SYSTEM

(FOR LARGE ORGANIZATIONS)

- IS A HIERARCHY OF COMPUTERS (INCLUDING PERSONALS?)

- PROVIDES BENEFIT NOW THROUGH GENERIC CAPABILITIES FOR TEXT, FILING AND COMMUNICATIONS

- REQUIRES ATTENTION TO HUMAN ENGINEERING, AND COST OF CAPABILITY (INCLUDING OWNERSHIP)

The slides I mentioned

Hierarchy of ...

OFFICE OF FUTURE (OOF)

USE OF EQUIPMENT WHICH ALLOW A DRASTIC RESTRUCTURING OF OFFICE WORK, AMONG A DIFFERENT COMPOSITE WORK FORCE.

PARAPHRASING THE APRIL 80 COOPERS AND LYBRAND NEWSLETTER: "A SECRETARY USES THE EQUIPMENT, IT'S OA; AND IF WE ALL USE IT, IT'S OOF".

OFFICE AUTOMATION - OA - EVOLUTIONARY USE OF WORD PROCESSING AND ELECTRONIC MAIL EQUIPMENT TO IMPROVE OFFICE PRODUCTIVITY, WHERE:

1. WORD PROCESSING EQUIPMENT, EVOLVING TO USER TYPESETTING REPLACES, TYPEWRITERS, SNOPAKE, AND COPIERS.

2. ELECTRONIC MAIL REPLACES COPIERS AND POST PEOPLE, FAX, TWX/TELEX AND INTRA-ORGANIZATION ELECTRONIC TORN TAPE MESSAGE SWITCHES.

3. COMMON CARRIER PACKETNETS EVOLVE FOR INTER-ORGANIZATIONAL MESSAGE AND DATA SWITCHING.

4. ELECTRONIC FILING REPLACES PAPER FILES.

5. DIRECT SOURCE FORMS ENTRY AND TRANSMISSION REPLACES MODERN KEYPUNCH.

6. LOCALIZED LIST PROCESSING FOR REPORTS REPLACES CENTRAL, DATA PROCESSING.

FUNCTIONAL LEVELS OF A PBS ROOT (HARDWARE, OS, LANGUAGES, NETWORKING AND DATA BASES)

GENERIC MODULES FOR COMMUNICATIONS WITHIN AN ORGANIZATION

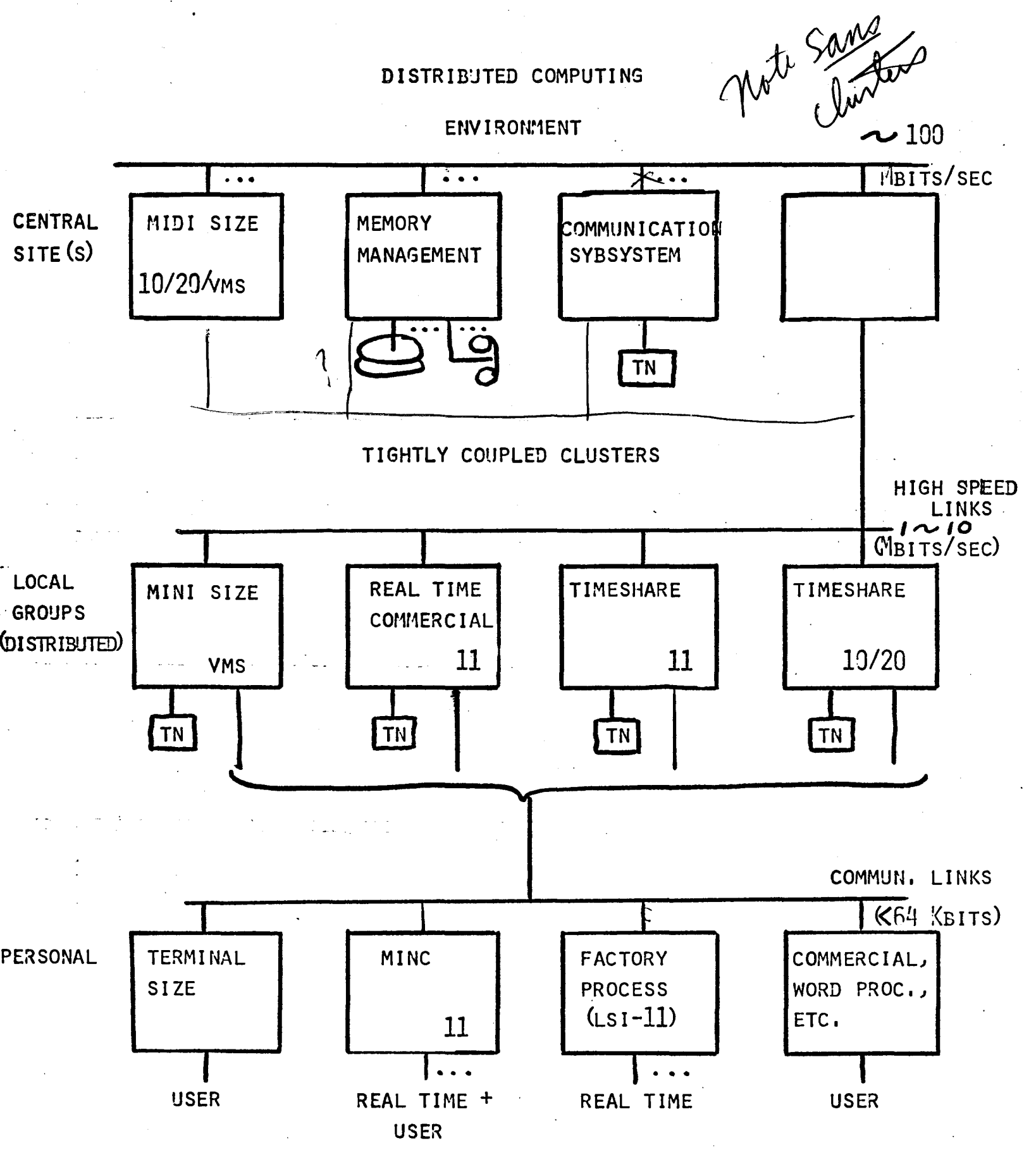
- TEXT AND GRAPHICS PROCESSING AND "USER TYPESETTING"
- FILING CABINETS FOR TEXT, MESSAGES, FORMS, ETC.
- ELECTRONIC MAIL AND COMPUTER CONFERENCING
- OFFICE PROCEDURES AND FORMS PROCESSING
- INTERFACE TO NON-COMPUTER COMMUNICATIONS (FAX, OCR, INTERFACE TO OTHER ORGANIZATIONS, TWX, TYPESETTERS, TELEPHONE)

GENERAL PROFESSIONAL DISCIPLINE MODULES (E.G. ENG.)

DEPARTMENTAL PROFESSIONAL DISCIPLINE (E.G. ELEC. ENG.)

COMPARTMENTAL PROFESSIONAL DISCIPLINE (E.G. RF CKT. DESIGN)

} these follow educational org. structures: colleges, depts, sub-depts



TN = TERMINAL NETWORK--CONNECTS SIMPLE TERMINALS, GATEWAY TO OTHER NETWORKS, MOST PERIPHERALS, AND PERSONAL COMPUTERS, AND PROCESS COMPUTERS

LARGE, CENTRALLY OPERATED FACILITIES PROVIDE:

LARGE, SHARED DATA BASES AT LOWEST COST/BYTE (THROUGH ECONOMY OF SCALE OF LARGE DISKS)

ARCHIVAL OF PERSONAL FILES

PROGRAMS FOR SPECIAL NON-COMPUTER OWNER COMMUNITIES

VERY HIGH PERFORMANCE PROCESSING

COMMUNICATIONS AMONG THE ENTIRE COMMUNITY AND GATEWAYS TO INTERNETS AND PACKETNETS

COMMUNICATIONS ORIENTED SERVICES (E.G. MAIL, TELECONFERENCING)?

SPECIAL FACILITIES SUCH AS TYPESETTING

GROUP CENTERED COMPUTERS PROVIDE:

RELATIVELY COST-EFFECTIVE FILE STORAGE FOR ITS COMMUNITY

FACILITIES BEST MATCHED TO COMMUNITY

RELATIVELY HIGH PERFORMANCE PROCESSING

COST-EFFECTIVENESS THROUGH GROUP SUPPORTED PROGRAMS

PERSONAL COMPUTERS PROVIDE:

PERSONAL DATA BASES AND SECURITY

FAST RESPONSE TO RELATIVELY COMPLEX REQUESTS (E.G. EDITING)

PROGRAM ENVIRONMENT FOR ENTERING AND GETTING INTO PRODUCTION

USER VIEW GOALS

LIVE AND WORK ON THE MACHINE

CONSISTENCY AND COMPATIBILITY ACROSS KEYBOARDS, SYNTAX/SEMANTICS, FILES, COMMUNICATIONS...PERMITTING TRUE DP HOMOGENETS AND HETEROGENETS

"CAMERA INSTRUCTION BOOK-LIKE" MANUALS PERSONALIZABLE WITHOUT PROGRAMMING CONTEXT DEPENDENT EDITING FOR TEST, TYPESETTING, MAIL, FILE CABINET, PICTURES FORMS, TABLES, ETC.

dictation of music
text
individual

IMPLEMENTATION DESIGN GOALS

NO ASSEMBLY LANGUAGE PROGRAMMING

CONSISTENCY AND COMPATIBILITY FOR FORMING DP HOMOGENETS AND HETEROGENETS

ALL PROGRAMS DRIVEN FROM: FILES, TERMINALS, TEXT, ANY OTHER PROGRAM USING VARIOUS PROGRAM MODELS (TP, PIPES, SINGLE PROCESS, AND NETWORK)

goal 1

must we or can we have all these forms?

BUILT IN FOREIGN LANGUAGES

TYPED DATA FOR FILES, FORMS AND PROGRAMS

COST OF CAPABILITY UNDERSTANDING

PERSONAL OR SHARED?

GIVEN: ECONOMY OF SCALE, EXCEPT DISKS AND SWITCHING DISAPPEARING. ALL MEMBERS OF HIERARCHY ARE NEEDED.

STRATEGY: MOVE FROM GENERAL TO SPECIFIC AND PERSONAL

PROBLEMS: DISTRIBUTING AND SHARING PROGRAMS, PROGRAMMING AND DATA. USING.

PBS (1985) GENERIC CAPABILITIES:

WPS: FULL PAGE, VOICE INPUT, GRAPHICS, PROFESSION DEPENDENT. ARCHIVES ANY PART AND ALL DOCUMENTS.

USER-TYPESETTING: YES

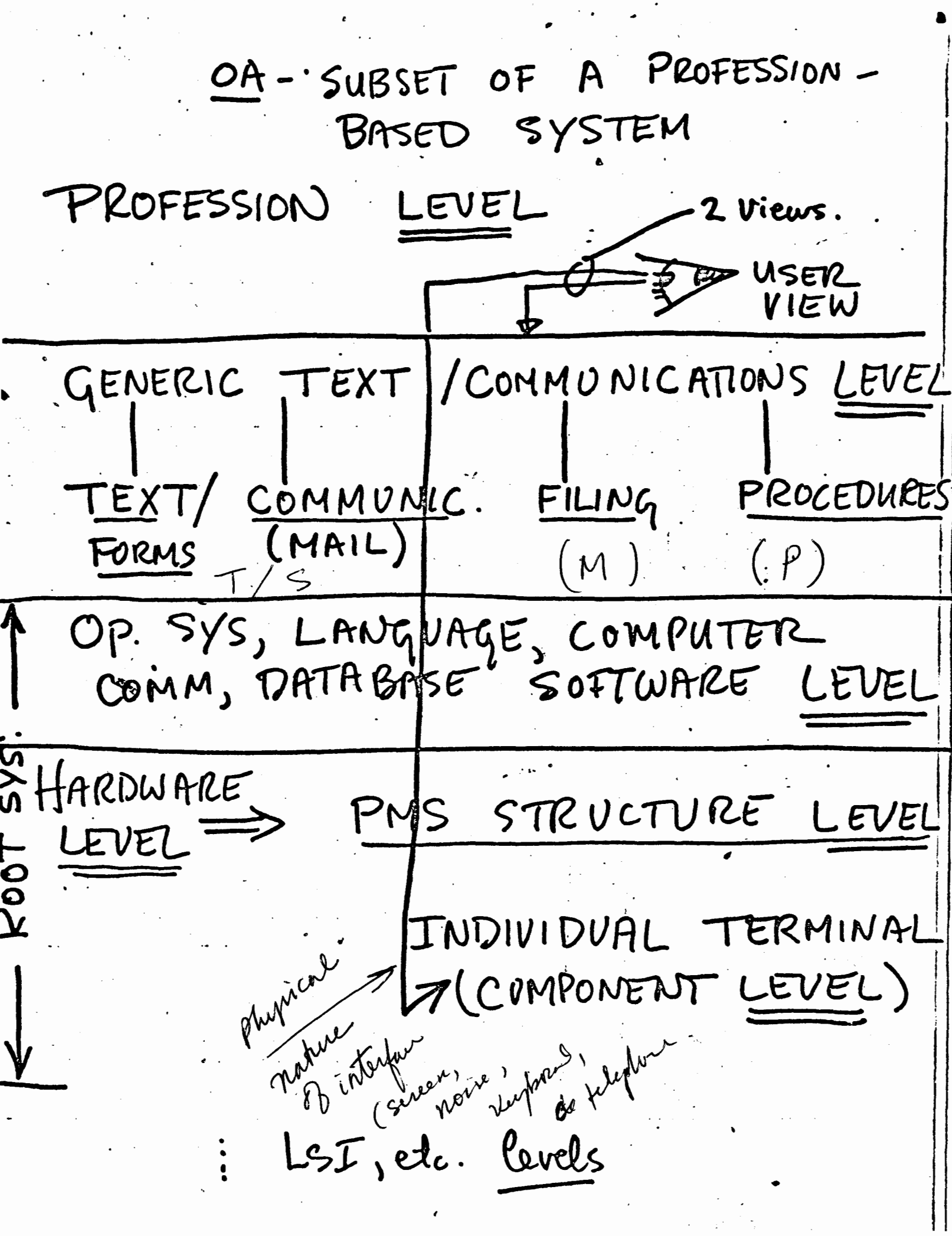
FILE CABINET: RETRIEVE BY MULTIPLE KEYWORD. SEARCH FOR CONTENT.

MAIL SYSTEMS: VOICE. COMPUTER CONFERENCING WITH PERSONAL VIDEO CONFERENCING IN SIGHT.

COMMUNICATIONS: INTERNETS, PACKETNETS, AND NON-COMPUTER NETS (E.G. PHONE, FAX, TWX, OCR FOR OLD DOCUMENTS).

OFFICE PROCEDURES: NUMEROUS

OA - SUBSET OF A PROFESSION - BASED SYSTEM



PHYSICAL STRUCTURE PARAMETERS

- COST (PURCHASABILITY, MAINT., ETC.), PERFORMANCE, RELIABILITY

- SECURITY, ATTITUDES ABOUT SHARING

- AESTHETICS/APPEARANCE

- ENVIRONMENTAL ADAPTABILITY

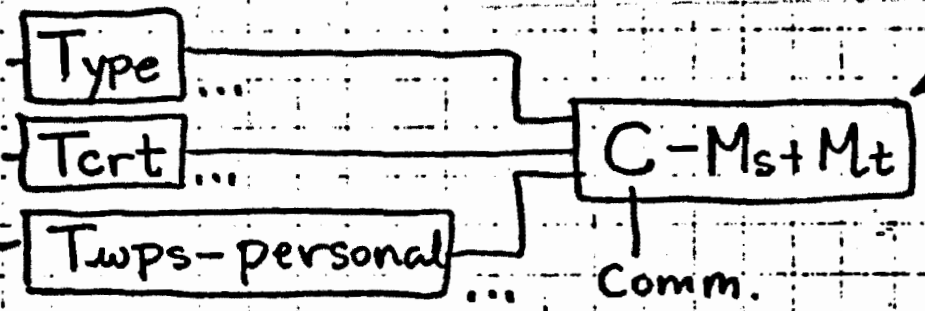
  (1). UNOBSTRUSIVE

  (2). DOMINATES & BECOMES (CREATES) THE ENVIR. (EG. WORK SPACE, NOISE, LIGHTING, FILING, DOCUMENTS, PHONE

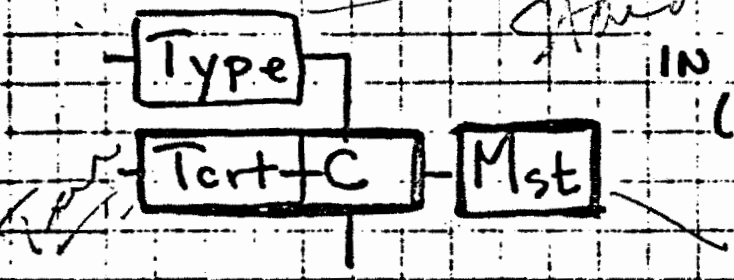
- COMMUNICATION WITH: OTHERS, OTHER WPS, DP,...

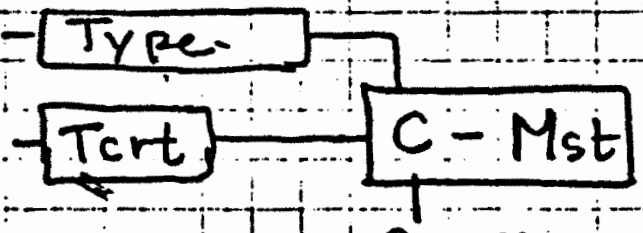
PHYSICAL STRUCTURES ALTERNATIVES

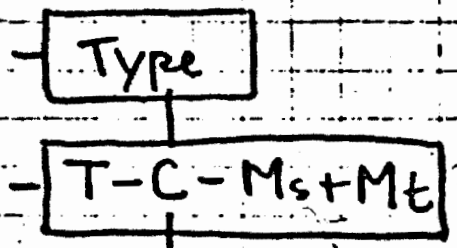
- SHARED: CENTRAL AND GROUP



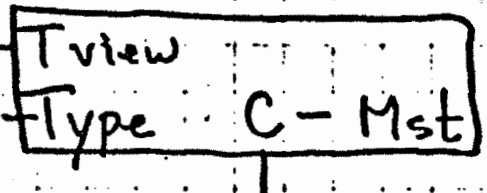
- PERSONAL:







IN Typewriter IV.



5/20/80

PRIME OA 5/80

WP

TEXT CREATION & EDITING

FILING & RETRIEVAL

BOILERPLATE LIB.

LIST PROC.

ADV. FEATURES:
PROOFING, HYPHENATE, TRANSLATE

MGMT COMM. & SUPPORT

EMAIL
- CREATE NOTES & MEMOS
- DIST.
- ANNOTATE
- ACK. & SECURITY CODES

CORRESP. MGMT
- FILE, RETRIEVE, ARCHIVE
- FILE CODES & REPORTS

MGMT SUPPORT
- INTRAY, CALENDAR, SCHEDULING, TICKLER FILE, TELEPHONE LOG

MGMT INFO.
- QUERIES, REPORTS, MODELLING, APPL.

COMPATIBILITY

EDITING SYNTAX

- WPS, EMS, FORMS TEXT, COMMANDS, USER TYPESET

FILES

- PERSONAL & SHARED WPS
- EMS
- INTERFACE TO DATA IN SYSTEM W/O CONVERSION (I.E. PROGRAMS)

COMMUNICATIONS

- DECNET ETC. VIA SYSTEM CALLS

PERFORMANCE/USE UNDERSTANDING

1981 GOALS

GENERIC LEVEL TEXT/COMMUNICATIONS PRODUCT INTRODUCTION

- PLAN, SPECIFY, DESIGN AND UNDERSTAND (I.E. MASTER) THIS LEVEL FOR NEXT 5 YEARS → ADDRESS PRODUCTIVITY (COST TO USE)
- DECNET COMMUNICATIONS WITH VIRTUAL TERMINALS AND COMMON PROTOCOLS VIA STANDARD SYSTEMS
- HIGH QUALITY, COMPATIBLE WPS BASE
  - STABILIZE THE 2XX MULTI-USER SYSTEM?
  - BUILD A FIRM BASE FOR 278 AND ENHANCE IT
  - BUILD A MULTI-USER BASE ON WPS COMPATIBLE EDT FOR RSTS AND VMS
  - BUILD A SINGLE USER 11 SYSTEM ON SAME EDITOR
  - LIST PROCESSING, SORT AND MATH.
  - GRAPHICS (PROTO)
  - DICTIONARY AND SPELLING (PROTO)

(WPS FILING ON ALL SYSTEMS)
(WPS COMM. " " ")

GB1.S4.13
5/23/80

- USER TYPESETTING BREADBOARD
- USER FORMS CREATION AND EDITING (VS LISTS?)
- FILING
  - PUT DOCUMENT HOLDER FOR 278 ON 11/M, RSTS AND VMS
  - MAIL
  - BASE FOR FORMS HOLDER
  - RELATIONAL
- QUERY BY FORMS (PROTO) USING CATS AND FORMS EDITOR
- VOICE MESSAGE STORAGE (PROTO)
- ELECTRONIC MAIL (EMS' COMPATIBLE WITH WPS) - TEST AT DEC
  - VMS (AND POSSIBLY RSTS)
  - VOICE READ MAIL (PROTO)
  - FORMS SIGNATURE ROUTING AND APPROVAL (PROTO)
- OFFICE PROCEDURES (PROTO)
  - TICKLER, SCHEDULING, PHONE MANAGEMENT

The Compatible Office System.

- Across functions
  - Word & Information Processing to "run" the office
  - Typesetting
  - Communications via Electronic Mail
  - Personal Computing
  - Corporate & Departmental TP/DP
  - Other functions; including Technical
- Across "Types" & Location
  - Personal, Department/group, Corporation
- Over time (past, present, future DEC).
- To other suppliers
- With Office Environment → physical Design

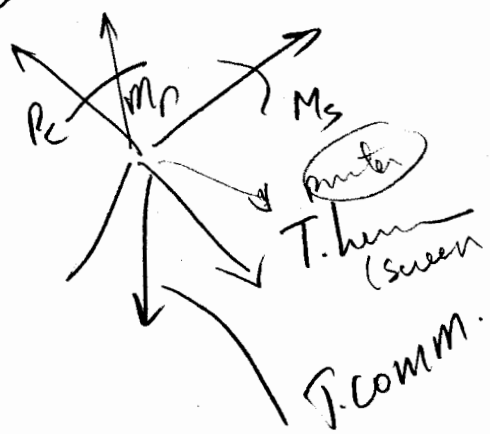
LANs & remote LANs (Global Net.)

7 Different Views

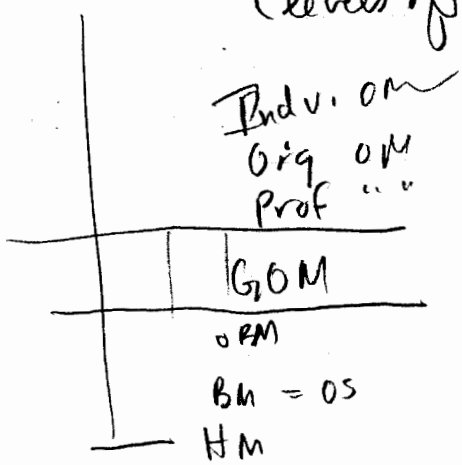
- Structure (Lof)
- Levels of interpretation
- Packaging
- Marketplace (by price classes)
- Application (Discipline)
- Practice of Design
- Characterization of CD (Blaauw).

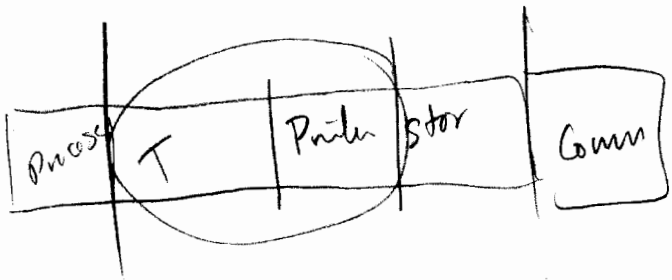
"System" Function from C perspective

(4)d



~~Cor~~ Prof. Intelligence (levels of Int





→ Here - Ker -

→ Exciting

Entering 3rd. Gen.

→ first components - electronic typewriter expt
- breadboard. Expensive typewriter, Teco. 72

→ 2nd WPS, timeshared text, seperate mail, 72
(word) automated rubbish. LARP

→ 3rd Integrated
Text / DP / Typesetting / Mail
→ Distributed + LANs

→ 4th Evolution to — voice, Graphics

- We're committed. You have to make it happen.

. It is a Generic Product → ~~Get~~ t others can evolve from it. I'd rather just provide it.

. We screwed up in not getting it to everyone!
attendy & competitiveness

→ Delighted with All-In-One for example.

The first, application I've seen that builds on VAX design Principles AND extends those.

| Brings up another conflict. Internally.

Good work.

Great! Basic products just have to be that reliable

PIONEERS IN:

OPERATING SYSTEMS (DEC 10/20, RT, RSTS, RSX, VMS)

SINGLE USER OPERATING SYSTEMS. PDP-6 WAS BASE FOR OUR INTERACTIVE PROGRAMMING EXPERIENCE. (1965)

RT WAS BASE FOR CP/M PERSONAL COMPUTER SOFTWARE (1974)

RSTS WAS OUR MAIN MINI- OPERATING SYSTEM FOR 11'S (1972)

EDITORS FOR PROGRAMS WERE FORE-RUNNERS OF TEXT EDITORS (15 years)

WORD PROCESSING- WE WERE THERE VERY EARLY (1975)

COBOL AND BASIC LANGUAGE (1975, 1972)

FILES AND DATABASES (1970)

OFFICE OF FUTURE (OOF)

USE OF EQUIPMENT WHICH ALLOW A DRASTIC RESTRUCTURING OF OFFICE WORK, AMONG A DIFFERENT COMPOSITE WORK FORCE.

PARAPHRASING THE APRIL 80 COOPERS AND LYBRAND NEWSLETTER: "A SECRETARY USES THE EQUIPMENT, IT'S OA; AND IF WE ALL USE IT, IT'S OOF".

OFFICE AUTOMATION - OA - EVOLUTIONARY USE OF WORD PROCESSING AND ELECTRONIC MAIL EQUIPMENT TO IMPROVE OFFICE PRODUCTIVITY, WHERE:

1. WORD PROCESSING EQUIPMENT, EVOLVING TO USER TYPESETTING REPLACES, TYPEWRITERS, SNOPAKE, AND COPIERS.

2. ELECTRONIC MAIL REPLACES COPIERS AND POST PEOPLE, FAX, TWX/TELEX AND INTRA-ORGANIZATION ELECTRONIC TORN TAPE MESSAGE SWITCHES. FIRST USE FOR INTER-OFFICE MAIL.

3. COMMON CARRIER PACKETNETS EVOLVE FOR INTER-ORGANIZATIONAL MESSAGE AND DATA SWITCHING.

4. ELECTRONIC FILING REPLACES PAPER FILES.

5. DIRECT SOURCE FORMS ENTRY AND TRANSMISSION REPLACES MODERN KEYPUNCH (I.E. FORMS ENTRY)

6. LOCALIZED LIST PROCESSING FOR REPORTS REPLACES CENTRAL, DATA PROCESSING.

A PROFESSION BASED SYSTEM (PBS)
(FOR LARGE ORGANIZATIONS)

- IS A HIERARCHY OF COMPUTERS (INCLUDING PERSONALS?)
- PROVIDES BENEFIT NOW THROUGH GENERIC CAPABILITIES FOR TEXT, FILING AND COMMUNICATIONS
- REQUIRES ATTENTION TO HUMAN ENGINEERING, AND COST OF CAPABILITY (INCLUDING OWNERSHIP) → NEW METRIC:
  TOTAL COST-TO-USE

FUNCTIONAL LEVELS OF A PBS ROOT (HARDWARE, OS, LANGUAGES, NETWORKING AND DATA BASES)

GENERIC MODULES FOR COMMUNICATIONS WITHIN AN ORGANIZATION

- TEXT AND GRAPHICS PROCESSING AND "USER TYPESETTING"
- FILING CABINETS FOR TEXT, MESSAGES, FORMS, ETC.
- ELECTRONIC MAIL AND COMPUTER CONFERENCING
- OFFICE PROCEDURES AND FORMS PROCESSING ←
- INTERFACE TO NON-COMPUTER COMMUNICATIONS (FAX, OCR, INTERFACE TO OTHER ORGANIZATIONS, TWX, TYPESETTERS, TELEPHONE)

GENERAL PROFESSIONAL DISCIPLINE MODULES (E.G. ENG.)

DEPARTMENTAL PROFESSIONAL DISCIPLINE (E.G. ELEC. ENG.)

COMPARTMENTAL PROFESSIONAL DISCIPLINE (E.G. RF CKT. DESIGN)

METHODS/LEVELS FOR

- ORGANIZATION
- INDIVIDUAL (PERSONALIZATION)

USER VIEW GOALS

LIVE AND WORK ON THE MACHINE

CONSISTENCY AND COMPATIBILITY ACROSS KEYBOARDS, SYNTAX/SEMANTICS, FILES, COMMUNICATIONS...PERMITTING TRUE DP HOMOGENETS AND HETEROGENETS

"CAMERA INSTRUCTION BOOK-LIKE" MANUALS PERSONALIZABLE WITHOUT PROGRAMMING CONTEXT DEPENDENT EDITING FOR TEXT, TYPESETTING, MAIL, FILE CABINET, PICTURES FORMS, TABLES, ETC.

SYSTEM TEACHES ITS USE

SYSTEM PROVIDES FOR NOVICE ... EXPERT USER.

DICHOTOMY

PHYSICAL SYSTEM

CLOSETABLE OR IN A DESK IF QUIET ENOUGH

Pc + Mp (1 MBYTE) + Ms (100 MBYTE; FIXED)...NOTE 1 FILE CABINET = 32 MBYTES

2 - 4 X T.CRT(1 PAGE B/W, OR COLOR)
WITH ABILITY TO REMOTE AT REDUCED BANDWIDTH

T(LETTER QUALITY AND SCREEN PRINTER)

T(TELEPHONE DIALER, PHONE ANSWERER, VOICE OUTPUT)

L(SYSTEMS OF THE SAME TYPE) FOR:
COMMUNICATION, EXECUTING OTHER PROGRAMS, TELE- AND COMPUTER-CONFERENCING, ETC.

L(CENTRAL SYSTEM) FOR:
- FILING, PRINTING, TYPESETTING, AND SLIDE MAKING
- DISTRIBUTION OF DOCUMENTS TO PEOPLE NOT ON SYSTEM
- ACCEPTANCE OF DOCUMENTS FROM PEOPLE NOT ON SYSTEM
- EMS'S, AND OTHER SYSTEMS

T(VIDEO AND VOICE I/O) - LARGE SCREEN FOR TELECONFERENCING)

STRUCTURE OF PROFESSION MODULES AND USE DEPENDENCIES

USE IS A FUNCTION OF THE PRODUCT OF:

PROFESSIONAL DISCIPLINE/PROJECT DISCIPLINE

X ORGANIZATION (BUYER, SELLER, KNOWLEDGE SELLER, CONTROLLER/GOV'T)

PERSON'S ROLE:

X MKT.-, MFG.- TECH- GATEKEEPER, IDEA GENERATOR/CREATIVE SCIENTIST, ENTREPENEUR, COACH/SPONSOR, PROBLEM SOLVER } EXAMPLE OF ENGINEERING ENVIRONMENT

(...NOTE VARYING DEGREE OF COMMUNICATION, ANALYSIS, NEED TO ACCESS AND PRESENT DATA IN EACH ROLE

X POSITION IN ORGANIZATION HIERARCHY

X TIME OF FISCAL YEAR AND OTHER PROCESSES (E.G. PLANNING)

X TIME OF TRANSACTION (PROCESS STATE)

E.G. PROJECT (PROPOSAL, DESIGN, ANNOUNCEMENT, DEATH) ETC.

DESIGN GOALS

FACILITIES [illegible] MOSTLY LIVE AND WORK VIA THE MACHINE

SELF DOCUMENTING [illegible] WITHOUT HELP FILES
[illegible] A CAMERA INSTRUCTION BOOK)

MINIMUM NUMBER OF EXTERNAL DOCUMENTS TO READ IS MEASURE. OF

[illegible] OF INTERFACE... [illegible]-LIKE, FRAMES LOOK-ALIKE,
[illegible], NO 3 CHAR ABBREVIATIONS
[illegible] NUMBERS, COMMANDS, ETC. ARE [illegible]

[illegible] THE END USER EXCEPT IN THE PROGRAMMER'S SYSTEM

[illegible] OF EDITING, [illegible] IN THE CONTEXT OF USE:
TEXT, TYPESET FORMAT, FILEBOX, PICTURES, FORMS, TABLES, ETC

ALL PROGRAMS CAN BE DRIVEN FROM: FILES, TERMINALS, TEXT WITH
[illegible] [illegible] MODES!

PROGRAMS [illegible] AS [illegible] MODEL [illegible] IN
[illegible]

A MINIMUM NUMBER OF SPECIAL FILE TYPES--VIRTUALLY ANY PROGRAM CAN
BE DRIVEN BY OUTPUT OF ANOTHER PROGRAM

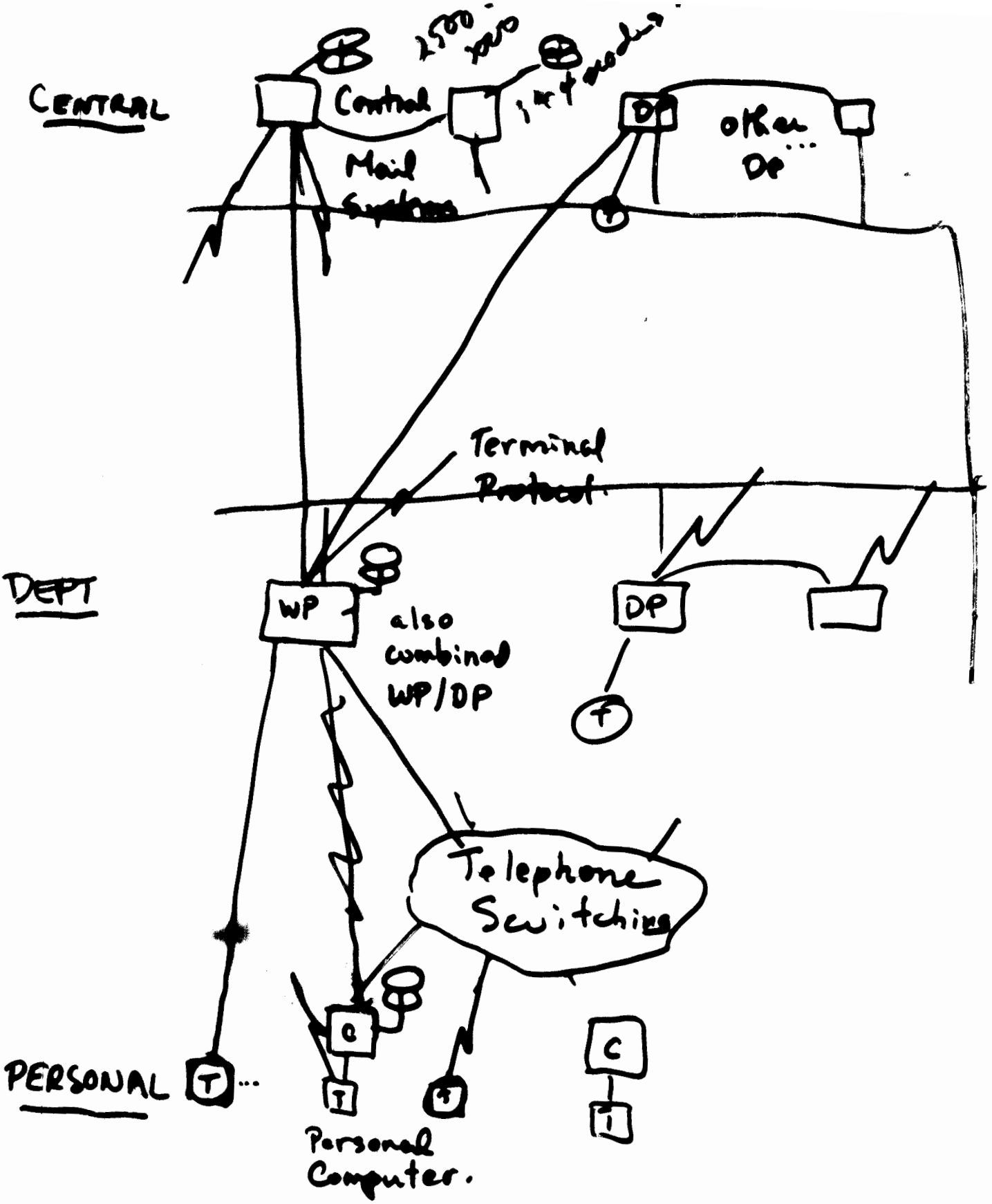
ABSOLUTELY EXTENDABLE TO FOREIGN LANGUAGES

NO ASSEMBLY LANGUAGE, [illegible] REVIEWED

HIGH LEVEL LANGUAGE(S) - SPECIFIC TO PROBLEM CONTEXT?

COMPLETELY TYPED DATA FOR FILES, FORMS, AND PROGRAMS
SO THAT PROGRAMS DON'T TYPE IT IMPLICITLY

[illegible]


CENTRAL
Control
Mail
DP
DP
Terminal
Protocol
DEPT
WP
also
combined
WP/DP
DP
T
Telephone
Switching
PERSONAL
T
Q
T
T
C
T
Personal
Computer.

PBS (1985) GENERIC CAPABILITIES:

WPS: FULL PAGE, VOICE INPUT, GRAPHICS, PROFESSION DEPENDENT. ARCHIVES ANY PART AND ALL DOCUMENTS.

USER-TYPESETTING: YES

FILE CABINET: RETRIEVE BY MULTIPLE KEYWORD. SEARCH FOR CONTENT.

MAIL SYSTEMS: VOICE. COMPUTER CONFERENCING WITH PERSONAL VIDEO CONFERENCING IN SIGHT.

COMMUNICATIONS: INTERNETS, PACKETNETS, AND NON-COMPUTER NETS (E.G. PHONE, FAX, TWX, OCR FOR OLD DOCUMENTS).

OFFICE PROCEDURES: NUMEROUS

PERSONAL OR SHARED?

GIVEN: ECONOMY OF SCALE, EXCEPT DISKS AND SWITCHING DISAPPEARING. ALL MEMBERS OF HIERARCHY ARE NEEDED.

STRATEGY: MOVE FROM GENERAL TO SPECIFIC AND PERSONAL

PROBLEMS: DISTRIBUTING AND SHARING PROGRAMS, PROGRAMMING AND DATA. USING.

IMPLEMENTATION DESIGN GOALS

NO ASSEMBLY LANGUAGE PROGRAMMING → NEED FOR VERY HLL EXTENSIBLE BY USERS (e.g. ADA)

CONSISTENCY AND COMPATIBILITY FOR FORMING DP HOMOGENETS AND HETEROGENETS

ALL PROGRAMS DRIVEN FROM: FILES, TERMINALS, TEXT, ANY OTHER PROGRAM USING VARIOUS PROGRAM MODELS (TP, PIPES, SINGLE PROCESS, AND NETWORK)

BUILT IN FOREIGN LANGUAGES

TYPED DATA FOR FILES, FORMS AND PROGRAMS

COST OF CAPABILITY UNDERSTANDING

DISTRIBUTED PROCESSING MATCHES COMPUTER SYSTEMS TO NEEDS ON A GEOGRAPHICAL OR ORGANIZATIONAL BASIS, AND INTERCONNECTS INDIVIDUAL COMPUTER SYSTEMS INTO A SINGLE NETWORK.

THE OBJECTIVES OF DISTRIBUTED PROCESSING ARE:

1. TO ALLOW EFFECTIVE MATCHING OF RESOURCES TO NEEDS.

2. TO ALLOW BOTH LOCAL AUTONOMY AND CENTRAL CONTROL OF THE VARIOUS DISTRIBUTED PARTS.

3. TO PROVIDE AN EVOLVING, OPEN ENDED SYSTEM SO THAT THE DEVELOPMENT OF DISTRIBUTED PARTS CAN PROCEED AT THEIR OWN PACE IN A QUASI INDEPENDENT FASHION.

4. TO ALLOW PURCHASE AND INSTALLATION OF COMPUTER IN THE MOST TIMELY, COST-EFFECTIVE WAY, TAKING ADVANTAGE OF REDUCED (WITH TIME) HARDWARE COSTS.

5. TO BUILD ON AND COMMUNICATE WITH EXISTING, MORE CENTRAL SYSTEMS, FULLY DISPERSED SYSTEMS, AND EMERGING PERSONAL COMPUTERS.

6. TO PROVIDE COMPUTING, CONTROL AND STORAGE OF INFORMATION NEAREST THE NEED.

DISTRIBUTED PROCESSING IS THE MATCHING OF COMPUTER RESOURCES TO NEEDS-ON A GEOGRAPHICAL OR ORGANIZATIONAL BASIS - AND THE INTERCONNECTION OF THESE RESOURCES TO FORM A SINGLE, COST-EFFECTIVE SYSTEM.

THE OBJECTIVES OF THIS STRATEGY FOR BUYING AND USING COMPUTERS ARE TO REDUCE DATA PROCESSING COSTS, INCREASE PRODUCTIVITY AND IMPROVE ORGANIZATIONAL EFFICIENCY.

TACTICALLY, DISTRIBUTED PROCESSING MAKES IT POSSIBLE TO:

- CONTROL COSTS BY MATCHING COMPUTER PROCUREMENT TO ACTUAL NEEDS.

- DECOUPLE OR CENTRALIZE SYSTEM DEVELOPMENT.

- CENTRALIZE OR DECENTRALIZE ADMINISTRATIVE CONTROLS.

- MATCH PROCESSING CAPABILITIES, CONTROL AND STORAGE OF INFORMATION ON THE MOST COST-EFFECTIVE BASIS.

- COMMUNICATION WITH THE EXISTING CENTRALIZED SYSTEMS, WITH FULLY DISPERSED SYSTEMS, AND WITH COMPUTER WORK-STATIONS AND PERSONAL COMPUTERS AS THEY EMERGE AT EVERY LEVEL OF THE ORGANIZATION.

- MANAGE OPEN-ENDED GROWTH.

LARGE, CENTRALLY OPERATED FACILITIES PROVIDE:

LARGE, SHARED DATA BASES AT LOWEST COST/BYTE (THROUGH ECONOMY OF SCALE OF LARGE DISKS)

ARCHIVAL OF PERSONAL FILES

PROGRAMS FOR SPECIAL NON-COMPUTER OWNER COMMUNITIES

VERY HIGH PERFORMANCE PROCESSING

COMMUNICATIONS AMONG THE ENTIRE COMMUNITY AND GATEWAYS TO INTERNETS AND PACKETNETS

COMMUNICATIONS ORIENTED SERVICES (E.G. MAIL, TELECONFERENCING)?

SPECIAL FACILITIES SUCH AS TYPESETTING

GROUP CENTERED COMPUTERS PROVIDE:

RELATIVELY COST-EFFECTIVE FILE STORAGE FOR ITS COMMUNITY

FACILITIES BEST MATCHED TO COMMUNITY

RELATIVELY HIGH PERFORMANCE PROCESSING

COST-EFFECTIVENESS THROUGH GROUP SUPPORTED PROGRAMS

PERSONAL COMPUTERS PROVIDE:

PERSONAL DATA BASES AND SECURITY

FAST RESPONSE TO RELATIVELY COMPLEX REQUESTS (E.G. EDITING)

PROGRAM ENVIRONMENT FOR ENTERING AND GETTING INTO PRODUCTION

9/3/80

TO: OOD

FROM: GORDON BELL

SUBJECT: DISTRIBUTED PROCESSING AND LIMITS TO ITS GROWTH

FYI -

Enclosed is a paper I will be giving at "State of the Art Review 1980" in England in November sponsored by Infotech.

To Steve Jeicher
F.Y.I.
L. Crahmore

DISTRIBUTED PROCESSING AND LIMITS TO ITS GROWTH

Gordon Bell
Vice President, Engineering, Digital Equipment Corp.
Professor, on leave, Carnegie-Mellon University

ABSTRACT

A fifth generation computer, can be fabricated on a very large scale integrated circuit (VLSI). Lower cost and increased use disperses computers in a manner analogous to the ubiquitous fractional horsepower motor. Distributed processing to interconnect dispersed computers is essential in order to avoid overloading people with information transmission and translation tasks.

The factors that affect and limit distributed processing are: physical technology and design complexity, ideas for new computer structures, basic tools to build applications, networking and other standards, useful applications, algorithms, and the human interface to the end user. A hierarchical, interconnecting model for distributing processing is based on established central and group level mini-computers, and evolving, personal computers.

DISTRIBUTED PROCESSING

Distributed processing matches computer systems to information processing needs (i.e. processing, memory, switching, transmission and transduction needs) on a geographical or organizational basis, and interconnects individual computers to form a single, integrated network so that related programs can share and transmit data among the computer nodes. The objectives are:

- to allow either local autonomy or central control of the various distributed parts;
- to provide an evolving open-ended system so that the development and installation of the parts can proceed in a quasi-independent fashion;
- to allow purchase and installation of hardware, taking advantage of timely, reduced hardware cost; and
- to build on and communicate with central systems, fully dispersed group-level mini-computer systems, and emerging personal computers.

Distributed processing is inherently hierarchical based on the principles that govern human organizational structures. In an organization, computers supplement their human, information processing counter-parts. As computers become better matched to people and organizations, and as people and organizations become more familiar with computers, an individual can interact directly with at least one computer and indirectly with group-level computers serving various functions of the organizational hierarchy. The opportunity of more egalitarian access to data provided by distributed processing may led to a change of the large organization from hierarchical to wider, functional matrix structures.

Large organizations need to interconnect the hierarchy of computers for:

communication among computer with dumb and intelligent terminals using large, central computers;
organization of central, group and individual sites;
a functional activity such as word processing or order processing; and
a specialized computer-based function such as archiving, typesetting, message switching, and electronic mail.

FORCES CREATING DISTRIBUTED PROCESSING

Rapid evolution of semiconductor and magnetic recording technologies have forced computers improvements along paths of:

1. constant cost, with increased performance and productivity for evolutionary use;
2. reduced cost, with constant performance permitting new uses commensurate with the lower cost; and
3. higher cost and performance structures permitting radically new applications.

Costs for nearly all other forms of information processing are going up because they are labor intensive. Traditional storage, processing, and transmission in libraries and postal systems are increasingly soaring. Simple word processing computers that replace typewriters save the time-consuming process of correcting errors. When groups associated with information processing start using computers a positive feedback, learning curve effect begins further increasing computer markets and uses, and lowering costs.

The industry groups supplying these products and services include:

computers - mainframe, minicomputers, personal computers and computer services;
semiconductors - nearly all LSI components are either memory or a computer processor;
communications - conventional voice and data, new packet networks and associated services;
television and cable TV - stand-alone use with TV sets (eg. games, home computers) and as an alternative to conventional communication;
office equipment - typewriters, copiers, and mechanical office equipment are increasingly electronic; and
control - gears, cams and levers, and mechanisms for control will become electronic, limited only by transducers and sensors.

LIMITS AND PROBLEM AREAS OF DISTRIBUTED PROCESSING

Ultimately all information processing will be computer based. Presently the speed of the evolution is limited by two factors: technical solutions to distributed processing problems and user assimilation.

PHYSICAL TECHNOLOGY

Semiconductors and magnetic recording technology provide the basis for cost and performance improvements. Although, extrapolations too far into the future are generally dangerous, the following technological rates of change, based on the past ten years, will continue for at least five years:

TECHNOLOGY (PERFORMANCE)	YEARLY-RATE OF CHANGE FACTOR
semiconductor memory density	2.0
semiconductors, random logic	1.4-1.6
core memory density improvement	1.3
magnetic disk recording density	1.3-1.4
magnetic tape data-rate	1.25
magnetic tape density	1.2

TECHNOLOGY (COST)	YEARLY-RATE OF CHANGE FACTOR
memory price reduction	0.7
computer system cost reduction	0.8
crt terminal cost reduction	0.85
communication cost/bit transmitted reduction	0.9
packaging (cost/vol.) and power (cost/watt)	1.0
communication line cost increase	1.12
paper cost increase	1.12

does CATV have a chance to alter this

Semiconductor technology, shared among several buyers groups, eg. consumer, communications, computers, has a faster rate of improvement than other technologies. Slower evolution has occurred in magnetic recording density because there is only one user, the computer industry. Widely used, well developed technologies, such as CRT's, previously improved for the mass television market are scarcely affected by their increasing use in computers. Costs of paper and communication lines increase with inflation.

Physical transducers that sense temperature, pressure and control power flow are slow to evolve, limiting computer use in automotive applications. Even the most widely used computer equipment, such as keyboards, printing devices and communications devices, evolve slowly by comparison with semiconductors.

COMPLEXITY OF SEMICONDUCTOR DESIGN

Gordon Moore of Intel, observed that the effort required to design semiconductors has doubled each 2-2/3 years since 1962, when a circuit only took 3 man months. 1979 circuits required 21 man years and 1982 circuits will take about 45 man years. While it is easy to conceive of organizing a team of 7 to complete a design in 3 years, the same time task by 15 people is difficult to imagine. Better management and design partitioning is required in order to avoid a drastic loss of productivity and quality that would increase the design effort even more. With one million circuits on a chip by 1982, new methodologies will be required to fully utilize VLSI's potential.

Time/transistor or time per function is decreasing.

Because of the concern and numerous approaches being pursued, I am confident that it will only take another two semiconductor generations (six years) to solve the VLSI design complexity problem. Although we do not have a good measure of circuit complexity, a given circuit description is far less complex than the largest programs (e.g. a million bit, or 128 Kbyte program is not especially large).

IDEAS ABOUT WHAT TO BUILD

New directions in computer structures are difficult to predict by simply looking at conventional machines. Current limiting factors point to needed innovations. Applications involving two dimensional signal processing for pictures appear to require a different processor design, and speech signal analysis requires vector processing. A general purpose processor could emerge from these alternatives for one-and two-dimensional arrays:

arrays of conventional microprocessors;
application specific, functional processors;
bit array processors to operate directly on the array data structures, including arrays, or associative processing;
processing associated with memory; and
data flow architectures.

BASIC TOOLS TO BUILD APPLICATIONS

Coupling knowledgeable user needs to machine development produces more capable, yet harder to understand systems: a paradox in the attempt to build highly capable and easy to use systems. The popularity of the Bell Labs UNIX System is a testimony to a single, consistent, easy to use language, that is described in a small manual. The popularity of APL and BASIC systems can be similarly explained. Although one would expect that additional capabilities (memory) would make the user interface simpler, few good examples are known. The time to build a given application using the multitude of systems/databases/languages is highly variable, indicating a continued lack of understanding of the design process.

NETWORK AND OTHER STANDARDS

Because standards are evolving, the current situation of distributed processing among countries and vendor systems is a disaster. International protocol standards provided by manufacturers (Internets) and by various common carriers for Packetnets which are called by the same name, are fundamentally different and incompatible. Many standards mean no standards.

We must get beyond the simple standards required for Packetnets and Internets to define protocols for passing high level messages, such as electronic mail, among computers. Office based applications, centered around text processing, electronic mail, user typesetting, office processing, and electronic filing, all require significant user level standards. Using only lower level communications protocol standards will cause a combinational explosion of high level protocol changing gateways. This leads to added overhead, extra development, delay, incompatibility, and often, misinterpretation of messages.

In the low priority area of intra-computer architecture, the U. S. Government has standardized on the existing defacto standard, the IBM Channel, as the means of interconnecting mass storage to computers. Unfortunately this act of standardization will limit change into newer systems architectures.

USEFUL APPLICATIONS AND DISTRIBUTING THEM

Decisions to use the major applications centered around office automation are very complex. Justifying an application generally requires an understanding of both computer systems (beyond that provided by manufacturers) and the organizational structure of individuals and group users. Although electronic mail seems right, measurements of increased productivity, decreased paper flow, better decision-making, efficiency of communication, and the creation of excess communication are hard to make. To my knowledge, they don't exist.

Given that few measures exist to rationalize, simple stand-alone applications, justifying a distributed network becomes a work of art. Tools have only recently become available for a system manager or developer to distribute the database, processing, and intercommunications over several systems. In the specific case of distributed processing for electronic mail, the results are encouraging but a general solution has not yet emerged.

An underlying difficulty of building applications beyond the generic office automation described above exists because problems are solved by patch-work. Usually programmers with computer science (computer engineering) training and a representative of a particular discipline (eg. accounting, mechanical engineering) put a solution together to get something started. This results in sub-optimal designs. In order to use the computer as a component of systems they design, rather than as a simple tool for problem solving, computer science must take on a pure role, like physics, and each of the disciplines take the responsibility for training people and engineering the systems within its own discipline.

ALGORITHMS

There are many cases of the adage: "It is better to work smarter rather than work harder". If always exponentially improving, technology will eventually permit solving a particular problem in a reasonable time, e.g. a 24 hour advanced weather forecast must be solved in less than 24 hours or an exponentially increasing machine population will be required. However, at a given time, algorithms limit when a problem can be solved and whether it is economically feasible.

HUMAN INTERFACE

The interface between the system and the final user is a barrier in the same way that a root system for building applications programs is a barrier to building applications. Adding more functions so that an application will perform better is generally accompanied by increased complexity requiring more documentation and training. The lack of standards at the user interface will limit getting the payoff inherent in a given system or set of systems, and may cause adverse user reaction. For example, word processing, electronic mail and user typesetting systems are all likely to have different syntax, semantics, manuals, training and procedures for dealing with the same text.

A DISTRIBUTED PROCESSING ENVIRONMENT

Proliferation of dispersed computing forces interconnection, hence distributed processing, so that human users don't have to become information carriers and translators between the different systems they use. Communication within and between organizations with common carrier networks is provided via an interconnected hierarchy.

INTERCONNECTING THE COMPONENTS

The three types of computers in a given organization will be connected via high bandwidth links in what may appear to be a hierarchical structure. In addition, clusters may be connected on a fixed basis. The alternative interconnect possibilities are:

- ethernets or rings to interconnect all terminals and computers with specialized terminal concentrators;
- evolution of phone circuit switches using digital techniques for both voice and data;
- packetnet switching; and
- direct interconnection among the computers with routing through each computer.

CENTRAL COMPUTERS

The top most computers of the hierarchy will evolve from the current, highly central computation facilities. These machines store most of the data and do most of the computing in today's organizations. Given the difficulty of migrating files and work from these machines, the emphasis within the centers will be interconnection among the machines within each center, creating in the short run, even larger data bases. The tight interconnection among the central computers will also permit trade-offs among cost, reliability, performance, and evolving performance, for a given application or set of applications. In order to get the economy of scale required to support the large human organizations that attend central computers, their functions will have to be specialized (e.g. front ends for handling many communications lines, and back ending for databases and archiving).

Central computing facilities will continue to be operated by large staffs whose emphasis is on knowledge of the operating systems and getting work done using highly specialized facilities such as CODASYL Databases. The casual user will be dependent on the central systems through the applications. Cost will be high for everything except the storage of very large files, where hardware provides an economy of scale. Programming costs at the center have to be the highest, because the facilities are general purpose and applications are most remote from the ultimate user. The role of central facility will be to provide:

- communications among all the other computers within the organization including gateways between various computer and telecommunications vendors;
- archival file storage;
- unique, sharable facilities such as very high speed computers and printing devices;
- computational functions for the entire organization e.g. electronic mail;
- operation of historical programs and data bases; and
- relatively high cost computing by having to provide generality and service for the worst case.

GROUP LEVEL COMPUTERS

Group level computers are based on the evolution of timeshared and real time minicomputers and cost roughly that of an additional person. Typically these machines support the single function of the group, (eg. order processing, engineering design and data base, laboratory data gathering and analysis, group word processing, single process control) running a single unattended program. Group level computers provide:

- relatively cost effective storage of the group data base;
- unique program(s) aligned with function of the group;
- relatively high performance processing; and
- cost-effective computing through sharing of a common function and specialization of work.

PERSONAL LEVEL COMPUTERS

Personal computers are emerging rapidly, and many believe that they will become the dominant form of computing. Since the only hardware technology for which economy of scale holds is mass storage, and given that all terminals already have embedded computers for control, it is easy to envision adding more primary memory and doing all the computation at the terminal instead of having computation done in any shared facility. A recent, Carnegie-Mellon University personal computer research proposal states:

> "The era of time-sharing is ending. Time-sharing evolved as a way to provide users with the power of a large interactive computer system at a time when such systems were too expensive to dedicate to a single individual...Recent advances in hardware open up new possibilities...high resolution color graphics, 1 mip, 16 Kword, 1 Mbyte primary memory, 100 Mbyte secondary memory, special transducers,...We would expect that by the mid-1980's such systems could be priced around $10,000."

Personal computers provide:

- personal data bases and security;
- more, average computing power, with better response time than shared systems;
- needed processing for the computationally intensive tasks like editing, and speech i/o;
- a program creation environment; and
- relatively higher costs than group level computing, unless the task is very specific and well-matched to the system.

Although both the novice and experienced user relish the independence that the personal computer provides, communications and support by the other levels is equally necessary. Given that we are substantially far from such distributed systems, there are surely additional problems, limits, and opportunities that are yet to be forecast.

COMPATIBILITY

EDITING SYNTAX

- WPS, EMS, FORMS TEXT, COMMANDS, USER TYPESET

FILES

- PERSONAL & SHARED WPS
- EMS
- INTERFACE TO DATA IN SYSTEM W/O CONVERSION (I.E. PROGRAMS)

COMMUNICATIONS

- DECNET ETC. VIA SYSTEM CALLS

PERFORMANCE/USE UNDERSTANDING

PHYSICAL STRUCTURE PARAMETERS

- COST (PURCHASABILITY, MAINT., ETC.), PERFORMANCE, RELIABILITY

- SECURITY, ATTITUDES ABOUT SHARING

- AESTHETICS/APPEARANCE

- ENVIRONMENTAL ADAPTABILITY

  (1). UNOBSTRUSIVE

  (2). DOMINATES & BECOMES (CREATES)
  THE ENVIR. (EG. WORK SPACE, NOISE, LIGHTING, FILING, DOCUMENTS, PHONE

- COMMUNICATION WITH: OTHERS, OTHER WPS, DP,...

PRIME OA 5/80

WP

TEXT CREATION & EDITING

FILING & RETRIEVAL

BOILERPLATE LIB.

LIST PROC.

ADV. FEATURES:
PROOFING, HYPHENATE, TRANSLATE

MGMT COMM. & SUPPORT

EMAIL

CREATE NOTES & MEMOS
DIST.
ANNOTATE
ACK. & SECURITY CODES

CORRESP. MGMT

FILE, RETRIEVE, ARCHIVE
FILE CODES & REPORTS

MGMT SUPPORT

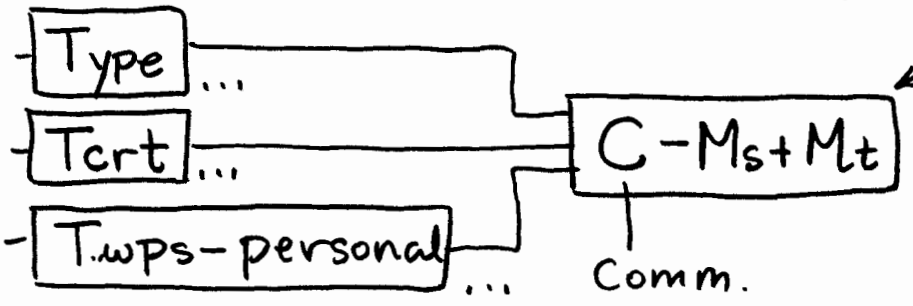
INTRAY, CALENDAR, SCHEDULING, TICKLER FILE, TELEPHONE LOG

MGMT INFO.

QUERIES, REPORTS, MODELLING, APPL.

PHYSICAL STRUCTURES ALTERNATIVES

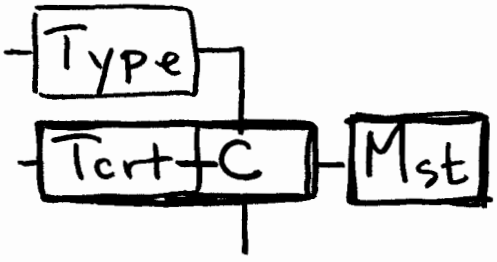
- SHARED: CENTRAL AND GROUP



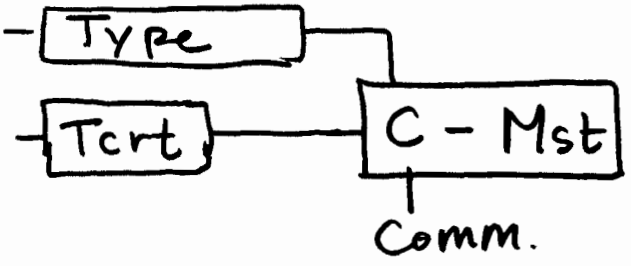
IN CAB(S).

10, 20, VMS, 11/M, RSTS, 2XX.

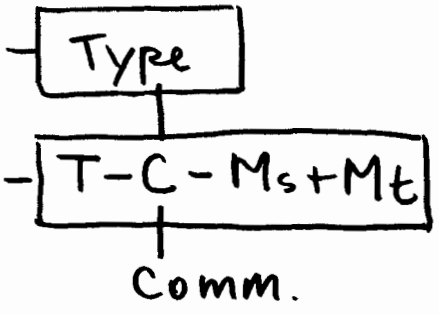
- PERSONAL:



IN DESK AND TERMINAL (E.g. UT 78, 278) I.

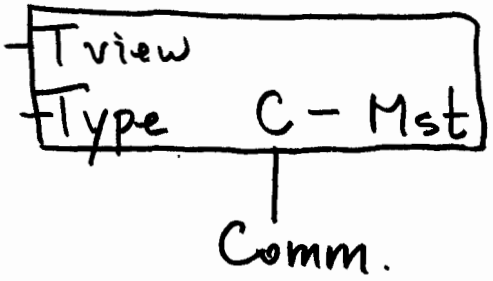


IN Mass. Storage (PDT) II.



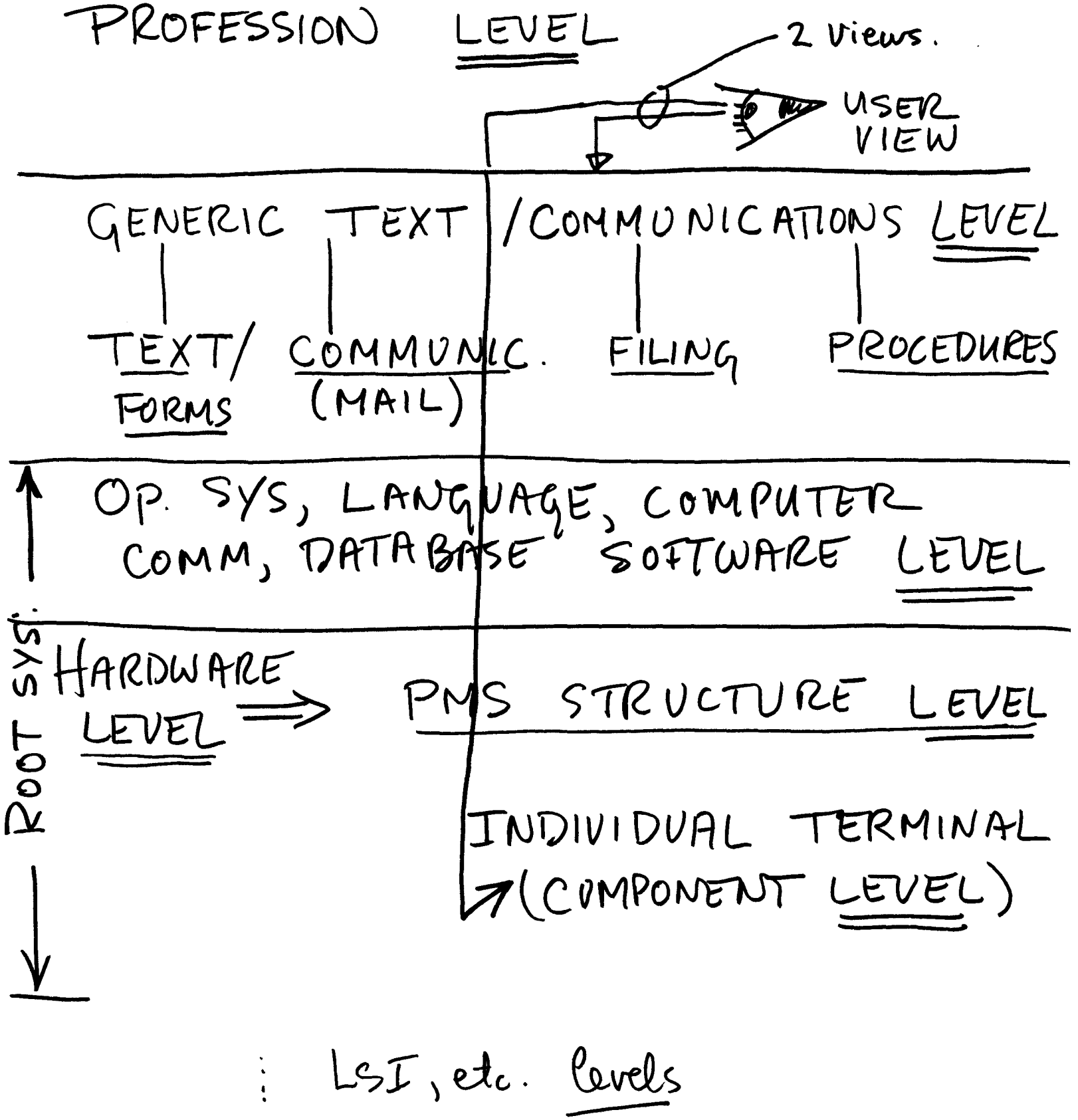
IN Terminal. III.

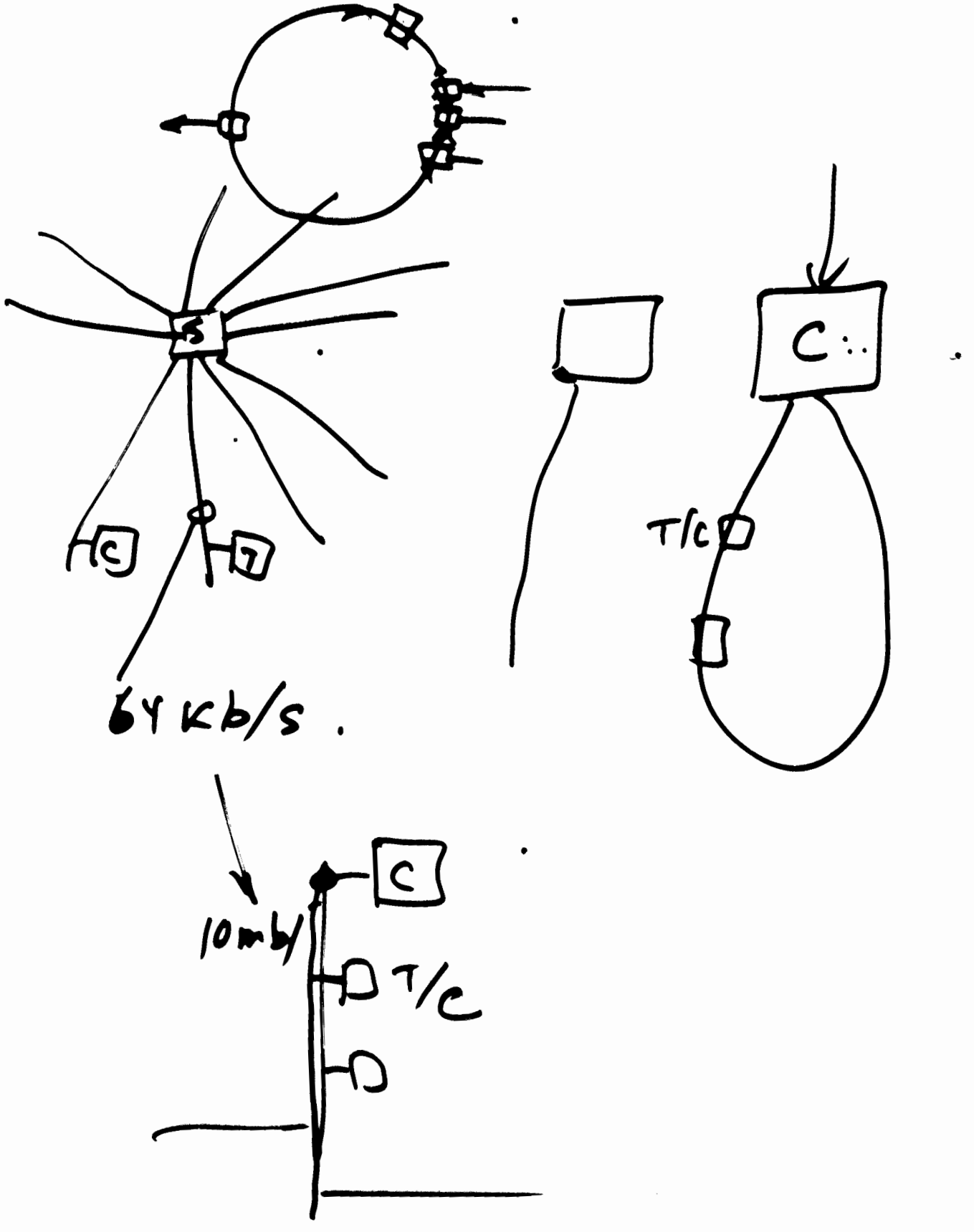
IN Typewriter IV.



5/20/80
GB

OA - SUBSET OF A PROFESSION - BASED SYSTEM

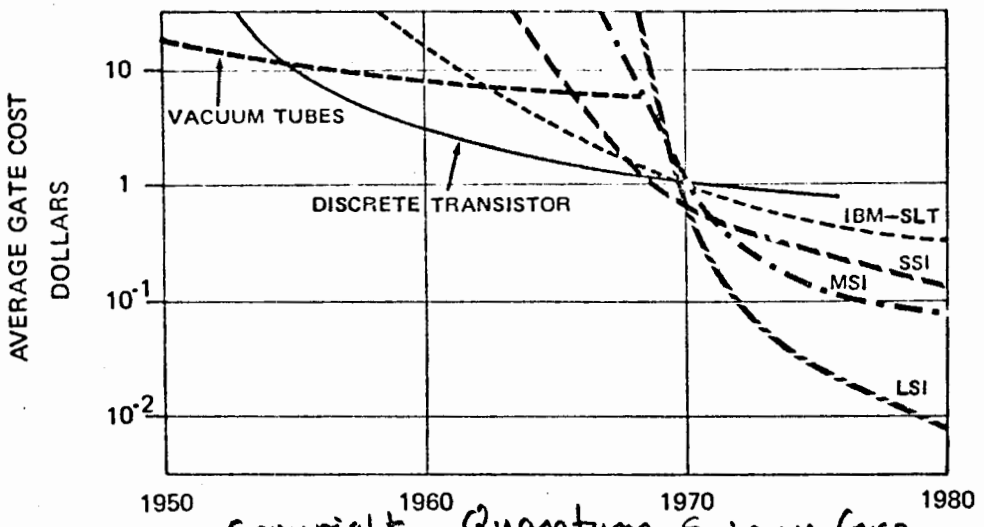



S
C
T
64 Kb/s
C
T/C
C
10mb/
T/C

95 slides

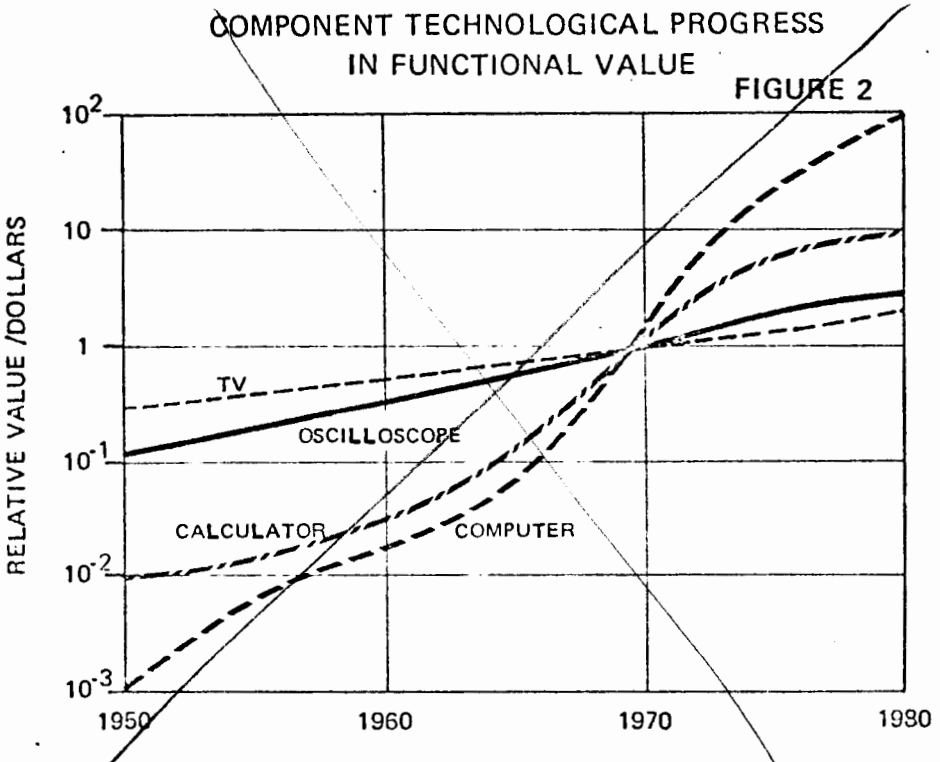
COMPARATIVE GATE COSTS

FIGURE 1



COMPONENT TECHNOLOGICAL PROGRESS IN FUNCTIONAL VALUE

FIGURE 2

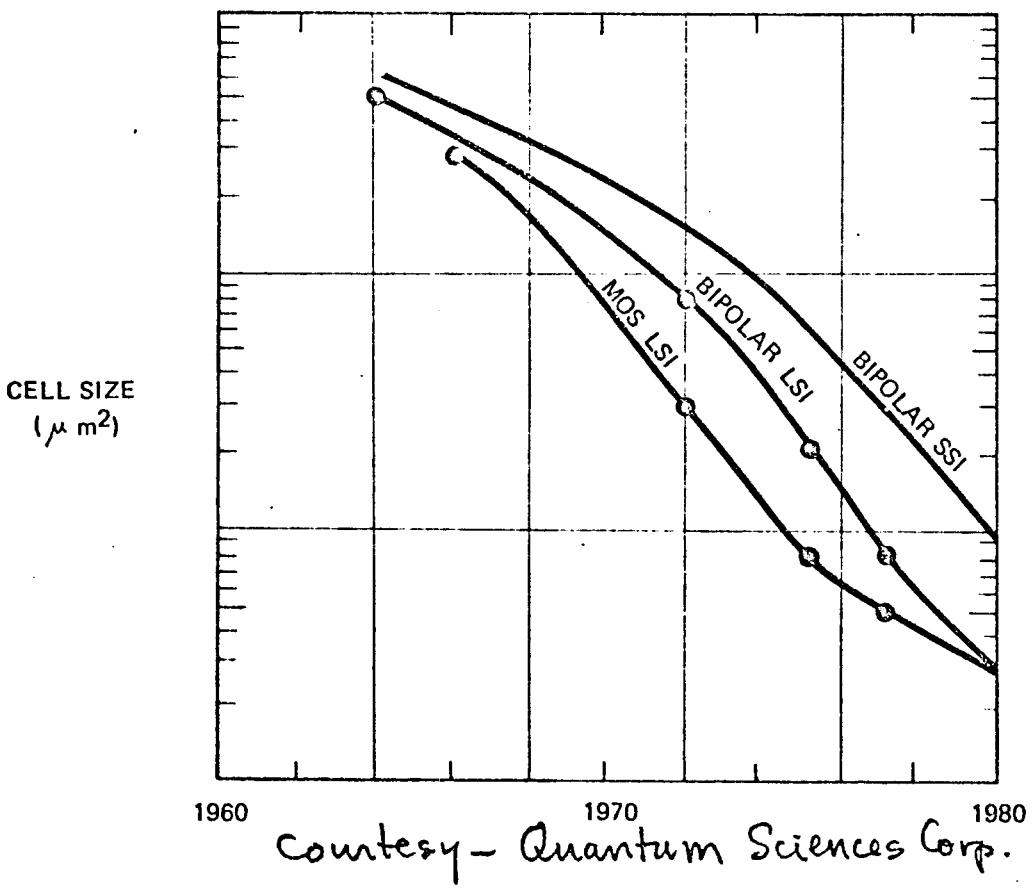


Note slide

FUNCTIONAL VALUE INCLUDES PERFORMANCE, QUALITY, UTILITY AND RELIABILITY. IN COMPUTERS AND CALCULATORS, COMPONENTS HAVE BEEN BY FAR THE MOST SIGNIFICANT FACTOR IN VALUE IMPROVEMENT.

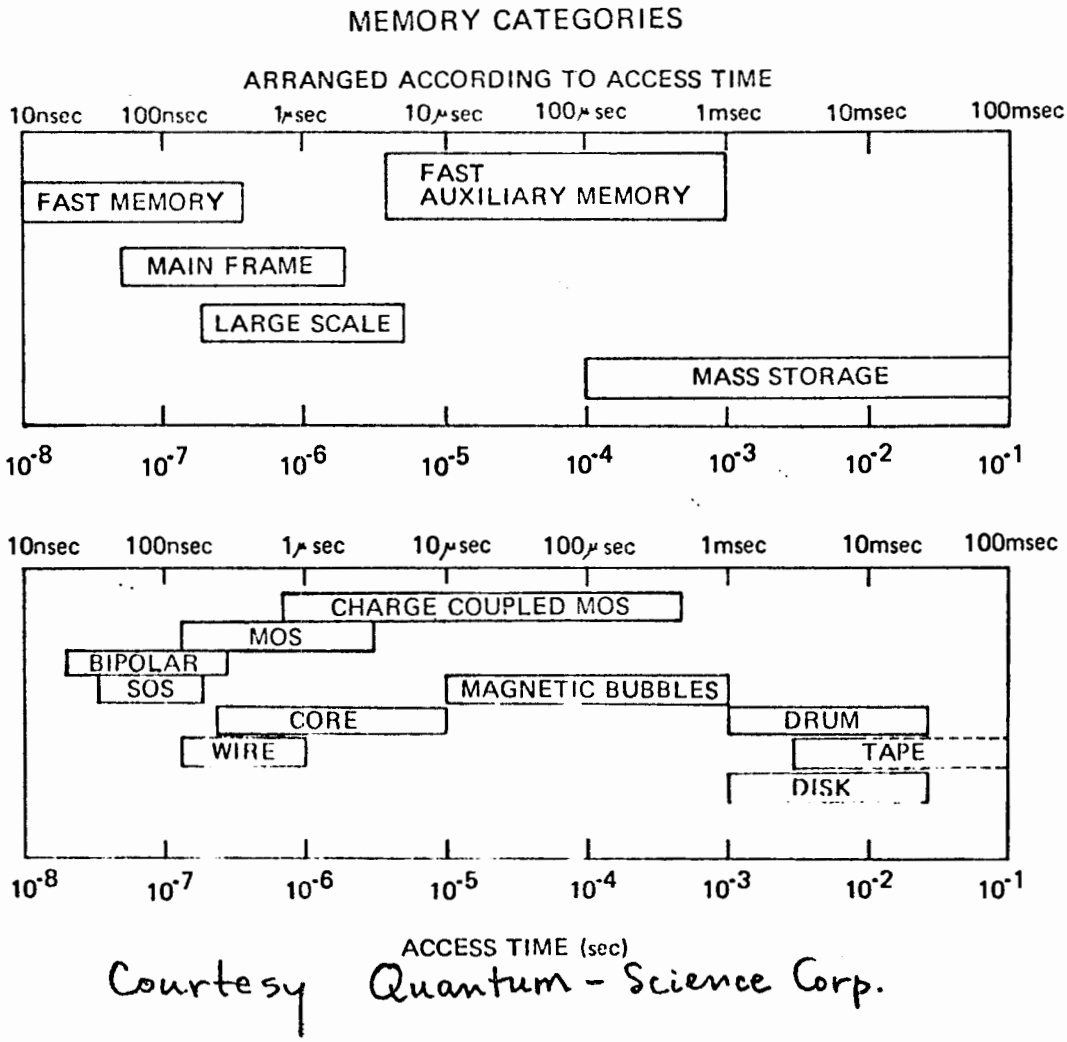
FIGURE 9

IC TECHNOLOGY DEVELOPMENT



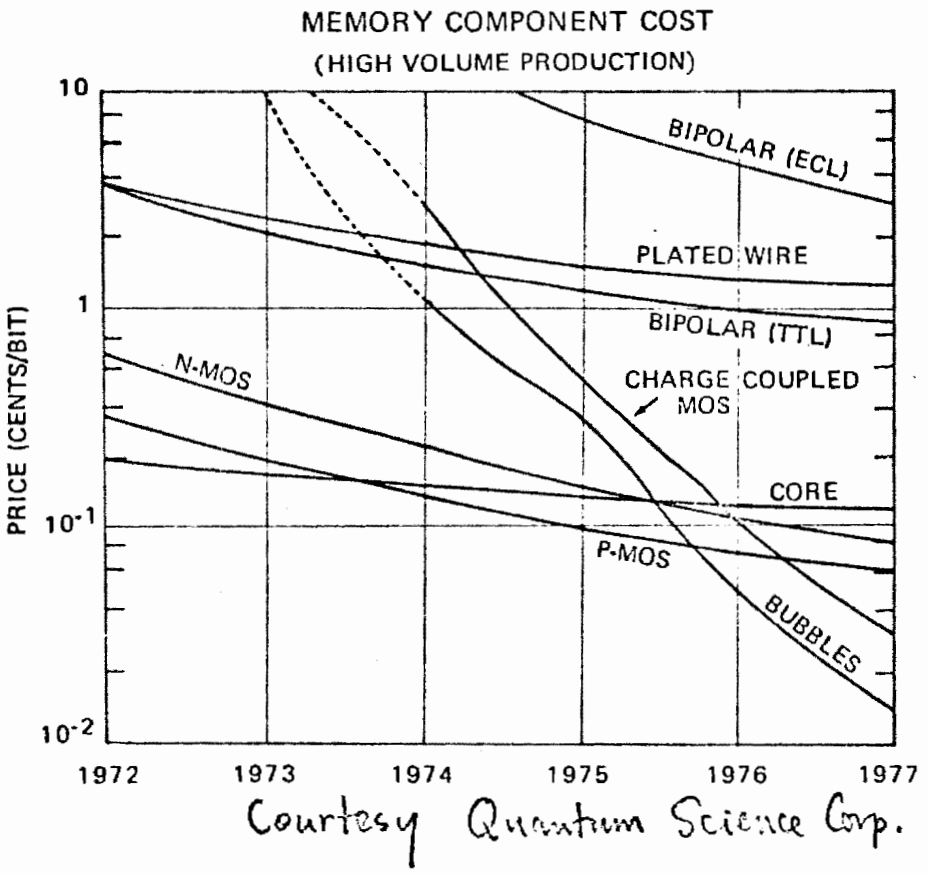
Courtesy – Quantum Sciences Corp.

FIGURE 12



Courtesy Quantum - Science Corp.

FIGURE 13



Courtesy Quantum Science Corp.

compatible with the DDP-516, and executed in the well known 930 series of IC flatpacks. The unit is packaged on large, double sided boards, 8 x 8½". The 4-wire, 3D memory has a 1.6-μs cycle time. It is not surprising that the factory cost distribution shows about the same logic cost ratio as the DDP-516, while the memory cost drops somewhat to 37%. The power supply represents 8% of the factory costs and the miscellaneous costs are 30%.

The next processor examined was the PDP-11, a 16-bit machine developed by Digital Equipment Corp. This machine is constructed of SSI and MSI TTL dual-in-line packages from several of the semiconductor manufacturers, mounted on 8½ x 10¼" and 8½ x 5¼" doubled-sided PC boards. The boards are plugged into assemblies of wirewrapped connectors which are in turn cabled together. A core memory is used.

The architecture of the PDP-11 is different from that of computers previously analyzed. The machine contains a number of registers which can be used for both data manipulation and address modification. However, the rather surprising result of the factory cost estimate is that the relative logic and memory costs are very close not only to those of the DDP-516, which is of a related but earlier technology, but also to those of the DDP-116, which is a different architecture constructed of a completely different technology. It appears that there may be a ratio of memory costs to logic cost which is fixed regardless of the technology and architecture.

12-Bit Machines

To allay the suspicion that this ratio appears only in the 16-bit minicomputers, two 12-bit machines were analyzed to see if the ratio held true in machines which were substantially different (Table 2). The first is the H112 developed by Honeywell. Its construction is of SSI DTL logic of the 930 series mounted on 2¾ x 2¾" circuit boards. The memory is a 1.6 μs, 4-wire, 3D design. Again the ratio of logic costs to total factory cost is in the 24% range, and the memory cost is 44%. The final machine analyzed was the PDP-8/E manufactured by Digital Equipment Corp. Costs of this machine were again estimated using industry prices and estimated labor costs. The PDP-8/E is constructed of MSI and SSI TTL dual-in-line packages mounted on double-sided boards. The estimated logic costs, however, and only 15% of factory cost as opposed to the 24% to 28% seen in the other machines. This apparent counter-example to the argument can be explained by noting that the PDP-8/E is the most recent redesign of a computer first delivered in 1963. Since the basic architecture has not been modified since then, this machine shows the faster reduction of logic cost in relation to memory costs. It is most probable that the original computer did in fact adhere to the ratio of logic cost vs. memory cost seen in the other machines. Since logic costs have dropped over four times as fast as memory costs, the

slide

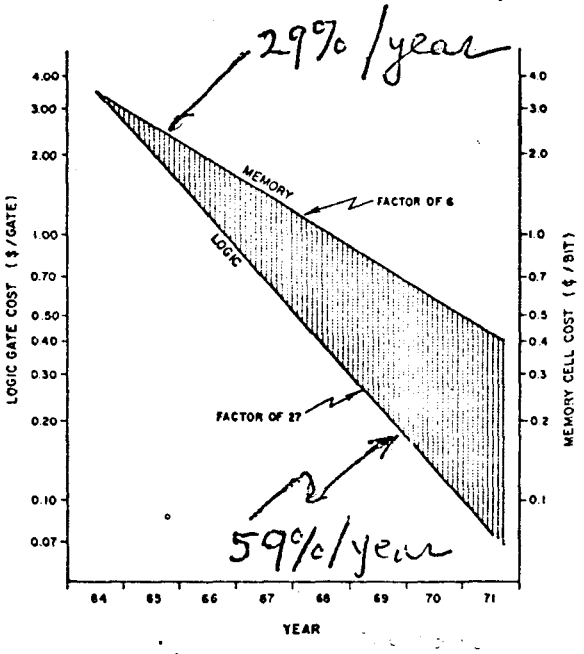


Fig. 2 Plot of logic gate and memory cell costs beginning in 1964 and extended into 1971. Core memory prices have decreased by a factor of 6 during these years, while logic prices have dropped by a factor of 27 over the same period

House & Henzel — Computer Design Jan. 1971

PDP-8/E shows a very low portion of factory cost devoted to CPU logic.

The apparent constant ratio of logic factory cost to memory factory cost has been demonstrated in a number of computers. It is reasonable to assume that the designer in each case did not have that ratio in mind as a goal when the design was started. Why, then, does the ratio constantly emerge?

The answer seems to lie in examining the characteristics of machines which do not meet the ratio. Assume that a machine was designed which had a significantly lower ratio of logic to memory costs. This machine, by its low number of gates, would have a very minimal instruction set, just barely enough to make a recognizable computer. At first glance it would seem that the machine would be a great success since it is substantially cheaper than the competition. The problem, however, would occur when users program the

CIRCULATE TO SYS MGRS Brian RLL

****
d i g i t a l *
****

TO: ENG STAFF:
AVRAM MILLER
STAN PEARSON
BILL PICOTT
BRUCE STEWART

DATE: THU 5 MAR 1981 21:46 EST
FROM: GORDON BELL
DEPT: ENG STAFF
EXT: 223 2236
LOC/MAIL STOP: ML12-1/A51

SUBJECT. WINNING, GREAT PRODUCTS. A CONSTRAINT ON OUR PRODUCT STRATEGY

After having approved a P/L plan at the December review of the LR Plan by the Operations Committee, one of our P/L's has just reduced their commitment to sell products in excess of 10% over last year. This amounts to a 90M$ reduction in NOR and a 4.5M$ reduction in engineering spending may result The reason for this that was given was more competition and that our new products being introduced in early 82 have slipped a bit, plus they don t look so hot (when they come out).

In this case, I don't expect anything of the Product Line and it's possible that there may be other new products and that it s too hard to sell anything. Hence, the NOR may slip more. Where we end up in sales is purely a game of chance because the only way that they can sell anything is if there is some feature that seperates our product from everyone else.

I believe they are right, and probably should go even further and suggest we close down the factories unless they get these kind of products. Unfortunately, they were part of the large mass of product managers, engineering strategists, and marketers who partipated in the generation of the product strategy. With such a mass, we clearly have a question of who is responsible. I want to make this clear:

I hold the engineering manager for a product, or product area solely responsible for the success of a product.

The issue then is what went wrong?
The products, now don't look good enough to be bought without what others might think of as marketing. In this case, the area looks "commodity like" and we don't have anything to differentiate us. This is clearly our responsibility!

Therefore, I want us to stop building products that we do not believe are going to be great products. This means no mid life kickers, unless, like the 70 they enhance performance and really extend the product life. The new products in this example are fundamentally cost reductions, and golden rule products in a new, questionable market area. (Please refer to p12 of Computer Engineering for the economics of why products should evolve along performance rather than price... in a constrained engineering budget if you haven't read it)

Therefore, the constraint on products are. fit the strategy; and

.O CRAPPY PRODUCTS. WE ARE ONLY GOING TO BUILD THE BEST PRODUCTS ... CAN!

(In the ensuing several months, I want to review several of the things we are doing against this criteria. I know buy in and all those groupie words are nice, but when the going gets rough, the nice folks who buy in are the first to sell out. When that happens and we're all that's left, it's clear to me that the responsibility is once again solely ours for the generation of good products. If we don't think we can do it then maybe we should just sell ones others build or perhaps buy they product from Tokyo or wherever and avoid all the risk and hassle.)

In our presentation in April, we have to be honest. If the product is marginal, then let's not do it... independent of who's brought in.. cause it's clear who's the first to sell out.

PS
The NOR reduction episode happened on Monday. On Wed. evening we met with Andy about the Technical Group use of CT. He's not buying, cause it isn't good enough. This I respect! It's regretable that one of our customers had to tell us that our prouduct isn't good enough!

PSS
I don't want to hear the issue of we aren't spending enough money, and what do you expect. In the disaster areas, we have spent incredible amounts of money, it's just that it s all been to get marginal and/or half-done products.. The new rules will stop this. we won't do any of them; someone of you have product area responsiblity and you must make the appropriate proposals (and breadboards) to get us good products.

Please join me in building quality products.

Any problem with the clarity or rationale of going this way?
Comments, please.
Are the rules clear?

Great ideas -Losers

Why C's Evolve

Future

~~Interaction of tech. + applic + im~~
Implic. of tech.

Ideas transferred between micro + macro

Wheel of incarnation

Product design guidelines

COSTS

Physical Mechanisms

Valve, Drums, Disks, Electrostatic Mem,
Core Mem, Integrated Ckts, Video, hard, audio

Stored Program Concept

Turing — Data vs. Program
Languages — Von Neumann.
Microprogramming — Tagged / Descriptors
Virtual Machines — 0 ← 1 → 2, 3 Address
Recursive VM — Pio | Pspecial
Families (Range & Time) to preserve Softw. invest — B-Register | Data Access

TIME Sharing of Equip. (Fractional II'ism)

Interrupts
Multiprogramming ; T/S ; Trans. Proc.
Real Time.

Parallelism

Multiprocessors.

Arrays, Pipelines, Concurrency (II' Process)
Dist. Proc. (Space Share) → S/F Nets

Reliability, Redundancy, Availability

Registers, Cache, Primary, Paging, Files, Archives

Memory Hierarchy + Associativity (Locality)

ADVANCES IN COMPUTER STRUCTURES*

COSERS

PHYSICAL MECHANISMS

SEMICONDUCTORS

MAGNETIC MEDIA

TRANSDUCERS (E.G., VIDEO, ROBOTS)

STORED PROGRAM CONCEPT (MACHINES)

TURING MACHINE

VON NEUMANN MACHINES — { DATA IS PROGRAM / DATA VS PROGRAM

- COMPUTER SPECIFIC (0,1,2,3 ADDRESS)
  TAGGED AND DESCRIPTORS
  GENERAL NOTION OF MOVING DATA-TYPES TO HARDWARE

MICROPROGRAMMED MACHINES

LANGUAGE MACHINE

VIRTUAL MEMORIES AND MACHINES

I/O AND SPECIAL PROCESSORS

ARCHITECTURAL FAMILIES OVER PRICE AND TIME

* Defined for COSERS Report.

FRACTIONAL PARALLELISM (TIMESHARING/TIME MULTIPLEXING)

INTERRUPTS

MULTIPROGRAMMING;

TIMESHARING;

MULTIPROCESSES FOR REAL TIME

TRANSACTION PROCESSING

PARALLELISM

PIPELINING

MULTIPROCESSORS

VECTOR AND ARRAYS PROCESSORS

GENERAL CONCURRENCY (PARALLEL PROCESSING)

DISTRIBUTED PROCESSING (SPACE SHARING)⇒

STORE AND FORWARD NETWORKS

REDUNDANCY FOR:

RELIABILITY, AVAILABILITY AND MAINTAINABILITY

MEMORY HIERARCHIES

(COMPUTATIONAL LOCALITY)

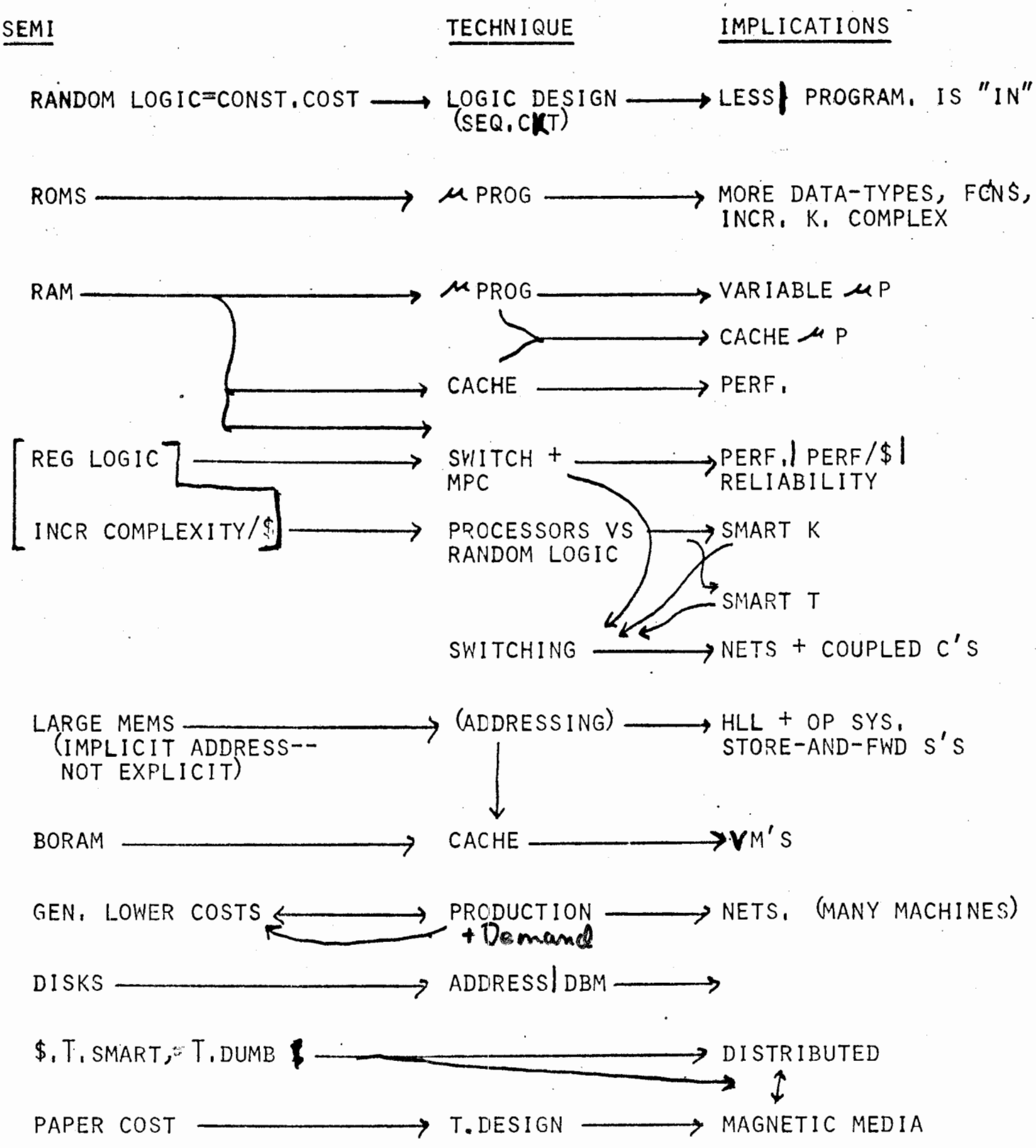
REGISTERS } INTRA-PROCESSOR
CACHES }

PROGRAM PRIMARY

PAGING } SECONDARY
FILES }

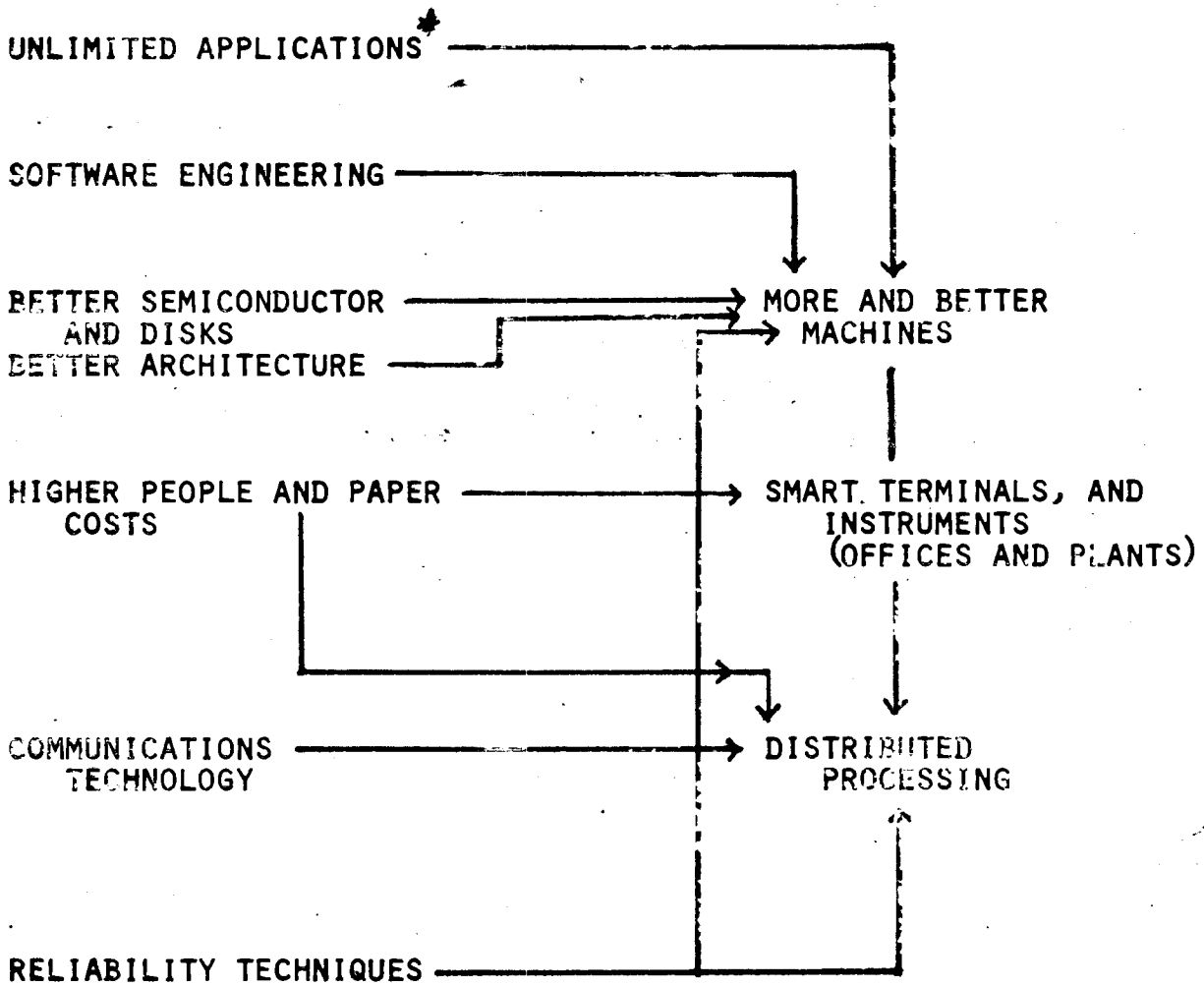
ARCHIVES - TERTIARY

TECHNOLOGY



GB
2/7/75

T-22 (NOT Send)



* Supplements all forms of information transmission, switching, transduction, storage and processing.

TABLE 1 - CHARACTERISTICS DERIVED FROM LARGER COMPUTERS

INTERNAL CENTRAL PROCESSOR

INDIRECT ADDRESSING; INTERRUPTS; INDEX REGISTERS; MULTIPLE, GENERAL PURPOSE REGISTERS; BASE AND/OR PAGE ADDRESSING; FLOATING POINT DATA-TYPES*; PAGING, SEGMENTATION, AND INTERPROCESS COMMUNICATION*

STRUCTURAL

SPECIALIZED PROCESSORS; MULTIPROCESSORS*

IMPLEMENTATION

MICROPROGRAMMING*; LOOKAHEAD*; CACHE*;

SOFTWARE

COMPILERS: FORTRAN; TIME-SHARING MONITORS*

*NOT EXTENSIVELY USED, BUT USE LIKELY TO INCREASE.

TABLE 2 - CHARACTERISTICS GENERIC TO MINICOMPUTERS

IMPLEMENTATIONS TRACK TECHNOLOGY CLOSELY.

INTERNAL CENTRAL PROCESSOR

BASE ADDRESSING; ADEQUATE INTERRUPT RESPONSE TIME; POWER ON-OFF INTERRUPT

STRUCTURAL

VERY LITTLE HARD COPY I/O, SECONDARY MEMORY; OBVIOUS STRUCTURE (ALLOWING EASY INTERFACING); DIRECT MEMORY ACCESS--ENCOURAGES PMS ARCHITECTURE + DESIGN.

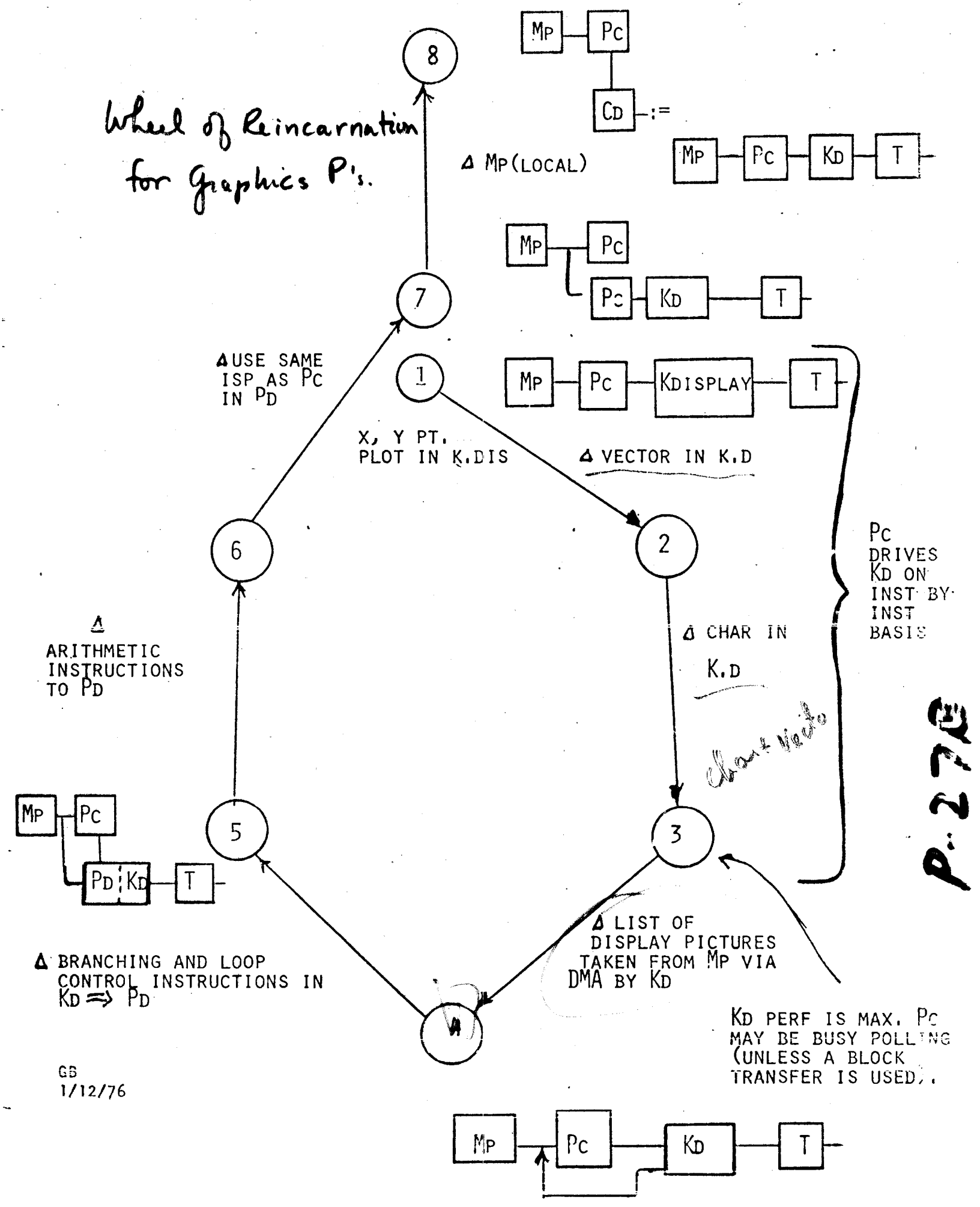
USES (DEDICATED)

CONTROL (E.G., PLANT, INSTRUMENT); COMMUNICATIONS (E.G., MESSAGE SWITCH); LARGER COMPUTER (E.G., TERMINALS, FILES, HARD COPY)

SOFTWARE

SMALL GENERAL PURPOSE MONITOR; LANGUAGES: PRIMITIVE ASSEMBLER, BASIC, FORTRAN; SPECIALIZED DEDICATED USE PACKAGES (E.G., TYPESETTING, INSTRUMENT TESTING, PROCESS)

APPROACHABLE--FIT COMPUTER TO PROBLEM VS...


Wheel of Reincarnation for Graphics P's.
8
MP
PC
CD
:=
MP
PC
KD
T
Δ MP(LOCAL)
MP
PC
PC
KD
T
7
ΔUSE SAME ISP AS PC IN PD
1
MP
PC
KDISPLAY
T
X, Y PT. PLOT IN K.DIS
Δ VECTOR IN K.D
6
2
PC DRIVES KD ON INST BY INST BASIS
Δ ARITHMETIC INSTRUCTIONS TO PD
Δ CHAR IN K.D
Chart Vector
MP
PC
PD
KD
T
5
3
Δ LIST OF DISPLAY PICTURES TAKEN FROM MP VIA DMA BY KD
Δ BRANCHING AND LOOP CONTROL INSTRUCTIONS IN KD ⇒ PD
4
KD PERF IS MAX. PC MAY BE BUSY POLLING (UNLESS A BLOCK TRANSFER IS USED).
GB
1/12/76
MP
PC
KD
T
P. 27

Product Design Guidelines

1. People costs dominate all others → Human Eng.
2. Approaches:
   a. Look at technology.
   b. Look at application.
   c. Find a thing → can it be built?
3. Extrapolate on within limits to 1980 — stay within physical laws.
4. Operate on cost effectiveness $E = \frac{1}{k} c^2/t$
5. Add Capability that no one has (and needs).
6. Languages.

SOLUTION = CLUSTER

A CLUSTER IS A LOOSELY COUPLED SYSTEM

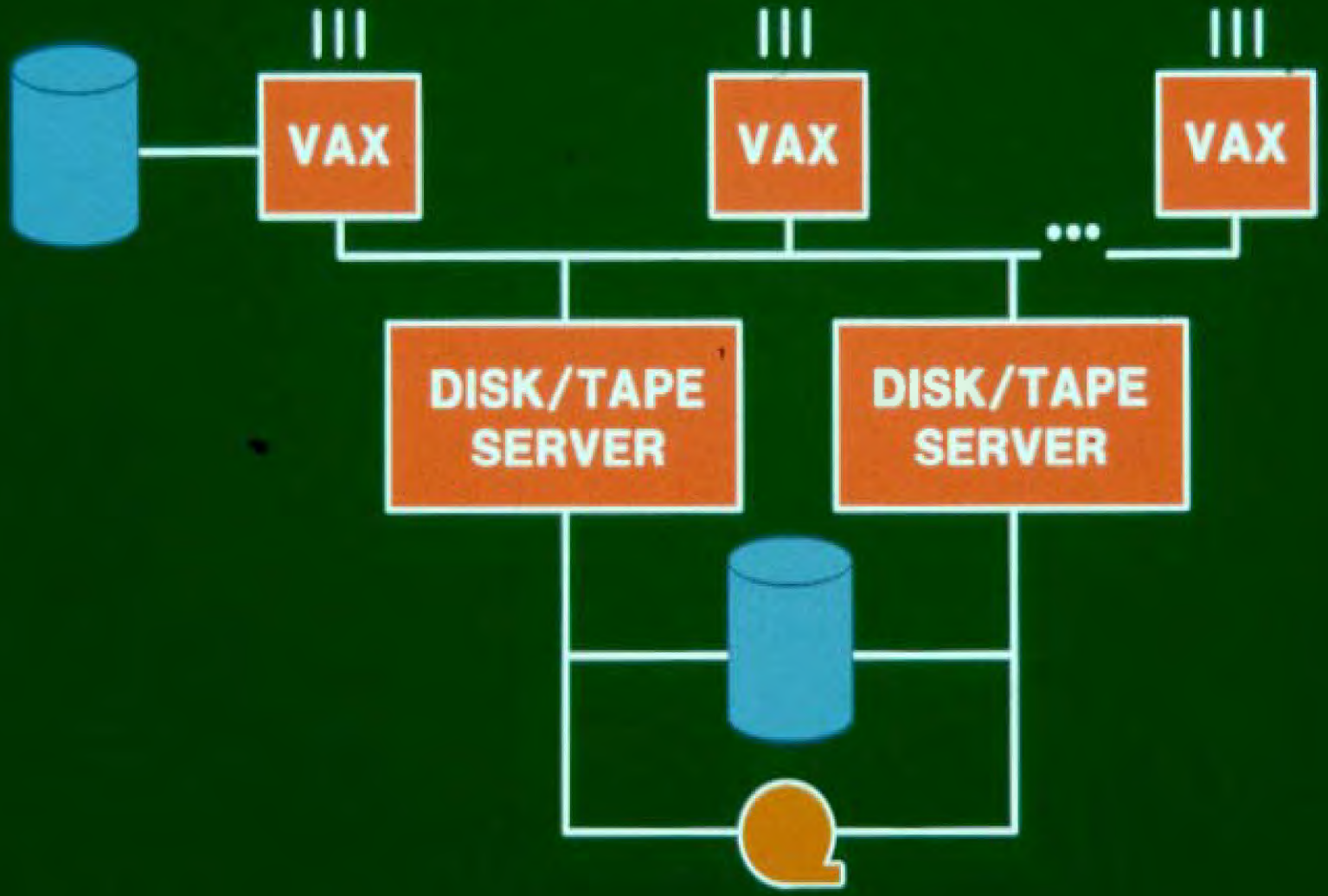
SINGLE SYSTEM → TIGHTLY COUPLED SYSTEM → CLUSTER → NETWORK

CLUSTER ATTRIBUTES

- "SINGLE MACHINE ROOM"
- MULTIPLE AUTONOMOUS PROCESSORS
- GENEROUS MEMORY PER NODE
- NO SHARED MEMORY
- HIGH SPEED PACKET ORIENTED INTERCONNECT
- PROCESSORS CRASH INDEPENDENTLY, NOT TOGETHER
- SHARED FILE SYSTEM

CLUSTER CONFIGURATION

LOCAL TTY'S, LP'S, ...



SHARED FILE SYSTEM

- BEHAVES AND PERFORMS LIKE LOCAL DISKS
- FILE ACP DISTRIBUTED OVER VAX CPU'S:
  - NO SINGLE FILE SERVER BOTTLENECK
  - ELIMINATE SINGLE POINT OF FAILURE
- FILE ACP & RMS USE DISTRIBUTED RESOURCE LOCK MANAGER
- DISK SERVER EMULATOR FOR LOCAL DISKS

THE CI COMPUTER INTERCONNECT

- PACKET ORIENTED TRANSMISSION
- SERIAL, 70 MEGBIT/PATH
- DUAL PATH FOR REDUNDANCY AND PERFORMANCE
- UP TO 16 NODES

CI PORT

- INTELLIGENT
  - USES PAGE TABLES AND VIRTUAL ADDRESSES
  - MESSAGES AND BLOCK TRANSFERS
  - PROTOCOL FOR PROVIDING RELIABLE TRANSMISSION
- SYSTEM COMMUNICATIONS ARCHITECTURE SOFTWARE UNDER VMS

DECNET IN A CLUSTER

- USES CI
- ALLOWS EXISTING NETWORK FEATURES:
  - REMOTE TERMINALS
  - MAIL
  - PHONE

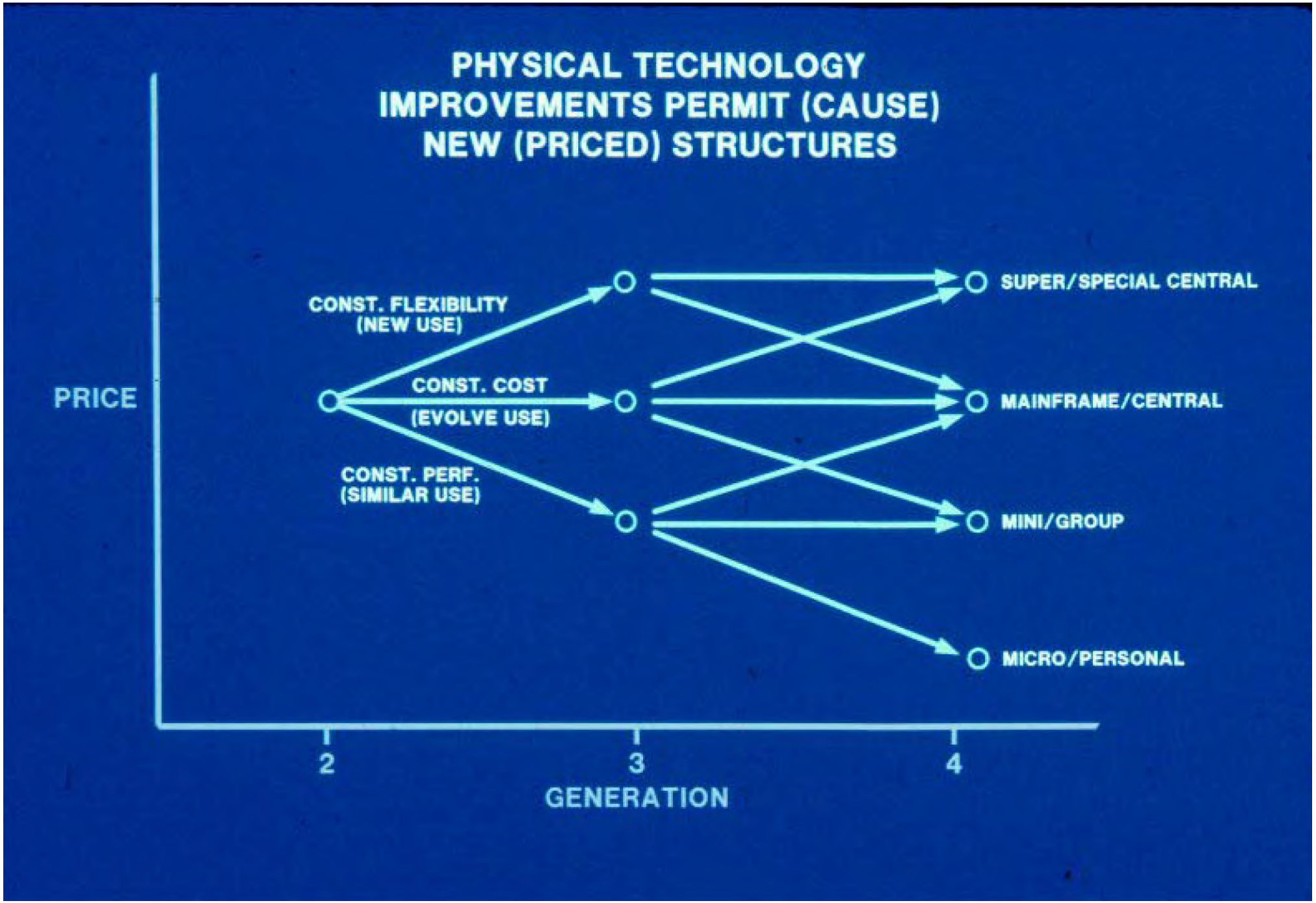
HIGH AVAILABILITY

GOAL IS TO SURVIVE SINGLE FAILURES:

FAILURE	RECOVERY
DISK VOLUME	VOLUME SHADOWING BY DISK SERVER
DISK SERVER	TWO DISK SERVERS AND DUAL PORTED DISKS
VAX	RECOVERY UNITS LOCK MANAGER
APPLICATION	RECOVERY UNITS JOURNALLING

DATA INTEGRITY TOOLS

- VOLUME SHADOWING
- JOURNALLING
- RECOVERY UNITS
- BACKUP


PHYSICAL TECHNOLOGY
IMPROVEMENTS PERMIT (CAUSE)
NEW (PRICED) STRUCTURES
PRICE
CONST. FLEXIBILITY
(NEW USE)
CONST. COST
(EVOLVE USE)
CONST. PERF.
(SIMILAR USE)
SUPER/SPECIAL CENTRAL
MAINFRAME/CENTRAL
MINI/GROUP
MICRO/PERSONAL
2
3
4
GENERATION

SEMICONDUCTOR-BASED COMPUTER GENERATIONS

1958 - 1990+

GENERATION	2 (TRANSISTOR)	3 (SSI, MSI)	4 (LSI)	5 (VLSI)	6 (ULSI)
BEGIN USE	1958	1964	1972	1980+	1958 - 1990
EVENT	VACUUM TUBE ALT.	MINICOMPUTER	MICROPROCESSOR (ON A CHIP)	MICROCOMPUTER (ON A CHIP)	COMPUTER SYSTEM (ON A CHIP)*
GATES/CHIP	1	10 - 100	1000	100,000	1M ~ 10M
BITS/CHIP**		1 ~ 2	1K	65K ~ 256K	1M BYTE

* ALL ELECTRONIC

** PAST RATE AT ISSCC + $2^{t - 1962}$

FACTOR OF 100 CHANGE REQUIRES ~ 6.6 YEARS

SEMICONDUCTOR-BASED COMPUTER GENERATIONS

1958 - 1990+

GENERATION	2 (TRANSISTOR)	3 (SSI, MSI)	4 (LSI)	5 (VLSI)	6 (ULSI)
EFFECT ON:					
4 BIT/10 ***			Pc	C	SYSTEM
8 BIT/16				Pc	C SYSTEM
16 BIT/20-24					Pc C SYSTEM
32 BIT/24-32					Pc C SYSTEM

*** DATA-TYPE/ADDRESS LENGTH

TABLE OF COMPUTING GENERATIONS, WITH NEED, USE AND STRUCTURES

GENERATION	HIGH LEVEL NEED	SPECIFIC USE	COMPUTER STRUCTURE
	TAXES, LAND	COUNTING	ABACUS, COUNTING TAB.
MANUAL 4 p.c. 1600	TRADE & EXPLORATION	ARITHMETIC	PASCAL, NAPIER'S TABLES, & GUNTER'S SCALE
MECHANICAL 3 p.c. 1800	INDUSTRIAL	SURVEY, NAVIGATION, LOOM CONTROL	ARITHMOMETER, DIFFERENCE ENGINE, PLANIMETER, SLIDE RULE, & TABLES
ELECTRO- MECHANICAL 2 p.c. 1890	MASS PRODUCTION & CENSUS	CENSUS & MODERN ACCOUNTING	COMPTOMETER, ELECTRIC CALCULATOR, HOLLERITH & ACCOUNT- ING MACHINES

TABLE OF COMPUTING GENERATIONS, WITH NEED, USE AND STRUCTURES

GENERATION	HIGH LEVEL NEED	SPECIFIC USE	COMPUTER STRUCTURE
ELECTRONIC (THERMIONIC) 1 p.c. 1930	POWER, HIGHWAY & COMMUNICATION GRIDS	ENGINEERING CALCULATIONS & CRYPTOGRAPHY	NETWORK ANALYZER, MARK I, BELL LABS CALCULATORS, ENIAC, COLLOSUS
ELECTRONIC (MAGNETIC) 1 c. 1945	DEFENSE	WAR-MACHINE CONTROL VIA TABLES & REAL TIME	EDVAC, EDSAC, IAS, WHIRLWIND, LGP30, IBM 650, 701, 709, UNIVAC
TRANSISTORS 2 c. 1958	SPACE & SCIENCE	AIR DEFENSE & TRAFFIC CONTROL; ENGINEERING & SCIENCE EDUCATION	TX-0, IBM 7090 ATLAS, STRETCH

TABLE OF COMPUTING GENERATIONS, WITH NEED, USE AND STRUCTURES

GENERATION	HIGH LEVEL NEED	SPECIFIC USE	COMPUTER STRUCTURE
INTEGRATED CIRCUITS 3 c. 1966	TRANSPORT FLOW CONTROL & WELFARE	PROCESS CONTROL & SOCIAL ACCOUNTING	PDP-8, B5000, PDP-6, IBM 360, 6600
LSI 4 c. 1972	ECONOMIC MODELS & R.T. CONTROL	INTERACTIVE COMPUTING	INTEL 4004, 8008, VAX-11, CRAY 1
VLSI 5 c. 1980	ENERGY & PRODUCTIVITY	OFFICE & HOME COMPUTING	
ULSI 6 c. 1985	INFORMATION & PROGRAM OVERLOAD	KNOWLEDGE BASED SYSTEMS	

TABLE OF COMPUTING GENERATIONS, WITH NEED, USE AND STRUCTURES

GENERATION	HIGH LEVEL NEED	SPECIFIC USE	COMPUTER STRUCTURE
ELECTRO-OPTICAL 7 c. 1990	ARTS, LEISURE, FOOD & ENERGY CRISIS	TRAVEL SUBSTITUTE & ENVIRONMENTAL MANAGEMENT	
PARTICLE 8 c.	COMPUTER-ASSISTED MICRO-ENVIRONMENTAL		

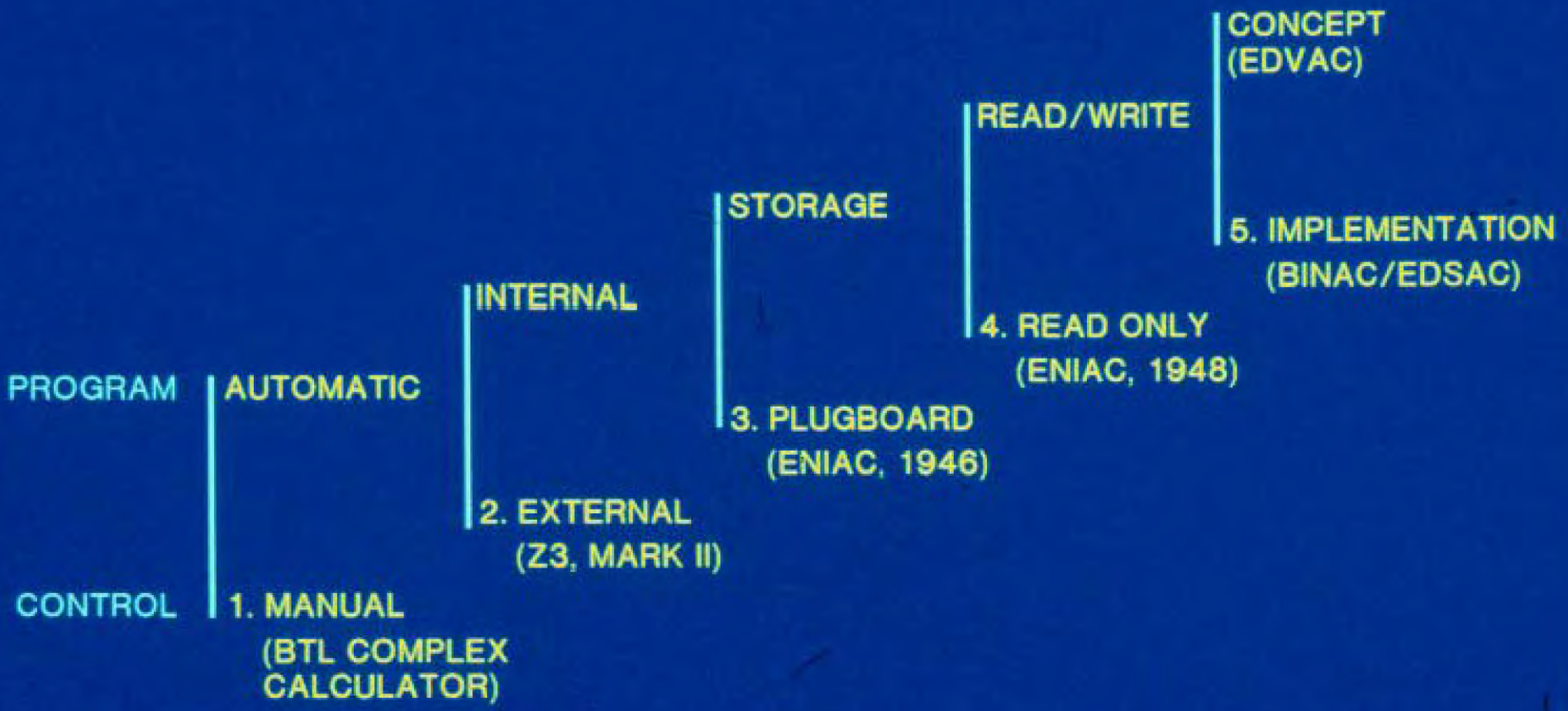
FOUR GENERATIONS OF MINICOMPUTERS

	MIT'S WHIRLWIND	PDP-1	8/I	LSI-11
GENERATION	FIRST (1950)	SECOND (1960)	THIRD (1968)	FOURTH (1975)
COST	?	120,000	10,000	650
PACKAGE	BUILDING	4 CABINETS	BOX	BOARD
SIZE	50'X50'X20'	8'X2.5'X6'	2'X2'X2'	8.5"X10"X.5"
POWER (WATTS)	150,000	2,500	250	50
SPEED (MEMORY ACCESS/SECOND)	80,000	200,000	600,000	1,000,000

FOUR GENERATIONS OF MINICOMPUTERS

	MIT'S WHIRLWIND	PDP-1	8/I	LSI-11
GENERATION	FIRST (1950)	SECOND (1960)	THIRD (1968)	FOURTH (1975)
COST	?	120,000	10,000	650
PACKAGE	BUILDING	4 CABINETS	BOX	BOARD
SIZE	50'X50'X20'	8'X2.5'X6'	2'X2'X2'	8.5"X10"X.5"
POWER (WATTS)	150,000	2,500	250	50
SPEED (MEMORY ACCESS/SECOND)	80,000	200,000	600,000	1,000,000

METROPOLIS' EVOLUTION OF PROGRAM CONTROL MODES



CN26,1

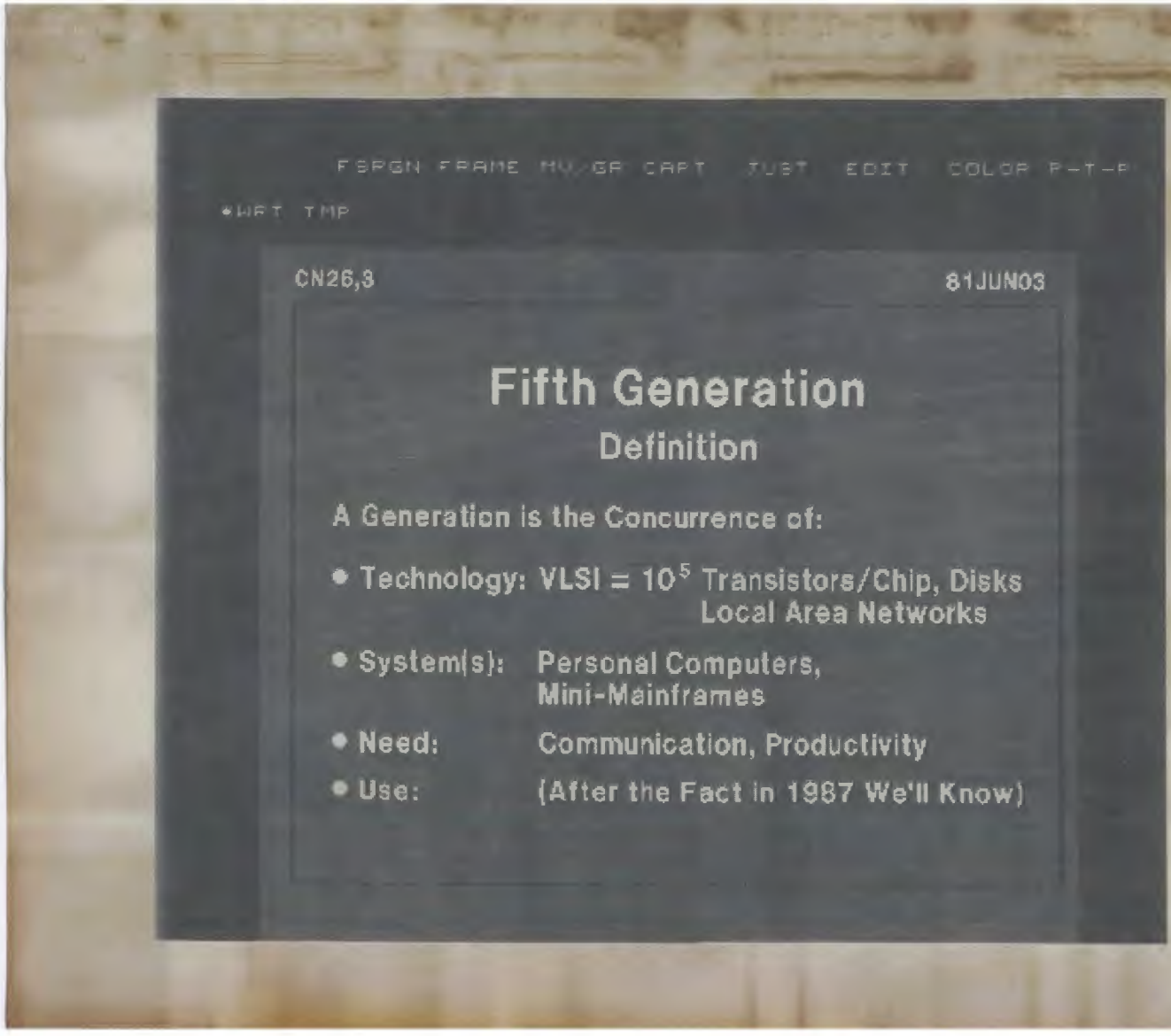
The Transitions

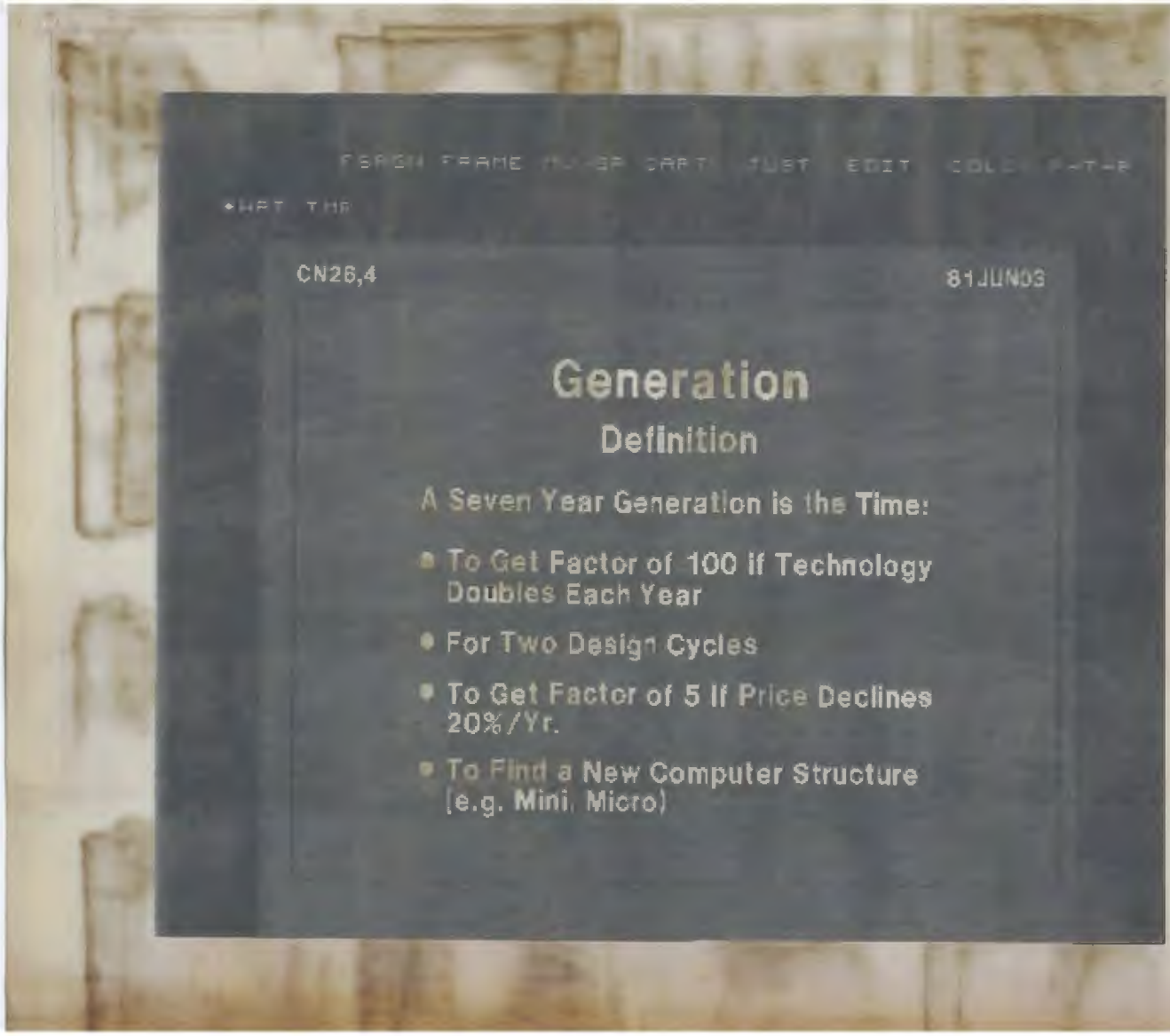
- Technology Transition
- Transition to Distributed Computing Based on Local Area Networks (NI)
- Transition to Personal Computers from Minis & Mainframes
- Transition from Conventional Rack & Stack 16-Bit Computers
- Transition to Software for End Use Versus Programmer Tools
- Transition in Hardware Design Skills

The Transitions

Transitions Imply Change (And Pain) In:

- What We Engineer (I.E. Projects)
- How We Design
- How Computers are Sold, Produced, Distributed & Used


FSPGN FRAME MV/GR CRPT JUST EDIT COLOR P-T-P
*WPT TMP
CN26,3
81JUN03
Fifth Generation
Definition
A Generation is the Concurrence of:
• Technology: VLSI = 10^5 Transistors/Chip, Disks
Local Area Networks
• System(s): Personal Computers,
Mini-Mainframes
• Need: Communication, Productivity
• Use: (After the Fact in 1987 We'll Know)


CN26,4
81JUN03
Generation
Definition
A Seven Year Generation is the Time:
• To Get Factor of 100 if Technology Doubles Each Year
• For Two Design Cycles
• To Get Factor of 5 if Price Declines 20%/Yr.
• To Find a New Computer Structure (e.g. Mini, Micro)

CN26.5 81JUN03

From the Generations Graph, We Can Observe:

- There is a wider range of useful systems, & these will be appealing to our customers, us & others; (For example, in 1985 we could be selling $1,000 computing terminals with the power of the original LINC, & $600K 10/20's)

CN26,6 81JUN03

From the Generations Graph, We Can Observe:

- The wide range of useful systems will force all suppliers to be more competitive & selective as new suppliers enter on a point product basis & as the 370 becomes a commodity
- IBM, Fujitsu, & others are likely to offer a 4341-2 class machine in our $40-100K Minicomputer Heartland

BG *

CN26,7 81JUN03

We Must Be Targeting the Following (for 1985)

- Cray 1 Power, $625K (or in 1990 for $250K)
- 3X Comet Power for $100K
- A sharable VAX (or big Micro) in $6.25K to $16K range
- A personal VAX (or big Micro) for under $6.25K
- A computing terminal with VT100 capability, & power of Apple II, or original LINC, for $1,000
- Computers in $400 to $1,000 range

make 'A' compatibility

We Have Not Provided Aggressive Enough Products Because:

- The Q & U Bus form factors have constrained system cost & size
- The 19" rack & stack, palletable form factor together with poorly packaged components, has been retained. Packaging in other, lower cost form factors enabling cardboard box shipment & customer merge is essential

82*

CN26.9

81JUN03

We Have Not Provided Aggressive Enough Products Because:

- The terminal has not been used as a package
- Point products have been insufficiently high quality, software supported, or cost-effective. Even $200 calculators are modular with mass storage, printer, modem & display options

DESIGN FRAME MAKE DRAFT JUST EDIT COLOR HI-P

•WRT TMP

CN26,10 81JUN03

Transition to Distributed Computing Based on NI, Interconnecting:

- Departmental & Central Computers to Each Other
- Personal Computers to Form Clusters
- Functional Server Components to Reduce the Number of Network Possibilities that are a Product of:
  - Hardware Systems
  - The 12 Operating Systems We Support
  - And the Desirable Protocols Including X.25, IBM, DECnet & Other Vendors

CN26,11 81JUN03

By Using the Server Concept Each System Can be Connected to NI with Specialized Servers As:

- Concentrators for Interconnecting Dumb Terminals & Personal Computers
- Gateways to Systems Using Other Protocols
- Repeaters & Interfaces to Other Networks
- Central Functional Servers for Files & Printing
- Real Time Front Ends

86

FSRGN FRAME MUJGR CAPT TUST EDIT DO OR P-T-P

•WPT TMP

CN26,12 81JUN03

Transition to Personal Computers from Minis & Mainframes

Timeshared Computers are Affected in Several Ways:

- Direct, Stand Alone Use As an Alternative
- More Terminal Load Can be Put on a Given Computer
- Interconnected Clusters of Personal Computers are a Substitution

FSRGN FRAME MULGR CAPT JUST EDIT [illegible] P-T-P

*WPT TMP

CN26,13 81JUN03

Transition from Rack & Stack 16-Bit Computers

The Alternatives:

- 16-Bit microprocessor cards & systems which have 24-32 bit memory address space & supplied by both semicomputer companies & their OEMs Transportable Systems such as UNIX are aimed at establishing hardware to be a commodity
- Board & box level systems that are oriented to modern special chip I/O as supplied by the semicomputer suppliers

CN26,14 81JUN03

Transition from Rack & Stack 16-Bit Computers

The Alternatives:

- Personal Computer & Clusters
- VAX & other 32-Bit Architectures
- Emerging commodity priced 370s in this price class
- Better Box-level form factors not possible with 19", FAT produced, Q - &, Unibus Systems; Systems must be shipped in cardboard boxes, integrated by the customer, & when broken, self-diagnosing with customer replaceability

BD*

CN26,15 81JUN03

Transition from Terminals to Computing Terminals

The Major Transition for Terminals is Semantic, i.e. What is a Terminal?

Terminals Must Change in the Following Ways:

- Larger Personal Computers are an alternative to our conventional, dumb terminals
- All terminals introduced beginning in FY83 must be customer programmable with at least firmware ROMS and RAM buffers

BG

CN26,16 81JUN03

Transition from Terminals to Computing Terminals

Terminals Must Change in the Following Ways:

- The interconnection, whether it be U.S. or European Modem, NI, or IBM Emulator, must be built into the terminal
- Decreasing memory cost based on 64K chip will offer fully programmable screens, which in turn will automatically provide graphics
- Higher resolution, full-page & color displays

CN26,17

Transition to Software for End Use vs. Programmer Tools

We Can Identify These Needs:

- Direct use in the office, including providing the ability of OEM's, office managers, organization & the individuals to tailor their systems
- Better human engineering at screen & in documentation; Documents & help should be built-in
- All products must be modifiable for use with natural languages
- Applications building tools for particular professional & commercial environments

Transition in Hardware Design Skills

The Immediate Transitions for System Designers Include:

- Standardization & use of general purpose controllers & processors for conventional controllers. We are not using enough standard VLSI! This implies options are programmed
- Use of gate arrays & other LSI to lower cost of all jelly bean & non-processor logic

CN26,19 81JUN03

Transition in Hardware Design Skills

The immediate Transitions for System Designers include:

- VLSI design, where processors & controllers are placed on a single chip
- Identification of either general purpose or special purpose computers based on VLSI for building the non-processor portion of systems to drastically reduce system cost
- Generally dealing with much more complexity

CN26,20 81JUN03

Departmental Timesharing of the 70's ('65 - '85)

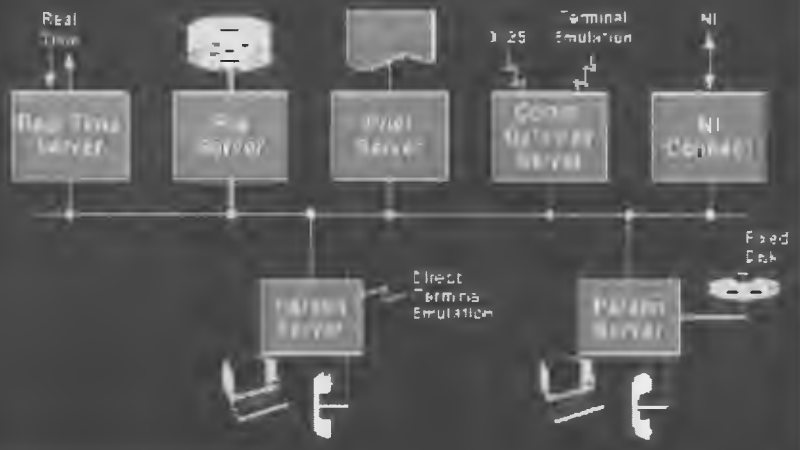
Personal Computers with Termina Emulation 1978 - 85

BG

CN26.21

81JUN03

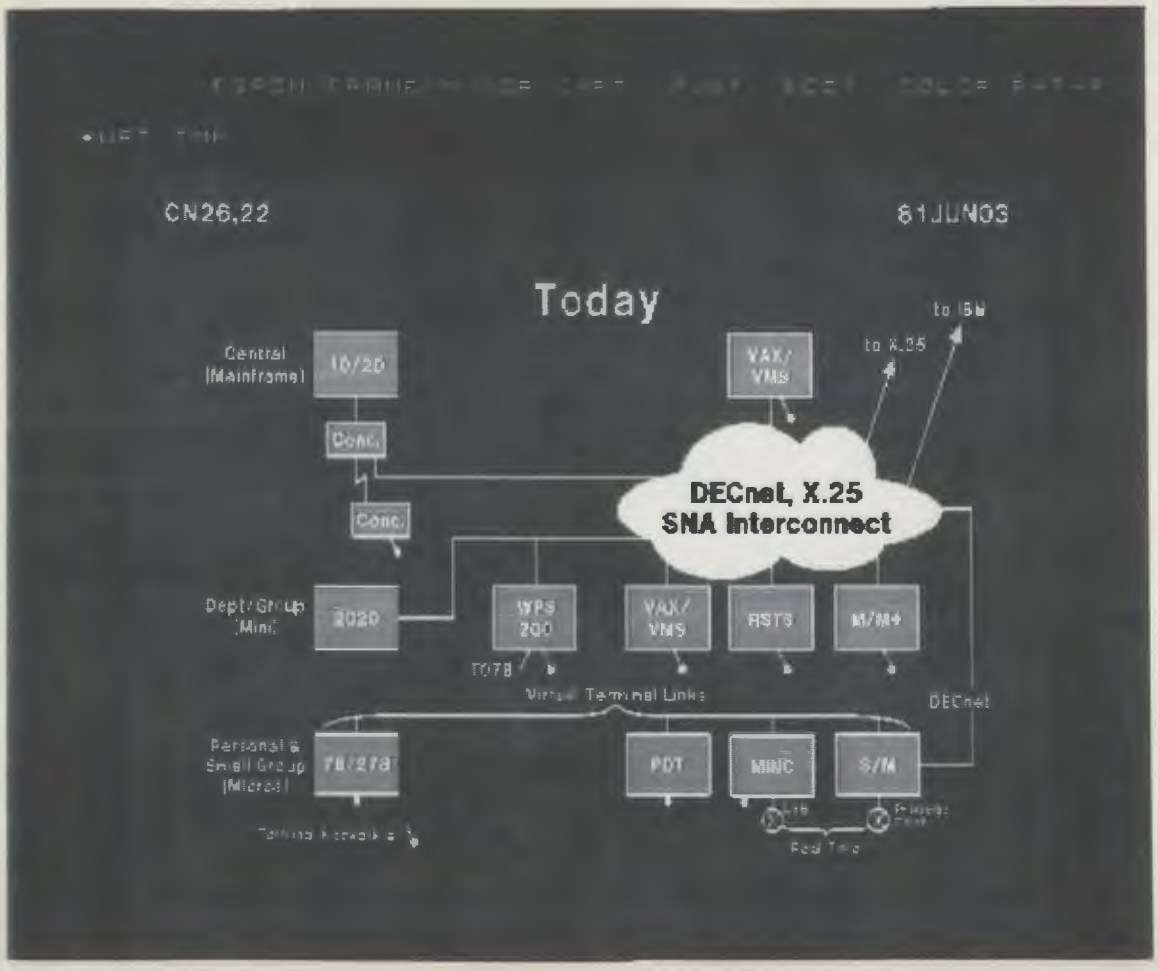
Personal Computer Clusters & Networks of the '80s (> 1981)



RD

CN26,22

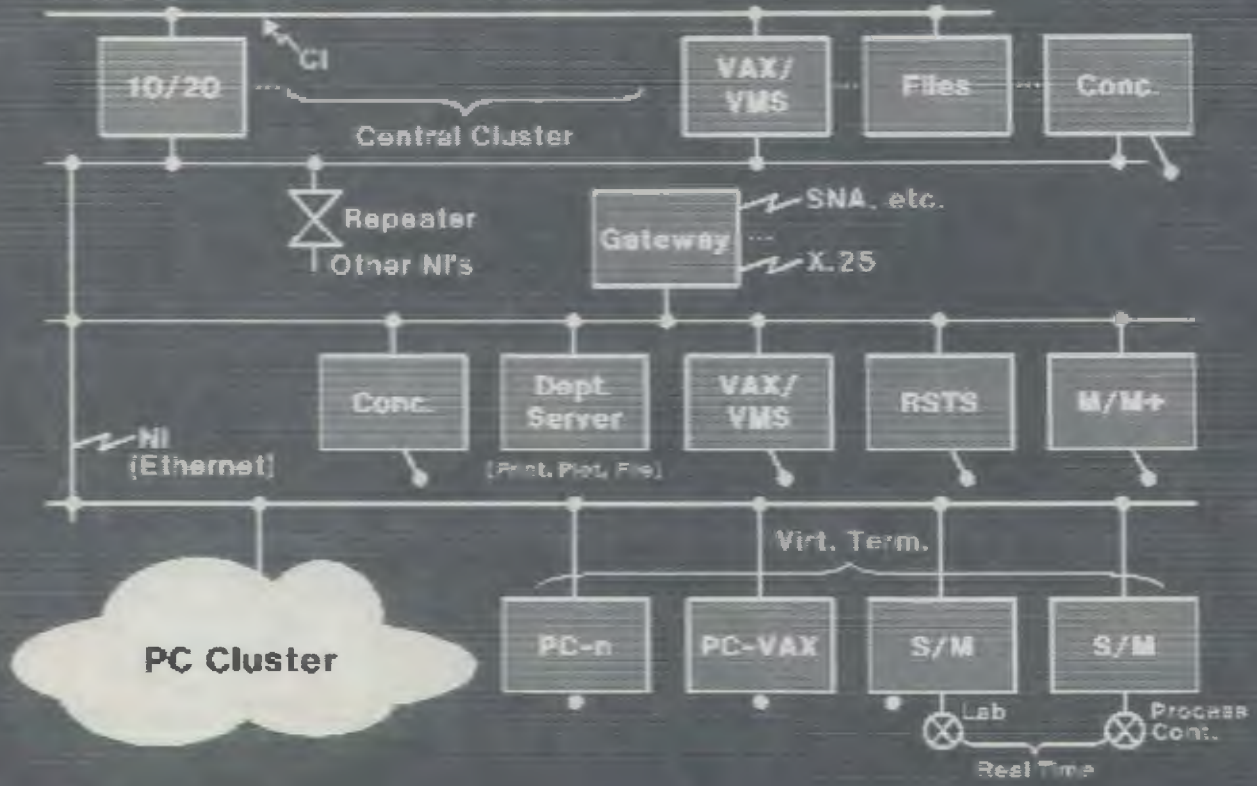
81JUN03



RD

CN26.23 81JUN03

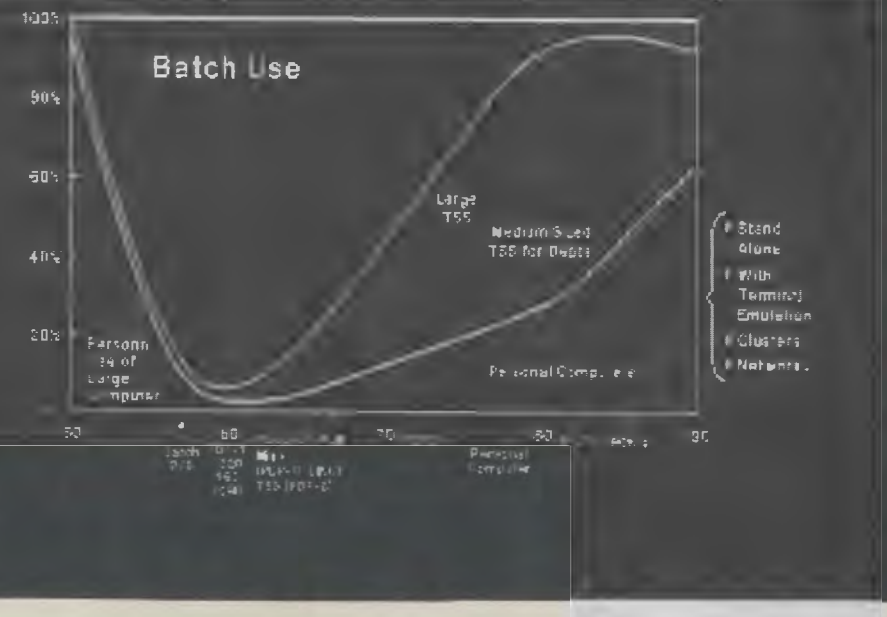
The Product Strategy



BG*

CN26,24 ■ ■ 81JUN04

Estimated (G. Bell) Percentage (in # Terminals)
of Computer Use vs. Time (1950–1990)



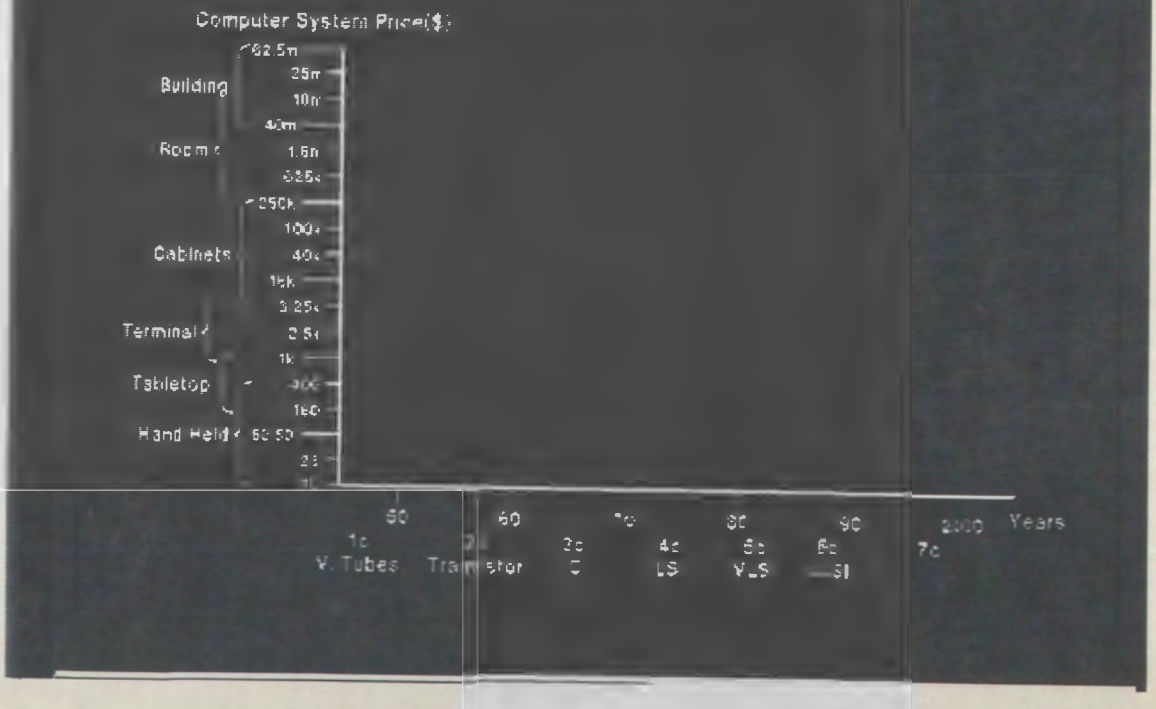
20

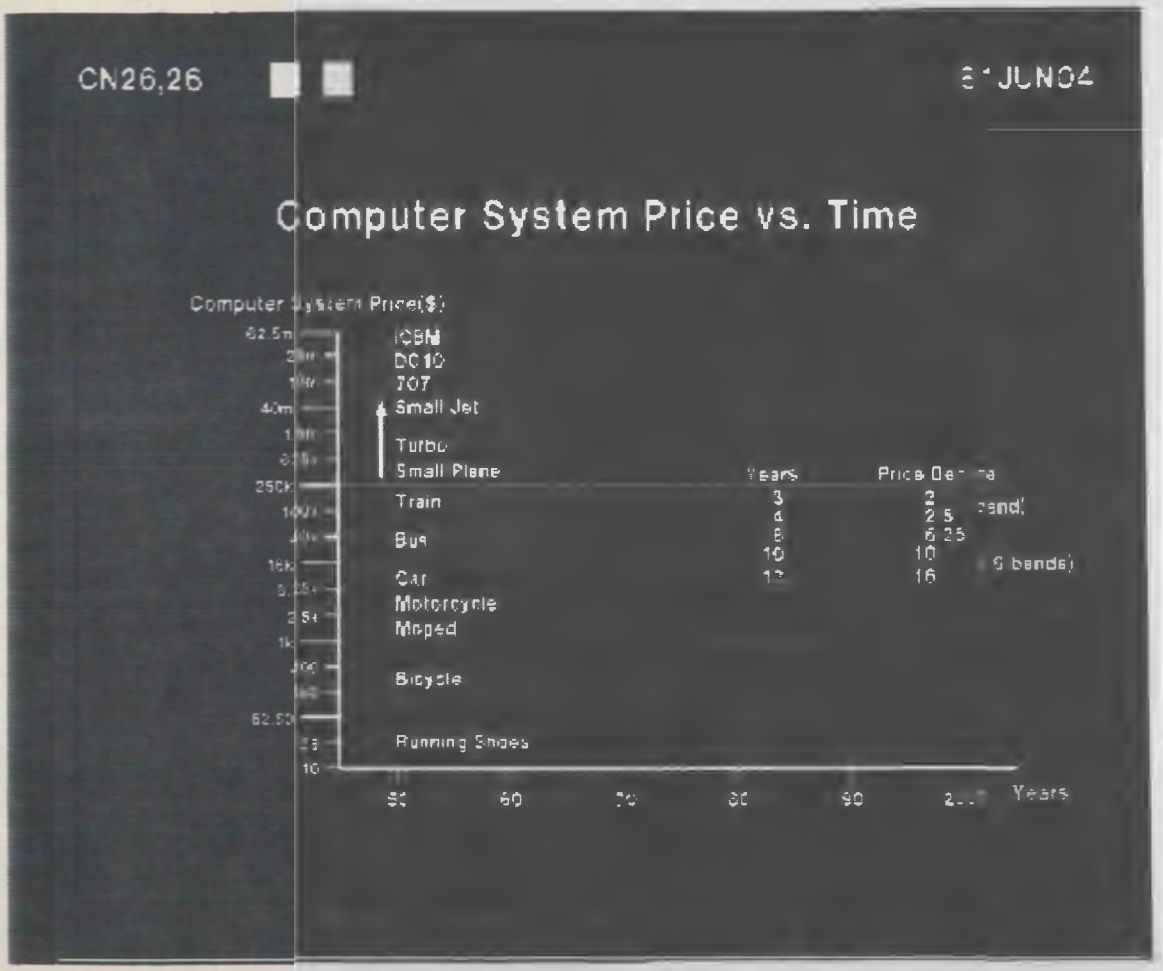
BG *

CN26.25

81JUN04

Computer System Price vs. Time




CN26,26
JUN04
Computer System Price vs. Time
Computer System Price($)
62.5m
40m
250k
16k
62.50
10
ICBM
DC10
707
Small Jet
Turbo
Small Plane
Train
Bus
Car
Motorcycle
Moped
Bicycle
Running Shoes
Years
Price De
Years
3
4
6
10
16
2
2.5
6.25
10
(6 bands)
60
70
90
Years

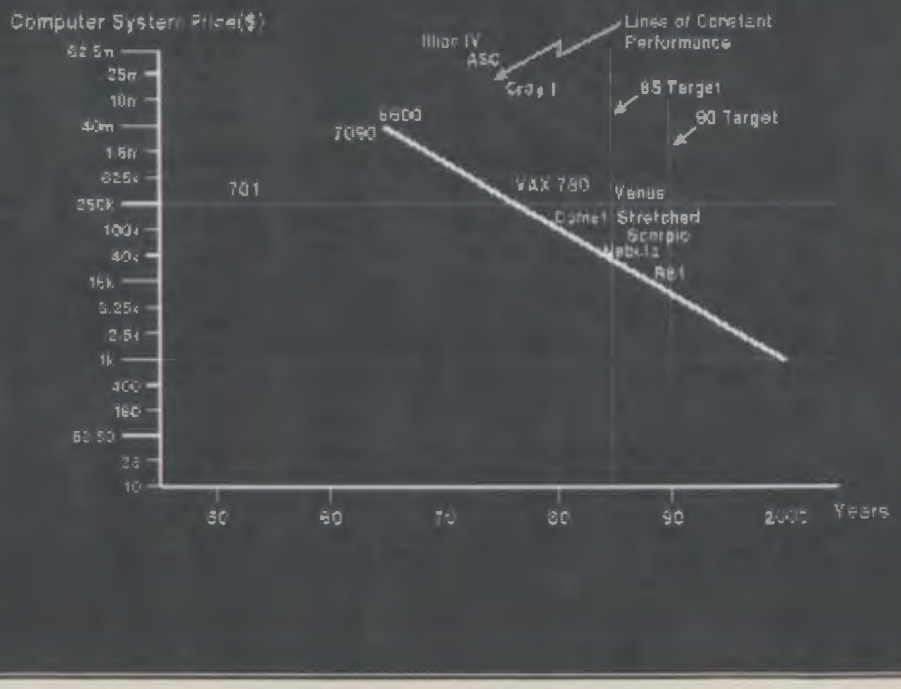
BJ

BC

CN26.27

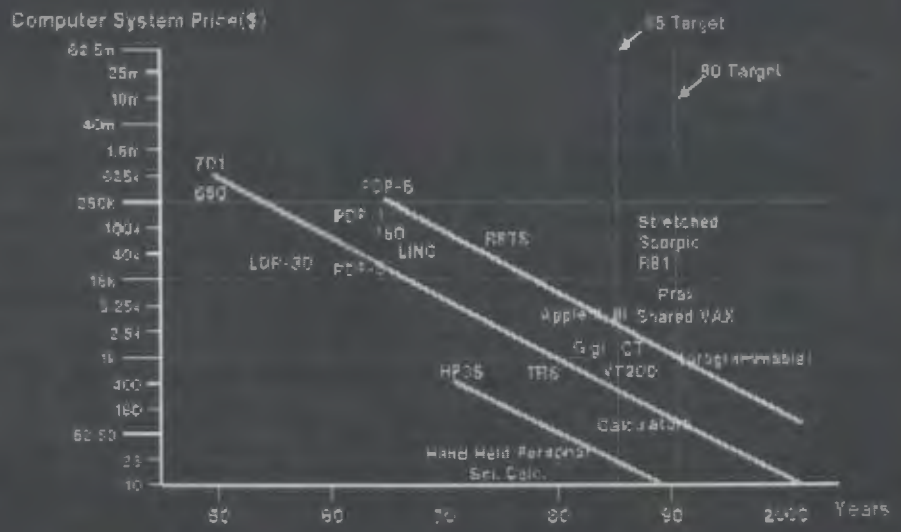
81 JUN04

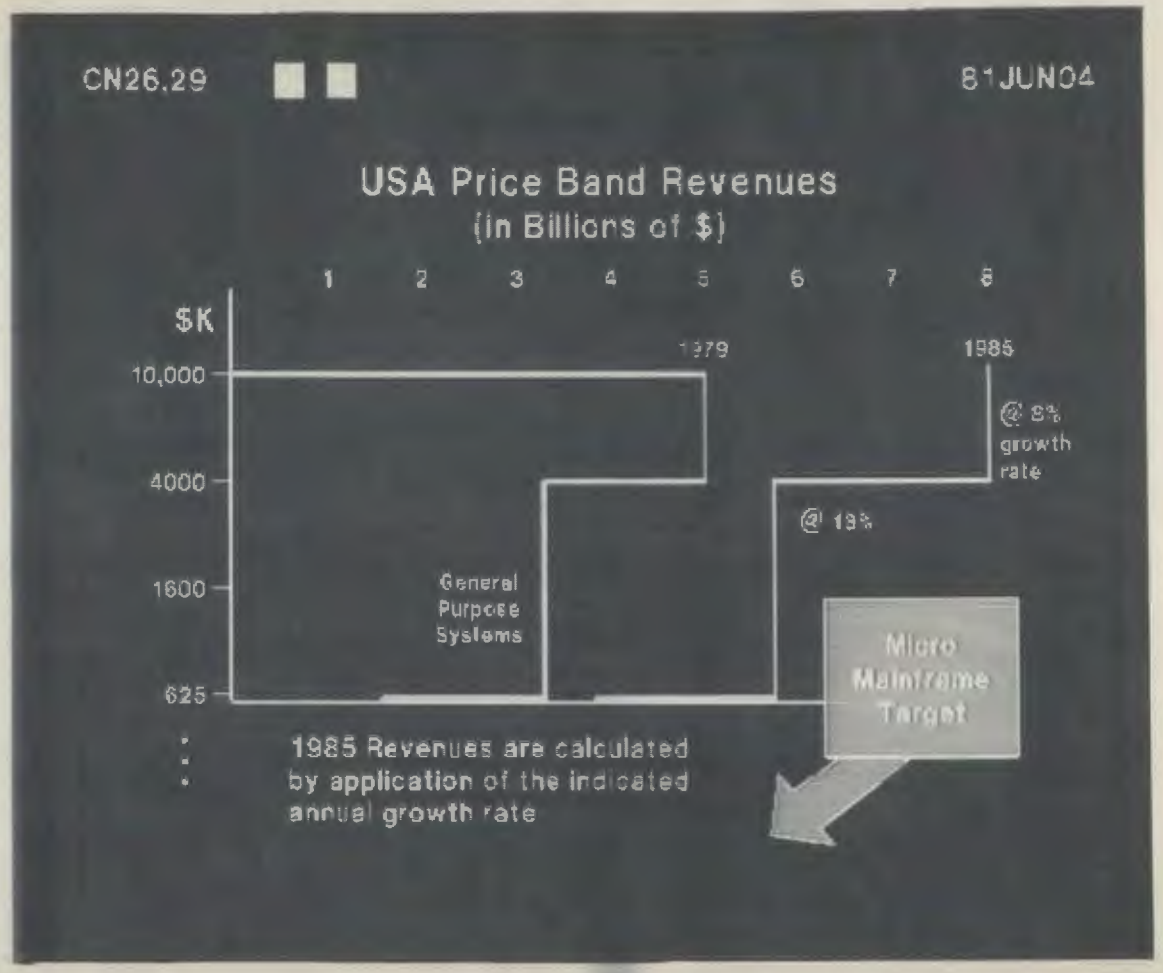
Computer System Price vs. Time

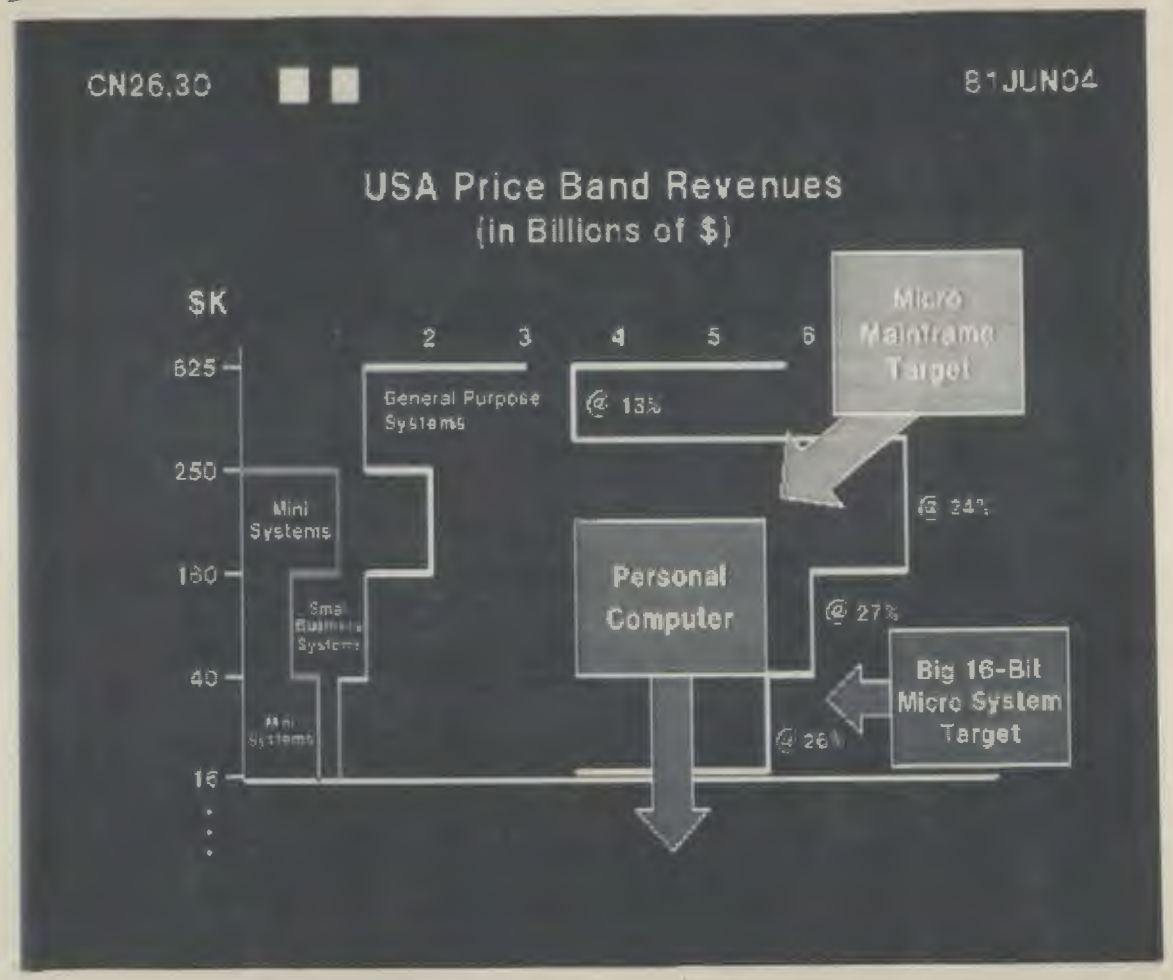


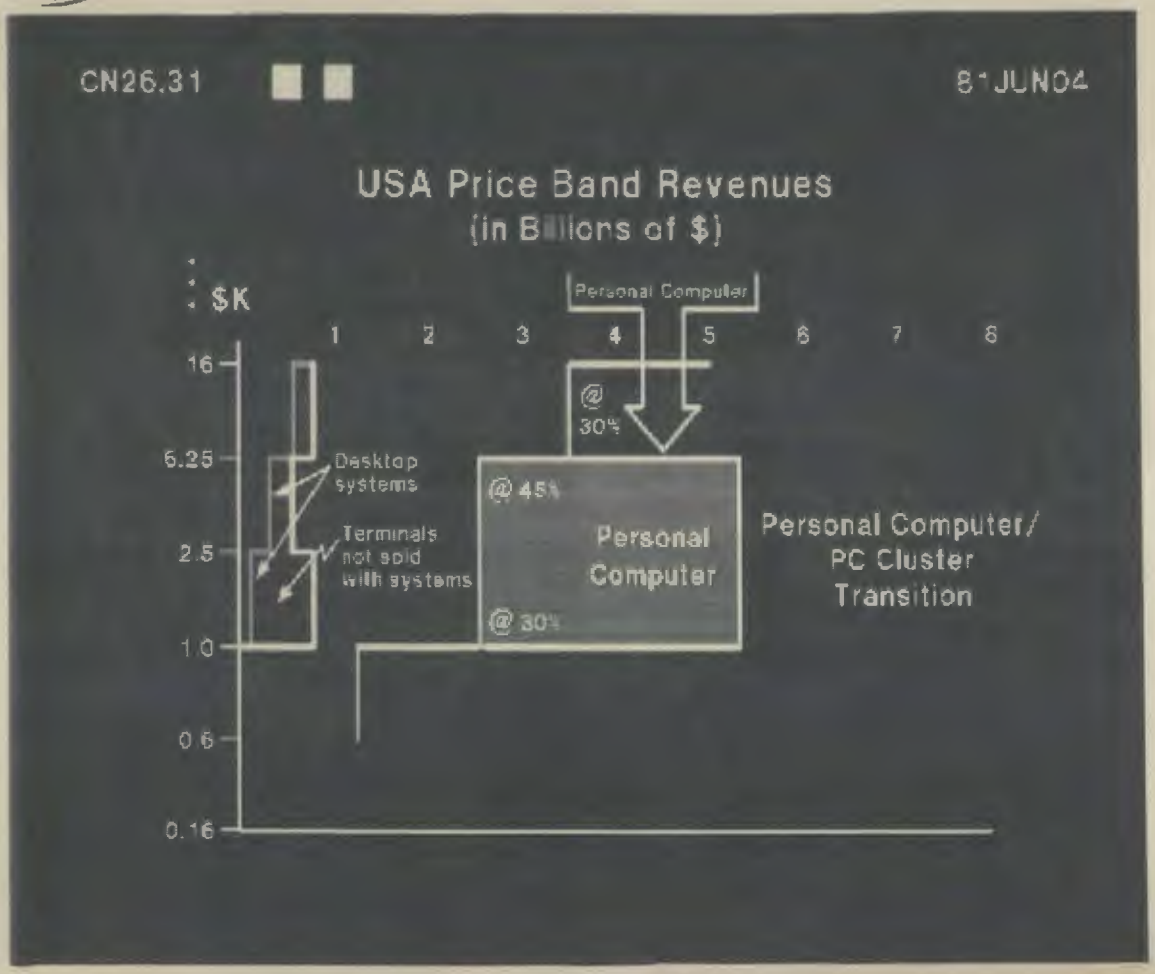
CN26,28 ■ ■ 81JUN04

Computer System Price vs. Time




CN26.29
81JUN04
USA Price Band Revenues
(in Billions of $)
1 2 3 4 5 6 7 8
$K
10,000
4000
1600
625
1979
1985
@ 8% growth rate
@ 19%
General Purpose Systems
Micro Mainframe Target
1985 Revenues are calculated by application of the indicated annual growth rate


CN26.30
81JUN04
USA Price Band Revenues
(in Billions of $)
$K
625
250
180
40
16
2
3
4
5
6
General Purpose Systems
@ 13%
Micro Mainframe Target
Mini Systems
@ 34%
Personal Computer
@ 27%
Big 16-Bit Micro System Target
@ 26%


CN26.31
81JUN04
USA Price Band Revenues
(in Billions of $)
$K
Personal Computer
1
2
3
4
5
6
7
8
16
6.25
2.5
1.0
0.6
0.16
@ 30%
Desktop systems
Terminals not sold with systems
@ 45%
Personal Computer
@ 30%
Personal Computer/
PC Cluster
Transition

To: Pog, gVPC, Barnlae, Lane, Connel, Kerr, Avram, Folsom, Bang Cioffi + Lydal + PET

These 3 slides (definitions) may be of interest to you. They try to segment what and how computing is (and may be) done.

I use them.

gordon

A TIMESHARING COMPUTER consists of:
•processor and primary memory;
•secondary memory for programs and data;
•communications links to other computers and to
•human interface terminals (eg. CRT and keyboard).

A timesharing computer is used interactively by several persons in a shared fashion. The computer belongs to a group, while the terminal usually belongs to an individual.

A PERSONAL COMPUTER consists of:
•processor and primary memory;
•secondary memory for programs and data; ← (files are on line)
•communications link to other computers; and
•human interface components (eg. CRT and keyboard).

A personal computer is used interactively by one person at a time. The computer usually belongs to an individual. (LINC is the first to satisfy this definition, if you ignore the additional constraint that says a PC must be portable!)

A CENTRAL FACILITY (mainframe) provides:
•network communications among computing nodes, with conventions for exchanging data;
•archival storage for group and personal facilities;
•large, shared, central data bases;
•large, special facilities beyond group or person (eg. printing, plotting, high performance processing, electronic mail);
•general computation on a service bureau basis.

A GROUP LEVEL FACILITY (timeshared minicomputer) provides:
•ability to be part of communicating network;
•intra-group communications via the facility;
•shared programs and data for a single group;
•special facilities for the group (eg. microprocessor debug, simulation, printing, plotting, processing);
•shared, general computation for members of the group.

A PERSONAL FACILITY (personal computer) provides:
•ability to be part of communicating network;
•private programs and data for an individual;
•fast response for simple human interactive (eg. editing) tasks.

The DEC 3-level Computing environment.

Comments?

DEC'S PRODUCT STRATEGY

PROVIDE A SET OF HOMOGENEOUS DISTRIBUTED COMPUTING SYSTEM PRODUCTS SO A USER CAN INTERFACE, STORE INFORMATION AND COMPUTE, WITHOUT RE-PROGRAMMING OR EXTRA WORK FOR THE FOLLOWING COMPUTER SYSTEM SIZES AND STYLES:

- AS A SINGLE USER, PERSONAL COMPUTER WITHIN A TERMINAL, AND EVOLVING TO PC CLUSTERS AND PC NETWORKS;
- AT A SMALL, LOCAL SHARED, DEPARTMENTAL COMPUTER SYSTEM, AND
- VIA A CLUSTER OF LARGE CENTRAL COMPUTERS
- WITH INTERFACING TO OTHER SYSTEMS FOR REAL TIME PROCESSING; AND
- ALL INTERCONNECTED VIA ETHERNET AND WIDE AREA NETWORKS

HOMOGENEOUS DISTRIBUTED COMPUTING APPROACH

(STRATEGIC TARGET FOR '85)

- ADOPT A SINGLE VAX-11/VMS ARCHITECTURE
- IMPLEMENT A WIDE RANGE OF PRODUCTS COVERING THE FOLLOWING COMPUTING "STYLES"
  - PERSONAL COMPUTING
  - TIMESHARED DEPARTMENTAL COMPUTING
  - CENTRAL COMPUTING
- INTERCONNECT THESE IN A HOMOGENEOUS NETWORK INCLUDING PERSONAL COMPUTING CLUSTERS
- BUILD CRITICAL AND UNIQUE APPLICATIONS

WHY THIS ARCHITECTURE?

- CUSTOMER INVESTMENT PROTECTED
  - DATA
  - PROGRAMMING
  - TRAINING
- HIGHEST FLEXIBILITY/COMPATIBILITY IN THE INDUSTRY
  - $50 CHIPS TO SEVERAL M$ CENTRALIZED CLUSTERS
- FEWEST SYSTEMS NEEDED TO SPAN RANGE, RESULTING IN
  - LOWER COST
  - HIGHER QUALITY
  - HIGHER RELIABILITY
- CLEAR DIRECTION LETS CUSTOMERS DEVELOP EFFECTIVE/FLEXIBLE PLANS
- FOCUS RESULTS IN RICHEST SET OF S/W TOOLS AND APPLICATIONS

FIFTH GENERATION

TECHNOLOGY

VLSI INCLUDING MEMORIES, LAN (CSMA/CD),
WINCHESTER DISKS AND HIGH RESOLUTION DISPLAYS

NEED

COMMUNICATIONS AMONG PEOPLE AND PROLIFERATING
COMPUTERS

STRUCTURE

- OFFICE AND HOME COMPUTING
- ? WHICH BUILDS THE BASIS FOR THE SIXTH GENERATION

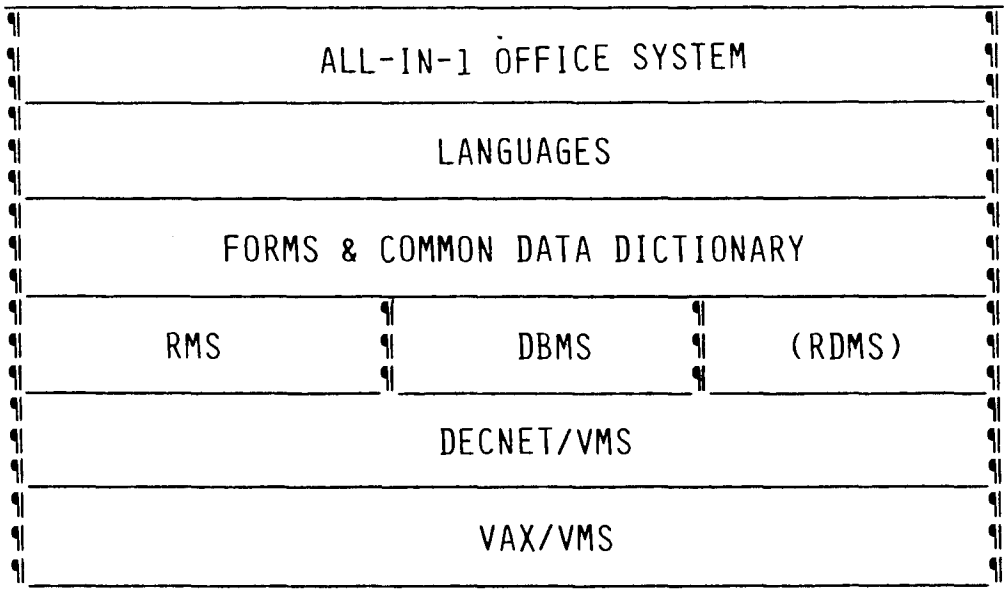
ETHERNET: THE UNIBUS OF FIFTH GENERATION BECAUSE IT IS THE STANDARD TO INTERCONNECT COMPUTERS AND FORM A FULLY DISTRIBUTED SYSTEM

COMPUTER GENERATIONS

- o A CONCURRENCE OF:
  - TECHNOLOGY
  - NEED
  - USE
  - STRUCTURE
- o GENERATION UNDER DEVELOPMENT TODAY IS THE FIFTH

GENERATION	NEED	USE	STRUCTURE
I. ELECTRONIC (MAGNETIC) 1945	DEFENSE	WAR MACHINE CONTROL	EDVAC, IAS WHIRLWIND, IBM 605
II. TRANSISTORS 1958	SPACE/SCIENCE	AIR DEFENSE AND CONTROL ENGR. AND SCIENTIFIC EDUCATION	TX-0, IBM 7090 ATLAS, STRETCH
III. INTEGRATED CIRCUITS 1966	TRANSPORTATION FLOW CONTROL AND WELFARE	PROCESS CONTROL AND SOCIAL ACCOUNTING	PDP-8, IBM 360 PDP-6, CDC 6600
IV. LSI 1972	ECONOMIC MODELS AND REAL TIME CONTROL	INTERACTIVE COMPUTING COMPUTERS FOR LOGIC	INTEL 4004, 8008, PDP-11 (RSTS) CRAY 1

VAX INFORMATION ARCHITECTURE
(VIA)



WIDE AREA NETWORK DEFINITION
(WAN)

- AGGREGATE OF HETEROGENEOUS SYSTEMS AND NETWORKS
- PURPOSE IS TO CONNECT SYSTEMS ACROSS A WIDE AREA
- RELATIVELY LOW SPEED INTERCONNECT (4-64KB/SEC) ... 128KB/SEC
  LOW CONNECTIVITY (PABX, CIRCUIT AND PACKET SWITCHES)
  SYSTEMS LOCATED IN DIFFERENT REGIONS
- COMMUNICATION SERVICES BETWEEN AUTONOMOUS SYSTEMS VIA
  DECNET AND GATEWAYS TO OTHER NETWORKS (X.25/SNA...)

EVOLUTION IN CENTRAL COMPUTING

LET'S DEFINE CLUSTERS

- AGGREGATION OF HOMOGENEOUS SINGLE AND MULTIUSER SYSTEMS (E.G., VAX/VMS, VAX/UNIX, DECSYSTEM 20, ALTOS, XEROX STAR)

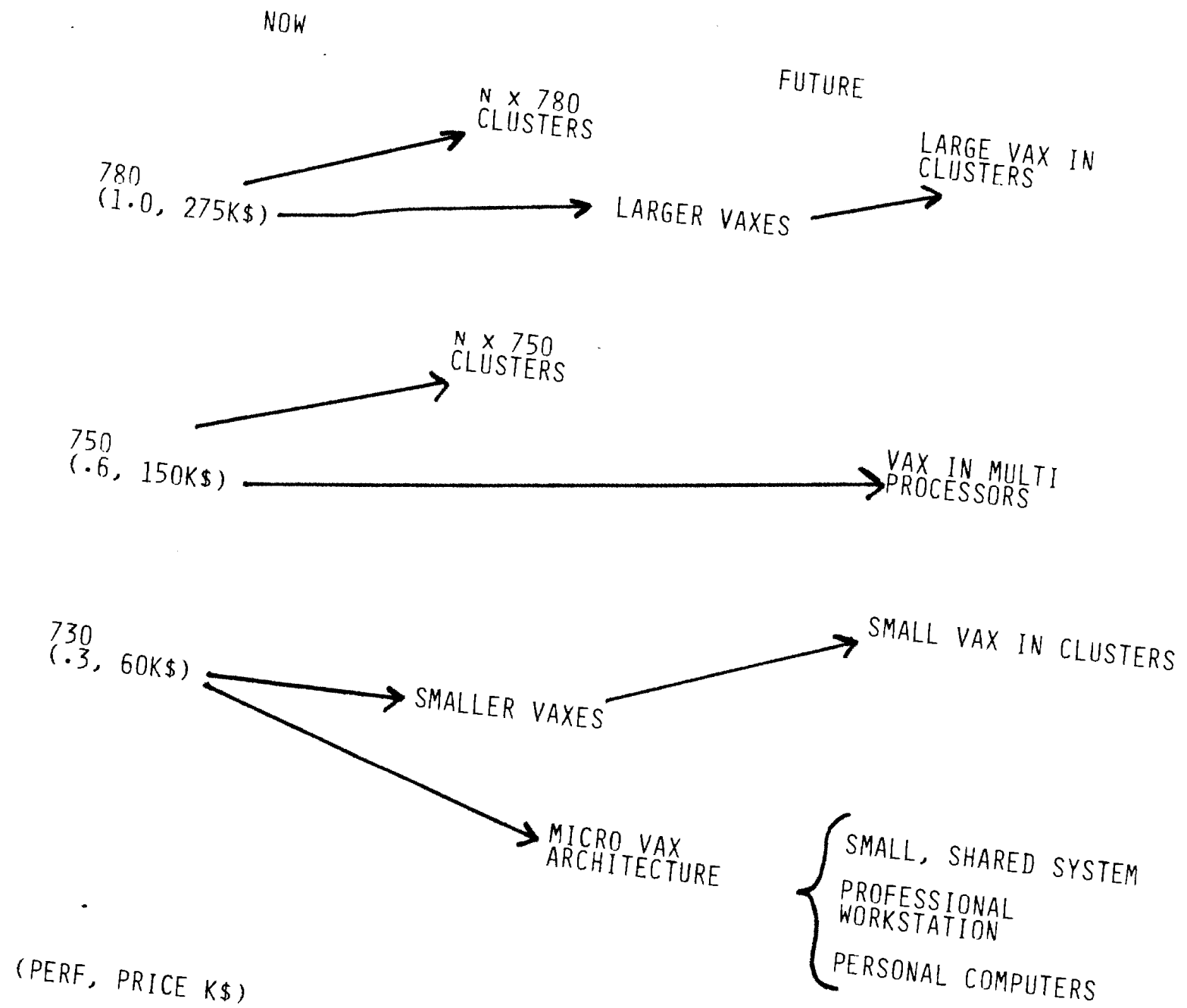
- BEHAVING AS A SINGLE, MULTIPLE ACCESS SYSTEM (USUALLY SHARING A COMMON FILE SYSTEM)

- HIGH SPEED INTERCONNECT (10-100 MBITS/SEC) WITH HIGH CONNECTIVITY AMONG SYSTEMS

- SYSTEMS LOCATED IN A SINGLE MACHINE ROOM OR OFFICE AREA

- EXTENSION OF LOW LEVEL O/S SERVICES (FILE, PRINT/PLOT) VIA RELIABLE INTERSYSTEM MESSAGE BASED "PROCEDURE ORIENTED" PROTOCOL

EVOLUTION OF VAX FAMILY



(PERF, PRICE K$)

PERF: 780 = 1.0

SIXTH GENERATION

- WILL BEGIN IN ROUGHLY 6 YEARS

TECHNOLOGY

- TRULY COST AND HIGH PERFORMANCE HARDWARE
- INSTALLED LAN'S AND HIGH BANDWIDTH WAN'S
- VOICE AND PICTURES

NEED

- INFORMATION OVERLOAD, PRIVACY AND PRODUCTIVITY

STRUCTURE

- KNOWLEDGE BASED SYSTEMS INCLUDING VARIOUS EXPERT SYSTEMS
- INTENSIVE COMMUNICATION OF ALL FORMS OF PEOPLE UNDERSTOOD DATA

USE

- SIGNIFICANT SUBSTITUTION OF COMPUTERS FOR OTHER INFORMATION PROCESSORS

DATA MANAGEMENT TRENDS

- RAPIDLY EXPANDING USE OF RELATIONAL SYSTEMS WITHIN NEXT TWO YEARS
- INTEGRATION OF MULTIPLE DB TECHNIQUES THROUGH SINGLE, EASY-TO-USE, INTERFACES (2-5 YEARS)
- EXTENSION OF DATA TYPES TO INCLUDE TEXT, VOICE, IMAGE (2-5 YEARS)
- DISTRIBUTION TO CLUSTER SERVERS (NOW) FOLLOWED BY "DATABASE" SERVERS (3-5 YEARS)
- ROBUST DISTRIBUTED COMMON DATA DICTIONARIES (2-3 YEARS)

TRENDS IN GRAPHICS

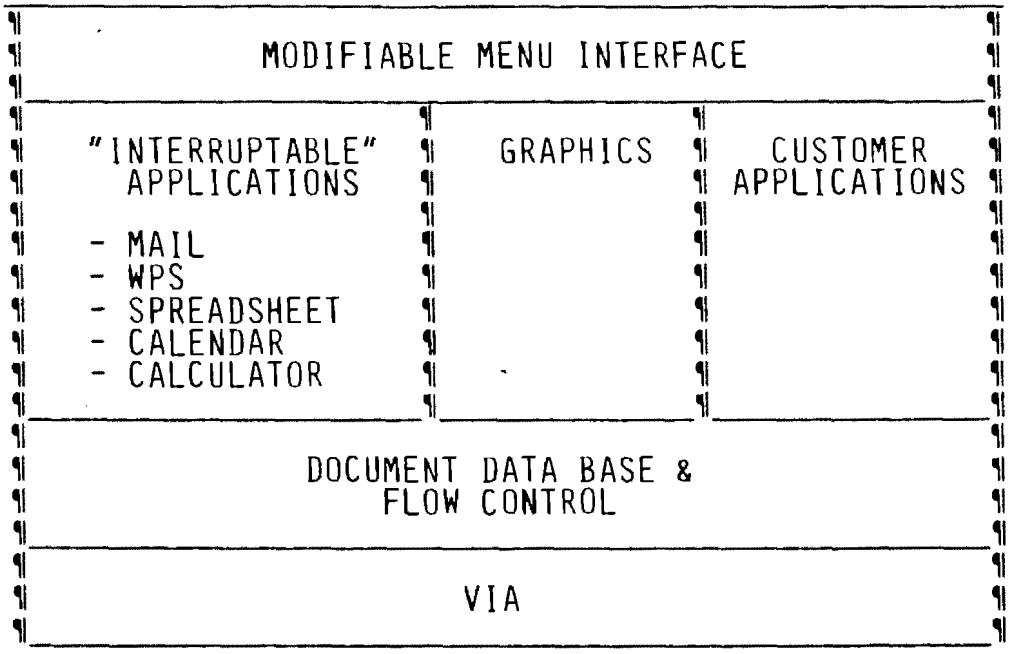
- o PROLIFERATION OF QUALITY GRAPHICS CAPABLE TERMINALS & PC WILL MAKE GRAPHICS COMMONPLACE IN NEXT TWO YEARS.

- o SIGNIFICANT INCREASE IN PROFESSION-SPECIFIC APPLICATIONS AND LEVEL OF INTEGRATION IN OFFICE SYSTEMS.

EXAMPLE: CURRENT ALL-IN-1 GRAPHICS

PRODUCT	USE	INTEGRATION
DECPLOT	DECISION SUPPORT MANAGEMENT SUMMARY	- CODASYL, ISAM DB'S - DUNN CAMERA & GRAPHICS PRINTER
DECSLIDE	PRESENTATION GRAPHICS	- IMAGE LIBRARY - LASER PRINTER
FINGRAPH	FINANCIAL MANAGEMENT (OPERATING RESULTS)	- "ACCOUNTING" APPLICATIONS - PRESENTATION COLOR MONITORS
EMPIRE	COMPLEX MODELING / DECISION SUPPORT	- DEPT. DB - PC-BASED GRAPHICS

ALL-IN-1 ARCHITECTURE



EVOLUTION OF PERSONAL COMPUTING

"DUMB" TERMINALS

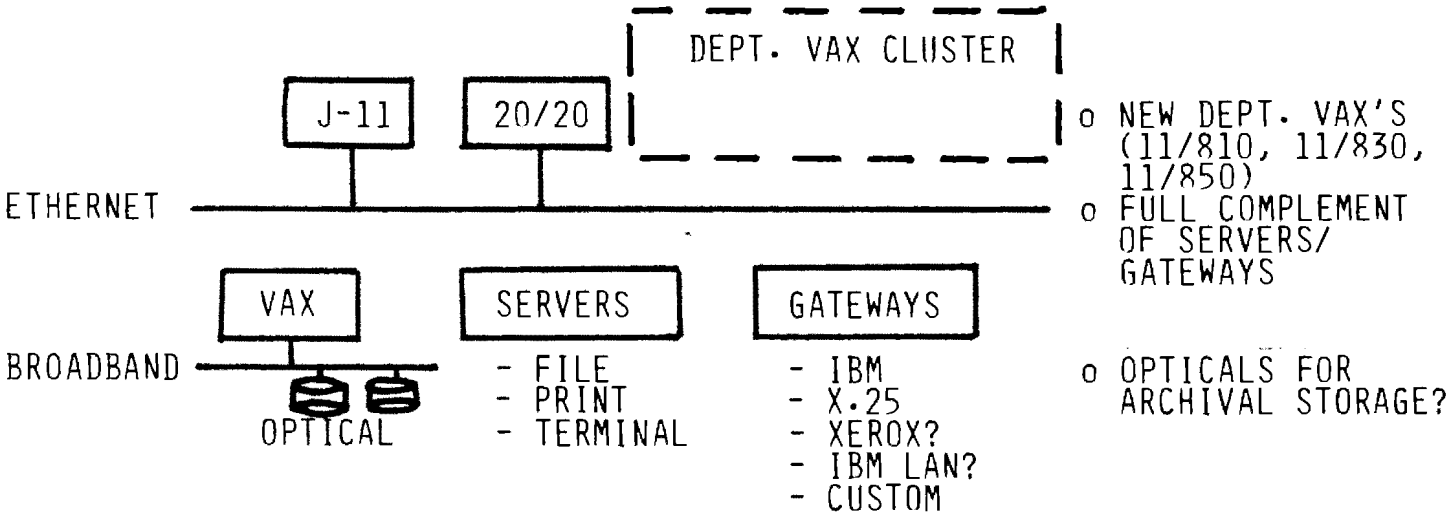
- EVERY TERMINAL WILL BECOME A COMPUTING TERMINAL!

TODAY		1983		1984
UBIQUITOUS DUMB TERMINAL	----->	16 BIT PDP-11 STANDARD IN TERMINAL	----->	TERMINALS HANG ON ETHERNET
- VT100 INDUSTRY STANDARD		- PC KEYBOARD, MONITOR		- ACCESS TO ETHERNET DIRECTLY
		- MEDIUM RESOLUTION GRAPHICS		- ACCESS VIA TERMINAL SERVER
		- EMULATES OTHER TERMINALS		- TELEPHONE AND VOICE MANAGEMENT

EVOLUTION OF PERSONAL COMPUTING

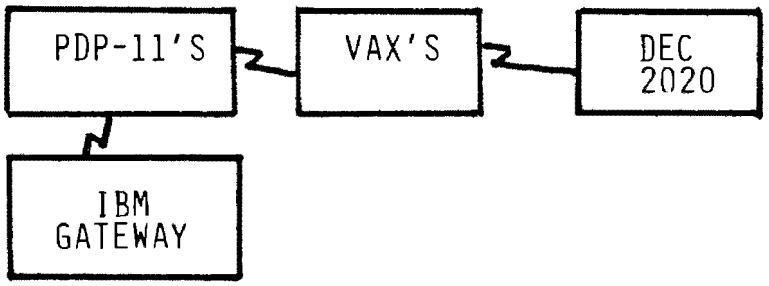
TODAY	1983-1984	1985
COMPATIBLE 16 BIT PC -->	PC CLUSTERS -->	COMPATIBLE 32 BIT PC
• PDP-11 BASED	• LOW COST "SMALL ETHERNET" FOR CLUSTERS	• μVAX
• COMPATIBLE FILES, TOOLS, LANGUAGE	• DIRECT ETHERNET CONNECT	• VMS COMPATIBLE
• TELEPHONE MANAGEMENT	• FILE, PRINT, COMM. SERVERS	• 16 BIT PC'S FIELD UPGRADEABLE (?)
• BITMAP GRAPHICS (GREYSCALE & COLOR)	• VLSI PDP-11 CPU (.5 MIPS)	
• "STEREO COMPONENT" APPROACH		
• INTERNATIONALIZED		
• WINCHESTERS		
• DUMB TERMINAL EMULATION		

1985


DEPT. VAX CLUSTER
J-11
20/20
ETHERNET
VAX
SERVERS
GATEWAYS
BROADBAND
OPTICAL
- FILE
- PRINT
- TERMINAL
- IBM
- X.25
- XEROX?
- IBM LAN?
- CUSTOM
o NEW DEPT. VAX'S (11/810, 11/830, 11/850)
o FULL COMPLEMENT OF SERVERS/ GATEWAYS
o OPTICALS FOR ARCHIVAL STORAGE?

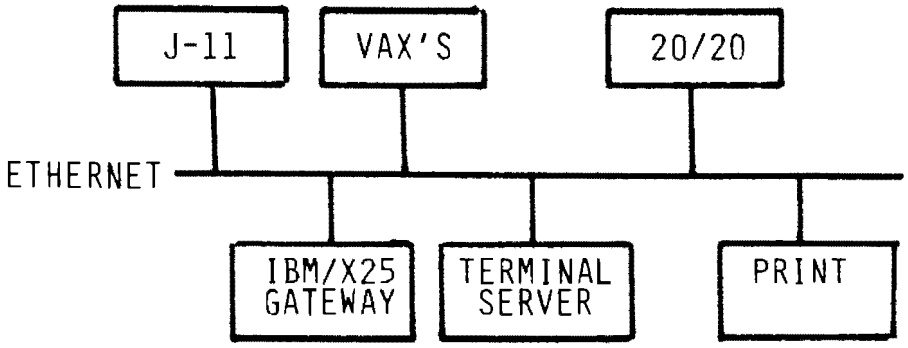
EVOLUTION OF DEPARTMENTAL COMPUTING

TODAY



- o HETEROGENEOUS NETS
- o FLEXIBLE NET ARCHITECTURE (DECNET)
- o INITIAL GATEWAYS
- o COMM. SPEED <1M BIT/SEC

1983-1984



- o HETEROGENOUS "VIRTUAL TERMINALS"
- o ETHERNET (10M BITS/SEC)
- o VLSI PDP-11'S
- o MORE GATEWAYS
- o MORE SERVERS

TYPICAL LARGE CLUSTER CAPACITY

	1983-1984	1984-1985
MIPS	8-->30*	30
BYTES X 10^9	80	160

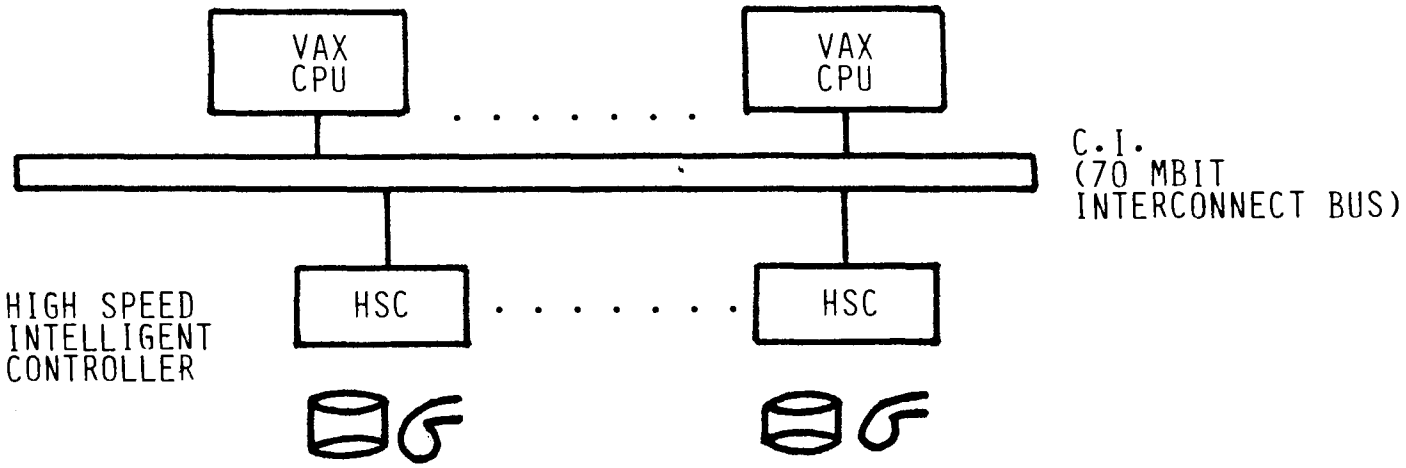
KEY NEW PRODUCTS IMPROVING CLUSTER CAPACITY

* - LARGE VAX (4 MIPS, LATE 1984)

- 900 MB 9" WINCHESTER DISKS (1985)

TYPICAL DEC CLUSTER

(1983-1984)



- EITHER LARGE VAX OR DECSYSTEM 20 CPU'S
- SHARED DATA ACCESS

LOCAL AREA NETWORK DEFINITION
(LAN)

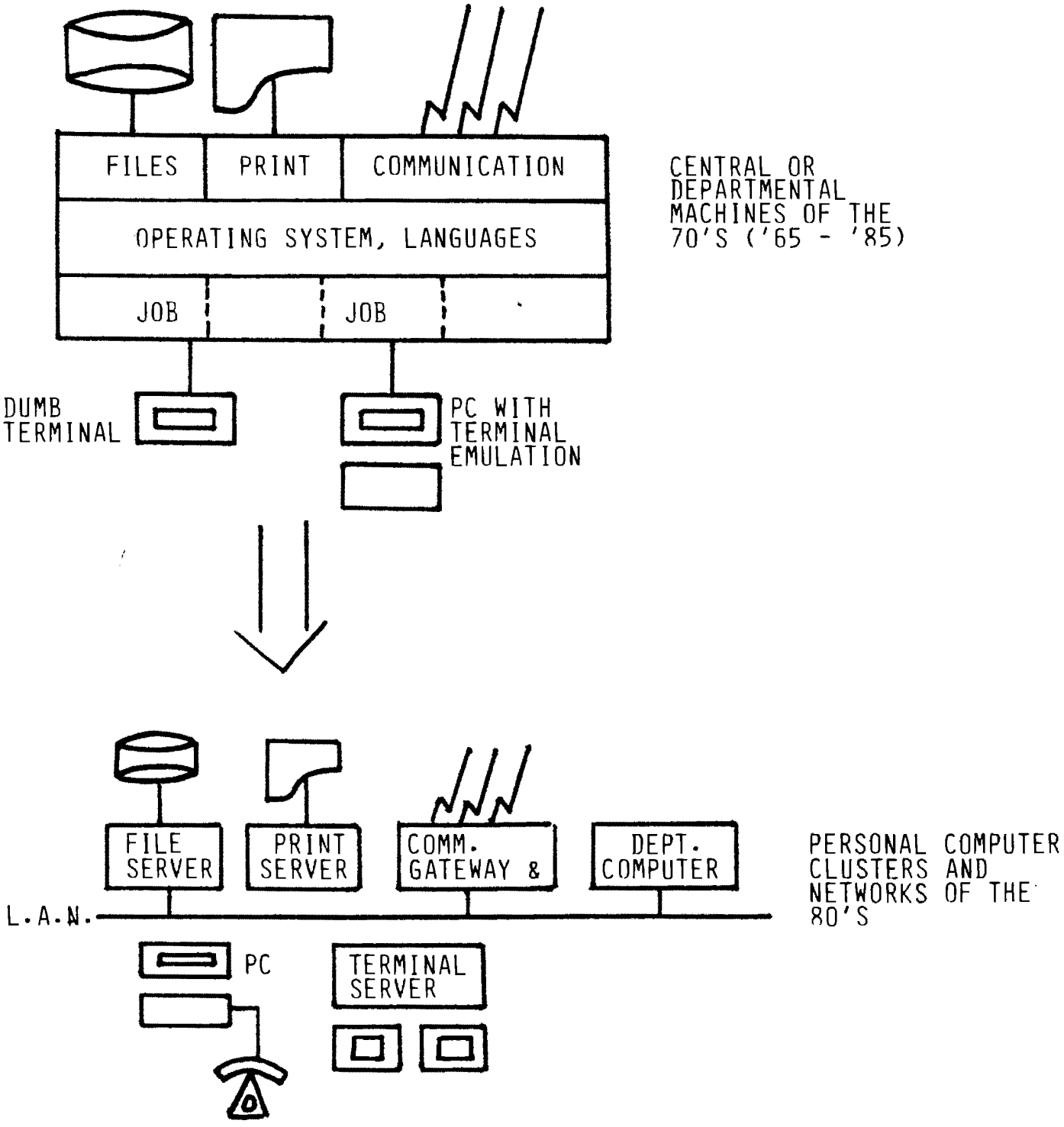
- AGGREGATION OF HETEROGENEOUS SYSTEMS
  (E.G., VAX/VMS-PC-TOPS 20-UNIX; GATEWAYS TO OTHERS)

- PURPOSE IS TO CONNECT A NETWORK OF AUTONOMOUS SYSTEMS
  (MESSAGE, FILE, PROCESS, TERMINAL INTERCOMMUNICATION)

- RELATIVELY HIGH SPEED INTERCONNECT (1-30 MBITS/SEC)
  HIGH CONNECTIVITY AMONG SYSTEMS (AND CLUSTERS)
  SYSTEMS LOCATED IN AN OFFICE AREA, BUILDING, OR CAMPUS

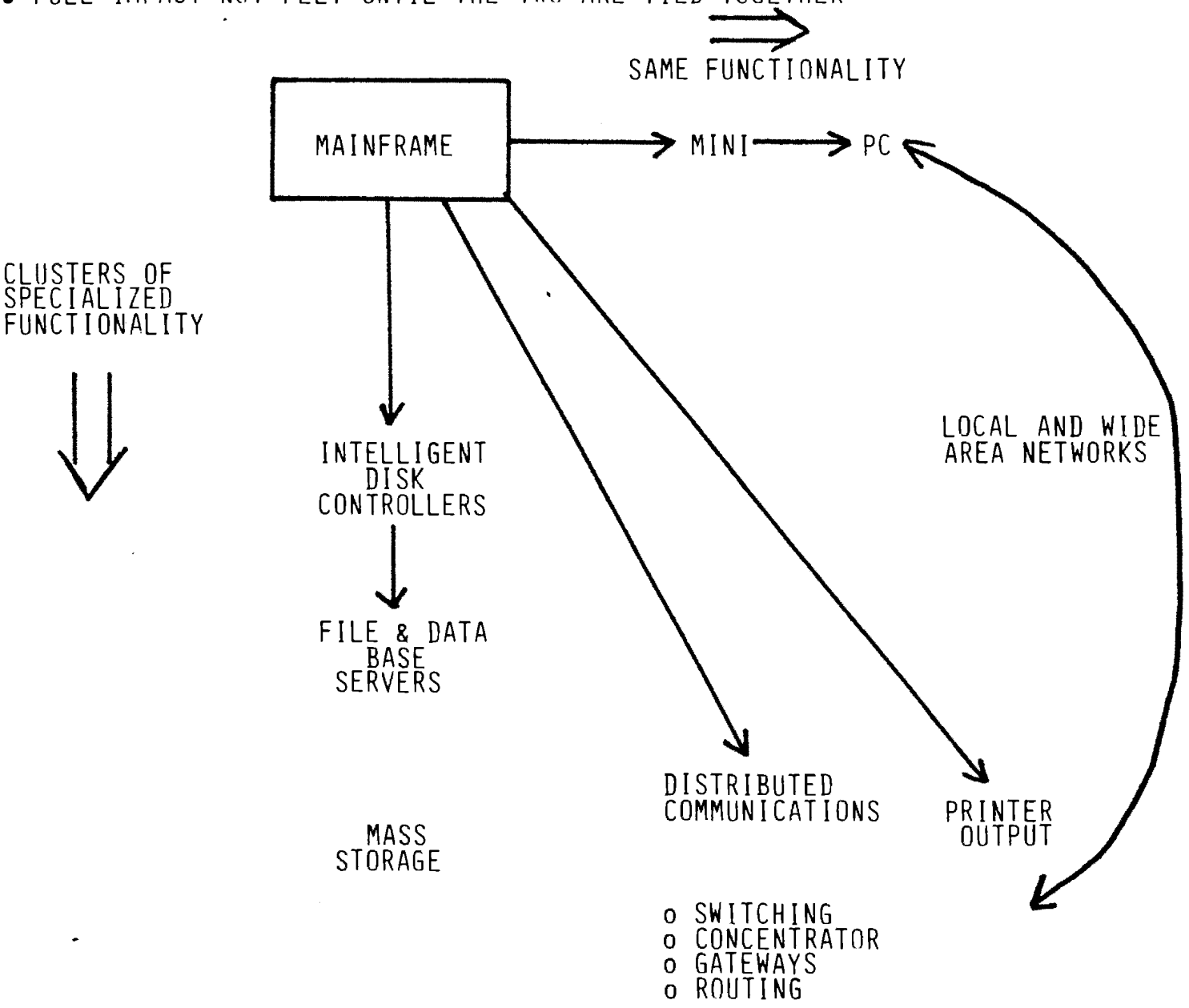
- BASED ON ISO 7 LAYER NETWORK PROTOCOLS (APPLICATION)

KEY EVOLUTIONARY TRENDS



KEY EVOLUTIONARY TRENDS

- THE TWO SEPARATE TRENDS ARE VISIBLE TODAY
- FULL IMPACT NOT FELT UNTIL THE TWO ARE TIED TOGETHER



- WHEN LINKED, THEY'RE THE BASIS FOR THE NEXT GENERATION OF COMPUTING ARCHITECTURE
- CLUSTERS ARE AN ALTERNATAIVE TO LARGER SYSTEMS

EVOLUTION OF MAJOR COMPUTING STYLES

CENTRAL	MAINFRAME	CENTRAL CLUSTERS
DEPARTMENTAL/ GROUP	GENERAL PURPOSE	LOCAL AREA NETS OF: - GENERAL PURPOSE MINI'S - DEPARTMENTAL SERVERS - DEPARTMENTAL CLUSTERS OF PC'S
	MINI	- SUPER MICRO (YESTERDAY'S $100K MINI FOR $10K)
PERSONAL	DUMB TERMINAL INTELLIGENT TERMINAL TO SHARED SYSTEM	PERSONAL COMPUTING CLUSTERS

CONTRAST BETWEEN VAX & CONVENTIONAL MAINFRAME

- NO CHANNELS!
- 1 OPERATING SYSTEM WITH ALL LAYERED PRODUCTS AVAILABLE
- LAYERED S/W TOOLS MORE FULLY INTEGRATED
  EXAMPLE: OFFICE AUTOMATION SYSTEM (ALL-IN-1)
- SUPERSET COMPATIBILITY WITH PDP-11 BASED DEPARTMENTAL SYSTEMS AND PC'S
- BUILT TO BE OPERATOR-LESS
- COVER A WIDER RANGE OF USE (COMPUTING STYLES) FROM PC TO MAINFRAME

The Transitions

Transitions Imply Change (And Pain) In:

- What We Engineer (I.E. Projects)
- How We Design
- How Computers are Sold, Produced, Distributed & Used

From the Generations Graph, We Can Observe:

- There is a wider range of useful systems, & these will be appealing to our customers, us & others; (For example, in 1985 we could be selling $1,000 computing terminals with the power of the original LINC, & $600K 10/20's)

From the Generations Graph, We Can Observe:

- The wide range of useful systems will force all suppliers to be more competitive & selective as new suppliers enter on a point product basis & as the 370 becomes a commodity
- IBM, Fujitsu, & others are likely to offer a 4341-2 class machine in our $40-100K Minicomputer Heartland

We Must Be Targeting the Following (for 1985)

- Cray 1 Power, $625K (or in 1990 for $250K)
- 3X Comet Power for $100K
- A sharable VAX (or big Micro) in $6.25K to $16K range
- A personal VAX (or big Micro) for under $6.25K
- A computing terminal with VT100 capability, & power of Apple II, or original LINC, for $1,000
- Computers in $400 to $1,000 range

We Have Not Provided Aggressive Enough Products Because:

- The Q & U Bus form factors have constrained system cost & size
- The 19" rack & stack, palletable form factor together with poorly packaged components, has been retained. Packaging in other, lower cost form factors enabling cardboard box shipment & customer merge is essential

We Have Not Provided Aggressive Enough Products Because:

- The terminal has not been used as a package
- Point products have been insufficiently high quality, software supported, or cost-effective. Even $200 calculators are modular with mass storage, printer, modem & display options

Transition to Distributed Computing Based on NI, Interconnecting:

- Departmental & Central Computers to Each Other
- Personal Computers to Form Clusters
- Functional Server Components to Reduce the Number of Network Possibilities that are a Product of:
  - Hardware Systems
  - The 12 Operating Systems We Support
  - And the Desirable Protocols Including X.25, IBM, DECnet & Other Vendors

By Using the Server Concept Each System Can be Connected to NI, with Specialized Servers As:

- Concentrators for Interconnecting Dumb Terminals & Personal Computers
- Gateways to Systems Using Other Protocols
- Repeaters & Interfaces to Other Networks
- Central Functional Servers for Files & Printing
- Real Time Front Ends

Transition to Personal Computers from Minis & Mainframes

Timeshared Computers are Affected in Several Ways:

- Direct, Stand Alone Use As an Alternative
- More Terminal Load Can be Put on a Given Computer
- Interconnected Clusters of Personal Computers are a Substitution

Transition from Rack & Stack 16-Bit Computers

The Alternatives:

- 16-Bit microprocessor cards & systems which have 24-32 bit memory address space & supplied by both semicomputer companies & their OEMs Transportable Systems such as UNIX are aimed at establishing hardware to be a commodity
- Board & box level systems that are oriented to modern special chip I/O as supplied by the semicomputer suppliers

Transition from Rack & Stack 16-Bit Computers

The Alternatives:

- Personal Computer & Clusters
- VAX & other 32-Bit Architectures
- Emerging commodity priced 370s in this price class
- Better Box-level form factors not possible with 19", FAT produced, Q - &, Unibus Systems; Systems must be shipped in cardboard boxes, integrated by the customer, & when broken, self-diagnosing with customer replaceability.

Transition from Terminals to Computing Terminals

The Major Transition for Terminals is Semantic, i.e. What is a Terminal?

Terminals Must Change in the Following Ways:

- **Larger Personal Computers are an alternative to our conventional, dumb terminals**
- **All terminals introduced beginning in FY83 must be customer programmable with at least firmware ROMS and RAM buffers**

Transition from Terminals to Computing Terminals

Terminals Must Change in the Following Ways:

- The interconnection, whether it be U.S. or European Modem, NI, or IBM Emulator, must be built into the terminal
- Decreasing memory cost based on 64K chip will offer fully programmable screens, which in turn will automatically provide graphics
- Higher resolution, full-page & color displays

Transition to Software for End Use vs. Programmer Tools

We Can Identify These Needs:

- Direct use in the office, including providing the ability of OEM's, office managers, organization & the individuals to tailor their systems
- Better human engineering at screen & in documentation; Documents & help should be built-in
- All products must be modifiable for use with natural languages
- Applications building tools for particular professional & commercial environments

Transition in Hardware Design Skills

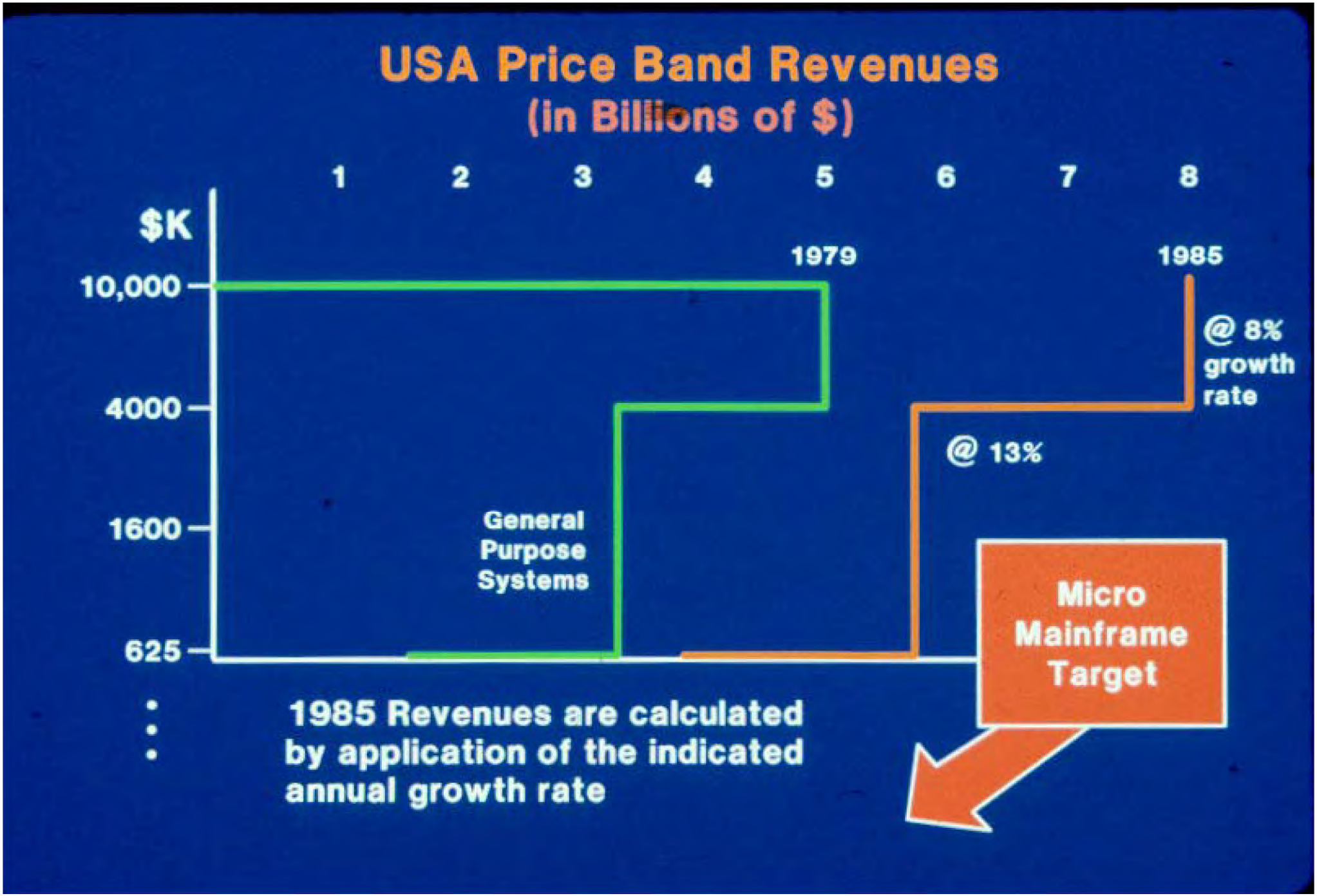
The Immediate Transitions for System Designers Include:

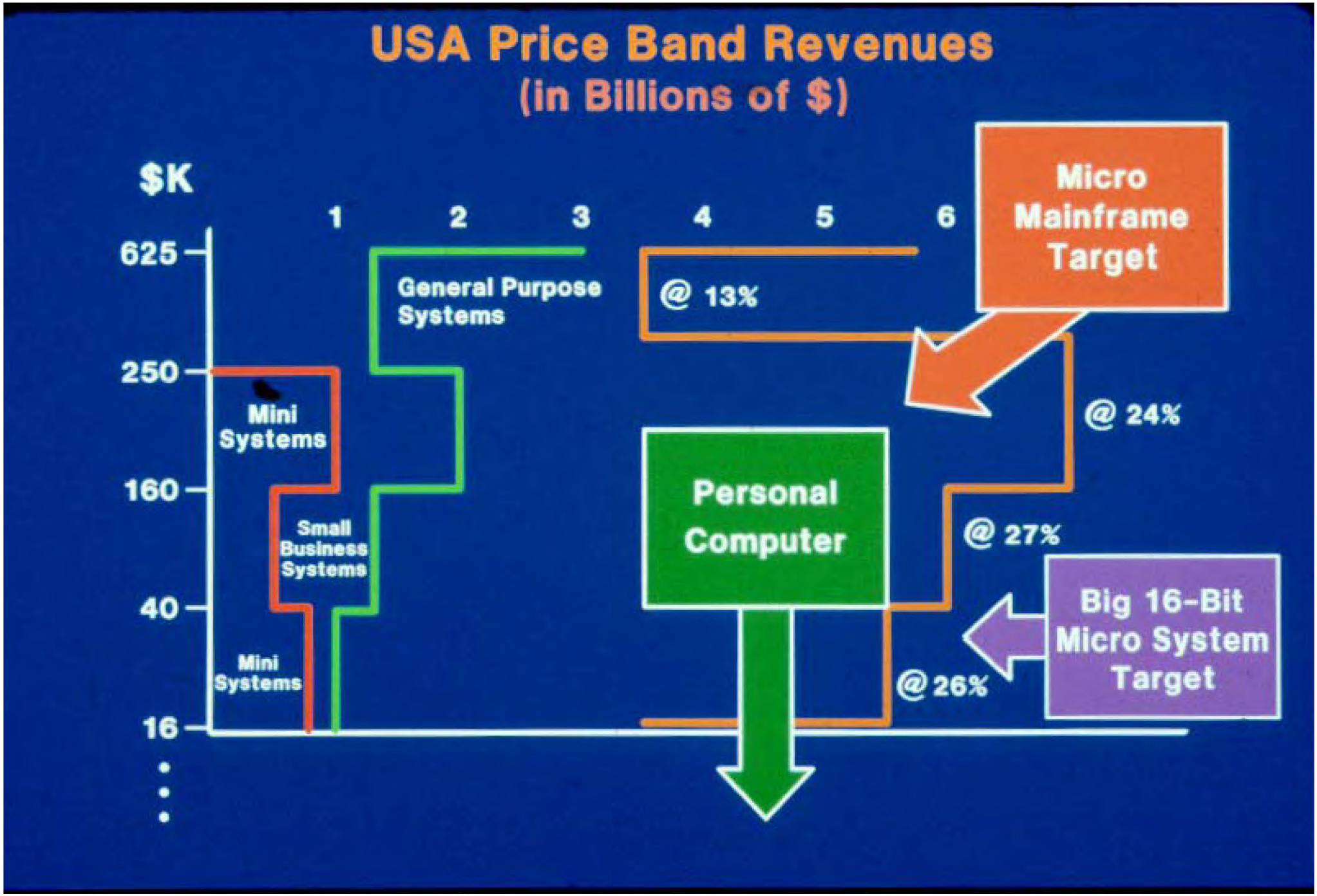
- Standardization & use of general purpose controllers & processors for conventional controllers. We are not using enough standard VLSI! This implies options are programmed
- Use of gate arrays & other LSI to lower cost of all jelly bean & non-processor logic

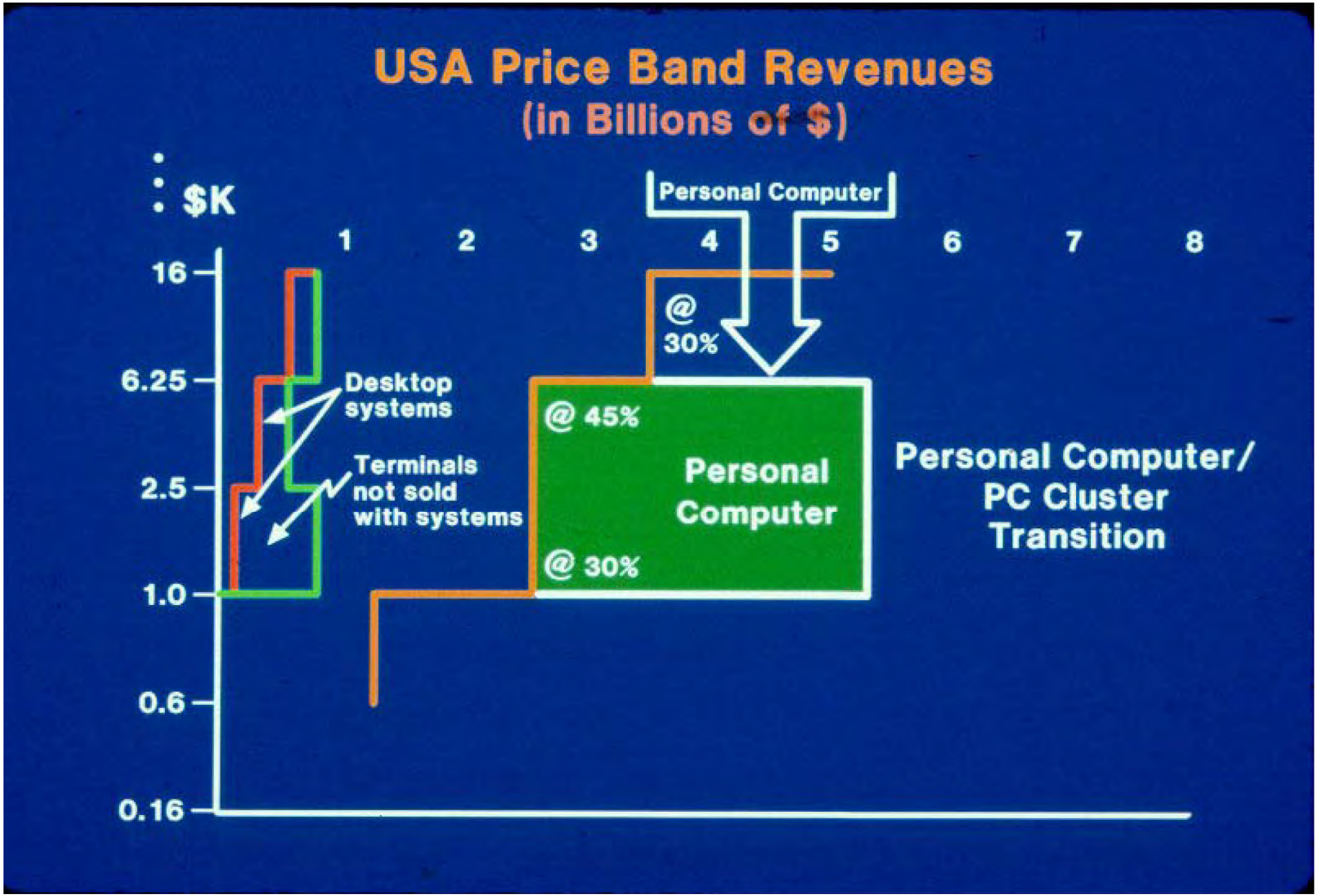
Transition in Hardware Design Skills

The Immediate Transitions for System Designers Include:

- VLSI design, where processors & controllers are placed on a single chip
- Identification of either general purpose or special purpose computers based on VLSI for building the non-processor portion of systems to drastically reduce system cost
- Generally dealing with much more complexity


USA Price Band Revenues
(in Billions of $)
1
2
3
4
5
6
7
8
$K
10,000
4000
1600
625
1979
1985
@ 8% growth rate
@ 13%
General Purpose Systems
Micro Mainframe Target
1985 Revenues are calculated by application of the indicated annual growth rate


USA Price Band Revenues
(in Billions of $)
$K
1
2
3
4
5
6
625
250
160
40
16
General Purpose Systems
@ 13%
Micro Mainframe Target
Mini Systems
Small Business Systems
Mini Systems
Personal Computer
@ 24%
@ 27%
@ 26%
Big 16-Bit Micro System Target


USA Price Band Revenues
(in Billions of $)
$K
1
2
3
4
5
6
7
8
16
6.25
2.5
1.0
0.6
0.16
Personal Computer
@ 30%
Desktop systems
Terminals not sold with systems
@ 45%
Personal Computer
@ 30%
Personal Computer/ PC Cluster Transition

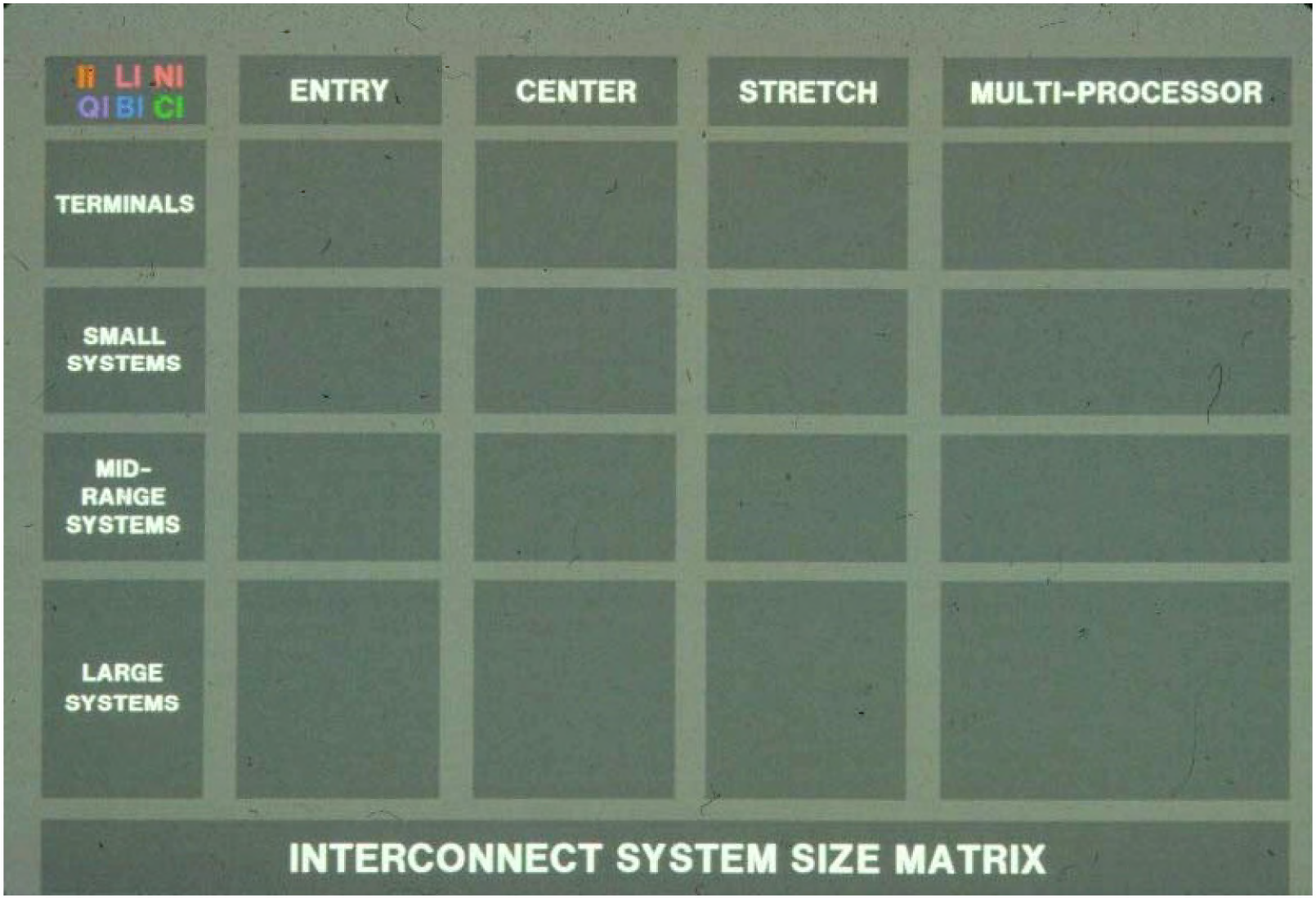
I/C ATTACHMENT NAMING CONVENTION

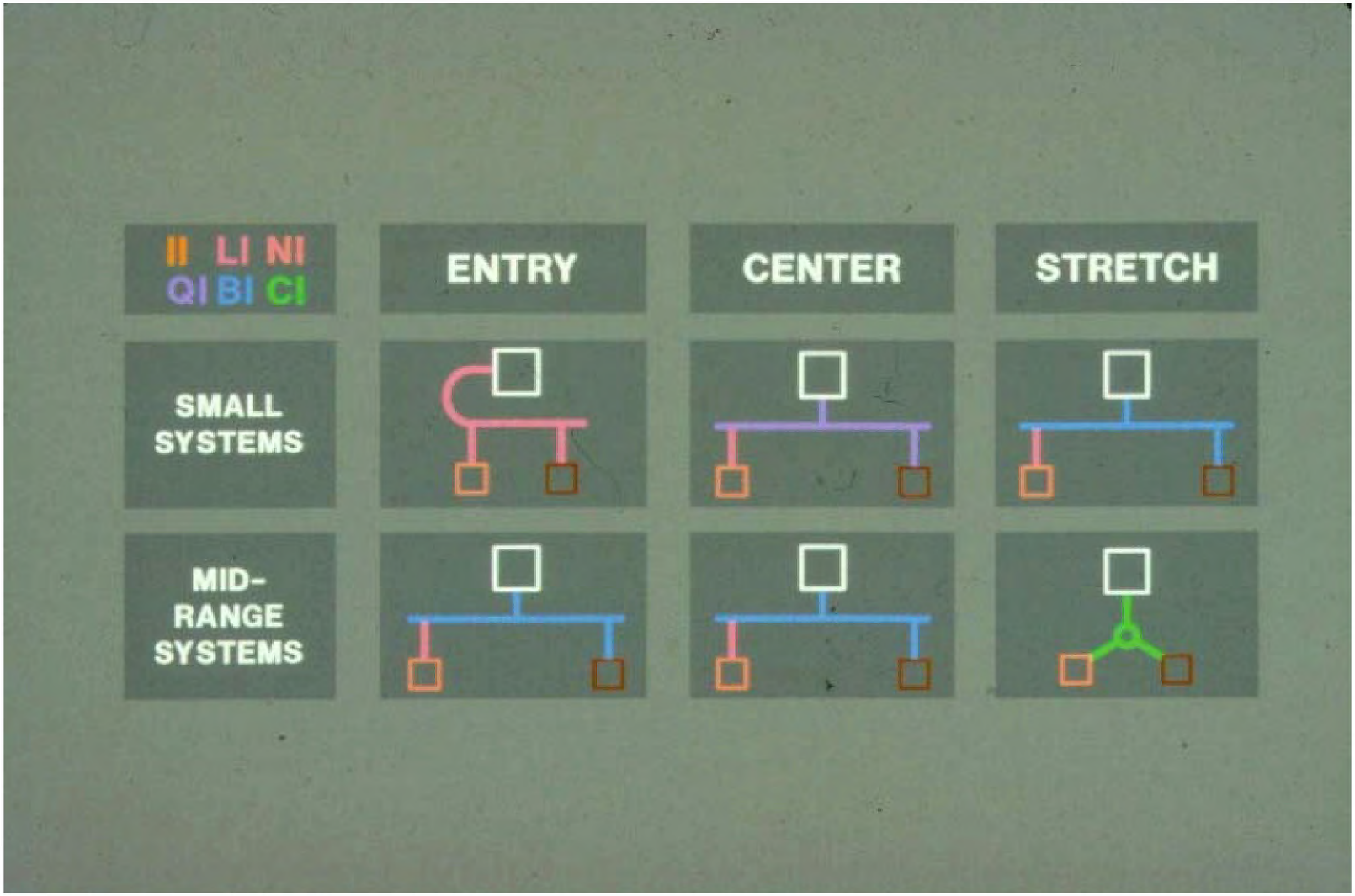
EXAMPLE:

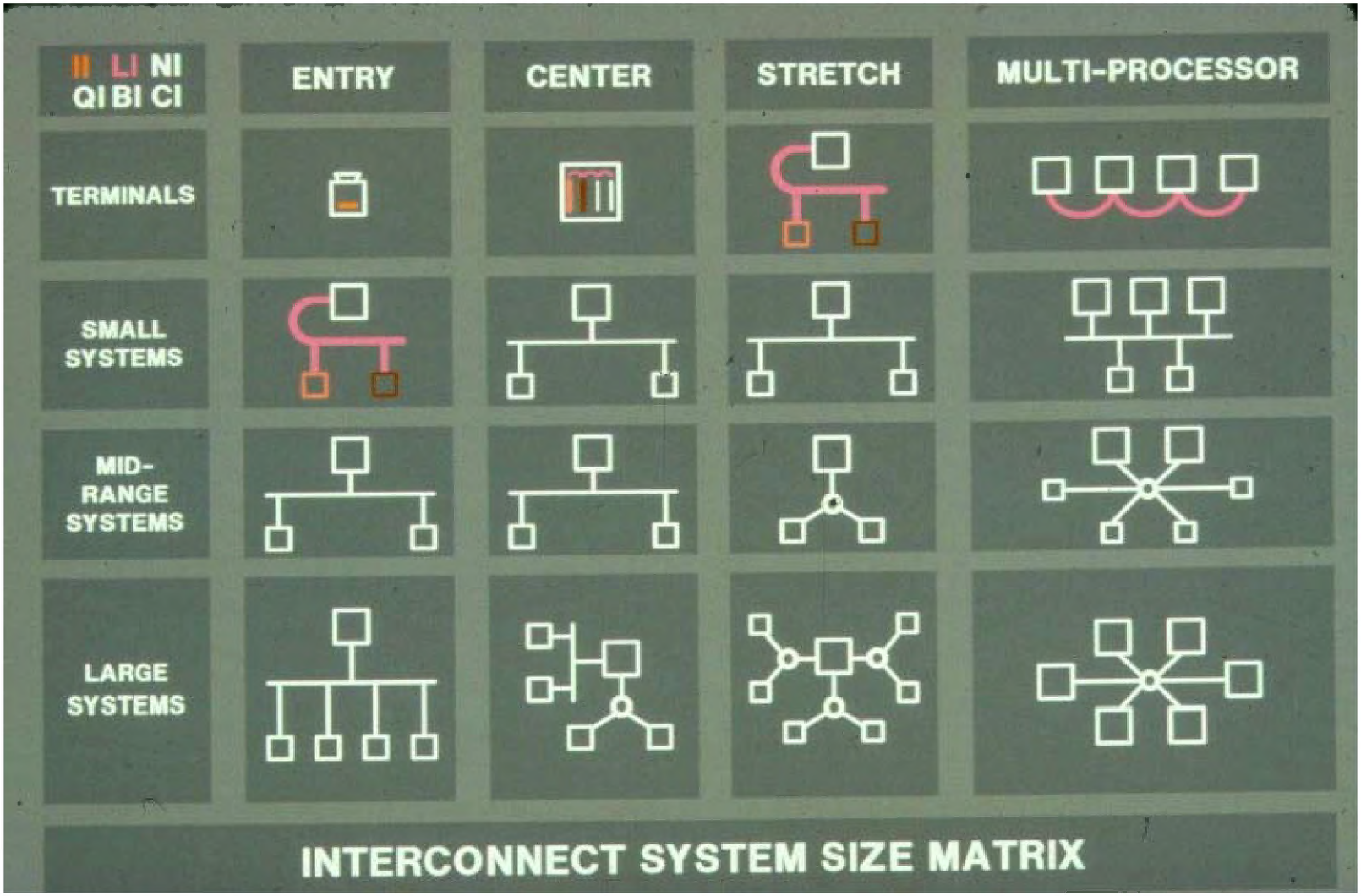
BI TO NI = BNI

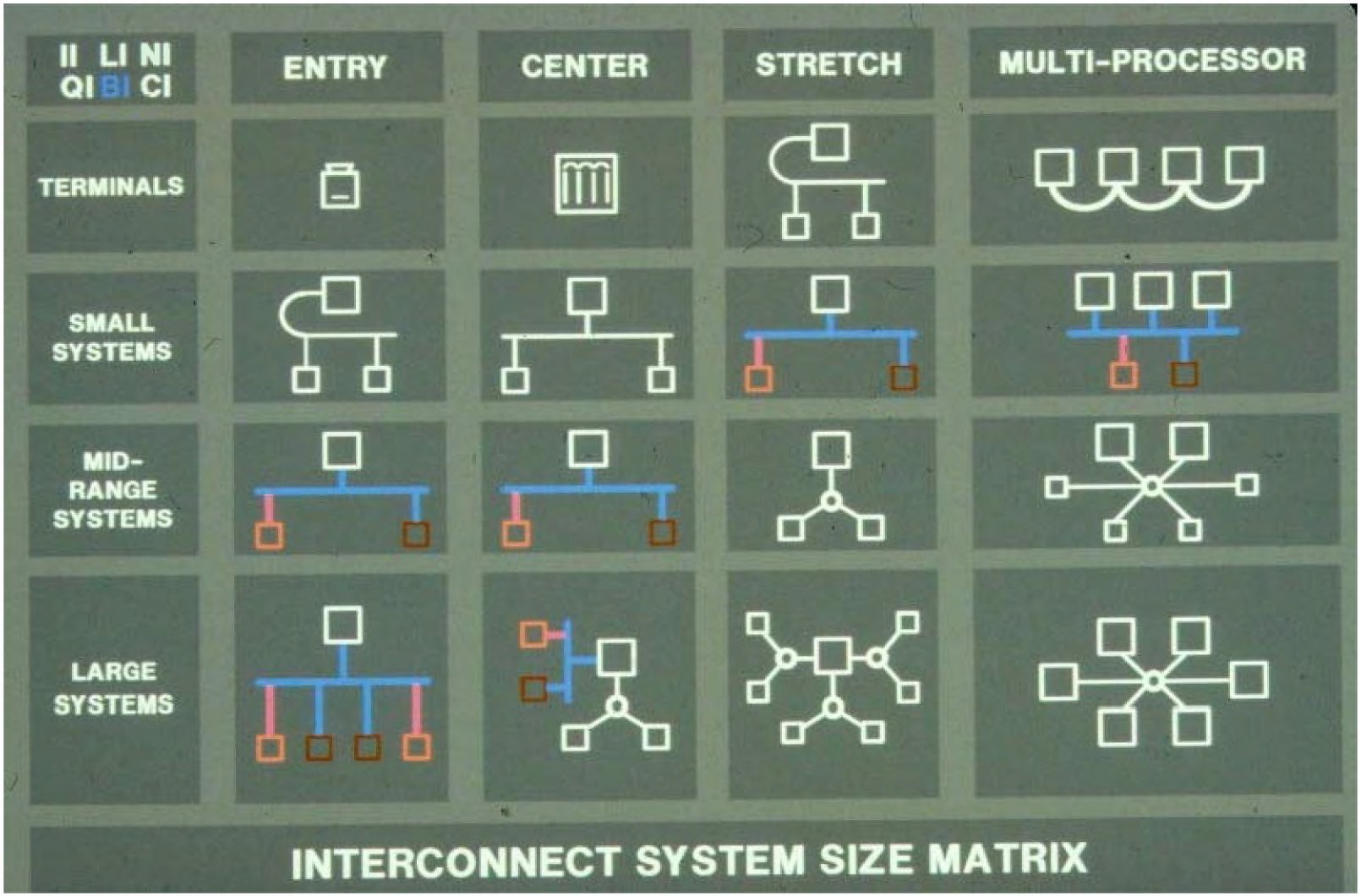
INTERCONNECT SPECTRUM

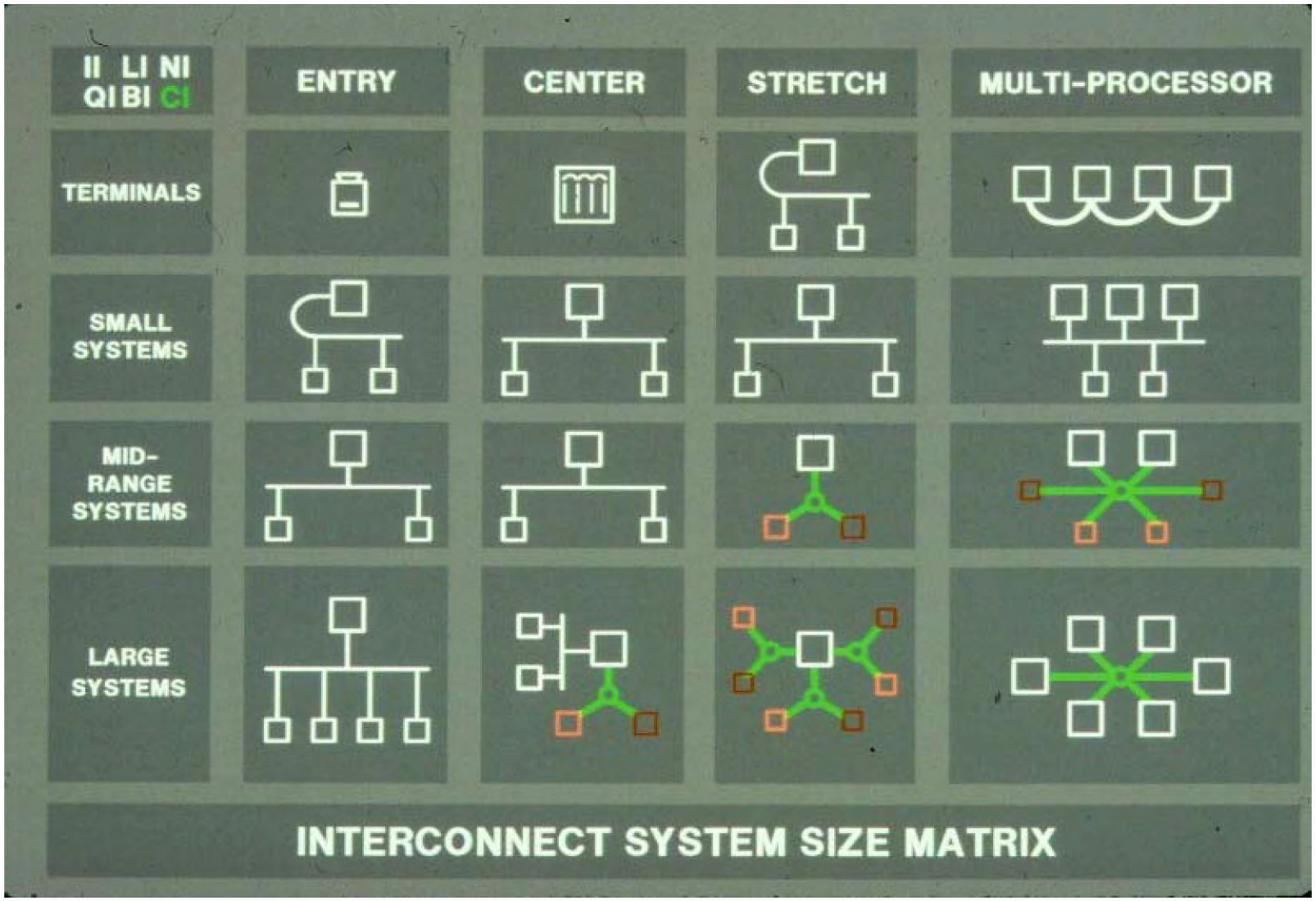
BI	BACKPLANE
CI	COMPUTER
DI	DEVICE OR COMMUNICATION
II	INTEGRATED CIRCUIT
LI	LOW END
NI	NETWORK
MI	MEMORY
QI	QZZ BUS
SI	STORAGE

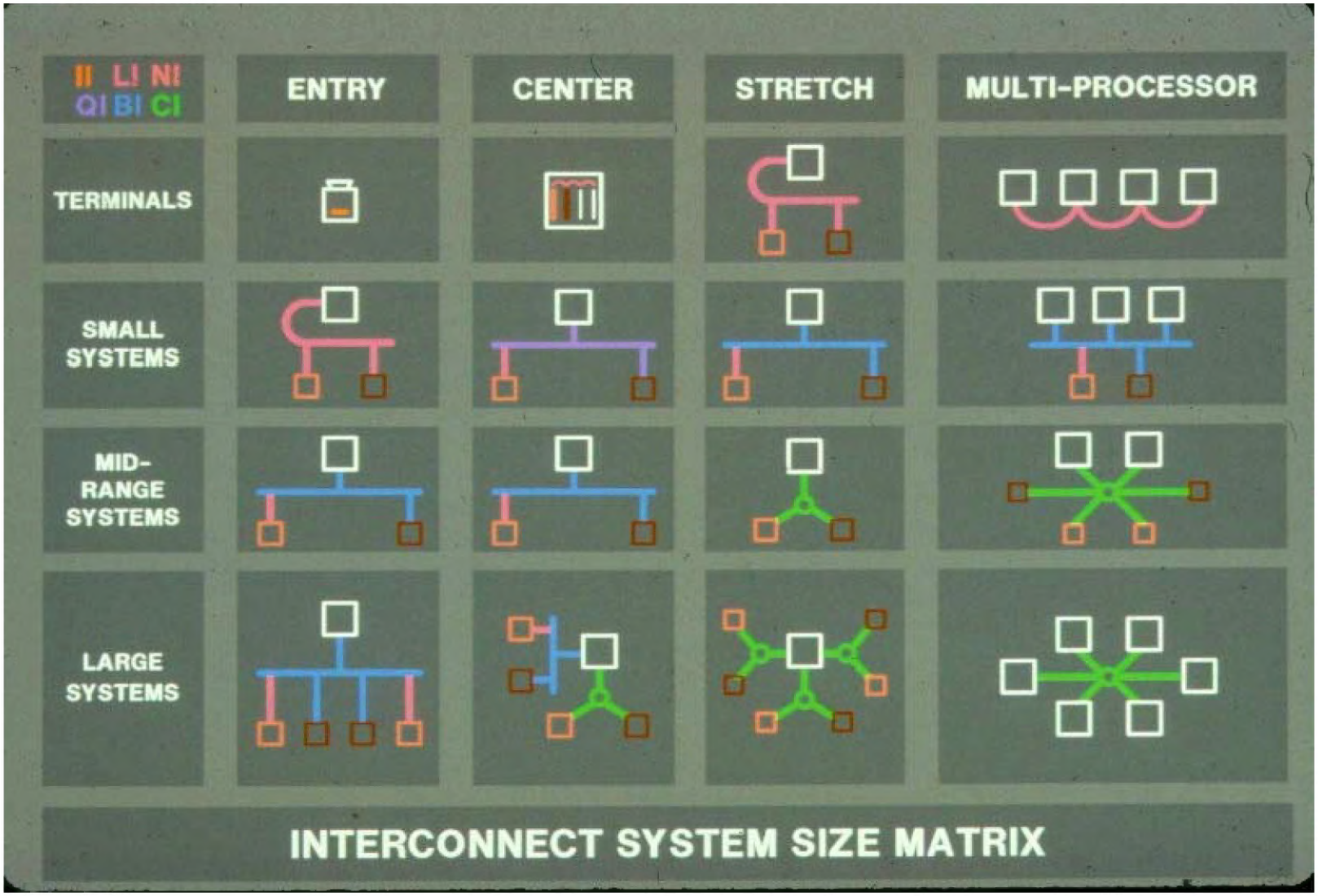

II LI NI
QI BI CI
ENTRY
CENTER
STRETCH
MULTI-PROCESSOR
TERMINALS
SMALL SYSTEMS
MID-RANGE SYSTEMS
LARGE SYSTEMS
INTERCONNECT SYSTEM SIZE MATRIX

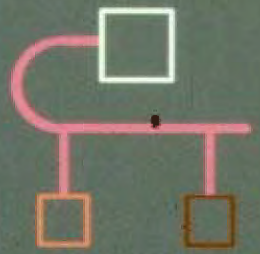
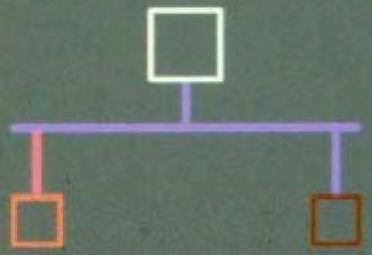

II LI NI
QI BI CI
ENTRY
CENTER
STRETCH
SMALL SYSTEMS
MID-RANGE SYSTEMS

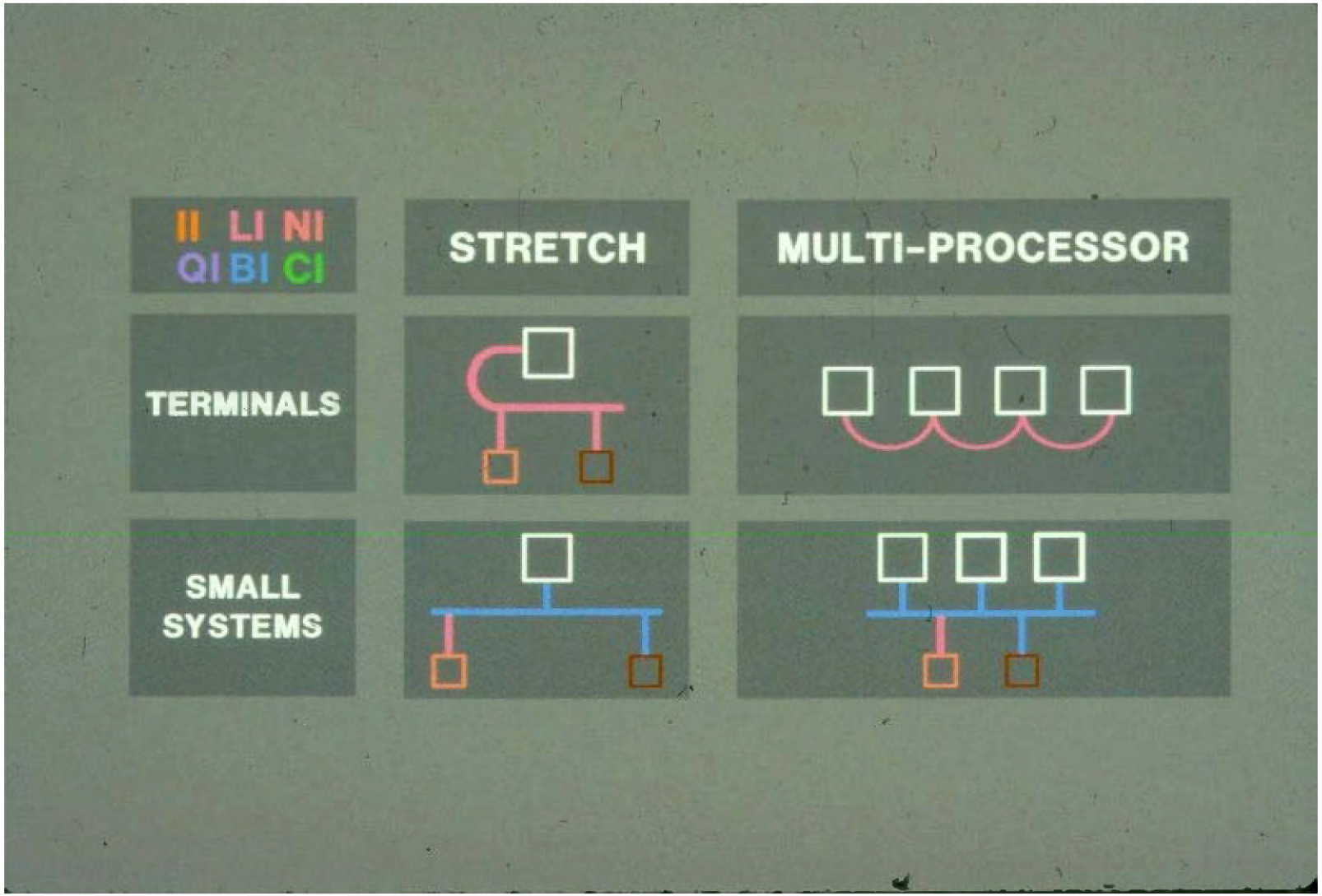

II LI NI
QI BI CI
ENTRY
CENTER
STRETCH
MULTI-PROCESSOR
TERMINALS
SMALL SYSTEMS
MID-RANGE SYSTEMS
LARGE SYSTEMS
INTERCONNECT SYSTEM SIZE MATRIX

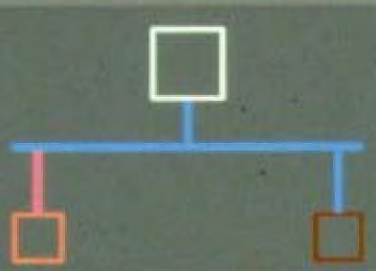
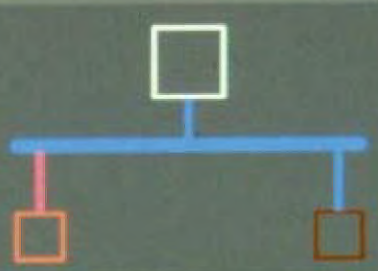
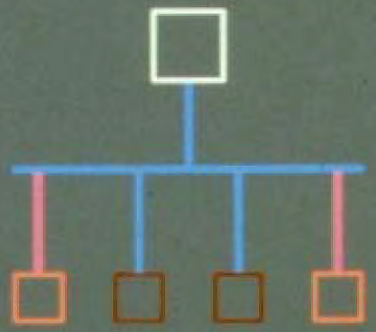
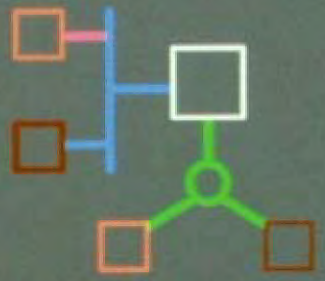

II LI NI
QI BI CI
ENTRY
CENTER
STRETCH
MULTI-PROCESSOR
TERMINALS
SMALL SYSTEMS
MID-RANGE SYSTEMS
LARGE SYSTEMS
INTERCONNECT SYSTEM SIZE MATRIX

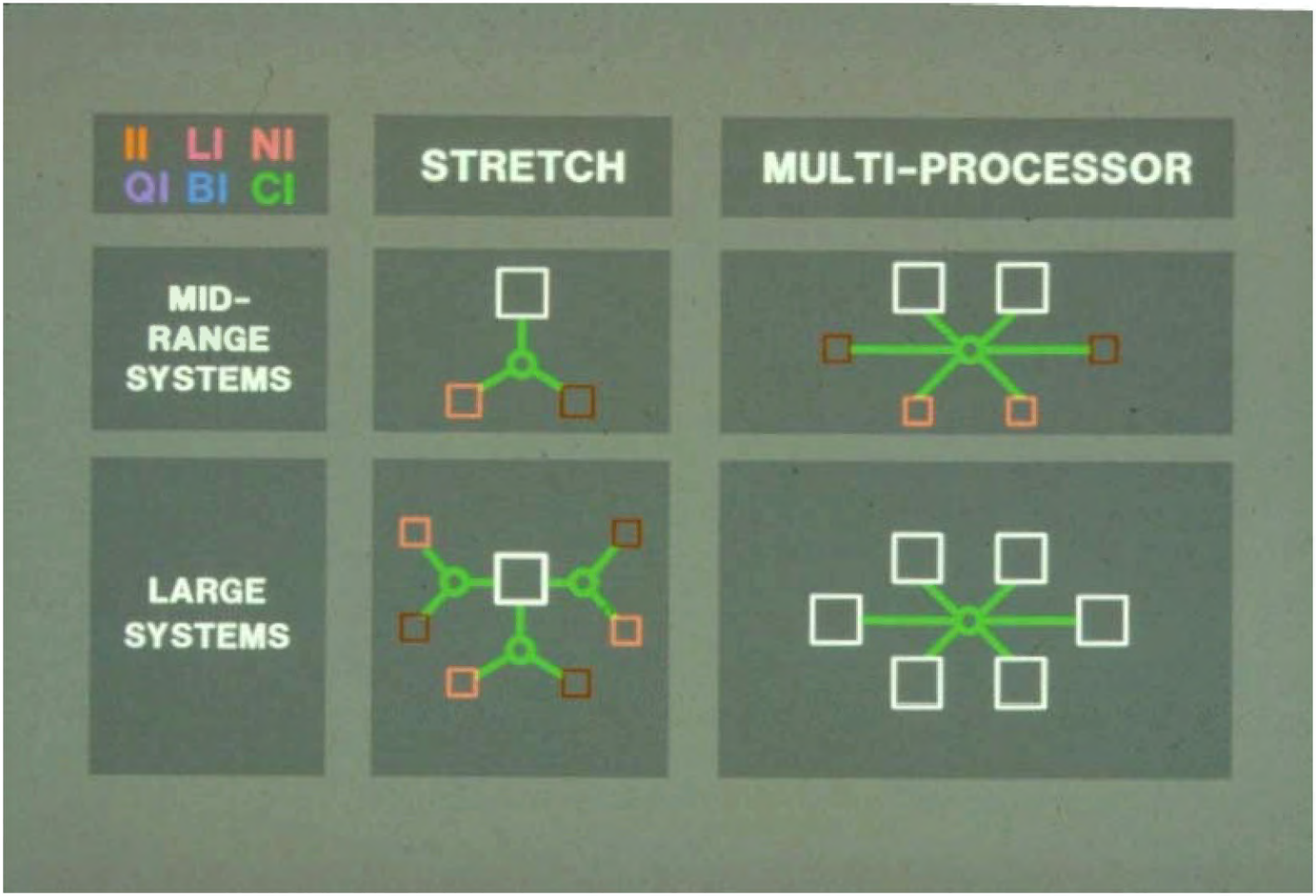

II LI NI
QI BI CI
ENTRY
CENTER
STRETCH
MULTI-PROCESSOR
TERMINALS
SMALL SYSTEMS
MID-RANGE SYSTEMS
LARGE SYSTEMS
INTERCONNECT SYSTEM SIZE MATRIX

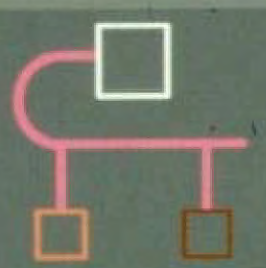
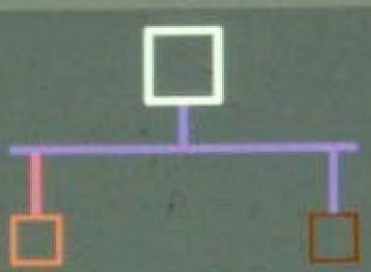
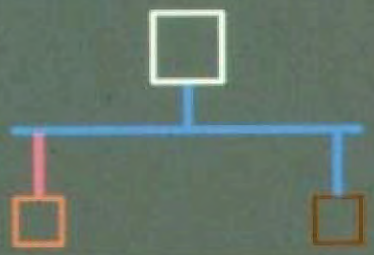
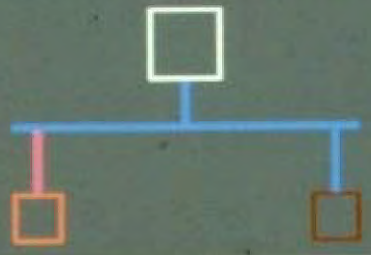

II LI NI
QI BI CI
ENTRY
CENTER
STRETCH
MULTI-PROCESSOR
TERMINALS
SMALL SYSTEMS
MID-RANGE SYSTEMS
LARGE SYSTEMS
INTERCONNECT SYSTEM SIZE MATRIX

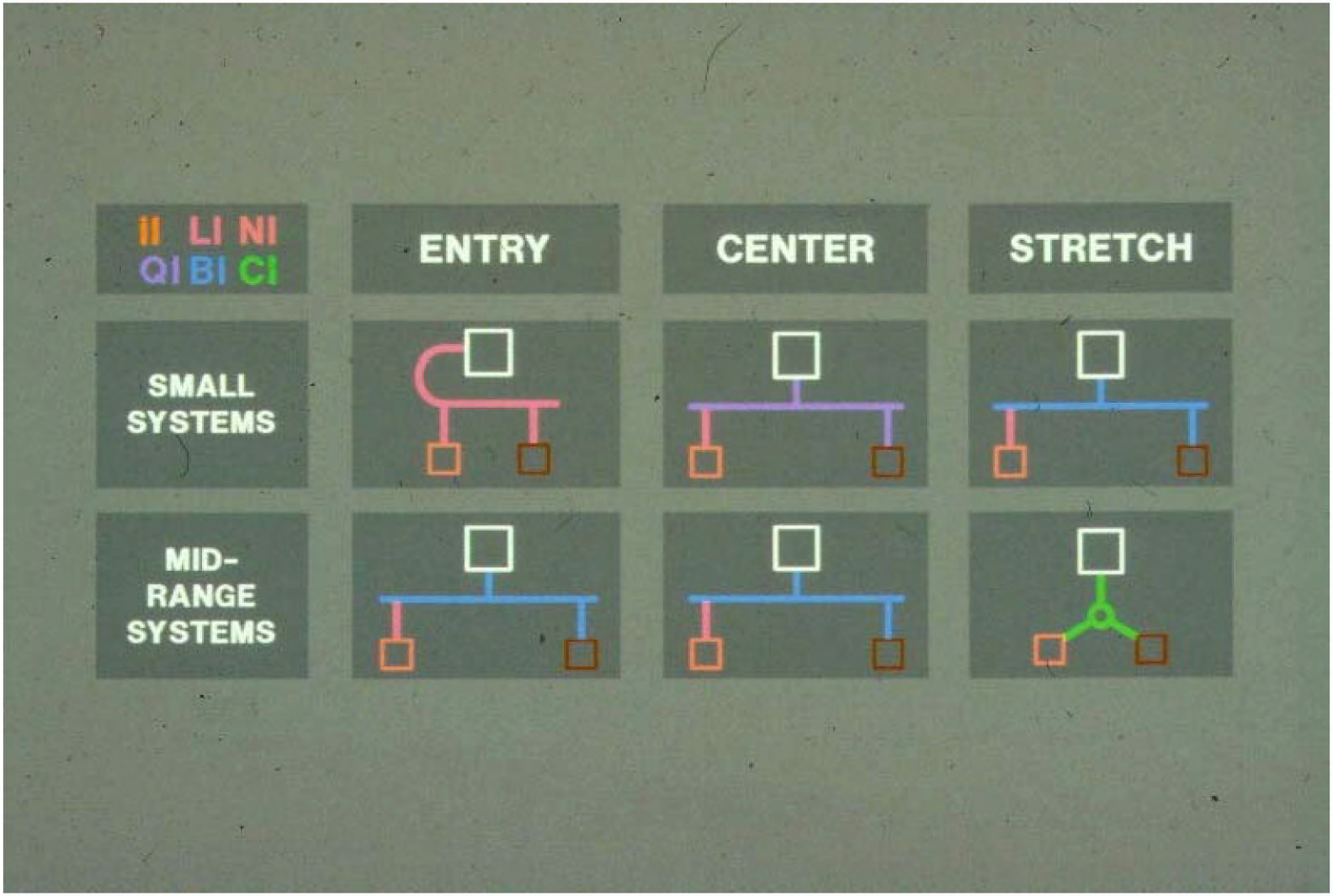
II LI NI QI BI CI	ENTRY	CENTER
TERMINALS		
SMALL SYSTEMS		


II LI NI
QI BI CI
STRETCH
MULTI-PROCESSOR
TERMINALS
SMALL SYSTEMS

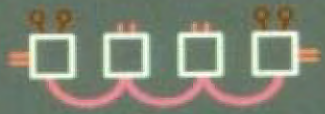
II LI NI QI BI CI	ENTRY	CENTER
MID-RANGE SYSTEMS		
LARGE SYSTEMS		


II LI NI
QI BI CI
STRETCH
MULTI-PROCESSOR
MID-
RANGE
SYSTEMS
LARGE
SYSTEMS

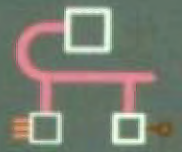
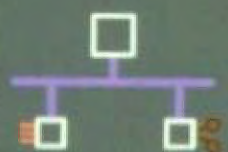
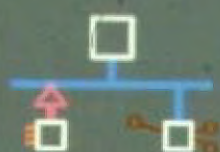
II LI NI QI BI CI	ENTRY	CENTER
SMALL SYSTEMS		
MID-RANGE SYSTEMS		


II LI NI
QI BI CI
ENTRY
CENTER
STRETCH
SMALL SYSTEMS
MID-RANGE SYSTEMS

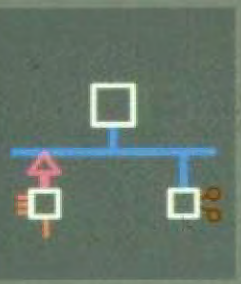
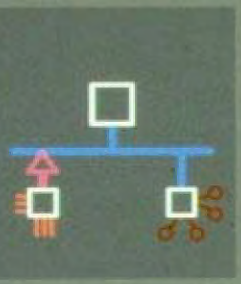
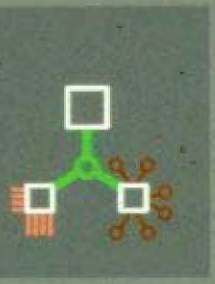
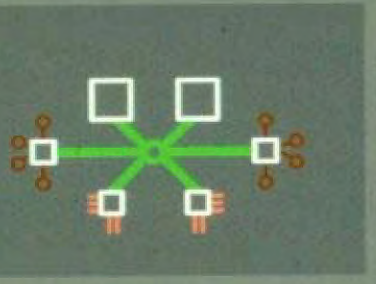
TERMINALS/BOUNDED SYSTEMS

ENTRY	CENTER	STRETCH	MULTI-PROCESSOR
			
SBC: T11	BOX: SB11	BOXES: MINC	MULTI-SBC

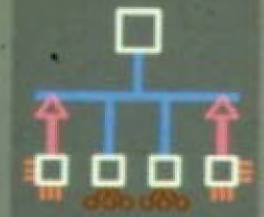
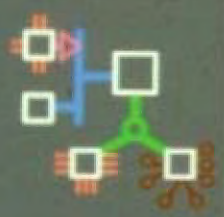
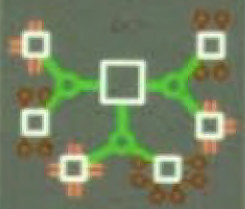
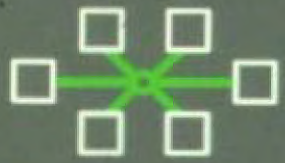
SMALL SYSTEMS

ENTRY	CENTER	STRETCH	MULTI-PROCESSOR
			
JAWS 11 -LI-	JAWS 11 -QI-	SCORPIO -BI-	MULTI-SCORPIO -BI-

MID-RANGE SYSTEMS

ENTRY	CENTER	STRETCH	MULTI-PROCESSOR
			
NEBULA -BI-	COMET -BI-	COMET -CI-	HI AVAILABILITY- HYDRA -CI-

LARGE SYSTEMS

ENTRY	CENTER	STRETCH	MULTI-PROCESSOR
			
VENUS -BI-	VENUS -BI& CI-	2080 -CI-	HETEROGENEOUS 32 & 36 -CI-

LIMITS TO COMPUTER GROWTH

- Technology and/or Process to Build Devices
- Designers and Computer Aided Design
- Ideas for Things (devices, computers, etc.)
- Lack of Standards ⟷ Too Many Standards (especially communications)
- Communications Links
- Algorithms for Effective Use
- Education of Interdisciplinary Engineers and Scientists to apply
- Market Size, Useful Applications and User's Ability to Assimilate
- People to Carry Information among Systems

THEME

- Computers ONLY Supplement (and Supplant) Other Information Processing* Systems

*INCLUDING Transmission, Transduction, Storage, Switching and Processing (Control)

THE POSSIBILITIES
ARE NEARLY LIMITLESS
BUT
SYSTEMS CHANGE MORE SLOWLY
THAN WE THINK (PREDICT)

COST* FOR VARIOUS MAIL SYSTEMS

	Transmission	Labor
Post	.16	4.06 ~
Telex	1.75	4.69 ~ 5.31
Fax	1.60	4.44 ~ 4.81
Phone (3 min)	.75	3.82 ~ 4.50
Computer	.27 ~ .98	2.25 ~ 3.76

*SRI Study, 1978

SINGLE SITE PARALLELISM (MULTIPLE COMPUTERS OR PROCESSORS)

- Independent Computers
- Shared Peripherals
- Communicating Processes
- Common Data Base
- Multiple Tasks in a Multi-Processor or Multi-Computer
  - Timesharing (n jobs)
  - Real Time (n processes)
  - Front End/Back End (functional)
- Single Task Parallelism
  - General Concurrency
  - Pipelining of Processes
  - Vectors and Arrays
  - Sets

BPO'S VIEWDATA

- Ran '73, Announced '75, Demo'd '76, Service by '80
- 1200/75 bps Link to Dumb Terminal using Modified Television Sets (40 x 24 characters) and Simple Keyboard

Charges: Information Stored, Accessor (at Line Charges and Per Month)

Size: approx. 100,000 Pages

WAYS TO DISTRIBUTE PROCESSING (AND MEMORY, TRANSDUCTION, ETC.)

Small Organizations (e.g. Business, Home)

- Independent (Decoupled) Computers
- Independent Computers with Information Transfers Via
  - Mail/Manual
  - Common Carriers
  - Common Carriers and Information Industry

WAYS TO DISTRIBUTE PROCESSING (AND MEMORY, TRANSDUCTION, ETC.)

Large Organizations

- Large, Shared Multi-Terminal System
- Organizationally: Central, Group, Individual
- By a Function for many Organizations (e.g. Order Processing)
- For Computer's Convenience: File Service, Printing, Switching

DISTRIBUTED SITE PARALLELISM

- Independent
- Network, with Explicit Transfer of Information among Nodes
- Single (but Distributed) Data Base
- Dynamic Assignment of Processing and Information Storage

PAPER COSTS (LAST 10 YEARS)

Mail - Increasing at 10%/Year
- Costs~$30 MBytes to Transmit, (1979)

Books - Increasing at 7%/Year

Periodicals - Increasing at 11%/Year
- Costs $1~20/MByte (1979)

Shelves - Increasing 7%/Year (with Inflation)

Cataloging - $4/Item (1979)

Human Information Processing is Improving a Few $/Year, While Costs are Increasing

COMMUNICATIONS COSTS

- Vague, although Forecasts Indicate Costs Halving by 1985.

  (The Numer of Lines is Not Increasing as Rapidly as Total Operating Company Revenues. Therefore, the Cost/Line is Increasing!)

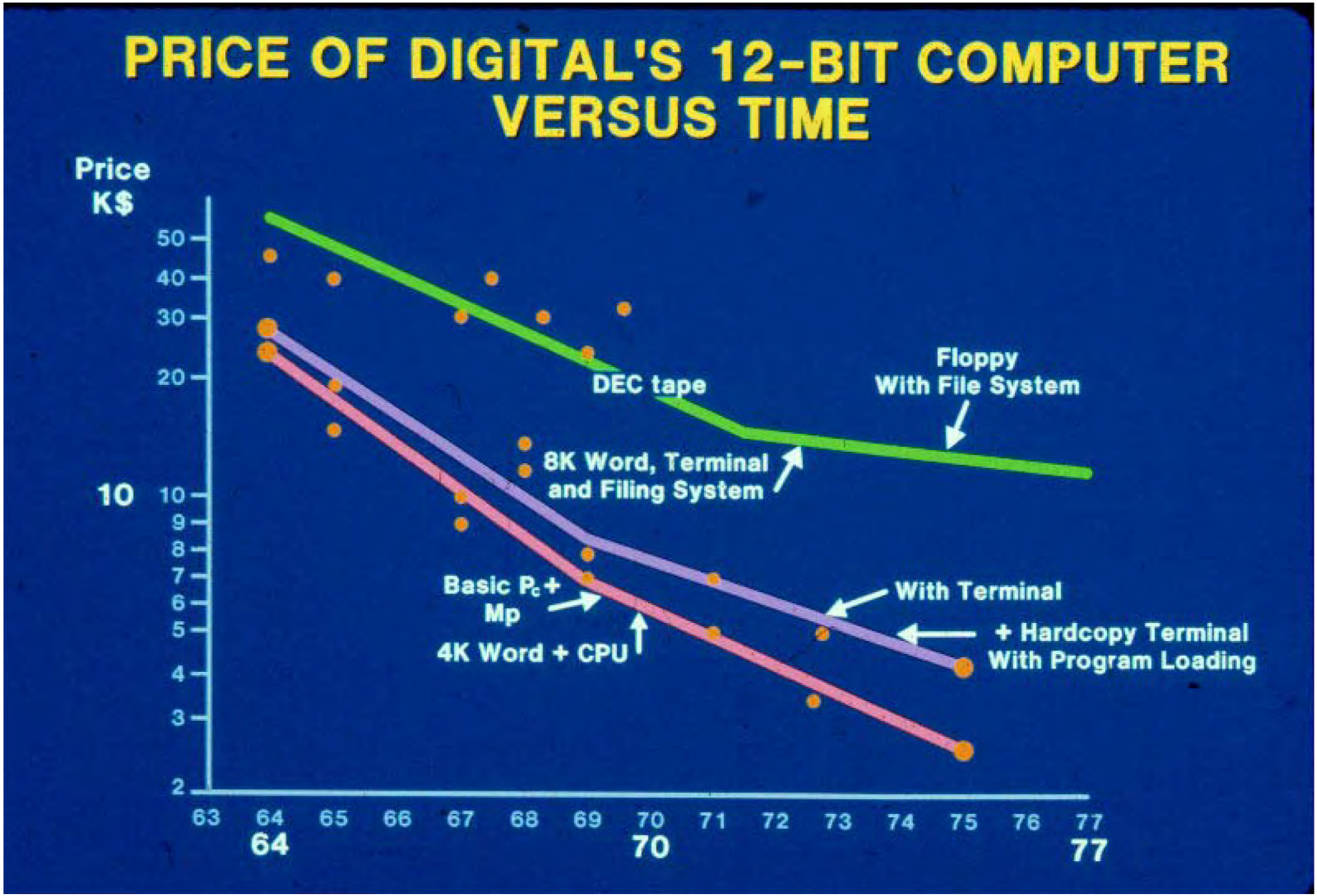
MODEM COSTS

1973 - 9.6 KB Modem Cost $9.6K
1979 - 9.6 KB Modem Cost $4.5K
} 12%/Year Reduction

Year	Data-Rate (Kbit)	Cost/Mbit
1960	2.4	$1.00
1963	40.3	.42
1964	50	.33
1976	56 (DDS)	.11

13 %/Year Reduction

PRICE OF DIGITAL'S 12-BIT COMPUTER VERSUS TIME



TECHNOLOGY PROGRESS

- niconductors
  - Density 2^{T-1962}
  - = 60 ∽ 80%/yr (conservative)
- e Price Improve 30%/Year
- ks (62 - 80) - Density ∽ 41%/Year
- e (52 - 73) - 23%/Year Density
  29%/Year Data-Rate
- ver (Cost/Watt), Packaging ∽ 0
- icomputer - 20% Price Decline Per Year
- minals - 10 ∽ 20% Decrease in Price Per Year

BASIC MODEL (1973)
BITS/DIE - 2^{T-1962}

Correction Factors

Bipolar	R/W	-2 Year
Bipolar	ROM	-1 Year
MOS	R/W	-
MOS	ROM	+1
Production	-1 ~ -2 Year	

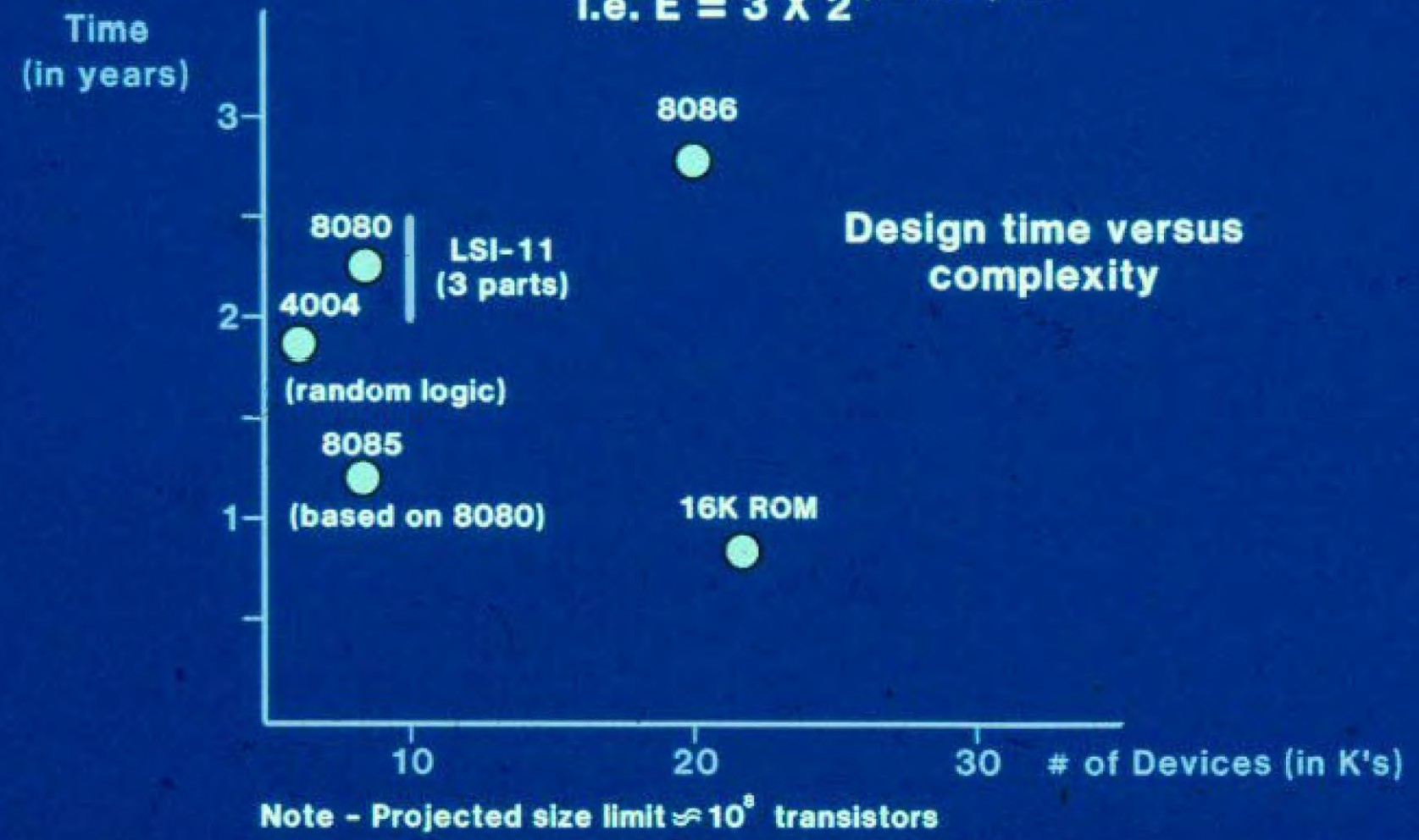
Results

Bipolar	R/W	16	69-70
		64	71-72
		1024	75-76
MOS	R/W	16K	77-78
		65K	79-80
		256K	81-82
Bipolar	RO	256	71-72
		1024	74-75
		2048	75-76

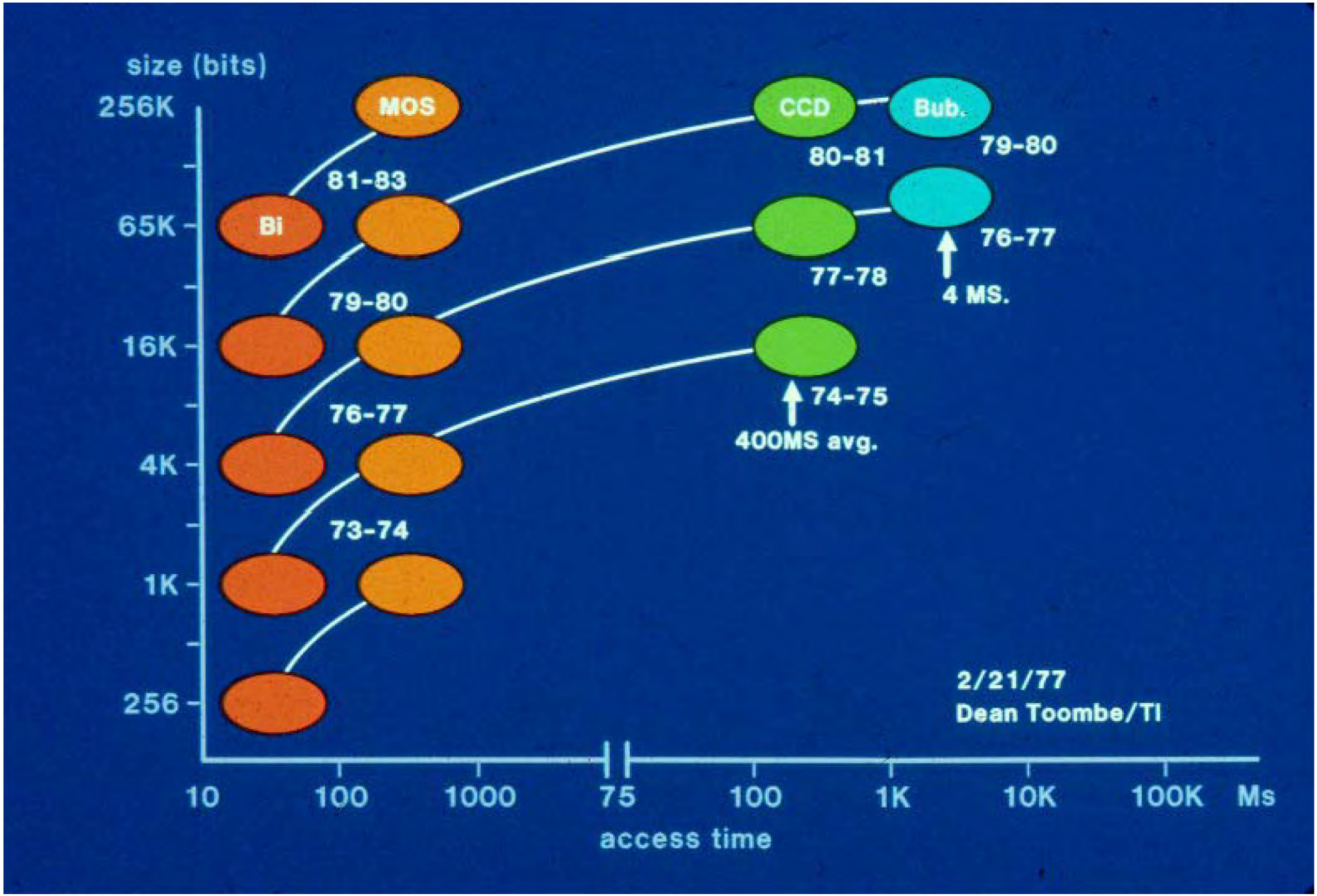
G. MOORE'S OBSERVATION
(1979 ISSCC)

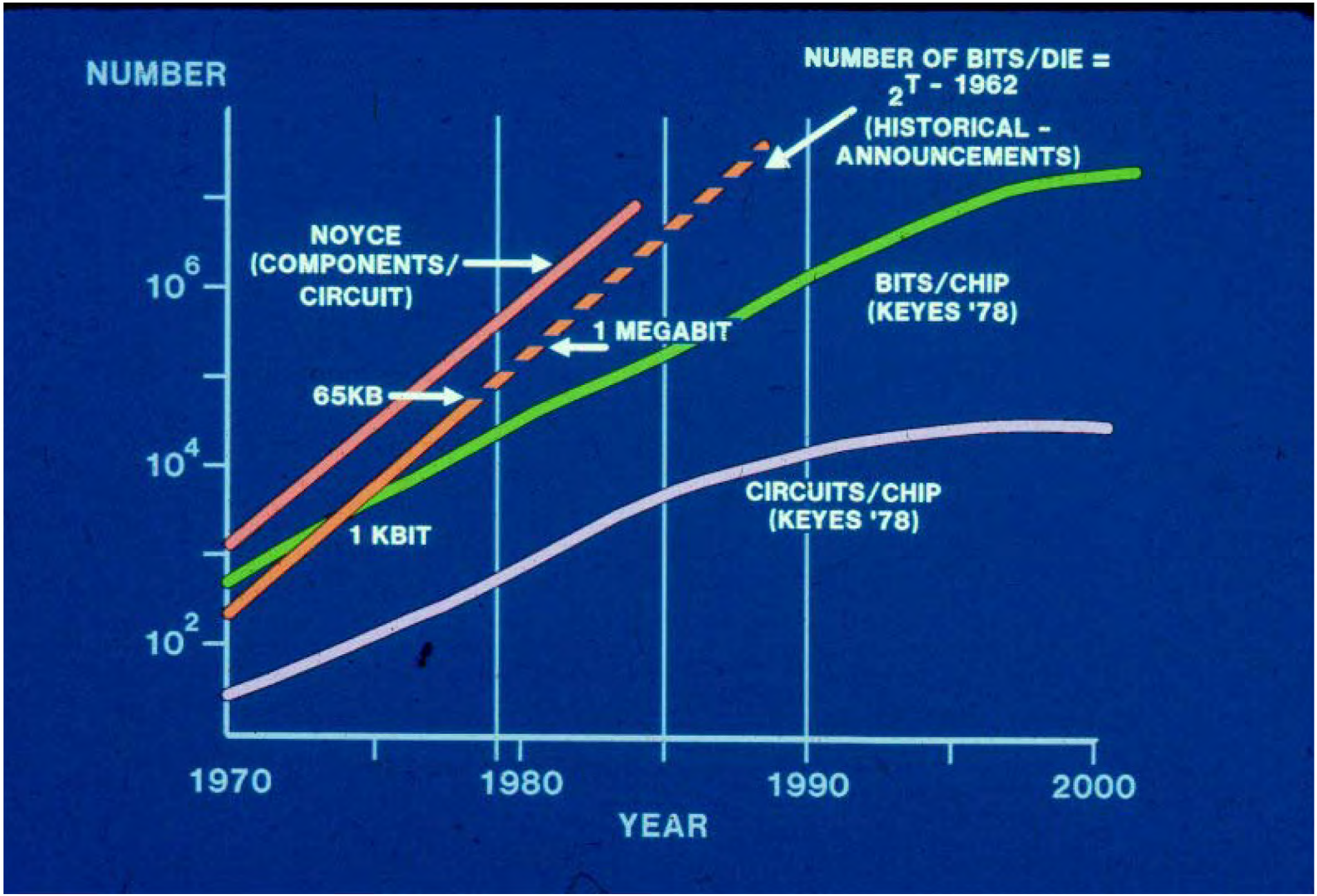
Effort (man-months) doubles each 2 2/3 years

i.e. $E = 3 \times 2^{(t-1962)/2.7}$



Note - Projected size limit $\backsim 10^8$ transistors


size (bits)
256K
65K
16K
4K
1K
256
MOS
Bi
81-83
79-80
76-77
73-74
CCD
Bub.
80-81
79-80
77-78
76-77
4 MS.
74-75
400MS avg.
2/21/77
Dean Toombe/TI
10
100
1000
75
100
1K
10K
100K
Ms
access time


NUMBER
NUMBER OF BITS/DIE = 2^{T-1962}
(HISTORICAL - ANNOUNCEMENTS)
NOYCE (COMPONENTS/ CIRCUIT)
10^6
10^4
10^2
1 MEGABIT
65KB
1 KBIT
BITS/CHIP (KEYES '78)
CIRCUITS/CHIP (KEYES '78)
1970
1980
1990
2000
YEAR

INDUSTRIES INVOLVED IN (INCREASED) INFORMATION PROCESSING

Semiconductor

- DIRECT
- Add-on and Emulation of Conventional Computers
- Indirect to ALL Industries → Microcomputer

Computer

- Mainframe
- Mini

} (Terminal Nets)

- Personal Computers
- Services

Communication

- New Phone-Based
- ACS
- Other Services Networks

Office Equipment

- Typewriters → Word Processing
- Fax → Communicating Xerox

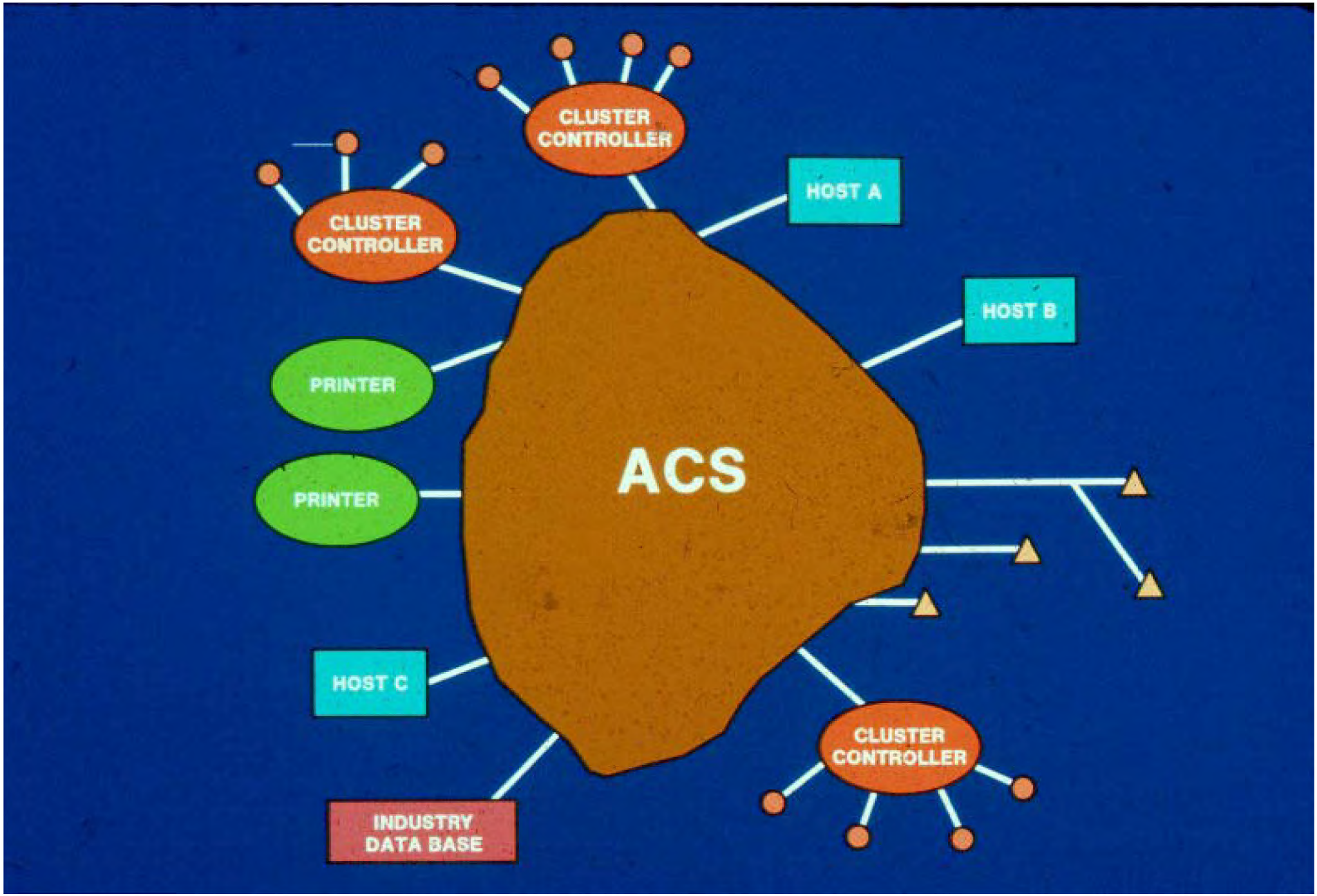
TV-Based Consumer Electronics

- Games → Personal Computers
- CATV as Communications

Substitution for Mechanical Control

WHY COMPUTERS EVOLVE (RAPIDLY)

- Science (Knowledge to Build With)
- Component Technology (What's Provided & We Cause)
- Development (What We Provide)
- Government (by Non-Interference)
- Users, e.g. (Demand & Development)
- Information Carried by Electrons vs Mass (Maxwell vs Newton)
- Clear Segmentation into Levels
- Computers are Fundamental (and Very Easy to Understand)
- Computer Engineering (Programming) Exists as a Well-Defined Body of Knowledge that can be Applied
- Infinite Number of Applications
- Economic Drive to Compete with (Substitute for) Other Information Switchers, Storers and Processors
- Lots of Involvement of Disciplines/Industries


CLUSTER CONTROLLER
CLUSTER CONTROLLER
HOST A
HOST B
PRINTER
PRINTER
ACS
HOST C
CLUSTER CONTROLLER
INDUSTRY DATA BASE

ACS

Access Control

- Terminate Access Lines
- Provide Terminal and Line Handling in Accordance with Standard Protocol
- Host – Character Oriented
  – Bit Oriented
- Supervisory Functions – Setup and Takedown
- Handles Network Command Consistent with Assigned Privileges
- Executes Interactive Customer Customized Programs
- Maintenance Line Testing

ACS

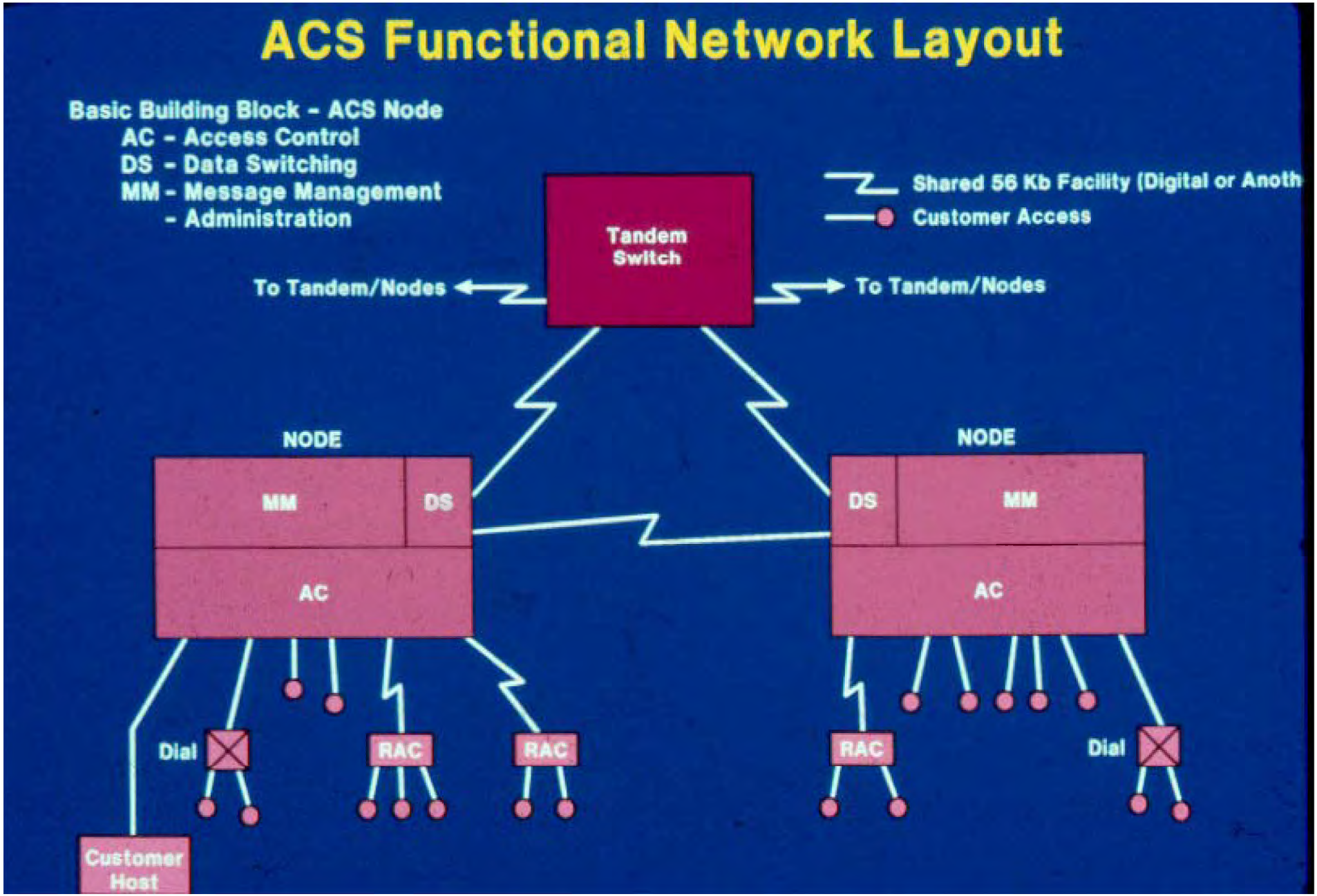
Data Switching

- Directs the Transfer of Customer Data Within the Network.
- Packet Switch is Employed
- Logical Paths Established through the Network from Organization to Destination

ACS

Message Management

- Messages Storage and Movement of Customer Data
- Provides a Wide Range of Service Options
  - Standard Message Features
  - Non-Interactive Customers Customized Programs
- Supports Service Administration and Maintenance


ACS Functional Network Layout
Basic Building Block - ACS Node
AC - Access Control
DS - Data Switching
MM - Message Management
- Administration
Shared 56 Kb Facility (Digital or Anoth
Customer Access
Tandem Switch
To Tandem/Nodes
To Tandem/Nodes
NODE
MM
DS
AC
NODE
DS
MM
AC
Dial
RAC
RAC
RAC
Dial
Customer Host

	SMALL (DECENTRAL)	LARGE (CENTRAL)
PERF	• >Avg.	• >>PEAK • >Mp. Peak
COST	• Economy Through Prod.	• Only Disk Economy of Scale
	• f (Comm. Costs, Utilization)	
	• Production Limited	• Design Limited
	• Overhead is Hidden - User is Programmer	
USE	• Small (Or O) Data Base	• Large Data Base
	• Fixed, Well-Defined Computation (e.g. Text, CAI, Stat. CALC.)	• Fully Gen. Purp.
SECURITY	• Private	• Easy to Share, Break
RELIABLE	• Dist.	• Cent. + Comm.