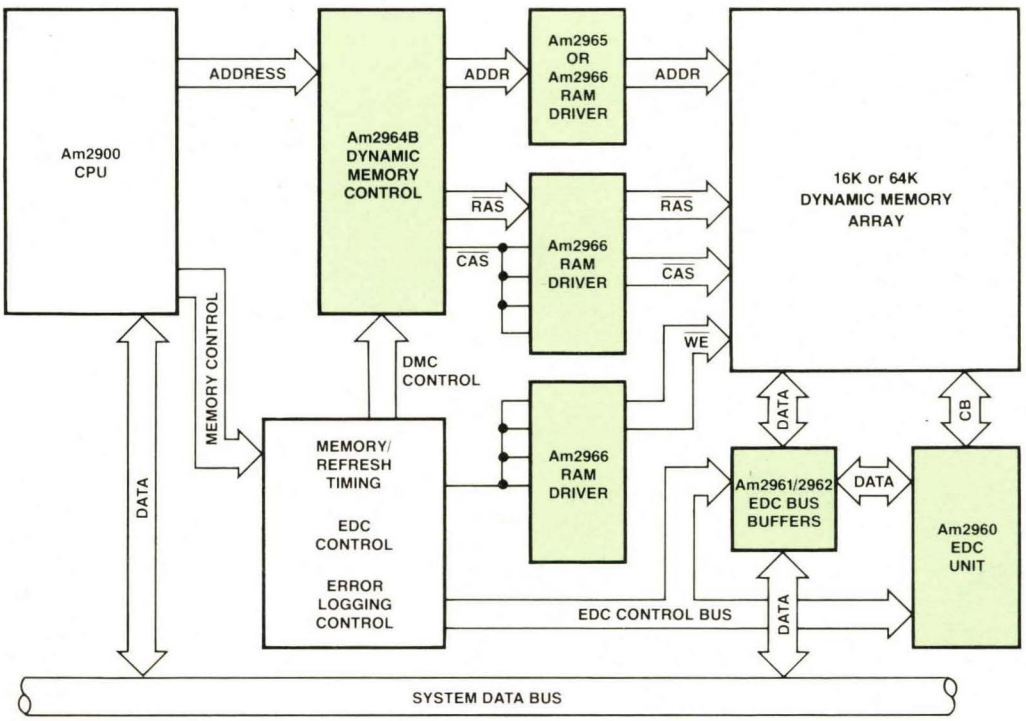
Advanced Micro Devices

Am2960 Series Dynamic Memory Support Handbook

- Error Detection/Correction
- Refresh and Control
- Data and Address Interface

Am2960 Dynamic Memory Support Handbook

HIGH PERFORMANCE COMPUTER MEMORY



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The International Standard of Quality guarantees these electrical AQLs on all parameters over the operating temperature range: 0.1% on MOS RAMs & ROMs; 0.2% on Bipolar Logic & Interface; 0.3% on Linear, LSI, ECL Logic & other memories.

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Am2900 FAMILY DYNAMIC MEMORY SUPPORT

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The Am2960 Family Dynamic Memory Support Products

Advanced Micro Devices has developed a set of bipolar high-performance memory-support products to maximize the speed and reliability of MOS dynamic RAM systems. This family is designed to provide, in the minimum package count, all the logic, interface and control functions required in the address and data paths of memory systems based on 16K and 64K devices.

These TTL-compatible products are specified for use in equipment based on either bipolar or MOS CPUs. The Am2960 Series serves bipolar microprocessors such as the Am2901, Am29203, etc., while the AmZ8160 Series serves MOS microprocessors, such as the 16-bit AmZ8000.

Key System Level Features

Maximum Memory Performance

- Schottky performance with matched T_{PD} paths and skew limit guarantees.
- Optimized interface devices for maximum speed.
- Hamming code EDC with internal ECL circuitry for maximum speed combined with maximum memory reliability.

Lowest Package Count Plus Maximum Flexibility

- LSI DMC Controller is designed for up to 64K RAMs.
- EDC is 16-bit expandable slice with byte I/O controls.
- Flexible interface for speed or minimum parts count.

Operation in Any Timing Environment

- Synchronous Clock Timing (AmZ8000 systems).
- Delay-line timing for maximum performance.

Operation with Any RAM Refresh Mode

- 128 of 256 Line Refresh

All Refresh Modes

- Burst Refresh
- Hidden (transparent) Refresh
- Cycle Steal Refresh

Am2960 Family Product Summary

Am2960 • AmZ8160 Error Detection and Correction (EDC)

- High-speed 16-bit slice expandable to 64 bits
- Single-bit correction/double-bit detection
- Byte-op controls
- Initialization and diagnostics built-in

Am2961/62 • AmZ8161/62 EDC Data Bus Buffer

- EDC interface between RAM, EDC and data bus
- 24mA bus drive with three-state control
- Separated RAM I/O with undershoot protection
- Bus latches for byte-op or multiplexed buses

AmZ8163 EDC and Refresh Control for AmZ8000 Systems

- RAS/MUX/CAS timing control for AmZ8164
- EDC control for word or byte read and write
- Memory/refresh request arbitration
- Refresh timer and control independent of CPU

Am2964 • AmZ8164 Dynamic Memory Control (DMC)

- 16-bit address for up to 64K RAMs
- Refresh Counter for 128- or 256-line refresh
- 3-port 8-bit Schottky speed address MUX
- RAS and CAS paths on-chip for minimum skew

Am2965/66 • AmZ8165/66 Octal Dynamic RAM Drivers

- −0.5V maximum undershoot
- V_{OH}/I_{OH} specs for MOS with no external resistors
- t_{PLH}/t_{PHL} min and max specs for 50pF and 500pF
- Pin-compatible with 'S240/244

System Overview

By John R. Mick

As larger and larger dynamic RAMs are used with microprocessors, minicomputers and even larger computer systems, the design engineer becomes increasingly concerned about the reliability of his memory system. As the RAM size increases, the error rate caused by alpha particles increases significantly. It is essential therefore that all new memory designs using higher density dynamic RAMs (and perhaps even larger static RAMs) use error detection and correction (EDC) to improve memory system reliability. Current estimates are that the reliability can be increased by a factor of 60 or more if a suitable error detection and correction scheme is employed.

Advanced Micro Devices is introducing a new set of LSI devices that allows the designer to implement error detection and correction in a cost effective fashion. In addition, EDC can slash field maintenance costs and allow systems to run longer uninterrupted due to soft or hard memory errors. If desired, memory errors can be logged for future use in determining marginal RAM chips by running memory diagnostics routines.

The Advanced Micro Devices Am2960 Memory Support family of products includes the Am2960 Error Detection and Correction Unit, the Am2961/2962 EDC Bus Buffers, the Am2964B Dynamic Memory Controller and the Am2965/2966 Dynamic RAM Drivers. The system interconnection of these devices is shown in Figure 1 where a typical Am2900 microcomputer memory system is configured. As shown in this diagram, the memory support subsystem interfaces to the System Data Bus, Address Bus, and control signals.

The Am2964B Dynamic Memory Controller is used to provide all address handling, as well as $\overline{RAS}$ and $\overline{CAS}$ decoding and control. A block diagram of the Am2964B dynamic memory controller is shown in Figure 2. The device contains 18 input latches for capturing an 18-bit address for memory control. The two highest order addresses are decoded in the Am2964B to select one of four banks of RAM by selecting one of the four $\overline{RAS}$ outputs.

The Am2964B is designed to operate with either 16K Dynamic RAMs or 64K Dynamic RAMs. Thus, the designer either uses 14 of the multiplexer address inputs and 7 of the address outputs or all 16 of the multiplexer address inputs and all 8 of the address outputs as needed by the memory. In the case of 16K dynamic RAMs, 7 address inputs are provided to the RAM during the $\overline{RAS}$ LOW signal and then the 8-bit multiplexer is switched so that 7 upper address bits are provided to the RAM for the $\overline{CAS}$ LOW part of the cycle. The Am2964B Dynamic Memory Controller contains an 8-bit refresh counter that is used to supply the refresh address to the dynamic memory during the refresh cycle. This counter can be used in either the 128 or 256 line refresh mode. A $\overline{CAS}$ buffer is included in the dynamic memory controller so that the $\overline{CAS}$ output can be inhibited during refresh.

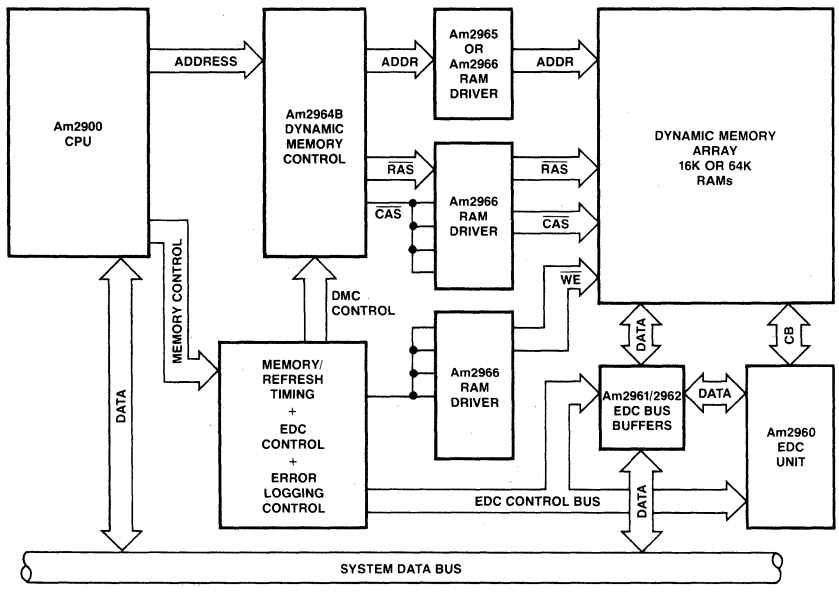

Figure 1. Am2900 High Performance Computer Memory

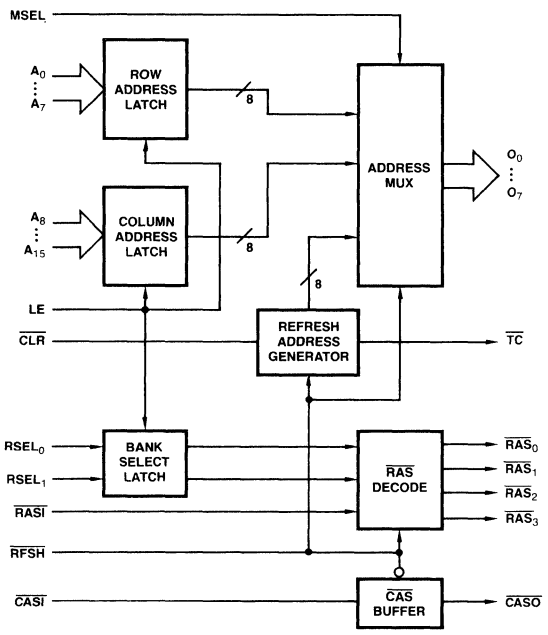

Figure 2. Am2964B Dynamic Memory Controller

Normal operation of the Dynamic Memory Controller is to provide the address, close the input address latches and kick off a normal memory cycle. This is accomplished by bringing the $\overline{RASI}$ input LOW which will cause one of the $\overline{RAS}$ outputs to go LOW. After the required memory timing, the MSEL input will be used to switch the multiplexer to the other address latch. Then, the $\overline{CASI}$ input will be driven LOW causing the $\overline{CASO}$ output to go LOW and execute the $\overline{CAS}$ part of the memory cycle. The refresh cycle is executed by driving the $\overline{RFSH}$ input LOW which causes the multiplexer to select the refresh counter to its address outputs. Then, the $\overline{RASI}$ input is driven LOW which causes all four $\overline{RAS}$ outputs to go LOW. This will simultaneously refresh all four banks of dynamic RAMs controlled by the Am2964B Dynamic Memory Controller. When either the $\overline{RFSH}$ or $\overline{RASI}$ input is brought HIGH, the refresh counter is advanced so it will be ready for the next refresh cycle.

As can be seen in Figure 1, Dynamic RAM Drivers can be used in large memory systems to buffer the Address, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE\ ENABLE}$ signals to the RAMs. The Am2965 and Am2966 are pin compatible devices with the Am74S240 and Am74S244. These RAM drivers are specifically designed for driving dynamic RAMs and feature high capacitance drive, guaranteed maximum undershoot of less than −0.5 volts and high V_{OH} of greater than V_{CC} −1.15 volts. The Am2965 is inverting and the Am2966 is noninverting. The devices feature symmetrical rise and fall times and have guaranteed minimum and maximum t_{PD} specifications at both 50pF and 500pF loads. loads.

Data interface between the dynamic memories, the Am2960 EDC chip and the system data bus is accomplished by means of the Am2961/2962 bus buffers. Figure 3 depicts the architecture of these devices along with a simplified block diagram of the Am2960. The Am2961 is inverting between the system data bus and the EDC bus while the Am2962 is noninverting between the system data bus and the EDC bus. As shown in Figure 3, the Am2961 and Am2962 contain two internal latches, a multiplexer, and a RAM driver output buffer.

These devices feature 4-bit wide data paths to and from the RAM, to the EDC, and to the system data bus. The bus-input (BI) latch is used predominantly in byte WRITE operations so that an incoming byte from the system data bus can be stored while the memory is being read and any necessary correction is made in the bytes not being changed. The bus-output (BO) latch in the bus buffer is used predominantly for storing the output data if the processor is in the single step mode. In the single step mode it is necessary to hold the output data on the system data bus but the memory must be released for refresh.

The Am2960 Error Detection and Correction Unit contains all the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming code and to correct the data word when check bits are supplied. Operating on the data read from memory, the Am2960 will correct any single bit error and will detect all double and some triple bit errors. For 16-bit words, 6 check bits are used. The Am2960 is expandable to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome bits available on separate outputs for data logging.

The Am2960 also features two diagnostic modes in which diagnostic data can be forced into portions of the device to simplify device testing and to execute system diagnostic functions.

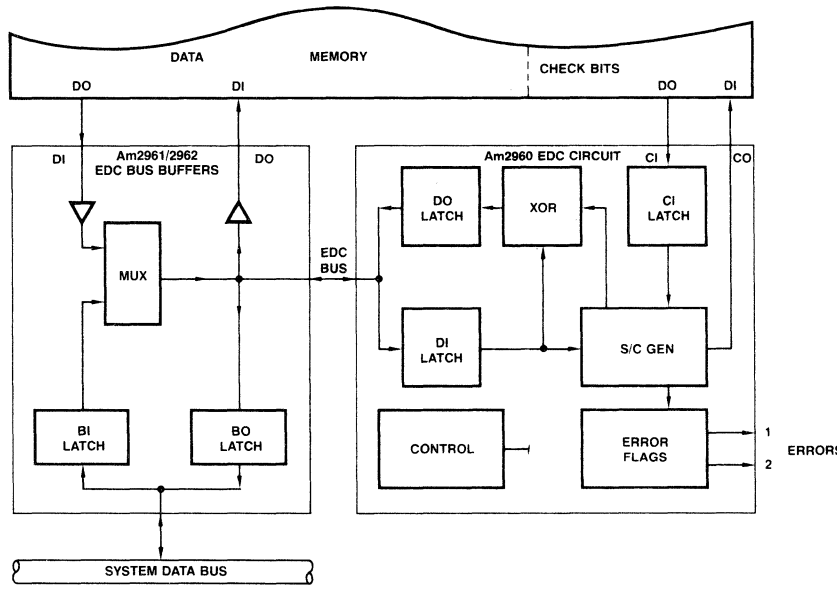

Figure 3. EDC Data Path

As shown in the Figure 4 Am2960 block diagram, the device consists of the following:

- Data Input Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Data Output Latch
- Diagnostic Latch
- Control Latch

16 bits of data are loaded into the Data Input Latch from the bidirectional Data lines under control of the Latch Enable input. Depending on the control mode the input data is either used for check bit generation or error detection/correction.

Seven check bits are loaded into the Check Bit Input Latch under control of LE IN. Check bits are used in the Error Detection and Error Correction modes.

The Check Bit Generation Logic generates the appropriate check bits for the 16 bits of data in the Data Input Latch. The check bits are generated according to a modified Hamming code.

In both Error Detection and Error Correction modes, the Syndrome Generation Logic block compares the check bits read from memory against a newly generated set of check bits produced for the data read in from memory. If both sets of check bits match, then there are no errors. If there is a mismatch, then one or more of the data or check bits is in error.

The syndrome bits are produced by an exclusive-OR of the two sets of check bits. If the two sets of check bits are identical (meaning there are no errors) the syndrome bits will be all zeroes. If the syndromes are non-zero, the syndrome bits can be decoded to determine the number of errors and the bit-in-error (single error).

The Error Detection Logic decodes the syndrome bits generated by the Syndrome Generation Logic. If there are no errors in either the input data or check bits, the $\overline{\text{ERROR}}$ and $\overline{\text{MULTI ERROR}}$ outputs remain HIGH. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, both $\overline{\text{ERROR}}$ and $\overline{\text{MULTI ERROR}}$ go LOW.

For single errors, the Error Correction Logic complements (corrects) the single data bit in error. This corrected data is loadable into the Data Output Latch, which can then be read onto the bidirectional data lines. If the single error is one of the check bits, the correction logic does not place corrected bits on the syndrome/check bit outputs. If the corrected check bits are needed the EDC must be switched to Generate Mode.

The Data Output Latch is used for storing the result of an error correction operation. The latch is loaded from the correction logic under control of the Data Output Latch Enable, LE OUT. The Data Output Latch may also be loaded directly from the Data Input Latch under control of the PASS THRU control input.The Data Output Latch is split into two 8-bit (byte) latches which may be enabled independently for reading onto the bidirectional data lines.

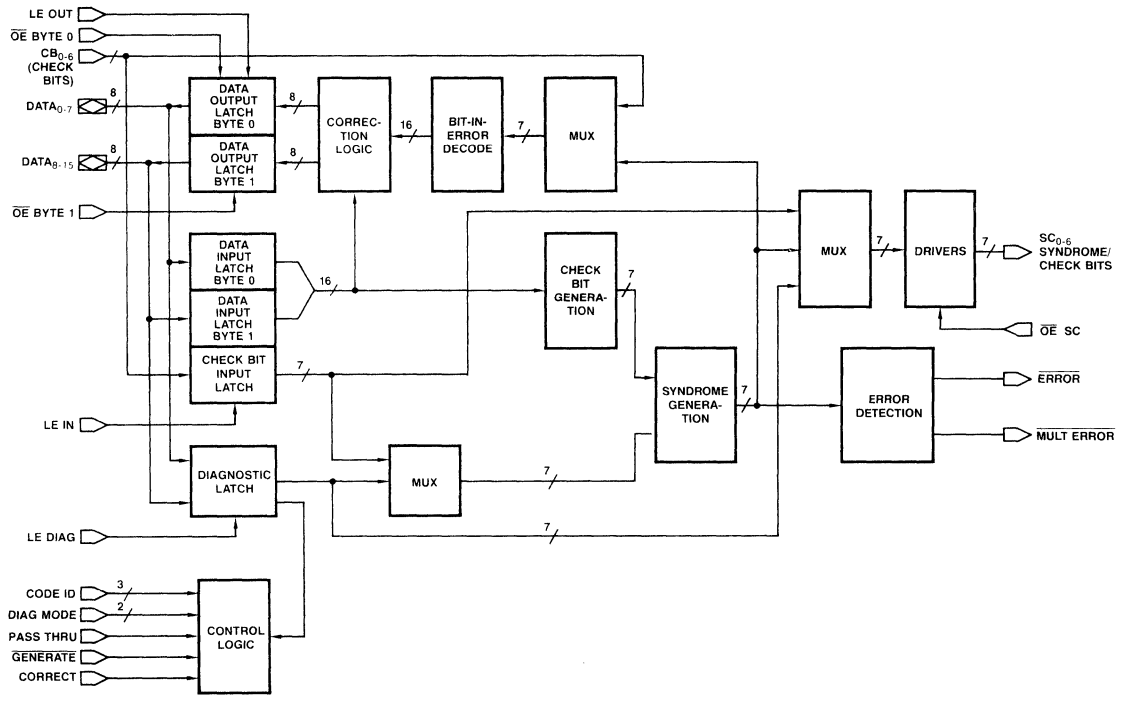

Figure 4. Am2960 Block Diagram

The Diagnostic Latch is a 16-bit latch loadable from the bidirectional data lines under control of the Diagnostic Latch Enable, LE DIAG. The Diagnostic Latch contains check bit information in one byte and control information in the other byte. The Diagnostic Latch is used for driving the device when in Internal Control Mode, or for supplying check bits when in one of the Diagnostic Modes.

The control logic determines the specific mode the device operates in. Normally the control logic is driven by external control inputs. However, in Internal Control Mode, the control signals are instead read from the Diagnostic Latch.

As can be seen, the Am2960 Family can be used to significantly improve the MTTF (Mean Time to Failure) of memory systems. By boosting memory reliability, two competitive advantages are gained. First, the system can run uninterrupted with either single soft errors or the loss of one memory chip. Second, field maintenance costs can be reduced in that service can be scheduled on a regular basis and faulty memory components can be replaced by reviewing logged errors.

The demand for reliable system performance is increasing steadily. Reliability is a must for applications in aerospace, medical, banking, process control and on-line systems. Applications such as word processors, small business systems and telecommunications also need memory reliability, as their users do not have the technical staff to handle system failures and are willing to pay for the convenience of smooth, error free operation. The Am2960 Family is the solution in these systems.

Am2960
Fast Error Detection and Correction for Memories

Corrects All Single-Bit Errors

Corrects all single bit errors. Detects all double and some triple bit errors.

Expandable

One Am2960 provides Error Detection and Correction for 16-bits. Two Am2960s handle 32 bits; four Am2960s handle 64 bits.

Fast

Worst case 32 nanoseconds for error detect and 65 nanoseconds for error correct (16 bits).

Latches Built-In

Check Bit, Data, and Diagnostic latches are built-in to save MSI.

Flexible

Can be used with Am2900-based designs, the AmZ8000 or other processors.

Diagnostics Built-In

Logic on-chip for device test and software-controlled diagnostics.

Increases Memory Reliability

And can significantly reduce field maintenance costs.

A Must for 64K RAMs

Alpha error rates are several times higher for 64K RAMs than 16Ks.

Also available as the AmZ8160 for AmZ8000 Systems

Am2960 EDC

Cascadable 16-Bit Error Detection and Correction Unit

DISTINCTIVE CHARACTERISTICS

- **Boosts Memory Reliability**
  Corrects all single-bit errors. Detects all double and some triple-bit errors. Reliability of dynamic RAM systems is increased more than 60-fold.
- **Very High Speed**
  Perfect for MOS microprocessor, minicomputer, and mainframe systems.
  - Data in to error detect: 32ns worst case.
  - Data in to corrected data out: 65ns worst case.

  High performance systems can use the Am2960 EDC in check-only mode to avoid memory system slowdown.
- **Replaces 25 to 50 MSI chips**
  All necessary features are built-in to the Am2960 EDC, including diagnostics, data in, data out, and check bit latches.
- **Handles Data Words From 8 to 64 Bits**
  The Am2960 EDC cascades: 1 EDC for 8 or 16 bits, 2 for 32 bits, 4 for 64 bits.
- **Easy Byte Operations**
  Separate byte enables on the data out latch simplify the steps and cuts the time required for byte writes.
- **Diagnostics Built-In**
  The processor may completely exercise the EDC under software control to check for proper operation of the EDC.

GENERAL DESCRIPTION

The Am2960 Error Detection and Correction Unit (EDC) contains the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming Code, and to correct the data word when check bits are supplied. Operating on data read from memory, the Am2960 will correct any single bit error and will detect all double and some triple bit errors. For 16-bit words, 6 check bits are used. The Am2960 is expandable to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome available on separate outputs for data logging.

The Am2960 also features two diagnostic modes, in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions. The product is supplied in a 48 lead hermetic DIP package.

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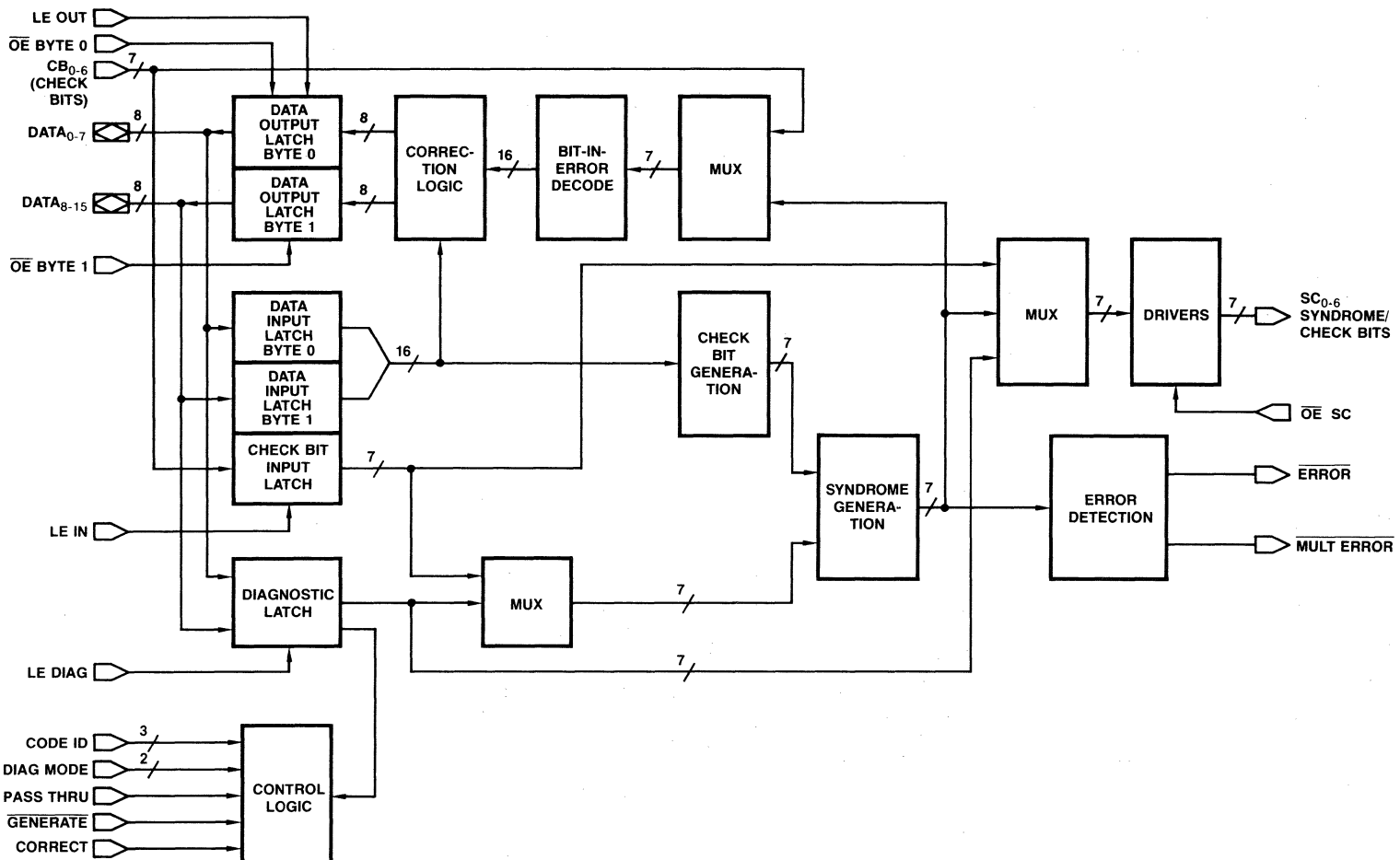
BLOCK DIAGRAM



EDC Architecture

The EDC Unit is a powerful 16-bit cascadable slice used for check bit generation, error detection, error correction and diagnostics.

As shown in the block diagram, the device consists of the following:

- Data Input Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Data Output Latch
- Diagnostic Latch
- Control Logic

Data Input Latch

16 bits of data are loaded from the bidirectional DATA lines under control of the Latch Enable input, LE IN. Depending on the control mode the input data is either used for check bit generation or error detection/correction.

Check Bit Input Latch

Seven check bits are loaded under control of LE IN. Check bits are used in the Error Detection and Error Correction modes.

Check Bit Generation Logic

This block generates the appropriate check bits for the 16 bits of data in the Data Input Latch. The check bits are generated according to a modified Hamming code.

Syndrome Generation Logic

In both Error Detection and Error Correction modes, this logic block compares the check bits read from memory against a newly generated set of check bits produced for the data read in from memory. If both sets of check bits match, then there are no errors. If there is a mismatch, then one or more of the data or check bits is in error.

The syndrome bits are produced by an exclusive-OR of the two sets of check bits. If the two sets of check bits are identical (meaning there are no errors) the syndrome bits will be all zeroes. If there are errors, the syndrome bits can be decoded to determine the number of errors and the bit-in-error.

Error Detection Logic

This section decodes the syndrome bits generated by the Syndrome Generation Logic. If there are no errors in either the input data or check bits, the $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ outputs remain HIGH. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, both $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ go LOW.

Error Correction Logic

For single errors, the Error Correction Logic complements (corrects) the single data bit in error. This corrected data is loadable into the Data Output Latch, which can then be read onto the bidirectional data lines. If the single error is one of the check bits, the correction logic does not place corrected check bits on the syndrome/check bit outputs. If the corrected check bits are needed the EDC must be switched to Generate Mode.

Data Output Latch

The Data Output Latch is used for storing the result of an error correction operation. The latch is loaded from the correction logic under control of the Data Output Latch Enable, LE OUT. The Data Output Latch may also be loaded directly from the Data Input Latch under control of the PASS THRU control input.

The Data Output Latch is split into two 8-bit (byte) latches which may be enabled independently for reading onto the bidirectional data lines.

Diagnostic Latch

This is a 16-bit latch loadable from the bidirectional data lines under control of the Diagnostic Latch Enable, LE DIAG. The Diagnostic Latch contains check bit information in one byte and control information in the other byte. The Diagnostic Latch is used for driving the device when in Internal Control Mode, or for supplying check bits when in one of the Diagnostic Modes.

Control Logic

The control logic determines the specific mode the device operates in. Normally the control logic is driven by external control inputs. However, in Internal Control Mode, the control signals are instead read from the Diagnostic Latch.

PIN DEFINITIONS

$DATA_{0-15}$ 16 bidirectional data lines. They provide input to the Data Input Latch and Diagnostic Latch, and receive output from the Data Output Latch. $DATA_0$ is the least significant bit; $DATA_{15}$ the most significant.

CB_{0-6} Seven Check Bit input lines. The check bit lines are used to input check bits for error detection. Also used to input syndrome bits for error correction in 32 and 64-bit configurations.

LE IN Latch Enable – Data Input Latch. Controls latching of the input data. When HIGH the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.

$\overline{\text{GENERATE}}$ Generate Check Bits input. When this input is LOW the EDC is in the Check Bit Generate Mode. When HIGH the EDC is in the Detect Mode or Correct Mode.

In the Generate Mode the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs.

In the Detect or Correct Modes the EDC detects single and multiple errors, and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In Correct Mode, single-bit errors are also automatically corrected – corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the bit-in-error.

SC_{0-6} Syndrome/Check Bit outputs. These seven lines hold the check/partial-check bits when the EDC is in Generate Mode, and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct Modes. These are 3-state outputs.

$\overline{\text{OE SC}}$ Output Enable – Syndrome/Check Bits. When LOW, the 3-state output lines SC_{0-6} are enabled. When HIGH, the SC outputs are in the high impedance state.

$\overline{\text{ERROR}}$ Error Detected output. When the EDC is in Detect or Correct Mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate Mode, $\overline{\text{ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{ERROR}}$ must be externally implemented.)

$\overline{\text{MULT ERROR}}$ Multiple Errors Detected output. When the EDC is in Detect or Correct Mode, this output if LOW indicates that there are two or more bit errors that have been detected. If HIGH this indicates that either one or no errors have been detected. In Generate mode, $\overline{\text{MULT ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{MULT ERROR}}$ must be externally implemented.)

CORRECT Correct input. When HIGH this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it onto the Data Output Latch. When LOW the EDC will drive data directly from the Data Input Latch to the Data Output Latch without correction.

LE OUT Latch Enable – Data Output Latch. Controls the latching of the Data Output Latch. When LOW the Data Output Latch is latched to its previous state. When HIGH the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are unspecified if the EDC is in Generate Mode.

$\overline{\text{OE}}$ BYTE 0, $\overline{\text{OE}}$ BYTE 1 Output Enable – Bytes 0 and 1, Data Output Latch. These lines control the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW these lines enable the Data Output Latch and when HIGH these lines force the Data Output Latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output Latch at a time.

PASS THRU Pass Thru input. This line when HIGH forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs (SC_{0-6}) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.

DIAG $MODE_{0-1}$ Diagnostic Mode Select. These two lines control the initialization and diagnostic operation of the EDC.

CODE ID_{0-2} Code Identification inputs. These three bits identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDC is processing. The three allowable data word sizes are 16, 32 and 64 bits and their respective modified Hamming codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID_2, ID_1, ID_0) is also used to instruct the EDC that the signals CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU are to be taken from the Diagnostic Latch, rather than from the input control lines.

LE DIAG Latch Enable – Diagnostic Latch. When HIGH the Diagnostic Latch follows the 16-bit data on the input lines. When LOW the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits, and internal control signals for CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU.

FUNCTIONAL DESCRIPTION

The EDC contains the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming code. Operating on data read from memory, the EDC will correct any single-bit error, and will detect all double and some triple-bit errors. The Am2960 may be configured to operate on 16-bit data words (with 6 check bits), 32-bit data words (with 7 check bits) and 64-bit data words (with 8 check bits). In fact the EDC can be configured to work on data words from 8 to 64 bits. In all configurations, the device makes the error syndrome bits available on separate outputs for error data logging.

Code and Byte Specification

The EDC may be configured in several different ways and operates differently in each configuration. It is necessary to indicate to the device what size data word is involved and which bytes of the data word it is processing. This is done with input lines CODE ID_{0-2}, as shown in Table I. The three modified Hamming codes referred to in Table I are:

- 16/22 – 16 data bits
  – 6 check bits
  – 22 bits in total.
- 32/39 code – 32 data bits
  – 7 check bits
  – 39 bits in total.
- 64/72 code – 64 data bits
  – 8 check bits
  – 72 bits in total.

CODE ID input 001 (ID_2, ID_1, $!D_0$) is a special code used to operate the device in Internal Control Mode (described later in this section).

Control Mode Selection

The device control lines are $\overline{\text{GENERATE}}$, CORRECT, PASS THRU, DIAG $MODE_{0-1}$ and CODE ID_{0-2}. Table III indicates the operating modes selected by various combinations of the control line inputs.

Diagnostics

Table II shows specifically how DIAG $MODE_{0-1}$ select between normal operation, initialization and one of two diagnostic modes.

The Diagnostic Modes allow the user to operate the EDC under software control in order to verify proper functioning of the device.

Check and Syndrome Bit Labeling

The check bits generated in the EDC are designated as follows:

- 16-bit configuration – CX C0, C1, C2, C4, C8;
- 32-bit configuration – CX, C0, C1, C2, C4, C8, C16;
- 64-bit configuration – CX, C0, C1, C2, C4, C8, C16, C32.

Syndrome bits are similarly labeled SX through S32. There are only 6 syndrome bits in the 16-bit configuration, 7 for 32 bits and 8 syndrome bits in the 64-bit configuration.

Initialize Mode

The inputs of the Data Output Latch are forced to zeroes. The check bit outputs (SC) are generated to correspond to the all-zero data. $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ are forced HIGH in the Initialize Mode.

Initialize Mode is useful after power up when RAM contents are random. The EDC may be placed in initialize mode and its' outputs written in to all memory locations by the processor.

TABLE I. HAMMING CODE AND SLICE IDENTIFICATION.

CODE ID_2	CODE ID_1	CODE ID_0	Hamming Code and Slice Selected
0	0	0	Code 16/22
0	0	1	Internal Control Mode
0	1	0	Code 32/39, Bytes 0 and 1
0	1	1	Code 32/39, Bytes 2 and 3
1	0	0	Code 64/72, Bytes 0 and 1
1	0	1	Code 64/72, Bytes 2 and 3
1	1	0	Code 64/72, Bytes 4 and 5
1	1	1	Code 64/72, Bytes 6 and 7

TABLE II. DIAGNOSTIC MODE CONTROL.

DIAG $MODE_1$	DIAG $MODE_0$	Diagnostic Mode Selected
0	0	**Non-diagnostic mode.** The EDC functions normally in all modes.
0	1	**Diagnostic Generate.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate Mode. The EDC functions normally in the Detect or Correct modes.
1	0	**Diagnostic Detect/Correct.** In the Detect or Correct Mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate Mode.
1	1	**Initialize.** The outputs of the Data Input Latch are forced to zeroes (and latched upon removal of the Initialize Mode) and the check bits generated correspond to the all-zero data.

HAMMING CODE SELECTION

The Am2960 EDC uses a modified Hamming Code that allows 1) the EDC to be cascaded, 2) all double errors to be detected, 3) the gross error conditions of all 0s or 1s to be detected.

The error correction code can be selected independent of the processor with the exception of diagnostics software.

Diagnostic software run by a processor to checkout the EDC system must know specifically which code is being used. This is only a problem when the EDC replaces an existing MSI implementation on an existing computer. In this case, the computer's software must first determine which of two codes (the old one used by the MSI implementation or the new one used by the EDC) is used by the computer's memory system.

This is easily determined by writing a test data word into memory and then examining whether the generated check bits are typical of the old or the new code. From then on the software runs only the diagnostic appropriate for the code used on that particular computer's memory system.

TABLE III. Am2960 OPERATING MODES

Operating Mode	Diagnostic Mode**		$\overline{\text{GENERATE}}$	
	DM_1	DM_0	0	1
Normal	0	0	Generate	Correct*
Diagnostic Generate	0	1	Diagnostic Generate	Correct*
Diagnostic Correct	1	0	Generate	Diagnostic Correct*
Initialize	1	1	Initialize	Initialize
Pass Thru	When PASS THRU is asserted the Operating Mode is defaulted to the Pass Thru Mode.			

*Correct if the CORRECT Input is HIGH, Detect if the CORRECT Input is LOW.
**In Code $ID_{2\text{-}0}$ 001 (ID_2, ID_1, ID_0) DM_1 and DM_0 are taken from the Diagnostic Latch.

FUNCTIONAL DESCRIPTION – 16-BIT DATA WORD CONFIGURATION

The 16-bit format consists of 16 data bits, 6 check bits and is referred to as 16/22 code (see Figure 5.)

The 16-bit configuration is shown in Figure 6.

Generate Mode

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the outputs SC_{0-5} (SC_6 is a logical one, or high).

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table IV. Each check bit is generated as either an XOR or XNOR of eight of the 16 data bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR is an odd parity check bit.

Figure 1 shows the data flow in the Generate Mode.

Detect Mode

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, $\overline{\text{MULT ERROR}}$ goes LOW. Both error indicators are HIGH if there are no errors.

Also available on device outputs SC_{0-5} are the syndrome bits generated by the error detection step. The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table V gives the chart for decoding the syndrome bits generated by the 16-bit configuration (as an example, if the syndrome bits SX/S0/S1/S2/S4/S8 were 101001 this would be decoded to indicate that there is a single-bit error at data bit 9). If no error is detected the syndrome bits will all be zeroes.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without correction.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. (see Figure 2.) If multiple errors are detected, the output of the correction network is unspecified. If the single-bit error is a check bit there is no automatic correction. If check bit correction is desired, this can be done by placing the device in Generate Mode to produce a correct check bit sequence for the data in the Data Input Latch.

Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch and the contents of the Check Bit Input Latch are placed on outputs SC_{0-5}. $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ are forced HIGH in this mode.

Diagnostic Latch

The Diagnostic Latch serves both for diagnostic uses and internal control uses. It is loaded from the DATA lines under the control of LE DIAG. Table VI shows the loading definitions for the DATA lines.

Diagnostic Generate
Diagnostic Detect
Diagnostic Correct

These are special diagnostic modes selected by DIAG $MODE_{0-1}$ where either normal check bit inputs or outputs are substituted for by check bits loaded into the Diagnostic Latch. See Table III for details. Figures 3 and 4 illustrate the flow of data during the two diagnostic modes.

Internal Control Mode

This mode is selected by CODE ID_{0-2} input 001 (ID_2, ID_1, ID_0).

When in Internal Control Mode, the EDC takes the CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU control signals from the internal Diagnostic Latch rather than from the external input lines.

Table VI gives the format for loading the Diagnostic Latch.

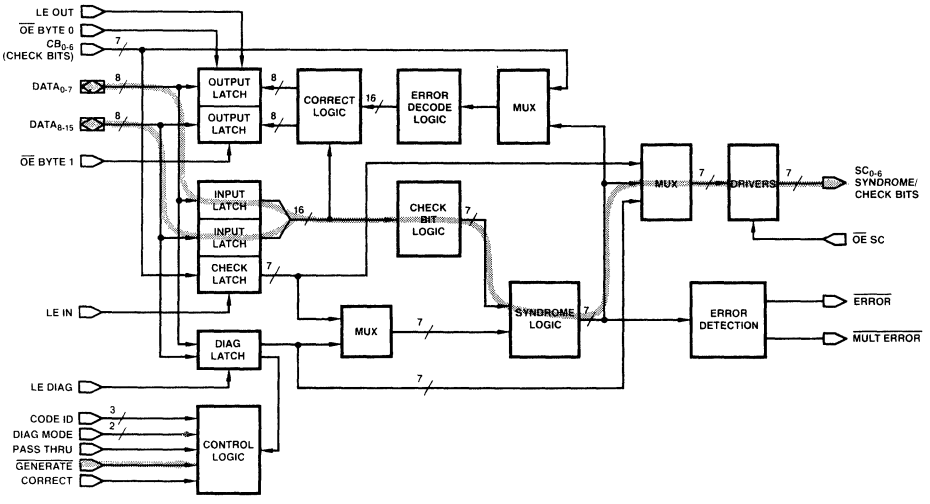


Figure 1. Check Bit Generation

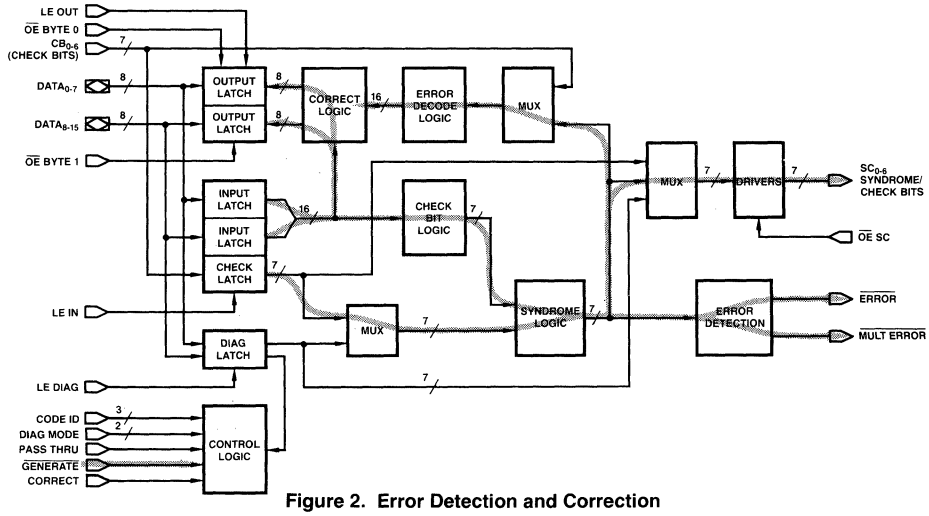


Figure 2. Error Detection and Correction

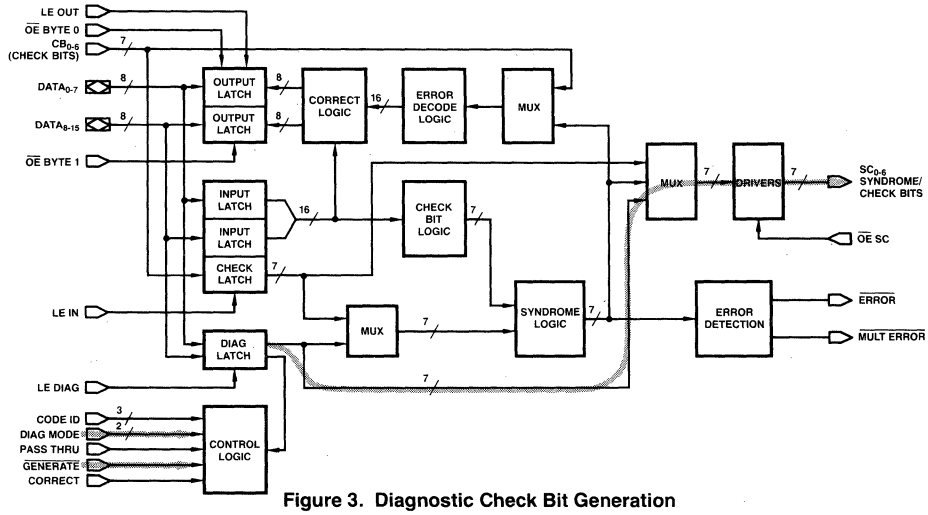


Figure 3. Diagnostic Check Bit Generation

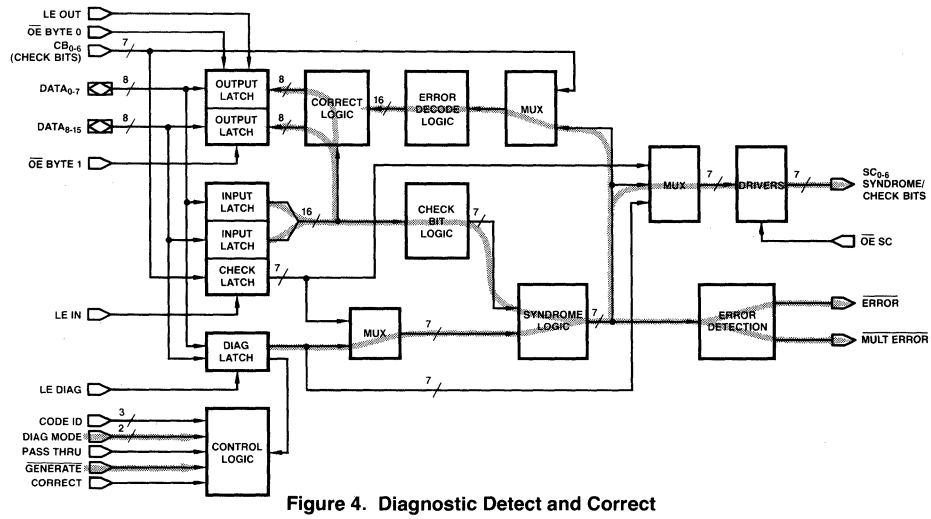
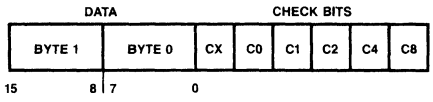


Figure 4. Diagnostic Detect and Correct



Uses Modified Hamming Code 16/22
- 16 data bits
- 6 check bits
- 22 bits in total

Figure 5. 16-Bit Data Format

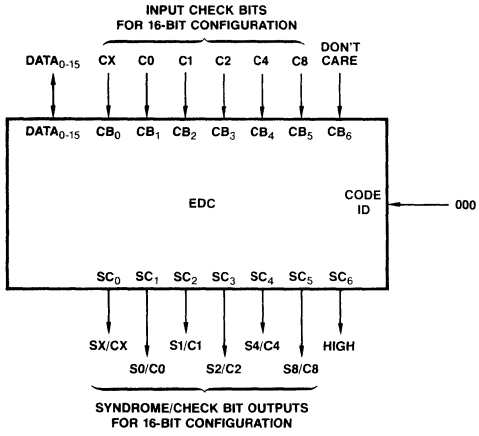


Figure 6. 16-Bit Configuration

TABLE IV. 16-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART.

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X

The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

TABLE V. SYNDROME DECODE TO BIT-IN-ERROR.

Syndrome Bits			S8	0	1	0	1	0	1	0	1
			S4	0	0	1	1	0	0	1	1
			S2	0	0	0	0	1	1	1	1
SX	S0	S1									
0	0	0		*	C8	C4	T	C2	T	T	M
0	0	1		C1	T	T	15	T	13	7	T
0	1	0		C0	T	T	M	T	12	6	T
0	1	1		T	10	4	T	0	T	T	M
1	0	0		CX	T	T	14	T	11	5	T
1	0	1		T	9	3	T	M	T	T	M
1	1	0		T	8	2	T	1	T	T	M
1	1	1		M	T	T	M	T	M	M	T

* – no errors detected
Number – the location of the single bit-in-error
T – two errors detected
M – three or more errors detected

TABLE VI. DIAGNOSTIC LATCH LOADING – 16-BIT FORMAT.

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	CODE ID 0
9	CODE ID 1
10	CODE ID 2
11	DIAG MODE 0
12	DIAG MODE 1
13	CORRECT
14	PASS THRU
15	Don't Care

FUNCTIONAL DESCRIPTION – 32-BIT DATA WORD CONFIGURATION

The 32-bit format consists of 32 data bits, 7 check bits and is referred to as 32/39 code (see Figure 7).

The 32-bit configuration is shown in Figure 8.

The upper EDC (Slice 0/1) handles the least significant bytes 0 and 1 – the external DATA lines 0 to 15 are connected to the same numbered inputs of the upper device. The lower EDC (Slice 2/3) handles the most significant bytes 2 and 3 – the external DATA lines for bits 16 to 31 are connected to inputs $DATA_0$ through $DATA_{15}$ respectively.

The valid syndrome and check bit outputs are those of Slice 2/3 as shown in the diagram. In Correct Mode these must be read into Slice 0/1 via the CB inputs and are selected by the MUX as inputs to the bit-in-error decoder (see block diagram), thus requiring external buffering and output enabling of the check bit lines as shown. The $\overline{OE}$ SC signal can be used to control enabling of check bit inputs – when syndrome outputs are enabled, the external check bit inputs will be disabled.

The valid $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ outputs are those of the Slice 2/3. The $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ outputs of Slice 0/1 are unspecified. All of the latch enables and control signals must be input to both of the devices.

Generate Mode

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the outputs $SC_{0\text{-}6}$ of Slice 2/3.

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table X. Check bits are generated as either an XOR or XNOR of 16 of the 32 data bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR in an odd parity check bit.

Detect Mode

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{ERROR}$ goes LOW. If two or more errors are detected, $\overline{MULT\ ERROR}$ goes LOW. Both error indicators are HIGH if there are no errors. The valid $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ signals are those of Slice 2/3 – those of Slice 0/1 are undefined.

Also available on Slice 2/3 outputs $SC_{0\text{-}6}$ are the syndrome bits generated by the error detection step. The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table VII gives the chart for decoding the syndrome bits generated for the 32-bit configuration (as an example, if the syndrome bits SX/S0/S1/S2/S4/S8/S16 were 0010011 this would be decoded to indicate that there is a single-bit error at data bit 25). If no error is detected the syndrome bits will be all zeroes.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without corrections.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified. If the single-bit error is a check bit there is no automatic correction – if desired this would be done by placing the device in Generate Mode to produce a correct check bit sequence for the data in the Data Input Latch.

For data correction, both Slices 0/1 and 2/3 require access to the syndrome bits on Slice 2/3's outputs $SC_{0\text{-}6}$. Slice 2/3 has access to these syndrome bits through internal data paths, but for Slice 0/1 they must be read through the inputs $CB_{0\text{-}6}$. The device connections for this are shown in Figure 8. When in Correct Mode the SC outputs must be enabled so that they are available for reading in through the CB inputs.

Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch and the contents of the Check Bit Input Latch are placed on outputs $SC_{0\text{-}6}$ of Slice 2/3. $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ are forced HIGH in this mode.

TABLE VII. SYNDROME DECODE TO BIT-IN-ERROR.

Syndrome Bits				S16	0	1	0	1	0	1	0	1
				S8	0	0	1	1	0	0	1	1
				S4	0	0	0	0	1	1	1	1
SX	S0	S1	S2									
0	0	0	0		*	C16	C8	T	C4	T	T	30
0	0	0	1		C2	T	T	27	T	5	M	T
0	0	1	0		C1	T	T	25	T	3	15	T
0	0	1	1		T	M	13	T	23	T	T	M
0	1	0	0		C0	T	T	24	T	2	M	T
0	1	0	1		T	1	12	T	22	T	T	M
0	1	1	0		T	M	10	T	20	T	T	M
0	1	1	1		16	T	T	M	T	M	M	T
1	0	0	0		CX	T	T	M	T	M	14	T
1	0	0	1		T	M	11	T	21	T	T	M
1	0	1	0		T	M	9	T	19	T	T	31
1	0	1	1		M	T	T	29	T	7	M	T
1	1	0	0		T	M	8	T	18	T	T	M
1	1	0	1		17	T	T	28	T	6	M	T
1	1	1	0		M	T	T	26	T	4	M	T
1	1	1	1		T	0	M	T	M	T	T	M

* – no errors detected
Numbers – number of the single bit-in-error
T – two errors detected
M – three or more errors detected

Uses Modified Hamming Code 32/39
– 32 data bits
– 7 check bits
– 39 bits in total

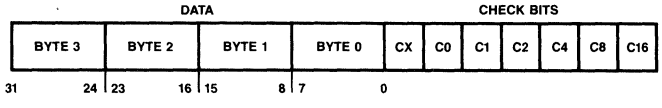


Figure 7. 32-Bit Data Format

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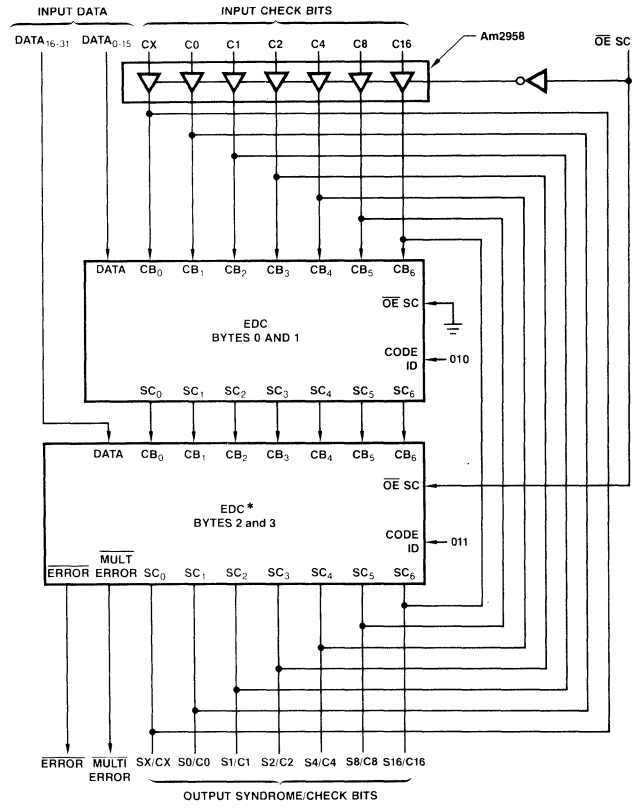


*Check Bit Latch is Forced Transparent in this Code ID Combination for this Slice.

Figure 8. 32-Bit Configuration

TABLE VIII. KEY AC CALCULATIONS FOR THE 32-BIT CONFIGURATION

32-Bit Propagation Delay		Component Delay from Am2960 AC Specifications, Table C
From	To	
DATA	Check Bits Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA In	Corrected DATA Out	(DATA to SC) + (CB to SC, CODE ID 011) + (CB to DATA, CODE ID 010)
DATA	Syndromes Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	$\overline{\text{ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{ERROR}}$, CODE ID 011)
DATA	$\overline{\text{MULT ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 011)

TABLE IX. DIAGNOSTIC LATCH LOADING – 32-BIT FORMAT.

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6	Diagnostic Check Bit 16
7	Don't Care
8	Slice 0/1 – CODE ID 0
9	Slice 0/1 – CODE ID 1
10	Slice 0/1 – CODE ID 2
11	Slice 0/1 – DIAG MODE 0
12	Slice 0/1 – DIAG MODE 1
13	Slice 0/1 – CORRECT
14	Slice 0/1 – PASS THRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 – CODE ID 0
25	Slice 2/3 – CODE ID 1
26	Slice 2/3 – CODE ID 2
27	Slice 2/3 – DIAG MODE 0
28	Slice 2/3 – DIAG MODE 1
29	Slice 2/3 – CORRECT
30	Slice 2/3 – PASS THRU
31	Don't Care

TABLE X. 32-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART.

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)	X				X		X	X	X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X					X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X

The check bit is generated as either an XOR or XNOR of the sixteen data bits noted by an "X" in the table.

FUNCTIONAL DESCRIPTION – 64-BIT DATA WORD CONFIGURATION

The 64-bit format consists of 64 data bits, 8 check bits and is referred to as 64/72 code (see Figure 9.).

The configuration to process 64-bit format is shown in Figure 6. In this configuration a portion of the syndrome generation and error detection is implemented externally of the EDCs in MSI. For error correction the syndrome bits generated must be read back into all four EDCs through the CB inputs. This necessitates the check bit buffering shown in the connection diagram of Figure 10. The $\overline{OE}$ SC signal can control the check bit enabling – when syndrome bit outputs are enabled the external check bit lines will be disabled so that the syndrome bits may be read onto the CB inputs.

The error detection signals for the 64-bit configuration differ from the 16 and 32-bit configurations. The $\overline{ERROR}$ signal functions the same: it is LOW if one or more errors are detected, and HIGH if no errors are detected. The DOUBLE ERROR signal is HIGH if and only if a double-bit error is detected – it is LOW otherwise. All of the $\overline{MULT\ ERROR}$ outputs of the four devices are valid. $\overline{MULT\ ERROR}$ is LOW for all three ERROR cases and some DOUBLE ERROR combinations. (See TOME definition in Functional Equations section.) It is HIGH if either zero or one errors are detected.

This is a different meaning for $\overline{MULT\ ERROR}$ than in other configurations.

Generate Mode

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated appear at the outputs of the XOR gates as indicated in Figure 10.

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table XII. Check bits are generated as either an XOR or XNOR of 32 of the 64 bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR in an odd parity check bit.

Detect Mode

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{ERROR}$ goes LOW. If exactly two errors are detected, DOUBLE ERROR goes HIGH. If three or more errors are detected, $\overline{MULT\ ERROR}$ goes LOW – the $\overline{MULT\ ERROR}$ output of any of the four EDCs may be used.

Available as XOR gate outputs are the generated syndrome bits (see Figure 10). The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table XIII gives the chart for encoding the syndrome bits generated for the 64-bit configuration (as an example, if the syndrome bits SX/S1/S2/S4/S8/S16/S32 were 00100101 this would be decoded to indicate that there is a single-bit error at data bit 41). If no error is detected the syndrome bits will all be zeroes.

In Detect Mode the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without corrections.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified. If the single bit error is a check bit there is no automatic correction. Check bit correction can be done by placing the device in generate mode to produce a correct check bit sequence for the data in the Data Input Latch.

To perform the correction step, all four slices require access to the syndrome bits which are generated externally of the devices. This access is provided by reading the syndrome bits in through the CB inputs where they are selected as inputs to the bit-in-error decoder by the multiplexer (see block diagram). The device connections for this are shown in Figure 10. When in Correct Mode the SC outputs must be enabled so that the syndrome bits are available at the CB inputs.

Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch, and the contents of the Check Bit Input Latch are passed through the external XOR network and appear inverted at the XOR gate outputs labeled CX to C32 (see Figure 10).

Diagnostic Latch

The Diagnostic Latch serves both for diagnostic uses and internal control uses. It is loaded from the DATA lines under the control of LE DIAG. Table XIV shows the loading definitions for the DATA lines.

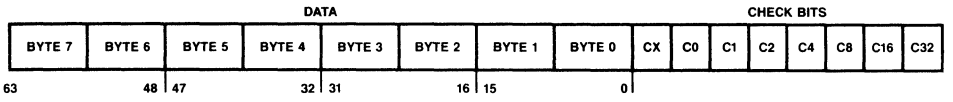
Diagnostic Generate
Diagnostic Detect
Diagnostic Correct

These are special diagnostic modes selected by DIAG $MODE_{0\text{-}1}$ where either normal check bit inputs or outputs are substituted for by check bits from the Diagnostic Latch. See Table II for details.

Internal Control Mode

This mode is selected by CODE $ID_{0\text{-}2}$, input 001 (ID_2, ID_1, ID_0).

When in Internal Control Mode the EDC takes the CODE $ID_{0\text{-}2}$, DIAG $MODE_{0\text{-}1}$, CORRECT and PASS THRU signals from the internal Diagnostic Latch rather than from the external control lines. Table XIV gives format for loading the Diagnostic Latch.



Uses Modified Hamming Code 64/72
- 64 data bits
- 8 check bits
- 72 bits in total

Figure 9. 64-Bit Data Format

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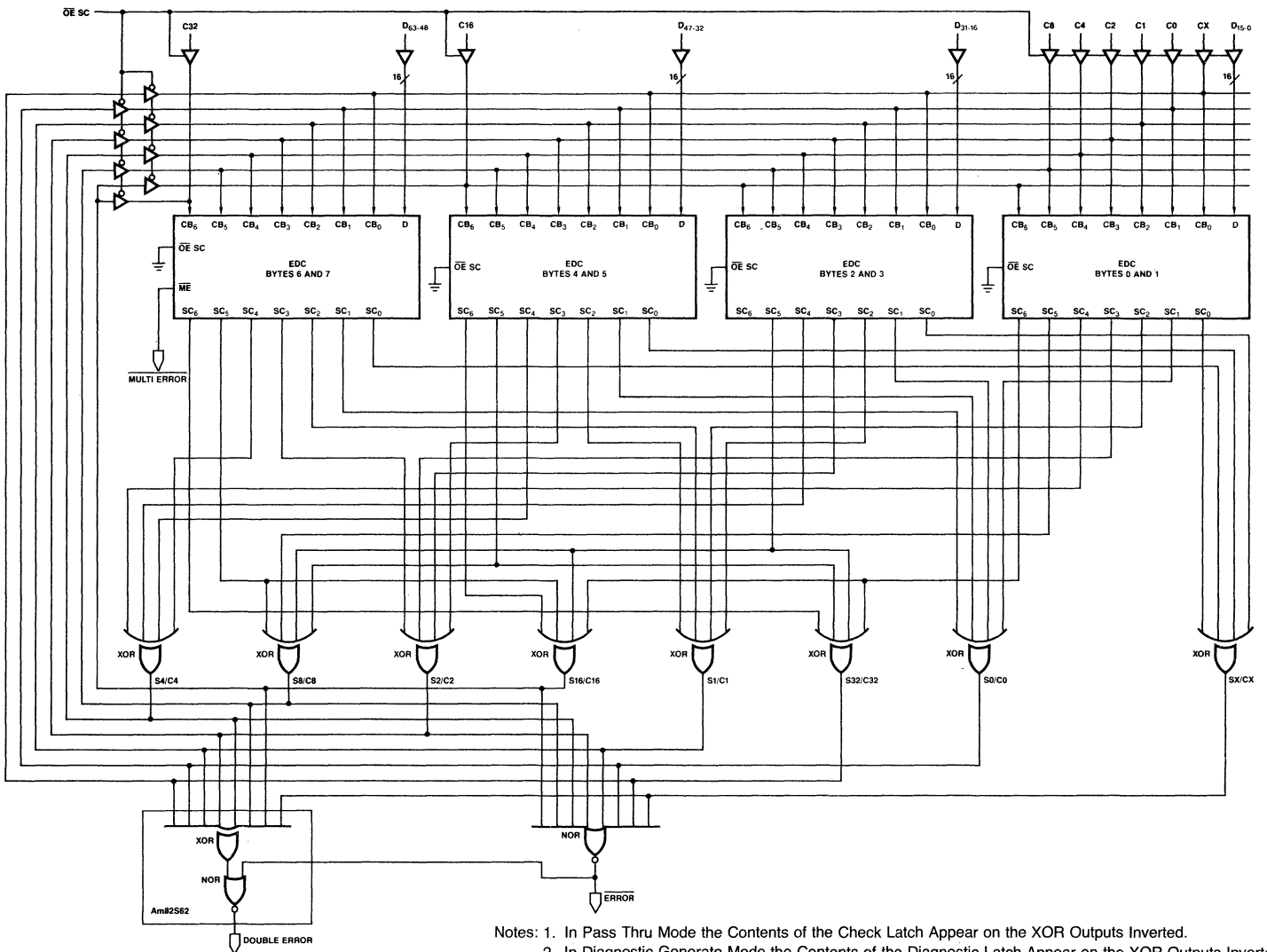


Notes: 1. In Pass Thru Mode the Contents of the Check Latch Appear on the XOR Outputs Inverted.
2. In Diagnostic Generate Mode the Contents of the Diagnostic Latch Appear on the XOR Outputs Inverted.

Figure 10. Am2960 — 64-Bit Data Configuration

TABLE XI. KEY AC CALCULATIONS FOR THE 64-BIT CONFIGURATION

64-Bit Propagation Delay		Component Delays from Am2960 AC Specifications, Table C (plus MSI)
From	To	
DATA	Check Bits Out	(DATA to SC) + (XOR Delay)
DATA In	Corrected DATA Out	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to DATA, CODE ID 1xx)
DATA	Syndromes	(DATA to SC) + (XOR Delay)
DATA	$\overline{\text{ERROR}}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (NOR Delay)
DATA	$\overline{\text{MULT ERROR}}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 1xx)
DATA	DOUBLE ERROR for 64 Bits	(DATA to SC) + (XOR Delay) + (XOR/NOR Delay)

TABLE XII. 64-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)	X	X	X	X	X	X	X	X								

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)									X	X	X	X	X	X	X	X

Generated Check Bits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)									X	X	X	X	X	X	X	X

Generated Check Bits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)	X	X	X	X	X	X	X	X								

The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

TABLE XIII. SYNDROME DECODE TO BIT-IN-ERROR.

Syndrome Bits SX	S0	S1	S2																
S32				0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
S16				0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
S8				0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
S4				0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	0	*	C32	C16	T	C8	T	T	M	C4	T	T	M	T	46	62	T
0	0	0	1	C2	T	T	M	T	43	59	T	T	53	37	T	M	T	T	M
0	0	1	0	C1	T	T	M	T	41	57	T	T	51	35	T	15	T	T	31
0	0	1	1	T	M	M	T	13	T	T	29	23	T	T	7	T	M	M	T
0	1	0	0	C0	T	T	M	T	40	56	T	T	50	34	T	M	T	T	M
0	1	0	1	T	49	33	T	12	T	T	28	22	T	T	6	T	M	M	T
0	1	1	0	T	M	M	T	10	T	T	26	20	T	T	4	T	M	M	T
0	1	1	1	16	T	T	0	T	M	M	T	T	M	M	T	M	T	T	M
1	0	0	0	CX	T	T	M	T	M	M	T	T	M	M	T	14	T	T	30
1	0	0	1	T	M	M	T	11	T	T	27	21	T	T	5	T	M	M	T
1	0	1	0	T	M	M	T	9	T	T	25	19	T	T	3	T	47	63	T
1	0	1	1	M	T	T	M	T	45	61	T	T	55	39	T	M	T	T	M
1	1	0	0	T	M	M	T	8	T	T	24	18	T	T	2	T	M	M	T
1	1	0	1	17	T	T	1	T	44	60	T	T	54	38	T	M	T	T	M
1	1	1	0	M	T	T	M	T	42	58	T	T	52	36	T	M	T	T	M
1	1	1	1	T	48	32	T	M	T	T	M	M	T	T	M	T	M	M	T

* – no errors detected
Number – the number of the single bit-in-error
T – two errors detected
M – more than two errors detected

TABLE XIV. DIAGNOSTIC LATCH LOADING – 64-BIT FORMAT.

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	Slice 0/1 – CODE ID 0
9	Slice 0/1 – CODE ID 1
10	Slice 0/1 – CODE ID 2
11	Slice 0/1 – DIAG MODE 0
12	Slice 0/1 – DIAG MODE 1
13	Slice 0/1 – CORRECT
14	Slice 0/1 – PASS THRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 – CODE ID 0
25	Slice 2/3 – CODE ID 1
26	Slice 2/3 – CODE ID 2
27	Slice 2/3 – DIAG MODE 0
28	Slice 2/3 – DIAG MODE 1
29	Slice 2/3 – CORRECT
30	Slice 2/3 – PASS THRU

Data Bit	Internal Function
31	Don't Care
32-37	Don't Care
38	Diagnostic Check Bit 16
39	Don't Care
40	Slice 4/5 – CODE ID 0
41	Slice 4/5 – CODE ID 1
42	Slice 4/5 – CODE ID 2
43	Slice 4/5 – DIAG MODE 0
44	Slice 4/5 – DIAG MODE 1
45	Slice 4/5 – CORRECT
46	Slice 4/5 – PASS THRU
47	Don't Care
48-54	Don't Care
55	Diagnostic Check Bit 32
56	Slice 6/7 – CODE ID 0
57	Slice 6/7 – CODE ID 1
58	Slice 6/7 – CODE ID 2
59	Slice 6/7 – DIAG MODE 0
60	Slice 6/7 – DIAG MODE 1
61	Slice 6/7 – CORRECT
62	Slice 6/7 – PASS THRU
63	Don't Care

MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Case) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for high Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0 mA

OPERATING RANGE

P/N	Range	Temperature	V_{CC}	
Am2960DC, XC	COM'L	T_A = 0 to +70°C	V_{CC} = 5.0V ±5%	(MIN = 4.75V, MAX = 5.25V)
Am2960DM, FM, XM	MIL	T_C = −55 to +125°C	V_{CC} = 5.0V ± 10%	(MIN = 4.50V, MAX = 5.50V)

DC CHARACTERISTICS

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −0.8mA	COM'L	2.7			Volts
				MIL	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA				0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 7)			2.0			Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 7)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V	$DATA_{0-15}$				−410	μA
			All Other Inputs				−360	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	$DATA_{0-15}$				70	μA
			All Other Inputs				50	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} MAX	$DATA_{0-15}$	V_O = 2.4			70	μA
				V_O = 0.5			−410	
			SC_{0-6}	V_O = 2.4			50	
				V_O = 0.5			−50	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = V_{CC} MAX +0.5V, V_O = 0.5V			−25		−85	mA
I_{CC}	Power Supply Current (Note 6)	V_{CC} = MAX		T_A = 25°C		275	390	mA
			COM'L	T_A = 0 to +70°C			400	
				T_A = +70°C			365	
			MIL	T_C = −55 to +125°C			400	
				T_C = +125°C			345	

Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input Characteristics are measured with output enables HIGH.
5. "MIL" = Am2960XM, DM, FM. "COM'L" = Am2960XC, DC.
6. Worst case I_{CC} is at minimum temperature.
7. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \leq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

1. Am2960 Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2960 over the commercial operating range of 0 to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2960DC, XC.

A. Combinational Propagation Delays
C_L = 50pF

From Input \ To Output	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	32	65*	32	50
CB_{0-6} (CODE ID_{2-0} 000, 011)	28	56	29	47
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	28	45	29	34
$\overline{GENERATE}$	35	63	36	55
CORRECT (Not Internal Control Mode)	–	45	–	–
DIAG MODE (Not Internal Control Mode)	50	78	59	75
PASS THRU (Not Internal Control Mode)	36	44	29	46
CODE ID_{2-0}	61	90	60	80
LE IN (From latched to transparent)	39	72*	39	59
LE OUT (From latched to transparent)	–	31	–	–
LE DIAG (From latched to transparent; Not Internal Control Mode)	45	78	45	65
Internal Control Mode: LE DIAG (From latched to transparent)	67	96	66	86
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	67	96	66	86

*Data In (or LE In) to Correct Data Out measurement requires timing as shown in Figure D opposite.

B. Set-up and Hold Times Relative to Latch Enables

From Input	To (Latching Up Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE IN	6	7
CB_{0-6}	LE IN	5	6
$DATA_{0-15}$	LE OUT	44	5
CB_{0-6} (CODE ID 000, 011)	LE OUT	35	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE OUT	27	0
$\overline{GENERATE}$	LE OUT	42	0
CORRECT	LE OUT	26	1
DIAG MODE	LE OUT	69	0
PASS THRU	LE OUT	26	0
CODE ID_{2-0}	LE OUT	81	0
LE IN	LE OUT	51	5
$DATA_{0-15}$	LE DIAG	6	8

C. Output Enable/Disable Times

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$ BYTE 0, $\overline{OE}$ BYTE 1	$DATA_{0-15}$	30	30
$\overline{OE}$ SC	SC_{0-6}	30	30

D. Minimum Pulse Widths

LE IN, LE OUT, LE DIAG	15

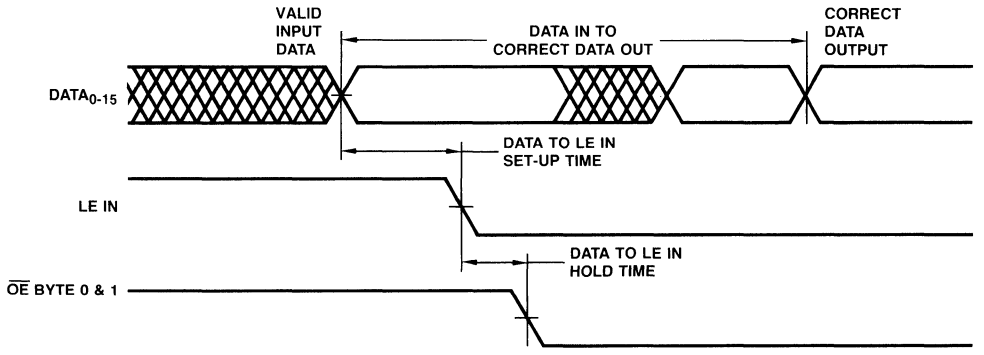


Figure D.

1. Am2960 Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the Am2960 over the military operating range of −55 to +125°C case temperature, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2960DM, FM, XM.

A. Combinational Propagation Delays
C_L = 50pF

From Input \ To Output	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	35	73*	36	56
CB_{0-6} (CODE ID_{2-0} 000, 011)	30	61	31	50
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	30	50	31	37
$\overline{GENERATE}$	38	69	41	62
CORRECT (Not Internal Control Mode)	–	49	–	–
DIAG MODE (Not Internal Control Mode)	58	89	65	90
PASS THRU (Not Internal Control Mode)	39	51	34	54
CODE ID_{2-0}	69	100	68	90
LE IN (From latched to transparent)	44	82*	43	66
LE OUT (From latched to transparent)	–	33	–	–
LE DIAG (From latched to transparent; Not Internal Control Mode)	50	88	49	72
Internal Control Mode: LE DIAG (From latched to transparent)	75	106	74	96
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	75	106	74	96

*Data In (or LE In) to Correct Data Out measurement requires timing as shown in Figure D opposite.

B. Set-up and Hold Times Relative to Latch Enables

From Input	To (Latching Up Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE IN	7	7
CB_{0-6}	LE IN	5	7
$DATA_{0-15}$	LE OUT	50	5
CB_{0-6} (CODE ID 000, 011)	LE OUT	38	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE OUT	30	0
$\overline{GENERATE}$	LE OUT	46	0
CORRECT	LE OUT	28	1
DIAG MODE	LE OUT	84	0
PASS THRU	LE OUT	30	0
$CODE\ ID_{2-0}$	LE OUT	89	0
LE IN	LE OUT	59	5
$DATA_{0-15}$	LE DIAG	7	9

C. Output Enable/Disable Times

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$ BYTE 0, $\overline{OE}$ BYTE 1	$DATA_{0-15}$	35	35
$\overline{OE}$ SC	SC_{0-6}	35	35

D. Minimum Pulse Widths

LE IN, LE OUT, LE DIAG	15

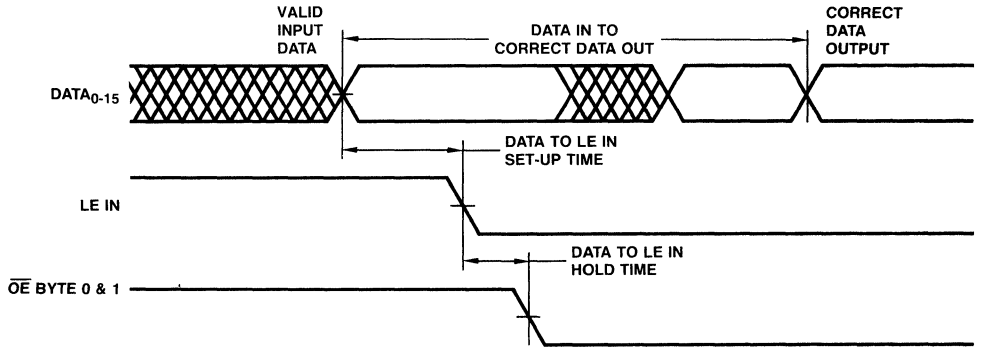
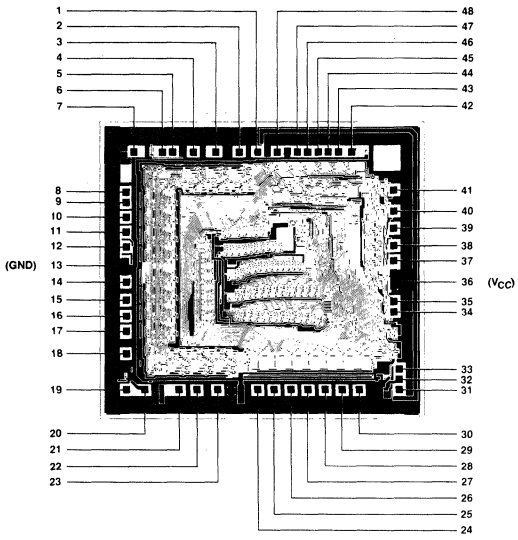


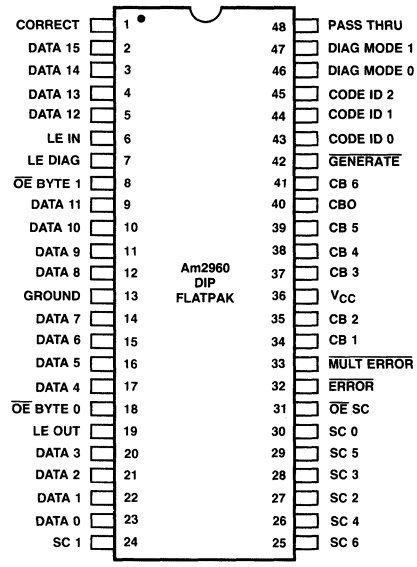
Figure D.

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.200" X 0.183"

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2960 Order Number (Note 3)	Package Type Order Number	Operating Range (Note 1)	Screening Level (Note 2)
AM2960DC	D-48	C	C-1
AM2960DC-B	D-48	C	B-2 (Note 4)
AM2960DM	D-48	M	C-3
AM2960DM-B	D-48	M	B-3
AM2960FM	F-48	M	C-3
AM2960FM-B	F-48	M	B-3
AM2960XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2960XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75V to 5.25V, M = −55 to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

TEST OUTPUT LOAD CONFIGURATION FOR Am2960

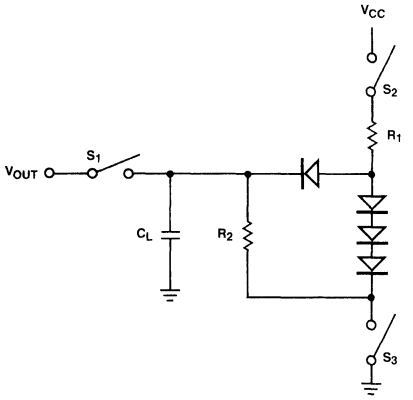


Figure 11. Three-State Outputs

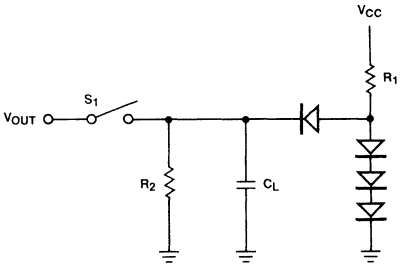


Figure 12. Normal Outputs

Notes:
1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function test and all A.C. tests, except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. R_2 = 1K for three-state output.
   R_2 is determined by the I_{OH} at V_{OH} = 2.4V for non-three-state outputs.
5. R_1 is determined by I_{OL} (MIL) with V_{CC} = 5.0V minus the current to ground through R_2.
6. C_L = 5.0 pF for output disable tests.

TEST OUTPUT LOADS

Pin #	Pin Label	Test Circuit	R_1	R_2
–	D_0-D_{15}	Fig. 11	430Ω	1kΩ
24-30	SC_0-SC_6	Fig. 11	430Ω	1kΩ
32	$\overline{\text{ERROR}}$	Fig. 12	470Ω	3kΩ
33	$\overline{\text{MULTERROR}}$	Fig. 12	470Ω	3kΩ

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

APPLICATIONS

Byte Write

Byte operations are increasingly common for 16 and 32-bit processors. These complicate memory operations because check bits are generated for a complete 16 or 32 or 64-bit memory word, not for a single byte.

To write a byte into memory with EDC requires the following steps:

- Latch the byte into the Am2961/62 bus buffers (Figure 13)
- Read the complete data word from memory (Figure 13)
- Correct the complete data word if necessary (Figure 13)
- Insert the byte to be written into the data word (Figure 14)
- Generate new check bits for the entire data word (Figure 14)
- Store the data word back into memory (Figure 14)

(In fact these steps must be taken for any piece of data being written into memory that is not as wide as a full memory word).

The Am2960 EDC is designed with the intent of keeping byte operations simple in EDC systems. The EDC has separate output enables for each byte in the Data Output Latch. As shown in figures 13 and 14, this allows the data word to be read from memory, the new byte to be inserted among the old, and new check bits to be generated using less time and less hardware than if separate byte enables were not available.

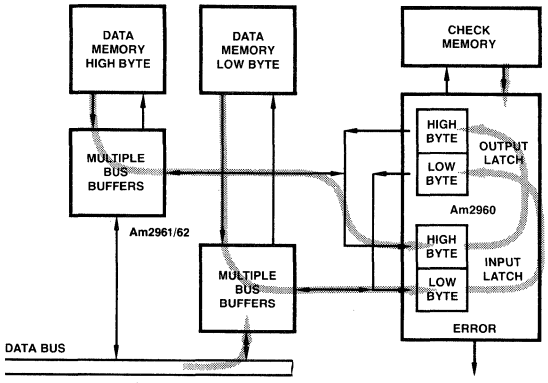


Figure 13. Byte Write, Phase 1: Read Out the Old Word and Correct

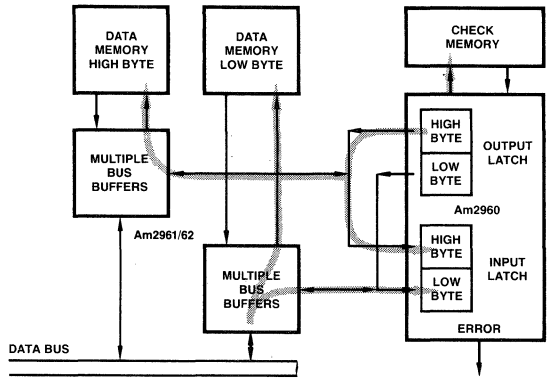


Figure 14. Byte Write, Phase 2: Insert the New Byte, Generate Checks and Write Into Memory

Diagnostics

EDC is used to boost the reliability of the overall system. It is necessary to also be able to check the operation of the EDC itself. For this reason the EDC has an internal control mode, a diagnostic latch, and two diagnostic modes.

To check that the EDC is functioning properly, the processor can put the EDC under software control by setting CODE ID_{2-0} to 001. This puts the EDC into Internal Control Mode. In Internal Control Mode the EDC is controlled by the contents of the Diagnostic Latch which is loaded from the DATA inputs under processor control.

The EDC is set into CORRECT Mode. The processor loads in a known set of check bits into the Diagnostic Latch, a known set of data bits into the Data In Latch, and forces data errors. The output of the EDC (syndromes, error flags, corrected data) is then compared against the expected responses. By exercising the EDC with a string of data/check combinations and comparing the output against the expected responses, the EDC can be fully checked out.

Eight Bit Data Word

Eight bit MOS microprocessors can use EDC too. Only five check bits are required. The EDC configuration for eight bits is shown in Figure 15. It operates as does the normal 16-bit configuration with the upper byte fixed at 0.

Check bit overhead for 8-bit data words can be reduced two ways. See the sections "Single Error Correction Only" and "Reducing Check Bit Overhead."

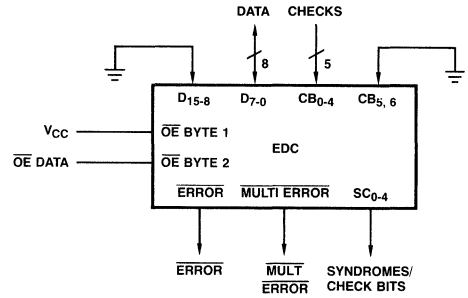


Figure 15. 8-Bit Configuration

Other Word Widths

EDC on data words other than 8, 16, 32, of 64 bits can be accomplished with the Am2960. In most cases the extra data bits can be forced to a constant, and EDC will procede as normal. For example a 24-bit data word is shown in Figure 16.

Single Error Correction Only

The EDC normally corrects all single bit errors *and* detects all double bit and some triple bit errors. To save one check bit per word the ability to detect double bit errors can be sacrificed – single errors are still detected and corrected.

Data Bits	Check Bits Required	
	Single Error Correction Only	Single Error Correct & Double Error Detect
8	4	5
16	5	6
32	6	7
64	7	8

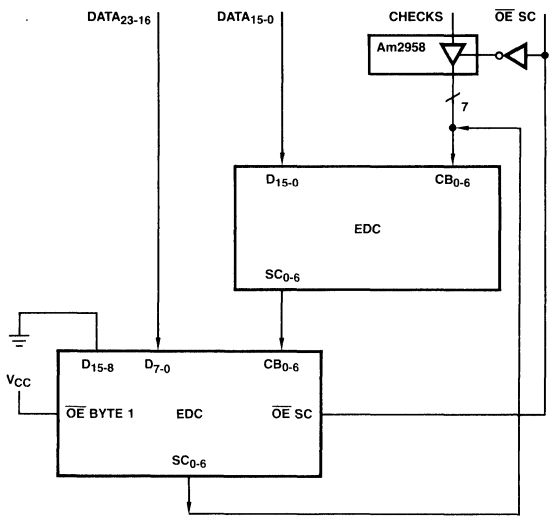


Figure 16. 24-Bit Configuration

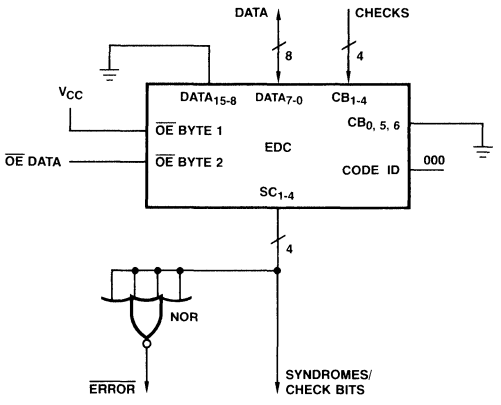


Figure 17. 8-Bit Single Error Correction Only

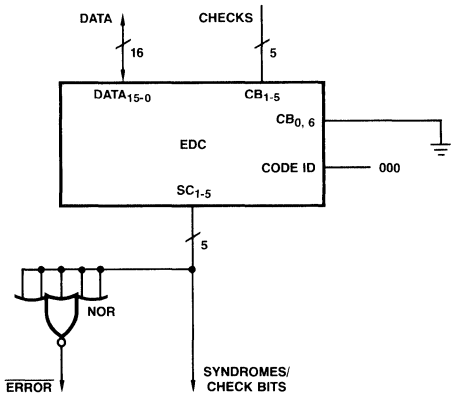
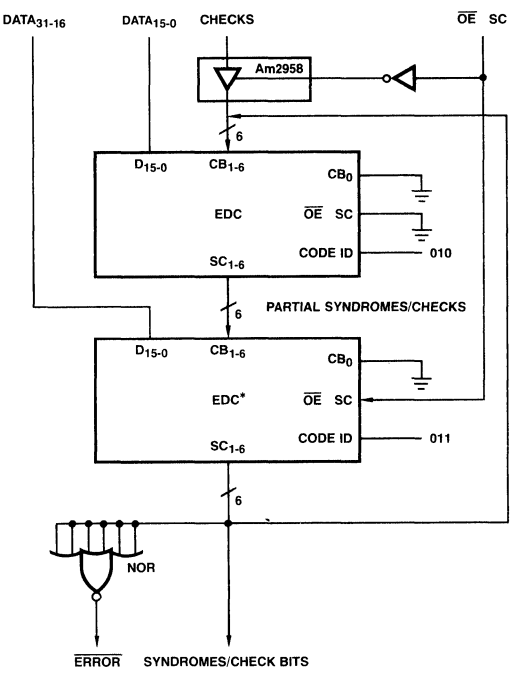


Figure 18. 16-Bit Single Error Correction Only



*The Code ID Combination for this Slice Forces the Check Bit Latch Transparent.

Figure 19. 32-Bit Single Correct Only

Figures 17, 18, 19, 20 show single error correction only configurations for 8, 16, 32, and 64-bit data words respectively.

Check Bit Correction

The EDC detects single bit errors whether the error is a data bit or a check bit. Data bit errors are automatically corrected by the EDC. To generate corrected check bits once a single check bit error is detected, the EDC need only be switched to GENERATE mode (data in the DATA INPUT LATCH is valid).

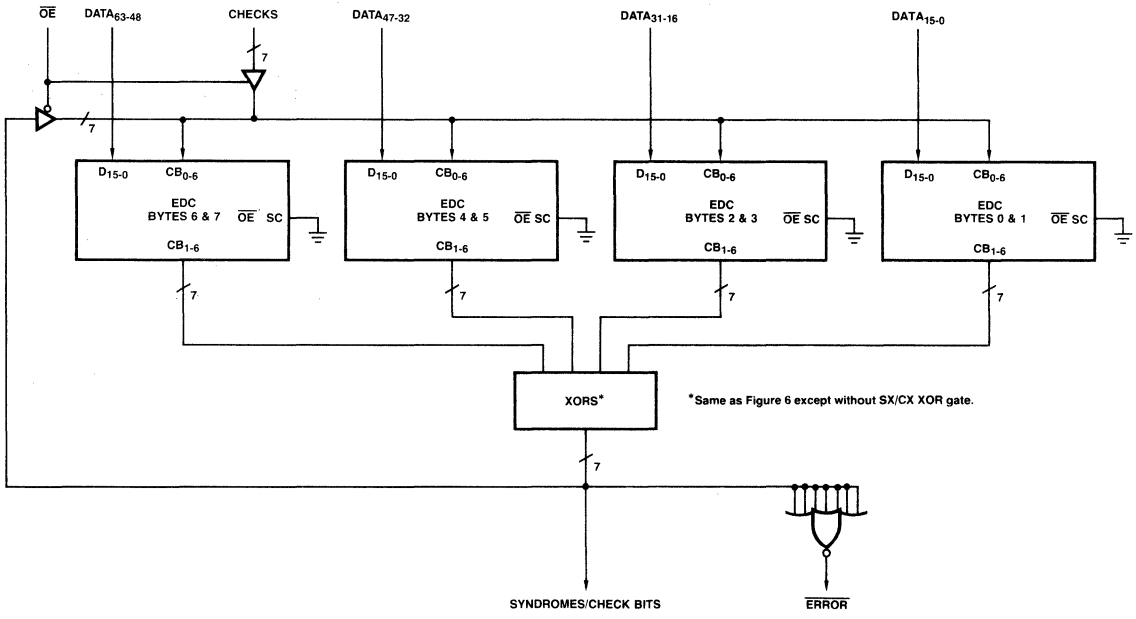
The syndromes generated by the EDC may be decoded to determine whether the single bit error is a check bit.

In many memory systems, a check bit error will be ignored on the memory read and corrected during a periodic "scrubbing" of memory (see section in System Design Considerations).

Multiple Errors

The bit-in-error decode logic uses syndrome bits S0 through S32 to correct errors, SX is only used in developing the multiple error signal. This means that some multiple errors will cause a data bit to be inverted.

For example, in the 16-bit mode if data bits 8 and 13 are in error the syndrome 111100 (SX, S0, S1, S2, S4, S8) is produced. This is flagged a double error by the error detection logic, but the bit-in-error decoder only receives syndrome 11100 (S0, S1, S2, S4, S8) which it decodes as a single error in data bit 0 and inverts that bit. If it is desired to inhibit this inversion, the multiple error output may be connected to the correct input as in Figure 21. This will inhibit correction when a multiple error occurs. Extra time delay may be introduced in the data to correct data path when this is done.



Notes: 1. In Pass Thru Mode the Contents of the Check Latch Appear on the XOR Outputs Inverted.
2. In Diagnostic Generate Mode the Contents of the Diagnostic Latch appear on the XOR Outputs Inverted.

Figure 20. 64-Bit Single Correct Only

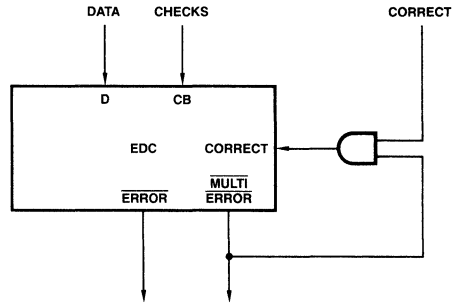


Figure 21. Inhibition of Data Modification

SYSTEM DESIGN CONSIDERATIONS

High Performance Parallel Operation

For maximum memory system performance the EDC should be used in the Check-Only configuration shown in Figure 22. With this configuration the memory system operates as fast with EDC as it would without.

On reads from memory, data is read out from the RAMs directly to the data bus (same as in a non-EDC system). At the same time, the data is read into the EDC to check for errors. If an error exists the EDC's error flags are used to interrupt the CPU and/or to stretch the memory cycle. If no error is detected, no slowdown is required.

If an error is detected, the EDC generates corrected data for the processor. At the designer's option the correct data may be written back into memory; error logging and diagnostic routines may also be run under processor control.

The Check-Only configuration allows data reads to proceed as fast with EDC as without. Only if an error is detected is there any slowdown. But even if the memory system had an error every hour this would mean only one error every 3-4 *billion* memory cycles. So even with a very high error rate, EDC in a Check-Only configuration has essentially zero impact on memory system speed.

On writes to memory, check bits must be generated before the full memory word can be written into memory. But using the Am2961/62 Data Bus Buffers allows the data word to be buffered on the memory board while check bits are generated. This makes the check bit generate time transparent to the processor.

EDC in the Data Path

The simplest configuration for EDC is to have the EDC directly in the data path as shown in Figure 23 (Correct-Always Configuration). In this configuration data read from memory is always corrected prior to putting the data on the data bus. The advantages are simpler operation and no need for mid-cycle interrupts. The disadvantage is that memory system speed is slowed by the amount of time it takes for error correction on ever cycle.

Usually the Correct-Always Configuration will be used with MOS microprocessors which have ample memory timing budgets. Most high performance processors will use the high performance parallel configuration shown in Figure 22. (Check-Only Configuration).

Scrubbing Avoids Double Errors

Single-bit errors are by far the most common in a memory system and are always correctable by the EDC.

Double bit memory errors are far less frequent than single bit (50 to 1, or 100 to 1) and are always detected by the EDC but not corrected.

In a memory system, soft errors occur only one at a time. A double bit error in a data word occurs when a single soft error is left uncorrected and is followed by another error in the data word hours, days, or weeks after the first.

"Scrubbing" memory periodically avoids almost all double-bit errors. In the scrubbing operation, every data word in memory is periodically checked by the EDC for single-bit errors. If one is found, it is corrected and the data word written back into memory. Errors are not allowed to pile up and so most double-bit errors are avoided.

The scrubbing operation is generally done as a background routine when the memory is not being used by the processor.

If memory is scrubbed frequently, errors that are detected and corrected during processor accesses need not be immediately written back into memory. Instead the error will be corrected in memory during scrubbing. This reduces the time delay involved in a processor access of an incorrect memory word.

Correction of Double-Bit Errors

In some cases, double-bit memory errors can be corrected! This is possible when one of the two bit errors is a hard error.

When a double bit error is detected the data word should be checked to determine if one of the errors is a hard error. If so the

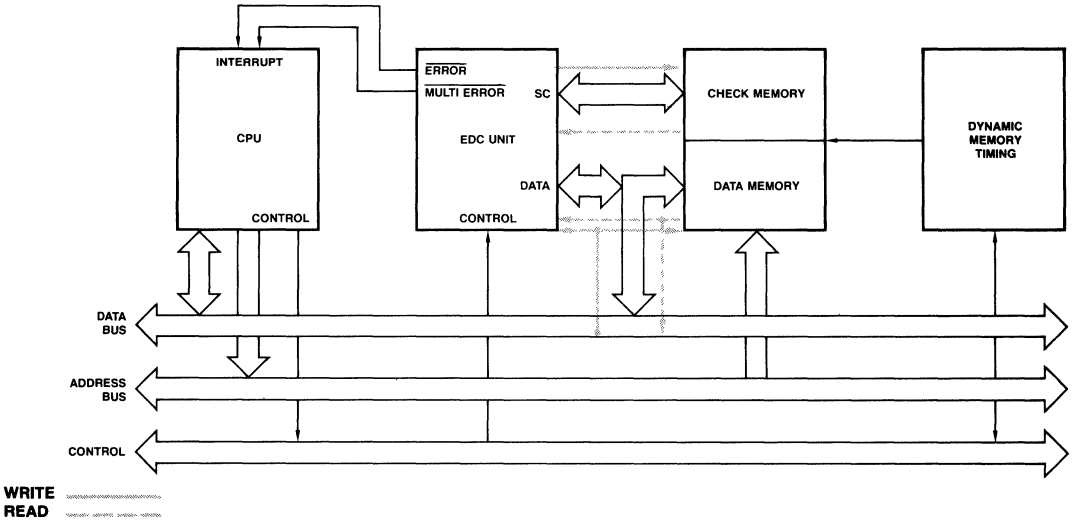


Figure 22. Check-Only Configuration

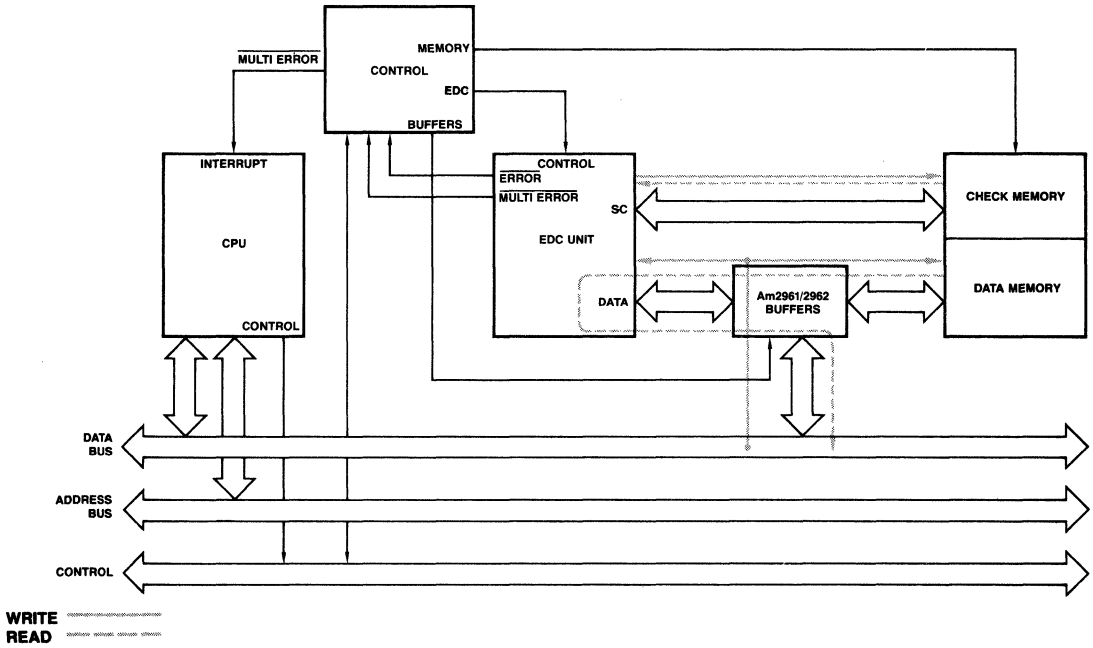


Figure 23. Correct-Always Configuration

hard error bit may be corrected by inverting it leaving only a single, correctable error. The time for this operation is negligible since it will occur infrequently.

The procedure after detection of a double error is as follows:

- Invert the data bits read from memory.
- Write the inverted data back into the same memory word.
- Re-read the memory location and XOR the newly read out value with the old. If there is no hard error then the XOR result will be all 1's. If there is a hard error, it will have the same bit value regardless of what was written in. So it will show as a 0 after the XOR operation
- Invert the hard error bit (this will "correct" it) leaving only one error in the data.
- The EDC can then correct the single bit error.
- Rewrite the correct data word into memory. This does not change the hard error but does eliminate the soft error. So the next memory access will find only a single-bit, correctable error.

An example helps to illustrate the procedure:

Example of Double Bit Error Correction When One is a Hard Error

1)	Data Read from Memory (D_1)	1111111100000011	011010
2)	EDC detects a multiple error. Syndromes:		011000
3)	Syndrome decode indicates a double bit error.		
4)	Invert the bits read from memory (D_1)	0000000011111100	100101
5)	Write D_1 back to the same memory location		
6)	Read back the memory location (D_2)	0000000011111101	100101
7)	XOR D_1 and D_2	1111111111111110	111111
8)	So the last data bit is the hard error. Use this to modify D_1	1111111100000010	011010
9)	Pass the modified D_1 through the EDC. The EDC detects a single bit correctable error and outputs corrected data:	1111111100000000	011010
10)	Write the corrected data back to memory to fix the soft error.		

Error Logging and Preventative Maintenance

The effectiveness of preventative maintenance can be increased by logging information on errors detected by the EDC. This is called error logging.

The EDC provides syndromes when errors are detected. The syndromes indicate which bit is in error. In most memory systems, each individual RAM supplies only one bit of the memory word. So the syndrome and data word address specify which RAM was in error.

Typically a permanent/hard RAM failure is preceded by a period of time where the RAM displays an increasing frequency of intermittent, soft errors. Error logging statistic can be used to detect an increasing intermittent error frequency so that the RAM can be replaced before a permanent failure occurs.

Error logging also records the location of already hard failed RAMs. With EDC a hard failure will not halt system operation. EDC always can correct single bit errors even if it is a hard error. EDC can also correct double bit errors where one is hard and one soft (see "Correction of Double Bit Errors" Section). The ability to continue operation despite hard errors can greatly reduce the need for emergency field maintenance. The hard-failed RAMs can be instead replaced at low cost during a regularly scheduled preventative maintenance session.

Reducing Check Bit Overhead

Memory word widths need not be the same as the data word width of the processor. There is a substantial reduction in check bit overhead if wider memory words are used:

Memory Word		Check Bit Overhead
# Data Bits	# Check Bits	
8	5	38%
16	6	27%
32	7	14%
64	8	11%

This reduction in check bit overhead lowers cost and increases the amount of data that can be packed on to each board.

The trade off is that when writing data pieces into memory that are narrower than the memory word width, more steps are required. These steps are exactly the same as those described in Byte Write in the Applications section. No penalty exists for reads from memory.

EDC Per Board vs EDC Per System

The choice of an EDC per system or per board depends on the economics and the architecture of the system.

Certainly the cheaper approach is to have only one EDC per system and this is a viable solution if only one memory location is accessed at at time.

This solution does require that the system has both data and check bit lines (see Figure 25). This makes retrofitting a system difficult and creates complications if static or ROM memory, which do not require check bits, are mixed in with dynamic RAM.

If the system has an advanced architecture it is quite likely that it is necessary to simultaneously access memory locations on different memory boards (see Figure 24). Architectural features that require this are interleaved memory, cache memory, and DMA that is done simultaneously with processor memory accesses. EDC per board is a simpler system from a design standpoint.

The EDC is designed to work efficiently in either the per system or per board configurations.

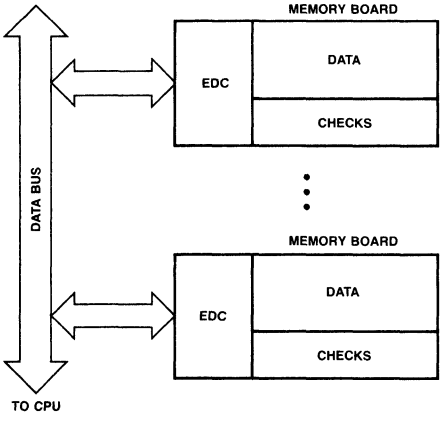


Figure 24. EDC Per Board

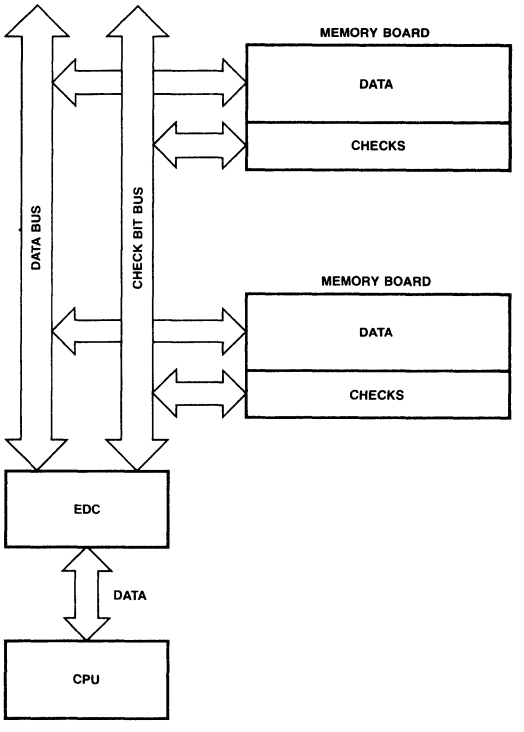


Figure 25. EDC Per System

FUNCTIONAL EQUATIONS

The following equations and tables describe in detail how the output values of the Am2960 EDC are determined as a function of the value of the inputs and the internal states. Be sure to carefully read the following definitions of symbols before examining the tables.

Definitions

D_i ← ($DATA_i$ if LE IN is HIGH or the output of bit i of the Data Input Latch if LE IN is LOW)
C_i ← (CB_i if LE IN is HIGH or the output of bit i of the Check Bit Latch if LE IN is LOW)
DL_i ← Output of bit i of the Diagnostic Latch
S_i ← Internally generated syndromes (same as outputs of SC_i if outputs enabled)
PA ← D0 ⊕ D1 ⊕ D2 ⊕ D4 ⊕ D6 ⊕ D8 ⊕ D10 ⊕ D12
PB ← D0 ⊕ D1 ⊕ D2 ⊕ D3 ⊕ D4 ⊕ D5 ⊕ D6 ⊕ D7
PC ← D8 ⊕ D9 ⊕ D10 ⊕ D11 ⊕ D12 ⊕ D13 ⊕ D14 ⊕ D15
PD ← D0 ⊕ D3 ⊕ D4 ⊕ D7 ⊕ D9 ⊕ D10 ⊕ D13 ⊕ D15
PE ← D0 ⊕ D1 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D11 ⊕ D12 ⊕ D13
PF ← D2 ⊕ D3 ⊕ D4 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D14 ⊕ D15
PG_1 ← D0 ⊕ D4 ⊕ D6 ⊕ D7
PG_2 ← D1 ⊕ D2 ⊕ D3 ⊕ D5
PG_3 ← D8 ⊕ D9 ⊕ D11 ⊕ D14
PG_4 ← D10 ⊕ D12 ⊕ D13 ⊕ D15

Error Signals

$$\overline{ERROR} \leftarrow (\overline{S6 \cdot (ID_1 + ID_2)}) \cdot \overline{S5} \cdot \overline{S4} \cdot \overline{S3} \cdot \overline{S2} \cdot \overline{S1} \cdot \overline{S0} + GENERATE + INITIALIZE + PASSTHRU$$

$$\overline{MULT\ ERROR}\ (16\text{ and }32\text{-Bit Modes}) \leftarrow \overline{((S6 \cdot ID_1) \oplus S5 \oplus S4 \oplus S3 \oplus S2 \oplus S1 \oplus S0)}\ (\overline{ERROR}) + TOME + GENERATE + PASSTHRU + INITIALIZE$$

$$\overline{MULT\ ERROR}\ (64\text{-Bit Modes}) \leftarrow TOME + GENERATE + PASSTHRU + INITIALIZE$$

TOME (Three or More Errors)*

S1	S2	S3	S0	**S6	S5	S4
			0	0	0	0
			1	0	0	0
			0	1	0	0
			1	1	0	0
			0	0	1	0
			1	0	1	0
			0	1	1	0
			1	1	1	0
			0	0	0	1
			1	0	0	1
			0	1	0	1
			1	1	0	1
			0	0	1	1
			1	0	1	1
			0	1	1	1
			1	1	1	1
0	0	0	0	0	0	0
0	0	1	0	1	1	1
0	1	0	0	1	1	1
0	1	1	1	1	1	1
1	0	0	0	1	1	1
1	0	1	0	0	0	0
1	1	0	1	1	1	1
1	1	1	0	0	0	0

S1	S2	S3	S0	**S6	S5	S4
			1	0	1	0
			0	1	1	0
			1	1	1	0
			0	0	0	1
			1	0	0	1
			0	1	0	1
			1	1	0	1
			0	0	1	1
			1	0	1	1
			0	1	1	1
			1	1	1	1
0	0	0	1	1	1	1
0	0	1	1	0	0	0
0	1	0	1	0	0	0
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	0	1	1	1	1	1
1	1	0	0	0	0	0
1	1	1	1	1	1	1

*S6, S5, . . . S0 are internal syndromes except in Modes 010, 100, 101, 110, 111 (CODE ID_2, ID_1, ID_0). In these modes the syndromes are input over the Check-Bit lines. S6 ← C6, S5 ← C5, . . . S1 ← C1, S0 ← C0.

**The S6 internal syndrome is always forced to 0 in CODE ID 000.

SC Outputs

Tables XV, XVI, XVII, XVIII, XIX show how outputs SC_{0-6} are generated in each control mode for various CODE IDs (internal control mode not applicable).

TABLE XV.

GENERATE Mode (Check Bits) \ CODE ID_{2-0}	000	010	011	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_3$	$PG_2 \oplus PG_4$	$PG_2 \oplus PG_3$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	PA	PA	PA	PA	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD}$	$\overline{PD}$	PD	$\overline{PD}$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE}$	$\overline{PE}$	PE	$\overline{PE}$	PE	PE	PE
$SC_4 \leftarrow$	PF	PF	PF	PF	PF	PF	PF
$SC_5 \leftarrow$	PC	PC	PC	PC	PC	PC	PC
$SC_6 \leftarrow$	1	PB	PC	PB	PB	PB	PB

TABLE XVI.

Detect and Correct Modes (Syndromes) \ CODE ID_{2-0}	000	010	011*	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3 \oplus C0$	$PG_1 \oplus PG_3 \oplus C0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus C0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	$PA \oplus C1$	$PA \oplus C1$	$PA \oplus CB_1$	$PA \oplus C1$	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD} \oplus C2$	$\overline{PD} \oplus C2$	$PD \oplus CB_2$	$\overline{PD} \oplus C2$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE} \oplus C3$	$\overline{PE} \oplus C3$	$PE \oplus CB_3$	$\overline{PE} \oplus C3$	PE	PE	PE
$SC_4 \leftarrow$	$PF \oplus C4$	$PF \oplus C4$	$PF \oplus CB_4$	$PF \oplus C4$	PF	PF	PF
$SC_5 \leftarrow$	$PC \oplus C5$	$PC \oplus C5$	$PC \oplus CB_5$	$PC \oplus C5$	PC	PC	PC
$SC_6 \leftarrow$	1	$PB \oplus C6$	$PC \oplus CB_6$	PB	PB	$PB \oplus C6$	$PB \oplus C6$

*In CODE ID_{2-0} 011 the Check-Bit Latch is forced transparent, the Data Latch operates normally.

TABLE XVII.

Diagnostic Read Mode \ CODE ID_{2-0}	000	010	011*	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_1 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	$PA \oplus DL_1$	$PA \oplus DL_1$	$PA \oplus CB_1$	$PA \oplus DL_1$	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD} \oplus DL_2$	$\overline{PD} \oplus DL_2$	$PD \oplus CB_2$	$\overline{PD} \oplus DL_2$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE} \oplus DL_3$	$\overline{PE} \oplus DL_3$	$PE \oplus CB_3$	$\overline{PE} \oplus DL_3$	PE	PE	PE
$SC_4 \leftarrow$	$PF \oplus DL_4$	$PF \oplus DL_4$	$PF \oplus CB_4$	$PF \oplus DL_4$	PF	PF	PF
$SC_5 \leftarrow$	$PC \oplus DL_5$	$PC \oplus DL_5$	$PC \oplus CB_5$	$PC \oplus DL_5$	PC	PC	PC
$SC_6 \leftarrow$	1	$PB \oplus DL_6$	$PC \oplus CB_6$	PB	PB	$PB \oplus DL_6$	$PB \oplus DL_7$

*In CODE ID_{2-0} 011 the Check-Bit Latch is forced transparent, the Data Latch operates normally.

TABLE XVIII.

Diagnostic Write Mode \ CODE ID_{2-0}	000	010	011*	100	101	110	111
$SC_0 \leftarrow$	DL_0	DL_0	CB_0	DL_0	1	1	1
$SC_1 \leftarrow$	DL_1	DL_1	CB_1	DL_1	1	1	1
$SC_2 \leftarrow$	DL_2	DL_2	CB_2	DL_2	1	1	1
$SC_3 \leftarrow$	DL_3	DL_3	CB_3	DL_3	1	1	1
$SC_4 \leftarrow$	DL_4	DL_4	CB_4	DL_4	1	1	1
$SC_5 \leftarrow$	DL_5	DL_5	CB_5	DL_5	1	1	1
$SC_6 \leftarrow$	1	DL_6	CB_6	1	1	DL_6	DL_7

*In CODE ID_{2-0} 011 the Check-Bit Latch is forced transparent; the Data Input Latch operates normally.

TABLE XIX.

PASS THRU Mode \ CODE ID_{2-0}	000	010	011*	100	101	110	111
$SC_0 \leftarrow$	C0	C0	CB_0	C0	1	1	1
$SC_1 \leftarrow$	C1	C1	CB_1	C1	1	1	1
$SC_2 \leftarrow$	C2	C2	CB_2	C2	1	1	1
$SC_3 \leftarrow$	C3	C3	CB_3	C_3	1	1	1
$SC_4 \leftarrow$	C4	C4	CB_4	C4	1	1	1
$SC_5 \leftarrow$	C5	C5	CB_5	C5	1	1	1
$SC_6 \leftarrow$	1	C6	CB_6	1	1	C6	C6

*In CODE ID_{2-0} 011 the Check-Bit Latch is forced transparent; the Data Input Latch operates normally.

Data Correction

Tables XX to XXVI shows which data output bits are corrected (inverted) depending upon the syndromes and the CODE ID position. Note that the syndromes that determine data correction are in some cases syndromes input externally via the CB inputs and in some cases syndromes generated internally by that EDC (S_i are the internal syndromes and are the same as the value of the SC_i output of that EDC if enabled).

The tables show the number of data bit inverted (corrected) if any for the CODE ID and syndrome combination.

TABLE XX. CODE ID_{2-0} = 000*

S2	S1 \ S5	S4	S3	0	0	0	0	1	1	1	1
				0	0	1	1	0	0	1	1
				0	1	0	1	0	1	0	1
0	0			–	–	–	5	–	11	14	–
0	1			–	1	2	6	8	12	–	–
1	0			–	–	3	7	9	13	15	–
1	1			–	0	4	–	10	–	–	–

*Unlisted S combinations are no correction.

TABLE XXI. CODE ID_{2-0} = 010*

CB_2	CB_1 \ CB_6	CB_5	CB_4	CB_3	0	0	0	0	1	1	1	1
					1	1	1	1	0	0	0	0
					0	0	1	1	0	0	1	1
					0	1	0	1	0	1	0	1
0	0				–	11	14	–	–	–	–	5
0	1				8	12	–	–	–	1	2	6
1	0				9	13	15	–	–	–	3	7
1	1				10	–	–	–	–	0	4	–

*Unlisted CB combinations are no correction.

TABLE XXII. CODE ID_{2-0} = 011*

	S6	0	0	0	0	1	1	1	1
	S5	0	0	0	0	1	1	1	1
	S4	0	0	1	1	0	0	1	1
	S3	0	1	0	1	0	1	0	1
S2	S1								
0	0	–	–	–	5	–	11	14	–
0	1	–	1	2	6	8	12	–	–
1	0	–	–	3	7	9	13	15	–
1	1	–	0	4	–	10	–	–	–

*Unlisted S combinations are no correction.

TABLE XXIII. CODE ID_{2-0} = 100*

	CB_0	0	0	0	0	1	1	1	1
	CB_6	0	0	0	0	1	1	1	1
	CB_5	1	1	1	1	0	0	0	0
	CB_4	0	0	1	1	0	0	1	1
	CB_3	0	1	0	1	0	1	0	1
CB_2	CB_1								
0	0	–	11	14	–	–	–	–	5
0	1	8	12	–	–	–	1	2	6
1	0	9	13	15	–	–	–	3	7
1	1	10	–	–	–	–	0	4	–

*Unlisted CB combinations are no correction

TABLE XXIV. CODE ID_{2-0} = 101*

	CB_0	0	0	0	0	1	1	1	1
	CB_6	0	0	0	0	1	1	1	1
	CB_5	0	0	0	0	1	1	1	1
	CB_4	0	0	1	1	0	0	1	1
	CB_3	0	1	0	1	0	1	0	1
CB_2	CB_1								
0	0	–	–	–	5	–	11	14	–
0	1	–	1	2	6	8	12	–	–
1	0	–	–	3	7	9	13	15	–
1	1	–	0	4	–	10	–	–	–

*Unlisted CB combinations are no correction.

TABLE XXV. CODE ID_{2-0} = 110*

	CB_0	0	0	0	0	1	1	1	1
	CB_6	1	1	1	1	0	0	0	0
	CB_5	0	0	0	0	1	1	1	1
	CB_4	0	0	1	1	0	0	1	1
	CB_3	0	1	0	1	0	1	0	1
CB_2	CB_1								
0	0	–	–	–	5	–	11	14	–
0	1	–	1	2	6	8	12	–	–
1	0	–	–	3	7	9	13	15	–
1	1	–	0	4	–	10	–	–	–

*Unlisted CB combinations are no correction.

TABLE XXVI. CODE ID_{2-0} = 111*

	CB_0	0	0	0	0	1	1	1	1
	CB_6	1	1	1	1	0	0	0	0
	CB_5	1	1	1	1	0	0	0	0
	CB_4	0	0	1	1	0	0	1	1
	CB_3	0	1	0	1	0	1	0	1
CB_2	CB_1								
0	0	–	11	14	–	–	–	–	5
0	1	8	12	–	–	–	1	2	6
1	0	9	13	15	–	–	–	3	7
1	1	10	–	–	–	–	0	4	–

*Unlisted CB combinations are no correction.

ADVANCED MICRO DEVICES

TECHNICAL REPORT

Am2960 BOOSTS MEMORY RELIABILITY

ABSTRACT

Memory error frequency will increase due to the use of larger memory systems and the use of 16K and 64K RAMs, which are more susceptible to soft errors because of their smaller memory cell geometry.

At the same time, the need for reliability is increasing, both for the user and the system manufacturer. EDC (Error Detection and Correction) can reduce system downtime, can reduce field maintenance expenses and can provide manufacturers a marketing advantage due to increased reliability.

The Am2960 implements EDC using a modified Hamming code, and so boosts memory reliability by a factor of 60 or better. It slashes package count and adds initialization, byte-write and diagnostic features. It is fast and flexible enough to handle word widths from 8 to 64 bits.

The Am2960 is one of a series of Memory Support devices designed for use with dynamic MOS RAM memory systems.

Prepared by: Advanced Micro Devices, Bipolar Microprocessor.

Am2960 BOOSTS MEMORY RELIABILITY

The Am2960 is a 16-bit, expandable Error Detection and Correction (EDC) unit. It is used in conjunction with system main memories to boost memory reliability.

The Am2960 can correct *all* single-bit memory errors in a data word. It detects all double-bit errors and even some triple-bit errors. The gross error conditions of all 0s or all 1s are always detected.

Memory error and detection using the Am2960 boosts system reliability by a factor of 60 or better. System crashes will occur far less frequently and maintenance costs can be slashed.

MEMORY ERRORS

Memory Error Frequency

Memory errors are becoming *more* frequent due to two general trends:

1. Total system memory size is growing, and,
2. The geometry of individual memory cells in dynamic RAMs is shrinking, making them more susceptible to "soft" errors.

There are two basic types of memory errors. Hard errors are permanent physical failures of either the whole RAM, a row, a column, or a single bit. Hard errors are caused by power shorts, open leads, and various other factors. Initial testing and burn-in will reduce but not eliminate hard error failures in RAMs during system operation.

Soft errors are non-repeating, single-bit errors where there is no permanent damage. A soft error occurs when the charge state of a bit incorrectly shifts from 0 to 1 or from 1 to 0. This can be caused by system noise, pattern sensitivity, power surges[6] or alpha particles. The new 16K and 64K dynamic RAMs, with their smaller memory cell geometries are especially susceptible to soft errors induced by alpha particles. (The smaller the memory cell geometry, the less energy is required to cause the cell to change state.)

A paper given at Wescon, 1979[1] presented these failure rates for dynamic RAMs of increasing size (see Table 1). This table reflects only soft errors due to alpha particles.

Undetected Memory Failures are Expensive

Memory failures will occur in a system. When they do they will result either in a system crash or in loss of data integrity, unless memory error detection schemes are used. Either situation is expensive and inconvenient for the system users. Either situation can result in maintenance calls to the system manufacturer.

If the memory error occurs in an instruction word and the instruction is executed without being corrected, then a system crash will almost certainly occur. For example, an "Add" instruction could be changed to a "Jump" instruction with only a one-bit change – if the error is undetected, the jump would take place to essentially a random location.

If the error occurs in a word that is used for storing data, then data integrity is lost. In typical applications this could mean that bank account balances would be altered, blood diagnosis would be incorrect, or cooling water valves could be closed instead of opened.

System failures of any kind will often result in unscheduled maintenance requests to the system manufacturers. Maintenance calls are expensive for the system manufacturer and are to be avoided by preventative means if at all possible.

Strategies for Memory Errors

For reliability and maintenance cost reduction, memory errors must be dealt with by the system designer.

A common scheme is to use parity. But parity schemes cannot correct errors and can detect only single-bit errors. If a double-bit error occurs in a word, the parity is unchanged and so the error goes undetected. Parity cannot correct errors.

Error detection and correction (EDC) is implemented by the Am2960 using a modified Hamming code. The Hamming code scheme involves generating several check bits that contain enough redundant information to correct *all* single-bit errors and to detect all double-bit errors and some triple-bit errors. Also, the EDC modified Hamming code detects the gross error conditions of all 0s and all 1s.

Table 2 demonstrates that EDC is the superior strategy for both the system user and the system manufacturer.

TABLE 1. ERRORS ARE INCREASING.

Density Bits/Chip	Typical Error Rate (% per 1,000 Hours)	
	Soft*	Hard**
1K	.001	.0001
4K	.02	.002
16K	.10	.011
64K	.5***	.016

*Reflects alpha particles only. Does not include errors due to noise, power, patterns.
**After infant mortality.
***Based on initial customer evaluation.
Note: 0.1% per 1000 hours equals 1 failure in 10^6 hours.

TABLE 2. COMPARISON OF ERROR STRATEGIES.

Error Type	No Checking	Parity	EDC Using Am2960
Single-Bit Error	System crash.	System halt.	Correctable. System runs.
Double-Bit Error	System crash.	System crash.	System halt.
Entire RAM Failure	System crash.	System halt.	Correctable. System runs.

With EDC, the incidence of maintenance calls is significantly reduced. Even the failure of an entire RAM chip will not necessarily result in a system failure. Double-bit errors are not corrected but are detected so that the system may be halted and the user informed of a memory error and the exact location of it. A controlled system halt is far more desirable than an uncontrolled system crash.

EDC Improves MTTF

Error detection and correction as implemented on the Am2960 significantly improves the MTTF (mean time to failure) of memory systems.

A paper presented at Wescon, 1979[1] used the dynamic RAM error rates shown previously to calculate the following MTTFs for a 16 Megabyte system using 64K RAMs (see Table 3).

TABLE 3.

Error Type	MTTF*
Correctable Soft Error (Single-Bit)	13 days
Correctable Hard Error (Single-Bit)	110 days
Non-Correctable Soft Error (Double-Bit)	864 days
Non-Correctable Hard Error (Double-Bit)	7,021 days

*Based on 64K RAM alpha error rate of 0.13% per 1000 hours.

The MTTF improves by a factor of at least 60 with EDC. This improvement factor has been noted by others[2].

Another paper [3,4] calculated that with EDC, RAM errors would become a small factor in memory based failures relative to failures of other board components such as MSI, capacitors and resistors. The same paper[4] discusses how frequently preventative maintenance should be done so that a hard-failed RAM is replaced prior to a second RAM experiencing a hard-failure. The Am2960 has features that allow easy logging of data errors – this aids the maintenance engineer in quickly pinpointing hard-failed RAMs and RAMs displaying excessive soft error rates.

Memory Reliability is a Competitive Edge

EDC boosts memory reliability and gives you two competitive advantages:

1. Your system is more reliable.
2. Your field maintenance costs are reduced.

The demand for reliable system performance is increasing steadily. Reliability is a must for applications in aerospace, medical, banking, process control and on-line systems. Applications such as word-processors, small business systems and telecommunications also need memory reliability, as their users do not have the technical staff to handle system failures and are willing to pay for the convenience of smooth, error-free operation.

REFERENCES

1. Eric C. Westerfield, Four-Phase Systems, "Memory System Strategies for Soft and Hard Errors," Wescon, September, 1979.
2. "As Memory Density Quadruples Again, Designers Focus on Reliability," Electronic Design, January 18, 1979.
3. Robert Koppel, "RAM Reliability in Large Memory Systems – Significance of Predicting MTBF," Computer Design, February, 1979.
4. Robert Koppel, "RAM Reliability in Large Memory Systems – Improving MTBF with ECC," Computer Design, March, 1979.
5. A.V. Ferris-Prabhu, IBM General Technology Division, "Improving Memory Reliability Through Error Correction," Computer Design, July, 1979.
6. "Power-Line Disturbances Scorecard," Electronic Design, February 15, 1979.
7. "Alphas Stymie Statics," Electronics, March 15, 1979.
8. "Analyzing Computer Technology Costs," Computer Design, October, 1978.
9. "Alphas Cause Rift at ECC," Electronic Engineering Times, May 28, 1979.
10. Ernst L. Wall, ITT, "Applying the Hamming Code to Microprocessor-Based Systems," Electronics, November 22, 1979.

These devices are also characterized as:
AmZ8161
AmZ8162

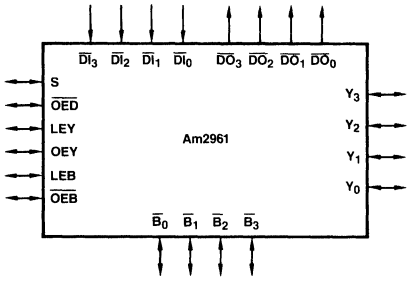
Am2961 • Am2962

4-Bit Error Correction Multiple Bus Buffers

DISTINCTIVE CHARACTERISTICS

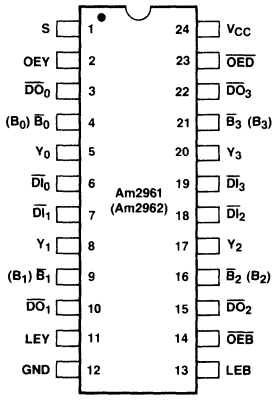
- Quad high-speed LSI bus-transceiver
- Provides complete data path interface between the Am2960 Error Detection and Correction Unit, the system data bus and dynamic RAM memory
- Three-state 24mA output to data bus
- Three-state data output to memory
- Inverting data bus for Am2961 and noninverting for Am2962
- Data bus latches allow operation with multiplexed buses
- Space saving 24-pin 0.3" package
- 100% MIL-STD-883 reliability assurance testing

LOGIC SYMBOL



B-Bus is noninverting for Am2962.

CONNECTION DIAGRAM
Top View



24 pin slim (0.3")

Note: Pin 1 is marked for orientation.

BLI-122

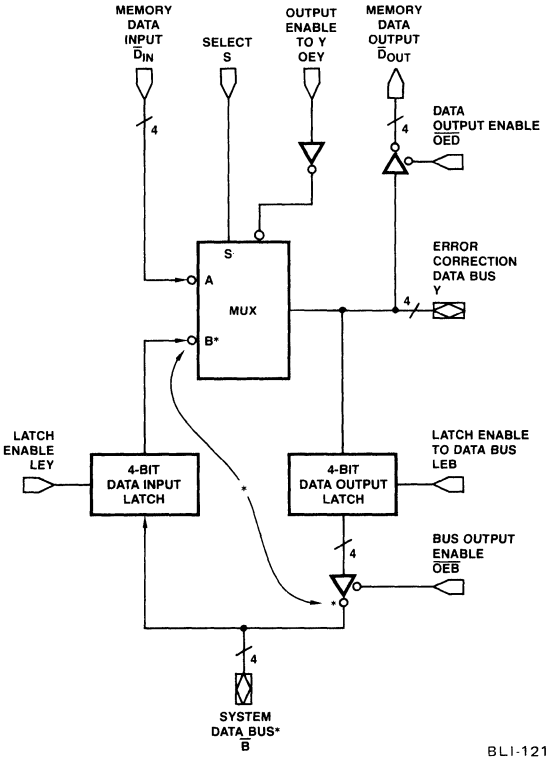
FUNCTIONAL DESCRIPTION

The Am2961 and Am2962 are high-performance, low-power Schottky multiple bus buffers that provide the complete data path interface between the Am2960 Error Detection and Correction Unit, dynamic RAM memory and the system data bus. The Am2961 provides an inverting data path between the data bus (B_i) and the Am2960 error correction data input (Y_i) and the Am2962 provides a noninverting configuration (B_i to Y_i). Both devices provide inverting data paths between the Am2960 and memory data bus thereby optimizing internal data path speeds.

The Am2961 and Am2962 are 4-bit devices. Four devices are used to interface each 16-bit Am2960 Error Detection and Correction Unit with dynamic memory. The system can easily be expanded to 32 or more bits for wider memory applications. The 4-bit configuration allows enabling the appropriate devices two-at-a-time for intermixed word or byte, read and write in 16-bit systems with error correction.

Data latches between the error correction data bus and the system data bus facilitate byte writing in memory systems wider than 8-bits. They also provide a data holding capability during single-step system operation.

LOGIC DIAGRAM



BLI-121

*Am2962 is the same function but noninverting to the system data bus, B.

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% (MIN = 4.75V MAX = 5.25V)

MIL T_A = −55 to +125°C V_{CC} = 5.0V ±10% (MIN = 4.50V MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE – Y BUS

Parameters	Description	Test Conditions (Note 1)			Min	Typ. (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.0mA		2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA			0.3	0.45	Volts
			I_{OL} = 16mA			0.35	0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		OEY = LOW			−2.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		OEY = LOW			100	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V		OEY = LOW			1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−130	mA

DC CHARACTERISTICS OVER OPERATING RANGE – B BUS

Parameters	Description	Test Conditions (Note 1)			Min	Typ. (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.0mA		2.4			Volts
			I_{OH} = −15mA		2.0			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA			0.3	0.45	Volts
			I_{OL} = 24mA			0.35	0.50	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		$\overline{OEB}$ = HIGH			−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		$\overline{OEB}$ = HIGH			100	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V		$\overline{OEB}$ = HIGH			1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−50		−150	mA

Notes: 1. For conditions as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

DC CHARACTERISTICS OVER OPERATING RANGE – DO OUTPUTS

Parameters	Description	Test Conditions (Note 1)		Min	Typ. (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL I_{OH} = −50μA	2.5			Volts
			COM'L I_{OH} = −100μA	2.7			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA			0.4	Volts
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−50		−150	mA
I_O	Off-State Out Current	V_{CC} = MAX	V_O = 0.4V			−100	μA
			V_O = 2.4V			+100	

DC CHARACTERISTICS OVER OPERATING RANGE – DI INPUTS AND CONTROLS

Parameters	Description	Test Conditions (Note 1)		Min	Typ. (Note 2)	Max	Units
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_C	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	DI Inputs			−1.0	mA
			Controls			−1.6	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA

DC CHARACTERISTICS OVER OPERATING RANGE – POWER SUPPLY

Parameters	Description	Test Conditions (Note 1)	Min	Typ. (Note 2)	Max	Units
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX		110	155	mA

Note 4:

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} MAX
DC Input Voltage	5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

Am2961
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% Min	COM'L Max	MIL T = −55 to +125°C V_{CC} = 5.0V ±10% Min	MIL Max	Units	Test Conditions
t_{PLH}	Propagation Delay $\overline{B}$ to Y (Latch Transparent, OEY = LEY = HIGH)		25		28	ns	Figure 1 C_L = 50pF R_L = 390Ω R_2 = 1kΩ
t_{PHL}			25		28	ns	
t_{PLH}	Propagation Delay $\overline{DI}$ to Y (OEY = HIGH, S = LOW)		15		18	ns	
t_{PHL}			15		18	ns	
t_{PLH}	Propagation Delay S to Y (OEY = HIGH)		25		28	ns	
t_{PHL}			25		28	ns	
t_{PLH}	Propagation Delay LEY to Y (OEY = S = HIGH)		25		30	ns	
t_{PHL}			35		40	ns	
t_{PZH}	Y Bus Output Enable Time OEY to Y		18		21	ns	
t_{PZL}			18		21	ns	
t_{PHZ}	Y Bus Output Disable Time OEY to Y		18		21	ns	
t_{PLZ}			18		21	ns	
t_{PLH}	Propagation Delay LEB to $\overline{B}$ ($\overline{OEB}$ = LOW)		25		30	ns	Figure 1 C_L = 50pF R_L = 270Ω R_2 = 1kΩ
t_{PHL}			35		40	ns	
t_{PLH}	Propagation Delay Y to $\overline{B}$ (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)		18		21	ns	
t_{PHL}			20		23	ns	
t_{PLH}	Propagation Delay Y to $\overline{B}$ (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)		26		30	ns	Figure 1 C_L = 300pF R_L = 270Ω R_2 = 1kΩ
t_{PHL}			31		35	ns	
t_{PZH}	$\overline{B}$ Bus Output Enable Time $\overline{OEB}$ to $\overline{B}$		18		21	ns	Figure 1 C_L = 50pF R_L = 270Ω R_2 = 1kΩ
t_{PZL}			18		21	ns	
t_{PLZ}	$\overline{B}$ Bus Output Disable Time $\overline{OEB}$ to $\overline{B}$		18		21	ns	
t_{PHZ}			18		21	ns	
t_{PLH}	Propagation Delay Y to $\overline{DO}$ ($\overline{OED}$ = OEY = LOW)		15		18	ns	Figure 2 C_L = 50pF R = 2kΩ
t_{PHL}			20		23	ns	
t_{PZH}	$\overline{DO}$ Output Enable Time $\overline{OED}$ to $\overline{DO}$		28		30	ns	S = 2 — Figure 3 C_L = 50pF R = 680Ω
t_{PZL}			28		30	ns	S = 1
t_{PHZ}	$\overline{DO}$ Output Disable Time $\overline{OED}$ to $\overline{DO}$		16		18	ns	S = 2
t_{PLZ}			24		28	ns	S = 1
t_S	$\overline{B}$ to LEY Set-up Time ($\overline{OEB}$ = HIGH)	6		6		ns	Figure 1 C_L = 50pF R_L = 390Ω R_2 = 1kΩ
t_H	$\overline{B}$ to LEY Hold Time ($\overline{OEB}$ = HIGH)	9		10		ns	
t_S	Y to LEB Set-up Time (OEY = LOW)	6		6		ns	Figure 1 C_L = 50pF R_L = 270Ω R_2 = 1kΩ
t_H	Y to LEB Hold Time (OEY = LOW)	9		10		ns	

*AC perfomance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

SWITCHING TEST CIRCUITS

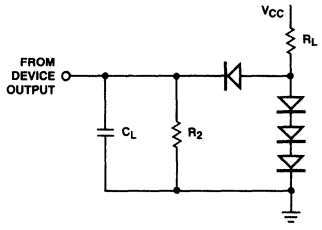


Figure 1.

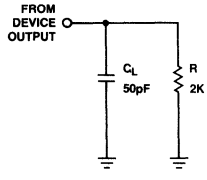


Figure 2.

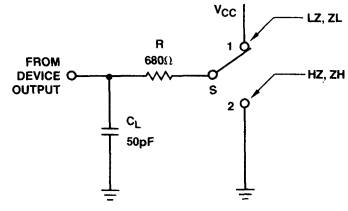


Figure 3.

Am2962
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ±5% Min	COM'L Max	MIL T = −55 to +125°C, V_{CC} = 5.0V ±10% Min	MIL Max	Units	Test Conditions
t_{PLH}	Propagation Delay B to Y (Latch Transparent, OEY = LEY = HIGH)		27		28	ns	Figure 1, C_L = 50pF, R_L = 390Ω, R_2 = 1kΩ
t_{PHL}			27		28	ns	
t_{PLH}	Propagation Delay $\overline{DI}$ to Y (OEY = HIGH, S = LOW)		15		18	ns	
t_{PHL}			15		18	ns	
t_{PLH}	Propagation Delay S to Y (OEY = HIGH)		25		28	ns	
t_{PHL}			25		28	ns	
t_{PLH}	Propagation Delay LEY to Y (OEY = S = HIGH)		25		30	ns	
t_{PHL}			35		40	ns	
t_{PZH}	Y Bus Output Enable Time OEY to Y		18		21	ns	
t_{PZL}			18		21	ns	
t_{PHZ}	Y Bus Output Disable Time OEY to Y		18		21	ns	
t_{PLZ}			18		21	ns	
t_{PLH}	Propagation Delay LEB to B ($\overline{OEB}$ = LOW)		25		30	ns	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ
t_{PHL}			35		40	ns	
t_{PLH}	Propagation Delay Y to B (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)		20		23	ns	
t_{PHL}			21		24	ns	
t_{PLH}	Propagation Delay Y to B (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)		28		32	ns	Figure 1, C_L = 300pF, R_L = 270Ω, R_2 = 1kΩ
t_{PHL}			32		36	ns	
t_{PZH}	B Bus Output Enable Time $\overline{OEB}$ to B		18		21	ns	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ
t_{PZL}			18		21	ns	
t_{PLZ}	B Bus Output Disable Time $\overline{OEB}$ to B		18		21	ns	
t_{PHZ}			18		21	ns	
t_{PLH}	Propagation Delay Y to $\overline{DO}$ ($\overline{OED}$ = OEY = LOW)		15		18	ns	Figure 2, C_L = 50pF, R = 2kΩ
t_{PHL}			20		23	ns	
t_{PZH}	$\overline{DO}$ Output Enable Time $\overline{OED}$ to $\overline{DO}$		28		30	ns	S = 2
t_{PZL}			28		30	ns	S = 1
t_{PHZ}	$\overline{DO}$ Output Disable Time $\overline{OED}$ to $\overline{DO}$		16		18	ns	S = 2
t_{PLZ}			24		28	ns	S = 1
							Figure 3, C_L = 50pF, R = 680Ω
t_S	B to LEY Set-up Time ($\overline{OEB}$ = HIGH)	8		8		ns	Figure 1, C_L = 50pF, R_L = 390Ω, R_2 = 1kΩ
t_H	B to LEY Hold Time ($\overline{OEB}$ = HIGH)	8		9		ns	
t_S	Y to LEB Set-up Time (OEY = LOW)	8		8		ns	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ
t_H	Y to LEB Hold Time (OEY = LOW)	8		9		ns	

*AC perfomance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

B_0, B_1 B_2, B_3 The four bidirectional system data bus inputs/outputs. The B-to-Y path is inverting for the Am2961 ($\overline{B}_i$) and noninverting for the Am2962 (B_i).

$\overline{OEB}$ The three-state Output Enable for the system data bus output drivers. When $\overline{OEB}$ is LOW data from the Data Output Latch is output to the system data bus. When $\overline{OEB}$ is HIGH the bus drivers are in the high-impedance state and the Data Input Latch can receive input data from the system data bus.

LEB Latch Enable for the Data Output Latch. When LEB is HIGH the latch is transparent and Y-Bus data is output to the B-Bus. When LEB goes LOW, Y-Bus data meeting the latch set-up and hold time requirements is latched for output to the B-Bus.

Y_0, Y_1, Y_2, Y_3 The four bidirectional EDC data inputs/outputs for connection to the EDC data I/O port.

LEY The Latch Enable control for the Data Input Latch for the data input from the system data bus (B). When LEY is HIGH the latch is transparent and B input data is available at the MUX input for selection to the Y outputs. When LEY goes LOW, B input data meeting the latch set-up and hold time requirements is latched for subsequent selection to the Y outputs.

OEY Output Enable for the Y (EDC) Bus outputs. When OEY is HIGH data selected by the input data multiplexer is output to the Y-bus. When OEY is LOW the MUX output is in the high-impedance state and the Y-Bus can receive input data from the EDC Unit.

S The Select input for the input data multiplexer. A LOW input selects data from the memory data input, $\overline{DI}$, for output to the EDC bus (Y). A HIGH input selects data from the system data bus Data Input Latch (B or $\overline{B}$).

$\overline{DO}_0$, $\overline{DO}_1$, $\overline{DO}_2$, $\overline{DO}_3$ The Data Outputs to the memory data inputs. The $\overline{DO}$ outputs are inverted with respect to the EDC Bus (Y). These outputs are "RAM Driver" outputs with a collector resistor in the lower output driver to protect against undershoot on the HIGH-to-LOW transition.

$\overline{OED}$ Output Enable for the $\overline{DO}$ outputs. An active LOW input causes the $\overline{DO}$ outputs to output inverted data from the EDC (Y) Bus and a HIGH input puts the $\overline{DO}$ outputs in the high-impedance state.

$\overline{DI}_0$, $\overline{DI}_1$, $\overline{DI}_2$, $\overline{DI}_3$ The Data Inputs from memory. $\overline{DI}$ inputs are selected by the data input MUX for output to the EDC (Y) Bus (controlled by S and OEY) and/or output to the system data bus (B) (controlled by LEB and $\overline{OEB}$).

FUNCTION TABLES

Y-BUS OUTPUT

LEY	$\overline{DI_i}$	$\overline{B_i}$* Am2961	B_i* Am2962	S	OEY	Y
X	X	X	X	X	L	Z
X	L	X	X	L	H	H
X	H	X	X	L	H	L
H	X	L	H	H	H	H
H	X	H	L	H	H	L
L	X	X	X	H	H	NC

*$\overline{OEB}$ = HIGH for B data input

B-BUS OUTPUT

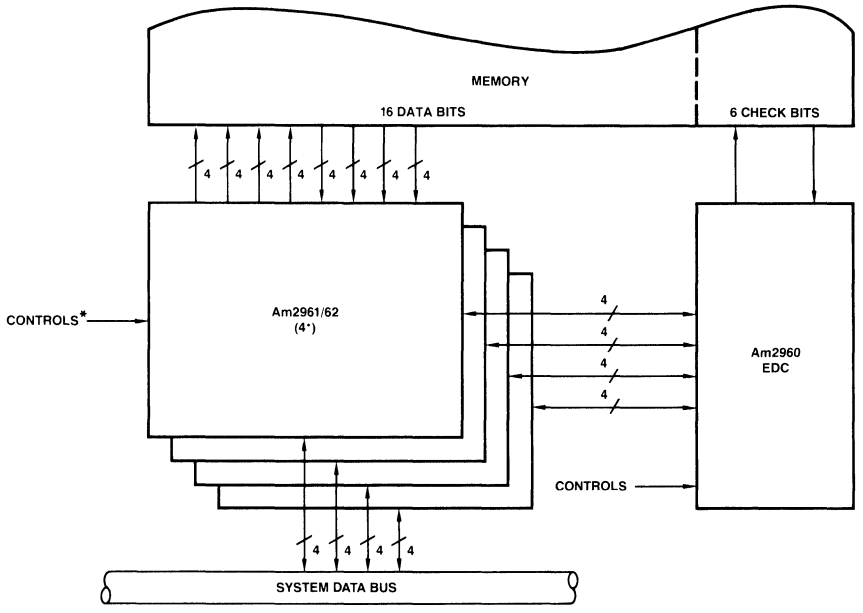
Y* Input	LEB	$\overline{OEB}$	$\overline{B}$ Am2961	B Am2962
X	X	H	Z	Z
L	H	L	H	L
H	H	L	L	H
X	L	L	NC	NC

*OEY = LOW for B data input

$\overline{DO}$ PORT OUTPUT

Y	$\overline{OED}$	$\overline{DO}$
X	H	Z
L	L	H
H	L	L

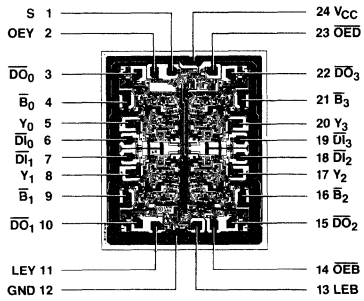
APPLICATION



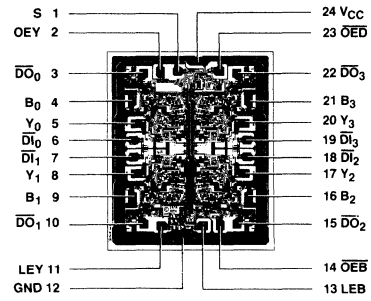
*Since the EDC Data Bus Buffers are four-bit wide devices, controls can be paired to device inputs to provide byte level controls (for any data width).

METALLIZATION AND PAD LAYOUTS

Am2961



Am2962



DIE SIZES .102" X .087"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2961 Order Number	Am2962 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2961DC	AM2962DC	D-24-SLIM	C	C-1
AM2961DC-B	AM2962DC-B	D-24-SLIM	C	B-2 (Note 4)
AM2961DM	AM2962DM	D-24-SLIM	M	C-3
AM2961DM-B	AM2962DM-B	D-24-SLIM	M	B-3
AM2961FM	AM2962FM	F-24	M	C-3
AM2961FM-B	AM2962FM-B	F-24	M	B-3
AM2961XC	AM2962XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B
AM2961XM	AM2962XM	Dice	M	

Notes: 1. D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75V to 5.25V, M = −55 to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

This device is also characterized as:
AmZ8164B

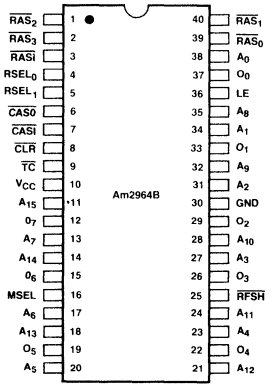
Am2964B
Dynamic Memory Controller

DISTINCTIVE CHARACTERISTICS

- Dynamic Memory Controller for 16K and 64K MOS dynamic RAMs
- 8-Bit Refresh Counter for refresh address generation, has clear input and terminal count output
- Refresh Counter terminal count selectable at 256 or 128
- Latch input $\overline{RAS}$ Decoder provides 4 $\overline{RAS}$ outputs, all active during refresh
- Dual 8-Bit Address Latches plus separate $\overline{RAS}$ Decoder Latches
- Grouping functions on a common chip minimizes speed differential or skew between address, $\overline{RAS}$ and $\overline{CAS}$ outputs
- 3-Port, 8-Bit Address Multiplexer with Schottky speed
- Burst mode, distributed refresh or transparent refresh mode determined by user
- Non-inverting address, $\overline{RAS}$ and $\overline{CAS}$ paths
- 100% MIL-STD-883 reliability assurance testing

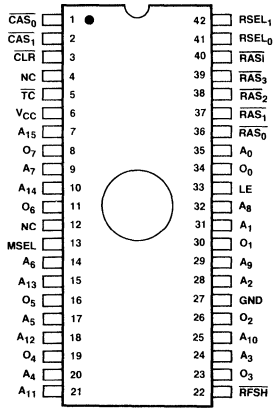
CONNECTION DIAGRAMS
Top Views

DIP



BLI-124

Flatpack



Note: Pin 1 is marked for orientation.

FUNCTIONAL DESCRIPTION

The Am2964B Dynamic Memory Controller (DMC) replaces a dozen MSI devices by grouping several unique functions. Two 8-bit latches capture and hold the memory address. These latches and a clearable, 8-bit refresh counter feed into an 8-bit, 3-input, Schottky speed MUX, for output to the dynamic RAM address lines.

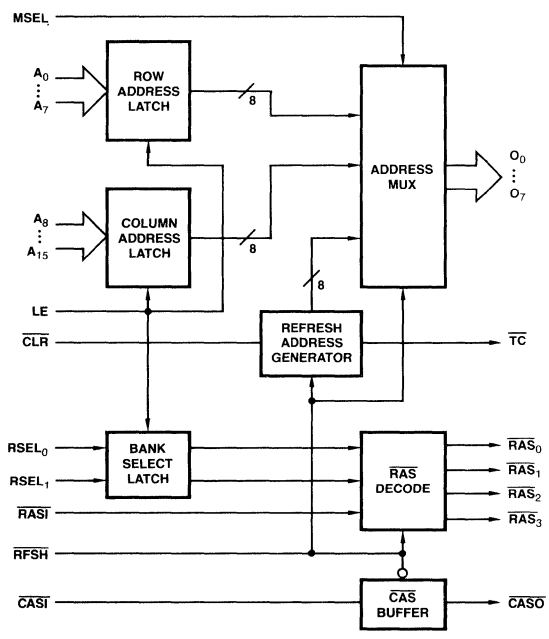
The same silicon chip also includes a special $\overline{RAS}$ decoder and $\overline{CAS}$ buffer. Placing these functions on the same chip minimizes the time skew between output functions which would otherwise be separate MSI chips, and therefore, allows a faster memory cycle time by the amount of skew eliminated.

The $\overline{RAS}$ Decoder allows upper addresses to select one-of-four banks of RAM by determining which bank receives a $\overline{RAS}$ input. During refresh ($\overline{RFSH}$ = LOW) the decoder mode is changed to four-of-four and all banks of memory receive a $\overline{RAS}$ input for refresh in response to a $\overline{RASI}$ active LOW input. $\overline{CAS}$ is inhibited during refresh.

Burst mode refresh is accomplished by holding $\overline{RFSH}$ LOW and toggling $\overline{RASI}$.

A_{15} is a dual function input which controls the refresh counter's range. For 64K RAMs it is an address input. For 16K RAMs it can be pulled to +12V through 1KΩ to terminate the refresh count at 128 instead of 256.

LOGIC DIAGRAM



BLI-123

MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	+0.5V to +V_{CC} MAX
DC Input Voltage	−0.5 to 5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

(Group A, Subgroups 1, 2 and 3)

Am2964XC T_A = 0 to + 70°C V_{CC} + 5.0V ± 5% (Com'l) MIN + 4.75V MAX = 5.25V

Am2964XM T_C = −55 to +125°C V_{CC} = 5.0V ± 10% (MIL) MIN = 4.50V MAX = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min	TYP (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}, I_{OH} = −1mA	$\overline{TC}$	2.5			Volts
			Others	3.0			Volts
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}, I_{OH} = −15mA	All outputs except $\overline{TC}$	2.0			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	All outputs except $\overline{TC}$, I_{OL} = 16mA			0.5	Volts
			$\overline{TC}$, I_{OL} = 8mA			0.5	Volts
V_{IH}	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{RASI}$			−3.2	mA
			$\overline{CASI}$, MSEL, $\overline{RFSH}$			−1.6	mA
			A_0 − A_{15}, $\overline{CLR}$, $RSEL_{0,1}$, LE			−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	$\overline{RASI}$			100	μA
			$\overline{CASI}$, MSEL, $\overline{RFSH}$			50	μA
			A_0-A_{15}, $\overline{CLR}$, $RSEL_{0,1}$, LE			20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} − 5.5V	$\overline{RASI}$			2.0	mA
			$\overline{CASI}$, MSEL, $\overline{RFSH}$			1.0	mA
		V_{CC} = MAX, V_{IN} = 7.0V	A_0-A_{15}, $\overline{CLR}$, $RSEL_{0,1}$, LE			0.1	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX (Note 3)		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	25°C, 5V			122		mA
		0 to 70°C	COM'L			173	mA
		70°C				165	mA
		−55 to +125°C	MIL			165	mA
		+125°C				150	mA
I_T	A_{15} Enable Current	A_{15} connected to +12V through 1KΩ ± 10%				5	mA

Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is worst case when the Address inputs are latched HIGH, the refresh counter is at terminal count (255), $\overline{RASI}$ and $\overline{CASI}$ are HIGH and all other inputs are LOW.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR C_L = 50pF

(Notes 5, 6)

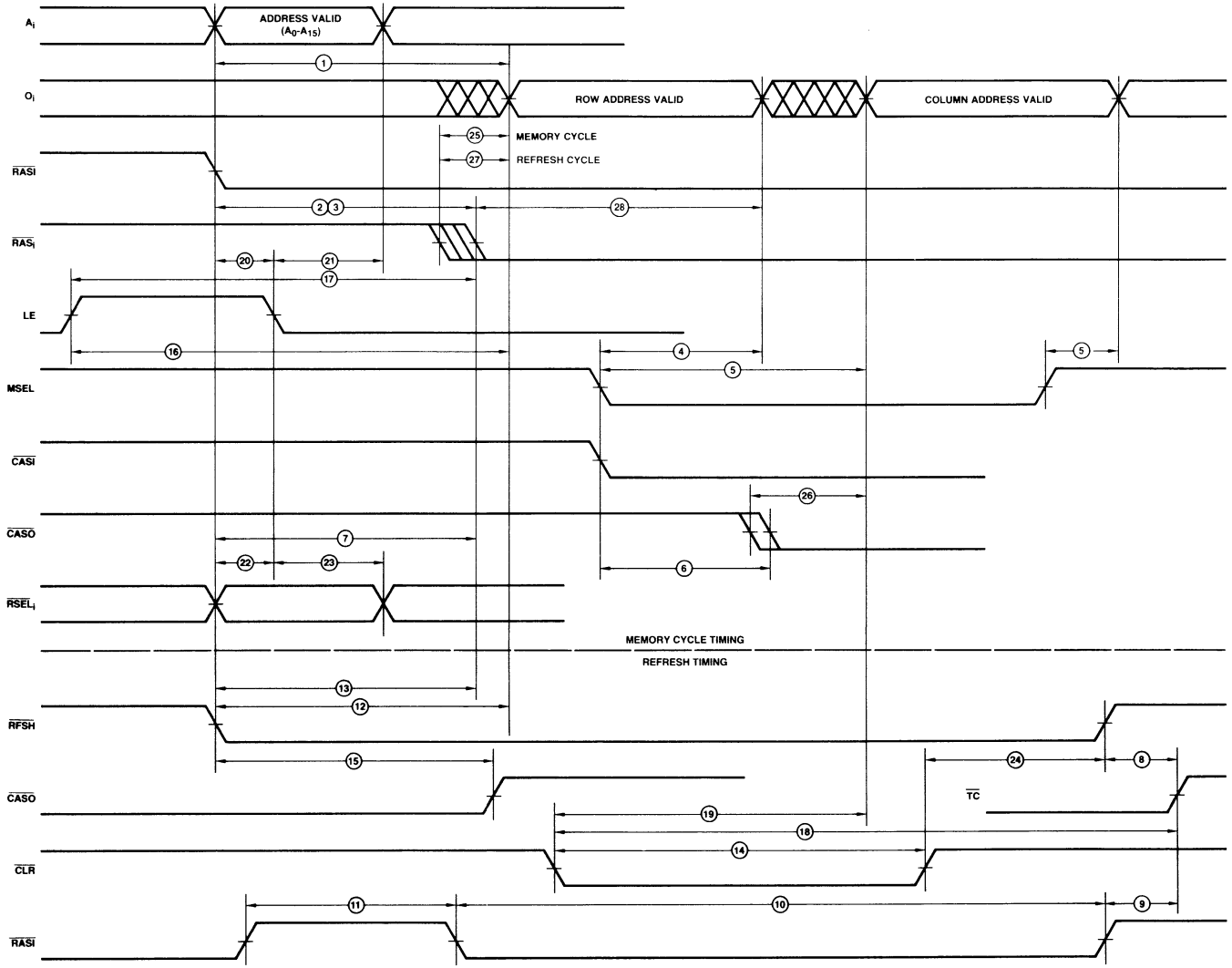
Parameter		Description	T_A = +25°C, V_{CC} = 5.0V Typ.	COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% Min.	COM'L Max.	MIL T_C = −55°C to +125°C, V_{CC} = 5.0V ± 10% Min.	MIL Max.	Units	Test Conditions
1	t_{PD}	A_i to O_i Delay	14		19		23	ns	
2	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = H)	14		20		23	ns	
3	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = L)	14		20		23	ns	
4	t_{PD}	MSEL to O_i	17	9		9		ns	
5	t_{PD}	MSEL to O_i	17		21		25	ns	
6	t_{PHL}	$\overline{CASI}$ to $\overline{CASO}$ ($\overline{RFSH}$ = H)	12		17		19	ns	
7	t_{PHL}	$RSEL_i$ to $\overline{RAS_i}$ (LE = H, $\overline{RASI}$ = L)	15		20		24	ns	
8	t_{PLH}	$\overline{RFSH}$ to $\overline{TC}$ ($\overline{RASI}$ = L)	30		40		50	ns	
9	t_{PLH}	$\overline{RASI}$ to $\overline{TC}$ ($\overline{RFSH}$ = L)	25		35		40	ns	
10	t_{PW}	$\overline{RASI}$ = L ($\overline{RFSH}$ = L)	10	50		50		ns	
11	t_{PW}	$\overline{RASI}$ = H ($\overline{RFSH}$ = L)	10	50		50		ns	
12	t_{PD}	$\overline{RFSH}$ to O_i ($\overline{RASI}$ = X)	17		21		25	ns	
13	t_{PHL}	$\overline{RFSH}$ to $\overline{RAS_i}$ ($\overline{RASI}$ = L)	19		26		29	ns	C_L = 50pF
14	t_{PW}	$\overline{CLR}$ = L	10	30		35		ns	
15	t_{PLH}	$\overline{RFSH}$ to $\overline{CASO}$ ($\overline{RASI}$ = L $\overline{CASI}$ = L, Note 7)	16		21		25	ns	
16	t_{PD}	LE to O_i	25		35		40	ns	
17	t_{PHL}	LE to $\overline{RAS_i}$	30		40		45	ns	
18	t_{PLH}	$\overline{CLR}$ to $\overline{TC}$	35		45		56	ns	
19	t_{PLH}	$\overline{CLR}$ to O_i ($\overline{RFSH}$ = L)	31		44		54	ns	
20	t_S	A_i to LE Set-up Time	0	5		5		ns	
21	t_H	A_i to LE Hold Time	5	12		15		ns	
22	t_S	$RSEL_i$ to LE Set-up Time	0	5		5		ns	
23	t_H	$RSEL_i$ to LE Hold Time	10	17		25		ns	
24	t_S	$\overline{CLR}$ Recovery Time	5	12		15		ns	
25	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = H, Note 8)	2		5		6	ns	
26	t_{SKEW}	O_i to $\overline{CASO}$ (Note 8)	4		6		8	ns	
27	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = L, Note 9)	6		8		10	ns	
28	t_{SKEW}	O_i to $\overline{RAS_i}$ (MSEL = ⌇, Note 10)	1		5		5	ns	

Notes:
5. Minimum spec limits for t_{PW}, t_S and t_H are minimum system operating requirements. Limits for t_{SKEW} and t_{PD} are guaranteed test limits for the device.
6. All AC parameters are specified at the 1.5V level.
7. $\overline{RFSH}$ inhibits $\overline{CASO}$ during refresh. Specification is for $\overline{CASO}$ inhibit time.
8. O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = HIGH) skew is guaranteed maximum difference between fastest $\overline{RASI}$ to $\overline{RAS_i}$ delay and slowest A_i to O_i delay within a single device. O_i to $\overline{CASO}$ skew is maximum difference between fastest $\overline{CASI}$ to $\overline{CASO}$ delay and slowest MSEL to O_i delay within a single device. See application section entitled Memory Cycle Timing for correlation to System Timing requirements.
9. O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = LOW) skew is guaranteed maximum difference between fastest $\overline{RASI}$ to $\overline{RAS_i}$ delay and slowest $\overline{RFSH}$ to O_i delay within a single device. See application section on Refresh Timing for correlation to system refresh timing requirements.
10. O_i to $\overline{RAS_i}$ (MSEL = ⌇) skew is guaranteed maximum difference between fastest MSEL ⌇ to O_i delay and slowest $\overline{RASI}$ to $\overline{RAS_i}$ delay within a single device.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR C_L = 150pF

(Notes 5, 6)

				COM'L		MIL			
			T_A = +25°C V_{CC} = 5.0V	T_A = 0°C to +70°C V_{CC} = 5.0V ± 5%		T_C = −55°C to +125°C V_{CC} = 5.0V ± 10%			Test
	Parameter	Description	Typ.	Min.	Max.	Min.	Max.	Units	Conditions
1	t_{PD}	A_i to O_i Delay	20		25		30	ns	
2	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = H)	18		24		27	ns	
3	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = L)	18		24		27	ns	
4	t_{PD}	MSEL to O_i	23	12		12		ns	
5	t_{PD}	MSEL to O_i	23		27		31	ns	
6	t_{PHL}	$\overline{CASI}$ to $\overline{CASO}$ ($\overline{RFSH}$ = H)	17		24		26	ns	
7	t_{PHL}	$RSEL_i$ to $\overline{RAS_i}$ (LE = H, $\overline{RASI}$ = L)	19		27		30	ns	
8	t_{PLH}	$\overline{RFSH}$ to $\overline{TC}$ ($\overline{RASI}$ = L)	34		45		55	ns	
9	t_{PLH}	$\overline{RASI}$ to $\overline{TC}$ ($\overline{RFSH}$ = L)	32		45		55	ns	
10	t_{PW}	$\overline{RASI}$ = L ($\overline{RFSH}$ = L)	10	50		50		ns	
11	t_{PW}	$\overline{RASI}$ = H ($\overline{RFSH}$ = L)	10	50		50		ns	
12	t_{PD}	$\overline{RFSH}$ to O_i ($\overline{RASI}$ = X)	21		27		30	ns	
13	t_{PHL}	$\overline{RFSH}$ to $\overline{RAS_i}$ ($\overline{RASI}$ = L)	25		33		36	ns	C_L = 150pF
14	t_{PW}	$\overline{CLR}$ = L	0	30		35		ns	
15	t_{PLH}	$\overline{RFSH}$ to $\overline{CASO}$ ($\overline{RASI}$ = L $\overline{CASI}$ = L, Note 7)	21		27		31	ns	
16	t_{PD}	LE to O_i	30		40		50	ns	
17	t_{PHL}	LE to $\overline{RAS_i}$	34		45		54	ns	
18	t_{PLH}	$\overline{CLR}$ to $\overline{TC}$	39		55		60	ns	
19	t_{PLH}	$\overline{CLR}$ to O_i ($\overline{RFSH}$ = L)	38		50		62	ns	
20	t_S	A_i to LE Set-up Time	0	5		5		ns	
21	t_H	A_i to LE Hold Time	5	12		12		ns	
22	t_S	$RSEL_i$ to LE Set-up Time	0	5		5		ns	
23	t_H	$RSEL_i$ to LE Hold Time	10	17		25		ns	
24	t_S	$\overline{CLR}$ Recovery Time	5	12		15		ns	
25	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = H, Note 8)	3		6		7	ns	
26	t_{SKEW}	O_i to $\overline{CASO}$ (Note 8)	4		7		8	ns	
27	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = L, Note 9)	6		9		10	ns	
28	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{MSEL}$ = ↯, Note 10)	1		5		5	ns	



Am2964B Dynamic Memory Controller Timing

DEFINITION OF FUNCTIONAL TERMS

A_0-A_7 The low order Address inputs are used to latch eight Row Address inputs for the RAM. These inputs drive the outputs 0_0-0_7 when MSEL is HIGH.

A_8-A_{15} The high order Address inputs are used to latch eight Column Address inputs for the RAM. These inputs drive the outputs 0_0-0_7 when MSEL is LOW.

A_{15} A_{15} is a dual input. With normal TTL level inputs A_{15} acts as address input A_{15} for 64K RAMs. If A_{15} is pulled up to +12V through a 1KΩ resistor, the terminal count output, $\overline{TC}$, will go LOW every 128 counts (for 16K RAMs) instead of every 256 counts.

0_0-0_7 The RAM address outputs. The eight-bit width is designed for dynamic RAMs up to 64K.

MSEL The Multiplexer-SELect input determines whether low order or high order address inputs appear at the multiplexer outputs 0_0-0_7. When MSEL is HIGH the low order address latches (A_0-A_7) are connected to the outputs. When MSEL is LOW the high order address latches are connected to the outputs.

$\overline{RFSH}$ The Refresh control input. When active LOW the $\overline{RFSH}$ input switches the address output multiplexer to output the inverted contents of the 8-bit refresh counter. $\overline{RFSH}$ LOW also inhibits the $\overline{CAS}$ buffer and changes the mode of the $\overline{RAS}$ decoder from one-of-four to four-of-four so that all four $\overline{RAS}$ decoder outputs, $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$ and $\overline{RAS_3}$, go LOW in response to a LOW input at $\overline{RASI}$. This action refreshes one row address in each of the four $\overline{RAS}$ decoded memory banks. The refresh counter is advanced at the end of each refresh cycle by the LOW-to-HIGH transition of $\overline{RFSH}$ or $\overline{RASI}$ (whichever occurs first). In burst mode refresh, $\overline{RFSH}$ may be held LOW and refresh accomplished by toggling $\overline{RASI}$.

$\overline{TC}$ The Terminal Count output. A LOW output at $\overline{TC}$ indicates that the refresh counter has been sequenced through either 128 or 256 refresh addresses depending on A_{15}. The $\overline{TC}$ output remains active LOW until the refresh counter is advanced by the rising edge of $\overline{RASI}$ or $\overline{RFSH}$.

$\overline{CLR}$ The refresh counter Clear input. An active LOW input at $\overline{CLR}$ resets the refresh counter to all LOW (refresh address output to all HIGH).

LE The address latch enable input. An active HIGH input at LE causes the two 8-bit address latches and the 2-bit $\overline{RAS}$ Select input latch to go transparent, accepting new input data. A LOW input on LE latches the input data which meets set-up and hold time requirements.

$RSEL_0$ and $RSEL_1$ The $\overline{RAS}$ decoder Select inputs. Data (latched) at these inputs (normally higher order addresses) is decoded by the $\overline{RAS}$ Decoder to "$\overline{RAS}$ Select" one of four banks of memory with $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$ or $\overline{RAS_3}$.

$\overline{RASI}$ The Row Address Strobe Input. During normal memory cycles the selected $\overline{RAS}$ Decoder output $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$ or $\overline{RAS_3}$ will go active LOW in response to an active LOW input at $\overline{RASI}$. During refresh ($\overline{RFSH}$ = LOW), all $\overline{RAS}$ outputs go LOW in response to $\overline{RASI}$ = LOW.

$\overline{RAS_0}$, $\overline{RAS_1}$ $\overline{RAS_2}$, $\overline{RAS_3}$ Row Address Strobe outputs ($\overline{RAS_i}$). Each provides a Row Address Strobe for one of the four banks of memory. Each will go active LOW only when selected by $RSEL_0$ and $RSEL_1$ and only when $\overline{RASI}$ goes active LOW. All $\overline{RAS_{0\text{-}3}}$ outputs go active low in response $\overline{RASI}$ when $\overline{RFSH}$ goes LOW.

$\overline{CASI}$ The Column Address Strobe. An active LOW input at $\overline{CASI}$ will result in an active LOW output at $\overline{CASO}$, unless a refresh cycle is in progress ($\overline{RFSH}$ = LOW).

$\overline{CASO}$ The Column Address Strobe output. The active LOW $\overline{CASO}$ output strobes the Column Address into the dynamic RAM. $\overline{CASO}$ is inhibited during refresh ($\overline{RFSH}$ = LOW).

$\overline{RAS}$ OUTPUT FUNCTION TABLE

$\overline{RFSH}$	$\overline{RASI}$	$RSEL_1$	$RSEL_0$	$\overline{RAS_0}$	$\overline{RAS_1}$	$\overline{RAS_2}$	$\overline{RAS_3}$
L	H	X	X	H	H	H	H
L	L	X	X	L	L	L	L
H	H	X	X	H	H	H	H
H	L	L	L	L	H	H	H
H	L	L	H	H	L	H	H
H	L	H	L	H	H	L	H
H	L	H	H	H	H	H	L

$\overline{CASO}$ FUNCTION TABLE

$\overline{RFSH}$	$\overline{CASI}$	$\overline{CASO}$
H	L	L
H	H	H
L	X	H

ADDRESS OUTPUT FUNCTION TABLE

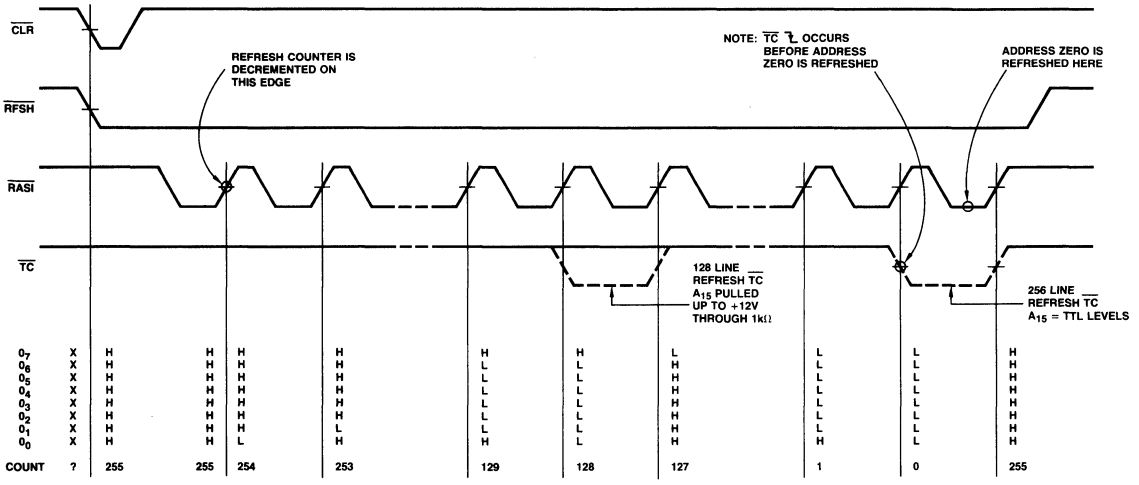
MSEL	$\overline{RFSH}$	0_0-0_7
H	H	A_0-A_7
L	H	A_8-A_{15}
X	L	Refresh Address

REFRESH ADDRESS COUNTER FUNCTION TABLE

A_{15}	$\overline{CLR}$	$\overline{RFSH}$	$\overline{RASI}$	$\overline{TC}$	REFRESH COUNT	FUNCTION
X	L	X	X	X	FF_H	Clear Counter
X	H	↓	X	X	NC	Output Refresh Address No Change for Counter
X	H	↓	L	X	Count − 1	Return to Memory Cycle Mode and Decrement Counter
X	H	L	↓	X	NC	Output all RAS_i to RAM No Change for Counter
X	H	L	↓	X	Count − 1	Return RAS_i to HIGH and Decrement Counter
L or H	H	X	X	L	00_H	Terminal Count for 256 Line Refresh
+12V*	H	X	X	L	00_H and 80_H	Terminal Count for 128 Line Refresh

*Through 1 kΩ resistor.

BURST REFRESH TIMING



The timing shown assumes that burst mode applications may power-down the Am2964B with the RAM. Therefore the counter is cleared prior to executing the refresh sequence.

APPLICATION

ARCHITECTURE

The Dynamic Memory Controller (DMC) provides address multiplexing, refresh address generation and $\overline{RAS}/\overline{CAS}$ control for the MOS dynamic RAM memories of any data width. The eight bit address path is designed for 64K RAMs and can be used with 16K RAMs.

Sixteen address input latches and two $\overline{RAS}$ Select latches (for higher order addresses) allow the DMC to control up to 256K words of memory (with 64K RAMs) by using the internal $\overline{RAS}$ decoder to select from one-of-four banks of RAMs.

SPEED WITH MINIMUM SKEW

The DMC provides Schottky speed in all of the critical paths. In addition, time skew between the Address, $\overline{RAS}$ and $\overline{CAS}$ paths is minimized (and specified) by placing these functions on the same chip. The inclusion of the $\overline{CAS}$ buffer allows matching of its propagation delay, plus provides the $\overline{CAS}$ inhibit function during $\overline{RAS}$ – only refresh.

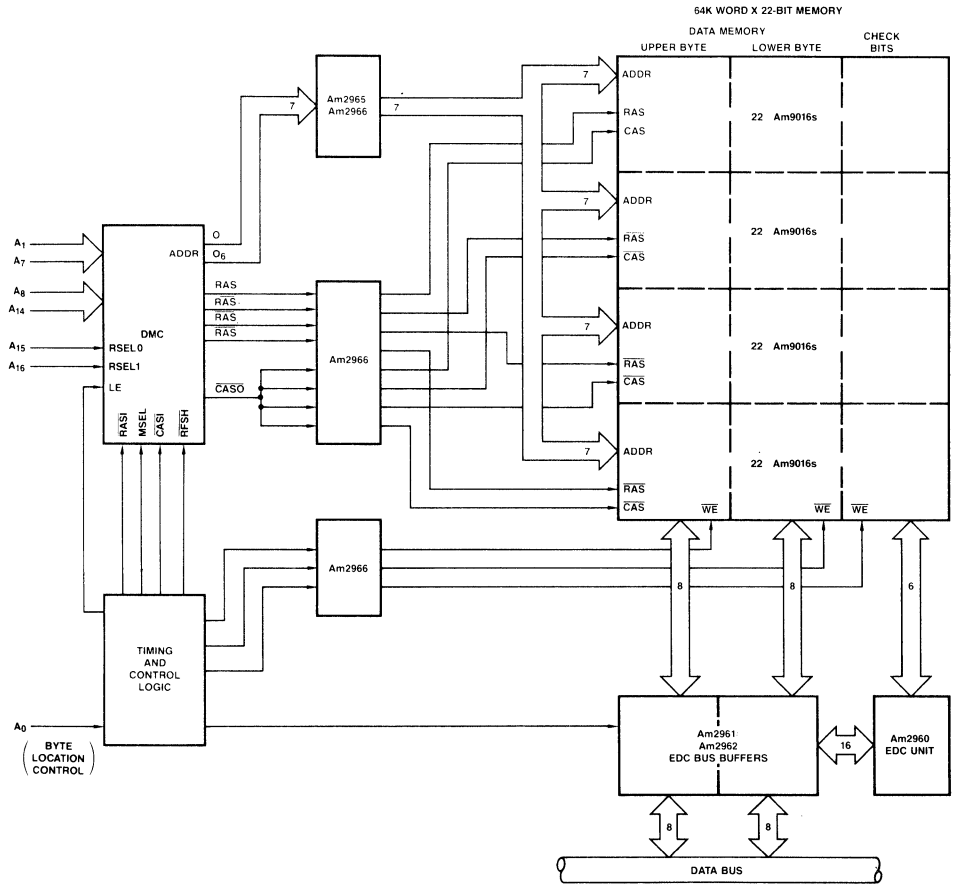
INPUT LATCHES

The eighteen input latches are transparent when LE is HIGH and latch the input data meeting set-up and hold time requirements when LE goes LOW. In systems with separate address and data buses, LE may be permanently enabled HIGH.

REFRESH COUNTER

The 8-bit refresh counter provides both 128 and 256 line refresh capability. Refresh control is external to allow maximum user flexibility. Transparent (hidden), burst, synchronous or asynchronous refresh modes are all possible.

The refresh counter is advanced at the LOW-to-HIGH transition of $\overline{RFSH}$ (or $\overline{RASI}$). This assures a stable counter output for the next refresh cycle. The counter will continue to cycle through 256 addresses unless reset to zero by $\overline{CLR}$. This actually causes all outputs to go HIGH since the output MUX is inverting. (Address inputs to outputs are non-inverting since both the input latches and output MUX are inverting).



*Address and $\overline{RAS}/\overline{CAS}$ drivers each drive 22 RAM inputs at each output. Timing skew is minimized by using one device for address lines and one device for $\overline{RAS}/\overline{CAS}$, spreading the $\overline{CAS}$ loading over four drivers to equalize the capacitive load on each driver.

Figure 1. Dynamic Memory Control with Error Detection and Correction

REFRESH TERMINAL COUNT

The refresh counter also provides a Terminal Count output for burst mode refresh applications. $\overline{TC}$ normally occurs at count 255 (0_7 to 0_7 all LOW when $\overline{RFSH}$ is LOW). $\overline{TC}$ can be made to occur at count 127 for 128 line burst mode refresh by pulling A_{15} up to +12V through a 1KΩ ± 10% resistor. The counter actually cycles through 256 with $\overline{TC}$ determined by A_{15}. Otherwise A_{15} functions as an address input when driven at normal TTL levels.

THREE INPUT 8-BIT ADDRESS MULTIPLEXER

The address MUX is 8-bits wide (for 64K RAMs) and has three data sources, the lower address input latch (A_0 to A_7), the upper address input latch (A_8 to A_{15}) and the internal refresh counter. The lower address latch is selected when MSEL is HIGH. This is normally the Row address. The upper address latch is selected when MSEL is LOW. This is normally the Column address. The third source – the refresh counter is selected when $\overline{RFSH}$ is LOW and overrides MSEL.

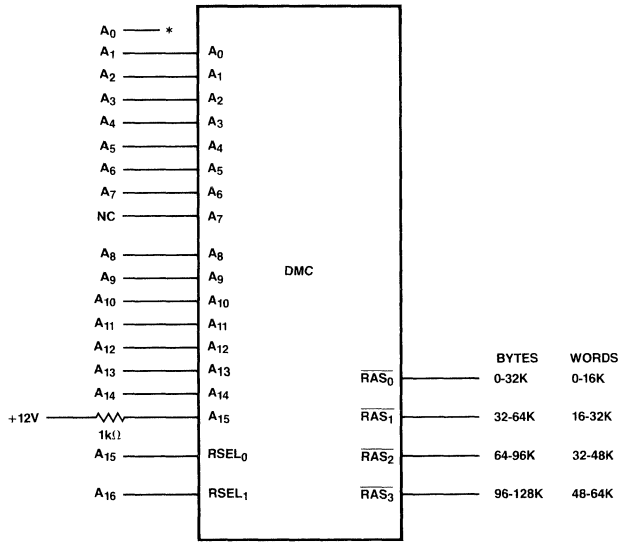
When $\overline{RFSH}$ goes LOW, the MUX selects the refresh counter address and $\overline{CASO}$ is inhibited. Also, the $\overline{RAS}$ Decoder function is changed from one-of-four to four-of-four so all $\overline{RAS}$ outputs $\overline{RAS_0}$-$\overline{RAS_3}$ go LOW to refresh all banks of memory when $\overline{RASI}$ goes LOW. When RFSH is HIGH only one $\overline{RAS}$ output goes low, determined by the $\overline{RAS}$ Select inputs, $RSEL_0$ and $RSEL_1$. In either case the $\overline{RAS}$ Decoder output timing is controlled by $\overline{RASI}$ to make sure the refresh count appears at 0_0-0_7 before $\overline{RAS_0}$-$\overline{RAS_3}$ go LOW. This assures meeting Row address Set-up time requirement of the RAM (t_{ASR}).

MAXIMUM PERFORMANCE SYSTEM

The typical organization of a maximum performance 16-bit system including Error Detection and Correction is shown in Figure 1. Delay lines provide the most accurate timing and are recommended for $\overline{RAS}$/MSEL/$\overline{CAS}$ timing in this type of system.

CONTROLLING 16K RAMS OR SMALLER SYSTEMS

16K RAMs require seven address inputs and 128 line refresh. Also, A_0 is often used to designate upper or lower byte trans actions in 16-bit systems. These modifications are shown in Figure 2.



*A_0 Controls Byte Select Logic

Figure 2. Word Organized Memory Using 16K RAMs

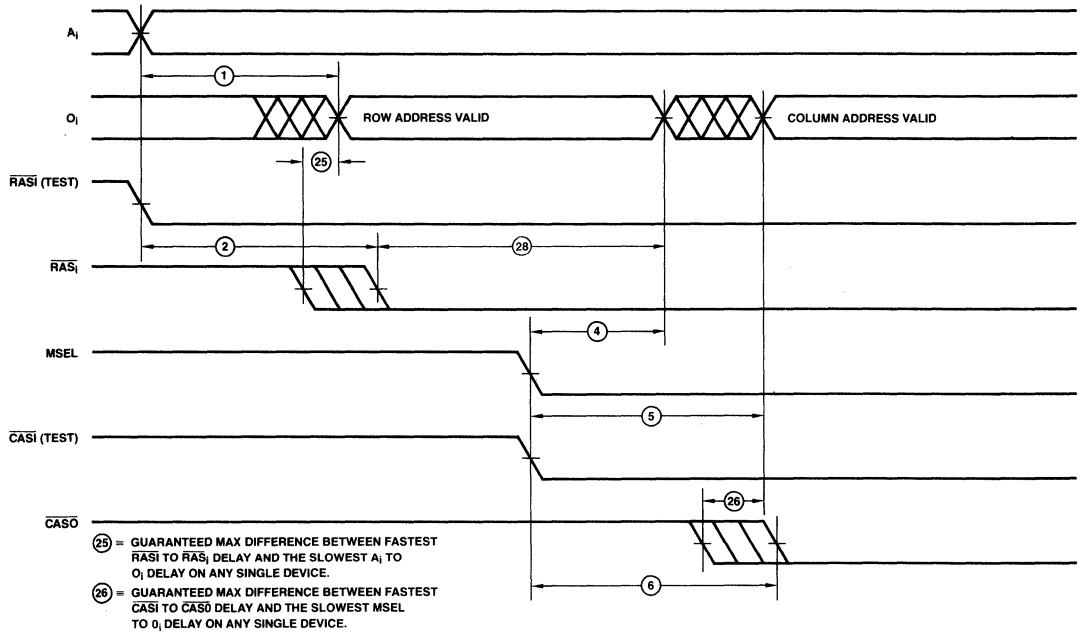
MEMORY CYCLE TIMING

The relationship between DMC specifications and system timing requirements are shown in Figure 3. T_1, T_2 and T_3 represent the minimum timing requirements at the DMC inputs to guarantee that RAM timing requirements are met and that maximum system performance is achieved.

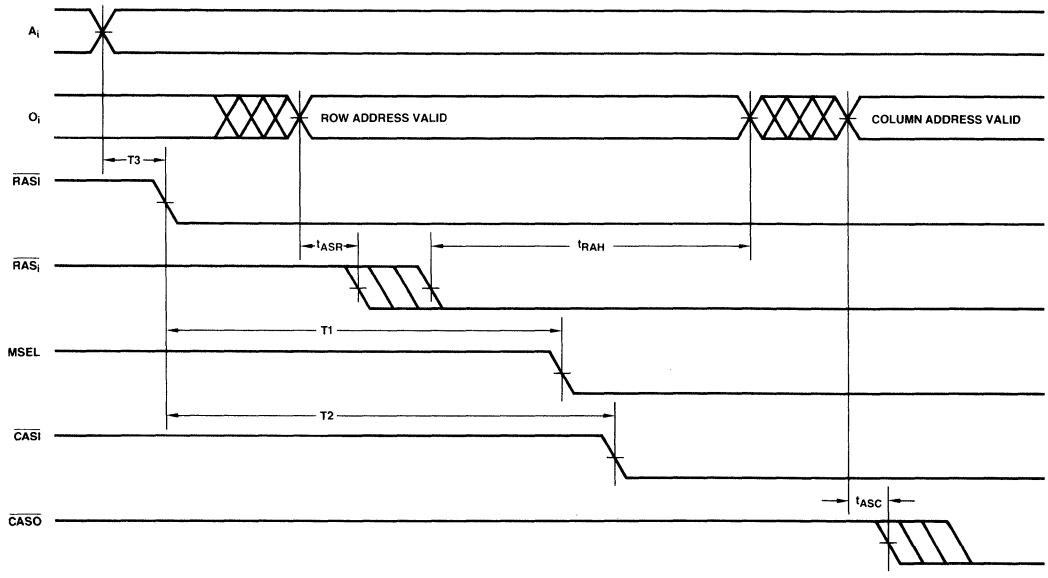
The minimum requirement for T_1, T_2, and T_3 are as follows:

$T_1MIN = t_{RAH} + t_{28}$
$T_2MIN = T_1 + t_{26} + t_{ASC}$
$T_3MIN = t_{ASR} + t_{25}$

See RAM data sheet for applicable values for t_{RAH}, t_{ASC} and t_{ASR}.



a) Specifications Applicable to Memory Cycle Timing



b) Desired System Timing

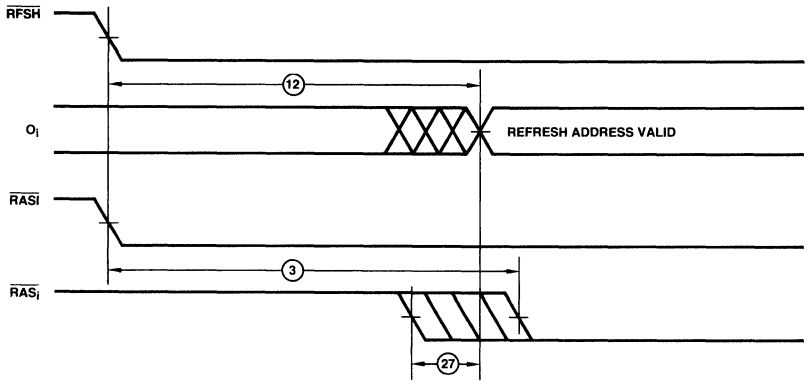
Figure 3. Memory Cycle Timing

REFRESH CYCLE TIMING

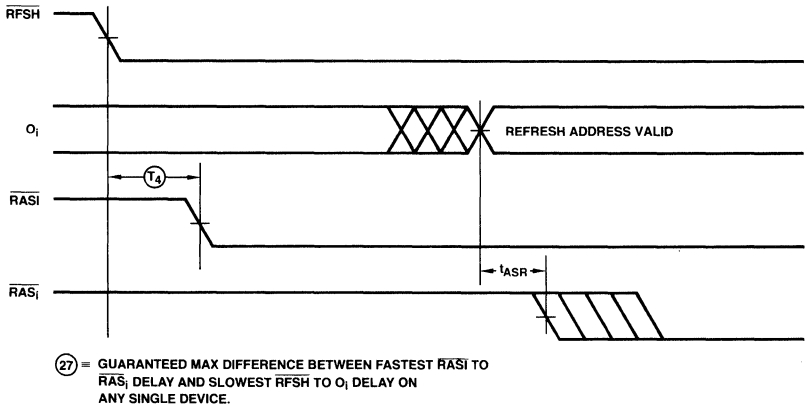
The timing relationships for refresh are shown in Figure 4.

T_4 minimum is calculated as follows:

$T_4 = t_{ASR} + t_{27}$



a) Test Waveforms

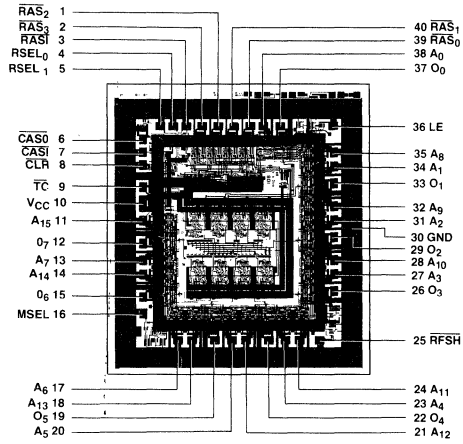


(27) = GUARANTEED MAX DIFFERENCE BETWEEN FASTEST $\overline{RASI}$ TO $\overline{RAS_i}$ DELAY AND SLOWEST $\overline{RFSH}$ TO O_i DELAY ON ANY SINGLE DEVICE.

b) Desired System Timing

Figure 4. Refresh Timing

Metallization and Pad Layout



DIE SIZE 0.156" X 0.143"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2964B Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2964BPC	P-40	C	C-1
AM2964BDC	D-40	C	C-1
AM2964BDC-B	D-40	C	B-2 (Note 4)
AM2964BDM	D-40	M	C-3
AM2964BDM-B	D-40	M	B-3
AM2964BFM	F-42	M	C-3
AM2964BFM-B	F-42	M	B-3
AM2964BXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B
AM2964BXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

This device is also characterized as:
AmZ8165
AmZ8166

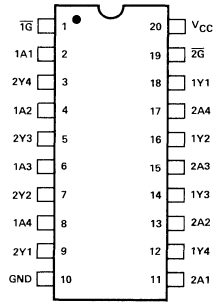
Am2965 • Am2966

Octal Dynamic Memory Drivers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- **Controlled rise and fall characteristics**
  Internal resistors provide symmetrical drive to HIGH and LOW states, eliminating need for external series resistor.
- **Output swings designed to drive 16K and 64K RAMs**
  V_{OH} guaranteed at V_{CC} −1.15V. Undershoot going LOW guaranteed at less than 0.5V.
- **Large capacitive drive capability**
  35mA min source or sink current at 2.0V. Propagation delays specified for 50pF and 500pF loads.
- **Pin-compatible with 'S240 and 'S244**
  Non-inverting Am2966 replaces 74S244; inverting Am2965 replaces 74S240. Faster than 'S240/244 under equivalent load.
- **No-glitch outputs**
  Outputs forced into OFF state during power up and down. No glitch coming out of three-state.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLI-125

FUNCTIONAL DESCRIPTION

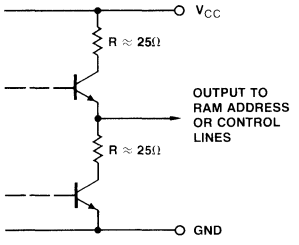
The Am2965 and Am2966 are designed and specified to drive the capacitive input characteristics of the address and control lines of MOS dynamic RAMs. The unique design of the lower output driver includes a collector resistor to control undershoot on the HIGH-to-LOW transition. The upper output driver pulls up to V_{CC} − 1.15V to be compatible with MOS memory and is designed to have a rise time symmetrical with the lower output's controlled fall time. This allows optimization of Dynamic RAM performance.

The Am2965 and Am2966 are pin-compatible with the popular 'S240 and 'S244 with identical 3-state output enable controls. The Am2965 has inverting drivers and the Am2966 has non-inverting drivers.

The inclusion of an internal resistor in the lower output driver eliminates the requirement for an external series resistor, therefore reducing package count and the board area required. The internal resistor controls the output fall and undershoot without slowing the output rise.

These devices are designed for use with the Am2964 Dynamic Memory Controller where large dynamic memories with highly capacitive input lines require additional buffering. Driving eight address lines or four $\overline{RAS}$ and four $\overline{CAS}$ lines with drivers on the same silicon chip also provides a significant performance advantage by minimizing skew between drivers. Each device has specified skew between drivers to improve the memory access worst case timing over the min and max t_{PD} difference of unspecified devices.

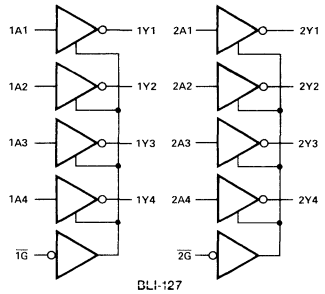
TYPICAL OUTPUT DRIVER



BLI-126

LOGIC DIAGRAMS

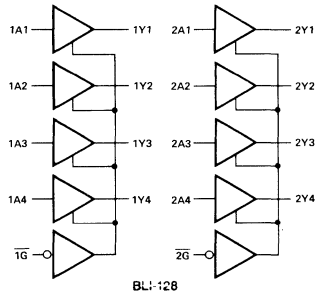
Am2965



BLI-127

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Am2966



BLI-128

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +7.0V
DC Output Current, into Outputs	200mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

Am2965/66XC, DC, PC	T_A = 0 to 70°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V	MAX = 5.50V)
Am2965/66XM, DM	T_A = −55 to +125°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V	MAX = 5.50V)
Am2965/66FM	T_C = −55 to +125°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V	MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1mA	V_{CC}−1.15	V_{CC}−0.7V		Volts
V_{OL}	Output LOW Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA			0.5	Volts
				I_{OL} = 12mA			0.8	
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current		V_{CC} = MAX, V_{IN} = 0.4V	DATA			−200	μA
				$\overline{1G}$, $\overline{2G}$			−400	
I_{IH}	Input HIGH Current		V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current		V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_{OZH}	Off-State Current		V_O = 2.7V				100	μA
I_{OZL}	Off-State Current		V_O = 0.4V				−200	μA
I_{OL}	Output Sink Current		V_{OL} = 2.0V		50			mA
I_{OH}	Output Source Current		V_{OH} = 2.0V		−35			mA
I_{SC}	Output Short Circuit Current (Note 3)		V_{CC} = MAX		−60 (see I_{OH})		−200	mA
I_{CC}	Supply Current	Am2965	All Outputs HIGH	V_{CC} = MAX, Outputs Open		24	50	mA
			All Outputs LOW			86	125	
			All Outputs Hi-Z			86	125	
		Am2966	All Outputs HIGH	V_{CC} = MAX, Outputs Open		53	75	
			All Outputs LOW			92	130	
			All Outputs Hi-Z			116	150	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Am2965 • Am2966
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

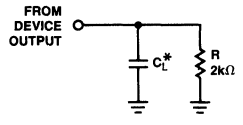
Parameters	Description	Test Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time from LOW-to-HIGH Output	Figure 1 Test Circuit Figure 3 Voltage Levels and Waveforms	C_L = 0pF		6	(Note 4)	ns
			C_L = 50pF	6	9	15	
			C_L = 500pF	18	22	30	
t_{PHL}	Propagation Delay Time from HIGH-to-LOW Output		C_L = 0pF		4	(Note 4)	ns
			C_L = 50pF	5	7	15	
			C_L = 500pF	18	22	30	
t_{PLZ}	Output Disable Time from LOW, HIGH	Figures 2 and 4, S = 1			11	20	ns
t_{PHZ}		Figures 2 and 4, S = 2			6.5	12	
t_{PZL}	Output Enable Time from LOW, HIGH	Figures 2 and 4, S = 1			12	20	ns
t_{PZH}		Figures 2 and 4, S = 2			12	20	
t_{SKEW}	Output-to-Output Skew	Figures 1 and 3, C_L = 50pF			±0.5	±3.0 (Note 5)	ns
V_{ONP}	Output Voltage Undershoot	Figures 1 and 3, C_L = 50pF			0	−0.5	Volts

SWITCHING CHARACTERISTICS
OVER OPERATING RANGE (Note 6)

Parameters	Description	Test Conditions		COM'L T_A = 0 to 70°C V_{CC} = 5.0V ±10% Min	COM'L Max	MIL (Note 7) T_A = −55 to +125°C V_{CC} = 5.0V ±10% Min	MIL Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Output	Figures 1 and 3	C_L = 50pF	4	17	4	20	ns
			C_L = 500pF	18	35	18	40	
t_{PHL}	Propagation Delay Time HIGH-to-LOW Output	Figures 1 and 3	C_L = 50pF	4	17	4	20	ns
			C_L = 500pF	18	35	18	40	
t_{PLZ}	Output Disable Time from LOW, HIGH	Figures 2 and 4	S = 1		24		24	ns
t_{PHZ}			S = 2		16		16	
t_{PZL}	Output Enable Time from LOW, HIGH	Figures 2 and 4	S = 1		28		28	ns
t_{PZH}			S = 2		28		28	
V_{ONP}	Output Voltage Undershoot	Figures 1 and 3, C_L = 50pF			−0.5		−0.5	Volts

Notes: 4. Typical time shown for reference only – not tested.
5. Time Skew specification is guaranteed by design but not tested.
6. AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.
7. T_C = −55 to +125°C for Flatpak versions.

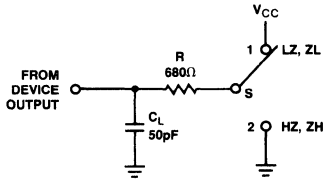
SWITCHING TEST CIRCUITS



BLI-129

*t_{pd} specified at C = 50 and 500pF

Figure 1. Capacitive Load Switching.

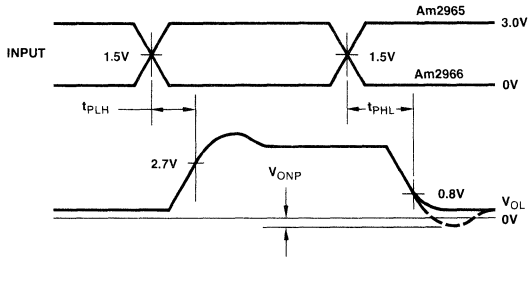


BLI-130

Figure 2. Three-State Enable/Disable.

TYPICAL SWITCHING CHARACTERISTICS

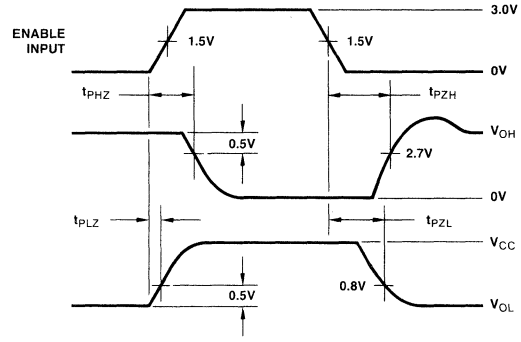
VOLTAGE WAVEFORMS



BLI-131

$t_r = t_f = 2.5ns$
f = 2.5MHz
$t_{pw} = 200ns$

Figure 3. Output Drive Levels.



BLI-132

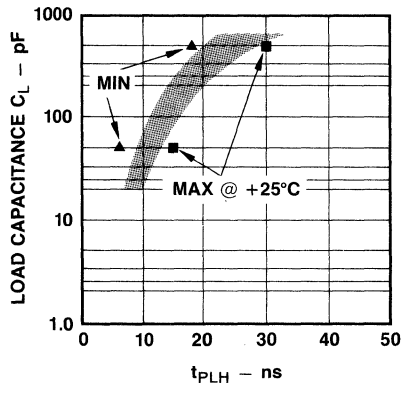
$t_r = t_f = 2.5ns$
f = 1MHz
$t_{pw} = 800ns$

Figure 4. Three-State Control Levels.

The RAM Driver symmetrical output design offers significant improvement over a standard Schottky output by providing a balanced drive output impedance (≈25Ω both HIGH and LOW), and by pulling up to MOS V_{OH} levels (V_{CC} – 1.5V). External resistors, not required with the RAM Driver, protect standard Schottky drivers from error causing undershoot but also slow the output rise by adding to the internal R.

The RAM Driver is optimized to drive LOW at maximum speed based on safe undershoot control and to drive HIGH with a symmetrical speed characteristic. This is an optimum approach because the dominant RAM loading characteristic is input capacitance.

The curves shown below provide performance characteristics typical of both the inverting (Am2965) and non-inverting (Am2966) RAM Drivers.



BLI-133

Figure 5. t_{PLH} for V_{OH} = 2.7 Volts vs. C_L.

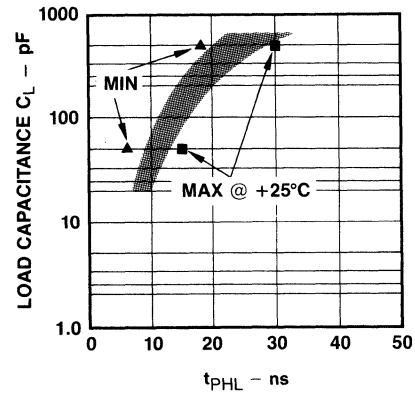
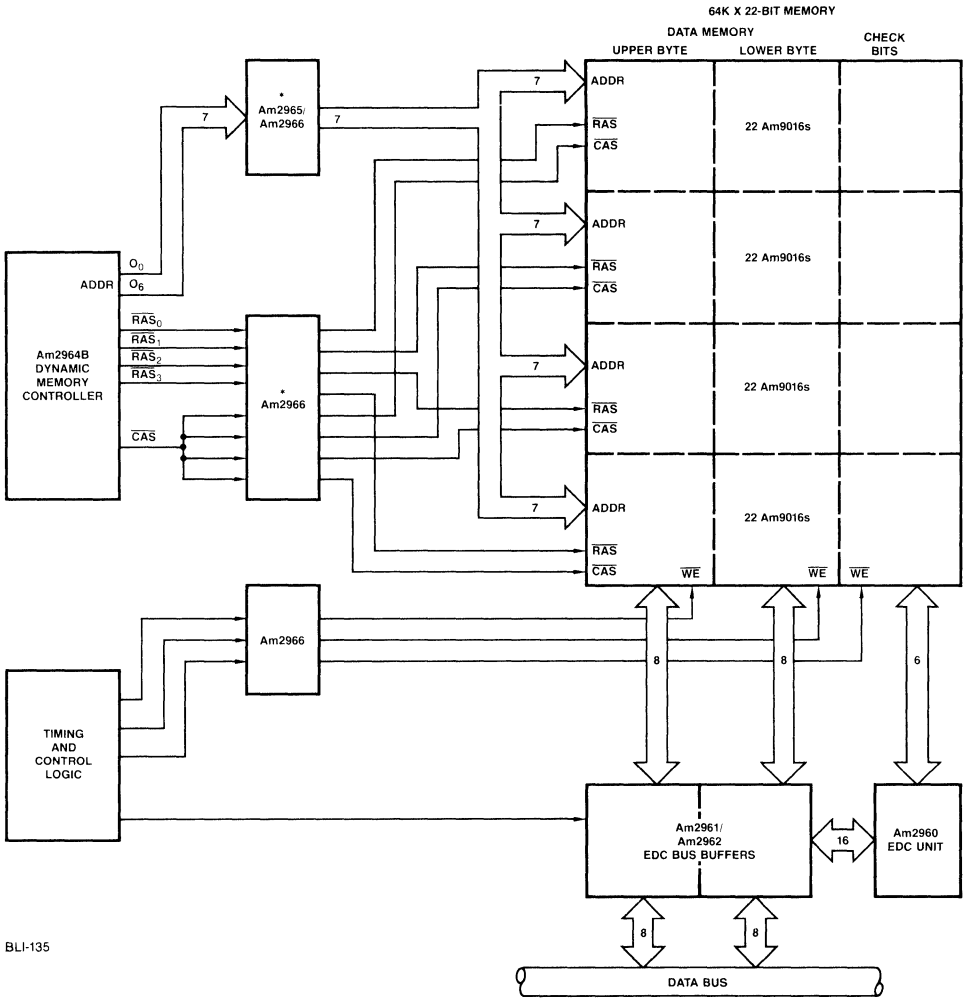


Figure 6. t_{PHL} for V_{OL} = 0.8 Volts vs. C_L.

The curves above depict the typical tPLH and tPHL for the RAM Driver outputs as a function of load capacitance. The minimums and maximums are shown for worst case design. The typical band is provided as a guide for intermediate capacitive loads.

APPLICATION

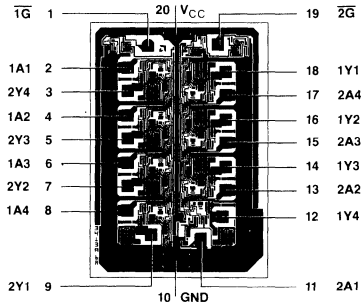


*Address and $\overline{RAS}/\overline{CAS}$ drivers each drive 22 RAM inputs at each output. Timing skew is minimized by using one device for address lines and one device for $\overline{RAS}/\overline{CAS}$, spreading the $\overline{CAS}$ loading over four drivers to equalize the capacitive load on each driver.

DYNAMIC MEMORY CONTROL WITH ERROR DETECTION AND CORRECTION

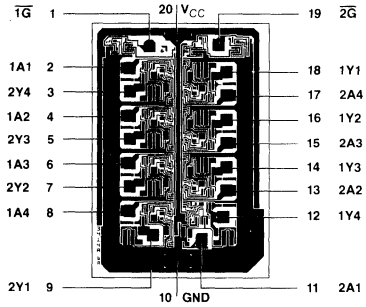
Metallization and Pad Layouts

Am2965



DIE SIZE 0.094" X 0.060"

Am2966



DIE SIZE 0.094" X 0.066"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2965 Order Number	Am2966 Order Number	Package Type	Temperature Range	Screening Level
AM2965PC	AM2966PC	P-20	C	C-1
AM2965DC	AM2966DC	D-20	C	C-1
AM2965DCB	AM2966DCB	D-20	C	B-1
AM2965DM	AM2966DM	D-20	M	C-3
AM2965DMB	AM2966DMB	D-20	M	B-3
AM2965FM	AM2966FM	F-20	M	C-3
AM2965FMB	AM2966FMB	F-20	M	B-3
AM2965XC	AM2966XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2965XM	AM2966XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flatpak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless othewise specified.
2. C = 0 to 70°C, V_{CC} = 4.50V to 5.50V, M = −55 to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2965 • Am2966

DYNAMIC MEMORY DRIVERS IMPROVE MEMORY PERFORMANCE

By John Mick and Roy Levy

OVERVIEW

The Am2965 and Am2966 are bipolar octal drivers for 16K and 64K dynamic RAMs. The devices offer a guaranteed maximum undershoot of −0.5V without requiring external resistors. The Am2965 and Am2966 feature a t_{PD} minimum and maximum specified at 50pF and 500pF. The V_{OH} is guaranteed at V_{CC} −1.15V minimum, and I_{OH} and I_{OL} are specified at +2.0V for minimum guarantee of charging capacitance. There are glitch-free three-state outputs during power-up and power-down as well as symmetrical, controlled rise time and fall time.

While the Am2965 and Am2966 have low-power Schottky input characteristics and are pin-compatible replacement for design using the 'S240 and 'S244 (plus external resistors), the Am2965/2966 offer improved performance. The cost of the components is also comparable to Schottky buffer/external resistor systems.

To assure product quality, the Am2965 and Am2966 are specified for COM'L and MIL-STD-883.

INTRODUCTION

In the past, memory system designers have used Schottky devices such as the Am74S240 or Am74S244 to drive the highly capacitive inputs of MOS Dynamic RAMs. However, because of the distributed inductance and distributed capacitance associated with many dynamic RAMs on printed circuit board, resistors are usually placed in series with the Schottky TTL outputs to minimize undershoot and dampen the ringing that occurs when driving the inductive/capacitive load.

To achieve maximum performance in today's memory systems, the designer should use the Am2965 or the Am2966 to drive large arrays of MOS Dynamic RAMs. These devices increase system speed by providing high-capacity drive and optimizing the drive characteristic time constant. They provide a new system solution for solving these problems that eliminates the external resistor and guarantees the maximum undershoot will not exceed −0.5V.

The address lines on most dynamic RAMs are specified at 5pF maximum while the $\overline{RAS}$, write enable ($\overline{WE}$) and $\overline{CAS}$ inputs can be as high as 10pF. Thus the RAM driver's output must drive extremely high capacitive levels with good speed and without undershoot. When several dynamic RAMs are put onto a printed circuit board, the traces look inductive, so the result resembles a transmission line with distributed inductance and capacitance.

More than 0.5V of undershoot at the RAM inputs can create serious memory system problems by causing internal breakdown and loss of data in RAM chips and possibly damaging the RAM.

System designers must also maintain voltage levels at the RAM inputs. Specifications require the data lines to exceed 2.4V, and the $\overline{RAS}$ and $\overline{CAS}$ lines actually have to exceed 2.7V. Speed must then be maintained while driving all of that capacity.

THE RAM DRIVING PROBLEM

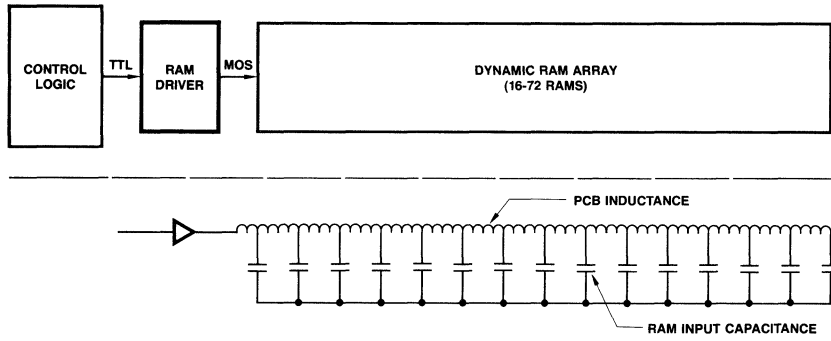
The situation can be pinpointed to an inductor/capacitance driving problem (Figure 1a). There is some inductance in series with the capacitance associated with each RAM input. In a simplified circuit, the inductance is being driven from a voltage having source impedance marked as R_S on Figure 1b. If the transition is LOW-to-HIGH, the voltage goes from LOW-to-HIGH with ringing at the HIGH state (Figure 2). Only above the 2.7V or 2.4V levels, depending upon the type of input, can a steady-state HIGH level be guaranteed on the RAM input. The rise time of the signal is a design consideration, recognizing the amount of capacitance being driven.

Conversely, when the signal drops from HIGH-to-LOW again, ringing can occur. If the ringing causes the voltage to go below ground, it is called undershoot. Figure 3a shows the signal falling to zero volts more quickly than the signal in Fig. 3b, resulting in a severe undershoot that takes longer to settle at the LOW steady state voltage. This delay time associated with the RC time constant is independent of the specification for the HIGH-to-LOW propagation delay time, t_{PHL}. It is a hidden delay that must be compensated for.

VOLTAGE SWING CONSIDERATIONS

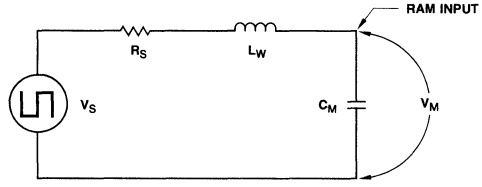
Recognizing that some ringing will occur, the system designer must determine how quickly the signal can be stabilized within the threshold limits of 0.5V below ground and 0.8V above ground. The best way to predict what happens with overshoot and undershoot is to examine the method of driving RAMs. Typically, it is done using one of several Schottky TTL devices connected directly to the RAM. Figure 4a shows an output transistor/resistor structure of a Schottky TTL device. When Q_1 is off and Q_2 is on, the LOW source impedance is about 3 ohms. When Q_2 is off and Q_1 is on, the HIGH impedance is that of the Q_1 transistor and the short circuit R_1. R_1 typically represents about 30-ohm source impedance, so that the source impedance HIGH and source impedance LOW represent a 10-to-1 difference with respect to each other (Figure 4b).

Other TTL devices can be driven in this way, but it is unacceptable for driving RAMs with this type of source impedance for several reasons. First, low source impedance in the LOW states causes ringing by turning on so fast that undershoot results at the RAM inputs. The impedance, however, drives well in the HIGH state. However, to solve the HIGH-to-LOW transition and undershoot problems a resistor is usually placed in series externally between the Schottky TTL gate and the RAM (Figure 4c). The resistor, of about 30 ohms, virtually eliminates undershoot by raising the source impedance in the LOW state to 33 ohms (Q_1 plus R_2).



Objective: Drive the load
- Avoid undershoot
- At MOS voltage levels
- Faster than Schottky

a) The RAM Driver Interface



V_S = the signal driving the chip
R_S = the output resistance of the driving source
L_W = the inductance of the circuit wiring between driving source and memory
C_M = input capacitance of memory chip
V_M = input signal to memory and voltage developed across capacitor

b) Model of Circuit Driving a Memory Chip

Figure 1.

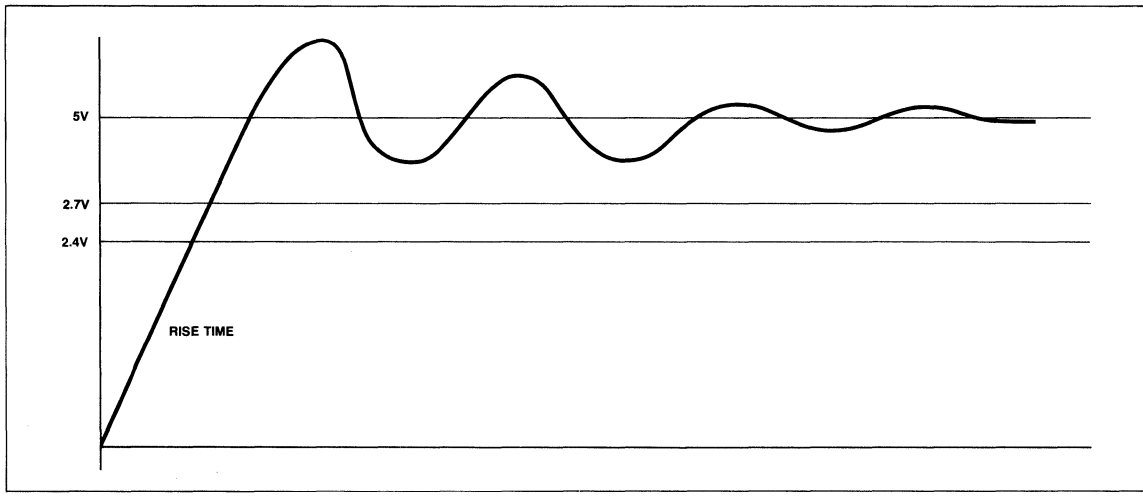


Figure 2. Overshoot in a Rising Signal

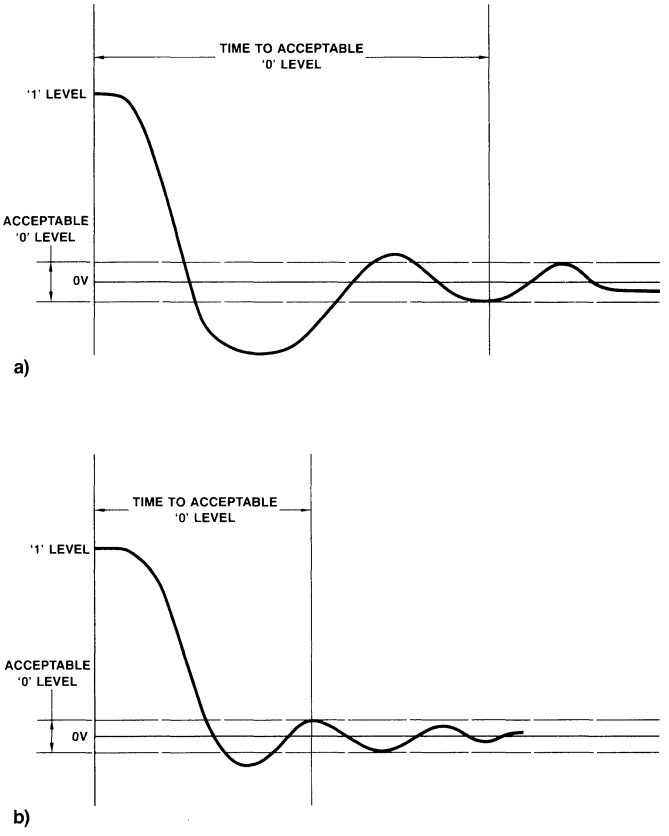


Figure 3. Undershoot in Falling Signals

When the HIGH state is turned on, the 30-ohm external resistor added to the 30-ohm terminal resistor in series totals 60 ohms of source impedance – an amount double of what is needed. While adding the external resistor in series solves undershoot, it causes the rise time (i.e., LOW-to-HIGH transition) to be slowed considerably – probably by a factor of two because resistance is doubled, so the RC time constant is doubled.

The ideal RAM driver source impedance is about 30 ohms in the HIGH state and 20 to 30 ohms in the LOW state (Figure 4d). The Am2965/2966 achieves the ideal RAM driver configuration by having approximately a 20- to 25-ohm source impedance in the LOW state and 25- to 30-ohm source impedance in the HIGH state. This ideal configuration is achieved by including a resistor (R_2) inside the Am2965/66 in series with the collector of Q_2. R_2 adds approximately a 15- to 20-ohm series resistance that has a source impedance in the LOW state of about 20 to 25 ohms and a source impedance in the HIGH state of about 25 to 30 ohms.

Remember, these figures are very nearly what was previously defined as the ideal RAM driver. What results is $R_1 + Q_1$ equivalent resistance in the HIGH state and $R_2 + Q_2$ resistance in the LOW state. The AMD family of RAM driver parts places the resistor inside and only increases the source impedance in the LOW state to achieve the ideal RAM driver configuration shown in Figures 4d and 4e. Now no resistor is needed outside the RAM driver as is typically used with today's Schottky devices.

APPLICATION

Figures 5a and 5b show typical overall memory subsystems for AmZ8000 and 2900 Family CPUs. The subsystems consist of the RAM drivers surrounding the RAMs almost directly; a dynamic memory controller; and interface, timing and controls required to drive the RAMS. There may also be an error detection and correction device as the figure shows.

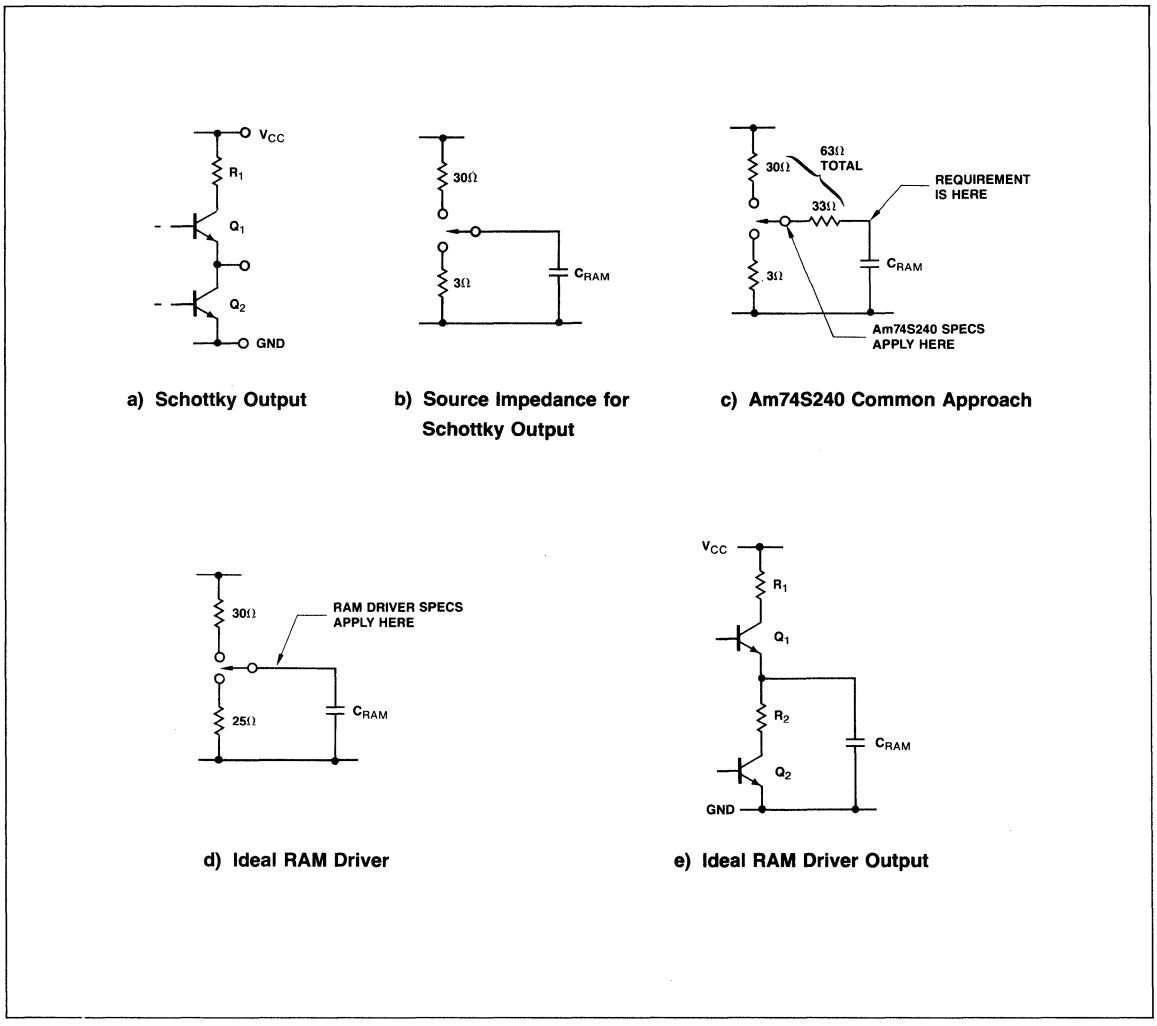
The objective of the memory subsystem is to drive the capacitive RAM inputs as rapidly as possible while meeting all the requirements for the undershoot and threshold levels. Figure 6 shows typical locations for RAM drivers to achieve this goal. Since a majority of the propagation delay times is an RC consideration, design flexibility allows the number of RAM input loads to be chosen for each RAM driver output. The best tradeoff includes fan-out choice and skew consideration. The skew specification for the Am2965 and Am2966 applies across the eight driver outputs but not between different devices.

The memory configuration of Figure 6 consists of an array of four rows by 16 columns of dynamic RAM chips for a total of 64 devices (Figure 7). The address drivers in Figure 6 have 16 x 4 x 5pF maximum = 320 pF (ignoring board capacitance) loading if one RAM driver drives all 64 RAM address inputs. Splitting this load with two RAM drivers reduces the capacitive load for each to 160pF and typically reduces the t_{PD} by 6 to 8nsec.

One of the unique aspects of the design in Figure 7 is the balanced number of loads on the $\overline{RAS}$ outputs of the RAM drivers and the number on loads of the $\overline{CAS}$ outputs of the RAM drivers.

Each driver drives the same number of RAMs. To balance the $\overline{CAS}$ line, the $\overline{CAS}$ inputs of four of the eight buffers are tied together on the RAM driver. Each RAM $\overline{RAS}$ and $\overline{CAS}$ input is 10pF maximum, so the $\overline{RAS}$ and $\overline{CAS}$ loading is 160pF at each RAM driver. The $\overline{CAS}$ inputs of each row are spread across four outputs to match the RAS loading and are shown using the same driver to reduce skew between the $\overline{RAS}$ and the $\overline{CAS}$ signals. The $\overline{WE}$ inputs are organized into upper and lower byte $\overline{WE}$ drive for each of the four rows. This amounts to 8 inputs x 10pF maximum = 80pF loading. By fanning out a full driver to the $\overline{WE}$ lines, four inputs are tied in parallel, balanced loading on the outputs are maintained.

If a full error detection and correction scheme shown in Figure 5 is used, all 22 bits in the row must be written simultaneously so a slightly different $\overline{WE}$ configuration would be used.



a) Schottky Output

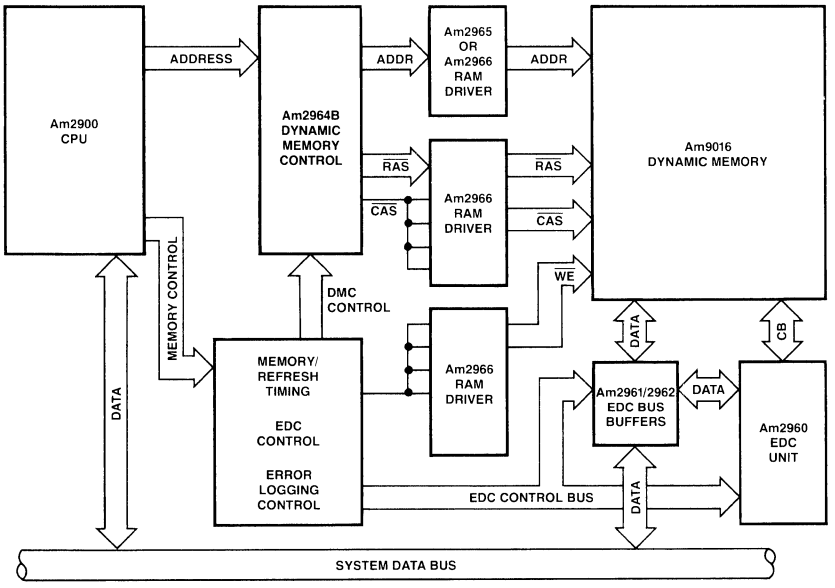
b) Source Impedance for Schottky Output

c) Am74S240 Common Approach

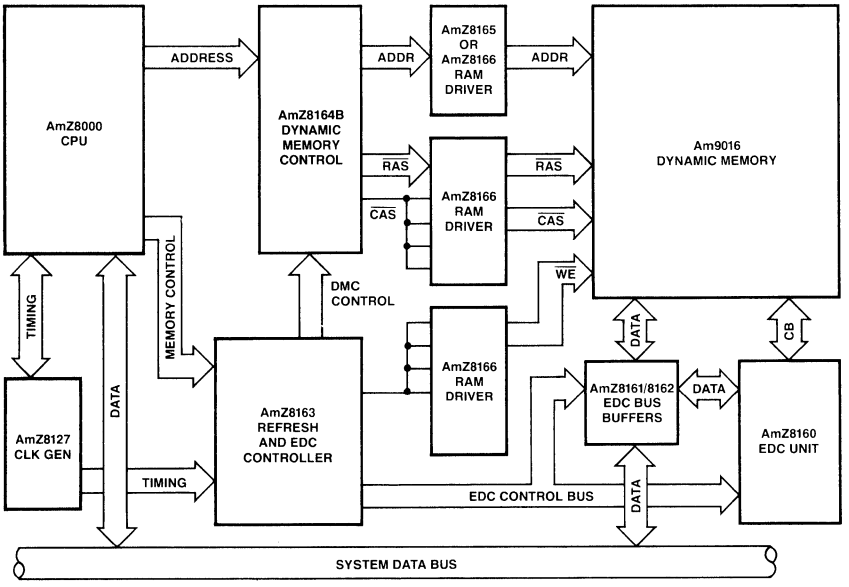
d) Ideal RAM Driver

e) Ideal RAM Driver Output

Figure 4. RAM Drivers vs. Schottky Output



a) High Performance Computer Memory



b) MOS Microcomputer Memory System

Figure 5. Overall Memory Subsystems for the Am2900 and AmZ8000 Family CPUs

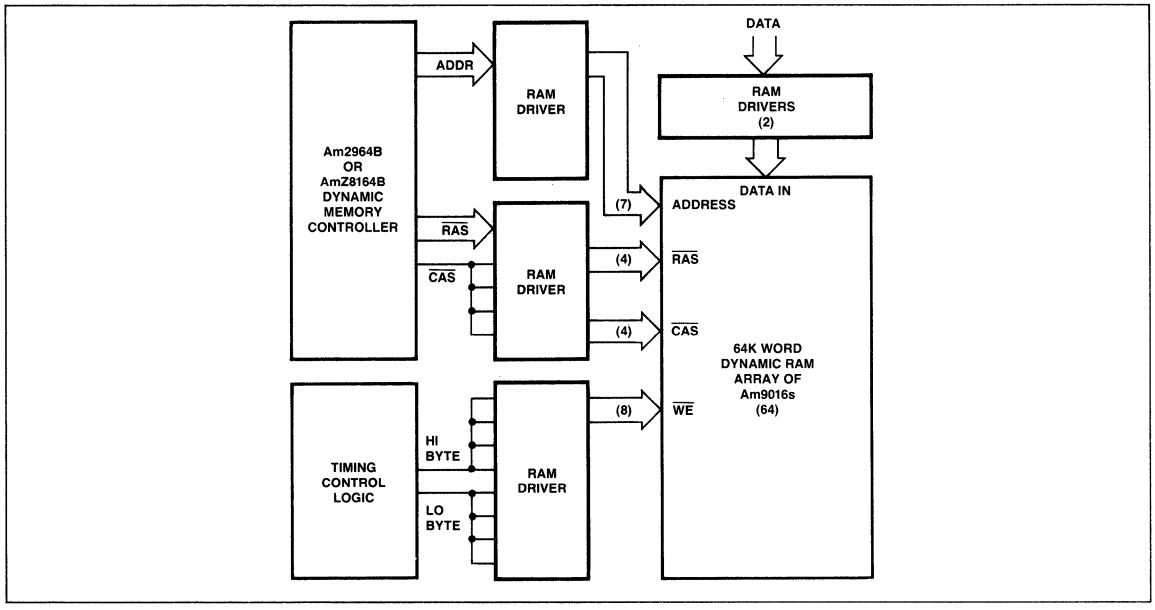


Figure 6. Typical Locations for RAM Drivers

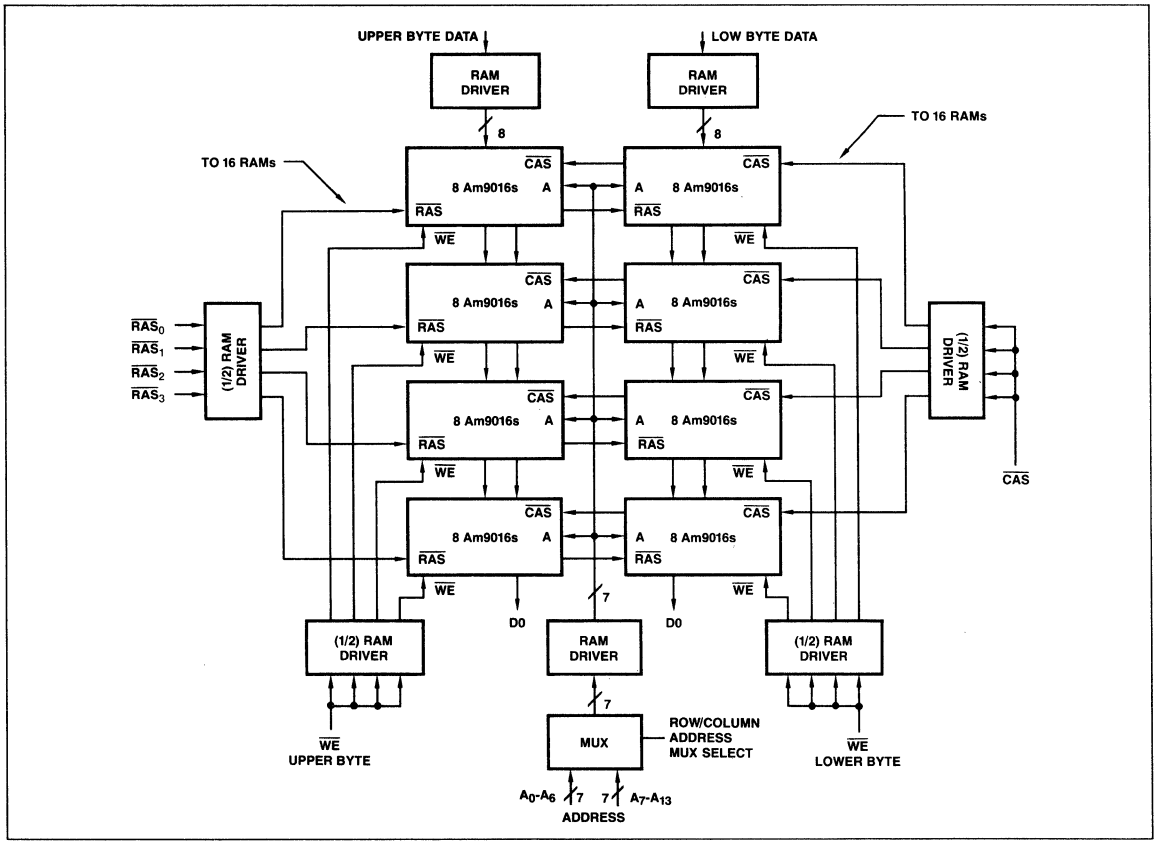


Figure 7. Typical 64K Word by 16-Bit Memory System

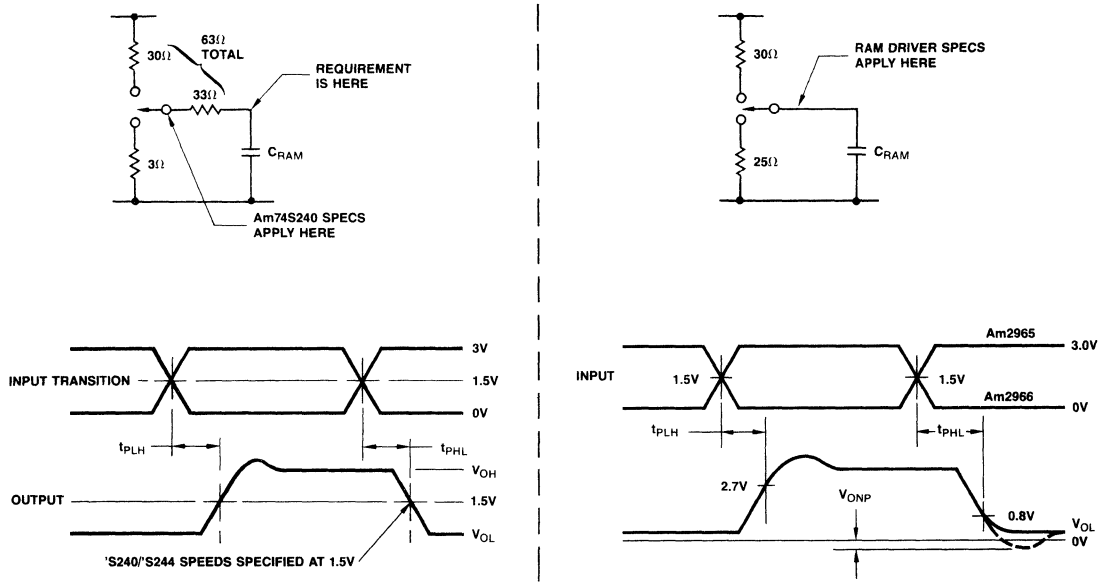
DESIGN ADVANTAGES OF THE Am2965/2966

Compared with Schottky parts such as the Am74S240 or Am74S244, which are used as RAM drivers today, the Am2965/66 RAM drivers offer more advantages than just a RAM driver having no external source resistor.

First, as Figure 8a shows, propagation delays for the Schottky Am74S240 or Am74S244 are measured at 1.5V, which is not where the RAM thresholds are. They are at 0.8V, 2.4V and 2.7V as shown in Figure 8b.

On the Am2965 and Am2966, the LOW-to-HIGH transition voltage propagation delay speeds are measured at 2.7V. Going from HIGH-to-LOW, speed is measured at 0.8V, which is where the actual RAM thresholds are.

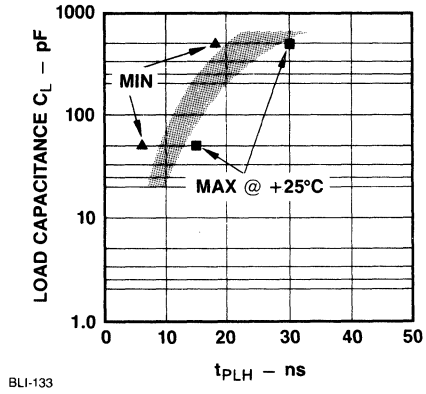
Propagation delays are specified differently, which also makes the Am2965/66 unique (Figure 9). Both minimum and maximum propagation delays are specified at 25°C and 5V. This enables the design engineer to do a worst-case design using both minimum and maximum numbers for the drivers to determine the skew between various drivers. A specified t_{PD} minimum of 50pF and an unusual maximum of 500pF provide a full range of capacitance specifications for both LOW-to-HIGH and HIGH-to-LOW transitions.



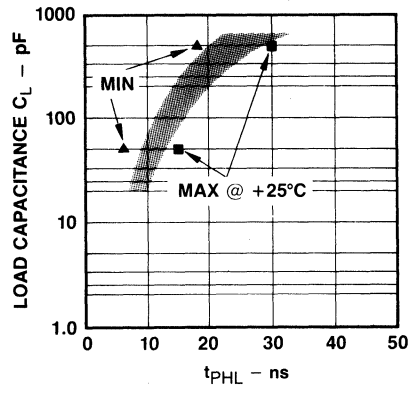
a) Am74S240 Common Approach

b) Ideal RAM Driver

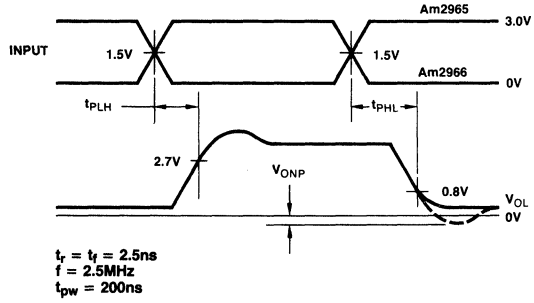
Figure 8. Am2965/66 • AmZ8165/66 Comparison with Am74S240



a) t_{PLH} for V_{OH} = 2.7 Volts vs. C_L



b) t_{PHL} for V_{OL} = 0.8 Volts vs. C_L



c) Output Drive Levels

Figure 9. RAM Driver Propagation Delays

AmZ8163

Dynamic Memory Timing, Refresh and EDC Controller

DISTINCTIVE CHARACTERISTICS

- Complete AmZ8000 CPU to dynamic RAM contol interface
- RAS/CAS Sequencer to eliminate delay lines
- Memory request/refresh arbitration
- Controls for Word/Byte read or write
- Complete EDC data path and mode controls
- Refresh interval timer independent of CPU
- Refresh control during Single Step or Halt modes
- EDC error flag latches for error logging under software control
- Also, complete control for 8-Bit MOS μP

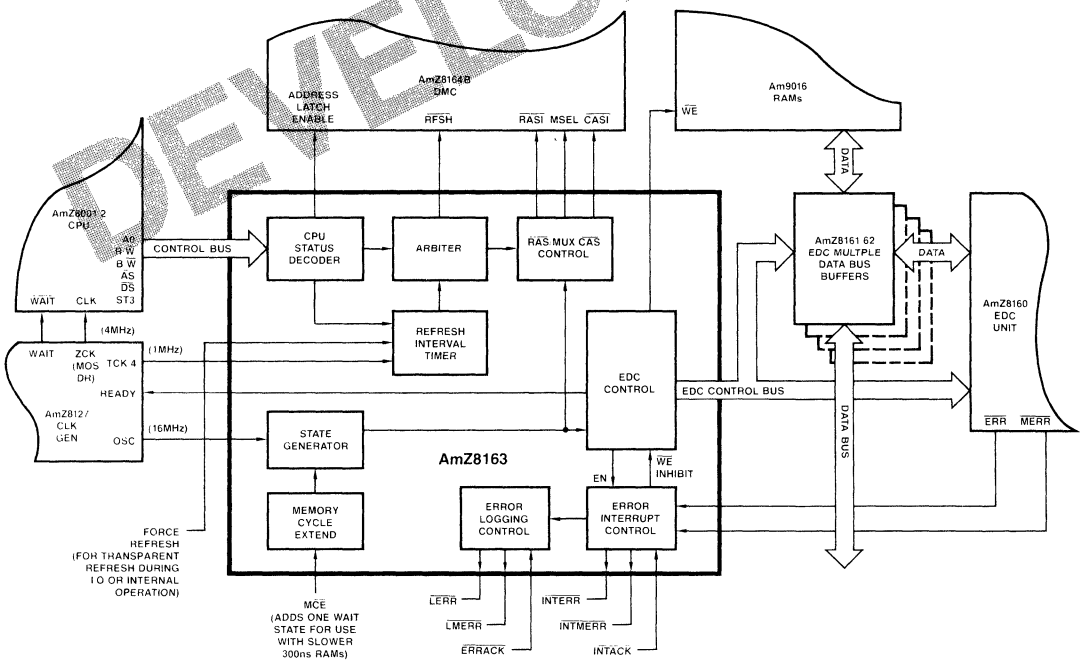
FUNCTIONAL DESCRIPTION

The AmZ8163 is a high speed bus interface controller forming an integral part of the AmZ8000 memory support chip set using dynamic MOS RAMs with Error Detection and Correction (EDC). The complete chip set includes the AmZ8127 Clock Generator and Controller, the AmZ8164 Dynamic Memory Controller, the AmZ8161/2 EDC Bus Buffers, the AmZ8160 EDC Unit and optional AmZ8165/6 RAM Drivers.

The AmZ8163 provides all of the control interface functions including RAS/Address MUX/CAS timing (without delay lines), refresh timing, memory request/refresh arbitration and all EDC enables and controls. The enable controls are configured for both word and byte operations including the data controls for byte write with error correction. The AmZ8163 generates bus and operating mode controls for the AmZ8160 EDC Unit.

The AmZ8163 uses the AmZ8127 16MHz (4 x CLK) output to generate RAS/Address MUX/CAS timing. An internal refresh interval timer generates the memory refresh request independent of the CPU to guarantee the proper refresh timing under all combinations of CPU and DMA memory requests.

FUNCTION DIAGRAM
REFRESH AND EDC CONTROLLER



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Am9016

Extended Operating Temperature Range
16,384 x 1 Dynamic R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

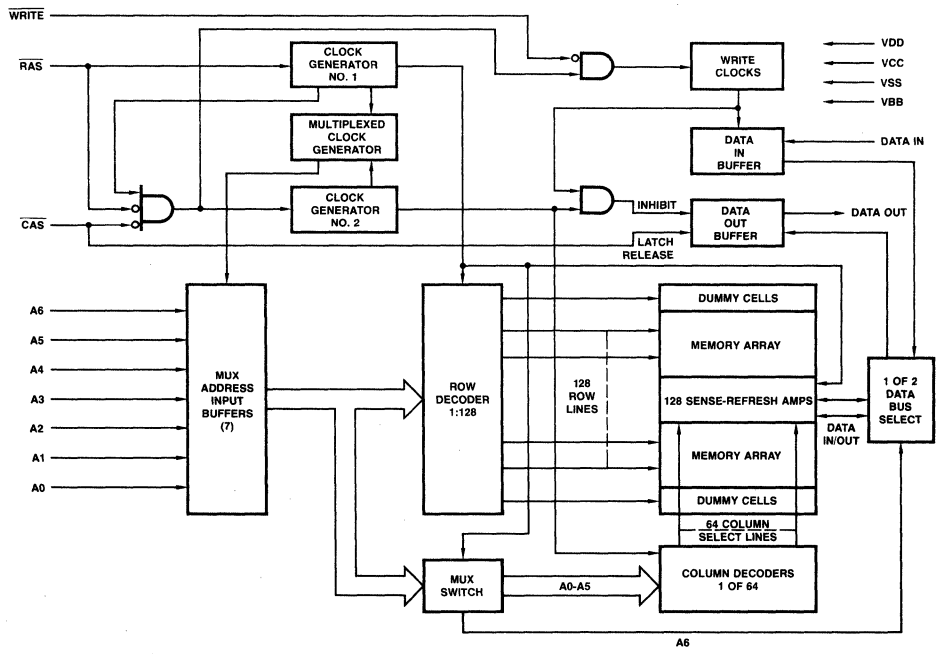
- High density 16K x 1 organization
- Replacement for MK4116 (P)-83/84
- Low maximum power dissipation – 462mW active, 20mW standby
- High speed operation – 200ns access, 375ns cycle
- ±10% tolerance on standard +12, +5, −5 voltages
- TTL compatible interface signals
- Three-state output
- RAS only, RMW and Page mode clocking options
- 128 cycle refreshing
- Unlatched data output
- Standard 16-pin, .3 inch wide dual-in-line package
- Double poly N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing
- Extended ambient operating temperature (−55 to +85°C)

GENERAL DESCRIPTION

The Am9016 is a high-speed, 16K-bit, dynamic, read/write random access memory. It is organized as 16,384 words by 1 bit per word and is packaged in a standard 16-pin DIP or 18-pin leadless chip carrier. The basic memory element is a single transistor cell that stores charge on a small capacitor. This mechanism requires periodic refreshing of the memory cells to maintain stored information.

All input signals, including the two clocks, are TTL compatible. The Row Address Strobe ($\overline{RAS}$) loads the row address and the Column Address Strobe ($\overline{CAS}$) loads the column address. The row and column address signals share seven input lines. Active cycles are initiated when $\overline{RAS}$ goes low, and standby mode is entered when $\overline{RAS}$ goes high. In addition to normal read and write cycles, other types of operations are available to improve versatility, performance and power dissipation.

The 3-state output buffer turns on when the column access time has elapsed and turns off after $\overline{CAS}$ goes high. Input and output data are the same polarity.



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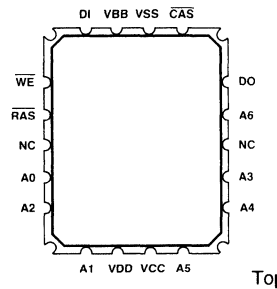
ORDERING INFORMATION

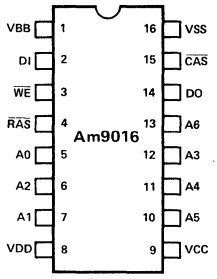
Ambient Temperature	Package Type	Access Time		
		300ns	250ns	200ns
$-55°C \leq T_A \leq +85°C$	Hermetic DIP	AM9016CDL	AM9016DDL	AM9016EDL
	Chip Carrier	AM9016CZL	AM9016DZL	AM9016EZL

CONNECTION DIAGRAMS

Leadless Chip Carrier



DIP



Top Views

A0 – A6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
DI	DATA IN
DO	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
VDD	POWER (+12V)
VCC	POWER (+5V)
VSS	GROUND
VBB	POWER (–5V)
$\overline{WE}$	WRITE ENABLE

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MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	–65 to +150°C
Ambient Temperature Under Bias	–55 to +85°C
Voltage on Any Pin Relative to VBB	–0.5 to +20V
VDD and VCC Supply Voltages with Respect to VSS	–1.0 to +15.0V
VBB – VSS (VDD – VSS > 0V)	0V
Power Dissipation	1.0W
Short Circuit Output Current	50mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Ambient Temperature	VDD	VCC	VSS	VBB
$-55°C \leq T_A \leq +85°C$	+12V ±10%	+5V ±10%	0	–5.0V ±10%

ELECTRICAL CHARACTERISTICS over operating range (Notes 1, 11)

Parameters	Description		Test Conditions	Am9016X Min	Typ	Max	Units
VOH	Output HIGH Voltage		IOH = –5.0mA	2.4		VCC	Volts
VOL	Output LOW Voltage		IOL = 4.2mA	VSS		0.40	Volts
VIH	Input HIGH Voltage for Address, Data In			2.4		7.0	Volts
VIHC	Input HIGH Voltage for $\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$			2.7		7.0	Volts
VIL	Input LOW Voltage			–1.0		0.80	Volts
IIX	Input Load Current		VSS ≤ VI ≤ 7V	–10		10	µA
IOZ	Output Leakage Current		VSS ≤ VO ≤ VCC, Output OFF	–10		10	µA
ICC	VCC Supply Current		Output OFF (Note 4)	–10		10	µA
IBB	VBB Supply Current, Average		Standby, $\overline{RAS} \geq$ VIHC			200	µA
			Operating, Minimum Cycle Time			400	
IDD	VDD Supply Current, Average	Operating IDD1	$\overline{RAS}$ Cycling, $\overline{CAS}$ Cycling, Minimum Cycle Times			35	mA
		Page Mode IDD4	$\overline{RAS} \leq$ VIL, $\overline{CAS}$ Cycling, Minimum Cycle Times			27	
		$\overline{RAS}$ – Only Refresh IDD3	$\overline{RAS}$ Cycling, $\overline{CAS} \geq$ VIHC, Minimum Cycle Times			27	
		Standby IDD2	$\overline{RAS} \geq$ VIHC			2.25	
CI	Input Capacitance	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Inputs at 0V, f = 1MHz, Nominal Supply Voltages			10.0	pF
		Address, Data In				5.0	
CO	Output Capacitance		Output OFF			7.0	

SWITCHING CHARACTERISTICS over operating range (Notes 2, 3, 5, 10)

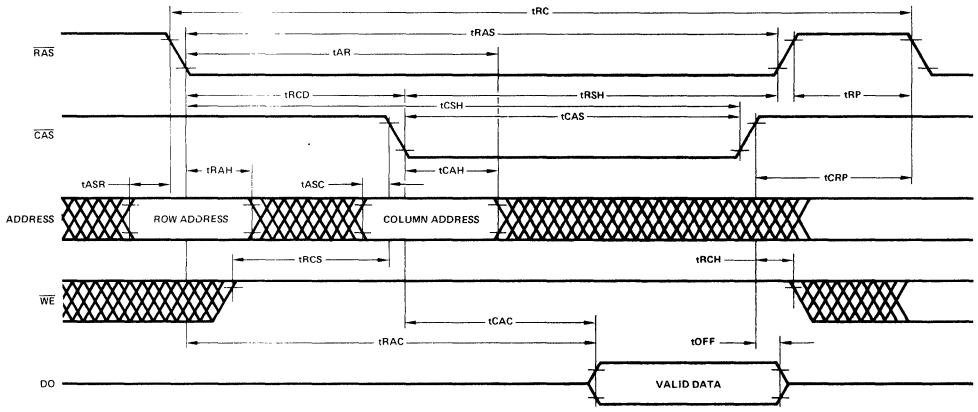
Parameters	Description	Am9016C Min	Am9016C Max	Am9016D Min	Am9016D Max	Am9016E Min	Am9016E Max	Units
tAR	$\overline{RAS}$ LOW to Column Address Hold Time	200		160		120		ns
tASC	Column Address Set-up Time	0		0		0		ns
tASR	Row Address Set-up Time	0		0		0		ns
tCAC	Access Time from $\overline{CAS}$ (Note 6)		185		165		135	ns
tCAH	$\overline{CAS}$ LOW to Column Address Hold Time	85		75		55		ns
tCAS	$\overline{CAS}$ Pulse Width	185	5,000	165	5,000	135	5,000	ns
tCP	Page Mode $\overline{CAS}$ Precharge Time	100		100		80		ns
tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		ns
tCSH	$\overline{CAS}$ Hold Time	300		250		200		ns
tCWD	$\overline{CAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9)	145		125		95		ns
tCWL	$\overline{WE}$ LOW to $\overline{CAS}$ HIGH Set-up Time	100		85		70		ns
tDH	$\overline{CAS}$ LOW or $\overline{WE}$ LOW to Data In Valid Hold Time (Note 7)	85		75		55		ns
tDHR	$\overline{RAS}$ LOW to Data In Valid Hold Time	200		160		120		ns
tDS	Data In Stable to $\overline{CAS}$ LOW or $\overline{WE}$ LOW Set-up Time (Note 7)	0		0		0		ns
tOFF	$\overline{CAS}$ HIGH to Output OFF Delay	0	60	0	60	0	50	ns
tPC	Page Mode Cycle Time	295		275		225		ns
tRAC	Access Time from $\overline{RAS}$ (Note 6)		300		250		200	ns
tRAH	$\overline{RAS}$ LOW to Row Address Hold Time	45		35		25		ns
tRAS	$\overline{RAS}$ Pulse Width	300	5,000	250	5,000	200	5,000	ns
tRC	Random Read or Write Cycle Time	460		410		375		ns
tRCD	$\overline{RAS}$ LOW to $\overline{CAS}$ LOW Delay (Note 6)	35	115	35	85	25	65	ns
tRCH	Read Hold Time	0		0		0		ns
tRCS	Read Set-up Time	0		0		0		ns
tREF	Refresh Interval		2		2		2	ms
tRMW	Read Modify Write Cycle Time	600		500		405		ns
tRP	$\overline{RAS}$ Precharge Time	150		150		120		ns
tRSH	$\overline{CAS}$ LOW to $\overline{RAS}$ HIGH Delay	185		165		135		ns
tRWC	Read/Write Cycle Time	525		425		375		ns
tRWD	$\overline{RAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9)	260		210		160		ns
tRWL	$\overline{WE}$ LOW to $\overline{RAS}$ HIGH Set-up Time	100		85		70		ns
tT	Transition Time	3	50	3	50	3	50	ns
tWCH	Write Hold Time	85		75		55		ns
tWCR	$\overline{RAS}$ LOW to Write Hold Time	200		160		120		ns
tWCS	$\overline{WE}$ LOW to $\overline{CAS}$ LOW Set-up Time (Note 9)	0		0		0		ns
tWP	Write Pulse Width	85		75		55		ns

NOTES

1. Typical values are for T_A = 25°C, nominal supply voltages and nominal processing parameters.
2. Signal transition times are assumed to be 5ns. Transition times are measured between specified high and low logic levels.
3. Timing reference levels for both input and output signals are the specified worst-case logic levels.
4. VCC is used in the output buffer only. ICC will therefore depend only on leakage current and output loading. When the output is ON and at a logic high level, VCC is connected to the Data Out pin through an equivalent resistance of approximately 135Ω. In standby mode VCC may be reduced to zero without affecting stored data or refresh operations.
5. Output loading is two standard TTL loads plus 100pF capacitance.
6. Both $\overline{RAS}$ and $\overline{CAS}$ must be low to read data. Access timing will depend on the relative positions of their falling edges. When tRCD is less than the maximum value shown, access time depends on $\overline{RAS}$ and tRAC governs. When tRCD is more than the maximum value shown access time depends on $\overline{CAS}$ and tCAC governs. The maximum value listed for tRCD is shown for reference purposes only and does not restrict operation of the part.
7. Timing reference points for data input set-up and hold times will depend on what type of write cycle is being performed and will be the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
8. At least eight initialization cycles that exercise $\overline{RAS}$ should be performed after power-up and before valid operations are begun.
9. The tWCS, tRWD and tCWD parameters are shown for reference purposes only and do not restrict the operating flexibility of the part. When the falling edge of $\overline{WE}$ follows the falling edge of $\overline{CAS}$ by at most tWCS, the data output buffer will remain off for the whole cycle and an "early write" cycle is defined. When the falling edge of $\overline{WE}$ follows the falling edges of $\overline{RAS}$ and $\overline{CAS}$ by at least tRWD and tCWD respectively, the Data Out from the addressed cell will be valid at the access time and a "read/write" cycle is defined. The falling edge of $\overline{WE}$ may also occur at intermediate positions, but the condition and validity of the Data Out signal will not be known.
10. Switching characteristics are listed in alphabetical order.
11. All voltages referenced to VSS.

SWITCHING WAVEFORMS

READ CYCLE



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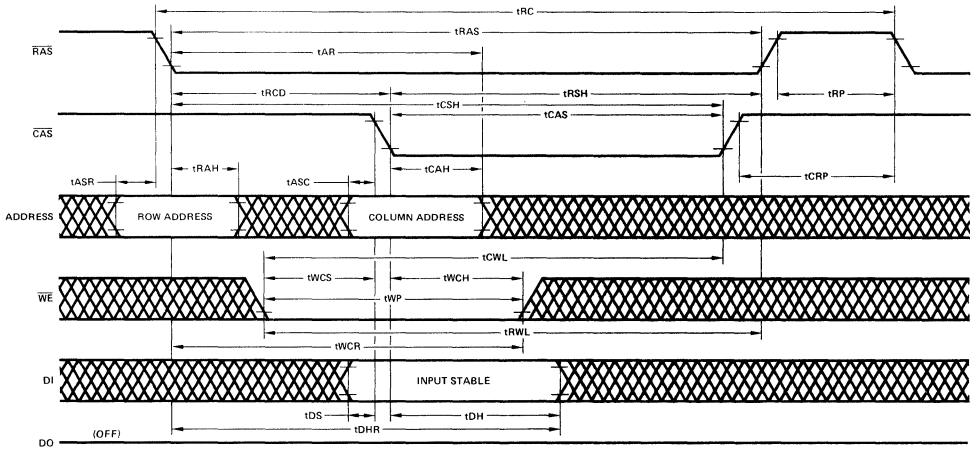
WRITE CYCLE (EARLY WRITE)



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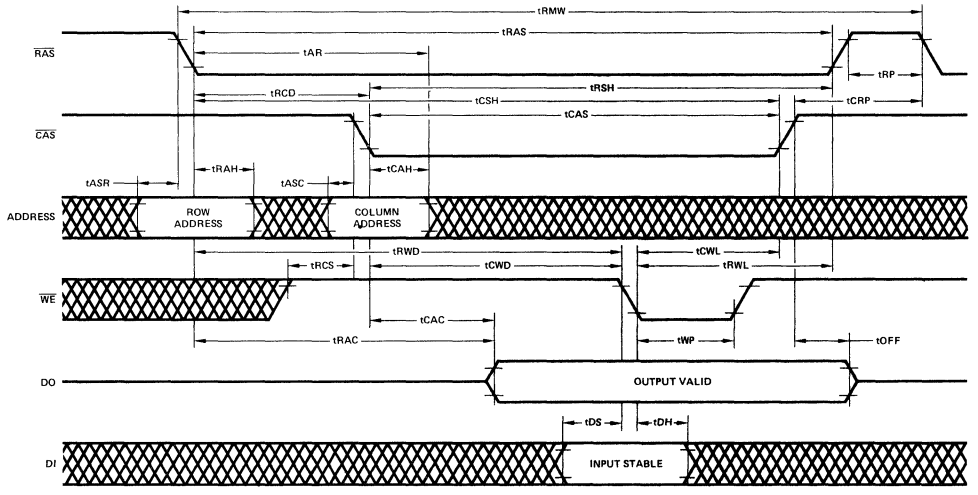
READ-WRITE/READ-MODIFY-WRITE CYCLE



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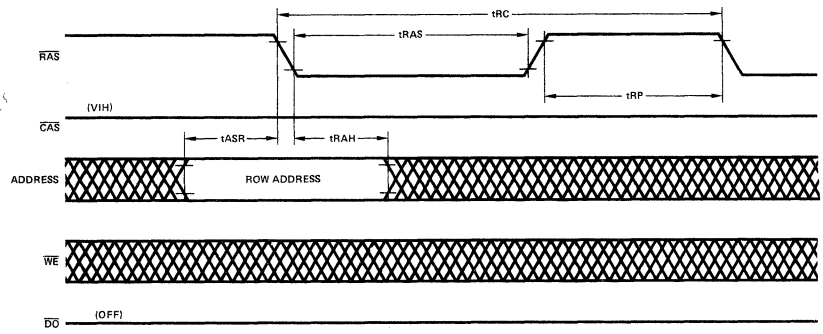
SWITCHING WAVEFORMS (Cont.)

$\overline{RAS}$ ONLY REFRESH CYCLE



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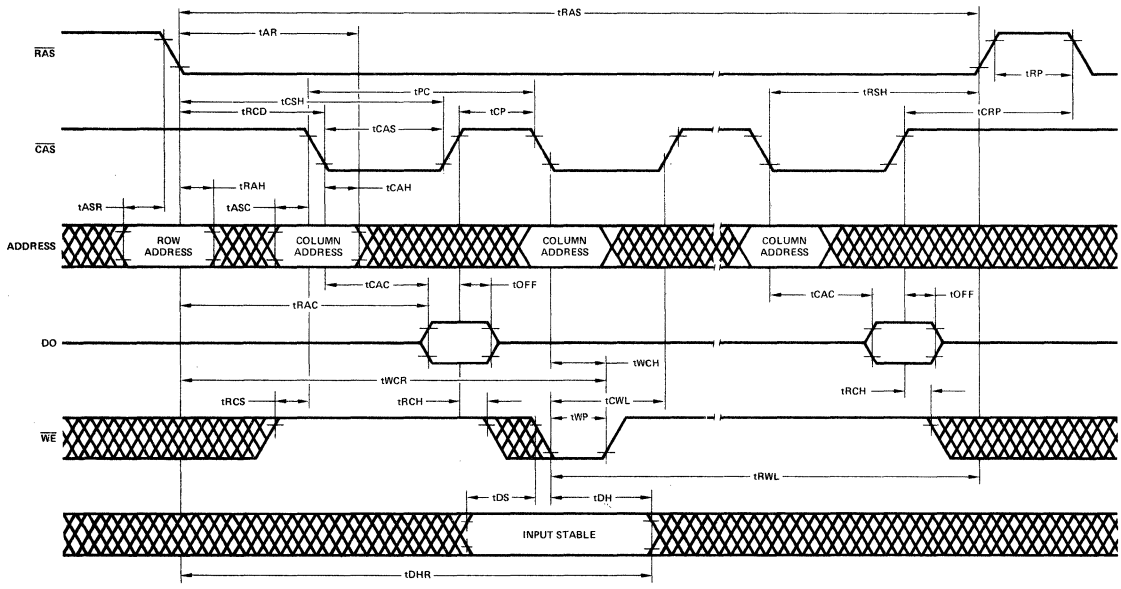
PAGE MODE CYCLE



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APPLICATION INFORMATION

The Am9016 electrical connections are such that if power is applied with the device installed upside down it will be permanently damaged. Precautions should be taken to avoid this mishap.

OPERATING CYCLES

Random read operations from any location hold the $\overline{WE}$ line high and follow this sequence of events:

1) The row address is applied to the address inputs and $\overline{RAS}$ is switched low.
2) After the row address hold time has elapsed, the column address is applied to the address inputs and $\overline{CAS}$ is switched low.
3) Following the access time, the output will turn on and valid read data will be present. The data will remain valid as long as $\overline{CAS}$ is low.
4) $\overline{CAS}$ and $\overline{RAS}$ are then switched high to end the operation. A new cycle cannot begin until the precharge period has elapsed.

Random write operations follow the same sequence of events, except that the $\overline{WE}$ line is low for some portion of the cycle. If the data to be written is available early in the cycle, it will usually be convenient to simply have $\overline{WE}$ low for the whole write operation.

Sequential Read and Write operations at the same location can be designed to save time because re-addressing is not necessary. A read/write cycle holds $\overline{WE}$ high until a valid read is established and then strobes new data in with the falling edge of $\overline{WE}$.

After the power is first applied to the device, the internal circuit requires execution of at least eight initialization cycles which exercise $\overline{RAS}$ before valid memory accesses are begun.

ADDRESSING

14 address bits are required to select one location out of the 16,384 cells in the memory. Two groups of 7 bits each are multiplexed onto the 7 address lines and latched into the internal address registers. Two negative-going external clocks are used to control the multiplexing. The Row Address Strobe ($\overline{RAS}$) enters the row address bits and the Column Address Strobe ($\overline{CAS}$) enters the column address bits.

When $\overline{RAS}$ is inactive, the memory enters its low power standby mode. Once the row address has been latched, it need not be changed for successive operations within the same row, allowing high-speed page-mode operations.

Page-mode operations first establish the row address and then maintain $\overline{RAS}$ low while $\overline{CAS}$ is repetitively cycled and designated operations are performed. Any column address within the selected row may be accessed in any sequence. The maximum time that $\overline{RAS}$ can remain low is the factor limiting the number of page-mode operations that can be performed.

Multiplexed addressing does not introduce extra delays in the access path. By inserting the row address first and the column address second, the memory takes advantage of the fact that the delay path through the memory is shorter for column addresses. The column address does not propagate through the cell matrix as the row address does and it can therefore arrive somewhat later than the row address without impacting the access time.

REFRESH

The Am9016 is a dynamic memory and each cell must be refreshed at least once every refresh interval in order to maintain the cell contents. Any operation that accesses a row serves to refresh all 128 cells in the row. Thus the refresh requirement is met by accessing all 128 rows at least once every refresh interval. This may be accomplished, in some applications, in the course of performing normal operations. Alternatively, special refresh operations may be initiated. These special operations could be simply additional conventional accesses or they could be "$\overline{RAS}$-only" cycles. Since only the rows need to be addressed, $\overline{CAS}$ may be held high while $\overline{RAS}$ is cycled and the appropriate row addresses are input. Power required for refreshing is minimized and simplified control circuitry will often be possible.

DATA INPUT/OUTPUT

Data is written into a selected cell by the combination of $\overline{WE}$ and $\overline{CAS}$ while $\overline{RAS}$ is low. The later negative transition of $\overline{WE}$ or $\overline{CAS}$ strobes the data into the internal register. In a write cycle, if the $\overline{WE}$ input is brought low prior to $\overline{CAS}$, the data is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the cycle is a read/write cycle then the data set-up and hold times are referenced to the negative edge of $\overline{WE}$.

In the read cycle the data is read by maintaining $\overline{WE}$ in the high state throughout the portion of the memory cycle in which $\overline{CAS}$ is low. The selected valid data will appear at the output within the specified access time.

DATA OUTPUT CONTROL

Any time $\overline{CAS}$ is high the data output will be off. The output contains either one or zero during read cycle after the access time has elapsed. Data remains valid from the access time until $\overline{CAS}$ is returned to the high state. The output data is the same polarity as the input data.

The user can control the output state during write operations by controlling the placement of the $\overline{WE}$ signal. In the "early write" cycle (see note 9) the output is at a high impedance state throughout the entire cycle.

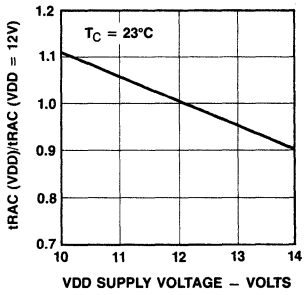
POWER CONSIDERATIONS

$\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the Am9016 but overall system power is minimized if $\overline{RAS}$ is used for this purpose. The devices which do not receive $\overline{RAS}$ will be in low power standby mode regardless of the state of $\overline{CAS}$.

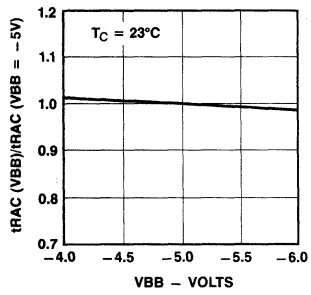
At all times the Absolute Maximum Rating Conditions must be observed. During power supply sequencing VBB should never be more positive than VSS when power is applied to VDD.

TYPICAL CHARACTERISTICS

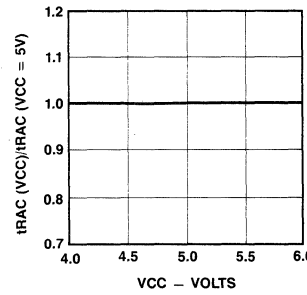
Typical Access Time (Normalized) tRAC Versus VDD



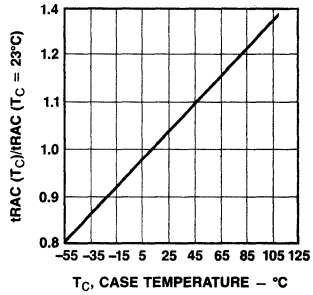
Typical Access Time (Normalized) tRAC Versus VBB



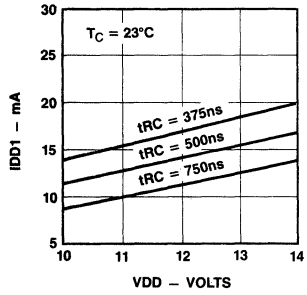
Typical Access Time (Normalized) tRAC Versus VCC



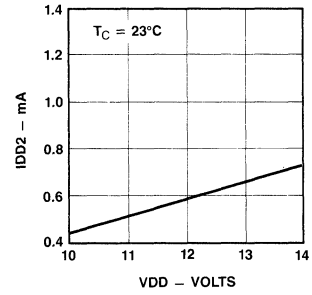
Typical Access Time (Normalized) tRAC Versus Case Temperature



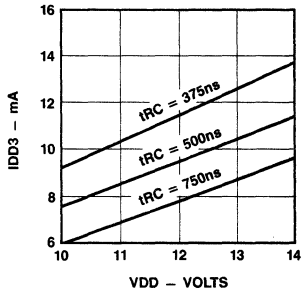
Typical Operating Current IDD1 Versus VDD



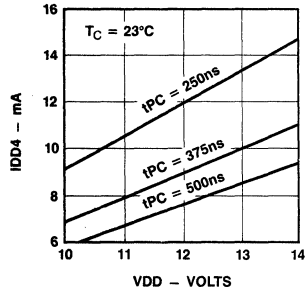
Typical Standby Current IDD2 Versus VDD



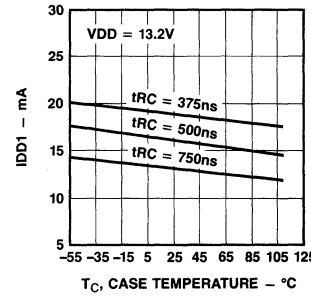
Typical Refresh Current IDD3 Versus VDD



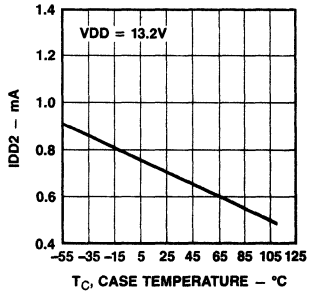
Typical Page Mode Current IDD4 Versus VDD



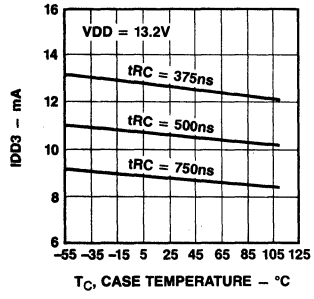
Typical Operating Current IDD1 Versus Case Temperature



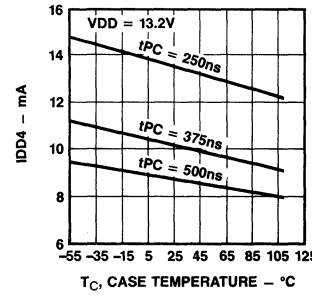
Typical Standby Current IDD2 Versus Case Temperature



Typical Refresh Current IDD3 Versus Case Temperature



Typical Page Mode Current IDD4 Versus Case Temperature



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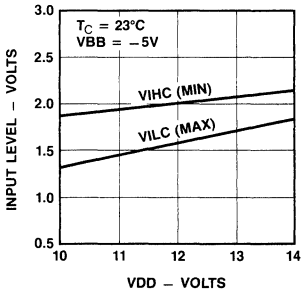
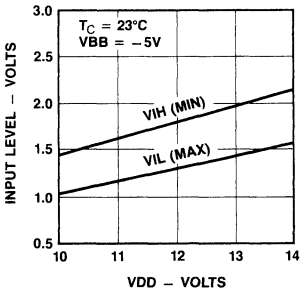
TYPICAL CHARACTERISTICS (Cont.)

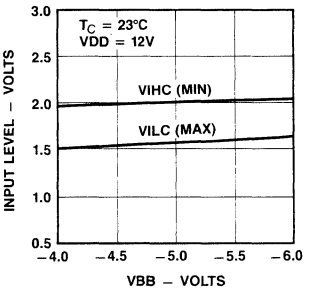
Input Voltage Levels Versus VDD



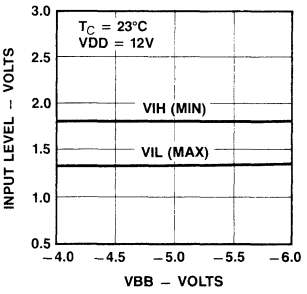
Input Voltage Levels Versus VDD



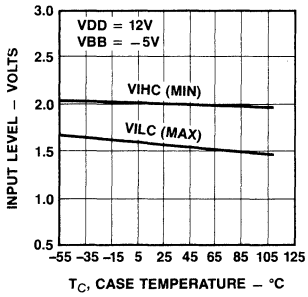
Input Voltage Levels Versus VBB



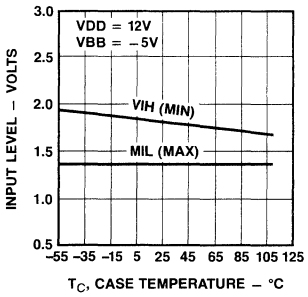
Input Voltages Levels Versus VBB



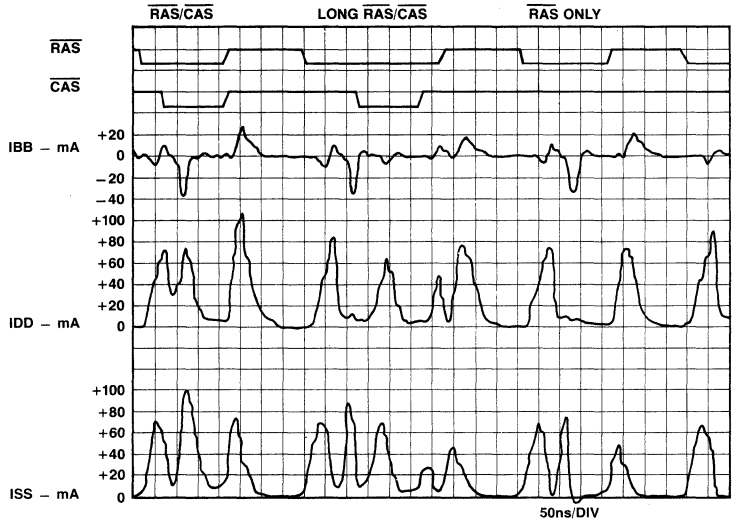
Input Voltage Levels Versus Case Temperature



Input Voltage Levels Versus Case Temperature



TYPICAL CURRENT WAVEFORMS



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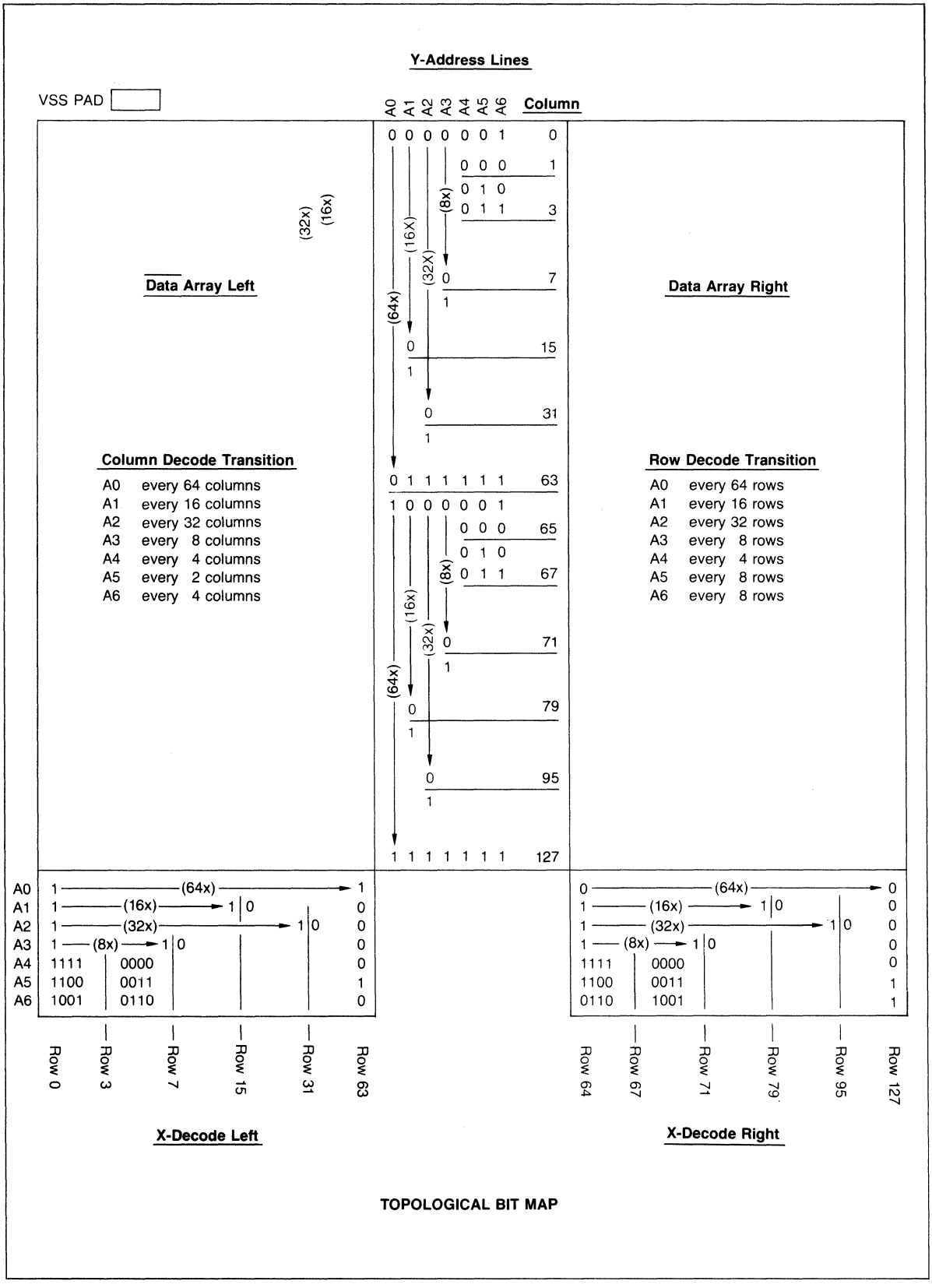
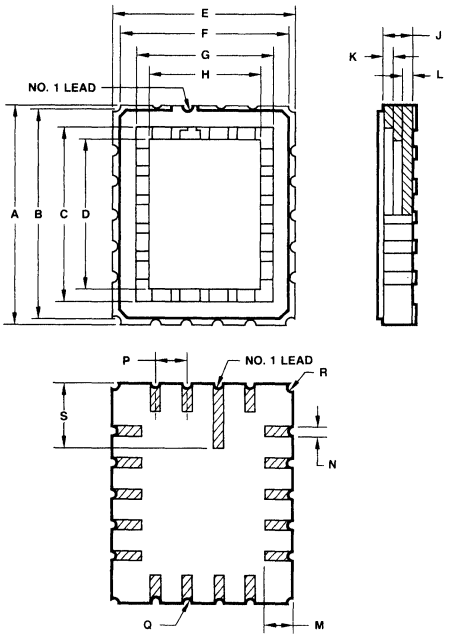


TOPOLOGICAL BIT MAP

PHYSICAL DIMENSIONS

18-Pin Leadless Chip Carrier

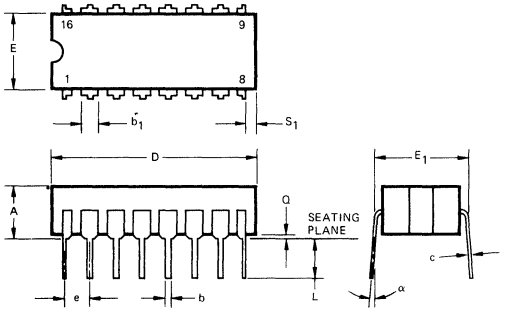


Reference Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.350	.360	8.89	9.14	
B	.330	.340	8.38	8.64	
C	.275	.285	6.99	7.24	
D	.235	.245	5.97	6.22	
E	.285	.295	7.24	7.37	
F	.265	.275	6.73	6.99	
G	.210	.220	5.33	5.59	
H	.170	.180	4.32	4.57	
J	.042	.048	1.07	1.22	
K	.012	.018	0.33	0.46	
L	.012	.018	0.33	0.46	
M	.040	.050	1.02	1.27	
N	.020	.030	0.51	0.76	5
P	.045	.055	1.14	1.40	2
Q	.008R		0.20R		5
R	.012R		0.30R		3
S	.090	.110	2.29	2.79	1

Notes:

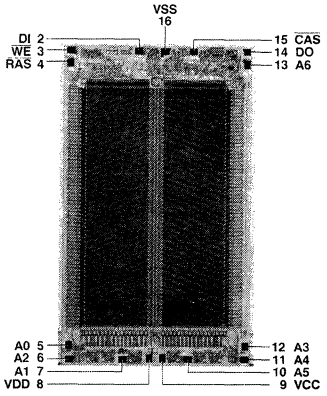
1. Index area: A notch, identification mark or elongation shall be used to identify pin 1.
2. 14 spaces.
3. Applies to all four corners.
4. Shaded areas are metallized to facilitate external connections.
5. 18 locations.
6. No organic or polymeric materials shall be molded to the package.

16-Pin Hermetic



Reference Symbol	Inches	
	Min	Max
A	.130	.200
b	.016	.020
b_1	.050	.070
c	.009	.011
D	.745	.785
E	.240	.310
E_1	.290	.320
e	.090	.110
L	.125	.150
Q	.015	.060
S_1	.005	
α	3°	13°
Standard Lead Finish	b	

Metallization and Pad Layout



DIE SIZE

0.106" X 0.205"

Am9016

16,384 x 1 Dynamic R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- High density 16k x 1 organization
- Direct replacement for MK4116
- Low maximum power dissipation — 462mW active, 20mW standby
- High speed operation — 150ns access, 320ns cycle
- ±10% tolerance on standard +12, +5, −5 voltages
- TTL compatible interface signals
- Three-state output
- RAS only, RMW and Page mode clocking options
- 128 cycle refreshing
- Unlatched data output
- Standard 16-pin, .3 inch wide dual in-line package
- Double poly N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

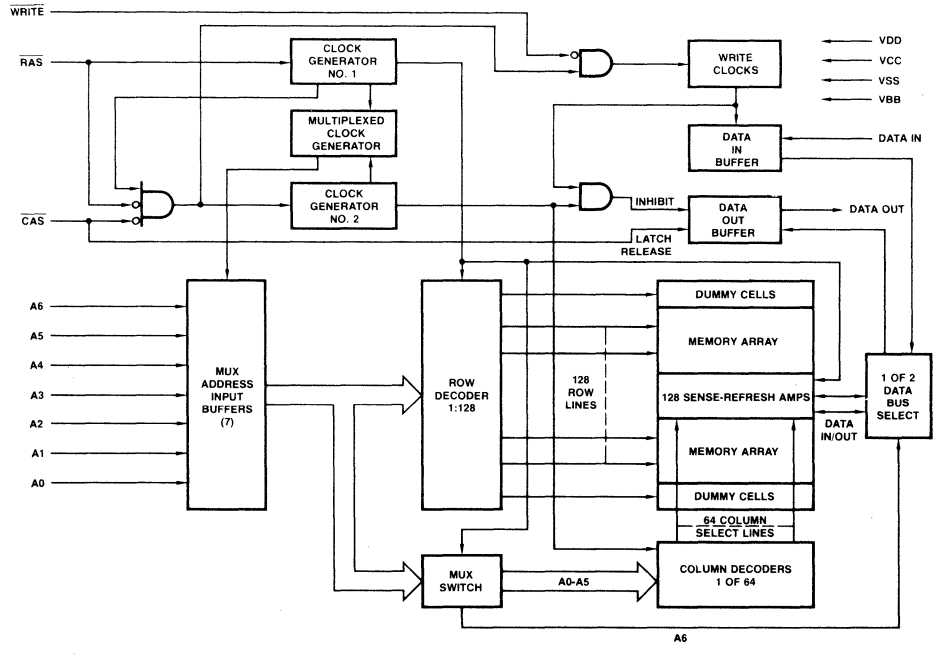
GENERAL DESCRIPTION

The Am9016 is a high speed, 16k-bit, dynamic, read/write random access memory. It is organized as 16,384 words by 1 bit per word and is packaged in a standard 16-pin DIP. The basic memory element is a single transistor cell that stores charge on a small capacitor. This mechanism requires periodic refreshing of the memory cells to maintain stored information.

All input signals, including the two clocks, are TTL compatible. The Row Address Strobe ($\overline{RAS}$) loads the row address and the Column Address Strobe ($\overline{CAS}$) loads the column address. The row and column address signals share 7 input lines. Active cycles are initiated when $\overline{RAS}$ goes low, and standby mode is entered when $\overline{RAS}$ goes high. In addition to normal read and write cycles, other types of operations are available to improve versatility, performance, and power dissipation.

The three-state output buffer turns on when the column access time has elapsed and turns off after $\overline{CAS}$ goes high. Input and output data are the same polarity.

BLOCK DIAGRAM



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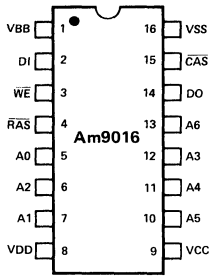
ORDERING INFORMATION

Ambient Temperature	Package Type	Access Time			
		300ns	250ns	200ns	150ns
0°C ≤ T_A ≤ +70°C	Hermetic DIP	AM9016CDC	AM9016DDC	AM9016EDC	AM9016FDC
	Molded DIP	AM9016CPC	AM9016DPC	AM9016EPC	AM9016FPC

CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

A0 – A6	ADDRESS INPUTS
CAS	COLUMN ADDRESS STROBE
DI	DATA IN
DO	DATA OUT
RAS	ROW ADDRESS STROBE
VDD	POWER (+12V)
VCC	POWER (+5V)
VSS	GROUND
VBB	POWER (–5V)
WE	WRITE ENABLE

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MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	–65°C to +150°C
Ambient Temperature Under Bias	0°C to +70°C
Voltage on Any Pin Relative to VBB	–0.5V to +20V
VDD and VCC Supply Voltages with Respect to VSS	–1.0V to +15.0V
VBB – VSS (VDD – VSS > 0V)	0V
Power Dissipation	1.0W
Short Circuit Output Current	50mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulation of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling, and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Ambient Temperature	VDD	VCC	VSS	VBB
$0°C \leq T_A \leq +70°C$	+12V ±10%	+5V ±10%	0	–5.0V ±10%

ELECTRICAL CHARACTERISTICS over operating range (Notes 1, 11)

Parameters	Description			Test Conditions	Am9016X Min.	Typ.	Max.	Units
VOH	Output HIGH Voltage			IOH = –5.0mA	2.4		VCC	Volts
VOL	Output LOW Voltage			IOL = 4.2mA	VSS		0.40	Volts
VIH	Input HIGH Voltage for Address, Data In				2.4		7.0	Volts
VIHC	Input HIGH Voltage for CAS, RAS, WE				2.7		7.0	Volts
VIL	Input LOW Voltage				–1.0		0.80	Volts
IIX	Input Load Current			VSS ≤ VI ≤ 7V	–10		10	µA
IOZ	Output Leakage Current			VSS ≤ VO ≤ VCC, Output OFF	–10		10	µA
ICC	VCC Supply Current			Output OFF (Note 4)	–10		10	µA
IBB	VBB Supply Current, Average			Standby, RAS ≥ VIHC			100	µA
				Operating, Minimum Cycle Time			200	
IDD	VDD Supply Current, Average	Operating	IDD1	RAS Cycling, CAS Cycling, Minimum Cycle Times			35	mA
		Page Mode	IDD4	RAS ≤ VIL, CAS Cycling, Minimum Cycle Times			27	
		RAS Only Refresh	IDD3	RAS Cycling, CAS ≥ VIHC, Minimum Cycle Times			27	
		Standby	IDD2	RAS ≥ VIHC			1.5	
CI	Input Capacitance	RAS, CAS, WE		Inputs at 0V, f = 1MHz, Nominal Supply Voltages			10	pF
		Address, Data In					5.0	
CO	Output Capacitance			Output OFF			7.0	

SWITCHING CHARACTERISTICS over operating range (Notes 2, 3, 5, 10)

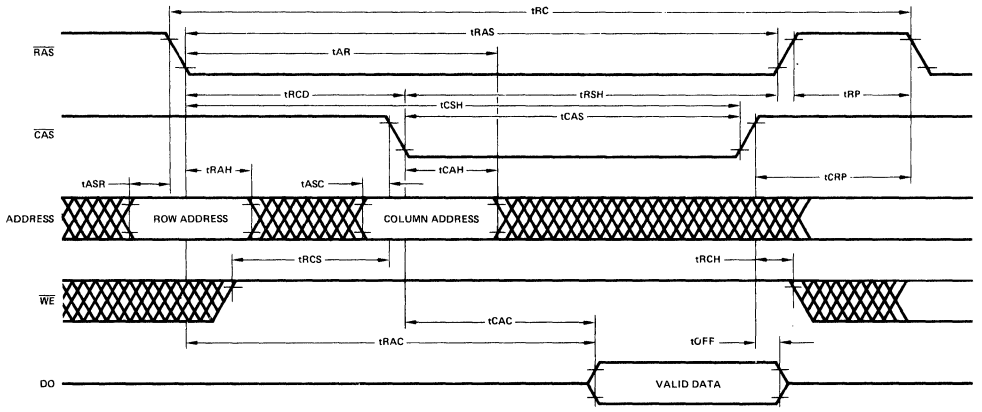
Parameters	Description	Am9016C		Am9016D		Am9016E		Am9016F		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
tAR	$\overline{RAS}$ LOW to Column Address Hold Time	200		160		120		95		ns
tASC	Column Address Set-up Time	−10		−10		−10		−10		ns
tASR	Row Address Set-up Time	0		0		0		0		ns
tCAC	Access Time from $\overline{CAS}$ (Note 6)		185		165		135		100	ns
tCAH	$\overline{CAS}$ LOW to Column Address Hold Time	85		75		55		45		ns
tCAS	$\overline{CAS}$ Pulse Width	185	10,000	165	10,000	135	10,000	100	10,000	ns
tCP	Page Mode $\overline{CAS}$ Precharge Time	100		100		80		60		ns
tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		−20		−20		ns
tCSH	$\overline{CAS}$ Hold Time	300		250		200		150		ns
tCWD	$\overline{CAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9)	145		125		95		70		ns
tCWL	$\overline{WE}$ LOW to $\overline{CAS}$ HIGH Set-up Time	100		85		70		50		ns
tDH	$\overline{CAS}$ LOW or $\overline{WE}$ LOW to Data In Valid Hold Time (Note 7)	85		75		55		45		ns
tDHR	$\overline{RAS}$ LOW to Data In Valid Hold Time	200		160		120		95		ns
tDS	Data In Stable to $\overline{CAS}$ LOW or $\overline{WE}$ LOW Set-up Time (Note 7)	0		0		0		0		ns
tOFF	$\overline{CAS}$ HIGH to Output OFF Delay	0	60	0	60	0	50	0	40	ns
tPC	Page Mode Cycle Time	295		275		225		170		ns
tRAC	Access Time from $\overline{RAS}$ (Note 6)		300		250		200		150	ns
tRAH	$\overline{RAS}$ LOW to Row Address Hold Time	45		35		25		20		ns
tRAS	$\overline{RAS}$ Pulse Width	300	10,000	250	10,000	200	10,000	150	10,000	ns
tRC	Random Read or Write Cycle Time	460		410		375		320		ns
tRCD	$\overline{RAS}$ LOW to $\overline{CAS}$ LOW Delay (Note 6)	35	115	35	85	25	65	20	50	ns
tRCH	Read Hold Time	0		0		0		0		ns
tRCS	Read Set-up Time	0		0		0		0		ns
tREF	Refresh Interval		2		2		2		2	ms
tRMW	Read Modify Write Cycle Time	600		500		405		320		ns
tRP	RAS Precharge Time	150		150		120		100		ns
tRSH	$\overline{CAS}$ LOW to $\overline{RAS}$ HIGH Delay	185		165		135		100		ns
tRWC	Read/Write Cycle Time	525		425		375		320		ns
tRWD	$\overline{RAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9)	260		210		160		120		ns
tRWL	$\overline{WE}$ LOW to $\overline{RAS}$ HIGH Set-up Time	100		85		70		50		ns
tT	Transition Time	3	50	3	50	3	50	3	35	ns
tWCH	Write Hold Time	85		75		55		45		ns
tWCR	$\overline{RAS}$ LOW to Write Hold Time	200		160		120		95		ns
tWCS	$\overline{WE}$ LOW to $\overline{CAS}$ LOW Set-up Time (Note 9)	−20		−20		−20		−20		ns
tWP	Write Pulse Width	85		75		55		45		ns

NOTES

1. Typical values are for T_A = 25°C, nominal supply voltages and nominal processing parameters.
2. Signal transition times are assumed to be 5ns. Transition times are measured between specified high and low logic levels.
3. Timing reference levels for both input and output signals are the specified worst-case logic levels.
4. VCC is used in the output buffer only. ICC will therefore depend only on leakage current and output loading. When the output is ON and at a logic high level, VCC is connected to the Data Out pin through an equivalent resistance of approximately 135Ω. In standby mode VCC may be reduced to zero without affecting stored data or refresh operations.
5. Output loading is two standard TTL loads plus 100pF capacitance.
6. Both $\overline{RAS}$ and $\overline{CAS}$ must be low to read data. Access timing will depend on the relative positions of their falling edges. When tRCD is less than the maximum value shown, access time depends on $\overline{RAS}$ and tRAC governs. When tRCD is more than the maximum value shown access time depends on $\overline{CAS}$ and tCAC governs. The maximum value listed for tRCD is shown for reference purposes only and does not restrict operation of the part.
7. Timing reference points for data input set-up and hold times will depend on what type of write cycle is being performed and will be the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
8. At least eight initialization cycles that exercise $\overline{RAS}$ should be performed after power-up and before valid operations are begun.
9. The tWCS, tRWD and tCWD parameters are shown for reference purposes only and do not restrict the operating flexibility of the part. When the falling edge of $\overline{WE}$ follows the falling edge of $\overline{CAS}$ by at most tWCS, the data output buffer will remain off for the whole cycle and an "early write" cycle is defined. When the falling edge of $\overline{WE}$ follows the falling edges of $\overline{RAS}$ and $\overline{CAS}$ by at least tRWD and tCWD respectively, the Data Out from the addressed cell will be valid at the access time and a "read/write" cycle is defined. The falling edge of $\overline{WE}$ may also occur at intermediate positions, but the condition and validity of the Data Out signal will not be known.
10. Switching characteristics are listed in alphabetical order.
11. All voltages referenced to VSS.

SWITCHING WAVEFORMS

READ CYCLE



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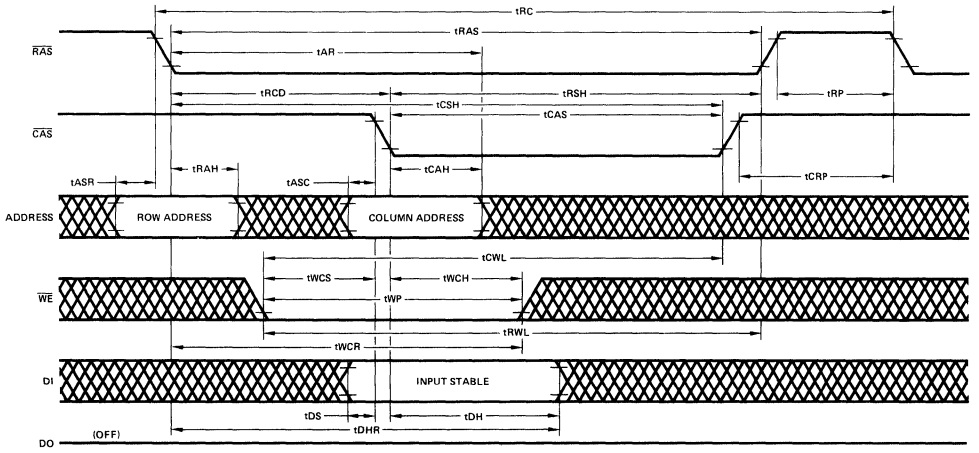
WRITE CYCLE (EARLY WRITE)



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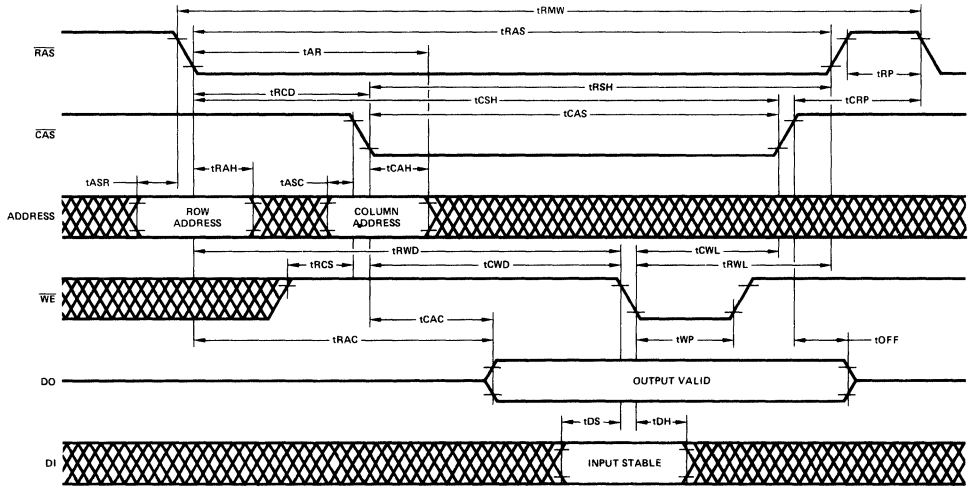
READ-WRITE/READ-MODIFY-WRITE CYCLE



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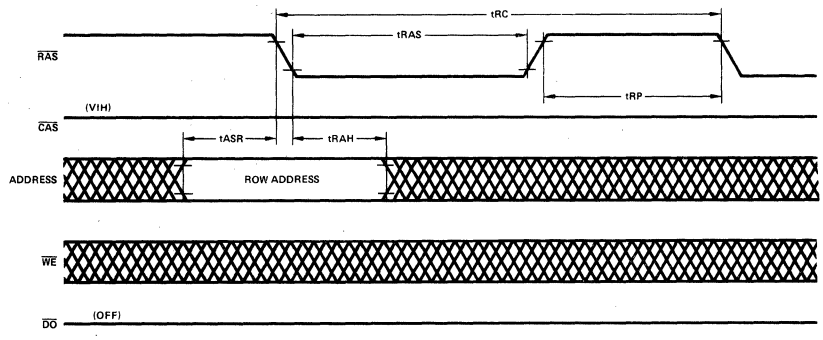
SWITCHING WAVEFORMS (Cont.)

$\overline{RAS}$ ONLY REFRESH CYCLE



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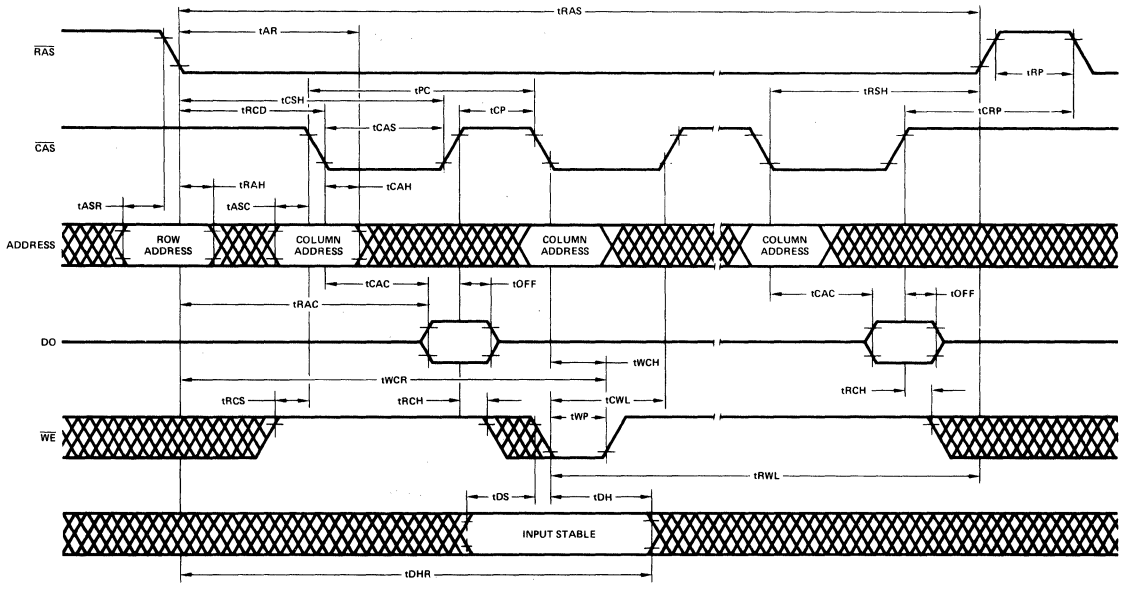
PAGE MODE CYCLE



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APPLICATION INFORMATION

The Am9016 electrical connections are such that if power is applied with the device installed upside down it will be permanently damaged. Precautions should be taken to avoid this mishap.

OPERATING CYCLES

Random read operations from any location hold the $\overline{WE}$ line high and follow this sequence of events:

1) The row address is applied to the address inputs and $\overline{RAS}$ is switched low.
2) After the row address hold time has elapsed, the column address is applied to the address inputs and $\overline{CAS}$ is switched low.
3) Following the access time, the output will turn on and valid read data will be present. The data will remain valid as long as $\overline{CAS}$ is low.
4) $\overline{CAS}$ and $\overline{RAS}$ are then switched high to end the operation. A new cycle cannot begin until the precharge period has elapsed.

Random write operations follow the same sequence of events, except that the $\overline{WE}$ line is low for some portion of the cycle. If the data to be written is available early in the cycle, it will usually be convenient to simply have $\overline{WE}$ low for the whole write operation.

Sequential Read and Write operations at the same location can be designed to save time because re-addressing is not necessary. A read/write cycle holds $\overline{WE}$ high until a valid read is established and then strobes new data in with the falling edge of $\overline{WE}$.

After the power is first applied to the device, the internal circuit requires execution of at least eight initialization cycles which exercise $\overline{RAS}$ before valid memory accesses are begun.

ADDRESSING

14 address bits are required to select one location out of the 16,384 cells in the memory. Two groups of 7 bits each are multiplexed onto the 7 address lines and latched into the internal address registers. Two negative-going external clocks are used to control the multiplexing. The Row Address Strobe ($\overline{RAS}$) enters the row address bits and the Column Address Strobe ($\overline{CAS}$) enters the column address bits.

When $\overline{RAS}$ is inactive, the memory enters its low power standby mode. Once the row address has been latched, it need not be changed for successive operations within the same row, allowing high-speed page-mode operations.

Page-mode operations first establish the row address and then maintain $\overline{RAS}$ low while $\overline{CAS}$ is repetitively cycled and designated operations are performed. Any column address within the selected row may be accessed in any sequence. The maximum time that $\overline{RAS}$ can remain low is the factor limiting the number of page-mode operations that can be performed.

Multiplexed addressing does not introduce extra delays in the access path. By inserting the row address first and the column address second, the memory takes advantage of the fact that the delay path through the memory is shorter for column addresses. The column address does not propagate through the cell matrix as the row address does and it can therefore arrive somewhat later than the row address without impacting the access time.

REFRESH

The Am9016 is a dynamic memory and each cell must be refreshed at least once every refresh interval in order to maintain the cell contents. Any operation that accesses a row serves to refresh all 128 cells in the row. Thus the refresh requirement is met by accessing all 128 rows at least once every refresh interval. This may be accomplished, in some applications, in the course of performing normal operations. Alternatively, special refresh operations may be initiated. These special operations could be simply additional conventional accesses or they could be "$\overline{RAS}$-only" cycles. Since only the rows need to be addressed, $\overline{CAS}$ may be held high while $\overline{RAS}$ is cycled and the appropriate row addresses are input. Power required for refreshing is minimized and simplified control circuitry will often be possible.

DATA INPUT/OUTPUT

Data is written into a selected cell by the combination of $\overline{WE}$ and $\overline{CAS}$ while $\overline{RAS}$ is low. The later negative transition of $\overline{WE}$ or $\overline{CAS}$ strobes the data into the internal register. In a write cycle, if the $\overline{WE}$ input is brought low prior to $\overline{CAS}$, the data is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the cycle is a read/write cycle then the data set-up and hold times are referenced to the negative edge of $\overline{WE}$.

In the read cycle the data is read by maintaining $\overline{WE}$ in the high state throughout the portion of the memory cycle in which $\overline{CAS}$ is low. The selected valid data will appear at the output within the specified access time.

DATA OUTPUT CONTROL

Any time $\overline{CAS}$ is high the data output will be off. The output contains either one or zero during read cycle after the access time has elapsed. Data remains valid from the access time until $\overline{CAS}$ is returned to the high state. The output data is the same polarity as the input data.

The user can control the output state during write operations by controlling the placement of the $\overline{WE}$ signal. In the "early write" cycle (see note 9) the output is at a high impedance state throughout the entire cycle.

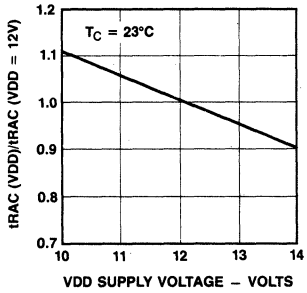
POWER CONSIDERATIONS

$\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the Am9016 but overall system power is minimized if $\overline{RAS}$ is used for this purpose. The devices which do not receive $\overline{RAS}$ will be in low power standby mode regardless of the state of $\overline{CAS}$.

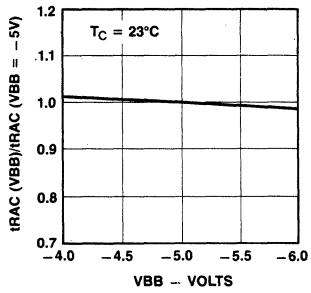
At all times the Absolute Maximum Rating Conditions must be observed. During power supply sequencing VBB should never be more positive than VSS when power is applied to VDD.

TYPICAL CHARACTERISTICS

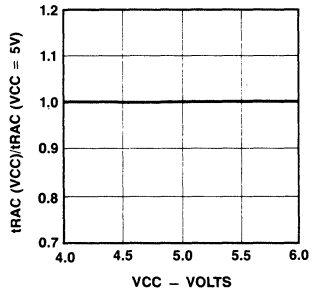
Typical Access Time (Normalized) tRAC Versus VDD



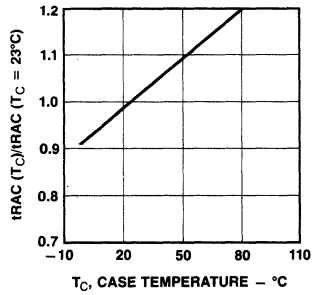
Typical Access Time (Normalized) tRAC Versus VBB



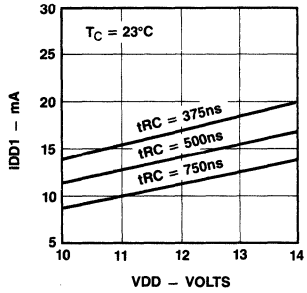
Typical Access Time (Normalized) tRAC Versus VCC



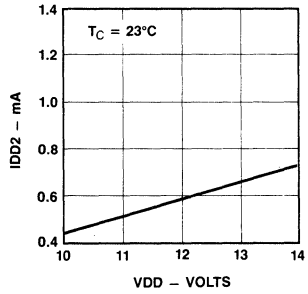
Typical Access Time (Normalized) tRAC Versus Case Temperature



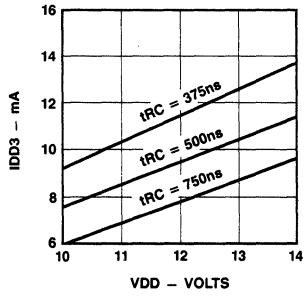
Typical Operating Current IDD1 Versus VDD



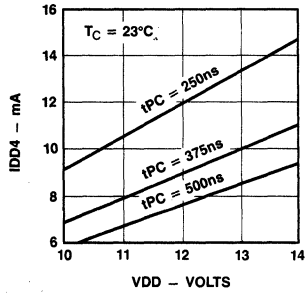
Typical Standby Current IDD2 Versus VDD



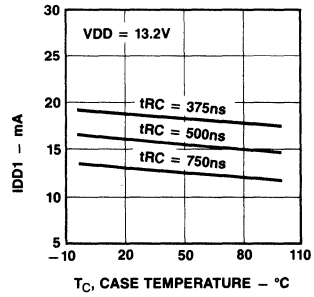
Typical Refresh Current IDD3 Versus VDD



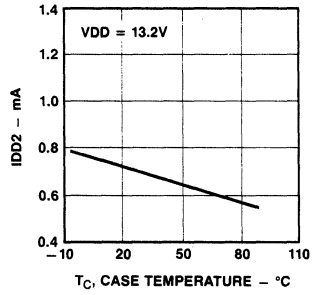
Typical Page Mode Current IDD4 Versus VDD



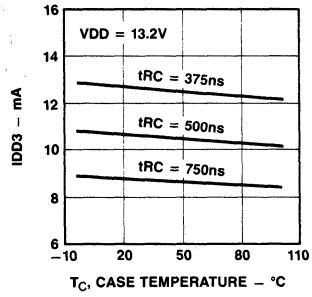
Typical Operating Current IDD1 Versus Case Temperature



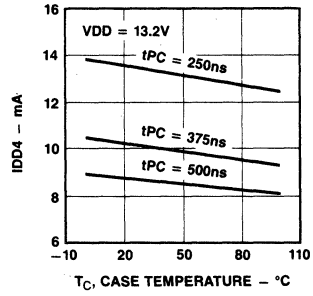
Typical Standby Current IDD2 Versus Case Temperature



Typical Refresh Current IDD3 Versus Case Temperature



Typical Page Mode Current IDD4 Versus Case Temperature



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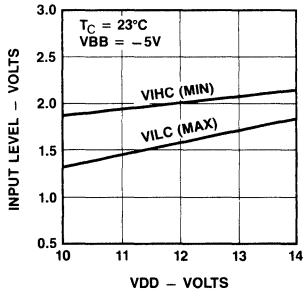
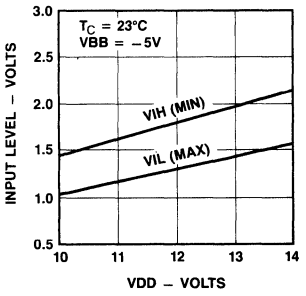
TYPICAL CHARACTERISTICS (Cont.)

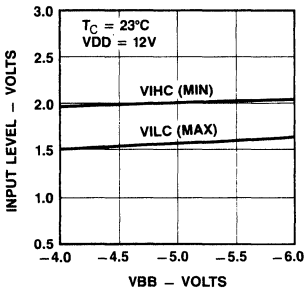
Input Voltage Levels Versus VDD



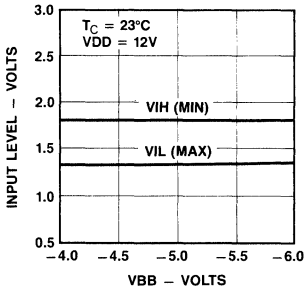
Input Voltage Levels Versus VDD



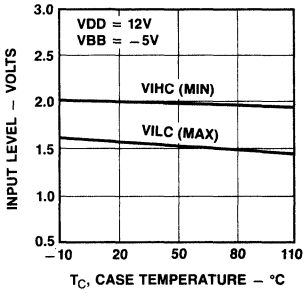
Input Voltage Levels Versus VBB



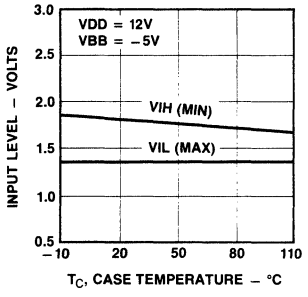
Input Voltages Levels Versus VBB



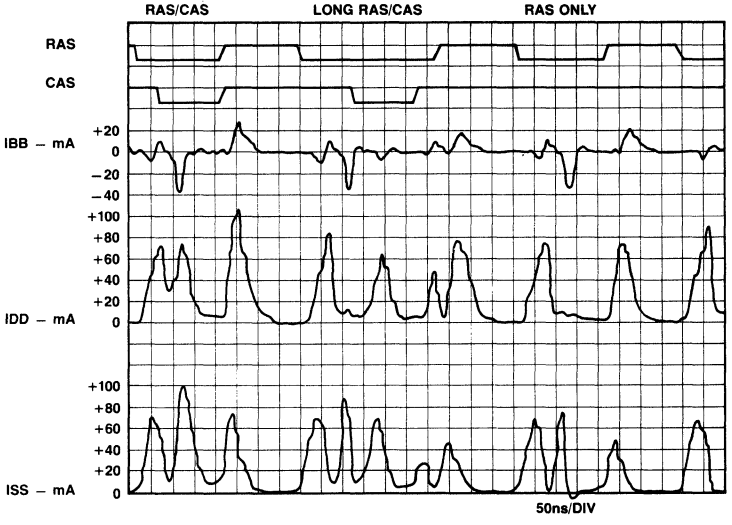
Input Voltage Levels Versus Case Temperature



Input Voltage Levels Versus Case Temperature



TYPICAL CURRENT WAVEFORMS



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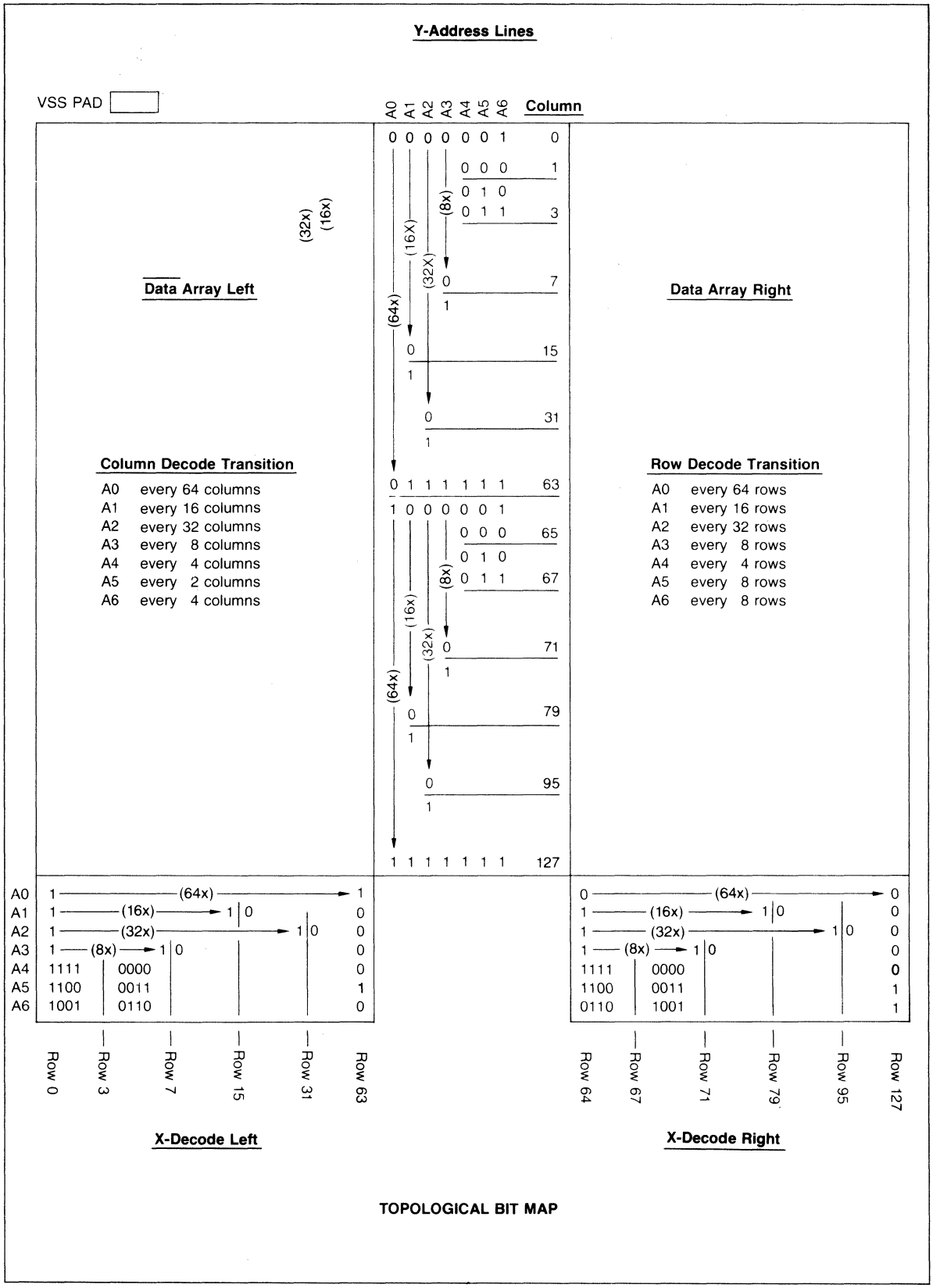
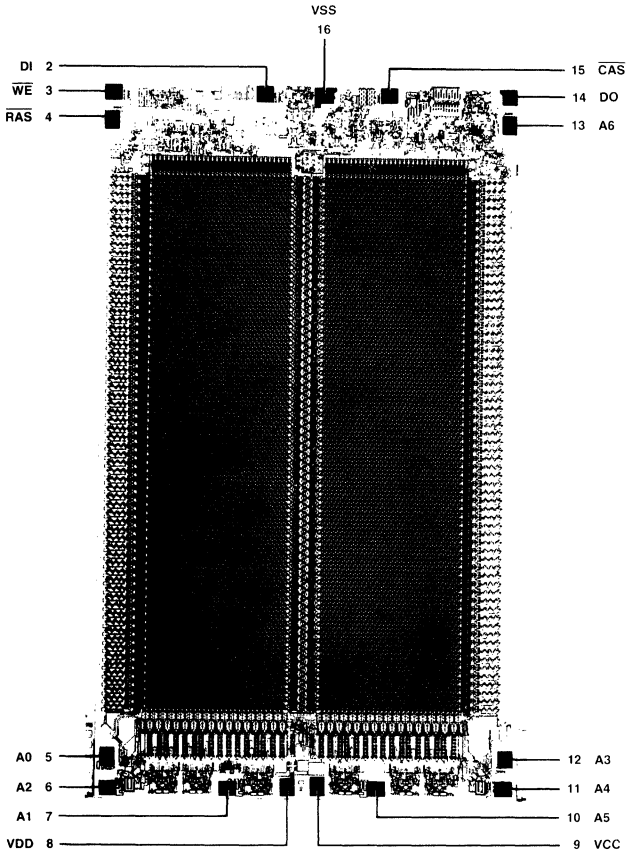


TOPOLOGICAL BIT MAP

METALLIZATION AND PAD LAYOUT

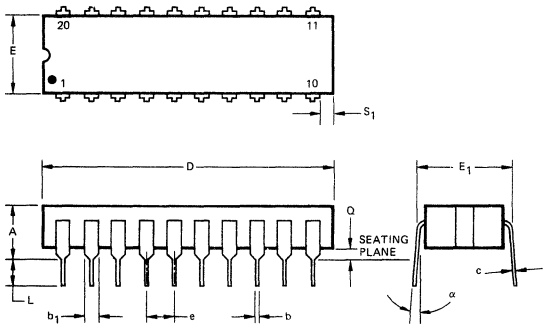


DIE SIZE 0.106" X 0.205"

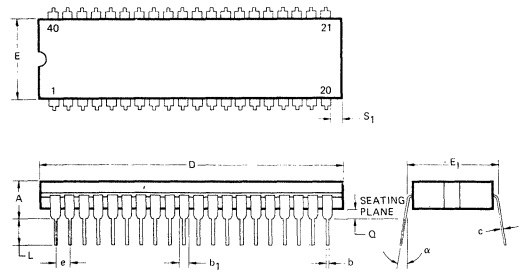
PACKAGE OUTLINES

HERMETIC DUAL IN-LINE PACKAGES

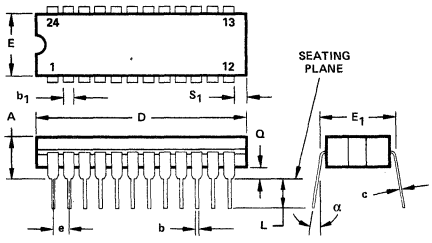
D-20-1



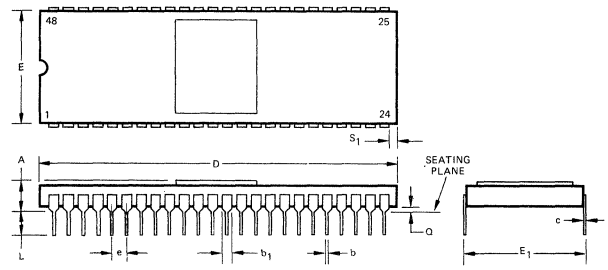
D-40-1



D-24-SLIM



D-48-2



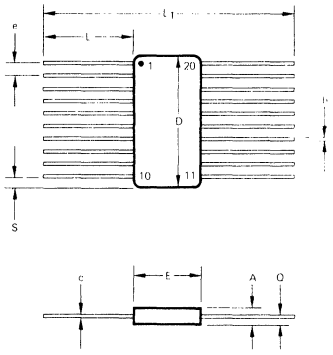
AMD Pkg	D-20-1		D-24		D-40-1		D-48-2	
Common Name	CERDIP		SLIM		CERDIP		SIDE-BRAZED	
38510 Appendix C	–		–		D-5		–	
Parameters	Min	Max	Min	Max	Min	Max	Min	Max
A	.140	.220	.120	.150	.150	.225	.100	.200
b	.016	.020	.016	.020	.016	.020	.015	.022
b_1	.050	.070	.045	.065	.045	.065	.030	.060
c	.009	.011	.009	.011	.009	.011	.008	.013
D	.935	.970	1.230	1.285	2.020	2.100	2.370	2.430
E	.245	.285	.245	.285	.510	.550	.570	.610
E_1	.290	.320	.290	.320	.600	.630	.590	.620
e	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.1120	.150	.120	.150	.125	.160
Q	.015	.060	.015	.060	.015	.060	.020	.060
S_1	.005		.010		.005		.005	
α	3°	13°	3°	13°	3°	13°		
Standard Lead Finish	b		–		b		b or c	

Notes: 1. Load finish b is tin plate. Finish c is gold plate
2. Used only for LM108/LM108A.
3. Dimensions E and D allow for off-center lid, meniscus and glass overrun.

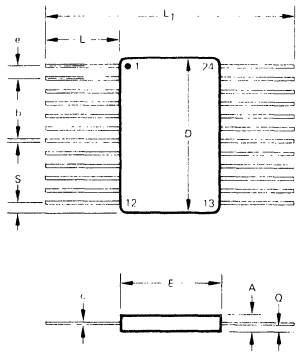
PACKAGE OUTLINES (Cont.)

FLAT PACKAGES

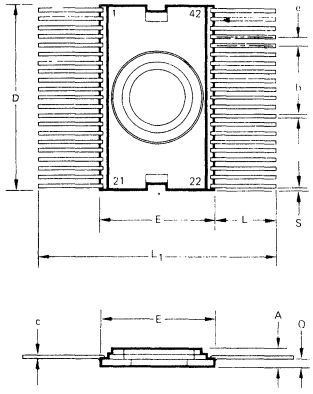
F-20-1



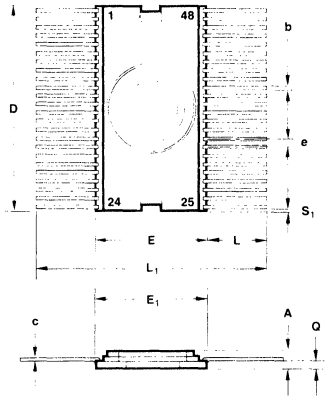
F-24-1



F-42-1



F-48-2



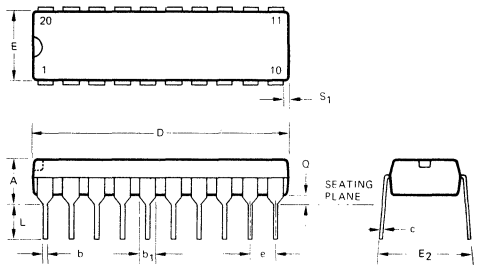
AMD Pkg	F-20-1		F-24-1		F-42-1		F-48-2	
Common Name	CERPACK		CERPACK		CERAMIC FLAT PAK		CERAMIC FLAT PAK	
38510 Appendix C	–		F-6		–		–	
Parameters	Min	Max	Min	Max	Min	Max	Min	Max
A	.045	.085	.050	.090	.070	.115	.070	.110
b	.015	.019	.015	.019	.017	.023	.018	.022
c	.004	.006	.004	.006	.006	.012	.006	.010
D	.490	.520	.580	.620	1.030	1.090	1.175	1.250
D_1						1.090		1.250
E	.245	.285	.360	.385	.620	.660	.615	.670
E_1		.290		.410		.660		.670
e	.045	.055	.045	.055	.045	.055	.045	.055
L	.300	.370	.265	.320	.320	.370	.320	.370
L_1	.920	.980	.920	.980	1.300	1.370	1.310	1.365
Q	.020	.040	.020	.040	.020	.060	.020	.055
S_1	.005		.005		.005		.015	
Standard Lead Finish	b		b		c		c	

Notes: 1. Lead finish is tin plate. Finish c is gold plate.
2. Dimensions E_1 and D_1 allow for off-center lid, meniscus, and glass overrun.

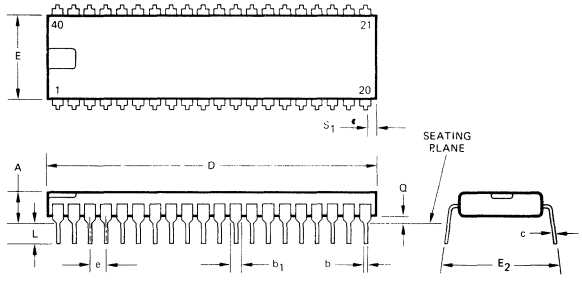
PACKAGE OUTLINES (Cont.)

MOLDED DUAL IN-LINE PACKAGES

P-20-1



P-40-1



AMD Pkg	P-20-1		P-40-1	
Parameters	Min	Max	Min	Max
A	.150	.200	.150	.200
b	.015	.020	.015	.020
b_1	.055	.065	.055	.065
c	.009	.011	.009	.011
D	1.010	1.050	2.050	2.080
E	.250	.290	.530	.550
E_2	.310	.385	.585	.700
e	.090	.110	.090	.110
L	.125	.150	.125	.160
Q	.015	.060	.015	.060
S_1	.025	.055	.040	.070

Notes: 1. Standard lead finish is tin plate or solder dip.
2. Dimension E_2 is an outside measurement.

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