Device Physics

6. MOSFET (1)

- The basic MOSFET operation
- Nonideal effects
- MOSFET scaling
- Threshold voltage modifications
- Additional electrical characteristics

The Basic MOSFET Operation

The transistor is a multi-junction semiconductor device that, in conjunction with other circuit elements, is capable of current gain, voltage gain, and signal power gain.
The basic transistor action is the control of current at one terminal by the voltage applied across the other two terminals of the device.
The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is one of two major types of transistors. The MOSFET is used extensively in digital circuit applications.

cf: the bipolar junction transistor (BJT, e.g., npn, pnp) is used extensively in analog electronic circuits.

MOSFET Structures

There are four basic MODFET device types.

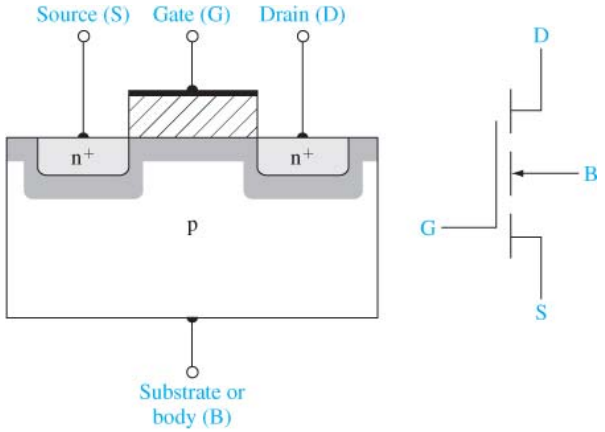


Figure 10.34 | Cross section and circuit symbol for an n-channel enhancement mode MOSFET.

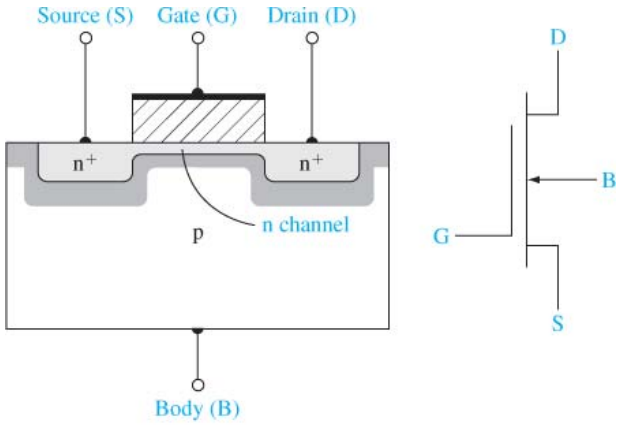
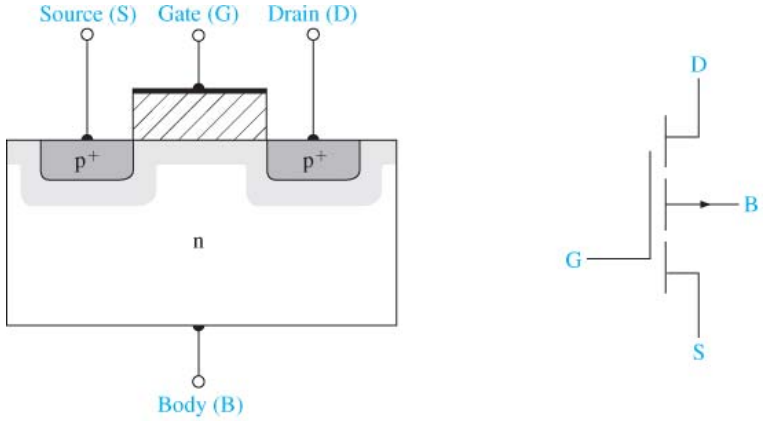
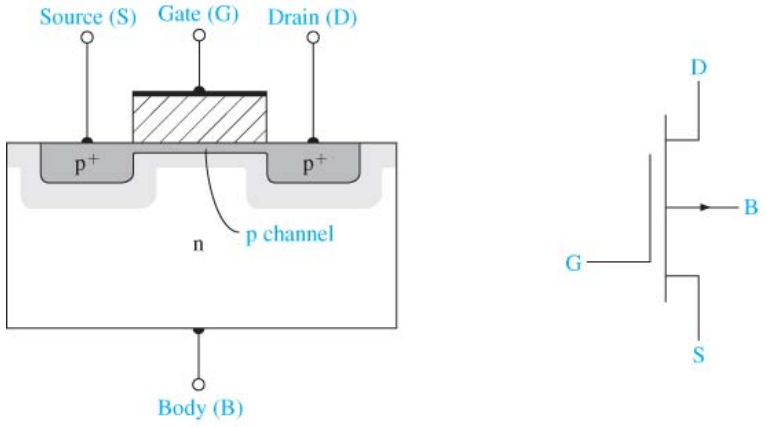


Figure 10.35 | Cross section and circuit symbol for an n-channel depletion mode MOSFET.



(a)



(b)

Figure 10.36 | Cross section and circuit symbol for (a) a p-channel enhancement mode MOSFET and (b) a p-channel depletion mode MOSFET.

I-V Relationship–Concepts

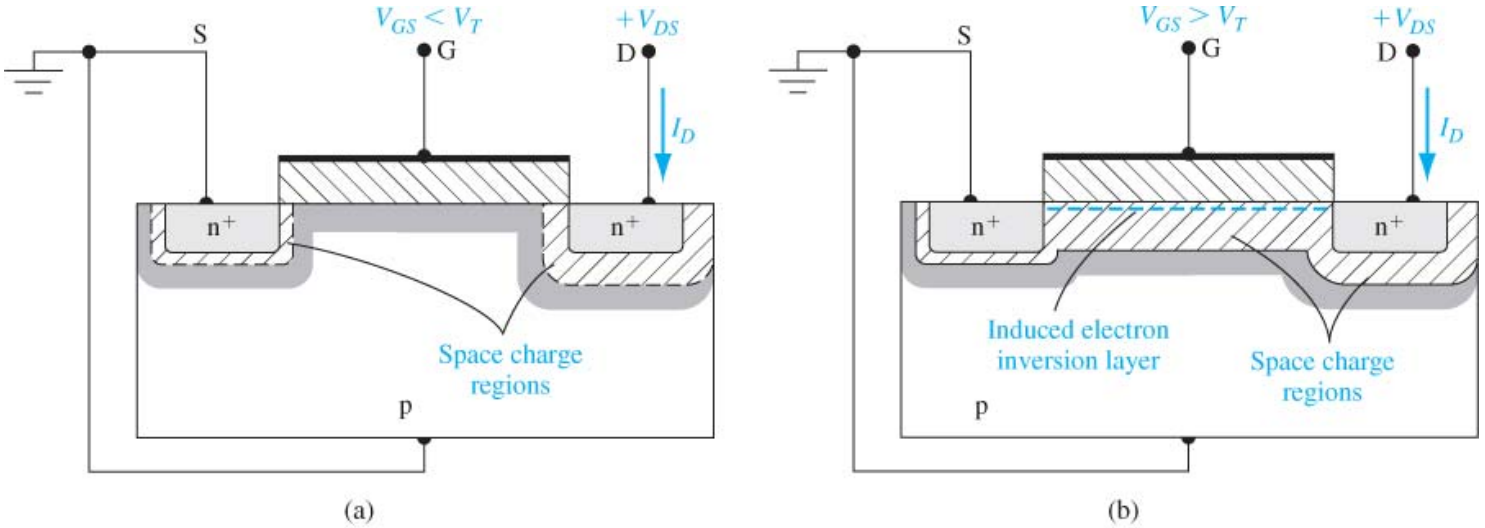


Figure 10.37 | The n-channel enhancement mode MOSFET (a) with an applied gate voltage $V_{GS} < V_T$ and (b) with an applied gate voltage $V_{GS} > V_T$.

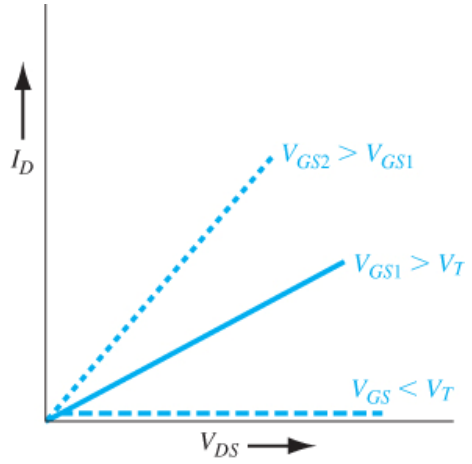


Figure 10.38 | I_D versus V_{DS} characteristics for small values of V_{DS} at three V_{GS} voltages.

For small V_{DS} values, the channel region has the characteristics of a resistor.

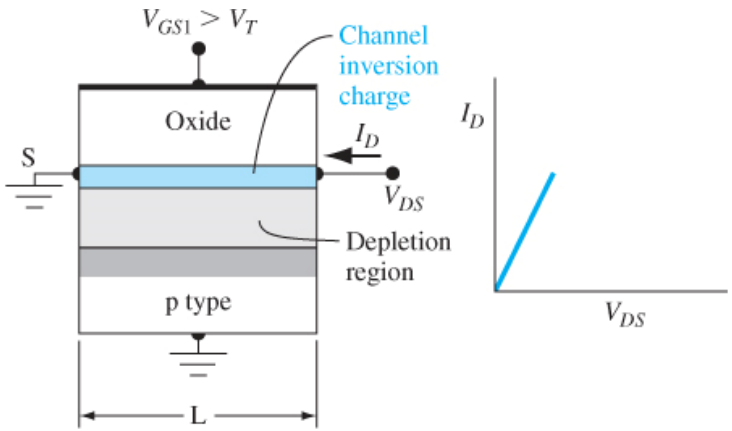
channel conductance

$$I_D = g_d V_{DS}$$

Inversion layer charge

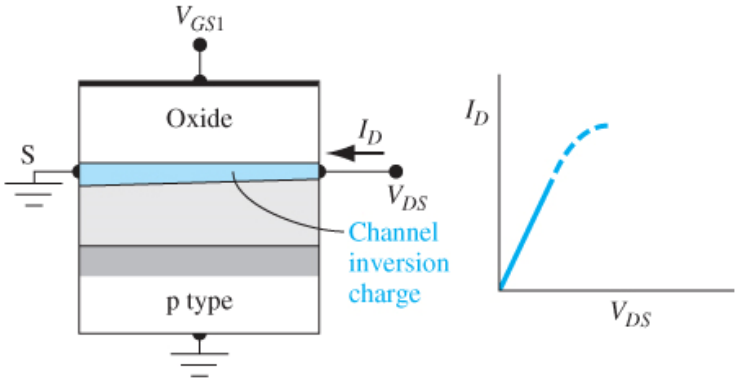
$$g_d = \frac{W}{L} \cdot \mu_n |Q_n'|$$

The inversion layer charge is a function of the gate voltage. Thus, the basic MOS transistor action is the modulation of the channel conductance by the gate voltage.



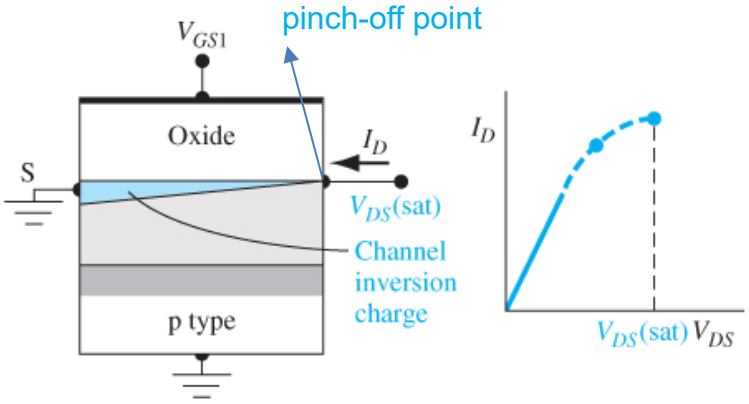
(a) Linear region

The channel acts as a resistor.



(b) Between linear and saturation region

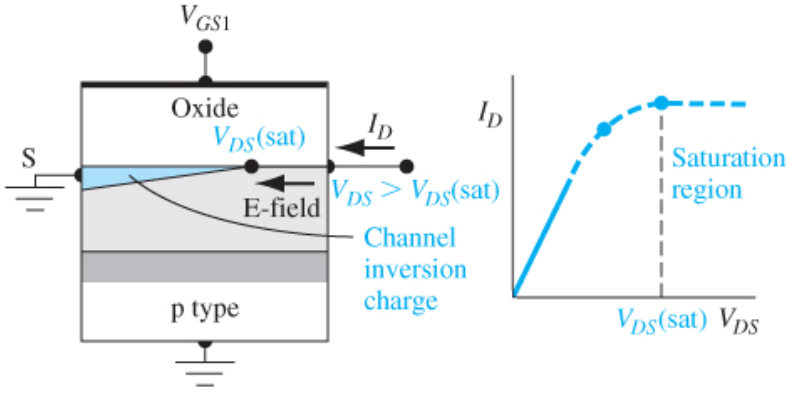
As the drain voltage increases, the voltage drop across the oxide near the drain terminal decreases. $[Q_n(L) \downarrow \Longrightarrow g_d \downarrow]$



(c) Onset of saturation

When the potential drop across the oxide at the drain terminal is equal to V_T, $Q_n(L)$ and g_d are zero.

$$V_{GS} - V_{DS}(sat) = V_T$$



(d) Beyond saturation

For $V_D > V_D(sat)$, $I_D = I_D(sat)$ because, the voltage at the pinch-off point remains as $V_D(sat)$.

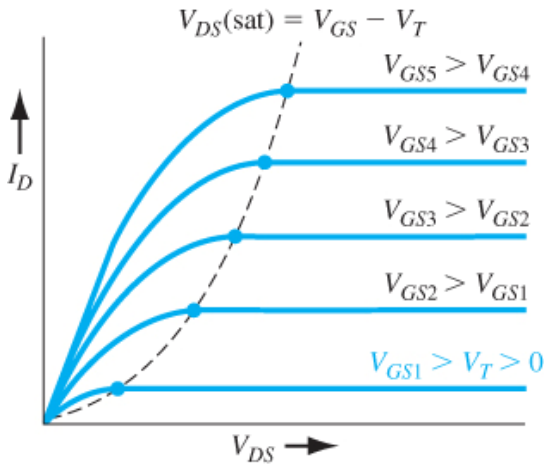


Figure 10.40 | Family of I_D versus V_{DS} curves for an n-channel enhancement mode MOSFET.

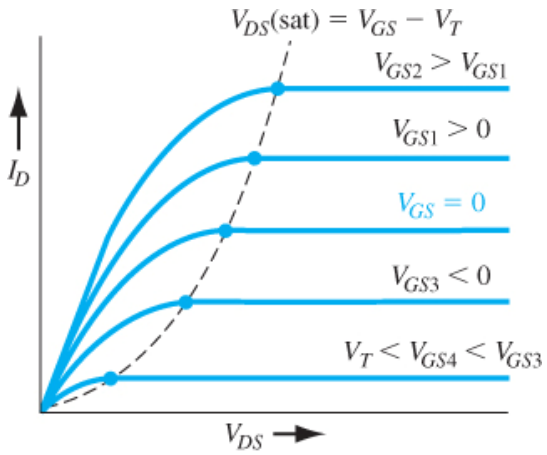


Figure 10.42 | Family of I_D versus V_{DS} curves for an n-channel depletion mode MOSFET.

In the linear region $[0 \leq V_{DS} \leq V_{DS}(sat)]$

$$I_D = \frac{W\mu_n C_{ox}}{2L}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \Rightarrow I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

$$I_D = K_n[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

In the saturation region $[V_{DS} \geq V_{DS}(sat)]$

$$I_D = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2 \Rightarrow I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$

$$I_D = K_n(V_{GS} - V_T)^2$$

process conduction parameter

$$k_n' = \mu_n C_{ox} \quad [A/V^2]$$

conduction parameter

$$K_n = (W\mu_n C_{ox})/2L = (k_n'/2) \cdot (W/L) \quad [A/V^2]$$

I-V Relationship–Mathematical Derivation

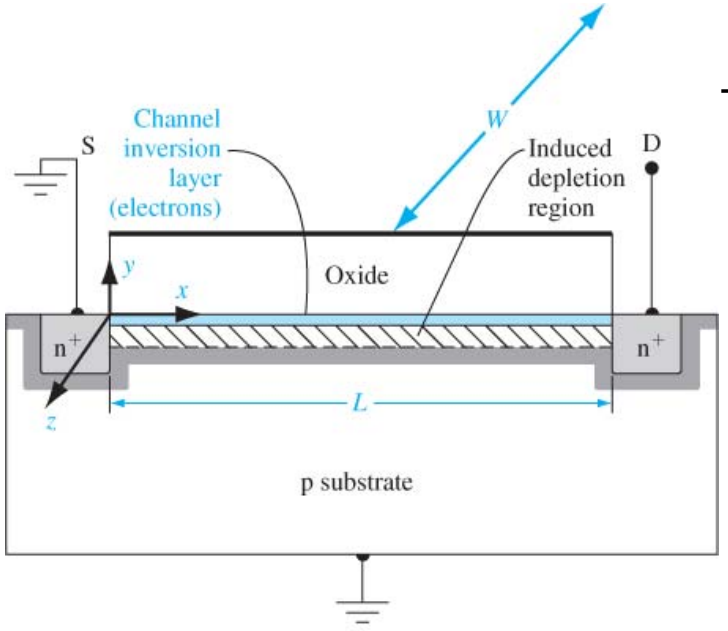


Figure 10.43 | Geometry of a MOSFET for I_D versus V_{DS} derivation.

The current in the channel is due to drift rather than diffusion.

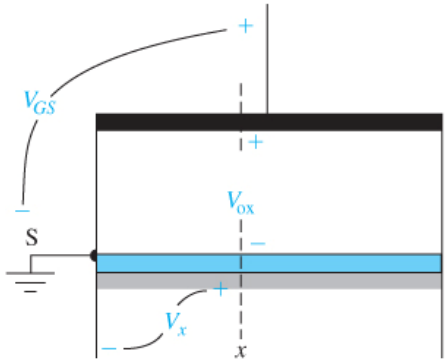
$$J_x = \sigma E_x \text{ (Ohm's law)} \qquad \sigma = e\mu_n n(y)$$

$$Q_n' = -\int en(y)dy$$

$$I_x = \int_y \int_z J_x \, dy \, dz$$

constant μ_n — By gradual channel approximation (E_x is constant in the channel)

$$I_x = \int_y \int_z e\mu_n n(y) E_x \, dy \, dz = \int_y en(y) \, dy \int_z \mu_n E_x \, dz = -Q_n' \mu_n E_x \int_z dz = -W \mu_n Q_n' E_x$$



$$Q_n' = -C_{ox}[(V_{GS} - V_x) - V_T]$$

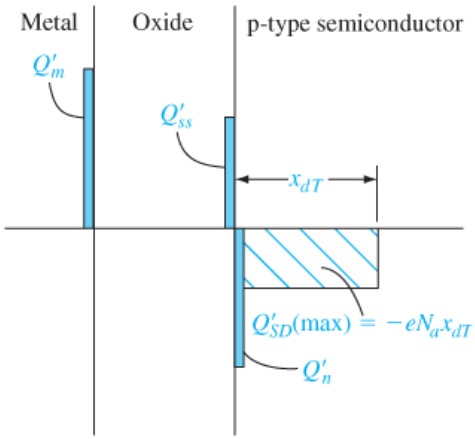


Figure 10.44 | Charge distribution in the n-channel enhancement mode MOSFET for $V_{GS} > V_T$.

Charge neutrality $Q'_m + Q'_{ss} + Q'_n + Q'_{SD}(max) = 0$

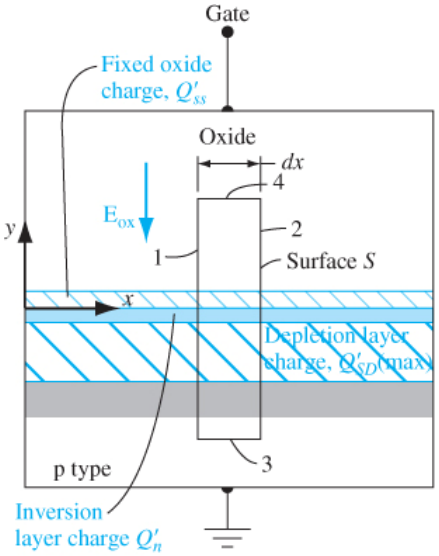


Figure 10.45 | Geometry for applying Gauss's law.

outward directed normal component of the electric field crossing the surface S

total charge enclosed by the surface

Gauss's law $\oint_S \varepsilon E_n \, dS = Q_T$

closed surface

$$\oint_S \varepsilon E_n \, dS = -\varepsilon_{ox} E_{ox} W dx = Q_T = [Q'_{ss} + Q'_n + Q'_{SD}(max)] W dx$$

$$-\varepsilon_{ox} E_{ox} = Q'_{ss} + Q'_n + Q'_{SD}(max)$$

$$E_{ox} = \frac{V_{ox}}{t_{ox}}$$

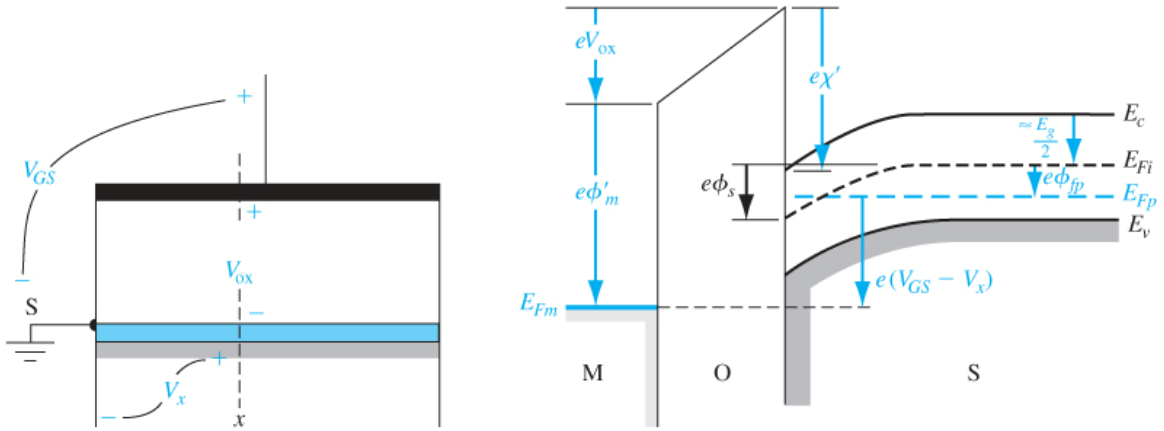


Figure 10.46 | (a) Potentials at a point x along the channel. (b) Energy-band diagram through the MOS structure at the point x.

$$E_{Fp} - E_{Fm} = e(V_{GS} - V_x)$$

$\phi_s = 2\phi_{fp}$ (inversion condition)

$$\phi_{ms} \equiv \phi'_m - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)$$

$$V_{GS} - V_x = (\phi'_m + V_{ox}) - \left(\chi' + \frac{E_g}{2e} - \phi_s + \phi_{fp}\right) = V_{ox} + 2\phi_{fp} + \phi_{ms}$$

$$-\varepsilon_{ox}E_{ox} = -\varepsilon_{ox} \cdot \frac{V_{ox}}{t_{ox}} = \frac{-\varepsilon_{ox}}{t_{ox}}\left[(V_{GS} - V_x) - (\phi_{ms} + 2\phi_{fp})\right] = Q'_{ss} + Q'_n + Q'_{SD}(max)$$

$$Q'_n = \frac{-\varepsilon_{ox}}{t_{ox}}\left[(V_{GS} - V_x) - (\phi_{ms} + 2\phi_{fp})\right] - Q'_{ss} - Q'_{SD}(max) = -C_{ox}[(V_{GS} - V_x) - V_T]$$

$$V_T = \frac{|Q'_{SD}(max)|}{C_{ox}} - \frac{Q'_{ss}}{C_{ox}} + \phi_{ms} + 2\phi_{fp} \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$Q_n' = -C_{ox}[(V_{GS} - V_x) - V_T] \qquad E_x = -\frac{dV_x}{dx}$$

$$I_x = -W\mu_n Q_n' E_x = -W\mu_n C_{ox}\frac{dV}{dx}[(V_{GS} - V_x) - V_T]$$

$$\int_0^L I_x\,dx = -W\mu_n C_{ox}\int_{V_x(0)}^{V_x(L)}[(V_{GS} - V_x) - V_T]\,dV_x = -W\mu_n C_{ox}\int_0^{V_{DS}}[(V_{GS} - V_x) - V_T]\,dV_x$$

For the n-channel device, the drain current enters the drain terminal and is constant along the entire channel length.

$$I_D = -I_x = \frac{W\mu_n C_{ox}}{2L}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

$$0 \le V_{DS} \le V_{DS}(sat)$$
$$V_{GS} \ge V_T$$

$$\frac{dI_D}{dV_{DS}} = 0 \rightarrow V_{DS} = V_{DS}(sat) = V_{GS} - V_T$$

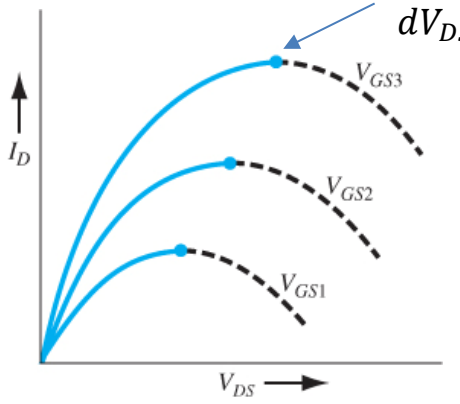


Figure 10.47 | Plots of I_D versus V_{DS} from Equation (10.62).

For $V_{DS} > V_{DS}(sat)$

$$I_D(sat) = \frac{W\mu_n C_{ox}}{2L}[2(V_{GS} - V_T)V_{DS}(sat) - V_{DS}^2(sat)]$$

$$= \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2$$

We can use the I-V relations to experimentally determine the mobility and threshold voltage parameters.

For very small values of V_{DS}, $$I_D = \frac{W\mu_n C_{ox}}{2L}[2(V_{GS} - V_T)V_{DS}]$$

For $V_{DS} > V_{DS}(sat)$, $$\sqrt{I_D(sat)} = \sqrt{\frac{W\mu_n C_{ox}}{2L}}(V_{GS} - V_T)$$

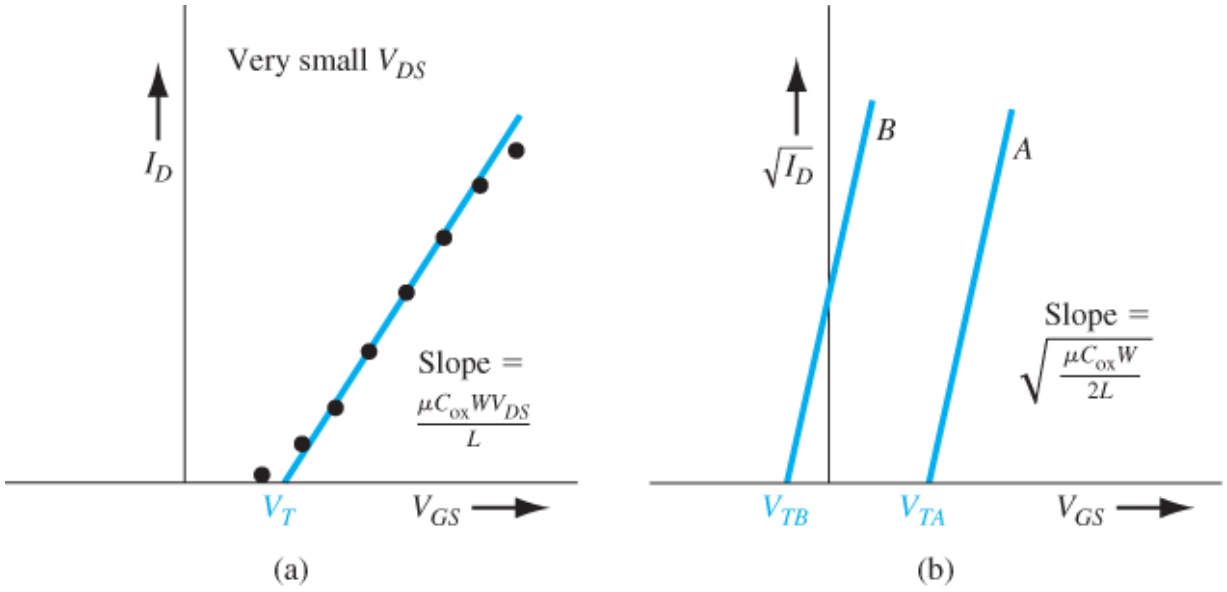


Figure 10.48 | (a) I_D versus V_{GS} (for small V_{DS}) for enhancement mode MOSFET. (b) Ideal $\sqrt{I_D}$ versus V_{GS} in saturation region for enhancement mode (curve A) and depletion mode (curve B) n-channel MOSFETs.

In general, the nonsaturation I-V characteristics produces the more reliable data.

One assumption we made in the derivation of the I-V relationship was the charge neutrality condition ($Q'_m + Q'_{ss} + Q'_n + Q'_{SD}(max) = 0$) was valid over the entire length of the channel.

We implicitly assumed that $Q'_{SD}(max)$ was constant along the length of the channel.
The space charge width, however, varies between source and drain due to the drain-to-source voltage; It is widest at the drain when $V_{DS} > 0$.

A change in the space charge density along the channel length must be balanced by a corresponding change in the inversion layer charge.
An increase in the space charge width means that the inversion layer charge is reduced, implying that the drain current and drain-to-source saturation voltage are less than the ideal values.

The actual saturation drain current may be as much as 20% less than the predicted values due to this bulk charge effect.

Transconductance

The MOSFET transconductance (or transistor gain)

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

In the nonsaturation region,

$$g_{mL} = \frac{\partial I_D}{\partial V_{GS}} = \frac{W \mu_n C_{ox}}{L} \cdot V_{DS}$$

increase linearly with V_{DS}

but is independent of V_{GS}

In the saturation region,

$$g_{ms} = \frac{\partial I_D(sat)}{\partial V_{GS}} = \frac{W \mu_n C_{ox}}{L} (V_{GS} - V_T)$$

a linear function of V_{GS}

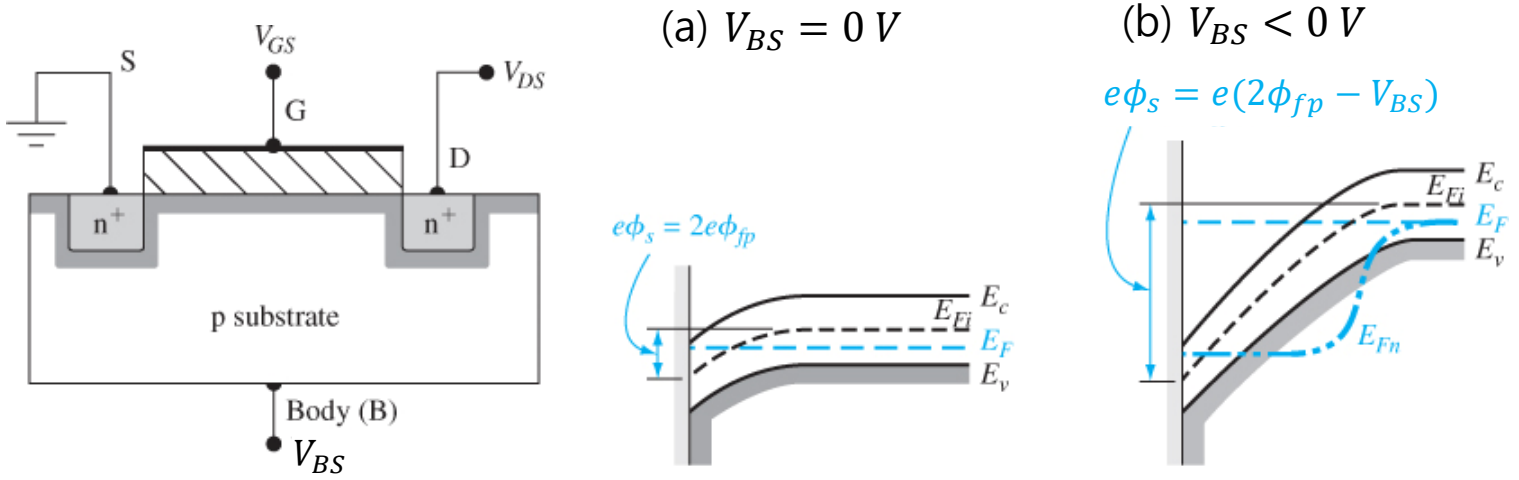
but is independent of V_{DS}

The transconductance is a function of the geometry of the device as well as of carrier mobility and threshold voltage. In the design of MOSFET circuits, the size of the transistor, especially the channel width W, is an important engineering design parameter.

Substrate Bias Effects

When a reverse-biased substrate (body)-source voltage is applied, the space charge region width under the oxide increases from the original x_{dT} value. With an applied $V_{BS} < 0$, there is more charge associated with this region. Considering the charge neutrality condition through the MOS structure, the positive charge on the top metal gate must increase to compensate for the increased negative space charge in order to reach the threshold inversion point. So when $V_{BS} < 0$, the threshold voltage of the n-channel MOSFET increases.

$$\Delta V_T = -\frac{\Delta Q'_{SD}}{C_{ox}} = \frac{\sqrt{2e\varepsilon_s N_a}}{C_{ox}}\left[\sqrt{2\phi_{fp} - V_{BS}} - \sqrt{2\phi_{fp}}\right]$$



Equivalent Circuits of MOSFET

The equivalent circuit contains capacitances and resistances that introduce frequency effects that limit the frequency response of the MOSFET.

A transistor cut-off frequency, which is a figure of merit, is defined as,

$$f_T = \frac{g_m}{2\pi C_G} = \frac{\frac{W\mu_n C_{ox}}{L}(V_{GS} - V_T)}{2\pi(C_{ox}WL)} = \frac{\mu_n(V_{GS} - V_T)}{2\pi L^2}$$

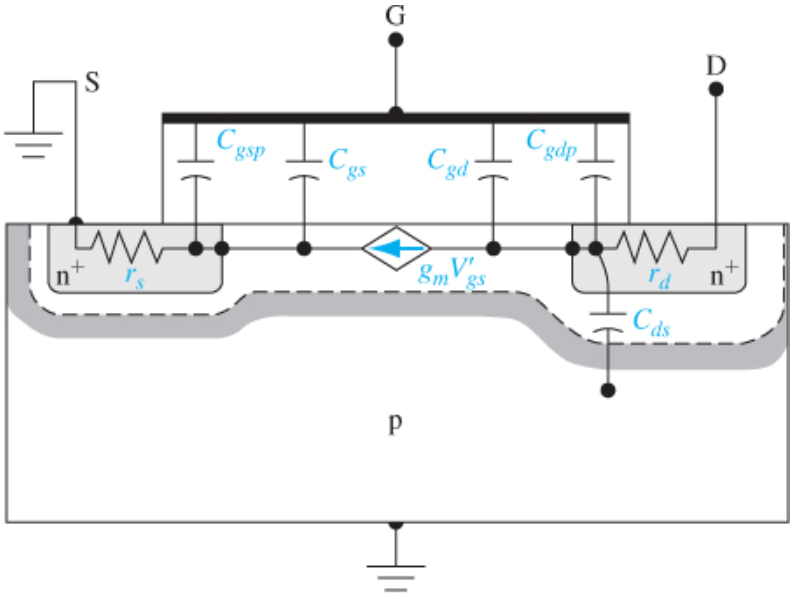


Figure 10.52 | Inherent resistances and capacitances in the n-channel MOSFET structure.