

# Ixia Platform Reference Guide

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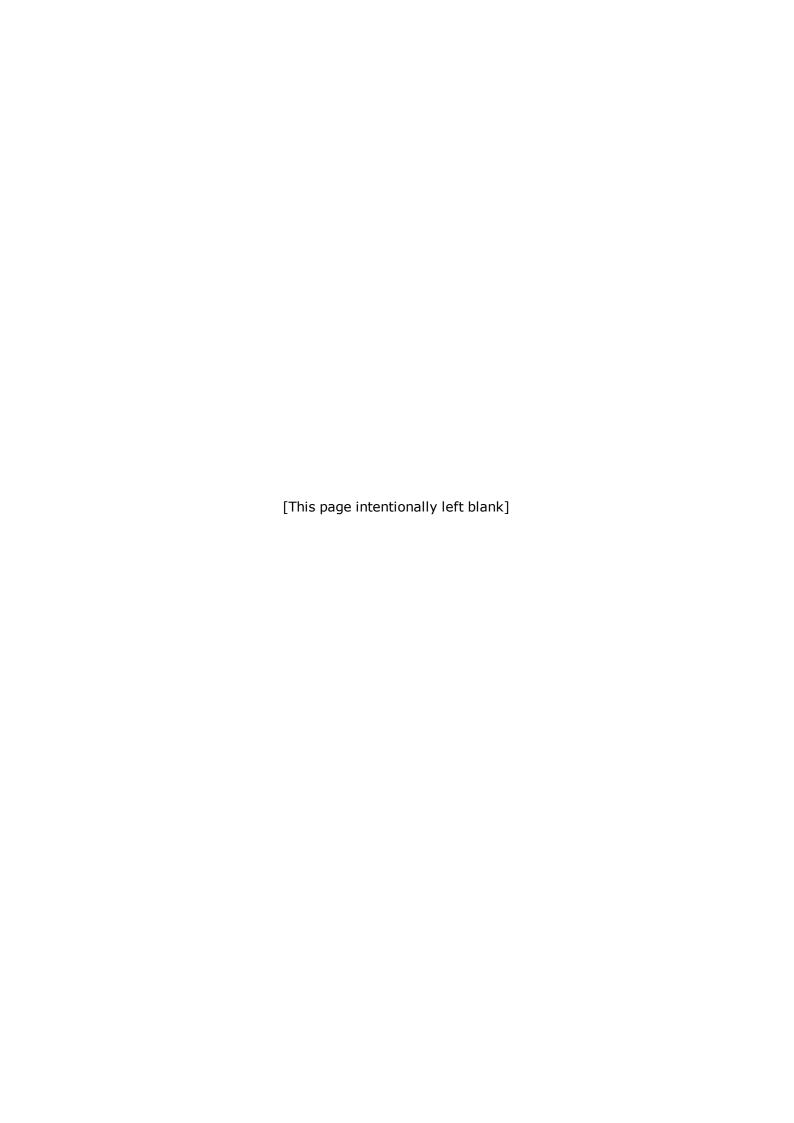
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## **About This Guide**

The information in this section is provided to help you navigate this guide and make better use of its content. A list of related documents is also included.

The Third-Party Software License document is included with the download package.

### **Purpose**

This guide provides information about Ixia hardware theory, features, functions, and options, as well as additional test setup details.

### **Manual Content**

This guide contains the following sections:

Section	Description
About This Guide (this section)	Provides information on this manual, including its purpose, content, and related documentation. Also explains how to contact technical support.
Chapter 1 Platform and Reference Over- view	Provides a basic overview of Ixia hardware and theory of operation. Hardware includes descriptions of all supported chassis and load modules.
Chapter 2 Theory of Operation: General	Provides a general overview of the various technologies used in both IxExplorer and in the IxOS.
Chapter 3 Theory of Operation: Protocols	Provides a general overview of the various technologies used in IxNetwork and IxRouter.
Chapter 4 Optixia XM12 Chassis	Provides a detailed description of the features and systems of the Optixia XM12 chassis.
Chapter 5 Optixia XM2 Chassis	Provides a detailed description of the features and systems of the Optixia XM2 chassis.
Chapter 6 XG12 Chassis	Provides a detailed description of the features and systems of the XG12 chassis.
Chapter 7 XGS12 Chassis Platform	Provides a detailed description of the features and systems of the XGS12 chassis platform.
Chapter 8 XGS2 Chassis Platform	Provides a detailed description of the features and systems of the XGS2 chassis platform.
Chapter 9 Optixia X16 Chassis	Provides a detailed description of the features and systems of the Optixia X16 chassis.
Chapter 10 IXIA 400T Chassis	Provides a detailed description of the features and systems of the 400T chassis.
Chapter 11 IXIA 400T v2 Chassis	Provides a detailed description of the features and systems of the 400T v2 chassis.

Section	Description
Chapter 12 XOTN Chassis Unit	Provides a detailed description of the features and systems of the XOTN chassis.
Chapter 13 Ixia GPS Auxiliary Function Device (AFD1)	Provides a detailed description of the features and systems of the Ixia Auxiliary Function Device (AFD1).
Chapter 14 Ixia IRIG-B Auxiliary Function Device (AFD2)	Provides a detailed description of the features and systems of the Ixia IRI-B Auxiliary Function Device (AFD2).
Chapter 15 Met- ronome	Provides a detailed description of the features and systems of the Ixia Metronome Timing System.
Chapter 16 IXIA Impairment Load Modules	Provides a detailed description of the features and capabilities of Xdensity (XDM10G32S) load module.
Chapter 17 IXIA Xcellon-Lava Load Modules	Provides a detailed description of the features and capabilities of Xcellon-Lava load module.
Chapter 18 IXIA Power over Ethernet Load Modules	Provides a detailed description of the features and capabilities of Power over Ethernet load modules.
Chapter 19 IXIA 10/100/1000 Load Modules	Provides a detailed description of the features and capabilities of 10/100/1000 Ethernet load modules.
Chapter 20 IXIA Net- work Processor Load Modules	Provides a detailed description of the features and capabilities of Xcellon-Ultra NP and Xcellon-Ultra XP load modules. It also provides card specifications and description of features when Xcellon-Ultra card is used in IxN2X mode with added IxN2X capability. The card is reported as Xcellon-Ultra NG by IxExplorer when it is running in IxN2X mode. Xcellon-Ultra NP, Xcellon-Ultra XP, and Xcellon-Ultra NG are all physically similar.
Chapter 21 IXIA 40/100 Gigabit Eth- ernet Load Modules	Provides a detailed description of the features and capabilities of 40 and 100 Gigabit Ethernet load modules.
Chapter 22 IXIA 10 Gigabit Ethernet Load Modules	Provides a detailed description of the features and capabilities of 10 Gigabit Ethernet load modules.
Chapter 23 IXIA OC12 ATM/POS Load Modules	Provides a detailed description of the features and capabilities of ATM load modules.
Chapter 24 IXIA 10/100 Load Mod-	Provides a detailed description of the features and capabilities of 10/100 Ethernet load modules.

Section	Description
ules	
Chapter 25 IXIA  10GE LAN/WAN and OC 192 POS Load Modules	Provides a detailed description of the features and capabilities of OC192c Optical Carrier load modules.
Chapter 26 IXIA OC12c/OC3c Load Modules	Provides a detailed description of the features and capabilities of OC12c/OC3c Optical Carrier load modules.
Chapter 27 IXIA OC48c Load Modules	Provides a detailed description of the features and capabilities of OC48c Optical Carrier load modules.
Chapter 28 IXIA FCMGXM Load Mod- ules	Provides a detailed description of the features and capabilities of Fibre Channel load modules.
Chapter 29 IXIA Xcellon-Flex Load Modules	Provides a detailed description of the features and capabilities of Xcellon-Flex load modules.
Chapter 30 IXIA Xcellon-Multis Load Modules	Provides a detailed description of the features and capabilities of Xcellon-Multis load modules.
Chapter 31 IXIA Xcellon-Multis Reduced Load Modules	Provides a detailed description of the features and capabilities of Xcellon-Multis Reduced load modules.
Chapter 32 Ixia Novus Load Modules	Provides a detailed description of the features and capabilities of Novus load modules.
Chapter 33 Ixia Novus-R Load Modules	Provides a detailed description of the features and capabilities of Novus-R load modules.
Chapter 34 Ixia Novus-M Load Mod- ules	Provides a detailed description of the features and capabilities of Novus-M load modules.
Chapter 35 Ixia Novus 10G/1G/100M Ethernet Load Modules	Provides a detailed description of the features and capabilities of Novus 10G/1G/100M Ethernet load modules.
Chapter 36 Ixia Novus-NP Load Modules	Provides a detailed description of the features and capabilities of Novus-NP load modules.
Chapter 37 Ixia Novus-32P Load Mod-	Provides a detailed description of the features and capabilities of Novus-32P load modules.

Section	Description
ules	
Chapter 38 Ixia Per- fectStorm Load Mod- ules	Provides a detailed description of the features and capabilities of PerfectStorm load modules.
Chapter 39 Ixia CloudStorm Load Modules	Provides a detailed description of the features and capabilities of CloudStorm load modules.
Chapter 40 Ixia XDensity XDM10G32S/8S Load Modules	Provides a detailed description of the features and capabilities of Xdensity (XDM10G32S) load module.
Chapter 41 Ixia XMVAEGE Ethernet Load Modules	Provides a detailed description of the features and capabilities of XMVAE Ethernet load module.
Chapter 42 Ixia Stream Extraction Load Modules	Provides a detailed description of the features and capabilities of Ethernet Stream Extraction load modules.
Chapter 43 Ixia Per- fectStormOne Appli- ances	Provides a detailed description of the features and capabilities of PerfectStormONE appliances.
Chapter 44 Ixia Novus One Appliances	Provides a detailed description of the features and capabilities of Novus ONE appliances.
Chapter 45 XAirXM Load Module	Provides a detailed description of the features and capabilities of XAir load modules.
Chapter 46 XAir2™ LTE Module	Provides a detailed description of the features and capabilities of XAir2 load module.
Appendix A XAUI Connector Spe- cifications	Provides a detailed description of various XAUI connectors provided by Ixia for various modules.
Appendix B Available Statistics	Lists all the statistics, by module and by technology, collected by Ixia hardware.
Appendix C GPS Antenna Installation Requirements	Describes the recommended installation method for an IXIA GPS Antenna.
Appendix D Hot- Swap Procedure	Describes the procedure for removing and reinstalling a Load Module without requiring the removal of power from the rest of the chassis.
Appendix E IP Port Assignments on Ixia	Lists the services assigned to IP ports on Ixia chassis and port CPUs.

Section	Description
Chassis and Linux port CPUs	
Appendix F Laptop Controller	Lists the specifications of the Laptop Controller.
Appendix G Soft- ware Licenses	Provides the copyright and license information of the various open source software that are delivered as part of IxOS.

## **Related Documentation**

The following guides help you learn more about the hardware for IxOS. The guides are available on the CD shipped with the application, as well as on the Ixia Website at <a href="www.ixi-acom.com">www.ixi-acom.com</a>.

- *IxExplorer User Guide*: Provides details on the usage of the IxExplorer GUI for operation with an Ixia chassis and Ixia load modules.
- *IxServer User Guide*: Provides details on the usage of the IxServer GUI for operation on an Ixia chassis.
- *IxOS Tcl Development Guide*: Provides details on the structure and conventions of the IxExplorer Tcl API and provides detailed information on all API commands.
- Ixia online Glossary of technical terms is located at www.ixiacom.com/glossary.

# **Technical Support**

You can obtain technical support for any Ixia product by contacting Ixia Technical Support by any of the methods mentioned on the inside cover of this manual. Technical support from Ixia's corporate headquarters is available Monday through Friday from 06:00 to 18:00, UTC (excluding American holidays). Technical support from Ixia's EMEA and India locations is available from Monday through Friday, 08:00 to 17:00 local time (excluding local holidays).

# Notes, Cautions, Warnings

#### **Power Cords**

CAUTION	Power cords that are included in shipments of Ixia equipment meet the approved/recognized standards of the national safety organization(s) of the destination country.  Use the power cord provided or a power cord approved by the appropriate agency for use in the country where the unit is being used. The power source should be properly grounded.
CAUTION	Les câbles d'alimentation livrés avec les équipements Ixia sont conformes aux/normes reconnues des organismes nationaux de sécurité du pays de destination.  Utilisez le câble d'alimentation fourni ou un câble approuvé par l'organisme
	adéquat du pays dans lequel l'unité est utilisée. La source d'alimentation doit être correctement mise à la terre.

## **Battery Replacement**

#### CAUTION

Danger of explosion if battery is incorrectly replaced. You should not attempt to replace the battery. Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries according to the battery manufacturer's instructions.

## Remplacement de la batterie

#### ATTENTION

Le remplacement incorrect de la batterie peut provoquer une explosion. Vous ne devez en aucun casessayer de remplacer la batterie.

Renvoyez le produit au service clients Ixia pour un échange avec le mêmetype de batterie ou un type équivalent. Ixia met les batteries usagées au rebut conformémentaux instructions du fabricant.

## **Ventilation Requirements**

The following caution applies to equipment installed into equipment racks.

#### CAUTION

Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced. Do not block the back or sides of the chassis, and leave approximately two inches of space around the unit for proper ventilation.

#### ATTENTION

Flux d'air réduit: installez l'équipement dans un rack de manière à ne pas réduire le flux d'air requis pour le fonctionnement en toute sécurité de l'équipement.

N'obstruez ni les côtés ni l'arrière du châssis et laissez environ cinq centimètres (deuxpouces) autour de l'unité pour une ventilation correcte. N'obstruez aucunorifice de ventilation du châssis.

Nettoyez régulièrement les grilles d'entrée d'air pour permettre une bonne entrée d'air.

## **Use End Caps on Open Ports**

The metal edges of the SFP port are sharp. To avoid injury, always keep unused SFP ports covered with end caps. When installing a load module into a chassis or removing from a chassis, ensure that end caps are in place on unused ports.

# Utilisez des capuchons de protection sur les ports ouverts

Les arêtes métalliques des ports SFP et SFP+ sont VIVES. Pour éviter toute blessure, recouvrez TOUJOURS les ports SFP non utilisés de capuchons. Lorsque vous installez un module de charge dans un châssis ou que vous le retirez, assurez-vous que les ports non utilisés sont bien protégés par des capuchons.

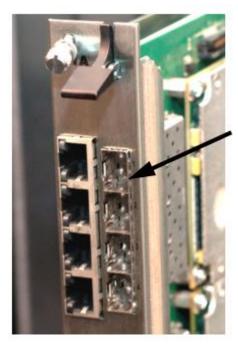
#### **▲WARNING**

To prevent accidental injury to personnel, do not leave unused SFP (or SFP+) ports uncovered. When transceivers are not installed, end caps must be used.

#### AVERTISSEMENT

Pour éviter toute blessure accidentelle de vos employés, ne laissez pas les ports SFP (ou SFP+) découverts. Lorsqu'il n'y a pas d'émetteurs-récepteurs installés, les capuchons doivent être installés.

The following image shows the precautionary measure to be taken while handling unused SFP/SFP+ Ports in the laboratory.



Unused SFP/SFP+ ports need end caps

Affected load modules include the following:

- NGY with SFP+ interface, 2/4/8-port, all models
- Dual PHY SFF cards with RJ45 and SFP Gigabit (TXS and STXS)
- · Xcellon-Ultra NP, XP, and NG
- LSM1000XMV 4/8/12/16-port
- LSM1000XMS
- ASM1000XMV
- AFM1000SP
- ELM1000ST

## **Use Ejector Tabs Properly**

Ejector tabs on load modules are to be used only to eject a load module from the chassis backplane connector. They are not designed to support the weight of the load module. Ejector tabs can bend or break if used improperly as handles to push, pull, or carry a load module.

#### CAUTION

Do not use ejector tabs as handles to support a load module while installing and seating into the chassis. The ejector tabs are to be used only to eject the module from the chassis backplane connector.

## **China RoHS Declaration Table Chassis**

零件项目(名称) (Component Name)	有毒有害物质或元素(Hazardous Substances or Elements)					
	铅 Lead (Pb)	汞 Mercury (Hg)	镉 Cadmium (Cd)	六价铬 Chromium VI Compounds (Cr6+)	多溴联苯 Poly- brominated Biphenyls (PBB)	多溴二苯醚 Poly- brominated Diphenyl Ethers (PBDE)
印制电路配件 (Printed Circuit Assemblies)	X	0	0	0	0	0
內部线路 (Internal wiring)	х	0	0	0	0	0
底架 (Chassis)	0	0	0	0	0	0
金属外壳 (Metal Enclosure)	0	0	0	0	0	0
螺帽,螺钉(栓),螺旋(钉), 垫圈,紧固件 (Nuts, bolts, screws, washers, Fasteners)	0	0	0	0	0	0
电源供应器 (Power Supply Unit)	0	0	0	0	0	0
风扇 (Fan)	0	0	0	0	0	0
正面(前)面板 (Front panel)	0	0	0	0	0	0

O: 表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006标准规定的限量要求以下.

O: Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006.

x: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006标准规定的限量要求.

X: Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement in SJ/T11363-2006.

# **Chapter 1 - Platform and Reference Overview**

The Ixia system is the most comprehensive tool available for testing multilayer 10/100 Mbps Ethernet, Ethernet Gigabit, 10 Gigabit Ethernet, ATM, and Packet over SONET switches, routers, and networks.

The Ixia product family includes chassis, load modules, the Ixia IxExplorer software program, and optional Tcl scripts and related software. A chassis can be configured with any mix of load modules, and multiple chassis can be daisy-chained and synchronized to support very large and complex test environments. The Ixia IxExplorer software provides complete configuration, control, and monitoring of all Ixia resources in the test network, and the Tcl scripts allow to rapidly conduct the most popular industry benchmark tests.

The Optixia XM12 provides high port density and hot swappable capability. The Optixia XM2 provides hot-swappable capability in a more portable format. The Optixia X16 chassis also provides hot-swappable capability for up to 16 load modules.

The Optixia XM2 is the next generation portable chassis that is a combination of the Optixia architecture with the XM form factor. The 2-slot platform allows for higher port density load modules in a portable chassis.

The XGS12 chassis models– XGS12-SD and XGS12-HS are the next generation high performance platform capable of supporting XM form factor load modules. XGS12-SD and XGS12-HS are 12-slot chassis with high-speed backplane designed for aggregation across load modules. This flexible platform supports layer 2-7 testing on a massive scale and provides the most comprehensive solution for performance, functional, security, and conformance testing of network equipment and network applications.

The XGS2 chassis models - XGS2-SD and XGS2-HS provide highly flexible and portable chassis that powers load modules and test applications to create an Ixia test system. The chassis platform supports Ixia applications for performance, functional, conformance, and security testing.

You can configure and control the unit directly through connections to a keyboard, mouse, monitor, and printer. Also, the unit can be connected to an Ethernet network, and an administrator can remotely monitor and control it using the IxExplorer software program. Multiple users can access the unit simultaneously, splitting the ports within a chassis and controlling the activity and configuration of all ports and functions.

Front panel displays give immediate indication of link state, transmission or reception of packets, and error conditions.

Ixia produces a number of load modules which provide data transmission and reception capabilities for a variety of Ethernet, ATM, and Packet Over Sonet (POS) speed and technologies. These load modules reside in an Ixia chassis, which provide different numbers of load module slots and power. This chapter introduces the Ixia hardware components. The Ixia chassis and load modules are compared and contrasted.

### **Ixia Chassis**

The following Ixia chassis are currently available for sale:

- XGS12 Chassis Platform: The XGS12 chassis platform is the next generation high performance platform capable of supporting all XM form factor load modules, including full chassis configurations of the Xcellon load modules. It is a 12-slot chassis platform with highspeed backplane (160 Gbps between each adjacent two cards) designed for aggregation across load modules.
- Optixia XM2 Chassis: Capable of holding two Ixia load modules and equipped with
  extra power and fans required for some high-powered load modules. Supports higher
  port density. Modules can be inserted and removed from the chassis without shutting
  the chassis down, and a load module can be removed without impacting the processes of other load modules.
- <u>IXIA 400Tv2 Chassis</u>: Ixia 400Tv2 is a portable 4-slot chassis for Ixia standard form factor (SFF) load modules. It supports an integrated test controller that manages all chassis and testing resources.
- <u>XGS2 Chassis Platform</u>: The XGS2 chassis platform supports highly flexible and portable chassis that powers load modules and test applications to create an Ixia test system. It is a 2-slot, 3RU modular bench-top test chassis.

The following Ixia chassis are no longer available for sale:

- XG12 Chassis: The XG12 Chassis is the next generation high performance chassis platform capable of supporting next generation load modules. It is a 12 slot chassis with increased power and airflow delivery along with reservations for increased performance to the card. The 12-slot platform allows for higher port density load modules.
- Optixia XM12 Chassis: Capable of holding up to 12 Ixia load modules and equipped with extra power and fans required for high-powered load modules. Supports higher port density. Modules can be inserted and removed from the chassis without shutting the chassis down, and a load module can be removed without impacting the processes of other load modules. An optional Sound Reducer (PN 943-0021) can be installed on the rear of the XM12 chassis, to reduce the fan noise by approximately 10 dB. The XM12 High Performance version (PN OPTIXIAXM12-02) has two 2.0 kW power supply; the standard XM12 version has two 1.6 kW power supply.
- Optixia X16 Chassis: Capable of holding up to 16 Ixia load modules and equipped with extra power and fans required for some high-powered load modules. Modules can be inserted and removed from the chassis without shutting the chassis down, and a load module can be removed without impacting the processes of other load modules.
- IXIA 400T Chassis: Capable of holding up to four Ixia load modules and equipped with extra power and fans required for some high-powered load modules.
- IXIA 1600T Chassis: Capable of holding up to 16 Ixia load modules and equipped with extra power and fans required for some high-powered load modules.
- Ixia 100 Chassis: The IXIA 100 is capable of holding one Ixia load module and includes a built-in GPS or CDMA receiver.
- IXIA 250 Chassis: A portable Field Service Unit (FSU) which includes a single port (either copper 10/100/1000 or fiber 1000) and capable of holding up to two additional Ixia load modules. May optionally be equipped with a built-in CDMA receiver.

Optixia XL10 Chassis: Capable of holding a combination of high-density Ixia load modules with 24 ports. It supports up to 240 10/100/1000 Mbps ports. It is equipped with redundant power supplies. Modules can be inserted and removed from the chassis without shutting the chassis down, and a load module can be removed without impacting the processes of other load modules. The Optixia XL10 chassis includes sufficient power and airflow to support high-powered load modules.

All Ixia chassis have the ability to hold one or more standard load modules. Ixia load modules provide media dependent and independent ports to Devices Under Test (DUTs). Any of the chassis may be daisy-chained and provide synchronized operations.

Each chassis contains a self-contained computer running Windows XP Professional™ and includes a 10/100/1000MB network interface and local disk. They may include a floppy drive, a CD-ROM drive, or DVD-ROM drive. A chain of chassis may be controlled through a monitor, keyboard, and mouse directly connected to any of the chassis or remotely through the network interface card. Multiple users may safely share ports in a chassis chain. Several of the high-end load modules consume more power and generate additional heat. Only a limited number of such modules may be used in selected chassis. The basic characteristics of these chassis are compared in the following table. The process of initial chassis configuration is explained in Platform and Reference Overview. Each chassis is further described in its own chapter.

Ixia Chassis Comparison

Chassis	# of Slots	Special Feature	Mounting
XGS12 Chassis Platform	12	The XGS12 chassis platform is the next generation high performance platform capable of supporting all XM form factor load modules, including full chassis configurations of the Xcellon load modules. It is a 12-slot chassis platform with highspeed backplane (160 Gbps between each adjacent two cards) designed for aggregation across load modules.	Rack
XGS2 Chassis Platform	2	The 2-slot XGS2 chassis models - XGS2-SD and XGS2-HS provide highly flexible and portable chassis that powers load modules and test applications to create an Ixia test system. The XGS2 platform provides the foundation for a complete benchtop or rackmount test environment. The chassis platform supports Ixia applications for performance, functional, conformance, and security testing.	Desktop/Rack
Optixia XM2	2	Two slots for load modules. Modular subcomponents for higher serviceability. Higher port density. Hot-swappable load modules. DVD-ROM drive.  DVD Drive is not present in newer versions of XM2 chassis (starting with 941-0003-07 and 941-0023-02).	Desktop/Rack

Chassis	# of Slots	Special Feature	Mounting
400Tv2	4	A portable 4-slot chassis for Ixia standard form factor (SFF) load modules.	Desktop/Rack

NOTE

Based on power requirements, Ixia chassis do not support all possible mixes of load modules. The Ixia chassis notifies you of conflicts on chassis power-up. Contact Ixia support for configuration verification.

## **Chassis Regulatory Standards**

The Ixia XM12 chassis and XGS2 and XGS12 chassis platforms meet the following regulatory testing standards:

Regulatory Testing Standards

	Regulatory lesting Standards		
Standards	Deta	ails	
	X M 1 2	XGS2 and XGS12	
Safety - US/Canada	UL 60950-1, and CSA C22.2 No. 60950-1-07 - Information Technology Equipment	UL 60950-1, & CSA C22.2 No. 60950-1-07 - Information Technology Equipment	
Safety - Inter- national		IEC 60950-1:2005 (Second Edition); Am1:2009 + Am2:2013 (CB Scheme)	
US/Canada	FCC Part 15, Subpart B, Class A, ICES-003	FCC Part 15, Subpart B, Class A, ICES-003	
		Low Voltage: 2006/95/EC	
European Directives	Low Voltage: 2006/95/EC	EMC: 2004/108/EC	
Lui opean Directives	EMC: 2004/108/EC	RoHS: 2011/65/EU	
		WEEE: 2002/96/EC	
	Safety:		
	• EN 60950- 1:2006+A11+A1+A12	Safety: EN 60950- 1:2006+A11+A1+A12	
EU Product Family Standards for CE compliance	<ul> <li>EMC:</li> <li>EN 55022: 2006+A1:2007</li> <li>EN 61000-3-2: 2006</li> <li>EN 61000-3-3: 1995 + A2: 2005</li> <li>EN 55024:1998 A2: 2003</li> </ul>	<ul> <li>EMC: EN 55022: 2010</li> <li>EN 61000 -3 -2: 2006, A1: 2009 + A2: 2009</li> <li>EN 61000-3-3: 2008</li> <li>EN 55024: 2010</li> </ul>	

#### **Environmental Conditions**

The Ixia XG12 chassis and test cards cover a range of temperature and humidity specified as follows:

- Operating temperature range: 41°F to 104°F, (5°C to 40°C)
- Humidity range: 0% to 85% non-condensing

There are certain exceptions that lower the total operating temperature range as follows:

Some high-density/high performance load modules require a lower maximum ambient operating temperature than the operating temperature standard for the chassis. When a load module that requires the lower maximum operating temperature is installed in an XM12 or a XM2 chassis, the maximum operating temperature of the chassis is adjusted downward to match the maximum operating temperature of the load module. The operating temperature range specification is specified in the published datasheet for these load modules.

As of this date, the lowest operating temperature range of a load module (i.e. test card) is provided below.

 41°F to 86°F (5°C to 30°C), ambient air operating temperature is a specification that only applies to Ixia's highest density 10GbE test cards and dual-speed, dual-PHY 1GbE with a port of 10GbE test cards.

Thresholds for temperature and humidity beyond which the failure of components can occur are indicated.

Temperature thresholds for test cards installed into the XM12 or XM2 chassis can be set by the user.

The XM12 and XM2 chassis and the test cards that may be installed, and made operational in the chassis, do have inherent default thresholds that allow them to operate until a threshold is exceeded. A test card that has exceeded a default or user-defined temperature threshold will automatically shut down its operation.

The modular, field replaceable power supplies for the XM12 HP chassis are CE and UL approved units. The field replaceable power supplies for the XM2 chassis are CE and UL approved units.

### **Ixia Load Modules**

Ixia offers a number of load modules that provide one to 24 ports of technology and media dependent interfaces to DUTs. The load modules are divided into logical families. Each family of load modules is discussed in details in its own chapter in this manual.

- <u>IXIA Impairment Load Modules</u>: Offer 4x1GE, 4x10GE, or 2x40GE Ethernet interfaces that can emulate 64, 32, or 8 unidirectional network clouds respectively.
- IXIA Xcellon-Lava Load Modules: Provide testing of high-density data center 40 Gigabit Ethernet (40GbE) and 100 Gigabit Ethernet (100GbE) network equipments.
- <u>IXIA Power over Ethernet Load Modules</u>: Provide 10/100/1000 port emulation of network Powered Devices.
- IXIA 10/100/1000 Load Modules: Provide either 10 Mbps, 100 Mbps, or 1000 Mbps Ethernet speeds with auto-negotiation (except for Gigabit).
- IXIA Network Processor Load Modules: Provides details about Ixia's Xcellon-Ultra XP and Xcellon-Ultra NP load modules the specifications, features, and functionality. It also provides details on Xcellon-Ultra load module when it operates in IxN2X mode.
- IXIA 40/100 Gigabit Ethernet Load Modules: Provide 40 and 100 Gbps Ethernet with a variety of interfaces.

- IXIA 10 Gigabit Ethernet Load Modules: Provide 10 Gbps Ethernet with a variety of interfaces.
- <u>IXIA OC12 ATM/POS Load Modules</u>: Provide Asynchronous Transfer Mode (ATM) functions.
- IXIA 10/100 Load Modules: Utilize a copper interface and provide either 10 Mbps or 100 Mbps Ethernet speeds with auto-negotiation with or without a per-port CPU.
- IXIA 10GE LAN/WAN and OC 192 POS Load Modules: Provides Optical Carrier interfaces that operate in concatenated mode at OC192 or 10 Gigabit Ethernet rates. The
- load modules can operate in multiple modes 10G MSM, OC-192c Triple Mode and UNIPHY.
- <u>IXIA OC12c/OC3c Load Modules</u>: Provide selectable Optical Carrier interfaces that operate in concatenated mode at OC3 or OC12 rates. Packet over Sonet (POS) is implemented on the interfaces.
- <u>IXIA OC48c Load Modules</u>: Provide Optical Carrier interfaces that operate in concatenated mode at OC48 rates. Either Packet over Sonet (POS) or Bit Error Rate Testing (BERT) may be performed.
- IXIA FCMGXM Load Modules: Deliver high-density converged data center infrastructure for testing end-to-end Fibre Channel and Fibre Channel over Ethernet (FCoE) testing.
- <u>IXIA Xcellon-Flex Load Modules</u>: Deliver high-density, high performance test solutions.
- IXIA Xcellon-Multis Load Modules: Deliver highest density 40G and 100G higher speed Ethernet (HSE) test equipment, providing more flexible test coverage and 4x100GE, 12x40GE. 12x10GE, or dual-rate 40GE/100GE, all in a single-slot load module.
- IXIA Xcellon-Multis Reduced Load Modules: Deliver highest-density 10GE and 40GE higher speed Ethernet (HSE) test equipment, providing more flexible test coverage at upto 320 10GE ports per chassis, with a dual-rate 40GE/10GE and 40GE only capability, all in single-slot load module.
- <u>IXIA PerfectStorm Load Modules</u>: Provides a scalable solution for testing converged multi-play services, application delivery, and network security platforms for both wired and wireless networks.
- IXIA CloudStorm Load Modules: Provides the first multi-terabit application and security test solution, breaking the SSL and DDoS test barriers and achieving over 960Gbps of traffic with strong encryption and ciphers or 2.4 terabit DDoS throughput in a single chassis.
- <u>IXIA Xdensity XDM10G32S/8S Load Modules</u>: Provide test solutions for high density 10GE converged data center switches and routers.
- <u>IXIA XMVAE Ethernet Load Modules</u>: Provide test solutions for complete Layer 2-7 network and application testing functionality in a single test system for Automotive Ethernet switch and ECU testing.
- <u>IXIA Stream Extraction Modules</u>: Provide 10/100/1000 stream capture and analysis of network devices.
- <u>IXIA PerfectStormONE Appliances</u>: Provides a portable solution in a compact form factor appliance consisting of a single-slot chassis integrated with a load module that is hard-mounted in it.

Load modules with part numbers that contain -3 or -M are limited in their functionality. Newer boards also may have an `L' before the last number in their part number, signifying the same limited functionality. In general, -3 and -M modules do **not** have the following functions:

- Flows, except where Streams are not supported
- Advanced Streams (however, included with OC48C-3)
- Packet Groups (however, included with OC48C-3)
- Latency (however, included with OC48C-3)
- Sequence Checking (however, included with OC48C-3)
- Data Integrity (however, included with OC48C-M)
- Multiple DLCIs on OC48c load modules
- · Convert to streams in capture view
- · Protocol Server for router testing

- · Advanced Routing functions
- · Receive port filtering

#### Reduced vs. Full Feature

Some load modules are available in a Reduced Features version, which is identified by an `R' before the last number in their part number. The following table illustrates the differences for one family of cards, NGY.

Comparison of Full/Reduced Features, NGY Cards

	Standard	eXtra Performance 8- port	eXtra Per- formance	Reduced
PCPU	800 MHz	800MHz	1GHz	400MHz
PCPU Memory	512MB	1GB	1GB	128MB
Capture Memory	512MB	350MB	350MB	64MB
Table UDF Entries	1M	1M	1M	32K
UDF Range List	512K	512K	512K	256K
UDF Value List Entries	512K	512K	512K	256K
PGID	1M	1M	1M	64K

<sup>`</sup>L' modules do **not** have the following functions:

#### **Load Module Names**

The load module names used within the IxExplorer software differ slightly from the load module names used in Ixia marketing literature. The Load Module to IxExplorer Card Name Map below describes the mapping from load module names to the names in the Ixia price list and those used in IxExplorer. The reverse mapping, alphabetized, is shown in the Load Module to IxExplorer Card Name Map.

NOTE

Load modules without a price list column entry are no longer available for purchase.

Load Module to IxExplorer Card Name Map

Family	Load Module	Price List Names	IxExplorer Card Name
10/100 Ethernet	LM100TX8	LM100TX8	10/100 TX8
	LM100TXS8	LM100TXS8	10/100 TXS8
10/100/1- 000 Eth- ernet	ALM1000T8	ALM1000T8	10/100/1000 ALM T8
	Xcellon-Ultra XP-01	Xcellon-Ultra XP	Xcellon-Ultra XP
	Xcellon-Ultra NP-01	Xcellon-Ultra NP	Xcellon-Ultra NP
	Xcellon-Ultra NG-01	Xcellon-Ultra NG	Xcellon-Ultra NG
	ELM1000ST2	ELM1000ST2	10/100/1000 ELM ST2
	LM1000STX2	LM1000STX2	10/100/1000 STX2
	LM1000STX4	LM1000STX4	10/100/1000 STX4
	LM1000STXS2	LM1000STXS2	10/100/1000 STXS2
	LSM1000XMVR12-01	LSM1000XMVR12-01	10/100/1000 LSM XMV1210/100/1000 LSM XMVR12
	LSM1000XMVR8-01	LSM1000XMVR8-01	10/100/1000 LSM XMV810/100/1000 LSM XMVR8
	LSM1000XMVR4-01	LSM1000XMVR4-01	10/100/1000 LSM XMV410/100/1000 LSM XMVR4
	LSM1000XMSP12-01	LSM1000XMSP12-01	10/100/1000 LSM XMSP12
	LSM1000XMVDC4-01	LSM1000XMVDC4-01	10/100/1000 LSM XMVDC4

Family	Load Module	Price List Names	IxExplorer Card Name
	LSM1000XMVDC4-NG	LSM1000XMVDC4-NG	10/100/1000 LSM XMVDC4NG
	LSM1000XMVDC8-01	LSM1000XMVDC8-01	10/100/1000 LSM XMVDC8
	LSM1000XMVDC12-01	LSM1000XMVDC12-01	10/100/1000 LSM XMVDC12
	LSM1000XMVDC16-01	LSM1000XMVDC16-01	10/100/1000 LSM XMVDC16
	LSM10/100/1000XMVDC- 16NG	LSM10/100/1000XMVDC- 16NG	LSM10/100/1000XMVDC- 16NG
	LM1000GBIC-P1	n/a	GBIC-P1
ATM	LM622MR,	LM622MR w/ OPTATMMR,	ATM 622 Multi-Rate
AIN	LM622MR-512	LM622MR-512 w/ OPTATMMR	ATM 022 Multi-Rate
		LM622MR w/ OPTPOSMR	ATM/POS 622 Multi-Rate
		LM622MR w/ OPTATMMR+OPTPOSMR	ATM/POS 622 Multi-Rate
OC12c/OC- 3c	LMOC12c/LMOC3c	LMOC12c, LMOC12cSM	OC12c/OC3c POS
OC48	LMOC48cPOS		OC48c POS
	LMOC48cPOS-M		OC48c POS-M
	LMOC48cBERT		OC48c BERT
	LMOC48POS/BERT		OC48c POS/BERT
	LMOC48VAR		OC48c POS VAR
	MSM2.5G1-01	MSM2.5G1-01	2.5G MSM
OC192	LMOC192cPOS		OC192c POS
	LMOC192cVSR-POS		OC192c VSR POS
	LMOC192cBERT		OC192c BERT
	LMOC192cVSR-BERT		OC192c VSR BERT

Family	Load Module	Price List Names	IxExplorer Card Name
	LMOC192cPOS+BERT		OC192c POS/BERT
	LMOC192cVSR- POS+BERT		OC192c VSR POS/BERT
	LMOC192cPOS+WAN		OC192c POS/10GE WAN
	LMOC192cPOS+BERT+- WAN		OC192c POS/BERT/10GE WAN
10GE	LM10GELAN		10GE LAN
	LM10GELAN-M		10GE LAN-M
	LM10GEWAN		10GE WAN
	LSM10G1-01	LSM10G1-01	10GE LSM
	LSM10GMS-01	LSM10GMS-01	10GE LSM MACSec
	LM10GEXAUI		10GE XAUI
	LM10GEXAUI+BERT		10GE XAUI/BERT
	LM10GEXAUI BERT only		10GE XAUI BERT
	LM10GEXENPAK		10GE XENPAK
	LM10GEXENPAK-M		10GE XENPAK-M
	LM10GEXENPAK+BERT		10GE XENPAK/BERT
	LM10GEXENPAK- MA+BERT		10GE XENPAK-M/BERT
	LM10GEXENPAK BERT only		10GE XENPAK BERT
	LSM10GXMR8- 01LSM10GXM8XP- 01LSM10GXM8S- 01LSM10GXMR8S-01	LSM10GXMR8- 01LSM10GXM8XP- 01LSM10GXM8S- 01LSM10GXMR8S-01	10GE LSM XM810GE LSM XMR810GE LSM XM8XP10GE LSM XM8S10GE LSM XMR8S 10GE LSM XM8
	LSM10GXM8GBT- 01LSM10GXMR8GBT- 01NGY-NP8-01	LSM10GXM8GBT- 01LSM10GXMR8GBT- 01NGY-NP8-01	10GBASE-T10GE LSM XMR8 10GBASE-T NGY-NP8 (10GE LSM XM8-NP)
	LSM10GXMR4- 01LSM10GXM4XP- 01LSM10GXM4S- 01LSM10GXMR4S-01	LSM10GXMR4- 01LSM10GXM4XP- 01LSM10GXM4S- 01LSM10GXMR4S-01	10GE LSM XM410GE LSM XMR410GE LSM XM4XP10GE LSM XM4S10GE LSM XMR4S

Family	Load Module	Price List Names	IxExplorer Card Name
	LSM10GXM4GBT- 01LSM10GXMR4GBT-	LSM10GXM4GBT- 01LSM10GXMR4GBT-	10GE LSM XM4 10GBASE-T10GE LSM XMR4 10GBASE-T
	01NGY-NP4-01	01NGY-NP4-01	NGY-NP4 (10GE LSM XM4-NP)
	LSM10GXM2XP- 01LSM10GXMR2- 01LSM10GXM2S- 01LSM10GXMR2S-01 LSM10GXM2GBT- 01LSM10GXMR2GBT- 01NGY-NP2-01	LSM10GXM2XP- 01LSM10GXMR2- 01LSM10GXM2S- 01LSM10GXMR2S-01 LSM10GXM2GBT- 01LSM10GXMR2GBT- 01NGY-NP2-01	10GE LSM XM2XP10GE LSM XMR210GE LSM XM2S10GE LSM XMR2S 10GE LSM XM2 10GBASE-T10GE LSM XMR2 10GBASE-T NGY-NP2 (10GE LSM XM2-NP)
	MSM10G1-02	MSM10G1-02	10G MSM
	Xcellon-Ultra XP-01	Xcellon-Ultra XP	Xcellon-Ultra XP
	Xcellon-Ultra NP-01	Xcellon-Ultra NP	Xcellon-Ultra NP
	Xcellon-Ultra NG-01	Xcellon-Ultra NG	Xcellon-Ultra NG
40GE	HSE40GETSP1-01	HSE40GETSP1-01	40GE LSM XMV
100GE	HSE100GETSP1-01	HSE100GETSP1-01	100GE LSM XMV
40/100GE	HSE40GETSP1-01	HSE40GETSP1-01	40GE LSM XMV
	HSE100GETSP1-01	HSE100GETSP1-01	100GE LSM XMV
	HSE40/100GETSP1-01	HSE40/100GETSP1-01	40/100GE LSM XMV
	HSE40GEQSFP1-01	HSE40GEQSFP1-01	40GE LSM XMV QSFP
Power over Eth- ernet	PLM1000T4-PD	PLM1000T4-PD	Power over Ethernet PLM 20W
	LSM1000POE4-02	LSM1000POE4-02	Power over Ethernet PLM 30W
Stream Extraction Module	AFM1000SP-01	AFM1000SP-01	AFM - Stream Extraction Module
Voice Quality	VQM01XM	VQM01XM	Voice Quality Resource Module
Excellon- Flex	FlexAP10G16S		FlexAP10G16S

Family	Load Module	Price List Names	IxExplorer Card Name
	FlexFE10G16S		FlexFE10G16S
10GE Eth- ernet	Xdensity		XDM10G32S
ImpairNet	EIM10G4S		EIM10G4S
	EIM1G4S		EIM1G4S
Xcellon- Lava	Lava AP40/100GE 2P		Lava AP40/100GE 2P
	Lava AP40/100GE 2P		Lava AP40/100GE 2P

IxExplorer Card Name to Load Module Name Map (Alphabetical)

IxExplorer Card Name	Load Module Nam	Price List Names
10/100 TX8	LM100TX8	LM100TX8
10/100 TXS8	LM100TXS8	LM100TXS8
10/100/1000 ALM T8	ALM1000T8	ALM1000T8
10/100/1000 ELM ST2	ELM1000ST2	ELM1000ST2
10/100/1000 LSM XMSP12	LSM1000XMSP12-01	LSM1000XMSP12-01
10/100/1000 LSM XMVDC4	LSM1000XMVDC4-01	LSM1000XMVDC4-01
10/100/1000 LSM XMVDC4NG	LSM1000XMVDC4-NG	LSM1000XMVDC4-NG
10/100/1000 LSM XMVDC8	LSM1000XMVDC8-01	LSM1000XMVDC8-01
10/100/1000 LSM XMVDC12	LSM1000XMVDC12-01	LSM1000XMVDC12-01
10/100/1000 LSM XMVDC16	LSM1000XMVDC16-01	LSM1000XMVDC16-01
10/100/1000 LSM XMVDC16NG	10/100/1000 LSM XMVDC16NG	10/100/1000 LSM XMVDC16NG
10/100/1000 LSM XMV1210/100/1000 LSM XMVR12	LSM1000XMVR12-01	LSM1000XMVR12-01
10/100/1000 LSM XMV810/100/1000 LSM XMVR8	LSM1000XMVR8-01	LSM1000XMVR8-01
10/100/1000 LSM XMV410/100/1000 LSM	LSM1000XMVR4-01	LSM1000XMVR4-01

IxExplorer Card Name	Load Module	Price List Names
XMVR4		
10/100/1000 STX2	LM1000STX2	LM1000STX2
10/100/1000 STX4	LM1000STX4	LM1000STX4
10/100/1000 STXS2	LM1000STXS2	LM1000STXS2
2.5G MSM	MSM2.5G1-01	MSM2.5G1-01
10G MSM	MSM10G1-02	MSM10G1-02
10GE LAN	LM10GELAN	
10GE LAN-M	LM10GELAN-M	
10GE LSM	LSM10G1-01	LSM10G1-01
10GE LSM MACSec	LSM10GMS-01	LSM10GMS-01
10GE LSM XM810GE LSM XMR810GE LSM XM8XP10GE LSM XM8S10GE LSM XMR8S 10GE LSM XM8 10GBASE-	LSM10GXMR8- 01LSM10GXM8XP- 01LSM10GXM8S- 01LSM10GXMR8S-01	LSM10GXMR8- 01LSM10GXM8XP- 01LSM10GXM8S- 01LSM10GXMR8S-01
T10GE LSM XMR8 10GBASE- T	LSM10GXM8GBT- 01LSM10GXMR8GBT-01	LSM10GXM8GBT- 01LSM10GXMR8GBT-01
NGY-NP8	NGY-NP8-01	NGY-NP8-01
10GE LSM XM410GE LSM XMR410GE LSM XM4XP10GE LSM XM4S10GE LSM XMR4S 10GE LSM XM4 10GBASE- T10GE LSM XMR4 10GBASE-	LSM10GXMR4- 01LSM10GXM4XP- 01LSM10GXM4S- 01LSM10GXMR4S-01 LSM10GXM4GBT-	LSM10GXMR4- 01LSM10GXM4XP- 01LSM10GXM4S- 01LSM10GXMR4S-01 LSM10GXM4GBT-
Т	01LSM10GXMR4GBT-01	01LSM10GXMR4GBT-01
NGY-NP4	NGY-NP4-01	NGY-NP4-01
10GE LSM XM2XP10GE LSM XMR210GE LSM XM2S10GE LSM XMR2S	LSM10GXM2XP- 01LSM10GXMR2- 01LSM10GXM2S- 01LSM10GXMR2S-01	LSM10GXM2XP- 01LSM10GXMR2- 01LSM10GXM2S- 01LSM10GXMR2S-01
10GE LSM XM2 10GBASE- T10GE LSM XMR2 10GBASE- TNGY-NP2	LSM10GXM2GBT- 01LSM10GXMR2GBT-01 NGY-NP2-01	LSM10GXM2GBT- 01LSM10GXMR2GBT-01 NGY-NP2-01
10GE WAN	LM10GEWAN	LM10GE123F,LM10GE124F
10GE XAUI	LM10GEXAUI	
10GE XAUI BERT	LM10GEXAUI BERT only	

IxExplorer Card Name	Load Module	Price List Names
10GE XAUI/BERT	LM10GEXAUI+BERT	
10GE XENPAK	LM10GEXENPAK	
10GE XENPAK BERT	LM10GEXENPAK BERT only	
10GE XENPAK/BERT	LM10GEXENPAK+BERT	
10GE XENPAK-M	LM10GEXENPAK-M	
10GE XENPAK-M/BERT	LM10GEXENPAK-MA+BERT	
40GE LSM XMV	HSE40GETSP1-01	HSE40GETSP1-01
100GE LSM XMV	HSE100GETSP1-01	HSE100GETSP1-01
40/100GE LSM XMV	HSE40/100GETSP1-01	HSE40/100GETSP1-01
40GE LSM XMV QSFP	HSE40GEQSFP1-01	HSE40GEQSFP1-01
Xcellon-Ultra NP	Xcellon-Ultra NP-01	Xcellon-Ultra NP
Xcellon-Ultra XP	Xcellon-Ultra XP-01	Xcellon-Ultra XP
Xcellon-Ultra NG	Xcellon-Ultra NG-01	Xcellon-Ultra NG
AFM1000SP-01	AFM Stream Extraction Mod- ule	AFM1000SP-01
ATM 622 Multi-Rate	LM622MR	LM622MR w/OPTATMMR
ATM/POS 622 Multi-Rate		LM622MR w/OPTPOSMR
ATM/POS 622 Multi-Rate		LM622MR w/ OPTATMMR+OPTPOSMR, LM622MR-512 w/ OPTATMMR+OPTPOSMR
GBIC-P1	LM1000GBIC-P1	
OC12c/OC3c POS	LMOC12c/LMOC3c	LMOC12c, LMOC12cSM
OC192c BERT	LMOC192cBERT	
OC192c POS	LMOC192cPOS	
OC192c POS/10GE WAN	LMOC192cPOS+WAN	
OC192c POS/BERT	LMOC192cPOS+BERT	
OC192c POS/BERT/10GE WAN	LMOC192cPOS+BERT+WAN	
OC192c VSR BERT	LMOC192cVSR-BERT	

IxExplorer Card Name	Load Module	Price List Names
OC192c VSR POS	LMOC192cVSR-POS	
OC192c VSR POS/BERT	LMOC192cVSR-POS+BERT	
OC48c BERT	LMOC48cBERT	
OC48c POS	LMOC48cPOS	
OC48c POS VAR	LMOC48VAR	
OC48c POS/BERT	LMOC48POS/BERT	
OC48c POS-M	LMOC48cPOS-M	
Power over Ethernet	LM1000T4-PD	LM1000T4-PD
Voice Quality Resource Mod- ule	VQM01XM	VQM01XM
Lava AP40/100GE 2P	Lava AP40/100GE 2P	
Lava AP40/100GE 2P	Lava AP40/100GE 2P	

# **Ixia Load Module Properties**

The Ixia load modules, or load modules, support a wide range of features, which are described in the following table.

The full set of supported features per card is described in the spreadsheet *Port Features by Port Type* on the *Ixiacom.com* website, under *Support/User Guides/Spreadsheets*.

Ixia Load Module Feature Descriptions

Feature Category	Feature	Usage
Basic	Local CPU	Each port on the card is supported by an individual CPU for use in protocol server and other sophisticated operations.
	Layer 2/3 Only	The card only supports Layer 2 and 3 control and operation. No protocols except ARP and PING are supported.
	Layer 7 Only	The card only supports Layer 7 usage through the local CPU. This type of card is generally only useful for application testing as in IxLoad and Chariot.
Statistics Selection	Checksum errors (IPv4/TCP/UDP)	Support generation and checking of special checksums for IPv4, TCP, and UDP packets.
	Data integrity	Supports data integrity generation and checking.
	Tx Duration	Supports the generation of a transmit duration stat-

Feature Category	Feature	Usage
		istic.
	Per stream stats	Statistics are available for each stream.
Receive Modes	Capture	Received data may be captured to a capture buffer.
	Packet groups	Supports generation of packet group IDs in packets.
	Latency S&Fwd LB to FB	Latency measurement offers the option of measuring the time from last data bit out to first data bit in
	Latency S&Fwd LB to FP	Latency measurement offers the option of measuring the time from last data bit out to first preamble bit in
	Inter-arrival Jitter	Inter-Arrival Time (IAT) compares the time between PGID packet arrivals. In this case, when a packet with a PGID is received, the PGID is examined. If a packet has already been received with the same PGID, then the timestamp of the previous packet is subtracted from the current timestamp.
		The interval between the timestamps is the jitter, and it is recorded for statistical purposes.
	Delay Variation	Offers the option of measuring variation between latency of consecutive frames.
	MEF Frame Delay	Measurement method: First data bit in to DUT; last data bit out of DUT.
	Forwarding Delay	Measurement method: Last data bit in to DUT; last data bit out of DUT.
	Advanced PG Filter	A set of features which allow packet group matching to ignore or mask:  Group ID Signature Filter data
	Round-trip flows	Supports calculation of round-trip flows.
	Data integrity	Supports data integrity generation and checking.
	First time stamp	Supports first time stamp operation.
	Tx/Rx Time Stamp Mode	Allows the system to use the time stamp of the last bit of the packet; this is useful when multiple

Feature Category	Feature	Usage
		rates are present in the network topology.
	Sequence checking	Supports packet sequence generation and verification.
	Sequence checking per packet ID	When packet groups are used, allows sequence checking generation and verification.
	ISL encapsulation	Receive side of port can accommodate ISL encapsulation on receive side.
	Small packets	Supports the ability to capture packets smaller than a legal packet; captured data may be corrupted when this feature is used.
	Wide packet groups	This feature allows ports, which utilize packet groups, to extend the number of bits in the PGID to 17 bits (or more).
	PRBS Mode	When the Receive Mode is set to PRBS mode, both Wide Packet Groups and Sequence Checking are automatically enabled. In PRBS mode, all latency-related statistics are removed and the following per PGID statistics are added:
		<ul><li>PRBS Bits Received</li><li>PRBS Errored Bits</li><li>PRBS BER</li></ul>
	Split PGIDs	Allows for the creation of split PGID data.
	Latency bins	Latency data may be categorized by latency values for each packet group.
	Time bins	Latency may be measured over time.
	Echo	Ports with this feature may echo all received traffic as transmitted packets.
	Preamble capture	Frame's preamble may be included in the capture buffer.
	Simulate cable disconnect	A cable disconnect state may be simulated.
	Flexible Pattern Offset	Allows to set the Filter/Trigger pattern to a specific offset.
	Multi Switched-Path	Allows for the detection of loss/duplicate packets.
	Intrinsic Latency Adjustment	Reduces the measured latency by the amount of latency that is induced by the test equipment itself (not the DUT). Retrieves pre-determined latency

Feature Category	Feature	Usage
		value for a `known' transceiver, or calculates and stores that value for a `new' transceiver.
	Misdirected Mask	Sets the signature mask used for identifying misdirected packets.
	Rate Monitoring (convergence)	Enables testing convergence times and service interruptions.
	Auto-Detect Instru- mentation	On the receive side, automatically detects a specified signature and Instrumentation parameters for Data Integrity, Sequence Checking, or Latency for streams generated with Automatic Instrumentation Offsets using Ixia software applications.
	TSO/LRO	Transmit Segmentation Offload/Large Receive Offload (TSO/LRO) operation mode.
Transmit Modes	Packet streams	Supports the generation of packet streams.
	Packet flows	Supports the generation of packet flows.
	Advanced scheduler	Supports the operation of the advanced scheduler, which allows inter-mixing of multiple packet streams.
	Forced collisions	Supports the insertion of forced collisions.
	Tx Data integrity	Supports data integrity generation and checking.
	Odd preamble	Supports the ability to send a preamble with an odd number of bytes. This is not applicable to boards with dual PHYs (Ethernet/Fiber) when a port is in fiber mode.
	Gap time units	The inter-frame, -burst, and -stream gaps can be programmed in discreet units of time as opposed to indirectly through a percentage of maximums frame rate.
	Gap byte count	Gaps may be expressed as a number of bytes.
		The packet's preamble content may be modified.
	Modifiable preamble	On 10GE load modules that support this feature there are two options: modify the 7 rightmost bytes of the 8 byte preamble or modify the inner 6 bytes of the 8 byte preamble.
	Forced minimum IPG	In advanced scheduler mode, a minimum gap may be enforced.

Feature Category	Feature	Usage
	Increment frame size by N	Frame sizes may be incremented by an arbitrary value between transmitted frames.
	Increment/Decrement DA/SA by N	DA and SA values may be incremented or decremented by an arbitrary value between transmitted frames.
	Random data on even offset only	When random data is generated within a frame's content, the random data may only be placed at even byte boundaries.
	Insert bad TCP check- sum	Supports the generation of bad TCP checksums.
	Checksum Override	Overrides IPv4, IPv6 and TCP checksums.
	Frequency offset	The frequency for the card as a whole may be modified a few percent from nominal.
	Echo	The port echoes all received packets.
	Flexible Time Stamp	The position of the time stamp in transmitted packets may be repositioned.
	Protocol Offset	The beginning of the IP (or other) protocol header may be repositioned so as to accommodate leading headers, as in PPP.
	Random IPG	The IPG between packets may be set to a random value.
	Copper RJ45/Fiber SFP	The port has the ability to transmit and receive from either its copper RJ-45 Ethernet or Fiber SFP optic interface.
	Weighted Random Frame Size	The port has the ability to generate packets with random frame sizes. The frame sizes are programmed through a set of frame sizes and weightings.
	Scheduled duration	The duration of the transmit operation may be scheduled for a number of seconds.
	Simulate cable dis- connect	A cable disconnect state may be simulated.
	Repeatable Random Streams	Allows for repeating randomly generated stream data.
	GRE	An IP transport protocol available for insertion into transmitted streams.
	Stacked VLANs	Allows for sending multiple VLAN IDs in a single

Feature Category	Feature	Usage
		packet.
	Tx Ignore Link	Allows for transmission of packets with the link down.
	Protocol Pad	Allows for a data pad to be added before the protocol head field in a frame.
	Dynamic Rate Change	Allow rate change without stopping transmit.
	Dynamic Frame Size Change	Allow frame size change without stopping transmit.
	New Incrementing Frame Size	Allow packets/burst setting in incrementing frame size mode
	Auto-Detect Instru- mentation	On the transmit side, automatically configures a specified signature and Instrumentation parameters for Data Integrity, Sequence Checking, Latency, or PRBS for streams generated for Ixia software applications that use Automatic Instrumentation Offsets.
	Intrinsic Latency Adjustment	Reduce the measured latency by the amount of latency that is induced by the test equipment itself (not the DUT). Retrieves pre-determined latency value for a `known' transceiver, or calculates and stores that value for a `new' transceiver.
	PRBS	When the port is in PRBS mode, all latency-related statistics are removed and the following per-PGID statistics are added:  • PRBS Bits Received  • PRBS Errored Bits  • PRBS BER
	TSO/LRO	Transmit Segmentation Offload/Large Receive Offload (TSO/LRO) operation mode.
User Defined Fields (UDF)	Odd offset	UDFs are allowed to start at an odd offset.
	Overlap	UDFs may overlap within a 4-octet boundary. Otherwise UDFs must start at least 4 octets apart.
	Cascade	UDFs may continue from previous stream values.
	Cascade from self	UDFs may continue from previous values on the

Feature Category	Feature	Usage
		same UDF.
	Split	UDFs may be split into multiple 8-bit and 16-bit counters.
	Bit mask	UDFs output data may be masked with an arbitrary bit mask. Otherwise limitations on the number of changes of bits applies.
	Incr By N	Allows UDFs to increment by an arbitrary value.
	UDF5	The port has a fifth UDF.
	Advanced	The port supports additional UDF features, including:  • Nested counters • Linked lists
		<ul><li>Step size</li><li>Value list</li><li>Range list</li></ul>
	IPv4	The port supports UDF - IPv4 type counting.
	Range List	The port supports UDF generated values over a list of value ranges.
	Value List	The port supports UDF generated values from a list of values.
	Nested Counter	The port supports UDF generated values from two nested counters.
	Table	The port supports a UDF that derives values from a table of offsets and values, by packet.
	Chained UDFs	The port supports the ability to chain from a specified UDF.
	Protocol Pad	Allows for a data pad to be added before the protocol head field in a frame.
POS/BERT	POS	Supports Packet over SONET operation.
	BERT	Supports Bit Error Rate Testing through the generation and verifications of patterns.
	Channelized BERT	Support channelized BERT testing.
	BERT error insertion	Supports BERT error insertion.
	DCC	Supports additional DCC channel streams.

Feature Category	Feature	Usage
	SRP	Supports Serial Reuse Protocol passive receive.
	SRP Full	Supports Serial Reuse Protocol active send/receive.
	RPR	Supports Resilient Packet Ring operation.
	FEC	Support Forwarding Error Correction.
	GFP	Supports the Generic Framing Protocol.
	SONET error insertion list	Support the insertion of Sonet errors.
	Multiple DLCIs	Supports the use of more than one DLCI in frame relay testing.
	CJPAT/CRPAT	Supports generated CJPAT and CRPAT frame data patterns.
10 Gigabit Ethernet	OC192	Supports OC192 POS operation.
	WAN	Supports 10 GE WAN operation.
	LAN	Supports 10 GE LAN operation.
	XAUI	Supports 10GE XAUI interface.
	XENPAK	Supports 10GE XENPAK interface.
	LASI	Supports Link Alarm Status Interrupt.
	XFP	Supports an XFP interface.
	SFP	Supports an SFP (small form-factor pluggable) transceiver interface.
	UNIPHY	Supports UNIPHY operation, which allows the same port to operate in LAN, WAN, POS and BERT modes.
	Lane skew	Supports the ability to skew multiple PCS (Physical Coding Sublayer) lanes.
	Set pause destination address	The destination for pause control packets may be set.
	Link Fault Signalling	Supports the link fault signalling protocol.
	Gap Control Mode	Allows for the selection of the gap control algorithm, as defined by IEEE.
	Pre-Emphasis	Allows for boosting transmit signal.

Feature Category	Feature	Usage
	MACSec	Supports MACSec functionality.  Media Access Control Security (MACsec) is a L2 protocol which authenticates the entire L2 frame (except for the Ethernet CRC) and provides confidentiality for all or some of the MACsec data segment. This protocol is defined in IEEE 802.1AE
Protocol Server	Basic Routing	Supports basic routing protocols, including BGP, IS-IS and OSPF, but none of those in the list for Advanced Routing.
	DHCP	Supports the DHCP protocol.
	DHCPv6	Supports the DHCPv6 protocol.
	Advanced Routing (note 1)	Supports advanced routing protocols:  BGP-IPv6  IGMP (new) with IPMPv3  ISIS-IPv6  OSPFv3  PIM-SM  Layer 2 VPN (LDP)  Layer 3 VPN (BGP)  MLD  RIPng
	ARP	Supports ARP generation and receipt handling.
	Gratuitous ARP	Gratuitous ARP is sent by the host when its IP to MAC mapping changes, so that everybody else on the subnet updates their ARP tables.
	ARP rate control	The rate at which multiple ARP packets are transmitted may be controlled.
	IGMP rate control	The rate at which multiple IGMP packets are transmitted may be controlled.
	PING	Supports PING generation and receipt.
	FCoE/NPIV	Supports Fibre Channel over Ethernet and N_Port_ ID Virtualization.
	PTP	Supports Precision Time Protocol.
	RTP	Supports Real-time Transport Protocol.

NOTE

On older OC48c, OC192c and 10GE modules, these protocols require that the ports have been upgraded to 128MB of CPU memory.

# **Card Properties**

Details about the card characteristics described in the following table are presented in the chapters about specific load modules.

Card Specifications

Specification	Usage
# ports	The number of ports supported by the card(s).
-3/-M/L Card Available	Whether a limited feature card is available.
L2/L3 Card Available	Whether a Layer 2/3 only card is available.
Layer 7 Card Available	Whether a Layer 7 only card is available.
Data Rate	The choice of data rates offered by the card.
Connector/Frequency- Mode	The connector type used on the card. For optical connections, the light frequency used and whether the fiber is used for singlemode or multimode.
Capture buffer size	The size of each port's capture buffer.
Captured packet size	The range of packet sizes that may be captured on the card.
Streams per port	The number of streams available on each port.
Flows per port	The number of stream flows available on each port. If available, this is always 15,872.
Advanced streams	The number of advanced streams available on each port.
Preamble size: min-max	The range of sizes, in bytes, for generated preambles.
Frame size: min-max	The range of sizes, in bytes, for generated frames.
Inter-frame gap: min- max	The gap between frames, expressed as a range of time.
Inter-burst gap: min- max	The gap between bursts of frames, expressed as a range of time.
Inter-stream gap: min- max	The gap between streams, expressed as a range of time. Sometimes expressed as a percentage of the maximum rate.
Latency	The accuracy of latency operations.
Intrinsic Latency Adjust- ment	Reduce the measured latency by the amount of latency that is induced by the test equipment itself (not the DUT). Retrieves pre-determined latency value for a `known' transceiver, or calculates and stores that value for a `new' transceiver.

Number of captured packets, an important characteristic, cannot be expressed as a simple number. It is dependent on a number of factors as mentioned in the following list:

- Size of the capture buffer
- Size of the captured packet
- Size of the capture slice, set by you
- Memory used by other functions
- Memory overhead per captured packet

The general equation is:

# of captured packets = (size of capture buffer) - (memory used by other functions) (min (captured packet, capture slice) + (per packet overhead)

## **Maximum number of PGIDs**

The maximum number of PGIDs for designated load module families is provided in the following table.

Maximum PGID Summary

Load Module Family	Receive Mode	Maximum Number PDIDs <sup>1</sup> Decimal
LM100TXS8		
	Packet Group	65536
	Packet Group + Sequence Checking	128
	Capture + Sequence Checking	128
	Wide Packet Group	131072
LSM1000XMSP12-01		
	Packet Group	65536
	Packet Group + Sequence Checking	128
	Capture + Sequence Checking	128
	Wide Packet Group	131072
	Wide Packet Group (Reduced Feature)	65536
LSM1000XMV (4, 8, 12, and 16-port)		
	Wide Packet Group	131072
	Wide Packet Group (Reduced Feature)	65536
	Wide Packet Group/Wide Bin Mode (Full Feature)	1048576
ASM1000XMV	Wide Packet Group/Wide Bin Mode	1048576
7.65.12500/111	That I defice of oup, while bill house	1010070
LSM10G including MSM10G and MSM2.5G		
	Wide Packet Group	2097152
	Wide Packet Group (Reduced	65536

Load Module Family	Receive Mode	Maximum Number PDIDs <sup>1</sup> Decimal
	Feature)	
100GE LSM XMV, 40GE LSM XMV, and 40/100GE LSM XMV	Wide Packet Group	1048576
LM10G and LM10GE		
	Packet Group	65536
	Sequence Checking	8192
	Packet Group + Sequence Checking	8192
LMOC-12		
	Packet Group	57344
	Sequence Checking	N/A
LMOC-48		
	Packet Group	65536
	Packet Group + Sequence Checking	
	Capture + Sequence Checking	512
LMOC-192		
LIMOC-192	Dacket Croup	1024
	Packet Group Sequence Checking	1024
	Packet Group + Sequence Checking	
	Wide Packet Group	131072
LM622MR		
LIMOZZIMK	Packet Group	65536
	Packet Group + Sequence Checking	
		128
	Capture + Sequence Checking Wide Packet Group	131072
LavaAP40/100GE		
	Sequence Checking	1048576
	Data Integrity	
	Wide Packet Groups	1048576
	Latency/Jitter	

<sup>1</sup>The maximum number of PGIDs is the maximum hardware PGID that can be supported by a particular load module in a particular mode. If time bin, latency, or other parameters are enabled, the maximum PGID that can be supported is reduced. All modules have a maximum 2048 time bins. All modules that support latency bins have quantity 16 latency bins.

### **New in Version 8.21 EA**

The following new features are added for 8.21 EA:

#### **Novus-M**

Novus-M is a family of load modules which provides L2-3 support with complete protocol coverage, and mid-range scale and performance protocol emulation for routing, switching and access protocols. For details, see Novus-M.

#### **Novus-NP**

Novus NP 10/1 combines the architecture of Novus load modules with Ixia's NP (network processor) technology. This load module family supports complete Layer 2-7 (L2-7) network and application testing in a single system and provides support for Dual-PHY (SFP+ and 10GBase-T RJ45). For details, see Novus-NP.

#### Novus-32P

Ixia's Novus-32P family of load modules supports complete Layer 2-3 (L2-3) network and application testing in a single system. It supports SFP+ ports, L2/3 traffic generation and analysis, routing/bridging protocol emulation, and L4-3 application traffic generation and subscriber emulation. For details, see Novus-32P.



# **Chapter 2 - Theory of Operation: General**

This chapter discusses the unifying concepts behind the Ixia system. Both the software and hardware structures, and their usage, are discussed. The chapter is divided into the following major sections:

- Ixia Hardware
- IxExplorer Software

#### **Ixia Hardware**

This section discusses the range and capabilities of the Ixia hardware, including general discussions of several technologies used by Ixia hardware. This section is divided into the following general areas:

- Chassis Chain (Hardware)
- Chassis
- Load Modules
- Port Hardware
  - Types of Ports
  - Port Transmit Capabilities
  - Port Data Capture Capabilities
  - Port Transmit/Receive Capabilities
  - Port Statistics Capabilities

## **Chassis Chain (Hardware)**

For daisy chain, the Ixia hardware can be structured as a chain of different types of chassis, up to 256 units. For a star topology, the Ixia hardware can be structured as a chain of different types (with restrictions) of chassis, up to 5. The following table describes the chassis available for the two types of chains:

Currently Available Ixia Chassis

Chassis	Number of Load Modules Supported	Daisy chain	Star
XG/XGS	12 high density modules	Yes	Yes
XM12	12 high density modules	Yes	Yes (slave only)
XM2	Two high density modules	Yes	Yes (slave only)
X16	16 standard load modules	Yes	No

All non-Optixia chassis support load modules that each may contain one to 8 ports. Up to 16 ports per load module are supported on Optixia XM2 and XM12 chassis, which can result in a very large number of ports for the overall system.

Multiple Ixia chassis are chained together through special Sync-out/Sync-in cables that allow for port-to-port synchronization across locally connected chassis in accordance with the specification mentioned in the Chassis Chain Timing Specification section.

## **Daisy Chain**

There are several rules that must be observed when connecting chassis in daisy chains. If a rule is violated, chassis timing may not meet the specification.

- Sync cable length between two chassis in a chain should be less than or equal to 6 feet.
- In a physical chassis chain, the Optixia chassis must be grouped together, and the non-Optixia chassis must be grouped together; that is, the two types can be on the

same chassis chain, but cannot be intermingled. In a virtual chain that consists of several physical chains, each physical chain must obey this rule.

- Sequence numbers must be unique in a chain. Within a chain, there cannot be duplicate sequence numbers. The master chassis must have the smallest sequence value in the physical chain. The order of sequence numbers must match the order of chassis (up to 99999). The numbers do not have to be sequentially contiguous (1, 2, 3, and so on.) but they must be sequentially increasing in value (1, 5, 8, and so on.)
- Certain load modules must be used in only the first 3 chassis in a chain. These include LM100TXS8, LM100TXS2, LM100TX8, and LM100TX1. If these boards are used in the fourth or later chassis in a chain, the network ports may not operate reliably.

The following figure is a representation of an independent Ixia chassis chain and control network. Chassis are chained together through their sync cables. The first chassis in a chain has a Sync-out connection (but no Sync-in unless it is the AFD1 GPS receiver), and is called the *master* chassis. All other chassis in the chain are termed *subordinates*.

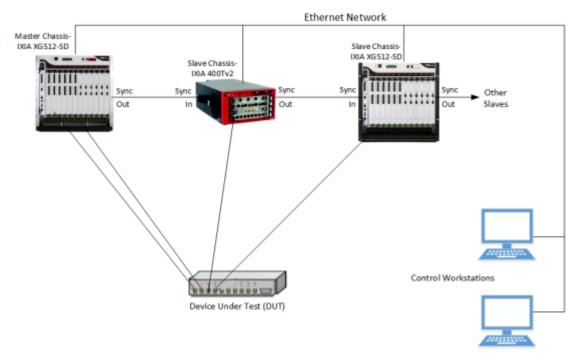


Figure: Ixia Chassis chain and Control Workstation

# **Star Topology**

There are several rules that must be observed connecting chassis in star topology. If a rule is violated, chassis timing may not meet the specification.

- Sync cable length between two chassis in a chain should be less than or equal to 6 feet.
- Only XG/XGS chassis can be the master of the chain.
- Only Optixia chassis (XG/XGS, XM2, XM12) chassis can be slaves.

All four sync out ports on the XG12 and XGS12 chassis shall be available for synchronization connection to slave chassis.

Figure: XG12 chassis sync-out ports

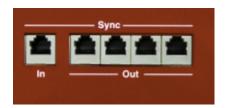


Figure: XGS12 chassis sync-out ports



In current deployment of these chassis, one sync-out port is available, and 3 additional sync-out ports are covered. There shall be a maximum of 5 synchronized chassis per system when deployed in the Star Topology with one slave connected to each of the 4 sync-out ports on the master. When there are fewer than 5 chassis, slaves may be connected to any sync-out port on the master.

You can choose to daisy chain chassis, or use star topology, but cannot combine the two.

Figure: Ixia Daisy Chain and Star Topology

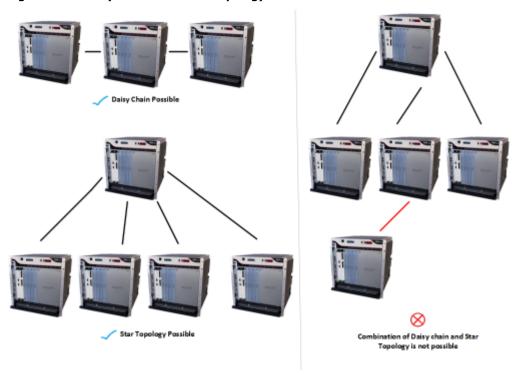
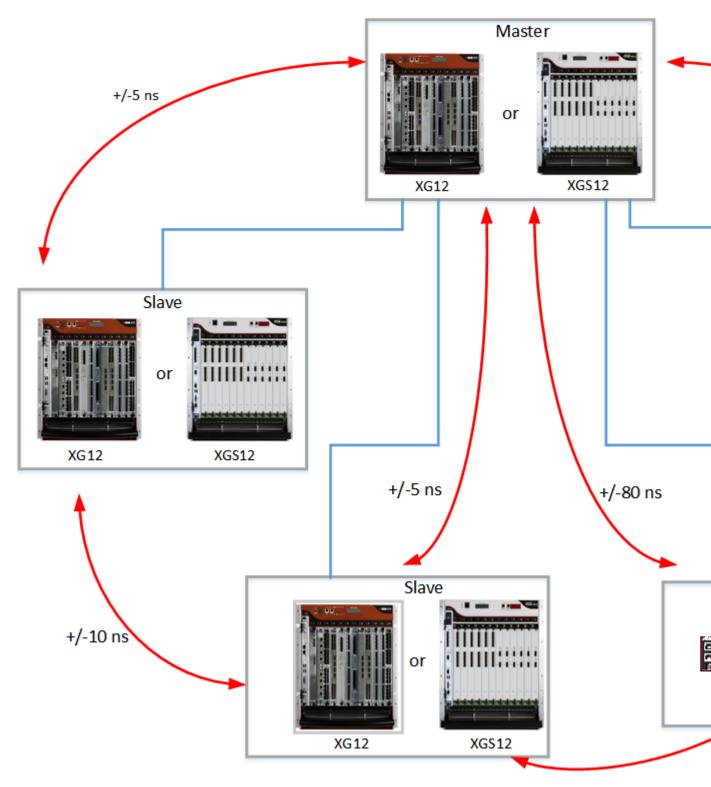


Figure: Ixia Star Topology chassis chain



Multiple, geographically-separated, independent chassis may be synchronized with a high degree of accuracy by using an Ixia chassis. Specific chassis include an integral GPS or CDMA receiver which is used for worldwide chassis synchronization. See <a href="Chassis Synchronization">Chassis Synchronization</a> for a complete discussion of chassis timing.

NOTE

Plugging-in or removing the sync cable while IxServer is starting or running can cause the IxServer to detect the change in the sync-in connection and shut down. If this occurs, restart IxServer, then restart all Ixia applications.

Ports from the chassis are connected to the Device Under Test (DUT) using cables appropriate for the media. Ports from any chassis may be connected to the similar ports on the DUT. It is even possible to connect multiple independent DUTs to different ports on different chassis.

Each chassis is driven by an Intel Pentium-based computer running Windows XP Professional and Ixia-supplied software. Each chassis may be directly connected to a monitor, keyboard, and mouse to create a standalone system, but it is typical to connect all chassis through an Ethernet network and run the IxExplorer client software or Tcl client software on one or more external control PC workstations. IxExplorer client software runs on any Windows 2000/XP based system or Windows Server 2003 (console usage or simultaneous remote terminal access for multiple users). Tcl client software runs on Windows 2000/XP based systems and several Unix-based systems.

## **Chassis Chain Timing Specification**

Depending on the chassis topology, there are different timing skews between chassis.

#### For daisy chain:

- Chassis timing skew between similar XG/XGS chassis <= +/- 5ns.
- Chassis timing skew between similar chassis (except XG and XGS) <= +/- 40ns.
- Chassis timing skew between different chassis <= +/- 80ns.

#### Based on the above numbers:

- Maximum latency error between similar XG/XGS chassis due to the chassis <= +/5ns.</li>
- Maximum latency error between similar chassis (except XG and XGS) due to the chassis <= +/- 40ns.
- Maximum latency error between different chassis due to the chassis <= +/- 80ns.</li>

#### For star topology:

- Chassis timing skew between similar XG/XGS chassis one master and one slave <= +/- 5ns.
- Chassis timing skew between similar XG/XGS chassis both slaves <= +/- 10ns.
- Chassis timing skew between similar chassis (except XG and XGS) both slaves <= +/- 160ns.
- Chassis timing skew between different chassis (XG master, XM slave) <= +/- 80ns.</li>
- Chassis timing skew between different chassis (XG slave, XM slave) <= +/- 85ns.</li>

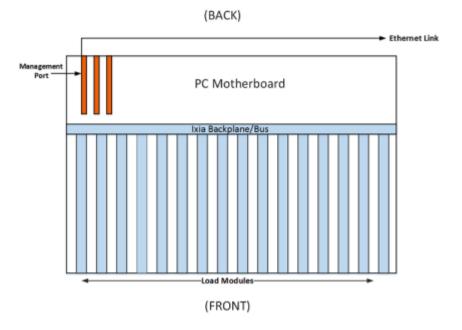
#### Based on the above numbers:

- Maximum latency error between similar XG/XGS chassis due to the chassis <= +/10ns.</li>
- Maximum latency error between similar chassis (except XG and XGS) due to the chassis <= +/- 160ns.</li>
- Maximum latency error between different chassis due to the chassis <= +/- 85ns.

## Chassis

Each Ixia chassis can operate as a complete standalone system when connected to a local monitor, keyboard, and mouse. The interior of an Ixia XGS12-SD chassis is shown in the following figure.

Figure: Ixia XGS12-SD Interior View (Top View)



The PC embedded in the chassis system is an Intel-compatible computer system which includes the following components:

- A Pentium processor
- Main memory
- · Keyboard interface
- Mouse interface
- Internal connection to the Ixia Backplane
- Video interface capable of 1024 x 768 or greater resolution
- Management Port

The Ixia Backplane is connected to the PC Motherboard, through an Ixia custom PCI interface card, and to the card slots where the Ixia load modules are installed.

# **Chassis Synchronization**

Measurement of unidirectional latency and jitter in the transmission of data from a transmit port to a receive port requires that the relationship between time signatures at each of the ports is known. This can be accomplished by providing the following signals between chassis:

Clock (frequency standard): This allows chassis to phase-lock their frequency standards so that a cycle counter on any chassis counts the same number of cycles during the same time interval. Each Ixia port maintains such a counter from a common chassis-wide frequency standard.

 Reset: A means must exist to either discover the fixed offset between their counters, or to simultaneously set the counters to a known value. You may think of this as the zero reset.

The use of both **Reset** and **Phase Lock** allow the establishment and maintenance of a fixed time reference between two or more chassis and the ports supported by the chassis.

In test setups where chassis and ports are physically close together, a sync cable is used to connect chassis in a `chassis chain' for synchronization operation.

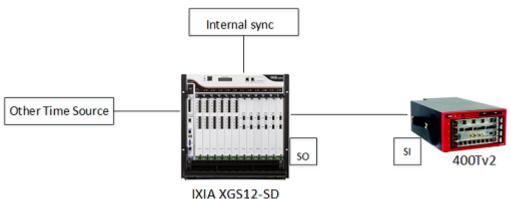
In widely distributed applications, such as monitoring traffic characteristics over a WAN, clock reference and/or reset signals cannot be transmitted between chassis over a physical connection because of unknown delay characteristics. An alternative means is required to satisfy these requirements.

Ixia has facilities that allow for the synchronization of independent Ixia chassis located anywhere in the world by replacing the existing inter-chassis sync cables with a widely available frequency and time standard supplied from an external source. This source provides a reference time used to obtain accurate latency and other measurements in a live global network. When geographically dispersed chassis are connected in this way, the combination is called a *virtual chassis chain*.

## **Physical Chaining**

Independent Ixia 400T, Optixia XM12, Optixia XM2, or Optixia X16 chassis may synchronize themselves with other chassis as shown in the following figure. The timing choices are explained in the following table.

Figure: Physical Chaining



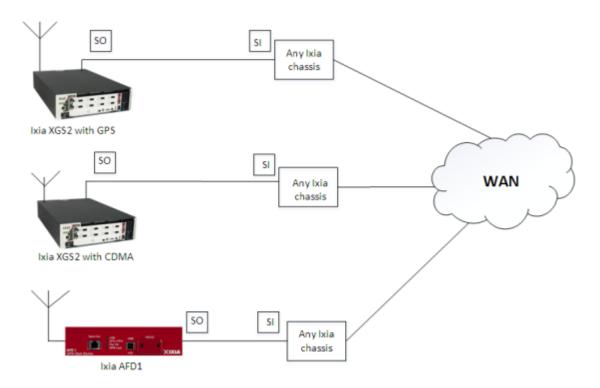
Physical Chaining Timing Choices

Choice	Usage
Internal Sync (Syn- chronous)	If a chassis is used in a standalone manner or the master of a chassis chain, it may generate its own start signal. In general, there is insufficient timing accuracy between timing masters for measurements over any distance. This is also known as the Synchronous Timing mode.
Sync-In (SI)	If a chassis is a subordinate, either directly connected to the master chassis or further down the chain, it derives its timing from the previous chassis' Sync-Out (SO) signal.

## **Virtual Chaining**

If two chassis are separated by any significant distance, a sync-out/sync-in cable cannot be used to connect them. In this case, an Ixia Auxiliary Function Device (AFD1) is used, one attached to each chassis through sync-out/sync-in cables, as shown in the following figure. The Ixia 100 maintains an accuracy of less than 150 nanoseconds when attached to a GPS antenna, or 100 microseconds when attached to a CDMA receiver, and provides chassis to chassis synchronization.

Figure: Virtual Chaining



To generate traffic for system latency testing, the Ixia 100 can be used alone or in conjunction with another Ixia chassis, or the Ixia AFD1 (GPS receiver) can be used with any other Ixia chassis. The timing features available with these chassis are shown in the following table. A GPS antenna requires external mounting. Refer to <a href="Appendix C, GPS">Appendix C, GPS</a> Antenna Installation Requirements for more information.

Virtual Chaining Timing Choices

Choice	Usage
GPS	The Ixia 100 or ixia AFD1 requires connection to an external antenna to `capture' multiple GPS satellites. It maintains an accuracy of less than 150 nano-seconds.
CDMA	The CDMA cellular network transmits an accurate time signal. CDMA (Code Division Multiple Access) cellular base-stations effectively act as GPS repeaters. The Ixia 100-CDMA receives the CDMA signals passively from an external antenna (you do not need to subscribe to any service) and decodes the embedded GMT time signal. Using this approach, the CDMA chassis can be time-synched to GMT. A CDMA antenna does not require external mounting.

The Sync-Out from a GPS or CDMA chassis is used to master a chassis chain at a specific geographic location. Since the Ixia 100 chassis has all other functions provided by the other Ixia chassis, it may also use independent timing when not used to synchronize with other chassis at other locations.

NOTE

CDMA reception depends on signal availability and may be impacted by cell location and chassis installation within the selected site. Consult your Ixia representative to determine the best solution for your installation.

For more information, including a formula for <u>Calculating Latency Accuracy for AFD1</u> (GPS), see Ixia GPS Auxiliary Function Device (AFD1).

#### **Ixia Chassis Connections**

A number of LEDs are available on the front panel of the Ixia 100, as described in the following table.

LED Usage Three LEDs indicate three separate status events: • 1: Indicates that the chassis is armed for a GPS sync event. Set Lock • 2: Indicates that the antenna is correctly connected. • 3: Indicates that the GPS is tracking satellites. Three LEDs indicate the Stratum connection level. The Stratum indicates the accuracy the time stamp. The following list explains the significance of the number of LEDs lit: Time Stamp • 0: Indicates Stratum 4, within 100 us of absolute GMT. • 1: Indicates Stratum 3, within 10 us of absolute GMT. • 2: Indicates Stratum 2, within 1 us of absolute GMT. • 3: Indicates Stratum 1, within 100 ns of absolute GMT. Shutdown The chassis is in the process of being shut down. Power Power is applied to the chassis.

IXIA 100 Front Panel LEDs

Similar information is available for the AFD1 GPS receiver in the Time Source tab of the Chassis Properties form (viewable through IxExplorer user interface).

#### **Load Modules**

Although each Ixia load module differs in particular capabilities, all modules share a common set of functions. Ixia load modules are generally categorized by network technology. The network technologies supported, along with names used to reference these technologies and more detailed information on load module differences, are available in the subsequent chapters of this manual.

NOTE

A load module can also be referred to as a *card*. The terms *load module* and *card* are used interchangeably in this manual.

The Load Module name prefix is used as the prefix to all load modules for that technology; for example, LM 100 in LM 100 TX. The IxExplorer name is used to label card and port types.

Some load modules are further labelled by the type of connector supported. Thus, a load module's name can be formed from a combination of its basic technology and the connector type. For example, LM 100 TX is the name of the 10/100 load module with RJ-45 connectors. An example for Packet Over SONET (POS) is the LMOC48c POS module, where no connector type is specified.

In addition, less expensive versions of several load modules are available. These are called Type-3 or Type-M modules, signified by an ending of `-3' or `-M' in the load module name and with a `-3'or `-M' suffix in the IxExplorer.

Newer boards also may have an `L' before the last number in their part number, signifying the same limited functionality.

Some load modules can be configured with less than standard amount of memory. Modules configured with such memory have a notation as to the memory upgrade following the module name. For example, LM622MR-512.

## **Port Hardware**

The ports on the Ixia load modules provide high-speed, transmit, capture, and statistics operation. The discussion which follows is broken down into a number of areas:

- <u>Types of Ports</u>: The different types of networking technology supported by Ixia load modules
- Port Transmit Capabilities: Facilities for generating data traffic
  - Streams and Flows: A set of packets, which may be grouped into bursts
  - Bursts and the Inter-Burst Gap (IBG): A number of packets
  - Packets and the Inter-Packet Gap (IPG): Individual frames/packets of data
- Frame Data: The construction of data within a frame/packet
- Port Data Capture Capabilities: Facilities for capturing data received on a port
- Port Statistics Capabilities: Facilities for obtaining statistics on each port

## **Types of Ports**

The types of load module ports that Ixia offers are divided into these broad categories:

- Ethernet
- Power over Ethernet
- 10GE
- 40GE and 100GE
- SONET/POS
- ATM
- BERT

Only the currently available Ixia load modules are discussed in this chapter. Subsequent chapters in this manual discuss all supported load modules and their optional features.

#### **Ethernet**

Ethernet modules are provided with various feature combinations, as mentioned in the following list:

- Speed combinations: 10 Mbps, 100 Mbps, and 1000 Mbps
- Auto negotiation
- Pause control
- With and without on-board processors, also called Port CPUs (PCPUs). Load modules without processors only allow for very limited routing protocol emulation
- Power over Ethernet (Described in Power over Ethernet)
- External connections including the following:
  - RJ-45
  - MII
  - RMII a custom Ixia connector
  - MT-RJ Fibre singlemode and multimode
  - SC multimode
  - GBIC singlemode and multimode

## **Power over Ethernet**

The Power over Ethernet (PoE) load modules (PLM1000T4-PD and LSM1000POE4-02) are special purpose, 4-channel electronic loads. They are intended to be used in conjunction with Ixia ethernet traffic generator/analyzer load modules to test devices that conform to IEEE std 802.3af.

A PoE load module provides the hardware interface required to test the Power Sourcing Equipment (PSE) of a 802.3af compliant device by simulating a Powered Device (PD).

#### Power Sourcing Equipment (PSE)

A PSE is any equipment that provides the power to a single link Ethernet Network section. The PSE's main functions are to search the link section for a powered device (PD), optionally classify the PD, supply power to the link section (only if a PD is detected), monitor the power on the link section, and remove power when it is no longer requested or required.

There are two power sourcing methods for PoE Alternative A and Alternative B.

PSEs may be placed in two locations with respect to the link segment, either coincident with the DTE/Repeater, or midspan. A PSE that is coincident with the DTE/Repeater is an `Endpoint PSE.' A PSE that is located within a link segment that is distinctly separate from and between the Media Dependent Interfaces (MDIs) is a `Midspan PSE.'

Endpoint PSEs may support either Alternative A, B, or both. Endpoint PSEs can be compatible with 10BASE-T, 100BASE-X, and/or 1000BASE-T.

Midspan PSEs must use Alternative B. Midspan PSEs are limited to operation with 10BASE-T and 100BASE-TX systems. Operation of Midspan PSEs on 1000BASE-T systems is beyond the scope of PoE.

## Powered Devices (PD)

A powered device either draws power or requests power by participating in the PD detection algorithm. A device that is capable of becoming a PD may or may not have the ability to draw power from an alternate power source and, if doing so, may or may not require power from the PSE.

One PoE Load Module emulates up to four PDs. The PoE Load Module (PLM) has eight RJ-45 interfaces four of them used as PD-emulated ports, with each having its own corresponding interface that connects to a port on any Ixia 10/100/1000 copper-based Ethernet load module (includes all copper-based TXS, and Optixia load modules).

The following figure demonstrates how the PoE modules use an Ethernet card to transmit and receive data streams.

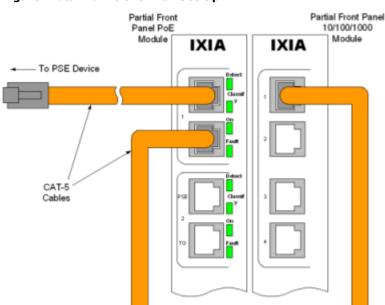


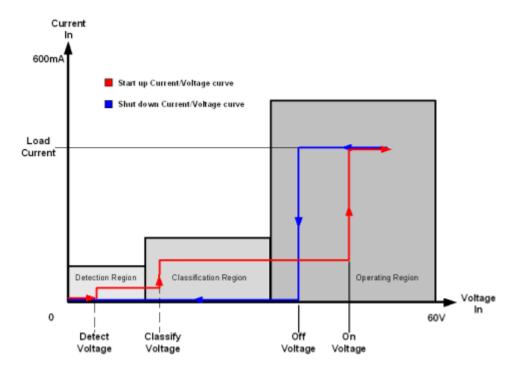
Figure: Data Traffic over PoE Set Up

The emulated PD device can 'piggy-back' a signal from a different load module along the cable connected to the PSE from which it draws power. In this manner, the emulated PD can mimic a device that generates traffic, such as an IP phone.

## **Discovery Process**

The main purpose for discovery is to prevent damage to existing Ethernet equipment. The Power Sourcing Equipment (PSE) examines the Ethernet cables by applying a small current-limited voltage to the cable and checking for the presence of a 25K ohm resistor in the remote Powered Device (PD). Only if the resistor is present, the full 48V is applied (and this is still current-limited to prevent damage to cables and equipment in fault conditions). The Powered Device must continue to draw a minimum current or the PSE removes the power and the discovery process begins again.

Figure: Discovery Process Voltage



There is also an optional extension to the discovery process where a PD may indicate to the PSE its maximum power requirements, called classification. Once there is power applied to the PD, normal transactions/data transfer occurs. During this period, the PD sends back a *maintain power signature* (MPS) to signal the PSE to continue to provide power.

## **PoE Acquisition Tests**

During the course of testing with the PoE module, it may be necessary to measure the amplitude of the incoming current. The PoE module has the ability to measure amplitude versus time in following two ways:

- Time test: The amount of time that elapses between a *Start* and *Stop* incoming current measurement.
- Amplitude test: The amplitude of the current after a set amount of time from a *Start* incoming current setting.

In both scenarios, a Start trigger is set, indicating when the test should commence based on an incoming current value (in either DC Volts or DC Amps).

In a Time test, a Stop trigger is also set (in either DC Volts or DC Amps) indicating when the test is over. Once the Stop trigger is reached, the amount of time between the Start and Stop trigger is measured (in microseconds) and the result is reported.

In an amplitude test, an Amplitude Delay time is set (in microseconds), which is the amount of time to wait after the Start trigger is reached before ending the test. The amplitude at the end of the Amplitude Delay time is measured and is reported.

Both Start and Stop triggers must also have a defined Slope type, either positive or negative. A positive slope is equivalent to rising current, while a negative slope is equivalent to decreasing current. A current condition must agree with both the amplitude setting and the Slope type to satisfy the trigger condition.

An example of a Time test is shown in the following figure.

Current In (DC Volts)

PoE Time Acquisition

Operating

Figure: PoE Time Acquisition Example

An example of an Amplitude test is shown in the following figure.

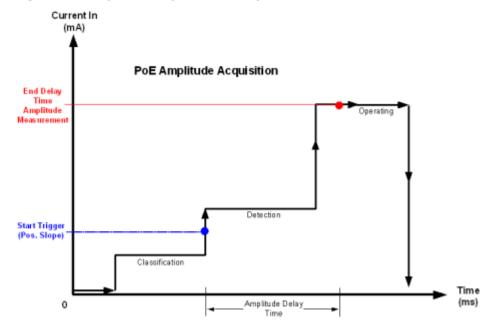


Figure: PoE Amplitude Acquisition Example

## **10GE**

The 10 Gigabit Ethernet (10GE) family of load modules implements five of the seven IEEE 8.2.3ae compliant interfaces that run at 10 Gbit/second. Several of the load modules may also be software switched to OC192 operation.

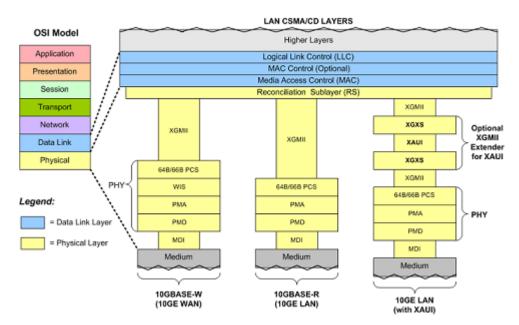
The 10 GE load modules are provided with various feature combinations, as mentioned in the following list:

- Interfaces types: LAN, WAN, XAUI, and XENPAK
- Interface connectors: SC singlemode (LAN and WAN), SC multimode (LAN), LC singlemode/multimode, XFP, XAUI, and XENPAK
- · Reach: Short, long, and extended
- Wavelengths: 850 nm, 1310 nm, 1550 nm

The relationship of the logical structures for the different 10 Gigabit types is shown in the diagram (adapted from the 802.3ae standard) in the following figure.

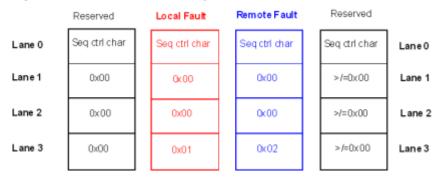
Figure: IEEE 802.3ae Draft 10 Gigabit Architecture

IEEE P802.3ae Model for 10GBASE-W, 10GBASE-R, & 10GE XAUI



For 10GE XAUI and 10GE XENPAK modules, a Status message contains a 4-byte ordered set with a Sequence control character plus three data characters (in hex), distributed across the four lanes, as shown in the following figure. Four Sequence ordered sets are defined in IEEE 802.3ae, but only two of these Local Fault and Remote Fault are currently in use; the other two are reserved for future use.

Figure: 10GE XAUI/XENPAK Sequence Ordered Sets



#### **XAUI Interfaces**

The 10 Gigabit XAUI interface has been defined in the IEEE draft specification P802.3ae by the 10 Gigabit Ethernet Task Force (10GEA). XAUI stands for `X' (the Roman Numeral for

10, as in `10 Gigabit'), plus `AUI' or Attachment Unit Interface originally defined for Ethernet.

The original Ethernet standard was defined in IEEE 802.3, and included MAC layer, frame size, and other `standard' Ethernet characteristics. IEEE 802.3z defined the Gigabit standard. IEEE 802.3ae has been created to create a simplified version of SONET framing to carry native Ethernet-framed traffic over high-speed fiber networks. This new standard allows a smooth transition from 10 Gbps native Ethernet traffic to work with 9.6 Gbps for SONET at OC-192c rate over WAN and MAN links. The 10GE XAUI has a XAUI interface for connecting to another XAUI interface, such as on a DUT. A comparison of the IEEE P802.3ae model for XAUI and the OSI model is shown in the following figure.

IEEE P802.3ae Model for 10GE XAUI LAN CSMA / CD LAYERS Higher Layers OSI Model Logical Link Control (LLC) Application MAC Control (Optional) Presentation Media Access Control (MAC) Session Reconciliation Sublayer (RS) 10 Gigabit Media Independent Interface Transport (XGMII) XGMII Extender Sublayer Network (DTE XGXS) Optional Data Link XGMII 10 Gigabit Attachment Unit Interface (XAUI) Extender for XAUI Physical XGMII Extender Sublayer (PHY XGXS) 10 Gigabit Media Independent Interface (XGMII) Physical Coding Sublayer64B/66B (PCS) Legend: Physical Medium Attachment PHY Sublayer (PMA) Data Link Layer Physical Medium Dependent Sublayer (PMD) = Physical Layer (PHY) Medium Dependent Interface (MDI) Medium

Figure: IEEE P802.3ae Architecture for 10GE XAUI

#### **Lane Skew**

The Lane Skew feature provides the ability to independently delay one or more of the four XAUI lanes. The resolution of the skew is 3.2 nanoseconds (ns), which consists of 10 Unit Intervals (UIs), each of which is 320 picoseconds (ps). Each UI is equivalent to the amount of time required to transmit one XAUI bit at 3.125 Gbps.

Lane Skew allows a XAUI lane to be skewed by as much as 310 UI (99.2ns) with respect to the other three lanes. To effectively use this feature, the four lanes should be set to different skew values. Setting all four lanes to zero is equivalent to setting all four lanes to +80 UI. In both cases, the lanes are synchronous and there is no lane skew. When lane skewing is enabled, /A/, /K/, and /R/ codes are inserted into the data stream BEFORE the

lanes are skewed. The principle behind lane skewing is shown in the diagrams in the following images.

Figure: XAUI Lane Skewing Lane Skew Disabled

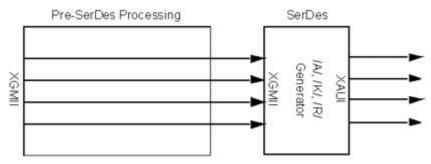
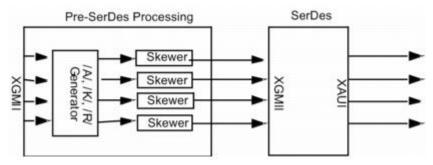


Figure: XAUI Lane Skewing Lane Skew Enabled



## **Link Fault Signaling**

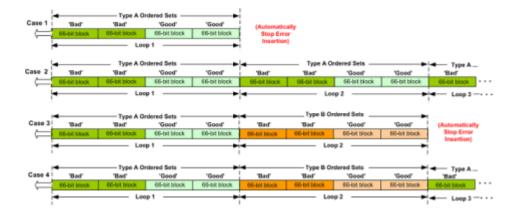
Link Fault Signaling is defined in Section 46 of the IEEE 802.3ae specification for 10 Gigabit Ethernet. When the feature is enabled, four statistics are added to the list in Statistic View for the port. One is for monitoring the Link Fault State; two for providing a count of the Local Faults and Remote Faults; and the last one is for indicating the state of error insertion, whether or not it is ongoing.

Link Fault Signaling originates with the PHY sending an indication of a local fault condition in the link being used as a path for MAC data. In the typical scenario, the Reconciliation Sublayer (RS) which had been receiving the data receives this Local Fault status, and then send a Remote Fault status to the RS which was sending the data. Upon receipt of this Remote Fault status message, the sending RS terminates transmission of MAC Data, sending only `Idle' control characters until the link fault is resolved.

For the 10GE LAN and LAN-M serial modules, the Physical Coding Sublayer (PCS) of the PHY handles the transition from 64 bits to 66 bit `Blocks.' The 64 bits of data are scrambled, and then a 2-bit synchronization (sync) header is attached before transmission. This process is reversed by the PHY at the receiving end.

Link Fault Signaling for the 10GE XAUI/XENPAK is handled differently across the four-lane XAUI optional XGMII extender layer, which uses 8B/10B encoding.

#### **Examples of Link Fault Signaling Error Insertion**



The examples in this figure are described in the following table:

Cases for Example

Case	Conditions
	Contiguous Bad Blocks = 2 (the minimum).
Case 1	Contiguous Good Blocks = 2 (the minimum).
	Send Type A ordered sets.
	Loop 1x.
	Contiguous Bad Blocks = 2 (the minimum).
Case 2	Contiguous Good Blocks = 2 (the minimum).
	Send Type A ordered sets.
	Loop continuously.
	Contiguous Bad Blocks = 2 (the minimum).
Case 3	Contiguous Good Blocks = 2 (the minimum).
	Send alternate ordered set types.
	Loop 1x.
	Contiguous Bad Blocks = 2 (the minimum).
Case 4	Contiguous Good Blocks = 2 (the minimum).
	Send alternate ordered set types.
	Loop continuously.

## Link Alarm Status Interrupt (LASI)

The link alarm status is an active low output from the XENPAK module that is used to indicate a possible link problem as seen by the transceiver. Control registers are provided so that LASI may be programmed to assert only for specific fault conditions.

Efficient use of XENPAK and its specific registers requires an end-user system to recognize a connected transceiver as being of the XENPAK type. An Organizationally Unique Identifier (OUI) is used as the means of identifying a port as XENPAK, and also to communicate the device in which the XENPAK specific registers are located.

Ixia's XENPAK module allows for setting whether or not LASI monitoring is enabled, what register configurations to use, and the OUI. The XENPAK module can use the following registers:

- Rx Alarm Control (Register 0x9003): It can be programmed to assert only when specific receive path fault condition(s) are present.
- Tx Alarm Control (Register 0x9001): It can be programmed to assert only when specific transmit path fault condition(s) are present.
- LASI Control (Register 0x9002): A LASI control register that allows global masking of the Rx Alarm and Tx Alarm.

You can control the registers by setting a series of sixteen bits for each register. The register bits and their usage are described in the following tables.

#### Rx Alarm Control

Bits	Description	Default
15 - 11	Reserved	0
10	Vendor Specific	N/A (vendor Setting)
9	WIS Local Fault Enable	1 (when imple- mented)
8 - 6	Vendor Specific	N/A (vendor Setting)
5	Receive Optical Power Fault Enable	1 (when imple- mented)
4	PMA/PMD Receiver Local Fault Enable	1 (when imple- mented)
3	PCS Receive Local Fault Enable	1
2 - 1	Vendor Specific	N/A (vendor Setting)
0	PHY XS Receive Local Fault Enable	1

Tx Alarm Control

Bits	Description	Default
15 - 11	Reserved	0
10	Vendor Specific	N/A (vendor setting)
9	Laser Bias Current Fault Enable	1 (when imple- mented)
8	Laser Temperature Fault Enable	1 (when imple- mented)

Bits	Description	Default
7	Laser Output Power Fault Enable	1 (when imple- mented)
6	Transmitter Fault Enable	1
5	Vendor Specific	N/A (vendor setting)
4	PMA/PMD Transmitter Local Fault Enable	1 (when imple- mented)
3	PCS Transmit Local Fault Enable	1
2 - 1	Vendor Specific	N/A (vendor setting)
0	PHY XS Transmit Local Fault Enable	1

LASI Control

Bits	Description	Default
15 - 8	Reserved	0
7 - 3	Vendor Specific	0 (when implemented)
2	Rx Alarm Enable	0
1	Tx Alarm Enable	0
0	LS Alarm Enable	0

For more detailed information on LASI, see the online document XENPAK MSA Rev. 3.

## **40GE and 100GE**

For theoretical information, refer to 40 Gigabit Ethernet and 100 Gigabit Ethernet Technology Overview White Paper, published by Ethernet Allliance, November, 2008. This white paper may be obtained through the Internet.

http://www.ethernetalliance.org/images/40G\_100G\_Tech\_overview.pdf

# **SONET/POS**

SONET/POS modules are provided with various feature combinations:

- Different speeds: OC3, OC12, OC48, OC192, Fibre Channel, 2x Fibre Channel, and Gigabit Ethernet.
- Interfaces: SC singlemode and multimode (OC3, OC12, OC192), SC singlemode (OC48), no optical transceiver, SFP LC singlemode (Unframed BERT) and custom interface.
- Reach: long, intermediate and long.
- Wavelengths: 850nm, 1310nm and 1550nm.

- Local processor support. All SONET/POS load modules include a local processor, but the power of the processor and amount of memory varies.
- Variable clocking OC48 only, see <u>Variable Rate Clocking</u>
- Concatenated or channelized SONET operation, see <u>SONET Operation</u>
- Error insertion, see Error Insertion
- BERT: Bit Error Rate Testing both framed and unframed, see <u>BERT</u>
- DCC: Data Communication Channel, see <a href="DCC Data Communications Channel">DCC Data Communications Channel</a>.
- RPR: Resilient Packet Ring, see RPR Resilient Packet Ring.
- GFP: Generic Framing Procedure, see GFP Generic Framing Procedure.
- PPP: Point to Point protocol, see PPP Protocol Negotiation.
- HDLC: High-Level Data Link Control, see HDLC.
- Frame Relay: see Frame Relay.
- DSCP: see DSCP Differentiated Services Code Point.

## **Variable Rate Clocking**

The OC48 VAR allows a variation of +/- 100 parts per million (ppm) from the clock source's nominal frequency, through a DC voltage input into the BNC jack marked `DC IN' on the front panel. The frequency may be monitored through the BNC marked `Freq Monitor.'

## **SONET Operation**

A Synchronous Optical NETwork/Synchronous Digital Hierarchy (SONET/SDH) frame is based on the Synchronous Transport Signal-1 (STS-1) frame, whose structure is shown in the figure below. Transmission of SONET Frames of this size correspond to the Optical Carrier level 1 (OC-1).

An OC-3c, consists of three OC-1/STS-1 frames multiplexed together at the octet level. OC-12c, OC-48c, and OC-192c, are formed from higher multiples of the basic OC-1 format. The suffix `c' indicates that the basic frames are concatenated to form the larger frame.

Ixia supports both concatenated (with the `c') and channelized (without the `c') interfaces. Concatenated interfaces send and receive data in a single streams of data. Channelized interfaces send and receive data in multiple independent streams.

Section & Line Overhead / Transport Synchronous Payload Envelope (SPE) -Overhead (TOH) Byte 2 Byte 3 Byte 1 Bytes 4-90 Payload Capacity Overhead Rows Line Overhead Path Byte 810 3 Bytes-87 Bytes 90 Bytes (for STS-1 Frame)

Figure: Generated Frame Contents SONET STS-1 Frame

SONET Frame Transmit time = 125 µsec

The contents of the SONET STS-1 frame are described in the following table.

SONET STS-1 Frame Contents

Section	Description
Section Over- head (SOH)	Consists of 9 bytes which include information relating to performance monitoring of the STS-n signal, and framing.
Line Over- head (LOH)	Consists of 18 bytes which include information relating to performance monitoring of the individual STS-1s, protection switching information, and line alarm indication signals.
Transport Overhead (TOH)	Consists of a combination of the Section Overhead and Line Overhead sections of the STS-1 frame.
Path Over- head (POH)	Part of the Synchronous Payload Envelope (SPE), contains information on the contents of the SPE, and handles quality monitoring.
Synchronous Payload Envel- ope (SPE)	Contains the payload information, the packets which are being transmitted, and includes the Path Overhead bytes.
Payload Capa-	Part of the SPE, and contains the packets being transmitted.

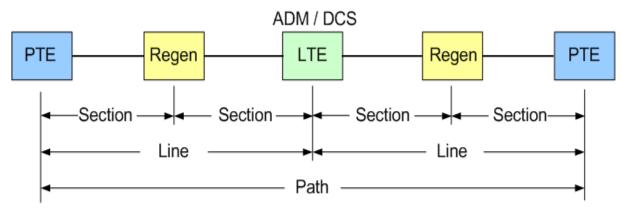
Section	Description
city	

The SONET STS-1 frame is transmitted at a rate of 51.84 Mbps, with 49.5 Mbps reserved for the frame payload. A SONET frame is transmitted in 125 microseconds, with the order of transmission of the starting with Row 1, Byte 1 at the upper left of the frame, and proceeding by row from top to bottom, and from left to right.

The section, line, and path overhead elements are related to the manner in which SONET frames are transmitted, as shown in the following figure.

#### **Example Diagram of SONET Levels and Network Elements**

# **SONET Levels**



#### Legend:

PTE = Path Terminating Entity, SONET Terminal or Switch

LTE = Line Terminating Entity, SONET Hub (ADM or DCS)

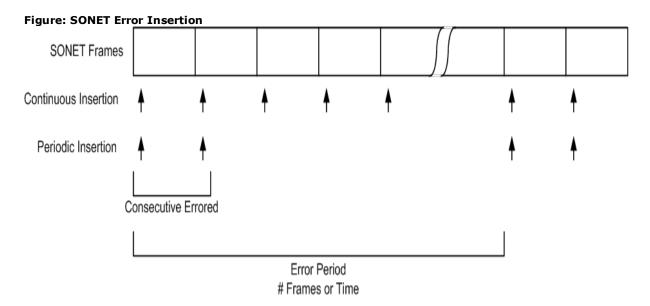
Regen = Regenerator

ADM = Add/Drop Multiplexer

DCS = Digital Cross-connect System

#### **Error Insertion**

A variety of deliberate errors may be inserted in SONET frames in the section, line or path areas of a frame. The errors which may be inserted vary by particular load module. Errors may be inserted continuously or periodically as shown in the following figure.



An error may be inserted in one of two manners:

- Continuous: Each SONET frame receives the error.
- Periodic: A number of errors are inserted in consecutive frames and the pattern is repeated based on a number of frames or a period of time. Predefined periods are available, or you may create your own predefined periods.

Each error may be individually inserted continuously or periodically. Errors may be inserted on a one time basis over a number of frames as well.

#### **DCC Data Communications Channel**

The data communication channel is a feature of SONET networks which uses the DCC bytes in the transport overhead of each frame. This is used for control, monitoring and provisioning of SONET connections. Ixia ports treat the DCC as a data stream which `piggybacks' on the normal SONET stream. The DCC and normal (referred to as the SPE - Synchronous Payload Envelope) streams can be transmitted independently or at the same time.

A number of different techniques are available for transmitting DCC and SPE data, utilizing Ixia streams and flows (see <u>Streams and Flows</u> and advanced stream scheduler (see <u>Advanced Streams</u>).

#### **SRP Spatial Reuse Protocol**

The Spatial Reuse Protocol (SRP) was developed by Cisco for use with ring-based media. It derives its name from the spatial reuse properties of the packet handling procedure. This optical transport technology combines the bandwidth-efficient and service-rich capabilities of IP routing with the bandwidth-rich, self-healing capabilities of fiber rings to deliver fundamental cost and functionality advantages over existing solutions. In SRP mode, the usual POS header (PPP, and so forth) is replaced by the SRP header.

SRP networks use two counter-rotating rings. One Ixia port may be used to participate in one of the rings; two may be used to simultaneously participate in both rings. Ixia supports SRP on both OC48 and OC192 interfaces.

In SRP-mode, SRP packets can be captured and analyzed. The IxExplorer capture view displays packet analysis which understands SRP packets. The Ixia hardware also collects specific SRP related statistics and performs filtering based on SRP header contents.

Any of the following SRP packet types may be generated in a data stream, along with normal IPv4 traffic:

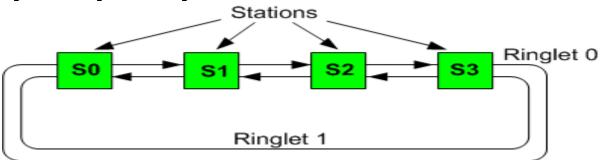
- SRP Discovery
- SRP ARP
- SRP IPS (Intelligent Protection Switching)

## **RPR Resilient Packet Ring**

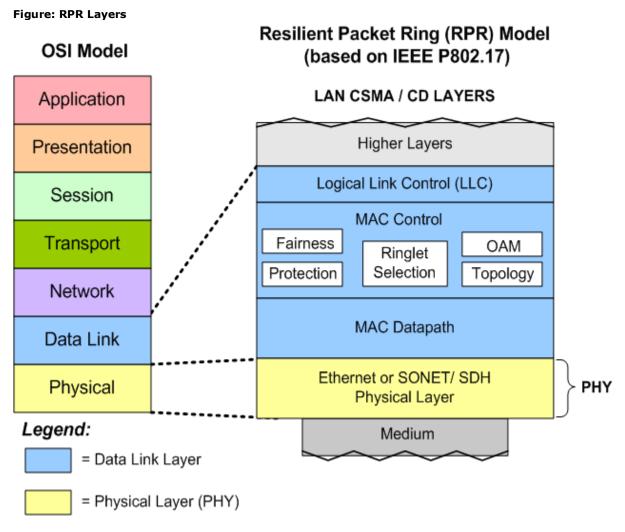
Ixia's optional Resilient Packet Ring (RPR) implementation is available on the OC-48c and OC-192c POS load modules. RPR is a proposed industry standard for MAC Control on Metropolitan Area Networks (MANs), defined by IEEE P802.17. This feature provides a cost-effective method to optimize the transport of bursty traffic, such as IP, over existing ring topologies.

A diagram showing a simplified model of an RPR network is shown in the following figure. It is made up of two, counter-rotating `ringlets,' with nodes called `stations' supporting MAC Clients that exchange data and control information with remote peers on the ring. Up to 255 nodes can be supported on the ring structure.

Figure: RPR Ring Network Diagram



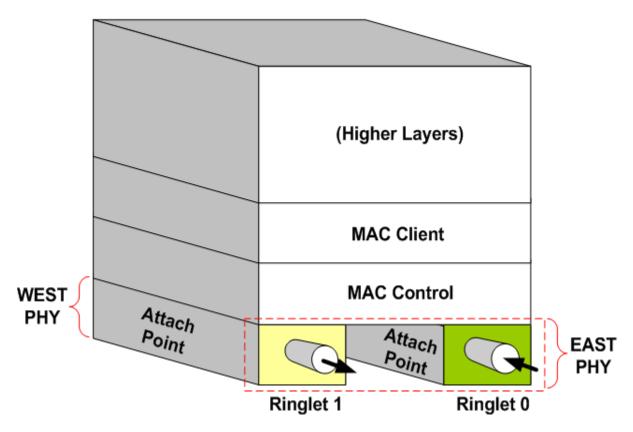
The RPR topology discovery is handled by a MAC sublayer, and a protection function maintains network connectivity in the event of a station or span failure. The structure of the RPR layers, compared to the OSI model, is illustrated in a diagram based on IEEE 802.17, shown in the following figure.



A diagram of the layers associated with an RPR Station is shown in the following figure.

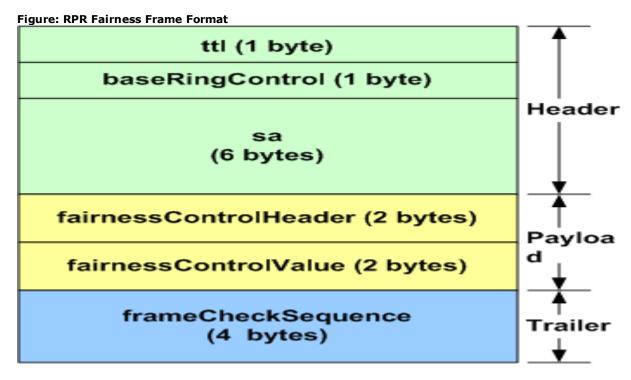
Figure: RPR Layer Diagram

## **RPR Station**



The Ixia implementation allows for the configuration and transmission of the following types of RPR frames:

• RPR Fairness Frames: The RPR Fairness Algorithm (FA) is used to manage congestion on the ringlets in an RPR network. Fairness frames are sent periodically to advertise bandwidth usage parameters to other nodes in the network to maintain weighted fair share distributions of bandwidth. The messages are sent in the direction opposite to the data flow, and therefore, on the other ringlet. A diagram of the RPR Fairness Frame, per IEEE 802.17/D2.1, is shown in the following figure.



A diagram of the baseRingControl byte, part of the Ring Control header for all types of RPR frames, is shown in the following figure.

#### Figure: RPR baseRingControl Byte

#### baseRingControl Field MSB LSB **Bits** 7 3:2 6 5:4 1 0 RI FE FT SC WE Р

- RPR Topology Discovery. Two types of messages are used:
  - RPR Topology Discovery Message: for the discovery of the physical topology.
  - RPR Topology Extended Status Message: for the transmission of additional information from a node concerning bandwidth and other configuration options. This format uses TLV (Type-Length-Value) options, including:
    - Weight
    - Total reserved bandwidth
    - Neighbor address
    - Individual reserved bandwidth
    - Station name
    - Vendor specific data
- RPR Protection Switching Message: used to support automatic, rapid switching of traffic in the presence of a ring failure.
- RPR Operations, Administration and Management (OAM). Three messages are supported:

- Echo Request and Response messages
- Flush Frames
- Vendor specific message

## **GFP Generic Framing Procedure**

GFP provides a generic mechanism to adapt traffic from higher-layer client signals over a transport network. Currently, two modes of client signal adaptation are defined for GFP.

- A PDU-oriented adaptation mode, referred to as Frame-Mapped GFP (GFP-F, for traffic such as IP/PPP or Ethernet MAC).
- A block-code oriented adaptation mode, referred to as Transparent GFP (GFP-T, for traffic such as Fibre Channel or ESCON/SBCON).

In the Frame-Mapped adaptation mode, the Client/GFP adaptation function operates at the data link (or higher) layer of the client signal. Client PDU visibility is required, which is obtained when the client PDUs are received from either the data layer network or a bridge, switch, or router function in a transport network element.

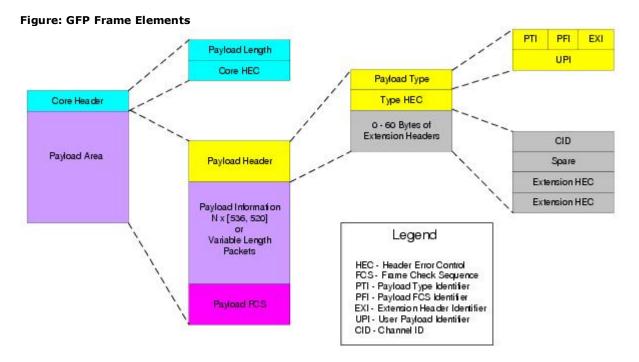
For the Transparent adaptation mode, the Client/GFP adaptation function operates on the coded character stream, rather than on the incoming client PDUs. Processing of the incoming code word space for the client signal is required.

Two kinds of GFP frames are defined: GFP client frames and GFP control frames. GFP also supports a flexible (payload) header extension mechanism to facilitate the adaptation of GFP for use with diverse transport mechanisms.

GFP uses a modified version of the Header Error Check (HEC) algorithm to provide GFP frame delineation. The frame delineation algorithm used in GFP differs from HEC in two basic ways:

- The algorithm uses the PDU Length Indicator field of the GFP Core Header to find the end of the GFP frame.
- HEC field calculation uses a 16-bit polynomial and, consequently, generates a twooctet cHEC field.

A diagram of the format for a GFP frame is shown in the following figure.



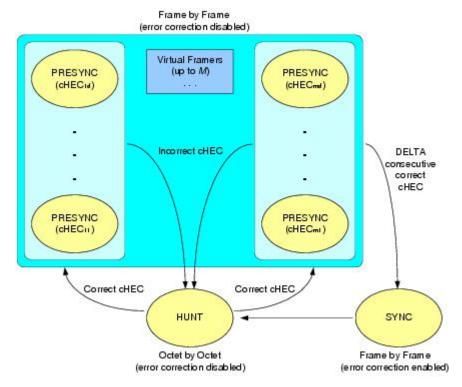
The sections of the GFP frame are described in the following list:

- Payload Length Indicator (PLI): The two-octet PLI field contains a binary number representing the number of octets in the GFP Payload Area. The absolute minimum value of the PLI field in a GFP client frame is 4 octets. PLI values 0-3 are reserved for GFP control frame usage.
- Core Header Error Control (cHEC): The two-octet Core Header Error Control field contains a CRC-16 error control code that protects the integrity of the contents of the Core Header by enabling both single-bit error correction and multi-bit error detection.
- Type Header Error Control (tHEC): The two-octet Type Header Error Control field contains a CRC-16 error control code that protects the integrity of the contents of the Type field by enabling both single-bit error correction and multi-bit error detection.
- Extension Header Error Control (eHEC): The two-octet Extension Header Error Control field contains a CRC-16 error control code that protects the integrity of the contents of the extension headers by enabling both single-bit error correction (optional) and multi-bit error detection.
- Connection Identification (CID): The CID is an 8-bit binary number used to indicate one of 256 communications channels at a GFP termination point.
- Payload: The GFP Payload Area, which consists of all octets in the GFP frame after the GFP Core Header, is used to convey higher layer specific protocol information. This variable length area may include from 4 to 65,535 octets. The GFP Payload Area consists of two common components:
  - A Payload Header and a Payload Information field
  - An optional Payload FCS (pFCS) field
     Practical GFP MTU sizes for the GFP Payload Area are application specific.
- Frame Check Sequence (FCS): The GFP Payload FCS is an optional, four-octet long, frame check sequence. It contains a CRC-32 sequence that protects the contents of

the GFP Payload Information field. A value of 1 in the PFI bit within the Type field identifies the presence of the payload FCS field.

GFP frame delineation is performed based on the correlation between the first two octets of the GFP frame and the embedded two-octet cHEC field. The following figure shows the state diagram for the GFP frame delineation method.

**Figure: GFP State Transitions** 



The state diagram works as follows:

- In the HUNT state, the GFP process performs frame delineation by searching octets for a correctly formatted Core Header over the last received sequence of four octets. Once a correct cHEC match is detected in the candidate Payload Length Indicator (PLI) and cHEC fields, a candidate GFP frame is identified and the receive process enters the PRESYNC state.
- 2. In the PRESYNC state, the GFP process performs frame delineation by checking frames for a correct cHEC match in the presumed Core Header of the next candidate GFP frame. The PLI field in the Core Header of the preceding GFP frame is used to find the beginning of the next candidate GFP frame. The process repeats until a set number of consecutive correct cHECs are confirmed, at which point the process enters the SYNC state. If an incorrect cHEC is detected, the process returns to the HUNT state.
- 3. In the SYNC state, the GFP process performs frame delineation by checking for a correct cHEC match on the next candidate GFP frame. The PLI field in the Core Header of the preceding GFP frame is used to find the beginning of the next candidate GFP frame. Frame delineation is lost whenever multiple bit errors are detected in the Core Header by the cHEC. In this case, a GFP Loss of Frame Delineation event is declared, the framing process returns to the HUNT state, and a client Server Signal

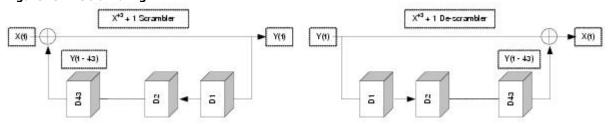
Failure (SSF) is indicated to the client adaptation process.

4. Idle GFP frames participate in the delineation process and are then discarded.

Robustness against false delineation in the resynchronization process depends on the value of DELTA. A value of DELTA = 1 is suggested. Frame delineation acquisition speed can be improved by the implementation of multiple `virtual framers,' whereby the GFP process remains in the HUNT state and a separate PRESYNC substate is spawned for each candidate GFP frame detected in the incoming octet stream.

Scrambling of the GFP Payload Area is required to provide security against payload information replicating scrambling word (or its inverse) from a frame synchronous scrambler (such as those used in the SDH RS layer or in an OTN OPUk channel). The following figure illustrates the scrambler and descrambler processes.

Figure: GFP Scrambling



All octets in the GFP Payload Area are scrambled using a  $x^{43} + 1$  self-synchronous scrambler. Scrambling is done in network bit order.

At the source adaptation process, scrambling is enabled starting at the first transmitted octet after the cHEC field, and is disabled after the last transmitted octet of the GFP frame. When the scrambler or descrambler is disabled, its state is retained. Hence, the scrambler or descrambler state at the beginning of a GFP frame Payload Area is, thus, the last 43 Payload Area bits of the GFP frame transmitted in that channel immediately before the current GFP frame.

The activation of the sink adaptation process descrambler also depends on the present state of the cHEC check algorithm:

- In the HUNT and PRESYNC states, the descrambler is disabled.
- In the SYNC state, the descrambler is enabled only for the octets between the cHEC field and the end of the candidate GFP frame.

#### **CDL Converged Data Link**

10GE LAN, 10GE XAUI, 10GE XENPAK, 10GE WAN, and 10GE WAN UNIPHY modules all support the Cisco CDL preamble format.

The Converged Data Link (CDL) specification was developed to provide a standard method of implementing operation, administration, maintenance, and provisioning (OAM&P) in Ethernet packet-based optical networks without using a SONET/SDH layer.

#### **PPP Protocol Negotiation**

The Point-to-Point Protocol (PPP) is widely used to establish, configure and monitor peer-to-peer communication links. A PPP session is established in a number of steps, with each step completing before the next one starts. The steps, or layers, are:

- 1. Physical: a physical layer link is established.
- 2. Link Control Protocol (LCP): establishes the basic communications parameters for the line, including the Maximum Receive Unit (MRU), type of authentication to be used and type of compression to be used.
- 3. Link quality determination and authentication. These are optional processes. Quality determination is the responsibility of PPP Link Quality Monitoring (LQM) Protocol. Once initiated, this process may continue throughout the life of the link. Authentication is performed at this stage only. There are multiple protocols which may be employed in this process; the most common of these are PAP and CHAP.
- 4. Network Control Protocol (NCP): establishes which network protocols (such as IP, OSI, MPLS) are to be carried over the link and the parameters associated with the protocols. The protocols which support this NCP negotiation are called IPCP, OSINLCP, and MPLSCP, respectively.
- 5. Network traffic and sustaining PPP control. The link has been established and traffic corresponding to previously negotiated network protocols may now flow. Also, PPP control traffic may continue to flow, as may be required by LQM, PPP keepalive operations, and so forth.

All implementations of PPP must support the Link Control Protocol (LCP), which negotiates the fundamental characteristics of the data link and constitutes the first exchange of information over an opening link. Physical link characteristics (media type, transfer rate, and so forth) are not controlled by PPP.

The Ixia PPP implementation supports LCP, IPCP, MPLSCP, and OSINLCP. When PPP is enabled on a given port, LCP and at least one of the NCPs must complete successfully over that port before it is administratively `up' and therefore be ready for general traffic to flow.

Each Ixia POS port implements a subset of the LCP, LQM, and NCP protocols. Each of the protocols is of the same basic format. For any connection, separate negotiations are performed for each direction. Each party sends a *Configure-Request* message to the other, with options and parameters proposing some form of configuration. The receiving party may respond with one of three messages:

- *Configure-Reject*: The receiving party does not recognize or prohibits one or more of the suggested options. It returns the problematic options to the sender.
- Configure-NAK: The receiving party understands all of the options, but finds one or more of the associated parameters unacceptable. It returns the problematic options, with alternative parameters, to the sender.
- Configure-ACK: The receiving party finds the options and parameters acceptable.

For the *Configure-Reject* and *Configure-NAK* requests, the sending party is expected to reply with an alternative *Configure-Request*.

The Ixia port may be configured to immediately start negotiating after the physical link comes up, or passively wait for the peer to start the negotiation. Ixia ports both sends and responds to PPP keepalive messages called echo requests.

## **LCP Link Control Protocol Options**

The following sections outline the parameters associated with the Link Control Protocol. LCP includes a number of possible command types, which are assigned option numbers in

the pertinent RFCs. Note that PPP parameters are typically independently negotiated for each direction on the link.

Numerous RFCs are associated with LCP, but the most important RFCs are RFC 1661 and RFC 1662. The HDLC/PPP header sequence for LCP is FF 03 C0 21.

During the LCP phase of negotiation, the Ixia port makes available the following options:

• Maximum Receive Unit: This LCP parameter (actually the set of Maximum Receive Unit (MRU) and Maximum Transmit Unit (MTU)) determines the maximum allowed size of any frame sent across the link subsequent to LCP completion. To be fully standards-compliant, an implementation must not send a frame of length greater than its MTU + 4 bytes + CRC length. For instance, if the negotiated MTU for a port is 2000 and 32 bit CRC is in use, no frame larger than 2008 bytes should ever be sent out that port. Packets that are larger are expected to be fragmented before transmitting or to be dropped. The Ixia port's MTU is the peer's MRU following LCP negotiation. Strictly speaking, the receiving side can assume that frames received is not greater than the MRU. In practice, however, an implementation should be capable of accepting larger frames. If a peer rejects this option altogether, the negotiated setting defaults to 1,500. Regardless of the negotiated MRU, all implementations must be capable of accepting frames with an information field of at least 1,500 bytes.

For the transmit direction portion of the negotiation, the peer sends the Ixia port its configuration request. The Ixia port accepts and acknowledges the peer's requested MRU as long as it is less than or equal to the specified user's desired transmit value (but greater than 26). For the receive direction portion of the negotiation, the Ixia port sends a configuration request based on the user's desired value. Generally, the Ixia port accepts what the peer desires (if it acknowledges the request, then the user value is used, or if the peer sends a *Configure-Nak* with another value the Ixia port uses that value as long as it is valid). This approach is used to maximize the probability of successful negotiation.

• Asynchronous Control Character Map: ACCM is only really pertinent to asynchronous links. On asynchronous lines, certain characters sent over the wire can have special meaning to one or more receiving entities. For instance, common implementations of the widely used XON/XOFF flow control protocol assign the ASCII DC3 character (0x13) to XOFF. On such a link, an embedded data byte that happens to have the value 0x13 would be misinterpreted by a receiver as an XOFF command, and cause suspension of reception. To avoid this problem, the 0x13 character embedded in the data could be sent through an `escape sequence' which consists of preceding the data character with a dedicated tag character and modifying the data character itself.

The Asynchronous Control Character Map (ACCM) LCP parameter allows independent designation of each character in the range 0x00 thru 0x1F as a control character. A control character is sent/received with a preceding `control-escape' character (0x7D). When the 0x7D is seen in the received data stream, the 0x7D is dropped and the next character is exclusive-or'd with 0x20 to get the original transmitted character. ACCM negotiation consists of exchanging masks between peers to reach an agreement as to which characters are treated as special control characters on transmission and reception. For example, sending a mask of 0xFFFFFFFF means all characters in the range 0x00 thru 0x1F are sent with escape sequences; a mask of 0 means no special handling, so all characters are arbitrary data.

Packet over SONET is an octet-synchronous medium. If the link is direct between POS peers, neither side should be generating control-escapes. (Exceptions to this are bytes 0x7D and 0x7E: the former is the special control escape character itself; the latter is the start/end frame marker. Escaping of these two characters is generally handled directly by physical layer hardware). On links in which there is some kind of intermediate asynchronous media, it is required that whatever device performs the asynchronous to synchronous conversion must also take care of any special character handling, isolating this from any POS port. See RFC 1662, sections 4.1 and 6.

If ACCM negotiation is enabled, the Ixia port advertises an ACCM mask of 0 to its peer in its LCP configuration request. The Ixia port accept whatever the peer puts forth, but does not act on the results. Regardless of the final negotiated settings for receive and transmit ACCM, the Ixia port does not send escape control sequences nor does it expect to receive them. This is the nature of a synchronous PPP medium, such as POS.

Magic Number: A magic number is a 32-bit value, ideally numerically random, which
is placed in certain PPP control packets. Magic numbers aid in detection of looped
links. If a received PPP packet that includes a magic number matches a previously
transmitted packet, including magic number, the link is probably looped.

IXExplorer and the Tcl APIs allow global enable/disable of magic number negotiation. If the `Use Magic Number' feature is enabled, the Ixia port does not request
magic number of its peer and rejects the option if the peer requests it. If the check

tiation. If the `Use Magic Number' feature is enabled, the Ixia port does not request magic number of its peer and rejects the option if the peer requests it. If the check box is selected, the port attempts to negotiate magic number. The result of the bi-directional negotiation process is displayed in the fields for transmit and receive: an indication of whether magic number is enabled is written in the field for the corresponding direction.

#### **NCP Network Control Protocols**

• IPCP: Internet Protocol Control Protocol Options for IPV4. IPCP includes three command types, which are assigned option numbers in the pertinent RFCs. Note that PPP parameters are typically independently negotiated for each direction on the link. The sender of this Configure-Request may either include its own IP address, to provide this information to its remote peer, or may send all 0.0.0.0 as an IP address, which requests that the remote peer assign an IP address for the local node. The receiver may refuse the requested IP address and attempt to specify one for the peer to use by using a Configure-NAK response to the request with a specification of a different address.

The Ixia implementation provides minimal configuration of this parameter. You must specify the local IP address of the unit and the peer must provide its own IP address. The Ixia port accepts any IP address the peer wishes to use as long as it is a valid address (for example, not all 0's). The Ixia port expects the peer to accept its address. If, however, the peer specifies a different address for use, the port acknowledges that address but not actually notify you that this has happened. The Ixia port accepts a situation in which local and peer addresses are the same following negotiation.

- IPv6CP: Internet Protocol Control Protocol Options for IPv6. IPv6CP includes three command types, which are assigned option numbers in the pertinent RFCs. Note that PPP parameters are typically independently negotiated for each direction on the link. A PPP peer may determine its IPv6 interface address by one or three methods:
  - Generate its own address.
  - Suggest its own address to its peer, but allow the peer to override that value.
  - Require that the peer designate an address.

In any of these cases, the *Configure-Request* must contain a tentative interface-identifier to send to the peer that is both unique to the link and if possible consistently reproducible.

The Ixia PPP implementation of IPv6CP is such that the negotiation mode of the local endpoint may be configured in one of three modes:

- Local may: the local peer may suggest an Interface Identifier (IID), but most allow a *Configure-NAK* with an alternate address to override its setting.
- Local must: the local peer must set the IID, which the peer must accept.
- Peer must: the peer must supply the IID. This is accomplished by sending an all zero tentative IID.

The peer endpoint may be configured in one of three modes:

- Peer may: the remote peer may suggest an IID, but most allow a Configure-NAK with an alternate address to override its setting.
- Peer must: the remote peer must set the IID, which the local peer accepts.
- Local must: the local peer must supply the IID.

One IID can be sent in each Configuration-Request. A zero value may be sent, in which case, the peer may send an IID in its response. Either node on the link can provide the valid, non-zero IID values for itself and its peer.

The tentative, or assigned IID in the *Peer - Local Must* case, may be assigned from one of four sources:

- Last Negotiated: the last negotiated interface-identifier.
- MAC Based: an address derived from the port's MAC address.
- IPv6: an IPv6 format address.
- Random: a randomly generated value.

See IPv6 Interface Identifiers as follows for more information.

- OSI Network Layer Control Protocol (OSINLCP): A single option is provided for this NCP protocol. If a non-zero value for alignment has been negotiated, subsequent ISO traffic (for example, IS-IS) arrives with or be sent with 1 to 3 zero pads inserted after the protocol header as per RFC 1377.
- MPLS Network Control Protocol (MPLSCP): No options are currently available for this
  protocol setup.

## IPv6 Interface Identifiers (IIDs)

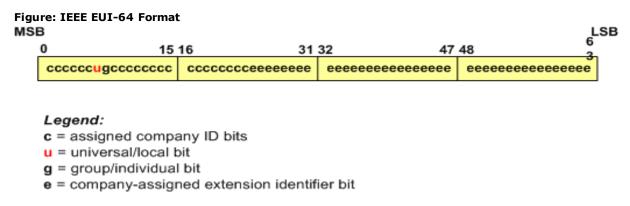
IIDs comprise part of an IPv6 address, as shown in the following figure for a link-local IPv6 address.

The IPv6 Interface Identifier is equivalent to EUI-64 Id in the Protocol Interfaces window.

Figure: IPv6 Address Format Link-Local Address
10 bits 54 bits 64 bits

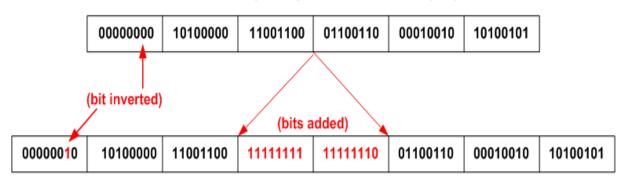
1111111010 0 Interface ID

The IPv6 Interface Identifier is derived from the 48-bit IEEE 802 MAC address or the 64-bit IEEE EUI-64 identifier. The EUI-64 is the extended unique identifier formed from the 24-bit company ID assigned by the IEEE Registration Authority, plus a 40-bit company-assigned extension identifier, as shown in the following figure.



To create the Modified EUI-64 Interface Identifier, the value of the universal/local bit is inverted from `0' (which indicates global scope in the company ID) to `1' (which indicates global scope in the IPv6 Identifier). For Ethernet, the 48-bit MAC address may be encapsulated to form the IPv6 Identifier. In this case, two bytes `FF FE' are inserted between the company ID and the vendor-supplied ID, and the universal/local bit is set to `1' to indicate global scope. An example of an Interface Identifier based on a MAC address is shown in the following figure.

# Example Encapsulated MAC in IPv6 Interface Identifier MAC Address (48 bits) = 00 A0 CC 66 12 A5 (hex)



Interface Identifier (64 bits) = 02 A0 CC FF FE 66 12 A5 (hex)

#### **Retry Parameters**

During the process of negotiation, the port uses three Retry parameters. RFC 1661 specifies the interpretation for all of the parameters.

#### **HDLC**

Both standard and Cisco proprietary forms of HDLC (High-level Data Link Control) are supported.

# **Frame Relay**

Packets may be wrapped in frame relay headers. The DLCI (Data Link Connection Identifier) may be set to a fixed value or varied algorithmically.

#### **DSCP Differentiated Services Code Point**

Differentiated Services (DiffServ) is a model in which traffic is treated by intermediate systems with relative priorities based on the type of services (ToS) field. Defined in RFC 2474 and RFC 2475, the DiffServ standard supersedes the original specification for defining packet priority described in RFC 791. DiffServ increases the number of definable priority levels by reallocating bits of an IP packet for priority marking.

The DiffServ architecture defines the DiffServ (DS) field, which supersedes the ToS field in IPv4 to make Per-Hop Behavior (PHB) decisions about packet classification and traffic conditioning functions, such as metering, marking, shaping, and policing.

Based on DSCP or IP precedence, traffic can be put into a particular service class. Packets within a service class are treated the same way.

The six most significant bits of the DiffServ field are called the Differential Services Code Point (DSCP).

The DiffServ fields in the packet are organized as shown in the following figure. These fields replace the TOS fields in the IP packet header.

Figure: DiffServ Fields

 .94.0. 2								
DS5	DS4	DS3	DS2	DS1	DS0	ECN	ECN	

The DiffServ standard utilizes the same precedence bits (the most significant bits are DS5, DS4, and DS3) as TOS for priority setting, but further clarifies the definitions, offering finer granularity through the use of the next three bits in the DSCP. DiffServ reorganizes and renames the precedence levels (still defined by the three most significant bits of the DSCP) into these categories (the levels are explained in greater detail in this document). The following table shows the eight categories.

**DSCP** Categories

Precedence Level	Description
7	Stays the same (link layer and routing protocol keep alive)
6	Stays the same (used for IP routing protocols)
5	Express Forwarding (EF)
4	Class 4
3	Class 3
2	Class 2

Precedence Level	Description
1	Class 1
0	Best Effort

With this system, a device prioritizes traffic by class first. Then it differentiates and prioritizes same-class traffic, taking the drop probability into account.

The DiffServ standard does not specify a precise definition of `low,' `medium,' and `high' drop probability. Not all devices recognize the DiffServ (DS2 and DS1) settings; and even when these settings are recognized, they do not necessarily trigger the same PHB forwarding action at each network node. Each node implements its own response based on how it is configured.

Assured Forwarding (AF) PHB group is a means for a provider DS domain to offer different levels of forwarding assurances for IP packets received from a customer DS domain. Four AF classes are defined, where each AF class is in each DS node allocated a certain amount of forwarding resources (buffer space and bandwidth).

Classes 1 to 4 are referred to as AF classes. The following table illustrates the DSCP coding for specifying the AF class with the probability. Bits DS5, DS4, and DS3 define the class, while bits DS2 and DS1 specify the drop probability. Bit DS0 is always zero.

Drop Precedence for Classes

Drop	Class 1	Class 2	Class 3	Class 4
	001010	010010	011010	100010
Low	AF11	AF21	AF31	AF41
	DSCP 10	DSCP 18	DSCP 26	DSCP 34
	001100	010100	011100	100100
Medium	AF12	AF 22	AF32	AF42
	DSCP 12	DSCP 20	DSCP 28	DSCP 36
	001110	010110	011110	100110
High	AF13	AF23	AF33	AF43
	DSCP 14	DSCP 22	DSCP 30	DSCP 38

#### **MTA**

The ATM load module enables high performance testing of routers and broadband aggregation devices such as DSLAMs and PPPoE termination systems.

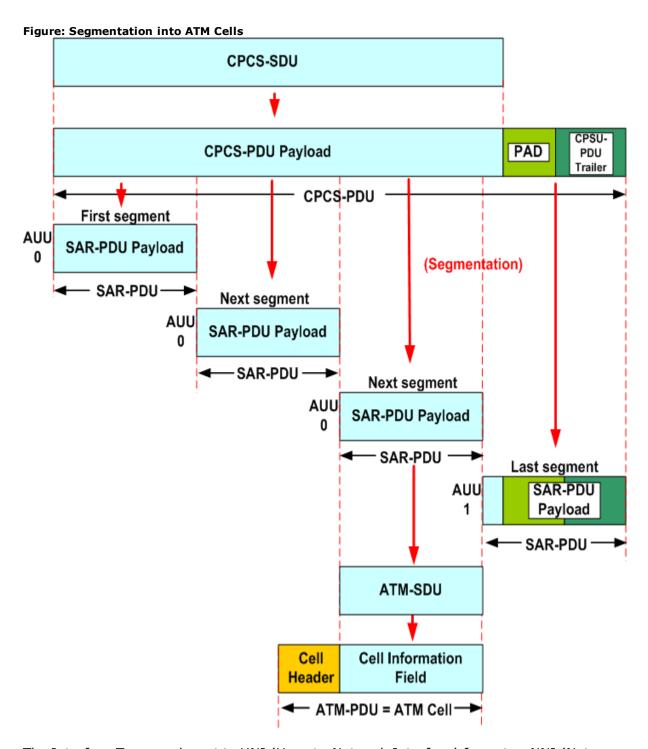
The ATM module is provided with various feature combinations:

- Interfaces: pluggable PHYs:
  - 1310nm multimode optics with dual -SC connectors
  - SFP socket
- Speeds: OC3 and OC12

- Encapsulations:
  - LLC/SNAP
  - LLC/NLPID
  - LLC Bridged Ethernet
  - LLC Bridged Ethernet without FCS
  - VC Mux Routed
  - VC Mux Bridged Ethernet
  - VC Mux Bridged Ethernet without FCS
- · Multiple independent data streams

ATM is a point-to-point, connection-oriented protocol that carries traffic over `virtual connections/circuits' (VCs), in contrast to Ethernet connectionless LAN traffic. ATM traffic is segmented into 53-byte cells (with a 48-byte payload), and allows traffic from different Virtual Circuits to be interleaved (multiplexed). Ixia's ATM module allows up to 4096 transmit streams per port, shared across up to 15 interleaved VCs.

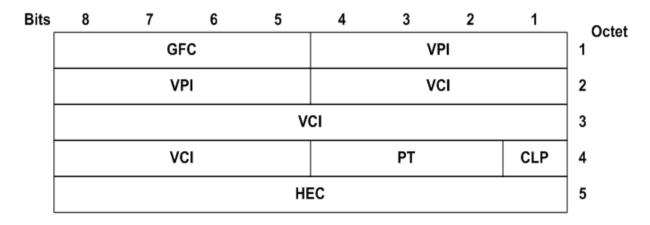
To allow the use of a larger, more convenient payload size, such as that for Ethernet frames, ATM Adaptation Layer 5 (AAL5) was developed. It is defined in ITU-T Recommendation I.363.5, and applies to the Broadband Integrated Services Digital Network (B-ISDN). It maps the ATM layer to higher layers. The Common Part Convergence Sublayer-Service Data Unit (CPSU-SDU) described in this document can be considered an IP or Ethernet packet. The entire CPSU-PDU (CPCS-SDU plus PAD and trailer) is segmented into sections which are sent as the payload of ATM cells, as shown in the following figure, based on ITU-T I.363.5.



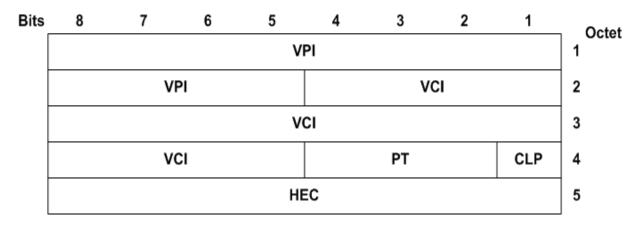
The Interface Type can be set to UNI (User-to-Network Interface) format or NNI (Network-to-Node Interface aka Network-to-Network Interface) format. The 5-byte ATM cell header is different for each of the two interfaces, as shown in the following figure.

Figure: ATM Cell Header for UNI and NNI

# **UNI Header Structure**



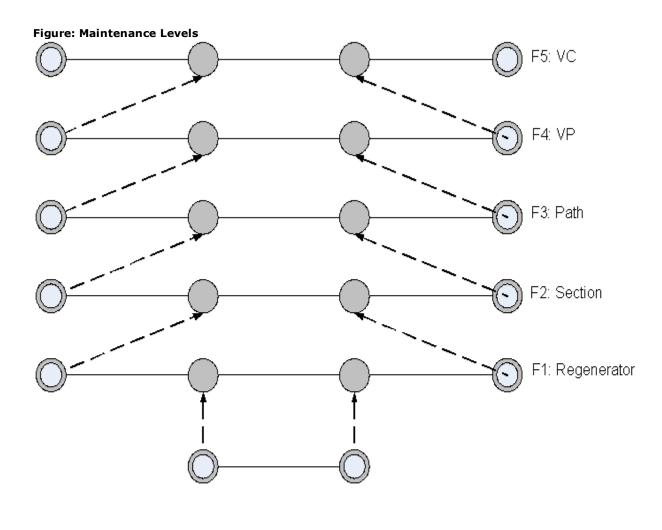
# **NNI Header Structure**



#### **ATM OAM Cells**

OAM cells are used for operation, administration, and maintenance of ATM networks. They operate on ATM's physical layer and are not recognized by higher layers. Operation, Administration, and Maintenance (OAM) performs standard loopback (end-to-end or segment) and fault detection and notification Alarm Indication Signal (AIS) and Remote Defect Identification (RDI) for each connection. It also maintains a group of timers for the OAM functions. When there is an OAM state change such as loopback failure, OAM software notifies the connection management software.

The ITU-T considers an ATM network to consist of five flow levels. These levels are illustrated in the following figure.



Connecting Point of the Corresponding Level

End Point of the Corresponding Level

The lower three flow levels are specific to the nature of the physical connection. The ITU-T recommendation briefly describes the relationship between the physical layer OAM capabilities and the ATM layer OAM.

From an ATM viewpoint, the most important flows are known as the F4 and F5 flows. The F4 flow is at the virtual path (VP) level. The F5 flow is at the virtual channel (VC) level. When OAM is enabled on an F4 or F5 flow, special OAM cells are inserted into the user traffic.

Four types of OAM cells are defined to support the management of VP/VC connections:

- Fault Management OAM cells. These OAM cells are used to indicate failure conditions. They can be used to indicate a discontinuity in VP/VC connection or may be used to perform checks on connections to isolate problems.
- Performance Management OAM cells. These cells are used to monitor performance (QoS) parameters such as cell block ratio, cell loss ratio and incorrectly inserted cells on VP/VC connections.

- Activation-deactivation OAM cells. These OAM cells are used to activate and deactivate the generation and processing of OAM cells, specifically continuity check (CC) and performance management (PM) cells.
- System management OAM cells. These OAM cells can be used to maintain and control various functions between end-user equipment. Their content is not specified by I.610, and they are limited to end-to-end flows.

The general format of an OAM cell is shown in the following figure.

#### OAM Cell Format

Header 5 bytes	OAM Type 4 bits	Function Type 4 bits	Function Specific Field 45 bytes	Reserved 6 bits	EDC CRC 10 bits
-------------------	-----------------------	----------------------------	--	--------------------	-----------------------

The header indicates which VCC or VPC an OAM cell belongs to. The cell payload is divided into five fields. The OAM-type and Function-type fields are used to distinguish the type of OAM cell. The Function Specific field contains information pertinent to that cell type. A 10 bit Cyclic Redundancy Check (CRC) is at the end of all OAM cells. This error detection code is used to ensure that management systems do not make erroneous decisions based on corrupted OAM cell information.

Ixia ATM modules allows to configure Fault Management and Activation/Deactivation OAM Cells.

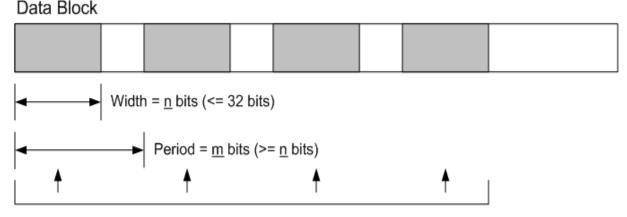
#### **BERT**

Bit Error Rate Test (BERT) load modules are packaged as both an option to OC48, POS, and 10GE load modules and as BERT-only load modules. As opposed to all other types of testing performed by Ixia hardware and software, BERT tests operate at the physical layer, also referred to as OSI Layer 1. POS frames are constructed using specific pseudorandom patterns, with or without inserted errors. The receive circuitry locks on to the received pattern and checks for errors in those patterns.

Both unframed and framed BERT testing is available. Framed testing can be performed in both concatenated and channelized modes with some load modules.

The patterns inserted within the POS frames are based on the ITU-T 0.151 specification. They consist of repeatable, pseudo-random data patterns of different bit-lengths which are designed to test error and jitter conditions. Other constant and user-defined patterns may also be applied. Furthermore, you may control the addition of deliberate errors to the data pattern. The inserted errors are limited to 32-bits in length and may be interspersed with non-errored patterns and repeated for a count. This is illustrated in the following figure. In the figure, an error pattern of  $\underline{n}$  bits occurs every  $\underline{m}$  bits for a count of 4. This error is inserted at the beginning of each POS data block within a frame.

#### Figure: BERT Inserted Error Pattern



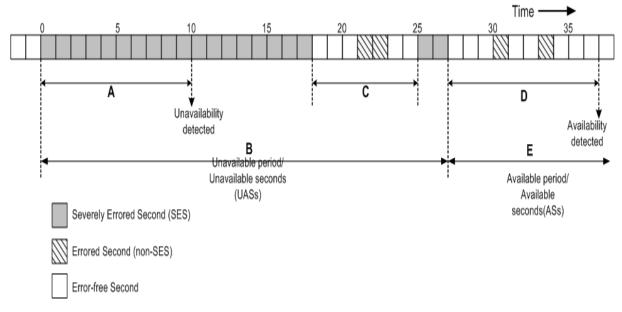
Count = 4

Errors in received BERT traffic are visible through the measured statistics, which are based on readings at one-second intervals. The statistics related to BERT are described in the *Available Statistics* appendix associated with the *Ixia Hardware Guide* and some other manuals.

# Available/Unavailable Seconds

Reception of POS signals can be divided into two types of periods, depending on the current state `Available' or `Unavailable,' as shown in the following figure. The seconds occurring during an unavailable period are termed Unavailable Seconds (UAS); those occurring during an available period are termed Available Seconds (AS).

Figure: BERT Unavailable/Available Periods



These periods are defined by the error condition of the data stream. When 10 consecutive SESs (A in the figure) are received, the receiving interface triggers an Unavailable Period. The period remains in the Unavailable state (B in the figure), until a string of 10 consecutive non-SESs is received (D in the figure), and the beginning of the Available state is triggered. The string of consecutive non-SESs in C in the figure was less than 10 seconds, which was insufficient to trigger a change to the Available state.

# **Port Hardware**

The ports on the Ixia load modules provide high-speed, transmit, capture, and statistics operation. The discussion which follows is broken down into a number of areas:

- <u>Types of Ports</u>: The different types of networking technology supported by Ixia load modules
- Port Transmit Capabilities: Facilities for generating data traffic
  - Streams and Flows: A set of packets, which may be grouped into bursts
  - Bursts and the Inter-Burst Gap (IBG): A number of packets
  - Packets and the Inter-Packet Gap (IPG): Individual frames/packets of data
- Frame Data: The construction of data within a frame/packet
- Port Data Capture Capabilities: Facilities for capturing data received on a port
- Port Statistics Capabilities: Facilities for obtaining statistics on each port

# **Types of Ports**

The types of load module ports that Ixia offers are divided into these broad categories:

- Ethernet
- · Power over Ethernet
- 10GE
- 40GE and 100GE
- SONET/POS
- ATM
- BERT

Only the currently available Ixia load modules are discussed in this chapter. Subsequent chapters in this manual discuss all supported load modules and their optional features.

#### **Ethernet**

Ethernet modules are provided with various feature combinations, as mentioned in the following list:

- Speed combinations: 10 Mbps, 100 Mbps, and 1000 Mbps
- Auto negotiation
- · Pause control
- With and without on-board processors, also called Port CPUs (PCPUs). Load modules without processors only allow for very limited routing protocol emulation
- Power over Ethernet (Described in Power over Ethernet)
- External connections including the following:
  - RJ-45
  - MII
  - RMII a custom Ixia connector
  - MT-RJ Fibre singlemode and multimode

- SC multimode
- GBIC singlemode and multimode

#### **Power over Ethernet**

The Power over Ethernet (PoE) load modules (PLM1000T4-PD and LSM1000POE4-02) are special purpose, 4-channel electronic loads. They are intended to be used in conjunction with Ixia ethernet traffic generator/analyzer load modules to test devices that conform to IEEE std 802.3af.

A PoE load module provides the hardware interface required to test the Power Sourcing Equipment (PSE) of a 802.3af compliant device by simulating a Powered Device (PD).

# **Power Sourcing Equipment (PSE)**

A PSE is any equipment that provides the power to a single link Ethernet Network section. The PSE's main functions are to search the link section for a powered device (PD), optionally classify the PD, supply power to the link section (only if a PD is detected), monitor the power on the link section, and remove power when it is no longer requested or required.

There are two power sourcing methods for PoE Alternative A and Alternative B.

PSEs may be placed in two locations with respect to the link segment, either coincident with the DTE/Repeater, or midspan. A PSE that is coincident with the DTE/Repeater is an `Endpoint PSE.' A PSE that is located within a link segment that is distinctly separate from and between the Media Dependent Interfaces (MDIs) is a `Midspan PSE.'

Endpoint PSEs may support either Alternative A, B, or both. Endpoint PSEs can be compatible with 10BASE-T, 100BASE-X, and/or 1000BASE-T.

Midspan PSEs must use Alternative B. Midspan PSEs are limited to operation with 10BASE-T and 100BASE-TX systems. Operation of Midspan PSEs on 1000BASE-T systems is beyond the scope of PoE.

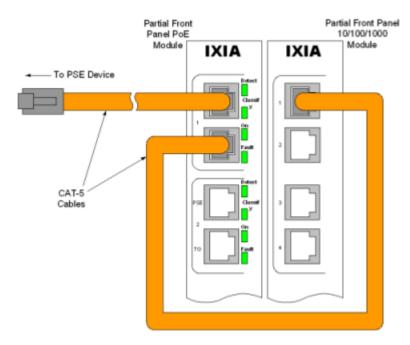
# Powered Devices (PD)

A powered device either draws power or requests power by participating in the PD detection algorithm. A device that is capable of becoming a PD may or may not have the ability to draw power from an alternate power source and, if doing so, may or may not require power from the PSE.

One PoE Load Module emulates up to four PDs. The PoE Load Module (PLM) has eight RJ-45 interfaces four of them used as PD-emulated ports, with each having its own corresponding interface that connects to a port on any Ixia 10/100/1000 copper-based Ethernet load module (includes all copper-based TXS, and Optixia load modules).

The following figure demonstrates how the PoE modules use an Ethernet card to transmit and receive data streams.

Figure: Data Traffic over PoE Set Up

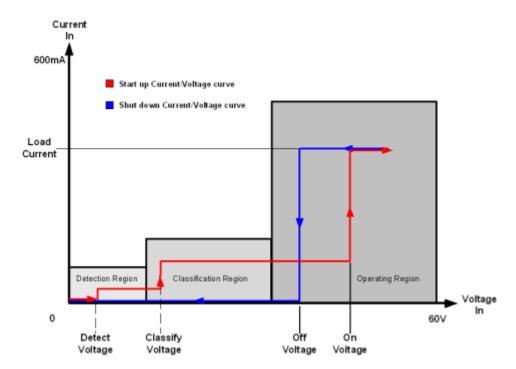


The emulated PD device can 'piggy-back' a signal from a different load module along the cable connected to the PSE from which it draws power. In this manner, the emulated PD can mimic a device that generates traffic, such as an IP phone.

# **Discovery Process**

The main purpose for discovery is to prevent damage to existing Ethernet equipment. The Power Sourcing Equipment (PSE) examines the Ethernet cables by applying a small current-limited voltage to the cable and checking for the presence of a 25K ohm resistor in the remote Powered Device (PD). Only if the resistor is present, the full 48V is applied (and this is still current-limited to prevent damage to cables and equipment in fault conditions). The Powered Device must continue to draw a minimum current or the PSE removes the power and the discovery process begins again.

Figure: Discovery Process Voltage



There is also an optional extension to the discovery process where a PD may indicate to the PSE its maximum power requirements, called classification. Once there is power applied to the PD, normal transactions/data transfer occurs. During this period, the PD sends back a *maintain power signature* (MPS) to signal the PSE to continue to provide power.

# **PoE Acquisition Tests**

During the course of testing with the PoE module, it may be necessary to measure the amplitude of the incoming current. The PoE module has the ability to measure amplitude versus time in following two ways:

- Time test: The amount of time that elapses between a *Start* and *Stop* incoming current measurement.
- Amplitude test: The amplitude of the current after a set amount of time from a *Start* incoming current setting.

In both scenarios, a Start trigger is set, indicating when the test should commence based on an incoming current value (in either DC Volts or DC Amps).

In a Time test, a Stop trigger is also set (in either DC Volts or DC Amps) indicating when the test is over. Once the Stop trigger is reached, the amount of time between the Start and Stop trigger is measured (in microseconds) and the result is reported.

In an amplitude test, an Amplitude Delay time is set (in microseconds), which is the amount of time to wait after the Start trigger is reached before ending the test. The amplitude at the end of the Amplitude Delay time is measured and is reported.

Both Start and Stop triggers must also have a defined Slope type, either positive or negative. A positive slope is equivalent to rising current, while a negative slope is equivalent to decreasing current. A current condition must agree with both the amplitude setting and the Slope type to satisfy the trigger condition.

An example of a Time test is shown in the following figure.

Current In (DC Volts)

PoE Time Acquisition

Operating

Figure: PoE Time Acquisition Example

An example of an Amplitude test is shown in the following figure.

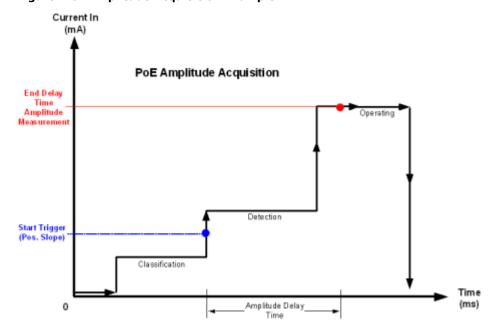


Figure: PoE Amplitude Acquisition Example

# **10GE**

The 10 Gigabit Ethernet (10GE) family of load modules implements five of the seven IEEE 8.2.3ae compliant interfaces that run at 10 Gbit/second. Several of the load modules may also be software switched to OC192 operation.

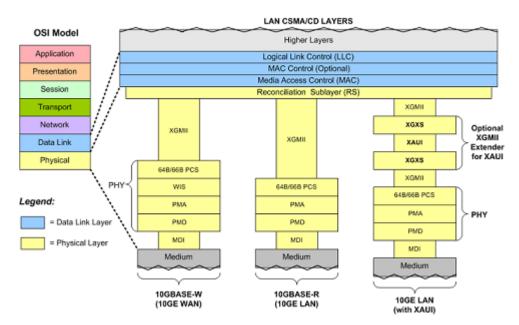
The 10 GE load modules are provided with various feature combinations, as mentioned in the following list:

- Interfaces types: LAN, WAN, XAUI, and XENPAK
- Interface connectors: SC singlemode (LAN and WAN), SC multimode (LAN), LC singlemode/multimode, XFP, XAUI, and XENPAK
- · Reach: Short, long, and extended
- Wavelengths: 850 nm, 1310 nm, 1550 nm

The relationship of the logical structures for the different 10 Gigabit types is shown in the diagram (adapted from the 802.3ae standard) in the following figure.

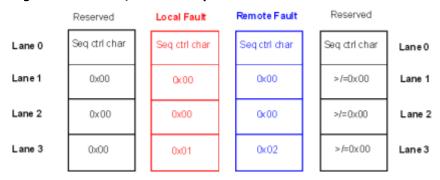
Figure: IEEE 802.3ae Draft 10 Gigabit Architecture

IEEE P802.3ae Model for 10GBASE-W, 10GBASE-R, & 10GE XAUI



For 10GE XAUI and 10GE XENPAK modules, a Status message contains a 4-byte ordered set with a Sequence control character plus three data characters (in hex), distributed across the four lanes, as shown in the following figure. Four Sequence ordered sets are defined in IEEE 802.3ae, but only two of these Local Fault and Remote Fault are currently in use; the other two are reserved for future use.

Figure: 10GE XAUI/XENPAK Sequence Ordered Sets



#### **XAUI Interfaces**

The 10 Gigabit XAUI interface has been defined in the IEEE draft specification P802.3ae by the 10 Gigabit Ethernet Task Force (10GEA). XAUI stands for `X' (the Roman Numeral for

10, as in `10 Gigabit'), plus `AUI' or Attachment Unit Interface originally defined for Ethernet.

The original Ethernet standard was defined in IEEE 802.3, and included MAC layer, frame size, and other `standard' Ethernet characteristics. IEEE 802.3z defined the Gigabit standard. IEEE 802.3ae has been created to create a simplified version of SONET framing to carry native Ethernet-framed traffic over high-speed fiber networks. This new standard allows a smooth transition from 10 Gbps native Ethernet traffic to work with 9.6 Gbps for SONET at OC-192c rate over WAN and MAN links. The 10GE XAUI has a XAUI interface for connecting to another XAUI interface, such as on a DUT. A comparison of the IEEE P802.3ae model for XAUI and the OSI model is shown in the following figure.

IEEE P802.3ae Model for 10GE XAUI LAN CSMA / CD LAYERS Higher Layers OSI Model Logical Link Control (LLC) Application MAC Control (Optional) Presentation Media Access Control (MAC) Session Reconciliation Sublayer (RS) 10 Gigabit Media Independent Interface Transport (XGMII) XGMII Extender Sublayer Network (DTE XGXS) Optional Data Link XGMII 10 Gigabit Attachment Unit Interface (XAUI) Extender for XAUI Physical XGMII Extender Sublayer (PHY XGXS) 10 Gigabit Media Independent Interface (XGMII) Physical Coding Sublayer64B/66B (PCS) Legend: Physical Medium Attachment PHY Sublayer (PMA) Data Link Layer Physical Medium Dependent Sublayer (PMD) = Physical Layer (PHY) Medium Dependent Interface (MDI) Medium

Figure: IEEE P802.3ae Architecture for 10GE XAUI

#### **Lane Skew**

The Lane Skew feature provides the ability to independently delay one or more of the four XAUI lanes. The resolution of the skew is 3.2 nanoseconds (ns), which consists of 10 Unit Intervals (UIs), each of which is 320 picoseconds (ps). Each UI is equivalent to the amount of time required to transmit one XAUI bit at 3.125 Gbps.

Lane Skew allows a XAUI lane to be skewed by as much as 310 UI (99.2ns) with respect to the other three lanes. To effectively use this feature, the four lanes should be set to different skew values. Setting all four lanes to zero is equivalent to setting all four lanes to +80 UI. In both cases, the lanes are synchronous and there is no lane skew. When lane skewing is enabled, /A/, /K/, and /R/ codes are inserted into the data stream BEFORE the

lanes are skewed. The principle behind lane skewing is shown in the diagrams in the following images.

Figure: XAUI Lane Skewing Lane Skew Disabled

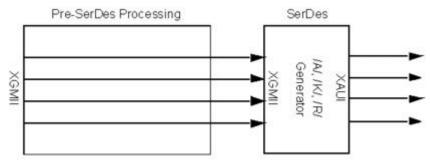
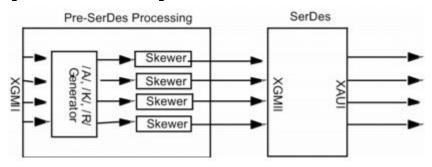


Figure: XAUI Lane Skewing Lane Skew Enabled



# **Link Fault Signaling**

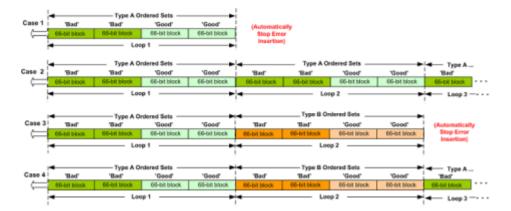
Link Fault Signaling is defined in Section 46 of the IEEE 802.3ae specification for 10 Gigabit Ethernet. When the feature is enabled, four statistics are added to the list in Statistic View for the port. One is for monitoring the Link Fault State; two for providing a count of the Local Faults and Remote Faults; and the last one is for indicating the state of error insertion, whether or not it is ongoing.

Link Fault Signaling originates with the PHY sending an indication of a local fault condition in the link being used as a path for MAC data. In the typical scenario, the Reconciliation Sublayer (RS) which had been receiving the data receives this Local Fault status, and then send a Remote Fault status to the RS which was sending the data. Upon receipt of this Remote Fault status message, the sending RS terminates transmission of MAC Data, sending only `Idle' control characters until the link fault is resolved.

For the 10GE LAN and LAN-M serial modules, the Physical Coding Sublayer (PCS) of the PHY handles the transition from 64 bits to 66 bit `Blocks.' The 64 bits of data are scrambled, and then a 2-bit synchronization (sync) header is attached before transmission. This process is reversed by the PHY at the receiving end.

Link Fault Signaling for the 10GE XAUI/XENPAK is handled differently across the four-lane XAUI optional XGMII extender layer, which uses 8B/10B encoding.

#### **Examples of Link Fault Signaling Error Insertion**



The examples in this figure are described in the following table:

Cases for Example

Case	Conditions
	Contiguous Bad Blocks = 2 (the minimum).
Case 1	Contiguous Good Blocks = 2 (the minimum).
	Send Type A ordered sets.
	Loop 1x.
	Contiguous Bad Blocks = 2 (the minimum).
Case 2	Contiguous Good Blocks = 2 (the minimum).
	Send Type A ordered sets.
	Loop continuously.
	Contiguous Bad Blocks = 2 (the minimum).
Case 3	Contiguous Good Blocks = 2 (the minimum).
	Send alternate ordered set types.
	Loop 1x.
	Contiguous Bad Blocks = 2 (the minimum).
Case 4	Contiguous Good Blocks = 2 (the minimum).
	Send alternate ordered set types.
	Loop continuously.

# Link Alarm Status Interrupt (LASI)

The link alarm status is an active low output from the XENPAK module that is used to indicate a possible link problem as seen by the transceiver. Control registers are provided so that LASI may be programmed to assert only for specific fault conditions.

Efficient use of XENPAK and its specific registers requires an end-user system to recognize a connected transceiver as being of the XENPAK type. An Organizationally Unique Identifier (OUI) is used as the means of identifying a port as XENPAK, and also to communicate the device in which the XENPAK specific registers are located.

Ixia's XENPAK module allows for setting whether or not LASI monitoring is enabled, what register configurations to use, and the OUI. The XENPAK module can use the following registers:

- Rx Alarm Control (Register 0x9003): It can be programmed to assert only when specific receive path fault condition(s) are present.
- Tx Alarm Control (Register 0x9001): It can be programmed to assert only when specific transmit path fault condition(s) are present.
- LASI Control (Register 0x9002): A LASI control register that allows global masking of the Rx Alarm and Tx Alarm.

You can control the registers by setting a series of sixteen bits for each register. The register bits and their usage are described in the following tables.

#### Rx Alarm Control

Bits	Description	Default
15 - 11	Reserved	0
10	Vendor Specific	N/A (vendor Setting)
9	WIS Local Fault Enable	1 (when imple- mented)
8 - 6	Vendor Specific	N/A (vendor Setting)
5	Receive Optical Power Fault Enable	1 (when imple- mented)
4	PMA/PMD Receiver Local Fault Enable	1 (when imple- mented)
3	PCS Receive Local Fault Enable	1
2 - 1	Vendor Specific	N/A (vendor Setting)
0	PHY XS Receive Local Fault Enable	1

Tx Alarm Control

Bits	Description	Default
15 - 11	Reserved	0
10	Vendor Specific	N/A (vendor setting)
9	Laser Bias Current Fault Enable	1 (when imple- mented)
8	Laser Temperature Fault Enable	1 (when imple- mented)

Bits	Description	Default
7	Laser Output Power Fault Enable	1 (when imple- mented)
6	Transmitter Fault Enable	1
5	Vendor Specific	N/A (vendor setting)
4	PMA/PMD Transmitter Local Fault Enable	1 (when imple- mented)
3	PCS Transmit Local Fault Enable	1
2 - 1	Vendor Specific	N/A (vendor setting)
0	PHY XS Transmit Local Fault Enable	1

LASI Control

Bits	Description	Default
15 - 8	Reserved	0
7 - 3	Vendor Specific	0 (when implemented)
2	Rx Alarm Enable	0
1	Tx Alarm Enable	0
0	LS Alarm Enable	0

For more detailed information on LASI, see the online document XENPAK MSA Rev. 3.

# **40GE and 100GE**

For theoretical information, refer to 40 Gigabit Ethernet and 100 Gigabit Ethernet Technology Overview White Paper, published by Ethernet Allliance, November, 2008. This white paper may be obtained through the Internet.

http://www.ethernetalliance.org/images/40G\_100G\_Tech\_overview.pdf

# **SONET/POS**

SONET/POS modules are provided with various feature combinations:

- Different speeds: OC3, OC12, OC48, OC192, Fibre Channel, 2x Fibre Channel, and Gigabit Ethernet.
- Interfaces: SC singlemode and multimode (OC3, OC12, OC192), SC singlemode (OC48), no optical transceiver, SFP LC singlemode (Unframed BERT) and custom interface.
- Reach: long, intermediate and long.
- Wavelengths: 850nm, 1310nm and 1550nm.

- Local processor support. All SONET/POS load modules include a local processor, but the power of the processor and amount of memory varies.
- Variable clocking OC48 only, see Variable Rate Clocking
- Concatenated or channelized SONET operation, see SONET Operation
- Error insertion, see Error Insertion
- BERT: Bit Error Rate Testing both framed and unframed, see <u>BERT</u>
- DCC: Data Communication Channel, see <a href="DCC Data Communications Channel">DCC Data Communications Channel</a>.
- RPR: Resilient Packet Ring, see RPR Resilient Packet Ring.
- GFP: Generic Framing Procedure, see GFP Generic Framing Procedure.
- PPP: Point to Point protocol, see PPP Protocol Negotiation.
- HDLC: High-Level Data Link Control, see HDLC.
- Frame Relay: see Frame Relay.
- DSCP: see DSCP Differentiated Services Code Point.

# Variable Rate Clocking

The OC48 VAR allows a variation of +/- 100 parts per million (ppm) from the clock source's nominal frequency, through a DC voltage input into the BNC jack marked `DC IN' on the front panel. The frequency may be monitored through the BNC marked `Freq Monitor.'

# **SONET Operation**

A Synchronous Optical NETwork/Synchronous Digital Hierarchy (SONET/SDH) frame is based on the Synchronous Transport Signal-1 (STS-1) frame, whose structure is shown in the figure below. Transmission of SONET Frames of this size correspond to the Optical Carrier level 1 (OC-1).

An OC-3c, consists of three OC-1/STS-1 frames multiplexed together at the octet level. OC-12c, OC-48c, and OC-192c, are formed from higher multiples of the basic OC-1 format. The suffix `c' indicates that the basic frames are concatenated to form the larger frame.

Ixia supports both concatenated (with the `c') and channelized (without the `c') interfaces. Concatenated interfaces send and receive data in a single streams of data. Channelized interfaces send and receive data in multiple independent streams.

Section & Line Overhead / Transport Overhead (TOH) Synchronous Payload Envelope (SPE) -Byte 2 Byte 3 Byte 1 Bytes 4-90 Payload Capacity Overhead Rows Line Overhead Path Byte 810 - 3 Bytes-87 Bytes 90 Bytes (for STS-1 Frame)

Figure: Generated Frame Contents SONET STS-1 Frame

SONET Frame Transmit time = 125 µsec

The contents of the SONET STS-1 frame are described in the following table.

SONET STS-1 Frame Contents

Section	Description
Section Over- head (SOH)	Consists of 9 bytes which include information relating to performance monitoring of the STS-n signal, and framing.
Line Over- head (LOH)	Consists of 18 bytes which include information relating to performance monitoring of the individual STS-1s, protection switching information, and line alarm indication signals.
Transport Overhead (TOH)	Consists of a combination of the Section Overhead and Line Overhead sections of the STS-1 frame.
Path Over- head (POH)	Part of the Synchronous Payload Envelope (SPE), contains information on the contents of the SPE, and handles quality monitoring.
Synchronous Payload Envel- ope (SPE)	Contains the payload information, the packets which are being transmitted, and includes the Path Overhead bytes.
Payload Capa-	Part of the SPE, and contains the packets being transmitted.

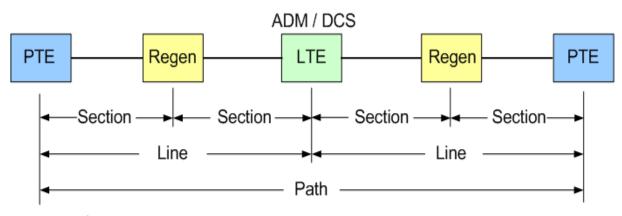
Section	Description
city	

The SONET STS-1 frame is transmitted at a rate of 51.84 Mbps, with 49.5 Mbps reserved for the frame payload. A SONET frame is transmitted in 125 microseconds, with the order of transmission of the starting with Row 1, Byte 1 at the upper left of the frame, and proceeding by row from top to bottom, and from left to right.

The section, line, and path overhead elements are related to the manner in which SONET frames are transmitted, as shown in the following figure.

#### **Example Diagram of SONET Levels and Network Elements**

# **SONET Levels**



#### Legend:

PTE = Path Terminating Entity, SONET Terminal or Switch

LTE = Line Terminating Entity, SONET Hub (ADM or DCS)

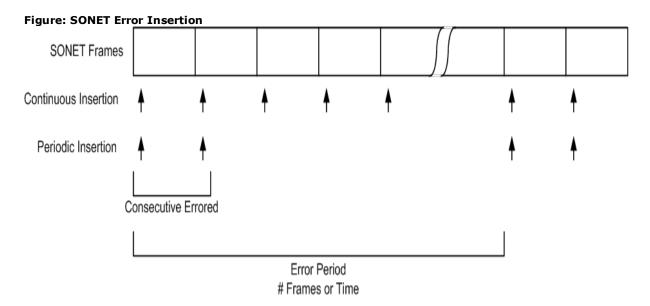
Regen = Regenerator

ADM = Add/Drop Multiplexer

DCS = Digital Cross-connect System

#### **Error Insertion**

A variety of deliberate errors may be inserted in SONET frames in the section, line or path areas of a frame. The errors which may be inserted vary by particular load module. Errors may be inserted continuously or periodically as shown in the following figure.



An error may be inserted in one of two manners:

- Continuous: Each SONET frame receives the error.
- Periodic: A number of errors are inserted in consecutive frames and the pattern is repeated based on a number of frames or a period of time. Predefined periods are available, or you may create your own predefined periods.

Each error may be individually inserted continuously or periodically. Errors may be inserted on a one time basis over a number of frames as well.

#### **DCC Data Communications Channel**

The data communication channel is a feature of SONET networks which uses the DCC bytes in the transport overhead of each frame. This is used for control, monitoring and provisioning of SONET connections. Ixia ports treat the DCC as a data stream which `piggybacks' on the normal SONET stream. The DCC and normal (referred to as the SPE - Synchronous Payload Envelope) streams can be transmitted independently or at the same time.

A number of different techniques are available for transmitting DCC and SPE data, utilizing Ixia streams and flows (see <u>Streams and Flows</u> and advanced stream scheduler (see <u>Advanced Streams</u>).

#### **SRP Spatial Reuse Protocol**

The Spatial Reuse Protocol (SRP) was developed by Cisco for use with ring-based media. It derives its name from the spatial reuse properties of the packet handling procedure. This optical transport technology combines the bandwidth-efficient and service-rich capabilities of IP routing with the bandwidth-rich, self-healing capabilities of fiber rings to deliver fundamental cost and functionality advantages over existing solutions. In SRP mode, the usual POS header (PPP, and so forth) is replaced by the SRP header.

SRP networks use two counter-rotating rings. One Ixia port may be used to participate in one of the rings; two may be used to simultaneously participate in both rings. Ixia supports SRP on both OC48 and OC192 interfaces.

In SRP-mode, SRP packets can be captured and analyzed. The IxExplorer capture view displays packet analysis which understands SRP packets. The Ixia hardware also collects specific SRP related statistics and performs filtering based on SRP header contents.

Any of the following SRP packet types may be generated in a data stream, along with normal IPv4 traffic:

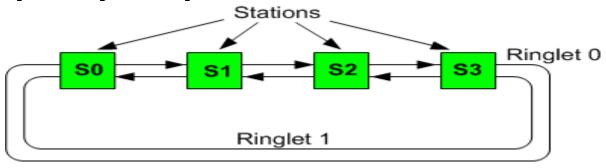
- SRP Discovery
- SRP ARP
- SRP IPS (Intelligent Protection Switching)

# **RPR Resilient Packet Ring**

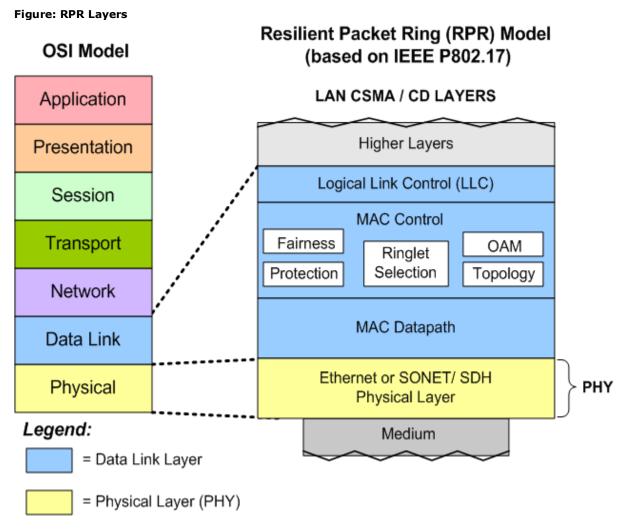
Ixia's optional Resilient Packet Ring (RPR) implementation is available on the OC-48c and OC-192c POS load modules. RPR is a proposed industry standard for MAC Control on Metropolitan Area Networks (MANs), defined by IEEE P802.17. This feature provides a cost-effective method to optimize the transport of bursty traffic, such as IP, over existing ring topologies.

A diagram showing a simplified model of an RPR network is shown in the following figure. It is made up of two, counter-rotating `ringlets,' with nodes called `stations' supporting MAC Clients that exchange data and control information with remote peers on the ring. Up to 255 nodes can be supported on the ring structure.

Figure: RPR Ring Network Diagram



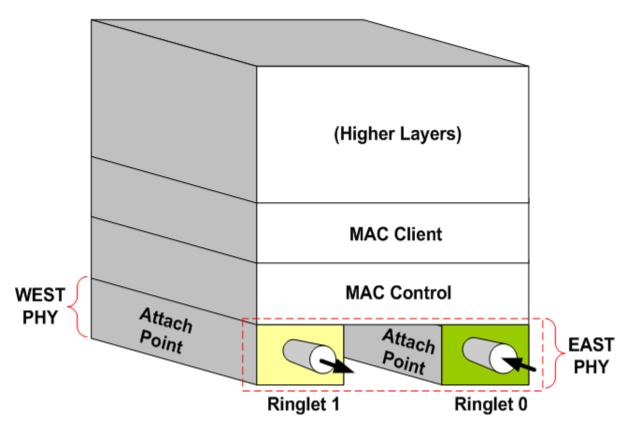
The RPR topology discovery is handled by a MAC sublayer, and a protection function maintains network connectivity in the event of a station or span failure. The structure of the RPR layers, compared to the OSI model, is illustrated in a diagram based on IEEE 802.17, shown in the following figure.



A diagram of the layers associated with an RPR Station is shown in the following figure.

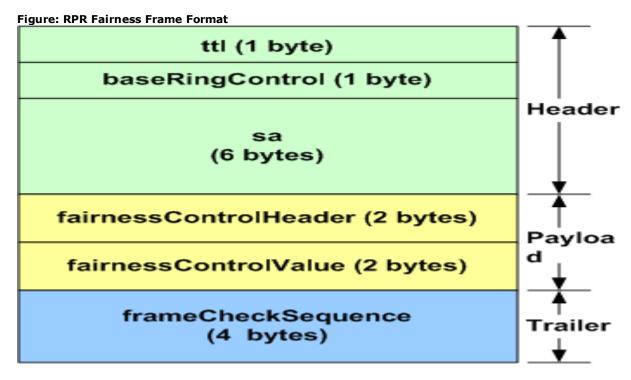
Figure: RPR Layer Diagram

# **RPR Station**



The Ixia implementation allows for the configuration and transmission of the following types of RPR frames:

• RPR Fairness Frames: The RPR Fairness Algorithm (FA) is used to manage congestion on the ringlets in an RPR network. Fairness frames are sent periodically to advertise bandwidth usage parameters to other nodes in the network to maintain weighted fair share distributions of bandwidth. The messages are sent in the direction opposite to the data flow, and therefore, on the other ringlet. A diagram of the RPR Fairness Frame, per IEEE 802.17/D2.1, is shown in the following figure.



A diagram of the baseRingControl byte, part of the Ring Control header for all types of RPR frames, is shown in the following figure.

#### Figure: RPR baseRingControl Byte

#### baseRingControl Field MSB LSB **Bits** 7 3:2 6 5:4 1 0 RI FE FT SC WE Р

- RPR Topology Discovery. Two types of messages are used:
  - RPR Topology Discovery Message: for the discovery of the physical topology.
  - RPR Topology Extended Status Message: for the transmission of additional information from a node concerning bandwidth and other configuration options. This format uses TLV (Type-Length-Value) options, including:
    - Weight
    - Total reserved bandwidth
    - Neighbor address
    - Individual reserved bandwidth
    - Station name
    - Vendor specific data
- RPR Protection Switching Message: used to support automatic, rapid switching of traffic in the presence of a ring failure.
- RPR Operations, Administration and Management (OAM). Three messages are supported:

- Echo Request and Response messages
- Flush Frames
- Vendor specific message

# **GFP Generic Framing Procedure**

GFP provides a generic mechanism to adapt traffic from higher-layer client signals over a transport network. Currently, two modes of client signal adaptation are defined for GFP.

- A PDU-oriented adaptation mode, referred to as Frame-Mapped GFP (GFP-F, for traffic such as IP/PPP or Ethernet MAC).
- A block-code oriented adaptation mode, referred to as Transparent GFP (GFP-T, for traffic such as Fibre Channel or ESCON/SBCON).

In the Frame-Mapped adaptation mode, the Client/GFP adaptation function operates at the data link (or higher) layer of the client signal. Client PDU visibility is required, which is obtained when the client PDUs are received from either the data layer network or a bridge, switch, or router function in a transport network element.

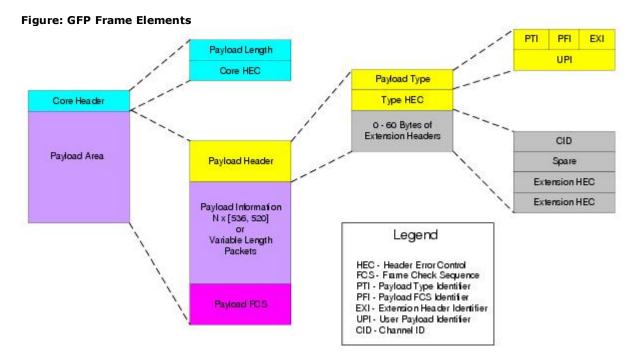
For the Transparent adaptation mode, the Client/GFP adaptation function operates on the coded character stream, rather than on the incoming client PDUs. Processing of the incoming code word space for the client signal is required.

Two kinds of GFP frames are defined: GFP client frames and GFP control frames. GFP also supports a flexible (payload) header extension mechanism to facilitate the adaptation of GFP for use with diverse transport mechanisms.

GFP uses a modified version of the Header Error Check (HEC) algorithm to provide GFP frame delineation. The frame delineation algorithm used in GFP differs from HEC in two basic ways:

- The algorithm uses the PDU Length Indicator field of the GFP Core Header to find the end of the GFP frame.
- HEC field calculation uses a 16-bit polynomial and, consequently, generates a twooctet cHEC field.

A diagram of the format for a GFP frame is shown in the following figure.



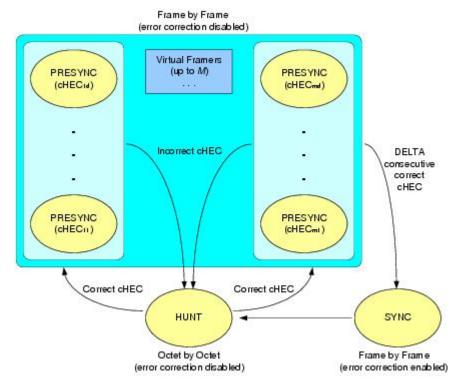
The sections of the GFP frame are described in the following list:

- Payload Length Indicator (PLI): The two-octet PLI field contains a binary number representing the number of octets in the GFP Payload Area. The absolute minimum value of the PLI field in a GFP client frame is 4 octets. PLI values 0-3 are reserved for GFP control frame usage.
- Core Header Error Control (cHEC): The two-octet Core Header Error Control field contains a CRC-16 error control code that protects the integrity of the contents of the Core Header by enabling both single-bit error correction and multi-bit error detection.
- Type Header Error Control (tHEC): The two-octet Type Header Error Control field contains a CRC-16 error control code that protects the integrity of the contents of the Type field by enabling both single-bit error correction and multi-bit error detection.
- Extension Header Error Control (eHEC): The two-octet Extension Header Error Control field contains a CRC-16 error control code that protects the integrity of the contents of the extension headers by enabling both single-bit error correction (optional) and multi-bit error detection.
- Connection Identification (CID): The CID is an 8-bit binary number used to indicate one of 256 communications channels at a GFP termination point.
- Payload: The GFP Payload Area, which consists of all octets in the GFP frame after the GFP Core Header, is used to convey higher layer specific protocol information. This variable length area may include from 4 to 65,535 octets. The GFP Payload Area consists of two common components:
  - A Payload Header and a Payload Information field
  - An optional Payload FCS (pFCS) field
     Practical GFP MTU sizes for the GFP Payload Area are application specific.
- Frame Check Sequence (FCS): The GFP Payload FCS is an optional, four-octet long, frame check sequence. It contains a CRC-32 sequence that protects the contents of

the GFP Payload Information field. A value of 1 in the PFI bit within the Type field identifies the presence of the payload FCS field.

GFP frame delineation is performed based on the correlation between the first two octets of the GFP frame and the embedded two-octet cHEC field. The following figure shows the state diagram for the GFP frame delineation method.

**Figure: GFP State Transitions** 



The state diagram works as follows:

- In the HUNT state, the GFP process performs frame delineation by searching octets for a correctly formatted Core Header over the last received sequence of four octets. Once a correct cHEC match is detected in the candidate Payload Length Indicator (PLI) and cHEC fields, a candidate GFP frame is identified and the receive process enters the PRESYNC state.
- 2. In the PRESYNC state, the GFP process performs frame delineation by checking frames for a correct cHEC match in the presumed Core Header of the next candidate GFP frame. The PLI field in the Core Header of the preceding GFP frame is used to find the beginning of the next candidate GFP frame. The process repeats until a set number of consecutive correct cHECs are confirmed, at which point the process enters the SYNC state. If an incorrect cHEC is detected, the process returns to the HUNT state.
- 3. In the SYNC state, the GFP process performs frame delineation by checking for a correct cHEC match on the next candidate GFP frame. The PLI field in the Core Header of the preceding GFP frame is used to find the beginning of the next candidate GFP frame. Frame delineation is lost whenever multiple bit errors are detected in the Core Header by the cHEC. In this case, a GFP Loss of Frame Delineation event is declared, the framing process returns to the HUNT state, and a client Server Signal

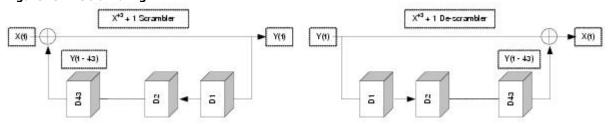
Failure (SSF) is indicated to the client adaptation process.

4. Idle GFP frames participate in the delineation process and are then discarded.

Robustness against false delineation in the resynchronization process depends on the value of DELTA. A value of DELTA = 1 is suggested. Frame delineation acquisition speed can be improved by the implementation of multiple `virtual framers,' whereby the GFP process remains in the HUNT state and a separate PRESYNC substate is spawned for each candidate GFP frame detected in the incoming octet stream.

Scrambling of the GFP Payload Area is required to provide security against payload information replicating scrambling word (or its inverse) from a frame synchronous scrambler (such as those used in the SDH RS layer or in an OTN OPUk channel). The following figure illustrates the scrambler and descrambler processes.

Figure: GFP Scrambling



All octets in the GFP Payload Area are scrambled using a  $x^{43} + 1$  self-synchronous scrambler. Scrambling is done in network bit order.

At the source adaptation process, scrambling is enabled starting at the first transmitted octet after the cHEC field, and is disabled after the last transmitted octet of the GFP frame. When the scrambler or descrambler is disabled, its state is retained. Hence, the scrambler or descrambler state at the beginning of a GFP frame Payload Area is, thus, the last 43 Payload Area bits of the GFP frame transmitted in that channel immediately before the current GFP frame.

The activation of the sink adaptation process descrambler also depends on the present state of the cHEC check algorithm:

- In the HUNT and PRESYNC states, the descrambler is disabled.
- In the SYNC state, the descrambler is enabled only for the octets between the cHEC field and the end of the candidate GFP frame.

#### **CDL Converged Data Link**

10GE LAN, 10GE XAUI, 10GE XENPAK, 10GE WAN, and 10GE WAN UNIPHY modules all support the Cisco CDL preamble format.

The Converged Data Link (CDL) specification was developed to provide a standard method of implementing operation, administration, maintenance, and provisioning (OAM&P) in Ethernet packet-based optical networks without using a SONET/SDH layer.

# **PPP Protocol Negotiation**

The Point-to-Point Protocol (PPP) is widely used to establish, configure and monitor peer-to-peer communication links. A PPP session is established in a number of steps, with each step completing before the next one starts. The steps, or layers, are:

- 1. Physical: a physical layer link is established.
- 2. Link Control Protocol (LCP): establishes the basic communications parameters for the line, including the Maximum Receive Unit (MRU), type of authentication to be used and type of compression to be used.
- 3. Link quality determination and authentication. These are optional processes. Quality determination is the responsibility of PPP Link Quality Monitoring (LQM) Protocol. Once initiated, this process may continue throughout the life of the link. Authentication is performed at this stage only. There are multiple protocols which may be employed in this process; the most common of these are PAP and CHAP.
- 4. Network Control Protocol (NCP): establishes which network protocols (such as IP, OSI, MPLS) are to be carried over the link and the parameters associated with the protocols. The protocols which support this NCP negotiation are called IPCP, OSINLCP, and MPLSCP, respectively.
- 5. Network traffic and sustaining PPP control. The link has been established and traffic corresponding to previously negotiated network protocols may now flow. Also, PPP control traffic may continue to flow, as may be required by LQM, PPP keepalive operations, and so forth.

All implementations of PPP must support the Link Control Protocol (LCP), which negotiates the fundamental characteristics of the data link and constitutes the first exchange of information over an opening link. Physical link characteristics (media type, transfer rate, and so forth) are not controlled by PPP.

The Ixia PPP implementation supports LCP, IPCP, MPLSCP, and OSINLCP. When PPP is enabled on a given port, LCP and at least one of the NCPs must complete successfully over that port before it is administratively `up' and therefore be ready for general traffic to flow.

Each Ixia POS port implements a subset of the LCP, LQM, and NCP protocols. Each of the protocols is of the same basic format. For any connection, separate negotiations are performed for each direction. Each party sends a *Configure-Request* message to the other, with options and parameters proposing some form of configuration. The receiving party may respond with one of three messages:

- *Configure-Reject*: The receiving party does not recognize or prohibits one or more of the suggested options. It returns the problematic options to the sender.
- Configure-NAK: The receiving party understands all of the options, but finds one or more of the associated parameters unacceptable. It returns the problematic options, with alternative parameters, to the sender.
- Configure-ACK: The receiving party finds the options and parameters acceptable.

For the *Configure-Reject* and *Configure-NAK* requests, the sending party is expected to reply with an alternative *Configure-Request*.

The Ixia port may be configured to immediately start negotiating after the physical link comes up, or passively wait for the peer to start the negotiation. Ixia ports both sends and responds to PPP keepalive messages called echo requests.

# **LCP Link Control Protocol Options**

The following sections outline the parameters associated with the Link Control Protocol. LCP includes a number of possible command types, which are assigned option numbers in

the pertinent RFCs. Note that PPP parameters are typically independently negotiated for each direction on the link.

Numerous RFCs are associated with LCP, but the most important RFCs are RFC 1661 and RFC 1662. The HDLC/PPP header sequence for LCP is FF 03 C0 21.

During the LCP phase of negotiation, the Ixia port makes available the following options:

• Maximum Receive Unit: This LCP parameter (actually the set of Maximum Receive Unit (MRU) and Maximum Transmit Unit (MTU)) determines the maximum allowed size of any frame sent across the link subsequent to LCP completion. To be fully standards-compliant, an implementation must not send a frame of length greater than its MTU + 4 bytes + CRC length. For instance, if the negotiated MTU for a port is 2000 and 32 bit CRC is in use, no frame larger than 2008 bytes should ever be sent out that port. Packets that are larger are expected to be fragmented before transmitting or to be dropped. The Ixia port's MTU is the peer's MRU following LCP negotiation. Strictly speaking, the receiving side can assume that frames received is not greater than the MRU. In practice, however, an implementation should be capable of accepting larger frames. If a peer rejects this option altogether, the negotiated setting defaults to 1,500. Regardless of the negotiated MRU, all implementations must be capable of accepting frames with an information field of at least 1,500 bytes.

For the transmit direction portion of the negotiation, the peer sends the Ixia port its configuration request. The Ixia port accepts and acknowledges the peer's requested MRU as long as it is less than or equal to the specified user's desired transmit value (but greater than 26). For the receive direction portion of the negotiation, the Ixia port sends a configuration request based on the user's desired value. Generally, the Ixia port accepts what the peer desires (if it acknowledges the request, then the user value is used, or if the peer sends a *Configure-Nak* with another value the Ixia port uses that value as long as it is valid). This approach is used to maximize the probability of successful negotiation.

• Asynchronous Control Character Map: ACCM is only really pertinent to asynchronous links. On asynchronous lines, certain characters sent over the wire can have special meaning to one or more receiving entities. For instance, common implementations of the widely used XON/XOFF flow control protocol assign the ASCII DC3 character (0x13) to XOFF. On such a link, an embedded data byte that happens to have the value 0x13 would be misinterpreted by a receiver as an XOFF command, and cause suspension of reception. To avoid this problem, the 0x13 character embedded in the data could be sent through an `escape sequence' which consists of preceding the data character with a dedicated tag character and modifying the data character itself.

The Asynchronous Control Character Map (ACCM) LCP parameter allows independent designation of each character in the range 0x00 thru 0x1F as a control character. A control character is sent/received with a preceding `control-escape' character (0x7D). When the 0x7D is seen in the received data stream, the 0x7D is dropped and the next character is exclusive-or'd with 0x20 to get the original transmitted character. ACCM negotiation consists of exchanging masks between peers to reach an agreement as to which characters are treated as special control characters on transmission and reception. For example, sending a mask of 0xFFFFFFFF means all characters in the range 0x00 thru 0x1F are sent with escape sequences; a mask of 0 means no special handling, so all characters are arbitrary data.

Packet over SONET is an octet-synchronous medium. If the link is direct between POS peers, neither side should be generating control-escapes. (Exceptions to this are bytes 0x7D and 0x7E: the former is the special control escape character itself; the latter is the start/end frame marker. Escaping of these two characters is generally handled directly by physical layer hardware). On links in which there is some kind of intermediate asynchronous media, it is required that whatever device performs the asynchronous to synchronous conversion must also take care of any special character handling, isolating this from any POS port. See RFC 1662, sections 4.1 and 6.

If ACCM negotiation is enabled, the Ixia port advertises an ACCM mask of 0 to its peer in its LCP configuration request. The Ixia port accept whatever the peer puts forth, but does not act on the results. Regardless of the final negotiated settings for receive and transmit ACCM, the Ixia port does not send escape control sequences nor does it expect to receive them. This is the nature of a synchronous PPP medium, such as POS.

Magic Number: A magic number is a 32-bit value, ideally numerically random, which
is placed in certain PPP control packets. Magic numbers aid in detection of looped
links. If a received PPP packet that includes a magic number matches a previously
transmitted packet, including magic number, the link is probably looped.

IxExplorer and the Tcl APIs allow global enable/disable of magic number negotiation. If the `Use Magic Number' feature is enabled, the Ixia port does not request

magic number of its peer and rejects the option if the peer requests it. If the check box is selected, the port attempts to negotiate magic number. The result of the bi-directional negotiation process is displayed in the fields for transmit and receive: an indication of whether magic number is enabled is written in the field for the corresponding direction.

#### **NCP Network Control Protocols**

• IPCP: Internet Protocol Control Protocol Options for IPV4. IPCP includes three command types, which are assigned option numbers in the pertinent RFCs. Note that PPP parameters are typically independently negotiated for each direction on the link. The sender of this Configure-Request may either include its own IP address, to provide this information to its remote peer, or may send all 0.0.0.0 as an IP address, which requests that the remote peer assign an IP address for the local node. The receiver may refuse the requested IP address and attempt to specify one for the peer to use by using a Configure-NAK response to the request with a specification of a different address.

The Ixia implementation provides minimal configuration of this parameter. You must specify the local IP address of the unit and the peer must provide its own IP address. The Ixia port accepts any IP address the peer wishes to use as long as it is a valid address (for example, not all 0's). The Ixia port expects the peer to accept its address. If, however, the peer specifies a different address for use, the port acknowledges that address but not actually notify you that this has happened. The Ixia port accepts a situation in which local and peer addresses are the same following negotiation.

- IPv6CP: Internet Protocol Control Protocol Options for IPv6. IPv6CP includes three command types, which are assigned option numbers in the pertinent RFCs. Note that PPP parameters are typically independently negotiated for each direction on the link. A PPP peer may determine its IPv6 interface address by one or three methods:
  - Generate its own address.
  - Suggest its own address to its peer, but allow the peer to override that value.
  - Require that the peer designate an address.

In any of these cases, the *Configure-Request* must contain a tentative interface-identifier to send to the peer that is both unique to the link and if possible consistently reproducible.

The Ixia PPP implementation of IPv6CP is such that the negotiation mode of the local endpoint may be configured in one of three modes:

- Local may: the local peer may suggest an Interface Identifier (IID), but most allow a *Configure-NAK* with an alternate address to override its setting.
- Local must: the local peer must set the IID, which the peer must accept.
- Peer must: the peer must supply the IID. This is accomplished by sending an all zero tentative IID.

The peer endpoint may be configured in one of three modes:

- Peer may: the remote peer may suggest an IID, but most allow a Configure-NAK with an alternate address to override its setting.
- Peer must: the remote peer must set the IID, which the local peer accepts.
- Local must: the local peer must supply the IID.

One IID can be sent in each Configuration-Request. A zero value may be sent, in which case, the peer may send an IID in its response. Either node on the link can provide the valid, non-zero IID values for itself and its peer.

The tentative, or assigned IID in the *Peer - Local Must* case, may be assigned from one of four sources:

- Last Negotiated: the last negotiated interface-identifier.
- MAC Based: an address derived from the port's MAC address.
- IPv6: an IPv6 format address.
- Random: a randomly generated value.

See IPv6 Interface Identifiers as follows for more information.

- OSI Network Layer Control Protocol (OSINLCP): A single option is provided for this NCP protocol. If a non-zero value for alignment has been negotiated, subsequent ISO traffic (for example, IS-IS) arrives with or be sent with 1 to 3 zero pads inserted after the protocol header as per RFC 1377.
- MPLS Network Control Protocol (MPLSCP): No options are currently available for this
  protocol setup.

# IPv6 Interface Identifiers (IIDs)

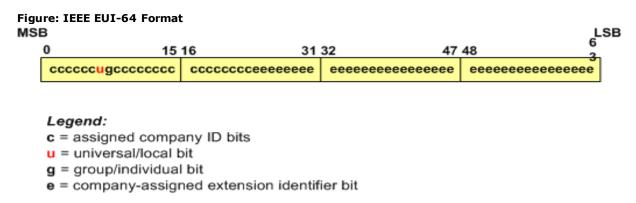
IIDs comprise part of an IPv6 address, as shown in the following figure for a link-local IPv6 address.

The IPv6 Interface Identifier is equivalent to EUI-64 Id in the Protocol Interfaces window.

Figure: IPv6 Address Format Link-Local Address
10 bits 54 bits 64 bits

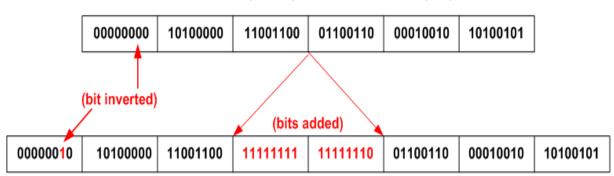
1111111010 0 Interface ID

The IPv6 Interface Identifier is derived from the 48-bit IEEE 802 MAC address or the 64-bit IEEE EUI-64 identifier. The EUI-64 is the extended unique identifier formed from the 24-bit company ID assigned by the IEEE Registration Authority, plus a 40-bit company-assigned extension identifier, as shown in the following figure.



To create the Modified EUI-64 Interface Identifier, the value of the universal/local bit is inverted from `0' (which indicates global scope in the company ID) to `1' (which indicates global scope in the IPv6 Identifier). For Ethernet, the 48-bit MAC address may be encapsulated to form the IPv6 Identifier. In this case, two bytes `FF FE' are inserted between the company ID and the vendor-supplied ID, and the universal/local bit is set to `1' to indicate global scope. An example of an Interface Identifier based on a MAC address is shown in the following figure.

# Example Encapsulated MAC in IPv6 Interface Identifier MAC Address (48 bits) = 00 A0 CC 66 12 A5 (hex)



Interface Identifier (64 bits) = 02 A0 CC FF FE 66 12 A5 (hex)

#### **Retry Parameters**

During the process of negotiation, the port uses three Retry parameters. RFC 1661 specifies the interpretation for all of the parameters.

#### **HDLC**

Both standard and Cisco proprietary forms of HDLC (High-level Data Link Control) are supported.

## **Frame Relay**

Packets may be wrapped in frame relay headers. The DLCI (Data Link Connection Identifier) may be set to a fixed value or varied algorithmically.

#### **DSCP Differentiated Services Code Point**

Differentiated Services (DiffServ) is a model in which traffic is treated by intermediate systems with relative priorities based on the type of services (ToS) field. Defined in RFC 2474 and RFC 2475, the DiffServ standard supersedes the original specification for defining packet priority described in RFC 791. DiffServ increases the number of definable priority levels by reallocating bits of an IP packet for priority marking.

The DiffServ architecture defines the DiffServ (DS) field, which supersedes the ToS field in IPv4 to make Per-Hop Behavior (PHB) decisions about packet classification and traffic conditioning functions, such as metering, marking, shaping, and policing.

Based on DSCP or IP precedence, traffic can be put into a particular service class. Packets within a service class are treated the same way.

The six most significant bits of the DiffServ field are called the Differential Services Code Point (DSCP).

The DiffServ fields in the packet are organized as shown in the following figure. These fields replace the TOS fields in the IP packet header.

Figure: DiffServ Fields

 .94.0. 2								
DS5	DS4	DS3	DS2	DS1	DS0	ECN	ECN	

The DiffServ standard utilizes the same precedence bits (the most significant bits are DS5, DS4, and DS3) as TOS for priority setting, but further clarifies the definitions, offering finer granularity through the use of the next three bits in the DSCP. DiffServ reorganizes and renames the precedence levels (still defined by the three most significant bits of the DSCP) into these categories (the levels are explained in greater detail in this document). The following table shows the eight categories.

**DSCP** Categories

Precedence Level	Description
7	Stays the same (link layer and routing protocol keep alive)
6	Stays the same (used for IP routing protocols)
5	Express Forwarding (EF)
4	Class 4
3	Class 3
2	Class 2

Precedence Level	Description
1	Class 1
0	Best Effort

With this system, a device prioritizes traffic by class first. Then it differentiates and prioritizes same-class traffic, taking the drop probability into account.

The DiffServ standard does not specify a precise definition of `low,' `medium,' and `high' drop probability. Not all devices recognize the DiffServ (DS2 and DS1) settings; and even when these settings are recognized, they do not necessarily trigger the same PHB forwarding action at each network node. Each node implements its own response based on how it is configured.

Assured Forwarding (AF) PHB group is a means for a provider DS domain to offer different levels of forwarding assurances for IP packets received from a customer DS domain. Four AF classes are defined, where each AF class is in each DS node allocated a certain amount of forwarding resources (buffer space and bandwidth).

Classes 1 to 4 are referred to as AF classes. The following table illustrates the DSCP coding for specifying the AF class with the probability. Bits DS5, DS4, and DS3 define the class, while bits DS2 and DS1 specify the drop probability. Bit DS0 is always zero.

Drop Precedence for Classes

Drop	Class 1	Class 2	Class 3	Class 4
	001010	010010	011010	100010
Low	AF11	AF21	AF31	AF41
	DSCP 10	DSCP 18	DSCP 26	DSCP 34
	001100	010100	011100	100100
Medium	AF12	AF 22	AF32	AF42
	DSCP 12	DSCP 20	DSCP 28	DSCP 36
	001110	010110	011110	100110
High	AF13	AF23	AF33	AF43
	DSCP 14	DSCP 22	DSCP 30	DSCP 38

#### **ATM**

The ATM load module enables high performance testing of routers and broadband aggregation devices such as DSLAMs and PPPoE termination systems.

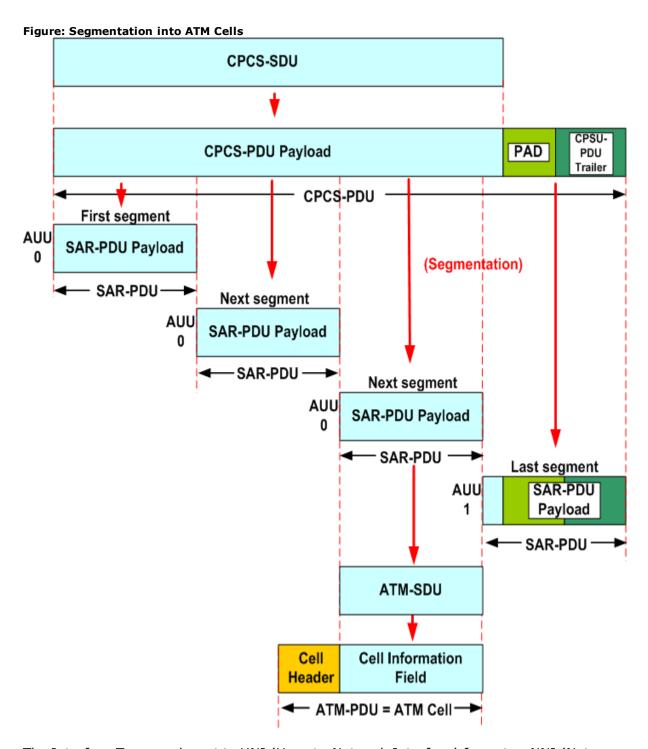
The ATM module is provided with various feature combinations:

- Interfaces: pluggable PHYs:
  - 1310nm multimode optics with dual -SC connectors
  - SFP socket
- Speeds: OC3 and OC12

- Encapsulations:
  - LLC/SNAP
  - LLC/NLPID
  - LLC Bridged Ethernet
  - LLC Bridged Ethernet without FCS
  - VC Mux Routed
  - VC Mux Bridged Ethernet
  - VC Mux Bridged Ethernet without FCS
- · Multiple independent data streams

ATM is a point-to-point, connection-oriented protocol that carries traffic over `virtual connections/circuits' (VCs), in contrast to Ethernet connectionless LAN traffic. ATM traffic is segmented into 53-byte cells (with a 48-byte payload), and allows traffic from different Virtual Circuits to be interleaved (multiplexed). Ixia's ATM module allows up to 4096 transmit streams per port, shared across up to 15 interleaved VCs.

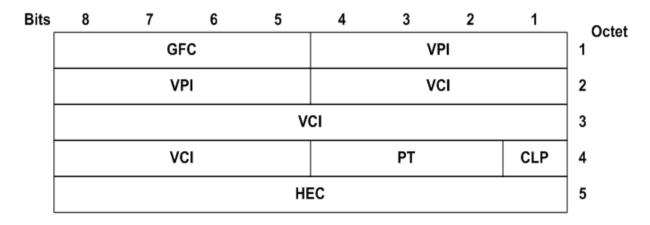
To allow the use of a larger, more convenient payload size, such as that for Ethernet frames, ATM Adaptation Layer 5 (AAL5) was developed. It is defined in ITU-T Recommendation I.363.5, and applies to the Broadband Integrated Services Digital Network (B-ISDN). It maps the ATM layer to higher layers. The Common Part Convergence Sublayer-Service Data Unit (CPSU-SDU) described in this document can be considered an IP or Ethernet packet. The entire CPSU-PDU (CPCS-SDU plus PAD and trailer) is segmented into sections which are sent as the payload of ATM cells, as shown in the following figure, based on ITU-T I.363.5.



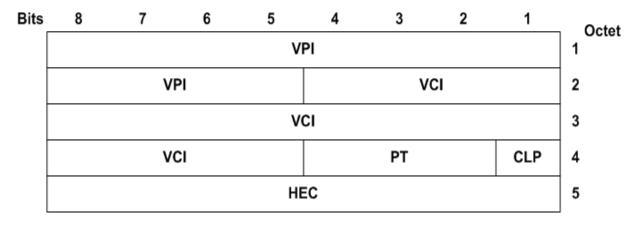
The Interface Type can be set to UNI (User-to-Network Interface) format or NNI (Network-to-Node Interface aka Network-to-Network Interface) format. The 5-byte ATM cell header is different for each of the two interfaces, as shown in the following figure.

Figure: ATM Cell Header for UNI and NNI

### **UNI Header Structure**



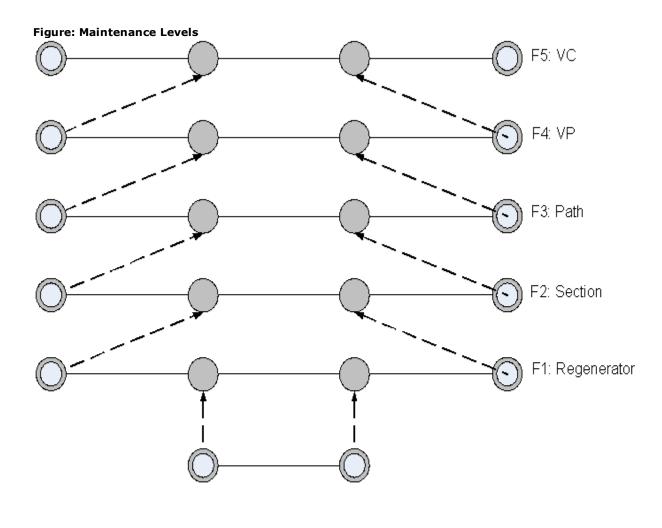
## **NNI Header Structure**



#### **ATM OAM Cells**

OAM cells are used for operation, administration, and maintenance of ATM networks. They operate on ATM's physical layer and are not recognized by higher layers. Operation, Administration, and Maintenance (OAM) performs standard loopback (end-to-end or segment) and fault detection and notification Alarm Indication Signal (AIS) and Remote Defect Identification (RDI) for each connection. It also maintains a group of timers for the OAM functions. When there is an OAM state change such as loopback failure, OAM software notifies the connection management software.

The ITU-T considers an ATM network to consist of five flow levels. These levels are illustrated in the following figure.



Connecting Point of the Corresponding Level

End Point of the Corresponding Level

The lower three flow levels are specific to the nature of the physical connection. The ITU-T recommendation briefly describes the relationship between the physical layer OAM capabilities and the ATM layer OAM.

From an ATM viewpoint, the most important flows are known as the F4 and F5 flows. The F4 flow is at the virtual path (VP) level. The F5 flow is at the virtual channel (VC) level. When OAM is enabled on an F4 or F5 flow, special OAM cells are inserted into the user traffic.

Four types of OAM cells are defined to support the management of VP/VC connections:

- Fault Management OAM cells. These OAM cells are used to indicate failure conditions. They can be used to indicate a discontinuity in VP/VC connection or may be used to perform checks on connections to isolate problems.
- Performance Management OAM cells. These cells are used to monitor performance (QoS) parameters such as cell block ratio, cell loss ratio and incorrectly inserted cells on VP/VC connections.

- Activation-deactivation OAM cells. These OAM cells are used to activate and deactivate the generation and processing of OAM cells, specifically continuity check (CC) and performance management (PM) cells.
- System management OAM cells. These OAM cells can be used to maintain and control various functions between end-user equipment. Their content is not specified by I.610, and they are limited to end-to-end flows.

The general format of an OAM cell is shown in the following figure.

#### OAM Cell Format

Header 5 bytes	OAM Type 4 bits	Function Type 4 bits	Function Specific Field 45 bytes	Reserved 6 bits	EDC CRC 10 bits
-------------------	-----------------------	----------------------------	--	--------------------	-----------------------

The header indicates which VCC or VPC an OAM cell belongs to. The cell payload is divided into five fields. The OAM-type and Function-type fields are used to distinguish the type of OAM cell. The Function Specific field contains information pertinent to that cell type. A 10 bit Cyclic Redundancy Check (CRC) is at the end of all OAM cells. This error detection code is used to ensure that management systems do not make erroneous decisions based on corrupted OAM cell information.

Ixia ATM modules allows to configure Fault Management and Activation/Deactivation OAM Cells.

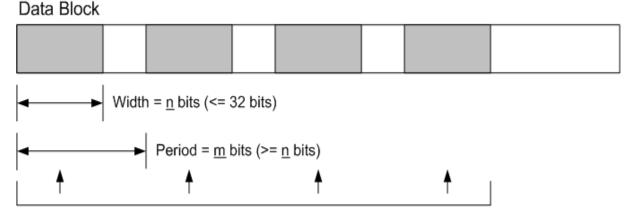
#### **BERT**

Bit Error Rate Test (BERT) load modules are packaged as both an option to OC48, POS, and 10GE load modules and as BERT-only load modules. As opposed to all other types of testing performed by Ixia hardware and software, BERT tests operate at the physical layer, also referred to as OSI Layer 1. POS frames are constructed using specific pseudorandom patterns, with or without inserted errors. The receive circuitry locks on to the received pattern and checks for errors in those patterns.

Both unframed and framed BERT testing is available. Framed testing can be performed in both concatenated and channelized modes with some load modules.

The patterns inserted within the POS frames are based on the ITU-T 0.151 specification. They consist of repeatable, pseudo-random data patterns of different bit-lengths which are designed to test error and jitter conditions. Other constant and user-defined patterns may also be applied. Furthermore, you may control the addition of deliberate errors to the data pattern. The inserted errors are limited to 32-bits in length and may be interspersed with non-errored patterns and repeated for a count. This is illustrated in the following figure. In the figure, an error pattern of  $\underline{n}$  bits occurs every  $\underline{m}$  bits for a count of 4. This error is inserted at the beginning of each POS data block within a frame.

### Figure: BERT Inserted Error Pattern



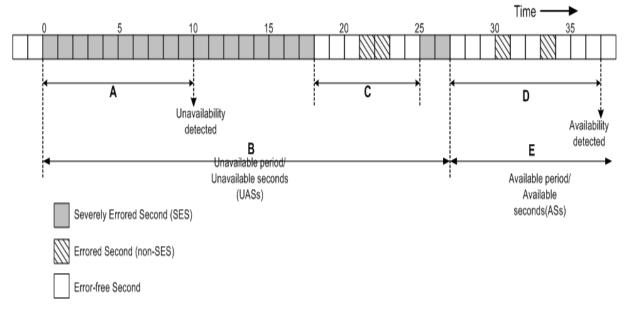
Count = 4

Errors in received BERT traffic are visible through the measured statistics, which are based on readings at one-second intervals. The statistics related to BERT are described in the *Available Statistics* appendix associated with the *Ixia Hardware Guide* and some other manuals.

### Available/Unavailable Seconds

Reception of POS signals can be divided into two types of periods, depending on the current state `Available' or `Unavailable,' as shown in the following figure. The seconds occurring during an unavailable period are termed Unavailable Seconds (UAS); those occurring during an available period are termed Available Seconds (AS).

Figure: BERT Unavailable/Available Periods



These periods are defined by the error condition of the data stream. When 10 consecutive SESs (A in the figure) are received, the receiving interface triggers an Unavailable Period. The period remains in the Unavailable state (B in the figure), until a string of 10 consecutive non-SESs is received (D in the figure), and the beginning of the Available state is triggered. The string of consecutive non-SESs in C in the figure was less than 10 seconds, which was insufficient to trigger a change to the Available state.

# **Port Transmit Capabilities**

The Ixia module ports format data to be transmitted in a hierarchy of structures:

- Streams and Flows-A set of related packet bursts
  - Bursts and the Inter-Burst Gap (IBG)-A repetition of packets
    - Packets and the Inter-Packet Gap (IPG)-Individual packets/frames

Timing of transmitted data is performed by the use of inter-stream, -burst, and -packet gaps. Ethernet modules use all three types of gaps, programmed to the resolution of their internal clocks. POS modules gaps are implemented by use of empty frames and the resolution of the gap is limited to a multiple of such frames. ATM modules do not use interstream or inter-packet gaps, and instead control the transmission rate through empty frames. The three types of gaps are discussed in:

- Streams and the Inter-Stream Gap (ISG)
- Bursts and the Inter-Burst Gap (IBG)
- Packets and the Inter-Packet Gap (IPG)

The percentage of line rate usage for ports is determined using the following formula:

```
(packet size + 12 byte IPG + requested preamble) / (packet size + requested IPG + requested preamble) * 100
```

### Streams and Flows

The Ixia system uses sophisticated models for the programming of data to be transmitted. There are two general modes of scheduling data packets for transmission:

- Sequential: The first configured stream in a set of streams is transmitted completely before the next one is sent, and so on, until all of the configured streams have been transmitted. Two types are available:
  - Packet Streams
  - Packet Flows (available on certain modules)
- Interleaved: The individual packets in the streams are multiplexed into a single stream, such that the total packet rate is the sum of the packet rates for each of the streams. One type is available:
  - Advanced Streams (Advanced Stream Scheduler feature)

ATM modules support up to 15 independent stream queues, each of which may contain multiple streams. Up to 4096 total streams may be defined. See <u>Stream Queues</u>.

#### **Packet Streams**

This sequential transmission model is supported by the Ixia load modules, where dedicated hardware can be used to generate up to 255 *Packet Streams* `on-the-fly,' with each stream consisting of up to 16 million bursts of up to 16 million packets each. Transmission of the entire set of packet streams may be repeated continuously for an indefinite period, or repeated only for a user-specified count. The variability of the data within the packets is necessarily generated algorithmically by the hardware transmit engine.

NOTE

Streams consisting of only one packet are not transmited at wire speed. Also, streams set to random frame size generation does not have accurate IP checksum information. See the *IxExplorer Users Guide*, Chapter 4, *Stream and Flow Control*, for more information on creating streams.

#### **Packet Flows**

A second sequential data transmission model is supported by software for any Ixia port which supports PacketFlows. An individual packet flow can consist of from 1 to 15,872 packets. For packet flows consisting of only one unique packet each, a maximum of 15,872 individual flows can be transmitted. Because the packets in each of the packet flows is created by the software, including <a href="User Defined Fields">User Defined Fields</a> (UDF) and checksums, and then stored in memory in advance of data transmission, there can be more unique types of packets than is possible with streams. Continuous transmission cannot be selected for flows, but by using a return loop, the flows can be retransmitted for a user-defined count.

Packet streams, which can contain larger amounts of data, are based on only one packet configuration per stream. In contrast, many packet flows can be configured for a single data transmission, where each flow consists of packets with a configuration unique to that flow. Some load modules permit saving/loading of packet flows.

### **Advanced Streams**

A third type of stream configuration is called *Advanced Streams*, which involves interleaving of all defined streams for a port into a single, multiplexed stream. Each stream is assigned a percentage of the maximum rate. The frames of the streams are multiplexed so that each stream's long-term percentage of the total transmitted data rate is as assigned. When the sum of all of the streams is less than 100% of the data rate, idle bytes are automatically inserted into the multiplexed stream, as appropriate.

#### **Example of Advanced Stream Generation** Advanced Streams Example Stream Advanced Stream = 100% of Max. Rate Stream 2 Max. Rate Stream 3 50% of Max. Rate Example Conditions: 1 - All frames are the same size Multiplex all 2 - 100% of max rate is utilized streams on port 3 - Continuous packet mode for all Note: streams Stream Number can be used as PGID for Sequence Checking

## **Stream Queues**

Stream queues allow standard packet streams to be grouped together. Up to 15 stream queues may be defined, each containing any number of streams so long as the total number of streams in all queues for a port does not exceed 4,096. Each queue is assigned a percentage of the total and traffic is mixed as in advanced streams. Each queue may

represent any number of VPI/VCI pairs; the VPI/VCI pairs may also be generated algorithmically.

## **Basic Stream Operation**

When multiple transmit modes are available, the *transmit mode* for each port must be set by you to indicate whether it uses streams, flows, or advanced stream scheduling. The programming of sequential streams or flows is according to the same programming model, with a few exceptions related to continuous bursts of packets. Since the model is identical in both cases, we refer to both streams and flows as `streams' while discussing programming.

There are three basic types of sequential streams:

- Continuous Packet: A continuous stream of packets. The packets are not necessarily identical; their contents may vary significantly. (Not available for packet flows.)
- Continuous Burst: A set of counted packets within a burst; the burst is repeated continuously. (Not available for packet flows.)
- Counted Burst (non-continuous): A user-specified number of bursts per stream, where each burst contains a counted number of packets.

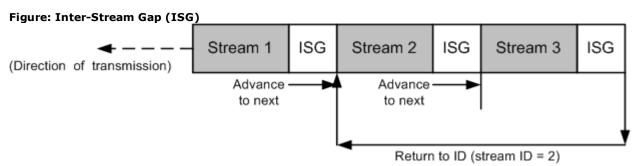
Each non-continuous stream is related to the next stream by one of four modes:

- Stop after this stream: Data transmission stops after the completion of the current stream. (For example, after transmission of a stream consisting of 10 bursts of 100 packets each.)
- Advance to Next: Data transmission continues on to the next stream after the completion of the current stream.
- Return to ID: After the completion of the current stream, a previous stream (designated by its Stream ID) is retransmitted once, and then transmission stops.
- Return to ID for Count: After the completion of the current stream, a previous stream (designated by its Stream ID) is retransmitted for the user-specified number of times (count), and then transmission stops.

If a Continuous Packet or Continuous Burst stream is used, it becomes the last stream to be applied and data transmission continues until a Stop Transmit operation is performed.

# Streams and the Inter-Stream Gap (ISG)

A programmable Inter-Stream Gap (ISG) can be applied after each stream, as shown in the following figure.

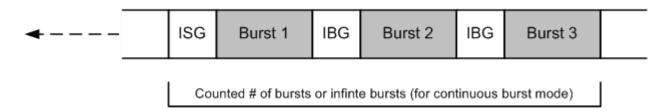


The size and resolution of the Inter-Stream Gaps depends on the particular Ixia module in use. For all modules except 10 Gigabit Ethernet modules, the stream uses the parameters set in the following stream. In 10 Gigabit Ethernet modules, it uses the parameters set in the preceding stream. There are no ISGs before Advanced Scheduler Streams. For non-Ethernet modules, the ISG is implemented by use of empty frames and the resolution of the ISG is limited to a multiple of such frames.

# Bursts and the Inter-Burst Gap (IBG)

Bursts are sets of a specified number of packets, separated by programmed gaps between the sets. For Ethernet modules, Inter-Burst Gaps (IBG) are inserted between the sets. For POS modules, bursts of packets are separated by Burst Gaps. ATM modules do not insert IBGs. The size and resolution of these gaps depends on the type of Ixia load module in use. The placement of Inter-Burst Gaps is shown in the following figure.

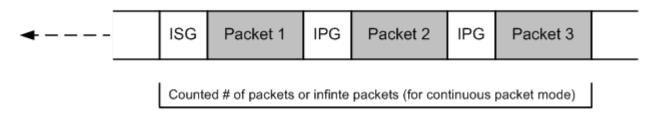
Figure: Inter-Burst Gap (IBG)/Burst Gap



# Packets and the Inter-Packet Gap (IPG)

Streams may contain a counted number of frames, or a continuous set of frames when Continuous Packet mode is used. Frames are separated by programmable Inter-Packet Gaps (IPGs), sometimes referred to as Inter-Frame Gaps (IFGs). The size and resolution of the Inter-Packet Gaps depends on the particular Ixia module in use. For non-Ethernet modules, the ISG is implemented by use of empty frames and the resolution of the IPG is limited to a multiple of such frames. ATM modules do not insert IBGs. The placement of Inter-Packet Gaps is shown in the following figure.

Figure: Inter-Packet Gap (IPG)



### **Frame Data**

The contents of every frame and packet are programmable in terms of structure and data content. The programmable fields are:

- Preamble or Header contents
  - Ethernet modules: Preamble Size: The size and resolution depends on the particular Ixia load module used.

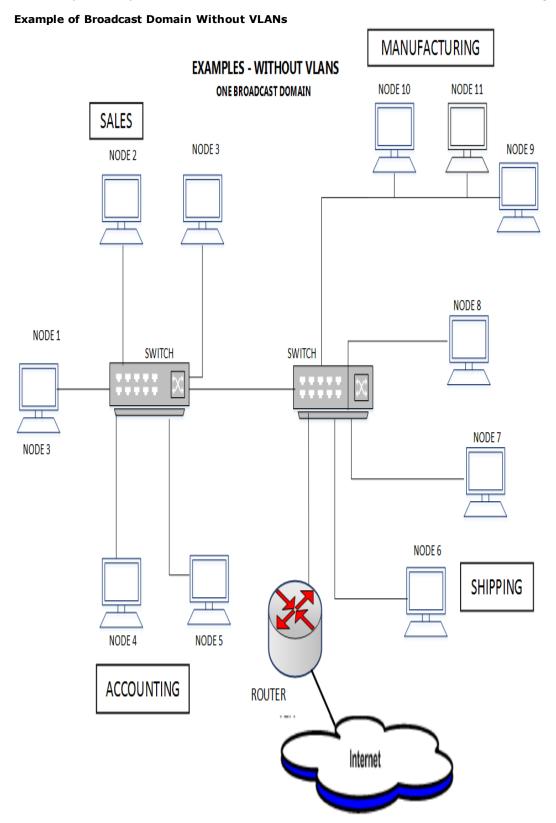
- POS modules: Minimum Flag and Header contents: The minimum number of flag fields to precede the packet within the POS frame and the type of encapsulation/signalling.
- ATM modules: Header contents.
- Frame size: The size and resolution depends on the particular Ixia load module used.
- Destination and Source MAC Addresses (Ethernet only): Allows the MAC addresses to be set to constants, vary randomly, or increment/decrement using a mask.
- Data generators: Five different data generators are available. These generators are listed as follows, in order of increasing priority (from top to bottom). The values from generators located lower in this list override data from those higher in the list.
  - Protocol-related data: Formatted to correspond to particular data link, transport, and protocol conventions.
    - Data link layer controls for Ethernet allow for Ethernet II/SNAP, 802.3
       Raw and 802.3 IPX formatting, with support for VLANs, MPLS, and Ciscoproprietary ISL. VLANs are described in Virtual LANs.
    - Protocol-specific data for formatting IPv4, IPv6, and IPX packets (such as Source and Destination IP addresses), as well as Layer 4 transport protocol headers (TCP/IP, IGMP, and so on) are also supported. IPv4/IPv6 and IPv6/IPv4 tunneling is also supported.
    - IP Source and Destination addresses may be incremented or decremented using a network mask.
  - Data Patterns: Can be one of three types: predefined patterns up to 8K bytes in length, randomly generated data, algorithmically generated data, industry standard (such as CJPAT and CRPAT) or user-specified.
  - User Defined Fields (UDFs): A number of 32-bit counters. For some modules the counters can each be flexibly configured as multiple 8, 16, 24, and 32-bit counters. Each counter may independently increment or decrement using a mask. These are further described in User Defined Fields (UDF).
  - Frame Identity Record (FIR): An identity record stored at the end of the packet. The information is very useful for determining the source of transmitted data found in capture buffers.
  - Frame Check Sequence (FCS): The checksum for a packet may be omitted, formatted correctly, or have deliberate errors inserted. Deliberate errors include incorrect checksum, dribble errors, and alignment errors.

### Virtual LANs

Virtual LANs (VLANs) are defined in IEEE 802.1Q, and can be used to create subdomains without the use of IP subnets. The IEEE 802.1Q specification uses the explicit VLAN tagging method and port-based VLAN membership. Explicit tagging involves the insertion of a tag header in the frame by the first switch that the frame encounters. This tag header indicates which VLAN the packet belongs to. A frame can belong to only one VLAN.

VLAN tag headers are inserted into the frames, following the source MAC address. A maximum of 4094 VLANs can be supported, based on the length of the 12-bit VLAN ID. The VID value is used to map the frame into a specific VLAN. VLAN IDs 0 and FFF are reserved. VID = 0 indicates the null VLAN ID, which means that the tag header contains only user priority information.

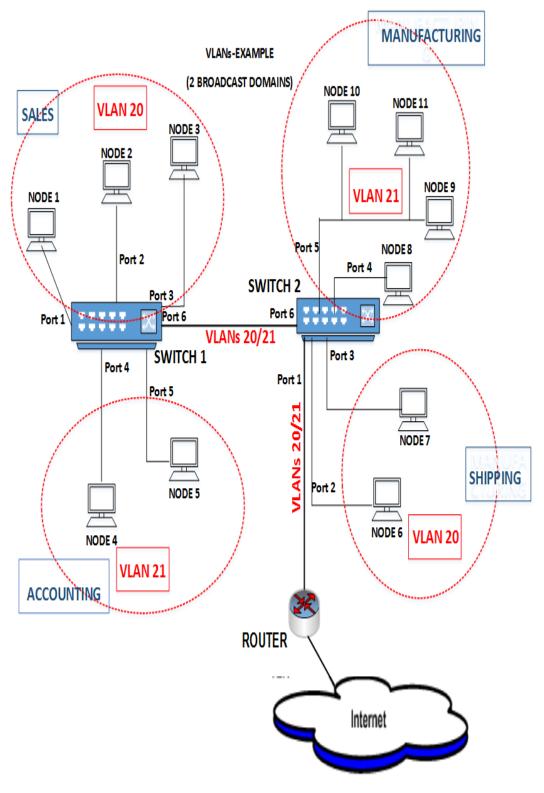
An example of Layer 2 broadcast domain without VLANs is shown in the following figure.



In the example above, a company has four departments (Sales, and so forth) which are in one switched broadcast domain. Broadcasts are flooded to all of the devices in the domain. A router sends/receives Internet traffic. In the figure below, the departments have been

grouped into two separate VLANs, cutting down on the amount of broadcast traffic. For example, VLAN 20 contains Ports 1, 2, 3, and 6 on Switch 1, and Ports 1, 2, 3, and 6 on Switch 2. VLAN 21 contains Ports 4, 5, and 6 on Switch 1, and Ports 1, 4, 5, and 6 on Switch 2

#### **Example of VLANs**



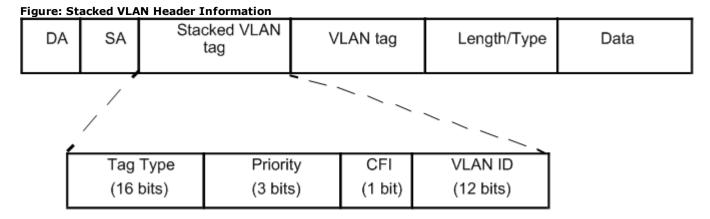
With the new network design, switch ports and attached nodes are assigned to VLANs. Frames are tagged with their VLAN ID as they leave the switch, en route to the second switch. The VLAN ID indicates to the second switch which ports to send the frame to. The VLAN tag is removed as the frame exits a port belonging to that VLAN, on its way to the attached node. With VLANs, bandwidth is conserved, and security is improved. Communication between the VLANs is handled by the existing Layer 3 router.

# Stacked VLANs (Q in Q)

VLAN Stacking refers to a mechanism where one VLAN (Virtual Local Area Network) may be encapsulated within another VLAN. This allows a carrier to partition the network among several networks, while allowing each network to still utilize VLANs to their full extent. Without VLAN stacking, if one network provisioned an end user into `VLAN 1,' and another network provisioned one of their end users into `VLAN 1,' the two end users would be able to see each other on the network.

VLAN stacking solves this problem by embedding each instance of the 802.1Q VLAN protocol into a second tier of VLANs. The first network is assigned a `Backbone VLAN,' and within that Backbone VLAN a unique instance of 802.1Q VLAN tags may be used to provide that network with up to 4096 VLAN identifiers. The second network is assigned a different Backbone VLAN, within which another unique instance of 802.1Q VLAN tags is available.

The following figure demonstrates an example packet of a stacked VLAN.



# **User Defined Fields (UDF)**

Seven different types of UDFs are available, depending on the load module type. The types of UDFs that are supported by particular port types is detailed in <a href="Platform and Reference">Platform and Reference</a>
<a href="Overview">Overview</a>. Not all features supported by a port type are available on all UDFs; whether a particular UDF type is supported on a particular UDF can be ascertained by looking at the UDF with IxExplorer or programatically using the Tcl API. These types are:

- Counter Mode UDF
- Random Mode UDF
- Value List Mode UDF
- Range List Mode UDF
- Nested Counter Mode UDF
- IPv4 Mode UDF
- Table Mode UDF

Some features are common across all UDFs:

- Counter Type: The size of the counter is available in two modes:
  - A single counter with a length of 8, 16, 24 or 32 bits, or
  - A 32-bit value that may be divided into one to four 8 to 32 bit counters in any order. For example, 8x8x8x8 (four 8-bit counters), 8x16 (an 8-bit counter followed by a 16 bit counter), or 24x8 (a 24-bit counter followed by an 8-bit counter). In this case, each of the up to four counters may be independently controlled as described in Counter Mode UDF.
- Offset: The offset from the beginning of the packet to the start of the counter.
- Init val: The initial value given to the counter.
- Cascade: Sets the initial value for the counter, in one of two ways:
  - From the last value for this stream: The counter continues from the last value generated by this UDF for this stream. The first value for the counter is set from the *Init val* setting. This type of cascade is sometimes referred to as *Cascade From Self*.
  - From the last value on the previous cascade stream: The counter continues from the last value generated by the last executed stream using this UDF that is also in this cascade mode. The first value for the first UDF is set from the *Init val* setting. This type of cascade is sometimes referred to as *Cascade From Previous Stream*.
- Masking: The bit masking operation allows certain bits to maintain constant values, while varying other values. In the IxExplorer GUI, a bit mask is represented as a string of characters, one character per counter bit. For example, a possible Bit Mask setting for an 8-bit counter might be:

#### 0110XXXX

The `0's and `1's represent fixed values after the mask value, while the `X's are bits which vary as a result of the increment, decrement or random value option.

In the TCL/C++ APIs, the *Bit Mask* value is split into two variables:

- maskSelect: Indicates which bits of the counter are fixed in value, and
- maskval: Indicates the fixed value for any of the bits set in maskSelect.

In all of the UDF figures, the generated counter value is shaded. The parameters are shown in ovals (blue in the online version).

### **Counter Mode UDF**

The counter mode UDF features the ability of a counter (up to four on some load modules) to count up or down or to use random values. Certain bits of the counter may be held at fixed values using a mask. The parameters that affect the counter's operation are shown in the following table.

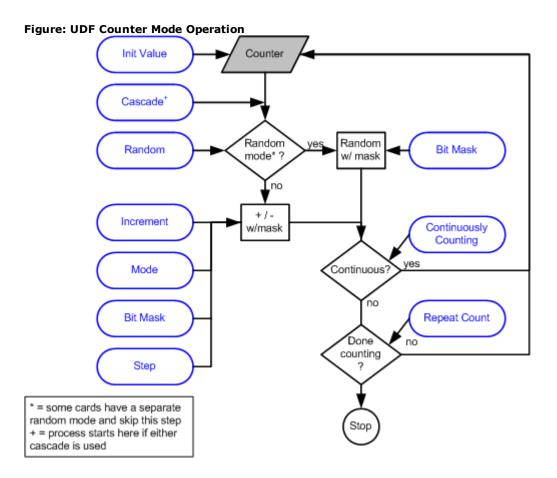
#### Counter Mode UDF Parameters

IxExplorer Label	Tcl API Variables
Counter Type	countertype

IxExplorer Label	Tcl API Variables
Offset	offset
Init Value	initval
Set from Init ValueContinue from last value for this streamCas- cade continue	cas- cadeTypeenableCascade
Random*	random
Continuously Counting	continuousCount
Step	step
Repeat Count	repeat
Mode	updown
Bit Mask	maskvalmaskselect

<sup>\*</sup> some card types include random mode as part of the counter mode and others use them as a separate mode.

In the TCL APIs the value of the *counterMode* variable in the *udf* command should be set to udfCounterMode (0). The operation of counter mode is described in the flowchart shown in the following figure.



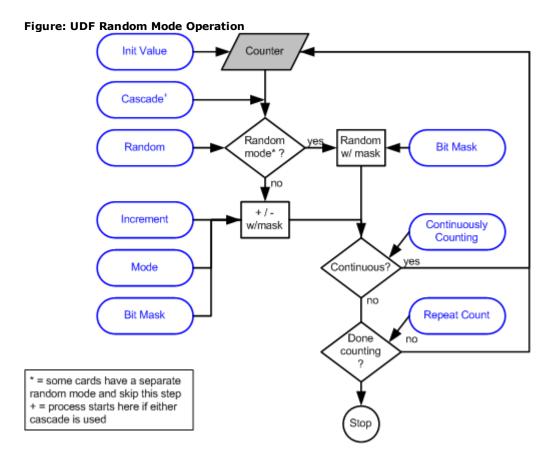
## **Random Mode UDF**

The random mode UDF features a counter whose values are randomly generated, but may be masked. Cascading modes do not apply to random mode UDFs. The parameters that affect the counter's operation are shown in the following table.

Random Mode UDF Parameters

IxExplorer Label	Tcl API Vari- ables
Offset	offset
Bit Mask	maskvalmaskselect

In the TCL APIs the value of the *counterMode* variable in the udf command should be set to udfRandomMode (1). The operation of random mode is described in the flowchart shown in the following figure.



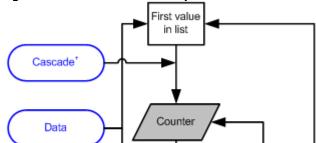
## Value List Mode UDF

The value list mode UDF features a counter whose values successively retrieved from a table of values. Cascading modes do not apply to value list mode UDFs. The parameters that affect the counter's operation are shown in the following table.

Value List Mode UDF Parameters

value List Mode obt Talameters				
IxExplorer Label	Ecl API Variables			
Offset	offset			
Counter Type	countertype			
Data	valueList			
Set from Init ValueContinu- e from last value for this stream	cas- cadeTypeenableCascade			

In the TCL APIs the value of the *counterMode* variable in the *udf* command should be set to *udfValueListMode* (2). The operation of value list mode is described in the flowchart shown in the following figure.



Next value

in list

Figure: UDF Value List Mode Operation

# Range List Mode UDF

+ = process starts

here if cascade is

used

The range list mode UDF features a counter whose values are generated from a list of value ranges. Each range has an initial value, repeat count, and step value. Cascading modes do not apply to range list mode UDFs. The parameters that affect the counter's operation are shown in the following table.

ind of

Range List Mode UDF Parameters

IxExplorer Label	Tcl API Variables
Offset	offset
Counter Type	countertype
Init Value	initval
Repeat Count	repeat
Step	step
Set from Init ValueContinue from last value for this stream	cascadeTypeenableCascade

In the TCL APIs the value of the *counterMode* variable in the *udf* command should be set to *udfRangeListMode* (4). The *initval*, *repeat*, and *step* values are added into the *udf* command by the *addRange* sub-command. The operation of range list mode is described in the flowchart shown in the following figure.

First range in list Init value for range Counter Cascade<sup>1</sup> More epeat count Step repeat count no + = process starts End of no here if cascade is list used yes Next range in list

#### Figure: UDF Range List Mode Operation

## **Nested Counter Mode UDF**

The nested counter mode UDF features a counter whose values are generated from three nested loops:

- 1. A given value may be repeated a number of times.
- 2. That value is incremented and step 1 is repeated for a count. This is called the *inner* loop.
- 3. That value is incremented and steps 1 and 2 repeated continuously for a count. This is called the outer loop.

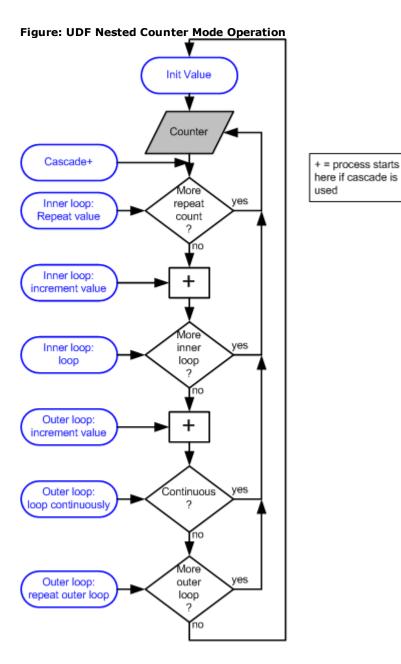
The parameters that affect the nested counter's operation are shown in the following table.

Nested Counter Mode UDF Para-

IxExplorer Label	Tcl API Variables
Offset	offset
Counter Type	countertype
Init Value	initval
Inner Loop: Repeat value	innerRepeat
Inner Loop: increment value	innerStep

IxExplorer Label	Tcl API Variables
Inner Loop:	innerLoop
Outer Loop:in- crement value	step
Outer Loop: loop con- tinuously	continuousCount
Outer Loop: repeat outer loop	repeat
Set from Init ValueContinue from last value for this stream	cas- cadeTypeenableCascade

In the TCL APIs the value of the *counterMode* variable in the *udf* command should be set to *udfNestedCouterMode* (3). The operation of range list mode is described in the flowchart shown in the following figure.



## **IPv4 Mode UDF**

The IPv4 counter mode UDF features a counter designed to be used with IPv4 addresses. The process is:

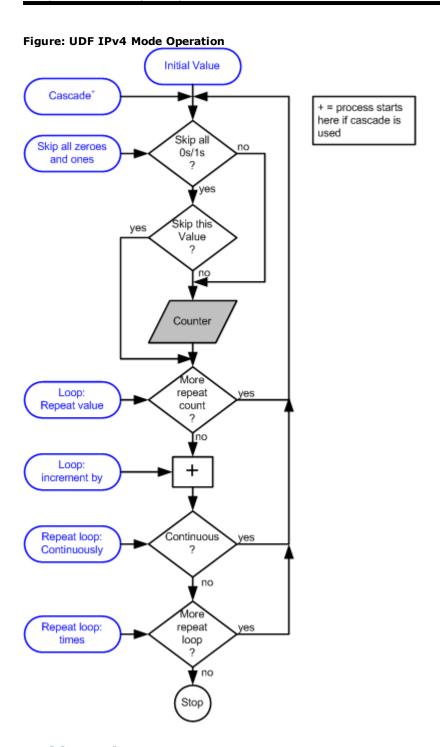
- 1. A given value may be repeated a number of times. Values with all `1's and `0's in a particular part of the value may be skipped so as to avoid broadcast addresses. The number of low order bits to check for `0's and `1's can be set.
- 2. That value is incremented and step 1 is repeated continuously or for a count.

The parameters that affect the counter's operation are shown in the following table.

IPv4 Mode UDF parameters

IxExplorer Label	Icl API Variables
Offset	offset
Counter Type	countertype
Init Value	initval
Loop: Repeat value	innerRepeat
Loop: incre- ment by	innerStep
Repeat Loop: Continuously	continuousCount
Repeat Loop: times	repeat
Skip all zeros and ones	enableSkipZerosAndOnes
masked with	skipMaskBits
Set from Init ValueContinu- e from last value for this stream	cas- cadeTypeenableCascade

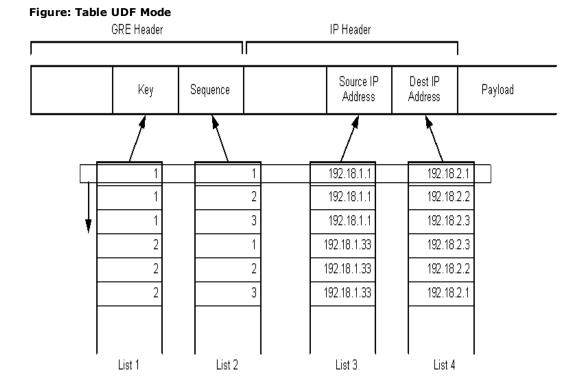
The operation of IPv4 mode is described in the flowchart shown in the following figure.



### **Table Mode UDF**

Table UDFs allows to specify a number of lists of values to be placed at designated offsets within a stream. Each list consists of an Offset, a Size, and a list of values.

The following figure illustrates the basic operation of the Table UDFs using a GRE encapsulated packet as an example. Four of the fields in the packets need to be modified on a packet by packet basis-the key and sequence GRE fields and the source and destination IP addresses in the IP header. The Table UDF provides a means by which lists are developed for each of these fields and the list is associated with an offset and size within the packet. During stream generation, all lists are applied at the same time in lock step.



A Table UDF is applied before, and can be combined with, the standard UDF fields already available on ports. By combining these two features you can model multiple flows using the powerful combination of a value list group for flow identity fields and UDFs for protocol related timestamp/sequence fields.

Table Mode UDF has a limitation compared to the other UDFs. Specifically, Table Mode behaves differently when Random Data payload is enabled for the frame.

Most UDFs are attached to the frame after the Random Data is placed in the frame; the UDFs `overlay'on top of the random data. The Table Mode UDF data, however, is put in the frame *before* the random data. As a result, the payload is random only after the Table UDF.

For example, if a frame has a Table UDF that is 1 byte wide starting at offset 100, random data cannot appear in the payload until byte 101. Thus, the first 100 of these frames would have the same `random' data appear within the first 99 bytes of the payload-for all 100 frames. The data would truly appear random starting at byte 101, after the Table UDF insertion.

This is the same limitation currently for random data packets that have PGID or Data Integrity enabled.

The parameters that affect the counter's operation are shown in the following table.

Table Mode UDF Parameters

IxExplorer Label	Tcl API Vari- ables
Offset	offset
Counter Type	countertype

IxExplorer Label	Tcl API Vari- ables
Init Value	initval
Add Column	addColumn
Add Row	addRow
Clear All Columns	clearColumns
Get First Column	getFirstColumn
Get Next Column	getNextColumn
Clear All Rows	clearRows
Get First Row	getFirstRow
Get Next Row	getNextRow
Export to File	export
Import from File	import

# **Transmit Operations**

The transmit operations may be performed across any set of chassis, cards, and ports specified by you. These operations are described in the following table.

Transmit Operations

Operation	Usage
Start Transmit	Starts the transmission operation on all ports included in the present set of ports. If no transmit operation has been performed yet, or if the last operation was <i>Stop Transmit</i> , then transmission begins with the first stream configured for each port. If a <i>Pause Transmit</i> operation was last performed, then transmission begins at the next packet in the queue for all ports.
Staggered Start Transmit	The same operation is performed as in <i>Start Transmit</i> , except that the start operation is artificially staggered across ports. The time interval between the start of transmission on consecutive ports is in the range of 25-30ms.
Stop Transmit	Stops the transmission operation on all ports included in the present set of ports. A subsequent <i>Start Transmission</i> or <i>Step Stream</i> operation commences from the first stream of each port.
Pause Transmit	Stops the transmission operation on all ports in the present set of ports at the end of transmission of the current packet. A subsequent <i>Start Transmission</i> or <i>Step Stream</i> commences at the beginning of the next packet in the queue on each port.
Step Stream	Causes one packet to be transmitted from each of the ports in the present set of ports.

## **Repeat Last Random Pattern**

The 10 GE LSM module transmit engine has the ability to provide repeatable random values in all its random number generators. This feature allows to run tests with random parameters such as frame size, frame data, and UDF values to rerun the tests with the same set of random data if a problem is found. A check box on the Port Properties transmit tab is used to enable/disable, repeating the last seed used on the port. In addition to the check box, there is a read-only window showing the last 32 bit master seed value used in generating seeds for all random number generators on the port.

# **Port Data Capture Capabilities**

Most ports have an extensive buffer which may be used either to capture the packet data `raw' as it is received, or to categorize it into groups known as Port Groups. Each port must be designated to have a *Receive mode* which is either *Capture* or *Packet Groups*. Packet groups are used in measuring latency.

The start of capture buffering may be triggered by a set of matching conditions applied to the incoming data, or all data may be captured. Packets can be filtered, as well. During capture mode operation, the amount of data saved in the capture buffer can be limited to a user-defined `capture slice' portion of each incoming packet, rather than the entire packet.

Each port's Capture trigger and filter conditions are based on:

- For Ethernet Modules:
  - Data link encapsulation type
  - Destination and source MAC addresses
  - Protocol layer type: such as IP, IPv6, and ARP
  - IPv4 and IPv6 source and destination addresses
  - TCP and UDP port numbers
  - VLAN IDs
- For POS Modules:
  - Use of PPP
  - Protocol layer type: such as IP, IPv6, and ARP
  - IPv4 and IPv6 source and destination addresses
  - TCP and UDP port numbers
- For ATM Modules:
  - VPI and VCI combinations
  - Protocol layer type: such as IP, IPv6, and ARP
  - IPv4 and IPv6 source and destination addresses
  - TCP and UDP port numbers
  - ATM OAM cells
- Data pattern match for the packet, and matching errors such as: Bad CRC, Bad Packet, Alignment Error, and Dribble Error
- Packet sizes within a user-specified range

## **Continuous Versus Trigger Capture**

For some load modules, there are more advanced options provided for setting up data capture operations on a port. These options are set in the receive mode dialog for the port. The available options are described in the following list:

- Continuous Capture. Options are as follows:
  - All packets are captured.
  - All packets which match a user-defined Capture Filter condition are captured.
- Trigger Capture:
  - Capture operation starts **before** a packet matching the user-defined Trigger condition is received. Options are:
    - All packets are captured.
    - No packets are captured.
    - All packets which match a user-defined Capture Filter condition are captured.
  - Capture operation starts after a packet matching the user-defined Trigger condition is met. Options are:
    - All packets are captured.
    - All packets that match a user-defined Capture Filter condition are captured.
    - All packets that match the user-defined Trigger Capture condition are captured.
  - Trigger Position: The slider bar is used to set the position (% transmitted) in the data stream where the Capture Trigger is first applied to incoming packets.

# **Port Capture Operations**

The data capture operations may be performed across any set of chassis, cards, and ports defined by you. These operations are described in the following table.

Capture Operations

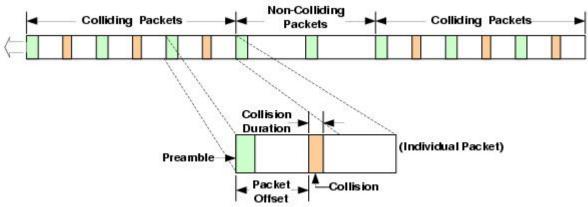
Operation	Usage
Start Capture	Enables data capture on all ports in the set of ports whose receive mode is set to <i>Capture</i> . Packets are not actually captured until the user-specified capture trigger condition is satisfied.
Stop Capture	Stops data capture on all ports in the set of ports.
Start Latency	Initiates latency measurements for all ports in the set of ports whose receive mode is set to <i>Packet Group</i> operation.
Stop Latency	Stops latency measurements on all ports in the set of ports.
Start Collision	Enables generation of forced collisions on received data, for all ports in the set of ports-if this option is selected for the port and enabled. Applies to half-duplex 10/100 Ethernet connections only.
Stop Collision	Stops generation of forced collisions for all ports in the set of ports.

## **Forced Collision Operation**

In addition to normal capture operation, forced collisions can be generated on the receive side of some 10/100/1000 load module ports, but only when the port is in half-duplex mode.

Forced collisions operate by generating `collision' data as information is being received on the incoming port. The `collision' takes the form of a number of nibbles inserted at a user-specified offset within a packet as it is received. A period with a number of consecutive `collisions' is followed by a period with no collisions. This combination of collisions and non-colliding periods can be repeated indefinitely, or repeated for a user-specified number of times. These parameters are shown in the following figure.

**Figure: Forced Collisions** 

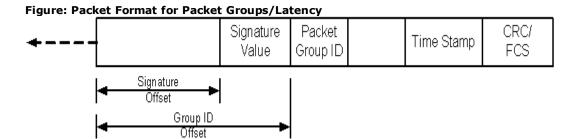


# **Packet Group Operation**

Packet groups are sets of packets which have matching tags, called *Packet Group IDs*. Real-time latency measurements within packet groups depend on coordination between port transmission and port reception. Each transmitted packet must include an inserted 4-byte packet `group signature' field, which triggers the receiving port to look for the packet group ID. This allows the received data to be recognized and categorized into packet groups for latency analysis.

Packet group IDs should be used to group similar packets. For example, packet groups can be used to tag packets connected to individual router ports. Alternatively, packet groups may be used to tag frame sizes. Such groupings allow to measure the latency with respect to different characteristics (for example, router port number or frame size as in the above scenario).

After packet group operation is triggered on the receiving port, the packet group ID-a 2-byte field which immediately follows the signature-is used as an index by the port's receive buffer to store information related to the latency of the packet. When packet group signatures and packet group IDs are included in transmitted data, an additional time stamp is automatically inserted into the packet. The following figure shows the fields within packets which are important for packet grouping and latency analysis.



A special version of packet groups, known as wide packet groups, uses a 4-byte packet group ID, of which only the low order 17 bits are active. A mask may be applied to the matching of the packet group ID. Latency, sequence checking, and first/last timestamps are supported at the same time. Latency over time and data integrity checking are not supported in this mode. Frames must be greater than or equal to 64 bytes.

## **Split Packet Group Operation**

Split PGID allows the 32-bit PGID field used to identify and group packets to be generated from a concatenation of three separate PGID fields. Note that the method for detecting and determining if a packet has a valid signature is no different from standard PGID operation. A valid signature is still required before the concatenated PGID is considered to be valid.

Instead of having one PGID offset value with one mask, you are allowed to enter up to three separate PGID offsets and masks. The split PGID method works with both the standard instrumentation method or the floating instrumentation method, and does not interfere with other features such as time bins and bin by latency.

In addition to having three 16 bit offset values and three 32 bit mask values, the following possibilities are available for the PGID offset:

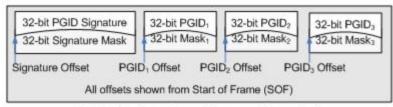
- Offset from Start of Frame (Original starting point for PGIDs)
- Offset from End of Floating Instrumentation Pattern Match
- · Offset from Start of IP
- Offset from Start of Protocol

The definition of the mask is also different when in split PGID mode. In the standard PGID mode, the mask is only used to zero out PGID values and not to change the width of the final PGID. In split PGID mode, the mask is used to reduce the overall width of the PGID value for that region. A value of 1 in mask field indicates the bit is discarded (masked out).

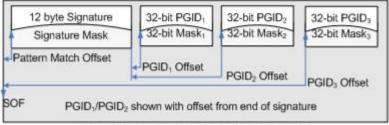
The final 32 bit PGID value used is a concatenation of the values extracted based on the off-set/mask combinations provided for the three PGID regions. The final 32 bit PGID is generated by concatenating the three regions as follows: PGID3, PGID2, and PGID1. If the concatenation of the three regions is not sufficient to fill the 32 bit value, a padding of 0 is used on the remaining leftmost bits.

The following figure demonstrates the three options when employing split PGIDs.

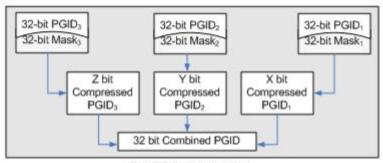
#### Figure: Split PGID Scenarios



Split PGID using traditional signature offset method



Split PGID using floating instrumentation method



Split PGID concatenation

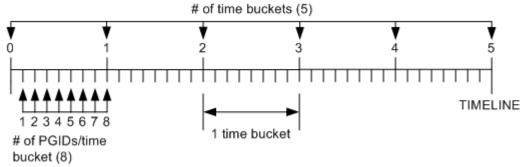
# **Latency/Jitter Measurements**

Latency and Jitter can be measured when packet groups are enabled on a transmitting port and received on a port enabled to receive packet groups. The difference between the received time and the transmitted time held in the packet's time stamp is the measured latency or jitter. The latency is included in a memory cell indexed by the packet group ID. The count of packets received, minimum, maximum, average, and mean latencies are maintained. There are two modes for latency measurement:

- Instantaneous: Latency measured for all received data (continuous). The number of PGID groups available depends on the features being employed on the receive side. The PGID is used as an index into an area of cells and the count/min/max/avg/mean is maintained for each PGID.
- Latency over time: Latency measured for a number of time intervals of equal length, called `time buckets.' The range of cells is divided up over a period of time-for example, for one second intervals over a 30 second period. Each time period (one second in this example) is called a *time bucket*. Within each time bucket, the data for all PGIDs must be stored into a limited number of cells. This is accomplished by grouping a number of PGIDs together. The grouping is called the `# of PGIDs/Time Bucket'. The figure below demonstrates the relationship between the time buckets and PGIDs in an example. The minimum size time bucket varies by port type, but the

size set should be reasonable for the transmission speed of the port-certainly no shorter than 1 microsecond.

Figure: Multiple Latency Time Measurements-Example



Total # of PGIDs = 8 x 40 = 40 PGIDs

The timeline is equally divided into a # of Time Buckets, each of which is **one**Time Bucket Duration in length. A time bucket duration can range anywhere from nanoseconds to hours, depending on the user configuration.

The maximum number of time buckets that can be handled is determined by the number of PGIDs in each bucket.

Four types of timing measurements are available, corresponding to the type of device under test:

- Cut-Through: For use with switches and other devices that operate using packet header information. The time interval between the first data bit out of the Ixia transmit port and the first data bit received by the Ixia receive port is measured. The first data bit received on Ethernet links (10/100 and Gigabit modules) is the start of the MAC DA field. For Packet over SONET links, the first bit received is the start of the IP header.
- Store and Forward: For use with routers and other devices that operate on the contents of the entire packet. The time interval between the last data bit out of the Ixia transmit port and the first data bit received by the Ixia receive port is measured. The last data bit out is usually the end of the FCS or CRC, and the first data bit received is as described above for Cut Through.NOTE: Store and Forward latency mode is intended to test Store and Forward switching devices, which receive the entire packet before transmitting it to its destination. If Store and Forward latency is used in loopback, back-to-back or without a Store and Forward switch, then either a zero latency or very high latency is reported.
- Store and Forward Preamble (only available on some load modules): As with store and forward, but measured with respect to the preamble to the Ethernet frame. In this case, the time interval between the last data bit out of the Ixia transmit port and the first preamble data bit received by the Ixia receive port is measured. For this measurement, the size of the preamble (in bytes) is considered.
- Inter-Arrival Time (IAT): Compares the time between PGID packet arrivals. In this case, when a packet with a PGID is received, the PGID is examined. If a packet has already been received with the same PGID, then the timestamp of the previous packet is subtracted from the current timestamp. The interval between the timestamps is the jitter, and it is recorded for statistical purposes.

## **Sequence Checking Operation**

A number of ports have the additional ability to insert a sequence number at a user-specified position in each transmitted packet. This sequence number is different and distinct from any IP sequence number within an IP header. On the receiving port, this special sequence number is retrieved and checked, and any out-of-sequence ordering is counted as a sequence error.

As in packet groups (see <u>Packet Group Operation</u>), for sequence checking a signature value is inserted into the packet on the transmit side to signal the receive side to check the packet. In fact, this particular signature value is shared by both the packet group and the sequence checking operations. Both the signature value and sequence number are 4-byte quantities and must start on 4-byte boundaries. These fields are shown in the following figure.

Figure: Packet Format for Sequence Checking

Sequence | Signature | CRC/ |
Number | Value | FCS

Sequence Number | Offset |
Signature | Offset | Offset | CRC/ |
Number | Offset | CRC/ |
Number | Signature | CRC/ |
Number | Offset | Offset | CRC/ |
Number | Offset | Offset | Offset | Offset |
Number | Offset | Offset | Offset | Offset | Offset | Offset |
Number | Offset | Offset | Offset | Offset | Offset | Offset | Of

Sequence numbers are integers which start at `0' for each port when transmission is started, and increment by `1' continuously until a Reset Sequence Index operation is performed. Note that multiple sequence errors results when a packet is received out of sequence. For example, if five packets are transmitted in the order 1-2-3-4-5 and received in the order 1-3-2-4-5, three sequence errors are counted:

- 1. At 1-3, when packet 2 is missed
- 2. At 1-3-2, when 2 is received after 3
- 3. At 1-3-2-4, when 4 is received after 2

# Switched-Path Duplicate/Gap Checking Mode

This is a mode in sequence checking that allows for detecting duplicate packets, or sequence gaps. IxExplorer stores the largest sequence number received. Any packet that arrives with a lower or equal sequence number is regarded as a duplicated packet. For a flow with no packet reordering, the `reversal errors' matches the number of duplicates received. For a flow with packet reordering, the `reversal errors' gives a count that may be higher than the number of duplicates received.

# **Data Integrity Checking Operation**

A number of ports also possess the ability to check the integrity of data contained in a received packet, by computing an additional 16-bit CRC checksum.

As with packet groups (see <u>Packet Group Operation</u>) and sequence checking (see <u>Sequence Checking Operation</u>), a signature value is inserted into the packet on the transmitting interface, to serve as a trigger for the receiving port to notice and process the additional checksum. The data integrity operation uses a different signature value from the one shared by packet groups and sequence checking.

The data integrity signature value marks the beginning of the range of packet data over which the 16-bit data integrity checksum is calculated, as shown in the figure below. This packet data ends just before the timestamp and normal CRC/FCS. The CRC-16 checksum value must end on a 4-byte boundary. There may be 1, 2, or 3 bytes of zeroes (padding) inserted after the CRC-16, but before the Time Stamp, to enforce all boundary conditions.

Figure: Packet Format for Data Integrity Checking

Data Integrity Signature

Data Integrity CRC/
CRC-16

Stamp

CRC/
Stamp

FCS

Signature
Offset

Packet Data
for Checksum

When the Receive Mode for a port is configured to check for data integrity, received packets are matched for the data integrity signature value, and the additional CRC-16 is checked for accuracy. Any mismatches are recorded as data integrity errors.

## **Automatic Instrumentation Signature**

The Automatic Instrumentation Signature feature allows the receive port to look for a signature at a variable offset from the start of frames. The feature supports Sequence Checking, Latency, Data Integrity functionality, with signature and Packet Group ID (when Automatic Instrumentation is enabled, these receive port options are enabled as well).

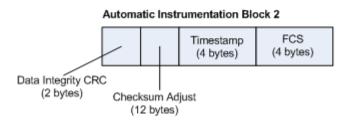
In normal stream operation, signatures for Data Integrity, Latency, and Sequence Checking are forced to a single, uniform offset location in each frame of the stream. Many of the Ixia software application (that is, IxVPN, IxChariot, and so forth) can generate streams that place a signature at random places within the frames of a single stream. To accurately detect these signatures on the receive side of the chassis, Automatic Instrumentation Signature is used.

Automatic Instrumentation Signature allows the chassis to look for a floating pattern in the frame. Two data blocks are placed in the frame (by some stream generating application). The first is positioned at a variable offset from the start of the frame. The second is positioned at a fixed 12 byte offset from the end of the frame.

The following figure shows the composition of the blocks.

Figure: Automatic Instrumentation Signature Block
Automatic Instrumentation Block 1





The receive port recognizes an instrumented frame by detecting the Signature in the first block. Once a signature match has occurred, the Packet Group ID (PGID) and Sequence

Number are extracted from the frame. Data Integrity also starts immediately following the signature.

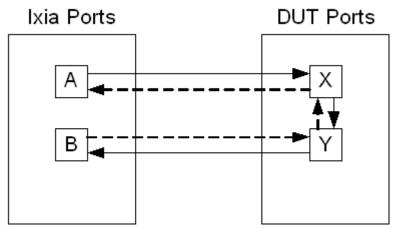
The Checksum Adjust field is reserved for load modules that cannot correctly do checksums on large frames.

### **Port Transmit/Receive Capabilities**

### **Round Trip TCP Flows**

For most 10/100 load modules, a special capability exists in the Ixia hardware to enable the measurement of round trip times for IP packets sent through a switch or other network device. The normal setup for this measurement is shown in the following figure.

Figure: RoundTrip TCP Flows Setup



In this scenario, Ports A and X are configured on one IP subnet, and Ports B and Y are configured on a different IP subnet. IP packets sent from A have a source address of A and destination address of B. The DUT is configured to route or forward to Y any packets that it receives on X for an address on B-Y's subnet. After being received on Port B, the packet is reconstructed in a modified form as described in the following list, and sent back in the opposite direction along the path to Port A.

When enabled on the Ixia receiving port (in this case, Port B), the Round Trip TCP Flows feature performs several operations on the received IP packet:

- The Source and Destination IP addresses are reversed, and a packet destined for Port A is created using the reversed addresses.
- The frame size, source and destination MAC addresses, and background data pattern are set as specified by you.
- The timestamp is copied to the new packet unmodified.
- The new packet is transmitted to Port Y on the DUT, and should be routed back to Port A by the DUT.

This re-assembly/retransmit process makes it possible to measure the round-trip time for the packet's trip from Port A through the DUT to Port B, and back through the DUT to Port A again. Note that the Packet Groups feature may be used, in addition, for latency measurements on this round trip. For latency testing, the background data set by the Round Trip TCP Flows feature overwrites the Packet Group Signature Value contained in the packet. It

is important that proper programming of the background data pattern be used to insert the appropriate signature value back into the packet.

## **Port Statistics Capabilities**

Each port automatically collects statistics. A wide range of statistics are preprogrammed and available for many types of load modules. Other statistics may be selected or programmed and include:

- User-Defined Statistics: Four counters which can be programmed to increment based on the same conditions as those involved in defining capture triggers and capture filters.
- Quality of Service Types: Separate counts for each of eight Quality of Service values used in IP headers.
- IP/UDP/TCP Checksum Verification Statistics: For hardware checksum verification.
- Data Integrity Statistics: For errors relating to Data Integrity Operation. Refer to Data Integrity Checking Operation.
- Packet Group Statistics: For statistics relating to Latency operations. Refer to Latency/Jitter Measurements.
- Protocol Server Statistics: Protocol-based statistics for a wide range of routing protocols.
- SONET Extended Statistics: Statistics associated with SONET Line, Section and Path characteristics.
- VSR Statistics: Statistics associated with OC192 VSR modules.
- ATM Statistics: Statistics associated with ATM modules.
- BERT Statistics: Statistics associated with BERT error generation and detection.
- Temperature Sensors Statistics: For verifying that temperatures on high-performance 10 Gigabit and OC-192c POS cards are within operational limits.

## **IxExplorer Software**

The IxExplorer software utilizes concepts that match the Ixia hardware hierarchy. The software hierarchy is:

- <u>Chassis Chain (Software)</u>: A set of Ixia chassis joined through sync-in/sync-out cables.
  - Chassis: A single Ixia chassis capable of holding different Ixia module cards.
    - Card: An Ixia module card, all of whose ports have the same features.
    - Port: An individual transmit/capture port on a card.
    - Capture View: A view of the capture buffer for the port.
    - Filters, Statistics and Receive Mode: A means of programming capture triggers, filters, and statistics.
    - Packet Streams: A means of programming sets of streams and flows.
    - Statistics: A view of the statistics gathered by the port.
- Global Views:
  - Port Groups: Hold groups of related ports that may be operated on at the same time.

- <u>Stream Groups</u>: Hold groups of related ports that may be operated on at the same time.
- Packet Group Statistic Views: Allows the latency data (including Inter-Arrival Time) to be collected from one or more ports that are configured to receive packet groups.
- <u>Statistic Views</u>: Holds groups of related ports, all of whose statistics can be viewed at one time.
- <u>Stream Statistic Views</u>: Holds groups of related streams, all of whose statistics can be viewed at one time.
- MII Templates: A means of creating and editing MII templates.
- Layouts: A means of saving open GUI features.
- <u>IxRouter Window</u>: A means of designating interface addresses associated with ports and programming routing protocol simulations on each port. Note that IxRouter must be installed for full use of this window. Without IxRouter, only limited use of ARP and PING are allowed. See *IxRouter User Guide* for more information.

## **Chassis Chain (Software)**

The IxExplorer chassis chain corresponds to the hardware chain. The chain starts with a master, whose sync-out line is connected to the sync-in line of the next chassis, and so on. Multiple chassis chains may be defined in the IxExplorer and operated independently or at the same time. Various forms of time synchronization may be used to coordinate multiple chassis chains dispersed world-wide into a single `virtual chassis chain'; see <a href="Chassis Synchronization">Chassis Synchronization</a>.

### **Chassis**

The IxExplorer chassis corresponds to an Ixia 400T, Optixia XM12, Optixia XM2, Optixia X16 or other chassis capable of holding Ixia module cards. The name or IP address of each chassis must be input; the type of the chassis is automatically discovered by the software. A chassis may hold any mix of module cards.

#### **Card**

The IxExplorer card corresponds to an Ixia load module card. The types of cards loaded in a chassis are automatically discovered and the appropriate number of ports are inserted into the hierarchy. Each port on a card has the same capabilities.

#### **Port**

The IxExplorer port corresponds to an individual port on an Ixia module card. Each port is independently programmed in terms of its transmit, capture and statistics capabilities. The IxExplorer software shows four separate views for programming and viewing operations:

- Filters, Statistics and Receive Mode: Sets the trigger and capture conditions for the capture buffer, conditions for the four user-defined statistics, and the receive mode for the port.
- Packet Streams/Flows: Defines the streams within stream regions and the contents of packets.

- Capture View: Shows the data gathered during capture operations. Data is displayed in raw form and interpreted for some protocols.
- Statistics: Shows the live statistics gathered during transmit and capture operation.

## **Port Properties**

A Port Properties dialog allows other port related properties to be programmed:

- Auto-Negotiation: Low level physical controls, such as 10 versus 100 Mbps operation and full duplex versus half duplex.
- Advanced MII controls: Additional low level MII register controls.
- Flow control: Related to pause control operation.
- Collision Backoff Algorithm: Handling of collision situations.
- Forced Collisions: The generation of collision packets on receive ports.
- Transmit mode: The choice of streams or flows for the port.
- SONET Header: For use with Packet Over SONET frames.
- SONET Overhead: For generation of APS (K1/K2), J0/J1 bytes, and Error Insertion.
- PPP: For use with SONET. Includes dialogs for Negotiation, Link Control Protocols, and Network Control Protocols.

## **Port Groups**

Port groups are an IxExplorer convenience. They allow to perform operations, such as start/stop transmit, start/stop capture and clear timestamps, for a wide range of ports all at the same time.

## **Stream Groups**

Stream groups are an IxExplorer convenience. They allow to perform operations, such as start/stop transmit, start/stop capture and clear timestamps, for a group of streams all at the same time.

## **Packet Group Statistic Views**

The Packet Group Statistics View allows the latency data (including Inter-Arrival Time) to be collected from one or more ports that are configured to receive packet groups. Packets representing different types of traffic profiles can be associated with packet group identifiers (PGIDs). The receiving port measures the minimum, maximum, and average latency in real time for each packet belonging to different groups. Measurable latencies include Instantaneous Latency, where each packet is associated with one group ID only, and Latency Over Time, where multiple PGIDs can be placed in `time buckets' with fixed durations.

### **Statistic Views**

Statistic Views are similar to port groups, in that they let you consider a set of ports all at once. When a Statistic View group is selected, all of the statistics for all of the ports are simultaneously viewed. The particular statistics viewed may be independently selected for

Statistics Logging and Alerts.

### **Stream Statistic Views**

Stream Statistic Views are like Statistic Views, but on a per stream basis rather than per port basis.

## **MII Templates**

Allows for the creation and/or editing of MII template files. Register templates are applied to physical ports through Port Properties dialogs.

## Layouts

Allows for the creation of templates for the layout of the IxExplorer GUI. A layout consists of the combined open features in the GUI.

### **IxRouter Window**

The IxRouter window provides the means by which routing protocols are emulated by the Ixia hardware and software. This window includes the interface by which multiple IPv4 and IPv6 interfaces are associated with each port. A growing number of protocols are supported in this window, including ARP, BGP, OSPF, ISIS, RSVP-TE, LDP, RIP, RIPng, and IGMP.

Note that full use of this window requires that IxRouter be installed. For more information on protocols and protocol testing, see *IxRouter User Guide*.

## **IxExplorer Operation**

IxExplorer saves all settings and programming in `saved' named files, which may be retrieved on each invocation. Captured data is lost when the IxExplorer is exited.

All IxExplorer test operations perform on an arbitrary set of ports, as single port or multiple ports may be selected. Any level of the hierarchy may be selected to include all ports below that level. For example, selecting a card includes all ports on that card, or selecting a chassis chain includes all ports on all cards in all chassis in the chassis chain. In addition, port groups may contain ports from any card; the port group may then be used in any testing operations.

The operations that can be performed on any group of ports:

- Start/Stop Capture: When capture is enabled, data for each port that is configured for capture (versus latency) is collected when the trigger is satisfied and to the extent that the filter is satisfied as well.
- Start/Stop Transmit: When transmit is enabled, data is transmitted as programmed to the extent designated by the synchronous stream region.
- Start/Stop Collision: Forced collisions are enabled/disabled for receive ports.
- Start/stop Latency: When latency measurement is enabled, data for each port configured for latency (versus capture) is collected when the trigger is satisfied and to the extent that the filter is satisfied as well.

- Pause/Single-Step Transmit: Transmittal of information may be paused and then single-stepped on a stream-by-stream basis or continued through a start transmit command.
- Interactive streams: This is a special function that allows for interactive variation of frame size and inter-packet gaps. Interactive streams may not be operated across ports that are configured for flows.

## **Multi-User Operation**

IxExplorer provides an optional means of coordinating the sharing of chassis ports among multiple users. If a single user is operating a chassis, multi-user commands are not required at all. As an user, you may perform any operation on any port. Two or more people may also share ports on a chassis without use of IxExplorer multi-user facilities, through some verbal agreement (for example, `You take cards 1-8 and I'll take cards 9-16'). IxExplorer provides no assistance in this instance.

Where more accurate control over port sharing is required, multi-user facilities should be used. IxExplorer's multi-user model is a very simple, advisory model. Each user logs in with an arbitrary name. Each and every user may take ownership of any and all ports. A port owner has the ability to read data and program the port; all other users have read-only access to the port. A port owner may clear ownership of ports, making them available for other users. You may take ownership of a port owned by someone else, with an optional warning message. Any user may clear all ownerships.

IxExplorer provides a further distinction of roles between users. Administrators are privileged users who may take ownership of ports, configure their characteristics, and initiate tests using those ports. Operators are unprivileged users who may only look at chassis, card, and port characteristics and measured data.

NOTE

We NEVER support multiple clients simultaneously changing data on one port. The rule is: one port-one owner for each system test. The ownership model should not be used to have one script take ownership of a port and another script take ownership of that same port with the same username because one client may be working with a copy of the port configuration that has been made invalid by another owner.

The two basic modes of multi-user operation are referred to as:

- Voluntary: All users are considered administrators and voluntarily login and take or clear ownership of ports. All chassis are initially configured in this mode.
- Secure: Users are characterized as Administrators or Operators. All users must login.
   Administrators operate in the same manner as all Voluntary mode users. Operators are restricted to viewing data.

## **Statistics Logging and Alerts**

IxExplorer has the ability to centrally log statistics from any port and to signal alert conditions when a particular statistic goes out of a specified, valid range. The following figure shows the basic operation of logging and alerts.

Client 1

Alerts 1

Chassis 1

Chassis 2

Statistics & Alert
Logs

Alerts 3

Chassis 3

Chassis 3

Figure: Statistics Logging and Alerts

The clients (Client 1 and Client 2) run IxExplorer and are connected to all of the chassis (Chassis 1, Chassis 2 and Chassis 3) in the chassis chain. The clients set up conditions under which statistics data is logged and alerts generated. These conditions are transmitted to all of the chassis. Each chassis interprets these conditions and logs statistics data and alert conditions to their local disks.

When a chassis detects an alert condition, it sends signals to **all** of the clients connected to the chassis at the moment. Each client receives alerts from **all** of the chassis, regardless of whether they set up the particular alert condition themselves.

It can take considerable effort to set up one port's statistics logging and alert conditions. It is not necessary to repeat this process for multiple ports that have identical logging and alert behavior. IxExplorer's Port Copy feature may be used to copy these specifications.

It should be noted that logging and alerts continue even after a client has exited IxExplorer.

## **Statistics Logging**

Each client selects particular statistics on particular ports to be logged. The data is logged at the chassis hosting the port. All clients connected to a chassis contribute their desired port-statistics to be logged. All statistics from all clients are logged to the same single file on a chassis.

The log file is ASCII in format and contains a line of text for each port on which statistics have been gathered. Each line contains all of the selected statistics for the port, separated by commas. The contents of the file are easiest to understand and interpret if the same statistics are gathered for all ports.

The statistic values that are logged are the rolling average' for the value logged. That is, a value at time slot n depends on the previous average and the current measured value, as per the following equation:

 $Average_n = (Average_{n-1} * (n-1)/n) + (Measurement_n * 1/n)$ 

The client specifies several parameters that affect the logging of statistics:

- Enable/Disable: Enable or disable all statistics logging specified from this client.
- Log at interval: Specify an interval between logged entries.
- Log during alerts: Log statistics while alert conditions exist.
- File naming: The format and location of logging files on the chassis.

Multiple clients should agree on the log interval and file naming conventions; the chassis uses the settings received from any client that applies changes.

#### **Alerts**

Each client sets up anticipated valid ranges for particular statistics on specific ports. All clients connected to a chassis distribute their specific valid ranges to all chassis. Each chassis watches for out of range values on the specified port-statistics and generates alerts for the conditions. **All** alert conditions are sent to **all** connected clients. Alert condition changes may be optionally logged on files at the chassis.

The client indicates how it wants to receive alerts for a particular statistic and port. There are three options:

- Visual: each statistic subject to alerting is displayed as green (in range), red (out of range) or yellow (was previously out of range) in any Statistic View containing the port-statistic.
- Audible: while any out of range condition exists, the client's computer issues a repeating beep-beep. A client may mute all audible alarms at once.
- · Both visual and audible.

In addition, the existence of an alert condition for a particular port-statistic may be used to initiate statistics logging for that port, as described in Statistics Logging.

The client specifies several parameters that affect the setup of alert conditions:

- Enable/Disable alerts: Enable or disable all visual and/or audible alerts specified from this client.
- Enable/Disable Alert Logging: Enable or disable the logging of alert change conditions on the chassis.
- File Naming: The format and location of alert files on the chassis.

Multiple clients should agree on the valid range of port-statistics values and file naming conventions; the chassis uses the settings received from any client that applies changes.

### **Tcl Software Structure**

The Tcl software is structured as a number of client-server pieces so that it may operate simultaneously in three different environments:

- On the Ixia chassis: The Tcl scripts are executed on the same computer that runs the Ixia hardware.
- On a Windows client: The Tcl scripts are executed on a Windows 2000/XP client.
- On a Unix client: The Tcl scripts are executed on a Unix client.

The following sections describe the components used in each of these scenarios.

## **Operation on the Ixia Chassis**

When the Tcl client software is installed on the Ixia chassis itself three distinct software components are used, as shown in the following figure.

Figure: Software Modules Used on an Ixia Chassis



In this scenario, three components are used as described in the following table.

Software Modules Used on an Ixia Chassis

Module	Usage
Tcl scripts	Ixia supplied and user developed Tcl. The Tcl extensions that program the Ixia hardware use the TclHAL layer.
TclHAL	A layer of software, supplied as a DLL (Dynamic Linked Library), that is responsible for interpreting the Tcl commands into C++ functions to be sent to the IxServer software.
IxServer	An independent Windows executable that is responsible for directly controlling the Ixia hardware.

## **Operation on a Windows Client**

When the Tcl client software runs on a Windows client, the same three components are used but in a different configuration, as shown in the following figure.

Ixia Chassis

Windows Client

Tol script

Tol script

Tol script

Windows Client

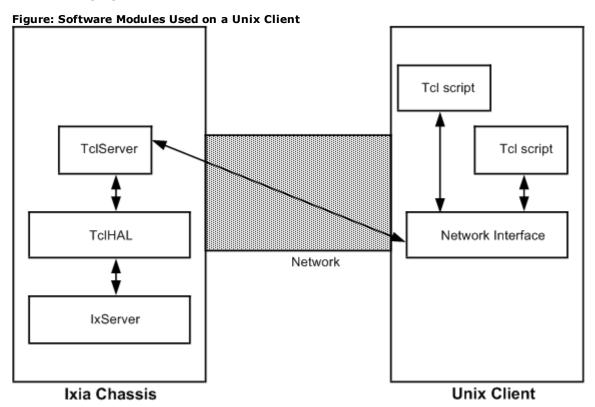
In this scenario, three components are used as described in the following table.

Software Modules Used on a Windows Client

Module	Usage
Tcl scripts	Ixia supplied and user developed tests run on the Windows client using the Tcl software. The Tcl extensions that program the Ixia hardware use the TclHAL layer.
TclHAL	A layer of software, supplied as a DLL (Dynamic Linked Library), that is responsible for interpreting the Tcl commands into C++ functions to be sent to the IxServer over the local network.
IxServer	An independent Windows executable running on the Ixia Chassis that is responsible for directly controlling the Ixia hardware. Its commands are received from clients over the LAN.

## **Operation on a Unix Client**

When the Tcl client software runs on a Unix client, five components are used as shown in the following figure.



In this scenario, five components are used as described in the following figure.

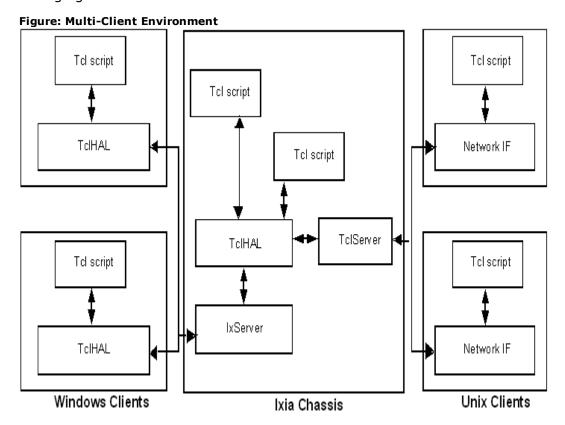
Software Modules Used on a Unix Client

Module	Usage
Tcl scripts	Ixia supplied and user developed tests run on the Windows client using the Tcl software. The Tcl extensions that program the Ixia hardware use the Tcl-DP client software.

Module	Usage
Network Interface	This is a layer of software within the TCL system that translates hardware commands into ascii commands, which are sent to the TCL Server on the connected Ixia chassis.
TclServer	This layer receives commands from the TcI-DP client on Unix client platforms. Commands are translated into calls to the TcIHAL layer.
TclHAL	A layer of software, supplied as a DLL (Dynamic Linked Library), that is responsible for interpreting the Tcl commands into C++ functions to be sent to IxServer on the chassis over the network.
IxServer	An independent Windows executable running on the Ixia Chassis that is responsible for directly controlling the Ixia hardware. Its commands are received from clients over the LAN.

# **Multiple Client Environment**

A single Ixia chassis may be used by multiple clients simultaneously. Clients may run from the Ixia chassis, Windows clients, and Unix clients simultaneously, as shown in the following figure.



### **TCL Version Limitations**

Note the following limitation with respect to Tcl versions and the use of Wish and Tclsh shells:

- 1. Tcl 8.0 is no longer supported.
- 2. Tclsh does not run on any version of Windows, with Ixia software. Under Linux or Solaris, Tclsh runs on any version of Tcl greater than or equal to 8.2.

The use of the Wish shell with Ixia software has been tested for Tcl 8.3 under Windows, Linux, and Solaris. It has not been tested, but should run with any Tcl version greater than or equal to 8.2.

Beginning with the Ixia TCL libraries supplied with IxOS version 3.80, these libraries are compatible with TCL version 8.3 and above. That is, it is not necessary to obtain a new version of the Ixia libraries when TCL 8.4 (or above) is installed on a computer.

## **Chapter 3 - Theory of Operation: Protocols**

### **Protocol Server**

Most ports in an Ixia chassis operate a Protocol Server. The Protocol Server includes a complete TCP/IP stack, allowing different forms of high-level DUT testing. The Protocol Server can be configured to test a set of provided Level 2 and Level 3 protocols, which include MAC and IP addressing and IP routing. The Protocol Server for Packet over SONET cards omits all MAC configuration items, since POS does not use a MAC layer. The information gathered by the Protocol Server is used within generated frame data, as well.

The Protocol Server can be accessed through the IxRouter Window. Each protocol must be individually enabled for a selected port in the IxRouter Window.

The protocols supported by the Ixia Protocol Server are described in the following sections in this chapter:

Protocols Supported by Ixia Protocol Server

Address Resolution Protocol (non- POS only) (includes IP to MAC addressing)	See ARP
(Includes IP to MAC addressing)	
Internet Gateway Management Protocol	See <u>IGMP</u>
Open Shortest Path First Protocol	See OSPF
Open Shortest Path First Protocol Version 3 (for IPv6)	See <u>OSPFv3</u>
Border Gateway Protocol	See <u>BGP4/BGP+</u>
Routing Information Protocol	See <u>RIP</u>
Routing Information Protocol: Next Generation (for IPV6)	See RIPng
Intermediate System to Intermediate System (Dual Mode)	See <u>ISISv4/v6</u>
Resource ReSerVation Protocol: with Traffic Engineering Extensions	See <u>RSVP-TE</u>
Label Distribution Protocol	See <u>LDP</u>
Multicast Listener Discovery	See MLD
Protocol Independent Multicast: Sparse Mode	See PIM-SM/SSM-v4/v6
Multi-Protocol Label Switching	See MPLS
Bi-Directional Forwarding	See BFD

Connectivity Fault Management	See <u>CFM</u>
Fibre Channel over Ethernet (FCoE), FCoE Initialization Protocol (FIP) and NPIV	See FCoE and NPIV
Precision Time Protocol (PTP)	See Precision Time Protocol (PTP) IEEE 1588v2

There are additional sections on the following topics:

- ATM Interfaces
- Generic Routing Encapsulation (GRE)
- DHCP Protocol
- Ethernet OAM

#### **ARP**

The Address Resolution Protocol (ARP) facility controls the manner in which ARP requests are sent. This option is only available on Ethernet load modules. The resulting responses from ARP requests are held in the ARP Table, which is used to set MAC addresses for transmitted data. ARP'ing the Device Under Test (DUT) allows tests and generated frames to be configured with a specific IP address, which at run time is associated with the MAC address of that particular DUT.

#### **IP**

The IP table within the ARP window specifies a per-port correspondence between IP addresses, MAC addresses (for Ethernet ports only), and the Default Gateway. IP addresses may be expressed as individual addresses or as a range of addresses.

All ARP requests (for Ethernet) are sent to the Default Gateway address. In most cases, the Default Gateway Address is the address of the DUT. When a gateway separates the Ixia port from the DUT, use the IP address of that gateway as the Default.

### **IGMP**

The Internet Group Management Protocol (IGMP) is used with IPv4 to control the handling of group membership in the Internet. Version 3, specified in RFC 3376, is supported and is interoperable with Versions 1 and 2. Version 1 of the protocol is specified in RFC 1112, and Version 2 is specified in RFC 2236.

IGMP normally works in an environment in which there are a number of IGMP-capable hosts connected to one or more IGMP routers. The routers forward membership information and packets to other IGMP routers and receive group membership information and packets from other IGMP routers.

The Ixia hardware simulates one or more hosts, while the DUTs are assumed to be IGMP routers. The simulation calls for groups of simulated hosts to respond to IGMP router-generated queries and to automatically generate reports at regular intervals. A number of IGMP groups are randomly shared across a group of hosts.

Version 3 adds the concept of filtering, based on the IP source address, to cut down on the reception of unwanted multicast traffic. This filtering consists of limiting the receipt of packets to only those from specific sources (INCLUDE) or to those from all but specific

sources (EXCLUDE). Refer to  $\underline{\text{MLD}}$  for information about similar functions for multicast traffic in IPv6 environments.

Compatibility with earlier versions of IGMP is an important part of IGMPv3. The Group Compatibility Modes for an IGMPv3 router are summarized as follows:

- IGMPv3 Compatibility Mode (default): An IGMPv2 and/or IGMPv1 Host is present, but NOT running.
- IGMPv2 Compatibility Mode: An IGMPv2 Host may be present and running. An IGMPv1 Host is present, but NOT running.
- IGMPv1 Compatibility Mode: An IGMPv1 Host is present and running.

#### **OSPF**

#### NOTE

See also OSPFv3

Open Shortest Path First (OSPF) is a set of messaging protocols that are used by routers located within a single Autonomous System (AS). The Ixia hardware simulates one or more OSPF routers for the purpose of testing one or more DUT routers configured for OSPF. The OSPF version 2 specification (RFC 2328) details the message exchanges by OSPF routers, as well as the meanings and usage.

OSPF has the following three principal stages:

- The HELLO Protocol
- Database transfer
- HELLO Keepalive

When an OSPF router initializes, it sends out HELLO packets and learns of its neighboring routers by receiving their HELLO packets. If the router is on a Point-to-Point link, or on an Ethernet (transit network) link, these packets are addressed to the *AllSPFRouters* multicast address (224.0.0.5). In these types of networks, there is no need to manually configure any neighbor information for the routers.

Each router that is traversed on the path between neighbors is added to a list contained in the HELLO packet. In this way, each router discovers the shared set of neighbors and creates individual state machines corresponding to each of its neighbors.

If the network type is broadcast, then the process for selecting a Designated Router (DR) and Backup Designated Router (BDR) begins. A Designated Router is used to reduce the number of adjacencies required in a broadcast network. That is, if no Designated Router is used, then each router must pair (form an adjacency) with each of the other routers. In this case, the number of required adjacencies is equal to the <u>square</u> of the number of routers ( $N^2$ ). If a DR and BDR are used, the number of required adjacencies drops to 2 times the number of routers (2N). Currently, the Ixia ports are unable to simulate a DR or BDR.

Once the routers have initialized their adjacency databases, they synchronize their databases. This process involves one router becoming the master and the other becoming the subordinate. On Ethernet networks, the DR is always the master; on point-to-point networks, the router with the highest Router ID is the master.

Link State Advertisements (LSAs) are OSPF messages that describe an OSPF router's local environment. The simplest LSA Type is the router-LSA (RouterLinks LSA). Each router is

required to generate exactly one of these LSAs to describe its own attached interfaces. If a network that consists of a single OSPF area is being simulated with only point-to-point links and there are no Autonomous System Border Routers (ASBR), then this is the only type of LSA that is sent.

The subordinate asks the master for its LSA (Link State Advertisement) headers, which enables the subordinate to determine the following information:

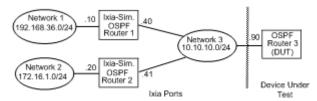
- 1. The subset of LSAs that the master holds, but that the subordinate does not have, and
- 2. The subset of LSAs that the master and subordinate both have, but which are more recent on the master.

The subordinate router then proceeds to explicitly query the master to send it each LSA from Steps (1) and (2). The subordinate sends an ACK to the master upon receipt of each LSA. The global Link State Database (LSDB) is constructed by each router, based on LSAs from all the other routers in the network.

Once this exchange process is complete, the routers are considered to have reached Full Adjacency, and each runs the link state algorithm to update its IP forwarding tables. The routers continue to exchange periodic HELLO packets, as keepalive messages, until a change occurs (for example, a link goes down or an LSA expires). OSPF routers continue to periodically exchange their LSAs every 30 minutes to ensure that they all hold identical LSDBs.

This section describes the programming of the Ixia hardware related to OSPF testing, as well as the theory of operation and protocol message formats. The Ixia hardware simulates multiple OSPF routers on multiple networks. For example, in the following figure, there are three networks and three routers.

Figure: Sample OSPF Network



The Protocol Server calls for the specification of router-network connections to be specified in a network-centric fashion. One specifies the network in terms of an Area ID and network mask. One specifies the routers in terms of the interface IP address on that network and Router ID, usually the lowest IP address for the router. For the sample OSPF network, in which Router 3 is the DUT, the three networks are specified by their significant characteristics as shown in the following table.

Sample OSPF Network Assignments

Network	Area ID	Network Mask	Router ID	Router Interface IP Address
1	192.168.36.0	255.255.255.0	192.168.36.10	10.0.0.40
2	172.16.0.0	255.255.255.0	172.16.0.20	10.0.0.41

Network	Area ID	Network Mask	Router ID	Router Interface IP Address
			10.0.0.40	10.0.0.40
3	10.0.0.0	255.255.0.0	10.0.0.41	10.0.0.41
			10.0.0.90	10.0.0.90

Within this framework, Link State Advertisements (LSAs) may be issued from the perspective of any interface on any router. Any OSPF messages from the DUT Routers may be captured and analyzed in the normal manner.

#### OSPFv3

Open Shortest Path First Protocol Version 3 supports Internet Protocol version 6 (IPv6), as defined in RFC 2740. The 128-bit IPv6 addressing scheme has been accommodated in OSPF through the use of new LSA types.

Some of the differences between OSPFv2 (for IPv4) and OSPFv3 (for IPv6) are listed as follows:

- Changes to adapt to the IPv6 128-bit address size. No addresses are carried in OSPF packets or basic LSAs, but addresses are carried in certain LSAs.
- OSPFv3 operation is per Link, with the IPv6 concept of `link' replacing the `IP subnet' and `network' terminology of OSPFv2.
- OSPVv3 supports multiple instances of the protocol per link, through `Instance IDs.'
- LSA flooding scope is explicitly defined in the LS Type field of each LSA.
- Authentication is handled by the IPv6 protocol itself, rather than by the OSPF protocol. For this reason, Authentication information has been removed from the packet headers in OSPFv3.

NOTE

In OSPFv2, IPv4 addresses were used in many contexts besides IP source and destination addresses. For example, they were assigned as name identifiers for routers (RIDs). This naming convention for RIDs has been retained in OSPFv3.

## BGP4/BGP+

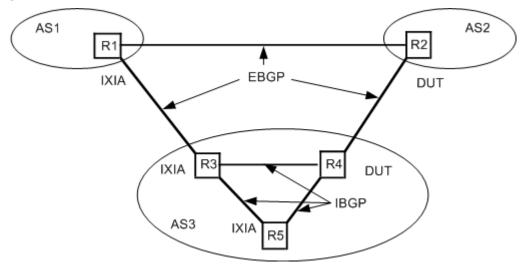
Border Gateway Protocol Version 4 (BGP-4) is the principal protocol used in the Internet backbone and in networks for large organizations. The BGP4 specification (RFC 1771) details the messages exchanged by BGP routers, as well as their meaning and usage. *BGP4 - Inter-Domain Routing in the Internet*, by John W. Stewart III is a descriptive reference on this protocol.

#### **Internal Versus External BGP**

The BGP4 protocol is used according to two sets of rules, depending on whether or not the two communicating BGP routers are within the same Autonomous System (AS). An AS is a collection of routers that implement the same routing policy and are typically administered by a single group of administrators. ASs connected to the Internet are assigned Autonomous System Numbers (ASNs) that are key to inter-domain routing. When BGP is used **between** two ASs, the protocol is referred to as EBGP (External BGP); when BGP is used

**within** an AS it is referred to as IBGP (Internal BGP). The following figure depicts the differences in topology between EBGP versus IBGP.

Figure: External BGP Versus Internal BGP



In the figure above, AS1, AS2, and AS3 are distinct Autonomous Systems. The Rns are routers in the various ASs. Routers on the links between ASs `speak' EBGP, while the routers within AS3 `speak' IBGP.

#### **IBGP Extensions**

In the original BGP4 specification (RFC 1771), all IBGP routers within an AS are required to establish a full mesh with each other. This leads to a lack of scalability which is solved by the introduction of two additional concepts: *route Reflection* and *Confederations*.

In route reflection, some routers in an AS are assigned the task of re-distributing internal routes to other internal AS routers. To prevent looping within an AS that uses route reflection, two concepts are important: the *originator-id* and *cluster-list* attributesThe originator-id is the identification of the router that originated a particular route. Routers within an AS propagate this information and refuse to send a route back to its originator. Even the use of route reflectors and originator-ids can lead to scalability problems in an AS. The cluster-list concept helps this problem. A cluster consists of a reflecting router and its clients. A Cluster ID is the IP address of the reflecting router if there is one, or a configured number otherwise. A cluster-list is a constructed list, consisting of the cluster IDs of all of the clusters that a route has passed through. Each router refuses to send a route back to a cluster that has seen the route already.

In a confederation, an AS is divided into multiple sub-confederation subsets. Each sub-confederation is defined in terms of its own ASN and a list of routers. Routers within a sub-confederation are expected to fully mesh using IGP. Sub-confederations within a confederation speak a variant of EGP, called EIGP. Additional path attributes are used with a confederation to indicate paths that should not be propagated outside the confederation.

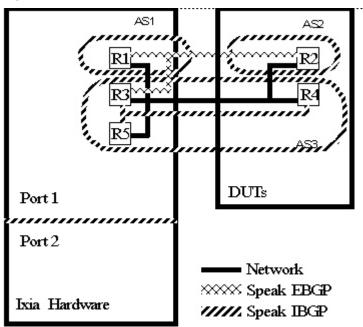
#### **Communities**

In deployment of BGP4 into a growing Internet environment, it became necessary to deal with certain routes in different manners not related to the strict routing of packets. The community attribute was invented to allow a route to be `tagged' with multiple numbers, called communities. This is also referred to sometimes as *route coloring*.

### **BGP Router Test Configuration**

The Ixia Protocol server implements an environment in which the Ixia hardware simulates multiple routers which speak IBGP and/or EBGP with one or more DUT routers. For example, in the <a href="External BGP Versus Internal BGP">External BGP Versus Internal BGP</a> figure, the Ixia hardware emulates R1, R3, and R5 while the DUTs are R2 and R4. The following figure depicts the same setup based on the location of the simulated or actual router:

Figure: BGP Interconnection Environment

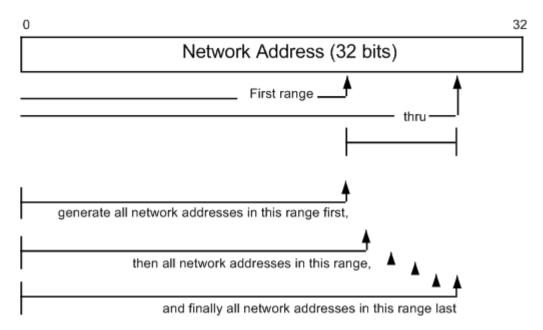


All of the routers are logically connected through appropriate networking hardware. The Ixia hardware is used to simulate three of the routers in two different ASs communicating with two routers being tested.

A single router emulated by the Ixia hardware is specified by a single IP address, and a number of emulated routers may be specified by a range of IP addresses. Each DUT router is identified by its IP address.

Messages may be sent between the emulated routers and the DUT routers when a connection is made and one of the two endpoints sends an OPEN message. Where the emulated routers and the DUT routers send their OPEN messages simultaneously, standard collision handling is applied. Thereafter, the emulated routers send a number of UPDATE messages to the DUT routers. The UPDATE messages contain a number of network address ranges (route ranges), also known as ranges of prefixes. The ranges of generated network addresses is illustrated in the following figure.

Figure: Generation of Network Addresses in BGP UPDATE Messages



A designated number of network addresses are generated with network Mask Width with the *From* through *To* values. The following table shows some examples of generated addresses. Network Addresses are generated by starting with the First Route and *From* mask width up to, but not including 224.0.0.0. (127.\*.\* is also skipped). If the requested number of network addresses has not been generated before 224.0.0.0 is reached, then the next mask length is used with the First Route to generate network addresses.

Examples of Generated BGP Routes (Network Addresses)

First Route	Mask Widt- h From	Mask Widt- h To	Iter- ator Step	Number of Routes	Generated BGP Routes (Network Addresses)
					192.168.36.0/24
					192.168.37.0/24
					192.168.38.0/24
	24	26	1	(14,378,75- 6 Max.)	223.255.255.0/24
					(224.0.0.0+ skipped)
192.168.36 0					192.168.36.0/25
					192.168.36.128/25
					192.168.37.0/25
					223.255.255.128/25
					(224.0.0.0+ skipped)
					192.168.36.0/26
					192.168.36.64/26

First Route	Mask Widt- h From	Mask Widt- h To	Iter- ator Step	Number of Routes	Generated BGP Routes (Network Addresses)
					192.168.36.128/26
					223.255.255.192/26
204 107 56					204.197.56.0/24204.197.66.0/
204.197.56	24	24	10	4	24204.197.76.0/24204.197.86.0- /24

All of the generated network addresses are associated with a set of attributes that describes routing to these generated network addresses and associated features.

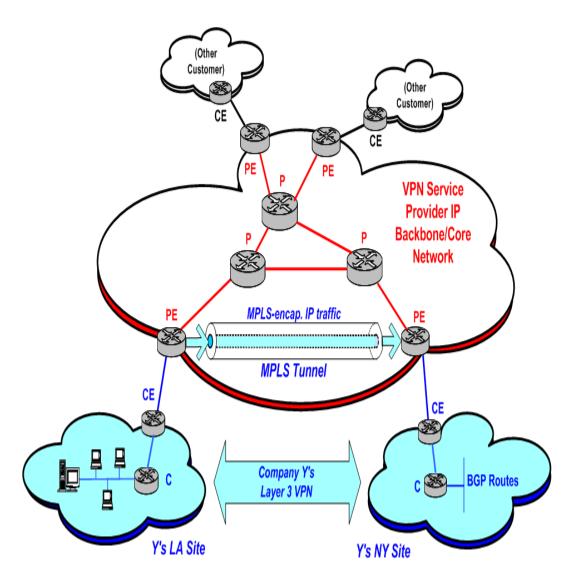
Only one route can be added per UPDATE message, but a variable number of *withdrawn* routes may be packed into each UPDATE message. The packing is randomly chosen across a range of a number of routes. The time interval between UPDATE messages is configurable, in units of milliseconds.

A BGP4 network condition called `flapping' can be emulated by the protocol server on an Ixia port. In the Link flapping emulation, a peer BGP router appears to be going offline and online repeatedly, which is accomplished on the Ixia port by alternate disconnects and reconnects of the TCP/IP stack. In the Route flapping emulation, BGP routes are repeatedly withdrawn, and then re-advertised, in UPDATE messages.

#### **BGP L3 VPNs**

L3 Virtual Private Networks (VPNs) over an IP backbone (at Layer 3 of the OSI model), may be provided to the customers of a Service Provider (SP), providing connectivity between two or more sites owned by the customer. L3 VPNs are independent of the Layer 2 protocol. While MPLS handles the packet forwarding in the backbone/core, the BGP protocol provides a means of advertising external routes/network addresses across that backbone between sites. IETF Internet Draft `draft-ietf-ppvpn-rfc2547bis-01.txt,' the proposed successor to RFC 2547, covers the VPN architecture designed for use by private service providers. A simplified example of a BGP L3 VPN topology is shown in the following figure.

Figure: Simplified BGP L3 VPN Diagram

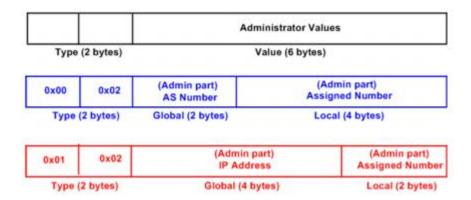


The term *site* refers to a customer/client site, which consists of a group of inter-connected IP devices, usually in one geographic location. A Customer Edge (CE) device, typically a router, connects the site, through a data link connection, to a Provider Edge (PE) router an entry point to the service provider's backbone. The PE-to-CE routing protocols may be static routing, or a dynamic protocol such as eBGP or RIPv2.

Provider (P) network core routers, `transparently' carry the IP traffic across the internal core between CE routers. CEs and Ps are not `VPN-aware' devices. CE devices are considered as belonging to a only one site, but that site may belong to multiple VPNs. A VPN Routing and Forwarding table (VRF) on a PE consists of an IP routing table, a forwarding table, and other information on the set of interfaces in the VPN. The VRF generally describes a VPN site's routing information, and a PE may maintain multiple VRFs, one for each connected customer site. See <u>L3 VPN VRFs</u> for additional information on VRFs.

Layer 3 VPN sites are identified by a Route Target (RT). A route target is based on the mechanism proposed in the IETF draft for the `BGP Extended Communities Attribute.' An 8-byte route target is common to all route ranges that belong to a single L3 site. Route targets are defined for individual VPN route ranges. The formats for Route Targets (RTs) are shown in the following figure.

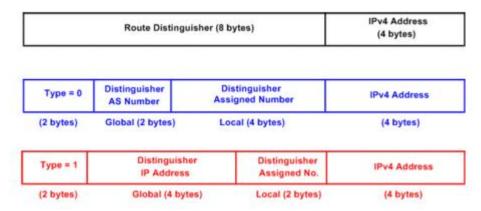
Figure: Route Target Formats (BGP Extended Community Types)



#### **BGP VPN-IPv4 Address Formats**

Globally unique 12-byte VPN-IPv4 prefixes are created by a PE router. This includes configuration of the 8-byte VPN Route Distinguishers (RDs). It should be noted that BGP IPv4 routes and VPN -IPv4 routes are considered noncomparable; VPN-IPv4 addresses can be used only within the VPN service provider network. The route distinguishers are used by PE routers to associate routes with the path to a particular CE site router in a VPN. Each route can only have one RD. The formats of the RDs are shown in the following figure.

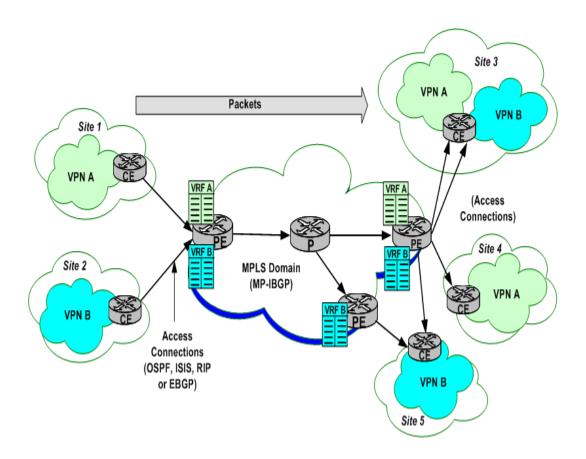
Figure: VPN-IPv4 Address Formats (with Route Distinguishers)



#### L3 VPN VRFs

For Layer 3 Virtual Private Network (L3 VPN) configurations, the Provider Edge (PE) routers maintain routing tables for each VPN that they participate in, termed VPN Routing and Forwarding tables (VRFs). The VRFs are populated with routes received from both the directly attached and remote Customer Edge (CE) routers. Each entry in the VRF is called a VPN Forwarding Instance (VPI). VRFs and CEs are not required to be configured on a one-to-one basis, although this is the typical situation. An example of the possible relationships between VRFs and CEs is shown in the following figure.

Figure: L3 VPN VRF Example



### **RIP**

The Routing Information Protocol (RIP) is an interior routing protocol. It is the oldest and most frequently used of the LAN routing protocol. RIP routers broadcast or multicast to each other on a regular basis and in response to REQUEST packets. RIP routers incorporate routing information received from their neighbors into their own routing table and forward them on to other neighbors. Two distinct versions of RIP exist: version 1 and version 2. Both IPv4 and IPv6 are supported.

As implemented by the Protocol Server, each Ixia port is capable of simulating one or more routers at distinct addresses. Routing tables for the simulated routers are configured by you and sent out at regular intervals, with a configurable randomizing factor. Either version 1 or version 2 packet formats may be sent through multicast or broadcast (for compatibility with version 1 routers). Received packets may be filtered for version 1 and/or 2 compatibility.

The current implementation of the Protocol Server uses Split Horizon with Space Saver as its update mode, which receives, but not process RIP broadcasts heard from DUT routers. That is, it does **not** incorporate received information into its own table, but rather always broadcast the same routing table. Future versions will offer Split Horizon, Split Horizon with Poison Reverse, and Silent modes of update.

The Protocol Server, however, responds to REQUEST packets that it receives. Two types of requests are processed:

• Request for all routes: The Protocol Server sends the same routing table that it sends at regular intervals back to the requestor.

• Request for specific routes: The Protocol Server fills in the requested information in the received packet and send it back to the requestor.

#### **RIP Overview**

The Routing Information Protocol (RIP) is an interior gateway routing protocol (IGP) and uses a Distance Vector Algorithm. It is the oldest and most frequently used of the LAN routing protocols. RIP routers broadcast or multicast to each other on a regular basis and in response to REQUEST packets. RIP routers optionally incorporate routing information received from their neighbors into their own routing table and forward it on to other neighbors.

For information on **RIPng** (RIP-Next Generation), based on IPv6, see RIPng

As implemented by the Protocol Server, each Ixia port is capable of simulating one or more routers with separate addresses. Routing tables for the simulated routers are configured by you and sent out at regular intervals, with a configurable randomizing factor. Either Version 1 or Version 2 packet formats may be sent through multicast or broadcast (for compatibility with Version 1 routers). Received packets may be filtered for Version 1 or Version 2 compatibility.

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## **RIPng**

Routing Information Protocol - Next Generation (RIPng) is specified for use with IPv6 in RFC 2080. Like the IPv4 version of RIP, this routing protocol is based on a Distance Vector algorithm. RIPng routers compare information for various routes through an IPv6 network, especially the information related to the RIPng metric. Due to the limited number of allowed hops, this protocol is used in small- to moderate-sized networks. The valid metric range is from 1 to 15 (hops). The metric values of 16 and above are defined as `infinity' and are considered unreachable.

An RIPng router is assumed to have interfaces to one or more directly-connected networks. Each router maintains a routing table, with one entry for every reachable destination in the RIPng network. Each routing table entry contains a minimum of:

- IPv6 destination prefix(es)
- total metric cost for the path to the destination(s)
- IPv6 address of the next hop router

- a `route change flag'
- timers

As a UDP-based protocol, the RIPng routing process functions on UDP well-known port number 521 (the `RIPng port'), on which datagrams are sent and received. The RIPng port supports the following:

- Receives all communications received from another router's RIPng process.
- Sends all RIPng routing update messages.
- Unsolicited routing update messages specify this port as the source and destination.
- Responses to request messages are sent to the originating UDP port.
- Specific requests need not come from the RIPng port, but the destination on the targeted device must be the RIPng port.

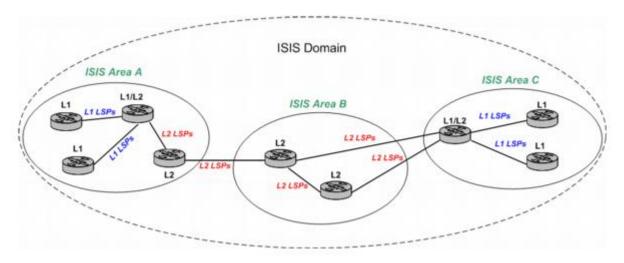
## ISISv4/v6

The Intermediate System to Intermediate System (ISIS) routing protocol was originally designed for use with the OSI Connectionless Network Protocol (CLNP) and was defined in ISO DP 10589. It was later extended to include IP routing in IETF RFC 1195. When routing for OSI and IP packets (defined in ISO/IEC 10589:1992(E)) is combined in this way, the protocol is referred to as Integrated ISIS or Dual ISIS. In addition, RFC 2966 extends the distribution of routing prefixes among ISIS routers, and IETF DRAFT draft-ietf-isis-ipv6-05 adds IPv6 routing capability to the protocol.

## **ISIS Topology**

ISIS areas are administrative domains which contain ISIS routers, have one or more private networks, and may share networks with other areas. The example shown in the following figure consists of a theoretical ISIS topology. Note that, as shown in this diagram, all ISIS routers are considered to reside entirely **within** an area, unlike some other protocols such as OSPF, where routers can reside at the edges of areas and domains.

Figure: ISIS Topology



One or more Area IDs are associated with an area. Most areas only require one ID during steady state operation, but up to three IDs may be needed during the process of migrating

a router from one area to another. In most cases, the maximum number of area IDs is set to three.

ISIS routers can be divided into three categories, as follows:

- **Level 1 (L1)**: These routers can connect only to L1 or L1/L2 routers within their own area (intra-area). They have no direct connection to any other ISIS area.
- Level 2 (L2): These routers can connect only to other L2 routers outside their area, or to L1/L2 routers within their own area. They are used as backbone routers in the routing domain, to connect ISIS areas.
- Level 1/2 (L1/L2): These routers have separate interfaces which can connect to both L1 routers within their own area and L2 routers in other areas.

Entirely separate routing tables are maintained for Level 1 and Level 2 ISIS information, even within L1/L2 routers. All L1s within an area maintain identical databases. All L2s within a domain maintain identical databases.

### **ISIS Processing**

Many OSI concepts are necessary for describing ISIS. The following terms are important to the following discussion:

- IS Intermediate System. An ISIS router is an IS.
- ES End System. A host is an ES. (Note: The Ixia hardware does not currently simulate End Systems.)
- PDU Protocol Data Unit. PDUs contain messages used for the ISIS protocol. The following PDUs are used in IS-IS communications:
  - IIH IS-to-IS Hello PDU. This message is multicast over broadcast networks, or unicast on point-to-point links, between ISs to discover neighbors and maintain ISIS state.
  - LSP Link State PDU. This message holds the significant part of the routing table sent between ISIS routers.
  - SNP Sequence Number PDU. This message is used to request LSPs and acknowledge receipt of LSPs. Two types are used depending on the network type:
    - CSNP Complete SNP. In broadcast networks, these are sent by the Designated Router in an area. On point-to-point connections, CSNPs are used for initialization. A CSNP contains a complete description of the LSPs in the sender's database.
    - PSNP Partial SNP. On broadcast networks, PSNPs are used to request LSPs. On point-to-point connections, PSNPs are used to acknowledge receipt of LSPs. On both types of networks, PSNPs are used to advertise newly learned LSPs or purge LSPs. A PSNP contains a subset of the received records.

ISIS routers maintain knowledge of each other by exchanging Hello PDUs at regular, configured *Hello intervals*. A router is considered down if it does not respond within a separately configured *Dead interval*.

ISIS routers update each other using Link State PDUs (LSPs) at a regular interval of 30 minutes. The LSP header contains the Remaining Lifetime for the LSP, a Sequence

Number, and a checksum. Each LSP contains information about a router's connection to local networks, plus a metric related to each network. ISO DP 10589 defines four types of metrics: default, delay, expense, and error.

In a Broadcast/LAN network, the Designated Router sends a Complete Sequence Number PDU (CSNP). In a Point-to-Point network, the receiving router sends a Partial Sequence Number PDU (PSNP).

In the ISIS protocol, for each of the levels (L1 or L2), one of the routers is elected as the Designated IS, based on priority values assigned to each interface as part of Hello PDU processing. The Ixia Protocol Server does not support the role of DR, so to ensure that it is not elected by its ISIS peers each Ixia-simulated ISIS router has a default priority of `0,' indicating its unwillingness to be the Designated IS.

#### **ISIS Addresses**

Due to the OSI derivation of the ISIS protocol, each ISIS router has an OSI NET address of 8 to 20 octets in length. The NET address consists of two parts: an Area ID and a System ID. The Area ID has a number of different formats defined in OSI specifications. The System ID may be from 1 to 8 octets in length. The default System ID length defaults to 6 octets and must be the same length for every router in the domain. The System ID is unique within its ISIS **area** for Level 1, or unique within the ISIS routing **domain** for Level 2 or Level 1/2. Two types of network connections are supported: broadcast and point-to-point. In a broadcast network, each interface on an ISIS dual-mode router must have an IP address and mask.

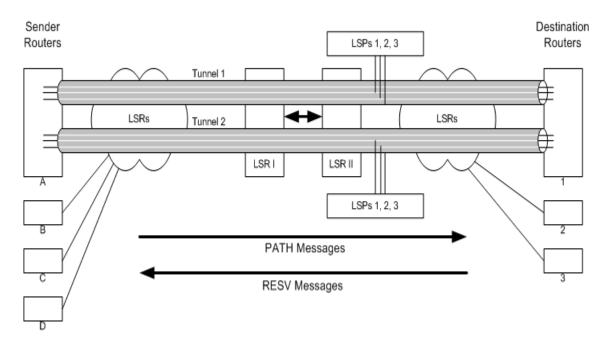
### **RSVP-TE**

The Ixia protocol server implements a part of the Resource Reservation Protocol (RSVP) used for Traffic Engineering (TE). This subset of the RSVP protocol, referred to as RSVP-TE, is used in the process of constructing a path through a sequence of MPLS-enabled label switched routers (LSRs), while reserving necessary bandwidth resources. The use of an internal gateway routing protocol (IGP), such as OSPF, is also required to automatically determine the `next hop' router.

Multi-Protocol Label Switching (MPLS) allows rapid forwarding of packets across a sequence of routers, without time-consuming examination of the packet contents at each hop. Label switching has been used extensively for ATM traffic, where overhead bytes for each `cell,' or packet, of data constitute a large percentage of the overall data transmitted. The addition of a `label' value to the header information in each cell or packet supplies the only forwarding information required to transit the MPLS domain. Based on information in its forwarding table, each LSR replaces (swaps) the incoming label with a new one which directs the packet to the next hop.

The most important output from an RSVP-TE setup session is the set of *MPLSlabels*, which are used by the MPLS-enabled routers along the path to efficiently forward network traffic. The operation of RSVP-TE is shown in the following figure.

Figure: RSVP-TE Overview



Through the use of RSVP-TE message exchanges, the router at the entry to the MPLS domain, also known as an Ingress LSR, initiates the creation of a dynamic `tunneled' pathway to the Egress LSR, the router at the exit side of the MPLS domain. Packets which pass through this `tunnel' are essentially `protected' from the extensive packet processing normally imposed by each router it traverses. Once this special pathway or Label Switched Path (LSP) is established, the router can **forward**, rather than route, packets across the domain, saving considerable processing time at each intermediate LSR (Transit LSR). The resulting tunneled pathway is known as an LSP Tunnel. The traffic flows through an LSP Tunnel are unidirectional. To establish bidirectional traffic through the MPLS domain, a second LSP Tunnel must be created in the opposite direction.

An LSP Tunnel is defined by a Destination Address (the IP address of the Egress LSR), and a Tunnel ID. At a finer level of granularity are LSP IDs. Essentially, these LSP IDs can serve to provide a set of aliases for alternate hop-by-hop paths between a single pair of Ingress and Egress LSRs, and therefore exist within the same LSP Tunnel.

Note: Ingress LSRs and Egress LSRs are also known as Label Edge Routers (LERs).

Two principal RSVP-TE message types are used to establish LSP Tunnels:

- PATH message. A PATH message is generated by the ingress router and sent toward
  the egress router. This is termed the *downstream* direction. This PATH message is a
  request by the sending LSR for the establishment of an LSP to the egress router. Each
  LSR in the path to the destination router digests the PATH message and does one of
  three things:
  - If the LSR cannot accommodate the request, it rejects the request by sending a PATH\_ERR message back to the source indicating the nature of the rejection.
  - If the LSR is not the egress router, it sends a PATH message to the next LSR toward the destination router.
  - If the LSR is the egress router, it should respond with a RESV message back to its most recent neighbor.

• RESV message. A RESV message is generated by the egress router and sent over the reverse path that the PATH messages took. This is termed the *upstream* direction.

An additional *HELLO* message is used between neighbor LSRs to ensure that LSRs are alive. This allows for quick tunnel replacement in the case of link or router failure.

A set of labels is passed in the RESV messages sent upstream from the egress to the ingress router. A label is sent from one LSR to its upstream neighbor telling the upstream router which label to use when later sending downstream traffic.

Three scenarios are currently supported to test MPLS/RSVP-TE on a DUT using Ixia equipment:

- 1. The DUT acts as the Ingress LSR, and the Egress LSR is simulated by an Ixia port.
- 2. The DUT acts as the Egress LSR, and the Ingress LSR is simulated by an Ixia port.
- 3. The DUT acts as a Transit/Intermediate LSR, and the Ingress and Egress LSRs are simulated by Ixia ports.

## **PATH Messages**

PATH messages contain a number of objects which define the tunnel to be established. These are shown in the following table.

RSVP-TE PATH Message Objects

Object	Contents	Usage
SESSION		Describes the destination router and associates a tunnel ID with the session.
	tunnel end- point	The destination router's IP address.
	tunnel ID	A unique LSP tunnel ID.
SENDER_ TEMPLATE		The description of the sender.
	tunnel sender address	The sender router's IP address.
	LSP ID	A unique LSP ID.
LABEL_ REQUEST		Asks all the LSRs to send back label values through RESV messages.
SENDER_ TSPEC andADSPEC		Both of these objects deal with bandwidth and other QoS requirements for the path.
TIME_ VALUES		Timing values related to the refresh of tunnel information.
	refresh interval	The interval between messages.

Object	Contents	Usage
EXPLICIT_ ROUTE		Allows the sender to request that the LSP tunnel follow a specific path from ingress to egress router. See <a href="Explicit_Route">Explicit_Route</a> for more details.
SESSION_ ATTRIBUTE		Other attributes associated with the session: tunnel establishment priorities, session name, and optionally resource affinity.
RSVP_HOP		Describes the immediate upstream router's address to the downstream router.

## **Explicit\_Route**

An explicit route is a particular path in the network topology. Typically, the explicit route is determined by a node with the intent of directing traffic along that path. An explicit route is described as a list of groups of nodes along the explicit route. In addition to the ability to identify specific nodes along the path, an explicit route can identify a group of nodes that must be traversed along the path. Each group of nodes is called an *abstract node*. Thus, an explicit route is a specification of a set of abstract nodes to be traversed.

There are three types of objects in an explicit route:

- IPv4 prefix
- IPv6 prefix
- · Autonomous system number

Each node has a *loose* bit associated with it. If the bit is not set, the node is considered *strict*. The path between a strict node and its preceding node may only include network nodes from the strict node and its preceding abstract node. The path between a loose node and its preceding node may include other network nodes that are not part of the strict node or its preceding abstract node.

## **RESV Message**

The RESV message contains object that indicate the success of the PATH request and the details of the assigned tunnel. These are shown in the following table.

RSVP-TE RESV Message Objects

Object	Usage
SESSION	Indicates which session is being responded to.
TIME_VALUES	As in the PATH message but from the downstream LSR to the upstream LSR.
STYLE	The type of reservation assigned by the egress router. This relates to whether individual tunnels are requested for each sender-destination connection or whether some connections may use the same tunnel.
FILTER_SPEC	The sender router's IP address and the LSP ID.
LABEL	The label value assigned by the downstream router for use by the

Object	Usage
	upstream router.
RECORD_ROUTE	If requested, the complete route from the destination back to the source. The contents of this object include the IP addresses in either v4 or v6 format of all the LSRs encountered in the formation of the LSP, and optionally the labels used at each step. Each LSR on the upstream path perpends its own address information.
RESV_CONF	If present, it indicates that the ingress router should send a RESV_CONF message in response to the destination to indicate that the tunnel has been completely established.

## **Other Messages**

Several additional messages are used in RSVP-TE, as explained in the following table.

Additional RSVP-TE Messages

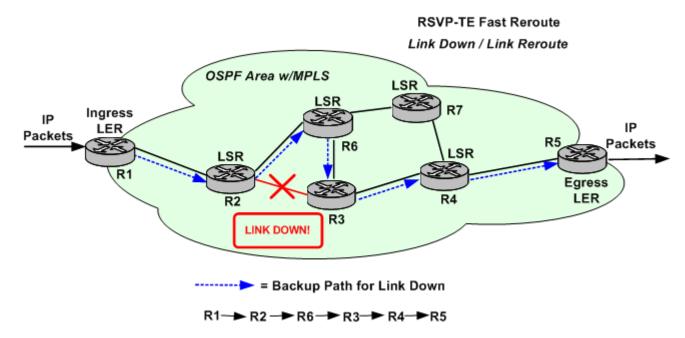
Message	Usage
PATH_ERR	Any LSR may determine that it cannot accommodate the tunnel requested in a PATH message. In this case it sends a PATH_ERR message back to the sender.
PATH_TEAR	When a sender router determines that it wants to tear down a tunnel, it sends a PATH_TEAR message to the destination router.
RESV_ERR	If a router cannot handle a reservation, it sends a RESV_ERR back to the destination router.
RESV_TEAR	When a destination router determines that it wants to tear down a tunnel, it sends a RESV_TEAR message upstream to the source router.
RESV_CONF	When requested, a sender router responds to the destination router with a RESV_CONF message to indicate that a complete tunnel has been successfully established.

#### **RSVP-TE Fast Reroute**

RSVP-TE Fast Reroute allows to configure backup LSP tunnels to provide local repair/protection ONLY for **explicitly-routed** LSPs/LSP tunnels, termed *protected LSPs* as described in IETF DRAFT draft-ietf-mpls-rsvp-lsp-fastreroute-03.

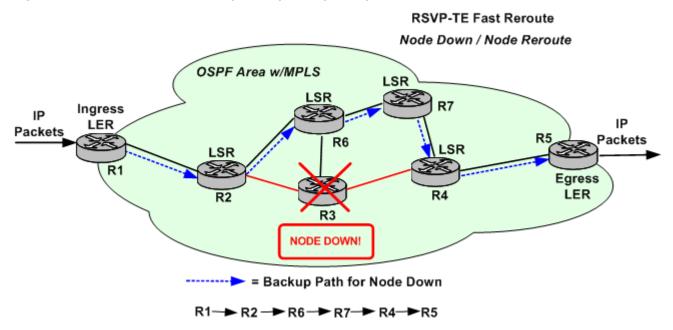
An example diagram of a backup scenario for rerouting around a downed link, using an LSP Detour, is shown in the following figure.

Figure: RSVP-TE Fast Reroute Backup Link (Detour) Example



The following image shows an example diagram for a backup scenario to reroute around a downed node, using an LSP Detour.

Figure: RSVP-TE Fast Reroute Backup Node (Detour) Example



The one-to-one backup method is based on including a DETOUR object in the Path message. The head-end router, the Point of Local Repair (PLR), sets up a separate detour LSP for each LSP it protects. For the Facility backup method, the PLR sets up a tunnel to protect multiple LSPs simultaneously, by using the MPLS label stack.

#### **Ixia Test Model**

The Ixia test process is designed so as to fully exercise RSVP functionality in MPLS routers. An Ixia port can simulate any number of LSR routers at the same time. Each router operates in an ingress or egress mode. In the following discussion, LSRs I and II refer to the figure in RSVP-TE Overview.

- Ingress mode: LSRs I and II are termed a neighbor pair, where LSR I is the upstream router being simulated and LSR II is its immediate downstream neighbor. The Ixia port generates the PATH and HELLO messages that LSR I would send. LSR II is the Device Under Test (DUT) and may be an egress router or be connected to other LSRs, as shown in the figure.
- Egress mode: the Ixia port simulates LSR II while LSR I is the DUT. The Ixia port interprets PATH messages that it receives to determine if they are directed for any of the defined destination routers. If that is the case, it responds with appropriate RESV messages.

If requested, HELLO messages are generated and responded to in either mode.

When the Ixia port operates in Ingress mode, it attempts to set up LSP tunnels for each combination of sender router and destination router, using any number of LSP tunnels and any number of LSP IDs for each LSP tunnel. Thus the number of PATH messages that the Ixia port attempts to generate for each refresh interval is:

# of sender routers
x # of destination routers
x # of LSPs
x # of LSP tunnels

The protocol server records all labels and other information that it receives on behalf of its simulated routers and displays those in a convenient format.

### **LDP**

The Label Distribution Protocol (LDP) version 1, defined in RFC 3036, works in conjunction with Multi-Protocol Label Switching (MPLS), to efficiently `tunnel' IP traffic across backbone topologies between Label Switching Routers (LSRs).

MPLS forwards packets based on added labels, so IP routing table lookups are not required along the length of the tunnel. RFC 3031 defines Forwarding Equivalence Classes (FECs) for use with MPLS, for purposes such as Quality of Service (QoS). LDP utilizes this option, assigning an FEC to every Label Switched Path (LSP) it sets up.

The LDP protocol creates peer sessions through a bidirectional exchange of messages, which include label requests and labels. While the initial Hello messages are based on UDP and sent to well-known port `646,' all other messages are based on TCP.

The following global timers can be configured: Hello Hold timer, Hello Interval timer, Keep-Alive Hold timer, and KeepAlive Interval timer. The values for these timers can be entered by you, but the final values are negotiated during the Discovery and Session setup processes. When the LDP remote peer has a timeout value which is lower than the one configured for the local LDP router, the lower value is used by both peers.

Virtual Circuit (VC) Ranges of MAC Addresses can be created to simulate Virtual Private LAN Services (VPLS), where L2 PDUs can be carried over VC LSPs, which, in turn, are carried over MPLS. This creates a `bridged,' Ethernet Layer Two Virtual Private Network (Ethernet L2VPN). Refer to IETF DRAFT draft-lasserre-vkompella-ppvpn-vpls-03, which defines the VC Type - Ethernet VPLS, and also discusses the use of MPLS transport tunnels by pseudowires (PWs).

A pseudowire is a logical link through the tunnel, made up of two parallel VC LSPs using the same VC Identifier (VCID), as shown in the following figures.

Figure: LDP VPLS Example

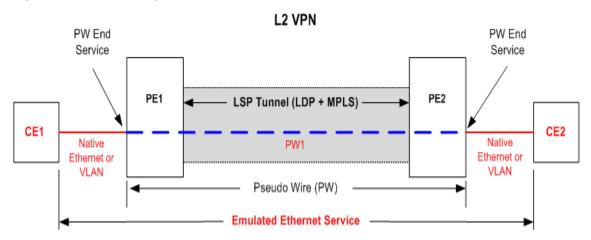
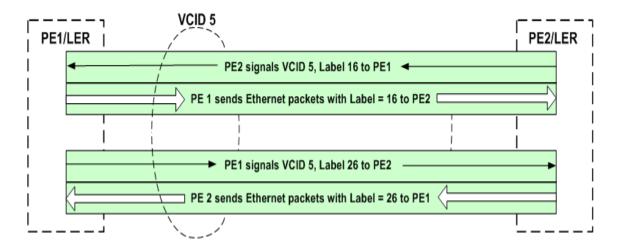


Figure: LDP VPLS Pseudowire Diagram

One Pseudo Wire (PW) = 2 VC Labels (1 in each direction)



#### **MLD**

The Multicast Listener Discovery (MLD) protocol is integral to the operation of Internet Protocol Version 6 (IPv6). MLDv1 is defined by RFC 2710, while MLDv2 is defined by RFC 3810. The MLD operations are based on operations similar to the Internet Group Management Protocol (IGMP) that supports IPv4. MLDv2 corresponds to IGMPv3. Both versions are supported by the protocol server.

An IPv6 router uses MLD to: (1) discover multicast listeners (nodes) on the directly attached links, and (2) find out which multicast addresses those nodes have interest in. In MLDv2, nodes can indicate interest in listening to packets that are sent to a specific multicast address from a filtered group of source IP addresses. This filtering can be based on `all but' (Excluding) or `only' (Including) certain source addresses. Host nodes can only be multicast `listeners,' while the multicast routers can act as routers or listeners.

## PIM-SM/SSM-v4/v6

Protocol Independent Multicast - Sparse Mode (PIM-SM) Version 2 protocol is designed for multicast routing, and is defined in RFC 2362. IETF DRAFT draft-ietf-pim-sm-v2-new-06.txt is being designed to obsolete RFC 2362.

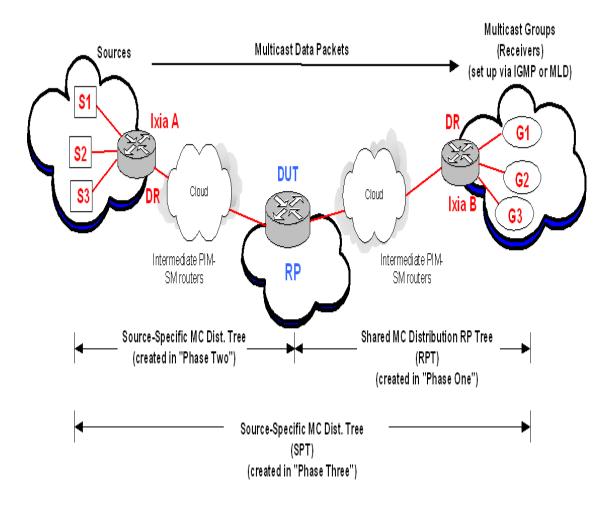
There is one Rendezvous Point (RP) per multicast group, and this router serves as the root of a unidirectional *shared* distribution tree whose `leaves' consist of multicast receivers. In addition, PIM-SM can create an optional shortest-path tree for an *individual* source (where the source is the root). The term *upstream* is used to indicate the direction toward the root of the tree; *downstream* indicates the direction away from the root of the tree. The address of the RP can be configured statically by an administrator, or configured through a Bootstrap router (BSR) mechanism.

PIM-SM can use two sources of topology information to populate its routing table, the Multicast Routing Information Base (MRIB): unicast or multicast-capable. In a LAN where there are multiple PIM-SM routers and directly-

connected hosts, one of the routers is elected as Designated Router (DR) to act on the behalf of the hosts.

The following diagram shows a simplified PIM-SM test setup using Ixia ports.

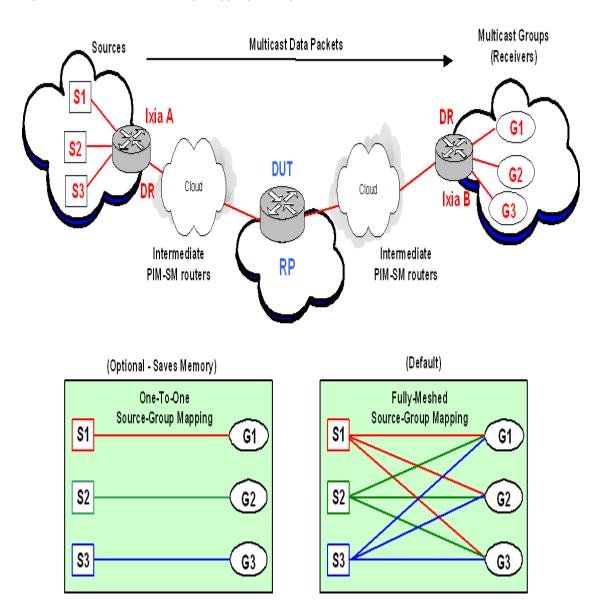
Figure: PIM-SM Diagram



#### **PIM-SM Source-Group Mapping**

PIM-SM Source-Group mapping involves the pairing of Sources and Groups. The default method is a fully-meshed mapping of sources to groups, where every source is paired with every group. For a situation where there are `X' number of sources and `Y' number of groups, there will be `X x Y' number of mappings, resulting in a great deal of memory usage for processing. When full-mesh mapping is not desired, the optional `One-To-One' Source-Group Mapping can be used to save memory. In comparison, if a one-to-one type mapping behavior was preferred and only a full-mesh setup was available, you would have to create `N' fully-meshed source-group mapping ranges of size `1' to emulate the one-to-one behavior. An example showing the differences between the two types of mapping is shown in the following figure.

Figure: PIM-SM Source-Group Mapping Example

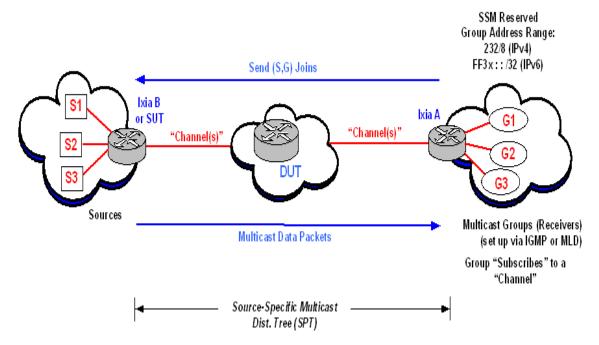


#### **PIM-SSM**

Protocol Independent Multicast - Source-Specific Multicast (PIM-SSM) uses a subset of the PIM-SM protocol, described in draft-ietf-ssm-arch-06, Source-Specific Multicast for IP, and in Section 4.8 of draft-ietf-pim-sm-v2-new-11, Protocol Independent Multicast - Sparse Mode (PIM-SM): Protocol Specification (Revised).

PIM-SSM is useful for broadcast-type applications, where one source sends packets to many host groups. There is no shared distribution tree topology, but there is a shortest-path tree (SPT) established, where the source is the root of the tree. In the case of SSM, the usual PIM-SM multicast terminology is modified, and the term *Channel* is used instead of *Group* and *Subscription* replaces *Join*. A multicast group (G) router that wants to receive packets from a specific Source (S) for its hosts/listeners, will `Subscribe' to `Channel (S,G).' An example of an PIM-SSM topology is shown in the following figure.

Figure: PIM-SSM Topology Example



An existing PIM-SM network can be modified to run SSM by enabling PIM-SSM on the source and destination/group routers. The typical PIM-SM signaling is not used for PIM-SSM, since the role of Rendezvous Point (RP) router is eliminated. The Subscribe (Join) message travels directly from the Destination router to the Source router, and data packets are transmitted in the opposite direction.

#### **PIM-SSM Addressing**

The PIM-SSM protocol uses a restricted addressing scheme, with reserved values for IPv4 SSM addresses defined by the IANA as 232.0.0.0 through 232.255.255.255 (232/8). IPv6 SSM addresses are defined in IETF DRAFT draft-ietf-ssm-arch- 06 and draft-ietf-pim-sm-v2-new-11 as FF3x: :/32. The range of FF3x: :/96 is proposed by RFC 3307, `Allocation Guidelines for IPv6 Multicast Addresses.'

#### **Differences Between PIM-SM and PIM-SSM**

Some of the principal differences between PIM-SM and PIM-SSM routers, per draft-ietf-ssm-arch-06, are mentioned in the following list:

- PIM-SSM-only routers must not send (\*,G) Join/Prune messages.
- PIM-SSM-only routers must not send (S,G,rpt) Join/Prune messages.
- PIM-SSM-only routers must not send Register messages for packets with SSM destination addresses.
- PIM-SSM-only routers must act in accordance with (\*,G) or (S,G,rpt) state by forwarding packets with SSM destination addresses.
- PIM-SSM-only routers acting as RPs must not forward Register messages for packets with SSM destination addresses.

#### **Protocol Elements for PIM-SSM**

Protocol elements *required* for PIM-SSM-only routers are mentioned in the following list:

- (S,G) Downstream and Upstream state machines.
- Hello messages, neighbor discovery, and DR election.
- Packet forwarding rules.
- [(S,G) Assert state machine]

Some of the Protocol elements **not required** for PIM-SSM-only routers are mentioned in the following list:

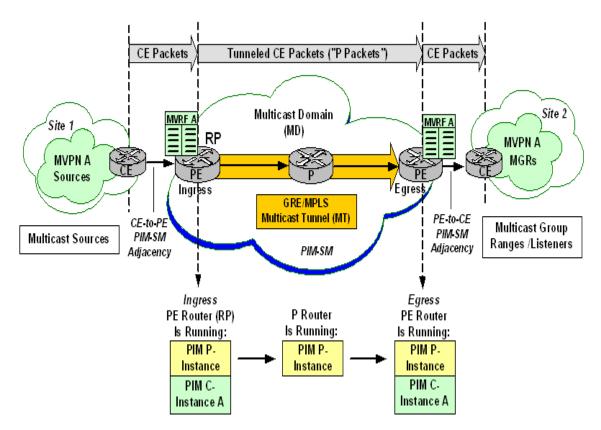
- · Register state machine
- (\*,G), (S,G,rpt), and (\*,\*,RP) Downstream and Upstream state machines.
- Keepalive Timer (treated as always running)
- SptBit (treated as always set for an SSM address)

#### **Multicast VPNs**

Multicast VPNs (MVPNs) can be created through the use of MP-BGP combined with PIM-SM. Multicast VPNs can be set up by a Service Provider to support scalable, IPv4 multicast traffic solutions, based on IETF draft-rosen-vpn-mcast-07, `Multicast in MPLS/BGP IP VPNs.'

Multicast VRFs (MVRFs) on each PE router contain multicast routing tables. Within a Service Provider's domain, each MVRF is assigned to a Multicast Domain (MD), which is a set of MVRFs that can send multicast traffic to one another. Multicast packets from CE routers are sent over a (GRE) multicast tunnel to other PE routers in the multicast domain. A simplified example of a Multicast VPN topology, with one MVPN, is shown in the following figure.

Figure: Multicast VPN Topology Example



Each CE and its connected PE set up a PIM-SM adjacency. However, CEs do not set up PIM-SM adjacencies with each other. Separate CE-associated instances of PIM are run by each PE router, and these are called `PIM C-instances.' Each C-instance is MVRF-specific. As each PE can be affiliated with many MVPNs/MVRFs, the router can run many PIM C-instances simultaneously, up to a maximum of one C-instance per MVRF.

PIM Provider-wide instances (`PIM P-instances') are run by each PE router, creating a global PIM adjacency with all of its IGP PIM-SM-enabled neighbors (P routers). P routers cannot set up PIM-SM C-instances.

At startup for the multicast domain's Provider Edge (PE) routers, the default Multicast Distribution Tree (MDT) is set up automatically. Each Multicast Domain is identified by a globally unique Service Provider (P) Group address and a Route Distinguisher. The MD group address is created by using BGP (L3 Site window). It is a valid 4-byte IPv4 multicast address prefix (for example, 239.1.1.1/32). The 12-byte Route Distinguisher is also created through BGP (L3 Site window). This Ixia implementation uses an RD value = 2. One C-Multicast Group Range (MGR) can be configured for each MVRF.

#### **MPLS**

Multi-Protocol Label Switching (MPLS) is based on the concept of label switching: and independent and unique `label' is added to each data packet and this label is used to switch and route the packet through the network. The label is simple, essentially a shorthand version of the packet's header information, so network equipment can be optimized around processing the label and forwarding traffic. This concept has been around the data communications industry for years. X.25, Frame Relay, and ATM are examples of label switching technologies.

It is important to understand the differences in the way MPLS and IP routing forward data across a network. Traditional IP packet forwarding uses the IP destination address in the packet's header to make an independent forwarding decision at each router in the network. These hop-by-hop decisions are based on network layer routing protocols, such as Open Shortest Path First (OPSF) or Border Gateway Protocol (BGP). These routing protocols are designed to find the shortest path through the network, and do not consider other factors, such as latency or traffic congestion.

MPLS creates a connection-based model overlaid onto the traditionally connectionless framework of IP routed networks. This connection-oriented architecture opens the door to a wealth of new possibilities for managing traffic on an IP network. MPLS builds on IP, combining the intelligence of routing, which is fundamental to the operation of the Internet and today's IP networks, with the high performance of switching. Beyond its applicability to IP networking, MPLS is being expanded for more general applications in the form of Generalized MPLS (GMPLS), with applications in optical and Time-Division Multiplexing (TDM) networks.

One of the primary original goals of MPLS, boosting the performance of software-based IP routers, has been superseded as advances in silicon technology have enabled line-rate routing performance implemented in router hardware. In the meantime, additional benefits of MPLS have been realized, notably Virtual Private Network (VPN) services and traffic engineering (TE).

#### **Advantages of MPLS**

Some of the advantages of using MPLS are:

- MPLS enables traffic engineering. Explicit traffic routing and engineering help squeeze more data into available bandwidth.
- MPLS supports the delivery of services with Quality of Service (QoS) guarantees.
   Packets can be marked for high quality, enabling providers to maintain a specified low end-to-end latency for voice and video.
- MPLS reduces router processing requirements, since routers simply forward packets based on fixed labels.

#### **How Does MPLS Work?**

MPLS is a technology used for optimizing forwarding through a network. Though MPLS can be applied in many different network environments, this discussion focuses primarily on MPLS in IP packet networks, by far the most common application of MPLS today.

MPLS assigns labels to packets for transport across a network. The labels are contained in an MPLS header inserted into the data packet.

These short, fixed-length labels carry the information that tells each switching node (router) how to process and forward the packets, from source to destination. They have significance only on a local node-to-node connection. As each node forwards the packet, it swaps the current label for the appropriate label to route the packet to the next node. This mechanism enables very-high-speed switching of the packets through the core MPLS network.

MPLS combines the best of both Layer 3 IP routing and Layer 2 switching. In fact, it is sometimes called a `Layer 2-1/2' protocol. While routers require network-level intelligence to determine where to send traffic, switches only send data to

the next hop, and so are inherently simpler, faster, and less costly. MPLS relies on traditional IP routing protocols to advertise and establish the network topology. MPLS is then overlaid on top of this topology. MPLS predetermines the path data takes across a network and encodes that information into a label that the network's routers can understand. This is the connection-oriented approach previously discussed. Since route planning occurs ahead of time and at the edge of the network (where the customer and service provider network meet), MPLS-labeled data requires less router horsepower to traverse the core of the service provider's network.

#### **MPLS Routing**

MPLS networks establish Label-Switched Paths (LSPs) for data crossing the network. An LSP is defined by a sequence of labels assigned to nodes on the packet's path from source to destination. LSPs direct packets in one of two ways: hop-by-hop routing or explicit routing.

#### **Hop-by-Hop Routing**

In hop-by-hop routing, each MPLS router independently selects the next hop for a given Forwarding Equivalency Class (FEC). A FEC describes a group of packets of the same type; all packets assigned to a FEC receive the same routing treatment. FECs can be based on an IP address route or the service requirements for a packet, such as low latency.

In the case of hop-by-hop routing, MPLS uses the network topology information distributed by traditional Interior Gateway Protocols (IGPs) routing protocols such as OPSF or IS-IS. This process is similar to traditional routing in IP networks, and the LSPs follow the routes the IGPs dictate.

#### **Explicit Routing**

In explicit routing, the entire list of nodes traversed by the LSP is specified in advance. The path specified could be optimal or not, but is based on the overall view of the network topology and, potentially, on additional constraints. This is called Constraint-Based Routing. Along the path, resources may be reserved to ensure QoS. This permits traffic engineering to be deployed in the network to optimize use of bandwidth.

#### **Label Information Base**

As the network is established and signaled, each MPLS router builds a Label Information Base (LIB), a table that specifies how to forward a packet. This table associates each label with its corresponding FEC and the outbound port to forward the packet to. This LIB is typically established in addition to the routing table and Forwarding Information Base (FIC) that traditional routers maintain.

Connections are signaled and labels are distributed among nodes in an MPLS network using one of several signaling protocols, including Label Distribution Protocol (LDP) and Resource reSerVation Protocol with Tunneling Extensions (RSVPTE). Alternatively, label assignment can be piggybacked onto existing IP routing protocols such as BGP.

The most commonly used MPLS signaling protocol is LDP. LDP defines a set of procedures used by MPLS routers to exchange label and stream mapping information. It is used to establish LSPs, mapping routing information directly to Layer 2 switched paths. It is also commonly used to signal at the edge of the MPLS network, the critical point where non-MPLS traffic enters. Such signaling is required when establishing MPLS VPNs.

RSVP-TE is also used for label distribution, most commonly in the core of networks that require traffic engineering and QoS. A set of extensions to the original RSVP protocol, RSVP-TE provides additional functionality beyond label distribution, such as explicit LSP routing, dynamic rerouting around network failures, preemption of LSPs, and loop detection. RSVP-TE can distribute traffic engineering parameters such as bandwidth reservations and QoS requirements.

Multi-protocol extensions have been defined for BGP, enabling the protocol to also be used to distribute MPLS labels. MPLS labels are piggybacked onto the same BGP messages used to distribute the associated routes. MPLS allows multiple labels (called a label stack) to be carried on a packet. Label stacking enables MPLS nodes to differentiate between types of data flows, and to set up and distribute LSPs accordingly. A common use of label stacking is for establishing tunnels through MPLS networks for VPN applications.

#### **BFD**

Bidirectional Forwarding Detection (BFD) is a network protocol used to detect faults between two forwarding engines. It provides low-overhead detection of faults even on physical media that don't support failure detection of any kind, such as ethernet, virtual circuits, tunnels and MPLS LSPs.

BFD establishes a session between two endpoints over a particular link. If more than one link exists between two systems, multiple BFD sessions may be established to monitor each one of them. The session is established with a three-way handshake, and is torn down the same way. Authentication may be enabled on the session. A choice of simple password, MD5 or SHA1 authentication is available.

BFD does not have a discovery mechanism; sessions must be explicitly configured between endpoints. BFD may be used on many different underlying transport mechanisms and layers, and operates independently of all of these. Therefore, it needs to be encapsulated by whatever transport it uses. For example, monitoring MPLS LSPs involves piggybacking session establishment on LSP-Ping packets. Protocols that support some form of adjacency setup, such as OSPF or IS-IS, may also be used to bootstrap a BFD session. These protocols may then use BFD to receive faster notification of failing links than would normally be possible using the protocol's own keepalive mechanism.

A session may operate in one of two modes: asynchronous mode and demand mode. In asynchronous mode, both endpoints periodically send Hello packets to each other. If a number of those packets are not received, the session is considered down.

In demand mode, no Hello packets are exchanged after the session is established; it is assumed that the endpoints have another way to verify connectivity to each other, perhaps on the underlying physical layer. However, either host may still send Hello packets if needed.

Regardless of which mode is in use, either endpoint may also initiate an Echo function. When this function is active, a stream of Echo packets is sent, and the other endpoint then sends these back to the sender through its forwarding plane. This is used to test the forwarding path on the remote system.

#### **CFM**

Ethernet CFM is an end-to-end per-service-instance Ethernet layer OAM protocol that includes proactive connectivity monitoring, fault verification, and fault isolation. End to end can be PE to PE or customer edge (CE) to CE. Per service instance means per VLAN.

Being an end-to-end technology is the distinction between CFM and other metro-Ethernet OAM protocols. For example, MPLS, ATM, and SONET OAM help in debugging Ethernet wires but are not always end-to-end. 802.3ah OAM is a single-hop and per-physical-wire protocol. It is not end to end or service aware. Ethernet Local Management Interface (E-LMI) is confined between the uPE and CE and relies on CFM for reporting status of the metro-Ethernet network to the CE.

Troubleshooting carrier networks offering Ethernet Layer 2 services can be difficult. Customers contract with service providers for end-to-end Ethernet service and service providers may subcontract with operators to provide equipment and networks. Compared to enterprise networks, where Ethernet traditionally has been implemented, these constituent networks belong to distinct organizations or departments, are substantially larger and more complex, and have a wider user base. Ethernet CFM provides a competitive advantage to service providers for which the operational management of link uptime and timeliness in isolating and responding to failures is crucial to daily operations.

#### FCoE and NPIV

IxExplorer provides GUI access to all Ixia platform functionality with full support for stateless FCoE functional and scalability testing. The FCoE and Priority Flow Control (PFC) and FCoE Initialization Protocol (FIP) features allow testing of FCoE switches running both FCoE traffic and traditional Ethernet traffic.

#### **Supported Load Modules**

The following Ixia load modules have the Fibre Channel over Ethernet (FCoE) capability:

- GXMR8-01 and GXM8XP-01, including 10GBASE-T versions LSM10GXM(R)8GBT-01
- GXMR4-01 and GXM4XP-01, including 10GBASE-T versions LSM10GXM(R)4GBT-01
- LSM10GXM2XP-01 and GXMR2-01, including 10GBASE-T versions LSM10GXM(R)2GBT-01
- LSM1000XMVDCx-01 load modules. 4-port, 8-port, 12-port, and 16-port
- LSM1000XMVDC4-NG load modules. 4-port

#### **Data Center Mode**

FCoE support requires a new port mode, Data Center Mode. You need to switch port mode between Normal Mode and Data Center Mode to use the desired features in each mode.

- Mode switching (to or from Data Center Mode) triggers an FPGA re-download.
- There is no Packet Stream Mode support in Data Center Mode; only Advanced Scheduler Mode is supported.
- Supports 4-Priority traffic mapping for frame size up to 9216-byte. The different frame size support is determined by a sub mode in Data Center Mode. This limitation applies to all frames in Data Center Mode, whether FCoE frame or not.

- Data Center Mode only supports auto instrumentation mode for both TX and RX.
- When the port is in Data Center Mode, both existing Ethernet frames and FCoE frames are generated.

#### **Priority Traffic Generation**

The scheduling function is based on the existing Advanced Scheduler. A new parameter called `Priority Group' has been added to each stream. You can map Priority Group to the priority field in the frame. The priority field in the same stream should not change (for example, if the priority is a VLAN priority field, then you cannot configure a UDF to control this field within a stream).

#### Priority-based Flow Control (PFC)

The Ixia port responds to either IEEE 802.3x pause frame or to IEEE 802.1Qbb Priority-based Flow Control (PFC) frame. The flow control type is determined by the selection made on the Flow Control tab of the Port Properties dialog, in IxExplorer.

#### **IxExplorer Reference**

See IxExplorer User Guide, Chapter 6 topic *Frame Data for FCoE Support*, subtopic *Priority-based Flow Control*.

#### **Fibre Channel over Ethernet**

When the port is in Data Center Mode, both existing Ethernet frames and FCoE frames are generated.

The Fibre Channel CRC is generated on the fly. This CRC is inserted at offset of Ethernet frame size minus 12 bytes. For example:

Ethernet Frame Size (bytes)	2000	2001	2002	2003
FC-CRC Offset in FCoE Frame (bytes)	1988	1989	1990	1991

The FC-CRC can be set to No Error or to Bad CRC.

#### **Packet View Support**

For Fibre Channel frame, there is no Extended Header and Optional Header support. It decodes only FC-2 Frame Header field.

#### **FCoE Initialization Protocol (FIP)**

FIP (FCoE Initialization Protocol) has been implemented (in addition to FCoE). It is used to discover and initialize FCoE capable entities connected to an Ethernet cloud.

#### **IxExplorer Reference**

See the IxExplorer User Guide, Chapter 6 topic Frame Data for FCoE Support.

#### **NPIV Protocol Interface**

NPIV stands for N\_Port ID Virtualization. These can be used to virtually share a single physical N\_Port. This allows multiple Fibre Channel initiators to occupy a single physical port, easing hardware requirements in SAN design. Up to 256 N\_Port\_IDs can be assigned to a single N\_Port. NPIV interfaces can be configured using the Protocol Interface Wizard.

See the topic NPIV Protocol Interface.in IxExplorer User Guide.

#### Precision Time Protocol (PTP) IEEE 1588v2

Precision Time Protocol (IEEE 1588v2) allows precise synchronization of clocks in measurement and controls systems implemented with technologies such as network communications, local computing and distributed objects. The protocol supports system wide synchronization accuracy in sub-microseconds range with minimal network and local clock computing resources. The protocol operates in master/subordinate configuration. IEEE1588 deploys Multicast over an Ethernet network, and devices such as routers and switches can sync to the provided timing source.

#### **Supported Load Modules**

The following Ixia load modules have the PTP capability:

- LSM1000XMV(R)16, XMV(R)12, XMV(R)8, XMV(R)4
- · Xcellon-Ultra XP, NP, and NG

#### **Supported Messages**

The following messages are supported between clocks participating in the PTP protocol.

- Event messages
  - Sync
  - Delay Request
- General Messages
  - Announce
  - Follow\_up
  - Delay\_Response

#### **Supported Features**

The following PTP features are supported.

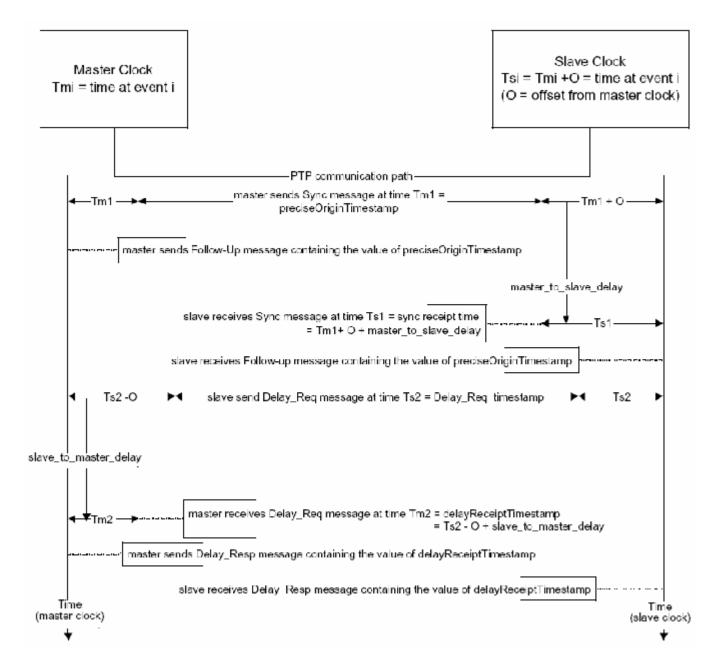
- Only one two-step clock is supported on an Ixia port, at this time. One-step clock is not supported.
- Ixia ports can run other (non-PTP) traffic along with PTP traffic. Ixia ports have the ability to throttle transmit based on flow control packets being received.
- IEEE 1588 version 2.2 in IPV4 (multicast) is supported.
- Ports are manually configured in Master or Subordinate mode.
- A histogram reporting Subordinate clock OFFSET from master is provided in the form of plot along with PTP messages transmitted and received.
- Aggregate statistics are displayed in Statistics View in IxExplorer.

- Session/Per Interface stats is displayed in IxNw/Tcl/csv file.
- Per Interface configuration is done in protocol interfaces.
- Ability to compose or decode PTP messages from the IxExplorer user interface.
- Negative testing is supported.
  - Programmable follow-up messages as a percentage of sync messages. See how dropping 10-90% of follow-up messages (while sending 100% of sync messages) affects the DUT.
  - Send follow-up messages with a bad packet.
  - Purposely send data with timestamps that include jitter (to try forcing a sync to fail).
  - Negative testing is done with packet streams/linux.

#### Local Clock synchronization through PTP to another PTP clock

The local clock of the is synchronized to the 's master clock by minimizing the Offset\_from\_master value of the current data set. The time and the rate characteristics of the local clock are modified upon receipt of either a sync message or follow-up message. The following figure illustrates the PTP communication path.

**Figure: PTP Communication Path** 



PTP Communication Path

Term	Value
sync_receipt_time = Ts1	Ts1 =Tm1+O+master_todelay
preciseOriginTimestamp = Tm1	Tm1
master_todelay (com- puted)	Ts1 Tm1
delay_req_sending_time = Ts2	Ts2
delayReceiptTimestamp	Tm2 = Ts2 O + _to_master_delay

Term	Value	
= Tm2		
_to_master_delay (com- puted)	Tm2 Ts2	
one_way_delay	{(master_todelay as computed) + (_to_master_delay as computed)}/2	
	{(Ts1-Tm1) + (Tm2-Ts2)}/2	
	{(O + master_todelay ) +	
	O +_to_master_delay)}/2	
	{(master_todelay ) + (_to_master_delay)}/2	
	master_todelay if path is symmetrical	



- 1. Offset shall be computed as O= Ts1-Tm1 one\_way\_Delay. Offset and One way delay shall be stored.
- 2. Offset correction shall be applied to the local clock.

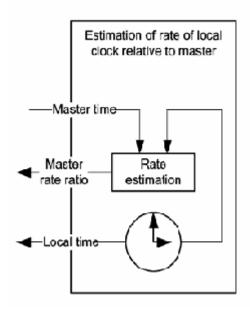
#### Local clock frequency transfer

In Slave mode of operation, the Ixia port implements a local clock in software (Linux). The frequency of the oscillator is not adjusted but allowed to free-run. The local clock shall be implemented based on time information synchronized from sync/follow\_up messages and hardware timestamps associated with these messages. The local clock is associated with a constant and a slope. The rate of a local clock relative to a master clock is illustrated in the figure below in IxExplorer References section.

#### **IxExplorer References**

See the IxExplorer User Guide, Chapter 10, Protocol Interfaces, especially topics *Protocol Interfaces Tab*, *PTP Discovered Information*, and *PTP Clock Configuration*.

Figure: Rate of Local Clock Relative to Master



- Clock = K+ Slope\*(TS-TS1),
- Slope = (T2-T1)/(TS2-TS1).
- K = T1

Where T1 is the time synchronized from the master and TS1 is the hardware timestamp associated with sync message 1. T2 and TS2 are corresponding parameters associated with sync message 2. T is the time at any point of time.

With a sync message, the parameters K and the slope are updated. The Clock Offset from master is calculated as discussed above and applied to K for correction.

Timestamps are cleared once when PTP is enabled.

In master mode of operation, server provides timestamp to the ports at the instant timestamps are cleared and slope is 1. OFFSET from master is 0.

If a GPS source is interfaced to the chassis, ports emulating the master are configured as Grand Master.

Local clock time format is seconds (32 bits) and nanoseconds (32 bits). The Ixia port supports a 2-step clock.

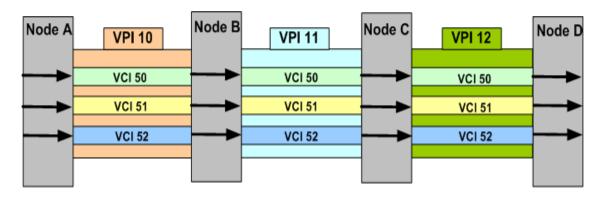
#### **ATM Interfaces**

On Asynchronous Transport Mode (ATM) is a Layer 2, connection-oriented, switching protocol, based on L2 Virtual Circuits (VCs). For operation in a connectionless IP routing or bridging environment, the IP PDUs must be encapsulated within the **payload field** of an ATM AAL5 CPCS-PDU (ATM Adaptation Layer 5 Common Part Convergence Sublayer Protocol Data Unit). The ATM CPCS-PDUs are divided into 48-byte segments which receive 5-byte headers to form 53-byte ATM cells.

The ATM cells are then switched across the ATM network, based on the Virtual Port Identifiers (VPIs) and the Virtual Connection Identifiers (VCIs). The relationship between VPIs (identifying one hop between adjacent nodes) and VCIs (identifying the end-to-end virtual connection) is illustrated in the following figure.

Figure: ATM VPI/VCI Pairs (PVCs)

# Node B VCIs VCIs



#### **Bridged ATM' Versus Routed ATM**

The ATM AAL5 frames allow for the overlay of the connectionless IP bridging or routing environment over the network of ATM nodes (that have frame handling capability). Each ATM node examines the payload of the AAL5 frame, and forwards the frame to the next node, based on the payload's MAC destination address (for IP bridging) or IP destination address (for IP routing). In effect, the ATM environment functions as a simulated Ethernet or IP network, respectively.

In the case of Label Distribution Protocol (LDP) routing over ATM, the process becomes more complex since MPLS tunnels are created over ATM core networks. For more information on the signaling, session setup, and label distribution for LDP routing over ATM, see the *IxNetwork Users Guide: Network Protocols - LDP chapter*.

#### **ATM Encapsulation Types**

There are two main types of ATM Multiplexing encapsulations defined by RFC 2684, `Multiprotocol Encapsulation over ATM Adaptation Layer 5.' The ATM AAL5 Frame is described in <u>"ATM Frame Formats" on page 192</u>. The various encapsulation types and references to diagrams of the encapsulated frame payloads are listed as follows:

- VC Multiplexing (VC Mux): used when only one protocol is to be carried on a single ATM VC. Separate VCs are used if multiple protocols are being transported.
  - "Figure: VC Mux IPv4 Routed" on page 194:
  - VC Mux IPv6 Routed
  - VC Mux Bridged Ethernet/802.3 (FCS)
  - VC Mux Bridged Ethernet/802.3 (no FCS)

- Logical Link Control (LLC): used for multiplexing multiple protocols over a single ATM virtual connection (VC).
  - LLC Routed AAL 5 Snap
  - LLC Bridged Ethernet (FCS)
  - LLC Bridged Ethernet (no FCS)

NOTE

The Protocol Configuration Wizards for BGP, OSPFv2, and ISIS allow configuration on ATM ports, but **ONLY** for the VC Mux Bridged Ethernet/802.3 (FCS) encapsulation type.

#### **Encapsulation Types by Protocol**

The types of RFC 2684 ATM encapsulations available for each Ixia routing protocol emulation are listed in the following table.

ATM Encapsulations for Protocols		
Routing Pro- tocol	ATM Encapsulation Type	
BGP	<ul> <li>Bridged ATM':</li> <li>VC Mux Bridged Ethernet/802.3 (FCS) - (the default)</li> <li>VC Mux Bridged Ethernet/802.3 (no FCS)</li> <li>LLC Bridged Ethernet (FCS)</li> <li>LLC Bridged Ethernet (no FCS)</li> <li>Routed ATM':</li> <li>VC Mux IPv4 Routed</li> <li>VC Mux IPv6 Routed</li> <li>LLC Routed AAL5 Snap</li> </ul>	
OSPF (v2 only)  NOTE Supported for both Point-to-Point and Point-to-MultiPoint links.	<ul> <li>`Bridged ATM':</li> <li>VC Mux Bridged Ethernet/802.3 (FCS) - (the default)</li> <li>VC Mux Bridged Ethernet/802.3 (no FCS)</li> <li>LLC Bridged Ethernet (FCS)</li> <li>LLC Bridged Ethernet (no FCS)</li> <li>`Routed ATM':</li> <li>VC Mux IPv4 Routed</li> <li>LLC Routed AAL5 Snap</li> </ul>	
Note: Discovery Mode must be set to Basic, and Advertising Mode must be set to Downstream on Demand (DoD).	<ul> <li>`Bridged ATM':</li> <li>VC Mux Bridged Ethernet/802.3 (FCS) - (the default)</li> <li>VC Mux Bridged Ethernet/802.3 (no FCS)</li> <li>LLC Bridged Ethernet (FCS)</li> <li>LLC Bridged Ethernet (no FCS)</li> <li>`Routed ATM':</li> </ul>	

Routing Pro- tocol	ATM Encapsulation Type
	<ul><li>VC Mux IPv4 Routed</li><li>LLC Routed AAL5 Snap</li></ul>
	`Bridged ATM':
RSVP-TE	<ul> <li>VC Mux Bridged Ethernet/802.3 (FCS) - (the default)</li> <li>VC Mux Bridged Ethernet/802.3 (no FCS)</li> <li>LLC Bridged Ethernet (FCS)</li> <li>LLC Bridged Ethernet (no FCS)</li> </ul>
	`Bridged ATM':
ISIS	<ul> <li>VC Mux Bridged Ethernet/802.3 (FCS) - (the default)</li> <li>VC Mux Bridged Ethernet/802.3 (no FCS)</li> <li>LLC Bridged Ethernet (FCS)</li> <li>LLC Bridged Ethernet (no FCS)</li> </ul>
	`Bridged ATM':
RIP	<ul> <li>VC Mux Bridged Ethernet/802.3 (FCS) - (the default)</li> <li>VC Mux Bridged Ethernet/802.3 (no FCS)</li> <li>LLC Bridged Ethernet (FCS)</li> <li>LLC Bridged Ethernet (no FCS)</li> </ul>
	`Bridged ATM':
RIPng	<ul> <li>VC Mux Bridged Ethernet/802.3 (FCS) - (the default)</li> <li>VC Mux Bridged Ethernet/802.3 (no FCS)</li> <li>LLC Bridged Ethernet (FCS)</li> <li>LLC Bridged Ethernet (no FCS)</li> </ul>
	`Bridged ATM':
IGMP	<ul> <li>VC Mux Bridged Ethernet/802.3 (FCS) - (the default)</li> <li>VC Mux Bridged Ethernet/802.3 (no FCS)</li> <li>LLC Bridged Ethernet (FCS)</li> <li>LLC Bridged Ethernet (no FCS)</li> </ul>
	`Bridged ATM':
MLD	<ul> <li>VC Mux Bridged Ethernet/802.3 (FCS)-(the default)</li> <li>VC Mux Bridged Ethernet/802.3 (no FCS)</li> <li>LLC Bridged Ethernet (FCS)</li> <li>LLC Bridged Ethernet (no FCS)</li> </ul>
	`Bridged ATM':
PIM-SM	<ul><li>VC Mux Bridged Ethernet/802.3 (FCS)-(the default)</li><li>VC Mux Bridged Ethernet/802.3 (no FCS)</li></ul>

ATM Encapsulation Type	
<ul><li>LLC Bridged Ethernet (FCS)</li><li>LLC Bridged Ethernet (no FCS)</li></ul>	

#### **ATM Frame Formats**

The image below shows the format of the <u>"Figure: ATM AAL5 CPCS-PDU (ATM AAL5 Frame)" below</u>. The formats of the various types of AAL5 CPCS-PDU payloads for these frames are shown in the following diagrams:

- · BRIDGED:
  - "Figure: VC Mux Bridged Ethernet/802.3 (FCS)" below
  - "Figure: VC Mux Bridged Ethernet/802.3 (no FCS)" on the facing page
  - "Figure: LLC Bridged Ethernet (FCS)" on the facing page
  - "Figure: LLC Bridged Ethernet (no FCS)" on the facing page
- ROUTED:
  - "Figure: VC Mux IPv4 Routed" on page 194
  - "Figure: VC Mux IPv6 Routed" on page 194
  - "Figure: LLC Routed AAL5 Snap" on page 194

Figure: ATM AAL5 CPCS-PDU (ATM AAL5 Frame)

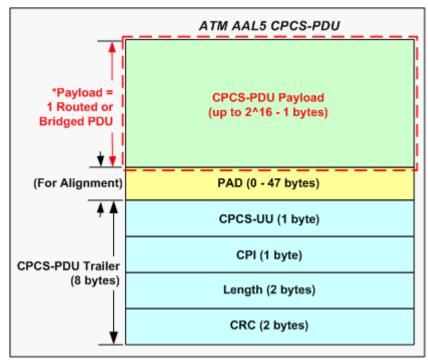


Figure: VC Mux Bridged Ethernet/802.3 (FCS)

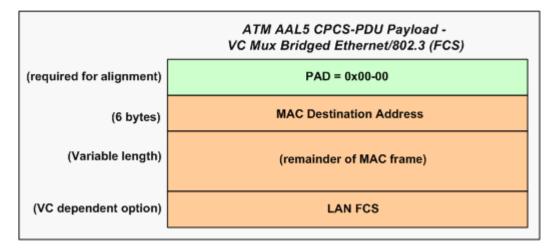


Figure: VC Mux Bridged Ethernet/802.3 (no FCS)

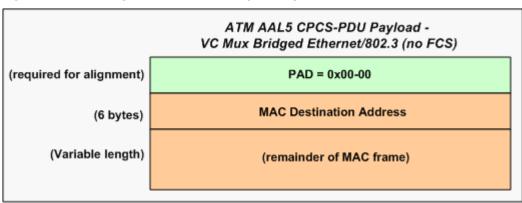


Figure: LLC Bridged Ethernet (FCS)

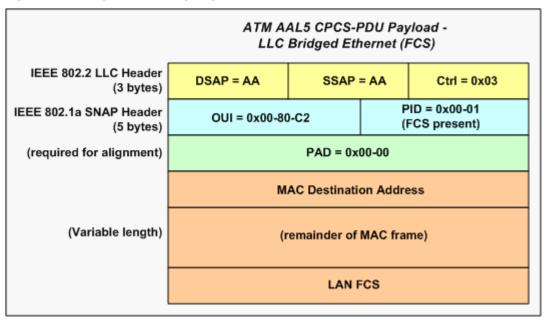


Figure: LLC Bridged Ethernet (no FCS)

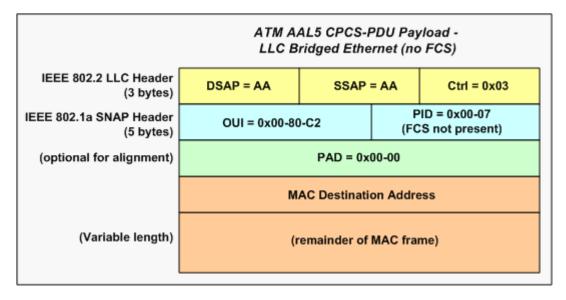


Figure: VC Mux IPv4 Routed

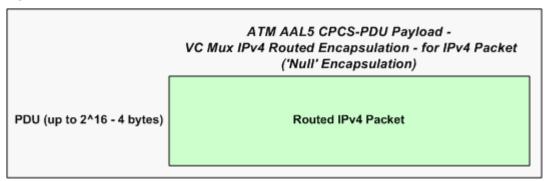


Figure: VC Mux IPv6 Routed

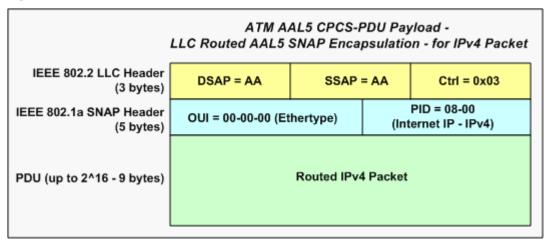
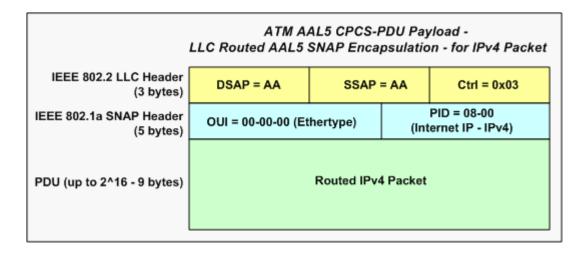


Figure: LLC Routed AAL5 Snap



#### **Generic Routing Encapsulation (GRE)**

RFC 2784, `Generic Routing Encapsulation' (GRE), provides a mechanism for encapsulating a payload packet to send that packet over a network of a different type. First, a GRE header is prepended to the payload packet, and the Ethertype for the protocol used in that packet is included in the GRE header. Then, a Delivery header is prepended to the GRE header, which adds a Layer 2 Data Link Layer address plus a Layer 3 Network address (for a network protocol in this implementation, either IPv4 or IPv6). After a GRE-encapsulated payload packet has reached the last router of the GRE `tunnel,' this router removes the GRE header and forwards the payload as a `normal' packet for the native protocol in the network.

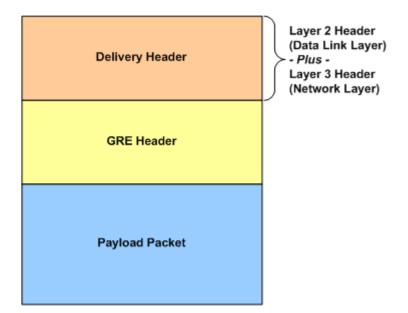
This is a relatively simple type of encapsulation and can be used to transparently carry packets for many different protocols, since it is based on Ethertypes. The original specifications for this encapsulation were RFC 1701, `Generic Routing Encapsulation (GRE),' published in 1994, and RFC 1702, `Generic Routing Encapsulation over IPv4 Networks,' also published in 1994.

RFC 2890, `Key and Sequence Number Extensions to GRE,' provides optional fields for identifying individual traffic flows within a GRE tunnel through an authentication key value, and for monitoring the sequence of packets within each GRE tunnel.

#### **GRE Packet Format**

Both control and data packets can be GRE-encapsulated. The overall format of a GRE-encapsulated packet is shown in the following figure.

Figure: GRE-Encapsulated Packet



#### **GRE Packet Headers**

There are two formats for the GRE Packet Headers:

- GRE Header per RFC 2784
- GRE Header per RFC 2890

#### **GRE Header per RFC 2784**

The format of a GRE packet header per RFC 2784 is shown in the following figure.

Figure: GRE Packet Header (per RFC 2784)

	0		15	16 31
	С	Reserved0	Ver	Protocol Type
I	Checksum (optional)			Reserved1 (optional)

The fields in the GRE header, per RFC 2784, are described in the following table.

GRE Header Fields (per RFC 2784)

Field	Description
	The Checksum Present flag bit.
С	If set (= 1), the Checksum and Reserved1 fields are present, and the information in the Checksum field is valid.
Reserved0	<ul> <li>(Bits 1 - 12)</li> <li>Bits 1 - 5 unless the receiver is implementing RFC 1701, the receiver must discard the packet if any of these bits are non-zero.</li> <li>Bits 6 - 12 reserved for future use.</li> </ul>
Ver	The Version Number field.  The value must be zero.

Field	Description
	Protocol Type field.
Protocol Type	The protocol type of the payload packet. These values are defined in RFC 1700, `Assigned Numbers' and by the IANA `ETHER TYPES' document.
	When the payload is an IPv4 packet, the protocol type must be set to 0x800 (Ethertype for IPv4).
	(Optional)
Checksum	The IP (one's complement) checksum of all of the 16-bit words in the GRE header and the payload packet. The value of the checksum field = zero for the purpose of computing the checksum.
	The checksum field is present only if Checksum Present bit is set (= 1).
	(Optional)
	These bits are reserved for future use.
Reserved1	This field is present only if the Checksum field is present (that is, the Checksum Present bit = 0).
	If present, this field must be transmitted as zero.

#### **GRE Header per RFC 2890**

The format of a GRE header, with added information per RFC 2890, is shown in the following figure.

Figure: GRE Header (per RFC 2890)

0	15 16			31	
С	кѕ	Reserved0	Ver	Protocol Type	
	Checksum (optional)			Reserved1 (optional)	
	Key (optional)				
	Sequence Number (optional)				

The fields in the GRE header, per RFC 2890, are described in the following table.

GRE Header Fields (per RFC 2890)

Field	Description		
	The Checksum Present flag bit.		
С	If set (= 1), the Checksum field and the Reserved1 is present, and the information in the Checksum field is valid.		
	Bits 1 - 12.		
Reserved0	For bits 1 - 5, unless the receiver is implementing RFC 1701 the receiver must discard the packet if any of these bits are non-zero.		

Field	Description
F	For bits 6 - 12, these bits are reserved for future use.
	The Key Present flag bit.
K	If set (= 1), the Key field is present. If not set (= 0), this field is not present.
	(Compatible with RFC 1701)
	The Sequence Number Present flag bit.
	If set (= 1), the Sequence Number Present field is present. If not set (= 0), this field is not present.
	(Compatible with RFC 1701)
Ver	The Version Number field.
	The value must be zero.
F	Protocol Type field.
Protocol Type i	The protocol type of the payload packet. These values are defined in RFC 1700, `Assigned Numbers' and by the IANA `ETHER TYPES' document (located at www.iana.org/assignments/ethernet-numbers).
	When the payload is an IPv4 packet, the protocol type must be set to 0x800 (Ethertype for IPv4).
(	(Optional)
Checksum	The IP (one's complement) checksum of all of the 16-bit words in the GRE header and the payload packet. The value of the checksum field = zero for the purpose of computing the checksum.
	The checksum field is present only if Checksum Present bit is set $(= 1)$ .
(	(Optional)
	These bits are reserved for future use.
	This field is only present if the Checksum field is present (that is, the Checksum Present bit $= 0$ ).
1	If present, this field must be transmitted as zero.
(	(Optional)
	This field is present only if the Key Present bit is set (= 1).
t t	A 4-octet number that can be used to identify an individual, logical traffic flow within the GRE tunnel. The encapsulator/sender uses the same key value for all packets within a single flow, for identification by the decapsulator/receiver.
Sequence Number (	(Optional)

Field	Description	
Present	This field is present only if the Sequence Number Present bit is set $(= 1)$ .	
	A 4-octet number that can be used to identify the order of transmission of the packets, with the goal of providing unreliable, but in-order delivery of packets.	
	The decapsulator/receiver uses the sequence number to monitor the order of the packets as they are received. Out-of-sequence packets should be silently discarded.	
	The sequence number of the first packet = 0. The value range is from 0 to $(2 ** 32) -1$ .	

#### **DHCP Protocol**

Dynamic Host Configuration Protocol (DHCP) is defined in RFC 2131, and it is based on earlier work with the protocol for BOOTP relay agents, which was specified in RFC 951. A DHCP Server provides permanent storage and dynamic allocation of IPv4 network addresses and other network configuration information. A DHCP Server is a host, and a DHCP Client is also a host. This protocol is designed for allocating IPv4 addresses to hosts, but not to routers.

A Client Identifier (Client ID) is required so that the DHCP Server can match a DHCP client with its `lease.' If the Client does not supply a Client Identifier option, the Client Hardware MAC Address (chaddr) is used by the Server to identify the Client. A lease is the period of time that a DHCP Client may use an IPv4 address that has been allocated by the DHCP Server. This lease period may be extended, and may even be set to `infinity' (0xffffffff hex), to indicate a `permanent' IPv4 address allocation.

DHCP messages are exchanged between client and server using UDP as the transport protocol. The DHCP Server port is UDP Port 67, and the DHCP Client port is UDP Port 68.

DHCPDISCOVER messages are broadcast by the Client on the local subnet, to reach the DHCP Server. Suggested values for a network address and lease period may be included in the Discover message. The Server(s) may respond with a DHCPOFFER message. The Offer message includes available IPv4 network address, plus configuration parameters contained in the DHCP options (TLVs/objects).

You will not be able to select DHCP-enabled protocol interfaces for use with Ixia protocol emulations, with the exception of IGMP.

#### **DHCPv6 Protocol**

The Dynamic Host Control Protocol for Version 6 (DHCPv6) is defined in RFC 3315. DHCPv6 uses UDP packets to exchange messages between servers and clients. The servers provide IPv6 addresses and additional configuration information to clients. A DHCPv6 server listens on a reserved, link-scope multicast address. A client identifies itself to the server by a link-local source address.

The groups of IPv6 addresses managed by the servers and clients are called Identity Associations (IAs), where each IA has a unique identifier. IA\_NAs are identity associations of

non-temporary (permanent) IPv6 addresses. IA\_TAs are identity associations of temporary addresses.

RFC 3633, `IPv6 Prefix Options for Dynamic Host Configuration Protocol (DHCP) Version 6,' adds capability for *automated* allocation of IPv6 prefixes from a delegating router to a requesting router. IA\_PDs are identity associations used for delegated IPv6 address prefixes.

The setup for DHCPv6 involves a four-message exchange `handshake.' Maintaining the DHCPv6 client-server relationship, and managing the return or deletion of IPv6 addresses involves three additional messages. These messages are described in the following list:

Message exchange (handshake):

- SOLICIT: Client sends a DHCPv6 SOLICIT message to the all DHCPv6 Agents multicast address to locate suitable servers.
- ADVERTISE: Multiple servers respond to the client's SOLICIT message by sending an ADVERTISE message to the client. The Client receives and stores ADVERTISE messages until the first retransmit timeout for SOLICIT messages, then accepts the message with the highest preference value. Or, the client immediately accepts an ADVERTISE message that has the preference value set to 255.
- REQUEST: Client sends a REQUEST message to the DHCPv6 server that has the highest preference value.
- REPLY: Server responds to the client's REQUEST message with a REPLY message containing the IPv6 address and configuration parameters required by the client.

Additional messages for Maintenance/Return/Deletion of Addresses:

- RENEW: Client sends a RENEW message to the assigned server after the Renew time specified for the IA. The server may respond with a REPLY message.
- REBIND: If the client does not receive a response (REPLY) from the primary (assigned) server, it multicasts a REBIND packet according to the Rebind time specified for the IA. The server(s) may each respond with a REPLY message.
- RELEASE: Client sends a RELEASE message to return one or more IPv6 addresses to the server when it has completed using the IPv6 address(es).
- **Note**: If the client does not receive any REPLY messages from the server in response to its RENEW or REBIND messages, the client deletes the assigned addresses according to the valid lifetimes of the addresses.

#### **Ethernet OAM**

The IEEE Std 802.3ah Operations, Administration, and Maintenance (OAM) sublayer provides mechanisms useful for monitoring link operation such as remote fault indication and remote loopback control. In general, OAM provides network operators the ability to monitor the health of the network and quickly determine the location of failing links or fault conditions.

OAM information is conveyed in Slow Protocol frames called OAM Protocol Data Units (OAM PDUs). OAM PDUs contain the appropriate control and status information used to monitor, test and troubleshoot OAM-enabled links.

The addition of Ethernet OAM support in IxOS involves the following:

- support in stream configuration dialogs to send OAM packets.
- support for a PCPU based state machine that is configured to act as a *passive* mode endpoint and reply to OAM packets.

A list of load modules and the Ethernet OAM statistics they can generate are provided in <a href="Ethernet OAM Statistics">Ethernet OAM Statistics</a>. Ethernet OAM statistics counters are defined in <a href="Description of Statistics">Description of Statistics</a>.



#### **Chapter 4 - Optixia XM12 Chassis**

This chapter provides details about the Optixia XM12 chassis its specifications and features.

The Optixia XM12 is a next generation chassis that is a combination of the Optixia back-plane architecture and a XM form factor. The 12-slot platform allows for higher port density load modules. The XM12 High Performance version has two 2.0 kW powersupplies, while the Standard version has two 1.6 kW power supplies. An upgrade kit is available to convert the Standard XM12 to the High Performance version. See <a href="High Performance"><u>High Performance</u></a> Upgrade Kit.

САЦПОМ	This equipment is intended to be installed and maintained by Service Personnel.
ATTENTION	Cet équipement est conçu pour être installé et entretenu par des techniciens de maintenance.

The Optixia XM12 Chassis has 12 slots for support of up to 12 single wide load modules. The Optixia XM12 supports all load modules with improved system power and cooling. The Optixia XM12, shown in the following figure, was specifically designed to allow the hotswapping of modules, without requiring the chassis to be powered down.

<b>▲</b> WARNING	To prevent accidental injury to personnel, do not leave unused SFP (or SFP+) ports on load modules uncovered. When transceivers are not installed, end caps must be used. For details, see <a href="Use End Caps on Open Ports">Use End Caps on Open Ports</a> .
AVERTISSEMENT	Pour éviter toute blessure accidentelle de vos employés, ne laissez pas les ports SFP (ou SFP+) non utilisés des modules de charge découverts. Lorsqu'il n'y a pas d'émetteurs-récepteurs installés, les capuchons doivent être installés.

Figure: Optixia XM12 Chassis



The Optixia family of chassis has improved data throughput between Load Modules and the chassis, with improved backplane performance.

The Optixia chassis provides improved modularity of major components to reduce downtime of a failed chassis and reduce the probability of needing to remove a failed chassis from the test environment. Among the modular features provided are:

- Power supplies
- Motherboard and support components (RAM, Hard Drive)
- Fans

The motherboard and power supplies are accessible from the front of the chassis. Each of the modular components is capable of being removed in the field and replaced with minimum downtime for the customer.

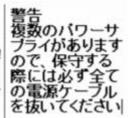
NOTE

In the event of indications of inadequate power, remove load modules starting from the low-number slots (slot 1, 2, 3), then working upward toward slot 12 until the problem is solved.

#### Warning Multiple Sources of Supply. Disconnect All Sources before Servicing

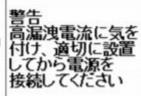
## Avertissement Présence de plusieurs sources d'alimentation électrique. Débrancher toutes les sources d'alimentation avant intervention

#### Achtung Mehrfachstromquellen! Alle Versorgungskabel vor Wartung entfernen.



Warning High Touch Current. Earth Connection Essential Before Connecting Supply Avertissement
Fort courant
de contact
Raccordement à la
Terre impératif
Avant branchement
de l'alimentation

Achtung Stellen Sie eine sichere Erdverbindung her, bevor Sie die Stromquelle anschließen.



#### **Specifications**

#### **XM12 Chassis**

The Optixia XM12 computer and chassis specifications are contained in the following table.

Optixia XM12 Specifications

CPU	Intel Pentium D, 3.0 GHz	
	CAUTION  Battery replacement: Danger of explosion if battery is incorrectly replaced. You should not attempt to replace the battery. Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries according to the battery manufacturer's instructions.	
	ATTENTION  Remplacement de la batterie: Le remplacement incorrect de la batterie peut provoquer une explosion. Vous ne devez en aucun casessayer de remplacer la batterie. Renvoyez le produit au service clients Ixia pour un échange avec le mêmetype de batterie ou un type équivalent. Ixia met les batteries usagées au rebut conformémentaux instructions du fabricant.	
Memory	4 GB	
Disk	250GB SATA Disk DVD Drive	
Operating System	Windows XP Professional	
Physical		
Load Module Slots	12	
Size	19.25 in. W x 17.5 in. H x 21 in. D(48.9cm W x 44.45cm H x 53.34cm D)	
Weight (empty)	83 lb (37.65 kg)	
Avg. Shipping Wt.	88 lb (39.92 kg)	

Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1		
Environmental			
Temperature			
Operating	Some high-density/high performance load modules require a lower maximum ambient operating temperature than the standard for the chassis. When a load module that requires the lower maximum operating temperature is installed in an XM chassis, the maximum operating temperature of the chassis is adjusted downward to match the maximum operating temperature of the load module. The operating temperature range specification is specified in the published datasheet for these load modules.		
Storage	41°F to 122°F, (5°C to 50°C)		
Humidity			
Operating	0% to 85%, non-condensing		
Storage	0% to 85%, non-condensing		
Clearance	Rear: 4 in (10 cm); fan openings should be clear of all cables or other obstructions. Sides: 2 in (5 cm) unless rack mounted.		
	Upper line cord 1: 200-240V 60/50Hz Standard: 10A, High Performance: 15A  Lower line cord 2: 200-240V 60/50Hz Standard: 8A, High Performance: 11A  Both power cords must be connected to the AC power		
Power	source to provide sufficient power to the chassis.  The upper line cord power supply provides power to the mother-board, fans, and some load modules. and the lower line cord power supply provides power to the remainder of the load modules. The chassis does not power up unless the upper power cord is installed.  For North American customers, the power cords have NEMA L6-20P plugs for attachment to the power source and IEC-60320-C19 connectors that attach to the XM12 chassis.		
	CAUTION  The chassis' safety approvals (UL and CE) are only valid when the unit is operating from 200-240VAC mains.  ATTENTION  Les homologations de sécurité (UL et CE) du		

	châssis ne sont valides que lorsque l'unité fonctionne sur une alimentation secteur de 200-240 VCA.		
	The socket/outlets used to power the unit must be installed near the equipment and be easily accessible because the power plug may be used to disconnect the unit from the power source.		
	Replacement of the power supply cord must be conducted by a Service Person. The same type cord and plug configuration shall be utilized.		
	Le remplacement du câble d'alimentation doit être effectué uniquement par un technicien de maintenance. La même configuration câble/prise doit être utilisée.		
Power Supplies	Standard: two 1.6 kW; High Performance: two 2.0 kW		
Front Panel Switches	On/Off momentary power push button		
Front Panel Con- nectors			
Mouse	PS/2 6-pin DIN		
Keyboard	PS/2 6-pin DIN		
Monitor	HD-DB15 Super VGA		
Printer	Female DB25 parallel port		
Ethernet	RJ-45 10/100/1000Mbps Gigabit Ethernet Management Port		
Firewire	IEEE 1394		
Serial	1 male DB9 port		
USB	4 USB dual type A, 4-pin jack connectors		
Sync In	4-pin RJ11		
Sync Out	4-pin RJ11		
Line In/Line Out/Mic	3.5mm mini-TRS stereo jacks (qty 3)		
Front Panel Indicators	See "LEDs/LCD Display" on the next page		
	2 Paired LEDs above each slot position indicating Power and Active status		
	LCD on front panel indicating chassis information		
Back Panel	Power On/Off rocker switch/Circuit Breakers (qty 2)		

Switches/Connectors	
Power	2 male receptacles (IEC 60320-C19)
Noise	The XM12 chassis running at maximum fan speed capacity may produce noise levels up to 84 db (A).

### Electrical Grounding requirements for Multi-Chassis system configuration

To ensure consistent grounding:

- All equipment must be mounted and screwed in to grounded 19" racks.
- Equipment should not be powered via distribution units with isolated grounding.

If equipment grounding is not consistent, the software will detect this and shutdown to protect equipment from damage.

#### **LEDs/LCD Display**

The Optixia XM12 has the following set of front panel LEDs, for each load module slot:

Optixia XM12 LEDs

Label	Color	Description	
Power	Green	For each load module slot, the Power LED is illuminated when the board is being powered.  When the Power LED is flashing, the board is being detected or initialized.	
In Use	Amber	For each load module slot, the Active LED is illuminated when a Load Module in a particular slot is owned by you.  If you run traffic from IxExplorer, without taking port ownership, the In Use light is not illuminated.	

#### **LCD Display**

An LCD display is provided on the chassis to indicate the status of the chassis without an external display device (monitor). The LCD operates in two modes:

- Startup: The LCD displays messages from IxServer to indicate the operation of IxServer as it initializes.
- Run: The LCD display provides chassis information. Information displayed includes chassis name, IxOS version, IP address, master/subordinate, and chassis status.

#### **Supported Modules**

The modules that are supported on the Optixia XM12 are listed in the following table.

Optixia XM12 Supported Modules

Module	SFF Requires Adapter	Function
HSE40GETSP1-		40 and 100 Gigabit Ethernet 1-port, 2-

Module	SFF Requires Adapter	Function
01HSE100GETSP1- 01HSE40/100GETSP1- 01		slot CFP interface (Full feature) dual- speed, 1-port, 2-slot CFP interface (Full feature)
HSE40GEQSFP1-01		1-port, 1-slot, QFSP interface (Full feature)
Xcellon-Ultra NP-01		12-port 10/100/1000 Mbps and 1-port 1GE aggregated and 1-port 10GE aggregated, Base T Ethernet copper, single-slot load module
Xcellon-Ultra XP-01		12-port 10/100/1000 Mbps and 1-port 1GE aggregated and 1-port 10GE aggregated, Base T Ethernet copper, single-slot load module
Xcellon-Ultra NG-01		12-port 10/100/1000 Mbps and 1-port 1GE aggregated and 1-port 10GE aggregated, Base T Ethernet copper, single-slot load module
LSM1000XMSP12-01		12-Port Gigabit Ethernet Load Module, Dual-PHY RJ45 10/100/1000 Mbps and SFP fiber
LSM1000XMVDC4-01 LSM1000XMVDC- NGLSM1000XMVDC8- 01LSM1000XMVDC12- 01LSM1000XMVDC16- 01 LSM1000XMVDC16NG		4/8/12/16-Port Dual-PHY RJ45 10/100/1000 Mbps and SFP fiber. FCoE enabled
LSM10GXM2XP- 01LSM10GXM2GBT- 01LSM10GXM2S-01		10 Gigabit Ethernet 2 port module, 1GHz, 1GB, Extra Per- formance.Includes 10GBASE-T ver- sion and SFP+ version.
LSM10GXMR2- 01LSM10GXMR2GBT- 01LSM10GXMR2S-01		10 Gigabit Ethernet 2 port module, 400MHz, 128MB, single slot, reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applic- ations.Includes 10GBASE-T version and SFP+ version.
LSM10GXM4XP- 01LSM10GXM4GBT- 01LSM10GXM4S-01		10 Gigabit Ethernet 4 port module, 1GHz, 1GB, Extra Per- formance.Includes 10GBASE-T ver-

Module	SFF Requires Adapter	Function
		sion and SFP+ version.
LSM10GXMR4- 01LSM10GXMR4GBT- 01LSM10GXMR4S-01		10 Gigabit Ethernet 4 port module, 400MHz, 128MB, single slot, reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applic- ations.Includes 10GBASE-T version and SFP+ version.
LSM10GXM8XP- 01LSM10GXM8GBT- 01LSM10GXM8S-01		10 Gigabit Ethernet 8 port module, 800MHz, 1GB, Extra Per- formanceIncludes 10GBASE-T version and SFP+ version.
LSM10GXMR8- 01LSM10GXMR8GBT- 01LSM10GXMR8S-01		10 Gigabit Ethernet 8 port module, 400MHz, 128MB, single slot, reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applic- ations.Includes 10GBASE-T version and SFP+ version.
NGY-NP8-01NGY- NP4-01NGY-NP2-01		10 Gigabit Application Network Processor Load Module, 2/4/8-Port LAN/WAN, SFP+ interface
AFM1000SP-01	Х	10/100/1000 3 port Stream extraction module
LSM1000XMVR4-01		4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule, reduced performance
LSM1000XMVR8-01		8-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule, reduced performance
LSM1000XMVR12-01		12-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule, reduced performance
LSM1000XMVR16-01		16-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule, reduced performance
MSM10G1-02	X	LAN/WAN/POS Multimode load mod- ule
LM100TXS2	X	10/100 Ethernet load module
LM100TXS8	х	8-port multilayer 10/100Mbps Eth- ernet load module

Module	SFF Requires Adapter	Function
LM100TX8	X	8-port 10/100Mbps Ethernet, reduced features
LM1000STXR4	X	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule, reduced feature set
LM1000STXS2	X	2-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule.
LM1000STXS4-256	X	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule; -256 version has 256MB of pro- cessor memory per port
LM1000STX2	X	2-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule
LM1000STX4	X	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule
ALM1000T8	X	Special 10/100/1000 Ethernet load module
ELM1000ST2	X	Special 10/100/1000 Ethernet load module
LSM10G1-01	X	10 Gigabit Ethernet load module
LSM10G1-01M	X	10 Gigabit Ethernet load module
LSM1000POE4-02	X	4-port PoE load module
PLM1000T4-PD	X	Power over Ethernet load module
LM622MR	X	ATM/POS load module
LM622MR-512	X	ATM/POS load module
MSM2.5G1-01	X	OC-48c load module
VQM01XM		Voice Quality Resource Module per- forms real-time processing of speech quality analysis using PESQ algorithm, on streams received on ports of the following load modules:
		<ul><li> Xcellon-Ultra NP-01</li><li> Xcellon-Ultra XP-01</li><li> Xcellon-Ultra NG-01</li></ul>

Module	SFF Requires Adapter	Function
		• ALM1000TS • CPM1000TS
		See Voice Quality Resource Module
EIM10G4S	SFP adapter	10 Gigabit Ethernet LAN Impairment module, 1-slot with 4-ports of SFP+ interfaces
EIM1G4S	SFP adapter	1Gigabit Ethernet LAN Impairment module, 1-slot with 4-ports of SFP interfaces
Xcellon-Lava	CFP to QSFP	Xcellon-Lava AP40/100GE2P     40/100 Gigabit Ethernet Gigabit     Ethernet Accelerated Performance, dual-speed, load module, 2-ports, 1-slot with CFP MSA interfaces and full performance     L2-7 support     Xcellon-Lava AP40/100GE2P-NG     FUSION 40/100 Gigabit Ethernet     Accelerated Performance, dualspeed, load module, 2-ports, 1-slot with CFP MSA interfaces and full performance L2-7 support     Xcellon-Lava 40/100GE2RP,     40/100 Gigabit Ethernet Reduced Performance, dual-speed, load module, 2-ports, 1-slot with CFP MSA interfaces and full featured L1-3 data plane support and up to 100 routing protocol emulations per port    NOTE
Xcellon-Multis	QSFP/CXP/CFP4/QSFP28	Xcellon-Multis     XM10/40GE12QSFP+FAN 40-Gig- abit Ethernet QSFP load module, 1-slot with 12-ports of 40GE QSFP with L2-7 support. The load module is compatible with the

Module	SFF Requires Adapter	Function
		XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). It requires purchase of one or more QSFP+ 40GBASE-SR4 optical transceivers (948-0028) and MT 12-fiber MMF cable, 3-meter length (942-0041).
		For 10GE fan-out capability the module requires either XM10GE-FAN-OUT 10GE fan-out option for a new module purchase (905-1000), or UPG-XM10GE-FAN-OUT 10GE fan-out UPGRADE option to UPGRADE an existing load module (905-1001).
		• Xcellon-Multis    XM10/40GE6QSFP+FAN 40-Gig-    abit Ethernet QSFP load module,    1-slot with 6-ports of 40GE QSFP    with L2-7 support. The load module is compatible with the XG12    rackmount chassis (940-0005),    XM12 HP rackmount chassis    (941-0009), and XM2 desktop    chassis (941-0003). It requires    purchase of one or more QSFP+    40GBASE-SR4 optical trans-    ceivers (948-0028) and MT 12-    fiber MMF cable, 3-meter length    (942-0041).
		For 10GE fan-out capability the module requires either XM10GE-FAN-OUT 10GE fan-out option for a new module purchase (905-1000), or UPG-XM10GE-FAN-OUT 10GE fan-out UPGRADE option to

Module	SFF Requires Adapter	Function
		UPGRADE an existing load module (905-1001).
		• Xcellon-Multis XM100GE4CXP 100-Gigabit Ethernet, single rate load module, 1-slot with 4-ports native CXP multimode fiber interfaces, L2-7 support, compatible with XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). Requires one or more per port of the following: CXP 100GE pluggable, multimode optical transceiver (948-0030) and MTP-MTP 24-fiber, multimode point-topoint 100GE cable, 3-meter (942-0035), or point-to-point, multimode CXP 100GE Active Optical Cable (AOC), 3-meter [942-0052].  • Xcellon-Multis XM100GE4CXP+FAN 100/40-Gigabit Ethernet, multiple rate load module, 1-slot with 4-ports native 100GE CXP multimode interfaces and up to 12-ports of 40GE via fan-out cables, L2-7 support, compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0009), and XM2 desktop chassis (941-0003). Requires one or more per port of the following 100GE media: CXP 100GE pluggable, multimode optical transceiver (948-0030) and MTP-MTP 24-fiber, multimode point-topoint 100GE cable, 3-meter (942-0035), or point-to-point, multimode CXP 100GE Active Optical Cable (AOC), 3-meter [942-0052]. Also requires one or more per port of the following 40GE media: CXP-to-3x40GE QSFP Act-
		ive Optical Cable (AOC) for

Module	SFF Requires Adapter	Function
		3x40GE fan-out, 3-meter [942-0054], or 5-meter [942-0055], or MTP-to-MTP passive fiber for 3x40GE fan-out, 3-meter (942-0060), 5-meter (942-0061). These cables may be used with QSFP 40GBASE-SR4 transceivers (948-0028).  • Xcellon-Multis XM40GE12QSFP+FAN 40-Gigabit Ethernet, load module, 1-slot with 12-ports of 40GE via multimode fan-out AOC cables, with L2-7 support. A quantity of 4 each, 3-meter, multimode CXP-to-3x40GE QSFP fan-out cables (942-0054) are supplied with the load module. The load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003).
		<ul> <li>Xcellon-Multis XM100GE4CFP4         100-Gigabit Ethernet, 1-slot with         4-ports with the native CFP4 physical interfaces</li> <li>Xcellon-Multis XM100GE4QSFP28         100-Gigabit Ethernet, 1-slot with         4-ports with the native QSFP28         physical interfaces</li> <li>Xcellon-Multis         XM100GE4QSFP28+ENH,         enhanced high density, 4-port         100GE with QSFP28 physical interface</li> </ul>
		<ul> <li>Xcellon-Multis         XM100GE4CFP4+ENH, enhanced         high density, 4-port 100GE with         CFP4 interface</li> </ul>
Xcellon-Multis Reduced	SFP/QSFP	Xcellon-Multis     XMR10GE16SFP+FAN 10-Gigabit     Ethernet, Reduced load module,     1-slot with 16-ports of 10GE via     multimode fan-out cables, with     L2-7 support, full featured L1-3

Module	SFF Requires Adapter	Function
		data plane support and up to 100 protocol emulations per port. This load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). It requires purchase of one or more QSFP+ 40GBASE-SR4 optical transceivers (948-0031) and MT 12-fiber MMF cable, 3-meter length (942-0041)).  NOTE For 40GE fan-out capability this module requires XM40GE-FAN-OUT 40GE fan-out option for a new module purchase (905-1002).  **Xcellon-Multis** XMR10GE32SFP+FAN 10-Gigabit Ethernet, Reduced load module, 1-slot with 32-ports of 10GE via multimode fan-out cables, with L2-7 support, full featured L1-3 data plane support and up to 100 protocol emulations per port. This load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). It requires purchase of one or more QSFP+ 40GBASE-SR4 optical transceivers (948-0031) and MT 12-fiber MMF cable, 3-meter length (942-0041).  NOTE For 40GE fan-out capability this module
		requires XM40GE-FAN- OUT 40GE fan-out option for a new mod- ule purchase (905- 1002).
		Xcellon-Multis XMR40GE12QSFP+     40-Gigabit Ethernet QSFP+

Module	SFF Requires Adapter	Function
		Reduced load module, 1-slot with 12-ports of 40GE QSFP+ with L2-7 support, full featured L1-3 data plane support and up to 100 protocol emulations per port. The load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). It requires purchase of one or more QSFP+ 40GBASE-SR4 optical transceivers (948-0031) and MT 12-fiber MMF cable, 3-meter length (942-0041), or QSFP+ 40GE, 40GBASE-LR4, single mode fiber optical transceiver (948-0032).  • Xcellon-Multis XMR40GE6QSFP+ 40-Gigabit Ethernet QSFP+ Reduced load module, 1-slot with 6-ports of 40GE QSFP+ with L2-7 support, full featured L1-3 data plane support and up to 100 routing emulations per port The load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). It requires purchase of one or more QSFP+ 40GBASE-SR4 optical transceivers (948-0031) and MT 12-fiber MMF cable, 3-meter length (942-0041), or QSFP+ 40GE, 40GBASE-LR4, single mode fiber optical transceiver (948-0032).

# **Hot-Swap Procedure**

Each Optixia XM12 chassis provides the ability of removing and reinstalling a Load Module without requiring the removal of power from the rest of the chassis. The process of removing/installing a Load Module does not impact either the operation of the OS or load modules installed in the chassis.

The hot-swap procedure is detailed in <u>Appendix D</u>, <u>Hot-Swap Procedure</u>.

## **SFF Adapter Module**

The Optixia XM12 adapter module allows legacy modules to be fit into the XM12 chassis. The following figures shows an SFF adapter module.

Figure: SFF Adapter



A legacy module is inserted into the front of the adapter module and connects to the pins in the rear of the adapter. The entire assembly can then be inserted into any Optixia XM12 slot.

Once an adapter module is installed in a chassis, legacy load modules can be hot-swapped without removing the adapter module from the chassis.

The following figure shows an SFF Adapter module with a legacy ATM card.

Figure: SFF Adapter with ATM Module



The <u>table</u> in <u>Supported Modules</u> section identifies the modules that can be used with the SFF Adapter.

# **Installing Filler Panels**

The airflow in an Optixia XM12 chassis is inefficient if load modules are installed in a few slots and the rest of the chassis is left open. For best cooling results, filler panels are required. It is required that filler panels are used in situations where the slots in the chassis are not all in use.

An empty Optixia XM12 chassis includes:

- 5 ea. 1-slot wide XM12 Filler Panel/Air Baffle units (p/n 652-0648-04)
- 1 ea. 6-slot wide XM12 Filler Panel/Air Baffle unit (p/n 652-0353)

### **Prerequisites for Filler Panel Installation:**

 The technician should use industry-standard grounding techniques, such as wrist and ankle grounding straps, to prevent damage to electronic components on any Ixia Load Modules.

### **Filler Panel Installation Procedure:**



**ESD Caution:** Use industry-standard grounding techniques to prevent Electrostatic Damage to the delicate electronic components on the Ixia Load Modules.

ATTENTION

**Décharges électrostatiques - Attention**: Utilisez les techniques standard de mise à la terre pour éviter tout dommage électrostatique sur les composants électroniques fragiles des modules de charge Ixia.

**Example**: Slide the one-slot filler panel, with the Ixia logo at the top, into the correct slot. The panel slides in on the slot rails in the chassis. Secure the faceplate of the filler panel to the chassis with two of the supplied screws.

NOTE

Use extreme care to prevent damage to delicate electronic components on an adjacent load module.

NOTE

Not using filler panels could cause random failures in port operations or damage installed modules.

# **Cooling Fan Speed Control**

The XM12 chassis automatically senses the temperature of specified modules and adjusts the cooling fan speed. If the system and board heat load is low enough, the cooling fan operates at a lower (quieter) speed.

The following modules have thermal sensors that report temperature readings:

- LSM1000XMS(R)12
- LSM1000XMV(R)16/12/8/4
- LSM10GXM(R)3
- NGY LSM10GXM2/4/8(R), LSM10GXM2/4/8XP, LSM10GXM(R)2/4/8S, and 10GBASE-T versions LSM10GXM(R)2/4/8GBT-01, NGY-NP2/4/8, and NGY SFP+ 2/4/8.
- LavaAP40/100GE 2P and LavaAP40/100GE 2RP

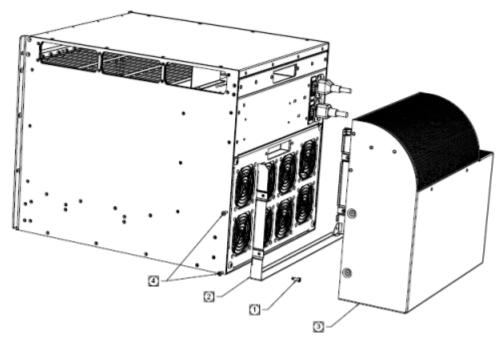
Other modules control the fan speed by means of a fixed speed setting. For a list of supported modules, see the table in Supported Modules section.

### XM12 Sound Reducer Installation

The XM12 Sound Reducer (PN 942-0021) is an optional accessory that installs on the rear of the XM12 chassis to reduce the sound of the cooling fans. It reduces the sound by approximately 10 dB.

Refer to the following figure when performing the installation.

Figure: XM12 Sound Reducer Installation



The chassis should be placed in a horizontal position, in a well-lighted work area.

- 1. On the XM12 chassis rear, remove the four shoulder screws that hold the fan panel in place. Do not remove the fan panel.
- 2. Attach the sound reducer mounting bracket to the fan panel using the same four shoulder screws removed in Step 1.
- 3. Slide the sound reducer onto the mounting bracket.
- 4. Secure the sound reducer onto the mounting bracket using the four pan-head screws included in the XM12 Sound Reducer kit.

### **Install XM12 Chassis**

The following steps describe the procedure of installing an XM12 chassis:

1. On the XM12 chassis rear, remove the four shoulder screws (marked in red circles) that hold the fan panel in place. Do not remove the fan panel.



- 2. Put two screws in the rack. Screw them in half way.
- 3. Put the empty chassis into the rack.
- 4. Reset the bottom of the empty XM12 chassis on top of the two screws. (refer to the area marked using red circles in the image below). The entire weight of the empty XM12 will be supported by these two screws.



- 5. Locate the two holes above that line up with the rack and screw in the other two screws (preferably the upper hole or one right below that)
- 6. Screw-in the bottom two screws all the way.
- 7. Find two or four more screws and screw them in. Do this optionally, and only if the holes line up.
- 8. Insert modules (ensure that any empty slots have the blank metal covers in them as marked in red in the image below).



### **Rack Mount Cautions**

CAUTION

If this unit is installed in a Rack Mount, observe the following precautions.

- a. Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the chassis (40° C).
- b. Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced. Do not block the back or sides of the chassis, and leave approximately two inches of space around the unit for proper ventilation.
- c. Mechanical Loading: Mount the equipment in the rack so that a hazardous condition is not caused due to uneven mechanical loading.
- d. Circuit Overloading: Consider the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Pay attention to equipment nameplate ratings when addressing this concern.

- e. Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Chassis frame should be screwed down to racks to ensure proper grounding path. In Addition, Pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).
- f. Replacement of the power supply cord must be conducted by a Service Person. The same type cord and plug configuration shall be utilized.

# Précautions relatives au montage en rack

ATTENTION

Si cette unité est installée dans une baie d'équipement réseau, observer les précautions suivantes:

- a. Température ambiante élevée: si installée dans un assemblage de baie fermé ou contenant plusieurs unités, la température ambiante de l'installation peut etre plus élevée que la température ambiante de la pièce. En conséquence, penser a installer l'équipement dans un environnement compatible avec la température ambiante maximale autorisée (40 C) spécifiée pour l'appareil.
- b. Circulation d'air réduite: installer l'équipement dans une baie de manière a ce que la circulation d'air requise pour faire fonctionner l'équipment en toute sécurité ne soit pas réduite. Ne pas bloquer les côtés de l'appareil, et laisser approximativement un espace de 12 pouces, de préférence 24 pouces, de chaque côté de l'unité pour une ventilation adéquate. L'espace laisse libre pour la circulation de l'air doit être de 12 pouces de chaque côté.
- c. Montage mécanique: monter l'appareil de manière a s'assurer qu'il soit droit dans la baie afin d'éviter de créer une condition dangereuse
- d. Un soin particulier doit etre apporté au branchement de l'équipement au circuit d'alimentation et aux conséquences qu'une charge excessive des circuits pourrait avoir sur le système de protection contre les surcharges et sur le cablâge d'alimentation. Prendre des précautions d'usage en prêtant attention aux normes figurant sur la plaque d'identification de l'équipement.
- e. Mise a la terre fiable: maintenir une mise a la terre fiable de l'équipement monté en baie. L'appareil doit etre vissé sur la baie afin d'assurer une mise a la terre correcte. De plus, faire particulièrement attention aux alimentations en courant autres que celles provenant de connections directes au circuit de dérivation (par exemple utilisation de prises multiples).
- f. Le remplacement du cordon d'alimentation doit comporter le même type de cordon et le même type de prise que ceux livrés avec l'unité.

# **High Performance Upgrade Kit**

A standard XM12 chassis (with two 1.6 kW power supplies) can be converted to a high performance XM12 (with two 2.0 kW power supplies) using an upgrade kit that is available from Ixia. Request `Field Replaceable Unit, Power Supply Upgrade Kit' (FRU-OPTIXIAXM12-01) PN 943-0005.

NOTE

Standard XM12 chassis that are running more than ten NGY load modules must have a power supply upgrade kit installed.

	We recommend the upgrade kit for existing XM12s with a fully loaded chassis combined with one or more NGY modules.		
САЦПОМ	This equipment is intended to be installed and maintained by Service Personnel.		
ATTENTION	Cet équipement est conçu pour être installé et entretenu par des techniciens de maintenance.		

# **Voice Quality Resource Module**

Voice Quality Resource Module (VQM01XM) performs real-time processing of speech quality analysis using PESQ algorithm, on streams received on ports of the following load modules:

- Xcellon-Ultra NP-01
- Xcellon-Ultra XP-01
- Xcellon-Ultra NG-01
- ALM1000TS
- CPM1000TS

The VQM01XM communicates with load modules through the chassis backplane. A single VQM01XM module can perform PESQ analyses, including necessary decoding, on up to 300 narrowband streams concurrently in real time. The PESQ stats are published in Stats View just after the last RTP packet of the analyzed sequence is received on port.

### **Statistics and Measurements**

The following real time metrics (Min, Max, and Average values) are provided by the Voice Quality Resource Module, depending on the application being run:

- Active level
- · Activity factor
- Noise level
- Peak level
- Listening effort (effort required to understand the meaning of spoken material)
- Listening quality (quality of speech)

These statistics are available in aggregated mode and individual per stream, as part of `VoIP RTP Per Channel' statistics.



# **Chapter 5 - Optixia XM2 Chassis**

This chapter provides details about the Optixia XM2 chassis its specifications and features.

The Optixia XM2 is the next generation portable chassis that is a combination of the Optixia architecture with the XM form factor. The 2-slot platform allows for higher port density load modules in a portable chassis.

The Optixia XM2 Chassis has 2 slots for support of up to 2 single wide load modules. The Optixia XM2 supports all XM form factor load modules and many standard form factor load modules with improved system power and cooling. The Optixia XM2 was specifically designed to allow the hot-swapping of load modules, without requiring the chassis to be powered down. The Optixia XM2 is shown in the figure below.

NOTE

The Optixia XM2 must only be operated in the horizontal position as shown in the figure below.

#### **▲** WARNING

To prevent accidental injury to personnel, do not leave unused SFP (or SFP+) ports on load modules uncovered. When transceivers are not installed, end caps must be used. For details, see <a href="Use End Caps on Open Ports">Use End Caps on Open Ports</a>.

### AVERTISSEMENT

Pour éviter toute blessure accidentelle de vos employés, ne laissez pas les ports SFP (ou SFP+) non utilisés des modules de charge découverts. Lorsqu'il n'y a pas d'émetteurs-récepteurs installés, les capuchons doivent être installés.

Figure: Optixia XM2 Chassis



The Optixia family of chassis has improved data throughput between Load Modules and the chassis, with improved backplane performance.

The Optixia chassis provides improved modularity of major components to reduce downtime of a failed chassis and reduce the probability of needing to remove a failed chassis from the test environment. Among the modular features provided are:

- · Power supplies
- Hard drive

The power supply is accessible from the back of the chassis. The hard drive is accessible from the bottom of the chassis.

# **Specifications**

### **XM2 Chassis**

The Optixia XM2 computer and chassis specifications are contained in the following table.

Optixia XM2 Specifications

СРИ	Intel Pentium Mobile, 2.0 GHz	
	CAUTION  Battery replacement: Danger of explosion if battery is incorrectly replaced. You should not attempt to replace the battery. Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries according to the battery manufacturer's instructions.	
	Remplacement de la batterie: Le remplacement incorrect de la batterie peut provoquer une explosion. Vous ne devez en aucun casessayer de remplacer la batterie. Renvoyez le produit au service clients Ixia pour un échange avec le mêmetype de batterie ou un type équivalent. Ixia met les batteries usagées au rebut conformémentaux instructions du fabricant.	
Memory	2 GB	
Disk	250GB SATA Disk HD  USB Drive  DVD Drive is not present in newer versions of XM2 chassis (starting with 941-0003-07 and 941-0023-02).	
Operating System	Windows XP Professional	
Physical	The Optixia XM2 must only be operated in the horizontal position as shown in the figure (Optixia XM2 Chassis) above.	
Load Module Slots	2 XM form factor	
Size	4.8 in. H x 20.0 in. W x 14.2 in. D(12.2cm H x 50.8cm W x 36.1cm D)	
Weight (empty)	25 lb (11.34 kg)	
Avg. Shipping Wt.	30 lb (13.61 kg)	
Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1	
Environmental		

Temperature		
	A10F to 1040F, (50C to 400C)  Some high-density/high performance load modules require a lower maximum ambient operating temperature than the standard for the chassis. When a load	
Operating	module that requires the lower maximum operating temperature is installed in an XM chassis, the maximum operating temperature of the chassis is adjusted downward to match the maximum operating temperature of the load module. The operating temperature range specification is specified in the published datasheet for each load module.	
Storage	41ºF to 122ºF, (5ºC to 50ºC)	
Humidity		
Operating	0% to 85%, non-condensing	
Storage	0% to 85%, non-condensing	
Clearance	Sides: 4 in (10 cm); fan openings should be clear of all cables or other obstructions.	
Power	100-240V 60/50Hz 12-6A	
	The socket/outlets used to power the unit must be installed near the equipment and be easily accessible because the power plug may be used to disconnect the unit from the power source.	
Front Panel Switches	On/Off momentary power push button	
Front Panel Con- nectors		
USB	1 USB dual type A, 4-pin jack connector	
Sync In	4-pin RJ11	
Sync Out	4-pin RJ11	
Front Panel Indicators	See <u>LEDs/LCD Display.</u>	
	2 Paired LEDs above each slot position indicating Power and Active status	
	1 LED indicating chassis Power ON 1 LED indicating HDD operation	
	LCD on front panel to display chassis information	

Rear Panel Con- nectors	
M	PS/2 6-pin DIN
Mouse	You <b>must</b> use the supplied Y-cable when using the PS/2 mouse.
Keyboard	PS/2 6-pin DIN (with or without the Y-cable)
Monitor	HD-DB15 Super VGA
Printer	Female DB25 parallel port
Ethernet	RJ-45 10/100/1000Mbps Gigabit Ethernet Management Port
Serial	1 male DB9 ports
USB	2 USB dual type A, 4-pin jack connectors
Power	Male receptacle (IEC 60320-C13)
	Condition:Ixia XM2
	Front Back Right Left
	Plugged in not started 56 54 57 58
Noise	Only CPU Running
	On Low Speed 58 56 58 60
	On Medium Speed-
	On Full Speed 70 67 70 73

# **LEDs/LCD Display**

The Optixia XM2 has the following set of front panel LEDs:

Optixia XM2 LEDs

Label	Color	Description
Power	Green	For each load module slot, the Power LED is illuminated when the board is being powered.  When the Power LED is flashing, the board is being detected or initialized.
Active	Amber	For each load module slot, the Active LED is illuminated when a Load Module in a particular slot is owned by you.  If you run traffic from IxExplorer, without taking port ownership, the Active LED is not illuminated.
Pwr	Green	For the chassis, indicated Power ON.
HDD	Green	For the chassis, indicates hard disk is active.

### **LCD Display**

An LCD display is provided on the chassis to indicate the status of the chassis without an external display device (monitor). The LCD operates in two modes:

- Startup: The LCD displays messages from IxServer to indicate the operation of IxServer as it initializes.
- Run: The LCD display provides chassis information. Information displayed includes chassis name, IxOS version, IP address, master/subordinate, and chassis status.

## **Supported Modules**

The modules that are supported on the Optixia XM2 are listed in the following table.

Optixia XM2 Supported Modules

Optivia XM2 Supported Modules			
Module	SFF Requires Adapater	Function	
HSE40GETSP1- 01HSE100GETSP1-		40 and 100 Gigabit Ethernet 1-port, 2-slot CFP interface (Full feature)	
01HSE40/100GETSP1- 01		dual-speed, 1-port, 2-slot CFP inter- face (Full feature)	
HSE40GEQSFP1-01		1-port, 1-slot, QFSP interface (Full feature)	
Xcellon-Ultra NP-01		12-port 10/100/1000 Mbps and 1-port 1GE aggregated and 1-port 10GE aggregated, Base T Ethernet copper, single-slot load module	
Xcellon-Ultra XP-01		12-port 10/100/1000 Mbps and 1-port 1GE aggregated and 1-port 10GE aggregated, Base T Ethernet copper, single-slot load module	
Xcellon-Ultra NG-01		12-port 10/100/1000 Mbps and 1-port 1GE aggregated and 1-port 10GE aggregated, Base T Ethernet copper, single-slot load module	
LSM1000XMSP12-01		12-Port Gigabit Ethernet Load Module, Dual-PHY RJ45 10/100/1000 Mbps and SFP fiber	
LSM1000XMVDC4-01			
LSM1000XMVDC4- NGLSM1000XMVDC8- 01LSM1000XMVDC12- 01LSM1000XMVDC16- 01 LSM1000XMVDC16NG		4/8/12/16-Port Dual-PHY RJ45 10/100/1000 Mbps and SFP fiber. FCoE enabled	
POWITOTOVIALADCTOMG			

Module	SFF Requires Adapater	Function
LSM10GXM2XP- 01LSM10GXM2GBT- 01LSM10GXM2S-01		10 Gigabit Ethernet 2 port module, 1GHz, 1GB, Extra Per- formanceIncludes 10GBASE-T version and SFP+ version.
LSM10GXMR2- 01LSM10GXMR2GBT- 01LSM10GXMR2S-01		10 Gigabit Ethernet 2 port module, 400MHz, 128MB, single slot, reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applic- ations.Includes 10GBASE-T version and SFP+ version.
LSM10GXM4XP- 01LSM10GXM4GBT- 01LSM10GXM4S-01		10 Gigabit Ethernet 4 port module, 1GHz, 1GB, Extra Per- formance.Includes 10GBASE-T ver- sion and SFP+ version.
LSM10GXMR4- 01LSM10GXMR4GBT- 01LSM10GXMR4S-01		10 Gigabit Ethernet 4 port module, 400MHz, 128MB, single slot, reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applic- ations.Includes 10GBASE-T version and SFP+ version.
LSM10GXM8XP- 01LSM10GXM8GBT- 01LSM10GXM8S-01		10 Gigabit Ethernet 8 port module, 800MHz, 1GB, Extra Per- formance.Includes 10GBASE-T ver- sion and SFP+ version.
LSM10GXMR8- 01LSM10GXMR8GBT- 01LSM10GXMR8S-01		10 Gigabit Ethernet 8 port module, 400MHz, 128MB, single slot, reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applic- ations.Includes 10GBASE-T version and SFP+ version.
NGY-NP8-01NGY- NP4-01NGY-NP2-01		10 Gigabit Application Network Processor Load Module, 2/4/8-Port LAN/WAN, SFP+ interface
AFM1000SP-01	Х	10/100/1000 3 port Stream extraction module
LSM1000XMVR4-01		4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule, reduced performance
LSM1000XMVR8-01		8-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod-

Module	SFF Requires Adapater	Function	
		ule, reduced performance	
LSM1000XMVR12-01		12-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule, reduced performance	
LSM1000XMVR16-01		16-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule, reduced performance	
MSM10G1-02	X	LAN/WAN/POS Multimode load module	
LM100TXS2	X	10/100 Ethernet load module	
LM100TXS8	X	8-port multilayer 10/100Mbps Eth- ernet load module	
LM100TX8	X	8-port 10/100Mbps Ethernet, reduced features	
LM1000STXR4	X	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule, reduced feature set	
LM1000STXS2	X	2-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule.	
LM1000STXS4-256	X	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule; -256 version has 256MB of pro- cessor memory per port	
LM1000STX2	X	2-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule	
LM1000STX4	X	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule	
ALM1000T8	X	Special 10/100/1000 Ethernet load module	
ELM1000ST2	Х	Special 10/100/1000 Ethernet load module	
LSM10G1-01	X	10 Gigabit Ethernet load module	
LSM10G1-01M	X	10 Gigabit Ethernet load module	
LSM1000POE4-02	X	4-port PoE load module	

Module	SFF Requires Adapater	Function
PLM1000T4-PD	X	Power over Ethernet load module
LM622MR	X	ATM/POS load module
LM622MR-512	X	ATM/POS load module
MSM2.5G1-01	X	OC-48c load module
VQM01XM		Voice Quality Resource Module performs real-time processing of speech quality analysis using PESQ algorithm, on streams received on ports of the following load modules:  • Xcellon-Ultra NP-01 • Xcellon-Ultra XP-01
		<ul><li>Xcellon-Ultra NG-01</li><li>ALM1000TS</li><li>CPM1000TS</li></ul>
		See Voice Quality Resource Module.
EIM10G4S	SFP adapter	10 Gigabit Ethernet LAN Impairment module, 1-slot with 4-ports of SFP+ interfaces
EIM1G4S	SFP adapter	1Gigabit Ethernet LAN Impairment module, 1-slot with 4-ports of SFP interfaces
Xcellon-Lava	CFP to QSFP	<ul> <li>Xcellon-Lava AP40/100GE2P 40/100 Gigabit Ethernet Gigabit Ethernet Accelerated Performance, dual-speed, load module, 2-ports, 1-slot with CFP MSA interfaces and full performance L2-7 support</li> <li>Xcellon-Lava AP40/100GE2P-NG FUSION 40/100 Gigabit Ethernet Accelerated Performance, dual-speed, load module, 2-ports, 1-slot with CFP MSA interfaces and full performance L2-7 support</li> <li>Xcellon-Lava 40/100GE2RP, 40/100 Gigabit Ethernet Reduced Performance, dual-speed, load module, 2-ports, 1-slot with CFP MSA interfaces and full featured L1-3 data plane support and up to 100 routing protocol emulations</li> </ul>

Module	SFF Requires Adapater	Function		
		per port  If XM12-01 (941-0002) chassis is used with this load module, the FRU-OPTIXIAXM12-01 (943-0005) power sup- ply upgrade kit must be installed.		
Xcellon-Multis	QSFP/CXP/CFP4/QSFP28	Xcellon-Multis     XM10/40GE12QSFP+FAN 40-Gigabit Ethernet QSFP load module,     1-slot with 12-ports of 40GE     QSFP with L2-7 support. The load module is compatible with the     XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). It requires purchase of one or more QSFP+ 40GBASE-SR4 optical transceivers (948-0028) and MT 12-fiber MMF cable, 3-meter length (942-0041).      NOTE     For 10GE fan-out capability the module requires either     XM10GE-FAN-OUT 10GE fan-out option for a new module purchase (905-1000), or UPG-XM10GE-FAN-OUT 10GE fan-out UPGRADE an existing load module (905-1001).      Xcellon-Multis     XM10/40GE6QSFP+FAN 40-Gigabit Ethernet QSFP load module, 1-slot with 6-ports of 40GE QSFP with L2-7 support. The load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). It requires		

Module	SFF Requires Adapater	Function
	Adapater	purchase of one or more QSFP+ 40GBASE-SR4 optical trans- ceivers (948-0028) and MT 12- fiber MMF cable, 3-meter length (942-0041).  For 10GE fan-out cap- ability the module requires either XM10GE-FAN-OUT 10GE fan-out option for a new module pur- chase (905-1000), or UPG-XM10GE-FAN- OUT 10GE fan-out UPGRADE option to UPGRADE an existing load module (905- 1001).  Xcellon-Multis XM100GE4CXP 100-Gigabit Ethernet, single rate load module, 1-slot with 4-ports native CXP multimode fiber inter- faces, L2-7 support, compatible with XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). Requires one or more per port of the following: CXP 100GE plug- gable, multimode optical trans- ceiver (948-0030) and MTP-MTP 24-fiber, multimode point-to- point 100GE cable, 3-meter (942- 0035), or point-to-point, mul- timode CXP 100GE Active Optical Cable (AOC), 3-meter [942- 0052].  Xcellon-Multis XM100GE4CXP+FAN 100/40-Gig- abit Ethernet, multiple rate load module, 1-slot with 4-ports nat- ive 100GE CXP multimode inter- faces and up to 12-ports of 40GE via fan-out cables, L2-7 support, compatible with the XG12 rack- mount chassis (940-0005), XM12

Module	SFF Requires Adapater	Function
		HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). Requires one or more per port of the following 100GE media: CXP 100GE pluggable, multimode optical transceiver (948-0030) and MTP-MTP 24-fiber, multimode point-topoint 100GE cable, 3-meter (942-0035), or point-to-point, multimode CXP 100GE Active Optical Cable (AOC), 3-meter [942-0052]. Also requires one or more per port of the following 40GE media: CXP-to-3x40GE QSFP Active Optical Cable (AOC) for 3x40GE fan-out, 3-meter [942-0054], or 5-meter [942-0055], or MTP-to-MTP passive fiber for 3x40GE fan-out, 3-meter (942-0060), 5-meter (942-0061). These cables may be used with QSFP 40GBASE-SR4 transceivers (948-0028).
		<ul> <li>Xcellon-Multis         XM40GE12QSFP+FAN 40-Gigabit         Ethernet, load module, 1-slot         with 12-ports of 40GE via multimode fan-out AOC cables, with         L2-7 support. A quantity of 4         each, 3-meter, multimode CXP-to-3x40GE QSFP fan-out cables         (942-0054) are supplied with the load module. The load module is compatible with the XG12 rackmount chassis (940-0005), XM12         HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0009).</li> <li>Xcellon-Multis XM100GE4CFP4         100-Gigabit Ethernet, 1-slot with 4-ports with the native CFP4 physical interfaces</li> <li>Xcellon-Multis XM100GE4QSFP28         100-Gigabit Ethernet, 1-slot with 4-ports with the native QSFP28         physical interfaces</li> </ul>

Module	SFF Requires Adapater	Function
		<ul> <li>Xcellon-Multis         XM100GE4QSFP28+ENH,         enhanced high density, 4-port         100GE with QSFP28 physical interface</li> <li>Xcellon-Multis         XM100GE4CFP4+ENH, enhanced         high density, 4-port 100GE with         CFP4 interface</li> </ul>
Xcellon-Multis Reduced	SFP/QSFP	Xcellon-Multis     XMR10GE16SFP+FAN 10-Gigabit     Ethernet, Reduced load module,     1-slot with 16-ports of 10GE via     multimode fan-out cables, with     L2-7 support, full featured L1-3     data plane support and up to 100     protocol emulations per port.     This load module is compatible     with the XG12 rackmount chassis     (940-0005), XM12 HP rackmount     chassis (941-0009), and XM2     desktop chassis (941-0003). It     requires purchase of one or more     QSFP+ 40GBASE-SR4 optical     transceivers (948-0031) and MT     12-fiber MMF cable, 3-meter     length (942-0041)).  NOTE  For 40GE fan-out capability this module     requires XM40GE-FAN-OUT 40GE fan-out     option for a new module purchase (905-     1002).  * Xcellon-Multis     XMR10GE32SFP+FAN 10-Gigabit     The protocology and produles  **The protocology and produces  **The protocology and p
		Ethernet, Reduced load module, 1-slot with 32-ports of 10GE via multimode fan-out cables, with L2-7 support, full featured L1-3 data plane support and up to 100 protocol emulations per port. This load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2

Module	SFF Requires Adapater	Function
		desktop chassis (941-0003). It requires purchase of one or more QSFP+ 40GBASE-SR4 optical transceivers (948-0031) and MT 12-fiber MMF cable, 3-meter length (942-0041).
		For 40GE fan-out capability this module requires XM40GE-FAN-OUT 40GE fan-out option for a new module purchase (905-1002).
		• Xcellon-Multis XMR40GE12QSFP+ 40-Gigabit Ethernet QSFP+ Reduced load module, 1-slot with 12-ports of 40GE QSFP+ with L2-7 support, full featured L1-3 data plane support and up to 100 protocol emulations per port. The load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). It requires purchase of one or more QSFP+ 40GBASE-SR4 optical transceivers (948-0031) and MT 12-fiber MMF cable, 3-meter length (942-0041), or QSFP+ 40GE, 40GBASE-LR4, single mode fiber optical transceiver (948-0032).
		• Xcellon-Multis XMR40GE6QSFP+ 40-Gigabit Ethernet QSFP+ Reduced load module, 1-slot with 6-ports of 40GE QSFP+ with L2-7 support, full featured L1-3 data plane support and up to 100 routing emulations per port The load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). It requires purchase of one or more QSFP+ 40GBASE-SR4 optical

Module	SFF Requires Adapater	Function
		transceivers (948-0031) and MT 12-fiber MMF cable, 3-meter length (942-0041), or QSFP+ 40GE, 40GBASE-LR4, single mode fiber optical transceiver (948- 0032).

## **Rack Mount Cautions**

**CAUTION** If this unit is installed in a rack mount, observe the following precautions:

- 1. Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the chassis (40° C).
- Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced. Do not block the back or sides of the chassis, and leave approximately two inches of space around the unit for proper ventilation.
- 3. Mechanical Loading: Mount the equipment in the rack so that a hazardous condition is not caused due to uneven mechanical loading.
- 4. Circuit Overloading: Consider the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Pay attention to equipment nameplate ratings when addressing this concern.
- 5. Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).

## Précautions relatives au montage en rack

Si cette unité est installée dans une baie d'équipement réseau, observer les précautions suivantes:

- a. Température ambiante élevée: si installée dans un assemblage de baie fermé ou contenant plusieurs unités, la température ambiante de l'installation peut etre plus élevée que la température ambiante de la pièce. En conséquence, penser a installer l'équipement dans un environnement compatible avec la température ambiante maximale autorisée (40 C) spécifiée pour l'appareil.
- b. Circulation d'air réduite: installer l'équipement dans une baie de manière a ce que la circulation d'air requise pour faire fonctionner l'équipment en toute sécurité ne soit pas réduite. Ne pas bloquer les côtés de l'appareil, et laisser approximativement un espace de 12 pouces, de préférence 24 pouces, de chaque côté de l'unité pour une ventilation adéquate. L'espace laisse libre pour la circulation de l'air doit être de 12 pouces de chaque côté.

- c. Montage mécanique: monter l'appareil de manière a s'assurer qu'il soit droit dans la baie afin d'éviter de créer une condition dangereuse
- d. Un soin particulier doit etre apporté au branchement de l'équipement au circuit d'alimentation et aux conséquences qu'une charge excessive des circuits pourrait avoir sur le système de protection contre les surcharges et sur le cablâge d'alimentation. Prendre des précautions d'usage en prêtant attention aux normes figurant sur la plaque d'identification de l'équipement.
- e. Mise a la terre fiable: maintenir une mise a la terre fiable de l'équipement monté en baie. L'appareil doit etre vissé sur la baie afin d'assurer une mise a la terre correcte. De plus, faire particulièrement attention aux alimentations en courant autres que celles provenant de connections directes au circuit de dérivation (par exemple utilisation de prises multiples).

### **Installing Rack-Mount Ear Brackets**

To mount the Optixia XM2 chassis into an equipment rack, first attach the rack-mount ears to the sides of the chassis.

- 1. If side feet are present (on left side of chassis) remove them. Discard the rubber feet, but keep the screws. See the figure Remove Side Feet (If Present).
- 2. Reinstall the screws removed in step 1 (into the same holes).
- Install left-side ear bracket (Ixia PN 652-0688-02) using supplied screws (PN 600-0105). See the figure Install Left Ear Bracket.
- 4. If this unit is installed in a rack mount, observe the following precautions:
- 5. Install right-side ear bracket (Ixia PN 652-0688-01) using supplied screws (PN 600-0105). See Install Right Ear Bracket.

Figure: Remove Side Feet (If Present)

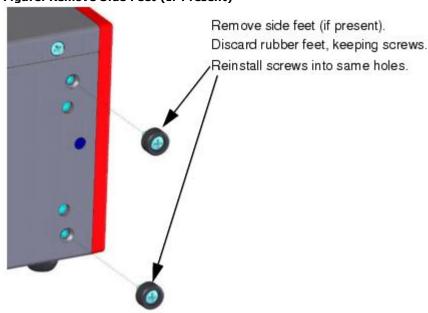


Figure: Install Left Ear Bracket

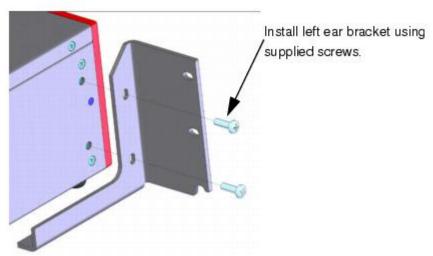
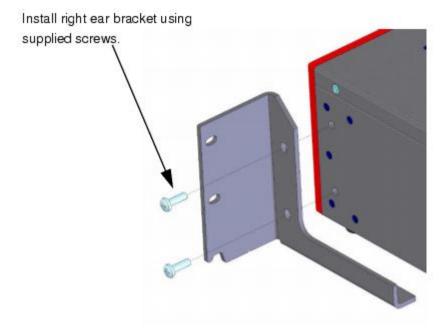


Figure: Install Right Ear Bracket



# **Hot-Swap Procedure**

Each Optixia XM2 chassis provides the ability of removing and reinstalling a Load Module without requiring the removal of power from the rest of the chassis. The process of removing/installing a Load Module does not impact either the operation of the OS or load modules installed in the chassis.

The hot-swap procedure is detailed in Appendix D, Hot-Swap Procedure.

## **SFF Adapter Module**

The Optixia XM adapter module allows legacy modules to be fit into the XM2 chassis. The following figure shows an SFF adapter module.

Figure: SFF Adapter



A legacy module is inserted into the front of the adapter module and connects to the pins in the rear of the adapter. The entire assembly can then be inserted into either Optixia XM2 slot.

Once an adapter module is installed in a chassis, legacy load modules can be hot-swapped without removing the adapter module from the chassis.

The following figure shows an SFF Adapter module with a legacy ATM card.

Figure: SFF Adapter with ATM Module



The <u>table</u> in Supported Modules section identifies the modules that can be used with the SFF Adapter.

# **Installing Filler Panels**

The airflow in an Optixia XM2 chassis can be inefficient if a load module is installed in one slot and the other is left open. For best cooling results, filler panels are required. Filler panels must be used in situations where the slots in the chassis are not all in use.

An empty Optixia XM2 chassis includes:

• 1 ea. 1 slot wide XM2 Filler Panel/Air Baffle units (p/n 652-0648-04)

### **Prerequisites for Filler Panel Installation:**

The technician should use industry-standard grounding techniques, such as wrist and ankle grounding straps, to prevent damage to electronic components on any Ixia Load Modules.

### Filler Panel Installation Procedure:

NOTE

**ESD Caution:** Use industry-standard grounding techniques to prevent Electrostatic Damage to the delicate electronic components on the Ixia Load Modules.

ATTENTION

**Décharges électrostatiques - Attention**: Utilisez les techniques standard de mise à la terre pour éviter tout dommage électrostatique sur les composants électroniques fragiles des modules de charge Ixia.

**Example**: Slide the one-slot filler panel, with the Ixia logo at the top, into the correct slot. The panel slides in on the slot rails in the chassis. Secure the faceplate of the filler panel to the chassis with two of the supplied screws.

NOTE

Use extreme care to prevent damage to delicate electronic components on an adjacent load module.

NOTE

Not using filler panels could cause random failures in port operations or damage installed modules.

## **Cooling Fan Speed Control**

The XM2 chassis automatically senses the temperature of specified modules and adjusts the cooling fan speed. If the system and board heat load is low enough, the cooling fan operates at a lower (quieter) speed.

The following modules have thermal sensors that report temperature readings:

- LSM1000XMS(R)12
- LSM1000XMV(R)16/12/8/4
- LSM10GXM(R)3
- NGY LSM10GXM2/4/8(R), LSM10GXM2/4/8XP, LSM10GXM(R)2/4/8S, 10GBASE-T versions LSM10GXM(R)2/4/8GBT-01, NGY-NP2/4/8, and NGY SFP+ 2/4/8.
- LavaAP40/100GE 2P and LavaAP40/100GE 2RP

Other modules control the fan speed by means of a fixed speed setting. For a list of supported modules, see the <u>table</u> in Supported Modules section.

# **Chapter 6 - XG12 Chassis**

This chapter provides details about the XG12 chassis its specifications and features.

The XG12 Chassis is the next generation high performance platform capable of supporting all XM form factor load modules, including full chassis configurations of the Xcellon load modules. It is a 12-slot chassis with increased total power capacity available for all load modules and front-to-back airflow delivery along with increased bandwidth from the CPU to the load modules.

The chassis provides improved modularity and access to the major components to reduce downtime of a failed chassis and to reduce the probability of needing to remove a failed chassis from the test environment. The four separate modules that make up the chassis are shown in the following table.

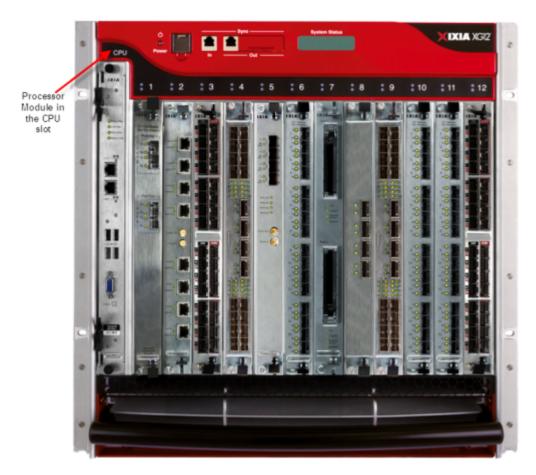
XG12 Pa	rt Num	bers	and	Modul	es
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Part Number	Description
941-0017	XG12, 12-Slot Chassis Frame Module
942-0031	XG12, 12-Slot Chassis Fan Module
942-0032	XG12, 12-Slot Chassis Power Supply Module
942-0033	XG12, 12-Slot Chassis Processor Module

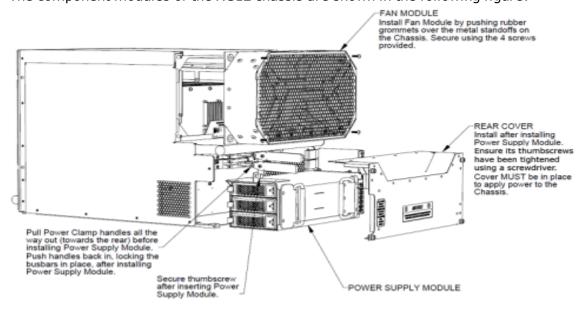
The XG12, shown in the figure below allows the hot-swapping of load modules, without requiring the chassis to be powered down. The Processor module for the XG12 chassis is not hot swappable.

The Processor Module is plugged into the front of the chassis. The power supplies and fans are accessible from the rear of the chassis. Each of the modular components is capable of being removed in the field and replaced with minimum downtime.

Figure: XG12 Chassis



The component modules of the XG12 chassis are shown in the following figure:



# **Specifications**

The XG12 chassis specifications are contained in the following tables:

### XG12 Processor Module Specifications

Processor Module	Field replaceable and removable processor card module with an
	Intel 2.26 GHz Core™ 2 Duo processor with 4 GB CPU memory,

	and 250 GB SATA hard drive	
Memory	4GB	
Hard Disk Drive	250GB	
Operating System	Windows 7	
	tery is incorrectly r to replace the batte vice for replacemen type of battery. Ixid	nt: Danger of explosion if bat- eplaced. You should not attempt ery. Return to Ixia Customer Ser- nt with the same or equivalent a disposes of used batteries ttery manufacturer's instruc-
	incorrect de la batto sion. Vous ne devez placer la batterie. F clients Ixia pour un batterie ou un type	a batterie: Le remplacement erie peut provoquer une explo- z en aucun casessayer de rem- Renvoyez le produit au service échange avec le mêmetype de équivalent. Ixia met les bat- ebut conformémentaux instruc-
		he Processor Module is located s used as the overall chassis

## XG12 Chassis Specifications

	• 19.0 in. W x 19.21 in. H x 27.2 in. D		
Size	• 48.26cm W x 48.79cm H x 69.09cm D		
	• 11 rackmount units (11RU)		
Load Module Slots	12 (compatible with Ixia XM form factor load modules)		
	The chassis requires three single phase, 200-240VAC, 50/60Hz circuits, each capable of providing 3680 watts. These circuits must provide protection against over-currents, short circuits and earth faults for the XG12 chassis. A 20A circuit breaker for each circuit is also required.  All three power cords must be plugged into their single phase 200-		
Chassis Power	240VAC, 50Hz/60Hz power sources at the same time for correct operation of the chassis.		
	The chassis power supplies are interlocked with the rear cover which must be installed for them to be enabled. After removing or installing the rear panel, ensure thumbscrews have been tightened down with a 'Flat Blade' screwdriver.		
	The load module power is enabled by the Ixia server pro-		

	gram. If it is not running, the load modules will not be powered on.		
	All three power cords are required to operate the XG12 chassis power supplies.		
	Power Cord shipments:		
	<ul> <li>Ixia provides three power cords that are configured and rated to meet the specifications of the target country where the chassis is being installed</li> </ul>		
Power Cords	<ul> <li>For North American customers, the power cords have NEMA L6-20P plugs for attachment to the power source and IEC- 60320-C19 connectors that attach to the XG12 chassis</li> </ul>		
	<ul> <li>For International shipments, the power cords supplied has plugs suitable for each destination country's power source and IEC-60320-C19 connectors that attach to the XG12 chassis</li> </ul>		
	<ul> <li>The XG12 chassis is CE marked and UL<sup>™</sup> certified when using the 200-240VAC power cords supplied with the chassis. However, these certifications for the chassis safety approvals are only valid when the unit is operating from all three 200- 240VAC main power sources</li> </ul>		
	Frame:		
	64 lbs. (29.1 kg) empty, component weight		
	<ul> <li>97 lbs. (44.1 kg) average shipping weight (with filler panels)</li> </ul>		
	Fan module:		
	• 10.2 lbs. (4.63 kg) component weight		
	• 17.3 lbs. (7.86 kg) average shipping weight		
	Power Supply module:		
Chassis Weights	<ul><li>28 lbs. (12.72 kg) component weight</li><li>35.1 lbs. (15.95 kg) average shipping weight</li></ul>		
	Processor module:		
	• 2.7 lbs. (1.23 kg) component weight		
	8.5 lbs. (3.86 kg) average shipping weight		
	Total chassis weight, without any load modules installed is 104.9 lbs. (47.6 kg). Do not attempt to lift the fully assembled chassis.		
	AVERTISSEMENT N'essayez pas de soulever le châssis entièrement assemblé.		
Fan Module	Field replaceable chassis fan assembly that is easily installed and removed.		
	12 inches is required at the rear of the chassis.		
Air flow Clearance	24 inches of clearance is preferred.		
	=		

Power Supply Module	Field replaceable power supply module that is easily installed and removed.  There are three 2825W power supplies in the Power Supply Module.  Each power supply may be removed or replaced separately.		
Timing Sources	Internal clock, synchronized with another Ixia chassis, GPS AFD- 1unit, AFD2 IRIG-B unit or with the Timing Distribution Module.		
Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1		
Operating tem- perature	A10F to 1040F, (50C to 400C)  Some high-density/high performance load modules require a lower maximum ambient operating temperature than the standard for the chassis. When a load module that requires the lower maximum operating temperature is installed in an XM chassis, the maximum operating temperature of the chassis is adjusted downward to match the maximum operating temperature of the load module. The operating temperature range specification is specified in the published datasheet for these load modules.		
Storage temperature	41ºF to 122ºF, (5ºC to 50ºC)		
Operating Humidity	0% to 85%, non-condensing		
Storage Humidity	0% to 85%, non-condensing		
Noise	The XG12 chassis running at maximum fan speed capacity may produce noise levels up to 87 dB(A). This is measured per the GR-63-CORE, Issue 1, paragraph 5.6.3 specification. The use of appropriate ear protection is recommended to protect against hearing impairment. Consult local health and safety regulations for recommended maximum exposure levels for noise and ear protection devices.  Shown below are the maximum XG12 chassis sound levels measured according to GR-63-CORE, Issue 1, Paragraph 5.6.3.  Front: 83.5 dB(A)  Left Side: 84.2 dB(A)  Rear: 86.5 dB(A)  Right Side: 84.4 dB(A)		

# Hearing Protection: The XG12 chassis generates noise levels above 80 dB(A). Ear protection must be worn. The use of appropriate ear protection is recommended to protect against hearing impairment. Consult local health and safety regulations for recommended maximum exposure levels for noise and ear protection devices. AVERTISSEMENT Produit un niveau sonore de 86.5db (A). Des protections auditives doivent etre portees pour eviter tout risque de

#### AVERTISSEMENT

perte d'audition.

Se referer au manuel IXIA Materiel et Reefrence pour plus d'information sur le chassis  $XG12^{\text{TM}}$  ou  $XGS12^{\text{TM}}$ .



WARNING: Noise levels of up to 86.5db (A) are produced.

Ear protection must be worn to protect against hearing impairment.

See Ixia Hardware and Reference manual for further information on the XG12™ chassis.

Produit un niveau sonore de 86.5db (A).

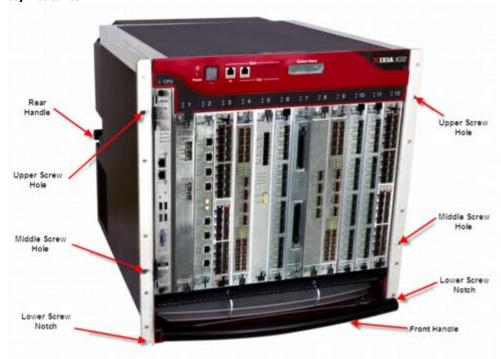
Des protections auditives doivent être portées pour éviter tout risque de perte d'audition.

Se référer au manuel IXIA Matériel et Référence pour plus d'information sur le chassis XG12™ ou XGS12™.

#### XG12 Chassis controls and indicators

Front Panel Switches	On/Off momentary power push button.	
Monitor	HD-DB15 Super VGA.	
Ethernet	Two RJ-45 10/100/1000Mbps Gigabit Ethernet Management Port.	
USB	4 USB dual type A, 4-pin jack connectors	
Sync In	Single Sync In jack with a 4-pin RJ11	
Sync Out	Single Sync Out jack with a 4-pin RJ11	
Front Panel Indicators	See <u>LEDs/LCD Display</u> .	
	2 Paired LEDs above each slot position indicating Power and Active status.	
	2x16 LCD on front panel indicating chassis information.	

Figure: Safety Features



#### XG12 chassis installation precautions:

- The chassis should be installed in the rack before installing the power supply module, fan module and load modules, thereby reducing the weight of the chassis.
- The two lower bolts used to secure the chassis to a rack can be used to hold the chassis frame in place while securing all of the other bolts (See Figure 6-2).
- Secure the chassis to rack face with all six bolts. Fully depress power supply clamps when installing power supply module.
- Secure the power supply module thumb bolt when installing power supply module.
- Install the rear power supply cover before applying AC power.
  - After removing or installing this cover, ensure that the thumbscrews are tightened down with a screwdriver.
- Do not use the chassis without installing the Fan module.
- Do not use the chassis without installing the Processor module.
- Do not leave unused slots open. Use the filler panels to cover the un-used slots. See Installing Filler Panels for more information.
- · Do not block the front air intake.
- A minimum air flow clearance of 12 inches is required. 24 inches of air flow clearance is preferred at the rear of the chassis.
- Operator intervention may be required to power cycle the XG12 chassis or restart a software program in the event the XG12 chassis operation is upset or stopped by electrostatic discharge.

## **LEDs/LCD Display**

The XG12 chassis has front panel LEDs for each load module slot.

#### XG12 LEDs

Label	Color	Description	
Power	Green	When the Power LED is flashing, the board is being detected or initialized.	
		The Power LED is illuminated when the board is powered.	
In Use	Amber  The Active LED is illuminated when you have taken ownership of to load module.  If you run traffic from IxExplorer, without taking port ownership, In Use light is not illuminated.		

## **LCD Display**

An LCD display is provided on the chassis to indicate the status of the chassis without an external display device (monitor). The LCD operates in two modes:

- Startup: The LCD displays messages from IxServer to indicate the operation of IxServer as it initializes.
- Run: The LCD display provides chassis information. Information displayed includes chassis name, IxOS version, IP address, master/subordinate, and chassis status.

#### **CPU Slot LED Definitions**

The specifications of LEDs for the Processor module and the LEDs above the Processor module slot are shown in the following table:

NOTE

**ESD Discharge**: Operator intervention may be required to power cycle the unit or restart a software program in the event the unit is upset by electrostatic discharge.

#### LED Specifications

	LED	Color	Description
On the chassis front face	CPU card Slot LED	Yellow	The backplane is initializing.
		Green	The backplane has initialized
Processor module - front panel	Stdby Pwr LED	Green	5V Stand-by power is avail- able
	CPU Pwr LED	Green	CPU Card power is avail- able
	HDD Act LED		
	Bkpln Link LED	Green	PCIe link to backplane is up

	LED	Color	Description
Processor module - Ethernet LEDs for each management port	Link LED	Green	Port has link
	Act LED		Flashes when port has activity

# **Supported Modules**

The modules that are supported on the XG12 are listed in the following table.

Supported Modules

Family	Module	Function
XM Form Factor (XMFF) load modules	Xcellon-Flex™ High density 10GbE products	<ul> <li>Xcellon-FlexAP10G16S 10 Gigabit Ethernet LAN Load Module, L2-7 Accelerated Performance, a 1-slot module with 16-ports of SFP+ interfaces</li> <li>Xcellon-FlexFE10G16S 10 Gigabit Ethernet LAN Load Module, L2-3 Full Emulation Performance, a 1-slot module with 16-ports of SFP+ interfaces</li> </ul>
	Xdensity™ Ultra-high dens- ity 10GbE	Xdensity, XDM10G32S, Ultra-high density, 10-Gigabit Ethernet load module with 32-ports of SFP+ interfaces and L2-3 data plane support
	Xcellon-Flex™ High density 10GbE and 40 GE products	<ul> <li>Xcellon-FlexAP10/4016SQ 10/40 Gigabit Ethernet Accelerated Performance Load Module, 16-Ports of SFP+ interfaces and 4-ports of QSFP 40 GE interfaces with full performance L1-7 support</li> <li>Xcellon-FlexFE40G4Q 40 Gigabit Ethernet Full Emulation Load Module, 4-ports of QSFP 40 GE with L1-3 support</li> </ul>
	K2 Higher Speed Ethernet product line	<ul> <li>HSE40GETSP1-01, 40-Gigabit Ethernet Load Module, 1-port, 2-slots, with the CFP MSA interface</li> <li>HSE100GETSP1-01, 100- Gigabit Ethernet Load Module, 1-port, 2-slots, with the CFP MSA interface</li> <li>HSE40/100GETSP1-01 Dual-Speed, 1-port, 2-slots, with CFP MSA interface</li> <li>HSE40/100GETSPR1-01, Dual Speed, 40 and 100-Gigabit Data Plane Ethernet Load Module, 1-port, 2-slots, with the CFP MSA interface</li> <li>HSE40GEQSFP1-01, 40-Gigabit Ethernet Load Module, 1-port, 1-slot with the QSFP+ pluggable interface for multimode fiber, 850nm, or QSFP+ copper cables</li> </ul>

Family	Module	Function
	Xcellon Ultra™ High Per- formance Applic- ation Test product line	Xcellon-Ultra NP-01, Application Network Processor Load Module, 1-10G XFP port and/or 12-Ports of Dual-PHY (SFP fiber and RJ45 copper) 10/100/1000 Mbps
	NGY High Density 10 Gigabit Ethernet product line	<ul> <li>LSM10GXMR2/4/8-port, reduced performance, load modules with the XFP interface</li> <li>LSM10GXM2/4/8XP-port, Extra performance, load modules with the XFP interface</li> <li>LSM10GXM2S/4S/8S-port, Extra performance, load modules with the SFP+ interface</li> <li>LSM10GXM2S/4S/8S-port, reduced performance, load modules with the SFP+ interface</li> <li>LSM10GXM2GBT/4GBT/8GBT-port, Extra performance, load modules with the 10GBASE-T interface</li> <li>LSM10GXM2GBT/4GBT/8GBT-port, reduced performance, load modules with the 10GBASE-T interface</li> </ul>
	Fibre Channel load module products	<ul> <li>FCMGXM4S-01, 4-Port Fibre Channel Load Module, with 2Gbps, 4Gbps, and 8Gbps support, SFP+ interface</li> <li>FCMGXM8S-01, 8-Port Fibre Channel Load Module, with 2Gbps, 4Gbps, and 8Gbps support, SFP+ interface</li> </ul>
	ImpairNet Load module products	<ul> <li>ImpairNet EIM1G4S Gigabit Ethernet LAN         Impairment module, 1-slot with 4-ports of SFP         interfaces</li> <li>ImpairNet EIM10G4S 10 Gigabit Ethernet LAN         Impairment module, 1-slot with 4-ports of         SFP+ interfaces</li> </ul>
	Voice Quality module	VQM0001, Resource module, for real time quality of voice measurement. Must purchased with VQM0001-B1, Solution Bundle, Resource module with IXLOAD-PESQ and IXLOAD-AUDIO-CODECS software license
	NGY NP High Density 10GbE Application Test product line	<ul> <li>NGY-NP8-01, 10 Gigabit Application Network Processor Load Module, 8-Port LAN/WAN, SFP+ interface</li> <li>NGY-NP4-01, 10 Gigabit Application Network Processor Load Module, 4-Port LAN/WAN, SFP+ interface</li> <li>NGY-NP2-01, 10 Gigabit Application Network Processor Load Module, 2-Port LAN/WAN, SFP+</li> </ul>

Family	Module	Function
		interface
	High Density Gigabit Ethernet product line	<ul> <li>LSM1000XMVDC 4/8/12/16-port, full performance, load modules with dual-phy SFP fiber and 10/100/1000Mbps RJ45 copper</li> <li>LSM1000XMVR4/8/12/16-port, reduced performance, load modules with dual-phy SFP fiber and 10/100/1000Mbps RJ45 copper</li> <li>LSM1000XMSP12-01, Gigabit Ethernet, Load Module, 12-Ports Dual-PHY (SFP fiber and RJ45 copper) 10/100/1000 Mbps</li> </ul>
	Xcellon-Lava	<ul> <li>Xcellon-Lava AP40/100GE2P 40/100 Gigabit Ethernet Gigabit Ethernet Accelerated Performance, dual-speed, load module, 2-ports, 1-slot with CFP MSA interfaces and full performance L2-7 support</li> <li>Xcellon-Lava AP40/100GE2P-NG FUSION 40/100 Gigabit Ethernet Accelerated Performance, dual-speed, load module, 2-ports, 1-slot with CFP MSA interfaces and full performance L2-7 support</li> <li>Xcellon-Lava 40/100GE2RP, 40/100 Gigabit Ethernet Reduced Performance, dual-speed, load module, 2-ports, 1-slot with CFP MSA interfaces and full featured L1-3 data plane support and up to 100 routing protocol emulations per port</li> <li>NOTE If XM12-01 (941-0002) chassis is used with this load module, the FRU-OPTIXIAXM12-01 (943-0005) power supply upgrade kit must be installed.</li> </ul>
	Xcellon-Multis	Xcellon-Multis XM10/40GE12QSFP+FAN 40-Gigabit Ethernet QSFP load module, 1-slot with 12-ports of 40GE QSFP with L2-7 support. The load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). It requires purchase of one or more QSFP+ 40GBASE-SR4 optical transceivers (948-0028) and MT 12-fiber MMF cable, 3-meter length (942-0041).  NOTE  For 10GE fan-out capability the module requires either XM10GE-FAN-OUT 10GE fan-out option for a new module purchase (905-1000), or UPG-XM10GE-FAN-OUT 10GE fan-out UPGRADE option to UPGRADE an

Family	Module	Function
		existing load module (905-1001).
		<ul> <li>Xcellon-Multis XM10/40GE6QSFP+FAN 40-Gigabit Ethernet QSFP load module, 1-slot with 6-ports of 40GE QSFP with L2-7 support. The load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). It requires purchase of one or more QSFP+ 40GBASE-SR4 optical transceivers (948-0028) and MT 12-fiber MMF cable, 3-meter length (942-0041).</li> </ul>
		For 10GE fan-out capability the module requires either XM10GE-FAN-OUT 10GE fan-out option for a new module purchase (905-1000), or UPG-XM10GE-FAN-OUT 10GE fan-out UPGRADE option to UPGRADE an existing load module (905-1001).
		<ul> <li>Xcellon-Multis XM100GE4CXP 100-Gigabit Ethernet, single rate load module, 1-slot with 4-ports native CXP multimode fiber interfaces, L2-7 support, compatible with XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). Requires one or more per port of the following: CXP 100GE pluggable, multimode optical transceiver (948-0030) and MTP-MTP 24-fiber, multimode point-to-point 100GE cable, 3-meter (942-0035), or point-to-point, multimode CXP 100GE Active Optical Cable (AOC), 3-meter [942-0052].</li> <li>Xcellon-Multis XM100GE4CXP+FAN 100/40-Gigabit Ethernet, multiple rate load module, 1-slot with 4-ports native 100GE CXP multimode interfaces and up to 12-ports of 40GE via fan-out</li> </ul>
		cables, L2-7 support, compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). Requires one or more per port of the following 100GE media: CXP 100GE pluggable, multimode optical transceiver (948-0030) and MTP-MTP 24-fiber, multimode point-to-point 100GE cable, 3-meter (942-0035), or point-to-point, multimode CXP 100GE Active Optical Cable (AOC), 3-meter [942-0052]. Also requires one or more per port of the following 40GE media: CXP-to-3x40GE QSFP Active

Family	Module	Function
		Optical Cable (AOC) for 3x40GE fan-out, 3-meter [942-0054], or 5-meter [942-0055], or MTP-to-MTP passive fiber for 3x40GE fan-out, 3-meter (942-0060), 5-meter (942-0061). These cables may be used with QSFP 40GBASE-SR4 transceivers (948-0028).  Xcellon-Multis XM40GE12QSFP+FAN 40-Gigabit Ethernet, load module, 1-slot with 12-ports of 40GE via multimode fan-out AOC cables, with L2-7 support. A quantity of 4 each, 3-meter, multimode CXP-to-3x40GE QSFP fan-out cables (942-0054) are supplied with the load module. The load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003).  Xcellon-Multis XM100GE4CFP4 100-Gigabit Ethernet, 1-slot with 4-ports with the native CFP4 physical interfaces  Xcellon-Multis XM100GE4QSFP28 100-Gigabit Ethernet, 1-slot with 4-ports with the native QSFP28 physical interfaces  Xcellon-Multis XM100GE4QSFP28+ENH, enhanced high density, 4-port 100GE with QSFP28 physical interface  Xcellon-Multis XM100GE4CFP4+ENH, enhanced high density, 4-port 100GE with CFP4 interface
	Xcellon-Multis Reduced	Xcellon-Multis XMR10GE16SFP+FAN 10-Gigabit Ethernet, Reduced load module, 1-slot with 16-ports of 10GE via multimode fan-out cables, with L2-7 support, full featured L1-3 data plane support and up to 100 protocol emulations per port. This load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0009), and XM2 desktop chassis (941-0003). It requires purchase of one or more QSFP+ 40GBASE-SR4 optical transceivers (948-0031) and MT 12-fiber MMF cable, 3-meter length (942-0041)).  NOTE  For 40GE fan-out capability this module requires XM40GE-FAN-OUT 40GE fan-out option for a new module purchase (905-1002).  Xcellon-Multis XMR10GE32SFP+FAN 10-Gigabit Ethernet, Reduced load module, 1-slot with 32-ports of 10GE via multimode fan-out cables,

Family	Module	Function
		with L2-7 support, full featured L1-3 data plane support and up to 100 protocol emulations per port. This load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). It requires purchase of one or more QSFP+ 40GBASE-SR4 optical transceivers (948-0031) and MT 12-fiber MMF cable, 3-meter length (942-0041).  NOTE For 40GE fan-out capability this module requires XM40GE-FAN-OUT 40GE
		fan-out option for a new module pur- chase (905-1002).
		• Xcellon-Multis XMR40GE12QSFP+ 40-Gigabit Ethernet QSFP+ Reduced load module, 1-slot with 12-ports of 40GE QSFP+ with L2-7 support, full featured L1-3 data plane support and up to 100 protocol emulations per port. The load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). It requires purchase of one or more QSFP+ 40GBASE-SR4 optical transceivers (948-0031) and MT 12-fiber MMF cable, 3-meter length (942-0041), or QSFP+ 40GE, 40GBASE-LR4, single mode fiber optical transceiver (948-0032).
		• Xcellon-Multis XMR40GE6QSFP+ 40-Gigabit Ethernet QSFP+ Reduced load module, 1-slot with 6-ports of 40GE QSFP+ with L2-7 support, full featured L1-3 data plane support and up to 100 routing emulations per port The load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003). It requires purchase of one or more QSFP+ 40GBASE-SR4 optical transceivers (948-0031) and MT 12-fiber MMF cable, 3-meter length (942-0041), or QSFP+ 40GE, 40GBASE-LR4, single mode fiber optical transceiver (948-0032).
Standard Form Factor (SFF) load modules for XG12 chassis	Gigabit Ethernet TX, TXS, STX and STXS products	<ul> <li>LM100TX8, 100MB Ethernet Load Module, 8-Port 10/100Mbps, L2-3 data plane support only</li> <li>LM100TXS8, 10/100Mbps Ethernet Load Module, 8-Port RJ45, 64MB Port CPU memory</li> <li>LM100TXS2, 10/100Mbps Ethernet Load Module, 2-Port RJ45, 64MB Port CPU memory</li> </ul>

Family	Module	Function
Requires 944- 0007 Adapter Card for XM Chassis instal- latio- ns		<ul> <li>LM1000STX4, Gigabit Ethernet Load Module, 4-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps, L2-3 data plane support only</li> <li>LM1000STX2, Gigabit Ethernet Load Module, 2-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps, L2-3 data plane support only</li> <li>LM1000STXS2, Gigabit Ethernet Load Module, 2-Port Dual-PHY (RJ45 and SFP) 10/100/1000 MbpsLM1000STXS4-256, Gigabit Ethernet Load Module, 4-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps</li> </ul>
	10 Gigabit Eth- ernet LSM products	<ul> <li>LSM10G1-01, 10 Gigabit Ethernet Load Module, 1-Port, Full L2-7 support, requires interface adapter module         Interchangeable interface adapter modules for SFP+, 10GBASE-T, XENPAK, X2, and CX4 interfaces for the LSM10G1-01     </li> </ul>
	Application and Encryption Test product line	<ul> <li>AFM (Auxiliary Function Module): AFM1000SP-0</li> <li>ALM (Application Load Module): ALM1000T8</li> <li>ELM (Encryption Load Module): ELM1000ST2</li> </ul>
	10-Gigabit UNIPHY and MacSec products	<ul> <li>MSM10G1- 10 Gigabit Ethernet OC192 Load Module, 1-port Multi Services Module with an XFP interface, supports 10GE LAN/WAN and optional OC-192c POS</li> <li>LSM10GMS1-01, 10 Gigabit Ethernet Load Module, 1-Port, LAN/WAN, Full performance and supports 802.1ae Media Access Control Security (MacSec) L2 security, including GCM/AES128</li> </ul>
	Packet over SONET and ATM products	<ul> <li>MSM2.5G1-01, OC48 Load Module, 1-Port 2.5G Multi Service Module supporting OC48c, Supports POS, Full L2-7 support</li> <li>LM622MR, OC3/OC12 ATM/POS, Load Module, 2-port ATM/Packet over SONET (POS); Full L2-7 Support. Supports 622 and 155 Mbps data rates</li> <li>LM622MR-512, OC3/OC12 ATM/POS, Load Module, 2-port ATM/Packet over SONET (POS), Full L2-7 Support. Supports 622 and 155 Mbps data rates, 512MB Port CPU memory</li> <li>OC3OC12PHY, OC3/OC12 ATM/POS Adapter, Dual-SC optical connector, Single-port OC-3/OC-12 PHY 1310nm Multimode; For the</li> </ul>

Family	Module	Function
		LM622MR or LM622MR-512) load modules
	Power over Ethernet (IEEE802.3af)	<ul> <li>PLM1000T4-PD (20W), Gigabit Ethernet Load Module, 4-Port PoE, supports 10/100/1000 Mbps Ethernet, and emulates up to 4 powered devices</li> <li>LSM1000POE4-02 (30W), Gigabit Ethernet Load Module, 4-Port PoE, supports 10/100/1000 Mbps Ethernet, and emulates up to 4 powered devices</li> </ul>

## **Hot-Swap Procedure**

Each XG12 chassis provides the ability of removing and reinstalling a load module without requiring the removal of power from the rest of the chassis. The process of removing/installing a Load Module does not impact either the operation of the OS or remaining load modules installed in the chassis.

The hot-swap procedure is detailed in Appendix D Hot-Swap Procedure.

## **SFF Adapter Module**

The XG12 adapter module allows Ixia Standard Form Factor (SFF) load modules to be adapted into the XG12 chassis. The following figure shows an SFF adapter module.





A SFF load module is inserted into the front of the adapter and connects to the pins in the rear of the adapter. The entire assembly can then be inserted into any XG12 chassis slot.

Once an adapter module is installed in a chassis, SFF load modules can be hot-swapped without removing the SFF load module from the chassis.

The following figure shows an SFF Adapter module with a legacy ATM card.

Figure: SFF Adapter with ATM Module



The <u>table</u> in section <u>Supported Modules</u> identifies the modules that can be used with the SFF Adapter.

## **Cooling Fan Speed Control**

The XG12 chassis automatically monitors and measures the temperature of installed load modules. The XG12 automatically adjusts the fan speed to maintain proper cooling.

## Power outage recovery and Automatic booting scenario

The BIOS on the XG12 is set to Power On after a power failure.

The XG12 chassis will start up, boot Windows 7 and automatically login to the Ixia user account. Anything that is in the Startup folder will also launch.

## **Rack Mount Cautions**

#### CAUTION

If this unit is installed in a network equipment rack, please observe the following precautions.

- 1. Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the chassis (40° C).
- 2. Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced. Do not block the back or the front of the chassis, and leave approximately 12 inches of space, 24 inches preferred, for the back of the unit for proper ventilation. The air flow clearance should be 12 inches on the front.
- 3. Mechanical Loading: Mount the chassis so that is it level in the rack and that a hazardous condition is not caused. Please install all six mounting bolts.
- 4. Circuit Overloading: Consider the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Pay attention to equipment nameplate ratings when addressing this concern.
- 5. Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Chassis frame should be screwed down to racks to ensure proper grounding path. In

- Addition, Pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).
- 6. Replacement of the power supply cord must of the same type cord and plug configuration that was shipped with the unit.

## Précautions relatives au montage en rack

ATTENTION

Si cette unité est installée dans une baie d'équipement réseau, observer les précautions suivantes:

- a. Température ambiante élevée: si installée dans un assemblage de baie fermé ou contenant plusieurs unités, la température ambiante de l'installation peut etre plus élevée que la température ambiante de la pièce. En conséquence, penser a installer l'équipement dans un environnement compatible avec la température ambiante maximale autorisée (40 C) spécifiée pour l'appareil.
- b. Circulation d'air réduite: installer l'équipement dans une baie de manière a ce que la circulation d'air requise pour faire fonctionner l'équipment en toute sécurité ne soit pas réduite. Ne pas bloquer les côtés de l'appareil, et laisser approximativement un espace de 12 pouces, de préférence 24 pouces, de chaque côté de l'unité pour une ventilation adéquate. L'espace laisse libre pour la circulation de l'air doit être de 12 pouces de chaque côté.
- c. Montage mécanique: monter l'appareil de manière a s'assurer qu'il soit droit dans la baie afin d'éviter de créer une condition dangereuse
- d. Un soin particulier doit etre apporté au branchement de l'équipement au circuit d'alimentation et aux conséquences qu'une charge excessive des circuits pourrait avoir sur le système de protection contre les surcharges et sur le cablâge d'alimentation. Prendre des précautions d'usage en prêtant attention aux normes figurant sur la plaque d'identification de l'équipement.
- e. Mise a la terre fiable: maintenir une mise a la terre fiable de l'équipement monté en baie. L'appareil doit etre vissé sur la baie afin d'assurer une mise a la terre correcte. De plus, faire particulièrement attention aux alimentations en courant autres que celles provenant de connections directes au circuit de dérivation (par exemple utilisation de prises multiples).
- f. Le remplacement du cordon d'alimentation doit comporter le même type de cordon et le même type de prise que ceux livrés avec l'unité.

## **Chapter 7 - XGS12 Chassis Platform**

This chapter provides details about the XGS12 chassis platform, its specifications and features.

The XGS12 Chassis models– XGS12-SD and XGS12-HS are the next generation high performance platform capable of supporting XM form factor load modules. XGS12-SD and XGS12-HS are 12-slot chassis with high-speed backplane designed for aggregation across load modules. These chassis are capable of testing high density, multi-Terabit bandwidth, Carrier class core, edge metro routers and data center switches. This flexible platform supports layer 2-7 testing on a massive scale and provides the most comprehensive solution for performance, functional, security, and conformance testing of network equipment and network applications.

The XGS12 chassis platform has the following features:

- High port densities in 11RU vertical rack space, that reduces space requirements and simplifies management
- High-speed backplane that enables resource aggregation across load modules
- Highly-serviceable with field-replaceable Modular Controller Card (slot 0), Fan Module, and Power Supply Module, enabling simple and quick field service
- The platform is future proof and designed to accept the next generation of load modules

The following are the two XGS12 chassis bundle models:

XGS12 Chassis Bundle Part Numbers, Components and Application Support

Part Number	Chassis	Components	Application Support
940-0006	XGS12-HS	<ul> <li>Chassis frame assembly, w/ STD SYNC (941-0041)</li> <li>High Performance Processor Module (942-0048)</li> <li>Fan assembly module (942-0031)</li> <li>6000W power supply module (942-0032)</li> <li>Linux and Windows 7 operating systems</li> </ul>	<ul><li>BPS</li><li>IxLoad</li><li>IxNetwork</li></ul>
940-0011	XGS12-SD	<ul> <li>Chassis frame assembly, w/ SD SYNC (941-0041)</li> <li>Standard Processor Module (942-0049)</li> <li>Fan assembly module (942-0031)</li> <li>6000W power supply module (942-0032)</li> <li>Windows 7 operating system</li> </ul>	<ul><li>IxLoad</li><li>IxNetwork</li><li>IxN2X</li></ul>

Both XGS12-HS and XGS12-SD chassis bundles require selection of a free IxOS software version. The chassis bundles provide improved modularity and access to the major components to reduce downtime in case of failure.

The four XGS12-HS chassis components that are bundled together are shown in the following table.

XGS12-HS Part Numbers and Modules

Part Num- ber	Description
941-0041	Chassis Frame Assembly, with STD SYNC
942-0048	High Performance Processor Module
942-0031	Fan Assembly Module
942-0032	6000W Power Supply Module

The four XGS12-SD chassis components that are bundled together are shown in the following table.

XGS12-SD Part Numbers and Modules

Part Num- ber	Description
941-0041	Chassis Frame Assembly, with STD SYNC
942-0049	Standard Performance Processor Module
942-0031	Fan Assembly Module
942-0032	6000W Power Supply Module

The XGS12-HS chassis, shown in the following figure, has the following features:

- Allows the hot-swapping of load modules, without requiring the chassis to be powered down.
- The power supplies and fans are accessible from the rear of the chassis.
- Each of the modular components is capable of being removed in the field and replaced with minimum downtime.
- The Processor module, plugged into chassis slot 0 chassis is not hot swappable.

Figure: XGS12-HS Chassis



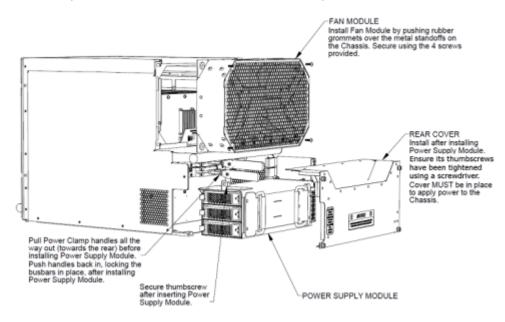
The XGS12-SD chassis, shown in the following figure, has the following features:

- A front to-back airflow system to ensure that all of Ixia's highest-density load modules operate efficiently.
- Each major system component is self-contained and field replaceable.
- The Processor module, plugged into chassis slot 0 chassis is not hot swappable.
- The fan, power supply, and processor components are designed to be readily installed and removed.
- Allows for hot-swapping of XM load modules, which ensures a highly-flexible and multi-user testing environment.
- Ixia's XM load module form factors are supported in the XGS12-SD chassis, providing a seamless integration with existing Ixia test systems.

Figure: XGS12-SD Chassis



The component modules of the XGS12 chassis platform are shown in the following figure:



## **Specifications**

The XGS12 chassis platform model specifications are contained in the following tables.

#### XGS12-HS Processor Module Specifications

Processor Mod- ule	Field replaceable and removable processor card module with 2 x INTEL Sandy Bridge EP, E5-2658 2.1 GHz processors
Memory	64 GB RAM
Hard Disk Drive	Dual 400 GB Solid-State Drives
Operating System	Native Linux OS and Win7 VM for IxOS
Other Specs	IPMI support

#### XGS12-SD Processor Module Specifications

	d312-3D Flocessor Module Specifications
Processor Mod- ule	Field-replaceable and removable processor card module with an Intel E5 2620 processor with 16GB CPU memory and 1TB SATA hard drive
Memory	4GB
Hard Disk Drive	250GB
Operating System	Windows 7 Professional, 32-bit version
	Battery replacement: Danger of explosion if battery is incorrectly replaced. You should not attempt to replace the battery. Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries according to the battery manufacturer's instructions.
	Remplacement de la batterie: Le remplacement incorrect de la batterie peut provoquer une explosion. Vous ne devez en aucun casessayer de remplacer la batterie. Renvoyez le produit au service clients Ixia pour un échange avec le mêmetype de batterie ou un type équivalent. Ixia met les batteries usagées au rebut conformémentaux instructions du fabricant.
	The serial number for the Processor Module is located on module itself. This is used as the overall chassis serial number.

## XGS12 Chassis Platform Specifications

	• 19.0 in. W x 19.21 in. H x 27.2 in. D
Size	• 48.26cm W x 48.79cm H x 69.09cm D
	11 rackmount units (11RU)

Load Module Slots	12 (compatible with Ixia XM form factor load modules)
	The chassis requires three single phase, 200-240VAC, 50/60Hz circuits, each capable of providing 3680 watts. These circuits must provide protection against over-currents, short circuits and earth faults for the XGS12 chassis platform. A 20A circuit breaker for each circuit is also required.
Chassis Power	All three power cords must be plugged into their single phase 200-240VAC, 50Hz/60Hz power sources at the same time for correct operation of the chassis.
	The chassis power supplies are interlocked with the rear cover which must be installed for them to be enabled. After removing or installing the rear panel, ensure thumbscrews have been tightened down with a 'Flat Blade' screwdriver.
	The load module power is enabled by the Ixia server program. If it is not running, the load modules will not be powered on.
	All three power cords are required to operate the XGS12 chassis plat- form power supplies.
	Power Cord shipments:
Power Cords	<ul> <li>Ixia provides three power cords that are configured and rated to meet the specifications of the target country where the chassis is being installed.</li> </ul>
	<ul> <li>For North American customers, the power cords have NEMA L6- 20P plugs for attachment to the power source and IEC-60320-C19 connectors that attach to the XGS12 chassis platform.</li> </ul>
	<ul> <li>For International shipments, the power cords supplied has plugs suitable for each destination country's power source and IEC- 60320-C19 connectors that attach to the XGS12 chassis platform.</li> </ul>
	Frame:
	64 lbs. (29.1 kg) empty, component weight
	• 97 lbs. (44.1 kg) average shipping weight (with filler panels)
Chassis Weights	Fan module:
	<ul><li>10.2 lbs. (4.63 kg) component weight</li><li>17.3 lbs. (7.86 kg) average shipping weight</li></ul>
	Power Supply module:
	28 lbs. (12.72 kg) component weight
	• 35.1 lbs. (15.95 kg) average shipping weight
	Processor module (SD):
	6.4 lbs. (2.9 kg) average shipping weight
	Processor module (HS)

	• 15.8 lbs. (7.17 kg) average shipping weight
	Total chassis weight, without any load modules installed is 112.2 lbs. (50.89 kg). Do not attempt to lift the fully assembled chassis.
	AVERTISSEMENT N'essayez pas de soulever le châssis entièrement assemblé.
Fan Module	Field replaceable chassis fan assembly that is easily installed and removed.
Air flow Clear-	12 inches is required at the rear of the chassis.
ance	24 inches of clearance is preferred.
Power Supply	<ul> <li>Field replaceable power supply module that is easily installed and removed.</li> <li>There are three 2825W power supplies in the Power Supply Mod-</li> </ul>
Module	ule.
	Each power supply may be removed or replaced separately.
Timing Sources	Internal clock, synchronized with another Ixia chassis, GPS AFD-1unit, AFD2 IRIG-B unit or with the Timing Distribution Module.
Shipping Vibra- tion	FED-STD-101C, Method 5019.1/5020.1
	41°F to 104°F, (5°C to 40°C)
Operating tem- perature	Some high-density/high performance load modules require a lower maximum ambient operating temperature than the standard for the chassis. When a load module that requires the lower maximum operating temperature is installed in an XM chassis, the maximum operating temperature of the chassis is adjusted downward to match the maximum operating temperature of the load module. The operating temperature range specification is specified in the published datasheet for these load modules.
Storage tem- perature	41°F to 122°F, (5°C to 50°C)
Operating Humidity	0% to 85%, non-condensing
Storage Humid- ity	0% to 85%, non-condensing
Noise	The XGS12-SD and XGS12-HS chassis running at maximum fan speed capacity may produce noise levels up to 87 dB(A). This is measured per the GR-63-CORE, Issue 1, paragraph 5.6.3 specification. The use of appropriate ear protection is recommended to protect against hearing impairment. Consult local health and safety regulations for recom-

mended maximum exposure levels for noise and ear protection devices.

Shown below are the maximum XGS12-SD and XGS12-HS chassis sound levels measured according to GR-63-CORE, Issue 1, Paragraph 5.6.3.

• Front: 83.5 dB(A)

• Left Side: 84.2 dB(A)

• Rear: 86.5 dB(A)

• Right Side: 84.4 dB(A)

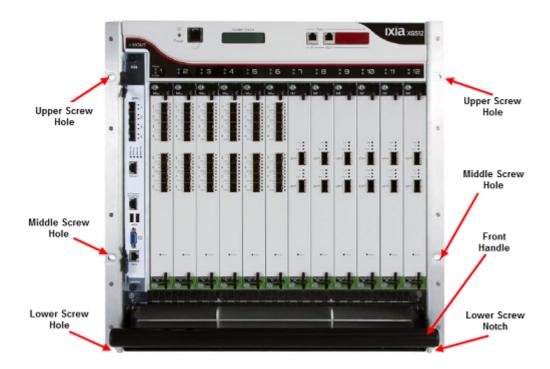
#### **▲**WARNING

**Hearing Protection**: The XGS12-SD and XGS12-HS chassis generates noise levels above 80 dB(A). Ear protection must be worn. The use of appropriate ear protection is recommended to protect against hearing impairment. Consult local health and safety regulations for recommended maximum exposure levels for noise and ear protection devices.

#### XGS12 Chassis controls and indicators

Front Panel Switches	On/Off momentary power push button
Monitor	HD-DB15 Super VGA
Ethernet	XGS12-SD chassis has one RJ-45 10/100/1000Mbps Management port and one RJ-45 RS232 serial port.
Ethernet	XGS12-HS chassis has one RJ-45 1GBaseT/10GBaseT management port and one RJ-45 RS232 serial port.
USB	XGS12-SD chassis has two USB ports and one RJ-45 10/100/1000Mbps Gigabit Ethernet Management Port. Another Gigabit Ethernet Management Port can be provisioned using one of the USB ports.
	XGS12-HS chassis has two USB ports. Additionally there are four SFP+ sockets and one RJ-45 1GBaseT/10GBaseT port.
Sync In	Single Sync In jack with a 4-pin RJ11
Sync Out	Single Sync Out jack with a 4-pin RJ11
	See <u>LEDs/LCD Display</u> .
Front Panel Indicators	2 Paired LEDs above each slot position indicating Power and Active status.
	2x16 LCD on front panel indicating chassis information.
	LEDs on Processor Module indicating power, hard disk activity, and Ethernet activity on each port
Industry Cer- tifications	The chassis safety approvals are UL and CE. These certifications are only valid when the unit is operating as specified.

Figure: Safety Features



#### **XGS12 Chassis Platform Installation Precautions**

XGS12-SD and XGS12-HS chassis installation precautions are as follows:

- The chassis should be installed in the rack before installing the power supply module, fan module and load modules, thereby reducing the weight of the chassis.
- The two lower bolts used to secure the chassis to a rack can be used to hold the chassis frame in place while securing all of the other bolts (See Figure 6-2).
- Secure the chassis to rack face with all six bolts. Fully depress power supply clamps when installing power supply module.
- Secure the power supply module thumb bolt when installing power supply module.
- Install the rear power supply cover before applying AC power.
  - After removing or installing this cover, ensure that the thumbscrews are tightened down with a screwdriver.
- Do not use the chassis without installing the Fan module.
- Do not use the chassis without installing the Processor module.
- Do not leave unused slots open. Use the filler panels to cover the un-used slots. See Installing Filler Panels for more information.
- · Do not block the front air intake.
- A minimum air flow clearance of 12 inches is required. 24 inches of air flow clearance is preferred at the rear of the chassis.
- Operator intervention may be required to power cycle the XGS12 chassis platform or restart a software program in the event the XGS12-SD or XGS12-HS chassis operation is upset or stopped by electrostatic discharge.

## **LEDs/LCD Display**

The XGS12-SD and XGS12-HS chassis have front panel LEDs for each load module slot.

#### XGS12 LEDs

Label	Color	Description
Power	ver Green	When the Power LED is flashing, the board is being detected or initialized.
		The Power LED is illuminated when the board is powered.
In Use	Amber	The Active LED is illuminated when you have taken ownership of the load module.  If you run traffic from IxExplorer, without taking port ownership, the In Use light is not illuminated.

### **LCD Display**

An LCD display is provided on the chassis to indicate the status of the chassis without an external display device (monitor). The LCD operates in two modes:

- Startup: The LCD displays messages from IxServer to indicate the operation of IxServer as it initializes.
- Run: The LCD display provides chassis information. Information displayed includes chassis name, IxOS version, IP address, master/subordinate, and chassis status.

#### **CPU Slot LED Definitions**

The specifications of LEDs for the Processor module and the LEDs above the Processor module slot are shown in the following table:

NOTE

**ESD Discharge**: Operator intervention may be required to power cycle the unit or restart a software program in the event the unit is upset by electrostatic discharge.

#### LED Specifications

	LED	Color	Description
On the chassis front face	CPU card Slot LED	Yellow	The backplane is initializing
		Green	The backplane has initialized
Processor module - front panel	Stdby Pwr LED	Green	5V Stand-by power is available
	CPU Pwr LED	Green	CPU Card power is available
	HDD Act LED		
	Bkpln Link LED	Green	PCIe link to back- plane is up
Processor module - Eth- ernet LEDs for each port	Link LED	Green	Port has link  NOTE Link and Activity

LED	Color	Description
		LEDs are included for all Ethernet ports.
Act LED		Flashes when port has activity

# **Supported Modules**

The modules that are supported on the XGS12 chassis platform are listed in the following table.

Supported Modules

Load Module	XGS12-SD	XGS12-HS
Xcellon-Lava		
<ul> <li>944-1067 Lava AP40/100GE2P 40/100GE Accelerated Performance</li> <li>944-1068 Lava AP40/100GE2RP 40/100GE Reduced</li> <li>944-1074 Lava AP40/100GE2P-NG 40/100GE FUSION</li> </ul>	Yes	Yes
Xcellon-Multis		
<ul> <li>944-1100 XM100GE4CXP, 4-port 100GE only</li> <li>944-1101 XM100GE4CXP+FAN, 40/100GE with 3x40GE fanout perport</li> <li>944-1102 XM40GE12QSFP+FAN, 12-ports 40GE CXP</li> <li>944-1105 XM10/40GE12QSFP+FAN, 12-port QSFP</li> <li>944-1109 XM10/40GE6QSFP+FAN, 6-port QSFP</li> <li>944-1114 Xcellon-Multis XMR40GE12QSFP+40GE, RED,12P,LM</li> <li>944-1115 Xcellon-Multis XMR40GE6QSFP+40GE, RED,12P,LM</li> <li>947-5053 Xcellon-Multis XMR10GE32SFP+FAN, 10GE Bundle</li> <li>947-5054 Xcellon-Multis XMR10GE16SFP+FAN, 10GE Bundle</li> <li>944-1110 Xcellon-Multis XM100GE4CFP4, 100GE CFP4</li> </ul>	Yes	Yes

Load Module	XGS12-SD	XGS12-HS
<ul> <li>944-1116 Xcellon-Multis         XM100GE4QSFP28, 100GE QSFP28</li> <li>944-1117 Xcellon-Multis         XM100GE4QSFP28+ENH, enhanced high         density, 100GE QSFP28</li> <li>944-1111 Xcellon-Multis         XM100GE4CFP4+ENH, enhanced high         density, 100GE CFP4</li> </ul>		
Xcellon-Flex		
<ul> <li>944-1060 FlexAP10G16S</li> <li>944-1061 FlexFE10G16S</li> <li>944-1062 FlexAP10/4016SQ (Combo)</li> <li>944-1065 FlexFE40G4Q (4x40GE)</li> </ul>	Yes	Yes
Yukon/NGY		
<ul> <li>944-0043 LSM10GXMR4-01, 4-port, Red</li> <li>944-0044 LSM10GXMR8-01, 8-port, Red</li> <li>944-0048 LSM10GXM2XP-01, 2-port</li> <li>944-0049 LSM10GXMR2-01, 2-port, Red</li> <li>944-0059 LSM10GXM4XP-01, 4-port</li> <li>944-0060 LSM10GXM8XP-01, 8-port</li> <li>944-1070 LSM10GXM8NG-01, 8-port</li> <li>944-1071 LSM10GXM4NG-01, 4-port</li> <li>944-1096 LSM10GXM2NG-01, 2-port</li> <li>944-0050 LSM10GXM4S-01, 4-port, SFP+</li> <li>944-0051 LSM10GXM8S-01, 8-port, SFP+</li> <li>944-0052 LSM10GXMR4S-01, 4-port, SFP+</li> <li>944-0053 LSM10GXMR8S-01, 8-port, SFP+</li> <li>Red</li> <li>944-0054 LSM10GXMR2S-01, 2-port, SFP+</li> <li>944-0055 LSM10GXMR2S-01, 2-port, SFP+</li> <li>944-1075 LSM10GXM8S-NG, 8-port 10GE SFP+</li> <li>944-1076 LSM10GXM4S-NG, 4-port SFP+</li> <li>944-1077 LSM10GXM2S-NG, 2-port SFP+</li> <li>944-0074 LSM10GXM2S-NG, 2-port SFP+</li> </ul>	Yes	Yes

Load Module	XGS12-SD	XGS12-HS
Red • 944-0076 LSM10GXM4GBT-01, 4-port • 944-0077 LSM10GXMR4GBT-01, 4-port, Red • 944-0078 LSM10GXM8GBT-01, 8-port • 944-0079 LSM10GXMR8GBT-01, 8-port, Red • 950-0002 FCMGXM8S-01, 8-Port Fibre Channel Load Module		
944-0095 LSM1000XMVDC4-01 GbE, 4-Port Dual-PHY		
944-0096 LSM1000XMVDC8-01 GbE, 8-Port Dual-PHY		
944-0097 LSM1000XMVDC12-01 GbE, 12-Port Dual-PHY		
944-0098 LSM1000XMVDC16-01 GigE, 16-Port Dual-PHY	Yes	Yes
944-1072 LSM1000XMVDC16NG GigE, 16-Port Dual-PHY		
944-1095 LSM1000XMVDC4NG, GigE, 4-port Dual-PHY		
XMVR		,
<ul> <li>944-0010 LSM1000XMVR16-01, 16-port, Dual-PHY, Red</li> </ul>		
<ul> <li>944-0029 LSM1000XMVR4-01, 4-port, Dual-PHY, Red (on EOS track)</li> </ul>	Voc	Vac
<ul> <li>944-0031 LSM1000XMVR8-01, 8-port Dual-PHY, Red (on EOS track)</li> </ul>	Yes	Yes
<ul> <li>944-0033 LSM1000XMVR12-01, 12-port Dual-PHY, Red (on EOS track)</li> </ul>		
ImpairNet		,
944-1081 ImpairNet EIM1G4S Gigabit Ethernet Impairment Module		
944-1082 ImpairNet EIM10G4S 10 Gig- abit Ethernet Impairment Module	Yes	Yes
944-1083 ImpairNet EIM40G2Q 40 Gig- abit Ethernet Impairment Module		
(NP) NGY and Xcellon Ultra		

Load Module	XGS12-SD	XGS12-HS
<ul> <li>944-0084 NGY-NP8-01, 10 Gigabit Application Network Processor LM</li> <li>944-0089 NGY-NP4-01, 10 Gigabit Application Network Processor LM</li> <li>944-0090 NGY-NP2-01, 10 Gigabit Application Network Processor LM</li> <li>944-0083 Xcellon-Ultra NP-01, Application Network Processor LM</li> <li>944-1073 Xcellon-Ultra NG, Fusionenabled, Application Load Module</li> <li>947-0029 VQM0001-B1, Solution Bundle</li> </ul>	Yes	Yes
PerfectStorm (Fusion)		
<ul> <li>944-1201 PerfectStorm 40GE Fusion 2-port Load Module, QSFP+</li> <li>944-1200 PerfectStorm 10GE Fusion 8-port Load Module, SFP+</li> <li>944-1209 PerfectStorm 10/1GE Fusion 4-port Load Module, SFP+</li> <li>944-1210 Perfect Storm 10GE Fusion 2-port Load Module, SFP+</li> <li>944-1202 PerfectStorm 100GE Fusion 1-port Load Module, CXP</li> </ul>	No	Yes
PerfectStorm (Non-Fusion)		
<ul> <li>944-1204 PerfectStorm 10GE 8-port Load Module, SFP+</li> <li>944-1205 PerfectStorm 40GE 2-port Load Module, QSFP+</li> <li>944-1207 PerfectStorm 10GE 4-port Load Module, SFP+</li> <li>944-1208 PerfectStorm 10GE 2-port Load Module, SFP+</li> <li>944-1206 PerfectStorm 100GE 1-port Load Module, CXP</li> </ul>	Yes	Yes
XAIR		
949-1008 IXLOAD-WRLS XAIR XM Module     LTE Multi-UE RLC/MAC/PHY one sector simulation.	Yes	Yes
Standard Form Factor LMs requiring Adap	oter module	
<b>ATM</b> • 946-0001 LM622MR-512, OC3/OC12	No	No

Load Module	XGS12-SD	XGS12-HS
ATM/POS, Load Module, 2-port		
POS		
<ul> <li>944-0012 MSM10G1-02, 10 Gigabit Ethernet OC192 Load Module, 1-Port</li> <li>945-0003 MSM2.5G1-01, OC48 Load Module, 1-Port</li> </ul>		
1G		
• 944-0019 LM1000STXS4-256, Gigabit Ethernet Load Module, 4-Port		
10G		
• 944-0022 LSM10G1-01, 10 Gigabit Eth- ernet Load Module, 1-Port		

## **Hot-Swap Procedure**

Each XGS12 platforms – XGS12-SD and XGS12-HS provide the ability of removing and reinstalling a load module without requiring the removal of power from the rest of the chassis. The process of removing/installing a Load Module does not impact either the operation of the OS or remaining load modules installed in the chassis.

The hot-swap procedure is detailed in Appendix D Hot-Swap Procedure.

## **Cooling Fan Speed Control**

The XGS12 platforms – XGS12-SD and XGS12-HS automatically monitor and measure the temperature of installed load modules. The XGS12 platforms – XGS12-SD and XGS12-HS, automatically adjust the fan speed to maintain proper cooling.

## Power outage recovery and Automatic booting scenario

The BIOS on the XGS12 platforms – XGS12-SD and XGS12-HS, is set to Power On after a power failure.

The XGS12-SD chassis will start up, boot Windows 7 and automatically login to the Ixia user account. Anything that is in the Startup folder will also launch.

## **Rack Mount Cautions**

CAUTION	If this unit is installed in a network equipment rack, please observe the fol-
	lowing precautions.

1. Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the chassis (40° C).

- Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced. Do not block the back or the front of the chassis, and leave approximately 12 inches of space, 24 inches preferred, for the back of the unit for proper ventilation. The air flow clearance should be 12 inches on the front.
- 3. Mechanical Loading: Mount the chassis so that it is level in the rack and that a hazardous condition is not caused. Please install all six mounting bolts.
- 4. Circuit Overloading: Consider the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Pay attention to equipment nameplate ratings when addressing this concern.
- 5. Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Chassis frame should be screwed down to racks to ensure proper grounding path. In addition, pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).
- 6. Replacement of the power supply cord must be of the same type of cord and plug configuration that was shipped with the unit.

## Précautions relatives au montage en rack

ATTENTION Si cot

Si cette unité est installée dans une baie d'équipement réseau, observer les précautions suivantes:

- a. Température ambiante élevée: si installée dans un assemblage de baie fermé ou contenant plusieurs unités, la température ambiante de l'installation peut etre plus élevée que la température ambiante de la pièce. En conséquence, penser a installer l'équipement dans un environnement compatible avec la température ambiante maximale autorisée (40 C) spécifiée pour l'appareil.
- b. Circulation d'air réduite: installer l'équipement dans une baie de manière a ce que la circulation d'air requise pour faire fonctionner l'équipment en toute sécurité ne soit pas réduite. Ne pas bloquer les côtés de l'appareil, et laisser approximativement un espace de 12 pouces, de préférence 24 pouces, de chaque côté de l'unité pour une ventilation adéquate. L'espace laisse libre pour la circulation de l'air doit être de 12 pouces de chaque côté.
- c. Montage mécanique: monter l'appareil de manière a s'assurer qu'il soit droit dans la baie afin d'éviter de créer une condition dangereuse
- d. Un soin particulier doit etre apporté au branchement de l'équipement au circuit d'alimentation et aux conséquences qu'une charge excessive des circuits pourrait avoir sur le système de protection contre les surcharges et sur le cablâge d'alimentation. Prendre des précautions d'usage en prêtant attention aux normes figurant sur la plaque d'identification de l'équipement.
- e. Mise a la terre fiable: maintenir une mise a la terre fiable de l'équipement monté en baie. L'appareil doit etre vissé sur la baie afin d'assurer une mise a la terre correcte. De plus, faire particulièrement attention aux alimentations en courant autres que celles provenant de connections directes au circuit de dérivation (par exemple utilisation de prises multiples).
- f. Le remplacement du cordon d'alimentation doit comporter le même type de cordon et le même type de prise que ceux livrés avec l'unité.

## **Chapter 8 - XGS2 Chassis Platform**

This chapter provides details about the XGS2 chassis platform, its specifications and features.

The 2-slot XGS2 chassis models - XGS2-SD and XGS2-HS provide highly flexible and portable chassis that powers load modules and test applications to create an Ixia test system. The XGS2 platform provides the foundation for a complete benchtop or rackmount test environment. The chassis platform supports Ixia applications for performance, functional, conformance, and security testing.

The XGS2 chassis platform has the following features:

- Provides a single platform for running a wide array of security, data, routing, and bridging protocol emulation; and signaling, voice, video, and application testing.
- Provides extensive 10Mbps to 100Gbps interface support.
- Can swap load modules in and out of the test bed without disrupting the ongoing test that is using installed modules.
- Has a high-speed backplane to support the high bandwidth requirements of largescale application tests.
- Has highly serviceable modular components consisting of the chassis controller module, fan module, sync module and power supply module.
- Allows you to Daisy-chain the XGS2 with these other Ixia chassis: XGS2-HS, XGS2-SD, XGS12-SD, XGS12-HS, XG12, XM12 HP, XM2, and 400Tv2.

The following are the two XGS2 chassis bundle models:

XGS2 Chassis Bundle Part Numbers, Components and Application Support

Part Number	Chassis	Components	Application Support
940-0012	XGS2-HS	<ul> <li>Chassis frame assembly</li> <li>High Performance Controller Module (942-0048)</li> <li>Fan assembly module</li> <li>2 Power supplies</li> <li>Standard Star Topology Sync module.</li> </ul>	<ul><li>BPS</li><li>IxLoad</li><li>IxNetwork</li><li>IxExplorer</li></ul>
940-0010	XGS2-SD	<ul> <li>Chassis frame assembly</li> <li>Standard Performance Controller Module (942-0049)</li> <li>Fan assembly module</li> <li>2 Power supplies</li> <li>Standard Star Topology Sync module.</li> </ul>	<ul><li>IxLoad</li><li>IxNetwork</li><li>IxN2X</li><li>IxExplorer</li></ul>

Both XGS2-HS and XGS2-SD chassis bundles require selection of a free IxOS software version. The chassis bundles provide improved modularity and access to the major components to reduce downtime in case of failure.

The XGS2-HS and XGS2-SD chassis, have the following benefits:

- Allows use of Ixia load modules in a small footprint chassis
- Has a high-speed backplane to support the high bandwidth requirements of largescale application tests.
- Has field-replaceable modular chassis synchronization unit that is easy to service.
- Provides better cooling by using front-to-back airflow
- Allows time synchronization using signal antenna: GPS with AFD1 or IRIG-B with AFD2 unit.

Figure: XGS2-HS Chassis



Figure: XGS2-SD Chassis



# **Specifications**

The XGS2 chassis platform model specifications are contained in the following tables.

XGS2 Chassis Platform Specifications

Slots	2 (compatible with Ixia XMFF load modules)
Size	<ul> <li>17.5 in. width (19.0 in. with rackmount bracket installed) x 5.1 in. height x 26.5 in. depth</li> <li>3 rackmount units (3RU)</li> </ul>
	XGS2-HS weighs 55 lbs. (25 kg)
Woight	• 71.3 lbs. (32.4 kg) average shipping weight
Weight	XGS2-SD weighs 53 lbs. (24 kg)
	• 69.3 lbs. (31.5 kg) average shipping weight
Chassis Power	<ul> <li>Two single phase power supplies rated 20A@110VAC; 60/50 Hz</li> <li>Two single phase power supplies rate 10A@220VAC; 60/50 Hz</li> <li>Supports an additional power supply that can be purchased for redundancy</li> </ul>
Timing Source	Internal or synchronized with another Ixia chassis, or external with the Ixia AFD1 appliance for a GPS time sources, or the Ixia AFD2 appliance for BITS and IRIG-B time format input with additional 1PPS input.
Operating System	<ul> <li>XGS2-HS: Native Linux and Windows 7 VM</li> <li>XGS2-SD: Windows 7, 32-bit version</li> </ul>
Chassis Con- troller Module	<ul><li>Field-replaceable</li><li>USB ports for connecting accessories</li></ul>
Temperature	<ul> <li>Operating: 41°F to 104°F (5°C to 40°C)</li> <li>Storage: 41°F to 122°F (5°C to 50°C)</li> </ul>
Humidity	<ul><li>Operating: 0% to 85%, non-condensing</li><li>Storage: 0% to 85%, non-condensing</li></ul>
Connectors	<ul> <li>Video: HD-DB15 Super VGA</li> <li>USB: Two Dual Type A, 4-pin jack connectors</li> <li>Management: 10/100/1000 Ethernet RJ45</li> <li>Serial: One RJ-45 RS-232 port</li> </ul>
Switches and Indicators	<ul> <li>Power, Standby, Master, External Clock</li> <li>LCD screen with chassis status information</li> <li>Two paired LEDs next to each slot position indicating slot power and card ownership</li> </ul>
Fans	One field-replaceable fan-tray assembly that is easily installed and removed

Noise	XGS2-SD and XGS2-HS chassis models running at maximum fan speed capacity may produce noise levels up to 80 dB(A). This is measured per the GR-63- CORE, Issue 1, and paragraph 5.6.3 specification. The use of appropriate ear protection is recommended to protect against hearing impairment. Consult local health and safety regulations for recommended maximum exposure levels for noise and ear protection devices.
	Fan speed is variable and adjusted based on present load and temperatures within the chassis.

#### **XGS2 Chassis Platform Installation Precautions**

XGS2-SD and XGS2-HS chassis installation precautions are as follows:

- The chassis should be installed in the rack before installing the power supply module, fan module and load modules, thereby reducing the weight of the chassis.
- The two lower bolts used to secure the chassis to a rack can be used to hold the chassis frame in place while securing all of the other bolts (See Figure 6-2).
- Secure the chassis to rack face with all six bolts. Fully depress power supply clamps when installing power supply module.
- Secure the power supply module thumb bolt when installing power supply module.
- Install the rear power supply cover before applying AC power.
  - After removing or installing this cover, ensure that the thumbscrews are tightened down with a screwdriver.
- Do not use the chassis without installing the Fan module.
- Do not use the chassis without installing the Processor module.
- Do not leave unused slots open. Use the filler panels to cover the un-used slots. See Installing Filler Panels for more information.
- · Do not block the front air intake.
- A minimum air flow clearance of 12 inches is required. 24 inches of air flow clearance is preferred at the rear of the chassis.
- Operator intervention may be required to power cycle the XGS2 chassis platform or restart a software program in the event the XGS2-SD or XGS2-HS chassis operation is upset or stopped by electrostatic discharge.

## **LEDs/LCD Display**

The XGS2-SD and XGS2-HS chassis have front panel LEDs for each load module slot.

#### XGS2 LEDs

Label	Color	Description
Power	Green	When the Power LED is flashing, the board is being detected or initialized.
		The Power LED is illuminated when the board is powered.
In Use	Amber	The Active LED is illuminated when you have taken ownership

Label	Color	Description
		of the load module.  If you run traffic from IxExplorer, without taking port ownership, the In Use light is not illuminated.

The XGS2-SD and XGS2-HS chassis have a single bi-color rear panel LED for each load module slot.

#### XGS2 LEDs

Label	Color	Description
Off	Nil	No AC input to PSU.
Power	Solid Green	The main output is ON.  The Power LED is illuminated when the board is powered.
Power Fail- ure	Blinking Amber	Power supply failure (OCP, OVP, OTP, FAN FAULT).
In Standby	Blinking Amber	The main output is OFF.  AC present, Standby ON.

### **LCD Display**

An LCD display is provided on the chassis to indicate the status of the chassis without an external display device (monitor). The LCD operates in two modes:

- Startup: The LCD displays messages from IxServer to indicate the operation of IxServer as it initializes.
- Run: The LCD display provides chassis information. Information displayed includes chassis name, IxOS version, IP address, master/subordinate, and chassis status.

#### **CPU Slot LED Definitions**

The specifications of LEDs for the Processor module and the LEDs above the Processor module slot are shown in the following table:

**ESD Discharge**: Operator intervention may be required to power cycle the unit or restart a software program in the event the unit is upset by electrostatic discharge.

LED Specifications

	LED	Color	Description
On the chassis front face	CPU card Slot LED	Yellow	The backplane is initializing
		Green	The backplane has initialized
Processor module - front panel	Stdby Pwr LED	Green	5V Stand-by power is available

	LED	Color	Description
	CPU Pwr LED	Green	CPU Card power is available
	HDD Act LED		
	Bkpln Link LED	Green	PCIe link to back- plane is up
Processor module - Eth- ernet LEDs for each port	Link LED	Green	Port has link  Link and Activity LEDs are included for all Ethernet ports.
	Act LED		Flashes when port has activity

### **Supported Modules**

The load modules that are supported on the XGS2 chassis platform are listed in the Product Compatibility Matrix:

XGS2-SD: <a href="https://support.ixiacom.com/support-overview/product-support/product-com-patibility-matrix">https://support.ixiacom.com/support-overview/product-support/product-com-patibility-matrix</a>

XGS2-HS: <a href="https://support.ixiacom.com/support-overview/product-support/product-com-patibility-matrix">https://support.ixiacom.com/support-overview/product-support/product-com-patibility-matrix</a>

# **Hot-Swap Procedure**

Each XGS2 platforms – XGS2-SD and XGS2-HS provide the ability of removing and reinstalling a load module without requiring the removal of power from the rest of the chassis. The process of removing/installing a Load Module does not impact either the operation of the OS or remaining load modules installed in the chassis.

The hot-swap procedure is detailed in Appendix D Hot-Swap Procedure.

# **Cooling Fan Speed Control**

The XGS2 platforms – XGS2-SD and XGS2-HS automatically monitor and measure the temperature of installed load modules. The XGS2 platforms – XGS2-SD and XGS2-HS, automatically adjust the fan speed to maintain proper cooling.

### Power outage recovery and Automatic booting scenario

The BIOS on the XGS2 platforms – XGS2-SD and XGS2-HS, is set to Power On after a power failure.

The XGS2-SD chassis will start up, boot Windows 7 and automatically log on to the Ixia user account. Anything that is in the Startup folder will also launch.

### **Rack Mount Cautions**

# **CAUΠΟΝ** If this unit is installed in a network equipment rack, please observe the following precautions.

- 1. Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the chassis (40° C).
- 2. Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced. Do not block the front and back of the chassis, and leave approximately 8 inches of space, on the front and back of the unit for proper ventilation. The air flow clearance should be 8 inches on the front and back of the chassis.
- 3. Mechanical Loading: Mount the chassis so that it is level in the rack and that a hazardous condition is not caused.
- 4. Circuit Overloading: Consideration should be given to the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on over-current protection and supply wiring. Appropriate consideration of equipment nameplate ratings should be used when addressing this concern.
- 5. Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Chassis frame should be screwed down to racks to ensure proper grounding path. In addition, pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).
- 6. Replacement of the power supply cord must be of the same type of cord and plug configuration that was shipped with the unit.



# **Chapter 9 - Optixia X16 Chassis**

This chapter provides details about Optixia X16 chassis its specifications and features.

The Optixia X16 Chassis has 16 slots for support of up to 16 single wide load modules. The Optixia X16 supports all high power load modules with enhanced power supplies and cooling. The Optixia X16 was specifically designed to allow the hot-swapping of modules, without requiring a restart of the chassis. The Optixia X16 is shown in the following figure.

CAUTION	This equipment is intended to be installed and maintained by Service Personnel.

Cet équipement est conçu pour être installé et entretenu par des techniciens de maintenance.

Figure: Optixia X16 Chassis



The Optixia family of chassis has improved data throughput between Load Modules and the chassis. Two methods of data throughput improvements is used: High Speed IxBus and Module to Module data transfer.

The Optixia chassis provides improved modularity of major components to reduce down-time of a failed chassis and reduce the probability of needing to remove a failed chassis from the test environment. Among the modular features provided are:

- Power supplies
- Motherboard and support components (RAM, Hard Drive)
- Backplane power control and interface

Each of the modular components is capable of being removed in the field and replaced with minimum downtime for the customer.

|--|

In the event of indications of inadequate power, remove load modules starting from the low-number slots (slot 1, 2, 3), then working upward toward slot 16 until the problem is solved.

#### **▲WARNING**

To prevent accidental injury to personnel, do not leave unused SFP (or SFP+) ports on load modules uncovered. When transceivers are not installed, end caps must be used. For details, see <a href="Use End Caps on Open Ports">Use End Caps on Open Ports</a>.

#### AVERTISSEMENT

Pour éviter toute blessure accidentelle de vos employés, ne laissez pas les ports SFP (ou SFP+) non utilisés des modules de charge découverts. Lorsqu'il n'y a pas d'émetteurs-récepteurs installés, les capuchons doivent être installés.

### **Specifications**

### X16 Chassis

Optixia X16 computer and chassis specifications are contained in the following table.

Optixia X16 Specifications

CPU	Intel Pentium 4, 3.0 GHz		
	CAUTION  Battery replacement: Danger of explosion if battery is incorrectly replaced. You should not attempt to replace the battery. Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries according to the battery manufacturer's instructions.		
	ATTENTION  Remplacement de la batterie: Le remplacement incorrect de la batterie peut provoquer une explosion. Vous ne devez en aucun casessayer de remplacer la batterie. Renvoyez le produit au service clients Ixia pour un échange avec le mêmetype de batterie ou un type équivalent. Ixia met les batteries usagées au rebut conformémentaux instructions du fabricant.		
Memory	2 GB		
Disk	80GB Sata Disk DVD Drive		
Operating System	Windows XP Professional		
Physical			
Load Module Slots	16		
Size	17.5"w x 14.5"h x 20.5"d		

	(44.5cm x 36.8cm x 52.1cm)		
Weight (empty)	47lbs (21kg)		
Avg. Shipping Wt.	51lbs (23kg)		
Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1		
Environmental			
	41ºF to 104ºF, (5ºC to 40ºC)		
Operating Tem- perature	Some high-density/high performance load modules may require a lower operating temperature; if this is the case, the operating temperature is specified in the load module datasheet.		
Storage	41ºF to 122ºF, (5ºC to 50ºC)		
Humidity			
Operating	0% to 85%, non-condensing		
Storage	0% to 85%, non-condensing		
Clearance	Rear: 4 in (10 cm); fan openings should be clear of all cables or other obstructions. Sides: 2 in (5 cm) unless rack mounted.		
Power	100-240V 60/50Hz 16-8A		
	<b>CAUΠΟΝ</b> The X16 unit requires the building installation to be fitted with a separate circuit fitted with a 20A circuit breaker.		
	The socket/outlets used to power the unit must be installed near the equipment and be easily accessible because the power plug may be used to disconnect the unit from the power source.		
	CAUTION  Replacement of the power supply cord must be conducted by a Service Person. The same type cord and plug configuration shall be utilized.		
	Le remplacement du câble d'alimentation doit être effectué uniquement par un technicien de maintenance. La même configuration câble/prise doit être utilisée.		
Front Panel Switches	On/Off momentary power push button		
Front Panel Connector	Front Panel Connectors		
Mouse	PS/2 6-pin DIN for external mouse		

Keyboard	PS/2 6-pin DIN for external keyboard
Monitor	HD-DB15 Super VGA for external monitor
Printer	Female DB25 parallel port for external printer
Ethernet	RJ-45 10/100/1000Mbps Gigabit Ethernet Management Port
Serial	2 male DB9 ports
USB	4 USB dual type A, 4-pin jack connectors
Sync In	4-pin RJ11
Sync Out	4-pin RJ11
Line In/Line Out/Mic	3.5mm mini-TRS stereo jacks
Back Panel Switches/Connectors	Power On/Off rocker switch
Power	Male receptacle (IEC 60320-C19)
Front Panel Indicators	See <u>" LEDs/LCD Display" below</u>
	2 Paired LEDs above each slot position indicating Power and Active status
	LCD on front panel to display chassis information
	Condition:Ixia XM2
	Front Back Right Left
VM2 N=: C/F	Plugged in not started 56 54 57 58
XM2 Noise Spec(Fan db)	Only CPU Running
	On Low Speed 58 56 58 60
	On Medium Speed-
	On Full Speed 70 67 70 73

# **LEDs/LCD Display**

The Optixia X16 has the following set of front panel LEDs, for each load module slot:

Optixia X16 LEDs

Label	Color	Description
Power	Green	For each load module slot, the Power LED is illuminated when the board is being powered.  When the Power LED is flashing, the board is being detected or initialized.

Label	Color	Description
In Use	Green	For each load module slot, the In Use LED is illuminated when a Load Module in a particular slot is owned by you.

### **LCD Display**

An LCD display is provided on the chassis to indicate the status of the chassis without an external display device (monitor). The LCD operates in two modes:

- Startup: The LCD displays messages from IxServer to indicate the operation of IxServer as it initializes.
- Run: The LCD display provides chassis information. Information displayed includes chassis name, IxOS version, IP address, and chassis status.

### **Supported Modules**

The modules that are supported on the Optixia X16 are listed in the following table.

Optixia X16 Supported Modules

Gigabit Ethernet TXS family	10/100/1000 Ethernet Load Modules
TXS8	10/100 Ethernet Load Module
ALM1000T8	Special 10/100/1000 Ethernet Load Module
ELM1000ST2	Special 10/100/1000 Ethernet Load Module
LM622MR	ATM/POS Load Module
LSM1000POE4-02	4-port PoE Load Module
2.5G MSM POS	OC-48c Load Module
10GE LSM	10 Gigabit Ethernet Load Module, including 10GE LSM MACSec
10G MSM	LAN/WAN/POS Multimode Load Module
PLM1000P4-PD	Power over Ethernet Load Module

### **Hot-Swap Procedure**

Each Optixia X16 chassis provides the ability of removing and reinstalling a Load Module without requiring the removal of power from the rest of the chassis. The process of removing/installing a Load Module does not impact either the operation of the OS or load modules installed in the chassis.

The hot-swap procedure is detailed in Appendix D, Hot-Swap Procedure.

### **Installing Filler Panels**

The airflow in an Optixia X16 chassis can be inefficient if high density load modules are installed in a few slots and the rest of the chassis is left open. For best cooling results,

filler panels are required. It is required that filler panels are used in situations where the slots in the chassis are not all in use.

An empty Optixia X16 chassis includes:

- Three 4-slot wide X16 Filler Panel units (p/n 652-0118-01)
- Two 1-slot wide X16 Filler Panel units (p/n 652-0117-01)
- Screws for attaching the panel faceplates to the chassis

### **Prerequisites for Filler Panel Installation**

- The technician should use industry-standard grounding techniques, such as wrist and ankle grounding straps, to prevent damage to electronic components on any Ixia Load Modules.
- The chassis should be placed in a horizontal position, in a well-lighted work area.

#### **Filler Panel Installation Procedure**

NOTE

**ESD Caution:** Use industry-standard grounding techniques to prevent Electrostatic Damage to the delicate electronic components on the Ixia Load Modules.

#### ATTENTION

**Décharges électrostatiques - Attention**: Utilisez les techniques standard de mise à la terre pour éviter tout dommage électrostatique sur les composants électroniques fragiles des modules de charge Ixia.

1. To install a 4-slot filler panel:

**Example**: Slide the 4-slot filler panel, with the Ixia logo at the top, into Slots 1 through 4. The panel slides in on the slot rails in the chassis. Secure the faceplate of the filler panel to the chassis with 4 of the supplied screws.

2. To install a 1-slot filler panel:

**Example**: Slide the 1-slot filler panel, with the Ixia logo at the top, into the correct slot. The panel slides in on the slot rails in the chassis. Secure the faceplate of the filler panel to the chassis with 2 of the supplied screws.



Use extreme care to prevent damage to delicate electronic components on an adjacent load module. Not using filler panels could cause random failures in port operations or damage installed modules.

#### **Rack Mount Cautions**

CAUTION

If this unit is installed in a Rack Mount, observe the following precautions:

- 1. Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the chassis (40° C).
- 2. Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced. Do not block the back or

- sides of the chassis, and leave approximately two inches of space around the unit for proper ventilation.
- 3. Mechanical Loading: Mount the equipment in the rack so that a hazardous condition is not caused due to uneven mechanical loading.
- 4. Circuit Overloading: Consider the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Pay attention to equipment nameplate ratings when addressing this concern.
- 5. Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Chassis frame should be screwed down to racks to ensure proper grounding path. In Addition, Pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).
- 6. Replacement of the power supply cord must be conducted by a Service Person. The same type cord and plug configuration shall be utilized.

# Précautions relatives au montage en rack

Si cette unité est installée dans une baie d'équipement réseau, observer les précautions suivantes:

- 1. Température ambiante élevée: si installée dans un assemblage de baie fermé ou contenant plusieurs unités, la température ambiante de l'installation peut etre plus élevée que la température ambiante de la pièce. En conséquence, penser a installer l'équipement dans un environnement compatible avec la température ambiante maximale autorisée (40 C) spécifiée pour l'appareil.
- 2. Circulation d'air réduite: installer l'équipement dans une baie de manière a ce que la circulation d'air requise pour faire fonctionner l'équipment en toute sécurité ne soit pas réduite. Ne pas bloquer les côtés de l'appareil, et laisser approximativement un espace de 12 pouces, de préférence 24 pouces, de chaque côté de l'unité pour une ventilation adéquate. L'espace laisse libre pour la circulation de l'air doit être de 12 pouces de chaque côté.
- 3. Montage mécanique: monter l'appareil de manière a s'assurer qu'il soit droit dans la baie afin d'éviter de créer une condition dangereuse
- 4. Un soin particulier doit etre apporté au branchement de l'équipement au circuit d'alimentation et aux conséquences qu'une charge excessive des circuits pourrait avoir sur le système de protection contre les surcharges et sur le cablâge d'alimentation. Prendre des précautions d'usage en prêtant attention aux normes figurant sur la plaque d'identification de l'équipement.
- 5. Mise a la terre fiable: maintenir une mise a la terre fiable de l'équipement monté en baie. L'appareil doit etre vissé sur la baie afin d'assurer une mise a la terre correcte. De plus, faire particulièrement attention aux alimentations en courant autres que celles provenant de connections directes au circuit de dérivation (par exemple utilisation de prises multiples).
- 6. Le remplacement du cordon d'alimentation doit comporter le même type de cordon et le même type de prise que ceux livrés avec l'unité.



# Chapter 10 - IXIA 400T Chassis

This chapter provides details about Ixia 400T chassis its specifications and features.

The IXIA 400T is shown in the below figure. The IXIA 400T chassis has 4 slots for Ixia Load Modules, but may also be used to support the high-powered load modules, including all OC192 and 10GE modules. The IXIA 400T Chassis is specifically designed to accommodate up to 2 OC192/10GE Load Modules and up to 3 TXS8, TXS4 or SFPS4 Load Modules. It has an enhanced power supply, providing more than twice the power of the original IXIA 400T chassis. Additional cooling fans have been added to the 400T chassis to meet the requirements of the high-powered modules.

The Ixia 400T chassis must only be operated in the horizontal position as shown in the following figure.

Figure: Ixia 400T Chassis



**▲**WARNING

In order to prevent accidental injury to personnel, do not leave unused SFP (or SFP+) ports on load modules uncovered. When transceivers are not installed, end caps must be used. For details, see <a href="Use End Caps on Open Ports">Use End Caps on Open Ports</a>.

#### AVERTISSEMENT

Pour éviter toute blessure accidentelle de vos employés, ne laissez pas les ports SFP (ou SFP+) non utilisés des modules de charge découverts. Lorsqu'il n'y a pas d'émetteurs-récepteurs installés, les capuchons doivent être installés.

# **Specifications**

#### **400T Chassis**

The computer specifications are contained in the following table.

IXIA 400T Chassis Specifications

CPU	Intel Celeron 1.2Ghz	
	CAUTION	Battery replacement: Danger of explosion if battery is incorrectly replaced. You should not attempt to replace the battery. Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries

	CAUTION according to the battery manufacturer's instructions.		
	Remplacement de la batterie: Le remplacement incorrect de la batterie peut provoquer une explosion. Vous ne devez en aucun casessayer de remplacer la batterie. Renvoyez le produit au service clients Ixia pour un échange avec le mêmetype de batterie ou un type équivalent. Ixia met les batteries usagées au rebut conformémentaux instructions du fabricant.		
Memory	512 MB		
Disk	IDE disk: 250 GB		
Operating System	Windows XP Professional		
Physical			
Load Module Slots	4		
Size	10.25"w x 5.75"h x 16"d (26.1cm x 14.6cm x 40.6cm)		
Weight (empty)	10lbs (4.5kg)		
Avg. Shipping Wt.	16lbs (7.3kg)		
Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1		
Environmental			
	41 <sup>0</sup> F to 104 <sup>0</sup> F, (5 <sup>0</sup> C to 40 <sup>0</sup> C)		
Operating Tem- perature	Some high-density/high performance load modules may require a lower operating temperature; if this is the case, the operating temperature is specified in the load module datasheet.		
Storage	41 <sup>0</sup> F to 122 <sup>0</sup> F, (5 <sup>0</sup> C to 50 <sup>0</sup> C)		
Humidity	·		
Operating	0% to 85%, non-condensing		
Storage	0% to 85%, non-condensing		
Rear: 4 in (10 cm); fan openings should be clear of all ca other obstructions.			
	Sides: 2 in (5 cm) unless rack mounted.		
Power	100-240 V 60/50 Hz 4-2 A		
	The CPU monitors each card's power requirements and refrains from applying power to the backplane if the		

	card's required load would cause the total power to exceed 350W.	
Fuse	4.0A 250V Time Lag	
Front Panel Switches	Momentary Standby Power push button	
Back Panel Switches	Power On/Off rocker switch	
Front Panel Indic- ators	Power, Master, External Clock	
Rear Panel Connector	S	
Power	Male receptacle (IEC 320-C13)	
Keyboard/Mouse	PS/2 6-pin DIN with Y-connector, for external mouse and/or keyboard	
	You <b>must</b> use the supplied Y-cable when using the PS/2 mouse.	
Monitor	HD-DB15 Super VGA for external monitor	
Printer	Female DB25 parallel port for external printer	
Ethernet	2 each RJ-45 10/100Mbps Fully integrated PC with 10/100 NIC	
Com 2	1 male DB9 serial port	
USB	2 USB dual type A, 4-pin jack connectors	
Sync In	4-pin RJ11	
Sync Out	4-pin RJ11	
Trigger In	BNC connector	
	Condition:Ixia XM2	
XM2 Noise Spec(Fan db)	Front Back Right Left	
	Plugged in not started 56 54 57 58	
	Only CPU Running	
	On Low Speed 58 56 58 60	
	On Medium Speed-	
	On Full Speed 70 67 70 73	

### **Use of Filler Panels**

Proper cooling of the cards in the Ixia 400T chassis requires that the Ixia 400T chassis is always mounted in a horizontal position and that the filler panels are installed in the unused slots. High powered cards available for use in the Ixia 400T chassis include all

variants of the OC192 load modules, all variants of the 10GE load modules, and all variants of the ALM1000T8. Refer to <u>Installing Filler Panels</u> for instructions on the installation of filler panels.

### **Rack Mount Cautions**

#### CAUTION

If this unit is installed in a Rack Mount, observe the following precautions:

- 1. Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the chassis (40° C).
- Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced. Do not block the back or sides of the chassis, and leave approximately two inches of space around the unit for proper ventilation.
- 3. Mechanical Loading: Mount the equipment in the rack so that a hazardous condition is not caused due to uneven mechanical loading.
- 4. Circuit Overloading: Consider the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Pay attention to equipment nameplate ratings when addressing this concern.
- 5. Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).

# Précautions relatives au montage en rack

#### ATTENTION

Si cette unité est installée dans une baie d'équipement réseau, observer les précautions suivantes:

- 1. Température ambiante élevée: si installée dans un assemblage de baie fermé ou contenant plusieurs unités, la température ambiante de l'installation peut etre plus élevée que la température ambiante de la pièce. En conséquence, penser a installer l'équipement dans un environnement compatible avec la température ambiante maximale autorisée (40 C) spécifiée pour l'appareil.
- 2. Circulation d'air réduite: installer l'équipement dans une baie de manière a ce que la circulation d'air requise pour faire fonctionner l'équipment en toute sécurité ne soit pas réduite. Ne pas bloquer les côtés de l'appareil, et laisser approximativement un espace de 12 pouces, de préférence 24 pouces, de chaque côté de l'unité pour une ventilation adéquate. L'espace laisse libre pour la circulation de l'air doit être de 12 pouces de chaque côté.
- 3. Montage mécanique: monter l'appareil de manière a s'assurer qu'il soit droit dans la baie afin d'éviter de créer une condition dangereuse
- 4. Un soin particulier doit etre apporté au branchement de l'équipement au circuit d'alimentation et aux conséquences qu'une charge excessive des circuits pourrait avoir sur le système de protection contre les surcharges et sur le cablâge

- d'alimentation. Prendre des précautions d'usage en prêtant attention aux normes figurant sur la plaque d'identification de l'équipement.
- 5. Mise a la terre fiable: maintenir une mise a la terre fiable de l'équipement monté en baie. L'appareil doit etre vissé sur la baie afin d'assurer une mise a la terre correcte. De plus, faire particulièrement attention aux alimentations en courant autres que celles provenant de connections directes au circuit de dérivation (par exemple utilisation de prises multiples).



# Chapter 11 - IXIA 400T v2 Chassis

This chapter provides details about Ixia 400T v2 chassis, its specifications and features.

The IXIA 400T v2 chassis is shown in the following figure. The IXIA 400T v2 chassis has 4 slots for Ixia Load Modules, but may also be used to support the high-powered load modules, including all OC192 and 10GE modules. The IXIA 400T v2 Chassis is specifically designed to accommodate up to 2 OC192/10GE Load Modules and up to 3 TXS8, TXS4 or SFPS4 Load Modules.

NOTE

The Ixia 400T v2 must only be operated in the horizontal position as shown in the following figure.

Figure: Ixia 400T v2 Chassis - Front View



Figure: Ixia 400T v2 Chassis - Rear View



**▲**WARNING

In order to prevent accidental injury to personnel, do not leave unused SFP (or SFP+) ports on load modules uncovered. When transceivers are not installed, end caps must be used. For details, see <a href="Use End Caps on Open Ports">Use End Caps on Open Ports</a>.

AVERTISSEMENT

Pour éviter toute blessure accidentelle de vos employés, ne laissez pas les ports SFP (ou SFP+) non utilisés des modules de charge découverts. Lorsqu'il n'y a pas d'émetteurs-récepteurs installés, les capuchons doivent être installés.

# **Specifications**

#### 400T v2 Chassis

The computer specifications are contained in the following table.

IXIA 400T v2 Specifications

IXIA 400T v2 Specifications  CPU Intel Atom N455 1.66Ghz		
CFU		
	te to vi ty ac	attery replacement: Danger of explosion if bat- ry is incorrectly replaced. You should not attempt replace the battery. Return to Ixia Customer Ser- ce for replacement with the same or equivalent pe of battery. Ixia disposes of used batteries ccording to the battery manufacturer's instruc- ons.
	in si pl cli ba te	emplacement de la batterie: Le remplacement correct de la batterie peut provoquer une explo- on. Vous ne devez en aucun casessayer de rem- acer la batterie. Renvoyez le produit au service ients Ixia pour un échange avec le mêmetype de atterie ou un type équivalent. Ixia met les bat- ries usagées au rebut conformémentaux instructors du fabricant.
Memory	2 GB	
Disk	SATA HDD.250 GB	
Operating System	Windows 7 Ultimate	
Physical		
Load Module Slots	4	
Size	10.25"w x 5.75"h x 18.5"d (26.1cm x 14.6cm x 47cm)	
Weight (empty)	13.65lbs (6.2kg)	
Avg. Shipping Wt.	19.65lbs (8.9kg)	
Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1	
Environmental		
	41°F to 104°F, (5°C to 40°C)	
Operating Tem- perature	may r the ca	high-density/high performance load modules equire a lower operating temperature; if this is se, the operating temperature is specified in the nodule datasheet.
Storage	41ºF to 122ºF, (5ºC to 50ºC)	
Humidity	,	
Operating	0% to 85%, non-condensing	
Storage	0% to 85%, non-condensing	

Rear: 4 in (10 cm); fan openings should be clear of all cables or other obstructions.  Sides: 2 in (5 cm) unless rack mounted.  Power 100-240 V 60/50 Hz 4-2 A  The CPU monitors each card's power requirements and refrains from applying power to the backplane if the card's required load would cause the total power to exceed 350W.  Front Panel Switches Power On/Off rocker switch  Front Panel Indicators Power, Master, External Clock  Rear Panel Connectors  Power Male receptacle (IEC 320-C13)  Reyboard/Mouse PS/2 6-pin DIN with Y-connector, for external mouse and/or keyboard You must use the supplied Y-cable when using the PS/2 mouse.  Monitor HD-DB15 Super VGA for external monitor  Ethernet 1 RJ-45 10/100/1000Base-T Interface  Com 2 male DB9 Serial Port  USB 4 USB dual type A (2 Front Mounted and 2 Rear Mounted), 4-pin jack connectors  Sync In 4-pin RJ11  Sync Out 4-pin RJ11  Condition:Ixia XM2 Front Back Right Left Plugged in not started 56 54 57 58  Only CPU Running On Low Speed 58 56 58 60 On Medium Speed- On Full Speed 70 67 70 73				
Power 100-240 V 60/50 Hz 4-2 A  The CPU monitors each card's power requirements and refrains from applying power to the backplane if the card's required load would cause the total power to exceed 350W.  Front Panel Switches Power On/Off rocker switch  Front Panel Indicators Power, Master, External Clock  Rear Panel Connectors  Power Male receptacle (IEC 320-C13)  Keyboard/Mouse PS/2 6-pin DIN with Y-connector, for external mouse and/or keyboard You must use the supplied Y-cable when using the PS/2 mouse.  Monitor HD-DB15 Super VGA for external monitor  Ethernet 1 RJ-45 10/100/1000Base-T Interface  Com 2 male DB9 Serial Port  USB 4-pin RJ11  Sync Out 4-pin RJ11  Sync Out 4-pin RJ11  Condition:Ixia XM2 Front Back Right Left Plugged in not started 56 54 57 58 Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-	Clearance	Rear: 4 in (10 cm); fan openings should be clear of all cables or other obstructions.		
The CPU monitors each card's power requirements and refrains from applying power to the backplane if the card's required load would cause the total power to exceed 350W.  Front Panel Switches  Back Panel Switches  Power On/Off rocker switch  Front Panel Indicators  Rear Panel Connectors  Power  Male receptacle (IEC 320-C13)  Reyboard/Mouse  Monitor  MD-DB15 Super VGA for external monitor  Ethernet  1 RJ-45 10/100/1000Base-T Interface  Com  2 male DB9 Serial Port  USB  4 USB dual type A (2 Front Mounted and 2 Rear Mounted), 4-pin jack connectors  Sync In  4-pin RJ11  Sync Out  4-pin RJ11  Condition: Ixia XM2  Front Back Right Left Plugged in not started 56 54 57 58  Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-		Sides: 2 in (5 cm) unless rack mounted.		
Front Panel Switches  Momentary Standby Power push button  Back Panel Switches  Power On/Off rocker switch  Front Panel Indicators  Power, Master, External Clock  Rear Panel Connectors  Power  Male receptacle (IEC 320-C13)  Reyboard/Mouse  PS/2 6-pin DIN with Y-connector, for external mouse and/or keyboard You must use the supplied Y-cable when using the PS/2 mouse.  Monitor  HD-DB15 Super VGA for external monitor  Ethernet  1 RJ-45 10/100/1000Base-T Interface  Com 2 male DB9 Serial Port  4 USB  4 USB dual type A (2 Front Mounted and 2 Rear Mounted), 4-pin jack connectors  Sync In  4-pin RJ11  Sync Out  4-pin RJ11  Condition:Ixia XM2  Front Back Right Left Plugged in not started 56 54 57 58  Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-	Power	100-240 V 60/50 Hz 4-2 A		
Switches  Back Panel Switches  Power On/Off rocker switch  Front Panel Indicators  Rear Panel Connectors  Power  Male receptacle (IEC 320-C13)  Reyboard/Mouse  PS/2 6-pin DIN with Y-connector, for external mouse and/or keyboard You must use the supplied Y-cable when using the PS/2 mouse.  Monitor  HD-DB15 Super VGA for external monitor  Ethernet  1 RJ-45 10/100/1000Base-T Interface  Com  2 male DB9 Serial Port  USB  4 USB dual type A (2 Front Mounted and 2 Rear Mounted), 4-pin jack connectors  Sync In  4-pin RJ11  Sync Out  4-pin RJ11  Condition:Ixia XM2 Front Back Right Left Plugged in not started 56 54 57 58  Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-		refrains from applying power to the backplane if the card's required load would cause the total power to		
Front Panel Indicators  Power, Master, External Clock  Rear Panel Connectors  Power Male receptacle (IEC 320-C13)  Reyboard/Mouse PS/2 6-pin DIN with Y-connector, for external mouse and/or keyboard You must use the supplied Y-cable when using the PS/2 mouse.  Monitor HD-DB15 Super VGA for external monitor  Ethernet 1 RJ-45 10/100/1000Base-T Interface  Com 2 male DB9 Serial Port  USB 4-USB dual type A (2 Front Mounted and 2 Rear Mounted), 4-pin jack connectors  Sync In 4-pin RJ11  Sync Out 4-pin RJ11  Condition:Ixia XM2  Front Back Right Left  Plugged in not started 56 54 57 58  Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-		Momentary Standby Power push button		
ators Power, Master, External Clock  Rear Panel Connectors  Power Male receptacle (IEC 320-C13)  Reyboard/Mouse PS/2 6-pin DIN with Y-connector, for external mouse and/or keyboard You must use the supplied Y-cable when using the PS/2 mouse.  Monitor HD-DB15 Super VGA for external monitor  Ethernet 1 RJ-45 10/100/1000Base-T Interface  Com 2 male DB9 Serial Port  USB 4 USB dual type A (2 Front Mounted and 2 Rear Mounted), 4-pin jack connectors  Sync In 4-pin RJ11  Sync Out 4-pin RJ11  Condition:Ixia XM2  Front Back Right Left Plugged in not started 56 54 57 58  Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-	Back Panel Switches	Power On/Off rocker switch		
Power Male receptacle (IEC 320-C13)  Reyboard/Mouse PS/2 6-pin DIN with Y-connector, for external mouse and/or keyboard You must use the supplied Y-cable when using the PS/2 mouse.  Monitor HD-DB15 Super VGA for external monitor  Ethernet 1 RJ-45 10/100/1000Base-T Interface  Com 2 male DB9 Serial Port  USB 4-USB dual type A (2 Front Mounted and 2 Rear Mounted), 4-pin jack connectors  Sync In 4-pin RJ11  Sync Out 4-pin RJ11  Condition:Ixia XM2  Front Back Right Left  Plugged in not started 56 54 57 58  Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-		Power, Master, External Clock		
Reyboard/Mouse  PS/2 6-pin DIN with Y-connector, for external mouse and/or keyboard You must use the supplied Y-cable when using the PS/2 mouse.  Monitor  HD-DB15 Super VGA for external monitor  Ethernet  1 RJ-45 10/100/1000Base-T Interface  Com  2 male DB9 Serial Port  USB  4 USB dual type A (2 Front Mounted and 2 Rear Mounted), 4-pin jack connectors  Sync In  4-pin RJ11  Sync Out  4-pin RJ11  Condition:Ixia XM2 Front Back Right Left Plugged in not started 56 54 57 58 Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-	Rear Panel Connector	S		
Keyboard/Mouse  board  You must use the supplied Y-cable when using the PS/2 mouse.  Monitor  HD-DB15 Super VGA for external monitor  Ethernet  1 RJ-45 10/100/1000Base-T Interface  Com  2 male DB9 Serial Port  USB  4 USB dual type A (2 Front Mounted and 2 Rear Mounted), 4-pin jack connectors  Sync In  4-pin RJ11  Sync Out  4-pin RJ11  Condition:Ixia XM2  Front Back Right Left  Plugged in not started 56 54 57 58  Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-	Power	Male receptacle (IEC 320-C13)		
Monitor HD-DB15 Super VGA for external monitor  Ethernet 1 RJ-45 10/100/1000Base-T Interface  Com 2 male DB9 Serial Port  USB 4 USB dual type A (2 Front Mounted and 2 Rear Mounted), 4-pin jack connectors  Sync In 4-pin RJ11  Sync Out 4-pin RJ11  Condition:Ixia XM2  Front Back Right Left  Plugged in not started 56 54 57 58  Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-	Keyboard/Mouse			
Ethernet 1 RJ-45 10/100/1000Base-T Interface  Com 2 male DB9 Serial Port  USB 4 USB dual type A (2 Front Mounted and 2 Rear Mounted), 4-pin jack connectors  Sync In 4-pin RJ11  Sync Out 4-pin RJ11  Condition:Ixia XM2 Front Back Right Left Plugged in not started 56 54 57 58  Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-		You <b>must</b> use the supplied Y-cable when using the PS/2 mouse.		
Com 2 male DB9 Serial Port  USB 4 USB dual type A (2 Front Mounted and 2 Rear Mounted), 4-pin jack connectors  Sync In 4-pin RJ11  Sync Out 4-pin RJ11  Condition:Ixia XM2 Front Back Right Left Plugged in not started 56 54 57 58  Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-	Monitor	HD-DB15 Super VGA for external monitor		
USB 4 USB dual type A (2 Front Mounted and 2 Rear Mounted), 4-pin jack connectors  Sync In 4-pin RJ11  Sync Out 4-pin RJ11  Condition:Ixia XM2  Front Back Right Left Plugged in not started 56 54 57 58  Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-	Ethernet	1 RJ-45 10/100/1000Base-T Interface		
jack connectors  Sync In 4-pin RJ11  Sync Out 4-pin RJ11  Condition:Ixia XM2 Front Back Right Left Plugged in not started 56 54 57 58  Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-	Com	2 male DB9 Serial Port		
Sync Out  4-pin RJ11  Condition:Ixia XM2  Front Back Right Left  Plugged in not started 56 54 57 58  Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-	USB			
Condition:Ixia XM2 Front Back Right Left Plugged in not started 56 54 57 58 Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-	Sync In	4-pin RJ11		
XM2 Noise Spec(Fan db)  The spectable of the spectage of the s	Sync Out	4-pin RJ11		
XM2 Noise Spec(Fan db)  Plugged in not started 56 54 57 58  Only CPU Running On Low Speed 58 56 58 60 On Medium Speed-		Condition:Ixia XM2		
XM2 Noise Spec(Fan db)  Only CPU Running  On Low Speed 58 56 58 60  On Medium Speed-		Front Back Right Left		
db) On Low Speed 58 56 58 60 On Medium Speed-		Plugged in not started 56 54 57 58		
On Low Speed 58 56 58 60 On Medium Speed-		Only CPU Running		
		On Low Speed 58 56 58 60		
On Full Speed 70 67 70 73		On Medium Speed-		
		On Full Speed 70 67 70 73		

### **Use of Filler Panels**

Proper cooling of the cards in the Ixia 400T v2 requires that the Ixia 400T v2 chassis is always mounted in a horizontal position and that the filler panels are installed in the unused slots. High powered cards available for use in the Ixia 400T v2 chassis include all variants of the OC192 load modules, all variants of the 10GE load modules, and all variants of the ALM1000T8. Refer to <a href="Installing Filler Panels">Installing Filler Panels</a> for instructions on the installation of filler panels.

### **Rack Mount Cautions**

**CAUTION** If this unit is installed in a Rack Mount, observe the following precautions:

- 1. Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the chassis (40° C).
- Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced. Do not block the back or sides of the chassis, and leave approximately two inches of space around the unit for proper ventilation.
- 3. Mechanical Loading: Mount the equipment in the rack so that a hazardous condition is not caused due to uneven mechanical loading.
- 4. Circuit Overloading: Consider the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Pay attention to equipment nameplate ratings when addressing this concern.
- 5. Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).

### Précautions relatives au montage en rack

ATTENTION Si cette unité est installée dans une baie d'équipement réseau, observer les précautions suivantes:

- 1. Température ambiante élevée: si installée dans un assemblage de baie fermé ou contenant plusieurs unités, la température ambiante de l'installation peut etre plus élevée que la température ambiante de la pièce. En conséquence, penser a installer l'équipement dans un environnement compatible avec la température ambiante maximale autorisée (40 C) spécifiée pour l'appareil.
- 2. Circulation d'air réduite: installer l'équipement dans une baie de manière a ce que la circulation d'air requise pour faire fonctionner l'équipment en toute sécurité ne soit pas réduite. Ne pas bloquer les côtés de l'appareil, et laisser approximativement un espace de 12 pouces, de préférence 24 pouces, de chaque côté de l'unité pour une ventilation adéquate. L'espace laisse libre pour la circulation de l'air doit être de 12 pouces de chaque côté.

- 3. Montage mécanique: monter l'appareil de manière a s'assurer qu'il soit droit dans la baie afin d'éviter de créer une condition dangereuse
- 4. Un soin particulier doit etre apporté au branchement de l'équipement au circuit d'alimentation et aux conséquences qu'une charge excessive des circuits pourrait avoir sur le système de protection contre les surcharges et sur le cablâge d'alimentation. Prendre des précautions d'usage en prêtant attention aux normes figurant sur la plaque d'identification de l'équipement.
- 5. Mise a la terre fiable: maintenir une mise a la terre fiable de l'équipement monté en baie. L'appareil doit etre vissé sur la baie afin d'assurer une mise a la terre correcte. De plus, faire particulièrement attention aux alimentations en courant autres que celles provenant de connections directes au circuit de dérivation (par exemple utilisation de prises multiples).



# **Chapter 12 - XOTN Chassis Unit**

This chapter provides details about the XOTN chassis its specifications and features.

The XOTN chassis unit is a part of the XOTN system. This system allows you to use IxNetwork protocols and scalable data plane test capabilities to test Optical Transport Network (OTN) devices. It provides flexible mapping of Ethernet frames to different OTN rates and structures according to ITU-T G.709.

Each system comprises an XOTN chassis unit, a USB cable, power cord, CFPs, and software. The XOTN ports are configured and managed by the IxNetwork application and can be used with any XM K2 load module (40Gb/s or 100Gb/s).

To test OTN devices, you must connect the XOTN chassis unit to a load module on the Client side, a DUT on the OTN side, and an XM chassis to centrally manage the XOTN chassis units using IxNetwork. Refer to XOTN Installation Guide for installation information and the online help for configuration information.

An XOTN system allows you to convert a 40Gb/s or 100Gb/s Ethernet signal to an Optical Channel Transport Unit (OTU3 or OTU4) signal and vice versa. On the Transmit side, XOTN can generate a PRBS pattern or transmit an Ethernet client signal from IxNetwork. The XOTN chassis unit converts the Ethernet traffic into an OTU3 (43.01Gb/s) or OTU4 (112Gb/s) signal; then transmits it to your OTN DUT. On the Receive side, XOTN receives OTU3 or OTU4 signals from your OTN DUT, converts the signal to 40Gb/s or 100Gb/s Ethernet, then transmits the received traffic to IxNetwork for further analysis. This means you can perform all IxNetwork Ethernet tests on your OTN enabled DUT. You also get detailed OTN statistics on the traffic passing through the XOTN unit.

### **About OTN Technology**

The Optical Transport Network (OTN) emerged in the late 1990's as a "digital wrapper" around client signals before they are transported over a WDM (Wavelength-division multiplexing) network. Since then, the amount of traffic, particularly data and video, has increased significantly, placing higher demands on the edge and core networks. This has been a major driver for the IP-optical integration. There is now an increasing need for a technology to replace the performance monitoring and fault-handling characteristics of SONET/SDH.

The OTN with G.709 framing has emerged as a way to add management capabilities directly to wavelengths. Using this technology, a client signal can be mapped directly into an optical network rather than requiring costly protocols, such as SONET/SDH, to provide the administrative functions.

The XOTN chassis unit is shown in the following figure:



The Part Number of XOTN chassis is 941-0030.

# **Specifications**

### **XOTN Chassis Unit**

The XOTN chassis unit specifications are contained in the following table.

XOTN Specifications		
	CAUTION  Battery replacement: Danger of explosion if battery is incorrectly replaced. You should not attempt to replace the battery. Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries according to the battery manufacturer's instructions.	
	Remplacement de la batterie: Le remplacement incorrect de la batterie peut provoquer une explosion. Vous ne devez en aucun casessayer de remplacer la batterie. Renvoyez le produit au service clients Ixia pour un échange avec le mêmetype de batterie ou un type équivalent. Ixia met les batteries usagées au rebut conformémentaux instructions du fabricant.	
Physical		
Size	<ul> <li>Width: 441.8 mm (17.394")</li> <li>Height: 88.1 mm (3.469")</li> <li>Depth: 500 mm (19.685")</li> </ul>	
Weight	11.5 kg (25.3 lb)	
Environmental		
Operating Tem-	5°C to 35°C (41°F to 95°F)	

perature	
Location	Indoor use only
	Maximum:
Power	5A@115Vac
	3A@230Vac
	90 ~ 264Vac,
	Full Range Input
AC Voltage	Mains supply voltage fluctuations not to exceed $+/-$ 10% of specified nominal voltage.
	Transient overvoltages are specified by Installation category II.
Frequency	47 ~ 63Hz



# **Chapter 13 - Ixia GPS Auxiliary Function Device (AFD1)**

This chapter provides details about Ixia GPS Auxiliary Function Device its specifications and features.

The IXIA Auxiliary Function Device 1 (AFD1) provides the means for accurate worldwide timing using GPS technology. The IXIA AFD1 is shown in the following figure.

Figure: Ixia AFD1



The IXIA AFD1 with integrated Global Positioning System (GPS) is designed for distributed end-to-end measurements of key metrics, including point-to-point latency and jitter.

The Ixia AFD1 GPS receiver is controlled by an Ixia chassis through a USB port. Chassis timing is provided by connecting the Sync Out of the AFD1 to the Sync In of the chassis. This configuration then enables the chassis to operate as a subordinate in a virtual chassis chain, with the Ixia AFD1 as the master.

The following figure shows the AFD1 in operation with other chassis in a local chassis chain. Multiple local chassis chains can be collected through GPS into a virtual chassis chain.



The IxExplorer GUI displays the status of the GPS interface to you. The <u>figure</u> below shows the Chassis Properties dialog with status information. The connection is determined to be either *locked* or *unlocked*. In the Locked state, the chassis is locked to GPS time ( GMT ) within 150nS. In the unlocked state, the AFD1 GPS hardware operates to acquire the minimum number of satellites required to achieve accurate GPS timing.

A chassis connected to an AFD1 chassis does not operate properly if set to Synchronous time source, unless the sync cable is disconnected.

The process of generating the Lock status for the AFD1 consists of getting GPS time lock and then synchronizing the internal clock to the GPS clock. The AFD1 does not enter the `Lock' state until both of these conditions are met. In the unlocked state, the chassis in the unlocked chain are not accurately time synchronized to the rest of the chain.

In operation, once a chassis chain is constructed and the chassis are synchronized, you can clear the timestamps to provide a baseline time for all chassis in the chain. The chain operations are then locked until such time that the GPS lock is lost by a member of the chain.

Data sent from one port in the chain to another provides one-way latency measurements by subtraction of the transmit time stamp from the receive time stamp.

For large or very remote chassis chains, the chassis chain properties provide an offset delay. This delay is defaulted to five seconds. For chassis chains where the communication delays are significant, as in worldwide or large chains, a longer delay should be selected to allow for setup communication delays. The delay is the time of a particular chassis operation (for example, start transmit, stop transmit) plus the configured delay for any synchronous operation. When an operation for the entire chain is executed, this delay is added to the operation. A dialog opens indicating that the operation is in process when the delays are significant.

The chassis time is taken from any chassis with a GPS interface attached. The setup for the chassis chain requires that all chassis in the chain be locked. This is indicated in the IxExplorer GUI. The IxExplorer GUI also provides antenna information such as satellite strength, to enable installation of the antenna in a location with a good `view' of the satellites.

The critical operation for a virtual chain is the reset of the System Time Stamps. All other actions are dependent on the synchronous execution of this operation. To reset time stamps for a GPS-connected system, the reset operation needs to be executed for the chassis chain, and not for the individual chassis.

Chassis Properties for Chassis 01 X General Time Source | Safety Features | Logging and Alerts | IxPiemotelp | Timer Source If set to Synchronous time source, a chassis C Synchronous connected to GPS does not operate properly @ GPS (AFD1) unless the sync cable is disconnected. **GPS Status** Locked Satelites Used 04 Lock Status Sat 1 ID:SNR[dBHZ] 27:34 23.13.39 UTC Time Sat 2 ID:SNR(d8HZ) 25:36 UTC 02:07:2007 Day Month Year Sat 3 ID: SNR(dBHZ) 23:37 Sal 4 ID:SNR(dBHZ) 08:34 0x000F Position Fix Valid SPS DK. Cancel

Figure: Chassis Properties AFD1-Time Source

# **AFD1 Setup**

#### The AFD1 Kit:

The AFD1 kit comes with cables and items required to install and connect the AFD1 in a lab. The AFD1 kit does not include the cable and antenna for permanent installation at a particular site. The antenna and cable kits need to be ordered separately after a site survey determines the site requirements.

The kit contains the following items:

- AFD1 chassis
- · AFD1 chassis rack mount ears
- 3-foot sync cable
- · 6-foot USB cable
- · Window antenna

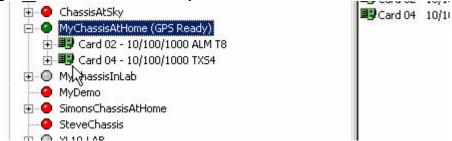
The AFD1 installation uses the USB cable for communication and power. The Ixia chassis automatically detects the connections.

The window antenna is included in the kit for demo use only and does not reliably provide a stable lock environment. For permanent installations, order either the 75-foot or 200-foot cable and antenna kits.

### Successful GPS Synchronization in IxExplorer

In the Chassis Properties dialog of IxExplorer, after selection of GPS as the timer source, the satellites used are displayed. In the preceding <u>figure</u>, satellite 04 is being used and the status is `locked'. In the chassis tree view of IxExplorer, the chassis status is shown as `GPS Ready' if it has successfully locked onto satellite signal. The highlighted chassis is GPS enabled and ready.





### **Enabling/Installing GPS Based Synchronization**

This procedure to set the time source needs to be followed only for the initial installation of the AFD1 GPS unit. Thereafter, upon subsequent restarts, the chassis and AFD1 unit starts fully operational.

1. Start the chassis without attaching the AFD1 GPS unit. Note the message regarding timing source, as shown in the following figure.

Figure: IxServer Start Log Before Attaching AFD1



Attach the AFD1 GPS unit by plugging in the USB and the Sync cables.
 When the chassis detects the GPS (AFD1) unit, it prompts to restart the IxServer, as shown in the following figure.

IXServer

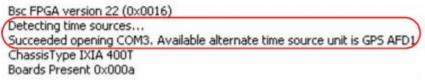
Time source change detected. Closing IxServer, restart required.

OK

3. Click **OK** to restart IxServer.

IxServer restarts, then detects GPS as the timing source and configures the chassis as a subordinate, since the chassis is receiving its timing through sync cable from the ADF1 GPS source. The expected log messages are shown in the following figures.

Figure: IxServer Log - GPS AFD1 Detected



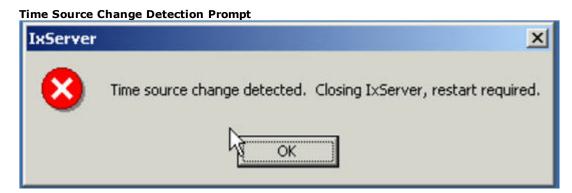
GPS AFD1 is detected and COM3 port is indicated as the communication channel between chassis and AFD1.

Figure: IxServer Log - Chassis Configured as Slave to AFD1
Feedback connection to IxDodServer established.
PowerUp
Chassis is slave
Download C:\Program Files\Tyia\Engals013801a bey

The chassis is configured as a subordinate to AFD1.

4. Open IxExplorer. In the **Chassis Properties** dialog box select GPS (AFD1) timer source, as depicted in the figure.

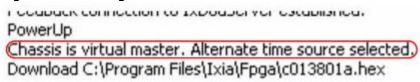
Upon selection of GPS option, IxServer must be closed and restarted for the changes to take effect, as the prompt in the following figure depicts.



5. Click OK to restart IxServer.

Once IxServer is restarted, the IxServer Log shows the AFD1 GPS unit is detected as the time source and the chassis is designated as `Virtual Master' rather than subordinate. See the following figure.

Figure: IxServer Log - Chassis is Virtual Master



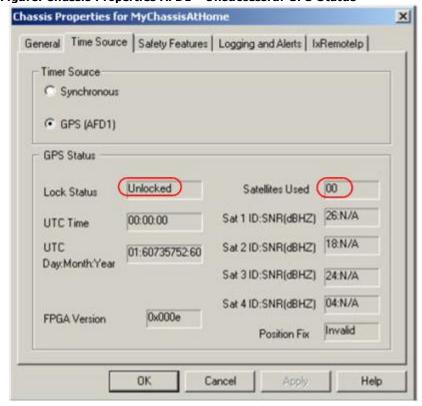
6. Check IxExplorer for GPS status, as shown in the <u>figure</u>. Satellite details changes periodically showing satellite number and signal strength. A good signal strength has SNR reading of more than 35.

Now the chassis is ready for operation based on GPS time source.

### Troubleshooting GPS Unit `Not Ready'

If, after completing installation by following the steps above, there is no GPS information and the status is `Unlocked' in the Time Sources tab of Chassis Properties in IxExplorer (See the following figure), then follow the steps mentioned here to ensure that the ADF1 unit comes up fully functional.

Figure: Chassis Properties AFD1 - Unsuccessful GPS Status



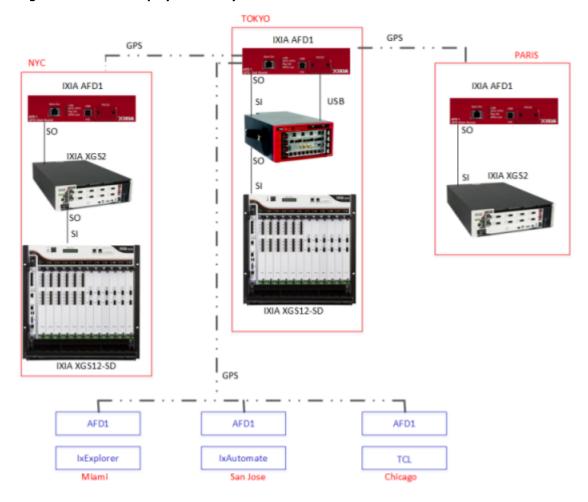
- 1. Ensure that the GPS Antenna has good positioning. Position the antenna outdoors with a clear view of the sky. Refer to <a href="Appendix C">Appendix C</a>, GPS Antenna Installation Requirements.
- 2. Ensure that the antenna cabling is correctly fitted. Reseat the coaxial cable into the AFD1 unit.

Allow five to 10 minutes to see GPS reception become established. A full lock requires three stable satellites.

### **Worldwide Synchronization**

Two or more Ixia chassis connected to a time reference may be distributed worldwide forming a virtual chassis chain based on GPS and/or CDMA timing. One possible configuration is shown in the following figure.

Figure: Worldwide Deployment of Synchronized Chassis



The ports on all of the chassis may be shared by one or more Ixia software users located likewise anywhere in the world. Where GPS and CDMA sources are used, all of the sources must have good quality time values in order for the trigger to be transmitted.

Once the timing features of the chassis is configured, operating a worldwide set of Ixia chassis is the same as local operation. The Ixia hardware and software program the clocks such that they all send a master trigger pulse to all Ixia chassis, within a tolerance of  $\pm 150$  ns with GPS and  $\pm 100$  us for CDMA.

Ixia chassis timing operates by resetting at a fixed time-of-day on all chassis from one source, and then maintaining the time accuracy through various different means. The following table describes the full set of options available and their approximate relative accuracies.

Summary of Timing Options

Available on Devices	Timing Option	Time of Day Accur- acy	Frequency Source	Frequency Accuracy
All Chassis	GPS	150 nano- seconds from GMT	Ixia AFD1	Stratum 1
Ixia 100, 400T	Synchronous	N/A	Internal PC clock	1 micro- second/second
Ixia 100	CDMA	100 micro- seconds from GMT	CDMA	Stratum 2
Ixia 100	GPS (with attached antenna)	150 nano- seconds from GMT	GPS	Stratum 1

### Calculating Latency Accuracy for AFD1 (GPS)

Use the following calculation for latency accuracy for AFD1 ( GPS ) setups.

Latency A to B = Lab

Latency B to A = Lba

Transmit path A to B = T1

Transmit path B to A = T2

Time at A = Ta

Time at B = Tb

Time Absolute = T

Time Error at any site = Terr

Lab=Ta+T1-Tb

Lba=Tb+T2-Ta

Delta L = Lab Lba

Delta L = Ta+T1-Tb (Tb+T2-Ta)

Delta L = T1-T2+2(Ta-Tb)

Delta L = 2(Ta Tb)

If Ta = T+/-Terr and Tb = T+/-Terr

Then

Delta L= 2(T+/-Terr T+/-Terr)

Delta L= 2( |Terr|+|Terr|)

Delta L = 4Terr

### **Front Panel LEDs**

The AFD1 has the following front panel LEDs:

AFD1 LEDs

Label	Color	Description
USB	Green	Indicates that the docnnection is enabled, and blinks with USB activity.
GPS 1PPS	Green	Indicates that the `1 Pulse Per Second' heartbeat is being generated by the GPS hardware. The GPS hardware has acquired at least one satellite and is receiving time information.
Pwr OK	Green	The AFD1 power has been validated.
GPS Lock	Green	Indicates that the GPS hardware has acquired a fix and that the 1PPS timing is valid. It also Indicates that the internal PLL has locked to the 1PPS signal. Testing is invalidated if the GPS Lock signal is not illuminated.

# **IXIA AFD1 Specifications**

The IXIA AFD1 specifications are contained in the following table.

Ixia AFD1 Specifications

General	·
Physical	
Size	9.6"x7"x2.9" ( with feet, 2.70" without feet)
Weight	3.15 lb
Avg. Shipping Wt.	6 lbs
Shipping Vibra- tion	FED-STD-101C, Method 5019.1/5020.1
Environmental	
Temperature	
Operating	41°F to 122°F, (5°C to 50°C)
Storage	41°F to 122°F, (5°C to 50°C)
Power	Worst case power = 2.5W
	5V regulated source

Humidity	
Operating	0% to 85%, non-condensing
Storage	0% to 85%, non-condensing
GPS Func- tionality	
Clock	12.5Mhz System clock
Pulse Width	80 ns
Rear Panel Switches	Reset switch
Front Panel Indicators	USB, GPS PPS, Pwr OK, GPS Lock
Front Panel Con- nectors	
USB Port	Туре В
Sync Out	RJ14
Back Panel Con- nectors	
Antenna	SMA
Power	(not used) 2.0mm Power jack



# Chapter 14 - Ixia IRIG-B Auxiliary Function Device (AFD2)

The IXIA Auxiliary Function Device 2 (AFD2) provides the means for accurate worldwide timing using Inter-Range Instrumentation Group (IRIG-B) technology. The ADF2 decodes the GPS satellites and time information and sends out a pulse to the Optixia chassis. The IXIA /AFD2 is shown in the following figure.

Figure: Ixia AFD2

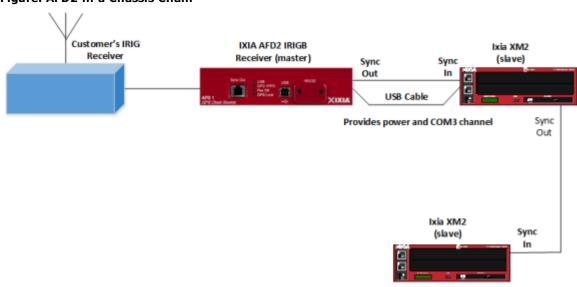


The IXIA AFD2 with integrated IRIG-B is designed to provide 12.5 MHz GPS clock with a programmable 80 ns sync pulse to the Optixia chassis.

The Ixia AFD2 IRIG-B receiver is controlled by an Ixia chassis through a USB port. Chassis timing is provided by connecting the Sync Out of the AFD2 to the Sync In of the chassis. This configuration then enables the chassis to operate as a subordinate in a virtual chassis chain, with the Ixia AFD2 as the master.

The following figure shows the AFD2 in operation with other chassis in a local chassis chain. Multiple local chassis chains can be collected through IRIG-B into a virtual chassis chain.

Figure: AFD2 in a Chassis Chain



The IxExplorer GUI displays the status of the IRIG-B interface to the user. The <u>figure</u> below shows the Chassis Properties dialog with status information. The connection is determined to be either *locked* or *unlocked*. In the Locked state, the chassis is locked to IRIG-B time within 150nS. In the unlocked state, the AFD2 IRIG-B hardware operates to lock its VCXO to 1PPS pulse.

NOTE

A chassis connected to an AFD2 chassis does not operate properly if set to Synchronous time source, unless the sync cable is disconnected.

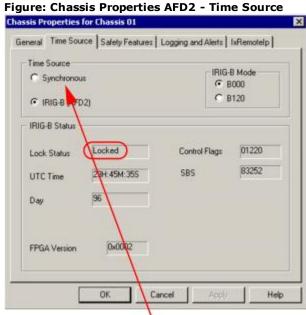
The process of generating the Lock status for the AFD2 consists of getting IRIG-B time lock and then synchronizing the internal clock to the IRIG-B 1PPS pulse. The AFD2 does not enter the `Lock' state until the VCXO lock condition is met. In the unlocked state, the chassis in the unlocked chain are not accurately time-synchronized to the rest of the chain.

In operation, once a chassis chain is constructed and the chassis are synchronized, you can clear the timestamps to provide a baseline time for all chassis in the chain. The chain operations are then locked until such time that the IRIG-B lock is lost by a member of the chain. Data sent from one port in the chain to another provides one-way latency measurements by subtraction of the transmit time stamp from the receive time stamp.

For large or very remote chassis chains, the chassis chain properties provide an offset delay. This delay is defaulted to 5 seconds. For chassis chains where the communication delays are significant, as in worldwide or large chains, a longer delay should be selected to allow for setup communication delays. The delay is the time of a particular chassis operation (for example, start transmit, stop transmit) plus the configured delay for any synchronous operation. When an operation for the entire chain is executed, this delay is added to the operation. A dialog opens indicating that the operation is in process when the delays are significant.

The chassis time is taken from any chassis with a IRIG-B interface attached. The setup for the chassis chain requires that all chassis in the chain be locked. This is indicated in the IxExplorer GUI.

The critical operation for a virtual chain is the reset of the System Time Stamps. All other actions are dependent on the synchronous execution of this operation. To reset time stamps for a IRIG-B-connected system, the reset operation needs to be executed for the chassis chain, and not for the individual chassis.



If set to Synchronous time source, a chassis

connected to IRIG-B does not operate properly unless the sync cable is disconnected.

Chassis Properties, Time Source Tab

Section	Field/Control	Description
Time Source	Synchronous	
	IRIG-B (AFD2)	
IRIG-B Mode	B000	B000 is straight TTL serial output (from the IRIG-B receiver)
	B120	B120 is amplitude modulation (AM) (from the IRIG-B receiver)
IRIG-B Status	Lock Status	Locked = locked to IRIG-B 1PPS input (from IRIG-B receiver)
	UTC Time	UTC Time (display only) in HH:MM:SS comes from the IRIG-B receiver
	Day	Increments from 1 to 366
	Control Flags	These are vendor-specific flags that are passed-through from the IRIG-B receiver
	SBS	Straight Binary Seconds from 1 to xxx each day, starting at midnight. Resets to 0 each midnight.
	FPGA Version	FPGA version

## **AFD2 Setup**

### The AFD2 Kit:

The AFD2 kit comes with cables and items required to install and connect the AFD2 in a lab. The AFD2 kit does not include the IRIG receiver and antenna for permanent installation at a particular site.

The kit contains these items:

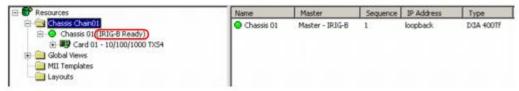
- AFD2 chassis
- · AFD2 chassis rack mount ears
- 3-foot sync cable
- 6-foot USB cable

The AFD2 installation uses the USB cable for communication and power. The Ixia chassis automatically detects the connections.

# Successful IRIG-B Synchronization in IxExplorer

In the Chassis Properties dialog of IxExplorer, after selection of IRIG-B as the timer source, the IRIG-B status is displayed. In the <u>figure</u> above, the status is `locked' to the 1PPS signal coming from the IRIG-B receiver. In the chassis tree view of IxExplorer (see the following figure), the chassis status is shown as `IRIG-B Ready' if it has successfully locked onto the 1PPS signal.

Figure: Chassis Tree View in IxExplorer



### **Enabling/Installing IRIG-B Based Synchronization**

This procedure to set the time source needs to be followed only for the initial installation of the AFD2 IRIG-B unit. Thereafter, upon subsequent restarts, the chassis and AFD2 unit starts up fully operational.

- 1. Set up the antenna and IRIG-B receiver (not supplied by Ixia).
- 2. Connect the 1PPS and IRIG-B outputs from the IRIG-B receiver to the AFD2.
- 3. Connect the sync and USB cables between AFD2 and the Ixia chassis. On the front panel of the AFD2,
  - the Pwr OK indicator lights solid,
  - the 1PPS indicator blinks to indicate the signal from the IRIG-B receiveris good, and
  - · the Lock indicator lights solid.
- 4. Start the chassis. After starting completely, the IxExplorer resource tree is displayed as shown in the preceding figure.
- 5. Note the message regarding timing source, as shown in the following figure.

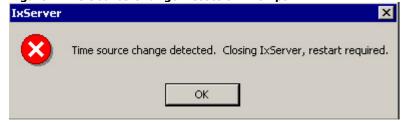
Figure: IxServer Start Log Before Attaching AFD2



### **Changing Time Source**

Any time the clock source is switched, IxServer must be restarted. When the chassis is switched from Synchronous time source to IRIG-B, or vice-versa, the following message is displayed as shown in the following figure.

**Figure: Time Source Change Detection Prompt** 



You are prompted to restart the IxServer. In this example, the time source was changed from synchronous to IRIG-B.

1. Click  $\mathbf{OK}$  and then manually restart IxServer.

IxServer restarts, then detects IRIG-B as the timing source and configure the chassis as a subordinate, since the chassis is receiving its timing through sync cable

from the AFD2 IRIG-B source. The expected IxServer log messages are shown in the following images.

Figure: IxServer Log - IRIG-B AFD2 Detected

```
Bsc FPGA version 4 (0x0004)

Detecting time sources...

Succeeded opening COM6. Available alternate time source unit is IRIG-B AFD2
```

IRIG-B AFD2 is detected and COM6 port is indicated as the communication channel between chassis and AFD2.

```
Figure: IxServer Log - Chassis Configured as Slave to AFD2

PowerUp

Chassis is slave
```

The chassis is configured as a subordinate to AFD2.

### Troubleshooting IRIG-B Unit `Not Ready'

If, after completing installation by following the steps above, there is no IRIG-B information and the status is `Unlocked' in the Time Sources tab of Chassis Properties in IxExplorer (See <a href="Chassis Properties AFD2 - Time Source">Chassis Properties AFD2 - Time Source</a>), then one of the following conditions needs to be corrected.

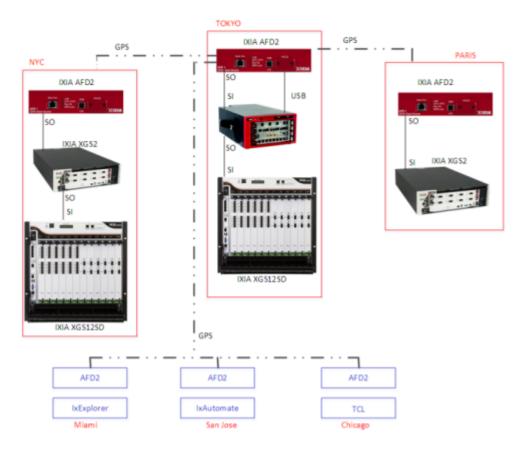
1PPS signal is not connected: check cabling between AFD2 and the IRIG-B receiver.

IRIG-B Mode B000 has been selected, but the IRIG-B receiver is sending B120 signal (or vice versa): change the selection in the Time Sources tab of Chassis Properties in IxExplorer (See <a href="Chassis Properties AFD2 - Time Source">Chassis Properties AFD2 - Time Source</a>), and see if the status is corrected (`Locked') after a short interval.

# **Worldwide Synchronization**

Two or more Ixia chassis connected to a time reference may be distributed worldwide forming a virtual chassis chain based on IRIG-B and/or CDMA timing. One possible configuration is shown in the following figure.

Figure: Worldwide Deployment of Synchronized Chassis



The ports on all of the chassis may be shared by one or more Ixia software users located likewise anywhere in the world. Where IRIG-B and CDMA sources are used, all of the sources must have good quality time values in order for the trigger to be transmitted.

Once the timing features of the chassis is configured, operating a worldwide set of Ixia chassis is the same as local operation. The Ixia hardware and software program the clocks such that they all send a master trigger pulse to all Ixia chassis, within a tolerance of  $\pm 150$  ns with IRIG-B and  $\pm 100$  us for CDMA.

Ixia chassis timing operates by resetting at a fixed time-of-day on all chassis from one source, and then maintaining the time accuracy through various different means. The following table describes the full set of options available and their approximate relative accuracies.

Summary of Timing Options

Available on Devices	Timing Option	Time of Day Accur- acy	Frequency Source	Frequency Accuracy
All Chassis	IRIG-B/GPS	150 nano- seconds from GMT	Ixia AFD2	Stratum 1
Ixia 100, 400T	Synchronous	N/A	Internal PC clock	1 micro- second/second
Ixia 100	CDMA in-built	100 micro- seconds from GMT	CDMA	Stratum 2

Available on Devices	Timing Option	Time of Day Accur- acy	Frequency Source	Frequency Accuracy
Ixia 100	GPS in-built	150 nano- seconds from GMT	GPS	Stratum 1

### Calculating Latency Accuracy for AFD2 (IRIG-B)

Use the following calculation for latency accuracy for AFD2 ( IRIG-B ) setups.

Latency A to B = Lab

Latency B to A = Lba

Transmit path A to B = T1

Transmit path B to A = T2

Time at A = Ta

Time at B = Tb

Time Absolute = T

Time Error at any site = Terr

Lab=Ta+T1-Tb

Lba=Tb+T2-Ta

Delta L = Lab Lba

Delta L = Ta + T1 - Tb (Tb + T2 - Ta)

Delta L = T1-T2+2(Ta-Tb)

Delta L = 2(Ta Tb)

If Ta = T+/-Terr and Tb = T+/-Terr

Then

Delta L= 2(T+/-Terr T+/-Terr)

Delta L= 2( |Terr|+|Terr|)

Delta L = 4Terr

### **Front Panel LEDs**

The AFD2 has the following front panel LEDs:

#### AFD2 LEDs

Label	Color	Description
USB	Green	Indicates that the connection is enabled, and glows solid with USB activity.
1PPS	Green	Indicates that the `1 Pulse Per Second' heartbeat is being gen-

Label	Color	Description
		erated by the IRIG-B hardware.
Pwr OK	Green	The AFD2 power has been validated.
Lock	Green	Indicates that the internal PLL has locked to the 1PPS signal. Testing is invalidated if the IRIG-B Lock signal is not illuminated.

# **IXIA AFD2 Specifications**

The IXIA AFD2 specifications are contained in the following table.

Ixia AF[	02 Specifications
General	
Physical	
Size	9.6"x7"x2.9" ( with feet, 2.70" without feet)
Weight	3.15 lb
Avg. Shipping Wt.	6 lbs
Shipping Vibra- tion	FED-STD-101C, Method 5019.1/5020.1
Environmental	
Temperature	
Operating	41°F to 122°F, (5°C to 50°C)
Storage	41°F to 122°F, (5°C to 50°C)
Power	Worst case power = 2.5W
	5V regulated source
Humidity	
Operating	0% to 85%, non-con- densing
Storage	0% to 85%, non-con- densing
IRIG-B Func- tionality	Bit rate is 100 pps and frame rate is 1fps for both code formats. 1pps pulse provides the precise time refrence.

DC level shift, pulse width coded with BCD, CF(control functions), SBS
1kHz carrier sine wave amplitude modulated with BCD, CF (control functions), SBS
12.5 Mhz GPS System clock
80 ns
Reset switch
USB, 1PPS, Pwr OK, Lock
Туре В
RJ14
BNC, IRIG-B code in
BNC, 1PPS pulse in
(not used) 2.0mm Power jack



# **Chapter 15 - Metronome**

This chapter provides details about Metronome, its specifications and features.

The Ixia Metronome Timing System is a precision test instrument enabling for large scale time synchronized testing within complex networks. Metronome solves the problem of sourcing time from external sources and translating that time into an IXIA proprietary time delivery interface. It recovers time from the actively selected external interface and time synchronizes the Metronome internal clock to the external source, distributes Metronome internal time downstream to IXIA endpoints, and generates aligned IXIA specific triggers to multiple downstream IXIA endpoints.

The following figures show the Metronome hardware:

**Figure: Metronome Front Panel** 



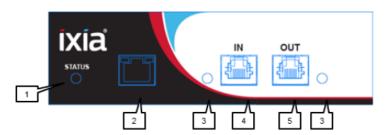
Figure: Metronome Rear Panel



### **Metronome Extender Chassis**

One Metronome Timing System EXTENDER (MTSx) is required for each MTS SyncOut Port that is in use (up to 8 per MTS chassis).

The following figure describes the Metronome Extender chassis:



- 1. MTSx unit status indicator.
- 2. **Sync In**:This port connects to a Metronome Sync Out port.
- 3. Port status indicator.
- 4. **IN**: This port connects to a XGS2-SD/HS or XGS12-SD/HS out port.
- 5. **OUT**: This port connects to a XGS2-SD/HS or XGS12-SD/HS in port.

#### **External Time Interfaces in Metronome**

Multiple types of external timing sources are accepted through Metronome, like GPS, Sync In (ToD+1PPS), BNC, and PTP (Phase 2).

### **Rear Panel LEDs**

A GPS status LED is present in the rear side of the Metronome chassis for the GPS interface.

Metronome GPS Status LEDs

Color	Description
Solid Green	Indicates that the satellites are acquired and valid time information is being received from the Ublox GPS receiver IC.
Blinking Green	Indicates that a GPS "lock" is being acquired.
Solid Red	Indicates that an antenna fault is detected.

# **Metronome Specifications**

The metronome specifications are contained in the following table.

Feature	Description
Metronome Timing System Part Number	942-0090
Metronome Timing System Extender Part Number	942-0091  Each timing link requires one MTSx adjacent to each chassis.
Chassis Supported	<ul><li> XGS12-SD</li><li> XGS12-HS</li><li> XGS2-SD</li><li> XGS2-HS</li></ul>
Dimensions	1U - 1.73x17.3x11
Operating Temperature	0° to 40° C
Storage temperature	-40°C to 70°C
Storage humidity	5 to 95% (RH), non-condensing
Input Voltage	100-240Vac
Input Frequency	47-63Hz
Max. Power Consumption	75W
Memory	1x 2GB @ 667MT/s, 64b data width (soDIMM)
Storage	1x 32GB microSD (boot code, application code, libraries)

Feature	Description	
Power	Worst case power = 2.5W	
Cable Lengths Supported – MTSx to MTS	MTS to MTS Extender Distance - 5m / 50m /100m	
	Cable Type - Metronome Sync Cable	
	Product Number - 942-0096, 942-0097, 942-0098	
	Ixia sells the cables listed above but you may construct cables of any length up to 200m.	
	Chassis to MTS Extender Distance - 6 feet	
Cable Lengths Supported – Chassis to MTSx	Cable Type - Ixia Chassis Sync Cable	
	Product Number - 942-0095	



# **Chapter 16 - IXIA Impairment Load Modules**

This chapter provides specification and details of Ethernet Impairment Modules (EIM). This family of load modules consist of the following cards:

- EIM1G4S 1G Ethernet LAN Impairment Module
- EIM10G4S 10G Ethernet LAN Impairment Module
- EIM40G2Q 40G Ethernet LAN Impairment Module

The Impairment load modules have a single-slot form factor and are inserted into a high-density XM2 or XM12 chassis to provide 2 to 12 modules per chassis configuration. The load modules offer 4x1GE, 4x10GE, or 2x40GE Ethernet interfaces that can emulate 64, 32, or 8 unidirectional network clouds respectively.

The high density 1GE, 10GE, and 40GE Impairment test modules are ideal for emulating real-life network impairments. The modules can emulate a WAN environment and simulate network characteristics, such as delay, delay variation, and impairments, such as packet loss, duplication, and re-ordering.

EIMs support the Impairment feature in IxNetwork and IxLoad applications that provides a quick and easy way to set up impairments, across multiple emulated WAN links. Using EIM ports, IxNetwork and IxLoad is capable of generating a number of impairments, for example packet drops, latency, or packet re-ordering, which replicates real-life WAN traversal conditions, whereby packet flows are impaired in different modes when traversing a network.

The EIM40G2Q load module is not supported in IxLoad.

For more information on the Impairment feature, refer to chapter on `Network Impairment' in the *IxNetwork Help* and *IxLoad Help*.

The key features of EIM are as follows:

- · High density 1GE, 10GE, and 40GE load modules
- · Realistic, high-scale WAN emulation
- Hardware-based impairment generation
- Integration with traffic generation, protocol emulation and analysis
- Scale port counts with high port density
- Simulate ultra-high latency: 500ms on each 40GE link, 600ms on each 10GE link and 6 sec. on each 1GE link at line rate traffic
- Leverage a single hardware chassis for traffic load modules
- Use IxNetwork for integrated traffic generation and impairment
- · Quickly configure traffic flows and apply impairment
- Automate tests
- Analyze measurements with StatViewer interface
- Achieve 1GE, 10GE and 40GE line-rate impairment on all frame sizes (64 to 9180 byte frames) with no packet loss

The 1/10GE EIM load module is shown in the following figure:

Figure: ImpairNet<sup>TM</sup> 1/10GE Load Module



The 40GE EIM load module is shown in the following figure:

Figure: ImpairNet<sup>TM</sup> 40GE Load Module



### **Part Numbers**

The part numbers are shown in the following table.

Part Numbers for Ethernet Impairment Load Module

Model Number	Part Number	Description
		ImpairNet EIM1G4S Gigabit Ethernet LAN Impairment module, 1-slot with 4-ports of SFP interfaces.
EIM1G4S	944-1081	For XM12-02 (P/N 941-0009) High Performance and XM2-02 (P/N 941-0003) portable chassis, SFP transceivers are required. Options for transceivers include SFP-LX, SFP-SX, and SFP-CU (for RJ45 copper support).
		ImpairNet EIM10G4S 10 Gigabit Ethernet LAN Impairment module, 1-slot with 4-ports of SFP+ interfaces.
EIM10G4S	944-1082	For XM12-02 (P/N 941-0009) High Performance and XM2-02 (P/N 941-0003) portable chassis, SFP+ transceivers are required. Options for transceivers include 10GBASE-SR/SW (948-0013), or 10GBASE-LR/LW (948-0014).
		ImpairNet EIM40G2Q 40 Gigabit Ethernet LAN Impairment module, 1-slot with 2-ports of QSFP+ interfaces.
EIM40G2Q 944-1083	For XM12-02 (P/N 941-0009) High Performance and XM2-02 (P/N 941-0003) portable chassis QSFP+ 40GBASE-SR4 transceivers (P/N 948-0028) is required.	

# **Specifications**

The load module specifications are described in the following table:

Ethernet Impairment Load Module 1/10GE Specifications

Ethernet Impairment Load Module 1/10GE Specifications		
Feature	Specification	
Number of ports per mod- ule	4-ports	
Number of chassis slots per module	1	
	The EIM load modules are supported on the following XM2 chassis:	
	941-0003-01 Rev. G and later version	
	941-0003-02 Rev. C and later version	
Chassis support	• 941-0003-03 Rev. F and later version	
Chassis support	<ul> <li>941-0003-04 Rev. G and later version</li> </ul>	
	• 941-0003-05 Rev. G or later version	
	<ul> <li>941-0003-06 Rev. A or later version</li> </ul>	
	Earlier models of XM2 chassis require factory upgrade for compatibility with EIM load modules.	
Module support	Up to 12 modules per XM12 Chassis	
	Up to 2 modules per XM2 Chassis	
SFP+ transceiver sup- port	Available with 1GE SFP, Electrical SFP RJ45 1GE Transceiver, and 10GE SFP+ Ethernet interface options	
Traffic Selection and	<ul> <li>16 traffic classifiers per link, total of 64 unidirectional classifiers per module for granular traffic classification</li> <li>16 impairment profiles per link, total of 64 profiles per module for granular service class emulation</li> <li>Emulate 32 unidirectional or 16 bidirectional network clouds per port pair</li> <li>Emulate 64 unidirectional or 32 bidirectional network clouds per module</li> <li>Easy-to-use, packet-analyzer-based selection interface</li> </ul>	
Impairment Configuration	<ul> <li>Traffic classifier support for numerous protocols and applications like bridging, routing, carrier Ethernet, broadband, MPLS, IPv6, and miscellaneous application-layer protocols</li> <li>Multiple service/traffic class emulation through independent and unique impairments per profile</li> <li>Emulate network cloud aggregation using mask and match support for packet classifiers</li> <li>Support for 8x16 bit frame matchers for each traffic classifier</li> </ul>	
Supported Impairments	Delay up to 600ms at 10GE, and up to 1.2s per module by cascading ports	

Feature	Specification	
	<ul> <li>Delay up to 6s at 1GE, and up to 12s per module by cas- cading ports</li> </ul>	
	<ul> <li>Packet Delay Variation using a selection of probability distributions</li> </ul>	
	<ul> <li>Delay resolution of 1µs</li> </ul>	
	<ul> <li>Emulate SLA validation by using normal/Gaussian, exponential, uniform, and custom probability distribution for delay variations</li> </ul>	
	<ul> <li>Packet drop at rates of up to 100% in clusters up to 65535 packets</li> </ul>	
	<ul> <li>Reorder packets at rates of up to 50% in clusters up to 255 packets</li> </ul>	
	<ul> <li>Packet duplication at a rate up to 100% in clusters up to 65535 packets by creating up to 31 copies of each packet</li> </ul>	
	<ul> <li>Emulation of network/transmission/processing error conditions through bit error insertion for L2-L7 protocols</li> </ul>	
	WAN forwarding error emulation	
	Ethernet FCS correction	
	<ul> <li>Emulation of DS3, OC3, DS1, DS0, E1, E3, and cable modem link speeds using rate limiting</li> </ul>	
Multi-core processor technology	Yes	
Operating temperature range	41°F to 86°F (5°C to 30°C), ambient air	
Minimoune Delay	• 1G: 300us	
Minimum Delay	• 10G: 30us	

### EIM Load Module 40GE Specification

Feature	Specification	
Interface Options	QSFP+	
Ports/Module	1 port pair per module	
Module/Chassis	<ul><li>1 module per XM2 chassis</li><li>Up to 6 modules per XM12 chassis</li></ul>	
Traffic Selection and	16 traffic classifiers per up/down link, total of 32 uni- directional classifiers per module for granular traffic classification	
Impairment Configuration	<ul> <li>4 impairment profiles per link, total of 8 profiles per mod- ule for granular service class emulation</li> </ul>	
	Emulates 32 unidirectional or 16 bidirectional network clouds per port pair	

Feature	Specification		
	Emulate 64 unidirectional or 32 bidirectional network clouds per module		
	Easy to use packet analyzer based selection interface		
	<ul> <li>Traffic classifier support for numerous protocols and applications like bridging, Routing, Carrier Ethernet, Broadband, MPLS, IPv6, and miscellaneous application- layer protocols</li> </ul>		
	<ul> <li>Multiple service/traffic class emulation through independent and unique impairments per profile</li> </ul>		
	<ul> <li>Emulate network cloud aggregation using mask and match support for packet classifiers</li> </ul>		
	Real-time preview of classifier match on live traffic		
	<ul> <li>Support for 8x16 bit frame matchers for each traffic classifier</li> </ul>		
	Delay up to 500ms at 40GE, and up to 1s per module by cascading ports		
	<ul> <li>Delay resolution of 1µs</li> </ul>		
	<ul> <li>Emulate SLA validation by using normal/Gaussian, exponential, uniform, and custom probability distribution for delay variations</li> </ul>		
	<ul> <li>Packet drop at rates of up to 100% in clusters up to 65535 packets</li> </ul>		
Supported Impairments	<ul> <li>Reorder packets at rates of up to 50% in clusters up to 255 packets</li> </ul>		
	<ul> <li>Packet duplication at a rate up to 100% in clusters up to 65535 packets by creating up to 31 copies of each packet</li> <li>WAN forwarding error emulation</li> </ul>		
	Ethernet FCS correction		
	<ul> <li>Emulation of DS3, OC3, DS1, DS0, E1, E3, and cable modem link speeds using rate limiting.</li> </ul>		



# Chapter 17 - IXIA Xcellon-Lava Load Modules

This chapter provides specification and feature details of the Xcellon-Lava 40/100 Gigabit Ethernet load modules. This family of load modules consist of the following 3-port cards:

- LavaAP40/100GE 2P
- LavaAP40/100GE 2RP
- LavaAP40/100GE 2P-NG

The Xcellon-Lava 40/100-Gigabit Ethernet load modules belong to the family of Ixia's High Speed Ethernet (HSE) products. These load modules combine the advantages of the Xcellon architecture and provide the highest 40GE and 100GE port densities. Lava load modules can be used for testing layer 1 to layer 7 applications. They are supported by Ixia's test applications, including IxNetwork and IxLoad.

Xcellon-Lava load modules are used for testing high-density data center 40 Gigabit Ethernet (40GbE) and 100 Gigabit Ethernet (100GbE) network equipments. 40GbE and 100GbE are high-speed computer network standards developed by the IEEE 802.3ba. Lava load modules extends the 802.3 protocol to operating speeds of 40 Gbps and 100 Gbps in order to provide greater bandwidth while maintaining maximum compatibility with the installed base of 802.3 interfaces.

Xcellon-Lava load modules are compatible with Ixia's XG12<sup>™</sup>, XM12, and XM2 chassis, and a broad range of Ethernet interfaces, allowing real-world, layer 1 to layer 7 test and measurement in a single chassis.

LavaAP40/100GE 2P-NG load module has capabilities similar to LavaAP40/100GE 2P and includes N2X support.

The Xcellon-Lava load module is shown in the following figure:





### **LED function table**

The LED functions are described in the following tables.

Xcellon-Lava LED Ports

LED Label	Usage
Link	Green if Ethernet link is up (established) or the port is in a forced Link Up state, OFF (no color) if link is down. Link may be down due to no signal or no PCS lock.
Tx Active	Green indicates that Tx is active and frames being sent; red indicates Tx is paused; off indicates Tx is not active.
Rx Active	Green indicates that Rx is active and frames being received; red indicates Rx is paused; off indicates Rx is not active.
Rx/Error	Green indicates valid Rx frames are being received; red indicates error frames being received; off indicates no frames being received.
Pwr Good	Green when power is on, red if power fault occurs.

# **CFP adapter diagrams**

CFP adapter diagrams are as follows:

The CFP-to-QSFP+ Interface adapter module is shown in the following figure:

Figure: CFP-to-QSFP+ Interface adapter

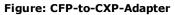


The CFP-to-QSFP+ Dual-Port Interface adapter module is shown in the following figure:

Figure: CFP-to-QSFP+ Dual-Port Interface adapter



The CFP to CXP-Adapter is shown in the following figure:





CFP-to-QSFP28 Interface Adapter is shown in the following figure:

Figure: CFP-to-QSFP28 Interface Adapter



### **Part Numbers**

The part numbers are shown in the following table.

Part Numbers for Xcellon-Lava Load Module and Supported Adapters

Adapters		
Model Number	Part Number	Description
Lava AP40/100GE 944-1067	This is the dual speed 40GE/100GE Ethernet Lava load module with Accelerated Performance. Each load module consists of 2-ports and 1-slot with CFP MSA interfaces. This load module supports full feature for layer 1 to layer 7 testing.	
2P		If XM12-01 (941-0002) chassis is used with this load module, the FRU-OPTIXIAXM12-01 (943-0005) power supply upgrade kit must be installed.
Lava AP40/100GE		This is the dual speed 40GE/100GE Ethernet Lava load module with data plane support only. It is an economic alternative to the Accelerated Performance load module, perfectly suitable for testing layer 1 to layer 3 applications that does not require routing protocol emulation. Each load module consists of 2-ports and 1-slot with CFP MSA interfaces.
2RP	If XM12-01 (941-0002) chassis is used with this load module, the FRU-OPTIXIAXM12-01 (943-0005) power supply upgrade kit must be installed.	
CFP-to- QSFP+ Interface Adapter Module	948-0022	A pluggable unit that converts an Ixia CFP MSA port interface to 1-port of the pluggable 40 GE QSFP+ for multimode fiber or copper cable assemblies or standalone transceivers. The adapter is compatible with the HSE40GETSP1-01, 40-Gigabit Ethernet load module (944-0069), HSE40/100GETSP1-01, 40/100-Gigabit Ethernet, dual-speed, load module (944-0091), HSE40/100GETSPR1-01, 40/100-Gigabit Ethernet, dual-speed, Data Plane Ethernet load module (944-0099), Xcellon-Lava 40/100-Gigabit Ethernet, Accelerated Performance, load module (944-1067) and Xcellon-Lava 40/100-Gigabit Ethernet, Reduced Performance load module (944-1068).
CFP-to- QSFP+ Dual-Port Interface Adapter Module	948-0023	A pluggable, 2-port unit that converts an Ixia Xcellon-Lava CFP MSA port interface to 2-ports of pluggable 40 GE QSFP+ for fiber or copper cable assemblies or standalone transceivers. The adapter is compatible with the Xcellon-Lava 40/100-Gigabit Ethernet, Accelerated Performance, load module (944-1067) and Xcellon-Lava 40/100-Gigabit Ethernet, Reduced Performance, load module (944-1068). Both load modules accept up to two of the Dual Interface Adapter Modules.
CFP-to-CXP Interface Adapter	948-0027	A pluggable unit that converts an Ixia CFP MSA port interface to 1-port of the pluggable 100 GE CXP for multimode fiber or

Model Number	Part Number	Description
Module		copper cable assemblies or standalone transceivers. The adapter is compatible with the HSE100GETSP1-01 100- Gigabit Ethernet load module (944-0070), HSE40/100GETSP1-01, 40/100-Gigabit Ethernet, dual-speed, load module (944-0091), HSE40/100GETSPR1-01, 40/100-Gigabit Ethernet, dual-speed, Data Plane load module (944-0099), Xcellon-Lava 40/100-Gigabit Ethernet, Accelerated Performance, load module (944-1067) and the Xcellon-Lava 40/100-Gigabit Ethernet, Reduced Performance load module (944-1068).
CFP-to- QSFP28 Interface Adapter Module	948-0029	CFP-to-QSFP28 Interface Adapter, 1P, 100GE, SFF-8665.  A pluggable unit that converts an Ixia CFP MSA port interface to 1-port of the pluggable 100 GE QSFP28 for multimode fiber or copper cable assemblies or standalone transceivers. The adapter is compatible with the HSE40GETSP1-01, 40-Gigabit Ethernet load module (944-0069), HSE40/100GETSPR1-01, 40/100-Gigabit Ethernet, dual-speed, Data Plane Ethernet load module (944-0099), Xcellon-Lava 40/100-Gigabit Ethernet, Accelerated Performance, load module (944-1067) and Xcellon-Lava 40/100-Gigabit Ethernet, Reduced Performance load module (944-1068).

# **CFP Adapter usage for Xcellon-Lava Ethernet Load Modules**

The CFP Slot #1 specification

Adapter Present	CFP Mode	Speed	Port(s) Avail- able
948-0027	Single	100G/40G	Port 1
948-0027	Dual	40G	Not Supported
948-0022	Single	40G	Port #1
946-0022	Dual	40G	Port #3
948-0023	Single	40G	Top port: Unavailable Bottom port: Port #1
	Dual	40G	Top port: Port #4  Bottom port: Port #3
948-0029	Single	100G	Port 1

The CFP Slot #2 specification

Adapter Present	CFP Mode	Speed	Port(s) Avail- able
948-0027	Single	100G/40G	Port 2
946-0027	Dual	40G	Not Supported
948-0022	Single	40G	Port #2
946-0022	Dual	40G	Port #5
948-0023	Single	40G	Top port: Unavail- able Bottom port: Port #2
	Dual	40G	Top port: Port #6  Bottom port: Port #5
948-0029	Single	100G	Port 1

#### **CFP Mode**

The CFP mode can be of two types:

- **Single Port Operation**: CFP provides one port of 40G or 100G. Speed is selected in a Port Property.
- **Dual Port Operation**: CFP provides two ports of 40G, when using CFP-to-QSFP+ Dual-Port Interface Adapter.

Dual Port Operations has following limitations:

- · BERT functionality not available
- Capture buffer is half the capacity of Single Port Operation.
- Max Streams supported = 256
- "No CRC" option not supported
- Value List memory is half that of Single Port Operation
- TX Flow sequence memory is half that of Single Port Operation
- Sequence Checking memory is half that of Single Port Operation
- PPM adjustment is per CFP (pair of QSFP+ ports)
- · DCE support not available at this time
- · Front panel LEDs not functional

# **Specifications**

The load module specifications are described in the following table:

Xcellon-Lava Ethernet Load Module Specifications

Aceiron-Lava	Ethernet Load Module S	pecifications
Feature	LavaAP40/100GE 2P	LavaAP40/100GE 2RP
Load Modules	LavaAP40/100GE 2P	LavaAP40/100GE 2RP
	2-100GE CFP MSA	2-100GE CFP MSA
Number of ports per mod- ule	2-40GE CFP MSA or (4) 40GE QSFP+ [with interface adapter]	2-40GE CFP MSA or (4) 40GE QSFP+ [with interface adapter]
Number of chassis slots per module	1	1
	XG12™	XG12™
Chassis Support	XM12	XM12
	XM2	XM2
	XG12™: (24) 100GE CFP MSA and (48)	XG12™: (24) 100GE CFP MSA and (48)
	40GE QSFP+	40GE QSFP+
Maximum ports per chassis	XM12: (20) 100GE CFP MSA and (40) 40GE QSFP+	XM12: (20) 100GE CFP MSA and (40) 40GE QSFP+
	XM2: (2) 100GE CFP MSA and (4)	XM2: (2) 100GE CFP MSA and (4)
	40GE QSFP+	40GE QSFP+
Capture buffer size	1.4 GB	1.4 GB
	256.	
Streams per port	stream (interleaved ition can generate r	sequential) or advanced d) mode, each stream definmillions of unique traffic Center mode, the number of 256.
Latency	Standard resolution in packet timestamp is 20ns. User selectable high resolution in packet timestamp is 2.5ns	No
Transceiver support	<ul> <li>CFP MSA 1.4, pluggable</li> <li>SFF-8436 QSFP+, pluggable fiber/copper cables (passive/active) with adapter</li> </ul>	
CFP interface adapters	<ul> <li>1-port, CFP-to-QSFP+ for 40GE</li> <li>2-port, CFP-to-QSFP+ for 40GE</li> <li>1-port CFP-to-CXP for 100GE operation</li> </ul>	

Feature	LavaAP40/100GE 2P	LavaAP40/100GE 2RP	
Hardware capture buffer per port	1.4 GB		
Interface protocols	40-Gigabit Ethernet 40GBASE-100GBASE-R as per IEEE802.3	-	
	The following protocols are supported in LavaAP40/100GE 2P Full Performance load module:		
	MPLS: RSVP-TE, RSVP-TE P2MP, LDP, PWE, L3 MPLS VPN, 6VP, MPLSTP		
	• Routing: RIP, RIPng, OS EIGRPv6, BGP-4,BGP+	PFv2/v3, ISISv4/v6, EIGRP,	
	port, VPLS-LDP, VPLS-BG		
Laver 3/2 routing protocol	• IP Multicast: IGMPv1/v SM/SSM, PIM-BSR, Multic	cast VPN, VPNv6	
Layer 2/3 routing protocol emulation		STP, PVST+/RPVST+, LACP	
emulation	• Carrier Ethernet: Link OAM, CFM, Service OAM, PBT/PBB-TE, SyncE, IEEE 1588v2 PTP		
	• High-Availability: BFD		
	The following Host/Client protocols are supported in LavaAP40/100GE2 RP Full Performance load module:		
	• ARP		
	• NDP		
	ICMP (PING)     IPv4		
	• IPv6		
Layer 4-7 application traffic testing	This is suppoted only in LavaAP40/100GE 2P Accelerated Performance load module.		
Transmit flows per port	Billions	Billions	
(sequential values)	DITIONS	DITIONS	
Transmit flows per port	1 million	1 million	
Trackable receive flows per port	1 million	1 million	
	512K		
Table UDF entries	Comprehensive packet editing function for emulating large numbers of sophisticated flows is supported by Xcellon-Lava load module. Entries of up to 256 bytes, using lists of values can be specified and placed at designated offsets within		

Feature	LavaAP40/100GE 2P LavaAP40/100GE 2RP	
	a stream. Each list consists of an offset, a size and a list of values in a table format.	
Packet flow statistics	Xcellon-Lava load module tracks over 1 million flows.	
Transmit engine	The Xcellon-Lava load module supports wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures.	
Receive engine	The Xcellon-Lava load module supports wire-speed packet filtering, capturing, realtime latency and inter-arrival time for each packet group, data Integrity, and sequence checking.	
User Defined Field (UDF) Features	The Xcellon-Lava load module supports the UDF features of fixed, increment or decrement by user-defined step, value list, cascade, random, and chained.	
Filters	The Xcellon-Lava load module uses 48-bit source/destination address, 2x128-bit userdefinable pattern and offset, frame length range, CRC error, data integrity error, sequence checking error (small, big, reverse)	
Error Generation	CRC (good/bad/none), undersize, oversize	
Transmit Line Clock Adjust- ment	Xcellon-Lava load module has the ability to adjust the parts per million (ppm) line frequency over a range of - 100 ppm to +100 ppm.	
	Standard resolution in packet timestamp is 20ns.	
Latency measurements	User selectable high resolution in packet timestamp is 2.5ns	
	The Xcellon-Lava load module supports the following BERT features on both 40 GE and 100 GE speeds:	
Layer 1 BERT capability	<ul> <li>User selected PRBS pattern for each PCS Lane</li> <li>User can select from a wide range of PRBS data patterns to be transmitted with the ability to invert the patterns</li> <li>Send single, continuous, and exponentially controlled amounts of error injection</li> <li>Wide range of statistics, including Pattern Lock, Pattern Transmitted, Pattern Received, Total Number of Bits Sent and Received, Total Number of Errors Sent and Received, Bit Error Ratio (BER), and Number of Mismatched 1's and 0's.</li> <li>Lane Stats Grouping per lambda for SMF and MMF 40GE and 100GE based on IEEE 802.3ba defined physical medium dependent (PMD).</li> </ul>	

Feature	LavaAP40/100GE 2P LavaAP40/100GE 2RP	
40/100 GE Physical Coding Sublayer (PCS) test fea- tures	The Xcellon-Lava load module supports IEEE 802.3ba compliant PCS transmit and receive side test capabilities. The supported PCS features are as follows:	
	<ul> <li>Per PCS lane, transmit lane mapping: Supports all combination of PCS lane mapping: Default, Increment, Decrement, Random, and Custom.</li> <li>Per PCS lane, skew insertion capability: User selectable from zero up to 3 microseconds of PCS Lane skew insertion on the transmit side.</li> <li>Per PCS lane, lane marker, or lane marker and payload error injections: User selectable ability to inject errors into the PCS Lane Marker and simultaneously into PCS Lane Marker and Payload fields. This includes the ability to inject sync bit errors into the Lane Marker and Payload. User can control the PCS lane, number or errors, period count and manage the repetition of the injected errors.</li> </ul>	
	• Per PCS lane, receive lanes statistics: PCS Sync Header and Lane Marker Lock, Lane Marker mapping, Relative lane deskew up to 52 microseconds for 40GE and 104 microseconds for 100GE, Sync Header and PCS Lane Marker Error counters, indicators for Loss of Synch Header and Lane Marker, and BIP8 errors.	
IPv4, IPv6, UDP, TCP check- sum	Xcellon-Lava load module supports hardware checksum generation and verification.	
Frame length controls	Xcellon-Lava load module supports fixed, random, weighted random, or increment by user-defined step, random, and weighted random.	
Preamble view	Xcellon-Lava load module allows to select to view and edit the preamble contents.	
Link Fault Signaling	Xcellon-Lava load module generates local and remote faults with controls for the number of faults and order of faults, plus the ability to select the option to have the transmit port ignore link faults from a remote link partner.	
	41°F to 95°F (5°C to 35°C), ambient air	
Operating temperature range	When an Xcellon-Lava load module is installed in an XM12, XM2, or XG12 chassis, the maximum operating temperature of the chassis is 35°C (ambient air).	
Load module dimensions	16.0" (L) x 12.0" (W) x 1.3" (H) 406mm (L) x 305mm (W) x 33mm (H)	

Feature	LavaAP40/100GE 2P	LavaAP40/100GE 2RP	
Woight	Module only: 9.8 lbs (4.45 kg)		
Weight	Shipping: 12.0 lbs (5.45 kg)		
ppm Adjust range	+/-100ppm	+/-100ppm	
ppm Adjust port/card	Card	Card	
Trigger out	No	No	
External Clock In(Frequence)	No	No	
External Clock Out	No	No	
Ambient Operating Temperature Range (C)	5-40	5-40	
Timestamp - Resolution	20ns	20ns	
Timestamp - High Res- olution	No	No	
Timestamp - End of Frame Instrumentation	No	No	
Timestamp - Floating Intrumentation	No	No	
IEEE802.3x Flow control	No	No	
WAN	No	No	
Streams per port	16	16	
Number of streams in Advanced Scheduler Mode (Data Center Mode)	16	16	
Transicevier Intrinsic Latency Calibration	No	No	
Intrinsic Latency	Yes	Yes	
Data Integrity	Yes	Yes	
Auto Instrumentation	Yes	Yes	
Preamble - Changeable Content	No	No	
Preamble - Byte Count Mode	No	No	
Preamble - SFD Detect Mode	Yes	Yes	

Feature	LavaAP40/100GE 2P	LavaAP40/100GE 2RP
Preamble - Cisco CDL Mode	No	No

The Ixia application support for Lava AP40/100GE 2P and Lava AP40/100GE 2RP is provided in the following table:

Xcellon-Lava Application Support

Lava AP40/100GE 2P	Lava AP40/100GE 2RP
IxExplorer	IxExplorer
IxNetwork	IxNetwork
IxAutomate	IxAutomate
TCL API	TCL API

# Updated enumerated types in API for LavaAP support in IxN2X

### AgtPortSelector ModuleType

- AGT\_CARD\_TWOPORT\_100GBASE\_R
- AGT\_CARD\_TWOPORT\_40GBASE\_R

#### **AgtPortSelector Personality**

Please note that the port speed is selected by the personality

- AGT\_PERSONALITY\_100GBASE\_R
- AGT\_PERSONALITY\_40GBASE\_R

### AgtEthernetLinkMode

- AGT\_ETHERNET\_LINK\_40G\_FULLDUPLEX,
- AGT\_ETHERNET\_LINK\_100G\_FULLDUPLEX

### **EAgtPluginMediaType**

- AGT\_PLUGIN\_CXP
- AGT\_PLUGIN\_QSFP
- AGT\_PLUGIN\_CFP

#### **EAgtPcsStatus**

- AGT\_PCS\_STATUS\_SYNC\_ERROR
- AGT\_PCS\_STATUS\_ILLEGAL\_CODE
- AGT\_PCS\_STATUS\_ILLEGAL\_IDLE

- AGT\_PCS\_STATUS\_EXTENDED\_ERROR\_MASK
- AGT\_PCS\_STATUS\_ALL\_ERROR\_MASK

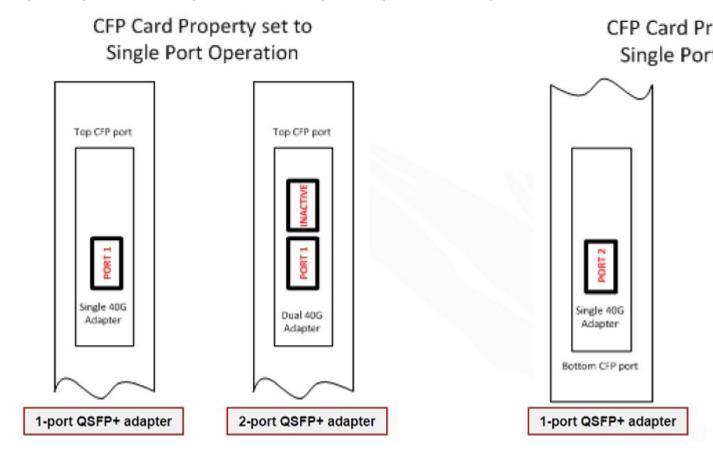
NOTE

The Xcellon-Lava AP is a CFP module. CFP-to-CXP and CFP-to-QSFP adaptors are available separately.

## 2x40 QSFP adaptor

N2X only supports single port mode, even with the dual-port adaptors. In a vertical orientation, it is the bottom port in each adaptor that is supported by N2X and the upper port is inactive.

Figure: Single Port Mode: Single and Dual CFP-to-QSFP+ adapter module configurations





# **Chapter 18 - IXIA Power over Ethernet Load Modules**

This chapter provides details about Power over Ethernet (PoE) Load Modules specifications and features.

Ixia's Power over Ethernet (PoE) Load Modules are used to test Power Sourcing Equipment (PSE) in accordance with IEEE Std 802.3af. The PoE Load Modules emulate Powered Devices (PDs) with programmable characteristics, and include data acquisition circuits for measuring voltage, current, and time.

The PoE Load Modules are intended to be used in conjunction with Ixia's line of Ethernet traffic generator/analyzer load modules. The PoE Load Modules handle the detection, classification, and power loading aspects of 802.3af, while passively conveying Ethernet data between the PSE and the traffic generator/analyzer load modules.

Ixia offers two models of PoE Load Modules. The basic model (PLM1000T4-PD) is rated for 20 Watts continuous power dissipation per port. The advanced module (LSM1000POE4-02) is rated for 30 Watts per port, and has several additional advanced features, including configurable ZAC2 settings. Both models include 4 independent and isolated PD emulators on a single-slot load module.

Figure: PLM1000T4-PD Load Module

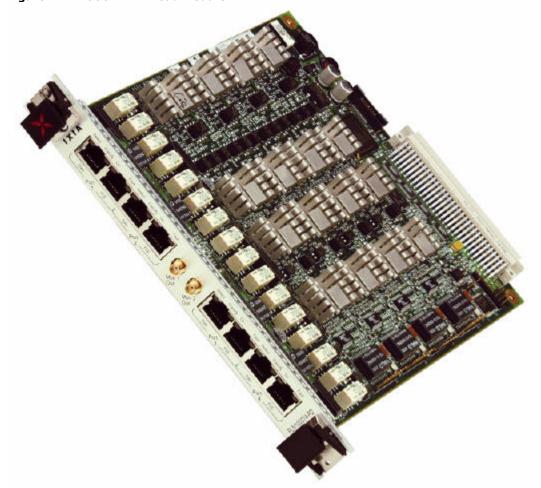


Figure: PLM1000T4-PD Load Module Face Plate



### **Part Numbers**

The part numbers are shown in the following table. Items without a *Price List Name* entry are no longer available.

Part Numbers for Gigabit Modules

Load Mod- ule	Price List Name	Description
PLM1000T4-PD	PLM1000T4-PD	4-port PoE Load Module, 20W/Port, emulating Powered Devices.
LSM1000POE4- 02	LSM1000POE4- 02	4-port PoE Load Module, 30W/Port, emulating Powered Devices.

# **Specifications**

The load module specifications are contained in the following table. The limitations of -3, Layer 2/3, and Layer 7 cards are discussed in <a href="Ixia Load Modules">Ixia Load Modules</a>.

PoE Load Module Specifications

	PLM1000T4-PD	LSM1000P0E4-02
# ports	4	4
Data Rate	10/100/1000 Base-T	10/100/1000 Base-T
Connector	RJ-45	RJ-45
R_SIG Range/Resolution	2 45k/200 Ohms	2 45k/200 Ohms
C_SIG Range/Resolution	0 220nF/10nf	0 220nF/10nf
I_CLASS Range	60mA	0 60mA
I_CLASS Res- olution/Accuracy	0.25mA	0.25mA
DC MPS Range/Resolution	0 60mA/0.25mA	0 60mA/0.25mA
AC MPS R_PD Range/Resolution	Zac1: 10 45k/200 Ohm- sZac2: Fixed/ > 4 Ohms	Zac1: 10 45k/200 Ohm- sZac2: 200 1200k/ 8k
AC MPS C_PD Range/Resolution	0 220nF/10nF	0 220nF/10nF
Data Acquisition Sample Rate	5MSPS	5MSPS
Data Acquisition Voltage	0 64V/10 bits/0.5%	0 64V/10 bits/0.5%

	PLM1000T4-PD	LSM1000POE4-02
Range/Resolution/Accuracy		
Data Acquisition Current Range/Resolution/Accuracy	0 1024mA/10 bits/0.5%	0 1024mA/10 bits/ 0.5%
Data Acquisition Power Readback Accuracy	100mW	100mW
Maximum Continuous Power	20W per port	30W per port
Load Modes	Constant Current (CC)Power (CP)	Constant Current (CC)Power (CP)
Pulse Modes (CC only)	Single, Continuous, Inrush	Single, Continuous, Inrush
Programmable Pulse Para- meters	Amplitude, Width, Duty, Slew Rate	Amplitude, Width, Duty, Slew Rate

### **Port LEDs**

Each port incorporates a set of LEDs, as described in the following table.

PoE Load Module Port LEDs

LED Label	Usage
Detect	When green, indicates the PSE is in the detection process.
Classify	When green, indicates the PSE is in the classification process.
Powered	When green, indicates the PSE is powering the emulated PD.
Fault	When red, indicates the PSE has performed an illegal operation. PoE disconnects under a fault condition until the PSE resets.

# **Test Monitor Output Ports**

There are two test monitor output ports on each PoE module, used to measure the power-/current into a selected port. These ports can be used in conjunction with an oscilloscope to view input characteristics. The ports have the following scale:

Test Monitor Ports

Factor	Measurement
DC Meas- urements	62.5mV out/Volts input
DC Current	4mV out/ mA Input
AC Meas- urement	.05V out/Volts Input (Planned Feature)

# **Statistics**

Statistics counters for PoE cards are available in <u>Description of Statistics</u>.

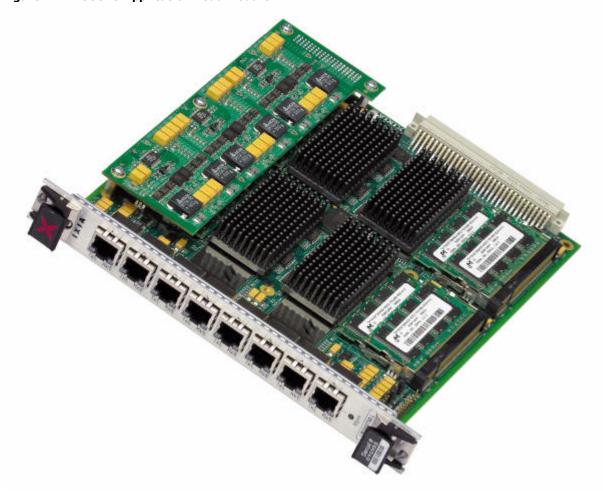
# Chapter 19 - IXIA 10/100/1000 Load Modules

This chapter provides details about Ixia 10/100/1000 family of load modules the specifications and features.

The 10/100/1000 family of load modules implements Ethernet interfaces that run at 10 Mbps, 100 Mbps, or Gigabit (1000 Mbps) speeds. Different numbers of ports and interfaces are available for the different board types. The specifications for these load modules are listed in the <u>table</u>. A representative selection of these load modules are pictured on the pages that follow.

The application load module ALM1000T8 is an 8-port 10/100/1000 Mbps Base T Ethernet copper module which supports the Real World Traffic Suite (includes IxVPN, IxChariot, and IxLoad). This module also supports ARP, PING, and independent Linux SDK applications. The ALM1000T8 load module is shown in the following figure.

Figure: ALM1000T8 Application Load Module



### **Part Numbers**

The part numbers are shown in the following table. Items without a *Price List Names* entry are no longer available.

Part Numbers for 10/100/1000 Modules

Part Numbers for 10/100/1000 Modules			
Load Module	Price List Names	Description	
		16-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule, reduced per- formance, 400MHz PowerPC Processor. 256MB of processor memory per port.	
LSM1000XMVR16-01	LSM1000XMVR16-01	In order to meet the emissions requirements of FCC part 15 Class A the RJ45 cables attached to this module's Ethernet ports must have ferrite beads (Fair-Rite 0431164281 or equivalent) present at both ends of the cable.	
LSM1000XMVR12-01	LSM1000XMVR12-01	12-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule, reduced per- formance, 400MHz PowerPC Processor. 256MB of processor memory per port.	
LSM1000XMVR8-01	LSM1000XMVR8-01	8-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule, reduced per- formance, 400MHz PowerPC Processor. 256MB of processor memory per port.	
LSM1000XMVR4-01	LSM1000XMVR4-01	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule, reduced per-	

Load Module	Price List Names	Description
		formance, 400MHz PowerPC Processor. 256MB of processor memory per port.
LSM1000XMSP12-01	LSM1000XMSP12-01	12-port Dual-PHY RJ45 10/100/1000 Mbps Gig- abit Ethernet and SFP fiber. A 750FL or 750GL PowerPC Processor with a minimum of 256MB per port of CPU memory and 256KB of layer 2 cache running at 600MHz.
LSM1000XMVDC4-01	LSM1000XMVDC4-01	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps. 1GB port CPU memory, full-featured L2-L7 with FCoE enabled; Fiber ports require SFP transceivers, options include SFP-LX, SFP-SX, and SFP-CU.
LSM1000XMVDC4-NG	LSM1000XMVDC4-NG	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps. 1GB port CPU memory, full-featured L2-L7 with FCoE enabled; Fiber ports require SFP transceivers, options include SFP-LX, SFP-SX, and SFP-CU.
LSM1000XMVDC8-01	LSM1000XMVDC8-01	8-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps. 1GB port CPU memory, full-featured L2-L7 with FCoE enabled; Fiber ports require SFP transceivers, options include SFP-LX, SFP-SX, and SFP-CU.
LSM1000XMVDC12-01	LSM1000XMVDC12-01	12-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps. 1GB port CPU memory, full-featured L2-L7 with FCoE enabled; Fiber ports require SFP

Load Module	Price List Names	Description
		transceivers, options include SFP-LX, SFP-SX, and SFP-CU.
LSM1000XMVDC16-01	LSM1000XMVDC16-01	16-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps. 1GB port CPU memory, full-featured L2-L7 with FCoE enabled; Fiber ports require SFP transceivers, options include SFP-LX, SFP-SX, and SFP-CU.
LSM10/100/1000XMVDC16NG	LSM10/100/1000XMVDC16NG  The Part Number of this load module is 944-1072-01.	16-port XMVDC16NG load module is Ixia's Fusion-enabled version of the existing LSM XMVDC16 load module. These two load modules are physically similar. The hardware components and application specifications remain unchanged. The key difference is the IxN2X capability to run the load module in IxN2X mode.
LM1000STXS2	LM1000STXS2	2-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load mod- ule. Does not include SFP transceivers.
LM1000STX2	LM1000STX2	2-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet Load Mod- ule. Supports Layer 2-3 stream generation only. No support for routing, Layer 4-7 applications and the Linux SDK. Does not include any SFP trans- ceivers.
LM1000STX4	LM1000STX4	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet Load Mod- ule. Supports Layer2-3

Load Module	Price List Names	Description
		stream generation only. No support for routing, Layer 4-7 applications and the Linux SDK. Does not include any SFP trans- ceivers.
ALM1000T8	ALM1000T8	8-port 10/100/1000 Mbps Base T Ethernet copper. Supports Real World Traffic Suite (includes
		IxVPN, IxChariot and IxLoad), and independent Linux-based SDK applications.
ELM1000ST2	ELM1000ST2	2-port Dual PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet Load Module featuring hardwarebased high-speed IPSec encryption for use with IxVPN.
	SFP-LX	1310 nm LX SFP transceiver used with LM1000STX2, LM1000STX4, LM1000STXS2, and LM1000STXS4-256.
	SFP-SX	850 nm SX SFP transceiver used with LM1000STX2, LM1000STX4, LM1000STXS2, LM1000STXS4-256, LSM1000XMV(R)4-01, LSM1000XMV(R)8-01, LSM1000XMV(R)12-01, and LSM1000XMV(R)16-01.
LSM1000XMVDC4-NG		4-port LSM1000XMVDC4NG- 01,GIGABIT ETHERNET LOAD MODULE

# **Specifications**

The load module specifications are contained in the following tables. The limitations of -3, Layer 2/3, and Layer 7 cards are discussed in the <a href="Ixia Load Modules">Ixia Load Modules</a>.

10/100/1000 Load Module Specifications Part 1

	ALM1000T8	ELM1000ST2
# ports	8	2
-3 Card Available	N	N
Layer2/Layer3 Card?	N	N
Data Rate	10/100/1000 Mbps	10/100/1000 Mbps
Connector	RJ-45 (copper)	RJ-45 (copper) andSFP (fiber)
Interfaces	1000Base-T100Base- TX10Base-T	1000Base-X1000Base- T100Base-TX10Base-T
Capture buffer size	N/A	N/A
Captured packet size	N/A	N/A
Streams per port	N/A	N/A
Advanced scheduler streams per port	N/A	N/A
Flows per port	N/A	N/A
Preamble size: min-max	N/A	N/A
Frame size: min-max	N/A	N/A
Inter-frame gap: min-max	N/A	N/A
Inter-burst gap: min-max	N/A	N/A
Inter-stream gap:min-max	N/A	N/A
Latency	N/A	N/A

<sup>2</sup>Odd frame sizes can cause diminishment in the actual data rate on this modules.

10/100/1000 Load Module Specifications Part 2

	LM1000STX2, LM1000STX40, LM1000STX24	LM1000STXS2, LM1000STXS4- 256, LSM1000XMSR12-01, LSM1000XMSP12-01, LSM1000XMV4/8/12/16-01, LSM1000XMVR4/8/12/16-01, LSM1000XMVDC4/8/12/16- 010, LM1000STXS24
# ports	2 (STX2)4 (STX4) 24 (STX24)	2 (STXS2)4 (STXS4) 4 (XMV(R)4)4

	LM1000STX2, LM1000STX40, LM1000STX24	LM1000STXS2, LM1000STXS4- 256, LSM1000XMSR12-01, LSM1000XMSP12-01, LSM1000XMV4/8/12/16-01, LSM1000XMVR4/8/12/16-01, LSM1000XMVDC4/8/12/16- 010, LM1000STXS24
		(XMVDC4)8 (XMV(R)8)8 (XMVDC8)12 (XMV(R)12)12 (XMS12/XMSR12)12 (XMSP12)12 (XMVDC12)16 (XMV16/XMVR16)16 (XMVDC16)16 (XMVDC16NG) 24 (STXS24)
-3 Card Available	N	N
Layer2/Layer3 Card?	Υ	Υ
Data Rate	10/100/1000 Mbps	10/100/1000 Mbps
Connector	Dual: RJ-45 (copper) and SFP (fiber)	Dual: RJ-45 (copper) and SFP (fiber) (1000 Mbps only)
Interfaces	1000Base-X1000Base- T100Base-TX10Base-T	1000Base-X1000Base-T100Base- TX10Base-T LSM1000XMV(R)4/8/12/16-01 and LSM1000XMVDC4/8/12/16-01 also have 100Base-FX
Ambient Oper- ating Tem- perature Range		LSM1000XMVR16-01 41°F to 86°F (5°C to 30°C)  NOTE  Using this load module in the XM2 or XM12 chassis lowers the chassis maximum operating temperature.
Capture buffer size	8MB	LSM1000XMV4/8/12/16-01 and LSM1000XMVDC4/8/12/16-01 32MB (Packet Group Engine Enabled) 64MB (Packet Group Engine Disabled) Others:8MB
Captured packet size	12-13k bytes	12-13k bytes
Number of stream in Packet Stream Mode	256	LSM1000XMV4/8/12/16-01 and LSM1000XMVDC4/8/12/16-01 4096

	LM1000STX2, LM1000STX40, LM1000STX24	LM1000STXS2, LM1000STXS4- 256, LSM1000XMSR12-01, LSM1000XMSP12-01, LSM1000XMV4/8/12/16-01, LSM1000XMVR4/8/12/16-01, LSM1000XMVDC4/8/12/16- 010, LM1000STXS24
		Others: 256
Number of streams in Advanced Sched- uler Mode (Non Data Center Mode)	LSM1000XMV4/8/12/16-01 and LSM1000XMVDC4/8/12/16-01  Fast: 16 Fast: 16 Slow: 240  All others: Fast: 16 Slow: 240	
Number of streams in Advanced Sched- uler Mode (Data Center Mode)	N	(For LSM1000XMVDC4/8/12/16-01 card) Fast: 16Medium: 240
Flows per port	N/A	N/A
Preamble size: min-max (bytes)	2-61 (10/100)8-61 (1000 fiber)6-61 (1000 copper)	2-61 (10/100)8-61 (1000 fiber)6-61 (1000 copper)
Frame size: min- max	12-13k bytes	12-13k bytes For XMVDC: Minimum Frame Size at Line Rate: 48 Minimum Frame Size - may not be at Line Rate: 12 Maximum Frame Size: 2500B
Inter-frame gap: min-max	Basic Scheduler:10: 6400ns-429s in 800ns steps100: 640ns-42.9s in 80ns steps1000: 64ns-4.29s in 16ns steps  Advanced Scheduler:10: 6400ns- 1717.99s in 800ns	Basic Scheduler:10: 6400ns-429s in 800ns steps100: 640ns-42.9s in 80ns steps1000: 64ns-4.29s in 16ns steps  Advanced Scheduler:10: 6400ns-1717.99s in 800ns steps100: 640ns-171.799s in 80ns steps1000: 64ns-68.719 in 16ns steps

	LM1000STX2, LM1000STX40, LM1000STX24	LM1000STXS2, LM1000STXS4- 256, LSM1000XMSR12-01, LSM1000XMSP12-01, LSM1000XMV4/8/12/16-01, LSM1000XMVR4/8/12/16-01, LSM1000XMVDC4/8/12/16- 010, LM1000STXS24
	steps100: 640ns- 171.799s in 80ns steps1000: 64ns-68.719 in 16ns steps	
	10: 6400ns-429s in 800ns steps100: 640ns- 42.9s in 80ns steps1000: 64ns- 16.7ms in 16ns steps	10: 6400ns-429s in 800ns steps100: 640ns-42.9s in 80ns steps1000: 64ns-16.7ms in 16ns steps
Inter-burst gap: min-max	Advanced Scheduler:	Advanced Scheduler:
IIIII IIIdx		10: 0.419s
	10: 0.419s	100: 0.0419s
	100: 0.0419s	1000: 0.0167s
	1000: 0.0167s	
Inter-stream gap:min-max	10: 6400ns-429s in 800ns steps100: 640ns- 42.9s in 80ns steps1000: 64ns-4.29s in 16ns steps	10: 6400ns-429s in 800ns steps100: 640ns-42.9s in 80ns steps1000: 64ns-4.29s in 16ns steps
Normal stream min frame rate	10: 0.00238fps100: 0.0238fps1000: 0.238fps	10: 0.00238fps100: 0.0238fps1000: 0.238fps
Advanced stream min frame rate	10: 0.000582fps100: 0.00582fps1000: 0.0146fps	10: 0.000582fps100: 0.00582fps1000: 0.0146fps
Latency	20ns resolution	20ns resolution
Table UDF fea- ture (based on minimum packet size 64K)	96K (full)32K (reduced)	786K (LSM1000XMV)96K others (full)32K others (reduced)
Max Value List Entries	48K	48K
Max Range List Entries 1	6K	6K

<sup>1</sup>192k memory is shared between value list entries (at 4 bytes per entry) and range list entries (at 32 bytes per entry).

#### **ALM1000T8**

The ALM100T8 has a feature that is non-conformant with the IEEE 802.3 specification. According to the specification, all 4 pairs of signals must be connected in gigabit copper mode for auto-negotiation to function. On the ALM100T8, if auto-negotiation fails using all 4 pairs, auto-negotiation is attempted using only the two pairs used in 10/100 modes. This allows auto-negotiation to succeed even if gigabit mode is enabled for auto-negotiation and a 10/100 only cable is used.

### **Card LEDs**

Each ELM1000ST2, LM1000STX2/4 and LM1000STXS2/4 card incorporates a single LED, as described in the following table.

10/100/1000 Card LEDs for ELM1000ST2, LM1000STX2/4 and LM1000STXS2/4

LED Label	Usage
Trig	The value of the `OR' function of all of the trigger out ports on the board. The LED's color is orange.

The ALM1000T8 has a card-level `mgmt' LED next to Port 8. This LED is not currently used.

### **Port LEDs**

Each port on the ALM1000T8 module incorporates a set of 2 LEDs, as described in the following table. The ALM1000T8 also has a card-level `mgmt' LED next to Port 8; this LED is not currently used.

ALM100T8 Port LEDs

LED Label	Usage
	Color is used to indicate the link speed:
Link/Tx (Upper LED)	<ul><li>1000Mbps Green</li><li>100Mbps Orange</li><li>10Mbps Yellow</li></ul>
	Flashing indicates transmit activity.
	Off if link is down.
Rx/Error (Lower LED)	<ul> <li>Three conditions apply:</li> <li>Full duplex or master (in 1000 Mbps case): Green with extended pulses off to indicate receive activity.</li> <li>Half duplex or subordinate (in 1000 Mbps case): Off with extended green pulses to indicate receive activity.</li> </ul>
	<ul><li>Error: Overrides the other two modes, with extended orange pulses.</li><li>No link: Off.</li></ul>

Port LEDs for LSM1000XMV4/8/12/16-01, are described in the following table.

Port LEDs for LSM1000XMV4/8/12/16-01

LED Label	Copper	Copper Fiber	
Link/Tx (Upper LED)	Color is used to indicate the link speed:  • 1000Mbps Green  • 100Mbps Orange  • 10Mbps Yellow  Flashing indicates transmit activity.  Off if link is down.	Green indicates link has been established and flashes during transmit activity.	
Rx/Error (Lower LED)	<ul> <li>Three conditions apply:</li> <li>Full duplex or master (in 1000 Mbps case): Green with extended pulses off to indicate receive activity.</li> <li>Half duplex or subordinate (in 1000 Mbps case): Off with extended pulses to indicate receive activity.</li> <li>Error: Overrides the other two modes and pulses red.</li> <li>No link: Off.</li> </ul>	Green indicates link has been established and flashes during receive activity.  Continuous red indicates a receive error.	

Each ELM1000ST2, LM1000STX2, LM1000STX4, LM1000STXS2, and LM1000STXS4-256 port incorporates a set of 6 LEDs, as described in the following table. The LEDs are arranged next to the two connectors associated with each port: Speed, Slave, and RJ45 Link/Tx/Coll are next to the RJ45 connector and Rx/Err, Half, and SFP Link/Tx/Coll are next to the SFP connector.

Port LEDs for ELM1000ST2, LM1000STX2, LM1000STX4, LM1000STXS2, LM1000STXS4, and LM1000STXS4-256

LED Label	Usage
Speed	<ul><li>Off for 10Mbps.</li><li>Orange for 100Mbps.</li><li>Green for 1000Mbps.</li></ul>
Slave	<ul><li>On in slave or subordinate mode.</li><li>Off otherwise.</li></ul>
RJ45 Link/Tx	<ul> <li>Off if SFP is the active connector.</li> <li>Steady Orange for no link.</li> <li>Flashing Orange for link with collision.</li> <li>Steady Green for link with no transmit.</li> </ul>

LED Label	Usage
	Flashing green during transmit.
Rx/Err	<ul><li>Flashes green on data receive.</li><li>Steady Red for error.</li></ul>
Half	<ul><li> Green for half-duplex mode.</li><li> Off for full-duplex mode.</li></ul>
SFP Link/Tx/Coll	<ul> <li>Off if RJ45 is the active connector.</li> <li>Steady Orange for no link.</li> <li>Flashing Orange for link with collision.</li> <li>Steady Green for link with no transmit.</li> <li>Flashing green during transmit.</li> </ul>

There is no trigger connector on the ALM100T8.

The ELM1000ST2's triggers are not currently used.

The signals available on the trigger out pins for the LM1000STX4, LM1000STXS4-256, LM1000STXS2, and LM1000STX2 cards is described in the following table.

LM1000STXS4, LM1000STX4, LM1000STXS4-256, LM1000STXS2, and LM1000STX2 Trigger Out Signals

Pin	Signal	
1	660ns negative pulse when User Defined Statistic 1 is true.	
2	660ns negative pulse when User Defined Statistic 1 is true.	
3	660ns negative pulse when User Defined Statistic 1 is true.	
4	660ns negative pulse when User Defined Statistic 1 is true.	
5	Ground	
6	Ground	

### **Statistics**

Statistics for 10/100/1000 cards, under various modes of operation may be found in <u>Available Statistics</u>.

# **Chapter 20 - IXIA Network Processor Load Modules**

This chapter provides details about Ixia's Xcellon-Ultra XP and Xcellon-Ultra NP load modules the specifications, features, and functionality. It also provides details on Xcellon-Ultra load module when it operates in IxN2X mode.

Ixia's Gigabit and 10 Gigabit Ethernet Network Processor load modules Xcellon-Ultra XP and Xcellon-Ultra NP. These are Ethernet modules with additional aggregation capability. Each features 12 ports of 10/100/1000Mbps Ethernet configurable in either aggregation mode, stream mode, or as 1 port of 10GE aggregation. The Xcellon-Ultra module can provide 144 GigE ports in the Optixia XM12 or 24 GigE ports in the Optixia XM2. The Xcellon-Ultra XP-01 module is shown in the figure below.

IxN2X capability is added to the regular Xcellon-Ultra load module to use it in IxN2X mode. Xcellon-Ultra XP and NP and Xcellon-Ultra NG load modules share similar physical properties. In addition to the physical properties, Xcellon-Ultra NG supports IxN2X mode.

The Xcellon-Ultra module offers complete Layer 2-7 network and application testing functionality in a single Optixia XM load module. The twelve Gig Ethernet ports may either be used individually or aggregated through a 10 Gigabit Ethernet port. This architecture allows the processing power and resources of up to twelve per-port CPUs to be combined into one physical port, providing the highest Layer 4-7 line-rate performance, unmatched in any other Layer 4-7 test solution. Each test port supports wire-speed Layer 2-3 traffic generation and analysis, high-performance routing/bridging protocol emulation, and true Layer 4-7 application traffic generation and subscriber emulation. Using 12 GbE ports per module, ultra-high density test environments can be created for auto-negotiable 10/100/1000 Mbps Ethernet over copper as well as fiber. With 12 slots per Optixia XM12 chassis, up to 144 Gigabit Ethernet and 12 10GbE test ports are available in a single test system.

# **Application Layer Performance Testing**

The Gigabit Ethernet Xcellon-Ultra module supports high performance testing of content-aware devices and networks through the Aptixia IxLoad application. IxLoad creates real-world traffic scenarios at the TCP/UDP (Layer 4) and Application (Layer 7) layers, emulating clients and servers for Web (HTTP, SSL), FTP, Email (SMTP, POP3, IMAP), Streaming (RTP, RTSP), Video (MPEG2, MPEG4, IGMP), Voice (SIP, MGCP), and services such as DNS, DHCP, LDAP and Telnet. Each GE XMV port can be independently configured to run different protocols and client/server scenarios.

# Real-time Transport Protocol (RTP) Feature

For the Xcellon-Ultra XP and NP modules, the RTP engine built into the FPGA can generate and terminate audio streams (video and data traffic is an option, too). The RTP engine works together with the VoIP Peer signaling protocols present in IxLoad. On a physical port the traffic is a mixture of signaling traffic generated and analyzed by PCPU, RTP traffic generated by CPCU, and RTP traffic generated by hardware.

The RTP feature is selectable from the Port Properties Operation Mode tab in IxExplorer. For details, see the *IxExplorer User Guide*, Chapter 18, topic *Port Properties for Xcellon-Ultra Modules*.

### **Modes of Operation**

The Xcellon-Ultra modules can operate in three different modes providing a flexible, scalable and powerful layer 4-7 performance.

### Non-Aggregated (Normal) Mode

In this mode, the twelve 10/100/1000Mbps ports provide L2-L7 XMV functionality. Each port is capable of providing high performance packet generation and application layer testing by employing its own port CPU resources as well as the dedicated hardware stream engine. In this mode the 10GE Aggregation Port is disabled.

### **Gigabit Aggregated Mode**

Gigabit Aggregated Mode allows the twelve PCPUs to be assigned to any of 12 GbE test ports through the switch fabric. Aggregation of the processing power allows application layer testing at line rate regardless of the test objective. A cluster of PCPU's can be assigned to any of the physical ports. Multiple clusters and their assigned physical ports can exist on the same module. Aptixia applications transparently configures the available PCPU resources and make the assignment to the physical port(s) to achieve the test objectives. This mode is exclusive to L4-7 testing and there is no support for hardware stream engine. In this mode the 10GE Aggregation Port is disabled.

### **10GE Aggregated Mode**

In 10GE Aggregated Mode, all of the twelve PCPUs are assigned to the 10GE Aggregation Port through the switch fabric. Aggregation of the processing power allows application layer testing at line rate (10 Gbps). Aptixia applications transparently configure the PCPU resources to achieve the test objectives. This mode is exclusive to L4-7 testing and there is no support for hardware stream engine. In this mode the twelve Gigabit ports are disabled.

### **Flexible Packet Generation**

Each Xcellon-Ultra test port is capable of generating precisely controlled network traffic at up to wire speed of the network interface using Ixia's IxExplorer test application. Up to millions of packet flows can be configured on each port with fully customizable packet header fields. Flexible header control is available for Ethernet, IPv4/v6, IPX, ARP, TCP, UDP, VLANs, QinQ, MPLS, GRE, and many others. Payload contents can also be customized with incrementing/decrementing, fixed, random, or user-defined information. Frame sizes can be fixed, varied according to a pattern, or randomly assigned across a weighted range. Rate control can be flexibly defined in frames per second, bits per second, percentage of line rate, or inter-packet gap time.

# **Real-Time Latency**

Packets representing different traffic profiles can be associated with Packet Group Identifiers (PGIDs). The receiving port measures the minimum, maximum, and average latency in real time for each packet belonging to different groups. Measurable latencies include:

- Instantaneous latency and inter-arrival time where each packet is associated with one group ID
- Latency bins, where PGIDs can be associated with a latency range
- Latency over time, where multiple PGIDs can be placed in `time buckets' with fixed durations
- First and last time stamps, where each PGID can store the timestamps of first and last received packets

#### **Transmit Scheduler**

There are two modes of transmission are available - Packet Stream and Advanced Stream Scheduler:

#### **Packet Stream Scheduler**

In Packet Stream Scheduler mode, the transmit engine allows configuration of up to 4096 unique sequential stream groupings on each port. Multiple streams can be defined in sequence, each containing multiple packet flows defined by unique characteristics. After transmission of all packets in the first stream, control is passed to the next defined stream in the sequence. After reaching the last stream in the sequence, transmission may either cease, or control may be passed on to any other stream in the sequence. Therefore, multiple streams are cycled through, representing different traffic profiles to simulate real network traffic.

#### **Advanced Stream Scheduler**

In Advanced Stream Scheduler mode, the transmission of stream groupings is interleaved per port. For example, assume a port is configured with three streams. If Stream 1 is defined with IP packets at 20% of line rate, Stream 2 is defined with TCP packets at 50% of line rate, and Stream 3 is defined with MPLS packets at 30% of line rate, data on the port is transmitted at an aggregate utilization of 100% with interleaved IP, TCP, and MPLS packets.

#### **Extensive Statistics**

- · Real-time 64-bit frame counts and rates
- Spreadsheet presentation format for convenient manipulation of statistics counters
- Eight Quality of Service counters (supporting 802.1p, DSCP, and IPv4 TOS measurements)
- Six user-defined statistics that use a trigger condition
- · Extended statistics for ARP, ICMP, and DHCP
- Transmit stream statistics for frame counts and rate
- External logging to file for statistics and alerts
- Audible and visual alerts with user-definable thresholds

# **Data Capture**

Each port is equipped with 64 MB of capture memory, capable of storing tens of thousands of packets in real time. The capture buffer can be configured to store packets based on

user-defined trigger and filter conditions. Decodes for IPv4, IPv6, UDP, ARP, BGP-4, IS-IS, OSPF, TCP, DHCP, IPX, RIP, IGMP, CISCO ISL, VLAN, and MPLS are provided.

### **Data Integrity**

As packets traverse through networks, IP header contents may change, resulting in the recalculation of packet CRC values. To validate device performance, the data integrity function of Gigabit Ethernet Xcellon-Ultra modules allows packet payload contents to be verified with a unique CRC that is independent of the packet CRC. This ensures that the payload is not disturbed as the device changes header fields.

# **Sequence and Duplicate Packet Checking**

Sequence numbers can be inserted at a user-defined offset in the payload of each transmitted packet. Upon receipt of the packets by the Device Under Test (DUT), out-of sequence errors or duplicated packets are reported in real time at wire-speed rates. You can define a sequence error threshold to distinguish between small versus big errors, and the receive port can measure the amount of small, big, reversed, and total errors. Alternatively, you can use the duplicate packet detection mode to observe that multiple packets with the same sequence number are received and analyzed.

# **Routing/Bridging Protocol Emulation**

Ixia's Gigabit Ethernet Xcellon-Ultra modules support performance and functionality testing using routing/bridging protocol emulation through the Aptixia IxNetwork and Aptixia IxAutomate applications. Protocols supported include IPv4/IPv6 routing (BGP-4, OSPF, ISIS, and RIP), MPLS (RSVP-TE, LDP, L2 MPLS VPNs, L3 MPLS VPNs, and VPLS), multicast (IGMP, MLD, and PIM-SM), and bridging (STP, RSTP, MSTP). Highly scalable scenarios can be created emulating up to thousands of routers advertising millions of routes per test port. Up to wire-speed Layer 2/3 traffic can be automatically created to target routes and MPLS tunnels.

### **Part Numbers**

The part numbers are shown in the following table.

Part Numbers for Network Processor Modules

Load Module	Price List Name	Description
Xcellon-Ultra XP-01	Xcellon-Ultra XP-01	10 Gigabit Ethernet, Application and Stream Load Module, 1-10G or 12-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps, for OPTIXIA XM2 or OPTIXIA XM12 chassis; 800MHz CPU with 1GB of memory per GbE port; On-Board Port Aggregation; GbE Fiber Ports REQUIRE SFP transceivers, options include SFP-LX or SFP-SX; and 10GbE port requires a XFP transceiver, options are either 948-0003 (XFP-850), XFP-1310, or XFP-1550
Xcellon-Ultra NP-01	Xcellon-Ultra NP-01	Same as version above but 1GHz CPU and 2GB of memory.

Load Module	Price List Name	Description
Xcellon-Ultra NG-01	Xcellon-Ultra NG-01	Same as above.
	SFP-SX	850nm SX SFP transceiver
	SFP-LX	SFP Transceiver - 1310nm LX
	XFP-850(948- 0003-01)	XFP 850nm Transceiver
	XFP-1550	XFP 1550nm Transceiver
	XFP-1310	XFP 1310nm Transceiver

# **Specifications**

The load module specifications are contained in the following table. The limitations of -3, Layer 2/3, and Layer 7 cards are discussed in <a href="Ixia Load Modules">Ixia Load Modules</a>.

Load Module Specifications

	Xcellon-Ultra XP-01		
	Xcellon-Ultra NP-01		
	Xcellon-Ultra NG-01		
Number of ports	12 GbE (10/100/1000) + 10GbE		
Maximum Ports per Chassis	144 GbE + 12 10GbE		
Connector	RJ-45 and SFP for GbE ports; XFP for 10GbE port		
Interfaces	Port 1 to port 12:1000Base-X100Base-FX1000Base-T (Aggreg ate, Copper mode)10/100/1000Base-T (Aggregate, Copper mode)100Base-TX10Base-TPort 13: 10GBase-X10G LAN XFP		
Port CPU	Xcellon-Ultra XP PowerPC 750GL x12 Port CPU Speed: 800 MHz Port CPU Memory: 1GB  Xcellon-Ultra NP PowerPC 750GX x12 Port CPU Speed: 1 GHz Port CPU Memory: 2GB		

	Xcellon-Ultra XP-01 Xcellon-Ultra NP-01 Xcellon-Ultra NG-01
	Xcellon-Ultra NG
	PowerPC 750GX x12
	Port CPU Speed: 1 GHz
	Port CPU Memory: 2GB
	41°F to 86°F (5°C to 30°C)
Ambient Operating Tem- perature Range	Using this load module in the XM2 or XM12 chassis lowers the chassis maximum operating temperature.
Connection rate (cps)	200K (in aggregated mode)
Layer 2-3 Routing Pro- tocol and Emulation	Yes
Layer 4-7 Application Traffic Testing	Yes
Capture Buffer per Port	32MB (Packet Group Engine Enabled)
Captare Barrer per Fort	64MB (Packet Group Engine Disabled)
Number of Transmit Flows per Port (sequen- tial values)	Bilions
Number of Transmit Flows per Port (arbitrary values)	98K
Number of Trackable Receive Flows per Port (PGIDs)	128K
Number of Stream Definitions per Port	Up to 4K in Packet Stream Mode (sequential) or Advanced Stream (interleaved) modes. Each Stream Definition can generate millions of unique traffic flows.
Transmit Engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures.
Receive Engine	Wire-speed packet filtering, capturing, real-time latency for each packet group, data integrity, and sequence checking.
User Defined Field (UDF) Features	Fixed, increment or decrement by user-defined step, value lists, range lists, cascade, random, and chained. Value list = 48K; Range list = 6K.

	Xcellon-Ultra XP-01 Xcellon-Ultra NP-01 Xcellon-Ultra NG-01
Table UDF Feature	Comprehensive packet editing function for emulating large numbers of sophisticated flows. Up to 786K table UDF entries are supported on the XMV12X.
Filters	48-bit source/destination address, 2x128-bit user-definable pattern and offset, frame length range, CRC error, data integrity error, sequence checking error (small, big, reverse)
Data Field (per stream)	Fixed, increment (Byte/Word), decrement (Byte/Word), random, repeating, user-specified up to 13K bytes.
Statistics and Rates: Counter Size: 64-Bit	Link State, Line Speed, Frames Sent, Valid Frames Received, Bytes Sent/Received, Fragments, Undersize, Oversize, CRC Errors, VLAN Tagged Frames, User-Defined Stat 1, User-Defined Stat 2, Capture Trigger (UDS 3), Capture filter (UDS 4), User-Defined Stat 5, User-Defined Stat 6, 8 QoS counters, Data Integrity Frames, Data Integrity Errors, Sequence Checking Frames, Sequence Checking Errors, ARP, and Ping requests and replies.
Error Generation	CRC (Good/Bad/None), Undersize, Oversize
Packet Flow Statistics	Real-time statistics to track up to 128K packet flows on the XMV12X with throughput and latency measurements.
Latency Measurements	20 ns resolution.
IPv4, IPV6, UDP, TCP	Hardware checksum generation.
Frame Length Controls	Fixed, random, weighted random, or increment by user- defined step, random, weighted random.
	Aptixia IxLoad: Layer 4-7 performance testing of content-aware devices and networks.
	Aptixia IxNetwork: Integrated Layer 2-3 data/control plane performance and functional testing, supporting routing, bridging, MPLS, and multicast protocols.
	Aptixia IxAutomate: Automation environment providing pre- built tests for Layer 2-7 data and control plane testing.
Applications	IxExplorer: Layer 2-3 wire-speed traffic generation and analysis.
	IxChariot®: Emulated application performance testing over Layer 4.
	IxAccess: Broadband access performance testing, including PPPoX and L2TPv2/v3.
	IxVPN: Performance verification of IPSec devices and net-

Xcellon-Ultra XP-01
Xcellon-Ultra NP-01
Xcellon-Ultra NG-01
works.
Tcl API: Custom user script development for Layer 2-7 testing.
Linux Software Development Kit (SDK): Custom user application development. Full TCP/IP connectivity through management interface (Telnet, FTP, and so on.)

### **Port LEDs**

Each Xcellon-Ultra port incorporates a set of two LEDs, as described in the following table. The 1GbE LEDs are used in Normal and 1GbE Aggregate modes. They behave identically in both modes, except that due to switch limitations, the `CRC Error' LED is non-operational in 1GE Aggregate mode (that is, it never indicates error). The 1GE LEDs are disabled (always off) in 10GE Aggregate mode.

1GE Port LEDs for Xcellon-Ultra Modules

LED Label	Copper	Fiber
1GE Link/Tx (Upper LED)	Color is used to indicate the link speed:  • 1000Mbps-Green  • 100Mbps-Orange  • 10Mbps-Yellow  Flashing indicates transmit activity.  Off if link is down.	Green indicates link has been established and flashes during transmit activity.No link = off.
1GE Rx/Error (Lower LED)	<ul> <li>Full duplex or master (in 1000 Mbps case) green with extended pulses off to indicate receive activity.</li> <li>Half duplex or subordinate (in 1000 Mbps case) off with extended pulses to indicate receive activity.</li> <li>Error overrides the other two modes and pulses red (supported only in Normal mode).</li> <li>No link off.</li> </ul>	Green indicates link has been established and flashes during receive activity.  Continuous red indicates a receive error (supported only in Normal mode).

10GE LEDs are disabled (always off) in Normal and 1GE Aggregate modes. In 10GE Aggregate mode, the two LEDs behave as described in the following table.

#### 10GE Port LEDS for Xcellon-Ultra Modules

LED Label	Usage
10GE Link/Tx (Upper LED)	Green indicates link has been established. Flashes during transmit activity.No link = off.
10GE Rx/Error (Lower LED)	Green indicates link has been established. Flashes during receive activity.No link = off.

# **Statistics**

Statistics for Xcellon-Ultra cards, under various modes of operation may be found in  $\underline{\text{Avail}}$ able Statistics.



# Chapter 21 - IXIA 40/100 Gigabit Ethernet Load Modules

This chapter provides details about Ixia's K2 40-Gigabit and 100-Gigabit Ethernet test modules the specifications and features.

Ixia's K2 40-Gigabit and 100-Gigabit Ethernet test modules are the world's first IP network traffic generation and layer 2-7 measurement and analysis test solution. K2 load modules are engineered to meet the needs of product teams developing 40 Gb/s and 100 Gb/s network devices such as routers, switches, and communications devices. K2 modules can measure and analyze the performance of Higher Speed Ethernet (HSE) standard-compliant devices at line rate, and are compatible with Ixia's chassis and broad range of 10 Mbps, 100 Mbps, 1 Gbps, and 10 Gbps interfaces, allowing real-world, full product testing in a single box.

Ixia's 40 Gb/s and 100 Gb/s load modules provide network device developers the ability to test 40 GE and 100 GE hardware electronics at full line-rate operation. Early adopters of the HSE technology can use the Ixia test system to validate their compliance with the new PCS lane operation of the IEEE P802.3ba draft standard.

Ixia's K2 load modules are valuable to developers who are integrating firmware and software into new electronics hardware, or integrating optical transceivers into their network devices and systems. Ixia's HSE modules can be used to validate and benchmark the performance limits of these network devices by employing layer 2 and 3 stress testing, virtual scalability testing, and negative testing. Ixia's HSE load modules ensure that a network device is ready to interoperate with other manufacturers' devices that claim compliance to the IEEE P802.3ba draft standard, and facilitate interoperability testing between different vendors of network devices and equipment.

Figure: 100GE and 40GE LSM XMV Load Modules



Figure: 40GE LSM XMV QSFP Load Module



### **Key Features**

Industry's first 40 Gb/s and 100 Gb/s Layer 2 through 7 IP test solutions:

- 6 ports per XM12 chassis (10 rack mount units)
   Compatible with XM12 (941-0002) and XM12 High Performance chassis (941-0009)
- 1 port per XM2 (941-0003) desktop chassis

Industry's first commercially available 100 Gb/s Physical Coding Sublayer (PCS) test system:

Provides the ability to check compliance to the IEEE P802.3ba draft standard for both Transmit and Receive sides

Generates and analyzes full 40 Gb/s and 100 Gb/s line rate traffic:

- Tracks and analyzes up to 1 million flows per port for;
  - Real-time latency
  - Inter-arrival time
  - Packet loss
  - Data integrity
  - Sequence checking
  - Packet capture

Ixia's 40 Gb/s and 100 Gb/s load modules are designed for comprehensive layer 2-7 testing with integrated data plane and control plane traffic generation and analysis.

### **Nomenclature**

The LSM HSE family identifying numbers are shown in the following table.

LSM HSE Modules

Load Mod- ule	Model Number	Description
		1-port 40GE, 2-slot, full-featured load module.
40GE LSM XMV1	HSE40GETSP1-01	Supports routing protocols, Linux SDK, and L4-7 applications (requires 40GE CFP MSA transceiver).
100GE LSM XMV1	HSE100GETSP1-01	1-port 100GE, 2-slot, full-featured load module. Supports routing protocols, Linux SDK, and L4-7

Load Mod- ule	Model Number	Description
		applications (requires 100GE CFP MSA transceiver).
40/100GE LSM XMV	HSE40/100GETSP1- 01	1-port, 2-slot, dual-speed, full-featured load module with CFP interface
40GE LSM XMV QSFP	HSE40GEQSFP1-01	1-port, 1-slot, full-featured load module with QSFP interface

Specification are given in the following table.

### **HSE Module Specifications**

113L Module Specifications		
	HSE40GETSP1HSE100GETSP1HSE40/100- GETSP1	HSE40GEQSF- P1
Number of ports per module	1	1
Number of chassis slots per module	2	1
Maximum ports per chassis	XM12: 6 XM12 High Performance: 6 XM2: 1	
Supported transceivers	CFP MSA Pluggable	QSFP Pluggable
Data Rate	40 Gbps100 Gbps	40 Gbps
Port CPU Speed and memory	1GHz/2 GB	1GHz/2 GB
Per-port Cap- ture buffer	1.4 GB	700 MB
Interface protocol	40 Gigabit Ethernet per IEEE P802.3ba, Draft 2.0, 100GBASE-R 100 Gigabit Ethernet per IEEE P802.3ba, Draft 2.0,40GBASE-R	40 Gigabit Ethernet per IEEE P802.3ba, Draft 2.0, 100GBASE-R
Ambient Operating Temp. Range	41°F to 95°F (5°C to 35°C)  Ambient air temperature at the installation site for the system should not exceed 95°F	41°F to 95°F (5°C to 35°C)

	HSE40GETSP1HSE100GETSP1HSE40/100- GETSP1	HSE40GEQSF- P1
	NOTE (35°C).	ent air tem- per- ature at the install- ation site for the sys- tem should not excee- d 95°F (35°- C).
Layer 2/3 routing pro- tocol emu- lation	Yes	
Layer 4-7 application traffic test- ing	Yes	
Number of transmit flows per port (sequen- tial)	Billions	
Number of transmit flows per port (arbit- rary values)	1 million	
Number of trackable receive flows	1 million	
Captured packet size	49-14,000 bytes	49-14,000 bytes

	HSE40GETSP1HSE100GETSP1HSE40/100- GETSP1	HSE40GEQSF- P1
Number of stream defin- itions per port	In packet stream (sequential) or advanced stream (interleaved) mode, each stream definition can generate millions of unique traffic flows.  In the Data Center mode, the number of transmit streams is 256.	256
Preamble size	8 bytes	8 bytes
Frame size: min-max (bytes)	49-14,000	49-14,000
Inter-frame gap: min- max	1.8ns - 21.99sec	1.8ns - 21.99sec
Inter-burst gap: min- max	1.8ns - 21.99sec	1.8ns - 21.99sec
Inter- stream gap:min- max	1.8ns - 21.99sec	1.8ns - 21.99sec
Normal stream frame rate	0.045 fps - full line rate	0.045 fps - full line rate
Advanced stream min frame rate	0.091fps	0.091fps
Latency meas- urements	standard resolution as 20ns user selectable high resolution as 2.5ns	20 nanosecond resolution user selectable high resolution as 2.5ns
Table UDF Entries	1million  Comprehensive packet editing function for emulating large numbers of sophisticated flows. Entries of up to 256 bytes, using lists of values, can be specified and placed at designated offsets within a stream. Each list consists of an offset, a size, and a list of values in a table format.	1 million

	HSE40GETSP1HSE100GETSP1HSE40/100- GETSP1	HSE40GEQSF- P1
Max Value List UDF entries	1 million entries for 32-bit and 24-bit, 2 million entries for 8 and 16-bit.	1 million entries for 32-bit and 24-bit, 2 million entries for 8 and 16-bit.
Max Range List UDF entries	N/A	N/A
Packet flow statistics	Track over 1 million flows	
Transmit Engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures	
Receive Engine	Wire-speed packet filtering, capturing, real-time latency and inter-arrival time for each packet group, data integrity, and sequence checking	
User defined field features	Fixed, increment, or decrement by user-defined step, value lists, range lists, cascade, random, and chained	
Filters	48-bit source/destination address, 2x128-bit user definable pattern and offset, frame length range, CRC error, data integrity error, sequence checking error (small, big, reverse)	
Data field per stream	Fixed, increment or decrement by user-defined step, value lists, range lists, cascade, random, and chained	
Statistics and rates (counter size: 64 bits)	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 userdefined stats, capture trigger (UDS 3), capture filter (UDS 4), user-defined stat 5, user-defined stat 6, 8 QoS counters, data integrity frames, data integrity errors, sequence checking frames, sequence checking errors, ARP, and ping requests and replies	
Error gen- eration	CRC (good/bad/none), undersize, oversize	
MDIO	Ability to calibrate and remove inherent latency from any MSAcompliant 40 Gb/s or 100Gb/s CFP transceiver	
Transmit line clock	Ability to adjust the parts per million (ppm) line frequency over a range of LAN mode: - 100 to +100 ppm	

	HSE40GETSP1HSE100GETSP1HSE40/100- GETSP1	HSE40GEQSF- P1
adjustment		
Clock In/Out	The load module provides two female SMA coaxial connectors one for clock input and one for clock output to allow the device under test (DUT) to frequency-lock with the load module interface. See <a href="Clock In/Out">Clock In/Out</a> .	
	The load module supports the following BERT features on both 40 Gb/s and 100 Gb/s speeds:	
Layer 1 BERT cap- ability	<ul> <li>User selected PRBS pattern for each PCS Lane</li> <li>User selects from a wide range of PRBS data patterns to be transmitted (true and complement)</li> <li>Send single, continuous, and exponentially controlled amounts of error injection</li> <li>Wide range of statistics, including: Pattern Lock, Pattern Transmitted, Pattern Received, Total Number of Bits Sent and Received, Total Number of Errors Sent and Received, Bit Error Ratio (BER), Number of Mismatched 1's and 0's.</li> <li>Lane Stats Grouping per lambda for SMF and MMF 40 Gb/s and 100 Gb/s based on IEEE802.3ba defined physical medium dependent (PMD).</li> </ul>	
Physical Coding Sublayer (PCS) test features	IEEE P802.3ba compliant PCS transmit and receive side test capabilities.	
Per PCS lane, trans- mit lane mapping	Supports all combination of PCS lane mapping: Default, Increment, Decrement, Random, and Custom.	
Per PCS lane, skew insertion and deskew capability	User selectable from zero up to 3 microseconds of skew insertion on transmit side. Ability to measure deskew up to 6 microseconds on receive side.	
IPv4, IPv6, UDP, TCP	Hardware checksum generation, and verification.	
Frame length con- trols	Fixed, random, weighted random, or increment by user-defined step, random, weighted random.	
Preamble view	Allows to select to view the preamble in Packet View.	

	HSE40GETSP1HSE100GETSP1HSE40/100- GETSP1	HSE40GEQSF- P1
Link Fault Signaling	Ability to select the option to have the transmit port ignore link faults from a remote link partner.	

### **Port LEDs**

Each 40/100GE port incorporates a set of LEDs, as described in the following tables.

40/100GE LSM Port LEDs

LED Label	Usage
Link	Green if Ethernet link is up (established) or the port is in a forced Link Up state, red if link is down. Link may be down due to no signal or no PCS lock.
Tx Active	Green indicates that Tx is active and frames being sent; red indicates Tx is paused; off indicates Tx is not active.
Rx Active	Green indicates that Rx is active and frames being received; red indicates Rx is paused; off indicates Rx is not active.
Rx/Error	Green indicates valid Rx frames are being received; red indicates error frames being received; off indicates no frames being received.
Attention	(Reserved for future use)
Pwr Good	Green when power is on, red if power fault occurs.

# **Clock In/Out**

The load module provides coaxial connectors for clock input and clock output to allow the DUT to frequency-lock with the interface. When running off an external clock, the clock input signal must meet the requirements listed in the following table to ensure proper performance of the load module.

The clock in/out electrical interface parameters are also defined in the following table.

Clock In/Out Electrical Interface Parameters

Parameter		Characteristic
ClockInput	Frequency	161.13 MHz ±100ppm
	Duty cycle	50%
	Jitter	±150ps max. cycle to cycle, >1kHz
		Recommended: 800mV
	Amplitude	Minimum: 150mV
		Maximum: 1200mV
	Impedance	50 ohm ± 5%, DC coupled

Parameter		Characteristic
	Connector	Female SMA
ClockOutput	Frequency	161.13 MHz +/-100ppm (Programmable ppm in Internal Clock Mode)
	Duty cycle	40 to 60%
	Jitter	20ps max cycle to cycle, >1kHz
	Amplitude	0.7Vpp min into 50 ohms, AC coupled output
	Edge rates	200ps to 340ps (20% to 80%) into 50 ohms
	Impedance	50 ohms +/-5%, AC coupled
	Connector	Female SMA

The load module contains a phase-locked loop (PLL) that reduces the jitter of the input clock, either from the internal or external clock source. The bandwidth of the PLL is approximately 1kHz.

#### **Statistics**

Statistics for 40/100GE LSM cards, under various modes of operation may be found in 40/100 GE Statistics.

# **Intrinsic Latency Adjustment**

This option, when present and enabled, reduces the measured latency by the amount of latency that is induced by the test equipment itself (not the DUT). For a specific transceiver, the system retrieves its pre-determined latency value and subtracts this from the measured overall latency. For an `unknown' transceiver (not previously measured), it calculates and stores the intrinsic latency value.

On the **General** tab in **Port Properties**, the **Latency Calibration** option is only enabled for cards with transceivers that have not been pre-measured for intrinisic latency by Ixia. The **Latency Calibration** option is grayed-out if any one of the following conditions are present:

- · there is no transceiver
- the transceiver is CFP and a value is found for it in the list of precalibrated values

The **Latency Calibration** option is enabled if the transceiver is CFP but no pre-calibrated value is found in the stored list. The **Latency Calibration** option is also enabled for transceivers that you have previously calibrated, so that the calibration measurement may be repeated (if desired).

Clicking the **Latency Calibration** option runs a Tcl script that measures intrinsic latency and stores the value in an .xml file. The .xml file contains the values that you have produced and saved. Each value is identified for a specific transceiver (per manufacturer,

model, and serial number). You can run the calibrate process repeatedly with the same transceiver (if desired). Each new measurement overwrites the previous one for that transceiver.

Running the calibration measurement puts the port into a special loopback mode to measure intrinsic latency. When done, the port is put back into default normal mode. Any port configuration you have set before calibrating intrinsic latency, is lost as the port reverts to a default configuration.

The **Enable** check box is grayed out when no value exists in the system for the specific transceiver. If a value exists in the .xml file, then the **Enable** check box is available. Select the check box to enable the intrinsic latency adjustment.

After the intrinsic latency adjustment has been done, you may want to refresh the chassis or close and reopen the Port Properties dialog.

# **Multilane Distribution Configuration**

The Tx Lane tab allows to control the PCS (Physical Coding Sublayer) lane configuration and skew. It is part of the Port Properties for the module.

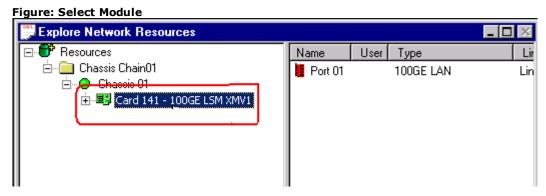
—— THE OU Guide

NOTE

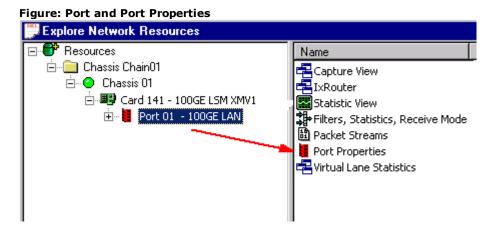
The other tabs in the Port Properties page are described in the *IxExplorer User Guide*, as are the rest of the controls for the module.

To open the Tx Lane tab:

1. Select the 40 or 100GE LSM XMV1 module in the left pane of the IxExplorer window as shown in the following figure.

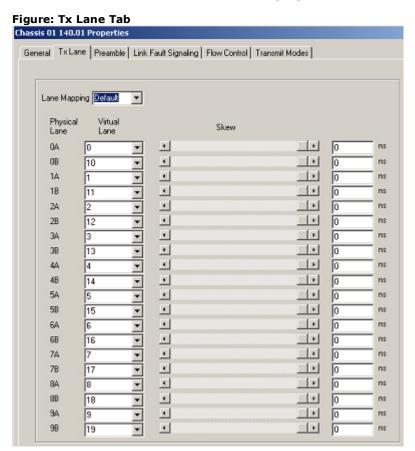


2. Expand the node, and select the Port object. In the right window pane, double-click the Port Properties object as shown in the following figure.



3. In the Port Properties dialog, select the Tx Lane tab. Use this tab to control the PCS lane order and the skew for each lane.

The Tx Lane tab is shown in the following figure.



The following table explains the options in the Tx Lane tab page.

Tx Lane Tab Configuration

Field	Description		
Lane Mapping	<ul> <li>Allows you to select a PCS lane ordering method. There are four options:</li> <li>Default: The default ordering method. The default order is each physical port corresponds to 2 PCS lanes that are n and n+10,</li> </ul>		

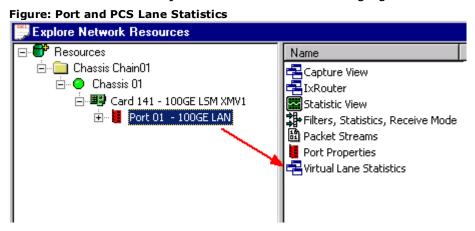
Field	Description	
	<ul> <li>where n = physical lane number.</li> <li>Increment: Orders the lanes from 0 to 19, straight down the list.</li> <li>Decrement: Orders the lanes from 19 to 0, straight down the list.</li> <li>Custom: Allows to put the lanes in any order by manually entering the numbers in the fields. The starting order is the last selected mapping.</li> </ul>	
Physical Lane	The physical lane identifier. The physical lane is paired with a corresponding PCS lane.	
PCS Lane	A number identifier for the PCS lane. The PCS lane is paired with a corresponding physical lane.	
	The skew slider is used to set a skew value for the PCS lane, in nano- seconds, on the transmit side. Lane Skew is the ability to inde- pendently delay one or more of the 20 PCS lanes.  When the slider is moved, the nanoseconds field is correspondingly	
Skew	adjusted. You can also enter a nano second value directly into this field.	
	When the slider is fully pushed to the right, the skew injected into the transmit stream is 0 (minimum). When the slider is pushed all the way to the left. the skew injected into the transmit stream is 3 uS (maximum).	

#### **PCS Lane Statistics**

The PCS lane statistics table allows to view the statistics for the configured PCS lanes.

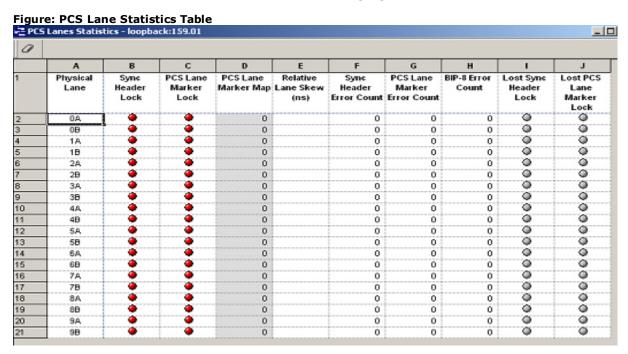
To open the PCS lane statistics table:

- 1. Select the 40 or 100GE LSM XMV1 module in the left pane of the IxExplorer window as shown in the figure.
- 2. Expand the node, and select the Port object. In the right window pane, double-click the PCS lane statistics object as shown in the following figure.



3. The PCS lane statistics table opens. Use this table to view the PCS lane statistics for each lane. The statistics are for the **receive** side.

The PCS lane statistics table is shown in the following figure.



The following table explains the entries in the PCS lane statistics table.

PCS Lane Statistics Data

Field	Description		
Physical Lane	The identifier for the Receive physical lane. This is a tag/fixed label to ID each lane.		
Sync Header Lock	Indicates if the received PCS lane achieved sync-bit lock. Green indicates success, red failure.		
PCS Lane Marker	Indicates if the received PCS lane has achieved alignment marker lock.		
LOCK	Green indicates success, red failure.		
PCS Lane Marker Map	The PCS lane number identified by the alignment marker. This is only valid when PCS Lane Marker Lock is green.		
	Shows the actual skew in nanoseconds.		
Relative Lane Skew (ns)	Skew measurements are valid only when all lanes are locked with 20 unique lane markers.		
	The first PCS Lane markers to arrive have skew of 0. All other lane skews are relative to them.		
Sync Header Error Count	The number of synchronization bit errors received.		
PCS Lane Marker	The number of incorrect PCS lane markers received while in PCS		

Field	Description	
Error Count	lane lock state.	
BIP-8 Error Count	Bit interleaved parity error count. It detects the number of BIP-8 errors for a PCS lane.	
Lost Sync Header Lock	When lit, indicates the loss of sync header lock since the last statistic was read. If colored gray, there is no error. If colored red, an error has occurred.	
Lost PCS Lane Marker Lock	When lit, indicates the loss of PCS lane marker lock since the last statistic was read. If colored gray, there is no error. If colored red, an error has occurred.	

# Chapter 22 - IXIA 10 Gigabit Ethernet Load Modules

This chapter provides details about 10 Gigabit Ethernet (10GE) family of load modules the specifications and features.

The 10 Gigabit Ethernet (10GE) family of load modules implements five of the seven IEEE 8.2.3ae compliant interfaces that run at 10Gbit/second. Cards are available which offer the following interfaces:

- 10GE LAN
- 10GE WAN
- XAUI
- XENPAK with options for XPAK or X2 transceiver use.

The following figure shows an LM10GEXENPAK module.

Figure: LM10GEXENPAK



In addition, two families of multimode card are available which offers combined 10GE LAN/WAN, OC192 POS, BERT, and FEC functionality. The features available for these load modules are described in IXIA 10GE LAN/WAN and OC 192 POS Load Modules.

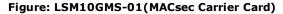
The full details for these families may be found at:

- LSM 10GE Family
- 10GE LAN Family
- XAUI Family
- XENPAK Family

### **LSM 10GE Family**

The Ixia 10 Gigabit Ethernet LAN Service Module (LSM) offers unprecedented scalability, performance, and service testing flexibility. The Ixia 10GE LSM is Ixia's third-generation 10 Gigabit Ethernet solution. It is the industry's first six-port solution, and it offers a broad portfolio of edge/ core testing solutions for the most demanding test environments including performance, scalability, and conformance testing of Layer 2-3, Routing Protocols, and high performance Layer 4-7 testing. It supports IPv4 and IPv6 wire-speed traffic generation, advanced analysis and IPv4 and IPv6 routing protocol emulation.

The Ixia 10GE LSM supports a comprehensive portfolio of service testing solutions for the next-generation service provider networks including Metro Ethernet E-LAN and E-LINE services; and MPLS VPNs such as Layer 2 VPNs, Layer 3 RFC 2547 VPNs, and VPLS.





#### **Part Numbers**

The LSM family part numbers are shown in the following table.

10GE LSM modules

Load Mod- ule	Part Number	Description
10GE LSM	LSM10G1-01	1-port 10GE, single slot, full-featured load module. Supports routing protocols, Linux SDK, and L4-7 applications (requires XENPAK or XFP adapter and matching transceiver).
10GE LSM MACSec	LSM10GMS-01	1-port 10GE, single slot, full-featured load module. Supports routing protocols, Linux SDK, and L4-7 applications. Supports MACSec functionality for stream generated traffic. XFP LAN/WAN carrier card is integrated.
10GE LSM	LSM10GXMR8- 01LSM10GXMR8GBT-	NGY 8-port 10GE, 400MHz, 128MB single slot,

Load Mod- ule	Part Number	Description
XMR810GE LSM XMR8 10GBASE-T	01	reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applications.Includes 10GBASE-T version.
10GE LSM XM8XP10GE LSM XM8 10GBASE-T	LSM10GXM8XP-01 LSM10GXM8GBT-01	NGY 8-port 10GE, 800MHz, 1GB, Extra Performance. Includes 10GBASE-T version.
10GE LSM XM8S	LSM10GXM8S-01	NGY 8-port 10GE, LAN/WAN, SFP+ interface with 1GB RAM per port; for OPTIXIA XM12-02 and OPTIXIA XM2-02 chassis; full L2/7 support. Requires one or more SFP+ transceiver options: 10GBASE-SR, 10GBASE-LR, 10GBASE-LRM, or 10GSFP+Cu.
10GE LSM XMR8S	LSM10GXMR8S-01	Same as 10GE LSM XM8S but reduced L2/3 support with limited L3 routing.
NGY-NP8-01	NGY-NP8-01	10 Gigabit Application Network Processor Load Module, 8-Port LAN/WAN, SFP+ interface.
10GE LSM XMR410GE LSM XMR4 10GBASE-T	LSM10GXMR4- 01LSM10GXMR4GBT- 01	NGY 4-port 10GE, 400MHz, 128MB, single slot, reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applications.Includes 10GBASE-T version.
10GE LSM XM4XP10GE LSM XM4 10GBASE-T	LSM10GXM4XP- 01LSM10GXM4GBT- 01	NGY 4-port 10GE, 1GHz, 1GB, Extra Performance. Includes 10GBASE-T version.
10GE LSM XM4S	LSM10GXM4S-01	NGY 4-port 10GE, LAN/WAN, SFP+ interface with 1GB RAM per port; for OPTIXIA XM12-02 and OPTIXIA XM2-02 chassis; full L2/7 support. Requires one or more SFP+ transceiver options: 10GBASE-SR, 10GBASE-LR, 10GBASE-LRM, or 10GSFP+Cu.
10GE LSM XMR4S	LSM10GXMR4S-01	Same as 10GE LSM XM4S but reduced L2/3 support with limited L3 routing.
NGY-NP4-01	NGY-NP4-01	10 Gigabit Application Network Processor Load Module, 4-Port LAN/WAN, SFP+ interface.
10GE LSM XM2XP10GE LSM XM2 10GBASE-T	LSM10GXM2XP- 01LSM10GXM2GBT- 01	NGY 2-port 10GE, 1GHz, 1GB, Extra Performance. Includes 10GBASE-T version.
10GE LSM XMR210GE LSM	LSM10GXMR2- 01LSM10GXMR2GBT-	NGY 2-port 10GE, 400MHz, 128MB, single slot, reduced L2/3 support with limited L3 routing,

Load Mod- ule	Part Number	Description	
XMR2 10GBASE-T	01	Linux SDK, and L4-7 applications. Includes 10GBASE-T version.	
10GE LSM XM2S	LSM10GXM2S-01	NGY 2-port 10GE, LAN/WAN, SFP+ interface with 1GB RAM per port; for OPTIXIA XM12-02 and OPTIXIA XM2-02 chassis; full L2/7 support. Requires one or more SFP+ transceivers: 10GBASE-SR, 10GBASE-LR, 10GBASE-LRM, or 10GSFP+Cu.	
10GE LSM XMR2S	LSM10GXMR2S-01	Same as 10GE LSM XM2S but reduced L2/3 support with limited L3 routing.	
NGY-NP2-01	NGY-NP2-01	10 Gigabit Application Network Processor Load Module, 2-Port LAN/WAN, SFP+ interface.	
XENPAK-ADAP- 01	948-0007	XENPAK LAN Adapter for LSM10Gx1-xx.	
XFP-ADAP-02	948-0002	LAN/WAN Adapter for LSM10Gx1-xx	
X2-ADAP-01	948-0008	X2 Carrier	
10GBASET- ADAP-01	948-0009	10GBase-T Adapter for LSM10Gx1-xx	
SFP-ADAP-01	948-0012	SFP+ Adapter for LSM10G1 and LSMGL1, must be used with an SFP+ transceiver.	
SFP+ trans- ceiver 10GBASE-SR	948-0013	10GBASE-SR Accessory, SFP+ Transceiver for 10GE LAN/WAN load modules with pluggable SFP interface, 850nm.	
SFP+ trans- ceiver 10GBASE-LR	948-0014	10GBASE-LR Accessory, SFP+ Transceiver for 10GE LAN/WAN load modules with pluggable SFP interface, 1310nm.	
SFP+ trans- ceiver 10GBASE-LRM	948-0015	10GBASE-LRM Accessory, SFP+ Transceiver for 10GE LAN load modules with pluggable SFP+ interface, 1300nm, MMF.  LAN mode is not supported.	
		· · · · · · · · · · · · · · · · · · ·	
SFP+ trans- ceiver 10GSFP+Cu	948-0016	10GSFP+Cu Accessory, Direct Attach Cable Transceiver for 10GE LAN/WAN load modules with pluggable SFP+ interface, Copper Wire, 3 meter length.	
10GE LSM XM8NGY	944-1070-01	LSM10GXM8NG-01 10 Gigabit Ethernet Load Module, 8-Port LAN/WAN, XFP interface	
10GE LSM XM4NGY	944-1071-01	LSM10GXM4NG-01 10 Gigabit Ethernet Load Module, 4-Port LAN/WAN, XFP	

Load Mod- ule	Part Number	Description
10GE LSM XM2NGY	944-1096-01	LSM10GXM2NG 10 GIGABIT ETHERNET LOAD MODULE, 2-Port LAN/WAN, XFP

### 10GE LSM Load Module Specifications (except NGY)

TOGE EST	LSM10G1-01	LSM10GMS- 01
# ports	1	1
Data Rate	10GB	10GB
Port CPU Speed	1GHz (G1)500MHz (GL1)	1GHz
Port CPU Memory	512MB (G1)128MB (GL1)	512MB
Connector/Frequency- Mode	XFP or XENPAK/X2. See XENPAK Connectors  10GBase-T Adapter, see Removable Carrier Cards	Integrated XFP LAN/WAN car- rier card Also XFP-CX4
	Also XFP-CX4 and SFP-CX4	
Ambient Operating Temp. Range	41°F to 95°(5°C to 35°C)	41º to 95º (5ºC to 35ºC)
Capture buffer size	Up to 384 MB	Up to 384 MB
Captured packet size	17-65,535 bytes	17-65,535 bytes
Streams per port	256	256
Advanced streams	256	256
Preamble size: min- max	8	8
Frame size: min-max (bytes)	17-65,535	17-65,535
Inter-frame gap: min-max <sup>3</sup>	4.0ns - 42sec in 3.2ns steps	4.0ns - 42sec in 3.2ns steps
Inter-burst gap: min- max	4.0ns - 42sec in 10.0ns steps	4.0ns - 42sec in 10.0ns steps
Inter-stream gap:min-max	4.0ns - 42sec in 10.0ns steps	4.0ns - 42sec in 10.0ns steps
Normal stream frame rate	0.023fps - full line rate	0.023fps - full line rate

	LSM10G1-01	LSM10GMS- 01
Advanced stream min frame rate <sup>4</sup>	Slow: 0.023fpsFast: 1525fps	Slow: 0.023fpsFast: 1525fps
Latency <sup>5</sup>	20ns resolution	20ns resolution  The `No CRC' option is not supported.
Table UDF Entries	1M (full)32K (reduced)	1M
Max Value List UDF entries	G1:512K entries GL1:8K entries	512K entries
Max Range List UDF entries	G1:256 entries GL1:16 entries	

<sup>&</sup>lt;sup>1</sup>The LSM10GMXR3-01 only supports IxNetwork, IxAutomate, and IxExplorer.

Load Module Specifications

Feature	Extra Performance	Reduced Performance
	LSM10GXM8XP	LSM10GXMR8
	LSM10GXM4XP	LSM10GXMR4
	LSM10GXM2XP	LSM10GXMR2
	LSM10GXM8S	LSM10GXMR8S
Load Modules	LSM10GXM4S	LSM10GXMR4S
	LSM10GXM2S	LSM10GXMR2S
	LSM10GXM8GBT	LSM10GXMR8GBT
	LSM10GXM4GBT	LSM10GXMR4GBT
	LSM10GXM2GBT	LSM10GXMR2GBT
Number of ports per mod- ule	8/4/2	8/4/2
Line rate	10 Gb/s	10 Gb/s
Number of chassis slots per module	1	1

<sup>&</sup>lt;sup>2</sup>Packet gap size also depends on the stream mode selected Fixed or Average.

<sup>&</sup>lt;sup>3</sup>Streams are divided up into two categories: 224 slow speed streams and 32 fast streams.

<sup>&</sup>lt;sup>4</sup>Cancel Intrinsic Latency feature measures and/or removes the latency induced by the test equipment (not the DUT). See <a href="Intrinsic Latency Adjustment">Intrinsic Latency Adjustment</a>.

Feature	Extra Performance	Reduced Performance	
Maximum ports per chassis			
XM12 High Performance	96/48/24 <sup>1</sup>	96/48/241	
XM2 Desktop	16/12 <sup>1</sup> /8/4	16/8/4	
Supported transceivers			
(optical and copper)			
The NGY family of load modules can support transceivers that use up to 2.5W of power. Do not use transceivers beyond 2.5W.	XFP, SFP+, RJ-45 10GBASE-T	XFP, SFP+, RJ-45 10GBASE-T	
Per-port CPU speed and memory	1 GHz, 1 GB <sup>2</sup>	400 MHz/128 MB	
Per-port capture buffer	512 MB	64 MB	
Captured packet size	17 bytes absolute minimum frame size64 bytes minimum frame size at line rate		
		For LSM10GXMR8,	
		LSM10GXMR4	
		LSM10GXMR2	
	Minimum: 48 bytes	Minimum Frame Size at Line Rate: 48	
Frame size	Maximum: 16,000 bytes	Minimum Frame Size - may not be at Line Rate: 48	
		Maximum Frame Size: 4Q: 9216	
		8 + 1Q: P0: 9216B others 2500B	
Interface protocols	10 GE LAN/WAN	10 GE LAN/WAN	
Layer 2/3 routing protocol emulation	Yes	Yes	
Layer 4-7 application traffic testing	Yes	No	

Feature	Extra Performance	Reduced Performance
Number of transmit flows per port (sequential values)	Billions	Billions
Number of transmit flow per port (arbitrary values)	1 million	32 K
Number of trackable receive flows	1 million	64K
Number of stream definitions per port	512	512
	In packet stream (sequential) leaved) mode, each stream de of unique traffic flows.	`
Preamble size: min-max	8	8
Inter-frame gap: min- max	3.2ns - 27.48sec in 3.2ns steps	3.2ns - 27.48sec in 3.2ns steps
Inter-burst gap: min-max	3.2ns - 27.48sec in 3.2ns steps	3.2ns - 27.48sec in 3.2ns steps
Inter-stream gap:min- max	3.2ns - 27.48sec in 3.2ns steps	3.2ns - 27.48sec in 3.2ns steps
Normal stream frame rate	0.023fps - full line rate	0.023fps - full line rate
Advanced stream min. frame rate	Slow: 0.023fpsFast: 1525fps	Slow: 0.023fpsFast: 1525fps
Number of streams in Packet Stream Mode (Non Data Center Mode)	512	512
Number of streams in Advanced Scheduler Mode (Non Data Center Mode)	Fast: 32Slow: 480	Fast: 32Slow: 480
Number of streams in Advanced Scheduler Mode (Data Center Mode)	Fast: 32Slow: 224	Fast: 32Slow: 224
Table UDF	1 million entries	32 K
	Comprehensive packet editing numbers of sophisticated flow using lists of values can be speignated offsets within a stream set, a size and a list of values	s. Entries of up to 256 bytes, ecified and placed at des- n. Each list consists of an off-

Feature	Extra Performance	Reduced Performance	
Max Value List UDF entries	512K entries for 32-bit and 24-bit, 1M entries for 8 and 16-bit.  256K entries for 32-bit and 24-bit, 512K entries for 8 and 16-bit.		
Max Range List UDF entries	512 entries	256 entries	
Packet flow statistics	Track 1 million flows	Track 64 K flows	
Transmit engine	Wire-speed packet generation numbers, data integrity signat natures		
Receive engine	Wire-speed packet filtering, ca inter-arrival time for each pac sequence checking	apturing, real-time latency and ket group, data integrity, and	
User defined field features	Fixed, increment or decremen lists, range lists, cascade, range	• •	
Filters	48-bit source/destination address, 2x128-bit user-definable pattern and offset, frame length range, CRC error, data integrity error, sequence checking error (small, big, reverse)		
Data field per stream	Fixed, increment (byte/word), decrement (byte/word), random, repeating, user-specified.		
Statistics and rates (counter size: 64 bits)	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 user-defined stats, capture trigger (UDS 3), capture filter (UDS 4), user-defined stat 5, user-defined stat 6, 8 QoS counters, data integrity frames, data integrity errors, sequence checking frames, sequence checking errors, ARP, and ping requests and replies.		
Error generation	CRC (good/bad/none), undersize, oversize.		
Latency measurements	20 ns standard		
Latericy measurements	10 ns user-selectable		
Latency self-calibration	Ability to calibrate and remove inherent latency from any MSA-compliant 10GbE XFP transceivers, including unsupported transceivers.		
Transmit line clock adjust-	Ability to adjust the parts per million (ppm) line frequency over a range of:		
ment	<ul> <li>LAN mode: -105 to +105 ppm<sup>3</sup></li> <li>WAN mode: -30 to +30 ppm</li> </ul>		
IPv4, IPv6, UDP, TCP	Hardware checksum generation and verification.		

Feature	Extra Performance	Reduced Performance
Frame length controls	Fixed, random, weighted random, or increment by user- defined step, random, weighted random.	
Operating temp. range	41°F to 95°F (5°C to 35°C), ambient air <sup>4</sup>	

<sup>1</sup>XM12 High Performance chassis (941-0009) is required for 80 or more ports of 10 GbE NGY XFP or SFP+ 8-port, load modules to be installed in a single chassis. A field replaceable power supply upgrade kit (943-0005) is available for the XM12 chassis (941-0002) to convert it to the high-performance version. Up to ten 8-port NGY 10GBASE-T full performance load modules are supported in an XM12 High Performance chassis, and up to eight 8-port NGY 10GBASE-T full performance load modules are supported in a standard XM12 chassis). The XM2 chassis (941-0003) supports up to twelve ports of 10GBASE-T full performance load modules.

<sup>2</sup>The LSM10GXM8XP, LSM10GXM8S, and LSM10GXM8GBT use a high performance 800MHz processor with additional layer 2 cache.

<sup>3</sup>For 10GBASE-T interfaces on NGY the ppm does change the data rate, but does not change the bit period due to phy chip limitations.

<sup>4</sup>When an NGY load module is installed in an XM12 or XM2 chassis, the maximum operating temperature of the chassis is 35°C (ambient air).

#### **Port LEDs**

The NGY 10GBASE-T load module has only 2 port LEDs:

- Rx/Error: Same as Rx/Error in the following table
- Tx/Link: Combines the Link and Tx/Pause functions. Solid green = link; blinking green = transmit; red = flow control.

Each 10GB port incorporates a set of LEDs, as described in the following figure.

#### 10GE LSM Port LEDs

LED Label	Usage	
Link	Green if Ethernet link is up (established) or the port is in a forced Link Up state, red if link is down. Link may be down due to no signal or no PCS lock.	
	Green while data is transmitted. Red while flow control frames are received. Off if no traffic is passing in either direction.	
Tx/Pause	For NGY load modules LSM10GXM(R)8 and LSM10GXM(R)4: green indicates that Tx is active and frames being sent; red indicates Tx is paused; off indicates Tx is not active.	
	Green while data is received. Red on any Ethernet error. Off if no frames are received.	
Rx/Error	For NGY load modules LSM10GXM(R)8 and LSM10GXM(R)4: green indicates valid Rx frames are being received; red indicates error frames being received; off indicates no	

LED Label	Usage		
	frames being received.		
LASER ON	Green when the port's laser is turned on. Off otherwise.		
Detect	Green when valid plug in module is detected, red otherwise.		
Power	Green when power is on, red if power fault occurs.		
Option1/2	N/A		
Trigger	See <u>Trigger Out Values.</u>		

### **Clock In/Out**

The load module provides coaxial connectors for clock input and clock output to allow the DUT to phase-lock with the interface. When running off an external clock, the clock input signal must meet the requirements listed in the following figure to ensure proper performance of the load module.

The clock in/out electrical interface parameters are also defined in the following figure.

Clock In/Out Electrical Interface Parameters

Parameter		Characteristic	
ClockInput	Frequency	156.25 MHz ±100ppm	
	Duty cycle	50%	
	Jitter	±150ps max. cycle to cycle, >1kHz	
		Recommended: 800mV	
	Amplitude	Minimum: 150mV	
		Maximum: 1200mV	
	Impedance	50 ohm ± 5%, DC coupled	
	Connector	Female SMA	
ClockOutput	Frequency	156.25MHz +/-105PPM (Programmable PPM in Internal Clock Mode) and variations: 156.25MHz (LAN) or 155.52MHz (WAN) +/-30PPM (Programmable PPM in Internal Clock Mode)	
	Duty cycle	40 to 60%	
	Jitter	20ps max cycle to cycle, >1kHz	
	Amplitude	0.7Vpp min into 50 ohms, AC coupled output	
	Edge rates	200ps to 340ps (20% to 80%) into 50 Ohms	
	Impedance	50 ohms +/-5%, AC coupled	
	Connector	Female SMA	

The load module contains a phase-locked loop (PLL) that reduces the jitter of the input clock, either from the internal or external clock source. The bandwidth of the PLL is approximately 1 kHz.

## **Trigger Out Values**

The signals and LEDs available on the trigger out pins for these cards are described in the following table.

10GE LAN Trigger Out Signals

Pin/LED	Value	
Trigger Out	Single ended output that pulses high for approximately 1.18s shortly after the Central FPGA is loaded, and following an event defined by UDS1.	
	Voltage output = 3.3V for high, 0V for low.	
Trigger LED	Pulses following an event defined by UDS1.	

#### **Removable Carrier Cards**

The 10GE10G1-01 load modules has removable carrier cards available for use:

- The XENPAK-ADAP-01 carrier card for XENPAK transceivers, shown in the figure XENPAK-ADAP-01 Carrier Card.
- The XFP-ADAP-02 LAN/WAN carrier card for XFP transceivers (shown being inserted into the LSM load module in the figure XFP-ADAP-02 Carrier Card.
- X2 carrier card for X2 Transceiver (shown with transceiver installed in the figure Carrier Card with X2 Transceiver).
- 10GBase-T-ADAP-01 10 Gigabit Ethernet adapter module (shown in the figure -10GBase-T Adapter Module)

Figure: XENPAK-ADAP-01 Carrier Card



Figure: Carrier Card with X2 Transceiver



Figure: XFP-ADAP-02 Carrier Card



Figure: 10GBase-T Adapter Module



#### **Carrier Card Installation**

To install the carrier card, do the following:

- 1. Insert the card into the opening in the 10GE LSM module.
- 2. Slide the card along the guide rails until it connects to the load module.
- 3. Tighten the screws so that the carrier card is firmly in place. Do not over tighten the screws (no more than a quarter turn once flush with the card front).

The carrier card can be installed either before or after the load module is connected to the chassis. It is best not to attach the transceiver to the carrier card until the card is installed in the load module. Load modules should be screwed down in the chassis before removing or installing a carrier card, to prevent from accidentally dislodging a load module from the chassis backplane.

NOTE

The carrier cards do not come with the required transceivers. They must be purchased separately.

### **XENPAK/XAUI Connectors**

The LSM10G1-01 load module has XAUI and XENPAK connectors available. See <u>XAUI Connectors</u> and <u>XENPAK Connectors</u> above for more information on XENPAK connectors.

These connectors are only applicable when the XENPAK carrier is being used.

#### **Statistics**

Statistics for 10GE LSM cards (except NGY), under various modes of operation may be found in <u>Statistics for 10GE LSM Modules (except NGY)</u>. Statistics for NGY load modules may be found in <u>Statistics for NGY Modules</u>.

# **NGY Fault Handling**

### **IEEE Requirements**

IEEE 802.3ae, section 46.3.4 defines how a Reconciliation Sublayer (RS) shall respond to Local and Remote Faults. Response to a Local Fault is to immediately cease sending traffic on the transmit data path (even if doing so truncates a frame) and to send continual Remote Faults. Response to a Remote Fault is to stop sending MAC data (completing any frame that is being transmitted) and to send continual idles.

# **NGY Operation**

NGY load modules have a single statistic for Faults called Link Fault State. This statistic is real-time and indicates the current state of the port's Reconciliation Sublayer (RS) state machine. The possible statistics values are:

- No Fault
- Local Fault
- Remote Fault

### Features that force deviation from IEEE spec

NOTE

In general, if a NGY port appears to be transmitting according to the Frames Sent statistic, be aware that Link Fault State may override this.

#### Tx Ignores Rx Link Faults

This feature is enabled through the **Link Fault Signaling** tab of Port Properties. When the feature is enabled, the Fault statistic continues to indicate the RS state of the port; however, the transmit-side response behaves as if no fault was received. That is to say, Remote Faults are not sent as a response to Local Fault and Idles are not forced as a response to Remote Fault, even though Link Fault State indicates the board is in a Fault state.

#### **Transmit Ignores Link Status**

This feature is enabled through the Transmit Modes tab of Port Properties. When the feature is enabled, a port is permitted to transmit under conditions that would normally inhibit transmit. For instance, a port that has no link and is not in diagnostic loopback appears in IxExplorer as red color, and is normally not permitted to transmit. Enabling this feature allows transmit. When the feature is enabled, the statistic called Link State indicates `Ignore Link'.

Note that if the port is in Fault, enabling this feature and forcing transmit may result in misleading results. The port shown in the following stat view (See the following figure) is ignoring link (see Link State statistic), is in Remote Fault (see Link Fault State statistic), yet appears to be transmitting (see Frames Sent Rate statistic). The reality is that no frames are actually leaving the port because the port is in Remote Fault. This is because the block that maintains the transmit statistics is located before the block that forces idles as a response to Remote Fault.

Figure: Statistic View for NGY, Ignore Link Status

6	A	В
1	Name	loopback:02.01
2	Link State	lgnore Link
3	Line Speed	10GE LAN
4	Frames Sent	164,624,279
5	Frames Sent Rate	14,880,954
6	Valid Frames Received	0
7	Valid Frames Received Rate	0
8	Bytes Sent	10,535,953,80
9	Bytes Sent Rate	952,380,945
10	Bytes Received	0
11	Bytes Received Rate	0
12	Fragments	0
13	Undersize	0
14	Oversize	0
15	CRC Errors	0
16	Link Fault State	Remote Fault
17	Scheduled Transmit Duration	0 : 0: 0.0
18	Bytes Sent / Transmit Duration	21,740,528
19	Bits Sent	84,287,630,43
20	Bits Sent Rate	7,619,047,560
21	Bits Received	0
22	Bits Received Rate	0
23	Central Chip Temperature(C)	45
24	Port Chip Temperature(C)	45
25	Port CPU Status	Ready
26	Port CPU DoD Status	Ready

### **Intrinsic Latency Adjustment**

This option, when present and enabled, reduces the measured latency by the amount of latency that is induced by the test equipment itself (not the DUT). For a specific transceiver, the system retrieves its pre-determined latency value and subtracts this from the measured overall latency. For an `unknown' transceiver (not previously measured), it calculates and stores the intrinsic latency value.

On the **General** tab in **Port Properties**, the **Latency Calibration** option is only enabled for cards with transceivers that have not been pre-measured for intrinisic latency by Ixia. The **Latency Calibration** option is grayed-out if any one of the following conditions are present:

- There is no carrier.
- There is no transceiver.
- The transceiver is XFP or XAUI (which do not need to be calibrated).
- The transceiver is XENPAK or X2 and a value is found for it in the list of pre-calibrated values.

The **Latency Calibration** option is enabled if the transceiver is XENPAK or X2 but no precalibrated value is found in the stored list. The **Latency Calibration** option is also enabled for transceivers that you have previously calibrated, so that the calibration measurement may be repeated (if desired).

Clicking the **Latency Calibration** option runs a Tcl script that measures intrinsic latency and stores the value in an .xml file. The .xml file contains the values that you have

produced and saved. Each value is identified for a specific transceiver (per manufacturer, model, and serial number). You can run the calibrate process repeatedly with the same transceiver (if desired). Each new measurement overwrites the previous one for that transceiver.

Running the calibration measurement puts the port into a special loopback mode to measure intrinsic latency. When done, the port is put back into default normal mode. Any port configuration you have set before calibrating intrinsic latency, is lost as the port reverts to a default configuration.

The **Enable** check box is grayed out when no value exists in the system for the specific transceiver. If a value exists (in the .xml file) then the **Enable** check box is available. Select the check box to enable the intrinsic latency adjustment.

After the intrinsic latency adjustment has been done, you may want to refresh the chassis or close and reopen the Port Properties dialog.



The LSM10GMS-01 load module always compensates for intrinsic latency it is not optional. Also, this load module does not support the 'No CRC' option. Any imported stream with No CRC enabled is Forced Valid to `Bad CRC'.

# **XAUI Family**

#### **Part Numbers**

The XAUI family part numbers are shown in the following table.

10GE XAUI Load Modules

Load Module	Part Num- ber	Description
LM10GEXAUI	LM10GE500F1	10GBASE (XAUI), 1 port
LM10GEXAUI+BERT	LM10GE500F1B	10GBASE (XAUI), Ethernet/BERT, 1 port
LM10GEXAUI BERT only	LM10GE500M1B	10GBASE (XAUI), BERT, 1 port
Cables	CAB10GE500S1	XAUI cable, 20 inch, standard pinout
	CAB10GE500S2	XAUI cable, 40 inch, standard pinout
	BOB10GE500	XAUI SMA break-out box
	CON10GE500	XAUI Fujitsu MicroGiGa connector
	LPG10GE500	XAUI front panel loopback connector

# **Specifications**

The limitations of -M, Layer 2/3 and Layer 7 cards are discussed in Ixia Load Modules.

10GB XAUI Load Module Specifications

	10GBASE (XAUI)	10GBASE (XAUI/BERT)
# ports	1	1
-M Card Available	N	N
Layer2/Layer3 Card Available?	N	N
Layer 7 Card Available	N	N
Data Rate	10GB	N/A
Connector/Frequency-Mode	See XAUI Connectors	See XAUI Connectors.
Capture buffer size	32MB	N/A
Captured packet size	24-65,000 bytes	N/A
Streams per port	255	N/A
Advanced streams	160	N/A
Preamble size: min-max	8	N/A
Frame size: min-max	24-65,000	N/A
Inter-frame gap: min-max	4.0ns - 42sec in 3.2ns steps	N/A
Inter-burst gap: min-max	4.0ns - 42sec in 10.0ns steps	N/A
Inter-stream gap: min-max	4.0ns - 42sec in 10.0ns steps	N/A
Normal stream frame rate	0.023fps - full line rate	
Advanced stream min frame rate 1	Slow: 0.023fpsMed: 95fpsFast: 1525fps	
Latency	20ns resolution	N/A

\_Streams are divided up into three categories: 144 slow speed streams, 8 medium streams and 8 fast streams.

XAUI accessories are discussed in <u>Appendix A, XAUI Connector Specifications</u>.

#### **Port LEDs**

Each 10GB XAUI port incorporates a set of LEDs, as described in the following table.

10GE XAUI Port LEDs

LED Label	Usage
Link	Green if Ethernet link has been established, red otherwise. Link may be

LED Label	Usage
	down due to no signal or no PCS lock.
Tx/Pause	Green while data is transmitted. Red while flow control frames are received. Off if no traffic is passing in either direction.
Rx/Error	Green while data is received. Red on any Ethernet error. Off if no frames are received.
Trigger	See below.
Option	Reserved for future use.
LASER ON	Green when the port's laser is turned on. Off otherwise.

### **Trigger Out Values**

The signals and LEDs available on the trigger out pins for these cards are described in the following table.

10GE XAUI Trigger Out Signals

Pin/LED	Value
Trigger Out A	Low (0V) on Rx Pause Request, high (+5V) otherwise.
Trigger Out B	Low (0V) on User Defined Statistic 1 true, high (+5v) otherwise.
Trigger LED	Pulses each time a Pause Request is detected.

# **Clock In/Out**

The XAUI load module provides SMA coaxial connectors for clock input and clock output to allow the DUT to phase-lock with the XAUI interface. When running off an external clock, the clock input signal must meet the requirements listed in the following table to ensure proper performance of the load module.

XAUI Reference Clock Input Requirements

Parameter	Characteristic
Frequency	156.25 MHz ±100ppm
Jitter	±150ps max. cycle to cycle, >1kHz
Amplitude	0.9 Vpp minimum, into 50 $\Omega$
Duty cycle	40 to 60%
Edge rates	600ps maximum, into 50

Parameter	Characteristic
(20% to 80%)	Ω

The clock in/out electrical interface parameters are defined in the following table.

XAUI Clock In/Out Electrical Interface Parameters

Parameter		Characteristic
Clock Input	Connector	Female SMA
	Impedance	50 ohm ± 5%, DC coupled
	Absolute max input	6V (DC plus half AC peak-to-peak
	Connector	Female SMA
	Impedance	50 ohm ± 5%, AC coupled
	Amplitude	0.9 Vpp minimum, into 50 $\Omega$ . (1.5 Vpp typical)
Clock Output	Edge rates	200ps to 340ps (20% to 80%) into 50Ω
	Duty cycle	45% to 55%
	Jitter	20ps max cycle to cycle, >1kHz
	Frequency	156.25 MHz ±20ppm (internal clock mode)

The load module contains a phase-locked loop (PLL) that reduces the jitter of the input clock, either from the internal or external clock source. The bandwidth of the PLL is approximately 1kHz.

#### **XAUI Connectors**

The following connectors and adapters are available for the XAUI Load Modules and are discussed in <a href="Appendix A">Appendix A</a>, XAUI Connector Specifications.

- <u>Standard Connector Specifications</u>: the signals carried on the Load Module's XAUI connector.
- <u>Front Panel Loopback Connector</u>: a connector used to loopback XAUI signals at the external connector.
- Standard Cable Specification: the CAB10GE500S1 (20 inch) and CAB10GE500S2 (40

inch) cables.

• SMA Break-Out Box: the BOB10GE500 SMA break-out box.

#### **MDIO**

A Management Data Input/Output (MDIO) interface is provided to you. The Ixia Load Module acts as the Station Management entity (STA), and can control one or more MDIO Manageable Devices (MMD) in the users system. Multiple MMDs can be attached to the interface. You can set/read the MDIO control/status registers inside a MMD through a graphical user interface.

The connector used for the MDIO interface is a 15-pin female D-sub and provides with the ability to add up to two external Mii interfaces compliant to either 802.3 clause 22 or 802.3ae clause 45. The connector pin assignments, Mii Interface, signal names, and functional descriptions are listed in the following table.

MDC/MDIO Connector Pin Assignments

Pin No.	Mii Interface	Signal Name	Functional Descriptin
1	External 2	DIR	Data direction control.
2	External 2	MDC	Clock.
3	External 2	MDIO	Bi-directional data.
4	External 2	+5V	+5Vdc supply.
5	External 1	+5V	+5Vdc supply.
6	External 1	MDIO	Bi-directional data.
7	External 1	MDC	Clock.
8	External 1	DIR	Data direction control.
9-15	GND	GND	Ground

Figure: MDC/MDIO D-sub Connector Pin Assignments

NOTE

The MDIO on the Ixia XAUI Load Module is 3.3V while the Ixia XENPAK Load Module, when used with the adapter for XAUI, is 1.2V. The reason for the difference is that the XENPAK MSA requires 1.2V for MDIO whereas most XAUI SerDes chips require 3.3V (LVTTL). Therefore, when using the XAUI Load Module to test a XENPAK transceiver or SerDes, which require 1.2V, a level shifter is needed to convert 3.3V to 1.2V.

The MDIO/MDC interface has a clock line (MDC) and bi-directional data line (MDIO) as defined in IEEE 802.3ae. In addition to these, a +5Vdc supply, and data direction control line (DIR) are provided to make interfacing easier for you. The +5Vdc output is intended to power buffers and/or optocouplers at the user-end of the cable. This supply can be turned ON or OFF under software control through the GUI.

The +5Vdc supply is OFF when the chassis is initially powered-up, or following a reset.

For more information on XAUI connectors, see Appendix A, XAUI Connector Specifications.

#### **Statistics**

Statistics for 10GB cards, under various modes of operation may be found in <u>Statistics for 10GE Modules with BERT</u> and <u>Statistics for 10G UNIPHY Modules with BERT</u>.

# **XENPAK Family**

The LM10GE700P3 family is referred to as the XENPAK load modules. Each card accepts a XENPAK transceiver, or with an appropriate carrier card accepts an XPAK or X2 transceiver. Five variants are available, which feature Ethernet and/or BERT modes and full or manufacturing mode.

### **Part Numbers**

The XENPAK family part numbers are shown in the following table.

10GE XENPAK Modules

Load Module	Part Num- ber	Description
Transceivers	XENPAK-LR	XENPAK Transceiver - 1310nm LAN, 10GBASE-LR
	XENPAK-SR	XENPAK Transceiver - 850nm LAN, 10GBASE-SR
	XENPAK-ER	XENPAK Transceiver - 1550nm LAN, 10GBASE-ER
	XENPAK-CX4	XENPAK Transceiver - CX4 Interface (10GBASE-CX4)
Cables	CAB10GE-CX4	CX4-to-CX4 cable, 1 meter
	CX410GE500	CX4 to XENPAK adapter
	FXN10GE500	XAUI Fujitsu to XENPAK Adapter

# **Specifications**

The limitations of -M, Layer 2/3 and Layer 7 cards are discussed in Ixia Load Modules.

10GB Load Module Specifications Part 3

# ports 1

-M Card Available Y

Layer2/Layer3 Card Available?

N

Layer 7 Card Avail-

Available?	N
Layer 7 Card Avail- able	N
Data Rate	10GB
Connector/Frequency- Mode	See XENPAK Connectors
Capture buffer size	32MB
Captured packet size	24-65,000 bytes
Streams per port	255, 32 (-M ver- sion)
Advanced streams	160
Preamble size: min-	8

	10GBASE (XENPAK)
max	
Frame size: min-max	24-65,000
Inter-frame gap: min- max	4.0ns - 42sec in 3.2ns steps
Inter-burst gap: min- max	4.0ns - 42sec in 10.0ns steps
Inter-stream gap:min-max	4.0ns - 42sec in 10.0ns steps
Normal stream frame rate	0.023fps - full line rate
Advanced stream min frame rate	Slow: 0.023fpsMed: 95fpsFast: 1525fps
Latency	20ns resolution

<sup>1</sup>Streams are divided up into three categories: 144 slow speed streams, 8 medium streams and 8 fast streams.

The -M load modules includes all of the features of the non-M board with the following exceptions:

- No support for routing protocols
- No real-time latency, but timestamps are included
- 32 streams in packet stream mode
- 16 streams in advanced scheduler mode
- No configurable preamble

When performing sequence checking, no more than 8192 packet group IDs should be used.

#### **Port LEDs**

Each 10GB port incorporates a set of LEDs, as described in the following tables.

10GE XENPAK Port LEDs

LED Label	Usage
Link	Green if Ethernet link has been established, red otherwise. Link may be down due to no signal or no PCS lock.
Tx/Pause	Green while data is transmitted. Red while flow control frames are received. Off if no traffic is passing in either direction.
Rx/Error	Green while data is received. Red on any Ethernet error. Off if no frames are received.

LED Label	Usage
Trigger	See below.
LASER ON	Green when the port's laser is turned on. Off otherwise.

## **Trigger Out Values**

Trigger out values depend on the particular board type.

#### **XENPAK Load Modules**

The signals and LEDs available on the trigger out pins for these cards are described in the following table.

10GE XENPAK 1-Slot Trigger Out Signals

Pin/LED	Value
Trigger Out A	Low (0V) on Rx Pause Request, high (+5V) otherwise.
Trigger Out B	Low (0V) on User Defined Statistic 1 true, high (+5v) otherwise.
Trigger LED	Pulses each time a Pause Request is detected.

### **Clock In/Out**

The load module provides SMA coaxial connectors for clock input and clock output to allow the DUT to phase-lock with the interface. When running off an external clock, the clock input signal must meet the requirements listed in the following table to ensure proper performance of the load module.

Reference Clock Input Requirements

Parameter	Characteristic
Frequency	156.25 MHz ±100ppm
Jitter	±150ps max. cycle to cycle, >1kHz
Amplitude	0.9 Vpp minimum, into 50 $\Omega$
Duty cycle	40 to 60%
Edge rates (20% to 80%)	600ps maximum, into 50 $\Omega$

The clock in/out electrical interface parameters are defined in the following table.

Clock In/Out Electrical Interface Parameters

Parameter		Characteristic
	Connector	Female SMA
Clock Input	Impedance	50 ohm ± 5%, DC coupled
	Absolute max input	6V (DC plus half AC peak-to-peak
	Connector	Female SMA
	Impedance	50 ohm ± 5%, AC coupled
	Amplitude	0.9 Vpp minimum, into 50 $\Omega$ . (1.5 Vpp typical)
Clock Out- put	Edge rates	200ps to 340ps (20% to 80%) into 50Ω
	Duty cycle	45% to 55%
	Jitter	20ps max cycle to cycle, >1kHz
	Frequency	156.25 MHz ±20ppm (internal clock mode)

The load module contains a phase-locked loop (PLL) that reduces the jitter of the input clock, either from the internal or external clock source. The bandwidth of the PLL is approximately 1kHz.

#### **XENPAK Connectors**

### **Power Sequencing Specification**

The Xenpak 2.1 MSA does not specify any particular power sequencing for the various Xenpak power supply rails (3.3V, 5V, and APS).

When Xenpak Power is enabled, power sequencing is as follows:

- The 5V rail comes up first, with a ramp-up time of approximately 2.25 ms.
- The 3.3V and APS rails both start to come up about 500 us after 5V rail is up.
  - The 3.3V supply has a ramp-up time of approximately two milliseconds.
  - The APS supply ramp-up time varies, according to level required by APS Set resistor, but will be no more than two milliseconds. When no Xenpak module is inserted into the Load Module, APS voltage is less than 150 mV.

#### Reset

Hardware asserts a Reset by bringing Xenpak connector pin 10 low whenever either of the following conditions is true:

- The Xenpak module is not inserted into the load module; that is, Xenpak pin 14 is high.
- Xenpak power is turned off.

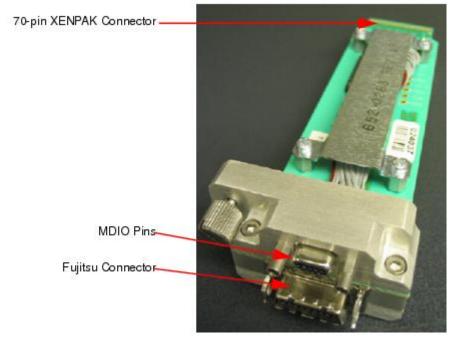
The hardware continues to assert Reset until both of these items are false. Once Xenpak Power is asserted, or if a Xenpak is hot-plugged, the system waits 5 seconds for Xenpak initialization (per MSA 2.1). Reset is then de-asserted, and the system waits an additional 500 ms for any vendor-based reset management to complete initialization. After this final

500 ms delay, the load module assumes the Xenpak module is ready for MII access or to transmit and receive.

## **XAUI Fujitsu to XENPAK Adapter**

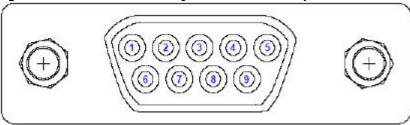
The XAUI Fujitsu to XENPAK Adapter (P/N FXN10GE500) is shown in the figure below.

Figure: XAUI Fujitsu to XENPAK Adapter



The MDIO pins are pictured and described in the following figure and table below.

Figure: MDIO Pins for XAUI Fujitsu to XENPAK Adapter



MDIO Pin Assignments for XAUI Fujitsu to XENPAK Adapter

Pin	Signal
1	PU-5V
2	PU-3.3V
3	PU-APS
4	LASI (GND)
5	RESET
6	TX ON/OFF
7	MDIO

Pin	Signal
8	MDC
9	GND

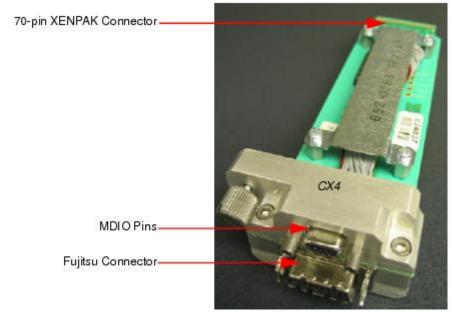
This MDIO pinout is the same for the CX4 to XENPAK adapter (P/N CX410GE500).

For more information on XAUI connectors, see Appendix A, XAUI Connector Specifications.

### **CX4 to XENPAK Adapter**

The CX4 to XENPAK Adapter (P/N CX410GE500) is shown in the following figure.

Figure: CX4 to XENPAK Adapter



The MDIO pins are pictured and described in the figure and table.

For more information on XAUI connectors, see <a href="Appendix A">Appendix A</a>, <a href="XAUI Connector Specifications">XAUI Connector Specifications</a>.

### **Statistics**

Statistics for 10GB cards, under various modes of operation may be found in <u>Statistics for 10GE Modules with BERT and Statistics for 10G UNIPHY Modules with BERT.</u>

# Chapter 23 - IXIA OC12 ATM/POS Load Modules

This chapter provides details about OC12 ATM/POS (LM622MR) load module specifications and features.

The OC12 ATM/POS (LM622MR) load module enables high performance testing of routers and broadband aggregation devices such as DSLAMs and PPP termination systems. The board accommodates pluggable PHYs: The features available for these load modules are included in the *Port Features by Port Type* matrix, which is located on the ixiacom.com website under Support/User Guides/Spreadsheets.

- 1310 nm multimode optics with dual-SC connectors
- Small Form-factor Pluggable (SFP) socket. Ixia offers 1310 nm singlemode and multimode transceivers with LC connectors; others may be purchased independently.

The LM622MR load module is shown in the following figure.

Figure: LM622MR Load Module with Pluggable PHYs Installed



### **Part Numbers**

The currently available part numbers are shown in the following table. Items without a *Price List Names* entry are no longer available.

Currently Available ATM/POS Modules

Load Module	Part Num- ber	Description
LM622MR	LM622MR	2-port ATM/Packet over SONET Load Module. Supports 622 and 155 Mbps data rates. Requires the purchase of 2 PHY modules (OC3OC12PHY or OC3OC12PHY-SFP) and the OPTATMMR and/or OPTPOSMR operational mode option.
LM622MR- 512	LM622MR-512	2-port ATM/Packet over SONET Load Module. Supports 622 and 155 Mbps data rates. Requires the purchase of 2 PHY modules (OC3OC12PHY or OC3OC12PHY-SFP) and the

Load Module	Part Num- ber	Description
		OPTATMMR and/or OPTPOSMR operational mode option.
	OPTATMMR	ATM operational mode option for LM622MR.
	OPTPOSMR	OC12c/OC3c Packet over SONET (POS) operational mode option for LM622MR.
	OC3OC12PHY	Single-port OC-3/OC-12 PHY module for the ATM/Packet over SONET Load Module. 1310 nm multimode optics with dual SC connectors.
	OC3OC12PHY- SFP	Single-port OC-3/OC-12 PHY module for the ATM/Packet over SONET Load Module. Requires one SFP pluggable transceiver (not included).
	SFP- OC12MM1310D	Multirate (OC-3, OC-12) SFP transceiver. 1310 nm, multimode with dual LC connectors. Supports diagnostic features.
	SFP- OC12SM1310D	Multirate (OC-3, OC-12) SFP transceiver. 1310 nm, single mode with dual LC connectors. Supports diagnostic features.

# **OC12 POS 622 Specifications**

The OC12c POS specifications for the LM622MR load module are contained in the following table.

OC12c POS Specifications for LM622MR Load Module

	LM622MR	L M 6 2 2 M R - 5 1 2
# ports	2	2
Data Rate	1-100% of OC12/OC3 speeds	1-100% of OC12/OC3 speeds
	Changeable physical interface (PHY) per port:	Changeable physical interface (PHY) per port:
Connector	<ul> <li>SC connectors for 1310 nm multimode</li> <li>SFP socket for SFP-LC module</li> <li>PHY clock-in and clock-out:</li> <li>SMA connectors.</li> </ul>	<ul> <li>SC connectors for 1310 nm multimode</li> <li>SFP socket for SFP-LC module</li> <li>PHY clock-in and clock-out:</li> <li>SMA connectors.</li> </ul>
CPCU RAM	256	512
Capture buffer size	8 MB	8 MB
Captured packet	34 - 65535 bytes	34 - 65535 bytes

	L M 6 2 2 M R	LM622MR-512
size		
Streams per port	255 Packet Streams	255 Packet Streams
Advanced streams	160	160
Frame size: min- max	35 - 65536 bytes (at full line rate)12 - 65536 bytes (otherwise)	35 - 65536 bytes (at full line rate)12 - 65536 bytes (otherwise)
Inter-frame gap: min-max	1 μs - 4.294967 secs	1 μs - 4.294967 secs
Inter-burst gap: min-max	1 μs - 4.294967 secs	1 μs - 4.294967 secs
Inter-stream gap: min-max	1 μs - 4.294967 secs	1 μs - 4.294967 secs
Latency	20 ns resolutionMinimum frame size of 33 bytes is required.	20 ns resolutionMinimum frame size of 33 bytes is required.

# **ATM Specifications**

The ATM load module specifications for the LM622MR are contained in the following table.

ATM Load Module Specifications

	LM622MR/LM622MR-512
# ports	2
Data Rate	0-100% of OC-12/OC-3 speeds
Connector	Changeable physical interface (PHY) per port:  • SC connectors for 1310 nm multimode  • SFP socket for SFP-LC module  PHY clock-in and clock-out:  • SMA connectors.
Capture buffer size	8 MB
Captured packet size	49 - 64K bytes (Note 1)
Streams per port	4096 shared by 15 interleaved transmit engines
Frame size: min- max	40 - 65,536 bytes (Note 1)
Latency	20 ns resolution

(Note 1) ATM ports transmits a packet of 65568 bytes, including the header. The receive buffer, however, is restricted to 65536 bytes. The last 32 bytes of a maximum size packet is not visible in the capture buffer.

ATM related specifications are detailed in the following table.

ATM Specifications

Parameter	Specification
Encapsulation	<ul> <li>LLC/SNAP Routed Protocol</li> <li>LLC/NLPID Routed Protocol</li> <li>LLC Bridged Ethernet/802.3</li> <li>LLC Bridged Ethernet/802.3 without FCS</li> <li>LLC Encapsulated PPP</li> <li>VC Mux Routed Protocol</li> <li>VC Mux Bridged Ethernet/802.3</li> <li>VC Mux Bridged Ethernet/802.3 without FCS</li> <li>VC Multiplexed PPP</li> </ul>
Virtual Circuits 65,536 VC ids distributed among 4,096 unique streams	
Cell Header Format	UNI or NNI per port
ATM Framing	AAL5, Constant Bit Rate (CBR) or Unspecified Bit Rate (UBR)

## **Physical Interfaces**

Two pluggable physical interfaces are available for the ATM card:

• **OC3OC12PHY**: Single OC3/OC12 port module. 1310 nm multimode optics with dual-SC connectors. This module is shown in the following figure. The optical characteristics are expressed in the table below.

Figure: OC3OC12PHY Physical Interface



OC3OC12PHY Optical Specifications

Trans- mitter/Receiver	Spe- cification	OC12/O- C3 Mul- timode
Transmitter	Fiber	62.5um fiber
	Waveleng- th	1270nm - 1380nm
	Mean Launched Power	-20dBm to - 14dBm
	Minimum Extinction Ratio	10dB
	Safety	LED based
Receiver	Fiber	62.5um fiber
	Waveleng- th	1100nm - 1600 nm
	Minimum Sens-	-26dBm

Trans- mitter/Receiver	Spe- cification	OC12/O- C3 Mul- timode
	itivity (OC12)	
	Minimum Sens- itivity (OC3)	-30dBm
	Minimum Overload	-14dBm

- **OC3OC12PHY-SFP**: Single OC3/OC12 port module. The PHY accommodates a SFP transceiver, which is not included with this part. Ixia offers two transceivers:
  - SFP-OC12MM1310D: 1310nm multimode transceiver
  - SFP-OC12SM1310D: 1310nm singlemode transceiver
    The following figure shows an OC3OC12PHY-SFP with a transceiver partially inserted.





The optical characteristics for the two available transceivers are expressed in the following table.

SFP-OC12xx1310 Optical Specifications

Specification	SFP-OC12MM1310D (62.5um fiber)	SFP-OC12SM1310D (short reach)
Transmit Center Wavelength Min/Max	1270 nm/1380 nm	1260 nm/1360 nm
Mean Launched Power Min/Max	-20 dBm/-14 dBm	-15 dBm/-8 dBm

Specification	SFP-OC12MM1310D (62.5um fiber)	SFP-OC12SM1310D (short reach)
Minimum Extinction Ratio	10dB	8.2dB
Safety	LED based	Laser based
Receive Wavelength	1100nm - 1600nm	1100nm - 1600nm
Minimum Sensitivity (OC12)	-26dBm	-23dBm
Minimum Sensitivity (OC3)	-30dBm	-8dBm
Minimum Overload	-14dBm	
Dispersion (OC12)		13ps/nm
Dispersion (OC3)		18ps/nm

The clock-in/clock-out signal characteristics on both PHYs are described in the following tables.

Clock Input Electrical Interface Parameters

Parameter	Characteristic
Connector	Female SMA
Impedance	50 ohm ± 5%, AC coupled
Absolute max input	6V (DC plus half AC peak-to-peak)
Frequency (OC12)	77.76 MHz
Frequency tolerance	+/- 20ppm
Duty Cycle	40/60% of UI
Jitter lim- its	(12kHz to 5MHz) 12 ps rms

Clock Output Electrical Interface Parameters

Parameter	Characteristic
Connector	Female SMA
Impedance	50 ohm ± 5%, AC coupled
Amplitude	1.3 Vpp minimum, into 50 $\Omega$ . (1.5 Vpp typical)
Edge rates	200ps to 340ps (20% to 80%) into 50Ω
Duty cycle	45% to 55%
Jitter	20ps max cycle to cycle, >1kHz
Frequency (OC12)	77.76 MHz (internal clock mode)
Frequency (OC3)	19.44 MHz (internal clock mode)

### **Port LEDs**

Each OC12c/OC3c port incorporates a set of 6 LEDs, as described in the following table.

LMOC12c Port LEDs

LED Label	Usage
LOS	Red during Loss of Signal and green otherwise.
LOF	Red during Loss of Frame and green otherwise.
Tx	Green while data is transmitted and blank otherwise.
Rx	Green while data is received and blank otherwise.
Err	Red on any receive error and blank otherwise.
Trig	Blank reserved for future use.

# **Statistics**

Statistics for ATM/POS cards, under various modes of operation, may be found in <u>Statistics</u> for ATM Modules.

# Chapter 24 - IXIA 10/100 Load Modules

This chapter provides details about 10/100 family of load modules specifications and features.

The 10/100 family of load modules implements Ethernet interfaces that may run at 10Mbps or 100Mbps. Different numbers of ports and interfaces are available for the different board types. The features available for these load modules are included in the *Port Features by Port Type* matrix, which is located on the ixiacom.com website under Support/User Guides/Spreadsheets.

One of the family's modules (the LM100TXS8) is shown in the following figure.





### **Part Numbers**

The part numbers are shown in the following table. Items without a *Price List Names* entry are no longer available.

Part Numbers for 10/100 Modules

Load Module	Price List Names	Description
LM100TX8	LM100TX8	8-port 10/100Mbps Ethernet, reduced features; no support for routing protocols, Linux SDK or L4-L7 applications.
LM100TXS8	LM100TXS8	8-port multilayer 10/100Mbps Ethernet

# **Specifications**

The load module specifications are contained in the following table. The limitations of -3, Layer 2/3 and Layer 7 cards are discussed in <a href="Ixia Load Modules">Ixia Load Modules</a>.

10/100 Load Module Specifications

10/100 Load Module Specific	LM100TXS8LM100TX8
# ports	8
-3 Card Available?	N
L2/L3 Card Available?	Y (LM100TX8)
Layer 7 Card Available	N
Data Rate	10/100 Mbps
Connector	RJ-45
Interfaces	100Base-TX10Base-T
Capture buffer size	6MB
Captured packet size	12-13k bytes
Streams per port	255
Flows per port	N/A
Advanced Streams	128
Preamble size: min-max	2-63 bytes
Frame size: min-max	12-13k bytes
Inter-frame gap: min-max	Basic scheduler:  10Mbps: 8000ns-429s in 400ns steps100Mbps: 800ns-42.9s in 40ns steps  Advanced scheduler:  10Mbps: 8000ns-53s in 400ns steps100Mbps: 800ns-5.3s in 40ns steps
Inter-burst gap: min-max	10Mbps: 8000ns-429s in 400ns steps100Mbps: 800ns-42.9s in 40ns steps
Inter-stream gap:min-max	10Mbps: 8000ns-429s in 400ns steps100Mbps: 800ns-42.9s in 40ns steps
Normal stream min frame rate	10: 0.00238fps100: 0.0238fps

	LM100TXS8LM100TX8
Advanced stream min frame rate <sup>3</sup>	10 slow: 0.0186fps10 fast: 9.53 fps100 slow: 0.186fps100 fast: 95.3fps
Latency	20ns resolution

<sup>&</sup>lt;sup>1</sup>AMPLIMITE Subminiature D connector 787170-4.

### **Port LEDs**

Each LM100TXS8 port incorporates a set of 2 LEDs, as described in the following table.

LM100TXS8 Port LEDs

LED	Color	Usage
Tx/L	Orange	10Mbps link. Pulses on activity.
	Green	100Mbps link. Pulses on activity.
RX/E	Orange	Pulses on error.
	Green	Full duplex. Pulse on activity.

All other 10/100 card types incorporate a set of 6 LEDs, as described in the following table.

10/100 Port LEDs

LED Label	Usage
Link	Green if link established. For Mii and RMii boards, Red if no transceiver is detected.
100	Green for 100Mbps.
Half	Green for half duplex operation.
Tx/Coll	Green during data transmission. Red during collisions.
Rx/Err	Green during error free reception. Red if errors received.
Trig	Follows the state of the <i>Trigger Out</i> pin, which is programmed through User Defined Statistic 1.

# **Trigger Out Values**

The signals available on the trigger out pins for all cards in this category are described in the following table. The LM100TXS8 and LM100TX8 cards output 60ns pulses and all other cards output 40ns pulses.

<sup>&</sup>lt;sup>2</sup>AMPLIMITE Subminiature D connector 787170-7.

<sup>&</sup>lt;sup>3</sup>Streams are divided up into tree categories: 112 slow speed streams and 16 fast streams.

10/100 Trigger Out Signals

Pin	Signal
1	Port 1: High pulse for each packet matching User Defined Statistic 1
2	Port 2: High pulse for each packet matching User Defined Statistic 1
3	Port 3: High pulse for each packet matching User Defined Statistic 1
4	Port 4: High pulse for each packet matching User Defined Statistic 1

# **Statistics**

Statistics for 10/100 cards, for various modes of operation may be found in <u>Statistics for 10/100 Cards</u> and <u>Statistics for 10/100 TXS Modules</u>.

# Chapter 25 - IXIA 10GE LAN/WAN and OC 192 POS Load Modules

### **Overview**

Ixia offers three families of load modules that operate in multiple modes, as specified in the following table.

Operating Modes Available for Multimode Cards

Family	OC-192 POS	BERT	10GE WAN	10GE LAN	FEC	VCAT/ Chan- nelized
10G MSM	X		X	X		X
OC-192 Triple Mode	x	X	X			
UNIPHY	X	X	X	X	X	

Full specifications for each family may be found at:

- 10G MSM Family
- OC-192c Triple Mode Family
- UNIPHY Family

# **10G MSM Family**

The 10G MSM load module family consists of a UNIPHY LM Load module which supports SONET and Ethernet at 10G rates. Modes supported on this board include POS, WAN, and LAN. For POS there is additional feature support such as DCC, RPR, and SRP.

The following figure displays the 10G MSM module.

Figure: MSM10G1-02 Load Module



NOTE

Due to power requirements, only one MSM module can be used in a 400T chassis. Other modules can be used with the MSM in the same chassis.

### **Part Numbers**

The MSM family part numbers are shown in the following table.

10G MSM Modules

Load Module	Part Num- ber	Description
MSM10G1- 02	944-0012	10GE OC192 load module, 1-port Multi Services Module, supports 10GE LAN/WAN and optional OC-192c POS (order OPTOC192POS). Full features: supports routing and Linux-based applications. Requires an XFP transceiver. Purchase options include XFP-1310 and XFP-1550.
		Maximum one (1) MSM10G1-02 load module permitted per IXIA 400T chassis.
	945-0005	SW-VCAT-SONET configuration option, SONET Virtual Concatenation (VCAT) Option license per port. Includes support for LCAS and GFP-F protocols. Requires purchase of a supported load module (see 945-0003 MSM2.5G1-01 or 944-0012 MSM10G1-02)
	945-0002	SW-RPRSRP-SONET, OC-48/OC-192 configuration option, SONET RPR and SRP stream generation and protocol support, license per port. Requires purchase of a supported load module (see LMOC192xx, LM10GUxF, LMOC48xx, 945-0003 MSM2.5G1-01, or 944-0012 MSM10G1-02)
	OPTOC192POS	10 Gigabit Ethernet OC-102 POS configuration option for

Load Module	Part Num- ber	Description	
		944-0012 (MSM10G1-02) and LM10GUxx load modules.	

# **Specifications**

10G MSM Load Module Specifications

Circatio	MSM10G1-02
# ports	1
-M Card Available	No
Layer2/Layer3 Card Available?	Yes
Layer 7 Card Available	No
Data Rate	10GB
Connector/Wavelength- Mode	XFP 1310nm or 1550nm Single or pluggable
Capture buffer size	Up to 384 MB
Captured packet size	17-65,535bytes
Streams per port	256
Advanced streams	256
Preamble size: min- max	8
Frame size: min-max (bytes)	17-65,535
Inter-frame gap: min- max <sup>1</sup>	4.0ns - 42sec in 3.2ns steps
Inter-burst gap: min- max	4.0ns - 42sec in 10.0ns steps
Inter-stream gap:min- max	4.0ns - 42sec in 10.0ns steps
Normal stream frame rate	0.023fps - full line rate
Advanced stream min frame rate <sup>2</sup>	Slow: 0.023fpsFast: 1525fps
Latency <sup>3</sup>	20ns resolution

- 1. <sup>3</sup>If sequence checking is enabled, then the number of packet group IDs is limited in this way:
  - i. <sup>3</sup>When Wide Bin Mode (on the Wide Packet Groups page) is **not** enabled = 65536.
  - ii.  $^{3}$ When Wide Bin Mode is enabled = 524288.
- 2. <sup>3</sup>If sequence checking is **not** enabled, then the number of packet group IDs is limited in this way:
  - i. <sup>3</sup>When Wide Bin Mode (on the Wide Packet Groups page) is **not** enabled = 65536.
  - ii.  $^{3}$ When Wide Bin Mode is enabled = 2097152.

### **Port LEDs**

Each 10G MSM port incorporates a set of LEDs, as described in the following table.

### 10G MSM Port LEDs

LED Label	Usage
LASER ON	Green when the port's laser is turned on. Blank otherwise.
Pause	Green when transmit is paused, blank when powered off.
PPP/Link	Green in link up condition, Red in link down condition, blank indicates loopback mode enabled.
Tx	Green if transmit is active and frames are being sent, blank otherwise.
LOS	Green when signal level is good, Red when loss of signal occurs, blank if no transceiver detected.
Option	N/A
Trigger	Green when Trigger A condition occurs, Red for Temperature Fault, blank otherwise.
Error	Red when module in error state (fault condition), blank otherwise.
Rx	Green indicates valid receive frames, Red indicates errored frames received, blank when no frames received.
LOF	Green when valid framing occurs, Red when Loss of Frame occurs.

<sup>&</sup>lt;sup>1</sup>Packet gap size also depends on the stream mode selected, Fixed or Average.

<sup>&</sup>lt;sup>2</sup>Streams are divided up into two categories: 224 slow speed streams and 32 fast streams.

<sup>&</sup>lt;sup>3</sup> When performing latency measurements in POS mode, the following restrictions apply:

 $<sup>^3</sup>$  The minimum frame size should be 80 bytes for latency measurements to be supported at line rate. On the MSM10G, there is only one packet group mode (wide packet groups). Two different scenarios apply:

# **Clock In/Out**

The load module provides coaxial connectors for clock input and clock output to allow the DUT to phase-lock with the interface. When running off an external clock, the clock input signal must meet the requirements listed in the following table to ensure proper performance of the load module.

Clock Input Specifications

Parameter	Characteristic
Connector	SMA
Frequency	SONET: 155.52 MHz ±20ppm
rrequency	10GE: 161.132 MHz ±- 100ppm
Amplitude	1.1 Vpp minimum, into 50 $\Omega$ , AC coupled
Duty cycle	40 to 60%

The clock in/out electrical interface parameters are defined in the following table.

Clock Output Specifications

Parameter	Characteristic
Connector	SMA
Fraguancy	SONET: 155.52 MHz ±20ppm
Frequency	10GE: 161.132 MHz ±- 100ppm
Amplitude	500m Vpp minimum, 600 Vpp typical into 50 $\Omega$
Duty cycle	40 to 60%

The load module contains a phase-locked loop (PLL) that reduces the jitter of the input clock, either from the internal or external clock source. The bandwidth of the PLL is approximately 1kHz.

# **Trigger Out**

The signals and LEDs available on the trigger out pins for these cards are described in the following table.

10G MSM Trigger Out Signals

Pin/LED	Value
Trigger Out	10nS active high pulse on trig- ger
Trigger	Indicates Trigger, Pause

Pin/LED	Value
LED	Frame received in 10GE mode.

### **Statistics**

Statistics for 10G MSM cards, under various modes of operation may be found in <u>Statistics</u> for 10G MSM modules.

# **OC-192c Triple Mode Family**

The OC-192c Triple Mode family of load modules implements Optical Carrier interfaces that run at OC192 speeds. The interface operates in concatenated mode, as opposed to channelized mode. One of the modules in this family (the LMOC192cPOS) is shown in the following figure.

Figure: LMOC192c Load Module



### **Part Numbering**

The OC192 cards come with a number of options. All part numbers are of the form:

LMOC192HTOS or

LMFOC192HTOS

where  $\boldsymbol{H}$  is the hundreds designator,  $\boldsymbol{T}$  is the tens designator,  $\boldsymbol{O}$  is the ones designator, and  $\boldsymbol{S}$  is the suffix.

**LMF** boards have no fiber optic interface. It allows for quick validation of serializer and deserializer designs for WAN Packet over SONET/SDH products operating at the STS-192c/STM-64 level. The LMF interface is a 300 pin MegaArray BERG connector, which is an industry standard MSA interface and is compliant per OIF1999.102.8, SFI-4 specification. A reference clock can be supplied through this interface ranging in frequency from 25 MHz to 622 MHz.

The part numbers for these load modules are shown in the following table. Items without a *Price List Names* entry are no longer available.

Load Module	Part Num- ber	Description
LMOC192cPOS		POS, 1-port, intermediate reach (SR1), 1310nm, singlemode.
		POS, 1-port, intermediate reach, 1310nm, singlemode.

OC-192c Load Modules

Load Module	Part Num- ber	Description
		POS, 1-port, intermediate reach, 1550nm, singlemode.
		POS, 1-port, no optics.
LMOC192cVSRPOS	LMOC192168	POS, 1-port, VSR optics, parallel interface.
LMOC192cBERT		BERT, 1-port, intermediate reach, 1310nm, singlemode.
		BERT, 1-port, intermediate reach, 1550nm, singlemode.
LMOC192cVSR-BERT		BERT, 1-port, VSR optics, parallel interface.
LMOC192cPOS+BERT		POS with BERT, 1-port, intermediate reach, 1310nm, singlemode.
		POS with BERT, 1-port, intermediate reach, 1550nm, singlemode.
LMOC192cVSR-POS+BERT	LMOC192468	POS with BERT, 1-port, VSR optics.
LMOC192cPOS+WAN		POS+WAN, 1-port, intermediate reach, 1310nm, singlemode.
LMOC192cPOS+BERT+WAN		POS+BERT+WAN, 1-port, intermediate reach, 1310nm, singlemode.
		POS+BERT+WAN, 1-port, intermediate reach, 1550nm, singlemode.
LM10GEWAN		10GBASE-LW (WAN), 1-port, 1310nm, singlemode.
		10GBASE-EW (WAN), 1-port, 1550nm, singlemode.
Options	SW- DCCSONET	DCC SONET support.
	945-0002	SW-RPRSONET SW-SRPSONET
	J <del>4</del> J-0002	SRP SONET and RPR SONET support.

# **Specifications**

The load module specifications are contained in the following table. Note that the -M modules are not included in the table; their limitations versus the non-M version are discussed in <a href="Ixia Load Modules">Ixia Load Modules</a>.

OC192 Load Module Specifications

	LMOC192cPOS		
	LMOC192cPOS+- WAN	LMOC192cBE- RT	LMOC192cPOS+B- ERT <sup>1</sup>
# ports	1	1	1
-M Card Available	N	N	N
Layer2/Layer3 Card Available?	N	N	N
Layer 7 Card Available	N	N	N
Data Rate	1-100% of OC192 speeds	N/A	
nector/wawelength-	SC/1310nm or 1550nm Singlemode	SC/1310nm or 1550nm Sin- glemode	SC/1310nm or 1550nm Singlemode
Capture buffer size	32MB	N/A	
Captured packet size	33-64k	N/A	
Streams per port 2	255	N/A	
Flows per port	N/A	N/A	
Advanced streams	160	N/A	
Preamble size: min- max	N/A	N/A	
Frame size: min- max	54-65535	N/A	
Inter-frame gap: min-max	N/A <sup>2</sup>	N/A	
Inter-burst gap:	1us - 42sec	N/A	
Inter-stream gap:	1us - 42sec	N/A	
	0.023fps - full line rate		
Advanced stream frame rate <sup>3</sup> I	Slow: 0.023 - 2083333 fpsMed: 95fps - full line rateFast: 1525fps - full line rate		
Latency 2	20ns resolution	N/A	

The Ixia VSR modules, which were developed in accordance with the OIF Implementation Agreement VSR-1, use twelve parallel multimode fiber optic lines operating at 1.25Gbps per channel, instead of existing 1310nm or 1550nm serial optics. VSR optics are designed to drive signals over distances less than 300 meters, which is sufficient for interconnecting devices within a service provider's Point-of-Presence (POP). Over these short distances, VSR optics offer a significant cost savings compared to intermediate and long-reach serial lasers.

When performing latency measurements, the following restrictions apply:

- If latency is measured with packets that are smaller than 80 bytes, then normal (not wide-packet group) mode should be used and the number of packet group IDs is limited to 1,024.
- If packets are 80 bytes or larger, then wide-packet group mode may be used. Two different scenarios apply when using wide-packet group mode:
  - If sequence checking is enabled, then the number of packet group IDs is limited to 8,192.
  - If sequence checking is not enabled, then the number of packet group IDs is limited to 128k.

### **Port LEDs**

Each OC192c port incorporates a set of 10 LEDs, as described in the following table.

### LMOC192cPOS Port LEDs

LED Label	Usage
LOS	Red during Loss of Signal, Green otherwise.
LOF	Red during Loss of Frame, Green otherwise.
PPP	Green if a PPP link has been established. Red otherwise.
Tx	Green while data is transmitted.
Rx	Green while data is received.
Error	Red on any error.
Trigger	Follows the state of the <i>Trigger Out</i> pin, which is programmed through User Defined Statistic 1.
Option 1	Reserved for future use.
Option 2	Reserved for future use.
LASER ON	Green when the port's laser is turned on.

<sup>&</sup>lt;sup>1</sup>Refer to the LMOC192cPOS and LMOC192cBERT columns for the characteristics of this card when its port is in POS or BERT mode, respectively.

<sup>&</sup>lt;sup>2</sup>The inter-frame gap is indirectly controlled by the frame rate.

<sup>&</sup>lt;sup>3</sup>Streams are divided up into three categories: 144 slow speed streams, 8 medium streams and 8 fast streams.

### **Trigger Out Values**

The signals available on the trigger out pins for all cards in this category are described in the following table.

OC192 Trigger Out Signals

Pin	Signal
Α	Low (0V) on User Defined Statistic 1 true. High (+5V) otherwise.
В	Low (0V) on User Defined Statistic 2 trueHigh (+5V) otherwise.

# **Optical Specifications**

The optical characteristics for the OC192c cards are described in the following table.

LMOC192c Optical Specifications

Specification	OC192c 1310nm	OC192c 1550nm	OC192c VSR-1
Manufacturer	GTRAN	GTRAN	Gore
Average Output Power Min/Max	+1 dBm/+5 dBm	-1 dBm/+2 dBm	-10 dBm/-5 dBm
Transmit Center Wavelength Min/Max	1300 nm/1320 nm	1530 nm/1565 nm	830 nm/860 nm
Receive Center Wavelength Min/Max	1280 nm/1580 nm	1280 nm/1580 nm	830 nm/860 nm
Receive Sensitive Min/Max	-17 dBm/0 dBm	-17 dBm/0 dBm	-16 dBm/-3 dBm
Safety	Class 1 Laser	Class 1 Laser	Class 1 Laser

NOTE

An attenuating should be used when looping back to the same port or when using a short length of cable.

### **Statistics**

Statistics for OC192 cards, under various modes of operation may be found in <u>Statistics for OC192c Modules with BERT.</u>

# **UNIPHY Family**

The UNIPHY family of load modules is based on a universal PHY which allows each port to operate in a number of modes.

### **Part Numbers**

The currently available part numbers are shown in the following table.

UNIPHY Load Modules

Load Mod- ule	Part Num- ber	Description
LM10GUVF	LM10GUVF	10GE Universal Base Load Module with VSR parallel optics, 1-port, 1310nm, singlemode. One or more of OPTOC192POS, or OPTOC192BERT must be purchased.
10G MSM	MSM10G1-02	10G Universal Base Load Module, 1-port, 1550nm, singlemodeP version uses a PowerPC with 256MB processor memory. One or more of OPTOC192POS must be purchased in addition.
Transceivers	XFP-1550	XFP Transceiver, 1550nm
Options	OPTOC192POS	OC-192 POS configuration option for the LM10GU*F.
	OPTOC192BERT	OC-192 BERT configuration option for the LM10GU*F.
	SW-DCCSONET	DCC SONET support for LM10GU*F.
	945-0002	SW-RPRSONET SW-SRPSONET
	713 0002	DCC SONET support for LM10GU*F.

# **Specifications**

The limitations of -M, Layer 2/3 and Layer 7 cards are discussed in <a href="Ixia Load Modules.">Ixia Load Modules</a>.

UNIPHY Load Module Specifications

	10GUEF/UL- F/UPF/UVF (10GEWAN mode)	10GUEF/UL- F/UPF/UVF (10GE LAN mode	10GUEF/UL- F/UPF/UVF (OC192 mode)	10GUEF/UL- F/UPF/UVF (BERT mode) <sup>1</sup>	10GU- EF- FEC <sup>2</sup>
# ports	1	1	1	1	1
-M Card Available	N	N	N	N	N
Lay- er2/Layer3 Card Avail- able?	N	N	N	N	N
Layer 7 Card Avail- able	N	N	N	N	N
Data Rate	1-100% of 10Gbps speeds	10GB	1-100% of OC192 speeds	N/A	1- 100% of

	10GUEF/UL- F/UPF/UVF (10GEWAN mode)	10GUEF/UL- F/UPF/UVF (10GE LAN mode	10GUEF/UL- F/UPF/UVF (OC192 mode)	10GUEF/UL- F/UPF/UVF (BERT mode) <sup>1</sup>	10GU- EF- FEC <sup>2</sup>
					10Gbp- s/OC1- 92 speeds
Con- nec- tor/Wavelen Mode	SC/1310nm or 1550nm Single gth- or pluggable	SC/1310nm or 1550nm Sin- glemode	SC/1310nm or 1550nm Sin- glemode	SC/1310nm or 1550nm Sin- glemode	SC/15- 50nm Sin- glemo- de
Capture buf- fer size	32MB	32MB	32MB	N/A	
Captured packet size	24-65,000 bytes	24-65,000 bytes	33-64k	N/A	
Streams per port	255	255, 32 (-M)	255	N/A	
Advanced streams	160	16016 (-M ver- sion)	160	N/A	
Preamble size: min- max	8	8	N/A	N/A	
Frame size: min- max	24-65,000	24-65,000	54-1600	N/A	
Inter- frame gap: min-max	3/4ns - 43sec in 3.4ns steps	3.2ns - 42sec in 3.2ns steps	N/A	N/A	
Inter-burst gap: min- max	3/4ns - 43sec in 3.4ns steps	3.2ns - 42sec in 3.2ns steps	N/A	N/A	
Inter- stream gap:min- max	3/4ns - 43sec in 3.4ns steps	3.2ns - 42sec in 3.2ns steps	4ns - 42secs	N/A	
Normal stream frame rate	0.023fps - full line rate	0.023fps - full line rate	0.023fps - full line rate	N/A	

	10GUEF/UL- F/UPF/UVF (10GEWAN mode)	10GUEF/UL- F/UPF/UVF (10GE LAN mode	10GUEF/UL- F/UPF/UVF (OC192 mode)	10GUEF/UL- F/UPF/UVF (BERT mode) <sup>1</sup>	10GU- EF- FEC <sup>2</sup>
Advanced stream min frame rate <sup>3</sup>	Slow: 0.023fpsMed: 95fpsFast: 1525fps	Slow: 0.023fpsMed: 95fpsFast: 1525fps	Slow: 0.023fpsMed: 95fpsFast: 1525fps	N/A	
Latency	20ns res- olution	20ns res- olution	20ns res- olution	N/A	

<sup>&</sup>lt;sup>1</sup>Framed BERT only, channelized and unframed BERT are not available.

### **Port LEDs**

Each UNIPHY port incorporates a set of LEDs, as described in the following table.

### UNIPHY Port LEDs

LED Label	Usage
LOS	Red during Loss of Signal. Green when link has been established and no Loss of Signal.
LOF	Red during Loss of Frame. Green when link has been established and no Loss of Signal.
PPP/Link	Green if Ethernet/PPP link has been established. Red otherwise.
Tx	Green while data is transmitted.
Rx	Green while data is received.
Error	Red on any Ethernet error.
Trigger	Green when Trigger is applied.
Pause	Indicates flow control frames have been received.
Option	Reserved for future use.
LASER ON	Green when the port's laser is turned on. Off otherwise.

# **Trigger Out Values**

The signals and LEDs available on the trigger out pins for UNIPHY family load modules are described in the following table.

<sup>&</sup>lt;sup>2</sup>For values not shown, use values from the 10GEWAN/10GELan/OC192 columns according to mode.

<sup>&</sup>lt;sup>3</sup>Streams are divided up into three speed streams: 144 slow, 8 medium and 8 fast. MSM family streams are divided into two speed streams: 224 slow and 32 fast.

10 GE UNIPHY Trigger Out Signals

Pin/LED	Value
Trigger Out A	Low (0V) on User Defined Statistic 1 true, high (+5v) otherwise.
Trigger Out B	Low (0V) on (POS mode) User Defined Statistic 2 true or (Ethernet mode) pause frame detect, high (+5V) otherwise.
Trigger LED	Pulses each time a Pause Request is detected.
Pause/Option1 LED	Pulses each time a Pause Acknowledge is granted.

### **Clock Out Values**

For -XFP suffix load modules, one coaxial connector is provided to allow phase-lock to the DUT. The frequency is either 311.0400 MHz or 322.2656 MHz  $\pm$ 100ppm.

# **Optical Specifications**

The optical characteristics for the UNIPHY cards are described in the following table.

**UNIPHY Optical Specifications** 

Type	Spe- cification	Wavelen- gth	
Trans- mit	Output power (dBm)	1310nm	-6 to -1
		1550nm	-1 to 2
	Distance (km)	1310nm	10
		1550nm	40
	Extinction ratio (dB)	1310nm	6
		1550nm	8.2
Receiv-	Rx Sens- itivity (dBm)	1310nm	-12.6
		1550nm	-14
	Overload (dBm)	1310nm	-1
		1550nm	-1
	Dispersion (ps/nm)	1310nm	40

Type	Spe-	Wavelen-	Val-
	cification	gth	ue
		1550nm	800

### **Statistics**

Statistics for UNIPHY cards, under various modes of operation may be found in <u>Statistics</u> for 10GE Modules with BERT and <u>Statistics</u> for 10G UNIPHY Modules with BERT.

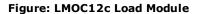


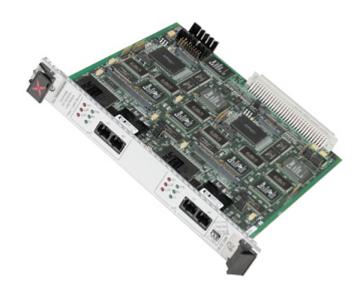
# Chapter 26 - IXIA OC12c/OC3c Load Modules

This chapter provides details about OC12c/OC3c family of load modules specifications and features.

The OC12c/OC3c family of load modules implements Optical Carrier interfaces that may run at OC12 or OC3 speeds. Both interfaces operate in concatenated mode, as opposed to channelized mode. Different numbers of ports and interfaces are available for the different board types. The features available for these load modules are included in the *Port Features by Port Type* matrix, which is located on the ixiacom.com website under Support/User Guides/Spreadsheets.

One of the modules in this family, the LMOC12c, is shown in the following figure.





### **Part Numbers**

The part numbers are shown in the following figure. Items without a *Price List Names* entry are no longer available.

Part Numbers for OC12c/OC3c Modules

Load Module	Price List	Description
LMOC12c/LMOC3c	LMOC12c	2-port multilayer OC12c/OC3c SR-1 POS/SDH, 1310nm multimode
	LMOC12cSM	2-port multilayer OC12c/OC3c SR-1 POS/SDH, 1310nm singlemode

# **Specifications**

The load module specifications are contained in the following table. The limitations of -3, Layer 2/3 and Layer 7 cards are discussed in Ixia Load Modules.

### OC12c/OC3c Load Module Specifications

	LMOC12cLMOC12cSM
# ports	2
-3 Card Available	N
Layer2/Layer3 Card Available?	N
Layer 7 Card Available	N
Data Rate	1-100% of OC12/OC3 speeds (See note 3)
Connector	SC-Singlemode or Multimode
Capture buffer size	16MB
Captured packet size	OC3: 49 - 5,120 bytesOC12: 49 - 15,500 bytes (See note 1)
Streams per port	255
Flows per port	N/A
Preamble Size: min- max	N/A
Frame size (trans- mit): min-max	34-65,536 bytes (See note 4)
Frame size (receive): min-max	12-65,536 bytes (See note 5)
Inter-frame gap: min-max	N/A
Inter-burst gap: min-max	1μs - 85secs
Inter-stream gap: min-max	1μs - 85secs
Latency	20ns resolution (See note 2)

- 1. Captured Packet Size Note: At 100% line rate. Smaller values are possible at lower line rates.
- 2. Requires that packets be larger than 70 bytes when operating at full line rate.
- 3. Correct data rates can only be maintained with a minimum number of packets, depending on packet size. For OC12 operation, the numbers of packets are required for the indicated ranges of packet sizes:

OC12 Minimum Number of Packets

Packet Size	Minimum Number of Pack- ets per Stream
45 or less	30
46 - 47	8
48 - 54	7
55 - 63	6
64 - 84	5
85 - 129	4
130 - 199	3
200 - 499	2
500+	0

For OC3 operation, the numbers of packets are required for the indicated ranges of packet sizes:

OC3 Minimum Number of Packets

Packet Size	Minimum Number of Pack- ets per Stream	
34 or less	4	
35 - 64	3	
65 - 274	2	
275+	0	

- 4. The maximum frame size depends on the type of header and PPP negotiation. The maximum frame size is 64k bytes although beyond 8192 bytes, the data is repeated.
- 5. 12 byte frames cannot be received back-to-back. A 34 byte frame is required to receive back-to-back frames.

### **Port LEDs**

Each OC12c/OC3c port incorporates a set of 4 or 6 LEDs, as described in the following table.

LMOC12c Port LEDs

LED Label	Usage
LOS	Red during Loss of Signal.
LOF	Red during Loss of Frame.
Error	Red on any POS error.

LED Label	Usage	
Tx	Green while data is transmitted.	
Rx	Green while data is received.	
Trig	Follows the state of the <i>Trigger Out</i> pin.	

# **Trigger Out Values**

The signals available on the trigger out pins for all cards in this category are described in the following table.

OC12c/OC3c Trigger Out Signals

Pin	Signal
1	Port 1: 10 ns high pulse for each packet matching User Defined Statistic 1
2	Port 2: 10 ns high pulse for each packet matching User Defined Statistic 1
3	Port 1: Low during transmit of frame, otherwise high
4	Port 2: Low during transmit of frame, otherwise high

# **Optical Specifications**

The optical characteristics for the OC12c/OC3c cards are described in the following table.

LMOC12c Optical Specifications

Specification	OC12c/OC3c Mul- timode	OC12c/OC3c Sin- glemode
Average Output Power Minimum/Maximum	-19 dBM/-14 dBM	-15 dBM/-8 dBM
Transmit Center Wavelength Min- imum/Maximum	1270 nm/1380 nm	1293 nm/1310 nm
Receive Center Wavelength Min- imum/Maximum	1270 nm/1380 nm	1200 nm/1550 nm
Receive Sensitive Min- imum/Maximum	-26 dBM/-14 dBM	-28 dBM/-5 dBM
Safety	Led based	Class 1 Laser

# **Statistics**

Statistics for OC12c cards, under various modes of operation may be found in <u>Statistics for OC12c/OC3c Modules</u>.



# Chapter 27 - IXIA OC48c Load Modules

This chapter provides details about OC48c family of load modules specifications and features.

The OC48c family of load modules implements Optical Carrier interfaces that runs at OC48 speeds. The interface operates in concatenated mode, as opposed to channelized mode. Cards are available that perform Packet Over SONET testing, Bit Error Rate Testing or both. The features available for these load modules are included in the *Port Features by Port Type* matrix, which is located on the ixiacom.com website under Support/User Guides/Spreadsheets.

One of the modules in this family, the LMOC48c, is shown in the following figure.

Figure: LMOC48c Load Module



Figure: MSM2.5G1-01 Load Module



# **Part Numbers**

The part numbers are shown in the following figure. Items without a *Price List Names* entry are no longer available.

Part Numbers for OC48 Modules

Load Module	Part Numbers	Description
LMOC48cPOS	LMOC48C	1-port multilayer OC48cSR-1 POS/SDH, 1310nm, singlemode
LMOC48cPOS-M	LMOC48C3	1-port multilayer OC48cSR-1 POS/SDH, 1310nm, singlemode, manufacturing version
LMOC48cBERT	LMOC48311	1-port multilayer OC48cSR-1 SONET/BERT, 1310nm, singlemode
	LMOC48312	1-port multilayer OC48cIR-2 SONET/BERT, 1550nm, singlemode
LMOC48cPOS/BERT	LMOC48411	1-port multilayer OC48cSR-1 POS/BERT, 1310nm, singlemode
	LMOC48412	1-port multilayer OC48cIR-2 POS/BERT, 1550nm, singlemode
2.5G MSM POS	MSM2.5G1- 01	1-port multilayer OC48cSR-1 POS/SDH, 1310nm, singlemode
SW-DCCSONET		DCC SONET support for all modules.

Load Module	Part Numbers	Description	
	SRP SONET support for all modules.		
SW-SRPSONET	945-0002	SRP SONET and RPR SONET support for all modules	
SW-RPRSONET	313 0002		
SW-VCAT-SONET	945-0005	SONET Virtual Concatenation (VCAT) option	

# **Specifications**

The load module specifications are contained in the following table. The limitations of -3, Layer 2/3, and Layer 7 cards are discussed in <a href="Ixia Load Modules">Ixia Load Modules</a>.

OC48 Load Module Specifications

OC40 Edad Module Specifications				
	LMOC4- 8c	LMOC48cBERTLMOC48c- BERTRx	LMOC48cPOS+- BERT	2.5G MSM POS <sup>2</sup>
# ports	1	1	1	1
-3/-M Card Available	Y	N	N	N
Lay- er2/Layer3 Card Avail- able?	N	N/A	N	Y
Layer 7 Card Avail- able	N	N/A	N	N
Data Rate	1-100% of OC48 speeds	2.488 Gbps		1-100% of OC48 speeds
Connector/ Wavelengt- h-Mode	SC/1310- nm or 1550nm Sin- glemode	SC/1310nm Singlemode		SFP/1310- nm or 1550nm Sin- glemode
Capture buffer size	32MB	N/A		Up to 384 MB
Captured packet size	26- 65,535 bytes	N/A		17-65,535 bytes

	L M O C 4 - 8 c	LMOC48cBERTLMOC48c- BERTRx	LMOC48cPOS+- BERT	2.5G MSM POS <sup>2</sup>
Streams per port	255	N/A		256
Flows per port	N/A	N/A		N/A
Advanced Streams	160			256
Preamble size: min-max	N/A	N/A		N/A
Frame size: min- max	26- 65,535	N/A		25-65,535
Inter- frame gap: min- max	N/A	N/A		4.0ns - 42sec in 3.2ns steps
Inter-burst gap: min- max	1μs - 42secs	N/A		4.0ns - 42sec in 10.0ns steps
Inter- stream gap: min- max	1μs - 42secs	N/A		4.0ns - 42sec in 10.0ns steps
Normal stream frame rate	0.023fps - full line rate			0.023fps - full line rate
Advanced streams frame rate <sup>3</sup>	Slow: 0.023 - 2083333 fpsMed: 95fps - full line rateFas- t: 1525fps - full line rate			Slow: 0.023fpsF- ast: 1525fps
Latency	20ns res- olution	N/A		20ns res- olution

<sup>1</sup>Refer to the LMOC48cPOS and LMOC48cBERT columns for the characteristics of this card when its port is in POS or BERT mode, respectively.

<sup>2</sup>Due to power requirements, only one 2.5G MSM POS module can be used in a 400T chassis. Other modules can be used with the 2.5G MSM POS in the same chassis, but only one 2.5G MSM POS at a time.

<sup>3</sup>Streams are divided up into three categories: 144 slow speed streams, 8 medium streams, and 8 fast streams (excluding the 2.5G MSM POS load module).

### **OC48c VAR Calibration**

This procedure allows the OC48 VAR module's transmission frequency to be varied to test compliance of devices to the limits of the specification.

### **Frequency Adjustment**

The OC48 VAR allows a variation of +/- 100 parts per million (ppm) from the clock source's nominal frequency, through a DC voltage input into the BNC jack marked `DC IN' on the front panel. The variation is from the lowest frequency when DC IN is 0 V, to highest frequency when DC IN is 3.3 V. The input voltage should be used only within this range, although the DC IN circuitry is designed to withstand +/- 30 V in the case of accidental overdrive from a function generator. The input has a single-pole low pass at 16 Hz to keep injected noise from causing a violation of OC48 jitter specifications. As a result, the system should be given 50 to 100 milliseconds to settle after a voltage step at DC IN.

### **Frequency Monitoring**

The frequency may be monitored through the BNC marked `Freq Monitor.' This output provides the OC48 line clock divided by 16. The center frequency is 155.52 MHz. The voltage is 70 mV peak-to-peak into 50 ohms, suitable for direct connection into a frequency counter (such as an HP53181A) through 50 ohm coaxial cable. The frequency counter should be set for 50 ohm termination in a suitably sensitive mode.

### **Port LEDs**

LOS

There are two sets of LEDs, one for LMOC-48c load modules and one for MSM OC-48c load modules.

Each OC48c port incorporates a set of LEDs, as described in the following figure.

# PPP Green if a PPP link has been established. Red otherwise. Option 1 Reserved for future use. Option 2 Reserved for future use.

Red during Loss of Signal, Green otherwise.

### LMOC48c Port LEDs

LED Label	Usage
Tx	Green while data is transmitted.
Rx	Green while data is received.
Trig	Follows the state of the <i>Trigger Out</i> pin, which is programmed through User Defined Statistic 1.

Each 2.5G MSM POS port incorporates a set of LEDs, as described in the following table.

MSM2.5G1-01 Port LEDs

LED Label	Usage
Trigger	Green if a Trigger A condition occurred, Red if a temperature condition occurred.
Tx	Green if transmit is active and frames are being sent, blank otherwise.
LOS	Green if signal level is good, Red if loss of signal condition is detected, blank if no transceiver is detected.
Error	Red if module is in an error state, blank otherwise.
Rx	Green if valid frames being received, Red if errored frames being received, blank otherwise.
LOF	Green if valid framing exists, Red if loss of frame condition exists.

# **Trigger Out Values**

The signals available on the trigger out pins for legacy OC-48c load modules in this category are described in the following table.

LMOC48c Trigger Out Signals

Pin	Signal
1	Always high (no trigger available)
2	Always high (no trigger available)
3	Always high (no trigger available)
4	Always high (no trigger available)

The signals available on the trigger out pins for MSM load modules in this category are described in the following table.

2.5G MSM POS Trigger Out Signals

Pin/LED	Value		
Trigger Out	10nS active high pulse on trigger.		
Trigger LED	Indicates Trigger. This triggers on User Defined Statistic 1.		

# **Optical Specifications**

The optical characteristics for the OC48c cards are described in the following table.

LMOC48c Optical Specifications

Specification	OC48c Singlemode
Average Output Power Minimum/Maximum	-10 dBM/-3 dBM
Transmit Center Wavelength Min- imum/Maximum	1266 nm/1360 nm
Receive Center Wavelength Min- imum/Maximum	1260 nm/1580 nm
Receive Sensitive Min- imum/Maximum	-18 dBM/-3 dBM
Safety	Class 1 Laser

### **Statistics**

Statistics for OC48 cards, under various modes of operation may be found in <u>Statistics for OC48c Modules with BERT.</u>



# **Chapter 28 - IXIA FCMGXM Load Modules**

This chapter provides details about FCMGXM family of load modules specifications and features.

The FCMGXM family of high speed load modules delivers high-density, 2/4/8G fibre channel test solution. These load modules deliver high-density converged data center infrastructure for testing end-to-end Fibre Channel and Fibre Channel over Ethernet (FCoE) testing. The fibre channel load module comes with four or eight ports and each port can be configured to run at 2, 4, or 8 G speeds.

The 4-port and 8-port FCMGXM load modules deliver complete FC-2 and FCP data plane capabilities and performance.

One of the modules in this family, the FCMGXM8, is shown in the following figure.

Figure: FCMGXM Load Module



### **Part Numbers**

The part numbers are shown in the following table.

Part Numbers for FCMGXM Modules

Load Module	Part Num- bers	Description
FCMGXM4	950-0001 FCMGXM4S- 01	4-Port Fibre Channel Load Module, with 2 Gbps, 4 Gbps and 8 Gbps support and SFP+ interface. It requires one or more SFP+ transceiver options.
FCMGXM8	950-0002 FCMGXM8S- 01	8-Port Fibre Channel Load Module, with 2 Gbps, 4 Gbps and 8 Gbps support and SFP+ interface. It requires one or more SFP+ transceiver options.

# **Specifications**

The load module specifications are contained in the following table.

FCMGXM Load Module Specifications

Feature	Specification
Load Modules	FCMGXM8/FCMGXM4
Number of ports per module	8/4
Number of chassis slots per module	1

Feature	Specification				
Maximum ports per chassis	XM12 High Performance chassis is required for 88 ports to be installed in a single chassis. Up to eleven 8-port load modules are supported in an XM12 High Performance chassis, and up to 8 8-port load modules are supported in a standard XM12 chassis. The XM2 chassis supports up to 16 ports.				
Supported trans- ceivers	SFP+ Tri-rate 2/4/8G duplex LC connector 850nm multimode 1310 single mode.				
Per-port CPU speed and memory	800 MHz, 1 GB/1 GHz, 1 GB.				
Per-port capture buf- fer	512 MB				
Interface speeds	2/4/8G FC				
FC-1 Primitives	Yes				
FC-2 Protocols	Yes				
FCP Support	Yes				
Number of transmit flows per port (sequential values)	Billions				
Number of transmit flows per port (arbit- rary values)	1 million				
Number of trackable receive flows per port	1 million				
	256				
Number of stream definitions per port	In packet stream (sequential) or advanced stream (interleaved) mode, each stream definition can generate millions of unique traffic flows.				
	1 million entries.				
Table UDF	Comprehensive packet editing function for emulating large numbers of flows. Entries of up to 256 bytes, using lists of values can be specified and placed at designated offsets within a stream. Each list consists of an offset, a size, and a list of values in a table format.				
Packet flow statistics	Tracks 1 million flows.				
Transmit engine	Wire-speed packet generation with timestamps, sequence num-				

Feature	Specification		
	bers, data integrity signature, and packet group signatures.		
Receive engine	Wire-speed packet filtering, capturing, real-time latency, and inter-arrival time for each packet group, data integrity, and sequence checking.		
User defined field features	Fixed, increment, or decrement by user-defined step, value lists, range lists, cascade, random, and chained fields.		
Filters	2x128-bit user-definable pattern and offset, frame length range, CRC error, data integrity error, and sequence checking error (small, big, reverse).		
Data field per stream	Fixed, increment (byte/word), decrement (byte/word), random, repeating, user-specified, CJPAT, and CRPAT fields.		
Error generation	CRC (good/bad), oversize frame, parity error, and R_RDY errors.		
Latency meas- urements	20 nanoseconds resolution in packet timestamp.		
Statistics	The new statistics are as follows:  Link State and speed  (Tx) Bytes, Frames, (count and rate)  (Rx) Bytes, Frames, (count and rate)  (Rx) CRC errors, Oversize (2112), Undersize (24) (count and rate)  Packet group Latency  Data Integrity  Capture Trigger/Filter (count and rate)  User Defined Stats: 6 (count and rate)  Protocol Server Tx/Rx (count and rate)  Remote B-B Credit Value  Remote B-B Credit Count  R_RDY Tx/Rx (count and rate)  Disparity errors (count and rate)  Stats: Port CPU status  Transmit Duration  Invalid EOF Count/Rate  Code Error Count/Rate  FLOGI Sent  FLOGI Sent  PLOGI Sent  PLOGI LS_ACC received  PLOGI Request received		

Feature	Specification
	<ul> <li>PLOGO Sent</li> <li>PLOGO Received</li> <li>FDISC Sent</li> <li>FDISC LS_ACC Received</li> </ul>
	<ul> <li>NS Registration Sent</li> <li>NS Registration Successful</li> <li>NxPort Enabled</li> <li>NxPort-IDs Acquired</li> <li>NS Query Sent</li> <li>NS Query Successful</li> <li>PRLI Sent</li> <li>PRLI Successful</li> <li>PRLI Received</li> <li>RSCN Received</li> <li>RSCN Acc Transmitted</li> <li>SCR Transmitted</li> </ul>
Operating temperature range	• SCR Acc Received 41°F to 95°F (5°C to 35°C), ambient air.

# Chapter 29 - IXIA Xcellon-Flex Load Modules

This chapter provides details about Xcellon-Flex family of load modules specifications and features.

The Xcellon-Flex family of high speed load modules delivers high-density, high-performance test solutions. Xcellon, the architecture behind these load modules, features aggregation of multi-core CPUs and high memory to meet testing needs for high-scale performance.

The Xcellon-Flex family consists of the following load modules:

- 10GbE Accelerated Performance
- 10GbE Full Emulation
- A 10/40 Gigabit Ethernet Accelerated Performance
- A 40 Gigabit Ethernet Full Emulation

The card names are FlexAP10G16S, FlexFE10G16S, FlexAP1040SQ, and FlexFE40QP.

The Accelerated Performance load module provides architecture for layer 2-7 performance testing, providing ultra-high-scale session and protocol emulation per port. The Full Emulation load module is for layer 2-3 mid-range protocol emulation and scale capacity testing for switches and routers. The Xcellon-Flex Combo 10/40GE Accelerated Performance load module provides both 10GE SFP+ and/or 40GE QSFP+ ports in a single chassis slot. It uses aggregation technoloAgy to combine CPU power and memory, and provides ultra-high networking protocol scalability. The 4x40GE Full Emulation load module has a rich layer 2-7 feature set and is well suited for mid-range protocol emulation and scale testing. The load module is ideal for manufacturers of large-port-count, converged data center switches.

The Xcellon-Flex family load module is shown in the following figure:

Figure: Xcellon-Flex Module-FlexAP10G16S



The Xcellon-Flex family load module is shown in the following figure:

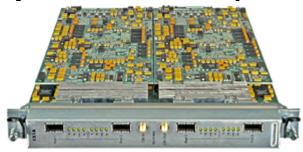
Figure: Xcellon-Flex Module-FlexFE10G16S



Figure: Xcellon-Flex Module-FlexAP1040SQ



Figure: Xcellon-Flex Module-FlexFE40QP



### **Part Numbers**

The part numbers are shown in the following table.

Part Numbers for Xcellon-Flex Modules

Model Num- ber	Part Number	Description
FlexAP10G16S	944-1060	10 Gigabit Ethernet Accelerated Performance Load Module, 16-Port LAN, SFP+ interface with full performance L2-L7 support.
FlexFE10G16S	944-1061	10 Gigabit Ethernet Full Emulation Load Module, 16-port LAN, SFP+ interface with L2-3 support.
FlexAP1040SQ	944-1062	10/40 Gigabit Ethernet Accelerated Performance Load Module, 16-Ports of SFP+ interfaces and 4-ports of QSFP+ 40GE interfaces with full performance L2-7 support, for XM12-02 (941-0009) High Performance rackmount chassis and XM2-02 (941-0003) portable chassis, requires one or more SFP+ transceiver options: 10GBASE-SR/SW (948-0013), or 10GBASE-LR/LW (948-0014).
FlexFE40QP	944-1065	40 Gigabit Ethernet Full Emulation Load Module, 4-ports of QSFP+ 40GE with L2-3 support.

# **Specifications**

The load module specifications are contained in the following table.

Xcellon-Flex Load Module Specifications

Feature	Everest 10GE Full Feature	Everest 10GE Reduced Feature	Everest Combo	Everest 40GE Only
Load Modules	FlexAP10G16S	FlexFE10G16S	FlexAP1040SQ	FlexFE40QP
Number of ports per mod-ule	16	16	4	4
Number of chassis slots per module	1	1	1	1
Maximum ports per chassis	XM12 High Per- formance: 128 XM2Desktop: 16	XM12 High Per- formance: 128 XM2Desktop: 16	XM12 High Per- formance: 96- ports 10GE SFP+ and 24- ports 40GE QSFP XM2Desktop: 16-ports 10GE SFP+ or 4- ports 40GE QSFP	XM12 High Per- formance: 24- ports 40GE QSFP+ XM2Desktop: 4- ports 40GE QSFP+

NOTE

XM12 High Performance chassis is required for the simultaneous operation of 128 ports in a single chassis. If a standard XM12 chassis (941-0002) is used with these load modules, conversion to the High Performance model is required. A field replaceable power supply upgrade kit (943-0005) is available for this purpose. When one or more FlexAP10G16S or FlexFE10G16S load modules is installed in an XM12 High Performance chassis, the maximum total number of load modules that may be installed at one time in a single chassis is 8. The XM2 portable chassis (941-0003) supports up to 16 ports (1 load module) of the FlexAP10G16S FlexFE10G16S modules. No other load module is installed in the XM2 chassis when a FlexAP10G16S or FlexFE10G16S load module is installed.

Supported trans- ceivers				
Per-port CPU speed and memory				
Capture buffer size	256 MB	64 MB	256MB (10GE), 1GB(40GE)	256 MB
Frame Size	Minimum Frame Size at	Minimum Frame Size at	Minimum Frame Size at	Minimum Frame Size at Line

Feature	Everest 10GE Full Feature	Everest 10GE Reduced Feature	Everest Combo	Everest 40GE Only
	Line Rate: 48 - No UDF 60 - UDF enabled Minimum Frame Size - may not be at Line Rate: 48 Maximum Frame Size: P0: 9216B others 2500B	Line Rate: 48 - No UDF 60 - UDF enabled Minimum Frame Size - may not be at Line Rate: 48 Maximum Frame Size: P0: 9216B others 2500B	Line Rate: 48 - No UDF 60 - UDF enabled Minimum Frame Size - may not be at Line Rate: 48 Maximum Frame Size: P0: 9216B others 2500B	Rate: 60 Minimum Frame Size - may not be at Line Rate: 60 Maximum Frame Size: P0: 9216B others 2500B
Streams per port Table UDF	512 1 million entries	256 256 K entries	512 1 million entries	256 1 million entries
Advanced sched- uler streams per port	512	256	512	256
Latency	20 ns resolution	20 ns resolution	20 ns resolution	2.5 ns res- olution
Ambient Operating Temperature Range	5-30	5-30	5-30	5-30
Tranceiver Type	SFP+	SFP+	SFP+	QSFP+
Direct Attach Copper	Yes	Yes	No	Yes
LED	2 LED per Port	2 LED per Port	1 LED per Port	4 LED per Port
ppm Adjust range	+/-100ppm	+/-100ppm	+/-100ppm	+/-100ppm
ppm Adjust port/card	Card	Card	Card	Card
10GbE Interface protocols	10GbE LAN	10GbE LAN	IEEE802.3ae 10GE LAN, IEEE802.3ba	IEEE802.3ae 10GE LAN, IEEE802.3ba

Feature	Everest 10GE Full Feature	Everest 10GE Reduced Feature	Everest Combo	Everest 40GE Only
			40GBASE-R LAN	40GBASE-R LAN
Data Center Pro- tocol Upgrades	FCoE, Priority-ba (IEEE	sed Flow Control		Priority-based Flow Control
(optional fea- ture)	802.1Qbb) and LL port	LDP/DCBX sup-		(IEEE 802.1Qbb)
Multi-core pro- cessors	Yes	Yes	Yes	Yes
Aggregation capability	Yes	Yes	Yes	No
Layer 2-3 rout- ing protocol emulation	Yes	Yes	Yes	Yes
Layer 4-7 application traffic testing	Yes	No	Yes	Yes
Number of transmit flows per port (sequential val- ues)	Billions	Billions	Billions	Billions
Number of transmit flows per port (arbitrary val- ues)	1 million	32 K		
Number of transmit flows per port			1 million	1 million
(PGID)				
Trackable receive flows	1 million	64 K	1 million	64 K
Table UDF	1 million entries	256 K entries	1 million entries	1 million entries
Packet flow statistics	Track 1 million flows	Track 64 K flows		

Feature	Everest 10GE Full Feature	Everest 10GE Reduced Feature	Everest Combo	Everest 40GE Only
Transmit engine	Wire-speed packet filtering capturing, real-time latency and intersequence numbers, data integrity signature, and packet group signatures.  Wire-speed packet generation with timestamps, and interarrival time for each packet group, data integrity, and sequence checking.			
Receive engine			ing, real-time late data integrity, and	•
User defined field features	i i	Fixed, increment or decrement by user defined step, value lists, range lists (supported in all 10 GE mode), cascade, random, and chained		
Filters	48-bit source/destination address, 2x128- bit user-definable pattern and offset, frame length range, CRC error, data integrity error, and sequence checking error (small, big, reverse)			
Data field per stream	Fixed, increment (byte/word), decrement (byte/word), random, repeating, and userspecified			
Error gen- eration	CRC (good/bad/none), undersize, oversize			
Latency self-cal- ibration	Ability to calibrate and remove inherent latency			
Link Fault Sig- naling	Link state indic- ator for No Fault, Local Fault, and Remote Fault.	Link state indic- ator for No Fault, Local Fault, and Remote Fault.	FlexAP1040SQ (10GE and 40GE): Generate local and remote faults with controls for the number of faults and order of faults, and the ability to select the option to have	Generate local and remote faults with controls for the number of faults and order of faults, and the ability to select the option to have the transmit port ignore link

Feature	Everest 10GE Full Feature	Everest 10GE Reduced Feature	Everest Combo	Everest 40GE Only
Feature	10GE Full	Reduced		
			count number of link transitions from No fault to Local fault  Remote Fault count - number of link transitions from No fault to Remote fault  Local fault orderedset count number of local fault ordered set (this is bigger than Local Fault count)	faults from a remote link partner.

Feature	Everest 10GE Full Feature	Everest 10GE Reduced Feature	Everest Combo	Everest 40GE Only
			• Remote fault ordered-set count - number of remote fault ordered set (this is bigger than Remote Fault count)	
Transmit line clock adjust-ment	Ability to adjust trange of the follo  LAN mode:	_	n (ppm) line frequ	ency over a
IPv4, IPv6, UDP, TCP	Hardware checksum generation and verification			
Frame length controls	Fixed, random, weighted random, or increment by user-defined step			
Operating temperature range	41°F to 86°F (5°C to 30°C), ambient air  When an Xcellon-Flex load module is installed in an XM12 chassis, the maximum operating temperature of the chassis			
		C (86°F) ambient a		
40 GE Physical Coding Sublayer (PCS) test features				IEEE 802.3ba compliant PCS transmit and receive side test capabilities
Per PCS lane, transmit lane mapping				Supports all combinations of PCS lane mapping: Default, Increment, Decrement, Random, and Custom
Per PCS lane, lane marker, or lane marker				Ability to inject errors into the PCS Lane

Feature	Everest 10GE Full Feature	Everest 10GE Reduced Feature	Everest Combo	Everest 40GE Only
				Marker and simultaneously into PCS Lane Marker and Payload fields by the user. This
and payload error injections				includes the ability to inject sync bit errors into the Lane Marker and Payload. User can control the PCS lane, number or errors, period count and manage the repetition of the injected errors.
Per PCS lane, receive lanes statistics				PCS Sync Header and Lane Marker Lock, Lane Marker mapping, Relative lane skew measurement (up to 104 microseconds), Sync Header and PCS Lane Marker Error counters, indicators for Loss of Synch Header and Lane Marker, BIP8 errors.

# Mechanical Specification of FlexAP10G16S/FlexFE10G16S Load Modules

#### **Front Panel**

The Front panel of FlexAP10G16S/FlexFE10G16S load module is shown in the following figure:

Figure: Front panel of FlexAP10G16S/FlexFE10G16S



### **Led Panel**

Led panel of FlexAP10G16S/FlexFE10G16S Load Module Specifications

Loau	Module Specifications
Feature	Specification
LED1	TX
	10GE Link up = Solid Green
	10GE TX Active = Blinking Green
	10GE TX Error = Blinking Red
	Inactive = Off
LED2	RX
	Loopback = Solid Green
	10GE RX Active = Blinking Green
	10GE RX Error = Blinking Red
	Link Down = Solid Red
	Port Inactive = Off

When port is in aggregation mode (the PCPU resource is used by other port), TX/RX LEDs are inactive (i.e. off). The aggregation egress port will have normal TX/RX LED operation.

# Mechanical Specification of FlexAP1040SQ Load Modules

### Front Panel Production 944-1062-02

The Front panel of FlexAP1040SQ load module is shown in the following figure:

Figure: Front panel of FlexAP1040SQ



### Led Panel Production 944-1062-02

The Led panel of FlexAP1040SQ load module is shown in the following figure:

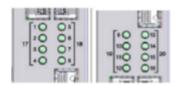


Figure: Led panel of FlexAP1040SQ

Led panel of FlexAP1040SQ Load Module Specifications

Feature	Specification	
10GE Mode	1 LED/Port where LED number matches port number	
Blinking Green	Tx/Rx Activity	
Blinking Red	Rx Error	
Solid Red	Link down	
Solid Green	Link up	
Solid Yel- low	Loopback	
Off	Port is inactive	

When port is in aggregation mode (the PCPU resource is used by other port), TX/RX LEDs are inactive (i.e. off). The aggregation egress port will have normal TX/RX LED operation.

Feature	Specification		
	LED/Port aligned from top/- down defined as follows:		
40GE Mode	<ul><li>Tx</li><li>Rx</li><li>Link</li><li>Error</li></ul>		

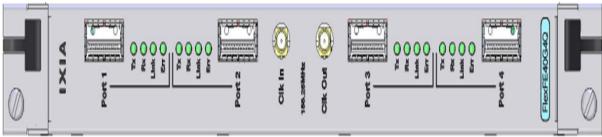
Definition matches the 40G Only definition.

# **Mechanical Specification of FlexAP40QP4 Load Modules**

### **Front Panel**

The Front panel of FlexAP40QP4 load module is shown in the following figure:

Figure: Front panel of FlexAP40QP4



### **Led Panel**

Led panel of FlexAP40QP4 Load Module Specifications

Feature	Specification	
	LED/Port aligned from top/- down defined as follows:	
	• Tx	
	• Rx	
	• Link	
	• Error	
LED1	TX	
	10GE TX Active = Blinking Green	
	10GE TX Error = Blinking Red	
	Inactive = Off	
LED2	RX	
	10GE RX Active = Blinking Green	
	10GE RX Error = Blinking Red	
	Port Inactive = Off	
LED3	Link	
	Link up = Solid Green	
	Link Down = Solid Red	
	Internal Loopback = Solid Yel-	

Feature	Specification
	low
	Line Loopback = Solid Blue
	Port Inactive = Off
LED4	Error
	Remote Faults = Blinking Yel- low
	Local Faults = Solid Red
	Port Inactive = Off



# **Chapter 30 - IXIA Xcellon-Multis Load Modules**

This chapter provides details about Xcellon-Multis family of load modules-specifications and features.

Xcellon-Multis is a new, next generation, high density, tri-speed, 100/40/50/10GE load module (i.e. NG 100GE) family of products. This load module family comprises the industry's highest density 10GE, 40GE, 50GE and 100GE higher speed Ethernet (HSE) test equipment, providing more flexible test coverage and 100GE, 50GE, 40GE, 10GE, 25GE speeds. Some Multis modules are capable of multi-rates within the same load module.

This is done using cable fan-out technology. Fan-out technology allows a higher speed port to fan-out to several ports of lower speed thus enabling you to have multiple speeds from a single port and higher port densities per chassis.

Xcellon-Multis QSFP load module family comprises the industry's highest- density 10GE, and 40GE higher speed Ethernet (HSE) test equipment, providing more flexible test coverage at 12x40GE ports per load module, with a dual-rate 40GE/10GE capability, all in a single-slot load module.

Xcellon-Multis native QSFP28 and CFP4 interface technology comprises high-density 100GE load module.

Xcellon-Multis QSFP28 enhanced multi-rate load module allows upto 16 ports of 25GE per blade and 4 ports of 25GE over a 100GE passive copper cable and Active Optical cable. This load module also supports 1x50GE and 2x25GE speeds.

The CFP4 enhanced load module is an enhanced high density, native CFP4 4-port load module for 100GE operation.

Xcellon-Multis supports the following:

- 4 x 100GE CXP ports per slot 2x Xcellon-Lava
- 12 x 40GE QSFP+ ports per slot 3x Xcellon-Flex
- Upto 32 SFP+ ports per slot
- 40x100GE or 120x40GE ports per XG12 chassis
- 6x40GE QSFP native ports per slot
- 3x10GE and 8x10GE CXP and QSFP ports per slot
- 16x25GE QSFP28 ports per slot
- 8X25GE QSFP28 ports per slot
- 4x50GE QSPF28 ports per slot
- 4x100GE QSFP28 ports per slot.
- 4x100GE CFP4 ports per slot.
- Broad Layer 23 protocol coverage
- Multimode fiber support on some variants

# **Key Features**

The key features of Xcellon-Multis load modules are as follows:

#### **Highest density QSFP module**

- Xcellon-Multis QSFP provides upto 12-ports of native QSFP 40GE interfaces in a single chassis slot.
- Up to 120 native QSFP 40GE interfaces are supported in XG12 rackmount chassis.
- With 10GE Fan-out enabled, Xcellon-Multis QSFP supports up to 320-ports of 10GE in the XG12 rackmount chassis.

#### **Highest density QSFP AVB module**

- Xcellon-Multis AVB provides upto 6-ports of native QSFP 40GE interfaces in a single chassis slot
- It provides upto 60 native QSFP 40GE interfaces are supported in Ixia's XGS12-SD rack mount chassis
- With 10GE fan-out enabled, Xcellon-Multis AVB can support up to 160-ports of 10GE in the XGS12-SD rack mount chassis

#### **Highest density CXP module**

Xcellon-Multis comprises three CXP-based load modules in a single chassis slot.

- 4x100GE only
- 12x40GE and upto 32 ports of 10GE, using fan-out technology
- Multi-rate 4x100GE, 12x40GE, and 32x10GE using fan-out technology

#### **Highest- density QSFP28 and CFP4 modules**

- Both Xcellon-Multis QSFP28 and CFP4 provide up to 4-ports of native QSFP28 and CFP4 100GE interfaces respectively in a single chassis slot.
- Support mid-range-to-high-scale protocol testing for L2/3 routing/switching and data center test cases with the Ixia's IxNetwork application.
- Perform multi-vendor interoperability between different QSFP28 and CFP4 optical transceiver solutions, and cable media such as Active Optical Cables.
- Conduct stress tests to ensure error-free network data transmission with long-term stability and high reliability.
- Detect and de-bug data transmission errors using 100Gb/s line rate packet capture and decode tools.
- Provide an excellent test platform for 100GBASE-SR4, 100GBASE-CR4, and 100GBASE-LR4 100GE ASIC designs, FPGAs and hardware switch fabrics at full line rate 100Gb/s.
- Benchmark the data plane and protocol performance of ultra-high-density 100GE network equipment using industry-standard RFC benchmark tests in 100GE test beds with hundreds of 100GE ports in a single test.

#### Enhanced high-density QSFP28 and CFP4 4-port load modules

 Per native QSFP28 port, supports 4x25GE speed over 100GE passive copper cable media up to 3 meters in length, providing the ability to test the leading-edge data center switches that support 100GE and 4x25GE over four 25Gb/s SERDES lanes

- Supports 2x25GE speed on QSFP28. The 2x25GE mode is a subset of 4x25GE and has the same capabilities, except that only 2 ports of the port group are activated.
- Supports 1x50GE speed per port (a total of 4 ports of 50GE across a single load module).
- Native CFP4 enhanced high density, 4-port load module for 100GE operation.
- Both QSFP28 and CFP4 enhanced load modules have multi-vendor interoperability between different CFP4 and QSFP28 multimode (100GBASE-SR4), single mode (100GBASE-LR4) and 100GBASE-CR4 optical transceiver solutions, and cable media such as Active Optical Cables.
- Provides an excellent test platform for full line rate 100Gb/s to evaluate the new 100GE ASIC designs, FPGAs, and hardware switch fabrics that use the 4x25Gb/s electrical interface.
- High density 4-ports of 100GE in a single slot with native QSFP28 physical interfaces supported by the 4x25GE/s electrical interface.
- Provides Reed-Solomon Forward Error Correction and Auto-Negotiation.

#### Layers 2-7 coverage

- Supports mid-range-to-high-scale protocol testing for L2-3 routing/switching and data center test cases.
- Provides L4-7 capability for all cards.

#### Same feature set across all speeds

- Provides data plane features for 100/40/10GE testing.
- Provides L23 protocol coverage for 100/40/10GE testing.

#### **Cost Effective**

Reduces total cost of ownership with more ports in a single chassis; 120x40GE, or upto 320 10GE ports with fan-out enabled technology.

#### **Load Modules**

The Xcellon-Multis family consists of the following models on a single slot card:

- **XM100GE4CXP**: CXP 100GE single rate module that has 4-ports of 100GE CXP, which is the highest density 100GE test module.
- XM100GE4CXP+FAN: CXP 100/40GE dual rate module that has 4-ports of 100GE CXP 12-ports of 40GE CXP (using fan-out technology) providing the highest density 40GE test module.
- **XM40GE12QSFP+FAN**: 12-ports of 40GE QSFP+ (using fan-out technology) providing the highest density 40GE test module.
- **XM10/40GE12QSFP+FAN**: 12-ports of 40/10GE QSFP+ (using fan-out technology) providing the highest density 40GE test module with 10GE Fan-out capability.
- **XM10/40GE6QSFP+FAN**: 6-ports of 40/10GE QSFP+ (using fan-out technology) providing the highest density 40GE test module with 10GE Fan-out capability.
- XM100GE4QSFP28: 4-ports of 100GE native QSFP28 high density test module.
- XM100GE4CFP4: 4-ports of 100GE native CFP4 high density test module.

- **XMAVB10/40GE6QSFP+FAN**: 6-ports of native QSFP interfaces with 10G fan-out capabilities supporting AVB protocols.
- **XM100GE4QSFP28+ENH**: 4-ports of 100GE native QSFP28 high density test module with RS-FEC and Auto Negotiation capabilities. 1x50GE speed per port (a total of 4 ports of 50GE across a single load module) is also supported.
- **XM100GE4CFP4+ENH**: 4-ports of 100GE native CFP4 high density test module with RS-FEC and Auto Negotiation capabilities.

Each of these load modules are described as follows:

#### XM100GE4CXP

Xcellon-Multis XM100GE4CXP is a 100-Gigabit Ethernet, single rate load module. It has 1-slot with 4-ports native CXP interfaces. It provides L2-7 support and is compatible with XM12 HP rackmount, XM2 desktop, XGS12-SD, XGS12-HS, and XG12 rackmount chassis.

You need to select one or more of the following per port:

- 948-0030 CXP 100GE pluggable
- Optical transceivers
- 942-0035 MTP-MTP 24-fiber multimode fiber cable, or point-to-point CXP Active Optical Cable (AOC)

The XM100GE4CXP load module is shown in the following figure:

Figure: Xcellon-Multis Module-XM100GE4CXP



NOTE

Xcellon-Multis load modules have 64KB memory per resource group for stream data. As the value list, frame size and other stream properties become more complex, the maximum number of streams decrease.

# XM100GE4CXP+FAN (+10G)

Xcellon-Multis XM100GE4CXP+FAN is a 100/40-Gigabit Ethernet, dual rate load module. It has 1-slot with 4-ports native CXP interfaces and up to 12-ports of 40GE via fan-out cables. The +10G variant supports up to 32 ports of 10GE.

It provides L2-7 support and is compatible with XM12 HP rackmount, XM2 desktop, XGS12-SD, XGS12-HS, and XG12 rackmount chassis.

You can select one or more of the available media per port of the following:

- 948-0030 CXP 100GE pluggable, optical transceivers.
- 942-0035 MTP-MTP 24-fiber multimode fiber cable, or point-to-point CXP Active
  Optical Cable (AOC), or CXP-to-3x40GE QSFP Active Optical Cable (AOC) for 3x40GE
  fan-out, or MTP-to-MTP passive fiber for 3x40GE Fan-out. This cable may be used

with 948-0028 QSFP 40GBASE-SR4 transceivers. The XM100GE4CXP+FAN load module is shown in the following figure:

Figure: Xcellon-Multis Module-XM100GE4CXP+FAN



### XM40GE12QSFP+FAN (+10G)

Xcellon-Multis XM40GE12QSFP+FAN is a 40-Gigabit Ethernet load module. It has 1-slot with 12-ports of 40GE via fan-out cables and provides L2-7 support. The  $\pm$ 10G variant supports up to 32 ports of 10GE.

A quantity of 4 each, 3-meter CXP-to-3x40GE QSFP fan-out cables (942-0054) are available with this load module. This is compatible with XM12 HP rackmount, XM2 desktop, XGS12-SD, XGS12-HS, and XG12 rackmount chassis.

The XM40GE12QSFP+FAN load module is shown in the following figure:

Figure: Xcellon-Multis Module-XM40GE12QSFP+FAN



# XM10/40GE12QSFP+FAN

Xcellon-Multis XM10/40GE12QSFP+FAN is a 40-Gigabit Ethernet QSFP load module. It has 1-slot with 12-ports of 40GE QSFP with L2-7 support. This load module has 10GE Fan-out capability. The load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), XGS12-SD (940-0011), XGS12-HS (940-0006), and XM2 desktop chassis (941-0003).

One or more QSFP+ 40GBASE-SR4 optical transceivers (948-0028) and MT 12-fiber MMF cable, 3-meter length (942-0041) are available with this load module.

The XM10/40GE12QSFP+FAN load module is shown in the following figure:

Figure: Xcellon-Multis Module-XM10/40GE12QSFP+FAN



### XM10/40GE6QSFP+FAN

Xcellon-Multis XM10/40GE6QSFP+FAN is a 40-Gigabit Ethernet QSFP load module. It has 1-slot with 6-ports of 40GE QSFP with L2-7 support. This load module has 10GE Fan-out capability and is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), XGS12-SD (940-0011), XGS12-HS (940-0006), and XM2 desktop chassis (941-0003).

One or more QSFP+ 40GBASE-SR4 optical transceivers (948-0028) and MT 12-fiber MMF cable, 3-meter length (942-0041) are available with this load module.

The XM10/40GE6QSFP+FAN load module is shown in the following figure:/

Figure: Xcellon-Multis Module-XM10/40GE6QSFP+FAN



# XM100GE4QSFP28

Xcellon-Multis XM100GE4QSFP28 is a 100-Gigabit Ethernet, single rate load module It has 1-slot with 4-ports with the native QSFP28 physical interfaces and provides L2-3 support. This load module is compatible with XGS12-SD Chassis (940-0011),XGS12-HS chassis (940-0006), XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0023).

The XM100GE4QSFP28 load module is shown in the following figure:

Figure: Xcellon-Multis Module-XM100GE4QSFP28



### XM100GE4QSFP28+ENH

Xcellon-Multis XM100GE4QSFP28+ENH is an enhanced high density 100-Gigabit Ethernet load module. It has 1-slot with 4-ports with the native QSFP28 physical interfaces, L2-7 support, enhanced for support of Forward Error Correction (RS-FEC) and Auto Negotiation. This load module is compatible with the XGS12-SD rack mount chassis (940-0011), XGS12-HS rack mount chassis (940-0006), XG12 rack mount chassis (940-0005), XM12 HP rack mount chassis (941-0024), and XM2 desktop chassis (941-0023).

This is a multi-rate load module and supports testing of 100GE, 50GE, and 25GE speeds.

The XM100GE4QSFP28+ENH load module is shown in the following figure:

Figure: Xcellon-Multis Module-XM100GE4QSFP28+ENH



# 4x25G options for XM100GE4QSFP28+ENH

4x25G options for XM100GE4QSFP28+ENH is available in two forms:

- Factory Installed
- Field Upgrade

NOTE

The 4x25GE speed options do not support Ethernet Forward Error Correction and Auto Negotiation.

# 4x25GE factory installed

The 4x25GE FACTORY INSTALLED option for the Xcellon-Multis QSFP28 XM100GE4QSFP28+ENH 100GE load module enables 4x25GE capability on all four 100GE QSFP28 ports on the module. The 4x25GE capability is per 100GE port and is ONLY supported over a single 100GE point-to-point QSFP28 cable where each channel of the cable is rated for 25GE per channel operation. This is ONLY supported on the XM100GE4QSFP28+ENH (944-1117) load module.

NOTE

The factory installed option is required for new purchases of the 4x25GE capability for the Xcellon-Multis XM100GE4QSFP28+ENH load module with native QSFP28 4x100GE physical interfaces.

### 4x25GE field upgrade

The 4x25GE FIELD UPGRADE option for the Xcellon-Multis QSFP28 XM100GE4QSFP28+ENH 100GE load module enables 4x25GE capability on all four 100GE QSFP28 ports on the module. The 4x25GE capability is per 100GE port and is ONLY supported over a single 100GE point-to-point QSFP28 cable where each channel of the cable is rated for 25GE per channel operation. This is ONLY supported on the XM100GE4QSFP28+ENH (944-1117) load module.

NOTE

The field upgrade option is required on field upgrade purchases of the 4x25GE capability for the Xcellon-Multis XM100GE4QSFP28+ENH load module with native QSFP28 4x100GE physical interfaces.

### 2x25G option for XM100GE4QSFP28+ENH

2x25G option is also available for XM100GE4QSFP28+ENH. The 2x25GE mode is a subset of 4x25GE and has the same capabilities, except that only 2 ports of the port group are activated.

### 1x50G option for XM100GE4QSFP28+ENH

1x50GE speed per port (a total of 4 ports of 50GE across a single load module) is available for XM100GE4QSFP28+ENH.

### XM100GE4CFP4

Xcellon-Multis XM00GE4CFP4 is a 100-Gigabit Ethernet, single rate load module. It has 1-slot with 4-ports with the native CFP4 physical interfaces and provides L2-3 support. This load module is compatible with XGS12 Chassis (940-0011), XGS12-HS chassis (940-0006), XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0023).

The XM100GE4CFP4 load module is shown in the following figure:

Figure: Xcellon-Multis Module-XM100GE4CFP4



#### XM100GE4CFP4+ENH

Xcellon-Multis XM00GE4CFP4+ENH is an enhanced high density 100-Gigabit Ethernet load module. It has 1-slot with 4-ports with the native CFP4 physical interfaces and provides L2-7 support, enhanced for support of Forward Error Correction (RS-FEC) and Auto Negotiation. This load module is compatible with XGS12-SD rack mount chassis (940-0011), XGS12-HS rack mount chassis (940-0006), XG12 rack mount chassis (940-0005), XM12 HP rack mount chassis (941-0024), and XM2 desktop chassis (941-0023).

The XM100GE4CFP4+ENH load module is shown in the following figure:





### XMAVB10/40GE6QSFP+FAN

XMAVB10/40GE6QSFP+FAN is a 40-Gigabit Ethernet load module. It has 1-slot with 6-ports of 40GE and 16-ports of 10GE via multimode fan-out cables, with full featured L2-7 control and data-plane support. This load module is compatible with the XGS12-SD rack-mount chassis (940-0011), XGS12-HS (940-0006), and XM2 desktop chassis (941-0023). This load module supports AVB protocols.

One or more QSFP+ 40GBASE-SR4 optical transceivers (948-0031) and MT 12-fiber MMF cable, 3-meter length (942-0041) are available with the load module.

**Note**: The 10GE Fan-out capability of this load module is provided by a software option, which is delivered using a software activation file.

The XMAVB10/40GE6QSFP+FAN load module is shown in the following figure:

Figure: Xcellon-Multis Module-XMAVB10/40GE6QSFP+FAN



#### 10GE fan-out options for XMAVB10/40GE6QSFP+FAN

The 10G Fan-out options are provided in the same manner as that for Xcellon Multis QSFP family.

#### **AVB Protocols**

- Supports MSRP+MVRP and gPTP protocols
- Has 2.5 ns of timestamp resolution and provides highly accurate gPTP measurements
- Facilitates a range of QoS (loss/delay/jitter) testing to verify CBS implementation
- Supports both 1722 and non-1722 encapsulated traffic
- Allows both AVB and Best-Effort traffic to be configured on the same port
  - These protocols are supported on Xcellon Multis AVB Load Module family only.

There are limitations on the number of Xcellon-Multis load modules that can be installed into the XG12, XM12 HP and XM2 chassis. These limitations apply even when Multis load modules are mixed with other Ixia load module types.

For more information, see Chassis Capacity: Maximum Number of Cards and Ports per Chassis Model section in <a href="Xcellon-Multis Load Module Specifications">Xcellon-Multis Load Module Specifications</a> table, and <a href="Xcellon-Multis 10GE Fan-out Load Module Specifications">Xcellon-Multis 10GE Fan-out Load Module Specifications</a> table.

# Xcellon-Multis Fan-out capability through 10GE license

10G option can be upgraded in the following Xcellon-Multis load modules through license. By default, the ports are in 40GE mode for these load modules.

- XM100GE4CXP+FAN
- XM40GE12QSFP+FAN
- XM10/40GE12QSFP+FAN
- XM10/40GE6QSFP+FAN
- XMAVB10/40GE6QSFP+FAN

### **Part Numbers**

Part Numbers for Xcellon-Multis Load Module and Supported Adapters are provided in the following table.

Part Numbers for Xcellon-Multis Modules

Part Numbers for		Acerron-Murcis Modures
Model Number	Part Number	Description
XM100GE4CXP	944-1100	<ul> <li>4-ports of 100GE with the CXP physical interface</li> <li>100GE only</li> <li>Does not have 40GE or Fan-out of 40GE</li> </ul>
XM100GE4CXP+FAN	944-1101	<ul> <li>4-ports of 100GE and upto 12 ports of 40GE with CXP physical interface (3x40GE fan-out x 4 ports)</li> <li>100GE and 40GE</li> <li>40GE Fan-out capable (3x40GE)</li> <li>Fan-out capable through 10GE license</li> </ul>
XM40GE12QSFP+FAN	944-1102	<ul><li>12-port 40GE with QSFP physical interface</li><li>40GE only</li><li>100GE speed is disabled on all 4-ports</li></ul>
XM10/40GE12QSFP+FAN	944-1105	<ul> <li>12-port 40GE with QSFP physical interface</li> <li>10GE Fan-out capable (1x10GEx12-ports)</li> <li>A second 10G mode offers 4x10GE on 8 specific QSFP+ ports, upto 32 ports of 10GE per card.</li> <li>1-slot</li> <li>Fan-out capable through 10GE license</li> </ul>
XM10/40GE6QSFP+FAN	944-1109	<ul> <li>6-port 40GE with QSFP physical interface</li> <li>10GE Fan-out capable (1x10GEx6-ports)</li> <li>A second 10G mode offers 4x10GE on 4 specific QSFP+ ports, upto 16 ports of 10GE per card.</li> <li>1-slot</li> <li>Fan-out capable through 10GE License</li> </ul>
XM100GE4QSFP28	944-1116	<ul><li>4-port 100GE with QSFP28 physical interface</li><li>1-slot</li></ul>
XM100GE4CFP4	944-1110	<ul><li>4-port 100GE with CFP4 physical interface</li><li>1-slot</li></ul>
XMAVB10/40GE6QSFP+FAN	944-1132	6-port 40GE with QSFP physical interface

Model Number	Part Number	Description
		<ul> <li>10GE Fan-out capable (1x10GEx6-ports and 4x10GEx16-ports)</li> <li>1-slot</li> <li>Fan-out capable through 10GE License</li> </ul>
	944-1117	<ul> <li>4-port 100GE or 4-port 50GE with QSFP28 physical interface (with 4x25GE/s host electrical interface)</li> <li>1-slot</li> <li>Provides L2-7 support, enhanced for support of RS-FEC (only for 100G)</li> </ul>
XM100GE4QSFP28+ENH	905-1004	<ul> <li>4x25GE factory installed option for XM100GE4QSFP28+ENH 100GE load module (944-1117)</li> <li>Enables 4x25GE capability on all four 100GE QSFP28 ports on the module</li> <li>Supported over a single 100GE point-topoint QSFP28 cable where each channel of the cable is rated for 25GE per channel operation</li> <li>Does not support 25GE fan-out</li> <li>Supports 100GE Auto Negotiation and 100GE RS-FEC</li> <li>Supports 2x25GE speed. The 2x25GE mode is a subset of 4x25GE and has the same capabilities, except that only 2 ports of the port group are activated.</li> </ul>
	905-1005	<ul> <li>The 4x25GE field upgrade option for XM100GE4QSFP28+ENH 100GE load module (944-1117)</li> <li>Enables 4x25GE capability on all four 100GE QSFP28 ports on the module</li> <li>Supported over a single 100GE point-topoint QSFP28 cable where each channel of the cable is rated for 25GE per channel operation</li> <li>Supports 100GE Autonegotiation and 100GE RS-FEC</li> <li>Does not support 25GE fan-out</li> <li>Supports 2x25GE speed. The 2x25GE mode is a subset of 4x25GE and has the same capabilities, except that only 2 ports of the port group are activated.</li> </ul>

Model Number	Part Number	Description
XM100GE4CFP4+ENH	944-1111	<ul> <li>4-port 100GE with CFP4 physical interface</li> <li>1-slot</li> <li>Supports 100GE Autonegotiation and 100GE RS-FEC</li> <li>Provides L2-7 support</li> </ul>

# **Specifications**

The specifications of the Xcellon-Multis load module variants are provided in the following tables.

### Specifications of 100GE, 40GE and 100/40GE Multis modules

The load module specifications are contained in the following table.

Xcellon-Multis Load Module Specifications

			Module Spec	Xcellon-	Xcellon-
Feature	Xcellon- Multis (100 GE only)	Xcellon- Multis (100/40GE combo)	Xcellon- Multis (40GE only)	Multis QSFP28 (100 GE only)	Multis CFP4 (100 GE only)
Load Modules	XM100GE4- CXP	XM100GE4CXP- +FAN	XM40GE12QSFP- +FAN	XM100GE4QS- FP28	XM100GE4- CFP4
Hardware	Load Modu	le Specification	s		
Slot/Ports	1-slot / 4x100GE ports	1-slot / 4x100GE and 12x40GE ports	1-slot / 12x40GE ports	1-slot / 4x100GE ports	1-slot / 4x100GE ports or 4x50GE ports
Physical Interface	CXP native	• CXP 4x100GE (native) • QSFP 12x40GE (fan-out)	12, via fan-out	<ul> <li>QSFP28 (native)</li> <li>4x25GE host electrical interface for the enhanced load module with 25GE support</li> <li>2x25GE support</li> </ul>	CFP4 (nat- ive)

Feature	Xcellon- Multis (100 GE only)	Xcellon- Multis (100/40GE combo)	Xcellon- Multis (40GE only)	Xcellon- Multis QSFP28 (100 GE only)	Xcellon- Multis CFP4 (100 GE only)		
				as a subset of 4x25GE with same capabilities for the enhanced load module.			
Chassis C	Chassis Capacity: Maximum Number of Cards and Ports per Chassis Model						
XG12 Chassis (940- 0005)	10 cards:  • 40-  ports  of  100GE	10 cards:  • 40-ports of 100GE  • 120-ports of 40GE	10 cards: • 120-ports of 40GE	<ul> <li>40-ports of 100GE</li> <li>40-ports of 50GE</li> <li>QSFP28 enhanced load module supports 160 links of 25GE (i.e. 4x100GE ports with 4x25GE per physical 100GE port). It also supports 2x25GE speed.</li> </ul>			
XM12 HP Chassis (941-0009	8 cards:  • 32-  ports  of  100GE	8 cards:  • 32-ports of 100GE  • 96-ports of 40GE	8 cards: • 96-ports of 40GE	8 cards:  • 32-ports of 100GE  • QSFP28 enhanced load module supports 128 links of 25GE (i.e. 4x100GE ports with 4x25GE per physical 100GE port). It also supports 2x25GE speed.			
XM2 Chassis (941- 0003)	1 card:  • 4-  ports  of  100GE	1 card:  • 4-ports of 100GE  • 12-ports of 40GE	1 card: • 12-ports of 40GE	<ul><li>1 card:</li><li>4-ports of 100GE</li><li>4-ports of 50GE</li></ul>			
XGS2-SD Chassis	2 cards:	2 cards:	2 cards:	2 cards:			

Feature	Xcellon- Multis (100 GE only)	Xcellon- Multis (100/40GE combo)	Xcellon- Multis (40GE only)	Xcellon- Multis  QSFP28 (100 GE only)  Xcellon- Multis CFP4 (100 GE only)	
(940- 0010)	• 8- ports of 100GE	<ul><li>8-ports of 100GE</li><li>24-ports of 40GE</li></ul>	• 24-ports of 40GE	<ul><li>8-ports of 100GE</li><li>8-ports of 50GE</li></ul>	
XGS2-HS Chassis (940- 0012)	2 cards:  • 8-  ports  of  100GE	2 cards:  • 8-ports of 100GE  • 24-ports of 40GE	2 cards: • 24-ports of 40GE	2 cards:  • 8-ports of 100GE  • 8-ports of 50GE	
XGS12-SD Chassis (940- 0011)	10 cards:  • 40 ports of 100GE	10 cards:  • 40 ports of 100G  • 120 ports of 40GE	10 cards: • 120 ports of 40GE	<ul> <li>40-ports of 100GE</li> <li>40-ports of 50GE</li> <li>QSFP28 enhanced load module supports 160-links of 25GE (i.e. 4x100GE ports with 4x25GE per physical 100GE port). It also supports 2x25GE speed.</li> </ul>	
XGS12-HS Chassis (940- 0006)	10 cards:  • 40 ports of 100GE	10 cards:  • 40 ports of 100G  • 120 ports of 40GE	10 cards: • 120 ports of 40GE	<ul> <li>40-ports of 100GE</li> <li>40-ports of 50GE</li> <li>QSFP28 enhanced load module supports 160-links of 25GE (i.e. 4x100GE ports with 4x25GE per physical 100GE port). It also supports 2x25GE speed.</li> </ul>	
CPU and Memory	Multicore processors with 4GB of memory per processor				
IEEE802.3- ba-2010 Interface Protocols	100GBAS- E-SR10	100GBASE- SR10 40GBASE-SR4	40GBASE-SR4	• IEEE 802.3 100GBAS-E-R ASE-R • IEEE 802.3 802.3b-	

Feature	Xcellon- Multis (100 GE only)	Xcellon- Multis (100/40GE combo)	Xcellon- Multis (40GE only)	Xcellon- Multis QSFP28 (100 GE only)	Xcellon- Multis CFP4 (100 GE only)	
				25GBAS- E-R • IEEE 802.3bj • IEEE P802.3b- m	j • IEEE P802.3- bm	
Trans- ceiver Sup- port	Pluggable CXP, 12- lane, MMF for 100GE operation	Pluggable CXP, 12-lane, MMF for 100GE oper- ation QSFP+ MSA	QSFP+ MSA	<ul> <li>100GBAS-E-LR4     QSFP28     for     single     mode     fiber</li> <li>100GBAS-E-SR4     QSFP28     for mul-     timode     fiber</li> </ul>	LR4 CFP4 for single mode fiber	
Operating Tem- perature Range	41°F to 95°F (5°C to 35°C), ambient air			<ul> <li>41°F to 95°F (5°C to 35°C), ambient air</li> <li>0% to 85%, non-condensing</li> </ul>		
Load Mod- ule Dimen- sions	16.0" (L) x 12.0" (W) x 1.3" (H) 406mm (L) x 305mm (W) x 33mm (H)			<ul> <li>16.1" (L) x 1.3" (W) x 12.0"</li> <li>(H) 409mm (L) x 33mm (W) x 305mm (H)</li> </ul>		
Load Mod- ule Weights				<ul> <li>Module only: 13.15 lbs. (5.96 kg)</li> <li>Shipping: 16.95 lbs. (7.69 kg)</li> </ul>		
Transmit Feature Specifications						
Transmit Engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures					
Max.	100GE:	100GE: 128	40GE: 32 / fan-	• 100GE and 50GE: 128		

Feature	Xcellon- Multis (100 GE only)	Xcellon- Multis (100/40GE combo)	Xcellon- Multis (40GE only)	Xcellon- Multis  QSFP28 (100 GE only)  Xcellon- Multis CFP4 (100 GE only)
Streams per Port	128	40GE: 32 / fan- out link	out link	<ul> <li>QSFP28 enhanced load module 25G support: 16</li> </ul>
Max. Streams per Port in Data Center Ethernet	Supported	Supported	Supported	<ul> <li>100GE and 50GE: 128</li> <li>QSFP28 enhanced load module 25G support: 16</li> </ul>
Stream Controls	Rate and fra scheduler	ame size change o	on the fly, sequenti	al and advanced stream
Minimum Frame Size	100GE:  • 60 bytes (line rate)  • 49 bytes (< line rate)	100GE:  • 60 bytes (line rate)  • 49 bytes (< line rate)  40GE:  • 64 bytes (line rate)  • 49 bytes (< line rate)	40GE:  • 64 bytes (line rate)  • 49 bytes (< line rate)	100GE, 50GE and 25GE:  • 60 bytes (line rate)  • 49 bytes (< line rate)
Maximum Frame Size	14,000 byte	s		
Maximum Fame Size in Data Center Eth- ernet	9,216 bytes			
Priority Flow Con- trol	8 line-rate-capable queues with each supporting up to 2,500 byte frame lengths  1 queue supporting up to 9,216 byte frame lengths			
Frame Length Controls	Fixed, incre		ined step, weighte	d pairs, uniform, repeatable

Feature	Xcellon- Multis (100 GE only)	Xcellon- Multis (100/40GE combo)	Xcellon- Multis (40GE only)	Multis M QSFP28 (100 GE (1	cellon- lultis CFP4 LOO GE only)
User defined fields (UDF)			•	step, sequence, va de UDFs are availal	
Value Lists (max.)	4 million / UDF	100GE: 4 mil- lion / UDF 40GE: 1 million / UDF	40GE: 1 million / UDF	<ul> <li>100 GE and 50 million / UDF</li> <li>QSFP28 enhar module 25G s million / UDF</li> </ul>	nced load
Sequence (max.)	256K / UDF	100GE: 256K / UDF 40GE: 64K / UDF	40GE: 64K / UDF	<ul> <li>100 GE and 50 256K / UDF</li> <li>QSFP28 enhar module 25G s 64K / UDF</li> </ul>	nced load
Error Gen- eration	Generate good CRC or force bad CRC, undersize and oversize standard Ethernet frame lengths, and bad checksum				lard Eth-
Hardware Checksum Gen- eration	1	Checksum generation and verification for IPv4, IP over IP, IGMP/GRE/TCP/UDP, L2TP, GTP			
Link Fault Signaling	port statisti Reports the  Link Fa Local fa  Local F itions f  Remote itions f  PCS Lofault or PCS Re	<ul> <li>Local Fault count - number of link transitions from No fault to Local fault</li> <li>Remote Fault count - number of link transitions from No fault to Remote fault</li> </ul>			alt port e local with con- er of faults, select the transmit ults from
Latency Meas- urement Resolution	100GE: 2.5 nano- seconds	100GE: 2.5 nanoseconds 40GE: 2.5 nano- seconds	40GE: 2.5 nano- seconds	100GE, 50GE, 2x25 4x25GE: 2.5 nanos	-

Feature	Xcellon- Multis (100 GE only)	Xcellon- Multis (100/40GE combo)	Xcellon- Multis (40GE only)	Xcellon- Multis QSFP28 (100 GE only)	Xcellon- Multis CFP4 (100 GE only)
Intrinsic Latency Com- pensation		Removes inherent latency error from 40GE or .00GE port electronics			Removes inherent latency error from 100GE port electronics
Transmit line clock adjust- ment		ljust the parts per 0 ppm per resour	r million line freque ce group	ency over a ranç	ge of -100
Receive F	eature Spec	cifications			
Receive Engine	time for each		capturing, real-tim with data integrity,	•	
Trackable Receive Flows per Port	100GE: 512K	100GE: 512K 40GE: 128K	40GE: 128K	• QSFP28 ei	d 50GE: 512K nhanced load 5G support:
Minimum Frame Size	<ul> <li>64 bytes at line rate</li> <li>&gt; 49 bytes not a line rate</li> <li>100GE, 50GE, and 25GE:</li> <li>60 bytes and greate at full line rate</li> <li>49 bytes at less than full line rate</li> </ul>				and greater rate at less than
Filters (User- Defined Statistics, UDS)	2 SA/DA pattern matchers, 2x16-byte user-definable patterns with offsets capability for start of: frame, IP, or protocol. Up to 6 UDS counters are available				
		100GE: 2GB			
Hardware Capture Buffer per Port or Resource Group	100GE: 2GB	40GE: 2GB per 1, user-selec- ted link of the 3x40GE fan- out link resource group	40GE: 2GB per 1, user-selected link of the 3x40GE fan-out link resource group	ed 100GE and 50GE: 2GB	
Statistics and Rates	Link state, I	Link state, line speed, frames sent, valid frames received, bytes sen-			

Feature	Xcellon- Multis (100 GE only)	Xcellon- Multis (100/40GE combo)	Xcellon- Multis (40GE only)	Xcellon- Multis QSFP28 (100 GE only)	Xcellon- Multis CFP4 (100 GE only)	
	frames, 6 us 4), 8 QoS co and advance	t/received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 user-defined stats, capture trigger (UDS 3), capture filter (UDS 4), 8 QoS counters, data integrity frames, data integrity errors, sequence and advanced sequence checking frames, sequence checking errors, ARP, and PING requests and replies				
PCS Lanes Port Stat- istics	Set, Illegal Order Data,	PCS Sync Errors, Illegal Codes, Remote Faults, Local Faults, Illegal Ordered Set, Illegal Idle, Illegal SOF, Out Of Order SOF, Out Of Order EOF, Out Of Order Data, Out Of Order Ordered Set  NOTE  These statistics are available only for 100G and 40G.				
Latency / Jitter Meas- urements	Cut-through, store and forward, forwarding delay, up to 16 time bins latency/jitter, MEF jitter, and inter-arrival time					
L2/3 Rout- ing, Bridging, and Tim- ing	Routing: RIP, RIPng, OSPFv2/v3, ISISv4/v6, EIGRP, EIGRPv6, BGP/BGP+ MPLS: RSVP-TE, RSVP-TE P2MP, LDP, mLDP, BGP RFC 3107, MPLS-TP, MPLS OAM  MPLS VPN: L2VPN PW, L3VPN/6VPE, 6PE, VPLS-LDP, VPLS-BGP, VPLS-BGP AD and LDP FEC 129, Inter-AS VPN Option A, B, and C, Seamless MPLS, Carrier Supporting Carrier (CsC), GRE mVPN, NG MVP (mLDP and RSVP-TE P2MP), EVPN/PBB-EVPN  High-Availability: BFD, Graceful Restart, MPLS Ping/TraceRoute, LSP BFD, VCCV BFD, Real-time dynamic label swap for convergence time measurement up to millisecond accuracy  IP Multicast: IGMPv1/v2/v3, MLDv1/v2, PIM-SM/SSM, PIM-BSR, multicast VPN  Switching: STP/RSTP, MSTP, PVST+/RPVST+, LACP, LLDP, Protocols over LACP Bundle  Carrier Ethernet: Link OAM, CFM, Service OAM, PBT/PBB-TE, SyncE, PTP					
Data Center Eth- ernet	Priority Class-Based Flow Control (IEEE802.1Qbb), FCoE/ FIP, LLDP/DCBX, VNTAG/VIC, OpenFlow, FabricPath, TRILL, SPBM, VEPA, VXLAN					
Broadband Access	L2TPv2, Rad	lius Attributes for	DHCPv4 client/serv L2TP, Dual-Stack BAuth, Cisco NAC		nt/server,	

# Specifications of Multis Modules with 10GE Fan-out capability

The load module specifications for the modules with 10GE Fan-out capability are contained in the following table.

Xcellon-Multis 10GE Fan-out Load Module Specifications

Featur- e	Xcellon- Multis (CXP 10 GE Fan- out upgrade)	Xcellon- Multis (12- port QSFP 10/40GE Fan-out)	Xcellon- Multis (6- port QSFP 10/40GE Fan-out)	Xcellon-Multis AVB (6-port QSFP 10/40GE Fan-out)
Load Mod- ules	XM100GE4CXP+F- AN+10GE	XM10/40GE12QS- FP+FAN	XM10/40GE6QS- FP+FAN	XMAVB10/40GE6Q- SFP+FAN
Hardwar	e Load Module Spe	cifications		
Slot/Port-s	1-slot / 4x100GE and 12x40GE ports	1-slot:  • 12x40GE QSFP native ports  • 10GE fan- out;  • 12x10GE ports (1x10GE/- port)	1-slot:  • 6x40GE QSFP native ports  • 10GE fanout;  - 6x10GE ports (1x10GE/port)	1-slot:  • 6x40GE QSFP native ports  • 10GE fan-out;  - 6x10GE ports (1x10GE/-port)  - 16x10GE ports (4x10GE/-port)
Physical Interface	CXP 4x100GE (native)  QSFP 12x40GE (fan-out)	QSFP 12x40GE (native) 10GE: LC con- nector (fiber), or SFP+ connector (copper)	QSFP 6x40GE (native) 10GE: LC con- nector (fiber), or SFP+ con- nector (copper)	QSFP 6x40GE (native)  10GE: LC connector (fiber), or SFP+ connector (copper)
Chassis (	Capacity: Maximun	n Number of Card	ds and Ports per	Chassis Model
XG12 Chassis (940- 0005)	12 cards:  • 48-ports of 100GE  • 144-ports of 40GE	10 cards:  • 120-ports of 40GE  • 120-ports of 10GE (1x10GE mode)	10 cards:  • 60-ports of 40GE  • 60-ports of 10GE (1x10GE mode)	10 cards:
SD Chassis				60-ports of

Featur- e	Xcellon- Multis (CXP 10 GE Fan- out upgrade)	Xcellon- Multis (12- port QSFP 10/40GE Fan-out)	Xcellon- Multis (6- port QSFP 10/40GE Fan-out)	Xcellon-Multis AVB (6-port QSFP 10/40GE Fan-out)
(940- 0011)				<ul> <li>40GE</li> <li>60-ports of 10GE (1x10GE mode)</li> <li>160-ports of 10GE (4x10GE mode)</li> </ul>
XM12 HP Chassis (941- 0009	8 cards:  • 32-ports of 100GE  • 96-ports of 40GE	8 cards:  • 96-ports of 40GE  • 96-ports of 10GE (1x10GE mode)	8 cards:  • 48-ports of 40GE  • 48-ports of 10GE (1x10GE mode)	
XM2 Chassis (941- 0003)	1 card:  • 4-ports of 100GE  • 2-ports of 40GE	1 card:  • 12-ports of 40GE  • 12-ports of 10GE (1x10GE mode)	1 card:  • 6-ports of 40GE  • 6-ports of 10GE (1x10GE mode)	1 card:  • 6-ports of 40GE  • 6-ports of 10GE (1x10GE mode)  • 16-ports of 10GE (4x10GE mode)
XGS2-SD Chassis (940- 0010)	2 cards:  • 8-ports of 100GE  • 4-ports of 40GE	2 cards:  • 24-ports of 40GE  • 24-ports of 10GE (1x10GE mode)	2 cards:  • 12-ports of 40GE  • 12-ports of 10GE (1x10GE mode)	2 cards:  • 12-ports of 40GE  • 12-ports of 10GE (1x10GE mode)  • 32-ports of 10GE (4x10GE mode)
XGS2-HS Chassis (940- 0012)	2 cards:  • 8-ports of 100GE  • 4-ports of 40GE	2 cards:  • 24-ports of 40GE  • 24-ports of 10GE (1x10GE mode)	2 cards:  • 12-ports of 40GE  • 12-ports of 10GE (1x10GE mode)	2 cards:  • 12-ports of 40GE  • 12-ports of 10GE (1x10GE mode)

Featur- e	Xcellon- Multis (CXP 10 GE Fan- out upgrade)	Xcellon- Multis (12- port QSFP 10/40GE Fan-out)	Xcellon- Multis (6- port QSFP 10/40GE Fan-out)	Xcellon-Multis AVB (6-port QSFP 10/40GE Fan-out)	
				• 32-ports of 10GE (4x10GE mode)	
CPU and Memory	Multicore processor	rs with 4GB of mem	ory per processor		
IEEE802 3ba-2010 Interface Protocols	100GBASE-SR10 40GBASE-SR4	40GBASE-SR4, 40 10GBASE-SR (802	GBASE-LR4 (802.3 .3ae-2002)	ba-2010)	
Trans- ceiver Support	Pluggable CXP, 12-lane, MMF for 100GE operation QSFP+ MSA	QSFP:  • 40GBASE-SR4 (multimode 850nm)  • 40GBASE-LR4 (single mode 1310nm)			
Operating Tem- perature Range	41°F to 95°F (5°C to 35°C), ambient air	41°F to 95°F (5°C to 35°C), ambient air 0% to 85%, non-condensing			
Load Mod- ule Dimen- sions	16.0" (L) x 1.3" (W) x 12.0" (H) 409mm (L) x 33mm (W) x 305mm (H)	16.8" (L) x 1.3" (W) x 12.0" (H) 427mm (L) x 33mm (W) x 305mm (H)			
Load Mod- ule Weights	Module only: 13.0 lbs. (5.90 kg) Shipping: 16.8 lbs. (7.62 kg)	12-port model:  • Module only: 12.5   6 port model:  • Module only: 9.3 lbs. (4.22 kg)  • Shipping: 16.2 lbs. (7.35 kg)		, ,	
Transmit	Transmit Feature Specifications				
Transmit Engine	Wire-speed packet integrity signature,	~		e numbers, data	
Max.	100GE: 128	40GE: 32		40GE: 32	
Streams per Port	40GE: 32 / fan-out link	10GE 12x10 mode fan-out/port)	: 32 (1x10GE	10GE 6x10 mode: 32 (1x10GE fan-	

Featur- e	Xcellon- Multis (CXP 10 GE Fan- out upgrade)	Xcellon- Multis (12- port QSFP 10/40GE Fan-out)	Xcellon- Multis (6- port QSFP 10/40GE Fan-out)	Xcellon-Multis AVB (6-port QSFP 10/40GE Fan-out)
				out/port)
				10GE 16x10 mode: 16 (4x10GE fan- out/port)
				40GE: 32
Max. Streams per Port in Data	Supported	40GE: 32 10GE 12x10 mode	: 32 (1x10GE	10GE 6x10 mode: 32 (1x10GE fan- out/port)
Center Ethernet		fan-out/port)		10GE 16x10 mode: 16 (4x10GE fan- out/port)
Stream Controls	Rate and frame size change on the fly, sequential and advanced stream scheduler			
	100GE:	40GE:		
Minimum	<ul><li>60 bytes (line rate)</li><li>49 bytes (&lt; line rate)</li></ul>	<ul><li>64 bytes (line rate)</li><li>49 bytes (</li><li>line rate)</li></ul>	40GE:  • 64 bytes (lin  • 49 bytes (<	•
Frame Size	40GE:	10GE:	10GE:	,
	<ul><li>64 bytes (line rate)</li><li>49 bytes (&lt; line rate)</li></ul>	<ul><li>64 bytes (line rate)</li><li>49 bytes (&lt; line rate)</li></ul>	<ul><li>64 bytes (lin</li><li>49 bytes (&lt;</li></ul>	-
Maximum Frame Size	14,000 bytes	,		
Maximum Fame Size in Data Center Ethernet	9,216 bytes			
Priority Flow Con- trol	8 line-rate-capable queues with each supporting up to 2,500 byte frame lengths			
	1 queue supporting		<del>-</del>	
Frame	Fixed, increment by	user-defined step,	, weighted pairs, u	niform, repeatable

Featur- e	Xcellon- Multis (CXP 10 GE Fan- out upgrade)	Xcellon- Multis (12- port QSFP 10/40GE Fan-out)	Xcellon- Multis (6- port QSFP 10/40GE Fan-out)	Xcellon-Multis AVB (6-port QSFP 10/40GE Fan-out)	
Length Controls	random, IMIX, and	Quad Gaussian			
User defined fields (UDF)	Fixed, increment or and random configu		· ·	-	
Value Lists (max.)	100GE: 4 million / UDF 40GE: 1 million / UDF	40GE: 1 million / UDF  10GE:  1million / UDF(1x10GE mode)  512K / UDF (4x10GE mode)			
Sequence (max.)	100GE: 256K / UDF 40GE: 64K / UDF	40GE: 128K / UDF 10GE: • 128K / UDF (1x10GE mode) • 64K / UDF (4x10GE mode)			
Error Gen- eration	Generate good CRC or force bad CRC, undersize and oversize standard Ethernet frame lengths, and bad checksum				
Hardware Check- sum Gen- eration	Checksum generation and verification for IPv4, IP over IP, IGMP/GRE/TCP/UDP, L2TP, GTP				
Link Fault Signaling	<ul> <li>Reports, no fault, remote fault, and local fault port statistics.</li> <li>Reports the following PCS statistics:</li> <li>Link Fault State - specifies if the link is in Local fault, Remote fault or No fault</li> <li>Local Fault count - number of link transitions from No fault to Local fault</li> <li>Remote Fault count - number of link transitions from No fault to Remote fault</li> <li>PCS Local Faults count - number of local fault ordered set</li> <li>PCS Remote Faults count - number of remote fault ordered set</li> </ul>				
Latency Meas- urement Res- olution	100GE: 2.5 nano- seconds  40GE: 2.5 nano- seconds  40GE and 10 GE: 2.5 nanoseconds				

Featur- e	Xcellon- Multis (CXP 10 GE Fan- out upgrade)	Xcellon- Multis (12- port QSFP 10/40GE Fan-out)	Xcellon- Multis (6- port QSFP 10/40GE Fan-out)	Xcellon-Multis AVB (6-port QSFP 10/40GE Fan-out)		
Intrinsic Latency Com- pensation	Removes inherent latency error from 40GE or 100GE port electronics	Removes inherent latency error from 40GE or 10GE port electronics				
Transmit line clock adjust- ment	Ability to adjust the parts per million line frequency over a range of -100 ppm to +100 ppm per resource group					
Receive I	Feature Specificat	ions				
Receive Engine	Wire-speed packet filtering, capturing, real-time latency and inter-arrival time for each packet group, with data integrity, sequence and advanced sequence checking capability					
Trackable Receive Flows per Port	100GE: 512K 40GE: 128K	40GE: 128K 10GE: • 128K (1x10GE mode) • 64K (4x10GE mode)				
Minimum Frame Size	64 bytes at line rate  > 49 bytes not a line					
Filters (User- Defined Stat- istics, UDS)	2 SA/DA pattern matchers, 2x16-byte user-definable patterns with offsets capability for start of: frame, IP, or protocol. Up to 6 UDS counters are available					
Hardware Capture Buffer per Port or Resource Group	100GE: 2GB  40GE: 2GB per 1, user-selected link of the 3x40GE fan- out link resource group	• 1x10GE mode: 2GB per 1 user-selected link of the 1x10GE fan-out link resource group				
Statistics and Rates	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 user-defined stats, capture trigger (UDS 3), capture filter (UDS 4), 8 QoS counters, data integrity frames, data integrity errors, sequence and advanced sequence checking frames, sequence checking errors, ARP, and PING requests and replies					

Featur- e	Xcellon- Multis (CXP 10 GE Fan- out upgrade)	Xcellon- Multis (12- port QSFP 10/40GE Fan-out)	Xcellon- Multis (6- port QSFP 10/40GE Fan-out)	Xcellon-Multis AVB (6-port QSFP 10/40GE Fan-out)	
Latency / Jitter Meas- urements	Cut-through, store & forward, forwarding delay, up to 16 time bins latency/jitter, MEF jitter, and inter-arrival time				
Protocol S	Support				
	Routing: RIP, RIPn	g, OSPFv2/v3, ISIS	Sv4/v6, EIGRP, EIG	GRPv6, BGP/BGP+	
	MPLS: RSVP-TE, RS	SVP-TE P2MP, LDP,	mLDP, BGP RFC 31	.07, MPLS-TP, MPLS	
L2/3 Rout- ing, Bridging,	P2MP) FVPN/PRR-FVPN				
Routing, Timing and Car-	<b>High-Availability:</b> BFD, Graceful Restart, MPLS Ping/TraceRoute, LSP BFD, VCCV BFD, Real-time dynamic label swap for convergence time measurement up to millisecond accuracy				
rier Eth- ernet	IP Multicast: IGMI VPN	Pv1/v2/v3, MLDv1/	v2, PIM-SM/SSM,	PIM-BSR, multicast	
	<b>Switching:</b> STP/RS LACP Bundle	TP, MSTP, PVST+/I	RPVST+, LACP, LLI	OP, Protocols over	
	Carrier Ethernet: (1588v2), E-LMI	Link OAM, CFM, Se	rvice OAM, PBT/PE	BB-TE, SyncE, PTP	
Data Center Ethernet	Priority Class-Based Flow Control (IEEE802.1Qbb), FCoE/ FIP, LLDP/DCBX, VNTAG/VIC, OpenFlow, FabricPath, TRILL, SPBM, VEPA, VXLAN				
Broad- band	<b>Broadband:</b> ANCP, PPPoX, DHCPv4 client/server, DHCPv6 client/server, L2TPv2, Radius Attributes for L2TP, Dual-Stack PPPoX, AMT				
Access	Authentication: 802.1x, WebAuth, Cisco NAC				
Audio video bridging				MSRP + MVRP, gPTP	

# **Application Support**

The Ixia application support for Xcellon-Multis load modules is provided in the following table:

Xcellon-Multis Application Support

Application	Support
IxNetwork	Provides wire-rate traffic generation with service modeling that builds realistic, dynamically-controllable data-plane traffic. IxNetwork offers the industry's best test solution for functional and performance testing by using comprehensive emulation for routing, switching, MPLS, IP multicast, broadband, authentication, Carrier Ethernet, and data center Ethernet protocols.
IxExplorer	Layer 2-3 wire-speed traffic generation and analysis and Layer 1 BERT and IEEE 802.3ba HSE PCS Lanes testing.
Tcl API	Custom user script development for layer 1-7 testing.

# **Mechanical Specifications**

## **Front Panel**

The Front panel of Xcellon-Multis load modules is shown in the following figure:

Figure: Front panel of Xcellon-Multis XM100GE4CXP



Figure: Front panel of Xcellon-Multis XM10/40GE12QSFP+FAN



Figure: Front panel of Xcellon-Multis XM10/40GE6QSFP+FAN



## **LED Panel**

The LED panel specifications for Multis CXP module are provided in the following table.

LED panel Specifications for Multis Load Module

Speed Mode	MODE LED	TX LED	RX LED
100G	Off	Link Up=Green Link Down=Red TX Active-Blink- ing Green	RX Active (error- s)=Blinking Red RX Act- ive=Blinking Green
40G	Green	Link Up (all ports)=Green	RX Active (errors)(any-

Speed Mode	MODE LED	TX LED	RX LED
		Link Up (par- tial)=Yellow	)=Blinking Red
		Link Down (all ports)=Red	RX Active (any- )=Blinking Green
		TX Active-Blink- ing Green	
		Link Up (all ports)=Green	
10G	Yellow	Link Up (par- tial)=Yellow	RX Active (errors)(any- )=Blinking Red
100		Link Down (all ports)=Red	RX Active (any- )=Blinking Green
		TX Active-Blink- ing Green	
		Link Up (all ports)=Green	
25G	Blue	Link Up (par- tial)=Yellow	RX Active (errors)(any- )=Blinking Red
230		Link Down (all ports)=Red	RX Active (any- )=Blinking Green
	Red	Faulty Card	Faulty Card

For 10/40GE QSFP modules, there are 2 LEDs per port. They operate the same way in 40GE and 10 GE modes. So the number of LEDs are:

- 12x2 = 24 LEDs on front pannel for 12-port QSFP card
- 6x2 = 12 LEDs for 6-port QSFP card

LED panel Specifications of XM10/40GE12QSFP+FAN, XM10/40GE6QSFP+FAN, and XMAVB10/40GE6QSFP+FAN Load Mod-ules

LED 1: Bi-Color Tx Status LED		LED 2: Bi-Color Rx Status LED	
Ports Inact- ive/No Power	Off	Ports Inact- ive/No Power	Off
Link Down	Solid Red	Rx Active with Errors	Blinking Red
Link Up	Solid Green	Rx Active	Blinking Green

LED 1: Bi-Color Tx Status LED		lor Rx Status ED
Tx Active	Blinking Green	
Partial Link up	Solid Yellow	

# **Fan-out Capability**

The 3x40GE fan-out is a new capability that provides up to 12 independent 40GE QSFP+ links or generic 40GE fiber links. There are up to three 40GE QSFP+ fiber-based links provided via a cable per 100GE CXP physical port, using all of the 4-ports of 100GE CXP on the Multis load module.

## **Fan-out Cable Options**

The Xcellon-Multis cable options are described in the following sections.

## 100GE CXP-to-3x40GE QSFP+ AOC fiber fan-out cables

CXP-to-3x40GE QSFP Active Optical Cable (AOC) cables are used with Xcellon-Multis XM100GE4CXP+FAN 100/40GE (944-1101) and XM40GE12QSFP+FAN 40GE (944-1102) load modules.

100GE CXP-to-3x40GE QSFP+ AOC fiber fan-out cables have the following features:

- Active Optical Cable (AOC)
- Multi-mode fiber (MMF), 850nm
- 942-0053 1 meter
- 942-0054 3 meter
- 942-0055 5 meter

The 100GE CXP-to-3x40GE QSFP+ AOC fiber fan-out cable is shown in the following figure:

Figure: 100GE CXP-to-3x40GE QSFP+ AOC fiber fan-out cable



## MT-MT 3x40GE passive fiber fan-out cables

The MT-MT 3x40GE passive fiber fan-out cables requires 1 each CXP 100GE pluggable optical transceiver (948-0030). This combination is compatible with Xcellon-Multis XM100GE4CXP+FAN 100/40GE (944-1101) and XM40GE12QSFP+FAN 40GE load modules.

The MT-MT 3x40GE passive fiber fan-out cables have the following features:

- Multi-mode frequency (MMF), 850nm
- F-F key-up compatible with CXP & QSFP optical transceivers
- 942-0060 3 meter

- 942-0061 5 meter
- Transceivers are sold separately

The MT-MT 3x40GE passive fiber fan-out cable is shown in the following figure:

Figure: MT-MT 3x40GE passive fiber fan-out cable



## **CXP point-to-point AOC Cable (no fan-out)**

The CXP point-to-point AOC cable has the following features:

- Active Optical Cable (AOC)
- Multi-mode frequency (MMF), 850nm
- 942-0052 3 meter

The CXP point-to-point AOC cable is shown in the following figure:

Figure: CXP point-to-point AOC cable



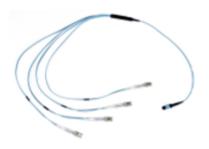
## MT-to-4x10GE LC fan-out, MMF

MT-to-4x10GE LC fan-out, MMF, 3-meter cable requires QSFP 40GBASE-SR4, pluggable, transceiver, 850nm, MMF (948-0031). The cables and transceiver are compatible with Xcellon-Multis XM10/40GE12QSFP+FAN 40-Gigabit Ethernet QSFP load module (944-1105), and the Xcellon-Multis XM10/40GE6QSFP+FAN 40-Gigabit Ethernet QSFP load module (944-1109).

MT-to-4x10GE LC fan-out, MMF, 5-meter cable requires QSFP 40GBASE-SR4, pluggable, transceiver, 850nm, MMF (948-0031). The cables and transceiver are compatible with Xcellon-Multis XM10/40GE12QSFP+FAN 40-Gigabit Ethernet QSFP load module (944-1105), and the Xcellon-Multis XM10/40GE6QSFP+FAN 40-Gigabit Ethernet QSFP load module (944-1109).

The MT-MT 4x10GE passive fiber fan-out cable is shown in the following figure:

Figure: MT-MT 4x10GE passive fiber fan-out cable



## QSFP-to-4x10GE SFP+ Direct Attach Cable (DAC)

QSFP-to-4x10GE SFP+ Direct Attach Cable (DAC) is a passive copper, fan-out, cable that is 3-meter in length. This cable is compatible with the load modules Xcellon-Multis XM10/40GE12QSFP+FAN 40-Gigabit Ethernet QSFP (944-1105) and Xcellon-Multis XM10/40GE6QSFP+FAN 40-Gigabit Ethernet QSFP (944-1109).

The load modules must have the 10GE fan-out option enabled to use this cable. This requires 905-1000 XM10GE-FAN-OUT 10GE fan-out option for NEW purchases of Xcellon-Multis load modules, or the 905-1001 UPG-XM10GE-FAN-OUT 10GE fan-out option UPGRADE for existing Xcellon-Multis load modules.

The QSFP-to-4x10GE SFP+ Direct Attach Cable (DAC) cable is shown in the following figure:

Figure: QSFP-to-4x10GE SFP+ Direct Attach Cable (DAC) cable



# QSFP-to-QSFP 40GE 40GBASE-CR4 Direct Attach Cable (DAC)

QSFP-to-QSFP 40GE 40GBASE-CR4 Direct Attach Cable (DAC) is a passive copper, point-to-point cable that is 3-meter in length. This cable is compatible with the load modules Xcellon-Multis XM10/40GE12QSFP+FAN 40-Gigabit Ethernet QSFP (944-1105) and Xcellon-Multis XM10/40GE6QSFP+FAN 40-Gigabit Ethernet QSFP (944-1109).

The QSFP-to-QSFP 40GE 40GBASE-CR4 Direct Attach Cable (DAC) is shown in the following figure:

Figure: QSFP-to-QSFP 40GE 40GBASE-CR4 Direct Attach Cable (DAC)



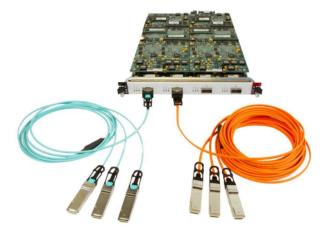
### **Features**

The 100GE fan-out capability has the following features:

- Each 100GE port and transceiver combination has the ability to fan-out to three 40GE QSFP+ links using a fiber fan-out cable media type, or a pluggable transceiver used with a fiber-only fan-out cable.
- Each 100GE port, when in the 3x40GE fan-out configuration, supports one-user for all three 40GE links.
- Each 100GE port with a transceiver that uses a fan-out cable to produce 3x40GE links will equally divide and allocate the data and control plane resources of the 100GE port to each 40GE link.
- There are 32 transmit streams for each of 40GE link in a 3x40GE fan-out configuration and at least 64K Rx PGID capacity per link.
- There is one LED per 100GE CXP port that indicates that the port is in fan-out mode.
- PCS lanes and Link Fault Signaling port counter support supports link troubleshooting for the entire port.

The Xcellon-Multis load module with CXP-to-3x40GE fan-out fiber cables for a 100GE CXP port with a 100GE transceiver installed, is shown in the following figure.

Figure: Xcellon-Multis load module with CXP-to-3x40GE fan-out



## **Benefits**

Due to the enormous growth in Internet users and devices, the total bandwidth requirements of a single switch or router has reached multiple terabits. Devices that scale up to hundreds of 40GE and 100GE ports, instead of dozens, are needed to match such huge bandwidth requirements.

Xcellon-Multis family of load modules allows Higher Speed Ethernet testing using cable fan-out technology. This allows higher ports speeds to fan-out to several ports (links) of another speed. It also has the following benefits:

- 100GE/40GE fan-out technology separates a physical interface into multiple interfaces.
- The same features for 100GE and 40GE can be used from a single port or a group of ports.
- The same features for 100GE and 40GE all able to be used from a single port or a group of ports.
- Enables higher port densities per chassis 2x the 100GE capacity and 3x the 40GE capacity.
- A simple fan-out cable allows you to have 3 ports of 40GE QSFP at a lower cost than a new, full load module.
- Multis provide an efficient way to have 100GE using the native physical port of CXP, and then have in the same port of the same card 3x40GE QSFP interfaces. A second card with 40GE QSFP naïve interface is not needed. This saves a slot in your chassis.
- The fan-out technology allows the user to have 100GE/40GE port all emanating from a single card. Compared to traditional Ixia cards, this saves power because you do not have to have two or three different cards in the chassis to perform 100GE/40GE tests.
- Every chassis in the lab produces less heat output to be cooled with less total number of load module installed in the chassis. Multis reduces the number of load modules in the chassis by being:
  - High port density
  - Providing Fan-out technology

#### **Transceivers and Cables**

The Xcellon-Multis family supports optical transceivers and fiber cables for each of the physical interfaces that are supported.

The following are the two types of 3x40GE fan-out cables:

- Active Optical cable (AOC): CXP to (3) QSFP+, fiber, active, fan-out cable.
- Fiber fan-out cable: MTP to (3) MTP QSFP+, fiber, passive, fan-out cable.

## **Active Optical Cable**

The following tables list the specifications of the AOC cable.

CXP to 3-QSFP+ 40GE AOC fan-out

CXP AOC part num- ber	Cable length	Cards/Adapters to Interoperate with
ICD120GVP2420-05	5.0 m	MK, 4x40GE, K2
1110251303	3.0 m	MK, 4x40GE, K2
1110251305	5.0 m	MK, 4x40GE, K2
1110251307	7.0 m	MK, 4x40GE

CXP AOC part num- ber	Cable length	Cards/Adapters to Interoperate with
1110251310	10.0 m	MK, 4x40GE

CXP 100GE Active Optical Cable

CXP AOC part number	Cable length	Cards/Adapters to Interoperate with
FCBGD10CD1C03/ICD120GVP2410- 03	5.0 m	MK, K2
FCBGD10CD1C05/ICD120GVP2410- 05	3.0 m	МК
FCBGD10CD1C10/ICD120GVP2410- 10	5.0 m	МК
FCBGD10CD1C20/ICD120GVP2410- 20	7.0 m	МК

## **Fibre Fan-out Cable**

The following table lists the specifications of the fibre fan-out cable.

MTP to (3) MTP QSFP+, fiber, passive, fan-out

MTP Fan-out part number	Cable length	Cards/Adapters/Optics to Interoperate with
Custom	1.0 m	QSFP optic, MK, 4x40GE, Combo
Custom	3.0 m	QSFP optic, MK, 4x40GE, Combo
Custom	5.0 m	QSFP optic, MK, 4x40GE, Combo
Custom	10.0 m	QSFP optic, MK, 4x40GE, Combo

# Cables used by Multis CXP, QSFP, and QSFP28

The following table lists the cables used by Multis CXP, QSFP, and QSFP28 load modules.

Cables used by Multis CXP, QSFP, and QSFP28

Part number   Media Type   Cable length		Cards on which sup-	
			ported
1-2231368-2	Q28-CR4	5.0 m	QSFP28 Enhanced
2231368-5	Q28-CR4	5.0 m	QSFP28 Enhanced

Part number	Media Type	Cable length	Cards on which sup- ported
2231368-8	Q28-CR4	3.0 m	QSFP28 Enhanced
2231368-1	Q28-CR4	1.0 m	QSFP28 Enhanced
MFA1A00-E003	AOC QSFP28	3.0 m	QSFP28 Enhanced
MCP1600-C002	Passive Copper Cable	2.0 m	QSFP28 Enhanced
IXIA 942-0064	MMF Fiber	3.0 m	Multis CXP
MB-752024-135- 071-343-010M-116	MMF Fiber	10.0 m	Multis CXP
942-0054-01	MMF Fiber	3.0 m	Multis CXP, Multis QSFP
942-0069-01	Copper	3.0 m	Multis QSFP

### **Transceivers**

## **QSFP Transceiver**

QSFP+ 40GE, 40GBASE-SR4 ia an optical, pluggable, MMF, 850nm transceiver is compatible with the load modules Xcellon-Multis XM10/40GE12QSFP+FAN 40-Gigabit Ethernet QSFP load module (944-1105), and Xcellon-Multis XM10/40GE6QSFP+FAN 40-Gigabit Ethernet QSFP (944-1109).

The QSFP+ 40GE, 40GBASE-SR4 transceiver is shown in the following figure:

Figure: QSFP+ 40GE, 40GBASE-SR4 transceiver



QSFP+ 40GE, 40GBASE-LR4, optical, pluggable, SMF, 1310nm transceiver is compatible with the load modules Xcellon-Multis XM10/40GE12QSFP+FAN 40-Gigabit Ethernet QSFP load module (944-1105), and Xcellon-Multis XM10/40GE6QSFP+FAN 40-Gigabit Ethernet QSFP (944-1109).

The QSFP+ 40GE, 40GBASE-LR4 transceiver is shown in the following figure:

Figure: QSFP+ 40GE, 40GBASE-LR4 transceiver



### **CXP**

CXP is useful in the clustering and high-speed computing areas. It is about one-fourth the size of a CFP transceiver providing higher density network interfaces. It is an excellent low cost 100GE system for Multimode fiber cables.

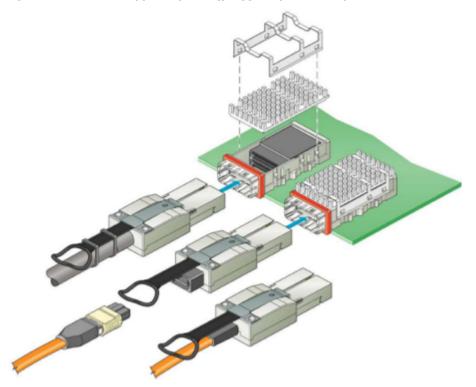
CXP is a copper connector system. It provides twelve 10 Gbps links suitable for 100 Gigabit Ethernet, three 40 Gigabit Ethernet channels, or twelve 10 Gigabit Ethernet channels or a single Infiniband  $12 \times QDR$  link.CXP components are low cost, field proven and available in volume.

The following are the CXP formats:

- · Pluggable transceiver
- Active Optical Cable

The following figure shows the CXP Active Copper, Optical (pluggable), Active Optical:

Figure: CXP Active Copper, Optical (pluggable), Active Optical



#### **OSFP**

The Quad (4-channel) Small Form-factor Pluggable (often abbreviated as QSFP or QSFP+) is a compact, hot-pluggable transceiver used for data communications applications. It interfaces a network device (switch, router, media converter or similar device) to a fiber optic cable.

The QSFP specification supports Ethernet, Fibre Channel, InfiniBand and SONET/SDH standards with different data rate options. QSFP+ transceivers are designed to support Serial Attached SCSI, 40G Ethernet, 20G/40G Infiniband, and other communications standards. QSFP modules increase the port-density by 3x-4x compared to CFP modules.

The following figures show the QSFP+ Pluggable and Cable modules:

Figure: QSFP+ Pluggable module



Figure: QSFP+ Cable module



# Chapter 31 - IXIA Xcellon-Multis Reduced Load Modules

This chapter provides details about Xcellon-Multis Reduced family of load modules-specifications and features.

Ixia's Xcellon-Multis Reduced load module family comprises the industry's highest-density 10GE and 40GE higher speed Ethernet (HSE) test equipment, providing more flexible test coverage at upto 320 10GE ports per chassis, with a dual-rate 40GE/10GE and 40 GE only capability, all in a single-slot load module. Xcellon-Multis provides 10GE fan-out technology that allows a higher-speed port to fan-out to several ports of a lower speed.

The Xcellon-Multis Reduced load modules provide high-density, cost-effective, and flexible 10GE and 40GE capability for testing next-generation multi-terabit networks. You can use them with Ixia applications to quickly and accurately assess the performance and reliability of network solutions before they are deployed.

For more information on Xcellon-Multis family of load modules, see <a href="IXIA Xcellon-Multis">IXIA Xcellon-Multis</a> <a href="Load Modules">Load Modules</a>.

# **Key Features**

The key features of Xcellon-Multis Reduced load modules are as follows:

## Highest- density test module in the industry

- Xcellon-Multis Reduced offers up to 32-ports of 10GE or 12-ports of 40GE interfaces in a single chassis slot
- Up to 320 native 10GE interfaces are supported in Ixia's XG12 rackmount chassis
- With 40GE fan-out enabled, Xcellon-Multis Reduced can support up to 120-ports of 40GE in the XG12 rackmount chassis
- Xcellon-Multis also offers a 40GE only version

#### Fan-out technology

- Provides high-density interfaces over multiple speeds; 10GE and 40GE
- Increases interface flexibility by allowing 10GE and 40GE in mixed speed tests
- Facilitates a wide range of interoperability testing

## **Multi-personality**

- Multi-speed 10GE and 40GE support
- Support for multiple interface types: QSFP+, SFP+ (LC), and MT fiber cable interfaces
- Support for QSFP-to-1x10GE or 4x10GE LC connector interfaces for fiber
- Support for 10GE SFP+ Direct Attach Cable (DAC) 1x10GE or 4x10GE fan-out over passive copper
- 40GBASE-SR4 (multimode) and 40GBASE-LR4 (single mode) optical transceivers
- Facilitates a wide range of 10GE and 40GE interoperability testing.

### Layers 2-7 coverage

- Supports low-range protocol testing for L2-3 routing/switching and data center test cases.
- Provides L4-7 capability for all Xcellon-Multis Reduced load modules.

#### Same feature set across all speeds

- Provides exactly the same data plane features for 10GE and 40GE testing.
- Provides exactly the same L23 protocol coverage for 10GE and 40GE testing.

## Highest ROI of any test and measurement load module

- Density
- · Versatility multiple speeds, multiple interfaces
- Balanced performance and scale
- · Greater test case coverage
- Industry-standard fan-out technology

#### **Cost-effective**

 Reduces total cost of ownership with more ports in a single chassis; 320x10GE or 120x10GE, or 120x40GE ports.

## **Load Modules**

The Xcellon-Multis Reduced family consists of the following models on a single slot card:

- XMR10GE32SFP+FAN: A 32-port module for 10GE operation that can also support 12 ports of 40GE
- XMR10GE16SFP+FAN: A 16-port module for 10GE operation that can also support 6 ports of 40GE
- 40GE fan-out enablement options for XMR10GE32SFP+FAN and XMR10GE16SFP+FAN:
  - XM40GE-FAN-OUT 40GE fan-out option for a new module purchase
  - UPG-XM40GE-FAN-OUT 40GE fan-out field upgrade option for existing load modules
- XMR40GE12QSFP+: A 12-port module for 40GE operation only
- XMR40GE6QSFP+: A 6-port module for 40GE operation only

Each of these load modules are described as follows:

## XMR10GE32SFP+FAN

Xcellon-Multis XMR10GE32SFP is a 10-Gigabit Ethernet load module. It takes up 1-slot with 32-ports 10GE via multimode fan-out cables. It provides L2-7 support and is compatible with XM12 HP rackmount, XM2 desktop, and XG12 rackmount chassis. The following components are available along with the load module:

- 8 each, 3 meter multimode MT-to-4x10GE LC fan-out cables (942-0067)
- 8 each, QSFP+ 40GBASE-SR4 optical transceivers (942-0067)

The XMR10GE32SFP+FAN load module is shown in the following figure:

Figure: Xcellon-Multis Reduced Module-XMR10GE32SFP+FAN



## XMR10GE16SFP +FAN

Xcellon-Multis XMR10GE16SFP+FAN is a 10-Gigabit Ethernet load module. It has 1-slot with 16-ports 10GE via multimode fan-out cables. It provides L2-7 support and is compatible with XM12 HP rackmount, XM2 desktop, and XG12 rackmount chassis.

The following components are available along with the load module:

- 4 each, 3-meter, multimode MT-to-4x10GE LC fan-out cables (942-0067)
- 4 each, QSFP+ 40GBASE-SR4 optical transceivers (948-0031).

The XMR10GE16SFP+FAN load module is shown in the following figure:

Figure: Xcellon-Multis Reduced Module-XMR10GE16SFP+FAN



## **40GE Fan-out options**

The following fan-out options are available for XMR10GE32SFP+FAN and XMR10GE16SFP+FAN:

- XM40GE-FAN-OUT 40GE FACTORY INSTALLED fan-out option This enables 40GE QSFP+ capability and is required on new purchases of the 40GE capability for XMR10GE32SFP+FAN and XMR10GE16SFP+FAN.
- UPG-XM40GE 40GE FIELD UPGRADE fan-out option This enables 40GE QSFP+ capability and is required on upgrade purchases of the 40GE capability for XMR10GE32SFP+FAN and XMR10GE16SFP+FAN.

# XMR40GE12QSFP+

Xcellon-Multis XMR40GE12QSFP+ is a 40-Gigabit Ethernet QSFP+ Reduced load module. It takes up 1-slot with 12-ports of 40GE QSFP+ only. It provides L2-7 support, full featured

L1-3 data plane support and up to 100 protocol emulations per port. The load module is compatible with XM12 HP rackmount, XM2 desktop, and XG12 rackmount chassis.

The following components are required along with the load module:

- One or more QSFP+ 40GBASE-SR4 optical transceivers (948-0031) and MT 12-fiber MMF cable
- 3-meter length (942-0041), or QSFP+ 40GE, 40GBASE-LR4, single mode fiber optical transceiver (948-0032).

The XMR40GE12QSFP+ load module is shown in the following figure:

Figure: Xcellon-Multis Reduced Module-XMR40GE12QSFP+



## XMR40GE6QSFP+

Xcellon-Multis XMR40GE6QSFP+ is a 40-Gigabit Ethernet QSFP+ Reduced load module. It has 1-slot with 6-ports of 40GE QSFP+ only. It provides L2-7 support, full featured L1-3 data plane support and up to 100 protocol emulations per port. The load module is compatible with the XG12 rackmount chassis (940-0005), XM12 HP rackmount chassis (941-0009), and XM2 desktop chassis (941-0003).

The following components are required along with the load module:

- One or more XMR40GE6QSFP+ optical transceivers (948-0031) and MT 12-fiber MMF cable
- 3-meter length (942-0041), or QSFP+ 40GE, 40GBASE-LR4, single mode fiber optical transceiver (948-0032).

The XMR40GE6QSFP+ load module is shown in the following figure:

Figure: Xcellon-Multis Reduced Module-XMR40GE6QSFP+



## **Part Numbers**

Part Numbers for Xcellon-Multis Reduced Load Modules are provided in the following table.

Part Numbers for Xcellon-Multis Modules

Model Number	Part Number	Description
	947-5053	32-ports of 10GE via multimode fan-out cables.
XMR10GE32SFP+FAN		UPG-XM40GE 40GE FIELD UPGRADE option for enabling 40GE QSFP+ capability on upgrade purchases.
	944-1107	XM40GE-FAN-OUT 40GE FACTORY INSTALLED fan- out option for enabling 40GE QSFP+ capability on new purchases.
	947-5054	16-ports of 10GE via multimode fan-out cables.
XMR10GE16SFP+FAN	944-1108	UPG-XM40GE 40GE FIELD UPGRADE option for enabling 40GE QSFP+ capability on upgrade purchases.
	944-1106	XM40GE-FAN-OUT 40GE FACTORY INSTALLED fan- out option for enabling 40GE QSFP+ capability on new purchases.
XMR40GE12QSFP+	944-1114	<ul><li>12-port 40GE with QSFP+</li><li>40GE only</li><li>1 slot</li></ul>
XMR40GE6QSFP+	944-1115	<ul><li>6-port 40GE with QSFP+</li><li>40GE only</li><li>1-slot</li></ul>

# **Specifications**

# Specifications of XMR10GE32SFP+FAN and XMR10GE16SFP+FAN modules

The load module specifications are contained in the following table.

Xcellon-Multis Reduced Load Module Specifications

Model	XMR10GE32SFP+FAN BUNDLE	XMR10GE16SFP+FAN BUNDLE
Part Number	947-5053	947-5054
Hardware Load Module Specific		
Slot/Ports	<ul><li>1 slot:</li><li>32x10GE SFP+ ports (via fan-out)</li><li>40GE fan-out (optional);</li></ul>	<ul><li>1 slot:</li><li>16x10GE SFP+ ports (via fan-out)</li><li>40GE fan-out (optional);</li></ul>

Model	XMR10GE32SFP+FAN BUNDLE	XMR10GE16SFP+FAN BUNDLE
	- 12x40GE ports (1x10GE/port)	- 6x10GE ports (1x10GE/port)
	QSFP 12x40GE (native)	QSFP 6x40GE (native)
Physical Interface	10GE: LC connector (fiber), or SFP+ connector (copper)	10GE: LC connector (fiber), or SFP+ connector (copper)
Chassis Capacity: Maximum Nu	mber of Cards and Ports per	Chassis Model
	10 cards:	10 cards:
XG12 Chassis (940-0005)	<ul> <li>320-ports of 10GE (4x10GE mode)</li> <li>120-ports of 10GE (1x10GE mode)</li> <li>120-ports of 40GE (optional)</li> </ul>	<ul> <li>160-ports of 10GE (4x10GE mode)</li> <li>60-ports of 10GE (1x10GE mode)</li> <li>120-ports of 40GE (optional)</li> </ul>
	8 cards:	8 cards:
XM12 HP Chassis (941-0009	<ul> <li>256-ports of 10GE (4x10GE mode)</li> <li>96-ports of 10GE (1x10GE mode)</li> <li>96-ports of 40GE (optional)</li> </ul>	<ul> <li>128-ports of 10GE (4x10GE mode)</li> <li>48-ports of 10GE (1x10GE mode)</li> <li>48-ports of 40GE (optional)</li> </ul>
	1 card:	1 card:
XM2 Chassis (941-0003)	<ul> <li>32-ports of 10GE (4x10GE mode)</li> <li>12-ports of 10GE (1x10GE mode)</li> <li>12-ports of 40GE (optional)</li> </ul>	<ul> <li>16-ports of 10GE (4x10GE mode)</li> <li>6-ports of 10GE (1x10GE mode)</li> <li>6-ports of 40GE (optional)</li> </ul>
	2 cards:	2 cards:
XGS2-SD Chassis (940-0010)	<ul> <li>64-ports of 10GE (4x10GE mode)</li> <li>24-ports of 10GE (1x10GE mode)</li> <li>24-ports of 40GE (optional)</li> </ul>	<ul> <li>32-ports of 10GE (4x10GE mode)</li> <li>12-ports of 10GE (1x10GE mode)</li> <li>12-ports of 40GE (optional)</li> </ul>
XGS2-HS Chassis	2 cards:	2 cards:
(940-0012)	64-ports of 10GE     (4x10GE mode)	32-ports of 10GE (4x10GE mode)

Model	XMR10GE32SFP+FAN BUNDLE	XMR10GE16SFP+FAN BUNDLE
	<ul><li>24-ports of 10GE (1x10GE mode)</li><li>24-ports of 40GE (optional)</li></ul>	<ul><li>12-ports of 10GE (1x10GE mode)</li><li>12-ports of 40GE (optional)</li></ul>
CPU and Memory	Multicore processors with 40	GB of memory per processor
IEEE Interface Protocols	10GBASE-SR (802.3ae-2002 LR4 (802.3ba-2010)	), 40GBASE-SR4, 40GBASE-
Transceiver Support	QSFP:  • 40GBASE-SR4 (multimo  • 40GBASE-LR4 (single m	•
Operating Temperature Range	41°F to 95°F (5°C to 35°C), 0% to 85%, non-condensing	
	16.8" (L) x 1.3" (W) x 12.0"	
Load Module Dimensions	427mm (L) x 33mm (W) x 305mm (H)	
Load Module Weights	<ul> <li>12-port model:</li> <li>Module only: 12.5 lbs. (5.67 kg)</li> <li>Shipping: 16.2 lbs. (7.35 kg)</li> <li>6 port model:</li> <li>Module only: 9.3 lbs. (4.22 kg)</li> <li>Shipping: 13.1 lbs. (5.94 kg)</li> </ul>	
Transmit Feature Specifications		
Transmit Engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures	
Max. Streams per Port	10GE 32x10 mode: 16 (4x10GE fan-out/port) 10GE 12x10 mode: 32 (1x10GE fan-out/port) 40GE: 32	
Max. Streams per Port in Data Center Ethernet	10GE 32x10 mode: 16 (4x10GE fan-out/port) 10GE 12x10 mode: 32 (1x10GE fan-out/port) 40GE: 32	

Model	XMR10GE32SFP+FAN BUNDLE	XMR10GE16SFP+FAN BUNDLE
Stream Controls	Rate and frame size change on the fly, sequential and advanced stream scheduler	
	10GE:	10GE:
	• 60 bytes (line rate)	60 bytes (line rate)
Minimum Frame Size	• 49 bytes (< line rate)	• 49 bytes (< line rate)
	40GE:	40GE:
	64 bytes (line rate)	64 bytes (line rate)
	• 49 bytes (< line rate)	• 49 bytes (< line rate)
Maximum Frame Size	14,000 bytes	
Maximum Fame Size in Data Center Ethernet	9,216 bytes	
Priority Flow Control	8 line-rate-capable queues with each supporting up to 2,500 byte frame lengths	
,	1 queue supporting up to 9,216 byte frame length	
Frame Length Controls	Fixed, increment by user-defined step, weighted pairs, uniform, repeatable random, IMIX, and Quad Gaussian	
User defined fields (UDF)	Fixed, increment or decrement by user-defined step, sequence, value list, and random configurations. Up to ten, 32-bit wide UDFs are available.	
	40GE: 1 million / UDF	
Value Lists (may )	10GE:	
Value Lists (max.)	1million / UDF(1x10GE mode)	
	• 512K / UDF (4x10GE mode)	
	40GE: 128K / UDF	40GE: 128K / UDF
	10GE:	10GE:
Sequence (max.)	• 128K / UDF (1x10GE mode)	• 128K / UDF (1x10GE mode)
	64K / UDF (4x10GE mode)	• 64K / UDF (4x10GE mode)
Error Generation	Generate good CRC or force bad CRC, undersize and oversize standard Ethernet frame lengths, and bad checksum	
Hardware Checksum Gen-	Checksum generation and verification for IPv4, IP over IP, IGMP/GRE/TCP/UDP, L2TP, GTP	
eration	_	

Model	XMR10GE32SFP+FAN XMR10GE16SFP+FAN BUNDLE BUNDLE
	istics.
Latency Measurement Resolution	40GE and 10GE: 2.5 nanoseconds
Intrinsic Latency Compensation	Removes inherent latency error from port electronics
Transmit line clock adjust- ment	Ability to adjust the parts per million line frequency over a range of -100 ppm to +100 ppm per resource group
Receive Feature Specifications	
Receive Engine	Wire-speed packet filtering, capturing, real-time latency and inter-arrival time for each packet group, with data integrity, sequence and advanced sequence checking capability
Trackable Receive Flows per Port	10GE:  • 128K (1x10GE mode)  • 64K (4x10GE mode)  40GE: 128K (optional)
M: : 5 0:	64 bytes at line rate
Minimum Frame Size	≥ 49 bytes not a line rate
Filters (User-Defined Statistics, UDS)	2 SA/DA pattern matchers, 2x16-byte user-definable patterns with offsets capability for start of: frame, IP, or protocol. Up to 6 UDS counters are available
Hardware Capture Buffer per Port or Resource Group	<ul> <li>10GE:</li> <li>1x10GE mode: 2GB per 1 user-selected link of the 1x10GE fan-out link resource group</li> <li>4x10GE: 256MB/port for all ports in the fan-out of the resource group</li> <li>40GE: 2GB per 1, user-selected port/resource group (optional)</li> </ul>
Statistics and Rates	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 user-defined stats, capture trigger (UDS 3), capture filter (UDS 4), 8 QoS counters, data integrity frames, data integrity errors, sequence and advanced sequence checking frames, sequence checking errors, ARP, and PING requests and replies

Model	XMR10GE32SFP+FAN XMR10GE16SFP+FAN BUNDLE BUNDLE	
PCS Lanes Port Statistics	PCS Sync Errors, Illegal Codes, Remote Faults, Local Faults, Illegal Ordered Set, Illegal Idle, Illegal SOF, Out Of Order SOF, Out Of Order EOF, Out Of Order Data, Out Of Order Ordered Set	
Latency / Jitter Measurements	Cut-through, store & forward, forwarding delay, up to 16 time bins latency/jitter, MEF jitter, and inter-arrival time	
	<b>Routing:</b> RIP, RIPng, OSPFv2/v3, ISISv4/v6, EIGRP, EIGRPv6, BGP/BGP+	
	<b>MPLS:</b> RSVP-TE, RSVP-TE P2MP, LDP, mLDP, BGP RFC 3107, MPLS-TP, MPLS OAM	
L2/3 Routing, Bridging, and Timing	MPLS VPN: L2VPN PW, L3VPN/6VPE, 6PE, VPLS-LDP, VPLS-BGP, VPLS-BGP AD and LDP FEC 129, Inter-AS VPN Option A, B, and C, Seamless MPLS, Carrier Supporting Carrier (CsC), GRE mVPN, NG MVP (mLDP and RSVP-TE P2MP), EVPN/PBB-EVPN	
	<b>High-Availability:</b> BFD, Graceful Restart, MPLS Ping/TraceRoute, LSP BFD, VCCV BFD, Real-time dynamic label swap for convergence time measurement up to millisecond accuracy	
	IP Multicast: IGMPv1/v2/v3, MLDv1/v2, PIM-SM/SSM, PIM-BSR, multicast VPN	
	<b>Switching:</b> STP/RSTP, MSTP, PVST+/RPVST+, LACP, LLDP, Protocols over LACP Bundle	
	Carrier Ethernet: Link OAM, CFM, Service OAM, PBT/PBB-TE, SyncE, PTP (1588v2), E-LMI	
Data Center Ethernet	Priority Class-Based Flow Control (IEEE802.1Qbb), FCoE/ FIP, LLDP/DCBX, VNTAG/VIC, OpenFlow, Fab- ricPath, TRILL, SPBM, VEPA, VXLAN	
Broadband Access	<b>Broadband:</b> ANCP, PPPoX, DHCPv4 client/server, DHCPv6 client/server, L2TPv2, Radius Attributes for L2TP, Dual-Stack PPPoX, AMT	
	Authentication: 802.1x, WebAuth, Cisco NAC	
Layer 2-7 Protocol Support (32x10GE Fan-out mode)		
	<b>Routing</b> : RIP, RIPng, OSPFv2/v3, ISISv4/v6, EIGRP, EIGRPv6, BGP/BGP+	
L2/3 routing, bridging and timing	MPLS: RSVP-TE, RSVP-TE P2MP, LDP, mLDP	
5	MPLS VPN: L3VPN/6VPE, 6PE , VPLS-LDP, VPLS-BGP, VPLS-BGP AD and LDP FEC 129, NG mVPN (mLDP and	

Model	XMR10GE32SFP+FAN BUNDLE	XMR10GE16SFP+FAN BUNDLE
	RSVP-TE P2MP), PWE3	
	High-Availability: BFD	
	IP Multicast: IGMPv1/v2/v3, MLDv1/v2, PIM-SM/SSM, multicast VPN	
	Switching: STP/RSTP, MSTP, PVST/PVST+/RPVST+	
	Carrier Ethernet: Link OAM, CFM/ Y.1731, PBB-TE, SyncE, PTP (1588v2), E-LMI	
Data center Ethernet	FCoE, DCBX, VNTAG/VIC, OpenFlow, FabricPath, TRILL, SPBM, VEPA, VXLAN, DHCPv4 over VXLAN over IPv4, DHCPv6 over VXLAN over IPv4, IPv4 over VXLAN over IPv4, IPv6 over VXLAN over IPv4, IGMP over VXLAN over IPv4, MLD over VXLAN over IPv4	
Broadband access	DHCPv4 client/server, DHCF	Pv6 client/server

# Specifications of Multis Reduced Modules with 40GE only capability

The load module specifications for the modules with 40GE only capability are contained in the following table.

Xcellon-Multis Reduced 40GE Load Module Specifications

Model Name	XMR40GE12QSFP+	SMR40GE6QSFP+
Part Number	944-1114	944-1115
Hardware Load Module Specifications		
	1-slot	1-slot:
Slot/Ports	12x40GE ports (1x10GE/port)	6x10GE ports (1x10GE/port)
Physical Interface	QSFP 12x40GE (native)	QSFP 6x40GE (native)
Chassis Capacity: Maximum Number of Cards and Ports per Chassis Model		
XG12 Chassis	10 cards:	10 cards:
(940-0005)	• 120-ports of 40GE	60-ports of 40GE
XM12 HP Chassis	8 cards:	8 cards:
(941-0009	96-ports of 40GE	48-ports of 40GE
XM2 Chassis	1 card:	1 card:
(941-0003)	• 12-ports of 40GE	6-ports of 40GE

Model Name	XMR40GE12QSFP+	SMR40GE6QSFP+
XGS2-SD Chassis	2 cards:	2 cards:
(940-0010)	• 24-ports of 40GE	• 12-ports of 40GE
XGS2-HS Chassis	2 cards:	2 cards:
(940-0012)	• 24-ports of 40GE	• 12-ports of 40GE
CPU and Memory	Multicore processors with processor	n 4GB of memory per
IEEE Interface Protocols	40GBASE-SR4, 40GBASE	-LR4 (802.3ba-2010)
	QSFP:	
Transceiver Support	<ul><li>40GBASE-SR4 (mult</li><li>40GBASE-LR4 (single</li></ul>	·
One wating Temporature Dange	41°F to 95°F (5°C to 35°C	C), ambient air
Operating Temperature Range	0% to 85%, non-condens	sing
Load Module Dimensions	16.8" (L) x 1.3" (W) x 12.0" (H)	
Load Module Differisions	427mm (L) x 33mm (W) x 305mm (H)	
	12-port model:	
	Module only: 12.5 lbs. (5.67 kg)	
Load Module Weights	• Shipping: 16.2 lbs. (	7.35 kg)
	6 port model:	(4.22 l)
	<ul><li>Module only: 9.3 lbs</li><li>Shipping: 13.1 lbs. (</li></ul>	, -,
Transmit Feature Specifications		
Transmit Engine	Wire-speed packet gener sequence numbers, data and packet group signatu	integrity signature,
Max. Streams per Port	40GE: 32	
Max. Streams per Port in Data Center Ethernet	40GE: 32	
Stream Controls	Rate and frame size char tial and advanced stream	
	40GE:	
Minimum Frame Size	• 64 bytes (line rate)	
	• 49 bytes (< line rate	2)
Maximum Frame Size	14,000 bytes	

Model Name	XMR40GE12QSFP+ SMR40GE6QSFP+
Maximum Fame Size in Data Center Ethernet	9,216 bytes
	8 line-rate-capable queues with each supporting up to 2,500 byte frame lengths
Priority Flow Control	1 queue supporting up to 9,216 byte frame lengths
Frame Length Controls	Fixed, increment by user-defined step, weighted pairs, uniform, repeatable random, IMIX, and Quad Gaussian
User defined fields (UDF)	Fixed, increment or decrement by user-defined step, sequence, value list, and random configurations. Up to ten, 32-bit wide UDFs are available.
Value Lists (max.)	40GE: 1 million / UDF
Sequence (max.)	40GE: 128K / UDF
Error Generation	Generate good CRC or force bad CRC, undersize and oversize standard Ethernet frame lengths, and bad checksum
Hardware Checksum Generation	Checksum generation and verification for IPv4, IP over IP, IGMP/GRE/TCP/UDP, L2TP, GTP
Link Fault Signaling	Reports, no fault, remote fault, and local fault port statistics.
Latency Measurement Resolution	40GE: 2.5 nanoseconds
Intrinsic Latency Compensation	Removes inherent latency error from port electronics
Transmit line clock adjustment	Ability to adjust the parts per million line frequency over a range of -100 ppm to +100 ppm per resource group
Receive Feature Specifications	
Receive Engine	Wire-speed packet filtering, capturing, real- time latency and inter-arrival time for each packet group, with data integrity, sequence and advanced sequence checking capability
Trackable Receive Flows per Port	40GE: 128K (optional)
Minimum Frame Size	64 bytes at line rate
Pililillulli i i aille Size	≥ 49 bytes not a line rate
Filters (User-Defined Statistics, UDS)	2 SA/DA pattern matchers, 2x16-byte user-

Model Name	XMR40GE12QSFP+ SMR40GE6QSFP+
	definable patterns with offsets capability for start of: frame, IP, or protocol. Up to 6 UDS counters are available
Hardware Capture Buffer per Port or Resource Group	40GE: 2GB per 1, user-selected port/resource group
Statistics and Rates	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 user-defined stats, capture trigger (UDS 3), capture filter (UDS 4), 8 QoS counters, data integrity frames, data integrity errors, sequence and advanced sequence checking frames, sequence checking errors, ARP, and PING requests and replies
PCS lanes port statistics (40GE mode only)	PCS Sync Errors, Illegal Codes, Remote Faults, Local Faults, Illegal Ordered Set, Illegal Idle, Illegal SOF, Out Of Order SOF, Out Of Order EOF, Out Of Order Data, Out Of Order Ordered Set
Latency / Jitter Measurements	Cut-through, store & forward, forwarding delay, up to 16 time bins latency/jitter, MEF jitter, and inter-arrival time
Layer 2-7 Protocol Support (40GE mode	2)
	Routing: RIP, RIPng, OSPFv2/v3, ISISv4/v6, EIGRP, EIGRPv6, BGP/BGP+
	MPLS: RSVP-TE, RSVP-TE P2MP, LDP, mLDP, BGP RFC 3107, MPLS-TP, MPLS OAM
L2/3 Routing, Bridging, and Timing	MPLS VPN: L2VPN PW, L3VPN/6VPE, 6PE, VPLS-LDP, VPLS-BGP, VPLS-BGP AD and LDP FEC 129, Inter-AS VPN Option A, B, and C, Seamless MPLS, Carrier Supporting Carrier (CsC), GRE mVPN, NG MVP (mLDP and RSVP-TE P2MP), EVPN/PBB-EVPN
	High-Availability: BFD, Graceful Restart, MPLS Ping/TraceRoute, LSP BFD, VCCV BFD, Real-time dynamic label swap for convergence time measurement up to millisecond accuracy
	IP Multicast: IGMPv1/v2/v3, MLDv1/v2, PIM-SM/SSM, PIM-BSR, multicast VPN
	<b>Switching:</b> STP/RSTP, MSTP, PVST+/RPVST+, LACP, LLDP, Protocols over LACP Bundle
	Carrier Ethernet: Link OAM, CFM, Service

Model Name	XMR40GE12QSFP+ SMR40GE6QSFP+
	OAM, PBT/PBB-TE, SyncE, PTP (1588v2), E-LMI
Data Center Ethernet	Priority Class-Based Flow Control (IEEE802.1Qbb), FCoE/ FIP, LLDP/DCBX, VNTAG/VIC, OpenFlow, FabricPath, TRILL, SPBM, VEPA, VXLAN
Broadband Access	Broadband: ANCP, PPPoX, DHCPv4 client/server, DHCPv6 client/server, L2TPv2, Radius Attributes for L2TP, Dual-Stack PPPoX, AMT  Authentication: 802.1x, WebAuth, Cisco NAC

# **Application Support**

The Ixia application support for Xcellon-Multis Reduced load modules is provided in the following table:

Xcellon-Multis Reduced Load Module Application Support

Application	Support
IxNetwork	Provides wire-rate traffic generation with service modeling that builds realistic, dynamically-controllable data-plane traffic. IxNetwork offers the industry's best test solution for functional and performance testing by using comprehensive emulation for routing, switching, MPLS, IP multicast, broadband, authentication, Carrier Ethernet, and data center Ethernet protocols.
IxExplorer	Layer 2-3 wire-speed traffic generation and analysis.
Tcl API	Custom user script development for layer 1-7 testing.

# **Fan-out Capability**

The following are the new fan-out capabilities of the Multis Reduced load module:

- 32x10GE fan-out This is a new capability that provides up to 32 independent 10GE QSFP+ links or generic 10GE fiber links.
- 16x10GE fan-out This is a new capability that provides up to 16 independent 10GE QSFP+ links or generic 10GE fiber links.

There are up to four 10GE links provided via a cable per physical port. For XMR10GE32SFP+FAN, we use 8 of the 12 ports which equals 32x10GE SFP+ports. For more information, see <u>XMR10GE32SFP+FAN</u>. For XMR10GE16SFP+FAN, we use 4 of the 6 ports which equals 16x10GE SFP+ports. For more information, see <u>XMR10GE16SFP+FAN</u>.

#### **Transceivers**

The Xcellon-Multis Reduced family supports optical transceivers and fiber cables for the physical interfaces that are supported.

#### QSFP+ 40GE, 40GBASE-SR4 Transceiver

QSFP+ 40GE, 40GBASE-SR4 ia an optical, pluggable, MMF, 850nm transceiver is compatible with the following load modules:

- Xcellon-Multis XMR10GE32SFP+FAN 40-Gigabit Ethernet QSFP load module (944-1105)
- Xcellon-Multis XMR10GE16SFP+FAN 40-Gigabit Ethernet QSFP (944-1109)

The QSFP+ 40GE, 40GBASE-SR4 transceiver is shown in the following figure:

Figure: QSFP+ 40GE, 40GBASE-SR4 transceiver



#### QSFP+ 40GE, 40GBASE-LR4 Transceiver

QSFP+ 40GE, 40GBASE-LR4, optical, pluggable, SMF, 1310nm transceiver is compatible with the load modules Xcellon-Multis XM10/40GE12QSFP+FAN 40-Gigabit Ethernet QSFP load module (944-1105), and Xcellon-Multis XM10/40GE6QSFP+FAN 40-Gigabit Ethernet QSFP (944-1109).

The QSFP+ 40GE, 40GBASE-LR4 transceiver is shown in the following figure:

Figure: QSFP+ 40GE, 40GBASE-LR4 transceiver



# **Fan-out Cable Options**

The Xcellon-Multis Reduced load module cable options are described in the following sections.

## QSFP+ 40GBASE-SR4 40GE active optical parallel fiber cable

The QSFP+ 40GBASE-SR4 40GE active optical parallel fiber cable assembly has the following features:

- OM3 Multimode Fiber (MMF) 850nm
- 3-meter length

This cable is compatible with the following load modules:

- Xcellon-Multis XMR10GE32SFP+FAN 40-Gigabit Ethernet QSFP load module (944-1105)
- Xcellon-Multis XMR10GE16SFP+FAN 40-Gigabit Ethernet QSFP load module (944-1109)

The QSFP+ 40GBASE-SR4 40GE active optical parallel fiber cable is shown in the following figure:

Figure: QSFP+ 40GBASE-SR4 40GE active optical parallel fiber cable



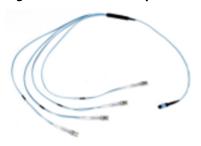
#### MT-to-4x10GE LC fan-out, MMF 3-meter

MT-to-4x10GE LC fan-out, MMF, 3-meter cable requires QSFP 40GBASE-SR4, pluggable, transceiver, 850nm, MMF (948-0031). The cables and transceiver are compatible with the following load modules:

- Xcellon-Multis XMR10GE32SFP+FAN 40-Gigabit Ethernet QSFP load module (944-1105)
- Xcellon-Multis XMR10GE16SFP+FAN 40-Gigabit Ethernet QSFP load module (944-1109).

The MT-MT 4x10GE passive fiber fan-out cable is shown in the following figure:

Figure: MT-MT 4x10GE passive fiber fan-out cable



#### MT-to-4x10GE LC fan-out, MMF 5-meter

MT-to-4x10GE LC fan-out, MMF, 5-meter cable requires QSFP 40GBASE-SR4, pluggable, transceiver, 850nm, MMF (948-0031). The cables and transceiver are compatible with the following load modules:

- Xcellon-Multis XMR10GE32SFP+FAN 40-Gigabit Ethernet QSFP load module (944-1105)
- Xcellon-Multis XMR10GE16SFP+FAN 40-Gigabit Ethernet QSFP load module (944-1109).

The MT-MT 4x10GE SFP+ direct attach cable is shown in the following figure:

Figure: MT-MT 4x10GE passive fiber fan-out cable



### QSFP-to-4x10GE SFP+ Direct Attach Cable (DAC)

QSFP-to-4x10GE SFP+ Direct Attach Cable (DAC) is a passive copper, fan-out, cable that is 3-meter in length. This cable is compatible with the following load modules:

- Xcellon-Multis XMR10GE32SFP+FAN 40-Gigabit Ethernet QSFP load module (944-1105)
- Xcellon-Multis XMR10GE16SFP+FAN 40-Gigabit Ethernet QSFP load module (944-1109).

NOTE

The load modules must have the 10GE fan-out option enabled to use this cable. This requires 905-1000 XM10GE-FAN-OUT 10GE fan-out option for NEW purchases of Xcellon-Multis load modules, or the 905-1001 UPG-XM10GE-FAN-OUT 10GE fan-out option UPGRADE for existing Xcellon-Multis load modules.

The QSFP-to-4x10GE SFP+ Direct Attach Cable (DAC) cable is shown in the following figure:

Figure: QSFP-to-4x10GE SFP+ Direct Attach Cable (DAC) cable



## QSFP-to-QSFP 40GE 40GBASE-CR4 Direct Attach Cable (DAC)

QSFP-to-QSFP 40GE 40GBASE-CR4 Direct Attach Cable (DAC) is a passive copper, point-to-point cable that is 3-meter in length. This cable is compatible with the following load modules:

- Xcellon-Multis XMR10GE32SFP+FAN 40-Gigabit Ethernet QSFP load module (944-1105)
- Xcellon-Multis XMR10GE16SFP+FAN 40-Gigabit Ethernet QSFP load module (944-1109).

The QSFP-to-QSFP 40GE 40GBASE-CR4 Direct Attach Cable (DAC) is shown in the following figure:

Figure: QSFP-to-QSFP 40GE 40GBASE-CR4 Direct Attach Cable (DAC)





# Chapter 32 - IXIA Novus QSFP28 Load Modules

This chapter provides details about Novus family of load modules and their specifications and features.

Novus is a next generation, high density, 8-port, native QSFP28 100/25GbE load module. This load module family supports the test needs of both high-density, multi-rate switch/router makers and the organizations implementing the network equipment. Novus supports eight native QSFP28 100GbE ports and up to 32 ports for 25GbE per load module, and enables interoperability and functional testing, as well as high-port count performance testing. Its native QSFP28 100GbE interfaces with 25GbE speed and fan-out cable support, that provides a more efficient and flexible set of 100/25GbE test use cases.

## **Key Features**

The key features of Novus load module are as follows:

- Supports multi-vendor interoperability 100GbE and 25GbE testing between speeds that run over these QSFP28 optical transceivers, Active Optical Cables and 100GBASE-CR4 passive copper Direct Attach Cable media:
  - Multimode 100GBASE-SR4 and single-mode 100GBASE-LR4
  - Multimode 25GBASE-SR and copper 25GBASE-CR
- Supports mid-range protocol testing for L2/3 routing/switching and data center test cases with the Ixia's IxNetwork application
- Supports traffic and protocol scale and benchmark performance stress tests to ensure error-free network data transmission with long-term stability and high reliability at full 100GbE and 25GbE line rate
- Provides 100Gb/s and 25Gb/s line rate packet capture and decode tools to detect and de-bug data transmission errors
- Provides an excellent test platform for full line rate 100Gb/s to evaluate the new 100GbE ASIC designs, FPGAs, and hardware switch fabrics that use the new 4x25Gb/s electrical interface
- Supports benchmarking of the data plane and protocol emulation performance and scale of ultra-high-density 100/25GbE-capable network equipment using industrystandard RFC benchmark tests in test beds with hundreds of 100GbE and/or 25GbE ports in a single test
  - 25GbE speed support (requires purchase of the 25GbE load module option):
    - Support for independent 25GbE virtual and physical fan-out configurations including: 4x25GbE
    - Up to 4x25GbE links over single point-to-point 100GbE cable media (MT-MT, AOC, or DAC media)
- Underlying support for advanced features such as: Ethernet Forward Error Correction, auto-negotiation, and link training on 100GbE and 25Gbe
- Provides a broad range of application support including: IxExplorer, IxNetwork, and the related Tcl and automation APIs.

#### **Load Modules**

The Novus family consists of the following model on a single slot card:

- NOVUS100GE8Q28+FAN
- NOVUS100GE8Q28+FAN+25G

The load module is described as follows:

## NOVUS100GE8Q28+FAN

NOVUS100GE8Q28+FAN is a 100 Gigabit Ethernet full-featured load module. It has 1-slot with 8-ports with the native QSFP28 physical interface. It provides L2-3 support and is compatible with the XGS12-SD rack mount chassis (940-0011), XGS12-HS rack mount chassis (940-0006), XGS12-HSL, 12-slot high speed rackmount chassis (940-0016), XGS2-SD 2-slot standard performance chassis (940-0010), 2-slot high performance chassis XGS2-HS chassis (940-0012), and the XGS2-HSL, 2-slot high performance chassis (940-0014).

The NOVUS100GE8Q28+FAN load module is shown in the following figure:

Figure: Novus Module-NOVUS100GE8Q28+FAN



# 4x25G options for NOVUS100GE8Q28+FAN

4x25G options for NOVUS100GE8Q28+FAN is available in two forms:

- Factory Installed
- · Field Upgrade

## 4x25GbE factory installed

The 4x25GbE Fan-Out FACTORY INSTALLED option for the NOVUS100GE8Q28+FAN load module enables 4x25GbE capability on all eight 100GbE QSFP28 ports on the module. The 4x25GbE capability is per 100GE port and is ONLY supported over a single 100GbE point-to-point QSFP28 cable where each channel of the cable is rated for 25GbE per channel operation. This is ONLY supported on the NOVUS100GE8Q28+FAN (944-1140) load module.

NOTE

The factory installed option is required for new purchases of the 4x25GbE capability for the NOVUS100GE8Q28+FAN load module with native QSFP28 8x100GbE physical interfaces.

### 4x25GbE field upgrade

The 4x25GbE Fan-Out FIELD UPGRADE option for the NOVUS100GE8Q28+FAN load module enables 4x25GbE capability on all eight 100GbE QSFP28 ports on the module. The 4x25GbE capability is per 100GbE port and is ONLY supported over a single 100GbE point-to-point QSFP28 cable where each channel of the cable is rated for 25GbE per channel operation. This is ONLY supported on the NOVUS100GE8Q28+FAN (944-1140) load module.

NOTE

The field upgrade option is required on field upgrade purchases of the 4x25GbE capability for the NOVUS100GE8Q28+FAN load module with native QSFP28 8x100GbE physical interfaces. Please provide the serial number of the desired load module at the time of placement of order, to install the option .

## Novus 4x25GbE capability through 25GbE license

25GbE option can be upgraded in the following Novus load module through license. By default, the ports are in 100GbE mode for this load module.

• NOVUS100GE8Q28+FAN (944-1140)

### **Part Numbers**

Part Numbers for Novus Load Module and Supported Adapters are provided in the following table.

Part Numbers for Novus Modules

Model Number	Part Num- ber	Description
NOVUS100GE8Q28+FAN	944-1144	<ul> <li>8-ports of 100GbE with the QSFP28 physical interface</li> <li>100GbE only</li> </ul>
NOVUS100GE8Q28+FAN	944-1140	<ul> <li>8-ports of 100GbE with the QSFP28 physical interface</li> <li>100GbE and 25GbEonly</li> </ul>
		4x25GbE factory installed option for NOVUS100GE8Q28+FAN load module (944-1140)
		Enables 4x25GbE capability on all eight 100GbE QSFP28 ports on the module
	905-1007	Supported over a single 100GbE point- to-point QSFP28 cable where each chan- nel of the cable is rated for 25GbE per channel operation
		Supports Auto Negotiation and RS-FEC for 100GbE and 25GbE
	905-1008	The 4x25GbE field upgrade option for NOVUS100GE8Q28+FAN load module (944-1140)

Model Number	Part Num- ber	Description
		Enables 4x25GbE capability on all eight 100GbE QSFP28 ports on the module
		<ul> <li>Supported over a single 100GbE point- to-point QSFP28 cable where each chan- nel of the cable is rated for 25GbE per channel operation</li> </ul>
		Supports Auto Negotiation and RS-FEC for 100GbE and 25GbE

# **Specifications**

The load module specifications are contained in the following table.

Novus Load Module Specifications

Feature	NOVUS100GE8Q28+FAN	
Hardware Load Module Specifications		
Slot / Number of Ports	1-slot / 8x100GE native QSFP28 ports and up to 32x25GbE ports via fan-out media	
Physical Interface	Native QSFP28	
Supported Port Speeds	<ul> <li>100GbE/port: 100GbE-capable fiber and passive copper cable media</li> <li>4x25GbE/port: 25GbE-capable fiber and passive copper point-point and fan-out cable media</li> </ul>	
CPU and Memory	Multicore processor with 2GB of CPU memory per port	
IEEE Interface Protocols	<ul> <li>IEEE 802.3 100GBASE-R</li> <li>IEEE 802.3bj</li> <li>IEEE 802.3bm</li> <li>IEEEP802.3by (draft specification 3.2)</li> </ul>	
25G Consortium spe- cification	25GbE: Compatible with version 1.5	
Advanced Layer 1 support	<ul> <li>25GbE:</li> <li>Auto-negotiation (AN), Clause 73 for passive copper DAC</li> <li>Link Training(LT) for 25GE copper DAC media (Clause 93, 110)</li> <li>Ethernet Forward Error Correction: BASE-R, Clause 74 and RS FEC, Clause 108</li> <li>FEC statistics: FEC Corrected and Uncorrected Codeword Counts</li> </ul>	

Feature	NOVUS100GE8Q28+FAN
	<ul> <li>Ability to independently turn ON or OFF AN with Link training, or FEC, or to allow IEEE defaults to automatically manage the interoperability</li> <li>Independent fan-out ports with physical fan-out media for up to 4x25GE per QSFP28 port</li> </ul>
	100GbE:
	<ul> <li>Auto-negotiation (AN, Clause 73 for copper DAC)</li> <li>Link training for 100GbE copper cable media (Clause 93)</li> </ul>
	<ul> <li>Ethernet Forward Error Correction (RS-FEC, Clause 91)</li> <li>FEC statistics: RS-FEC Corrected and Uncorrected Codeword Counts</li> </ul>
	<ul> <li>Ability to independently turn ON or OFF AN with and Link Training, or FEC, or to allow IEEE defaults to auto- matically manage the interoperability. AN needs to be turned on to enable Link Training</li> </ul>
Tuo no oci von Cumant	<ul> <li>100GBASE-SR4 and 4x25GBASE-SR QSFP28 for multimode fiber</li> <li>Pluggable transceiver</li> <li>25GbE speed support requires a point-to-point or a fan-out cable</li> </ul>
Transceiver Support	■ Active Optical Cable (AOC)  NOTE  ■ This transceiver supports the 25GbE speed (NOVUS 25GbE FAN-OUT Option 905-1007, and the NOVUS 25GbE FAN-OUT-UPG FIELD UPGRADE Option 905-1008) on the NOVUS100GE8Q28+FAN load module
	100GBASE-SR4 multimode fiber Active Optical Cable (AOC) and MT-MT 12-fiber point-to-point cables for QSFP28
Cable Media	100GBASE-CR4, passive, copper Direct Attached Cable (DAC) up to 5 meters in length; note: requires RS-FEC to be enabled
	<ul> <li>25GBASE-SR multimode fiber Optical Cable (AOC) and MT-MT 12-fiber point-to-point cable for QSFP28, 3 meter length is available</li> </ul>
	<ul> <li>25GBASE-SR multimode fiber MT-to-4xLC fan-out cable for QSFP28, 3 meter and 5 meter lengths are available</li> <li>25GBASE-CR passive, copper Direct Attached Cable (DAC) point-point, up to 5 meters in length; Note: Requires BASE-R FEC Clause 74 to be enabled</li> </ul>
	25GBASE-CR passive, copper Direct Attached Cable (DAC) QSFP28-to-4xSFP28 fan-out media, up to 5

Feature	NOVUS100GE8Q28+FAN
	meters in length; Note: Requires BASE-R FEC Clause 74 to be enabled
	When operating in 25GbE mode, the only supported Direct Attached Copper (DAC) cables are the ones that respect the compliance code for CA-L, CA-S or CA-N cable assembly type. If cables without compliance code are used, link will not be established on IXIA equipment side.
	<ul> <li>942-0067: MT-to-4x10GbE LC fan-out, MMF, 3-meter cable for 10GbE and 25GbE fan-out. For 4x25GbE fan-out it requires a 100GBASE-SR4 QSFP28 100GBASE-SR4 100GbE pluggable transceiver, 850nm, MMF (QSFP28-SR4-XCVR).</li> <li>942-0068: MT-to-4x10GbE LC fan-out, MMF, 5-meter cable for 10GbE and 25GbE fan-out. For 4x25GbE fan-</li> </ul>
	out it requires a 100GBASE-SR4 QSFP28 100GBASE-SR4 100GbE pluggable transceiver, 850nm, MMF (QSFP28-SR4-XCVR).
Cables	• 942-0088: QSFP28 passive, copper, Direct Attach Cable (DAC), 3-meter length for Xcellon-Multis XM100GE4QSFP28+ENH 100GE load module (944-1117) and the NOVUS100GE8Q28+FAN, 8-port, QSFP28 100GbE load module (944-1140).
	<ul> <li>942-0092: QSFP28 Active Optical Cable (AOC), multimode fiber, 850nm, 3-meter length. Compatible with the Xcellon-Lava CFP-to-QSFP28 interface adapter (948-0029), Xcellon-Multis XM100GE4QSFP28+ENH 100-Gigabit Ethernet, Enhanced load module (944-1117) and the NOVUS100GE8Q28+FAN, 8-port, QSFP28 100GbE load module (944-1140).</li> </ul>
Load Module Dimensions	17.3" (L) x 1.3" (W) x 12.0" (H)
Load Module Difficustrisions	440mm (L) x 33mm (W) x 305mm (H)
Load Module Weights	Module only: 11.8 lbs. (5.35 kg)
	Shipping: 18.6 lbs. (8.44 kg)
Temperature	Operating: 41°F to 95°F (5°C to 35°C)
	Storage: 41°F to 122°F (5°C to 50°C)
Humidity	Operating: 0% to 85%, non-condensing
,	Storage: 0% to 85%, non-condensing
Chassis Capacity: Maxii	mum Number of Cards and Ports per Chassis Model
XGS12-SD Chassis (940-	12 load modules:

Feature	NOVUS100GE8Q28+FAN
0011)	<ul><li>Rackmount chassis</li><li>96-ports of 100GbE</li><li>384-ports of 25GbE</li></ul>
XGS12-HS Chassis (940- 0006)	12 load modules:  Rackmount chassis 96-ports of 100GbE 384-ports of 25GbE
XGS12-HSL Chassis (940- 0016)	12 load modules:  Rackmount chassis 96-ports of 100GbE 384-ports of 25GbE
XGS2-SD Chassis (940- 0010)	2 load modules:  • Desktop chassis  • 16-ports of 100GbE  • 64-ports of 25GbE
XGS2-HS Chassis (940- 0012)	<ul><li>2 load modules:</li><li>Desktop chassis</li><li>16-ports of 100GbE</li><li>64-ports of 25GbE</li></ul>
XGS2-HSL Chassis (940- 0014)	2 load modules:  Rackmount chassis  16-ports of 100GbE  64-ports of 25GbE
Transmit Feature Speci	fications
Transmit Engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures
Max. Streams per Port	<ul><li>100GbE: 32</li><li>25GbE: 16</li></ul>
Max. Streams per Port in Data Center Ethernet	<ul><li>100GbE: 32</li><li>25GbE: 16</li></ul>
Stream Controls	Rate and frame size change on the fly, sequential and advanced stream scheduler
Minimum Frame Size	100GbE and 25GbE:  • 6 bytes at full line rate

Feature	NOVUS100GE8Q28+FAN
	49 bytes at less than full line rate
Maximum Frame Size	14,000 bytes
Maximum Fame Size in Data Center Ethernet	9,216 bytes
Priority Flow Control	<ul> <li>8 line-rate-capable queues with each supporting up to 2,500 byte frame lengths</li> <li>1 queue supporting up to 9,216 byte frame lengths</li> </ul>
Frame Length Controls	Fixed, increment by user-defined step, weighted pairs, uniform, repeatable random, IMIX, and Quad Gaussian
User defined fields (UDF)	Fixed, increment or decrement by user-defined step, sequence, value list, and random configurations. Up to ten, 32-bit wide UDFs are available.
Value Lists (max.)	100GbE and 25GbE: 1M / UDF
Sequence (max.)	<ul><li>100GbE: 8K / UDF</li><li>25GbE: 2K/UDF</li></ul>
Error Generation	Generate good CRC or force bad CRC, undersize and over- size standard Ethernet frame lengths, and bad checksum
Hardware Checksum Generation	Checksum generation and verification for IPv4, IP over IP, IGMP/GRE/TCP/UDP, L2TP, GTP
Link Fault Signaling	Reports, no fault, remote fault, and local fault port statistics; generate local and remote faults with controls for the number of faults and order of faults, plus the ability to select the option to have the transmit port ignore link faults from a remote link partner.
Latency Measurement Resolution	100GbE and 25GbE: 2.5 nanoseconds
Intrinsic Latency Compensation	Removes inherent latency error from the 100GbE port electronics
Transmit line clock adjust- ment	Ability to adjust the parts per million line frequency over a range of -100 ppm to $+100$ ppm across all 100GbE ports on the load module. This applies to all ports when in 25GbE speed mode.
Receive Feature Specifi	cations
Receive Engine	Wire-speed packet filtering, capturing, real-time latency and inter-arrival time for each packet group, with data integrity, sequence and advanced sequence checking capability
Trackable Receive Flows per Port	100GbE:

Feature	NOVUS100GE8Q28+FAN
	<ul><li> 32K limited statistics mode</li><li> 4K full statistics mode</li></ul>
	25GbE:
	<ul> <li>8K limited statistics mode</li> <li>2K full statistics mode</li> <li>4K PGIDs in non-TxRxSynch mode</li> <li>2K PGIDs in TxRxSynch mode</li> </ul>
	100GbE and 25GbE:
Minimum Frame Size	<ul><li>60 bytes at full line rate</li><li>64 bytes at full line rate into the capture buffer</li><li>49 bytes at less than full line rate</li></ul>
Filters (User-Defined Statistics, UDS)	2 SA/DA pattern matchers, 2x16-byte user-definable patterns with offsets capability for start of: frame, IP, or protocol. Up to 6 UDS counters are available.
Hardware Capture Buffer per Port or Resource Group	100GbE and 25GbE: There are two 512MB per capture buffers on the card; user can select which port and/or resource group each capture buffer may be assigned for capture purposes. For the 25GbE ports, only one capture buffer may be assigned to a single Resource Group (i.e. 4x25GbE mode).
Statistics and Rates	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 user-defined stats, capture trigger (UDS 3), capture filter (UDS 4), 8 QoS counters, data integrity frames, data integrity errors, sequence and advanced sequence checking frames, sequence checking errors, ARP, and PING requests and replies, FEC statistics: RS-FEC Corrected and Uncorrected Codeword Counts.
Latency / Jitter Meas- urements	Cut-through, store and forward, forwarding delay, up to 16 Latency bins / jitter, MEF frame delay, and inter-arrival time.
Receive-side PCS Lanes Port Statistics Counters	PCS Sync Errors, Illegal Codes, Remote Faults, Local Faults, Illegal Ordered Set, Illegal Idle, Illegal SOF, Out Of Order SOF, Out Of Order EOF, Out Of Order Data, Out Of Order Ordered Set.
100GE Physical Coding Sublayer (PCS) Receive- Side Statistics and Indic- ators	IEEE 802.3ba-compliant PCS transmit and receive side test capabilities include: Per PCS lane, receive lanes statistics - PCS Sync Header and Lane Marker Lock, Lane Marker mapping, Relative lane deskew up to 104 microseconds for 100GE, Sync Header and PCS Lane Marker Error counters, indicators for Loss of Synch Header and Lane Marker, and BIP8 errors.

Product Descrip- tion	NOVUS100GE8Q28+FAN
Routing and Switching	BGP-4, BGP+, OSPFv2/v3, ISISv4/v6, EIGRP, EIGRPv6, RIP, RIPng, BFD, IGMPv1/v2/v3, MLDv1/v2, PIM-SM/SSM, PIM-BSR, STP/RSTP, MSTP, PVST+/RPVST+, Link Aggregation (LACP), LLDP
Software Defined Network	VXLAN, EVPN VXLAN, OpenFlow, ISIS Segment Routing, OSPF Segment Routing, BGP Segment Routing, BGP Link State (BGP-LS), PCEP, OVSDB
MPLS	RSVP-TE, RSVP-TE P2MP, LDP/LDPv6, mLDP, PWE, VPLS-LDP, VPLS-BGP, BGP auto-discovery with LDP FEC 129 support, L3 MPLS VPN/6VPE, 6PE, BGP RT-Constraint, BGP Labeled unicast, L3 Inter-AS VPN Options (A, B, C), MPLS-TP, MPLS OAM, Multicast VPN (GRE, mLDP, RSVP-TE P2MP), EVPN, PBB-EVPN
Broadband and Authentication	PPPoX, DHCPv4, DHCPv6, L2TPv2, Radius attributes for L2TP, ANCP, IPv6 Autoconfiguration (SLAAC), IGMPv1/v2/v3, MLDv1/v2, 802.1x
Industrial Ethernet	Link OAM IEEE 802.3ah, CFM IEEE 802.1ag, Service OAM ITUT-Y.1731, PBT/PBB-TE, Sync-E ESMC, PTP IEEE 1588 with G.8265.1 Telecom Profile, ELMI
Data Center Ethernet	FCoE/FIP, Priority Flow Control IEEE 802.1Qbb (PFC), LLDP/DCBX, TRILL, TRILL OAM, SPBM, Cisco FabricPath, VEPA

# **Application Support**

The Ixia application support Novus load modules is provided in the following table:

Novus Application Support

Application	Support
IxNetwork	Provides wire-rate traffic generation with service modeling that builds realistic, dynamically-controllable data-plane traffic. IxNetwork offers the industry's best test solution for functional and performance testing by using comprehensive emulation for routing, switching, MPLS, IP multicast, broadband, authentication, Carrier Ethernet, and data center Ethernet protocols.
IxExplorer	Provides layer 2-3 wire-speed traffic generation and analysis and IEEE 802.3ba HSE PCS Lanes testing.  Note: Not all Ixia loads modules support Layer 1 BERT and/or the complete set of PCS Lanes test capabilities.
Tcl API	Allows custom user script development for layer 1-3 testing.

# **Mechanical Specifications**

### **Front Panel**

The front panel of Novus load modules is shown in the following figure:

Figure: Front panel of NOVUS100GE8Q28+FAN



### **LED Panel**

There are 3 tricolor LEDs per port. The LED panel specifications for Novus are provided in the following table.

LED panel Specifications for Novus Load Module

Speed Mode	LED1: TX LED	LED2: RX LED	LED3: MODE LED
100GbE	Port Inactive/No Power- r=Off Link Down (all)=Solid Red Link Up (all)=Solid Green Tx Active=Blinking Green	Port Inactive/No Power- r=Off  Rx Active with Error- s=Blinking Red  Rx Active=Blinking  Green	Mode=Off Card Fault=Solid Red
25GbE	Link Up (1,2, or 3 links) =Solid Yellow Link Down (all)=Solid Red Link Up (all)=Solid Green Tx Active=Blinking Green	Port Inactive/No Power- r=Off  Rx Active with Error- s=Blinking Red  Rx Active=Blinking  Green	25GbE Speed Mode- e=Solid Blue Card Fault=Solid Red



# Chapter 33 - IXIA Novus-R QSFP28 Load Modules

This chapter provides details about Novus-R family of load modules and their specifications and features.

Novus-R is a new, next generation, high density, 8-port, native QSFP28 100/25GE load module. This load module family supports the test needs of both high-density, multi-rate switch/router makers and the organizations implementing the network equipment. Novus-R supports eight native QSFP28 100GE ports and up to 32 ports for 25GE per load module, and enables interoperability and functional testing, as well as high-port count performance testing. Its native QSFP28 100GE interfaces with 25GE speed and fan-out cable support, that provides a more efficient and flexible set of 100/25GE test use cases. It is field upgradeable to the full feature compliant NOVUS100GE8Q28+FAN load module.

For more information on Novus family of load modules, see Novus Load Modules.

# **Key Features**

The key features of Novus-R load module are as follows:

- Supports multi-vendor interoperability 100GE and 25GE testing between speeds that run over these QSFP28 optical transceivers, Active Optical Cables and 100GBASE-CR4 passive copper Direct Attach Cable media:
  - Multimode 100GBASE-SR4 and single-mode 100GBASE-LR4
  - Multimode 25GBASE-SR and copper 25GBASE-CR
- Supports limited host protocols and data center test cases with the Ixia's IxNetwork application
- Provides 100Gb/s and 25Gb/s line rate packet capture and decode tools to detect and de-bug data transmission errors
- Provides an excellent test platform for full line rate 100Gb/s to evaluate the new 100GE ASIC designs, FPGAs, and hardware switch fabrics that use the new 4x25Gb/s electrical interface
- Supports benchmarking of the data plane and protocol emulation performance and scale of ultra-high-density 100/25GE-capable network equipment using industrystandard RFC benchmark tests in test beds with hundreds of 100GE and/or 25GE ports in a single test
  - 25GbE speed support (requires purchase of the 25GbE load module option):
    - Support for independent 25GE virtual and physical fan-out configurations including: 4x25GE
    - Up to 4x25GE links over single point-to-point 100GbE cable media (MT-MT, AOC, or DAC media)
- Underlying support for advanced features such as: Ethernet Forward Error Correction, auto-negotiation, and link training on 100GE and 25GE
- Provides a broad range of application support including: IxExplorer, IxNetwork, and the related Tcl and automation APIs.
- It is field upgradeable to the full feature compliant NOVUS100GE8Q28+FAN load module

#### **Load Modules**

The Novus-R family consists of the following model on a single slot card:

- NOVUS-R100GE8Q28+FAN
- NOVUS-R100GE8Q28+FAN+25G
- NOVUS-R100GE8Q28+FAN+RU
- NOVUS-R100GE8Q28+FAN+RU+25G

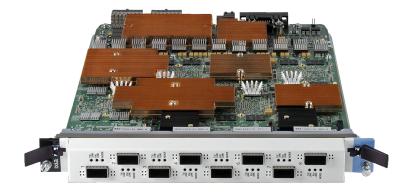
The load module is described as follows:

## NOVUS-R100GE8Q28+FAN

NOVUS-R100GE8Q28+FAN is a 100 Gigabit Ethernet reduced feature load module. It is field upgradeable to the full feature compliant NOVUS100GE8Q28+FAN load module. It has 1-slot with 8-ports with the native QSFP28 physical interface. It provides L2-3 support and is compatible with the XGS12-SD rack mount chassis (940-0011), XGS12-HS rack mount chassis (940-0006), XGS12-HSL, 12-slot high speed rackmount chassis (940-0016), XGS2-SD 2-slot standard performance chassis (940-0010), 2-slot high performance chassis XGS2-HS chassis (940-0012), and the XGS2-HSL, 2-slot high performance chassis (940-0014).

The NOVUS-R100GE8Q28+FAN load module is shown in the following figure:

Figure: Novus Module-NOVUS-R100GE8Q28+FAN



# 4x25G options for NOVUS-R100GE8Q28+FAN

4x25G options for NOVUS-R100GE8Q28+FAN is available in two forms:

- Factory Installed
- Field Upgrade

## 4x25GE factory installed

The 4x25GE Fan-Out FACTORY INSTALLED option for the NOVUS-R100GE8Q28+FAN load module enables 4x25GE capability on all eight 100GE QSFP28 ports on the module. The 4x25GE capability is per 100GE port and is ONLY supported over a single 100GE point-to-point QSFP28 cable where each channel of the cable is rated for 25GE per channel

operation. This is supported on the NOVUS100GE8Q28+FAN (944-1140) and NOVUS-R100GE8Q28+FAN (944-1147) load modules.



The factory installed option is required for new purchases of the 4x25GE capability for the NOVUS-R100GE8Q28+FAN load module with native QSFP28 8x100GE physical interfaces.

### 4x25GE field upgrade

The 4x25GE Fan-Out FIELD UPGRADE option for the NOVUS-R100GE8Q28+FAN load module enables 4x25GE capability on all eight 100GE QSFP28 ports on the module. The 4x25GE capability is per 100GE port and is ONLY supported over a single 100GE point-to-point QSFP28 cable where each channel of the cable is rated for 25GE per channel operation. This is supported on the NOVUS100GE8Q28+FAN (944-1140) and NOVUS-R100GE8Q28+FAN (944-1147) load modules.



The field upgrade option is required on field upgrade purchases of the 4x25GE capability for the NOVUS-R100GE8Q28+FAN load module with native QSFP28 8x100GE physical interfaces. Please provide the serial number of the desired load module at the time of placement of order, to install the option .

## Novus-R UPG field upgrade

The following Novus-R load module can be upgraded to enhance the data plane feature set and to add full support for all IxNetwork L23 protocol emulations equal to that of the full featured Novus QSFP28 8x100GE load module (944-1140).

• NOVUS-R100GE8Q28+FAN (944-1147)

After the upgrade is complete, the load module is named NOVUS-R100GE8Q28+FAN+RU instead of NOVUS100GE8Q28+FAN.



For the Novus-R upgrade purchase, please provide the serial number of the desired load module at the time of placement of order, to install the option .

#### **Part Numbers**

Part Numbers for Novus-R Load Module and Supported Adapters are provided in the following table.

Model Number	Part Num- ber	Description
NOVUS- R100GE8Q28+FAN	944-1147	<ul> <li>Reduced load module</li> <li>8-ports of 100GE with the QSFP28 physical interface</li> <li>100GE only</li> </ul>
	905-1007	<ul> <li>4x25GE factory installed option for NOVUS100GE8Q28+FAN load module (944-1140) and NOVUS- R100GE8Q28+FAN load module (944-</li> </ul>

Part Numbers for Novus Modules

Model Number	Part Num- ber	Description
		<ul> <li>1147)</li> <li>Enables 4x25GE capability on all eight 100GE QSFP28 ports on the module</li> <li>Supported over a single 100GE point-topoint QSFP28 cable where each channel of the cable is rated for 25GE per channel operation</li> <li>Supports 100GE Auto Negotiation and 100GE RS-FEC</li> <li>Support 25GE Auto Negotiation and 25GE FC-FEC</li> </ul>
	905-1008	<ul> <li>The 4x25GE field upgrade option for NOVUS100GE8Q28+FAN load module (944-1140) and NOVUS-R100GE8Q28+FAN load module (944-1147)</li> <li>Enables 4x25GE capability on all eight 100GE QSFP28 ports on the module</li> <li>Supported over a single 100GE point-topoint QSFP28 cable where each channel of the cable is rated for 25GE per channel operation</li> <li>Supports 100GE Auto Negotiation and 100GE RS-FEC</li> <li>Support 25GE Auto Negotiation and 25GE FC-FEC</li> </ul>
	905-1013	<ul> <li>The NOVUS-R-UPG field upgrade option for NOVUS-R100GE8Q28+FAN load module (944-1147)</li> <li>Enhances data plane feature set</li> <li>Adds full support for all IxNetwork L23 protocol emulations equal to that of Novus QSFP28 8x100GE load module (944-1140)</li> </ul>

# **Specifications**

The load module specifications are contained in the following table.

Novus Load Module Specifications

Hardware Load Module Specifications		
Feature	NOVUS-R100GE8Q28+FAN	
Novas Load Module Specifications		

Feature	NOVUS-R100GE8Q28+FAN
Slot / Number of Ports	1-slot / 8x100GE native QSFP28 ports
Physical Interface	Native QSFP28
Supported Port Speeds	<ul> <li>100GE/port: 100GE-capable fiber and copper cable media</li> <li>4x25GbE/port: 25GbE-capable fiber and copper point-point and fan-out cable media</li> </ul>
CPU and Memory	Multicore processor with 2GB of CPU memory per port
IEEE Interface Protocols	<ul> <li>IEEE 802.3 100GBASE-R</li> <li>IEEE 802.3bj</li> <li>IEEE 802.3bm</li> <li>IEEEP802.3by (draft specification 3.2)</li> </ul>
25G Consortium spe- cification	25GE: Compatible with version 1.5
Advanced Layer 1 support	<ul> <li>Auto-negotiation (AN, Clause 73 for copper DAC)</li> <li>Link training for 100GE copper cable media (Clause 73)</li> <li>Ethernet Forward Error Correction (RS-FEC, Clause 91)</li> <li>FEC statistics: RS-FEC Corrected and Uncorrected Codeword Counts</li> <li>Ability to independently turn ON or OFF AN with and Link Training, or FEC, or to allow IEEE defaults to automatically manage the interoperability. AN needs to be turned on to enable Link Training</li> <li>25GE: <ul> <li>Auto-negotiation (AN, Clause 73 for copper DAC)</li> <li>Link training for 25GE copper DAC media (Clause 93, 110)</li> <li>Ethernet Forward Error Correction (BASE-R, Clause 74)</li> <li>FEC statistics: FC-FEC Corrected and Uncorrected Codeword Counts</li> <li>Ability to independently turn ON or OFF AN with and Link Training, or FEC, or to allow IEEE defaults to automatically manage the interoperability</li> <li>Independent fan-out ports with physical fan-out media for up to 4x25GE per QSFP28 port</li> </ul> </li> </ul>
Transceiver Support	<ul> <li>100GBASE-SR4 and 4x25GBASE-SR QSFP28 for multimode fiber</li> <li>Pluggable transceiver</li> <li>25GbE speed support requires a point-to-point or a</li> </ul>

Feature	NOVUS-R100GE8Q28+FAN
	fan-out cable
	■ This transceiver supports the 25GE speed (NOVUS 25GE FAN-OUT Option 905-1007, and the NOVUS 25GE FAN-OUT-UPG FIELD UPGRADE Option 905-1008) on the NOVUS100GE8Q28+FAN and NOVUS-R100GE8Q28+FAN load modules
	<ul> <li>100GBASE-LR4 QSFP28 for single-mode fiber</li> <li>Pluggable transceiver</li> </ul>
	100GBASE-SR4 multimode fiber Active Optical Cable (AOC) and MT-MT 12-fiber point-to-point cables for QSFP28
	• 100GBASE-CR4, passive, copper Direct Attached Cable (DAC) up to 5 meters in length; note: requires RS-FEC to be enabled
Cabla Madia	<ul> <li>25GBASE-SR multimode fiber Optical Cable (AOC) and MT-MT 12-fiber point-to-point cable for QSFP28, 3 meter length is available</li> </ul>
Cable Media	<ul> <li>25GBASE-SR multimode fiber MT-to-4xLC fan-out cable for QSFP28, 3 meter and 5 meter lengths are available</li> <li>25GBASE-CR passive, copper Direct Attached Cable (DAC) point-point, up to 5 meters in length; note: requires BASE-R FEC Clause 74 to be enabled</li> </ul>
	<ul> <li>25GBASE-CR passive, copper Direct Attached Cable (DAC) QSFP28-to-4xSFP28 fan-out media, up to 5 meters in length; note: requires BASE-R FEC Clause 74 to be enabled</li> </ul>
	• 942-0067: MT-to-4x10GE LC fan-out, MMF, 3-meter cable for 10GE and 25GE fan-out. For 4x25GE fan-out it requires a 100GBASE-SR4 QSFP28 100GBASE-SR4 100GE pluggable transceiver, 850nm, MMF (QSFP28-SR4-XCVR).
Cables	<ul> <li>942-0068: MT-to-4x10GE LC fan-out, MMF, 5-meter cable for 10GE and 25GE fan-out. For 4x25GE fan-out it REQUIRES a 100GBASE-SR4 QSFP28 100GBASE-SR4 100GE pluggable transceiver, 850nm, MMF (QSFP28- SR4-XCVR).</li> </ul>
	• 942-0088: QSFP28 passive, copper, Direct Attach Cable (DAC), 3-meter length for Xcellon-Multis XM100GE4QSFP28+ENH 100GE load module (944-1117) and the NOVUS100GE8Q28+FAN, 8-port, QSFP28 100GE load module (944-1140).
	• 942-0092: QSFP28 Active Optical Cable (AOC), mul-

Feature	NOVUS-R100GE8Q28+FAN
	timode fiber, 850nm, 3-meter length. Compatible with the Xcellon-Lava CFP-to-QSFP28 interface adapter (948-0029), Xcellon-Multis XM100GE4QSFP28+ENH 100-Gigabit Ethernet, Enhanced load module (944-1117) and the NOVUS100GE8Q28+FAN, 8-port, QSFP28 100GE load module (944-1140).
Load Module Dimensions	17.3" (L) x 1.3" (W) x 12.0" (H)
Load Module Difficusions	440mm (L) x 33mm (W) x 305mm (H)
Load Module Weights	Module only: 11.8 lbs. (5.35 kg)
Loud Floudic Weights	Shipping: 18.6 lbs. (8.44 kg)
Temperature	Operating: 41°F to 95°F (5°C to 35°C)
remperatare	Storage: 41°F to 122°F (5°C to 50°C)
Humidity	Operating: 0% to 85%, non-condensing
Trainialty	Storage: 0% to 85%, non-condensing
Chassis Capacity: Maxi	mum Number of Cards and Ports per Chassis Model
XGS12-SD Chassis (940- 0011)	<ul><li>12 load modules:</li><li>Rackmount chassis</li><li>96-ports of 100GE</li><li>384-ports of 25GE</li></ul>
	12 load modules:
XGS12-HS Chassis (940- 0006)	<ul><li>Rackmount chassis</li><li>96-ports of 100GE</li><li>384-ports of 25GE</li></ul>
	2 load modules:
XGS2-SD Chassis (940- 0010)	<ul><li>Desktop chassis</li><li>16-ports of 100GE</li><li>64-ports of 25GE</li></ul>
	2 load modules:
XGS2-HS Chassis (940- 0012)	<ul><li>Desktop chassis</li><li>16-ports of 100GE</li><li>64-ports of 25GE</li></ul>
Transmit Feature Speci	fications
Transmit Engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures

Feature	NOVUS-R100GE8Q28+FAN
Max. Streams per Port	<ul><li>100GE: 32</li><li>25GE: 16</li></ul>
Max. Streams per Port in Data Center Ethernet	<ul><li>100GE: 32</li><li>25GE: 16</li></ul>
Stream Controls	Rate and frame size change on the fly, sequential and advanced stream scheduler
Minimum Frame Size	<ul> <li>100GE and 25GE:</li> <li>60 bytes at full line rate</li> <li>64 bytes at full line rate into the capture buffer</li> <li>49 bytes at less than full line rate</li> </ul>
Maximum Frame Size	14,000 bytes
Maximum Fame Size in Data Center Ethernet	9,216 bytes
Priority Flow Control	<ul> <li>8 line-rate-capable queues with each supporting up to 2,500 byte frame lengths</li> <li>1 queue supporting up to 9,216 byte frame lengths</li> </ul>
Frame Length Controls	Fixed, increment by user-defined step, weighted pairs, uniform, repeatable random, IMIX, and Quad Gaussian
User defined fields (UDF)	Fixed, increment or decrement by user-defined step, sequence, value list, and random configurations. Up to ten, 32-bit wide UDFs are available.
Value Lists (max.)	100GE and 25GE: 32K / UDF
Sequence (max.)	<ul><li>100GE: 8K / UDF</li><li>25GE: 2K/UDF</li></ul>
Error Generation	Generate good CRC or force bad CRC, undersize and over- size standard Ethernet frame lengths, and bad checksum
Hardware Checksum Generation	Checksum generation and verification for IPv4, IP over IP, IGMP/GRE/TCP/UDP, L2TP, GTP
Link Fault Signaling	Reports, no fault, remote fault, and local fault port statistics; generate local and remote faults with controls for the number of faults and order of faults, plus the ability to select the option to have the transmit port ignore link faults from a remote link partner.
Latency Measurement Resolution	100GE and 25GE: 2.5 nanoseconds
Intrinsic Latency Compensation	Removes inherent latency error from the 100GE port electronics

Feature	NOVUS-R100GE8Q28+FAN
Transmit line clock adjust- ment	Ability to adjust the parts per million line frequency over a range of -100 ppm to $+100$ ppm across all 100GE ports on the load module. This applies to all ports when in 25GbE speed mode.
Receive Feature Specifi	cations
Receive Engine	Wire-speed packet filtering, capturing, real-time latency and inter-arrival time for each packet group, with data integ- rity, sequence and advanced sequence checking capability
Trackable Receive Flows per Port	<ul> <li>100GE:</li> <li>32K limited statistics mode</li> <li>4K full statistics mode</li> </ul> 25GE: <ul> <li>8K limited statistics mode</li> <li>2K full statistics mode</li> </ul>
Minimum Frame Size	<ul> <li>100GE and 25GE:</li> <li>60 bytes at full line rate</li> <li>64 bytes at full line rate into the capture buffer</li> <li>49 bytes at less than full line rate</li> </ul>
Filters (User-Defined Statistics, UDS)	2 SA/DA pattern matchers, 2x16-byte user-definable patterns with offsets capability for start of: frame, IP, or protocol. Up to 6 UDS counters are available.
Hardware Capture Buffer per Port or Resource Group	100GE and 25GE: There are two 1MB hardware capture buffers on the card; user can select which port and/or resource group each capture buffer may be assigned for capture purposes. For the 25GbE ports, only one capture buffer may be assigned to a single Resource Group (i.e. 4x25GbE mode).
Statistics and Rates	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 user-defined stats, capture trigger (UDS 3), capture filter (UDS 4), 8 QoS counters, data integrity frames, data integrity errors, sequence and advanced sequence checking frames, sequence checking errors, ARP, and PING requests and replies, FEC statistics: RS-FEC Corrected and Uncorrected Codeword Counts.
Latency / Jitter Meas- urements	Cut-through, store and forward, forwarding delay, up to 16 Latency bins / jitter, MEF frame delay, and inter-arrival time.
Receive-side PCS Lanes Port Statistics Counters	PCS Sync Errors, Illegal Codes, Remote Faults, Local Faults, Illegal Ordered Set, Illegal Idle, Illegal SOF, Out Of Order SOF, Out Of Order EOF, Out Of Order Data, Out Of Order

Feature	NOVUS-R100GE8Q28+FAN
	Ordered Set.
100GE Physical Coding Sublayer (PCS) Receive- Side Statistics and Indic- ators	IEEE 802.3ba-compliant PCS transmit and receive side test capabilities include: Per PCS lane, receive lanes statistics - PCS Sync Header and Lane Marker Lock, Lane Marker mapping, Relative lane deskew up to 104 microseconds for 100GE, Sync Header and PCS Lane Marker Error counters, indicators for Loss of Synch Header and Lane Marker, and BIP8 errors.

Product Descrip- tion	NOVUS-R100GE8Q28+FAN
Routing and Switching	Only supported with Novus-R upgrade option (905-1013).
Software Defined Network	Only supported with Novus-R upgrade option (905-1013).
MPLS	Only supported with Novus-R upgrade option (905-1013).
Broadband and Authentication	IPv4/IPv4, DHCP, PPPoE, L2TP, IGMP, MLD, 802.1x.
Industrial Ethernet	Only supported with Novus-R upgrade option (905-1013).
Data Center Ethernet	FCoE/FIP, Priority Flow Control IEEE 802.1Qbb (PFC), and LLDP/DCBX.

# **Application Support**

The Ixia application support Novus load modules is provided in the following table:

Novus-R Application Support

Application	Support
IxNetwork	Provides wire-rate traffic generation with service modeling that builds realistic, dynamically-controllable data-plane traffic. IxNetwork offers the industry's best test solution for functional and performance testing by using comprehensive emulation for routing, switching, MPLS, IP multicast, broadband, authentication, Carrier Ethernet, and data center Ethernet protocols.
IxExplorer	Provides layer 2-3 wire-speed traffic generation and analysis and IEEE 802.3ba HSE PCS Lanes testing.  Note: Not all Ixia loads modules support Layer 1 BERT and/or the complete set of PCS Lanes test capabilities.
Tcl API	Allows custom user script development for layer 1-3 testing.

# **Mechanical Specifications**

### **Front Panel**

The front panel of Novus-R load module is shown in the following figure:

Figure: Front panel of NOVUS-R100GE8Q28+FAN



### **LED Panel**

There are 3 tricolor LEDs per port. The LED panel specifications for Novus-R are provided in the following table.

LED panel Specifications for Novus-R Load Module

Speed Mode	LED1: TX LED	LED2: RX LED	LED3: MODE
100GE	Port Inactive/No Power- r=Off Link Down (all)=Solid Red Link Up (all)=Solid Green Tx Active=Blinking Green	Port Inactive/No Power- r=Off Rx Active with Error- s=Blinking Red Rx Active=Blinking Green	Mode=Off Card Fault=Solid Red
25GE	Link Up (1,2, or 3 links) =Solid Yellow Link Down (all)=Solid Red Link Up (all)=Solid Green Tx Active=Blinking Green	Port Inactive/No Power- r=Off  Rx Active with Error- s=Blinking Red  Rx Active=Blinking  Green	25GE Speed Mode- e=Solid Blue Card Fault=Solid Red



# Chapter 34 - IXIA Novus-M QSFP28 Load Modules

This chapter provides details about Novus-M family of load modules and their specifications and features.

Novus-M is a next generation, high density, 8-port, native QSFP28 100/25GE load module. This load module family supports the test needs of both high-density, multi-rate switch/router makers and the organizations implementing the network equipment. Novus-M supports eight native QSFP28 100GE ports and up to 32 ports for 25GE per load module, and enables interoperability and functional testing, as well as high-port count performance testing. Its native QSFP28 100GE interfaces with 25GE speed and fan-out cable support, that provides a more efficient and flexible set of 100/25GE test use cases.

For more information on Novus family of load modules, see Novus Load Modules.

## **Key Features**

The key features of Novus-M load module are as follows:

- Supports multi-vendor interoperability 100GE and 25GE testing between speeds that run over these QSFP28 optical transceivers, Active Optical Cables and 100GBASE-CR4 passive copper Direct Attach Cable media:
  - Multimode 100GBASE-SR4 and single-mode 100GBASE-LR4
  - Multimode 25GBASE-SR and copper 25GBASE-CR
- Supports L2/3 protocol emulation to validate performance and scalability of L2/3 routing/switching and data center test cases using Ixia's IxNetwork application
- Supports medium host protocols and data center test cases with the Ixia's IxNetwork application
- Provides 100Gb/s and 25Gb/s line-rate packet capture and decode tools to detect and de-bug data transmission errors
- Provides an excellent test platform for full line rate 100Gb/s to evaluate the new 100GE ASIC designs, FPGAs, and hardware switch fabrics that use the new 4x25Gb/s electrical interface
- Supports benchmarking of the data plane and protocol emulation performance and scale of ultra-high-density 100/25GE-capable network equipment using industrystandard RFC benchmark tests in test beds with hundreds of 100GE and/or 25GE ports in a single test
  - 25GbE speed support (requires purchase of the 25GbE load module option):
    - Support for independent 25GE virtual and physical fan-out configurations including: 4x25GE
    - Up to 4x25GE links over single point-to-point 100GbE cable media (MT-MT, AOC, or DAC media)
- Underlying support for advanced features such as: Ethernet Forward Error Correction, auto-negotiation, and link training on 100GE and 25GE
- Provides a broad range of application support including: IxExplorer, IxNetwork, and the related Tcl and automation APIs.

#### **Load Modules**

The Novus-M family consists of the following model on a single slot card:

• NOVUS-M100GE8Q28+FAN

The load module is described as follows:

### NOVUS-M100GE8Q28+FAN

NOVUS-M100GE8Q28+FAN is a 100 Gigabit Ethernet reduced feature load module. It has 1-slot with 8-ports with the native QSFP28 physical interface. It provides L2-3 support with complete protocol coverage, and mid-range scale and performance protocol emulation for routing, switching and access protocols. and is compatible with the XGS12-SD 12-slot, standard performance rack mount chassis bundle (940-0011), XGS2-SD 2-slot, 3RU standard performance chassis bundle (940-0010), XGS2-HSL 2-slot, 3RU high-speed performance chassis bundle (940-0014), and XGS12-HSL 12-slot, high-speed performance rackmount chassis bundle (940-0016).

The NOVUS-M100GE8Q28+FAN load module is shown in the following figure:

Figure: Novus Module-NOVUS-M100GE8Q28+FAN



# 4x25G options for NOVUS-M100GE8Q28+FAN

4x25G options for NOVUS-M100GE8Q28+FAN is available in two forms:

- Factory Installed
- · Field Upgrade

#### 4x25GE Factory Installed

The 4x25GE Fan-Out FACTORY INSTALLED option for the NOVUS-M100GE8Q28+FAN load module enables 4x25GE capability on all eight 100GE QSFP28 ports on the module. The 4x25GE capability is per 100GE port and is ONLY supported over a single 100GE point-to-point QSFP28 cable where each channel of the cable is rated for 25GE per channel operation. This is supported on the NOVUS-M100GE8Q28+FAN (944-1156) load module.



The factory installed option is required for new purchases of the 4x25GE capability for the NOVUS-M100GE8Q28+FAN load module with native QSFP28 8x100GE physical interfaces.

### 4x25GE Field Upgrade

The 4x25GE Fan-Out FIELD UPGRADE option for the NOVUS-M100GE8Q28+FAN load module enables 4x25GE capability on all eight 100GE QSFP28 ports on the module. The 4x25GE capability is per 100GE port and is ONLY supported over a single 100GE point-to-point QSFP28 cable where each channel of the cable is rated for 25GE per channel operation. This is supported on the NOVUS-M100GE8Q28+FAN (944-1156) load module.



The field upgrade option is required on field upgrade purchases of the 4x25GE capability for the NOVUS-M100GE8Q28+FAN load module with native QSFP28 8x100GE physical interfaces. Please provide the serial number of the desired load module at the time of placement of order, to install the option .

#### **Part Numbers**

Part Numbers for Novus-M Load Module and Supported Adapters are provided in the following table.

Part Numbers for Novus-M Load Modules

Model Number	Part Num- ber	Description
	944-1156	<ul> <li>8-ports of 100GE with the QSFP28 physical interface</li> <li>100GE only</li> </ul>
NOVUS- M100GE8Q28+FAN	905-1007	<ul> <li>4x25GE factory installed option for NOVUS100GE8Q28+FAN load module (944-1140) and NOVUS- R100GE8Q28+FAN load module (944- 1147)</li> <li>Enables 4x25GE capability on all eight 100GE QSFP28 ports on the module</li> <li>Supported over a single 100GE point-to- point QSFP28 cable where each channel of the cable is rated for 25GE per channel operation</li> <li>Supports 100GE Auto Negotiation and 100GE RS-FEC</li> <li>Support 25GE Auto Negotiation and 25GE FC-FEC</li> </ul>
	905-1008	The 4x25GE field upgrade option for NOVUS100GE8Q28+FAN load module (944-1140) and NOVUS- R100GE8Q28+FAN load module (944-1147)

Model Number	Part Num- ber	Description
		<ul> <li>Enables 4x25GE capability on all eight 100GE QSFP28 ports on the module</li> </ul>
		<ul> <li>Supported over a single 100GE point-to- point QSFP28 cable where each channel of the cable is rated for 25GE per channel operation</li> </ul>
		<ul> <li>Supports 100GE Auto Negotiation and 100GE RS-FEC</li> </ul>
		<ul> <li>Support 25GE Auto Negotiation and 25GE FC-FEC</li> </ul>

# **Specifications**

The load module specifications are contained in the following table.

Novus-M Load Module Specifications

Feature	NOVUS-M100GE8Q28+FAN			
Hardware Load Module Specifications				
Slot / Number of Ports	1-slot / 8x100GE native QSFP28 ports and up to 32x25GE ports via fan-out media.			
Physical Interface	8-ports of Native QSFP28.			
Supported Port Speeds	<ul> <li>100GE/port: 100GE-capable fiber and passive copper cable media</li> <li>4x25GbE/port: 25GbE-capable fiber and passive copper point-point and fan-out cable media</li> </ul>			
CPU and Memory	Multicore processor with 2GB of CPU memory per port.			
IEEE Interface Protocols	<ul> <li>IEEE 802.3 100GBASE-R</li> <li>IEEE 802.3bj</li> <li>IEEE 802.3bm</li> <li>IEEEP802.3by (draft specification 3.2)</li> </ul>			
25G Consortium spe- cification	25GE: Compatible with version 1.6.			
Advanced Layer 1 support	<ul> <li>Auto-negotiation (AN, Clause 73 for copper DAC)</li> <li>Link training for 100GE copper cable media (Clause 73)</li> <li>Ethernet Forward Error Correction (RS-FEC, Clause 91)</li> <li>FEC statistics: RS-FEC Corrected and Uncorrected Codeword Counts</li> </ul>			

Feature	NOVUS-M100GE8Q28+FAN
	Ability to independently turn ON or OFF AN with Link training, or FEC, or to allow IEEE defaults to auto- matically manage the interoperability
	25GE:
	<ul> <li>Auto-negotiation (AN, Clause 73 for copper DAC)</li> <li>Link training (LT) for 25GE copper DAC media (Clause 93, 110) Note: Clause 72 link training patterns are not supported</li> <li>Ethernet Forward Error Correction (BASE-R, Clause 74)</li> <li>FEC statistics: FC-FEC Corrected and Uncorrected Codeword Counts</li> <li>Ability to independently turn ON or OFF AN with and Link Training, or FEC, or to allow IEEE defaults to automatically manage the interoperability</li> <li>Independent fan-out ports with physical fan-out media for up to 4x25GE per QSFP28 port</li> </ul>
Transceiver Support	<ul> <li>100GBASE-SR4 and 4x25GBASE-SR QSFP28 for multimode fiber</li> <li>Pluggable transceiver</li> <li>25GbE speed support requires a point-to-point or a fan-out cable</li> <li>NOTE</li> <li>This transceiver supports the 25GE speed (NOVUS 25GE FAN-OUT Option 905-1007, and the NOVUS 25GE FAN-OUT-UPG FIELD UPGRADE Option 905-1008) on the NOVUS100GE8Q28+FAN and NOVUS-R100GE8Q28+FAN load modules</li> </ul>
	<ul> <li>100GBASE-LR4 QSFP28 for single-mode fiber</li> <li>Pluggable transceiver</li> </ul>
Cable Media	<ul> <li>100GBASE-SR4 multimode fiber Active Optical Cable (AOC) and MT-MT 12-fiber point-to-point cables for QSFP28</li> <li>100GBASE-CR4, passive, copper Direct Attached Cable (DAC) up to 5 meters in length; note: requires RS-FEC to be enabled</li> <li>25GBASE-SR multimode fiber Optical Cable (AOC) and MT-MT 12-fiber point-to-point cable for QSFP28, 3 meter length is available</li> <li>25GBASE-SR multimode fiber MT-to-4xLC fan-out cable for QSFP28, 3 meter and 5 meter lengths are available</li> <li>25GBASE-CR passive, copper Direct Attached Cable (DAC) point-point, up to 5 meters in length; note:</li> </ul>

Feature	NOVUS-M100GE8Q28+FAN	
	requires BASE-R FEC Clause 74 to be enabled  • 25GBASE-CR passive, copper Direct Attached Cable (DAC) QSFP28-to-4xSFP28 fan-out media, up to 5 meters in length; Note: requires BASE-R FEC Clause 74 to be enabled	
Cables and Transceivers	<ul> <li>QSFP28 100GBASE-SR4 100GE pluggable optical transceiver, MMF (multimode), 850nm, 100m reach</li> <li>QSFP28 100GBASE-LR4 100GE pluggable optical transceiver, SMF (single mode fiber), 1310nm, 10km reach</li> <li>942-0067: MT-to-4x10GE LC fan-out, MMF, 3-meter cable for 10GE and 25GE fan-out. For 4x25GE fan-out it requires a 100GBASE-SR4 QSFP28 100GBASE-SR4 100GE pluggable transceiver, 850nm, MMF (QSFP28-SR4-XCVR).</li> <li>942-0068: MT-to-4x10GE LC fan-out, MMF, 5-meter cable for 10GE and 25GE fan-out. For 4x25GE fan-out it REQUIRES a 100GBASE-SR4 QSFP28 100GBASE-SR4 100GE pluggable transceiver, 850nm, MMF (QSFP28-SR4-XCVR).</li> <li>942-0088: QSFP28 passive, copper, Direct Attach Cable (DAC), 3-meter length for Xcellon-Multis XM100GE4QSFP28+ENH 100GE load module (944-1117) and the NOVUS100GE8Q28+FAN, 8-port, QSFP28 100GE load module (944-1140).</li> <li>942-0092: QSFP28 Active Optical Cable (AOC), multimode fiber, 850nm, 3-meter length. Compatible with the Xcellon-Lava CFP-to-QSFP28 interface adapter (948-0029), Xcellon-Multis XM100GE4QSFP28+ENH 100-Gigabit Ethernet, Enhanced load module (944-1117) and the NOVUS100GE8Q28+FAN, 8-port, QSFP28 100GE load module (944-1140).</li> </ul>	
Load Module Dimensions	17.3" (L) x 1.3" (W) x 12.0" (H) 440mm (L) x 33mm (W) x 305mm (H)	
Load Module Weights	Module only: 11.8 lbs. (5.35 kg) Shipping: 18.6 lbs. (8.44 kg)	
Temperature	Operating: 41°F to 95°F (5°C to 35°C) Storage: 41°F to 122°F (5°C to 50°C)	
Humidity	Operating: 0% to 85%, non-condensing Storage: 0% to 85%, non-condensing	
Chassis Capacity: Maximum Number of Cards and Ports per Chassis Model		
XGS12-SD Chassis (940-	12 load modules:	

Feature	NOVUS-M100GE8Q28+FAN
0011)	<ul><li>Rackmount chassis</li><li>96-ports of 100GE</li><li>384-ports of 25GE</li></ul>
XGS12-HS Chassis (940- 0006)	12 load modules:  Rackmount chassis 96-ports of 100GE 384-ports of 25GE
XGS2-SD Chassis (940- 0010)	2 load modules:  • Desktop chassis  • 16-ports of 100GE  • 64-ports of 25GE
XGS2-HS Chassis (940- 0012)	2 load modules:  • Desktop chassis  • 16-ports of 100GE  • 64-ports of 25GE
XGS2-HSL Chassis (940-0014)	2 load modules:  • Desktop chassis  • 16-ports of 100GE  • 64-ports of 25GE
XGS12-HSL Chassis (940-0016)	12 load modules:  Rackmount chassis  96-ports of 100GE  384-ports of 25GE
Transmit Feature Speci	fications
Transmit Engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures.
• 100GE: 32 • 25GE: 16	
Max. Streams per Port in Data Center Ethernet	• 100GE: 32 • 25GE: 16
Stream Controls	Rate and frame size change on the fly, sequential and advanced stream scheduler
Minimum Frame Size	<ul><li>100GE and 25GE:</li><li>60 bytes at full line rate</li></ul>

Feature	NOVUS-M100GE8Q28+FAN		
	49 bytes at less than full line rate		
Maximum Frame Size	14,000 bytes		
Maximum Fame Size in Data Center Ethernet	9,216 bytes		
Priority Flow Control	<ul> <li>8 line-rate-capable queues with each supporting up to 2,500 byte frame lengths</li> <li>1 queue supporting up to 9,216 byte frame lengths</li> </ul>		
Frame Length Controls	Fixed, increment by user-defined step, weighted pairs, uniform, repeatable random, IMIX, and Quad Gaussian .		
User defined fields (UDF)	Fixed, increment or decrement by user-defined step, sequence, value list, and random configurations. Up to ten, 32-bit wide UDFs are available.		
Value Lists (max.)	100GE and 25GE: 32K / UDF		
Sequence (max.)	<ul><li>100GE: 8K / UDF</li><li>25GE: 2K/UDF</li></ul>		
Error Generation	Generate good CRC or force bad CRC, undersize and over- size standard Ethernet frame lengths, and bad checksum.		
Hardware Checksum Generation	Checksum generation and verification for IPv4, IP over IP, IGMP/GRE/TCP/UDP, L2TP, GTP .		
Link Fault Signaling	Reports, no fault, remote fault, and local fault port statistics; generate local and remote faults with controls for the number of faults and order of faults, plus the ability to select the option to have the transmit port ignore link faults from a remote link partner.		
Latency Measurement Resolution	100GE and 25GE: 2.5 nanoseconds .		
Intrinsic Latency Compensation	Removes inherent latency error from the 100GE port electronics.		
Transmit line clock adjust- ment	Ability to adjust the parts per million line frequency over a range of -100 ppm to $\pm$ 100 ppm across all 100GE and 25GE ports on the load module.		
Receive Feature Specifications			
Receive Engine	Wire-speed packet filtering, capturing, real-time latency and inter-arrival time for each packet group, with data integrity, sequence and advanced sequence checking capability.		
Trackable Receive Flows per Port	100GE:  • 32K limited statistics mode		

Feature	NOVUS-M100GE8Q28+FAN
	4K full statistics mode
	25GE:
	8K limited statistics mode
	2K full statistics mode
	100GE and 25GE:
Minimum Frame Size	60 bytes at full line rate
	<ul><li>64 bytes at full line rate into the capture buffer</li><li>49 bytes at less than full line rate</li></ul>
Filters (User-Defined Statistics, UDS)	2 SA/DA pattern matchers, 2x16-byte user-definable patterns with offsets capability for start of: frame, IP, or protocol. Up to 6 UDS counters are available.
	100GE and 25GE: There are two 1MB hardware capture buf-
Hardware Capture Buffer per Port or Resource	fers on the card; user can select which port and/or resource group each capture buffer may be assigned for capture pur-
Group	poses. For the 25GbE ports, only one capture buffer may be assigned to a single Resource Group (i.e. 4x25GbE mode).
	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC
	errors, VLAN tagged frames, 6 user-defined stats, capture trigger (UDS 3), capture filter (UDS 4), 8 QoS counters,
Statistics and Rates	data integrity frames, data integrity errors, sequence and
	advanced sequence checking frames, sequence checking errors, ARP, and PING requests and replies, FEC statistics:
	RS-FEC Corrected and Uncorrected Block Counts, FEC Corrected Error Bits, FEC Sync.
Latency / Jitter Meas- urements	Cut-through, store and forward, forwarding delay, up to 16 Latency bins / jitter, MEF frame delay, and inter-arrival
urements	time.
Receive-side PCS Lanes	PCS Sync Errors, Illegal Codes, Remote Faults, Local Faults, Illegal Ordered Set, Illegal Idle, Illegal SOF, Out Of Order
Port Statistics Counters	SOF, Out Of Order EOF, Out Of Order Data, Out Of Order
	Ordered Set.
	IEEE 802.3ba-compliant PCS transmit and receive side test capabilities include: Per PCS lane, receive lanes statistics -
100GE Physical Coding Sublayer (PCS) Receive-	PCS Sync Header and Lane Marker Lock, Lane Marker map-
Side Statistics and Indic-	ping, Relative lane deskew up to 104 microseconds for 100GE, Sync Header and PCS Lane Marker Error counters,
ators	indicators for Loss of Synch Header and Lane Marker, and
Lavor 2.2 Buch and Comm	BIP8 errors.
Layer 2-3 Protocol Supp	
Routing and Switching	BGP-4, BGP+, OSPFv2/v3, ISISv4/v6, EIGRP, EIGRPv6,

Feature	NOVUS-M100GE8Q28+FAN
	RIP, RIPng, BFD, IGMPv1/v2/v3, MLDv1/v2, PIM-SM/SSM, PIM-BSR, STP/RSTP, MSTP, PVST+/RPVST+, Link Aggregation (LACP), LLDP
Software Defined Network	VXLAN, EVPN VXLAN, OpenFlow, ISIS Segment Routing, OSPF Segment Routing, BGP Segment Routing, BGP Link State (BGP-LS), PCEP, OVSDB
Basic	IPv4/IPv6, DHCP, PPPoE, L2TP, IGMP, MLD, 802.1x
MPLS	RSVP-TE, RSVP-TE P2MP, LDP/LDPv6, mLDP, PWE, VPLS-LDP, VPLS-BGP, BGP auto-discovery with LDP FEC 129 support, L3 MPLS VPN/6VPE, 6PE, BGP RT-Constraint, BGP Labeled unicast, L3 Inter-AS VPN Options (A, B, C), MPLS-TP, MPLS OAM, Multicast VPN (GRE, mLDP, RSVP-TE P2MP), EVPN, PBB-EVPN
Broadband and Authentication	PPPoX, DHCPv4, DHCPv6, L2TPv2, Radius attributes for L2TP, ANCP, IPv6 Autoconfiguration (SLAAC), IGMPv1/v2/v3, MLDv1/v2, 802.1x
Industrial Ethernet	Link OAM IEEE 802.3ah, CFM IEEE 802.1ag, Service OAM ITUT-Y.1731, PBT/PBB-TE, Sync-E ESMC, PTP IEEE 1588 with G.8265.1 Telecom Profile, ELMI
Data Center Ethernet	FCoE/FIP, Priority Flow Control IEEE 802.1Qbb (PFC), LLDP/DCBX

Product Descrip- tion	NOVUS-M100GE8Q28+FAN
Routing and Switching	Only supported with Novus-R upgrade option (905-1013).
Software Defined Network	Only supported with Novus-R upgrade option (905-1013).
MPLS	Only supported with Novus-R upgrade option (905-1013).
Broadband and Authentication	IPv4/IPv4, DHCP, PPPoE, L2TP, IGMP, MLD, 802.1x.
Industrial Ethernet	Only supported with Novus-R upgrade option (905-1013).
Data Center Ethernet	FCoE/FIP, Priority Flow Control IEEE 802.1Qbb (PFC), and LLDP/DCBX.

The Ixia application support Novus load modules is provided in the following table:

Novus-M Application Support

Application	Support		
IxNetwork	Provides wire-rate traffic generation with service modeling that builds realistic, dynamically-controllable data-plane traffic. IxNetwork offers the industry's best test solution for functional and performance testing by using comprehensive emulation for routing, switching, MPLS, IP multicast, broadband, authentication, Carrier Ethernet, and data center Ethernet protocols.		
IxExplorer	Provides layer 2-3 wire-speed traffic generation and analysis and IEEE 802.3ba HSE PCS Lanes testing.  Note: Not all Ixia loads modules support Layer 1 BERT and/or the complete set of PCS Lanes test capabilities.		
Tcl API	Allows custom user script development for layer 1-3 testing.		

# **Mechanical Specifications**

#### **Front Panel**

The front panel of Novus-M load module is shown in the following figure:

Figure: Front panel of NOVUS-M100GE8Q28+FAN



#### **LED Panel**

There are 3 tricolor LEDs per port. The LED panel specifications for Novus-M are provided in the following table:

LED panel Specifications for Novus-M Load Module

Speed Mode	LED1: TX LED	LED2: RX LED	LED3: MODE LED
100GE	Port Inactive/No Power- r=Off Link Down (all)=Solid Red Link Up (all)=Solid Green Tx Active=Blinking Green	Port Inactive/No Power- r=Off  Rx Active with Error- s=Blinking Red  Rx Active=Blinking  Green	Mode=Off Card Fault=Solid Red
25GE	Link Up (1,2, or 3 links) =Solid Yellow Link Down (all)=Solid Red	Port Inactive/No Power- r=Off Rx Active with Error- s=Blinking Red	25GE Speed Mode- e=Solid Blue Card Fault=Solid Red

Speed Mode	LED1: TX LED	LED2: RX LED	LED3: MODE LED
	Link Up (all)=Solid Green Tx Active=Blinking Green	Rx Active=Blinking Green	

# Chapter 35 - IXIA Novus 10GE/1GE/100M Ethernet Load Modules

This chapter provides details about Novus 10/1 family of load modules and their specifications and features.

Novus 10/1 is a new, tri-speed, high density, with up to 16 Dual-PHY ports per module, multi-rate ethernet load module. This load module family supports complete Layer 2-7 (L2-7) network and application testing in a single system. It provides support for Dual-PHY (SFP+ and 10GBase-T RJ45), and enables up to line-rate L2/3 traffic generation and analysis, high-performance routing/bridging protocol emulation, and true L4-7 application traffic generation and subscriber emulation. All these features are available within one load module. It allows ultra-high-density test environments for 10GE/1GE/100M Ethernet over copper and fiber and supports up to 192 10GE/1GE/100M Ethernet test ports in a single 12-slot Ixia chassis.

For more information on Novus family of load modules, see Novus Load Modules.

# **Key Features**

The key features of Novus 10/1 load module are as follows:

- Provides support for testing SFP+ and 10GBase-T RJ-45 copper ports at different speeds simultaneously on the same load module
- Allows industry-standard RFC test and protocol emulation in large test bed with hundreds of 10G, 1G, and/or 100M ports in a single test. This helps to benchmark data plane, performance, and scale of ultra-high-density network equipment.
- 10G, 1G, and 100M line-rate hardware packet capture and decode tools to detect and debug data transmission errors
- Provides a broad range of application support including: IxExplorer, IxNetwork, IxLoad, and the related Tcl and automation APIs
- Adds IxLoad L4-7 including Voice, Video and Access protocols
- Has a flexible 4:1 CPU and memory aggregation, for high-scale protocol emulation and performance
- Uses flexible custom packet generation
- Provides real-time latency with latency resolution of up to 2.5ns
- Enables extensive port and traffic flow statistics
- Allows advanced sequence checking with duplicate packet detection

#### **Load Modules**

The Novus 10/1 family are available in the following three models:

- NOVUS10/1GE16DP
- NOVUS10/1GE8DP
- NOVUS1GE16DP

The load modules are described as follows:

#### NOVUS10/1GE16DP

NOVUS10/1GE16DP is a full-featured 16-port, Dual-PHY (RJ45 and SFP+) 10GE/1GE/100M load module designed for high-density requirements. It is compatible with the XGS12-SD rack mount chassis (940-0011), XGS12-HSL, 12-slot high speed rackmount chassis (940-0016), XGS2-SD 2-slot standard performance chassis (940-0010), and the XGS2-HSL, 2-slot high performance chassis (940-0014).

## NOVUS10/1GE8DP

NOVUS10/1GE8DP is a full-featured 8-port, Dual-PHY (RJ45 and SFP+) 10GE and 1GE load module designed for high-density switch testing. It is compatible with the XGS12-SD rack mount chassis (940-0011), XGS12-HSL, 12-slot high speed rackmount chassis (940-0016), XGS2-SD 2-slot standard performance chassis (940-0010), and the XGS2-HSL, 2-slot high performance chassis (940-0014).

#### **NOVUS1GE16DP**

NOVUS1GE16DP is a full-featured 16-port, Dual-PHY (RJ45 and SFP+) 1GE and 100M load module designed for high-density requirements. It is compatible with the XGS12-SD rack mount chassis (940-0011), XGS12-HSL, 12-slot high speed rackmount chassis (940-0016), XGS2-SD 2-slot standard performance chassis (940-0010), and the XGS2-HSL, 2-slot high performance chassis (940-0014).

The NOVUS10/1GE16DP load module is shown in the following figure:

Figure: Novus Module-NOVUS10/1GE16DP



## NOVUS10/1GE8DP Field Upgrade

The following Novus 10/1, 8 port load module can be upgraded to support evolving test needs, by a software field-upgrade to a full 16-port NOVUS10/1GE16DP load module.

• NOVUS10/1GE8DP (944-1143)



For the additional 8-port upgrade purchase, please provide the serial number of the desired load module at the time of placement of order, to install the option .

#### **Part Numbers**

Part Numbers for Novus 10G/1G/100M Load Modules and Supported Adapters are provided in the following table.

Part Numbers for Novus 10G/1G/100M Modules

Model Number	Part Num- ber	Description
NOVUS10/1GE16DP	944-1142	Dual-PHY with 16-ports each of the

Model Number	Part Num- ber	Description	
10G/1G/100M		<ul><li>SFP+</li><li>1-slot</li><li>10GBASE-T RJ45 physical interfaces</li><li>L2-7 support</li></ul>	
NOVUS10/1GE8DP 10G/1G/100M	944-1143	<ul> <li>Dual-PHY with 8-ports each of the SFP+</li> <li>1-slot</li> <li>10GBASE-T RJ45 physical interfaces</li> <li>L2-7 support</li> </ul>	
NOVUS1GE16DP 1G/100M	944-1146	Dual-PHY with 16-ports each of the SFP+     1-slot     1000BASE-T RJ45 physical interfaces     L2-7 support  NOTE  This is the NOVUS10/1GE16DP, 16-port load module (944-1142) enabled for ONLY 1GE/100Mbps operation on all 16-ports.	

# **Specifications**

The load module specifications are contained in the following table.

Novus 10G/1G/100M Load Module Specifications

Feature	NOVUS10/1GE16D- P 10G/1G/100M	NOVUS10/1GE8D- P 10G/1G/100M	NOVUS1GE16D- P 1G/100M
Hardware Lo cifications	ad Module Spe-		
Slot / Number of Ports	1-slot with 16x10/1G Dual-PHY SFP+/10GBASE-T ports	1-slot with 8x10/1G Dual-PHY SFP+/10GBASE-T ports	1-slot with 16x10/1G Dual-PHY SFP+/100BASE-T ports
Physical Inter- faces	16-ports of Dual-PHY SFP+/10GBASE-T RJ-45	8-ports of Dual-PHY SFP+/10GBASE-T RJ- 45	16-ports of SFP+/100BASE-T RJ-45
Supported Port Speeds	<ul> <li>10G/port and 1G/port: 10G and 1G-capable fiber and copper cable media</li> <li>100M/port: 100M capable fiber and copper media</li> </ul>		<ul> <li>1G/port: 1G-capable fiber and copper cable media</li> <li>100M/port: 100M capable</li> </ul>

Feature	NOVUS10/1GE16D- P 10G/1G/100M	NOVUS10/1GE8D- P 10G/1G/100M	NOVUS1GE16D- P 1G/100M	
			fiber and cop- per media	
CPU and Memory	Multicore processor with 2	2GB of CPU memory per p	ort	
Cable Media	<ul><li>CAT5e</li><li>CAT6</li><li>CAT6A</li></ul>	• CAT6		
Load Module Dimensions	• 17.3" (L) x 1.3" (W) x • 440mm (L) x 33mm (	` '		
Load Module Weights	<ul><li>Module only: 12.9 lbs</li><li>Shipping: 19.7 lbs (8.</li></ul>			
Temperature	<ul> <li>Operating: 41°F to 10</li> <li>Storage: 41°F to 122°</li> </ul>	` ,		
Humidity	<ul><li>Operating: 0% to 85%</li><li>Storage: 0% to 85%,</li></ul>	•		
Chassis Capa	acity: Maximum Number	of Cards and Ports pe	r Chassis Model	
XGS12-SD Chassis (940- 0011)	<ul><li>12 load modules:</li><li>192-ports of 10GbE</li><li>192-ports of 1GbE</li><li>192-ports of 100MbE</li></ul>	<ul><li>12 load modules:</li><li>96-ports of 10GbE</li><li>96-ports of 1GbE</li><li>96-ports of 100MbE</li></ul>	12 load modules:  • 192-ports of 1GbE  • 192-ports of 100MbE	
XGS12-HSL Chassis (940- 0016)	12 load modules:  • 192-ports of 10GbE  • 192-ports of 1GbE  • 192-ports of 100MbE	12 load modules:  • 96-ports of 10GbE  • 96-ports of 1GbE  • 96-ports of 100MbE	12 load modules:  • 192-ports of 1GbE  • 192-ports of 100MbE	
XGS2-SD Chassis (940- 0010)	2 load modules:  • 32-ports of 10GbE  • 32-ports of 1GbE  • 32-ports of 100MbE	2 load modules:  • 16-ports of 10GbE  • 16-ports of 1GbE  • 16-ports of 100MbE	2 load modules:  • 32-ports of 1GbE  • 32-ports of 100MbE	
XGS2-HSL Chassis (940- 0014)	2 load modules:  • 32-ports of 10GbE  • 32-ports of 1GbE  • 32-ports of 100MbE	2 load modules:  • 16-ports of 10GbE  • 16-ports of 1GbE  • 16-ports of	2 load modules:  • 32-ports of 1GbE  • 32-ports of 100MbE	

Feature	NOVUS10/1GE16D- P 10G/1G/100M	NOVUS10/1GE8D- P 10G/1G/100M	NOVUS1GE16D- P 1G/100M
		100MbE	
Transmit Fea	ture Specifications		
Transmit Engine	Wire-speed packet genera data integrity signature, a	• •	•
Max. Streams per Port	512		
Max. Streams per Port in Data Center Ethernet	256		
Stream Controls	Rate and frame size chang scheduler.	ge on the fly, sequential, a	and advanced stream
	10GbE:		
Minimum Frame Size	<ul> <li>49 bytes at full line rate without UDF60 bytes at full line rate with UDF</li> </ul>		
Traine Size	1GbE and 100MbE:		
	49 bytes at less than f	full line rate	
Maximum Frame Size	16,384 bytes		
Maximum Fame Size in Data Center Ethernet	9,216 bytes		
Priority Flow Control	<ul> <li>8 line-rate-capable queues with each supporting up to 2,500 byte frame lengths</li> <li>1 queue supporting up to 9,216 byte frame lengths</li> </ul>		
Frame Length Controls	Fixed, increment by user-defined step, weighted pairs, uniform, repeatable random, IMIX, and Quad Gaussian		
User defined fields (UDF)	Fixed, increment or decrement by user-defined step, sequence, value list, and random configurations. Up to ten, 32-bit wide UDFs are available.		
Value Lists (max.)	2M across 5 User Defined Fields		
Sequence (max.)	512		
Error Gen- eration	Generate good CRC or force bad CRC, undersize and oversize standard Ethernet frame lengths, and bad checksum.		

Feature		OVUS10/1GE8D- 10G/1G/100M	NOVUS1GE16D- P 1G/100M
Hardware Checksum Generation	Checksum generation and verification for IPv4, IP over IP, ICMP/GRE/TCP/UDP, L2TP, GTP.		
Link Fault Sig- naling	10GE: Reports, no fault, remote fault, and local fault port statistics; ability to select the option to have the transmit port ignore link faults from a remote link partner		Not Applicable
Latency Meas- urement Res- olution	2.5 nanoseconds		
Transmit line clock adjust-ment	Ability to adjust the parts-per 100 ppm to +100 ppm across		_
Receive Feat	ure Specifications		
Receive Engine	Wire-speed packet filtering, capturing, real-time latency and inter- arrival time for each packet group, with data integrity, sequence, and advanced sequence checking capability.		
Trackable Receive Flows per Port	<ul> <li>1M without Tx/Rx Sync and sequence checking</li> <li>512k with Tx/Rx Sync and sequence checking</li> </ul>		
Minimum Frame Size	<ul><li>64 bytes at full line rate into the capture buffer</li><li>49 bytes at less than full line rate</li></ul>		
Filters (User- Defined Stat- istics, UDS)	2 SA/DA pattern matchers, 2x16-byte user-definable patterns with offsets capability for start of: frame, IP, or protocol. Up to 6 UDS counters are available.		
Hardware Capture Buffer per Port or Resource Group	512MB per port		
Statistics and Rates	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 user-defined stats, capture trigger (UDS 3), capture filter (UDS 4), 8 QoS counters, data integrity frames, data integrity errors, sequence and advanced sequence checking frames, sequence checking errors, ARP, and PING requests and replies.		
Latency / Jit- ter Meas- urements	Cut-through, store and forward, forwarding delay, up to 16 Latency bins / jitter, MEF frame delay, and inter-arrival time.		

Feature	NOVUS10/1GE16D- NOVUS10/1GE8D- NOVUS1GE16D- P 10G/1G/100M P 10G/1G/100M P 1G/100M			
Layer 2-3 Pro	Layer 2-3 Protocol Support			
Routing and Switching	BGP4/BGP4+, OSPFv2/v3, ISISv4/v6, EIGRP/EIGRPv6, RIP/RIPng, BFD, IGMP/MLD, PIM-SM/SSM, STP/RSTP/MSTP, PVST+/RPVST+, Link Aggregation (LACP), LISP.			
Software Defined Net- work	OpenFlow, Segment Routing, BGP Link State (BGP-LS), PCEP, VXLAN, EVPN VXLAN, OVSDB, GENEVE.			
MPLS	RSVP-TE P2P/P2MP, LDP/LDPv6/mLDP, LDP L2VPN (PWE/VPLS), BGP VPLS, L3VPN/6VPE, 6PE, BGP RFC3107, MPLS-TP, MPLS OAM, EVPN/PBB-EVPN, Multicast VPN Rosen Draft, NG Multicast VPN.			
Broadband and Authentic- ation	PPPoX/L2TPv2, DHCPv4/DHCPv6, ANCP, IPv6 Autoconfiguration (SLAAC), IGMP/MLD, IPTV, 802.1x, WebAuth, EAPoUDP, Cisco NAC.			
Industrial Eth- ernet	Link OAM (IEEE 802.3ah), CFM/Y.1731, PBB/PBB-TE, ELMI, TWAMP, Sync-E ESMC, IEEE 1588v2 (PTP), gPTP (IEEE 802.1AS), MSRP (IEEE 802.1 Qat), IEEE 1722.			
Data Center Ethernet	DCBX/LLDP, FCoE/FIP, PFC (IEEE 802.1Qbb), TRILL, Cisco FabricPath, SPBM, VEPA.			
Layer 4-7 App	olication Traffic Testing Support			
Data	HTTP, HTTPS, TCP Session, FTP, DNS, Mail (SMTP, POP3, and IMAP),TFTP, AppReplay, AppLibrary.			
Video	RTSP, IPTV, VoD, Adobe Flash Client, Apple HLS Client, Microsoft Silverlight Client, Adobe HDS Client, DASH Client; includes Video Quality VQMON and TCP Video Quality.			
Voice	Advanced VoIP SIP & RTP, Audio & Video Codecs, VoLTE, MSRP, Telepresence, SMS, T.38; includes: Voice Quality and Video Quality for conversational video traffic.			
Storage	iSCSI, CIFSv1, CIFSv2 (SMB2), SMB3, NFSv3 Client, NFSv4 Client, NFS4.1 Client, Cloud Storage Client.			
Access	IPv4, IPv6, VLAN, Emulated Routers, DNS, DHCP.			

The Ixia application support for Novus 10G/1G/100M load modules is provided in the following table:

Novus 10G/1G/100M Application Support

Application	Support
IxNetwork	Provides wire-rate traffic generation with service modeling that builds realistic, dynamically-controllable data-plane traffic. IxNetwork offers the industry's best test solution for functional and performance testing by using comprehensive emulation for routing, switching, MPLS, IP multicast, broadband, authentication, Carrier Ethernet, and data center Ethernet protocols.
IxExplorer	Provides layer 2-3 wire-speed traffic generation and analysis test application.
Tcl API	Allows custom user script development for layer 2-7 testing.
IxLoad	Provides a scalable L4-7 solution for testing converged multiplay services, application delivery platforms, and security devices and systems. IxLoad ensures quality of experience (QoE) through emulation of data, access, storage, voice and video subscribers, and associated protocols.

# **Mechanical Specifications**

#### **Front Panel**

The front panel of one of the Novus 10G/1G/100M load module is shown in the following figure:

Figure: Front panel of NOVUS10/1GE16DP



#### **LED Panel**

There are 2 bicolor LEDs per port for the SFP+ (10G) variant. The LED panel specifications for Novus SFP+ (10G) are provided in the following table.

LED panel Specifications for Novus SFP+ (10G) Load Module

Speed Mode	LED1: TX LED	LED2: RX LED
10GE	Port Inactive/No Power=Off	Port Inactive/No Power=Off
	Link Down (all)=Solid Red	Rx Active with Errors=Blinking
	Link Up (all)=Solid Green	Red
	Tx Active=Blinking Green	Rx Active=Blinking Green

#### **Transceivers and Cables**

The Novus 10/1 family supports optical transceivers and fiber cables for each of the physical interfaces that are supported:

• **988-0011**: This is an SFP+10GBASE-SR/SW and 1000BASE-SX optical, dual-rate, 850nm transceiver with pluggable SFP+ interface. It is compatible with all 10/1 Gigabit Ethernet Novus, PerfectStorm, and Firestorm load modules, and appliances.

A 3 meter, multi-mode fiber LC-LC cable is included with this transceiver.

• **988-0012**: This is an SFP+10GBASE-LR/LW and 1000BASE-LX optical, dual-rate, 1310nm transceiver with pluggable SFP+ interface. It is compatible with all 10/1 Gigabit Ethernet Novus, PerfectStorm, and Firestorm load modules, and appliances.

A 10 ft, single-mode fiber LC-LC cable is included with this transceiver.

- 988-0013: This is an SFP+10GBASE-SR/SW, Accessory, 850nm transceiver with pluggable SFP+ interface. It is compatible with 944-0050 (LSM10GXM4S-01), 944-0051 (LSM10GXM8S-01), 944-0052 (LSM10GXMR4S-01), 944-0053 (LSM10GXMR8S-01), 944-0054 (LSM10GXM2S-01), 944-0055 (LSM10GXMR2S-01); and 944-0022 (LSM10G1-01) with 948-0012 (SFP+ADAP-01); or 944-0024 (LSM10GL1-01) with 948-0012 (SFP+ADAP-01).
- 988-0014: This is an SFP+10GBASE-LR/LW, Accessory, 1310nm transceiver with pluggable SFP+ interface. It is compatible with 944-0050 (LSM10GXM4S-01), 944-0051 (LSM10GXM8S-01), 944-0052 (LSM10GXMR4S-01), 944-0053 (LSM10GXMR8S-01), 944-0054 (LSM10GXM2S-01), 944-0055 (LSM10GXMR2S-01); and 944-0022 (LSM10G1-01) with 948-0012 (SFP+ADAP-01); or 944-0024 (LSM10GL1-01) with 948-0012 (SFP+ADAP-01).
- 988-0015: This is an SFP+10GBASE-LRM, Accessory, 1310nm transceiver, for multimode fiber, with pluggable SFP+ interface. It is compatible with 944-0050 (LSM10GXM4S-01), 944-0051 (LSM10GXM8S-01), 944-0052 (LSM10GXMR4S-01), 944-0053 (LSM10GXMR8S-01), 944-0054 (LSM10GXM2S-01), 944-0055 (LSM10GXMR2S-01); and 944-0022 (LSM10G1-01) with 948-0012 (SFP+ADAP-01); or 944-0024 (LSM10GL1-01) with 948-0012 (SFP+ADAP-01).

SFP+10GBASE-LRM does not support the 10GbE WAN mode in any of the load modules listed above.

- **988-0016**: This is an SFP+10GSFP+Cu, Accessory, passive, copper Direct Attach Cable Assembly, with pluggable SFP+ interface. It is compatible with NGY 10GE SFP+ modules, Xdenisty modules, and Xcellon-Flex 10GE SFP+ FE and AP modules.
- **SFP-LX**: This is a 1310nm LX, SFP 1 Gigabit Ethernet Transceiver.
- SFP-SX: This is a 850nm SX, SFP 1 Gigabit Transceiver.



# Chapter 36 - IXIA Novus-NP 10GE/1GE/100M Ethernet Load Modules

This chapter provides details about Novus-NP 10/1 family of load modules and their specifications and features.

Novus-NP 10/1 combines the architecture of Novus load modules with Ixia's NP (network processor) technology. It is a high density, with up to 16 Dual-PHY ports per module, multi-rate ethernet load module. This load module family supports complete Layer 2-7 (L2-7) network and application testing in a single system. It provides support for Dual-PHY (SFP+ and 10GBase-T RJ45), and enables up to line-rate L2/3 traffic generation and analysis, high-performance routing/bridging protocol emulation, and true L4-7 application traffic generation and subscriber emulation. All these features are available within one load module. It allows ultra-high-density test environments for 10GE/1GE/100M Ethernet over copper and fiber and supports up to 192 10GE/1GE/100M Ethernet test ports in a single 12-slot Ixia chassis.

For more information on Novus family of load modules, see Novus Load Modules.

## **Key Features**

The key features of Novus-NP 10/1 load module are as follows:

- Allows high-performance layer 4-7 testing using Ixia's IxLoad application: up to 40G application throughput per load module
- Provides ultra-high scale and performance for emulating L2/3 protocols to validate performance and scalability of L2/3 routing/switching and data center test cases using Ixia's IxNetwork application
- Supports full line-rate traffic generation to evaluate ASIC designs, FPGAs, and hardware switch fabrics
- Provides support for testing SFP+ and 10GBase-T RJ-45 copper ports at different speeds simultaneously on the same load module
- Allows industry-standard RFC test and protocol emulation in large test bed with hundreds of 10G, 1G, and/or 100M ports in a single test. This helps to benchmark data plane, performance, and scale of ultra-high-density network equipment.
- 10G, 1G, and 100M line-rate hardware packet capture and decode tools to detect and debug data transmission errors
- Provides a broad range of application support including: IxExplorer, IxNetwork, IxLoad, and the related Tcl and automation APIs
- Adds IxLoad L4-7 including Voice, Video and Access protocols
- Has a flexible 4:1 CPU and memory aggregation, for high-scale protocol emulation and performance
- Uses flexible custom packet generation
- Provides real-time latency with latency resolution of up to 2.5ns
- Enables extensive port and traffic flow statistics
- Allows advanced sequence checking with duplicate packet detection

#### **Load Modules**

The Novus-NP 10/1 family are available in the following two models:

- NOVUS-NP 10/1GE8DP
- NOVUS-NP 10/1GE16DP

The load modules are described as follows:

#### **NOVUS-NP 10/1GE8DP**

NOVUS-NP 10/1GE8DP is a full-featured 8-port, Dual-PHY (RJ45 and SFP+) 10GE and 1GE load module designed for high-density switch testing. It is compatible with the XGS12-SD rack mount chassis (940-0011), XGS12-HSL, 12-slot high speed rackmount chassis (940-0016), XGS2-SD 2-slot standard performance chassis (940-0010), and the XGS2-HSL, 2-slot high performance chassis (940-0014).

## **NOVUS-NP 10/1GE16DP**

NOVUS-NP10/1GE16DP is a full-featured 16-port, Dual-PHY (RJ45 and SFP+) 1GE and 100M load module designed for high-density requirements. It is compatible with the XGS12-SD rack mount chassis (940-0011), XGS12-HSL, 12-slot high speed rackmount chassis (940-0016), XGS2-SD 2-slot standard performance chassis (940-0010), and the XGS2-HSL, 2-slot high performance chassis (940-0014).

The NOVUS-NP 10/1GE16DP load module is shown in the following figure:

Figure: Novus Module-NOVUS-NP 10/1GE16DP



## NOVUS-NP 10/1GE8DP Field Upgrade

The following Novus-NP 10/1, 8 port load module can be upgraded to support evolving test needs, by a software field-upgrade to a full 16-port NOVUS-NP 10/1GE16DP load module by a 905-1006 field upgrade:

• NOVUS-NP 10/1GE8DP (944-1163)



For the additional 8-port upgrade purchase, please provide the serial number of the desired load module at the time of placement of order, to install the option .

#### **Part Numbers**

Part Numbers for Novus-NP 10G/1G/100M Load Modules and Supported Adapters are provided in the following table.

Part Numbers for Novus-NP 10G/1G/100M Modules

Model Number	Part Num- ber	Description
NOVUS-NP 10/1GE16DP 10G/1G/100M	944-1162	<ul> <li>Dual-PHY with 16-ports each of the SFP+</li> <li>1-slot</li> <li>10GBASE-T RJ45 physical interfaces</li> <li>L2-7 support</li> </ul>
NOVUS-NP 10/1GE8DP 10G/1G/100M	944-1163	<ul> <li>Dual-PHY with 8-ports each of the SFP+</li> <li>1-slot</li> <li>10GBASE-T RJ45 physical interfaces</li> <li>L2-7 support</li> </ul>

# **Specifications**

The load module specifications are contained in the following table:

Novus-NP 10G/1G/100M Load Module Specifications

Feature	NOVUS-NP 10/1GE16DP 10G/1G/100M	NOVUS-NP 10/1GE8DP 10G/1G/100M
Hardware Load Module Specifications		
Slot / Number of Ports	1-slot with 16x10/1G Dual-PHY SFP+/10GBASE-T ports	1-slot with 8x10/1G Dual-PHY SFP+/10GBASE-T ports
Physical Interfaces	16-ports of Dual-PHY SFP+/10GBASE-T RJ-45	8-ports of Dual-PHY SFP+/10GBASE-T RJ-45
Supported Port Speeds	<ul> <li>10G/port and 1G/port: 10G and 1G-capable fiber and copper cable media</li> <li>100M/port: 100M capable fiber and copper media</li> </ul>	
CPU and Memory	Multicore processor with 2GB of CPU memory per port	
Cable Media	<ul><li>CAT5e</li><li>CAT6</li><li>CAT6A</li></ul>	
Cables and Trans- ceivers	<ul> <li>988-0011: SFP+10GBASE-SR/SW and 1000BASE-SX Dual-Rate pluggable optical transceiver for 10/1 Gigabit Ethernet LAN/WAN load modules with pluggable SFP+ interface, 850nm. Compatible with all 10/1 Gigabit Ethernet Novus, PerfectStorm and Firestorm load modules and appliances. Note: Multi-mode fiber LC-LC, 3 meter cable included.</li> <li>988-0012: SFP+10GBASE-LR/LW and 1000BASE-LX Dual-Rate pluggable optical transceiver for 10/1 Gigabit Ethernet</li> </ul>	

Feature	NOVUS-NP 10/1GE16DP NOVUS-NP 10/1GE8DP 10G/1G/100M
	LAN/WAN load modules with pluggable SFP+ interface, 1310nm, 10km reach. Compatible with all 10/1 Gigabit Ethernet Novus, PerfectStorm and Firestorm load modules and appliances. Note: Single-mode fiber LC-LC, 10 ft cable included.  948-0014: SFP+10GBASE-LR/LW, Accessory, SFP+ Transceiver for 10 Gigabit Ethernet LAN/WAN load modules with pluggable SFP+ interface, 1310nm; Operates with 944-0050 (LSM10GXM4S-01), 944-0051 (LSM10GXM8S-01), 944-0052 (LSM10GXMR4S-01), 944-0053 (LSM10GXMR8S-01), 944-0052 (LSM10GXMR2S-01); and 944-0023 (LSM10GI-01) with 948-0012 (SFP+ADAP-01); or 944-0024 (LSM10GL1-01) with 948-0012 (SFP+ADAP-01).  942-0068: MT-to-4x10GE LC fan-out, MMF, 5-meter cable for 10GE and 25GE fan-out. For 4x25GE fan-out it REQUIRES a 100GBASE-SR4 QSFP28 100GBASE-SR4 100GE pluggable transceiver, 850nm, MMF (QSFP28-SR4-XCVR).  948-0015: SFP+10GBASE-LRM, Accessory, SFP+ Transceiver for 10 Gigabit Ethernet LAN/WAN load modules with pluggable SFP+ interface, For multimode fiber, 1310nm; Operates with 944-0050 (LSM10GXM4S-01), 944-0051 (LSM10GXM8S-01), 944-0052 (LSM10GXMR4S-01), 944-0053 (LSM10GXMR8S-01), 944-0054 (LSM10GXM2S-01), 944-0055 (LSM10GXMR8S-01); and 944-0022 (LSM10G1-01) with 948-0012 (SFP+ADAP-01); or 944-0024 (LSM10GL1-01) with 948-0012 (SFP+ADAP-01); or 944-0024 (LSM10GS-SFP+10GSFP+Cu, Accessory, passive, copper Direct Attach Cable Assembly for 10 Gigabit Ethernet LAN/WAN load modules, and xcellon-Flex 10GE SFP+ FE and AP modules.  948-0016: SFP+10GSFP+Cu, Accessory, passive, copper Direct Attach Cable Assembly for 10 Gigabit Ethernet LAN/WAN load modules with pluggable SFP+ interface, 3 meter length; NGY 10GE SFP+ FE and AP modules.  95FP-LX: SFP 1 Gigabit Ethernet Transceiver - 1310nm LX  95FP-SX: SFP 1 Gigabit Transceiver - 850nm SX
Load Module Dimensions	<ul> <li>17.3" (L) x 1.3" (W) x 12.0" (H)</li> <li>440mm (L) x 33mm (W) x 305mm (H)</li> </ul>
Load Module Weights	<ul><li>Module only: 12.9 lbs (5.85 kg)</li><li>Shipping: 19.7 lbs (8.94 kg)</li></ul>
Temperature	<ul> <li>Operating: 41°F to 104°F (5°C to 40°C)</li> <li>Storage: 41°F to 122°F (5°C to 50°C)</li> </ul>

Feature	NOVUS-NP 10/1GE16DP 10G/1G/100M	NOVUS-NP 10/1GE8DP 10G/1G/100M	
Humidity	<ul><li>Operating: 0% to 85%, non-condensing</li><li>Storage: 0% to 85%, non-condensing</li></ul>		
Chassis Capacity: Ma	aximum Number of Cards and	Ports per Chassis Model	
XGS12-SD Chassis (940-0011)	<ul><li>12 load modules:</li><li>192-ports of 10GbE</li><li>192-ports of 1GbE</li><li>192-ports of 100MbE</li></ul>	<ul><li>12 load modules:</li><li>96-ports of 10GbE</li><li>96-ports of 1GbE</li><li>96-ports of 100MbE</li></ul>	
XGS12-HSL Chassis (940-0016)	12 load modules:  • 192-ports of 10GbE  • 192-ports of 1GbE  • 192-ports of 100MbE	12 load modules:  • 96-ports of 10GbE  • 96-ports of 1GbE  • 96-ports of 100MbE	
XGS2-SD Chassis (940-0010)	2 load modules:  • 32-ports of 10GbE  • 32-ports of 1GbE  • 32-ports of 100MbE	<ul><li>2 load modules:</li><li>16-ports of 10GbE</li><li>16-ports of 1GbE</li><li>16-ports of 100MbE</li></ul>	
XGS2-HSL Chassis (940-0014)	2 load modules:  • 32-ports of 10GbE  • 32-ports of 1GbE  • 32-ports of 100MbE	<ul><li>2 load modules:</li><li>16-ports of 10GbE</li><li>16-ports of 1GbE</li><li>16-ports of 100MbE</li></ul>	
Transmit Feature Sp	ecifications		
Transmit Engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures.		
Max. Streams per Port	512		
Max. Streams per Port in Data Center Ethernet	256		
Stream Controls	Rate and frame size change on the fly, sequential, and advanced stream scheduler.		
Minimum Frame Size	<ul> <li>10GbE:</li> <li>49 bytes at full line rate without UDF60 bytes at full line rate with UDF</li> <li>1GbE and 100MbE:</li> <li>49 bytes at less than full line rate</li> </ul>		

Feature	NOVUS-NP 10/1GE16DP NOVUS-NP 10/1GE8DP 10G/1G/100M	
Maximum Frame Size	16,384 bytes	
Maximum Fame Size in Data Center Eth- ernet	9,216 bytes	
Priority Flow Control	<ul> <li>8 line-rate-capable queues with each supporting up to 2,500 byte frame lengths</li> <li>1 queue supporting up to 9,216 byte frame lengths</li> </ul>	
Frame Length Controls	Fixed, increment by user-defined step, weighted pairs, uniform, repeatable random, IMIX, and Quad Gaussian	
User defined fields (UDF)	Fixed, increment or decrement by user-defined step, sequence, value list, and random configurations. Up to ten, 32-bit wide UDFs are available.	
Value Lists (max.)	2M across 5 User Defined Fields	
Sequence (max.)	512	
Error Generation	Generate good CRC or force bad CRC, undersize and oversize standard Ethernet frame lengths, and bad checksum.	
Hardware Checksum Generation	Checksum generation and verification for IPv4, IP over IP, ICMP/GRE/TCP/UDP, L2TP, GTP.	
Link Fault Signaling	10GE: Reports, no fault, remote fault, and local fault port statistics; ability to select the option to have the transmit port ignore link faults from a remote link partner	
Latency Measurement Resolution	2.5 nanoseconds	
Transmit line clock adjustment	Ability to adjust the parts-per-million line frequency over a range of -100 ppm to +100 ppm across all ports on the load module.	
Receive Feature Spe	cifications	
Receive Engine	Wire-speed packet filtering, capturing, real-time latency and inter-arrival time for each packet group, with data integrity, sequence, and advanced sequence checking capability.	
Trackable Receive Flows per Port	<ul> <li>1M without Tx/Rx Sync and sequence checking</li> <li>512k with Tx/Rx Sync and sequence checking</li> </ul>	
Minimum Frame Size	<ul><li>64 bytes at full line rate into the capture buffer</li><li>49 bytes at less than full line rate</li></ul>	
Filters (User-Defined Statistics, UDS)	2 SA/DA pattern matchers, 2x16-byte user-definable patterns with offsets capability for start of: frame, IP, or protocol. Up to 6 UDS counters are available.	

Feature	NOVUS-NP 10/1GE16DP 10G/1G/100M	NOVUS-NP 10/1GE8DP 10G/1G/100M	
Hardware Capture Buffer per Port or Resource Group	512MB per port		
Statistics and Rates	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 user-defined stats, capture trigger (UDS 3), capture filter (UDS 4), 8 QoS counters, data integrity frames, data integrity errors, sequence and advanced sequence checking frames, sequence checking errors, ARP, and PING requests and replies.		
Latency / Jitter Meas- urements	Cut-through, store and forward, f Latency bins / jitter, MEF frame of		
Layer 2-3 Protocol S	upport		
Routing and Switching	BGP4/BGP4+, OSPFv2/v3, ISISvaRIP/RIPng, BFD, IGMP/MLD, PIMPVST+/RPVST+, Link Aggregation	-SM/SSM, STP/RSTP/MSTP,	
Software Defined Network	OpenFlow, Segment Routing, BGP Link State (BGP-LS), PCEP, VXLAN, EVPN VXLAN, OVSDB, GENEVE.		
MPLS	RSVP-TE P2P/P2MP, LDP/LDPv6/mLDP, LDP L2VPN (PWE/VPLS), BGP VPLS, L3VPN/6VPE, 6PE, BGP RFC3107, MPLS-TP, MPLS OAM, EVPN/PBB-EVPN, Multicast VPN Rosen Draft, NG Multicast VPN.		
Broadband and Authentication	PPPoX/L2TPv2, DHCPv4/DHCPv6, ANCP, IPv6 Autoconfiguration (SLAAC), IGMP/MLD, IPTV, 802.1x, WebAuth, EAPoUDP, Cisco NAC.		
Industrial Ethernet	Link OAM (IEEE 802.3ah), CFM/Y.1731, PBB/PBB-TE, ELMI, TWAMP, Sync-E ESMC, IEEE 1588v2 (PTP), gPTP (IEEE 802.1AS), MSRP (IEEE 802.1 Qat), IEEE 1722.		
Data Center Ethernet	DCBX/LLDP, FCoE/FIP, PFC (IEEE ricPath, SPBM, VEPA.	802.1Qbb), TRILL, Cisco Fab-	
Layer 4-7 Application	Layer 4-7 Application Traffic Testing Support		
Data	HTTP, HTTPS, TCP Session, FTP, DNS, Mail (SMTP, POP3, and IMAP),TFTP, AppReplay, AppLibrary.		
Video	RTSP, IPTV, VoD, Adobe Flash Client, Apple HLS Client, Microsoft Silverlight Client, Adobe HDS Client, DASH Client; includes Video Quality VQMON and TCP Video Quality.		
Voice	Advanced VoIP SIP & RTP, Audio & Video Codecs, VoLTE, MSRP, Telepresence, SMS, T.38; includes: Voice Quality and Video Quality for conversational video traffic.		

Feature	NOVUS-NP 10/1GE16DP 10G/1G/100M	NOVUS-NP 10/1GE8DP 10G/1G/100M
Storage	iSCSI, CIFSv1, CIFSv2 (SMB2), SMB3, NFSv3 Client, NFSv4 Client, NFS4.1 Client, Cloud Storage Client.	
Access	IPv4, IPv6, VLAN, Emulated Routers, DNS, DHCP.	

The Ixia application support for Novus-NP 10G/1G/100M load modules is provided in the following table:

Novus-NP 10G/1G/100M Application Support

Application	Support
IxNetwork	Provides wire-rate traffic generation with service modeling that builds realistic, dynamically-controllable data-plane traffic. IxNetwork offers the industry's best test solution for functional and performance testing by using comprehensive emulation for routing, switching, MPLS, IP multicast, broadband, authentication, Carrier Ethernet, and data center Ethernet protocols.
IxExplorer	Provides layer 2-3 wire-speed traffic generation and analysis test application.
Tcl API	Allows custom user script development for layer 2-7 testing.
IxLoad	Provides a scalable L4-7 solution for testing converged multiplay services, application delivery platforms, and security devices and systems. IxLoad ensures quality of experience (QoE) through emulation of data, access, storage, voice and video subscribers, and associated protocols.

# **Mechanical Specifications**

#### **Front Panel**

The front panel of one of the Novus 10G/1G/100M load module is shown in the following figure:

Figure: Front panel of NOVUS-NP 10/1GE16DP



#### **LED Panel**

There are 2 bicolor LEDs per port for the SFP+ (10G) variant. The LED panel specifications for Novus SFP+ (10G) are provided in the following table.

LED panel Specifications for Novus-NP Load Module

Speed Mode	LED1: TX LED	LED2: RX LED
10GE	Port Inactive/No Power=Off	Port Inactive/No Power=Off
	Link Down (all)=Solid Red	Rx Active with Errors=Blinking
	Link Up (all)=Solid Green	Red
	Tx Active=Blinking Green	Rx Active=Blinking Green

#### **Transceivers and Cables**

The Novus 10/1 family supports optical transceivers and fiber cables for each of the physical interfaces that are supported:

• **988-0011**: This is an SFP+10GBASE-SR/SW and 1000BASE-SX optical, dual-rate, 850nm transceiver with pluggable SFP+ interface. It is compatible with all 10/1 Gigabit Ethernet Novus, PerfectStorm, and Firestorm load modules, and appliances.

A 3 meter, multi-mode fiber LC-LC cable is included with this transceiver.

• **988-0012**: This is an SFP+10GBASE-LR/LW and 1000BASE-LX optical, dual-rate, 1310nm transceiver with pluggable SFP+ interface. It is compatible with all 10/1 Gigabit Ethernet Novus, PerfectStorm, and Firestorm load modules, and appliances.

A 10 ft, single-mode fiber LC-LC cable is included with this transceiver.

- 988-0013: This is an SFP+10GBASE-SR/SW, Accessory, 850nm transceiver with pluggable SFP+ interface. It is compatible with 944-0050 (LSM10GXM4S-01), 944-0051 (LSM10GXM8S-01), 944-0052 (LSM10GXMR4S-01), 944-0053 (LSM10GXMR8S-01), 944-0054 (LSM10GXM2S-01), 944-0055 (LSM10GXMR2S-01); and 944-0022 (LSM10G1-01) with 948-0012 (SFP+ADAP-01); or 944-0024 (LSM10GL1-01) with 948-0012 (SFP+ADAP-01).
- 988-0014: This is an SFP+10GBASE-LR/LW, Accessory, 1310nm transceiver with pluggable SFP+ interface. It is compatible with 944-0050 (LSM10GXM4S-01), 944-0051 (LSM10GXM8S-01), 944-0052 (LSM10GXMR4S-01), 944-0053 (LSM10GXMR8S-01), 944-0054 (LSM10GXM2S-01), 944-0055 (LSM10GXMR2S-01); and 944-0022 (LSM10G1-01) with 948-0012 (SFP+ADAP-01); or 944-0024 (LSM10GL1-01) with 948-0012 (SFP+ADAP-01).
- **988-0015**: This is an SFP+10GBASE-LRM, Accessory, 1310nm transceiver, for multimode fiber, with pluggable SFP+ interface. It is compatible with 944-0050 (LSM10GXM4S-01), 944-0051 (LSM10GXM8S-01), 944-0052 (LSM10GXMR4S-01), 944-0053 (LSM10GXMR8S-01), 944-0054 (LSM10GXM2S-01), 944-0055 (LSM10GXMR2S-01); and 944-0022 (LSM10G1-01) with 948-0012 (SFP+ADAP-01); or 944-0024 (LSM10GL1-01) with 948-0012 (SFP+ADAP-01).

SFP+10GBASE-LRM does not support the 10GbE WAN mode in any of the load modules listed above.

- **988-0016**: This is an SFP+10GSFP+Cu, Accessory, passive, copper Direct Attach Cable Assembly, with pluggable SFP+ interface. It is compatible with NGY 10GE SFP+ modules, Xdenisty modules, and Xcellon-Flex 10GE SFP+ FE and AP modules.
- SFP-LX: This is a 1310nm LX, SFP 1 Gigabit Ethernet Transceiver.
- SFP-SX: This is a 850nm SX, SFP 1 Gigabit Transceiver.

# Chapter 37 - IXIA Novus-32P 10GE/1GE/100M Ethernet Load Modules

This chapter provides details about Novus-32P 10/1 family of load modules and their specifications and features.

Novus-32P 10/1 is a tri-speed, high density, with up to 32 ports per module, multi-rate ethernet load module. This load module family supports complete Layer 2-3 (L2-3) network and application testing in a single system. It provides support for SFP+ ports, and enables up to line-rate L2/3 traffic generation and analysis, and high-performance routing/bridging protocol emulation. All these features are available within one load module. It allows ultra-high-density test environments for 10GE/1GE/100M Ethernet and supports up to 384 10GE/1GE/100M Ethernet test ports in a single 12-slot Ixia chassis.

For more information on Novus family of load modules, see Novus Load Modules.

# **Key Features**

The key features of Novus-32P 10/1 load module are as follows:

- Provides ultra-high scale and performance for emulating L2/3 protocols to validate performance and scalability of L2/3 routing/switching and data center test cases using Ixia's IxNetwork application
- Supports full line-rate traffic generation to evaluate ASIC designs, FPGAs, and hardware switch fabrics
- Allows industry-standard RFC test and protocol emulation in large test bed with hundreds of 10G, 1G, and/or 100M ports in a single test. This helps to benchmark data plane, performance, and scale of ultra-high-density network equipment.
- 10G, 1G, and 100M line-rate hardware packet capture and decode tools to detect and debug data transmission errors
- Provides a broad range of application support including: IxExplorer, IxNetwork, and the related Tcl and automation APIs
- Has a flexible 4:1 CPU and memory aggregation, for high-scale protocol emulation and performance
- Uses flexible custom packet generation
- Provides real-time latency with latency resolution of up to 2.5ns
- Enables extensive port and traffic flow statistics
- Allows advanced sequence checking with duplicate packet detection

#### **Load Modules**

The Novus-32P 10/1 family is available in the following model:

• NOVUS10/1GE32S

The load module is described as follows:

## NOVUS10/1GE32S

NOVUS10/1GE32S is a 32-port, SFP+ 10GE/1GE/100M load module designed for high-density requirements. It is compatible with the XGS12-SD rack mount chassis (940-0011), XGS12-HSL, 12-slot high speed rackmount chassis (940-0016), XGS2-SD 2-slot standard performance chassis (940-0010), and the XGS2-HSL, 2-slot high performance chassis (940-0014).

The NOVUS10/1GE32S load module is shown in the following figure:

Figure: Novus Module-NOVUS10/1GE32S



## **Part Numbers**

Part Numbers for Novus-32P 10G/1G/100M Load Modules and Supported Adapters are provided in the following table.

Part Numbers for Novus-32P 10G/1G/100M Modules

Part Number	Description
	• 32-ports of SFP+
944-1141	• 1-slot
	• L2-3 support

# **Specifications**

The load module specifications are contained in the following table.

Novus-32P 10G/1G/100M Load Module Specifications

Feature	NOVUS 10/1GE32S 10G/1G/100M	
Hardware Load Module Specifications		
Slot / Number of Ports	1-slot with 32x10/1G SFP+ ports	
Physical Interfaces	32-ports of SFP+	
Supported Port Speeds	10G, 1G, 100M	
CPU and Memory	Multicore processor with 2GB of CPU memory per port	
Cable Media	<ul><li>CAT5e</li><li>CAT6</li><li>CAT6A</li></ul>	
Load Module Dimen-	• 16.4" (L) x 1.3" (W) x 12.0" (H)	

Feature	NOVUS 10/1GE32S 10G/1G/100M	
sions	• 417mm (L) x 33mm (W) x 305mm (H)	
Load Module Weights	<ul><li>Module only: 11.4 lbs (5.15 kg)</li><li>Shipping: 18.2 lbs (8.26 kg)</li></ul>	
Temperature	<ul> <li>Operating: 41°F to 95°F (5°C to 35°C)</li> <li>Storage: 41°F to 122°F (5°C to 50°C)</li> </ul>	
Humidity	<ul><li>Operating: 0% to 85%, non-condensing</li><li>Storage: 0% to 85%, non-condensing</li></ul>	
Chassis Capacity: Max	kimum Number of Cards and Ports per Chassis Model	
XGS12-SD Chassis (940-0011)	<ul><li>12 load modules:</li><li>384-ports of 10GbE</li><li>384-ports of 1GbE</li><li>384-ports of 100MbE</li></ul>	
XGS12-HSL Chassis (940-0016)	12 load modules:  • 384-ports of 10GbE  • 384-ports of 1GbE  • 384-ports of 100MbE	
XGS2-SD Chassis (940- 0010)	<ul><li>2 load modules:</li><li>64-ports of 10GbE</li><li>64-ports of 1GbE</li><li>64-ports of 100MbE</li></ul>	
XGS2-HSL Chassis (940- 0014)	2 load modules:  • 64-ports of 10GbE  • 64-ports of 1GbE  • 64-ports of 100MbE	
Transmit Feature Spe	cifications	
Transmit Engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures.	
Max. Streams per Port	512	
Max. Streams per Port in Data Center Ethernet	256	
Stream Controls	Rate and frame size change on the fly, sequential, and advanced stream scheduler.	
Minimum Frame Size	10GbE:	

Feature	NOVUS 10/1GE32S 10G/1G/100M	
	<ul> <li>49 bytes at full line rate without UDF60 bytes at full line rate with UDF</li> </ul>	
	1GbE and 100MbE:	
	49 bytes at less than full line rate	
Maximum Frame Size	16,384 bytes	
Maximum Fame Size in Data Center Ethernet	9,216 bytes	
Priority Flow Control	<ul> <li>8 line-rate-capable queues with each supporting up to 2,500 byte frame lengths</li> <li>1 queue supporting up to 9,216 byte frame lengths</li> </ul>	
Frame Length Controls	Fixed, increment by user-defined step, weighted pairs, uniform, repeatable random, IMIX, and Quad Gaussian	
User defined fields (UDF)	Fixed, increment or decrement by user-defined step, sequence, value list, and random configurations. Up to ten, 32-bit wide UDFs are available.	
Value Lists (max.)	2M across 5 User Defined Fields	
Sequence (max.)	512	
Error Generation	Generate good CRC or force bad CRC, undersize and oversize standard Ethernet frame lengths, and bad checksum.	
Hardware Checksum Generation	Checksum generation and verification for IPv4, IP over IP, ICMP/GRE/TCP/UDP, L2TP, GTP.	
Link Fault Signaling	10GE: Reports, no fault, remote fault, and local fault port statistics; ability to select the option to have the transmit port ignore link faults from a remote link partner	
Latency Measurement Resolution	2.5 nanoseconds	
Transmit line clock adjustment	Ability to adjust the parts-per-million line frequency over a range of -100 ppm to +100 ppm across all ports on the load module.	
Receive Feature Spec	ifications	
Receive Engine	Wire-speed packet filtering, capturing, real-time latency and inter-arrival time for each packet group, with data integrity, sequence, and advanced sequence checking capability.	
Trackable Receive Flows per Port	<ul> <li>1M without Tx/Rx Sync and sequence checking</li> <li>512k with Tx/Rx Sync and sequence checking</li> </ul>	
Minimum Frame Size	<ul><li>64 bytes at full line rate into the capture buffer</li><li>49 bytes at less than full line rate</li></ul>	

Feature	NOVUS 10/1GE32S 10G/1G/100M
Filters (User-Defined Statistics, UDS)	2 SA/DA pattern matchers, 2x16-byte user-definable patterns with offsets capability for start of: frame, IP, or protocol. Up to 6 UDS counters are available.
Hardware Capture Buffer per Port or Resource Group	512MB per port
Statistics and Rates	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 user-defined stats, capture trigger (UDS 3), capture filter (UDS 4), 8 QoS counters, data integrity frames, data integrity errors, sequence and advanced sequence checking frames, sequence checking errors, ARP, and PING requests and replies.
Latency / Jitter Meas- urements	Cut-through, store and forward, forwarding delay, up to 16 Latency bins / jitter, MEF frame delay, and inter-arrival time.
Layer 2-3 Protocol Sup	pport
Routing and Switching	BGP4/BGP4+, OSPFv2/v3, ISISv4/v6, EIGRP/EIGRPv6, RIP/RIPng, BFD, IGMP/MLD, PIM-SM/SSM, STP/RSTP/MSTP, PVST+/RPVST+, Link Aggregation (LACP), LISP.
Software Defined Network	OpenFlow, Segment Routing, BGP Link State (BGP-LS), PCEP, VXLAN, EVPN VXLAN, OVSDB, GENEVE.
MPLS	RSVP-TE P2P/P2MP, LDP/LDPv6/mLDP, LDP L2VPN (PWE/VPLS), BGP VPLS, L3VPN/6VPE, 6PE, BGP RFC3107, MPLS-TP, MPLS OAM, EVPN/PBB-EVPN, Multicast VPN Rosen Draft, NG Multicast VPN.
Broadband and Authentication	PPPoX/L2TPv2, DHCPv4/DHCPv6, ANCP, IPv6 Autoconfiguration (SLAAC), IGMP/MLD, IPTV, 802.1x, WebAuth, EAPoUDP, Cisco NAC.
Industrial Ethernet	Link OAM (IEEE 802.3ah), CFM/Y.1731, PBB/PBB-TE, ELMI, TWAMP, Sync-E ESMC, IEEE 1588v2 (PTP), gPTP (IEEE 802.1AS), MSRP (IEEE 802.1 Qat), IEEE 1722.
Data Center Ethernet	DCBX/LLDP, FCoE/FIP, PFC (IEEE 802.1Qbb), TRILL, Cisco FabricPath, SPBM, VEPA.

The Ixia application support for Novus-32P 10G/1G/100M load modules is provided in the following table:

Novus-32P 10G/1G/100M Application Support

Application	Support
IxNetwork	Provides wire-rate traffic generation with service modeling that builds realistic, dynamically-controllable data-plane traffic. IxNetwork offers the industry's best test solution for functional and performance testing by using comprehensive emulation for routing, switching, MPLS, IP multicast, broadband, authentication, Carrier Ethernet, and data center Ethernet protocols.
IxExplorer	Provides layer 2-3 wire-speed traffic generation and analysis test application.
Tcl API	Allows custom user script development for layer 2-7 testing.

# **Mechanical Specifications**

#### **Front Panel**

The front panel of one of the Novus-32P 10G/1G/100M load module is shown in the following figure:

Figure: Front panel of NOVUS-32P NOVUS10/1GE32S



#### **LED Panel**

There are 2 bicolor LEDs per port for the SFP+ (10G) variant. The LED panel specifications for Novus-32P SFP+ (10G) are provided in the following table.

LED panel Specifications for Novus-32P Load Module

Speed Mode	LED1: TX LED	LED2: RX LED
10GE	Port Inactive/No Power=Off	Port Inactive/No Power=Off
	Link Down (all)=Solid Red	Rx Active with Errors=Blinking
	Link Up (all)=Solid Green	Red
	Tx Active=Blinking Green	Rx Active=Blinking Green

#### **Transceivers and Cables**

The Novus-32P 10/1 family supports optical transceivers and fiber cables for each of the physical interfaces that are supported:

• **988-0011**: This is an SFP+10GBASE-SR/SW and 1000BASE-SX optical, dual-rate, 850nm transceiver with pluggable SFP+ interface. It is compatible with all 10/1 Gigabit Ethernet Novus, PerfectStorm, and Firestorm load modules, and appliances.

A 3 meter, multi-mode fiber LC-LC cable is included with this transceiver.

• **988-0012**: This is an SFP+10GBASE-LR/LW and 1000BASE-LX optical, dual-rate, 1310nm transceiver with pluggable SFP+ interface. It is compatible with all 10/1 Gigabit Ethernet Novus, PerfectStorm, and Firestorm load modules, and appliances.

A 10 ft, single-mode fiber LC-LC cable is included with this transceiver.

- 988-0013: This is an SFP+10GBASE-SR/SW, Accessory, 850nm transceiver with pluggable SFP+ interface. It is compatible with 944-0050 (LSM10GXM4S-01), 944-0051 (LSM10GXM8S-01), 944-0052 (LSM10GXMR4S-01), 944-0053 (LSM10GXMR8S-01), 944-0054 (LSM10GXM2S-01), 944-0055 (LSM10GXMR2S-01); and 944-0022 (LSM10G1-01) with 948-0012 (SFP+ADAP-01); or 944-0024 (LSM10GL1-01) with 948-0012 (SFP+ADAP-01).
- 988-0014: This is an SFP+10GBASE-LR/LW, Accessory, 1310nm transceiver with pluggable SFP+ interface. It is compatible with 944-0050 (LSM10GXM4S-01), 944-0051 (LSM10GXM8S-01), 944-0052 (LSM10GXMR4S-01), 944-0053 (LSM10GXMR8S-01), 944-0054 (LSM10GXM2S-01), 944-0055 (LSM10GXMR2S-01); and 944-0022 (LSM10G1-01) with 948-0012 (SFP+ADAP-01); or 944-0024 (LSM10GL1-01) with 948-0012 (SFP+ADAP-01).
- 988-0015: This is an SFP+10GBASE-LRM, Accessory, 1310nm transceiver, for multimode fiber, with pluggable SFP+ interface. It is compatible with 944-0050 (LSM10GXM4S-01), 944-0051 (LSM10GXM8S-01), 944-0052 (LSM10GXMR4S-01), 944-0053 (LSM10GXMR8S-01), 944-0054 (LSM10GXM2S-01), 944-0055 (LSM10GXMR2S-01); and 944-0022 (LSM10G1-01) with 948-0012 (SFP+ADAP-01); or 944-0024 (LSM10GL1-01) with 948-0012 (SFP+ADAP-01).

SFP+10GBASE-LRM does not support the 10GbE WAN mode in any of the load modules listed above.

- **988-0016**: This is an SFP+10GSFP+Cu, Accessory, passive, copper Direct Attach Cable Assembly, with pluggable SFP+ interface. It is compatible with NGY 10GE SFP+ modules, Xdenisty modules, and Xcellon-Flex 10GE SFP+ FE and AP modules.
- SFP-LX: This is a 1310nm LX, SFP 1 Gigabit Ethernet Transceiver.
- SFP-SX: This is a 850nm SX, SFP 1 Gigabit Transceiver.
- **SFP-FX-100M-XCVR**: This is a SFP 100BASE-FX 100M pluggable optical transceiver with MMF (multimode), 1310nm, and a 2km reach.



# Chapter 38 - IXIA PerfectStorm Load Modules

This chapter provides details about PerfectStorm 10GE, 40GE and 100GE family of load modules specifications and features.

Ixia's PerfectStorm family of load modules is a scalable solution for testing converged multi-play services, application delivery, and network security platforms for both wired and wireless networks.

The PerfectStorm product family consists of a new next generation XGS12 chassis platform, an XGS integrated system controller for both IxLoad and BreakingPoint and load modules 8x10GE, 2x40GE and 1x100GE. The PerfectStorm10GE, 40GE, and 100GE load modules have two variants, fusion (IxLoad and BreakingPoint) and non-fusion (IxLoad only). The key feature of PerfectStorm 10GE/40GE/100GE NG cards is the fusion between IxLoad and BreakingPoint applications.

PerfectStorm supports the following:

- both IxLoad and BreakingPoint software applications; BPS runs on the fusion variants of the load module
- native 40GE QSFP+ and 100GE CXP interfaces
- line-rate application performance per interface
- hardware-based acceleration for SSL and IPsec performance

## **Key Features**

The key features of PerfectStorm load modules are as follows:

#### **Unified Applications and Security Test Platform**

PerfectStorm is a unified applications and security test platform, with support for BreakingPoint and IxLoad software.

#### **Networking Interfaces per Blade**

- 8 x 10GE
- 2 x 40GE
- 1 x 100GE

#### **Blended Application Traffic**

PerfectStorm Fusion can create blended application traffic and current security attacks with a very high count of concurrent wired and wireless users from a single 11u chassis.

#### **Massive Scale Real-World Traffic Conditions**

PerfectStorm tests and validates IT systems under controlled real-world scenarios that model your own unique environments. It understands actual performance, system limitations, and real security posture in a better way, to right size data centers and eliminate incidents in production. It generates stateful applications and malicious traffic that simulate millions of real-world end-user environments to test and validate infrastructure, a single device, or an entire system. This includes complex data, video, voice, storage, and network application workloads.

#### **Real Attacks**

- 6,000+ live security attacks, 35,000+ pieces of live malware found in enterprise, core, and mobile networks, 180+ evasions
- DDoS and botnet simulation and custom attacks
- Research and frequent updatesHardware-based Acceleration

#### **Multi-user Environment**

PerfectStorm's multi-user environment leverages the per port user ownership model for all ports on the test modules installed into the chassis.

#### **High-performing Business Applications**

PerfectStorm ensures high-performing, and more available and secure business applications.

#### **Disaster Recovery**

PerfectStorm validates disaster recovery and business continuity.

#### **Reduced Legal Exposure**

PerfectStorm provides reduced legal exposure due to data loss by validating security using the industry's most up to date application and threat intelligence.

## **Platform Support**

PerfectStorm is equipped with powerful multi-core, multi-threaded network processors, to satisfy the testing needs of equipment manufacturers having higher-density 10GE and 40GE equipments. As service providers and large enterprises prepare to deploy these equipments in their own networks, they must test and verify performance and functionality prior to deployment.

PerfectStorm's single, integrated system equipped with 12 PerfectStorm blades allows control of application traffic to nearly a terabit, up to 720 million concurrent connections, and new TCP connection rates of up to 24 Million. The hardware-based acceleration supports massive encryption levels. The system uses inline field programmable gate arrays (FPGAs) for enhanced accuracy pertaining to latency measurements with a resolution of 10ns.

PerfectStorm is compatible with XGS12, which is a 12-slot Chassis platform. The Chassis platform architecture supports easy setup and management of high scale, multi-user system. The XGS12 chassis platform includes a pluggable system controller for chassis management and web-based UI. This chassis platform is backward compatible with XM2/XM12 blades.

For more information on XGS12, see XGS12 Chassis Platform.

#### **Load Modules**

PerfectStorm load module comprises a two board set, the Main Board and the PHY Card. The Main Board contains the backplane interface, processors and FPGAs. The card occupies one slot in the XGS12 chassis platform and consumes no more than 400W of power.

The PerfectStorm family consists of the following models:

- PerfectStorm 10GE 8-port (SFP+)
- PerfectStorm Fusion 10GE 8-port (SFP+)
- PerfectStorm 40GE 2-port (QSFP+)
- PerfectStorm Fusion 40GE 2-port (QSFP+)
- PerfectStorm 100GE1 1-port (CXP)
- PerfectStorm 100GE1NG 1-port (CXP)

Each of these load modules are described as follows:

#### **PS10GE8**

PerfectStorm PS10GE8 is a 8 port 10-Gigabit Ethernet, load module with SFP+ interface. Each 10GE port uses of 1/8th of the network processor and memory resources available on the load module, allowing delivery of application traffic at wire-speeds for each port.It supports only IxLoad software and is compatible with XGS12 chassis platform.

The PS10GE8 load module is shown in the following figure:

Figure: PerfectStorm Module-PS10GE8



#### **PS10GE8NG**

PerfectStorm PS10GE8NG is a 8 port 10-Gigabit Ethernet, fusion load module with SFP+ interface. This mode provides extra flexibility to allocate all available NP resources and memory available on a single module while using a single 10 GE interface to transmit or receive the traffic. Ixia test applications transparently configure the allocation of NP resources to achieve the maximum performance. It supports IxLoad and BreakingPoint software and is compatible with XGS12 chassis platform. The PS10GE8NG load module is shown in the following figure:

Figure: PerfectStorm Module-PS10GE8NG



#### PS40GE2

PerfectStorm PS40GE2 is a 2 port 40-Gigabit Ethernet, load module with QSFP+ interface. Each 40GE port uses of  $\frac{1}{2}$  of the network processor and memory resources available on the load module, allowing delivery of application traffic at wire-speeds for each port. It supports only IxLoad software and is compatible with XGS12 chassis platform.

The PS40GE2 load module is shown in the following figure:

Figure: PerfectStorm Module-PS40GE2



#### PS40GE2NG

PerfectStorm PS40GE2NG is a 2 port 40-Gigabit Ethernet, fusion load module with QSFP+ interface. This mode provides extra flexibility to allocate all network processor and memory resources available on a load module to a single 40GE port. Ixia test applications transparently configure the allocation of NP resources to achieve the maximum performance. It supports IxLoad and BreakingPoint software and is compatible with XGS12 chassis platform.

The PS40GE2NG load module is shown in the following figure:

Figure: PerfectStorm Module-PS40GE2NG



#### **PS100GE1**

PerfectStorm PS100GE1 is a 1-port 100-Gigabit Ethernet load Module with CXP interface. This supports upto 2-ports of 40GE OR 8-ports of 10GE via Fan-out cables. It requires one CXP 100GE pluggable, multimode optical transceiver (948-0030) and a point-to-point, multimode CXP 100GE Active Optical Cable (AOC) (942-0052), or alternatively, one PerfectStorm 100G transceiver and cable bundle to enable support for the native 100G and all the fan-out options (942-0073).

This load module is compatible only with XGS12-HS chassis bundle.

The PS100GE1 load module is shown in the following figure:

Figure: PerfectStorm Module-PS100GE1



#### PS100GE1NG

PerfectStorm PS100GE1NG is a 1-port 100-Gigabit Ethernet fusion load Module with CXP interface. This supports upto 2-ports of 40GE or 8-ports of 10GE via optional Fan-out cables. It requires BreakingPoint Application and Threat Intelligence (ATI) (909-0856), one CXP 100GE pluggable, multimode optical transceiver (948-0030) and a point-to-point, multimode CXP 100GE Active Optical Cable (AOC) (942-0052), or alternatively, one PerfectStorm 100G transceiver and cable bundle to enable support for the native 100G and all the fan-out options (942-0073).

This load module is compatible only with XGS12-HS chassis bundle.

The PS100GE1NG load module is shown in the following figure:





### **Part Numbers**

Part Numbers for PerfectStorm Load Modules and supported adapters are provided in the following table.

Part Numbers for PerfectStorm Modules

Model Number	Part Number	Description
PS10GE8NG	944-1200	<ul><li>8-ports of 10GE with the SFP+ physical interface.</li><li>SSL and IPsec hardware acceleration.</li></ul>
PS10GE8	944-1204	<ul><li>8-ports of 10GE with the SFP+ physical interface.</li><li>SSL and IPsec hardware acceleration.</li></ul>
PS40GE2NG	944-1201	<ul><li>2-ports of 40GE with the SFP+ physical interface.</li><li>SSL and IPsec hardware acceleration.</li></ul>
PS40GE2	944-1205	<ul><li>2-ports of 40GE with the SFP+ physical interface.</li><li>SSL and IPsec hardware acceleration.</li></ul>
PS100GE1NG	944-1202	<ul><li>1-port 100GE CXP interface.</li><li>SSL and IPsec hardware acceleration.</li></ul>
PS100GE1	944-1206	<ul><li>1-port 100GE CXP interface.</li><li>SSL and IPsec hardware acceleration.</li></ul>

# **Specifications**

The load module specifications are contained in the following table.

PerfectStorm Load Module Specifications

	reiit	ectotoriii t	_oad Modu	ie Specific	Lations	
Featur- e	Per- fectStor- m 10GE	Per- fectStor- m Fusion 10GE	Per- fectStor- m 40GE	Per- fectStor- m Fusion 40GE	Per- fectStor- m 100GE	Per- fectStor- m Fusion 100G
Load Modules	PS10GE8	PS10GE8NG	PS40GE2	PS40GE2NG	PS100GE1	PS100GE1NG
Hardware	, Load Module	e Specification	ns	,	,	
Number of Ports	8	8	2	2	1	1
Physical Inter- face	8-port, 10GE SFP+	8-port, 10GE SFP+	2-port, 40GE QSFP+	2-port, 40GE QSFP+	1-port, 100GE CXP	1-port, 100GE CXP
Trans- ceiver Support (plug- gable trans- ceivers)	10GBASE- SR/SW (850 nm) 10GBASE- LR/LW (1310 nm)	10GBASE- SR/SW (850 nm) 10GBASE- LR/LW (1310 nm)	QSFP+, 40GBASE- SR4	QSFP+, 40GBASE- SR4	CXP 100GBASE- SR10	CXP 100GBASE- SR10
Memory	64GB	64GB	64GB	64GB	64GB	64GB
Hard- ware Encryp- tion Off- load	Yes	Yes	Yes	Yes	Yes	Yes
Hard- ware- Based Traffic Capture	N/A	N/A	N/A	N/A	N/A	2GB per 100GbE interface 1GB per 40GbE interface 256 MB per 10GbE interface

Featur- e	Per- fectStor- m 10GE	Per- fectStor- m Fusion 10GE	Per- fectStor- m 40GE	Per- fectStor- m Fusion 40GE	Per- fectStor- m 100GE	Per- fectStor- m Fusion 100G
FPGA Offload	Yes	Yes	Yes	Yes	Yes	Yes
IPv4, IPv6, UDP, TCP	Hardware ch	necksum gene	eration			
MTU(IP)	8900B	8900B	8900B	8900B	8900B	8900B
Load Module Dimen- sions	, ,	00" (W) x 1.3 x 305 mm (W	'' (H) ') x 33 mm (H	)		
Oper- ating Tem- perature Range	41°F to 95°F (5°C to 35°C), ambient air					
Chassis C	apacity					
Cards per Chassis	12	12	12	12	12	12
Port Density per XGS12 Chassis	144-port, 10GE SFP+	144-port, 10GE SFP+	24-port, 40GE QSFP+	24-port, 40GE QSFP+	12-port, 100GE CXP	12-port, 100GE CXP
Chassis Com- pat- ibility	XGS12 , XGS2	XGS12 , XGS2	XGS12 , XGS2	XGS12 , XGS2	XGS12 , XGS2	XGS12 , XGS2
XGS12 Chassis Bundles	XGS12-HS (940-0006) XGS12 (940-0007)	XGS12-HS (940-0006)	XGS12-HS (940-0006) XGS12 (940-0007)	XGS12-HS (940-0006)	XGS12-HS (940-0006)	XGS12-HS (940-0006)
XGS2 Chass- is Bundl-	XGS2-HS (940-0012)	XGS2-HS (940-0012)	XGS2-HS (940-0012)	XGS2-HS (940-0012)	XGS2-HS (940-0012)	XGS2-HS (940-0012)

Featur- e	Per- fectStor- m 10GE	Per- fectStor- m Fusion 10GE	Per- fectStor- m 40GE	Per- fectStor- m Fusion 40GE	Per- fectStor- m 100GE	Per- fectStor- m Fusion 100G
e s						

# **Transceiver and Cable Support**

The transceiver and cable support for PerfectStorm load modules is provided in the following table:

PerfectStorm Transceiver and Cable Support

Hardware	Transceiver/Cable Part Number	Description
PerfectStorm     PS10GE8	988-0011	SFP+, 10Gb/1Gb SR optical Xcvr, 850nm (cable included)
<ul><li>PerfectStorm Fusion PS10GE8NG</li></ul>	988-0012	SFP+, 10Gb/1Gb LR optical Xcvr, 1310nm
PerfectStorm     PS40GE2	948-0028	QSFP+ 40GBASE-SR4 optical trans- ceivers
<ul> <li>PerfectStorm</li> <li>Fusion</li> <li>PS40GE2NG</li> </ul>	942-0041	MT 12-fiber MMF cable, 3-meter length
	948-0030	CXP 100GbE pluggable, multimode optical transceiver
	942-0035	MT cable, 24-filer, Mul- timode fiber, Key Up/Down, 3 meter length
	942-0052	Point-to-point, multimode CXP 100GbE Active Optical Cable (AOC)
<ul><li>PerfectStorm PS100GE1</li><li>PerfectStorm</li></ul>	942-0072	CXP-to-2x40GbE QSFP Active Optical Cable (AOC), 850nm, 3 meter cable to support the fan-out option
Fusion PS100GE1NG		PerfectStorm Transceiver and Cable bundle containing the following:
PS100GEING	942-0073	<ul> <li>(942-0035) MT cable, 24-filer, Multimode fiber, Key Up/Down, 3 meter,</li> <li>(942-0052) Multis, CXP-to-CXP 100GE Active Optical Cable, point-to-point (AOC), 3M,</li> <li>(942-0064) MT-to-8x10GE LC fanout, MMF, 3-meter cable,</li> </ul>

Hardware	Transceiver/Cable Part Number	Description
		<ul> <li>(942-0072) PerfectStorm, CXP-to-2x40G QSFP Active Optical Cable (AOC), 850NM,3-METER,</li> <li>(948-0030) Multis, CXP,100GE,MMF,850NM,pluggable transceiver</li> </ul>
	942-0074	CXP-to-2x40GbE QSFP Active Optical Cable (AOC), 850nm, 5 meter cable to support the fan-out option
	942-0064	MT-to-8x10GbE LC fan-out, MMF, 3-meter cable to support the fan-out option
	942-0068	MT-to-4x10GbE LC fan-out, MMF, 5-meter cable to support the fan-out option

# **Application Support**

The Ixia application support for PerfectStorm load modules is provided in the following table:

PerfectStorm Application Support

Hardware	Application Support
PerfectStorm PS10GE8	IxOS, IxLoad, TCL API
PerfectStorm Fusion PS10GE8NG	IxOS, IxLoad, BreakingPoint, TCL API
PerfectStorm PS40GE2	IxOS, IxLoad, TCL API
PerfectStorm Fusion PS40GE2NG	IxOS, IxLoad, BreakingPoint, TCL API
PerfectStorm PS100GE1	IxOS, IxLoad, TCL API
PerfectStorm Fusion PS100GE1NG	IxOS, IxLoad, BreakingPoint, TCL API

# **Mechanical Specifications**

#### **Front Panel**

The Front panel of the 8x10GE, 2x40GE, and 1x100GE PerfectStorm load modules are shown in the following figures (applies to Fusion and non-Fusion versions):

Figure: Front panel of 8x10GE PerfectStorm PS10GE8



Figure: Front panel of 2x40GE PerfectStorm PS40GE2



Figure: Front panel of 2x40GE Fusion PerfectStorm PS40GE2NG



Figure: Front panel of 1x100GE Fusion PerfectStorm PS100GE1NG



Figure: Front panel of 1x100GE PerfectStorm PS100GE1



#### **LED Panel**

The LED panel specifications are provided in the following table.

LED panel specifications of PS10GE8(NG) and PS40GE2(NG) Load Modules

Feature	Specification
Link	<ul><li>OFF indicates link is down</li><li>Solid Green indicates link is up</li></ul>
Тх	<ul><li>Off indicates Tx is inactive</li><li>Blinking Green indicates Tx is active</li></ul>
Rx/Err	<ul> <li>Off indicates Rx is inactive</li> <li>Blinking Red indicates Rx is active with errors</li> <li>Blinking Green indicates Rx is active</li> </ul>

# **Chapter 39 - IXIA CloudStorm Load Modules**

This chapter provides details about CloudStorm 100GE load modules specifications and features.

Ixia's CloudStorm family of load modules is the first multi-terabit application and security test solution. It breaks the SSL and DDoS test barriers, achieving over 960Gbps of traffic with strong encryption and ciphers or 2.4 terabit DDoS throughput in a single chassis.

Each CloudStorm load module supports two native QSFP28 100GE interfaces with an innovative architecture that allows concurrent emulation of complex applications, unprecedented SSL encrypted applications, and a large volume of DDoS traffic to validate your network infrastructure is high performing and secure.

The CloudStorm product family consists of 100GE load modules that have two variants, fusion (IxLoad and BreakingPoint) and non-fusion (IxLoad only). A key feature of CloudStorm 100GE load modules is the fusion between IxLoad and BreakingPoint applications—the industry-leading test solutions for application delivery and security resiliency testing.

CloudStorm supports the following:

- BreakingPoint software application which runs on the fusion variant of the load module and IxLoad which runs on the non-fusion variant
- · QSFP28 interfaces
- hardware-based SSL acceleration delivering 4X encryption performance

## **Key Features**

The key features of CloudStorm load modules are as follows:

#### **Massive Scale Real-World Traffic Conditions**

CloudStorm delivers 3X-application and 4X-SSL-emulation scale over any other test system. It helps NEMs shortening their development cycles, and enterprises and data center operators find the right balance between mitigating security risks and delivering high enduser application performance.

#### **SSL** Acceleration

CloudStorm provides hardware-based SSL acceleration to deliver 80G of encrypted traffic with strong encryption and chiphers.

#### **Multi-user Environment**

CloudStorm's multi-user environment leverages the per port user ownership model for all ports on the test modules installed into the chassis.

#### **Emulate Multi-terbit DDoS**

CloudStorm emulates multi-terbit DDoS and botnet attacks to future-proof security solutions.

#### **Unified Application and Security Test Platform**

CloudStorm provides a unified application and security test platform with layers 2-7 capabilities and support for BreakingPoint and IxLoad software.

## **Platform Support**

CloudStorm provides cloud-grade L4-7 application performance with fully integrated L2/3 stateless traffic support. It exercises the systems under test in real world conditions, helping the customers to easily identify the performance and interoperability issues. The modular architecture of the solution allows linear performance scaling to multi terabit, by populating an Ixia's XGS12-HSL chassis with multiple CloudStorm load modules—up to 12.

CloudStorm is compatible with XGS12-HSL, a 12-slot chassis platform and XGS2-HSL, a 2-slot chassis platform. The Chassis platform architecture supports easy setup and management of high scale, multi-user system.

For more information on XGS12 and XGS2, see the following:

- XGS12 Chassis Platform
- XGS2 Chassis Platform

#### **Load Modules**

Each CloudStorm load module supports two native QSFP28 100GE interfaces with an innovative architecture that allows concurrent emulation of complex applications, unprecedented SSL encrypted applications, and a large volume of DDoS traffic to validate your network infrastructure is high performing and secure.

The dual-port capabilities of CloudStorm enable 100GE inline devices like firewalls to be tested with a single card. The CloudStorm load module also includes a mission control center CPU (MCC) equipped with dedicated memory and a solid-state drive (SSD) to accelerate boot time and reduce test configuration time.

The CloudStorm family consists of the following models:

- CloudStorm 100GE 2-port QSFP28
- CloudStorm Fusion 100GE 2-port QSFP28

Each of these load modules are described as follows:

## CS100GE2Q28

CloudStorm CS100GE2Q28 is a 2 port 100-Gigabit Ethernet, load module with QSFP28 interface. It provides support for native QSFP28 100GE pluggable multi-mode optical transceiver or single-mode optical transceiver. It is compatible only with XGS12-HSL and XGS2-HSL chassis.

This load module supports only IxLoad software application.

The CS100GE2Q28 load module is shown in the following figure:

Figure: CloudStorm Module-CS100GE2Q28



## **CS100GE2Q28NG**

CloudStorm CS100GE2Q28NG is a 2 port 100-Gigabit Ethernet, fusion load module with QSFP28 interface. It provides support for native QSFP28 100GE pluggable multi-mode optical transceiver or single-mode optical transceiver. It is compatible only with XGS12-HSL and XGS2-HSL chassis.

This load module supports both IxLoad and BreakingPoint software applications.

The CS100GE2Q28NG load module is shown in the following figure:

Figure: CloudStorm Module-CS100GE2Q28NG



#### **Part Numbers**

Part Numbers for CloudStorm Load Modules and supported adapters are provided in the following table.

Part Numbers for CloudStorm Modules

Model Num- ber	Part Number	Description
CS100GE2Q28	944-1232	2-ports of 100GE with the QSFP28 physical interface.
CS100GE2Q28NG	944-1231	2-ports of 100GE with the QSFP28 physical interface.

# **Specifications**

The load module specifications are contained in the following table.

CloudStorm Load Module Specifications

Feature	CloudStorm 100GE	CloudStorm Fusion 100G			
Load Modules	CS100GE2Q28	CS100GE2Q28NG			
Hardware, Load Module Specifications					

Feature	CloudStorm 100GE	CloudStorm Fusion 100G		
Physical Interfaces	2-port, 100GE QSFP28			
Transceiver Support	QSFP28 SR4 and LR4 (pluggab	le transceivers)		
Memory	128GB	128GB		
Hardware Encryption Off- load	Yes	Yes		
Hardware-Based Traffic Capture (for Break- ingPoint)	N/A	2GB per 100GB interface		
Capture Memory (for IxLoad)	Maximum between 2GB or 2 Million packets, per interface	Maximum between 2GB or 2 Million packets, per interface		
FPGA Offload	Yes	Yes		
IPv4, IPv6, UDP, TCP	Hardware checksum generation			
Load Module Dimensions	16.4" (L) x 12.0" (W) x 1.3" (H)			
Load Module Difficusions	417mm (L) x 305mm (W) x 33mm (H)			
Operating Temperature Range	41°F to 95°F (5°C to 35°C), an	nbient air		
Chassis Capacity				
Cards per Chassis	<ul><li>12 on XGS12-HSL</li><li>2 on XGS2-HSL</li></ul>			
Port Density	<ul><li>XGS12-HSL: 24-ports, 100GE QSFP28</li><li>XGS2-HSL: 4-ports, 100GE QSFP28</li></ul>			
XGS12 and XGS2 Chassis Bundles	<ul><li>XGS12-HSL (940-0016)</li><li>XGS2-HSL (940-0014)</li></ul>	<ul><li>XGS12-HSL (940-0016)</li><li>XGS2-HSL (940-0014)</li></ul>		

# **Transceiver and Cable Support**

The transceiver and cable support for CloudStorm load modules is provided in the following table:

CloudStorm Transceiver and Cable Support

Hardware	Transceiver/Cable Part Number	Description
<ul><li>CloudStorm CS100GE2Q28</li><li>CloudStorm Fusion</li></ul>	QSFP28-SR4-XCVR	QSFP28 100GBASE-SR4 100GE pluggable optical transceiver, MMF (multimode), 850 nm, 100 m reach
CS100GE2Q28NG	QSFP28-LR4-XCVR	QSFP28 100GBASE-LR4 100GE

Hardware	Transceiver/Cable Part Number	Description
		pluggable optical transceiver, SMF (single mode fiber), 1310 nm, 10 km reach
	942-0088	QSFP28 passive, copper, Direct Attach Cable (DAC), 3 meter length
	942-0092	QSFP28 Active Optical Cable (AOC), multimode fiber, 850 nm, 3 meter length

# **Application Support**

The Ixia application support for CloudStorm load modules is provided in the following table:

CloudStorm Application Support

Hardware	Application Support
CloudStorm CS100GE2Q28	IxOS, IxLoad, TCL API
CloudStorm Fusion CS100GE2Q28NG	IxOS, IxLoad, BreakingPoint, TCL API

# **Mechanical Specifications**

#### **Front Panel**

The Front panel of the CloudStorm load module is shown in the following figures (applies to Fusion and non-Fusion versions):

Figure: Front panel of 100GE Fusion CloudStorm CS100GE2Q28NG



Figure: Front panel of 100GE CloudStorm CS100GE2Q28



#### **LED Panel**

There are 3 tricolor LEDs per port. The LED panel specifications for CloudStorm are provided in the following table.

LED panel Specifications for CloudStorm Load Module

Speed Mode	LED1: TX LED	LED2: RX LED	LED3: MODE LED
100GE	Port Inactive/No Power-r=Off Link Down (all)=Solid Red Link Up (all)=Solid Green Tx Active=Blinking Green	Port Inactive/No Power- r=Off  Rx Active with Error- s=Blinking Red  Rx Active=Blinking  Green	Mode=Off Card Fault=Solid Red

## Remove and Insert SSD on CloudStorm

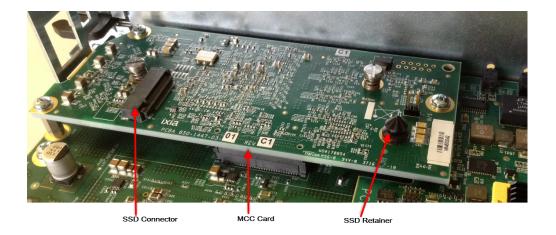
You can remove the Solid State Drive (SSD) on the CloudStorm load module and insert it back when needed.

#### To remove the SSD:

Bend the top of the retainer away from the SSD card. The SSD will spring upward. Now pull the SSD card straight out.



The SSD edge connector on the MCC card is shown in the following figure.



To insert SSD, do the following:

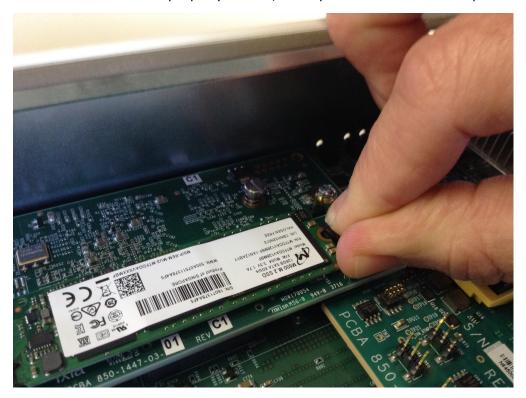
1. Align SSD edge connector with SSD connector on the MCC card.



2. Insert SSD edge connector and push SSD downward towards the MCC card.



3. With your finger, bend the top of the retainer away from the SSD card and push the SSD downward until it hits the retainer. Now release the retainer. If the SSD card is properly seated, the top of the retainer will capture the SSD card.



4. The SSD card is now properly placed on the MCC card.





# Chapter 40 - IXIA Xdensity XDM10G32S/8S Load Modules

#### XDM10G32S Load Modules

This section provides details about Xdensity family of load modules specifications and features. The IxExplorer name of this load module is XDM10G32S.

Xdensity is a 32 port load module with 10GE density per port. Each slot in this load module consists of 32 ports that can scale up to 384 ports in a single XM12 chassis. The high scalability feature of Xdensity load module provides test solutions for high density 10GE converged data center switches and routers.

The key features of Xdensity load module are mentioned as follows:

#### **Key Features**

- An optimum solution for testing ultra-high-density 10GE switches
- Economical, energy-efficient solution for the build-out of large 10GE testbeds
- Industry's leading 10GE SFP+ port density:
  - 32-ports of 10GE in a single-slot load module
  - 384-ports of 10GE SFP+ interfaces in a single 10U rackmount chassis
- Up to 4 users can access the load module at one time, with 8-ports per user
- Compatible with Ixia's XM2, XM12, and XG12 chassis
- Support for host protocol emulation to test layer 3 devices: ARP, NDP, IPv4, IPv6, IGMP, MLD, and DHCPv4/v6 (client and server)
- A targeted set of routing and bridging protocols are supported per port that can be configured with any mix of supported protocols required: BFD, BGPv4/v6, CFM, EIGRP, ISISv4/v6, ISIS-DCE, LDP, Link OAM, OSPFv2, OSPFv3, PIM-SM/SSM-v4/v6, RIP, RIPng, STP/RSTP/MSTP, RSVP-TE
- Data center-ready with data center bridging LLDP/DCBX, FCoE, FIP, FCF, and priority-based flow control (PFC, IEEE802.1Qbb) protocol support
- Built with multicore processor technology

The XDM10G32S load module is shown in the following figure:

Figure: Xdensity Load Module(XDM10G32S)



#### XDM10G8S Load Modules

This section provides details about Xdensity family of load modules specifications and features. The IxExplorer name of this load module is XDM10G8S.

Xdensity is a 8 port load module with 10GE density per port. Each slot in this load module consists of 8 ports that can scale up to 96 ports in a single XM12 or XG12 chassis. The high

scalability feature of Xdensity load module provides test solutions for high density 10GE converged data center switches and routers.

The key features of Xdensity load module are mentioned as follows:

- An optimum solution for testing high density network switches that requires higher per port levels of L23 protocol emulation scale and performance. The XDM10G8S offers up to 4 times higher protocol performance per port compared to the XDM10G32S.
- Energy-efficient solution for 10GE test environments
- 8-ports of 10GE in a single-slot load module
- 96-ports of 10GE SFP+ interfaces in a single 10U rackmount chassis:
  - Compatible with Ixia's XM2, XM12, and XG12 chassis
  - Support for host protocol emulation to test layer 3 devices: ARP, NDP, IPv4, IPv6, IGMP, MLD, and DHCPv4/v6 (client and server)
  - A targeted set of routing and bridging protocols are supported per port that can be configured with any mix of supported protocols required: BFD, BGPv4/v6, CFM, EIGRP, ISISv4/v6, ISIS-DCE, LDP, Link OAM, OSPFv2, OSPFv3, PIM-SM/SSM-v4/v6, RIP, RIPng, STP/RSTP/MSTP, RSVP-TE
  - Built with multicore processor technology
- Compatible with Ixia's XM2 and XM12 chassis
- Compatible with Ixia's XG12 chassis

The XDM10G8S load module is shown in the following figure:

Figure: Xdensity Load Module(XDM10G8S)



#### **Part Numbers**

The part numbers are shown in the following table.

Part Numbers for Xdensity Load Module

Model Number	Part Number	Description
XDM10G32S	944-1080	Xdensity, XDM10G32S, Ultra-high density, 10-Gigabit Ethernet load module with 32-ports of SFP+ interfaces with L2-3 data plane and limited routing protocol emulation support; for XG12 (940-0005) Rackmount chassis, XM12-02 (941-0009) High Performance chassis and XM2-02 (941-0003) portable chassis; REQUIRES one or more SFP+ transceiver options: 10GBASE-SR/SW (948-0013), or 10GBASE-LR/LW (948-0014); NOTE: If XM12-01 (941-0002) chassis is used

Model Number	Part Number	Description
		with this load module, the FRU-OPTIXIAXM12-01 (943-0005) power supply upgrade kit must be installed.
XDM10G8S	944-1098	Xdensity, XDM10G8S, 10-Gigabit Ethernet load module with 8-ports of SFP+ interfaces with L2-3 routing protocol emulation and data plane support; for XG12 (940-0005) Rackmount chassis, XM12-02 (941-0009) High Performance chassis and XM2-02 (941-0003) portable chassis; REQUIRES one or more SFP+ transceiver options: 10GBASE-SR/SW (948-0013), or 10GBASE-LR/LW (948-0014); ); NOTE: If XM12-01 (941-0002) chassis is used with this load module, the FRU-OPTIXIAXM12-01 (943-0005) power supply upgrade kit must be installed.

# **Specifications**

The load module specifications are contained in the following table.

Xdensity Load Module Specifications

Feature	Xdensity 32 port	Xdensity 8 port
Load Modules	XDM10G32S	XDM10G8S
Number of ports per mod- ule	32	8
Number of chassis slots per module	1	1
	XM12 High Performance (4000W): 384ports 10GESFP+	XM12 High Performance (4000W): 384ports 10GESFP+
Maximum ports per chassis	XM2 Desktop: 64-ports 10GESFP+	XM2 Desktop: 64-ports 10GESFP+
	XG12: 384 ports	XG12: 384 ports
SFP+ transceiver support	<ul><li>10GBASE-SR/SW (multim</li><li>10GBASE-LR/LW (single r</li><li>10GBASE-CR (passive, co</li></ul>	mode fiber)
Multi-core processor tech- nology	Yes	Yes
	Minimum Frame Size at Line Rate: 64	Minimum Frame Size at Line Rate: 64
Frame Size	Minimum Frame Size - may not be at Line Rate: 64	Minimum Frame Size - may not be at Line Rate: 64
	Maximum Frame Size: P0:	Maximum Frame Size: P0:

Feature	Xdensity 32 port	Xdensity 8 port
	9216B	9216B
	others 2500B	others 2500B
Interface protocols	IEEE8002.3ae10GE LAN	IEEE8002.3ae10GE LAN
Host protocol emu- lationsupport	ARP, NDP, IPv4, IPv6, IGMP, MLD and DHCPv4/v6 (Client+Server)	ARP, NDP, IPv4, IPv6, IGMP, MLD and DHCPv4/v6 (Client+Server)
Routing protocol emulation support	BFD, BGPv4/v6, CFM, EIGRP, ISISv4/v6, ISIS- DCE, LDP, Link OAM, OSPFv2, OSPFv3, PIM- SM/SSM-v4/v6, RIP, RIPng, STP/RSTP/MSTP, RSVP-TE	BFD, BGPv4/v6, CFM, EIGRP, ISISv4/v6, ISIS- DCE, LDP, Link OAM, OSPFv2, OSPFv3, PIM- SM/SSM-v4/v6, RIP, RIPng, STP/RSTP/MSTP, RSVP-TE
Performance benchmark tests	RFC 2544, RFC 2889, RFC 3819	RFC 2544, RFC 2889, RFC 3819
Number of transmit flows per port (sequential values)	Billions	Billions
Number of transmit flows per port (non-sequential values)	Millions	Millions
User-Defined Fields (UDF)	Counter, Value List, and Nested Counter UDFs	Counter, Value List, and Nested Counter UDFs
Transmit engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures
User defined field features	Fixed, increment or decrement by userdefined step, value list, and nested UDF	Fixed, increment or decrement by userdefined step, value list, and nested UDF
Data field pattern per stream	Random, increment (word/-byte), decrement (word/-byte)	Random, increment (word/-byte), decrement (word/-byte)
Frame length controls	Fixed, uniform random, auto, increment by user-defined step, dynamic frame rate change, and frame size change on the fly	Fixed, uniform random, auto, increment by user-defined step, dynamic frame rate change, and frame size change on the fly
Error generation	CRC good, bad	CRC good, bad

Feature	Xdensity 32 port	Xdensity 8 port
IPv4, UDP, TCP, ICMP, ICMPv6, IGMP checksum	Hardware checksum generation and verification	Hardware checksum generation and verification
Receive engine	Wire-speed packet filtering, data integrity, real-time latency, and sequence check- ing for each packet group	Wire-speed packet filtering, data integrity, real-time latency, and sequence checking for each packet group
Trackable receive flows	8K per port	8K per port
Filters	48-bit source/destination address, 2x128-bit user-definable pattern and offset, frame length range, CRC error, data integrity error, sequence checking error, IP/TCP/ UDP checksum error	48-bit source/destination address, 2x128-bit user-definable pattern and offset, frame length range, CRC error, data integrity error, sequence checking error, IP/TCP/UDP checksum error
Statistics and rates (counter size: 64 bits)	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 userdefined stats (UDS), data integrity frames, data integrity errors, sequence checking frames, and sequence checking errors	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 userdefined stats (UDS), data integrity frames, data integrity errors, sequence checking frames, and sequence checking errors
Intrinsic latency adjust- ment	Ability to remove inherent latency from any MSA-com- pliant 10GE SFP+ trans- ceivers without factory support	Ability to remove inherent latency from any MSA-com- pliant 10GE SFP+ trans- ceivers without factory support
Transmit line clock adjust- ment	Ability to adjust the parts per million (ppm) line frequency over a range of +/-100 ppm	Ability to adjust the parts per million (ppm) line frequency over a range of +/-100 ppm
Operating temperature range	41°F to 104°F (5°C to 40°C), ambient air temperature	41°F to 104°F (5°C to 40°C), ambient air temperature
Load module dimensions	15.95" (L) x 12.00" (W) x 1.28" (H) 405mm (L) x 305mm (W) x 33mm (H)	15.95" (L) x 12.00" (W) x 1.28" (H) 405mm (L) x 305mm (W) x 33mm (H)

Feature	Xdensity 32 port	Xdensity 8 port
Load module weights	Module only: 7.1 lbs. (3.2 kg)	Module only: 7.1 lbs. (3.2 kg)
Load module weights	Shipping weight: 9.4 lbs. (4.3 kg)	Shipping weight: 9.4 lbs. (4.3 kg)
Tranceiver Type	SFP+	SFP+
Direct Attach Copper	No	Yes
LED	No	No
ppm Adjust range	+/-100ppm	+/-100ppm
ppm Adjust port/card	Card	Card
Trigger out	No	No
External Clock In(Frequence)	No	No
External Clock Out	No	No
Ambient Operating Temperature Range (C)	5-40	5-40
Timestamp - Resolution	20ns	20ns
Timestamp - High Res- olution	No	No
Timestamp - End of Frame Instrumentation	No	No
Timestamp - Floating Intru- mentation	No	No
IEEE802.3x Flow control	No	No
WAN	No	No
Streams per port	16	16
Number of streams in Advanced Scheduler Mode (Data Center Mode)	16	16
Transicevier Intrinsic Latency Calibration	No	No
Intrinsic Latency	Yes	Yes
Data Integrity	Yes	Yes
Auto Instrumentation	Yes	Yes
Preamble - Changeable Con-	No	No

Feature	Xdensity 32 port	Xdensity 8 port
tent		
Preamble - Byte Count Mode	No	No
Preamble - SFD Detect Mode	Yes	Yes
Preamble - Cisco CDL Mode	No	No

## **Xdensity Four User Support**

As many as Four users can operate on a single Xdensity load module. A user can own from one to four port resource groups per load module. 32 ports of Xdensity is divided into four resource groups and each resource group consists of 8 ports defined as follows:

- Resource group 1: Ports 1-8 (Port 1 is resource group Master)
- Resource group 2: Ports 9-16 (Port 9 is resource group Master)
- Resource group 3: Ports 17-24 (Port 17 is resource group Master)
- Resource group 4: Ports 25-32 (Port 25 is resource group Master)

A user can own non-consecutive resource group (i.e. resource group 1 and resource group 4). Port Cluster specifications are as follows:

- A Port Cluster may be owned by exactly one user
- Taking ownership of any un-owned port within the port cluster will automatically force ownership of the entire Port Cluster. Ownership of some (but not all) ports within a Port Cluster is not a legal condition.
- Releasing ownership of any owned port within a Port Cluster will automatically force release of ownership of all ports within that Port Cluster.
- Reboot of CPU must take place through the Resource Group Master. If user wish to reboot for example port two entier resource group that is port one to port eight gets re-booted.
- User can only Telnet to a Resource Group Master
- Frequency adjustment (PPM Adjust) functionality is available across the entire Xdensity load module. If there is one owner across an entire Xdensity load module then the user will be allowed to change PPM value for the card. If more than one user owns Port Clusters across an Xdensity load module, then PPM cannot be changed by anyone.



## Chapter 41 - IXIA XMVAE Gigabit Ethernet Load Modules

This chapter provides details about Ixia's XMVAE-Gigabit Ethernet test modules the specifications and features.

Ixia's XMVAE Gigabit Ethernet test modules provide complete Layer 2-7 network and application testing functionality in a single test system for Automotive Ethernet switch and ECU testing. Ixia test system supports Automotive Ethernet specific interface for 10/100/1000 Mbps Ethernet speeds for testing Automotive Ethernet network components in next-generation vehicles and smart cars.

The XMVAE load modules include support for BroadR-Reach transceivers for testing BroadR-Reach enabled Automotive Ethernet switch and ECU functionality. Each test port on the module has the following:

- Auto-negotiable /100/1000 Mbps Ethernet over copper
- · Gigabit Fiber and 100Base-FX Ethernet over fiber
- · A powerful RISC processor running Linux
- · A full, test-optimized TCP/IP stack

The XMVAE architecture provides unprecedented performance and flexibility for testing the following:

- BroadR-Reach enabled Automotive switches
- ADAS/Infotainment ECUs
- Media and wireless access devices
- · Gateways and AUTOSAR IP/Ethernet applications for Automotive use

The XMVAE load module supports the following:

- Wire-speed Layer 2-3 traffic generation and analysis
- · High performance IPv4/IPv6 protocol emulations
- Ethernet ECU behavior emulation and true Layer 4-7 application traffic generation on each test port

Ixia's XMVAE Gigabit Ethernet modules comprise an 8 and a 16 port full-performance configuration, providing scalability and affordability for a diverse range of test requirements. With 12 slots per XGS12-SD high performance chassis, up to 96/192 Ethernet ECU ports can be simulated in a single test system to create high density automotive network test environments. In an XM2 chassis system, up to 32 ECU ports can be simulated for low scale requirements.

# **Key Features**

The key features of XMVAE load modules are as follows:

#### **Flexible Packet Generation**

• Each Ixia GE XMVAE test port is capable of generating precisely-controlled network traffic at up to wire speed using Ixia's IxExplorer test application.

- Millions of packet flows can be configured on each port with fully customizable packet header fields. Flexible header control is available for Ethernet, IPv4/v6, IPX, ARP, TCP, UDP, VLANs, QinQ, and many others protocols.
- Payload contents can also be customized with incrementing/decrementing, fixed, random, or user-defined information.
- Frame sizes can be fixed, varied according to a pattern, or randomly assigned across a weighted range.
- Rate control can be flexibly defined in frames per second, bits per second, percentage of line rate, or inter-packet gap time.

#### **Real-time Latency**

Packets representing different traffic profiles can be associated with packet group identifiers (PGIDs). The receiving port measures the minimum, maximum, and average latency in real time for each packet belonging to different groups. Measurable latencies include:

- Instantaneous latency and inter-arrival time where each packet is associated with one group ID
- Latency bins, where PGIDs can be associated with a latency range
- Latency over time, where multiple PGIDs can be placed in "time buckets" with fixed durations
- First and last time stamps, where each PGID can store the timestamps of first and last received packets

#### **Transmit Scheduler**

There are two modes of transmission available - Packet Stream and Advanced Stream Scheduler.

In **Packet Stream Scheduler** mode, the transmit engine allows configuration of up to 256 unique sequential stream groupings on each port. Multiple streams can be defined in sequence, each containing multiple packet flows defined by unique characteristics. After transmission of all packets in the first stream, control is passed to the next defined stream in the sequence. After reaching the last stream in the sequence, transmission may either cease, or control may be passed on to any other stream in the sequence. Therefore, multiple streams are cycled through, representing different traffic profiles to simulate real network traffic.

In **Advanced Stream Scheduler** mode, the transmission of stream groupings is interleaved per port. For example, assume a port is configured with three streams. If Stream 1 is defined with IP packets at 20% of line rate, Stream 2 is defined with TCP packets at 50% of line rate, and Stream 3 is defined with MPLS packets at 30% of line rate, data on the port will be transmitted at an aggregate utilization of 100% with interleaved IP, TCP, and MPLS packets.

#### **Extensive Statistics**

- Real-time 64-bit frame counts and rates
- Spreadsheet presentation format for convenient manipulation of statistics counters
- Eight quality of service counters (supporting 802.1p, DSCP, and IPv4 TOS measurements)

- Six user-defined statistics that use a trigger condition
- Extended statistics for ARP, ICMP, and DHCP
- Transmit stream statistics for frame counts and rate
- · External logging to file for statistics and alerts
- Audible and visual alerts with user-definable thresholds

#### **Data Capture**

Each port of the load module is equipped with 64 MB of capture memory, capable of storing tens of thousands of packets in real time. The capture buffer can be configured to store packets based on user-defined trigger and filter conditions. Decodes for VLAN, IPv4, IPv6, ARP, ICMP, DHCP, IGMP, UDP, TCP and various other protocols are provided.

#### **Data Integrity**

As packets traverse through networks, IP header contents may change resulting in the recalculation of packet CRC values. To validate device performance, the data integrity function of XMVAE Gigabit Ethernet modules allows packet payload contents to be verified with a unique CRC that is independent of the packet CRC. This ensures that the payload is not disturbed as the device changes header fields.

#### **Sequence and Duplicate Packet Checking**

Sequence numbers can be inserted at a user-defined offset in the payload of each transmitted packet. Upon receipt of the packets by the device under test (DUT), out-of-sequence errors or duplicated packets are reported in real time at wire-speed rates. The user can define a sequence error threshold to distinguish between small versus big errors, and the receive port can measure the amount of small, big, reversed, and total errors. Alternatively, the user can use the duplicate packet detection mode to observe that multiple packets with the same sequence number are received and analyzed.

#### **L2-3 Protocol Emulation**

Ixia's XMVAE Gigabit Ethernet modules support performance and functionality testing using routing/bridging protocol emulation via the IxNetwork and IxAutomate applications. Protocols supported include: VLAN, STP/RSTP, MSTP, PVST+/RPVST+, MSRP, link aggregation (LACP), ESMC, PTP, PPPoX, DHCPv4 client/server, DHCPv6 client/server, 802.1x, WebAuth.

IxNetwork offers the customization and flexibility to test hundreds of switches and ECUs. IxNetwork can customize millions of traffic flows to stress data plane performance. Powerful GUI wizards and grid controls allow users to create sophisticated traffic flows with ease. Its enhanced real-time analysis and statistics are capable of reporting comprehensive protocol status and detailed per-flow traffic performance metrics.

#### **AVB Testing**

Ixia's XMVAE Gigabit Ethernet modules support functional and performance testing of MSRP and gPTP protocols. You can send both 1722 encapsulated and VLAN encapsulated traffic at line rate for the AVB reserved streams. Clock hierarchy can be established using gPTP BMCA algorithm and synchronization of various clocks can be measured using the inbuilt Stratum-3 clock that has 20 ns of timestamp resolution. This load module's capability to measure the latency, latency variation, loss and sequence errors allows extensive performance evaluation of various algorithms such as strict priority queuing, Weighted Round-Robin, Weighted Fair Queuing and Credit Based Shaper implementations.

#### **ECU Testing**

Ixia's XMVAE Gigabit Ethernet load modules can connect to the BroadR-Reach interface in ECUs using PHY media converters. The load module can be used to load the Automotive Ethernet network with traffic and test ECU functionality. IxNetwork's powerful Traffic Template can be used to generate custom ECU protocols and load the desired traffic that can be sent at any rate up to the wire-speed. Various bench marking tests like RFC 2544 can be run to fully qualify the embedded switches in the ECUs.

#### **Application Layer Performance Testing**

Ixia's XMVAE Gigabit Ethernet modules support performance testing of content-aware devices and networks via the IxLoad application. IxLoad creates real-world traffic scenarios at the TCP/UDP (Layer 4) and application (Layer 7) layers, emulating clients and servers for web (HTTP, SSL), P2P, FTP, email (SMTP, POP3, IMAP), streaming (RTP, RTSP), video (MPEG2, MPEG4, IGMP and RSTP), voice (SIP, H.323, H.248, SCCP and MGCP), and infrastructure services such as DNS, DHCP, LDAP, AAA, and Telnet. Security platforms can be tested with integrated L2/L3 authentication mechanisms such as 802.1x and NAC, as well generated malicious traffic to test for security. Each 1GbE XMVAE port can be independently configured to run different protocols and client/server scenarios.

#### **Tcl API**

Ixia's XMVAE Gigabit Ethernet modules are supported by a comprehensive Tcl application programming interface (API). This API allows users to develop custom scripts and integrate the modules into automated test environments.

#### **Load Modules**

The XMVAE family consists of the following models:

- An 8-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps load module
- A 16-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps load module

Each of these load modules are described as follows:

#### LSM1000XMVAE8

LSM1000XMVAE8 Gigabit Ethernet is an 8-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps load module. It provides complete L2-7 support and is compatible with the XGS12-SD rack mount chassis (940-0011) and XM2 desktop chassis (941-0023).

It requires the following:

- Separate BroadR-Reach transceivers
- SFP transceivers- SFP-LX, SFP-SX, and SFP-CU, required by Fiber ports

The LSM1000XMVAE8 load module is shown in the following figure:

Figure: LSM1000XMVAE8



#### LSM1000XMVAE16

LSM1000XMVAE16 Gigabit Ethernet is a 16-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps load module. It provides complete L2-7 support and is compatible with the XGS12-SD rack mount chassis (940-0011) and XM2 desktop chassis (941-0023).

It requires the following:

- Separate BroadR-Reach transceivers
- SFP transceivers- SFP-LX, SFP-SX, and SFP-CU, required by Fiber ports

The LSM1000XMVAE16 load module is shown in the following figure:

Figure: LSM1000XMVAE16



#### **Part Numbers**

Part Numbers for XMVAE Load Module and Supported Adapters are provided in the following table.

Part Numbers for XMVAE Modules

Model Num- ber	Part Number	Description
LSM1000XMVAE8	944-1130	<ul> <li>8-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps</li> <li>Full featured L2-L7 with BroadR-Reach enabled (requires separate BroadR-Reach transceivers)</li> </ul>

Model Num- ber	Part Number	Description
		Fiber Ports require SFP transceivers, options include SFP-LX, SFP-SX, and SFP-CU
LSM1000XMVAE16 944-113		<ul> <li>16-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps</li> </ul>
	944-1131	<ul> <li>Fiber Ports require SFP transceivers, options include SFP-LX, SFP-SX, and SFP-CU</li> </ul>
		<ul> <li>Full featured L2-L7 with BroadR-Reach enabled (requires separate BroadR-Reach transceivers)</li> </ul>

# **Specifications**

The load module specifications are provided in the following table:

XMVAE Load Module Specifications

Feature	Details
Load module	LSM1000XMVAE8
Load Module	LSM1000XMVAE16
Connector type	SFP, can connect to BroadR-Reach transceivers or BroadR-Reach media converters, or 1GE copper or fiber transceivers.
Maximum ports per chassis	32 ports - XM2 Desktop
Maximum ports per chassis	192 ports in XGS12-SD Rack mount
Connection speed	Auto-negotiable 10/100/1000 Mbps Ethernet over copper and Gigabit Fiber and100Base-FX Ethernet over Fiber
Port CPU/memory per port	800MHz /1GB
Number of ports per model	16/8
Layer 2-3 switching/routing protocol testing	Yes
Layer 4-7 application traffic testing	Yes
AUTOSAR IP/Ethernet bus compatibility tests	Yes
AUTOSAR IP/Ethernet stack functionality tests	Yes
IEEE Audio/Video Bridging tests for AVB bridge and end points	Yes
802.1AS/gPTP timing and sync tests	Yes

Feature	Details
Capture buffer per port	64 MB
Number of transmit flows per port (sequential values)	Billions
Number of transmit flows per port (arbitrary values)	98 K
Number of track-able receive flows per port	512 K
Number of stream definitions per port	4096
Transmit engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures.
Receive engine	Wire-speed packet filtering, capturing, real- time latency for each packet group, data integ- rity, and sequence checking.
Statistics and rates (counter size: 64-Bit)	Link State, Line Speed, Frames Sent, Valid Frames Received, Bytes Sent/Received, Fragments, Undersize, Oversize, CRC Errors, VLAN Tagged Frames, 8 QoS counters, Data Integrity Frames, Data Integrity Errors, Sequence Checking Frames, Sequence Checking Frames, Sequence Checking Errors, ARP, and Ping requests and replies.
Error generation	CRC (Good/Bad/None), Undersize, Oversize.
Packet flow statistics	Real-time statistics to track up to 128K packet flows with throughput and latency measurements.
Latency measurements	20ns resolution
IPv4, IPv6, UDP, TCP	Hardware checksum generation
Frame length controls	Fixed, random, weighted random, or increment by user-defined step, random, weighted random.

# **Application Support**

The Ixia application support for XMVAE load modules is provided in the following table:

XMVAE Application Support

ATTIVE Application Support		
Application	Support	
IxExplorer	A full-featured layer 2-3 wire-speed Ethernet traffic generation and analysis test application with full support for stateless protocol functional and scalability testing. IxExplorer is included with the purchase of all	

Application	Support
	Ixia chassis.
IxNetwork	IxNetwork provides wire-rate traffic generation with service modeling that builds realistic, dynamically-controllable data-plane traffic. IxNetwork offers the industry's best test solution for functional and performance testing by using comprehensive emulation for switching, routing, ARP, ICMP, DHCP, IPv4, IPv6, multicast, timing and AVB protocols.
IxLoad	Provides a scalable solution for testing converged multiplay services and application delivery platforms. IxLoad emulates data, voice, and video subscribers and associated protocols for performance testing as well as the ability to generate malicious traffic to test for security.
IxANVL	Provides industry standard AUTOSAR IP/Ethernet bus compatibility, standards compliance, interoperability, ECU configuration and functionality tests for Automotive Ethernet switches and ECUs.

# **Mechanical Specifications**

#### **LED Panel**

Each LSM1000XMVAE8 and LSM1000XMVAE16 port incorporates a set of 2 LEDs, as described in the following table.

Port LEDs for LSM1000XMVAE8 and LSM1000XMVAE16

LED Label	Copper	Fiber
Link/Tx (Upper LED)	Color is used to indicate the link speed:  • 1000Mbps Green  • 100Mbps Orange  • 10Mbps Yellow  Flashing indicates transmit activity.  Off if link is down.	Green indicates link has been established and flashes during transmit activity.
Rx/Error (Lower LED)	<ul> <li>Three conditions apply:</li> <li>Full duplex or master (in 1000 Mbps case): Green with extended pulses off to indicate receive activity.</li> <li>Half duplex or subordinate (in 1000 Mbps case): Off with extended pulses to indicate receive activity.</li> <li>Error: Overrides the other two modes and pulses red.</li> </ul>	Green indicates link has been established and flashes during receive activity.  Continuous red indicates a receive error.

LED Label	Copper	Fiber
	No link: Off.	



# **Chapter 42 - IXIA Stream Extraction Modules**

The Stream Extraction module has three ports: two test ports and one monitor port. The monitor port has up to eight pattern matchers that you can configure. In addition, there are AND/OR operations to the pattern matching that do not exist in other module

Figure: AFM1000SP-01 Load Module



You can configure the pattern matching based on the MAC address, IP Address, or TCP/UDP address.

### **Part Numbers**

The part numbers are shown in the following table. Items without a *Price List Names* entry are no longer available.

Part Numbers for Gigabit Modules

Load Mod- ule	Price List Name	Description
AFM1000SP- 01	AFM1000SP- 01	3 port Stream Extraction module, port 1 RJ-45 copper, port 2/3 RJ-45 Dual PHY copper/fiber.

# **Specifications**

The load module specifications are contained in the following table.

AFM1000SP-01 Load Module Specifications

	AFM1000SP-01	
# ports	3 (to capture, one analyzer)	
Data Rate	10/100/1000 Mbps	
Campantan	RJ-45 (Copper) port 1	
Connector	RJ-45 Dual PHY (Copper and Fiber) port 2/3	

	AFM1000SP-01
Capture buffer size	N/A
Captured packet size	N/A
Streams per port	N/A
Advanced scheduler streams per port	N/A
Flows per port	N/A
Preamble size: min-max	N/A
Frame size: min-max	N/A
Inter-frame gap: min- max	N/A
Inter-burst gap: min- max	N/A
Inter-stream gap:min- max	N/A
Latency	N/A

### **Port LEDs**

Each port incorporates a set of LEDs, as described in the following table.

AFM1000SP-01 Load Module Port LEDs

LED Label	Usage
Link/Tx (Upper LED)	Color is used to indicate the link speed:  • 1000Mbps Green  • 100Mbps Orange  • 10Mbps Yellow  Flashing indicates transmit activity.
	Off if link is down.

### **Statistics**

Statistics counters for AFM1000SP-01 cards may be found in Statistics for  $\underline{10/100/1000}$  AFM.

# Chapter 43 - IXIA PerfectStormONE Appliances

This chapter provides details about PerfectStormONE 10GE and 40GE family of appliancesspecifications and features.

The PerfectStormONE appliance provides the platform to seamlessly unify the IxLoad and BreakingPoint software applications into a single and more powerful system, and at the same time provides a portable solution in a compact form factor appliance. Due to the compact form factor and reduced power requirements, you can use the appliance when you need high performance, but have space and power availability constraints in the lab. The single appliance allows control of up to 80Gbps of blended application traffic, 60 million concurrent connections, and new TCP connection rates of up to 2 million/sec. The hardware-based acceleration supports massive encryption levels with up to 40Gbps encrypted throughput per system.

PerfectStormONE's unique combination of portability, performance, and cost-effectiveness allows you to perform enterprise-scale performance and security testing anywhere, at any time, using the exact application, attack, and load behavior needed to optimize and harden your IT infrastructure.

The PerfectStormONE 10GE and 40GE appliances have two variants, fusion (supports IxLoad and BreakingPoint) and standard (supports IxLoad only).

PerfectStormONE supports the following:

- both IxLoad and BreakingPoint software applications; BPS runs on the fusion variants of the appliance
- native 40GE QSFP+ and 10GE SFP+ interfaces
- native 40GE QSFP+ interfaces with 4 x 10GE fan-out option
- compact form factor and reduced power requirements
- line-rate application performance per interface
- hardware-based acceleration for SSL and IPsec performance
- software licensing upgrades enable affordable 4Gbps performance now with easy expansion for future needs of up to 80Gbps

# **Key Features**

The key features of PerfectStormONE appliances are as follows:

#### **Unified Applications and Security Test Platform**

PerfectStormONE is a unified applications and security test platform, with support for BreakingPoint and IxLoad software.

#### Flexible Modes

- PerfectStormONE 10GE and 40GE variants can operate in both Aggregated and Non-Aggregated modes. For more information, see <u>PerfectStormONE 10GE</u> and <u>PerfectStormONE 40GE</u>.
- PerfectStormONE 10GE appliance can operate either in 1GE mode or 10GE mode using SFP+ interfaces.

 PerfectStormONE 40GE appliance can connect to 10GE devices using 40GE to 4x10GE fan-out cables. In fan-out mode, the appliance provides access to 8x10GE SFP+ interfaces.

#### **Blended Application Traffic**

PerfectStormONE Fusion can create blended application traffic and current security attacks with a very high count of concurrent wired and wireless users from a single chassis less than 2u.

#### **Massive Scale Real-World Traffic Conditions**

PerfectStormONE tests and validates IT systems under controlled real-world scenarios that model your own unique environments. It understands actual performance, system limitations, and real security posture in a better way, to right size data centers and eliminate incidents in production. It generates stateful applications and malicious traffic that simulate millions of real-world end-user environments to test and validate infrastructure, a single device, or an entire system. This includes complex data, video, voice, storage, and network application workloads.

#### **Real Attacks**

- 6,000+ live security attacks, 35,000+ pieces of live malware found in enterprise, core, and mobile networks, 180+ evasions
- DDoS and botnet simulation and custom attacks
- Research and frequent updatesHardware-based Acceleration

PerfectStormONE provides hardware-based acceleration for SSL and IPsec.

#### **Multi-user Environment**

PerfectStormONE's multi-user environment leverages the per port user ownership model for all ports on the test modules installed into the appliance.

#### **High-performing Business Applications**

PerfectStormONE ensures high-performing, and more available and secure business applications.

#### **Disaster Recovery**

PerfectStormONE validates disaster recovery and business continuity.

#### **Reduced Legal Exposure**

PerfectStormONE provides reduced legal exposure due to data loss by validating security using the industry's most up to date application and threat intelligence.

# PerfectStormONE Appliances

PerfectStormONE appliances can generate stateful applications and malicious traffic, simulating millions of real-world end-user environments to test and validate infrastructure, a single device, or an entire system.PerfectStormONE's unique combination of portability, performance, and cost-effectiveness allows you to perform enterprise-scale performance and security testing anywhere, at any time, using the exact application, attack, and load behavior needed to optimize and harden your IT infrastructure.

PerfectStormONE's unified architecture platform in the form of a compact form-factor appliance provides portability. It also provides the flexibility to license the port count and their operating speed. PerfectStormONE appliance comprises the variants provided in the following table.

PerfectStormONE 10GE and 40GE appliances:

	Standard	Fusion
	PerfectStormONE 1GE/10GE 8- port SFP+	PerfectStormONE Fusion 1GE/10GE 8-port (SFP+)
	PerfectStormONE 1GE/10 GE 4-port SFP+	PerfectStormONE Fusion, 1GE/10GE 4-port SFP+
10GE	PerfectStormONE 1GE/10GE 2- port SFP+	PerfectStormONE Fusion, 1GE/10GE 2-port SFP+
	PerfectStormONE , 1GE 8-port SFP+	PerfectStormONE Fusion, 1GE, 8-port SFP+
	PerfectStormONE , 1GE 4-port SFP+	PerfectStormONE Fusion, 1GE, 4-port SFP+
40GE	PerfectStormONE 40GE 2-port QSFP+	PerfectStormONE Fusion 40GE 2-port QSFP+

#### PerfectStormONE 10GE

The PerfectStormONE 10GE appliance consist of 8-port 1GE/10GE SFP+ interfaces, and is licensed as five variants, each one available in both standard (enables support for IxLoad) and Fusion (enables support for both IxLoad and BreakingPoint) as provided in the table above. You can upgrade your appliance from any of the variants to another using an activation code. These variants can operate in three different flexible modes as follows:

- Non-Aggregated Mode: In this mode,
  - Each 10GE port uses of 1/8th of the network processor and memory resources available on the appliance
  - Delivery of application traffic happens at wire-speeds for each port, with up to 80Gbps.
- 10GE Aggregated Mode: In this mode,
  - There is an extra flexibility of allocating all available NP resources and memory available on an appliance while using a single 10GE interface to transmit/receive the traffic.
  - Ixia test applications transparently configure the allocation of NP resources to achieve the maximum performance.
- 1GE or 10GE mode: In this mode,
  - The PerfectStorm ONE 10GE appliance can operate either in 1GE mode or 10GE mode, using SFP+ interfaces.

#### PerfectStormONE 40GE

The PerfectStormONE 40GE appliances consist of 2-port 40GE QSFP+ interfaces, and is available in two variants as provided in the  $\underline{\text{table}}$  above. Both the variants support the following:

- 8 x 10GE SFP+ via fan-out cable (MT-to-4x10GE LC fan-out, MMF, 3-meter or 5-meter cables)
- QSFP+ 40GE optical transceiver, MMF, 850nm (948-0031)

These variants can also operate in three different flexible modes as follows:

- Non-Aggregated Mode: In this mode,
  - Each 40GE port uses of ½ of the network processor and memory resources available on the load module
  - Delivery of application traffic happens at wire-speeds for each port, with up to 80 Gbps per module.
- 40GE Aggregated Mode: In this mode,
  - There is extra flexibility to allocate all network processor and memory resources available on a load module to a single 40GE port, doubling the performance the performance achieved per 40GE port.
  - Ixia test applications transparently configure the allocation of NP resources to achieve the maximum performance.
- 40GE QSFP+ to 4x10GE SFP+ Mode: In this mode,
  - There is an additional flexibility of connecting to 10GE devices using 40GE to 4 x 10GE fan-out cables.
  - In fan-out mode, the appliance provides access to 8 x 10GE SFP+ interfaces.

PerfectStormONE appliances are described as follows:

#### **PS10GE8**

PerfectStormONE PS10GE8 is a 8 port 10-Gigabit Ethernet, appliance with SFP+ interface.It supports only IxLoad software.

The PS10GE8 appliance is shown in the following figure:

Figure: PerfectStormONE appliance-PS10GE8



### **PS10GE8NG**

PerfectStormONE PS10GE8NG is a 8 port 10-Gigabit Ethernet, fusion appliance with SFP+ interface. It supports IxLoad and BreakingPoint software. The PS10GE8NG appliance is shown in the following figure:

Figure: PerfectStormONE appliance-PS10GE8NG



### PS40GE2

PerfectStormONE PS40GE2 is a 2 port 40-Gigabit Ethernet, appliance with QSFP+ interface.It supports only IxLoad software.

The PS40GE2 appliance is shown in the following figure:

Figure: PerfectStormONE appliance-PS40GE2



### PS40GE2NG

PerfectStormONE PS40GE2NG is a 2 port 40-Gigabit Ethernet, fusion appliance with QSFP+ interface. It supports IxLoad and BreakingPoint software.

The PS40GE2NG appliance is shown in the following figure:

Figure: PerfectStormONE appliance-PS40GE2NG



# **Part Numbers**

Part Numbers for PerfectStormONE appliances are provided in the following table.

Model Num- ber	Part Num- ber	Description
PSO10GE8	941-0037-01	<ul> <li>8-ports of 10GE with the SFP+ appliance.</li> <li>SSL and IPsec hardware acceleration.</li> <li>Supports IxLoad</li> </ul>
PSO10GE8NG	941-0027-01	<ul> <li>8-ports of 10GE with the SFP+ appliance.</li> <li>SSL and IPsec hardware acceleration.</li> <li>Supports IxLoad and BPS</li> </ul>
PSO10GE4	941-0038-01	<ul> <li>4-ports of 10GE with the SFP+ appliance.</li> <li>SSL and IPsec hardware acceleration.</li> <li>Supports IxLoad</li> </ul>
PSO10GE4NG	941-0031-01	<ul> <li>4-ports of 10GE with the SFP+ appliance.</li> <li>SSL and IPsec hardware acceleration.</li> <li>Supports IxLoad and BPS</li> </ul>
PSO10GE2	941-0039-01	<ul> <li>2-ports of 10GE with the SFP+ appliance.</li> <li>SSL and IPsec hardware acceleration.</li> <li>Supports IxLoad</li> </ul>
PSO10GE2NG	941-0032-01	<ul> <li>2-ports of 10GE with the SFP+ appliance.</li> <li>SSL and IPsec hardware acceleration.</li> <li>Supports IxLoad and BPS</li> </ul>
PSO1GE8	941-0044-01	<ul><li>8-ports of 1GE with the SFP+ appliance.</li><li>Supports IxLoad</li></ul>
PSO1GE8NG	941-0033-01	<ul><li>8-ports of 1GE with the SFP+ appliance.</li><li>Supports IxLoad and BPS</li></ul>
PSO1GE4	941-0045-01	<ul><li>4-ports of 1GE with the SFP+ appliance.</li><li>Supports IxLoad</li></ul>

Model Num- ber	Part Num- ber	Description
PSO1GE4NG	• 4-ports of 1GE with the SFP+ appliance. • Supports IxLoad and BPS	
PS40GE2	941-0036-01	<ul> <li>2-ports of 40GE with the QSFP+ appliance.</li> <li>SSL and IPsec hardware acceleration.</li> <li>Supports IxLoad</li> </ul>
PS40GE2NG	941-0028-01	<ul> <li>2-ports of 40GE with the QSFP+ appliance.</li> <li>SSL and IPsec hardware acceleration.</li> <li>Supports IxLoad and BPS</li> </ul>

# **Specifications**

The appliance specifications are contained in the following table.

PerfectStormONE Appliance Specifications

Feature	PerfectStormONE 10GE Standard/PerfectStormONE 10GE Fusion		PerfectStormONE 40GE Standard/PerfectStormONE 40GE Fusion	
Hardware, Ap	pliance Specification	ons		
Number of Ports	8		2	
Physical Interface	8-port, 10GE SFP+		2-port, 40GE QSFP+ (native) 8-port, 10GE SFP+ via fan-out cable	
1GE Support	Yes		No	
Transceiver Support (pluggable trans- ceivers)	<ul><li>10GBASE-SR/SW (850 nm)</li><li>10GBASE-LR/LW (1310 nm)</li></ul>		QSFP+, 40GBASE transcievers)	-SR4 (pluggable
Memory	64GB + 16GB on s	system controller	64GB + 16GB on system controller	
Operating System	Native Linux with Windows 7 Virtual Machine for IxOS		Native Linux with Machine for IxOS	Windows 7 Virtual
Hardware Encryption Offload	Yes	Yes	Yes	Yes
Hardware- Based Traffic Cap-	256MB per 10GE interface (available in BreakingPoint). This is applicable for Fusion variants only		• 1GB per 40GE • 256 MB per 1	

Feature	PerfectStormONE 10GE Standard/PerfectStormONE 10GE Fusion	PerfectStormONE 40GE Standard/PerfectStormONE 40GE Fusion	
ture		This is available in BreakingPoint and applicable for Fusion variants only	
FPGA Off- load	Yes	Yes	
IPv4, IPv6, UDP, TCP	Hardware checksum generation	Hardware checksum generation	
Appliance Dimensions	17.1 x 13.23 x 3.12 inches	17.1 x 13.23 x 3.12 inches	
Appliance Weight	21 lbs (9.52 Kg)	21 lbs (9.52 Kg)	
Tem- perature Range	<ul> <li>Operating: 41°F to 104°F (5°C to 40°C), ambient air</li> <li>Storage: 41°F to 122°F (5°C to 50°C), ambient air</li> </ul>	<ul> <li>Operating: 41°F to 104°F (5°C to 40°C), ambient air</li> <li>Storage: 41°F to 122°F (5°C to 50°C), ambient air</li> </ul>	
Humidity	<ul> <li>Operating: 0% to 85%, non-condensing</li> <li>Storage: 0% to 85%, non-condensing</li> </ul>	<ul> <li>Operating: 0% to 85%, non-condensing</li> <li>Storage: 0% to 85%, non-condensing</li> </ul>	
RU	Chassis <2U	Chassis <2U	
	With Rack Mount Shelf 2U	With Rack Mount Shelf 2U	
Power	600W, 90 to 264 VAC. The main 750W power supply output provides 12V@62.5A and has a standby voltage of 12V@3A. At a cold start the power supply inrush current is 38A; the carrier board and backplane 12V power rails support 70A.	600W, 90 to 264 VAC. The main 750W power supply output provides 12V@62.5A and has a standby voltage of 12V@3A. At a cold start the power supply inrush current is 38A; the carrier board and backplane 12V power rails support 70A.	
Shipping Vibration	1.5G rms	1.5G rms	
Integrated Sy	stem Controller		
CPU	Quad-Core, Intel Processor	Quad-Core, Intel Processor	
HDD	1 TB, Enterprise Class, High MTBF	1 TB, Enterprise Class, High MTBF	
Rack Mount (i	Rack Mount (included with Appliance)		
Rack Mount Dimensions	19.0 x 17.15 x 3.46 inches	2U rackmount, 19.0 x 17.15 x 3.46 inches	

Feature	PerfectStormONE 10GE Standard/PerfectStormONE 10GE Fusion	PerfectStormONE 40GE Standard/PerfectStormONE 40GE Fusion	
Rack Mount Weight	4.1 lbs	4.1 lbs	

NOTE

In the unlikely event that the unit stops working and does not automatically restore the previous session due to an ESD event, the unit must be manually restarted.

# **Application Support**

The Ixia application support for PerfectStormONE appliances is provided in the following table:

PerfectStormONE Application Support

Terresessiment Approaches Support		
Hardware	Application Support	
<ul> <li>PerfectStormONE         10GE Standard     </li> <li>PerfectStormONE         40GE Standard     </li> </ul>	IxOS, IxLoad, TCL API	
<ul> <li>PerfectStormONE         10GE Fusion     </li> <li>PerfectStormONE         40GE Fusion     </li> </ul>	IxOS, IxLoad, BreakingPoint, TCL API	

# **Transceiver and Cable Support**

The transceivers and cables supported by PerfectStormONE appliances are provided in the following table:

PerfectStormONE Transceiver and Cable Support

Applicances	Transceiver/Cable Part number	Description
PerfectStormONE 10GE     Standard     ONE 10GE	988-0011	SFP+, 10Gb/1Gb SR optical Xcvr, 850nm (cable included)
PerfectStormONE 10GE     Fusion	988-0012	SFP+, 10Gb/1Gb LR optical Xcvr, 1310nm
PerfectStormONE 40GE     Standard	948-0028	QSFP+ 40GBASE-SR4 optical transceivers (incompatible with fan-out)
PerfectStormONE 40GE     Fusion	948-0031	QSFP+ 40GBASE-SR4 optical transceivers (required for fan-out)

Applicances	Transceiver/Cable Part number	Description
	948-0041	MT 12-fiber MMF cable, 3- meter length
	948-0067	MT-to-4x10GE LC fan-out, MMF, 3-meter
	948-0068	MT-to-4x10GE LC fan-out, MMF, 5-meter

# **Mechanical Specifications**

### **Controls and Indicators**

The PerfectStormONE appliance controls and indicators are provided in the following table:

Controls and Indicators of PerfectStormONE appliances

Feature	Specification		
Ethernet	One RJ-45 10/100/1000-BaseT management port		
Serial	One RJ-45 RS232 serial port		
USB	2 USB dual type A, 4-pin jack connectors		

### **Front Panel**

The Front panel of the 8x10GE and 2x40GE PerfectStormONE appliances are shown in the following figures (applies to Fusion and non-Fusion versions):

Figure: Front panel of 8x10GE PerfectStormONE



Figure: Front panel of 2x40GE PerfectStormONE



The front panel switches and indicators are provided in the following table:

Front panel specifications of PerfectStormONE appliances

Feature	Specification	
	On/Off momentary power push button:	
Front Panel Switches	<ul> <li>Short press (0.5-2 seconds) - Graceful system shutdown</li> <li>allow up to 30 seconds before power-off.</li> </ul>	
	Long press (4 seconds) - Force Power Shutdown - immediate	
	Power LED	
Front Panel Indicators	<ul> <li>Green indicates that the system is ON and all power supplies are operational.</li> </ul>	
	<ul> <li>Off indicates that the system is OFF, or one or more power supplies are not operational.</li> </ul>	

#### **LED Panel**

The LED panel specifications are provided in the following table.

LED panel specifications of PerfectStormONE appliances

Feature	Specification		
Link	<ul><li> OFF indicates link is down</li><li> Solid Green indicates link is up</li></ul>		
Tx	<ul><li>Off indicates Tx is inactive</li><li>Blinking Green indicates Tx is active</li></ul>		
Rx/Err	<ul> <li>Off indicates Rx is inactive</li> <li>Blinking Red indicates Rx is active with errors</li> <li>Blinking Green indicates Rx is active</li> </ul>		

## **Cooling Fan Speed Control**

The PerfectStormONE appliance automatically monitors and measures the temperature of installed appliances. The appliance automatically adjusts the fan speed to maintain proper cooling.

## Power outage recovery and Automatic booting scenario

The BIOS on PerfectStormONE is set to Power On after a power failure.

The PerfectStormONE appliance will start up, boot Windows 7 and automatically login to the Ixia user account. Anything that is in the Startup folder will also launch.

### **Rack Mount Cautions**

CAUTION	If this unit is installed in a network equipment rack, please observe the fol-
	lowing precautions:

- a. Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the appliance (40° C).
- b. Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced. Do not block the sides of the appliance, and leave approximately 8 inches of space, on either sides of the unit for proper ventilation. The air flow clearance should be 8 inches on either sides.
- c. Mechanical Loading: Mount the appliance so that it is level in the rack and that a hazardous condition is not caused.
- d. Circuit Overloading: Consideration should be given to the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Appropriate consideration of equipment nameplate ratings should be used when addressing this concern.
- e. Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Appliance frame should be screwed down to racks to ensure proper grounding path. In addition, pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).
- f. Replacement of the power supply cord must of the same type cord and plug configuration that was shipped with the unit.

### Précautions relatives au montage en rack

ATTENTION

Si cette unité est installée dans une baie d'équipement réseau, observer les précautions suivantes:

- a. Température ambiante élevée: si installée dans un assemblage de baie fermé ou contenant plusieurs unités, la température ambiante de l'installation peut etre plus élevée que la température ambiante de la pièce. En conséquence, penser a installer l'équipement dans un environnement compatible avec la température ambiante maximale autorisée (40 C) spécifiée pour l'appareil.
- b. Circulation d'air réduite: installer l'équipement dans une baie de manière a ce que la circulation d'air requise pour faire fonctionner l'équipment en toute sécurité ne soit pas réduite. Ne pas bloquer les côtés de l'appareil, et laisser approximativement un espace de 12 pouces, de préférence 24 pouces, de chaque côté de l'unité pour une ventilation adéquate. L'espace laisse libre pour la circulation de l'air doit être de 12 pouces de chaque côté.
- c. Montage mécanique: monter l'appareil de manière a s'assurer qu'il soit droit dans la baie afin d'éviter de créer une condition dangereuse
- d. Un soin particulier doit etre apporté au branchement de l'équipement au circuit d'alimentation et aux conséquences qu'une charge excessive des circuits pourrait avoir sur le système de protection contre les surcharges et sur le cablâge d'alimentation. Prendre des précautions d'usage en prêtant attention aux normes figurant sur la plaque d'identification de l'équipement.
- e. Mise a la terre fiable: maintenir une mise a la terre fiable de l'équipement monté en baie. L'appareil doit etre vissé sur la baie afin d'assurer une mise a la terre correcte. De plus, faire particulièrement attention aux alimentations en courant autres que

- celles provenant de connections directes au circuit de dérivation (par exemple utilisation de prises multiples).
- f. Le remplacement du cordon d'alimentation doit comporter le même type de cordon et le même type de prise que ceux livrés avec l'unité.



For instructions on rack mounting and administration of the PerfectStormONE appliance, see the *PerfectStormONE Getting Started Guide*.



# **Chapter 44 - IXIA Novus ONE Appliances**

This chapter provides details about Novus ONE family of appliances-specifications and features.

The Novus ONE appliance provides the platform for complete layer 2 to 7 network and application testing in a compact form-factor.

Novus ONE's unique combination of portability, performance - up to 16 Dual-PHY ports per appliance, allows you to create cost-effective test environments for 10GE/1GE/100M Ethernet over copper and fiber media.

The Novus ONE appliances have two variants:

- 16-port, Dual-PHY (RJ45 and SFP+) 10GE/1GE/100M appliance
- 8-port, Dual-PHY (RJ45 and SFP+) 10GE/1GE/100M appliance

Novus ONE supports the following:

- dual-PHY SFP+/10GBASE-T RJ-45 interfaces
- 10Gbps, 1Gbps, and 100Mbps port speeds
- · compact form factor and reduced power requirements
- broad test functions across layer 2-7 with unified architecture that supports Ixia's IxNetwork, IxExplorer and IxLoad applications

### **Key Features**

- Full line-rate traffic generation to evaluate ASIC designs, FPGAs, and hardware switch fabrics.
- High scale and performance for emulating L2/3 protocols to validate performance and scalability of routing/switching and data center test cases using the Ixia's IxNetwork application.
- Support for testing SFP+ and 10GBase-T RJ-45 copper ports at different speeds simultaneously.
- Industry-standard RFC tests and protocol emulation on 10G, 1G, and/or 100M ports in a single test—to benchmark data-plane and performance and scale of network equipment.
- 10G, 1G, and 100M line-rate packet capture and decode tools to detect and debug data transmission errors.
- Application support for IxExplorer, IxNetwork, and IxLoad applications and related Tcl and automation APIs.
- Flexible 4:1 CPU and memory aggregation, for high-scale protocol emulation and performance.
- Real-time latency with latency resolution of up to 2.5 ns.
- Extensive port and traffic flow statistics.

## **Novus ONE Appliances**

Novus ONE appliances use Ixia's next-generation architecture designed to meet high-throughput testing needs. Due to its compact form-factor and reduced power

requirements, Novus ONE is a great option for providing high performance testingfor users constrained by the space and power availability in their lab.

Novus ONE's unified architecture platform in the form of a compact form-factor appliance provides portability.

Novus ONE appliance comprises the variants described as follows:

### **NOVUS10/1GE16DP**

Novus ONE 10/1GE16DP Appliance is a 16-port, SFP+/10GBASE-T Dual-PHY 10GE/1GE/100M Appliance with 1-slot Dual-PHY with 16-ports each of the SFP+ and 10GBASE-T RJ45 physical interfaces. It provides layer 2-7 support.

The NOVUS10/1GE16DP appliance is shown in the following figure:





### **NOVUS10/1GE8DP**

Novus ONE NOVUS10/1GE8DP is an 8-port SFP+/10GBASE-T Dual-PHY 10GE/1GE/100M Appliance with 1-slot Dual-PHY with 8-ports each of the SFP+ and 10GBASE-T RJ45 physical interfaces. It provides layer 2-7 support.

The NOVUS10/1GE8DP appliance is shown in the following figure:

Figure: Novus ONE appliance-NOVUS10/1GE8DP



### **Part Numbers**

Part Numbers for Novus ONE appliances are provided in the following table.

Model Number	Part Num- ber	Description
NOVUS10/1GE16DP	941-0060	<ul> <li>16-port SFP+/10GBASE-T Dual-PHY 10GE/1GE/100M appliance.</li> <li>1-slot Dual-PHY with 16-ports each of the SFP+ and 10GBASE-T RJ45 physical interfaces.</li> <li>Supports layer 2-7</li> </ul>
NOVUS10/1GE8DP	941-0061	<ul> <li>8-port SFP+/10GBASE-T Dual-PHY 10GE/1GE/100M appliance.</li> <li>1-slot Dual-PHY with 8-ports each of the SFP+ and 10GBASE-T RJ45 physical interfaces.</li> <li>Supports layer 2-7</li> </ul>

# **Specifications**

The appliance specifications are contained in the following table.

Novus ONE Appliance Specifications

Feature	NOVUS ONE 10/1GE16DP 10G/1G/100M	NOVUS ONE 10/1GE8DP 10G/1G/100M <sup>i</sup>	
Hardware,	Appliance Specifications		
Number of Ports	16 Tri-Speed	8 Tri-Speed	
Physical Inter- faces	Dual-PHY SFP+/10GBASE-T RJ-45	Dual-PHY SFP+/10GBASE-T RJ-45	
Support Port Speeds	10Gbps, 1Gbps, and 100Mbps		
Cable Media	<ul><li>Fiber</li><li>CAT5e</li><li>CAT6</li><li>CAT6A</li></ul>		
CPU and Memory	Multicore processor with 2GB of CPU memory per port pair		
Operating System	Native Linux		
Appliance Dimensions	<ul> <li>13.2" (W) x 3.0" (H) x 18" (D)</li> <li>335mm (W) x 76mm (H) x 457mm (D)</li> </ul>		
Appliance Weights	<ul><li>Appliance only: 27.4 lbs (12.41 kg)</li><li>Shipping: 34.5 lbs (15.65 kg)</li></ul>		

Feature	NOVUS ONE 10/1GE16DP NOVUS ONE 10/1GE8DP 10G/1G/100M 10G/1G/100Mi		
Temperature	<ul> <li>Operating: 41°F to 95°F (5°C to 35°C)</li> <li>Storage: 41°F to 122°F (5°C to 50°C)</li> </ul>		
Humidity	<ul><li>Operating: 0% to 85%, non-condensing</li><li>Storage: 0% to 85%, non-condensing</li></ul>		
Transmit F	eature Specifications		
Transmit Engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures		
Max. Streams per Port	512		
Max. Streams per Port in Data Center Ethernet	256		
Stream Con- trols	Rate and frame size change on the fly, sequential and advanced stream scheduler		
Minimum Frame Size	<ul> <li>10GbE:</li> <li>49 bytes at full line rate without UDF</li> <li>60 bytes at full line rate with UDF</li> <li>1GbE and 100MbE:</li> <li>49 bytes at full line rate</li> </ul>		
Maximum Frame Size	16,384 bytes		
Maximum Fame Size in Data Center Ethernet	9,216 bytes		
Priority Flow Control	<ul> <li>8 line-rate-capable queues, each supporting up to 2,500-byte frame lengths</li> <li>1 queue supporting up to 9,216-byte frame lengths</li> </ul>		
Frame Length Controls	Fixed, increment by user-defined step, weighted pairs, uniform, repeatable random, IMIX, and Quad Gaussian		
User-Defined Fields (UDF)	Fixed, increment or decrement by user-defined step, sequence, value list, and random configurations; up to five, 32-bit-wide UDFs are available		
Value Lists (Max.)	2M across 5 UDF		

Feature	NOVUS ONE 10/1GE16DP NOVUS ONE 10/1GE8DP 10G/1G/100M 10G/1G/100Mi	
Sequence (Max.)	512	
Error Gen- eration	Generate good CRC or force bad CRC, undersize and oversize standard Ethernet frame lengths, and bad checksum	
Hardware Checksum Generation	Checksum generation and verification for IPv4, IP over IP, ICMP/GRE/TCP/UDP, L2TP, GTP	
Link Fault Sig- naling	10GE: Reports, no fault, remote fault, and local fault port statistics; ability to select the option to have the transmit port ignore link faults from a remote link partner	
Latency Meas- urement Res- olution	2.5 nanoseconds	
Transmit Line Clock Adjust- ment	Ability to adjust the parts-per-million line frequency over a range of - 100 ppm to +100 ppm across all ports on the appliance	
Receive Fe	eature Specifications	
Receive Engine	Wire-speed packet filtering, capturing, real-time latency, and inter- arrival time for each packet group, with data integrity, sequence and advanced sequence checking capability	
Trackable Receive Flows per Port	<ul> <li>1M without Tx/Rx Sync and sequence checking</li> <li>512k with Tx/Rx Sync and sequence checking</li> </ul>	
Minimum Frame Size	<ul> <li>64 bytes at full line rate into the capture buffer</li> <li>49 bytes at less than full line rate</li> </ul>	
Filters (User- Defined Stat- istics, UDS)	2 SA/DA pattern matchers, 2x16-byte user-definable patterns with off- sets capability for start of: frame, IP, or protocol; up to 6 UDS counters are available	
Hardware Cap- ture Buffer	512 MB per port	
Statistics and Rates	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 user-defined stats, capture trigger (UDS 3), capture filter (UDS 4), 8 QoS counters, data integrity frames, data integrity errors, sequence and advanced sequence checking frames, sequence checking errors, ARP, and PING requests and replies	
Latency/Jitter Measurements	Cut-through, store & forward, forwarding delay, up to 16 time bins latency/jitter, MEF jitter, and inter-arrival time	

Feature	NOVUS ONE 10/1GE16DP NOVUS ONE 10/1GE8DP 10G/1G/100M 10G/1G/100Mi	
Layer 2-3	Protocol Support	
Routing and Switching	BGP4/BGP4+, OSPFv2/v3, ISISv4/v6, EIGRP/EIGRPv6, RIP/RIPng, BFD, IGMP/MLD, PIM-SM/SSM, STP/RSTP/MSTP, PVST+/RPVST+, Link Aggregation (LACP), LISP	
Software Defined Net- work	OpenFlow, Segment Routing, BGP Link State (BGP-LS), PCEP, VXLAN, EVPN VXLAN, OVSDB, GENEVE	
MPLS	RSVP-TE P2P/P2MP, LDP/LDPv6/mLDP, LDP L2VPN (PWE/VPLS), BGP VPLS, L3VPN/6VPE, 6PE, BGP RFC3107, MPLS-TP, MPLS OAM, EVPN/PBB-EVPN, Multicast VPN Rosen Draft, NG Multicast VPN	
Broadband and Authentic- ation	PPPoX/L2TPv2, DHCPv4/DHCPv6, ANCP, IPv6 Autoconfiguration (SLAAC), IGMP/MLD, IPTV, 802.1x, WebAuth, EAPoUDP, Cisco NAC	
Industrial Eth- ernet	Link OAM (IEEE 802.3ah), CFM/Y.1731, PBB/PBB-TE, ELMI, TWAMP, Sync-E ESMC, IEEE 1588v2 (PTP), gPTP (IEEE 802.1AS), MSRP (IEEE 802.1 Qat), IEEE 1722	
Data Center Ethernet	DCBX/LLDP, FCoE/FIP, PFC (IEEE 802.1Qbb), TRILL, Cisco FabricPath, SPBM, VEPA	
Layer 4-7	Application Traffic Testing Support	
Data	HTTP, HTTPS, TCP Session, FTP, DNS, Mail (SMTP, POP3, and IMAP),TFTP, AppReplay, AppLibrary	
Video	RTSP, IPTV, VoD, Adobe Flash Client, Apple HLS Client, Microsoft Silverlight Client, Adobe HDS Client, DASH Client; includes Video Quality VQMON and TCP Video Quality	
Voice	Advanced VoIP SIP & RTP, Audio & Video Codecs, VoLTE, MSRP, Telepresence, SMS, T.38; includes: Voice Quality and Video Quality for conversational video traffic	
Storage	iSCSI, CIFSv1, CIFSv2 (SMB2), SMB3, NFSv3 Client, NFSv4 Client, NFS4.1 Client, Cloud Storage Client	
Access	IPv4, IPv6, VLAN, Emulated Routers, DNS, DHCP	
In the unlikely event that the unit stops working and does not automatically restore the previous session due to an ESD event, the unit must be manually restarted.		

# **Application Support**

The Ixia application support for Novus ONE appliances is provided in the following table:

Novus ONE Application Support

Hardware	Application Support	
NOVUS10/1GE16DP	IxExplorer, IxLoad, IxNetwork, TCL API	
NOVUS10/1GE8DP	IxExplorer, IxLoad, IxNetwork, TCL API	

# **Transceiver and Cable Support**

The transceivers and cables supported by Novus ONE appliances are provided in the following table:

Novus ONE Transceiver and Cable Support

Applicances	Transceiver/Cable Part number	Description
• NOVUS10/1GE16DP • NOVUS10/1GE8DP	988-0011	SFP+10GBASE-SR/SW and 1000BASE-SX Dual-Rate pluggable optical transceiver for 10/1 Gigabit Ethernet LAN/WAN load modules with pluggable SFP+ interface, 850nm. Multi-mode fiber LC-LC, 3 meter cable included.
	988-0012	SFP+10GBASE-LR/LW and 1000BASE-LX Dual-Rate pluggable optical transceiver for 10/1 Gigabit Ethernet LAN/WAN load modules with pluggable SFP+ interface, 1310nm, 10km reach. Single-mode fiber LC-LC, 10 ft. cable included.
	948-0013	SFP+10GBASE-SR/SW, Access- ory, SFP+ Transceiver for 10 Gigabit Ethernet LAN/WAN load modules with pluggable SFP+ interface, 850nm
	948-0014	SFP+10GBASE-LR/LW, Access- ory, SFP+ Transceiver for 10 Gigabit Ethernet LAN/WAN load modules with pluggable SFP+ interface, 1310nm
	948-0015	SFP+10GBASE-LRM, Accessory, SFP+ Transceiver for 10 Gigabit Ethernet LAN/WAN load mod- ules with pluggable SFP+ inter- face, for multimode fiber, 1310nm

Applicances	Transceiver/Cable Part number	Description
	948-0016	SFP+10GSFP+Cu, Accessory, passive, copper Direct Attach Cable Assembly for 10 Gigabit Ethernet LAN/WAN load modules with pluggable SFP+ interface, 3 meter length
	SFP-LX	SFP 1 Gigabit Ethernet Trans- ceiver - 1310nm LX
	SFP-SX	SFP 1 Gigabit Transceiver - 850nm SX
	SFP-FX-100M-XCVR	SFP 100BASE-FX 100M plug- gable optical transceiver, MMF (multimode), 1310nm, 2km reach

# **Mechanical Specifications**

### **Front Panel**

The Front panel of the Novus ONE appliance is shown in the following figure:





The front panel switches and indicators are provided in the following table:

Front panel specifications of Novus ONE appliance

Feature	Specification
Front Panel Switches	On/Off momentary power push button:
	<ul> <li>Short press (0.5-2 seconds) - Graceful system shutdown</li> <li>allow up to 30 seconds before power-off.</li> </ul>
	Long press (4 seconds) - Force Power Shutdown - immediate
	Power LED
Front Panel Indicators	<ul> <li>Green indicates that the system is ON and all power supplies are operational.</li> <li>Off indicates that the system is OFF, or one or more</li> </ul>

Feature	Specification
	power supplies are not operational.

#### **LED Panel**

The LED panel specifications are provided in the following table.

LED panel specifications of Novus ONE appliance

Feature	Specification
Link	<ul><li>OFF indicates link is down</li><li>Solid Green indicates link is up</li></ul>
Tx	<ul><li>Off indicates Tx is inactive</li><li>Blinking Green indicates Tx is active</li></ul>
Rx/Err	<ul> <li>Off indicates Rx is inactive</li> <li>Blinking Red indicates Rx is active with errors</li> <li>Blinking Green indicates Rx is active</li> </ul>

### **Cooling Fan Speed Control**

The Novus ONE appliance automatically monitors and measures the temperature of installed appliances. The appliance automatically adjusts the fan speed to maintain proper cooling.

### **Rack Mount Cautions**

CAUTION	If this unit is installed in a network equipment rack, please observe the fol-
	lowing precautions:

- a. Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the appliance (35° C).
- b. Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced. Do not block the sides of the appliance, and leave approximately 8 inches of space, on either sides of the unit for proper ventilation. The air flow clearance should be 8 inches on either sides.
- c. Mechanical Loading: Mount the appliance so that it is level in the rack and that a hazardous condition is not caused.
- d. Circuit Overloading: Consideration should be given to the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Appropriate consideration of equipment nameplate ratings should be used when addressing this concern.
- e. Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Appliance frame should be screwed down to racks to ensure proper grounding path. In addition, pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).

f. Replacement of the power supply cord must of the same type cord and plug configuration that was shipped with the unit.

### Précautions relatives au montage en rack

Si cette unité est installée dans une baie d'équipement réseau, observer les précautions suivantes:

- a. Température ambiante élevée: si installée dans un assemblage de baie fermé ou contenant plusieurs unités, la température ambiante de l'installation peut etre plus élevée que la température ambiante de la pièce. En conséquence, penser a installer l'équipement dans un environnement compatible avec la température ambiante maximale autorisée (35 C) spécifiée pour l'appareil.
- b. Circulation d'air réduite: installer l'équipement dans une baie de manière a ce que la circulation d'air requise pour faire fonctionner l'équipment en toute sécurité ne soit pas réduite. Ne pas bloquer les côtés de l'appareil, et laisser approximativement un espace de 12 pouces, de préférence 24 pouces, de chaque côté de l'unité pour une ventilation adéquate. L'espace laisse libre pour la circulation de l'air doit être de 12 pouces de chaque côté.
- c. Montage mécanique: monter l'appareil de manière a s'assurer qu'il soit droit dans la baie afin d'éviter de créer une condition dangereuse
- d. Un soin particulier doit etre apporté au branchement de l'équipement au circuit d'alimentation et aux conséquences qu'une charge excessive des circuits pourrait avoir sur le système de protection contre les surcharges et sur le cablâge d'alimentation. Prendre des précautions d'usage en prêtant attention aux normes figurant sur la plaque d'identification de l'équipement.
- e. Mise a la terre fiable: maintenir une mise a la terre fiable de l'équipement monté en baie. L'appareil doit etre vissé sur la baie afin d'assurer une mise a la terre correcte. De plus, faire particulièrement attention aux alimentations en courant autres que celles provenant de connections directes au circuit de dérivation (par exemple utilisation de prises multiples).
- f. Le remplacement du cordon d'alimentation doit comporter le même type de cordon et le même type de prise que ceux livrés avec l'unité.

For instructions on rack mounting and administration of the Novus ONE appliance, see the *Novus ONE Native IxOS Getting Started Guide*.

# Chapter 45 - XAir™ XM Module

Ixia's new XAir™ is the next generation hardware for LTE UE emulation. It delivers the unparalleled LTE performance in the smallest footprint providing the industry highest UE density. This module will allow LTE Advanced feature support. The XM/XG platform can easily expand to support additional sectors.

With the XAir module, complex subscriber modeling can be achieved with the following parameters:

- 1000 UEs per sector
- · Voice (VoLTE), Video and Data Traffic Support
- · QoE analysis and scoring of each traffic stream
- · Mobility over multiple sectors
- Channel Modeling per UE



Each XAir board supports one sector, with 1 Gbps Ethernet ports connected to the IxLoad Xcellon NP or IxCatapult m500/p250 chassis. It also supports up to 4 CPRI interfaces to an eNB or to Ixia's Remote Radio Head r10 units that cover all FDD & TDD frequency bands.

## **Key Features**

- Highest density LTE UE emulation starting at 1000 connected active UEs per board
- Board has its own high accuracy 10MHz clock for eNB synchronization
- Based on Ixia's NP technology for line-rate traffic through a large number of connections
- Fully compatible with the Ixia XM/XG chassis and load modules for seamless testing with other Ixia hardware and test applications.

# **Specifications**

XAir Module Specifications

Hardware Specification	
Number of Ports	3x 1 Gbps Ethernet ports, 1x 10 Gbps Ethernet port, 4x Optical SFP+ CPRI ports, 1x Serial port, SMA Clock In/Out and Analog Out
Physical	
Form Factor	1U Module for insertion into Ixia XM/XG chassis

Height	12.00" (304.8mm)
Width	1.28" (32.5mm)
Depth	15.95" (405.1mm)
Gross Weight	7.5 lbs (3.4kg)
Power Consumption	184 Watts

# Chapter 46 - XAir2™ LTE Module

The XAir2 LTE load module supports LTE UE Simulation at the 3GPP LTE UU interface. The XAir2 module provides a rich array testing capabilities for all layers of 3GPP LTE User Equipment including the PHY, MAC, RLC, PDCP, RRC and NAS protocols. In conjunction with the Ixia PerfectStorm 10G Load Module and IxLoad, the XAir2 provides a complete evolved Node-B (eNB) test environment in a single powerful, intuitive, easy to use system. Application layer traffic such as VoLTE voice, HTTP, FTP and streaming video can be generated on 1 or 1000s of simulated UEs. These simulated UEs can support the latest LTE Advanced PRO functionality for increased throughput such as multiple carrier aggregation (FDD and TDD).

XAir2 provides all of the key features and capabilities provided by the previous generation XAir XM module. In addition, the XAir2 module provides support for an increased number of carriers, increased throughput and the latest of LTE-Advanced and LTE-Advanced PRO PHY and MAC functionality.

### **Key Features**

The XAir2 LTE load module features will continue to be significantly enhanced with a steady stream of frequent and new software releases. New features and enhancements to existing features as defined in the 3GPP Release 10, Release 11, Release 12 and Release 13 3GPP specifications. Not all of the features listed below will be available in the initial release. For a detailed description of available features, please consult Ixia representative.

- 4 Primary Carriers
- FDD and TDD duplex, selectable on each carrier
- LTE-Advanced Carrier Aggregation (2CA through 5CA)
- 4 CPRI Ports supporting CPRI line rates 3,5 and 7 (2457.6 to 9830.4 Mbit/s)
- SISO, 2x2 and 4x4 MIMO antenna configurations
- Transmission Modes ranging from TM1 to TM9
- Up to 256QAM Downlink and 64QAM Uplink
- Built-in high accuracy Stratum 1 10MHz clock
- LTE Advanced PRO Licensed Assisted Access (LAA)
- 1000s of simulated UEs
- Mobility validation with Handover and ReEstablishment scenarios
- Standard and Custom Channel Modeling features
- Support for simulated UE Categories 1-7 and 9-12
- Application support for IxLoad Voice, Video and Data protocols including VoLTE, HTTP, FTP
- Tcl and automation APIs
- Supports the Ixia Wideband Radio with support for all bands in the range of 400 MHz to 6 GHz

### **Part Numbers**

Part Numbers for XAir2 LTE Load Module and Supported Adapters are provided in the following table.

Part Numbers for XAir2 LTE Module

Model Number	Part Number	Description
XAir2		<ul><li> 3GPP LTE UE Simulation Module</li><li> 1-slot</li></ul>
960-0518	960-0518	<ul><li>CPRI and 10GE interfaces</li><li>IxLoad Application Test Support</li></ul>

# **Specifications**

The load module specifications are contained in the following table.

XAir2 LTE Load Module Specifications

Feature	TE Load Module Specifications  NOVUS-R100GE8Q28+FAN
Hardware Load Module Specifications	
Chassis Slots Used	1 slot
Physical Interfaces per module	16
Number of CPRI Ports	4
Number of 10G Ethernet Ports	1
CPU and Memory	Multicore processor with 32GB Memory
Load Module Dimensions	17.3" (L) x 1.3" (W) x 12.0" (H)
Load Module Diffielisions	440mm (L) x 33mm (W) x 305mm (H)
Load Module Weights	Module only: 12.9 lbs (5.85 kg)
Load Module Weights	Shipping: 19.7 lbs (8.94 kg)
Tomporatura	Operating: 41°F to 104°F (5°C to 40°C)
Temperature	Storage: 41°F to 122°F (5°C to 50°C)
Humidity	Operating: 0% to 85%, non-condensing
	Storage: 0% to 85%, non-condensing
Chassis Capacity: Maximum Number of XAir2 Cards per Chassis Model	
XGS12-SD Chassis (940- 0011)	12 load modules, 48 carriers

Feature	NOVUS-R100GE8Q28+FAN	
XGS12-HS Chassis (940- 0006)	12 load modules, 48 carriers	
XGS2-SD Chassis (940- 0010)	2 load modules, 8 carriers	
XGS2-HS Chassis (940- 0012)	2 load modules, 8 carriers	
LTE PHY Features		
Number of carriers	4 carriers per XAir2 module	
Bandwidths	5,10,15,20 MHz	
CPRI line rate options	3,5 and 7 (2457.6, 4915.2, 9830.4 Mbit/s)	
Bands	Supports all 3GPP defined LTE bands in the 400MHz to 6000 MHz range	
Duplex	FDD, TDD	
Physical Antenna Configurations	1x1, 2x2	
Transmission Modes	TM1, TM2, TM3, TM4	
Carrier Aggregation	2CA and 3CA Downlink in all R12 supported combinations of FDD and TDD	
Channel Modeling	Custom channel modeling and pre-defined DL channel models based on 3GPP TS 36.101 (AWGN, EPA5Hz, EVA5Hz, EVA70Hz, ETU70Hz, ETU300Hz, HST)	
Layer 4-7 Application Traffic Testing Support		
Data	UDP, HTTP, HTTPS, TCP Session, FTP	
Video	RTSP, IPTV, VoD	
Voice	Advanced VoIP SIP & RTP, Audio & Video Codecs, VoLTE, MSRP, SMS, includes: Voice Quality and Video Quality for conversational video traffic	
Access	IPv4, IPv6	

# **Application Support**

The Ixia application support for the XAir2 load module is provided in the following table:

XAir2 LTE Load Module Application Support

Application	Support
Tcl API	Allows custom user script development for layer 2-7 testing.

Application	Support
IxLoad	Provides a scalable L4-7 solution for simulating a broad variety of traffic mixes commonly found on LTE User Equipment devices including Voice, Video and Data.

## **Additional Specifications**

#### **Front Panel**

The front panel of the XAir2 LTE load module is shown in the following figure. There are a total of 16 SFP+ transceiver ports on the XAir2 front panel with 8 labeled CPRI 1-8 and 8 more labeled Port 1-8. Not all ports are currently used on the XAir2 LTE product with the remaining unused ports available for possible future expansion features. The ports currently supported are:

CPRI 1, CPRI 2, CPRI 5, CPRI 6 and Port 4

Figure: Front panel of XAir2 Load Module



#### **LED Panel**

The XAir2 LTE card has 16 multi-color LEDs visible on the front panel. Each LED is located directly below or directly above a SFP+ transceiver port. These LEDs provide you with a visible status related to the operation of each of the XAir2 ports. Not all SFP+ ports are currently used on the XAir2 module as described above. Therefore, the LEDs associated with ports that are not used will always be off. A description of the LEDs for the ports that are active on the XAir2 module are described in the table below.

LED panel Specifications for XAir2 LTE Load Module

SFP+ Port Label	Active Port Num- bers	Description	
		LED Color	Meaning
CPRI	1, 2, 5, 6	Off	No test actively running
		Red	Test running, no CPRI sync
		Blue	Test running, CPRI Hyper- frame sync but no LTE radio frame alignment
		Yellow	Test running, CPRI Hyper- frame sync and Radio Frame alignment suc- cessful, but no BCH sync
		Green	Test running and BCH is being decoded
PORT	4	Off	No Link or no test actively running
		Yellow	Test running, No Link Status on 10GE
		Green	Test running, 10GE Link Status

NOTE

If more than one carrier is configured to utilize the same CPRI port, it is possible that one carrier is indicating Yellow (Radio Frame Alignment) and the second carrier is indicating Green (BCH decoded). In this case, the LED color will be Yellow, indicating that at least one of the carriers is not successfully decoding BCH. An example of this scenarios is where the radio is being used to support 2 independent 2x2 MIMO carriers (primary carriers or a primary and secondary carrier). The radio has a single CPRI connection supporting both carriers in this configuration. This would be different than the radio supporting a single 4x4 carrier.

### **Transceivers and Cables**

The XAir2 LTE load module supports optical transceivers and fiber cables for each of the physical interfaces that are enabled for the product. The following SFP+ transceivers are supported and qualified on the specified SFP+ port.

Transceivers and Cables for XAir2 LTE Load Module

SFP+ Port	Active Port Num-	Ixia Part Num-	Description
Label	bers	ber	
CPRI	1, 2, 5, 6	988-0012	Optical Singlemode, LC-LC 1310nm transceiver with

SFP+ Port Label	Active Port Num- bers	Ixia Part Num- ber	Description
			pluggable SFP+ interface and 3m LC-LC singlemode optical cable. This provides the direct CPRI connection to the Ixia 6 GHz Wideband Radio.
			This SFP+ transceiver is also compatible with all 10/1 Gigabit Ethernet Novus, PerfectStorm, and Firestorm load modules and appliances.
PORT	4	988-0011	Optical Multimode, LC-LC 850nm transceiver with pluggable SFP+ interface and 3m LC-LC multimode optical cable. This SFP+ and cable provides the con- nectivity between the Per- fectStorm L4-7 IxLoad application module and the XAir2 LTE module through the 10 Gigabit Ethernet Switch provided with the Ixia LTE Access XGS Con- nection Kit.  NOTE  This SFP+ trans- ceiver is also compatible with all 10/1 Gigabit Ethernet Novus, PerfectStorm, and Firestorm load modules and appliances.
		955-8123	Optical Multimode, LC-LC 850nm transceiver with pluggable SFP+ interface and 3m LC-LC multimode optical cable. This SFP+ and cable provides the connectivity between the Per-

SFP+ Port	Active Port Num-	Ixia Part Num-	Description
Label	bers	ber	
			fectStorm L4-7 IxLoad application module and the XAir2 LTE module through the 10 Gigabit Ethernet Switch provided with the Ixia LTE Access XGS Connection Kit.

# **Additional Hardware Required with XAir2 LTE**

### **General Information**

The complete XAir2 LTE Access UE Simulation solution requires several other hardware and software components. The additional hardware items are listed in the table below.

Additional Hardware Required with the XAir2 LTE Module

Category	Options	Ixia Part Number
	XGS12-SD, 12-slot chassis bundle with Standard Processor Module	940-0011
	XGS2-SD, 2-slot chassis bundle with Standard Processor Module	940-0010
Chassis	XGS12-HS, 12-slot chassis bundle with High Performance Processor Module	940-0006
	XGS2-HS, 2-slot chassis bundle with High Performance Pro- cessor Module	940-0012
Connection Kit	LTE Access XGS Connection Kit. One connection kit is required for every chassis with an XAir2 module present	949-1035
Radio	LTE Access 6GHz Wideband Radio	949-1034
Radio Connection	LTE Access Radio Connection Enclosure (RCE) Standard 700 MHz-2700MHz	949-1026
Enclosure	LTE Access Radio Connection Enclosure (RCE) High Band 1000MHz-3900MHz	949-1029

### **Radio**

The XAir2 Module is connected to the Device Under Test (DUT), typically an evolved-NodeB (eNB) through a Radio Frequency (RF) connection provided by the Ixia 6GHz Wideband Radio. The specifications for this radio are provided in the table below.

Figure: Ixia 6GHz Wideband Radio



LTE Access 6GHz Wideband Radio

Feature	cess 6GHz Wideband Radio  XAir2 Specification
Physical Dimensions	
General	19" Rack Mount
Height	1U
Depth	<500mm
Weight	<12kg
Mounting	Tool-less Rack Mount Kit (included)
Environmental	
Operating Temperature	+5C to +50C
Humidity	0% to 85%, non-condensing
Power	
Mains Power	100 – 240 VAC, 50-60 Hz
Front Panel Interfaces	
Receiver inputs	4 SMA connectors, female
Transmitter outputs	4 SMA connectors, female
Status LED	16 multi colour LEDs
Rear Panel Interfaces	
Mains input	IEC-C14
CPRI	Duplex LC
Ethernet	The Ethernet Port is designed for compatibility with an Ethernet cable meeting the requirements for Category 5e or Category 6, however the Ethernet port is not used in the Ixia IxLoad LTE Access solu-

Feature	XAir2 Specification
	tion and no Ethernet cable is required.
RF Specifications	
Frequency Range	400MHx - 5925MHz
Bandwidths Supported	5MHz, 10MHz, 15MHz, 20MHz
Display status indication	
Sys Clk	<ul><li> Green Flashing = Not locked</li><li> Green=Locked</li></ul>
SFP1 status	Off=SFP not present
(Only SFP 1 on Radio 0 is externally accessible)	<ul><li> Orange = Initializing</li><li> Green = Link active</li></ul>
AxC TX (TX baseband configuration status)	<ul><li>Orange = Awaiting config</li><li>Green = Configured for data</li></ul>
AxC RX (RX baseband configuration status)	<ul><li>Orange = Awaiting config</li><li>Green = Configured for data</li></ul>
RF TX ports	Green = Active
RF RX ports	Green = Active
STS (CPRI link embedded Ethernet status)	<ul> <li>CPRI link embedded Ethernet status:</li> <li>Orange = Initialising</li> <li>Flashing Green = Network discovery</li> <li>Green = configured to network</li> </ul>



## **Appendix A: XAUI Connector Specifications**

# **Description**

The following cable and accessories for the 10GE XAUI cards are described in this appendix. These include the following:

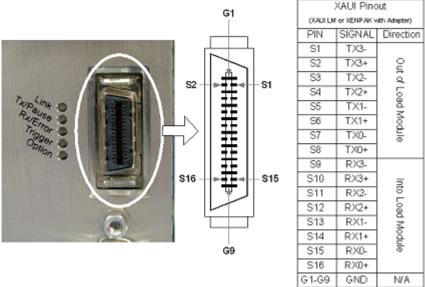
- <u>Standard Connector Specifications</u>: The signals carried on the Load Module's XAUI connector.
- <u>Front Panel Loopback Connector</u>: A connector used to loopback XAUI signals at the external connector.
- <u>Standard Cable Specification</u>: The CAB10GE500S1 (20") and CAB10GE500S2 (40") cables.
- SMA Break-Out Box: The BOB10GE500 SMA break-out box.
- XAUI Fujitsu to XENPAK Adapter: An adapter used with Ixia XENPAK load modules to create a XAUI interface.
- XAUI Tyco Interoperability Backplane HM-Zd Adapter: An adapter used to connect to the Tyco Interoperability Backplane.

## **Standard Connector Specifications**

The Ixia XAUI Load Module's front panel connector is the Fujitsu MicroGiGa. This connector can be mounted on the Device Under Test (DUT), eliminating the need for SMA cables. This part is also available directly from Fujitsu as part number FCN-268D008-G/1D-/2D.

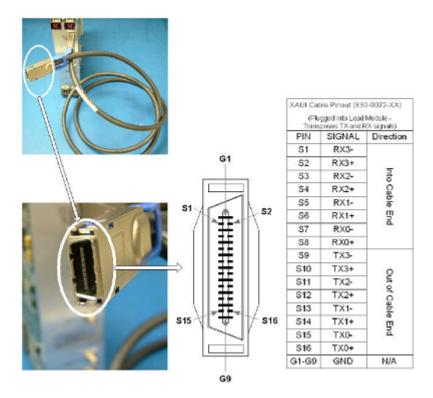
The connector as mounted on the Ixia load module is shown in the figure below, along with the signal names, functional description, and connector pin assignments. The same pinouts apply to XENPAK load modules which use the XENPAK to XAUI adapter.

Figure: Fujitsu MicroGiGa Connector Mounted on Load Module



The XAUI Cable plugs into the load module and transposes the transmit and receive signals, as shown in the following figure.

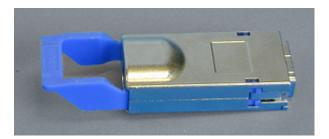
Figure: XAUI Cable Pinouts



## **Front Panel Loopback Connector**

In order to verify that the Ixia XAUI Load Module is operational, a loopback connector may be used to test external loopback on the front panel. You can remove the connector by pulling back on the blue handle, releasing the connection to the Fujitsu MicroGiGa connector. The loopback connector (Ixia P/N LPG10GE500) is shown in the following figure.

XAUI Front Panel Loopback Connector



# **Standard Cable Specification**

The same connector and pin assignments used on the Load Module can also be used on the Device Under Test (DUT). Ixia supplies a 20-inch cross-pinned cable assembly (CAB10GE500S1) that allows a straight connection as shown in the <a href="figure">figure</a>. This cable can also be used for loopback testing on an Ixia chassis equipped with two or more XAUI ports. Longer cable assemblies can be made on request, but we do not recommend that the cable length exceed 2 meters, because losses and skew may become unacceptable. Ixia makes a 40" cable available as part number CAB10GE500S2. The 40" cable is shown in the following figure.

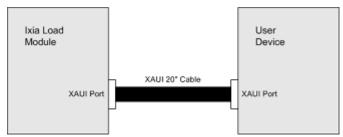
Figure: Ixia XAUI Cable (CAB10GE500S2)



NOTE

The 50cm maximum length suggested in the XAUI section of 802.3ae is a rough guideline for keeping the losses on PCB traces under 7.5 dB. Well designed cables usually have much lower losses per meter than PCB traces, so cables can be much longer than 50cm.

Figure: Direct XAUI Interface Using Ixia Supplied Cable



## **SMA Break-Out Box**

If the DUT uses coaxial connectors for the XAUI interface, a special break-out box (BOB10GE500) is required in addition to the XAUI cable, as shown in the following figure.. You must provide the sixteen 50 ohm coaxial cables with a male SMA connector on the end that mates to the BOB. The actual break-out box is shown in the following figure.

Figure: XAUI SMA Break-Out Box

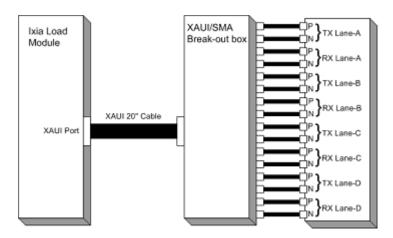


Figure: XAUI SMA Break-Out Box



When using coaxial cables for the XAUI interface, extreme care should be taken to match the electrical lengths of the two cables in each pair. The pairs can be of different lengths, since the XAUI SerDes should automatically correct for skew between lanes. Skew between the `P' and `N' lines within a pair, however, can introduce bit errors. The XAUI edge-rates can be as short as 60ps. Therefore, the total in-pair skew should be kept below 30 ps to avoid bit-errors. Some of this in-pair skew must be budgeted to the Load Module, Ixia XAUI cable, BOB, and the DUT. Allocating 10ps of in-pair skew to the coax cables would require length matching them to within about 0.08" (for RG-174). The propagation velocity of coax can vary slightly between manufacturers, lots, and as it is bent or stretched. Therefore, we recommend that coax cables be kept as short as possible.

XAUI Electrical Interface Performance

Parai	neter	Characteristic
	Impedance	100 ohm balanced differential, AC coupled.
	Amplitude	1.2Vpp minimum (with 0 pre-emphasis)
TxOutputs	Pre- emphasis	Software selectable (0, 18%, 38% or 75%)
Jitter	0.35 UI max. (UI is Unit Interval = 320ps nominal).	

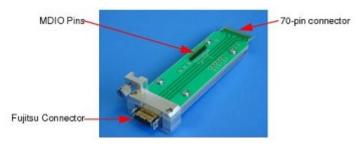
Parai	neter	Characteristic
	Impedance	100 ohm differential, AC coupled.
RxInputs	Amplitude	0.2 to 2.3 Vpp.
,	Jitter tol- erance	0.55 UI.

# **XAUI Fujitsu to XENPAK Adapter**

The electrical interface to XENPAK is XAUI, which uses an industry standard 70-pin connector. Ixia's XAUI Load Module, however, uses a Fujitsu MicroGiGa connector to both transmit and receive four XAUI lanes through eight twisted pairs through a 20" cable. Ixia offers an adapter (part number FXN10GE500) that routes the XAUI lanes from the Fujitsu connector to the pins on the XENPAK connector.

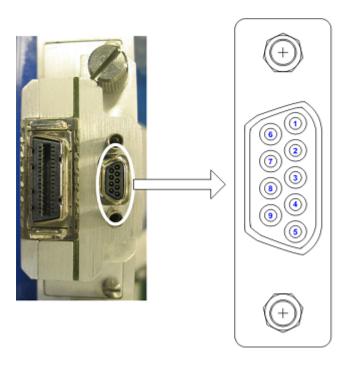
The adapter is shown in the following figure.

Figure: Fujitsu to XENPAK Adapter



This enables a XENPAK Load Module to act as a XAUI Load Module. However, the XENPAK Load Module can only run in Ethernet mode and transmit and verify Layer 2 or 3 traffic. Furthermore, there is an FD D-sub connector for MDIO on the front panel of the XENPAK Load Module (shown in the following figure). Both the MDIO and power are available through pins on the adapter and serve the same function as the D-sub connector on the XAUI Load Module.

Figure: CX4 and XAUI MDIO Pinouts



Front Panel MDIO Pinout		
PIN	SIGNAL	Direction
1	5V	OUT
2	3.3V	OUT
3	APS	OUT
4	LASI	OUT
5	RESET	OUT
6	TX_ON	OUT
7	MDIO	OUT
8	MDC	OUT
9	GND	OUT

# **XAUI Tyco Interoperability Backplane HM-Zd Adapter**

XAUI interoperability testing has been conducted using a Tyco built simulated backplane. Each XAUI vendor has been required to build a line card to connect to the backplane through the Tyco HM-Zd connector. Tyco had also built an SMA adapter to connect to the backplane, but it is too time-consuming and difficult to connect through SMAs. Ixia has built an HM-Zd adapter (P/N FTY10GE500), which allows direct connection to the backplane through the Fujitsu connector, saving significant setup time. This is shown in the following figure.

Figure: Tyco Interoperability Backplane HM-Zd Adapter



# **Appendix B: Available Statistics**

This appendix covers the available statistics for the following different card types:

- Statistics for 10/100 TXS Modules. These cards include the following:
  - 10/100 TX8 (LM100TX8)
  - 10/100 TXS8 (LM100TXS8)
- Statistics for 10/100/1000 TXS, 10/100/1000 XMS(R)12, 1000 SFPS4, and 1000STXS24 Cards. These cards include the following:
  - 10/100/1000 STXS2, STXS4, STXS24 (LM1000STXS2/4)
  - 10/100/1000 XMS12, XMSR12 (LSM1000XMSR12)
- Statistics for 10/100/1000 LSM XMV(R)4/8/12/16, and 10/100/1000 ASM XMV12X Cards. These cards include the following:
  - 10/100/1000 XMV4/8/12/16, XMVR4/8/12/16 (LSM1000XMV4/8/12/16, LSM1000XMVR4/8/12/16)
  - 10/100/1000 ASM XMV12X
- Statistics for OC12c/OC3c Modules. These cards include the following:
  - OC12c/OC3c (LMOC12c, LMOC3c)
- Statistics for OC48c Modules with BERT, Statistics for OC48c Modules with SRP and DCC, and Statistics for OC48c Modules with RPR and DCC. These cards include the following:
  - OC48c POS (LMOC48cPOS, LMOC48cPOS-M)
  - OC48 POS VAR (LMOC48VAR)
  - OC48c BERT (LMOC48cBERT)
  - OC48c BERT Rx
  - OC48c POS/BERT (LMOC49POS/BERT)
- Statistics for 2.5G MSM POS modules. These cards include the following:
  - 2.5 Gigabit MSM POS OC-48c modules (MSM2.5G1-01)
- Statistics for OC192c Modules with BERT, Statistics for OC192c Modules with SRP and DCC, and Statistics for OC192c Modules with RPR and DCC. These cards include the following:
  - OC192c with optional BERT and 10 Gigabit Ethernet. (LMOC192cPOS+BERT, LMOC192cPOS+BERT+WAN)
  - OC192c VSR. Note that all VSR cards have available all of the VSR statistics listed in the VSR section of Table B-6 on page B-25. (LMOC192cVSR-POS, LMOC192cVSR-BERT, LMOC192cVSR-POS+BERT)
- Statistics for 10GE Modules with BERT. These cards include the following:
  - 10 Gigabit Ethernet with optional BERT. (LM10GELAN, LM10GELAN-M, LM10GEWAN, LM10GEXAUI+BERT, LM10GEXAUI BERT only, LM10GEXENPAK+BERT, LM10GEXENPAK BERT only)
- Statistics for 10G UNIPHY Modules with BERT. These cards include the following:
  - 10 Gigabit UNIPHY with optional LAN/WAN, POS and BERT. (LM10G)
- Statistics for 10GE LSM Modules (except NGY). These cards include the following:

- 10 Gigabit LSM modules using XFP, XENPAK, or X2 carrier cards. (LSM10G1-01)
- 10 Gigabit LSM modules supporting MACSec. (LSM10GMS-01). See also <u>MACSec</u> statistics.
- 10 Gigabit LSM XM3 (LSM10GXM3)
- NGY LSM10GXM(R)8(XP)(S)-01, LSM10GXM(R)4(XP)(S)-01,LSM10GXM2XP-01, LSM10GXMR2(S)-01, LSM10GXM2S-01, including 10GBASE-T versions LSM10GXM(R)2/4/8GBT-01
- Statistics for NGY Modules. These cards include the following:
  - NGY LSM10GXM(R)8(XP)(S)-01, LSM10GXM(R)4(XP)(S)-01,LSM10GXM2XP-01, LSM10GXMR2(S)-01, LSM10GXM2S-01, including 10GBASE-T versions LSM10GXM(R)2/4/8GBT-01
- Statistics for 10G MSM modules. These cards include the following:
  - 10 Gigabit Ethernet MSM modules. (MSM10G1)
- Statistics for ATM Modules. These include the following:
  - ATM 622 Multi-Rate (LM622MR, LM622MR-512)
- Statistics for PoE Modules. These include the following:
  - Power over Ethernet (PLM1000T4-PD, LSM1000POE4-02)
- Statistics for 10/100/1000 AFM. These include the following:
  - 10/100/1000 AFM Stream Extraction Module. (AFM1000SP-01)
- <u>Statistics for IxNetwork</u>. These statistics are common to all cards that support IxNetwork.
- ALM, ELM and CPM Statistics. These include the following:
  - ALM1000T8 and ELM1000ST2 load modules
- 40/100 GE Statistics. These include the following:
  - 40GE LSM XMV1 and 100GE LSM XMV1 load modules
  - Lava 40/100GE load modules

## **Table Organization**

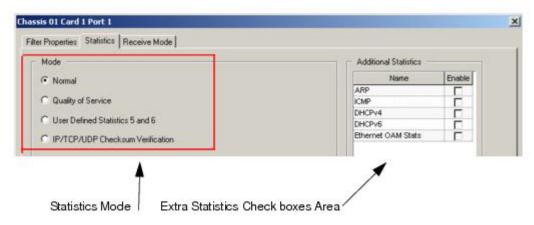
Each of the following tables details the statistics available for that set of cards. Available statistics are controlled by three sets of controls.

### **IxExplorer**

#### **Statistics Modes**

From the IxExplorer pane, select a port and select **Filter, Statistics, Receive Mode** from the right-hand pane. Select the tab at the top labelled **Statistics**. This is shown here for a Gigabit module with the statistics modes highlighted. The choices here are mutually exclusive. In most cases, when one is selected new statistics are available at the expense of others.

**Figure: Statistics Mode Selection** 



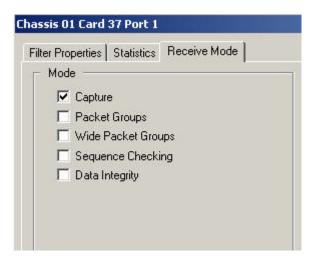
#### **Extra Statistics Check Boxes**

Additional statistics are selected through a set of check boxes located on the same **Statistics** tab, in the **Additional Statistics** section. These statistics are always in addition to those in the **Statistics Mode** section.

#### **Receive Mode**

From the IxExplorer pane, select a port and select **Filter**, **Statistics**, **Receive Mode** from the right-hand pane. Select the tab at the top labelled **Receive Mode**. This is shown here for a 10GE LAN module. The check boxes generally result in additional statistics.

Figure: Receive Mode Selection



# **Key to Tables**

The following table lists the headings that appear in the tables in this appendix and their correspondence to IxExplorer dialogs and selections.

Key for Statistics Table

Heading Item	IxExplorer Dialog	IxExplorer Label
Statistics Mode		
UDS 5&6	Statistics	User Defined Statistics 5 and 6
QoS	Statistics	Quality of Service
Normal	Statistics	Normal
Checksum Errors	Statistics	IP/TCP/UDP Checksum Verification
Data Integrity	Statistics	Data Integrity
Extra Statistics Check boxes		
IxRouter	Statistics	IxRouter Stats
ARP STATS	Statistics	ARP Stats
ICMP STATS	Statistics	ICMP Stats
BGP STATS	Statistics	BGP Stats
OSPF STATS	Statistics	OSPF Stats
ISIS STATS	Statistics	ISIS Stats
RSVP-TE STATS	Statistics	RSVP-TE Stats
LDP STATS	Statistics	LDP Stats
POS Ext	Statistics	POS Extended Stats

Heading Item	IxExplorer Dialog	IxExplorer Label
DHCPv4	Statistics	DHCPv4 Stats
DHCPv6	Statistics	DHCPv6 Stats
Temp Sensors	Statistics	Temperature Sensor Stats
OAM Stats	Statistics	Ethernet OAM Stats
PTP Stats	Statistics	Ptp Stats
Receive Mode		
Rx Capture	Receive Mode	Capture
Rx Seq Checking	Receive Mode	Sequence Checking
Rx Data Integrity	Receive Mode	Data Integrity
Rx Packet Group	Receive Mode	Packet Group
Rx Mode Bert	Receive Mode	Mode Bert
Rx Mode ISL	Receive Mode	Mode ISL
Rx Bert Channelized	Receive Mode	Bert Channelized
Rx Mode Echo	Receive Mode	Mode Echo
Rx Mode DCC	Receive Mode	Mode DCC
Rx Wide Packet Group	Receive Mode	Wide Packet Groups
Rx Mode PRBS	Receive Mode	PRBS
Rx Rate Monitoring	Receive Mode	Rate Monitoring
Rx Per Flow Error Stats	Receive Mode	Per PGID Checksum Error Stats

# **TCL Development**

### **Statistics Mode**

The statistics mode is controlled by the use of the Tcl stat mode command. The following table lists the available choices and their correspondence to IxExplorer choice.

Tcl Stat Mode Options

Option	IxExplorer Choice
statNormal (0) (default)	Normal
statQos (1)	Quality of Service
statStreamTrigger (2)	User Defined Statistics 5 and 6
statModeChecksumErrors (3)	IP/TC@/UDP Checksum Verification

Option	IxExplorer Choice
statModeDataIntegrity (4)	Data Integrity

### **Access to Statistics**

Most statistics are accessed through the use of stat command. VSR statistics are access through the use of the vsrStat command.

### **Receive Mode**

The receive mode is controlled through the use of the port receiveMode option. The choices available are or'd together and list the bits available to control the receive mode.

Tcl Port Receive Options

Option	IxExplorer Choice
portCapture (1)	Capture
portPacketGroup (2)	Packet Groups
portRxTcpSessions (4)	Does not affect statistics.
portRxTcpRoundTrip (8)	Does not affect statistics.
portRxDataIntegrity (16)	Data Integrity
portRxFirstTimeStamp (32)	Does not affect statistics.
portRxSequenceChecking (64)	Sequence Checking
portRxModeBert (128)	BERT Mode
portRxModeBertChannelized (128)	Channelized BERT Mode
portRxModeIsl	ISL Mode
portRxModeEcho	Echo Mode
portRxModeDcc	DCC Mode
portRxModeWidePacketGroup	Wide Packet Groups
portRxModePrbs	PRBS Mode
portRxModeRateMonitoring	Rate Monitoring
portRxModePerFlowErrorStats	Per PGID Checksum Error Stats

## C++ Development

### **Statistics Mode**

The statistics mode is controlled by the use of the stat.mode member. "Key for Statistics Table" on page 690 lists the available choices and their correspondence to IxExplorer choices and the labels used in the tables in this appendix.

C++ Stat Members

Member Value	IxExplorer Choice
statNormal (0) (default)	Normal
statQos (1)	Quality of Service
statStreamTrigger (2)	User Defined Statistics 5 and 6
statModeChecksumErrors (3)	IP/TCP/UDP Checksum Verification
statModeDataIntegrity (4)	Data Integrity

### **Access to Statistics**

Most statistics are accessed through the use of <code>TCLStatistics</code> class. VSR statistics are accessed through the use of the <code>TCLvsrStat</code> class.

#### **Receive Mode**

The receive mode is controlled through the use of the port.receiveMode member. The choices available are or'd together and list the bits available to control the receive mode.

Tcl Port Receive Options

Member Value	IxExplorer Choice
portCapture (1)	Capture
portPacketGroup (2)	Packet Groups
portRxTcpSessions (4)	Does not affect statistics
portRxTcpRoundTrip (8)	Does not affect statistics
portRxDataIntegrity (16)	Data Integrity
portRxFirstTimeStamp (32)	Does not affect statistics
portRxSequenceChecking (64)	Sequence Checking
portRxModeBert (128)	BERT Mode
portRxModeBertChannelized (128)	Channelized BERT Mode

Member Value	IxExplorer Choice
portRxModeIsl	ISL Mode
portRxModeEcho	Echo Mode
portRxModeDcc	DCC Mode
portRxModeWidePacketGroup	Wide Packet Groups
portRxModePrbs	PRBS Mode
portRxModeRateMonitoring	Rate Monitoring
portRxModePerFlowErrorStats	Per PGID Checksum Error Stats

# **Description of Statistics**

The table below lists all of the available statistics, along with an explanation of those statistics. The following three columns are used:

- Counter: the name of the statistics as it appears in IxExplorer. These are organized by general category, as used in the remaining tables in this appendix.
- Interpretation: the description of the statistics.
- Internal Baseame: the internal basename used to describe the statistics in the TCL and C++ API. The base name is used to form other names:
  - TCL stat command options: the basename is the name of the option.
  - TCL stat command get sub-command counterType argument: the counterType name needed to fetch a particular statistic is formed by prepending the letters stat to the basename, while capitalizing the first letter of the statistic. For example, for basename alignmentErrors, the counterType name is statAlignmentErrors.
  - C++ *statistic* class members: the *basename* is the name of the member.
  - C++ statistic command get method counterType argument: the counterType name needed to fetch a particular statistic is formed by prepending the letters stat to the basename, while capitalizing the first letter of the statistic. For example, for basename alignmentErrors, the counterType name is statAlignmentError

#### Statistics Counters

Counter	Inter- pretation	Internal Basename
Optixia X16 Chassis		
Opix Power Supply 1 Status	The status of the #1 (left most) power supply.	Not available.
Opix Power Supply 2 Status	The status of the #2 power supply.	Not available.

Counter	Inter- pretation	Internal Basename
Opix Power Supply 3 Status	The status of the #3 power supply.	Not available.
Opix Power Supply 4 Status	The status of the #4 power supply.	Not available.
Opix Power Supply 1 Cur- rent	The current of the #1 power supply. This should be within 3 amps of other installed power supplies.	Not available.
Opix Power Supply 2 Cur- rent	The current of the #2 power supply. This should be within 3 amps of other installed power supplies.	Not available.
Opix Power Supply 3 Cur- rent	The current of the #3 power supply. This should be within 3 amps of other installed power supplies.	Not available.
Opix Power Supply 4 Cur- rent	The current of the #4 power supply. This should be within 3 amps of other installed power supplies.	Not available.
Opix Fan Bank 1 Status	The status of the #1 bank of fans, located in the fan tray.	Not available.
Opix Fan Bank 2 Status	The status of the #2 bank of fans, located in the fan tray.	Not available.
Opix Fan Bank 3 Status	The status of the #3 bank of fans, located in the fan	Not available.

Counter	Inter- pretation	Internal Basename
	tray.	
Opix Fan Bank 4 Status	The status of the #4 bank of fans, located in the fan tray.	Not available.
Optixia X16 Load Modules	A variable number of the statistics in this category are available for OLM load modules.	
5V Power Status	Indicates that the 5VDC bus A rail is on and valid.	Not available.
3.3V Power Status	Indicates that the 3.3VDC bus A rail is on and valid.	Not available.
3.3V/5V Power Status	Indicates that either the bus A 5VDC or 3.3VDC rail had an overcurrent event and shut down.	Not available.
LM Other Power Output	Indicates that power is good for the miscellaneous power supplies.	Not available.
LM 48V Power Output	Indicates that the -48VDC input is on.	Not available.
LM Tem- perature 1 Status	LM 83 pro- grammable inter- rupt - over temperature alarm.	Not available.
LM Tem- perature 2 Status	LM 83 critical temperature alarm.	Not available.
LM Bus B 5V Power Status	Indicates that the 5VDC bus B rail is on and valid.	Not available.

Counter	Inter- pretation	Internal Basename
LM Bus B 3.3V Power Status	Indicates that the 3.3VDC bus B rail is on and valid.	Not available.
LM Bus B 3.3V/5V Power Status	Indicates that either the bus B 5VDC or 3.3VDC rail had an overcurrent event and shut down.	Not available.
LM Tem- perature Cen- tral FPGA	Nominal board temperature in area 3.	Not available.
LM Tem- perature LM83	Nominal board temperature in area 1.	Not available.
LM Tem- perature LM87	Nominal board temperature in area 2.	Not available.
LM -48VDC Status	Indicates that the -48VDC input is in the valid input range.	Not available.
LM System V1	Dependent on each Optixia Load Module. Monitors one of several sys- tem buses.	Not available.
LM SMBUS 3.3V	Measures the SM bus. This value should be 3.3VDC =/- 10%.	Not available.
LM System V2	Dependent on each Optixia Load Module. Monitors one of several sys- tem buses.	Not available.
LM System V3	Dependent on each Optixia Load Module. Monitors one of several system buses.	Not available.

Counter	Inter- pretation	Internal Basename
LM System V4	Dependent on each Optixia Load Module. Monitors one of several sys- tem buses.	Not available.
LM System V5	Dependent on each Optixia Load Module. Monitors one of several sys- tem buses.	Not available.
LM System V6	Dependent on each Optixia Load Module. Monitors one of several system buses.	Not available.
LM System V7	Dependent on each Optixia Load Module. Monitors one of several sys- tem buses.	Not available.
User Con- figurable		
User Defined Stats 1 and 2 & Rate	Counters that increment each time the statistics conditions are met. The user-defined statistics conditions are set up in the Capture Filter window.	userDefinedStat1userDefinedStat2
Capture Trig- ger (UDS3) & Rate	A counter that increments each time the capture trigger conditions are met, as defined in the Capture Filter window.	captureTrigger
Capture Filter (UDS4) & Rate	A counter that increments each time the capture filter conditions	captureFilter

Counter	Inter- pretation	Internal Basename
	are met, as defined in the Capture Filter window.	
User Defined Stats 5 and 6 & Rate	Counters that increment each time the statistics conditions are met. The user-defined statistics conditions are set up in the Capture Filter window. (N/A to OC192 modules.)	streamTrigger1streamTrigger2
States		
Link State	`Up' when a link is established with another device, `Loopback' when the port has loopback enabled, `Down' when there is no connection to another device. (See note 2 in Notes.)	link
Line Speed	`10,' `100,' or `1000' (denoting Mbps) and OC-12, OC-3 or OC-48 for POS modules. (See note 6 in Notes)	lineSpeed
Duplex Mode	`Half' or `Full.' Half duplex only applies to 10/100 Load Modules. (See note 7 in Notes.)	duplexMode
Transmit State	Not shown in IxEx- plorer. The cur- rent transmit state of the port.	transmitState

Counter	Inter- pretation	Internal Basename
	See the stat command in the Tcl Development Guide and C++ Development Guide.	
Capture State	Not shown in IxExplorer. The current capture state of the port. See the stat command in the Tcl Development Guide and C++ Development Guide.	captureState
Pause State	Not shown in IxExplorer. The current pause state of the port. See the stat command in the Tcl Development Guide and C++ Development Guide.	pauseState
Common		
Frames Sent & Rate	A counter that increments only when a frame is successfully transmitted. This counter does not count collision attempts.	framesSent
Valid Frames Received & Rate	The valid frame size is from 64 bytes to 1518 bytes inclusive of FCS, exclusive of preamble and SFD and must be an integer number of octets. This 32 bit counter only counts frames	framesReceived

Counter	Inter- pretation	Internal Basename
	with good FCS. VLAN tagged frames that are greater than 1518 but less than 1522 bytes in size are also counted by this counter.	
Bytes Sent & Rate	A counter that counts the total number of bytes transmitted.	bytesSent
Bytes Received & Rate	A counter that counts the total number of bytes received.	bytesReceived
Bits Sent & Rate	A counter that counts the total number of bits transmitted.	bitsSent
Bits Received & Rate	A counter that counts the total number of bits received.	bitsReceived
Scheduled Transmit Time	The scheduled transmit time associated with the port.	scheduledTransmitTime
CPU Status	The status of the port's CPU.	portCpuStatus
CPU DoD Status	The status of the port's DoD process.	portCpuDodStatus
Transmit Dur- ation		
Transmit Dur- ation	Reserved for future use	transmitDuration
Quality of Service		
Quality of Service 0 - 7 &	Counters which increment each	qualityOfService0qualityOfService1

Counter	Inter- pretation	Internal Basename
Rate	time a frame with that particular QoS setting is received. (N/A to OC192-3)	
Framer Stats		
Framer CRC Errors	CRC errors detected by the POS framer.	framerFCSErrors
Framer Abort	POS frames aborted by the Framer.	framerAbort
Framer Min Length & Rate	POS frames received with less than the minimum length.	framerMinLength
Framer Max Length & Rate	POS frames received with more than the maximum length.	framerMaxLength
Extended Framer Stats		
Framer Frames Sent	Reserved for future use.	framerFramesTx
Framer Frames Received	Reserved for future use.	framerFramesRx
Checksum Stats		
IP Packets Received	The number of IP packets received.	ipPackets
UDP Packets Received	The number of UDP packets received.	udpPackets
TCP Packets Received	The number of TCP packets received.	tcpPackets
IP Checksum Errors	The number of IP checksum errors	ipChecksumErrors

Counter	Inter- pretation	Internal Basename
	detected.	
UDP Check- sum Errors	The number of UDP checksum errors detected.	udpChecksumErrors
TCP Checksum Errors	The number of TCP checksum errors detected.	tcpChecksumErrors
Data Integrity		
Data Integrity Frames	The number of data integrity frames received.	dataIntegrityFrames
Data Integrity Errors	The number of data integrity errors detected.	dataIntegrityErrors
Sequence Checking		
Sequence Frames	The number of sequence checking frames received.	sequenceFrames
Sequence Errors	The number of sequence checking errors detected.	sequenceErrors
Small Sequence Errors	The number of times when the current sequence number minus the previous sequence number is less than or equal to the error threshold and not negative, or when the current sequence number is equal to the previous sequence number.	smallSequenceErrors
Big Sequence Errors	The number of times when the	bigSequenceErrors

Counter	Inter- pretation	Internal Basename
	current sequence number minus the previous sequence number is greater than the error threshold.	
Reverse Sequence Errors	The number of times when the current sequence number is less than the previous sequence number.	reverseSequenceErrors
Total Sequence Errors	The sum of the small, bug and reverse sequence errors.	totalSequenceErrors
Packet Group Mode		
Packets Skipped In Packet Group Mode	The number of packets which were not assigned to a packet group. This can occur if the packet contains the anticipated packet group signature, but is too short to hold the group ID.	packetsSkippedInPacketGroupMode
IxRouter Stats		
General		
IxRouter Server Trans- mit	Packets trans- mitted by the pro- tocol handler.	protocolServerTx
IxRouter Receive	Packets received by the protocol handler.	protocolServerRx
VLAN Dropped Frames	The number of VLAN frames dropped by the	protocolServerVlan DroppedFrames

Counter	Inter- pretation	Internal Basename
	IxRouter.	
ARP		
Transmit Arp Reply	Number of ARP replies generated.	txArpReply
Transmit Arp Request	Number of ARP requests generated.	txArpRequest
Receive Arp Reply	Number of ARP replies received.	rxArpReply
Receive Arp Request	Number of ARP requests received.	rxArpRequest
ICMP		
Receive Ping Reply	Number of Ping replies received. (N/A to OC192-3)	rxPingReply
Receive Ping Request	Number of Ping requests gen- erated. (N/A to OC192-3)	rxPingRequest
Transmit Ping Reply	Number of Ping replies generated. (N/A to OC192-3)	txPingReply
Transmit Ping Request	Number of Ping requests received. (N/A to OC192-3)	txPingRequest
Asynchronous Frames Sent	The number of frames sent as a result of user request	asynchronousFramesSent
Scheduled Frames Sent	The number of frames originating from the stream engine.	scheduledFramesSent
Port CPU Frames Sent	The number of frames originating from the port's	portCPUFramesSent

Counter	Inter- pretation	Internal Basename
	CPU as opposed to the stream engine.	
DHCPv4		
DHCPv4 Dis- covered Mes- sages Sent	The number of Discovered messages sent	dhcpV4DiscoveredMessagesSent
DHCPv4 Offers Received	The number of Offer messages received.	dhcpV4OffersReceived
DHCPv4 Requests Sent	The number or Request mes- sages sent.	dhcpV4RequestsSent
DHCPv4 ACKs Received	The number or ACK messages received.	dhcpV4AcksReceived
DHCPv4 NACKs Received	The number of NACK messages received	dhcpV4NacksReceived
DHCPv4 Releases Sent	The number of Release messages sent.	dhcpV4ReleasesSent
DHCPv4 Enabled Inter- faces	The number of enabled interfaces.	dhcpV4EnabledInterfaces
DHCPv4 Addresses Learned	The number of address learned.	dhcpV4AddressesLearned
DHCPv6		
DHCPv6 Soli- cits Sent	The number of DHCPv6 Solicits Sent	dhcpV6SolicitsSent
DHCPv6 Advert- isements Received	The number of DHCPv6 Advertisements Received.	dhcpV6AdvertisementsReceived
DHCPv6 Requests Sent	The number of DHCPv6 Requests Sent.	dhcpV6RequestsSent

Counter	Inter- pretation	Internal Basename
DHCPv6 Declines Received	The number of DHCPv6 Declines Received.	dhcpV6DeclinesSent
DHCPv6 Replies Received	The number of DHCPv6 Replies Received.	dhcpV6RepliesReceived
DHCPv6 Releases Sent	The number of DHCPv6 Releases Sent.	dhcpV6ReleasesSent
DHCPv6 Enabled Inter- faces	The number of DHCPv6 Enabled Interfaces.	dhcpV6EnabledInterfaces
DHCPv6 Addresses Learned	The number of DHCPv6 Addresses Learned.	dhcpV6AddressesLearned
Ethernet OAM Stats		
EOAM Inform- ation PDUs Sent	The number of OAM Information PDUs Sent	ethernetOAMInformationPDUs Sent
EOAM Inform- ation PDUs Received	The number of OAM Information PDUs Received	ethernetOAMInformationPDUs Received
EOAM Event Notification PDUs Received	The number of OAM Event Noti- fication PDUs Received	ethernetOAMEventNotification PDUsReceived
EOAM Loop- back Control PDUs Received	The number of OAM Loopback Control PDUs Received	ethernetOAMLoopbackControl PDUsReceived
EOAM Organ- ization PDUs Received	The number of OAM Organization PDUs Received	ethernetOAMOrgPDUsReceived
EOAM Variable Request PDUs Received	The number of OAM Variable Request PDUs Received	ethernetOAMVariableRequest PDUsReceived
EOAM Variable	The number of	ethernetOAMVariableResponse PDUsReceived

Counter	Inter- pretation	Internal Basename
Response PDUs Received	OAM Variable Response PDUs Received	
EOAM Unsup- ported PDUs Received	The number of OAM Unsupported PDUs Received	ethernetOAMUnsupportedPDUs Received
BGP		
BGP Sessions Configured	The number of BGP4 sessions that were configured.	bgpTotalSessions
BGP Sessions Established	The number of configured BGP4 sessions that established adjacencies.	bgpTotalSessionsEstablished
IGMP		
Received IGMP Frames	The number of IGMP frames received by all logical hosts after being internally broadcast (For newer IGMPv3 emulation).	rxIgmpFrames
Transmitted IGMP Frames	The number of IGMP frames transmitted. (For newer IGMPv3 emulation).	txIgmpFrames
ISIS		
ISIS L1 Sessions Configured	The total number of level 1 configured sessions.	isisSessionsConfiguredL1
ISIS L2 Ses- sions Con- figured	The total number of level 2 configured sessions.	isisSessionsConfiguredL2
ISIS L1 Ses- sions Up	The total number of level 1 configured sessions that are fully up.	isisSessionsUpL1

Counter	Inter- pretation	Internal Basename
ISIS L2 Sessions Up	The total number of level 2 configured sessions that are fully up.	isisSessionsUpL2
MLD		
MLD Frames Received	The number of MLD frames received by all logical hosts after being internally broadcast.	rxMldFrames
MLD Frames Transmitted	The number of MLD frames transmitted.	txMIdFrames
OSPF		
OSPF Total Sessions	The number of OSPF sessions that were configured.	ospfTotalSessions
OSPF Neigh- bors in Full State	The number of OSPF neighbors that are fully up.	ospfFullNeighbors
OSPFv3		
OSPFv3 Ses- sions Con- figured	The number of OSPFv3 sessions that were configured.	ospfV3SessionsConfigured
OSPFv3 Neighbors in Full State	The number of OSPFv3 neighbors that are fully up.	ospfV3SessionsUp
PIM-SM		
PIM-SM Routers Con- figured	The number of configured PIM-SM routers.	pimsmRoutersConfigured
PIM-SM Routers Run- ning	The number of PIM-SM routers in the run state.	pimsmRoutersRunning
PIM-SM Learned Neigh-	The number of learned PIM-SM	pimsmNeighborsLearned

Counter	Inter- pretation	Internal Basename
bors	neighbors.	
RSVP		
RSVP Ingress LSPs Con- figured	The number of ingress LSPs configured.	rsvpIngressLSPsConfigured
RSVP Ingress LSPs Up	The number of ingress LSPs configured and running.	rsvpIngressLSPsUp
RSVP Egress LSPs Up	The number of egress LSPs configured and running.	rsvpEgressLSPsUp
LDP		
LDP Sessions Configured	The number of LDP sessions configured for targeted peers.	IdpSessionsConfigured
LDP Sessions Up	The number of LDP sessions configured and running with targeted peers.	IdpSessionsUp
LDP Basic Sessions Up	The number of LDP sessions up for broadcast peers.	IdpBasicSessionsUp
Ethernet		
Fragments & Rate	A counter that counts the number of frames less than 64 bytes in size with a bad FCS.	fragments
Undersize & Rate	A counter that counts the number of frames less than 64 bytes in size with a good FCS.	undersize

Counter	Inter- pretation	Internal Basename
Oversize & Rate	A counter that counts the number of frames greater than 1518 bytes in size. The following modules count oversize packets with both good and bad FCSs: 10/100 TX, and 10/100 MII. All other modules include oversize packets with a good FCSs only.	oversize
CRC Errors & Rate	A counter that counts all valid size frames that have CRC errors.	fcsErrors
Vlan Tagged Frames & Rate	A counter that counts the number of VLAN tagged frames.	vlanTaggedFramesReceived
Line Errors & Rate	A counter that counts the number of 4B/5B (100Mbps) or 8B/10B (Gigabit) symbol errors.	symbolErrors
Flow Control Frames & Rate	A counter that counts the number of PAUSE frames received. This counter only increments when Flow Control is enabled for that port (using the port properties dialog).	flowControlFrames
10/100		
Alignment Errors & Rate	A counter that counts all frames that are <b>not</b> an	alignmentErrors

Counter	Inter- pretation	Internal Basename
	integer multiple of 8 bits and have an invalid FCS. The frame is truncated to the nearest octet and then the FCS is validated. If the FCS is bad, then this frame is counted as an alignment error.	
Dribble Errors & Rate	A counter that counts all frames that are <b>not</b> an integer multiple of 8 bits and have a valid FCS. The frame is truncated to the nearest octet and then the FCS is validated. If the FCS is good, then this frame is counted as a dribble bit error.	dribbleErrors
Collisions & Rate	A counter that counts all occurrences (only one count per frame or fragment) of the Collision Detect signal from the physical layer controller that are not late collisions.	collisions
Late Collisions & Rate	A counter that counts all collisions that occur after the 512th bit time (preamble included) or after the 56th byte.	lateCollisions
Collision Frames & Rate	A counter that counts the num-	collisionFrames

Counter	Inter- pretation	Internal Basename
	ber of frames that were retrans- mitted due to one or more col- lisions.	
Excessive Collision Frames & Rate	A counter that counts the number of frames that were attempted to be sent but had 16 or more consecutive collisions.	excessiveCollisionFrames
Gigabit		
Oversize and CRC Errors & Rate	A counter that counts the number of frames greater than 1518 bytes in size with a bad FCS.	oversizeAndCrcErrors
Line Error Frames & Rate	A counter that counts the number of frames received that contain symbol errors.	symbolErrorFrames
Byte Align- ment Error & Rate	A counter that counts the number of times that a comma character is detected to be out of alignment.	synchErrorFrames
POS		
Section LOS	`OK' or `ALARM' during loss of signal. (See note 3 in Notes.)	sectionLossOfSignal
Section LOF	`OK' or `ALARM' during loss of frame. (See note 3 in Notes.)	sectionLossOfFrame
Section BIP	The number of	sectionBip

Counter	Inter- pretation	Internal Basename
(B1) & Rate	section bit inter- leaved parity errors.	
Line AIS	`OK' or `ALARM' during a line alarm indication signal condition. (See note 3 in Notes.)	lineAis
Line RDI	`OK' or `ALARM' during a remote defect indication. (See note 3 in Notes.)	lineRdi
Line REI(FEBE) & Rate	A count of the number of remote error indicate conditions.	lineRei
Line BIP(B2) & Rate	The number of line bit interleaved parity errors.	lineBip
Path AIS	`OK' or 'ALARM' during a path alarm indication signal condition. (See note 3 in Notes.)	pathAis
Path RDI	`OK' or `ALARM' during a path remote defect indication. (See note 3 in Notes.)	pathRdi
Path REI (FEBE) & Rate	A count of the number of path remote error indicate conditions.	pathRei
Path BIP(B3) & Rate	The number of path bit interleaved parity errors.	pathBip
Path LOP	`OK' or `ALARM'	pathLossOfPointer

Counter	Inter- pretation	Internal Basename
	during a loss of pointer condition. (See note 3 in Notes.)	
Path PLM(C2)	Either `OK' or `ALARM' along with the current received path signal label byte. `ALARM' occurs when a path signal label mismatch occurs. (See note 5 in Notes.)	pathPlm
Section BIP Errored Seconds	A count of the number of seconds during which (at any point during the second) at least one section layer BIP was detected.	sectionBipErroredSecs
Section BIP Severely Errored Seconds	A count of the number of seconds during which K or more Section layer BIP errors were detected, where K = 2,392 for OC-48 (per ANSI T1.231-1997).	sectionBipSeverlyErroredSecs
Section LOS Seconds	A count of the number of seconds during which (at any point during the second) at least one section layer LOS defect was present.	sectionLossOfSignalSecs
Line BIP Errored	A count of the seconds during	lineBipErroredSecs

Counter	Inter- pretation	Internal Basename
Seconds	which (at any point during the second) at least one Line layer BIP was detected.	
Line REI Errored Seconds	A count of the seconds during which at least one line BIP error was reported by the far end.	lineReiErroredSecs
Line AIS Alarmed Seconds	A count of the seconds during which (at any point during the second) at least one Line layer AIS defect was present.	lineAisAlarmSecs
Line RDI Unavailable Seconds	A count of the seconds during which the line is considered unavailable at the far end.	lineRdiUnavailableSec
Path BIP Errored Seconds	A count of the seconds during which (at any point during the second) at least one Path BIP error was detected.	pathBipErroredSecs
Path REI Errored Seconds	A count of the seconds during which (at any point during the second) at least one STS Path error was reported by the far end.	pathReiErroredSecs
Path AIS Alarmed Seconds	A count of the seconds during which (at any	pathAisAlarmSec

Counter	Inter- pretation	Internal Basename
	point during the second) an AIS defect was present)	
Path AIS Unavailable Seconds	A count of the seconds during which the STS path was considered unavailable.	pathAisUnavailableSecs
Path RDI Unavailable Seconds	A count of the seconds during which the STS path was considered unavailable at the far end.	pathRdiUnavailableSec
Input Signal Strength (dB)	(OC-192) This statistic monitors the receive optical input power. (See note 8 in Notes)	inputSignalStrength
POS K1 Byte	Monitors the k1 status byte in SONET Headers.	posK1byte
POS K2 Byte	Monitors the k1 status byte in SONET Headers.	posK2byte
SRP		
SRP Data Frames Received	The number of data frames received. IPv4 frames fall in this category.	srpDataFramesReceived
SRP Discovery Frames Received	The number of discovery type frames received.	srpDiscoveryFramesReceived
SRP IPS Frames Received	The number of IPS type frames received.	srpIpsFramesReceived
SRP Header	The number of	srpParityErrors

Counter	Inter- pretation	Internal Basename
Parity Errors	SRP frames received with SRP header parity error. This includes all frame types.	
SRP Usage Frames Received	The number of usage frames received with good CRC, good header parity, and only those that match the MAC address set for the SRP's port. Bad CRC frames, frames with header errors or those with other MAC addresses are received but not counted.	srpUsageFramesReceived
SRP Usage Frames Sent	The number of usage frames sent. These are sent periodically to keep the link alive.	srpUsageFramesSent
SRP Usage Status	If the number of consecutive timeouts exceeds the Keep Alive threshold, this status changes to FAIL. Otherwise shows OK.	srpUsageStatus
SRP Usage Timeouts	The number of times a usage frame was not received within the time period.	srpUsageTimeouts
RPR		
RPR Discovery Frames	The number of RPR discovery	rprDiscoveryFramesReceived

Counter	Inter- pretation	Internal Basename
Received	frames received.	
RPR Data Frames Received	The number of RPR encapsulated data frames received.	rprDataFramesReceived
RPR Fairness Frames Received	The number of RPR fairness frames received.	rprFairnessFramesReceived
RPR Fairness Frames Sent	The number of RPR fairness frames sent.	rprFairnessFramesSent
RPR Timeout Events	The number of timeouts that occurred waiting for RPR fairness frames.	rprFairnessTimeouts
RPR Header CRC Errors	The number of RPR frames received with header CRC errors.	rprHeaderCrcErrors
RPR OAM Frames Received	The number of RPR OAM frames received.	rprOamFramesReceived
RPR Payload CRC Errors	The number of RPR frames received with payload CRC errors.	rprPayloadCrcErrors
RPR Protection Frames Received	The number of RPR protection frames received.	rprProtectionFramesReceived
RPR Idle Frames Received	The number or RPR idle frames received.	rprIdleFramesReceived
GFP		
GFP Idle Frames	The number of GFP idle frames received.	gfpIdleFrames
GFP Sync State	The GFP sync state.	gfpSyncState

Counter	Inter- pretation	Internal Basename
GFP SYNC/HUNT Transitions	The number of Sync/Hunt state transition frames received.	gfpSyncHuntTransitions
GFP eHEC Errors	Number of GFP extension header HEC errors detected.	gfpeHecErrors
GFP Payload FCS Errors	Number of pay- load FCS errors detected.	gfpPayloadFcsErrors
GFP Receive Bandwidth	The measured receive GFP bandwidth, in Mbps.	gfpRxBandwidth
GFP tHEC Errors	Number of GFP type header HEC errors detected.	gfptHecErrors
BERT		
BERT Status	For BERT: The status of the connection. `Locked' when the receiving interface locks onto the data pattern. (See note 1 in Notes)	bertStatus
BERT Bits Sent	For BERT, it is the total number of bits sent.	bertBitsSent
BERT Bits Received	For BERT, it is the total number of bits received.	bertBitsReceived
BERT Bit Errors Sent	For BERT, it is the total number of bit errors sent.	bertBitErrorsSent
BERT Bit Errors Received	For BERT, it is the total number of bit errors received.	bertBitErrorsReceived
BERT Bit Error Ratio	For BERT, it is the ratio of the num-	bertBitErrorRatio

Counter	Inter- pretation	Internal Basename
	ber of errored bits compared to the total number of bits transmitted.	
BERT Errored Blocks	For BERT (EB) Number of blocks containing at least one errored second.	bertErroredBlocks
BERT Errored Seconds	For BERT (ES) Number of seconds con- taining at least one errored block or a defect.	bertErroredSeconds
BERT Errored Second Ratio	For BERT (ESR) the ratio of Errored Seconds (ES) to the total seconds.	bertErroredSecondRatio
BERT Severely Errored Seconds	For BERT (SES) Number of seconds with 30% or more of the errored blocks or a defect.	bertSeverelyErroredSeconds
BERT Severely Errored Second Ratio	For BERT (SESR) the ratio of Severely Errored Seconds (SESs) to the total seconds in available time.	bertSeverelyErroredSecondsRatio
BERT Error Free Seconds	For BERT (EFS) Number of seconds with no errored blocks or defects.	bertErrorFreeSeconds
BERT Available Seconds	For BERT (AS) Number of seconds which have occurred dur- ing Available Peri- ods.	bertAvailableSeconds

Counter	Inter- pretation	Internal Basename
BERT Unavail- able Seconds	For BERT (UAS) Number of seconds which have occurred during Unavailable Periods.	bertUnavailableSeconds
BERT Block Error State	For BERT Available Period or Unavailable Period, determined according to the running count and calculation of seconds in various error conditions. A min. of 10 non-SESs must pass for the state to change from Unavailable to Available. A min. of 10 SESs must pass for the state to change from Available to Unavailable to Unavailable. See note 4 in Notes.)	bertBlockErrorState
BERT Back- ground Block Errors	For BERT (BBE) The number of errored blocks not occurring as part of a Severely Errored Second.	bertBackgroundBlockErrors
BERT Back- ground Block Error Ratio	For BERT (BBER) the ratio of Back- ground Block Errors (BBEs) to the total number of blocks in avail- able time.	bertBackgroundBlockErrorRatio
BERT Elapsed Test Time	For BERT the elapsed test time, expressed in seconds.	bertElapsedTestTime
BERT Number	The number of	bertNumberMismatchedZeros

Counter	Inter- pretation	Internal Basename
Mismatched Zeros	expected zeroes received as ones.	
BERT Mis- matched Zeros Ratio	The ratio of the number of expected zeroes received as ones to all bits.	bertismatchedZerosRatio
BERT Number Mismatched Ones	The number of expected ones received as zeroes.	bertNumberMismatchedOnes
BERT Mis- matched Ones Ratio	The ratio of the number of expected ones received as zeroes to all bits.	bertMismatchedOnesRatio
Service Dis- ruption	A service dis- ruption is the period of time dur- ing which the ser- vice is unavailable while switching rings. The SONET spec calls for this to be less than 50 ms.	
Last Service Disruption Time (ms)	The length of the last service dis- ruption that occurred, expressed in mil- liseconds.	bertLastServiceDisruptionTime
Min Service Disruption Time (ms)	The shortest service disruption that occurred, expressed in milliseconds.	bertMinServiceDisruptionTime
Max Service Disruption Time (ms)	The longest service disruption that occurred, expressed in milliseconds.	bertMaxServiceDisruptionTime
Cumulative	The total service	bertServiceDisruptionCumulative

Counter	Inter- pretation	Internal Basename
Service Dis- ruption Time (ms)	disruption time encountered, expressed in milliseconds.	
DCC		
DCC Bytes Received	The number of DCC bytes received.	dccBytesReceived
DCC Bytes Sent	The number of DCC bytes sent.	dccBytesSent
DCC CRC Receive Errors	The number of DCC CRC errors received.	dccCrcErrorsReceived
DCC Frames Received	The number of DCC frames received.	dccFramesReceived
DCC Frames Sent	The number of DCC frames sent.	dccFramesSent
DCC Framing Errors Received	The number of DCC framing errors received.	dccFramingErrorsReceived
Link Fault Sig- nalling		
Insertion State	The current state of link fault insertion. 0 = not inserting, 1 = inserting.	insertionState
Link Fault State	The current state of link fault detection on a port. 0 = no fault, 1 = local fault, 2 = remote fault.	linkFaultState
Local Faults	The number of local faults detected.	localFaults
Remote Faults	The number of remote faults detected.	remoteFaults

Counter	Inter- pretation	Internal Basename
CDL	Converged Data Layer	
CDL Error Frames Received	The number of CDL error frames received.	cdlErrorFramesReceived
CDL Good Frames Received	The number of good CDL frames received.	cdlGoodFramesReceived.
FEC	Forwarding Error Correction	
FEC Corrected 0s Count	Number of 0 errors (1s changed to 0s) that have been corrected.	fecCorrected0sCount
FEC Corrected 1s Count	Number of 1 errors (0s changed to 1s) that have been corrected.	fecCorrected1sCount
FEC Corrected Bits Count	Number of flipped bits errors (0s changed to 1s and vice versa) that have been cor- rected.	fecCorrectedBitsCount
FEC Corrected Bytes Count	Number of bytes that have had errors corrected.	fecCorrectedBytesCount
FEC Uncor- rectable Subrow Count	Number of sub- rows that have had uncorrectable errors.	fecUncorrectableSubrowCount
OC192		
Temperature		
DMA Chip Temperature (C)	(OC-192 - Tem- perature Sensors Stats) Tem- perature of the DMA chip.	dMATemperature

Counter	Inter- pretation	Internal Basename
Capture Chip Temperature (C)	(OC-192 - Tem- perature Sensors Stats) Tem- perature of the Capture chip.	captureTemperature
Latency Chip Temperature (C)	(OC-192 - Tem- perature Sensors Stats) Tem- perature of the Latency chip.	latencyTemperature
Background Chip Tem- perature (C)	(OC-192 - Tem- perature Sensors Stats) Tem- perature of the Background chip.	backgroundTemperature
Overlay Chip Temperature (C)	(OC-192 - Tem- perature Sensors Stats) Tem- perature of the Overlay chip.	overlayTemperature
Front End Chip Temperature (C)	(OC-192 - Tem- perature Sensors Stats) Tem- perature of the Front End Chip.	frontEndTemperature
Scheduler Chip Temperature (C)	(OC-192 - Tem- perature Sensors Stats) Tem- perature of the Scheduler Chip.	scheduleTemperature
Plm Internal Chip Tem- perature 1 (C)	(OC-192 - Tem- perature Sensors Stats) Internal temperature of temperature measuring device #1.	plmDevice1InternalTemperature
Plm Internal Chip Tem- perature 2 (C)	(OC-192 - Tem- perature Sensors Stats) Internal temperature of temperature measuring device	plmDevice2InternalTemperature

Counter	Inter- pretation	Internal Basename
	#2.	
Plm Internal Chip Tem- perature 3(C)	(OC-192 - Temperature Sensors Stats) Internal temperature of temperature measuring device #3.	plmDevice3InternalTemperature
Fom Port Temperature (C)	(OC-192 - Tem- perature Sensors Stats) Tem- perature for one of the sensors on the Fiber optic module (Fom).	fobPort1Fp- gaTemperaturefobPort2FpgaTemperature
Fom Board Temperature (C)	(OC-192 - Tem- perature Sensors Stats) Tem- perature for one of the sensors on the Fiber optic module (Fom).	fobBoardTemperature
Fom Internal Temperature (C)	(OC-192 - Tem- perature Sensors Stats) Tem- perature for one of the sensors on the Fiber optic module (Fom).	fobDevice1InternalTemperature
VSR	The statistics in this sub-section relate to all VSR channels. See VSR per Channel statistics for further per-channel statistics.	
Rx Channel Protection Dis- abled	The status of the channel protection on the receiving interface.	rxChannelProtectionDisabled <sup>8</sup>
Rx Channel Skew Error	The status of the channel skew	rxChannelSkewError8

Counter	Inter- pretation	Internal Basename
	error detection on the receiving inter- face.	
RX Channel Skew First	The channel number of the earliest channel to arrive on the receiving interface. If more than one channel arrives at the same time, Channel #1 has the highest priority and so on.	rxChannelSkewFirst <sup>8</sup>
Rx Channel Skew Last	The channel number of the latest channel to arrive on the receiving interface. If more than one channel arrives at the same time, Channel #1 has the highest priority, and so on.	rxChannelSkewLast <sup>8</sup>
Rx Channel Skew Max	This counter increments every time the channel skew is equal to or greater than the maximum channel skew.	rxChannelSkewMax <sup>8</sup>
Rx Channel Swapped	Indicates one or more channel swap errors.	rxChannelSwapped <sup>8</sup>
Rx Code Word Violation Error	Indicates one or more 8b/10b code word violation errors.	rxCodeWordViolationError <sup>8</sup>
Rx CRC Cor- rected Errors	The number of cor- rected CRC block errors accu- mulated on the receiving inter-	rxCrcCorrectedErrorCounter <sup>8</sup>

Counter	Inter- pretation	Internal Basename
	face.	
Rx CRC Cor- rection Dis- abled	Indicates the status of the CRC correction on the receiving interface.	rxCrcCorrectionDisabled <sup>8</sup>
Rx CRC Error	Indicates one or more detected CRC errors.	rxCrcError8
Rx CRC Uncor- rected Errors	The number of uncorrected CRC block errors accumulated on the receiving interface.	rxCrcUnCorrectedErrorCounter <sup>8</sup>
Rx Hardware Error	The number of hardware errors detected on the receive side.	rxHardwareError <sup>8</sup>
Rx Loss Of Syn- chronization Counter	Indicates the number of times that a protection channels was in the loss of synchronization state.	rxLossOfSynchronizationCounter <sup>8</sup>
Rx Multi-loss Of Syn- chronization Counter	Indicates the number of times that two or more data or protection channels were in the Loss of Synchronization state.	rxMultiLossOfSynchronizationCounter <sup>8</sup>
Rx Multi-loss Of Syn- chronization Status	Indicates that two or more data or protection channels are in the Loss of Synchronization state.	rxMultiLossOfSynchronizationStatus <sup>8</sup>
Rx Out of Frame Counter	Indicates the number of frame	rxOutOfFrameCounter <sup>8</sup>

Counter	Inter- pretation	Internal Basename
	errors for the receiving interface.	
Rx Out of Frame Status	Indicates one or more out of frame errors for the receiving interface.	rxOutOfFrameStatus <sup>8</sup>
Rx Section BIP Error Counter	The number of Section BIP errors detected on the receiving interface.	rxSectionBipErrorCounter <sup>8</sup>
Tx Hardware Error Counter	The number of hardware errors detected on the transmit side.	txHardwareError8
Tx Out Of Frame Counter	The number of out of frame errors detected on the transmit side.	txOutOfFrameCounter <sup>8</sup>
Tx Out of Frame Status	Indicates one or more out of frame errors for the transmit interface.	txOutOfFrameStatus <sup>8</sup>
Tx Section BIP Error Counter	The number of Section Bit Inter- leaved Parity (BIP) errors which have been detec- ted on the trans- mit interface.	txSectionBipErrorCounter <sup>8</sup>
VSR per Chan- nel	The statistics in this sub-section relate to a specific VSR channel.	
Rx Code Word Violation Counter	This per-channel statistic indicates the number of codeword violations detected on	rxCodeWordViolationCounter <sup>9</sup>

Counter	Inter- pretation	Internal Basename
	the receiving chan- nel interface. Codeword viol- ations include run- ning disparity errors, undefined codewords, and any control char- acters besides K28.5.	
Rx CRC Error Counter	This per-channel statistic indicates the number of corrected and uncorrected errors on the receive interface.	rxCrcErrorCounter <sup>9</sup>
Rx Loss Of Syn- chronization Status	This per-channel statistic indicates the loss of synchronization status of the receiving interface.	rxLossOfSynchronization <sup>9</sup>
Rx Out of Frame Status	This per-channel statistic indicates the out of frame status of the receiving interface for a particular channel.	rxOutOfFrame <sup>9</sup>
10 Gig		
LSM		
Local Ordered Sets Sent	The number of local ordered sets sent. Ordered sets are part of Link Fault Signaling, and can be configured in the Link Fault Signaling tab.	localOrderedSetsSent
Local Ordered	The number of	localOrderedSetsReceived

Counter	Inter- pretation	Internal Basename
Sets Received	local ordered sets received. Ordered sets are part of Link Fault Signaling, and can be configured in the Link Fault Signaling tab.	
Remote Ordered Sets Sent	The number of remote ordered sets sent. Ordered sets are part of Link Fault Signaling, and can be configured in the Link Fault Signaling tab.	remoteOrderedSetsSent
Remote Ordered Sets Received	The number of remote ordered sets received. Ordered sets are part of Link Fault Signaling, and can be configured in the Link Fault Signaling tab.	remoteOrderedSetsReceived
Custom Ordered Sets Sent	The number of custom ordered sets sent. Ordered sets are part of Link Fault Signaling, and can be configured in the Link Fault Signaling tab.	customOrderedSetsSent
Custom Ordered Sets Received	The number of custom ordered sets received. Ordered sets are part of Link Fault Signaling, and can be configured in the Link Fault Signaling.	customOrderedSetsReceived

Counter	Inter- pretation	Internal Basename
	naling tab.	
Frames Received with Coding Errors	The number of frames received with coding errors.	codingErrorFramesReceived
Frames Received with /E/ error Character	The number of frames received with DUT labeled errors received.	eErrorCharacterFramesReceived
Dropped Frames	The number of dropped frames.	droppedFrames
Pause Frame		
Pause Acknow- ledge	The number of clocks for which transmit has been paused.	pauseAcknowledge
Pause End Frames	The number of pause frames received with a quanta of 0.	pauseEndFrames
Pause Over- write	The number of pause frames received while transmit was paused with a quanta not equal to 0.	pauseOverwrite
Temperature		
Lan Transmit FPGA Tem- perature	For the 10Gig LAN board, the temperature at the transmit FPGA.	10GigLanTxFpgaTemperature
Lan Receive FPGA Tem- perature	For the 10Gig LAN board, the temperature at the receive FPGA.	10GigLanRxFpgaTemperature
ATM and ATM/POS		
ATM AAL5 Bytes Received	The number of AAL5 bytes	atmAal5BytesReceived

Counter	Inter- pretation	Internal Basename
	received.	
ATM AAL5 Bytes Sent	The number of AAL5 bytes sent.	atmAal5BytesSent
ATM AAL5 CRC Error Frames	The number of AAL5 frames received with CRC errors.	atmAal5CrcErrorFrames
ATM AAL5 Frames Received	The number of AAL5 frames received.	atmAal5FramesReceived
ATM AAL5 Frames Sent	The number of AAL5 frames sent.	atmAal5FramesSent
ATM AAL5 Length Error Frames	The number of AAL5 frames received with length errors.	atmAal5LengthErrorFrames
ATM AAL5 Timeout Error Frames	The number of AAL5 frames received with timeout errors.	atmAal5TimeoutErrorFrames
ATM Cells Received	The number of ATM cells received.	atmCellsReceived
ATM Cells Sent	The number of ATM cells sent.	atmCellsSent
ATM Corrected HCS Error Count	The number of AAL5 frames received with HCS errors that were corrected.	atmCorrectedHcsErrorCount
ATM Idle Cell Count	The number of idle ATM cells sent.	atmIdleCellCount
ATM Sched- uled Cells Sent	The number of scheduled (non-idle) ATM cells sent.	atmScheduledCellsSent
ATM Uncor- rected HCS	The number of AAL5 frames	atmUncorrectedHcsErrorCount

Counter	Inter- pretation	Internal Basename
Error Count	received with HCS errors that were not corrected.	
ATM Unre- gistered Cells	The number of unregistered ATM cells that were received.	atmUnregisteredCellsReceived
OAM Tx Cells	Number of ATM OAM cells trans- mitted.	atmOamTxCells
OAM Tx Bytes	Number of ATM OAM bytes trans- mitted.	atmOamTxBytes
OAM Tx Fault Management AIS	Number of ATM OAM Fault Man- agement AIS cells transmitted.	atmOamTxFaultMgmtAIS
OAM Tx Fault Management RDI	Number of ATM OAM Fault Man- agement RDI cells transmitted.	atmOamTxFaultMgmtRDI
OAM Tx Fault Management CC	Number of ATM OAM Fault Man- agement CC cells transmitted.	atmOamTxFaultMgmtCC
OAM Tx Fault Management LB	Number of ATM OAM Fault Man- agement LB cells transmitted.	atmOamTxFaultMgmtLB
OAM Tx Fault ActDeact CC	Number of ATM OAM ActDeact cells transmitted.	atmOamTxActDeactCC
OAM Rx Good Cells	Number of ATM OAM good cells received.	atmOamRxGoodCells
OAM Rx Bytes	Number of ATM OAM bytes received.	atmOamRxBytes
OAM Rx Fault Management AIS	Number of ATM OAM Fault Man- agement AIS cells	atmOamRxFaultMgmtAIS

Counter	Inter- pretation	Internal Basename
	received.	
OAM Rx Fault Management RDI	Number of ATM OAM Fault Man- agement RDI cells received.	atmOamRxFaultMgmtRDI
OAM Rx Fault Management CC	Number of ATM OAM Fault Man- agement CC cells received.	atmOamRxFaultMgmtCC
OAM Rx Fault Management LB	Number of ATM OAM Fault Man- agement LB cells received.	atmOamRxFaultMgmtLB
OAM Rx Bad Cells	Number or ATM OAM bad cells received.	atmOamRxBadCells
OAM Rx ActDe- act CC	Number of ATM OAM ActDeact cells transmitted.	atmOamRxActDeactCC
Ethernet CRC	The Ethernet CRC, representing AAL5 CRCs.	ethernetCrc
Power Over Ethernet		
PoE Status	The PoE status.	poeStatus
PoE Input Voltage	The PoE input voltage.	poeInputVoltage
PoE Input Cur- rent	The PoE input current.	poeInputCurrent
PoE Input Power	The PoE input power.	poeInputPower
PoE Amplitude Arm Status	The state of the current signal acquisition arming for amplitude measurements.	poeAmplitudeArmStatus
PoE Amplitude Done Status	Indicates whether the signal acquisition of the amp-	poeAmplitudeDoneStatus

Counter	Inter- pretation	Internal Basename
	litude meas- urement has occurred.	
PoE Amplitude Time Status	The state of the current signal acquisition arming for time measurements.	poeTimeArmStatus
PoE Amplitude Time Status	Indicates whether the signal acquisition of the time measurement has occurred.	poeTimeDoneStatus
PoE Trigger Amplitude DC Amps	The DC amps of the measured PoE amplitude measurements.	poeTriggerAmplitudeDCAmps
PoE Trigger Amplitude DC Volts	The DC voltage of the measured PoE amplitude measurements.	poeTriggerAmplitudeDCVolts
PoE Active Input	Displays the type of PSE in use, Alt. A or Alt B.	poeActiveInput
PoE Tem- perature	The temperature of the PoE port, in Celsius.	poeTemperature
PoE AutoCal- ibration	The stage in the port diagnostic test.	poeAutocalibration
Stream Extraction Module		
Bytes from Application	The number of bytes received on either port 2 or 3 from the application.	bytesFromApplication
Packets from Application	The number of packets received on either port 2 or 3 from the applic-	packetsFromApplication

Counter	Inter- pretation	Internal Basename
	ation.	
Bytes from Port 2	The number of bytes received on the monitor port from port 2.	monitorBytesFromPort2
Bytes from Port 3	The number of bytes received on the monitor port from port 3.	monitorBytesFromPort3
Packets from Port 2	The number of packets received on the monitor port from port 2.	monitorPacketsFromPort2
Packets from Port 3	The number of packets received on the monitor port from port 3.	monitorPacketsFromPort3

### **Notes**

#### Notes for Statistics Counters

NOTE	Choices Displayed for Statistic
1	Locked - All Ones
	Locked - Inverted Alternating One/Zero
	Locked - Inverted User Defined Pattern
	Locked - Inverted 2^31 Linear Feedback Shift Reg
	Locked - Inverted 2^11 Linear Feedback Shift Reg
	Locked - Inverted 2^15 Linear Feedback Shift Reg
	Locked - Inverted 2^20 Linear Feedback Shift Reg
	Locked - Inverted 2^23 Linear Feedback Shift Reg
	Locked - All Zero
	Locked - Alternating One/Zero
	Locked - User Defined Pattern
	Locked - 2^11 Linear Feedback Shift Reg
	Locked - 2^15 Linear Feedback Shift Reg

NOTE	Choices Displayed for Statistic
	Locked - 2^20 Linear Feedback Shift Reg
	Locked - 2^23 Linear Feedback Shift Reg
	Not Locked
2	Demo Mode
	Link Up
	Link Down
	Loopback
	WriteMii
	Restart AutoNegotiate
	End RestartAutoNegotiate
	AutoNegotiate
	WriteMii Failed
	No Transceiver
	Invalid PHY Address
	Read LinkPartner
	No LinkPartner
	FPGA Download Failed
	No GBIC Module
	Fifo Reset
	Fifo Reset Compete
	PPP Off
	PPP Up
	PPP Down
	PPP Init
	PPP WaitForOpen
	PPP AutoNegotiate
	PPP Close
	PPP Connect
	Loss of Frame

NOTE	Choices Displayed for Statistic
	Loss of Signal
	StateMachine Failure
	PPP RestartNegotiation
	PPP RestartNegotiation Init
	PPP RestartNegotiation WaitForOpen
	PPP RestartNegotiation WaitForClose
	PPP RestartNegotiation Finish
	LP Boot Failed
	PPP Disabled - LOF
	Ignore Link
	Temperature Alarm
	PPP Closing
	PPP LCP Negotiate
	PPP Authenticate
	PPP NCP Negotiate
3	OK
	Alarm
	`_'
	Defect
4	Unavailable Period
	Available Period
5	OK
	OK (%)
	Alarm (%)
	`_'
6	OC-3c
	OC-12c
	OC-48c
	OC-192c

NOTE	Choices Displayed for Statistic
	10GE WAN
	10 Mbps
	100 Mbps
	1000 Mbps
7	Full
	Half
8	Loss of Signal
	[-] %d.%d
8	The statistics in this section must be accessed using the <i>vsrStat</i> command in TCL and the <i>TCLvsrStat</i> class in C++.
9	The statistics in this section must be accessed using the <i>vsrStat</i> command in TCL and the <i>TCLvsrStat</i> class in C++. In addition, the desired channel must be set with the <i>getChannel</i> sub-command (TCL) or method (C++).

# Statistics for 10/100 Cards

Statistics for 10/100 Cards

		Normal			Qos	St	ream	Trigg	er
	Capture	PacketGroup	RxTcpRoundTrip	RxFirstTimeStamp	Capture	Capture	PacketGroup	RxTcpRoundTrip	RxFirstTimeStamp
Type: User Configurable									
UserDefinedStat1	Х	Х	Χ	Х		Х	X	Х	Х
UserDefinedStat2	Х	X	Х	X		X	X	X	Х
CaptureTrigger	X		Х			X		X	
CaptureFilter	X		Х			Х		Х	
StreamTrigger1						Х			
StreamTrigger2						X			
Type: States									

		Normal			Qos	St	ream	Trigg	er
	Capture	PacketGroup	RxTcpRoundTrip	RxFirstTimeStamp	Capture	Capture	PacketGroup	RxTcpRoundTrip	RxFirstTimeStamp
Link	Х	Х	Х	Х	Х	Х	Х	Х	Х
LineSpeed	X	X	Х	Х	X	X	X	X	Х
DuplexMode	X	X	Х	Х	X	Х	X	Х	Х
TransmitState	X	X	Х	Х	Х	Х	Х	Х	Х
CaptureState	Х	X	Χ	Х	Х	Х	Х	Х	Х
PauseState	X	X	Χ	Х	Х	Х	Х	Х	Х
Type: Common									
FramesSent	X	X	Χ	Х	Х	Х	Х	Х	Х
FramesReceived	Х	X	Χ	Х	Х	X	X	Х	Х
BytesSent	Х	X	Х	Х	Х	Х	Х	Х	Х
BytesReceived	X	X	Х	Х		Х	Х	Х	Х
FcsErrors	X	X	Х	Х	Х	Х	X	Х	Х
BitsReceived	Х	X	Х	Х		Х	Х	Х	Х
BitsSent	Х	X	Χ	Х	Х	X	Х	Х	Х
PortCpuStatus									
PortCpuDodStatus									
Type: Transmit Duration									
TransmitDuration	X	X		Х	X	X	X		Х
Type: Quality of Service									
QualityOfService0					Х				
Type: Ethernet									
Fragments	Х	Х	Х	Х	Х	Х	Х	Х	X
Undersize	X	X	Х	Х	Х	Х	Х	Х	Х

		Normal			Qos	St	ream	Trigg	er
	Capture	PacketGroup	RxTcpRoundTrip	RxFirstTimeStamp	Capture	Capture	PacketGroup	RxTcpRoundTrip	RxFirstTimeStamp
Oversize	X	X	X	X	X	X	X	X	X
VlanTaggedFramesRx	X		Χ					X	
FlowControlFrames	X	Х	Х	Х	X	X	X	X	Х
Type: 10/100									
AlignmentErrors	X	Х	Х	Х	X	X	X	X	Х
DribbleErrors	X	Х	Х	Х		Х	Х	Х	Х
Collisions	X	Х	Х	Х	Х	Х	Х	Х	Х
LateCollisions	X	Х	Х	Х	X	X	X	X	Х
CollisionFrames	X	Х	Х	Х	Х	Х	Х	Х	Х
ExcessiveCollisionFrames	X	Х	Х	Х	Х	Х	X	X	Х
Type: 10/100 + Gigabit									
SymbolErrors	X								
OversizeAndCrcErrors									

## Statistics for 10/100 TXS Modules

#### Statistics for 10/100 TXS Modules

			No	or m	al												ger		м	o d e C	hecl	k s u m	Erro	rs	М	ode	Data	Int	egri	tv
	Capture	PacketGroup	RXTcpRoundTrip	RxDataIntegrity	RXFirstTimeStamp a	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RXFirstTimeStamp 0	RxModeWidePacketGroup	Capture	PacketGroup	RXTcpRoundTrip	RxDataIntegrity 3	RxFirstTimeStamp	RxSequenceChecking a	RxModeWidePacketGroup	Capture	PacketGroup BP	RxDataIntegrity a	RXFirstTimeStamp n	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup p	RxDataIntegrity p	RXFirstTimeStamp u	RxSequenceChecking 6	RxModeWidePacketGroup
Capture	ဦ	Pa	2	Rx	\$	2	RX	ca	Pa	Ð	æ	ප	Pa	2	RX	2	2	æ	Ca	Ра	Rx	2	2	\X	Ca	Pa	Æ	2	2	X
Type: User Configurable																														
UserDefinedStat1	X	X	X	X	X	X	X					X	X	Х	x	X	X	x	X	X	x	X	X	X	x	X	X	X	X	x
UserDefinedStat2	X	X	Х	X	X	X	Х					X	X	X	X	X	X	X			x		X		x	X	X	X	X	x
CaptureTrigger	X	X	Х		X		X					X	X	Х		X		X	X	X		X		X	X	X		X		X
CaptureFilter	X	X	Х		Х		Х					х	Х	Х		X		Х	x	х		X		X	x	X		X		х
StreamTrigger1												Х	Х			Х		Х												

			No	rm	al				Q	0 S			Sti	rea	m T	rig	ger		М	o d e C	heck	(sum	Erro	rs	М	o d e	Data	ıInt	egri	ty
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
StreamTrigger2												Х	Х			Х		Х												
Type: States																														
Link	X	X	х	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X	x	X
LineSpeed	X	Х	х	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	Х	Х	X	х	х	X	Х	Х	X	Х	Х	X	x	Х	X	X	X
DuplexMode	X	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	х	х	х	х	х	х	Х	X	X	х	X	Х	X	X	Х	Х	Х	X
TransmitState	X	Х	Х	Х	Х	X	Х	Х	X	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	X	X	Х	X	X	X	Х	Х	X	X	X
CaptureState	Х	Х	X	Х	Х	Х	X	Х	Х	Х	Х	Х	Х	X	X	X	Х	х	Х	x	X	Х	х	x	X	Х	Х	X	X	Х
PauseState	X	Х	X	X	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	X	X	Х	Х	Х	X	X	Х	х	x	X	Х	Х	X	X	Х
Type: Common																														

			No	o r m	nal				Q	0 S			Sti	rea	m Tı	rigg	ger		М	o d e C	heck	su m	Erro	rs	М	o d e	Data	ıInt	egri	ty
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
FramesSent	Х	Х	х	Х	Х	Х	Х	Х	Х	Х	Х	х	Х	Х	х	х	х	х	Х	Х	Х	Х	х	Х	Х	х	Х	Х	Х	Х
FramesReceived	X	Х	х	Х	Х	Х	X	Х	Х	X	Х	х	X	Х	х	Х	х	х	Х	X	Х	Х	Х	Х	Х	х	Х	Х	Х	X
BytesSent	Х	Х	х	Х	Х	Х	X	Х	Х	Х	Х	Х	Х	Х	х	Х	Х	х	Х	Х	Х	X	Х	Х	x	х	Х	Х	X	Х
BytesReceived	X	Х	Х	X	X	X	Х					Х	Х	х	х	Х	х	х	х	X	X	X	X	X	Х	Х	X	X	X	X
FcsErrors	X	Х	Х	X	X	X	Х	Х	Х	Х	Х	Х	X	х	х	Х	х	х	Х	X	Х	X	X	X	Х	Х	Х	X	Х	X
BitsReceived	X	Х	Х	X	X	X	Х					Х	Х	Х	Х	Х	х	Х	X	X	X	X	X	X	Х	Х	Х	X	Х	X
BitsSent	X	Х	Х	X	X	X	X	Х	Х	Х	Х	Х	X	Х	Х	Х	х	х	x	X	X	X	X	X	Х	Х	Х	X	Х	X
PortCpuStatus	X	X		X	X	X	X	X	X	X	X	x	x		x	x	x	x	х	х	x	х	Х	Х	Х	Х	х	х	x	X

			No	o r m	al				Q	o s			Sti	rea	m T	rigg	ger		М	o d e C	heck	(sum	Erro	rs	М	o d e	Data	ıInt	egri	ty
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
PortCpuDodStatus	Х	Х		Х	Х	Х	Х	Х	Х	Х	Х	х	Х		Х	Х	Х	х	х	х	Х	х	х	Х	х	Х	Х	Х	Х	Х
Type: Transmit Duration																														
TransmitDuration	X	Х		X	X	X	X	X	X	X	X	Х	Х		Х	Х	Х	х	х	X	х	x	х	X	х	Х	Х	Х	Х	X
Type: Quality of Service																														
QualityOfService0								X	X	X	Х																			
Type: Checksum Stats																														
IpPackets																			Х	Х		Х		Х						
UdpPackets																			Х	X		Х		Х						
TcpPackets																			Х	X		Х		Х						

			No	or m	al				Q	0 S			Str	r e a	m T	rig	ger		М	o d e C	heck	sum	Erro	rs	М	o d e	Data	Int	egri	ty
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
IpChecksumErrors																			Х	Х		Х		Х						
UdpChecksumErrors																			Х	Х		Х		Х						
TcpChecksumErrors																			X	X		X		X						
Type: Data Integrity																														
DataIntegrityFrames				X											X						X						X			
DataIntegrityErrors				X											X						X						Х			
Type: Sequence Checking																														
SequenceFrames						X											Х						x						X	
SequenceErrors						X											Х						X						X	

			No	o r m	al				Q	o s			St	rea	m T	rig	ger		ModeChecksumErrors							ModeDataIntegrity						
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup		
Type: Ethernet																																
Fragments	X	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Undersize	Х	X	Х	X	X	Х	X	Х	X	X	X	Х	Х	Х	X	X	Х	Х	Х	Х	Х	X	Х	Х	X	X	X	X	X	Х		
Oversize	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	х	X	X	Х	х	Х	Х	Х	Х	Х	Х	X	Х	Х	Х	Х	Х		
VlanTaggedFramesRx	X	Х	х		X		Х							Х											X	Х		X		Х		
FlowControlFrames	X	X	х		Х		Х	X	Х	Х	X	х	X	X		X		X							X	Х		X		Х		
Type: 10/100																																
AlignmentErrors	X	X	х		X		Х							Х											X	X		X		X		
DribbleErrors	X	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	X	X	Х	X	Х	X	Х	Х	Х	Х	Х	X	Х	Х	Х	Х		

			No	or m	al				Q	0 S			Sti	ea	m Tı	rigg	ger		ModeChecksumErrors							ModeDataIntegrity						
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup		
Collisions	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
LateCollisions	X	X	х	X	X	X	X	X	X	X	X	x	Х	х	Х	Х	Х	Х	X	X	X	X	X	X	X	X	X	X	X	x		
CollisionFrames	X	Х	X	Х	X	Х	Х	Х	Х	X	Х	х	х	Х	х	х	Х	Х	X	X	Х	Х	x	X	X	Х	X	X	X	X		
Excess- iveCollisionFrames	Х	Х	Х	Х	X	Х	Х	X	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	x	x	x	x	x	x	X	X	Х	X	X	Х		
Type: 10/100 + Gigabit																																
SymbolErrors																																
OversizeAndCrcErrors	X	X		X	X	X	X	X	X	X	X	х	X		х	X	х	X	X	X	X	X	X	X	X	X	X	X	X	X		

## Statistics for 10/100/1000 TXS, 10/100/1000 XMS(R)12, 1000 SFPS4, and 1000STXS24 Cards

Statistics for 10/100/1000 TXS, 10/100/1000 XMS(R)12, 1000 SFPS4, and 1000STXS24 Cards

Statistics Mode		N	o r m	al			QoS			Strea	a m T r	igger		Mod	le C h e	cksu	m Eri	rors	Мс	d e D	ata rity		eg-
	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
Type: User Configurable																							
UserDefinedStat1	Х	Х	Х	Х	Х				Χ	Х	X	X	Х	Х	Х	X	X	Х	Х	Х	Х	Х	X
UserDefinedStat2	Х	Х	Х	Х	Х				Χ	X	X	X	Х		X	X	X		Х	Х	Х	Х	X
CaptureTrigger	X		X		X				Χ		X	X	X	X		X	X	Х	Х			Х	X
CaptureFilter	X		X		X				Χ		X	X	X	X		X	X	Х	Х			Х	X
StreamTrigger1									Χ				Х										
StreamTrigger2									Х				Х										
Type: States																							
Link	X	X	X	X	X	X	X	Х	X	X	X	Х	X	X	Х	X	X	X	Х	Х	X	X	X
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Statistics Mode		N	o r m	al			QoS	}		Strea	am Tr	igger		Mod	l e C h e	cksu	m Er	rors	Мс	d e D	ata rity	Int	e g -
	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
DuplexMode	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
TransmitState	Х	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	Х	X	Х	Х	X	Х	X	Х	Х	Х	Х	Х
CaptureState	Х	Х	Х	Х	Х	Х	X	X	Х	Х	Х	Х	X	X	X	X	X	X	Х	Х	Х	Х	Х
PauseState	Х	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	Х	X	Х	Х	Х	X	X	Х	Х	Х	Х	Х
Type: Common																							
FramesSent	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	Х	X	X	X	X	X	X	X	Х	Х	Х	Х	X
FramesReceived	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	X	X	Х	X	X	Х	X	X	Х	Х	Х	Х	X
BytesSent	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	X	X	Х	X	X	X	X	X	Х	Х	Х	Х	X
BytesReceived	Х	Х	Х	Х	Х				Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
FcsErrors	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	Х	Х	Х	Х
BitsReceived	Х	Х	Х	Х	Х				Х	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	Х	Х	Х	Х
BitsSent	X	Х	Х	X	X	Х	Х	Х	Х	Х	X	Х	X	X	X	Х	X	Х	X	X	Х	Х	X

Statistics Mode		N	orm	al			QoS	;		Strea	a m T r	igger		Mod	l e C h e	cksu	m Er	rors	Мо	d e D	ata rity		eg-
	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
PortCpuStatus					Х		Х	Х					Х					Х					Х
PortCpuDodStatus					Х		X	Х					X					X					Х
Type: Transmit Duration																							
TransmitDuration	Х	X	X	X	X	X	Х	X	X	X	X	X	X	X	X	X	X	X	X	Х	Х	Х	Х
Type: Quality of Service																							
QualityOfService0						Х	Х	Х															
Type: Checksum Stats																							
IPv4Packets														X	X								
UdpPackets														X	Х								
TcpPackets														X	Х								
IPv4ChecksumErrors														X	Х								
UdpChecksumErrors														X	Х								

Statistics Mode		N	o r m	al			QoS	}		Strea	a m T r i	igger		Mod	l e C h e	cksu	m Er	rors	Мс	d e D	ata rity		e g -
	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
TcpChecksumErrors														Х	Х								
Type: Data Integrity																							
DataIntegrityFrames			Х								Х					X					Х		
DataIntegrityErrors			Х								X					X					Х		
Type: Sequence Checking																							
SequenceFrames				Х								Χ					X					Х	
SequenceErrors				Х								Х					Х					Х	
Type: Ethernet																							
Fragments	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
Undersize	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
Oversize	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	Х

Statistics Mode		N	orm	al			QoS	;		Strea	a m T r	igger		Mod	le C h e	cksu	m Eri	rors	Мс	d e D	ata rity	Int	e g -
	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
VlanTaggedFramesRx	Х	Х			Х					Х					Х				Х	Х			Х
FlowControlFrames	Х	Х			Х	X	Х	Х	Х	X			X		Х				Х	Х			Х
Type: 10/100																							
AlignmentErrors					Х																		Х
DribbleErrors					Х		Х	Х					Х					Х					Х
Collisions					Х		Х	Х					Х					Х					Х
LateCollisions					Х		Х	Х					Х					Х					Х
CollisionFrames					Х		Х	Х					Х					Х					Х
ExcessiveCollisionFrames					Х		Х	Х					Х					Х					Х
Type: Gigabit																							
SymbolErrorFrames	Х	Х	Х	Х					Х	Х	Х	Х			Х	Х	Х		Х	Х	Х	Х	
SynchErrorFrames	Х	Х				Х			Х	Х					Х				Х	Х			

Statistics Mode		N	o r m	al			QoS	}		Strea	am Tr	igger		Mod	l e C h e	cksu	m Er	rors	Мс		ata rity	Inte	eg-
	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
Type: 10/100 + Gigabit																							
SymbolErrors	Х	Х								Х					Х				Х	Х			
OversizeAndCrcErrors	X	Х	X	Х	Х	X	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х

## Statistics for 10/100/1000 LSM XMV(R)4/8/12/16, and 10/100/1000 ASM XMV12X Cards

Statistics for 10/100/1000 LSM XMV(R)4/8/12/16, and 10/100/1000 ASM XMV12X Cards

Statistics Mode	, 10		orm		7(11)		QoS				a m T r i				odeD	ata Ir	ntegri	ty
Receive Mode	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
Type: User Configurable																		
UserDefinedStat1	X	X	X	X	X				X	X	X	X	X	X	X	X	X	X
UserDefinedStat2	X	X	X	X	X				X	X	X	X	X	X	X	X	X	X
CaptureTrigger	Х		X		X				X		X	Х	Х	Х			X	X
CaptureFilter	Х		Х		Х				Х		Х	Х	Х	Х			X	X
StreamTrigger1									Х				Х					
StreamTrigger2									Х				Х					
Type: States																		
Link	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	X
LineSpeed	Х	Х	Х	Х	X	X	Х	Х	Х	X	X	X	Х	X	X	X	X	X

Statistics Mode	Normal						QoS			Stre	a m T r i	gger		М	o d e D	ata In	ntegri	ty
Receive Mode	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
DuplexMode	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	X
TransmitState	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	X	Х	Х	Х	Х	Х	X	Х
CaptureState	Х	X	X	X	X	Х	X	Х	X	X	X	X	X	Х	X	X	X	X
PauseState	Х	X	X	X	X	Х	Х	X	X	X	X	X	X	Х	X	Х	X	X
Type: Common																		
FramesSent	Х	X	Х	X	X	Х	Х	X	X	X	X	X	X	Х	X	X	X	X
FramesReceived	Х	X	Х	X	Х	Х	X	Х	X	X	X	X	X	Х	X	Х	X	X
BytesSent	Х	X	X	X	X	Х	Х	Х	X	X	X	X	X	Х	X	X	X	X
BytesReceived	Х	Х	Х	Х	X				X	Х	X	X	Х	Х	Х	Х	X	Х
FcsErrors	Х	X	Х	X	Х	Х	Х	Х	X	Х	X	X	Х	Х	Х	Х	X	Х
BitsReceived	Х	Х	Х	Х	Х				X	Х	X	X	Х	Х	Х	Х	X	Х
BitsSent	Х	Х	Х	Х	X	X	Х	X	X	X	X	X	X	X	X	Х	X	Х

Statistics Mode		N	orm	a l			QoS			Stre	a m Tri	gger		М	o d e D a	ata In	tegri	ty
Receive Mode	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
PortCpuStatus					Х		Х	Х					Х					Х
PortCpuDodStatus					Х		Х	Х					Х					X
Type: Transmit Duration																		
TransmitDuration	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	X	X
Type: Quality of Service																		
QualityOfService0						Х	Х	Х										
Type: Checksum Stats																		
IPv4Packets	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	X	Х	X	X
UdpPackets	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	X	Х
TcpPackets	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	X	X	X	Х
IPv4ChecksumErrors	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	X	Х
UdpChecksumErrors	X	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	X

Statistics Mode		N	orm	a l			QoS			Stre	a m T r i	gger		М	o d e D	ata Ir	ntegri	ty
Receive Mode	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
TcpChecksumErrors	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	X	X
Type: Data Integrity																		
DataIntegrityFrames			Х								Х					Х		
DataIntegrityErrors			Х								Х					Х		
Type: Sequence Checking																		
SequenceFrames				Х								X					X	
SequenceErrors				Х								X					X	
Type: Ethernet																		
Fragments	Х	Х	Х	Х	Х	Х	Х	Х	X	X	Х	Х	Х	Х	Х	X	X	X
Undersize	Х	Х	Х	X	X	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	X
Oversize	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	Х	X	Х	Х	Х	X	X	X
VlanTaggedFramesRx	Х	Х			Х					Х				Х	Х			X

Statistics Mode		N	orm	a l			QoS			Stre	amTri	igger		М	o d e D a	ata In	tegri	ty
Receive Mode	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
FlowControlFrames	X	X			X	X	X	X	X	X			X	X	X			X
Type: 10/100																		
AlignmentErrors					X													X
DribbleErrors					X		X	X					X					X
Collisions					X		Х	Х					Х					Х
LateCollisions					Х		Х	Х					Х					Х
CollisionFrames					Х		Х	Х					Х					Х
ExcessiveCollisionFrames					Х		Х	Х					Х					Х
Type: Gigabit																		
SymbolErrorFrames	Х	Х	Х	Х					Х	Х	Х	Х		Х	Х	Х	Х	
SynchErrorFrames	Х	Х				Х			X	Х				X	X			
Type: 10/100 + Gigabit																		

Statistics Mode		N	orm	a l			QoS			Stre	a m T r i	gger		М	o d e D a	ata In	tegri	ty
Receive Mode	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
SymbolErrors	Х	X								Х				Х	X			
OversizeAndCrcErrors	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х

# **Statistics for Gigabit Modules**

#### Statistics for Gigabit Modules

			No	rm	al				Q	o s			Str	e a	m T					o d e C	heck	(sum	Erro	rs	М	o d e l	Data	Int	egri	ty
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
Type: User Configurable																														
UserDefinedStat1	X	Х	Х	Х	Х	Х	Х					Х	Х	Х	X	X	Х	X	x	х	x	х	Х	х	X	Х	X	Х	х	Х
UserDefinedStat2	X	Х	X	Х	Х	Х	Х					Х	Х	Х	X	Х	Х	X		x	x	x	x		X	Х	X	Х	x	X
CaptureTrigger	X		X	Х			Х					Х		Х	X		Х	Х	x		x		x	x	X				x	X
CaptureFilter	X		Х	Х			Х					Х		Х	Х		х	X	X		X		X	x	X				x	X
StreamTrigger1												Х						Х												
StreamTrigger2												Х						Х												

			No	o r m	nal				Q	o s			Sti	rea	m T	rig	g e r		М	o d e C	heck	sum	Erro	ors	М	o d e l	Data	Int	egri	ty
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
Type: States																														
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	X	x	x	x	X	X	X	X	X	X	X
LineSpeed	X	Х	X	Х	X	X	Х	Х	Х	X	Х	Х	Х	Х	x	Х	Х	Х	х	X	x	X	x	x	X	Х	X	Х	Х	X
DuplexMode	X	Х	Х	X	X	X	X	X	Х	X	X	Х	Х	Х	х	X	X	Х	x	Х	Х	X	x	х	X	Х	Х	Х	Х	Х
TransmitState	X	Х	X	X	X	X	X	X	X	X	X	X	Х	Х	Х	Х	Х	Х	x	X	x	x	х	X	X	X	Х	Х	X	Х
CaptureState	X	Х	X	X	X	X	X	X	X	X	X	X	Х	Х	Х	X	X	Х	x	X	X	X	Х	Х	X	X	X	X	Х	Х
PauseState	X	Х	X	X	X	X	X	X	X	X	X	X	Х	Х	Х	X	X	Х	x	X	x	Х	Х	Х	X	X	Х	Х	Х	X
Type: Common																														
FramesSent	Х	Х	Х	Х	Х	X	X	Х	Х	Х	Х	Х	Х	X	Х	Х	Х	Х	Х	Х	Х	Х	Х	X	X	X	Х	Х	Х	X

			No	rm	al				Q	0 S			Str	ea	m T	rig	ger		М	o d e C	heck	(sum	Erro	rs	М	o d e l	Data	Int	e g r i	ty
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
FramesReceived	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BytesSent	Х	Х	X	Х	Х	Х	Х	Х	Х	Х	X	Х	Х	Х	Х	Х	Х	Х	x	X	Х	Х	x	x	Х	Х	Х	Х	Х	X
BytesReceived	Х	Х	Х	Х	X	Х	X					Х	Х	Х	X	Х	Х	Х	х	Х	х	х	x	х	Х	х	Х	X	X	X
FcsErrors	Х	X	Х	Х	X	Х	X	X	Х	Х	X	Х	Х	Х	Х	Х	Х	Х	х	х	х	х	х	х	X	X	X	X	X	X
BitsReceived	X	X	X	X	X	X	X					Х	Х	Х	X	X	Х	Х	х	х	Х	X	x	x	X	X	X	X	X	X
BitsSent	X	X	X	Х	X	X	X	X	X	X	X	Х	Х	Х	X	X	Х	Х	x	х	Х	X	x	x	X	X	X	X	X	X
PortCpuStatus							X		X	X	Х							x						Х						X

			Νo	rm	al				Q	o s			Str	e a ı	m Tı	rig	ger		Мо	od e C	heck	s u m	Erro	ors	М	o d e l	Data	Int	egri	ty
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
PortCpuDodStatus							Х		Х	Х	Х							Х						Х						Х
Type: Transmit Duration																														
TransmitDuration	Х	Х		Х	Х	Х	Х	Х	Х	Х	X	X	Х		х	х	Х	х	Х	Х	х	Х	Х	Х	X	Х	Х	Х	X	X
Type: Quality of Service																														
QualityOfService0								Х	Х	Х	X																			
Type: Checksum Stats																														
IpPackets																			Х					Х						
UdpPackets																			Х					Х						
TcpPackets																			Х					Х						

			No	o r m	nal				Q	0 S			Str	e a	m T	rig	ger		М	o d e C	heck	sum	Erro	ors	М	o d e l	Data	Int	egri	ty
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
IpChecksumErrors																			Х					Х						
UdpChecksumErrors																			Х					Х						
TcpChecksumErrors																			X					X						
Type: Data Integrity																														
DataIntegrityFrames				X											X						x						X			
DataIntegrityErrors				X											X						Х						Х			
Type: Sequence Checking																														
SequenceFrames						X											X						х						X	
SequenceErrors						Х											Х						Х						Х	

			No	r m	nal				Q	o s			Sti	ea	m T	rig	ger		М	o d e C	heck	sum	Erro	ors	М	o d e l	Data	Int	egri	ty
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
Type: Ethernet																														
Fragments	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X	X	X	X
Undersize	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	x	X	x	X	X	X	X
Oversize	Х	Х	Х	Х	X	Х	Х	X	X	Х	X	Х	X	X	Х	х	Х	Х	Х	Х	X	X	x	Х	Х	х	Х	Х	Х	X
VlanTaggedFramesRx	X	Х	Х		X		X						X	X		Х				X		X			X	X		X		X
FlowControlFrames	X	Х	Х		X		X	X	X	X	X	Х	X	Х		X		X		x		Х			X	X		X		X
Type: 10/100																														
AlignmentErrors			Х				X							Х																x
DribbleErrors			Х				X		X	X	X			X				Х						Х						X

			No	rm	nal				Q	0 S			Str	ea	m T	rig	ger		М	o d e C	heck	(sum	Erro	ors	М	o d e	Data	ıInt	e g r i	ty
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
Collisions			X				X		X	X	X			X				X						X						x
LateCollisions			Х				X		Х	Х	Х			Х				Х						X						х
CollisionFrames			Х				X		Х	Х	X			Х				X						X						х
Excess-iveCollisionFrames			X				X		Х	Х	X			Х				Х						X						х
Type: Gigabit																														
SymbolErrorFrames	X	X		Х	X	X						Х	X		X	Х	Х			X	х	x	X		X	Х	X	X	X	
SynchErrorFrames	X	X			X			X				Х	X			Х				Х		х			X	Х		Х		
Type: 10/100 + Gig-																														

			No	rm	al				Q	0 S			Str	ea	m T	rig	ger		М	o d e C	heck	sum	Erro	rs	М	o d e l	Data	Int	egri	ty
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
abit																														
SymbolErrors	X	Х			Х								Х			X				x		x			X	Х		Х		
OversizeAndCrcErrors	Х	Х		Х	Х	Х	Х	Х	Х	Х	Х	х	Х		Х	Х	Х	Х	Х	x	X	X	x	x	X	Х	X	Х	Х	Х

# **Statistics for OC12c/OC3c Modules**

Statistics for OC12c/OC3c Modules

			Νo	rm	al				Q								geı			d e C	heck	(sum	ıErr	ors	Mo	d e E	Data	Int	e g r i	ity	Ad	d d' - I
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PoSExtendedStats	
Type: User Configurable																																
UserDefinedStat1	X	X	X	X	х	х	Х					X	Х	Х	х	X	X	X	x	Х	Х	х	Х	Х	Х	X	x	x	X	Х		
UserDefinedStat2	X	x	Х	X	X	X	Х					X	X	X	х	x	X	X		X	X	X	x		x	x	x	x	x	x		
CaptureTrigger	X		X				X					X		X				X	X					X	X					X		
CaptureFilter	X		X				X					X		X				X	X					X	X					X		

			Νo	rm	al				Q	o s			Str	e a ı	n T	rig	g e r		Мо	d e C	heck	(sum	Err	ors	Мс	od e [	Data	Int	egri	ity	A d	d'-
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PoSExtendedStats	
StreamTrigger1												X	X					X														
StreamTrigger2												Х	Х					Х														
Type: States																																
Link	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X	X	X	X	x	X	X	X	X	X	X	X	X	X		
LineSpeed	х	Х	X	X	X	X	х	х	X	X	Х	X	х	Х	X	Х	Х	Х	Х	Х	х	Х	Х	Х	X	X	x	X	x	x		
DuplexMode			X		X		X			X	Х			X		X		X				Х		X				X		X		
TransmitState	х	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	X	Х	X	X	X	X	X	X	X	X	x		

			Νo	rm	al				Q	0 S			Str	e a ı	m T	rig	geı	1	Мо	d e C	heck	(sun	ıErr	ors	Мс	o d e I	Data	Int	egri	ity	A d	l d'- I
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PoSExtendedStats	
CaptureState	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X	x	X	X	X	X	X	x	X	X	X		
PauseState	X	х	X	Х	X	Х	Х	x	X	х	x	Х	X	X	Х	X	X	X	x	X	Х	X	X	X	X	X	x	X	X	X		
Type: Common																																
FramesSent	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X	x	X	X	X	X	X	x	X	X	X		
FramesReceived	X	х	Х	Х	Х	X	Х	x	X	х	x	X	Х	X	Х	x	X	Х	x	X	Х	X	X	Х	x	x	x	x	X	x		
BytesSent	X	х	Х	Х	Х	Х	Х	х	Х	х	x	Х	Х	Х	Х	Х	Х	Х	x	x	Х	X	x	X	x	x	Х	x	x	x		

			No	rm	nal				Q	os			Str	e a ı	m T	rig	g e r	-	Мо	d e C	heck	(sun	ıErr	ors	Мс	d e E	ata	Int	egri	ity	A d	d'-
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PoSExtendedStats	
BytesReceived	X	X	X	X	X	X	X					x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x		
FcsErrors	X	х	X	X	х	X	X	X	X	X	х	X	X	X	X	X	X	X	X	X	Х	X	X	X	x	X	x	x	X	x		
BitsReceived	X	х	X	X	X	Х	X					X	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	x	X	x		
BitsSent	X	х	X	Х	X	Х	Х	X	X	Х	х	X	Х	Х	Х	Х	Х	X	Х	Х	X	Х	Х	Х	X	X	X	x	X	x		
PortCpuStatus							X			Х	Х							X						Х						Х		
PortCpuDodStatus							X			Х	Х							X						Х						х		

			Νo	rm	nal				Q	o s			Str	e a i	m T	rig	g e i	r	Мо	d e C	heck	(sun	ıErr	ors	М	o d e I	Data	Int	e g r i	ity	Ac	l d'- I
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PoSExtendedStats	
Type: Transmit Duration																																
TransmitDuration	х	Х		X	Х	Х	Х	Х	Х	Х	Х	X	X		х	X	х	X	X	X	X	X	X	X	x	X	x	X	X	X		
Type: Quality of Service																																
QualityOfService0								х	Х	Х	х																					
Type: Framer																																
FramerFCSErrors																																
FramerAbort																															X	
FramerMinLength																															X	

			Νo	rm	al				Q	0 S		;	Stı	e a	m 1	Γri	i g g	ı e r		Мо	d e C	heck	(sun	nErr	ors	Мс	d e E	ata	Int	egr	ity	A d	<b>d'-</b> 
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity		RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PoSExtendedStats	
FramerMaxLength																																Х	
Type: Checksum Stats																																	
IpPackets																				X					X								
UdpPackets																				X					Х								
TcpPackets																				X					Х								
IpChecksumErrors																				Х					Х								
UdpChecksumErrors																				X					Х								
TcpChecksumErrors																				X					Х								
Type: Data Integrity																																	
DataIntegrityFrames				X											X							X						Х					
DataIntegrityErrors				X											X	,						Х						х					

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PoSExtendedStats	
Type: Sequence Check-ing																																
SequenceFrames						X											X						X						X			
SequenceErrors						X											X						X						X			
Type: Ethernet																																
Fragments			X		X		X			X	X			X		X		X				X		X				X		X		
Undersize			Х		Х		X			X	X			Х		X		Х				х		X				Х		Х		
Oversize			Х		Х		X			X	X			Х		X		Х				х		Х				Х		Х		
VlanTaggedFramesRx			Х		Х		Х							Х		X						Х						х		x		

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PoSExtendedStats	
FlowControlFrames			Х		X		X			Х	X			Х		Х		Х				х						х		Х		
Type: 10/100																																
AlignmentErrors			Х				X							X																Х		
DribbleErrors			X				X			X	X			X				X						X						X		
Collisions			X				X			X	X			X				X						X						Х		
LateCollisions			X				X			X	X			X				X						X						X		
CollisionFrames			Х				X			X	X			X				X						x						Х		
Excess- iveCollisionFrames			Х				X			X	X			X				X						Х						X		

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	;	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PoSExtendedStats	
Type: Gigabit																																	
SymbolErrorFrames					X											X							X						X				
SynchErrorFrames					X											X							X						Х				
Type: 10/100 + Gigabit																																	
SymbolErrors					X											X							X						X				
OversizeAndCrcErrors					X		X			X	X					X		X					X		X				Х		Х		
Type: POS																																	
SectionLossOfSignal																																Х	
SectionLossOfFrame																																Х	

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PoSExtendedStats	
SectionBip																															Х	
LineAis																															Х	
LineRdi																															Х	
LineRei																															Х	
LineBip																															Х	
PathAis																															Х	
PathRdi																															Х	
PathRei																															Х	
PathBip																															Х	
PathLossOfPointer																															Х	
PathPlm																															Х	
SectionBipErroredSecs																																

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PoSExtendedStats	
Sec- tionBipSeverlyErroredS- ecs																																
Sec- tionLossOfSignalSecs																																
LineBipErroredSecs																																
LineReiErroredSecs																																
LineAisAlarmSecs																																
LineRdiUnavailableSecs																																
PathBipErroredSecs																																
PathReiErroredSecs																																
PathAisAlarmSecs																																
PathAisUnavailableSecs																																

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PoSExtendedStats	
PathRdiUnavailableSecs																																
InputSignalStrength																																
PosK1Byte																																
PosK2Byte																																
SrpDataFramesRe- ceived																																
SrpDis- coveryFramesReceived																																
SrpIpsFramesReceived																																
SrpParityErrors																																
SrpUsageFramesRe- ceived																																

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PoSExtendedStats	
SrpUsageStatus																																
SrpUsageTimeouts																																

### Statistics for OC48c Modules with BERT

#### Statistics for OC48c Modules with BERT

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			N	o r	m a	1					Qc	S				Sti	· e a	ım'	Γri	gg	er		Мс	ode (	C h e	cks	u m	Err	ors	M	o d e	Da	taI	nte	gri	ty	Į į	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PoSExtendedStats	
Type: User Configurable																																						
UserDefinedStat1	X	X	X	х	х	x	X	X							X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
UserDefinedStat2	X	X	X	х	х	x	х	X							X	X	X	Х	X	X	X	X		X	X	X	X			X	X	Х	X	Х	X	Х		
CaptureTrigger	X		X					X							X		X					X	X					X	X	X						Х		
CaptureFilter	X		X					X							X		X					X	Х						x	х						х		

			1	101	m	a I					Q	o s				Sti	r e a	a m	Tr	i g g	er		Мс	od e	C h e	cks	u m	Erro	ors	М	o d e	Da	taI	nte	gri	ty	Add'
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PoSExtendedStats
StreamTrigger1															X	X				X	x	X															
StreamTrigger2															X	X				X	x	X															
Type: States																																					
Link	X	X	X	X	X	X	X	X	X	х	X	x	х	X	х	X	X	x	x	X	X	X	х	X	X	X	X	X	X	X	X	X	X	X	X	X	
LineSpeed	X	X	X	X	X	X	X	X	X	х	x	x	x	х	X	X	X	х	x	Х	x	X	Х	Х	X	X	X	X	Х	Х	Х	Х	Х	Х	Х	Х	
DuplexMode			X		X			X			x			х			Х		x			X				X			X				X			X	

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PoSExtendedStats	
TransmitState	X	X	X	X	X	х	X	X	X	X	X	x	X	x	X	X	X	X	X	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
CaptureState	x	x	х	x	х	Х	X	X	X	X	X	х	х	x	x	X	x	X	X	X	x	X	X	X	X	X	X	X	X	X	Х	х	Х	Х	Х	X		
PauseState	х	х	Х	х	х	Х	X	X	X	X	X	х	х	X	X	X	X	X	X	X	x	X	Х	X	X	X	X	X	Х	X	Х	Х	Х	Х	Х	Х		
Type: Common																																						
FramesSent	X	x	X	x	X	X	X	X	X	X	X	X	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
FramesReceived	X	х	x	х	X	х	X	X	X	X	X	x	X	X	X	X	X	X	X	X	x	X	X	X	Х	Х	Х	X	x	X	x	x	x	x	x	x		

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PoSExtendedStats
BytesSent	х	X	Х	X	Х	X	Х	Х	х	Х	х	х	х	х	X	х	X	х	x	X	х	х	Х	Х	X	x	X	x	Х	X	Х	Х	Х	X	Х	x	
BytesReceived	х	Х	Х	X	X	X	X	X							X	х	X	х	X	X	x	х	X	X	X	X	X	X	X	Х	Х	Х	Х	Х	Х	X	
FcsErrors	х	X	Х	Х	Х	Х	X	Х	х	Х	x	х	х	х	х	х	X	Х	x	X	х	х	Х	Х	X	X	Х	X	X	Х	Х	Х	Х	Х	Х	X	
BitsReceived	х	X	Х	Х	х	X	X	х							x	x	X	X	x	X	x	х	Х	X	X	X	X	X	X	X	X	X	X	X	X	X	
BitsSent	х	X	X	X	X	X	X	X	x	X	х	x	х	x	X	х	X	x	х	X	x	Х	х	X	X	X	X	X	X	X	X	X	X	Х	X	X	
PortCpuStatus																							Х	X	Х		X		X	X	Х	Х		Х		Х	

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PoSExtendedStats	
	X	X		Х		Х		Х	Х	X	Х	Х		Х	Х	Х		Х		Х		Х																
PortCpuDodStatus	X	X		X		X		X	X	Х	Х	Х		X	Х	Х		X		X		Х	Х	X	X		X		X	X	X	X		X		X		
Type: Transmit Duration																																						
TransmitDuration	X	х		X	X	X	X	X	X	X	X	X	X	X	X	X		X	х	X	Х	х	X	x	X	X	x	X	x	x	X	X	x	x	x	x		
Type: Quality of Service																																						
QualityOfService0									X	x	x	x	X	X																								

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	distribution of the	KATCPROMINITION	KXDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PoSExtendedStats	
Type: Checksum Stats																																							
IpPackets																								X					X	X									
UdpPackets																								Χ					X	X									
TcpPackets																								Χ					X	X									
IpChecksumErrors																								Χ					X	X									
UdpChecksumErrors																								X					X	Х									
TcpChecksumErrors																								X					X	Х									
Type: Data Integrity																																							
DataIntegrityFrames				x														)	×							X							X						
DataIntegrityErrors				x															×							X							X						

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup		KxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PoSExtendedStats	
Type: Sequence Check- ing																																							
SequenceFrames						X						X								X								X							X				
SequenceErrors						Х						X								X								X							X				
Type: Ethernet																																							
Fragments			X		X			X			X			X			X		X			X					Х			X				X			X		
Undersize			X		X			X			X			X			X		x			X					X			Х				X			Х		
Oversize			X														Х										X			X				Х			X		

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RXTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	BxModeBert	RxModeWidePacketGroup	Capture		PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PoSExtendedStats	
					X			X			X			X					X			X																	
VlanTaggedFramesRx			X		х			х									X		X								X							Х			X		
FlowControlFrames			X		x			x			Х			x			X		X			X	(				Х							X			X		
Type: 10/100																																							
AlignmentErrors			X					X									X																				X		
DribbleErrors			X					х			Х			x			X					X								X							X		
Collisions			X														X													X							X		

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PoSExtendedStats	
								X			X			X								Х																
LateCollisions			X					X			X			Х			X					х							Х							Х		
CollisionFrames			Х					X			X			Х			X					х							Х							Х		
Excess- iveCollisionFrames			X					X			X			X			X					х							Х							Х		
Type: Gigabit																																						
SymbolErrorFrames					X														х							X							X					
SynchErrorFrames																										Х							Х					

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PoSExtendedStats	
					Х														Х																			
Type: 10/100 + Gig- abit																																						
SymbolErrors					X														X							X							X					
OversizeAndCrcErrors					x			х			х			х					X			X				X			x				X			X		
Type: POS																																						
SectionLossOfSignal																																					X	
SectionLossOfFrame																																					X	

			N	lor	m a	a I					Qd	s				Stı	r e a	a m	Tr	i g g	j e r		М	od e	C h e	cks	u m	Erro	ors	М	o d e	Da	taI	nte	gri	ty	A	d d ' - I
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PoSExtendedStats	
SectionBip																																					Х	
LineAis																																					X	
LineRdi																																					X	
LineRei																																					Х	
LineBip																																					X	
PathAis																																					X	
PathRdi																																					X	
PathRei																																					X	

			1	lor	m a	a I					Q	o s				St	rea	ı m	Tri	i g g	er	•	Мо	od e	C h e	cks	u m	Erro	ors	М	o d e	Da	taI	nte	gri	ty	A d	d'-
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PoSExtendedStats	
D. III D.																																					X	_
PathBip																																						
PathLossOfPointer																																					X	
PathPlm																																					Х	
SectionBipErroredSecs	X	х		X		X	Х		х	X		Х	X		X	х		Х		Х	X		Х	X	X		X	x		Х	Х	Х		Х	Х			
Sec- tionBipSeverlyErrored- Secs	X	x		х		X	x		x	X		x	X		X	х		х		х	X		Х	X	Х		Х	Х		х	х	х		Х	х			
Sec- tionLossOfSignalSecs	X	x		x		X	x		x	X		x	X		X	х		x		x	x		Х	Х	X		Х	X		x	x	x		x	x			

			N	or	m a	ı					Q	o s				Sti	r e a	m	Tr	i g g	er		Мс	de	Che	cks	u m	Erro	ors	М	o d e	Da	taI	nte	gri	ty	A d	ld'- I
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PoSExtendedStats	
LineBipErroredSecs	X	x		X		X	Х		X	Х		Х	X		X	х		х		X	x		X	Х	x		Х	Х		Х	Х	X		х	X			
LineReiErroredSecs	X	x		X		X	X		X	X		X	X		X	х		х		X	x		X	X	X		X	x		X	X	X		X	X			
LineAisAlarmSecs	X	x		X		X	Х		X	X		X	X		X	X		х		X	x		X	Х	X		Х	X		Х	Х	Х		Х	Х			
LineRdiUnavail- ableSecs	X	x		X		X	Х		X	X		X	X		X	х		х		X	x		Х	Х	X		Х	Х		X	Х	Х		Х	Х			
PathBipErroredSecs	X	x		X		X	Х		X	X		X	X		X	х		х		X	x		Х	Х	X		Х	Х		Х	Х	Х		Х	X			
PathReiErroredSecs																							Х	X	Х		X	X		Х	X	X		X	X			

			N	lor	m a	a I					Q	o s				St	r e a	m '	Tri	gg	er		Мс	od e	C h e	cks	u m	Erro	ors	М	o d e	Da	taI	nte	gri	ty	A	d d ' - I
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PoSExtendedStats	
	X	X		X		X	X		Х	X		Х	X		X	Х		X		X	X																	
PathAisAlarmSecs	X	x		X		x	x		х	X		х	x		Х	х		х		х	х		Х	X	X		Х	x		X	Х	X		х	Х			
PathAisUnavail- ableSecs	x	x		X		x	x		х	X		х	x		X	х		Х		Х	X		х	X	X		Х	x		X	Х	Х		х	Х			
PathRdiUnavail- ableSecs	X	х		X		х	х		X	X		х	х		X	х		X		Х	X		Х	X	X		X	X		X	X	X		Х	X			
InputSignalStrength																																						
PosK1Byte																																						
PosK2Byte																																						
SrpDataFramesRe-																																						

			N	or	m a	1					Q	) S				St	rea	a m	Tri	i g g	er		Мс	de	Che	cks	u m	Erro	ors	M	o d e	Da	taI	nte	gri	ty	A	d d ' - I
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PoSExtendedStats	
ceived																																						
SrpDis- cov- eryFramesReceived																																						
SrpIpsFramesRe- ceived																																						
SrpParityErrors																																						
SrpUsageFramesRe- ceived																																						
SrpUsageStatus																																						
SrpUsageTimeouts																																						

## Statistics for OC48c Modules with SRP and DCC

Statistics for OC48c Modules with SRP and DCC

		N	lor	m a	ıl			Q	0 S		S	tre	a m	Tri	g g e	r	Мо	d e C	heck	sum	Erre	ors	М	o d e l	Dat <i>a</i>	Int	e g r i	ty	Ad	d'I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
Type: User Configurable																														
UserDefinedStat1	X	X	X	X	X	X					Χ	Х	X	X	X	X	X	x	X	x	X	x	X	X	X	X	X	X		
UserDefinedStat2	X	Х	Х	X	X	Х					X	Х	Х	Х	Х	Х		x	X	x	Х		X	Х	Х	Х	Х	Х		
CaptureTrigger	X										Х						X					Х	Х					Х		
CaptureFilter	X										X						Х						X					Х		
StreamTrigger1											X	Х			Х	Х														
StreamTrigger2											X	Х			X	Х														
Type: States																														

		N	lor	m a	ıl			Q	o s		S	tre	a m	Tri	g g e	r	Мо	d e C	heck	sum	Erro	ors	М	o d e l	Data	Int	e g r i	ty	A d	d'I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
Link	Х	Х	Х	Х	Х	Х	Х	X	Х	Х	х	Х	Х	Х	Х	Х	х	х	x	Х	х	х	Х	Х	Х	Х	Х	Х		
LineSpeed	X	X	X	Х	Х	Х	Х	X	X	Х	Х	Х	X	X	Х	X	Х	х	x	X	x	Х	X	Х	X	X	X	Х		
DuplexMode				Х										X						X						X				
TransmitState	X	X	X	Х	Х	Х	Х	X	X	Х	Х	Х	X	X	X	X	х	x	x	X	Х	Х	X	Х	Х	X	Х	Х		
CaptureState	X	X	X	X	X	X	X	X	X	X	Х	Х	Х	X	X	Х	х	x	x	Х	х	Х	X	Х	Х	Х	Х	Х		
PauseState	X	X	X	X	X	Х	X	X	X	X	Х	Х	X	Х	Х	x	х	X	х	X	Х	X	X	X	X	X	X	Х		
Type: Common																														
FramesSent	X	Х	X	X	X	X	X	X	X	X	Х	X	X	X	X	X	X	X	Х	X	X	X	X	X	X	X	X	X		

	etGroup C C C C C C C C C C C C C C C C C C C							Q	o s		S	tre	a m	Tri	g g e	r	Мо	d e C	h e c k	su m	Erro	ors	М	o d e l	Data	Int	egri 	ty	Add	d'I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
FramesReceived	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	х	Х	Х	х	Х	Х	Х	х	х	x	x	x	X	Х	Х	Х	Х	Х		
BytesSent	X	X	X	X	Х	Х	X	X	Х	X	Х	Х	X	х	X	Х	Х	x	x	x	x	x	Х	Х	X	Х	Х	Х		
BytesReceived	X	X	X	X	Х	X					Х	Х	X	X	X	X	X	х	х	х	х	x	Х	X	X	Х	X	X		
FcsErrors	X	X	X	X	Х	X	X	Х	Х	X	Х	Х	X	X	Х	X	X	х	х	х	х	x	Х	X	X	Х	X	X		
BitsReceived	X	X	X	X	Х	X					Х	Х	X	X	X	X	X	Х	х	х	х	x	Х	X	X	Х	X	X		
BitsSent	X	X	X	X	Х	X	X	X	Х	X	Х	Х	X	х	X	Х	Х	x	x	x	x	x	Х	Х	Х	Х	Х	Х		
PortCpuStatus	X	X	X		X	X	X	Х	Х	X	Х	Х	X		X	Х	Х	х	Х		x	Х	Х	Х	X		X	Х		
PortCpuDodStatus	X	Х	X		Х	Х	X	Х	Х	Х	x	x	X		X	X	Х	Х	Х		Х	Х	x	X	x		x	X		

		N	lor	m a	ıl			Q	o s		S	Stre	a m	Tri	g g e	r	Мо	d e C	h e c k	sum	Erre	ors	М	o d e l	Data	Int	e g r i	ty	A d	d'I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
Type: Transmit Duration																														
TransmitDuration	X	X	X	X	X	X	X	X	X	X	X	x	X	x	X	X	X	x	X	x	X	x	x	X	X	X	X	X		
Type: Quality of Service																														
QualityOfService0							Х	X	X	X																				
Type: Checksum Stats																														
IpPackets																	Х					Х								
UdpPackets																	Х					Х								
TcpPackets																	Х					Х								
IpChecksumErrors																	Х					Х								
UdpChecksumErrors																	Х					Х								
TcpChecksumErrors																	Х					X								

		N	lor	m a	ı			Q	o s		S	tre	a m	Tri	g g e	r	Мо	d e C	h e c k	su m	Erro	ors	М	o d e l	Data	Int	e g r i	ty	Ad	d'I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
Type: Data Integrity																														
DataIntegrityFrames			X										X						X						X					
DataIntegrityErrors			Х										Х						x						X					
Type: Sequence Check-ing																														
SequenceFrames					X				Х						X						Х						Х			
SequenceErrors					X				Х						Х						Х						Х			
Type: Ethernet																														
Fragments				X										X						x						X				
Undersize				Х										X						Х						Х				

		N	lor	m a	ı			Q (	o s		S	tre	e a m	Tri	g g e	r	Мо	d e C	heck	sum	Err	ors	М	o d e l	Data	Int	e g r i	ty	A d	d'I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
Oversize				X										X						X						X				
VlanTaggedFramesRx				X										X						x						X				
FlowControlFrames				Х										х						x						Х				
Type: Gigabit																														
SymbolErrorFrames				X										X						x						X				
SynchErrorFrames				Х										Х						х						Х				
Type: 10/100 + Gigabit																														
SymbolErrors				X										x						X						X				

		N	lor	m a	ıl			Q	o s		S	tre	a m	Tri	g g e	r	Мо	d e C	h e c k	sum	Erre	ors	М	o d e l	Data	Int	e g r i	ty	A d	d'l
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
OversizeAndCrcErrors				Х										х						Х						Х				
Type: POS																														
SectionLossOfSignal																													X	
SectionLossOfFrame																													X	
SectionBip																													X	
LineAis																													X	
LineRdi																													X	
LineRei																													X	
LineBip																													X	
PathAis																													Х	
PathRdi																													Х	
PathRei																													X	

	Normal							Q	os		S	tre	a m	Tri	g g e	r	Мо	d e C	heck	su m	Err	ors	М	o d e l	Data	Int	egri	ty	A d	d'I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
PathBip																													Х	
PathLossOfPointer																													Х	
PathPlm																													Х	
SectionBipErroredSecs	X	X	X		X	X	X	Х	Х	Х	х	Х	Х		X	X	x	Х	Х		х	Х	Х	Х	Х		Х	Х		
Sec- tionBipSeverlyErroredSe- cs	X	Х	X		X	х	х	Х	X	х	Х	Х	X		X	Х	Х	Х	Х		Х	Х	X	X	x		x	x		
SectionLossOfSignalSecs	X	X	X		X	Х	Х	X	X	X	Х	Х	Х		X	X	Х	Х	х		х	Х	Х	Х	X		Х	Х		
LineBipErroredSecs	X	X	X		X	X	X	X	X	X	Х	Х	X		X	X	Х	Х	X		Х	Х	X	Х	Х		X	Х		
LineReiErroredSecs	X	X	X		X	X	X	X	X	X	Х	Х	X		X	X	Х	Х	X		Х	Х	X	Х	X		X	Х		
LineAisAlarmSecs	Х	Х	X		Х	Х	Х	Х	Х	Х	Х	Х	Х		Х	Х	Х	Х	Х		X	Х	X	Х	Х		Х	Х		

		rity our management of the control o						Q	0 S		S	tre	a m	Tri	g g e	r	Мо	d e C	h e c k	sum	Erro	ors	М	o d e l	Data	Int	e g r i	ty	A d	d'l
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
LineRdiUnavailableSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	x		
PathBipErroredSecs	X	X	X		Х	X	X	X	X	X	Х	Х	X		Х	х	x	x	х		х	х	Х	Х	X		X	X		
PathReiErroredSecs	Х	Х	Х		Х	Х	Х	Х	Х	Х	Х	Х	Х		Х	Х	x	x	x		x	x	X	Х	Х		X	Х		
PathAisAlarmSecs	Х	Х	Х		Х	Х	Х	X	X	X	Х	Х	Х		Х	х	x	x	x		x	x	Х	Х	Х		Х	Х		
PathAisUnavailableSecs	Х	Х	Х		Х	X	Х	X	Х	X	х	X	X		Х	Х	Х	Х	x		Х	х	Х	Х	X		Х	Х		
PathRdiUnavailableSecs	X	X	X		X	X	X	X	X	X	х	Х	X		Х	Х	Х	х	x		Х	Х	X	Х	X		Х	Х		
InputSignalStrength																														
PosK1Byte	X	Х	Х		Х	Х					Х	Х	Х		Х	Х							Х	Х	Х		Х	Х		

	Normal Gujy						Q	o s		S	tre	a m	Tri	g g e	r	Мо	deC	h e c k	sum	Err	ors	М	o d e I	Data	Int	e g r i	ty	A d	d'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
PosK2Byte	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		
SrpDataFramesReceived	X	X	X		X	X					X	X	X		X	X							X	X	х		X	X		
SrpDis- coveryFramesReceived	X	X	X		X	X					Х	Х	Х		Х	Х							Х	Х	X		Х	Х		
SrpIpsFramesReceived	X	X	X		X	X					Х	Х	X		Х	X							Х	Х	X		Х	Х		
SrpParityErrors	X	X	X		X	X					Х	Х	х		Х	X							Х	Х	X		Х	Х		
SrpUsageFramesRe- ceived	X	X	X		Х	X					Х	Х	X		Х	X							Х	Х	X		Х	Х		
SrpUsageStatus	X	Х	X		Х	Х					X	х	Х		х	X							Х	Х	Х		Х	х		

		N	lor	m a	ıI			Q	os		S	tre	a m	Tri	g g e	r	Мо	d e C	heck	sum	Err	ors	М	o d e I	Data	Int	egri	ty	A d	ld'I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
SrpUsageTimeouts	Х	Х	Х		Х	Х					Х	Х	х		х	Х							Х	Х	Х		Х	Х		
Type: DCC																														
DccBytesReceived						Х				X						X						X						Х		
DccBytesSent																														
DccCrcErrorsReceived						Х				X						Х						X						Х		
DccFramesReceived						Х				Χ						х						Х						Х		
DccFramesSent																														
DccFram- ingErrorsReceived																														

# **Statistics for OC48c Modules with RPR and DCC**

### Statistics for OC48c Modules with RPR and DCC

		1	lor	m a	1			Q	0 S						g g e			o d e C			Erro	ors	М	o d e	Data	Int	egri	ty	A d	d'I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
Type: User Configurable																														
UserDefinedStat1	X	X	X	X	X	X					Χ	X	X	X	X	X	x	X	X	x	X	X	x	X	X	X	x	X		
UserDefinedStat2	X	Х	Х	Х	Х	X					X	Х	х	х	Х	Х		Х	X	X	х		X	X	Х	X	Х	Х		
CaptureTrigger	X										X						X					X	Х					Х		
CaptureFilter	X										X						X						X					Х		
StreamTrigger1											X	Х			Х	Х														
StreamTrigger2											X	X			Х	Х														
Type: States																														

		N	lor	m a	I			Q	o s		9	Stre	a m	Tri	g g e	r	Мо	o d e C	h e c k	(sum	Erro	ors	М	o d e l	Data	Int	egri	ty	Add	'1
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
Link	X	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	х	x	х	х	x	x	х	х	х	Х	Х	х	Х		
LineSpeed	Х	Х	Х	Х	Х	Х	X	X	Х	Х	Х	X	Х	Х	X	Х	Х	x	x	х	x	x	Х	Х	X	Х	Х	X		
DuplexMode				Х										Х						х						Х				
TransmitState	X	Х	Х	Х	Х	X	Х	X	Х	Х	Х	X	Х	Х	X	Х	X	x	X	х	х	X	Х	X	X	Х	X	Х		
CaptureState	X	Х	Х	Х	Х	Х	Х	X	Х	Х	Х	X	Х	Х	X	Х	X	x	X	X	x	X	Х	X	X	Х	X	Х		
PauseState	X	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	X	X	x	X	х	X	x	X	x	x	X	Х	X	Х	X	X	Х		
Type: Common																														
FramesSent	X	X	X	X	X	Х	X	X	X	X	х	X	X	X	X	х	X	х	Х	х	х	X	X	X	X	X	X	X		

		1	Nor	m a	ı			Q	o s		S	Stre	a m	Tri	g g e	r	М	o d e C	heck	su m	Erro	ors	М	o d e	Data	Int	egri	ty	A d	d'l
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
FramesReceived	Х	Х	Х	Х	Х	Х	Х	Х	X	X	х	х	Х	х	Х	Х	x	x	х	x	x	x	X	Х	х	Х	Х	Х		
BytesSent	Х	Х	Х	Х	Х	Х	Х	Х	X	X	х	Х	X	Х	X	Х	х	х	Х	x	х	x	Х	Х	Х	Х	Х	X		
BytesReceived	Х	X	Х	Х	Х	X					х	X	X	х	X	X	x	х	x	х	х	x	X	Х	Х	Х	Х	X		
FcsErrors	Х	X	Х	Х	Х	X	Х	X	X	X	х	Х	X	Х	X	X	x	х	x	х	х	x	X	Х	Х	Х	Х	X		
BitsReceived	Х	Х	Х	Х	Х	Х					х	Х	X	Х	X	X	x	х	x	х	х	x	X	Х	Х	X	Х	Х		
BitsSent	Х	Х	Х	Х	Х	Х	Х	Х	X	X	х	Х	X	Х	X	X	x	х	х	x	х	x	X	Х	Х	X	Х	Х		
PortCpuStatus	X	X	Х		Х	X	Х	X	X	X	Х	Х	X		X	X	Х	X	x		x	x	X	X	X		X	X		
PortCpuDodStatus	X	Х	X		Х	Х	Х	Х	X	X	х	х	X		X	X	Х	X	Х		X	Х	X	Х	X		Х	Х		

		N	lor	m a	ıI			Q	o s		9	Stre	a m	Tri	g g e	r	М	o d e C	hecl	(sum	Erro	ors	М	o d e l	Data	Int	egri	ty	Add	d'l
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
Type: Transmit Duration																														
TransmitDuration	X	X	X	X	X	X	X	X	X	X	х	X	X	X	X	X	x	X	X	X	x	x	X	x	x	X	X	X		
Type: Quality of Service																														
QualityOfService0							Х	Х	Х	Х																				
Type: Checksum Stats																														
IpPackets																	Х					Х								
UdpPackets																	Х					Х								
TcpPackets																	Х					Х								
IpChecksumErrors																	Х					Х								
UdpChecksumErrors																	Х					X								
TcpChecksumErrors																	Х					Х								

		1	lor	m a	I			Qd	s		S	Stre	a m	Tri	g g e	r	Ма	d e C	h e c k	(sum	Erro	ors	М	o d e l	Data	Int	e g r i	ty	A d	d'l
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
Type: Data Integrity																														
DataIntegrityFrames			X										X						x						X					
DataIntegrityErrors			Х										X						х						Х					
Type: Sequence Checking																														
SequenceFrames					X				X						X						х						X			
SequenceErrors					X				X						Х						х						Х			
Type: Ethernet																														
Fragments				Х										х						х						X				
Undersize				X										Х						х						X				

		I	Noı	m a	ı I			Q	o s		9	Stre	e a m	Tri	g g e	r	Мс	o d e C	heck	su m	Erro	ors	М	o d e l	Data	Int	egri	ty	A d	d'I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
Oversize				Х										Х						x						Х				
VlanTaggedFramesRx				Х										Х						x						X				
FlowControlFrames				X										Х						х						X				
Type: Gigabit																														
SymbolErrorFrames				X										X						х						Х				
SynchErrorFrames				X										Х						x						X				
Type: 10/100 + Gigabit																														
SymbolErrors				X										X						x						X				
OversizeAndCrcErrors				X										Х						Х						X				

		N	lor	m a	ı			Q	o s		9	Str	e a m	Tri	g g e	r	Мс	d e C	h e c l	(sum	Erro	rs	М	o d e l	Data	Int	e g r i	ty	Ad	d'l
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
Type: POS																														
SectionLossOfSignal																													X	
SectionLossOfFrame																													Х	
SectionBip																													Х	
LineAis																													Х	
LineRdi																													Х	
LineRei																													Х	
LineBip																													Х	
PathAis																													Х	
PathRdi																													X	
PathRei																													Х	

		N	lor	m a	I			Q	o s		9	Stre	e a m	Tri	gge 	r	Мс	d e C	heck	su m	Erro	ors	М	o d e l	Data	Int	egri	ty	A d	d'I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
PathBip																													Х	
PathLossOfPointer																													Х	
PathPlm																													Х	
SectionBipErroredSecs	Х	Х	Х		Х	Х	Х	X	X	Х	х	Х	X		X	X	Х	x	Х		x	x	X	х	Х		Х	Х		
Sec- tionBipSeverlyErroredSec- s	х	X	X		X	Х	Х	X	X	Х	Х	Х	X		X	Х	х	х	Х		Х	Х	X	Х	X		Х	Х		
SectionLossOfSignalSecs	X	Х	Х		Х	Х	Х	X	X	Х	Х	X	X		X	X	Х	x	x		x	x	X	Х	Х		Х	Х		
LineBipErroredSecs	X	Х	Х		X	X	X	X	X	X	Х	X	X		X	X	X	х	X		Х	X	X	Х	Х		Х	Х		
LineReiErroredSecs	X	Х	Х		X	X	X	X	X	Х	Х	X	X		X	X	X	х	X		Х	X	X	Х	Х		Х	X		
LineAisAlarmSecs	Х	X	X		Х	X	Х	X	X	X	Х	X	Х		Х	X	Х	Х	Х		Х	Х	X	Х	X		Х	Х		

		N	lor	m a	I			Q	o s		9	Str	e a m	Tri	g g e	r	М	o d e C	h e c l	(sum	Erro	ors	М	o d e l	Data	Int	egri	ty	A d	d'I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
LineRdiUnavailableSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
PathBipErroredSecs	X	X	X		X	X	X	X	X	X	X	Х	X		x	X	х	X	X		X	х	X	X	X		X	X		
PathReiErroredSecs	X	Х	Х		Х	Х	Х	Х	X	X	Х	х	X		х	X	x	x	x		х	x	X	Х	X		Х	X		
PathAisAlarmSecs	X	Х	Х		Х	Х	Х	Х	X	X	Х	X	Х		х	Х	х	Х	Х		Х	х	X	Х	Х		Х	Х		
PathAisUnavailableSecs	X	Х	Х		Х	X	Х	Х	X	Х	Х	Х	Х		х	Х	x	Х	Х		Х	х	Х	Х	Х		Х	Х		
PathRdiUnavailableSecs	X	Х	X		X	X	X	X	X	X	Х	х	Х		Х	X	х	х	Х		Х	Х	Х	X	Х		Х	Х		
InputSignalStrength																														
PosK1Byte																														

		N	lor	m a	I			Q	o s		9	Stre	e a m	Tri	g g e	r	Мс	o d e C	h e c l	su m	Erro	rs	М	o d e l	Data 	Int	e g r i	ty	A d	ld'l
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
PosK2Byte																														
SrpDataFramesReceived																														
SrpDis- coveryFramesReceived																														
SrpIpsFramesReceived																														
SrpParityErrors																														
SrpUsageFramesReceived																														
SrpUsageStatus																														
SrpUsageTimeouts																														
Type: DCC																														
DccBytesReceived						Х				X						х						X						X		

		1	lor	m a	I			Q	o s		9	Stre	a m	Tri	g g e	r	Мо	d e C	h e c k	(sum	Erro	ors	М	o d e l	Data	Int	egri	ty	A d	d'I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
DccBytesSent																														
DccCrcErrorsReceived						X				X						X						X						X		
DccFramesReceived						X				X						X						X						X		
DccFramesSent																														
DccFram- ingErrorsReceived																														
Type: RPR																														
RprDis- coveryFramesReceived	X	X	X		X	X					Х	Х	Х		х	x							X	Х	X		X	X		
RprDataFramesReceived	X	Х	X		Х	X					Х	Х	X		х	х							X	X	Х		X	X		
RprFair- nessFramesReceived	X	X	X		X	X					х	Х	Х		Х	Х							X	X	X		X	Х		

		N	lor	m a	I			Q	0 S		9	Stre	a m	Tri	g g e	r	Мо	o d e C	heck	(sum	Erro	ors	М	o d e	Data	Int	egri	ty	Add	'1
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PoSExtendedStats	
RprFairnessFramesSent	Х	Х	Х		Х	Х					х	Х	Х		Х	х							Х	Х	Х		Х	Х		
RprFairnessTimeouts	X	Х	X		Х	Х					х	X	X		Х	х							Х	Х	X		Х	Х		
RprHeaderCrcErrors	X	Х	Х		Х	Х					Х	X	X		X	х							X	X	X		X	X		
RprOamFramesReceived	X	X	X		X	X					Х	X	X		X	х							X	X	X		X	X		
RprPayloadCrcErrors	X	Х	Х		X	X					Х	X	X		X	х							X	X	X		X	X		
RprPro- tectionFramesReceived	X	X	X		X	Х					x	X	X		X	x							X	X	X		X	Х		

## **Statistics for 2.5G MSM POS modules**

#### Statistics for 2.5G MSM POS modules

			ı	N o I	r m	al							Qos						tre							uı	N		eCl 1Er				M	o d	e E	at	a I	n t	e g	rit	y		d d - ' I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	KXModeDcc	Canture	DacketGroup	RxDataIntegrity	By Eiret Time Stamp	RySequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: User Configurable								I			I				I																												
UserDefinedStat1	X	x	X	X	X		X	X	x	x	X .	x	X			>	( x	×	X	X	×		X	X	X	X	X	X	X	X		X	X	x	x	X	x	X	X	Х	X		
UserDefinedStat2	X	X	x	x	X		X	X	X	x	X	x	X			>	< ×	×	X	X	×		X	X	X				X				X	x	X	х	x	х	х	х	x		
CaptureTrigger	X	X	X		X				X	X	X	X	X			>	< ×	×	×		X				X	x						х	X	x	X		x				x		
CaptureFilter	X	X	X		X				X	X	X	X	X			>	< ×	×	×		×				X	х							X	х	X		х				X		

				Νo	r m	al						C	Q o s	S				s	tro	e a i	m T	ri	g g	er						he roi				Мо	d e	D a	ta	In	te	gri	ty	A	\ d d - ' l
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	kxmodeBertChannellzed	RxModeDcc	KXModeWidePacketGroup	Capture	PacketGroup	Deciretimestamo	RXSequenceChecking	RxModeBert	Porilogoustation	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Canturo	Capture	PacketGroup	DVEiretTimoStamn	December	RyModeBert		ExmodebertChannelized	PyModeWideDarketGroup	PoSExtendedStats	TemperatureSensorsStats
StreamTrigger1	X	x	X		X				x x	<b>x</b> 2	<b>x</b> 2	<b>x</b> 2	X				x 2	< >	<b>(</b> )	(	X		×	X	X								>	( )	< >	<	>	(			×	(	
StreamTrigger2	X	x	X		X				x x	<b>x</b> 2	x z	X I	x				x   2	< >	< ×	(	X		×	X	X								>	( )	< >	<	>	(			×	(	
Type: States																																											
Link	X	x	X	x	X	X	X	X	x x	<b>x</b> 2	<b>x</b> 2	<b>x</b>	x z	X	< 2	x 2	x 2	< >	<b>(</b> )	×	X	X	×	X	X	X	X	X	X	X	X	X	>	( )	< >	( x	( )	< ×	( )	<b>(</b> )	( x	(	
LineSpeed	X	X	X	x	X	x	x	X	× x	<b>x</b>	x 2	X :	x x	X	< 2	x 2	x 2	< >	< ×	×	X	X	×	X	X	X	X	X	X	X	X	X	>	( )	<b>(</b> )	< ×	<b>(</b> )	( X	( )	<b>(</b> >	( ×	(	
DuplexMode				x																×	(								X							×							

				Νo	rm	n a l							Q٥	S					St	re	a m	۱Tı	rig	g	er					e C I n E r				M	l o d	l e [	Dat	a I	n t	e g	rit	У	A c	d d - I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
CaptureState	X	x	x	x	x	X	X	X	X	X	X	X	X	X	X	X	x	x	X	X	X	X	x	X	X	X	X	x	X	X	X	X	X	X	x	x	X	x	x	x	X	x		
PauseState	X	X	X	х	х	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	Х	X	x	x	X	X	Х	X	X	Х	X	х	X	X	х	X	X	X	X	X	X		
Type: Common																																												
FramesSent	X	X	x	x	x		X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X		X	X	X				X			X	x	X	x	X	X	X	X	X	X		
FramesReceived	X	X	x	x	x		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X				X			X	X	X	x	X	X	X	X	X	X		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity		RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	KxDataIntegrity	RXFirstTimeStamp DySoguenceChacking	washing a second	KXModeBert	EXMODE BETCH BINE IIZED	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity		KXFIFSUIIMESTAMP	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
BytesSent	x	х	X	x	X		X	x	x x	<b>x</b>	<b>x</b>	x	X .	X	X	X	x	X	x >	x >	x >	(	>	< ×	×				>	<			X	Х	X	X	X	X	х	X	x	х		
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FcsErrors	X	Х	X	x	X		X	X	x x	<b>x</b>	<b>x</b>	x	X	X	X	X I	x	X	x >	x x	× >	(	>	< ×	×	X	X	X		<	X		Х	X	X	X	X	X	х	x	х	Х		
BitsReceived	X	X	X	x	X		X	X	x									X	x x	x >	× >	(	>	< ×	×	X	X	X		<	X		Х	X	X	X	X	X	X	X	x	Х		
BitsSent	X	Х	X	X	X		X	X	x x	<b>x</b>	X Z	x	X :	X	X	X	x	X	x x	x x	× >	(	>	< ×	( x	X	X	X		Κ	X		х	X	X	x	X	X	х	х	х	х		
PortCpuStatus																										Х	Х	X	,		X		Х											

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Type: Transmit Duration																																												
TransmitDuration	X	X	X	x	Х		X	X	x	x	X	х	х	x	X	X	X	x	X	х	х	х		x	x	X	Х	Х	Х	X	X		X	X	: ×	( ×	X	X	X	X	Х	Х		
Type: Quality of Service																																												
QualityOfService0										X	X	X	X	X	X	X	X																											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: Checksum Stats																																												
IpPackets																											X	Х	Х		Х		Х											
UdpPackets																											Х	X	Х		Х		Х											
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IpChecksumErrors																											X	Χ	Х		Х		Х											
UdpChecksumErrors																										7	Х	X	Х		Х		Х											
TcpChecksumErrors																											X	Χ	Х		Х		Х											
Type: Data Integrity																																												
DataIntegrityFrames			X									X								x																x								
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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	Canture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: Sequence Check-ing																																											
SequenceFrames					X							X									X																X						
SequenceErrors					X							Х									X																X						
Type: Ethernet																																											
Fragments				X			x						x	x						x			x						X							X		X	X				
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VlanTaggedFramesRx				X			X						X	×	(					X			X						Х							x		x	x				
FlowControlFrames				X			X						X	×	(					X			X						Х							x		x	X				
Type: Gigabit																																											
SymbolErrorFrames				X																X									X							X							
SynchErrorFrames				X																X									Х							X							

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RyDataInfority	RyEirstTimeStamn	The second secon	KXSequence Checking	NAME OF THE PARTY	KxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: 10/100 + Gigabit																																													
SymbolErrors				X																	X									х							X								
OversizeAndCrcErrors				x			X							X	X						X			x						X							X		>		×				
Type: POS																																													
SectionLossOfSignal						X																	X									X												X	
SectionLossOfFrame																																												X	
SectionBip																																												X	

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
LineAis																																											X	
LineRdi																																											X	
LineRei																																											X	
LineBip																																											X	
PathAis																																											X	
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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSeauenceCheckina	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
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PathLossOfPointer																																												
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SectionBipErroredSecs																X																	X										X	
Sec- tionBipSeverlyErroredS- ecs																x																	X										х	
Sec- tionLossOfSignalSecs																x																	X										X	
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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	DacketCroms	Packeteroup	KXDataIntegrity	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
LineReiErroredSecs															X																	X										X	
LineAisAlarmSecs															X																	Х										X	
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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	NAME OF THE OWNER OWNER OF THE OWNER	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
PathAisAlarmSecs																X																	X										X	
PathAisUnavailableSecs																X																	Х										Х	
PathRdiUnavailableSecs																X																	X										X	
InputSignalStrength							x	X						X	x									x	x														X	X	x			
PosK1Byte	x	x	x		X				x	X	X	X	X				X	x	X	X		x				X								X	x	Х		X				х		
PosK2Byte																																												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Canture		Packeteroup	kxDataillegiltý	KXFIFSUIMEStamp	KxSequenceChecking	KxModeBert	RxModeBertChannelized	RxModeDcc	kxmodewidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
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SrpDataFramesRe- ceived	X	x	X		x				X	X	x	X	x				X	X	X	X		X				X								×	· >	<b>( )</b>	(		×			>	×		
SrpDis- coveryFramesReceived	X	X	X		x				x	X	x	X	X				X	X	x	X		X				X								X	: >	<b>( )</b>	(		X			>	×		
SrpIpsFramesReceived	X	x	X		x				X	X	x	X	x				X	X	x	x		X				X								×	· >	<b>(</b> )	(		×			>	×		
SrpParityErrors	X	X	x		x				x	x	x	X	X				X	X	x	X		X				X								X	: >	<b>( )</b>	(		X			>	×		
SrpUsageFramesRe- ceived	X	X	X		X				X	X	x	X	X				X	X	X	X		X				X								X	· >	<b>( )</b>	(	,	X			>	×		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
SrpUsageStatus	X	X	X		X				X	X	X	X	X				X	X	X	X		х				X								X	X	X		X				X		
SrpUsageTimeouts	X	X	X		Х				X	X	X	X	Х				X	X	X	Х		Х				X								X	X	X		X				X	,	
Type: DCC																																												
DccBytesReceived								X								X									X								X								X			
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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
DccFramesReceived								X								x									X								X								X			
DccFramesSent																																												
DccFram- ingErrorsReceived																																												
Type: BERT																																												
BertStatus						X																	X									X												
BertBitsSent						X																	x									х												
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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	on the contract of	DacketGroup	RxDataIntegrity	1.50	RxSequenceChecking	100000000000000000000000000000000000000	RXModeBert By ModeBert Channelized	Rymodebertenamenzed	RxModeWidePacketGroup	Capture	PacketGroup	KXDdtaIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
BertBitErrorsSent						X																	>	<								x												
BertBitErrorsReceived						X																	>	<								X												
BertErroredBlocks						X																	>	<								X												
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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	DarketGroup	RxDataIntegrity	PyFirstTimeStamn	RxSequenceChecking	RxModeBert		RXModeBertChannelized BxModeDcc	RxModeWidePacketGroup	Capture	Darkotorom	declaration	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
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BertAvailableSeconds						X																	X										X												
Ber- tUnavailableSeconds						Х																	x										х												
BertBlockErrorState						Х																	x										Х												
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BertBitErrorRatio						х																	X										X												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Ber- tErroredSecondRatio						X																	X									X												
Ber- tSeverlyErroredSe- condRatio						X																	X									X												
Ber- tBack- groundBlockErrorRatio						X																	X									X												
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Ber- tMismatchedOnesRatio						x																	X									X												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Ber- tNum- berMismatchedZeros						X																	X								Γ	X												
Ber- tMismatchedZerosRatio						х																	Х									X												
BertElapsedTestTime						x																	X									X												
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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
BertDeskewPatternLock																																												
Ber- tRxDeskewErroredFram- es																																												
Ber- tRxDeskewEr- rorFreeFrames																																												
Ber- tRxDeskewLossOfFram- e																																												
BertTimeSinceLastError																																												
BertTriggerCount																																												
BertTxDeskewBitErrors																																												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Ber- tTxDeskewErroredFram- es							Ī							Ī	Ī					Ī																								
Ber- tTxDeskewEr- rorFreeFrames																																												
Type: Service Dis- ruption																																												
Ber- tLastSer- viceDisruptionTime						X																	x									x												
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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	PyModeBort	Namous de la company de la com	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
viceDisruptionTime																														П															
Ber- tSer- viceDisruptionCumulative	e					X																	X									×	(												
Type: OC192 - Temperature																																													
DMATemperature																																													Х
CaptureTemperature																																													Х
LatencyTemperature																																													Х
Back- groundTemperature																																													X

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	DyModeller	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
OverlayTemperature																																												X
FrontEndTemperature																																												X
SchedulerTemperature																																												
PlmDevice1In- ternalTemperature																																												
PlmDevice2In- ternalTemperature																																												
PlmDevice3In- ternalTemperature																																												
FobPort1Fp- gaTemperature																																												
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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Cantiure	PacketGroup	document	KxDataIntegrity	KxFirstTimeStamp	RxSequenceChecking	KxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
FobBoardTemperature																																													
FobDevice1In- ternalTemperature																																													
Type: 10 Gig																																													
PauseAcknowledge							X							x	X									X																<b>x</b>	x				
PauseEndFrames							X							x	X									X															)	<b>x</b>	x				
PauseOverwrite							X							X	X									X																<b>x</b>	x				
10GigLanTxFp- gaTemperature																																													

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Cantiire	on Otto Contract	racheteroup	exparaintegrity	Wer in section of	RxSequenceCnecking	) ladapoeta	KxModeBertChannelized	KXModeDcc ByModeWideBacketCroup	KXModeWidePacketsToup	PosExtendedStats	TemperatureSensorsStats
10GigLanRxFp- gaTemperature																																													
Cod- ingEr- rorFramesReceived																																													
EEr- rorChar- acterFramesReceived																																													
DroppedFrames																																													
Type: Link Fault Sig- naling																																													
LinkFaultState							X								X									X																	x				
LocalFaults							x								X									Х																	X				

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	KXModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
RemoteFaults							X								X									X																X				
Type: RPR																																												
RprDis- coveryFramesReceived								X																	X																X			
RprDataFramesRe- ceived								X																	x																X			
RprFair- nessFramesReceived								X																	x																Х			
RprFairnessFramesSent								х																	X																X			

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
RprFairnessTimeouts								X																	X																X			
RprHeaderCrcErrors								X																	x																X			
RprOamFramesRe- ceived								x																	x																X			
RprPayloadCrcErrors								X																	x																X			
RprPro- tectionFramesReceived								x																	X																x			

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## Statistics for OC192c Modules with BERT

## Statistics for OC192c Modules with BERT

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	Capture		Do Top Dought in	exicproduiding	KXDatamtegrity	KXFIrstlimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeWideDacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	KxModeBert	RxModeBertChannelized	RxModeDcc RxModeWideDacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: User Configurable																						I																								
UserDefinedStat1	X	( <b>X</b>	( <b>X</b>	( >	( )	x 2	x 2	<b>x</b> 2	x >	×									X	x	x	X	X	x z	<b>X</b>	X Z	×	x	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X		
UserDefinedStat2	X	( <b>&gt;</b>	×	<b>( )</b>	< >	× >	x :	<b>x</b> :	×	×									X	X	x	X	X	x :	X :	X X	××	(	X	X	X	X				X	×	X	X	x	x	x	X	X		
CaptureTrigger	X		<b>×</b>	(															X		x							X					X	X	X	X							X			
CaptureFilter	×		×	(															X		x							X							X	X							X			

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	Capture	n.c., Jest Caron	Packeteroup	rxicproduiditip	KXDatailitegrity	KxFirstTimeStamp	KxSequenceChecking	RxModeBert	RxModeBertChannelized	RXModeDcc RxModeWideDacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	KX I CpRound I rip	exparaintegrity  DyfiretTimeStamp	RXSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
StreamTrigger1																			X	x			X	X	X	X	x																			
StreamTrigger2																			X	x			X	X	X	X	X																			
Type: States																																														
Link	X	>	( ×	( >	( )	<b>x</b> >	<b>x</b> 2	x x	×	×	X	X	X	X	X	X	X	X	X	x x	< >	×	< X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
LineSpeed	X	×	( ×	( >	< >	× >	<b>x</b> 2	x x	××	×	X	x	X	X	x	X	X	x	X	x x	<b>( )</b>	×	( x	X	X	X	x	Х	Х	х	х	X	X	X	X	x	x	x	x	x	x	x	x	x		
DuplexMode			×	(	)	X							X							)	<	<b>&gt;</b>	<								Х				X				X							

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	Capture	PacketGroup	RXTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	PyEirchTimeStamn	dimensional to the second	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats TemperatureSensorsStats
TransmitState	X	х	X	X	X	X	x	x	X	X	x	x	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X	X	X	X		X	X	X	x	x	X	x	X	X	X	х	х	X	
CaptureState	X	х	x	X	X	X	x	x	X	X	x	X	X	X	X	X	x	x	X	х	х	X	X	X	X	X	x >	X	X	×	X	(	X	X	X	Х	x	Х	x	X	x	X	x	X	x	
PauseState	X	х	x	X	X	X	X	x	X	X	x	X	X	X	X	Х	X	х	X	х	х	X	X	X	X	X	x >	X	X	X	×	(	X	X	X	Х	X	x	X	X	x	X	х	X	x	
Type: Common																																														
FramesSent	X	х	X	X	X	X	x	X	X	X	x	X	X	X	X	X	X	X	X	X	Х	X	X	X	X	X	x >	X	X	X	X		X	X	X	х	x	X	x	X	X	X	X	X	X	
FramesReceived	X	Х	X	X	X	X	X	х	Х	Х	X	X	X	X	х	Х	X	X	X	Х	Х	X	X	X	X	X	x >	×	X	X	×		X	X	X	Х	X	X	X	X	X	X	х	X	X	

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	Packeteroup	KXFIrstIImeStamp	rxsequencecinecking	DVM odebertChannelized	RXModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RXTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RXSequenceChecking	RxModeBert	RxModeBertChannelized		RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
BytesSent	X	x	X	X	X	X	X	X	X	x >	< ×	<b>(</b> >	<b>(</b> >	( <b>&gt;</b>	×	X	X	X	x	x	x	X	x	X	x	X	x	x	Х	X	Х	x	X	x	X	X	X	X	X	X	X	x	x	x		
BytesReceived	X	x	x	X	X	X	X	X	X	X								X	X	x	X	X	X	X	X	X	X	X	X	X	Х	х	X	X	X	X	X	X	X	X	X	х	x	х		
FcsErrors	X	X	X	X	X	X	X	X	X	x >	< ×	<b>( &gt;</b>	< >	<b>(</b> >	×	X	X	X	X	X	x	X	X	X	x	X	X	X	X	X	Х	X	X	X	X	X	x	X	X	x	X	х	х	х		
BitsReceived	X	x	x	X	X	X	X	X	X :	X								X	X	X	X	X	X	X	x	X	x	X	X	X	X	x	X	X	X	X	X	X	X	X	X	x	X	х		
BitsSent	X	X	X	X	X	X	X	X	X :	X	< ×	<b>( )</b>	< >	< >	×	X	X	X	X	X	X	X	X	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PortCpuStatus																												X	X	X		Х		X	X											

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Ry Mode Bert Channelized	Rywode Der	RxModeWidePacketGroup	Capture	PacketGroun	RxTcpRoundTrip	RyDataIntegrity	DefigetTimeStamp	RXFIRSTIIMEStamp PySequenceChecking	Para de porte de la constante	KAMOdebert	KXModeBertChannelized	RXModeDcc ByModeWideDacketGroup	Capture	PacketGroup	RyDataIntenrity	A Company	KXFIrstIImestamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	· · · · · · · · · · · · · · · · · · ·		PacketGroup	KXDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
	X	Х		X		Х			X	X	Χ	Χ	Χ	Х			X	X	X	X		X	(	×	(		>	×	(									>	( )	( )	X		X			X	Х		
PortCpuDodStatus	X	X		X		X			X	X	X	X	X	X			×	X	X	X	,	×	(	×	(		>	< ×	X	X	×	(		X		X	X	>	( )	< 2	x		X			X	X		
Type: Transmit Duration																																																	
TransmitDuration	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	×	X	X	X		×	( <b>&gt;</b>	×	<b>(</b> >	<b>(</b> )	× >	×	X	X	×	( )	×	X	X	X	X	>	( )	<b>(</b>   )	x	x	X	X	X	X	X		
Type: Quality of Service																																																	
QualityOfService0											X	X	X	x	X	X	×	X																															
Type: Checksum																																																	

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	PyFirstTimeStamn	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	ByModeDcc	DyModeWideBacketCroun	do la	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Stats																																																
IpPackets																													X					X	X	:   <b>&gt;</b>	(											
UdpPackets																													X					X	X	<b>&gt;</b>	(											
TcpPackets																													X					X	X	· >	(											
IpChecksumErrors																													X					X	X	· >												
UdpChecksumErrors																													X					X	X	· >	(											
TcpChecksumErrors																													X					X	X	· >	(											
Type: Data Integrity																																																

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RXTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Canture		PacketGroup	KxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
DataIntegrityFrames				x																		X									x									×								
DataIntegrityErrors				х																		х									Х									x								
Type: Sequence Checking																																																
SequenceFrames						X								X										X									X									X						
SequenceErrors						X								X										X									X									x						
Type: Ethernet																																																
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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RXTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	DefiretTimoCtamn	KAFIISCHIIIIESCAIIID	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	The state of the s	Posextendedstats	TemperatureSensorsStats
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VlanTaggedFramesR- x			X		X																X		X									<b>&gt;</b>	(								X								
FlowControlFrames			x		X								X								X		X									>	(								X								
Type: 10/100									+																																								
AlignmentErrors																																																	

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamn	RxSequenceChecking	RxModeBert	DovilonmentChangelized	RxModeDcc	RxModeWidePacketGroup	Doctor and a feature	Posextendedstats	TemperatureSensorsStats
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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	Kasequencechecking	KAMOdebert	RxModeBertChannelized	RxModeDcc	KxModeWidePacketGroup	Capture	Packeteroup	RxDataIntegrity	RyEirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: Gigabit																																														
SymbolErrorFrames					X																	X	(								X								Х							
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Type: 10/100 + Gig- abit																																														
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Type: POS																																															
SectionLossOfSignal																																														X	
SectionLossOfFrame																																														Х	
SectionBip																																														Х	
LineAis																																														Х	
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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	kxsequencecnecking	KXModeBert	RxModeBertChannelized	KXModeDcc	KXM ode Wide Packet Group	Capture	PacketGroup	Exicprounding	by Figure 11 in Street	RxSequenceChecking	ByModeBert	RyModeBertChannelized	Rymodebertciiaiiieiized	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RyModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
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PathRdi																																													Х	
PathRei																																													Х	
PathBip																																													X	
PathLossOfPointer																																													X	
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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	DackotGroun	RyDataIntegrity	on the state of th	KXFIISUIIIIIESIAIIIIP	KxsequenceCnecking	RxModeBert	KxModeBertChannelized	PyModeWideDacketGroup	The state of the s	Posexientedatas	Iemperaturesensorsstats
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Sec- tionLossOfSignalSecs									x								X										x		x	X	X		X	X	X									>	(			
LineBipErroredSecs									X								X										X		X	X	X		х	X	X									>	<			
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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	DacketCroun	Facheteroup	RXFirstTimeStamp PySognopcoChocking	PyModeBert	RyMode BertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RXTcpRoundTrip	RxDataIntegrity	RyFirstTimeStamn	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
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PathBipErroredSecs									x							X										X		x	X	X		X	X	Х									X			
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PathAisAlarmSecs									X							X	,									X		x	X	X		X	X	х									х			
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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	KXModeWidePacketGroup	Capture	PacketGroup	KXFIrstIImeStamp	KXSequenceChecking	KXModebert	EXMODEBERTCHANNELLZED	De Mode Wide Backet Crous	Cantiire	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamn	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	DarketGroup	Por Data Introduity	exparamegins)	KXFIIFSUIIMESTAMP	RxSequenceChecking	KxModeBert	RXModeBertChannelized DVModeDcr	DVM ode Wide Darket Crosses	KXModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
InputSignalStrength	X	X		X		x	X	X		<b>x</b> 2	x >	X	>	<b>&lt;</b>  >	()	<	×	< x	X		X	,	X	X	X		x									×	×	( )	(		× >	<b>x</b>   2	<	>	<b>x</b>		
PosK1Byte																																															
PosK2Byte																																															
SrpDataFramesRe- ceived																																															
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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	PyFirstTimeStamn	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
SrpUsageFramesRe- ceived										Ī					Ī																																
SrpUsageStatus																																															
SrpUsageTimeouts																																															
Type: DCC																																															
DccBytesReceived									X								X										X								Х									X			
DccBytesSent																																															
DccCr- cErrorsReceived									X								X										X								x									X			
DccFramesReceived									X								x										X								x									X			

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamn	PySomioncoChocking	DVM odeBert	Down odo Bost Change Live	PvModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	By Mode Bert Channelized	PyModeDcc	RxModeWidePacketGroup	Capture	DacketGroun	Packetoloup	RyDataIntegrity	DefiretTimeStamp	RXFITSTIIMEStamp RXSequenceChecking	ByModeBert	Dymodebert Dymodebert	by Mode Derichannenzed	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	KXModeDCC	KXModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
DccFramesSent																																															
DccFram- ingErrorsReceived																																															
Type: OC192 - Temperature																																															
DMATemperature																																															Х
CaptureTemperature																																															Х
LatencyTemperature																																															X
Back- groundTemperature																																															
OverlayTemperature																																															X

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	BxModeDcc	DyWodeWideBacketGroup	www.decachedon	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
FrontEndTem- perature															Ī		Ī					Ī																										Х
Sched- ulerTemperature																																																X
PlmDevice1In- ternalTemperature																																																X
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FobPort1Fp- gaTemperature																																																X
FobPort2Fp- gaTemperature																																																
FobBoardTem-																																																X

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	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	KXModeBertChannelized	RXModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RyModeBert	KXModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
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FobDevice1In- ternalTemperature																																													X

## Statistics for OC192c Modules with SRP and DCC

## Statistics for OC192c Modules with SRP and DCC

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert		RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	<b>TemperatureSensorsStats</b>
Type: User Configurable																																					
UserDefinedStat1	x	X	X	X	X	X	X	X					X	X	x	X	X	X		x	X	X	X	x	x	X	X	X	X	X	X	X	X	X	X		
UserDefinedStat2	x	х	х	x	x	х	Х	х					X	x	х	X	x	X		X	x		Х	X	x	x		X	X	X	X	X	X	X	Х		
CaptureTrigger	x												X									x					x	X						X			
CaptureFilter	x												X									X						X						X			

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
StreamTrigger1													X	X			X	x	x	x																
StreamTrigger2													X	X			X	X	x	X																
Type: States																																				
Link	x	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	x	x	X	X	X	x	X	X	X	X	X	X	X	X	X		
LineSpeed	x	X	x	x	x	x	X	x	X	x	x	x	X	Х	X	X	X	x	x	x	x	x	X	X	х	X	Х	х	X	х	Х	X	X	X		
DuplexMode				X												X								X						X						

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
TransmitState	X	X	X	X	X	X	X	X	X	X	x	X	X	X	x	X	x	x	x	X	X	X	x	X	X	X	X	X	X	X	X	X	X	X		
CaptureState	X	х	х	X	X	X	X	х	X	X	X	X	X	X	X	X	x	X	x	X	x	x	x	x	x	x	X	X	X	X	X	X	X	X		
PauseState	X	х	х	х	X	x	x	х	х	х	x	x	x	x	х	х	X	X	X	X	X	X	x	X	X	X	Х	х	х	X	X	X	X	Х		
Type: Common																																				
FramesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	x	x	x	X	x	x	X	x	X	X	X	X	X	X	X	X	X		
FramesReceived	x	X	х	x	х	x	x	X	X	X	x	x	x	x	x	x	x	x	x	x	Х	x	Х	x	Х	x	х	Х	Х	X	X	X	X	X		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
BytesSent	X	x	x	x	x	X	X	x	X	X	x	x	X	x	x	x	X	X	x	X	x	X	X	X	X	X	X	X	X	X	X	X	x	X		
BytesReceived	X	X	x	X	x	X	X	x					X	X	x	X	x	X	x	X	x	X	X	x	x	x	X	X	X	X	X	X	X	X		
FcsErrors	X	х	х	X	х	X	X	X	X	X	X	x	X	X	X	X	X	X	x	X	Х	x	X	x	x	x	X	Х	X	X	X	X	X	Х		
BitsReceived	x	x	х	x	x	x	x	X					X	X	x	x	Х	x	x	X	Х	x	X	X	x	x	X	Х	Х	х	X	X	Х	Х		
BitsSent	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X	X	X	x	X	X	X	X	X	x	x	X	X	X	X	X	X	X	X		
PortCpuStatus																	X		Х	X	Х	X	X		X	Х	Х	Х	Х		X		X	Х		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
	X	Х	Х		Х		Х	Х	X	Х	Х	Х	X	Х	X																					
PortCpuDodStatus	X	X	X		X		X	X	X	Х	X	X	X	X	X		X		X	X	X	X	X		X	X	X	X	x		X		X	X		
Type: Transmit Duration																																				
TransmitDuration	X	x	X	X	x	x	X	x	x	Х	X	x	x	x	x	X	X	X	x	X	X	X	X	X	X	Х	Х	Х	х	Х	Х	X	Х	Х		
Type: Quality of Service																																				
QualityOfService0									x	x	x	x																								

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Canture	participation of the second	Packetaloup	exparamegnry	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: Checksum Stats																																					
IpPackets																						Х					X										
UdpPackets																						X					X										
TcpPackets																						X					X										
IpChecksumErrors																						X					X										
UdpChecksumErrors																						X					X										
TcpChecksumErrors																						X					X										
Type: Data Integrity																																					
DataIntegrityFrames			X												>	<								X						X							
DataIntegrityErrors			х												>	<								x						X							

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: Sequence Checking																																				
SequenceFrames					x						X						X								X						X					
SequenceErrors					x						Х						X								X						X					
Type: Ethernet																																				
Fragments				X												X								X						X						
Undersize				X												X								X						X						
Oversize																								X						X						

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
				Х												X																				
VlanTaggedFramesRx				Х												X								x						X						
FlowControlFrames				X												X								X						X						
Type: Gigabit																																				
SymbolErrorFrames				X												X								X						X						
SynchErrorFrames				Х												X								x						X						
Type: 10/100 + Gigabit																																				

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
SymbolErrors				x												X								X						X						
OversizeAndCrcErrors				x												X								X						X						
Type: POS																																				
SectionLossOfSignal																																			Х	
SectionLossOfFrame																																			Х	
SectionBip																																			Х	
LineAis																																			Х	

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
LineRdi																																			X	
LineRei																																			X	
LineBip																																			Х	
PathAis																																			X	
PathRdi																																			Х	
PathRei																																			X	
PathBip																																			X	

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
PathLossOfPointer																																			X	
PathPlm																																			Х	
SectionBipErroredSecs									x	X	X	X									X	X	x		X	X										
Sec- tionBipSeverlyErrored- Secs									x	X	X	X									X	Х	Х		Х	x										
Sec- tionLossOfSignalSecs									X	X	X	X									X	X	X		X	x										
LineBipErroredSecs									x	X	X	X									x	x	x		x	x										

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
LineReiErroredSecs									x	x	x	x									x	x	x		х	x										
LineAisAlarmSecs									X	X	x	X									X	x	X		X	X										
LineRdiUnavail- ableSecs									X	X	x	x									X	x	X		Х	X										
PathBipErroredSecs									X	X	x	X									X	X	X		X	X										
PathReiErroredSecs									X	х	x	x									x	x	X		Х	X										
PathAisAlarmSecs																					X	Х	Х		Х	Х										

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
									Х	Χ	Х	Х																								
PathAisUnavail- ableSecs									x	X	X	x									X	X	X		X	X										
PathRdiUnavail- ableSecs									X	X	X	x									X	X	X		X	X										
InputSignalStrength	X	х	X		X	X	X	X					х	X	X		x	x	X	X							X	Х	Х		х	X	X	Х		
PosK1Byte	X	x	x		X	X	X	X					X	X	X		x	X	X	X							X	Х	X		X	Х	X	X		
PosK2Byte	Х	X	х		x	Х	х	Х					X	X	X		Х	X	X	X							X	Х	Х		X	X	Х	Х		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
SrpDataFramesRe- ceived	X	X	X		X	X	X	X					X	X	X		X	X	X	 X							X	X	X		X	X	X	X		
SrpDis- coveryFramesReceived	x	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
SrpIpsFramesReceived	X	х	x		х	х	X	X					X	X	X		Х	X	X	X							X	х	Х		х	X	x	Х		
SrpParityErrors	x	x	x		X	X	X	X					X	X	X		X	X	X	X							X	Х	X		х	Х	x	X		
SrpUsageFramesRe- ceived	x	x	x		X	X	X	X					X	X	X		X	X	X	X							x	X	Х		х	X	x	х		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	PyDataIntourity	exparameginty	KXFIIFSUIIMESTAMP	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
SrpUsageStatus	X	X	x		X	X	X	X					X	X	×	(		x	X	X	X							X	X	X		X	X	X	X		
SrpUsageTimeouts	X	X	х		x	х	X	x					X	X	×	(	)	X	X	X	X							X	x	X		X	X	X	X		
Type: DCC																																					
DccBytesReceived						X	x					X							X	X							X						X	X			
DccBytesSent																																					
DccCrcErrorsReceived						x	x					x							X	X							X						X	X			
DccFramesReceived						х	Х					X							X	Х							X						X	X			

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RyFiretTimeStamp	RxSequenceChecking	tro do bostino	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
DccFramesSent																																					
DccFram- ingErrorsReceived																																					
Type: OC192 - Temperature																																					
DMATemperature																																					X
CaptureTemperature																																					X
LatencyTemperature																																					X
Back- groundTemperature																																					

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
OverlayTemperature																																				X
FrontEndTemperature																																				X
SchedulerTemperature																																				X
PlmDevice1In- ternalTemperature																																				X
PlmDevice2In- ternalTemperature																																				X
PlmDevice3In- ternalTemperature																																				X
FobPort1Fp- gaTemperature																																				X
FobPort2Fp-																																				

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	9	PacketGroup	RxDataIntegrity	DyCirctTimoStamp	Strimestalli	kxsequencecnecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
gaTemperature																																					
FobBoardTemperature																																					X
FobDevice1In- ternalTemperature																																					X

## Statistics for OC192c Modules with RPR and DCC

Statistics for OC192c Modules with RPR and DCC

			N	or	m a						o s								ger			М	ode um E	Che	ck-		M	l o d	e D	ata	Ιn	teg	rit	У	A	l d'- I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: User Configurable																																				
UserDefinedStat1	X	X	X	X	X	X	X	X					X	X	X	x	X	x	X	x	X	X	X	X	X	X	X	X	X	X	X	X	x	X		
UserDefinedStat2	X	x	X	X	x	X	X	X					X	X	х	x	X	x	X	x		x	X	x	x		X	X	X	X	X	X	X	X		
CaptureTrigger	x												X								X					X	X						X			
CaptureFilter	x												X								X						X						X			

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
StreamTrigger1													X	X			х	X	X	x																
StreamTrigger2													X	X			X	x	X	x																
Type: States																																				
Link	X	X	x	х	x	х	x	X	X	X	X	X	X	X	X	x	X	x	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
LineSpeed	X	x	X	Х	х	х	x	X	х	X	X	X	Х	X	х	х	х	X	X	x	Х	X	X	X	X	Х	X	X	х	х	х	х	х	Х		
DuplexMode				х												х								X						Х						

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
TransmitState	X	X	x	x	x	x	х	х	x	х	х	x	X	X	X	x	х	х	x	х	x	x	x	X	x	х	х	X	X	X	Х	x	х	x		
CaptureState	X	X	х	х	х	х	х	х	х	х	x	X	X	X	x	х	х	х	х	х	x	Х	X	X	x	X	X	х	х	Х	Х	X	X	х		
PauseState	X	x	X	x	x	x	x	х	x	х	x	x	X	X	X	X	х	х	X	х	X	x	X	X	x	X	Х	Х	X	Х	Х	х	х	х		
Type: Common																																				
FramesSent	X	X	X	X	X	x	X	Х	X	Х	X	X	X	X	X	X	х	х	X	х	X	x	x	X	x	X	X	X	X	X	X	x	X	X		
FramesReceived	X	X	x	X	X	x	X	x	X	x	X	X	X	X	x	x	x	x	x	x	X	x	x	x	Х	x	X	X	X	X	Х	х	Х	х		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
BytesSent	X	x	х	х	х	х	x	х	x	X	X	x	х	x	х	x	x	x	x	x	X	x	X	x	×	X	X	X	x	x	x	x	x	Х		
BytesReceived	X	x	х	х	X	X	x	х					x	x	x	x	x	X	X	X	X	X	X	x	x	X	X	X	X	X	X	X	X	X		
FcsErrors	X	х	х	Х	X	Х	X	х	х	X	X	X	х	х	х	х	х	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BitsReceived	X	x	x	X	X	х	x	x					x	x	x	x	x	X	X	X	X	X	X	X	X	Х	X	X	Х	Х	Х	X	X	X		
BitsSent	X	x	х	х	х	х	x	х	х	X	х	x	х	X	x	x	X	x	X	x	X	X	X	X	X	X	X	X	х	х	х	х	Х	Х		
PortCpuStatus																					Х	Х	X		X	X	X	X	Х		X		Х	X		

									Q	0 S			St	rea	a m	Tri	i g g	j e r					Che Erro			N	1 o d	e D	ata	Ιn	teg	ırit	У	Ad	ld'- I	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
	Х	Х	Х		Х		Х	Х	Х	Х	Х	Х	Х	Х	Х		Х		Х	Х																
PortCpuDodStatus	X	X	X		X		X	X	X	x	х	X	X	X	X		X		X	X	X	X	X		X	X	X	X	X		X		X	X		
Type: Transmit Duration																																				
TransmitDuration	X	X	X	X	x	X	X	x	Х	X	X	X	x	X	X	x	X	Х	X	x	X	X	X	X	X	X	X	X	X	X	Х	X	X	X		
Type: Quality of Service																																				
QualityOfService0									X	X	X	X																								
Type: Checksum Stats																																				

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
IpPackets																					Х					Х										
UdpPackets																					Χ					Х										
TcpPackets																					X					X										
IpChecksumErrors																					Χ					X										
UdpChecksumErrors																					Χ					X										
TcpChecksumErrors																					Χ					X										
Type: Data Integrity																																				
DataIntegrityFrames			X												X								X						X							
DataIntegrityErrors			X												x								X						X							
Type: Sequence Check-																																				

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
ing																																				
SequenceFrames					X						X						X								X						X					
SequenceErrors					х						X						X								x						Х					
Type: Ethernet																																				
Fragments				х												X								X						X						
Undersize				х												X								x						X						
Oversize				Х												X								X						X						

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
VlanTaggedFramesRx				X												X								X						X						
FlowControlFrames				X												X								X						X						
Type: Gigabit																																				
SymbolErrorFrames				X												x								x						X						
SynchErrorFrames				X												х								X						Х						
Type: 10/100 + Gigabit																																				

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking		Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
SymbolErrors				х												x								X						Х						
OversizeAndCrcErrors				х												х								X						X						
Type: POS																																				
SectionLossOfSignal																																			X	
SectionLossOfFrame																																			X	
SectionBip																																			X	
LineAis																																			X	

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
LineRdi																																			Х	
LineRei																																			X	
LineBip																																			Х	
PathAis																																			X	
PathRdi																																			X	
PathRei																																			X	
PathBip																																			X	
PathLossOfPointer																																			X	

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RyDataIntegrity	By Eiret Timo Stamp	RxSequenceChecking	trodoponod	RxModeBert	and January and Market Market	Canture	capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
PathPlm																																				X	
SectionBipErroredSecs									X	X	Х	x									>	<	X	X		X	X										
Sec- tionBipSeverlyErroredSe- cs									X	X	х	X									>	<	Х	Х		x	X										
SectionLossOfSignalSecs									X	X	x	X									>	<	X	x		x	x										
LineBipErroredSecs									X	X	X	X									>	<	X	X		x	x										
LineReiErroredSecs																					>	<	X	Х		Х	Х										

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	Defigetiment	Kritstilliestallip	KxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
									Х	Х	Х	Х				Ī	T	T																			
LineAisAlarmSecs									х	х	х	x										Χ	x	x		X	x										
LineRdiUnavailableSecs									х	x	х	x										X	x	x		X	x										
PathBipErroredSecs									x	x	x	x										X	X	x		X	X										
PathReiErroredSecs									X	X	X	x										X	x	x		X	x										
PathAisAlarmSecs									Х	х	Х	X										X	х	х		х	Х										

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
PathAisUnavailableSecs									х	X	X	X									X	Х	x		Х	X										
PathRdiUnavailableSecs									x	X	X	X									X	X	x		X	х										
InputSignalStrength	X	х	х		x	х	х	Х					X	X	х		Х	Х	х	Х							X	X	Х		Х	Х	X	X		
PosK1Byte																																				
PosK2Byte																																				
SrpDataFramesReceived																																				
SrpDis-																																				

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
coveryFramesReceived																																				
SrpIpsFramesReceived																																				
SrpParityErrors																																				
SrpUsageFramesRe- ceived																																				
SrpUsageStatus																																				
SrpUsageTimeouts																																				
Type: DCC																																				
DccBytesReceived						X	X					X						x	X							X						X	X			
DccBytesSent																																				
DccCrcErrorsReceived						Х	Х					Х						X	X							х						X	X			

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
DccFramesReceived						x	X					x						x	X							X						X	X			
DccFramesSent																																				
DccFram- ingErrorsReceived																																				
Type: OC192 - Tem- perature																																				
DMATemperature																																				Х
CaptureTemperature																																				Х
LatencyTemperature																																				X
BackgroundTemperature																																				

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking		RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
OverlayTemperature															П																					Х
FrontEndTemperature																																				Х
SchedulerTemperature																																				X
PlmDevice1In- ternalTemperature																																				x
PlmDevice2In- ternalTemperature																																				X
PlmDevice3In- ternal Temperature																																				X
FobPort1Fp- gaTemperature																																				X
FobPort2Fp- gaTemperature																																				
FobBoardTemperature																																				X

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
FobDevice1In- ternalTemperature																																				Х
Type: RPR																																				
RprDis- coveryFramesReceived	X	х	х		x	X	X	X					X	x	X		х	X	X	X							X	X	X		X	X	X	X		
RprDataFramesReceived	X	х	х		x	X	х	X					Х	x	x		х	x	x	X							х	Х	X		х	Х	Х	х		
RprFair- nessFramesReceived	X	x	x		x	x	X	x					Х	x	x		x	X	x	x							x	X	Х		X	X	X	Х		
RprFairnessFramesSent	X	х	x		X	X	x	X					Х	x	x		X	X	x	X							х	х	X		х	х	х	х		
RprFairnessTimeouts																											X	Х	X		X	X	X	X		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
	Х	Х	Х		Х	Х	Х	Х					Χ	Х	X		Х	Х	Х	Х																
RprHeaderCrcErrors	X	х	х		х	х	х	х					X	х	X		Х	х	X	х							Х	Х	X		X	X	X	Х		
RprOamFramesReceived	X	х	х		х	х	х	х					X	х	X		х	х	X	х							Х	Х	X		X	X	X	Х		
RprPayloadCrcErrors	X	x	x		x	x	x	x					X	x	X		x	x	X	x							Х	X	X		X	X	X	X		
RprPro- tectionFramesReceived	X	x	X		x	x	X	x					X	x	X		x	x	x	x							X	X	X		X	X	X	X		

## Statistics for OC192c Modules with BERT

## Statistics for 10GE Modules with BERT

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				Νo	rm	ı a l						Q	o s	;			s	Str	· e a	m	Tr	· i g	g e	r					C h e rro			M	100	de I	D a	ta	Ιn	te	gr	ity	y	Α (	d d - I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	Over Time Champ	RySequenceChecking	6	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: User Configurable																																											
UserDefinedStat1	×	X	X	X	X	x	X	X	x								<b>x</b> 2	X	X	X	x	X	X	x	X	X	X	x	X	X	X	X	X	X	<b>X</b>	( x	( )	x	x	X	x		
UserDefinedStat2	X	X	x	х	х	x	X	X	x								<b>X</b>	X	X	X	X	x	X	X	X		Х	X	X	X		X	X	X	<b>X</b>	×	( )	X	X	X	x		
CaptureTrigger	X																X									X					X	x								x			
CaptureFilter	X																X									X						X								X			

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
StreamTrigger1																	X	X			X	X	X	X	x																	
StreamTrigger2																	X	x			x	X	X	X	x																	
Type: States																																										
Link	x	X	X	x	X	x	x	X	X	X	X	X	X	X	X	X	X	x	x	X	x	x	X	X	X	Χ	X	x	x	X	X	X	x	X	X	X	X	x	X	X		
LineSpeed	X	X	X	x	X	x	x	X	X	X	X	X	X	X	X	X	X	x	x	X	x	X	X	X	x	Х	X	Х	X	X	X	X	x	X	X	X	x	x	Х	X		
DuplexMode				X																X									Х						x							

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
TransmitState	X	х	x	x	x	X	X	X	x	x	x	X	x	X	X	х	x	x	x	X	X	X	X	X	X	X	Х	X	x	X	X	X	X	X	X	X	X	x	X	x		
CaptureState	X	x	х	Х	х	X	X	X	x	X	X	X	X	X	X	х	х	Х	x	X	X	X	X	X	X	X	Х	X	X	X	X	X	X	X	X	X	x	x	X	X		
PauseState	X	х	x	x	x	X	X	X	x	x	X	X	X	X	х	х	x	x	x	X	X	x	X	X	X	X	Х	x	X	X	X	X	X	X	X	X	x	x	х	X		
Type: Common																																										
FramesSent	X	x	x	x	x	X	x	x	x	x	X	X	x	X	X	x	x	x	x	X	X	X	X	X	X	Χ	X	X	X	X	x	X	X	X	X	X	x	x	X	X		
FramesReceived	X	x	X	X	X	X	X	X	x	x	X	X	X	X	X	х	X	X	x	X	X	X	X	X	X	X	Х	X	X	X	X	X	X	X	X	X	x	x	X	X		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamn	RXSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
BytesSent	X	X	×	X	X	X	X	x	X	X	X	X	X	X	X	x	X	X	X	X	X	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x		
BytesReceived	X	X	×	X	X	X	X	X	X								X	X	X	X	X	x	x	X	X	X	X	X	X	x	X	X	X	X	X	X	x	X	X	x		
FcsErrors	X	x	X	X	X	X	Х	x	X	X	x	x	X	X	X	X	X	X	x	X	X	X	x	X	X	X	X	X	X	X	Х	X	x	X	X	X	X	X	x	x		
BitsReceived	X	x	×	X	X	X	X	x	X								X	X	X	x	X	X	X	x	X	X	Х	X	X	X	X	X	X	X	X	X	X	X	х	х		
BitsSent	x	x	X	X	X	x	X	x	x	X	Х	х	x	X	X	X	X	X	Х	x	X	X	X	X	X	X	Х	X	X	x	X	X	X	x	x	x	x	x	x	x		
PortCpuStatus																										Х	Х	Х		Х	Х											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
	X	Х	Х		Х			Х	X	X	Х	Х			Х	X	Х	X	Х		Х			Х	Х							X	X	Х		X			Х	Х		
PortCpuDodStatus	X	x	X		X			X	Х	x	x	X			X	x	x	X	X		х			x	Х	X	X	X		X	X	X	x	X		X			X	x		
Type: Transmit Duration																																										
TransmitDuration	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	x	X	X	X	x	X	X	X	X	X	X	X	X	X	x	X	x	X	X		
Type: Quality of Service																																										
QualityOfService0										X	X	X	X	X	X	X																										
Type: Checksum																																										

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Stats																																										
IpPackets																										X					X											
UdpPackets																										X					X											
TcpPackets																										X					X											
IpChecksumErrors																										Х					Х											
UdpChecksumErrors																										Х					Х											
TcpChecksumErrors																										Х					Х											
Type: Data Integrity																																										
DataIntegrityFrames			X																X									X						X								
DataIntegrityErrors			х																X									Х						x								

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: Sequence Checking																																										
SequenceFrames					x						,	x									X									x						X						
SequenceErrors					X							x									X									x						X						
Type: Ethernet																																										
Fragments	X	X		x	x	X	X		× z	<b>x</b> 2	X I	x	x	x		x	X	X		x	X	x	X		X				X			X	X		X	X	X	X		X		
Undersize	X	X		x	X	X	X		× Z	<b>x</b> 2	X I	X	X	x		X	X	x		x	X	X	X		X				Х			X	х		x	X	x	x		х		
Oversize																													Х													

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RXSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
	Х	Х		Х	Х	Х	X		X	X	Х	X	X	X		X	Х	Х		Х	X	Х	X		X							X	Х		Х	Х	X	X		Х		
VlanTaggedFramesRx	X	X		X	X	x	x		X	X	X	X	X	X		x	x	X		x	X	x	X		X				Х			X	x		х	х	x	х		х		
FlowControlFrames	x	X		x	x	x	x		x	X	x	X	X	X		x	x	X		X	X	x	x		X				Х			x	x		х	х	х	х		X		
Type: Gigabit																																										
SymbolErrorFrames				x																x									X						x							
SynchErrorFrames				X																X									Х						х							
Type: 10/100 + Gig-																																										

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
abit																																										
SymbolErrors				x																X									x						X							
OversizeAndCrcErrors	х	X		x	X	X	x		X	x	x	X	х	x		X	X	X		Х	х	X	X		x				X			X	X		x	х	x	x		X	,	
Type: POS																																										
SectionLossOfSignal																																									X	
SectionLossOfFrame																																									X	
SectionBip																																									X	
LineAis																																									X	

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RySequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
LineRdi																																									X	
LineRei																																									X	
LineBip																																									X	
PathAis																																									X	
PathRdi																																									X	
PathRei																																									X	
PathBip																																									X	

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
PathLossOfPointer																																									X	
PathPlm																																									X	
Sec- tionBipErroredSecs															x											X	Х	x		X	X											
Sec- tionBipSeverlyErrore- dSecs															x											Х	X	X		X	X											
Sec- tionLossOfSignalSecs															x											X	x	Х		Х	Х											
LineBipErroredSecs															X											Χ	X	x		X	X											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
LineReiErroredSecs															X											X	X	X		X	X											
LineAisAlarmSecs															X											X	X	x		x	x											
LineRdiUnavail- ableSecs															X											X	X	X		X	X											
PathBipErroredSecs															X											X	X	X		X	X											
PathReiErroredSecs															X											X	X	X		X	X											
PathAisAlarmSecs																										Х	Х	Х		Х	X											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
															X																					Γ						
PathAisUnavail- ableSecs															x											X	Х	X		X	X											
PathRdiUnavail- ableSecs															X											X	Х	X		X	X											
InputSignalStrength	X	X	X		X	X	X	X	x	x	X	X	х	X		X	X	X	X		X	X	X	X	X							X	X	X		X	X	X	X	X		
PosK1Byte			X					X											X					X										X					X			
PosK2Byte			Х					X											X					Х										X					Х			

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
SrpDataFramesRe- ceived			X					X											X					X										X					X			
SrpDis- cov- eryFramesReceived			X					X											x					X										X					X			
SrpIpsFramesRe- ceived			x					x											x					X										x					x			
SrpParityErrors			X					X											х					X										X					X			
SrpUsageFramesRe- ceived			X					X											X					X										X					X			

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
SrpUsageStatus			X					X											X					X										X					X			
SrpUsageTimeouts			x					X											X					X										X					X			
Type: DCC																																										
DccBytesReceived								X							X									x							X								X			
DccBytesSent																																										
DccCrcErrorsReceived								X							X									X							X								X			
DccFramesReceived								X							X									X							Х								Х			

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RXFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
DccFramesSent																																										
DccFram- ingErrorsReceived																																										
Type: OC192 - Temperature																																										
DMATemperature																																										X
CaptureTemperature																																										X
LatencyTemperature																																										X
Back- groundTemperature																																										

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
OverlayTemperature																																										X
FrontEndTemperature																																										X
Sched- ulerTemperature																																										Х
PlmDevice1In- ternalTemperature																																										X
PlmDevice2In- ternalTemperature																																										X
PlmDevice3In- ternalTemperature																																										X
FobPort1Fp- gaTemperature																																										X
FobPort2Fp-																																										

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RXModeDcc	Capture	Daylot Cross	PacketsToup	Exparaintegrity  DyfiretTimeStamn	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
gaTemperature																																									
FobBoardTem- perature																																									X
FobDevice1In- ternalTemperature																																									X
Type: 10 Gig																																									
PauseAcknowledge	X	X			Х	X	x		x x	x x	<b>x</b> 2	x 2	<b>X</b>	x	>	<b>(</b> )	( <b>&gt;</b>	(		X	x	x		X							X	X			x	х	Х		X		
PauseEndFrames	X	X			X	X	X		x >	x x	x :	x :	X :	X	>	< ×	( <b>&gt;</b>	(		X	X	X		X							X	X			x	х	X		х		
PauseOverwrite	X	X			x	X	X		× ×	x x	x :	x :	x :	x	>	< ×	( ×	(		X	X	x		X							X	x			x	x	X		x		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	KxModeWidePacketGroup	Capture	Packeteroup	NASequencecinecaling	RyModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RXFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
10GigLanTxFp- gaTemperature												Γ		Γ		Γ															Γ			Γ							
10GigLanRxFp- gaTemperature																																									
Cod- ingEr- rorFramesReceived																																									
EEr- rorChar- acterFramesReceived																																									
DroppedFrames																																									
Type: Link Fault Sig- naling																																									
LinkFaultState	X	X			X		X		<b>x</b>	<b>(</b> )	( )	(	X		X	X	X			X		X		Х							X	X			X		X		Х		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	lodeBe	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	lodeD	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	ModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
LocalFaults	X	X			X		X		X	X	X	X		X		X	X	X			X		X		X							X	X			X		X		X		
RemoteFaults	x	х			X		X		X	x	X	X		X		x	X	X			X		x		X							X	x			X		X		X		

## **Statistics for 10G UNIPHY Modules with BERT**

## Statistics for 10G UNIPHY Modules with BERT

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	Over Time Champ	PySequenceChecking	6	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: User Configurable																																											
UserDefinedStat1	X	x	X	X	X	X	x	X	X								X	X	X	X	X	X	X	x	X	X	X	x	X	X	X	X	X	X	<b>X</b>	( ) ×		x	x	X	X		
UserDefinedStat2	X	х	x	x	x	x	х	X	x								X	x	x	x	X	X	X	x	X		x	x	x	x		X	X	X	<b>X</b>	( )×	( )	x	x	х	x		
CaptureTrigger	X																X									X					X	X											
CaptureFilter	X																X									X						X											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
StreamTrigger1																	X	X			X	X	X	X	x																	
StreamTrigger2																	X	x			x	X	X	X	x																	
Type: States																																										
Link	x	X	X	x	X	x	x	X	X	X	X	X	X	X	X	X	X	x	x	X	x	x	X	X	x	Χ	X	x	x	X	X	X	x	X	X	X	X	x	X	X		
LineSpeed	X	X	X	x	X	x	x	X	X	X	X	X	X	X	X	X	X	x	x	X	x	X	X	X	x	Х	X	Х	X	X	X	X	x	X	X	X	x	x	Х	X		
DuplexMode				X																X									Х						x							

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	ert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
TransmitState	X	Х	x	x	X	X	X	X	X	x	X	x	X	X	X	X	X	X	X	X	X	X	x	X	X	X	Х	x	X	X	X	X	X	x	x	X	x	x	х	X		
CaptureState	X	х	х	X	х	x	x	X	х	х	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	Х	X	X	X	Х	X	X	x	x	X	х	х	х	X		
PauseState	X	х	x	x	x	x	X	X	X	x	X	x	х	X	X	X	X	X	X	X	x	X	x	X	X	X	Х	x	x	X	X	X	X	x	x	X	х	х	х	x		
Type: Common																																										
FramesSent	X	X	x	x	x	x	X	x	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Χ	X	X	X	X	X	X	X	X	x	X	X	X	X	X		
FramesReceived	X	X	x	X	X	x	X	x	X	X	x	X	X	X	X	Х	X	x	x	X	X	x	X	X	X	Х	Х	Х	X	X	X	X	X	X	X	x	x	x	х	X		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
BytesSent	X	x	X	X	X	X	x	x	X	X	X	X	X	X	X	x	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesReceived	Х	X	x	x	х	X	X	X	x								X	X	X	X	X	X	X	x	X	Х	X	X	x	X	X	X	X	x	x	x	x	X	X	x		
FcsErrors	X	X	x	x	x	X	X	X	x	x	X	X	X	x	X	x	X	X	X	X	X	X	X	x	X	Х	X	X	x	X	Х	X	X	x	x	x	X	x	X	X		
BitsReceived	X	X	x	X	X	X	x	X	x								X	X	X	X	X	X	X	X	x	X	X	X	x	X	Х	X	X	X	x	X	X	X	X	X		
BitsSent	x	X	x	X	x	X	X	X	x	x	X	X	X	x	X	x	X	X	X	X	X	X	X	x	x	Х	Х	X	X	X	X	X	X	X	x	x	X	x	X	X		
PortCpuStatus																										X	Х	X		X	X											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking		RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
	X	Х	X		X			X	X	Χ	Χ	Χ			X	Х	X	Х	Х		X			X	X							X	Х	X		Х			Х	Х		
PortCpuDodStatus	X	X	X	,	X			X	X	X	Х	X			X	x	X	X	X		х			х	x	x	x	X		x	X	X	X	Х		X			Х	Х		
Type: Transmit Duration																																										
TransmitDuration	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Quality of Service																																										
QualityOfService0										X	X	X	X	X	X	X																										
Type: Checksum																																										

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Stats																																										
IpPackets																										X					X											
UdpPackets																										X					X											
TcpPackets																										X					X											
IpChecksumErrors																										Χ					X											
UdpChecksumErrors																										Х					Х											
TcpChecksumErrors																										Х					Х											
Type: Data Integrity																																										
DataIntegrityFrames			X																X									X						X								
DataIntegrityErrors			X																x									X						X								

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	Cantiire	Darket	RySomienceChecking	Developer t	Porilogous Action of the Control of	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: Sequence Checking																																									
SequenceFrames					X						X									X									X						X						
SequenceErrors					Х						X									Х									x						х						
Type: Ethernet																																									
Fragments				X		X	X		×	×	×	X >	( )	(	×				X		x	x						x						x		Х	X				
Undersize				X		X	X		×	×	×	×	( <b>&gt;</b>	(	X				X		x	x						x						х		Х	Х				
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	Capture	PacketGroup	RxDataIntegrity	PyEiretTimoStamn	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
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VlanTaggedFramesRx				×		X	x			X	X	X	X	X		x				X		x	X						X						x		х	x				
FlowControlFrames				×		X	X			X	X	X	X	X		x				X		x	X						X						x		x	x				
Type: Gigabit																																										
SymbolErrorFrames				X																x									X						X							
SynchErrorFrames				X																X									X						x							
Type: 10/100 + Gig-																																										

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking		RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
abit																																											
SymbolErrors				x																X									X							X							
OversizeAndCrcErrors				х		Х	X			x	x	x	x	X		X				X		x	X						X							X		X	x				
Type: POS																																											
SectionLossOfSignal																																										X	
SectionLossOfFrame																																										X	
SectionBip																																										Х	
LineAis																																										Х	

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
LineRdi																																									X	
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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
PathLossOfPointer																																									X	
PathPlm																																									X	
Sec- tionBipErroredSecs															x											X	Х	x		X	X											
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LineBipErroredSecs															X											Χ	X	x		X	X											

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	Capture	PacketGroup	RxDataIntegrity	ByEiretTimeStamn	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
LineReiErroredSecs															X											X	X	X		X	X											
LineAisAlarmSecs															X											Χ	X	X		X	X											
LineRdiUnavail- ableSecs															X											Х	Х	Х		X	Х											
PathBipErroredSecs															X											X	Х	Х		Х	Х											
PathReiErroredSecs															X											X	X	Х		Х	Х											
PathAisAlarmSecs																										X	Х	X		Х	X											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	DarkotGroup	DyDataIntonrity	ore intrinsical to	RXFIFSTIIMEStamp PySoguenceChecking	kxsequencecnecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
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PathAisUnavail- ableSecs															X											X	Х	X		X	X												
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InputSignalStrength	X	х	х		х	x	X	Х	x	X	X	Х	X	Х		X	x	X	X		X	Х	х	X	X							X	×	( <b>X</b>	(	>	< 1	X	X	Х	Х		
PosK1Byte								+																+											+								
PosK2Byte																																				1	T	$\top$					
SrpDataFramesRe- ceived																																											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RyMode BertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
SrpDis- cov- eryFramesReceived																																										
SrpIpsFramesRe- ceived																																										
SrpParityErrors																																										
SrpUsageFramesRe- ceived																																										
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Type: DCC																																										
DccBytesReceived								X							x									x							X								х			

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DccBytesSent																																										
DccCrcErrorsReceived								X							X									X							X								Х			
DccFramesReceived								X							X									X							X								Х			
DccFramesSent																																										
DccFram- ingErrorsReceived																																										
Type: OC192 - Temperature																																										
DMATemperature																																										Х
CaptureTemperature																																										Х

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LatencyTemperature																																										X
Back- groundTemperature																																										
OverlayTemperature																																										X
FrontEndTemperature																																										X
Sched- ulerTemperature																																										X
PlmDevice1In- ternalTemperature																																										Х
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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
PlmDevice3In- ternalTemperature									Ī																						Г											Х
FobPort1Fp- gaTemperature																																										X
FobPort2Fp- gaTemperature																																										
FobBoardTem- perature																																										X
FobDevice1In- ternalTemperature																																										X
Type: 10 Gig																																										
PauseAcknowledge						X	X			X	X	X	X	X		X						X	X														X	X				
PauseEndFrames																																										

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	Capture	PacketGroup	RxDataIntegrity	RyFirstTimeStamn	PySequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamn	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	DacketGroup	developed	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
						X	X			Х	Х	Х	Х	Х		Х						X	Х															Х	X				
PauseOverwrite						X	X			X	x	x	x	x		X						x	X															X	х				
10GigLanTxFp- gaTemperature																																											
10GigLanRxFp- gaTemperature																																											
Cod- ingEr- rorFramesReceived																																											
EEr- rorChar- acterFramesReceived																																											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	DyEiretTimoStamo	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
DroppedFrames																																										
Type: Link Fault Sig- naling																																										
LinkFaultState							X			x	X	X		X		X							x															X				
LocalFaults							X			X	X	X		x		X							X															X				
RemoteFaults							х			X	X	X		X		Х							X															X				
Type: RPR								1														+	+																			
RprDis- cov- eryFramesReceived	X	X	X		X			x	X								X	X	X		X			x	X							×	X	X	,	X			X	X		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
RprDataFramesRe- ceived	X	x	X	,	X			X	x								X	X	Х		x			X	X							x	x	x		x			х	х		
RprFair- nessFramesReceived	X	x	X		X			X	x								X	X	X		X			X	X							X	X	X		X			х	x		
RprFair- nessFramesSent	X	x	X	,	X			Х	x								X	X	X		X			X	X							X	X	X		X			х	X		
RprFairnessTimeouts	X	X	X		X			X	x								X	X	X		X			X	X							X	X	X		X			х	X		
RprHeaderCrcErrors	X	X	X	,	X			X	x								X	X	X		X			x	X							X	x	x		X			х	X		
RprOamFramesRe-																																										

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamn	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Exten	TemperatureSensorsStats
ceived	Х	X	Х		X			X	Х								X	X	X		Х			X	X							X	Х	X		X			X	X		
RprPayloadCrcErrors	X	x	X		X			x	x								x	x	X		X			X	X							X	X	X		X			X	X		
RprPro- tec- tionFramesReceived	x	Х	x		X			X	x								X	x	x		x			X	X							X	X	X		X			X	X		

## Statistics for 10GE LSM Modules (except NGY)

Statistics for 10GE LSM Modules (except NGY)

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: User Configurable																																											
UserDefinedStat1	X	x	x	x	x	x	x	X	X	X	x	X	X				x	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	x	X	X	X	X	X	x	x		
UserDefinedStat2	X	x	X	X	x	x	X	X	X	X	x	X	X				x	X	X	X	x	X	X	X	X	X		X	X	X	X		X	x	x	X	X	X	X	x	X		
CaptureTrigger	X	X							X	X	X						x	X	X							X	X					X	X	X							X		
CaptureFilter	X	X							X	X	X						X	Х	X							X	X						Х	Х							X		

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
StreamTrigger1	X	X	X		X				X	X	X	X	X				X	X	X	X		x	X	X	X	X							X	X	X		x				X		
StreamTrigger2	x	X	X		x				X	x	X	x	X				X	X	X	X		х	Х	X	x	X							X	X	x		х				х		
Type: States																																											
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	x	X	X	X	X	X	X	X	X	X	X	X	X		
LineSpeed	x	X	x	X	x	x	X	X	X	x	X	x	X	X	X	x	X	X	X	X	X	x	X	X	x	X	X	X	x	X	x	X	X	X	x	X	х	X	х	Х	х		
DuplexMode																														X													

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
				Χ							Ī										X															X							
TransmitState	X	x	X	X	X	X	X	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Х	Х	Х	X	X	X	X	X	X	x	X	X	X	X		
CaptureState	X	x	X	X	Х	X	X	X	X	x	x	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X	Х	X	Х	X	X	X	X	X	X	x	X	X	X	X		
PauseState	X	x	X	X	X	х	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X	X	Х	x	x	X	X	X	X	X	X	X	x	х	X	X	X		
Type: Common																																											
FramesSent	x	x	x	X	X	X	X	X	X	x	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	x	x	X	X	X		

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	ByEiretTimoStamn	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
FramesReceived	X	X	X	X	X	X	x	X	X	x	x	X	X	X	X	X	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	×	X	X	X	X	X	,	
BytesSent	X	X	X	X	X	X	X	X	х	х	x	х	X	X	X	x	X	X	x	X	X	X	X	X	x	X	X	Х	Х	X	X	X	X	X	X	×	X	X	X	X	X		
BytesReceived	X	X	X	X	X	X	Х	X	x	x	X	х	X				X	х	X	х	X	x	x	X	X	X	X	Х	X	X	X	X	X	X	X	×	X	X	X	X	X	,	
FcsErrors	X	X	X	X	X	X	x	X	X	X	X	X	x	X	X	x	x	X	X	x	X	x	x	x	x	X	Х	Х	Х	X	X	X	X	X	X	×	X	X	X	x	X	,	
BitsReceived	X	x	X	X	X	x	x	x	X	X	x	X	x				X	X	x	х	X	x	X	X	X	X	X	х	х	X	X	X	X	X	X	X	X	X	X	X	X		

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	odeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	odeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
BitsSent	X	X	X	X	X	x	X	X	X	X	X	X	X	X	X	x	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X	X	X	,	
PortCpuStatus	X	X	X	7	X			х	X	X	X	X	X			x	X	X	X	X		x			x	X	X	X	X		X	X	X	X	X		X			X	X	,	
PortCpuDodStatus	X	X	X		X			X	X	X	X	X	X			x	X	X	X	X		X			X	X	X	X	X		X	X	X	X	X		X			X	X	,	
Type: Transmit Duration																																											
TransmitDuration	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	,	
Type: Quality of Ser-																																											

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
vice																																											
QualityOfService0										x	x	x	X	X	X	X	x																										
Type: Checksum Stats																																											
IpPackets																											Х					X											
UdpPackets																											Χ					Х											
TcpPackets																											Χ					Х											
IpChecksumErrors																											Χ					Х											
UdpChecksumErrors																											Χ					Х											
TcpChecksumErrors																											X					Х											

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RXModeBertChannelized DxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: Data Integrity																																										
DataIntegrityFrames			X								X								X									X						X								
DataIntegrityErrors			x								X								X									X						X								
Type: Sequence Checking																																										
SequenceFrames					x							X									X									X						X						
SequenceErrors					X							X									x									X						x						

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Extende	TemperatureSensorsStats
Type: Ethernet																																											
Fragments	X	X	x	x	X	X	X		X	X	X	x	X	X	X		X	X	X	X	X	x	X	X		X				X			X	X	X	X	X	X	X		X		
Undersize	X	x	X	X	X	x	X		X	x	X	X	x	X	X		x	X	X	x	x	x	X	X		X				X			X	X	X	X	X	X	X		X		
Oversize	X	x	X	X	X	x	X		X	X	X	X	x	X	X		X	X	X	x	x	x	X	X		X				X			X	X	X	X	X	x	X		X		
VlanTaggedFramesRx	X	x	X	X	X	x	X		X	X	x	x	x	X	X		X	X	X	x	x	x	X	X		X				X			X	X	X	X	X	x	X		x		
FlowControlFrames	X	Х	х	X	X	х	X		X	x	X	X	X	Х	х		Х	X	Х	х	X	х	X	X		Х				X			X	X	X	X	X	Х	X		Х		

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity		RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats		l emperaturesensorsstats
Type: Gigabit																																													
SymbolErrorFrames				X																	X									)	X						X								
SynchErrorFrames				X																	X									>	X						X								
Type: 10/100 + Gig- abit																																													
SymbolErrors				х																	X									)	X						X								
OversizeAndCrcErrors	X	X	X	X	X	X	X		X	X	X	X	X	X	X		X	X	X	X	X	X	X	X		X				)	X			X	X	X	X	X	X	X		X			

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: POS																																											
SectionLossOfSignal																																										X	
SectionLossOfFrame																																										Х	
SectionBip																																										Х	
LineAis																																										X	
LineRdi																																										Х	
LineRei																																										Х	

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
LineBip																																										X	
PathAis																																										X	
PathRdi																																										X	
PathRei																																										Х	
PathBip																																										Х	
PathLossOfPointer																																										X	
PathPlm																																										X	

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Sec- tionBipErroredSecs																X											X	x	X		X	x											
Sec- tionBipSeverlyErrored- Secs																x											X	X	X		X	X											
Sec- tionLossOfSignalSecs																x											X	X	X		X	X											
LineBipErroredSecs																X											X	X	X		X	X											
LineReiErroredSecs																X											X	X	X		X	X											

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
LineAisAlarmSecs																X											X	X	X		X	X											
LineRdiUnavail- ableSecs																Х											X	Х	Х		X	X											
PathBipErroredSecs																Х											Х	Х	Х		X	x											
PathReiErroredSecs																X											X	X	X		X	x											
PathAisAlarmSecs																X											X	X	Х		X	X											

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
PathAisUnavail- ableSecs																х											Х	Х	Х		x	Х											
PathRdiUnavail- ableSecs																X											Х	Х	X		X	X											
InputSignalStrength	X	x	x		X	х	x	x	X	X	x	X	X	X	x		х	X	х	Х		X	X	x	x	X							X	x	X		X	Х	х	X	х		
PosK1Byte																																											
PosK2Byte																																											
SrpDataFramesRe- ceived																																											
SrpDis- cov-																																											

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
eryFramesReceived																																											
SrpIpsFramesRe- ceived																																											
SrpParityErrors																																											
SrpUsageFramesRe- ceived																																											
SrpUsageStatus																																											
SrpUsageTimeouts																																											
Type: DCC																																											
DccBytesReceived								X								X									X							X								X			
DccBytesSent																																											

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
DccCrcErrorsReceived								X								X									x							х								х			
DccFramesReceived								X								x									X							Х								х			
DccFramesSent																																											
DccFram- ingErrorsReceived																																											
Type: OC192 - Temperature																																											
DMATemperature																																											X
CaptureTemperature																																											X

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
LatencyTemperature																																											Х
Back- groundTemperature																																											X
OverlayTemperature																																											X
FrontEndTemperature																																											X
Sched- ulerTemperature																																											
PlmDevice1In- ternalTemperature																																											
PlmDevice2In- ternalTemperature																																											

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	Packetoroup	KXDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
PlmDevice3In- ternalTemperature																																			Ī								
FobPort1Fp- gaTemperature																																											
FobPort2Fp- gaTemperature																																											
FobBoardTemperature																																											
FobDevice1In- ternalTemperature																																											
Type: 10 Gig																																											
PauseAcknowledge	X	X	x		X	X	x		X	X	x	X	X	X	X		x	X	x	x		X	X	X		X							<b>x</b> 2	<	×		X	X	X		X		

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	PyEiretTimeStamn	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
PauseEndFrames	X	x	X		X	x	X		X	X	X	x	X	X	X		X	x	X	x		x	X	x		Х							x	X	X		X	X	X		x		
PauseOverwrite	X	X	X		X	x	X		X	X	х	X	Х	X	х		Х	х	х	Х		Х	Х	х		x							X	X	X		X	X	X		X		
10GigLanTxFp- gaTemperature																																											
10GigLanRxFp- gaTemperature																																											
Cod- ingEr- rorFramesReceived	X	X	X		X				X	x	X	X	X				х	x	X	X		x				Х							x	X	X		X				X		
EEr- rorChar-	X	X	X		X				X	X	Х	X	Х				Х	х	Х	х		Х				Х							Х	X	X		X				X		

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
acterFramesReceived																																										
DroppedFrames	X	X	x		X			X	X	X	X	X				X	X	X	X		X				X							X	X	X		X				X		
Type: Link Fault Sig- naling																																										
LinkFaultState	X	X	X		X		X	X	X	x	X	X		X		X	X	X	X		X		X		X							X	X	x		X		X		X		
LocalFaults	X	X	X		X		X	X	x	X	X	X		x		х	X	X	X		X		X		X							X	X	x		х		Х		X		
RemoteFaults	X	x	X		X		X	X	X	X	X	X		X		X	X	X	X		X		X		X							X	X	X		X		X		X		

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RXFirstTimeStamp	RySequenceChecking	RyModeBert	RXModeBert DyModeBertChannelized	by Mode Derichannelized	RXModeDcc ByModeWideDacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Canture	Capture	RyDataIntegrity		EXFIRST IIII estamp	wasedness and a	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
Type: RPR																																												
RprDis- cov- eryFramesReceived								X																	>	<															x			
RprDataFramesRe- ceived								X																	>	<															X			
RprFair- nessFramesReceived								X																	>	<															X			
RprFair- nessFramesSent								X																	>	<															X			
RprFairnessTimeouts								X																	<b>&gt;</b>	<															X			

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
RprHeaderCrcErrors								X																	X															X			
RprOamFramesRe- ceived								X																	X															X			
RprPayloadCrcErrors								X																	X															х			
RprPro- tec- tionFramesReceived								X																	X															X			
Type: Ordered Sets																																											
LocalOrderedSetsSent																																											

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Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Cantura	DackotGroup	PyDataIntourity	Definition	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
	Х	Х	Х		X				Х	X	X	X	X				X	X	X	Х		Х				Х							>	( )	( <b>X</b>	(	Х				Х		
LocalOrderedSet- sReceived	X	X	X		X				X	X	X	x	X				X	X	x	X		x				X							×	( ×	( ×		X				X		
RemoteOrderedSet- sSent	x	X	X		x				X	X	X	X	X				X	X	X	X		x				Х							×	( ×	( ×	(	X				X		
RemoteOrderedSet- sReceived	x	X	X		x				X	X	X	X	X				X	X	X	X		x				Х							×	( ×	( ×	(	X				X		
Cus- tomOrderedSetsSent	X	x	X		x				X	X	X	X	X				X	X	X	X		x				х							×	( ×	( ×	(	X				X		
Cus-																																											

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:	Statistics Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	TemperatureSensorsStats
	omOrderedSet- Received	X	X	X		X				X	X	X	X	Х				X	X	X	X		Х				X							X	X	Х		Х				Х		

## **Statistics for NGY Modules**

## Statistics for NGY Modules

Statistics Mode		Nor	mal			Q	0 S	
Receive Mode	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
Type: User Configurable								
UserDefinedStat1	X	X	X	X	X	X	X	X
UserDefinedStat2	X	X	X	X	X	X	X	X
UserDefinedStatByteCount1	X	X	X	X	X	X	X	X
UserDefinedStatByteCount2	X	X	X	X	X	X	X	X
CaptureTrigger	X			X	Х			Х
CaptureFilter	X			X	Х			X
StreamTrigger1	X	Х	X	X	X	X	X	X
StreamTrigger2	X	Х	X	X	X	X	X	X
Type: States								

Statistics Mode		Nor	m a l			Q	0 S	
Receive Mode	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
Link	Χ	Х	X	X	Х	X	X	Х
LineSpeed	X	Х	X	X	Х	X	X	X
DuplexMode								
TransmitState	X	X	X	X	X	X	X	X
CaptureState	X	Х	X	X	Х	Х	X	X
PauseState	X	X	X	X	X	X	X	X
Type: Common								
FramesSent	X	X	X	X	X	X	X	X
FramesReceived	X	X	X	X	Х	Х	X	Х
BytesSent	X	Х	X	X	Х	Х	X	Х
BytesReceived	X	Х	Х	Х	Х	X	X	X
FcsErrors	X	X	X	X	X	X	X	Х

Statistics Mode		Nor	m a l			Q	0 S	
Receive Mode	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
BitsReceived	X	X	X	X	X	X	X	X
BitsSent	X	X	X	X	X	X	X	X
PortCpuStatus	X	X	X	X	X	X	X	X
PortCpuDodStatus	X	X	X	X	X	X	X	X
Type: Transmit Duration								
TransmitDuration	X	X	X	X	X	X	X	X
Type: Quality of Service								
QualityOfService0					Х	X	Х	Х
Type: Checksum Stats								
IPv4Packets	X	Х	Х	X	Х	Х	Х	Х
UdpPackets	X	Х	Х	X	X	X	Х	Х
TcpPackets	X	X	X	X	Х	X	X	X

Statistics Mode		Nor	m a l			Q	0 S	
Receive Mode	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
IPv4ChecksumErrors	X	X	X	X	X	X	X	X
UdpChecksumErrors	X	X	X	X	X	X	X	X
TcpChecksumErrors	X	X	X	X	X	X	X	X
Type: Data Integrity								
DataIntegrityFrames		X				X		
DataIntegrityErrors		Х				X		
Type: Sequence Checking								
SequenceFrames			X				X	
SequenceErrors			Х				Х	
Type: Ethernet								
Fragments	X	X	Х	X	Х	X	Х	Х
Undersize	X	X	Х	X	Х	Х	Х	Х

Statistics Mode		Nor	m a l			Q	0 S	
Receive Mode	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
Oversize	X	X	X	X	X	X	X	X
VlanTaggedFramesRx	X	X	X	X	X	X	X	X
FlowControlFrames	X	X	X	X	X	X	X	X
Type: Gigabit								
SymbolErrorFrames								
SynchErrorFrames								
Type: 10/100 + Gigabit								
SymbolErrors								
OversizeAndCrcErrors	X	Х	X	X	X	Х	X	X
Type: POS								
SectionLossOfSignal								
SectionLossOfFrame								

Statistics Mode		Nor	m a l			Q	o s	
Receive Mode	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
SectionBip								
LineAis								
LineRdi								
LineRei								
LineBip								
PathAis								
PathRdi								
PathRei								
PathBip								
PathLossOfPointer								
PathPlm								
SectionBipErroredSecs								

Statistics Mode		Nor	mal			Q	0 S	
Receive Mode	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
SectionBipSeverlyErroredSecs								
SectionLossOfSignalSecs								
LineBipErroredSecs								
LineReiErroredSecs								
LineAisAlarmSecs								
LineRdiUnavailableSecs								
PathBipErroredSecs								
PathReiErroredSecs								
PathAisAlarmSecs								
PathAisUnavailableSecs								
PathRdiUnavailableSecs								
InputSignalStrength	Х	Х	X	X	X	Х	X	X

Statistics Mode		Nor	mal			Q	o s	
Receive Mode	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
PosK1Byte								
PosK2Byte								
SrpDataFramesReceived								
SrpDiscoveryFramesReceived								
SrpIpsFramesReceived								
SrpParityErrors								
SrpUsageFramesReceived								
SrpUsageStatus								
SrpUsageTimeouts								
Type: DCC								
DccBytesReceived								
DccBytesSent								

Statistics Mode		Nor	mal			Q	0 S	
Receive Mode	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
DccCrcErrorsReceived								
DccFramesReceived								
DccFramesSent								
DccFramingErrorsReceived								
Type: OC192 - Temperature								
DMATemperature								
CaptureTemperature								
LatencyTemperature								
BackgroundTemperature								
OverlayTemperature								
FrontEndTemperature								
SchedulerTemperature								

Statistics Mode		Nor	mal			Q	0 S	
Receive Mode	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
PlmDevice1InternalTemperature								
PlmDevice2InternalTemperature								
PlmDevice3InternalTemperature								
FobPort1FpgaTemperature								
FobPort2FpgaTemperature								
FobBoardTemperature								
FobDevice1InternalTemperature								
Type: 10 Gig								
PauseAcknowledge	X	X	X	X	Х	Х	X	X
PauseEndFrames	X	Х	Х	X	Х	Х	Х	X
PauseOverwrite	X	Х	Х	X	Х	Х	X	X
10GigLanTxFpgaTemperature								

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Statistics Mode		Nor	m a l			Q	0 S	
Receive Mode	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
10GigLanRxFpgaTemperature								
DroppedFrames	X	X	X	X	X	X	X	X
Type: Link Fault Signaling								
LinkFaultState	X	X	X	X	X	X	X	X
Type: RPR								
RprDiscoveryFramesReceived								
RprDataFramesReceived								
RprFairnessFramesReceived								
RprFairnessFramesSent								
RprFairnessTimeouts								
RprHeaderCrcErrors								
RprOamFramesReceived								

Statistics Mode		Nor	m a l			Q	0 S	
Receive Mode	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
RprPayloadCrcErrors								
RprProtectionFramesReceived								
Type: Ordered Sets								
LocalOrderedSetsSent	X	X	X	X	X	X	X	X
LocalOrderedSetsReceived	X	X	X	X	X	X	X	X
RemoteOrderedSetsSent	X	X	X	X	X	X	X	X
RemoteOrderedSetsReceived	Х	Х	X	X	X	Х	Х	X
CustomOrderedSetsSent	X	Х	X	X	X	Х	X	X
CustomOrderedSetsReceived	X	X	X	X	X	X	X	X

## **Statistics for 10G MSM modules**

## Statistics for 10G MSM modules

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
Type: User Configurable																							I																					
UserDefinedStat1	X	X	X	x	x		X	X	x	X	X	x	X				x	x	x	x	X	X		X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	Х	X		
UserDefinedStat2	X	X	x	x	x		X	x	X	X	x	X	X				X	X	X	X	X	x		X	X	X				X				X	X	X	X	x	x	х	х	x		
CaptureTrigger	X	X							X	x	x						X	X	x							x	X						X	X	X							x		
CaptureFilter	X	X							X	x	X						x	X	x							x	X							X	X							x		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
StreamTrigger1	X	x	X		X				X Z	X	x	x	x				x	x	x	x		x		X	x z	X								X	x	X		X				X		
StreamTrigger2	X	x	X		X				X Z	X	x	x	X				x	X	x	x		X		X	x z	×								X	x	X		X				х		
Type: States																																												
Link	X	x	X	x	X	X	X	X	X Z	X	x	x	x	X	x	x	x	x	x	x	X	x	x	X	x z	<b>x</b>	х	X	X	X	X	X	X	X	x	X	X	X	X	X	X	X		
LineSpeed	X	X	X	x	X	x	X	X	X Z	X	x	x	X	X	X	X	X	X	X	x	X	X	X	X	X Z	<b>x</b>	X	X	Х	Х	Х	X	X	X	X	X	х	X	X	X	X	x		
DuplexMode				x																	X									X							X							

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	R×M ode BertChannelized	NAME OF THE PARTY	RXModeDCC BVModeWideDacketGroup	NAMOURE MICHELS OUD	Capture	RyDataIntenrity	Designation of the second	Exercise Charling	The state of the s	KXMOdebert Dawy Job of China	RYMODEDERICHALITED	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity		RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
TransmitState	X	X	X	X	x	X	x	X	X	X	X	х	х	X	X	( >	< ×	( >	<b>( )</b>	< x	( <b>&gt;</b>	<b>(</b> )	( <b>&gt;</b>	<b>(</b> >	×	X	х	X	X	2	x	X	x	х	X	х	x	X	X	x	x	x	X		
CaptureState	X	X	X	X	x	X	x	X	X	X	X	х	х	X	X	<b>( )</b>	< ×	( >	<b>(</b> )	< x	( <b>&gt;</b>	<b>( )</b>	( <b>&gt;</b>	<b>(</b> >	×	X	x	x	X		x	X	x	х	X	x	x	X	X	x	x	x	X		
PauseState	X	X	х	X	x	х	x	x	X	x	X	х	х	X	X	<b>( )</b>	< ×	( >	<b>( )</b>	( x	( <b>&gt;</b>	<b>( &gt;</b>	( <b>&gt;</b>	< >	×	X	х	X	X	2	x	X	Х	х	X	X	х	X	x	х	х	х	X		
Type: Common																																													
FramesSent	X	x	X	X	x		x	X	X	X	X	X	x	X	X	< >	< ×	( >	< >	( x	( <b>&gt;</b>	<b>(</b> >	(	<b>\</b>	×	X					x			X	X	x	X	X	x	x	X	x	X		
FramesReceived	X	X	X	X	X		x	X	X	X	X	X	x	X	X	<b>( )</b>	<b>(</b> >	( )	<b>( )</b>	< ×	<b>(</b> >	<b>(</b> )	(	×	X	X					X			Х	x	x	x	X	X	X	x	X	X		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
BytesSent	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	x	X	x	X		x	x	X				X			X	X	X	X	X	X	X	X	X	X		
BytesReceived	X	X	X	x	x		x	X	X	X	X	X	X				X	X	x	x	x	X		x	x	x				X			X	X	X	x	X	x	х	х	X	X		
FcsErrors	X	x	х	X	X		X	x	X	X	X	х	х	X	X	X	X	X	x	X	X	X		x	x	X	X	Х	Х	х	X		X	X	X	X	X	X	Х	X	х	Х		
BitsReceived	x	x	Х	X	X		X	X	x	X	X	х	x				X	X	x	x	X	x		X	X	X	X	Х	X	Х	X		X	X	X	X	X	x	x	x	x	x		
BitsSent	x	X	X	X	X		X	X	X	X	X	X	x	X	X	X	X	X	x	X	X	X		x	x	X	X	Х	X	X	X		X	X	X	X	X	X	Х	X	x	Х		
PortCpuStatus																											X	Х	Х		X		X											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	odinostatete Cod	PyEiretTimeStamn	RySequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSencoreState	PoSExtendedStats
	Х	Х	X		Х			X	Х	Х	Х	Х	X			Х	Х	Х	X	X		X			X	Х								X	X	<b>( )</b>	(	×			Х	Х		Т
PortCpuDodStatus	X	X	X		X			X	x	X	X	X	X			X	X	X	X	x		x			X	X	X	X	X		X		X	X	X	<b>X</b>	(	×			X	X		
Type: Transmit Duration																																												
TransmitDuration	X	X	X	x	X		X	x	x	x	X	X	х	X	x	x	x	x	х	x	Х	x		X	X	x	Х	X	Х	Х	X		X	X	×	<b>X</b>	X	×	X	X	X	X		
Type: Quality of Service																																												
QualityOfService0										X	X	X	X	X	X	X	X																											

	Capture PacketGroup RxDataIntegrity RxFirstTimeStamp RxSequenceChecking RxModeBert RxModeBert RxModeBertChannelized RxModeWidePacketGroup Capture																		St	rea	a m	ı Tı	¹i g	ı g e	er					e C I n E r				М	o d	e D	at	аI	n t e	e g ı	rity	У	Α α	l d - I
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
Type: Checksum Stats																																												
IpPackets																											Х	Х	Х		Х		Х											
UdpPackets																											X	Х	Х		Х		Х											
TcpPackets																											Х	Х	Х		Х		Х											
IpChecksumErrors																											Χ	Х	Х		Х		X											
UdpChecksumErrors																											X	Х	Х		Х		Х											
TcpChecksumErrors																											Χ	Х	Х		Х		Х											
Type: Data Integrity																																												
DataIntegrityFrames			X									X								x																x								
DataIntegrityErrors			X									x								x																х								

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	KxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RyDataIntenrity	RxFirstTimeStamn	RxSequenceChecking	RxModeBert	PyModeBertChannelized	RyModeDcc	RyModeWideDacketGroup	NAMO DE MANAGEMENTO DE LA COMPANSIONE DEL COMPANSIONE DE LA COMPAN	PoSExtendedStats
Type: Sequence Check-ing																																												
SequenceFrames					X								X									x																X						
SequenceErrors					x								×									x																X						
Type: Ethernet																																												
Fragments	X	X	X	x	x		X		<b>x</b> 2	<b>x</b>	x z	<b>x</b> 2	<b>x</b> 2	X	x		x	X	x	X	x	x		x		X				X				X	X	×	X	X	X	X	(	×	<	
Undersize	x	X	X	x	x		X		x 2	X I	x z	<b>x</b> 2	<b>X</b>	X	X		X	X	X	X	X	x		X		X				Х				X	X	×	X	X	X	×	(	×	(	
Oversize																														X														

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
	X	Х	Х	Х	Х		Х		Χ	Х	Х	Х	Х	Χ	Х		Х	Х	Χ	X	Χ	Х		X		X								Х	Х	Х	Х	Х	Х	Х		Х		
VlanTaggedFramesRx	X	X	x	X	X		X		X	x	X	X	X	X	X		X	X	X	X	X	X		X		X				X				X	x	X	x	X	X	x		x		
FlowControlFrames	X	x	x	x	х		X		X	x	X	X	x	X	X		X	x	Х	X	X	X		X		X				х				X	x	X	X	x	х	Х		Х		
Type: Gigabit																																												
SymbolErrorFrames				X																	X									X							X							
SynchErrorFrames				x																	X									х							X							

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	ByDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	By Wode Bert Channelized	PyModeDer	PvWodeDcc PvWodeWideDacketCroup	KXMOdeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
Type: 10/100 + Gigabit																																												I	
SymbolErrors				X																	X									X							X								
OversizeAndCrcErrors	X	x	X	x	x		X		X I	X I	x	x	X	X	X		x	X	X	x	X	x		X		x				X				X	X	X	X	X	X	×	(	×	<		
Type: POS																																													
SectionLossOfSignal						X																	x									X													
SectionLossOfFrame																																													
SectionBip																																													
LineAis																																													

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	KxDataIntegrity	RxSequenceChecking	KAMOdebert Demodebert	by Mode bert Channell Zed	nxmodelecc	Capture	Capture	RxDataIntegrity	Decirettimostamo	RXSequenceChecking	RxModeBert	NAMOURDEI C	KxModeBertChannelized	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Canturo	Dacket Group	rachetter out	KXDataIntegrity DyEigetTimeStamm	KXFIFSUIMEStamp	KxSequenceChecking	KXModeBert	KxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
tionBipSeverlyErroredS- ecs																X																													
Sec- tionLossOfSignalSecs																X																	X												
LineBipErroredSecs																X																	X												
LineReiErroredSecs																x																	x												
LineAisAlarmSecs																X																	X												
LineRdiUnavailableSecs																X																	X												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	KxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	A september of the sept	KXModeBert	RxModeBertChannelized	RxModeDcc PvModeWideDarketCross	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
PathBipErroredSecs																X																X											
PathReiErroredSecs															,	×																X											
PathAisAlarmSecs																x																Х											
PathAisUnavailableSecs																×																х											
PathRdiUnavailableSecs																x																X											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	ByModeBert	PyModeBertChannelized	KXModeDcc	KXModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
InputSignalStrength	X	Х	X		х		X	X	X	X	X	х	X	X	X	>	<b>(</b> )	X Z	x	x		X		X	X	X								x	x	X		X	x	X	Х	X		
PosK1Byte																																												
PosK2Byte																																												
SrpDataFramesRe- ceived																																												
SrpDis- coveryFramesReceived																																												
SrpIpsFramesReceived																																												
SrpParityErrors																																												
SrpUsageFramesRe- ceived																																												
SrpUsageStatus																																												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	KxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Cantiuro		Packetoroup	KXDataIntegrity	KXFIrstIImestamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
SrpUsageTimeouts												T							T		T				T	T					П			Т			Τ								
Type: DCC																																													
DccBytesReceived								X								X								,	X								X									x			
DccBytesSent																																													
DccCrcErrorsReceived								X								×									X								X									x			
DccFramesReceived								X								×									x								X									x			
DccFramesSent																																													
DccFram- ingErrorsReceived																																													

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
Type: BERT																																												
BertStatus						X																	X									X												
BertBitsSent						X																	X									X												
BertBitsReceived						X																	х									Х												
BertBitErrorsSent						X																	X									X												
BertBitErrorsReceived						X																	X									X												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
BertErroredBlocks						x																	х									Х												
BertErroredSeconds						Х																	X									Х												
Ber- tSeverelyErroredSe- conds						X																	X									X												
BertErrorFreeSeconds						X																	X									X												
BertAvailableSeconds						x																	X									X												
Ber-																																X												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	Packetoroup	KXDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
tUnavailableSeconds						X																	X																					
BertBlockErrorState						X																	X									X												
Ber- tBack- groundBlockErrors						X																	X									X												
BertBitErrorRatio						X																	X									X												
Ber- tErroredSecondRatio						X																	X									X												
Ber- tSeverlyErroredSe-						Х																	X									X												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
condRatio									T				Т		Т					П	Т			T																				
Ber- tBack- groundBlockErrorRatio						X																	x									X												
Ber- tNum- berMismatchedOnes						X																	X									Х												
Ber- tMismatchedOnesRatio						X																	X									Х												
Ber- tNum- berMismatchedZeros						X																	X									X												
Ber- tMismatchedZerosRatio						X																	X									x												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	KxSequenceCnecking	RxModeBert	RxModeDcc	RXModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
BertElapsedTestTime						Х																	x								x												
Ber- tUn- framedOutputSignalStrer	ngt	h																																									
Ber- tUn- framedDetectedLineRate																																											
BertDeskewPatternLock																																											
Ber- tRxDeskewErroredFram- es																																											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Pv Mode Bert Channelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
Ber- tRxDeskewEr- rorFreeFrames																																												
Ber- tRxDeskewLossOfFram- e																																												
BertTimeSinceLastError																																												
BertTriggerCount																																												
BertTxDeskewBitErrors																																												
Ber- tTxDeskewErroredFram- es																																												
Ber- tTxDeskewEr- rorFreeFrames																																												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
Type: Service Dis- ruption																																												
Ber- tLastSer- viceDisruptionTime						x																	X									х												
Ber- tMinSer- viceDisruptionTime						x																	X									х												
Ber- tMaxSer- viceDisruptionTime						x																	X									х												
Ber- tSer- viceDisruptionCumulative	è					X																	x									X												
Type: OC192 - Tem-																																												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RySequenceChecking	RxModeBert	Porilogned Attached by Myd	KXMOdebertChannelized	KXModeDcc	KxModeWidePacketGroup	Capture	PacketGroup	KXDataIntegrity	RXFirstTimeStamp	kxsequencechiecking	KxModeBert	RxModeBertChannelized	RxModeDcc	Capture	capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	BySequenceChecking	RxModeBert		KXModeBertChannellZed	RxModeDcc PvModeWideDacketCroum	doo is a service of the service of t	TemperatureSensorsStats	PoSExtendedStats
perature																																														
DMATemperature																																													X	
CaptureTemperature																																													X	
LatencyTemperature																																													X	
Back- groundTemperature																																													Х	
OverlayTemperature																																													Х	
FrontEndTemperature																																													Х	
SchedulerTemperature																																														

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
PlmDevice1In- ternalTemperature																									Ī																			
PlmDevice2In- ternalTemperature																																												
PlmDevice3In- ternalTemperature																																												
FobPort1Fp- gaTemperature																																												
FobPort2Fp- gaTemperature																																												
FobBoardTemperature																																												
FobDevice1In- ternalTemperature																																												
Type: 10 Gig																																												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	PyDataIntourity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
PauseAcknowledge	X	x	x		x		X		X	×	x	x	x	x	X		X	x	X	X		x		x		x								X	×	×		×	X	X		X		
PauseEndFrames	X	X	x		X		X		X	x	x	x	x	x	X		Х	X	X	X		x		X		x								X	×	×		×	X	X		X		
PauseOverwrite	X	X	x		X		x		X	X	x	X	x	X	x		Х	х	X	X		x		x		X								X	X	×		X	X	X		X		
10GigLanTxFp- gaTemperature																																												
10GigLanRxFp- gaTemperature																																												
Cod- ingEr- rorFramesReceived	X	X	x		x				X	X	x	x	x				х	X	X	x		x				x								X	×	×		×				X		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RyDataIntenrity	RxFirstTimeStamn	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats PoSExtendedStats
EEr- rorChar- acterFramesReceived	Х	Х	x		x				x	X	X	X	X				X	X	X	x		x				X								X	x	×		x				X	
DroppedFrames	X	x	X		X				X	X	X	x	X				X	X	X	X		X				X								X	X	X		X				X	
Type: Link Fault Sig- naling																																											
LinkFaultState	X	X	X		X		X		x	X	X	x	X		X		X	x	x	X		X		X		X								X	X	X		X		x		X	
LocalFaults	X	X	X		X		x		X	X	X	x	X		X		X	X	X	x		X		x		X								X	X	×		X		x		X	
RemoteFaults	X	x	X		X		X		X	X	X	x	X		X		X	X	Х	X		X		x		X								X	X	X	7	X		Х		X	

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Canting	a modern	rachetaloup	KXDataIntegrity	KXFIrstlimestamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
Type: RPR																																													_
RprDis- coveryFramesReceived								X																	X																	X			
RprDataFramesRe- ceived								X																	X																	X			
RprFair- nessFramesReceived								X																	X																	x			
RprFairnessFramesSent								X																	X																	X			
RprFairnessTimeouts								X																	X																	X			

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
RprHeaderCrcErrors								X																	X																X			
TOTAL CITE OF S																																												
RprOamFramesRe- ceived								x																	x																X			
RprPayloadCrcErrors								X																	X																X			
RprPro- tectionFramesReceived								X																	x																X			
Type: Ordered Sets																																												
LocalOrderedSetsSent																																												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	PoSExtendedStats
LocalOrderedSet- sReceived	X	X	x		x				<b>x</b>	x	x	x	X				X	X	X	X		X				X								X	х	X		X				X		
RemoteOrderedSet- sSent																																												
RemoteOrderedSet- sReceived	X	X	x		X				X I	x	x	x	x				x	X	X	X		X				X								X	X	X		X				X		
Cus- tomOrderedSetsSent																																												
Cus- tomOrderedSet- sReceived	X	X	X		X				X I	X	x	x	X				x	X	x	X		X				x								X	x	х		X				X		

## **Statistics for ATM Modules**

## Statistics for ATM Modules

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	expatamentry pysogiones/hocking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats
Type: User Con- figurable																																										
UserDefinedStat1	X	X	x	x	x		X	X	x							x	x	X	X	X	X		X	x	X	X	X	X	X	X		X	X	x	x	X	x	X	X	х	X	
UserDefinedStat2	X	X	X	X	X		X	x	X							x	x	X	X	X	X		x	X	x				X				X	X	x	X	X	X	X	х	X	
CaptureTrigger	X								X							X	x								X	X						Х	X								x	
CaptureFilter	X								X							x	x								x	X							X								X	

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	KxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
StreamTrigger1									X								x	x	x	x	,	x		X	X Z	x																X		
StreamTrigger2									X								X	X	x	X		x		X	X Z	x																Х		
Type: States																																												
Link	X	X	X	x	X	X	X	X	X	X	X	x	X	X	x	x	x	x	X	X Z	X Z	X	x	X	X Z	X	X	X	X	x	X	X	X	X	X	X	X	X	X	х	X	х		
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	X	x	X	X	X Z	X Z	X	x	X	X Z	X	Х	X	Х	х	Х	X	X	X	x	X	X	X	X	X	х	х		
DuplexMode				X																	X									X							X							

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
CaptureState	X	X	X	X	X	X	X	X	x	x	X	X	X	X	X	X	X	x	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	x	x	x	x	X		
PauseState	X	X	х	x	X	X	X	X	X	x	X	x	X	X	X	X	x	X	x	X	X	X	X	X	X	X	X	x	X	X	X	X	Х	x	X	x	X	x	X	x	x	x		
Type: Common																																												
FramesSent				X			X	X	x					X	X	X	x				X			X	X	X				X			X				X		x	X	X	X		
FramesReceived				x			X	X	X					X	X	X	X				X			X	X	X				X			X				X		X	X	X	x		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
BytesSent				X			X	X	X					X	X	X	X				X			X	X	X				X			X				X		X	X	X	X		
BytesReceived				x			X	x	X								X				x			X	X	X				X			X				X		X	X	X	X		
FcsErrors	x	X	X	x	X		x	x	x	X	X	X	x	X	x	x	x	X	X	x	x	x		x	X	x	X	x	X	X	X		x	X	×	X	X	X	X	x	x	X		
BitsReceived	x	X	X	X	X		x	X	x								X	X	X	X	X	x		X	X	X	X	х	х	X	X		X	X	×	X	X	X	X	x	X	X		
BitsSent	x	X	X	x	X		x	X	x	X	X	X	x	X	x	x	x	X	X	X	X	x		X	X	X	X	х	Х	X	X		X	X	×	X	X	X	X	x	x	X		
PortCpuStatus																											X	Х	X		X		X											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RyModeDcc	RxModeWidePacketGroup	Capture	DacketGroup	RxDataIntegrity	RxFirstTimeStamn	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	Doctivettimochama	KAFIISUIIIIEStaiiip	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
	Х	Х	Х		Х			X	X	X	Х	Х	Х			Х	X	X	X	X		X			Х	Х									Х	Х	Х		X			Х	Х		
PortCpuDodStatus	X	х	X		X			X	X	X	X	х	Х			×	X	X	×	X		X			X	X	X	X	X			X		X	X	X	X		x			X	X		
Type: Transmit Duration																																													
TransmitDuration	X	х	X	x	X		X	X	x	X	X	х	x	x	X	X	X	X	X	X	X	X		X	X	x	х	X	X	>	(	X		Х	X	X	X	Х	x	X	X	X	Х		
Type: Quality of Service																																													
QualityOfService0										X	X	X	X	x	X	X	X																												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	DyfiretTimoStamp	RxSequenceChecking	RyModeBert		RXModeBertChannelized	RXModeDcc PvModeWideDacketCroun	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	DocEvtondodetate	Posexterioedstats
Type: Checksum Stats																																												
IpPackets																											X	X	Χ		X		X											
UdpPackets																											X	X	Χ		Х		Х											
TcpPackets																											X	Х	Х		Х		Х											
IpChecksumErrors																											X	Х	Χ		Х		Х											
UdpChecksumErrors																											X	X	Χ		Х		Х											
TcpChecksumErrors																											X	X	X		Х		Х											
Type: Data Integrity																																												
DataIntegrityFrames																																				x								
DataIntegrityErrors																																				X								

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	KxDataIntegrity	KXSequenceChecking	KXModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
Type: Sequence Check-ing																																												
SequenceFrames					x																																	X						
SequenceErrors					x																																	X						
Type: Ethernet																																												
Fragments				X			X		X				>	<b>&lt;</b>	X		x				x			X		X				X							X		X	X		X		
Undersize				x			X		X				>	<b>\</b>	x		x				x			X		X				Х							х		X	X		x		
Oversize																														X														

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
				X			Х		X					X	X		X				X			X		Х											Х		Х	Х		Х		
VlanTaggedFramesRx				X			x		X					X	X		X				X			x		X				X							X		X	x		x		
FlowControlFrames				X			X		X					x	x		x				X			X		x				Х							X		X	X		X		
Type: Gigabit																																												
SymbolErrorFrames				X																	X									X							X							
SynchErrorFrames				x																	X									X							X							

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	PyDataInfourity	RyFirstTimeStamn		KXSequence Checking	NAMOUR DE LA COMPANIA DEL COMPANIA DE LA COMPANIA D	KxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
Type: 10/100 + Gigabit																																													
SymbolErrors				X																	x									X							X	,							
OversizeAndCrcErrors				X			X		х					X	х		X				x			X	,	x				X							X		>		×		X		
Type: POS																																													
SectionLossOfSignal						X																	X									X												X	
SectionLossOfFrame																																												X	
SectionBip																																												X	

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
LineAis																																											Х	
LineRdi																																											X	
LineRei																																											X	
LineBip																																											Х	
PathAis																																											X	
PathRdi																																											X	
PathRei																																											X	-
PathBip																																											X	

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
PathLossOfPointer																																											X	
PathPlm																																											X	
SectionBipErroredSecs																x																	X											
Sec- tionBipSeverlyErroredS- ecs																X																	X											
Sec- tionLossOfSignalSecs																x																	X											
LineBipErroredSecs																X																	X											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
LineReiErroredSecs																X																	X											
LineAisAlarmSecs																x																	Х											
LineRdiUnavailableSecs																x																	Х											
PathBipErroredSecs																x																	Х											
PathReiErroredSecs																X																	X											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	0.11416	a modern	Packeteroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
PathAisAlarmSecs																X																	X												
PathAisUnavailableSecs																X																	X												
PathRdiUnavailableSecs																x																	X												
InputSignalStrength							X	X	Х					X	X		X							x	X	x														X	x	Х	X		
PosK1Byte																																													
PosK2Byte																																													
SrpDataFramesRe- ceived																																													

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	DarketGroup	RxDataIntegrity	DvEiretTimoStamn	RxSequenceChecking	RxModeBert		RXModeBertChannellZed PvModeDcr	RxModeWidePacketGroup	Capture	DackotGroun	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedState	
SrpDis- coveryFramesReceived																																												Π
SrpIpsFramesReceived																																												
SrpParityErrors																																												
SrpUsageFramesRe- ceived																																												
SrpUsageStatus																																												
SrpUsageTimeouts																																												
Type: DCC																																												
DccBytesReceived								X								X									X	(							X								x			
DccBytesSent																																												
DccCrcErrorsReceived																																	X											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
								X								Χ									X																Х			
DccFramesReceived								X								x									X								X								X			
DccFramesSent																																												
DccFram- ingErrorsReceived																																												
Type: BERT																																												
BertStatus						X																	X									X												
BertBitsSent						X																	X									X												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	DarketGroun	RxDataIntegrity	ovejettimostama	RxSequenceChecking	ByModeBert	KXMOdebert	RxModeBertChannelized	RxModeWidePacketGroup	Capture	PacketGroup	 RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
BertBitsReceived						x																	×	(								x												
BertBitErrorsSent						X																	×	(								X												
BertBitErrorsReceived						X																	×	(								X												
BertErroredBlocks						X																	×	(								x												
BertErroredSeconds						x																	×	(								Х												
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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	DacketGroup		KXDataintegrity	KXFIrstIIImestamp	RxSequenceChecking	KxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
tSeverelyErroredSe- conds						Х				Ī													X																	I					
BertErrorFreeSeconds						x																	X									X													
BertAvailableSeconds						x																	X									X													
Ber- tUnavailableSeconds						x																	X									X													
BertBlockErrorState						x																	X									X													
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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
groundBlockErrors																																												
BertBitErrorRatio						X																	x									x												
Ber- tErroredSecondRatio						X																	x									Х												
Ber- tSeverlyErroredSe- condRatio						X																	x									X												
Ber- tBack- groundBlockErrorRatio						X																	X									X												
Ber- tNum- berMismatchedOnes						X																	x									х												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
Ber- tMismatchedOnesRatio						x																	X									Х												
Ber- tNum- berMismatchedZeros						x																	x									Х												
Ber- tMismatchedZerosRatio						x																	X									X												
BertElapsedTestTime						x																	X									X												
Ber- tUn- framedOutputSignalStrer	ngti	h																																										

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
Ber- tUn- framedDetectedLineRate										Ī																																		
BertDeskewPatternLock																																												
Ber- tRxDeskewErroredFram- es																																												
Ber- tRxDeskewEr- rorFreeFrames																																												
Ber- tRxDeskewLossOfFram- e																																												
BertTimeSinceLastError																																												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	PyModeDec	B×ModeWideBacketCromp	Contract of the contract of th	a dolore	RyDataIntegrity	DyfietTimoCt	RXFIIIST IIMESTAMP  RYSequence Checking	Designation of the second	KXModebert	KXModeBertChannelized	Powodeboc Powodewidebacketorum	Capture	 PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup		expataintegrity	KXFIrstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
BertTriggerCount																																													
BertTxDeskewBitErrors																																													
Ber- tTxDeskewErroredFram- es																																													
Ber- tTxDeskewEr- rorFreeFrames																																													
Type: Service Dis- ruption																																													
Ber- tLastSer- viceDisruptionTime						x																	>	<								X													
Ber-																																Х													

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
tMinSer- viceDisruptionTime						Х																	Х																					
Ber- tMaxSer- viceDisruptionTime						X																	x									X												
Ber- tSer- viceDisruptionCumulative	ž					X																	X									X												
Type: 10 Gig																																												
PauseAcknowledge							X		x					x	X		X							x		×													x	X		X		
PauseEndFrames							X		X					X	X		X							x		×													X	X		X		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSFxtendedStats	
PauseOverwrite							X		x					X	x		Х							x		x													х	x		х		
10GigLanTxFp- gaTemperature																																												
10GigLanRxFp- gaTemperature																																												
Cod- ingEr- rorFramesReceived									x								x									x																x		
EEr- rorChar- acterFramesReceived									x								x									x																X		
DroppedFrames									x								X									X																X		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Canture	DacketGroun	decision and a second	exparaintegrity	KKFIFSUIMEStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
Type: ATM																																													
AtmAal5BytesReceived	X	X	X		X					X	X	X	X					X	X	X		X					X	X	X		X			X	<b>X</b>		<		X						
AtmAal5BytesSent	x	х	X		X					X	x	X	X					x	X	х		х					Х	Х	Х		X			X	: ×		<		X						
AtmAal5Cr- cErrorFrames																																													
AtmAal5FramesRe- ceived	X	X	x		X					x	x	X	X					x	X	X		X					X	X	X		X			X	<b>X</b>	( )	<b>&lt;</b>		x						
AtmAal5FramesSent	X	X	X		X					X	x	X	X					x	X	X		X					Х	X	X		X			X	×	( )	<		X						
AtmAal5LengthEr-																																													

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Cantiure	O softon	document of the second	KxDataIntegrity	KxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
rorFrames																																													
AtmAal5TimeoutEr- rorFrames																																													
AtmCellsReceived	X	X	X		X					X	X	X	X					x	X	X		X					X	X	X		X			×	<b>X</b>	( )	x		x						
AtmCellsSent	x	х	Х		х					x	х	X	X					x	X	х		x					Х	Х	Х		X			×	<b>X</b>		×		x						
AtmCor- rectedHcsErrorCount	x	x	X		X					X	x	x	X					X	X	X		X					Х	X	X		X			×	· >	( )	X		X						
AtmIdleCellCount	x	x	х		x					X	x	x	X					X	X	x		X					Х	Х	х		X			×	<b>X</b>		×		x						
AtmScheduledCellsSent																											X	Х	X		X														

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
	Х	Х	X		х					X	X	Χ	Х					Х	Х	Х		Х												Х	Х	Х		Х						Г
AtmUn- correctedHcsErrorCount	X	X	X		X					X	x	X	X					X	X	X		X					X	X	X		X			X	X	X		X						
AtmUn- registeredCell- sReceived	x	X	Х		X					X	X	X	x					x	X	X		x					X	X	X		X			X	x	x		x						
EthernetCrc	X	X	X		X					X	X	X	X					X	X	X		x					X	X	x		X			X	X	x		X						
Type: Link Fault Sig- naling																																												
LinkFaultState							X		X						X		x							X		X														X		x		

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	DVM odobort	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
LocalFaults							x		X						x		X							x		X														X		x		
RemoteFaults							X		X						x		X							X		x														X		x		
Type: RPR																																												
RprDis- coveryFramesReceived								X																	x																X			
RprDataFramesRe- ceived								X																	x																X			
RprFair- nessFramesReceived								X																	X																X			

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	KxDataIntegrity	RxSequenceChecking	KAMOdebert	Exmode Bertonannelized	By Mode Wide Backet Cross	KXModeWidePacketsioup	Capture	PacketGroup	RXDatamtegrity	RXFIrst limeStamp BySequenceChecking	## do Po ## d	KXModeBert	RxModeBertChannelized	RXModeDcc PyModeWideDacketCroun	Capture	 PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
RprFairnessFramesSent								X																>	<															x			
RprFairnessTimeouts								X																>	<															X			
RprHeaderCrcErrors								X																>	<															X			
RprOamFramesRe- ceived								X																>	<															x			
RprPayloadCrcErrors								X																>	<															X			
RprPro-																																											

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	PySoquoncoChocking	RxModeBert	Rx Mode Bert Channelized	NAMOGEDEI CONSTITUENTE DE CONS	KXModeDcc	RxModeWidePacketGroup	PoSExtendedStats
tectionFramesReceived								X																	X																>	Κ		
Type: Ordered Sets																																												
LocalOrderedSetsSent									X								X									X																>	X	
LocalOrderedSet- sReceived									X								X									X																>	X	
RemoteOrderedSet- sSent									X								X									X																>	X	
RemoteOrderedSet- sReceived									x								X									X																>	×	
Cus-																																												

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	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	DyModeBort	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PoSExtendedStats	
tomOrderedSetsSent									X								X									X																Χ		
Cus- tomOrderedSet- sReceived									X								X									x																X		

## **Statistics for PoE Modules**

Statistics for PoE Modules

Type: PoE	
PoeStatus	X
PoeInputVoltage	X
PoeInputCurrent	X
PoeInputPower	X
PoeActiveInput	X
PoeTemperature	X
PoeAutocalibration	X

#### Statistics for 10/100/1000 AFM

	Single Mode
Type: AFM	
bytesFromApplication	X
packetsFromApplication	X
monitorBytesFromPort2	X
monitorBytesFromPort3	X
monitorPacketsFromPort2	X
monitorPacketsFromPort3	x

#### Statistics for IxNetwork

	Additional Modes							
	Pro- tocolServerStats	ArpStat- s	Icm- pStats					
Type: Protocol Server - General								
ProtocolServerTx	X							
ProtocolServerRx	X							
TxArpReply		X						
TxArpRequest		X						
TxPingReply			X					
TxPingRequest			X					
RxArpReply		X						
RxArpRequest		X						
RxPingReply			X					
RxPingRequest			X					
Pro- tocolServerVlanDroppedFrames	Х							

	Additional Modes							
	Pro-	ArpStat-	Icm-					
	tocolServerStats	s	pStats					
ScheduledFramesSent								
AsynchronousFramesSent								
PortCPUFramesSent								

## **Ethernet OAM Statistics**

Ethernet OAM statistics are capable of being generated for the load modules listed in the following table.

Ethernet OAM Statistics

Et	nerne	t UAN	1 Stat					
			Ethe	ernet	OAM S	tats		
	OAM Information PDUs Sent	OAM Information PDUs Received	OAM Event Notification PDUs Received	OAM Event Notification PDUs Received	OAM Organization PDUs Received	OAM Variable Request PDUs Received	OAM Variable Response PDUs Received	OAM Unsupported PDUs Received
Load Module								
10/100/1000 (S)TX(S)2, 4, 24	X	X	X	x	x	x	x	x
1000 SFP(S)4	X	X	X	Х	Х	X	X	Х
10/100/1000 XMS(R)12	X	X	X	X	X	X	X	X
10/100/1000 LSM XMV(R)4, 16	X	X	X	X	X	X	X	X
10/100/1000 ASM XMV12	X	X	X	X	X	X	X	Х
10GE LSM (XM3, XMR3, XL6) in LAN mode	X	X	X	X	X	X	X	X
10GE LSM (XM8, XMR8, XM4, XMR4) in LAN mode	X	X	X	X	X	X	X	X
10GE LSM (XFP, XENPAK, X2, 10GBase-T) in LAN mode	X	X	X	X	X	X	X	X
10G MSM in LAN mode	X	X	X	X	Х	X	X	Х
10GE LSM MACSec LAN mode	X	Х	X	X	X	X	X	X

#### **MACsec Statistics**

MACsec statistics can be generated for the LSM10GMS load module and are listed in the following table. For details, see *IEEE standard 802.1 AE-2006, Media Access Control (MAC) Security*.

**MACsec Statistics** 

Statistic Type	Name	Description
MACSec Valid Frames Sent	macSecValidFramesSent	32-bit stat counter that indicates the total number valid MACSEC packets transmitted
MACSec Valid Bytes Sent	macSecValidBytesSent	64-bit stat counter that indicates the total numbre valid MACSEC bytes transmitted
MACSec Frames With Unknown Key Sent	macSecFramesWithUnknownKeySent	32-bit stat counter that indicates the total number of transmit packets for which no key was found
MACSec Valid Frames Received	macSecValidFramesReceived	32-bit stat counter that indicates the total number valid MACSEC packets received
MACSec Valid Bytes Received	macSecValidBytesReceived	64-bit stat counter that indicates the total numbre valid MACSEC bytes received
MACSec Frames With Unknown Key Received	macSecFramesWithUnknownKeyReceived	32-bit stat counter that indicates the total number of receive packets for which no key was found
MACSec Frames With Bad Hash Received	macSecFramesWithBadHashReceived	32-bit stat counter that indicates the total number of receive packets with a bad ICV

## **FCoE Statistics**

FCoE statistics can be generated for the NGY LSM10GXM family of load modules and are listed in the following table.

FCoE Statistics

Statistic Type	Name
FCoE Fabric Login sent	fcoeFlogiSent
FCoE Fabric	fcoeFlogiLsAccReceived

Statistic Type	Name			
Login Link Ser- vice Accept received				
FCOE Port Login sent	fcoePlogiSent			
FCOE Port Login Link Ser- vice Accept received	fcoePlogiLsAccReceived			
FCOE Port Login Requests received	fcoePlogiRequestsReceived			
FCoE Fabric Logout sent	fcoeFlogoSent			
FCOE Port Logout sent	fcoePlogoSent			
FCOE Port Logout received	fcoePlogoReceived			
FCoE Dis- covery sent.	fcoeFdiscSent			
FCoE Dis- covery Link Service Accept received	fcoeFdiscLsAccReceived			
FCoE Name Server Regis- tration sent	fcoeNSRegSent			
FCoE Name Server Regis- tration suc- cessful	fcoeNSRegSuccessful			
FCoE Nx Ports Enabled	fcoeNxPortsEnabled			
FCoE Nx Port IDs Acquired	fcoeNxPortIdsAcquired			
FCoE Rx	fcoeRxSharedStat1			

Statistic Type	Name
Shared Stat 1	
FCoE Rx Shared Stat 2	fcoeRxSharedStat2

#### fcoeRxSharedStat1 and fcoeRxSharedStat2

Select the statistic to be assigned to these two counters from these options:

statFcoeInvalidDelimiter
statFcoeInvalidFrames
statFcoeInvalidSize
statFcoeNormalSizeBadFccRc
statFcoeNormalSizeGoodFccRc
statFcoeUndersizeBadFccRc
statFcoeUndersizeGoodFccRc
statFcoeValidFrames

#### **FIP Statistics**

FIP statistics can be generated for any load module capable of FCoE and are listed in the following table.

**FIP Statistics** 

Statistic Type	Name					
Number of FIP Discovery Solicitations that have been sent	FipDiscoverySolicitationsSent					
Number of FIP Discovery Advertisements that have been received.	FipDiscoveryAdvertisementsReceived					
Number of FIP Keep Alives that have been sent.	FipKeepAlivesSent					
Number of FIP Clear Virtual Links that have been received.	FipClearVirtualLinksReceived					

## **ALM, ELM and CPM Statistics**

Statistics generated for ALM1000T8 and ELM1000ST2 load modules are listed in the following table.

#### Statistics for 10/100/1000 ALM T8, ELM ST2, and CPM T8

		Additional Statistics								
	Common	ArpStats	DHCPv4Stats	DHCPv6Stats	TempSensors Stats					
Link State	X									
Line Speed	X									
Duplex Mode	X									
Frames Sent	X									
Valid Frames Received	x									
Bytes Sent	X									
Bytes Received	X									
Fragments	X									
Undersize	X									
Oversize and Good CRCs	x									
CRC Errors	Х									
Alignment Errors	x									
Dribble Errors	Х									
Collisions	X									
Late Collisons	X									
Collision Frames	X									
Excessive Collision Frames	х									
Oversize and CRC Errors	х									
ProtocolServer Transmit	х									
ProtocolServer Receive	х									
Transmit ARP Reply		x								
Transmit ARP		X								

		Additional Statistics									
	Common	ArpStats	DHCPv4Stats	DHCPv6Stats	TempSensors Stats						
Request											
Transmit Ping Reply	x										
Transmit Ping Request	x										
Receive ARP Reply		x									
Receive ARP Request		X									
Receive Ping Reply	x										
Receive Ping Request	x										
Bits Sent	X										
Bits Received	Х										
Central Chip Temperature (C)					X						
Port Chip Tem- perature (C)					X <sup>1</sup>						
Port CPU Status	x										
Port CPU DoD Status	x										
DHCPv4 Dis- covered Mes- sages Sent			X								
DHCPv4 Offers Received			x								
DHCPv4 Requests Sent			X								
DHCPv4 ACKs Received			X								
DHCPv4 NACKs			Х								

		Additional Statistics									
	Common	ArpStats	DHCPv4Stats	DHCPv6Stats	TempSensors Stats						
Received											
DHCPv4 Releases Sent			x								
DHCPv4 Enabled Inter- faces			X								
DHCPv4 Addresses Learned			X								
DHCPv6 Solicits Sent				x							
DHCPv6 Advert- isements Received				Х							
DHCPv6 Requests Sent				x							
DHCPv6 Declines Sent				x							
DHCPv6 Replies Received				x							
DHCPv6 Releases Sent				x							
DHCPv6 Enabled Inter- faces				Х							
DHCPv6 Addresses Learned				Х							

<sup>&</sup>lt;sup>1</sup>Not ELM (ALM and CPM only)

# 40/100 GE Statistics

Statistics for 40/100GE LSM Modules

Statistics to			mal				0 S		
	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	TemperatureSensorsStats
Type: User Configurable									
UserDefinedStat1	X	X	X	X	X	X	X	X	
UserDefinedStat2	X	Х	Х	Х	Х	Х	Х	Х	
UserDefinedStatByteCount1									
(supported only on Lava AP40/100GE 2P	X	X	X	X	X	X	X	X	
UserDefinedStatByteCount2									
(supported only on Lava AP40/100GE 2P	X	X	X	X	X	X	X	X	
CaptureTrigger	X	Х	Х	Х	Х	Х	Х	Х	
CaptureFilter	X	Х	Х	Х	Х	X	Х	X	
StreamTrigger1	X	Х	Х	Х	Х	X	Х	X	
StreamTrigger2	X	Х	Х	Х	Х	Х	Х	X	
UserDefinedStat5	X	Х	Х	Х	Х	Х	Х	X	
UserDefinedStat6	X	Х	Х	Х	Х	Х	Х	X	
Type: States									
Link	X	X	Х	X	Х	Х	X	X	
LineSpeed	X	Х	Х	Х	Х	Х	Х	Х	
TransmitState	X	Х	Х	Х	Х	Х	Х	Х	
CaptureState	X	Х	Х	Х	Х	Х	Х	Х	
PauseState	X	Х	Х	Х	Х	Х	Х	Х	
Type: Common									

		Nor	m a l			Q	0 S		
	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	TemperatureSensorsStats
FramesSent	Х	Х	Х	Х	Х	Х	Х	Х	
FramesReceived	Х	Х	Х	Х	Х	Х	Х	Х	
BytesSent	Х	Х	Х	Х	Х	Х	Х	Х	
BytesReceived	Х	Х	Х	Х	Х	Х	Х	Х	
FcsErrors	Х	Х	Х	Х	Х	Х	Х	Х	
BitsReceived	Х	Х	Х	Х	Х	Х	Х	Х	
BitsSent	Х	Х	Х	Х	Х	Х	Х	Х	
PortCpuStatus	Х	Х	Х	Х	Х	Х	Х	Х	
PortCpuDodStatus	Х	Х	Х	Х	Х	Х	Х	Х	
ScheduledTransmitTime	Х	Х	Х	Х	Х	Х	Х	Х	
Type: Transmit Duration									
TransmitDuration	Х	Х	Х	Х	Х	Х	Х	Х	
Type: Quality of Service									
QualityOfService 0-7					Х	Х	Х	Х	
Type: Checksum Stats									
IPv4Packets	Х	Х	Х	Х	Х	Х	Х	Х	
UdpPackets	Х	Х	Х	Х	Х	Х	Х	Х	
TcpPackets	Х	Х	Х	Х	Х	Х	Х	Х	
IPv4ChecksumErrors	Х	Х	X	Х	Х	Х	Х	Х	
UdpChecksumErrors	Х	Х	Х	Х	Х	Х	Х	Х	
TcpChecksumErrors	Х	Х	Х	Х	Х	Х	Х	Х	
Type: Data Integrity									
DataIntegrityFrames		Х				Х			
DataIntegrityErrors		Х				Х			

		Nor	mal			Q	0 S		
	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	TemperatureSensorsStats
Type: Sequence Checking									
SequenceFrames			Χ				X		
SequenceErrors			Χ				X		
ReverseSequenceErrors			Χ				X		
SmallSequenceErrors			Χ				Х		
TotalSequenceErrors			Χ				Х		
BigSequenceErrors			Х				Х		
Type: Ethernet									
Fragments	Х	Х	Х	Х	Х	Х	Х	Х	
Undersize	Х	Х	Х	Х	Х	Х	Х	Х	
Oversize	Х	Х	Х	Х	Х	Х	Х	Х	
VlanTaggedFramesRx	Х	Х	Χ	Х	Х	Х	Х	Х	
FlowControlFrames	Х	Χ	Χ	Х	Х	Х	Х	Х	
Type: Temperature									
PCPU FPGA Temperature									Х
Capture1 Fpga Temperature									Х
Capture2 Fpga Temperature									Х
Tx1 Fpga Temperature									Х
Tx2 Fpga Temperature									Х
Latency1 Fpga Temperature									Х
Latency2 Fpga Temperature									Х
TxSchedulerOverlay Temperature									Х
TxFmx Fpga Temperature									Х
RxFmx Fpga Temperature									Х

		Nor	m a l			Q	0 S		
	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	TemperatureSensorsStats
Type: Pause									
PauseEndFrames									
PauseOverwrite	X	Х	Χ	Х	Х	Х	Х	Χ	
Type: Gigabit									
Oversize and CRC Errors	Х	Х	Х	Х	Х	Х	Х	Х	
Type: POS									
Input Signal Strength	Х	Х	Х	Х	Х	Х	Х	Х	
Type: ARP									
TxArpReply	Х	Х	Х	Х	Х	Х	Х	Х	
TxArpRequest	X	Х	Х	Х	Х	Х	Х	Х	
RxArpReply	Х	Х	Х	Х	Х	Х	Х	Х	
RxArpRequest	Х	Х	Х	Х	Х	Х	Х	Х	
Type: ICMP									
TxPingReply	Х	Х	Х	Х	Х	Х	Х	Х	
TxPingRequest	Х	Х	Х	Х	Х	Х	Х	Х	
RxPingReply	Х	Х	Х	Х	Х	Х	Х	Х	
RxPingRequest	Х	Х	Х	Х	Х	Х	Х	Х	
ScheduledFramesSent	Х	Х	Х	Х	Х	Х	Х	Х	
AsynchronousFramesSent	Х	Х	Х	Х	Х	Х	Х	Х	
PortCPUFramesSent	Х	Х	Х	Х	Х	Х	Х	Х	
Type: Protocol Server-General									
ProtocolServerTx	X	Х	Х	Х	Х	Х	Х	Х	
ProtocolServerRx	Х	Х	Х	Х	Х	Х	Х	Х	

		Nor	mal			Q	0 S		
	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	TemperatureSensorsStats
ProtocolServerVlanDroppedFrames	x	х	Х	х	х	Х	х	х	
Type: Link Fault Signaling									
LinkFaultState	Х	Χ	X	X	Х	Χ	Χ	Χ	
LocalFaults	Х	Χ	X	Χ	Х	Χ	Χ	Χ	
RemoteFaults	Х	Χ	Χ	Χ	Х	Χ	Χ	Х	
Type: LSM									
codingErrorFramesReceived	Х	Χ	X	Х	Х	X	Χ	Х	
eErrorCharacterFramesReceived	Х	Χ	X	Х	Х	X	Χ	Х	
Type: PCS									
PcsSyncErrorsReceived	Х	Х	X	Х	Х	X	Χ	Х	
PcsIllegalCodesReceived	Х	Χ	X	Х	Х	X	Χ	Х	
PcsRemoteFaultsReceived	Х	Χ	X	Х	Х	X	Χ	Х	
PcsLocalFaultsReceived	Х	Χ	X	Χ	Х	X	Χ	Х	
PcsIllegalOrderedSetReceived	Х	Х	Χ	Χ	X	X	Х	Х	
PcsIllegalIdleReceived	Х	Х	Χ	Х	X	X	Х	Х	
PcsIllegalSofReceived	Х	Χ	X	Χ	Х	X	Χ	Х	
PcsOutOfOrderSof Received	Х	Х	X	Х	Х	X	Х	Х	
PcsOutOfOrderEof Received	Х	Х	Х	Х	Х	Х	Х	Х	
PcsOutOfOrderData Received	Х	Х	Х	Х	Х	Х	Х	Х	
PcsOutOfOrderOrderedSetReceived	x	х	x	х	х	x	х	х	
TotalFrames	Х	Х	Х	Х	Х	Х	Х	Х	
ReadTimeStamp	Х	Х	X	Х	Х	Х	Х	Х	

		Normal			Qos				
	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	TemperatureSensorsStats
Type: Latency/Jitter									
MinLatency	X	Χ	X	X	X	X	X	X	
MaxLatency	X	Χ	X	X	X	X	X	X	
MaxminInterval	Х	X	Χ	X	Х	Χ	Х	X	
AverageLatency	Х	Χ	Χ	Х	Х	Х	Х	Х	
TotalByteCount	Х	Χ	Χ	X	Х	Χ	X	X	
BitRate	Х	Х	Х	Х	Х	Х	Х	X	
ByteRate	Х	Х	Х	Х	Х	Х	Х	X	
FrameRate	Х	Х	Х	Х	Х	Х	Х	X	
FirstTimeStamp	Х	Х	Х	Х	Х	Х	Х	X	
LastTimeStamp	Х	Х	Х	Х	Х	Х	Х	Х	



## **Appendix C: GPS Antenna Installation Requirements**

Ixia GPS equipped systems used to provide local Stratum 1 timing signals requires the installation of a GPS antenna kit (942-0003 or 942-0005, where the facility or environment prevent the window mount antenna from functioning). This section describes the installation method we recommend for an IXIA GPS Antenna. This section also provides a scheme for installation of lightning protection for an installed antenna. In order to ensure that all of the following criteria in this manual can be met, we recommend a site survey.

CAUTION	This is not an installation manual and should not be used in place of building codes for electronic installations applicable to specific sites.
ATTENTION	Ce manuel n'est pas un manuel d'installation et ne doit pas être utilisé à la place des normes de construction pour les installations électroniques qui s'appliquent à des sites spécifiques.

This appendix has the following sections:

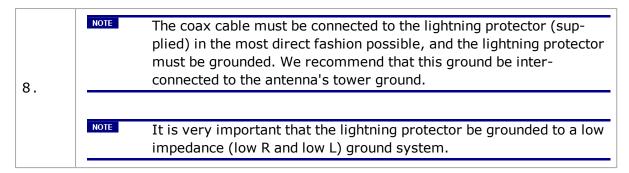
- Roof Mount Antenna
- Window Mount Antenna

#### **Roof Mount Antenna**

The general location requirements for installation of the GPS antenna and conduit are:

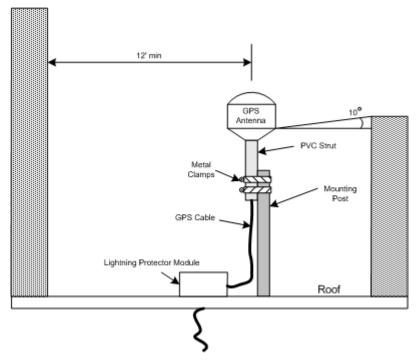
#### GPS Location Requirements

	or a Location Requirements
1.	Ideally, a roof area with an unobstructed 360-degree view of the sky above the horizon. At the minimum, a 180-degree view of the sky is required.
2.	Mounted away from and above a plane from items such as elevators, air conditions and other machinery.
3.	Should have the best view of the horizon that is possible. No obstructions should be within a ten-degree angle from the horizontal.
4.	There should be adequate space available on the roof to install two antennas with an absolute minimum of 10 feet between antennas.
5.	The antenna should be 12 feet away from metallic objects.
6.	Sufficient access to the roof for installation of the GPS conduit/mast and antenna.
7.	Permission to run a 2-inch PVC conduit from the GPS antenna on the roof to the building entrance point.



One possible installation is shown in the following figure.

Figure: GPS Installation Requirements



The following items are included as part of the Ixia package:

- The GPS Antenna
- GPS Cables (1 long and 1 short)
- · Lightning Protector
- The PVC Strut
- · Two metal clamps

The placement and construction illustrate many of the recommendations found in this section.

#### **Conduit**

We recommend the coax from the GPS antenna to the Ixia unit to be installed in a secure conduit from the point directly above the chassis to the GPS antenna. The conduit serves two purposes:

- 1. It protects the coax cable.
- 2. It provides a rigid mast on which the GPS can be mounted.

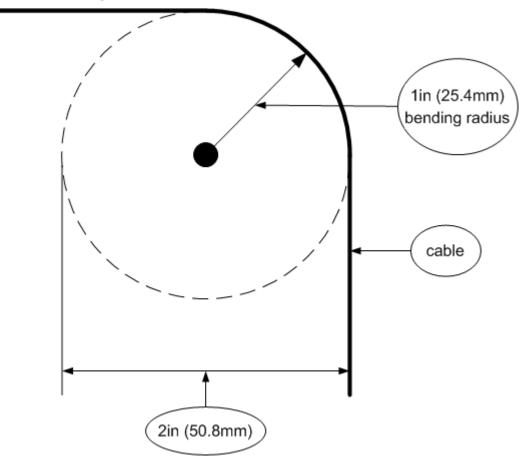
#### **Conduit Type**

The GPS conduit should be 2-inch PVC. Installation of the coaxial cable is uncomplicated within the pipe. There should be no more than four 90-degree bends between pull boxes.

#### **Coaxial Bending Radius**

The coaxial cable should be run as straight as possible to meet the manufacturer phase stability. The coaxial cable may have a greater than 1in (25.4 mm) bending radius.

Figure: Coaxial Bending Radius



In order to go around a corner a conduit that has less than the required bending radius, it would be necessary to use either a junction box with an accessible elbow installed at each 90-degree turn or two 45-degree elbow connected with a piece of straight pipe. A 2-inch conduit only requires one 90-degree elbow to make the correct bending radius around a 90-degree turn.

## **Lightning Protection**

**Lightning protection for the installation is required.** The lightning protector must be correctly grounded to function properly. It must be connected to a low impedance (low R and low L) ground system. We recommend that this ground be interconnected to the tower ground and power ground to form one system.

When attaching to the grounding stud (M8), use a maximum of 88.5 lbf-in. (10 N-m) of torque.

The earth ground electrode should be driven in at least 8 ft. (2.44m) into the earth. A #6 grounding wire should be used.

## **GPS Mast Location Requirements**

#### **Preferred Location**

The preferred mounting location for the GPS antenna is an unobstructed 360-degree view of the sky above the horizon. The specific requirements are:

GPS Mast Preferred Location Requirements

1.	Optimal view of the sky.
2.	Not the highest point of the building so as to reduce the possibility of lightning strikes.
3.	Located at least 12 ft. from any large metal objects.
4.	Located at least 10 ft. from any other GPS antenna.
5.	Located within 30 ft. of where the coax cable enters the building.
6.	The GPS antenna mast should be mounted at least 4 feet higher than the highest horizontal <b>reflective surface</b> such as roof top mounted AC units.

## **Requirements if Preferred Location is Not Available**

If an unobstructed 360-degree view of the sky is not available then the following requirements should be met:

GPS Mast Location Requirements if a Preferred Location is not Available

1.	300-degree azimuth view of the sky.
2.	No vertical obstructions to obscure the view of the antenna from the horizon for more than 10 degrees.
3.	No high-power radar signal beamed directly at the unit; this may damage the pre-amplifier in the antenna.
4.	No harmonics from a high-power, broad band transmitter within a few megahertz of the carrier frequency (1.575 GHz) should be present. This may jam the GPS receiver.

## **Window Mount Antenna**

The GPS chassis kit includes a window mount antenna. This antenna is capable of operation in areas with a relatively unrestricted view of the sky, and low background interference from other radiators.

## **Mounting**

Mount the antenna on the metal frame of the window. The antenna should be no lower than the lower edge of the glass. A 180-degree view of the sky is preferred, with no buildings

adjacent to the window.

In the absence of a metal window frame, a nine centimeter square metal plact can be used to mount the antenna in a position above the window sill.



## **Appendix D: Hot-Swap Procedure**

Each Optixia chassis provides the ability of removing and reinstalling a Load Module without requiring the removal of power from the rest of the chassis. The process of removing/installing a Load Module does not impact either the operation of the OS or load modules installed in the chassis. The following features are part of the installation/removal process:

- Remove Notification sent to you through IxServer and IxExplorer
- · No impact on tests operating on other cards
- Safe power application/removal from the card interface

Legacy modules installed in the SFF adapter module can also be hot-swapped.

The following guidelines should be applied when hot-swapping modules:

- Modules can be hot-swapped in and out of a chassis without impacting server operation only if they are not currently being used to run a test.
- Do not add or remove more than one module at a time.
- Do not add or remove modules during IxServer start up wait until LCD display shows `Server OK.'
- `In Use' LED indicates the module is currently owned by an application. This is to warn of hot-swapping conflicts.

## **Load Module Hot-Swap Insertion**

The process of insertion of a Load Module causes the slot location to apply power to the Load Module and determine that there is no immediate fault condition. The presence of a Load Module in a slot is flagged to IxServer. Upon recognition of a Load Module's presence, IxServer determines if the Load Module is a supported type. All supported types shall be loaded automatically. In all cases, once IxServer has determined the presence of a Load Module in a slot, IxExplorer represents the Load Module as present and advertises the type. For unsupported Load Modules, the module type is shown and is indicated as unsupported in the IxExplorer GUI as long as it resides in a slot.

To insert a load module:

- 1. Carefully slide the load module along the chassis slot runners until it clicks into place. Ensure that it is firmly connected to the backplane.
- 2. Secure the holding screws. Be careful not to over tighten the screws.

NOTE

You should not hot-swap more than one load module at a time into a powered Optixia chassis.

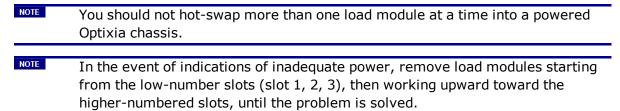
## Load Module Hot-Swap Removal

The removal of a load module does not impact the operation of other Load Modules in the chassis with respect to power or independent operation. In the event that an application is using the Load Module, the application operations for that Load Module are terminated and a message is sent to you. In the event that inter-board operations are enabled, the other

Load Modules interfacing the removed Load Module are notified of its absence and are instructed to terminate operations to the removed Load Module.

#### To remove a load module:

- 1. Loosen the holding screws.
- 2. Disconnect the load module from the backplane and remove it from the chassis. Be sure to use correct ESD handling procedures at all times.



# Appendix E: IP Port Assignments on Ixia Chassis and Linux port CPUs

## **Applicability**

The information in this bulletin applies to:

- · All Ixia chassis
- · All Load Modules with embedded Linux port CPUs

#### **Services on Ports**

The following table lists the services assigned to IP ports on Ixia chassis and port CPUs as of May 10, 2012. Services listed in the Used on Chassis column are accessed through the chassis management port (the NIC located in the rear of the chassis). Services listed in the Used on Port CPU column are accessed through the test ports.

Do not expose any port on an Ixia chassis to an untrusted network.

Connections are initiated in the following directions:

#### Port Directions

Port	Direction
2809-2825	client<>chassis
2809-2825	client<>chassis
All others	client ->chassis

Services assigned to Ports

Port	Use	ТСР	UDP	Used on Chassis	Used on Port CPU	IxOS 5.30 and later
9	Discard service	X	X		X	X
21	FTP daemon	X				X
22	SSH (IxLoad)	X		X		
23	Telnet daemon	X			X	X
58	Reserved	X			X	X
67	Dnsmasq		X			X
68	Dhclient		X			X
80	HTTP, License Management, IxSAN	X		X (IxSAN)	x	x
103	PIM daemon	X	X		X	X

Port	Use	ТСР	UDP	Used on Chassis	Used on Port CPU	IxOS 5.30 and later
	(test port only)					
111	Sun RPC portmap	X	X	X		X
123	NTP		X	X	X	X
125	Private NTP		X	X		X
135	Windows COM ser- vices	X	X	x		x
179	BGP daemon (test port only)	x			x	х
445	Windows COM ser- vices	x	X	x		x
797-800	NFS mounts		X		X	X
998		Х				X
999		X				X
1000		X	X			X
1024	Windows MStask.exe (Google for 'mstask vul- nerability' for details)	x	X	X		X
1080	SOCKS proxy	X		X		Х
2048	Service man- agement	X		x	х	
2049	NFS	X	Х	X	Х	Х
2050-2111	Service man- agement	x		x	х	
2345		X				Х
2600 -26991	Ixia Reserved	Х			X	X
2601		Х				X
2705	IxVPN	Х			X	Х
2782	CliX	Х		Х		X
2809 -2825	Aptixia CORBA	X		Х		Х

Port	Use	ТСР	UDP	Used on Chassis	Used on Port CPU	IxOS 5.30 and later
3222	File Cabinet port	Х		X	X	Х
3600-39991	Ixia Reserved	Х			X	X
3705	IxVPN	Х			X	X
4501-4502	Licence Man- agement	x				Х
4601		Х				Х
4555	IxTclServer	Х		Х		Х
4900	VNC	X		X		Х
5285	IxServer status connection to IxDodServer	x		X		X
5286	IxServer con- nection to IxAd- min	X		X		X
5326	IxServerConsole (IxServer RPF Interface)	X				X
5480	Ixia Reserved	X				Х
5488-5489	Ixia Reserved	X				Х
5555	IxVPN	Х			Х	Х
6001	Service manager	Х		X	X	Х
6002	Capture service	Х			Х	Х
6003	Capture service relay	x		X		Х
6004	Download on Demand broadcast data		X	X	X	x
6005	Download on Demand server	x		X		Х
6101	IxNetwork	Х		X	X	
6809-6825	Aptixia / CORBA	Х			X	Х
6665	InterfaceManager (IxAuthenticate &	X			X	X

Port	Use	ТСР	UDP	Used on Chassis	Used on Port CPU	IxOS 5.30 and later
	IxAccess)					
6967	Ixia Reserved	X				X
6978	Ixia Reserved	X				X
7768	RPF Impairment	Х		Х	X	X
8003	IxAuthenticate	X			X	Х
8008	IxNetwork	X			Х	Х
8881	CP/DP	X			X	Х
8890	Mono	X				Х
9101-9102	Statistics engine (Statengine)	x		X	x	x
9613-9676	Service man- agement	х		X	X	х
9888	OTN	X		Х		Х
10115	IxChariot	X		Х	х	Х
10116	Ixia Reserved	X	Х			Х
17662		X				Х
17668	IxServer	X		Х		Х
17669 (4505h)	IxServer	х		X		X
17670 (4506h)	Statistics watch	x		X		x
17671 (4507h)	Protocol watch	X		x		
17674 (450Ah)	Logcollector	X		x		х
17777 (4571h)	Port CPU serial console	X		x		х
21653	Statistics engine (DataSeqBroker)	x				х
23123	Statistics engine (CoordinatorNode)	x				х
26999	License Man-	Х		X		X

Port	Use	ТСР	UDP	Used on Chassis	Used on Port CPU	IxOS 5.30 and later
	agement pre- 2.40SP1					
27009	(if license server is running on chassis)					
27000	License Man- agement 2.40SP1 and later	X		X		X
27000	(if license server is running on chassis)	^		^		^
32769	mountd	Х		Х		Х
3280-32816	IxVPN CORBA	Х			X	Х
38001- 38096	IxSAN	x			x	x
54321	IxVPN	X		X		X

## **Legend for Chart**

- Blank = not supported or not applicable
- X = supported feature

#### **More Information**

For more information, contact Ixia Technical Support:

Phone	(877) 367 4942, ext. 1
Fax	(818) 444 3101
Email:	support@ixiacom.com



## **Appendix F: Laptop Controller**

The Laptop Controller supports the following Ixia applications:

- IxNetwork
- IxN2X
- IxLoad
- IxAutomate
- IxANVL
- IxOS

The Laptop Controller has a dual-use operation similar to the IxN2X Controller and the Ixia Application Server. So we do not require simultaneous operation for these two.

# **Specifications**

The following table lists the sspecifications of the Laptop Controller:

Laptop Controller Specifications

Specification	Details				
Supported Configurations	1 heavy user (complex and high scale configurations)				
Base Unit	Dell Latitude E6430n (225-3543)				
Processor	3rd gen Intel Core i5-3210M Processor (2.5GHz, 3M cache), Dell Latitude E6X30 (317-9440)				
RAM	8.0GB, DDR3-1600MHz SDRAM				
Hard Drive	750 GB, 7200 RPM				
Ports	2 LAN Ports (10/100/1000-Base-T)				
Keyboard	Internal English Keyboard				
Monitor	14.0" HD (1366x768) Anti-Glare LED-backlit				
Graphics	Intel HD Graphics 4000				
Performance	Multi-core / Hi-performance				
Life Cycle	Projected life-cycle of at least 2 years (2 years before EOL date by the manufacturer)				

Some of the other specifications of the Laptop Controller are as follows:

- Documentation (English/French)
- Tech Setup Guide, English
- No Dell ControlVault, No Fingerprint Reader, No Smartcard Reader and No Contactless Smartcard Reader
- Windows OS
- Ixia Label

- Dell Wireless 380 Bluetooth 4.0 LE Module
- No Modem
- No Modem for Latitude E-Family
- US 3 foot Flat Power Cord
- 90W 3-Pin, AC Adapter
- 8X DVD+/-RW
- 8X DVD+/-RW Bezel
- Noise Cancelling Digital Array Microphone
- Dell Wireless 1504 802.11g/n Single Band Wi-Fi Half Mini-card
- No Intel vPro Technology Advanced Management Features
- 6-Cell (60WH) Primary Lithium Ion Battery, (2.8Ah) ExpressCharge

# **Appendix G: Software Licenses**

IxOS contains certain third-party software that is delivered as part of the product. A list of such third party software that is licensed to Ixia, is identified as follows.

For details about the third-party software licenses, please see the <u>Ixia Reference Guide</u> <u>Third Party Software License Appendix</u>.

Third- party Soft- ware	Vend- or Nam- e	Soft- war- e Ver- sion	Lic- ens- e	License URL
xmlPar- ser1.2	Expla- in	1.2	Cus- tom	<pre>https://- source- forge.net/p/tclxml/svn/11/tree/trunk/LICENSE</pre>
	Stef- fen Trae- ger	1.2	BSD	https://spdx.org/licenses/BSD-4- Clause.html
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