DesignCon 2001

Delivering Solutions and Technology to the World's Design Engineering Community

January 29 – February 1, 2001
Exhibits: January 30–31, 2001
Santa Clara Convention Center
Santa Clara, California

Four Solutions-Oriented Conferences

- System-on-Chip Design Conference
- IP World Forum
- High-Performance System Design Conference
- Wireless and Optical Broadband Design Conference

Special Technology Focus Areas

- Internet and Information Appliance Design
- Embedded Design
- RF, Optical, and Analog Design

NEW!

- IEC Executive Forum

International Engineering Consortium
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Register by January 5 and save $100 – and be entered to win a Palm Pilot!

Practical Design Solutions


DesignCon provides attendees with design solutions from peers and professionals.

Practical design-engineering solutions presented by practicing engineers—The DesignCon reputation of excellence has been built largely by the practical nature of its sessions. Design engineers hand selected by our team of professionals provide you with the best electronic design and silicon-solutions information available in the industry.

DesignCon has an established reputation for the high quality of its papers and its expert-level speakers from Silicon Valley and around the world. Each year more than 100 industry pioneers bring to light the design-engineering solutions that are on the leading edge of technology. This elite group of design engineers presents unique case studies, technology innovations, practical techniques, design tips, and application overviews.

The most complete educational experience in the industry

The four conference options of DesignCon 2001 provide a complete educational experience, including the practical design solutions you need. DesignCon is the only meeting that brings leading designers together to discuss the current industry trends, learn the best design solutions, network with industry peers, and interact with the companies that provide the equipment that makes solutions possible. At DesignCon 2001, you will find the best educational value available in the industry.

Selected paper presentations at DesignCon are closely tied to technological exhibits. Attendees will see the technological future in action! Take part in the DesignCon difference today and become part of the most prestigious and most complete educational conference offered in design engineering.


Attendees find valuable networking opportunities throughout the conference.

Who Should Attend

Any professionals who need to stay on top of current information regarding design-engineering theories, techniques, and application strategies should attend this conference. DesignCon attracts engineers and allied professionals from all levels and disciplines. Professionals attending DesignCon work in ASIC design, communications, digital design, radio frequency (RF) and analog design, test and measurement, mixed signal, field programmable gate arrays (FPGAs), printed circuit boards (PCBs), programmable logic devices (PLDs), circuit-board design, integrated-circuit (IC) design, software optionality control and applications design, systems architecture, hardware/software integration, convergent technologies, packaging, testing, debugging, applications design, and more.

- Advisory Engineers
- Chief Scientists
- Circuit Designers
- CMOS Circuit Analysis and Development Engineers
- Presidents, Vice Presidents, and Chief Executive Officers
- Design Engineers and Principals
- Directors of Research and Development
- EDA Engineering Managers
- Editors and Executives of the Technical Media
- Embedded System Designers
- Engineering Fellows
- Engineering Managers
- Field Applications Engineers
- Hardware Engineers
- Hardware Verification Engineers
- Hardware/Software IC Design
- Internet and Information Appliance Designers
- Technical Staff
- Program Directors
- Project Engineers, Leaders, and Managers
- Research Engineers
- R&D Engineers
- Semiconductor Product Managers
- Senior Engineers
- Senior Members of Technical Staff
- Senior Productivity Engineers
- Signal Integrity Engineers
- Software Engineers
- System Architects
- System-Design Engineers and Managers
- Technical Vice Presidents
- Venture-Capital Analysts

Tuesday, January 30 • 12:00 pm – 1:00 pm

Tuesday Keynote Presentation

Walden Rhines, President and Chief Executive Officer, Mentor Graphics, is on the board of directors for the Electronic Design Automation Consortium (EDAC) and is a board member for the Oregon Independent College Foundation and for Lewis and Clark College. Prior to joining Mentor Graphics, Dr. Rhines was executive vice president in charge of Texas Instruments' Semiconductor Group. During his career at TI, Dr. Rhines was responsible for developing products such as TI's first speech synthesis devices (used in "Speak and Spell") and the TMS 320 family of digital signal processors.

Wednesday, January 31 • 12:00 pm – 1:00 pm

Wednesday Keynote Presentation

Charles Fox, President and Chief Executive Officer, Chameleon Systems, has 20 years of experience in microprocessor, FPGA and ASIC products in both marketing and general management. He was most recently vice president and general manager of the ASIC business unit at Xilinx. Previously he was vice president of worldwide marketing. Prior to Xilinx, Mr. Fox spent nine years in marketing management within Intel's microprocessor, peripheral, and ASIC groups.

Tuesday, January 30, 6:30 pm – 8:00 pm

Special Evening Reception and Speaker

Join us for a relaxing evening with **Robert A. Pease,** Staff Scientist-Circuit Design, National Semiconductor. A well-recognized speaker, Mr. Pease will enlighten attendees with trends in circuit design and the Semiconductor Industry, and entertain everyone with his humor, wit and insight into industry snafus, and successes! Mr. Pease obtained his BSEE from Massachusetts Institute of Technology and is a noted columnist with Electronic Design Magazine.

Contents

Wednesday, January 31 • 11:00 am – 12:00 pm

Plenary Panel

Design Engineering and the World Wide Web: Where They Meet to Create Ultimate Value

Chip and system design engineers are being offered new Web-based options for access to EDA tools, component data, and computer services. It is uncertain whether such services will only represent a niche for tool use and component access or whether engineers will receive great value and develop a high dependence on the web for electronic design. Expert users on this panel discuss the value that they are experiencing, or would expect to receive, from web-based services. Suppliers of web-based services discuss the benefits that they see the web bringing to the design community and how the services can best be deployed.

CHAIRPERSON

Jack Shandle, Chief Editor, eChips, has worked for daily newspapers and electronics OEM trade magazines, freelanced for national publications, and authored a novel. He has also worked for four national and statewide political campaigns as an advance man and media coordinator. In 1986, he joined *Electronics* magazine. From *Electronics,* Mr. Shandle moved to *Electronic Design* magazine where he became chief editor in 1994.

PANELISTS

David Burow, Senior Vice President, Internet Design and Services Group, Synopsys, joined Synopsys in connection with the company's merger with Viewlogic in December 1997. He was with Viewlogic from August of 1995 as vice president of the high-level design group after serving in a number of key management positions at Silicon Architects, which was acquired by Synopsys in May 1995.

Judy M. Owen, Founder, President, and Chief Executive Officer, SiliconX, started her career at Intel, developing memory chips and then microprocessor chips. In 1981 she was appointed to manage a select group within Intel to develop proprietary CAD software tools to protect Intel's intellectual property and shorten the chip design cycle. Prior to starting SiliconX, Ms. Owen founded Wireless Access in 1991, serving as its president and chief executive officer.

Mark Ross, Director, Engineering, Cisco Systems, began his career developing full custom CMOS chips at Weitek, where he was an early customer of what eventually became Cadence. In 1989, Mr. Ross joined NeXT and led the development of a RISC workstation. At NeXT he was an early customer of Synopsys and specified numerous internal development tools. His next job was at Sun, where he led the development of the Ultrasparc workstations.

Harry Baeverstad, Manager, Research and Development, Hewlett-Packard, is currently leading a new initiative at Hewlett-Packard to deliver "always-on" Internet-based technical computing solutions for engineers and scientists. The first product produced from this initiative is "e-utilica," a scalable, secure, Internet-enabled computer farm providing computer capacity-on-demand solutions for service providers.

Tuesday, January 30 • 4:00 pm – 5:15 pm

System-on-Chip Conference Panel

The ASIC/FPGA Battle: Will a Hybrid Solution Win?

FPGA technology has come a long way over the past three years and is now encroaching on traditional ASIC turf. As the battleground continues to be contested, system designers are asking for a hybrid product that can give them the best of both worlds. Many companies are starting to introduce hybrid products targeting selected applications. How large will the market be for such products? What will be the applications that will drive the market? Who will be the winners? Come hear the market leaders share their views.

CHAIRPERSON

Bryan Lewis, Principal Analyst, Dataquest, joined Dataquest in 1985 and founded Dataquest's ASIC/SLI service. He has responsibility for tracking and evaluating market movements, forecasting markets, and tracking technology trends.

PANELISTS

Ronnie Vasishta, Senior Director, Technology Product Marketing, LSI Logic, is responsible for overseeing the definition and development of the company's ASIC products including silicon technologies, advanced packaging, mixed signal, embedded memory I/Os, CAD tools, and methodologies. Before joining LSI Logic, Mr. Vasishta worked in process engineering for Motorola and in test and process engineering for STC Semiconductors in the UK.

Peter Feist, Vice President, Marketing, QuickLogic, has over 20 years of experience in the semiconductor industry in marketing, sales, and engineering. Before joining QuickLogic, Mr. Feist spent ten years at LSI Logic Corporation in management and marketing posts including general manager for Central Europe, director of marketing for Europe, and director of strategic marketing at corporate headquarters in the United States.

Chris Balough, Senior Director, Strategic Planning, Triscend, is responsible for defining and developing Triscend's product roadmap. Mr. Balough has more than 10 years of experience in semiconductor product marketing and sales. Prior to founding Triscend, Mr. Balough served in product marketing at Xilinx. Before Xilinx, he worked in technical sales for Texas Instruments.

J. Marc Edwards, Hardware Engineer, Cisco Systems, spent 11 years working with IBM in the field of computer communications, networking, and RISC I/O architecture, concentrating on ASIC and FPGA design implementations. For the last 5 years, he has held a similar role with Cisco Systems, concentrating also on object-oriented system modeling, architecture, and verification. Mr. Edwards' present interests lie in the area of re-configurable logic architectures for network processing applications and next-generation system descriptions.

Bruce Weyer, Senior Director, Marketing, Xilinx is responsible for product marketing and applications efforts for the Xilinx advanced product division. Before joining Xilinx in 1998, Mr. Weyer served as director of marketing at Actel Corporation and held marketing and engineering positions at Advanced Micro Devices and Lockheed Missiles and Space Company.

Tuesday, January 30 • 4:00 pm – 5:15 pm

Optical Broadband Design Conference Panel

The Future of Optical Broadband Networking

Optical technology may soon dominate the network and communications markets at all levels: backbone, wide-area network, last mile, and local area network. This panel projects how optical technology will impact networks and communications. Panelists represent all layers in the communications hierarchy: optical backbone fiber, integrated circuit drivers and interfaces, optical wave casting for the last mile to the office or home, and the optical networking infrastructure. Optical techniques are also leading to 3D multiplexing designs and special network architectures to match optical capacities. Each panelist will briefly address technology projections and the impact of these projections on networking and the communications marketplace.

CHAIRPERSON

Debra Vogler, Editor, Link2Semiconductor, has 20 years of industry experience as a reliability engineer. She has held various positions at Watkins-Johnson Semiconductor Equipment Group and Varian Thin Film Systems. Before joining Link2Semiconductor (a division of AvantCom Network), Ms. Vogler was senior account manager and editor at Mathews & Clark Communications where she defined PR strategy and tactics for key clients in the semiconductor industry.

PANELISTS

Scott Bloom, Vice President, Engineering, Advanced Development, AirFiber, co-founded AirFiber in May 1998. Prior to his current position, Dr. Bloom was vice president, business development, at AstroTerra. Throughout his tenure as senior vice president, applied physics group manager, and senior scientist, Dr. Bloom researched, designed, and built many free-space optical communications systems for spacecraft, aircraft, and terrestrial applications.

Philip Anthony, Vice President, Engineering, E-Tek Dynamics, joined E-TEK from Lucent Technologies, where he spent ten years in various senior positions that spanned research and development, product management, and manufacturing. He was most recently director of passive devices and integrated optical modules in Lucent's microelectronics group, where he drove operation of the optoelectronics business unit that produced advanced photonic products for a worldwide market.

Tom Palkert, Senior Systems Architect, AMCC, is currently involved in the system applications of high-performance serializer/deserializer chip sets and physical media dependent integrated circuits. The applications for these high performance chipsets include SONET OC3, OC12, OC48, OC192, OC768, DWDM systems, Gigabit Ethernet, 10 Gigabit Ethernet, fiber channel, HDTV, and proprietary serial backplane interfaces.

Philip Ong, Manager, Optical Networking Group, Lucent Technologies, is responsible for assisting the ONG product line teams in optical data feature planning, strategy setting, and system architecture designs. He is also responsible for providing assistance to Lucent's ONG chief strategy officer in defining overall strategic direction and advanced technology evaluation for the ONG product business units.

Wednesday, January 31 • 4:00 pm – 5:15 pm

High-Performance Conference Panel

Design for Extreme Data Rate Performance: Reaching toward Theoretical Limits

Signal integrity has always been a key element of high-bandwidth system design. Design rules were adequate to provide the required performance. However, demand for 10 Gbps rates has made SI a highly visible part of the process. Designers must include all parts of a high-performance product: intra-chip pathways, chips, package, mounting, bus signaling, board, peripheral buses, and external connectors. The backplane may drive the system to success or doom it to failure. To respond to this complexity, the engineering process now requires simulation, measurement, modeling, and test verification of a design prior to shipment. Also, engineers must consider interfaces with optical methods and communication protocol architectures. The panel will address the impact of design at extreme data rates on the engineering process, on high bandwidth product performance, and on the capacity delivered for leading technology systems.

Chairperson

David Taylor, Strategic Solutions Manager, Electronic Products and Solutions Group, Agilent Technologies, has influence over all of Agilent's bench-top instruments; his current focus is InfiniBand program management. Mr. Taylor's 11-year career with HP/Agilent has been primarily focused on developing logic analyzer solutions for the computer industry. As a research and development engineer he developed solutions for Intel's i860XP and Pentium® Processor, and, as a project manager, Mr. Taylor managed the development of high-performance oscilloscopes and scope-probing solutions.

Panelists

Michael Mott, Associate Technical Fellow, Boeing Company, provides architectural concepts and designs for high-bandwidth networking and high-performance computing (HPC) systems to programs throughout the integrated defense systems division at Boeing's Seal Beach facility. Mr. Mott has worked in the field of high-performance computing since the late 1970s when he began his career with McDonnell Douglas as a systems programmer for Control Data Corporation (CDC) mainframes. During the first half of the 1990s, Mr. Mott worked on the International Space Station.

Edward Sayre, President and Chief Executive Officer, North East Systems Associates, founded NESA in 1973. Dr. Sayre is also the founder and chairperson of the IBIS users group, which focuses on usability issues of the behavioral simulator. Prior to forming NESA, Dr. Sayre designed microwave antennas and electromagnetic systems for AVCO Systems Division. During his time at AVCO, Dr. Sayre was an inventor of the space shuttle microwave landing antennas, as well as numerous conformal microwave stripline antenna structures.

Juergen Flamm, Manager, Electronic Engineering, Litton Systems, is responsible for the design of high-performance power supplies; analog, digital, RF, and mixed-mode circuits for the entire military and commercial product lines of inertial systems, LCD display systems, IFF systems; and mission computer systems produced and sold by Litton Systems. Prior to his current role at Litton, Mr. Flamm was responsible for the next-generation high-accuracy FOG inertial navigation system electronics design.

Steve Kaufer, Director, Technology, Innoveda, has 15 years of multi-faceted design expertise spanning both hardware and software development. He was a system and ASIC engineer at Data I/O and worked as an engineering manager at Synario Design Automation. In 1989, he co-founded HyperLynx, a company focused on signal-integrity and EMC tools for the desktop. Currently, he manages a portion of Innoveda's high-speed-design tools group.

Wednesday, January 31 • 4:00 pm – 5:15 pm

IP World Forum Conference Panel

Engineering Management Business Considerations in the use of Semiconductor Intellectual Property

The use of semiconductor intellectual property (SIP) in SoC designs today requires an equal amount of business savvy and technical expertise. By understanding the motivations of the SIP provider, one can make better-informed decisions and leverage the advantages rather than wander into the pitfalls that emerge when using cutting-edge SIP. This panel represents both experienced users and suppliers of SIP and will focus on the business issues important to making the attendee a better-informed and more effective manager. Each member will present a short overview of important points for consideration to be followed by an open and interactive discussion with the audience.

Chairperson

Daniel Caldwell, Intellectual Property Licensing Consultant, has been in design, EDA, and IP licensing for 20 years at companies such as Intel, AT&T Bell Labs, Phoenix Technologies/InSilicon, Mentor's Inventra division, and the Virtual Component Exchange. He has published papers on SIP licensing and has personally negotiated over one hundred IP licenses.

Panelists

Timothy O'Donnell, President, ARM, established the U.S.-based operation of ARM in 1991. He was instrumental in establishing ARM's U.S. presence as a semiconductor IP provider and has been a leading advocate of the advantages of IP as a system-on-chip design methodology. Mr. O'Donnell has more than 25 years experience in international management and technical positions within the semiconductor industry, most notably with National Semiconductor and Cadence Design Systems.

Shannon Johnston, Senior Manager, Nortel Microelectronics, Nortel Networks, has worked in various aspects of the electronic product development business for the past 15 years. In that time, he has designed digital ASICs, developed EDA tools, worked in the manufacturing environment developing system tests, and managed a variety of functions including the provisioning of ASIC and PLD design services, technologies, and tools on behalf of Nortel Networks.

Gabriele Saucier, Ph.D., Chairman of the Board, Design and Reuse, recently retired from the INPG (Institut National Polytechnique de Grenoble) to concentrate her attention on start ups. She taught at the university for 30 years and served as the director of a research laboratory on integrated system design. Ms. Saucier has been involved in research in a broad spectrum of VLSI CAD areas, namely test, floorplan/partitioning, and synthesis.

Andrew Travers, Chief Executive Officer, Virtual Component Exchange, has been the driving force behind the formation and evolution of the VCX, and he is involved in every aspect of the ongoing development of VCX operations and management. His primary focus within VCX is to develop the company's business plan and strategic relationships as well as to promote VCX to the industry at large.

Mark Bowles, President and Chief Operating Officer, BOPS, has 13 years experience in the semiconductor industry, including 6 years at Motorola Semiconductor where he held various sales and market development positions. He left Motorola in 1996 as vice president, MSPI, and PowerPC market development manager to found BOPS.

System-on-Chip Design Conference

The System-on-Chip Design Conference opens on Monday of DesignCon week with an exciting TecForum on Internet appliances and the application of National Semiconductor's Geode processor. TecForum sessions continue with Xilinx's latest advancements in the design of FPGAs, the latest design closure methodology by Monterey Design Systems, and design platforms by Cadence Design Systems and Philips Semiconductors.

The technical sessions on Tuesday continue with papers presented by experts on chip-design cases covering voice over IP by Tality, and design verification and testing by BrightLink Networks and AT&T Labs. Platform-based developments move to configurable architecture in a paper by Palmchip. Hybrid design technology has arrived. As an attendee you will hear from LSI Logic, Atmel and ChipExpress how to integrate programmable logic with ASIC logic and how AMI has successfully converted many FPGA designs to ASIC technology. Tuesday technical sessions conclude with a panel on the ASIC/FPGA battle.

We begin Wednesday of DesignCon week with a paper on the design of a Bluetooth radio-on-a-chip by Alcatel Microelectronics. Expert speakers present new techniques on prototyping SoCs when using the AMBA bus with LSI Logic's SoC solutions and a flexible hardware emulation solution used at Hewlett-Packard. Modular platform design for concurrent hardware/software development is presented by Cadence Design Systems. If you have yearned for a unified ASIC and FPGA flow for timing convergence, Actel would like to show you their solution. A PCI based system described by Wayne Scott Associates and SynaptiCAD illustrates automated bus functional model test bench generation. Expert speakers from AMI describe embedded power management in mixed signal ASICs and from Texas Instruments a design case describing a winning solution for designing and testing mixed signal SoCs. Avant! gives an 'A' to 'Z' tutorial on design closure with hierarchical design methods. Gray Research describes the code for implementing a RISC processor in FPGA technology.

The conference concludes on Thursday with a full TecForum on ASIC verification and functional verification of hardware and software by Mentor Graphics and Verisity Design and a TecForum on practical design solutions on Internet-aware embedded systems by speakers from Verplex Systems, UFMG, and Advanced RISC Machines.

IP World Forum

Monday TecForums begin with presentations on the design and verification of a USB 2.0 controller by Mentor Graphics, a comprehensive analysis of what is different for Star IP compared to commodity IP by MoSys and MIPS speakers. Other sessions include topics on high-level design such as IP Modeling by Co-Ware, a methodology for creating an application specific virtual prototype in C by Synergy Systems Design, and a design flow being used by Infineon Technologies for consistency from algorithm to implementation level.

The Tuesday IP World sessions start with Lexra's experience as an IP core supplier with Soft CPU core layout integration for a VoIP ASSP, expert speakers on memory architecture from Infinite Technology, solving memory soft errors from MoSys, and the integration of a DDR controller from IBM Microelectronics. Star IP design and deployment advice continues on Tuesday led by a speaker from Synopsys. A speaker from Mentor Graphics Inventra shares advice on IP implementation in FPGAs. Infineon Technologies presents a novel solution for DSP extensions when performance is the issue. Tuesday is also circuit design and analog/mixed signal day! Useful design tips that you can immediately apply are shared by speakers from Oren Semiconductor, WIPRO Technologies, and Mentor Graphics and originate from a research project on optimum comparators and Sigma-Delta modulators. A speaker from National Semiconductor provides application advice on the application of an 8-bit highly integrated microcontroller, available for immediate use. Avnet Design Services describes a practical design case with Internet appliance application that uses a Xilinx PCI core and Intel StrongArm processor. Genesys Testware gives a tutorial on automating IP Core integration. Solutions for managing your design data are addressed by Beach Solutions.

By Wednesday the IP World program moves to rapid IP prototyping and static functional verification. These topics with practical application are discussed in sessions led by Aptix and by 0-In Design Automation. If you are involved with IP deployment, a new topic at DesignCon, four sessions and a panel may be of interest to you. Tool support is discussed by Synchronicity. Systems for access to IP are presented by the Virtual Component Exchange and by HelloBrain.com. Speakers from Hewlett-Packard describe the capabilities of an internal company IP repository. The panel late Wednesday afternoon is a discussion of how to streamline IP acquisition. The DesignCon Plenary panel, also on Wednesday, should be an exciting discussion on where the Web and design engineering meet to create value. Finally, the IP World TecForum on Thursday by Simutech focuses on IP evaluation and SoC verification.

DesignCon is a very comprehensive conference and exhibition. It's a place for engineers to share experiences and catch up on new design techniques, and see new solutions and technology first-hand. Register for sessions and you'll gain firsthand knowledge from leaders in design engineering.

High-Performance System Design Conference

On Monday, January 29, the High-Performance System Design Conference begins strongly with TecForums on high performance buses (PCI-X and InfiniBand) and signal integrity methods applied to connectors and surface mount. The PCI-X Workgroup presents a TecForum on working with the PCI-X standard. PCI-X is needed to meet the demands of faster peripheral applications such as gigabit ethernet, ultra160 SCSI and fibre channel. In the same morning, MacroExpressions presents a focused TecForum on embedded code reusability. That afternoon the Harting TecForum uses two signal integrity investigations of high pin-count connectors to guide the design of 10Gbps per pin-pair high speed/high density SMT and compact PCI 2mm hard-metric connectors. The TecForum shows how to combine 3D FEM-simulations, SPICE simulations and measurement data to show pin-in-hole effect, crosstalk, and skew influences. Also in the afternoon Agilent Technologies presents a TecForum on InfiniBand. These InfiniBand designs are used for ultra-high speed interconnect of server class computer clusters and their I/O subsystems. Techniques for functional validation and debug of InfiniBand-based systems using protocol aware real time bus analyzers are presented for design and verification of InfiniBand-based systems.

Signal integrity is becoming the key word in design as performance pushes past old physical limits. In the High-Performance System Design Conference all aspects of the intersection of high speed, reliable data movement and physical and electrical infrastructure are considered. The authors give design cases showing signal integrity techniques for multilevel signaling, source-synchronous signaling, high-performance memory bus, and 10 Gbps transmission. Design approaches include data pathway standards, such as InfiniBand, RAMBUS, PCI-X, compact PCI, and 3G data networks. Signal driver technologies, design issues and test measurement are stressed for interconnect technologies. The papers consider cases where multiple methods are coupled: design, modeling, and measurement using the latest instruments. Several papers consider the component model integration approach where component models derived from small-scale simulation and measurement are integrated into full system level results and verified on a prototype. Engineers will also suggest techniques for design solutions at physical limits. These techniques enable engineers to consider the effects and tradeoffs of dispersive, lossy media. Other papers will reveal advances in differential mode measurements and related design.

On Thursday the High-Performance System Design Conference wraps up with a key topic that will summarize many of the principles given in the prior three days: a TecForum by Texas Instruments, providing a general overview of single-ended and differential bus solutions and an in-depth analysis of backplane line theory and design techniques. The TecForum provides a guide to optimal technology selection, signal integrity, and performance.

Wireless and Optical Broadband Design Conference

On Monday, January 29, the Wireless and Optical Broadband Design Conference begins with two TecForums that promise to change how telecommunication, networking, and base station infrastructure platform designs are accomplished. The Philips Semiconductor TecForum is on a new generation of general purpose ICs that offer repeatable, dependable logic translation and clock distribution. These include translation between LVDS–PECL at 800 Mbps, universal logic translation and multiplexing. Then Celoxica provides a look at their revolutionary system-level design environment that is capable of transferring concepts into silicon. Their environment creates a flexible hardware system that can change each millisecond into another form. These FPGA designs are transformed from code representing processor cores, MP3 and VoIP.

On Tuesday the sessions begin with a vertical slice of advanced broadband design cases. Global broadband communication systems require multiple layers of hardware and embedded software. These papers give the engineer a top-to-bottom view of all design aspects, levels and scale. Papers cover the gamut of optical fiber interconnect and switching designs, optical-copper interface and switches, backplane, board, mounting and chip pathways, adaptive hardware methods, studies of software radios and 3G receivers, Bluetooth personal size networks and service discovery, and network protocol architectures to deliver broadband communications. Design cases include optical fiber, high bandwidth infrastructure, network architecture, optical-copper interfaces, high performance switching, pathway infrastructure (backplanes, connectors, and chips), smart-flexible computing, switching-routing devices, wireless environment, mobile broadband data networks, handheld devices, short range networks and personal communication device coordination. Tracks are network and communication infrastructure pathways, Bluetooth/3G/handheld application design, advanced embedded communication techniques, flexible/intelligent network design, and fiber optical performance optimization.

On Thursday morning, key TecForums for the wireless and optical broadband engineer are presented. The StarCore TecForum describes how next generation communications challenges can be met through the StarCore SC100 DSP architecture. The TecForum covers application development and key DSP concepts for high performance. The second TecForum describes the design effort necessary for incorporating wireless local area networks into a standard communication infrastructure shows how wireless technology is put into action. This tutorial provides the design engineer with a target environment in which his work must be delivered.

To Register
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Executive Forum Workshops @ DesignCon 2001

New to DesignCon this year are the Executive Forum Workshops, two unique educational events designed specifically for industry leaders. DesignCon 2001 offers both a morning and an afternoon Executive Forum that will highlight current hot topics in the world of design engineering. The Executive Forum Workshops @ DesignCon 2001 give executives the opportunity to meet, network, and trade knowledge and expertise in an interactive educational atmosphere.

In what direction is the design-engineering industry headed? What challenges will the 21st century bring? Panelists at the Executive Forum Workshops will share their insights, perspectives, predictions, and visions in individual presentations and panel discussions. Attendees will take from these Forums the tools and guidance they need to forge ahead in the exciting world of design engineering.

Tuesday, January 30 • 10:00 am – 12:00 pm

The Internet Appliance Market: Business Factors and Technologies That Will Make It Soar

This workshop includes three executive presentations and an interactive panel discussion. Topics addressed include the market and technology factors needed to energize the Internet appliance industry and the technologies needed to make Internet appliances ubiquitous.

CHAIRPERSON

Gabe Moretti, Technical Editor, Cahners, writes about ASICs and the EDA industry and keeps an active role in EDA standard-making efforts from his home base in Colorado. From 1968 to 1982, Mr. Moretti developed CAE software for TRW Systems, Compucorp, Intel, and Philips/Signetics. Over the next 18 years, he worked for EDA companies, from small start-ups, to his own CAE service company, finishing with Intergraph/VeriBest for the last seven years.

SPEAKERS

Jerry Tu, Director, Communication Technology, Handspring, oversees the company's production of wireless communication products for handheld computing. Prior to his role at Handspring, Mr. Tu served as director of DSP and system engineering for interWAVE Communications International, where he worked on radio and network signaling products for GSM equipment manufacturers. He has had more than 18 years of industry experience in companies such as Applied Signal Technology, ViTel Communications, and Hughes Aircraft Company.

Jim Tully, Chief Analyst, European Enabling Technologies Group, Dataquest, specializes in design-centric semiconductor research and leads Dataquest's activities in intellectual property. He also consults widely in topics such as strategy development, company assessments, and technology analysis. Before joining Dataquest, he worked with the EDA company Racal Redac, initially as a system architect and engineering manager.

Larry Mittag, Vice President and Chief Technologist, Stellcom, has more than twenty years experience with embedded systems design and development. He is one of the leading experts in the field of embedded systems, embedded Internet and wireless computing, and is a regular class instructor for the embedded systems conferences and a longstanding member of their advisory committee. Mr. Mittag serves as a contributing editor for Embedded Systems Programming and writes a monthly column for Communications Systems Design.

Tuesday, January 30 • 2:30 pm – 4:00 pm

How to Achieve Success with Global Research and Development

What factors will play a role in guaranteeing the success of research and development as we enter the 21st century? A panel of industry leaders will answer this question while providing senior-level executives with advice on the global organizational development of systems, chips and software. Time will be reserved for a dynamic, interactive discussion with the workshop audience, as speakers and attendees address exciting and innovative developments in the research and development field.

SPEAKERS

Chau Pham, Vice President and Director, Core Engineering, Motorola Computer Group, is responsible for the development of the complete product lines for MCG, from ASIC chipsets to boards and platforms including VME, CompactPCI, PrPMC, and various embedded motherboard form factors. Mr. Pham joined Motorola in 1984 as a board and ASIC designer for the VME single board computers. Prior to joining MCG, Mr. Pham spent four years as a logic design engineer at Space Data (Orbital Science) where he was involved in numerous NASA projects.

Gerald Buurma, Senior Vice President, Research and Development, Cadence Design Systems, has 29 years of industry experience, equally split between integrated circuit design at major semiconductor companies, such as National Semiconductor and Toshiba America, and EDA companies, such as Cadence. Mr. Buurma has worked on manufacturing sign off, which includes OPC and PSM, and has extensive experience with place and route, floorplanning and physical design.

Robert Yung, Chief Technology Officer, Communication Products Group, Intel, is leading the organization that shapes the future of products and services for emerging e-businesses and converged communication by driving long-term technology directions and successful implementation and integration of core technologies via research and development. Prior to his current role at Intel, Mr. Yung was a director at the Intel Architecture Group and Intel's Chief Technology Officer for China.

IEC University Program

Through the University Program, sponsoring organizations provide grants for full-time faculty members and their students to attend IEC Forums. The generous contributions of the following sponsoring organizations make this valuable program possible. For more information about the program, please call +1-312-559-4613 or send an e-mail to *universityprogram@iec.org.*

This past year, the University Program has provided more than 400 grants to professors to attend the educational opportunities offered at IEC Forums. Because of their participation in IEC Forums, professors created or updated 600 university courses; more than 10,000 students were impacted by these new and upgraded courses, and more than 12,000 students benefited from improvements made in university laboratories. Since its inception in 1984, the University Program has enhanced the education of more than 500,000 students worldwide.

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École Nationale Supérieure des Télécommunications de Bretagne
École Nationale Supérieure des Télécommunications de Paris
École Supérieure d'Électricité
University of Edinburgh
University of Florida
Georgia Institute of Technology
University of Glasgow
Howard University
Illinois Institute of Technology
University of Illinois at Chicago
University of Illinois at Urbana/Champaign
Imperial College of Science, Technology and Medicine
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Instituto Tecnológico y de Estudios Superiores de Monterrey
Iowa State University
KAIST
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Marquette University
University of Maryland at College Park
Massachusetts Institute of Technology
University of Massachusetts
McGill University
Michigan State University
The University of Michigan
The University of Mississippi
University of Minnesota
University of Missouri-Columbia
University of Missouri-Rolla
Technische Universität München
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North Carolina State University at Raleigh
Northwestern University
University of Notre Dame
The Ohio State University
Oklahoma State University
The University of Oklahoma
Oregon State University
Université d'Ottawa
The Pennsylvania State University
University of Pennsylvania
University of Pittsburgh
Polytechnic University
Purdue University
The Queen's University of Belfast
Rensselaer Polytechnic Institute
University of Southampton
University of Southern California
Stanford University
Syracuse University
University of Tennessee, Knoxville
Texas A&M University
The University of Texas at Austin
University of Toronto
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New Advancements in Technology

Solutions for the Silicon Valley – and the World

DesignCon 2001 exhibits are the best place in Silicon Valley to find the solutions, technologies, and services you need to perform your job. Each year, the attendance of DesignCon takes on a broader scope, covering more and more of the issues important to industry professionals like you. This past year, DesignCon attracted 4,400 design-engineering professionals, 72% of which were from California, 19% from other U.S. states, and 9% from international locations – can you afford not to be there? In addition to the sessions, attendees will view more than 130 technological exhibits from the leading vendors in EDA, silicon, and IP. Attendees will find important new product releases from some of the best companies in Silicon Valley and around the world and then have the opportunity to discuss their functionality right on the exhibit floor.

Exhibits and demonstrations include leading design-engineering companies from Silicon Valley and around the world.

Exhibitors at DesignCon 2001* are all leaders in electronic design, semiconductors, IP, and system OEM. Attendees are sure to find value in visiting the exhibits, researching new technologies, and getting a firsthand look at new solutions, equipment, and services available to them for solving their challenging design problems.

Exhibitor	Booth
3DSP	825
Abelconn	649
Advanced Resources	738
Agilent Technologies	205, 305 Demo Pavilion
Alcatel – IP Group	711
ALDEC	106
Amherst Systems Associates	110
Anadigm	847
Applied Simulation Technology	832
Aptix Corporation	325
ARC Cores Ltd.	621
Artisan Components	715
ASIC Alliance	910
ASSET Intertech	909
Atmel Corporation	724
ATMOS	818
Avant! Corporation	521
Averant	836
Axis Systems	627
Barcelona Design	923
BOPS	809
C Level Design	301
Cadabra	920
Cadence Design Systems	503
Cahners Electronics Group	427
CAST	703
Chip Express	321
Co-Design Automation	940
CynApps	516
Denali Software	102
Design & Reuse	700
EDAconnect.com	925
EDAToolsCafe	937
EEMBC	TBD
ERNI Components	747
Faraday Technology	804
Flextronics Semiconductor	718
Fujitsu Takamisawa America	732
Genesys Testware	808
Get2Chip.com	417
Global Unichip	707
Harting Incorporated	639
Hewlett-Packard	114
Hybricon	938
IBIS	TBD
Improv Systems	919
InTime Software	844
INICORE	701
InnoLogic Systems	946
Innoveda (Viewlogic, Summit Design, and PADS)	515
inSilicon Corporation	805
Intellitech	118
Interconnect Systems Inc.	830
International Engineering Consortium	TBD
InterNiche Technologies	820
Intrinsix	931
Kluwer Academic Publishers	633
LEDA Systems	838
Legend Design Technology	743
LSI Logic	819
Mentor Graphics	403
MET Laboratories	200
MIPS Technologies	721
Monterey Design Systems	739
MoSys	712
National Semiconductor	512
North East Systems Associates	937
NOVAS Software	221
NurLogic Design	821
OEA International	629
Optimal Corporation	941
Packard-Hughes Interconnect	733
Palmchip	607
Philips Semiconductors	615
picoTurbo, Inc.	801
Prolific	704
QuickLogic	405
Rambus	123
Sagantec	611
Sequence Design	101
Sican Microelectronics	708
Sigrity	845
Silicon Perspective	840
Simplex Solutions	409
Simpod	735
Simutech	609
Siqual	736
SmartSand	730
Sonics, Inc.	837
SynaptiCAD	841
Synopsys	111
Synplicity	402
SynTest Technologies	621
TDA Systems	740
TechOnLine	727
Tensilica	813
Teradyne	509
Texas Instruments	227
Tharas Systems	741
TransEDA	122
Translogic USA	202
Transtector Systems	643
TSMC	932
Tyco Electronics	419
UMC (USA)	520
VaST Systems Technology	914
Verisity Design	942
Verplex Systems	647
Virtio	812
Virtual Component Exchange (VCX)	919
Virtual Silicon Technology	603
Wavecrest	831
Western Design Center	902

* List current as of 11/00

Hot Technologies at DesignCon 2001

Attendees will have a firsthand look at these new products at DesignCon 2001!

Company	Product
Advanced Resources	Exclusive Engineer Staffing
ASIC Alliance Corporation	SYSTEMware
ATMOS	Custom Memory SIP
BOPS, Inc.	DSP Architecture
C Level Design, Inc.	System Compiler™
Flextronics Semiconductors	Encore!Plus
Global UniChip	Sub-Micron SOC Design Solutions
Improv Systems, Inc.	Jazz PSA Platform
Inicore, Inc.	FPGA and AISC Solutions
Innoveda (Viewlogic, Summit Design, and PADS)	XTK˚, HyperLynx˚
Legend Design Technology, Inc.	MemChar and SpiceCut Memory
National Semiconductor	LVDS Technology
Optimal Corporation	PakSi-TM, PakSi-E
Prolific, Inc.	ProGenesis EDA Software
Simplex Solutions	VoltageStorm™ SoC
Simpod Inc.	DeskPOD™
SmartSand Incorporated	SmartMerlins
SynaptiCAD Inc.	TestBencher Pro v7.0
Synplicity, Inc.	Synplify Pro™ Tool
Teradyne Connection Systems	HSD6 Row Connector
Translogic	EASE 5.0
Verplex Systems, Inc.	BlackTie™ Functional Checker

...and many more!

To Register
Turn to Page 43

Exhibit Hours

Tuesday, January 30	12:30 pm – 6:30 pm
Wednesday January 31	12:30 pm – 6:00pm

Reception Hours:

Tuesday, January 30	4:45 pm – 6:30 pm
Wednesday January 31	4:45 pm – 6:00 pm

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DesignCon Exhibits and Sponsorships are Limited

Industry leaders take part in DesignCon demonstrating their presence in design engineering and commitment to Silicon Valley. Maximize your company's presence at DesignCon 2001 by reserving an exhibit or sponsorship today. Contact Kevin Fields via e-mail at kfields@iec.org.

DesignCon 2001

January 29 – February 1, 2001 • Exhibits: January 30–31, 2001
Santa Clara Convention Center • Santa Clara, California

For Exhibits and Sponsorship details, please contact:

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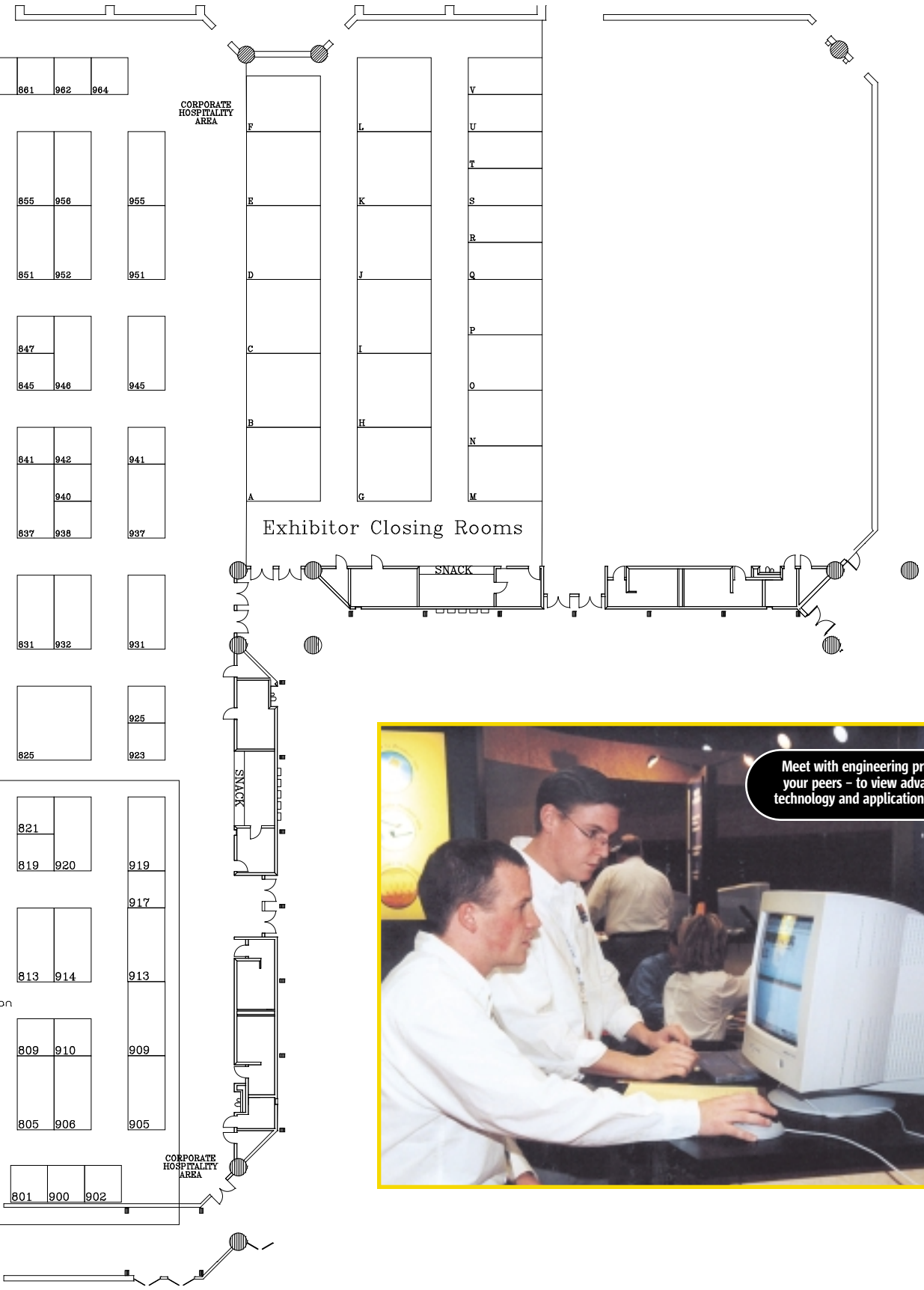
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Meet with engineering professionals – your peers – to view advancements in technology and applications engineering.

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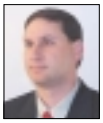

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DesignCon Sessions

Practical Design Solutions to fit your changing needs

The diverse session selections of DesignCon 2001 allow you to find the topic most vital to your operation, design challenge, and everyday concerns. With sessions in System-on-Chip, Intellectual Property, High-Performance Systems, and Wireless and Optical Broadband Design, DesignCon offers you the flexibility to plan your schedule around the hottest topics and specific solutions for your organization. Session details can be found on pages 26–41 of this catalog.

DesignCon TecForums

In-Depth 1/2 day presentations

With 19 TecForums at DesignCon, you're sure to find the topics and presentations that provide an in-depth learning experience from leaders in the field. TecForum topics include advanced design issues and methodologies from each of the four conferences, all presented by leading engineers and professionals from the top companies. See details for these TecForums on pages 21–25 of this catalog.

Monday, January 29

8:30 am – 5:00 pm
IBIS Open Forum Meeting

9:00 am – 12:00 pm
TecForums

12:00 pm – 1:00 pm
Luncheon

1:00 pm – 4:00 pm
TecForums

4:15 pm – 6:00 pm
VSIA Forum on VSIA Compliance and Reception

Tuesday, January 30

9:00 am – 11:50 am
Conference Sessions*

10:00 am – 12:00 pm
Morning Executive Forum Workshop
How to Achieve Success with Global Research & Development

12:00 pm – 1:00 pm
Luncheon with Keynote Presentation
Walden Rhines, President and Chief Executive Officer, Mentor Graphics

12:30 pm – 6:30 pm
Exhibits Open

12:30 pm – 1:30 pm
Exhibit Reception

2:00 pm – 4:50 pm
Conference Sessions*

2:30 pm – 4:00 pm
Afternoon Executive Forum Workshop
The Internet Appliance Market: Business Factors and Technologies That Will Make It Soar

4:00 pm – 5:15 pm
Wireless and Optical Broadband Design Conference Panel
The Future of Optical Networking

4:00 pm – 5:15 pm
System-on-Chip Design Conference Panel
The ASIC/FPGA Battle: Will a Hybrid Solution Win?

4:45 pm - 6:30 pm
Evening Reception on Exhibit Floor

6:30 pm – 8:00 pm
Special Evening Speaker
Robert A. Pease, Staff Scientist-Circuit Design, National Semiconductor

Wednesday, January 31

9:00 am - 10:50 am
Conference Sessions*

12:00 pm – 1:00 pm
Luncheon with Keynote Presentation
Charles Fox, President and Chief Executive Officer, Chameleon Systems

12:30 pm – 1:00 pm
Dessert on the Exhibit Floor

12:30 pm – 6:00 pm
Exhibits Open

2:00 pm – 4:50 pm
Conference Sessions*

4:00 pm – 5:15 pm
Plenary Panel
Design Engineering and the World Wide Web: Where They Meet to Create Ultimate Value

4:00 p.m – 5:15 pm
IP World Forum Conference Panel
Engineering Management Business Considerations in the use of Semiconductor IP

4:00 p.m – 5:15 pm
High-Performance Design Conference Panel
Design for Extreme Data Rate Performance: Reaching toward Theoretical Limits

4:45 pm – 6:00 pm
Exhibit Reception

Thursday, February 1

9:00 am – 12:00 pm
TecForums

*** Conference Sessions are 50-minute presentations**

System-on-Chip Planning Guide

Monday, January 29

9:00 am – 12:00 pm

SC-TF1 • Design Tradeoffs in Developing Personal Access Devices
James Colgan, National Semiconductor

SC-TF2 • Advancements in Designing with FPGAs
Peter Alfke, Xilinx

12:00 pm – 1:00 pm

TecForum Luncheon

1:00 pm – 4:00 pm

SC-TF3 • Platform-Based Design of SOC
Grant Martin, Cadence Design Systems

SC-TF4 • Tutorial on Design Closure
Dr. Olivier Coudert, Monterey Design Systems

Tuesday, January 30

9:00 am – 9:50 am

SC-01 • Techniques to Address Greater On-Chip Performance
Bill Cordan, Palmchip

SC-02 • Vectorless Translation of FPGAs to ASICs: Experiences and Design Tips
Dan Mangen, AMI

10:00 am – 10:50 am

SC-03 • System-on-Chip Multi-Processor for Voice over IP
Doug Chisholm, Tality

SC-04 • Reconfigurable SoC Using an Embedded Module Array
Tomer Buchnik, Chip Express

10:00 am – 12:00 pm

Executive Forum Workshop • The Internet Appliance Market: Business Factors and Technologies That Will Make It Soar

11:00 am – 11:50 am

SC-05 • The Dynamics of SoC Design Methodologies and Application Specific Platforms
Pascal Nsame, IBM Microelectronics

SC-06A • Design Verification: RTL sign-off and Design Intent Validation
Claudionor Coelho, Verplex Systems

SC-06B • Hierarchical Design Methodology for Multi-Million Gate ASICs
Wei-Jin Dai, Silicon Perspective

12:00 pm – 1:00 pm

Opening Keynote Address and Industry Luncheon

12:30 pm – 6:30 pm

Exhibits Open

2:00 pm – 2:50 pm

SC-07 • The Programmable Logic Core: Bringing Configurability to System-on-Chip
John Hesketh, LSI Logic

SC-08 • When All You Have Is Money: Verification Experience at a Start-Up
Sherri Al-Ashari, BrightLink Networks

2:30 pm – 4:00 pm

Executive Forum Workshop • How to Achieve Success With Global Research and Development

3:00 pm – 3:50 pm

SC-09 • FPSLIC for SoC: Micros With Muscle or FPGA With Brains?
Wendy Lockhart, Atmel

SC-10 • Verification Techniques for Processor-Based Communications SoCs
Peter Onufryk, AT&T Laboratories

4:00 pm – 5:15 pm

System-on-Chip Conference Panel • The ASIC/FPGA Battle: Will a Hybrid Solution Win?

4:45 pm – 6:30 pm

Evening Reception on Exhibits Floor

Wednesday, January 31

9:00 am – 9:50 am

SC-11 • Design of a Bluetooth Radio on a Chip
Bernard Goffart, Alcatel Microelectronics

SC-12 • Accelerating Inkjet Printer Design and Verification Through Flexible Hardware Emulation
Brian Levy, Hewlett-Packard

10:00 am – 10:50 am

SC-13 • AMBA Development Board Accelerates Peripheral Verification and Software Development
Curtis Settles, LSI Logic

SC-14 • SoC Design in Six Months: From Concept to Reality
Hari Kotcherlakota, Cadence Design Systems

11:00 am – 12:00 pm

DesignCon Plenary Panel • Design Engineering and the World Wide Web: Where They Meet to Create Ultimate Value

12:00 pm – 1:00 pm

Keynote Address and Industry Luncheon

12:30 pm – 6:00 pm

Exhibits Open

2:00 pm – 2:50 pm

SC-15 • Embedded Power Management in Mixed-Signal ASICs
Marcos Laraia, AMI

SC-16 • Automatic Bus Functional Model Test Bench Generation for PCI-Based Systems
Wayne Armbrust, Wayne Scott Associates

3:00 pm – 3:50 pm

SC-17 • Unified ASIC and FPGA Flows for Timing Convergence
Hichem Belhadj, Actel

SC-18 • Design for Test in Mixed Signal SoC: A Case Study
Krunali Patel, Texas Instruments

4:00 pm – 4:50 pm

SC-19 • A Hierarchical Design Methodology for 50M Gate Designs
Harvey Toyama, Avant!

SC-20 • Designing a Simple FPGA RISC CPU and System-on-Chip
Jan Gray, Gray Research

4:45 pm – 6:00 pm

Evening Reception on Exhibits Floor

Thursday, February 1

9:00 am– 12:00 pm

SC-TF5 • Functional Verification of Hardware and Software in Embedded Systems Designs – ASIC Verification
Eric Johnson, Mentor Graphics

SC-TF6 • Internet-Aware Embedded Systems
Claudionor Coelho, Verplex Systems

To Register
TURN TO PAGE 43

Monday, January 29

9:00 am – 12:00 pm

IP-TF1 • USB 2.0 Function Controller Design and Verification
Runbir Singh, Mentor Graphics

12:00 pm – 1:00 pm

TecForum Luncheon

1:00 pm – 4:00 pm

IP-TF2 • What Constitutes Star IP?
Mark-Eric Jones, MoSys

IP-TF3 • IP Modeling At Different Abstraction Levels in a Top Down Design Flow
Peter Vanbekbergen, CoWare

Tuesday, January 30

9:00 am – 9:50 am

IP-01 • An Intelligent Memory Approach Using Address and Data Port Processing
Les Veal, Infinite Technology

IP-02 • Solving Problems Incurred During Layout of a Soft CPU IP Core for Integration into a VoIP ASSP
Greg Kahlert, Lexra

10:00 am – 10:50 am

IP-03 • IP Implementation in FPGAs
Kevin Edwards, Mentor Graphics

IP-04 • Integration of a DDR Controller into SOC ASIC
Timothy Dell, IBM Microelectronics

10:00 am – 12:00 pm

Executive Forum Workshop • The Internet Appliance Market: Business Factors and Technologies That Will Make It Soar

11:00 am – 11:50 am

IP-05 • Application Extensions for DSP Core
Daniel Martin, Infineon Technologies

IP-06A • When Memories Forget: Soft Errors in Very Deep Sub-micron Memories
Mark-Eric Jones, MoSys

IP-06B • Development and Deployment of Star IP
Alan Gibbons, Synopsys

12:00 pm – 1:00 pm

Opening Keynote Address and Industry Luncheon

12:30 pm – 6:30 pm

Exhibits Open

2:00 pm – 2:50 pm

IP-07 • Clock Tuning Circuit for IP Core Integration in SoC
Yaron Elboim, Oren Semiconductor

IP-08 • Automated IP Core Integration Using Tool Command Language (Tcl)
Bejoy G. Oomman, Genesys Testware

2:30 pm – 4:00 pm

Executive Forum Workshop • How to Achieve Success With Global Research and Development

3:00 pm – 3:50 pm

IP-09 • A Solution for Avoiding Spurious Transitions in Asynchronous Circuits
Sambaran Mitra, WIPRO Technologies

IP-10 • Hardware Description Languages: They Aren't Just for Digital Anymore
Gary Pratt, Mentor Graphics

Tuesday, January 30 (cont.)

3:00 pm – 3:50 pm

IP-11 • 8-Bit Microcontroller With Integrated Programmable Gain Amplifier in 10-bit A/D Signal Path
Volker Soffel, National Semiconductor

IP-12 • Design Case Study: Internet Appliance Development Platform Using Intel StrongArm Processor and Xilinx PCI core
Kent Narveson, Avnet Design Services

4:45 pm – 6:30 pm

Evening Reception on Exhibits Floor

Wednesday, January 31

9:00 am – 9:50 am

IP-13 • Re-Usable IP Takes Center Stage in Rapid Prototyping and Verifying of SoC Design
Leif Rosqvist, Aptix

IP-14 • Real-World Requirements for an IP Reuse System
Tom Simon, Synchronicity

10:00 am – 10:50 am

IP-15 • Verifying Virtual Components and VC-Based SoC Designs
Tom Anderson, 0-In Design Automation

IP-16 • A Fundamental Design Problem: Finding the Right Design
Caroline O'Donnell, The Virtual Component Exchange

11:00 am – 12:00 pm

DesignCon Plenary Panel • Design Engineering and the World Wide Web: Where They Meet to Create Ultimate Value

12:00 pm – 1:00 pm

Keynote Address and Industry Luncheon

12:30 pm – 6:00 pm

Exhibits Open

2:00 pm – 2:50 pm

IP-17 • The Hardware Software Interface. The Weak Link?
Dr. David Lear, Beach Solutions

IP-18 • Web-Based Exchange of Complex DSP IP for Wireless SoC Applications
James Gunn, HelloBrain.com

3:00 pm – 3:50 pm

IP-19 • The Application of Trapezoidal Association of Transistors for Comparators and Sigma-Delta Modulators in a Pre-diffused Digital CMOS Array
Jung Hyun Choi, University of Rio Grande do Sul

IP-20 • Virtual Component Repository: Connecting with Suppliers
Mobashar Yazdani, Hewlett-Packard

4:00 pm – 5:15 pm

IP World Forum Conference Panel • Engineering Management Business Considerations in the Use of Semiconductor Intellectual Property

4:45 pm – 6:00 pm

Evening Reception on Exhibits Floor

Thursday, February 1

9:00 am– 12:00 pm

IP-TF4 8 Internet Intellectual Property Evaluation and SoC Verification: Accelerating Systems Design
Steve Glaser, Simutech

High-Performance System Planning Guide

Monday, January 29

9:00 am – 12:00 pm

HP-TF1 • PCI-X: Designing Advanced I/O
Alan Goodrum, PCI Special Interest Group

HP-TF2 • Improving Code Maintainability and Saving ROM Using Unified Macro Language
Arkady Khasin, MacroExpressions

12:00 pm – 1:00 pm

TecForum Luncheon

1:00 pm – 4:00 pm

HP-TF3 • Signal Integrity Investigation of High Speed/High Density SMT and Compact PCI Connectors
Ulrich Wallenhorst, Harting

HP-TF4 • Functional Validation and Debug of InfiniBand Systems
Perry Keller, Agilent Technologies

Tuesday, January 30

9:00 am – 9:50 am

HP-01 • Using TDR and Frequency Domain Analysis to Ensure Signal Integrity in High-Speed Interconnects
Dima Smolyansky, TDA Systems

HP-02 • LVDS SERDES 660 Mbps Testing Uses JTAG, BIST, and Loopback
Kevin Yee, QuickLogic

10:00 am – 10:50 am

HP-03 • The Engineering Engine and InfiniBand Architecture at Speed
Henri Merkelo, atSpeed Technologies

10:00 am – 12:00 pm

Executive Forum Workshop • The Internet Appliance Market: Business Factors and Technologies That Will Make It Soar

11:00 am – 11:50 am

HP-05 • Advances in High-Speed Design in Dispersively Attenuating Environments Such As Cables and Backplanes
Timothy Hochberg, atSpeed Technologies

HP-06 • GTLP in Live Insertion Applications
Stephen Blozis, Texas Instruments

12:00 pm – 1:00 pm

Opening Keynote Address and Industry Luncheon

12:30 pm – 6:30 pm

Exhibits Open

2:00 pm – 2:50 pm

HP-07A • Design Trade-Offs for High-Speed-Serial Transmission in Lossy Media
Dennis Miller, Intel

HP-07 • Solution Space Analysis: Attacking the High-Speed Analysis Problem: Signal Integrity Software
Douglas Burns, Signal Integrity Software

HP-08 • Improved Method for Characterizing and Modeling Flex-Circuit Based Connectors at 2.5 Gbps
Laurie Taira-Griffin, Packard-Hughes Interconnect

2:30 pm – 4:00 pm

Executive Forum Workshop • How to Achieve Success With Global Research and Development

2:00 pm – 2:50 pm

HP-09A • Broadband Measurements in the Differential Mode: Accurate Determination of Dispersive Attenuation
Timothy Hochberg, atSpeed Technologies

HP-09B • Rigorous Evaluation of Worst-Case Total Cross-Talk
James Rautio, Sonnet Software

HP-10 • Signal Integrity Measurement and the Requirements Imposed by High-Speed Design
Mike Grabois, Fujitsu Network Communications

Tuesday, January 30 (cont.)

4:00 pm–4:50 pm

HP-11 • Using Silicon Technology to Extend the Useful Life of Backplane and Card Subtrates at 3.125 Gbps and Beyond
Paul Galloway, Chip2Chip

HP-12 • A 1.6 G-Bit/s/pin Multi-Level Parallel Interconnection
Haw-Jyh Liaw, Rambus

4:45 pm – 6:30 pm

Evening Reception on Exhibits Floor

Wednesday, January 31

9:00 am – 9:50 am

HP-13A • 2.5 Gbps Backplane Design, Simulation, and Measurement
John Goldie, National Semiconductor

HP-13B • Practical Analysis and Simulation of Lossy Transmission Line
Eric Bogatin, Bogatin Enterprises

HP-14 • Memory Architectures: Analyzing and Probing Rambus, PC133, and Double Data Rate (DDR) SDRAM
Gregg Buzard, FuturePlus

10:00 am – 10:50 am

HP-15 • Signal Integrity Considerations for 10Gbit/s Transmission Over Backplane Systems
Gautam Patel, Teradyne

HP-16 • Design of Sony PlayStation2 Memory Sub-Systems
David Secker, Rambus

11:00 am – 12:00 pm

DesignCon Plenary Panel • Design Engineering and the World Wide Web: Where They Meet to Create Ultimate Value

12:00 pm – 1:00 pm

Keynote Address and Industry Luncheon

12:30 pm – 6:00 pm

Exhibits Open

2:00 pm – 2:50 pm

HP-17 • Demonstrator for Transmission Via Backplane in CMOS-Technology
Helmut Katzier, Siemens AG

HP-18 • Source Synchronous Bus Design and Timing Analysis for High Volume Manufacturable System Interconnect
Ahmed Omer, Intel

3:00 pm – 3:50 pm

HP-19 • A Comprehensive Power Bus Design Procedure for Digital Systems Switching 100 Amps/nsec.
JP Miller, Compaq Computer

HP-20 • Layout Constraints for Signal Integrity on Digital Boards with Sub-Nanosecond Driver Edge Rates
Dr. Lynne Green, Innoveda

4:00 pm – 5:15 pm

High-Performance System Design Conference Panel
Design for Extreme Data Rate Performance: Reaching Toward Theoretical Limits

4:45 pm – 6:00 pm

Evening Reception on Exhibits Floor

Thursday, February 1

9:00 am– 12:00 pm

HP-TF5 • Analysis and Overview of Bus Solutions Overview and Analysis of GTLP/BTL Backplane Design and Operation
Stephen Blozis, Texas Instruments

Monday, January 29

9:00 am – 12:00 pm

WB-TF1 • High-Performance Logic Translation and Clock Distribution ICs Allow New Design Methodologies
Nic Roozeboom, Philips Semiconductors

12:00 pm – 1:00 pm

TecForum Luncheon

1:00 pm – 4:00 pm

WB-TF2 • One-Day System Level Design Environment
Stephen Chappell, Celoxica

Tuesday, January 30

9:00 am – 9:50 am

WB-01 • Performance Evaluation of Gbps Backplane Serial Links
Bilal Ahmad, Cisco Systems

WB-02 • Top Ten Requirements for Service Discovery
Robert Pascoe, Salutation Consortium

10:00 am – 10:50 am

WB-03 • Non-Linear Full Wave Time Domain Solutions using FDTD_SPICE for High-Speed Digital and RF
Raj Raghuram, Applied Simulation Technology

WB-04 • Design and Verification of a UMTS CDMA Rake Receiver
GVL NarasimhaBabu, Synopsys

10:00 am – 12:00 pm

Executive Forum Workshop • The Internet Appliance Market: Business Factors and Technologies That Will Make It Soar

11:00 am – 11:50 am

WB-05 • Overcoming Packaging Limitations in High-Speed Wireless IC Designs
Chris Mueth, Agilent Technologies

WB-06 • Transactional Interactive Messaging
Kayvan Alikhani, MagNetPoint

12:00 pm – 1:00 pm

Opening Keynote Address and Industry Luncheon

12:30 pm – 6:30 pm

Exhibits Open

2:00 pm – 2:50 pm

WB-07 • Probing and Analyzing Communication System Embedded PCI Designs
Gregg Buzard, FuturePlus

WB-08 • Bluetooth Compliance Validation at the RTL Design Stage
John Gallagher, Synplicity

2:30 pm – 4:00 pm

Executive Forum Workshop • How to Achieve Success With Global Research and Development

3:00 pm – 3:50 pm

WB-09 • Design Analyses for Broadband, Non-Interfering, Multiple Access RF Communications Links from User Terminals to Comsat Hub in Two-Way VSAT Networks
Lester Turner, eVox

WB-10
New Processor Advances Make Soft Radio a Reality
Pete Foley, nBand Communications

Tuesday, January 30 (cont.)

4:00 pm–5:15

Wireless and Optical Broadband Design Conference Panel
The Future of Optical Broadband Networking

4:45 pm – 6:30 pm

Evening Reception on Exhibits Floor

Wednesday, January 31

9:00 am – 9:50 am

WB-11 • Open Switching Architectures
Paul Lisenberg, ZettaCom

WB-12 Computers Without Computing
Will Golby, Celoxica

10:00 am – 10:50 am

WB-13 • Fiber Optical Signal Integrity From Deterministic, Random, Periodic Components of a Jitter Signal and Associated Frequency Domain Spectrum
Mike Li, Wavecrest

WB-14 • Vector-Based Graphical Modeling of Physical Layer (PHY) Functions in High-Performance Communications ICs
Eyran Lida, Mysticom

11:00 am – 12:00 pm

DesignCon Plenary Panel • Design Engineering and the World Wide Web: Where They Meet to Create Ultimate Value

12:00 pm – 1:00 pm

Keynote Address and Industry Luncheon

12:30 pm – 6:00 pm

Exhibits Open

2:00 pm – 2:50 pm

WB-15 • Multiplexing LAN Architectures for 3D Wafer Bonding Technologies
Ronald Gutmann, Rensselaer Polytechnic Institute

WB-16 • IP-Centric Architecture for Optical Network Architecture
Krishna Bala, Tellium

3:00 pm – 3:50 pm

WB-17 • SOIS: Smart Optical Interconnection Systems
Karl Gerdom, Harting

WB-18 8 Laser Micro-Machining for Optical Interconnection
Brian Patterson, Tyco Electronics

4:00 pm – 5:15 pm

WB-19 • An Open Platform for the Rapid Prototype and Deployment of Hardware-Based Networking Modules
John Lockwood, Washington University, Saint Louis

WB-20 • When Less Is More: Lowering Insertion Loss in High Density Optical Connectors Is a Key Enabling Technology in Advanced Optical Systems Design
Beth Murphy, Tyco Electronics

4:45 pm – 6:00 pm

Evening Reception on Exhibits Floor

Thursday, February 1

9:00 am– 12:00 pm

WB-TF3 • A Next-Generation Digital Signal Processing Core Ideal for Communications Applications
Scott Beach, StarCore

WB-TF4 • Wireless Local Area Networks: Putting Technology Innovation Into Action
Hatim Zaghloul, Wi-LAN

Sessions by Topical Interest

Product Categories ▼	High-Performance Systems Design	IP World Forum	System-on-Chip Design	Wireless and Optical Broadband Conference
Memories Double Rate SDRAM/Rambus; Controllers; Architectures	HP-14, HP-16	IP-01, IP-04, IP-06B, IP-TF2	SC-01	
PCI, PC133, PCI-X, CompactPCI, USB,1394, AMBA & Other Busses	HP-02, HP-06, HP-14, HR-18, HP-19, HP-TF2, HP-TF3, HP-TF5	IP-03, IP-12, IP-15, IP-17, IP-TF1	SC-01, SC-08, SC-10, SC-13, SC-16, SC-18, SC-20	WB-07
Embedded Design, Micro-processors, Microcontrollers	HP-18, HP-TF1	IP-02, IP-03, IP-11, IP-12, IP-TF2, IP-TF3	SC-03, SC-05, SC-06B, SC-08, SC-13, SC-18, SC-20, SC-TF1, SC-TF5	WB-05, WB-12, WB-10, WB-14, WB-TF1,WB-TF2, WB-TF3
Internet Appliances	Plenary Panel	IP-12	SC-05, SC-TF1, SC-TF6	WB-02, WB-08
Switch-Network-Base Station				WB-01, WB-02, WB-11, WB-13, WB-16, WB-19, WB-TF4
Fiber Optics				WB-11, WB-15, WB-16, WB-17, WB-18, WB-20, Wireless and Optical Broadband Panel
Voice over IP (VoIP)		IP-02	SC-03	
InfiniBand	HP-01, HP-03, HP-05, HP-07, HP-09, HP-13, HP-13C, HP-Panel, HP-TF4			
Bluetooth/Handhelds			SC-11	WB-02, WB-04, WB-06, WB-08
Networks			SC-08	WB-06, WB-09, WB-13, WB-14, WB-15, WB-16, WB-TF4
Copper-Optical Interface	HP-03, High-Performance System Design Panel			WB-15, WB-17, Wireless and Optical Broadband Panel
Analog and Mixed Signal	IP-11, IP-19		SC-05, SC-15, SC-18	WB-11
RF/Wireless/3G WCDMA			SC-05	WB-03, WB-04, WB-05, WB-06, WB-09, WB-10, WB-15, WB-19
Signal Processing		IP-05, IP-11, IP-18		WB-10, WB-TF1, WB-TF3
Configurable Chip Architecture	HP-TF1	IP-05, IP-06	SC-01, SC-10	WB-TF2, WB-12, WB-13
High-Speed-Serial	HP-02, HP-06, HP-07, High-	Performance Panel		
Connector Models	HP-01, HP-17			WB-01, WB-07, WB-18, WB-20
Microstrip, Buses, Interconnects	HP-03, HP-06, HP-07C, HP-08, HP-12, HP-13C, HP-18, HP-20, High-Performance Panel, HP-TF5			WB-01, WB-03, WB-17, WB-18, WB-19, WB-20
Backplane	HP-11, HP-13, HP-15, HP-17, HP-19, High-Performance Panel, HP-TF5			
Power Management	HP-19		SC-15	
Hybrid - Programmable Logic/ASIC			SC-04, SC-07, SC-09, System-on-Chip Design Panel	WB-TF1, WB-TF2
Dynamically Reconfiguring Hardware				WB-10, WB-12, WB-14, WB-16, WB-TF2
FPGA-ASIC - IC-VLSI	HP-TF1	All Sessions	All Sessions	WB-12, WB-13, WB-14, WB-TF2
Chip I/O-chip Packaging/ 3Dmultiplexing	HP-01, HP-TF1		SC-TF2	WB-05, WB-15
Chip Circuit Design		IP-07, IP-09, IP-11, IP-19		
Platform Based Design		IP-08	SC-01, SC-11, SC-14, SC-TF3	
Prototyping and Emulation		IP-12, IP-13	SC-12, SC-13	
Chip Timing Convergence		IP-03	SC-02, SC-17, SC-19, SC-TF2, SC-TF4	
Chip Layout	HP-TF1	IP-02	SC-06B	
Static Functional and Formal Verification	HP-01, HP-08, HP-20	IP-15	SC-02, SC-06, SC-TF5	
Standards Compliance				WB-04, WB-07, WB-08
Test Benches	HP-05, HP-09, HP-14	IP-03, IP-08, IP-09	SC-08, SC-10, SC-16, SC-TF5	
Modeling, Integration of Simulated and Measured Models/Components	HP-01, HP-05, HP-07C, HP-08, HP-10, HP-12, HP-15, HP-16, HP-20			WB-05, WB-11
Lossy-Dispersive, Attenuation-Electromagnetic Analysis-TDR	HP-01, HP-03, HP-05, HP-09, HP-11, HP-12, HP-13, HP-13C, HP-19			
SPICE – FDTD Simulation	HP-01, HP-06, HP-11, HP-12			WB-01, WB-03, WB-11
Source-Synchronous Bus	HP-18			
Test and Measurement	HP-01, HP-02, HP-05, HP-08, HP-11, HP-12, HP-13, HP-13C, HP-14, HP-TF4, HP-TF2, HP-TF1	IP-04, IP-08, IP-13	SC-13. SC-18	WB-07

SC-TF1 Monday, January 29 • 9:00 am – 12:00 pm

System-on-Chip Design Conference

Design Tradeoffs in Developing Personal Access Devices


Colgan

James Colgan, Business Unit Manager, Information Appliance Division, National Semiconductor

The information appliance (IA) market has experienced dramatic growth since National Semiconductor introduced the first mobile information appliance at Fall Comdex 1998 in the form of its National Semiconductor® Geode v WebPAD v Personal Access Device. The WebPAD appliance brought together technologies from various disciplines to create a mobile device that brings all of the benefits of the Internet, without the disadvantages of the PC. National Semiconductor combined a highly integrated x86 instruction set compatible processor solution, various optional wireless transmission standards, advanced power management and battery technology with LCD display technology. This provided the ideal hardware platform for real time operating system (RTOS) vendors and system integrators (SI) to place their small, fast, robust and reliable software stacks to create a true internet appliance: &instant-on 8, no &blue-screen 8 and intuitive user interface. In this TecForum, National Semiconductor and its partners will focus on WebPAD platforms within the newly developing IA market, the various form factors now in production and some of the issues and considerations surrounding the development and deployment of information appliances.

Mr. Colgan is creating and driving products for a new consumer information appliance market: the personal access device market. He is responsible for strategic and operational business plans as well as managing customer and partner relationships. Mr. Colgan began his National career in Japan as an engineer supporting the introduction and growth of a new family of integrated processors into this market.

SC-TF2 Monday, January 29 • 9:00 am – 12:00 pm

System-on-Chip Design Conference

Advancements in Designing With FPGAs


Alfke

Peter Alfke, Director, Applications Engineering, Xilinx

This TecForum will provide design guidelines and expand upon new technologies recently introduced for FPGAs. Massive architectural parallelism in FPGAs can provide a dramatic performance improvement for DSP applications, outperforming the most advanced DSP chips. A digital radio example is used to illustrate. Design and tool technology tips are provided on timing assurance, thermal considerations and signal integrity. These include: timing convergence with new synthesis tools, improved timing prediction from hierarchical routing structures, clock management, thermal considerations and thermal management in packaging, and innovative methods to reduce or eliminate signal reflections to solve board signal integrity issues.

Mr. Alfke has been the director of applications engineering at Xilinx since 1988. His previous positions have included director of applications engineering at AMD, applications manager at Fairchild Semiconductor, and applications manager at Zilog. Early in his career, Mr. Alfke served as a computer design engineer in Sweden. He has more than 40 years of industry experience.

Attend the VSIA's Compliance Forum

Monday, January 29 • 4:15 pm – 6:00 pm

with Social Hour following!

IP-TF1 Monday, January 29 • 9:00 am – 12:00 pm

IP World Forum

USB 2.0 Function Controller Design and Verification


Singh


Chang

Runbir Singh, Director, IP Cores, Mentor Graphics

Angela Chang, Product Marketing Manager, IP Cores, Mentor Graphics

Thomas Chow, Technical Marketing Manger, IP Cores, Mentor Graphics

The need for higher performance connectivity has driven the development of the USB2.0 specification capable of delivering 480 Mbits per second. A key enabler for this solution is the USB function controller residing in the high performance peripheral and interfacing with the USB PHY. This TecForum examines the successful development of a re-usable USB2.0 core for SoC integration. The architectural requirements and solutions are first reviewed. Two key interfaces are discussed in detail: the VCI bus and the UTMI. Then the reuse methodology constraints are examined, and examples of the application in the current design are highlighted. Successful implementation requires in-depth verification, and the three-step verification plan is presented with an example in the verification environment.

Mr. Singh has been a technology professional in the semiconductor industry for more than 20 years. He has been a major contributor at various high-tech companies such as Fairchild Semiconductor, National Semiconductor, Hyundai Electronics, and VLSI Technology.

Ms. Chang has 15 years of experience in the semiconductor industry. She is responsible for product management at Mentor Graphics' Inventra IP Business Unit.

Mr. Chow has 16 years of experience in the electronics industry. He is currently responsible for technical marketing of Intellectual Property cores at Mentor Graphics.

HP-TF1 Monday, January 29 • 9:00 am – 12:00 pm

High-Performance System Design Conference

PCI-X: Designing Advanced I/O

Alan Goodrum, PCI-X Workgroup Chair, PCI Special Interest Group

The PCI local bus is the internal I/O interconnect of choice for most of today's computer systems. Its speed and simplicity have enabled its proliferation throughout the computing industry, telecommunications and industrial applications. Recently, faster peripheral applications such as gigabit ethernet, ultra160 SCSI and fibre channel have created new and immediate demands for higher bandwidth. In addition, complex host system chip sets and the demand for efficient bridges have created a need for protocol enhancements that allow devices to work not just faster, but smarter. Some highlights and new features of the presentation will include: the benefits PCI-X has over conventional PCI; how PCI-X maintains hardware and software compatibility with conventional PCI; and the ease of migration to PCI-X from conventional PCI OEMs, IHVs, SI designers, and board designers.

Mr. Goodrum is a Staff Fellow in the Industry Standard Server Group of Compaq Computer. Prior to working on PCI-X, Mr. Goodrum was instrumental in the development of the PCI Hot-Plug Specification and has been a member of the PCI Protocol Workgroup and the PCI Bridge Workgroup since 1994. Currently at Compaq, Mr. Goodrum is part of a group that develops new technology such as PCI-X and PCI Hot-Plug that will be needed by industry-standard servers several years in the future.

HP-TF2 Monday, January 29 • 9:00 am – 12:00 pm

High-Performance System Design Conference

Improving Code Maintainability and Saving ROM Using Unified Macro Language


Khasin

Arkady Khasin, Software Developer, MacroExpressions

This TecForum focuses on code reusability in product-line, model year, and/or twin-variants environment. It shows that many maintenance/reuse problems are solved without runtime penalty by sharing parameters among languages and by performing complex static (compile-time) initialization. A language-independent macro language is described which enables these capabilities while (partially) preserving look and feel of the target language. Unified macro language allows developers to provide simple solutions to "simple" problems, like parameter sharing, but it makes solutions to complex problems (like guaranteed two-step search) possible. Unimal reduces code maintenance complexity, the project's memory requirements and "ROM-izes" that otherwise had to be calculated in runtime.

Dr. Khasin has more than 20 years of experience in ROMable embedded applications ranging from custom devices to mass-produced controllers. He currently develops embedded code and techniques for maintainability, reusability and efficiency.

WB-TF1 Monday, January 29 • 9:00 am – 12:00 pm

Wireless and Optical Broadband Design Conference

High-Performance Logic Translation and Clock Distribution ICs Allow New Telecommunication, Networking, and Base Station Infrastructure Design Methodologies


Roozeboom

Nic Roozeboom, International Product Marketing, Philips Semiconductor

Kristina Avrionova, Applications Engineer, Logic Product Group, Philips Semiconductor

Jeff DeAngelis, Product Family Manager, Philips Semiconductor

This session presents a new generation of general-purpose ICs (GPICs) that simplify design methodology and provide benefits in the area of signal integrity by offering repeatable, dependable logic translation and high-speed clock distribution. Several new IC products will be presented including: Compact logic translator ICs that translate from either LVDS to differential PECL or vice versa at 800Mbps; a Universal Logic Translator (both logic translation, multiplexing and de-multiplexing functions) for 800Mbps LVDS and differential PECL in the areas of telecommunication, networking, and base station infrastructure platforms; and high-speed clock distribution ICs, either differential PECL or LVDS signaling, at speeds in excess of 1.5GHz. The session presents the purpose and design of these ICs, demonstrates performance and illustrates typical measurement scenarios and challenges. The authors will show reference designs that illustrate typical application considerations.

Mr. Roozeboom leads Philips Semiconductor's efforts to create general-purpose ICs focused on networking, telecom, and base station infrastructure. He helped define the world's first USB Audio Conversion IC and other digital audio conversion and USB ICs.

Ms. Avrionova is an experienced high-speed interconnect ASIC designer for networking and telecom applications.

Mr. DeAngelis is a manager of innovative GPIC product solutions that address the telecom, networking, and base station infrastructure marketplace.

SC-TF3 Monday, January 29 • 1:00 pm – 4:00 pm

System-on-Chip Design Conference

Platform-Based Design of System-on-Chip


Martin

Grant Martin, Chief Technologist, Front End Products, System Level Design and Verification Group, Cadence Design Systems

Augusto de Oliveira, Chief Architect, Consumer Systems Business Unit, Philips Semiconductor

David Barringer, Vice President, Marketing, Digital Video Interactive Segment, Philips Semiconductor

This TecForum covers the basic trends of design reuse evolution which have led to the platform-based design approach to SoC. It discusses the implications and requirements of shifting to this design approach, and illustrates it with a number of industry examples. Finally, it touches on design methodology requirements for adopting platform-based design and outlines a number of evolution paths for the future. This overview will be followed by a detailed examination of a particular platform, the Nexperia Digital Video Platform, and its use. The Nexperia Digital Video Platform is the first incarnation of Philips Semiconductor's System-on-Chip platform strategy, aimed at consumer systems applications. Mr. de Oliveira's presentation starts with the market and technical motivation behind the Philips Nexperia platform approach. Next, Mr. de Oliveira will discuss the key technical aspects of the Nexperia DVP Software and Hardware Architecture. He will cover the current implementation as well as how Philips is planning to evolve and extend the approach. Finally, Mr. de Oliveira will touch upon the non-technical challenges related to the deployment of a platform approach across a large corporation like Philips Semiconductors. Mr. de Oliveira will address the need for organization and management processes that are aligned to the platform strategy. Specifically, the issues of IP management, IP roadmapping, and IP creation will be addressed. Finally, Mr. Barringer's presentation will focus on the use of Nexperia-DVP for the creation of a family of products addressing the interactive digital set-top box market.

Mr. Martin worked for Burroughs in Scotland for 6 years and Nortel/BNR in Canada for 10 years prior to his current position with Cadence Design Systems. He co-authored the book "Surviving the SOC Revolution: A Guide to Platform-Based Design," published by Kluwer Academic Publishers in November of 1999.

Mr. de Oliveira is responsible for Digital VideoPlatform software and hardware architectures. Before joining the Consumer Systems group of Philips Semiconductor, Mr. de Oliveira held various technical and management positions with Philips in Brazil, The Netherlands, and the USA, including department manager for the Philips MIPS Technology Center and chief technology officer. and systems development manager for the Handheld Computing Group.

SC-TF4 Monday, January 29 • 1:00 pm – 4:00 pm

System-on-Chip Design Conference

Tutorial on Design Closure


Coudert

Olivier Coudert, Technical Manager, Monterey Design Systems

The issues that designers will face, as they embark upon deep-submicron designs at 0.18 micron and below, will be covered by this TecForum presented by Monterey Design Systems. The methodology to address these design closure issues will be covered in detail and various alternative strategies will be critiqued. The TecForum will act as a good review of the design challenges with deep sub-micron and how design productivity can be maintained even with these technical challenges. The most popular ASIC design flow and COT flows will be reviewed and how closely designers can hold to these familiar flows will be covered with new tools such as Sonar™ and Dolphin™.

Dr. Coudert joined Monterey Design Systems in 1998 to lead the synthesis and timing group. There he has architected and developed logic optimizations within a multi-threaded placement, timing, and routing environment. Prior to his current role, Dr. Coudert was a member of the advanced technology group at Synopsys and a research scientist at DEC Paris Research Labs. He has worked on a wide spectrum of topics, including formal verification, logic synthesis, and combinatorial optimization.

IP-TF2 Monday, January 29 • 1:00 pm – 4:00 pm

IP World Forum

What Constitutes Star IP?


Jones


Knowles

Mark-Eric Jones, Vice President and General Manager, Intellectual Property, MoSys

Brian Knowles, Vice President, Marketing, MIPS

Although both so-called "star" and "commodity" silicon Intellectual Property (IP) are needed to enable the next generation of system-on-chip (SOC) designs, the benefits and characteristics of these two types of IP are very different. The speakers will illustrate some of the unique technical characteristics found in star IP and show how these characteristics result in very different technical benefits and business models compared with commodity IP. A framework will be presented to help the objective assessment of whether IP is truly differentiated. Although focused on star IP, the presentations will also illustrate the value and benefits of commodity IP and how these two complementary forms of IP should be used in the SoC design process.

Mr. Jones managed Mentor Graphics' "Inventra" IP business before joining MoSys. He was chief executive officer and founder of 3Soft, which was one of the first businesses to adopt the silicon IP business model in 1988. Mr. Jones was involved in founding RAPID (the IP industry business association) in 1996 and has served as chairman of its board of directors.

Mr. Knowles is responsible for product marketing, industry segment marketing, semiconductor licensee marketing programs, partner programs for software and tools, and marketing communications activities. For his role, Mr. Knowles draws on 20 years of experience in building partnerships for the application of microprocessor technology in the telecom/networking and consumer electronics markets.

IP-TF3 Monday, January 29 • 1:00 pm – 4:00 pm

IP World Forum

IP Modeling at Different Abstraction Levels in a Top-Down Design Flow


Vanbekbergen


Matta

Peter Vanbekbergen, Director, European Engineering, CoWare

Ashwin Matta, Product Manager, Synergy Systems Design

David Gilbert, Product Leader, Synergy Systems Design

Markus Buecker, Design Engineer, Infineon Technologies

Patrick Runkel, Design Engineer, Infineon Technologies

The first paper will explain how the CoWare N2C solution enables the modeling of processors at different levels of abstraction for simulation and synthesis purposes. As such, the CoWare solution enables the delivery of a "Design Re-use Platform" allowing easy re-use of bus architectures, processors and software development tools during the whole design process. This process starts from a high level executable specification (untimed functional descriptions) and goes via hardware/software partitioning down to implementation (RTL and target object code). Modeling the IP at different levels of abstraction, in a consistent way, enables informed design decisions at those different levels of abstraction. This results in a fast design process with high quality results. In the second paper, a methodology for creating an application specific virtual prototype (ASVP) in C for highly complex SoCs using RTL-accurate building blocks for its components is presented. The RTL-accurate C technology (RTL-C) maintains bit, pin and clock-edge accuracy that is essential for functional verification of the SoC. The productivity and accuracy issues for creating these RTL-C models are addressed through automation. Upon integration with source-level debuggers, the C virtual prototype becomes a fast, flexible and clock-edge-accurate simulation engine for verifying real-time embedded software. This approach is compared with alternative solutions and its efficacy is supported by simulation data. Finally, the

IP-TF3 Continued

third paper examines the use of a real-life design method for setting up a verification environment that can be used for system definition at the algorithmic level and also later for verification of the design through the whole semiconductor design flow. Consistency is guaranteed beginning from definition through RTL verification to gate-level sign-off verification. The method is based upon modeling the algorithmic level in a C dialect and then setting up a test bench in a schematic like algorithm development tool, COSSAP. The test bench can be used for concurrent simulation with a RTL simulator or for pattern generation of functional patterns. The test bench elements can be defined in a flexible environment (REFLECTIVE) to increase the re-use factor of the verification environment.

Mr. Vanbekbergen joined CoWare in 1997. Prior to his current role, he worked for Synopsys, where he did research and development work in the areas of asynchronous synthesis, low power synthesis, and synthesis for FPGAs.

Mr. Matta joined CAE Plus, now Synergy Systems Design, in April 1999, contributing his talents in the areas of design methodology, verification, and design and specification of EDA software tools. His current activities include guiding software tool development through customer and market interactions.

Mr. Gilbert joined CAE Plus, now Synergy Systems Design, in August 1996, with the responsibility of creating cycle-accurate C models and integrating these models into entire systems simulations in C. Currently, he is product lead for ArchGen, Synergy Systems Design's behavioral modeling environment.

Mr. Buecker has been with Infineon Technolgies AG since 1999, working on the definition and implementation of integrated circuits for broadband communication systems. He came to Infineon Technologies from Siemens semiconductors where he was involved with the development of integrated circuits for ISDN systems.

Mr. Runkel joined Siemens AG, semiconductors group, now Infineon Technologies AG, in June 1995, where he was involved in the hardware development of digital TV circuits. Since February 2000 he is responsible for a new satellite receiver IC.

HP-TF3 Monday, January 29 • 1:00 pm – 4:00 pm

High-Performance System Design Conference

Signal Integrity Investigation of High-Speed/High-Density SMT and Compact PCI Connectors


Wallenhorst

Ulrich Wallenhorst, Director, Advanced Interconnection Solutions, Harting

Dirk Michel, Signal Integrity Engineer, Harting

Markus Witte, Signal Integrity Engineer, Harting

This TecForum gives an insightful view into Signal Integrity investigation of high pin-count connectors, with 3D FEM-simulations, SPICE simulations, and measurement data of high speed/high density SMT and compactPCI 2mm hard-metric connectors. The SMT-connector in a 1mm pitch is a blind-mateable board-to-board connector, where the balanced signal travels over a copper-pair. This differential-transmission environment works at speeds up to 10Gbps per pin-pair. Here very small, and well-balanced card-to-backplane conductor guidance yield next generation transmission speeds. Controlled impedance, transmission losses, and crosstalk are considered. The compact PCI study concentrates on measurements of the eye opening of differential signals between 2.5-4.0 Gbps/pair, by de-embedding the real connector-influence. The authors show pin-in-hole effect, crosstalk, and skew influences. Limits of pin-in-hole and the advantages of SMT are derived, while emphasizing the overrated influence of integrated shielding.

Mr. Wallenhorst headed the internal accredited EMC center prior to his current role as director of the advanced interconnection solutions department at the connector company Harting.

HP-TF4 Monday, January 29 • 1:00 pm – 4:00 pm

High-Performance System Design Conference

Functional Validation and Debug of InfiniBand Systems


Keller


Taylor

Perry Keller, Senior Engineer, Digital Design PGU, Agilent Technologies

David Taylor, Strategic Solutions Manager, Electronic Product and Solutions Group, Agilent Technologies

InfiniBand is a significant new technology for the ultra high speed interconnect of server-class computer clusters and their I/O subsystems. The design and verification of InfiniBand based systems requires expertise over a huge range of technologies from microwave design to protocol analysis. This TecForum focuses on the benefits and details of InfiniBand technology, engineering challenges, InfiniBand bring up, developing device driver software, functional validation and debug of InfiniBand based systems using protocol aware real time bus analyzers, and compliance verification and interoperability verification techniques. Examples of validation using potential ITA compliance and interoperability working group specifications will be described. Based upon InfiniBand implementation examples, it will be shown how silicon, modules and systems will be switched on, which critical parameters must be verified and how this can be done in an efficient way. This will help hardware and hardware/software design teams apply these tools most effectively when turning on their InfiniBand based systems.

Mr. Keller is responsible for the logic analyzer support of computer system busses. He has more than 20 years of experience at Agilent Technologies in the areas of high-speed hardware and ASIC design and validation, software engineering, product marketing, and project management.

Mr. Taylor has influence over all of Agilent's bench-top instruments; his current focus is InfiniBand program management. Mr. Taylor's 11-year career with HP/Agilent has been primarily focused on developing logic analyzer solutions for the computer industry.

WB-TF2 Monday, January 29 • 1:00 pm – 4:00 pm

Wireless and Optical Broadband Design Conference

One-Day System Level Design Environments


Chappell

Stephen Chappell, Manager, Design Services, Celoxica

Celoxica will unveil a revolutionary system-level design environment that makes a significant step towards reducing the design process to one day. The tutorial will examine a new approach to rapid design that enables application specialists to increase their productivity and take concepts directly to silicon. The session will also illustrate the business potential of flexible hardware by demonstrating how Internet reconfigurable platforms can support a myriad of applications such as VOIP, MP3, and processor cores running games. Attendees will be given the opportunity to learn how to use these tools, design their own hardware applications for this device, and observe its operation within a few hours.

Dr. Chappell manages the design consultancy arm of Celoxica, applying new methodologies to embedded systems design, from the development of reusable intellectual property (IP) cores to services for complete system development.

DesignCon is an informative and energizing conference that presents an excellent mix of the latest design ideas and applications for the design community.

SC-TF5 Thursday, February 1 • 9:00 am – 12:00 pm

System-on-Chip Design Conference

Functional Verification of Hardware and Software in Embedded Systems Design


Johnson


Tokic

Eric Johnson, Marketing Manager, SoC Verification Group, Mentor Graphics

Dave Tokic, Manager, Strategic Relationships, Verisity Design

Mentor Graphics and Verisity provide verification tools that individually address portions of the verification problem for hardware/software system design. Mentor Graphics' Seamless is used for hardware/software co-verification and Verisity's Specman Elite for hardware functional verification. While both of these tools work very well to isolate design problems, they have the capability to do much more, together. Integration between these two verification environments adds the capability to perform functional verification of the hardware and software with combinational testing. The embedded software can now be controlled and verified through the 'e' code running in Specman Elite. Methods for the best use of each tool and the capabilities available through the integration will be discussed in this workshop.

Mr. Johnson has been with Mentor Graphics for over 10 years. His current responsibilities include managing EDA partnerships for Mentor Graphics' seamless and product marketing for C model extensions in seamless. He has been involved in product marketing for the last four years. Prior to that Mr. Johnson worked in various software development positions.

Mr. Tokic started with Verisity in April 1998. Prior to that, he worked at Synopsys as manager of their in-Sync EDA partnership program and as a corporate applications engineer. Before Synopsys, Mr. Tokic was a design engineer at Frequency Electronics Labs.

SC-TF6 Thursday, February 1 • 9:00 am – 12:00 pm

System-on-Chip Design Conference

Internet-Aware Embedded Systems


Coelho

Claudionor Coelho, Staff Engineer, Verplex Systems

Diogenes da Silva, System Analyst, Computer Science Department, Federal University of Minas Gerais

An Advanced RISC Machines Presenter

In the last few years there has been a significant effort to connect embedded systems to the Internet. This connection adds many new features to embedded systems. However, it differs from desktop Internet connection, since embedded systems have severe constraints on CPU power and speed, display capability, persistent storage, fault tolerance and costs. This TecForum presents an overview of the Internet technology including Internet protocols, the advantages of connecting embedded systems to the Internet, and a general software and hardware layered architecture for Internet-aware embedded systems. We will present popular hardware and software components used in industrial environments, with real examples. We also address the issue of designing graphical user interfaces for embedded systems with limited resources.

Dr. Coelho is currently with Verplex Systems, on a sabbatical leave from the Computer Science Department of the Federal University of Minas Gerais where he has been an associate professor since 1996. He has published over 40 conference and journal papers in several areas including formal verification, hardware-software co-design, embedded systems, wearable computers and Web-enabled embedded systems.

Mr. da Silva has research interests in the areas of specification, synthesis and validation of hardware/software systems, real-time systems, and embedded hardware/software systems.

IP-TF4 Thursday, February 1 • 9:00 am – 12:00 pm

IP World Forum

Internet Intellectual Property Evaluation and SoC Verification: Accelerating Systems Design

Steve Glaser, Vice President, Marketing, Simutech

The impact of the Internet on business has virtually changed the way we think and act and has ignited a wave of change in the electronics business. It has significantly impacted the procurement processes and is starting to impact systems and SoC design. This TecForum presents methodologies and technologies that enable component evaluation and qualification over the Internet, hardware-software co-development, and full SoC verification. The forum will provide designers with insight into how to realize significant benefits that include the exploration of a broader range of IP components, faster and more confident design-in of those components, and the fastest path available through component integration and verification.

Mr. Glaser has spent over 16 years in the electronics industry, developing a broad industry perspective through experiences in system house, semiconductor, and EDA market segments. Before joining Simutech, he was vice president of strategic marketing at Cadence Design Systems. In this role, Mr. Glaser led the definition and creation of the VSI alliance, helped define the industry's methodology direction toward platform-based design, and led the definition of Cadence's recently communicated front to back technology and methodology roadmaps.

HP-TF5 Thursday, February 1 • 9:00 am – 12:00 pm

High-Performance System Design Conference

High-Performance Bus Solutions Overview and Analysis of GTLP/BTL Backplane Design and Operation

Blozis

Stephen Blozis, Strategic Business Development, Texas Instruments

Ernest Cox, Senior Applications Technician, Texas Instruments

Jose Soltero, Standard Linear and Logic Applications, Texas Instruments

Johannes Huchzermeier, Data Transmission Applications Engineer, Texas Instruments

This tutorial provides an overview of all single-ended and differential bus solutions and an in-depth analysis of backplane line theory and design techniques. This will allow the design engineer to learn which technology is most appropriate for their requirements, what types of devices are available in each technology, and how to optimize signal integrity and data throughput. The authors will distribute material highlighting the different key parameters of each bus solution and the maximum data throughput of each technology. A 20-slot demonstration backplane will be used to show construction techniques and signal integrity under different loading and termination conditions.

Mr. Blozis has been with Texas Instruments for over two years with the majority of that time focused on the new GTLP and VME high performance bus solution families, including customer interface/education, new product schedule, design goal data sheets specifications and applications report generation.

Mr. Cox is responsible for customer support, new product development, backplane design/operation/simulations and application report generation. He spent twenty years with the U.S. Air Force in the electronics research and development field.

Mr. Soltero has most recently been the strategic marketing and applications engineer for commodity data transmission devices offered by TI. His efforts include customer interface/education, new product proposal creation, design goal data sheet specifications and applications report generation.

WB-TF3 Thursday, February 1 • 9:00 am – 12:00 pm

Wireless and Optical Broadband Design Conference

A Next-Generation Digital Signal Processing Core Ideal for Communications Applications

Shay

Scott Beach, Platform Marketing Manager, StarCore

Kevin Shay, Computer Architect, Lucent Technologies

Emerging standards in both wireless and broadband applications are requiring digital signal processors (DSPs) to provide increasing levels of performance at much lower levels of power dissipation and code size. Product time to market pressures are reducing the amount of software development time. This tutorial will describe the application development challenges amplified by next-generation communications systems, and how the StarCore SC100 DSP architecture addresses those challenges. The tutorial will include a detailed look into application development with the SC100 architecture, and how it can help reduce code development time. In the second half of the tutorial the authors focus on the key DSP architectural concepts that address high performance without compromising power dissipation and cost (code density). They will also look at the features within the SC100 architecture that make it compiler friendly, maximizing the opportunity for development of DSP code in C, which is key to reducing application development time.

Mr. Beach is responsible for market analysis and new product definition for the first generation of StarCore DSP cores. He has 6 years of experience in the DSP industry, including previous positions in Texas Instruments' catalog and data communications organizations.

Mr. Shay is primarily responsible for algorithm performance analysis. His DSP experience includes former Research and development positions with Ericsson's Cellular Terminal Design Center and Home Wireless Networks.

WB-TF4 Thursday, February 1 • 9:00 am – 12:00 pm

Wireless and Optical Broadband Design Conference

Wireless Local Area Networks: Putting Technology Innovation Into Action

Zaghloul

Hatim Zaghloul, Chairman and Chief Executive Officer, Wi-LAN

This TecForum case study will examine how a wireless design is incorporated into practical use. There are several advantages of this wireless application, which speaks to its efficiency as a "last mile" solution. The demand is growing for high-speed Internet access, encouraging public utilities to look for a cost-effective way to deploy the system. Addressing the needs of the public, private, and industry sectors, Midland PUC provides high-speed access for the rapid transfer of engineering designs, specifications, and parts purchase. The cost of wireless deployment is significantly lower than fiber and copper.

Dr. Zaghloul is recognized internationally as a leading innovator in the field of OFDM radio technology. He is the co-inventor of two new wireless technologies: Wide-band Orthogonal Frequency Division Multiplexing (W-OFDM) and Multi-code Direct Sequence Spread Spectrum (MC-DSSS). Dr. Zaghloul is the inventor of Network Living™, which allows seamless network communication through current and future technologies.

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SC-01 Tuesday, January 30 • 9:00 am – 9:50 am

Techniques to Address Greater On-Chip Performance

New Architectures and System Level IC Design

Bill Cordan, Vice President, SoC Services, Palmchip
Billy Mills, Senior Staff Engineer, SoC Architectures, Palmchip

Platform-based design techniques can offer a means to meet the time-to-market demands of system-on-chip product development. Integration platforms are built upon an SoC architecture. Some architectures may limit the ability to address particular applications or meet their performance requirements. The authors of this paper present a configurable platform-based design architecture that uses reusable, configurable architectural logic allowing platform-based SoC development. Architectural solutions that increase the available on-chip bandwidth are also presented. Bringing configurability to the SoC architecture also adds considerable power to creating derivative platform-based designs and expands the range of SoC application and performance derivatives that can be addressed while reducing development time-to-silicon.

SC-02 Tuesday, January 30 • 9:00 am – 9:50 am

Vectorless Translation of FPGAs to ASICs: Experiences and Design Tips

Chip Implementation Solutions

Dan Mangen, Manager, Design Technology, AMI

This paper describes what has been learned from completing over 30 vectorless translations from FPGAs to ASICs. There are methods available other than dependence upon vectors to verify a design. Formal verification software will guarantee a Boolean equivalent netlist, while static timing can be used to help verify that the timing of an ASIC will match what is presently being used. Using the static timing information from the FPGA and converting that to constraints for the layout of the ASIC allows the timing to be consistent. Installing SCAN, using an IDDQ methodology, and timing driven layouts are examples of completing over 30 successful vectorless translations.

SC-03 Tuesday, January 30 • 10:00 am – 10:50 am

System-on-Chip Multi-Processor for Voice over IP

New Architectures and System Level IC Design

Doug Chisholm, SoC Design Centre, Tality

This paper is a design case study of a system-on-chip (SoC) for Voice-over-IP (VoIP) appliances. The SoC integrates the popular ARM and OAK processors and is now available as standard part. The ARM processor was integrated to run the real-time-operating-system (RTOS), Internet protocol software and the application. Two identical OAK DSP subsystems were integrated to execute the speech vocoder (G.723.1) and the modem (V.34) software. Asynchronous communication between the ARM and deeply embedded DSP systems is via mailboxes designed to support interactive messaging and data downloading. A platform based methodology enabled software co-development and architecture validation. This methodology minimized the amount of software porting between the emulation board, prototype boards and the final product.

SC-04 Tuesday, January 30 • 10:00 am – 10:50 am

Reconfigurable SoC Using an Embedded Module Array

Chip Implementation Solutions

Tomer Buchnik, Manager, SoClet Products Group, Chip Express
Ofer Hareuveni, Managing Director, Chip Express
Uzi Yoeli, Chief Technology Officer, Chip Express

One could observe system-on-chip (SoC) as a design approach that is trying to mimic the well-established system-on-board design approach and adapt it to the ASIC arena. In this session the speakers analyze SoC through this analogy, and identify the specific points where current SoC solutions are not offering sufficient solutions. Then, they introduce a unique technology for bridging most of these barriers, using the top metal level programmable module array technology.

SC-05 Tuesday, January 30 • 11:00 am – 11:50 am

The Dynamics of SoC Design Methodologies and Application-Specific Platforms

New Architectures and System Level IC Design

Pascal Nsame, SoC Methodology Team Lead, ASIC Product Solutions, IBM Microelectronics

The characterization of system-on-chip (SoC) and the difficulty of designing and validating these complex devices suggest an automated approach to SoC design. This paper discusses platform creation and platform deployment challenges that enable a platform-based design strategy within a corporation. It proposes a set of attributes associated with an application specific platform for SoC with an emphasis on IP reuse requirements that supports market reality. The automation and enabling technologies discussed in this paper support first-pass success SoC designs.

SC-06A Tuesday, January 30 • 11:00 am – 11:50 am

Design Verification: RTL Sign-Off and Design Intent Validation

Design Verification and Test

Claudionor Coelho, Staff Engineer, Verplex Systems
Michal Siwinski, Applications Engineer, Verplex Systems

The constant growths in design sizes and aggressive design cycles have increased the verification gap between what is designed and what is verified. As a result, new methodologies must be used to increase the verification coverage. Design intent verification using formal verification techniques is becoming a viable solution addressing the verification gap and RTL sign-off. In this paper we will introduce BlackTie, a new breed of static functional verification tools targeting full chip multi-million gate designs. This design intent validation solution complements simulation by exhaustively proving commonly found functional errors that are hard to detect. Incorporating design intent validation into the design and verification flows significantly reduces the overall verification time and effort, thus shortening the time to market.

SC-06B Tuesday, January 30 • 11:00 am – 11:50 am

Hierarchical Design Methodology for Multi-Million Gate ASICs

Chip Implementation Solutions

Wei-Jin Dai, Vice President, Research and Development, Silicon Perspective

There is an insatiable requirement for higher integration, faster, more complex technology. However the physical implementation of multi-million gate designs can be a major bottleneck. The productivity of the back-end designers does not seem to be tracking the increase in gate complexity. This paper illustrates a successful hierarchical methodology applied to two actual designs recently implemented. The first is a Pentium III desktop multimedia processor that includes 7.1 million gates where the designers partitioned the full chip into six blocks without sacrificing die size area. The second is a network processor chip consisting of 8 million gates with the challenge to partition the design into modules that could be implemented with the back-end tools while ensuring routability for the highly interconnected design.

SC-07 Tuesday, January 30 • 2:00 pm – 2:50 pm

The Programmable Logic Core: Bringing Configurability to System-on-Chip

Chip Implementation Solutions

John Hesketh, Senior Manager, SoC Methodology, LSI Logic

The paper describes LSI Logic's Programmable Logic Core PLC product, and how it is being integrated into the company's system on a chip design flow from synthesis through to final layout. Included in this description is the method used to integrate the PLC programming capability and tools with the ASIC design flow. The architecture of the PLC and its technical specifications including capacity, performance, and power are described as is the testing methodology used. A typical application with a configurable AMBA bus peripheral will be used to demonstrate the capability of programmable logic cores.

SC-08 Tuesday, January 30 • 2:00 pm – 2:50 pm

When All You Have Is Money: Verification Experience at a Start-Up

Design Verification and Test

Sherri Al-Ashari, Manager, Design Verification Group, BrightLink Networks

This paper presents a verification methodology for a switch ASIC that BrightLink designed and verified. It includes a discussion of tradeoffs of time vs. money since BrightLink was a very small start-up. It discusses the tools used, as well as the tradeoffs made as to the level of integration from block verification up to system verification. The focus of the paper is on the single chip verification and block verification. The author discusses the use of a hardware modeler that was used to verify the microprocessor interface, and device drivers.

SC-09 Tuesday, January 30 • 3:00 pm – 3:50 pm

FPSLIC for SoC: Micros With Muscles or FPGA With Brains?

Chip Implementation Solutions

Wendy Lockhart, Applications Engineer, Atmel

FPSLIC is a new architecture that provides an innovative approach to system-on-chip design. Instead of implementing a design in a million gate FPGA, this solution provides hard IP cores in gate array with programmable logic on the same silicon. The second advance is that the existing 8 bit AVR micro products run at 12MHz, giving approximately 10 MIPs of performance. Running the AVR out of SRAM gives up to 30 MIPs of performance. Application of this new technology is described with a design case. The system design software provides a new approach to programmable logic. For design verification the FPGA hardware may be simulated in parallel with the instruction set simulator for the microcontroller.

SC-10 Tuesday, January 30 • 3:00 pm – 3:50 pm

Verification Techniques for Processor-Based Communications SoCs

Design Verification and Test

Peter Onufryk, Technology Consultant, AT&T Laboratories

Dan Steinberg, Design Engineer, AT&T Laboratories

With each function added to a SoC, it is necessary not only to verify the function in isolation, but also its interactions with other functions of the SoC. The result can be an exponential increase in the number of test cases required to fully verify a design. New verification techniques are needed since traditional block level test benches do not scale well to complex system level verification. New techniques are described for the verification of Banyan, a highly integrated programmable communications SoC. Banyan combines a RISC core, a complex 16-channel descriptor based DMA controller, and system support logic (SDRAM controller, timers, etc.) with seven communications interfaces (two ATM interfaces, a 10/100 Ethernet interface, a USB device interface, a TDM interface, two serial channels, and an I2C-bus interface).

SC-11 Wednesday, January 31 • 9:00 am – 9:50 am

Design of a Bluetooth Radio on a Chip

New Architectures and System Level IC Design

Bernard Goffart, Manager, Technical Marketing, Alcatel Microelectronics

Having solved some of the most difficult chip design and system integration issues facing electronic design engineers, chip and system designers of wireless telephone hand-sets are taking on another challenge, that of adding the Bluetooth technology. The task is to design a second additional radio for the handset that will communicate with other near-neighbor appliances. The many varied applications anticipated for the Bluetooth technology present new design opportunities, yet difficult design challenges. This paper describes how design engineers at Alcatel Microelectronics and their development partners confronted the challenges to design one of the most novel first-out Bluetooth solutions.

SC-12 Wednesday, January 31 • 9:00 am – 9:50 am

Accelerating Inkjet Printer Design and Verification Through Flexible Hardware Emulation

Chip Implementation Solutions

Brian Levy, Senior Productivity Engineer, Hewlett-Packard
Tim Kutscha, ASIC Design Engineer, Hewlett-Packard

The increasing complexity of Inkjet printer systems coupled with continuous consumer demands for new features, lower cost, and faster performance requires significant improvements in the design and verification process to deliver competitive products. Custom hardware emulation (using FPGAs) reduces time-to-market by enabling firmware development and system integration before the ASIC design finishes. This paper presents a connectivity solution for custom emulation systems using a Laser Programmable Wiring Plate (LPWP). All connectivity between the FPGAs and the system are routed on the LPWP, allowing complete interconnect flexibility and small interconnect delays. By eliminating the need to design a new printed circuit board for each ASIC, this solution allows system emulation to start 3–4 months earlier, further reducing time-to-market.

SC-13 Wednesday, January 31 • 10:00 am – 10:50 am

AMBA Development Board Accelerates Peripheral Verification and Software Development

New Architectures and System Level IC Design

Curtis Settles, Manager, Processor Core Applications, LSI Logic

This session describes how to prototype and program an AMBA AHB or APB peripheral in the same environment as the ASIC design. A development board complete with the most commonly used memory systems, daughter card sockets with the same uni-directional functionality as the on-chip AMBA busses, and a full set of microcontroller peripherals is the solution. The designer may port the peripheral's RTL code directly to an FPGA on one daughter card socket and after the processor of choice and other system peripherals are plugged into other sockets, the designer is ready to start running code while monitoring it with a logic analyzer.

SC-14 Wednesday, January 31 • 10:00 am – 10:50 am

SoC Design in Six Months: From Concept to Reality

Chip Implementation Solutions

Hari Kotcherlakota, Senior Engineering Manager, System-on-Chip Design Services, Cadence Design Systems
Alan Baillie, Chief Consulting Engineer, Cadence Design Systems

Complex system-on-chip designs are demanding a new set of design skills and methodologies such as platform based design approaches. This session describes such methodologies used by the Cadence Digital IC design team to tape-out several complex SoCs over the last three years. Descriptions of real-life experiences of the problems that can occur with an incomplete methodology and how such problems can be avoided are included. Modular platforms that are being produced are designed to ease the integration of IP blocks into new applications and include the provisioning of an environment for developing software as early as possible in the development cycle where a microprocessor is one of the IP block being integrated.

SC-15 Wednesday, January 31 • 2:00 pm – 2:50 pm

Embedded Power Management in Mixed-Signal ASICs

Chip Implementation Solutions

Marcos Laraia, System Architect, AMI
Farshad Dailami, Mixed-Signal Design Engineer, AMI

With the increasing complexity of today's ASICs, power management features normally found at the board or system level are being embedded. On-chip voltage regulators, standby modes, inrush current control, and efficient power distribution are becoming commonplace. This architectural approach contributes to a lower overall cost, increased reliability, and a more compact product than what would be possible with off-the-shelf components. On the other hand, all constraints and trade-offs should be understood so that an optimized system architecture can be defined. This paper presents some practical power management solutions recently used by AMI on its mixed-signal ASICs. Design techniques for the most frequent building blocks are discussed and a detailed case study is presented.

SC-16 Wednesday, January 31 • 2:00 pm – 2:50 pm

Automatic Bus Functional Model Test Bench Generation for PCI-Based Systems

Design Verification and Test

Wayne Armbrust, Design Engineer, Wayne Scott Associates
Lizann Epley, Verification Engineer, TestBench Tools, SynaptiCAD
Daniel Notestein, President, SynaptiCAD

Design verification is currently one of the most time consuming and expensive steps in the design process. Test benches are difficult to write, understand, and maintain in the phase of design changes if they are not properly constructed. Reusable bus-functional models provide an efficient, consistent, and maintainable method of design verification. Test bench design requires that the designer overcome many pitfalls, such as type conversion, signal driver conflict, race conditions and synchronization issues. Automatic test bench generation allows the designer to focus on the overall design rather than language specific problems. This case study will demonstrate how the automatic generation of Verilog, VHDL and Vera test benches can overcome these obstacles for a PCI-based system.

SC-17 Wednesday, January 31 • 3:00 pm – 3:50 pm

Unified ASIC and FPGA Flows for Timing Convergence

Chip Implementation Solutions

Hichem Belhadj, Applications Manager, Actel

FPGA and ASIC designers face several barriers when targeting programmable technologies and find the need for specific design tools. In addition, there is often a long and costly learning curve in order to use efficiently the FPGAs capabilities and to achieve the best performance. However, the most daunting challenge is related to timing convergence and closure. This paper introduces a clear design methodology to target a fine-grained FPGA that takes full advantage of both ASIC and FPGA synthesis tools and investigates the implications on place and route tools. It ensures not only better quality of results but also post-synthesis and post-layout timing convergence.

SC-18 Wednesday, January 31 • 3:00 pm – 3:50 pm

Design for Test in Mixed-Signal SoC: A Case Study

Design Verification and Test

Krunali Patel, ASIC Designer, Texas Instruments

David Kimble, ASIC Designer, Texas Instruments

Advances in the process technology and migration to smaller geometries are driving higher levels of integration. One result of immense integration is the creation of large complex mixed signal devices. Multiple data-paths, multiple I/O interfaces, multiple voltages and multiple clock domains in these systems make verification and test of such systems complex, costly and time consuming, both at the RTL and silicon stages. This paper describes some of these challenges and describes solutions for them through a case study. The subject mixed signal device is an audio/video IEEE 1394, a link layer integrated with the IEEE1394, a physical layer, an embedded processor and on chip memory. This session highlights that testability is best achieved when planned during the initial stages of the chip definition.

SC-19 Wednesday, January 31 • 4:00 pm – 4:50 pm

A Hierarchical Design Methodology for 50M Gate Designs

Chip Implementation Solutions

Harvey Toyama, Jupiter Product Manager, Avant!

As process geometries shrink and designs get larger, faster and more complex, GigaHertz speeds, tens of millions of gates, analog and full-custom blocks present new challenges to designers. A new methodology must be used to allow designers to implement these new designs. Hierarchy is a must since the design sizes preclude flat approaches. RTL purification is needed to save months of debug time. Silicon accurate synthesis, re-synthesis and optimization must be available to achieve early design timing closure. Correlation to place and route must be within a few percent to correctly contain the risk the front-end team faces in releasing a design.

SC-20 Wednesday, January 31 • 4:00 pm – 4:50 pm

Designing a Simple FPGA RISC CPU and System-on-Chip

Chip Implementation Solutions

Jan Gray, President, Gray Research

This paper presents the complete design of a simple FPGA RISC processor/microcontroller and system-on-chip in synthesizable Verilog. It provides an example of a simple RISC instruction set architecture that is easily targeted by the lcc retargetable C compiler, and describes how to implement every part of the processor: instruction store, decoding, register file, operand selection, ALU, result selection, memory load and store, and program sequencing and branching. The role of soft CPU cores in hybrid FPGA plus hard-core parts devices is configured at power-up by an external configuration ROM. It has an 8 row _ 12 column array of configurable logic blocks (CLBs), four dual-ported synchronous 256x16 block RAMs, and 60 I/O blocks (IOBs) in a sea of programmable interconnect.

IBIS Open Forum at DesignCon 2001

Monday, January 29, 2001 • 4:30 pm – 5:00 pm

The EIA IBIS Open Forum (over 30 member companies) is responsible for producing the ANSI/EIA-656-A standard for IBIS (Input Output Buffer Information Specification). IBIS models are used for high-speed digital printed circuit board design and analysis. The IBIS format describes Input/Output characteristics and uses behavioral V-I and V-T tables that protect proprietary process and circuit information. You are invited to participate in IBIS meetings and e-mail reflector discussions. Sent your request to ibis-request@eda.org.

DesignCon is the only design-engineering event where you can learn the industry's latest techniques and theories through comprehensive conference sessions and then immediately see them in application at the hands-on demonstrations and exhibits that are linked to the conferences. At DesignCon, you will find solutions to the most demanding design challenges and then discover the products that will help put your knowledge to use immediately. You'll also have plenty of opportunity to interact with your peers and colleagues in the design engineering community at several corporate-sponsored luncheons and receptions held each day.

The exhibit floor of DesignCon is an excellent venue to establish and maintain industry relationships.

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IP-01 Tuesday, January 30 • 9:00 am – 9:50 am

An Intelligent Memory Approach Using Address and Data Port Processing

Architecture, Specification, and Planning

Les Veal, Vice President, Infinite Technology Corporation
Neal Stollon, Director, SoC Technology, Infinite Technology Corporation

Enhanced address and datapath functions and subsequent in-line processing that can boost the performance of existing and future RAM devices has been labeled as part of an emerging technology collectively known as Intelligent Memories. Integration of distributed and reconfigurable architectural blocks that encapsulate basic DRAM and SRAM technology can extend the level of standalone performance that can be performed on-chip. This paper discusses distributed and reconfigurable datapath processing technology to improve performance of Intelligent Memories systems and the use of block architectures that support independent processing of both the addressing of the memory and processing of the input/output data. This approach has advantages in overall flexibility in modes of operations and support of diverse modes of data and address granularity of memory processing.

IP-02 Tuesday, January 30 • 9:00 am – 9:50 am

Solving Problems Incurred During Layout of a Soft CPU IP Core for Integration into a VoIP ASSP

Design Implementations

Gregory Kahlert, Applications Engineer, Lexra

One of the toughest problems an intellectual property cores supplier faces is allowing a customer to configure the soft IP and then have the customer request that the supplier produce the final layout that can be dropped into the customer's design. To further complicate the task, the customer has a Cadence back-end flow and the IP vendor has a Savant! back end flow. This paper details a few of the problems that were solved to make this happen on time and without a design iteration when Lexra produced the layout for a reconfigured RISC CPU core for its customer, a fabless IC manufacturing building a 250-channel VoIP chip in which the RISC CPU was to control a number of VoIP codes.

IP-03 Tuesday, January 30 • 10:00 am – 10:50 am

IP Implementation in FPGAs

Architecture, Specification, and Planning

Kevin Edwards, IP Product Specialist, Mentor Graphics

FPGAs can offer benefits such as a prototyping platform for large ASIC projects, reducing the risk element often associated with IP. This session analyzes the challenges and benefits when using IP in FPGA design, ways in which implementation could be speeded up, and factors that can slow it down. EDA tools can assist, particularly if they have good links to the FPGA back-end flow, the capacity to cope with high-end FPGAs, and an easy way to import IP. The issues are discussed in the context of a full design flow containing IP evaluation and selection, integration, verification, and place & route.

IP-04 Tuesday, January 30 • 10:00 am – 10:50 am

Integration of a DDR Controller into SoC ASICs

Design Implementation

Timothy Dell, Senior Applications Engineer, Microelectronics Division, IBM

While embedded DRAM can offer a designer great bandwidth, it can't be upgraded in the field and it can't be made as cheaply as discrete DRAM. Thus the stage is set for aggressive designs where the base memory is embedded and expansion memory is provided external to the SOC. Of course, such an approach is not without its challenges. This paper investigates the integration of a DDR SDRAM memory port into a system on a chip ASIC with 32MB of embedded DRAM. Issues such as bandwidth matching, on-chip core busses, DDR interface timing, and technology selection are examined. A case study utilizing the IBM SA-27E Design System is presented.

IP-05 Tuesday, January 30 • 11:00 am – 11:50 am

Application Extensions for DSP Core

Architecture, Specification, and Planning

Daniel Martin, Senior Architect, Infineon Technologies
Philippe Bettler, Technical Marketing Manager, Infineon Technologies
Jinan Lin, Senior Application Engineer, Infineon Technologies

New applications like next generation wireless phones require many more MIPS than any DSP can deliver. The "new" MIPS are not all traditional MAC based operations. Hardware coprocessors complement general-purpose DSPs for specialized, "new" MIPS-intensive tasks. Also DSP cores must reach a very competitive level of efficiency in terms of power consumption per function. These extreme requirements are driving designers to request configurable DSP instruction sets and SoC architectures with scalable MIPS. This paper describes the Infineon Carmel DSP (Carmel 20xx), a configurable architecture utilizing PowerPlug™ modules that allocate user-defined execution units side-by-side with standard execution units. PowerPlug™ MAC and Viterbi allowed us to reach up to 4 times faster performances on the most time consuming algorithms found in next generation wireless phones.

IP-06A Tuesday, January 30 • 11:00 am – 11:50 am

When Memories Forget: Soft Errors in Very Deep Sub-Micron Memories

Design Implementation

Mark-Eric Jones, Vice President and General Manager, Intellectual Property, MoSys

It is well established that semiconductor memories are subject to bit errors introduced by the bombardment of alpha particles and cosmic rays. The soft error rate (SER) is the metric used to describe these errors. At high enough levels, SER impacts the system reliability and requires corrective actions. Research has shown a close correlation between new process generations and the memory type. This paper presents measured data showing surprising results for SER of various memory design processes. Designers may well have to reconsider some architectural and technology choices in semiconductor product design to correctly cater to the problem of memory soft errors.

IP-06B Tuesday, January 30 • 11:00 am – 11:50 am

Development and Deployment of Star IP

Design Implementation

Alan Gibbons, IP Methodology Manager, Synopsys

Current system-on-chip (SoC) developments call for an integration of configurable IP with a complexity beyond that of commodity IP into an area know as Star IP. Integration of highly advanced microprocessor IP and communication based IP utilizing proprietary algorithms into a single VLSI device is now becoming more common. In order to support this level of integration, Star IP providers require a methodology which supports both the creation of Soft IP that is configurable by a licensee as well as the creation and delivery of abstract views of this IP, protected through a hardening process. This paper discusses the underlying technical issues and presents a proven methodology that addresses these issues. The methodology presented supports the automatic creation of abstract views of hardened soft IP as well as the deployment of such models into an SoC design environment.

IP-07 Tuesday, January 30 • 2:00 pm – 2:50 pm

Clock Tuning Circuit for IP Core Integration in SoC

Design Implementation

Elboim Yaron, Project Manager, VLSI, Oren Semiconductor

Ran Ginosar, Head, VLSI Systems Research Center, Technnion-Israel Institute of Technology

Avinoam Kolodny, Researcher

SoC design depends heavily on effective reuse of semiconductor intellectual property (IP), enabling a reasonable time to market. Clock distribution has become an increasing problem for SoC design. Different IP cores clock delays are among the major obstacles in merging IP cores into a single synchronized SoC. This paper describes a clock tuning circuit, which enhances design flexibility. The tuning circuit inserts programmable delays between the clock distribution network and each IP core, such that clock alignment and synchronization are achieved. Design iterations are eliminated with the use of the tuning circuit, saving cost and effort.

IP-08 Tuesday, January 30 • 2:00 pm – 2:50 pm

Automated IP Core Integration Using Tool Command Language

Design Implementation

Bejoy Oomman, President, Genesys Testware

Widespread adoption of design reuse using IP cores by IC designers has been stymied by the difficulty of integrating IP cores into systems on chip (SoC). IP core integration consists of interconnecting the IP core with other modules, reconfiguring IP core for usage scenario, verifying the correct operation of this subsystem by interfacing it to self-checking test benches, synthesizing the IP core to the target library, and re-verifying the gate level sub-system using self-checking test benches. This process is time consuming and error prone. The author describes use of the tool command language (Tcl) to improve the process. The effective use of Tcl scripts for IP core integration is illustrated by describing in detail the architecture of Gtshell™: an automated tool for built-in self-test (BIST) IP core integration.

IP-09 Tuesday, January 30 • 3:00 pm – 3:50 pm

A Solution for Avoiding Spurious Transitions in Asynchronous Circuits

Design Implementation

Sambaran Mitra, Senior Engineer, VLSI Systems Design, WIPRO Technologies

This session describes a buffer and compare circuit that masks spurious transitions on a vector-signal (multiple bits). In asynchronous circuits where there is no global-sequencing-signal (i.e. clock) the sequencing may be done implicitly with the help of transitions on signals itself. If the signal is a multi-bit signal, then there is a problem in using its transition as a sequencing event. This is because in the real circuit, all the bits of a multi-bit signal will never be driven at the same instant. This will result in spurious transitions. The focus of the paper is to describe a real design solution that gives glitch free transitions without having a global-timing-signal when a bit-vector is wrapped with a buffer-and-compare-circuit.

IP-10 Tuesday, January 30 • 3:00 pm – 3:50 pm

Hardware Description Languages: They Aren't Just for Digital Anymore

Design Implementation – Analog and Mixed Signal

Gary Pratt, Technical Marketing Manager, Analog/Mixed-Signal Products Group, Mentor Graphics

The ideal analog and mixed signal simulation environment will allow algorithmic investigations at the hardware system level, architectural trade-offs at the behavioral level, and detailed design at the transistor level; using VHDL-AMS, Verilog-A, VHDL-D, Verilog-D, C, and SPICE modeling interchangeably. This presentation shows the use of analog HDL modeling in the top-down design of a clock recovery PLL for a CDMA transceiver from specification to the transistor level. These models will then be used in the bottom-up verification of the complete multi-million transistor mixed-signal CDMA transceiver (after they are calibrated to precisely match the transistor level design). An introduction to VHDL-AMS, and how that language compares with Verilog-A, is included as an appendix.

IP-11 Tuesday, January 30 • 4:00 pm – 4:50 pm

8-Bit Microcontroller With Integrated Programmable Gain Amplifier in 10-Bit A/D Signal Path

Design Implementation – Analog and Mixed-Signal

Volker Soffel, Marketing Manager, Application and Development Tools, National Semiconductor

Many of today's typical analog signal processing systems are built around a microcontroller with an integrated A/D converter. However, the maximum amplitude of the analog signals to be processed is often not large enough to utilize the full dynamic range of the integrated A/D. Designers typically use external OpAmps to amplify those signals. In this paper a programmable gain operational amplifier is integrated between the analog input multiplexer and a 10-bit successive approximation A/D. The microcontroller software can program different gain factors for each of the analog inputs, thus eliminating the need for any external OpAmps. The performance characteristics are discussed together with approaches on addressing common design challenges, like offset correction. The speaker also discusses the challenges of emulating the analog functionality integrated on a microcontroller, and a method that allows superior analog emulation capability.

IP-12 Tuesday, January 30 • 4:00 pm – 4:50 pm

Design Case Study: Internet Appliance Development Platform Using Intel StrongArm Processor and Xilinx PCI Core

Design Implementations

Kent Narveson, Design Engineer, Avnet Design Services

Warren Miller, Vice President, Marketing, Avnet Design Services

This case study presents the design, by Avnet Design Services, of an Internet appliance development platform. This design utilizes an Intel StrongArm processor (SA1110) as the main processing engine and a Xilinx Spartan-II FPGA to interface the processor to the PCI bus. The Xilinx PCI core was used to implement the interface between the StrongArm Processor and the PCI bus. This design case study will share the key points we learned about the design of the development platform, both at the architecture design level and at the FPGA PCI core level. Specific tricks and tips that can be used in other designs will be shared making the session valuable to hardware, FPGA and system designers.

IP-13 Wednesday, January 31 • 9:00 am – 9:50 am

Re-Usable IP Takes Center Stage in Rapid Prototyping and Verifying of SoC Design

Verification

Leif Rosqvist, Chief Operating Officer, Aptix

To close the current "RTL productivity gap" the two closely related issues of IP reuse and verification of an SoC in its intended environment must be addressed. This session discusses the findings of a leading IC design team that evaluated the verification alternatives available. The industry is experiencing a shift away from simulation only centric verification. This session also discusses the architectural considerations of the competing options and offers a strategy for IP block-level evaluation and verification that leads naturally to complex SoC verification using hardware rapid prototyping and emulation techniques.

IP-14 Wednesday, January 31 • 9:00 am – 9:50 am

Real-World Requirements for an IP Re-Use System

IP Deployment

Tom Simon, Business Development Manager, Synchronicity

Building an IP reuse system seems very straightforward. Just create and maintain a list of IP and make it visible to users via the Web. But a robust system must have advanced searching capabilities, sophisticated access control for its many users and suppliers of IP, and comprehensive communication tools. An IP block qualification process within the reuse system is necessary to significantly raise the quality of the IP and its documentation. A reuse system becomes part of the IP supplier's development system, enabling complete IP life cycle management. A well-designed reuse system becomes an integrated part of the IP consumer's design methodology and is much more effective when combined with internal design and project management systems.

IP-15 Wednesday, January 31 • 10:00 am – 10:50 am

Verifying Virtual Components and VC-Based SoC Designs

Verification

Tom Anderson, Vice President, Applications Engineering, 0-In Design Automation

This session covers a range of topics related to the verification of virtual components (VCs) and system-on-chip (SoC) designs that include VCs as building blocks. The stage is set by some examples of VCs and then the challenge of verifying VCs in stand-alone mode is covered. Various methods for testing and verifying VCs are presented, with a special emphasis on how the stand-alone VC effort can be leveraged in the test and verification of the full SoC. The paper closes by surveying emerging technologies that are changing the way that VCs and SoCs are verified, including on-chip busses, white-box verification and semi-formal verification.

IP-16 Wednesday, January 31 • 10:00 am – 10:50 am

A Fundamental Design Problem: Finding the Right Design

IP Deployment

Caroline O'Donnell, The Virtual Component Exchange

The designer's job is difficult. Companies frequently face the 'make or buy' decision. Several factors impact this choice: a poorly developed infrastructure for sharing and trading constrains the third party SIP market. Engineers face numerous problems in finding and evaluating SIP…and then the legal problems begin. This paper explores the solution offered by the Virtual Component Exchange (VCX) – the marketplace developed by the SoC industry. The lack of an industry standard for profiling a Virtual Component and the resulting problems have been solved; the difficulties in obtaining evaluation data when needed, have been solved. This session explains how.

IP-17 Wednesday, January 31 • 2:00 pm – 2:50 pm

The Hardware Software Interface: The Weak Link?

Design Implementation

David Lear, Chief Technologist, Beach Solutions

Today's SoC products comprise dozens of IP blocks containing thousands of address-mapped registers. These massive interfaces directly impact project time scales, because associated with this interface are not only the issues of basic hardware design and driver software, but also verification, debug, documentation, project management and then reuse. Using an object-oriented representation of a generic embedded system, objects, data and associated relationships can be captured in a common data standard. Directly from this one source, many data views required throughout an SoC project can then be automatically generated. All information is captured just once, facilitating reuse within a project, and for future designs.

IP-18 Wednesday, January 31 • 2:00 pm – 2:50 pm

Web-Based Exchange of Complex DSP IP for Wireless SoC Applications

IP Deployment

James Gunn, Associate, HelloBrain.com
Shiv Balakrishnan, General Manager, DSP Business Unit, HelloBrain.com

This session addresses the Web-based exchange of complex DSP IP for rapidly emerging wireless SoC opportunities. First, various forms of IP are discussed based on the typical design flow from system level algorithms to integrated hardware and software implementation. Second, an overview of the evolution from the current 2G to 3G cellular standards is discussed. Third, the infrastructure and tools that are anticipated to be required to support an efficient exchange of complex IP are discussed. Next, HelloBrain.com's Web-based IP exchange technology is discussed. Finally, the anticipated benefits of Web-based complex IP are discussed.

IP-19 Wednesday, January 31 • 3:00 pm – 3:50 pm

The Application of Trapezoidal Association of Transistors for Comparators and Sigma-Delta Modulators in a Pre-Diffused Digital CMOS Array

Design Implementation – Analog and Mixed Signal

Jung Hyun Choi, Integrated Circuit Designer, Microelectronics Group, Federal University of Rio Grande do Sul
Sergio Bampi, Professor, Federal University of Rio Grande do Sul

There are advantages in using the trapezoidal association of transistors (TAT) for mixed analog-digital systems applications on pre-diffused digital arrays like the sea-of-transistors (SOT). TAT emulates the behavior of a single full-custom transistor, which should have an arbitrary geometry, using only a composition of regularly placed minimum-length transistors in a linear-matrix style SOT. TAT achieves an analog performance that is equivalent to the single transistor. Second-order sigma-delta modulators for specific applications using TAT on SOT also exist. Simulation and experimental results are for technologies at 1.0mm and 0.5mm minimum-lengths.

IP-20 Wednesday, January 31 • 3:00 pm – 3:50 pm

Virtual Component Repository: Connecting With Suppliers

IP Deployment

Mobashar Yazdani, ASIC Technical Engineer, Hewlett-Packard
Jean Christophe Pautrat, Engineer, Research and Development, Hewlett-Packard
Eric Kadyrov, Engineer, Research and Development, Hewlett-Packard
Genny Chen, Engineer, Research and Development, Hewlett-Packard

This session describes a system that aids transfer and cataloging of external IP used in product generation. IP must be evaluated for functional completeness, design quality, and the ability to integrate it in SoCs. This effort is usually time consuming and many viable IP solutions can be missed because of time and resource constraints. The speakers have devised means to encapsulate and transfer external IP information to a central HP database. The IP specifications are encapsulated in the form of name value pairs and the transfer format lends itself to be written out by suppliers which have XML based systems. The authors describe the encapsulation, representation and transmission mechanism of our solution.

VSIA's Compliance Forum at DesignCon 2001

Monday, January 29, 2001 • 4.15 pm - 6.00 pm — with social hour to follow

The Virtual Socket Interface Alliance (VSIA) invites you to attend its forum on VSIA Compliance at DesignCon. Besides presenting an overview of the process of determining if your virtual components (VCs) are compliant with VSIA Specifications, this forum will explain the VSIA's Deliverables Document, which is the central reference for all VSIA Specifications and referenced IP. This forum will include the perspectives of both IP developers and system integrators. IP developers will discuss the value of the compliance auditing exercise in determining the completeness of their products and how they compare to the other products. A detailed description of how to fill out VSIA Compliance Reports will also be described. The system integrators will focus on the value of reviewing the compliance of different competing products and show how to compare them. Join us for this discussion and enjoy refreshments in the social hour following. For reservations, please contact *jennifer@vsi.org.*

DesignCon Exhibits

Visit the exhibits of DesignCon to have a first hand look at new technology and solutions available to you from Electronic Design, Semiconductor, IP and System OEM companies.

Exhibit Hours

Tuesday, January 30	12:30 pm – 6:30 pm
Wednesday January 31	12:30 pm – 6:00pm

Reception Hours:

Tuesday, January 30	4:45 pm – 6:30 pm
Wednesday January 31	4:45 pm – 6:00 pm

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HP-01 Tuesday, January 30 • 9:00 am – 9:50 am

Using TDR and Frequency Domain Analysis to Ensure Signal Integrity in High-Speed Interconnects

Extending Physical Limits – InfiniBand

Dima Smolyansky, Product Marketing Engineer, TDA Systems

This session presents simple techniques for the characterization of high-speed interconnects from TDR measurements. A process for computing an equivalent SPICE model for interconnects and for characterization of input die and package capacitance is presented. The resulting models help designers predict reflections, ringing and crosstalk in high-speed digital systems, ensuring that signals propagate through the board with minimal distortion. The authors cover techniques for obtaining frequency domain information (both spectrum and S-parameters) for interconnects from TDR measurements, and provide suggestions on how to use this information to help with high speed interconnect characterization.

HP-02 Tuesday, January 30 • 9:00 am – 9:50 am

LVDS SERDES 660 Mbps Testing Uses JTAG, BIST, and Loopback

Signal Driver Technology – LVDS, PECL, GTLP

Kevin Yee, Director, Applications and Product Planning, QuickLogic

Sean Large, Product Engineer, QuickLogic

As the demand for bandwidth increases, engineers move from shared parallel architectures to high-speed serial bus structures. This leads to more sophisticated test and verification methods. Digital communications analysis has moved from simple set-up and hold measurements to more complicated eye-diagram analysis and bit-error-rate-testing, accommodating data transmission rates up to and beyond 660 Mbps. This paper will present verification, characterization and testability methods utilizing JTAG, BIST, and loopback modes. It will also discuss the use of state-of-the-art testing equipment including Digital Communications Analyzer and Bit-Error-Rate-Testers for QuickLogic's new series of ESP (Embedded Standard Products): QuickSD (a family of LVDS SERDES devices).

HP-03 Tuesday, January 30 • 10:00 am – 10:50 am

The Engineering Engine and InfiniBand Architecture at Speed

Extending Physical Limits – InfiniBand

Henri Merkelo, Principal, Technical Staff, AtSpeed Technologies

The momentum for increases in digital speed is unprecedented and so is its effect on both copper and optical technologies. The digital speeds achieved on subsystems and the high speeds targeted for future systems are both straining and energizing the engineering resources needed to implement future strategies at the desired speeds, at the most attractive costs. This session establishes the practical as compared to the perceived boundaries of copper-based versus optoelectronically-based high-speed technologies. The constantly changing and contested reachable "limiting distances" via the two technologies, at a given cost, provide examples and impetus for the theme.

HP-05 Tuesday, January 30 • 11:00 am – 11:50 am

Advances in High-Speed Design in Dispersively Attenuating Environments Such as Cables and Backplanes

Extending Physical Limits – InfiniBand

Timothy Hochberg, Technical Staff, AtSpeed Technologies

Henri Merkelo, Principal, Technical Staff, AtSpeed Technologies

Michael Resso, Product Manager, Agilent Technologies

This session considers advances in design automation and predictive analysis for high-performance digital networks that transmit information through dispersively attenuating paths. The speakers discuss differential measurements and modeling of dispersive attenuation characteristics, eye-pattern prediction, and signal conditioning design. Measurement-based modeling of complex structures is valid if the spectrum of the model data rate is within the measured characteristic bandwidth. Tools provide automated processing of measured data, determination of EPD and equalization circuit parameters for specified data rates, propagation, and optimization.

HP-06 Tuesday, January 30 • 11:00 am – 11:50 am

GTLP in Live Insertion Applications

Signal Driver Technology – LVDS, PECL, GTLP

Stephen Blozis, Strategic Business Development, Texas Instruments

Ernest Cox, Senior Applications Technician, Texas Instruments

Timothy Minnick, Senior Engineer, System Interconnect, Texas Instruments

Jose Soltero, Standard Linear and Logic Applications, Texas Instruments

This session presents design issues required for card insertion into energized systems without disrupting active signal data and the protective circuitry needed for given isolation levels. Using a specially designed backplane, they explore and analyze several power-sequencing schemes using HSPICE simulations correlated to actual backplane waveforms. Optimized power sequencing recommendations are provided. The backplane pin precharge, Power Up 3-State and Partial Power Down features in Texas Instruments' new GTLP high performance bus interface devices are examined. Nanosecond discontinuities are also examined using Tyco Electronics' new Quiet Mate™ resistive tip technology as a way to control this phenomenon.

HP-07A Tuesday, January 30 • 2:00 pm – 2:50 pm

Design Trade-Offs for High-Speed Serial Transmission in Lossy Media

Extending Physical Limits – InfiniBand

Dennis Miller, Senior Design Engineer, Technology Development, Intel

High-speed serial transmission (HSS) technology, particularly the imminent release of the InfiniBand standard, requires an upgrade to standard approaches. This presentation describes the major challenges involved in design of a physical link between HSS devices, and then presents a fairly easy to understand method of mathematically approximating the tradeoffs between the loss budget, crosstalk, common-mode conversions, and equalization in an HSS link. This presentation explains the reasons that frequency-dependent loss at GigaHertz frequencies cause signal jitter. Also it addresses the microwave characteristics of FR4. Attendees will be left with an understanding of how and why budgeted parameters interact and can be traded for each other.

HP-07B Tuesday, January 30 • 2:00 pm – 2:50 pm

Solution Space Analysis: Attacking the High-Speed Analysis Problem – Signal Integrity Software

Extending Physical Limits – Analysis Tools

Douglas Burns, Principal Consultant, Signal Integrity Software
Stephen Coe, Signal Integrity Consultant, Signal Integrity Software
Barry Katz, President, Signal Integrity Software
Walter Katz, Chief Scientist, Signal Integrity Software

This session discusses solution space analysis, a technique for creating and managing skew, etch topology, cross talk, process variations, and packaging concerns in high-speed design. This methodology breaks the analysis into smaller, easily understood components. Each of these smaller components is then simulated over a simulation space, with consideration of process variations, etch length, network topology, environment, and the effects of inter-symbol interference and cross talk. The use of small analysis components may automate a generation of simulation data. A comprehensive solution re-combines the results from smaller components to yield the expected overall system design operation.

HP-08 Tuesday, January 30 • 2:00 pm – 2:50 pm

Improved Method for Characterizing and Modeling Flex-Circuit-Based Connectors at 2.5 Gbps

Signal Driver Technology – LVDS, PECL, GTLP

Laurie Taira-Griffin, Senior Design Engineer, Research and Development, Packard Hughes Interconnect
Eric Jensen, Senior Project Engineer, Packard Hughes Interconnect
Michael Resso, Product Manager, Agilent Technologies
Dima Smolyansky, Product Marketing Engineer, TDA Systems

Today's high-speed digital designers are faced with the ever-growing challenge of managing signal integrity to maximize data throughput. Advanced switch fabrics that connect various elements of computing systems will need carefully designed hardware for even the simplest of components. High-speed connection systems, using flexible printed circuits with integrated contacts, have novel advantages for many board-to-board architectures. Physical layer optimization of flexible circuit based interconnects is possible when partnered with an effective design.

HP-09A Tuesday, January 30 • 3:00 pm – 3:50 pm

Broadband Measurements in the Differential Mode: Accurate Determination of Dispersive Attenuation

Extending Physical Limits – InfiniBand

Timothy Hochberg, Technical Staff, AtSpeed Technologies
Henri Merkelo, Principal, AtSpeed Technologies
Glen Kimitsuka, Design Engineer, Compaq Computer
John Grebenkemper, Engineering Manager, Tandem Division, Compaq Computer
Dean Vermeersch, Engineer, Tyco Electronics

New methods and tools allow existing instruments to obtain data in the differential mode without the use of baluns. The elimination of baluns preserves the intrinsic frequency range of the instruments and provides means for broadband measurements in the differential mode. Three approaches are discussed and examples of data obtained by using them are presented and compared within bandwidths exceeding 10 GHz. Implications to high-performance design and simulation in the differential mode are also discussed.

HP-09B Tuesday, January 30 • 3:00 pm – 3:50 pm

Rigorous Evaluation of Worst-Case Total Cross-Talk

Extending Physical Limits – Analysis Tools

James Rautio, President, Sonnet Software

Total cross-talk is the sum of all cross-talk waveforms due to input waveforms simultaneously present on all input ports of a circuit. This session evaluates worst-case cross-talk by viewing each cross-talk waveform as a sum of sinusoidal waveforms, or spectrum. The worst case occurs when all sinusoidal waveforms add in phase. The magnitudes of the cross-talk spectral components are determined by means of an electromagnetic analysis. Given knowledge of the worst-case crosstalk, the high-speed digital designer can design the critical portions of a circuit so that a given level of cross-talk can not be exceeded for any possible input excitation.

HP-10 Tuesday, January 30 • 3:00 pm – 3:50 pm

Signal Integrity Measurement and the Requirements Imposed by High-Speed Design

Signal Driver Technology – LVDS, PECL, GTLP

Michael Grabois, Senior Engineer, Fujitsu Network Communications

Transmission line measurement techniques become more demanding as interface speed increases. Testing is necessary when a new interface design concept is validated, when a first prototype arrives, or when interface problems arise. This session gives signal integrity testing methodology fundamentals and provides test examples, checklists, and guidance for high-speed interface design validation, testing and simulation. The progression of testing techniques is explored through interface examples. Specific needs of measurements are described and techniques to incorporate simulation are evaluated.

HP-11 Tuesday, January 30 • 4:00 pm – 4:50 pm

Using Silicon Technology to Extend the Useful Life of Backplane and Card Substrates at 3.125 Gbps

High-Rate Backplane Design

Kevin Roselle, Director, Research and Development, Packaging Architecture and System Design, Chip2Chip
Robert Cutler, High-Speed Interconnection Consultant, RDC Consulting

At 3.125 Gbps and beyond, dielectric loss factors cause frequency dependent losses too large for the link lengths used in FR4 card and backplane substrates. Solutions using alternate lower loss materials have higher cost, lower availability, single sourcing, fabrication and processing issues, and long term reliability questions. The useful life of FR4 substrates can be significantly extended by chip I/O techniques that include programmable driver output equalization, controlled slew rates, adaptive internal termination at both driver and receiver, and very sensitive differential receiver input. The paper presents specifics and compares conventional and new chip I/O approaches using HSPICE simulations and measured data.

HP-12 Tuesday, January 30 • 4:00 pm – 4:50 pm

A 1.6 G-Bit/s/pin Multi-Level Parallel Interconnection

Board and Bus Design – PCI-X, Rambus

Haw-Jyh Liaw, Principal Engineer, Rambus
Gong-Jong Yeh, Member of Technical Staff, Rambus
Greg Pitner, Senior Member of Technical Staff, Rambus

Multi-level signaling, a necessary complication of high-speed parallel interconnection, requires special design and implementation techniques. Anticipating that future bus systems will be bandwidth limited leads to the choice of multilevel signaling. The physical design process begins with a frequency domain bandwidth study. The speakers then create interconnection models from combined simulations and measurements of test structures. Measurements, needed to create models, rely on the essential tools of VNA and TDR and are made on the test structure. The approach is to create a system level SPICE model by integrating individual interconnection models. A prototype is then built and verified using a high-speed oscilloscope. The authors discuss and demonstrate simulation and measurement results.

HP-13A Wednesday, January 31 • 9:00 am – 9:50 am

2.5 Gbps Backplane Design, Simulation, and Measurement

High-Rate Backplane Design

John Goldie, Manager, Applications Engineering, Analog Products Group, National Semiconductor
Gautam Patel, Signal Integrity Engineer, Teradyne Connection Systems
Edward Sayre, President and Chief Executive Officer, North East Systems Associates
Michael Resso, Product Manager, Agilent Technologies

This session is a project of National Semiconductor, NESA, Teradyne, and Agilent Technologies on 2.5Gbps backplane design, simulation and measurement. It focuses on high-speed point-to-point links, using LVDS technology across an FR4 based backplane and logic cards using the VHDM-HSD connector system. Board design, SPICE simulations, and channel performance measurements are discussed. The session concludes with recommendations on achieving maximum throughput for tomorrow's high performance backplanes operating in the 1-3 Gbps range.

HP-13B Wednesday, January 31 • 9:00 am – 9:50 am

Practical Analysis and Simulation of Lossy Transmission Line

Extending Physical Limits – InfiniBand and More

Eric Bogatin, President, Bogatin Enterprises
Michael Resso, Product Manager, Agilent Technologies
Dima Smolyansky, Product Marketing Manager, TDA Systems

At greater than 500 MHz on board and 10Gbps telecommunication products, losses result due to rise time degradation, added delays, bandwidth reduction and most importantly, pattern-dependent noise, often referred to as collapse of the eye diagram. Techniques are presented to fully extract the material properties of any lossy line, using measurements on standard-test structures from off-the-shelf time domain reflectometer (TDR) instruments. The speakers show how end users can evaluate interconnects and establish realistic specs that can be used by any interconnect fabricator using a simulation of transmission line behavior generated from material properties and a lossy line simulator.

HP-14 Wednesday, January 31 • 9:00 am – 9:50 am

Memory Architectures: Analyzing and Probing Rambus, PC133, and Double Data Rate (DDR) SDRAM

Board and Bus Design – PCI-X, Rambus

Gregg Buzard, Marketing Engineer, FuturePlus Systems

Competing memory architectures and the ever-changing direction of the industry can force some designers to wonder which choice will be best. A common test strategy can be used to address all these architectures thus saving a company's time and money when migrating from one to the other. This presentation will discuss these architectures and show designers how state of the art probing technology and acquisition logic will allow them to analyze and verify all three of these architectures. In addition, probing a Rambus channel without using a RIMM socket will be discussed.

HP-15 Wednesday, January 31 • 10:00 am – 10:50 am

Signal Integrity Considerations for 10 Gbit/s Transmission Over Backplane Systems

High-Rate Backplane Design

Gautam Patel, Signal Integrity Engineer, Teradyne Connection Systems
Marc Cartier, Signal Integrity Engineer, Connection Systems Division, Teradyne
Tom Cohen, Mechanical Designer, Connection Systems Division, Teradyne
Jeff Smith, Senior Applications Engineer, AMCC

New-generation devices are handling OC-192 or 10 Gbps data rates. Engineers will want to pass these data rates over printed circuit boards due to cost and application requirements. It will be shown that 10 Gbps transmission is possible over copper in a traditional backplane system. In order to show this, a signal integrity analysis was performed on the individual components of the "system" including board laminates and connectors. The best performing individual components were integrated into a "system" test rig to demonstrate 10 Gbps performance at not only the component level but also at the system level.

HP-16 Wednesday, January 31 • 10:00 am – 10:50 am

Design of Sony PlayStation2 Memory Sub-Systems

Board and Bus Design – PCI-X, Rambus

David Secker, Technical Staff, Rambus
Haw-Jyh Liaw, Principal Engineer, Rambus
Greg Pitner, Senior Member of Technical Staff, Rambus

The speakers use interconnect models, created using Pacific Numerix 2D and 3D field solvers, to design and implement the Sony PlayStation® 2 memory sub-system (32 Mbytes at 3.2 GByte/sec). Only two Dual Direct Rambus RDRAMs memory devices with 800 Mbit/sec/pin are used, saving package pin count, PCB area and system cost. The interconnect models, made with various board design constraints, reveal effects of impedance variation and mutual coupling on system-level voltage and timing margins. The system timing margin is measured by skewing the RDRAM clock phase relative to the memory controller. Simulation and TDR/oscilloscope results will be discussed and demonstrated.

HP-17 Wednesday, January 31 • 2:00 pm – 2:50 pm

Demonstrator for Transmission Via Backplane in CMOS Technology

High-Rate Backplane Design

Helmut Katzier, Director, Engineering, Information and Communication Networks, Siemens AG

This Session presents measurements and simulation results based on a high-speed, backplane-data-transmission demonstrator operating at data rates of 2.5 Gbps and higher. All elements of the interconnection in the transmission path are included: silicon, bond wires, packages, vias and transmission lines in the printed circuit boards, and back plane connectors. Different types of board connector technologies and silicon technologies are presented as well as optimization techniques. Measurements of eye patterns, jitter values and bit error rates are presented and compared depending on connector types, optimization techniques, transmission line lengths, and PCB material.

HP-18 Wednesday, January 31 • 2:00 pm – 2:50 pm

Source Synchronous Bus Design and Timing Analysis for High-Volume Manufacturable System Interconnect

Board and Bus Design – PCI-X, Rambus

Ahmed Omer, Staff Hardware Design Engineer, Intel
Maynard Falconer, Staff Engineer, Intel

As the speeds of VLSI components increase so do the speeds of buses between these components. More and more buses in the today's high-speed digital platforms are embracing source synchronous timing methods. Thus, the understanding of source synchronous design and timing analysis becomes crucial for today's designs. In this session, fundamentals of source synchronous timing analysis and bus design techniques for high volume manufacturable system interconnects will be discussed. Terminology and equations used in these analyses will be explained. Also, the system bus of the Pentium® 4 processor will be used as an implementation example.

HP-19 Wednesday, January 31 • 3:00 pm – 3:50 pm

A Comprehensive Power Bus Design Procedure for Digital Systems Switching 100 Amps./nsec.

High-Rate Backplane Design

JP Miller, Principal Member of Technical Staff, Compaq Computer
Joe Stoddard, Senior Member of Technical Staff, Compaq Computer
Mitch Wright, Member of Technical Staff, Compaq Computer

As operating speeds increase, it becomes necessary to understand a power bus as an integrated subsystem with all of its parts functioning. This session presents a design procedure that includes the following: load characteristics, capacitor characteristics, board characteristics and power supply response time. Thin dielectric spacing between power and ground appears to be the most practical way to stabilize power supply voltage during the first 500 psec of a current step. This session explores the future role of thin dielectrics. Many sessions have presented parts of the above, but this comprehensive session includes all the above in systematic step-by-step easy to follow procedure.

HP-20 Wednesday, January 31 • 3:00 pm – 3:50 pm

Layout Constraints for Signal Integrity on Digital Boards With Sub-Nanosecond Driver Edge Rates

Board and Bus Designs – PCI-X, Rambus

Lynne Green, Technical Marketing Engineer, Innoveda

Falling driver edge rates have made placement and routing tradeoffs and simulation necessary and a critical step in finding signal integrity problems before shipment. Faults caused by signal integrity problems are difficult to troubleshoot on prototypes, being sensitive to switching of neighboring nets, IC process corner (fast/typical/slow), temperature, and Vcc voltage, as well as variations in manufactured boards. Simulation avoids recalls due to undetected signal integrity and mortality problems. This session examines interactions between system design and layout, including termination. This session also presents guidelines and tips for system designers to ensure signal integrity requirements are met.

The International Engineering Consortium (IEC) is a nonprofit organization dedicated to catalyzing positive change in the information industry and its university communities. The IEC provides high-quality educational opportunities for industry professionals, academics, and students. In conjunction with the industry, the IEC develops free on-line Web-based tutorials. The IEC conducts industry-university programs that have substantial impact on curricula. It also conducts research and develops conferences, publications, and technological exhibits addressing major opportunities and challenges of the information age. More than 70 leading, high-technology universities are currently affiliated with the Consortium. The industry is represented through substantial corporate support and the involvement of many thousands of executives, managers, and professionals.

DesignCon sessions provide informative, up-to-date solutions.

WB-01 Tuesday, January 30 • 9:00 am – 9:50 am

Performance Evaluation of Gbps Backplane Serial Links

Network and Communication Infrastructure Pathways

Bilal Ahmad, Hardware Engineer, Cisco Systems
Jeff Cain, Technical Leader, Cisco Systems

This session evaluates the performance of the backplane and daughter card system at Gbps speeds. It quantitatively analyzes effects of impedance mismatch at connectors, dielectric and skin effect losses, pre- and post-emphasis filtering, cross-talk, and jitter effects. Results are presented in the form of eye diagrams and probability of error vs. signal-to-noise ratio curves. The speakers discuss measurement and simulation tools and techniques for domains of time and frequency. They compare measurement and simulation results and discuss techniques used to "tune" connector models.

WB-02 Tuesday, January 30 • 9:00 am – 9:50 am

Top Ten Requirements for Service Discovery

Bluetooth/3G/Handheld Application Design

Robert Pascoe, President, Salutation Consortium

The personal area network, radiating from the mobile devices we carry, will reach network nodes located in shopping malls, hotels, and airports, and connect us to data bases and information sources as we wander by. Dynamic networking paradigms are enabled by Bluetooth™, power line transfer, and Home RF™. Devices, applications, and services may enter a network or move from one location to another with ease. Each network resource must advertise services provided, locate services needed, and build a relationship between devices. A technology is needed to find services and bind them. This session will review design requirements of service discovery technologies and review current front-runners.

WB-03 Tuesday, January 30 • 10:00 am – 10:50 am

Non-Linear Full-Wave Time Domain Solutions Using FDTD_SPICE for High-Speed Digital and RF

Network and Communication Infrastructure Pathways

Raj Raghuram, Director, Research and Development, Applied Simulation Technology
Neven Orhanovic, Signal Integrity Developer, Applied Simulation Technology
Norio Matsui, EMI/EMC Leader, Applied Simulation Technology

Quasi-static and TEM solutions are no longer valid for high-speed digital designs in the GHz range. Although SPICE provides visualization of time domain waveforms, only frequency domain electromagnetic solvers account for full wave effects. The speakers use a simulator that combines FDTD and SPICE as a solution to this problem. They simulate nonlinear circuit elements in SPICE and structural elements in FDTD. The simulators are tightly integrated, communicating at each time step. They give examples of difficult problems such as: meanders, ground bounce, and decoupling capacitor placement in a PCB and dispersion in microstrips.

WB-04 Tuesday, January 30 • 10:00 am – 10:50 am

Dynamic Spectral Sharing in Mobile-Mobile Networks

Bluetooth/3G/Handheld Application Design

James Solinsky, Vice President and Chief Technology Officer, Nomikon

Mobile-Mobile networks do not require a fixed cell in their vicinity; they dynamically form and separate using inter-unit protocols. This work addresses dynamic detection of and adjustment to a frequency spectrum in use by others so the network works in a locally non-interfering manner. As a result of the high dynamic and variable RF connectivity, the routing protocol is embedded in hardware and reacts based on a prediction of the local spectral use by others. The speaker describes simulation and experimental results demonstrating the RF predictor and dynamic adjustment so the mobile-mobile network can operate in a shared frequency spectrum within the spectral environment of other communications.

WB-05 Tuesday, January 30 • 11:00 am – 11:50 am

Overcoming Packaging Limitations in High-Speed Wireless IC Designs

Network and Communication Infrastructure Pathways

Chris Mueth, Product Marketing Manager, Agilent Technologies

Wireless IC or component designs may be limited by the frequency response or signal integrity due to physical, distributive and electromagnetic packaging effects. This session explores high frequency packaging value propositions and design flow, functional requirements, and technical limitations. The speaker proposes a solution for wireless package design for a wide variety of RF and microwave applications. He introduces a modeling approach, design methodology and use of specific electronic design analysis (EDA) tools to simulate package performance and facilitate the design procedure. The design methodology and modeling process is an improvement to the overall design flow, and leverages these technological benefits into wireless markets.

WB-06 Tuesday, January 30 • 11:00 am – 11:50 am

Transactional Interactive Messaging

Bluetooth/3G/Handheld Application Design

Kayvan Alikhani, Chief Technology Officer, MagNetPoint
Ron Hooper, Chief Executive Officer, MagNetPoint

This session discusses a new method of rule-based conversion/delivery of messages to the user independent of device or location. The method allows service providers to use simple, out-sourced interfaces and hosts to interact with mobile users, keeping independent of the "device-of-the-day" syndrome. It also allows users to interact and transact using messages. The session discusses mechanisms for creating interactive and device independent intelligence, working with messaging protocols for wired, wireless, SMS, WAP, voice-mail, e-mail, fax-mail, and two-way paging. A live example is presented of a vertical (financial) service provider application. The session reviews HP e-speak technology and its potential use in standards based transactional interactive messaging.

WB-07 Tuesday, January 30 • 2:00 pm – 2:50 pm

Probing and Analyzing Communication System Embedded PCI Designs

Network and Communication Infrastructure Pathways

Gregg Buzard, Marketing Engineer, FuturePlus

PCI has grown to enormous proportions and is now used in many diverse applications. This session will focus on the needs of the embedded PCI designer. Compact PCI, PMC and embedded desktop designers will learn newly developed techniques for post processing acquired PCI traffic to find compliance violations, timing errors and measure to performance metrics. Validation techniques for PCI systems with no standard connector or no connector at all will also be discussed.

WB-08 Tuesday, January 30 • 2:00 pm – 2:50 pm

Bluetooth Compliance Validation at the RTL Design Stage

Bluetooth/3G/Handheld Application Design

John Gallagher, Director, Certify Marketing, Synplicity

ASIC-based Bluetooth devices implement new forms of functional verification. Currently verification waits on a full ASIC fabrication run for a prototype. Then software integration, taking over 6 to 9 months after correct RTL code is generated, is necessary to test system-level functionality and compliance. This session describes design automation software and programmable logic devices that enable Bluetooth compliance validation at the RTL stage. With an RTL-level hardware prototype, Bluetooth system designers can perform hardware/software co-verification and system integration when HDL code is verified. The speaker discusses design flow, reduction in system-integration time and Bluetooth debugging and interfacing.

WB-09 Tuesday, January 30 • 3:00 pm – 3:50 pm

Design Analyses for Broadband, Non-Interfering, Multiple-Access RF Communications Links from User Terminals to Comsat Hub in Two-Way VSAT Networks

Network and Communication Infrastructure Pathways

Lester Turner, Vice President and Chief Technical Officer, eVox

Dedicated WANs, consisting of RF linked hub facility, Comsat, and many very small aperture terminals (VSATs), are becoming popular for broadband connectivity to the Internet. These WANs implement the direct video broadcast (DBV) standard to provide 45 Mbps broadband channels for two-way transmission. Presently, return communications links from VSATs to the hub via the Comsat and from the hub to the Internet operate at maximum rate of 64 Kbps, which is unacceptable for two-way, broadband-Internet access. This session examines applicable capabilities, presents pertinent analyses, configures an implementation and discusses test results of the StealthWare RF communications technology.

WB-10 Tuesday, January 30 • 3:00 pm–3:50 pm

New Processor Advances Make SoftRadio a Reality

Advanced Embedded Communication Techniques

Pete Foley, Vice President, Systems Engineering, nBand Communications

The "Holy Grail" of broadband wireless has been a software-defined radio that implements programmable baseband and MAC layers. This session presents the programming model and hardware architecture considerations that led to a programmable, broadband wireless communications processor. As an illustration of this approach, the development time and effort of implementing a wireless LAN using this processor will be compared with a more traditional fixed-function approach. This session will also present the cost and speed tradeoffs between fixed function and programmable implementations. The lessons learned point to possible extensions that can be made to future broadband wireless systems using this new paradigm.

WB-11 Wednesday, January 31 • 9:00 am – 9:50 am

Open Switching Architecture

Flexible/Intelligent Network Design

Paul Lisenberg, Director, Strategic Marketing, Zettacom

This presentation briefly analyzes why outsourcing key components is becoming more commonplace in the high-end networking industry, and presents the vision and benefits of universal switching architecture(s) that enables outsourcing. It presents emerging interfaces that allow such architectures and addresses time-to-market and convergence benefits. The speaker presents the functional modules that comprise an open switching architecture and the requirements on different sub-systems.

WB-12 Wednesday, January 31 • 9:00 am – 9:50 am

Computers Without Computing

Advanced Embedded Communication Techniques

Will Golby, Vice President, Celoxica

Celoxica will examine a new approach to rapid design, citing customer case studies and benchmarks that show how application specialists can increase their productivity and take concepts directly to silicon. The session will also illustrate, with live demonstrations, how Internet reconfigurable platforms can support a myriad of applications such as VoIP and MP3.

WB-13 Wednesday, January 31 • 10:00 am – 10:50 am

Fiber-Optical Signal Integrity from Deterministic, Random, and Periodic Components of a Jitter

Signal and Associated Frequency Domain Spectrum

Mike Li, Director and Senior Scientist, Research and Development, Wavecrest
Jan Wilstrup, Corporate Consultant, Wavecrest

The speakers use case studies, based on quantitative measure for deterministic, random, periodic components of a jitter signal, and its associated frequency domain spectrum, to provide practical signal integrity/jitter solutions. They use both case studies and bench measurements to: verify design performance, debug and identify a signal integrity/jitter related failure, assure test standards compliance, and shorten cycle time from design to production. The session demonstrates how to measure and analyze key parameters for a high-speed digital, analog, optical system, such as power, jitter and bit error rate, using a single "smart" measurement/analysis system that crosses electrical-optical worlds, with applications in data communication, PLL/clock, and fiber optical systems.

WB-14 Wednesday, January 31 • 10:00 am – 10:50 am

Vector-Based Graphical Modeling of Physical Layer (PHY) Functions in High-Performance Communications

Advanced Embedded Communication Techniques

Eyran Lida, Manager, Software and CAD Group, MystiCom

The increasing bandwidth requirements of high-performance communications functions, such as those used in gigabit and multi-gigabit Ethernet physical layers, require the integration of large, complex parallel data paths on a single chip. The modeling of these functions can be complicated and time consuming. This process can be simplified by using a vectors-based graphical modeling approach to deliver flexible, bit-exact models. Using an adaptive pipeline filter at the physical layer as an example, this presentation will compare and contrast various modeling approaches, illustrating how vectors-based graphical modeling can be used to reduce the design complexity of parallel data paths in high-performance communications ICs.

WB-15 Wednesday, January 31 • 2:00 pm – 2:50 pm

Multiplexing LAN Architectures for 3D Wafer Bonding Technologies

Flexible/Intelligent Network Design

Ronald Gutmann, Professor, Center for Integrated Electronics and Electronics Manufacturing, Rensselaer Polytechnic Institute
J.Q. Lu, Rensselaer Polytechnic Institute
J.F. McDonald, Rensselaer Polytechnic Institute
R.P. Kraft, Rensselaer Polytechnic Institute

Three-dimensional (3D) ICs offer the potential of reducing fabrication and performance limitations of future generations of planar ICs. The speakers discuss alternative 3D integration technologies and the advantages of wafer bonding, then lay out design implications for both intellectual property (IP) core-based designs and high-speed processor design. They present 3D integration with multiplexing local area network (LAN) architectures compatible with 3D wafer bonding and give a packaging technology compatible with RF/microwave, millimeter wave and optical wireless interconnects.

WB-16 Wednesday, January 31 • 2:00 pm – 2:50 pm

IP-Centric Architecture for Optical-Network Architecture

Fiber-Optical Performance Optimization

Krishna Bala, Chief Technical Officer, Tellium
Bala Rajagopalan, Tellium

This session presents a control architecture for optical mesh networks based on a new generation of high capacity, intelligent optical switches. The speaker shows how these network elements provide superior bandwidth, on-demand service provisioning, and seamless integration with client equipment, such as IP routers. The network elements maintain optical-level standards for high reliability and restoration capabilities. The architecture utilizes protocols developed for the control of IP networks, namely addressing, routing and signaling.

WB-17 Wednesday, January 31 • 3:00 pm – 3:50 pm

SOIS: Smart Optical Interconnection System

Flexible/Intelligent Network Design

Karl Gerdom, Project Manager, Optical Interconnection, Harting
Ulrich Wallenhorst, Advanced Solutions, Harting

The speakers show how the smart optical interconnect solution (SOIS) solves design problems of next generation telecommunication cross connects, data buses, and board-to-board transmission at 10Gbps over individual optical fibers. SOIS integrates a robust electrical connector, an integrated transceiver with metallized plastic chip aligner/carrier, and a star-coupler used for signal distribution. The electrical connector provides 10 Gbps transfer over microstrip lines and meets the compactPCI standard. The aligner/carrier is the copper/optical interface, interconnecting high-speed board signals to photodiodes. The waveguide star-coupler includes a polymer optical waveguide structure and a groove structure for passive fiber alignment.

WB-18 Wednesday, January 31 • 3:00 pm – 3:50 pm

Laser Micro-Machining for Optical Interconnection

Fiber-Optical Performance Optimization

Brian Patterson, Global Business Manager, Fiber-Optic Division, Tyco Electronics

A new patented, laser, micro-machining technology that enables a whole new generation of fiber optic inter-connection is presented. The session compares its capability with the existing one in terms of physical geometry, design versatility, optical and physical performance and probable application. The speaker reviews proposed applications and existing product enhancements in detail. In particular, the coverage includes interconnected performance of wavelength multiplexing, photonic switching and a variety of other fiber dense, performance sensitive devices. Finally, the session introduces concepts for new interconnection form factors for dense backplane packaging.

WB-19 Wednesday, January 31 • 4:00 pm – 4:50 pm

An Open Platform for the Rapid Prototype and Deployment of Hardware-Based Networking Modules

Flexible/Intelligent Network Design

John Lockwood, Research Assistant Professor, Computer Science, Washington University, Saint Louis

A new device, the field programmable port extender (FPX), augments the Washington University gigabit switch with reprogrammable logic. FPX enables applications such as IP routing, packet classification, and distributed queuing, to be rapidly prototyped in hardware and tested within a functional, high-speed router. Through the use of network-reprogrammable FPGAs, FPX enables routers to have both the flexibility to be dynamically reconfigured and the capability to process packets at the full rate of an Internet backbone link. Though a collaborative project with several universities, FPX is being used as a platform to prototype and implement several hardware-based applications.

WB-20 Wednesday, January 31 • 4:00 pm – 4:50 pm

When Less Is More: Lowering Insertion Loss in High-Density Optical Connectors Is a Key Enabling Technology in Advanced Optical Systems Design

Fiber-Optical Performance Organization

Beth Murphy, Product Manager, Fiber-Optic Division, Tyco Electronics

This session explores why high-density, low-insertion-loss interconnects are critical in the design of many advanced optical systems. The speaker discusses the technology used to achieve low insertion loss in high-fiber count interconnects. She will discuss various systems design architectures, highlighting easily separable backplane optics. Many of today's systems have very strict loss budgets, and this session focuses on design alternatives for loss-sensitive systems, including typical system architectures.

DesignCon 2001 Planning Committee

DesignCon 2001 is developed under the direction of the Conference Planning Committee, which is comprised of the design engineering industry's leading technologists, strategists, editors, and consultants. Led by program development managers Earl Reinkensmeyer, President of Summit Innovation, a leading industry consulting firm, and Carl Murphy, President of Accord Solutions, the Planning Committee provides guidance to the DesignCon content-development team, helping to identify the industry's leading technological advances and most compelling issues.

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The Westin Santa Clara Hotel

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The official headquarters for DesignCon 2001 is the Westin Hotel Santa Clara. With 500 luxurious guest rooms–each equipped with small touches that will give you a taste of home, including an in-room coffee maker and complimentary morning newspaper–the Westin Santa Clara is one of the finest convention hotels in the country. Served by three major airports (San Jose, 10 minutes away; San Francisco, 30 minutes away; and Oakland, 35 minutes away), the Westin Santa Clara is conveniently located in the heart of Silicon Valley. For the sports- and fitness-minded, it offers on-site exercise facilities, is adjacent to the Santa Clara Golf and Tennis Club, and is near a jogging trail. For those interested in more pedestrian pursuits, the Westin Santa Clara's Lobby Lounge features fine California wines and live piano music, while the restaurant Tresca offers a menu that reflects the diversity found throughout Northern California, with Mediterranean undercurrents. There is truly something for everyone, from a seared Ahi tuna salad and fresh seafood to homemade pizzas and fine steaks. For combining business with pleasure, few convention hotels match the combination of services and amenities offered by the Westin Hotel Santa Clara.

Santa Clara Convention Center

Located just south of San Francisco in the center of Silicon Valley, this state-of-the-art meeting, trade, and convention complex has taken its cue from the dynamic business that now surrounds it. In addition to being one of the most modern, well-equipped facilities in the state, the Santa Clara Convention Center is the only complete resort-style convention center in the Bay Area, featuring an 18-hole championship golf course and complete tennis facility.

The Westin Santa Clara Hotel and the Santa Clara Convention Center

The DesignCon Experience

DesignCon is the only design-engineering event where you can learn the industry's latest techniques and theories through comprehensive conference sessions and then immediately see them in application at the hands-on demonstrations and exhibits that are linked to the conferences. At DesignCon, you will find solutions to the most demanding design challenges and then discover the products that will help put your knowledge to use immediately. You'll also have plenty of opportunity to interact with your peers and colleagues in the design engineering community at several corporate-sponsored luncheons and receptions held each day.

Each year, thousands attend DesignCon to stay current on leading techniques.

United Airlines

Ten percent (10%) discount off unrestricted coach fares or a 5% discount off lowest applicable fares, including first class. To make your reservations today, call United Airlines at 1-800-521-4041 Monday–Sunday 7:00 am–midnight (EST). Please identify yourself as a DesignCon participant and refer to file code number 544WU.

Special Needs

Should you have special needs or requirements, please call the DesignCon registration team at +1-888-486-8736. One of our representatives will be happy to assist you with the proper arrangements.

Cancellation and Refund Policy

Advance registration may be cancelled and refund made only if WRITTEN notice is postmarked prior to midnight, December 29, 2000. Participants who register after midnight, December 29, 2000 will be responsible for full registration payment. No full or partial cancellations or refunds will be granted after midnight, January 2, 2001. Note: Badges and Tickets to DesignCon 2000 are issued to individual registrants. Each attendee must be registered for the event attending. Badges and/or Tickets may not be transferred from one individual to another. Registration may be substituted in its entirety only if WRITTEN notification is made prior to January 22, 2001.

DesignCon 2001 Registration Form

January 29 – February 1, 2001 • Exhibits: January 30 – 31, 2001 • Santa Clara Convention Center

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Session Selections

Please indicate your session selections by referencing session codes found on pages 21–41 of this catalog.

Monday, January 29 _____ _____

Tuesday, January 30 _____ _____ _____ _____ _____ _____

Wednesday, January 31 _____ _____ _____ _____ _____ _____

Thursday, February 1 _____

Registration Fees

Register for conferences packages by January 5 and receive $100.00 off any conference!

All packages include access to keynote and plenary sessions, plus attend exhibits and exhibit-floor receptions. All Sessions are available for selection on-line!.

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Includes one half day of TecForums.

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FREE if you register before January 5!

Total Registration Fee **$_____**

DesignCon strictly adheres to the cancellation and refund policy detailed on page 42.

Attendance Dates

Check all that apply:

☐ Monday, January 29
☐ Tuesday, January 30
☐ Wednesday, January 31
☐ Thursday, February 1

Conferences

Indicate primary conference:

☐ System-On-Chip
☐ High-Performance System
☐ Wireless and Optical Broadband
☐ IP World Forum

Primary Products or Services Your Company Produces (check all that apply)

☐ C1 Computer Systems and Peripherals
☐ C2 Controls, Test, and Medical Equipment
☐ C3 Avionics, Marine, Government, and Military Electronics
☐ C4 Communication Systems
☐ C5 Automotive, Consumer Electronics, and Appliances
☐ C6 Components
☐ C7 Other_____

Type of Design in Which You Are Involved (check one selection only)

☐ B1 Analog
☐ B2 Software
☐ B3 ASIC
☐ B4 Communications
☐ B5 Digital
☐ B6 Systems
☐ B7 FPGAs
☐ B8 Test & Evaluation
☐ B9 Mixed Signal ICs
☐ B10 PCB or MCM
☐ B11 PLDs
☐ B12 Other_____

Job Function (check one selection only)

☐ A1 General and Corporate Management
☐ A2 Design and Development Engineering
☐ A3 CAD Developer
☐ A4 Manufacturing and Production
☐ A5 Sales and Marketing
☐ A6 Engineering Management
☐ A7 Engineering Service
☐ A8 Research and Development
☐ A9 Purchasing
☐ A10 Other_____

Products and Services You Purchase, Specify, or Recommend (check all that apply)

☐ D1 Standard ICs
☐ D2 Digital ICs
☐ D3 Memory ICs
☐ D4 Analog ICs
☐ D5 ASICs
☐ D6 Design Automation Tools
☐ D7 System Boards
☐ D8 Semiconductors
☐ D9 EDA/CAE Tools
☐ D10 Computers/Software
☐ D11 Mixed Signal ICs
☐ D12 Mixed Signal Systems
☐ D13 FPGAs
☐ D14 PLDs
☐ D15 Computer Peripherals
☐ D16 Components
☐ D17 Interconnection Devices
☐ D18 Packaging
☐ D19 Power Sources
☐ D20 Services
☐ D21 Other_____

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January 29 – February 1, 2001
Exhibits: January 30–31, 2001
Santa Clara Convention Center
Santa Clara, California

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The high-quality programming of DesignCon attracts participants from more than 1,000 leading organizations in EDA, semiconductor, electronics, and information industries to attend seminars, present papers and sessions, and view and demonstrate technologies. Experience the DesignCon difference—design solutions presented by top engineers in a practical, straightforward fashion. The following list includes the leading organizations that participated in DesignCon 2000.

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