EMBEDDED SYSTEMS WEEK

2012

October 7 - 12, 2012

Technical Programme

Tampere

Tampere Hall, Finland

TABLE OF CONTENTS

WELCOME MESSAGE 2

ORGANIZING COMMITTEES 4

PROGRAMME OVERVIEW 7

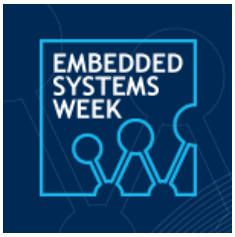
FLOOR MAPS 7

DAILY PROGRAMME 12

SOCIAL PROGRAMME 53

GENERAL INFORMATION 54

TAMPERE SIGHTSEEING 58



Embedded Systems Week 2012

WELCOME MESSAGE

On behalf of the Organizing Committee and the committees of our participating conferences - CASES, CODES+ISSS, and EMSOFT - we would like to welcome you to Embedded Systems Week - ESWEEK 2012 - in Tampere, Finland. 2012 marks the 8th edition of ESWEEK. Earlier meetings were held in Jersey City, Seoul, Salzburg, Atlanta, Grenoble, Scottsdale and Taipei. This meeting has grown from two conferences and a handful of workshops to three conferences and ten workshops and symposia. ESWEEK is now widely recognised as the premier technical event in embedded computing.

The combined programme of the three conferences will offer three plenary keynotes, an industry day, and over 100 technical paper presentations. ESWEEK will also offer a number of half-day tutorials that cover hot topics of general interest to the embedded systems community. Additionally, this year, the International Symposium on System-on-Chip (SoC) will be co-located with ESWEEK. First of all, special thanks go to the technical programme chairs of the three conferences: Vincent Mooney, Rodric Rabbah, Franco Fummi, Naehyuck Chang, Florence Maraninchi, and John Regehr. This year, Embedded Systems Week includes ten workshops featuring outstanding contributions on specific topics. We especially wish to thank the workshop organisers: Aviral Shrivastava, Wolfgang Ecker, Wolfgang Mueller, Shahrokh Daijavad, Sumedh Sathaye, Seraphin Calo, Dimitrios Serpanos, Jian-Jia Chen, Maurizio Palesi, Nikil Dutt, Jason Xue, Jeff Jackson, Peter Marwedel, Kenneth Ricks, Fabiano Hessel, Jérôme Hugues, Frédéric Rousseau, Rolf Ernst and Alberto Sangiovanni-Vincentelli.

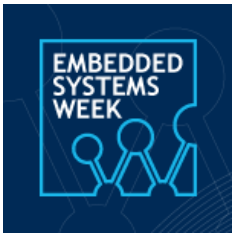
A complex event such as ESWEEK is a team effort that requires a dedicated group of volunteers to manage the success of the conference's growth in scale and offerings. We wish to thank every member of the organizing committee for their dedicated efforts in making the event a success. In particular, special thanks go to the following people for managing critical aspects of the conference organization: Jari Nurmi and Irmeli Lehto for local organization; David Atienza for finances; Suzanne Lesecq for publications; Francescantonio Della Rosa and Aviral Shrivastava for the conference website; Edward Chu and Frédéric Pétrot for electronic media and the paper submission system; Sungjoo Yoo, Tapani Ahonen and Yuan Xie for industry liaison; Gabriela Nicolescu, Jian-Jia Chen and Roberto Airoldi for workshops; Saddek Bensalem for tutorials; Henri-Pierre Charles, Xiaobo Sharon Hu and Hamaguchi Kiyoharu for publicity; Enrico Macii for coordinating the best paper award selections; Rolf Ernst for panels and special sessions; Hiroto Yasuura and Hiroyuki Tomiyama for handling the Asia liaison; Luigi Carro and Fabiano Hessel for handling Latin America liaison; Rajesh Gupta, Alex Orailoglu, Marilyn Wolf, Naehyuck Chang and Donald Thomas for professional society liaisons.

We also thank the Steering Committee members and the Technical Programme Committee members of each conference and workshop for selecting papers of the highest quality. Finally, we thank our sponsoring societies: ACM (SIGBED, SIGDA, SIGMICRO), IEEE (CAS, Computer, CEDA); and the cooperation with IFIP.

Tampere – the SoC city – is situated in the heart of beautiful Finnish Lakeland. The banks of the Tammerkoski rapids still feature old traditional industrial buildings which have now been converted to house pleasant restaurants, pubs or high-tech companies. Tampere is also a city of theatres, arts, sciences, sport and modern industrial culture. We therefore invite you to attend ESWEEK 2012 to learn about the latest in embedded system technologies, and also discover the beauty, culture and technological miracles of Finland.

Ahmed Jerraya
ESWeek 2012 General Chair
CEA, France

Luca Carloni
ESWeek 2012 General co-Chair
Columbia University, USA



Embedded Systems Week 2012

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IEEE CS Liaison:

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IFIP Liaison:

- Marilyn Wolf, Georgia Tech, USA

ACM SIGDA Liaison:

- Naehyuck Chang, Seoul National University, Korea

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- Donald Thomas, Carnegie Mellon University, USA

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EMSOFT:

- Insup Lee, University of Pennsylvania, USA
- Lothar Thiele, ETH Zurich, Switzerland

PROGRAMME OVERVIEW

Oct. 7 (SUN)	Pieni Sali	Sopraano	Sonaatti 1	Studio	Sonaatti 2	Opus 4	Aaria
0800-0930		EMSOFT Tutorial 1	CASES Tutorial 1	CODES+ISSS Tutorial 1	CASA	MeCoES	EON
0930-1000		**Coffee Break (Room Rondo)**					
1000-1200		EMSOFT Tutorial 1	CASES Tutorial 1	CODES+ISSS Tutorial 1	CASA	MeCoES	EON
1200-1300		**Lunch (Tampere Hall Restaurant)**					
1300-1500		EMSOFT Tutorial 2	CASES Tutorial 2	CODES+ISSS Tutorial 2	CASA	MeCoES	EON
1500-1530		**Coffee Break (Room Rondo)**					
1530-1730		EMSOFT Tutorial 2	CASES Tutorial 2	CODES+ISSS Tutorial 2	CASA	MeCoES	EON
1800-1930		**Welcome Reception (Museum Center Vapriikki)**					

Oct. 8 (MON)	Pieni Sali	Sopraano	Sonaatti 1	Studio	Sonaatti 2	Opus 4	Aaria
0800-0830	Opening Remarks						
0830-0930	Keynote by Hannu Kauppinen, Nokia						
0930-1000	**Coffee Break (Room Rondo)**						
1000-1200	EMSOFT Session 1A	CASES Session 1	EMSOFT Session 1B	CODES+ISSS Session 1A	CODES+ISSS Session 1B		
1200-1300	**Lunch (Tampere Hall Restaurant)**						
1300-1500	EMSOFT Session 2A	CASES Session 2	EMSOFT Session 2B	CODES+ISSS Session 2A	CODES+ISSS Session 2B		
1500-1530	**Coffee Break (Room Rondo)**						
1530-1730		CASES Session 3	EMSOFT Session 3	CODES+ISSS Session 3A	CODES+ISSS Session 3B		
1830-2030	**ESWeek Organizing Committee and TPC Meeting (Restaurant Finlaysonin Palatsi)**						

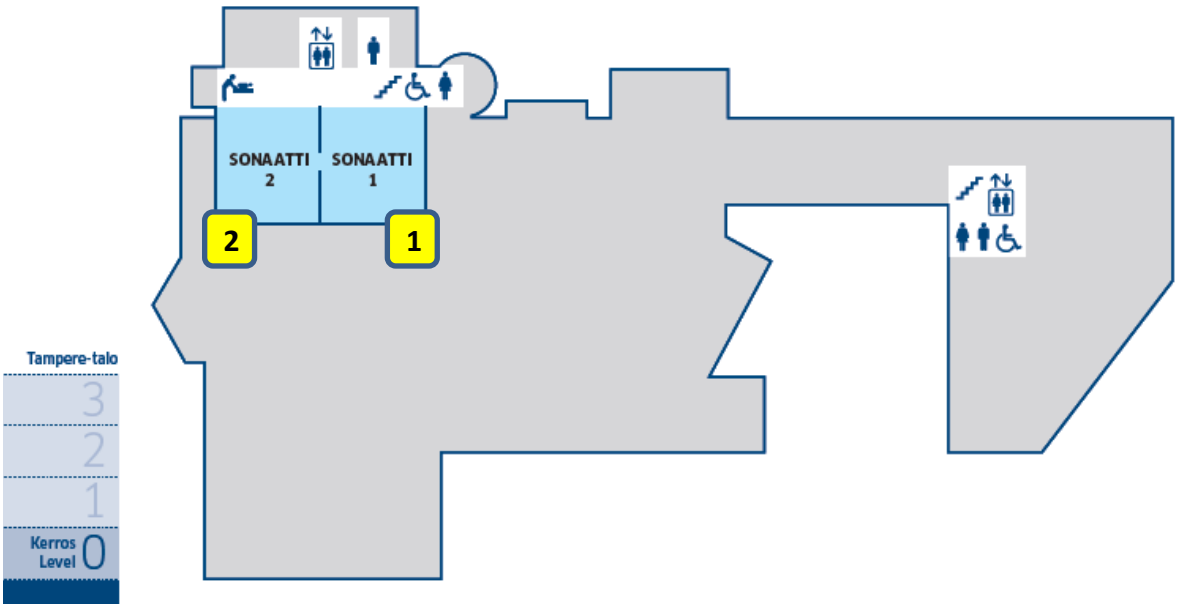
Oct. 9 (TUE)	Pieni Sali	Sopraano	Sonaatti 1	Studio	Sonaatti 2	Opus 4	Aaria
0830-0930	Keynote by Satnam Singh, Google						
0930-1000	**Coffee Break (Room Rondo)**						
1000-1200		CASES Session 4	EMSOFT Session 4	CODES+ISSS Session 4A	CODES+ISSS Session 4B		
1200-1300	**Lunch (Tampere Hall Restaurant)**						
1300-1500	Industrial Session 1	CASES Session 5	EMSOFT Session 5	CODES+ISSS Session 5A	CODES+ISSS Session 5B		
1500-1530	**Coffee Break (Room Rondo)**						
1530-1730	CODES+ISSS Session 6A	CASES Session 6	EMSOFT Session 6	CODES+ISSS Session 6B	CODES+ISSS Session 6C		
1830-2030	**Banquet Gala (Restaurant Scandic Rosendahl)**						

Oct. 10 (WED)	Pieni Sali	Sopraano	Sonaatti 1	Studio	Sonaatti 2	Opus 4	Aaria
0830-0930	Keynote by Jong Choi, Samsung						
0930-1000	**Coffee Break (Room Rondo)**						
1000-1200	Industrial Session 2	CASES+CODES+ISSS Session 7	EMSOFT Session 7	CODES+ISSS Session 7A	CODES+ISSS Session 7B		
1200-1300	**Lunch (Tampere Hall Restaurant)**						
1300-1500	Industrial Session 3	CASES+CODES+ISSS Session 8	EMSOFT Session 8	CODES+ISSS Session 8A	CODES+ISSS Session 8B		
1500-1530	**Coffee Break (Room Rondo)**						
1530-1730	Industrial Panel						
1730-1745	Best paper award Announcements Closing remarks						

Oct. 11 (THU)	Pieni Sali	Sopraano	Sonaatti 1	Studio	Sonaatti 2	Opus 4	Aaria
0800-0900		RSP	ESTIMedia		MeAOW	WESE	WESS
0900-0930		**Coffee Break (Room Rondo)**					
0930-1130		RSP	ESTIMedia		MeAOW	WESE	WESS
1130-1300		**Lunch (Tampere Hall Restaurant)**					
1300-1500		RSP	ESTIMedia		MeAOW	WESE	WESS
1500-1530		**Coffee Break (Room Rondo)**					
1530-1730		RSP	ESTIMedia		MeAOW	WESE	WESS

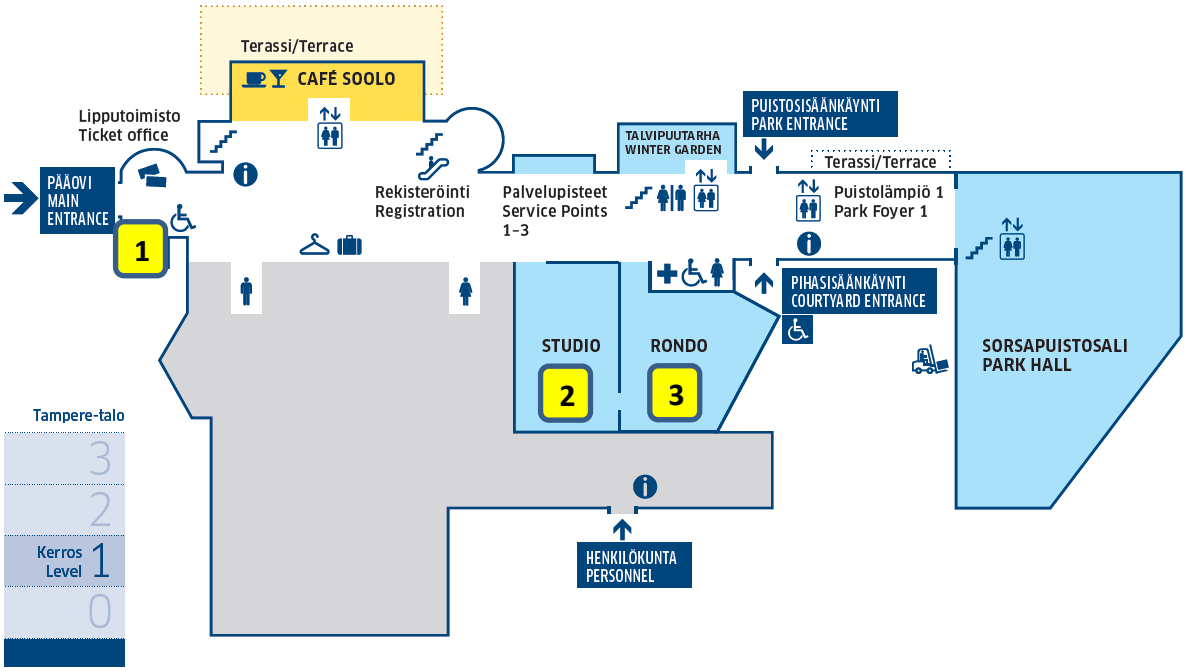
Oct. 12 (FRI)	Pieni Sali	Sopraano	Sonaatti 1	Studio	Sonaatti 2	Opus 4	Aaria
0830-0930		RSP	ESTIMedia				
0930-1000		**Coffee Break (Room Rondo)**					
1000-1200		RSP	ESTIMedia				

Floor Maps



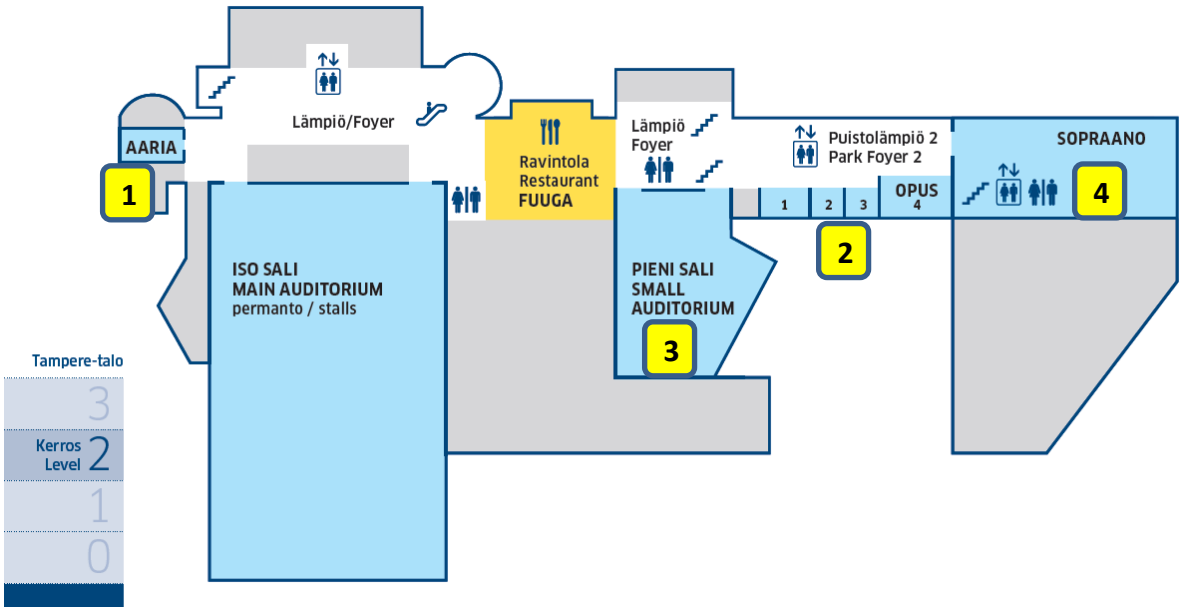
Ground floor

1	**Sonaatti 1**	Sun	CASES Tutorial
		Mon – Wed	EMSOFT
		Thu – Fri	ESTIMedia 2012
2	**Sonaatti 2**	Sun	CASA 2012
		Mon – Wed	CODES+ISSS
		Thu	MeAOW 2012



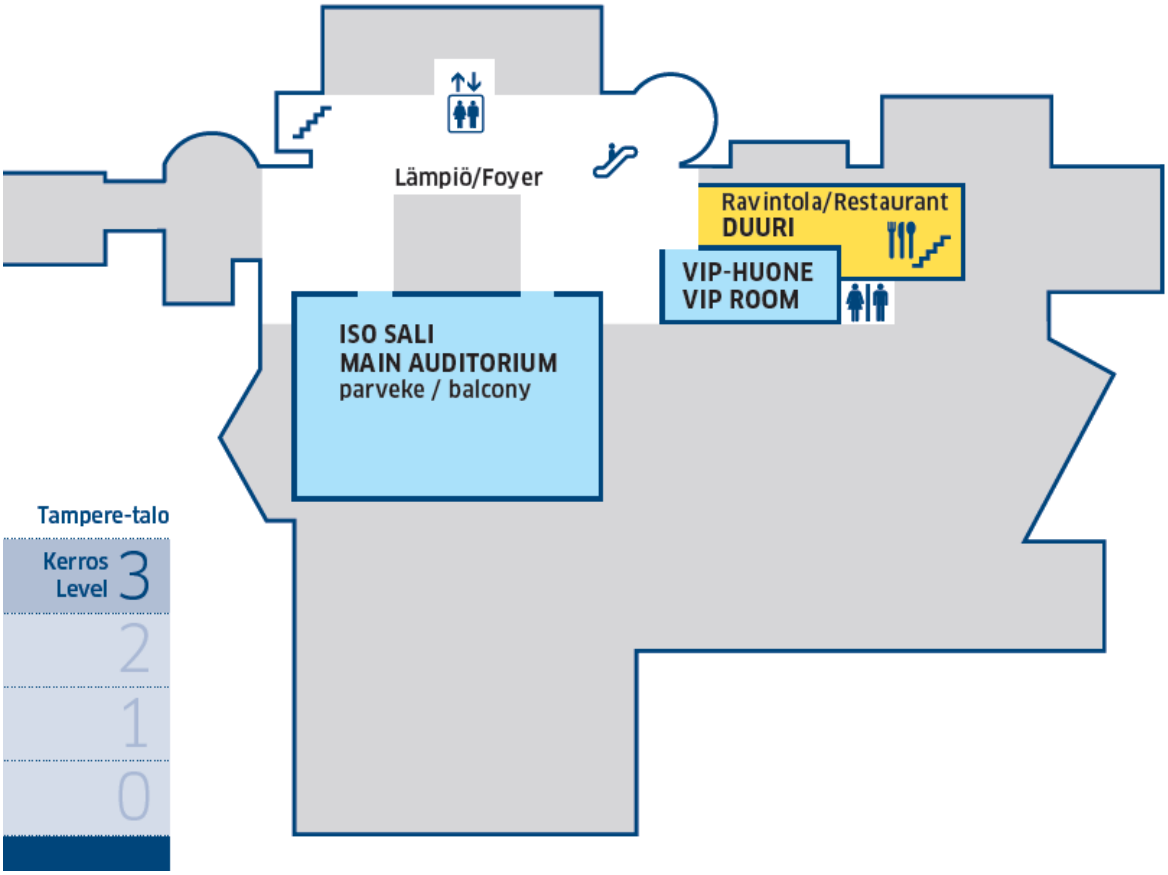
Level 1: main entrance

1	**Lobby**	Sun - Fri	Registration and information counter
2	**Studio**	Sun	CODES+ISSS Tutorial
		Mon – Wed	CODES+ISSS
		Thu – Fri	SoC Conference
3	**Rondo**	Sun - Fri	Coffee and posters; Tour Counter



Level 2

1	**Aaria**	Sun	EON
		Thu	WESS 2012
		Fri	WSS 2012
2	**- Opus 1**	Sun – Fri	Presentation rehearsal and testing room
	- Opus 4	Sun	MeCoES
		Thu	WESE 2012
3	**Pieni Sali**	Mon – Wed	Opening / Keynotes / EMSOFT / CODES+ISSS specials / Industry Day / Closing
4	**Sopraano**	Sun	EMSOFT Tutorial
		Mon – Tue	CASES
		Wed	Joint CASES & CODES+ISSS
		Thu	RSP 2012



Level 3: There are no scheduled events on this floor.

KARTTASYMBOLIT / MAP SYMBOLS

- PÄÄOVI MAIN ENTRANCE — sisäänkäynti / entrance
- esteetön sisäänkäynti / wheelchair access
- WC
- WC
- vaatesäilytys / cloakroom
- lipputoimisto / ticket office
- info/information
- hissi / elevator
- portaat/stairs
- rullaportaat / escalators
- ensiapu / first aid
- ravintola / restaurant
- kahvila / coffee bar
- vauvanhoito / baby care room
- lastaus / loading

DAILY PROGRAMME

Sunday, October 7

Oct. 7 (SUN)	Sopraano	Sonaatti 1	Studio	Sonaatti 2	Opus 4	Aaria
0800-0930	EMSOFT Tutorial 1	CASES Tutorial 1	CODES+ISSS Tutorial 1	CASA	MeCoES	EON
0930-1000	**Coffee Break (Room Rondo)**					
1000-1200	EMSOFT Tutorial 1	CASES Tutorial 1	CODES+ISSS Tutorial 1	CASA	MeCoES	EON
1200-1300	**Lunch (Tampere Hall Restaurant)**					
1300-1500	EMSOFT Tutorial 2	CASES Tutorial 2	CODES+ISSS Tutorial 2	CASA	MeCoES	EON
1500-1530	**Coffee Break (Room Rondo)**					
1530-1730	EMSOFT Tutorial 2	CASES Tutorial 2	CODES+ISSS Tutorial 2	CASA	MeCoES	EON
1800-1930	**Welcome Reception (Museum Center Vapriikki)**					

Tutorials

EMSOFT Tutorial 1: Runtime Verification of Real-time Embedded Systems

Organiser: Borzoo Bonakdarpour, University of Waterloo, Canada

Abstract: *Time-triggered* runtime verification aims at tackling two defects associated with runtime overhead: *unboundedness* and *unpredictability*. In this approach, a monitor runs in parallel with the program under inspection and periodically samples the program state to evaluate a set of properties. The fact that the monitoring tasks occur only at predictable time ticks makes the approach predictable and especially suitable for embedded systems.

In this tutorial, we will discuss the main challenges in implementing time-triggered runtime verification and our solutions. In particular, we will present our work on optimal program state reconstruction, where the problem is known to be NP-complete. This includes our techniques using modern SMT- and ILP-solvers and efficient heuristics. We will also describe our work on time-triggered self-monitoring programs, where a program under inspection is instrumented, so that it monitors its own state within fixed time intervals. We also describe our GPU-based monitoring technique. Such a technique accelerates monitoring tasks and effectively separates monitoring from functional concerns at hardware level. The tutorial will also present our tool chains as well as case studies on monitoring embedded systems using our tools.

Speakers

- Borzoo Bonakdarpour is a Research Assistant Professor with the School of Computer Science at the University of Waterloo, Canada. He obtained his Ph.D. from the Department of Computer Science and Engineering at Michigan State University, USA, in 2009. His Ph.D. dissertation, “Automated Revision of Distributed and Real-Time Programs”, studies a wide range of model repair problems in closed and open systems and was nominated for the 2010 ACM Doctoral Dissertation Award. He was a post-doctoral researcher at the Verimag Laboratory, France, working on the BIP project. His other research interests include runtime verification, compositional verification of embedded systems, and model-based software development. He is the main developer of the tool SYCRAFT which is capable of

synthesizing fault-tolerant distributed programs of size 10^{80} reachable states and beyond.

- Sebastian Fischmeister is an Assistant Professor in the Department of Electrical and Computer Engineering at the University of Waterloo, Canada. He received his MASc in Computer Science at the Vienna University of Technology, Austria, and his Ph.D. degree at the University of Salzburg, Austria. He was awarded the APART stipend in 2005 and worked as a research associate at the University of Pennsylvania, USA, until 2008. He performs systems research at the intersection of software technology, distributed systems, and formal methods. His preferred application areas are distributed real-time embedded systems in the domain of automotive systems, avionics, and medical devices.

EMSOFT Tutorial 2: Mixed critical system design and analysis

Organiser: Rolf Ernst, Technische Universität Braunschweig, Germany

Abstract: With increasing use of embedded systems in safety critical systems, architectures and design processes for safety have become a primary objective in systems design. Most such systems are also time critical leading to safety and time critical systems. Safety standards impose strong requirements on such systems challenging system performance and cost. Very often, however, only part of the functions is safety and time critical calling for a design approach that both meets the safety requirements and provides efficiency and flexibility for less critical functions. These conflicting requirements have given rise to the new research area of mixed critical system design with enormous practical relevance.

The tutorial addresses key aspects of mixed critical system design. The tutorial starts with a short introduction to the topic summarizing requirements and challenges of mixed critical system design. The first lecture by Alan Burns gives an overview of scheduling issues in mixed critical systems and explains first solutions. The second lecture by Lothar Thiele addresses the lack of multicore timing predictability which challenges mixed critical systems integration and proposes a solution based on reducing timing variation. The third lecture by Rolf Ernst and Jimmy Le Rhun explains integration solutions based on switched networks and presents a scalable manycore architecture for mixed critical systems integration.

Topics covered

- Mixed Critical Systems Design – Overview
- Mixed Critical System Scheduling
- Increasing Predictability in Multicore Systems
- Switched Network Systems Integration for Manycore Architectures

Speakers

- Alan Burns is Professor of Real-Time Systems at the University of York, UK. He has pub-lished over 450 papers in the area of real-time systems and is an expert in scheduling theory. In 2009 he was elected a Fellow of the Royal Academy of Engineering and in 2012 he was elected a Fellow of the IEEE for contributions to fixed-priority scheduling for embedded real-time systems.
- Rolf Ernst is a professor at TU Braunschweig. His research activities include embedded systems hardware and software architectures and formal methods for real-time and safety critical systems. He is involved in many projects with automotive, avionics, and smart energy industries.
- Jimmy Le Rhun is research engineer at Thales Research & Technology France, within the Embedded System Lab. He was recently in charge of middleware design for embedded multi-core processors on FPGA, and of the integration of a hardware operating system for heterogeneous reconfigurable multicore platform. He is currently involved in the definition and integration of a safety-critical manycore platform on FPGA.
- Lothar Thiele joined ETH Zurich, Switzerland, in 1994. His research interests include models, methods and software tools for the design of embedded systems, embedded software and bioinspired optimization techniques.

CASES Tutorial 1: Analytical Approaches for Performance Evaluation of Networks-on-Chip

Organiser: Axel Jantsch, KTH Royal Institute of Technology, Sweden

Abstract: In modern system-on-chip (SoC), the on-chip communication infrastructure or network-on-chip (NoC) is a dominant factor for design, validation and performance analysis. SoC designers have tackled performance analysis by exploring the design space using detailed simulations. Simulation tools are flexible and accurate, but often have to be complemented by a formal performance modeling approach. In particular, formal performance analysis can analyze the worst case.

This tutorial reviews four popular mathematical formalisms – dataflow analysis, schedulability analysis, network calculus, and queueing theory – and how they have been applied to the analysis of NoC performance. We review the basic concepts and results of each formalism and provide examples of how they have been used in on-chip communication performance analysis. The tutorial also discusses the respective strengths and weaknesses of each formalism, their suitability for a specific purpose, and the attempts that have been made to bridge these analytical approaches. Finally, we conclude the tutorial by discussing open research issues. The tutorial will be useful to engineers and researchers to obtain a comprehensive overview of formal performance analysis in NoC. It will also be beneficial to researchers that actively work on one of these formalisms and are interested to understand the relation to the other popular models.

Speakers

- Axel Jantsch is professor in Electronic Systems Design at the KTH Royal Institute of Technology, Stockholm, Sweden. His main research interest is in Networks-on-Chip and modeling of embedded systems. He has published over 200 papers in international conferences and journals, and several books in the areas of System-on-Chip and Network-on-Chip, system level modeling, and reconfigurable computing. He has given over 100 invited talks, seminars, tutorials and keynotes.
- Alan Burns is Professor of Real-Time Systems at the University of York, UK. He has published over 450 papers in the area of real-time systems and is an expert in scheduling theory. In 2009 he was elected a Fellow of the Royal Academy of Engineering and in 2012 he was elected a Fellow of the IEEE for contributions to fixed-priority scheduling for embedded real-time systems.
- Marco Bekooij received a M.S.E.E. degree from Twente University of Technology in 1995 and a Ph.D. degree from the Eindhoven University of Technology in 2004. He is currently a principal researcher at NXP Semiconductors and part-time professor at the University of Twente. At NXP he is involved in the hardware and software design of channel decoders. His current research is focused on the design and analysis of real-time embedded multiprocessor systems for stream processing applications and the development of multiprocessor compilers for real-time systems.
- Zhonghai Lu is an associate professor at KTH Royal Institute of Technology, Sweden. He received B.Sc. from Beijing Normal University in July 1989, and earned M.Sc. in June 2002 and Ph.D. in March 2007 from KTH. He had gained 11 years of engineering experience in circuit and embedded systems design after obtaining his B.Sc. and before conducting his M.Sc. and PhD studies at KTH. Since 2002, he has been researching on network-on-chip architectures and performance analysis. He has published over 100 papers in this area.
- Abbas Eslami Kiasari received his M.Sc. degree in computer engineering from the Sharif University of Technology, Tehran, Iran, in 2005. He is currently pursuing the Ph.D. degree in electronic systems under supervision of Prof. Axel Jantsch at the KTH Royal Institute of Technology, Stockholm, Sweden. His research interests include design methodologies and performance analysis of network-based systems.

CASES Tutorial 2: Embedded Reconfigurable Architectures

Organiser: Stephan Wong, Delft University of Technology, The Netherlands

Abstract: In current-day embedded systems design, one is faced with cut-throat competition to deliver new functionalities in increasingly shorter time frames. This is now achieved by incorporating processor cores into embedded systems through (re-)programmability. However, this is not always beneficial for the performance or energy consumption. Therefore, adaptable embedded systems have been proposed to deal with these negative effects by reconfiguring the critical sections of an embedded system. In these proposals, we are clearly witnessing a trend that is moving from static configurations to dynamic (re)configurations.

Consequently, the proposed embedded systems can adapt their functionality at run-time to meet the application(s) requirements (e.g., performance) while operating in different environments (e.g., power and hardware resources). Besides processor cores, we have to deal with memory hierarchies and network-on-chips that should also be (dynamically) reconfigurable. Furthermore, the interplay of these components is increasing the design complexity that can be only alleviated if they can self-optimize.

In this tutorial, we will present and discuss several strategies to perform the mentioned dynamic reconfiguration of the processor, memory, and NoC components - together with their interaction. We will review and present the state-of-the-art for the design of each component that allows for a gradual selection of design points in the trade-off between performance and power. Finally, we will highlight an open-source project that incorporates many approaches for dynamic reconfiguration in both actual hardware and simulation accompanied by the necessary tools.

Topics covered

- Introduction: Need for (dynamic) adaptability? - This part will provide a general introduction to adaptability within embedded systems from the applications and hardware design perspectives. It will be argued that dynamic reconfigurability is the next stage in embedded systems design.
- Heterogeneous behavior of the applications and systems – This part will show, using examples, how the behavior of even a single thread execution is heterogeneous, and how difficult it is to distribute heterogeneous tasks processes among the components in a SOC environment, reinforcing the need for adaptability. This is furthermore complicated when considering multiple threads and the existence of an embedded operating system.
- Adaptive and reconfigurable architectures – This part will present an overview of adaptive and reconfigurable systems and their basic functioning. We will also discuss those which present some level of dynamic adaptability.
- Communication architectures - NoCs – This part will discuss how important NoCs are for future embedded systems, which will have more heterogeneous applications being executed, and how the communication pattern might aggressively change, even with the same set of heterogeneous cores, from application to application.
- Reconfigurable memory hierarchies - This part will present the need for sophisticated memory hierarchies to deal with varying applications and present techniques how the organization of these memory components can be "morphed" when switching applications without much performance loss.
- Tools (compilers and simulators) - This part will discuss the need for a new breed of tools that are needed to support the earlier mentioned approaches.
- Putting it all together – An analysis on the aforementioned techniques: how they can work together

and what will be the impact of their use in future embedded systems. What is the price to pay for adaptability, and for which kind of applications it is well suited.

- Conclusions – A summary of the research discussed and the road ahead.
- Hands-on tutorial (optional) - In this tutorial, we intend to highlight one integrative platform of the earlier mentioned components (core, memory, and NoC) and demonstrate the trade-off using benchmarks and an embedded application.

Speakers

- Luigi Carro (Universidade Federal do Rio Grande do Sul - UFRGS) is a full professor at the Institute for Informatics at UFRGS. He has considerable experience with computer engineering with emphasis on hardware and software design for embedded systems focusing on: embedded electronic systems, processor architecture dedicated test, fault-tolerance, and multi-platform software development.
- Roberto Giorgi (University of Siena - UNISI) is an associate professor at the Department of Information Engineering at UNISI. His main research area is in computer architecture with emphasis on multiprocessor/multicore issues (processor, coherence, and programmability).
- Stamatis Kavvadias (University of Siena - UNISI) is a research associate at the Department of Information Engineering at UNISI. His main research area is memory hierarchy microarchitecture, communication, synchronization, cache coherence, and task scheduling in CMPs.
- Stefanos Kaxiras (Uppsala University - UU) is a full professor at the Department of Information Technology at UU. He has considerable experience in memory systems (highly scalable cache coherence, cache management using reuse distances), power (decay), instruction-based prediction, network processors (IPstash IP-lookup memories), memory/processor integration (datascalar/distributed vector architectures).
- Georgios Keramidas (Industrials Systems Institute - ISI) is a post-doctoral fellow at ISI and a visiting assistant professor at the University of Patras, Greece. His research interests include computer architecture, in particular, the design of memory subsystems of single core and multicore systems.
- Francesco Papariello (ST Microelectronics - STMICRO) is a researcher in the Advanced Systems Technology R&D group at STMICRO. He has been involved in the design and development of simulation and design space exploration tools, among them the Lx (ST2xx family) simulation models and the xSTreamISS, the simulation infrastructure for the xSTream platform (streaming multi-core heterogeneous system).
- Claudio Scordino (Evidence - EVI) is a project manager within EVI and his research activities include operating systems, real-time scheduling, energy saving and embedded devices.
- Stephan Wong (Delft University of Technology - TUD) is an associate professor at Computer Engineering laboratory at TUD. He is the co-inventor of the MOLEN processor architecture and has considerable experience with reconfigurable architectures. He is coordinator of the ERA project (an European funded FP7 project) that is focusing on many topics described in this proposal.

CODES+ISSS Tutorial 1: Coarse-Grained Reconfigurable Architectures - Compilation and Exploration

Organiser: Tom Vander Aa, Imec, Belgium

Abstract: CGRAs consist of an array of a large number of functional units (FUs) interconnected by a mesh style network. Register files are distributed throughout the CGRAs to hold temporary values and are accessible only by a subset of FUs. The FUs can execute common word-level operations, including addition, subtraction, and multiplication. CGRA processors accelerate inner loops of applications by exploiting instruction level parallelism (ILP) and in some cases also data-level and task-level parallelism (DLP & TLP).

The aim of this tutorial is to give insight in CGRA architectures, their compilation techniques, and to experience first-hand how to do source code mapping on a CGRA. Therefore the tutorial consists of presentations as well as a hands-on session.

Topics covered

- Presentation: Introduction to CGRAs and their compilation techniques, taking the ADRES CGRA as an example (45')
- Presentation + demo: Introduction to the DRESC tool chain (15')
- Guided hands-on: The audience can have a first try at compilation and simulation (30')
- Presentation: How to optimize your source code for CGRAs (30')
- Hands-on: The audience will try to optimize a prepared example for the CGRA. (30')
- Presentation: Current research in CGRA compilation: building optimizing compilers using machine learning. (30')

Speakers

- Tom Vander Aa is a senior researcher in the Wireless Communication group of IMEC working on low energy high performance architectures and compilation techniques. Since 2005 he has been working on the ADRES coarse-grain array processor. In 2005, Tom Vander Aa obtained a PhD in electrical engineering from KULeuven, Leuven, Belgium on energy optimization for instruction memory of embedded processors. He has a master in computer science degree, also from KULeuven and is a member of the IEEE.
- Panagiotis Theocharis is a doctoral researcher in the Computer Systems Lab of Ghent University working on split compilation for accelerator-based multicores. He holds a diploma in electrical and computer engineering from the National Technical University of Athens and is a member of the ACM and the IEEE.

CODES+ISSS Tutorial 2: Soft Errors: The Hardware-Software Interface

Organiser: Kyoungwoo Lee, Yonsei University, South Korea

Abstract: A recent report from the ITRS identifies soft errors, as one of the most important reliability challenges for the coming decades. Soft errors are transient errors caused by several effects e.g., voltage fluctuations, wire-cross talks, and cosmic particle strike, and manifest as a temporary switch of the logic value of a transistor. While it is not possible to neither prove nor disprove that a certain error happened due to soft errors, several fiscal disasters (e.g. Sun server crashes in 2000, and HP server crashes in 2005) have been attributed to soft errors. Industry has moved from the position of ignoring soft errors to protection from them. For instance, in nVIDIA's recently announced Fermi GPUs, the L1 cache, L2 cache and register files are ECC protected. Although the soft error rate is about once per year today, it is expected to reach alarming levels of once-per-day in about a decade or two. Researchers are busy finding cost-effective solutions to protect computing devices from soft errors.

This tutorial will attempt to cover the entire gamut of soft error protection techniques, but will particularly focus on the soft error mitigation techniques at the hardware/software interface. Much time will be spent on microarchitectural, compiler, and hybrid compiler-microarchitectural techniques for soft error mitigation. This tutorial will be particularly useful for budding researchers who are fascinated by soft errors, and want to explore this as their research direction. For such researchers, this tutorial will be a one-stop-shop to acquire knowledge of and analyze seminal research work in the field of soft error mitigation, at several design layers. For developers who have been working on soft errors at different levels, this will give them a picture of what can be done at other levels, so that they can provide complementary cross-layer protection. Finally, researchers and developers working on other aspects of system design can learn how soft errors are going to affect them.

Topics covered

- Soft Errors, Trends, and Challenges
- Low-level and Microarchitectural Techniques
- Compiler Techniques for Soft Error Mitigation
- System and Program Level Techniques
- Conclusion and Future Directions

Speakers

- Prof. Aviral Shrivastava: is Associate Professor in the Department of Computer Science and Engineering, at the Arizona State University, USA; where he has established and heads the Compiler Microarchitecture Lab (CML). He received his Masters and Ph.D. in Computer Science from University of California, Irvine, and bachelors in Computer Science from Indian Institute of Technology, Delhi. Prof. Shrivastava received the prestigious 2010 NSF CAREER award for his research and education on Soft Errors.
- Prof. Kyoungwoo Lee: is an assistant professor in the department of computer science and engineering at Yonsei University, Seoul, South Korea, where he has established and heads the Dependable Computing Lab (DC Lab). His research is in the area of embedded systems, with a specific focus on cross-layer design and optimization for error-aware and energy-efficient embedded systems.
- Dr. Reiley Jeyapaul: is a Post-Doctoral Researcher at the Compiler Microarchitecture Lab (CML), ArizonaState University, USA. The focal point of his research is in developing methods to ensure reliability in modern and future computing systems. His PhD thesis involved designing smart

compiler-based techniques for power-efficient reliability in embedded systems. His recent paper on Smart Cache Cleaning, published in CASES'11 was the runner-up Best Paper candidate.

Sunday's Workshops

CASA 2012: Compiler-Assisted SoC Assembly

Organiser: Aviral Shrivastava

The Workshop on Compiler-Assisted System-On-Chip Assembly (CASA) brings together top researchers working on compilation and synthesis of systems-on-chip to talk about their recent research experiences. The theme of this year's workshop is "Accuracy vs. Reliability in Embedded Systems," and in this, we will highlight the simultaneous adversarial and symbiotic relationship between accuracy and reliability, especially in the context of embedded systems.

Held as a part of ESWEEK, CASA is a relatively small workshop, but features high quality presentations from top researchers in the field. As opposed to regular conference talks, the presentations are not narrow, and provide a broad base of understanding. They are excellent for young researchers looking for a deeper understanding of the field, and seeking the questions for next generation research. The workshop allows significant time for question and answer sessions, to foster open and lively discussions.

This year, the 9th CASA workshop will feature keynote by Prof. Krishna Palem, from Rice University, who has over a decade of research insights about "inaccurate computing," and then talks by several luminaries in the field including, Rakesh Kumar (University of Illionois, Urbana Champagne), Christoph Kirsch (University of Salsburg), David Kaeli, (Northeastern University), etc.

MeCoES: Metamodeling and Code Generation for Embedded Systems

Organisers: Wolfgang Ecker and Wolfgang Mueller

Metamodeling is known in the SW domain for over one decade. For almost the same time, applications of metamodels are under development in embedded systems domain: UML metamodels and profiles like SysML, MARTE, or IP-XACT. Metamodeling serves with its domain specific approach (one-fits-one-challenge) as an extension to the classical EDA paradigm (one-fits-all-users). Therefore, metamodeling gives the chance to provide automation for designs following the more-than-Moore paradigm.

Metamodeling is no theoretical construct since recent industrial applications show up to 60% design effort reduction in the complete implementation (Specification-to-Netlist) and up to 95% reduction to specific tasks. This workshop is planned as a platform for the exchange of information between academia and industry and drive forward metamodeling and code generation techniques for Embedded Systems and the exploration of new applications and directions.

EON 2012: Optimization of Computing at the Edge of Network

Organisers: Shahrokh Daijavad, Sumedh Sathaye and Seraphin Calo

The exploding number of mobile devices connected to the network, both operated by humans and self-operated devices (commonly referred to as Machine-to-Machine or M2M) has put a significant burden on both wireless infrastructure and backhaul networks. The notion of edge-computing refers to moving some computation from the traditional back-end data centers or core networks to various edges of the network, closer to the end user. This move results in superior performance of metrics such as latency and quality of experience by end-users in addition to savings such as the network bandwidths. From well-known caching mechanisms to novel analytics performed on "data in motion", in contrast with "data at rest" in the back-end servers, computation at the edge with optimum performance, power, cost and footprint is becoming of

paramount importance. In this workshop, we explore the latest developments both in industry and academia in all aspects of hardware and software (both middleware and applications) that target optimization at the edge of the network. Telecommunications companies and Network Equipment Providers (NEPs) are the main contributors and beneficiaries of computing at the edge, therefore there will be special focus on representative points of view from these industries in this workshop.

Monday, October 8

Oct. 8 (MON)	Pieni Sali	Sopraano	Sonaatti 1	Studio	Sonaatti 2
0800-0830	Opening Remarks Keynote by Hannu Kauppinen, Nokia				
0830-0930					
0930-1000	**Coffee Break (Room Rondo)**				
1000-1200	EMSOFT Session 1A	CASES Session 1	EMSOFT Session 1B	CODES+ISSS Session 1A	CODES+ISSS Session 1B
1200-1300	**Lunch (Tampere Hall Restaurant)**				
1300-1500	EMSOFT Session 2A	CASES Session 2	EMSOFT Session 2B	CODES+ISSS Session 2A	CODES+ISSS Session 2B
1500-1530	**Coffee Break (Room Rondo)**				
1530-1730		CASES Session 3	EMSOFT Session 3	CODES+ISSS Session 3A	CODES+ISSS Session 3B
1830-2030	**ESWeek Organizing Committee and TPC Meeting (Restaurant Finlaysonin Palatsi)**				

Keynote

Room Pieni Sali

Wireless Innovations for Smartphones

The ever increasing demand for fast mobile internet connectivity continues to set challenges for research in radio communications. On one hand the capacity demand can be served by offloading data traffic to local networks. On the other hand using more bandwidth, and possibly dynamically allocating spectrum in a flexible way, will improve the usage of the available spectrum. The future of wireless access continues to be defined by the 3GPP and IEEE standards setting bodies. Radios can also provide innovative features that offer new functionalities for consumers, such as ultra-fast local connectivity, sensing and positioning. This talk will present examples of various radio, sensing and multimedia innovations for smartphones.

Hannu Kauppinen, Nokia Research Center, Finland

Dr. Hannu Kauppinen is currently holding the position of Vice President, Head of Nokia Research Center. In this capacity he is responsible for the long term research of mobile technologies that will secure product differentiation and long-term profitable growth for Nokia. Hannu Kauppinen has a strong track record in bringing research innovations to products.

Hannu Kauppinen joined Nokia Research Center in 1997 has since then held key leadership positions in Nokia's wireless research. He has contributed to and overseen research in cognitive radio systems, cellular systems, wireless local connectivity, networking technologies, software defined radios, RF and antenna design, as well as sensing and positioning radios. During 2007-2008 and 2010-2011 Hannu Kauppinen was

the Director of the Radio Systems Laboratory in Nokia Research Center. He was responsible for the research for 3GPP and IEEE radio standards as well as the research for cognitive and sensor radios to ensure innovativeness and competitiveness of wireless communication solutions in Nokia's products.

Hannu Kauppinen holds a PhD degree in Physics from the Helsinki University of Technology (1997) and an Executive MBA from the Helsinki School of Economics (2007).

CASES

Room Sopraano

Session 1: Security in Memory

Session chair: Heiko Falk

Abstract: Embedded systems are handling sensitive data more often, increasing security requirements. Papers in this session address the intersection of embedded memory design and security by providing techniques for information flow tracking and data authentication, as well as considering side channel attacks in non-volatile memory.

1.1 Side Channel Attacks and the Non Volatile Memory of the Future

Zoya Dyka, Christian Walcyk, Christian Wenger and Peter Langendoerfer

1.2 Static Secure Page Allocation for Light-Weight Dynamic Information Flow Tracking

Juan Carlos Martinez Santos, Yunsi Fei and Zhijie Jerry Shi

★1.3 A Cost-Effective Tag Design for Memory Data Authentication in Embedded Systems

Mei Hong, Hui Guo and X. Sharon Hu

Session 2: Static and Dynamic Compilation Techniques

Session chair: Aviral Shrivastava

Abstract: Static and dynamic compilation systems play an essential role in any software/hardware platform. This session explores ideas related to both static and dynamic techniques, and shows how these techniques can be used to increase performance and portability of various applications in the context of new and emerging architectures.

2.1 From Sequential Programming to Flexible Parallel Execution

Arun Raman, David I. August and Jae W. Lee

2.2 A Hybrid Just-In-Time Compiler for Android

Guillermo A. Perez, Yeh-Ching Chung, Chung-Min Kao and Wei-Chung Hsu

2.3 LLBT: An LLVM-based Static Binary Translator

Bor-Yeh Shen, Jiunn-Yeu Chen, Wei-Chung Hsu and Wuu Yang

Session 3: Optimizing Heterogeneous Multicore Systems

Session chair: Brett Meyer

Abstract: Embedded system designers are increasingly depending on multi-mode, heterogeneous multi-core architectures. The papers in this session present techniques that accelerate thermal modeling by eliminating the need for power traces and physical design knowledge, optimize application mapping for multi-scenario systems, and optimize dynamic application mapping for systems with general-purpose accelerators (FPGAs and GPUs).

★3.1 Power Agnostic Technique for Efficient Temperature Estimation of Multicore Embedded Systems

Devendra Rai, Hoeseok Yang, Iuliana Bacivarov and Lothar Thiele

3.2 Scenario-Based Design Flow for Mapping Streaming Applications onto On-Chip Many-Core Systems

Lars Schor, Iuliana Bacivarov, Devendra Rai, Hoeseok Yang, Shin-haeng Kang and Lothar Thiele

3.3 RACECAR: A Heuristic for Automatic Function Specialization on Multi-core Heterogeneous Systems

John Wernsing, Greg Stitt and Jeremy Fowers

★ Nominated for Best Paper award

EMSOFT

Room Pieni Sali

Session 1A: Testing and Characterization of Embedded Software

1A.1 Debugging Embedded Multimedia Application Traces Through Periodic Pattern Mining
Patricia Lopez Cueva, Aurelie Bertaux, Alexandre Termier, Jean Francois Mehaut and Miguel Santana

1A.2 Smart Layers and Dumb Result: IO Characterization of an Android-Based Smartphone
Kisung Lee and Youjip Won

1A.3 XEMU: An Efficient QEMU Based Binary Mutation Testing Framework for Embedded Software
Markus Becker, Daniel Baldin, Christoph Kuznik, Mabel Mary Joy, Tao Xie and Wolfgang Mueller

Session 2A: Operating Systems

2A.1 Server-Based Scheduling of Parallel Real-Time Tasks
Luis Nogueira and Luis Miguel Pinho

2A.2 Operating System Support for Redundant Multithreading
Björn Döbel, Hermann Härtig and Michael Engel

2A.3 Flattening Hierarchical Scheduling
Adam Lackorzynski, Alexander Warg, Marcus Völp and Hermann Härtig

EMSOFT

Room Sonaatti 1

Session 1B: Theoretical Aspects of Embedded Systems

1B.1 Finite Automata with Time-Delay Blocks

Krishnendu Chatterjee, Thomas Henzinger and Vinayak Prabhu

★**1B.2 Synthesis from Incompatible Specifications**

Pavol Cerny, Sivakanth Gopi, Thomas A. Henzinger, Arjun Radhakrishna and Nishant Totla

1B.3 Timed Model Checking with Abstractions: Towards Worst-Case Response Time Analysis in Resource-Sharing Manycore Systems

Georgia Giannopoulou, Kai Lampka, Nikolay Stoimenov and Lothar Thiele

Session 2B: Control Theory

2B.1 Trigger Memoization in Self-Triggered Control

Indranil Saha and Rupak Majumdar

2B.2 Feedback Thermal Control of Real-Time Systems on Multicore Processors

Yong Fu, Chenyang Lu, Nicholas Kottenstette and Xenofon Koutsoukos

★**2B.3 Synthesis of Minimal-Error Control Software**

Rupak Majumdar, Indranil Saha and Majid Zamani

Session 3: Hardware Support

3.1 Shared Hardware Data Structures for Hard Real-Time Systems

Gedare Bloom, Gabriel Parmer, Bhagirath Narahari and Rahul Simha

3.2 A Low-Overhead Dedicated Execution Support for Stream Applications on Shared-Memory CMP

Paul Dubrulle, Stéphane Louise, Renaud Sirdey and Vincent David

3.3 Partitioned Scheduling for Real-Time Tasks on Multiprocessor Embedded Systems with Programmable Shared SRAMS

Che-Wei Chang, Jian-Jia Chen, Waqaas Munawar, Tei-Wei Kuo and Heiko Falk

★ Nominated for Best Paper award

CODES+ISSS

Room Studio

Session 1A: Software Solutions for Handling Physical Effects in Embedded Platforms

Session chair: Karam S. Chatha

Abstract: The first paper handles the problems created by permanent wear out faults in modern circuits. The work presents the design of a runtime task mapping subsystem which mitigates these faults using a wear-based heuristic. The second work introduces a comprehensive approach to accelerate the design of a heterogeneous multicore embedded system by providing a suite of energy-aware system software with tightly coupled real-time support and performance/power modelling facilities. The last talk presents a system level solution that opportunistically exploits DRAM power variation through physical address zoning.

★**1A.1 A Real-Time, Energy-Efficient System Software Suite for Heterogeneous Multicore Platforms**
Shih-Hao Hung, Chi-Sheng Shih, Tei-Wei Kuo, Chia-Heng Tu and Che-Wei Chang

1A.2 Lifetime Improvement through Runtime Wear-based Task Mapping
Adam Hartman and Donald Thomas

1A.3 ViPZonE: OS-Level Memory Variability-Driven Physical Address Zoning for Energy Savings
Luis Bathen, Mark Gottscho, Nikil Dutt, Puneet Gupta and Alex Nicolau

Session 2A: Managing Parallelism in Multi-core Systems

Session chair: Rolf Ernst

Abstract: The first paper presents a multi-objective optimisation technique exploiting pipeline parallelism automatically, to make it best suitable for resource-restricted embedded devices. The authors of the second contribution consider the problem of hard-real-time scheduling of embedded streaming applications, modeled using data flow graphs, while minimizing the application latency. The third talk addresses the problem of dynamic scheduling of streaming applications on embedded multi-core architectures.

2A.1 Automatic Extraction of Multi-Objective Aware Pipeline Parallelism Using Genetic Algorithms
Daniel Cordes, Michael Engel, Peter Marwedel and Olaf Neugebauer

2A.2 Managing Latency in Embedded Streaming Applications under Hard-Real-Time Scheduling
Mohamed Bamakhrama and Todor Stefanov

2A.3 Dynamic Scheduling of Stream Programs on Embedded Multi-core Processors
Haeseung Lee, Weijia Che and Karam Chatha

Session 3A: Efficient Simulation Techniques

Session chair: Mingsong Chen

Abstract: Functional validation is a major bottleneck in designing complex embedded systems. This session presents fast simulation techniques to reduce overall validation time. The first paper describes a hybrid compiled simulation approach that takes advantage of source-level simulation and provides support for target dependent code by incorporating instruction-level compiled simulation. The next paper presents an efficient strategy to perform dynamic binary translation of VLIW codes on scalar architectures for simulation purposes. The last paper addresses coherency and scalability challenges in adapting a single-pass simulator to a multi-processor SoC with two-level cache hierarchy.

3A.1 HyCoS: Hybrid Compiled Simulation of Embedded Software with Target Dependent Code
Zhonglei Wang and Joerg Henkel

3A.2 Fast simulation of systems embedding VLIW processors
Luc Michel, Nicolas Fournel and Frédéric Pétrot

3A.3 DIMSim: A Rapid Two-level Cache Simulation Approach for Deadline-based MPSoCs
Mohammad Shihabul Haque, Roshan Ragel, Angelo Ambrose, Swarnalatha Radhakrishnan and Sri Parameswaran

★ Nominated for Best Paper award

CODES+ISSS

Room Sonaatti 2

Session 1B: Robust Embedded Architecture

Session chair: José L. Ayala

Abstract: The papers of this session show novel solutions for increasing robustness of embedded systems for single processor architectures, for single processors in a wireless sensor network application, and in network-on-chip of multi-processors.

1B.1 Dynamic Transient Fault Detection and Recovery for Embedded Processor Datapaths
Garo Bournoutian and Alex Orailoglu

1B.2 SPI-SNOOPER: A Hardware-Software Approach for Transparent Network Monitoring in Wireless Embedded Systems
Mohammad Hossain, Woo Suk Lee and Vijay Raghunathan

1B.3 A Novel NoC–based Design for Fault-tolerance of Last-level Caches in CMPs
Abbas BanaiyanMofrad, Gustavo Girão and Nikil Dutt

Session 2B: NOC and Memory Performance Analysis and Mapping

Session chair: Jari Nurmi

Abstract: This session presents new promising approaches that target large scale NoC-based systems and DRAM access optimization. The first presentation introduces efficient distributed interleaving access to DRAM. The second presentation proposes a new mapping strategy aiming to create a balanced activity distribution in order to minimize the power supply noise of NoC-based Systems-on-a-Chip. The last presentation presents a method based on network calculus for worst-case performance analysis of multi-path routing for 2D mesh NoCs.

★**2B.1 A Distributed Interleaving Scheme for Efficient Access to WideIO DRAM Memory**
Ciprian Seiculescu, Luca Benini and Giovanni De Micheli

2B.2 Minimizing Power Supply Noise Through Harmonic Mappings in Networks-on-Chip
Nizar Dahir, Terrence Mak, Fei Xia and Alex Yakovlev

2B.3 Worst-case Performance Analysis of 2-D Mesh NoCs using Multi-path Minimal Routing
Gaoming Du, Cunqiang Zhang, Zhonghai Lu, Alberto Saggio and Minglun Gao

Session 3B: Routing Algorithms and NoC Architectures for Next-Generation 2D/3D SoCs

Session chair: Zhonghai Lu

Abstract: This session presents new routing methods and on-chip interconnect architectures for 2D/3D SoC designs. The first paper presents TDNoC, which is a reconfigurable NoC architecture and dynamic distributed routing algorithm for next-generation flexible SoC designs. Then, the second paper proposes the Roce-Bush router, which is a novel routing-aware design for 3D SoCs. Finally, the third paper proposes a low-cost NoC architecture to provide non-intrusive tracing and debugging support for multi-synchronous SoC designs.

3B.1 The Roce-Bush Router: A Case for Routing-centric Dimensional Decomposition for Low-latency 3D NoC Routers
Miguel Salas and Sudeep Pasricha

3B.2 Non-Intrusive Trace & Debug NoC Architecture with Accurate Timestamping for GALS SoCs
Vladimir Todorov, Alberto Ghiribaldi, Helmut Reinig, Davide Bertozzi and Ulf Schlichtmann

★**3B.3 A Traffic-aware Adaptive Routing Algorithm on a Highly Reconfigurable Network-on-Chip Architecture**
Zhiliang Qian, Paul Bogdan, Chi-Ying Tsui, Radu Marculescu and Guopeng Wei

★ Nominated for Best Paper award

Tuesday, October 9

Oct. 9 (TUE)	Pieni Sali	Sopraano	Sonaatti 1	Studio	Sonaatti 2
0830-0930	Keynote by Satnam Singh, Google				
0930-1000	**Coffee Break (Room Rondo)**				
1000-1200		CASES Session 4	EMSOFT Session 4	CODES+ISSS Session 4A	CODES+ISSS Session 4B
1200-1300	**Lunch (Tampere Hall Restaurant)**				
1300-1500	Industrial Session 1	CASES Session 5	EMSOFT Session 5	CODES+ISSS Session 5A	CODES+ISSS Session 5B
1500-1530	**Coffee Break (Room Rondo)**				
1530-1730	CODES+ISSS Session 6A	CASES Session 6	EMSOFT Session 6	CODES+ISSS Session 6B	CODES+ISSS Session 6C
1830-2030	**Banquet Gala (Restaurant Scandic Rosendahl)**				

Keynote

Room Pieni Sali

Computing Without Processors by Satnam Singh

The duopoly of computing has up until now been delimited by drawing a line in the sand that defines the instruction set architecture as the hard division between software and hardware. On one side of this contract Intel improved the design of processors and on the other side of this line Microsoft developed ever more sophisticated software. This cozy relationship is now over as the distinction between hardware and software is blurred due to relentless pressure for performance and reduction in latency and energy consumption. Increasingly we will be forced to compute with architectures and machines which do not resemble regular processors with a fixed memory hierarchy based on heuristic caching schemes. Other ways to bake all that sand will include the evolution of GPUs and FPGAs to form heterogeneous computing resources which are much better suited to meeting our computing needs than racks of multicore processors. This presentation will highlight some of the programming challenges we face when trying to develop for heterogeneous architectures and a few promising lines of attack are identified.

Satnam Singh, Technical Infrastructure division, Google, USA

Prof. Singh works in the Technical Infrastructure division of Google in Mountain View, California and focuses on the configuration management of Google's data-center services. Previously Prof. Singh worked on the design of heterogeneous systems at Microsoft Research in Cambridge UK and on parallel programming techniques at Microsoft's Developer Division in Redmond USA. He has also worked on re-configurable computing and formal verification at Xilinx in San Jose, California and as an academic at the University of Glasgow. He also currently holds a part-time position as the Chair of Reconfigurable Systems at the University of Birmingham.

Industrial Session

Room Pieni Sali

Session 1: Trends in Automotive Embedded Systems

Session Chair: Rolf Ernst, TU Braunschweig, Germany

Automotive embedded systems have developed from single controllers to networked embedded systems integrating an ever growing variety of distributed applications. New features for driving assistance, improved safety, motor and energy management, and infotainment lead to shorter innovation cycles for software architectures, network technologies, and hardware architectures. While, e.g., the new FlexRay bus standard has just been introduced, next generation Ethernet is already at the edge of introduction. The 4 talks in this session present OEM, 1st tier supplier and semiconductor vendor views from leading automotive companies and suppliers.

Trends and new Challenges in Automotive E/E Architectures

Dan Gunnarsson, BMW, Germany

Over the last decades integrated systems, where functions are partitioned on several ECUs, connected with data communication networks has evolved. During this development new communication methods and principal have been introduced, starting with system with low to moderate complexity moving to highly complex systems. Current requirements on the E/E Architecture are increasingly complex e.g. through the introduction of new and more advanced driver assistance systems where new use-cases like transmission of video streams with real-time requirements are becoming more common. To meet these requirements Ethernet is currently being introduced as an Automotive network. This means that new challenges with regard to gateways and the transition between different protocols and networks have to be mastered. To cope with these increasingly complex tasks new modeling and analysis capabilities are needed.

New Challenges in HW and SW Integration

Stefan Kuntz, Continental, Germany

The continuing increase in/of functionality and density of functions in embedded distributed real-time systems within the automotive industry, as well as the importance of satisfying safety and security requirements in such systems require new approaches in managing the resulting complexities. Namely the integration of hardware and software is a concern and faces new challenges with the advent of multicore and manycore systems in the automotive domain. This presentation identifies the main challenges and sketches out some directions to tackle those challenges utilizing model based development and methodologies.

Virtualisation Support for an Embedded Automotive Environment

Glenn Farrall, Infineon Technologies, UK

Virtualisation is now a well-established and relied upon technology for many environments - servers, cloud computing and even some environments that can be considered embedded. There is a difference however between soft-real time or multimedia embedded environments and systems in the safety and the hard-real time application space. This presentation covers some of the differences in the Automotive arena making the problem both easier and harder in various aspects and some of the features and solutions provided in the AURIX(r) multicore devices to address these issues.

Software Engineering for the next-generation automotive systems

Akihiko Iwai, Denso, Japan

Nowadays automotive E/E systems are getting large and complex due to its growing needs for new functionalities. The source of such new functionalities include active safety applications using vehicle to infrastructure communication, telematics services cooperating with services on cloud, vehicle to grid/home energy management applications. In this talk, while introducing some cooperative works in Japanese embedded systems industries, we will talk about current works and some technical issues of automotive software development.

Session 4: Frontline Challenges in Versatile Computing

Session Chair: Muhammad Shafique

Abstract: New processor architectures have emerged as attractive design options due to their increased computational versatility and performance efficiency. These design options however increase the burden for new adaptive technologies in order to realize their benefits in versatile embedded systems. This session presents some interesting works on low-overhead interconnect architecture for intermediate fabrics, code optimization techniques for loop acceleration for a commercial coarse-grained reconfigurable processor, and automatic workload migration between heterogeneous processors.

4.1 SiblingRivalry: Online Autotuning Through Local Competitions
Jason Ansel, Maciej Pacula, Yee Lok Wong, Cy Chan, Marek Olszewski, Una-May O'Reilly and Saman Amarasinghe

4.2 Function Inlining and Loop Unrolling for Loop Acceleration in Reconfigurable Processors
Narasinga Rao Miniskar, Pankaj Shailendra Gode and Soma Kohli

4.3 A Low-Overhead Interconnect Architecture for Virtual Reconfigurable Fabrics
Aaron Landy and Greg Stitt

Session 5: Static and Dynamic Energy Management

Session chair: Henri-Pierre Charles

Abstract: Energy efficiency remains an important design goal for today's embedded systems. This session presents papers that reduce energy consumption by integrating OLED and EPD displays in a single display system, enabling low-power integration of special instructions in compact ISAs, and controlling the number of active application threads.

5.1 Energy Efficient Hybrid Display and Predictive Models for Embedded and Mobile Systems
Yuanfeng Wen, Ziyi Liu, Weidong Shi, Yifei Jiang, Albert Cheng and Khoa Le

***5.2 Energy Efficient Special Instruction Support in an Embedded Processor with Compact ISA**
Dongrui She, Yifan He and Henk Corporaal

5.3 When Less Is MOre (LIMO): Controlled Parallelism for Improved Energy Efficiency
Gaurav Chadha, Satish Narayanasamy and Scott Mahlke

Session 6: Software/Hardware Techniques for Cache Management

Session chair: Oliver Bringmann

Abstract: This session presents software and architecture level techniques to improve the cache performance in embedded processors. The first paper re-thinks the L0-cache architecture with new L0 data cache organization and explores the impact of migration policy on cache performance. The second paper introduces a novel technique for invalidating cache lines using an instruction and TLB considering dynamic code optimization using just-in-time compilation. The third paper targets static task partitioning for caches with locking support in multi-core systems subjected to hard real-time constraints.

6.1 Lazy Cache Invalidation for Self-Modifying Codes
Anthony Gutierrez, Joseph Pusdesris, Ronald Dreslinski and Trevor Mudge

6.2 Static Task Partitioning for Locked Caches in Multi-Core Real-Time Systems
Abhik Sarkar, Frank Mueller and Harini Ramaprasad

6.3 Revisiting Level-0 Caches in Embedded Processors
Nam Duong, Taesu Kim, Dali Zhao and Alex Veidenbaum

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* Nominated for Best Paper award

Session 4: Invited Session – Code-Level Timing Analysis

Abstract: Embedded systems are often business- or safety-critical, with strict timing requirements that have to be met for the information-processing. Code-level timing analysis (used to analyze software running on some given hardware with regards to its timing properties) is an indispensable technique for ascertaining whether or not these requirements are met. However, recent developments in hardware, especially multi-core processors, and in software organization render analysis increasingly more difficult, thus challenging the evolution of timing analysis techniques. This special session aims to give an overview over the current state of the art and the future challenges with regards to code-level timing analysis and introduces TACLe, a recently started EU-funded networking activity targeting these challenges.

4.1 Timing Analysis for Multicore/Manycore Architectures
Kevin Hammond

4.2 Reconciling Compilation and Timing Analysis
Heiko Falk

4.3 Early-Stage and Portable Timing Analysis
Stefan M. Petters

4.4 Analysis of Mixed-Critical Embedded Systems with Multiple Objectives
Kim G. Larsen

4.5 TACLe - An EU COST Action on Timing Analysis on Code-Level
Björn Lisper

Session 5: Timing Analysis

5.1 Estimation of Probabilistic Bounds on Phase CPI and Relevance in WCET Analysis
Archana Ravindar and Srikant Y. N.

5.2 Assessing the Suitability of the NGMP Multi-Core Processor in the Space Domain
Mikel Fernandez, Roberto Gioiosa, Eduardo Quiñones, Luca Fossati, Marco Zulianello and Francisco J. Cazorla

5.3 Compositional Temporal Analysis Model for Incremental Hard Real-Time System Design
Joost Hausmans, Stefan Geuns, Maarten Wiggers and Marco Bekooij

Session 6: Special Session: An Overview Of The Career of Paul Caspi

Speakers: Edward A. Lee, Stavros Tripakis, Albert Benveniste, Marc Pouzet, Florence Maraninchi

Abstract: This session is dedicated to Paul Caspi. The speakers will present some of his main contributions to the development of safe embedded systems, from programming languages and implementation principles, to control theory and robustness of critical embedded systems.

CODES+ISSS

Room Studio

Session 4A: Advanced Simulation Techniques for Simulation-Based Validation

Session chair: Frederic Petrot

Abstract: Simulation is widely used in today's design methodology for validation of both specification and implementation. This session presents efficient static and dynamic analysis techniques in simulation-based validation. The first paper describes a dynamic mining approach that can infer linear temporal logic properties for embedded software. The next paper presents self-learning techniques to reduce test generation time. The last paper presents an efficient technique to extract code coverage from emulation/prototyping platforms.

★**4A.1 Dynamic Property Mining for Embedded Software**
Marco Bonato, Giuseppe Di Guglielmo, Masahiro Fujita, Franco Fummi and Graziano Pravadelli

4A.2 Efficient Self-Learning Techniques for SAT-Based Test Generation
Ang Li and Mingsong Chen

4A.3 Using Static Analysis for Coverage Extraction from Emulation/Prototyping Platforms
Viraj Athavale, Sam Hertz, Darshan Jetly, Vijay Ganesan, Jim Krysl and Shobha Vasudevan

Session 5A: Advances in Power/thermal optimization

Session chair: Tohru Ishihara

Abstract: This session consists of 3 papers that propose new advances in power/thermal optimization. The first paper proposes to leverage CMOS-TFET heterogeneous architecture to improve performance while satisfy power constraints. The second paper presents a novel load-balancing approach to optimize thermal behaviors. The last paper proposes a new power optimization method for reconfigurable embedded systems.

★**5A.1 Performance Enhancement under Power Constraints using Heterogeneous CMOS-TFET Multicores**
Emre Kultursay, Karthik Swaminathan, Vinay Saripalli, Vijaykrishnan Narayanan, Mahmut Kandemir and Suman Datta

5A.2 COOL: Control-based Optimization Of Load-balancing for Thermal Behavior
Thomas Ebi, Hussam Amrouch and Jörg Henkel

5A.3 Adaptive Online Heuristic Performance Estimation and Power Optimization for Reconfigurable Embedded Systems
Jingqing Mu and Roman Lysecky

Session 6B: Power-Efficient Mobile Computing

Session chair: William Fornaciari

Abstract: This session features papers on power analysis and optimization for smartphone platforms. The first paper deals with an accurate power analysis for hardware components in smartphones. The second paper proposes a technique to detect energy inefficiencies in software on smartphone. The final paper proposes a technique to allow tasks to execute beyond what the worst case thermal constraints would allow for mobile platforms.

6B.1 DevScope: A Nonintrusive and Online Power Analysis Tool for Smartphone Hardware Components
Wonwoo Jung, Chulkoo Kang, Chanmin Yoon, Dongwon Kim and Hojung Cha

6B.2 ADEL: An Automatic Detector of Energy Leaks for Smartphone Applications
Lide Zhang, Mark Gordon, Robert Dick, Morley Mao, Perter Dinda and Lei Yang

6B.3 Don't burn your mobile! Safe Computational Re-Sprinting via Model Predictive Control
Andrea Tilli, Andrea Bartolini, Matteo Cacciari and Luca Benini

★ Nominated for Best Paper award

Session 4B: Emulation of Physical Systems and Design of Wireless Sensor Networks

Session chair: Petru Eles

Abstract: The session presents three papers addressing topics in physical system emulation and wireless sensor networks. The first paper addresses design and synthesis of ordinary differential equation based physical system descriptions on FPGAs for emulation purposes. The second paper discusses a design space exploration and optimization technique for nodes in a wireless sensor network. The final paper presents innovative communication protocols for wireless sensor network composed of energy scavenging nodes.

4B.1 Synthesis of Custom Networks of Heterogeneous Processing Elements for Complex Physical System Emulation

Chen Huang, Bailey Miller, Frank Vahid and Tony Givargis

4B.2 Knowledge-Based Design Space Exploration of Wireless Sensor Networks

Paolo Roberto Grassi, Ivan Beretta, Vincenzo Rana, Donatella Sciuto and David Atienza

4B.3 Spatially- and Temporally-Adaptive Communication Protocols for Zero-Maintenance Sensor Networks Relying on Opportunistic Energy Scavenging

Xuejing He, Robert Dick and Russ Joseph

Session 5B: Enabling Hardware Design in System Context

Session chair: Jarmo Takala

Abstract: Custom hardware, while being an integral part of modern system design, is plagued by long turnaround times and low productivity. This session presents several approaches for accelerated hardware synthesis in a system context. The first paper presents a fast place and route approach to make FPGA synthesis comparable to software compilation. The second paper shows how custom processor architectures can be synthesized directly from a universal ISA specification. Finally, the last paper presents a unified way of modeling hardware components targeting both synthesis as well as vertical integration.

5B.1 BPR: Fast FPGA Placement and Routing Using Macroblocks

James Coole and Greg Stitt

5B.2 Generating Interlocked Instruction Pipelines from Specifications of Instruction Sets

Ralf Dreesen

5B.3 Designing Parameterized Signal Processing IPs for High Level Synthesis in a Model Based Design Environment

Shahzad Ahmad Butt and Luciano Lavagno

Session 6C: System-level synthesis and optimization

Session chair: Brett Meyer

Abstract: Increasing system complexity makes it more challenging to consider real-time constraints, fault tolerance, and heterogeneity in system design. This session has three papers that confront this challenge based on system-level design methodology. The first paper proposes a concurrent optimization technique of the communication architecture and scheduling for an automotive embedded system, in order to satisfy stringent real-time constraints. The second paper presents a simulation framework that supports the early exploration of the different possibilities to apply fault tolerance patterns to MPSOC-based embedded multi-media systems. The third paper presents an approach for synthesis of optimized hardware

communication interfaces integrated into an overall system design flow.

6C.1 Concurrent Architecture and Schedule Optimization of Time-triggered Automotive Systems
Martin Lukasiewycz and Samarjit Chakraborty

6C.2 A SAFE Approach towards Early Design Space Exploration of Fault-tolerant Multimedia MPSoCs
Peter van Stralen and Andy Pimentel

6C.3 Synthesis of Optimized Hardware Transactors from Abstract Communication Specifications
Dongwook Lee, Hyungman Park and Andreas Gerstlauer

CODES+ISSS Special session

Room Pieni Sali

Session 6A: Testbenches for Advanced TLM Verification

Session chair: Wolfgang Mueller

Abstract: This special session presents and reviews new developments for the specification and implementation of test environments with focus on TLM verification and SystemC. The first presentation gives a motivation for the application of UVM-based testbenches (Universal Verification Methodology) in industry. It discusses top-down vs. bottom-up approaches and indicates challenges in the context of industrial SystemC-based design flows. The second presentation introduces the SystemC SVM (System Verification Methodology) libraries, which follow the principles of UVM with standard compatible language and library enhancements for advanced TLM verification. The third presentation deals with mutation testing to measure the quality of testbenches. It proposes an innovative automated framework to generate testbenches that detect mutations for concurrency related defects on SystemC TLM models. The fourth presentation introduces TSL (Testbench Specification Language) as a novel SVM-based approach for stimuli specification. It supports the definition of stimuli generators by means of constrained, weighted and user-defined drivers for mixed digital/analogue models which evolve over time intervals. Finally, since efficient simulation is mandatory for effective testbench-based verification, the last presentation introduces an automatic methodology to simulate SystemC designs on massively parallel GPGPUs architectures, targeting both CUDA and OpenCL thread management libraries.

6A.1 SystemC as A Completing Pillar in Industrial UVM Based Verification Environments

Wolfgang Ecker, Volkan Esen, Tudor Timisescu and Andreas v. Schwerin

6A.2 The System Verification Methodology for Advanced TLM Verification

Christoph Kuznik, Marcio Oliviera, Wolfgang Müller, Finn Haedicke, Hoang Le, Daniel Grosse, Rolf Drechsler, Wolfgang Ecker, and Volkan Esen

6A.3 Generation of TLM Testbenches using Mutation Testing

Marcelo Sousa and Alper Sen

6A.4 A Testbench Specification Language for SystemC Verification

Graziano Pravadelli and Giuseppe Di Guglielmo

6A.5 SystemC simulation on GP-GPUs: CUDA vs. OpenCL

Nicola Bombieri, Sara Vinco, Valeria Bertacco and Debapriya Chatterjee

Wednesday, October 10

Oct. 10 (WED)	Pieni Sali	Sopraano	Sonaatti 1	Studio	Sonaatti 2
0830-0930	Keynote by Jong Choi, Samsung				
0930-1000	**Coffee Break (Room Rondo)**				
1000-1200	Industrial Session 2	CASES+CODES+ISSS Session 7	EMSOFT Session 7	CODES+ISSS Session 7A	CODES+ISSS Session 7B
1200-1300	**Lunch (Tampere Hall Restaurant)**				
1300-1500	Industrial Session 3	CASES+CODES+ISSS Session 8	EMSOFT Session 8	CODES+ISSS Session 8A	CODES+ISSS Session 8B
1500-1530	**Coffee Break (Room Rondo)**				
1530-1730	Industrial Panel				
1730-1745	Best paper award Announcements Closing remarks				

Keynote

Room Pieni Sali

A Standards-Based, Fully-Open Software Platform for Smart Embedded Systems by Dr. Jong-Deok Choi

There has been an explosion of smart mobile devices over the last few years. These smart devices, such as smartphones and tablets, have changed many aspects of modern life. They have also enabled whole new industries to grow up that develop and manufacture "companion products" of the smart devices. These companion products, however, are mostly built around the smart devices, instead of being tightly integrated into them, and fail to utilize the full capabilities of the smart devices. The main cause for their failure is that the software platforms these smart devices are built on are not fully open. This hinders efforts by device manufacturers or software developers to create innovative new products or product categories based on those software platforms.

In this talk, we present Tizen (www.tizen.org), which is a "fully open" software platform for embedded systems. Tizen allows for everyone involved in building and using devices built on it to freely define, invent, add new features or business models, or create new device categories. Tizen offers an industry leading HTML5-based application APIs, the preferred development environment for apps and services for the future. The HTML5-based APIs make it easy for developers to create applications that run across various categories of devices such as mobile, in-vehicle infotainment (IVI), Digital TV, netbooks, health and medical devices, etc. In this talk we also present Tizen's optimization technologies that enable HTML5-based applications to enjoy performance comparable to that of native applications. We also describe how Tizen balances the trade-offs between performance and power consumption, which is of extreme importance for mobile devices.

Jong-Deok Choi, Executive Vice President, Samsung Electronics, Korea

Dr. Jong-Deok Choi is an Executive Vice President at Samsung Electronics in Korea, and is currently in charge of the Software Platform Team within Samsung's Software Research Center. Before joining Samsung electronics, he worked at IBM T. J. Watson Research Center as a Research Staff Member and Manager. While working at IBM Research, he contributed to optimizing Java Webservices applications, the JikesRVM open-source Java virtual machine (JVM), the PTRAN parallelizing-compiler project, and others.

Dr. Choi has published over 50 technical papers in top journals and conferences on various fields in computer science, and holds over 20 US patents. He has served as a program (co-)chair, conference steering-committee member, and program-committee member for numerous technical conferences.

Dr. Choi received his Ph.D. and M.S. in Computer Sciences from University of Wisconsin - Madison, USA, in 1989 and 1985, respectively; M.S. in Electrical Engineering from KAIST, Korea, in 1981; and B.S. in Electronic Engineering from Seoul National University (SNU), Korea, in 1979

Session 2: Internet-of-Energy: Combining Embedded Computing and Communication for the Smart Grid

Session Chair: Ovidiu Vermesan, Sintef ICT, Norway

Driven by increasing cost of energy and by the inclusion of renewable but time variant sources of energy on the production side, and by new requirements from electromobility, building and home automation on the consumption side, the energy grid has moved in the focus of research, industry and infrastructure development. One of the key challenges is the interaction of the numerous em-bedded systems controlling energy producing and consuming devices using an “internet of energy.”

This session will provide different views on this development towards a smart energy grid. The first talk given by a leading provider of energy grid equipment will give an overview on the new developments and challenges in modeling and simulating local grid behavior. The second talk discusses building energy management at the interface between home automation and the smart grid, both from the application and the embedded platform perspective. The third talk addresses home automation which serves many objectives, besides being a terminal network of the smart grind. Last not least, the fourth talk presents new development in wireless sensor devices as an important component of future home and energy networks.

Interactions of Large Scale EV Mobility and Smart Grids - Chances and Challenges of Grid Infrastructure Simulations

Randolf Mock, Siemens, Germany

The complex interactions between electric mobility on a large scale with the electric distribution grid constitute a considerable challenge regarding the feasibility, the efficiency and the stability of smart electric distribution grids. Grid infrastructure simulations which take into account the details of these interactions and which are backed by comprehensive demonstrators may help to shed light on crucial aspects of both energy and information exchange between the traffic and the electric energy infrastructure regime. This will be highlighted by selected topics which intend to shed light on the scope and the challenges inherent in this area of simulation.

Reliable Building Energy Management in the Smart Grid

Moritz Neukirchner, TU Braunschweig; Ruud Wijtvliet, Centrosolar, Germany

Reliable building energy management must guarantee a variety of services, support of local network control for grid stability and optimization, access for remote device maintenance and diagnosis, tamperfree metering, security against attacks targeting the building or network operations. The talk discusses applications, derives embedded platform requirements, and shows first solutions based on virtualization and self-protection.

Home Networks for the Smart Grid and Other Future Applications

Michael Huetwohl, Lantiq, Germany

The number of connected devices in our daily live has significantly increased. And it will continue to further increase x-fold in the near future. IPv6 is the key enabler. The huge social-economic challenges like the transition to renewable energy sources or the aging society are the drivers for this development. The devices and related applications will have a wide spread of different requirements: data rates from kbit/s to Gbit/s, Qualtity of Service, security and reliability will be of significant importance. In order to support these requirements a powerful Home Network and smart, easy-to-use, interoperable communication devices will be needed. The current status of Home Networks is not adequate and needs improvement.

Wireless Sensor Components
Pascal Urard, ST Microelectronics, France

Session 3: Research issues in smart phones, notepads and related services

Session Chair: Tatu Koljonen, VTT, Finland

- **Speakers:**
- **Petri Liuha, Nokia**
- **Kari Pehkonen, Renesas Mobile**
- **Juhani Rummukainen, ST-Ericsson,**
- **Veli-Pekka Vatula, Intel, (tbc)**

Panel: "Low power high performance computing - How could this trend help embedded systems technology?"

Session Chair: Luca Carloni, Columbia University, USA

The computing part determines the effectiveness of many, if not all, of new electronic products such as mobile phones and digital TV and all other kinds of consumer devices. The main indicator of that effectiveness is energy-efficiency, i.e. having higher performance while lowering power consumption. The environmental pressure is generating stringent constraints on computing systems where energy-efficiency needs to be improved drastically. To reach this goal, system and architecture solutions need to be aligned with circuit and fabrication process solutions. This special day brings together key actors from system, architecture, circuit and fabrication technologies to explore strategies for high-performance low-power computing.

Evolution of NoC Technology

Kurt Shuler, Arteris, USA

Energy efficient computing : from technology to algorithm

Fabien Clermidy, CEA, France

Energy efficient computing requires attention at all the embedded system design levels, from technology to algorithm. In this talk, I will discuss how associating technology, design and architectural considerations can lead to drastic power consumption reduction in multi-core systems. On technology side, FDSOI, 3D and Resistive RAM technologies are considered. On design side, asynchronous communication infrastructure associated to mixed variability / power management provide an appealing solution. Finally, power aware and/or algorithm-aware micro-architectures can further help reducing power.

TBD

Jochen Haerdtlein, Bosch, Germany

Session 7: New Advances in Microfluidic Chips

Session chair: Fadi Kurdahi

Abstract: The papers in this session deal with the emerging area of microfluidic chips and systems. The first paper proposes a new virtual biochip topology and associated flow for their dynamic reprogramming. The Second paper addresses the problem of efficient routing in digital microfluidic biochips with limited control pins available, which is very important for biochip scaling. The third paper deals with the architectural synthesis of flow-based, large scale microfluidic chips.

7.1 Fast Online Synthesis of Generally Programmable Digital Microfluidic Biochips

Daniel Grissom and Philip Brisk

7.2 An Intelligent Compaction Technique for Pin Constrained Routing in Cross Referencing Digital Microfluidic Biochips

Pranab Roy, Sudipta Chakraborty, Modud Sohid, Hafizur Rahaman, Parthasarathi Dasgupta and Rupam Bhattacharya

7.3 Architectural Synthesis of Flow-Based Microfluidic Large-Scale Integration Biochips

Wajid Hassan Minhass, Paul Pop, Jan Madsen and Felician Blaga

Session 8: Memory management

Session Chair: Frank Mueller

Abstract: Embedded systems are often characterized by specialized memory structures, including on-chip memories and dedicated memory buffers. Papers in this session manage address mapping for flash memory, allocate data in a local memory with both a software cache and a static buffer, and improve the space efficiency of dedicated buffers by allowing the buffers to be used for multiple purposes.

8.1 DaaC: Device-reserved Memory as an Eviction-based File Cache

Jinkyu Jeong, Hwanju Kim, Jeaho Hwang, Joonwon Lee and Seungryoul Maeng

8.2 Integrating Software Caches with Scratch Pad Memory

Prasenjit Chakraborty and Preeti Ranjan Panda

8.3 Working-Set-Based Address Mapping for Ultra-Large-Scaled Flash Devices

Ming-Chang Yang, Yuan-Hao Chang, Po-Chun Huang and Tei-Wei Kuo

EMSOFT

Room Sonaatti 1

Session 7: Languages, Formal Models and Algorithms (1)

★**7.1 Programming Parallelism with Futures in Lustre**

Albert Cohen, Leonard Gerard and Marc Pouzet

7.2 Towards Network-on-Chip Agreement Protocols

Borislav Nikolic and Stefan Petters

7.3 Input-Output Robustness for Discrete Systems

Paulo Tabuada, Ayca Balkan, Sina Yamac Caliskan, Yasser Shoukry and Rupak Majumdar

Session 8: Languages, Formal Models and Algorithms (2)

8.1 On Model Based Synthesis of Embedded Control Software

Vadim Alimguzhin, Federico Mari, Igor Melatti, Ivano Salvo and Enrico Tronci

8.2 A New Data Flow Analysis Model for TDM

Alok Lele, Orlando Moreira and Pieter Cuijpers

★ Nominated for Best Paper award

CODES+ISSS

Room Studio

Session 7A: Power, Reliability, and Security Issues from Systems to Circuits

Session chair: Vijaykrishnan Narayanan

Abstract: The session features three papers dealing with different metrics for different classes of systems. The first paper addresses the energy efficiency of wireless sensors nodes through novel hardware/software architecture. The second paper describes a methodology for reducing NBTI-induced processor aging that exploits the different criticality of instructions. The third paper presents an architecture that combines retiming and clock gating to cope with side-channel attacks.

7A.1 Enabling Ultra-Low Power Operation in High-End Wireless Sensor Networks Nodes

Carlo Brandolese, William Fornaciari, Luigi Rucco and Federico Terraneo

7A.2 Reducing NBTI-induced Processor Wearout by Exploiting the Timing Slack of Instructions

Fabian Oboril, Farshad Firouzi, Saman Kiamehr and Mehdi Tahoori

7A.3 LRCG: Latch-based Random Clock-Gating for Preventing Power Analysis Side-Channel Attacks

Kazuyuki Tanimura and Nikil Dutt

Session 8A: Co-design in the real world

Session chair: Claudio Brunelli

Abstract: This session will start with an SW-only exploration exercise to find optimal settings for an imaging application. The second paper updates the trade-offs in verification approaches and fills an important gap in modelling multi-core systems. The last paper brings together existing and emerging standards to build reusable test benches for system integration.

8A.1 An Exploration Methodology for a Customizable OpenCL Stereo-Matching Application Targeted to an Industrial Multi-Cluster Architecture

Edoardo Paone, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, Diego Melpignano, Germain Haugou and Thierry Lepley

8A.2 A Case of System-level Hardware/Software Co-design and Co-verification of a Commodity Multi-Processor System with Custom Hardware

Sungpack Hong, Tayo Oguntebi, Jared Casper, Nathan Bronson, Christos Kozyrakis and Kunle Olukotun

8A.3 A Configurable Test Infrastructure using a Mixed-Language and Mixed-Level IP Integration IP-XACT Flow

Erwin de Kock, Jos Verhaegh and Serge Amougou

Session 7B: Real-time and Mixed Critical Systems

Session chair: Todor Stefanov

Abstract: The proliferation of real-time and mission-critical makes safe and efficient design of growing importance. This session presents papers investigating new techniques for (a) worst-case analysis for synchronous data flow models, (b) scheduling critical and non-critical communication on the same shared medium, and (c) improving the energy efficiency of distributed video encoding and decoding. The first paper addresses the problem of multi-scenario synchronous data flow graphs that are not self-timed bounded. The second paper presents a scheduling flow for time-triggered Ethernet where some traffic is rate constrained; a time-triggered schedule is initially developed and subsequently optimized to improve rate constrained traffic performance. The last paper balances video encoding and decoding effort to optimize global energy requirements by focusing motion estimation effort on regions of interests rather than compression the entire image.

7B.1 Worst-Case Throughput Analysis of Real-Time Dynamic Streaming Applications

Firew Siyoum, Marc Geilen, Orlando Moreira and Henk Corporaal

7B.2 Synthesis of Communication Schedules for TTEthernet-based Mixed-Criticality Systems

Domitian Tamas-Selicean, Paul Pop and Wilfried Steiner

7B.3 A Hierarchical Control Scheme for Energy Quota Distribution in Hybrid Distributed Video Coding

Muhammad Usman Karim Khan, Muhammad Shafique and Jörg Henkel

Session 8B: Synthesis of Executable Extra-Functional System-Level Models for Timing and Power Exploration

Session chair: Kim Grüttner

Abstract: In the design of embedded systems extra-functional properties like time and power need to be considered during the entire design process. Often these properties can only be estimated after manually implementing a design for a certain target platform and using state-of-the-art timing and power analysis tools. This special session aims to present current research towards automatic synthesis of executable system-level timing and power models for early exploration. The different talks will cover model-driven design, performance model synthesis, and model-driven design-space exploration of embedded software, synthesis of dynamic power management for embedded software on low-power CPUs, RTL to TLM re-synthesis and abstraction of timing and power properties, run-time resource management for heterogeneous MPSoCs obtained from system-level extra-functional models, and power-aware configuration and synthesis of networked embedded applications.

8B.1 A MDD Methodology for Specification of Embedded Systems and Automatic Generation of Fast Configurable and Executable Performance Models

Eugenio Villar, Fernando Herrera Casanueva and Francisco Ferrero Mateos

8B.2 Software Energy Optimization Through Fine-Grained Function-Level Voltage and Frequency Scaling

William Fornaciari and Carlo Brandolese

8B.3 From RTL IP to Functional System-Level Models with Extra-Functional Properties

Daniel Lorenz, Kim Grüttner, Nicola Bombieri, Valerio Guarnieri and Sara Bocchio

8B.4 Run-time Resource Management Based on Design Space Exploration

Chantal Couvreur, Philipp A. Hartmann, Gianluca Palermo and Fabien Colas-Bigey

8B.5 Network-aware Design-Space Exploration of a Power-Efficient Embedded Application

Mihai Lazarescu, Parinaz Sayyah, Davide Quaglia, Emad Ebeid and Sara Bocchio

Thursday, October 11

Oct. 11 (THU)	Sopraano	Sonaatti 1	Studio	Sonaatti 2	Opus 4	Aaria
0800-0900	RSP	ESTIMedia		MeAOW	WESE	WESS
0900-0930	**Coffee Break (Room Rondo)**					
0930-1130	RSP	ESTIMedia		MeAOW	WESE	WESS
1130-1300	**Lunch (Tampere Hall Restaurant)**					
1300-1500	RSP	ESTIMedia		MeAOW	WESE	WESS
1500-1530	**Coffee Break (Room Rondo)**					
1530-1730	RSP	ESTIMedia		MeAOW	WESE	WESS

Workshops

WESS 2012: Workshop on Embedded Systems Security

Organisers: Dimitrios Serpanos

Abstract: Embedded systems security is becoming increasingly important, considering the increasing adoption of embedded systems in a wide range of applications areas, including a large number of safety-critical systems as well as critical information management systems. The increasing population of Internet-enabled systems introduces significant problems as well, since the Internet can be exploited to attack embedded systems and embedded systems can be used to attack the Internet. Embedded systems are vulnerable to a wider range of attacks than traditional computing systems (e.g., servers) are, because they are physically accessible and widespread. Importantly, bugs, improper use, etc. can also have effects that are indistinguishable from malicious attacks.

WESS provides a forum for the presentation of research work related to all aspects of embedded systems security, ranging from hardware to systems software to application.

ESTIMedia 2012: 10th IEEE Symposium on Embedded Systems for Real-Time Multimedia

Organisers: Jian-Jia Chen and Maurizio Palesi

Abstract: The IEEE ESTIMedia aims to bring together people from different multimedia-related research communities who have worked separately, but did not interact sufficiently to address the challenges facing the design of hardware and software for multimedia systems. After a very successful debut in 2003 and consolidated in successive years, ESTIMedia is continuing to be run in Embedded Systems Week. We hope that this 10th edition will present a good opportunity for specialists from academia and industry to contribute to this exciting research area. The program will bring together original work from both, academic and industrial research and development.

MeAOW 2012: Memory Architecture and Organization Workshop

Organisers: Nikil Dutt and Jason Xue

Abstract: Memory technologies are evolving rapidly, resulting in many new storage opportunities that demand novel memory architectures, organizations and management strategies to effectively leverage their unique features. Newer memories, such as Phase Changing Memory (PCM), STT-RAM, Memristor,

embedded-RAM, etc., have their unique advantages as well as disadvantages. MeAOW 2012 is the second workshop in this series that addresses the urgent need for system designers to model, analyze, design and evaluate novel memory management techniques at varying abstraction levels for these novel memories. The event is designed to foster interactive presentation of early results, new ideas and speculative directions. The workshop will combine a number of invited talks from researchers in academia, technologists from industry, case studies on the use of novel memories, as well as talks selected from submissions to the workshop.

WESE 2012: Workshop on Embedded and Cyber-Physical Systems Education

Organisers: Jeff Jackson, Peter Marwedel, and Kenneth Ricks

Abstract: Embedded and cyber-physical systems design requires multidisciplinary skills from control and signal processing theory, electronics, computer engineering and science, telecommunication, etc., as well as application domain knowledge. Demand for embedded systems engineers has motivated a growing interest in the question of educating specialists in this domain. As system designs grow more complex and the time to market diminishes, quality education becomes more and more important. This sixth workshop on the subject aims to bring researchers, educators, and industrial representatives together to assess needs and share design, research, and experiences in embedded and cyber-physical systems education.

RSP 2012: IEEE International Symposium on Rapid System Prototyping

Organisers: Fabiano Hessel, Jérôme Hugues, Frédéric Rousseau

Abstract:

Keynote: Virtualizing the On-Chip Memory Space by Prof. Nikil Dutt, University of California, Irvine

- Technical Session 1 – Application
  - Hardware-assisted virtualization targeting MIPS-based SoCs.
    Alexandra Aguiar, Carlos Moratelli, Marcos Sartori and Fabiano Hessel.
  - Buffer Length and Traffic Influence on Three-Dimensional NoCs Performance.
    Yan Ghidini, Thais Webber, Edson Moreno, Fernando Grando, Rubem Fagundes and César Marcon.
  - FPGA Prototyping and Performance Evaluation of Multi-standard Turbo/LDPC Encoding and Decoding.
    Purushotham Murugappa, Jean-Noel Bazin, Amer Baghdadi and Michel Jezequel.
  - Case study: deployment of the 2D NoC on 3D for the generation of large emulation platforms.
    Virginie Fresse, Zhiwei Ge, Junyan Tan and Frederic Rousseau.
  - A Spectrum of MPSoC Models for Design and Verification Spaces Exploration.
    Carlos Petry, Eduardo Wächter, Fernando Moraes, Ney L. V. Calazans and Guilherme Castilhos.
  - Graphically Notated Fault Modeling and Safety Analysis in the Context of Electric and Electronic Architecture Development and Functional Safety.
    Nico Adler, Martin Hillenbrand and Klaus D. Müller-Glaser (short).

- Technical Session 2 - Performance evaluation
  - Parity-Based Mono-Copy Cache for Low Power Consumption and High Reliability.
    Ihsen Alouani, Smail Niar, Fadi Kurdahi and Mohamed Abid.
  - A Cycle-level Parallel Simulation Technique Exploiting both Space and Time Parallelism.
    Dukyoung Yun, Youngmin Yi, Sungchan Kim and Soonhoi Ha.
  - An ArchC approach for automatic energy consumption characterization of processors.
    Marcelo Guedes, Rafael Auler, Edson Borin and Rodolfo Azevedo.
  - Automatic Congestion Detection in MPSoC Programs Using Data Mining on Simulation Traces.
    Sofiane Lagraa, Alexandre Termier and Frédéric Pétrot.

• Design For Prototyping of a Parameterizable Cluster-Based Multi-Core System-on-Chip on a Multi-FPGA Board.

Qingshan Tang, Matthieu Tuna and Habib Mehrez.

- Technical Session 3 - Model-based techniques

• HySon: Set-based Simulation of Hybrid Systems.

Olivier Bouissou, Samuel Mimram and Alexandre Chapoutot.

• Automatic Generation of Observers from MARTE/CCSL.

Frédéric Mallet.

• Integrating semantic properties within a Petri net based scheduling tool.

Christian Fotsing and Annie Geniet.

• Seamless Model-Based Design and Deployment of Wireless Networked Systems.

Tobias Schwalb, Tobias Gädeke, Johannes Schmid and Klaus D. Müller-Glaser.

• Enabling Partially Reconfigurable IP cores Parameterisation and Integration using IP-XACT And MARTE.

Gilberto Ochoa, Ouassila Labbani, El-Bay Bourennane and Philippe Soulard.

Friday, October 12

Oct. 12 (FRI)	Sopraano	Sonaatti 1	Studio	Sonaatti 2	Opus 4	Aaria
0830-0930	RSP	ESTIMedia				
0930-1000			**Coffee Break (Room Rondo)**			
1000-1200	RSP	ESTIMedia				

Workshops

ESTIMedia 2012: 10th IEEE Symposium on Embedded Systems for Real-Time Multimedia

Organisers: Jian-Jia Chen and Maurizio Palesi

Abstract: The IEEE ESTIMedia aims to bring together people from different multimedia-related research communities who have worked separately, but did not interact sufficiently to address the challenges facing the design of hardware and software for multimedia systems. After a very successful debut in 2003 and consolidated in successive years, ESTIMedia is continuing to be run in Embedded Systems Week. We hope that this 10th edition will present a good opportunity for specialists from academia and industry to contribute to this exciting research area. The program will bring together original work from both, academic and industrial research and development.

RSP 2012: IEEE International Symposium on Rapid System Prototyping

Organisers: Fabiano Hessel, Jérôme Hugues, Frédéric Rousseau

Abstract:

- Technical Session 4 - Reconfigurable systems
  - Challenges in Software Development for Multicore System-on-Chip Development.
    Ian Gray and Neil Audsley. (short)
  - A New Approach for Pin Detection for an Electronic System Prototyping Reconfigurable Platform.
    Hai Nguyen, Mikael Guillemot, Blaquière Yves and Yvon Savaria.
  - Visualization Support for FPGA Architecture Exploration.
    Konstantin Nasartschuk, Rainer Herpers and Kenneth Kent.
  - Integrated Architecture Exploration Workflow: a NoC-based Case Study.
    Diego Puschini, Julien Mottin, Nicolas Palix, Lian Apostol and Christian Fabre (short).

- Technical Session 5 - System synthesis
  - A Model-Based I/O Interface Synthesis Framework for the Cross-Platform Software-Model.
    Baekgyu Kim, Linh T.X. Phan, Insup Lee and Oleg Sokolsky.
  - Fault-Aware Task Re-Mapping for Throughput Constrained Multimedia Applications on NoC-based MPSoC.
    Anup Das and Akash Kumar.
  - System-Level Prototyping Framework for Heterogeneous Multi-Core Architecture applied to Biological Sequence Analysis.
    Nuno Roma and Pedro Magalhães.
  - FlashBench: A Workbench for a Rapid Development of Flash-Based Storage Devices.
    Sungjin Lee, Jisung Park and Jihong Kim.
  - A Design Flow for Partially Reconfigurable Heterogeneous Multi-Processor Platforms.
    Li Jiashu, Anup Das and Akash Kumar.

- Reducing communication costs on Dynamic Networks-on-Chip through runtime relocation of tasks.
  Philipp Mahr and Christophe Bobda. (short)
- Closing sessions: GC et PC chairs

INTERNATIONAL SYMPOSIUM ON SYSTEM-ON-CHIP (SoC) 2012

SoC is co-located with ESWEEK on Thursday 11th and Friday 12th October 2012. It is being organised for the 13th time now, and it is technically co-sponsored by IEEE Circuits and Systems Society. SoC covers all the aspects from system-level design methodology and design tools through architectures and software to circuit-level implementation issues. The special theme of this year is Reconfigurable Circuits and Systems.

ESWEEK participants can register to attend SoC with a €40 discount. For further information see http://soc.cs.tut.fi/

SOCIAL PROGRAMME

■ ***Lunch***

Date Sunday, October 7 to Thursday, October 11

Time 12:00-13:00

Location Tampere Hall Restaurant

Remarks All registrants are cordially invited; all attendees are requested to wear the ESWEEK 2012 badges.

■ **Welcome Reception**

Date Sunday, October 7

Time 18:00-19:30

Location Museum Center Vapriikki

Remarks All registrants are cordially invited; all attendees are requested to wear the ESWEEK 2012 badges.

■ **ESWEEK Organizing Committee & TPC Meeting**

Date Monday, October 8

Time 19:00-22:00

Location Restaurant Finlaysonin Palatsi

Remarks All ESWEEK Organizing Committee and TPC Members are cordially invited.

■ **Conference Banquet Gala**

Date Tuesday, October 9

Time 19:00-22:00

Location Restaurant Scandic Rosendahl

Remarks Conference registrants (excluding student registrants) will receive banquet coupons.

GENERAL INFORMATION

Conference Venue

Tampere Hall

Yliopistonkatu 55, 33100 Tampere, Finland

Tel. +358 3 243 4111

Registration and Information Counter — Lobby

Operating Hours:

Sunday, October 7	07:30-17:30
Monday, October 8	07:30-17:30
Tuesday, October 9	07:30-17:30
Wednesday, October 10	07:30-17:30
Thursday, October 11	07:30-17:30
Friday, October 12	07:30-10:00

Tour Counter *(Tour reservations, rental of bicycles, kick-bikes, canoes)* — Rondo

Operating Hours:

Sunday, October 7	09:00-12:00 (at registration desk in lobby)
Wednesday, October 10	08:00-17:30
Thursday, October 11	08:00-17:30
Friday, October 12	08:00-17:30

Presentation Rehearsal and Testing Room — Opus1

Operating Hours:

Sunday, October 7	08:00-19:00
Monday, October 8	08:00-19:00
Tuesday, October 9	08:00-19:00
Wednesday, October 10	08:00-19:00
Thursday, October 11	08:00-19:00
Friday, October 12	08:00-12:00

This room on the 2nd floor is equipped with a computer and a projector to be used to test the PPT/PDF presentations before uploading to the computer in the actual session room.

Insurance

The Organizers of ESWEEK 2012 do not provide insurance and do not take responsibility for any loss, accident, or illness that might occur during the Conference or in the course of travel to or from the meeting site. It is, therefore, the responsibility of the participants to check their coverage with their insurance provider.

Bank, Currency, Credit Cards

The currency is the euro (€). The exchange rate in recent months is around US$1.30 to €1. Foreign currencies can be exchanged at banks (typically open Monday-Friday 10:00-16:30) and exchange kiosks (e.g. Forex). Major credit cards are widely accepted in taxis, coaches, trains, shops and restaurants. Traveller's cheques may also be accepted by banks. In city buses you need cash or a pre-paid electronic card.

Service Charges and Tipping

Possible service charges and taxes are included in prices when they apply. Tips are not expected in Finland.

Internet Access

Free wireless internet is available throughout the meeting rooms and public areas of Tampere Hall. Most of the hotels in Tampere, as well as all the Finnish airports, provide free wireless internet. You can also access the internet in a number of places including the City Hall (Aleksis Kiven katu 14), the City Tourist Office (Verkatehtaankatu 2) and the Main Library Metso (Pirkankatu 2).

Author Instructions

Oral Presentation Instructions:

Technical session rooms are equipped with a projector and a laptop with Windows 7. Presenters are requested to upload their presentations to the room laptop using a USB stick. The laptops are equipped with Microsoft PowerPoint, Adobe Reader, and Windows Media Player.

Poster Presentation Instructions:

Display boards (100cm wide by 125cm high) will be available at the coffee break/poster room Rondo. The poster should measure no more than 90cm horizontally and 120cm vertically (e.g. portrait A0 size). Means to attach the posters will be provided at the poster stands. Presenters of the morning sessions are requested to set up their posters prior to the morning coffee break/poster session and remove them by lunchtime. Presenters of the afternoon sessions are requested to set up the posters prior to the afternoon coffee break and remove them by the end of the day.

Electricity

Finland uses electric current of 230 volts at 50 Hz, using the continental European standard plugs with two round pins. Appliances with any other specifications will need an adapter or a transformer. This includes appliances from, e.g., Americas, the UK and Commonwealth, parts of Southern Europe and the Far East.

Travel in Tampere

Helsinki Airport Express Bus

The airport express bus from Helsinki International Airport to Tampere City leaves in front of the terminals

1 and 2 approximately once an hour. In Tampere the bus stops at the main bus station, just a few hundred metres from the conference venue Tampere Hall and the city centre. The price for one way ticket is about €30, and a return ticket about €50. The trip takes 2 to 2½ hours. See http://www.expressbus.fi for more information.

Tampere Airport Bus

Tampere-Pirkkala airport is just 15 km from the centre of Tampere. There are bus services both between terminal 1 and the city (city bus no. 61, running between 6:00 and 22:00 about once an hour), and terminal 2 and the city (Ryanair bus, running at major arrival/departure times). The bus stops are in front of the terminals. The prices are in the range of €4 to €6.

Airport Taxi

Airport Taxi carries passengers between the Tampere-Pirkkala airport and city hotels for a fixed price of €17 per person. It is typically the first taxi at the taxi stand at the airport, and runs according to a predefined schedule from the city direction (you can ask your hotel receptionist to reserve a seat).

Taxi

A regular taxi ride from/to Tampere airport takes about 20 minutes and costs about €40. A taxi ride within central Tampere can be expected to cost between €10 and €20. In the city there are taxi poles at, for example, Keskustori (Central Square), the railway station, the bus station, next to Sokos Department Store and Hotel Cumulus Koskikatu. Call the taxi centre for a taxi to pick you up wherever you are.

City Bus

A single ticket within Tampere (including change of bus line if needed) costs €2.50. Pay upon boarding to the driver with coins or small notes (€20 or smaller). Personal traveller's tickets can be bought for €6 for the first day, €4 per additional day. You may also purchase an electronic ticket (€5) on which you can credit in 20 € increments and benefit from a discounted rate (currently €1.62/person/ride). These tickets can be bought in the city transport (TKL) office at the central square (Frenckellinaukio 2 B, an old brick building). The traveller's tickets can also be bought from kiosks at the bus station, the railway station and the central square. Buses 13, 22 and 10 will take you to Tampere Hall from Keskustori (Central Square).

For further information and timetables, please visit Tampere City Transport's website http://joukkoliikenne.tampere.fi/en/home.html

Railways

The train is a convenient way to visit Helsinki or other cities from Tampere. For further information see www.vr.fi. There are hourly services between Helsinki and Tampere throughout the day. A trip to Helsinki takes only 1:30 to 1:45 hours; the price varies according to a number of variables. The train is less convenient for travelling to and from Helsinki airport, as a city bus or taxi is needed to connect between Tikkurila railway station and Helsinki airport. Tampere airport does not have a railway connection either.

Walking and Biking

As the central area of Tampere is very compact, walking is a good way to get around. Most of the hotels are within 1 km of Tampere Hall and the city centre. You can also rent a bicycle or a kick-bike.

Useful Phone Numbers

The international dialing code for Finland is +358.

Helsinki Airport 24h Info	+358-20-014-636
Tampere Airport	+358-20-708-5450
Tampere City Tourist Info	+358-3-5656-6800
Taxi in Tampere and Surroundings	+358-100-4131
Emergency Number	**112**

Tampere Sightseeing

Pyynikki gravel ridge, café and observation tower

The world's highest gravel ridge Pyynikinharju (ridge of Pyynikki) provides nice views over the lakes surrounding Tampere, especially if you climb up to the old red granite observation tower built in 1929. The café at the root of the tower is renowned for its delicious doughnuts, spiced with cardamom. Or you can just enjoy the nature in the pine forest of the park within walking distance from central Tampere.

Address: Näkötornintie 20, 33230 Tampere

Pispala suburb and haulitorni

A bit further away from central Tampere, yet on the same gravel ridge, begins the famous suburb of Pispala where there are former residences of industry workers from early 1900's and a tower used to make lead grains for bullets (haulitorni). Pispala has been the home of many famous Finns, e.g. the poet and novelist Lauri Viita.

Address: Haulikatu 8, 33250 Tampere (the old shot factory)

Näsinneula observation tower

Take a view over the whole Tampere and its surroundings from the highest building in the Nordic countries. Näsinneula is 168 m high, and near the top there is a revolving restaurant (one revolution takes 45 minutes).

The tower is within Särkänniemi family park which includes an aquarium, a planetarium, a dolphinarium, and, in the summertime, a large theme park with rides for adults and small kids as well (e.g. the world's first Angry Birds Land). The Sara Hildén art museum is also located within the park.

Address: Särkänniemi, 33210 Tampere

Main library "Metso"

The main library of the city was designed by Raili and Reima Pietilä, famous Finnish architects. As the name Metso hints, it looks like a bird from the air (metso = capercaillie, a big bird living in Finnish forests). In the basement of the library is the Moominvalley (Moomin museum). Moomins are fairy tale (and later on cartoon and video) characters created by the Finnish writer Tove Jansson.

Address: Pirkankatu 2, 33230 Tampere

Tammerkoski rapids.

The rapids flow through the city centre. On the banks, there are both parks and old brick-made factory buildings. The Finlayson factories are nowadays hosting restaurants, cinemas, shops and offices. The best local beer can be found in brewery restaurant Plevna.

Address: Itäinenkatu 8, 33210 Tampere (restaurant Plevna)

Museum Center Vapriikki

Vapriikki is also on the banks of the Tammerkoski. The old factory houses a number of special museums and exhibits, such as the Ice Hockey Museum, the Shoe Museum, the Natural History Museum, exhibits on the Tammerkoski, innovations, Tampere 1918 (The Civil War), Historical Toys, etc.

Address: Alaverstaanraitti 5, 33100 Tampere

Lakes Näsijärvi and Pyhäjärvi

Tampere is on a narrow neck of land between two lakes. You can admire the lakes from terra firma, or maybe take a late autumn cruise or rent a canoe for a closer look.

Address: Laukontori (boat harbour) + several locations

The Market Hall is a bit hidden between the central square and the department store Sokos. You find there meat, fish, vegetables, bread, and a couple of simple cafés offering not just coffee but also straightforward lunch, such as Finnish green pea soup (hernekeitto).

Mustamakkara (black sausage) is a famous delicacy from Tampere, made of blood, grains and meat (pork). You can taste it fresh in the Market Hall or at Tammelantori or Laukontori market squares.

Address: Hämeenkatu 19 / Hallituskatu 10, 33200 Tampere

Sokos department store is located near the central square, along the main street Hämeenkatu. In addition to stocking well-known domestic and international brands, offerings include Sokos private label products. There is a grocery store and lunch café in the underground part of Sokos, and two other cafés on street level and on the 4th floor.

Address: Hämeenkatu 21, 33200 Tampere

Stockmann department store is another big department store in the city, near the railway station. In addition to a large variety of goods of all kinds, it hosts a takeaway café on street level, and a lunch café on the 3rd floor. Next to it, there is a large book store Akateeminen Kirjakauppa.

Address: Hämeenkatu 4, 33100 Tampere

Koskikeskus shopping centre near Hotel Ilves consists of about 70 shops, cafés, restaurants, and services. You can find fashion for all ages and sizes, sports utilities, books, jewellery, shoes, kitchenware, interior design, a chemist, toys, mobile phones, etc.

Address: Hatanpäänvaltatie 1, 33100 Tampere

Kehräsaari Boutiques: next to Laukontori market square, across a pedestrian bridge from Koskikeskus, there is the small island of Kehräsaari, which hosts small boutiques in old factory buildings. You can find Finnish handcrafts and design, unique clothing items, and utensils for the sauna.

Address: Kehräsaari, 33100 Tampere

IKEA store is on the outskirts of Tampere. In addition to inexpensive and clever furniture, there are a lot of home and office utensils and interior textiles for sale. There is also a café and restaurant serving, for example, the famous Ikea meat balls, so you can continue shopping for the whole day if you so wish.

Address: Leppästensuonkatu 4, 33840 Tampere (**City bus no. 3**)

Ideapark shopping mall is located about 20 km from Tampere city, beside the Helsinki to Tampere highway. There are nearly 200 shops and 30 restaurants and cafés. There is also an inside theme park.

Address: Ideaparkinkatu 4, 37570 Lempäälä (**bus line 55**, 51 or 52)

TAMPERE UNIVERSITY OF TECHNOLOGY

An international university of technology at the leading edge

Tampere University of Technology (TUT) conducts scientific research in technology and architecture and provides higher education within these fields. TUT started operating in the form of a foundation in the beginning of 2010. TUT is a significant national and international pioneer in the development of technology and a sought-after cooperation partner among the scientific community and business life. In its own fields, TUT is Finland's most attractive research and study environment. Internationality is inherently linked to all activities.

TUT's operations are founded on a combination of strong research of the natural sciences and technology and research related to industry and business. Many research fields play a major role in addressing global challenges, such as climate change and demographic ageing. The most extensive and established of the international leading-edge fields of research at TUT are signal processing, nanophotonics and intelligent machines. TUT offers its students an opportunity for a broad, cross-disciplinary education. The largest fields of study at TUT are information technology and electrical, mechanical, automation and civil engineering.

The local organization of ESWEEK 2012 is carried out by the Department of Computer Systems of TUT.

Banquet Bus Timetable

Date	Time	Depart From	Destination
Oct. 9	18:10	Tampere Hall	Scandic Rosendahl
	18:10	Hotel Ilves	Scandic Rosendahl
	18:10	Hotel Scandic City	Scandic Rosendahl
	18:40	Holiday Inn	Scandic Rosendahl
	18:40	Railway Station	Scandic Rosendahl
	18:40	Old Church at Central Square	Scandic Rosendahl
Oct. 9	21:40	Scandic Rosendahl	Holiday Inn / Tampere Hall
	21:40	Scandic Rosendahl	Hotel Scandic City / Railway Station
	21:40	Scandic Rosendahl	Main Street / Hotel Ilves
	22:20	Scandic Rosendahl	Holiday Inn / Tampere Hall
	22:20	Scandic Rosendahl	Hotel Scandic City / Railway Station
	22:20	Scandic Rosendahl	Main Street / Hotel Ilves

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