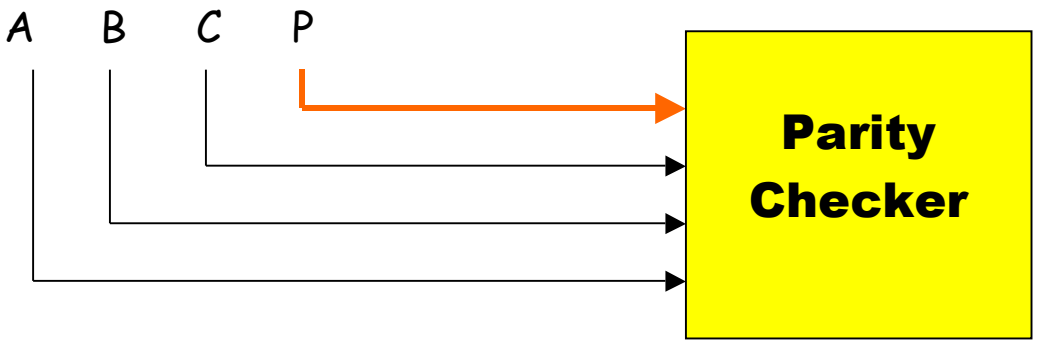
Error Detection and Correction

Transmission or reading errors can corrupt data. If the extent of the damage is known, then error detection codes can **detect** if the data has been corrupted. Using special type of error-correction codes, we can even **correct** errors.

Parity Checking for single error detection



The parity-bit generator generates a P so that the number of 1's in the transmitted data is odd (or even). The **parity checker** checks this in the received data. How will you design (1) a parity-bit generator, and (2) a parity checker?

Hamming Code

Hamming code not only detects if there is an error, but also locates where the error is, and subsequently corrects it. Here is an example:

1	0	1	**1**	1	**1**	**0**
7	6	5	4	3	2	1

The 4-bit data (1 0 1 1) to be sent is placed in bit positions 7, 6, 5, 3 of a 7-bit frame. The remaining bit positions are reserved for error-correction bits, and their values are chosen so that there is **odd parity** for bit combinations

(4, 5, 6, 7),

(2, 3, 6, 7),

and (1, 3, 5, 7).

What is special about these sets of bits?

The receiver, upon receiving the 7-bit data, computes the parities of the above bit combinations, and reports the result using three bits b2, b1, b0 as follows:

Odd parity for bits 4, 5, 6, 7 □ b2 = 1 else b2 = 0.

Odd parity for bits 2, 3, 6, 7 □ b1 = 1 else b1 = 0.

Odd parity for bits 2, 3, 6, 7 □ b0 = 1 else b0 = 0.

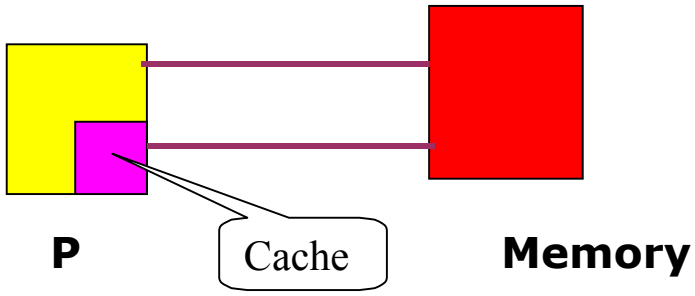
If b2 b1 b0 = 000 then there is no error, otherwise, the decimal equivalent of b2 b1 b0 reports the position of the corrupt bit. To correct the error, the receiver flips that bit.

Question 1. It works for single errors only.

Can you figure out why it works?

Question 2. Can you generalize it to 32-bit data? How many extra bits will you need to correct a single error? Where will you position these bits?

Cache memory



Cache

Cache is a small high-speed memory. Stores data from some frequently used addresses (of main memory).

Cache hit

Data found in cache. Results in data transfer at maximum speed.

Cache miss

Data not found in cache. Processor loads data from M and copies into cache (miss penalty).

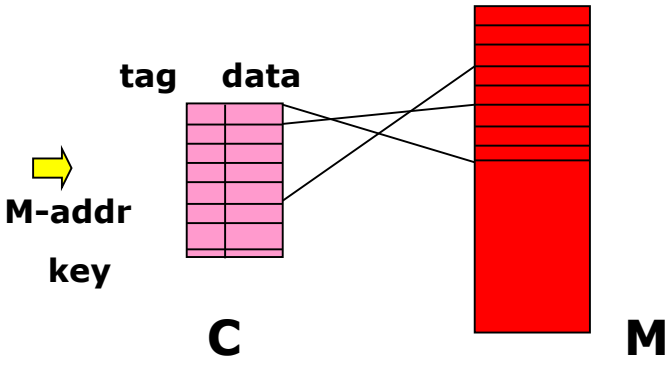
What are Hit and Miss ratios?

What happens during a write operation?

Cache Line

Cache is partitioned into lines (also called blocks). Each line has 4-64 bytes in it. During data transfer, **a whole line** is read or written.

Each line has a tag that indicates the address in M from which the line has been copied.



Cache hit is detected through an associative search of all the tags. Associative search provides a fast response to the query:

"Does this key match with any of the tags?"

Data is read only if a match is found.