Embedded COMPUTING DESIGN

2006
Resource Guide

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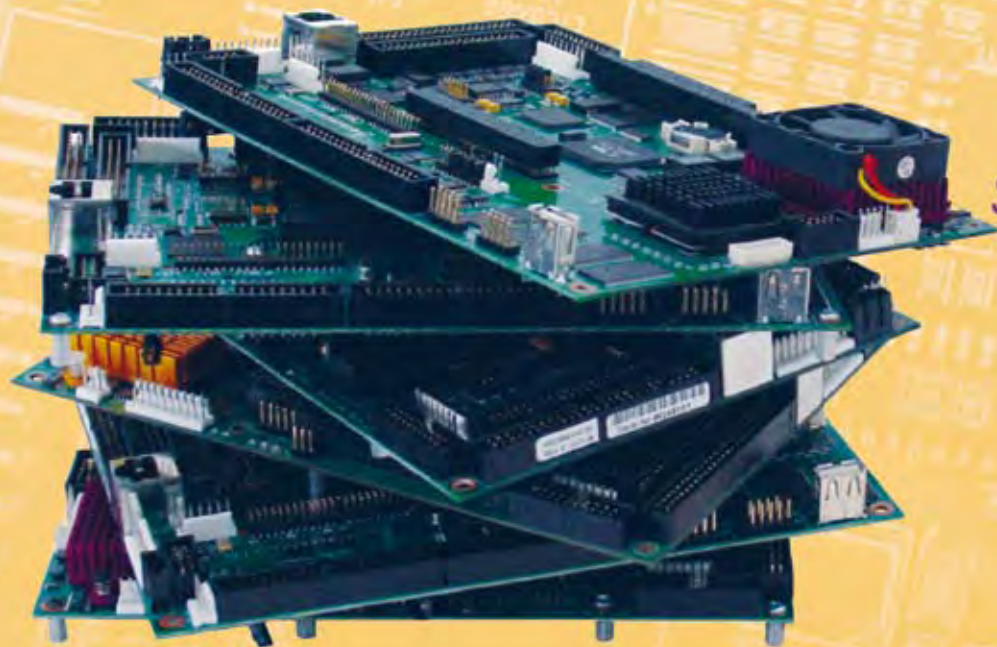
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Federation *of* Associations

Jerry Gipper

This month we're spotlighting customization of embedded computing designs, a trend based on various degrees of product modularity. The special feature on page 17 analyzes each type of modularity a design team should consider when designing a product. The modularity strategy chosen determines the degree of customization possible.

Successful modularity demands module standards. Without standards, modules are not compatible and interchangeable enough to make the strategy work. Standards must be broadly accepted to maximize the options a consumer can choose from to enable the desired level of product or service customization.

The embedded computing industry has a cornucopia of standards, many of which have been very successful. Some examples include VMEbus, PCI bus, PMCs, Ethernet, SCSI, RS-232, and so on. Others started out proprietary and have become de facto standards simply through great market acceptance; for example, the Intel architecture and Windows. As technology evolves, more standards will appear to facilitate the acceptance of advancing technology.

Many organizations, alliances, and associations have formed through the years to address the need for standards in embedded computing. Most of these are established to rally around some type of innovation developed by a single company looking to expand the supporting ecosystem. Others are formed by several companies that have a common interest in a technology or market. Many have evolved from a single point of focus to a broader focus within their interest domain, opening to broader markets to give consumers the choices they demand.

But I wonder: How many of these organizations are appropriate? Do they have the right focus? Are they really interested in the good of the consumers? Can or should some of them be consolidated? I am currently tracking more than 100 different organizations working on some form of common goal, a standard or specification for the embedded computing industry. New organizations are added to my list every week, and I'm sure I'm capturing less than half of all the established organizations out there. See for yourself at www.embedded-computing.com/consortia.

I would like to see these organizations work more closely together for the good of the embedded computing industry. How should this be done? Should the industry form a *Federation of Associations*, an organization of associations of embedded computing interest groups? This Federation of Associations could provide a forum for cooperation in addressing common issues in the embedded computing industry. It would support activities to endorse standards, delivery of specifications, specification gap analysis, and regulatory action to protect consumers. It could also provide educational opportunities and foster communication and discussion on the latest technologies.

Some organizations have begun doing this. SCOPE Alliance, www.scope-alliance.org, is an association of network equipment providers aimed at accelerating the deployment of carrier grade base platforms for service provider applications. In this case, equipment providers are defining technical profiles that reflect the technical requirements regarding interfaces and building blocks to form a carrier grade base platform that meets service providers' requirements. SCOPE works with existing standards-focused organizations to level their work in the profiles and identifies gaps that need additional specifications work. For the scoop on SCOPE, check out the E-cast entitled "Working Together to Drive a Mainstream Market for Open Industry-standards-based Communications Platforms" at www.opensystems-publishing.com/ecast.

> "Establishing sets of specifications or profiles with high degrees of inter-operability (leading to larger consumer acceptance) would be beneficial for the entire industry.

SCOPE may be a good model for other technology segments within the embedded computing industry to follow. Establishing sets of specifications or profiles with high degrees of interoperability (leading to larger consumer acceptance) would be beneficial for the entire industry. These types of profiles could be used in nearly any type of embedded computing application, from HDTV to PCI Express. Maybe it is time to form a strategic Federation of Associations.

As always, I would enjoy hearing your comments on embedded computing standards organizations. What would you like to see changed to make using embedded computing technology easier? I would be happy to feature some of your ideas in upcoming issues. Your suggestions and comments are welcome. Please contact me at jgipper@opensystems-publishing.com.

Jerry Gipper
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By Don Dingee

Ab fabless deals

Did you hear that? It sounded like a couple of big semiconductor firms left a part of the market and a couple of smaller fabless companies stepped in to try to make money with two popular embedded processor architectures.

Two major semiconductor vendors recently announced plans to sell off their well-known but financially underperforming embedded processor families:

- AMD sold their Alchemy line of processors to Raza Microelectronics, Inc. (RMI)
- Intel sold their XScale line of processors to Marvell Semiconductor

Both these architectures were acquired just a few short years ago when AMD and Intel thought handheld devices would be their next great battleground. But both companies decided they couldn't make a sustainable profit on these parts.

Most analysis of these deals has highlighted the benefits AMD and Intel may gain from shedding these pieces. But I see something else going on here – the move to a fabless model for embedded processor firms. Can fabless companies perform better with these architectures?

RMI gets the magic

RMI's acquisition of the Alchemy lines seems to be a natural fit for them, as they develop advanced semiconductor solutions for information infrastructure, network security, wireless, and digital consumer markets.

RMI is a relatively small private company with undisclosed revenue figures. RMI's CEO, Atiq Raza, previously founded NexGen and served as COO of AMD after NexGen was acquired. The small firm focuses on delivering power efficient solutions with their most popular product to date, the XLR processor family, a high-end MIPS64 multicore architecture for network acceleration functions.

The Alchemy product lines create an opportunity for RMI to enter the lower end of the MIPS spectrum in their application space, but they'll face stiff competition there. The real win for RMI may be an agreement to collaborate on Torrenza, AMD's ecosystem effort to open up and promote Direct Connect Architecture and HyperTransport technologies around the AMD64 core architecture.

Marvell scales up

Marvell is best known for providing switching, transceiver, wireless, communication controller, and storage silicon. Their acquisition of the XScale lines immediately gives them a strong position in some of today's latest consumer devices, including the Motorola Q, the Palm Treo 700p and 700w, and the RIM Blackberry 8700.

Marvell had fiscal 2006 revenue of $1.67 billion. Intel will continue to fab the XScale parts until Marvell transitions them into their fab suppliers. Marvell had already been optimizing their WLAN products to work with XScale processors, so the technical synergy of the deal is clear. With their portfolio, focus, and some new innovation, Marvell could create *critical mass* for XScale devices where Intel struggled.

Ab fabless is money

Is fabless the key to making money in the embedded space? I'd say so, and the acquiring companies in these deals would probably agree.

> **Smaller fabless firms are generally more nimble, better focused, and better able to leverage available contract fab technology and capacity.**

Big, asset-heavy companies, especially those focused on high-end processors, are often lost when it comes to smaller, lower-cost embedded devices. These firms have giant, multibillion wafer fabs that must be fed by enormous volumes of very large, complex wafers. It's the *operational excellence* model applied to high tech – mass produce items where the barriers to entry are high, and profit by creating and executing high-yield processes. This is a key requirement for a device such as an Opteron or a Core Duo, but it's not quite the right model for less expensive embedded processors.

Smaller fabless firms are generally more nimble, better focused, and better able to leverage available contract fab technology and capacity. This frees them to spend intellectual capital innovating new, creative solutions for embedded markets, while still remaining cost competitive. Other benefits include more concentrated sales and marketing efforts, shorter development cycles, and potential profitability on a smaller volume of shipments.

The fabless semiconductor model fits with this issue's theme of *mass customization*, which we think is the wave of the future in embedded computing designs. I think Marvell has a good chance to put life back into the XScale architecture, while I see the win for Raza as a larger partnership with AMD. Whatever the outcomes, I consider the fabless model the right way to go. What do you think? Are these deals a good thing for our industry? Do fabless business models seem to work? We welcome your thoughts and ideas. E-mail me at ddingee@opensystems-publishing.com.

Images Courtesy of Navy.mil

Better than Ultimate?
The ICS-645D puts it all together.

The ICS-645C was a finalist in the EE Times Ultimate Products program – so imagine how good the 32-channel ICS-645D PCI data acquisition card is. It takes the robust, stable ICS-645C platform with its differential inputs and four voltage ranges and builds on it, with onboard storage increased to 16 MBytes. Even better, the ICS-645D now features 64-bit, 66 MHz PCI 2.2, increasing PCI bandwidth by a factor of four. Integrated ADC, gain, anti-alias filtering and programmable clock all come as standard.

The benefit? No need to provide separate signal conditioning circuitry in advance of the analog to digital conversion – and no need for an auxiliary clock source either. It's all there, right on the board, ready to go. That can mean simpler, more compact, more cost-effective systems – and shorter development times.

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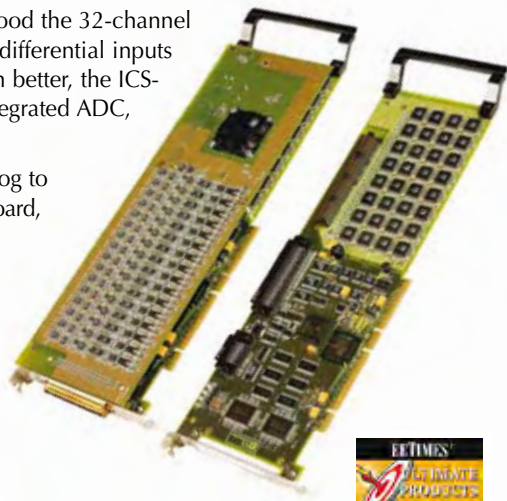
ICS-645C chosen as a finalist in the Ultimate
Products supplement of EE Times Feb 2005

Embedded devices for those with disabilities

By Hermann Strass

N ot all embedded computers just compute or move data. Embedded computing devices such as those from Otto Bock Healthcare, Germany, and other companies can significantly improve the lives of people with disabilities. Embedded computing electronics can monitor, control, navigate, and communicate with devices from artificial prosthetics to various types of transportation.

Embedded prosthetics

Embedded systems may be *embedded* in technical equipment as well as in and on the human body. An artificial elbow joint called DynamicArm (Figure 1) from Otto Bock Healthcare is the world's first completely microprocessor-controlled, orthobionic auto-adaptive dynamic arm that can lift up to 6 kg (more than 12 pounds), about six times its own weight. Nerve actions sensed through muscular vibrations on the living arm translate into computer-controlled arm movements. Essentially, the DynamicArm becomes an integral part of a human body.

This embedded system is based on a commercial microcontroller using the Time Triggered Protocol (TTP/A) on an Axon bus (often used on aircraft) for communication among the sensors, microprocessor, and infinitely variable drive motors. It automatically adapts in real time to various loads on the arm. The DynamicArm, which Otto Bock Healthcare jointly developed with their Austrian research subsidiary and the Technical University of Vienna, gets its individual parameters through a Bluetooth-based BionicLink.

Figure 1

The C-Leg pictured in Figure 2 (see the Embedded Technology in Europe column in the May 2005 issue of *Embedded Computing Design*) has been upgraded in the last year. A wireless remote control that allows switching between activity modes has been added. The C-Leg wearer can use remote control to quickly and inconspicuously switch from first mode to second mode when bicycling, inline skating, ice skating, and so on. A standing mode can be activated for additional safety. This standing mode stabilizes the C-Leg at any flexion angle, in spite of dynamic alignment, without the wearer having to use muscular strength to ensure steadiness.

Individual adjustment of the swing phase control has also been added to the C-Leg, which users can easily adjust by remote control without compromising safety. A knee angle sensor measures step length and frequency, and transmits this information for dynamic control of the swing phase. For safe standing, a load sensor measures the heel strike and forefoot load through strain gauges.

> **The Superfour can drive a world record distance of up to 200 km (120 miles) without refueling or battery charging.**

Embedded assistance vehicles

Otto Bock Healthcare also has developed a motor-powered wheelchair that can be used off-road like a jeep. The Superfour resembles a quad all-terrain vehicle and is powered by batteries and a diesel engine. It has a GPS system, sensors, and embedded computers that monitor the geographic location, inclination angle, diesel fuel supply, battery status, and other parameters of the vehicle as well as heart beat, oxygen in the blood, and other medical data of the wheelchair occupant. The electronic supervision in a central base station can monitor a whole fleet of wheelchairs. It automatically generates alarms if the wheelchair starts to tip over or the user's heart rate increases to a dangerous level. The seat automatically adjusts to a horizontal position in rough terrain. Four independent drive motors enable the Superfour to accelerate even in terrain with a 40 percent incline. The Superfour can drive a world record distance of up to 200 km (120 miles) without refueling or battery charging.

Figure 2

Another vehicle from Otto Bock Healthcare, the Paragolfer (Figure 3), can drive in uneven terrain and help people with disabilities, including paraplegics, play golf outdoors. It lifts the user's body to an upright position so he or she can freely move their shoulders to hit the golf ball right at the target. Some airlines carry the Paragolfer onboard their aircraft free of charge. Christian Nachtwey, a German golf professional, and the trainer of the German National Golf Team, Anthony Netto, helped develop the Paragolfer.

Recognition

Otto Bock Healthcare's DynamicArm was runner-up for this year's Hermes Award, which was presented at the International Hannover Fair in April with the German chancellor in attendance. Otto Bock Healthcare is one of 50 members of Germany's all-time innovation hall of fame, which covers the last 500 years. The

Figure 3

hall of fame includes individuals such as Johannes Gutenberg, inventor of the printing press, Rudolf Diesel, inventor of the diesel engine, and Gottlieb Daimler, inventor of the motorcycle in 1885 and coinventor of the automobile with Carl Benz (DaimlerBenz, now DaimlerChrysler).

For more information, contact Hermann at: hstrass@opensystems-publishing.com.

Figures courtesy of Otto Bock Healthcare

Embedded World review and an embedded human body system
By Hermann Strass
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ALF and 10 questions every QA team should ask

By Tracy Ragan

To head off software problems before they start, developers and Quality Assurance (QA) teams need a way to anticipate, identify, and manage issues that might arise. When problems occur with a new release, QA teams get a lot of questions, many of which are tied more to the code development process than just the QA process.

Ten questions QA teams ask on an every day basis can expose key issues that show up in most new software releases:

1 What requirements initiated the new software release?

Be sure requirements are understood and accepted and that new features are really necessary.

2 What additional features were added to the release and who requested these new features?

Avoid *scope creep* and understand how new features not defined in the initial requirements may have been added to a release.

3 Were the new features reported to QA and were test cases created?

QA is too often the last to know about any new feature. Test cases against new features should be the first set of cases to be executed.

4 How did the changes affect the overall application and was the impact added to the time line?

Development teams often do not know the answer since analysis may be difficult and time consuming. The application build process should provide this level of impact information, and QA can use it to target particular test cases at crunch time.

5 Did the development team initiate any unexpected changes?

Developers often like to sneak in a few modifications to source code *while they are in there*. If a module must be updated, fixing old problems and cleaning up code is not unusual, but can be problematic.

6 Who approved the changes to be promoted to the new release and do these changes match the approved requirements?

The project manager should be aware of the level of system testing completed before the application moved to QA, and be confident the development team is truly finished and all requirements have been met.

7 Where is the approved source code managed and stored, and are all third-party libraries also managed and stored?

Getting all the pieces together is a must. If baselined source code can't be found, it's difficult to fix a release.

8 How did the application build process verify matching source to executables, and is all source code used in the build coming from the approved and managed source code repository?

Just because source code is stored in a central repository does not mean the executables moving through the QA environment were created from that source code.

9 Based on the impact of the source code changes, what test cases were selected as *critical*?

Discover what test cases must be executed prior to a production release. Knowing this will allow QA teams to refine the testing process so that any affected code is tested before moving to production.

10 Who approved the release to production?

Finally, understand who was ultimately responsible for approving the QA release. Development and QA teams should be on the same page regarding readiness for release.

> "As vendors roll out tools integrated with ALF, organizations will benefit from implementing modern life-cycle tools with better information gathering and sharing capability.

These are reasonable questions. Now if only getting the answers was easier. With solid process tools, the answers can be found with a little digging. Questions 1 and 2 can be answered using a requirements gathering tool. Question 3 needs information from both a requirements tool and a testing tool. Question 4 can be answered using a commercial build management tool that provides impact analysis information. For the answers to Questions 5-8, a combination of tools must be used including requirements, configuration management, and build management tools. Question 9 may require knowledge from both an impact analysis build management feature and a test tool. And finally, Question 10 involves a release management tool.

ALF lands to help QA
Some challenges remain, including:

- No single software team can quickly get answers to most of these questions with just one tool – cooperation is required between people and tools
- If teams have them, the necessary life-cycle tools seldom share data or even a common vocabulary
- Expertise in all of these tools is required to retrieve data needed to report on the most basic of development metrics

The Eclipse Application Lifecycle Framework (ALF) project can help. The ALF project, which is in the implementation phase with teams working on vocabulary and service flow definitions, will allow tools that support the application life-cycle process to communicate with one another using Web services transactions via a common communication framework.

ALF defines a *common vocabulary between application life-cycle tools*. This alone will improve the interaction between tools. Tools will communicate via Simple Object Access Protocol (SOAP) transactions over the Eclipse ALF.

ALF also defines *service flows*. An example of a service flow would be Build/Deploy/Test. For example, to answer Question 9, "Based on the impact of the source code changes, what test cases were selected as *critical*?", the build management tool could send a list of the impacted executables to the test tool. The test tool could then determine which test cases must be retested prior to production release based on the list provided by the build management tool impact analysis function.

Teams using ALF might make better use of requirements. Often QA does not have a complete picture of the requirements of a new release. To answer Question 3, "Were the new features reported to QA and were test cases created?", the ALF service flow Requirements Management to Test Management will allow requirement tools to pass requirement information to testing tools. This aids QA in better defining new test cases for new requirements. Getting this information early as soon as the requirement is defined will give QA an immediate notification that new test cases are required.

ALF is independent, but communicates
Developers don't need to use the Eclipse IDE for teams to take advantage of the Eclipse ALF project. ALF is not a development tool, but a life-cycle tool.

Life-cycle tools include requirements gathering, issue tracking, version control, configuration management, build management, testing, and deployment. No single team uses all these tools independently. Organizations break down these responsibilities

into diverse teams, each using tools for their part of the job. These teams must work together, and tools designed to ALF specifications will have the potential to communicate directly as well.

Actively pursuing these types of questions and sharing the information found across the organization helps improve software quality. As vendors roll out tools integrated with ALF, organizations will benefit from implementing modern life-cycle tools with better information gathering and sharing capability.

More information: www.eclipse.org/alf/

Tracy Ragan has served as CEO of Catalyst Systems Corporation since it was founded in 1995. She is an industry leader specializing in version management tools, testing tools, IDEs, and deployment tools. Tracy has been an active member of the Eclipse Foundation since 2002. As CEO of Catalyst, she has worked with large financial, insurance, and embedded systems companies on defining a software life-cycle process that fully incorporates testing. Tracy can be reached at tracy.ragan@openmake.com.

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Customization for the masses

By Jerry Gipper

The perpetual petition

Who hasn't encountered this scenario: A sales or marketing representative approaches the engineering team and laments "The customer loves our product, but …" This usually means the customer wants a specific configuration, I/O payload, memory size, pinout, or other requirement not accommodated in the catalog product. Closing a deal often hinges on how a company responds to these types of requests, as some degree of customization can result in significant additional revenue. Friction between sales/marketing and engineering develops because these requests, regardless of complexity, require considerable effort, resources, costs, and risks, usually at the expense of other planned development projects.

Customization is a fact of life that poses important questions for embedded computing designers. How does a company better position themselves to handle these requests? How can customization become a part of the company's strategic business model? Designers must understand the evolution of designing and manufacturing and the methods of how to accommodate change to succeed in today's market.

Manufacturing shift

Industries evolve as they mature, from food, clothing, transportation, and yes, as hard as it is to believe, even electronics. Fledgling industries start out designing products by hand and manufacturing them in small custom quantities. As the product gains market acceptance, it enters a stage of high volume or mass production. If the product continues to succeed, it may enter a stage of what is commonly called mass customization where each product is produced in mass quantities but with unique characteristics per each buyer's needs.

Examples of this phenomenon appear everywhere. For instance, a century ago, local blacksmiths built automobiles one at a time. Then Henry Ford introduced mass production, and consumers could pick any color they wanted, as long as it

was black. Today's automobiles are mass produced, but with loads of customized elements right off the sales lot. Look around any parking lot and rarely will you find two automobiles with the same set of features.

Shoes underwent this same transition. Custom made by a cobbler, mass produced by shoe manufacturers (remember *Hush Puppy* shoes all you boomers!), and now custom mass produced (Nike lets you pick colors and text for your shoes on their website).

Each industry moves at its own pace of change, sometimes even reverting temporarily when a new technology is introduced before it's ready for mass production. Each industry also has its own degree of required customization and thus its own mass customization requirements. Some products will always be uniquely designed and built, some will always be mass produced, and others will make the leap to mass customization.

The electronics industry is no exception. Microprocessors were originally custom designed for a specific application, primarily funded by a government program. Now, they appear at the tail end of the mass production phase for many product families. New generations are adding the ability to customize circuits while still being built in mass quantities. FPGAs, some of the best-equipped devices for mass customization, are designed in such a way that designers can easily configure them as needed and users can field configure them as application needs change.

Board products are often custom designed per a specific set of program needs. Commercially available boards have only been generally available for the past 15-20 years. Now many manufacturers have standard form factors, interconnects, mezzanines, zero-ohm resistors, or FPGA

capability to allow some degree of customization. Board products allow a variety of mass customization opportunities.

Systems span the whole range of customization. Many are custom made for specific programs, yet desktop or server platforms are mass produced. Customization usually occurs at some intermediate step by a system integrator. Standards make customization easier for system platforms. Many system products have a standard internal bus structure of some type that allows modules to be added. These modules may be storage devices such as hard drives or DVD drives, memory modules, or I/O boards that plug into a PCI bus or PCI Express slot. Dell Computers is all about mass customization.

Embedded software is often custom at the application level but mass produced at the operating systems and middleware layers. Operating systems such as Windows, Linux, and various Real-Time Operating Systems (RTOSs) are prime examples of mass-produced software. Software is also unique in that it can lend a level of customization to mass-produced hardware. Hardware can be reprogrammed to handle different tasks based on application needs. Many processors are general purpose in design, and software customizes it to the application. Signs that software is entering the mass customization phase are starting to show up in the market now.

Unique, just like everyone else

The need to be unique drives customization. While humans thrive on being different, manufacturers depend on high-volume, low-cost manufacturing. Mass customization addresses both of these desires. Items can be produced at high-volume manufacturing economies of scale yet appear to be designed and manufactured uniquely for the buyer. It's a natural phenomenon and part of the

evolution of products that reach high volumes.

Table 1 compares mass production to mass customization. Most embedded applications fit neatly in the mass customization model. Many applications' product development and life cycles are short. Even the exceptions are struggling to keep up with the rest of the industry, which is permeated with short development and life cycles.

Table 2 shows how product and process change can also influence if mass customization is appropriate. Dynamic products in a stable process environment are ideal for mass customization. Often with mass customization process changes must be implemented to accommodate the customization model. Thus an axis forms between dynamic process change/stable product change and stable process change/dynamic product change that makes it easier to transition between these two quadrants.

> **Mass customization represents a lucrative strategic model for gaining market share, expanding into new markets, and closing complex deals with demanding customers.**

	Mass production	Mass customization
Focus	Efficiency through stability and control	Variety and customization through flexibility and quick responsiveness
Goal	Developing, producing, marketing, and delivering goods and services at prices low enough that nearly everyone can afford them	Developing, producing, marketing, and delivering affordable goods and services with enough variety and customization that nearly everyone finds exactly what they want
Key features	• Stable demand • Large, homogeneous markets • Low-cost, consistent quality, standardized goods and services • Long product development cycles • Long product life cycles	• Fragmented demand • Heterogeneous niches • Low-cost, high quality, customized goods and services • Short product development cycles • Short product life cycles

Table 1

	Stable	**Dynamic**
Dynamic	Mass customization	Invention
Stable	Mass production	Continuous improvement

Product change (vertical axis) — Process change (horizontal axis)

Table 2

Mass customization represents a lucrative strategic model for gaining market share, expanding into new markets, and closing complex deals with demanding customers. The associated costs, risks, and resources to reconfiguring products and processes to accommodate a mass customization strategic business model pose a prohibitive barrier to many companies. However, a number of strategies can help overcome this barrier, namely product modularity.

Keeping change under control

A company's ability to handle customization depends on how well they calculate the platform architecture of their product lines. Successful customization requires a solid platform upon which changes can be applied. The platform must be robust enough to handle anticipated changes in a quick and cost-effective manner.

A good product platform has one or more of the following modularity characteristics that make it suitable for customization.

Component sharing: The same component is used across multiple product lines. This type of modularity allows parts to be purchased in mass quantities, but does not truly result in individual customization unless used with other types of modularity. Costs can be better contained if component sharing is enforced across all products, including custom products. Using the same resistor packs, capacitors, memory components, microprocessors, chipsets, connectors, and software routines are all examples of how designers practice component sharing.

Component swapping: Different components are paired with the same basic product, creating as many combinations of products as there are components to swap. The key to success with this type of modularity is to find the most customizable part of the product and separate it into a component that can be easily reintegrated into the product. The component should be highly valuable to the customer, reintegrate easily, and have great variety. Disk drives, memory modules, and mezzanine cards are common examples of component swapping used today.

Cut-to-fit: This type of modularity is more difficult to achieve in typical embedded computing designs, and is more appropriate for cables and similar components that lend themselves to sizing on-the-fly variability. Backplanes offer another example of a type of cut-to-fit modularity.

Mix: Mix modularity combines any of the aforementioned types of modularity to create a new and unique product. This type of modularity is usually based on a *recipe*. Integrated systems use a type of mix modularity when a system is built of various components to an established recipe.

Bus: Standard structures are used to attach different types of components. Standards drive this type of modularity, which is perhaps the most common type of modularity in embedded computing design since its classification is derived from computer terminology. Examples include PCI bus, PCI Express, VMEbus, Ethernet, SCSI, and ATA.

Sectional: Sectional modularity provides the greatest degree of variety and customization, allowing the configuration of different types of components in arbitrary ways as long as each component is connected to another at standard interfaces. FPGAs are a prime example of sectional modularity. Some software components are also more advanced in this type of modularity than most hardware.

Performance and costs can always be optimized at the sacrifice of modularity. Careful tradeoffs must be made to determine the degree of flexibility each product should have. It's always possible to take a low-volume, flexible design and apply performance and cost optimization if the product volumes and life cycles warrant.

Equipped for a snappy comeback

Customization will always be required as long as consumers desire to be unique. Demand and technology improvements will only enable engineering design teams to customize quickly and cost effectively.

Companies must focus on methods of creating custom products. Once methods are determined based on the various types of modularity, individual product production becomes more a matter of automating the production process than manually creating different products. New tools being developed each year make the entire process of mass customization easier for embedded computing designers to manage. Response times will shrink and the amount of variability will increase.

Organizations that realize the value of mass customization typically have a strong platform-based product line with varying degrees of customization available. They have learned to leverage the various types of modularity to gain the greatest advantages, and can quickly respond to the sales team's everlasting plea "The customer loves our product, but …" **ECD**

Easing COTS integration

Curtiss-Wright Controls Embedded Computing (CWCEC) uses a variety of modularity across their various product lines, including mezzanine cards, FPGAs, and configurable I/O. They recently introduced a new initiative that reflects their understanding of and movement to a strategic model supporting customization in the embedded computing industry, a step that could enable them to reach the next level of customization.

CWCEC's Continuum Software Architecture (CSA) helps reduce customers' development, integration, life-cycle maintenance, and support costs. CSA will enhance the ease of Commercial Off-the-Shelf (COTS) integration with Curtiss-Wright's system *building blocks* such as single board computers and mezzanine cards.

CSA delivers a cohesive and comprehensive approach to compatibility and interoperability beyond the traditional hardware interfaces. CSA provides a twofold approach for significantly improving the customer's ability to integrate and evolve with COTS hardware and software. First, it provides the binding elements to facilitate easy integration of a multitude of embedded products. Second, CSA offers a common and comprehensive set of software APIs extending, enabling, and simplifying the full and efficient usage of all available hardware devices.

CSA is the newest element of Curtiss-Wright's innovative COTS Continuum initiative, an R&D initiative to develop a common software, hardware, and mechanical architecture for future Curtiss-Wright products. The architecture will standardize I/O routing and pinouts, electrical interfaces, APIs to all hardware functionality, and provide a common Hardware Abstraction Layer (HAL) and user documentation across Curtiss-Wright products. The net result is a common out-of-box experience between product families and next-generation products.

"The introduction of our Continuum Software Architecture is truly a major leap forward as we realize our goal of developing a common software, hardware, and mechanical architecture for future products," said Lynn Patterson, vice president and general manager of Curtiss-Wright's Modular Solutions group. "CSA delivers a great out-of-box experience common to all our products. This will benefit all of our customers by easing their technology insertion requirements and delivering exceptional performance over a broader range of embedded computing products."

CSA includes:

- Consolidated and configurable firmware
- Intelligent hardware abstraction
- Powerful, intuitive, user-centric, and consistent APIs
- Extensive built-in-test capabilities
- Standard, optimal, and user optional card configurations
- Flexible and efficient compiler and development environment integrations
- Extensible hardware/software component frameworks
- Rich sets of device driver, board support package libraries, and RTOS support
- Complete validations over a broad spectrum of rugged defense and aerospace application areas

In addition, CSA provides backwards-compatible support mechanisms. Developers can leverage and easily support compatibility with legacy software, APIs, systems, and products by accessing shim layers as required.

Similar products, different features

BigLever Software, Inc. has a product exclusively developed to facilitate software mass customization. The centerpiece of the BigLever solution is Gears, a software product line development tool. BigLever also has an innovative software product line methodology that complements Gears.

Gears is designed to accelerate the development of standalone or embedded software for a product line portfolio of similar products with variations in features and functions. Gears is used throughout a development organization – by developers, architects, build engineers, configuration managers, test developers, product managers, and project managers – to engineer their software product line portfolio as though it is a single system rather than a multitude of products.

Gears can be used in any or all stages of the portfolio development life cycle for more effective requirements management, change and configuration management, source code development, software builds, testing, and document development.

BigLever's software product line methodology approach is based on new methods across three primary categories:

- **Software mass customization:** The dichotomy of Domain Engineering (DE) and Application Engineering (AE) in early generation software product line methods introduces dissonance and inefficiency in software development. The software mass customization methodology utilizes abstraction and automation to eliminate application engineering and thereby the negative effects of the DE/AE dichotomy.
- **Minimally invasive transitions:** The amount of cost, time, and effort required for organizations to adopt early-generation software product line methods is disruptive and prohibitive. Minimally invasive transition methods enable rapid adoption of software product line practice with low disruption, low cost, and rapid return on investment.
- **Bounded combinatorics:** Combinatorics in feature models, requirements, architecture, implementation variation points, and test coverage can easily exceed the number of atoms in the universe, which leads to complexity, errors, and poor testability. New methods for bounded combinatorics utilize modularity, hierarchy, encapsulation, abstraction, and constraints to reduce combinatorics from exponential and astronomical to linear and tractable.

Anyone who has to manage multiple product variations such as those from a line of flexible and customizable products can benefit from using Gears for software mass customization.

Design cycles in a flash

New tools enhance simulation and software development of various module combinations before a physical piece of hardware is available for development. These tools enable better hardware decisions and shorten design cycle times because the software team can write and test code to the simulation models. Combining simulation with a good modularity strategy creates a powerful customization solution.

VaST Systems

Several companies are starting to offer practical virtual simulation tools that allow testing and development before final hardware and software development. These tools help speed the development process and enable faster responses to mass customization opportunities.

VaST Systems technology includes an ultrafast, full event wheel, simulation engine, plus specialized peripheral, bus, and processor modeling techniques to achieve high performance in every component of a system on a chip. VaST's CoMET, Meteor, Metrix, and Perhiperal Device Builder provide quick development and exploration environments tightly integrated with the models and the simulator. The combined power of VaST tools and models allows a single-core simulation to achieve up to 200 MIPS, while multicore systems with tiered memory structures, multilevel buses, bus bridges, and peripherals can be simulated at up to 100 MIPS depending on the configuration.

These speeds are fast enough to support real-world tasks, such as booting an RTOS in a matter of seconds. The VaST virtual system prototype can run the same compiled and linked target code as the actual hardware device while accurately representing the system's real-world behavior. Meanwhile, the integrated environment provides real-world synchronization between all of the cores, buses, memories, and peripherals.

Virtutech

Virtutech's product suite Simics can simulate any computer system, from a single board computer to cabinets containing hundreds of microprocessors, allowing software development and test to be completed in a simulated environment. Even production binaries run unchanged so everything right up until the final test of the software on real hardware can be accomplished using the simulated system. Simics is used for developing software for high-performance computing, communications, and aerospace/defense applications.

Virtutech Simics is a family of products optimized to the tasks performed by different engineers. Simics Developer and Simics Hindsight are products for the software developer and quality assurance engineer. Simics Model Builder is a product for engineers building the system models required by Simics Developer. Simics includes Device Modeling Language (DML), which enables anyone to create high-performance device models that can then be combined into models of complete systems. Simics Architect facilitates a much finer-grained examination of the system to examine architectural tradeoffs such as bus widths, cache sizes, or queue depths. Additionally, custom solutions can be developed to perform data analysis or to integrate Simics into nonstandard environments.

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Advanced functional verification and debug of PCI Express-based designs

By Chris Browy

Verification Intellectual Property (VIP) streamlines the path to compliance sign-off through a reusable, layered verification methodology supported by highly configurable and feature-rich transactors, protocol assertions, advanced debug support, and comprehensive functional and compliance checklist test suites. Chris considers the role of VIP for core- and chip-level verification of PCI Express-based designs to ensure robust device-level and interface compliance.

The challenge

Designing with today's high-speed serial interfaces such as PCI Express presents a more significant functional verification challenge than its predecessors, conventional PCI or PCI-X. Systems and peripherals using PCI Express interfaces can take advantage of Generation 1 and Generation 2 transfer rates, differentiated services such as quality of service, access control services, trusted configuration, active state power management, and advanced error reporting. However, these advanced features come at the expense of a more complex interface protocol, application logic, and software driver design.

This has given rise to a strong IP core market for PCI Express. Utilizing PCI Express logic core and PHY core design IP can significantly reduce the complexity of adding PCI Express support to chips and systems. This shifts the burden to the IP supplier for ensuring a rigorous verification of all the various core configurations before being considered trusted in any end-user design. Still, many of the advanced protocol features are substantially controlled through application logic and require custom tests to properly exercise the design functions.

The functional verification of PCI Express logic cores and the chips and systems utilizing them requires significant investment to develop and maintain a layered test bench environment comprised of transactors, assertions, test suites, and debug methods to isolate design bugs in different protocol layers. The test bench should be capable of core-through-chip verification including full control over the Device Under Verification's (DUV's) application logic interface as illustrated in Figure 1. Furthermore, the functional
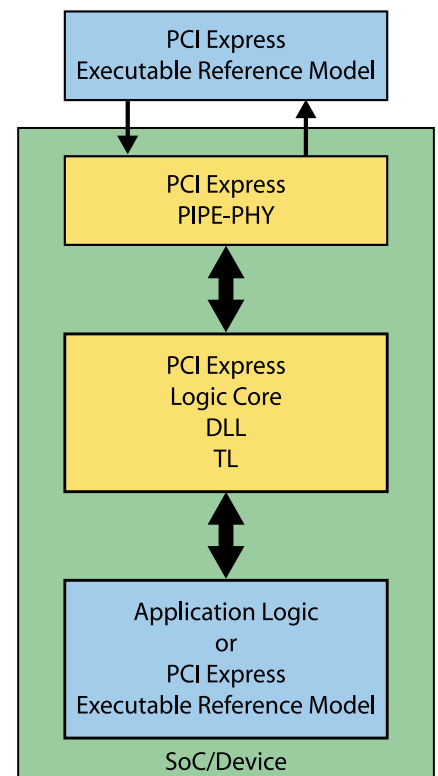
Figure 1

verification environment must constantly evolve to keep up-to-date with the latest specification errata and revisions. For example, since its initial release in 2003, the PCI Express standard has been revised several times, and major enhancements currently in the works signify that more changes will be made.

Verification framework

A designer can choose from the following two options when performing the verification:

1. Develop their own test bench that will have its own inherent risks
2. Utilize an off-the-shelf test suite that has been proven through commercial use to provide the necessary verification coverage

Designers can then execute a comprehensive compliance validation test suite that exceeds basic compliance workshop requirements and supports advanced auto-debugging methods that isolate design bugs more effectively using a reference model and extensive protocol checkers.

A good verification solution should have a set of Executable Reference Models (ERMs) and test suites that simulate the behavior of any type of PCI Express and Advanced Switching (AS) components and links. The ERMs should be developed and presented as behavioral Verilog HDL source code models and augmented with a rich set of protocol assertions to provide the best verification. An ERM is between one to two orders of magnitude more efficient than implementation RTL in simulation.

DUVs should be verified against all realistic system topologies including simple crosslink, multihosted embedded systems, and switch-based topologies. All types of PCI Express Transaction Layer Packets (TLPs) and Data Link Layer Packets (DLLPs) should be generated. Robust controls over ERM operation at all protocol layers and back-end completion generation are needed. Host functions such as advanced PCI BIOS features including enumeration and device capability search must be supported as well as application-level features such as DMA.

The objective of the models is to aid in the functional verification process prior to silicon or board fabrication. A test environment supporting Verilog, VHDL, SystemC, ANSI C/C++, Vera, SystemVerilog, Specman, and other programming environments can provide a native high-level API to interact with behavioral models supporting AS nodes, PCI Express root complexes, endpoints, switches, and PCI-X/PCI 2.3 devices.

A monitoring model that passively monitors and reports AS, PCI Express, and PCI/PCI-X protocol violations; validates end-to-end transactions; and measures and reports transaction trace analysis of devices by link bandwidth, latency, routing, address, and command types utilized helps in the debugging process. A test environment that includes a full suite of compliance test scenarios that verify endpoint, switch, and bridge designs comply fully with the AS, PCI Express, and PCI/PCI-X specifications gives the maximum test coverage.

Compliance tests can be used to assist in the verification of each PCI Express component type and design. Portable tests with parameterized test sequence libraries supporting a rich set of transaction sequences for each of the PCI Express protocol layers and major functions best exercises the DUV. Test sequences are highly directed in nature and represent tens of months of work effort to cover all relevant scenarios. As shown in Figure 2, it is desirable to have test sequences that can be combined under directed or random modes to create a complete set of tests to verify a design against the expansive PCI-SIG compliance checklists. End users typically reuse test sequences to create custom device-level tests that meet their specific test needs.

Bug detection and isolation methods

In response to these challenges, Avery Design Systems developed a complete verification framework for PCI Express that enables creating a highly accurate system model of a DUV in its system context.

An advancement in PCI Express verification over traditional verification methods, Avery's PCI-Xactor coverification has an ERM and innovative auto-debugging methods for bug detection and isolation. Using coverification the DUV and ERM run concurrently, applying the compliance and systems tests to both models. Transaction and sequential consistency is verified using preconfigured design match points, which track transaction flow between protocol layers of the DUV and ERM (see Figure 3). Architectural visible state and transactions are analyzed applying relaxed time, ordering, and content rules defined by the PCI Express protocol to ensure meaningful sequential consistency checking.

> "Coverification is also especially useful in the context of random testing where expected device operation is too complex to predict ...

Test Sequences

PCI-SIG Transaction
Avery Transaction
PCI-SIG Data Link
Avery Data Link
Avery Physical
Avery Power Management
Avery Interrupt
Avery System
PCI-SIG Configuration
Avery Configuration
Avery Isochronous
PCI-SIG Platform
Avery BIOS

Scenario Generator (Directed/Random)

Scenario Parameters

	Assertion	Test Scenario
PHY	√	√
DLL	√	√
TPL	√	√
TXN	√	√
SYS	√	√
PMG	√	√
CFG	√	√
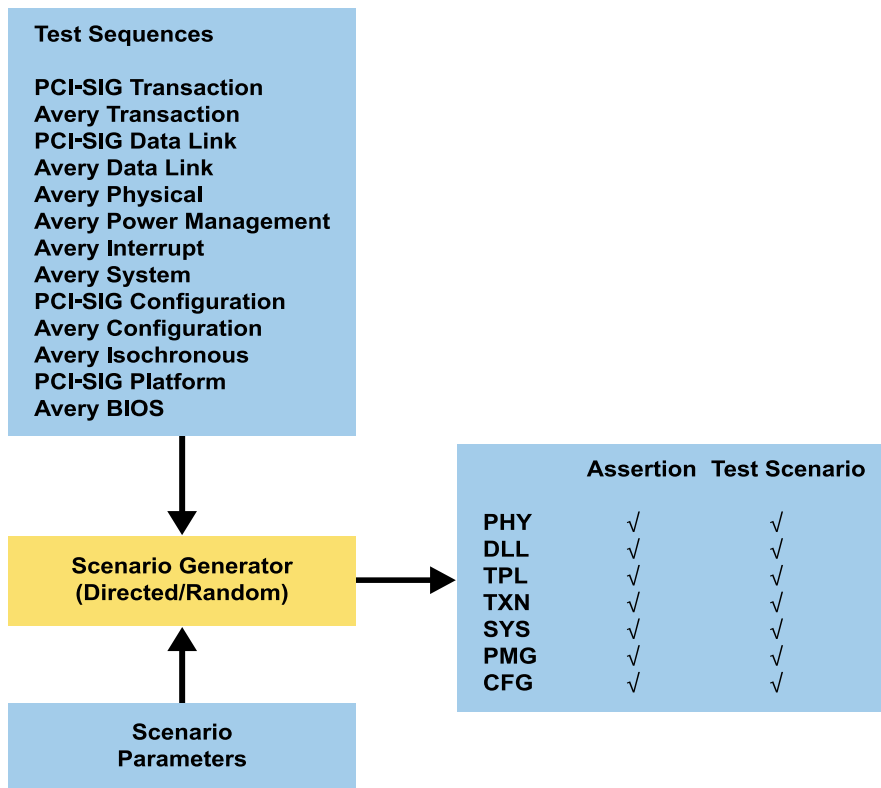
Figure 2

When a mismatch occurs, auto-debugging is then used to perform causal analysis of the implementation model and ERM. Auto-debugging utilizes enhanced behavior traversal and transaction views added to advanced behavioral debugging systems such as Novas' Verdi for better visualization of the behavior of the DUV and shadow ERM. Coverification is also especially useful in the context of random testing where expected device operation is too complex to predict or when assertions are too complex to write. Here, match points verify the architectural state of the models on-the-fly under random input sequences.

Some example of match points include:

- Link Training and Status State Machine (LTSSM) transitions
- Retry buffer entries and replay trigger
- VC flow credits counters
- Configuration and status registers

For example, Avery's design match capability isolated an incorrect LTSSM state transition to lower power state in a multifunction DUV under random test sequences.

Embracing verification

Today, many systems companies and PCI Express logic core IP vendors are using advanced verification frameworks such as PCI-Xactor. Systems companies utilize core-level verification of logic and PHY cores in addition to complete device-level verification. **ECD**

Chris Browy is vice president of sales and marketing of Avery Design Systems. Prior to Avery, he maintained various positions in ASIC design services and product marketing at Cadence Design Systems and worked for other EDA and computer startups. A participant in several standards bodies, Chris holds a BSEE from Rensselaer Polytechnic Institute.

For more information, contact Chris at:

Figure 3

Middleware: The last roadblock to distributed systems development

Both embedded systems and networking are high growth fields; combining them creates a world of opportunities. The list of applications goes on and on, including military systems, telecommunications, factory automation, traffic control, financial trading, medical imaging, building automation, consumer electronics, and more. Each of these industries struggles daily with how to create a single system from many distributed parts.

The information is out there. The network is fast, cheap, and reliable. We could build whole classes of new distributed applications, if we could just get the data. Unfortunately, today, getting the data isn't that simple.

By Dr. Stan Schneider

The last roadblock

So what's holding distributed systems back? Network software architecture has not kept pace with easy-to-use operating systems and network hardware. The fundamental information models built for office and enterprise networks are fine for sharing files and executing transactions, but they simply don't fill the needs of embedded systems. In a real-time network, the main problem is to find and disseminate information quickly to many nodes; that problem is not yet completely solved.

Middleware, a class of software serving distributed applications by delivering data, is a layer between the ubiquitous network *stack* and the user application. The stack provides fundamental access to the network hardware and low-level routing and connection management. The application software, a set of custom-written modules, implements the various parts of the particular system. The middleware delivers data to the application software modules by using the underlying stack. However, finding the right data, knowing where to send it, and delivering it to the right place at the right time is a real challenge.

Embedded system developers, for the most part, have written their own in-house middleware layers. These range from simple, crude stack interfaces to sophisticated connection management and delivery services. They are often efficient, customized implementations that directly map to, or even merge with, the application. But, each one is unique and thus expensive to maintain and slow to adapt. Without a general solution, each application becomes complex, costly, and unreliable.

Recently, general embedded middleware technologies have begun emerging. The pattern follows the classic technological infrastructure evolution path: A few scrappy vendors generalize from custom implementations, gradually building a solution that will work for all. The benefit comes when standards (de facto or not) emerge, allowing industries to concentrate on the next, higher-level problem. Infrastructure software that clearly has adhered to this pattern includes operating systems, compilers, debuggers, network stacks, and so on. Middleware is positioned to be the next major area of standardization.

Generic middleware shows promise for standardized, easy distributed data access. If middleware can deliver on that promise, it has the potential to fuel an explosion in embedded applications that parallels the enterprise growth of IT.

Publish-subscribe networks

The fastest-growing embedded middleware technologies are publish-subscribe architectures. In contrast to the *central server with many clients* model of enterprise middleware, publish-subscribe nodes simply *subscribe* to data they need and *publish* information they produce. Messages pass directly between the communicating nodes. This design mirrors time-critical information delivery systems in everyday life, including television, magazines, and newspapers. Publish-subscribe systems excel at distributing large quantities of time-critical information quickly, even in the presence of unreliable delivery mechanisms.

BIOS, firmware, middleware

Publish-subscribe architectures map well to the embedded communications problem. Finding and sending the right data is straightforward; nodes just request what they want and the system delivers it. Sending the data at the right time is also natural; publishers simply send data whenever new information is available. Publish-subscribe is efficient because the data flows directly from sender to receiver without intermediate servers. Multiple senders and receivers are easily supported, making redundancy and fault tolerance natural. Finally, and perhaps most importantly, each publisher-subscriber pair can establish independent Quality of Service (QoS) agreements. Thus, publish-subscribe designs can support extremely complex, flexible dataflow requirements. Publish-subscribe networks deliver the right data to the right place at the right time.

Emerging standards

Publish-subscribe designs are not new. Custom, in-house publish-subscribe layers abound. Industrial automation *fieldbus* networks have used publish-subscribe designs for decades. Commercial middleware products today control ships, digital television systems, large traffic grids, flight simulators, military systems, and thousands of other real-world applications. The technology is proven and reliable.

What is new is that standards are evolving. The Object Management Group (OMG), the standards body responsible for technologies like CORBA and UML, recently recognized the importance of publish-subscribe architectures. The newly adopted OMG standard, Data

> Embedded middleware is crossing the threshold from specialized point solution to widely adopted infrastructure.

Distribution Service (DDS), is the first open international standard directly addressing publish-subscribe middleware for embedded systems. DDS, outlined in Figure 1, features extensive, fine control of QoS parameters, including reliability, bandwidth control, delivery deadlines, and resource limits. Several industry groups are rallying around DDS; for example, the U.S. Navy's Open Architecture specification stipulates DDS for all future Navy platforms. DDS represents the combined experience of many applications, and could be an important technology milestone.

Of course, many difficult problems remain in middleware. For instance, complex systems require merged data distribution and client-server services. Guaranteed bandwidth reservations and prioritized message

delivery is not yet available. Highly intermittent transports, such as wireless networks, must be supported. Scalability to large networks with thousands or millions of nodes presents an unsolved challenge.

Nonetheless, embedded middleware is crossing the threshold from specialized point solution to widely adopted infrastructure. When it completes that transition, the technology could render bold new distributed systems with much greater capabilities than are practical today. **ECD**

More information:
www.omg.org/news/whitepapers/
IsDDS4U.pdf

Dr. Stan Schneider is CEO of Real-Time Innovations, Inc., a leader in software infrastructure and tools for embedded systems.

Immediately before RTI, Stan was an independent technical and management consultant, working with companies in medical products, digital signal processing, aerospace, semiconductor manufacturing, video and television, and networking. Before that, Stan managed one of the largest laboratories at Stanford University, focusing on intelligent mechanical systems. At Sperry Computer Systems (now Unisys), Stan developed networked communications systems and led the software team responsible for Sperry's personal computer product line. Stan began his career building data acquisition systems for automotive impact testing.

Stan holds a PhD in Electrical Engineering and Computer Science from Stanford, an MS in Computer Engineering, and a BS in Applied Mathematics.

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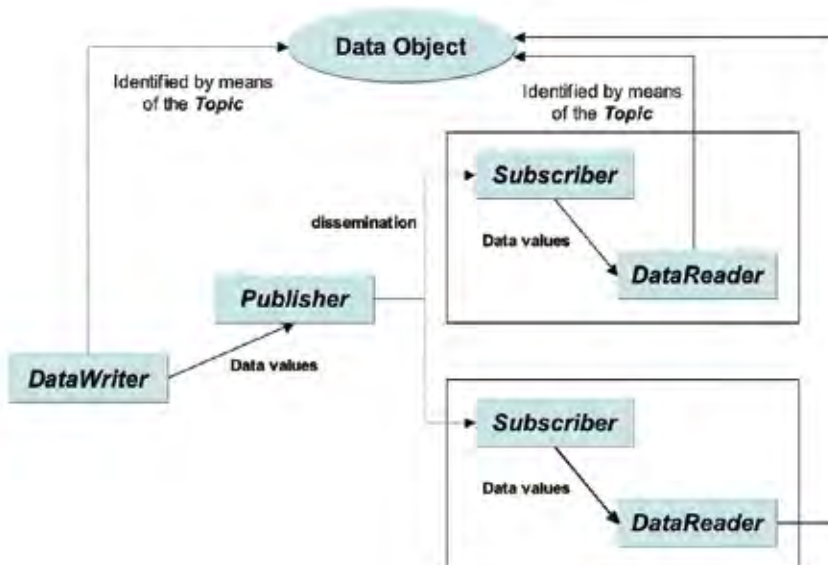
Figure 1

Ardence, Inc.

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RTX

By operating in kernel mode (Ring 0), RTX is the highest performing deterministic extension for Windows 2000, XP Pro, XPe, and Server 2003. RTX is the only hard real-time solution to support multiprocessor, multicore, and mobile platforms. Based on the Win32 API, RTX utilizes Microsoft's development and debugging tools to reduce system cost and speed time to market. RTX now supports host/target debugging with Visual Studio 2005 and .NET 2003. It also enables debugging an RTSS application on target hardware (running with an RTX runtime but not an SDK). RTX is proven in thousands of demanding applications in industries such as: industrial automation, military/aerospace, medical devices, test and measurement, and robotics.

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Accelerating test automation for high-tech equipment

With rising product complexity and global competitive pressure to shorten product release cycles, QA organizations are struggling to do more in a shorter amount of time with the same or fewer resources. Tools are needed to break the QA backlog by radically simplifying and accelerating test automation. With FanfareSVT, testing activities that used to take weeks or months can now be performed in hours or minutes at the push of a button.

FanfareSVT is the first commercially developed test automation software for validating high-tech equipment functionality. Test cases are easily reused and ported to new devices, freeing up QA teams to focus on increasing test coverage and improving time to market. FanfareSVT is built specifically for functional, stress, and load testing equipment and systems accessed through command line interfaces, embedded Web interfaces, and any device that can be controlled through Tcl. FanfareSVT easily integrates with existing in-house QA systems including regression testing infrastructures, commercial test equipment, and bug tracking systems.
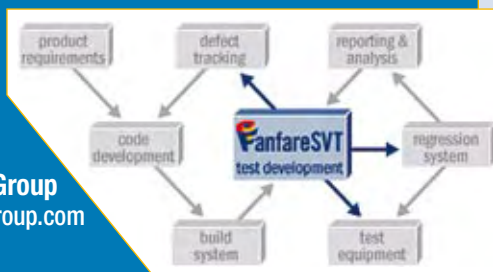
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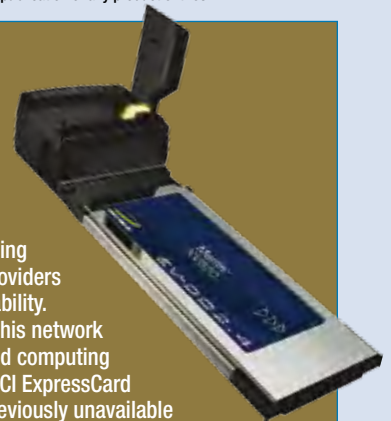
EV-DO data networks are becoming common as wireless network providers improve their data network capability. Adding the ability to connect to this network in existing laptops and embedded computing devices already equipped with PCI ExpressCard support gives them access to previously unavailable high-speed data networks.

Novatel Wireless' new Merlin ExpressCard XV620 ExpressCard products address an urgent need in the mobile computing market. The ExpressCard standard is the next generation of PC card technology that allows notebook computer users to add new hardware capabilities. This ExpressCard is the first PCI ExpressCard/34 solution available on the market that incorporates EV-DO technology (backward compatible with CDMA legacy technology) offering Internet connection speeds up to 2.4 Mbps.

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(M) MOTOROLA

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Altera Corporation

101 Innovation Drive • San Jose, CA 95134
Tel: 408-544-7000 • Fax: 408-544-6411
www.altera.com

Nios II Dev. Kit, Cyclone II Edition

Altera® Cyclone® II FPGAs are optimized for low cost, extending the reach of FPGAs further into cost-sensitive, high-volume applications and continuing the success of the first-generation Cyclone device family. Cyclone II FPGAs offer a customer-defined feature set, industry-leading performance, and low power consumption. They also offer greatly increased density and more features, all at significantly lower cost. Featuring up to 150 embedded 18 x 18 multipliers, Cyclone II FPGAs can be used alone or as Digital Signal Processing (DSP) coprocessors to improve price-to-performance ratios for DSP applications, including video and image processing, communications systems, and common DSP functions.

The Nios® II Development Kit, Cyclone II Edition, offers a variety of Intellectual Property (IP) cores to speed development, including three Nios II 32-bit RISC processors. The Nios II processors – fast, standard, and economy – are each optimized for a specific price and performance range, allowing designers to choose a system configuration that is an exact fit for their embedded needs. All three processors use the same instruction set architecture and are 100 percent binary code compatible. Nios II processors can be added to a designer's system using the SOPC Builder system development tool in the Quartus® II development software. This kit includes 12 months of upgrades so you can keep your system up-to-date with the latest enhancements to the Nios II processor, peripherals, and system design tools. This development kit is now RoHS-compliant.

Visit www.altera.com/nios for more information.

FEATURES:

- Complete embedded FPGA development environment featuring the versatile Nios II embedded processor and the low-cost Cyclone II family
- Embedded software development tools:
  - Nios II Integrated Development Environment (IDE) and debugger, Nios II Instruction Set Simulator (ISS)
  - GNU tool chain, MicroC/OS-II RTOS, and LightweightIP TCP/IP stack software
- Hardware design tools, including the Quartus II design software with the SOPC Builder system development tool
- Library of standard embedded IP cores, including:
  - Three Nios II 32-bit RISC CPU cores (fast, standard, economy)
  - DDR SRAM controller, timer, UART, SPI, JTAG UART, GPIO, DMA, Ethernet interface, interface-to-user logic, custom instruction, and more
- Complete embedded development board featuring:
  - Cyclone II EP2C35 FPGA and 10/100 Ethernet PHY/MAC
  - 1 MB SSRAM, 16 MB DDR SDRAM, 16 MB flash, JTAG connectors for FPGA and CPLD, Mictor trace/debug connector, 32-bit PMC headers
- No license or royalty fees when developing with the Nios II processor in Altera FPGAs and HardCopy® series structured ASICs

Altera Corporation

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Nios II Dev. Kit, Stratix II Edition

Altera® 90 nm Stratix® II devices are the industry's biggest and fastest FPGAs and feature an innovative logic structure that packs more functionality into less area to dramatically reduce device costs. With internal clock frequency rates up to 500 MHz and typical performance > 250 MHz, these devices deliver on average 50 percent faster performance and more than twice the logic capacity than first-generation Stratix FPGAs. Stratix II FPGAs deliver 50 times higher multiplier bandwidth than single-chip, standalone Digital Signal Processors (DSPs). The DSP blocks have the flexibility and performance to implement fast, arithmetic-intensive applications such as image processing, wireless communications, military, broadcast, and medical. Each DSP block has dedicated multiwidth multipliers to implement DSP algorithms and functions, including filtering, video and image processing, correlation, transforms, encryption, and error correction.

The Nios II Development Kit, Stratix II Edition, offers a variety of Intellectual Property (IP) cores to speed development, including three Nios® II 32-bit RISC processors. The Nios II processors – fast, standard, and economy – are each optimized for a specific price and performance range, allowing designers to choose a system configuration that is an exact fit for their embedded needs. All three processors use the same instruction set architecture and are 100 percent binary code compatible. Nios II processors can be added to a designer's system using the SOPC Builder system development tool in the Quartus® II development software. This kit includes 12 months of upgrades so you can keep your system up-to-date with the latest enhancements to the Nios II processor, peripherals, and system design tools. This development kit is now RoHS-compliant.

See www.altera.com/nios for more information.

FEATURES:

- Complete embedded development environment featuring the Nios II embedded processor and high-density, high-performance Stratix II FPGAs
- Embedded software development tools, including:
  - Nios II Integrated Development Environment (IDE) and debugger, and the Nios II Instruction Set Simulator (ISS)
  - GNU tool chain, MicroC/OS-II RTOS, and LightweightIP TCP/IP stack software
- Hardware design tools, including the Quartus II design software, with the SOPC Builder system development tool
- Library of standard embedded IP cores, including:
  - Three Nios II 32-bit RISC CPU cores (fast, standard, economy)
  - DDR SRAM controller, timer, UART, SPI, JTAG UART, GPIO, DMA, Ethernet interface, interface-to-user logic, custom instruction, and more
- Complete embedded development board featuring:
  - Stratix II EP2S60 FPGA and 10/100 Ethernet PHY/MAC
  - 1 MB SSRAM, 16 MB DDR SDRAM, 16 MB flash, JTAG connectors for FPGA and CPLD, Mictor trace/debug connector, 32-bit PMC headers
- No license or royalty fees when developing with the Nios II processor in Altera FPGAs and HardCopy® series structured ASICs

AMIRIX Systems Inc.

77 Chain Lake Drive • Halifax, NS B3S 1E1 Canada
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www.amirix.com/products

AMIRIX FPGA Boards

The AP100 and AP1000 PCI platform FPGA development boards are PCI cards with a Xilinx Virtex-II Pro!™ FPGA that provide an instant, out-of-box system for developing embedded FPGA System-on-Chip (SoC) solutions. The boards come configured as a single board computer with monitor software and Linux OS and also provide an advanced design starting point to improve time to market and reduce development costs. Additional platform modules and accessories are available to support the development of programmable systems.

FEATURES:

- Devices supported: XC2VP7, XC2VP20, XC2VP30, XC2VP70, XC2VP100
- Memory: DDR SDRAM, SRAM, program flash, configuration flash, SystemACE with CompactFlash
- Networking: 10/100 Ethernet controller, 10/100/1000 BASE-T Ethernet, RS-232D serial ports, MGT with SMA, SFP
- MGT support for up to four InfiniBand-style connectors
- 32/64-bit, 33/66 MHz, PCI Rev 2.2 add-in card via standard PCI bridge devices
- IEEE-P1386.1 32-bit/66 MHz PMC slot allowing third-party I/O cards; expansion for up to 223 general purpose I/O

For more information, contact: request.info@amirix.com

RSC# 24301 @ www.embedded-computing.com/rsc

Arcobel Embedded Solutions

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Arcobel

Arcobel Embedded Solutions supplies a variety of specialized boards, systems, and solutions. Our highly trained staff and the experience they have in innovative industrial electronics have given us the tools we proudly share with our partners.

Arcobel Embedded Solutions distributes, integrates, and helps develop real-time, high-performance computers for applications in industry, research, defense, aerospace, medical, and telecom. We give advice, select products, integrate these products into systems loaded with software, and provide full test reports. Our customers have access to our high-level technical support.

FEATURES:

- Design services for ASIC and FPGA development
- Official training center for Synplicity in the Benelux
- Since July 2006, official partner for FPGA training(s) for Doulos in the Benelux
- Hardware supplier for VME, CompactPCI, PCI, SBC, Mini-ITX, and all other form factors

For more information, contact: allard.van.veelen@arcobel.nl

RSC# 31389 @ www.embedded-computing.com/rsc

FPGAs, reconfigurable computing

Annapolis Micro Systems, Inc.

190 Admiral Cochrane Drive, Suite 130 • Annapolis, MD 21401
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www.annapmicro.com

Dual 1.5 GHz A/D

Annapolis Micro Systems is a world leader in high-performance, COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, DSP, FFTs, communications, Software-Defined Radio, encryption, image processing, prototyping, text processing, and other processing intensive applications. The Annapolis Dual 1.5 GHz A/D I/O card provides two channels of 1.5 GSps input (with 8-bit resolution) or one channel of 3.0 GSps input (with 8-bit resolution). The board has two Max108 8-bit ADCs, each one fed by its own pair of differential signals. The differential clock signals coming into the board can provide identical clocks to both A/Ds for dual 1.5 GSps channels or an inverted clock to one of the A/Ds to interleave the data for a single 3.0 GSps channel. Multiple I/O cards can be synched together via the Annapolis Clock Sync Distribution Board, as in the 24 GSps A/D Collection, Processing, and Distribution (CPD) systems.

The Xilinx Virtex-II Pro 70 on the board provides user-configurable, real-time continuous sustained processing of the full data stream. Up to two of these I/O cards can reside on the Annapolis WILDSTAR II or WILDSTAR II Pro FPGA-based VME and PCI bus boards, which provide up to 30 million more user-reprogrammable FPGA gates for onboard processing.

Our boards run on many different operating systems. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models. VHDL source is provided for interfaces to SRAM, LAD bus, I/O bus, and DACs. CoreFire users will have the usual CoreFire board support package. Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customers' applications succeed. We offer training and exceptional special application development support, as well as more conventional support.

FEATURES:

■ Two MAX 108 8-bit A/D converters – two 1.5 GSps channels or one 3 GSps channel

■ Two sets of differential or single-ended input signals – one for each A/D

■ Differential or single-ended clock input – synchronize or interleave the two data streams

■ Up to 4 GBps I/O bandwidth to WILDSTAR II Pro motherboard I/O slot

■ Xilinx Virtex-II Pro XC2V70 FPGA for user-reprogrammable processing with CoreFire

■ Heat sink on A/Ds; heat sink/fan in PCI chassis

■ Host software: Win NT, 2000, XP, Linux, VxWorks, Solaris, DECAlpha, and SGI

■ Full CoreFire board support package for fast, easy application development

■ VHDL model, including source code for board level interfaces and ChipScope access

■ Save time and effort and reduce risk with COTS boards and software

■ Achieve world-class performance – WILD solutions outperform the competition

■ Includes one-year hardware warranty, software updates, and customer support; training available

Annapolis Micro Systems, Inc.
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Dual 2.3 GSps DAC

Annapolis Micro Systems, Inc. is a world leader in high-performance COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, digital signal processing, FFTs, communications, software radio, encryption, image processing, prototyping, text processing, and other processing intensive applications.

The Annapolis Dual 2.3 GSps DAC I/O card provides two 12-bit output streams at up to 2.3 GSps per stream.

The board has both a high-precision trigger for inner-board or board-to-board synchronization and a low-precision trigger. The card supports three modes: NRZ, RF, and RZ.

The Xilinx Virtex-II Pro 70 on the board provides user-configurable, real-time continuous sustained processing of the full data stream. Up to two of these I/O cards can reside on the Annapolis WILDSTAR II or WILDSTAR II Pro FPGA-based VME and PCI bus boards, which provide up to 30 million user-reprogrammable FPGA gates for onboard processing. Our boards run on many different operating systems. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models. A VHDL source is provided for interfaces to SRAM, LAD bus, I/O bus, and DACs. CoreFire users will have the usual CoreFire board support package.

Develop applications with CoreFire (more than 1,000 cores), which transforms the FPGA development process, making it possible for theoreticians to easily and quickly build and test their algorithms on the real hardware that will be used in the field. The combination of our COTS hardware and CoreFire enables our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customers' applications succeed. We offer training and exceptional special application development support, as well as more conventional customer support.

FEATURES:

- Choice of up to 2.3 GSps or 1.5 GSps output per channel
- Two individually configurable output streams of 12-bit data
- High output power and exceptional gain
- Flatness in multiple Nyquist zones
- One Xilinx Virtex-II Pro 70-5, -6, or -7
- Up to 1 GB DDR SDRAM in four banks
- Supports three modes: NRZ, RF, and RZ
- Both high-precision and low-precision triggers
- JTAG and serial port access
- Proactive thermal management system
- Available in both commercial and industrial temperature grades
- Includes one-year hardware warranty, software updates, and customer support

Annapolis Micro Systems, Inc.

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WILDSTAR 4 for PCI

Annapolis Micro Systems is a world leader in high-performance, COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, DSP, FFTs, communications, Software-Defined Radio, encryption, image processing, prototyping, text processing, and other processing intensive applications. Our 10th-generation WILDSTAR 4 for PCI-X uses Xilinx's newest Virtex-4 FPGAs for state-of-the-art performance. It accepts one I/O card in one, or up to two I/O cards in two, PCI-X slots, including single 1.5 GHz 8-bit ADC, quad 250 MHz 12-bit ADC, dual 2.3/1.5 GSps 12-bit DAC, Universal 3 Gbit serial I/O (Rocket I/O, 10 GbE, InfiniBand), and Tri XFP (10 GbE, 10G FC). Our boards work on a number of operating systems, including Windows, Linux, ALTIX, and VxWorks. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models.

Develop your application quickly with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily build and test their algorithms on the real hardware that will be used in the field. CoreFire, based on dataflow, automatically generates distributed control fabric between cores.

Our extensive IP and board support libraries contain more than 1,000 cores, including floating point and the world's fastest FFT. CoreFire uses a graphical user interface for design entry, supports hardware-in-the-loop debugging, and provides proven, reusable, high-performance IP modules. WILDSTAR 4 for PCI-X, with its associated I/O cards, provides extremely high overall throughput and processing performance. The combination of our COTS hardware and CoreFire allows our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customers' applications succeed. We offer training and exceptional special application development support, as well as more conventional support.

FEATURES:

- Four Virtex-4 FPGA processing elements – One XC2VP70, XC2VP100, XC4VFX100, or XC4VFX140, and three XC4VSX55 or XC4VLX40 – 100

- Up to 3.5 GB DDR2 DRAM in 14 Banks or up to 96 MB DDRII or QDRII SRAM

- PCI or PCI-X bus – 133 MHz

- High-speed DMA multichannel PCI controller

- Programmable flash for each FPGA to store FPGA images and for PCI controller

- Auxiliary connector for additional power

- Full CoreFire board support package for fast, easy application development

- VHDL model, including source code for hardware interfaces and ChipScope access

- Available in both commercial and industrial temperature grades

- Proactive thermal management system – board-level current measurement and FPGA temperature monitor accessible through host API

- Save time, effort, reduce risk with COTS boards and software. Achieve world-class performance – WILD solutions outperform the competition

- Includes one-year hardware warranty, software updates, and customer support; training available

For more information, contact: jdonald@annapmicro.com   **RSC# 31247 @ www.embedded-computing.com/rsc**

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WILDSTAR II Pro VME

Annapolis Micro Systems is a world leader in high-performance, COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, DSP, FFTs, communications, Software-Defined Radio, encryption, image processing, prototyping, text processing, and other processing intensive applications. Our ninth-generation WILDSTAR II Pro for VME uses Xilinx's newest Virtex-II Pro FPGAs for state-of-the-art performance. It accepts up to two I/O cards in one VME slot, including Dual 1.5 GHz A/D, Dual 1.5 GSps D/A, Quad 105 MHz, Universal 3 Gb (Rocket I/O, 10 GbE, InfiniBand), Quad FC2, Quad GbE, and LVDS. Our boards work on a number of operating systems, including Win NT, 2000, XT, Linux, Solaris, IRIX, ALTIX, and VxWorks.

We support our board products with a standardized set of drivers, APIs, and VHDL simulation models. Develop your application very quickly with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily build and test their algorithms on the real hardware that will be used in the field. CoreFire, based on dataflow, automatically generates distributed control fabric between cores. Our extensive IP and board support libraries contain more than 1,000 cores, including floating point and the world's fastest FFT. CoreFire uses a graphical user interface for design entry, supports hardware-in-the-loop debugging, and provides proven reusable, high-performance IP modules.

WILDSTAR II Pro for VME, with its associated I/O cards, provides extremely high overall throughput and processing performance. The combination of our COTS hardware and CoreFire allows our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

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FEATURES:

- One to three Virtex-II Pro Xilinx FPGA processing elements – XC2VP70 or XC2VP100
- Up to 144 MB DDRII or QDRII SRAM
- Up to 768 MB DDR SDRAM
- Programmable flash for each processing element to store FPGA images
- Works with VME64x backplane
- High-speed multichannel DMA controller
- Host software: Win NT, 2000, XP, Linux, VxWorks
- Full CoreFire board support package for fast, easy application development
- VHDL model, including source code for hardware interfaces and ChipScope access
- Save time and effort and reduce risk with COTS boards and software
- Achieve world-class performance – WILD solutions outperform the competition
- Includes one-year hardware warranty, software updates, and customer support; training available

ChipX, Inc.

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CX Structured ASIC

ChipX, Inc. is a leader in the development of Structured ASIC products and technology. Using our patented technology, ChipX provides the widest range of Structured ASICs in the market today, backed by a track record of more than 1,500 Structured ASIC designs completed and in production. ChipX Structured ASICs offer high speed and low power, without the long manufacturing times or risks associated with traditional ASICs. Whether your design is small or large, your volume is low or high, ChipX offers a fast, low-risk path to production silicon.

The CX6000 family is based on UMC's 0.13µ high-speed process. The CX6100 embeds a complete PCI Express subsystem, and the CX6200 integrates a USB 2.0 OTG PHY. ChipX PCI Express PHY IP is silicon proven with PCI-SIG certification, and our USB 2.0 OTG PHY is certified with the USB-IF. Using our hard PHY IP in combination with our efficient gate fabric and memory architecture allows you to build System-on-Chip (SOC) and SideChip™ solutions in record time. Use the CX6000 product to add new functions to your existing system, or be the first to build solutions when new opportunities emerge.

A Standard-Cell ASIC may allow you to integrate a complete subsystem with your application, but large resources will be tied up locating IP, negotiating contracts, integrating third-party IP, and dealing with the complexities of troubleshooting multiple vendors' IP. With ChipX, we've taken care of the connectivity subsystem for you. Our silicon proven PHYs are already integrated and tested. By using our PHY development boards, you will use the same trusted PHY through your entire development from prototyping through production.

ChipX offers five Structured ASIC families with more than 50 individual targeted slices. Each Structured ASIC family support the requirements of industrial, consumer, medical, or military/aerospace (ITAR compliant) applications. With a wide range of targeted slices covering gates, memory, and hard IP cells such as PCI Express, USB 2.0 OTG, and DDR/DDRII PHY, ChipX Structured ASICs are ideal for migrating quickly from prototypes to volume production.

FEATURES:

- Up to 250 MHz maximum global operating frequency
- Core operating voltages of 1.2 V, 1.8 V, 2.5 V, 3.3 V, and 5 V
- Highly configurable I/Os support LVTTL, LVCMOS, HSTL, SSTL (18/2/3), 840 Mbps LVDS, LVPECL, RSDS, PCI, PCI-X, XOSC, and double data rate
- Output drive strengths of up to 16 mA
- Low-jitter PLLs with output frequency range of 10 MHz-1 GHz
- Synthesizable DLLs with output frequency of up to 500 MHz
- PCI Express PHY (one to eight lanes)
- USB 2.0 OTG PHY
- DDR/DDRII support
- PCI Express Development Kit
- Migration of FPGAs into ASICs
- USB2.0 T&MT Board Evaluation Kit

For more information, contact: moreinfo@chipx.com

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Emerson Network Power, Embedded Computing

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www.artesyncp.com

Pm8540

For customers in the wireless and convergence market who need a cost-effective and high-performance control subsystem, the Pm8540 provides a highly integrated processor and I/O to meet their system and blade control requirements. The Pm8540 is designed for hardened telecom applications with Carrier Grade Linux support and long service life of 15 years. A modular processor subsystem also lowers your lifetime cost of ownership by providing an easy upgrade path and protecting you from obsolescence issues. The module can be used in both ProcessorPMC monarch and nonmonarch modes, acting as the host for the local PCI bus or as a peripheral on the local PCI bus, depending on the application or baseboard.

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Formerly Artesyn Technologies

FEATURES:

■ VITA 32 ProcessorPMC

■ Freescale 8540 PowerQUICC III integrated processor

■ 256 or 512 MB DDR DRAM

■ 32 MB flash

■ 16 MB persistent memory

■ Dual 10/100/1000 Ethernet ports with P14 access

For more information, contact: info@artesyncp.com   RSC# 23098 @ www.embedded-computing.com/rsc

Emerson Network Power, Embedded Computing

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www.artesyncp.com

Pm8560

The Pm8560 is a Processor PCI Mezzanine Card (ProcessorPMC) module with up to eight E1/T1/J1 interfaces.

The Pm8560 is ideal for 3G (UTMS and W-CDMA) and 2.5 G (GPRS) data and signaling applications. The module is capable of supporting a wide variety of protocols including SS7 and SIGTRAN. Other applications include signaling gateways and soft switches as a signaling interface card.

The Pm8560 includes a Reduced Media-Independent Interface (RMII) on Pn3 for Ethernet PHYs and management interface.

Physical connectivity of E1/T1/J1 spans the Pm8560 via Rear Transition Modules (RTMs) that interface from either 2.16/cPSB blades or AdvancedTCA blades such as Emerson's Katana product line.

EMERSON.
Network Power

Formerly Artesyn Technologies

FEATURES:

■ Processor PMC (VITA 32-2003) with up to eight software selectable E1/T1/J1 interfaces

■ Freescale Semiconductor MPC8560 PowerQUICC III communication processor

■ Up to 512 MB DDR SDRAM with ECC

■ Up to 32 MB flash

■ PCI bus operation of 32-bit/66 MHz

■ 10/100/1000 Ethernet port

For more information, contact: info@artesyncp.com   RSC# 22783 @ www.embedded-computing.com/rsc

Emerson Network Power, Embedded Computing

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PmPPC7447

Artesyn's PmPPC7447 is a complete processor subsystem in a very compact, industry standard form factor. It is designed to allow communication equipment manufacturers to add modular and upgradeable functionality to their I/O baseboard.

The module can be used in both Processor PMC monarch and nonmonarch modes, acting as the host for the local PCI bus or as a peripheral on the local PCI bus, depending on the application or baseboard. The SDRAM memory is contained in a SODIMM package, the same memory package widely used in laptop computers so you can take advantage of the rapidly advancing memory capacity.

FEATURES:

■ 1 GHz PowerPC® MPC7447A processor
■ Up to 2 GB SDRAM in SODIMM packaging
■ Marvell Discovery III system controller
■ Dual 10/100/1000 Ethernet with P14 access
■ 10/100 Ethernet on front bezel
■ I2C and four GPIO ports with P14 access

For more information, contact: info@artesyncp.com   RSC# 30605 @ www.embedded-computing.com/rsc

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Emerson Network Power, Embedded Computing

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www.artesyncp.com

PmPPC7448

Artesyn's PmPPC7448 is a complete processor subsystem in a very compact, industry standard form factor.

Considerable engineering effort has gone into ensuring maximum flexibility on the PmPPC7448. The module can be used in both Processor PMC monarch and nonmonarch modes, acting as the host for the local PCI bus or as a peripheral on the local PCI bus, depending on the application or baseboard. The SDRAM memory is contained in a SODIMM package, the same memory package widely used in laptop computers so you can take advantage of the rapidly advancing memory capacity.

FEATURES:

■ Up to 1.4 GHz PowerPC® MPC7448 processor
■ Up to 2 GB SDRAM in SODIMM packaging
■ Marvell Discovery III system controller
■ Dual 10/100/1000 Ethernet with P14 access
■ 10/100 Ethernet on front bezel
■ I2C and 4 GPIO ports with P14 access

For more information, contact: info@artesyncp.com   RSC# 22181 @ www.embedded-computing.com/rsc

Global IP Sound

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www.globalipsound.com

GLOBAL IP SOUND

VoiceEngine

GIPS VoiceEngine Embedded is an extension to the world-renowned GIPS VoiceEngine product family. Building on the success of VoiceEngine, Global IP Sound has created an embedded solution that meets the highest requirements of today's voice processing solutions. GIPS VoiceEngine Embedded is designed for use in CPU-based VoIP equipment such as hardware IP phones or residential gateways – often referred to as TAs (Terminal Adaptors) or IADs (Integrated Access Devices). It provides manufacturers with a solution that solves all of the complex voice processing functions in one integral piece of software that guarantees the best voice quality with the lowest possible delay and takes full advantage of Global IP Sound's patented technology and expertise.
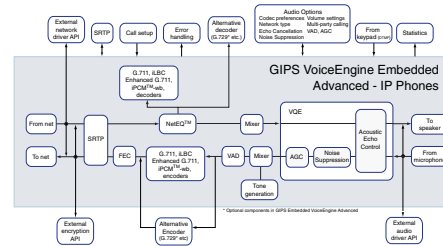
FEATURES:

- Same high-level API on all platforms to facilitate easy integration and rapid time to market
- Low latency and high packet loss robustness with GIPS jitter buffer/PLC module (NetEQ) and GIPS codecs
- Complex speech enhancements such as echo cancellation, noise suppression, and automatic gain control
- Compatible with any call setup protocol, such as SIP and H.323
- Advanced telephony features such as call progress tone generation and caller ID generation
- Support for multiple hardware and OS platforms

For more information, contact: info@globalipsound.com   RSC# 24323 @ www.embedded-computing.com/rsc

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Hunt Engineering

Chestnut Court, Burton Row • Brent Knoll, Somerset, TA9 4BP
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www.hunt-rtg.com

FPGA/DSP Systems

Ready-for-use affordable, high-performance, reconfigurable, real-time FPGA/DSP systems – USB connected or used embedded/standalone.

Hunt Engineering RTG systems allow you to implement your FPGA design quickly and efficiently. Each system includes example projects to use as an instant starting point to create your design. VHDL accessing hardware features with guaranteed timings and protocols are provided. Systems connect to your PC using Hi-Speed USB with data exchange at up to 40 MBps. Device drivers and APIs for your PC are supplied together with examples to show you how to develop a C or C++ application on your PC to interact with the system. PCI format also available, see www.hunteng.co.uk. All systems can be used standalone/embedded.

FEATURES:

- User programmable Xilinx FPGA/TI DSP hardware of choice; FPGA can be configured via USB, JTAG cable, or PROM
- Also included: 128/256 MB DDR SDRAM, digital I/Os, fast A/Ds and D/As according to individual system specs
- Hi-Speed USB connection to host PC; can be used standalone for embedded systems; PCI format also available
- Host API support for Windows 2000/XP/Linux; FPGA/DSP loading/resetting/data exchange via simple s/w interface
- USB cable, I/O cables to interface to peripherals, mains power supply unit plus full documentation included
- Systems can be used for suggested application or one of the developer's choice; can also be expanded later

For more information, contact: sales@hunteng.co.uk   RSC# 30766 @ www.embedded-computing.com/rsc

ICS Sensor Processing

296-300 Concord Road, Corporate Center, Suite 120
Billerica, MA 01821
Tel: 703-263-1483/800-368-2738 (Toll Free) • Fax: 703-263-1486
www.ics-ltd.com

ICS-8550

Designed to bring more bandwidth and processing power to Software-Defined Radio (SDR) applications, the ICS-8550 XMC module features two analog inputs equipped with AD9430 210 MHz, 12-bit ADCs, and a Xilinx Virtex-4 XC4VFX60 FPGA. This card has been optimized for wide bandwidth front-end digital signal processing associated with digital receiver applications common to spectrum monitoring, signal intelligence, communications, and radar systems.

Five levels of ruggedization are available from commercial air-cooled to conduction-cooled. Careful selection of components and thermal management techniques allows intensive DSP functionality to be maintained at sample rates up to 210 MHz.

FEATURES:

- Two ADC channels (Analog Devices AD9430): 12 bits @ 210 MHz
- Xilinx Virtex-4 FX60 FPGA
- High-speed serial I/O through XMC connector
- Companion to Radstone V4DSP
- VITA 42 XMC compliant high-speed serial links (eight lanes @ 2.5 GHz)
- Windows, Linux, and VxWorks device drivers with extensive application and technical support available

For more information, contact: sales@ics-ltd.com

RSC# 29957 @ www.embedded-computing.com/rsc

Innovative Integration

2390-A Ward Avenue • Simi Valley, CA 93065
Tel: 805-578-4260 • Fax: 805-578-4225
www.innovative-dsp.com

Quadia

Quadia is a quad-DSP, dual FPGA, dual PMC site, CompactPCI board with an advanced architecture that provides the best interprocessor connectivity and access to the finest external interfaces available today, delivering blazing performance and extreme flexibility for advanced signal capture and real-time processing applications.

The board features four C6416 DSPs split in two independent clusters each hosting a PMC site and one large FPGA for end-user code, a central FPGA routing interprocessor communication, end-user FPGA communication, external port serial I/O for PCI Express or other private link, global memory, and PCI interface.

FEATURES:

- 1 GHz TMS320C6416 DSP (x4)
- 64 MB SDRAM per processor
- Flexible internal/external communication mesh
- 64-bit/66 MHz CompactPCI
- Two PMC sites with Jn4 to FPGA
- External data port, up to 12 Gbps

For more information, contact: sales@innovative-dsp.com

RSC# 22230 @ www.embedded-computing.com/rsc

Innovative Integration

2390-A Ward Avenue • Simi Valley, CA 93065
Tel: 805-578-4260 • Fax: 805-578-4225
www.innovative-dsp.com

Quixote

Quixote is a 64-bit CompactPCI 6U board for advanced signal capture, generation, and coprocessing. It combines one C6416 DSP with a two or six million gate Virtex-II FPGA, utilizing the best of both worlds in signal processing technology to provide extreme processing flexibility and efficiency and deliver unmatched performance. Dual 105 MHz analog input/output integrate signal capture and waveform generation right on the FPGA external interface. One PMC site facilitates integration of off-the-shelf or custom PMC mezzanine boards. Finally, a PCI-to-StarFabric bridge offers two 2.5 Gbps ports to the new PICMG2.17 switched interconnect backplane, for up to 625 MBps board-to-board or chassis-to-chassis communication.

FEATURES:

- 1 GHz TMS320C6416 DSP
- Two to six MGATE Virtex-II FPGAs
- 32 MB SDRAM, 8 MB ZBT SBSRAM
- AD6645 and AD9764 converters
- 64/32-bit CompactPCI, 66 MHz, 5 V/3.3 V
- Complex trigger modes with hardware event logging

Jacyl Technology, Inc.

P.O. Box 350 • Leo, IN 46765
Tel: 800-590-6067 • Fax: 260-471-6067
www.jacyltechnology.com

AXR-16

Jacyl Technology, Inc. has developed a PC/104 board based upon the Anadigm FPAA. The AXR-16 harnesses the power of the FPAA's fundamental characteristics as a reprogrammable- and reconfigurable-based technology and combines it with the small form factor of the PC/104 platform. The AXR-16 features four Anadigm AN221E04 FPAA components, a Xilinx XC95288 CPLD, a programmable Direct Digital Synthesis (DDS) component (programmable up to 33 MHz), 25 differential or single-ended analog inputs/outputs, five additional dedicated differential or single-ended analog outputs, and 42 user-configurable digital I/O lines.
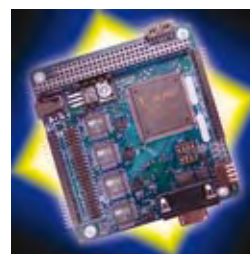
FEATURES:

- Configured with four Anadigm AN221E04 Field Programmable Analog Array (FPAA) components
- Configured with a Xilinx 95288 in-system programmable CPLD
- 25 user-selectable differential or single-ended analog inputs/ outputs
- The outputs of the 8-bit A/D converter located within each AN221E04 can be sent directly into the CPLD
- Each FPAA is completely configurable and programmable through the CPLD
- Programmable 0-33 MHz Direct Digital Synthesis (DDS) source clock for the CPLD and FPAAs

Jacyl Technology, Inc.

P.O. Box 350 • Leo, IN 46765
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www.jacyltechnology.com

LT-300K and LT-50K

The LT-300K and the LT-50K, the LT-Family, were designed to meet the requirements of an FPGA-based PC/104 module needing the maximum number of user-programmable I/O pins and a selectable number of FPGA gates. The LT-300K uses the Xilinx Spartan IIE, XC2S300E-6PQ208, and the LT-50K uses the Xilinx Spartan IIE, XC2S50E-6PQ208, both which have extensive programmable and performance features. The LT-Family of products can be powered from the PC/104 bus or can be powered from an external DC source allowing the boards to be utilized as a stacked module in PC/104 applications or as a stand-alone product design platform. This allows the boards to be ideal in embedded PC/104 applications or to be utilized in development platforms, design prototypes, or production products.

FEATURES:

■ 100 user-programmable I/O pins

■ Two user-defined FPGA global clock inputs

■ Xilinx XC18V00 series in-system programmable configuration PROM

■ Power source either through the PC/104 bus or an external power source

■ Fully supported by the Xilinx free Webpack software

■ Available in commercial and industrial temperature range

For more information, contact: sales@jacyl.com   RSC# 15974/15975 @ www.embedded-computing.com/rsc

Jacyl Technology, Inc.
P.O. Box 350 • Leo, IN 46765
Tel: 800-590-6067 • Fax: 260-471-6067
www.jacyltechnology.com

XG-300K

The XG-300K is a PC/104-based board featuring a Xilinx 300K Spartan IIE, 4Meg of high-speed (10 ns) RAM, 512K of EEPROM, programmable Direct Digital Synthesis (DDS) chip, 44 I/O pins, and dedicated differential inputs and outputs. The board uses the Xilinx Spartan IIE, XC2S300E-6PQ208, which has extensive features including: 6,912 logic cells, 98,304 distributed RAM bits, and 64K block RAM bits. The XG-300K can be powered from the PC/104 bus or can be powered from an external DC source allowing the board to be utilized as a stacked module in PC/104 applications or as a standalone product design platform. This allows the board to be ideal in embedded PC/104 applications or to be utilized in development platforms, design prototypes, or production products. The small size, versatility, and extensive features of the XG-300K make it a prime target for embedded applications or as an integrated part of a larger system.

The Spartan IIE FPGA's four global clock inputs are configured with the PC/104 master clock, a 100 MHz onboard oscillator, and two outputs from the DDS (one direct and one complimentary output of the DDS). This allows the XG-300K to be very flexible on single or multiple system clock requirements or system clock configurations.

The form factor and robustness of the XG-300K provides an ideal platform for embedded applications or as an integrated piece of a system.

FEATURES:

- Xilinx Spartan IIE 300,000 gate FPGA
- 4Meg (256K x 16-bit) high-speed RAM
- 512K (64K x 8-bit) EEPROM
- 0-33 MHz programmable Direct Digital Synthesis (DDS) chip
- FPGA global clocks include PC/104 bus, 100 MHz onboard oscillator, and the DDS outputs
- 44 I/O pins (potential of a total of 50 I/O pins)
- Xilinx XC18V02 series in-system programmable configuration PROM
- Two dedicated pairs of differential inputs and two dedicated pairs of differential outputs
- Fully supported by the Xilinx free Webpack software
- IEEE 1149.1 JTAG compliant communication port
- Power sources either through the PC/104 bus or an external power source
- Available in commercial and industrial temperature range

Jacyl Technology, Inc.
P.O. Box 350 • Leo, IN 46765
Tel: 800-590-6067 • Fax: 260-471-6067
www.jacyltechnology.com

XG-5000K

The XG-5000K, the 5 million gate PC/104-*Plus* FPGA board.

Centered around a 5 million gate Spartan 3 FPGA, the XG-5000K is the ultimate PC/104-*Plus* FPGA board that is ready to meet the most demanding of system designs. The board features a 5 million gate Spartan 3 FPGA, 256 MB of onboard Micron SRAM, 32 MB of onboard Intel flash, 264 user-programmable I/O, Type 1 CompactFlash connector, a secondary 400K Gate Spartan III FPGA, 10/100BASE-T Ethernet interface, two RS-232 interfaces, PC/104 connector, PC/104-*Plus* connector, 0-25 MHz programmable DDS master clock source, 8 MB of secondary DataFlash, and a 25 MHz initial master clock.

The XG-5000K has the advanced feature of allowing the user to remotely reconfigure the entire board through the onboard JTAG connector, PC/104 connector, PC/104-*Plus* connector, 10/100BASE-T Ethernet interface, or any external interface connected to the XG-5000K. The XG-5000K has been developed with Xilinx's advanced design revisioning technology. This allows the XG-5000K to retain onboard as many as 16 partial or up to 4 complete design revisions for the 5 million gate Spartan 3 FPGA. Any one of these design revisions can be remotely programmed into the 5 million gate Spartan 3 FPGA, or the XG-5000K can be programmed to reconfigure itself based upon external or internal events.

The XG-5000K also incorporates a secondary 400,000 gate Spartan III FPGA. This second FPGA is initially configured to control remote reprogramming and control of the design revisioning features of the XG-5000K. But the secondary Spartan III FPGA can be reconfigured by the user to meet the requirements of a particular system design.

The XG-5000K can be powered from the PC/104 bus or can be powered from an single 5 Vdc external source allowing the board to be utilized as a stacked module in PC/104 applications or as a standalone product design platform. This allows the board to be ideal in embedded PC/104 applications or to be utilized in development platforms, design prototypes, or production products.

Available in industrial temperature range.
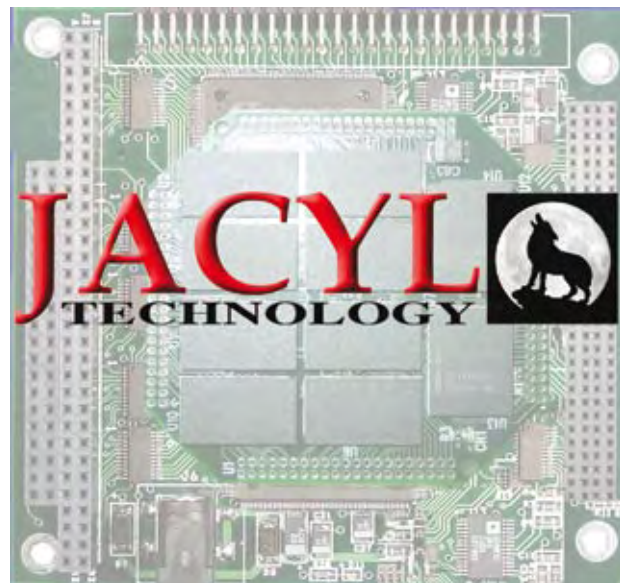
FEATURES:

- 5 million gate Xilinx Spartan III FPGA on a PC/104-*Plus* platform
- Onboard 256 MB of Micron SRAM and 32 MB of Intel flash
- Four 66-pin VHDC connector banks providing a total of 264 user-programmable I/O
- CompactFlash Type 1 connector
- A secondary 400K gate Spartan III FPGA for remote reconfiguration and design revisioning of the XG-5000K or custom user configuration
- 10/100BASE-T Ethernet interface and two RS-232 interfaces
- Can be used in a PC/104 stack or as a standalone product design platform
- 0-25 MHz user-programmable DDS FPGA master clock source along with a fixed 25 MHz FPGA master clock source
- Incorporates Xilinx's design revisioning technology and can retain onboard as many as 16 partial or up to 4 complete design BIT files
- Can be reconfigured through the configuration PROMs, JTAG, 10/100BASE-T Ethernet, PC/104, PC/104-*Plus* connectors, or the user I/O
- Can be powered from the PC/104 connector or an external 5 Vdc source
- Available in industrial temperature range

For more information, contact: sales@jacyl.com

RSC# 31406 @ www.embedded-computing.com/rsc

QuickLogic Corporation

1277 Orleans Drive • Sunnyvale, CA 94089
Tel: 408-990-4000 • Fax: 408-990-4040
www.quicklogic.com

PolarPro™ Solutions

Power conservation and the challenge of connecting numerous peripherals to an embedded processor have become critical issues as the convergence within the portable electronics market grows. Traditionally, ASICs were used to resolve power issues since FPGAs were not seen as an option for low power design.

Today, QuickLogic® squashes this belief with its low power PolarPro FPGA that not only supersedes low power requirements but also solves the problem of connecting peripherals to processors that lack the required interfaces for Wi-Fi, wired LAN, mobile digital TV, and Hard Disk Drives (HDDs).

The PolarPro Family offers the lowest power programmable logic available in the industry, with a standby current of less than 10 µA. This family mimics ASIC-like power consumption in static, idle, and dynamic modes, enabling it to extend battery life by four times, as compared to other technologies. The key to PolarPro's low power capability is its unique Very Low Power (VLP) mode. VLP mode can be entered into from normal operation in under 250 µs and return just as quickly. This is a significant improvement over other sleep modes, which can take as long as 2 ms to exit from sleep mode, making them impractical for real-life applications.

QuickLogic uses this PolarPro architecture to solve the connectivity dilemma by providing companion devices that support PCI-based peripherals such as Wi-Fi, USB, LAN controllers, IDE-based HDDs, and SDIO-based peripherals such as Wi-Fi and digital TV. These power-efficient solutions connect seamlessly to the Intel® PXA2xx processor. QuickLogic also provides software drivers for both Windows CE and Linux. These solutions have all been verified with peripherals and modules from industry-leading suppliers.

To enable design engineers to develop both their connectivity and storage solutions quickly, QuickLogic has also developed a Mobile Applications Board (MAB) to be used with the Intel PXA2xx processor, accelerating time-to-market.

FEATURES:

- Standby current is less than 10 µA
- Flexible, high-density, low power programmable logic device extends battery life by four times compared to competing devices
- Internal memory circuits maintain original logic values after exiting VLP mode; competitors' devices lose all register values
- Companion devices resolve interface challenges for Wi-Fi, HDD, LAN, USB, and UWB
- Both Linux and Microsoft Windows® CE solutions have been system verified and optimized for maximum throughput

VMETRO Inc.

1880 S. Dairy Ashford, Suite 400 • Houston, TX 77077
Tel: 281-584-0728 • Fax: 281-584-9034
www.vmetro.com

Phoenix VPF1

The Phoenix VPF1 is a 6U VME64x data and signal processor supporting VITA 41 backplane switch fabric communications via VXS over P0. The VPF1 comprises four processor nodes: two 1 GHz PowerPC 7447A CPUs and two Xilinx XC2VP70 Virtex-II Pros. Each processor has fully distributed memory, and each FPGA supports multiple inter-node communication channels via RocketIO. These channels bind together local processors and those on separate boards for seamless and scalable processing.

A PMC site, GbE, and P2 resources enable I/O. A comprehensive suite of PowerPC and FPGA tools facilitate rapid development and deployment. Phoenix VPF1s are available in air-cooled or conduction-cooled builds, enabling easy migration from development to production.

FEATURES:

- 2x PowerPC 7447 CPU nodes and 2x Xilinx Virtex-II Pro FPGA nodes
- 8x 2.0-3.125 Gbps off-board serial communications channels
- Ethernet, RS-232, RS-422
- 64-bit, 66 MHz PMC site for local I/O
- VXS (VITA 41) compatible
- Air-cooled and rugged, conduction-cooled build variants

For more information, contact: info@vmetro.com

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VMETRO Inc.

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Tel: 281-584-0728 • Fax: 281-584-9034
www.vmetro.com

PMC-FPGA03/F PMC

The PMC-FPGA03 is a Xilinx XC2VP50 Virtex-II Pro-based FPGA PMC module, which interfaces directly to two banks of DDR SDRAM and three banks of QDR-II SRAM for high-performance, low-latency applications. Xilinx RocketIO channels are available at either the front panel or PMC connector as a build option. The PMC-FPGA03 communicates with a variety of Windows, VxWorks, and Linux host computers via an optimized 64-bit, 66 MHz PCI bus interface. The module is available in air-cooled and conduction-cooled variants. Fiber-optic options are also available. Example VHDL code blocks are provided to show how the PMC-FPGA03 resources can be used, along with utilities for configuring flash.

FEATURES:

- Xilinx XC2VP50 Virtex-II Pro FPGA
- Multi-Gbps serial I/O
- Modular I/O system supporting standards such as LVDS, Camera Link, and custom I/O
- Multiple banks of QDR-II SRAM and DDR SDRAM
- Rugged, conduction-cooled build variants

For more information, contact: info@vmetro.com

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High-performance computing

Advantech Corporation

15375 Barranca Parkway, Suite A-106 • Irvine, CA 92618
Tel: 800-866-6008 • Fax: 949-789-7179
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Trusted ePlatform Services

ADVANTECH

ARK-7480

ARK-7480 is a high-performance and robust application-ready embedded box computer supporting UFCPGA2, 478-pin embedded Intel® Pentium® 4 or Celeron® D processors up to 2.8 GHz, an Intel 852GME chipset with Graphics Memory Controller Hub (GMCH), and Intel 82801DB I/O Controller Hub 4 (ICH4). Includes three PCI expansion slots, dual Fast Ethernet (optional GbE), six USB 2.0 ports, six COM ports, DVI, LVDS, and VGA display interface, a drive bay for a 3.5" HDD (optional second 3.5" HDD space), CompactFlash socket, Mini PCI, and an optional expansion drive bay for a CD-ROM, card reader, or other peripherals. ARK-7480 is ideal for diverse embedded system applications requiring the highest processor performance and expansion capability. It offers a truly unique combination of power, rugged reliability, and size that make it great to build applications around.

The 295 mm x 180 mm x 260 mm cast aluminum chassis allows the ARK-7480 to not only offer scalable CPU performance and flexible I/O expansion (customization support available), but its smart, cableless, modular design makes setup, mounting, and maintenance more efficient and flexible. One side of the ARK-7480 gives easy access to all connectors and allows for easier horizontal or vertical mounting. The chassis and vibration-resistant construction feature antivibration card holders for PCI I/O expansion cards as well as HDD cushions, allowing the system to provide up to 1 *g* vibration/10 *g* shock protection. Simply put, the ARK-7480 can handle machine automation applications, industrial environments or control cabinets, support gaming, ATM, Kiosks, and more.

ARK-7480's six USB 2.0 ports support USB peripherals such as storage subsystems, security ID devices, card readers, barcode scanners, multifunction printers, and scanners used directly or shared among users via a network. It is equipped with dual Fast Ethernet and 6x serial ports, including one RS-232/422/485 serial port and five RS-232 serial ports that enable communication and control at the field level for measurement and operator control.

FEATURES:

- Supports Embedded Intel Pentium 4/Celeron D processors
- 6x USB ports, 6x serial ports, and dual LAN port capacity for intensive control and communication
- CRT, DVI, LVDS, display interface with dual display capability
- Antivibration to HDD and PC board to ensure maximum reliability
- One side access for all external wiring connections, easy integration, and easy maintenance
- Support wall mount in horizontal or vertical direction
- Robust, heavy-duty metal cast construction; modularized design offers maximum space efficiency

For more information, contact: ECGInfo@advantech.com   RSC# 31245 @ www.embedded-computing.com/rsc

Annapolis Micro Systems, Inc.

190 Admiral Cochrane Drive, Suite 130 • Annapolis, MD 21401
Tel: 410-841-2514 • Fax: 410-841-2518
www.annapmicro.com

WILDSTAR II Pro PCI

Annapolis Micro Systems is a world leader in high-performance, COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, DSP, FFTs, communications, Software-Defined Radio, encryption, image processing, prototyping, text processing, and other processing intensive applications. Our ninth-generation WILDSTAR II Pro for PCI uses Xilinx's newest Virtex-II Pro FPGAs for state-of-the-art performance. It accepts one I/O card in one, or up to two I/O cards in two, PCI or PCI-X slots, including Dual 1.5 GHz A/D, Dual 1.5 GSps D/A, Quad 105 MHz, Universal 3 Gb (Rocket I/O, 10 GbE, InfiniBand), Quad FC2, Quad GbE, and LVDS. Our boards work on a number of operating systems, including Win NT, 2000, XT, Linux, Solaris, IRIX, ALTIX, and VxWorks. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models.

Develop your application very quickly with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily build and test their algorithms on the real hardware that will be used in the field. CoreFire, based on dataflow, automatically generates distributed control fabric between cores.

Our extensive IP and board support libraries contain more than 1,000 cores, including floating point and the world's fastest FFT. CoreFire uses a graphical user interface for design entry, supports hardware-in-the-loop debugging, and provides proven, reusable, high-performance IP modules. WILDSTAR II Pro for PCI, with its associated I/O cards, provides extremely high overall throughput and processing performance. The combination of our COTS hardware and CoreFire allows our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customers' applications succeed. We offer training and exceptional special application development support, as well as more conventional support.

FEATURES:

■ One or two Virtex-II Pro Xilinx FPGA processing elements – XC2VP70 or XC2VP100

■ Up to 96 MB DDRII or QDRII SRAM

■ Up to 512 MB DDR DRAM

■ Programmable flash for each processing element to share FPGA images

■ Works with PCI or PCI-X backplane

■ High-speed DMA multichannel PCI controller

■ Host software: Win NT, 2000, XP, Linux, Solaris, DECAlpha, IRIX, and ALTIX

■ Full CoreFire board support package for fast, easy application development

■ VHDL model, including source code for hardware interface and ChipScope access

■ Save time and effort and reduce risk with COTS boards and software

■ Achieve world-class performance – WILD solutions outperform the competition

■ Includes one-year hardware warranty, software updates, and customer support; training available

HARTMANN ELEKTRONIK GmbH

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Tel: +49-711-13989-0 • Fax: +49-711-866-11-91
www.hartmann-elektronik.com

PCI Extension Cassette

Now you can conveniently extend the possibilities of your PC or compact PC using THE BRIDGE StarFabric cards and PCI extension modules from HARTMANN ELEKTRONIK.

Thanks to the PCI Extension Cassette from HARTMANN ELEKTRONIK, the limited number of slots in your PC is no longer a problem – simply plug in a cable, and off you go!

Up to three PCI Extension Cassettes from HARTMANN ELEKTRONIK can be installed in a 19 3U card rack. You can connect up to five PCI Extension Cassettes to one PC or CompactPCI system by using a six-port switch.

The Fabric 6 Port Switch from HARTMANN ELEKTRONIK supports virtually unlimited extension. The PCI extension module introduces a great deal of flexibility, making it an ideal solution for test setups or integrated systems.

FEATURES:

- Effective speed: Data transfer up to 440 MBps
- Distances of up to 15 m from the PC are possible using CAT5 cabling between PC and extension
- Four PCI slots with 32- or 64-bit are available additional
- No additional software required, completely transparent connection
- Available as a box, board, or cassette for individual networking with the Fabric 6 Port Switch
- ATX connector or Faston for power; front panel: 3U/28 HP; depth: 200 mm

For more information, contact: info@hartmann-elektronik.de

RSC# 30775 @ www.embedded-computing.com/rsc

Octagon Systems

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www.octagonsystems.com

XMB-1

The XMB-1 is part of Octagon's line of IND-CORE™ systems that offer out-of-the-box solutions for transportation, military, and security applications. The XMB-1 is a "no compromise" design for a mobile server that optimizes the electrical, thermal, and mechanical components for maximum reliability. The result is a powerful, yet fanless system in a rugged extrusion. The basic unit includes the processing power, power supply, memory, and I/O for most applications. Yet it can be easily expanded using PC/104 I/O function blocks or Octagon's XBLOK™ half-size PC/104 expansion modules. Applications include planes, trains, buses, military, homeland security, police, communications, and SCADA markets.

FEATURES:

- Linux and Windows® XPs, OS Embedder™ kits
- 6-32 VDC power supply
- Shock and vibration mounting options
- -40 °C to 75 °C operating temperature
- Removable option panel allows for custom connectors, annunciators, and controls
- Size is 6" (W) x 4.2" (H) x 10.8" (D)

For more information, contact: sales@octagonsystems.com

RSC# 31411 @ www.embedded-computing.com/rsc

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ICPe-SYSC-EXP

Complete 3U and 4U *CompactPCI Express* systems and components make their debut for high-end rugged applications in industrial environments.

The **GoldNugget** is a 3U, 44 HP system complete with a 2 GHz, actively cooled Pentium M or conduction-cooled ULV Celeron M CPU board, five free 32-bit CompactPCI slots (of which three are "hybrid" and can be used for dedicated Express I/O boards), 100 W AC/DC PSU and translation board (CompactPCI Express to CompactPCI) with independent Gigabit Ethernet, provision for an onboard Serial ATA hard disk and/or rear I/O based SATA RAID solutions.

For high-end industrial applications, a full-size, 84HP, 4U **GoldRush** enclosure is available with provision for either an ATX power supply or standard Inova 100 W CompactPCI Express PSU. The **GoldRush** enclosure may be open (ventilation holes) to allow the free passage of air, or closed, but still benefit from the airflow supplied by the supervised underslung removable fan tray unit.

The newly developed **GoldMine** CompactPCI Express CPUs for use in these systems are based on the i915 chipset and address up to 2 GB of 533 MHz DDR2 RAM. These CPUs provide legacy I/O support, USB 2.0, Gigabit Ethernet, graphic translation (LVDS, SDVO), and Serial ATA or conventional EIDE mass storage interfacing. For true rugged deployment, application code and OS can be neatly accommodated in either µDOC Flash, conventional CompactFlash, or the latest 1.8" hard disk medium.

Integrated into the BIOS Flash is a µLinux kernel for total cost-of-ownership reduction (OS license), remote diagnostic and field servicing, rapid boot, and for robust applications where rotating parts cannot be tolerated.

An implementation of the Intelligent Platform Management Interface (IPMI) enables the boards to monitor, log, and control many of the CPU's functions for fast pre-boot diagnostics, OS self-repair, and lifetime forecasting in harsh industrial environments.

Complete with the ULV Celeron M CPU, the **GoldNugget** system is available for rugged applications starting at $2,990 for OEM volume.

FEATURES:

■ **First complete 3U/4U CompactPCI Express system**
– 100 W CompactPCI Express 115 V/230 V AC/DC PSU
– Optional ATX power supply
– 6-slot CompactPCI Express backplane with legacy support
– Translation board with Gigabit Ethernet and HD interface
– Windows XP Embedded
– MTBF > 200,000 hours
– 0 °C to +60 °C operational temperature
– Conforms to EN50155 (DC PSU)

■ **1 GHz ULV Celeron M/ 2.0 GHz Pentium M CPU**
– Intel 915GM chipset with DirectX 9 H/W support
– Up to 2 GB 533 MHz DDR2 RAM
– VGA/DVI/TFT supported video formats
– Up to 2048 x 1536 pixel video resolution
– Up to two independent Gigabit interfaces
– Up to eight USB 2.0 interfaces
– CPU extension with HD, COM, and PS-2 interfaces
– Single-slot, inline Serial ATA interface
– µDOC technology or CompactFlash
– µController for system management
– Intelligent rear I/O

The conduction-cooled 1 GHz Celeron version is just 4HP wide and is suited to applications in harsh environments or extremes of temperature.

Inova Computers, Inc.

610 Ten Rod Road • North Kingstown, RI 02852
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www.inova-computers.de/icpepm2e.php

ICPe-PM2e GOLDMINE

The new GoldMine from Inova Computers is part of a new family of highly integrated 3U *CompactPCI Express* CPUs offering performance and functionality levels typically reserved for 6U boards.

During the board's design phase, Inova Computers considered, in particular, the requirements of the embedded server market and, as a result, integrated a Baseboard Management Controller (BMC). Hence, for the first time, features such as remote diagnostic or remote, OS-free serviceability, crash recovery, and self-healing functions have been introduced to the 3U world.

Inova customers profit from the **GoldMine** CPU twofold from the μLinux Kernel (SuSe) integrated in the BIOS flash. It can be used as a free standalone operating system with total cost-of-ownership reduction through zero OS license costs. Or, if the Linux OS is integrated fully, then system commissioning in the field becomes a whole lot simpler. As an added free bonus, boot times are kept to a minimum and the OS is immunized against vibration and the extreme climatic conditions typically found in mobile (transportation) or outdoor applications.

The single-slot, 4HP CPU has three USB 2.0 interfaces, a Gigabit Ethernet interface, and DirectX 9.0 compatible video from the i915 chipset available on the front panel. In addition, a bootable USB μDOC device can be installed for very robust, embedded applications. An 8HP version has an additional independent Gigabit Ethernet, three more USB 2.0 interfaces, a configurable RS-232/485 COM port and legacy PS/2 mouse/keyboard interface. Both CPU variants can extend their already rich I/O feature set through rear I/O, which offers Fast Ethernet connectivity alongside a Serial ATA, which suits RAID systems for example, and additional USB, COM, and legacy PS/2 support.

These CPUs open the door for CompactPCI Express to address high-end server, mission-critical, or high-availability applications, such as those found in demanding control systems, video servers, or data servers in production areas.

The fully functional, high-end CPU is available for $1,875 in OEM quantities.

FEATURES:

1 GHz ULV Celeron M/2.0 GHz Pentium M CPU

- ■ ***CompactPCI Express*** architecture throughout
- ■ Supports all 1 GHz to 2.0 GHz Dothan processors
- ■ Intel 915GM chipset with DirectX 9 H/W support
- ■ Up to 2 GB 533 MHz DDR2 RAM clocked at 400 MHz or 533 MHz
- ■ VGA/DVI/TFT supported video formats
- ■ Up to 2048 x 1536 pixel video resolution
- ■ Up to two independent Gigabit interfaces
- ■ Up to 8x USB 2.0 interfaces
- ■ CPU extension with HD, COM, and PS-2 interfaces
- ■ Single-slot, inline Serial ATA interface
- ■ μDOC technology or CompactFlash
- ■ μController for system management
- ■ Serial ATA HD support up to 160 GB devices
- ■ LPC routing through the backplane
- ■ Integrated IPMI bus
- ■ Comprehensive and intelligent rear I/O
- ■ For a customized application to your needs, send your requirements to Paul or Debra at 401-667-7218 or e-mail sales@inova-computers.com

  The conduction-cooled 1 GHz Celeron version is just 4HP wide and is suited to applications in harsh environments or extremes of temperature.

For more information, contact: sales@inova-computers.com

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www.mc.com/ensemble

Computer Systems, Inc.
MERCURY

Ensemble2 Platform

The Ensemble2™ Application Platform is a standards-based system for developing, prototyping, and deploying applications. Ensemble2 allows developers to evaluate and deploy their applications on the same platform. Built around the power, functionality, and scalability of Serial RapidIO, AdvancedTCA, and AdvancedMC the platform supports a variety of I/O sources and heterogeneous processing, thereby reducing project costs, improving resource efficiency, and minimizing the design and deployment risks of next-generation communications systems.

The Ensemble2 platform scales to 14- or 16-slot configurations, supports hot-swappable AdvancedMC modules, and delivers 10 Gbps of Serial RapidIO capacity to every processing component in the heterogeneous platform. This critical functionality facilitates application-level evaluations in the lab and deployments in the field, and the system management software delivered with Ensemble2 reduces development and porting time. A fully configured Ensemble2 chassis can encompass up to 56 AdvancedMC modules per system. This scalability and flexibility is essential to support application benchmarking tasks, with the backplane delivering as much as 150 Gbps of low latency and efficient data messaging capacity. Multichassis support is available via Serial RapidIO fiber mezzanine modules.

As communications system developers migrate to Commercial Off-the-Shelf (COTS) alternatives, they need open standards-based system-level solutions with the support of Tier 1 ecosystems. They are increasingly relying on these integrated solutions to make the evaluation of their applications easier over a broad range of vendor technologies. The Ensemble2 platform is architected to help OEMs leverage the RapidIO standard and its rich ecosystem, allowing them to manipulate and tune the embedded fabric for specific application requirements.

The Ensemble2 platform supports either a heterogeneous or a homogeneous OS environment, such as Linux and OSE, among others. The software suite allows Ensemble2 systems to exploit RapidIO's rich configuration and runtime features.

FEATURES:

■ Completely integrated 10 Gbps AdvancedTCA system solution

■ Early access to latest Serial RapidIO silicon

■ Modular configurations based on AdvancedMC form factor

■ Scales to 14- or 16-slot configurations

■ Supports hot-swappable AdvancedMC modules

■ Ideal for application development

■ Facilitates application-level evaluations in the lab and deployments in the field

■ System management software reduces development and porting time

■ High performance and broad interoperability among platform components

■ RapidIO hub card has 80 Gbps of bisectional communication and support for interchassis and intershelf bridging

■ Configuration options support heterogeneous processing: AdvancedMC carrier, RapidIO Ethernet, interchassis AdvancedMC, DSP farm, FPGA, or NP

■ Production ready, quick to market

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Thermite® COTS PC

Thermite® is the first low-cost, COTS, open architecture, small form factor, tactical visual computer designed for wearable and vehicle-based deployment. Thermite is optimized for 2D/3D graphics and video-intensive C2, C4ISR, surveillance, embedded training, mission planning, and other apps where the combination of PC compatibility (Linux or Windows), MIL-SPEC hardness, small size, long battery life, and high performance (compute, networking, graphics, and video) is essential. Compliant with MIL-STD-810F/461E, Thermite features a sealed alloy case, embedded CPU and GPU with 2D/3D advanced graphics and video support, solid-state drives, power management, and comprehensive I/O, all of which enable Thermite to deliver work station performance in extreme environments.

FEATURES:

- Open architecture – 100 percent PC compatible with support for Linux and Microsoft® Windows Operating Systems
- Low cost, small, light, and efficient (4.5" x 6.8" x 3", 2.5 pounds, ~ 23 W) – with vehicle and battery power options
- Conduction-cooled, rugged design with MIL-SPEC I/O – for use in MIL-STD-810F/461E extended environments
- Advanced GPU/video module option for 2D/3D graphics-intensive apps with support for video capture and display
- Intel Pentium M CPU, 1-2 GB RAM, solid-state or shock-resistant HD, and PC I/O (Ethernet, USB2, SIO, 1394)
- Optional GPS, MIL-STD-1553B, 802.11, secure comms, CANbus, Gigabit Ethernet, and other I/O options

For more information, contact: salesinfo@quantum3d.com

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www.vmetro.com

Phoenix VXS System

Phoenix systems are built around high-performance processing, I/O, and multichannel Gbps serial communications with supporting software and firmware. They solve the next generation of performance computing requirements by combining the processing benefits of large FPGAs and PowerPC CPUs with a high-speed serial communications fabric. This configuration gives developers access to increased levels of processor density to produce smaller, lower-cost, and more effective solutions.

VMETRO's Phoenix VXS family includes FPGA/PowerPC processing, real-time switches, intelligent I/O controller with XMC/PMC sites, high-speed analog I/O, software/firmware communications support, backplanes, and enclosures. Phoenix solutions are suited for applications such as radar, ELINT, and EW.
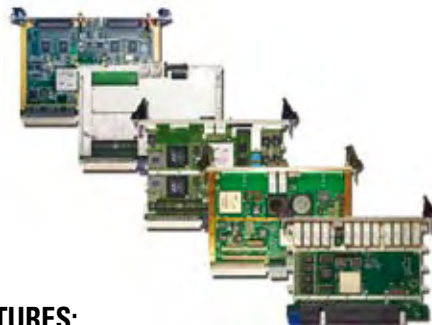
FEATURES:

- High-performance data processing utilizing dual PowerPC and dual FPGA CPUs
- High-speed communications through a VXS fabric, multichannel data links, and raw or switch-packet protocols
- High-speed serial communication, zero-latency switch cards
- Intelligent PMC/XMC I/O controller, carrier, and recorder blade
- High-speed analog input cards
- TransComm FPGA Communications Toolbox for low-latency, efficient data communications

For more information, contact: info@vmetro.com

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V5SC

The V5SC is a high-performance DC-to-DC 35 W converter that supplies +5 V. The V5SC also includes a flash-based microcontroller that supplies advanced power management, smart battery charger, and an RS-232 serial port. The V5SC is designed for low-noise embedded computer systems, has a wide input range of 6-40 V(> 6:1), and is ideal for battery or unregulated input applications. The V5SC is specifically designed for vehicular applications and has heavy-duty transient suppressors (6,000 W) that clamp the input voltage to safe levels while maintaining normal power supply operation.

FEATURES:

- 35 W capability
- PC/104 size and mounting holes
- RS-232 serial port
- 750 mA-hour battery backup
- 6 V to 40 V DC input range
- Supports up to eight digital temperature sensors
- Opto-coupled inputs

Why automate testing?

By Kingston Duffie

T*he software embedded in high-tech equipment allows vendors to offer an astounding variety of features to their customers. But, while technology advances and competitive pressures drive companies to rapidly add new features and expedite product release cycles, the process for validating equipment has not changed significantly to keep pace with technology changes. As a result, equipment vendors may think they are left with the undesirable choice of either shipping products before they are adequately tested or missing time-to-market opportunities. Kingston explores how test automation tools can remedy this problem.*

Quality assurance quandary

The problem of adequate testing is always challenging, but compounds dramatically over the product life cycle. As features are added, the test plan isn't restricted to new features in the current version. The complete system must be tested to ensure that all new features work, nothing that was working has broken, and that there is seamless interaction between existing and new features. Testers must deal with rapidly growing test plans in a timeline reduced by market deadlines driven by competition. This creates an uneasy balance with a backlog of test cases and frustrated testers at one end and the increasing costs of field service for unresolved Quality Assurance (QA) issues at the other. It is a reactive, not proactive, stance that hampers the abilities of QA organizations to adequately test the stability of new products before delivery to market.

Fanfare's customers and other equipment vendors have identified an obvious answer to this dilemma – test automation. A significant portion of today's testing effort is spent performing mundane and repetitive tasks such as configuring test beds, manually executing regression tests, documenting existing test cases, and attempting to reproduce bugs. When performed manually, these tasks are often error prone and poorly documented. QA teams need to automate these routine tasks so they can free up time to focus on real-world use cases, corner cases, and testing strategies that result in high-quality products.

While there is no question that test automation benefits the QA industry, the lack of tools that support the automation effort challenges QA teams. There are many commercial tools available for specific portions of the testing effort, including traffic generators from companies such as Ixia, Spirent, and Agilent, or software built for the special needs of corporate IT departments that test enterprise applications such as Mercury's WinRunner or Segue's Silk. Most test automation for high-tech equipment, however, is performed with scripting languages such as Tcl, Perl, and Python.

The predicament: Scripting works, but it doesn't scale. With the complex skill sets necessary to build and execute effective test case scripts, it is increasingly difficult to find and retain staff with combined expertise in QA, domain knowledge of the device under test, and the advanced scripting skills required for developing maintainable regression tests. Many companies assign scripting tasks to special test automation teams that then must implement specific processes and measurements to ensure effective coordination and communication with other testers involved in the QA process.

The right tools

QA teams need modern tools that will make test automation accessible to every member of the testing team, such as FanfareSVT, an IDE for testing high-tech equipment (see Figure 1 next page). With the right tools, all testers can create new automated test cases and adjust existing regression tests, working easily with sophisticated test beds that include many heterogeneous devices. Historically, equipment has been controlled exclusively via custom interfaces. But, today's devices are configured, controlled, and monitored through a variety of standard mechanisms including command line interfaces, embedded Web interfaces, or Tcl APIs. This standardization has enabled the development of commercial automation tools.

Integrated development environment

Testing is accelerated by the ability to run routine tests with predetermined criteria, for example, on a pass-fail basis or through conditional structures. This allows testers to eliminate mundane manual test case execution and accelerate test bed initiation to dramatically increase test coverage. QA teams that in the past would run a complete regression on a new release two or three times during a QA cycle with their existing Tcl scripts now can run a complete regression every night with the adoption of test automation tools. And, frequent testing means faster analysis of test failures since less code has changed between test runs.

Test automation tools ease the documentation process and improve communication among team members. A good test automation tool includes a test authoring system that allows tests to be created and documented at the same time. What has traditionally been a sequential process of designing, executing, documenting, and automating tests can now be unified into a single step. Therefore, once a feature has been tested, it is also automated and documented, allowing teams to share straightforward execution reports between testers, developers, and other teams, improving the ability to efficiently communicate identified bugs. Automation teams also benefit from using tools designed to integrate with existing regression testing infrastructures. Test scripts can continue to be used, QA processes are leveraged not replaced, and the overall level of automation increases.
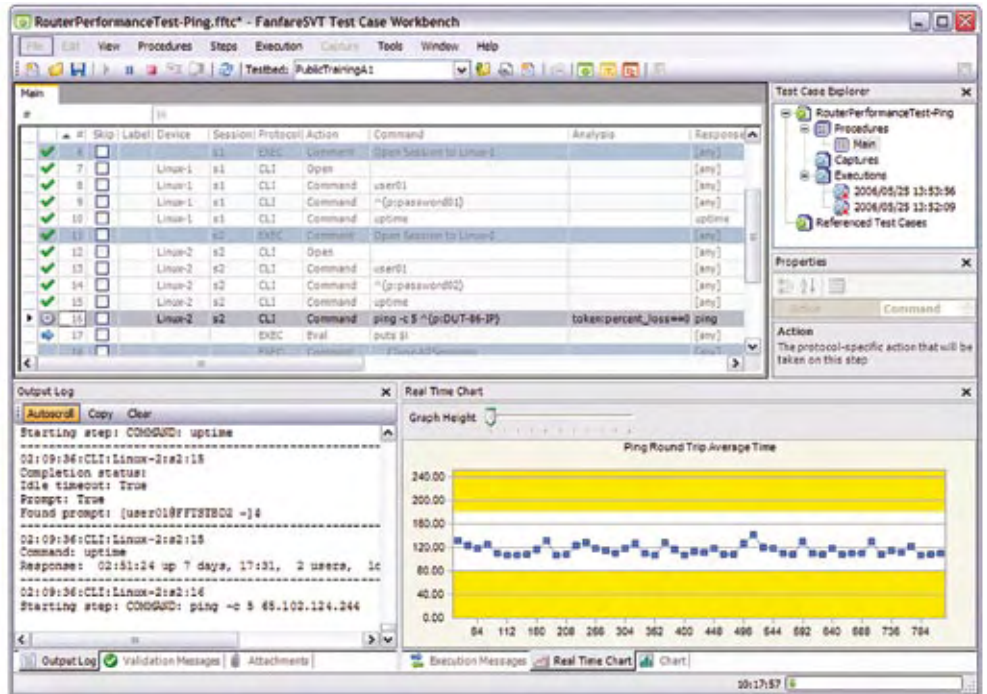
With the right tools, every member of the test team can contribute directly to the automation effort. Ultimately, automated testing frees QA teams to do what they do best – provide the highest-quality products and services to market by anticipating the end-user experience. ECD

Figure 1

Kingston Duffie is founder and CTO of Fanfare and creator of FanfareSVT, the industry's first IDE for testing high-tech equipment. Kingston has more than more than 20 years of experience in the computer networking and telecommunication industries and has founded several highly successful companies in this space. During his career, Kingston has earned a reputation for delivering progressive ideas, innovative solutions, and quality products. He holds a BS in Engineering Physics from Queen's University in Kingston, Ontario and an MS in Electrical Engineering from McGill University in Montreal.

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Develop your application very quickly and easily with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily and quickly build and test their algorithms on the real hardware that will be used in the field.

Use CoreFire's graphical interface to drag and drop library elements onto the design window. Modify your input and output types, numbers of bits, and other core variables by changing module parameters with pull-down menus. The modules automatically provide correct timing and clock control. Insert debug modules to report actual hardware values for hardware-in-the-loop debugging. Hit the Build button to check for errors and as-built core sizes and to build an encrypted EDIF file. Use the Xilinx ISE tool to place and route each FPGA design. Modify and use the jar file or the C program created by the CoreFire Build to load your new file into your WILDSTAR II and I/O card hardware. Use the CoreFire Debugger to view and modify register and memory contents in the FPGA and to step through the dataflow of your design running in the real physical hardware.

Our extensive IP and board support libraries contain more than 1,000 proven, reusable high-performance cores, including FIR and CIC filters, a channelizer, and the world's fastest FFT. We support conversion between data types: bit, signed and unsigned integers, single precision floating point, integer and floating point complex, and arrays. A few of the newly added array cores include array composition and decomposition; slice, parallelize, serialize, repack, split, merge, reorder, rotate, and concatenate transformations; matrix math, sliding windows, and convolutions.

The combination of our COTS hardware and CoreFire enables our customers to make massive improvements in processing speed while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.
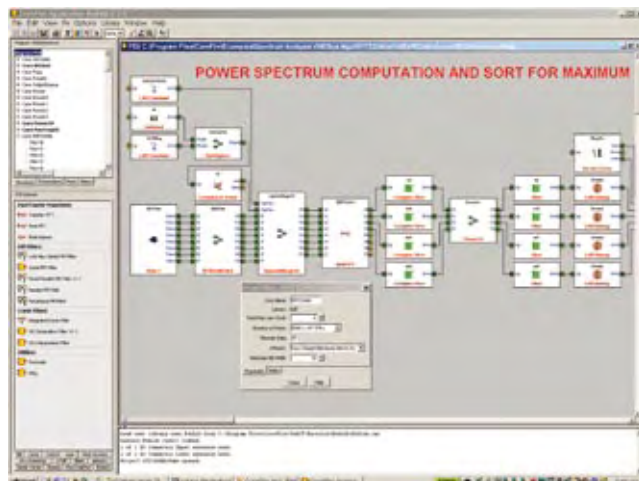
FEATURES:

- Dataflow-based – automatically generates intermodule control fabric
- Drag-and-drop graphical interface
- Work at high conceptual level – concentrate on solving algorithmic problems
- Hardware-in-the-loop debugging
- More than 1,000 modules incorporate years of application experience
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E-Guardian 1000

The rugged and ultracompact E-Guardian series is the most affordable industrial-grade mobile digital video recorder. It is specially designed to withstand harsh environments and is suitable for diversified mobile security applications.

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FEATURES:

- 4/8-channel video-in and 1/2-channel audio-in; retrieve video by date, time, and event; motion detection
- Menu-driven, easy to operate, external device activation (DI/DO connectors), remote controller
- Support plug-and-play GPS function, date, time, speed, and GPS data on screen display
- Designed to withstand harsh environments and suitable for diversified mobile security applications
- Ideally deploy to heavy-duty and passenger vehicles, and protect your assets and people
- Advertisement and public announcement; wirelessly update contents

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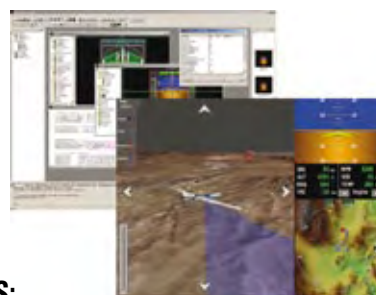
IData™ HMI Toolkit

IData™ is a suite of powerful, cost-effective, PC-based Human Machine Interface (HMI) tools that enables rapid prototyping, development, and deployment of dynamic and interactive cross-platform 2D and 3D OpenGL-based HMIs for embedded systems, data display, and simulation applications. IData dramatically reduces development time and integration efforts by enabling developers to move seamlessly between prototype/simulation environments and deployed systems, under both desktop and embedded operating systems. IData's optional IData3D module integrates a mature scene manager into IData. The result is a powerful tool set for the creation of truly innovative 2D/3D applications with unprecedented portability.

QUANTUM3D®

FEATURES:

- Easy-to-use GUI that enables rapid prototyping
- Support for industry-standard OpenGL and its common embedded subsets
- Built-in windowing and control system for dynamic GUIs and command/control screens
- Image file import and display enables use of digital photographs and industry-standard image editor tools
- High-performance 3D scene manager supports industry-standard file formats through optional IData3D module
- Electronic Flight Instrument System (EFIS) symbology support including complex behaviors and live video

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First Silicon Solutions

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www.fs2.com

FS2 Bus Navigator™

The FS2 Bus Navigator™ is used for monitoring signal activity and for debugging complex bus/system interactions in System-on-Chip (SoC) designs. It allows the user to capture bus activity in real time and display critical information for analysis on a host PC for faster debugging and verification of the design.

The system consists of an On-Chip Instrumentation (OCI®) synthesizable logic block, a JTAG hardware probe, and PC-based software for controlling probing and analysis. The OCI transparently captures bus activity, buffers it using on-chip RAM, and transfers the collected data off-chip via a JTAG port to the external JTAG probe. The host PC controls the trace collection process and provides captured bus history to the user with an easy-to-use graphical interface.

The OCI block is synthesized into the SoC design. The OCI block monitors all the bus signals sampled with the processor clock. Signals include address data combined from the read and write data buses, and all critical control and status signals. Additional signals can be hooked up to any nodes in the SoC, such as interrupt requests, peripheral status, and CPU control signals. The additional signals can also be used to recognize specific on-chip activity outside the bus and transmitted to the probe for triggering purposes.
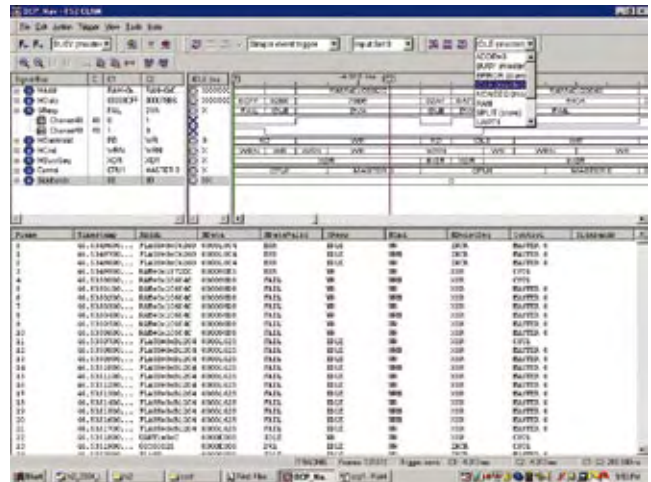
FEATURES:

- Captures bus activity in real time
- Available for custom buses, AMBA, OCP, and Sonics SiliconBackplane buses
- Captures bus signals and additional user-defined inputs attached to other nodes in the SoC
- Bus clock mode trace stores signals on every clock
- Bus transfer mode aligns bus transfers and response phases for single event triggering using combinations of address, data, and control
- Filtering of wait and idle state cycles in bus transfer mode
- Trace storage qualifiers; single cycle, start or stop trace on any trigger, counter, and state sequencer condition
- Configurable for user-defined number of Masters
- Trace buffer stores bus cycles or bus transfers based on RAM memory size
- Up to 16 user-defined triggers recognize combinations of 1, 0, X, signal values
- Sequential event monitoring using cascading trigger states
- User-definable time stamp records duration of each trace frame from the start of trace, displayable as absolute or delta times
- Optional VCD format export for integration with simulation environments

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### FS2 System Navigator EJTAG Debugger for MIPS Cores

The FS2 System Navigator™ EJTAG debugger supports all available MIPS32® and MIPS64® cores from the M4K™ through the latest in the family, the 34K™, with multi-threading capabilities. On-Chip Instrumentation (OCI®) extensions are provided in the MIPS PDtrace™ trace block. Both on-chip and off-chip trace capabilities are integrated into the synthesizable IP model for the core and freely available for the chip designer to implement. This allows FS2 to provide a powerful debug tool with advanced features at a competitive price.

System Navigator is contained in a compact chassis that connects to the target system using a standard 14-pin EJTAG debug connector or 38-pin Mictor connector. Two versions are available. System Navigator supports on-chip trace only requiring some resources in the SoC to capture and store the trace messages on-chip. System Navigator OE (Original Edition), supports both on-chip and off-chip trace features. In off-chip trace capture mode, trace data is streamed off the SoC device and captured in the FS2 system analyzer probe hardware.

The System Navigator is integrated with the GNU-based MIPS SDE software tools with GDB/Insight debugger running on Windows and Linux. All the FS2 tool features are available from the GDB or Insight debugger interfaces. This provides an excellent source-level debugger at a low cost. The probe software is also integrated with the Mentor Graphics Nucleus Edge, Green Hills MULTI, and the Viosoft embedded Linux Arriba debugger. Now you can use the FS2 System Navigator with the best-in-class software tools for an intuitive, easy-to-use interface that fits your application requirements.
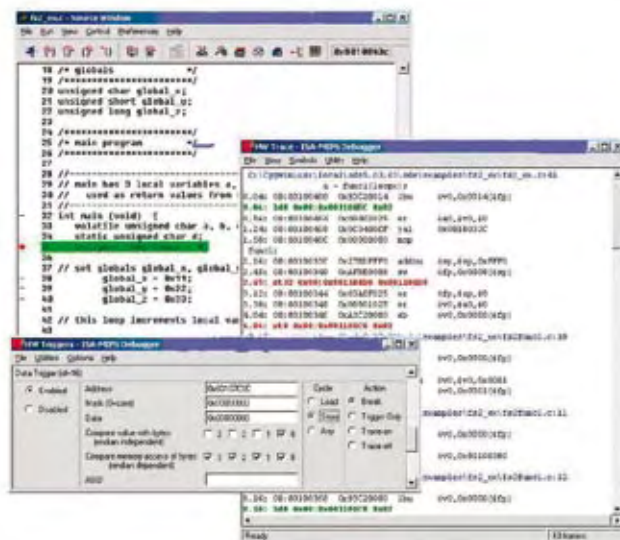
FEATURES:

■ Utilizes On-Chip Instrumentation (OCI®) debug extensions in the synthesizable core

■ Supports all MIPS32® and MIPS64® Cores from M4K™ through 34K™

■ Source-level debug using: GDB/Insight, Mentor Graphics Nucleus Edge, Green Hills MULTI, and Viosoft Arriba

■ On-chip trace and optional off-chip trace

■ Real-time PC execution trace, load/store address, and data trace

■ Trace can be gated on/off by on-chip triggers

■ Scalable internal trace depth or external trace port width and speed

■ Unlimited software breakpoints

■ Single step by assembly or C source line

■ Read-write all CPU registers, and read-write memory whether CPU is stopped or running

■ Flash programming support

■ Multicore debug with multiple MIPS cores; mixed core debug with MIPS and other cores supported as an option

---

For more information, contact: info@fs2.com   **RSC# 31399 @ www.embedded-computing.com/rsc**

Zeligsoft

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Component Enabler

Zeligsoft Component Enabler (CE) is a model-driven development tool designed to minimize the risks that impact cost, time-to-market, and software quality of Software-Defined Radio (SDR) projects developing with the JTRS SCA standard. CE serves as the SCA backbone development tool. It provides a modeling methodology conforming to the SCA standard and abstracts the complexity and intricacy of the SCA rules away from designers. CE validates against the SCA rules and generates correct-by-construction artifacts. By adapting to any project environment, and by working with other best-in-class tools, CE ensures that domain-specific and non-domain-specific software aspects are developed together, integrated early, and executed often, dramatically reducing project risk.
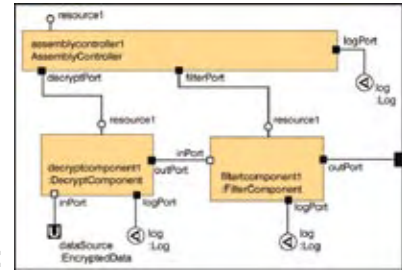
FEATURES:

- Model components, applications, devices, nodes, platforms, deployments; UML 2.0 based; define SCA constructs

- Automatically validate for SCA compliance; import and validate third-party and legacy components, applications

- Push-button generation of XML descriptor files; documentation generation; model and artifacts kept in sync

- Start and stop SCA Core Framework on host within CE environment; load and unload multiple applications; test

- Also available: Zeligsoft Code Generator; industrial strength SCA component code generation; portable code

- Also available: Software-Defined Radio (SDR) Development Suite; complete with SCA operating environment

For more information, contact: info@zeligsoft.com

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MIPS Technologies, Inc.

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Multi-threading

The MIPS32® 34K™ core family is the first series of licensable MIPS cores that offers SoC designers a superior multi-threading solution to boost system performance while significantly reducing overall SoC die area, cost, and power consumption. Single-threaded microprocessors waste many cycles while accessing memory – considerably limiting system performance. The 34K cores are designed to mask the effect of memory latency by increasing processor utilization. As one thread stalls for memory, additional threads are fed into the pipeline, resulting in significant gains in application throughput.

Internal benchmarks indicate that the 34Kc™ core running two threads achieved a 60 percent speed-up over a single-threaded processor with only a 14 percent increase in die size.

FEATURES:

- Based on the proven 24K® processor core microarchitecture, with added DSP and multi-threading extensions

- Significant boost in system performance, with lower die area, costs, and power consumption

- Single development environment and flexible programming models

- Rapid real-time response for embedded applications

- Robust MIPS® Ecosystem provides unparalleled software support and development tools

- OCI available for debug and performance tuning

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CEVA-X DSP

The CEVA-X family of cores is based on CEVA's latest pioneering DSP architecture. This architecture offers best-in-class performance, scalability, and lowest cost of development for DSP deployment.

CEVA-X1620 is the first implementation of the CEVA-X DSP family consisting of 16-bit data width and two MAC units. CEVA-X1620 target markets include 3G cellular handsets and software radio, smart phones/PDAs, video and audio processing for mobile devices, VoIP gateways and broadband modems, and home entertainment (digital TV, HDTV, PVR, HD-DVD).

CEVA-X1622 is the second implementation of the CEVA-X DSP family consisting of 16-bit data width and two MAC units. CEVA-X1622 is a high-performance, low-power, fully synthesizable DSP with enhanced memory architecture including configurable memory size (64 kB or 128 kB), and configurable memory bank organizations in two or four blocks. The flexible memory architecture allows the customer to make an optimal cost/performance selection in line with market needs. CEVA-X1622 target markets include 3G/3.5G cellular handsets and software radio, multimode terminals, smartphones, and VoIP gateways and broadband modems.

The CEVA-X DSP architecture has a unique mix of Very Long Instruction Word (VLIW) and Single Instruction Multiple Data (SIMD) architectures. The VLIW architecture allows a high level of concurrent instructions processing, thus providing extended parallelism, as well as low power consumption.

SIMD architecture allows single instructions to operate on multiple data elements resulting in code size reduction and increased performance. Low power consumption is also achieved in the CEVA-X DSP cores through instructions and dedicated mechanisms such as dynamic and selective units shutdowns and clock slow downs.

CEVA-X1622 design implementations are soft core based, allowing the customer to select the optimal operating point in terms of die size, power consumption, and performance. In addition, the customer has complete flexibility in selecting the foundry, process (for example, 0.13 µ, 90 nm, 65 nm), and complementary IPs.
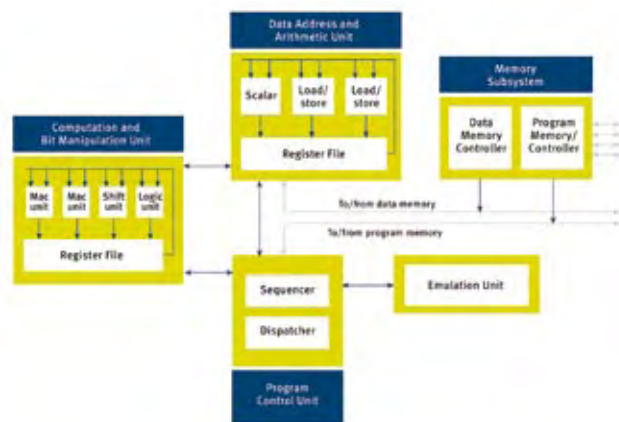
FEATURES:

- Dual MAC 16-bit fixed point DSP
- Combination of VLIW and SIMD architecture concepts
- Up to eight instructions issued simultaneously
- Variable instruction width (16-/32-bit) and variable length of instruction packets
- Two-level memory architecture
- Up to 4 GB addressable memory space
- 64 kB L1 program memory and cache
- 64 kB L1 data memory for CEVA-X1620; 64 kB/128 kB L1 data memory for CEVA-X1622
- Nine-stage pipeline
- All instructions can be conditionally executed

VMETRO

1880 S. Dairy Ashford, Suite 400 • Houston, TX 77077
Tel: 281-584-0728 • Fax: 281-584-9034
www.vmetro.com

Serial FPDP IP

The VMETRO serial FPDP IP core provides support for the full serial FPDP specification, bringing the power of this serial interface to any Xilinx Virtex-II Pro™ FPGA with available RocketIO interfaces.

The core has a light resource usage footprint for each instantiation and a 32-bit internal data interface that is relatively easy to integrate with client FPGA applications, making it an ideal data input/output mechanism for FPGAs running Digital Signal Processing (DSP) algorithms.

The Serial FPDP standard specifies three link speeds: 1.0625 Gbps, 2.125 Gbps, and 2.5 Gbps. The IP core supports all three signaling rates and at the highest link speed provides reliable, sustained data transfer bandwidths of 247 MBps.
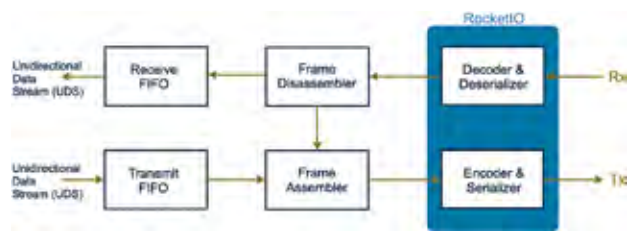
FEATURES:

■ Supported on Xilinx Virtex-II Pro FPGAs

■ Supports 1.0625 Gbps, 2.125 Gbps, and 2.5 Gbps Serial FPDP link operation

■ Complete ANSI/VITA 17.1-2003 implementation allows links to support any Serial FPDP mode

■ 32-bit data + 4-bit control/status back end interface to client application

For more information, contact: info@vmetro.com

RSC# 23649 @ www.embedded-computing.com/rsc

Embedded Planet

4760 Richmond Road • Cleveland, OH 44128
Tel: 216-245-4180 • Fax: 216-292-0561
www.embeddedplanet.com

85xxM

The EP85xxM uses the Freescale PowerQUICC III family to create a full featured PrPMC/Standalone card ready for you to design, develop, and deploy advanced networked devices. The PowerQUICC III family of processors features an integrated e500 PowerPC core and Communications Processor Module (CPM) to provide a scalable computing solution for networked devices. The PowerPC core provides control plane functionality, while the dedicated CPM offloads communications functions such as Gigabit Ethernet, HDLC protocols, and ATM. Embedded Planet supports the EP85xxM with PlanetCore hardware diagnostics, multiple OS options, and an open source bootloader/flash programmer, allowing you to focus on your application. The EP85xxM can be custom configured to meet your needs.

FEATURES:

■ Freescale 85xx processor operating at up to 833 MHz with up to 256 MB of flash, 512 MB DDR SDRAM, 512 kB of NVRAM

■ Operating Modes: Standalone or PrPMC/PT7MC monarch and nonmonarch

■ Connectivity: Two 10/100/1000 Ethernet Ports, RS-232 monitor port, JTAG for debug

■ Serial I2C Devices: EEPROM, temperature sensor, and real-time clock

■ Expansion: Standard PMC connectors, 133 MHz PCI-X Bus

■ Support: PlanetCore Diagnostics, U-boot, Linux, Green Hills INTEGRITY, and VxWorks BSPs

For more information, contact: info@embeddedplanet.com

RSC# 31396 @ www.embedded-computing.com/rsc

AdvancedIO Systems, Inc.

595 Howe Street, Suite 502 • Vancouver, BC V6C 2T5 Canada
Tel: 877-331-7755 • Fax: 604-331-1800
www.AdvancedIO.com

V10x0 XMC Modules

The V10x0 family of mezzanine modules is the industry's first full-production, 10 GbE configurable solution for embedded computing. Utilizing Xilinx® FPGAs, the V10x0 family includes processing modules that perform system functions, such as deep packet inspection, UDP acceleration, up/down conversion, encryption/decryption, and FFT.

The V10x0 family offers extreme scalability for applications requiring 10 GbE, such as: SIGINT, radar/sonar, EW, MILCOM, and wireless infrastructure.

AdvancedIO™ works with customers to achieve solutions that meet their packet processing requirements, and offers consultation for FPGA application development. AdvancedIO™ is partnered with lead system providers and also offers total system solutions.

FEATURES:

- Based on VITA 42 XMC form factor
- Supports Serial RapidIO, PCIe, and PCI-X interfaces
- Supports VxWorks and Linux Operating Systems
- 10 Gb packet processing at line speed
- Common architecture allows for application migration
- Based on Xilinx FPGA technology

For more information, contact: sales@advancedio.com

RSC# 31261 @ www.embedded-computing.com/rsc

Condor Engineering, a Part of GE Fanuc Embedded Systems

101 W. Anapamu Street • Santa Barbara, CA 93101
Tel: 805-965-8000 • Fax: 805-963-9630
www.condoreng.com

EPMC-1553

Condor's EPMC-1553 is the first PCI Mezzanine Card (PMC) module to offer up to eight dual redundant MIL-STD-1553B Notice II channels. Available in commercial, ruggedized, and conductively cooled versions with one, two, four, or eight dual redundant channels, the EPMC-1553 includes advanced Application Programming Interface (API) software that reduces application development time.

Standard features include: transformer coupling; 128 kB of RAM per channel; 45-bit message time tagging; triggers; eight bidirectional avionics-level discretes; eight bidirectional RS-485 differential discretes; support for 66 or 33 MHz PCI bus operation; automatic/manual RT Status Bit and Mode Code responses; programmable or hardwired RT address lines.

FEATURES:

- One, two, four, or eight independent MIL-STD-1553B Notice II dual redundant channels
- All configurations are multifunction with simultaneous Bus Controller, Remote Terminal(s), and Bus Monitor
- Configuration options – either single RT or 31 RT
- CORE-API provided in source code with support for Windows and VxWorks
- Front panel or rear (P14) I/O options
- Complete message programmability

For more information, contact: sales@condoreng.com

RSC# 30750 @ www.embedded-computing.com/rsc

Annapolis Micro Systems, Inc.

190 Admiral Cochrane Drive, Suite 130 • Annapolis, MD 21401
Tel: 410-841-2514 • Fax: 410-841-2518
www.annapmicro.com

Tri XFP I/O Card

Annapolis Micro Systems, Inc. is a world leader in high-performance Commercial Off-the-Shelf FPGA-based processing for radar, sonar, SIGINT, ELINT, digital signal processing, FFTs, communications, software radio, encryption, image processing, prototyping, text processing, and other processing intensive applications.

The Annapolis Tri XFP I/O Card, which works with the WILDSTAR 4/5 Family Architecture, has three 10 Gb individually configured XFP connectors, each with its own XAUI to XFI converter. Industry-standard pluggable fiber optic transceivers can be purchased from Annapolis or from other vendors. The Tri XFP provides up to 30 Gb Full Duplex I/O directly between the outside world and the Rocket I/O pins on the Xilinx Virtex-II Pro or Virtex-4 I/O FPGA on the WILDSTAR 4 main board. No other vendor provides that volume of data straight into the heart of the processing elements and then back out again.

Two I/O cards can reside on each WILDSTAR 4 or WILDSTAR 5 VXS or PCI-X/E board, with up to 30 million user reprogrammable gates.

The Tri XFP card will support 10 Gb Ethernet, 10 Gb Fibre Channel, and OC 192. Although the protocols will be provided as black box solutions with few modifications by users allowed, more adventurous users who choose to develop their own communications protocols from the basics already have access to all the board resources through VHDL source for the interfaces to SRAM, signal conditioners, LAD bus, I/O bus, and PPC flash. CoreFire users will have the usual CoreFire board support package.

The Tri XFP is the first of many I/O cards Annapolis will be releasing for its new WILDSTAR 4/5 Architecture Family, which uses Xilinx Virtex-4 and Virtex-5 FPGAs for processing elements. WILDSTAR 4 is the 10th generation of Xilinx FPGA processing-based COTS boards from Annapolis.

Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customers' applications succeed. We offer training and exceptional special application development support, as well as more conventional customer support.

FEATURES:

- Up to 10 Gb Full Duplex Ethernet per connector
- Up to 10 Gb Fibre Channel
- OC 192
- Three 10 Gb XFP connector
- Accepts industry-standard pluggable transceivers
- Available in both commercial and industrial temperature grades
- Includes one-year hardware warranty, software updates, and customer support
- One or two I/O cards fit on a single WILDSTAR 4/5 processing board
- New I/O form factor for improved thermal performance
- First of many WILDSTAR 4/5 Family I/O cards, including superior performance A/D, D/A, and additional high-speed communication cards
- Save time and effort and reduce risk with COTS boards and software
- Achieve world-class performance; WILD solutions outperform the competition

For more information, contact: jdonald@annapmicro.com

RSC# 31253 @ www.embedded-computing.com/rsc

Diamond Systems Corporation

1255 Terra Bella Avenue • Mountain View, CA 94043
Tel: 650-810-2500 • Fax: 650-810-2525
www.diamondsystems.com

PC/104 I/O Modules

Diamond Systems' extensive PC/104 I/O lineup includes analog and digital I/O, serial communications, and multifunction networking. Our flagship DMM-32X DAQ solution offers 32 16-bit analog inputs, 4 12-bit analog outputs, and 24 DIO lines. Our patented auto-autocalibration technology assures high accuracy across the entire -40 °C to +85 °C operating temperature range. Our new FPGA-based GPIO digital I/O module with 48 DIO lines and 10 counter/timers can be easily customized with new FPGA code. Our popular line of four- to eight-port multiprotocol serial communications boards includes the new EMM-8P with software protocol configuration. And our new Janus dual CAN board hosts both GPS and Wireless Modem Modules. All are supported by our Universal Driver with wide OS support.

FEATURES:

■ Patented auto-autocalibration provides highest accuracy A/D across the full operating temperature range

■ Range of DAQ solutions with up to 32 16-bit inputs at 250 kHz, 1,024 sample FIFO, 4 12-bit outputs, and 24 DIO

■ FPGA-based digital I/O module with 48 DIO and 10 counter/timers enables easy customization/reconfiguration

■ Four- to eight-port multiprotocol serial communications modules offer RS-232/422/485 with flexible configuration

■ Multifunction networking module with dual CAN controllers supports GPS and Wireless Modem Modules

■ Rugged, long life, +5 V only modules with -40 °C to +85 °C operating temperature range and broad software support

For more information, contact: sales@diamondsystems.com

RSC# 30772 @ www.embedded-computing.com/rsc

ICS Sensor Processing

296-300 Concord Road, Corporate Center, Suite 120
Billerica, MA 01821
Tel: 703-263-1483/800-368-2738 (Toll Free) • Fax: 703-263-1486
www.ics-ltd.com

ICS-8554 and 8552

The ICS-8554 four-channel rugged IF receiver and the ICS-8552 two-channel rugged IF receiver are designed for Software-Defined Radio (SDR) applications in demanding environments. The products include two Graychip GC4016 DDC devices and a 3M gate Xilinx Virtex-II FPGA. The majority of FPGA resources are free for user-defined digital signal processing algorithms.

The ICS-8552 brings high performance to standalone, man-pack applications by including a high-stability (1 PPM) onboard TCXO in addition to two ADC/DDC FPGA channels. The ICS-8554 trades the TCXO for two additional ADCs and is intended for higher channel count in vehicle-mounted systems where a high-precision clock source is externally supplied.

FEATURES:

■ Four ADC channels, 14 bits @ 105 MHz, and two ADC channels, 14 bits @ 105 MHz (ADS5424)

■ Two Graychip 4016 DDC ASICS and 3M gate Xilinx Virtex-II FPGA

■ ICS-8552 – 1PPM Temperature Compensated Crystal Oscillator (TCXO) onboard

■ 2 MB of FIFO storage

■ Pn4 user I/O supports LVTTL or LVDS signaling levels

■ Windows, Linux, and VxWorks device drivers

For more information, contact: sales@ics-ltd.com

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www.embeddedplanet.com

EMBEDDEDPLANET™

EP8548A

The EP8548A is the answer to rapidly developing and deploying high-performance Serial RapidIO based AdvancedTCA and MicroTCA applications. You have a choice of operating systems and custom hardware diagnostics letting you focus on your application development and getting to market first.

The EP8548A is a single-width, full-height AdvancedMC processor board with a low-power, high-performance Freescale MPC8548E processor operating at up to 1.33 GHz and Serial RapidIO fabric connection. In addition to the AdvancedMC configuration the EP8548AMC can operate as a standalone module and boot from onboard flash allowing for rapid application development outside of the integrated AdvancedTCA or MicroTCA environment. For fabric connectivity the EP8548A is compliant with the AMC.4 specification for Serial RapidIO fabric interfaces, but is also built for flexibility. PCI Express and Gigabit Ethernet connections are also routed to the AdvancedMC connector to simplify testing and integration of additional SERDES interfaces.

At the heart of the EP8548AMC is a Freescale MPC8548E PowerQUICC III processor. The MPC8548E is a highly integrated System-on-Chip (SoC) platform that includes a PowerPC core, an integrated security engine, integrated Serial RapidIO, PCI Express, and Gigabit Ethernet controllers, double precision floating-point support, and a DDRII memory interface. The integrated security engine ensures that encryption doesn't slow down your application. The highly integrated SoC architecture improves system performance, simplifies board design, lowers power consumption, and reduces cost.

The EP8548A includes a Module Management Controller (MMC) built from a 32-bit Freescale ColdFire processor. The MMC supports the Intelligent Platform Management Interface (IPMI) and allows for independent management and monitoring of the EP8548AMC board. Embedded Planet also supports the EP8548A with PlanetCore hardware diagnostics, multiple OS options, and an open source bootloader and flash programmer, allowing you to focus on your application. Like all Embedded Planet products the EP8548A can be custom configured to meet your needs.

FEATURES:

- AMC.0 and AMC.4 compliant design for simple inclusion in Serial RapidIO fabric-based AdvancedTCA systems
- Operates in standalone mode with included power supply to simplify and accelerate early application development
- Freescale PowerQUICC III MPC8548 operating at up to 1.33 GHz delivering an estimated 3065 MIPS (Dhrystone 2.1)
- Integrated security engine supporting DES, 3DES, MD-5, SHA-1/2, AES, RSA, RNG, Kasumi F8/F9, and ARC-4 encryption algorithms
- One Gigabit Ethernet to front RJ-45 connector and three Gigabit Ethernet connections to rear AdvancedMC connector for the AdvancedTCA base interface
- Configurable x4 and x8 PCI Express signals to Zone 3 of the AdvancedMC connector, allowing for simplified testing of PCI Express
- Single SODIMM slot with DDR2 interface for high-bandwidth RAM access and 16 MB of onboard flash
- Front-panel RS-232 connection available for direct module management interface
- Onboard JTAG connection to simplify development and debugging of software applications
- Software support includes: PlanetCore Hardware Diagnostics, U-Boot Bootloader, Linux, INTEGRITY, and VxWorks Board Support Packages
- Complete AdvancedTCA development systems available including AdvancedTCA carrier boards, chassis, and multiple AdvancedMC cards

For more information, contact: info@embeddedplanet.com   **RSC# 23603 @ www.embedded-computing.com/rsc**

Emerson Network Power, Embedded Computing

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Tel: 608-831-5500 • Fax: 608-831-4249
www.artesyncp.com

EMERSON.
Network Power

Formerly Artesyn Technologies

KosaiPM

Advanced Mezzanine Card (AdvancedMC) is a collaboration of major telecom OEMs and suppliers to create an optimal expansion platform for AdvancedTCA or proprietary baseboards that addresses major bandwidth, availability, field upgradeability, cost, scalability, management, and interoperability issues.

KosaiPM is an AdvancedMC module based on the Intel Pentium M processor, providing a complete processor subsystem. It is designed to allow communication equipment manufacturers to add modular and upgradeable compute functionality to their AdvancedTCA or proprietary baseboards and provide the localized horsepower necessary for applications such as protocol processing, packet processing, data management, and I/O management.

To support high-speed packet data transfers on and off the card, KosaiPM features both PCI Express and dual GbE interfaces to the baseboard. With ever-increasing application and data transfer requirements, this combination of more traditional GbE interfaces and the emerging PCI Express interface allows developers to easily migrate existing applications to PCI Express.

KosaiPM is hot swappable, which allows modules to be replaced by operators or service organizations in the field without bringing down an entire AdvancedTCA blade or system. This reduces costs and Mean Time to Repair (MTTR), lowering both CAPEX and OPEX. KosaiPM also provides an IPMI-based system management interface, which enables operators to pinpoint and fix problems at the module level, also lowering MTTR and OPEX.

FEATURES:

- Intel Pentium M® running at up to 1.8 GHz
- Full-height and half-height PICMG AdvancedMC form factor
- Up to 2 GB DDR DRAM with ECC
- 256 MB onboard USB flash device
- Dual GbE connectivity to baseboard
- PCI Express connectivity to baseboard
- Full hot-swap support
- USB and console serial ports via front panel
- Intelligent peripheral management functionality
- Carrier Grade Linux support
- RoHS/WEEE compliant configuration available in 2006
- Quality assured by more than 30 years of design experience and a TL-9000 and ISO 9001:2000 certified quality management system (FM 26789)

Innovative Integration
2390-A Ward Avenue • Simi Valley, CA 93065
Tel: 805-578-4260 • Fax: 805-578-4225
www.innovative-dsp.com

DR PMC/XMC Digital Receiver

The DR PMC/XMC Digital Receiver PMC card features 16 receiver channels on one card using the most advanced architecture for ultrafast signal capture and real-time processing. It integrates the latest analog chips with a 4M Virtex-II Pro FPGA for user code, ample memory, and flexible clocks/triggers on a 64/66 PCI mezzanine format.

High-speed digital signal processing algorithms in the FPGA are developed using MATLAB and VHDL code. The FPGA framework logic allows quick integration of custom signal processing into the dataflow of the module through use of component-based modular design. DSP algorithms are rapidly designed using high-level MATLAB simulations that can be integrated into the FPGA hardware with minimal VHDL coding.

FEATURES:

■ 16 Channel Digital Receiver, 4 A/D 125 MHz

■ Virtex-II Pro FPGA, 4 million gates

■ PCI 64/66 with P4 port to host card

■ 16 MB SDRAM plus 2 MB RAM for FPGA

■ Low-jitter PLL clock source

■ Advanced SW and firmware demo programs

For more information, contact: sales@innovative-dsp.com

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Innovative Integration
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www.innovative-dsp.com

TX VelociaPMC

The TX VelociaPMC transmitter card features the most advanced architecture for ultrafast signal generation and real-time processing in wideband radio systems and similar wide spectrum applications. It integrates the latest analog circuit chips with a large FPGA for user code, ample memory, and flexible clocks/triggers on a 64/66 PCI mezzanine format. Novel features include a combination of large, user-programmable FPGA, 1 GSPS DACs, onboard low-jitter PLL clock, Sync Burst RAM dedicated to FPGA for fast, block-oriented processing, and a direct PMC/XMC J4 DIO connection to the host card. This 64-bit J4 interface offers a 1.6 GBps transfer-capable, low-latency connection to Innovative Integration's Velocia series of DSP and FPGA CompactPCI boards.

FEATURES:

■ Four AD9779, 16-bit, 1 GSPS converters

■ Virtex-II Pro FPGA, 4 million gates

■ PCI 64/66 with P4 port to host card

■ Low-jitter PLL clock source

■ Advanced SW and firmware demo programs

For more information, contact: sales@innovative-dsp.com

RSC# 31402 @ www.embedded-computing.com/rsc

Innovative Integration
2390-A Ward Avenue • Simi Valley, CA 93065
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www.innovative-dsp.com

UWB

The UWB Receiver PMC/XMC card features the most advanced architecture for ultrafast signal capture and real-time processing in wideband radio systems and similar wide spectrum applications. It integrates two 250 MSPS, 12-bit A/D channels with a large FPGA for user code, ample memory, and flexible clocks/triggers on a PMC/XMC mezzanine format. The UWB has a Xilinx Virtex-II Pro FPGA for signal processing that may be quickly customized using Innovative's Framework Logic in VHDL or in the MATLAB Simulink graphical environment. Large on-card memories for data capture and analysis, a flexible clocking structure, and 1 GBps connectivity to host DSP cards make the UWB a powerful front end to many applications.

FEATURES:

- Two LTC2224, 12-bit 250 MSPS converters
- Virtex-II Pro FPGA, 4 million gates
- PCI 64/66 with Pn4 port to host card
- XMC – 1 GBps full-duplex rates per VITA 42
- 64 MB SDRAM plus 2 MB RAM for FPGA
- Sample clocks: Dual external or on-card PLL

For more information, contact: sales@innovative-dsp.com

RSC# 31401 @ www.embedded-computing.com/rsc

Interphase Corporation
2901 N. Dallas Parkway, Suite 200 • Plano, TX 75093
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www.iphase.com/forward/3639.jsp

iSPAN® 3639

The Interphase iSPAN® 3639 AdvancedMC multiprotocol T1/E1/J1 communications controller delivers best-in-class communications I/O for next-generation telecom equipment. With its software-selectable interfaces and a powerful onboard MPC8560 processor, the 3639 provides the functionality necessary for migrating applications to next-generation networks while preserving investments in legacy technologies. Robust software development tools, a comprehensive SS7 Layer 1/Layer 2 and iTDM protocol software suites make the 3639 a powerful solution for decreasing costs and time to market for telecom integration projects. Applications include: GGSNs, HLRs, soft switches, DSLAMs, SGSNs, routers, media gateways, wireless base stations, BSCs/RNCs, and BTS/Node Bs.

FEATURES:

- Freescale MPC8560 (PowerQUICC III™) onboard processor at 800 MHz
- Four or eight individually software-selectable T1/E1/J1 interfaces
- Onboard FPGA for media termination and transport; support for iTDM or UDP/IP encapsulation
- Onboard support for multiple network protocols and interworkings: Q.SAAL/GR-2878, SS7, frame relay, HDLC, and ATM
- Preintegrated protocol stacks available using Interphase lower layers and various third-party upper-layer stacks
- Telecom clock management; master or slave synchronization

For more information, contact: fastnet@iphase.com

RSC# 22267 @ www.embedded-computing.com/rsc

Technobox, Inc.

140 Mount Holly Bypass – Unit 1 • Lumberton, NJ 08048
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www.technobox.com

3923 FlexATX Processor PMC (PrPMC)

The 3923 is a FlexATX Processor PMC (PrPMC) carrier and development platform. This carrier board provides two PMC sites plus three PCI card slots (two 64-bit and one 32-bit). Using the 3923, a designer can work with a single PrPMC, dual PrPMCs, or a PrPMC and PMC for hardware and/or software development. All PCI slots are keyed for 3.3 V signaling. The PCI bus will run at 66 MHz, if all PCI cards assert 66 MHz enabled. At least one PMC site must be populated with a PrPMC running in Monarch mode. Site A's rear I/O is directed to connectors for a floppy disk and/or external IDE device. Each site has a fan to cool the mounted PrPMC or PMC.

FEATURES:

■ FlexATX platform for PrPMC development and/or delivery

■ Dual PMC sites enable various configurations with PrPMCs and PMCs

■ Slots for three PCI cards (two 64-bit, one 32-bit), rear I/O access for external IDE or floppy drive

■ Auxiliary cooling for PMC sites

■ LED status for memory, configuration, I/O access, power, PCI interrupt, and bus mastering activity

■ Site B rear I/O is directed to a DIN connector that emulates P2 of a VMEbus board

For more information, contact: info@technobox.com

RSC# 13761 @ www.embedded-computing.com/rsc

Technobox, Inc.

140 Mount Holly Bypass – Unit 1 • Lumberton, NJ 08048
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www.technobox.com

4383

This PCI-X capable board provides four 1.5 Gbps links to support as many as four cable-attached SATA devices. Although designed for PCI-X, the 4383 will also function with lower-speed 33/66 MHz buses and in 32/64-bit modes. It supports 3.3 V and 5 V bus signaling. Four SATA ports are front-panel accessible. Each port has a retention mechanism. Status LEDs show link activity. BIOS is stored in EEPROM, accessible via a Serial Peripheral Interface (SPI) bus.

FEATURES:

■ Supports four SATA devices (1.5 Gbps per link)

■ Intel 31244 controller

■ PCI-X capable (33/66 MHz, 32/64-bit modes; 3.3 V and 5 V bus signaling)

■ Status LEDs show link activity

■ Onboard BIOS (EEPROM)

For more information, contact: info@technobox.com

RSC# 24219 @ www.embedded-computing.com/rsc

Technobox, Inc.

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www.technobox.com

4435

This Quad 10/100-TX Ethernet Adapter, which is built around Intel 82551ER Ethernet controllers, provides four Ethernet connections. The Quad's configuration options allow either front-panel connectiviy via RJ-45 connectors or rear I/O accessibility using a VITA 36 PIM module (for example, Technobox P/N 4516). The 82551ER Ethernet controllers feature an integrated MAC and PHY for operating at either 10 Mbps or 100 Mbps (full-duplex). Each controller connects to the 32-bit, 66 MHz PCI bus through a PLX 6150B bridge and appears as an independent device on the bus. A dual-color LED (one for each port) provides indication of link mode/status and activity.

FEATURES:

■ Four 10/100-TX Ethernet ports, using Intel 82551ER Ethernet controllers

■ Full-duplex operation at both 10 Mbps and 100 Mbps

■ PLX 6150B PCI bridge (32/64-bit, 33/66 MHz)

■ Front-panel I/O via RJ-45 interface

■ Rear I/O access supported using PIM (for example, Technobox P/N 4516)

■ Dual-color LEDs provide indication of link mode/status

For more information, contact: info@technobox.com   **RSC# 22639 @ www.embedded-computing.com/rsc**

Technobox, Inc.

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www.technobox.com

Technobox P/N 4792

The conduction-cooled, 32-channel, reconfigurable RS-422/485 digital I/O PMC provides a vehicle for implementing complex user-specific digital designs requiring a differential interface. Thirty-two general-purpose RS-422/485-driven digital I/O differential pairs are wired to the rear PN4 connector. For each of the 32 channels, the bidirectionality is controlled by an output from the FPGA. This product is a conduction-cooled version of the P/N 4289 board. All features of the 4289 are retained, except the ICS1522 PLL has been eliminated in favor of Cyclone internal PLLs, and the differential I/O is available at PN4 only. For ease of migration, the Cyclone BGA pinout is the same as on the 4289 board.

FEATURES:

■ 32 channels of general-purpose RS-485/422 digital I/O

■ Conduction-cooled, industrial temperature

■ 64-bit/66 MHz PCI

■ Altera 12 K logic element FPGA

■ Reprogrammable by host, onboard flash, or byte blaster cable

■ Sample FPGA design and host C code

For more information, contact: info@technobox.com   **RSC# 30696 @ www.embedded-computing.com/rsc**

THEMIS
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Tel: 510-252-0870 • Fax: 510-490-5529
www.themis.com/prod/hardware/ta64.htm

Themis TA64™

TA64 is the first in a new family of 6U VMEbus com-
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processor. It is compatible with Themis' USPIIe-USB™
SBC, at the application level, and features front-panel
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tion provide a performance boost with minimal or no
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configurations offering a wide range of I/O and perfor-
mance options.

FEATURES:

■ Themis' new family of 6U VMEbus AMD processor-based SBCs
■ AMD Turion 64 Mobile processor running at 1.6 GHz
■ Memory – Up to 4 GB ECC DDR333 SDRAM
■ Low 38 W power dissipation (without PMC)
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■ For full information: Contact Themis at info@themis.com or call
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www.themis.com/prod/hardware/tppc64.htm

Themis TPPC64™

The TPPC64 is the industry's first commercially avail-
able 6U VMEbus computer family based on the IBM®
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applications and new 64-bit applications.

The TPPC64 is available in single-slot uniprocessor and
two-slot, dual symmetric multiprocessing configura-
tions. I/O extension and graphics boards added to
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additional VMEbus slots. The TPPC64 includes two GbE
ports and dual Ultra320 SCSI channels. I/O expansion is
supported via a PCI riser. PMC I/O can be expanded to
four slots with two different PMC carrier boards.

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FEATURES:

■ IBM PowerPC 970FX processor – 1.8 GHz clock rate in single and
dual processor configurations
■ Up to 4 GB of DDR400 SDRAM memory
■ Two Gb Ethernet ports, two USB ports, two serial ports, and one
SCSI port on front panel
■ Carrier board PCI expansion supports up to three additional PMC
slots
■ Support for Linux® OS
■ Rugged design for reliability in harsh operating environments –
up to 30 G shock

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VMETRO

1880 S. Dairy Ashford, Suite 400 • Houston, TX 77077
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www.vmetro.com

PMC-FPGA05 Module

The PMC-FPGA05 is a Xilinx Virtex-5 XC5VLX110 platform FPGA-based, PMC module with high-speed digital I/O and PCI-X interface to the host computer. Three banks of 2 Mb x 18 (4 MB) QDR II SRAM support DSP functions in the Virtex-5. Two independent banks of 512 Mb x 16 (64 MB) DDR2 SDRAM are directly connected to the FPGA. There are 138 signals routed to a 180-way connector near the front panel. These lines are routed so that they may be used as single-ended signals or differential pairs. I/O modules available include ADC, DAC, LVDS, FPDP II, CameraLink, and RS-422.

Example VHDL code blocks are provided to show how the PMC-FPGA05 resources can be used, along with utilities for configuring flash. The PMC-FPGA05 is supported under Windows XP.

FEATURES:

■ Xilinx Virtex-5 LX110 FPGA
■ Multiple banks of SRAM for DSP
■ Multiple banks of SDRAM for large buffers
■ Customizable digital I/O or choose an I/O module for ADC, DAC, LVDS, FPDP II, CameraLink, or RS-422
■ PCI-X interface
■ Windows XP support

For more information, contact: info@vmetro.com   RSC# 30636 @ www.embedded-computing.com/rsc

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SFM Quad sFPDP

The SFM uses highly integrated FPGA technology to provide one, two, or four channels of fast, low-latency, point-to-point ANSI/VITA 17.1-2003 Serial FPDP in an XMC/PMC module. Each independent channel supports the standard sustained Serial FPDP data rates of 1.0625 Gbps, 2.125 Gbps, and 2.5 Gbps through front-panel fiber optic transceivers. Each channel may be operated as a Serial FPDP transmitter or receiver. Smooth dataflow is ensured using a 256 MB pool of DDR2 SDRAM to provide each data stream with 64 MB of FIFO buffering.

An FPGA-based PCI Express x8 core provides the module with a host interface through the XMC connector. Each PCI Express lane supports data rates of 2.5 Gbps bidirectionally.

FEATURES:

■ One, two, or four 2.5 Gbps fiber optic transceivers fitted as standard
■ Supports 1.0625 Gbps, 2.125 Gbps, and 2.5 Gbps serial data rates
■ 64 MB DDR2 SDRAM buffering per channel
■ XMC supports 2.5 Gbps PCI Express or PMC supports 133 MHz PCI-X
■ All SFPDP topologies are supported including: simple point-to-point, copy, and copy/loop modes
■ Windows 2000/XP, VxWorks, and Linux support

For more information, contact: info@vmetro.com   RSC# 30061 @ www.embedded-computing.com/rsc

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Emerson Network Power's new Embedded Computing business is anchored by recently acquired Artesyn Communication Products. It enhances Emerson's global capabilities to offer more comprehensive, highly integrated and reliable platform solutions.

Artesyn Communication Products' rebranding as Emerson Network Power's Embedded Computing business builds on the company's innovative work in the open architecture telecom platform industry. The formation makes it possible for telecom equipment manufacturers (TEMs) and network equipment providers (NEPs) to reduce their development cost and time to market.

The new business will offer telecom components, blades, software and systems to equipment markets in a broad range of telecom infrastructure applications, including network access, soft switches, signaling systems, and media gateways. These products, based on industry standards make it easier for TEMs and NEPs to outsource their platform design and focus precious engineering resources on value-added applications and services.

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AMD64 Technology

Balance between processor performance, I/O bandwidth, and power consumption are major concerns to high-end embedded systems architects. AMD currently offers three different AMD64 processor families – Mobile AMD Sempron™, AMD Opteron™, and AMD Turion™ 64 processors – providing design flexibility on an industry-standard platform for high-end embedded systems. With the AMD64 Longevity Program, system architects gain the confidence that the processor they choose will be there throughout the life of their embedded design.

These 32- and 64-bit x86 processor families help high-end embedded designers meet existing and next-generation design requirements with a highly scalable x86 platform. Direct Connect Architecture helps reduce the bottlenecks of traditional systems as memory is directly connected to the CPU to optimize memory system performance; I/O is directly connected to the CPU for more balanced throughput; CPUs are directly connected allowing for latency reduction between processors.

An integrated 128-bit wide DDR DRAM memory controller allows direct access of main memory, scales with each additional CPU, and increases bandwidth while reducing memory latencies.

HyperTransport provides a scalable, low-power bandwidth interconnect between processor, I/O subsystems, and other chipsets with up to 8.0 GBps per link and supports PCI, PCI-X, PCI Express, InfiniBand, and 10 Gigabit Ethernet. System architects can also gain direct access to AMD64 expertise and comprehensive engineering support services through AMD's Professional Design Support Services, which has helped many AMD customers bring complex embedded and multiprocessor systems to market quickly and effectively.

Imagine it. Build it. Bring it to market with AMD64 Embedded Solutions.
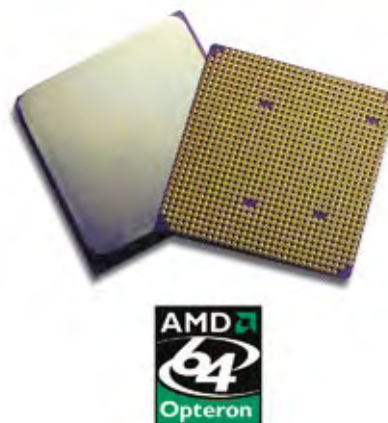
FEATURES:

- Mobile AMD Sempron™ processors: 32-bit; 25 W; 1.8 or 2.0 GHz; 1 MB L2 cache; 64/72 ECC DDR unbuffered memory; lidless 754-pin uPGA pkg

- AMD Turion™ 64 processors: 32- and 64-bit; 25 W; 2.0 GHz; 1 MB L2 cache; 64/72 ECC DDR unbuffered memory; lidless 754-pin uPGA pkg

- AMD Opteron™ processors: 32- and 64-bit; available in a power range of 30-95 W; with a core frequency range of 1.4-2.6 GHz; 1 MB L2 cache; up to three HyperTransport links per CPU; dual 64/72 DDR registered DIMMs, ECC, and Chip Kill in a lidded 940-pin uPGA pkg

- Dual-core AMD Opteron™ processors are offered at core frequency of 1.8 GHz with 1 MB L2 cache per core

- AMD64 embedded products can provide support for CompactPCI, AdvancedTCA, and other industry-standard telecommunications platforms

- Storage, imaging, military/COTs, and other embedded or ruggedized platforms can benefit from the system efficiencies of AMD64

Intel Corporation

2200 Mission College Blvd. • Santa Clara, CA 95052
Tel: 916-356-3104/800-628-8686
**www.intel.com/design/intarch**

(intel)®

Intel® Core™ Duo Processors

Intel® Core™ Duo processors are members of Intel's growing product line of multicore processors. These dual-core processors combine the benefits of two high-performance execution cores with intelligent power management features to deliver significantly greater performance-per-watt over previous Intel® processors. Intel's 65 nm process technology makes it possible to integrate two cores, along with many advanced features, in one physical package.

Intel Core Duo processors meet the needs of a wide range of low-power embedded applications such as interactive clients and industrial automation equipment. While incorporating advanced processor technology, they remain software-compatible with previous 32-bit Intel® architecture processors. Intel Core Duo processors integrate two execution cores derived from the Intel® Pentium® M processor, whose power efficiency is enabled through significant hardware architecture enhancements in stack management, instruction execution, and branch prediction. Integrating two execution cores enables Intel Core Duo processors to provide significant performance improvements while remaining in a thermal envelope that is similar to existing Intel Pentium M processors.

Intel Core Duo processors are validated with the Mobile Intel® 945GM Express chipset. This chipset provides greater flexibility for developers of embedded applications by offering improved graphics and increased I/O bandwidth over previous Intel® chipsets, as well as remote asset management capabilities and improved storage speed and reliability. Intel's comprehensive processor/chipset validation process enables fast deployment of next-generation platforms to help developers maximize competitive advantage while minimizing development risks.
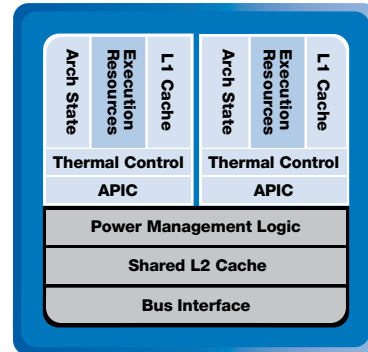
667 MHz Front-Side Bus

Configuration of the Intel® Core™ Duo processor shows two complete execution cores and shared L2 cache. Intelligent power management features deliver significantly greater performance-per-watt over previous Intel® single-core processors.

FEATURES:

■ Two complete execution cores in one processor package support multithreading and multitasking environments

■ Dual-core processing efficiently delivers performance while balancing power requirements

■ Two execution cores share a high-performance, power-optimized 667 MHz front-side bus to access the same chipset memory

■ Enhanced Intel SpeedStep® technology helps decrease average power consumption and heat production

■ Intel® Smart Cache Design allows two execution cores to share 2 MB of L2 cache, reducing FSB traffic and enhancing system responsiveness

■ Intel® Advanced Thermal Manager supports new digital temperature sensors and thermal monitors to enhance thermal monitoring accuracy

■ Streaming SIMD Extensions 3 (SSE3) provides significant performance enhancement for multimedia applications

■ Additional instructions help improve thread synchronization, complex arithmetic, graphics, and video encoding

■ Fully code compatible with existing Intel architecture-based 32-bit application software

■ Utilizing Intel® Dynamic Power Coordination, application software or OS support balanced platform performance and power dissipation

■ Embedded life-cycle support protects system investment by enabling extended product availability for embedded and communications customers

■ A strong ecosystem of hardware and software vendors (intel.com/go/ica) helps developers reduce costs and shorten time to market

For more information, contact: www.intel.com/design/intarch **RSC# 31256 @ www.embedded-computing.com/rsc**

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Dual-Core Intel® Xeon® Processor LV 2.0

The Dual-Core Intel® Xeon® processor LV 2.0 GHz is a member of Intel's growing product line of multicore processors, delivering significantly greater performance-per-watt over previous single-core Intel® Xeon® processor-based platforms.[1] Two cores in one physical package support increased blade density, making it particularly attractive for AdvancedTCA* form factor designs, as well as CompactPCI*, COM Express, and custom-bladed and rack-mounted designs. A high-performance 667 MHz Front-Side Bus (FSB) provides dual-processor support for demanding multithreaded and multitasking usage environments.

Based on Intel 65nm process technology, this processor combines the benefits of dual-core with dual-processor capabilities to provide four high-performance cores per platform. This dual-core/dual-processor capability provides ideal solutions for a wide range of low-power embedded, storage, and communications applications such as Storage Area Networks (SANs), Network Attached Storage (NAS), routers, Virtual Private Networks (VPN), ruggedized small form factor systems, intrusion detection systems, and telecommunications (wireless and wireline) servers. While incorporating advanced processor technology, this dual-core processor remains software-compatible with previous 32-bit Intel® Architecture processors.

The Dual-Core Intel Xeon processor LV 2.0 GHz is validated with the widely deployed Intel® E7520 chipset featuring high bandwidth for increased memory and I/O throughput, PCI Express*, and serial I/O technology. Enhanced 36-bit memory addressing supports up to 16 GB of DDR2 memory. Intel's comprehensive processor/chipset validation process enables fast deployment of next-generation platforms to help developers maximize competitive advantage while minimizing development risks.

[1]Benchmark tests demonstrate significant gain in performance and performance-per-watt, when comparing the Dual-Core Intel® Xeon® processor LV 2.0 GHz to previous single-core Intel® Xeon® processors. (See intel.com/design/intarch/prodbref/311375.htm)

*Other names and brands may be claimed as the property of others.

FEATURES:

- Two complete execution cores in one processor package support multithreaded applications and multitasking environments
- Dual-core processing efficiently delivers performance while balancing power requirements
- High-performance 667 MHz FSB provides dual processor support for demanding, high-performance, volume applications
- Supports up to four simultaneous threads on system
- Dynamically adjusts processor voltage and core frequency, decreasing average power consumption and average heat production
- Intel® Smart Cache Design allows two execution cores to share 2 MB of L2 cache, reducing FSB traffic and enhancing system responsiveness
- Intel® Advanced Thermal Manager supports digital temperature sensors and thermal monitors on each execution core
- Streaming SIMD Extensions 3 (SSE3) provides significant performance enhancement for multimedia applications
- Fully code compatible with existing Intel architecture-based 32-bit application software
- Enhanced 36-bit memory addressing supports up to 16 GB of DDR2 memory when paired with the Intel® E7520 chipset
- Embedded life-cycle support protects system investment by enabling extended product availability
- A strong ecosystem of hardware and software vendors (intel.com/go/ica) helps developers reduce costs and shorten time to market

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Jacyl Technology, Inc.

P.O. Box 350 • Leo, IN 46765
Tel: 800-590-6067 • Fax: 260-471-6067
www.jacyltechnology.com

CM-256

The CM-256 is an embedded memory module designed for integration into a larger system. The CM-256 features a total of 256 MB of 133 MHz Micron SRAM and 32 MB of Intel flash on a miniature 50 mm x 46 mm circuit board. The CM-256 is uniquely designed with two individual address and data bus configurations. One address and data bus is connected to 128 MB of SRAM and the 32 MB of flash. The second address and data bus is connected to the remaining 128 MB SRAM. This custom layout provides the greatest flexibility for incorporation into larger systems requiring multiple individually controlled memory banks. All control line for each individual memory IC is available to the user. The CM-256 only requires a signal 3.3 Vdc power source.

FEATURES:

■ Total of 256 MB of 133 MHz Micron SRAM and 32 MB of Intel flash

■ Memory is devided between two individual address and data buses

■ A complete microprocessor system memory solution in a miniature size, 46 mm x 50 mm

■ Control signals for each individual memory are available at the interface header pins

■ Only requires a single 3.3 Vdc source

■ Available in industrial temperature range

For more information, contact: sales@jacyl.com   **RSC# 31405 @ www.embedded-computing.com/rsc**

## Vesta Technology, Inc.

11049 W. 44th Avenue, Suite 100 • Wheat Ridge, CO 80033
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www.vestatech.com/pg

Antero

The Antero controller from Vesta Technology is optimized for embedded control applications. Based on 32-bit ARM7 technology, it offers high performance with low power, small size, and low cost. It features a rich I/O set that includes Ethernet, CANbus, USB, IRDA, I2C, SPI, serial, PWM, quadrature, analog, and digital. Antero is ideal for machine and industrial control, equipment monitoring, process control, instrumentation, and many other applications.

The Antero Development Kit provides everything needed to develop your application. It includes the processor module, baseboard with connections to the many I/O ports, power supply, and enclosure. It also includes a royalty-free RTOS and a complete development environment with GNU/GCC compiler.
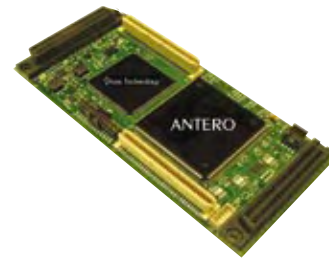
FEATURES:

■ Single board computer based on Philips LPC2292 ARM7 32-bit microcontroller running at 60 MIPS

■ I/O: CANbus x2, Ethernet, USB, IRDA, I2C, SPI, RS-232 x3, RS-485, PWM x16, quadrature, analog x10, digital x24

■ Rugged – including operation over the industrial temperature range (-40 °C to +85 °C)

■ Very low power; calendar and alarm functions in very low-power standby; suitable for battery operation

■ Processor is implemented as an Industry Pack Standard mezzanine board (1.8" x 3.9")

■ Onboard memory options include 1-16 MB flash and 1-8 MB RAM

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Improving code migration and reuse

By Robert Day

As the amount of embedded software grows, an organization's ability to generate, debug, and test it becomes more difficult. Software groups must be able to reuse as much code as possible from both their own previous designs and from commercial and open source avenues. Robert considers what tools, methodologies, and practices can be utilized to make reuse and code migration possible and some complex applications where software black boxes can help.

The combination of processing power increases and the additional features, functionality, and connectivity of today's embedded devices has expanded software content dramatically. However, time-to-market pressures have also increased, and while the software side has not provided magic answers to generate this new mountain of code, a number of practices, standards, and tools can help.

Often as new features are required in products, *make versus buy* issues must be considered. As an example, consider an embedded product that must be networked in its next generation, requiring a software TCP/IP stack. The dilemma then is whether to:

- Hire networking specialists to write the stack
- Outsource to some networking specialists
- Buy a TCP/IP stack and integrate it
- Find an open source networking stack and integrate it

The options all have cost and time implications, and for most situations, a combination of acquiring some software and gaining some expertise in that arena is the most efficient, timely, and cost-effective route.

When porting applications or creating the next generation of device, the more software that can be reused, the greater chance the software will be ready on time and work properly. Reusable software Intellectual Property (IP) can take many forms, but it essentially equates to software building blocks or components that have been used before and hence have a built-in reliability and modularity that allows for ease of implementation into new designs. It is now common for embedded software designs to have many software IP blocks; some proprietary to the developer's organization and often specific to the embedded application itself; some commercially acquired general purpose IP such as Real-Time Operating Systems (RTOSs) and networking stacks; and some specific applications such as databases and Web browsers. All of this IP must be brought together, integrated, and tested.

Higher-level programming languages

Most software written for embedded systems (especially larger systems with 16-, 32-, and 64-bit architectures) is written in a high-level language, primarily C. While using C language gives an element of portability and reusability by recompilation, much C code in the embedded world has not been written with portability in mind. In fact, code is often tailored and compiler options tweaked to increase performance or optimize memory use, and the result is nonportable. When migrating to a newer environment, perhaps utilizing a different or newer C compiler, the code often breaks.

Using C++ as a programming language can help with reusability. Commonly used and reused sections of code can manifest themselves as objects. These small software IP *black boxes* allow some of the often low-level functions of embedded code to be hidden yet accessible through a high-level interface. When the next system is being designed, these pieces can be ported without breaking the application view, allowing most of the embedded application to be ported through a recompile.

C++ compilers and the language itself tend to be stricter and more clearly defined than C. Today's C++ compilers often have

Operating systems – embedded

built-in portability checking and will flag errors for nonportable code, helping to keep code standard and more portable than much of the existing embedded C code. C++ still has some issues when programming tightly memory constrained systems, but for most large embedded systems, its performance is adequate. Some embedded programmers prefer to use a C++ compiler even though their code is written in C because of its better error and portability checking.

A study once showed the average programmer can write 10 lines of fully debugged code per day, irrespective of programming language, in other words, 10 lines of assembler or 10 lines of C or C++. By using high-level languages and tools for modern processors geared toward high-level compilers, the productivity per machine instruction increases dramatically. This begs an interesting question: Is there anything higher than C or C++ that could further increase productivity? The answer is high-level design languages, such as Unified Modeling Language (UML).

UML is a graphical language allowing the software developer to show the software system at a higher level than in traditional high-level languages such as C and C++. These design languages allow the programmer to specify the system's building blocks, the events and triggers that come in and out of those blocks, and the association they have with other building blocks. This becomes a design specification and can be used to document how the system will behave down to the smallest building blocks, which is useful when programmers have to write certain modules interfacing with modules written by other programmers, as it gives a clearly defined reference. However, today's UML tools take this one step further and generate high-level code from UML, meaning that for each line of UML code written, the UML compiler generates a certain number of C or C++ or other high-level language lines.

Since UML defines system level modules that will generate C or C++ code based on a set of predefined and consistent rules, the ability to migrate this code across different applications, hardware platforms, and operating systems is much easier. Using UML can also make code testing simpler and more automatic. With the interactions described for the modules, developers specify a domain for each parameter and representative test values for each parameter, enabling another tool to generate test vectors from the described interactions and supplied data.

Eclipse provides a framework that allows software tools to plug in using a strict set of APIs and a feature-rich Graphical User Interface (GUI).

A highly portable language and environment such as Java aids reuse and migration for embedded applications. Running a Java Virtual Machine (JVM) on an embedded system enables having portable applications not bound by processor architecture. Though more of an application language than an embedded programming language, Java for large applications could play an interesting part in the overall system. The performance of today's processors and JVMs now make this a firm possibility.

Tools move to Eclipse

In the embedded software world, reuse and code migration are also closely tied to software development tools. As previously mentioned, using a high-level language can increase productivity and code migration. But in the embedded world, that migration has often required changing development tools, hampering developers' productivity. Finding a consistent development environment over different processor architectures, RTOSs, and programming languages has been difficult. Chip companies have highly optimized tools for their architectures, and RTOS companies have tools that include detailed awareness of their operating systems, all with their own proprietary Integrated Development Environment (IDE).

Today, a major change sweeping across the embedded tools world marries open source and commercial tools offering a consistent user interface for embedded developers regardless of chip, RTOS, and programming language: Eclipse.

Eclipse provides a framework that allows software tools to plug in using a strict set of APIs and a feature-rich Graphical User Interface (GUI). The framework offers a consistent interface when developing, editing, and building the software, regardless of compiler, making project migration easy. Additional plug-ins for requirements tools, high-level design tools, and version management also allow embedded engineers to take advantage of high-quality products from the enterprise space, all preconfigured in the Eclipse environment.

Even debuggers now have a consistent look and feel under Eclipse. The CDT project in Eclipse provides a modern but standard GUI for debuggers, and comes preconfigured to work with the GNU Project Debugger engine. Many RTOS vendors have chosen to use the CDT debugger and added functionality specific to their RTOS, allowing users to migrate across different operating systems without having to make dramatic changes to tools they use. Figure 1 shows the Luminosity Debugger from LynuxWorks based on the CDT project.

The Eclipse plug-in environment is so flexible that any tools written in-house can also be given an Eclipse plug-in and GUI, meaning tools that have been previously *standalone* can now be brought into the IDE and integrated with the rest of the build, debug, and test tools that are either provided commercially or from the open source community.

Software IP ties to hardware

When building embedded systems, hardware architecture plays a large part in the portability of the software that runs on it. Choosing a processor and high-level tool set is an important step, but the hardware isn't just the processor; it is a myriad of peripherals that must be driven and controlled by the software. Changes in standards, customer requirements, and even protocols can have a dramatic impact on the selection of peripheral devices and the code portability.

Several aspects should be considered, including:

- Choose a processor architecture that supports a wide range of peripheral devices. For example, PowerPC and ARM processors are widely supported by multiple companies for embedded environments, and the popularity of the x86 platform from the PC world has spawned a range of software drivers and IP.
- Instead of writing and porting software, choose peripheral devices where there are commercial or open source software IP providers that provide code and also integration
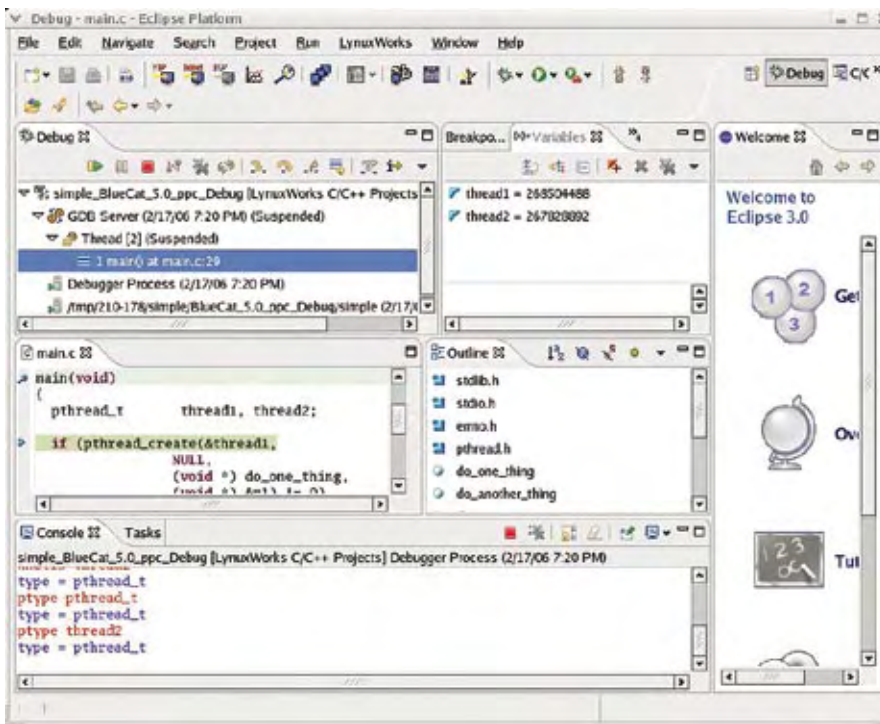
Figure 1

support. This is particularly true of complex communication stacks such as TCP/IP, USB, Bluetooth, Wi-Fi, ZigBee, and similar standards.

- Use reconfigurable hardware. An FPGA's programmable fabric can bring standard hardware IP blocks with software IP to support them into an easily integrated, tested, and prototyped solution upgradeable by reprogramming.

Whatever the choices, integrating the solution presents a significant challenge. Using software IP truly helps speed up development time, as these pieces do not have to be written from scratch. But, this time saved can easily be used up if the software pieces do not work together well.

The answer is to select pieces of software IP that have been preintegrated or at least tested together. The best examples of preintegration are between RTOS and software stacks. Most RTOS vendors also offer a number of software stacks that they maintain and sometimes develop in-house, and a broader selection through partnerships. This gives the assurance that these key pieces of the software architecture and the communication parts work together without major integration work required by the developer, and aids in obtaining support if other integration or testing is necessary.

If support is less of an issue than integration or code writing, then the open source movement could be a good place

to obtain preintegrated IP. Often hardware peripheral companies build the underlying chip-specific drivers, integrated with open source stacks and tested with open source operating systems such as Linux, providing a complete integrated software and hardware solution. However, support for this solution is costly, reliant on hardware vendors, or based on the open source community, all of which present risks for software developers.

Certification goes deeper

For certain applications, other considerations make software reuse compelling, such as when the application must be certified. The avionics, transportation, and medical industries all have certification requirements for embedded systems. This can make software IP use difficult because the code will also need to be certified with the application. In this case, new factors come into play when considering the software IP use.

Software maturity and reliability is a very important factor. If the software IP has already been used in a certified application, its credibility for reuse in others is vastly improved. Some commercial RTOS vendors offer artifacts for the different components of the operating systems that can be used by the certification authorities to show its certifiability, reducing risk and potentially speeding up the certification process.

The Federal Aviation Administration (FAA) is trying to speed up the certification process for avionics systems by allowing software IP to be precertified.

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This precertification produces a *Reusable Software Component* (RSC) and allows these software IP components to be viewed as a software black box when it comes to the certification process. The traditional certification process takes place on the software IP, and thus risks failing certification. With an RSC, the component does not have to go through the same level of certification scrutiny, hence dramatically reducing the risk of failure and cost of certification. To date, only the LynxOS-178 RTOS (Figure 2) from LynuxWorks has been given an RSC by the FAA.

Opening possibilities

Open standards and open source are different things, but both have their place and often apply together in reuse situations. Software standards are generally beneficial for code reusability because adherence to these standards when building code allows portability across architectures, compilers, and when combining software modules together. Conforming to ANSI standard programming rules and using compilers to enforce them makes for better and more portable code.

Using a standard operating system interface is also appealing as it allows for portability across operating systems. Embedded operating systems often have proprietary APIs, and some even resemble other vendors' offerings. This similarity helps developers migrate from one to another, often using their own abstraction layers to insulate the application code from the RTOS API.

POSIX is an open standard API with the idea that code written for one POSIX-based RTOS should be easily portable to another POSIX-based RTOS. However, POSIX is rather large and unwieldy; thus, few operating systems actually fully comply with the POSIX standard. That said, it is still a good practice to use this standard as it is well defined, mature, and well published, and offers a great deal of future proofing for code written to it.

Another API that has emerged in both the enterprise and embedded software worlds, Linux, includes an open source community, an operating system API, a vast collection of open source and commercial applications written for it, and a wide range of Linux operating system ports and distributions. Since its implementation is similar to both UNIX and POSIX, code migration across the three APIs is relatively easy.

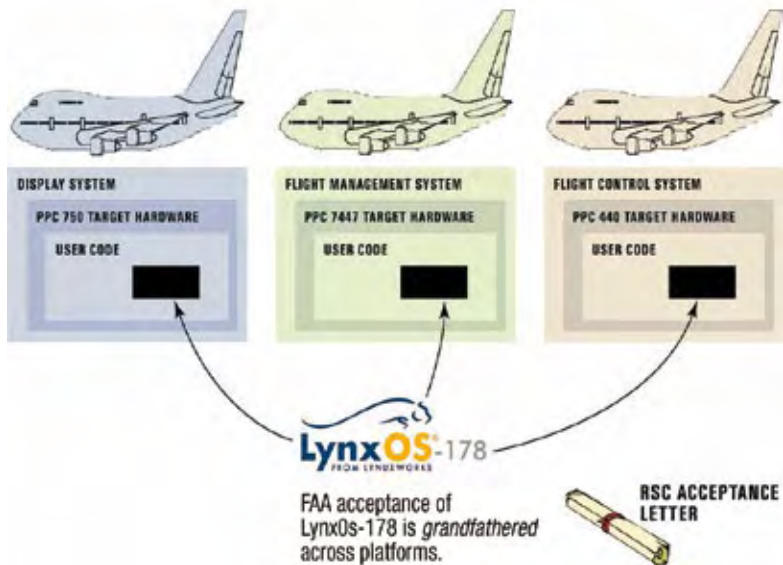Making Linux suitable for embedded and real-time use can be difficult. While the open standards nature of Linux is

Figure 2

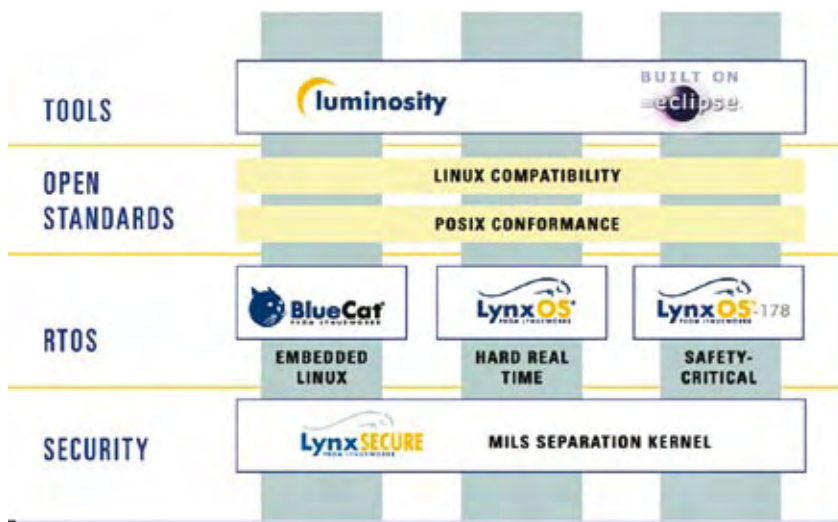**Figure 3**

appealing, what developers can download from www.kernel.org or other open sources is not often suitable for running in embedded systems. For example, the ability to run diskless, as many embedded systems do not have access to a hard disk, involves work for the embedded engineer. The ability to run in a hard real-time or deterministic system is also not well supported from open source.

To actually use Linux in a number of embedded systems requires help from an embedded Linux company. There are a number of embedded Linux providers with varied approaches and offerings of technical support and embedded expertise. Most embedded distributions of Linux will run diskless, but the way of dealing with hard real-time and determinism varies. Some embedded Linux offerings modify or patch the Linux kernel to offer better

performance and determinism; some even replace the Linux kernel with a more proprietary kernel to achieve the same results. Both of these solutions break away from Linux's open source and open standard nature because they may or may not make it back into the open community in a future version of the Linux kernel. However, they do offer the ability to get Linux running on embedded targets without too much pain for the developer.

LynuxWorks offers a Linux distribution and hard real-time and certifiable operating systems based on POSIX (see Figure 3). BlueCat Linux, a fully embeddable diskless operating system based on the standard Linux distribution, provides the same embedded technical support services as for RTOSs. For users who require hard real-time performance, LynuxWorks gives a unique Linux

Application Binary Interface (ABI) that resides above the POSIX API and offers the ability to run Linux applications directly on the LynxOS RTOS. This ABI maintains Linux standards support and helps with code reuse over both soft and hard real-time systems.

These Linux solutions also provide embedded engineers with access to the wealth of applications already written for Linux, hence greatly aiding software IP use. Applications such as networking stacks, Web browsers, databases, and other enterprise applications are more readily available on Linux than any other operating system. This demonstrates how the combination of open source and open standards helps drive software IP availability and aids the reuse of software in embedded systems.

Lifting the burden

As the embedded world moves closer to the enterprise space with applications and software required in embedded devices, the amount of embedded software is growing at an exponential rate. It is clear that without a software reuse and migration strategy, embedded companies will not be able to keep up with the pace and demands of the market, and software will increasingly become the critical path for deliverables.

Fortunately, using standard processors and peripherals, software IP, open standards operating systems, and higher-level programming languages and tools make this job easier and lift the burden for the embedded software developer. **ECD**

Robert Day is the vice president of marketing for LynuxWorks. His responsibilities include leading program management teams and driving worldwide marketing initiatives, including corporate communications and brand strategy.

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Ardence, Inc.

266 2nd Avenue • Waltham, MA 02451
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www.Ardence.com/Embedded/ReadyOn.htm

Ardence ReadyOn

The enhanced end-user experience of instant-on/off functionality and secure, corruption-proof reliability in devices using Windows OS provides OEMs with clear advantages. ReadyOn-enabled devices bypass driver loads, OS boot, network configuration, and application loading time by accessing a preconfigured *environment* – bringing the device to full operability in seconds. Because the preconfigured environment is hardened, viruses cannot permanently install into a ReadyOn-enabled system. Any problem is fixed by simply powering off the device and turning it back on. ReadyOn has been deployed in 2,000,000 systems, with manufacturers such as NEC and Fujitsu, and is ideally suited for consumer electronics, medical devices, automation, portable systems, and testing.
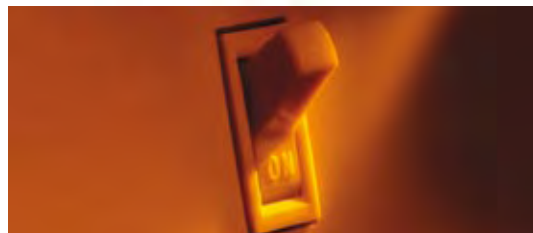
FEATURES:

- Protects key partitions while leaving writeable partitions for saving data, including use with removable storage
- Robust, high-performance Windows instant-on and off: Boot time is virtually eliminated
- Microsoft Windows Support: Windows XP Pro, XP Embedded, Server 2003, including all current service packs
- Integrated appliance environment: OEMs can implement multipurpose functionality on a single system
- *Ghosting* support: Simplifies manufacturing; speeds time to market
- Comprehensive GUI-based configuration and management: Intuitive interface results in reduced time to configure

For more information, contact: info@ardence.com   RSC# 30156 @ www.embedded-computing.com/rsc

## Ardence, Inc.

266 2nd Avenue • Waltham, MA 02451
Tel: 781-693-6278 • Fax: 781-647-3999
www.Ardence.com/Embedded/ETS.htm

Phar Lap ETS

The Phar Lap ETS Real-Time Operating System (RTOS) provides system designers with the most reliable, highest performing, and easy-to-deploy hard real-time development environment. Based on x86 architectures, ETS offers a comprehensive suite of tools that smoothly integrates into the well-known Microsoft Visual Studio IDE – minimizing development and debugging time.

With support for all standard BIOS implementations and the industry's smallest operational footprint, the Win32 API-compliant Phar Lap ETS RTOS enables developers to install, configure, and start developing within two to four hours. ETS has proven itself in thousands of demanding environments, such as multimedia streaming solutions, ocean vessel location systems, submicron scanning systems, and RFID products.

FEATURES:

- Real-time file system: High-speed media access with FAT16 and FAT32 support
- Fully Win32 compliant: No need to use code wrappers for API mapping
- Complete IA32 x86 support: 386, 486, Pentium I, II, III, 4, Multicore, M, Xenon, as well as AMD CPUs
- Smallest operational footprint: < 500 kB with I/O graphics and TCP/IP
- Support for all standard BIOS implementations: Support includes ACPI-compliant PIC and uniprocessor APIC
- Integrated WinSock-compliant real-time TCP/IP stack: Fully Windows independent

For more information, contact: info@ardence.com   RSC# 31390 @ www.embedded-computing.com/rsc

Carlo Gavazzi Computing Solutions

10 Mupac Drive • Brockton, MA 02301
Tel: 800-926-8722 • Fax: 508-588-0498
www.gavazzi-computing.com

5359 FabricPac SM

CompactPCI 2.16 compliant switch fabric platform that contains redundant IPMI system management cards, along with dual AC or DC input 600 W or 400 W PICMG 2.11 power supplies. This platform provides the system integrator with flexibility of designing a system, using both legacy bus-based and next-generation fabric baseboards. At the heart of the system are two PICMG 2.9 IPMI compliant system managers in over/under slot configurations. The IPMI system managers are integrated into the chassis' electronics to provide a fully system-managed environment that includes the cooling unit, system temperature, power supplies, fabric switches, and boards. FabricPac SM contains a PICMG 2.16 switch fabric backplane that delivers a maximum data throughput of more than 40 Gbps.

FEATURES:

- Dimensions: 15.75" H (9U) x 17.00" W x 12.00" D; weight: 35 pounds (13.6 kg) approximately, without cards
- Construction/Finish: .09" lightweight 5052-H32 aluminum alloy; CO white FM code 0S11150 RoHS compliant
- 13-slot right justified with: 10 2.16 fabric node slots and two 2.16 fabric switch slots; all slots support CompactPCI
- Eight slots contain the PCI bus; PICMG 2.0 R3.0; PICMG 2.1 R2.0 hot swap; PICMG 2.9 R1.0 system management
- PICMG 2.10 R1.0 keying; PICMG 2.11 R1.0 power interface; PICMG 2.16 R1.0 cPSB 10/100/1000 BASE-T Ethernet
- Input: AC 90-264 Vac, DC 36-75 Vdc; output: 400 W (600 W) +5 V 50 A (50 A), +3.3 V 40 A (65 A), +12 V 12 A (12 A),-12 V 4 A (3 A)

For more information, contact: jfoley@cg-cs.com

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eCosCentric

Barnwell House, Barnwell Drive • Cambridge, CB5 8UU United Kingdom
Tel: +44-1223-245571 • Fax: +44-1223-248712
www.ecospro.com

eCosPro

eCos is the most widely adopted open source Real-Time Operating System (RTOS), and one of the fastest growing RTOSs overall. Surveys show its market share has now expanded to around 6 percent of the global embedded OS market.

eCosPro delivers the stability, expanded feature set, and support necessary for commercial embedded development with eCos. Rigorously tested and quality assured, it provides a stable and reliable foundation for your products, and incorporates all the tools and runtime features needed for embedded application development. Most importantly, support is included as standard, acting as a safeguard against any issues you may encounter, helping your project to stay on track. It is also highly cost effective due to its lack of royalty and license fees.

FEATURES:

- Real-time performance delivers fast response times with extremely low interrupt latencies
- Advanced configuration technology enables minimal resource footprints
- Available for all major 32-bit embedded architectures: ARM, ColdFire, MIPS, PowerPC, SuperH, XScale, x86
- Tools include: Eclipse IDE, GNU tool chain, and eCos configuration, profiling, and debug utilities
- Runtime features: C/C++ libraries, POSIX/uITRON APIs, TCP/IP, file systems, device drivers, bootloader
- Middleware available: USB, GUI, database, Java VM, CANbus, and others

For more information, contact: info@ecospro.com

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Embedded Planet

4760 Richmond Road, Suite 400 • Cleveland, OH 44128
Tel: 216-245-4180 • Fax: 216-292-0561
www.embeddedplanet.com

Training Courses

Today's embedded systems developers need every advantage they can get in producing world-class software and systems on schedule and within tight budget constraints. Appropriate training is the key to shorter time to productivity and more able personnel. Embedded Planet offers introductory and advanced training courses in Embedded Linux, VxWorks, and Eclipse designed to help our customers become proficient in embedded software development. The Linux and VxWorks courses take students from the basic structures of the operating systems through writing device drivers and creating board support packages. The Eclipse courses teach students how to create Eclipse plug-ins with a focus on embedded software development tools.

Naturally, training instructors have to be the best in their field in order to maximize your training investment. Our training instructors continue to work in the industry on projects for customers involving device driver development, board support package development, and diagnostic development. This ensures that the trainers stay up to date on the latest changes in the industry and bring that real world experience to the classroom.

Embedded Planet believes that the only way to truly learn embedded systems software development is by doing and our courses emphasize this with significant hands-on lab components on Embedded Planet single board computers. In addition, students keep all of the code that they work on during the class so that they don't have to reinvent it when they return to their desks.

Embedded Planet's courses are offered either at our training facility or at a facility specified by the customer giving you flexibility in planning and delivering training when and where it is needed most. We have standard course offerings, but they can be customized ahead of time to meet specific project needs. We encourage students to bring real-world problems to class for exercises.

Contact us to get a list of times and locations for upcoming training or to schedule a training course at your facility.

Ready to Lose the Training Wheels?

FEATURES:

- All courses include significant hands-on laboratory components on production-quality Embedded Planet single board computers

- Training can be delivered at Embedded Planet's training facilities or onsite at customers' facilities for flexibility

- Standard courses are available, but training can be tailored to meet specific project goals for the customer

- Developing for Embedded Linux (EL-201): A four-day course introducing the Linux Operating System and Embedded Linux distributions

- Linux Board Support Package and Device Drivers (EL-805): A four-day course introducing the Embedded Linux BSP and Linux device drivers

- Introduction to VxWorks (VX-401): A four-day course introducing the VxWorks RTOS and the Tornado IDE

- VxWorks Board Support Package and Device Drivers (VX-805): A four-day course introducing the VxWorks BSP and VxWorks device drivers

- Eclipse Plug-in Development (EC-301): A four-day course on the basics of plug-in development for the Eclipse framework

- Advanced Eclipse Plug-in Development (EC-601): A four-day course on advanced topics including productization, branding, and delivery

For more information, contact: info@embeddedplanet.com

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Express Logic, Inc.

11423 West Bernardo Court • San Diego, CA 92127

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www.rtos.com

express**logic**

ThreadX® RTOS

ThreadX is the leading royalty-free Real-Time Operating System (RTOS) for embedded applications running on 32-bit microprocessors and DSPs. ThreadX provides basic thread and interrupt management functions and advanced technology for efficient real-time performance. With more than 300 million deployments, ThreadX is one of the most widely used commercial RTOSs on the market.

ThreadX is intended for use by developers choosing to invest their time on application programming, therefore seeking to use a commercial RTOS, and choosing an RTOS with small memory footprint, low overhead, high performance, low cost, and that is easy to learn and use. ThreadX and its companion NetX TCP/IP networking stack, FileX file system, and USBX USB stack enable developers to focus on the application and to achieve cost-effective solutions for their embedded development needs.

FEATURES:

- Small and scalable – The minimal ROM size of ThreadX is approximately 4 kB
- High performance – ThreadX context switch times are less than 1 microsecond
- Ease of use – ThreadX has the best documentation and the easiest-to-use API
- Certifiable – ThreadX is certified in many applications, including medical, avionics, automotive, and defense
- Advanced debug integration – ThreadX is integrated with almost every major compiler and debugger in the industry
- Value – ThreadX is royalty free
- ThreadX is delivered with complete, highly structured source code

Operating systems — embedded

IBASE Technology (USA), Inc.
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iBASE

Mini-ITX: MB899

The MB899, a Mini-ITX motherboard, supports the latest Intel® Core™ Duo processor and the Mobile Intel® 945GM Express chipset. The latest Intel® Core™ Duo processors give you the competitive edge in the ever-growing embedded market. The Mobile Intel® 945GM Express chipset provides greater flexibility for developers of embedded applications by offering improved graphics and increased I/O bandwidth.

This new embedded motherboard offers intelligent power management capability and greater performance per watt, which enhances the end-user experience for medical, multimedia, industrial automation, and gaming applications.

FEATURES:

- Socket 478 for Intel® Core™ Duo processors
- Mobile Intel® 945GM Express chipset
- Two DDR2 DIMM sockets
- Supports CRT, LVDS, optional TV-Out, or DVI
- 10/100BASE-T LAN, PCI Express Gigabit LAN
- SATA x2, USB x6, digital I/O, watchdog timer
- PCI x1, PCIe (x1) x1, Mini PCI x1, Mini PCIe x1
- Dimensions: 170 mm x 170 mm

Microsoft

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Tel: 800-MICROSOFT • Fax: 425-93-MSFAX
www.microsoft.com/windowsembedded

Windows Embedded

Windows Embedded

Windows Embedded is an innovative suite of operating systems, tools, and technologies that are specifically designed for today's advanced embedded devices. The family of products include: Windows Embedded CE for small footprint devices; Windows XP Embedded, a componentized version of Windows XP; and Windows Embedded for Point of Service (WEPOS), an operating system tailored for retail POS systems.

Choice and control

With a choice of componentized and fully configured platforms and a flexible set of development tools, Windows Embedded puts you in control and helps you more easily build what you want, how you want. Windows Embedded also offers serviceability and manageability to help you maintain control over the quality and performance of your device.

Faster time to market

Windows Embedded offers the complete tool kit you need to quickly configure, build, and ship your device. In addition, because upfront development license costs are low and you can build before you buy, Windows Embedded gives your project a head start, helping you accelerate time to market and create competitive advantage.

Global support networks

Windows Embedded offers the assurance of a 10-year product support life cycle, and an industry-leading, global ecosystem of partner and community resources, helping to foster innovation in the device market.

Windows Embedded will help turn your vision and ingenuity into superior business results by offering a great combination of the creative tools and technology you need and the support and resources only Microsoft and its partners can provide.

FEATURES:

- Windows Embedded CE is a sixth-generation embedded operating system built from the ground up for developing small footprint devices

- Windows CE is a hard Real-Time Operating System (RTOS) and has been proven to satisfy RTOS requirements by independent industry laboratories

- The CE shared source program allows you to modify the OS code for your device while maintaining control over your intellectual property

- With Windows CE you can use Visual Studio, C++, C#, and Win 32 APIs to create flexible development models for devices

- Windows XP Embedded compatibility with XP Pro tools and resources gives you access to the skills and contributions of a global community

- Windows XP Embedded supports enterprise-class manageability of both operating system and application-level updates

- Windows XP Embedded is a proven platform with a development environment that is based on rich, mature, and familiar Microsoft APIs

- With Windows XP Embedded you can build and test applications in the familiar XP Pro development environment

- With Win32 API support, Windows XP Embedded is compatible with thousands of production quality off-the-shelf applications and services

- WEPOS offers plug-and-play support for retail peripherals and industry standards such as Unified Point of Service (UPOS)

- WEPOS is preconfigured to automatically detect and install drivers for POS hardware to decrease installation time

- WEPOS Licensing Model gives OEMs the flexibility to build and ship WEPOS devices for field-installed applications

Micro Digital, Inc.

2900 Bristol Street, G 204 • Costa Mesa, CA 92626
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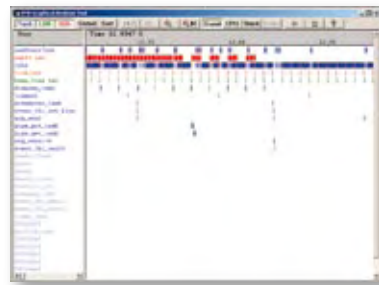
SMX.Blaze RTOS

SMX.Blaze offers networking and multitasking in a low-cost, integrated package. Multitasking allows the networking and application portions to operate independently, thus making design easier. SMX.Blaze saves valuable startup time by providing an out-of-the-box solution that requires no integration for the chosen processor and development tools. Also included in the package are smxAware with its Graphical Analysis Tools. These debugger plug-ins reduce debug time by providing a clear picture of system operation. (See diagram.) smxSim, also included, permits high-level development to proceed without final hardware. File systems, GUIs, USB host and/or device stacks, Web server, e-mail, and numerous device drivers from Micro Digital can be added to extend SMX.Blaze, as needed.

FEATURES:

- Hard real-time multitasking kernel
- Processor-specific BSP and startup code
- Kernel-aware debug and Graphical Analysis Tools
- Compact, fast TCP/IP stack; BOOT, DHCP, FTP, TFTP, and Telnet
- Ethernet and UAART drivers
- Simulator

For more information, contact: bettymd@smxrtos.com
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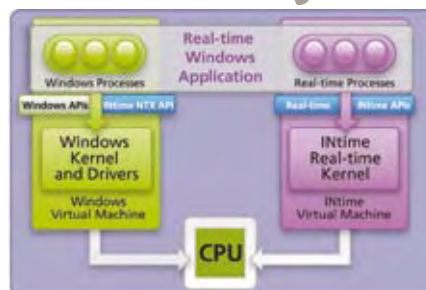
INtime

The best solution for adding hard real-time performance to Windows

The INtime® RTOS for Microsoft® Windows® is the only fully protected solution available for building hard real-time applications that run concurrently with the Windows operating system on a single hardware platform.

Combining robust industrial-grade control with enterprise-rich Windows functionality allows applications to take full advantage of every Windows feature and thousands of off-the-shelf applications, without having to sacrifice real-time responsiveness.

INtime applications are edited, compiled, and debugged with the same Microsoft Visual Studio tools you use to build standard Windows applications. There is no reason to purchase or learn new development tools to build INtime applications.

FEATURES:

- Field-proven real-time technology with more than 25 years of application
- Seamless real-time operation for Windows XP, XP Embedded, 2000, and Windows Server 2003
- Support for multicore processors
- Integrated with Visual Studio – edit, compile, link, and debug real-time software using Visual Studio
- Scalable architecture – real-time applications run locally alongside Windows or on multiple nodes
- DeviceNet, Profibus, CANopen, EtherCAT, and ControlNet fieldbus drivers available

For more information, contact: info@tenasys.com
RSC# 21684 @ www.embedded-computing.com/rsc

AP Labs

10864 Thornmint Road • San Diego, CA 92127
Tel: 858-674-2850 • Fax: 858-674-2869
www.aplabs.com

FS-1280 Rackmount Enclosure

The AP Labs FS-1280 is a 9U ruggedized CompactPCI enclosure designed for 6U CompactPCI boards.

Highly serviceable and maintainable, this chassis provides easy access to front loading boards and utilizes a single 400 W plug-in style power supply. It has a removable peripheral carrier, and can accommodate up to four 5.75" removable drive carriers. The FS-1280 is designed to meet MIL-S-901D in an isolated rack, and MIL-STD-810 and MIL-STD-167 shock and vibration specifications for severe environments. Optionally, it can be upgraded to meet MIL-STD-108E for drip-proof requirements. Versatile and reliable, the AP Labs family of CompactPCI and VME enclosures are especially designed to meet the needs of embedded, development, testing, and military applications.

FEATURES:

- Front-load, rugged, hard-mount chassis single or dual 8-slot – 19" (W) x 15.75" (H) x 18" (D); weight 85 pounds
- Shock: MIL-STD-810, MIL-S-901D
- Vibration: MIL-STD-167, EMI/RFI: MIL-STD-461
- Hinged front door for easy card access; removable peripheral carrier in 8-slot single backplane version
- Available with CompactPCI backplanes
- Front-to-rear airflow

For more information, contact: sales@aplabs.com   RSC# 30156 @ www.embedded-computing.com/rsc

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www.gavazzi-computing.com

5059 Series

The 5059 Series is a 19-inch rack-mountable/benchtop industrial 9U (15.75-inch) high, 12-inch deep chassis that can be configured to meet your needs. There are 21 usable 6U x 160 mm front accessible slots and 21 6U x 80 mm rear transition slots that allow for a variety of configurations. Support for hot swap, N+1 front pluggable AC input power supplies. A front pluggable positive pressure cooling scheme, providing two 12 Vdc 90 CFM fans and tach alarm output. This cooling design provides low MTTR and high reliability. Front-panel controls/indicators include a DC inhibit switch and backplane voltage LEDs, as well as an ESD jack. The rear I/O 400 W or 600 W panel includes an AC/DC power switch, ESD jack, and ground stud, designed with telecom and NEBS compliance in mind.

FEATURES:

- Dimensions: 15.75" H (9U) x 17" W x 12" D; finish: 09" lightweight 5052-H32 aluminum; black medium Fed-ST D595-27038
- Backplane: VME 64X: ABt connector; VITA 41 (opt.); VI/O selectable +5.0 or +3.3 V; coding keys for 3.3 and 5 V
- Input: AC 90-264 Vac, DC 40-72 Vdc, 12 A mA; output: 400 W (600 W): 5 V = 50 A (50 A), +3.3 V = 50 A (65 A), +12 V = 12 A (6 A), -12 V = 4 A (3 A)
- Thermal management; monitored hot-pluggable fan tray with two 90 CFM DC brushless ball bearing fans; front air intake
- Designed to meet NEBS FCC Class A/B UL1950 CSA 22.2 PICMG 2.0 Rev. 3.0 CE
- Peripheral cards supported; 6U x 160 mm 4-12 HP; shielded front panels; front accessible and embedded HDD

For more information, contact: jfoley@cg-cs.com   RSC# 31393 @ www.embedded-computing.com/rsc

Interconnect Systems, Inc. (ISI)

708 Via Alondra • Camarillo, CA 93012
Tel: 805-482-2870 • Fax: 805-482-8470
www.isipkg.com

PC/104 Connectors

Interconnect Systems, Inc. (ISI) offers a complete line of PC/104 and PC/104-*Plus* connectors. Products include: stackthrough, non-stackthrough, and end-of-stack in solder tail, solder bearing, gold, or press fit leads. We also offer a 104 combination molding a 40-pin and 64-pin connector together. Customers can also choose plating options as well as request custom configurations. We also offer a complete line of PC/104 hardware. Ordering is easy by calling our factory direct or using our website to order online. ISI also offers the following connector lines: male headers, female sockets, shunts, drive array, CompactPCI, IP Module EBX, VME, automotive, and custom applications.

FEATURES:

- One- to three-week delivery available – the industry's quickest
- Complete product line
- Solder tail, press fit, and solder bearing options
- RoHS and lead-free compliant
- ISO 9001-2000 certification
- Visa, MasterCard, American Express accepted

For more information, contact: connectors@isipkg.com

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RAF Electronic Hardware

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Male-Female Stacking

Male-female stacking spacers from RAF Electronic Hardware help overcome space limitations that may occur when PC/104 or PC/104-*Plus* bus drives are installed. With this approach, standalone module stacks are used like ultracompact bus boards, but without needing backplanes or bird cages. Module boards are spaced exactly 0.6" apart using RAF precision-made nylon or aluminum male-female spacers, to build structurally secure standalone module stacks.

RAF stacking spacers allow PC/104 and PC/104-*Plus* embedded system designers to employ application-specific module stacks for their products that are easily and securely assembled. The RAF hardware can be used with any of more than 100 different PC/104 ultracompact bus board modules produced by manufacturers today.

FEATURES:

- Nylon or aluminum (mating screw and hex nut available for either material)
- Length: 0.600"; diameter 3/16"; round and hexagon profiles
- 3/16" long, 4-40 male thread on one end
- 1/4" deep, 4-40 internal thread depth
- Precision manufactured for perfect fit
- Availability immediate – in stock

For more information, contact: info@rafhdwe.com

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Techniques to shrink embedded system design cycles

By Rodger H. Hosking

Never-ending demands for increased performance in real-time embedded systems drive system integrators to exploit cutting-edge technology, though new devices may be moving targets and software tools may be far from stable. Facing tough time-to-market pressure, budget constraints on development resources, and no tolerance for trial and error, today's project managers are urgently seeking lower-risk embedded system development strategies.

Savvy board vendors can help customers overcome these obstacles by designing products for ease of use, delivering intuitive and effective software tools, and offering services to help ease critical tasks. Examples of some successful initiatives include modular hardware architectures with strategic ports and hooks, enhanced Board Support Packages (BSPs) for complex peripheral functions, high-level tools for developing and installing custom algorithms on FPGAs, and complete subsystem offerings to handle critical sections of a larger system.

Hardware design strategy: Ease of use

When comparing Commercial Off-the-Shelf (COTS) board-level product candidates, embedded system engineers often create spreadsheets emphasizing features, performance, and price. To achieve higher scores, board vendors struggle to populate their products with an inspired combination of essential resources, all of maximum size or density and operating at the highest possible speed. While this approach boosts ratings for features and performance, price is obviously a disadvantage. To compensate for this, vendors offer depopulated versions of boards or boards with lower-density devices or lower-speed grade devices.

Far too often, the resulting designs consume all available real estate, leaving scant room for less prominent, but vital, facilities. These include timing resources for clocking, gating, triggering, and synchronization functions essential for successfully integrating various system components. Also, connections for monitoring traffic on internal data buses and timing signals can save hours or days of tediously attaching probe wires. These savings are reaped not only during the initial engineering development cycle, but also for recurring troubleshooting in production.

As most manufacturing departments know, COTS boards are notoriously subject to modifications for specific customer program needs. Examples include special requirements for analog input and output impedance matching, AC or DC coupling, and signal bandwidth and gain. Simplifying the addition of these options through judicious board layout of certain components allows larger standard production runs with minor rework for option installation. This improves manufacturing efficiency, reduces finished goods inventory, cuts delivery time, and boosts reliability.

Built-in board health monitoring and diagnostic facilities may seem mundane and near the bottom of the features list, but they often prove to be invaluable. Temperature monitoring circuits connected to junctions within critical silicon devices and to sensors on heat sinks and power supplies can alert the system when a fan fails or airflow is blocked. Voltage monitoring circuits can report out-of-tolerance conditions at the early stage of power supply failure. These resources can be incorporated in a system-level health monitoring application where stored profiles of normal temperatures and voltages are continuously compared to current conditions to help predict problems before they become critical.

BSPs: Abstracting the details

Single Board Computers (SBCs), a standard component in embedded systems, usually run under an operating system and are delivered with a BSP developed by the board vendor. Written for a specific operating system, each BSP must fully comply with the operating system vendor's tools so the customer can start writing the application at a fairly high level, usually in C. BSPs include drivers and libraries that manage memory and other board resources, and handle DMA data transfer operations,

communication links, and interfaces to the system and the backplane.

Filling out the rest of the system are specialty boards targeted to meet specific application requirements such as data acquisition, software-defined radio, digital signal processing, data storage, and high-speed digital interfaces. These boards usually lack a general purpose processor and come with no standardized BSP support. Therefore, the SBC is often responsible for controlling and interacting with these boards across the backplane to make them work.

Originally, specialty board vendors provided some rather primitive tools for customers, such as memory maps for locating each of the various memory resources and status/control registers. Written descriptions of bit definitions in these registers were often the only pieces of information the system engineer received in the way of a BSP. Customers were also handed a copy of the manufacturer's data sheet to support any programmable registers within that device, and not much more. In this case, the system engineer was forced to become intimately familiar with the details of the hardware devices and often had to refer to board schematics.

Now, with unprecedented board device complexity, a few insightful COTS vendors have developed a successful strategy to handle the problem. Low-level bits and control words for the hardware devices are abstracted using a consistent naming strategy for all these programmable variables, which are then arranged in logical groups and defined within C language data structures that can be easily manipulated.

High-level, C-callable library functions referencing these variables and data structures handle the most common operations including initialization, control parameter passing, interrupt generation and handling, data transfers and DMA operations, and built-in test functions. These functions are organized in several hierarchical layers with the upper-level functions calling lower-level functions.

The Pentek ReadyFlow Board Support Library offerings successfully implement this paradigm. Full source code is supplied for all functions at every level so that if high-level functions fall short of achieving a particular mode of operation or if the function is too slow because of unnecessary generality, the system engineer can drill down to whatever level needed to resolve the problem. Figure 1 shows Pentek's Model 7142, four-channel A/D, one-channel D/A with Virtex-4 FPGAs PMC/XMC module, fully supported with ReadyFlow board support libraries and GateFlow FPGA resources.

Figure 1

FPGA tools: Taming the beast

One of the hottest technologies for real-time signal processing is the FPGA. Now virtually all the latest device offerings from major FPGA vendors include ready-to-use building blocks for DSP applications. These include new, sophisticated structures called DSP slices to help implement complex signal processing functions.

Once again, the mounting level of complexity within these devices challenges system engineers to reap their widely publicized benefits. While the high degree of FPGA parallelism can deliver a tenfold improvement in algorithm execution speeds over general-purpose programmable RISC and DSP processors, finding the right combination of talent and tools to make it happen can be quite difficult.

Several solutions have emerged to address these problems. Many DSP programmers create and validate algorithms and even entire signal processing systems on popular workstation tools such as MATLAB. During development, powerful signal generation and analysis tools allow designers to verify correct operation, validate dynamic range performance, and check for exception handling.

After validating a DSP system, HDL code generation tools such as SIMULINK interface directly with FPGA design tools such as the ISE Foundation tools from Xilinx. MATLAB and SIMULINK, both products of The MathWorks, are well integrated through compatible links to Xilinx and Altera FPGA design environments.

Board vendors can help by supplying an FPGA design kit that includes all the board-specific IP structures contained in the standard factory board-level product. This includes interfaces to peripherals and external buses, data movement and formatting blocks, and hooks to external timing signals. With proper organization and documentation, this design kit can be imported into

> Purchasing factory-installed FPGA IP cores and functional subsystems reduces both time to market and development risks ...

the FPGA vendor tool suite as a project, ready for the customer to add application-specific algorithms.

Another solution to FPGA complexity is the vast collection of IP core library offerings now available from hundreds of vendors. Targeted for specialized functions, each represents a highly optimized structure of FPGA resources usually supplied without source code in object form. When installed in a compatible FPGA development tool environment, they appear as objects that can be dropped into the block diagram and connected into other design elements using sophisticated graphical editors. IP core use is a cost-effective strategy to significantly slash FPGA development cycles for these new technology products.

Installed FPGA IP cores: Instant performance

Even with all these high-level design tools, VHDL code generators, and IP FPGA resources, the system engineer is still required to port the new custom FPGA algorithm into a specific COTS board, with its unique set of connections to peripheral devices, buses, memory, and high-speed data converters. Becoming proficient with FPGA design tools requires time and experience, and even for seasoned FPGA developers, this aspect of system integration can represent the highest risk.

By offering to install standard IP cores in COTS hardware products, board vendors can eliminate those risks and guarantee immediate delivery of well-characterized, high-performance functions, fully documented and supported with software libraries and drivers. The system integrator also saves on costs for FPGA development tools and the salary of a highly skilled FPGA designer.

Pentek offers all three of these FPGA productivity boosters in the family of GateFlow FPGA Resources.

Subsystems: Eliminating the risk

By listening to embedded system integrators' requests, board vendors have begun offering functional subsystems consisting of one or more open architecture boards bundled together with software and firmware that implement a complete functional section of a larger system. These subsystem offerings include complete performance specifications that can be incorporated within a system integrator's proposal bid. This dramatically reduces risk for the system integrator in both schedule and cost and creates higher-perceived credibility in the eyes of the end customer.

As part of the offering, it is also imperative for the board vendor to develop a complete subsystem API so the system integrator can easily interface to other system hardware products and software environments.

Resolving system integration issues

Board vendors can truly help embedded systems integrators shrink design cycles in many different ways. Starting at the product definition phase, hardware engineers can include features that simplify timing design, improve testability, and help maintain system health. Well-designed BSPs, IP cores, and FPGA design kits can streamline product development efforts for custom

application code, algorithms, and IP. Purchasing factory-installed FPGA IP cores and functional subsystems reduces both time to market and development risks by shifting these responsibilities to vendor teams that specialize in these areas.

COTS vendors that successfully execute some or all of these clever strategies for solving system integration problems will win customer loyalty and distinguish themselves from the competition. ECD

Rodger H. Hosking is vice president and cofounder of Pentek, which started in 1986. With more than 26 years of experience in the electronics industry, he is responsible for matching new technology to advanced signal processing applications and for the definition of new products. He designed the first commercial direct digital frequency synthesizer, and holds patents in frequency synthesis and FFT spectrum analysis techniques. Rodger has a BS in Physics from Allegheny College and both BS and MS degrees in Electrical Engineering from Columbia University.

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AIMB-762

AIMB-762 is an industrial ATX motherboard built on the Intel 945G Express. It supports dual-core Intel® Pentium® D and Intel® Pentium® 4 processors and delivers system enhancements through high-bandwidth interfaces such as dual-channel DDR2 533/677 memory, PCI Express interfaces, Serial ATA II, and Hi-Speed USB 2.0 connectivity. It also features a graphics engine with outstanding graphics performance, impressive visual quality, and flexible display options. AIMB-762 is definitely the ideal price and performance solution for multimedia, multitasking applications.

AIMB-762 features excellent graphics performance with integrated graphics and an exclusive PCI Express x16 expansion slot. The onboard integrated VGA controller along with the unique Intel Graphics Media Accelerator 950 (Intel GMA 950) are equipped to share memory up to 224 MB and offer a cost-effective graphics solution with superior multimedia and 3D performance. Through the integrated Intel GMA 950 and DVO outputs, the AIMB-762 supports a dual independent display with flexible video output options such as DVI and LVDS. When higher graphics computing abilities are needed, the AIMB-762 provides an advanced PCI Express x16 expansion interface that delivers greater than 3.5 times the bandwidth over the traditional AGP 8X interface to support the latest high-performance graphics cards.

Incorporating the Intel ICH7R chipset, the AIMB-762 comes with rich expandability for future business growth. Several outstanding I/O expansion options are available: one PCIe x16 and one PCIe x4 interface, as well as five 32-bit/33 MHz PCI slots. With up to 8 GBps concurrent, bidirectional bandwidth, the PCIe x16 interface operates as a graphics or general purpose I/O. The 32-bit/33 MHz PCI supports most current expansion devices. To satisfy increasing demands for data transfer speeds, the AIMB-762 provides eight Hi-Speed USB 2.0 connectivity and four onboard Serial ATA II ports with transfer rates up to 3 Gbps for a wide range of peripheral devices.

FEATURES:

- Intel 945G chipset 800 MHz FSB
- Dual-channel DDR2 533/667 SDRAM up to 4 GB
- Chipset integrated VGA sharing 224 MB system memory
- PCI Express x16 slot for VGA card
- Four SATA II ports with 300 MB transfer rate (software RAID 0, 1, 10, 5)
- Supports dual 10/100/1000BASE-T Ethernet via dedicated PCIe x1 bus
- Compatible with Advantech's 2U, 4U, 5U, and 7U chassis
- European Union RoHS compliant

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COM Express

SOM-5780 is an embedded COM Express Type 2 CPU module that fully complies with the PICMG COM Express standard. The new CPU module has an onboard Intel® Pentium® M processor and Intel 915GM/ICH6-M chipset, which supports faster PCI Express and SATA interfaces. The SOM Express modular design concept, on customers' own application-specific baseboard, delivers the highest performance available, safeguards investment with lower Total Cost of Ownership (TCO), and meets current and future demand from customers.

"The SOM-Express series expands upon Advantech's existing solutions by giving customers innovation for their current and future embedded applications. Customers not only want the newest technology like PCI Express, but need their current applications supported equally as well," said Jeff Chen, Advantech Chief Technology Officer. Following the continued broad adoption of PCI Express in the consumer desktop market, the modular, high-bandwidth, low pin count connector is a natural fit for embedded applications requiring higher bandwidth like communications and applications in retail, medical, and military markets.

In a basic form factor of 95 mm x 125 mm, the SOM-5780 provides a scalable, high-performance, and easy-to-integrate solution for customers' applications by utilizing a plug-in CPU module on an application-specific customer solution board. The SOM-5780 with advanced I/O capacity incorporates serial differential signaling technologies such as PCI Express, Serial ATA, USB 2.0, LVDS, and serial DVO interfaces. SOM-5780FL offers design partners more choices for their own applications needing higher computing speeds while maintaining a compact form factor.

FEATURES:

- Embedded Intel Pentium M/Celeron® M processor
- Intel new graphics core based on GMA 900 and external PCI Express x16 graphics interface
- Supports the upcoming primary datapath PCI Express
- Supports eight host USB 2.0 ports and two SATA ports
- Supports up to dual-channel LVDS panels
- European Union RoHS compliant
- Perfect for embedded applications such as communications, retail, medical, and military

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PCM-4386 - EPIC

PCM-4386 is Advantech's first new EPIC form factor embedded CPU board for industrial computing. With a defined 4.53" x 6.50" footprint, which sits between the smaller PC/104 and the larger EBX form factor, PCM-4386 is the first Advantech EPIC Single Board Computer (SBC) that passes the stricter Phoebus Design Extended Temperature Testing (ETT) process, which guarantees reliable operation in extreme temperatures ranging from -40 °C to 85 °C and can resist the most severe shock and vibration.

Advantech SBCs that pass the Phoebus Design ETT are guaranteed for thermal reliability and quality. PCM-4386 uses a fanless 800 MHz ULV Intel® Celeron® M processor and up to 1 GB DDR SDRAM memory that is a perfect match for low-power economical applications. It does not require active cooling; instead, the low-power Intel CPU has passive cooling using a specially designed heat sink on the reverse of the board, allowing PCM-4386 to continuously operate in extreme temperatures ranging from -40 °C to 85 °C and making it an ideal, cost-conscious solution for transportation and automation control in remote and austere locations.

PCM-4386 has PC/104-*Plus* expansion connectors, allowing for scalable ISA and PCI modular expansion – an ideal connection for high shock and vibration. Additional Advantech communication, data acquisition, and peripheral modules can be easily stacked on. It offers a dual channel LVDS panel support up to UXGA (1,600 x 1,200) panel resolution, a popular display solution for POS terminal applications. The EPIC specification defines a unique external I/O coastline zone for easy access and expansion and the flexibility to implement internal I/O connectors as either pin headers or box header connectors. PCM-4386 is also European Union RoHS compliant.

PCM-4386, a PC/104-*Plus* embedded SBC in the EPIC form factor, combines features of severe shock and vibration resistance, with Phoebus Design extreme temperature reliability. It provides multiple I/O options and ultimate scalability, making it ideal for transportation, military, and automation applications in the most severe and harsh environments.

FEATURES:

- EPIC form factor
- Embedded Celeron M processor onboard and support for PC/104-*Plus* bus
- SODIMM socket supports up to 1 GB DDR SDRAM (optional)
- Display combination: CRT + LVDS display support
- Supports four COM and four USB 2.0 ports
- Dual 10/100/1000 Mbps PCI Ethernet interface
- Supports CompactFlash/uDOC (option)
- Temperature ranging from -40 °C to 85 °C
- Phoebus Design Extended Temperature Testing
- European Union RoHS compliant
- Suitable for transportation, military, automation applications, and in the most severe and harsh environments

Arbor Solution Inc.

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ITX-i7435

ARBOR Mini-ITX motherboard has become the most popular platform for gaming machines due to its compact size without compromising on performance.

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FEATURES:

- Support Intel Pentium M Socket 478 up to 2.26 GHz (FSB 400/533 MHz)
- Support PCI Express x16 expansion slot
- Support dual-channel DDRII SDRAM DIMM socket up to 2 GB
- Support dual display (independent display, 18/36-bit LVDS, DVI, and TV-out)
- Support two Serial ATA ports and eight USB 2.0 ports
- Dual Intel PCI Express Giga LAN

For more information, contact: info@arborsolution.com   RSC# 22958 @ www.embedded-computing.com/rsc

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2 in 1 SBCs w/ DAQ

Diamond Systems' rugged 2 in 1 SBCs combine high-accuracy data acquisition with a CPU on a single board to lower cost, reduce space/weight, and improve reliability. CPUs range up to 2.0 GHz with up to 1 GB of memory. USB 2.0, SATA, DDR2 memory, and GbE are available. High-performance graphics on CRT/flat panel displays means you can use the same CPU for the user interface and control. These SBCs are available in PC/104, EPIC, EBX, or custom form factors. DAQ features include up to 32 16-bit analog inputs, 4 12-bit analog outputs, and up to 40 programmable DIO lines with two counter/timers. Diamond Systems' patented auto-autocalibration technology assures high A/D accuracy across the entire operating temperature range. Most provide fanless operation from -40 °C to +85 °C.

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FEATURES:

- 2 in 1 SBCs combine CPU and data acquisition on one board, reducing cost and size and improving reliability
- Available in PC/104, EBX, EPIC, and custom form factors, all with PC/104 or PC/104-*Plus* expansion
- Broad range of processors (128 MHz to 2.0 GHz) and CPU features (video, Ethernet, serial, USB, IDE, and more)
- Data acquisition includes up to 32 16-bit A/D (with auto-autocalibration), 4 12-bit D/A, and up to 40 DIO lines
- Low-power fanless operation, solid-state disk, and optional DC/DC supply yield truly rugged embedded solutions
- Long life, +5 V only SBCs with -40 °C to +85 °C operating temperature range and broad software support

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SBC-GX533 EBX SBC

The SBC-GX533 is a low-profile, fanless, RoHS compliant EBX form factor board based on a 400 MHz AMD Geode™ GX 533 @ 1.1 W processor. It includes all the standard PC interfaces and a full range of multimedia features including onboard graphics that can drive a standard analog display or a flat panel, dual 10/100BASE-TX Ethernet, onboard 32 MB flash drive, CompactFlash CF+ port, four USB ports, four serial ports, and an analog touch screen interface.

An SMI Lynx3DM+ 2D/3D graphics accelerator with an MPEG-2 hardware decoder provides fast graphics into either an analog CRT or a flat screen TFT or DSTN display. The CompactFlash port accepts additional flash memory or wireless cards carrying Wi-Fi, Bluetooth, or cellular modems. The PC/104-*Plus* site offers I/O expansion using Arcom's wide range of PC/104 industrial I/O modules and PC/104-*Plus* video capture modules from Eurotech. Very high-speed serial communication with rates to 921.6 kbps is possible on two of the serial ports.

Rapid application Development Kits for Windows XP Embedded, Embedded Linux, Windows CE 5.0, and an entry-level ROM-DOS option are available. These kits include preconfigured operating system images, device drivers, libraries, cable sets, power supplies, resource CDs, and remote development tools, saving weeks or even months of development effort.

SBC-GX533 offers fanless operation in temperatures to 60 °C. It is an ideal, fully solid-state communications or process controller for remote or unattended locations, with its security features being particularly useful in military IT and other applications.

FEATURES:

- AMD Geode GX 533 @ 1.1 W processor running at 400 MHz
- Full range of multimedia features and hardware accelerator
- Graphics output to analog CRT, or TFT or DSTN flat panel display
- Four-wire analog touch screen controller
- Fanless operation to 60 °C
- Fully solid-state implementation with flash drive
- Four serial ports, four USB ports, and two 10/100 BASE-TX Ethernet ports
- CompactFlash CF+ port for flash memory expansion or Wi-Fi, Bluetooth, or cellular modem cards
- PC/104 and PC/104-*Plus* site for industrial I/O expansion
- Low-profile design for space-limited applications
- Full range of embedded operating systems supported – Windows CE 5.0, Windows XP Embedded, Embedded Linux, and ROM DOS
- Development kits save users weeks or even months of development effort

DIGITAL-LOGIC AG

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MSEP855

With the MICROSPACE EPIC 855 board (MSEP855), DIGITAL-LOGIC offers an embedded computer platform based on the open Embedded Platform for Industrial Computing (EPIC) standard of the PC/104 Consortium. Designed for harsh environments, the MSEP855 provides all interfaces for modern applications. CPU and RAM are protected against shock and vibration. With a typical power consumption as low as 12 W to 25 W, extended temperature solutions (-40 °C to +70 °C) can be realized. Many smart technical details in hardware and BIOS support the integration.

The MSEP855 module is perfectly suited for embedded computing with high CPU and graphics performance in transportation, telecommunication, medical, aerospace, or automotive applications.

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FEATURES:

■ MICROSPACE MSEP855 EPIC with Intel processors Celeron M or Pentium M from 800 MHz up to 1.8 GHz

■ Intel Extreme Graphics with 64 MB VRAM, 1xVGA-CRT, 18-bit LVDS, AC97 stereo

■ Intel 855GME, 400 MHz FSB, Intel ICH4, 256 MB to 1 GB DDR-RAM SODIMM, PC/104-*Plus* ISA/PCI bus

■ CompactFlash socket Type II, FD, 2xP-ATA, COM1, COM2 (all as RS-232), 4x USB V2.0

■ LAN Port A Ethernet 100/10BASE-T, LAN Port B Ethernet 1 Gb BASE-T

■ Thermal concept, operating temperature -20 °C to +50 °C (optional -40 °C to +70 °C), EEPROM support, watchdog

For more information, contact: sales@digitallogic.com   **RSC# 30236 @ www.embedded-computing.com/rsc**

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MSM800SEV

This robust MICROSPACE CPU board in the PC/104-*Plus* format is based on the AMD Geode LX800 processor, a x86-based chip that has been specially designed for embedded applications and mobile industrial and consumer electronic devices. The new processor runs at 500 MHz and is said to provide performance equivalent to an 800 MHz processor. It does not require a cooling fan, since it only consumes about 1.6 W (CPU). The LX800 provides an integrated 2D graphic chip with an analog and a digital output.

The new MSM800SEV CPU board features an ideal price/performance ratio and provides a wide variety of PC interfaces. The PC/104 CPU module is designed for harsh environmental conditions, insensitive to vibration and shock.

DIGITAL-LOGIC
smart embedded computers

FEATURES:

■ MICROSPACE MSM800SEV PC/104-*Plus* CPU board with AMD Geode LX800, 500 MHz, 128-1,024 MB DDR-RAM SODIMM

■ Geode UXGA CRT/LCD 256 MB UMA, 18/24-bit TFT 3 V, LCD resolution 240 x 320 – 1,600 x 1,200, AC97 stereo

■ MS, KB, FD, 1xP-ATA, COM1, COM2 (all as RS-232), IrDA (external), LPT1, 2x USB V2.0

■ LAN Ethernet 100/10BASE-T (external PHY), EEPROM support, watchdog, power supply 5 V

■ Optional PC/104-*Plus* PCI bus connector or CompactFlash socket, cable kit

■ Optimized thermal concept and cooling feature for operating temperature of -25 °C to +70 °C, optional -40 °C

For more information, contact: sales@digitallogic.com   **RSC# 25331 @ www.embedded-computing.com/rsc**

Dynatem, Inc.

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CRM1

The CRM1 is a rugged, conduction-cooled 6U single-slot CompactPCI (PICMG 2.16 compatible) platform based on the Intel® low-power Pentium® M processor. The CRM1 takes advantage of the Pentium M's low power consumption as a rugged Single Board Computer (SBC) with wedge locks and a full-board heat sink for high shock/vibration environments and temperature extremes.

The CRM1 is the same board design as the convection-cooled CPM1. The CPM1 typically uses front-panel I/O routing, but can be provided with identical I/O routing as the CRM1 for application development in a standard CompactPCI bus chassis.

FEATURES:

- CompactPCI and PICMG 2.16 compatible
- Intel Pentium M processor
- Single-slot operation with an onboard CompactFlash disk for bootable mass storage
- 855GME and 6300ESB chipset
- -40 °C to +85 °C operation with 1.4 GHz Pentium M

For more information, contact: sales@dynatem.com

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EMAC, Inc.

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SoM-5282M

The SoM-5282M is a 32-bit System on Module (SoM) based on the ColdFire MCF5282 processor running uClinux 2.6. This 32-bit processor runs uClinux and utilizes an Eclipse IDE, making it extremely easy to create smart network/Internet capable devices, with data acquisition and control properties. EMAC has incorporated all of this functionality on to a small form factor (144-pin SODIMM, 2.66" x 1.5"). The SoM-5282M is ideal for any Web/network data acquisition and control application. EMAC can also provide Carrier Boards that feature A/D, D/A, and GPIO that can be used for development or as part of the product. Unit pricing starts at $150 each. For additional information go to: www.emacinc.com/som/som5282em.htm.

FEATURES:

- Low-power V2 ColdFire core delivering 54 MIPS at 66 MHz
- SD/MMC flash disk with Linux file system
- 10/100BASE-T Ethernet
- Three serial ports and one CAN 2.0 B port
- A/D, PWM, and GPIO
- Free Eclipse IDE with GCC and GDB development tools

For more information, contact: info@emacinc.com

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EP88xS

The EP88xS uses Freescale PowerQUICC I MPC885 and MPC880 processors to create a compact and powerful credit card-sized single board computer module. The small form factor and expansion bus capability make the EP88xS the ideal board for implementing a cost-efficient yet powerful embedded CPU module. You can take the CPU design out of your critical path and concentrate on your application specific hardware.

The processor expansion bus on the EP88xS brings all of the processor signals to standard connectors allowing you simple and full access to the power of the processor. Like all Embedded Planet products, the EP88xS can be custom configured to meet your requirements and is volume production ready.

FEATURES:

- ■ Processor: MPC880 or MPC885 at up to 133 MHz
- ■ Memory: Up to 64 MB of SDRAM and up to 32 MB of flash
- ■ Connectivity: 10/100 Ethernet and RS-232 serial port on the main board or routed to the expansion connector
- ■ Expansion: EBC bus brings out CPU signals for drop-in CPU module
- ■ Debug: Onboard JTAG connection for simplicity in software debug
- ■ Software: Bootloader and diagnostic firmware, Linux, Green Hills INTEGRITY, and VxWorks BSPs available

For more information, contact: info@embeddedplanet.com   RSC# 30719 @ www.embedded-computing.com/rsc

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FEATURES:

- ■ Intel XScale PXA-255 RISC processor
- ■ Atmel 180 MHz AT91RM9200 ARM9-based low-power embedded controller
- ■ AMD ELAN SC520 586 x86 microprocessor
- ■ Freescale 32-bit MCF528x ColdFire with 66 MHz clock speed
- ■ Net ARM NS7520 ARM7TDMI 32-bit with 55 MHz system clock
- ■ DSTni EX X86 120 MHz clock speed

For more information, contact: sales@gridconnect.com   RSC# 30774 @ www.embedded-computing.com/rsc

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KAT4000

KAT4000 is a single-slot Advanced Telecom Computing Architecture (AdvancedTCA) carrier with up to four Advanced Mezzanine Cards (AdvancedMC) expansion modules. This expansion capability enables a wide variety of control and packet processing applications such as WAN access, traffic processing, signaling gateways, media gateways, and many others.

The KAT4000 features onboard Ethernet and PCI Express switches for the AdvancedMC Common Options Region, where the majority of control plane data flows and a flexible modular Fat Pipe Switch (FPS) to address data plane traffic in the AdvancedMC Fat Pipes Region. The FPS is implemented using a plug-over module, enabling simple maintenance and a rapid upgrade path when a newer switch fabric is required. An optional onboard processor gives users additional processing power and can be used to offload system management or OA&M functionality.

In telecom network elements, system management is essential. KAT4000 is an intelligent Field Replaceable Unit (FRU). It fully supports the Intelligent Platform Management Interface (IPMI), allowing it to be monitored by a local shelf management controller or by a remote OA&M system over Ethernet.

For quality in real time, choose the performance, reliability, and responsiveness of Artesyn Communication Products. Our customer support group is available to answer your questions. Please call 1-800-356-9602 or visit our website at www.artesyncp.com for more details.

FEATURES:

- AdvancedMC carrier up to four AdvancedMC modules
- (Optional) Freescale MPC8548 PowerQUICC III running at up to 1.3 GHz
- (Optional) Up to 2 GB of DDR2 553 memory
- (Optional) Up to 1 GB of NAND flash
- Ethernet and PCI Express switches for the AdvancedMC Common Options Region
- Flexible GbE Modular Fat Pipe Switch module
- Up to two GbE to ports 0 and 1 in Common Options Region
- One PCIe to port 1 in Common Options Region
- Four GbE to ports 4-7 in Fat Pipes Region Carrier Grade Linux
- Carrier Grade Linux
- RoHS/WEEE compliant
- Quality assured by more than 30 years of design experience and a TL-9000 and ISO 9001:2000 certified quality management system (FM 26789)

For more information, contact: info@artesyncp.com   RSC# 30597 @ www.embedded-computing.com/rsc

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KatanaQp

The KatanaQp features a two-way Symmetric Multi-processing (SMP) architecture with dual PowerPC MPC7447A or MPC7448 processors and a full complement of I/O for communications applications.

KatanaQp's PCI Telephony Mezzanine Card (PTMC) PICMG 2.15, VITA 32 expansion sites give telecom OEMs, who want to get started with AdvancedTCA today, instant access to a wealth of third-party PTMC modules. This off-the-shelf expansion capability makes it easy to configure the KatanaQp for a wide variety of control and packet processing applications, including WAN access, SS7/SIGTRAN signaling, media gateways, traffic processing, wireless base station controllers, and soft switches.

In telecom network elements, system management is essential. KatanaQp is an intelligent FRU and implements a redundant System Management Bus (SMB). It also fully supports the Intelligent Platform Management Interface (IPMI) with AdvancedTCA extensions to support standards-based shelf management.

Using an off-the-shelf processor blade saves you time to market by allowing you to focus your engineering efforts on the key value-add portions of the system without spending time and effort on the processor design and testing. A processor subsystem blade also lowers your lifetime cost of ownership by providing an easy upgrade path and protecting you from obsolescence issues.

Katana is a Japanese word for sword. The Katana family of processor blades embodies the power and swiftness of this sword.

FEATURES:

- Single or dual PowerPC MPC7447A or MPC7448 processors running at up to 1.3 GHz
- Two-way SMP architecture
- AdvancedTCA PICMG 3.1 node (1000BASE-T base fabric + Octal high-speed GbE fabric)
- Layer 2/3 Ethernet switch option
- Quad PTMC expansion sites
- Redundant SMB with IPMI controller
- Up to 2 GB DDR SDRAM with ECC in SODIMM package
- Up to 64 MB linear flash
- Real-time clock with supercap backup
- VxWorks and CG Linux support
- RoHS/WEEE compliant configuration available in 2006
- Quality assured by more than 30 years of design experience and a TL-9000 and ISO 9001:2000 certified quality management system (FM 26789)

Eurotech

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www.eurotech.it

EUROTECH
G R O U P

CPU-1433 RoHS SBC

Eurotech presents the CPU-1433 module, a new highly versatile PC/104-*Plus* Single Board Computer (SBC) based on the high-performance low-power Geode® GX466 333 MHz processor. This module is fully RoHS compliant and is ideally suited for the latest highly integrated, power-sensitive embedded designs.

Replacing the very popular Geode GX1-based CPU-1432, it has been completely redesigned and now incorporates improved features such as enhanced peripheral connectivity. Compatability is guaranteed with the most commonly used commercial operating systems such as Windows CE® and XPE®, VxWorks®, Linux®, and QNX®.

Integrated peripheral interfaces include: two USB 2.0 ports, TFT and CRT display interfaces, two serial ports, 10/100 Mbps Ethernet, IDE, AC97 audio, AT keyboard, and PS/2 mouse. Onboard features include a real-time clock, watchdog timer, and nonvolatile setup storage.

A wide operating temperature range is achieved with a low-power design that allows structural passive heat dissipation when installed within a system. The CPU-1433 is available in standard (0 °C to +60 °C) and extended (-40 °C to +85 °C) temperature ranges. 128 MB of DDR memory has been soldered onboard to improve system reliability in mobile installations, where severe shock and vibration are common.

As well as standard IDE devices, mass storage can be implemented using a solid-state flash Disk-On-Module (DOM), extending the usability of this module in applications requiring secure data storage and improved storage reliability in harsh environmental conditions.

Ideal applications for the CPU-1433 include: mobile computer systems, real-time industrial control, process automation, digital video and multimedia data acquisition, in-vehicle electronics networking, and wireless communications.

FEATURES:

- Architecture: PC PCI architecture with ISA bus
- Dimensions: Fully compliant with the PC/104-*Plus* standard
- Processor: AMD Geode GX466 333 MHz
- Memory: 128 MB DDR soldered onboard
- Solid-state disk: Connector for a secured Disk-On-Module
- Supported Operating Systems: Windows CE® and XPE®, VxWorks®, Linux®, and QNX®
- BIOS flash: 1 MB 8-bit +5 V flash EPROM
- Interfaces:
  - IDE controller
  - TFT/CRT interface
  - Two USB 2.0 ports
  - Audio
    - AC97 specification v 2.3 compliant
  - 10/100 Mbps Ethernet (Wake-On-LAN availability)
  - Serial ports
    - 1 RS-232
    - 1 RS-232/422/485
  - AT keyboard
  - PS/2 mouse
- Bus: PCI/ISA PC/104-*Plus* compliant
- Power supply: +5 V only

Highland Technology

18 Otis Street • San Francisco, CA 94103
Tel: 415-551-1700 • Fax: 415-551-5129
www.HighlandTechnology.com

T560

The T560 builds on Highland Technology's family of small digital delay generators, intended for use in embedded OEM applications. The T560 standard, packaged versions are usable in many OEM applications and as evaluation units for custom versions. It uses the technology developed for the Highland models V851 VME module, V951 VXI module, and P400 (benchtop) digital delay generators, with basic TTL/CMOS input and output levels and simplified logic.

The T560 accepts an internal or external trigger and generates four precise output pulses, each user programmable in time delay and width. It is ideal for laser sequencing, radar/lidar simulation, or sequential event triggering.

FEATURES:

- Four TTL-level delay outputs, individually programmable for delay and pulse width
- 10 ps delay resolution, 10-second range, 25 ns insertion delay, 20 MHz maximum trigger rate
- Low jitter, highly accurate DSP phaselock system has crystal-clock delay accuracy w/ zero indeterminancy from external trigger
- Time base with external lock capability, optional TCXO; DDS synthesizer for internal trigger rates
- COMM: RS-232 serial interface standard, Ethernet optional; PWR: External universal power supply or 12 Vdc power
- Easily mounted enclosure allows short cable runs and reliable unattended operation; custom OEM package or board-only also available

For more information, contact: info@HighlandTechnology.com   RSC# 21155 @ www.embedded-computing.com/rsc

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ICOP Technology Inc.

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www.icoptech.com

Vega86-6270

This Single Board Computer (SBC) is built with VIA Mark CoreFusion 533 MHz CPU. It has integrated 2D/3D AGP-4X graphics with MPEG accelerator and VIA VT1612A AC97 codec to support multimedia application. The onboard Realtek-8100 10/100BASE-T Ethernet is compatible with the Realtek-8139 device driver available for most legacy and modern OS. The board's general x86 computing hardware spec, such as IDE, FDD, RS-232, RS-485, parallel, USB, and so forth, provides a development environment to take advantage of many existing application development resources available generally on the desktop computer. The board's soldered-on system memory, single 5 Vdc power source, support of -20 °C to +60 °C temperatures, and compact PC/104 footprint make the Vega86-6270 board an ideal choice for embedded applications.

FEATURES:

- Integrated VGA, LCD, AC97 audio, IDE, FDD, RS-232, RS-485, parallel, USB, and Ethernet
- 128 MB soldered on-system memory enables the board to support operation in environments with vibration
- 2D, 3D, AGP-4X with MPEG accelerator to support multimedia application
- -20 °C to +60 °C wide operating temperature range supports operation in harsh environment
- Small footprint and single 5 Vdc power requirement make it easy to adapt this board into existing design
- Board Support Packages (BSPs) available for Windows CE, Windows XP Embedded, and Linux Operating Systems

For more information, contact: samuelp@icoptech.com   RSC# 31255 @ www.embedded-computing.com/rsc

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www.ieiworld.com

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IEI's AMD LX/6W LOW POWER CONSUMPTION 3.5" SBC

Powerful capabilities with small form factor

IEI Technology Corp. introduces the new RoHS compliant, low-power WAFER-LX 3.5" AMD LX processor based SBC with an onboard AMD CS5536 chipset. With total power consumption of only 6 W, powerful performance capabilities, a compact size, and embedded software, the IEI WAFER-LX is specifically designed for fanless, space-limited embedded applications in critical operational environments.

The WAFER-LX is ideal for thin client restaurant applications where ordering, cooking, and billing systems demand hardware performance and reliability.

The new WAFER-LX offers RoHS-converted to several existing IEI SBCs with Geode processors. This allows customers to upgrade existing solutions to the AMD LX processors in RoHS.

The AMD Geode LX processor offers x86 performance with low power consumption and versatility for a variety of SBC applications. The WAFER-LX from IEI Technology is an innovative solution for manufacturers seeking the latest technology for reliable small form factor devices.

Onboard SATA RAID function is another unique design feature of the WAFER-LX that enables faster storage performance with data striping and protects against data loss when a hard drive fails by mirroring all the data across multiple devices.

The 3.5" WAFER-LX is available with an embedded low-power AMD LX 800 MHz processor, operates at temperatures of up to 60 °C (140 °F), and typically consumes only 6 W while supporting numerous peripherals.

Some other WAFER-LX features include the AC'97 Realtek ALC203 audio function, dual Ethernet interfaces, an 18-bit TTL interface, a parallel port, four USB 2.0 interfaces, two SATA interfaces, two RS-232 interfaces, and one RS-422/485 interface. The SSD solution supports CompactFlash cards Type II.

Designed by an innovative team of professionals with superior computer know-how, the IEI WAFER-LX is the world's leading embedded computing control board.

AMD Geode

FEATURES:

- Form factor: 3.5" embedded board
- CPU: AMD® Geode LX-800 processor
- Power consumption: 6 W only
- System chipset: AMD® CS5536
- System memory: 1x 200-pin DDR 333/400 MHz SODIMM SDRAM socket support up to 1 GB
- Ethernet: 10/100BASE-T dual RTL8100C
- I/O interface: 4x USB 2.0
  – 2x SATA
  – 1x LPT
  – 1x FDD
  – 1x CFII
  – 2x RS-232
  – 1x RS-422/485
  – 1x PS/2 keyboard/mouse
- Power supply: +5 V ±5 percent, AT/ATX power support
- Temperature: Operation: 0 ~ 60 °C (32 ~ 140 °F)
- Green product: RoHS compliance
- For more information visit us at www.ieiworld.com or contact an IEI sales rep at sales@usa.ieiworld.com

Innovative Integration

2390-A Ward Avenue • Simi Valley, CA 93065
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www.innovative-dsp.com

SBC6713e

SBC6713e is a high-performance, flexible, standalone DSP board with Ethernet connectivity, loaded with I/O peripherals. Built around the powerful, C-friendly, 300 MHz floating-point C6713 DSP, it is a fully open platform with 15+ off-the-shelf OMNIBUS I/O modules available that provide a wide choice of A/D and D/A and also support simple EMIF bus interface to custom I/O daughter cards. TCP/IP is running on a dedicated DM642 coprocessor to preserve the C6713 for user code and other peripheral controls. System-level integration is facilitated with onboard digital I/O, DDS time base, external clock input, multicard sync, FPDP port data links, 2 MB flash ROM, and watchdog.

FEATURES:

■ 300 MHz TMS320C6713 DSP (floating point)
■ Two OMNIBUS I/O expansion sites
■ 10/100 Ethernet, RS-232 port
■ FPDP data port to 200 MBps
■ Capable of 100 percent standalone operation
■ 600K gate Spartan-IIE for user code (optional)

For more information, contact: sales@innovative-dsp.com   **RSC# 21162 @ www.embedded-computing.com/rsc**

Interphase Corporation

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www.iphase.com/forward/31K.jsp

iNAV® 31K

The iNAV® 31K AdvancedMC Carrier Card is a flexible, high-performance addition to next-generation systems. It meets the needs of a wide variety of applications in AdvancedTCA 3.1 systems, including I/O, processing, and storage. The iNAV 31K allows the creation of a subsystem on a blade by combining PrAdvancedMC, I/O, AdvancedMC, etc. on a carrier. Optional configurations allow the 31K to be customized to meet specific solution requirements. In addition, the 31K supports AdvancedMC.1, AdvancedMC.2, and AdvancedMC.3 specifications. Key applications include: GGSNs, HLRs, soft switches, SGSNs, media gateways, BSCs/RNCs, audio and video service platforms, routers, wireless base stations, and IP Multimedia Subsystems (IMS).

FEATURES:

■ Flexible AdvancedMC carrier with both PCI Express (AdvancedMC.1) and Gigabit Ethernet (AdvancedMC.2) interconnect
■ Supports four mid-size AdvancedMCs or up to two double-width AdvancedMCs
■ Powerful Linux®-based board management computer
■ Supports 10 Gigabit or single, dual, or quad-Gigabit links to the AdvancedTCA fabric, as well as base interface links
■ Dual Gigabit Ethernet links to each AdvancedMC bay
■ Supports APS for optical I/O cards

For more information, contact: fastnet@iphase.com   **RSC# 31404 @ www.embedded-computing.com/rsc**

IP Fabrics

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Tel: 503-444-2400 • Fax: 503-444-2401
www.ipfabrics.com

Double Espresso

IP Fabrics' Double Espresso is the market's first dual Intel® IXP2350 PCI Express card. Each processor has 640 MB of DDR DRAM and an additional 8 MB of external QDRII SRAM. In addition to offering the most advanced NPU development environment – including the ability to incorporate NPU-to-host packet transfer and interaction – the Double Espresso is a fully deployable subsystem, compatible with many existing rack-mount and desktop servers, allowing for advanced integration with the server CPU via the PCI Express interface.

Double Espresso's I/O includes four 10/100/1000 Gbps data plane Ethernet connections with pluggable SFP modules and two 10/100 BASE-T management/console Ethernet connections.

FEATURES:

- Flexibility – configured dual IXP2350s for high-speed packet processing
- PCI Express host interface enables high packet throughput with host computer
- Network processors operate as ingress/egress, pipelined, or independent NPU subsystems
- PPL development software lets you create complex deep-packet processing applications faster
- Innovative PXD add-on provides high-speed packet transfer and remote procedure call over PCI Express
- Time-to-market shortened with available integrated development platform

For more information, contact: info@ipfabrics.com

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KineticSystems

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Tel: 815-838-0005 • Fax: 815-838-4424
www.kscorp.com

VXI Controllers

KineticSystems provides computer interfaces and VXI controllers, including plug-and-play drivers and full VISA library support, for high-performance data acquisition, control, and ATE systems.

Choose from our PowerPC-based VXI slot-0 controllers, or the V153 VXI slot-0 controller featuring a high-performance Pentium® 4 embedded processor as well as the economical V155 Pentium M-based embedded module.

Complete Fiber-Optic Interface Systems (FOXI™) are available to support distances between nodes up to 2 km (6560 ft) with an I/O throughput up to 10 MBps. The FOXI system includes a V122 FOXI PCI Host Adapter that is capable of linking up to 126 V120 VXI slot-0 controllers via a fiber-optic highway.

The VCDS and V15x VME to VXI adapters are also available.

FEATURES:

- V151, V152, V154: Single-width C-size slot-0 controllers with embedded PowerPC processors
- V153/V155: New high-performance Pentium 4/M-based slot-0 controllers with 1.1 to 2.2 GHz clock options
- Includes Ethernet, RS-232, real-time clock, timers and counters, and 2 PMC sites for SCSI, IEEE 488, USB, etc.
- VCDS: Adapts VME devices into VXI form factor and maintains the VMEbus environment, timing, and backplane
- V15x: Converts VME controllers into slot-0 VXI controllers and provides buffered data, access, and trigger lines
- FOXI: PCI host interface and high-performance controllers connected via a 10 MBps fiber-optic highway

For more information, contact: mkt-info@kscorp.com

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Embedded Computing Design Resource Guide 2006

Kontron

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Kontron ETXexpress-CD

ETXexpress is the module concept of the new open standard COM Express (by PICMG). The new Kontron ETXexpress-CD module is based on the Intel® Core Duo processor and Intel Core Solo processor as well as the Intel 945GM chipset. PCI Express is the primary data path for upcoming x86-based systems. Non-PCI Express components such as PCI plug-in cards can still be supported with the PCI 2.1 32-bit interface as ETXexpress COMs will continue supporting the PCI bus for legacy applications. The Kontron ETXexpress-CD will support three PCI Express x1 lanes (opt. five PCI Express x1 lanes), PCI Express Graphic (PEG) x16 lanes.

FEATURES:

- With Intel Core Duo processor and Intel Core Solo processor
- 2x Serial ATA for high-speed drives, 8x USB 2.0 for fast peripherals
- Up to five PCI Express x1 lanes and PCI Express Graphic x16 lanes
- GbE for high connectivity
- 100 percent COM Express compliant
- Basic form factor, pin-out Type 2

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For more information, contact: sales@us.kontron.com

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Kontron ETX-LX

The Kontron ETX-LX (Embedded Technology eXtended) is a highly integrated and fast PC module at extremely low power consumption. It is the RoHS alternative for ETX-mgx and other low-power ETX boards. It allows, due to use of the AMD LX800 processor, the usage of the board without active cooling in applications where space limitations are major requirements. (The maximum height without heat sink is only 10 mm.)

FEATURES:

- ETX 3.0 long-term support
- Energy-efficient AMD Geode LX800 processor
- Drop-in replacement for EOL Geode GX1 solutions
- Up to 512 MB DDR SODIMM
- SATA, USB 2.0, CompactFlash, graphics, and so on
- Ideal for semi-custom solutions

For more information, contact: sales@us.kontron.com

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kontron

Kontron MOPSlcdLX

The Kontron MOPSlcdLX (Minimized Open PC System) is the latest PC/104 platform offered by Kontron. It is based on the AMD LX800™ CPU that boasts an average CPU core power rating of only .9 W. Its TDP rating is only 2.9 W making this the ideal low-power, fanless solution for mission-critical environments. The CPU is also highly integrated with features such as memory and graphics controllers. Coupled with AMD's highly efficient GeodeLink™ bus core, the LX800 at only 500 MHz outperforms many 800 MHz and 1 GHz CPUs in its class. The Kontron MOPSlcdLX is a PC/104-*Plus* (ISA and PCI) based board that enables you to use a wide variety of legacy ISA or high-performance PCI I/O. The Kontron MOPSlcdLX is a highly integrated CPU board and includes onboard PCI graphics, 10/100 Mb Ethernet, and two USB 2.0 ports. A watchdog timer and a real-time clock are standard. The SODIMM socket enables this board to be equipped with up to 1 GB of DDR-RAM. There is also flat-panel support using Kontron's flexible JILI (LVDS) interface for connecting LCDs. The on-chip Graphics+ Controller supports CRT and TFT, and a Kontron chipDISK (IDE compatible flash disk) with capacity up to 512 MB can be plugged directly into the 2.5" hard disk interface. All MOPS PC/104 boards provide the same pin-out for keyboard, COM1 and COM2, 44-pin IDE, 2x USB, LPT, as well as LAN. This feature, common to all the members of the MOPS family, simplifies upgradeability within the Kontron MOPS PC/104 product line.

FEATURES:

- Low power and fanless operation at only .9 W average; at only 500 MHz, outperforms many 800 MHz and 1 GHz CPUs in its class
- High-speed graphics with on-chip VRAM and graphics controller
- PC/104-*Plus* compatible for flexible I/O expansion
- Rich onboard I/O including two USB 2.0, two COM, LAN, IDE, floppy, LPT1, keyboard, and mouse
- LVDS interface for flat-panel support
- High operating temperature range; 0-60 °C
- Up to 1 GB DDR system RAM
- Built in watchdog timer and real-time clock
- Compatible with Kontron solid-state chipDISK drives
- RoHS compliant

RoHS compliant
2002/95/EC

LiPPERT Embedded Computers, Inc.

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www.lippert-at.com

Cool LiteRunner 2

The Cool LiteRunner 2 is an affordable PC/104 single board computer powered by an AMD Geode™ GX 466 @ 0.9 W Pentium-compatible processor running at 333 MHz. It features 256 MB RAM, AC97 sound, and four USB 2.0 host ports, one of which can be configured as device, too. The processor is combined with the CS5536 I/O companion chip, which integrates many of the standard PC peripherals. Together with a Super I/O, these chips form a complete PC with the most common interfaces. The Cool LiteRunner 2 can be expanded using the PC/104 connector or the built-in Mini PCI slot. LiPPERT offers a line of specialized Mini PCI cards, too; check our website for available types. Two independent Fast Ethernet controllers are also onboard, making the Cool LiteRunner the selection of choice for applications such as managed bridges and industrial automation. The Cool LiteRunner 2 comes with an integrated graphics controller that shares its graphics memory with the system memory (UMA). It handles both VGA monitors or digital TFT displays (18-bit parallel or 24-bit LVDS), selectable via jumper or BIOS settings.

In addition to the above-mentioned interfaces, the Cool LiteRunner 2 has even more to offer: Floppy disk adapter, PS/2 keyboard and mouse, parallel printer and three serial ports are integrated onboard, too. Two of the serial ports can be configured by software for the RS-232 or RS-485 standards; the third is RS-485 only. An integrated GoldCap buffers the real-time clock. There are eight freely usable I/O pins for application-defined signals available on a flat cable connector. The ATA-66 compliant EIDE interface connects to hard disks, CD/DVD drives, or similar devices. A CompactFlash adapter facilitates construction of devices without moving parts, as it is often required for mobile applications.

The Cool LiteRunner comes with 256 MB RAM soldered to the circuit board, assuring mechanical stability. Troubleshooting is easy with supervision LEDs for power, watchdog, Ethernet, and application-defined life signalization on the module. The PC/104 bus allows system expansion with many commercially available peripheral I/O boards.

FEATURES:

- AMD Geode GX 466 @ 0.9 W processor, providing x86 performance with support for MMX® and 3DNow!™
- AC97 sound
- 256 MB soldered RAM
- A Mini PCI slot is available and allows integration of WLAN cards
- CompactFlash socket for all permanent storage needs
- 2 x 10/100 BASE-T Ethernet ports facilitate the construction of router and bridge applications
- 4 USB 2.0 host ports
- 3x serial RS-232/422/485, software configurable
- Eight general-purpose I/O signals, available for user-defined functions
- GoldCap for backup
- Flash BIOS with the option to store setup parameters permanently in FEPROM
- Power consumption: ~ 6.5 W, no heat sink required; versions for the extended temperature range of -40 °C to +85 °C available

Single board computers and blades

LiPPERT Embedded Computers, Inc.

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Cool MoteMaster

The Cool MoteMaster has been developed as a gateway node for wireless sensor ("Motes") networks. These sensor networks are used in many applications where wireless connections are needed to allow installation flexibility, or where wired networks are simply not possible to build. Both *fixed* or *ad hoc* networks can be built using the Cool MoteMaster, providing maximum flexibility.

The module features an AMD Alchemy™ Au 1550™ MIPS architecure processor with high processing performance at 500 MHz and, at the same time, very low power consumption. Combined with this powerful device is an IEEE 802.15.4 compliant wireless transceiver module from Freescale, enabling the creation of very low power wireless sensor networks.

The integrated Mini PCI slot can be used to hold a standard laptop WLAN card, allowing it to make connections to wireless access points, too. Should the application require a wired connection, the built-in Ethernet port can handle it. The board is supplied by Power over Ethernet (PoE) or a single +5 V supply.

The small, 90 mm x 96 mm board further integrates two USB host and one device port, three RS-232 serial ports, analog/digital and digital/analog converters, as well as digital I/O.

Comfortable 128 MB RAM and 256 MB FlashPROM make it easy to use Linux as an operating system for the Cool MoteMaster. Troubleshooting is made easy with supervision LEDs for power, watchdog, Ethernet, and application-defined life signalization on the module. The PCI-104 bus allow system expansion with commercially available peripheral I/O boards. The application areas for this module range from its obvious gateway functionality to home control systems and medical applications to industrial controls.

FEATURES:

■ AMD Alchemy Au 1550 processor, a System-on-Chip with embedded security technology

■ IEEE 802.15.4 transceiver

■ 128 MB RAM

■ 10/100 BASE-T Ethernet with Power over Ethernet

■ 2x USB 1.1 host, 1x device port

■ 3x serial RS-232 ports

■ Analog and digital I/O with 12-bit resolution and 128 kSps each

■ A built-in Mini PCI slot allows to add WLAN cards

■ Support CD with Linux drivers available

■ The power consumption is a mere 2.5 W; no heat sink is required

■ Versions for the extended temperature range of -40 °C to +85 °C are available

LiPPERT Embedded Computers, Inc.

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Cool RoadRunner 4

The Cool RoadRunner 4 provides embedded PC applications with the computing power of the Pentium® M 7xx processor. It is a complete single board computer built according to the PCI-104 standard. There are several processor variants with different clock rates available: Pentium M 738 @ 1.4 GHz and Pentium M 745 @ 1.8 GHz, and a Celeron M 373 @ 1.0 GHz. The Cool RoadRunner 4's i82855GME chipset features a fast Intel Extreme Graphics 2 graphics engine with 2D and 3D capabilities, delivering outstanding graphics performance for embedded computer applications. The main memory can be expanded up to 1 GB using suitable DDR-SODIMM modules. As for network connectivity, there is a GbE (1000BASE-T) controller integrated onboard. An AC-97 codec is also onboard for sound I/O. The ATA-100 compliant EIDE interface allows connection of standard hard disks or other storage devices.

The graphics and display controllers use up to 64 MB of memory, shared with the system RAM. An improved Unified Memory Architecture (UMA) guarantees the maximum possible display performance. Display resolutions as high as 2,048 x 1,536 at 75 Hz are supported. In addition to ordinary SVGA monitors, all kinds of TFT flat panels can be connected through the dual-channel LVDS interface. Troubleshooting is made easy with supervision LEDs for power, watchdog, Ethernet, and life signalization on the module. The system can easily be expanded using the PCI-104 bus.

For applications that require the ISA bus, there is a bridge board available, which comes with 2x FireWire IEEE1394, two COM ports, parallel port, floppy disk adapter, DiskOnChip socket, and user programmable FPGA I/O.

FEATURES:

- Intel® Pentium M or Celeron® M processor, up to 1.8 GHz
- A maximum of 1 GB DDR-SODIMM can be handled
- SVGA graphics with 2,048 x 1,536 pixel maximum resolution and dual-channel LVDS
- GbE
- 6 x USB 2.0 host ports
- Sound I/O AC97 compatible
- Programmable watchdog
- Flash BIOS with the option to store parameters in FEPROM; the real-time clock is buffered with a GoldCap
- Supervision LED for power, watchdog, Ethernet, and life signalization
- Power consumption: max. 18 W; passive cooling is possible
- A variant operating in the extended temperature range of -40 °C to +85 °C is available for the 1.0 GHz version

For more information, contact: ussales@lippert-at.com   RSC# 20978 @ www.embedded-computing.com/rsc

LiPPERT
the embedded PC Company

LiPPERT Embedded Computers, Inc.

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Hurricane-LX800

With the Hurricane-LX800, LiPPERT offers a high-performance EPIC board with AMD's Geode™ LX processor with very low power requirements. The board integrates all peripherals needed to build an embedded PC on a small 115 mm x 165 mm (4.5" x 6.5") printed circuit board.

The Hurricane-LX800 integrates a powerful yet efficient AMD Geode LX800 processor together with a CS5536 I/O companion and a Super I/O chip to form a complete PC with all the standard peripherals already onboard. There is a graphics controller with VGA, LVDS, and parallel TFT adapters to connect to many sorts of display terminals. Backlighting is provided for LCD modules.

Two Fast 100/10BASE-T Ethernet ports, RS-232/422/485 serial ports, and four USB 2.0 host ports handle the communication with external devices. There are PS/2 connectors for keyboard and mouse as well as a parallel printer port available. Sound I/O according to AC97 is supported, too. An IDE ATA100 adapter allows connection of hard disk or CD drives. Applications that require nonmoving storage can use the built-in uDOC interface and connect a suitable FlashDrive to it.

Additionally, digital and analog I/O is available for the application. There is a high-speed data input port for 8-bit data capture or video input with 300 Mbps isochronous speed integrated to facilitate fast data acquisition. System expansion is easily done using the PC/104-*Plus* connector and adding suitable specialized I/O modules. The Hurricane-LX800 is powered by a micro ATX supply and supports ACPI, advanced power management, and PCI power management.

Security-critical applications take advantage of the Geode LX processor, too. It has an on-chip AES 128-bit crypto acceleration block capable of 44 Mbps throughput on either encryption or decryption. The AES block runs asynchronously to the processor core and is DMA-based. The Hurricane-LX800 runs Windows, Linux, and VxWorks operating systems.

FEATURES:

- AMD Geode LX800 processor running at 500 MHz
- 1 GB DDR333 RAM maximum
- The graphics controller handles up to 1,920 x 1,440 pixels for VGA, LVDS, and parallel TFT screens
- Two Ethernet ports are available for all types of network applications
- 4 x USB 2.0 host ports; one of these is configurable as device port
- IDE Ultra ATA100
- 2 x RS-232/422/485 serial ports
- Analog and digital I/O as well as raw 16-bit input with 300 Mbps isochronous capture
- AC97 5.1 sound
- Mini PCI slot
- Only 5.25 W power consumption; a heat sink is not required
- A variant for the extended temperature range of -40 °C to +85 °C is available

Men Micro, Inc.

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www.menmicro.com

EM1 ESM

The EM1 is one of several of MEN Micro's MPC5200 PowerPC compute products. Complemented by the 3U CompactPCI F12 Single Board Computer (SBC) and the PCI-104 PP1, the EM1 is a MPC5200-based Embedded System Module (ESM) with 760 MIPS of compute bandwidth, an onboard FPGA for I/O flexibility, low power consumption, and an extended industrial temperature range (40 °C to +85 °C). The MPC5200 includes a telematics communications unit, FPU, MMU, and DRAM controller. Ideal for embedded systems in industrial and transportation applications, these MPC5200-based SBCs can be successfully deployed in the most demanding operating environments.

The EM1 can function as a standalone compute engine or, when mounted on a carrier card, the EM1 can be integrated into bus-based systems, such as CompactPCI, VME, or others. Onboard resources include a variety of memory types, a Fast Ethernet port, a USB connection, a serial port, and other I/O. Optional conformal coating and soldered memory add to the EM1's rugged operating capability.

The EM1's FPGA is Altera's Cyclone. Application-specific functionality can be quickly loaded into the FPGA. For example, the FPGA can be configured with CAN or graphics controllers, or other I/O functionality. Core functions are available from MEN's library or from third parties. Functionality is loaded into the FPGA when the system is booted and is available in less than 200 microseconds. The FPGA can be updated dynamically while the EM01 is operating.

ESMs like the EM1 can be combined with PMC, PC•MIP, M-Module, or other types of mezzanine cards. All ESMs are electrically compatible with the PCI bus and all have the same 71 x 149 mm footprint.

Other MPC5200 PowerPC-based products from MEN include the PP1 PCI-104 module and the F12 CompactPCI SBC. The 3U F12 can functions as a CompactPCI system-slot controller or in a peripheral slot. The F12 features an FPGA that enables the implementation of application-specific I/O.

FEATURES:

■ Based on a 384 MHz MPC5200 PowerPC, the EM1 is an Embedded System Module (ESM)

■ Rugged, low power for embedded industrial and transportation applications

■ 760 MIPS of compute bandwidth from MPC5200 PowerPC

■ Telematics comm unit, FPU, MMU, DRAM controller, and the BestComm/Direct Memory Access controller for industrial interfaces

■ Onboard FPGA enables the implementation of application-specific I/O, such as CAN and other industrial I/O

■ Extensive resources: Fast Ethernet, USB, serial port, SPI, onboard memory flash, and SDRAM

■ Based on the MEN Embedded System Module specification: PCI-104 compatible, small 71 x 149 mm footprint

■ Rugged characteristics: Extended industrial temperature range of -40 °C to +85 °C, conformal coating, soldered memory

■ Low power consumption: MPC5200 consumes less than 850 mW, the entire EM1 operates on only 2.5 W

■ Up to 256 MB onboard DDR SDRAM, 128 MB NAND flash, 2 MB NVRAM, 16 MB of graphics memory

■ Stackable with PC/104 cards, mounted on a carrier card or standalone compute module

■ ESM Starter Kit aids EM1 evaluation, shortens the development cycle, and accelerates time to market

Octagon Systems

6510 W. 91st Avenue • Westminster, CO 80031
Tel: 303-430-1500 • Fax: 303-426-8126
www.octagonsystems.com

New EPIC CPU

Octagon continues to expand its EPIC format series. This new industry standard, administered by the PC/104 Consortium, is the first format to offer a "bridge to the future" – a platform designed to defy obsolescence. Our current products range from 133 MHz to 1.0 GHz, each with a wealth of I/O. Octagon EPIC cards use vertical connectors, minimizing the footprint and eliminating interference with other components in small enclosures. Current Octagon EPIC cards in this series include the low power XE–700, which uses ST Micro Atlas; the 300 MHz GX–1, XE–800; and the high-performance XE–900 using a VIA processor.

FEATURES:

- All Octagon EPIC cards are bootable from CompactFlash
- Conduction cooling kit for the XE–900 permits 1.0 GHz operation without a cooling fan
- Octagon's current EPIC products range from 133 MHz to 1.0 GHz
- Significant I/O expansion capabilities for PC/104 and PC/104-*Plus* systems
- -40 °C to +80 °C operating range
- Small footprint, all connectors are vertical

For more information, contact: sales@octagonsystems.com

RSC# 31410 @ www.embedded-computing.com/rsc

Thales Computers

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www.thalescomputers.com

PowerNode5

PowerNode5 is a rugged 6U VME clone of the IBM JS20 blade design. This new product provides a very high level of performance with full binary compatibility with IBM JS20 blade servers in a form factor fully adapted to any of today's embedded systems requirements.

The PowerNode5 is available in standard convection-cooled and rugged conduction-cooled versions for harsh environment applications. PowerNode5 features two IBM 970FX processors clocked at 1.6 GHz – even the rugged conduction-cooled version – and up to 2 GB DDR SDRAM ECC memory with an outstanding 6.4 GBps memory peak bandwidth.

FEATURES:

- Dual PPC970 @ 1.6 GHz
- 6U one-slot VME
- Compatible with IBM JS20 blade
- Standard commercial grade plus rugged (-40 °C/+85 °C)
- Onboard RapidIO interface
- Gedae Workbench support

For more information, contact: lto@thalescomputers.fr

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www.radi.com

Radicom
Affordable Modem Technology

Embedded Modems

Radicom's Half-InchModem is a reliable modem module featuring ultralow power consumption, high performance, and a footprint that integrates easily into a wide range of existing OEM product configurations.

Measuring just 1.0" x 1.0" x 0.2", the Half-InchModem is loaded with advanced features that allow embedded applications designers to add modem functionality to virtually any product platform without taxing engineering resources. It requires only a serial TTL interface and phone line access to provide data, fax, and voice operation. The modem's fast connection provides a simple but effective approach to data collecting, logging, remote diagnostics, and communications.

The Half-InchModem is EN60601-1 Medical Electronics compliant. The product has been FCC 68, CS-03, c/UL certified and recognized. It meets RoHS compliance directives, bears the CE marking, and conforms to all standards required for immediate shipping to the United States, Canada, Europe, and many other major countries around the globe.

The Half-InchModem is ideal for applications including medical devices, POS terminal, vending machine, remote monitoring systems, data loggers, home security and automation systems, handheld computers, backup communication systems, and any small footprint device that needs to communicate data reliably with low power consumption.

Radicom works closely with its customers to ensure their embedded data communications systems are successfully integrated at the lowest cost with the highest capability. Radicom modifies its award-winning modems to meet specific application requirements, and designs custom components to fit special needs, maintaining the fastest turnaround time in the industry. R&D efforts are focused on raising performance standards for small footprint data communication components embedded in applications across a spectrum of industries.

FEATURES:

- ■ -40 °C to +85 °C operating temperature
- ■ RoHS compliance on select models
- ■ Small footprint - 1.0" x 1.0" x 0.2" in size
- ■ Serial TTL interface
- ■ 2,400 bps to 56K bps data/fax/voice
- ■ Low power consumption; digital line guard protection
- ■ Caller ID, DTMF tones detection
- ■ Enhanced AT command set
- ■ V.42, MNP 2-4 error correction; V.42bis and MNP 5 data compression
- ■ Line-in use, remote hangup, extension pickup, call waiting detection
- ■ FCC68, CS-03, CTR21 certified; c/UL recognized, EN60950-1 compliance
- ■ EN-60601-1 (Medical) compliance FCC15B, EN55022B, EN55024 compliance, CE marking

Trenton Technology Inc.

2350 Centennial Drive • Gainesville, GA 30504
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www.trentontechnology.com

SLT 6515 Processor

Trenton's SLT System Host Board (SHB) features two dual-core processors that together provide four execution cores per SLT. The SLT's two Dual-Core Intel® Xeon® LV processors deliver superior processing capability and system performance using about half as much power as compared to previous generations of low-voltage Intel Xeon processors. The SLT is a server-class PICMG® 1.3 SHB that supports one x4 and two x8 PCI Express links to a PICMG 1.3 backplane. An additional x4 PCIe link to a backplane is available using Trenton's IOB31 expansion module. These links support PCI Express™, PCI, and PCI-X option cards on a PICMG 1.3 server-class backplane. The standard SLT ships with a low-profile passive cooling solution, and an optional active cooling option is available.

FEATURES:

■ Processors: Dual-Core Intel Xeon LV processors at 1.66 GHz to 2.0 GHz; processor package: Micro-FCPGA (478-pin)

■ Chipset: Increased system performance possible by the Intel E7520 chipset's ability to support a 667 MHz system bus

■ PCI Express interfaces: High-speed serial links make PCI Express interfaces typically have data rates twice of PCI interfaces

■ Memory: DDR2-400 interface is dual channel at Memory Controller Hub terminating at 2 DIMM module sockets, totaling four memory sockets

■ Standards: PCI Express Spec 1.0a – SHB Express™ System Host Board PCI Express Spec – (PICMG) 1.3 Spec.

■ Delivers superior performance in telecommunications, industrial automation, and medical system applications

For more information, contact: jrenehan@TrentonTechnology.com   **RSC# 30770 @ www.embedded-computing.com/rsc**

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TML 6490 PROCESSOR

Trenton's TML is a graphics-class, PICMG® 1.3 System Host Board (SHB) that offers dual-core processor performance with a low-profile passive heat sink. The SHB supports x16, x4, and x1 PCI Express™ links, and a 32-bit/33 MHz PCI interface to a PICMG 1.3 backplane. The TML handles a wide range of system option cards, from the latest x16 PCI Express video cards to legacy 32-bit/33 MHz PCI cards. The dual-core processor options feature shared 2 MB L2 cache memories. The Intel® 945G MCH and Intel ICH7R ICH unlock the advanced capabilities of the TML SHB. The ICH7R supports four Serial ATA/300 ports that can operate independent SATA/300 devices or can be configured to support RAID level 0, 1, 5, or 10 drive arrays.

FEATURES:

■ Processor: Intel Core™ Duo processor at 1.66 GHz to 2.0 GHz; Intel Core™ Solo processor at 1.66 GHz to 1.83 GHz

■ Chipset: Intel 945G chipset with advanced video and graphics capabilities with high-bandwidth interfaces

■ PCIe interfaces: TML graphics-class system host board provides one x16 PCIe link on the SHB's edge connectors A and B

■ Memory: DDR2-667 interface dual channel at the Memory Controller Hub, each channel terminating at a DIMM module socket

■ Video: Three connection options; direct via the chipset media accelerator – A x16 PCIe graphics port – ADD2 video and graphics cards

■ Delivers superior performance in imaging, infrastructure, video manipulation, and process automation applications

For more information, contact: jrenehan@TrentonTechnology.com   **RSC# 30771 @ www.embedded-computing.com/rsc**

Tri-M Systems

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TRI-M
SYSTEMS - ENGINEERING

MZ104

The MZ104 is a PC/104 compliant system controller measuring just 3.55" x 3.775". The MZ104 offers the quickest route of integrating a full x86 AT-compatible computer into your embedded control application using the PC/104 form factor. In addition, the built-in peripherals minimize the number of additional modules required. By combining the system hardware, I/O, software (integrated RTOS image), and solid-state mass storage, the MZ104 lowers your exposure to possible development risks and costs and significantly reduces your time to market.

The MZ104's full compatibility with the popular PC/104 embedded expansion bus allows you to easily integrate the widest selection of low-cost hardware peripherals. The numerous features provide an ideal price/performance solution.

FEATURES:

■ Featuring the new edition ZFx86 FailSafe® Embedded PC-on-a-Chip

■ Dual watchdog timers, Phoenix BIOS, and FAILSAFE Boot ROM

■ Dual RS-232 serial, dual EIDE and floppy support, USB, parallel port

■ Low power/low cost 100 percent x86

■ DiskOnChip socket

■ Extended temperature -40 °C to 85 °C

VMETRO

1880 S. Dairy Ashford, Suite 400 • Houston, TX 77077
Tel: 281-584-0728 • Fax: 281-584-9034
www.vmetro.com

Phoenix M6000

The Phoenix M6000 is a Single Board Computer and VXS-enabled I/O controller with dual XMC/PMC sites and dual 4 Gbps Fibre Channel. As an I/O controller and intelligent PMC/XMC carrier, the Phoenix M6000 provides unprecedented power and flexibility. Dual switched PCI Express x8 XMC sites provide users with high-performance connectivity by easily integrating COTS XMC modules into a VXS/VME environment. In addition to XMC, the Phoenix M6000 incorporates traditional PMC sites with independent PCI-X local buses for maximum performance and flexibility. Users can, therefore, integrate any third-party PMC or XMC module on the board. Additional I/O is available via GbE, RS-232, RS-422, and the VME P2 connector.

FEATURES:

- 6U VME/2eSST/VXS Single Board Computer and I/O controller
- Dual XMC sites with x8 PCI Express connections
- AMCC PowerPC 440SP processor
- Dual 4 Gbps Fibre Channel ports
- Independent 64-bit, 133 MHz PCI-X bus for each PMC site
- Ruggedized versions available

For more information, contact: info@vmetro.com

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WDL Systems

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Tel: 800-548-2319 • Fax: 919-545-2559
www.wdlsystems.com

eBox Embedded PC

WDL Systems, The Embedded Products Source, distributes eBox from ICOP Technology. eBox is a complete Embedded PC in a rugged aluminum chassis. The eBox 2600 series has a 200 MHz Vortex86 processor and 128 MB of SDRAM. The eBox 3800 series comes with an 800 MHz VIA Eden-N processor and 256 MB DDR266 system memory. New models 3851, 3852, and 3853 feature rear-accessible CompactFlash socket, wireless networking, and dual Ethernet options. The entire line of eBox Embedded PCs from ICOP Technology is an economical low-power solution for any embedded project or industrial application. Obtain pricing and specifications by visiting www.ebox-pc.com.

FEATURES:

- Fanless operation
- 2x USB ports (one in front)
- 44-pin IDE connector
- Onboard 10/100 Mbps Ethernet
- AC/DC power supply included
- Optional Dual LAN and wireless

For more information, contact: sales@wdlsystems.com

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Embedded Computing Design Resource Guide 2006

WinSystems, Inc.

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WinSystems®

-40 °C to +85 °C SBCs

WinSystems' SBCs embed the x86-based PC architecture into space-limited and rugged industrial applications. They conform to the industry-standard PC/104, EPIC, and EBX form factors. These boards operate from -40 °C to +85 °C. Each is available with software development kits, device drivers, and online documentation. They support Linux, Windows® CE, and Windows® XP Embedded operating systems.

WinSystems targets industrial, security, utility, transportation, medical, communications, COTS, instrumentation, and other low-power, extended temperature applications. We emphasize long-term availability of all of our products.

PC/104 – These small, stackable boards measure 3.6" x 3.8" (90 mm x 96 mm) and support the SC520 and GX500 processors with PC/104 and PC/104-*Plus* expansion. They have four COM ports, 10/100 Ethernet, LPT, CompactFlash SSD, plus support for video and USB.

EPIC – Measuring at 4.5" x 6.5" (115 mm x 165 mm), the EPIC platform supports the more powerful AMD and Via fanless processors operating up to 1 GHz. This larger format provides more I/O space as well as PC/104 expansion. Onboard I/O includes 10/100 Ethernet, four COM ports, USB 2.0, 24 parallel I/O, CRT/flat panel, keyboard, PS/2 mouse, LPT port, and audio.

EBX – The EBX board size is 5.75" x 8.0" (147 mm x 203 mm) and will support up to a 1.6 GHz Intel Pentium® M processor. This form factor allows the greatest number of I/O devices to be on the baseboard while still supporting PC/104 modules for expansion. They support USB, CRT/flat panel/LVDS video, 48-digital I/O lines, AC97 audio, and PC/104 I/O expansion.

The EBC-C3 and EBC-855 are Via- and Intel-based designs for processor-intensive applications. The LBC-GX500 is an AMD-based SBC designed for wired or wireless machine-to-machine connectivity. It can support GSM/GPRS/CDMA/802.11/ZigBee wireless communications, 10/100 Ethernet, USB 2.0, six COM channels, plus an optional world-class, dial-up modem.

PC/104

EPIC

EBX
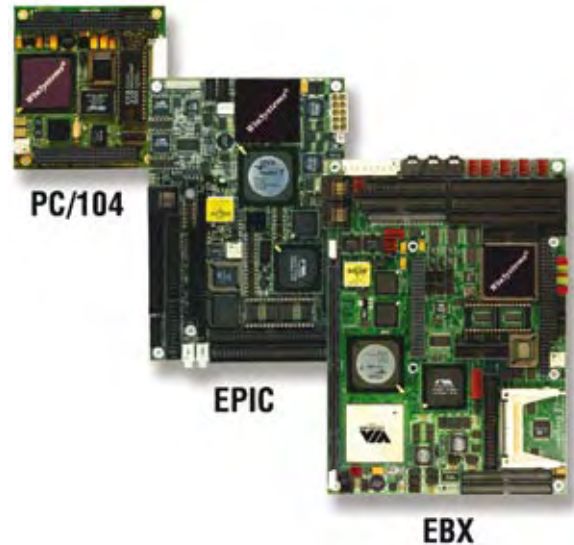
FEATURES:

■ x86 processors with performance up to 1.6 GHz Pentium® M

■ Runs Linux and Windows® CE and XP Embedded operating systems

■ Quick-start software developer kits available

■ Up to 8 GB of CompactFlash SSD supported

■ High-resolution video with CRT and flat-panel support

■ Common PC peripheral controllers include keyboard, mouse, RTC, and LPT

■ Optional onboard 12-bit A/D converter on selected SBCs

■ PC/104 and PC/104-*Plus* connectors for additional I/O expansion

■ Fanless -40 °C to +85 °C extended temperature operation

■ Supports wired and wireless machine-to-machine communications

■ Long-term availability of products

■ 30-day product evaluation program

For more information, contact: info@winsystems.com

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ATP

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Flash Card, Module

Founded in 1991, ATP Electronics has grown to be a leading manufacturer of top-quality memory products, including high-density memory modules and flash digital media solutions. With commitment to excellence, we are involved in each stage of our manufacturing process.

ATP's advanced technology provides durability features to all our flash products – water and extreme temperature resistant. We offer only the best solutions to our customers and their demanding lifestyles in the current digital era. Our current product lineup includes highly durable industrial-grade CF/SD, ultra-high-speed 150X ProMax SD/CF, high-performance 200X USB drives, and the new USB drive/reader combo.

ATP uses the highest-grade DRAM devices from only major DRAM makers and performs rigorous module testing in order to provide the highest quality and optimal performance. To ensure compatibility and functionality, ATP works with major motherboard and system providers, which include Intel, Tyan, Supermicro, and IWILL, to perform thorough testing and qualification. All ATP memory products apply strict Bill of Materials (BOM) control.

ATP has proven to be the leader in providing best-in-class memory solutions to the server/workstation applications. ATP memory products include FB-DIMMs, DDR, DDR2, and Very Low Profile (VLP) modules.

For sales inquiries, please e-mail sales@atpinc.com.

FEATURES:

- ATP VLP REG ECC (0.72" H) for AMD Opteron Blade, CompactPCI platform, single board computers
- ATP VLP DDR2 REG ECC (0.72" H) for Intel Xeon Blade, DDR2 CompactPCI platform, DDR2 single board computers
- ATP VLP DDR2 UNB (0.72" H) for DDR2 CompactPCI, platform DDR2 single board computers
- ATP DDR2 REG ECC SODIMM for special embedded board that required DDR2 SODIMM Registered ECC
- ATP 240-pin fully buffered DIMM, individually tested at 533 MHz/1.80 V for optimal performance; rank: single and dual, up to 4 GB
- ATP industrial-grade CF are dust and static discharge proof as well as shock and pressure resistant, and can sustain extreme temperature
- ATP industrial SD are waterproof; dust, shock, and static discharge proof; and pressure and extreme temperature resistant (-40 °C to 85 °C)
- ATP 200X ToughDrive: Armed with a solid rubber housing and an ultraquick 200X (30 MBps) speed, ToughDrive is the most versatile, robust USB drive

ICS Sensor Processing

296-300 Concord Road, Corporate Center, Suite 120
Billerica, MA 01821
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www.ics-ltd.com

ICS daqPC

ICS daqPC is a PC-based, real-time data acquisition and playback system that can be fully configured to offer a powerful sensor processing solution. Capable of accepting both ICS and third-party boards, the daqPC can be fully integrated for real-time applications that require acquisition, processing, and archiving of large volumes of analog input signal data.

The 600 MBps recording and playback solution requires two 19" rack-mountable chassis with a total height of 7U (12.3"), providing 2.8 TB of data storage capability. Additional storage is available by using an expansion chassis.

The daqPC can be used as an arbitrary waveform generation simulator and stimulator system as well as a cost-effective replacement for dedicated lab equipment.

FEATURES:

- Offers high-speed record/playback capability, storing up to 2.8 TB of digital data on array of hard drives
- Digital recording of sensor signals at more than 600 MBps sustained rate
- Customized solutions to fit the user's requirements – compact and portable solutions available
- Available in rack-mount or portable versions
- Built-in 1 Gb network interface and an NTFS file system for easy postprocessing of recorded data
- Integrated FPGA solutions for software radio applications can be easily integrated into the ICS daqPC

For more information, contact: sales@ics-ltd.com

RSC# 31242 @ www.embedded-computing.com/rsc

Editor's Choice
products

EpicA series graphics cards

Embedded computing applications often need to display more information than what can be shown on a single monitor. The traditional solution to add more graphics cards is often not possible due to limited available expansion slots and costs, but now enabling multiple displays can be accomplished with a single graphics card.

The EpicA series dual- and quad-display graphics cards are designed for thin clients and other mission-critical systems. EpicA products have new, innovative, server-based software from Matrox to manage multidisplay configurations in remote sessions. The cards also feature support for two or four digital and analog monitors at a time, small form factors, low power consumption, passive (fanless) cooling, and PCI bus interfaces.

The EpicA series includes TC4, TC2, and TC2-Lite models. EpicA TC4 supports four monitors at a time and has 128 MB of graphics memory. EpicA TC2 and EpicA TC2-Lite support two monitors at a time and have 64 MB and 32 MB of graphics memory, respectively.

Matrox Graphics Inc.
www.matrox.com/graphics
EpicA series
RSC# 31297

Robust storage security in embedded system applications

The need for advanced storage that incorporates high levels of security is at an all time high, evidenced by the theft of flash cards containing sensitive military data from a U.S. military base in Afghanistan. In addition, new regulations such as Health Insurance Portability and Accountability Act (HIPAA) and Common Criteria raise the bar for security within embedded systems. Typical applications that require advanced data security levels include data recorders, wearable and field computers, medical monitoring and diagnostic equipment, POS systems, and voting machines.

SiliconSystems' new SiliconDrive Secure provides the industry's most comprehensive suite of proprietary technologies enabling multiple user-selectable options for assuring data and software IP security. Offering designers easy implementation, SiliconDrive Secure provides advanced security features such as ultrafast data erasure and sanitization, data zones with independent security parameters, and secure areas for OEMs to add unique encryption/decryption keys as a basis for implementing customer-specific security strategies.

SiliconSystems
www.siliconsystems.com
SiliconDrive Secure
RSC# 31296

www.embedded-computing.com/products

Tri-M Systems

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www.tri-m.com

TRI-M
SYSTEMS - ENGINEERING

CT104

Tri-M's PC/104 Can-Tainer™ is a unique design specifically intended to protect PC/104 electronics such as instrumentation, data collectors, remote terminals, SCADA packages, or other solutions that operate in hostile environments. The Can-Tainer™ is constructed of 0.125" aluminium that can accommodate any number of PC/104 modules, including their cabling and peripherals, with maximum flexibility in a minimum amount of space. Surprisingly, these units are also priced to be used anywhere embedded electronics require a black box.

When deploying electronics in mobile or vehicle applications, vibration and g forces can greatly reduce their life expectancy and reliability. The Can-Tainer™ ensures the PC/104 modules receive maximum protection from vibration and g forces. This is accomplished using Tri-M's dual system of isolating and absorbing rubber mountings. Internally, each of the four corners of the PC/104 stack is held in place by a rubber corner system, which isolates the PC/104 cards from the extruded aluminum enclosure as it absorbs high-frequency vibration. Externally, the anodized aluminum enclosure mates with a thick rubber-mounting pad, allowing the Can-Tainer™ to be attached to a bulkhead while it absorbs low-frequency g forces. The rubber pad is optional and may be removed.

FEATURES:

- The CT104 Can-Tainer is a rugged anodized aluminum PC/104 enclosure designed for harsh environments
- With an isolating shock mount and an internal stack vibration mount, the CT104 provides protection from high frequency vibrations
- Internal rubber corner guides allow for easy insertion of PC/104 modules
- Custom sizes and end caps available
- Standard 2", 4", 5", 6", 8", 10", and 12" sizes
- Dual system of isolating and absorbing shock
- Corner guides, rubber stops, glue, end cap screws
- Protects and enhances the reliability of PC/104 components

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SD-IDE40/44

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FEATURES:

- Directly pluggable to an IDE 40- or 44-pin header
- Hardware bridging between IDE and Transflash/micro SD
- OS installable to Transflash/micro SD
- Bootable from Transflash/micro SD
- Supports PIO 0-4 and Ultra DMA 3 mode
- Supports up to two Transflash/micro SD (Master/Slave)
- Supports Transflash/micro SD up to 1 Gb
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Switch network fabrics

It's all just plumbing, isn't it?

By Victor Menasce

PowerPC continues to dominate most applications in the wireless infrastructure space as the control plane processor of choice. This extends from base transceiver station (Node B) to Radio Network Controller (RNC) cards. The increase in processing needs consequently drives an immediate need for the right interconnects on devices. These interconnects determine how effectively a PowerPC device communicates with other system components such as DSPs. Thus, systems demand high-bandwidth, low-power, and seamless connectivity.

It's all just plumbing. Who cares anyway? The connection wars are over and the Internet won. The volume of data in the Internet dominates the legacy voice networks by a wide margin, so why bother architecting the network to handle voice? It's all about data and multimedia, right?

Well, not exactly.

Today's wireless networks are increasingly required to carry data and video in addition to voice, which adds requirements to the architecture of these systems. All three traffic classes have unique requirements that ultimately merge onto a single unified infrastructure. So the carriage of multimedia, voice, video, and data adds requirements to the network infrastructure.

Wireless network needs

One cannot assume that data channels in a wireless network are only carrying data. Today, push-to-talk services that emulate the old walkie-talkie model use a nailed-up data connection to transmit voice to a predefined receiver with no call setup delay. This voice traffic must meet TDM network grade-of-service expectations. Otherwise, voice quality will suffer and

the perception of an inferior product will prevail. This is one of many advanced services that utilize the data channels in a cellular network.

Cellular traffic has been steadily rising on an annual basis. As the cost of a cellular phone call decreases, the number of subscribers continues to increase with the number of minutes per month. However, cellular networks consume much of their resources managing the mobility aspect, not just the data associated with a voice or data service. Each time a subscriber traverses from one cell to another, the Visitor Location Register (VLR) must be updated. Some high-density cellular networks can consume up to 70 percent of the computing resources performing VLR updates and only 30 percent performing actual call processing. The key metric is subscriber density. As this increases, so does the number of sectors required to service a subscriber base. This is usually accomplished by reducing the power and radius of a cell site and inserting other cell sites in close proximity, which increases overall network calling capacity.

However, most calls still take place over a wired network. By mid 2005 cell phone

usage had increased to an average of 507 minutes per month, an amount that is growing. Wireline customers speak an average of 1,200 minutes per month, a number that appears to be declining. Cellular traffic is billed at an average of 12-15 cents per minute in North America. Wireline is tariffed as a fixed price service, but based on usage, we are paying an average of 2-3 cents per minute.

Two barriers to subscribers' adoption of a pure wireless model include:

- Cost. Cellular is still a premium technology.
- Signal degradation that occurs in many buildings. Cellular customers often have to stand outside a building or next to a window to get acceptable signal quality, a real impediment to disconnecting from wireline services.

As customers roam from the cellular network to the Internet, the potential exists to close the price gap between wireline and wireless services. This will enable wireless customers to roam from a wireless LAN connection to the cellular network and back in a seamless manner, and will entice customers to switch from

Switch network fabrics

their wired residential telephone service to cellular. So the number of voice minutes on the cellular network will grow significantly as people transition from wireline service, translating into tremendous growth requirements for wireless networks.

The wireless network upsurge requires additional capacity, which is usually gained by increasing subscriber density and shrinking the overall cell site radius. Since radio spectrum is a fixed and scarce commodity, the conventional way to increase subscriber density is through the addition of cell sites.

It turns out that traditional bricks and mortar, not technology, drive the economic model for a cell site. The most expensive element of a cell site is the tower and associated infrastructure. The spectrum allocation in cellular follows a uniform model. In reality, subscriber density is far from uniform. For example, cars traveling on a highway through a rural area are starved for bandwidth, whereas a lone farmer in a field has surplus bandwidth available. If it was possible to redirect some of the spectrum from the field to the road, we could increase subscriber density without adding more cell sites.

Based on the concepts in phased array antenna technology, a new technology called *smart antenna* or *adaptive antenna* does precisely that. With a uniform array of antennas, the same signal can be sent to all of the antennas, and modulating the phase of the signal can complete beam forming. This technology has been used in radar installations at U.S. airports for decades. A cellular base station contains an array of antennas just like a phased array antenna. However, the array isn't currently used as a phased array.

Base station architecture

Today's base stations have a hardwired connection between the antenna and the digitizer and from the digitizer to the DSP in the modem pool. Figure 1 shows the conventional architecture. The DSP takes in a wire-speed digitized RF signal and performs radio processing to extract the baseband signal from the TDM data stream coming off the antenna. This fixed provisioning of DSP resources in the system means that base station designers must over-provision DSP resources everywhere in the system to future-proof the system. These extra resources can't be shared easily due to the hardwired data path in the system. By connecting all the DSPs together, the array of DSPs can be treated as a resource pool that can be

shared. This can accommodate a much more scalable DSP resource provisioning, thereby reducing the base station's overall cost.

With the introduction of adaptive antenna, all the DSPs in the modem pool need access to the antenna data from all the antennas. The egress path requires all the antennas to integrate and encode the data for all the sectors. This necessitates a dramatic increase in the base station's computational bandwidth. The interconnect bandwidth between base station elements is also dramatically increased. This attracts much more computational cost in the base station and dramatically increases chip-to-chip interconnect bandwidth require-ments over previous generations.

DSPs typically perform baseband pro-cessing in a base station. This processing provides benefits as it is pooled together as a shared resource using a fabric ar-chitecture and allows the base station designer to cost optimize the DSP pool more effectively.

Interconnect candidates

The new wireless infrastructure economic model is based on increasing subscriber density without having to add extra towers and infrastructure for new cell sites. It turns out carriers are willing to spend more money on base station electronics provided the total cost of ownership is lowered.

Thus, the next generation of cellular base stations will require greater compu-tational power in the modem pool and control plane processors, which typically means in today's architecture a PowerPC processor on each card in the modem pool with an array of DSPs. In the past, DSPs and PowerPC CPUs were interconnected on an ATM-like interface using FPGAs and ATM switches. In the
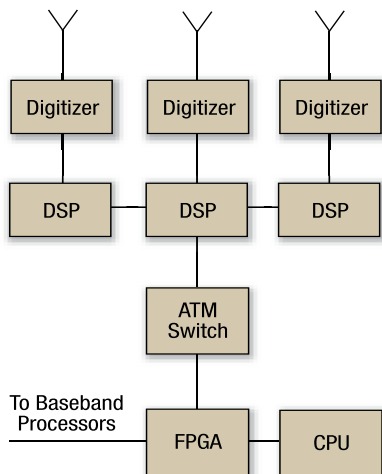
Figure 1

future, the interconnect will be required to carry voice, data, and video, control information, and integrate antenna data from the array of antennas. Separate interconnect technologies for each of these traffic classes would be prohibitively expensive. So a high-bandwidth, fabric-based, peer-to-peer interconnect that can carry multiple traffic classes is required. The possible technologies include:

- Ethernet
- PCI Express
- HyperTransport
- RapidIO
- Advanced Switching Interconnect

The practical solution requires that the chosen technology be widely available on integrated high-performance PowerPC processors, wireless infrastructure DSPs, and switches, thus narrowing the options.

HyperTransport is available in MIPS architecture and ASICs and FPGAs. However, the PowerPC and wireless DSP communities have not embraced it, so it is not a viable choice.

Ethernet could be adapted to the task, but does not have the necessary bandwidth at Gigabit speeds. This would drive the solution toward more costly 10 Gigabit Ethernet solutions. Since Ethernet is a data-gram technology, message delivery is not guaranteed in hardware. The TCP layer in the protocol stack typically resolves this, however, the processing requirements for a full protocol stack at these bandwidths would be cost prohibitive. So a lower-cost hardware-based solution is more suitable. This is true, despite the fact that the network interface between the base station and the RNC will migrate to Gigabit Ethernet. The wireless backhaul must use the most economical wide area network. The bandwidth in the backhaul network is a fraction of the data traffic within the base station.

PCI Express is widely available on integrated PowerPC processors, though not necessarily on DSPs. It has the hardware-based guaranteed message de-livery Ethernet lacks, but is based on a tree model that assumes a single host or root complex in the system. So it lacks true peer-to-peer capability, a necessity for this application.

Advanced Switching Interconnect theo-retically addresses PCI Express peer-to-peer limitations, but has not been widely adopted by semiconductor vendors. Even Intel, which initiated the technology, has backed away from implementing it in silicon.

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RapidIO, however, is the technology of choice for this application. It has the performance scalability the application requires and the hardware-based guaranteed message delivery carriers expect. Switches are available from at least three different vendors (and growing). DSPs are available from two leading companies in wireless infrastructure DSPs. PowerPC processors with RapidIO from AMCC and other PowerPC vendors are also available and on future roadmaps. This choice enables a high-performance homogeneous interconnect technology for the hub of the entire base station.

Figure 2 shows the more flexible and scalable base station architecture that results from introducing RapidIO fabrics in the system. RapidIO has the bandwidth to support the application and the ability to prioritize traffic based on data classification. So one can assign different priorities and queues to each traffic class and segregate traffic using different transmission methods. Data plane data traffic can be transmitted using the RapidIO messaging protocol, while control plane is sent using direct memory mapped I/O. The priorities of these traffic classes can be controlled so that user data never causes head-of-line blocking for control plane traffic. This traffic segregation on a unified interconnect enables carrier-grade reliability related to separate control and data planes with the simplicity and cost of a unified model.

RapidIO has advanced data plane features that enable quality of service traffic management, which is inherent to the architecture and does not require heavyweight traffic managers to correct excessive jitter and wander introduced by some of the other interconnect technologies.

> **[RapidIO] has the performance scalability the application requires and the hardware-based guaranteed message delivery carriers expect.**
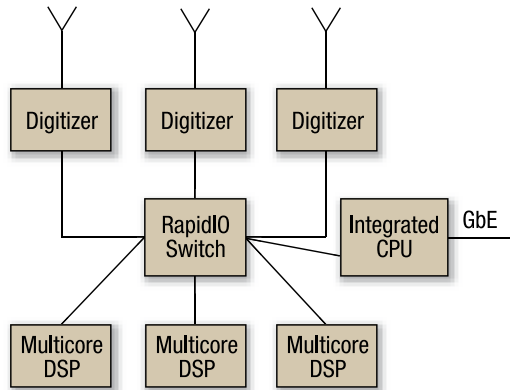
Figure 2

Future 3G standard releases include:

- High-Speed Downlink Packet Access (HSDPA): Provides a high-bandwidth asymmetric downlink data channel
- Asymmetric Digital Subscriber Line (ADSL): Assumes there is more downstream bandwidth requirement than upstream
- High-Speed Uplink Packet Access (HSUPA): Adds a symmetric high-bandwidth data channel

All of this drives the requirement for increased bandwidth in the base station and radio network controller. The key to enabling the next generation of services in wireless networks is the right mix of processing power, signal processing, and interconnect technologies. **ECD**

Victor Menasce is currently CTO at AMCC where he has overall responsibility for the processor and network processor product line strategies. He is an active member of the RapidIO Trade Association, and previously served as vice president of engineering and CTO at AMCC with responsibility for the PowerPC product line. Prior to joining AMCC, Victor worked at Tundra Semiconductor and Nortel Networks in a variety of marketing and engineering leadership roles. He is based in Ottawa, Canada.

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Universal 3Gbit IO

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Initial release of the Universal 3Gbit Card will come with an easy-to-use Rocket I/O protocol supporting up to 12 Gb full duplex per connector. Third quarter 2006 will see releases of up to 10 G full-duplex InfiniBand per connector, up to 10 G full-duplex Ethernet per connector, and Serial FPDP. Although the InfiniBand, Ethernet, and Serial FPDP protocols will be provided as black-box solutions with few modifications by users allowed, more adventurous users who choose to develop their own communications protocols from the basics already have access to all the board resources through a VHDL source for the interfaces to SRAM, signal conditioners, LAD bus, I/O bus, and PPC flash. CoreFire users will have the usual CoreFire board support package.

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The RapidIO interconnect architecture is an ISO-certified open standard that seamlessly enables the chip-to-chip, board-to-board, control, backplane, and dataplane interconnections needed in high-performance systems. This established, scalable, packet-switched fabric addresses the needs of equipment designers in the wireless infrastructure, edge networking, storage, military, and industrial markets. Developers will find that the RapidIO ecosystem offers a critical mass of products on the market today – including a wide assortment of endpoints, which can minimize the amount of bridging required in a design. Detailed information about the RapidIO ecosystem products, design tools, and member companies is featured in the Company Showcase at www.RapidIO.org.

FEATURES:

■ The RapidIO standard is defined in three layers – Logical, Transport, and Physical:

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– Transport – Provides the necessary route information for a packet to move from endpoint to endpoint

– Physical – Describes device level interface specifics: packet transport mechanisms, flow control, and so on

■ RapidIO Trade Association Steering Committee members: AMCC, EMC2, Ericsson, Freescale Semiconductor, Lucent Technologies, Mercury Computer Systems, PMC-Sierra, Texas Instruments, Tundra, and Wind River

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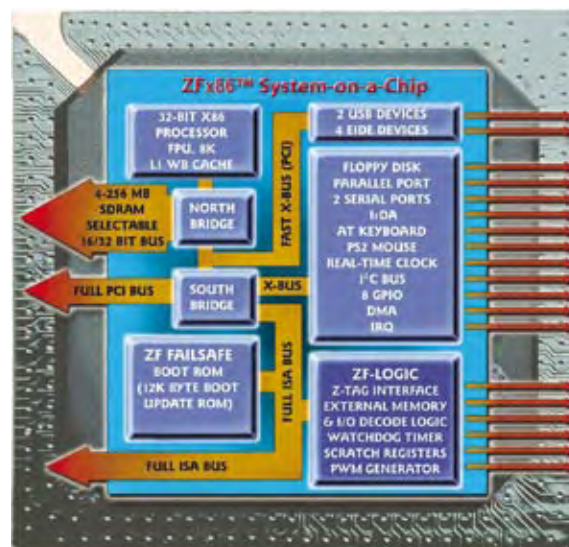
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Using assertions to track functional coverage

By Kelly D. Larson

The EDA industry reports that functional verification is becoming an increasingly large portion of the design effort for today's complex chip designs, often consuming as much as 70 percent of the overall development time. Verification teams must continually seek ways to become more efficient. One of the methodologies being used to address this growing need is verification through assertions, which provide a way to describe the expected behavior of a block or to validate design assumptions regarding its behavior.

Assertions are not new; they've been around for about as long as computer languages. What is new, however, is the recent widespread acceptance of standard assertion languages such as Property Specification Language (PSL), SystemVerilog Assertions (SVA), and Open Verification Library (OVL) by multiple tools vendors.

The adoption of these standard assertion languages by multiple vendors and tools allows assertions to be used in a variety of ways. PSL was originally developed at IBM in the early '90s as a way to describe design properties for static formal analysis. While still very much in use for formal model checking, major tools vendors have more recently adopted PSL and other assertion languages as a way to specify properties during the dynamic simulation of a Hardware Description Language (HDL)-based design. It's now possible for a verification engineer to reuse the same set of assertions during a formal analysis of a block, and then again in a dynamic simulation. There is yet another use for assertions, the use of assertions for functional coverage.

Functional coverage

One of the most important metrics to track prior to taping out a new chip design is the goal of 100 percent functional coverage. Each design block that is verified should have a formalized verification test plan that, hopefully, identifies every feature that must be tested in order to demonstrate full functionality. This presents the verification engineer with two big challenges:

1. How do you know all the functionality that needs to be tested has been identified?
2. Once the functionality has been identified, how do you prove that everything that has been identified has been properly tested?

One popular approach to determining block verification quality is using a code coverage tool. Those with experience using code coverage know that this can be a great negative indicator. By identifying lines of code in the design that have never been executed during simulation, this tool will single out areas of a design that have not been fully tested.

Code coverage by its very nature is an automated, mechanical process, which can be both a strength and a weakness. The strength to this approach is that it does not depend on human interpretation of the spec or understanding the design. Thus, the tool will often highlight areas of the design that have been overlooked or inadvertently left out of a verification test plan. The simple fact that a line of code has been executed, however, doesn't guarantee that a design functioned correctly. Code coverage tools have no way of evaluating what the correct behavior of a design should be. In effect, code coverage indicates the design has *been there*, but not necessarily if it has *done that*. Because of this, code coverage can often be more helpful with the first challenge rather than the second.

As for conquering the second challenge, using assertions for functional coverage can be a very powerful technique. Assertion languages are most often associated with property checking, which tends to be their primary use. Conceptually, however, the use of assertions for functional coverage accomplishes a completely different task than for property checking. Property checking tests the behavior of the design and whether or not the design behaves correctly under specific conditions. Coverage checks have little to do with the correct behavior of the design, and are instead used to determine the correct behavior of the tests themselves. Defining correct behavior is only part of the verification job. The

test environment itself must be capable of stimulating the design through the full range of expected, and in some cases unexpected, behavior.

A single assertion can complete both property checking and coverage. If assertions are used for property checking during block design and verification, these same assertions can form a good base for functional coverage. Many times assertions are written as implications so that one set of conditions, X, implies that another set of conditions, Y, holds true, or $X{\to}Y$. In the context of coverage, it's the X part, or the triggering condition, that is important. Tracking when and how often these triggers are hit creates a clearer picture of what is going on during a simulation.

A full behavioral description of a block with property checks, however, does not automatically imply all the necessary functional coverage as well. In most cases, more work will be required since the goals of these two activities differ. Again, property checking verifies the proper behavior of the design, whereas functional coverage checks determine if sufficient stimulus has been applied to the design. In short, property checks make sure bad things do not happen, and coverage checks make sure good things do happen. For example, Figure 1 shows a simple arbitration block with three request lines as inputs and three grant lines as outputs.

Figure 2 shows several basic PSL assertions for describing the desired behavior of this arbitration block. These assertions make use of the implication operator and assume a default clock. Even those who are unfamiliar with PSL can see what's going on. The first assertion requires that if the request signal, req1, is high on any clock, then the grant signal, gnt1, should be high on the next default clock, and all others should be low. The next assertion states that when req2 goes high, then only its grant should be high on the next clock, unless, of course, the higher priority req1 is also making a request. Similarly, req3 will get its grant, as long as there aren't any requests from req1 or req2. The final assertion prevents a spurious grant signal when none of the request lines are high.
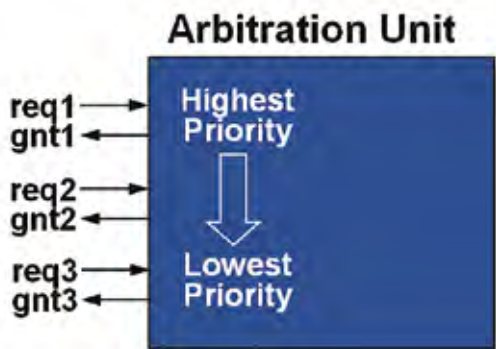
From a functional verification standpoint, this small set of property checks does a fairly complete job of describing the desired arbitration behavior. This same set of assertions is not sufficient, however, from a functional coverage standpoint. If none of the three requests arrive in the same clock cycle during testing, the assertions may all still pass without the block actually having to arbitrate. Simply measuring that the trigger conditions have all been hit might give a false sense of security since hitting all the trigger conditions in this case never guarantees there were ever any simultaneous requests.

It would not be difficult to use a waveform viewer to verify that simultaneous requests were happening, but this does not ensure that changes to the design and the environment would not prevent this from happening in the future. For this example, the property checking does not fill in all the gaps needed for functional coverage.

Figure 3 shows one approach to filling in the gaps using assertions, or in this case, PSL cover statements, to show that the test environment has indeed caused simultaneous requests, and that the arbitration logic is actually getting exercised. PSL and SVA both support a *cover* statement that allows the definition of a trigger condition without the need to check for a property, much like having a nonfailing assertion whose trigger condition can be tracked with all the other property checks.

```
cover {Req1 && Req2 && !Req3};
cover {!Req1 && Req2 && Req3};
cover {Req1 && !Req2 && Req3};
cover {Req1 && Req2 && Req3};
```

Figure 3

With this simple example, it would have been effortless to enumerate explicitly all the possible input combinations for the three request lines using cover statements or even within the original arbitration property checks. While that might be easy for only three levels of arbitration, what if there were 8, 12, or 16? For coverage checking, it is often necessary to determine what the most important corner cases are and make intelligent decisions on what to instrument. A haphazard approach in a large design could easily lead to scores of relatively useless coverage points, which could eventually have negative effects on simulation performance as well.

Assertions in your environment

Most mainstream HDL simulation tools today provide quite a few ways to view assertion activity from a high level. At the end of the simulation, these tools allow the generation of tables that report on the runtime activity of every assertion, including how often they were triggered. Most tools will also enable the

Figure 1

```
assert always {req1} |=> {gnt1 && !gnt2 && !gnt3};
assert always {req2 && !req1} |=> {gnt2 && !gnt1 && !gnt3};
assert always {req3 && !req1 && !req2} |=> {gnt3 && !gnt1 && !gnt2};
assert always {!req1 && !req2 && !req3} |=> {!gnt1 && !gnt2 && !gnt3};
```

Figure 2

> The test environment itself must be capable of stimulating the design through the full range of expected, and in some cases unexpected, behavior.

Figure 4

concatenation of results from multiple simulation runs. This provides the feedback to help verification teams analyze how complete their regression suite is or how well their randomization is performing (see Figure 4). Some tools will also allow the ranking of tests based on how much additional coverage they provide.

All the recent enhancements to simulation tools have made viewing global functional coverage data easier, but what if a need to focus on the behavior of a single test arises? High-level test bench languages are helping provide amazing capability in the area of random testing, but there remains a need for directed tests, usually to target a specific feature or set up a specific event. It would seem reasonable to make use of the same functional coverage points provided by the assertions to determine whether or not the test case is doing what it was intended to do, and more importantly, to fail the test if it is not.

Tools support in this context is not very good, at least not yet. Current tools don't have built-in capabilities that allow the user to target specific coverage points during a simulation. For now, the user must develop these capabilities. This requires the simulation environment to support an additional way to fail a simulation beyond any of the behavioral checks already built into the environment. In this case, the assertions determine whether or not the intended coverage points have been hit. Did the test do what it was supposed to do? This is a different failure mechanism than a property failing, which would indicate a problem in the design.

The Analog Devices design center in Austin, Texas, has extended the simulation environment by adding the capability to specify at runtime which coverage points are required to be hit during the course of the simulation for each individual directed test. This ensures that desired conditions such as buffer overflows, resource contention, cache behavior, interrupts, or anything else describable by an assertion are reached during the test. The robustness of a regression test suite is greatly enhanced if all tests fail not only for illegal behavior, but also if desired behavior is not achieved. The ability to specify coverage points that should not be hit during a test is also useful on occasion. These are not normally illegal conditions, but simply conditions that should not be encountered for a specific test case. Examples of where this might be useful include verifying that a bus can sustain a particular bandwidth without stalling or that a test designed to exactly fill up an instruction cache can do so without a single cache miss.

Stimulus versus system effects
Advocates of high-level test bench languages such as SystemVerilog and Specman are quick to point out built-in features of these languages during discussions of functional coverage. Test bench constructs such as cover groups can be an efficient way of analyzing whether or not the test bench is generating the full range of transactions and other expected random stimulus.

It should not be assumed, however, that full coverage of the types of stimulus the test bench can provide also equates to full functional coverage within the design itself. Many aspects of the design still require additional coverage points beyond stimulus, including arbitration, buffer overflow/underflow, cache behavior, and many other conditions indirectly related to the external stimulus.

Enhanced visibility
Using assertions for functional coverage adds a level of visibility

to a test environment that brings about additional benefits. These assertions can be considered a way to verify waveforms in batch mode, automating what used to be a very manual process.

Because languages such as PSL and SVA efficiently describe the complex interaction of signals, assertions can be an ideal way to communicate testing needs between Register Transfer Language (RTL) and verification engineers. During a test plan review it can be much simpler to review assertions than the test code itself. An engineer writing RTL who is adept at writing assertions can also use this to their advantage by embedding critical coverage points into the design, which will give valuable feedback about the testing quality.

Once the infrastructure for tracking functional coverage through assertions during simulation is in place, engineers can have a better grasp of the overall test and test environment quality. This makes it easier to quickly answer questions such as:

- Do we currently have a test for *Feature X*? Which one?
- What types of bus activity does *Test Y* induce? What interrupts?
- I've written some randomization routines. Do they induce the behavior I'm expecting?
- What random seed value will produce the specific behavior I'm looking for?

Functional coverage is an important metric for evaluating the readiness of a design for tape out. Recent advances in language standards and tools support have made assertions an ideal choice for measuring functional coverage. Using coverage points to determine the pass/fail status of tests can add to the robustness of a test strategy. The added benefit that this type of approach can bring to the verification of a design is well worth the effort. **ECD**

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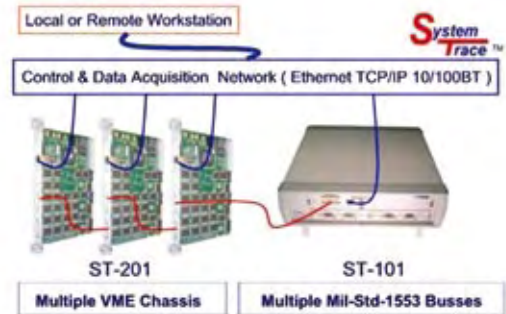
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