Amplifier-discriminator ASICs to read out thin Ultra-Fast Silicon detectors for ps resolution

A. Martinez Rojas, M. Ferrero, N. Cartiglia, R. Arcidiacono, F. Siviera, L. Menzio, M. Tornago, V. Sola, F. Fausti, J. Olave, M. Mandurrino

Istituto Nazionale di Fisica Nucleare, Turin, Italy.

Abstract— **This paper presents the FAST2 family of ASICs. FAST2 aims to keep the jitter below 20 picoseconds when coupled to Ultra-Fast Silicon detectors (UFSD). FAST2 is designed in standard 110 nm CMOS technology, and it comes in 2 versions: the amplifier-comparator version comprises 20 readout channels while the amplifier-only version of 16 channels. The ASIC power rail is at +1.2 V, and its power consumption is 2.4 mW/ch. In our tests, the FAST2 ASIC, coupled to a UFDS with a capacitance of 3.4 pF, achieves timing jitters lower than 15 ps, at an input charge of about 15 fC. In tests with an Sr90 beta source, the FAST2 reached a time resolution below 45 ps.**
The worst case of Near-end and Far-end crosstalk due to the mutual capacitance between neighboring channels achieves an amplitude of -23 dB at 50 W of load.

***Index Terms*—Silicon radiation detectors, Timing Jitter, UFDS, Ultra-Fast electronics, Crosstalk, CMOS technology.**

I. INTRODUCTION

The FAST2 family of ASICs has been designed to empower the realization of silicon trackers with an excellent temporal resolution (< 40 ps). Such silicon trackers are foreseen in future experiments to mitigate the pile-up effects [1] due to increased luminosity [2]. For this reason, front-end electronics with a timing jitter lower than 30 ps are required. Starting with these requirements, we have designed the FAST2 family of ASICs, the third generation of front-end electronics, following the TOFFEE and FAST1 ASIC [3][4].

The FAST2 family comprises three different ASICs: two (FAST2D_EVO1, FAST2D_EVO2) have 20 readout channels and implement an amplifier-comparator architecture, while the third ASIC (FAST2A) has 16 channels with only the amplification stage, 8 with the EVO1 front-end and 8 with the EVO2 front-end.
This contribution presents the first results obtained with the FAST2D_EVO1, and FAST2A ASICs coupled to a UFSD (Ultra-Fast Silicon Detector) with a capacitance equal to 3.4 pF. Two different setups were used: (i) a scanning-TCT system instrumented with a 1060 nm wavelength picosecond laser. In these tests, the laser intensity was tuned to generate a signal equivalent to that due to a minimum ionization particle (MIP). (ii) A beta telescope instrumented with 37.7 kBq Strontium-90 (Sr90) source.
The UFSDs were biased from 120 to 240 V during the tests, giving a signal from 5 to 30 fC. The TCT setup was mostly used to assess the FAST2 jitter performances as a function of the input signal. In the beta setup, the signal variation dominates the resolution due to non-uniform energy deposition, the so-called Landau noise.

II. ASIC ARCHITECTURE

The FAST2 prototypes have been designed in 110 nm CMOS technology. In the digital version (FAST2D), each readout channel is composed of a transimpedance (TIA) amplifier connected to a fast discriminator, as shown the Figure 1. The FAST2D_EVO1 implements a Pulse Width Regulator (PWR) to increase the width of the discriminator output waveform. This step is necessary to connect FAST2 to external commercial TDCs since often they require a minimum distance between the Time-of-Arrival and the Time-over-Threshold edges of at least 6-8 ns. The output signal uses an LVDS driver. In the FAST2A version, the discriminator is replaced by a simple driver to send the signal off-chip. FAST2 has 16 channels, 8 with the EVO1 architecture and 8 with the EVO2.

A local register of 12 bits controls each channel of FAST2D.
- 6 bits are used to program the local threshold of the discriminator. This local Vth compensation covers a range of 32 mV. It is used to eliminate the DC variation per channel
- The following 5 bits program the DC gain and signal shape of the pre-amplifier (8 selectable gains). This option allows the device to increase or reduce the DC gain. In this way, the front-end can guarantee a low jitter over a large range of input charges.
- The last bit of the local register enables the internal charge injection system.

A global register of 6 bits controls the amplitude of the calibration signal.

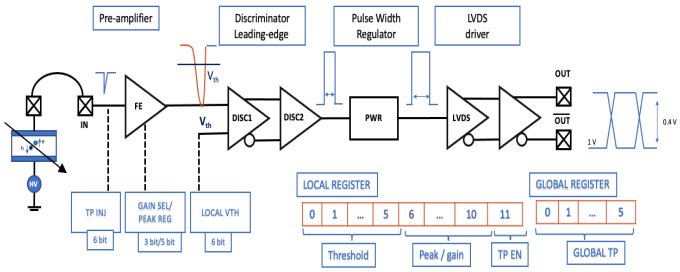

Figure 1. Full readout chain schematic of the FAST2_EVO1 ASIC.

The pre-amplifier stage implements a broad-band architecture with an nMOS input transistor topology. The nMOS topology guarantees a high-speed circuit [5]. The pre-amplifier architecture is divided into two stages, as shown the Figure 2. The first stage uses a common source topology with an auxiliary branch to provide the maximum drain current in the input transistor. A high drain current in the input transistor increases the transconductance and reduces the input resistance [6]. The first stage implements a close loop architecture with a variable gain since the R4 has eight selectable resistance values through 3 programmable bits.

The second stage presents a common source with a common gate cascode configuration. This architecture allows the Miller effect to be suppressed due to the absence of direct coupling of the output to the input port [7]. As a result, the circuit has relatively high bandwidth (> 400 MHz). This stage handles an open-loop configuration with a dc gain equal to 5. The second stage is connected at the input through an AC coupling to eliminate the DC component of the first stage.

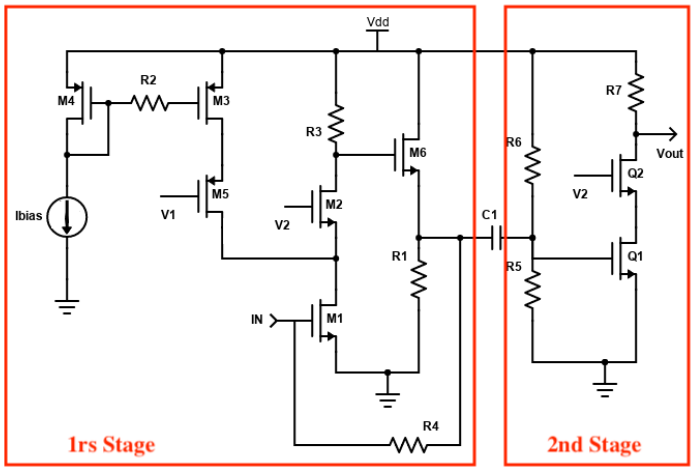

Figure 2. Broad-band architecture schematic.

The FAST2D_EVO1(2) ASIC includes a fast-timing discriminator stage. The leading-edge discriminator has a selectable threshold voltage. This architecture prevents the comparator from triggering on the baseline noise [8]. The discriminator is also biased at 1.2 V.

The length of the discriminator output signal can be increased via a pulse width regulator (PWR) [9]. This function is used to connect FAST2D to external Time to Digital Converters (TDC) that cannot operate with a pulse width of 2 ns. It is also possible to bypass the PWR stage entirely and have the comparator output signal of the same length as the analog input signal generated by the pre-amplifier circuit. The last stage is an LDVS driver that transmits the data off-chip, for instance, to an FPGA or to an oscilloscope.

III. Experimental Setup

The characterization of FAST2 connected to a UFSD sensor was performed using two different setups.

The first setup uses a scanning TCT system: the board hosting FAST2+UFSD is placed on a computer-controlled micrometric x-y stage. A 1060 nm wavelength picosecond laser is used to reproduce the energy deposited by a MIP. The laser intensity can be changed to map the energy range of a Landau distribution. The system is shown in Figure 3. Given the regularity of the signal generated by a laser, this system measures the jitter of FAST2.

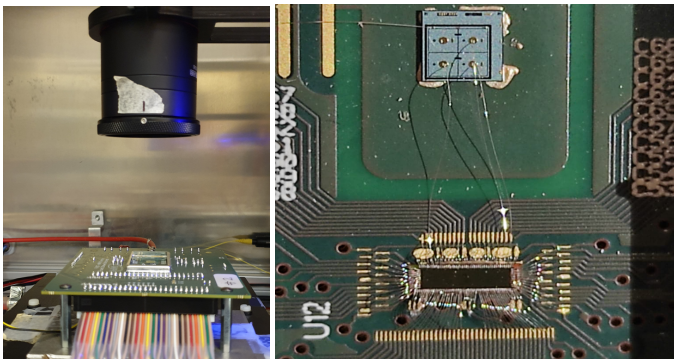

Figure 3. Scanning TCT system (left) FAST2_EVO1 ASIC and UFSD bonding to the PCB (right).

The second experimental setup is a "beta telescope" that uses a 37.7 kBq Sr90 source. The electrons from the source cross the UFSD and are detected by a triggering plane. This configuration assures that the energy of the electrons is high enough for them to be MIPs. In this measurement, both the jitter and the Landau contributions to the time resolution are present.

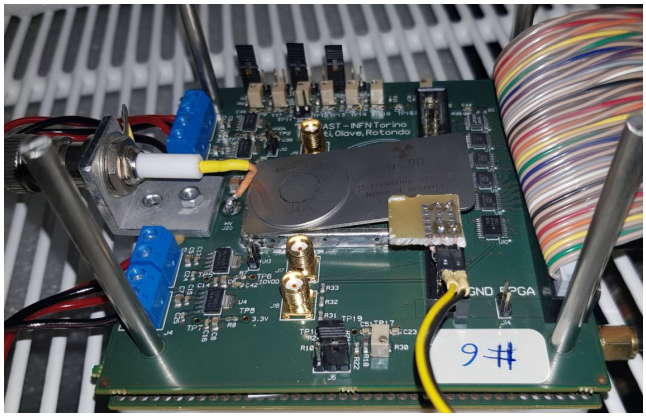

Figure 4. FAST2_EVO1 ASIC and UFSD bonding to the PCB using the Beta source (Sr90).

IV. Baseline Scan and Crosstalk

The baseline scan test is realized by lowering the threshold voltage to detect the position of the baseline value. When the threshold voltage approaches the baseline value, the discriminator starts firing. This procedure tests if a channel is ON or OFF, and what is its DC value. For the FAST2D_EVO1 ASICs tested so far, all channels are working. One example is shown the Figure 5.

Furthermore, we analyzed the baseline variation. A maximum variation of around 80 mV was measured; however, most channels show a much smaller deviation. About 80% of channels can be aligned using the local threshold adjustment.

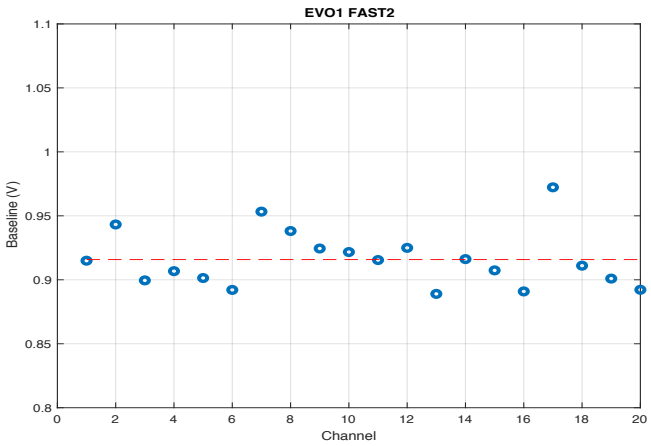

Figure 5. Output baseline value along the 20 readout channels of FAST2 evo1.

The Near-end and Far-end crosstalk can be defined as the disturbance in a channel due to the activity in one of the adjacent channels [10]. The results are shown in Figure 6. The graphic shows how the crosstalk, due to the capacitive coupling, increases as the amplitude of the signal increases. The crosstalk components are attenuated more than 23 dB at 50 W of load.

Figure 6 shows the Far-End crosstalk behavior since the Near-End presents negligible disturbances.

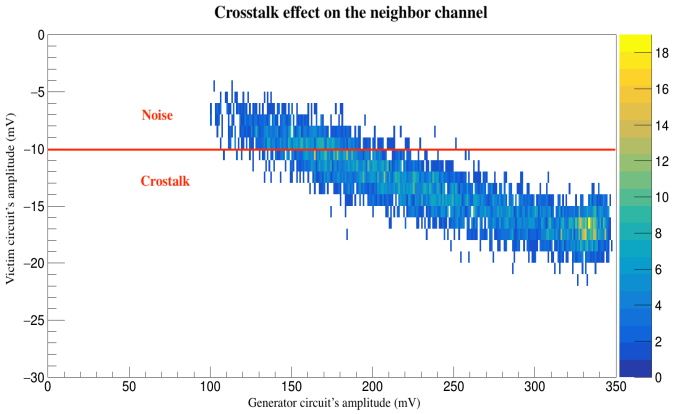

Figure 6. Far-end crosstalk behavior on the neighbor readout channel.

V. Temporal Resolution

The ASICs for timing, such as FAST2 and others [11][12], aim at minimizing the timing jitter (the jitter is defined as the RMS noise over the slope of the leading edge.) The jitter is measured using the scanning-TCT setup when the laser generates an amount of charge equivalent to that of a MIP. Since the energy deposition from a laser is uniform, the signals do not contain event-to-event variations: in this condition, the jitter is the dominant component of the temporal resolution. Figure 7 shows the output of FAST2A_EVO1. These waveforms allow us to analyze the performances of the first stage. In this figure, FAST2A has a rising time of about 1.5 ns, and an RMS noise equal to 1.5 mV. Figure 8 shows the output signal of FAST2D_EVO1.

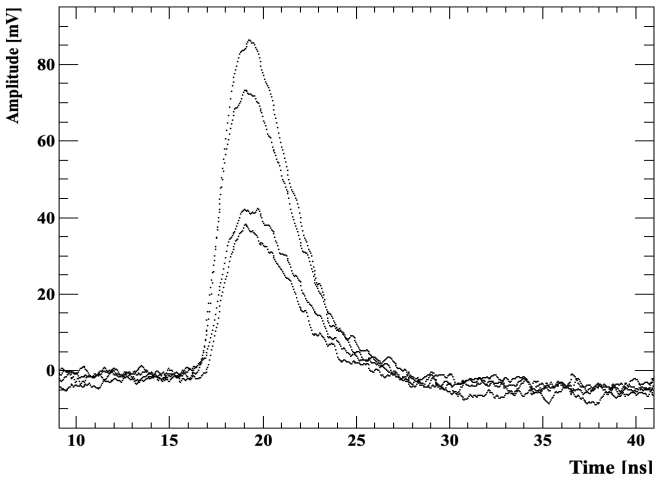

Figure 7. Output signal of pre-amplifier stage. The waveforms were obtained from different input charges.

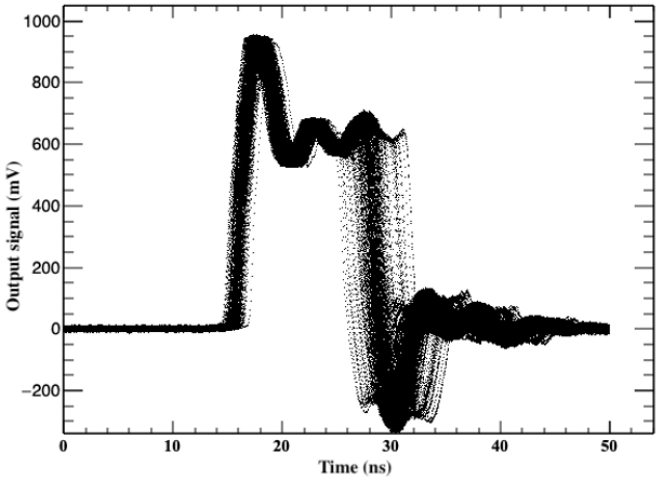

Figure 8. Output signal of FAST2 Evo1. The waveforms were acquired using a constant input charge.

The timing jitter as a function bias voltage of UFSD is reported in Figure 9. At high bias, i.e., for a signal charge of about 25 fC, FAST2 achieves a jitter of about 15 ps.

The second experimental test measures the temporal resolution of the UFSD-ASIC system using a beta telescope. Here, 2 MeV electrons from the Sr90 beta source are used to evaluate the combined time performances of the sensor and the front-end. The MIPs generate a non-uniform energy deposition, introducing signal variations, called Landau noise [8], leading to an additional uncertainty of around 30 ps. The combined time resolution can be expressed by Eq (1), keeping only the most important terms.

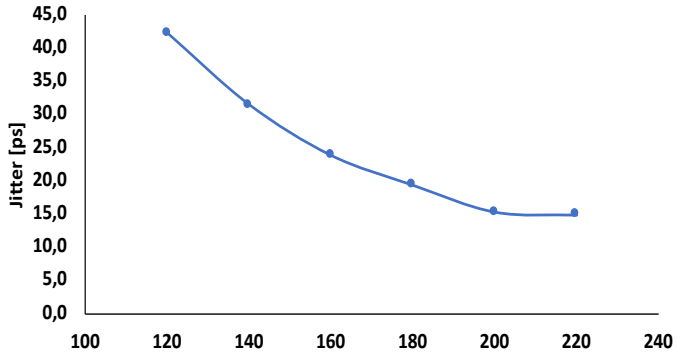

Figure 9. Timing performance of FAST2 using TCT scanning (timing jitter).

$$t_{resolution} = \sqrt{\sigma^2{}_{jitter} + \sigma^2{}_{landau}}, \quad (1)$$

The time resolution of FAST2D_Evo1 is about 40 ps for a bias voltage equal to 200 v, as shown in Figure 10. The time resolution is obtained by correcting the Time of Arrival (ToA) from the time walk effect.

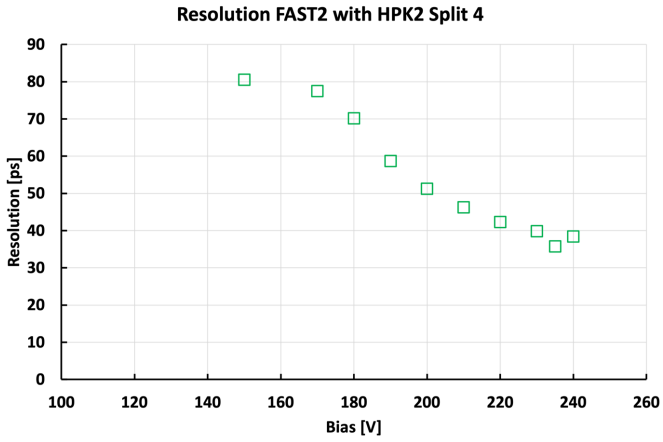

Figure 9. Timing performance of FAST2 using Beta source (combined time resolution).

The FAST2A EVO1 reaches a resolution of about 40 ps using a bias voltage of 200 V. The jitter and the time resolution of the analog version can be improved further by redesigning the output buffer and the second stage to reduce signal distortion due to saturation and open-loop gain. Thus, an optimization of FAST2 will be realized to reduce further the time resolution at the high bias voltage.

REFERENCES

[1] CMS collaboration, *A MIP Timing Detector for the CMS Phase-2 Upgrade*, CERN-LHCC-2019-003 [CMS-TDR-020] (2019).

[2] Soyez G, Pileup mitigation at the LHC, arXiv: 1801.09721v2 30 Jul 2019.

[3] J. Olave et al., Design and characterization of the FAST chip: a front-end for 4D tracking systems based on Ultra-Fast Silicon Detectors aiming at 30 ps time resolution," NIMA 985 (2021) 164615, HSTD12.

[4] J. Olave et al., A multichannel front-end readout ASIC for picosecond time resolution systems based on UFSD", JINST 15. C07012-C07012. 10.1088/1748-0221/15/07/C07012 July 2020.

[5] W. Sansen, Analog design essentials," Springer, pp. 166-168. 2006, ISBN: 978-0-387-25746-4.

[6] A. Rivetti, CMOS: Front-end electronics for radiation sensors," CRC press, January 2015.

[7] B. Razavi, Design of Analog CMOS Integrated Circuits," McGraw hill education, 2nd Edition, 2017 ISBN 978-0-07-252493-2.

[8] Yeong-Tsair Lin, et al. Integrated low-voltage pulse width modulation circuit using CMOS processes," The 3rd International IEEE-NEWCAS Conference, 2005.

[9] Clayton R. Paul, Transmission Lines in Digital and Analog Electronic Systems: Signal Integrity and Crosstalk," Wiley-IEEE Press, chapter 1.4.2, (2010).

[10] H.F.W. Sadrozinski, A. Seiden and N. Cartiglia, *4D tracking with ultra-fast silicon detectors*, *Rept. Prog. Phys.* **81** (2018) 026101 [arXiv:1704.08666].

[11] Anghinolfi, et al. NINO: An ultra-fast and low-power front-end amplifer/discriminator ASIC designed for the multigap resistive plate chamber," Nuclear Instruments and Methods in Physics Research, p. 183-187 (2004). Issn: 0168-9002.

[12] Ahmad, et al. Triroc: A Multi-Channel SiPM Read-Out ASIC for PET/PET-ToF Application", IEEE Transactions on Nuclear Science, 62 (2015).