Nos. 14-1076, -1317

United States Court of Appeals for the Federal Circuit

HTC CORPORATION and HTC AMERICA, INC.,

Plaintiffs-Cross-Appellants,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED,

Defendants-Appellants.

Appeals from the United States District Court for the Northern District of California in Case No. 5:08-cv-00882-PSG,
United States Magistrate Judge Paul S. Grewal

PRINCIPAL AND RESPONSE BRIEF OF PLAINTIFFS-CROSS-APPELLANTS HTC CORPORATION AND HTC AMERICA, INC.

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June 27, 2014

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Nos. 14-1076, -1317

CERTIFICATE OF INTEREST

Counsel for the Plaintiffs-Cross-Appellants HTC Corporation and HTC America, Inc. certifies the following (use "None" if applicable; use extra sheets if necessary):

1. The full name of every party or amicus represented by me is:

HTC Corporation and HTC America, Inc.

2. The name of the real party in interest (if the party name in the caption is not the real party in interest) represented by me is:

None.

3. All parent corporations and any publicly held companies that own 10 percent or more of the stock of the party or amicus curiae represented by me are:

HTC America, Inc. is a wholly owned subsidiary of HTC Corporation.

4: The names of all law firms and the partners or associates that appeared for the party or amicus now represented by me in the trial court or agency or are expected to appear in this court are:

Cooley LLP (formerly known as Cooley Godward Kronish LLP), Heidi L. Keefe, Mark R. Weinstein, Stephen R. Smith, Kyle D. Chen, Lam K. Nguyen, Neil N. Desai, Matthew J. Leary, Mark F. Lambert (all of Cooley LLP);

Ronald S. Lemieux, Jason C. Fan, Dena Chen, Lia C. Smith (all former counsel at Cooley LLP);

White & Case LLP, William S. Coats, III, Samuel C. O'Rourke, Taryn Lam, Jennifer Yokoyama, Wendi R. Schepler (all former counsel at White & Case LLP).

Dated: June 27, 2014

/s/ Heidi L. Keefe
Heidi L. Keefe

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STATEMENT OF RELATED CASES

Pursuant to Federal Circuit Rule 47.5(a), Plaintiffs-Cross-Appellants HTC Corporation and HTC America, Inc. (collectively "HTC") are unaware of any other appeal to this or any other appellate court from the district court action that is the subject of the pending appeal and cross-appeal.

Pursuant to Federal Circuit Rule 47.5(b), HTC is aware of eight other cases pending in the United States District Court for the Northern District of California that may be directly affected by this Court's decisions in the pending appeal and cross-appeal:

- *Technology Properties Ltd. et al. v. Barnes & Noble, Inc.*, Case No. 3:12-cv-03863-VC (N.D. Cal., filed July 24, 2012);
- *Technology Properties Ltd. et al. v. ZTE Corp. et al.*, Case No. 5:12-cv-03876-PSG (N.D. Cal., filed July 24, 2012);
- *Technology Properties Ltd. et al. v. Novatel Wireless, Inc.*, Case No. 4:12-cv-03879-PJH (N.D. Cal., filed July 24, 2012);
- *Technology Properties Ltd. et al. v. Nintendo Co., Ltd. et al.*, Case No. 3:12-cv-03881-JSW (N.D. Cal., filed July 24, 2012);
- *Technology Properties Ltd. et al. v. Garmin, Ltd. et al.*, Case No. 5:12-cv-03870-EJD (N.D. Cal., filed July 24, 2012) (closed);

- *Technology Properties Ltd. et al. v. Samsung Electronic Co. et al.*, Case No. 5:12-cv-03877-LHK (N.D. Cal., filed July 24, 2012);
- *Technology Properties Ltd. et al. v. LG Electronics, Inc. et al.*, Case No. 5:12-cv-03880-PSG (N.D. Cal., filed July 24, 2012); and
- *Technology Properties Ltd. et al. v. Huawei Technologies Co. et al.*, Case No. 4:12-cv-03865-PJH (N.D. Cal., filed July 24, 2012).

In each of these pending cases, two of the Defendants-Appellants, Technology Properties Ltd. and Patriot Scientific Corporation, are asserting U.S. Patent Nos. 5,809,336 (the "'336 patent") and 5,530,890 (the "'890 patent"), the same two patents that are the subject of the present appeal and cross-appeal. This Court's decisions in the present appeal and cross-appeal will be binding on Technology Properties Ltd. and Patriot Scientific Corporation and thus may directly influence the claim construction proceedings in these other pending actions and have a dispositive impact on them.

JURISDICTIONAL STATEMENT

The district court had subject matter jurisdiction over this patent infringement case pursuant to 28 U.S.C. §§ 1331, 1338(a), and 2201. On October 3, 2013, the district court entered a judgment following a verdict in which a jury found that HTC literally infringed the patent-in-suit (the "Original Judgment"). (A0218 at Dkt. Nos. 654-55, A0125-29.)

On October 31, 2013, HTC timely filed a renewed motion for judgment as a matter of law ("JMOL") under Federal Rule of Civil Procedure 50(b) (A0219 at Dkt. No. 671, A9009-18, the "Renewed JMOL") and a motion to correct/amend judgment under Federal Rule of Civil Procedure 60(a)/59(e) (A0219 at Dkt. No. 674, the "Motion To Amend Judgment") (collectively, the "Post-Judgment Motions"). Under Federal Rules of Appellate Procedure 4(a)(1)(A) and 4(a)(4)(A), the filing of the Post-Judgment Motions tolled the deadline to file a notice of appeal.

On January 21, 2014, the district court issued an order denying the Renewed JMOL (A0222 at Dkt. No. 707, A0130-44), an order granting-in-part the Motion To Amend Judgment (A0223 at Dkt. No. 708, A0145-47), and an order modifying the Original Judgment (A0223 at Dkt. No. 709, A0148-49), thus disposing of all Post-Judgment Motions. On February 20, 2014, HTC timely filed its notice of appeal. (A0224 at Dkt. No. 725.) This Court therefore has appellate jurisdiction over HTC's cross-appeal under 28 U.S.C. § 1295.

STATEMENT OF THE ISSUES

I. ISSUES CONCERNING HTC'S CROSS-APPEAL ON THE '336 PATENT

HTC's cross-appeal involves a straightforward question of the proper construction of the "entire oscillator" limitation found in both of the two asserted independent claims of the '336 patent. This cross-appeal presents the following issues:

1. Did the district court err in declining to construe "entire oscillator" as excluding an oscillator that relies on an input control signal from an external (off-chip) clock to determine the oscillator's frequency, notwithstanding the repeated disclaimers and disavowals the '336 patent applicants made throughout the intrinsic evidence?

2. Did the district court err in denying HTC's renewed motion for judgment as a matter of law of non-infringement, given that the undisputed evidence at trial demonstrated that HTC's accused products operate precisely as those disclaimed in the intrinsic evidence, even under the district court's claim construction?

II. ISSUES CONCERNING TPL'S APPEAL ON THE '890 PATENT

TPL's appeal concerning the '890 patent presents the following issue:

1. Was the district court correct in granting summary judgment in favor of HTC that absolute intervening rights barred any claims of infringement based on activities occurring prior to March 1, 2011, the issuance date of the *ex parte*

reexamination certificate, considering that TPL amended and substantively narrowed every asserted claim of the '890 patent during the reexamination?

TPL stipulated to an order dismissing all claims under the '890 patent (A7223.006-10) because the district court's intervening rights ruling precluded liability for all HTC products accused of infringing the '890 patent. (A7223.007.) Affirmance of the district court's intervening rights ruling would dispose of TPL's appeal and render it unnecessary to consider the second issue raised by TPL below. Only if this Court reverses the intervening rights ruling would TPL's appeal present the following second issue:

2. Did the district court correctly construe the phrase "separate direct memory access central processing unit" as recited in claim 11 of the '890 patent?

As noted, this second issue is unrelated to and will not affect the district court's intervening rights ruling.

STATEMENT OF THE CASE

The central issue presented by HTC's cross-appeal concerns the proper construction of the "entire oscillator" limitation recited in each of the two asserted independent claims of the '336 patent (*i.e.*, claims 6 and 13). The district court submitted this case to the jury based on an unclear and incomplete claim construction that resulted in an erroneous finding of literal infringement.[1]

Before trial, the district court issued an order denying HTC's motion for summary judgment of non-infringement (A0009-11), but in that order, held that the "entire oscillator" limitation should be "properly understood to exclude any external clock used to generate a signal." (A0011.) The district court based this claim construction ruling on arguments in the intrinsic record that the applicants made to distinguish the prior art. (A0011 n.24.) The district court incorporated this aspect of the claim construction into the jury instructions at trial.

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[1] HTC's cross-appeal is based on the district court's January 21, 2014 order denying HTC's Renewed JMOL (A0130-44). HTC's cross-appeal is also based on the order modifying the Original Judgment (A0148-49, 1/21/2014), the order granting-in-part the Motion To Amend Judgment (A0145-47, 1/21/2014), the Original Judgment (A129, 10/3/2013), the jury verdict (A0125-28, 10/3/2013), the jury note (A9007, 10/2/2013), the order denying JMOL (under Fed. R. Civ. P. 50(a)) (A0124, 10/2/2013), the final jury instructions (A0079-123, 09/30/2013), the order on addendum to jury instructions (A0077-78, 09/20/2013), the order clarifying jury instructions (A0078.001-02, 09/23/2013), the order regarding HTC's motions for summary judgment (A0001-23, 09/17/2013), the final claim construction order (A0050-67, 08/21/2013), the interim claim construction order (A0047-49, 12/04/2012), and the first claim construction order (A0024-46, 06/12/2012).

Although the district court correctly recognized that the '336 patent applicants had disclaimed certain subject matter during prosecution, the court's construction did not completely capture what was disclaimed. HTC accordingly asked the district court to clarify its claim construction (and its instructions to the jury) to make clear that the applicants did not just disclaim an oscillator that uses an external clock to generate a clock signal, but also disclaimed an oscillator whose frequency is determined by an input control signal (*e.g.*, from an external (off-chip) crystal clock). (A7224-26.) HTC pointed out numerous places in the prosecution history where the '336 patent applicants specifically disclaimed the use of such an input control signal in order to overcome the prior art. (*See*, *e.g.*, A7236-38; A7276-78 at 38:17-40:25; A7283-84 at 45:9-46:7.)

At the hearing on HTC's motion to amend the district court's claim construction, TPL's counsel admitted that, under HTC's proposal, TPL could not show infringement and "should have judgment taken against us and then we can take our appeal." (A7281-82 at 43:17-44:3.) The district judge then asked TPL's counsel, "[s]o if I were simply to instruct the jury that the disputed limitations exclude any external clock that is used to generate [the] signal,[nothing more, nothing less,] would you have any problem with that?" (A7282-83 at 44:4-10, 44:25-45:1-3.) TPL's counsel responded: "No, because we win." (A7283 at 45:4.)

Following this exchange, the district court declined to include HTC's proposed clarification, and the case proceeded to trial.

The evidence at the jury trial, from experts and fact witnesses for both sides, confirmed what TPL's counsel had represented – that TPL could not show infringement under the "entire oscillator" construction if properly clarified as requested by HTC. The undisputed evidence showed that the oscillator in all of the accused HTC products relied on an input control signal from an external (off-chip) clock to determine the oscillator's frequency. The evidence also established non-infringement even under the incomplete construction adopted by the district court because the oscillator in all of the accused HTC products uses an external clock frequency in generating the signal used to clock the CPU.

At trial, after denying HTC's motion for judgment as a matter of law under Federal Rule of Civil Procedure 50(a) (A8968-80), the district court instructed the jury using the incomplete "entire oscillator" claim construction. The jury apparently did not understand the district court's construction because, during its deliberations, the jury asked the district court to clarify the meaning of "generate" in "any external clock used to generate the signal." The district court provided no further guidance to the jury. (A9007.)

The jury subsequently returned a verdict of literal infringement and awarded damages of $958,560, about 10% of what TPL had requested. (A0125-28; A8156

at 856:15-17; A7125, A7161-63.) The jury also found that HTC's infringement was not willful, and found for HTC on indirect infringement. (A0125-28.) The district court then denied HTC's Renewed JMOL (A0130-44), and this cross-appeal followed (A0224 at Dkt. No. 725).

STATEMENT OF THE FACTS

I. FACTS CONCERNING HTC'S CROSS-APPEAL

A. The '336 Patent

1. Background

The '336 patent generally relates to techniques for clocking a central processing unit ("CPU"). By way of background, the CPU in a microprocessor integrated circuit or "chip," which is a silicon substrate[2] where the circuitry is made, consists of millions of transistors[3] that perform the CPU's operations. To ensure that these millions of transistors operate in harmony, the CPU relies on a timing signal known as a "clock" signal to coordinate the timing of such operations. The process of providing this timing or "clock" signal to the CPU is known as "clocking the CPU."[4]

This "clock" signal is generated by a clocking device such as an "oscillator," which oscillates to generate a periodic "high" or "low" signal akin to the tick-tock

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[2] *See* A7892 at 18-20 ("Integrated circuit, or, … 'chip' [are the same thing.]"); *see also* 7890-91 at 591:19-592:1 ("A substrate … is silicon die or piece of silicon. … So it is on the same … Integrated circuit, or [on] the same chip, [or] on the same die[. They are synonymous.]").

[3] A transistor works like an electrical switch, which depending on its operations turns on or off. (*See*, *e.g.*, A7845 at 546:9-11 ("In a digital world, the transistor is like a switch, so it is on or off …."); *see also* A7846 at 547:4-14 ("[On a modern microprocessor, e]verything is made out of transistors. … [The CPU is made out of transistors] entirely.").)

[4] *See*, *e.g.*, A0040-41; A0103 at ¶ 14 ("The term 'clocking said central processing unit' means 'providing a timing signal to said central processing unit.'").

in a mechanical clock, which can be used to clock the CPU.[5] How fast this periodic high/low signal alternates is known as the oscillator's "frequency," "speed," or "clock rate," often measured in a unit called "hertz" (equal to one cycle per second).[6]

2. The '336 Patent Purports To Clock the CPU with "a Familiar Ring Oscillator," Whose Speed Varies in Response to Parameters Associated with the Microprocessor Chip.

The '336 patent purports to disclose an allegedly novel way of clocking a microprocessor's CPU using an "entire oscillator" placed on a microprocessor chip. Because the transistors in a CPU depend on electrical signals to operate, their maximum speed for proper operation is constrained by the amount of time necessary for the electrical signals to propagate (*i.e.*, transmit) through them, known as the "transistor propagation delays." The '336 patent explains that these propagation delays generally depend on three parameters associated with the

[5] *See*, *e.g.*, A7510 at 213:14-16 ("[In the context of computers, a] clock is a periodic signal that is used to determine when an instruction begins and when it ends."); *see also* A7452 at 155:13-14 ("It's actually very similar to the tick, tock, tick, tock of a normal clock that we're all familiar with."); *see also* A7830 at 531:14-15 ("To oscillate means to change periodically the output of the signal.")

[6] *See*, *e.g.*, A7453 at 156:14-15 ("[W]hen we talk about the speed of a clock, there's a special word that we use to refer to that and that's frequency."); *see also* A7826 at 527:14-22 ("Frequency means how often something changes …. Generally in technical term, we define frequency in hertz. 1 hertz means it changes one per second. 2 hertz means change twice per second. 1 megahertz means it changes one million times per second. 1 gigahertz means one billion times per second.").

microprocessor chip: (1) the manufacturing **p**rocess ("P") used in fabricating the chip, (2) the **v**oltage ("V") supplied to the chip, and/or (3) the **t**emperature ("T") of the chip. (A0254 at 16:47-48.) TPL's expert at trial referred to these as the "PVT" parameters. (*See*, *e.g.*, A8022 at 722:4-12.)

The '336 patent states that the CPU's maximum speed for proper operation depends on these PVT parameters, which can vary widely. (A0254 at 16:44-47 ("The designer of a high speed microprocessor must produce a product which operate [*sic*] over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing.").) If the temperature ("T") of the microprocessor chip rises, for example, the CPU's maximum speed for proper operation decreases in response. (A0254 at 16:59-67.) Conversely, if the temperature decreases, the CPU's maximum speed increases in response. (*Id.*)

The patent goes on to explain that prior art CPU designs dealt with these variations by restricting the CPU to a frequency that was slow enough to account for the worst case combination of PVT parameters:

> Traditional CPU designs are done so that with the worse [*sic*] case of the three parameters, the circuit will function at the rated clock speed. The result [*sic*] are designs that must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse [*sic*] case conditions.

(A0254 at 16:48-53.)

But prior art designs setting the frequency based on the worst case conditions had a significant drawback – they failed to take advantage of the full performance potential of the microprocessor. (A4571 (January 1997 Amendment) ("Under other than worst case operating conditions, the prior art microprocessors are actually capable of operating at a faster clock speed than their rated speed.").)

The '336 patent purports to overcome this issue by providing a clocking device whose frequency can vary (or change) with the varying PVT parameters associated with the microprocessor chip. To that end, the '336 patent discloses a clocking device, "a familiar 'ring oscillator'" already well known in the prior art, made of the same transistors as the CPU and located on the same microprocessor chip as the CPU. (A0254 at 16:54-58.) According to the '336 patent, the "familiar" ring oscillator would thus respond to the PVT parameters in the same way as the CPU because they are both made of the same transistors and subject to the same PVT parameters. The '336 patent claims that, as a result, the speed of the ring oscillator and the CPU's maximum speed for proper operation would vary together in the same way in response to the varying PVT parameters. (A0254 at 16:59-67.) In doing so, the '336 patent explains:

> By deriving system timing from the ring oscillator **430,** CPU **70** will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die [or chip[7]] is not good resulting in slow transistors, the latches and gates on the

[7] *See supra* n.2.

> microprocessor **50** will operate slower than normal. Since the microprocessor **50**[’s] ring oscillator clock **430** is made from the same transistors on the same die [or chip] as the latches and gates, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip’s logic to operate properly.

(A0254-55 at 16:67-17:10 (emphasis added).) As the ’336 patent applicants further explained:

> Crucial to the present invention is that since both the oscillator or variable speed clock and [the] driven device [*i.e.*, the CPU] are on the same substrate, when the fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device [*i.e.*, the CPU] will automatically vary together.

(A4538.)

3. The Prosecution History Makes Clear that the Claimed “Entire Oscillator” Does Not Rely on an Input Control from an External Clock To Determine Its Frequency.

During the prosecution of the ’336 patent, the Examiner rejected the proposed claims based on two primary references: U.S. Patent No. 4,670,837 to Sheets (A5494-501, “Sheets”) and U.S. Patent No. 4,503,500 to Magar (A5460-92, “Magar”). The applicants repeatedly distinguished these prior art references by arguing that the claimed on-chip “oscillator” did not rely on an external (off-chip) clock or a command input to determine its frequency.

a. Sheets

As described by the ’336 patent applicants, the Sheets reference disclosed a voltage-controlled oscillator (“VCO 12”) whose frequency was determined by a

signal that specified the oscillator's desired operating frequency. (A4564; *see also* A5498 (Sheets) at 2:55-56 ("voltage-controlled oscillator (VCO)".) In an attempt to overcome the prior art in their April 1996 response (A4557-66), the '336 patent applicants argued that Sheets failed to disclose an on-chip oscillator on the same chip as the CPU. (A4564.) But as the '336 patent applicants acknowledged in their January 1997 response (A4568-72), the Examiner expressly disagreed.[8]

The '336 patent applicants responded by emphasizing a second argument – that Sheets was distinguishable because its clock frequency was determined by a clock control signal supplying frequency control information:

> *Even if the Examiner is correct that the variable clock in Sheets is in the same integrated circuit as the microprocessor of system 100, that still does not give the claimed subject matter*. In Sheets, a command input is required to change the clock speed. In the present invention, the clock speed varies correspondingly to variations in operating parameters of the electronic devices of the microprocessor because both the variable speed clock and the microprocessor are fabricated together in the same integrated circuit. No command input is necessary to change the clock frequency.

(A4571 (emphasis added).)

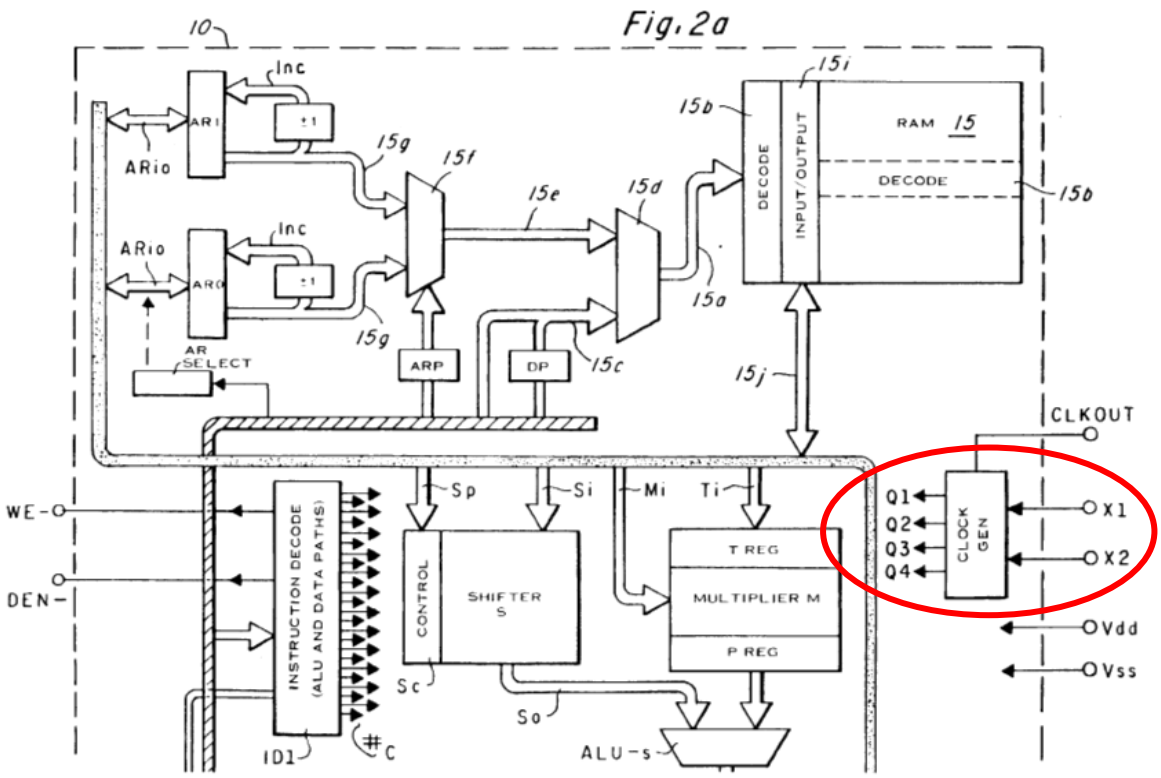
In short, the applicants distinguished Sheets by arguing that the on-chip oscillator of the claimed invention does not rely on frequency control information, such as a "command input," to determine its frequency. (A4564, A4571.)

[8] *See* A4571 (January 1997 response) ("[T]he Examiner contends that the Sheets reference 'clearly indicates in lines 46-48 of column 2 that the system 100 shown in Figure 1 is fabricated *on a single chip* using MOS technology.'") (emphasis in original).

b. Magar

The applicants made similar arguments in responding to the Examiner's rejections based on Magar, which was the next reference cited by the Examiner to reject the '336 patent claims. The applicants' responses to Magar again drove home the point that the frequency of the claimed "entire oscillator" is not determined by frequency control signals from an external crystal clock.

Figure 2a below from Magar shows the system that was distinguished by the applicants (red circle on bottom left showing clock circuitry "CLOCK GEN"):



(A5462 (red circle added).)

In their July 1997 response to the Examiner (A1173-77), the '336 patent applicants described the chip shown in Figure 2a of Magar as having "a clock generator 17 which has two external pins X1 and X2 to which a crystal (or external generator) is connected." (A1174 (citing to "col. 15, lines 26-41 of Magar").) The applicants went on to argue that Magar was distinguishable from the claimed invention because, like the accused HTC products, the frequency of the clock was determined by an external (off-chip) crystal clock:[9]

> Contrary to the Examiner's assertion in the rejection that 'one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock vary together due to manufacturing variation, operating voltage and temperature of the IC', one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock *do not* vary together due to manufacturing variation, operating voltage and temperature of the IC in the Magar microprocessor, as taught in the above quotation from the reference. This is simply because the Magar microprocessor clock is **frequency controlled** by a crystal which is also external to the microprocessor. Crystals are by design fixed-frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The Magar microprocessor in no way contemplates a variable speed clock as claimed.

(A1175-76 (first italics in original, boldface and underlining added).) The applicants further distinguished Magar by arguing that the claimed invention

[9] An external crystal clock is an off-chip, crystal-based oscillator that generates a clock signal. (*See*, *e.g.*, A7555 at 257:1-2 ("Almost all computers had a crystal oscillator, a separate off-chip device that would generate a clock signal for them.").)

excludes an oscillator whose frequency is controlled, even if the oscillator is fabricated on the same integrated circuit as the CPU:

> [C]rystal oscillators have never, to Applicants' knowledge, been fabricated on a single silicon substrate with a CPU, for instance. Even if they were, as previously mentioned, crystals are by design fixed-frequency devices whose oscillation frequency is designed to be **tightly controlled** and to vary minimally due to variations in manufacturing, operating voltage and temperature. The oscillation frequency of a crystal on the same substrate with the microprocessor would inherently not vary due to variations in manufacturing, operating voltage and temperature in the same way as the frequency capability of the microprocessor on the same underlying substrate, as claimed.

(A1176 (emphasis added).)

The applicants filed a subsequent response in February 1998 (A1168-72) and again argued that "the essential difference" between the invention and Magar is that the frequency of the oscillator in the '336 patent is determined by the PVT parameters, whereas Magar's clock frequency is "determined by … the external crystal":

> The signals PHASE 0, PHASE 1, PHASE 2, and PHASE 3 in Applicants' Fig. 18 are synonymous with Q1, Q2, Q3, and Q4 depicted in Magar Fig. 2a. The *essential difference* is that the frequency or rate of the PHASE 0, PHASE 1, PHASE 2, and PHASE 3 signals is determined by the processing and/or operating parameters of the integrated circuit containing the Fig. 18 circuit, *while the frequency or rate of the Q1, Q2, Q3, and Q4 signals depicted in Magar Fig. 2a are determined by the fixed frequency of the external crystal* connected to the circuit portion outputting the Q1, Q2, Q3, and Q4 signals shown in Magar Fig. 2a.

(A1171 (emphasis added).) Finally, the applicants summarized their arguments:

> The Magar teaching is well known in the art as a conventional ***crystal controlled*** oscillator. It is specifically distinguished from the instant case in that it is both fixed frequency *(being crystal based)* and requires an external crystal or external frequency generator.

(A1172 (emphasis added).)

The applicants' arguments regarding Sheets and Magar, therefore, clearly and unequivocally disavowed an oscillator whose frequency is determined by a control signal, whether taking the form of the "command input" in Sheets or the external crystal clock in Magar. The applicants emphasized that the purpose of the claimed invention was instead to provide an on-chip oscillator whose frequency would automatically vary in response to variations in manufacturing process or operating parameters such as temperature and voltage. (A1177.) An on-chip oscillator whose frequency depends on a control signal to determine its frequency, as the applicants argued, would defeat this purpose.

B. Claim Construction Proceedings Before Trial

HTC filed a motion for summary judgment of non-infringement (A0200, Dkt. No. 457; A0202, Dkt. No. 477), in which HTC asked the district court to construe the claimed "entire oscillator" (A4291-300) and to find non-infringement because, among other reasons, HTC's accused products do not satisfy the "entire oscillator" limitation under its proper construction (A4300-03).

The district court denied HTC's motion, but ruled that the disputed "entire oscillator" claim limitation should be "properly understood to exclude any

external clock used to generate a signal," based on statements in the prosecution history of the '336 patent. (A0011 n.24.) The district court articulated the factual issue for trial as: "whether HTC's products contain an on-chip ring oscillator that is self-generating and does not rely on an input control to determine its frequency." (A0011 (emphasis added).)

HTC subsequently filed a motion to clarify the district court's claim construction to specify that the term "entire oscillator" excludes an on-chip oscillator that relies on an input control (*e.g.* from an off-chip crystal clock) to determine the oscillator's frequency, as the file history and the district court's order contemplated. (A7224-26; A7236-38; A7276-78 at 38:17-40:25; A7283-84 at 45:9-46:7; A7286-87 at 48:3-49:6.)

At the hearing on HTC's motion,[10] TPL's counsel conceded that the '336 patent applicants did disclaim subject matter in distinguishing Magar,[11] but argued that the disclaimer did not pertain to controlling the frequency of an on-chip oscillator. (A7282 at 44:11-19.) He also admitted to the district court that "if …

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[10] The hearing effectively turned into a further claim construction hearing for the "entire oscillator" limitation in claims 6 and 13, and similar "entire" terms in other independent claims of the '336 patent. By the time of trial, however, TPL had dropped all independent claims except claims 6 and 13.

[11] For example, the '336 patent applicants told the Examiner that "Magar's clock generator relies on an external crystal connected to terminals X1 and X2 to oscillate[.]" (A1170.)

the court instructs the jury that they [*i.e.*, HTC] don't infringe because an external crystal is used to determine the frequency or set the frequency or control the frequency -- … we [*i.e.*, TPL] should have judgment taken against us and then we can take our appeal. … You know, obviously I don't want that, but I just don't want to waste the court's time or the parties' time." (A7281-82 at 43:17-44:3.) The judge then asked TPL's counsel, "[s]o if I were simply to instruct the jury that the disputed limitations exclude any external clock that is used to generate [the] signal,[nothing more, nothing less,] would you have any problem with that?" (A7282 at 44:4-10, 25; A7283 at 45:1-3.) TPL's counsel responded: "No, because we win." (A7283 at 45:4.)

The district court subsequently declined to include the additional guidance from the summary judgment order that HTC requested. (*See* A0078.001-002.) The district court did not express its reasons for this decision, but held that the claim construction issue was preserved for appeal. (A0137-39 at 8:11-10:3; A8758 at 1456:16-21.) The district court's final instruction to the jury on the meaning of "entire oscillator" was simply:

> The term 'entire oscillator' (in claims 6 and 13) is properly understood to exclude any external clock used to generate the signal used to clock the CPU.

(A0104 (Final Jury Instructions at 26:4-5).)

But that construction, as HTC had predicted, was ultimately insufficient to resolve the jury's confusion over the proper claim construction, and resulted in an erroneous finding of literal infringement.

C. The Trial Evidence Showed that All HTC Products Contain an Oscillator that Relies on an Input Control Signal from an External Clock To Determine the Oscillator's Frequency.

At trial, TPL's technical expert, Dr. Vojin Oklobdzija, confirmed what TPL's counsel conceded before trial – that the on-chip oscillator in the HTC accused products relies on an input control signal from an external (off-chip) crystal clock to determine the oscillator's frequency. His testimony confirmed that the accused HTC products use the CPU clocking mechanism that had been disavowed by the applicants in distinguishing Sheets and Magar.

As Dr. Oklobdzija acknowledged, although each accused HTC product may include a chip made by Qualcomm, Texas Instruments ("TI"), or Samsung, "they generally work the same way." (A8034 at 734:10-18.) Each accused chip includes an on-chip Phase Locked Loop ("PLL"),[12] which is a device that includes an oscillator and relies on an external crystal clock to determine the frequency of

[12] The use of a PLL to clock a microprocessor was well known in the prior art before the '336 patent, of which the priority date is August 3, 1989. (A0227.) For example, U.S. Patent No. 4,689,581 to Talbot ("Talbot"), issued on August 25, 1987, disclosed an "Integrated Circuit **Phase Locked Loop** Timing Apparatus" (as in its title) to clock a microcomputer. (A1145-56) (emphasis added). TPL distinguished a related claim term, "ring oscillator," from Talbot. (*See*, *e.g.*, A1158-61.)

the oscillator (for clocking the CPU).[13] In particular, the PLL relies on a "reference" signal from the external crystal clock, which is, according to Dr. Oklobdzija, "essential" to the PLL. (A8037-38 at 737:17-738:2.) That external crystal clock produces a "stable" reference signal that "is used to adjust the frequency generated by the ring oscillator [to clock the CPU], so it has some relationship with it." (A8038 at 738:9-13.) In fact, the purpose of the PLL is to adjust the frequency of the on-chip oscillator based on that external crystal clock reference. (A8046 at 746:11-18; *see also* A7852-53 at 552:16-553:11.) The evidence at trial confirmed that all of the accused products use such a PLL to determine and control the on-chip oscillator's frequency.[14]

Dr. Oklobdzija also acknowledged that there is a formula contained "in every textbook" that defines the on-chip oscillator's frequency as a function of

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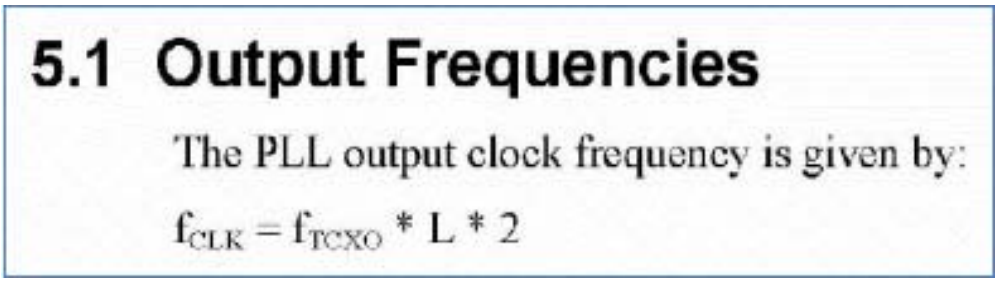
[13] *See*, *e.g.*, A8034 at 734:19-22; A8035-36 at 735:2-736:5; A8036 at 736:9-11; A8044-45 at 744:15-745:3.

[14] *See*, *e.g.*, A9041 (the "TCXO 19.2MHz" signal goes through the "PM7540" chip and then into the "Clock" inside the Qualcomm "MSM7201A" chip); A9043-45 (the "TCXO" in Fig. 12-1 on A9045); A9316-17; A9050-52 ("TCXO_HV" in Figure 2-1 on A9051); A9054 (the "CLKTCXO" in the "OMAP850" chip receiving the "26MHz" frequency from the external "EDGE module"); A9057 (the "CK_REF" signal goes into the "DPLL1" block); A9058 ("The DPLL block synthesizes a frequency clock from the fixed reference input clock signal CK_REF using the digital phase-locked loop mechanism."); A9060-63 (Trial Ex. 3100 at A9061-62) ("The main clock source comes from an external crystal (XTlpll) or an external clock (EXTCLK). The clock generator includes an oscillator (Oscillator Amplifier), which is connected to an external crystal, and also has two PLLs (Phase-Locked-Loop), which generate the high frequency clock required in the SC32442A.").

the frequency of the reference signal from the external crystal clock. (A8035 at 735:2-5; A8039 at 739:12-24; A8049 at 749:4-6.) The Qualcomm, TI, and Samsung chips included in HTC's products all use such a formula to determine the frequency of the oscillator's signal used to clock the CPU. (A8034 at 734:10-18.) Although the notation used to express this formula may differ from chip to chip, in each case the formula expressly relies on the frequency of the external crystal clock to determine the frequency of the on-chip oscillator.[15]

One example of such a formula (for a Qualcomm chip (A9072-73)) was discussed during Dr. Oklobdzija's cross-examination:



(A9073.)

The formula shown above states that the output frequency of the on-chip clock (f_{CLK}) equals: the frequency of the external crystal clock (f_{TCXO}),[16]

[15] *See*, *e.g.*, A9050-52 (Trial Ex. 3112 at A9052); A9056-58 (Trial Ex. 3115 at A9058); A9060-63 (Trial Ex. 3100 at A9063); A9065-66 (Trial Ex. 3101 at A9066); A9068-69 (Trial Ex. 3117 at A9069).

[16] *See* A8346 at 1045:8-10 ("TCXO … stands for temperature compensated crystal oscillator.").

multiplied by a parameter "L" and 2. (A8043 at 743:5-20.) Thus, the frequency of the on-chip oscillator is determined in part by the frequency of the external clock (f_{TCXO}). It is also determined by the "L" value, which can be selected by a manufacturer depending on what it wanted to achieve in its product, as admitted by Dr. Oklobdzija. (A8046 at 746:8-18.) The document showing this formula also included a table providing examples of how to achieve specific desired output frequencies for the on-chip oscillator in the PLL by "plugging-in" certain values into the formula. (A9073, Table 5-1; A8043-46 at 743:21-746:18, A8048-49 at 748:22-749:6.)

D. Closing Arguments and Jury Deliberations Turned on Questions of Claim Construction – Not How the Products Operate.

As noted previously, the district court instructed the jury that "[t]he term 'entire oscillator' (in claims 6 and 13) is properly understood to exclude any external clock used to generate the signal used to clock the CPU." (A0104.) Regrettably, this construction was insufficient to inform the jury of the proper claim scope and required the parties to argue claim construction to the jury.

In closing argument, for example, TPL did not dispute that all accused HTC products include an external clock that controls the frequency of the on-chip oscillator. (A8854 at 1551:16-18.) Instead, TPL argued this fact was irrelevant to whether or not HTC's products met the "entire oscillator" limitation. All that mattered, according to TPL, was that the on-chip oscillator generated *its own*

signal for clocking the CPU. To illustrate his argument, TPL's counsel analogized the on-chip oscillator to a fast sports car following behind a slow recreational vehicle (RV) on the road. TPL's counsel asked the rhetorical question: "But is the RV and the engine in that motor home, is that used to generate the clock signal, or the engine power for the sports car?" (A8855 at 1552:18-20.) His response: "No way. No way. The sports car has its own engine, generates its own power." (A8855 at 1552:20-21.)

HTC argued, on the other hand, that its products did not satisfy the "entire oscillator" limitation because the on-chip oscillator used the external crystal clock's frequency in generating the clock signal used to clock the CPU. HTC pointed to the undisputed testimony at trial, from multiple witnesses, confirming that the output of the PLL in each accused HTC product expressly depended on the reference signal from the external crystal clock. (A8875 at 1572:15-23; A8882-83 at 1579:18-1580:14.) Whether the on-chip oscillator physically generated its own signal was irrelevant, in other words, because the external crystal clock was indisputably "used" in the process of generating the signal that clocked the CPU, and therefore, fell within the district court's exclusion. (A8891-92 at 1588:16-1589:18.)

The confusion that HTC predicted before trial was confirmed during jury deliberations, when the jury sent out a note asking for the "court[']s definition of

'generate' [in "any external clock used to generate the signal used to clock the CPU" on] pg 26 lines 4&5 [in the final jury instructions]." (A9007; A0104 (Final Jury Instructions at 26:4-5).) The district court held a hearing on how to respond to the jury's question. HTC's counsel observed at the hearing that "this is exactly what we were worried about when we were asking for clarification of your definitions, because it seems like the jury is now engaging in claim construction instead of applying facts." (A8947 at 1643:5-8.) But because the case had already been tried and submitted to the jury based on the district court's existing construction, it was too late to provide any further guidance. (A8947 at 1643:14-18.) The district court accordingly responded to the jury that "[t]he court has no further definition." (A9007.) The jury subsequently returned a verdict of literal infringement and awarded damages of $958,560. (A0125-28.)

E. Post-Verdict Proceedings

Following the jury verdict, HTC renewed its motion for judgment as a matter of law. (A9009-18.) At the hearing for HTC's renewed motion, TPL's counsel again confirmed that if HTC's interpretation of the claims was correct, TPL could not show infringement: "[a]nd I said [before trial], if what [the court's] construction means in the summary judgment order is that an external clock or an external crystal can't be used … for frequency regulation, then I lose and we shouldn't go to trial." (A9153-54 at 16:25-17:3.)

II. FACTS CONCERNING TPL'S APPEAL

A. TPL Had Ample Notice of HTC's Intention To Defend Based on Intervening Rights Due to Reexamination of the '890 Patent.

On November 21, 2008, TPL filed a counterclaim against HTC accusing it of infringing the '890 patent. (A0167 at Dkt. No. 60.) HTC answered on December 11, 2008, and at that time, no *ex parte* reexamination had been filed against the '890 patent yet. HTC accordingly did not plead a defense of intervening rights. (A0167 at Dkt. No. 65.) As explained below, however, TPL had ample notice early in the litigation that HTC intended to defend based on intervening rights to the extent the defense was justified by the reexamination.

As early as 2009, HTC raised the intervening rights issue. In April 2009, the Patent Office granted a request for *ex parte* reexamination of the '890 patent filed by an anonymous third-party requester. (A0328.003 at 2:23-26; *see also* A0328.012-.025.) In light of the reexamination, HTC moved to stay the litigation. (A0328.001-.011; A0328.026-.037.) HTC specifically argued that "to the extent the claims subject to reexamination [including those in the '890 patent] are narrowed …, the scope of this case will be significantly reduced by the doctrine of 'intervening rights'" because there would be "no liability for any allegedly infringing activities that took place prior to the date of issuance of the reexamination certificate …." (A0328.007 at 6:20-28; *see also* A0328.029 at

3 n.2).) HTC notified TPL of the intervening rights issue again in a subsequent case management statement. (A0328.038-045 (A0328.042 at 5:9-18).)

B. The Examiner Relied on a New Claim Limitation Added During Reexamination in Allowing New Claim 11, While Finding Claim 1 Without the Additional Limitation Unpatentable.

TPL was, in the meantime, attempting to defend the '890 patent in the *ex parte* reexamination. (A6060-71.) The Examiner found independent claim 1 unpatentable based on various prior art references. In order to overcome the prior art, TPL canceled claim 1 and added a new independent claim 11, which was identical to claim 1 but included an additional limitation: "said stack pointer pointing into said first push down stack." (A0328, A6067-68.) The Examiner relied exclusively on this new limitation in finding the new claim 11 (and its dependents) allowable over the prior art. (A6067-68.) On March 1, 2011, the Patent Office issued an *ex parte* reexamination certificate reflecting the cancellation of claim 1 and the addition of claim 11 with the new limitation mentioned above. (A0318, A0328.)

Based on the results of the *ex parte* reexamination, the district court granted-in-part a motion by TPL to amend its infringement contentions to assert the new claim 11 of the '890 patent and claims 12, 13, 17, and 19 depending from claim 11. (A0076.) The district court also allowed TPL to amend its infringement contentions to accuse additional HTC products. (*Id.*)

C. The District Court Granted HTC's Motion for Summary Judgment Based on Intervening Rights.

As it said it would, HTC filed a motion for summary judgment based on absolute intervening rights for the '890 patent. (A5972-83.) The motion argued that HTC could have no liability for alleged infringement under the '890 patent for any activities that took place prior to March 1, 2011, the date of issuance of the reexamination certificate. (A5974-76.) The district court granted the motion. (A0021.) TPL subsequently stipulated to an order dismissing all claims under the '890 patent (A7223.006-10) because the summary judgment order precluded liability for all HTC products accused of infringing the '890 patent. (A7223.007.)

D. The District Court Twice Rejected TPL's Proposed Construction for "Separate Direct Memory Access Central Processing Unit."

TPL's appeal also raises the question of the proper construction of the term, "separate direct memory access central processing unit" in the '890 patent. This issue is separate and unrelated to the district court's intervening rights ruling that TPL challenges in its appeal. With respect to the claim construction issue, the district court construed this term in June 2012 (A0036), further modified the construction in December 2012 (A0048), and confirmed the modified construction in August 2013 (A0063). The district court has twice rejected the construction that TPL is now again proposing to this Court. (A0034-36, A0061-63.)

SUMMARY OF ARGUMENT

I. SUMMARY OF ARGUMENT FOR HTC'S CROSS-APPEAL

The central issue presented by HTC's cross-appeal concerns the proper construction of the "entire oscillator" limitation recited in each of the two asserted independent claims of the '336 patent. The case went to the jury on the issue of infringement under an incomplete and confusing claim construction that resulted in an erroneous finding of literal infringement.

The district court's construction of "entire oscillator" only partially identified the subject matter that the '336 patent applicants disclaimed during prosecution. The court held that "entire oscillator" is "properly understood to exclude any external clock used to generate the signal used to clock the CPU." (A0104.) Although the district court correctly recognized that the '336 patent applicants had disclaimed certain subject matter, the construction failed to articulate the full scope of those disclaimers.

The district court's construction did not capture the fact that the applicants repeatedly told the Patent Office that the claimed on-chip "entire oscillator," unlike the prior art, operated at a frequency that was *not* determined by an input control signal from an external (off-chip) clock, such as an external crystal clock. The applicants made clear, in the specification and prosecution history of the '336 patent, that the purpose and the benefit of the claimed "entire oscillator" were to

run at a frequency not constrained by the frequency of an external crystal clock and therefore to run at the fastest safe frequency based on the combination of PVT parameters. In other words, the applicants did not only disclaim an "entire oscillator" that does not use an external clock "to generate the signal used to clock the CPU," as the district court held, but also disclaimed the use of an input control from an external clock to determine the oscillator's frequency. The applicants obtained the '336 patent by criticizing, distinguishing, and disavowing the very type of clocking systems employed by all of HTC's accused products.

The district court articulated the factual issue for the jury as: "whether HTC's products contain an on-chip ring oscillator that is self-generating and does not rely on an input control to determine its frequency." (A0011 (emphasis added).) But the district court failed to provide that clarifying language to the jury, leaving the he jury with an incomplete claim construction. That construction proved so unhelpful that the jury asked the district court to clarify its meaning, but the district court could provide no further guidance. (A9007.) The jury's confusion was understandable, considering that the technical witnesses on both sides agreed on how the accused HTC products operated, which transformed the entire trial into the question (ultimately unanswered) of what it means to "generate" a clock signal under the district court's incomplete construction.

Despite the jury's confusion and the resulting erroneous verdict of infringement, the undisputed evidence at trial established that HTC's products do not infringe any asserted claim. The witnesses on both sides testified that all of HTC's accused products include an oscillator whose frequency directly relies on an input control from an external crystal clock – precisely the type of clocking system the '336 patent applicants disclaimed during prosecution. The evidence and trial further established that, even under the district court's incomplete construction, HTC's products did not infringe because they included an oscillator that depended on an external clock's frequency to generate the clock signal for the CPU.

TPL therefore cannot establish infringement of the '336 patent under either the correct claim construction or the incomplete one adopted by the district court. This Court should therefore reverse the district court and remand with instructions to enter judgment of non-infringement in HTC's favor.

II. SUMMARY OF ARGUMENT FOR TPL'S APPEAL ON THE '890 PATENT

After the commencement of litigation in the district court, an anonymous third party filed a request for *ex parte* reexamination of the '890 patent. In an attempt to overcome prior art cited by the Examiner in that reexamination, TPL amended its sole independent claim to add a limitation not recited in any original claim. TPL's amendment convinced the Examiner to allow the amended claims over the prior art, and a reexamination certificate issued in March 2011.

HTC subsequently moved for summary judgment on the ground that TPL could not recover for any act of alleged infringement prior to March 2011 under the doctrine of absolute intervening rights. After the district court granted HTC's motion, TPL stipulated to an order dismissing all claims under the '890 patent (A7223.006-10) because the summary judgment order precluded liability for all HTC products accused of infringing the '890 patent. (A7223.007, A7199-200.)

TPL's appeal raises two issues concerning the district court's intervening rights ruling – one procedural issue, and one substantive issue. TPL first argues that the district court erred in considering absolute intervening rights on summary judgment because HTC did not plead it as a defense in its answer. But under Ninth Circuit law, a district court may consider an affirmative defense raised for the first time on summary judgment when, as here, there is no prejudice to the non-moving party. The district court in the present case correctly found that TPL did not suffer unfair prejudice from the assertion of intervening rights, and therefore, chose to consider HTC's arguments. TPL has shown no error, let alone an abuse of discretion, in the district court's decision.

TPL spends an inordinate amount of time on this procedural issue because it knows that the district court's intervening rights ruling is legally unassailable on the merits. TPL's arguments consist of little more than an assertion that a limitation it added to its claims during reexamination – upon which the Examiner

expressly relied in allowing the claims over the prior art – was meaningless surplusage that did not change the scope of the claims. But the intrinsic record reveals otherwise. New claim 11 added a limitation requiring that the "stack pointer" recited in the claim "point[] into said first push down stack," changing the scope of claim 11 and all claims that depend from it. Because claim 11 has a different scope from the original claim 1 it replaced, the district court correctly applied the doctrine of absolute intervening rights.

TPL's appeal also challenges the district court's construction of the term "separate direct memory access central processing unit" ("separate DMA CPU"). TPL primarily argues that the district court erred in adopting a construction of "separate DMA CPU" that excludes the "DMA controller" devices of the prior art. But as the district court correctly observed, the '890 specification draws a clear distinction between a DMA CPU and a DMA controller, and the plain language of the claim term recites a "CPU" and does not cover a DMA controller. TPL's reliance on restriction requirements that occurred early in the prosecution is misplaced because those requirements mentioned nothing about "separate DMA CPU" and are entitled to little, if any, weight. Thus, TPL has identified no error in the district court's construction.

ARGUMENT

I. ARGUMENT FOR HTC'S CROSS-APPEAL

A. Standard of Review

This Court reviews decisions on motions for judgment as a matter of law ("JMOL") under the law of the regional circuit, in this case the Ninth Circuit. *See Verizon Servs. Corp. v. Cox Fibernet Va., Inc*., 602 F.3d 1325, 1331 (Fed. Cir. 2010). "The Ninth Circuit reviews the denial of JMOL *de novo*." *Integrated Tech. Corp. v. Rudolph Techs., Inc*., 734 F.3d 1352, 1356 (Fed. Cir. 2013) (citing *Hangarter v. Provident Life & Accident Ins. Co*., 373 F.3d 998, 1005 (9th Cir. 2004)). "In the Ninth Circuit, JMOL is appropriate after a jury trial when a party has been fully heard on an issue and there is no legally sufficient evidentiary basis for a reasonable jury to find for that party on that issue." *Id.* (citation and quotation marks omitted).

Claim construction is a legal issue that this Court reviews *de novo*. *Lighting Ballast Control LLC v. Philips Elecs. N. Am. Corp*., 744 F.3d 1272, 1276-77 (Fed. Cir. 2014) (*en banc*). "When a patent infringement verdict is based on an incorrect claim construction, we reverse the trial court's denial of a motion for judgment as a matter of law if no reasonable jury could have found infringement under the proper claim construction." *800 Adept, Inc. v. Murex Sec., Ltd*., 539 F.3d 1354, 1366 (Fed. Cir. 2008); *Finisar Corp. v. DirecTV Grp., Inc*., 523 F.3d 1323, 1333 (Fed. Cir. 2008). Moreover, "[i]f no reasonable jury could have found infringement

under the proper claim construction, this court may reverse a district court's denial of JMOL without remand." *Id.*

B. The District Court Erred in Declining To Construe "Entire Oscillator" To Reflect the Disclaimers the '336 Patent Applicants Made During Prosecution.

The district court's construction of "entire oscillator," although incomplete, correctly recognized that the applicants had disclaimed certain subject matter during prosecution of the '336 patent. The district court held that the "entire oscillator" term is "properly understood to exclude any external clock used to generate a signal." (A0011.) HTC does not disagree with this holding to the extent it comports with the part of the prosecution history it reflects. But the district court legally erred in declining to clarify for the jury the meaning of this exclusion and capture the full scope of the disclaimers made by the applicants during prosecution. The '336 patent applicants repeatedly emphasized that the "entire oscillator" is not simply a self-generating oscillator that does not require an external (off-chip) clock to generate a clock signal. Another essential characteristic of the "entire oscillator" emphasized by the applicants was its ability to provide a frequency not constrained or otherwise determined by an input control signal from an external (off-chip) clock or a command input.

This Court's rules governing claim construction are well-established. In construing claims, this Court looks primarily to the "intrinsic" evidence including

the language of the claims, the specification, and the prosecution history. *See generally Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). Claim construction is an issue of law for the court to decide. *O2 Micro Int'l. Ltd. v. Beyond Innovation Tech. Co*., 521 F.3d 1351, 1360 (Fed. Cir. 2008). "When the parties raise an actual dispute regarding the proper scope of these claims, the court, not the jury, must resolve that dispute." *Id*.

"The purpose of consulting the prosecution history in construing a claim is to 'exclude any interpretation that was disclaimed during prosecution.'" *Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) (citation omitted). "Accordingly, 'where the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender.'" *Id*. (citation omitted); *see also, e.g.*, *Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1325 (Fed. Cir. 2002) ("Explicit arguments made during prosecution to overcome prior art can lead to narrow claim interpretations because 'the public has a right to rely on such definitive statements made during prosecution.'") (citation omitted).

Although this Court's precedents require that a disclaimer of subject matter be clear and unmistakable, they do not require that an applicant use any particular magic words to effectuate a disclaimer. "Where an applicant argues that a claim possesses a feature that the prior art does not possess in order to overcome a prior

art rejection, the argument may serve to narrow the scope of otherwise broad claim language." *Seachange Int'l, Inc. v. C-COR Inc.*, 413 F.3d 1361, 1372-73 (Fed. Cir. 2005); *see also Shire Dev., LLC v. Watson Pharms., Inc.*, 746 F.3d 1326, 1330 (Fed. Cir. 2014) ("[B]y distinguishing the claimed invention over the prior art, an applicant is indicating what the claims do not cover [and] he is by implication surrendering such protection.") (quoting *Ekchian v. Home Depot, Inc.*, 104 F.3d 1299, 1304 (Fed. Cir. 1997)).

1. The Purpose of the Claimed "Entire Oscillator" Was To Clock a CPU that Operates at the Fastest Safe Frequency.

The '336 patent specification (of over 30 columns) describes various aspects of a microprocessor system, but only three paragraphs of that description (spanning approximately half of one column) actually pertain to the disputed "entire oscillator" limitation. (A0254-55 at 16:43-17:10.) As discussed in section I.A.2 in the Statement of the Facts above, that portion of the specification explains that CPUs are designed to operate over wide variety of PVT parameters. (A0254 at 16:44-47.) Prior art CPUs, according to the specification, suffered from the drawback of being designed to always operate at a rated clock speed that is slow enough to function properly even under the worst case combination of PVT parameters. (A0254 at 16:48-53.) By accounting for the worst case conditions, in other words, prior art designs do not take advantage of the full performance potential of the microprocessor. (A4571.)

The ’336 patent sought to address this perceived problem by providing a microprocessor system in which the oscillator was “fabricated on the same silicon chip as the rest of the microprocessor **50**,” which includes the CPU **70**. (A0254 at 16:57-58.) According to the ’336 patent, the on-chip oscillator is thus exposed to the same PVT parameters as the CPU. (A0254-A0255 at 16:67-17:2.) “This allows the microprocessor to operate at its fastest safe operating speed, given its manufacturing process or changes in its operating temperature or voltage.” (A4570-71.) The ’336 applicants amplified these points during prosecution in an attempt to distinguish the prior art.

2. The District Court’s Construction Erroneously Failed to Include Applicants’ Disclaimer of an Oscillator that Relies on an External (Off-Chip) Clock Signal To Determine the Oscillator’s Frequency.

As fully discussed in section **I.A.3** in the **Statement of Facts** above, the Examiner rejected the proposed claims based primarily on the Sheets and Magar references. The applicants repeatedly distinguished these references by arguing that the claimed on-chip “oscillator” did not rely on a command input or an external (off-chip) clock to determine the frequency of the on-chip oscillator. The applicants emphasized that the purpose of the claimed invention was instead to provide an on-chip oscillator whose frequency would automatically vary in response to variations in manufacturing process or operating parameters such as

temperature and voltage. (A1177.) An on-chip oscillator whose frequency depends on a control signal to determine its frequency would defeat this purpose.

As this Court has made clear, "[t]he public notice function of a patent and its prosecution history requires that a patentee be held to what he declares during the prosecution of his patent." *Springs Window Fashions LP v. Novo Indus., L.P.*, 323 F.3d 989, 995 (Fed. Cir. 2003). The district court acknowledged the applicants' disclaimers regarding frequency control when it articulated the issue for trial as "whether HTC's products contain an on-chip ring oscillator that is self-generating and does not rely on an input control to determine its frequency." (A0011 (emphasis added).) But the district court's construction never gave the jury the tools to resolve this infringement question at trial because the incomplete construction did not capture the fact that the frequency of an "entire oscillator" may not depend on an external (off-chip) clock or a command input.

The district court's incomplete construction enabled TPL to argue to the jury that there was a difference between (a) an external clock used to perform the *actual* generation of the CPU clock signal, and (b) an external clock used to regulate or adjust the frequency at which the CPU clock signal is generated. According to TPL, only the former was excluded by the district court's construction, while the latter was not. This argument was misleading because, as the applicants' disclaimers made clear, a clock signal is generated at a frequency

and is defined by its frequency. Generation of the clock signal, and the frequency at which the clock signal is generated, are interrelated and inseparable concepts, but the district court's construction enabled TPL to misleadingly separate those concepts in its arguments to the jury.

This point was recognized in a parallel infringement action brought by TPL in the International Trade Commission ("ITC") against HTC and several other respondents. The ITC rejected TPL's infringement claim under the '336 patent by finding that, among other things, the accused products did not satisfy the "entire oscillator" limitation. The ITC expressly rejected the distinction TPL argued to the jury in the instant case by observing that the process of generating a clock signal "includes more than simply delivering sufficient power to enable the oscillator to oscillate." (Request for Judicial Notice (filed herewith), Ex. A, at 30.) It correctly observed that "the process of setting the frequency of a clock signal and generating a clock signal are inseparable, because a clock signal must have a frequency, since it[s] sole purpose is to provide a frequency for timing the operations of devices." (*Id.*)[17]

For all of the reasons in section **I.A.3** in the **Statement of Facts** above, the district court erred in failing to construe the "entire oscillator" limitation as

[17] TPL did not appeal the ITC's ruling of no infringement to this Court, and the time for doing so has passed.

excluding an oscillator whose frequency is determined by an input control, whether taking the form of the "command input" in Sheets or the external crystal clock in Magar.

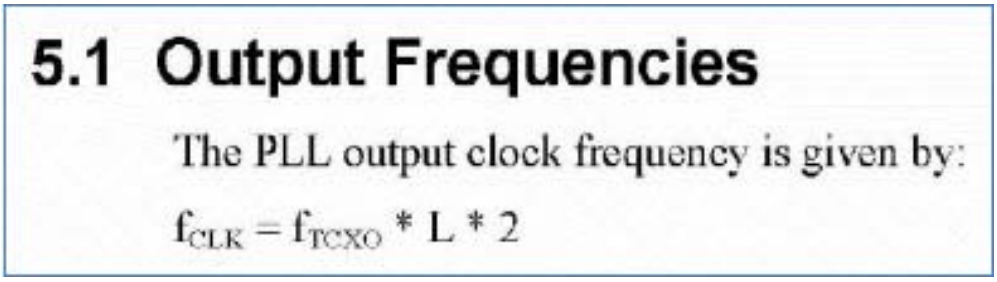
C. No Reasonable Jury Could Find Literal Infringement of Any Accused HTC Product Under the Correct Construction of "Entire Oscillator."

As explained in section **I.A.3** in the **Statement of Facts** above, the '336 patent applicants repeatedly distinguished their invention from prior art microprocessors with oscillators whose frequency was controlled by a command input or an external crystal clock. But in the district court, TPL based its infringement claims against HTC's products upon their accused microprocessors that operate in precisely the same way that the '336 patent applicants criticized and disavowed during prosecution. As this Court has made clear, "[a] patentee may not state during prosecution that the claims do not cover a particular device and then change position and later sue a party who makes that same device for infringement." *Springs Window Fashions, LP*, 323 F.3d at 995. But this is exactly what TPL has done here.

This Court has made clear that "[i]f no reasonable jury could have found infringement under the proper claim construction, this court may reverse a district court's denial of JMOL without remand." *Finisar Corp.*, 523 F.3d at 1333. This is such a case. As explained in section **I.B** in the **Statement of the Facts** above,

TPL's counsel conceded both before and after the trial that if "entire oscillator" is construed as excluding an oscillator whose frequency was determined by an external crystal, HTC's products would not infringe the '336 patent. (A7281-82 at 43:17-44:1 (before trial); A9153-54 at 16:25-17:3 (reiterating after trial: "I said [before trial], if what [the court's] construction means in the summary judgment order is that an external clock or an external crystal can't be used … for frequency regulation, then I lose and we shouldn't go to trial.").) The evidence at trial confirms TPL's concession.

As explained in section **I.C** in the **Statement of the Facts** above, it is undisputed that the microprocessor chips in all of HTC's accused products include a Phase Locked Loop ("PLL") that controls the accused oscillator's frequency according to a formula similar to the following one:



5.1 Output Frequencies

The PLL output clock frequency is given by:

$f_{CLK} = f_{TCXO} * L * 2$

(A9073.) The formula establishes that the output frequency of the on-chip oscillator (f_{CLK}) equals the frequency of the external crystal clock (f_{TCXO}), multiplied by the command input value "L," and then multiplied by 2. (A8042-49 at 742:24-749:6.)

As TPL's counsel recognized, therefore, it is undisputed that all HTC products contain an oscillator whose frequency is determined based on the frequency of an external crystal clock (f_{TCXO}). The oscillator in HTC products also relies on a selectable command input value (L) to determine its frequency. Because the claimed "entire oscillator" is properly construed as excluding an oscillator whose frequency is controlled in this manner, HTC's accused products do not meet the "entire oscillator" limitation. No reasonable jury could find, based on the undisputed evidence, that HTC's accused products infringe under the correct construction of the "entire oscillator" limitation. This Court should accordingly reverse the district court's denial of JMOL and direct the district court to enter judgment of non-infringement for HTC.

D. No Reasonable Jury Could Find Infringement of HTC's Accused Products Even Under the District Court's Incomplete Construction.

The district court construed "entire oscillator" as excluding only an oscillator that uses an external clock to generate the signal used to clock the CPU, but declined to further specify that the "entire oscillator" may not rely on an input control to determine its frequency. Even if this Court concludes that the district court was correct in not incorporating the latter requirement into its construction, judgment as a matter of law was still required because the evidence at trial established non-infringement of all accused HTC products.

The district court's construction of the "entire oscillator" limitation stated that an external clock may not be "used" to generate the signal used to clock the CPU." (A0078.002.) But all HTC accused products use an external crystal clock for this precise purpose. As explained in the previous section, the clocking signal in all HTC accused products comes from an on-chip PLL that outputs a clocking signal that is defined by a precise mathematical formula that includes the frequency of the external (off-chip) crystal clock. TPL conceded as much in closing argument, asserting that the external crystal clock is "**used** to limit or regulate the speed of the clock signal that is generated by the ring oscillator." (A8854 at 1551:16-18 (emphasis added).) Because that external clock is indisputably "used" in generating the signal used to clock the CPU (of which the frequency is an inherent part during generation), HTC's accused products fall squarely within the type of devices excluded by the district court's construction of "entire oscillator." Because no reasonable jury could find infringement of HTC's products, even under the district court's incomplete construction, this Court should reverse the district court's denial of JMOL and direct the district court to enter judgment for HTC.

II. ARGUMENT FOR TPL'S APPEAL ON THE '890 PATENT

A. Standard of Review

TPL appeals the district court's grant of summary judgment of absolute intervening rights on the '890 patent. TPL's appeal first challenges the district court's decision to even consider HTC's intervening rights argument on summary judgment. This Court has reviewed this procedural decision for abuse of discretion. *See Ultra-Precision Mfg., Ltd. v. Ford Motor Co.*, 411 F.3d 1369, 1376 (Fed. Cir. 2005).[18] This Court reviews the substantive merits of the district

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[18] This Court's decision in *Ultra-Precision* involved the Sixth Circuit law. HTC has not located any Ninth Circuit authority setting forth the standard of review when a district court considers an affirmative defense raised for the first time on a dispositive motion. Other circuits, however, review such a decision for abuse of discretion. *See, e.g., Ultra-Precision*, 411 F.3d at 1376 (applying Sixth Circuit law); *Levy Gardens Partners 2007, L.P. v. Commonwealth Land Title Ins. Co*., 706 F.3d 622, 633 (5th Cir. 2013); *Sanders v. Dep't of Army*, 981 F.2d 990, 991 (8th Cir. 1992) (*per curiam*). HTC believes that Ninth Circuit law is consistent with an abuse of discretion standard here for at least two reasons.

First, the district court's decision to allow an affirmative defense to be considered on summary judgment has substantially the same effect as allowing an amendment to HTC's answer under Federal Rule of Civil Procedure 15(b), which would be reviewed for abuse of discretion under Ninth Circuit law. *See, e.g., C.F. ex rel. Farnan v. Capistrano Unified Sch. Dist*., 654 F.3d 975, 983 (9th Cir. 2011) ("[R]equests for leave to amend an answer are reviewed for abuse of discretion."). There is no reason to apply a different standard of review here given that the district decision was tantamount to allowing HTC to amend its answer at the time it filed its motion for summary judgment.

Second, the Ninth Circuit consistently applies the abuse of discretion standard to procedural issues incident to summary judgment rulings. *See, e.g., Wong v. Regents of Univ. of Cal.*, 410 F.3d 1052, 1060 (9th Cir. 2005) ("Rulings regarding evidence made in the context of summary judgment are reviewed for an abuse of

court's grant of summary judgment *de novo*. *Brain Life, LLC v. Elekta Inc.*, 746 F.3d 1045, 1052 (Fed. Cir. 2014).

B. The District Court Did Not Abuse Its Discretion or Commit Clear Error in Finding that HTC Could Raise Absolute Intervening Rights on Summary Judgment.

TPL contends that the district court erred in allowing HTC to raise an absolute intervening rights defense on summary judgment. Under Ninth Circuit law, however, a party may raise an affirmative defense for the first time in a motion for summary judgment so long as the timing of the assertion does not prejudice the opposing party. *See*, *e.g.*, *Panaro v. City of N. Las Vegas*, 432 F.3d 949, 952 (9th Cir. 2005); *Camarillo v. McCarthy*, 998 F.2d 638, 639 (9th Cir. 1993) ("In the absence of a showing of prejudice, however, an affirmative defense may be raised for the first time at summary judgment."); *Rivera v. Anaya*, 726 F.2d 564, 566 (9th Cir. 1984) ("Our circuit liberalized the requirement that affirmative defenses be raised in a defendant's initial pleading …."); *see also Stored Value Solutions, Inc. v. Card Activation Techs., Inc.*, 499 F. App'x 5, 7 (Fed. Cir. 2012) (district court properly considered written description defense raised for the first

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discretion."); *Pickern v. Pier 1 Imports (U.S.), Inc.*, 457 F.3d 963, 968-69 (9th Cir. 2006) (abuse of discretion standard applied to district court decision to exclude expert testimony as untimely on summary judgment); *Michelman v. Lincoln Nat'l Life Ins. Co.*, 685 F.3d 887, 892 (9th Cir. 2012) (abuse of discretion standard applied to district court's decision on whether to continue summary judgment motion to allow further discovery). HTC believes that an abuse of discretion standard should therefore apply.

time on summary judgment because defense was based on claim limitations added during reexamination completed after the filing of the suit).

The district court here did not abuse its discretion in allowing HTC to assert a defense of absolute intervening rights on summary judgment. The district court's decision was predicated on a factual finding that TPL had failed to show prejudice to bar HTC's defense as required by Ninth Circuit law. (*See* A0018-19 at 18:23-19:2.) The district court noted that "TPL does not, for example, articulate the discovery it might have otherwise taken had HTC promptly moved to amend its answer in 2011." (*Id.* at 18:24-19:2.) TPL's argument before the district court regarding prejudice, in fact, amounted to nothing more than a bare assertion that "allowing HTC to raise this affirmative defense for the first time on summary judgment would … unfairly prejudice TPL." (A6171 at 7:5-6.) The district court did not abuse its discretion in concluding that TPL was not prejudiced by the assertion of intervening rights on summary judgment.

Nor could TPL credibly have claimed any prejudice or unfair surprise. As explained in Section **II.A** of the **Statement of the Facts** above, HTC notified TPL of the intervening rights issue at multiple points early in the litigation. TPL had

clear notice that HTC intended to raise intervening rights after the issuance of the reexamination certificate. (A0328.007 at 6:20-28; *see also* A0328.029 at 3 n.2.)[19]

TPL's opening brief asserts, for the first time on appeal, that it would have taken further discovery to oppose summary judgment based on intervening rights, and therefore, was prejudiced. (TPL Op. Br. at 8-9, 12-16.) But TPL did not present any of those arguments to the district court, and therefore, cannot raise them on appeal. *See Fresenius USA, Inc. v. Baxter Int'l, Inc.,* 582 F.3d 1288, 1296 (Fed. Cir. 2009) ("If a party fails to raise an argument before the trial court, or presents only a skeletal or undeveloped argument to the trial court, we may deem that argument waived on appeal, and we do so here."). TPL's arguments concerning prejudice are meritless, however, even if considered.

The lack of prejudice to TPL is underscored by the purely legal nature of the absolute intervening rights issue. The intervening rights issue turns on a straightforward question of whether the scope of the asserted claims substantively changed during the reexamination – a purely legal question of claim construction.

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[19] TPL asserts that HTC stated in briefing to the district court that the scope of the original and reexamined claims in the '890 patent was identical. (Principal Brief for Defendants-Appellants Technology Properties Limited, *et al.* ("TPL Op. Br."), Case Nos. 14-1076, -1317, Doc. No. 27, at 15.) This is untrue. HTC repeatedly argued that the reexamined claims were narrower. (*See*, *e.g.*, A0413 at 10:3-4 ("[T]he new claims introduce narrowing limitations that will require additional analysis to locate those limitations in the prior art."); *see also* A0409 at n.2 ("[HTC] does not concede that the newly issued claims have the same scope as the original claims, <u>*but rather, contends that the new claims are narrower.*</u>" (emphasis added).)

Laitram Corp. v. NEC Corp., 163 F.3d 1342, 1346-47 (Fed. Cir. 1998). HTC's motion presented only a question of claim construction, not a factual issue that would have required any discovery.[20] Finally, TPL fully briefed the merits of the intervening rights issue in the opposition brief it filed with the district court, which included a lengthy expert declaration. TPL had a full and fair opportunity to present its response. The district court did not abuse its discretion in considering HTC's intervening rights arguments.

C. The District Court Correctly Found that TPL Substantively Changed the Scope of the '890 Patent During Reexamination.

As discussed above, the '890 patent was involved in an *ex parte* reexamination. That reexamination resulted in the addition of a new independent claim (claim 11) that added a narrowing additional limitation not present in the original claim it replaced (claim 1), which was found unpatentable and cancelled. As shown below, the district court correctly determined that the new limitation added by TPL substantively changed the scope of the claims.

[20] Moreover, if TPL sincerely believed that it needed further discovery to oppose HTC's motion, as it suggests for the first time on appeal, it could have asked the district court to postpone HTC's motion as authorized under Federal Rule of Civil Procedure 56(d) to allow TPL to conduct such discovery. *See* Fed. R. Civ. P. 56(d) (authorizing district court to "allow time to obtain affidavits or declarations or to take discovery" to oppose summary judgment). Because TPL failed to make any such a request to the district court, it cannot be heard to complain on appeal that it was deprived of discovery needed to oppose HTC's motion.

Under the doctrine of absolute intervening rights in 35 U.S.C. § 307(b), "[u]nless a claim granted or confirmed upon reexamination is ***identical to an original claim***, the patent can not be enforced against infringing activity that occurred before issuance of the reexamination certificate." *Bloom Eng'g Co. v. N. Am. Mfg. Co.*, 129 F.3d 1247, 1250 (Fed. Cir. 1997) (emphasis added). "'Identical' does not mean verbatim, but means at most without substantive change." *Id.* Because all asserted claims of the '890 patent underwent "substantive change" during reexamination, the district court's decision was correct and should be affirmed.

The '890 patent issued on June 25, 1996 with ten originally-issued claims, with claim 1 being the sole independent claim. (A0316-17.) In January 2009, an *ex parte* reexamination request was filed against the '890 patent, which was initiated by the Patent Office in April 2009. (A0328.012-.025 (Order Granting/Denying Request for *Ex Parte* Examination) at A0328.014.) More than two years later, on March 1, 2011, the Patent Office issued an *ex parte* reexamination certificate canceling claims 1-4 and adding new claims 11-20. (A0318; A0328.) After the reexamination certificate issued, TPL amended its infringement contentions in the district court to assert new claims 11, 12, 13, 17 and 19 against HTC and to add additional accused HTC products. (A0076.) Claim 11 was the sole independent claim asserted by TPL, and thus, the focus of the district court's analysis.

During the reexamination, TPL added claim 11 by copying the language from claim 1 but adding a new limitation to overcome the prior art. Claim 11 as issued from the reexamination reads (new limitation shown in bold underlining):

> 11. A microprocessor, which comprises a main central processing unit and a separate direct memory access central processing unit in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being bidirectionally connected to a loop counter, said loop counter being connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, **said stack pointer pointing into said first push down stack**, said internal data bus being connected to a memory controller, to a Y register of a return push down stack, an X register and a program counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said incrementer being connected to said internal data bus, said direct memory access central processing unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

(A0328 (emphasis added).) As shown above, TPL added the limitation, "**said stack pointer pointing to said first push down stack**," to claim 11.

The addition of this new limitation came in response to a Final Rejection in which the Examiner rejected original claim 1 (and other claims) based on a number

of prior art references. TPL responded by adding new claims 11-20 and making various arguments about its original claims. (A6036-55.)

The Examiner subsequently relied on this new additional language, "said stack pointer pointing to said push down stack," to draw clear distinctions between original claim 1 and new claim 11. He issued an Advisory Action on August 12, 2010 (A6057-71) maintaining the rejection of claim 1 but indicating that claim 11 would be confirmed. (*See* A6067-68.) He observed that unlike newly-added claim 11, "the current language of claim 1 does not require that a stack pointer **points to the push-down stack.** ... Thus, there is no function claimed for the 'stack pointer', only that a stack pointer is bidirectionally connected to an internal bus." (A6065 (bold in original).)

The Examiner subsequently conducted a telephone interview with TPL's representative in which TPL authorized an examiner's amendment cancelling claim 1. (*See* A6073-83 (Notice of Intent To Issue Reexamination Certificate, at A6076).) In that same amendment, the Examiner found claim 11 patentable over the prior art, stressing the importance of the newly-added claim limitation:

> The closest prior art of record, being the May '948 reference does teach of using a push down stack. However, the May '948 reference does not expressly describe a stack pointer that points "into said first push down stack". With this feature, which was added in the Patent Owner's amendment dated 6/29/2010, claim 11 is deemed patentable.

(A6082.) This reexamination record leaves no doubt that the limitation added during the reexamination, "said stack pointer pointing to said push down stack," substantively changed the scope of the claims. The Reexamination Certificate for the '890 patent issued on March 1, 2011, and as such, TPL cannot recover for any alleged infringement prior to that date.

In determining whether there has been a substantive change during reexamination, a court analyzes "the claims of the original and the reexamined patents in light of the particular facts, including the prior art, the prosecution history, other claims, and any other pertinent information." *Laitram Corp.*, 163 F.3d at 1347. The court in *Laitram* observed that although there is no *per se* rule defining when an amendment is substantive, "it is difficult to conceive of many situations in which the scope of a rejected claim that became allowable when amended is not substantively changed by the amendment." *Id*. at 1348 (emphasis added). It is even more difficult to conceive of such a situation here considering that the newly-added claim language was the ***sole*** basis for allowance of the amended claims in reexamination.

TPL nonetheless now tries to argue that the additional limitation in claim 11 was meaningless and did nothing more than capture requirements that were inherent, implicit, or obvious in the originally-issued claim 1. TPL's arguments are based largely on extrinsic evidence in the form of expert testimony

from Dr. Oklobdzija (TPL Op. Br. at 20-22 (citing A6546-47 at ¶¶ 56-58)), not the intrinsic record of the '890 reexamination. This Court's precedents make clear that this extrinsic evidence is entitled to little or no weight in the claim construction question presented here. *See, e.g., Bell & Howell Document Mgmt. Prods. Co. v. Altek Sys.*, 132 F.3d 701, 706 (Fed. Cir. 1997).

A straightforward evaluation of the claims before and after the reexamination confirms that TPL's amendments narrowed the claims. Original claim 1 recited a "stack pointer" within the larger phrase: "said internal data bus being bidirectionally connected to a stack pointer." (A0316.) This "stack pointer" was not referenced anywhere else in the claim. Claim 1 did not, for example, require the "stack pointer" to point to any particular stack or be used in any specific way – or at all. The claim merely required the presence of "a stack pointer" and imposed one requirement on it – that it be "bidirectionally connected" to "said internal data bus." New claim 11, on the other hand, narrowed the claim by imposing a further requirement of "said stack pointer pointing to said first push down stack," which was plainly not required by the language of original claim 1.

TPL argues that this new limitation merely clarified an already-present requirement because, according to TPL, "stack pointer" of original claim 1 necessarily had to point to the "first push down stack." TPL reasons that the only

other stack recited in the claim is a separately-recited "return stack," which has its own "return stack pointer." The gist of TPL's argument, therefore, is that the "stack pointer" could not have pointed anywhere but the "first push down stack."

The flaw in TPL's argument is that nothing in the claim restricted the claimed microprocessor to only the recited "first push down stack" and the "return stack." Original claim 1 used a "comprising" transitional phrase and therefore did not exclude a microprocessor having additional push down stacks beyond those recited in the claim. *See, e.g., CollegeNet, Inc. v. ApplyYourself, Inc*., 418 F.3d 1225, 1235 (Fed. Cir. 2005) (holding that transitional phrase "comprising" is "inclusive or open-ended and does not exclude additional, unrecited elements or method steps.") (citation omitted). Original claim 1 could therefore have covered a microprocessor having two, three, or even ten push down stacks. The original claim would have been satisfied with a "stack pointer" that pointed to any one of those stacks.

The '890 specification confirms that a microprocessor in accordance with the alleged invention could in fact include multiple push down stacks, including at least a "first push down stack" and a separate "second push down stack." (A0302 at 3:4-15 (describing "first push down stack" (at 3:5-6) and "second push down stack" (at 3:13-14)).) TPL concedes that the specification discloses this "second push down stack," but attempts to diminish it by arguing that "[w]hile the

specification discusses a second push down stack, a second push down stack is not an element of any of the original or reexamined claims." (TPL Op. Br. at 22.) But this does not matter because, as explained above, original claim 1 was a "comprising" claim that did not exclude the second stack.

Because the "stack pointer" element of original claim 1 was silent as to where it pointed, it would have been satisfied by pointing into the recited "first push down stack" ***or*** one or more other push down stacks employed in an accused system. But TPL's amendment excluded such a system by expressly requiring that the recited "stack pointer" point to only "the first push down stack." This amendment substantively narrowed the scope of the claim by causing it to no longer cover a microprocessor that would have been covered by the claim prior to reexamination. *See Laitram*, 163 F.3d at 1346. The district court was therefore correct in finding absolute intervening rights.

As explained in section **II.C** of the **Statement of Facts** above, TPL stipulated to judgment on the '890 patent because the district court's intervening rights ruling precluded liability for all HTC products accused of infringing the '890 patent. (A7223.001-05, A7199-200.) If this Court affirms the district court's ruling on intervening rights, therefore, it disposes all claims under the '890 patent and renders it unnecessary to consider TPL's arguments concerning the claim construction of "separate direct memory access central processing unit." (A1048.)

D. The District Court Correctly Construed "Direct Memory Access Central Processing Unit" (DMA CPU) in the '890 patent.

The '890 patent purports to describe aspects of the specialized microprocessor architecture intended to allow faster access to certain memory locations. Claim 11, the only independent claim of the '890 patent following the reexamination,[21] recites "[a] microprocessor, which comprises a main central processing unit and **a separate direct memory access central processing unit** in a single integrated circuit …." (A0328, Claim 11 (emphasis added).) TPL's brief uses the shorthand phrase, "separate DMA CPU" to identify this term.

The term "direct memory access" or "DMA" is a well-known memory accessing method in the prior art for improving the efficiency of computer systems.[22] DMA allows certain subsystems or components within a computer (such as a disk drive or other device) to transfer data to memory without the main CPU having to perform the actual data transfer, allowing the CPU to perform other tasks.

TPL's appeal focuses on the distinction between two different types of DMA devices – the prior art "**DMA controller**" and the allegedly inventive "**DMA**

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[21] As discussed, claim 1 was canceled in the reexamination, and new claim 11 was added with the additional, narrowing limitation.

[22] *See*, *e.g.*, A1433-42 (A1440 at ¶ 44 ("DMA is well known in the art. … It would have been obvious to a person of ordinary skill in the art to incorporate a DMA … because that would render [the] system more efficient.”))

CPU" described and claimed in the '890 patent. The specification acknowledges that conventional "DMA controllers can provide routine handling of DMA requests and responses, but some processing by the main central processing unit (CPU) of the microprocessor is required." (A0301 at 1:55-58.) The specification identifies as an object of the invention a processor "in which DMA does not require use of the main CPU during DMA requests and responses and which provides very rapid DMA response with predictable response times." (A0301 at 2:2-5.) The '890 patent purports to address these perceived issues through a "separate direct memory access **central processing unit**" ("separate DMA CPU"). As explained in the specification: "The DMA CPU **72** controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU **70** (FIG. **2**) for time specific processing." (A0304 at 8:22-24.) The district court thus construed "separate DMA CPU" as:

> a central processing unit that accesses memory and that fetches and executes instructions directly and separately of the main central processing unit.

(A0063.)

The district court's construction comports with the specification and claim language of the '890 patent. The claim language itself recites "a **separate** direct memory access central processing unit" that is "separate" in the sense that it is distinct from the main CPU recited in the claim. As shown below, the construction

also properly reflects the fact that a "DMA CPU" is a "CPU" and, therefore, capable of fetching and executing instructions.

1. The District Court's Construction Properly Excludes the "DMA Controller" of the Prior Art.

TPL contends that the district court's construction of "DMA CPU" was erroneous because it excludes the "DMA controllers" discussed as prior art in the '890 patent. But the exclusion of DMA controllers from the claims was a direct result of the plain language the applicants chose when they drafted the claims. As explained above, the specification draws a clear distinction between the "DMA CPU" of the alleged invention and the "DMA controller" of the prior art. But the claim language itself recites only the "separate DMA CPU," not a DMA controller. Had the applicants intended to cover the distinct and separately-disclosed DMA controller, they could have recited a DMA controller in the claim.

The district court's construction also properly incorporates the component word "CPU" within the "DMA CPU" claim term. The district court correctly recognized that "a person of ordinary skill in the art would understand 'CPU' to mean a unit of a computing system that fetches, decodes, and executes programmed instructions," and that "the inventors use the term CPU consistently with its plain and ordinary meaning." (A0035 at 12:5-9; *see also* A0062-63.) TPL conceded that the ability to fetch and execute instructions defined the differences between the claimed DMA CPU and prior art DMA controllers when it told the

district court: "This 'more traditional DMA controller' is one that functions more as a **traditional** state machine, **without the ability to fetch its own instructions that characterizes a CPU**." (A0755 at 9:24-26 (emphasis added).) In other words, the claimed DMA CPU, unlike a conventional DMA controller, has the ability to fetch and execute instructions. The district court's construction properly reflects and incorporates this distinction.

TPL relies on two embodiments in the specification to suggest that the patent describes a DMA CPU and DMA controller interchangeably (*e.g.*, TPL Op. Br. at 6-7, 25-27), but TPL is wrong.[23] Figure 9 of the '890 patent shows "a layout diagram of a second embodiment of a microprocessor" that has a "DMA CPU 314." (A0302 at 4:61-63; A0290 at Fig. 9.) A separate passage appearing eight columns later in the specification describes a different and unclaimed embodiment in which "the DMA processor **72** of the microprocessor **50** has been replaced with a more traditional DMA controller **314**." (A0306 at 12:62-65.) That later passage

[23] "While … a patentee can act as his own lexicographer to specifically define terms of a claim contrary to their ordinary meaning, *the written description in such a case must clearly redefine a claim term* …. *Absent an express intent to impart a novel meaning, claim terms take on their ordinary meaning*." *Elekta Instrument S.A. v. O.U.R. Sci. Int'l*, 214 F.3d 1302, 1307 (Fed. Cir. 2000) (internal quotation and citation omitted) (emphasis added). As the district court has twice found, the specification of the '890 patent does not support a different meaning for "CPU" in the "DMA CPU" phrase. *See* A0035 ("In the written description, the inventors use the term CPU consistently with its plain and ordinary meaning."); *see also* A0062 ("Thus where the patent claims a DMA CPU, it means a DMA CPU and not a DMA controller.").

makes no reference to Figure 9 or the DMA CPU described earlier in the specification, and in fact, actually supports the district court's construction. By disclosing an alternative system in which a DMA CPU has been "**replaced** with a more traditional DMA controller 314" (*id.* (emphasis added)), the specification actually provides further support for a DMA CPU being **different** from a DMA controller.

TPL's assertion that HTC's construction would exclude a preferred embodiment is similarly without merit. The Federal Circuit has repeatedly recognized that a specification can disclose subject matter not covered by the claims. *See TIP Sys., LLC v. Phillips & Brooks/Gladwin, Inc*., 529 F.3d 1364, 1373 (Fed. Cir. 2008) ("Our precedent is replete with examples of subject matter that is included in the specification, but is not claimed."). "Therefore, the mere fact that there is an alternative embodiment disclosed in the [patent-in-suit] that is not encompassed by [a proposed] claim construction does not outweigh the language of the claim, especially when [that] construction is supported by the intrinsic evidence." *Id.* Because the specification describes the separate DMA CPU as an improvement and replacement over the conventional DMA controller, it makes sense that the claims exclude the DMA controller. TPL's construction improperly seeks to lay claim over the DMA controller that the specification distinguishes from the claimed separate DMA CPU.

2. The District Court Properly Rejected TPL's Argument Based on the Restriction Requirement.

The Patent Office issued a restriction requirement (A2171-74) on August 31, 1992 in the parent application of the '890 patent that later issued as U.S. Patent No. 5,440,749 (the "'749 patent"), another patent-in-suit that had been dismissed before trial. The Patent Office divided the proposed claims into 10 groups (Group I through Group X). TPL argues that the restriction requirement supports its position that "DMA CPU" should be interpreted as including a DMA controller. As shown below, the restriction requirement is entitled to no weight.

Courts have repeatedly given restriction requirements little to no weight in claim construction when, as here, they are unaccompanied by a substantive discussion of the meaning of the disputed claim language. *See, e.g., Honeywell Int'l, Inc. v. ITT Indus., Inc.*, 452 F.3d 1312, 1319 (Fed. Cir. 2006) (assigning little weight to restriction requirement where examiner did not construe the disputed claim term); *Amersham Pharmacia Biotech, Inc. v. Perkin-Elmer Corp.*, No. C 97-CV-4203 CRB, 2000 WL 34204509, at *15 (N.D. Cal. Feb. 28, 2000) ("A restriction requirement is not a rejection and it cannot be used to controvert the plain language of the claim.").

Nothing in the restriction requirement cited by TPL undermines or even addresses the district court's reasoning. The Patent Office's restriction requirement did not make any reference to the "separate DMA CPU" phrase

recited in the '890 patent. TPL cannot identify a single statement by either the Examiner or the applicants regarding the restriction requirement that even references the separate DMA CPU, let alone sheds light on its proper claim construction.

TPL's argument relies on a simple yet irremediably flawed premise—that because Group III recited a DMA "processing unit" that fetches and executes instructions, that subject matter cannot be within the scope of the claims in Group VIII or any of the other Groups. TPL cites no authority to support this theory. A restriction requirement merely indicates that "two or more independent and distinct inventions are claimed in one application." 35 U.S.C. § 121 (2012). Because the scope of an invention is determined by its claims, with all of their limitations, two inventions can recite common limitations yet still qualify as "independent and distinct inventions" and therefore justify the issuance of a restriction requirement.[24]

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[24] Indeed, there are multiple instances of overlapping claim limitations in several of the groups established by the restriction requirement. (A2171-74; A2140-59.) For example, the claims in Group VIII that issued as the '890 patent recited a CPU that comprised, among other things, an "arithmetic logic unit" and a "first push down stack." (A2173 at ¶ 22 (defining Group VIII as including claim 48); A2153-54 at claim 48.) But the claims in Group VI, directed to "a CPU having stacks and pointers," recite the same limitations (A2172 at ¶ 20 (defining Group VI as including claim 22); A2163-64 at claim 22 (reciting a CPU with an "arithmetic logic unit" and a "push down stack")), and so do the claims in Group II (A2172 at ¶ 16 (defining Group II as including claim 6); A2161 at claim 6 (reciting an "arithmetic logic unit" and a "first push down stack").) As another example, the claims in Group VIII recited an internal data bus "bidirectionally connected to a loop counter" that is connected to a "decrementer." (A2173 at ¶ 22 (defining

The fact that Group III recited a DMA "processing unit" that fetches and executes instructions, therefore, does not prevent this subject matter from being covered by the longer and more detailed claims of Group VIII that issued as the '890 patent. The district court properly concluded that the restriction requirement has no bearing on the meaning of the "separate DMA CPU."

3. The '890 Reexamination Provides No Basis for Ignoring the "CPU" in the Term "Separate DMA CPU."

TPL also attempts to rely on an *ex parte* reexamination request (A2176-217) filed by the anonymous third party who challenged the '890 patent.[25] TPL claims that the reexamination requester mapped the separate DMA CPU recited in the '890 patent against a conventional DMA controller. (A2186-89.) TPL cites no case law, however, suggesting that statements of an anonymous third-party reexamination requester – which were not adopted by either the patent owner or the Examiner – should carry any weight in claim construction.

TPL does not identify any of its own statements in the reexamination that supposedly support its position on the meaning of "separate DMA CPU." TPL merely asserts that "[a]t no time did the patent owner ever try to distinguish the

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Group VIII as including claim 48); A2153-54 at claim 48 (emphasis added).) Group II, however, contains claims that recite this same requirement. (A2172 at ¶ 16 (defining Group II as including claim 10); A2162 at claim 10 (reciting "a loop counter connected to receive a decrement control signal . . .").)

[25] HTC was not involved in that reexamination.

prior art" on the basis of the separate DMA CPU. (TPL Op. Br. at 38.) But inaction by the patent owner falls far short of specific statements regarding the scope of its claims. Moreover, as explained above, TPL's decision to avoid distinguishing prior art that disclosed DMA controllers was presumably motivated by its desire to not undermine its infringement theory, which depends on mapping the separate DMA CPU to DMA controllers. TPL's litigation-inspired decision to say nothing about the separate DMA CPU during reexamination provides no evidence relevant to claim construction.

CONCLUSION AND STATEMENT OF RELIEF SOUGHT

This Court should reverse the judgment with respect to the '336 patent in the district court's Amended Judgment (A0148-49) and direct the district court to enter judgment in favor of HTC with respect to the '336 patent.

This Court should affirm the judgment with respect to the '890 patent in the Amended Judgment. *Id.*

Dated: June 27, 2014

Respectfully submitted,

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ADDENDUM

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United States District Court
For the Northern District of California

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, et al., Defendants.	Case No.: 5:08-cv-00882-PSG **ORDER RE: HTC'S MOTIONS FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT AND NO WILLFULNESS** **(Re: Docket Nos. 457, 458)**

Before the court in this patent case are two motions for summary judgment brought by Plaintiffs HTC Corporation and HTC America, (collectively "HTC"). HTC first moves for "full" summary judgment of non-infringement and no willful infringement of U.S. Patent No. 5,809,336 ("the '336 patent"). HTC separately moves for partial summary judgment of non-infringement of the '336 patent and U.S. Patent No. 5,530,890 ("the '890 patent") and no willful infringement of the '890 patent. On August 13, 2013, the parties appeared for a hearing. Having considered the papers and arguments of counsel:

The court DENIES HTC's motion for summary judgment of "full" non-infringement of the '336 patent.

The court DENIES HTC's motion for partial summary judgment of non-infringement of the '336 patent.

The court DENIES HTC's motion for summary judgment of no willful infringement of the '336 patent.

The court GRANTS HTC's motion for partial summary judgment of non-infringement of the '890 patent.

The court GRANTS-IN-PART HTC's motion for partial summary judgment of no willful infringement of the '890 patent.

The court sets forth its reasoning below.

I. BACKGROUND

HTC Corporation is a Taiwan corporation with its principal place of business in Taoyuan, Taiwan, R.O.C. HTC's subsidiary, HTC America, is a Texas corporation with its principal place of business in Bellevue, Washington. Defendants Technology Properties Limited and Alliacense, Limited ("Alliacense") are California corporations with their principal place of business in Cupertino, California; Patriot Scientific Corporation ("Patriot") is a Delaware corporation with its principal place of business in Carlsbad, California. These defendants – Technology Properties Limited, Alliacense, and Patriot (collectively "TPL") – claim ownership of a family of related microprocessor patents. TPL refers to those patents as the Moore Microprocessor Portfolio patents ("MMP patents"), in recognition of co-inventor Charles Moore's contributions. HTC filed this suit on February 8, 2008, seeking a judicial declaration that four of the MMP patents – U.S. Patent Nos. 5,809,336 ("the '336 patent"), 5,784,584 ("the '584 patent"), 5,440,749 ("the '749 patent"), and 6,598,148 ("the '148 patent") – are invalid and/or not infringed.[1] TPL counterclaimed for

[1] *See* Docket No. 1.

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infringement of the '336, '749, '148, and '890 patents on November 21, 2008.[2] On April 25, 2008, TPL filed two complaints in the Eastern District of Texas against HTC alleging infringement of the four patents at issue in the pending declaratory judgment action.[3] On June 4, 2008, TPL filed additional patent infringement actions against HTC in the Eastern District of Texas asserting U.S. Patent No. 5,530,890 ("the '890 patent").[4] On July 10, 2008, HTC amended its complaint before this court, adding claims for declaratory relief with respect to the '890 patent.[5] On February 23, 2009 the parallel Texas litigation was dismissed without prejudice following Judge Fogel's decision to deny TPL's Motion to Dismiss, or in the Alternative, to Transfer Venue in the California action.[6] On March 25, 2010, the court accepted the parties' stipulation to dismiss the '584 patent from this litigation.[7] On August 24, 2012, Technology Properties Limited, Patriot, and Phoenix Digital Solutions initiated an International Trade Commission ("ITC") investigation regarding HTC's alleged infringement of the '336 patent.[8] On July 17, 2013, the court accepted the parties' stipulation to dismiss the '148 and '749 patents from this litigation.[9]

The bottom line is that only the '336 and '890 patents remain at issue for the purposes of this litigation.

A. The '336 Patent

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[2] *See* Docket No. 60 at 6-8.

[3] *See* Docket No. 16 at 3.

[4] *See* Docket No. 35 at 5.

[5] *See* Docket No. 34.

[6] See Docket Nos. 49 (denying motion to dismiss, to transfer venue, and to stay) and 88 (granting motion for leave to file motion for reconsideration and denying motion for reconsideration).

[7] *See* Docket No. 152.

[8] *See* Docket No. 561-1. Claims 1, 6, 7, 9-11, and 13-16 were asserted in the investigation. On September 6, 2013, Administrative Law Judge James Gildea issued an Initial Determination from in the ITC proceeding holding that HTC did not violate Section 337 of the Tariff Act of 1930. *See id.*

[9] *See* Docket No. 462.

The '336 patent issued on September 15, 1998 and describes a microprocessor with an internal variable speed clock, or oscillator, that drives the processor's central processing unit ("CPU"). Traditional microprocessors use external, fixed speed crystals to clock the CPU. A CPU's maximum possible processing capacity depends on process, voltage, and temperature ("PVT parameters"). An external clock must therefore set the timing of the CPU to suboptimal PVT conditions, resulting in waste of the CPU's processing speed under optimal conditions. The internal, variable clock described in the '336 patent claims real-time adjustment of the timing of the CPU by placing the clock on the chip itself. Thus, the CPU can perform optimally under any set of parameters. The microprocessor nevertheless requires a second external clock because devices other than the CPU do not operate at variable speed.

TPL claims that HTC's accused products infringe the '336 patent by their internal, variable speed oscillator on their microprocessors. At issue are claims 1, 6, 10, 11, 13, and 16.[10]

Claim 1 provides:

> A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.

Claim 6 provides:

> A microprocessor system comprising:

[10] Docket No. 494 at 7.

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices; an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.

Claim 10 provides:

In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency; providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors; clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate; connecting an [on chip] on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.

Claim 11 provides:

A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator

variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperatureof said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein said central processing unit operates asynchronously to said input/output interface.

Claim 13 provides:

A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices; an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and further wherein said central processing unit operates asynchronously to said input/output interface.

Claim 16 provides:

In a microprocessor system including a central processing unit, a method for locking said central processing unit comprising the steps of providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency; providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors; clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate; connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus,

> and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock, wherein said central processing unit operates asynchronously to said input/output interface.

B. The '890 Patent

The '890 patent first issued on June 25, 1996 and originally included ten claims, nine of which depended from the sole independent claim, claim 1.[11] On January 19, 2009, the '890 patent was subjected to ex parte reexamination.[12] An amended version of the patent emerged on March 1, 2011.[13] The reexamination proceeding resulted in the cancellation of claims 1-4, confirmation of the patentability of claims 5-10, and addition of claims 11-20. At issue in this suit are claims 11, 12, 13, 17, and 19.[14]

Claim 11, the amended independent claim on which all of the other claims depend, describes:

> A microprocessor, which comprises a main central processing unit and a separate direct memory access central processing unit in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being bidirectionally connected to a loop counter, said loop counter being connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said stack pointer pointing into said first push down stack, said internal data bus being connected to a memory controller, to a Y register of a return push down stack, an X register and a program counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said incrementer being connected to said internal data bus, said direct memory access central processing

[11] *See* Docket No. 458 at 2.

[12] *See id.*

[13] *See id.*

[14] *See id.*

> unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

During reexamination, the patentee added the phrase "said stack pointer pointing into said first push down stack," which did not appear in claim 1.

II. SUMMARY JUDGMENT STANDARDS

Summary judgment is appropriate only if there is "no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law."[15] The moving party bears the initial burden of production by identifying those portions of the pleadings, discovery, and affidavits which demonstrate the absence of a triable issue of material fact.[16] The standard for summary judgment differs depending on whether the moving party bears the burden of persuasion at trial.[17] If the moving party bears the burden of persuasion at trial, that party must present "credible evidence" showing that he is entitled to a directed verdict.[18] The burden of production then shifts to the non-moving party to produce evidence raising a genuine issue of material fact.[19] On the other hand, if the moving party does not bear the burden of persuasion at trial, he can prevail on a motion for summary judgment in two ways: by proffering "affirmative evidence negating an element of the non-moving party's claim," or by showing the non-moving party has insufficient evidence to establish an "essential element of the non-moving party's claim."[20] If met by the moving party, the burden of production then shifts to the non-moving party, who must then provide

[15] Fed. R. Civ. P. 56(a).

[16] *See* Fed. R. Civ. P. 56(c)(1); *Celotex Corp. v. Catrett*, 477 U.S. 317, 323 (1986).

[17] *See Celotex Corp.*, 477 U.S. at 331.

[18] *Id.*

[19] *See id.*

[20] *Id.*

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specific facts showing a genuine issue of material fact for trial.[21] In both instances, the ultimate burden of persuasion remains on the moving party.[22] In reviewing the record, the court must construe the evidence and the inferences to be drawn from the underlying evidence in the light most favorable to the non-moving party.[23]

III. DISCUSSION

A. HTC's Motion for Summary Judgment of Non-Infringement and No Willful Infringement of the '336 Patent

1. Non-Infringement of the '336 Patent

The court first considers HTC's motion for summary judgment of "full" non-infringement of the '336 patent. HTC argues that summary judgment is warranted because when the independent claims of the '336 patent are properly construed, HTC's products do not perform the claimed invention. HTC specifically points to three terms that each appear in two claims: (1) "entire ring oscillator variable speed system clock" (claims 1 and 11), (2) "entire oscillator" (claims 6 and 13), and (3) "an entire variable speed system clock" (claims 10 and 16).

HTC argues as follows. The prosecution history of the '336 patent demonstrates the applicants' repeated and express disclaimer that the claimed timing element – the oscillator or variable speed clock – had any connection to or dependence on a reference signal from an external crystal or other fixed timing piece. To further distinguish the '336 patent, the applicants added the "entire" term to explicitly claim only a timing element that wholly and exclusively appeared with the CPU on the chip. HTC's processors, in contrast, rely on an external crystal timing piece (called

[21] *See id.* at 330; *T.W. Elec. Service, Inc. v. Pac. Elec. Contractors Ass'n*, 809 F.2d 630, 630 (9th Cir. 1987).

[22] *See id.*

[23] *See Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248 (1986); *Matsushita Elec. Indus. Co. v. Zenith Radio Corp.*, 475 U.S. 574, 587 (1986).

a phase-locked loop or "PLL"). Unlike the invention, therefore, the timing elements of HTC's processors do not sit entirely on the chip and do not vary with PVT parameters.

TPL responds that HTC improperly seeks reconsideration of this court's previous claim construction. The court properly construed the "entire variable speed system clock" term and this construction should extend to the other three "entire" terms. HTC's additional limitations are not supported by the specification, which does not speak to whether the oscillator or variable speed system clock also could work with an external crystal. As for any disclaimer, the applicants never disclaimed all reliance or reference to an off-chip crystal. Instead, the disclaimer to avoid the Magar reference was to an off-chip oscillator that generated the on-chip clock. As to the Sheets reference, the applicants distinguished their clock reference by pointing out that it was not an on-chip oscillator but rather an off-chip clock, and that off-chip clock required a command input to change its frequency. The oscillator taught by the '336 patent, in contrast, is self-generating on the chip itself and does not require an outside command to change frequency. As to the variation argument, even by HTC's own admission, the on-chip HTC oscillators vary and the PLLs in fact serve to limit that variation. That the net result may be a minimal change in the frequency of the clock is not enough to take HTC's accused products beyond the claim language.

HTC replies that the on-chip oscillator does not "generate" the CPU clock unless it communicates with the PLL, making the PLL necessary to "generate" the clock – and thereby outside of the claim language (as construed in light of the disclaimers). HTC further replies that frequency control in fact is generation of the clock because the oscillator does not begin to run independently. The PLL controls the oscillator and sets the frequency, which generates the clock. As to the variation issue, HTC argues that a person of ordinary skill in the art would understand the de minimis variation experienced by its products as rendering the timing element essentially fixed.

The court agrees with HTC that the disputed limitations are properly understood to exclude any external clock used to generate a signal.[24] Nevertheless, there remains a factual dispute whether HTC's products contain an on-chip ring oscillator that is self-generating and does not rely on an input control to determine its frequency. While HTC's expert says that the PLLs generate the clock, TPL's expert counters that the ring oscillators generate the clock and the PLLs merely buffer or fix the frequency.[25] This is a classic factual question that requires a trial to answer.

2. Willful Infringement of the '336 Patent

To "establish willful infringement, a patentee must show by clear and convincing evidence that the infringer acted despite an objectively high likelihood that its actions constituted infringement of a valid patent."[26] A patentee therefore must establish two elements. First, the patentee must show the accused infringer acted with "objective recklessness." Objective recklessness remains a question of law "predicated on underlying mixed questions of law and fact."[27] The objective recklessness prong "entails an objective assessment of potential defenses based on the risk presented" by the patent which "may include questions of infringement but also can be expected in almost every case to entail questions of validity that are not necessarily

[24] The patentee's arguments traversing the prior art narrowed the claims. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 740 (2002) ("A patentee's decision to narrow his claims through amendment may be presumed to be a general disclaimer of the territory between the original claim and the amended claim."); *cf. Saeilo Inc. v. Colt's Mfg. Co.*, 26 F. App'x 966, 973 (Fed. Cir. 2002) ("Where an amendment narrows the scope of a claim for a reason related to the statutory requirements for patentability, prosecution history estoppel acts as a complete bar to the application of the doctrine of equivalents to the amended claim element.").

[25] *Compare* Docket No. 457 at 16 ("the oscillators in the accused products indisputably rely on an external crystal or clock generator to clock" the CPU), *with* Docket No. 470 at 14 ("Each HTC product includes a CPU/system clock – a ***ring oscillator*** within a PLL – that ***generates*** a clock signal ***on its own***, as long as it has a power supply.") (emphasis in original).

[26] *In re Seagate Tech., LLC*, 497 F.3d 1360, 1371 (Fed. Cir. 2007) (*en banc*).

[27] *See Bard Peripheral Vascular, Inc. v. W.L. Gore & Assocs., Inc.*, 682 F.3d 1003, 1006-07 (Fed. Cir. 2012) (holding that the objective determination of recklessness, even though predicated on underlying mixed questions of law and fact, is decided by the judge as a question of law subject to de novo review).

dependent on the factual circumstances of the particular party accused of infringement."[28] Second, if the requisite threshold objective recklessness is established, then the patentee must show that the "objectively-defined risk" of infringement determined by the record developed in the infringement proceeding "was either known or so obvious that it should have been known to the accused infringer."[29]

HTC argues that TPL has not presented sufficient evidence to make a prima facie case of willful infringement, in view of its "clear, legitimate, and objectively reasonable defenses" to HTC's claims of infringement.[30] In particular, its proposed constructions have been adopted by other tribunals and the ITC in particular. HTC's non-infringement position at the ITC was "sufficiently compelling and reasonable" that both the ITC staff attorney and Judge Gildea himself agreed with HTC's position.[31]

TPL takes issue with HTC's reference in this case to the ITC litigation. Different theories of infringement and different products are implicated by the two cases. Different claim constructions have issued in the cases. The staff attorney's position and Judge Gildea's conclusions are therefore irrelevant. Separately, TPL's successful licensing of the MMP patent portfolio suggests that HTC could not reasonably or realistically expect its invalidity or

[28] *Id.* at 1006.

[29] *Seagate*, 497 F.3d at 1371.

[30] Looking to Fed. R. Civ. P. 37(c)(1) HTC further points out that TPL failed to substantively respond to its interrogatory about willful infringement. *See* Fed. R. Civ. P. 37(c)(1) ("If a party fails to provide information or identify a witness as required by Rule 26(a) or (e), the party is not allowed to use that information or witness to supply evidence on a motion, at a hearing, or at a trial, unless the failure was substantially justified or is harmless."). But TPL's response raising a host of objections appears substantially justified, even if it is not ultimately persuasive, and in any event HTC does not appear to have taken any steps whatsoever in the intervening four years to compel a more complete response.

[31] Judge Gildea's Initial Determination ("ID") did not issue until September 6, 2013, after the papers for this motion were filed.

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non-infringement defenses to succeed in this litigation. Finally, direct pre-suit communication between HTC and TPL establishes that HTC had notice of its allegedly infringing activities.

District courts appear split as to whether current evidence that a party's actions were objectively reasonable is relevant to a willfulness analysis under *Seagate*. In *i4i Ltd. P'ship v. Microsoft Corp.*, Judge Davis held that the correct willfulness analysis "focuses on whether, given the facts and circumstances prior to [the accused infringer's] infringing actions, a reasonable person would have appreciated a high likelihood that acting would infringe a valid patent."[32] The "number of creative defenses that Microsoft is able to muster in an infringement action after years of litigation and substantial discovery is irrelevant to the objective prong of the *Seagate* analysis."[33] Judge Davis then explained that the court should more properly focus on whether defenses would have been objectively reasonable and apparent before Microsoft infringed and was sued.[34] In *Uniloc USA, Inc. v. Microsoft Corp.*, Judge Smith was "not convinced that such a 'before and after' line is so easily drawn, or for that matter appropriate, to measure the objective likelihood (or lack thereof) that a party acted to infringe a valid patent."[35] Judge Smith emphasized that "the inquiry is case-specific" and should focus on an objective view of the record.[36]

The court agrees with HTC that favorable court rulings can support the objective reasonableness of its non-infringement positions. The court cannot help but take note of the analogous issue of the "book of wisdom" when addressing patent damages. The Supreme Court has affirmed that after-arising "[e]xperience . . . is a book of wisdom that courts may not

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[32] 670 F. Supp. 2d 568, 582 (E.D. Tex. 2009).

[33] *Id.*

[34] *See id.*

[35] 640 F. Supp. 2d 150, 177 n. 33 (D.R.I. 2009).

[36] *Id.*

neglect."[37] Nonetheless, "as the party moving for summary judgment" HTC "must do more than persuade [the court] that its defenses were reasonable."[38] Instead, HTC "must establish that 'there is no genuine dispute as to any material fact' and that [the accused infringer] 'is entitled to judgment as a matter of law'—in other words, that *no reasonable fact-finder* could find willful infringement."[39]

Viewing the evidence in the light most favorable to TPL, the court concludes that a reasonable fact finder could plausibly find facts sufficient to support a conclusion of willful infringement. TPL's burden to show willful infringement by clear and convincing evidence is a steep one. But where factfinding is necessary, trial courts generally reserve willfulness until after a full presentation of the evidence on the record to the jury.[40] The record supports a finding that HTC knew about the patents and TPL's claims of infringement before it began the activities that allegedly infringe and as explained above, here there remains an important issue regarding the role of the external crystal in HTC's products in generating a signal.[41] Under these circumstances summary judgment on the issue of willfulness is not warranted.

B. Partial Summary Judgment of Non-Infringement of the '336 Patent and the '890 Patent and No Willful Infringement of the '890 Patent

HTC next moves for partial summary judgment of non-infringement of the '336 patent and the '890 patent based on the doctrine of absolute intervening rights. By this same motion, HTC also seeks summary judgment of no willful infringement under the '890 patent.

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[37] *Sinclair Ref. Co. v. Jenkins Petroleum Process Co.*, 289 U.S. 689, 690 (1933).

[38] *Kimberly-Clark Worldwide, Inc. v. First Quality Baby Products, LLC*, Case No. 1:09-cv-1685, 2013 WL 1465403, at *2 (M.D. Pa. Apr. 11, 2013)

[39] *Id.* (citing Fed. R. Civ. P. 56(a)).

[40] *See, e.g. Bard*, 682 F.3d at 1008; *Fujitsu Ltd. v. Belkin Int'l, Inc.*, Case No. 10-cv-03972-LHK, 2012 WL 4497966, at *39 (N.D. Cal. Sept. 28, 2012).

[41] *See* Docket No. 470-1, Ex. A (Nov. 7, 2006 correspondence from Alliacense to HTC); Docket No. 470-1, Ex. B (Nov. 20, 2006 correspondence from Alliacense to HTC).

Under 35 U.S.C § 307(b), a patent owner may not recover for infringement of claims that are invalidated or amended through the reexamination process.[42] The "reexamination statute restricts a patentee's ability to enforce the patent's original claims to those claims that survive reexamination in 'identical' form."[43] "'Identical' does not mean verbatim, but means at most without substantive change."[44] The court must therefore determine whether the scope of the claims are the same, not just whether the same words are used.[45] Section 307 shields "those who deem an adversely held patent to be invalid; if the patentee later cures the infirmity by reissue or reexamination, the making of substantive changes in the claims is treated as an irrebuttable presumption that the original claims were materially flawed."[46] The "statute relieves those who may have infringed the original claims from liability during the period before the claims are validated."[47]

Whether "amendments made to overcome rejections based on prior art are substantive depends on the nature and scope of the amendments, with due consideration to the facts in any given case that justice will be done."[48] "An amendment that clarifies the text of the claim or makes it more definite without affecting its scope is generally viewed as identical."[49] To make its determination under the so-called doctrine of intervening rights, the court must consider "the scope of the original and reexamined claims in light of the specification, with attention to the references

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[42] *See Fresenius USA, Inc. v. Baxter Intern., Inc.*, 721 F.3d 1330, 1339 (Fed. Cir. 2013).

[43] *Id.* (listing cases).

[44] *Id.*

[45] *See id.*

[46] *Bloom Eng'g Co. v. N. Am. Mfg. Co.*, 129 F.3d 1247, 1249 (Fed. Cir. 1997).

[47] *Id.*

[48] *Id.*

[49] *Id.*

that occasioned the reexamination, as well as the prosecution history and any other relevant information."[50]

1. Non-Infringement of the '336 Patent

As noted earlier the '336 patent issued September 15, 1998, and included ten originally-issued claims.[51] A series of ex parte reexamination requests were filed against the '336 patent between October 2006 and January 2007.[52] When the reexamination proceedings completed, claims 1, 6, and 10 emerged with modified language, and new independent claims 11, 13, and 16 were added. TPL amended claim 1 to further describe the "second clock independent of said ring oscillator" to say that "wherein a clock signal of said clock originates from a source other than said ring oscillator variable speed system clock." Claim 6 was amended to describe the "off-chip external clock" to likewise derive its "clock signal" "from a source other than said oscillator." Claim 10 includes a similar amendment that adds that the "off-chip external clock" has a "clock signal" that "originates form a source other than said variable speed clock." Claims 6 and 10 also added "off-chip" references to the descriptions of the second clocks. Claims 11, 13, and 16 were based on independent claims 1, 6, and 10, but during reexamination TPL added an additional clause to the end of each claim: "wherein said central processing unit operates asynchronously to said input/output interface."

In HTC's view, it should not be held liable for infringement of the '336 patent claims 1, 6, 10, 11, 13, and 16 because those claims were either substantially narrowed or newly-added through reexamination. Any recovery for the '336 patent should be limited to the date of the issuance of the reexamination certificate on December 15, 2009, because the amendments were sufficiently substantive to preclude recovery from before the amendments.

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[50] *Id.*

[51] *See* Docket No. 458 at 5.

[52] *Id.*

TPL responds that these amendments serve as nothing more than clarification of the claim language and that the scope of the claims have not changed. Several excerpts from the prosecution history of the reexamination demonstrate that the patentee believed the amended claim language only clarified how the second clock was "independent"[53] and that the "external" components were in fact "off-chip"[54].

HTC replies that the original claims differ from the amended claims in scope because the original claims spoke only to the difference in frequency control – and that is what "independence" really references in these claim terms. Because a clock with signal origins from the ring oscillator but with an independent frequency could exist under the original claims but not under the amended claims, the claim is narrower and therefore substantively different. For claims 11, 13, and 16, the "independent" clock signals could have a "readily predictable phase relationship." Because of that possibility, the claims are narrower and thereby substantively different. Further, the court should not credit self-serving testimony from the prosecution history.[55]

On balance, the court finds that the amended claim language added during reexamination did not substantively amend the asserted '336 claims' scope. "Independent" in the disputed claims must be understood to be just that: without dependence of any kind. While HTC offers a more nuanced interpretation that focuses exclusively on frequency control, it cites no intrinsic – or for that matter extrinsic evidence – to support its position. Coupled with the references in the prosecution history indicating that the amendments really were for clarification purposes only, TPL's argument is more persuasive.

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[53] *See* Docket No. 471-5, Ex. E at 2; Docket No. 471-6, Ex. F at 11, 27; Docket No. 471-7, Ex. G at 8-12, 14.

[54] *See* Docket No. 471-7, Ex. G at 12, 16.

[55] *See Moleculon Research Crop. v. CBS, Inc.*, 793 F.2d 1261, 1270 (Fed. Cir. 1986) (holding that documents submitted by the patentee during prosecution may be considered for claim interpretation purposes, but "might very well contain merely self-serving statements which likely would be accorded no more weight than testimony of an interested witness or argument of counsel. Issues of evidentiary weight are resolved on the circumstances of each case.").

2. Motion for Partial Summary Judgment of Non-Infringement and No Willful Infringement of the '890 Patent

a. Non-Infringement of the '890 Patent

The court next considers HTC's motion for summary judgment of non-infringement of the '890 patent claims 11, 12, 13, 17, and 19. As noted above, claims 12, 13, 17, and 19 all depend on independent claim 11.

HTC again argues the doctrine of absolute intervening rights entitles it to summary judgment of non-infringement. During reexamination, TPL added claim language further defining a stack pointer as "pointing into said first push down stack," after the examiner identified no function for the stack pointer in the original claim language. The examiner noted that the amendment to claim 1 prevented the claim from being anticipated by the prior art under 35 U.S.C. § 102. This change to the '890 patent during reexamination was substantive and that the absolute intervening rights doctrine bars liability arising before the reexamination terminated.

TPL initially responds that HTC's assertion of the absolute intervening rights doctrine is untimely because it did not include the affirmative defense in its answer to TPL's complaint.[56] As to the merits, TPL says that the amendment only clarified the claim scope but did not substantively amend the claim, precluding the absolute intervening rights doctrine. Further, in *Norwood v. Vance* the Ninth Circuit noted that parties may raise affirmative defenses for the first time at summary judgment only if the opposing party is not prejudiced.[57] Allowing HTC to assert the defense – four years into this litigation – would subject it to unfair prejudice.

The court is not persuaded that TPL has established the prejudice necessary to bar HTC's assertion of the absolute intervening rights doctrine at this stage in the litigation. TPL does not, for

[56] The initial declaratory judgment complaint in this case was filed February 8, 2008. *See supra* note 1. The '890 patent did not reissue following reexamination until March 1, 2011. *See supra* note 13.

[57] 591 F.3d 1062, 1075 (9th Cir. 2010).

example, articulate the discovery it might have otherwise taken had HTC promptly moved to amend its answer in 2011.

Turning to the merits, HTC asserts estoppel and argues claim 11 emerged from reexamination substantively different from former claim 1. During reexamination, the examiner found claim 1 invalid. In an August 12, 2010, advisory action the examiner noted that claim 1 failed to provide a function for the "stack pointer" and the claim language only identified the stack pointer as "bidirectionally connected to an internal bus," – an error claim 11 corrected. The examiner also observed that the additional language in claim 11 avoided the May reference, U.S. Patent No. 4,758,948 ("the '948 patent"), that teaches using a push down stack but not expressly a stack pointer performing the function that the amended language defines. Therefore, that the absolute intervening rights doctrine bars infringement liability prior to the issuance of the reexamination certificate.

TPL sees it differently. The change to claim 11 only makes the claim more definite. The examiner's primary concern with claim 1 centered on the discussion in the May patent of an instruction pointer. The instruction pointer identifies the instructions of a process and under the broadest interpretation the stack pointer likewise could be construed to read onto the prior art. No person of ordinary skill in the art would understand a stack pointer could not perform equivalently to an instruction pointer. As described in claim 1, the stack pointer would be understood by a person of ordinary skill in the art to point to only to the first push down stack referenced in claim 1 – and so the additional language only explicitly states what a person of ordinary skill in the art already would understand claim 1 to teach.

HTC replies that TPL's arguments rely on extrinsic evidence and that the intrinsic evidence reveals that absent the added limitation, the stack pointer was impermissibly vague and the amendment substantively narrowed the claim.

The court agrees with HTC. As the examiner's office actions indicated, in the original claim language the stack pointer did nothing except connect to the internal data bus, but TPL's argument that a person of ordinary skill in the art necessarily would color in the ambiguity with an understanding that the stack pointer points only to the first push down stack is not persuasive. As HTC points out, claim 1 (and claim 11) employs the term "comprising," which reveals that the claim is "inclusive or open-ended and does not exclude additional, unrecited elements or method steps."[58] Given that the specification in fact references a second push down stack, the second stack must be presumed to be distinct from the return stack identified in the claim language, other push down stacks potentially could be used and still fall within claim 1. Thus, where the stack pointer points matters. If multiple push down stacks were included in a processor, it is unclear under the language of claim 1 whether the stack pointer points to one of the stacks, all of the stacks, or some multiple in between.

At bottom, the court finds the added language limits the stack pointer to the first push down stack and substantively changes the scope of the claim. Because the added claim language narrows the scope of the claims, any claims of infringement before the date of the issuance of the reexamination certificate must be precluded.

b. Willful Infringement of the '890 Patent

The court finally addresses the issue of willful infringement related to the '890 patent.

HTC asserts that under the objective recklessness prong, the reexamination and amendment of the '890 patent supports HTC's position that it was not objectively reckless. HTC points out that TPL has offered no evidence that it even knew of the '890 patent before the suit. HTC also argues that the failure by TPL to pursue a preliminary injunction suggests that willful infringement is not at issue.

[58] *CollegeNet, Inc. v. ApplyYourself, Inc.*, 418 F.3d 1225, 1235 (Fed. Cir. 2005).

TPL responds that it provided notice to HTC of the patents and of its infringing behavior in 2006. The reexamination process actually cuts against HTC because most of the substance of the patents in fact survived intact with a "second stamp of validity from the PTO."[59] The PTO accepts 92% of reexamination applications, so the PTO's grant of patent reexamination is not enough to undercut willful infringement.[60] A "substantial question of patentability raised by a reexamination request is not dispositive" in a willfulness inquiry.[61]

Although the record at least suggests that HTC was made aware of the patents-in-suit as early as November 2006,[62] as discussed above the reexamined '890 patent bars claims of infringement before the date of the issuance of the certificate because the additional language added to independent claim 11 narrowed the scope of the claim.[63] It follows that because HTC cannot be held liable for infringement before March 1, 2011, willful infringement for this period is precluded.

The court next turns to whether HTC can be found to have willfully infringed the '890 patent following reexamination. Generally, a "patentee who does not attempt to stop an accused infringer's activities [by moving for a preliminary injunction] should not be allowed to accrue

[59] Docket No. 469 at 17.

[60] *See id.* n.11.

[61] *Plumley v. Mockett*, 836 F. Supp. 2d 1053, 1075 (C.D. Cal. 2010); *see also See Lucent Techs., Inc. v. Gateway, Inc.*, Case No. 07–cv–2000–H, 2007 WL 6955272, at *7 (S.D. Cal. Oct. 30, 2007) ("The Court does not assume that a reexamination order will always prevent a plaintiff from meeting their burden on summary judgment regarding willful infringement, but it does consider this as one factor among the totality of the circumstances.").

[62] *See* Docket No. 469-12, Ex. C (correspondence from Alliacense notifying HTC that HTC was infringing the patents contained in the MMP Portfolio, including the '890 patent).

[63] Moreover, at least one district court has noted, albeit in dicta, that "a patentee's willful infringement claim fails as a matter of law where the PTO requires amendments to the patent before issuing a reexamination certificate." *Plumley*, 836 F. Supp. 2d at 1075 (explaining court's opinion in *TGIP, Inc. v. AT & T Corp.*, 527 F. Supp. 2d 561 (E.D. Tex. 2007)).

enhanced damages based solely on the infringer's post-filing conduct."[64] But as TPL happily highlights, HTC conceded in prior litigation "that *Seagate* did not create a *per se* bar to claims for post-filing willful infringement where an injunction was not sought."[65] "Because *Seagate* did not create a *per se* bar, the determination of whether a patentee may pursue a claim for willful infringement based on post-filing conduct without seeking a preliminary injunction 'will depend on the facts of each case.'"[66] Patentees who neither practice the invention nor directly compete with the accused infringer are "excused from *Seagate's* rule that a patentee must seek an injunction to sustain a claim for post-filing willful infringement."[67] There may be circumstances "where an infringer's post-filing conduct was found to be willful" where "some material change that could create an objectively high likelihood of infringing a valid patent, such as a patent surviving a reexamination proceeding without narrowed claims."[68]

Viewing the evidence in the light most favorable to TPL and drawing all reasonable inferences in its favor, especially TPL's successful licensing program related to the patents-in-suit, the court concludes that a reasonable fact finder could plausibly find facts supporting a conclusion of willful infringement following the reexamination of the '890 patent.

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[64] *Seagate*, 497 F.3d at 1372; *see also Anascape, Ltd. v. Microsoft Corp.*, Case No. 9:06-cv-158, 2008 WL 7182476 (E.D. Tex. Apr. 25, 2008) (patentee who did not move for preliminary injunction was not entitled to benefit from its lack of diligence by obtaining enhanced damages for willfulness during the post-filing period).

[65] *DataQuill Ltd. v. High Tech Computer Corp.*, 887 F. Supp. 2d 999, 1015 (S.D. Cal. 2011).

[66] *Id.* (citing *Seagate* 497 F.3d at 1374).

[67] *Id.*

[68] *LML Holdings, Inc. v. Pac. Coast Distrib. Inc.*, Case No. 11-cv-06173-YGR, 2012 WL 1965878 (N.D. Cal. May 30, 2012) (citing *St. Clair Intellectual Prop. Consultants, Inc. v. Palm, Inc.*, Case No. 04–1436–JJF–LPS, 2009 WL 1649751, at *1 (D. Del. Jun.10, 2009)); *see also Webmap Technologies, LLC v. Google, Inc.*, Case No. 2:09–cv–343–DF–CE, 2010 WL 3768097, at *2-3 (E.D. Tex. Sep. 10, 2010).

IT IS SO ORDERED.

Dated: September 17, 2013

PAUL S. GREWAL
United States Magistrate Judge

United States District Court
For the Northern District of California

IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

Acer, Inc.,

Plaintiff,

v.

Technology Properties Ltd, et al.,

Defendants.
_____/

HTC Corp.,

Plaintiff,

v.

Technology Properties Ltd, et al.,

Defendants.
_____/

Barco NV,

Plaintiff,

v.

Technology Properties Ltd, et al.,

Defendants.
_____/

NO. C 08-00877 JW
NO. C 08-00882 JW
NO. C 08-05398 JW

FIRST CLAIM CONSTRUCTION ORDER

I. INTRODUCTION

Technology Properties Limited, Patriot Scientific Corporation and Alliacense, Ltd. (collectively, "Defendants") own a group of five patents known as the Moore Microprocessor

Portfolio patents.[1] Plaintiffs Acer, Inc.,[2] HTC Corp.[3] and Barco, N.V.[4] each filed lawsuits seeking a judicial declaration that the Patents-in-Suit are either invalid or are not infringed. Defendants filed counterclaims for infringement of the Patents-in-Suit. In due course, the actions were related and consolidated.[5]

On January 27, 2012, the Court conducted a hearing in accordance with Markman v. Westview Instruments, Inc.,[6] to construe language of the asserted claims over which there is a dispute. At the hearing, in addition to the normal intrinsic evidence, the parties relied upon a prior

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[1] The five Patents-in-Suit are U.S. Patent Nos. 5,809,336 ("the '336 Patent"), 5,784,584 ("the '584 Patent"), 5,440,749 ("the '749 Patent"), 6,598,148 ("the '148 Patent") and 5,530,890 ("the '890 Patent").

[2] The first of these now-consolidated actions was filed on February 8, 2008. Acer filed suit against Defendants seeking a judicial declaration that the '336 Patent, the '584 Patent and the '749 Patent are invalid or are not infringed by Acer. (See Docket Item No. 1 in No. C 08-00877 JW.) On November 21, 2008, Defendants counterclaimed for infringement of the '336 Patent and the '749 Patent. (See Docket Item No. 60 in No. C 08-00877 JW.) On February 9, 2009, Acer amended its complaint to add claims pertaining to the '148 Patent and the '890 Patent. (See Docket Item No. 98 in No. C 08-00877 JW.) On February 24, 2009, Defendants counterclaimed with respect to those two patents. (See Docket Item No. 99 in No. C 08-00877 JW.)

[3] On February 8, 2008, HTC also filed suit seeking a judicial declaration that the '336 Patent, the '584 Patent, the '749 Patent and the '148 Patent are invalid or are not infringed by HTC. (See Docket Item No. 1 in No. C 08-00882 JW.) On July 10, 2008, HTC amended its complaint to add claims pertaining to the '890 Patent. (See Docket Item No. 34 in No. C 08-00882 JW.) On November 21, 2008, Defendants counterclaimed with respect to each of those patents except for the '584 Patent. (See Docket Item No. 60 in No. C 08-00882 JW.)

[4] On December 1, 2008, Barco filed suit seeking a judicial declaration that the '584 Patent, the '749 Patent and the '890 Patent are invalid or are not infringed by Barco. (See Docket Item No. 1 in No. C 08-05398 JW.) On February 17, 2009, Defendants counterclaimed for infringement with respect to the '749 Patent, the '890 Patent and the '336 Patent. (See Docket Item No. 27 in No. C 08-05398 JW.)

[5] Judge Fogel ordered the cases related. (See Docket Item No. 21 in No. C 08-00882 JW; Docket Item No. 21 in No. C 08-05398 JW.) On September 1, 2011, this matter was reassigned from Judge Fogel to Chief Judge Ware. (See Docket Item No. 291 in No. C 08-00877 JW.)

[6] 517 U.S. 370 (1996).

claim construction order by Judge T. John Ward[7] and documentary material from reexamination proceedings.[8]

This Claim Construction Order sets forth the Court's construction of disputed words and phrases tendered to the Court for construction.

II. STANDARDS AND PROCEDURES FOR CLAIM CONSTRUCTION

A. General Principles of Claim Construction

Claim construction is a matter of law, to be decided exclusively by the Court. Markman, 517 U.S. at 387. In accordance with the Patent Local Rules of the Northern District, the parties submit their joint selection of the ten disputed terms that are significant in resolving the case as well as their proposed definitions for construction. See Patent L.R. 4-3. After the Markman hearing and upon consideration of the parties' briefs, the Court issues an order construing the meaning of the disputed terms. The Court's construction becomes the legally operative meaning of the disputed terms that governs further proceedings in the case. See Chimie v. PPG Indus., Inc., 402 F.3d 1371, 1377 (Fed.

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[7] In 2006, Defendants filed a patent infringement suit based upon three of the Patents-in-Suit in this matter–the '336 Patent, the '148 Patent and the '584 Patent–in the Eastern District of Texas. (See Order Denying Motions to Dismiss, to Transfer Venue, and to Stay at 3, Docket Item No. 47 in No. C 08-00877 JW (discussing the Texas action).) Defendants brought that action against unrelated third parties. (See id.) On June 15, 2007, Judge Ward issued a Claim Construction Order in the Texas action in which he construed some of the words and phrases from the three patents at issue in that case. See Tech. Props. Ltd. v. Matsushita Elec. Indus. Co., Ltd., 514 F. Supp. 2d 916 (E.D. Tex. 2007).

[8] As of April 30, 2009, "a total of eleven reexamination proceedings had been initiated against the [Patents-in-Suit] in the United States Patent and Trademark Office ('USPTO')." (Order Granting in part Motion to Stay at 2-3, Docket Item No. 144 in No. C 08-00877 JW.) On June 17, 2009, the Court granted in part motions to stay this action pending reexamination of several of the Patents-in-Suit. (See id.) On February 22, 2010, the Court lifted the stay. (See Docket Item No. 156 in No. C 08-00877 JW.)

The reexamination certificate for the '749 Patent was issued on June 7, 2011. (See Declaration of James C. Otteson in Support of Defendants' Opening Claim Construction Brief for the "Top Ten" Terms, hereafter, "Otteson Decl.," Ex. BB, Ex Parte Reexamination Certificate, Docket Item No. 310-6.) The reexamination of the '749 Patent resulted in amendments to Claim 1, among others. Claim 1 of the '749 Patent–which includes multiple disputed terms–was amended to include the two "wherein" clauses. (See id.)

The reexamination certificate for the '336 Patent was issued on December 15, 2009. (See Otteson Decl., Ex. DD, Ex Parte Reexamination Certificate, Docket Item No. 310-8.) The reexamination of the '336 Patent resulted in amendments to Claims 1, 6 and 10, and the addition of Claim 11, among others. (Id.)

Cir. 2005). Although greater weight should always be given to the intrinsic evidence,[9] claim construction is a fluid process in which the Court may consider a number of extrinsic sources of evidence, so long as they do not contradict the intrinsic evidence. See Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582-83 (Fed. Cir. 1996).

B. Construction from the Viewpoint of an Ordinarily Skilled Artisan

A patent's claims define the scope of the patent: the invention that the patentee may exclude others from practicing. Phillips, 415 F.3d at 1312. The Court generally gives the patent's claims their ordinary and customary meaning. In construing the ordinary and customary meaning of a patent claim, the Court does so from the viewpoint of a person of ordinary skill in the art at the time of the invention, which is considered to be the effective filing date of the patent application. Thus, the Court seeks to construe the patent claim in accordance with what a person of ordinary skill in the art would have understood the claim to have meant at the time the patent application was filed. This inquiry forms an objective baseline from which the Court begins its claim construction. Id. at 1313.

The Court proceeds from that baseline under the premise that a person of ordinary skill in the art would interpret claim language not only in the context of the particular claim in which the language appears, but also in the context of the entire patent specification of which it is a part. Phillips, 415 F.3d at 1313. Additionally, the Court considers that a person of ordinary skill in the art would consult the rest of the intrinsic record, including any surrounding claims, the drawings and the prosecution history, if it is in evidence. Id.; see also Teleflex, Inc. v. Fisosa N. Am. Corp., 299 F.3d 1313, 1324 (Fed. Cir. 2002). In reading the intrinsic evidence, a person of ordinary skill in the art would give consideration to whether the disputed term is a term commonly used in lay language, a technical term, or a term defined by the patentee.

C. Commonly Used Terms

In some cases, disputed claim language involves a commonly understood term that is readily apparent to the Court. In such a case, the Court considers that a person of ordinary skill in the art

[9] Phillips v. AWH Corp., 415 F.3d 1303, 1324 (Fed. Cir. 2005).

would give the term its widely accepted meaning, unless a specialized definition is stated in the patent specification or was stated by the patentee during prosecution of the patent. In articulating the widely accepted meaning of such a term, the Court may consult a general purpose dictionary. Phillips, 415 F.3d at 1314.

D. Technical Terms

If a disputed term is a technical term in the field of the invention, the Court considers that one of skill in the art would give the term its ordinary and customary meaning in that technical field, unless a specialized definition is stated in the specification or during prosecution of the patent. Phillips, 415 F.3d at 1314. In arriving at this definition, the Court may consult a technical art-specific dictionary or invite the parties to present testimony from experts in the field on the ordinary and customary definition of the technical term at the time of the invention. Id.

E. Defined Terms

It is well established that a patentee is free to act as his or her own lexicographer. See, e.g., Process Control Corp. v. HydReclaim Corp., 190 F.3d 1350, 1357 (Fed. Cir. 1999). Acting as such, the patentee may use a term differently than a person of ordinary skill in the art would understand it, without the benefit of the patentee's definition. Vitronics Corp., 90 F.3d at 1582. Thus, the Court examines the claims and the intrinsic evidence to determine if the patentee used a term with a specialized meaning.

The Court regards a specialized definition of a term stated in the specification as highly persuasive of the meaning of the term as it is used in a claim. Phillips, 415 F.3d at 1316-17. However, the definition must be stated in clear words which make it apparent to the Court that the term has been defined. See id.; Vitronics Corp., 90 F.3d at 1582. If the definition is not clearly stated or cannot be reasonably inferred, the Court may decline to construe the term pending further proceedings. Statements made by the patentee in the prosecution of the patent application as to the scope of the invention may be considered when deciding the meaning of the claims. Microsoft Corp. v. Multi-Tech Systems, Inc., 357 F.3d 1340, 1349 (Fed. Cir. 2004). Accordingly, the Court

may also examine the prosecution history of the patent when considering whether to construe the claim term as having a specialized definition.

In construing claims, it is for the Court to determine the terms that require construction and those that do not. See U.S. Surgical Corp. v. Ethicon, Inc., 103 F.3d 1554, 1568 (Fed. Cir. 1997). Moreover, the Court is not required to adopt a construction of a term, even if the parties have stipulated to it. Pfizer, Inc. v. Teva Pharm. USA, Inc., 429 F.3d 1364, 1376 (Fed. Cir. 2005). Instead, the Court may arrive at its own constructions of claim terms, which may differ from the constructions proposed by the parties.

III. DISCUSSION

Pursuant to the Patent Local Rules, the parties have tendered ten terms that they have identified as significant to resolving these cases. The parties have asked the Court to consider the tendered words and phrases in a particular order. However, because the sequence in which the patents were issued might influence how a person of ordinary skill in the art would understand the patents, the Court will discuss the words and phrases in the order in which they appear in the Patents-in-Suit.[10]

A. '749 Patent

The '749 Patent is entitled: "High Performance, Low Cost Microprocessor Architecture."

Claim 1 of the '749 Patent, as allowed after reexamination, provides:[11]

> A microprocessor system, comprising a central processing unit integrated circuit, a memory external of said central processing unit integrated circuit, a bus connecting said central processing unit integrated circuit to said memory, and means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory, said means for fetching instructions being configured and connected to fetch **multiple sequential instructions** from said memory in parallel and **supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle**, said bus having a width at least equal to a number of bits in each of the instructions times a number of the

[10] Subject to further proceedings, the Court's construction of any particular term is presumed to apply consistently across all claims in the Patents-in-Suit in which the term appears. See, e.g., Paragon Solutions, LLC v. Timex Corp., 566 F.3d 1075, 1087 (Fed. Cir. 2009).

[11] Unless otherwise indicated, all bold typeface is added by the Court for emphasis.

> instructions fetched in parallel, said central processing unit integrated circuit including an arithmetic logic unit and **a first push down stack connected to said arithmetic logic unit**, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input, a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack, said arithmetic logic unit having an output connected to said means for storing a top item;
> wherein
> the microprocessor system comprises an **instruction register** configured to store the multiple sequential instructions and from which instructions are accessed and decoded;
> and wherein
> the means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to the central processing unit integrated circuit during a single memory cycle comprises supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched.

Claim 1 recites a microprocessor system. The parties have tendered for construction a number of words and phrases used in Claim 1.

1. "multiple sequential instructions"

Claim 1 recites that the system comprises, among other components, a "means for fetching"[12] that is configured to fetch "multiple sequential instructions." The parties tender for construction the phrase "multiple sequential instructions."

Upon review, the Court finds that this phrase is composed of commonly used words that have a plain and ordinary meaning. There is nothing in the claim or written description that would lead a person of ordinary skill in the art to conclude that the inventors intended to use the phrase with anything other than its plain and ordinary meaning. In particular, the Court finds that the word "multiple" would have been understood, by a person of ordinary skill in the art, to mean "two or more," while the phrase "sequential instructions" would have been understood to mean "computer

[12] For convenience, the Court will refer to this "means" as the "means for fetching limitation."

instruction in a sequential order." Therefore, at this time, the Court declines to use any different words or phrases to construe the phrase "multiple sequential instructions."

2. ". . . configured and connected to . . . supply multiple sequential instructions to central processing unit integrated circuit during a single memory cycle"

Claim 1 recites that the "means for fetching" is configured and connected to supply multiple sequential instructions to the central processing unit "during a single memory cycle." The parties request the Court to decide what, if any, effect the reexamination proceedings had on the meaning of the phrase "during a single memory cycle."[13] Specifically, the issue tendered to the Court is whether the phrase should be defined as requiring a "prefetch buffer."

During reexamination, the inventors, in referring to the phrase "during a single memory cycle," defended allowance of the claim over a prior art reference known as "Edwards" by stating the following:

> Edwards describes the way the Transputer decodes and executes instructions. As described in Edwards, see, e.g., Fig. 8, below, instructions are supplied to a one-instruction-wide instruction buffer, one at a time, and are there decoded. Fetching multiple instructions into a prefetch buffer and then supplying them one at a time is not sufficient to meet the claim limitation–the supplying of "multiple sequential instructions to a CPU during a single memory cycle."[14]

Upon review, the Court does not find that the cited statements constitute a basis for construing the language of Claim 1 to include the presence or configuration of a prefetch buffer.[15]

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[13] (See, e.g., Plaintiffs' Consolidated Responsive Claim Construction Brief at 26-28, hereafter, "Plaintiffs' Brief," Docket Item No. 315 in No. C 08-00877 JW.)

[14] (See Declaration of Kyle Chen in Support of Plaintiffs' Consolidated Responsive Claim Construction Brief, hereafter, "Chen Decl.," Ex. 16, Amendment in Response to Non Final Office Action in Ex Parte Reexamination Proceedings at 26, Docket Item No. 316-16.)

[15] Plaintiffs cite to three additional statements made by the inventors that purportedly contain similar disavowals. (See Plaintiffs' Brief at 27-28.) However, the Court finds that none of these cited statements refer to a "prefetch buffer." Further, each cited statement expressly distinguishes the alleged invention from the prior art reference on the same basis, namely, that the instructions are supplied to the CPU "during a single memory cycle." (Id.)

Having disposed of the only issue tendered with respect to this phrase, the Court declines to further construe it.[16]

3. "push down stack connected to said arithmetic logic unit"

Claim 1 recites a central processing unit integrated circuit including an arithmetic logic unit and "a first push down stack connected to said arithmetic logic unit." The parties tender for construction the phrase "push down stack connected to said arithmetic logic unit."

As to this phrase, the Court finds that a person of ordinary skill in the art reading the '749 Patent would understand the phrase "push down stack" to mean a last-in, first-out ("LIFO") data storage structure, in which the last item placed (pushed) onto the stack is the first item removed (popped) from the stack.[17] Further, the Court finds that a person of ordinary skill in the art at the time of the invention would understand that a "push down stack" can be implemented using a dedicated top-of-stack register or a logical stack "pointer" to indicate the "top of the stack" element regardless of its location. For example, the written description discusses stack pointers 102 and 104 in Fig. 2.[18]

Finally, with respect to this phrase, the parties dispute whether the "connected to" language should be construed as "directly connected to" or "physically connected to." The claim requires that the push down stack be "connected" to the arithmetic logic unit. The Court finds that a person of

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[16] The parties did not request the Court to construe the meaning of the phrase "during a single memory cycle."

[17] See, e.g., MODERN DICTIONARY OF ELECTRONICS 603 (7th ed. 1999) (defining a "pushdown stack" as a "circuit that operates in the reverse of a shift register," and explaining that "[w]hereas[] a shift register is a first-in first-out (FIFO) circuit, pushdown stacks are last-in, first-out (LIFO) memories. When data is requested, the stack will read the last data stored, and all other data will move one step closer to the output. Unless memory is emptied, the first data in will never be retrieved."). The same source alternatively defines a "pushdown stack" as "[e]ssentially a last-in, first-out buffer" in which, "[a]s data is added, the stack moves down with the last item, added [sic] taking the top position. Id. Thus, the "[s]tack height varies with the number of stored items, increasing or decreasing with the entering or retrieving of data. The words push (move down) and pop (retrieve the most recently stoked [sic] item) are used to describe its operation." Id.

[18] Referring to Fig. 2, the specification states: "Stack pointer 102, return stack pointer 104, mode register 106 and instruction register 108 are also connected to the internal data bus 90 by lines 110, 112, 114 and 116, respectively." (See '749 Patent, Col. 6:39-42.)

ordinary skill in the art would understand that the stack might be implemented using "pointers," which negates the need to connect the stack directly or physically to the arithmetic logic unit.[19] Therefore, the Court declines to add as a limitation that the connection must be direct or physical.

Accordingly, the Court construes the phrase "push down stack connected to said arithmetic logic unit" to mean:

a last-in-first-out data storage element connected to the arithmetic logic unit.

4. "instruction register"

Claim 1 contains two "wherein" clauses. With respect to the first "wherein" clause, the parties tender for construction the phrase "wherein the microprocessor system comprises an instruction register."[20]

In computer systems, the phrase "instruction register" has a plain and ordinary meaning, namely, a "register in a central processing unit that holds the address of the next instruction to be executed."[21] A person of ordinary skill in the art reading the written description would understand that the inventors are using the phrase with its plain and ordinary meaning:

> Instruction register 108 receives four 8-bit byte instruction words 1-4 on 32-bit internal data bus 90.

('749 Patent, Col. 7:53-55.)[22]

The parties have drawn the Court's attention to a related term that was construed by Judge Ward and that was subsequently affirmed by the Federal Circuit. Judge Ward's construction related to phrases such as "instruction groups" and "operand" in Claim 29 of the '584 Patent. See Tech.

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[19] See MODERN DICTIONARY OF ELECTRONICS 603 (7th ed. 1999) ("In actual practice, a hardware-implemented pushdown stack is a collection of registers with a counter that serves as a pointer to indicate the most recently loaded register. Registers are unloaded in the reverse of the sequence in which they were loaded.").

[20] The Court notes that both the body of the claim and the first "wherein" clause disclose a microprocessor system *comprising* recited limitations. However, conventional claim language would have the wherein clause formatted to provide that "the microprocessor system *further* comprises . . ." to avoid any confusion between the wherein clause and the body of the claim.

[21] See MICROSOFT COMPUTER DICTIONARY 276 (5th ed. 2002).

[22] The Court notes that the phrase "8-bit byte" is unusual and appears to be redundant.

Props. Ltd., 514 F. Supp. 2d at 931-34. The claims of the '584 Patent deal specifically with an embodiment that includes "variable width operands." (See '584 Patent, Col. 16:7-26.) This particular embodiment requires all operands to be right justified in the instruction register so that the microprocessor can quickly locate the operands of variable width without the need "to specify the different operand sizes." (See '584 Patent, Col. 16:24-26.) However, unlike Claim 29 of the '584 Patent, Claim 1 of the '749 Patent does not contain such phrases. Thus, the Court does not find Judge Ward's construction pertinent.

Because the Court finds that the language of the claim has been used with its plain and ordinary meaning, the Court declines to further construe it.[23]

B. '890 Patent

Claim 11 of the '890 Patent[24] provides:

> A microprocessor, which comprises a main central processing unit and a **separate direct memory access central processing unit** in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being bidirectionally connected to a loop counter, said loop counter being connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said stack pointer pointing into said first push down stack, said internal data bus being connected to a memory controller, to a Y register of a return push down stack, an X register and a program counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said

[23] The Court notes that in a summary of an in-person interview with the examiner issued on October 25, 1994, the examiner noted with respect to Claim 1: "operand width is variable and right adjusted." (See Chen Decl., Ex. 19, Examiner Interview Summary Record, Docket Item No. 316-20.) The statement appears to have been made in an attempt to distinguish prior art known as "Boufarah," and the Court finds that it may potentially impose a limitation on the type of operands that are to be used and the positioning of the operands in the instruction register. The Court finds that a full understanding of the meaning of this statement and the events that gave rise to it might be relevant to the present analysis. Thus, the Court finds that it would benefit from further briefing as to this issue, as discussed below.

[24] The '890 Patent and the '336 Patent were filed on the same day. However, the '890 Patent was issued earlier than the '336 Patent. (See Chen Decl. ¶¶ 2, 12 (stating that the '890 Patent was issued on June 25, 1996, while the '336 Patent was issued on September 15, 1998).)

> incrementer being connected to said internal data bus, said direct memory access central processing unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

The parties tender for construction the phrase "separate direct memory access central processing unit."

Claim 11 provides two separate central[25] processing units ("CPU"): a "main" CPU and a "direct memory access" ("DMA") CPU. The Court finds that a person of ordinary skill in the art would understand "CPU" to mean a unit of a computing system that fetches, decodes, and executes programmed instructions.[26] In the written description, the inventors use the term CPU consistently with its plain and ordinary meaning.[27]

Further, the written description criticizes "[c]onventional microprocessors" that use "DMA controllers" because "some processing by the main central processing unit (CPU) of the microprocessor is required."[28] With respect to the DMA CPU, the written description states that an object of the invention is to provide a microprocessor "in which DMA does not require use of the main CPU during DMA requests and responses and which provides very rapid DMA response with predictable response times."[29]

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[25] The parties agree that a person of ordinary skill would understand "central" processing unit to refer to a processing unit, and that the word "central" does not necessarily connote the primary processor in a particular hierarchy.

[26] See, e.g., MODERN DICTIONARY OF ELECTRONICS 107 (7th ed. 1999) (defining a CPU as "[t]hat unit of a computing system that fetches, decodes, and executes programmed instructions and maintains the status of results as the program is executed").

[27] (See, e.g., '890 Patent, Col. 8:22-24 ("The DMA CPU 72 controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU 70 (FIG. 2) for time specific processing.").)

[28] ('890 Patent, Col. 1:52-58.)

[29] ('890 Patent, Col. 2:2-5.)

Accordingly, the Court construes the term "separate direct memory access central processing unit" to mean:

> **a central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit.**

C. '336 Patent

1. Claim 1

Claim 1 of the '336 Patent provides:

> A microprocessor system, comprising
> a single integrated circuit including a central processing unit and an **entire ring oscillator variable speed system clock** in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,
> said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,
> a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;
> an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and
> a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.

The parties tender the phrase "ring oscillator" for construction.

Upon review, the Court finds that one of ordinary skill in the art would understand the phrase "ring oscillator" to mean: "interconnected electronic components comprising multiple odd numbers of inverters arranged in a loop."[30] When a voltage is applied, the ring oscillator generates signals that are used by the processing unit to regulate the timing of its operations. In contrast with a circuit

[30] The parties agree that a "ring oscillator" is "an oscillator having a multiple, odd number of inversions arranged in a loop," which is the construction arrived at by Judge Ward in the Texas action, though they disagree about whether additional limitations should be added to Judge Ward's construction of the term. (See Plaintiffs' Brief at 3; Defendants' Opening Claim Construction Brief for the "Top Ten" Terms at 16-17, Docket Item No. 310 in No. C 08-00877 JW.)

that receives its timing signal from an external clock, a person of ordinary skill in the art reading the patent would understand that Claim 1 claims a "single integrated circuit," fabricated so as to include a "ring oscillator."

At issue is whether the phrase "ring oscillator" should be given a specialized meaning based on statements made by the inventors during reexamination of Claims 4 and 8 of the '148 Patent.[31]

Claim 4 of the '148 Patent claims in pertinent part:

> A microprocessor integrated circuit comprising . . . a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said integrated circuit substrate.

Claim 8 of the '148 Patent has a similarly worded limitation.

During reexamination, the examiner reviewed the allowance of Claims 4 and 8 over U.S. Patent No. 4,689,581 ("Talbot"). The Talbot Patent, which is entitled "Integrated Circuit Phase Locked Loop Timing Apparatus," claims:

> an integrated circuit device . . . and a timing apparatus . . . formed on a common single chip, said timing apparatus comprising a phase locked loop [comprising, *inter alia*] a voltage controlled oscillator arranged to be controlled by [a] voltage signal to produce [an] output timing signal at its output.

(Talbot, Col. 10:48-11:9.)

Preliminarily, the examiner rejected Claims 4 and 8 of the '148 Patent as unpatentable over Talbot. During the course of reexamination proceedings, the examiner conducted an interview with the patent owner and discussed whether Claims 4 and 8 were allowable over Talbot.[32] Afterward,

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[31] Because the '148 Patent shares the same specification with the '336 Patent and is directly related to the other three Patents-in-Suit, the Court finds that any representation regarding similar terms made by the inventors during the prosecution of the '148 Patent is relevant to its consideration and construction of the terms in the '336 Patent. See Microsoft Corp. v. Multi-Tech Sys., Inc., 357 F.3d 1340, 1350 (Fed. Cir. 2004) ("Any statement of the patentee in the prosecution of a related application as to the scope of the invention would be relevant to claim construction.").

[32] (See Otteson Decl., Ex. X, Ex Parte Reexamination Interview Summary, Docket Item No. 310-2.)

the examiner prepared and sent to the patent owner an "Interview Summary."[33] Specifically, with respect to the discussion of Talbot, the examiner wrote:

> Continuing, the patent owner further argued that the reference of Talbot does not teach of a "ring oscillator." The patent owner discussed features of a ring oscillator, such as being **non-controllable**, and being **variable based on the environment**. **The patent owner argued that these features distinguish over what Talbot teaches**. The examiner will reconsider the current rejection based on a forthcoming response, which will include arguments similar to what was discussed.[34]

In its post-interview submission, the patent owner reiterated the contention that the claim should be allowed because Talbot disclosed a "voltage-controlled oscillator" and not the "ring oscillator" disclosed in the claim:

> Further, Talbot does not teach, disclose, or suggest the ring oscillator recited in claim 4. The Examiner cited col. 3, ll. 26-36, and oscillator circuit 12 shown in FIG. 1 of Talbot as teaching the recited ring oscillator. Talbot discusses a voltage-controlled oscillator (VCO) 12, but does not teach or disclose a ring oscillator.[35]

During the course of these claim construction proceedings, the inventors have continued to maintain that Talbot was overcome during reexamination because it does not disclose a "ring oscillator."[36]

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[33] An examiner's interview summary may serve as a basis for finding a prosecution disclaimer that narrows the claim scope. See, e.g., Rheox, Inc. v. Entact, Inc., 276 F.3d 1319, 1322 (Fed. Cir. 2002); Biovail Corp. Int'l v. Andrx Pharms., Inc., 239 F.3d 1297, 1302-04 (Fed. Cir. 2001).

[34] (See Chen Decl., Ex. 4, Ex Parte Reexamination Interview Summary, Docket Item No. 316-4 (emphasis added).)

[35] (Otteson Decl., Ex. Y, Remarks/Arguments at 11, hereafter, "Remarks," Docket Item No. 310-3.)

[36] For instance, Defendants argued during the Markman hearing that the inventors' written submission distinguished the Talbot reference because Talbot lacked a ring oscillator and never mentioned a requirement of "non-controllability." Further, Defendants also refer to the inventors' written response on February 21, 2008, which states:

> Further, **Talbot does not teach, disclose, or suggest the ring oscillator** recited in claim 4. ... Talbot discusses a voltage-controlled oscillator (VCO) 12, but **does not teach or disclose a ring oscillator**. Talbot provides two different implementations of the VCO 12 in FIGS. 3-4, **neither one of which is a ring oscillator**. Talbot refers to the oscillator of FIG. 3 as a "frequency controlled oscillator" (col. 7, ll. 21-22) and the oscillator of FIG. 4 simply as a "voltage controlled oscillator" (col. 8, ll. 59-65). As the sole inventor of the cited reference,

The Court has examined the Talbot patent. Although the component is, indeed, referred to as a "voltage-controlled oscillator," declarations and other extrinsic materials that have been tendered during the claim construction proceedings call into question the validity of the inventors' contention to the PTO and to this Court that the "ring oscillator" is different from the "voltage-controlled oscillator" disclosed in Talbot. On the one hand, the Court has received extrinsic evidence that the voltage-controlled oscillator disclosed in Talbot *is* a ring oscillator. On the other hand, arguments have been submitted claiming that the voltage-controlled oscillator of Talbot *is not* a ring oscillator.[37]

Under clear Federal Circuit law, a submission made by an inventor during reexamination is regarded as a disavowal only if the court finds that the allegedly disavowing statement is "so clear as to show reasonable clarity and deliberateness, and so unmistakable as to show unambiguous evidence of disclaimer." Omega Eng'g, Inc. v. Raytek Corp., 334 F.3d 1314, 1325 (Fed. Cir. 2003) (citations omitted).

Here, before arriving at a decision on the definition of the phrase "ring oscillator" in the context of the Talbot reference, the Court finds that it would benefit from further briefing. In the supplement briefs, the declarants shall fully articulate the technical basis for their opinions with respect to whether the voltage-controlled oscillator disclosed in Talbot is or is not a ring oscillator. The Court will return to the construction of the phrase "ring oscillator" following the completion of the supplement briefing.

> Talbot presumably possesses at least ordinary skill in the art, yet Talbot did not characterize either of the disclosed oscillators as ring oscillators. Applicants respectfully assert that the reason they were not characterized by Talbot as ring oscillators is because **they are not ring oscillators**. For at least the foregoing reasons, **Talbot does not teach, disclose, or suggest a ring oscillator** as recited in the claims. (Remarks at 11 (emphases added).)

[37] This issue is important to claim construction, because it is relevant to understanding in what manner the ring oscillator is "non-controllable," as distinguished from the voltage-controlled oscillator disclosed in Talbot. Resolving this conflict might affect how the Court approaches issues with respect to the validity of the patent claim at issue.

2. Claim 6

Claim 6 of the '336 Patent provides:

> A microprocessor system comprising:
> a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;
> an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator **clocking said central processing unit** at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way **as a function of parameter variation** in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and
> an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.

a. "clocking said central processing unit"

The parties tender for construction the phrase "clocking said central processing unit."

Upon review, the Court finds that to one of ordinary skill in the art, the plain and ordinary meaning of "clocking said central processing unit" is to provide a clock signal to the central processing unit.

A further issue tendered with respect to this phrase is whether, based on the written description, the construction should include a limitation of the maximum or optimum frequency of the "clocking" function. In the written description of the '336 Patent, the phrase "maximum frequency possible" is used with respect to an embodiment.[38] A description of an embodiment in the specification may not be imposed as a limitation "unless the patentee has demonstrated a clear

[38] (See '336 Patent, Col. 16:67-17:2 (stating that "[b]y deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast.").)

intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'" Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc., 381 F.3d 1111, 1117 (Fed. Cir. 2004) (citation omitted). Here, the Court finds that the cited language does not demonstrate "a clear intention to limit the claim scope." Id.

Accordingly, the Court construes "clocking said central processing unit" to mean:

providing a timing signal to said central processing unit.

b. "as a function of parameter variation"

The parties tender for construction the phrase "as a function of parameter variation." The full phrase is: "thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way **as a function of parameter variation."**

The disputed issue is whether the phrase requires a mathematical type predetermined functional relationship. Upon review, the Court finds that a person of ordinary skill in the art reading the patent would understand that the phrase "as a function of" is describing a variable that depends on and varies with another.[39] Because neither the written description nor the prosecution history provide a basis for concluding that the phrase should be limited to a narrower definition of an exact mathematical type functional relationship, the Court declines to do so. Having resolved the only dispute tendered with respect to this phrase, the Court declines to construe it further.

3. Claim 10

Claim 10 of the '336 Patent provides:

> In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:
>
> providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a

[39] The Court observes that "function" is a very broad term. See, e.g., MODERN DICTIONARY OF ELECTRONICS 311-12 (7th ed. 1999) (defining "function" as, *inter alia*, a "quantity of value that depends on the value of one or more other quantities" or a "specific purpose of an entity, or its characteristic action," and defining a number of phrases that include the term "function," such as "function codes," "function keys" and a "function table").

> first plurality of transistors and being operative at a processing frequency;
>
> **providing an entire variable speed clock disposed upon said integrated circuit substrate**, said variable speed clock being constructed of a second plurality of transistors;
>
> clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;
>
> connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and
>
> clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.

The parties have tendered for construction the phrase "providing an entire variable speed clock disposed upon said integrated circuit substrate." There are two issues that are tendered with respect to this language. First, there is a dispute over whether the "variable speed clock" should be defined as limited to a ring oscillator. Here, the Court observes that, in other claims, the inventor discusses a "ring oscillator" as a variable speed system clock. Nonetheless, with respect to this Claim, the Court declines to limit the broader phrase found in Claim 10 to a ring oscillator only.

Second, the parties tender a dispute over the degree of independence between the signal of the "variable speed clock" and any external reference signal. However, upon review the Court finds that this dispute is not pertinent to the construction of the tendered phrase.

Accordingly, the Court construes "providing an entire variable speed clock disposed upon said integrated circuit substrate" to mean:

> **Providing a variable speed clock that is located entirely on the same semiconductor substrate as the central processing unit.**

4. Claim 11

Claim 11 of the '336 Patent provides:

> A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, **wherein said central processing unit operates asynchronously to said input/output interface**.

The parties tender for construction the phrase "wherein said central processing unit operates asynchronously to said input/output interface."

Claim 11 discloses a microprocessor system comprising, among others, a central processing unit and an entire ring oscillator variable speed system clock connected to said central processing unit, an on-chip input/output interface, and "a second clock independent of said ring oscillator variable speed system clock" connected to said input/output interface. The subject phrase is contained in a "wherein" clause that describes the relationship between the timing control signal of the central processing unit and the timing signal of the on-chip input/output interface. The claim discloses that the central processing unit operates "asynchronously" to the input/output interface.

The written description is silent as to whether there is or can be *any* timing relationship between the central processing unit and the input/output interface or between their respective clocks.

The inventors first introduced the term "operates asynchronously to" during the re-examination of the '336 Patent in order to "clarify the meaning of 'independent' as recited in the

claims."[40] The examiner had focused on a reference known as "Kato" that purported to show two clock signals that are "in synchronism with each other." (Id. at 19.) The inventors explained that "Kato does not reveal any teaching that any of the components of the data processing circuit operate asynchronously with each other." (Id.) In support of the "independent" and "asynchronous" nature of its clocks, the inventors cited a textbook that describes what an asynchronous system is:

> An *asynchronous* system is one containing two or more independent clock signals. So long as each clock drives independent logic circuitry, such a system is effectively a collection of independent synchronous systems. **The logical combination of signals derived from independent clocks, however, poses difficulty because of the unpredictability of their phase relationship**.[41]

Reading this prosecution history, a person of ordinary skill would understand that the word "asynchronously"[42] means that the timing signal from one clock is independent from and not derived from the other clock such that a phase relationship between the two clocks is not readily predictable.

Accordingly, the Court construes "wherein said central processing unit operates asynchronously to said input/output interface" to mean:

> **the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them.**

IV. CONCLUSION

The Court has construed the phrases and terms tendered for construction.

On or before **June 29, 2012**, the parties shall meet and confer and file a Joint Statement addressing the following issues:

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[40] (See Declaration of Eugene Mar in Support of Defendants' Opening Claim Construction Brief, Ex. G, In re Ex Parte Reexamination of U.S. Patent No. 5,809,336 at 17, Docket Item No. 213-2.)

[41] (Id. (citing STEPHEN A. WARD & ROBERT H. HALSTEAD, JR., COMPUTATION STRUCTURES 93 (1990)) (emphasis added).)

[42] One source provides nine different meanings for the term "asychronous." See MODERN DICTIONARY OF ELECTRONICS 40 (7th ed. 1999) (defining the term, *inter alia*, as a "communication method in which data is sent when it is ready without being referenced to a timing clock, rather than waiting until the receiver signals that it is ready to receive" or as referring to "computer program execution [that is] unexpected or unpredictable with respect to the instruction sequence").

(1) A proposed schedule for supplemental briefs consistent with the terms of this Order;

(2) In light of the Court's impending retirement,[43] the Court proposes to assign this case to Magistrate Judge Grewal. In their Statement, the parties shall state whether they jointly consent to having this case immediately reassigned to Judge Grewal. In the event the parties do not consent to the immediate reassignment, the case will remain with Judge Ware and be subject to reassignment in due course.

Dated: June 12, 2012

JAMES WARE
United States District Chief Judge

[43] On April 28, 2012, Chief Judge Ware announced that he plans to "retire in August 2012 as the terms of his current law clerks come to an end." See Chief Judge Ware Announces Transition, *available at* http://www.cand.uscourts.gov/news/82.

THIS IS TO CERTIFY THAT COPIES OF THIS ORDER HAVE BEEN DELIVERED TO:

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Dated: June 12, 2012

Richard W. Wieking, Clerk

By: /s/ JW Chambers
William Noble
Courtroom Deputy

United States District Court
For the Northern District of California

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-00877 PSG **(Re: Docket Nos. 356, 357, 358, 374)**
HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-00882 PSG **(Re: Docket Nos. 385, 387, 388, 403)**

CLAIM CONSTRUCTION ORDER

In this patent infringement suit, Plaintiffs Acer, Inc., Acer America Corp., Gateway, Inc., and Plaintiffs HTC Corp. and HTC America, Inc. (collectively "Plaintiffs") seek a declaratory

judgment that they do not infringe patents owned by Defendants Technology Properties Ltd., Patriot Scientific Corp., and Alliacense Ltd. (collectively "Defendants").[1] Consistent with Pat. L.R. 4-3(c), the parties seek further construction of terms and phrases in claims in the patents-in-suit.[2] Plaintiffs and Defendants each also seek reconsideration of Judge Ware's earlier constructions of certain terms.[3]

As part of those motions for reconsideration, Plaintiffs seek to file a sur-reply on the grounds that Defendants' reply to their motion for reconsideration introduced new arguments and new evidence.[4] The court GRANTS Plaintiffs' motion to file the sur-reply.

In light of this case's long history and the trial date set for June 24, 2013, the court does not wish to add any further delay to the constructions by its preparation of a complete opinion setting forth its reasoning and analysis. To that end, the court at this time will simply issue its constructions without any significant reasoning and analysis:

CLAIM TERM	**CONSTRUCTION**
"instruction register"	Register that receives and holds one or more instructions for supplying to circuits that interpret the instructions
"ring oscillator"	an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment
"separate DMA CPU"	a central processing unit that accesses memory and that fetches and executes instructions directly and separately of the main central processing unit
"supply the multiple sequential instructions"	provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during

[1] Unless otherwise noted, the docket citations refer to Case No. 5:08-cv-00882 PSG.

[2] *See* Docket Nos. 387, 394.

[3] *See* Docket Nos. 385, 388.

[4] *See* Docket No. 403.

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	a single memory cycle
"clocking said CPU"	Providing a timing signal to said central processing unit

The parties should rest assured that the court arrived at these constructions with a full appreciation of not only the relevant intrinsic and extrinsic evidence, but also the Federal Circuit's teaching in *Phillips v. AWH Corp.*,[5] and its progeny. So that the parties may pursue whatever recourse they believe is necessary, a complete opinion will issue before entry of any judgment.

IT IS SO ORDERED.

Dated: December 4, 2012

PAUL S. GREWAL
United States Magistrate Judge

[5] 415 F.3d 1303, 1312-15 (Fed. Cir. 2005).

United States District Court
For the Northern District of California

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-00877 PSG **(Re: Docket Nos. 356, 357, 358, 374)**
HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-00882 PSG **(Re: Docket Nos. 385, 387, 388, 403)**

CLAIM CONSTRUCTION ORDER

On November 30, 2012, following reassignment of this case to the undersigned with the consent of the parties and in light of the retirement of Chief Judge Ware, and the completion of an

extended *Markman* hearing, the court issued an order from the bench construing five of the parties' disputed terms. The court provided a written summary of its constructions a few days later.[1] The court now explains its reasoning below.

I. BACKGROUND

In this suit, Plaintiffs Acer, Inc., Acer America Corp., Gateway, Inc., HTC Corp., and HTC America, Inc.[2] seek a declaratory judgment that they do not infringe patents owned by Defendants Technology Properties, Patriot Scientific, and Alliacense (collectively "TPL"). All of the patents at issue relate to various aspects of microprocessors.

On November 30, 2012, the court held a claim construction hearing to consider five disputed terms. Prior to the case being reassigned to the undersigned, Judge Ware considered the same five terms.[3] He construed three of them and asked for more briefing on two of them, although he also provided a tentative construction for the two.[4]

The Eastern District of Texas also has considered related terms in another case that TPL filed in 2006 against unrelated third parties. In that case, Judge Ward held a claim construction hearing and issued a decision construing terms based upon patents with the same specification as the patents at issue in this suit.[5] Several terms he construed overlap with terms at issue here. Although the case resolved before proceeding to trial, TPL appealed a portion of the claim construction ruling to the Federal Circuit with respect to one of the three patents in suit; the Federal Circuit affirmed the district court's judgment against TPL.[6]

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[1] *See* Docket No. 381.

[2] Barco N.V. was originally a party and was a party to the motions at issue, but is no longer involved in the case.

[3] *See* Docket No. 336.

[4] *See id*.

[5] *See Tech. Properties Ltd. v. Matsushita Elec. Indus. Co., Ltd.*, 514 F. Supp. 2d 916, 927 (E.D. Tex. 2007) *aff'd sub nom.*, 276 F. App'x 1019 (Fed. Cir. 2008). At issue were United States Patent Nos. 5,809,336, 6,598,148, and 5,784,584.

[6] *See Tech. Properties Ltd., Inc. v. Arm, Ltd.*, 276 F. App'x 1019 (Fed. Cir. 2008).

The terms at issue are found in United States Patent No. 5,440,749 (the "'749 Patent") titled "High Performance, Low Cost Microprocessor Architecture,"[7] United States Patent No. 5,809,336 (the "'336 Patent") titled "High Performance Microprocessor Having Variable Speed System Clock,"[8] and United States Patent No. 5,530,890 (the "'890 Patent"), titled "High Performance, Low Cost Microprocessor."[9] All three patents derive from the same original patent application that was subject to a ten-way restriction requirement and eventually resulted in six different patents known as the Moore Microprocessor Portfolio patents, all of which share a common specification.

The '749 Patent claims an invention that accelerates the operation of microprocessors by fetching multiple instructions from memory per memory cycle. Because a CPU can execute instructions faster than it can fetch them from memory, fetching multiple instructions per memory cycle can improve overall performance.

The '336 Patent claims an invention that allows the frequency of a CPU to fluctuate based upon conditions. Traditional microprocessors use fixed frequency clocks to regulate the frequency with which the CPU operates. Fixed clocks generally have to be set lower than the CPU's maximum possible frequency to ensure proper operation under the worst-case conditions. The '336 Patent claims an invention that solves this problem by placing a ring oscillator on the same microchip as the CPU to act as the clock. Because the ring oscillator is on the same microchip and made out of the same components as the CPU, it is subject to the same environmental conditions and thus it will operate at a variable speed based upon conditions allowing the CPU to operate at higher rates during good conditions and lower rates during bad.

The '890 Patent relates to microprocessor architecture and claims a direct memory access mechanism. Most microprocessors have a direct memory access controller that handles the slow operation of reading and writing to memory so that the CPU can execute other instructions while waiting. The patent discloses a direct memory access CPU, which can execute some instructions in addition to reading and writing to memory for the CPU.

[7] *See* Docket No. 358-2.

[8] *See* Docket No. 358-6.

[9] *See* Docket No. 368-2.

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II. LEGAL STANDARDS

Claim construction is exclusively within the province of the court.[10] "To construe a claim term, the trial court must determine the meaning of any disputed words from the perspective of one of ordinary skill in the pertinent art at the time of filing."[11] This requires a careful review of the intrinsic record, comprised of the claim terms, written description, and prosecution history of the patent.[12] While claim terms "are generally given their ordinary and customary meaning," the claims themselves and the context in which the terms appear "provide substantial guidance as to the meaning of particular claim terms."[13] Indeed, a patent's specification "is always highly relevant to the claim construction analysis."[14] Claims "must be read in view of the specification, of which they are part."[15]

Although the patent's prosecution history "lacks the clarity of the specification and thus is less useful for claim construction purposes," it "can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be."[16] The court also has the discretion to consider extrinsic evidence, including dictionaries, scientific treatises, and testimony from experts and inventors. Such evidence, however, is "less significant than the intrinsic record in determining the legally operative meaning of claim language."[17]

Judge Ware has already considered all of the terms currently before the court. Although the court granted leave for parties to file motions for reconsideration, it will take as its starting point that

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[10] *See Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 387 (1996).

[11] *Chamberlain Group, Inc. v. Lear Corp.*, 516 F.3d 1331, 1335 (Fed. Cir. 2008).

[12] *See id.*; *Phillips v. AWH Corp*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (internal citations omitted).

[13] *Phillips*, 415 F.3d at 1312, 1314.

[14] *Id.* at 1312-15.

[15] *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996); *see also Ultimax Cement Mfg. Corp v. CTS Cement Mfg. Corp.*, 587 F. 3d 1339, 1347 (Fed. Cir. 2009).

[16] *Phillips*, 415 F.3d at 1317 (internal quotations omitted).

[17] *Id.* (internal quotations omitted).

the earlier constructions are correct. Consistent with Local Rule 7-9, absent newly discovered material facts, change in law, or manifest failure to consider material facts or arguments, the court will not alter any earlier constructions.[18]

III. CLAIM CONSTRUCTION

A. "instruction register"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
Register that receives and holds one or more instructions for supplying to circuits that interpret the instructions, in which any operands that are present must be right-justified in the register	Register that receives and holds one or more instructions for supplying to circuits that interpret the instructions

The parties dispute the construction of "instruction register" as used in claim 1 of the '749 Patent. The term "instruction register" was added to a wherein clause in claim 1 of the '749 patent during reexamination. The patent claims a microprocessor system

> wherein the microprocessor system comprises an instruction register configured to store the multiple sequential instructions and from which instructions are accessed and decoded.[19]

Judge Ware tentatively construed "instruction register" in the '749 patent as having its plain and ordinary meaning.[20] Quoting a dictionary, he determined that instruction register meant a "register in a central processing unit that holds the address of the next instruction to be executed."[21] After construing the term, the court noted that the prosecution history might convince the court to limit its construction and requested more briefing.[22]

The parties agree that the term has a slightly different meaning than the one the court previously adopted because the court's previous definition came from a software dictionary and the patents are hardware-related. The parties agree that the meaning of "instruction register" in the

[18] *See Therasense, Inc. v. Becton, Dickinson & Co.*, 560 F. Supp. 2d 835, 844 (N.D. Cal. 2008) (following courts in the Northern District of California that "have required a litigant to meet the Civil Local Rule 7-9 standard when requesting reconsideration of a claim construction").

[19] *See* Docket No. 358-2, Reexam. Cert., col.1 ll.55-60.

[20] *See* Docket No. 336 at 11.

[21] *Id.* at 10 (quoting MICROSOFT COMPUTER DICTIONARY 276 (5th ed. 2002)).

[22] *See id.* at 11 n.23.

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context of hardware is a "register that receives and holds one or more instructions for supplying to circuits that interpret the instructions." The court takes this construction as its starting point.

TPL urges the court to keep this construction while Plaintiffs argue for a more limited construction requiring that the operands in the register be right-justified. Even though Judge Ware's prior order indicated he was interested in an explanation of the prosecution history, the parties' arguments remain focused on the specification.

Plaintiffs argue that the specification requires the right-justified limitation for the register that it seeks. The Federal Circuit has instructed that "the specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess" or "reveal an intentional disclaimer."[23] However, only a clear disclaimer can justify narrowing the construction.[24] Where a patent consistently references a certain limitation or a preferred embodiment as the present invention, that also can serve to limit the scope of the invention where no other intrinsic evidence suggests otherwise.[25]

Here, Plaintiffs rely on a section of the patent specification that explains that the patented invention is able to use variable width operands because "operands must be right justified in the instruction register."[26] The specification describes this limitation as necessary to make the "magic" of the patent possible.[27] Plaintiffs argue that this is the equivalent of defining the "present invention," but the intrinsic evidence does not clearly support this limitation.

First, the right justified limitation is not a clear and consistent limitation given the overall context of the patent and the specification. The '749 patent is derived from an application that was subject to a ten-way restriction requirement that eventually resulted in six different patents. The original application, which eventually issued as the '749 patent disclosed all of the inventions in

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[23] *Phillips*, 415 F.3d at 1316.

[24] *See Voda v. Cordis Corp.*, 536 F.3d 1311, 1320 (Fed. Cir. 2008).

[25] *See Absolute Software, Inc.*, 659 F.3d at 1136.

[26] *See* Docket No. 358-2 at col.18 ll.43-45.

[27] *Id.*

what is now their extensive shared specification.[28] Plaintiffs rely on one small section of the common specification, with the heading "Variable Width Operands," covering about twenty lines of the thirty-three column specification.[29] Although this small section contains strong limiting language, because the specification is common to ten different inventions, it does not necessarily apply to the '749 Patent. In fact, Judge Ware previously held that one of those inventions, disclosed in the '584 patent, deals specifically with variable width operands.[30] But variable width operands are not essential to what is claimed in the '749 Patent. Claim 1 of the '749 Patent, the claim at issue here, does not contain the term operand or require variable width operands. Although parties focus on the '749 patent, the same reasoning applies to the '890 Patent.

Second, the specification actually discloses an embodiment where the operands are not right justified. In one embodiment, the instruction register receives four 8-bit instructions.[31] The specification disclosed two instructions, the "Read-Local-Variable XXXX" and "Write-Local-Variable XXXX," which are fixed width instructions that have a 4-bit opcode and a 4-bit operand.[32] These instructions can go into any of the four 8-bit slots in the instruction register and thus would contain operands that are not right justified.[33] At oral argument, Plaintiffs disputed TPL's characterization of these embodiments, arguing that the "4-bit operands" are not actually operands, but the location in temporary storage where the operand actually exists.[34] Even if the location in temporary storage is not a traditional operand, it acts similarly to one and adds further intrinsic evidence supporting a finding that the right justified limitation does not apply to the '749 and '890 patents.

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[28] *See generally*, Docket No. 358-2 at col.1-35.

[29] *See* Docket No. 358-2 at col.18 ll.35-56.

[30] *See* Docket No. 336 at 11.

[31] *See* Docket No. 358-2 at col.7 ll.50-58.

[32] *See* Docket No. 358-2 at col.31-32 ll.45-15.

[33] *See generally*, *id.* at col.7 ll.50-58.

[34] *See* Docket No. 382 at 106-07.

Plaintiffs do briefly cite to the prosecution history where, in a handwritten summary of an in-person interview in response to a Patent Office Action rejecting several of the claims of a related patent, the examiner stated "Claim 1: Operand width is variable + right adjusted."[35] Because various claims were withdrawn, however it is unclear to exactly what claim the examiner referred. This is not clear and unmistakable disavowal by the applicant.[36]

The parties agreed upon meaning alone should control. Accordingly, the court construes "instruction register" as the "register that receives and holds one or more instructions for supplying to circuits that interpret the instructions."

B. "ring oscillator"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is (1) non-controllable; and (2) variable based on the temperature, voltage and process parameters in the environment	an oscillator having a multiple, odd number of inversions arranged in a loop

The parties ask the court to construe the term "ring oscillator" as it is used in claim 1 of the '336 Patent. Judge Ware held that one of ordinary skill in the art would understand the term to mean "interconnected electronic components comprising multiple odd numbers of inverters arranged in a loop."[37] However, he ordered more briefing as to whether the court should give the terms a specialized meaning based upon the statements of the inventors during reexamination to distinguish their invention from the Talbot Patent.[38]

Once again, the parties agree on the basic meaning of the term, but dispute additional limitations. They agree that the meaning of the term is at least "an oscillator having a multiple, odd

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[35] Docket No. 363-19 at 2.

[36] *See Univ. of Pittsburgh of Commonwealth Sys. of Higher Educ. v. Hedrick*, 573 F.3d 1290, 1297 (Fed. Cir. 2009) (finding a "patentee may limit the meaning of a claim term by making a clear and unmistakable disavowal of scope during prosecution," but an examiner's summary of disavowal may only create a "weak inference" of the disavowal); *3M Innovative Properties Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1373 (Fed. Cir. 2003) (finding that prosecution history "cannot be used to limit the scope of a claim unless the *applicant* took a position before the PTO." (emphasis in the original)).

[37] Docket No. 336 at 13.

[38] *Id.* at 14-16.

number of inversions arranged in a loop." TPL urges the court to adopt meaning alone while the Plaintiffs argue that the term must be further limited to be: (1) non-controllable and (2) variable based on temperature, voltage, and process parameters in the environment. Plaintiffs argue that the prosecution history and specification support their position. As explained below, the prosecution history is too ambiguous to support Plaintiffs' construction in full, but the specification and especially the claim language do support Plaintiffs' second limitation.

1. Prosecution history

A "clear and unmistakable" disavowal by the patentee during prosecution or reexamination can narrow the scope of a claim.[39] However, because the "ongoing negotiations between the inventor and the examiner" can "often produce ambiguities," the doctrine only applies to "unambiguous disavowals."[40]

In the patent examiner's summary of his meeting with the patent owner, he wrote that

> the patent owner further argued that the reference of Talbot does not teach of a 'ring oscillator.' The patent owners discussed features of a ring oscillator, such as being non-controllable and being variable based upon the environment. The patent owner argued that these features distinguish over what Talbot teaches.[41]

The examiner finished his summary noting that he would "reconsider the current rejection based upon a forthcoming response, which will include arguments similar to what was discussed."[42] The subsequent written response argued that the Talbot reference did not teach a ring oscillator generally, and did *not* specifically argue that the ring oscillator was "non-controllable."[43] The examiner accepted this argument and withdrew the rejection.[44]

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[39] *Grober v. Mako Products, Inc.*, 686 F.3d 1335, 1341 (Fed. Cir. 2012), reh'g denied (Sept. 14, 2012).

[40] *Id.*

[41] Docket No. 357-5 at 5. The interview summary relates to the '148 patent, but it shares the same specification with the '336 patent.

[42] *Id.*

[43] *See id.*

[44] *Id.* at 27.

Plaintiffs argue that the examiner's summary is a clear disavowal that should limit the scope of the claim. The court disagrees. The Federal Circuit has suggested that where, as here, the "disavowal" is only an examiner's summary of a patentee's statement, it only creates a "weak inference" of a disavowal.[45] The subsequent prosecution history does not support Plaintiffs' claim construction because the patent owner appears to have made a different argument in his written reply, simply stating that the Talbot reference did not include a ring oscillator *generally* and not distinguishing the ring oscillator of the '336 Patent based on the examiner's stated exemplary features of ring oscillators.[46]

During prosecution, the patent owner also stated that the "the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so."[47] This statement is not a disavowal because it only affirms that external inputs are "not required." The statement does not clearly impose a prohibition on all types of control.

2. Specification

Plaintiffs also argue that the specification supports their proposed construction. The specification describes the "ring oscillator" as having its frequency "determined by the parameters of temperature, voltage, and process."[48] Although this portion of the specification appears to disclose the preferred embodiment rather than constitute an express limitation on the claimed invention,[49] Claim 1 of the '336 Patent *claims* that the processing frequency of the CPU and the ring

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[45] *See Univ. of Pittsburgh*, 573 F.3d at 1297.

[46] *See generally, Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1124 (Fed. Cir. 2004) (describing a series of exchanges between the patent owner and the examiner as the parties "talking past one another" and finding no clear evidence of a disavowal from the confused exchange).

[47] Docket No. 363-4 at 6.

[48] *See* Docket No. 358-6 at col.16 ll.59-60.

[49] *See Brookhill-Wilk 1, LLC. v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1301-02 (Fed. Cir. 2003) ("statements from the description of the preferred embodiment are simply that-descriptions of a preferred embodiment. . . Absent a clear disclaimer of particular subject matter, the fact that the inventor anticipated that the invention may be used in a particular manner does not limit the scope to that narrow context.")

oscillator vary together due to manufacturing variations, operating voltage, and temperature.[50] The claim itself provides that the "ring oscillator" is "constructed of the same process technology with corresponding manufacturing variations" on the same single integrated circuit so that its performance will fluctuate with the CPU because they are subject to the same "manufacturing variations" and "operating voltage and temperature."[51] During oral argument, TPL admitted that a ring oscillator on the same microprocessor as the CPU will vary based upon voltage, temperature, and process variations.[52] Therefore, based upon the claim language and the specification, the court finds that the disclosed "ring oscillator" varies with voltage, temperature, and process variations.

Even though the claimed "ring oscillator" is "determined by the parameters of temperature, voltage, and process," it does not necessarily follow, as Plaintiffs' argue, that the "ring oscillator" must be non-controllable.[53] The claims do not mention "controllable" or "non-controllable" in relation to the "ring oscillator" and neither does the specification. The term "non-controllable" is only used by the patent examiner in the prosecution history discussed above. Additionally, in the preferred embodiment, the "ring oscillator" is "determined" by temperature, voltage, and process,[54] which suggests at least one embodiment in which the ring oscillator is controlled.

Because of the clear limitation in the claims that temperature, voltage, and process determine the "ring oscillator's" frequency, the court includes those limitations in the construction of the term, but does not find similar support for importing the "non-controllable" limitation. The court therefore construes "ring oscillator" as "an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment."

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[50] *See* Docket No. 358-6, Reexam. Cert. col.2 ll.3-5.

[51] *Id.* at col.1-2 ll.59-05.

[52] *See* Docket No. 382 at 49:3-7.

[53] *See, e.g., Brookhill-Wilk*, 334 F.3d at 1301-02.

[54] *See* Docket No. 358-6 at col.16 ll.59-60.

C. "separate DMA CPU"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
a central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit	Electrical circuit for reading and writing to memory that is separate from a main CPU

Judge Ware previously construed the term "separate direct memory access central processing unit" ("separate DMA CPU") from Claim 11 of the '890 Patent. Claim 11 claims

> A microprocessor, which comprises a main central processing unit and a separate direct memory access [DMA] central processing unit [CPU] in a single integrated circuit comprising said microprocessor . . .

The court construed "separate DMA CPU," consistent with its plain and ordinary meaning as "a central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit."[55] Plaintiffs urge the court to keep this construction while TPL argues that previously unaddressed parts of the prosecution history support a different construction broad enough to include standard DMA controllers, which do not execute instructions.

TPL's primary argument is that the history of the Moore patents supports a broader construction. TPL argues that the DMA CPU that fetches and executes its own instructions was one of the ten categories of inventions derived from the original application, but not the invention that eventually became the patent at issue, the '890 Patent. As explained above, the original patent application for what became the '749 Patent was subject to a ten-way restriction. A restriction indicates that "two or more independent and distinct inventions are claimed in one application."[56] One of these 10 categories of inventions was focused on a "microprocessor system having a DMA for fetching instruction[s] for a CPU and itself."[57] The patentee eventually abandoned this application. The '890 Patent came from a different category of invention "drawn to a microprocessor architecture."[58] TPL argues that because the '890 Patent came from a different

[55] Docket No. 336 at 13.

[56] 35 U.S.C. § 121.

[57] Docket No. 368-7 at 3.

[58] *Id*. *See also* Docket No. 356 at 3-4.

invention category, it should not be read to include the definition of the "DMA CPU" that was the subject of another invention.

The court disagrees. The fact that one abandoned patent focused on a particular subject matter does not necessarily mean that same subject matter cannot be within the scope of another related patent based upon the same specification. First, restriction requirements have little, if any, evidentiary weight.[59] Second, there is nothing in the claims to suggest that "DMA CPU" should have anything other than its plain and ordinary meaning. Third, the specification supports the plain and ordinary meaning. The specification discloses a "DMA CPU" in figures 2 and 9. When describing figure 2, the specification states that the "DMA CPU 72 controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU 70."[60] The "DMA CPU 314" in figure 9 is part of another microprocessor that the specification describes as equivalent to the microprocessor in figure 2.[61] A separate passage in a later section of the specification describes another embodiment where the "DMA processor 72 of the microprocessor 50 has been replaced with a more traditional DMA controller 314."[62] The specification goes on to describe the characteristics of a DMA controller. These sections are clear that a DMA controller is distinct from a DMA CPU and the patent refers to each by name where appropriate. Thus where the patent claims a DMA CPU, it means a DMA CPU and not a DMA controller.

TPL also argues that statements made during reexamination by the requester and the examiner support its position. The court disagrees. First, the examiner and the reexamination requester made the cited statements, not the patent owner.[63] Second, regardless of who made the

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[59] *See Honeywell Int'l, Inc. v. ITT Indus., Inc.*, 452 F.3d 1312, 1319 (Fed. Cir. 2006); *Rambus Inc. v. Hynix Semiconductor Inc.*, 569 F. Supp. 2d 946, 962 (N.D. Cal. 2008) ("In laying out the details of the original restriction requirement, the court recognizes its limited evidentiary significance.").

[60] *See* Docket No. 368-2 at col.8 ll.22-24.

[61] *See id.* at col.9 ll.5-6.

[62] *Id.* at col.12 ll.62-65.

[63] *See 3M Innovative Properties Co.*, 350 F.3d at 1373 (finding that prosecution history "cannot be used to limit the scope of a claim unless the *applicant* took a position before the PTO."(emphasis in the original)).

statements, they do not clearly show that the term "DMA CPU" was understood to include a DMA controller.[64]

During oral argument, TPL argued that the term "independently" in the original construction is unsupported.[65] The court agrees with this point. Even if the DMA CPU fetches and executes its own instructions, it cannot do so independently. The reason for putting the CPU and DMA CPU on the same chip is so they can work together.[66] Otherwise, the evidence in support of changing the court's prior construction is unpersuasive.

The court construes "separate DMA CPU" as "a central processing unit that accesses memory and that fetches and executes instructions directly and separately of the main central processing unit."

D. "supply the multiple sequential instructions"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during a single memory cycle without using a prefetch buffer or a one-instruction-wide instruction buffer that supplies on instruction at a time	provide the multiple sequential instructions in parallel to said central processing unit integrated circuit during a single memory cycle

The parties ask the court to construe the phrase "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle," from claim 1 of the '749 patent. Judge Ware previously determined that this phrase was composed of commonly used words that the patentee intended to have their plain and ordinary meaning. Plaintiffs argue for a narrower construction based upon disavowals during reexamination while TPL argues for a broad construction. The parties specifically dispute what limitations the patent places on how the "multiple sequential instructions" are provided to the CPU.

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[64] *See id.* at 1346-47 ("An applicant's silence in response to an examiner's characterization of a claim does not reflect the applicant's clear and unmistakable acquiescence to that characterization if the claim is eventually allowed on grounds unrelated to the examiner's unrebutted characterization.").

[65] *See* Docket No. 382 at 121-22.

[66] *See* Docket No. 368-2, Reexam. Cert., col.1 ll.22-24; Docket No. 368-2 at col.8 ll.22-24 (the DMA CPU "operates as a co-processor to the main CPU").

During reexamination, TPL unambiguously disavowed that instructions could be provided to the CPU one-by-one. The PTO issued a reexamination rejecting claims in the '749 Patent, including claim 1, based upon the "Edwards" patent[67] and an article by Doug MacGregor.[68] To distinguish the Edwards patent, TPL argued that in the Edwards patent, "instructions are supplied to a one-instruction-wide instruction buffer, one at a time," while for the '749 Patent "[f]etching multiple instructions into a prefetch buffer and then supplying them one at a time is not sufficient to meet the claim limitation—the supplying of 'multiple sequential instructions to a CPU during a single memory cycle.'"[69] Similarly, in distinguishing the invention in MacGregor, TPL wrote that "non-parallel supplying of instructions to the CPU is not supplying them to the CPU during a single memory cycle as required by the claim."[70] By this language, TPL clearly and unambiguously disavowed supplying instructions to the CPU one-by-one.

Plaintiffs also urge the court to find TPL disavowed specific structures or components in the above statements, but these statements as to structures are not clearly disavowals because they are made in the context of describing the prior art. There may be ways of incorporating such structures consistent with not supplying the instructions one-by-one.

Accordingly, the court construes the phrase "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle" as "provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during a single memory cycle."

E. "clocking said CPU"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
timing the operation of the CPU such that it will always execute at the maximum frequency possible, but never too fast	timing the operation of the CPU

[67] U.S. Patent No. 4,680,698.

[68] Doug MacGregor *et al.*, "The Motorola MC68020," IEEE Micro 101 (August 1984).

[69] Docket No. 358-3 at 27.

[70] *Id.* at 46.

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The parties ask the court to construe "clocking said CPU," which appears in claims 1, 6, and 10 of the '336 Patent. Generally speaking, "clocking the CPU" refers to using the system clock to control the speed of the CPU. Judge Ware previously considered "clocking said CPU" and based upon the plain and ordinary meaning of the term, construed it as "providing a timing signal to said central processing unit." The court considered other language in the written description that suggested a more limited construction, but ultimately determined that the patentee had not "demonstrated a clear intention to limit the claim scope."[71] Similarly, Judge Ward construed a longer term[72] from claim 1 containing the term "clocking said CPU" as "an oscillator that generates the signal(s) used for timing the operation of the CPU."[73] In construing the term, Judge Ward similarly did not adopt the type of limiting language that Plaintiffs advocate.

As discussed above and explained in the patent, the disclosed invention uses a variable speed clock—a ring oscillator—that varies with temperature, voltage, and process. The specification states that "[b]y deriving system time from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast."[74] Plaintiffs argue that this is a clear limitation that should be read into the claims. In general, absent a clear intention to limit the scope of a claim, a description of an embodiment should not limit claim language that otherwise has a broader effect.[75] This rule applies even if the patent only describes a single embodiment.[76] Judge Ware previously considered and rejected Plaintiffs attempt to limit the claim based upon the specification and this court agrees. There is no support in the claim language itself for the requirement that the clock always forces the CPU to operate at its maximum frequency. The court finds that operating at

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[71] Docket No. 336 at 17-18 (quoting *Innova/Pure Water*, 381 F.3d at 1117).

[72] Judge Ward construed "an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit."

[73] *Tech. Properties Ltd. v. Matsushita Elec. Indus. Co., Ltd.*, 514 F. Supp. 2d 916, 927 (E.D. Tex. 2007) aff'd sub nom., 276 F. App'x 1019 (Fed. Cir. 2008).

[74] *See* Docket No. 358-6 at col.16-17 ll.63-2.

[75] *See Innova/Pure Water*, 381 F.3d at 1117.

[76] *See id.*

the maximum frequency is merely the preferred embodiment and not the only manner in which the invention can operate.

Plaintiffs also try to introduce evidence from the prosecution history to support their argument. Although Plaintiffs quote a section from the prosecution history where the applicants used the magic words "the present invention," what the applicants disclosed is that the present invention includes a variable speed clock on the same microprocessor as the CPU and thus its speed will vary based upon environmental conditions.[77] This is exactly what is claimed in claim 1. The excerpt goes on to explain that one advantage of the variable speed clock is that it "allows the microprocessor to operate at its fastest safe operating speed,"[78] but again, this is just one embodiment and not necessarily a *requirement* of the invention. Plaintiffs' other citations to the prosecution history are similarly unconvincing.

Because the parties have not convinced the court that the prior construction was in error, the Court declines to change its construction. Accordingly, the court construes "clocking said CPU" as "providing a timing signal to said central processing unit."

IV. CONCLUSION

For the reasons set forth above, the court construes the claims as follows:

CLAIM TERM	CONSTRUCTION
"instruction register"	Register that receives and holds one or more instructions for supplying to circuits that interpret the instructions
"ring oscillator"	an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment
"separate DMA CPU"	a central processing unit that accesses memory and that fetches and executes instructions directly and separately of the main central processing unit
"supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle"	provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during

[77] *See* Docket No. 358-9 at 4-5.

[78] *Id.* at 5.

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	a single memory cycle
"clocking said CPU"	Providing a timing signal to said central processing unit

Dated: August 21, 2013

PAUL S. GREWAL
United States Magistrate Judge

United States District Court
For the Northern District of California

United States District Court
For the Northern District of California

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, et al., Defendants.	Case No.: 5:08-cv-00882-PSG **ORDER RE: EMERGENCY MOTION FOR ADDENDUM TO JURY INSTRUCTIONS** **(Re: Docket Nos. 513, 590)**

Before the court is Plaintiff HTC Corporation and HTC America, Inc.'s (collectively "HTC") Emergency Motion for Addendum to Jury Instructions. The parties appeared for a hearing earlier today. After considering the parties' arguments the court rules as follows:

The court's final jury instructions will instruct the jury that the terms "entire ring oscillator variable speed system clock" (in claims 1 and 11), "entire oscillator" (in claims 6 and 13), and "entire variable speed clock" (in claims 10 and 16) are properly understood to exclude any external clock used to generate a signal.[1]

[1] *See* Docket No. 513 at 11.

IT IS SO ORDERED.

Dated: September 20, 2013

PAUL S. GREWAL
United States Magistrate Judge

United States District Court
For the Northern District of California

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION and HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED,

Defendants.

Case No. 5:08-cv-00882 PSG

[Related to Case No. 5:08-CV-00877 PSG]

~~[PROPOSED]~~ ORDER GRANTING EMERGENCY MOTION FOR CLARIFICATION OF ORDER ON ADDENDUM TO JURY INSTRUCTIONS

Complaint Filed: February 8, 2008
Trial Date: September 23, 2013

Date: September 23, 2013
Time: 9:00 a.m.
Place: Courtroom 5, 4th Floor
Judge: Hon. Paul S. Grewal

Having considered Defendants' Emergency Motion for Clarification of the Order on Addendum to the Joint Proposed Jury Instructions, the record in this case and all related facts and circumstances, and good cause appearing therefor, IT IS HEREBY ORDERED THAT:

The court's final jury instructions will instruct the jury that the terms "entire ring oscillator variable speed system clock" (in claims 1 and 11), "entire oscillator" (in claims 6 and 13), and "entire variable speed clock" (in claims 10 and 16) are properly understood to exclude any external clock used to generate the signal used to clock the CPU.

IT IS SO ORDERED.

Dated: September 23, 2013

Hon. Paul S. Grewal
United States Magistrate Judge

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United States District Court
For the Northern District of California

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, et al.,

Defendants.

Case No.: 5:08-cv-00882-PSG

FINAL JURY INSTRUCTIONS

(Re: Docket Nos. 513, 645)

1. FINAL INSTRUCTIONS

Duty of Jury

Members of the Jury: It is my duty to instruct you on the law.

You must not infer from these instructions or from anything I have said or done as indicating that I have an opinion regarding the evidence or what your verdict should be.

It is your duty to find the facts from all the evidence in the case. To those facts you will apply the law as I give it to you. You must follow the law as I give it to you whether you agree with it or not. And you must not be influenced by any personal likes or dislikes, opinions, prejudices, or sympathy. That means that you must decide the case solely on the evidence before you. You will recall that you took an oath to do so.

In following all my instructions, you must follow all of them and not single out some and ignore others; they are all important.

Burden of Proof – Preponderance of the Evidence

When a party has the burden of proof on any claim or affirmative defense by a preponderance of the evidence, it means you must be persuaded by the evidence that the claim or affirmative defense is more probably true than not true.

You should base your decision on all of the evidence, regardless of which party presented it.

Burden of Proof – Clear and Convincing Evidence

When a party has the burden of proof on any claim or affirmative defense by clear and convincing evidence, it means you must be persuaded by the evidence that the claim or affirmative defense is highly probable. This is a higher standard of proof than proof by a preponderance of the evidence.

You should base your decision on all of the evidence, regardless of which party presented it.

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What Is Evidence

The evidence you are to consider in your deliberations in deciding what the facts are consists of:

1. The sworn testimony of any witness;

2. The exhibits which are received into evidence; and

3. Any facts to which the lawyers have agreed.

What Is Not Evidence

In reaching your verdict, you may consider only the testimony and exhibits received into evidence. Certain things are not evidence, and you may not consider them in deciding what the facts are. I will list them for you:

(1) Arguments and statements by lawyers are not evidence. The lawyers are not witnesses. What they have said in their opening statements and their closing arguments, and at other times is intended to help you interpret the evidence, but it is not evidence. If the facts as you remember them differ from the way the lawyers have stated them, your memory of them controls.

(2) Questions and objections by lawyers are not evidence. Attorneys have a duty to their clients to object when they believe a question is improper under the rules of evidence. You should not be influenced by the objection or by the court's ruling on it.

(3) Testimony that has been excluded or stricken, or that you have been instructed to disregard, is not evidence and must not be considered. In addition sometimes testimony and exhibits are received only for a limited purpose; when I have given a limiting instruction, you must follow it.

(4) Anything you may have seen or heard when the court was not in session is not evidence. You are to decide the case solely on the evidence received at the trial.

Evidence for a Limited Purpose

Some evidence may be admitted for a limited purpose only.

When I instruct you that an item of evidence has been admitted for a limited purpose, you must consider it only for that limited purpose and for no other.

Direct and Circumstantial Evidence

Evidence may be direct or circumstantial. Direct evidence is direct proof of a fact, such as testimony by a witness about what that witness personally saw or heard or did. Circumstantial evidence is proof of one or more facts from which you could find another fact. You should consider both kinds of evidence. The law makes no distinction between the weight to be given to either direct or circumstantial evidence. It is for you to decide how much weight to give to any evidence.

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Ruling on Objections

There are rules of evidence that control what can be received into evidence. When lawyers asked questions or offered exhibits into evidence and a lawyer on the other side thought it was not permitted by the rules of evidence, that lawyer may have objected. If I overruled the objection, the question was to be answered or the exhibit received. If I sustained the objection, the question was not answered, and the exhibit was not received. Whenever I sustained an objection to a question, you must ignore the question and must not guess what the answer might have been.

Sometimes I may have ordered that evidence be stricken from the record and that you disregard or ignore the evidence. That means that when you are deciding the case, you must not consider the evidence that I told you to disregard.

Credibility of Witnesses

In deciding the facts in this case, you may have to decide which testimony to believe and which testimony not to believe. You may believe everything a witness says, or part of it, or none of it. Proof of a fact does not necessarily depend on the number of witnesses who testify about it.

In considering the testimony of any witness, you may take into account:

(1) The opportunity and ability of the witness to see or hear or know the things testified to;

(2) The witness's memory;

(3) The witness's manner while testifying;

(4) The witness's interest in the outcome of the case and any bias or prejudice;

(5) Whether other evidence contradicted the witness's testimony;

(6) The reasonableness of the witness's testimony in light of all the evidence; and

(7) Any other factors that bear on believability.

The weight of the evidence as to a fact does not necessarily depend on the number of witnesses who testify about it.

No Transcript Available to the Jury

During deliberations, you will have to make your decision based on what you recall of the evidence. You will not have a transcript of the trial.

Taking Notes

I have permitted you to take notes to help you remember the evidence. If you did take notes, you may share them with your fellow jurors as you deliberate. No one will read your notes. They will be destroyed at the conclusion of the case.

Whether or not you took notes, you should rely on your own memory of the evidence. Notes are only to assist your memory. You should not be overly influenced by your notes or those of your fellow jurors.

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Jury to Be Guided By Official English Language Translation/Interpretation

Languages other than English were used during this trial.

The evidence to be considered by you is only that provided through the official court interpreters or translators. Although some of you may know the language used, it is important that all jurors consider the same evidence. Therefore, you must accept the English interpretation or translation. You must disregard any different meaning.

Use of Interpreters in Court

You must not make any assumptions about a witness or a party based solely upon the use of an interpreter to assist that witness or party.

Duty to Deliberate

At the conclusion of these final instructions, you will begin your deliberations. When you begin your deliberations, you should elect one member of the jury as your presiding juror. That person will preside over the deliberations and speak for you here in court.

You will then discuss the case with your fellow jurors to reach agreement if you can do so. Your verdict must be unanimous. Each of you must decide the case for yourself, but you should do so only after you have considered all of the evidence, discussed it fully with the other jurors, and listened to the views of your fellow jurors.

Do not hesitate to change your opinion if the discussion persuades you that you should. Do not come to a decision simply because other jurors think it is right.

It is important that you attempt to reach a unanimous verdict but, of course, only if each of you can do so after having made your own conscientious decision. Do not change an honest belief about the weight and effect of the evidence simply to reach a verdict.

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Deposition in Lieu of Live Testimony

You heard deposition testimony in this case. A deposition is the sworn testimony of a witness taken before trial. The witness is placed under oath to tell the truth and lawyers for each party may ask questions. The questions and answers are recorded. When a person is unavailable to testify at trial, the deposition of that person may be used at the trial.

You should consider deposition testimony, presented to you in court in lieu of live testimony, insofar as possible, in the same way as if the witness had been present to testify.

Do not place any significance on the behavior or tone of voice of any person reading the questions or answers.

Impeachment Evidence – Witness

The evidence that a witness lied under oath on a prior occasion may be considered, along with all other evidence, in deciding whether or not to believe the witness and how much weight to give to the testimony of the witness and for no other purpose.

Expert Opinion

Some witnesses, because of education or experience, were permitted to state opinions and the reasons for those opinions.

Opinion testimony should be judged just like any other testimony. You may accept it or reject it, and give it as much weight as you think it deserves, considering the witness's education and experience, the reason given for the opinion, and all the other evidence in the case.

Charts and Summaries Not in Evidence

Certain charts and summaries not received in evidence have been shown to you in order to help explain the contents of books, records, documents, or other evidence in the case. They are not themselves evidence or proof of any facts. If they do not correctly reflect the facts or figures shown by the evidence in the case, you should disregard these charts and summaries and determine the facts from the underlying evidence.

Demonstrative Evidence

During the trial, materials have been shown to you to help explain testimony or other evidence in the case. Other materials have also been shown to you during the trial, but they have not been admitted into evidence. You will not be able to review them during your deliberations because they are not themselves evidence or proof of any facts. You may, however, consider the testimony given in connection with those materials.

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Communication with Court

If it becomes necessary during your deliberations to communicate with me, you may send a note through the courtroom deputy, signed by your presiding juror or by one or more members of the jury. No member of the jury should ever attempt to communicate with me except by a signed writing; I will communicate with any member of the jury on anything concerning the case only in writing, or here in open court. If you send out a question, I will consult with the parties before answering it, which may take some time. You may continue your deliberations while waiting for the answer to any question. Remember that you are not to tell anyone – including me – how the jury stands, numerically or otherwise, until after you have reached a unanimous verdict or have been discharged. Do not disclose any vote count in any note to the court.

Return of Verdict

A verdict form has been prepared for you. After you have reached unanimous agreement on a verdict, your presiding juror will fill in the form that has been given to you, sign and date it, and advise the court that you are ready to return to the courtroom.

II. PATENT JURY INSTRUCTIONS

Summary of Contentions

I will now summarize for you each party's contentions in this case. I will then tell you what each party must prove to win on each of its contentions.

As I previously explained, HTC filed suit in this court seeking a declaration that no claim of the '336 patent is infringed by HTC.

TPL filed a counter complaint alleging that HTC infringes the '336 patent by making, importing, using, selling, and offering for sale products that TPL argues are covered by claims 6, 7, 9, 13, 14, and 15 of the '336 patent. TPL also argues that HTC's infringement was willful. TPL also argues that HTC actively induced infringement of these claims of the '336 patent by others. TPL is seeking money damages.

Your job will be to decide whether claims 6, 7, 9, 13, 14, and 15 of the '336 patent have been infringed. If you decide that any claim of the '336 patent has been infringed, you will then need to decide any money damages to be awarded to TPL to compensate it for the infringement. You will also need to make a finding as to whether the infringement was willful. If you decide that any infringement was willful, that decision should not affect any damage award you give. I will take willfulness into account later.

Interpretation of Claims

Before you decide whether HTC has infringed the claims of the patent, you will need to understand the patent claims. As I mentioned, the patent claims are numbered sentences at the end of the patent that describe the boundaries of the patent's protection. It is my job as judge to explain to you the meaning of any language in the claims that needs interpretation.

I have interpreted the meaning of some of the language in the patent claims involved in this case. You must accept those interpretations as correct. You should disregard any conflicting interpretation. My interpretation of the language should not be taken as an indication that I have a view regarding the issue of infringement. The decision regarding infringement is yours to make. The Parties have agreed to or the court has interpreted the following terms in the claims at issue. Any terms not construed below should be interpreted according to their plain and ordinary meaning.

U.S. Patent Number 5,809,336 ("the '336 patent")

1. The term "central processing unit" means "an electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions."

2. The term "oscillator" means "[a] circuit capable of maintaining an alternating output."

3. The term "on-chip input/output interface" means "[a] circuit having logic for input/output communications, where that circuit is located on the same semiconductor substrate as the CPU."

4. The term "integrated circuit" means "[a] miniature circuit on a single semiconductor substrate."

5. The term "microprocessor" means "[a]n electronic circuit that interprets and executes programmed instructions."

6. The term "oscillator . . . clocking" means "an oscillator that generates the signal(s) used for timing the operation of the CPU."

7. The term "processing frequency" means "[t]he speed at which the CPU operates."

8. The term "varying . . . in the same way" mean "[i]ncreasing and decreasing proportionally."

9. The term "external clock is operative at a frequency independent of a clock frequency of said oscillator" means "an external clock wherein a change in the frequency of either the external clock or oscillator does not affect the frequency of the other."

10. The term "external memory bus" means "[a] group of conductors coupled between the I/O interface and an external storage device."

11. The term "Off-chip external clock" means "[a] clock not on the integrated circuit substrate."

12. The term "external clock is operative at a frequency independent of a clock frequency of said oscillator" means "[a]n external clock wherein a change in the frequency of either the external clock or oscillator does not affect the frequency of the other."

13. The term "Track" means "[i]ncreasing and decreasing proportionally."

14. The term "clocking said central processing unit" means "providing a timing signal to said central processing unit."

15. The term "wherein said central processing unit operates asynchronously to said input/output interface" means "the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them."

16. The term "ring oscillator" means "an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment."

17. The court has also found that a person of ordinary skill in the art reading the patent would understand that the phrase "as a function of" is describing a variable that depends on and varies with another, though not necessarily in an exact mathematical type functional relationship.

18. The term "entire oscillator" (in claims 6 and 13) is properly understood to exclude any external clock used to generate the signal used to clock the CPU.

Infringement

I will now instruct you on the rules you must follow in deciding whether TPL has proven that HTC has infringed one or more of the asserted claims 6, 7, 9, 13, 14, and 15 of the '336 patent. To prove infringement of any claim, TPL must persuade you that it is more likely than not that HTC has infringed that claim.

Direct Infringement

A patent's claims define what is covered by the patent. A product directly infringes a patent if it is covered by at least one claim of the patent.

Deciding whether a claim has been directly infringed is a two-step process. The first step is to decide the meaning of the patent claim. I have already made this decision, and I have already instructed you as to the meaning of the asserted patent claims. The second step is to decide whether HTC has made, used, sold, offered for sale or imported within the United States a product that is covered by a claim of the '336 patent. If it has, it infringes. You, the jury, make this decision.

With one exception, you must consider each of the asserted claims of the patent individually, and decide whether the HTC products infringe that claim. The one exception to considering claims individually concerns dependent claims. A dependent claim includes all of the requirements of a particular independent claim, plus additional requirements of its own. As a result, if you find that an independent claim is not infringed, you must also find that its dependent claims are not infringed. On the other hand, if you find that an independent claim has been infringed, you must still separately decide whether the additional requirements of its dependent claims have also been infringed.

Whether HTC knew their respective products infringed or even knew of the patent does not matter in determining direct infringement. For purposes of this case, there is one way in which a patent claim may be directly infringed: literal infringement. The following instructions will provide more detail on this type of direct infringement.

Literal Infringement

To decide whether an HTC product literally infringes a claim of the '336 patent, you must compare that product with the patent claim and determine whether every requirement of the claim is included in that product. If so, that product literally infringes that claim. If, however, that product does not have every requirement or element of the patent claim, the product does not literally infringe that claim. You must decide literal infringement for each asserted claim separately and each of the accused HTC products should be separately compared to the invention described in each patent claim they are alleged to infringe.

Unless otherwise excluded by construction of the court, if the patent claim uses the term "comprising," that patent claim is to be understood as an open claim. An open claim is infringed as long as every requirement in the claim is present in an accused HTC product. The fact that an HTC mobile phone also includes other parts will not avoid infringement, as long as it has every requirement in the patent claim.

Inducing Patent Infringement

TPL argues that HTC indirectly infringed by actively inducing another to infringe the '336 patent. In order for there to be inducement of infringement by HTC, someone else must directly infringe a claim of the '336 patent; if there is no direct infringement by anyone, there can be no induced infringement. In order to be liable for inducement of infringement, HTC must:

(1) have intentionally taken action that actually induced direct infringement by another;

(2) have been aware of the '336 patent; and

(3) have known that the acts it was causing would be infringing.

If HTC did not know of the existence of the patent or that the acts it was inducing were infringing, it cannot be liable for inducement unless it actually believed that it was highly probable its actions would encourage infringement of a patent and it took intentional acts to avoid learning the truth. It is not enough that HTC was merely indifferent to the possibility that it might encourage infringement of a patent. Nor is it enough that HTC took a risk that was substantial and unjustified.

If you find that HTC was aware of the patent, but believed that the acts it encouraged did not infringe that patent, or that the patent was invalid, HTC cannot be liable for inducement.

Willful Infringement

In this case, TPL argues that HTC willfully infringed TPL's patent.

To prove willful infringement, TPL must first persuade you that HTC infringed a valid claim of TPL's patent. The requirements for proving such infringement were discussed in my prior instructions. In addition, to prove willful infringement, TPL must persuade you that it is highly probable that prior to the filing of the complaint on February 8, 2008, HTC acted with reckless disregard of the claims of TPL's patent.

To demonstrate such "reckless disregard," TPL must satisfy a two-part test. The first part of the test is objective. TPL must persuade you that HTC acted despite an objectively high likelihood that its actions constituted infringement of a valid patent. The state of mind of HTC is not relevant to this inquiry. Rather, the appropriate inquiry is whether the defenses put forth by HTC fail to raise any substantial question with regard to infringement or validity. Only if you conclude that the defenses fail to raise any substantial question with regard to infringement or validity, do you need to consider the second part of the test.

The second part of the test does depend on the state of mind of HTC. TPL must persuade you that HTC actually knew, or it was so obvious that HTC should have known, that its actions constituted infringement of a valid patent.

In deciding whether HTC acted with reckless disregard for TPL's patent, you should consider all of the facts surrounding the alleged infringement including, but not limited to, the following factors:

(1) Whether HTC acted in a manner consistent with the standards of commerce for its industry;

(2) Whether HTC intentionally copied a product of TPL covered by the patent;

(3) Whether or not HTC made a good-faith effort to avoid infringe the ’336 patent, for example, whether HTC attempted to design around the ’336 patent;

(4) Whether or not HTC tried to cover up its infringement;

(5) Whether or not there is a reasonable basis to believe that HTC did not infringe or had a reasonable defense to infringement.

Burden of Proof

I will instruct you about the measure of damages. By instructing you on damages, I am not suggesting which party should win on any issue. If you find that HTC infringed any valid claim of the '336 patent, you must then determine the amount of money damages to be awarded to TPL to compensate it for the infringement.

The amount of those damages must be adequate to compensate TPL for the infringement. A damages award should put the patent holder in approximately the financial position it would have been in had the infringement not occurred, but in no event may the damages award be less than a reasonable royalty. You should keep in mind that the damages you award are meant to compensate the patent holder and not to punish an infringer.

TPL has the burden to persuade you of the amount of its damages. You should award only those damages that TPL more likely than not suffered. While TPL is not required to prove their damages with mathematical precision, they must prove them with reasonable certainty. TPL is not entitled to damages that are remote or speculative.

Reasonable Royalty

If you determine that any products sold by HTC infringed any valid claims of the '336 patent, then TPL should be awarded a reasonable royalty for all sales associated with each such product infringing a particular patent.

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Reasonable Royalty – Definition

A royalty is a payment made to a patent holder in exchange for the right to make, use or sell the claimed invention. This right is called a "license." A reasonable royalty is the payment for the license that would have resulted from a hypothetical negotiation between the patent holder and the infringer taking place at the time when the infringing activity first began. In considering the nature of this negotiation, you must assume that the patent holder and the infringer would have acted reasonably and would have entered into a license agreement. You must also assume that both parties believed the patent was valid and infringed. Your role is to determine what the result of that negotiation would have been. The test for damages is what royalty would have resulted from the hypothetical negotiation and not simply what either party would have preferred.

One way to calculate a royalty is to determine a one-time lump sum payment that the infringer would have paid at the time of the hypothetical negotiation for a license covering all sales of the licensed product both past and future. This differs from payment of an ongoing royalty because, with an ongoing royalty, the licensee pays based on the revenue of actual licensed products it sells. When a one-time lump sum is paid, the infringer pays a single price for a license covering both past and future infringing sales.

It is up to you, based on the evidence, to decide what royalty is appropriate in this case.

Reasonable Royalty – Relevant Factors

In determining the outcome of the hypothetical negotiation, you should consider all facts known to the parties at the time infringement began. Some of the factors you may consider are:

(1) Royalties received by the patent holder for licensing the patent-in-suit, proving or tending to prove an established royalty.

(2) Rates the infringer paid for using other patents comparable to the patent-in-suit.

(3) The nature of the license, i.e., exclusive or nonexclusive, restricted or unrestricted in terms of territory or to whom products covered by the patent claim may be sold.

(4) The patent holder's policy to maintain its patent monopoly by not licensing others or by granting licenses under special conditions designed to preserve its monopoly.

(5) The commercial relationship between the patent holder and infringer, such as whether they are competitors in the same territory in the same line of business.

(6) The effect of selling the patented invention in promoting sales of other products of the infringer, the existing value of the patented invention to the patent holder as a generator of sales of non-patented items, and the extent of such derivative or convoyed sales.

(7) The duration of the patent and the term of the license.

(8) The established profitability of products covered by the patent claim, their commercial success, and their current popularity.

(9) The advantages and benefits of the patented invention over older modes or devices, if any, that had been used to work on similar problems.

(10) The nature of the patented invention, the character of the patent holders' products covered by it, and the benefits to those who have used the invention.

(11) The extent to which the infringer has made use of the patented invention and any evidence probative of the value of that use.

(12) The portion of the profit or selling price that was customary in the business or in comparable businesses allow for the use of the invention or analogous inventions.

(13) The portion of the realizable profits that should be credited to the patented invention as distinguished from non-patented elements, the manufacturing process, business risks, or significant features or improvements added by the infringer.

(14) The opinion and testimony of qualified experts.

(15) The amount that a prudent licensor (such as the patent holder) and a prudent licensee (such as the infringer) would have agreed upon at the time infringement began if both had been reasonably and voluntarily trying to reach an agreement.

No one factor is dispositive, and you should consider the evidence that has been presented to you in this case on each one of the factors. You may also consider any other factors which in your mind would have increased or decreased the royalty the infringer would have been willing to pay and the patent holder would have been willing to accept, acting as normally prudent business people. The final factor establishes the framework which you should use in determining a reasonable royalty, that is, the payment that would have resulted from a negotiation between the patent holder and the infringer taking place at a time when infringement began.

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Date of Commencement

Damages that TPL may be awarded by you commence on the date that HTC infringed the '336 patent.

Calculating Damages in Cases of Inducement

In order to recover damages for induced infringement, TPL must either prove that the accused devices necessarily infringe the ’336 patent or prove acts of direct infringement by others that were induced by HTC. Because the amount of damages for induced infringement is limited by the number of instances of direct infringement, TPL must further prove the number of direct acts of infringement of the ’336 patent—for example, by showing individual acts of direct infringement or by showing that a particular type of HTC products or uses directly infringes.

Patent Term Glossary

A number of terms are defined below for your information and convenience.

Abstract: A brief summary of the technical disclosure in a patent to enable the U.S. Patent and Trademark Office and the public to determine quickly the nature and gist of the technical disclosure in the patent.

Assignment: A transfer of patent rights to another called an "assignee" who upon transfer becomes the owner of the rights assigned.

Claim: Each claim of a patent is a concise, formal definition of an invention and appears at the end of the specification in a separately numbered paragraph. In concept, a patent claim marks the boundaries of the patent in the same way that a legal description in a deed specifies the boundaries of land, i.e. similar to a land owner who can prevent others from trespassing on the bounded property, the inventor can prevent others from using what is claimed. Claims may be independent or dependent. An independent claim stands alone. A dependent claim does not stand alone and refers to one or more other claims. A dependent claim incorporates whatever the other referenced claim or claims say.

Drawings: The drawings are visual representations of the claimed invention contained in a patent application and issued patent, and usually include several figures illustrating various aspects of the claimed invention.

Elements: The required parts of a device or the required steps of a method. A device or method infringes a patent if it contains each and every requirement of a patent claim.

Embodiment: A product or method that contains the claimed invention.

Examination: Procedure before the U.S. Patent and Trademark Office whereby a Patent Examiner reviews the filed patent application to determine if the claimed invention is patentable.

Filing Date: Date a patent application, with all the required sections, has been submitted to the U.S. Patent and Trademark Office.

Infringement: Violation of a patent occurring when someone makes, uses or sells a patented invention without permission of the patent holder, within the United States during the term of the patent. Direct infringement is making, using or selling the patented invention without permission.

Limitation: A required part of an invention set forth in a patent claim. A limitation is a requirement of the invention. The word "limitation" is often used interchangeably with the word "requirement."

Office Action: A written communication from the Patent Examiner to the patent applicant in the course of the application examination process.

Patent: A patent is an exclusive right granted by the U.S. Patent and Trademark Office to an inventor to prevent others from making, using, offering to sell, or selling an invention within the United States, or from importing it into the United States, during the term of the patent. When the patent expires, the right to make, use or sell the invention is dedicated to the public. The patent has three parts, which are a specification, drawings, and claims. The patent is granted after examination by the U.S. Patent and Trademark Office of a patent application filed by the inventor which has these parts, and this examination is called the prosecution history.

Patent and Trademark Office (PTO): An administrative branch of the U.S. Department of Commerce that is charged with overseeing and implementing the federal laws of patents and

trademarks. It is responsible for examining all patent applications and issuing all patents in the United States.

Prior Art: Previously known subject matter in the field of a claimed invention for which a patent is being sought. It includes issued patents, publications, and knowledge deemed to be publicly available such as trade skills, trade practices and the like.

Prosecution History: The prosecution history is the complete written record of the proceedings in the PTO from its initial application to the issued patent. The prosecution history includes the office actions taken by the PTO and the amendments to the patent application filed by the applicant during the examination process.

Reads On: A patent claim "reads on" a device or method when each required part (requirement) of the claim is found in the device or method.

Requirement: A required part or step of an invention set forth in a patent claim. The word "requirement" is often used interchangeably with the word "limitation."

Royalty: A royalty is a payment made to the owner of a patent by anon-owner in exchange or rights to make, use or sell the claimed invention.

Specification (Patent): The specification is a required part of a patent application and an issued patent. It is a written description of the invention and of the manner and process of making and using the claimed invention.

Addendum

A number of the HTC products accused of infringement in this case contain Qualcomm chips. The parties have agreed and HTC has verified that the HTC Phones listed in the table in Exhibit A contain the Qualcomm chips next to them. The parties have also agreed, and Qualcomm has verified, the following facts about the Qualcomm chips listed in Exhibit A:

1. The Qualcomm chips shown in Exhibit A contain the application processors shown in Exhibit A;

2. Each of the Qualcomm chips listed in Exhibit A includes phase locked loops (PLLs) at least one of which is associated with clocking the corresponding application processor;

3. Each of the PLLs in paragraph 2 contains a voltage controlled oscillator or a current controlled oscillator that has a multiple, odd number of inversions arranged in a loop.

4. The terms “application processor,” “clocking,” “voltage controlled oscillator” and “current controlled oscillator” used above come from Qualcomm technical documents produced in this case.

EXHIBIT A

HTC Phones with Qualcomm Chips

HTC Phone(s)	Qualcomm Chip	Application Processor
Mobile Phone Tilt / TyTN II [Kaiser]	MSM7200	ARM 11
HTC Touch Dual [Neon]	MSM7200	ARM 11
Touch Phone P3650 [Polaris]	MSM7200	ARM 11
Mobile Phone S730	MSM7200	ARM 11
HTC Touch Diamond [Diamond]	MSM7201	ARM 11
HTC T-Mobile G1 [Dream]	MSM7201	ARM 11
HTC Touch Phone Fuze [Raphael]	MSM7201	ARM 11
HTC Smartphone Wildfire [Bee]	MSM7625	ARM 11
HTC Shift X9000 [Atlantis]	MSM7500	ARM 11
HTC Smartphone S640 [Iris]	MSM7500	ARM 11
HTC S720 / SMT5800 [Libra]	MSM7500	ARM 11
Mobile Phone XV6800 / HTC PDA Phone P4000 / PPC-6800 [Mogul, Titan]	MSM7500	ARM 11
Touch Phone P3450	MSM7500	ARM 11
HTC Smartphone EVO Shift 4G [Speedy]	MSM7x30	Scorpion
HTC Smartphone G2 [Vision]	MSM7x30	Scorpion
HTC Smartphone Inspire 4G [Ace]	MSM7x30 / MSM8255	Scorpion
HTC Smartphone myTouch 4G [Glacier]	MSM7x30 / MSM8255	Scorpion
HTC Smartphone ThunderBolt	MSM7x30 / MSM8655	Scorpion
HTC Smartphone Desire [Bravo]	QSD8x50	Scorpion
HTC Smartphone Surround [Mondrian]	QSD8x50	Scorpion
HTC Smartphone HD7 [Schubert]	QSD8x50	Scorpion
HTC Smartphone EVO 4G [Supersonic]	QSD8x50	Scorpion

IT IS SO ORDERED.

Dated: September 30, 2013

PAUL S. GREWAL
United States Magistrate Judge

United States District Court
For the Northern District of California

Date Filed	#	Docket Text
10/02/2013	651	**ORDER DENYING 647 MOTION FOR JUDGMENT AS A MATTER OF LAW entered by Magistrate Judge Paul Singh Grewal. (This is a text-only entry generated by the court. There is no document associated with this entry.) (Entered: 10/02/2013)**

United States District Court
For the Northern District of California

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, et al.,

Defendants.

Case No.: 5:08-cv-00882-PSG

FINAL VERDICT FORM

(Re: Docket No. 524)

United States District Court
For the Northern District of California

VERDICT FORM

When answering the following questions and filling out this Verdict Form, please follow the directions provided throughout the form. Your answer to each question must be unanimous. Some of the questions contain legal terms that are defined and explained in detail in the Jury Instructions. Please refer to the Jury Instructions if you are unsure about the meaning or usage of any legal term that appears in the questions below.

We, the jury, unanimously agree to the answers to the following questions and return them under the instructions of this court as our verdict in this case.

I. U.S. Patent No. 5,809,336 ("the '336 patent")

A. Infringement

1. Literal Infringement

1. Do you find that TPL has proven by a preponderance of the evidence that HTC has literally infringed any of the following claims of the '336 patent?

You can only find claims 7 or 9 infringed if you previously found claim 6 infringed. You can only find claims 14 or 15 infringed if you previously found claim 13 infringed.

Claim	Yes (for TPL)	No (for HTC)
6	☑	☐
7	☑	☐
9	☑	☐
13	☑	☐
14	☑	☐
15	☑	☐

2. Inducement

2. Do you find that TPL has proven by a preponderance of the evidence for each of the claims below that HTC:

a. intentionally took an action that actually induced direct infringement of the '336 patent by a third party;

b. was aware of the '336 patent; and

c. knew that the actions, if taken, would cause infringement of the '336 patent?

You can only find claims 7 or 9 infringed if you previously found claim 6 infringed. You can only find claims 14 or 15 infringed if you previously found claim 13 infringed.

Claim	Yes (for TPL)	No (for HTC)
6	☐	☑
7	☐	☑
9	☐	☑
13	☐	☑
14	☐	☑
15	☐	☑

II. Damages

If you have found that HTC has not infringed any claim of the '336 patent please skip Question 3. Only answer Question 3 if you have found that HTC has infringed at least one claim of the '336 patent.

3. To the extent you have found that at least one claim of the '336 patent is infringed, what has TPL proven that it is entitled to as a reasonable royalty for infringement:

One-time (lump sum) payment of $ 958,560 for the life of the patent.

III. Willfulness

4. If you have found that HTC has infringed at least one claim of the '336 patent, has TPL proven that it is highly probable that HTC's infringement was willful?

Yes (for TPL)	No (for HTC)
☐	☑

The foreperson must sign and date this verdict form.

Signed: _____ Date: 10/03/2013

Foreperson

IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

HTC CORPORATION, et al.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, et al.,

Defendants.
_____/

No. CV08-00882 PSG

JUDGMENT IN A CIVIL CASE

(X) Jury Verdict. This action came before the court for a trial by jury. The issues have been tried and the jury has rendered its verdict.

() Decision by Court. This action came to trial or hearing before the court. The issues have been tried or heard and a decision has been rendered.

IT IS SO ORDERED AND ADJUDGED that pursuant to the jury verdict filed October 3, 2013, judgment is entered in favor of Defendants.

Dated: October 3, 2013

Richard W. Wieking, Clerk

By: Oscar Rivera
Deputy Clerk

United States District Court
For the Northern District of California

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, et al., Defendants.	Case No. 5:08-cv-00882-PSG **ORDER DENYING PLAINTIFFS' RENEWED MOTION FOR ENTRY OF JUDGMENT AS A MATTER OF LAW** **(Re: Docket No. 671)**

In this patent infringement suit, a jury found that the Plaintiffs in this action, HTC Corporation and HTC America, Inc. infringed a lone patent owned by Defendants Technology Properties Limited, Patriot Scientific Corporation, and Alliacense Limited (collectively, "TPL"). HTC now renews its motion for judgment as a matter of law pursuant to Fed. R. Civ. P. 50(b), arguing that no reasonable jury could have found that HTC infringes any asserted claim of U.S. Patent No. 5,809,336 ("the '336 patent). TPL opposes. The parties appeared for a hearing. After considering their oral arguments and those in the papers, the court DENIES HTC's motion.

I. BACKGROUND

Technology Properties Limited and Alliacense, Limited are California corporations with their principal place of business in Cupertino, California; Patriot Scientific Corporation is a Delaware corporation with its principal place of business in Carlsbad, California. These defendants – Technology Properties Limited, Alliacense, and Patriot (collectively "TPL") – claim ownership of a family of related microprocessor patents. TPL refers to those patents as the Moore Microprocessor Portfolio patents ("MMP patents"), in recognition of co-inventor Charles Moore's contributions.

A. The Long, Winding Road To Trial

HTC filed this suit on February 8, 2008, seeking a judicial declaration that four of the MMP patents – U.S. Patent Nos. 5,809,336 ("the '336 patent"), 5,784,584 ("the '584 patent"), 5,440,749 ("the '749 patent"), and 6,598,148 ("the '148 patent") – are invalid and/or not infringed.[1] TPL counterclaimed for infringement of the '336, '749, '148, and '890 patents on November 21, 2008.[2] On April 25, 2008, TPL filed two complaints in the Eastern District of Texas against HTC alleging infringement of the four patents at issue in the pending declaratory judgment action.[3] On June 4, 2008, TPL filed additional patent infringement actions against HTC in the Eastern District of Texas asserting U.S. Patent No. 5,530,890 ("the '890 patent").[4] On July 10, 2008, HTC amended its complaint before this court, adding claims for declaratory relief with respect to the '890 patent.[5] On February 23, 2009 the parallel Texas litigation was dismissed without prejudice following Judge Fogel's decision to deny TPL's Motion to Dismiss, or in the Alternative, to

[1] *See* Docket No. 1.

[2] *See* Docket No. 60 at 6-8.

[3] *See* Docket No. 16 at 3.

[4] *See* Docket No. 35 at 5.

[5] *See* Docket No. 34.

Transfer Venue in the California action.[6] On March 25, 2010, the court accepted the parties' stipulation to dismiss the '584 patent from this litigation.[7] On August 24, 2012, Technology Properties Limited, Patriot, and Phoenix Digital Solutions initiated an International Trade Commission investigation regarding HTC's alleged infringement of the '336 patent.[8] On July 17, 2013, the court accepted the parties' stipulation to dismiss the '148 and '749 patents from this litigation.[9] On September 19, 2013, the court accepted the parties stipulation to dismiss all claims relating to the '890 patent from this litigation.[10]

In sum, only the '336 patent was considered by the jury at trial.

B. The '336 Patent

The '336 patent issued on September 15, 1998, and describes a microprocessor with an internal variable speed clock, or oscillator, that drives the processor's central processing unit ("CPU").[11] Traditional microprocessors use external, fixed speed crystals to clock the CPU.[12] A CPU's maximum possible processing capacity depends on process, voltage, and temperature

[6] *See* Docket Nos. 49 (denying motion to dismiss, to transfer venue, and to stay) and 88 (granting motion for leave to file motion for reconsideration and denying motion for reconsideration).

[7] *See* Docket No. 152.

[8] *See* Docket No. 561-1. Claims 1, 6, 7, 9-11, and 13-16 were asserted in the investigation. On September 6, 2013, Administrative Law Judge James Gildea issued an Initial Determination from in the ITC proceeding holding that HTC did not violate Section 337 of the Tariff Act of 1930. *See id.*

[9] *See* Docket No. 462.

[10] *See* Docket No. 594.

[11] *See* Docket No. 393-3 at 1 ("A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a Central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor.").

[12] *See id.* at 17:12-14 ("Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations.").

("PVT parameters").[13] An external clock must therefore set the timing of the CPU to suboptimal PVT conditions, resulting in waste of the CPU's processing speed under optimal conditions. The internal, variable clock described in the '336 patent claims real-time adjustment of the timing of the CPU by placing the clock on the chip itself. Thus, the CPU can perform optimally under any set of parameters.[14] The microprocessor nevertheless requires a second external clock because devices other than the CPU do not operate at variable speed.[15]

Independent claim 6 provides:

A microprocessor system comprising:

> a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;
>
> an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

[13] *See id.* at 17:21-22 ("Speed may vary by a factor of four depending upon temperature, voltage, and process.").

[14] *See id.* at 17:32-34 ("By decoupling the variable speed of the CPU 70 from the fixed speed of the I/O interface 432, optimum performance can be achieved by each.").

[15] *See id.* at 44-53 ("The designer of a high speed microprocessor must produce a product which operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing. Temperature, voltage, and process all affect transistor propagation delays. Traditional CPU designs are done so that with the worse case of the three parameters, the circuit will function at the rated clock speed. The result are designs that must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse case conditions."); *id.* at 16:67-17:10 ("By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor 50 will operate slower than normal. Since the microprocessor 50 ring oscillator clock 430 is made from the same transistors on the same die as the latches and gates, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.").

> an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.[16]

C. The Verdict: HTC Infringes

A seven-day jury trial was held to consider whether HTC infringed the '336 patent.[17] At trial, HTC did not contest the validity of the '336 patent. HTC moved for judgment as a matter of law after the close of TPL's case.[18] After two days of deliberations, the jury found that HTC and its accused products literally infringed all asserted claims: 6, 7, 9, 13, 14, and 15.[19] As to damages, the jury made the following findings:

> 3. To the extent you have found that at least one claim of the '336 patent is infringed, what has TPL proven that it is entitled to as a reasonable royalty for infringement:
>
> One-time (lump sum) payment of $958,560 for the life of the patent.[20]

Following the jury verdict HTC filed a renewed motion for judgment as a matter of law that its products do not infringe the '336 patent.[21]

II. LEGAL STANDARDS

Fed. R. Civ. P. 50(b) provides that, upon a renewed motion for judgment as a matter of law, the court may: (1) "allow judgment on the verdict, if the jury returned a verdict," (2) "order a new trial," or (3) "direct the entry of judgment as a matter of law." To grant a Rule 50(b) motion, the court must determine that "the evidence, construed in the light most favorable to the non-moving

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[16] Docket No. 393-3.

[17] *See* Docket No. 657.

[18] *See* Docket No. 647. HTC also moved for judgment as a matter of law as to willful infringement and damages. The jury returned a verdict that HTC's infringement was not willful. HTC has not renewed its motion for judgment as a matter of law on the issue of damages. *See* Docket No. 654 at 3-4.

[19] *See* Docket No. 654 at 2.

[20] *Id.* at 4.

[21] *See* Docket 671.

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party, permits only one reasonable conclusion, and that conclusion is contrary to the jury's."[22] In other words, to set aside the verdict, there must be an absence of "substantial evidence" – meaning "relevant evidence that a reasonable mind would accept as adequate to support a conclusion" – to support the jury's verdict.[23] "Substantial evidence is more than a mere" scintilla;[24] it constitutes "such relevant evidence as reasonable minds might accept as adequate to support a conclusion even if it is possible to draw two inconsistent conclusions from the evidence."[25] In reviewing a motion for judgment as a matter of law, the court "must view the evidence in the light most favorable to the non-moving party and draw all reasonable inferences in its favor."[26] "In ruling on such a motion, the trial court may not weigh the evidence or assess the credibility of witnesses in determining whether substantial evidence exists to support the verdict."[27]

III. DISCUSSION

A. The Jury Considered Substantial Evidence that the Accused Products Involve An "Entire Oscillator"

HTC first disputes the sufficiency of evidence regarding practice of the "entire oscillator" limitation. The court addressed the term in its order granting-in-part summary judgment of

[22] *Callicrate v. Wadsworth Mfg.*, 427 F.3d 1361, 1366 (Fed. Cir. 2005) (*quoting Pavao v. Pagay*, 307 F.3d 915, 918 (9th Cir. 2002)) ("The Ninth Circuit upholds any jury verdict supported by substantial evidence.").

[23] *Id.*

[24] *Chisholm Bris. Farm Equip. Co. v. Int'l Harvester Co.*, 498 F.2d 1137, 1140 (9th Cir. 1974) (*quoting Consol. Edison Co. v. NLRB*, 305 U.S. 197, 229 (1938)).

[25] *Landes Constr. Co. v. Royal Bank of Canada*, 833 F.2d 1365, 1371 (9th Cir. 1987).

[26] *Transbay Auto Serv., Inc. v. Chevron U.S.A., Inc.*, Case No. 3:09-cv-04932 SI, 2013 WL 496098, at *2 (N.D. Cal. Feb. 7, 2013) (*quoting Josephs v. Pacific Bell*, 443 F.3d 1050, 1062 (9th Cir. 2006) ("We must view the evidence in the light most favorable to the nonmoving party – here, Josephs, – and draw all reasonable inferences in that party's favor.")).

[27] *Id.* (citing *Mosesian v. Peat, Marwick, Mitchell & Co.*, 727 F.2d 873, 877 (9th Cir. 1984) ("Neither the district court nor this court may weigh the evidence or order a result it finds more reasonable if substantial evidence supports the jury verdict.")).

non-infringement and no willfulness.[28] The court explained:

> The court agrees with HTC that the disputed limitations are properly understood to exclude any external clock used to generate a signal.[29] Nevertheless, there remains a factual dispute whether HTC's products contain an on-chip ring oscillator that is self-generating and does not rely on an input control to determine its frequency. While HTC's expert says that the PLLs generate the clock, TPL's expert counters that the ring oscillators generate the clock and the PLLs merely buffer or fix the frequency.[30] This is a classic factual question that requires a trial to answer.[31]

HTC argues that the record at trial was uncontroverted that the ring oscillator in all accused HTC products is a phase locked loop ("PLL") and that the frequency output from the PLL is used to clock the CPU in the accused products. In particular, the frequency generated by that PLL relies on an off-chip crystal to set the frequency which is used to clock the CPU. The court's construction teaches that if an off chip crystal is used to clock the CPU, then the accused products fall outside of the claims. Because this was the factual predicate under which the trial was held and all of the evidence at trial demonstrates the PLLs in the accused products necessarily reference an off-chip signal in order to set the frequency to clock the CPU, no reasonable jury could find infringement. At bottom, the evidence was undisputed that the signal that is used to clock the CPU cannot exist but for the existence of the off chip crystal's input – there is nothing to clock the CPU if the off chip crystal is not referenced.

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[28] *See* Docket No. 585.

[29] The patentee's arguments traversing the prior art narrowed the claims. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 740 (2002) ("A patentee's decision to narrow his claims through amendment may be presumed to be a general disclaimer of the territory between the original claim and the amended claim."); *cf. Saeilo Inc. v. Colt's Mfg. Co.*, 26 F. App'x 966, 973 (Fed. Cir. 2002) ("Where an amendment narrows the scope of a claim for a reason related to the statutory requirements for patentability, prosecution history estoppel acts as a complete bar to the application of the doctrine of equivalents to the amended claim element.").

[30] *Compare* Docket No. 457 at 16 ("the oscillators in the accused products indisputably rely on an external crystal or clock generator to clock" the CPU), *with* Docket No. 470 at 14 ("Each HTC product includes a CPU/system clock – a ***ring oscillator*** within a PLL – that ***generates*** a clock signal ***on its own***, as long as it has a power supply.") (emphasis in original).

[31] Docket No. 585 at 11.

TPL counters that HTC failed to preserve the issue, and that in any event there was sufficient evidence that even if the external crystal can be used to regulate frequency clocking the CPU that is separate and distinct from the generation of the clock. TPL points to testimony from its expert, Dr. Oklobdzija, that because one could remove the crystal and still see a signal, even though that was not how the accused products operate, that suggested to him, an expert in the field, that the crystal was not being used to generate the signal.[32] Oklobdzija also opined that no off-chip crystal is relied upon to generate a clock signal.[33] Even HTC's own expert opined that the external crystal clocks were used in HTC phones as reference signals, not to actually generate the on-chip clock signal itself.[34]

As an initial matter, the court is satisfied that HTC's arguments regarding the meaning of "entire oscillator" were preserved. After the court issued its order denying HTC's motion for summary judgment of non-infringement, HTC filed a motion requesting that the court adopt a jury instruction incorporating a construction of "entire oscillator" consistent with the order. In particular, HTC asked the court to adopt a construction that included two sentences: (1) a first sentence stating that the limitation is "not satisfied by an accused system that uses any external clock to generate a signal," and (2) a second sentence specifying, among other things, that an accused product can infringe only if it "does not rely on an input control to determine its frequency."[35] The court held a hearing on HTC's motion and issued an order adopting a

[32] *See* Docket No. 641, Trial Tr. at 565:15-19 ("The ring oscillator generates the clock regardless, and it will continue to generate the clock even when you disconnect this, the crystal.").

[33] *See id.*, Trial Tr. at 565:22-25 ("Q: Does any on-chip component rely on the off-chip crystal to generate a clock signal? A: No.").

[34] *See* Docket No. 643, Trial Tr. at 1019:23-1020:3 ("Q: And have you heard of the term "Crystal Clock," or "Crystal Oscillator"? A: Yeah. Crystal Oscillator is a component that you put a voltage on the component and then it starts oscillating at a fixed frequency. It's also part of a PLL. It feeds a PLL and makes sure that the PLL has a reference signal.").

[35] Docket No. 590 at 2:19-23; *see also* Docket No. 604 (citing the intrinsic record).

construction of "entire oscillator" based on a modified version of the first sentence of HTC's proposal. The court chose not to adopt the second sentence of HTC's proposal and informed the parties that it would instruct the jury in accordance with its construction.[36]

HTC raised this issue again with the court on the day before closing arguments in the context of jury instructions on the construction of "entire oscillator." During the jury instruction conference with the court, after taking up the jury instruction on claim construction, counsel for HTC asked the court to confirm that HTC's earlier objections and arguments with respect to its proposed two-sentence construction of "entire oscillator" had been preserved for the record. The court confirmed that they were.

> Mr. Weinstein:
>
> I just want to make sure, we understand you -- we had extensive argument about the entire oscillator term. We had a hearing prior to the trial and I just wanted to make sure that the objections that we had regarding the two sentences that we wanted are still preserved.
>
> The court:
>
> They are preserved, absolutely.[37]

Second, HTC's pre-verdict JMOL motion fully raised the argument that the accused HTC products do not infringe because the oscillator in the accused HTC products relies on an input control to determine its frequency.[38] HTC's pre-verdict motion specifically argued, for example, that the "entire oscillator" limitation was not satisfied because "the output frequency of the on-chip clock is expressly calculated, in each instance, based on the input frequency provided by the external clock."[39] HTC's motion explained in detail how the frequency of the on-chip oscillator

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[36] *See* Docket No. 607 at 1.

[37] Docket No. 695-2, Ex. 16 at 1456:16-21.

[38] *See* Docket No. 647 at 4-6.

[39] *Id.* at 6.

was based on a formula that expressly relies on the frequency input from the external clock, including specific citations to the evidentiary record at trial.[40]

This was sufficient.[41]

As for the merits of the dispute, Oklobdzija took the stand and offered expert testimony that, after considering the accused products, his opinion was that the CPU was clocked by an on-chip crystal. He emphasized that a ring oscillator in an HTC accused product does not use an external crystal/clock to generate a clock signal used by the CPU. In particular, he repeatedly clarified that a ring oscillator generates a clock signal on its own, without relying on external crystals.[42] HTC's technical expert, Mr. Gafford, also admitted that it is the ring oscillator that generates the clock signal for the CPU.[43] Gafford further admits that the external crystal is not used to generate the signal. Rather, its clock is used only to compare with the phase of the ring oscillator's already generated clock signal that has been steeply divided by the frequency divider.[44] As Oklobdzija explained, the ring oscillator generates a very high frequency clock signal on its

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[40] *See id.* at 4-6.

[41] *See C.B. v. City of Sonora*, 730 F.3d 816, 824 n.5 (9th Cir. 2013) (citing *EEOC v. Go Daddy Software, Inc.*, 581 F.3d 951, 961 (9th Cir. 2009)) (In the Ninth Circuit, "Rule 50(b) 'may be satisfied by an ambiguous or inartfully made motion under Rule 50(a),' and it is given a 'liberal interpretation' to avoid overly harsh results."); *W. Union Co. v. MoneyGram Payment Sys., Inc.*, 626 F.3d 1361, 1367 (Fed. Cir. 2010) (*quoting Blackboard, Inc. v. Desire2Learn, Inc.*, 574 F.3d 1371, 1379-80 (Fed. Cir. 2009) (holding that even "a cursory motion suffices to preserve an issue on JMOL so long as it 'serves the purposes of Rule 50(a), i.e., to alert the court to the party's legal position and to put the opposing party on notice of the moving party's position as to the insufficiency of the evidence.'").

[42] *See* Docket No. 641, Trial Tr. at 565:15-19 ("The ring oscillator generates the clock regardless, and it will continue to generate the clock even when you disconnect this, this crystal."); Trial Tr. 565:22-25 ("Q: Does any on-chip component rely on the off-chip crystal to generate a clock signal? A: No.").

[43] *See* Docket No. 684, Trial Tr. at 1364:18-22 ("Q: So you've got a 2.0 gigahertz clock signal generated by the ring oscillator that's clocking the CPU, and you divide by 100, and that's what this circuitry actually does; correct? A: Yes.").

[44] *See id.*, Trial Tr. at 1364:18-1365:1 ("Q: [The 2.0-gigahertz clock signal generated by the ring oscillator is divided by 100] [t]o get a 20 megahertz signal so that you can do edge matching with the external reference crystal signal in the phase detector, correct? A: Yes.").

own, which must then be divided to obtain a lower frequency so that its phase can be compared to the phase of the external reference.[45] After that, the PLL can make adjustments to the analog voltage/current provided to the ring oscillator to regulate – but not to generate – its frequency.[46]

Even if Oklobdzija's positions were later undermined by other evidence to a degree or diminished through cross-examination, his expert testimony as corroborated by other experts provides sufficient substantial evidence as required under Rule 50(b).

B. The Jury Considered Substantial Evidence of Variation of the Processing Frequency and Entire Oscillator as a Function of PVT

HTC next argues that no reasonable jury could have found infringement because TPL did not provide substantial evidence that the processing frequency of the CPU and entire oscillator "varied as a function of process, voltage, or temperature." In support, HTC claims the accused products "are designed to maintain the target frequency across PVT variations."[47] What's more, none "of the formulae for any Qualcomm, TI or Samsung chip recites any fabrication or operational parameter variation as playing any role in the determination of the PLL output

[45] *See* Docket No. 641, Trial Tr. at 569:2-18 ("Q: Where is the digital to analog converter here? A: It says DAC. DAC means digital to analog converter, the component here (indicating). So this output operation to extend the digital signal to DAC, this DAC just makes the plain voltage out (indicating), this voltage which comes from here (indicating), and produces this voltage which will smoothly move this one in the range we want it to oscillate (indicating). Now, let me go back just one second. This is a divider (indicating), and this is a comparator (indicating). This is what is called a phase detector (indicating). Here is the reference (indicating). This reference is compared with the divided signal here, and what it does is, you can see the switches, it either moves this voltage up or down. These capacitors have been charged and they filter that voltage so it's not jumping up and down, so it's smooth, that voltage, okay, when connected.").

[46] *See id.* at 569:19-22 ("And in this case this is disconnected, but when connected, it's converted into a current some with what digital PLL does, or digital output, same thing, voltage, and it will adjust this VCO, voltage control oscillator, ring oscillator.").

[47] Docket No. 643, Trial Tr. at 1062:2-3 ("Regarding PLL's, I can tell you that PLL's are designed to maintain the target frequency across PVT variations."); Docket No. 640, Trial Tr. at 359:2-8 ("Q: Is the output frequency from the DPLL stable? A: That is part of the specification. In other words, the outer clock is always known to have a known value within a tight range. That's how the specification on the PLL is developed. So yes, the answer is correct, it's stable, it's a known value.").

frequency. The accused HTC products, therefore, do not meet the "varying" limitations as a matter of law."[48]

Again, the court finds substantial evidence supports the jury's verdict. Gafford, HTC's expert, testified that the processing frequency of the CPU and the clock rate of the on-chip oscillator must always vary in the same way.[49] Because the claim limitation is disjunctive, TPL needed to show only that such variation is a function of at least one parameter among the several fabrication or operational parameters (e.g., voltage and temperature). With respect to at least the process / fabrication parameters, TPL met its burden. Process parameters vary from chip to chip because, as Gafford testified, process parameters are the same for components of the same chip, such as the CPU and the on-chip oscillator in each HTC accused product.[50] Gafford also admitted that such process variation between chips results in variation between chips in processing frequency and the associated clock rate.[51]

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[48] Docket No. 671 at 8.

[49] *See* Docket No. 684, Trial Tr. at 1387:13-1388:1 ("Q: Let me ask you this: the processing frequency of the CPU and the clock rate of the entire oscillator must always vary together; right? A: Yes, they must vary in the same way. Q: They all – they must always vary in the same way, and the reason is that the CPU gets its processing frequency from the clock rate of the entire oscillator; right? A: I believe that's the way—I believe that's how everyone has agreed we're interpreting this element. Q: Okay. Like Dr. Oklobdzija's analogy, if I'm the entire oscillator and you're the CPU and we're shaking hands and I'm moving my hand at two hertz, your hand is also moving at two hertz; correct?

[50] *See id.*, Trial Tr. at 1394:8-11 ("Q: Now, Variations in fabrication parameters, again, are from chip to chip. They're not in the same chip during operation; right? A: Yes."); Trial Tr. at 1393:16-23 ("Q: Now, you also recognized that there have to be process variations among the chips in the HTC accused products; right? A: Yes. Q: Because process variation is endemic to silicon production; correct? A: Yes. Q: You can't get away from it; right? A: Yes.)".

[51] *See id.*, Trial Tr. at 1390:2-11 ("Q: But when we're talking about fabrication variations, those are variations from chip to chip; right? A: Yes. Q: So some chips will have the ability to run faster and some chips will only be able to run at slower speeds; right? A: That's right. Q: And that's why we have a binning step in manufacturing chips; correct? A: As to its effect on the CPU speed, yes, that is what binning does."); Trial Tr. at 1394:8-11 ("Q: Now, Variations in fabrication parameters, again, are from chip to chip. They're not in the same chip during operation; right? A: Yes.").

Evidence of process variation, and therefore processing frequency and clock rate variation, between chips, was shown in all HTC accused products. Qualcomm's representative, Sina Dena, testified, for example, that for the same chip design, Qualcomm separates chips with higher clock speeds at the "high end" or "fast corner of the process," from chips with lower clock speeds at the "slower corner of the process" -- a practice called binning.[52] Qualcomm assigns different product names or designations to chips in different bins even though they have the "same design."[53] In fact, "the higher speed bin products will have potentially a different frequency plan."[54] Qualcomm charges more for such chips.[55] Gafford confirmed that "there have to be process variations among

[52] *See* Docket No. 643, Trial Tr. at 1083:5-14 ("The court: The next question has to do with binning. We've heard much discussion in this trial about binning. When you were describing binning earlier during your testimony, were you referring to binning of a single or common IC design? The witness: Yes. Basically it's – it's – it's the same design which performs, can take higher clock speeds at the high end of the process, at the fast corner of the process and versus, you know, lower clock speed at the slower corner of the process.")

[53] *See id.*, Trial Tr. at 1083:5-14 ("The court: The next question has to do with binning. We've heard much discussion in this trial about binning. When you were describing binning earlier during your testimony, were you referring to binning of a single or common IC design? The witness: Yes. Basically it's – it's – it's the same design which performs, can take higher clock speeds at the high end of the process, at the fast corner of the process and versus, you know, lower clock speed at the slower corner of the process."); Trial Tr. at 1064:14-24 ("Q: Okay. Understood so you change the PLL based on the speed bin that the chip goes in; right? A: Right. And the chips usually are going to have a different identification when they are at the higher speed versus the one that – Q: And I think you called these premium chips, the faster ones, right? A: I don't know if it's premium, but the marketing group. Q: But you're able to charge more money for those chips; right? A: Yes."); 1083:22-23 ("Now, usually when the binning is done, either product name is changed or there is some sort of designation that goes.").

[54] *See id.*, Trial Tr. at 1083:22-1084:5. ("Now, usually when the binning is done, either product name is changed or there is some sort of designation that goes. So it's -- even though you might call it the same design, the higher speed bin products will have potentially a different frequency plan, and it's very simple to manage with a single release of software that we do for these chips. Basically the software reads the fuse space, finds it, okay, this is a faster device, so I'm going to change my PLL plan to a different setting for this particular device.").

[55] *See id.*, Trial Tr. at 1064:10-24 ("A: Now, is there a market for 1.2 Gigahertz? Sure, there is if you do that. So we have a premium for the fast corner process devices, and then the frequency plan, the PLL plan is going to change for that particular group of devices. Q: Okay. Understood so you change the PLL based on the speed bin that the chip goes in; right? A: Right. And the chips usually are going to have a different identification when they are at the higher speed versus the one that – Q: And I think you called these premium chips, the faster ones, right? A: I don't know if it's premium, but the marketing group. Q: But you're able to charge more money for those chips; right? A: Yes.").

the chips in the HTC accused products," "because process variation is endemic to silicon production."[56]

As to the formulae cited by HTC, they merely show how the ring oscillator uses the external crystal clock as a reference, not how the ring oscillator actually generates the clock signal. HTC's own witness, Mr. Fichter, testified that the external crystal clock in the HTC phones serves merely as a reference signal.[57] Dena confirmed that this crystal functions as a reference for the Qualcomm chips used in the HTC phones.[58] Dr. Haroun, a corporate representative from Texas Instruments, also confirmed that the external crystal clock functions as a reference for the TI chips used in the HTC phones.[59] Because the external crystal serves merely as a reference, if that crystal

[56] *See* Docket No. 684, Trial Tr. at 1393:16-23 ("Q: Now, you also recognized that there have to be process variations among the chips in the HTC accused products; right? A: Yes. Q: Because process variation is endemic to silicon production; correct? A: Yes. Q: You can't get away from it; right? A: Yes.)".

[57] *See* Docket No. 643, Trial Tr. at 1019:23-1020:3 ("Q: And have you heard of the term "Crystal Clock," or "Crystal Oscillator"? A: Yeah. Crystal Oscillator is a component that you put a voltage on the component and then it starts oscillating at a fixed frequency. It's also part of a PLL. It feeds a PLL and makes sure that the PLL has a reference signal.").

[58] *See id.*, Trial Tr. at 1044:2-12 ("Q: And at a high level, what is the purpose of a phase lock loop? A: Phase lock loop is used to provide a fixed target frequency clock signal. Q: And generally how is that achieved? A: In the Qualcomm family of chips, basically there's a fixed reference input clock that comes to a box, phase lock loop. There are elements that go into it, we call them L, M, N, different parameters, and the output frequency of the phase lock loop would be a mathematical formula of those elements multiplied by the input reference clock frequency."), Trial Tr. at 1048:10-15 ("Q: Okay. Now, one more last question about this. This TCXO right here, is that a -- what type of signal is that (indicating)? A: It's what you call a reference clock signal fixed at 19.2 and it's extremely important for PLL operation for this signal to be fixed across variation and temperatures (indicating).").

[59] Docket No. 640, Trial Tr. at 350:14-17 ("Q: Now, all of the – now, all of the OMAP chips use PLL's with -- that have a reference signal from an external clock; correct? A: That is correct."). In fact, Dr. Haroun admitted that only the ring oscillator in the TI chips could create or generate the high frequency used to clock the CPU. *Id.* at Trial Tr. at 353:23-354:3 ("Q: Okay. Let me clarify it this way: there's no other portion in the PLL besides the ring osciallator that can create a frequency that's so much higher than the external crystal; correct? A: That is correct. That is where it's -- where the extra edges are generated, yes.").

is disconnected, the ring oscillator will still be able to generate a clock signal.[60] HTC's focus on the formulae therefore ignores the fact that differently binned chips – even if they have the same design – are set to run at different frequencies and sold for different prices.

In sum, substantial evidence supports the jury's infringement verdict.

IT IS SO ORDERED.

Dated: January 21, 2014

PAUL S. GREWAL
United States Magistrate Judge

[60] *See* Docket No. 641, Trial Tr. at 567:8-22 ("Q: So the ring oscillator will still run if you disconnect the crystal? A: Yes, because crystal is not essential to generate the clock. Crystal is not needed to generate the clock.")

United States District Court
For the Northern District of California

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, et al., Defendants.	Case No. 5:08-cv-00882-PSG **ORDER GRANTING-IN-PART HTC'S MOTION TO CORRECT THE JUDGMENT** **(Re: Docket No. 674)**

Both HTC and TPL agree that the court needs to modify the judgment as it currently stands to incorporate the court's prior order dismissing the '890 patent from this case.[1] Where the parties disagree is what form the modified judgment should take. TPL suggests the court hew closely to the present language of the judgment to which both parties previously agreed.[2] HTC believes it

[1] *See* Docket Nos. 674 and 690.

[2] *See* Docket No. 690 at 3 ("pursuant to the Court's Order dismissing U.S. Patent No. 5,530,890 (the "'890 patent") entered September 19, 2013 (Dkt. No. 594), judgment with respect to the '890 patent is entered as follows:

a) Because Defendants cannot establish entitlement to damages in the present action based on the Court's Summary Judgment Order (issued on September 17, 2013 (Dkt. No. 585)), the Court on September 19, 2013 DISMISSED the Fifth Claim for Relief in HTC's First Amended Complaint (seeking a declaration that HTC does not infringe any valid and enforceable claim of the '890 patent), and Count IV of Defendants' Answer and Counterclaim (alleging infringement of the '890 patent), subject to the conditions of the September 19, 2013 Order (Dkt. No. 594);

would be appropriate to go further by describing the dismissal of the '890 patent as entering judgment in its favor.[3]

The court agrees with TPL that moving well beyond the terms of the court's prior order would be unwarranted in this case. The prior order dismissed the '890 patent because HTC prevailed on its motion for partial summary judgment and was able to avoid a portion of TPL's infringement claims and the potential for money damages. But if the claim had proceeded to trial, broader relief to HTC was available. In particular, HTC may have invalidated the patent altogether. Under such circumstances, language characterizing the dismissal of the'890 patent as a complete victory in favor of HTC is not warranted.

b) The September 19, 2013 Order (id.) shall not affect any other claim or counterclaim asserted in the present action, and shall not impair any rights of Defendants or HTC to challenge on appeal any pretrial ruling by the Court for which an appeal is permissible including, without limitation, any challenge to the Summary Judgment Order's application of the intervening rights doctrine;

c) In the event the Federal Circuit reverses the Summary Judgment Order with respect to application of the intervening rights doctrine to the '890 patent, HTC's declaratory judgment claim and Defendants' counterclaim under the '890 patent will be reinstated and proceed unaffected by the dismissal provided in the September 19, 2013 Order (Dkt. No. 594).).

[3] Docket No. 674 at 3 ("**IT IS FURTHER ORDERED AND ADJUDGED** that pursuant to the Joint Request To Dismiss All Claims Relating to U.S. Patent No. 5,530,890 Under F.R.C.P. 41(a)(2) (Dkt. No. 594), the provisions of which are incorporated herein by reference, judgment is hereby entered in favor of Plaintiffs on Defendants' claim of infringement of U.S. Patent No. 5,530,890.").

In any event, the court finds some modification of the language from the proposed order in this case is warranted. The court adopts the following language:

Pursuant to the court's order dismissing U.S. Patent No. 5,530,890 ("the '890 patent") entered September 19, 2013 (Docket No. 594), judgment with respect to the '890 patent is entered as follows:

a) Because Defendants cannot establish entitlement to damages in the present action based on the court's summary judgment order (issued on September 17, 2013 (Docket No. 585)), the court on September 19, 2013 DISMISSED the Fifth Claim for Relief in HTC's First Amended Complaint (seeking a declaration that HTC does not infringe any valid and enforceable claim of the '890 patent), and Count IV of Defendants' Answer and Counterclaim (alleging infringement of the '890 patent), subject to the conditions of the September 19, 2013 order (Docket No. 594);

b) The September 19, 2013 order (Docket No. 594) shall not affect any other claim or counterclaim asserted in the present action, and shall not impair any rights of Defendants or HTC to challenge on appeal any pretrial ruling by the court for which an appeal is permissible including, without limitation, any challenge to the summary judgment order's application of the intervening rights doctrine;

c) In the event the Federal Circuit reverses the summary judgment order with respect to application of the intervening rights doctrine to the '890 patent, HTC's declaratory judgment claim and Defendants' counterclaim under the '890 patent will be reinstated and proceed unaffected by the dismissal provided in the September 19, 2013 order (Docket No. 594).

A revised judgment consistent with this order will issue.

IT IS SO ORDERED.

Dated: January 21, 2014

PAUL S. GREWAL
United States Magistrate Judge

United States District Court
For the Northern District of California

United States District Court
For the Northern District of California

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, et al., Defendants.	Case No. 5:08-cv-00882-PSG **ORDER MODIFYING JUDGMENT** **(Re: Docket No. 674)**

(X) Jury Verdict. This action came before the court for a trial by jury. The issues have been tried and the jury has rendered its verdict.

IT IS SO ORDERED AND ADJUDGED that pursuant to the jury verdict filed October 3, 2013, judgment is entered in favor of Defendants.

IT IS FURTHER ORDERED pursuant to the court's order dismissing U.S. Patent No. 5,530,890 ("the '890 patent") entered September 19, 2013 (Docket No. 594), judgment with respect to the '890 patent is entered as follows:

a) Because Defendants cannot establish entitlement to damages in the present action based on the court's summary judgment order (issued on September 17, 2013 (Docket No. 585)), the court on September 19, 2013 DISMISSED the Fifth Claim for Relief in HTC's First Amended Complaint (seeking a declaration that HTC does not infringe any valid and enforceable claim of the '890 patent), and Count IV of Defendants' Answer and

Counterclaim (alleging infringement of the '890 patent), subject to the conditions of the September 19, 2013 order (Docket No. 594);

b) The September 19, 2013 order (Docket No. 594) shall not affect any other claim or counterclaim asserted in the present action, and shall not impair any rights of Defendants or HTC to challenge on appeal any pretrial ruling by the court for which an appeal is permissible including, without limitation, any challenge to the summary judgment order's application of the intervening rights doctrine;

c) In the event the Federal Circuit reverses the summary judgment order with respect to application of the intervening rights doctrine to the '890 patent, HTC's declaratory judgment claim and Defendants' counterclaim under the '890 patent will be reinstated and proceed unaffected by the dismissal provided in the September 19, 2013 order (Docket No. 594).

IT IS SO ORDERED.

Dated: January 21, 2014

PAUL S. GREWAL
United States Magistrate Judge

US005809336A

United States Patent [19]

Moore et al.

[11] Patent Number: 5,809,336

[45] Date of Patent: Sep. 15, 1998

[54] **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

[75] Inventors: **Charles H. Moore**, Woodside; **Russell H. Fish, III**, Mt. View, both of Calif.

[73] Assignee: **Patriot Scientific Corporation**, San Diego, Calif.

[21] Appl. No.: **484,918**

[22] Filed: **Jun. 7, 1995**

Related U.S. Application Data

[62] Division of Ser. No. 389,334, Aug. 3, 1989, Pat. No. 5,440,749.

[51] **Int. Cl.**[6] **G06F 1/04**

[52] **U.S. Cl.** **395/845**

[58] **Field of Search** 395/500, 551, 395/555, 845

[56] **References Cited**

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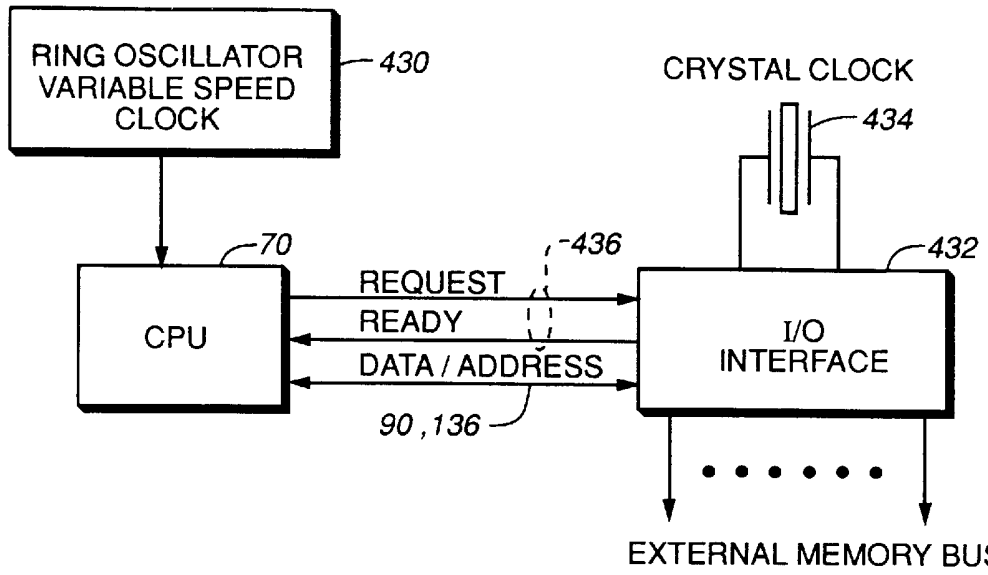
Primary Examiner—David Y. Eng

Attorney, Agent, or Firm—Cooley Godward LLP

[57] **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.

10 Claims, 19 Drawing Sheets



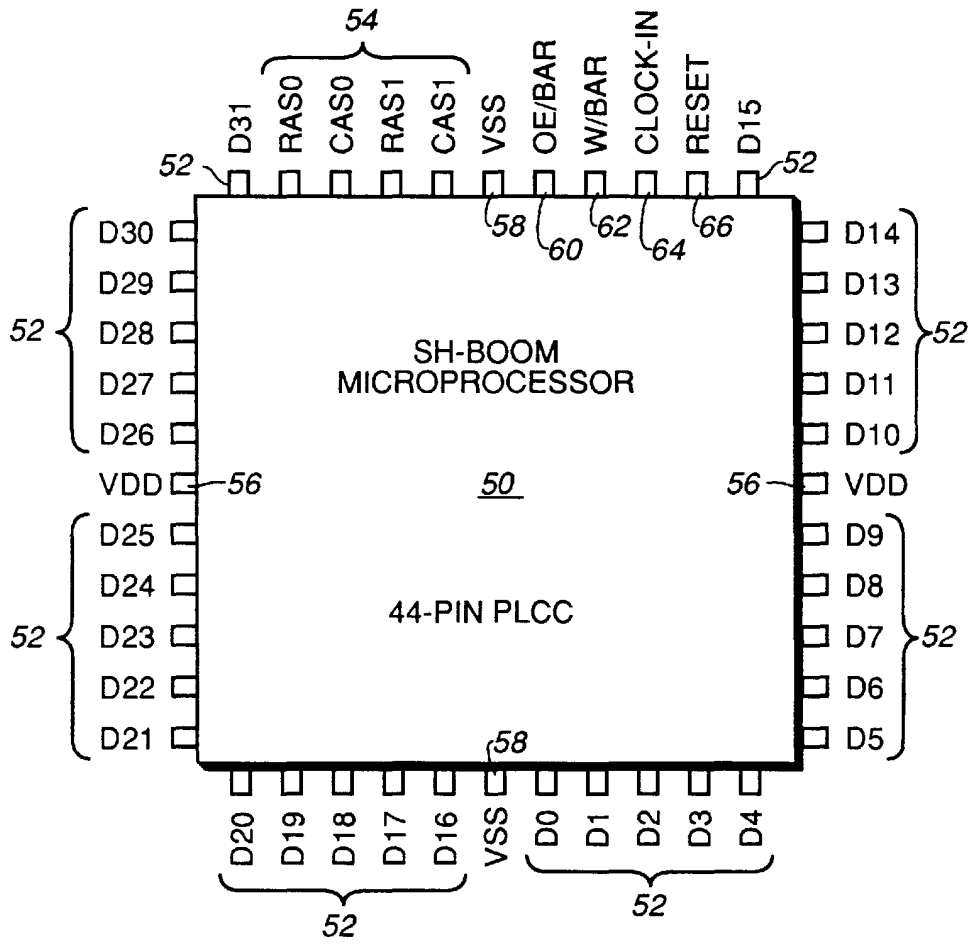

54
D31
RAS0
CAS0
RAS1
CAS1
VSS
OE/BAR
W/BAR
CLOCK-IN
RESET
D15
52
58
60
62
64
66
D30
D29
D28
D27
D26
VDD
D25
D24
D23
D22
D21
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
56
SH-BOOM
MICROPROCESSOR
50
44-PIN PLCC
D20
D19
D18
D17
D16
D0
D1
D2
D3
D4

FIG._1

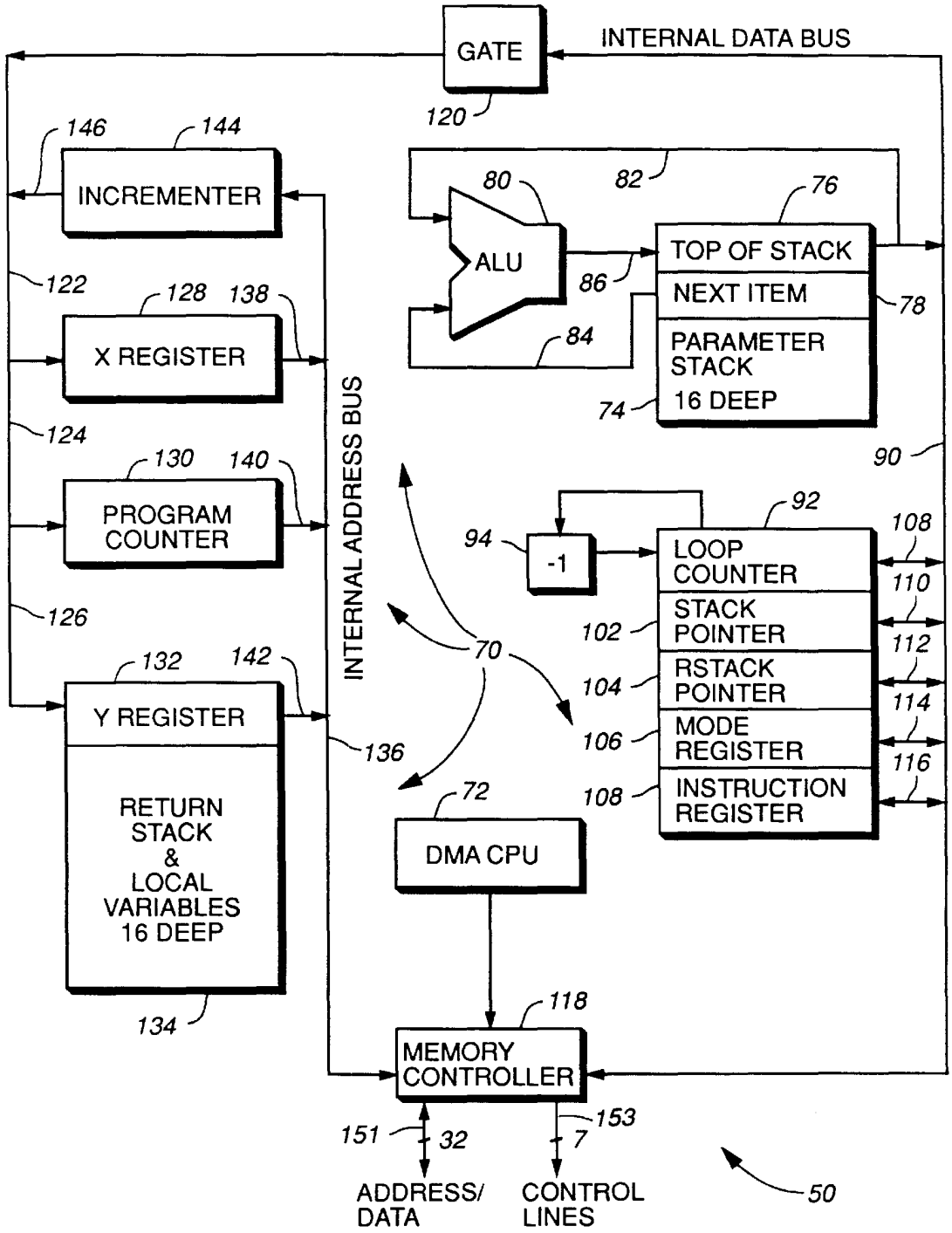

GATE
INTERNAL DATA BUS
120
146
144
INCREMENTER
80
82
76
ALU
TOP OF STACK
NEXT ITEM
PARAMETER STACK
16 DEEP
78
86
84
74
122
128
138
X REGISTER
124
130
140
PROGRAM COUNTER
126
INTERNAL ADDRESS BUS
90
92
94
-1
LOOP COUNTER
STACK POINTER
RSTACK POINTER
MODE REGISTER
INSTRUCTION REGISTER
108
110
112
114
116
102
104
106
108
70
132
142
Y REGISTER
136
RETURN STACK & LOCAL VARIABLES 16 DEEP
134
72
DMA CPU
118
MEMORY CONTROLLER
151
32
153
7
ADDRESS/ DATA
CONTROL LINES
50

FIG._2

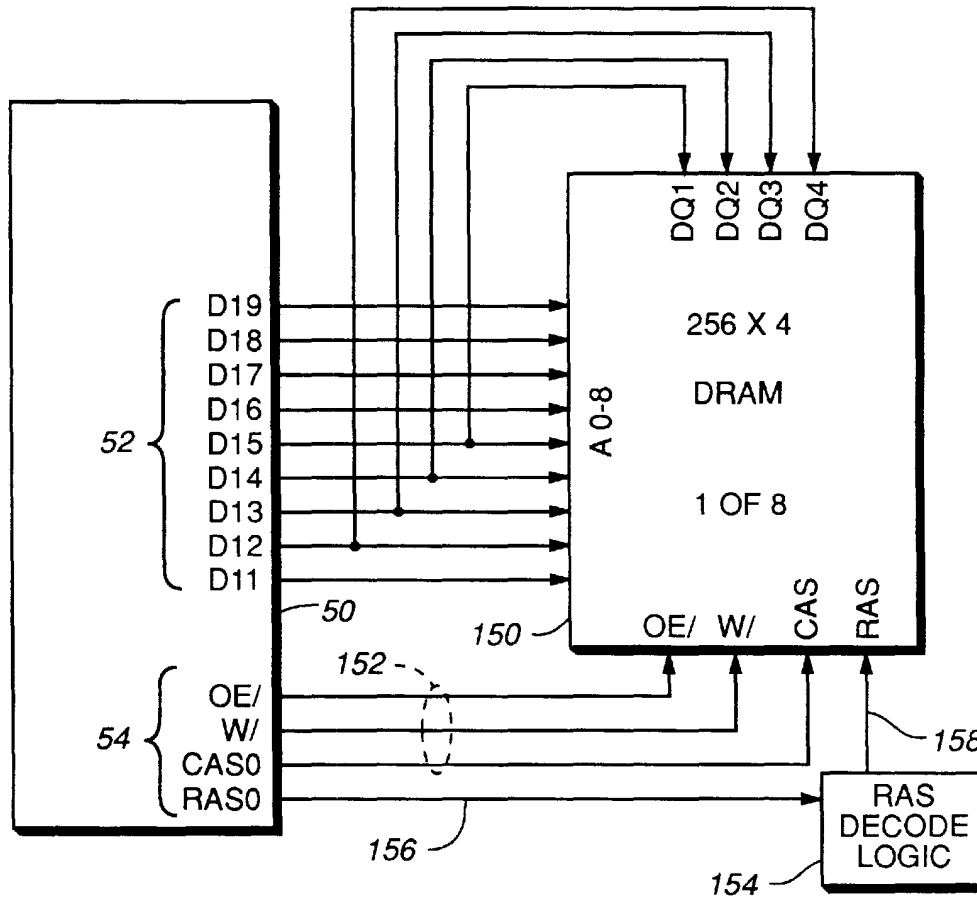

DQ1
DQ2
DQ3
DQ4
256 X 4
DRAM
1 OF 8
A 0-8
OE/
W/
CAS
RAS
D19
D18
D17
D16
D15
D14
D13
D12
D11
52
50
150
152
54
OE/
W/
CAS0
RAS0
156
158
RAS
DECODE
LOGIC
154

FIG._3

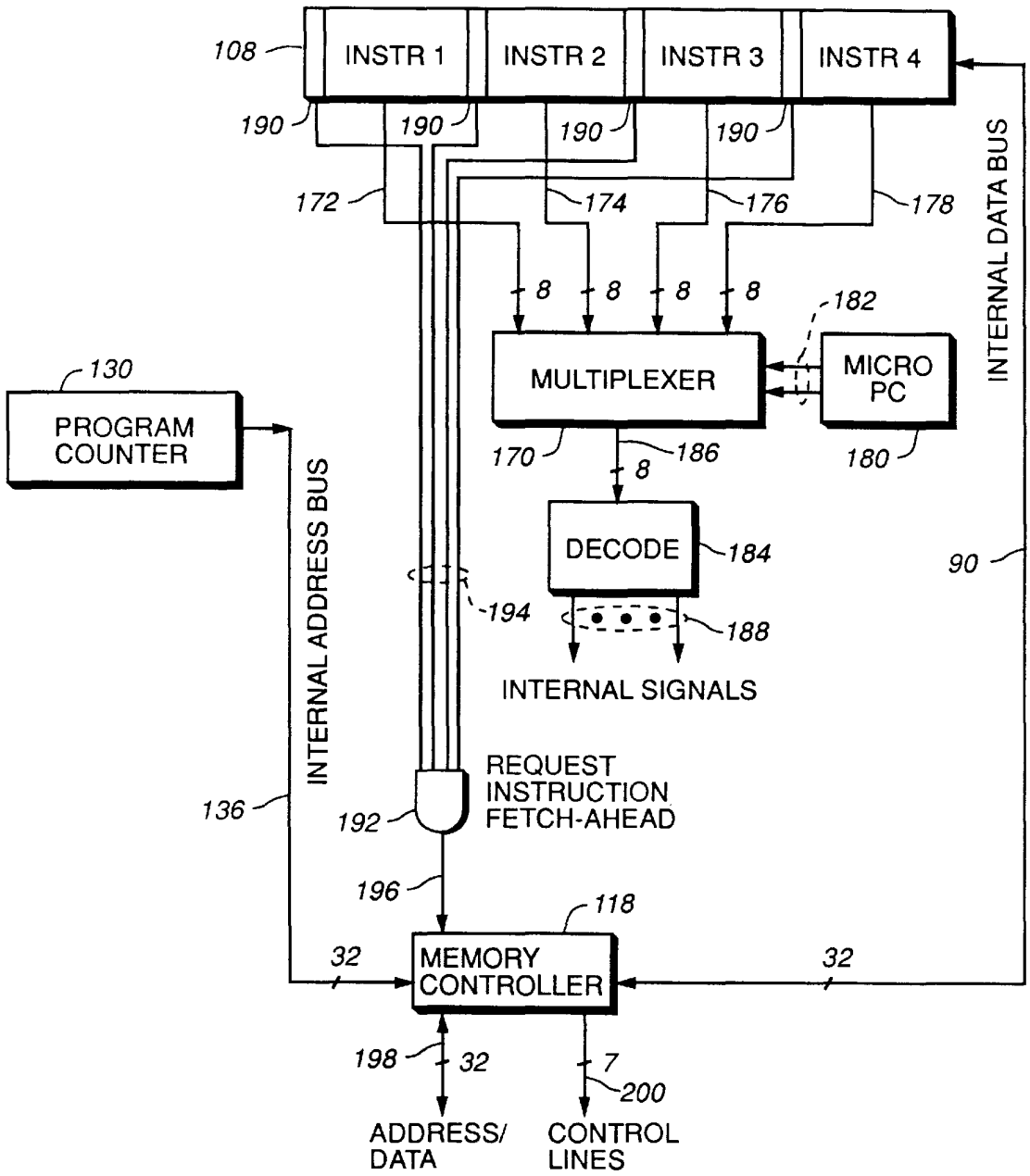

108
INSTR 1
INSTR 2
INSTR 3
INSTR 4
190
190
190
190
172
174
176
178
8
8
8
8
182
MULTIPLEXER
MICRO PC
INTERNAL DATA BUS
130
PROGRAM COUNTER
170
186
180
8
DECODE
184
90
194
188
INTERNAL SIGNALS
INTERNAL ADDRESS BUS
REQUEST INSTRUCTION FETCH-AHEAD
136
192
196
118
32
MEMORY CONTROLLER
32
198
32
7
200
ADDRESS/ DATA
CONTROL LINES

FIG._4

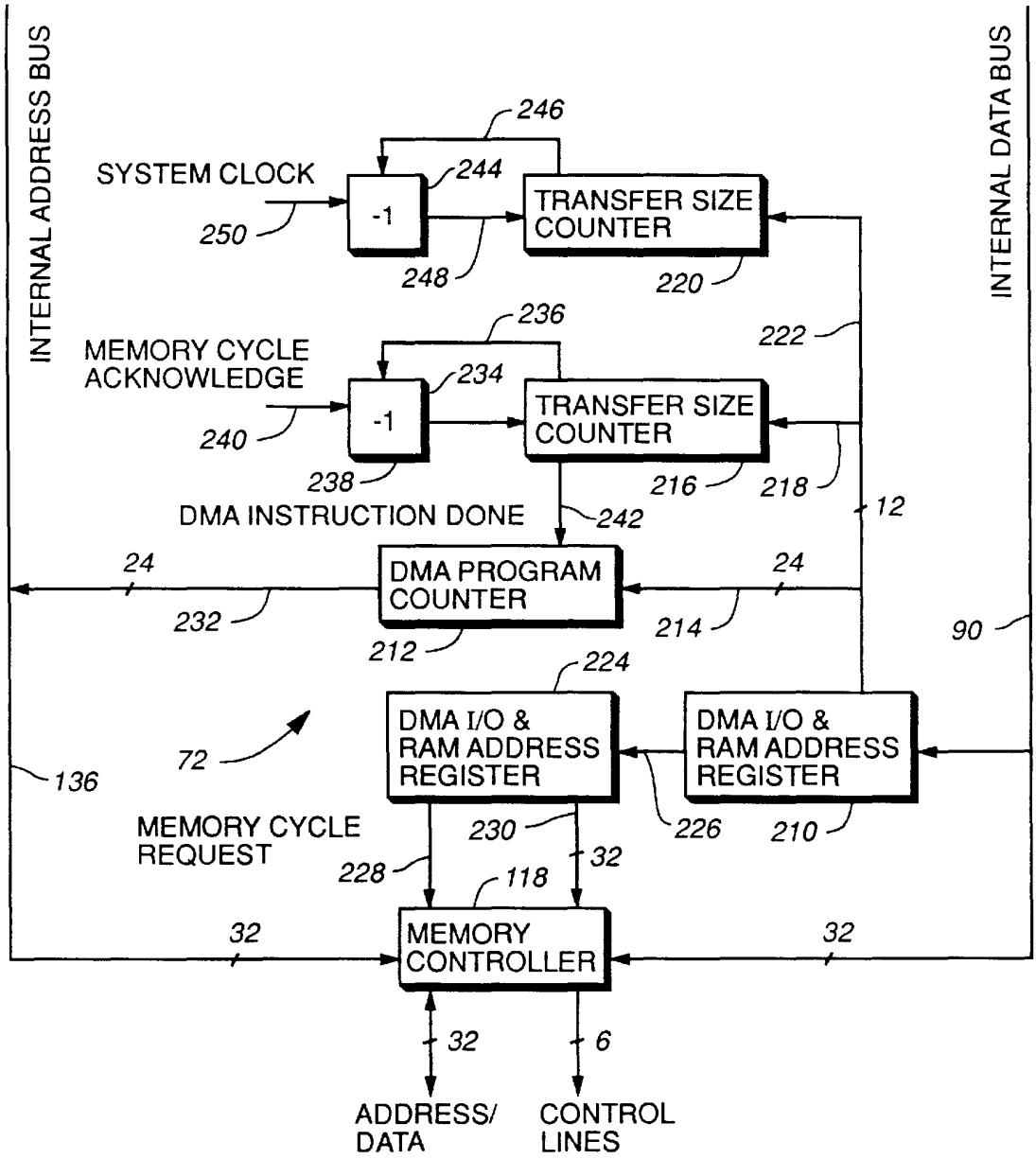

INTERNAL ADDRESS BUS
INTERNAL DATA BUS
SYSTEM CLOCK
246
244
250
-1
TRANSFER SIZE COUNTER
248
220
236
MEMORY CYCLE ACKNOWLEDGE
234
240
-1
TRANSFER SIZE COUNTER
238
216
218
222
12
DMA INSTRUCTION DONE
242
24
DMA PROGRAM COUNTER
24
232
214
212
90
224
DMA I/O & RAM ADDRESS REGISTER
DMA I/O & RAM ADDRESS REGISTER
72
136
MEMORY CYCLE REQUEST
230
226
210
228
32
118
32
MEMORY CONTROLLER
32
32
6
ADDRESS/ DATA
CONTROL LINES

FIG._5

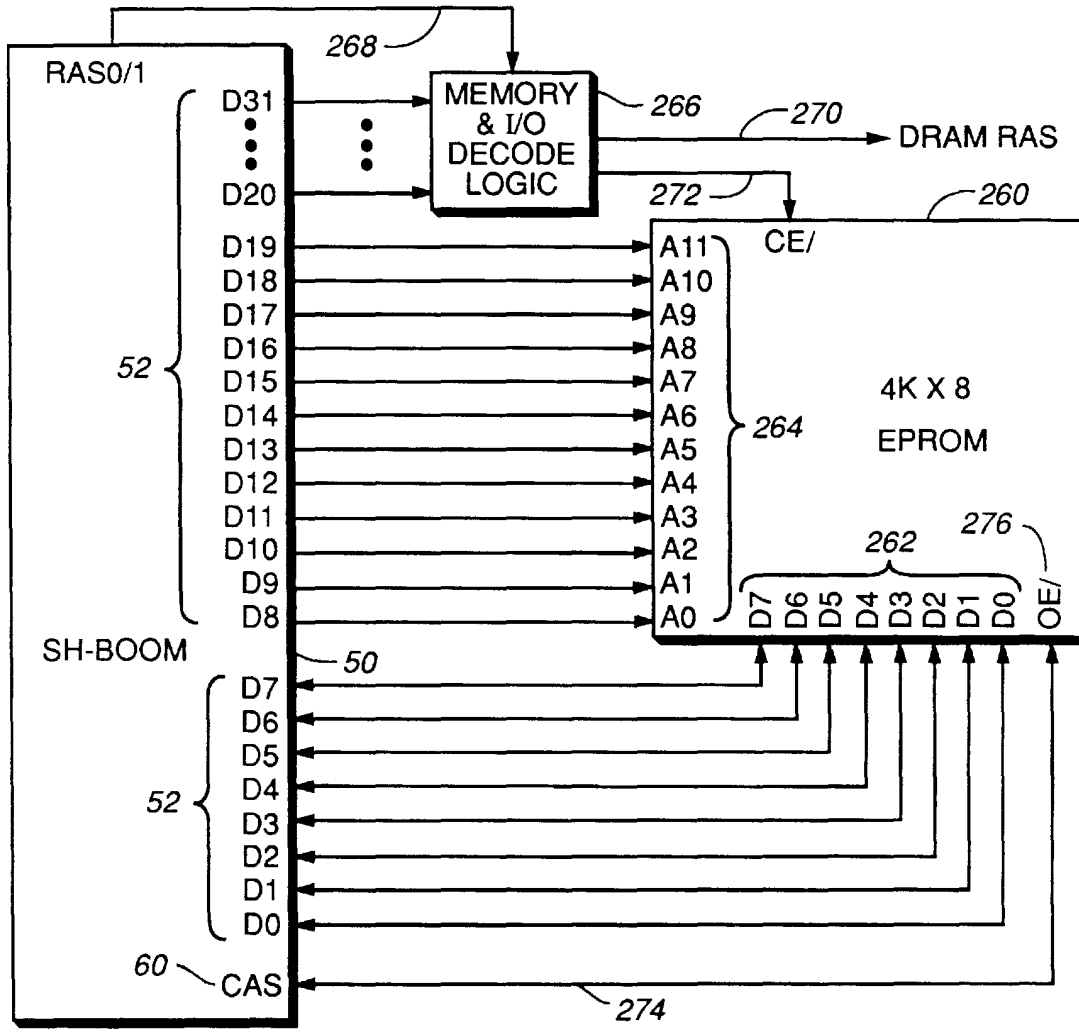

RAS0/1
D31
D20
D19
D18
D17
D16
D15
D14
D13
D12
D11
D10
D9
D8
52
SH-BOOM
50
D7
D6
D5
D4
D3
D2
D1
D0
52
60
CAS
268
MEMORY & I/O DECODE LOGIC
266
270
DRAM RAS
272
260
CE/
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
264
4K X 8
EPROM
262
276
D7
D6
D5
D4
D3
D2
D1
D0
OE/
274

FIG._6

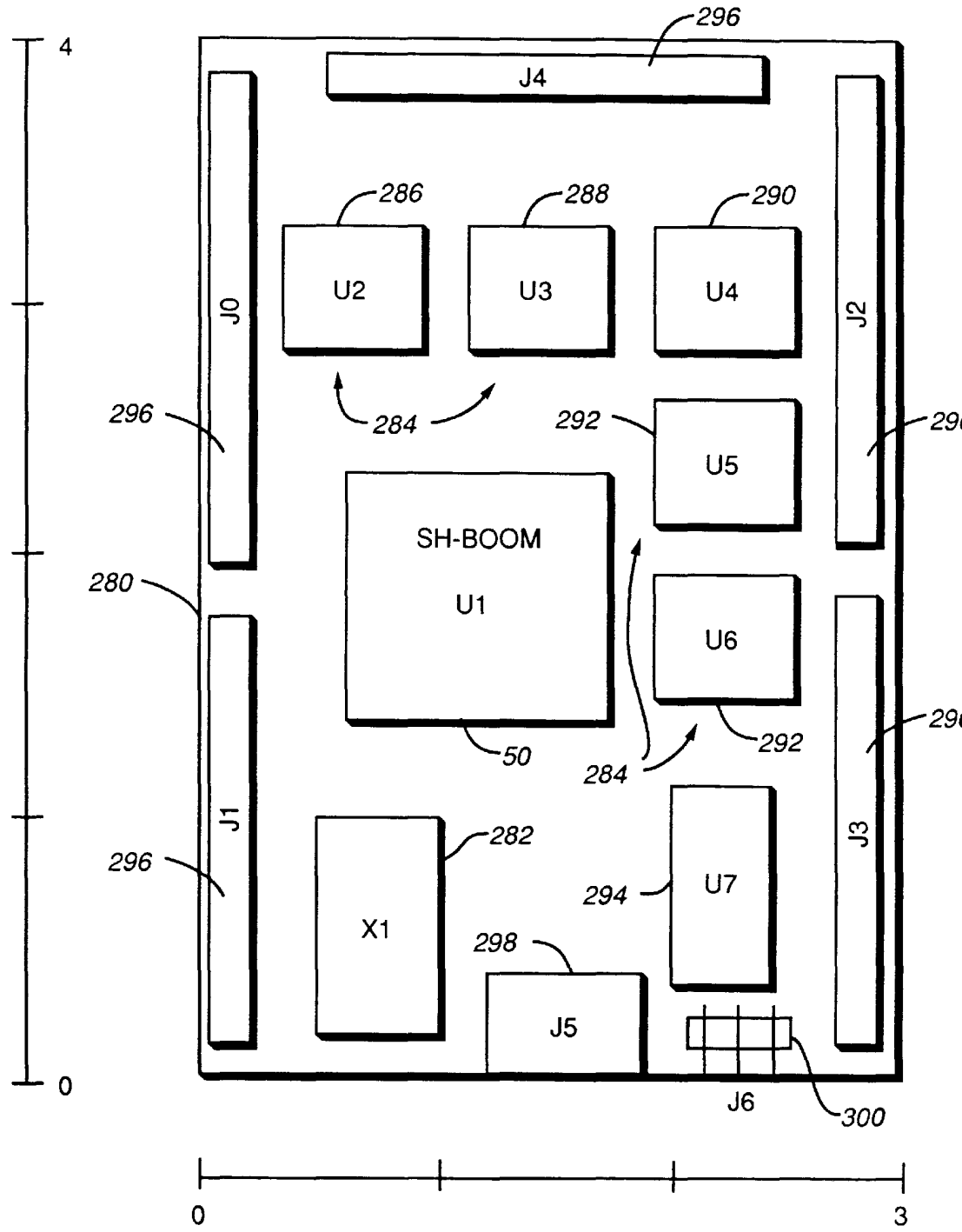

296
J4
286
288
290
U2
U3
U4
J0
J2
284
296
292
296
U5
SH-BOOM
U1
280
U6
296
50
292
284
J1
J3
296
282
294
U7
X1
298
J5
J6
300
4
0
0
3

FIG._7

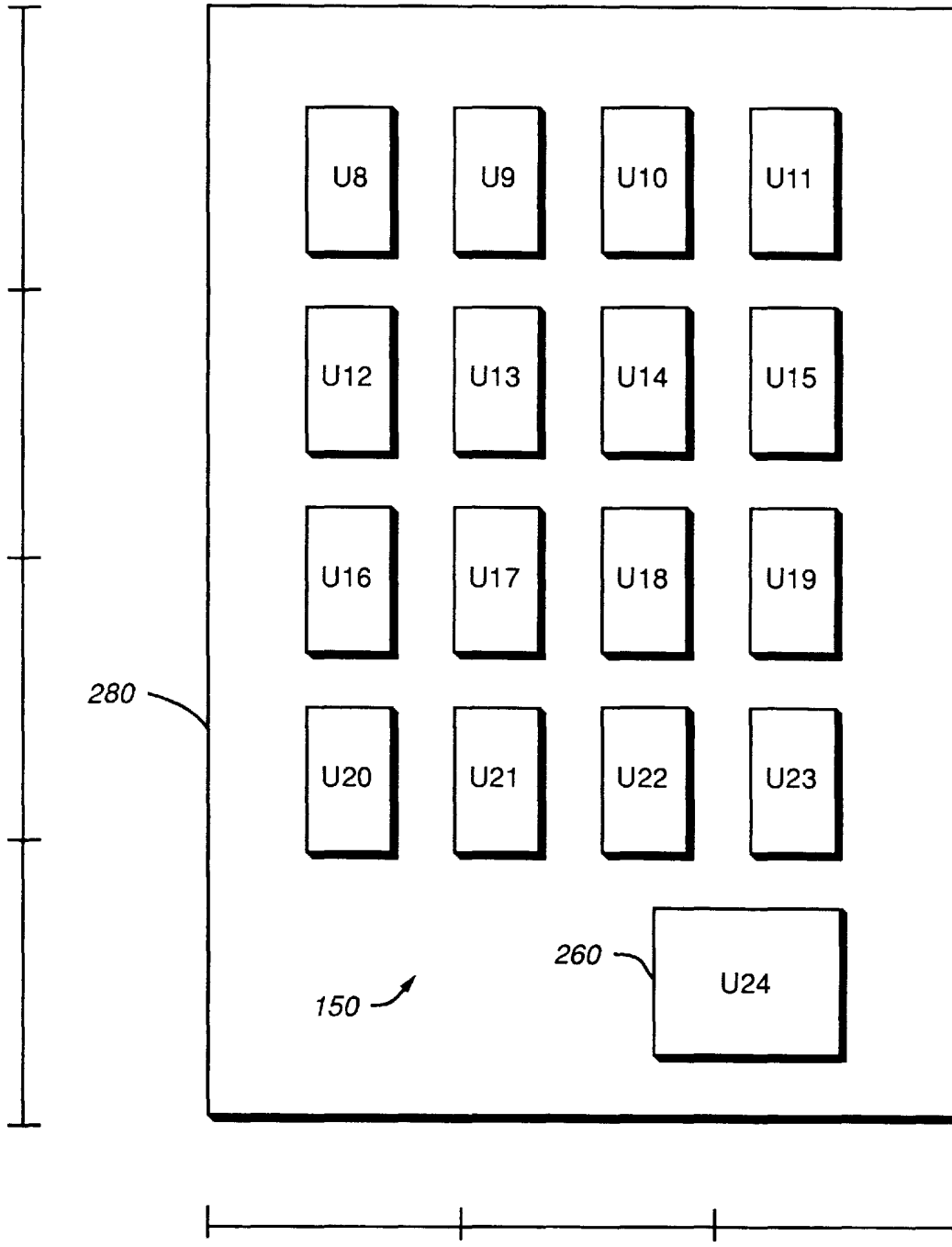

U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
280
260
150

FIG._8

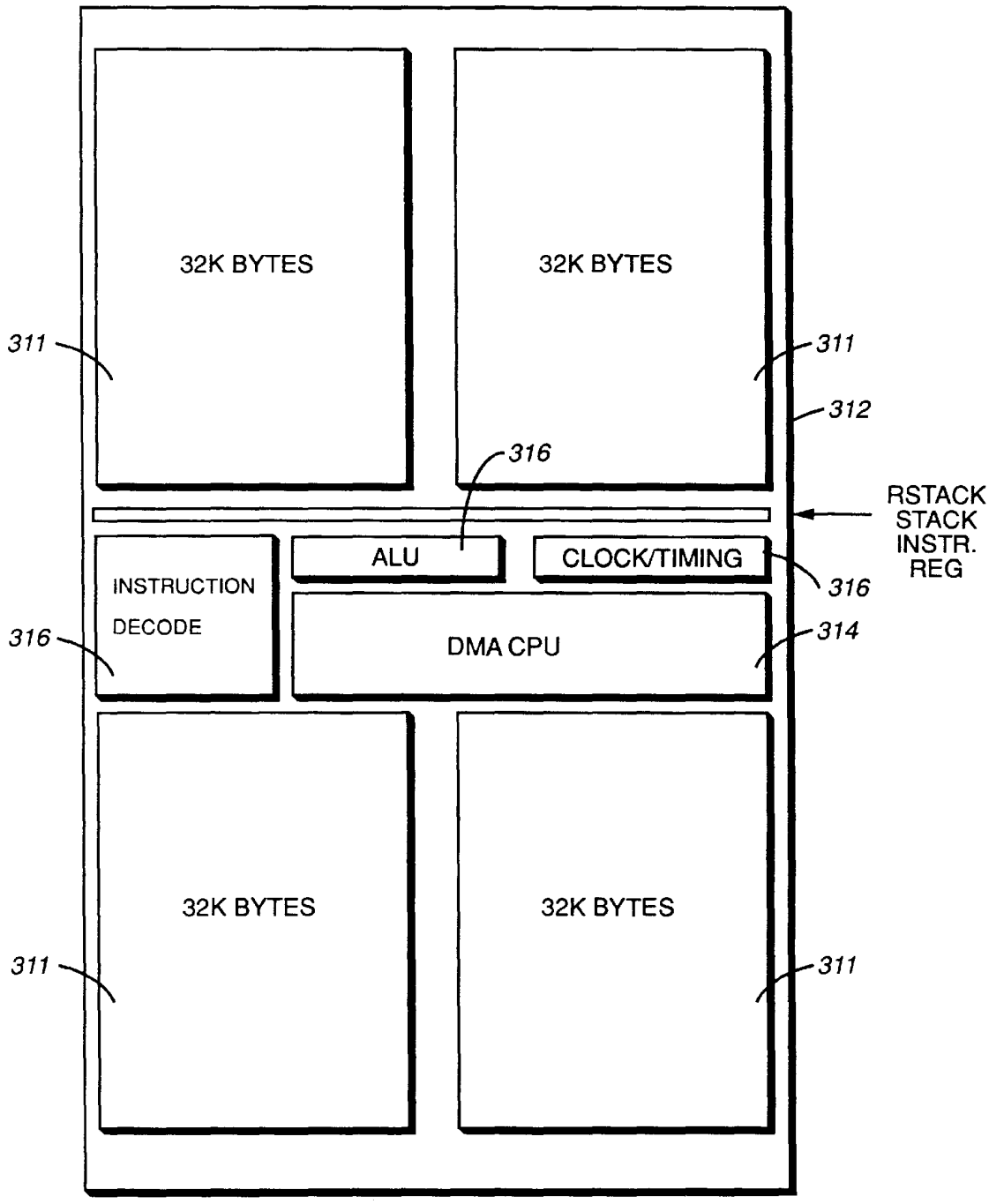

32K BYTES
32K BYTES
311
311
312
316
RSTACK
STACK
INSTR.
REG
ALU
CLOCK/TIMING
316
INSTRUCTION
DECODE
316
DMA CPU
314
32K BYTES
32K BYTES
311
311

FIG._9

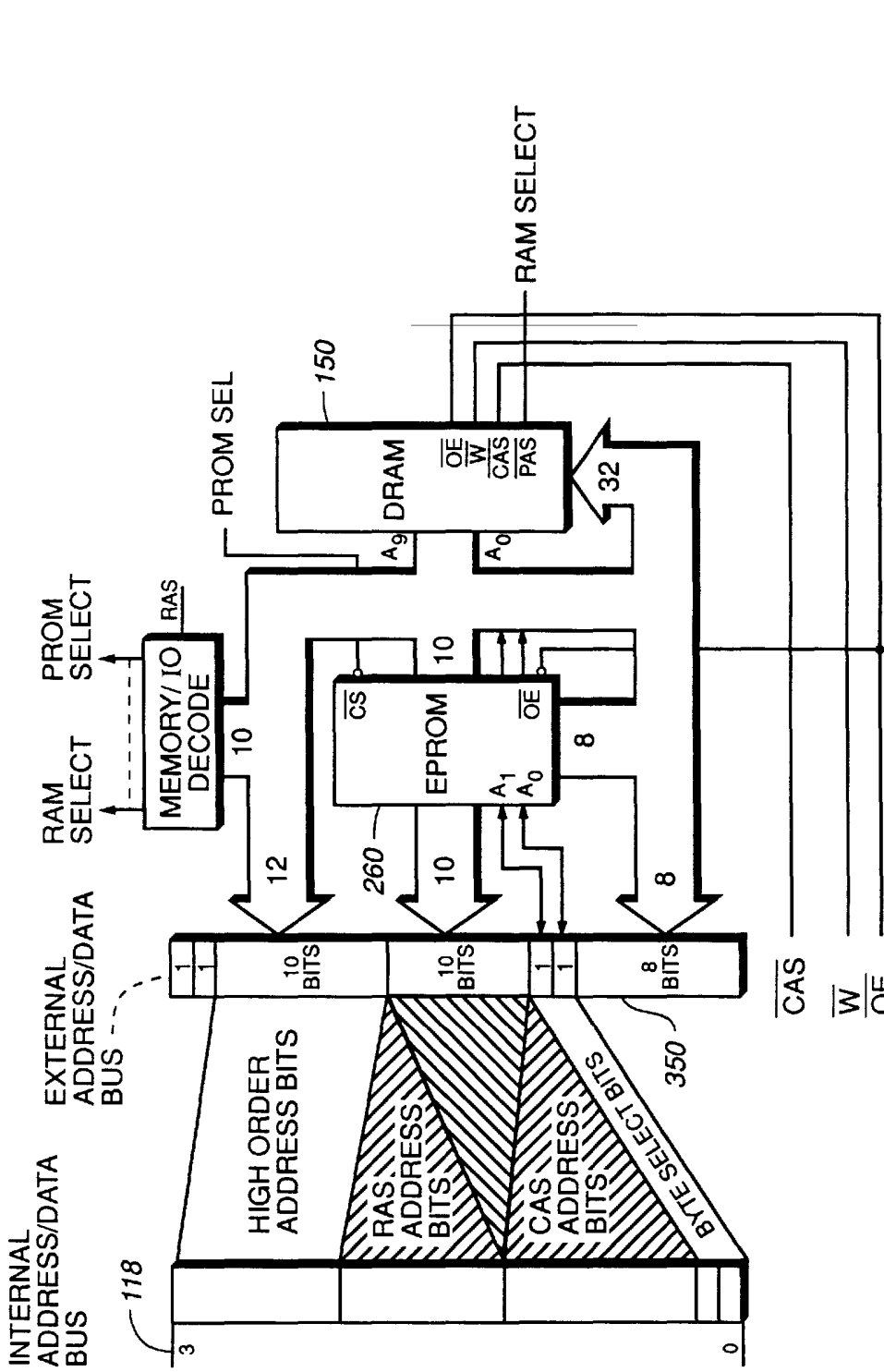
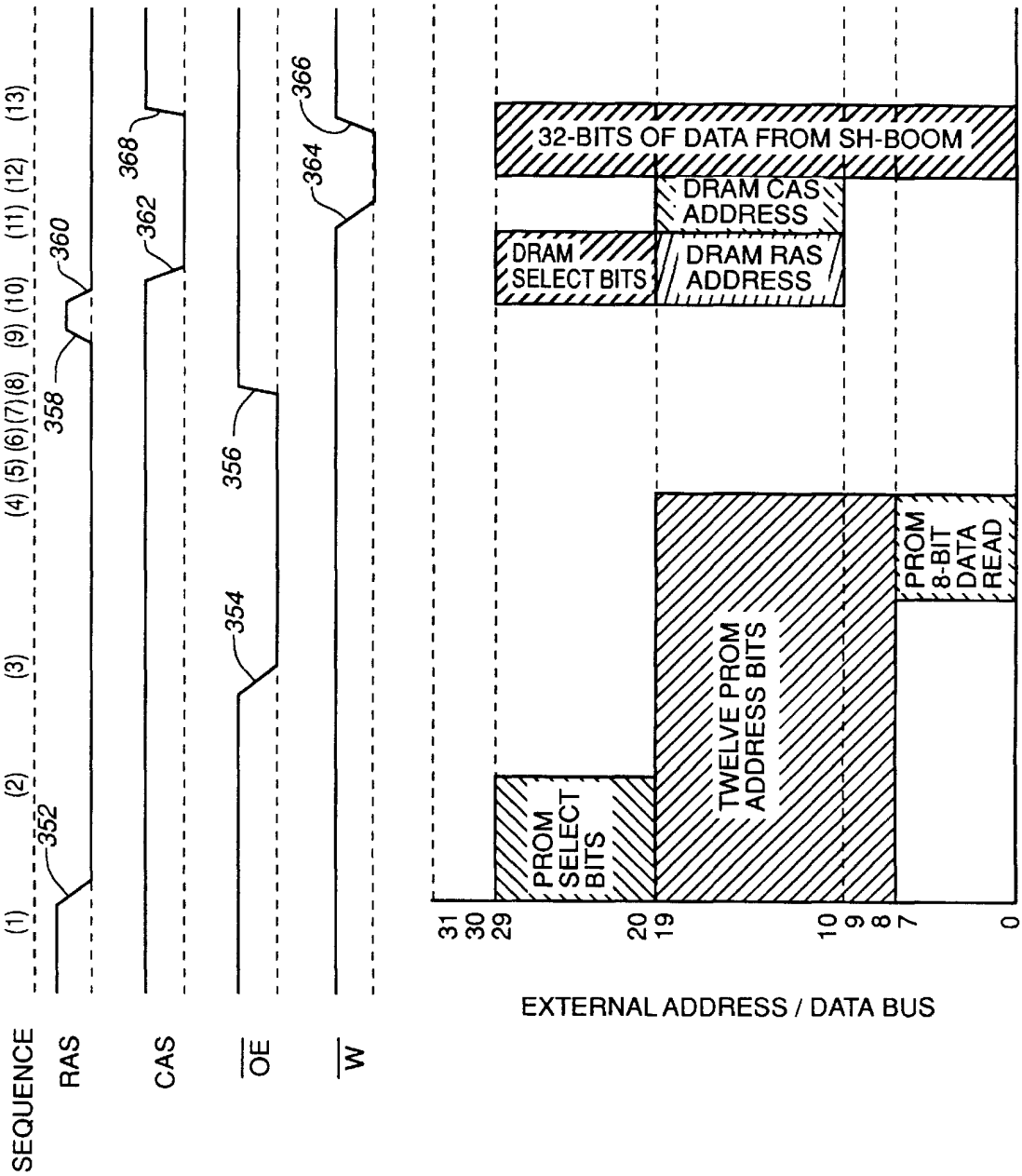

RAM SELECT
150
PROM SEL
DRAM
OE
W
CAS
RAS
32
A9
A0
PROM SELECT
RAS
MEMORY/IO DECODE
10
RAM SELECT
CS
EPROM
OE
10
8
A1
A0
260
12
10
8
EXTERNAL ADDRESS/DATA BUS
1
1
10 BITS
10 BITS
1
1
8 BITS
CAS
W
OE
350
HIGH ORDER ADDRESS BITS
RAS ADDRESS BITS
CAS ADDRESS BITS
BYTE SELECT BITS
INTERNAL ADDRESS/DATA BUS
118
3
0

FIG._10

FIG._11


SEQUENCE
RAS
CAS
OE
W
(1)
(2)
(3)
(4) (5) (6) (7) (8)
(9) (10)
(11) (12)
(13)
352
354
356
358
360
362
364
366
368
32-BITS OF DATA FROM SH-BOOM
DRAM CAS ADDRESS
DRAM SELECT BITS
DRAM RAS ADDRESS
PROM SELECT BITS
TWELVE PROM ADDRESS BITS
PROM 8-BIT DATA READ
31 30 29 20 19 10 9 8 7 0
EXTERNAL ADDRESS / DATA BUS

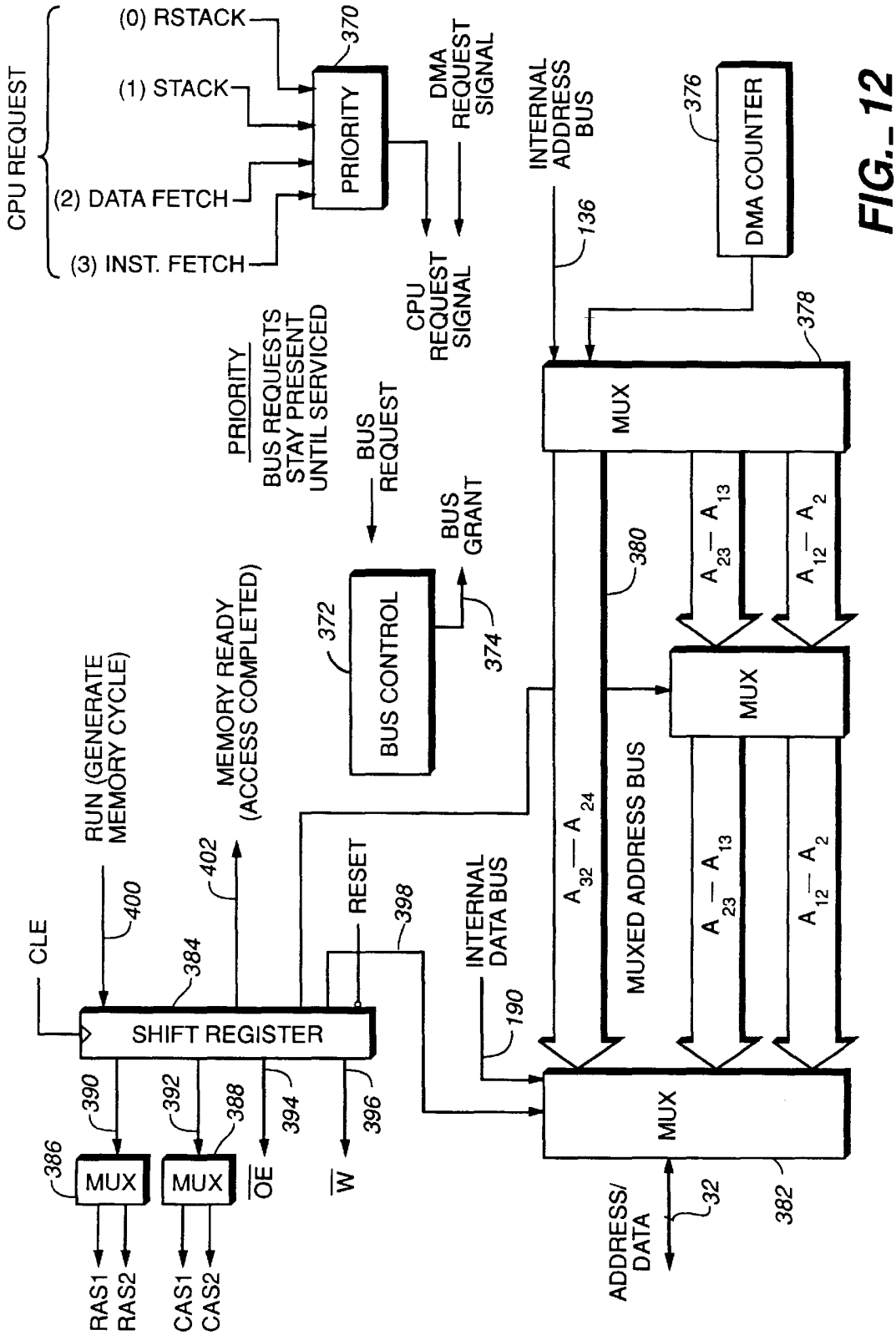

CPU REQUEST
(0) RSTACK
(1) STACK
(2) DATA FETCH
(3) INST. FETCH
370
PRIORITY
DMA REQUEST SIGNAL
CPU REQUEST SIGNAL
INTERNAL ADDRESS BUS
136
376
DMA COUNTER
PRIORITY
BUS REQUESTS STAY PRESENT UNTIL SERVICED
BUS REQUEST
BUS GRANT
372
BUS CONTROL
374
378
MUX
380
A23 — A13
A12 — A2
MUX
MEMORY READY (ACCESS COMPLETED)
RUN (GENERATE MEMORY CYCLE)
400
402
RESET
398
CLE
384
SHIFT REGISTER
INTERNAL DATA BUS
190
A32 — A24
MUXED ADDRESS BUS
A23 — A13
A12 — A2
MUX
390
392
388
394
396
386
MUX
MUX
OE
W
RAS1
RAS2
CAS1
CAS2
ADDRESS/ DATA
32
382

FIG._12

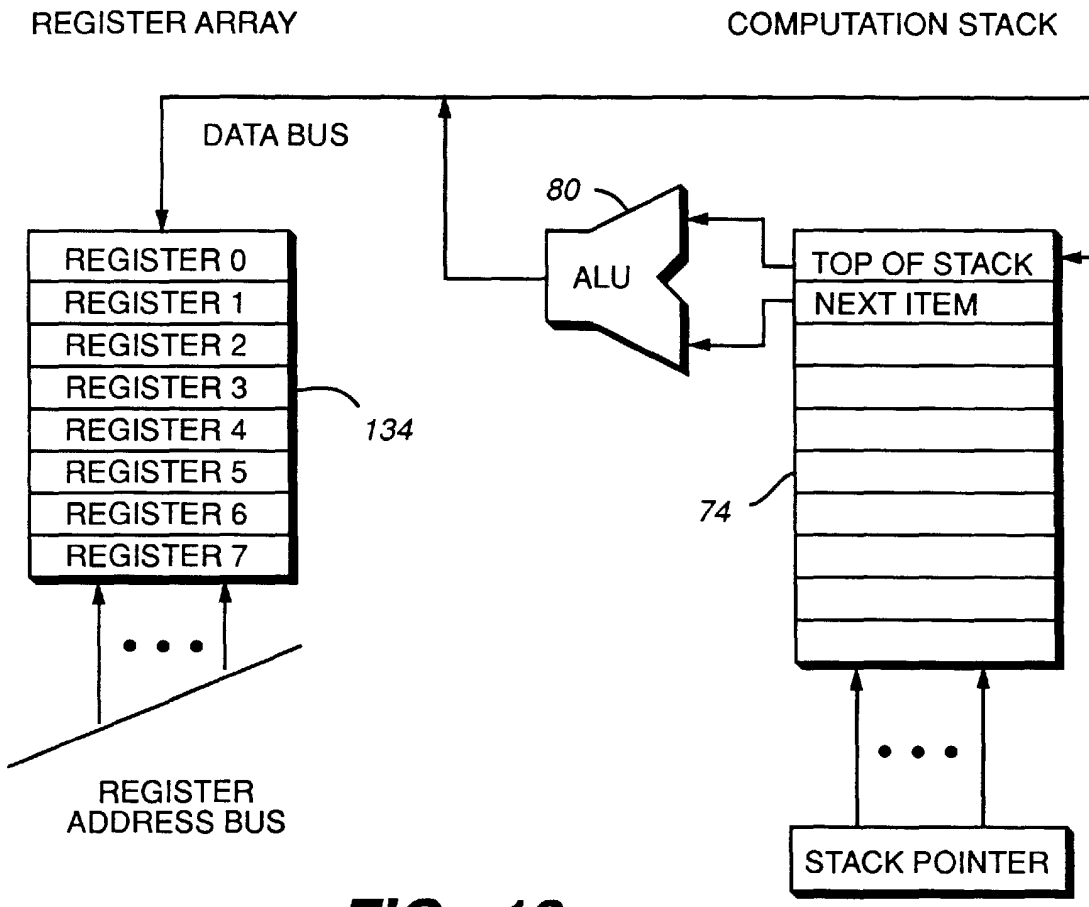

REGISTER ARRAY
COMPUTATION STACK
DATA BUS
80
ALU
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
REGISTER 7
134
TOP OF STACK
NEXT ITEM
74
REGISTER
ADDRESS BUS
STACK POINTER

FIG._13

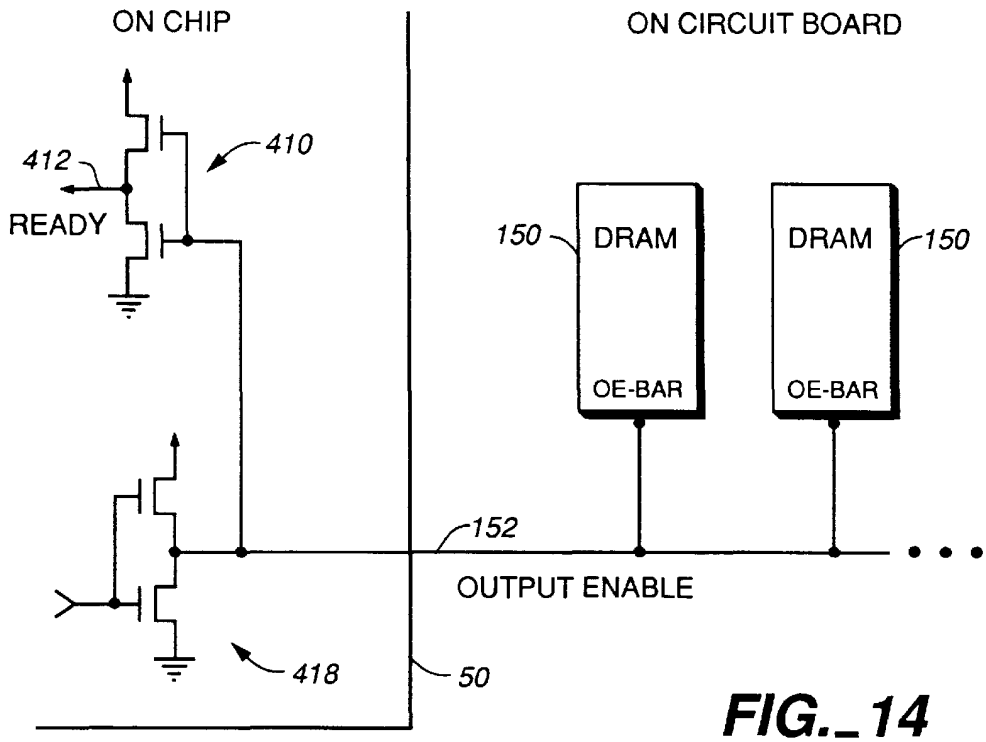

ON CHIP
ON CIRCUIT BOARD
412
410
READY
150
DRAM
DRAM
150
OE-BAR
OE-BAR
152
OUTPUT ENABLE
418
50

FIG._14

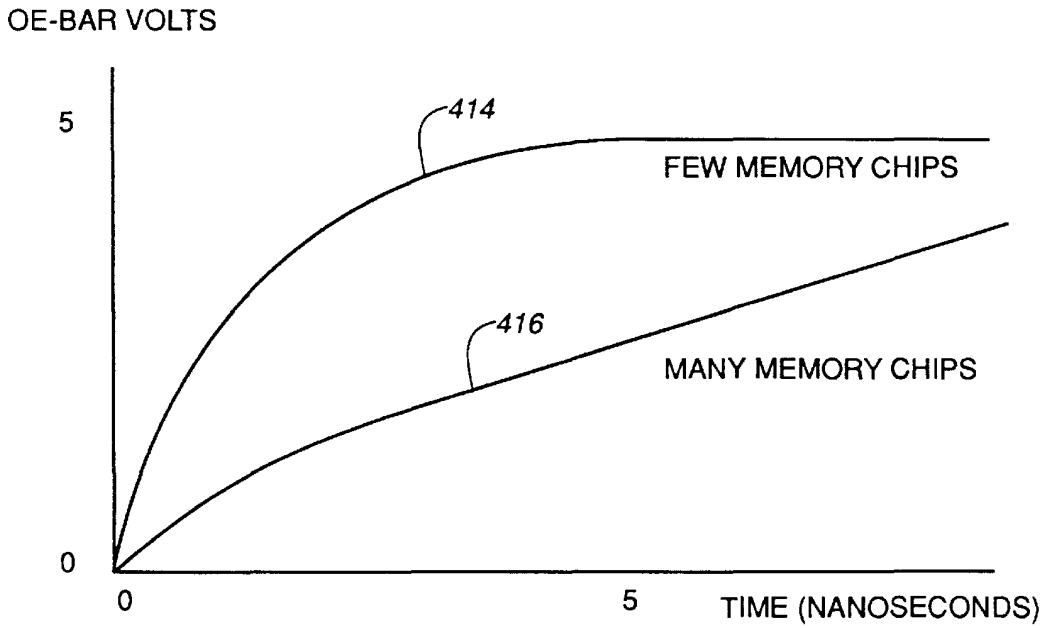

OE-BAR VOLTS
5
414
FEW MEMORY CHIPS
416
MANY MEMORY CHIPS
0
0
5
TIME (NANOSECONDS)

FIG._15

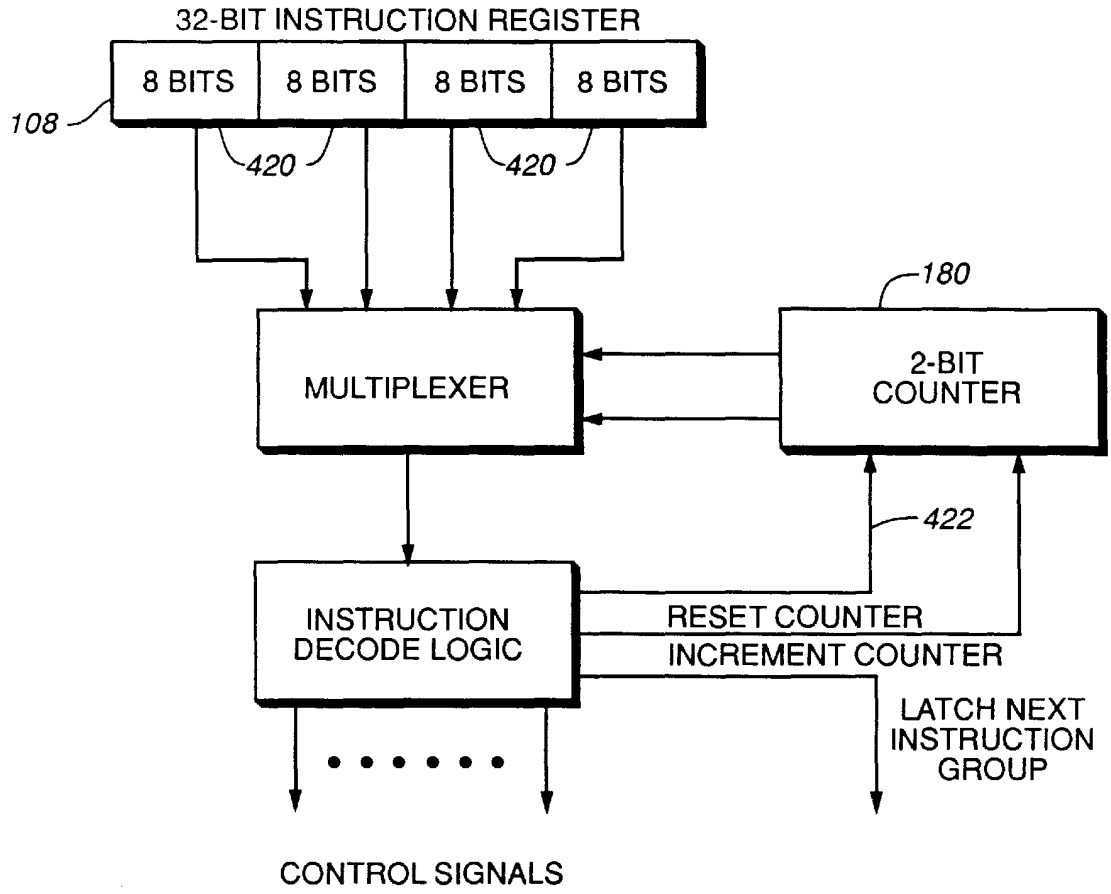

32-BIT INSTRUCTION REGISTER
8 BITS
8 BITS
8 BITS
8 BITS
108
420
420
180
MULTIPLEXER
2-BIT COUNTER
422
INSTRUCTION DECODE LOGIC
RESET COUNTER
INCREMENT COUNTER
LATCH NEXT INSTRUCTION GROUP
CONTROL SIGNALS

FIG._16

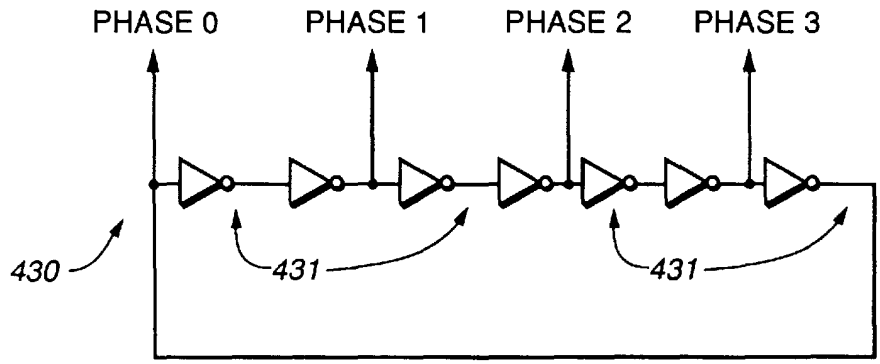

PHASE 0
PHASE 1
PHASE 2
PHASE 3
430
431
431

FIG._18

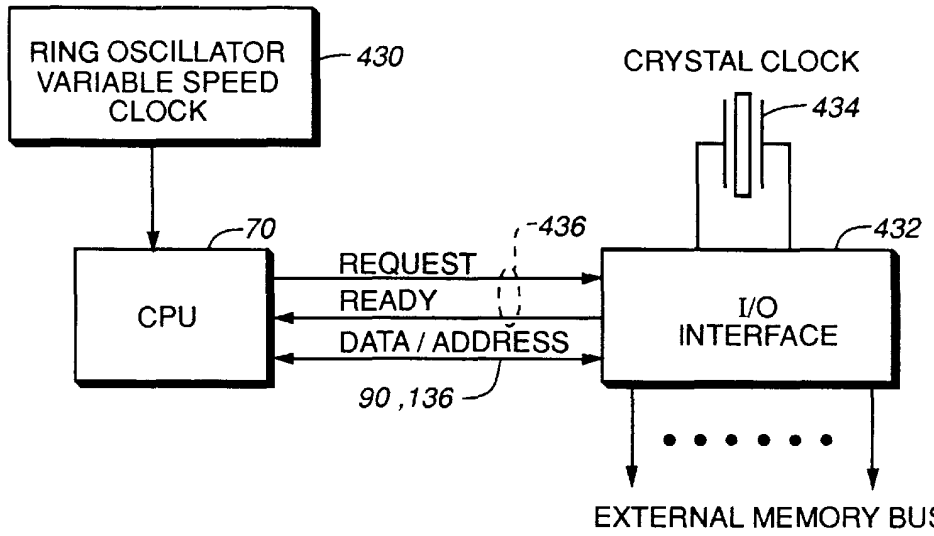

RING OSCILLATOR
VARIABLE SPEED
CLOCK
430
CRYSTAL CLOCK
434
70
436
432
CPU
REQUEST
READY
DATA / ADDRESS
I/O
INTERFACE
90 ,136
EXTERNAL MEMORY BUS

FIG._17

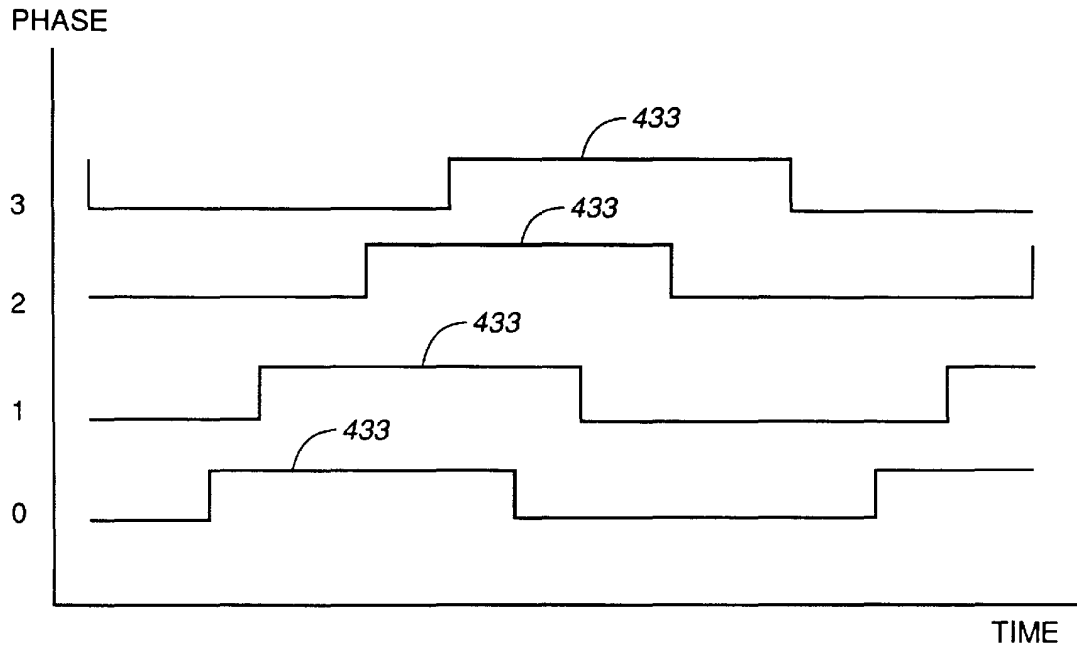

PHASE
3
2
1
0
433
433
433
433
TIME

FIG._19

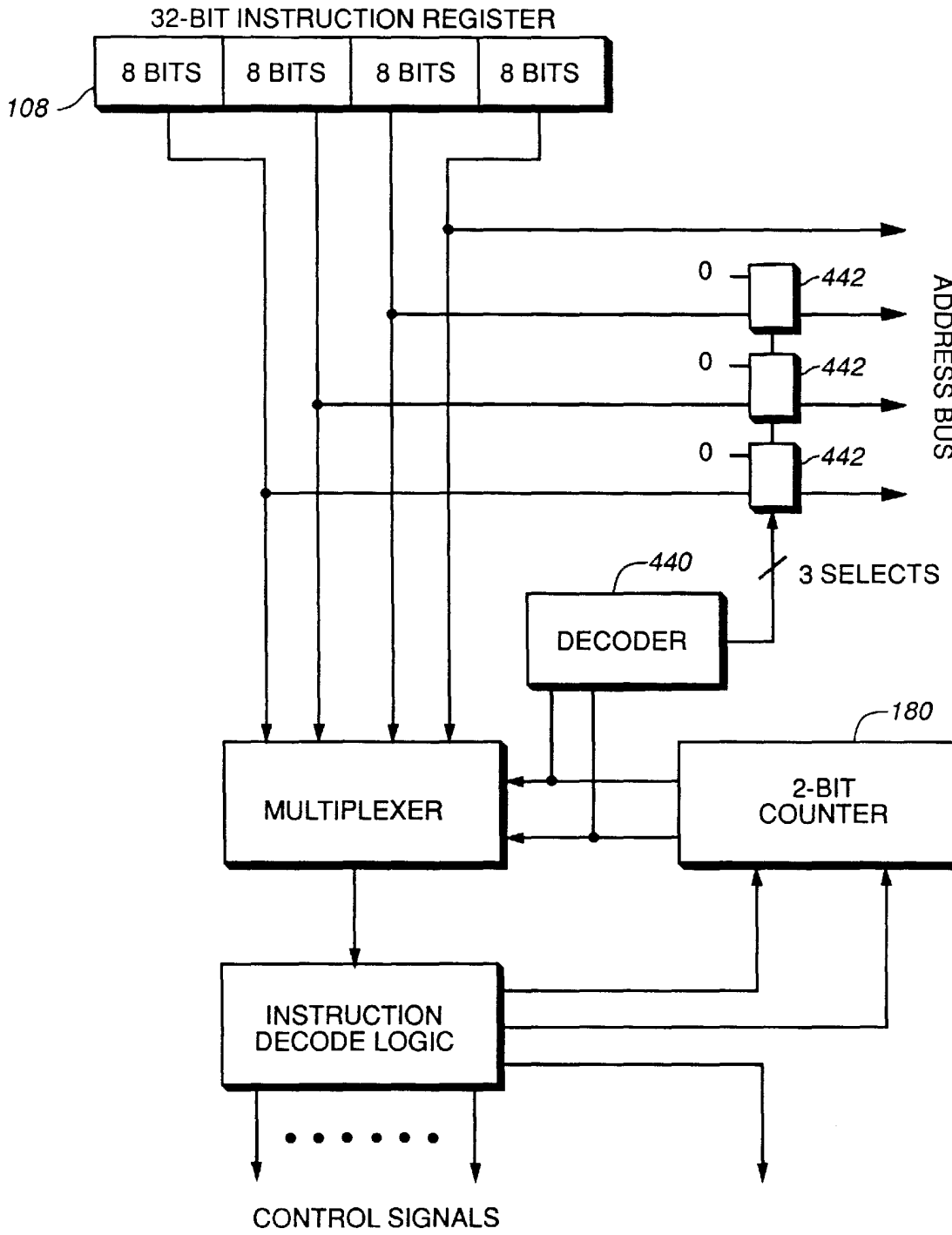

32-BIT INSTRUCTION REGISTER
8 BITS
8 BITS
8 BITS
8 BITS
108
0
442
0
442
0
442
ADDRESS BUS
440
3 SELECTS
DECODER
180
MULTIPLEXER
2-BIT COUNTER
INSTRUCTION DECODE LOGIC
CONTROL SIGNALS

FIG._20

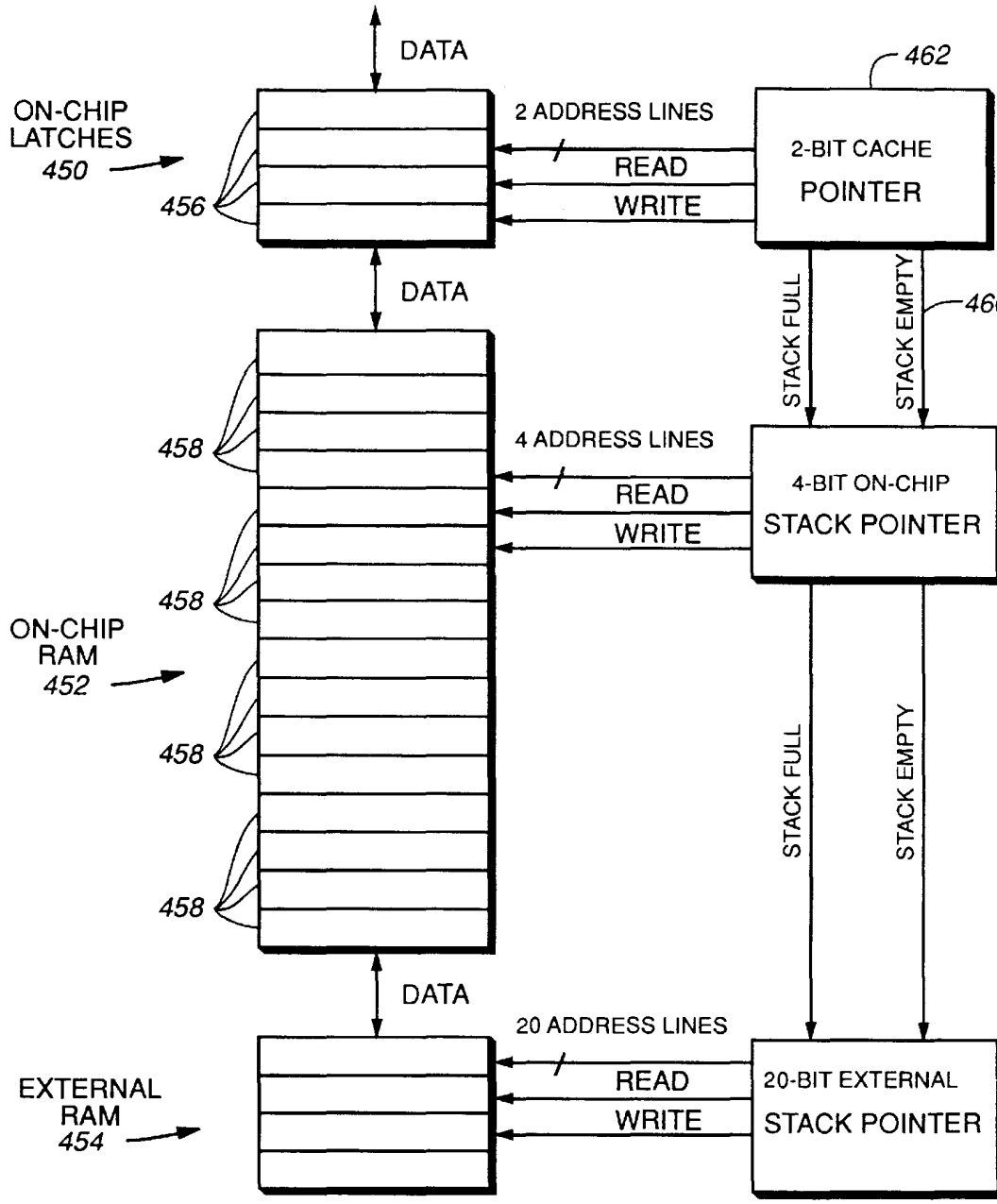

DATA
462
ON-CHIP LATCHES 450
2 ADDRESS LINES
READ
WRITE
2-BIT CACHE POINTER
456
DATA
STACK FULL
STACK EMPTY
460
458
4 ADDRESS LINES
READ
WRITE
4-BIT ON-CHIP STACK POINTER
458
ON-CHIP RAM 452
458
458
STACK FULL
STACK EMPTY
DATA
20 ADDRESS LINES
READ
WRITE
20-BIT EXTERNAL STACK POINTER
EXTERNAL RAM 454

FIG._21

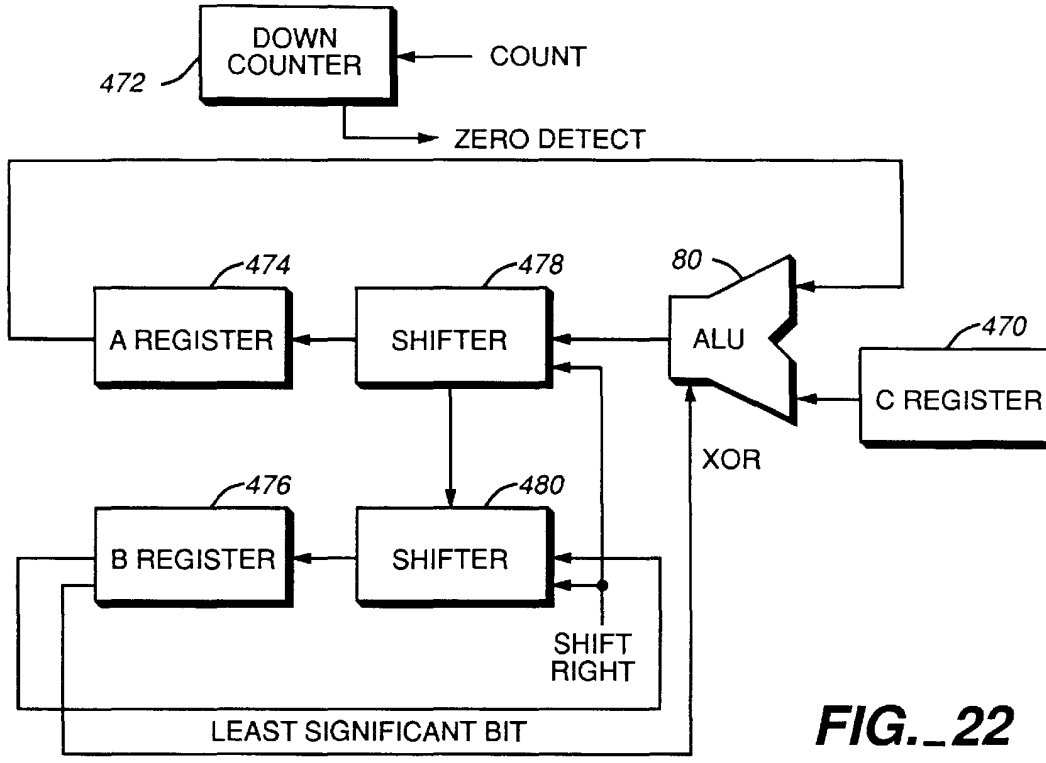

DOWN COUNTER
472
COUNT
ZERO DETECT
474
A REGISTER
478
SHIFTER
80
ALU
470
C REGISTER
XOR
476
B REGISTER
480
SHIFTER
SHIFT RIGHT
LEAST SIGNIFICANT BIT

FIG._22

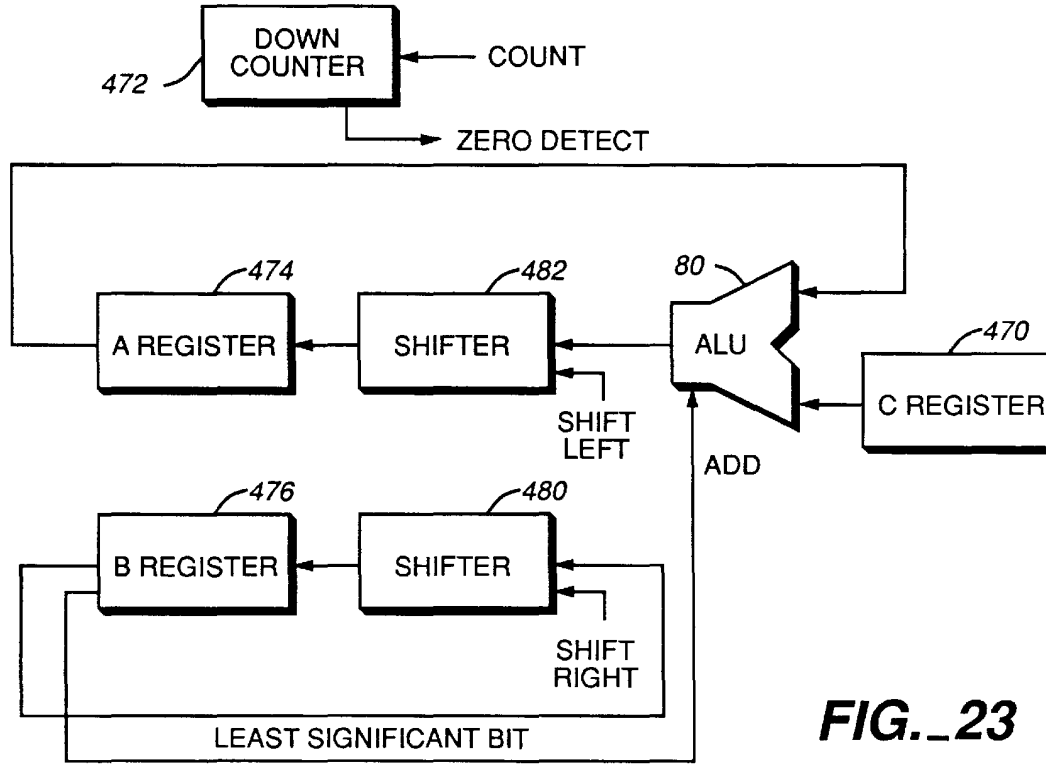

DOWN COUNTER
472
COUNT
ZERO DETECT
474
A REGISTER
482
SHIFTER
80
ALU
470
C REGISTER
SHIFT LEFT
ADD
476
B REGISTER
480
SHIFTER
SHIFT RIGHT
LEAST SIGNIFICANT BIT

FIG._23

HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a division of U.S. application Ser. No. 07/389,334, filed Aug. 3, 1989, now U.S. Pat. No. 5,440,749.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a simplified, reduced instruction set computer (RISC) microprocessor. More particularly, it relates to such a microprocessor which is capable of performance levels of, for example, 20 million instructions per second (MIPS) at a price of, for example, 20 dollars.

2. Description of the Prior Art

Since the invention of the microprocessor, improvements in its design have taken two different approaches. In the first approach, a brute force gain in performance has been achieved through the provision of greater numbers of faster transistors in the microprocessor integrated circuit and an instruction set of increased complexity. This approach is exemplified by the Motorola 68000 and Intel 80X86 microprocessor families. The trend in this approach is to larger die sizes and packages, with hundreds of pinouts.

More recently, it has been perceived that performance gains can be achieved through comparative simplicity, both in the microprocessor integrated circuit itself and in its instruction set. This second approach provides RISC microprocessors, and is exemplified by the Sun SPARC and the Intel 8960 microprocessors. However, even with this approach as conventionally practiced, the packages for the microprocessor are large, in order to accommodate the large number of pinouts that continue to be employed. A need therefore remains for further simplification of high performance microprocessors.

With conventional high performance microprocessors, fast static memories are required for direct connection to the microprocessors in order to allow memory accesses that are fast enough to keep up with the microprocessors. Slower dynamic random access memories (DRAMs) are used with such microprocessors only in a hierarchical memory arrangement, with the static memories acting as a buffer between the microprocessors and the DRAMs. The necessity to use static memories increases cost of the resulting systems.

Conventional microprocessors provide direct memory accesses (DMA) for system peripheral units through DMA controllers, which may be located on the microprocessor integrated circuit, or provided separately. Such DMA controllers can provide routine handling of DMA requests and responses, but some processing by the main central processing unit (CPU) of the microprocessor is required.

SUMMARY OF THE INVENTION

Accordingly, it is an object of this invention to provide a microprocessor with a reduced pin count and cost compared to conventional microprocessors.

It is another object of the invention to provide a high performance microprocessor that can be directly connected to DRAMs without sacrificing microprocessor speed.

It is a further object of the invention to provide a high performance microprocessor in which DMA does not require use of the main CPU during DMA requests and responses and which provides very rapid DMA response with predictable response times.

The attainment of these and related objects may be achieved through use of the novel high performance, low cost microprocessor herein disclosed. In accordance with one aspect of the invention, a microprocessor system in accordance with this invention has a central processing unit, a dynamic random access memory and a bus connecting the central processing unit to the dynamic random access memory. There is a multiplexing means on the bus between the central processing unit and the dynamic random access memory. The multiplexing means is connected and configured to provide row addresses, column addresses and data on the bus.

In accordance with another aspect of the invention, the microprocessor system has a means connected to the bus for fetching instructions for the central processing unit on the bus. The means for fetching instructions is configured to fetch multiple sequential instructions in a single memory cycle. In a variation of this aspect of the invention, a programmable read only memory containing instructions for the central processing unit is connected to the bus. The means for fetching instructions includes means for assembling a plurality of instructions from the programmable read only memory and storing the plurality of instructions in the dynamic random access memory.

In another aspect of the invention, the microprocessor system includes a central processing unit, a direct memory access processing unit and a memory connected by a bus. The direct memory access processing unit includes means for fetching instructions for the central processing unit and for fetching instructions for the direct memory access processing unit on the bus.

In a further aspect of the invention, the microprocessor system, including the memory, is contained in an integrated circuit. The memory is a dynamic random access memory, and the means for fetching multiple instructions includes a column latch for receiving the multiple instructions.

In still another aspect of the invention, the microprocessor system additionally includes an instruction register for the multiple instructions connected to the means for fetching instructions. A means is connected to the instruction register for supplying the multiple instructions in succession from the instruction register. A counter is connected to control the means for supplying the multiple instructions to supply the multiple instructions in succession. A means for decoding the multiple instructions is connected to receive the multiple instructions in succession from the means for supplying the multiple instructions. The counter is connected to said means for decoding to receive incrementing and reset control signals from the means for decoding. The means for decoding is configured to supply the reset control signal to the counter and to supply a control signal to the means for fetching instructions in response to a SKIP instruction in the multiple instructions. In a modification of this aspect of the invention, the microprocessor system additionally has a loop counter connected to receive a decrement control signal from the means for decoding. The means for decoding is configured to supply the reset control signal to the counter and the decrement control signal to the loop counter in response to a MICROLOOP instruction in the multiple instructions. In a further modification to this aspect of the invention, the means for decoding is configured to control

the counter in response to an instruction utilizing a variable width operand. A means is connected to the counter to select the variable width operand in response to the counter.

In a still further aspect of the invention, the microprocessor system includes an arithmetic logic unit. A first push down stack is connected to the arithmetic logic unit. The first push down stack includes means for storing a top item connected to a first input of the arithmetic logic unit and means for storing a next item connected to a second input of the arithmetic logic unit. The arithmetic logic unit has an output connected to the means for storing a top item. The means for storing a top item is connected to provide an input to a register file. The register file desirably is a second push down stack, and the means for storing a top item and the register file are bidirectionally connected.

In another aspect of the invention, a data processing system has a microprocessor including a sensing circuit and a driver circuit, a memory, and an output enable line connected between the memory, the sensing circuit and the driver circuit. The sensing circuit is configured to provide a ready signal when the output enable line reaches a predetermined electrical level, such as a voltage. The microprocessor is configured so that the driver circuit provides an enabling signal on the output enable line responsive to the ready signal.

In a further aspect of the invention, the microprocessor system has a ring counter variable speed system clock connected to the central processing unit. The central processing unit and the ring counter variable speed system clock are provided in a single integrated circuit. An input/output interface is connected to exchange coupling control signals, addresses and data with the input/output interface. A second clock independent of the ring counter variable speed system clock is connected to the input/output interface.

In yet another aspect of the invention, a push down stack is connected to the arithmetic logic unit. The push down stack includes means for storing a top item connected to a first input of the arithmetic logic unit and means for storing a next item connected to a second input of the arithmetic logic unit. The arithmetic logic unit has an output connected to the means for storing a top item. The push down stack has a first plurality of stack elements configured as latches and a second plurality of stack elements configured as a random access memory. The first and second plurality of stack elements and the central processing unit are provided in a single integrated circuit. A third plurality of stack elements is configured as a random access memory external to the single integrated circuit. In this aspect of the invention, desirably a first pointer is connected to the first plurality of stack elements, a second pointer connected to the second plurality of stack elements, and a third pointer is connected to the third plurality of stack elements. The central processing unit is connected to pop items from the first plurality of stack elements. The first stack pointer is connected to the second stack pointer to pop a first plurality of items from the second plurality of stack elements when the first plurality of stack elements are empty from successive pop operations by the central processing unit. The second stack pointer is connected to the third stack pointer to pop a second plurality of items from the third plurality of stack elements when the second plurality of stack elements are empty from successive pop operations by the central processing unit.

In another aspect of the invention, a first register is connected to supply a first input to the arithmetic logic unit. A first shifter is connected between an output of the arithmetic logic unit and the first register. A second register is connected to receive a starting polynomial value. An output of the second register is connected to a second shifter. A least significant bit of the second register is connected to The arithmetic logic unit. A third register is connected to supply feedback terms of a polynomial to the arithmetic logic unit. A down counter, for counting down a number corresponding to digits of a polynomial to be generated, is connected to the arithmetic logic unit. The arithmetic logic unit is responsive to a polynomial instruction to carry out an exclusive OR of the contents of the first register with the contents of the third register if the least significant bit of the second register is a "ONE" and to pass the contents of the first register unaltered if the least significant bit of the second register is a "ZERO", until the down counter completes a count. The polynomial to be generated results in said first register.

In still another aspect of the invention, a result register is connected to supply a first input to the arithmetic logic unit. A first, left shifting shifter is connected between an output of the arithmetic logic unit and the result register. A multiplier register is connected to receive a multiplier in bit reversed form. An output of the multiplier register is connected to a second, right shifting shifter. A least significant bit of the multiplier register is connected to the arithmetic logic unit. A third register is connected to supply a multiplicand to said arithmetic logic unit. A down counter, for counting down a number corresponding to one less than the number of digits of the multiplier, is connected to the arithmetic logic unit. The arithmetic logic unit is responsive to a multiply instruction to add the contents of the result register with the contents of the third register, when the least significant bit of the multiplier register is a "ONE" and to pass the contents of the result register unaltered, until the down counter completes a count. The product results in the result register.

The attainment of the foregoing and related objects, advantages and features of the invention should be more readily apparent to those skilled in the art, after review of the following more detailed description of the invention, taken together with the drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an external, plan view of an integrated circuit package incorporating a microprocessor in accordance with the invention.

FIG. **2** is a block diagram of a microprocessor in accordance with the invention.

FIG. **3** is a block diagram of a portion of a data processing system incorporating the microprocessor of FIGS. **1** and **2**.

FIG. **4** is a more detailed block diagram of a portion of the microprocessor shown in FIG. **2**.

FIG. **5** is a more detailed block diagram of another portion of the microprocessor shown in FIG. **2**.

FIG. **6** is a block diagram of another portion of the data processing system shown in part in FIG. **3** and incorporating the microprocessor of FIGS. **1–2** and **4–5**.

FIGS. **7** and **8** are layout diagrams for the data processing system shown in part in FIGS. **3** and **6**.

FIG. **9** is a layout diagram of a second embodiment of a microprocessor in accordance with the invention in a data processing system on a single integrated circuit.

FIG. **10** is a more detailed block diagram of a portion of the data processing system of FIGS. **7** and **8**.

FIG. **11** is a timing diagram useful for understanding operation of the system portion shown in FIG. **12**.

FIG. **12** is another more detailed block diagram of a further portion of the data processing system of FIGS. **7** and **8**.

FIG. **13** is a more detailed block diagram of a portion of the microprocessor shown in FIG. **2**.

FIG. **14** is a more detailed block and schematic diagram of a portion of the system shown in FIGS. **3** and **7–8**.

FIG. **15** is a graph useful for understanding operation of the system portion shown in FIG. **14**.

FIG. **16** is a more detailed block diagram showing part of the system portion shown in FIG. **4**.

FIG. **17** is a more detailed block diagram of a portion of the microprocessor shown in FIG. **2**.

FIG. **18** is a more detailed block diagram of part of the microprocessor portion shown in FIG. **17**.

FIG. **19** is a set of waveform diagrams useful for understanding operation of the part of the microprocessor portion shown in FIG. **18**.

FIG. **20** is a more detailed block diagram showing another part of the system portion shown in FIG. **4**.

FIG. **21** is a more detailed block diagram showing another part of the system portion shown in FIG. **4**.

FIGS. **22** and **23** are more detailed block diagrams showing another part of the system portion shown in FIG. **4**.

DETAILED DESCRIPTION OF THE INVENTION

Overveiw

The microprocessor of this invention is desirably implemented as a 32-bit microprocessor optimized for:

HIGH EXECUTION SPEED, and

LOW SYSTEM COST.

In this embodiment, the microprocessor can be thought of as 20 MIPS for 20 dollars. Important distinguishing features of the microprocessor are:

Uses low-cost commodity DYNAMIC RAMS to run 20 MIPS

4 instruction fetch per memory cycle

On-chip fast page-mode memory management

Runs fast without external cache

Requires few interfacing chips

Crams 32-bit CPU in 44 pin SOJ package

The instruction set is organized so that most operations can be specified with 8-bit instructions. Two positive products of this philosophy are:

Programs are smaller,

Programs can execute much faster.

The bottleneck in most computer systems is the memory bus. The bus is used to fetch instructions and fetch and store data. The ability to fetch four instructions in a single memory bus cycle significantly increases the bus availability to handle data.

Turning now to the drawings, more particularly to FIG. **1**, there is shown a packaged 32-bit microprocessor **50** in a 44-pin plastic leadless chip carrier, shown approximately 100 times its actual size of about 0.8 inch on a side. The fact that the microprocessor **50** is provided as a 44-pin package represents a substantial departure from typical microprocessor packages, which usually have about 200 input/output (I/O) pins. The microprocessor **50** is rated at 20 million instructions per second (MIPS). Address and data lines **52**, also labelled **D0–D31**, are shared for addresses and data without speed penalty as a result of the manner in which the microprocessor **50** operates, as will be explained below.

DYNAMIC RAM

In addition to the low cost 44-pin package, another unusual aspect of the high performance microprocessor **50** is that it operates directly with dynamic random access memories (DRAMs), as shown by row address strobe (RAS) and column address strobe (CAS) I/O pins **54**. The other I/O pins for the microprocessor **50** include V_{DD} pins **56**, V_{SS} pins **58**, output enable pin **60**, write pin **62**, clock pin **64** and reset pin **66**.

All high speed computers require high speed and expensive memory to keep up. The highest speed static RAM memories cost as much as ten times as much as slower dynamic RAMs. This microprocessor has been optimized to use low-cost dynamic RAM in high-speed page-mode. Page-mode dynamic RAMs offer static RAM performance without the cost penalty. For example, low-cost 85 nsec. dynamic RAMs access at 25 nsec when operated in fast page-mode. Integrated fast page-mode control on the microprocessor chip simplifies system interfacing and results in a faster system.

Details of the microprocessor **50** are shown in FIG. **2**. The microprocessor **50** includes a main central processing unit (CPU) **70** and a separate direct memory access (DMA) CPU **72** in a single integrated circuit making up the microprocessor **50**. The main CPU **70** has a first **16** deep push down stack **74**, which has a top item register **76** and a next item register **78**, respectively connected to provide inputs to an arithmetic logic unit (ALU) **80** by lines **82** and **84**. An output of the ALU **80** is connected to the top item register **76** by line **86**. The output of the top item register at **82** is also connected by line **88** to an internal data bus **90**.

A loop counter **92** is connected to a decrementer **94** by lines **96** and **98**. The loop counter **92** is bidirectionally connected to the internal data bus **90** by line **100**. Stack pointer **102**, return stack pointer **104**, mode register **106** and instruction register **108** are also connected to the internal data bus **90** by lines **110**, **112**, **114** and **116**, respectively. The internal data bus **90** is connected to memory controller **118** and to gate **120**. The gate **120** provides inputs on lines **122**, **124**, and **126** to X register **128**, program counter **130** and Y register **132** of return push down stack **134**. The X register **128**, program counter **130** and Y register **132** provide outputs to internal address bus **136** on lines **138**, **140** and **142**. The internal address bus provides inputs to the memory controller **118** and to an incrementer **144**. The incrementer **144** provides inputs to the X register, program counter and Y register via lines **146**, **122**, **124** and **126**. The DMA CPU **72** provides inputs to the memory controller **118** on line **148**. The memory controller **118** is connected to a RAM (not shown) by address/data bus **150** and control lines **152**.

FIG. **2** shows that the microprocessor **50** has a simple architecture. Prior art RISC microprocessors are substantially more complex in design. For example, the SPARC RISC microprocessor has three times the gates of the microprocessor **50**, and the Intel 8960 RISC microprocessor has 20 times the gates of the microprocessor **50**. The speed of this microprocessor is in substantial part due to this simplicity. The architecture incorporates push down stacks and register write to achieve this simplicity.

The microprocessor **50** incorporates an I/O that has been tuned to make heavy use of resources provided on the integrated circuit chip. On chip latches allow use of the same I/O circuits to handle three different things: column addressing, row addressing and data, with a slight to non-existent speed penalty. This triple bus multiplexing results in fewer buffers to expand, fewer interconnection lines, fewer I/O pins and fewer internal buffers.

The provision of on-chip DRAM control gives a performance equal to that obtained with the use of static RAMs. As a result, memory is provided at ¼ the system cost of static RAM used in most RISC systems.

The microprocessor **50** fetches 4 instructions per memory cycle; the instructions are in an 8-bit format, and this is a 32-bit microprocessor. System speed is therefore 4 times the memory bus bandwidth. This ability enables the microprocessor to break the Von Neumann bottleneck of the speed of getting the next instruction. This mode of operation is possible because of the use of a push down stack and register array. The push down stack allows the use of implied addresses, rather than the prior art technique of explicit addresses for two sources and a destination.

Most instructions execute in 20 nanoseconds in the microprocessor **50**. The microprocessor can therefore execute instructions at 50 peak MIPS without pipeline delays. This is a function of the small number of gates in the microprocessor **50** and the high degree of parallelism in the architecture of the microprocessor.

FIG. **3** shows how column and row addresses are multiplexed on lines D**8**–D**14** of the microprocessor **50** for addressing DRAM **150** from I/O pins **52**. The DRAM **150** is one of eight, but only one DRAM **150** has been shown for clarity. As shown, the lines D**11**–D**18** are respectively connected to row address inputs A**0**–A**8** of the DRAM **150**. Additionally, lines D**12**–D**15** are connected to the data inputs DQ**1**–DQ**4** of the DRAM **150**. The output enable, write and column address strobe pins **54** are respectively connected to the output enable, write and column address strobe inputs of the DRAM **150** by lines **152**. The row address strobe pin **54** is connected through row address strobe decode logic **154** to the row address strobe input of the DRAM **150** by lines **156** and **158**.

D**0**–D**7** pins **52** (FIG. **1**) are idle when the microprocessor **50** is outputting multiplexed row and column addresses on D**11**–D**18** pins **52**. The D**0**–D**7** pins **52** can therefore simultaneously be used for I/O when right justified I/O is desired. Simultaneous addressing and I/O can therefore be carried out.

FIG. **4** shows how the microprocessor **50** is able to achieve performance equal to the use of static RAMS with DRAMs through multiple instruction fetch in a single clock cycle and instruction fetch-ahead. Instruction register **108** receives four 8-bit byte instruction words 1–4 on 32-bit internal data bus **90**. The four instruction byte 1–4 locations of the instruction register **108** are connected to multiplexer **170** by busses **172**, **174**, **176** and **178**, respectively. A microprogram counter **180** is connected to the multiplexer **170** by lines **182**. The multiplexer **170** is connected to decoder **184** by bus **186**. The decoder **184** provides internal signals to the rest of the microprocessor **50** on lines **188**.

Most significant bits **190** of each instruction byte 1–4 location are connected to a 4-input decoder **192** by lines **194**. The output of decoder **192** is connected to memory controller **118** by line **196**. Program counter **130** is connected to memory controller **118** by internal address bus **136**, and the instruction register **108** is connected to the memory controller **118** by the internal data bus **90**. Address/data bus **198** and control bus **200** are connected to the DRAMS **150** (FIG. **3**).

In operation, when the most significant bits **190** of remaining instructions 1–4 are "1" in a clock cycle of the microprocessor **50**, there are no memory reference instructions in the queue. The output of decoder **192** on line **196** requests an instruction fetch ahead by memory controller **118** without interference with other accesses. While the current instructions in instruction register **108** are executing, the memory controller **118** obtains the address of the next set of four instructions from program counter **130** and obtains that set of instructions. By the time the current set of instructions has completed execution, the next set of instructions is ready for loading into the instruction register.

Details of the DMA CPU **72** are provided in FIG. **5**. Internal data bus **90** is connected to memory controller **118** and to DMA instruction register **210**. The DMA instruction register **210** is connected to DMA program counter **212** by bus **214**, to transfer size counter **216** by bus **218** and to timed transfer interval counter **220** by bus **222**. The DMA instruction register **210** is also connected to DMA I/O and RAM address register **224** by line **226**. The DMA I/O and RAM address register **224** is connected to the memory controller **118** by memory cycle request line **228** and bus **230**. The DMA program counter **212** is connected to the internal address bus **136** by bus **232**. The transfer size counter **216** is connected to a DMA instruction done decrementer **234** by lines **236** and **238**. The decrementer **234** receives a control input on memory cycle acknowledge line **240**. When transfer size counter **216** has completed its count, it provides a control signal to DMA program counter **212** on line **242**. Timed transfer interval counter **220** is connected to decrementer **244** by lines **246** and **248**. The decrementer **244** receives a control input from a microprocessor system clock on line **250**.

The DMA CPU **72** controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU **70** (FIG. **2**) for time specific processing.

FIG. **6** shows how the microprocessor **50** is connected to an electrically programmable read only memory (EPROM) **260** by reconfiguring the data lines **52** so that some of the data lines **52** are input lines and some of them are output lines. Data lines **52** D**0**–D**7** provide data to and from corresponding data terminals **262** of the EPROM **260**. Data lines **52** D**9**–D**18** provide addresses to address terminals **264** of the EPROM **260**. Data lines **52** D**19**–D**31** provide inputs from the microprocessor **50** to memory and I/O decode logic **266**. RAS 0/1 control line **268** provides a control signal for determining whether the memory and I/O decode logic provides a DRAM RAS output on line **270** or a column enable output for the EPROM **260** on line **272**. Column address strobe terminal **60** of the microprocessor **50** provides an output enable signal on line **274** to the corresponding terminal **276** of the EPROM **260**.

FIGS. **7** and **8** show the front and back of a one card data processing system **280** incorporating the microprocessor **50**, MSM514258-10 type DRAMs **150** totalling 2 megabytes, a Motorola 50 MegaHertz crystal oscillator clock **282**, I/O circuits **284** and a 27256 type EPROM **260**. The I/O circuits **284** include a 74HC04 type high speed hex inverter circuit **286**, an IDT39C828 type 10-bit inverting buffer circuit **288**, an IDT39C822 type 10-bit inverting register circuit **290**, and two IDT39C823 type 9-bit non-inverting register circuits **292**. The card **280** is completed with a MAX12V type DC-DC converter circuit **294**, 34-pin dual AMP type headers **296**, a coaxial female power connector **298**, and a 3-pin AMP right angle header **300**. The card **280** is a low cost, imbeddable product that can be incorporated in larger systems or used as an internal development tool.

The microprocessor **50** is a very high performance (50 MHz) RISC influenced 32-bit CPU designed to work closely with dynamic RAM. Clock for clock, the microprocessor **50** approaches the theoretical performance limits possible with a single CPU configuration. Eventually, the microprocessor **50** and any other processor is limited by the bus bandwidth and the number of bus paths. The critical conduit is between the CPU and memory.

One solution to the bus bandwidth/bus path problem is to integrate a CPU directly onto the memory chips, giving every memory a direct bus the CPU. FIG. **9** shows another microprocessor **310** that is provided integrally with 1 mega-

bit of DRAM **311** in a single integrated circuit **312**. Until the present invention, this solution has not been practical, because most high performance CPUs require from 500,000 to 1,000,000 transistors and enormous die sizes just by themselves. The microprocessor **310** is equivalent to the microprocessor **50** in FIGS. **1–8**. The microprocessors **50** and **310** are the most transistor efficient high performance CPUs in existence, requiring fewer than 50,000 transistors for dual processors **70** and **72** (FIG. **2**) or **314** and **316** (less memory). The very high speed of the microprocessors **50** and **310** is to a certain extent a function of the small number of active devices. In essence, the less silicon gets in the way, the faster the electrons can get where they are going.

The microprocessor **310** is therefore the only CPU suitable for integration on the memory chip die **312**. Some simple modifications to the basic microprocessor **50** to take advantage of the proximity to the DRAM array **311** can also increase the microprocessor **50** clock speed by **50** percent, and probably more.

The microprocessor **310** core on board the DRAM die **312** provides most of the speed and functionality required for a large group of applications from automotive to peripheral control. However, the integrated CPU **310**/DRAM **311** concept has the potential to redefine significantly the way multiprocessor solutions can solve a spectrum of very compute intensive problems. The CPU **310**/DRAM **311** combination eliminates the Von Neumann bottleneck by distributing it across numerous CPU/DRAM chips **312**. The microprocessor **310** is a particularly good core for multiprocessing, since it was designed with the SDI targeting array in mind, and provisions were made for efficient interprocessor communications.

Traditional multiprocessor implementations have been very expensive in addition to being unable to exploit fully the available CPU horsepower. Multiprocessor systems have typically been built up from numerous board level or box level computers. The result is usually an immense amount of hardware with corresponding wiring, power consumption and communications problems. By the time the systems are interconnected, as much as 50 percent of the bus speed has been utilized just getting through the interfaces.

In addition, multiprocessor system software has been scarce. A multiprocessor system can easily be crippled by an inadequate load-sharing algorithm in the system software, which allows one CPU to do a great deal of work and the others to be idle. Great strides have been made recently in systems software, and even UNIX V.4 may be enhanced to support multiprocessing. Several commercial products from such manufacturers as DUAL Systems and UNISOFT do a credible job on 68030 type microprocessor systems now.

The microprocessor **310** architecture eliminates most of the interface friction, since up to 64 CPU **310**/RAM **311** processors should be able to intercommunicate without buffers or latches. Each chip **312** has about 40 MIPS raw speed, because placing the DRAM **311** next to the CPU **310** allows the microprocessor **310** instruction cycle to be cut in half, compared to the microprocessor **50**. A 64 chip array of these chips **312** is more powerful than any other existing computer. Such an array fits on a 3×5 card, cost less than a FAX machine, and draw about the same power as a small television.

Dramatic changes in price/performance always reshape existing applications and almost always create new ones. The introduction of microprocessors in the mid 1970s created video games, personal computers, automotive computers, electronically controlled appliances, and low cost computer peripherals.

The integrated circuit **312** will find applications in all of the above areas, plus create some new ones. A common generic parallel processing algorithm handles convolution/Fast Fourier Transform (FFT)/pattern recognition. Interesting product possibilities using the integrated circuit **312** include high speed reading machines, real-time speech recognition, spoken language translation, real-time robot vision, a product to identify people by their faces, and an automotive or aviation collision avoidance system.

A real time processor for enhancing high density television (HDTV) images, or compressing the HDTV information into a smaller bandwidth, would be very. feasible. The load sharing in HDTV could be very straightforward. Splitting up the task according to color and frame would require 6, 9 or 12 processors. Practical implementation might require 4 meg RAMs integrated with the microprocessor **310**.

The microprocessor **310** has the following specifications:

CONTROL LINES
4—POWER/GROUND
1—CLOCK
32—DATA I/O
4—SYSTEM CONTROL
EXTERNAL MEMORY FETCH
EXTERNAL MEMORY FETCH AUTOINCREMENT X
EXTERNAL MEMORY FETCH AUTOINCREMENT Y
EXTERNAL MEMORY WRITE
EXTERNAL MEMORY WRITE AUTOINCREMENT X
EXTERNAL MEMORY WRITE AUTOINCREMENT Y
EXTERNAL PROM FETCH
LOAD ALL X REGISTERS
LOAD ALL Y REGISTERS
LOAD ALL PC REGISTERS
EXCHANGE X AND Y
INSTRUCTION FETCH
ADD TO PC
ADD TO X
WRITE MAPPING REGISTER
READ MAPPING REGISTER
REGISTER CONFIGURATION
MICROPROCESSOR **310** CPU **316** CORE
COLUMN LATCH**1** (1024 BITS) 32×32 MUX
STACK POINTER (16 BITS)
COLUMN LATCH**2** (1024 BITS) 32×32 MUX
RSTACK POINTER (16 BITS)
PROGRAM COUNTER 32 BITS
X0 REGISTER 32 BITS (ACTIVATED ONLY FOR ON-CHIP ACCESSES)
Y0 REGISTER 32 BITS (ACTIVATED ONLY FOR ON-CHIP ACCESSES)
LOOP COUNTER 32 BITS
DMA CPU **314** CORE
DMA PROGRAM COUNTER 24 BITS
INSTRUCTION REGISTER 32 BITS
I/O & RAM ADDRESS REGISTER 32 BITS
TRANSFER SIZE COUNTER 12 BITS
INTERVAL COUNTER 12 BITS

To offer memory expansion for the basic chip **312**, an intelligent DRAM can be produced. This chip will be optimized for high speed operation with the integrated circuit **312** by having three on-chip address registers: Program Counter, X Register and Y register. As a result, to access the intelligent DRAM, no address is required, and a total access cycle could be as short as 10 nsec. Each

expansion DRAM would maintain its own copy of the three registers and would be identified by a code specifying its memory address. Incrementing and adding to the three registers will actually take place on the memory chips. A maximum of 64 intelligent DRAM peripherals would allow a large system to be created without sacrificing speed by introducing multiplexers or buffers.

There are certain differences between the microprocessor **310** and the microprocessor **50** that arise from providing the microprocessor **310** on the same die **312** with the DRAM **311**. Integrating the DRAM **311** allows architectural changes in the microprocessor **310** logic to take advantage of existing on-chip DRAM **311** circuitry. Row and column design is inherent in memory architecture. The DRAMs **311** access random bits in a memory array by first selecting a row of 1024 bits, storing them into a column latch, and then selecting one of the bits as the data to be read or written.

The time required to access the data is split between the row access and the column access. Selecting data already stored in a column latch is faster than selecting a random bit by at least a factor of six. The microprocessor **310** takes advantage of this high speed by creating a number of column latches and using them as caches and shift registers. Selecting a new row of information may be thought of as performing a 1024-bit read or write with the resulting immense bus bandwidth.

1. The microprocessor **50** treats its 32-bit instruction register **108** (see FIGS. **2** and **4**) as a cache for four 8-bit instructions. Since the DRAM **311** maintains a 1024-bit latch for the column bits, the microprocessor **310** treats the column latch as a cache for 128 8-bit instructions. Therefore, the next instruction will almost always be already present in the cache. Long loops within the cache are also possible and more useful than the 4 instruction loops in the microprocessor **50**.

2. The microprocessor **50** uses two 16×32-bit deep register arrays **74** and **134** (FIG. **2**) for the parameter stack and the return stack. The microprocessor **310** creates two other 1024-bit column latches to provide the equivalent of two 32×32-bit arrays, which can be accessed twice as fast as a register array.

3. The microprocessor **50** has a DMA capability which can be used for I/O to a video shift register. The microprocessor **310** uses yet another 1024-bit column latch as a long video shift register to drive a CRT display directly. For color displays, three on-chip shift registers could also be used. These shift registers can transfer pixels at a maximum of 100 MHz.

4. The microprocessor **50** accesses memory via an external 32-bit bus. Most of the memory **311** for the microprocessor **310** is on the same die **312**. External access to more memory is made using an 8-bit bus. The result is a smaller die, smaller package and lower power consumption than the microprocessor **50**.

5. The microprocessor **50** consumes about a third of its operating power charging and discharging the I/O pins and associated capacitances. The DRAMs **150** (FIG. **8**) connected to the microprocessor **50** dissipate most of their power in the I/O drivers. A microprocessor **310** system will consume about one-tenth the power of a microprocessor **50** system, since having the DRAM **311** next to the processor **310** eliminates most of the external capacitances to be charged and discharged.

6. Multiprocessing means splitting a computing task between numerous processors in order to speed up the solution. The popularity of multiprocessing is limited by the expense of current individual processors as well as the limited interprocessor communications ability. The microprocessor **310** is an excellent multiprocessor candidate, since the chip **312** is a monolithic computer complete with memory, rendering it low-cost and physically compact.

The shift registers implemented with the microprocessor **310** to perform video output can also be configured as interprocessor communication links. The INMOS transputer attempted a similar strategy, but at much lower speed and without the performance benefits inherent in the microprocessor **310** column latch architecture. Serial I/O is a prerequisite for many multiprocessor topologies because of the many neighbor processors which communicate. A cube has 6 neighbors. Each neighbor communicates using these lines:

DATA IN
CLOCK IN
READY FOR DATA
DATA OUT
DATA READY?
CLOCK OUT

A special start up sequence is used to initialize the on-chip DRAM **311** in each of the processors.

The microprocessor **310** column latch architecture allows neighbor processors to deliver information directly to internal registers or even instruction caches of other chips **312**. This technique is not used with existing processors, because it only improves performance in a tightly coupled DRAM system.

7. The microprocessor **50** architecture offers two types of looping structures: LOOP-IF-DONE and MICRO-LOOP. The former takes an 8-bit to 24-bit operand to describe the entry point to the loop address. The latter performs a loop entirely within the 4 instruction queue and the loop entry point is implied as the first instruction in the queue. Loops entirely within the queue run without external instruction fetches and execute up to three times as fast as the long loop construct. The microprocessor **310** retains both constructs with a few differences. The microprocessor **310** microloop functions in the same fashion as the microprocessor **50** operation, except the queue is 1024-bits or 128 8-bit instructions long. The microprocessor **310** microloop can therefore contain jumps, branches, calls and immediate operations not possible in the 4 8-bit instruction microprocessor **50** queue.

Microloops in the microprocessor **50** can only perform simple block move and compare functions. The larger microprocessor **310** queue allows entire digital signal processing or floating point algorithms to loop at high speed in the queue.

The microprocessor **50** offers four instructions to redirect execution:

CALL
BRANCH
BRANCH-IF-ZERO
LOOP-IF-NOT-DONE

These instructions take a variable length address operand 8, 16 or 24 bits long. The microprocessor **50** next address logic treats the three operands similarly by adding or subtracting them to the current program counter. For the microprocessor **310**, the 16 and 24-bit operands function in the same manner as the 16 and 24-bit operands in the microprocessor **50**. The 8-bit class operands are reserved to operate entirely within the instruction queue. Next address decisions can therefore be made quickly, because only 10 bits of addresses are affected, rather than 32. There is no carry or borrow generated past the 10 bits.

8. The microprocessor **310** CPU **316** resides on an already crowded DRAM die **312**. To keep chip size as small as

possible, the DMA processor **72** of the microprocessor **50** has been replaced with a more traditional DMA controller **314**. DMA is used with the microprocessor **310** to perform the following functions:

Video output to a CRT

Multiprocessor serial communications

8-bit parallel I/O

The DMA controller **314** can maintain both serial and parallel transfers simultaneously. The following DMA sources and destinations are supported by the microprocessor **310**:

DESCRIPTION	I/O	LINES
1. Video shift register	OUTPUT	1 to 3
2. Multiprocessor serial	BOTH	6 lines/channel
3. 8-bit parallel	BOTH	8 data, 4 control

The three sources use separate 1024-bit buffers and separate I/O pins. Therefore, all three may be active simultaneously without interference.

The microprocessor **310** can be implemented with either a single multiprocessor serial buffer or separate receive and sending buffers for each channel, allowing simultaneous bidirectional communications with six neighbors simultaneously.

FIGS. **10** and **11** provide details of the PROM DMA used in the microprocessor **50**. The microprocessor **50** executes faster than all but the fastest PROMs. PROMS are used in a microprocessor **50** system to store program segments and perhaps entire programs. The microprocessor **50** provides a feature on power-up to allow programs to be loaded from low-cost, slow speed PROMs into high speed DRAM for execution. The logic which performs this function is part of the DMA memory controller **118**. The operation is similar to DMA, but not identical, since four 8-bit bytes must be assembled on the microprocessor **50** chip, then written to the DRAM **150**.

The microprocessor **50** directly interfaces to DRAM **150** over a triple multiplexed data and address bus **350**, which carries RAS addresses, CAS addresses and data. The EPROM **260**, on the other hand, is read with non-multiplexed busses. The microprocessor **50** therefore has a special mode which unmultiplexes the data and address lines to read 8 bits of EPROM data. Four 8-bit bytes are read in this fashion. The multiplexed bus **350** is turned back on, and the data is written to the DRAM **150**.

When the microprocessor **50** detects a RESET condition, the processor stops the main CPU **70** and forces a mode **0** (PROM LOAD) instruction into the DMA CPU **72** instruction register. The DMA instruction directs the memory controller to read the EPROM **260** data at 8 times the normal access time for memory. Assuming a 50 MHz microprocessor **50**, this means an access time of 320 nsec. The instruction also indicates:

The selection address of the EPROM **260** to be loaded,

The number of 32-bit words to transfer,

The DRAM **150** address to transfer into.

The sequence of activities to transfer one 32-bit word from EPROM **260** to DRAM **150** are:

1. RAS goes low at **352**, latching the EPROM **260** select information from the high order address bits. The EPROM **260** is selected.
2. Twelve address bits (consisting of what is normally DRAM CAS addresses plus two byte select bits are placed on the bus **350** going to the EPROM **260** address pins. These signals will remain on the lines until the data from the EPROM **260** has been read into the microprocessor **50**. For the first byte, the byte select bits will be binary 00.
3. CAS goes low at **354**, enabling the EPROM **260** data onto the lower 8 bits of the external address/data bus **350**. NOTE: It is important to recognize that, during this part of the cycle, the lower 8 bits of the external data/address bus are functioning as inputs, but the rest of the bus is still acting as outputs.
4. The microprocessor **50** latches these eight least significant bits internally and shifts them 8 bits left to shift them to the next significant byte position.
5. Steps 2, 3 and 4 are repeated with byte address 01.
6. Steps 2, 3 and 4 are repeated with byte address 10.
7. Steps 2, 3 and 4 are repeated with byte address 11.
8. CAS goes high at **356**, taking the EPROM **260** off the data bus.
9. RAS goes high at **358**, indicating the end of the EPROM **260** access.
10. RAS goes low at **360**, latching the DRAM select information from the high order address bits. At the same time, the RAS address bits are latched into the DRAM **150**. The DRAM **150** is selected.
11. CAS goes low at **362**, latching the DRAM **150** CAS addresses.
12. The microprocessor **50** places the previously latched EPROM **260** 32-bit data onto the external address/data bus **350**. W goes low at **364**, writing the 32 bits into the DRAM **150**.
13. W goes high at **366**. CAS goes high at **368**. The process continues with the next word.

FIG. **12** shows details of the microprocessor **50** memory controller **118**. In operation, bus requests stay present until they are serviced. CPU **70** requests are prioritized at **370** in the order of: 1, Parameter Stack; 2, Return Stack; 3, Data Fetch; 4, Instruction Fetch. The resulting CPU request signal and a DMA request signal are supplied as bus requests to bus control **372**, which provides a bus grant signal at **374**. Internal address bus **136** and a DMA counter **376** provide inputs to a multiplexer **378**. Either a row address or a column address are provided as an output to multiplexed address bus **380** as an output from the multiplexer **378**. The multiplexed address bus **380** and the internal data bus **90** provide address and data inputs, respectively, to multiplexer **382**. Shift register **384** supplies row address strobe (RAS) **1** and **2** control signals to multiplexer **386** and column address strobe (CAS) **1** and **2** control signals to multiplexer **388** on lines **390** and **392**. The shift register **384** also supplies output enable (OE) and write (W) signals on lines **394** and **396** and a control signal on line **398** to multiplexer **382**. The shift register **384** receives a RUN signal on line **400** to generate a memory cycle and supplies a MEMORY READY signal on line **402** when an access is complete.

STACK/REGISTER ARCHITECTURE

Most microprocessors use on-chip registers for temporary storage of variables. The on-chip registers access data faster than off-chip RAM. A few microprocessors use an on-chip push down stack for temporary storage.

A stack has the advantage of faster operation compared to on-chip registers by avoiding the necessity to select source and destination registers. (A math or logic operation always uses the top two stack items as source and the top of stack as destination.) The stack's disadvantage is that it makes some operations clumsy. Some compiler activities in particular require on-chip registers for efficiency.

As shown in FIG. **13**, the microprocessor **50** provides both on-chip registers **134** and a stack **74** and reaps the benefits of both.

BENEFITS:

1. Stack math and logic is twice as fast as those available on an equivalent register only machine. Most programmers and optimizing compilers can take advantage of this feature.
2. Sixteen registers are available for on-chip storage of local variables which can transfer to the stack for computation. The accessing of variables is three to four times as fast as available on a strictly stack machine.

The combined stack **74**/register **134** architecture has not been used previously due to inadequate understanding by computer designers of optimizing compilers and the mix of transfer versus math/logic instructions.

ADAPTIVE MEMORY CONTROLLER

A microprocessor must be designed to work with small or large memory configurations. As more memory loads are added to the data, address, and control lines, the switching speed of the signals slows down. The microprocessor **50** multiplexes the address/data bus three ways, so timing between the phases is critical. A traditional approach to the problem allocates a wide margin of time between bus phases so that systems will work with small or large numbers of memory chips connected. A speed compromise of as much as 50% is required.

As shown in FIG. **14**, the microprocessor **50** uses a feedback technique to allow the processor to adjust memory bus timing to be fast with small loads and slower with large ones. The OUTPUT ENABLE (OE) line **152** from the microprocessor **50** is connected to all memories **150** on the circuit board. The loading on the output enable line **152** to the microprocessor **50** is directly related to the number of memories **150** connected. By monitoring how rapidly OE **152** goes high after a read, the microprocessor **50** is able to determine when the data hold time has been satisfied and place the next address on the bus.

The level of the OE line **152** is monitored by CMOS input buffer **410** which generates an internal READY signal on line **412** to the microprocessor's memory controller. Curves **414** and **416** of the FIG. **15** graph show the difference in rise time likely to be encountered from a lightly to heavily loaded memory system. When the OE line **152** has reached a predetermined level to generate the READY signal, driver **418** generates an OUTPUT ENABLE signal on OE line **152**.

SKIP WITHIN THE INSTRUCTION CACHE

The microprocessor **50** fetches four 8-bit instructions each memory cycle and stores them in a 32-bit instruction register **108**, as shown in FIG. **16**. A class of "test and skip" instructions can very rapidly execute a very fast jump operation within the four instruction cache.

SKIP CONDITIONS:

Always

ACC non-zero

ACC negative

Carry flag equal logic one

Never

ACC equal zero

ACC positive

Carry flag equal logic zero

The SKIP instruction can be located in any of the four byte positions **420** in the 32-bit instruction register **108**. If the test is successful, SKIP will jump over the remaining one, two, or three 8-bit instructions in the instruction register **108** and cause the next four-instruction group to be loaded into the register **108**. As shown, the SKIP operation is implemented by resetting the 2-bit microinstruction counter **180** to zero on line **422** and simultaneously latching the next instruction group into the register **108**. Any instructions following the SKIP in the instruction register are overwritten by the new instructions and not executed.

The advantage of SKIP is that optimizing compilers and smart programmers can often use it in place of the longer conditional JUMP instruction. SKIP also makes possible microloops which exit when the loop counts down or when the SKIP jumps to the next instruction group. The result in very fast code.

Other machines (such as the PDP-8 and Data General NOVA) provide the ability to skip a single instruction. The microprocessor **50** provides the ability to skip up to three instructions.

MICROLOOP IN THE INSTRUCTION CACHE

The microprocessor **50** provides the MICROLOOP instruction to execute repetitively from one to three instructions residing in the instruction register **108**. The microloop instruction works in conjunction with the LOOP COUNTER **92** (FIG. **2**) connected to the internal data bus **90**. To execute a microloop, the program stores a count in LOOP COUNTER **92**. MICROLOOP may be placed in the first, second, third, or last byte **420** of the instruction register **108**. If placed in the first position, execution will just create a delay equal to the number stored in LOOP COUNTER **92** times the machine cycle. If placed in the second, third, or last byte **420**, when the microloop instruction is executed, it will test the LOOP COUNT for zero. If zero, execution will continue with the next instruction. If not zero, the LOOP COUNTER **92** is decremented and the 2-bit microinstruction counter is cleared, causing the preceding instructions in the instruction register to be executed again.

Microloop is useful for block move and search operations. By executing a block move completely out of the instruction register **108**, the speed of the move is doubled, since all memory cycles are used by the move rather than being shared with instruction fetching. Such a hardware implementation of microloops is much faster than conventional software implementation of a comparable function.

OPTIMAL CPU CLOCK SCHEME

The designer of a high speed microprocessor must produce a product which operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing. Temperature, voltage, and process all affect transistor propagation delays. Traditional CPU designs are done so that with the worse case of the three parameters, the circuit will function at the rated clock speed. The result are designs that must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse case conditions.

The microprocessor **50** uses the technique shown in FIGS. **17–19** to generate the system clock and its required phases. Clock circuit **430** is the familiar "ring oscillator" used to test process performance. The clock is fabricated on the same silicon chip as the rest of the microprocessor **50**.

The ring oscillator frequency is determined by the parameters of temperature, voltage, and process. At room temperature, the frequency will be in the neighborhood of 100 MHZ. At 70 degrees Centigrade, the speed will be 50 MHZ. The ring oscillator **430** is useful as a system clock, with its stages **431** producing phase 0-phase 3 outputs **433** shown in FIG. **19**, because its performance tracks the parameters which similarly affect all other transistors on the same silicon die. By deriving system timing from the ring

oscillator **430**, CPU **70** will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor **50** will operate slower than normal. Since the microprocessor **50** ring oscillator clock **430** is made from the same transistors on the same die as the latches and gates, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.

ASYNCHRONOUS/SYNCHRONOUS CPU

Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor **50** provides a dual-clock scheme as shown in FIG. **17**, with the CPU **70** operating a synchronously to I/O interface **432** forming part of memory controller **118** (FIG. **2**) and the I/O interface **432** operating synchronously with the external world of memory and I/O devices. The CPU **70** executes at the fastest speed possible using the adaptive ring counter clock **430**. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor **50** for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface **432**, speed of which is controlled by a conventional crystal clock **434**. The interface **432** processes requests for memory accesses from the microprocessor **50** and acknowledges the presence of I/O data. The microprocessor **50** fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU **70** from the fixed speed of the I/O interface **432**, optimum performance can be achieved by each. Recoupling between the CPU **70** and the interface **432** is accomplished with handshake signals on lines **436**, with data/addresses passing on bus **90**, **136**.

ASYNCHRONOUS/SYNCHRONOUS CPU IMBEDDED ON A DRAM CHIP

System performance is enhanced even more when the DRAM **311** and CPU **314** (FIG. **9**) are located on the same die. The proximity of the transistors means that DRAM **311** and CPU **314** parameters will closely follow each other. At room temperature, not only would the CPU **314** execute at 100 MHZ, but the DRAM **311** would access fast enough to keep up. The synchronization performed by the I/O interface **432** would be for DMA and reading and writing I/O ports. In some systems (such as calculators) no I/O synchronization at all would be required, and the I/O clock would be tied to the ring counter clock.

VARIABLE WIDTH OPERANDS

Many microprocessors provide variable width operands. The microprocessor **50** handles operands of 8, 16, or 24 bits using the same op-code. FIG. **20** shows the 32-bit instruction register **108** and the 2-bit microinstruction register **180** which selects the 8-bit instruction. Two classes of microprocessor **50** instructions can be greater than 8-bits, JUMP class and IMMEDIATE. A JUMP or IMMEDIATE op-code is 8-bits, but the operand can be 8, 16, or 24 bits long. This magic is possible because operands must be right justified in the instruction register. This means that the least significant bit of the operand is always located in the least significant bit of the instruction register. The microinstruction counter **180** selects which 8-bit instruction to execute. If a JUMP or IMMEDIATE instruction is decoded, the state of the 2-bit microinstruction counter selects the required 8, 16, or 24 bit operand onto the address or data bus. The unselected 8-bit bytes are loaded with zeros by operation of decoder **440** and gates **442**. The advantage of this technique is the saving of a number of op-codes required to specify the different operand sizes in other microprocessors.

TRIPLE STACK CACHE

Computer performance is directly related to the system memory bandwidth. The faster the memories, the faster the computer. Fast memories are expensive, so techniques have been developed to move a small amount of high-speed memory around to the memory addresses where it is needed. A large amount of slow memory is constantly updated by the fast memory, giving the appearance of a large fast memory array. A common implementation of the technique is known as a high-speed memory cache. The cache may be thought of as fast acting shock absorber smoothing out the bumps in memory access. When more memory is required than the shock can absorb, it bottoms out and slow speed memory is accessed. Most memory operations can be handled by the shock absorber itself.

The microprocessor **50** architecture has the ALU **80** (FIG. **2**) directly coupled to the top two stack locations **76** and **78**. The access time of the stack **74** therefore directly affects the execution speed of the processor. The microprocessor **50** stack architecture is particularly suitable to a triple cache technique, shown in FIG. **21** which offers the appearance of a large stack memory operating at the speed of on-chip latches **450**. Latches **450** are the fastest form of memory device built on the chip, delivering data in as little as 3 nsec. However latches **450** require large numbers of transistors to construct. On-chip RAM **452** requires fewer transistors than latches, but is slower by a factor of five (15 nsec access). Off-chip RAM **150** is the slowest storage of all. The microprocessor **50** organizes the stack memory hierarchy as three interconnected stacks **450**, **452** and **454**. The latch stack **450** is the fastest and most frequently used. The on-chip RAM stack **452** is next. The off-chip RAM stack **454** is slowest. The stack modulation determines the effective access time of the stack. If a group of stack operations never push or pull more than four consecutive items on the stack, operations will be entirely performed in the 3 nsec latch stack. When the four latches **456** are filled, the data in the bottom of the latch stack **450** is written to the top of the on-chip RAM stack **452**. When the sixteen locations **458** in the on-chip RAM stack **452** are filled, the data in the bottom of the on-chip RAM stack **452** is written to the top of the off-chip RAM stack **454**. When popping data off a full stack **450**, four pops will be performed before stack empty line **460** from the latch stack pointer **462** transfers data from the on-chip RAM stack **452**. By waiting for the latch stack **450** to empty before performing the slower on-chip RAM access, the high effective speed of the latches **456** are made available to the processor. The same approach is employed with the on-chip RAM stack **452** and the off-chip RAM stack **454**.

POLYNOMIAL GENERATION INSTRUCTION

Polynomials are useful for error correction, encryption, data compression, and fractal generation. A polynomial is generated by a sequence of shift and exclusive OR operations. Special chips are provided for this purpose in the prior art.

The microprocessor **50** is able to generate polynomials at high speed without external hardware by slightly modifying how the ALU **80** works. As shown in FIG. **21**, a polynomial is generated by loading the "order" (also known as the feedback terms) into C Register **470**. The value thirty one (resulting in 32 iterations) is loaded into DOWN COUNTER **472**. A register **474** is loaded with zero. B register **476** is loaded with the starting polynomial value. When the POLY

instruction executes, C register **470** is exclusively ORed with A register **474** if the least significant bit of B register **476** is a one. Otherwise, the contents of the A register **474** passes through the ALU **80** unaltered. The combination of A and B is then shifted right (divided by 2) with shifters **478** and **480**. The operation automatically repeats the specified number of iterations, and the resulting polynomial is left in A register **474**.

FAST MULTIPLY

Most microprocessors offer a 16×16 or 32×32 bit multiply instruction. Multiply when performed sequentially takes one shift/add per bit, or 32 cycles for 32 bit data. The microprocessor **50** provides a high speed multiply which allows multiplication by small numbers using only a small number of cycles. FIG. **23** shows the logic used to implement the high speed algorithm. To perform a multiply, the size of the multiplier less one is placed in the DOWN COUNTER **472**. For a four bit multiplier, the number three would be stored in the DOWN COUNTER **472**. Zero is loaded into the A register **474**. The multiplier is written bit reversed into the B Register **476**. For example, a bit reversed five (binary 0101) would be written into B as 1010. The multiplicand is written into the C register **470**. Executing the FAST MULT instruction will leave the result in the A Register **474**, when the count has been completed. The fast multiply instruction is important because many applications scale one number by a much smaller number. The difference in speed between multiplying a 32×32 bit and a 32×4 bit is a factor of 8. If the least significant bit of the multiplier is a "ONE", the contents of the A register **474** and the C register **470** are added. If the least significant bit of the multiplier is a "ZERO", the contents of the A register are passed through the ALU **80** unaltered. The output of the ALU **80** is shifted left by shifter **482** in each iteration. The contents of the B register **476** are shifted right by the shifter **480** in each iteration.

INSTRUCTION EXECUTION PHILOSOPHY

The microprocessor **50** uses high speed D latches in most of the speed critical areas. Slower on-chip RAM is used as secondary storage.

The microprocessor **50** philosophy of instruction execution is to create a hierarchy of speed as follows:

Logic and D latch transfers	1 cycle	20 nsec
Math	2 cycles	40 nsec
Fetch/store on-chip RAM	2 cycles	40 nsec
Fetch/store in current RAS page	4 cycles	80 nsec
Fetch/store with RAS cycle	11 cycles	220 nsec

With a 50 MHZ clock, many operations can be performed in 20 nsec. and almost everything else in 40 nsec.

To maximize speed, certain techniques in processor design have been used. They include:

Eliminating arithmetic operations on addresses,

Fetching up to four instructions per memory cycle,

Pipelineless instruction decoding

Generating results before they are needed,

Use of three level stack caching.

PIPELINE PHILOSOPHY

Computer instructions are usually broken down into sequential pieces, for example: fetch, decode, register read, execute, and store. Each piece will require a single machine cycle. In most Reduced Instruction Set Computer (RISC) chips, instruction require from three to six cycles.

RISC instructions are very parallel. For example, each of 70 different instructions in the SPARC (SUN Computer's RISC chip) has five cycles. Using a technique called "pipelining", the different phases of consecutive instructions can be overlapped.

To understand pipelining, think of building five residential homes. Each home will require in sequence, a foundation, framing, plumbing and wiring, roofing, and interior finish. Assume that each activity takes one week. To build one house will take five weeks.

But what if you want to build an entire subdivision? You have only one of each work crew, but when the foundation men finish on the first house, you immediately start them on the second one, and so on. At the end of five weeks, the first home is complete, but you also have five foundations. If you have kept the framing, plumbing, roofing, and interior guys all busy, from five weeks on, a new house will be completed each week.

This is the way a RISC chip like SPARC appears to execute an instruction in a single machine cycle. In reality, a RISC chip is executing one fifth of five instructions each machine cycle. And if five instructions stay in sequence, an instruction will be completed each machine cycle.

The problems with a pipeline are keeping the pipe full with instructions. Each time an out of sequence instruction such as a BRANCH or CALL occurs, the pipe must be refilled with the next sequence. The resulting dead time to refill the pipeline can become substantial when many IF/THEN/ELSE statements or subroutines are encountered.

THE PIPELINE APPROACH

The microprocessor **50** has no pipeline as such. The approach of this microprocessor to speed is to overlap instruction fetching with execution of the previously fetched instruction(s). Beyond that, over half the instructions (the most common ones) execute entirely in a single machine cycle of 20 nsec. This is possible because:

1. Instruction decoding resolves in 2.5 nsec.
2. Incremented/decremented and some math values are calculated before they are needed, requiring only a latching signal to execute.
3. Slower memory is hidden from high speed operations by high-speed D latches which access in 4 nsec.

The disadvantage for this microprocessor is a more complex chip design process. The advantage for the chip user is faster ultimate throughput since pipeline stalls cannot exist. Pipeline synchronization with availability flag bits and other such pipeline handling is not required by this microprocessor.

For example, in some RISC machines an instruction which tests a status flag may have to wait for up to four cycles for the flag set by the previous instruction to be available to be tested. Hardware and software debugging is also somewhat easier because the user doesn't have to visualize five instructions simultaneously in the pipe.

OVERLAPPING INSTRUCTION FETCH/EXECUTE

The slowest procedure the microprocessor **50** performs is to access memory. Memory is accessed when data is read or written. Memory is also read when instructions are fetched. The microprocessor **50** is able to hide fetch of the next instruction behind the execution of the previously fetched instruction(s). The microprocessor **50** fetches instructions in 4-byte instruction groups. An instruction group may contain from one to four instructions. The amount of time required to execute the instruction group ranges from 4 cycles for simple instructions to 64 cycles for a multiply.

When a new instruction group is fetched, the microprocessor instruction decoder looks at the most significant bit of all four of the bytes. The most significant bit of an instruction determines if a memory access is required. For example, CALL, FETCH, and STORE all require a memory access to

execute. If all four bytes have nonzero most significant bits, the microprocessor initiates the memory fetch of the next sequential 4-byte instruction group. When the last instruction in the group finishes executing, the next 4-byte instruction group is ready and waiting on the data bus needing only to be latched into the instruction register. If the 4-byte instruction group required four or more cycles to execute and the next sequential access was a column address strobe (CAS) cycle, the instruction fetch was completely overlapped with execution.

INTERNAL ARCHITECTURE

The microprocessor **50** architecture consists of the following:

PARAMETER STACK	<---> ALU* <--->	Y REGISTER RETURN STACK
<---32 BITS---> 16 DEEP		<---32 BITS---> 16 DEEP
Used for math and logic.		Used for subroutine and interrupt return addresses as well as local variables.
Push down stack. Can overflow into off-chip RAM.		Push down stack. Can overflow into off-chip RAM. Can also be accessed relative to top of stack.
LOOP COUNTER	(32-bits, can decrement by 1) Used by class of test and loop instructions.	
X REGISTER	(32-bits, can increment or decrement by 4). Used to point to RAM locations.	
PROGRAM COUNTER	(32-bits, increments by 4). Points to 4-byte instruction groups in RAM.	
INSTRUCTION REG	(32-Bits). Holds 4-byte instruction groups while they are being decoded and executed.	

MODE - A register with mode and status bits.

MODE-BITS:

- Slow down memory accesses by 8 if "1". Run full speed if "0". (Provided for access to slow EPROM.)
- Divide the system clock by 1023 if "1" to reduce power consumption. Run full speed if "0". (On-chip counters slow down if this bit is set.)
- Enable external interrupt 1.
- Enable external interrupt 2.
- Enable external interrupt 3.
- Enable external interrupt 4.
- Enable external interrupt 5.
- Enable external interrupt 6.
- Enable external interrupt 7.

ON-CHIP MEMORY LOCATIONS:

MODE-BITS	
DMA-POINTER	
DMA-COUNTER	
STACK-POINTER	- Pointer into Parameter Stack.
STACK-DEPTH	- Depth of on-chip Parameter Stack
RSTACK-POINTER	- Pointer into Return Stack
RSTACK-DEPTH	- Depth of on-chip Return Stack

*Math and logic operations use the TOP item and NEXT to top Parameter Stack items as the operands. The result is pushed onto the Parameter Stack. *Return addresses from subroutines are placed on the Return Stack. The Y REGISTER is used as a pointer to RAM locations. Since the Y REGISTER is the top item of the Return Stack, nesting of indices is straightforward.

ADDRESSING MODE HIGH POINTS

The data bus is 32-bits wide. All memory fetches and stores are 32-bits. Memory bus addresses are 30 bits. The least significant 2 bits are used to select one-of-four bytes in some addressing modes. The Program Counter, X Register, and Y Register are implemented as D latches with their outputs going to the memory address bus and the bus incrementer/decrementer. Incrementing one of these registers can happen quickly, because the incremented value has already rippled through the inc/dec logic and need only be clocked into the latch. Branches and Calls are made to 32-bit word boundaries.

INSTRUCTION SET

32-BIT INSTRUCTION FORMAT

The thirty two bit instructions are CALL, BRANCH, BRANCH-IF-ZERO, and LOOP-IF-NOT-DONE. These instructions require the calculation of an effective address. In many computers, the effective address is calculated by adding or subtracting an operand with the current Program Counter. This math operation requires from four to seven machine cycles to perform and can definitely bog down machine execution. The microprocessor's strategy is to perform the required math operation at assembly or linking time and do a much simpler "Increment to next page" or "Decrement to previous page" operation at run time. As a result, the microprocessor branches execute in a single cycle.

24-BIT OPERAND FORM:

Byte 1	Byte 2	Byte 3	Byte 4
WWWWWW XX -	YYYYYYYY -	YYYYYYYY -	YYYYYYYY

With a 24-bit operand, the current page is considered to be defined by the most significant 6 bits of the Program Counter.

16-BIT OPERAND FORM: QQQQQQQQ-WWWWWW XX-YYYYYYYY-YYYYYYYY With a 16-bit operand, the current page is considered to be defined by the most significant 14 bits of the Program Counter.

8-BIT OPERAND FORM: QQQQQQQQ-QQQQQQQQ-WWWWWW XX-YYYYYYYY With an 8-bit operand, the current page is considered to be defined by the most significant 22 bits of the Program Counter.

QQQQQQQQ—Any 8-bit instruction.

WWWWWW—Instruction op-code.

XX—Select how the address bits will be used:

00—Make all high-order bits zero. (Page zero addressing)

01—Increment the high-order bits. (Use next page)

10—Decrement the high-order bits. (Use previous page)

11—Leave the high-order bits unchanged. (Use current page)

YYYYYYYY—The address operand field. This field is always shifted left two bits (to generate a word rather than byte address) and loaded into the Program Counter. The microprocessor instruction decoder figures out the width of the operand field by the location of the instruction op-code in the four bytes.

The compiler or assembler will normally use the shortest operand required to reach the desired address so that the leading bytes can be used to hold other instructions. The effective address is calculated by combining:

The current Program Counter,

The 8, 16, or 24 bit address operand in the instruction,

Using one of the four allowed addressing modes.

EXAMPLES OF EFFECTIVE ADDRESS CALCULATION

Example 1

Byte 1	Byte 2	Byte 3	Byte 4
QQQQQQQQ	QQQQQQQQ	00000011	10011000

The "QQQQQQQQs" in Byte 1 and 2 indicate space in the 4-byte memory fetch which could be hold two other

instructions to be executed prior to the CALL instruction. Byte 3 indicates a CALL instruction (six zeros) in the current page (indicated by the 11 bits). Byte 4 indicates that the hexadecimal number **98** will be forced into the Program Counter bits **2** through **10**. (Remember, a CALL or BRANCH always goes to a word boundary so the two least significant bits are always set to zero). The effect of this instruction would be to CALL a subroutine at WORD location HEX 98 in the current page. The most significant 22 bits of the Program Counter define the current page and will be unchanged.

Example 2

Byte 1	Byte 2	Byte 3	Byte 4
000001 01	00000001	00000000	00000000

If we assume that the Program Counter was HEX 0000 0156 which is binary:

00000000 00000000 00000001 01010110=OLD PROGRAM COUNTER.

Byte 1 indicates a BRANCH instruction op code (000001) and "01" indicates select the next page. Byte 2,3, and 4 are the address operand. These 24-bits will be shifted to the left two places to define a WORD address. HEX 0156 shifted left two places is HEX 0558. Since this is a 24-bit operand instruction, the most significant 6 bits of the Program Counter define the current page. These six bits will be incremented to select the next page. Executing this instruction will cause the Program Counter to be loaded with HEX 0400 0558 which is binary:

00000100 00000000 00000101 01011000=NEW PROGRAM COUNTER.

INSTRUCTIONS

CALL-LONG

0000 00XX-YYYYYYYY-YYYYYYYY-YYYYYYYY

Load the Program Counter with the effective WORD address specified. Push the current PC contents onto the RETURN STACK.

OTHER EFFECTS: CARRY or modes, no effect. May cause Return Stack to force an external memory cycle if on-chip Return Stack is full.

BRANCH

0000 01XX-YYYYYYYY-YYYYYYYY-YYYYYYYY

Load the Program Counter with the effective WORD address specified.

OTHER EFFECTS: NONE

BRANCH-IF-ZERO

0000 10XX-YYYYYYYY-YYYYYYYY-YYYYYYYY

Test the TOP value on the Parameter Stack. If the value is equal to zero, load the Program Counter with the effective WORD address specified. If the TOP value is not equal to zero, increment the Program Counter and fetch and execute the next instruction.

OTHER EFFECTS: NONE

LOOP-IF-NOT-DONE

0000 11YY-(XXXX XXXX)-(XXXX XXXX)-(XXXX XXXX)

If the LOOP COUNTER is not zero, load the Program Counter with the effective WORD address specified. If the LOOP COUNTER is zero, decrement the LOOP COUNTER, increment the Program Counter and fetch and execute the next instruction.

OTHER EFFECTS: NONE

8-BIT INSTRUCTIONS PHILOSOPHY

Most of the work in the microprocessor **50** is done by the 8-bit instructions. Eight bit instructions are possible with the microprocessor because of the extensive use of implied stack addressing. Many 32-bit architectures use 8-bits to specify the operation to perform but use an additional 24-bits to specify two sources and a destination.

For math and logic operations, the microprocessor **50** exploits the inherent advantage of a stack by designating the source operand(s) as the top stack item and the next stack item. The math or logic operation is performed, the operands are popped from the stack, and the result is pushed back on the stack. The result is a very efficient utilization of instruction bits as well as registers. A comparable situation exists between Hewlett Packard calculators (which use a stack) and Texas Instrument calculators which don't. The identical operation on an HP will require one half to one third the keystrokes of the TI.

The availability of 8-bit instructions also allows another architectural innovation, the fetching of four instructions in a single 32-bit memory cycle. The advantages of fetching multiple instructions are:

Increased execution speed even with slow memories,

Similar performance to the Harvard (separate data and instruction busses) without the expense,

Opportunities to optimize groups of instructions,

The capability to perform loops within this mini-cache.

The microloops inside the four instruction group are effective for searches and block moves.

SKIP INSTRUCTIONS

The microprocessor **50** fetches instructions in 32-bit chunks called 4-byte instruction groups. These four bytes may contain four 8-bit instructions or some mix of 8-bit and 16 or 24-bit instructions. SKIP instructions in the microprocessor skip any remaining instructions in a 4-byte instruction group and cause a memory fetch to get the next 4-byte instruction group. Conditional SKIPs when combined with 3-byte BRANCHES will create conditional BRANCHES. SKIPs may also be used in situations when no use can be made of the remaining bytes in a 4-instruction group. A SKIP executes in a single cycle, whereas a group of three NOPs would take three cycles.

SKIP-ALWAYS—Skip any remaining instructions in this 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group.

SKIP-IF-ZERO—If the TOP item of the Parameter Stack is zero, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is not zero, execute the next sequential instruction.

SKIP-IF-POSITIVE—If the TOP item of the Parameter Stack has a the most significant bit (the sign bit) equal to "0", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is not "0", execute the next sequential instruction.

SKIP-IF-NO-CARRY—If the CARRY flag from a SHIFT or arithmetic operation is not equal to "1", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the CARRY is equal to "1", execute the next sequential instruction.

SKIP-NEVER (NOP) execute the next sequential instruction. (Delay one machine cycle).

SKIP-IF-NOT-ZERO—If the TOP item on the Parameter Stack is not equal to "0", skip any remaining instructions

in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is equal "0", execute the next sequential instruction.

SKIP-IF-NEGATIVE—If the TOP item on the Parameter Stack has its most significant bit (sign bit) set to "1", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item has its most significant bit set to "0", execute the next sequential instruction.

SKIP-IF-CARRY—If the CARRY flag is set to "1" as a result of SHIFT or arithmetic operation, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the CARRY flag is "0", execute the next sequential instruction.

MICROLOOPS

Microloops are a unique feature of the microprocessor architecture which allows controlled looping within a 4-byte instruction group. A microloop instruction tests the LOOP COUNTER for "0" and may perform an additional test. If the LOOP COUNTER is not "0" and the test is met, instruction execution continues with the first instruction in the 4-byte instruction group, and the LOOP COUNTER is decremented. A microloop instruction will usually be the last byte in a 4-byte instruction group, but it can be any byte. If the LOOP COUNTER is "0" or the test is not met, instruction execution continues with the next instruction. If the microloop is the last byte in the 4-byte instruction group, the most significant 30-bits of the Program Counter are incremented and the next 4-byte instruction group is fetched from memory. On a termination of the loop on LOOP COUNTER equal to "0", the LOOP COUNTER will remain at "0". Microloops allow short iterative work such as moves and searches to be performed without slowing down to fetch instructions from memory.

EXAMPLE

Byte 1 FETCH-VIA-X-AUTO-INCREMENT	Byte 2 STORE-VIA-Y-AUTOINCREMENT
Byte 3 ULOOP-UNTIL-DONE	Byte 4 QQQQQQQQ

This example will perform a block move. To initiate the transfer, X will be loaded with the starting address of the source. Y will be loaded with the starting address of the destination. The LOOP COUNTER will be loaded with the number of 32-bit words to move. The microloop will FETCH and STORE and count down the LOOP COUNTER until it reaches zero. QQQQQQQQ indicates any instruction can follow.

MICROLOOP INSTRUCTIONS

ULOOP-UNTIL-DONE—If the LOOP COUNTER is not "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0", continue execution with the next instruction.

ULOOP-IF-ZERO—If the LOOP COUNTER is not "0" and the TOP item on the Parameter Stack is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULOOP-IF-POSITIVE—If the LOOP COUNTER is not "0" and the most significant bit (sign bit) is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULOOP-IF-NOT-CARRY-CLEAR—If the LOOP COUNTER is not "0" and the floating point exponents found in TOP and NEXT are not aligned, continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the exponents are aligned, continue execution with the next instruction. This instruction is specifically designed for combination with special SHIFT instructions to align two floating point numbers.

ULOOP-NEVER—(DECREMENT-LOOP-COUNTER) Decrement the LOOP COUNTER. Continue execution with the next instruction.

ULOOP-IF-NOT-ZERO—If the LOOP COUNTER is not "0" and the TOP item of the Parameter Stack is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULOOP-IF-NEGATIVE—If the LOOP COUNTER is not "0" and the most significant bit (sign bit) of the TOP item of the Parameter Stack is "1", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the most significant bit of the Parameter Stack is "0", continue execution with the next instruction.

ULOOP-IF-CARRY-SET—If the LOOP COUNTER is not "0" and the exponents of the floating point numbers found in TOP and NEXT are not aligned, continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the exponents are aligned, continue execution with the next instruction.

RETURN FROM SUBROUTINE OR INTERRUPT

Subroutine calls and interrupt acknowledgements cause a redirection of normal program execution. In both cases, the current Program Counter is pushed onto the Return Stack, so the microprocessor can return to its place in the program after executing the subroutine or interrupt service routine.

NOTE: When a CALL to subroutine or interrupt is acknowledged the Program Counter has already been incremented and is pointing to the 4-byte instruction group following the 4-byte group currently being executed. The instruction decoding logic allows the microprocessor to perform a test and execute a return conditional on the outcome of the test in a single cycle. A RETURN pops an address from the Return Stack and stores it to the Program Counter.

RETURN INSTRUCTIONS

RETURN-ALWAYS—Pop the top item from the Return Stack and transfer it to the Program Counter.

RETURN-IF-ZERO—If the TOP item on the Parameter Stack is "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-POSITIVE—If the most significant bit (sign bit) of the TOP item on the Parameter Stack is a "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-CARRY-CLEAR—If the exponents of the floating point numbers found in TOP and NEXT are not aligned, pop the top item from the Return Stack and

transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-NEVER (NOP)—Execute the next instruction.

RETURN-IF-NOT-ZERO—If the TOP item on the Parameter Stack is not "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-NEGATIVE—If the most significant bit (sign bit) of the TOP item on the Parameter Stack is a "1", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-CARRY-SET—If the exponents of the floating point numbers found in TOP and NEXT are aligned, pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

HANDLING MEMORY FROM DYNAMIC RAM

The microprocessor **50**, like any RISC type architecture, is optimized to handle as many operations as possible on-chip for maximum speed. External memory operations take from 80 nsec. to 220 nsec. compared with on-chip memory speeds of from 4 nsec. to 30 nsec. There are times when external memory must be accessed.

External memory is accessed using three registers:

X-REGISTER—A 30-bit memory pointer which can be used for memory access and simultaneously incremented or decremented.

Y-REGISTER—A 30-bit memory pointer which can be used for memory access and simultaneously incremented or decremented.

PROGRAM-COUNTER—A 30-bit memory pointer normally used to point to 4-byte instruction groups. External memory may be accessed at addresses relative to the PC. The operands are sometimes called "Immediate" or "Literal" in other computers. When used as memory pointer, the PC is also incremented after each operation.

MEMORY LOAD & STORE INSTRUCTIONS

FETCH-VIA-X—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. X is unchanged.

FETCH-VIA-Y—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. Y is unchanged.

FETCH-VIA-X-AUTOINCREMENT—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of X to point to the next 32-bit word address.

FETCH-VIA-Y-AUTOINCREMENT—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of Y to point to the next 32-bit word address.

FETCH-VIA-X-AUTODECREMENT—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. After fetching, decrement the most significant 30 bits of X to point to the previous 32-bit word address.

FETCH-VIA-Y-AUTODECREMENT—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. After fetching, decrement the most significant 30 bits of Y to point to the previous 32-bit word address.

STORE-VIA-X—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. X is unchanged.

STORE-VIA-Y—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. Y is unchanged.

STORE-VIA-X-AUTOINCREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. After storing, increment the most significant 30 bits of X to point to the next 32-bit word address.

STORE-VIA-Y-AUTOINCREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. After storing, increment the most significant 30 bits of Y to point to the next 32-bit word address.

STORE-VIA-X-AUTODECREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. After storing, decrement the most significant 30 bits of X to point to the previous 32-bit word address.

STORE-VIA-Y-AUTODECREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. After storing, decrement the most significant 30 bits of Y to point to the previous 32-bit word address.

FETCH-VIA-PC—Fetch the 32-bit memory content pointed to by the Program Counter and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of the Program Counter to point to the next 32-bit word address.

*NOTE When this instruction executes, the PC is pointing to the memory location following the instruction. The effect is of loading a 32-bit immediate operand. This is an 8-bit instruction and therefore will be combined with other 8-bit instructions in a 4-byte instruction fetch. It is possible to have from one to four FETCH-VIA-PC instructions in a 4-byte instruction fetch. The PC increments after each execution of FETCH-VIA-PC, so it is possible to push four immediate operands on the stack. The four operands would be the found in the four memory locations following the instruction.

BYTE-FETCH-VIA-X—Fetch the 32-bit memory content pointed to by the most significant 30 bits of X. Using the two least significant bits of X, select one of four bytes from the 32-bit memory fetch, right justify the byte in a 32-bit field and push the selected byte preceded by leading zeros onto the Parameter Stack.

BYTE-STORE-VIA-X—Fetch the 32-bit memory content pointed to by the most significant 30 bits of X. Pop the TOP item from the Parameter Stack. Using the two least significant bits of X place the least significant byte into the 32-bit memory data and write the 32-bit entity back to the location pointed to by the most significant 30 bits of X.

OTHER EFFECTS OF MEMORY ACCESS INSTRUCTIONS:

Any FETCH instruction will push a value on the Parameter Stack **74**. If the on-chip stack is full, the stack will overflow into off-chip memory stack resulting in an additional memory cycle. Any STORE instruction will pop a value from the Parameter Stack **74**. If the on-chip stack is empty, a memory cycle will be generated to fetch a value from off-chip memory stack.

HANDLING ON-CHIP VARIABLES

High-level languages often allow the creation of LOCAL VARIABLES. These variables are used by a particular procedure and discarded. In cases of nested procedures, layers of these variables must be maintained. On-chip storage is up to five times faster than off-chip RAM, so a means of keeping local variables on-chip can make operations run faster. The microprocessor **50** provides the capability for both on-chip storage of local variables and nesting of multiple levels of variables through the Return Stack.

The Return Stack **134** is implemented as 16 on-chip RAM locations. The most common use for the Return Stack **134** is storage of return addresses from subroutines and interrupt calls. The microprocessor allows these 16 locations to also be used as addressable registers. The 16 locations may be read and written by two instructions which indicate a Return Stack relative address from 0–15. When high-level procedures are nested, the current procedure variables push the previous procedure variables further down the Return Stack **134**. Eventually, the Return Stack will automatically overflow into off-chip RAM.

ON-CHIP VARIABLE INSTRUCTIONS

READ-LOCAL-VARIABLE XXXX—Read the XXXXth location relative to the top of the Return Stack. (XXXX is a binary number from 0000–1111). Push the item read onto the Parameter Stack.

OTHER EFFECTS: If the Parameter Stack is full, the push operation will cause a memory cycle to be generated as one item of the stack is automatically stored to external RAM. The logic which selects the location performs a modulo **16** subtraction. If four local variables have been pushed onto the Return Stack, and an instruction attempts to READ the fifth item, unknown data will be returned.

WRITE-LOCAL-VARIABLE XXXX—Pop the TOP item of the Parameter Stack and write it into the XXXXth location relative to the top of the Return Stack. (XXXX is a binary number from 0000–1111.)

OTHER EFFECTS: If the Parameter Stack is empty, the pop operation will cause a memory cycle to be generated to fetch the Parameter Stack item from external RAM. The logic which selects the location performs a modulo **16** subtraction. If four local variables have been pushed onto the Return Stack, and an instruction attempts to WRITE to the fifth item, it is possible to clobber return addresses or wreak other havoc.

REGISTER AND FLIP-FLOP TRANSFER AND PUSH INSTRUCTIONS

DROP—Pop the TOP item from the Parameter Stack and discard it.

SWAP—Exchange the data in the TOP Parameter Stack location with the data in the NEXT Parameter Stack location.

DUP—Duplicate the TOP item on the Parameter Stack and push it onto the Parameter Stack.

PUSH-LOOP-COUNTER—Push the value in LOOP COUNTER onto the Parameter Stack.

POP-RSTACK-PUSH-TO-STACK—Pop the top item from the Return Stack and push it onto the Parameter Stack.

PUSH-X-REG—Push the value in the X Register onto the Parameter Stack.

PUSH-STACK-POINTER—Push the value of the Parameter Stack pointer onto the Parameter Stack.

PUSH-RSTACK-POINTER—Push the value of the Return Stack pointer onto the Return Stack.

PUSH-MODE-BITS—Push the value of the MODE REGISTER onto the Parameter Stack.

PUSH-INPUT—Read the 10 dedicated input bits and push the value (right justified and padded with leading zeros) onto the Parameter Stack.

SET-LOOP-COUNTER—Pop the TOP value from the Parameter Stack and store it into LOOP COUNTER.

POP-STACK-PUSH-TO-RSTACK—Pop the TOP item from the Parameter Stack and push it onto the Return Stack.

SET-X-REG—Pop the TOP item from the Parameter Stack and store it into the X Register.

SET-STACK-POINTER—Pop the TOP item from the Parameter Stack and store it into the Stack Pointer.

SET-RSTACK-POINTER—Pop the TOP item from the Parameter

Stack and store it into the Return Stack Pointer.

SET-MODE-BITS—Pop the TOP value from the Parameter Stack and store it into the MODE BITS.

SET-OUTPUT—Pop the TOP item from the Parameter Stack and output it to the 10 dedicated output bits.

OTHER EFFECTS: Instructions which push or pop the Parameter Stack or Return Stack may cause a memory cycle as the stacks overflow back and forth between on-chip and off-chip memory.

LOADING A SHORT LITERAL

A special case of register transfer instruction is used to push an 8-bit literal onto the Parameter Stack. This instruction requires that the 8-bits to be pushed reside in the last byte of a 4-byte instruction group. The instruction op-code loading the literal may reside in ANY of the other three bytes in the instruction group.

EXAMPLE

BYTE 1 LOAD-SHORT-LITERAL BYTE 4 00001111	BYTE 2 QQQQQQQQ	BYTE 3 QQQQQQQQ

In this example, QQQQQQQQ indicates any other 8-bit instruction. When Byte 1 is executed, binary 00001111(HEX 0f) from Byte 4 will be pushed (right justified and padded by leading zeros) onto the Parameter Stack. Then the instructions in Byte 2 and Byte 3 will execute. The microprocessor instruction decoder knows not to execute Byte 4. It is possible to push three identical 8-bit values as follows:

BYTE 1 LOAD-SHORT-LITERAL BYTE 3 LOAD-SHORT-LITERAL SHORT-LITERAL-INSTRUCTION	BYTE 2 LOAD-SHORT-LITERAL BYTE 4 00001111

LOAD-SHORT-LITERAL—Push the 8-bit value found in Byte 4 of the current 4-byte instruction group onto the Parameter Stack.

LOGIC INSTRUCTIONS

Logical and math operations used the stack for the source of one or two operands and as the destination for results. The stack organization is a particularly convenient arrangement for evaluating expressions. TOP indicates the top value on the Parameter Stack **74**. NEXT indicates the next to top value on the Parameter Stack **74**.

AND—Pop TOP and NEXT from the Parameter Stack, perform the logical AND operation on these two operands, and push the result onto the Parameter Stack.

OR—Pop TOP and NEXT from the Parameter Stack, perform the logical OR operation on these two operands, and push the result onto the Parameter Stack.

XOR—Pop TOP and NEXT from the Parameter Stack, perform the logical exclusive OR on these two operands, and push the result onto the Parameter Stack.

BIT-CLEAR—Pop TOP and NEXT from the Parameter Stack, toggle all bits in NEXT, perform the logical AND operation on TOP, and push the result onto the Parameter Stack. (Another way of understanding this instruction is thinking of it as clearing all bits in TOP that are set in NEXT.)

MATH INSTRUCTIONS

Math instruction pop the TOP item and NEXT to top item of the Parameter Stack **74** to use as the operands. The results are pushed back on the Parameter Stack. The CARRY flag is used to latch the "33rd bit" of the ALU result.

ADD—Pop the TOP item and NEXT to top item from the Parameter Stack, add the values together and push the result back on the Parameter Stack. The CARRY flag may be changed.

ADD-WITH-CARRY—Pop the TOP item and the NEXT to top item from the Parameter Stack, add the values together. If the CARRY flag is "1" increment the result. Push the ultimate result back on the Parameter Stack. The CARRY flag may be changed.

ADD-X—Pop the TOP item from the Parameter Stack and read the third item from the top of the Parameter Stack. Add the values together and push the result back on the Parameter Stack. The CARRY flag may be changed.

SUB—Pop the TOP item and NEXT to top item from the Parameter Stack, Subtract NEXT from TOP and push the result back on the Parameter Stack. The CARRY flag may be changed.

SUB-WITH-CARRY—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP. If the CARRY flag is "1" increment the result. Push the ultimate result back on the Parameter Stack. The CARRY flag may be changed.

SUB-X—

SIGNED-MULT-STEP—

UNSIGNED-MULT-STEP—

SIGNED-FAST-MULT—

FAST-MULT-STEP—

UNSIGNED-DIV-STEP—

GENERATE-POLYNOMIAL—

ROUND—

COMPARE—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP. If the result has the most significant bit equal to "0" (the result is positive), push the result onto the Parameter Stack. If the result has the most significant bit equal to "1" (the result is negative), push the old value of TOP onto the Parameter Stack. The CARRY flag may be affected.

SHIFT/ROTATE

SHIFT-LEFT—Shift the TOP Parameter Stack item left one bit. The CARRY flag is shifted into the least significant bit of TOP.

SHIFT-RIGHT—Shift the TOP Parameter Stack item right one bit. The least significant bit of TOP is shifted into the CARRY flag. Zero is shifted into the most significant bit of TOP.

DOUBLE-SHIFT-LEFT—Treating the TOP item of the Parameter Stack as the most significant word of a 64-bit number and the NEXT stack item as the least significant word, shift the combined 64-bit entity left one bit. The CARRY flag is shifted into the least significant bit of NEXT.

DOUBLE-SHIFT-RIGHT—Treating the TOP item of the Parameter Stack as the most significant word of a 64-bit number and the NEXT stack item as the least significant word, shift the combined 64-bit entity right one bit. The least significant bit of NEXT is shifted into the CARRY flag. Zero is shifted into the most significant bit of TOP.

OTHER INSTRUCTIONS

FLUSH-STACK—Empty all on-chip Parameter Stack locations into off-chip RAM. (This instruction is useful for multitasking applications). This instruction accesses a counter which holds the depth of the on-chip stack and can require from none to 16 external memory cycles.

FLUSH-RSTACK—Empty all on-chip Return Stack locations into off-chip RAM. (This instruction is useful for multitasking applications). This instruction accesses a counter which holds the depth of the on-chip Return Stack and can require from none to 16 external memory cycles.

It should further be apparent to those skilled in the art that various changes in form and details of the invention as shown and described may be made. It is intended that such changes be included within the spirit and scope of the claims appended hereto.

What is claimed is:

1. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

2. The microprocessor system of claim **1** in which said second clock is a fixed frequency clock.

3. In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;

using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;

providing an on chip input/output interface for the microprocessor integrated circuit; and

clocking the input/output interface with a second clock independent of the ring oscillator system clock.

4. The method of claim **3** in which the second clock is a fixed frequency clock.

5. The method of claim **3** further including the step of:

transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.

6. A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and

the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

an on-chip input/output interface, connected between said said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

7. The microprocessor system of claim **6** wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

8. The microprocessor system of claim **6** wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

9. The microprocessor system of claim **6** wherein said oscillator comprises a ring oscillator.

10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

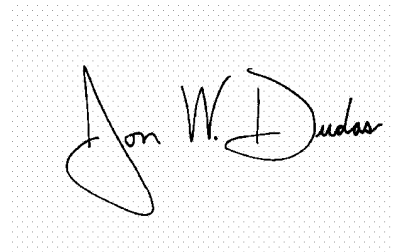
PATENT NO. : 5,809,336
APPLICATION NO. : 08/484918
DATED : September 15, 1998
INVENTOR(S) : Moore et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 34,
Line 25, delete "oscillator" and insert --variable speed clock--.

Signed and Sealed this

Twenty-second Day of May, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office

US005809336C1

(12) EX PARTE REEXAMINATION CERTIFICATE (7235th)

United States Patent

Moore et al.

(10) Number: US 5,809,336 C1

(45) Certificate Issued: Dec. 15, 2009

(54) **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

(75) Inventors: **Charles H. Moore**, Woodside, CA (US); **Russell H. Fish, III**, Mt. View, CA (US)

(73) Assignee: **Patriot Scientific Corporation**, San Diego, CA (US)

Reexamination Request:
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No. 90/008,237, Nov. 17, 2006
No. 90/008,474, Jan. 30, 2007

Reexamination Certificate for:

Patent No.:	**5,809,336**
Issued:	**Sep. 15, 1998**
Appl. No.:	**08/484,918**
Filed:	**Jun. 7, 1995**

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Related U.S. Application Data

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(51) **Int. Cl.**

G06F 7/76	(2006.01)
G06F 7/48	(2006.01)
G06F 12/08	(2006.01)
G06F 7/78	(2006.01)
G06F 9/30	(2006.01)
G06F 9/32	(2006.01)
G06F 15/76	(2006.01)
G06F 15/78	(2006.01)
G06F 7/52	(2006.01)
G06F 9/38	(2006.01)
G06F 7/58	(2006.01)

(52) **U.S. Cl.** **710/25**; 711/E12.02; 712/E9.016; 712/E9.028; 712/E9.046; 712/E9.055; 712/E9.057; 712/E9.058; 712/E9.062; 712/E9.078; 712/E9.08; 712/E9.081

(58) **Field of Classification Search** ..... None
See application file for complete search history.

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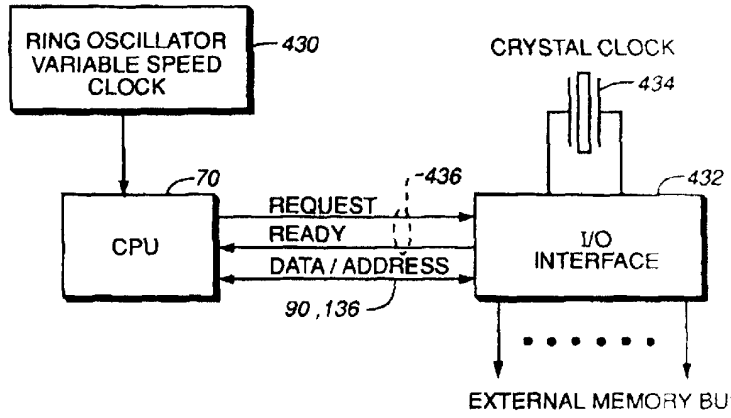
(Continued)

Primary Examiner—Sam Rimell

(57) **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.



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EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

ONLY THOSE PARAGRAPHS OF THE SPECIFICATION AFFECTED BY AMENDMENT ARE PRINTED HEREIN.

Column 17, lines 12–37:

Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor **50** provides a dual-clock scheme as shown in FIG. **17**, with the CPU **70** operating **[**a synchronously**]** *asynchronously* to I/O interface **432** forming part of memory controller **118** (FIG. **2**) and the I/O interface **432** operating synchronously with the external world of memory and I/O devices. The CPU **70** executes at the fastest speed possible using the adaptive ring counter clock **430**. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor **50** for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface **432**, speed of which is controlled by a conventional crystal clock **434**. The interface **432** processes requests for memory accesses from the microprocessor **50** and acknowledges the presence of I/O data. The microprocessor **50** fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU **70** from the fixed speed of the I/O interface **432**, optimum performance can be achieved by each. Recoupling between the CPU **70** and the interface **432** is accomplished with handshake signals on lines **436**, with data/addresses passing on bus **90**, **136**.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claims **3**–**5** and **8** are cancelled.

Claims **1**, **6** and **10** are determined to be patentable as amended.

Claims **2**, **7** and **9**, dependent on an amended claim, are determined to be patentable.

New claims **11**–**16** are added and determined to be patentable.

1. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, *wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.*

6. A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an *off-chip* external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an *off-chip* external clock, independent of said oscillator, connected to said input/output interface wherein said *off-chip* external clock is operative at a frequency independent of a clock frequency of said oscillator *and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.*

10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an **[**on chip**]** *on-chip* input/output interface between said central processing unit and an *off-chip* external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an *off-chip* external clock wherein said *off-chip* external clock is operative at a frequency independent of a clock frequency of said variable speed clock *and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.*

11. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein said central processing unit operates asynchronously to said input/output interface.

12. The microprocessor system of claim 11, in which said second clock is a fixed frequency clock.

13. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and further wherein said central processing unit operates asynchronously to said input/output interface.

14. The microprocessor system of claim 13 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

15. The microprocessor system of claim 13 wherein said oscillator comprises a ring oscillator.

16. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock, wherein said central processing unit operates asychronously to said input/output interface.

* * * * *

US005809336C2

(12) EX PARTE REEXAMINATION CERTIFICATE (7887th)

United States Patent

Moore et al.

(10) Number: US 5,809,336 C2

(45) Certificate Issued: Nov. 23, 2010

(54) **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

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(73) Assignee: **Charles H. Moore**, Incline Village, NV (US)

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(51) **Int. Cl.**

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G06F 7/48	(2006.01)
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G06F 7/78	(2006.01)
G06F 9/30	(2006.01)
G06F 9/32	(2006.01)
G06F 15/76	(2006.01)
G06F 15/78	(2006.01)
G06F 7/52	(2006.01)
G06F 9/38	(2006.01)
G06F 7/58	(2006.01)

(52) **U.S. Cl.** **710/25**; 711/E12.02; 712/E9.016; 712/E9.028; 712/E9.046; 712/E9.055; 712/E9.057; 712/E9.058; 712/E9.062; 712/E9.078; 712/E9.08; 712/E9.081

(58) **Field of Classification Search** ..... None
See application file for complete search history.

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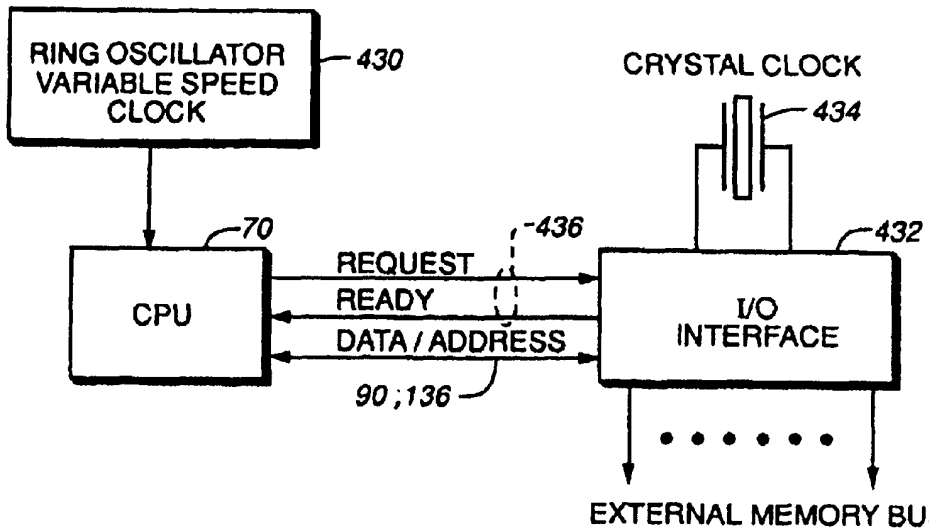
Primary Examiner—B. James Peikari

(57) **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and the ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.



EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

NO AMENDMENTS HAVE BEEN MADE TO THE PATENT

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims **1**, **2**, **6**, **7** and **9-16** is confirmed.

Claims **3-5** and **8** were previously cancelled.

* * * * *

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

Nos. 14-1076, -1317

CERTIFICATE OF SERVICE

I, Robyn Cocho, being duly sworn according to law and being over the age of 18, upon my oath depose and say that:

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