Teradyne, Inc.

The Dynamic World of Semiconductors and Implications for Test

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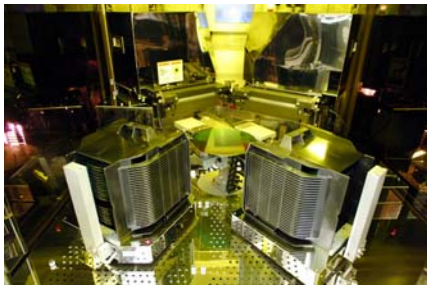
Overall Semiconductor Industry Trends

- Industry consolidation/partnerships/outsourcing growing
  - Design is King, Manufacturing technology less of a differentiator
  - Shared risks and costs of progress in face of complexity
  - Test methods are still IP, test execution increasingly outsourced.

- Lithography migration “velocity” is slowing
  - New nodes getting lower percentage of new designs
  - Devices rely on “multi-core” designs to increase performance
  - More testing complexity at protocol level, non-deterministic.



- Consumer Market is driving device roadmaps and volumes
  - Time to market becomes a key differentiator
  - Implies need for more streamlined design-to-test processes
  - Is test cost keeping up?

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Cost of Test Trends

- ATE Buy Rate Measures Productivity of Capital Expense
  - Calculated as Yearly ATE CAPEX/Semi Revenue

- ATE Buy Rate has been trending down for 20+ years

Lets look at the historical data!

Korea Test Conference June 2007

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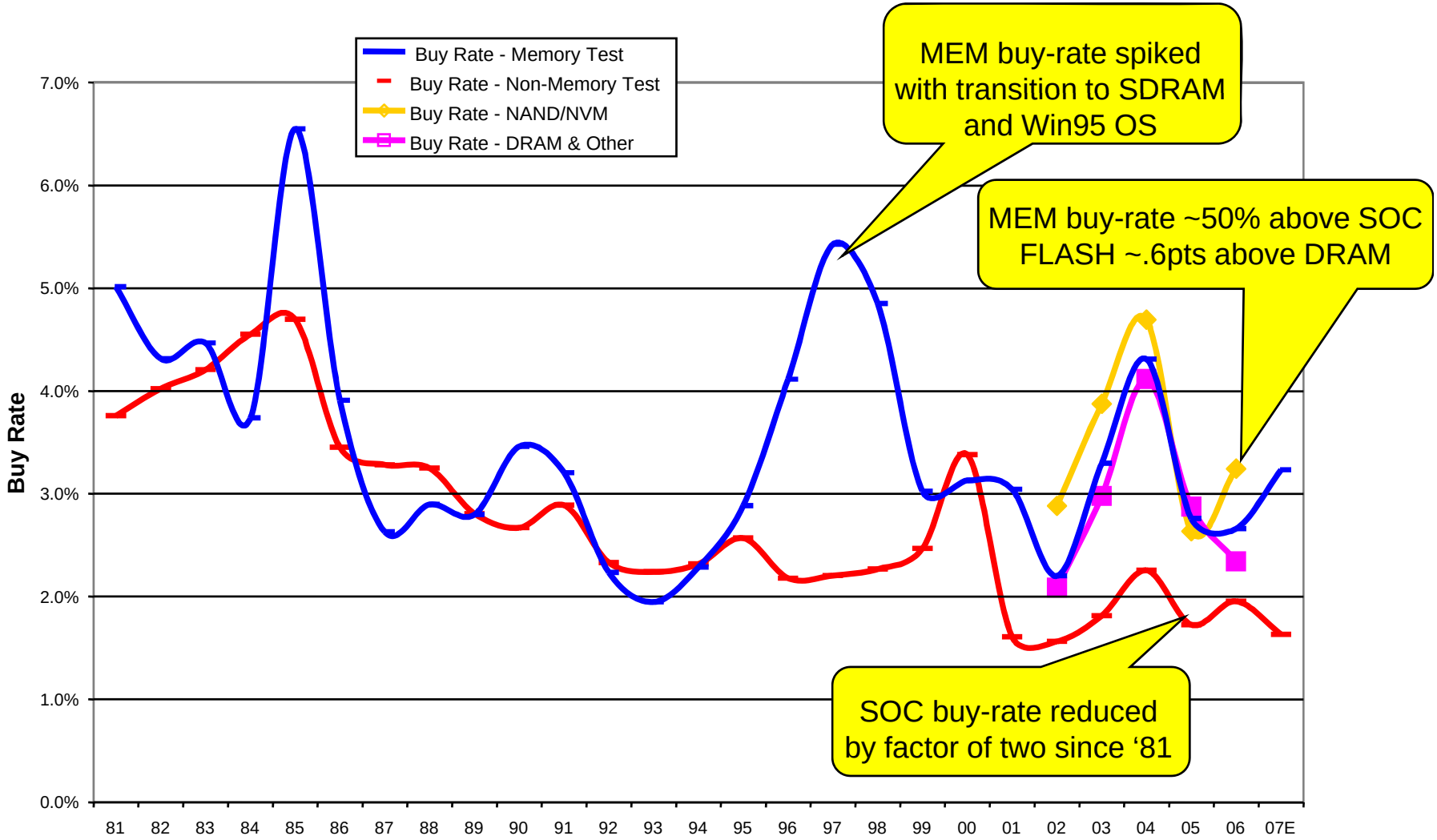
Historical Buy Rates in ATE



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CAPEX Productivity Improvement in Memory

- SOC CAPEX is More Efficient by Nearly 50%
  - ~2% vs ~3% buy rate

- Current Trends in Memory to Improve CAPEX Productivity
  - Reduced pin count test → Lower capital cost per site
  - Increased wafer level testing → Increase package test yield
  - Known Good Die test → Eliminate final test insertions
  - Single Touchdown wafer test → Reduced test time per wafer

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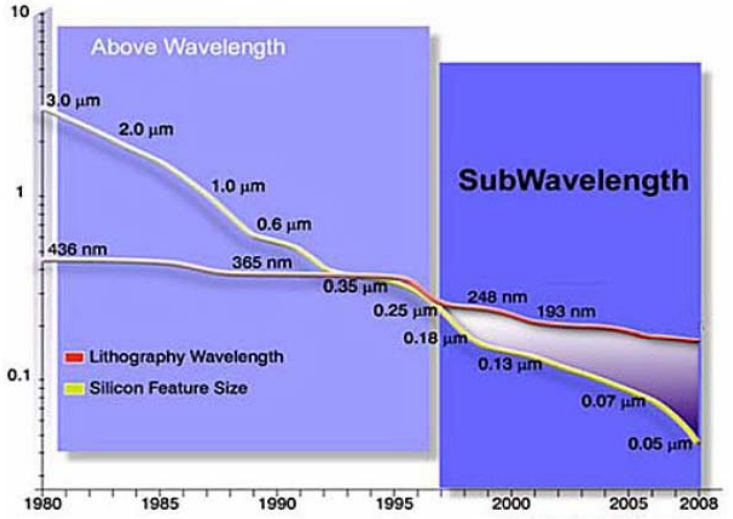
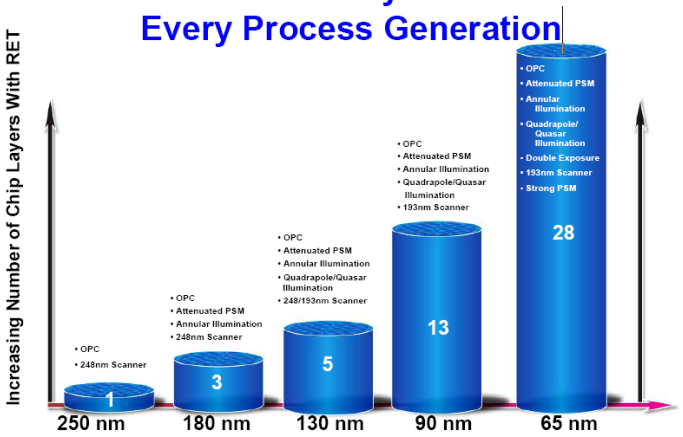
Lithography is getting more complex

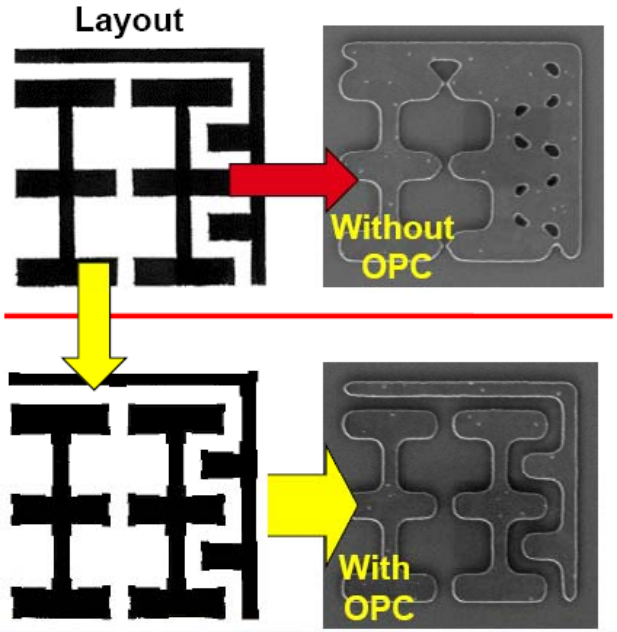
Growing Gap Between Lithography Wavelength and Feature Size



Number of RET Layers Increases Every Process Generation



What You Design Is Not What's on the Photomask



These techniques are called Reticule enhancement or RET.

Source: Mentor Graphics

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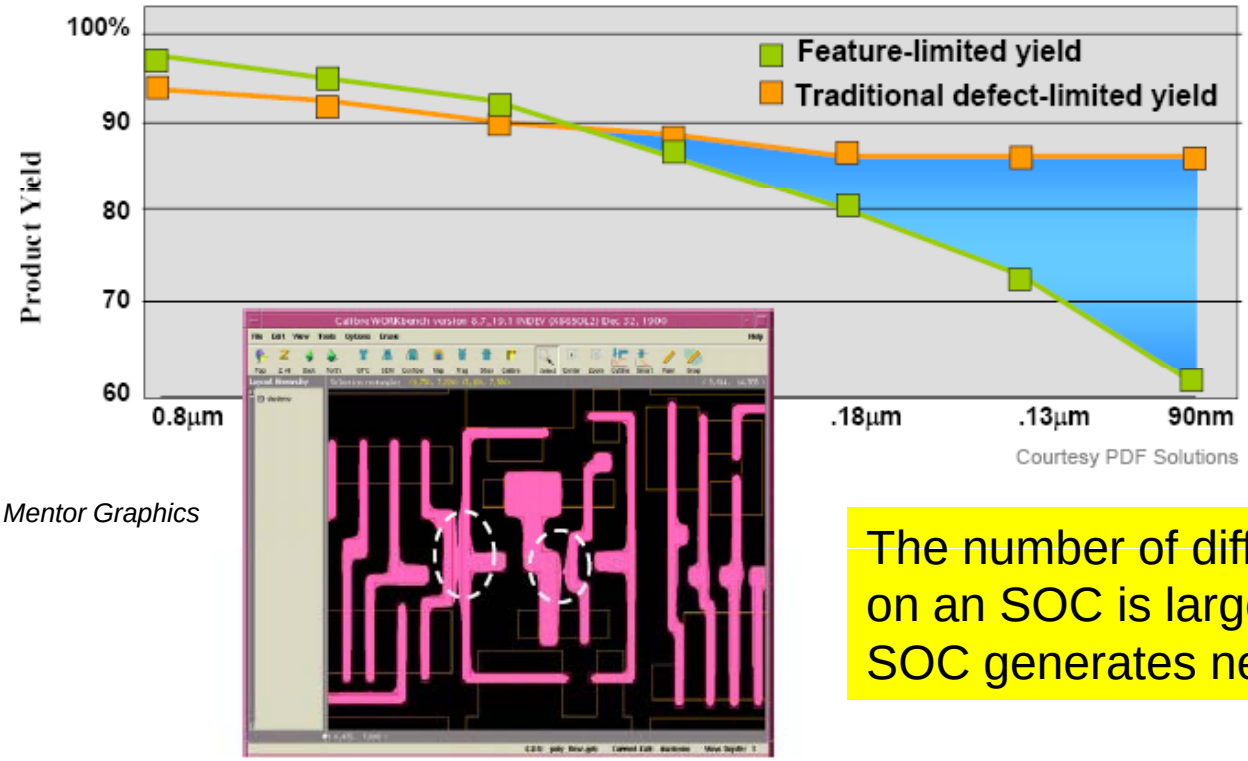
Yield limited by Structures not Particles

Manufacturing Yields Increasingly Limited by Physical Features Instead of Particles



Source: Mentor Graphics

The number of different structures on an SOC is large and each new SOC generates new structures.

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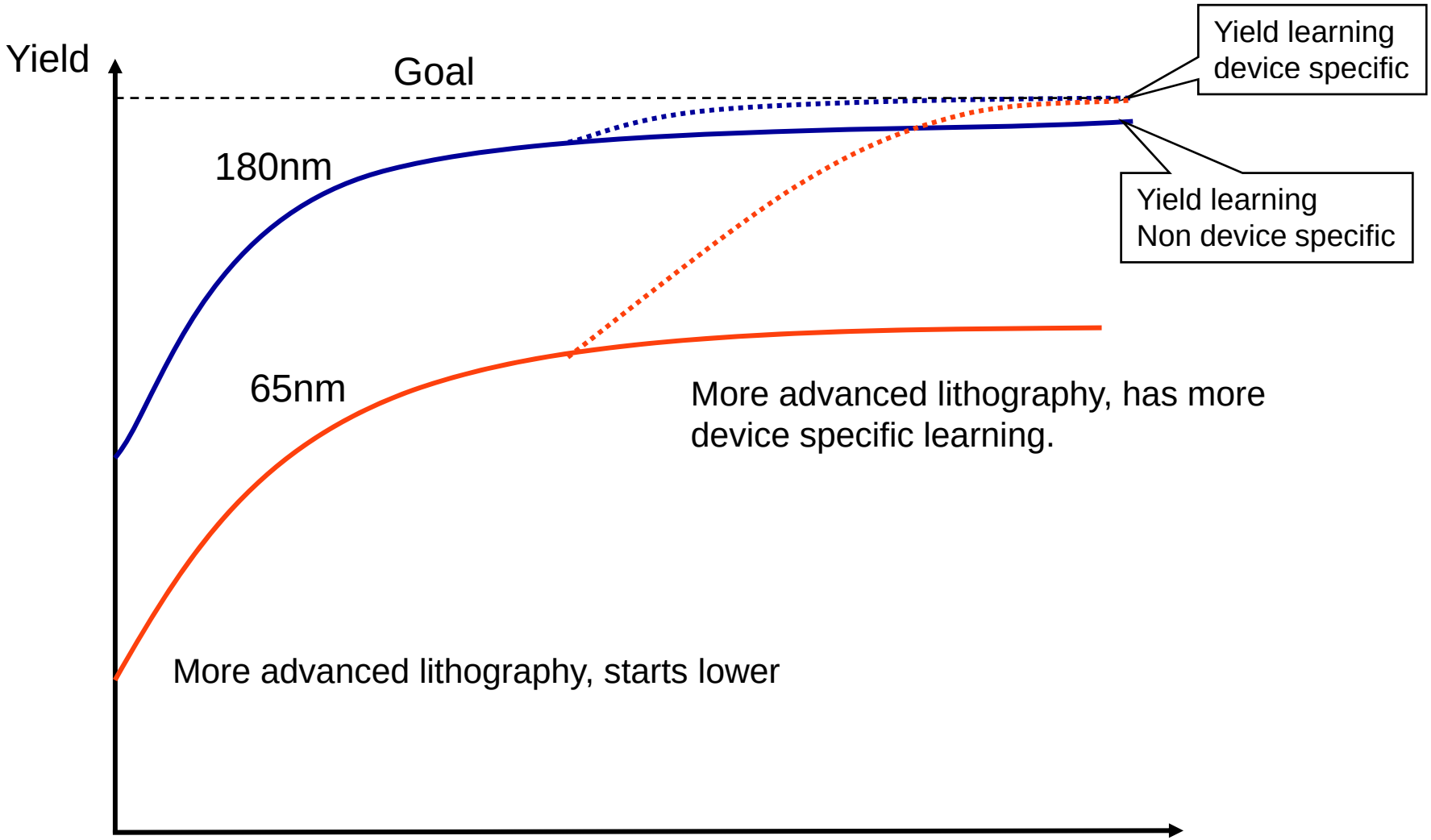
Achieving Good Yield Requires Device Specific Learning



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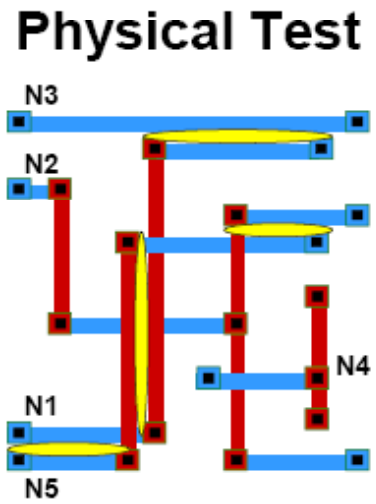
Scan can isolate the failures for Yield Learning with new models

Physical Layout Based Test



Prioritized Failure Modes Based on Physical Design

Potential Bridging Faults

- N2 to N5
- N1 to N3
- N1 to N5

Priority

- N1 to N5 – 50%
- N1 to N3 – 30%
- N2 to N5 – 20%

Source: Mentor Graphics

New fault models are generated more scan vectors to find these faults at SCAN.

- Stuck-At SCAN
- AC SCAN (transition faults
- Bridging
- Opens

Capturing 250 failures allows unique isolation of a fault

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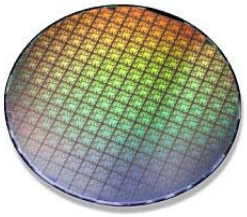
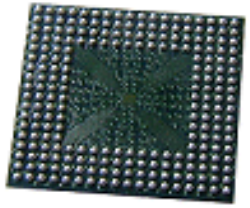
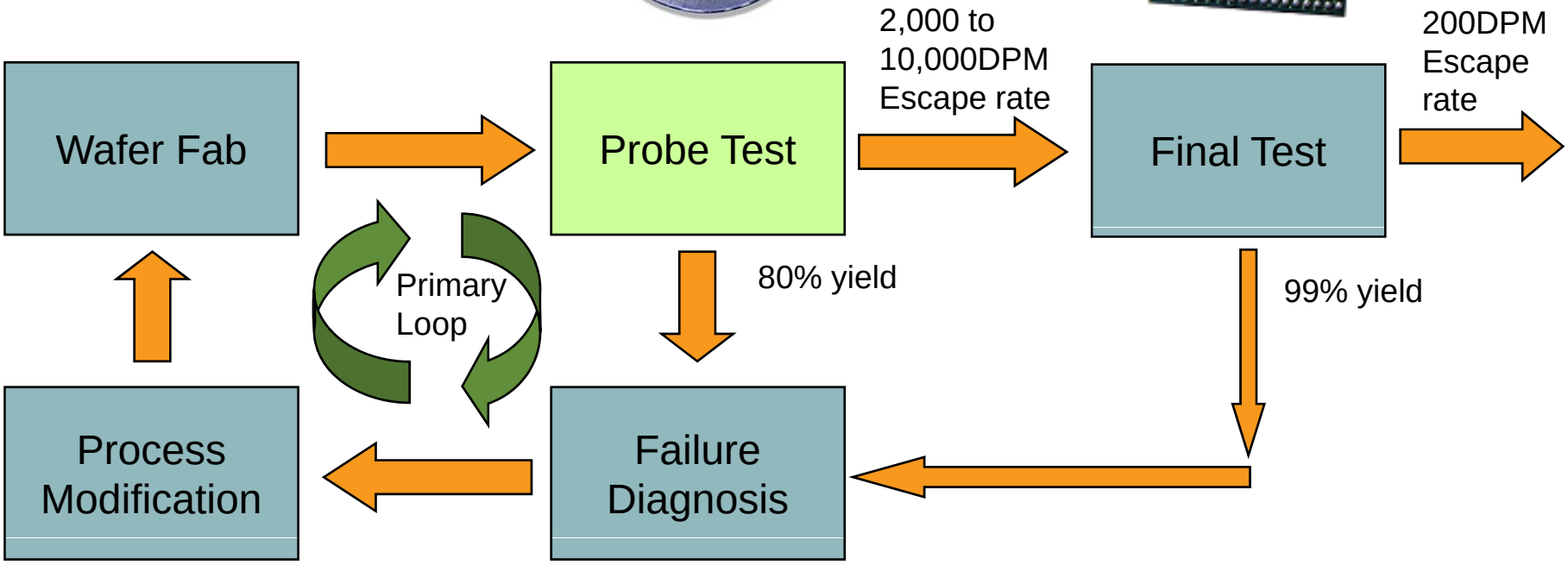
Key yield learning loop is Probe Test to Wafer Fab







Probe results are primary path for yield learning.

- Tighter connection to the Wafer foundry
- Data is available sooner
- Lower cost insertion

SCAN results are the primary data used because they enable rapid fault isolation.

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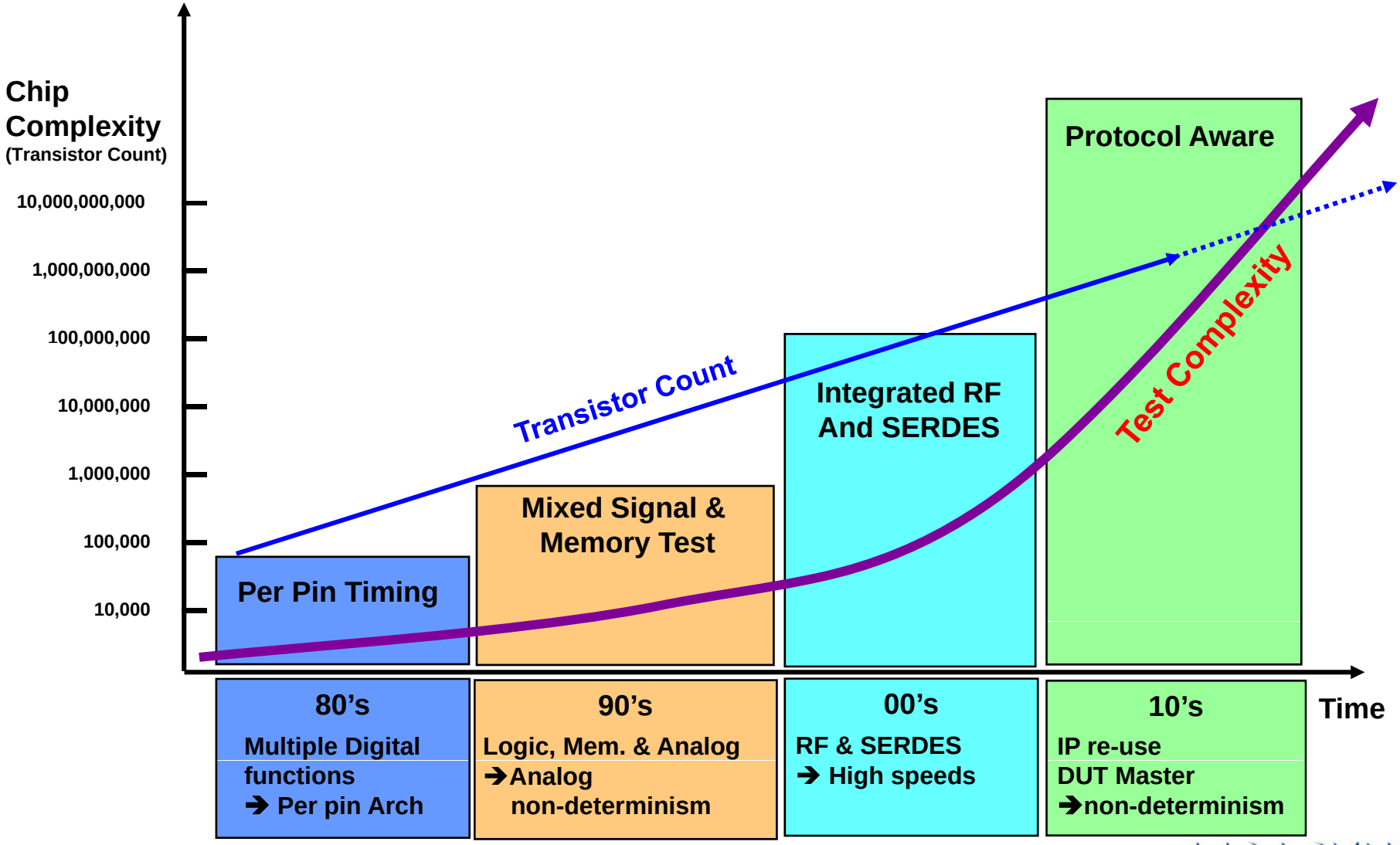
Impact of Integration on Device and ATE Complexity



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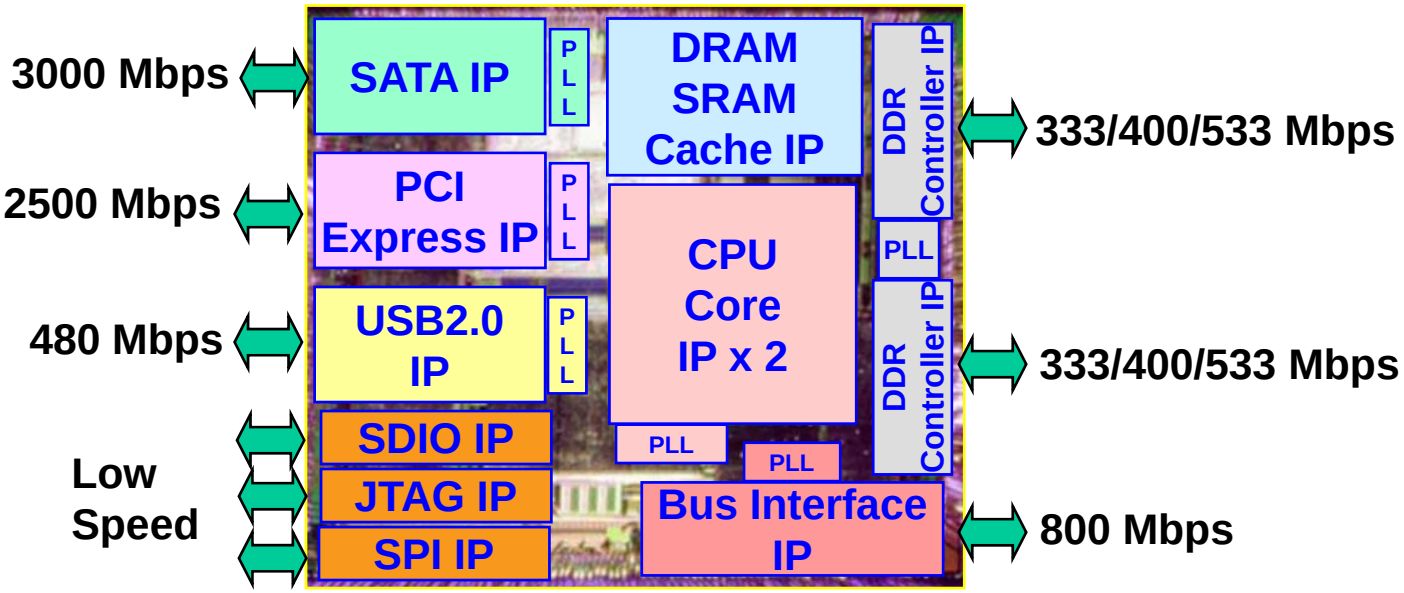
IP re-use: Design Engineers Heaven, Test Engineer's Hell



- Designers tape out full feature designs faster using Asynchronous IP that speeds design time and chip timing closure
- Designers work with high level behavior simulations, simplifying verification of complex bus protocols.

- Test Engineers do not have re-usable TEST IP
- Asynchronous I/F make test results non-deterministic, a tough test challenge
- Test Engineers work at a low level of abstraction, dealing with every bit in each complex protocol.

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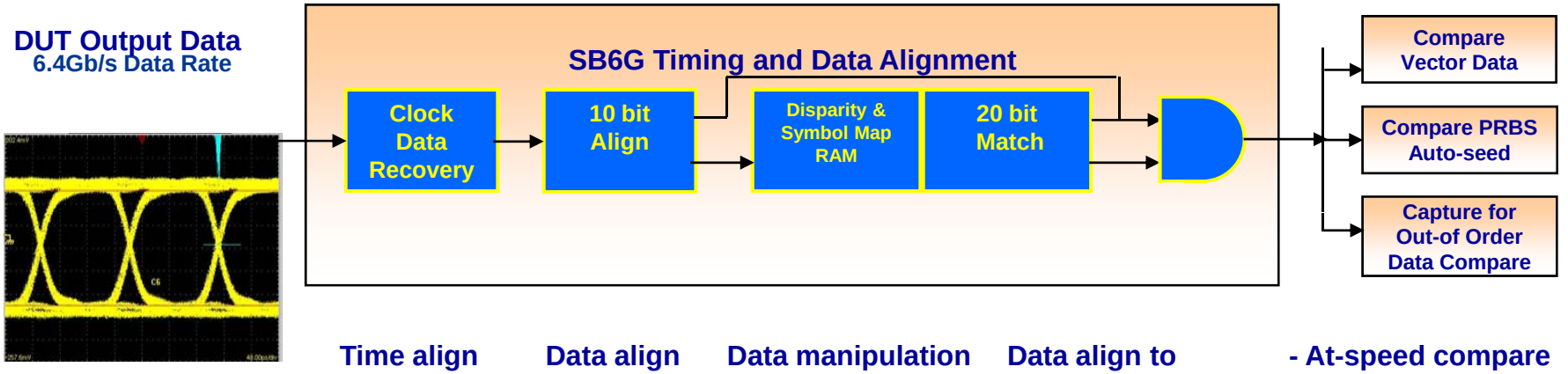
The Future of ATE is Protocol Aware

- **Limited Protocol Aware ATE capability is available today**
- **A first generation Protocol Aware Instrument is the UltraFLEX SB6G**
  - Designed for at-speed test of High Speed Serial buses like PCI Express and SATA
  - SB6G can recognize, manipulate, and compare 8b/10b encoded DUT output data



DUT output: 8b/10b encoded data @ up to 6.4Gbps

Time align to incoming data

Data align to specific 8b/10b Symbol Boundary

Data manipulation
- Ignore Idles
- Map +/- disparity
- Re-map symbols

Data align to a specific two symbol sequence

- At-speed compare with stored pattern
- At-speed compare with PRBS pattern
- Capture for later compare with Out-of-Order data

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The Future of ATE is Protocol Aware

- **ATE will become Protocol Aware rather than just stored-response patterns**

- **Future Protocol Aware ATE capabilities include:**
  - Transactional level software so design and test interact with the device at the same high level of abstraction. Faster time to yield and faster test development and debug.
  - Low latency DUT<-> ATE handshaking to support higher level functions such as memory (RAM/Flash/ROM) emulation.
  - Deal with non-deterministic DUT behavior such as timing shifts, idles, & out-of-order data.
  - Support at-speed functional test in device native operating mode (Mission Mode) for lower DPM.

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Thank You

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