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Silicon Photonics

Business Situation Report

Prepared by

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February, 2017

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Executive Summary

Silicon Photonics is the science and engineering used to leverage silicon semiconductor foundries to access to the vast knowledge, experience, and installed capital base in semiconductor manufacturing to produce photonic integrated circuits (PICs) with high yield, and low cost. As used in reference to commercial devices, Silicon Photonics is a finished product that includes use of silicon PICs and whatever else is needed to complete the desired product. The "modern era" of Silicon Photonics, meaning significant level of component integration in a single PIC, dates from around 2000; in the following 17 years, thousands of universities and dozens of companies have contributed to the technology, investing 10s of billions of dollars.

This work is intended to provide a detailed understanding of the Business Situation regarding Silicon Photonics. This is not a typical market research report, in that we do not develop market forecasts nor slice them across various market dimensions. While many companies, universities, and other laboratories are mentioned, in general we won't develop detailed vignettes about them. Instead, we focus on the technology status, the many options open, and what that means to participants in the value chain.

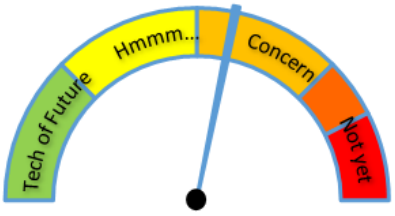
In some cases, Silicon Photonics is taken to imply the silicon PIC is directly integrated with electronics to make a complete transceiver or other product. However, even research examples of that level of integration are rare, and full integration in a single wafer flow is very unlikely for some time, due to differences in the process node size used by Silicon Photonics (~65 nm node) today vs. state of the art electronics (14 nm or 10 nm node), among other reasons.

Complete products based on Silicon Photonics thus require downstream integration, and there are some novel processes demonstrated such as integration on an optical interposer, or another substrate. In any case, chip to fiber coupling is a high risk area, having been demonstrated in only limited high-volume cases. The optical interface also points out the need for active optical and electrical test, which creates additional work flows compared to electronics. Additional process flows, downstream integration, test, and final packaging all add cost and risks. These seemingly simpler problems are viewed by industry experts as the main barriers to large-scale adoption of Silicon Photonics.

Although it is becoming rare to read a trade article having to do with data centers or the cloud without some reference to Silicon Photonics, we will motivate in the narrative that Silicon Photonics is far from mature technology, and that rapid evolution and improvements will occur over the next 10 years. The nascent state of Silicon Photonics technology creates risks to not only designers and foundries, but also early adopters. This manifested as the risk of paying too much for too little performance, impacting capital investment, capacity, or operating costs negatively compared to next-generation products. In the hyper-competitive cloud services market, decisions to go with new technology must be made with diligence.

We summarize the risks in a Risk Meter:

Building Block --> / exposed to risk	light source	modulation	waveguides	photo-transduction	control	fab	chip to fiber	packaging	form factor	assembly	test
silicon providers	90	20	50	20	75	100	85	90	75	75	80
packaging house	75	10	10	10	50		95	95	95	95	80
early adopters	85	50	0	0	75	85	80	80	65	65	70
cloud providers	75	50	0	0	40	75	75	75	40	40	50
enterprises	20	0	0	0	10	20	20	20	20	20	20
cloud consumers	35	10	0	0	30	35	35	35	30	30	35



We arrive at the above by looking across 11 key elements needed to deploy a Silicon Photonics solution and across the perspective of various stakeholders from Silicon Providers to Cloud Consumers. We conclude there is a level of risk that raises some concerns, especially for silicon providers (including fabless), packaging houses (or equialent in a vertically integrared supplier), and early adopters.

The underlying driver for all the investment and work in Silicon Photonics is the relentless increase in network and data center capacity demand, in turn driven by the internet. The challenge operators and providers are facing is that higher and higher data rates, from the chipsets to the intra-data center switches, are exceeding the limits of copper-based communication. Initially, the demand was met by migration to gigabit Ethernet, then 10 GbE, and now 25 GbE.

At 25 Gb/s on a single channel (or copper trace, or single fiber) even the data movement in the server boards and backplanes is challenging. At the same time, data centers have become much larger, and the physical distance of the longest interconnect may be over 1 km. All of these factors make a transition to optical communication imperative and inevitable. It has already begun in many cases, and the challenge is now to create lower cost, smaller, lower power, and higher performance ports to connect from the severs on up in the data center fabric. 100 Gb/s in a 4x25 (4 fibers, 25 Gb/s per fiber) configuration will rapidly become the standard at the server backplane. At present, Silicon Photonics is viewed as the most likely solution to these challenges in cloud-scale data centers.

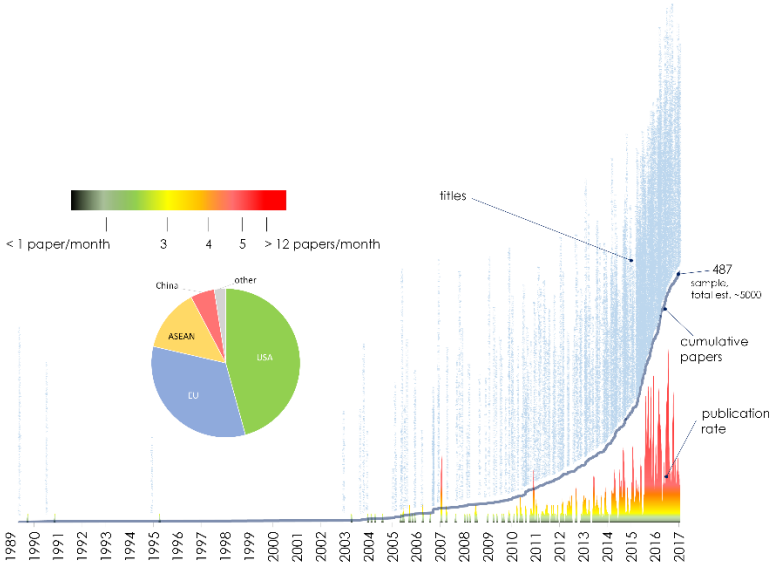
There are several key points that should be kept in mind while reviewing this work or researching the Silicon Photonics market.

- Relentless increases in data traffic drive huge increases in data movement within cloud data centers, pushing interconnect to higher speeds, already moving from 10 Gb/s per channel to 25 Gb/s per channel. Given the physical scale of cloud-scale data centers, at these speeds, photonics is the only feasible solution at present.
- Before long, even data within the servers will need to be moved on photonic channels, and eventually from chip to chip. Silicon photonics is viewed as a path to integrate the needed photonic functionality with electronics without incurring large cost penalties and while lowering energy consumption.
- Silicon Photonics can enable a new design paradigm for data center and server design, including a flatter network architecture. This implies some products are more likely to appear in new data centers sooner than upgrades, although upgrades will certainly take place.

- Once a generation of photonically enabled servers is commercialized, costs will fall rapidly. In addition, prices for "traditional" data center hardware may fall in response. Enterprises and data center operators will need to make decisions even while the technology is still evolving.
- Whether you are an IT consumer of hardware or services, or in some other part of the value chain, this report will help you frame your thinking and reduce the risk to your strategy of being unaware of possible huge shifts.

Important ideas developed in this work include:

- Silicon Photonics in some form can disrupt current on-offer data center interconnects, including some existing optical solutions.
- The current market leaders are in good positions to ride the cost curve down somewhat, but companies like Intel and IBM may be better positioned because they have vertically integrated fabs and broader product offerings.
- Over the last 10 years, a range of EU programs have been funded specifically to advance commercialization of photonics technology, including Silicon Photonics. One result is that STMicroelectronics is one of the few Silicon Photonics-capable foundries available.
- A significant share of the market likely will be served by fabless companies leveraging commercial foundries. The barriers to this are limited foundry capabilities and design kits available at present.
- Intel, IBM, NTT, Cisco, Fujitsu, Oracle and others are likely looking at long-term roadmaps with more integrated photonics of their own designs or sourced, including possibly at the chip to chip level.
- Existing interconnect specialists are in the situation of either controlling their own destiny by adding Silicon Photonics offering, or watching prices get crushed anyway.
- Fragmentation of the market poses a challenge to get enough share of the TAM to drive economies of scale.
- There is nearly frenetic level of activity in the R&D community and in many start-ups. This is exemplified by the following figure, which charts the publication of papers related to light sources (lasers) for Silicon Photonics.



In conclusion, we think that Silicon Photonics has earned a place in the next generation data center optical communication solutions. The technology is ready to begin a life cycle similar to the Moore's Law trajectory followed by electronics integration. We expect rapid introduction of new solutions in a very competitive market for the next 10 years, or more.

In addition to the narrative analysis, we provide a timeline history of developments in Silicon Photonics, containing 446 entries from 2000 to 2017. All material used in this work is cited in the included bibliography, containing 792 entries with author, title, and web links.

All players in the Silicon Photonics value chain should be making informed decisions today about how and when to participate, from fabless design houses to communication specialists to data center architects. We sincerely hope you find this work enabling in your decision making process.

Best regards,
Blaine Bateman
President, EAF LLC

Introduction

Silicon Photonics most generally means implementation of some level of photonic integrated circuit in silicon (see below for a more structured definition). As most commonly used, it means leveraging silicon semiconductor foundries--so called CMOS compatible processes--to get high yield, low cost, and access to a vast knowledge and experience and installed capital base in manufacturing semiconductors. As used in reference to commercial devices, Silicon Photonics is a finished product that includes use of silicon PICs (Photonic Integrated Circuits) and whatever else is needed to complete the desired product (a 25 Gb/s transmitter, for instance). The basic concept of Silicon Photonics has been around a long time (see below). The modern era, which might be taken to mean Integrated Silicon Photonics, dates from 2000 or earlier, or over 15 years ago. A very brief history is illustrative.

Six years of "almost there"

May 2000:
: Springer publishes a book by Horst Zimmerman entitled "Integrated Silicon Optoelectronics".

July 2000:
: MIT Technology Review publishes an article "The Microphotonics Revolution" in which author Peter Farley states "Squeezing light inside individual computer chips to replace metal interconnects may not be far behind".

December 2000:
: SPIE publishes an article by Yvonne Carts-Powell "Integrating optics and electronics without MEMS".

June 2001:
: MIT Technology Review publishes an article "Silicon Lasers" discussing near-term possibilities for both monolithic and heterogeneous lasers in/on silicon.

July 2003:
: PC Magazine runs an article "Broadband: Silicon Photonics" painting a picture with Silicon Photonics as the solution for demand for high-speed Internet.

July 2003:
: Science Magazine publishes "Photonics--A Technological Revolution" which describes potential for nanophotonics highlighting work at the MIT Microphotonics Center.

January 2004:
: Springer publishes another book by Horst Zimmerman entitled "Silicon Optoelectronic Integrated Circuits".

February 2004:
: Intel publishes in a letter to Nature "A high-speed silicon optical modulator based on metal-oxide-semiconductor capacitor" describing a CMOS manufacturable GHz modulator.

January 2005:
: Intel publishes in a letter to Nature "An all-Silicon Raman laser"; at that time it was considered a candidate for integrated Silicon Photonics, but was abandoned later.

April 2005:

The University of Twente publishes a paper "Reconfigurable Optical Add-Drop Multiplexer Using Microring Resonators in a Silicon Nitride-silica System". Microring resonators are a key component in today's designs.

April 2005:

Ghent University-imec publishes an article in Future Fab International "Silicon Nanophotonics" describing on-chip silicon photonic integrated circuits and developments in several other groups.

April 2005:

The State Key Laboratory on Integrated Optoelectronics in Beijing publishes a paper "Research progress on SOI optical waveguide devices and integrated optical switch matrix" in which they report on an integrated 8x8 optical switch in silicon on insulator.

May 2005:

The MIT Microphotonics Center publishes a report on Silicon Microphotonics entitled "Microphotonics: Hardware for the Information Age" in which they describe a roadmap for integrated Silicon Photonics.

November 2005:

UC Santa Barbara publishes a paper "Hybrid silicon evanescent laser fabricated with a silicon waveguide and III-V offset quantum wells" which describes a viable method of integration of III-V gain material to Silicon Photonic integrated circuits. Myriad variations of this theme are still in play today.

December 2005:

The Institute of Semiconductors (Beijing) publishes a paper "Recent Progresses of SOI-based Photonic Devices" describing a 16x16 optical switch in silicon on insulator with ~2 μS response time.

January 2006:

MIT, Cornell University, BAE Systems, Lucent Bell Labs, and Columbia University publish a paper "Electronic-photonic integrated circuits on the CMOS platform" describing a high payoff program launched by DARPA and status of the full range of needed functionalities for fully integrated CMOS manufacturable Silicon Photonics.

April 2006:

Luxtera publishes "CMOS Photonics for High-Speed Interconnects" showing many of the passive features in silicon needed to design complete transceivers, and reports that product development is underway. Luxtera is first to market using a separate laser built on a micro-bench and integrated to the passive silicon PIC.

December 2006:

UCLA publishes a paper "Silicon Photonics" in which the authors highlight the explosive growth of the field, stating "The burgeoning of the field over the last five years has made it all but impossible to provide a comprehensive coverage of the numerous worldwide efforts that are advancing the state of the art".

So from what seemed like early promise and real progress, it took Intel another 10 years to get a first product to market. Now, like other industry buzz-terms, it is becoming rare to read a trade journal having to do with the Internet, data centers, or the cloud without seeing at least one reference to Silicon Photonics. Frequently, references to Silicon Photonics are made in reference to data demand from the Internet of Things (IoT). Since Intel's strategy includes being at the center of both the IoT and cloud infrastructure, it may add to this line of thought since Intel is also

a leader in Silicon Photonics development. Indeed, while all the hoopla is going on about Intel finally launching a Silicon Photonic-based product and news about several other groups now out in the open with product or near to product, it would be easy to think that now it is just economies of scale, process engineering, and volume to compete and take share. There is something to this thinking, considering that global foundry leader STMicroelectronics has invested in developing a Silicon Photonics process flow in a 300 mm line, as reported by Mitch Heins on semiwiki.com and elsewhere. It is true that the level of activity is very high in Silicon Photonics R&D and product development.

OFC 2016 (March 2016)

Like many industries, Silicon Photonics product launches and announcements are frequently aligned to trade shows and professional society meetings/symposiums. Among those announcing products this year in March (2016) (at or in conjunction with the OFC conference):

- NeoPhotonics announced 1310nm and 1550nm high power lasers and laser arrays, designed for use in 100Gb s Silicon Photonics-based QSFP28 modules for datacenter applications,
- Infinera introduced their Infinite Capacity Optical Engine (ICE),
- Mellanox presented 'first' 200G Silicon Photonics devices,
- Kaiam showed a new 100G CWDM4 Silicon Photonics transceiver,
- IRT Nanoelec integrated lasers on silicon with MZ modulators in a cooperative effort with STMicroelectronics,
- Imec reviewed their Silicon Photonics platform to support 50Gb/s NRZ data transmission,
- Oclaro showed a line of 40G and 100G products for data centers enabling up to 400Gb s connections using single mode fiber,
- IBM reviewed how their Silicon Photonics systems target the 'high bandwidth future',
- thirteen companies including Broadcom Brocade, Cisco, Finisar, and others formed a collaboration to pave the way for 400 GB/s pluggable solutions, and
- Inphi unveiled their Silicon Photonics products for 100G data center applications,

to name a few.

ECOC 2016 (September 2016)

These announcements were followed up by additional releases in the intervening months up through the ECOC conference in September (2016).

- In a rare release of information about their development, Skorpios published a paper on their hybrid-integration-based Silicon Photonics Tx and Rx chips, and a 100 Gb/s CWDM platform based upon them,
- Intel, at their developer forum, announced they were shipping samples of a 100 Gb/s QSFP form factor transceiver using their own Silicon Photonics, as well as a new partnership with ARM, which could lead to an eventual multi-ARM core with photonic interconnect for ultra-low power Internet of things applications as well as future server designs,
- amid the growing wave of announcements about Silicon Photonics, EFFECT Photonics announced a new TOSA (Transmit Optical Sub Assembly) using their InP system on chip (SoC) technology capable of providing 500 Gb/s and targeted at inter-data center communications,

- seemingly in response, Infinera announced their Cloud Xpress 2 data center interconnect platform, offering 12x100 Gb/s,
- Lightwave Logic announced a new product integrating their polymer waveguide technology with silicon photonics and said their goal is 200Gb/s and beyond,
- Acacia Communications filed for an IPO and focused comments on integrated Silicon Photonics for data centers, reducing transceiver size from a pizza box to an iPhone, then subsequently launched a long-haul transceiver based on silicon photonics,
- AEPONYX joined the Silicon Valley incubator Silicon Catalyst and discussed plans to integrate MEMS technology with Silicon Photonics to make faster and lower cost switching for data centers,
- Global telecom leader Huawei launched their Fusion Server E9000 server based on Intel's Rack Scale architecture, including Intel silicon photonics as a cornerstone of the design,
- Applied Micro Circuits announced a partnership with Macom and BrPhotonics to develop a single wavelength 100Gb/s channel using PAM-4 modulation; Macom had announced a similar partnership with Applied Optoelectronics earlier in the year,
- startup Ayar Labs announced targeting 400 Gb/s ports in prototype by end of 2016, with production in 2019, to follow the ever-growing data center bandwidth appetite,
- Chinese photonics provider Gigalight founded a Silicon Photonics Alliance and said they will invest in Silicon Photonics development from 2017,
- Kaiam officially launched their LightScale2 platform, in a CWDM4 100G QSFP28 form factor, and said the platform will scale to 200G and 400G in the future,
- startup Aurrion was acquired by Juniper Networks instantly jumping Juniper into the Silicon Photonics mainstream,
- Ranovous launched a DWDM Silicon Photonics solution using Broadcom's PAM4 PHY, with range up to 80 km for data center interconnect,
- Hitachi and Oclaro published results of a new lens-integrated micro platform distributed feedback laser component for Silicon Photonics,
- ColorChip, a system on glass Silicon Photonics startup, announced closing another $20M funding round, and launch of 100G QSFP transceivers with 10 km reach,
- Effect Photonics announced they have developed a DWDM PAM-4 single chip solution sending 500 Gb/s up to 75 km,
- exhibiting at the Intel IDF, Ericsson showed its HDS 8000; the platform collapses the data center into two networking layers residing inside its rack, leveraging Silicon Photonics (presumably Intel's), and
- Mellanox and Oclaro demonstrated compatibility by linking four Oclaro SFP28 long-reach interconnects to the Mellanox PSM4 4x25 Gb/s data center solution to show 100 Gb/s up to 2km for high performance data centers, and Oclaro also showed a prototype 400 Gb/s CFP8 module,

comprising only some of the highlights. It should be clear there is a lot of activity in the development community.

Frontiers in Optics 2016 (October 2016)

Late in 2016 was OSA's (Optical Society of America) Frontiers in Optics in October (2016). Some of the announcements before or around that conference include:

- Leti announced a new EU Horizon 2020 project (COSMICC) targeting mass commercialization of Si-photonics based transceivers building on the Silicon Photonics platform of STMicroelectronics, with a goal of 200 Gb/s per fiber at about $0.21/Gb/s, or five times lower than the current market target; other industry partners include Finisar, Vario-Optics, Seagate, and Ayming,
- after winning a European Photonics Startup Challenge in October 2016, startup Sicoya announced in November receipt of and additional € 1M series A investment from KfW and said they are on track to ship fully integrated Silicon Photonic transceivers for 100G in 2017,
- Optical Connections News reported on another EU program (DIMENSION = DIrectly ModulatEd lasers oN SIlicON) targeting integration of BICMOS with Silicon Photonics for complete transceivers, with first results in early 2017; industry partners include IBM, Adva Optical Networking and Opticap,
- Mellanox announced 200Gb/s HDR InfiniBand AOC and DAC LinkX ® Cables,
- startup Elenion emerged announcing they have been working on Silicon Photonics for over two years, will formally introduce products next March (2017), and expect to address the $1/Gb/s cost target,
- leveraging Luceda's IPKISS design and simulation software RMIT (Australia) announced a turnkey service for passive Silicon Photonic PICs with only 6 week turnaround, in cooperation with the Australian National Fabrication Facility,
- Infinera joined the US AIM Photonics initiative as a tier-1 industry partner, giving the program critical manufacturing knowledge in Indium Phosphide technology, and
- Samtec, an electrical and optical interconnect provider, joined AIM Photonics as a tier-3 partner, augmenting the manufacturing and design capabilities of the initiative.

Given these and other developments, we believe this is a period of not only intense activity in Silicon Photonics, but also great uncertainty. This view is supported by a number of reviews in the last two years of the status and roadmap of/for Silicon Photonics development. We seek to provide some clarity as well as provoke thought regarding the development and deployment of Silicon Photonics and the attendant impacts on the various commercial products/markets that integrate or use electronic communication. Although highly technical, the goal of this work is to uncover the business situation as it applies to the use of Silicon Photonics. The focus is mainly on data centers.

Focus on Data Center applications

Data centers are the likely sweet spot for early Silicon Photonics applications, although even that is open to question. In a 2015 white paper, Acacia Communications noted Silicon photonics is usually considered only for low-cost, short-reach, high-volume (> 1M/year) products. This is because it is assumed that a large number of wafer starts is required to pay for mask and development costs and that Silicon Photonics has a significant performance penalty for metro and long-haul products. However, the real situation is actually the opposite. This is because in low-cost, short-reach, high-volume applications, there is tremendous competition from vertical cavity surface-emitting lasers (VCSELs) and directly modulated lasers (DMLs), and Silicon Photonics' weakness of not having an easy way to integrate lasers is a significant disadvantage. On the other hand, in metro and long-haul applications, it is better to keep the laser separate anyway as it is preferable to integrate the Silicon Photonics and DSP together, which is a hot environment. Also, coherent detection can make up for many of Silicon Photonics'

imperfections, such as the dark current is much smaller than the local oscillator photocurrent. Also, the argument that one needs a large number of wafer starts to pay for mask and development costs is fallacious, because Silicon Photonics is done in a very large node size compared to state-of-the-art CMOS, and thus the masks and runs are relatively inexpensive. This view notwithstanding, we believe focusing on data center applications makes sense in the short term.

This research report does not predict the growth of sales of Silicon Photonics components nor make forecasts on the shipments or market shares. For such details, we recommend Yole Developpement and LightCounting, among others. Although many companies will be mentioned, we won't provide vignettes on key players as you would find in a typical market research report.

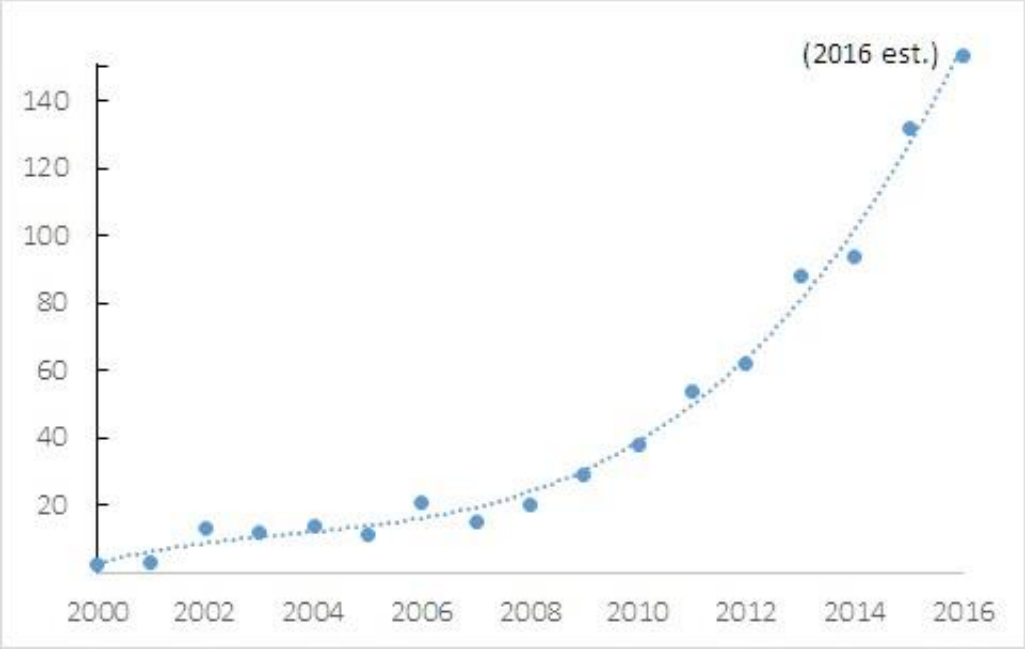
An important theme in this work is that, despite more than 15 years of intensive research and thousands of publications, articles, and conference presentations, Silicon Photonics is nearly at the beginning of innovation and productization of technology. That is not to say there are not impressive demonstrations of the technology already. For example, in 2015 Columbia University published a detailed analysis of optimization challenges in a Silicon Photonics optical switch fabric, and showed that 128 x 128 switches were feasible with acceptable insertion losses. In July 2016, UC Santa Barbara showed a complete on-chip optical switching network with 8 x 8 configurable ports, with operation to 40 Gb/s, such as might be used in an optical router. The entire device was implemented in CMOS Silicon Photonics plus integration of active III-V material by bonding III-V material dies onto the silicon on insulator wafer.

Although our focus in this report will be on active optical interconnects with integrated lasers and Silicon Photonic-based photonic integrated circuits, there is progress in many other areas, such as the switch fabric examples here, all leading to complete deployment of Silicon Photonics throughout the entire data center communication fabric. The challenge we hope to portray is understanding when these products will reach mainstream, and using what technology and design choices. The latter is very important; we will show that there are limited manufacturing (foundry) resources at present which may limit or slow introduction of novel designs. *This creates risk for first movers and early adopters*.

On the other hand, existing photonic interconnect technology has continued to advance, so the bar for Silicon Photonics has been raised. As early as 2006, Intel and the IEEE 802.3 High Speed Study Group realized the target had to be 100 Gb/s (in a 4x25 Gb/s configuration), even while 10G optical was not fully adopted. Another point could be taken from optical communication company Infinera's 2014 release of a rack-sized switching fabric that provided 21 Tb/s total capacity in one rack. The need for low-cost, high-speed optical links has thus become clear. Less clear is what design rules future Silicon Photonic-based, high-speed, low-cost links will use. We will show in the key necessary technology areas that there are many options and it is far from finalized what are the best solutions.

Metrics show frenetic activity

There are many indicators supporting this position. As one example, although in this work we do not attempt an analysis of intellectual property in this area, we show the trend of US patent applications containing reference to the term Silicon Photonics.



Trend of US patent applications containing the term Silicon Photonic in the title, abstract, claims, or specification. Source: EAF analysis.

It is evident that the trend of patent filings has accelerated and continues to do so (2016 is estimated). This acceleration will be seen in other measures later in this work. We feel in the particular case of intellectual property the trend is highly correlated to activity in R&D, and shows that more work is being done every year. As noted, it is outside the scope of this work to analyze the intellectual property situation. Nonetheless with more than 700 applications (more than 400 granted) it is likely the situation is complex and may present some barriers to widespread adoption in the short term.

Based on our own work researching the trade press, we are confident that a broad range of professionals throughout computing and communication industries have seen a fair amount of hype regarding Silicon Photonics. Part of the purpose here is to help ground you with the reality that there is still tremendous R&D to do before mass commercialization. Not to say that products will not come to market; indeed some are already in the market, but that the tipping point is some ways in the future. In part, that is because there are still many options coming out of industrial and (mainly) academic laboratories, so the risk of early adoption on a mass scale is still high, in our view. A view from the R&D community that we think epitomizes the challenges as

well as highlights that significant further integration levels, likely in 3D, will be needed to meet needs can be found in:

Yoo, S. Ben J., Binbin Guan, and Ryn P. Scott. Heterogeneous 2D/3D Photonic Integrated Microsystems. *Microsystems & Nanoengineering* 2. (31 Dec. 2015): <http://www.nature.com/articles/micronano201630#affiliations>,

one of over 700 citations in the bibliography of this report. Another perspective may be found in a very recent publication from NTT Device Technology Laboratories:

Watanabe, Kei, et al. Recent Progress in Optical Waveguide Technologies Enabling Integration of High-Density Compact Photonics. *NTT Technical Review* 2017.1 (18 Jan. 2017): <https://www.ntt-review.jp/archive/ntttechnical.php?contents=ntr201701fa2.html>.

The situation is changing quickly, however, and we hope that some portion of this report resonates with you and can help lay down a thought process to get the information you need to make decisions confronting you.

Audience

Participants anywhere in the value chains* to be impacted by Silicon Photonics:

- ✓ Executives and managers in telecom and datacom
- ✓ Technologists and researchers seeking a broader overview of how Silicon Photonics will affect R&D priorities
- ✓ Business analysts and others seeking decision support
- ✓ Consumers of internet and cloud services
- ✓ Enterprise data center architects
- ✓ Server designers and manufacturers
- ✓ Data center builders and owners
- ✓ Financial analysts monitoring sever, cloud, data center and photonics and related markets and companies
- ✓ CIOs who develop roadmaps for in-house/cloud/hybrid data centers
- ✓ Other players in the value chain, such as cable/interconnect providers, to assess market demand shifts

* The value chain is extensive. For Silicon Photonics *manufacturing* today, there are a limited number of foundries, fabless designers, and integrated electronics manufacturers (like Intel or IBM [now, GlobalFoundries]) in the value chain. On the other hand, there are a large number of players from small design houses to niche technology developers and startups to the multinational R&D firms. Significant investments in Europe from the early 2000's to develop capabilities have expanded the playing field and built out a nearly complete EU Silicon Photonics value chain. Investments included substantial government support and public-private partnerships such as HELIOS. New investments in the US in the AIM Photonics initiative as well as large investments from US academia and industry have had and will have similar impacts in the US (although the US is significantly behind in the sense that EU efforts have been more coordinated).

Depending on the manufacturing process, adoption of Silicon Photonics may impact wafer suppliers if, for example, demand is shifted away from InP or if some hybrid process such as bonding Lithium Niobate (LiNBO3) or III-V wafers within the process flow becomes important. The process also affects the foundry, of course. Early stage Silicon Photonics is in some cases based on smaller wafer size and larger feature size CMOS processing for fully integrated designs than is state of art in processors today. This may present a windfall for legacy fabs that tool up for Silicon Photonics, but more likely fragments the process across several fabs and integration steps. Thus, a given design and process may not be run in any single (existing) fab, and will likely not run in the highest volume lines for years.

The choice of process impacts not only foundry choice, but intellectual property owners. If heterogeneous integration of light sources becomes a significant share of supply, then a market for supply of micro-scale lasers that can be integrated into a CMOS process may grow (although we think that is unlikely). Similarly, there could be demand for wafers or packages with light sources feeding into a wafer-bonding or pick and place processes in CMOS foundries.

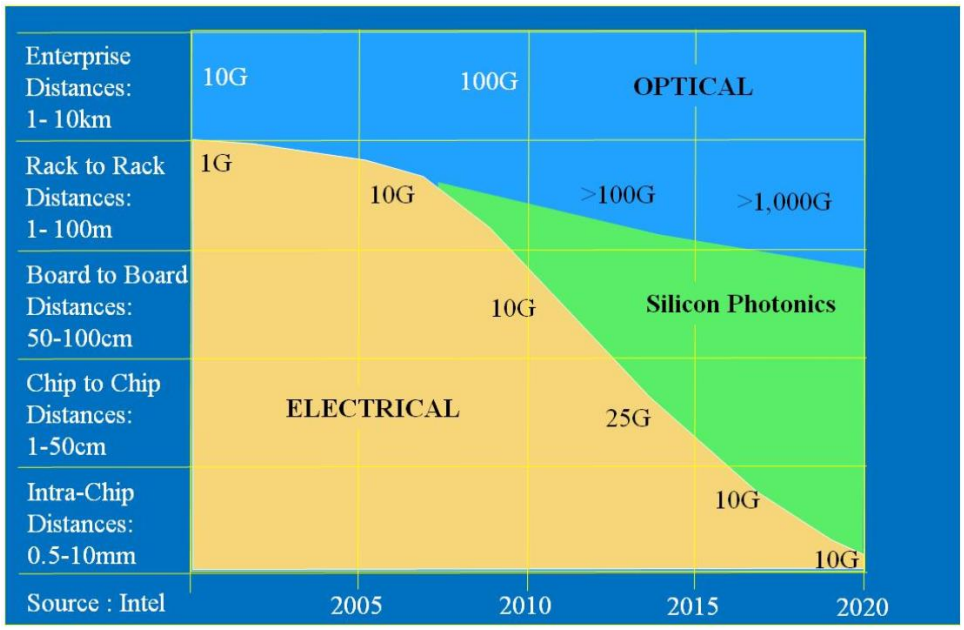
Downstream, device makers supplying photonic interconnect products will be affected if the cost structure of Silicon Photonic-based optics is low enough to affect market share of existing PIC-based products. It is likely that server architecture for data centers will be affected as next generation servers migrate to photonic backplanes or dis-aggregated architectures such as proposed by Facebook and Intel. An excellent example of new architecture enabled by photonic interconnect was reported by Oracle in December (2016). The authors describe the system as " all optically-interconnected 100G/port 8.2Tb/s InfiniBand packet switch ASIC with 41 ports running 100Gb/s per port interconnected by 12-channel mid-board optical transceivers with 25Gb/s per channel per direction of optical I/O. Using a blind-mate optical backplane, these components enable systems with up to 50Tb/s bandwidth in a 2U standard rack mount configuration with industry-leading density, efficiency, and latency."

The designers of interconnect will have choices beyond VCSEL or discrete (InP) options available today. This could affect not only the server design process but affect demand for VCSELs vs. new solutions in other interconnect products. Beyond interconnect, switch design is likely to be changed as Silicon Photonic solutions become available allowing deeper use of photonics. Even without Silicon Photonic switches, switch throughput will need to increase as higher speed ports are deployed on servers. Photonic switching is an active area of development within the broader Silicon Photonics design community.

Long term, photonic integration down to chip to chip interconnect and up to main switch levels in data centers will disrupt the current value chain feeding data centers today. This may appear as a significant disruption or it may occur over time and seem more of a refresh. We will make the case later that the chip to chip use of Silicon Photonics is the end game. Time will tell.

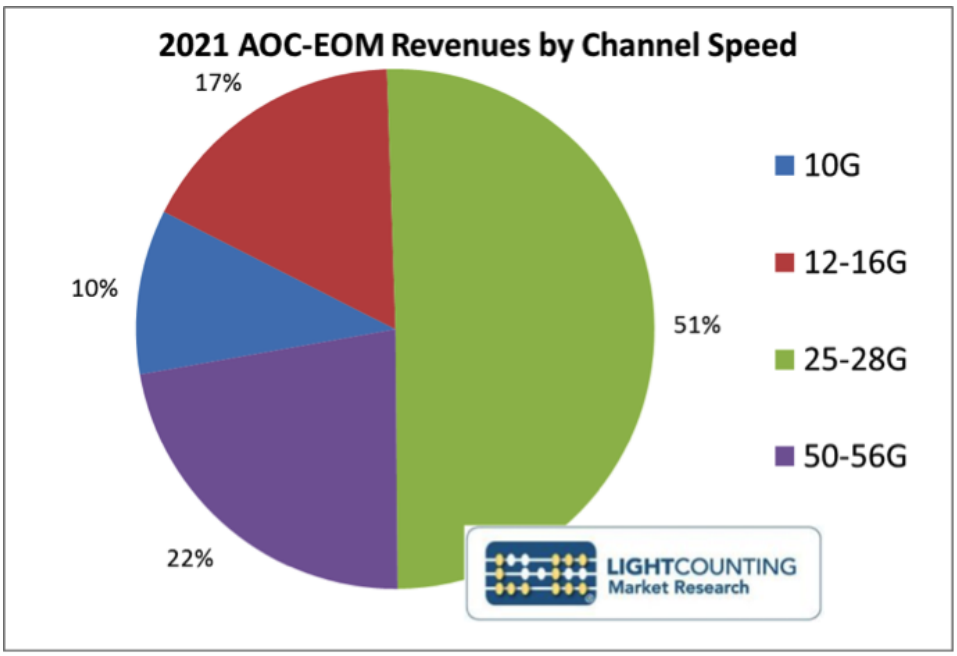
Business Implications

The business implications of a paradigm shift to fully integrated IPE (Integrated Photonic Electronic) devices are far-reaching. Consider a medium size cloud data center with servers as far apart as 500 m. This makes the distance from a rack to a data center switch greater than the maximum distance for all multi-Gigabit Ethernet interfaces over copper cable (note--this may change in the future, see below). Migrating to an optical interconnect can increase the data rates per port, but there are limitations in range vs. data rate, and in port density depending on the technology used. This has driven market growth in 10 Gb/s optical interconnects in data centers, and 40 Gb/s more recently. The driving forces are nicely summarized in a figure from a Photonics 21 conference workshop presented by STMicroelectronics (Maurizio Zuffada):



Operating ranges for electrical (copper Ethernet, etc.), optical, and Silicon Photonics based optical. From Zuffada, Maurizio. "Vision on silicon Photonics for efficient data communications." Photonics 21 - WG6 Workshop.: photonics21.org, 30 Apr. 2013. The author notes: "Communications based on copper are approaching their intrinsic limits. Hybrid 2D-3D Photonics cannot meet the long term spec requirements. Silicon Photonics can fill the gap."

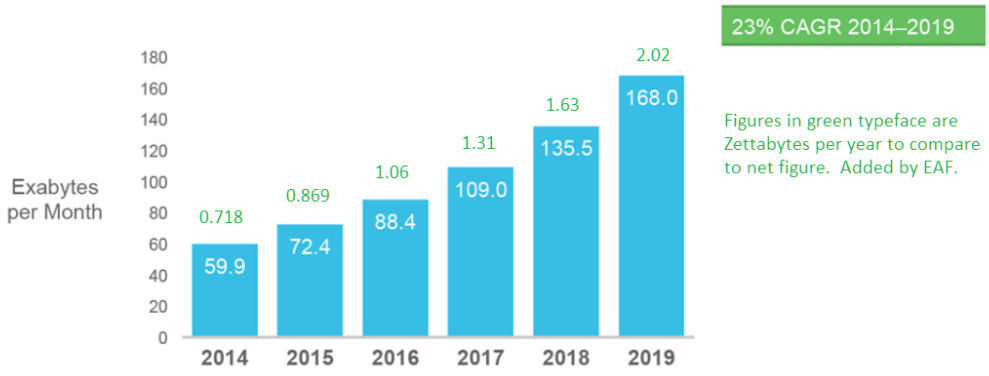
Premier Photonic-related market research firm LightCounting believes, in fact, that data center demand will be the core driver of huge growth rates in active optical cable (AOC) sales and embedded optical module (EOM) sales. Late in December 2015, they reported "LightCounting thinks the future for both AOCs and EOMs is bright, with the next two years marking a real departure from the past. We predict that the combined market will grow 48% to $262 million in 2015 and will go on to approach $850 million by 2021." They went on to explain the driver: "We are seeing some brand new opportunities, however, especially for EOMs. After being 'the next big thing' for some years, *datacenter applications* (*emphasis* added) have finally arrived. Both AOCs and EOMs are included in the plans of some of the largest cloud-scale players. These customers buy large quantities and by the end of our forecast, will dominate unit shipments, admittedly at very competitive prices." LightCounting forecasts that 25-28 Gb/s channel will dominate according to their long-term forecast:



Source/credit: LightCounting, used with permission.

The inexorable growth in data volume and connection speeds simply cannot be ignored. Cisco's forecasts of IP traffic illustrate the issue--annual growth of 23% for at least the next 5 years.

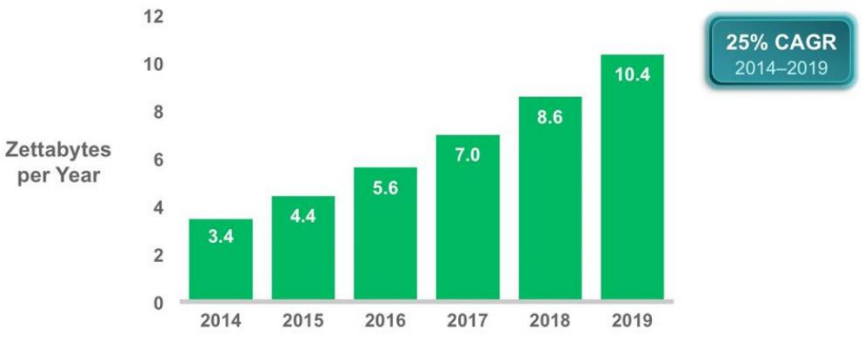
Figure 1. Cisco VNI Forecasts 168 Exabytes per Month of IP Traffic by 2019



Source: Cisco VNI Global IP Traffic Forecast, 2014–2019

The situation for data centers is actually *more demanding*. The externally visible IP traffic for 2015 shown above works out to 869 Exabytes per year, or 0.869 Zettabytes per year. But inside the data centers, there is actually much more traffic--roughly 5 times as much traffic that must be handled by servers, interconnects, and switches.

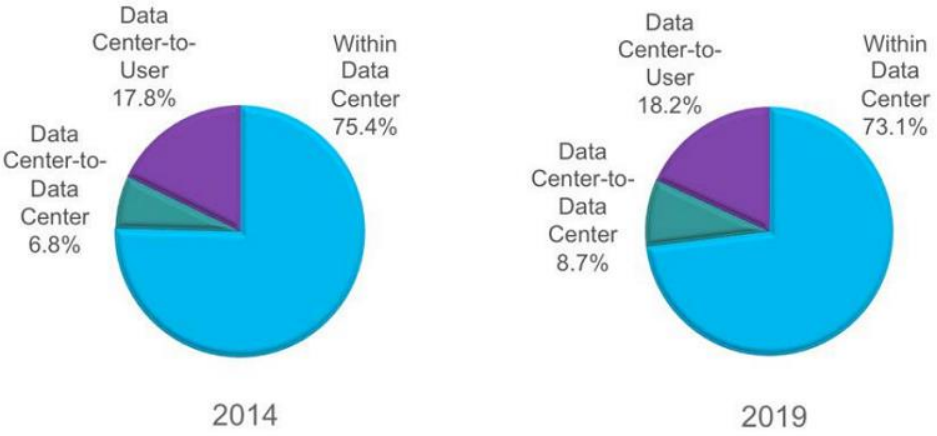
Figure 1. Global Data Center IP Traffic Growth



Source: Cisco Global Cloud Index, 2014–2019

The real data volume challenge is inside the data center. The source of this higher level comes from data shuttling around between servers; for instance in a cloud compute situation, data might be moving in and out of storage to memory, or other resources might be moving around from server to server--code pulling from a development server to production when a release is done, for instance. Another source of inter-data center traffic is the increase in specialized cloud compute resources such as GPU-based machine learning and artificial intelligence tasks. The website The Next Platform reported in May 2016 about how "Google, Facebook, Amazon, Microsoft, Tesla, Baidu and others [who] have quietly but rapidly shifted their hardware philosophy over the past twelve months." This higher demand within data centers is summed up by Cisco:

Figure 2. Global Data Center Traffic by Destination



Source: Cisco Global Cloud Index, 2014–2019

The latest QSFPx form factor can offer 4 x 10 Gigabit channels in the same panel space a 2 Cat 6 (RJ45) ports, but the costs are orders of magnitude higher. Fully integrated Silicon photonic implementations may bring costs significantly (already over 30% for early implementations), eventually in smaller form factors and having lower power requirements. The initial target socket is 4x25 Gb/s in QSFP, such as the product announced to be sampling by Intel earlier this year (2016).

Indeed, Jose Pozo of EPIC, the European Photonics Industry Consortium charged with promoting the European photonics industry, wrote in an article on Compound Semiconductor, "Networking equipment consumes about 50 percent of a typical datacentre's energy. Air movement and cooling equipment consume about 37 percent, transformers and uninterruptible power supplies account for 10 percent and lighting and other items take another 3 percent. The easiest solution is to focus on innovative technologies that can enable more efficient networking equipment with less loss sources, and hence, fewer cooling requirements." In a 2005 analysis of data center cost models, Hewlett Packard determined as well that that amortized cost of the networking was about equal to the amortized cost of the rest of the data center. Thus, from a raw power standpoint and a power standpoint, significant improvements in the communication links is needed urgently.

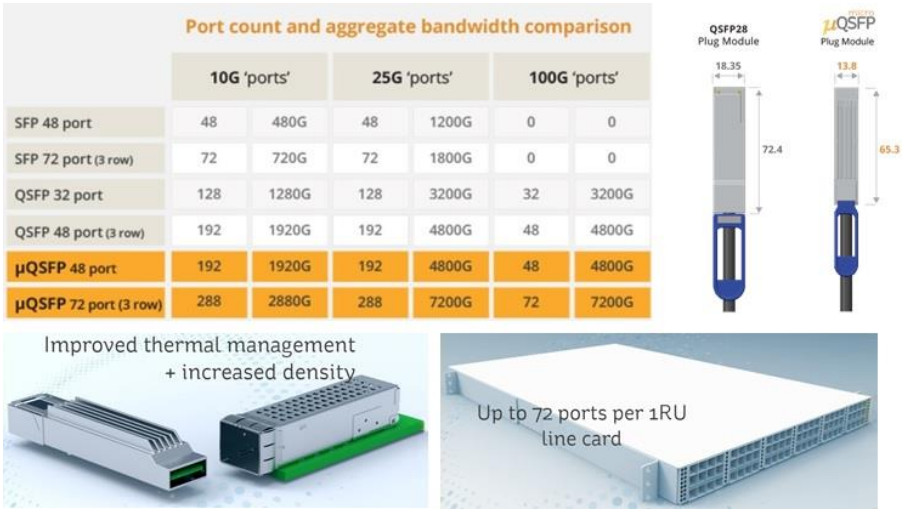
He also noted "this has been seen by many as the long awaited window of opportunity for the silicon photonics technology." and he amplified the fact that the market is only nascent, writing "As of today, only a very limited silicon photonic based product range is commercially available, and those products consist mainly [of] VOAs, Active Optical Cables (AOCs), and transceivers by Luxtera, Kotura/Mellanox and Cisco/Lightwire." It is interesting as well to note that this situation has not changed much since 2007--in that year MIT Technology Review trumpeted "Silicon Photonics Comes to Market" in an article almost exclusively about Luxtera's product launch.

Omnipresent Photonic Interconnects

Some possible impacts of ubiquitous photonic interconnect are:

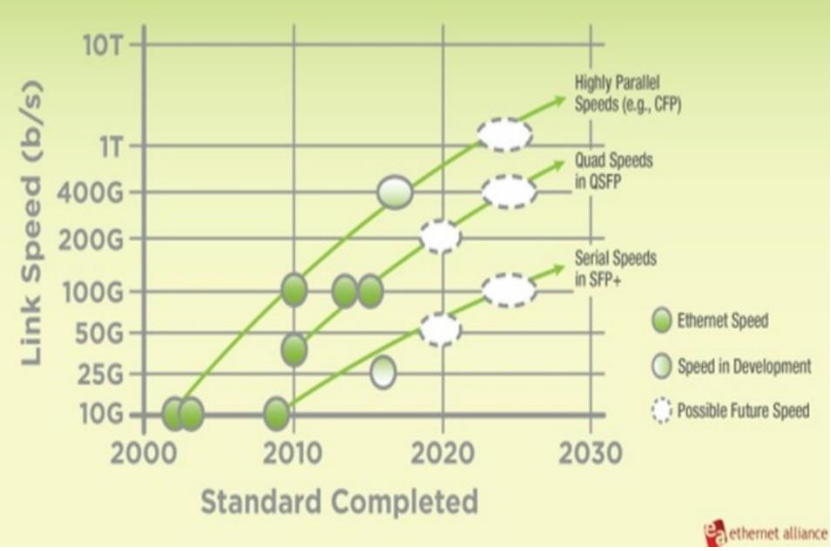
1) Reduction in cost for existing IPE applications, such as:
    a) CFPx 100G
    b) CPAC 100G
    c) QSFPx 100G
2) Introduction of new I/O form factors significantly increasing front-plane I/O density
    a. 40G in CAT-6 form factor
    b. MicroQSFP providing higher density (see below)
3) Improvements in user benefits, such as:
    a) Decreasing power per bit
    b) Migration to higher bit rates at lower power or cost
4) Migration of optical interconnect deeper into data center architectures:
    a) Rack backplane to switch
    b) Rack backplane
    c) Board to backplane
    d) Chip to board
5) Transformation of server and data center architecture:
    a) Optical from chip level enables higher CPU density due to lower power
    b) Optical from chip level enables dis-aggregation/modularization of CPU, memory, and network functions (as promoted by Facebook and Intel)
    c) Massive deployment of 100G+ optical interconnect allows beyond-hyperscale data centers

Point 5(c) is important to amplify. The expectation is for strong growth in 100 Gb/s interconnects in data centers in the future; however this may depend significantly on the roll out of lower cost and smaller form factors driven by Silicon Photonics. The interconnect industry is preparing for this direction by moving rapidly to define standards for smaller, more dense form factor interconnects. An industry group has formed to develop specifications for a "micro" QSFP form factor that will increase port density another 33% over QSFP, and initially support 100 G per plug, with a roadmap to 200 G. Wireless Week has called this interface a "game changer".



Source / credit: images adapted from microqsfp.com

We note with interest that Hitachi recently published results of a different form factor, called DensPac™, which exceeds the µQSFP density by about 1.5 times and the QSFP density by about 4 times. Like nearly every aspect of the Silicon Photonics for data center interconnect "ecosystem", this area is not settled. Advancements in form factor (density) and physical interface (connector) are important to maintain a roadmap to introduce new, faster Ethernet standards into data centers. The Ethernet Alliance reports on industry standards activities supporting the constant increases in speed. The increases have been coming in factor of 10 jumps until the latest round, when the 10x target was hit with 100 GbE, but 40 GbE was also standardized.



Source / credit: The Ethernet Alliance

As shown above, the next standards add complexity by standardizing some slower speeds; these are really about supporting higher speeds on existing CAT 5 or similar installed cable, not optical interconnect. What is important is that while 100 GbE can be supported in a QSFP package with 4 x 25 Gb/s channels, to get to 400 GbE in similar form factor will then require 100 Gb/s channels (i.e. 100 Gb/s on a single fiber or "lane"). At that point, less than five years away, Silicon Photonics may be very important in short-range/data center applications of the 400 GbE standard. Of very important interest to buyers and data center architects is the 200 Gb/s standard shown above that is a few years ahead of 400 Gb/s. According to LightCounting, some companies are planning to go directly from 100 Gb/s to 400 Gb/s, but LightCounting's position is that the 1-lane 4-lane paradigm will hold and many customers will adopt 200 Gb/s as a useful enhancement using 4x50G lanes (such as a 200 Gb/s PSM4 transceiver in QSFP form factor). At present (Q4 2016) Intel is sampling Silicon Photonics using 25 Gb/s lanes in a 4x25 100 Gb/s package), and 25 Gb/s on a single fiber is effectively the state of the art.

Although even farther out, in all likelihood, a recent review from Stanford University notes that in long-haul links, single-fiber data capacity has been reached, and to increase capacity requires adding more spatial channels. This means either more single-mode fibers, use of isolated multi-core fibers, or in some schemes use of multi-mode fiber. Depending on when such limits affect data center links and what direction development has taken, this could eventually require even more optical ports per server or switch, adding more pressure to miniaturize, minimize power consumption, and minimize cost.

Applications and Architecture

Some key questions thus are: (1) what is the application, (2) what architecture and standards (including yet to be created/completed standards as noted), and (3) what performance is desired? With answers to these questions, the optical communication technology choices will be informed. For the longer links in a data center, does it make sense to go with the 100 Gb/s links, and later upgrade to 200 Gb/s, or go from 100 Gb/s Silicon Photonics to 400 Gb/s? Today, with limited exceptions (importantly: Luxtera), all of the optical communication implementations for the standards noted above (and many others) are integrated optical systems (PICs)

combined with separate electronics. It is an open question whether Silicon Photonics enablement of IPE devices will be a better or necessary solution versus further development of integrated photonics and discrete electronics. At present (Q4 2016) long-haul optical links used in telecommunications use discrete PICs based on InP, discrete lasers, and discrete electronics, packaged to provide the speed and optical quality needed for such links. But that technology is simply too costly for ubiquitous use in data centers. Thus, the (apparently) inherent substantial cost advantage of a silicon PIC vs. existing materials is a key driver even in the same form factor and performance. On the other hand, there are groups working on using Silicon Photonics for long-haul links; recently, for example, IRT Nanoelec demonstrated 25 Gb/s over 10 km of fiber using a Silicon Photonics transceiver.

In fact, leaders in integrated photonics circuits such as Finisar have been skeptical: As reported by lightwaveonline.com during a March 2013 analyst call, Finisar Executive Chairman of the Board Jerry Rawls said about Silicon Photonics "I don't think there's a technology that's in the market at this time," he added in response to another question about whether a Silicon Photonic alternative might blunt the opportunities for the optical engine Finisar has developed for board-level communications. "We've seen a lot of discussions about technology demonstrations that might yield products in the next decade. But not -- most of them aren't in the market at this time, and there's clearly not much productization or commercialization."

Yet by 2014 things had changed significantly. Finisar, in a press release, said in September 2014: "Finisar Corporation (NASDAQ: FNSR) today announced the industry's first demonstration of a 50 Gb/s optical interface using silicon photonics technology. The technology concept shows both 40G and 50G NRZ-based transceiver modules running error-free on a single wavelength over single-mode fiber (SMF), complimenting Finisar's previously demonstrated 40G and 50 Gb/s VCSEL technology over multi-mode fiber (MMF)."

Author Roy Rubenstein reported in 2015 that photonic provider Oclaro views the Silicon Photonics supply chain as not yet robust, and the Silicon Photonics foundries as "boutique". In the same article Rubenstein cited Lumentum executive management that choosing to use Silicon Photonics technology adds many issues in test, packaging, and others. Nonetheless, currently leaders such as Intel, Cisco, Aurrion (now Juniper Networks), Mellanox, Teraxion, Lumentum, and Finisar all have Silicon Photonics platforms in various stages of development, and there are several other startups in the market as well. We think it may be that Silicon Photonics has advantages in certain applications and certain standards implementations, while PICs made in InP or GaAs technologies have advantage elsewhere. Power is a significant factor in high-density servers and data centers; Cisco has been able to migrate from 100G solution to a 400G solution in the same form factor at the same power. As the IEEE and the communications industries works to standardize 100G, 40G and 400G implementations, the need for higher data rate channels with less power and small form factors may favor Silicon Photonics.

As for the application, data center leaders like Facebook are already planning for widespread use of 100G interconnects in their data centers. In her abstract for an OIDA Workshop on Integrated Photonics High Volume Packaging in March 2016, Katharine Schmidtke head of Optical Technology Strategy for Facebook said "The migration to 100G-based datacenters is underway" and "Data center requirements differ from those of the traditional

Telecommunication equipment central offices in many ways—making it possible to optimize for shorter life-times, relaxed environmental conditions (e.g. temperature, humidity, and mechanics), and also reduced link budgets." This means that time to market and performance along with lower power consumption and lower cost will be paramount for use of high-rate interfaces in data centers. The former (time to market) may favor PIC-based technology; the latter (performance at lower power) may favor Silicon photonics. As noted, we think Silicon Photonics clearly will have the cost advantage in the future.

It is worth noting as well the impact ever larger and more efficient data centers are having on the traditional telecom industry. Acacia's CEO Raj Shanmugaraj was quoted in August 2016 saying ""If you take ten years ago, a lot of the traffic was being driven by traditional service providers like Verizon and AT&T. But today, a lot of the traffic is going into the data centers. The hyperscale guys are connecting the data centers today." The shift puts even more pressure on the data center capacity and efficiency. As Jeff Hecht reported in Nature: "On 19 June [2016], several hundred thousand US fans of the television drama *Game of Thrones* went online to watch an eagerly awaited episode — and triggered a partial failure in the channel's streaming service. Some 15,000 customers were left to rage at blank screens for more than an hour. The channel, HBO, apologized and promised to avoid a repeat. But the incident was just one particularly public example of an increasingly urgent problem: with global Internet traffic growing by an estimated 22% per year, the demand for bandwidth is fast outstripping providers' best efforts to supply it."

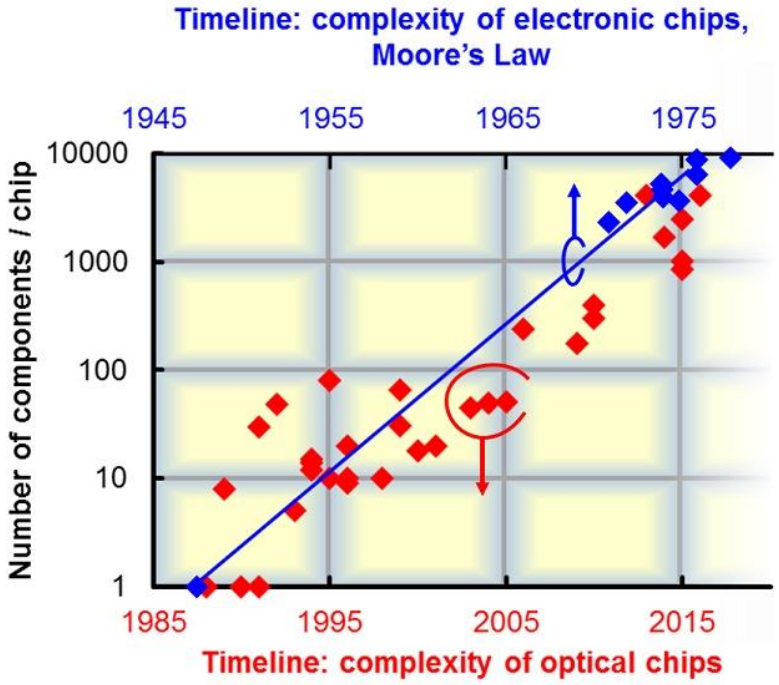
Regarding time to market, the aforementioned experts LightCounting quoted their own CEO in a January 2016 release: "Many in the industry have predicted that Silicon Photonics (SiP) will enable inexpensive, mass produced optical connectivity, radically changing the optical components and modules industry," commented Vladimir Kozlov CEO and Founder of LightCounting. "Our analysis suggests this will not happen in the next 5 years, but sales of SiP based optical products may reach $1 billion by 2020, accounting for about 10% of the market." The implication is that while there are and will be early-adopter silicon-based IPE devices marketed, there may be several iterations of interconnect evolution and server performance gains before this technology is mainstream. Nonetheless, it is true that both Intel and HP are sampling new IPE products to their top tier customers today (2016), Luxtera has already shipped one million Silicon Photonics products, and Cisco has integrated the technology brought in with the acquisition of Lightwire into their products.

Returning to the business implications, it is clear that companies that are part of the integrated photonics supply chain clearly are being pushed to include Silicon Photonics in their portfolios. Server and data center designers and users will need to consider if they should design around existing solutions or try to get something new and better via Silicon Photonics. Similarly, if today's IPE offerings aren't sufficiently attractive, at a design cycle in the future decisions will need to be made.

The New Moore's Law?

As an example, consider the early days of microprocessors being leveraged to bring "personal" computers to market. If the design cycles weren't aligned, a competitor might appear with a more advanced product by surprise. The point is that designs today based on existing solutions

could be surpassed in just a few years. This is nicely illustrated by the following figure, from a LinkedIn Pulse article authored by Martijn Heck (Associate Professor at Aarhus University who has been involved in Silicon Photonics for many years). If, as he illustrates, Photonic integration is at a point similar to electronic integration in the 1970s then changes will come quickly with large performance (or size, cost, etc.) gains. The slope of the trend for Silicon Photonics suggests a 10-fold increase in integration every 10 years. Thus, future designs with increasing complexity are enabled by Silicon Photonics.



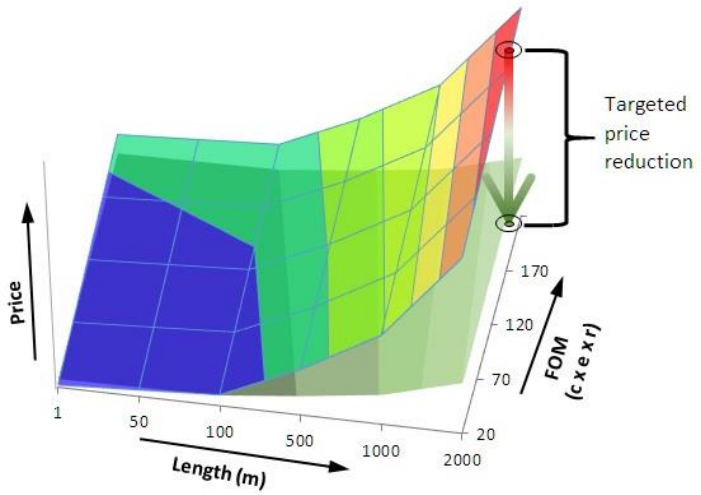
Comparison of the integration level vs. time of today's optical intergrated circuits to the early trajectory of Moore's Law for electronic integrated circuits. From: Heck, Martijn. "Photonic Technology Is Ready for the Next Bill Gates or Steve Jobs" Linkedin, 19 Oct. 2016. Web. <https://www.linkedin.com/pulse/photonic-technology-ready-new-bill-gates-steve-jobs-martijn-heck>.

Data center designers and owners face important decisions for the interconnect technologies. Since beyond-hyperscale data centers are in the near future, the choice of photonic interconnect technology could spell commercial disaster if not done carefully and with consideration of this highly fluid state of technology maturation.

EE Times reported last year (2015) that Facebook is pushing to upgrade in 2016 to higher throughput photonic interconnects. EE Times as others have reported that Facebook is standardizing on the QSFP28 form factor and CWDM4 as the underlying photonic approach. QSFP28 uses four (hence Q for quad) optical lanes with up to 28 Gb/s speed; CWDM4 is Coarse Wavelength Division Multiplexing which breaks up the output of a laser into four sub-wavelengths. Facebook is quoted as saying multiple technologies can meet their specifications, meaning product using PICs and electronics as well as IPE devices using Silicon Photonics can be offered.

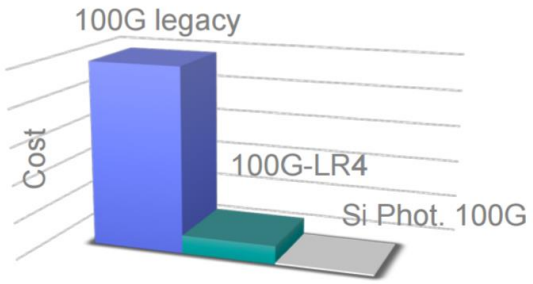
However, Facebook is also quoted as targeting a cost of $1 per Gb/s, meaning one QSFP28 port supplying 100 Gb/s would be $100. That is many times lower than typical pricing available with PIC based technology today. Thus Facebook is trying to drive the interconnect industry to find solutions far exceeding the price-performance envelope today. Light Reading reported that last spring a Facebook network engineer said Facebook expects Silicon Photonics to be the platform that gets them where they want to be. We also learned from another source that Intel's Silicon Photonics QSFP28 CWDM4 price is around $5 per Gb/s now (2016). Since almost no Silicon Photonics products have ramped to volume, it is likely that figure can drop towards Facebook's goal. Yet given the microQSFP activity noted, might Facebook's QSFP decision be questioned in a few years?

To illustrate the price elasticity around distance and performance, consider prices for photonic interconnect products. We modeled the price sensitivity as the product of channel rate times the number of channels, and looked at the price versus this figure of merit and the interconnect distance. The upper surface represents where things stand today (at low volumes; keep in mind that buyers like Facebook or Microsoft negotiate lower prices); the circled point in red would be a 50 meter cable with QSFP plug form factor capable of 100 Gb/s. The lower surface and the terminus of the arrow is representative of where hyper-scale data center builders need prices to go; the key point is that very short cables at lower data rates today are above the price targets; getting to those prices represents a fundamental market change, not just volume.



Graphical representation of optical cable pricing today (top, colored surface) and where large buyers want to see them for future hyper-scale data centers (lower, grey surface). Source / credit: EAF analysis.

Does Silicon Photonics have the potential to achieve these order of magnitude cost reductions? In a plenary address entitled "Enabling Large-Scale Deployment of Photonics Through Cost-Efficient & Scalable Packaging," to the 2015 Group IV Photonics Conference, Tymon Barwicz, from IBM's T.J. Watson Research Center, showed the following chart which nicely summarizes IBM's view at the time of the potential:



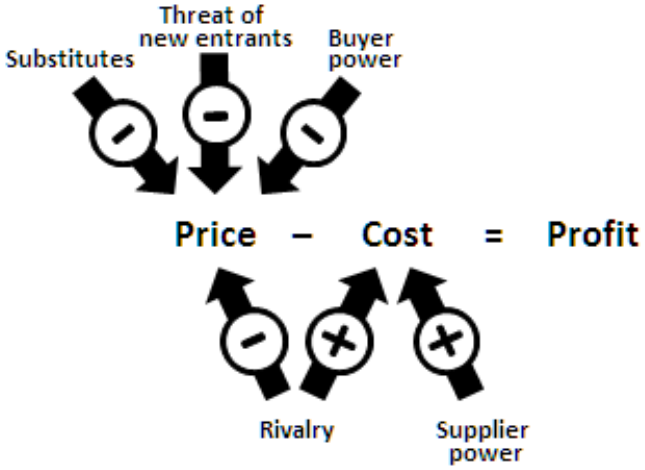
Source: Tymon, 2015.

The potential disruption could occur all the way down to chipsets. Referring to an announced partnership, Joshua Yeh, senior vice president of Applied Optoelectronics Inc.'s network equipment module business unit said "Macom offers an extensive chipset product portfolio for data center applications for both coarse wavelength division multiplexing and PSM 4 applications that is key for the transition of the mega-datacenter customers from 40G to 100G." With a large installed base and rapidly growing market, data centers represent a large number of ports that will be contested between PIC-based and Silicon Photonics-based products.

We can sum up this point by saying that we think that any business that touches the photonic interconnect supply chain at all should be thinking about how Silicon Photonics could change the market structure.

Market Motivation

There has been (and continues to be) a long and costly development of Silicon Photonics-based products. In open markets, there is constant competition for market share. It is illuminating to look at this from the Dr. Michael Porter 5-forces viewpoint. Today we have purpose built servers for data centers that communicate using electrical signals from the CPU to and from memory, storage, other servers, or switches. There are uniform rows of connectors for cables to perform the out-of-server communication, typically to a rack level switch. The competitive situation can be depicted as a balance of market forces:



Market forces per Dr. Porter's model. Figure adapted from Dr. Joan Magretta (J. Magretta, Understanding Michael Porter: The essential guide to competition and strategy, 1st edition, Boston, MA: Harvard Business Review Press, 2011), with permission.

In this model, Profit is what is available to you if you are selling into, say, the data center value chain. Your customer is the owner of the data center. (In reality, there are more layers in the value chain). Here is a generic/hypothetical scenario in this context: In 2017, the Buyers have considerable power, due to the large scale of their purchases, among other things. This power is represented by the buyer power in the upper right. High buyer power pushes prices down, reducing the available profit to you, represented by the minus symbol. Over time, the buyer has been approached, first by vendors selling higher speed pluggable communication (Ethernet) modules, who sold them on a new, higher density form factor, allowing them to put in more 1G sockets, and now 10G, increasing the total throughput of their servers. Then, other vendors came along and sold them active optical cables, converting from electrical to optical at the connector allowing them to have longer (fiber optic) cable runs, supporting higher data rates, which they needed because the data centers keep getting larger and data consumption is increasing exponentially. The combination of longer interconnect distance at higher data rates pushed beyond the limit of copper cables. Then they were sold on going to an even higher density pluggable module with optical out.

Substitution

All of these examples are of substitution--a different and better (or lower cost, or with higher feature sets, etc.) way to do the same basic function (connect the server to something else). There were performance factors in there too, but the basic decision was how to do the connectivity. Do you use ten 1Gb/s ports or one 10Gb/s port? In this context, then, Silicon Photonics offers to substitute if not at the processor level, then very close to there, converting to photonic communication while still on the board. While that substitution make take years to occur commercially, the substitution of optical for electrical from the top of rack and up has been occurring and will continue. Once the market broadly adopts optical connection at a given layer in the data center, competition continues on factors of price, quality, performance, delivery, and other factors, often in combination. The motivation is to lower cost, increase density, reduce power per bit, increasing throughput per watt per dollar. As an aside, although we are focusing on data center applications, optical communication leader Acacia Communications noted as early as 2012 that optimal design for metro-scale communications would include both InP PIC technology and Silicon Photonics, implying that Silicon Photonics could be a substitute in those markets as well.

In addition, Silicon Photonics will likely be a path to allow optical communication at the chip level, such as a believed Intel technology reported by Barron's and Fortune (both citing the same Susquehanna Financial source), and is considered a key "post-Moore" technology as described by Koji Yamada in PIC magazine. We agree that Intel is likely looking at the chip level interconnect as a potential differentiator in future server processor, memory, and accelerator markets. Other groups as well are interested in the chip level application, in particular Skorpios has stated their intent in that market. Recently (November 2016) LuxIO of Israel demonstrated chip level integration of Silicon Photonics with an ASIC as a building block of an optical switching network for future data center architectures. PETRA (Japan) demonstrated in November 2016 integrating multiple Silicon Photonics optical cores integrated to an ASIC using a hybrid PCB as the integration platform and designing the interface to be multi-mode allowing assembly without active alignment. IIT Madras showed in December 2016 another approach using a silicon platform bringing multiple waveguides to an optical core mounted adjacent to the CMOS-electronics. Columbia University has now (January 2017) shown feasibility of integrating Silicon Photonics with FPGAs for a software defined switch architecture.

The "post-Moore" distinction has to do with shifting performance gains from miniaturization and processor speed (i.e. the Moore's Law trend) to 3D architectures, faster interconnect, and more cores/parallelism. Indeed, while power consumption is a current concern, the "memory bandwidth wall" is nearly as urgent a problem, as noted by the University of Manchester in an October 2016 article in Computer magazine. Similar analysis is given by Wen et al in a recent article. (Note: as will become clear in this report, however, there are many options for nearly every low-level functionality in photonic interconnect. Even in the case of chip-to-chip communication, there are other options being explored, such as wireless communication demonstrated by work at Boston College.)

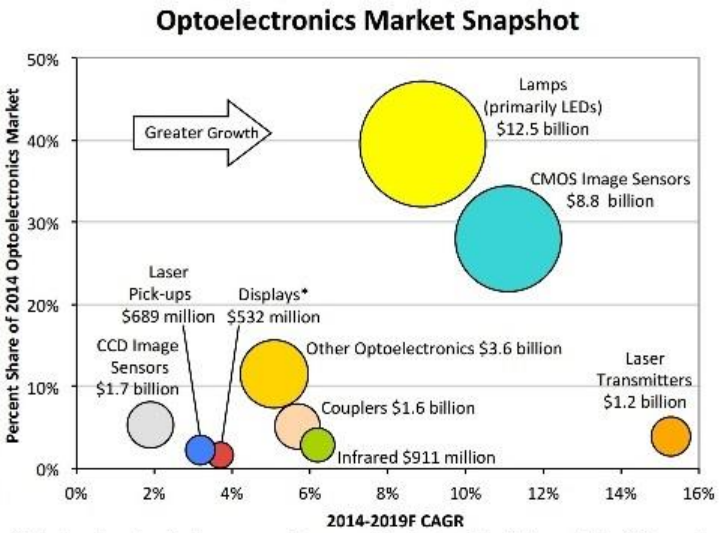
In all cases, such a substitution puts large pressure on the price of the previous way of doing the function. It may also shuffle the relationships in the supply chain, allowing some new entrants and changing the rivalry among suppliers. On the other hand, for those offering the new products, some of the power is shifted back to the lower right into the suppliers. As an example

of the latter, it was well publicized that Facebook stated in 2015 a target for data links of $1/Gb/s (in other words, a 100Gb/s port would cost $100); however we had a conversation with an industry expert and media contact that indicated Intel was engaged with Facebook with an initial price of $5/Gb/s being discussed. This indicates Intel had improved their power as a supplier, at least initially. So far (late 2016), there is no pricing openly disclosed for Intel's newly released 100G Silicon Photonics ports, so we cannot further update the situation. Of interest is to look at a Silicon Photonics roadmap document prepared by MIT in 2005, in cooperation with many industry groups. The authors estimated limit costs for copper-Ethernet ports ranging from $0.38 to $1.5/Gb/s, and suggested Silicon Photonics would need to be competitive. This range neatly frames the Facebook target and, if the $5/Gb/s figure is accurate for Intel's current (late 2016) product, indicates *significant work is needed to take costs out before widespread adoption*. Although we aren't aware of a similar price target from Google, it is reported that Google is already looking at 200 Gb/s links but so far has not used any Silicon Photonics based product in their data center designs. When/if Silicon Photonics reaches a certain cost/performance/throughput metric, a large pent-up demand may be available (see later regarding reports that Silicon Photonics is at or near a tipping point).

From the point of view of a supplier offering a Silicon Photonic solution, there is the potential to displace other, older suppliers, increase market share, and increase profits. From the data center owner point of view, the new solution increases capacity and density while lowering power demands, all at a lower net price. Consider that in 2013 the Natural Resources Defense Council estimated there were about 12M servers in the US in 2011. Market research firm IDC said global shipments were 2.6M in 2015, growing over 5%, so we have 10s of millions installed and millions more per year. Each server, depending on the data center design, will have two or more ports, so, once the photonic migration occurs between the servers and the next level (top of rack, etc.) the number of ports for which the connectivity vendors are competing is over 5M per year, plus refitting the huge installed infrastructure.

Another view comes from Cisco's Global Cloud Index, "an ongoing effort to forecast the growth of global data center and cloud-based IP traffic." Cisco's most recent report states that hyperscale data centers will be 47% of all data center servers by 2020, and will account for 53% of all inter-data center traffic. The traffic will grow to over 15 zettabytes by 2020. Thus, we conclude there is a significant motivation on both sides to make this transition. For the data centers, if data rate per port is increased to, say, all 40G ports then there can be fewer ports and the overall density in the data center goes up. For the optical connectivity vendors, that is a lot of ports to replace or substitute for.

Let's look at this from a more macro-market view. The chart below is beautifully put together by IC insights as a representation of the total optoelectronics market.



This chart, published by IC Insights in June 2015, was accompanied by a stated view of the markets: "...more recently, laser transmitters have re-emerged as a major growth driver in optoelectronics. IC Insights believes these three products will be key contributors to overall growth of the optoelectronics market through 2019." As evidenced by the chart, even "small" optoelectronic segments are attractive from a TAM (total available market) point of view. The noted laser transmitter segment is also forecast to grow at nearly 16 percent in the next few years. So how much of that might be Silicon Photonics and therefore motivate the research, development, and capital investments that have been made and continue to be made in Silicon Photonics?

Disruption?

In 2002, an article in EE Times reported on Intel's development of an optical filter / frequency comb in silicon. The author stated that Intel had done on a $1 chip what cost $10,000 to purchase for an optical communication system. Any development that could reduce costs by factors of thousands is disruptive. In those early days of the modern Silicon Photonics era, many believed the technology would be disruptive and would move ahead quickly. From a market standpoint, on the customer side a cost reduction of even many times, much less thousands, would be highly desired. The appearance of such products would be huge threat to many existing optical equipment providers. Realistically, long-distance telecom links require high quality and powerful photonics systems, and were not likely to be disrupted by early Silicon Photonics offerings. Viewed in hindsight from 2016, it seems obvious that the demand for Silicon Photonics would come first from data centers, high-performance computing, and similar highly-concentrated, high-bandwidth applications. (It is interesting to note that even 10 years later, Finisar, a leader in optical communications, was being pestered by analysts and the press about the "threat" of Silicon Photonics. Until 2013, Finisar did not see a need to integrate Silicon Photonics into their products. In an article on optics.org in 2013, Finisar Chairman Jerry Rawls was quoted: “I think there’s been a lot of gross exaggeration about the ‘threat’ of silicon photonics.”)

Thus, the market appeared attractive even in the early 2000s. As Intel continued announcements of Silicon Photonics progress, Luxtera, another key player in optical communications, debuted a 10 Gb/s optical modulator in CMOS in 2005. Two years later, the MIT Technology Review said of Luxtera: "For the first time, a silicon-based optical cable will be commercially available". Also in 2005, Intel announced a silicon Raman laser, apparently solving the problem of light generation from a monolithic silicon system. (Note: this was quietly set aside and was not used in later designs, being outperformed by heterogeneous solutions, including in Intel's current product.) In 2005 BCC, a market research firm, said the overall market for subsystems using photonic integrated circuits was growing at over 18% CAGR and would be worth nearly $6B in 2009. BCC also reported that the optical communication consumption of PICs was growing at nearly 80% CAGR. Doing some simple math, this implied a total available market for Silicon Photonics was $2B in 2009 (the *Opportunity*, not the actual sales). Given this market, if the selling prices are going to be so much lower (i.e. 10x or more lower), the actual market, at best, would have represented a few hundred million dollars in the late 2000s. We are not attempting in any way to forecast the demand for Silicon Photonics, but are trying to frame it in terms of the implications of bringing to the market optical interconnect products that are smaller and much lower in price than previous options.

Interest in Silicon Photonics and potential disruption of the data center interconnect market was piqued in 2004 when Intel announced their Gigabit modulator in silicon. Many trade journals and analysts were over the moon when Luxtera (acquired by Molex) launched their "Silicon Photonics" product, a 10 Gb/s AOC (active optical cable), in 2005; in some cases ignoring that it was only the passive circuitry in silicon. Even the SPIE said, in a 2006 article, "Silicon poises for disruption." When Intel showed a 50 Gb/s Silicon Photonics link in 2010, some were ready to declare victory. This seemed very timely, as pundits were projecting the end of Moore-scaling by the early 2010s, such as in an article on indybay.com by Kurt Kress in May 2006: "all will go down with Moore's Law".

Let There be Hype

Heading into the second decade of modern Silicon Photonics, Intel announced "The 50 Gbps Si Photonics Link--A research milestone from Intel Labs". Ghent University-imec announced a commercial spin-out company Caliopa (later acquired by Huawei). An IBM researcher, Solomon Assefa, was quoted in a cnet article: "In three to five years, silicon photonics will be the main enabler for that level of computation", referring to the need for high speed links in large-scale computing. Research firm MarketsandMarkets, a market research seller, said the Silicon Photonics market would be about $2B in 2014, and the trade press started hyping the end of Moore's Law. In the MarketsandMarkets report it is stated "wavelength division multiplex filter [sic] is the largest segment [growing] at CAGR of 106% from the year 2009 to 2014". While this appears consistent with the development trajectory, in reality segmentation of Silicon Photonics into components/functionalities is likely misleading as the most important application and goal is to integrate complete transceivers. (Note: see below. Two years later, throwing a bit of cold water on the enthusiasm, Yole Developpement, a primary market research firm and leader in photonics market information, said Silicon Photonics would be only $115M in 2014 and $215M in 2017.) Regarding Moore's Law, the line of thought was that around the 5 nm node, transistors would not get any smaller, and other solutions would need to be found. This pointed to a potential market for chip-level photonic interconnect. Silicon Photonics was touted as the

obvious approach, since it would be "compatible" with CMOS processing. Although this is a real motivation to continue development of chip-scale photonics, we view this as further downstream than discrete interconnect. The fact that current Silicon Photonics runs on 45 nm or larger process nodes is a challenge to be overcome to integrate with state of the art CMOS.

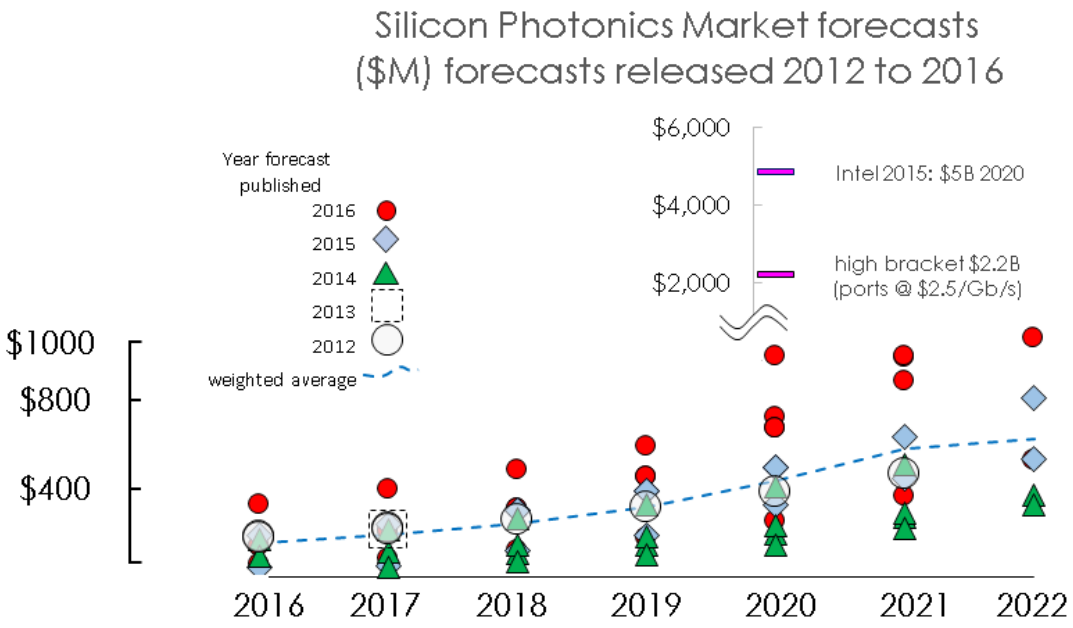
Over the next five or so years, to around 2015, the market potential estimates diverged in many ways. Compared to a roughly $2B near-term potential already noted, Semiconductor Today in 2012 reported that Yole Developpement forecast the Silicon Photonics market would triple from 2012 to 2017, reaching over $200M by then; the implication is that 2012 market was in the 10s of $M at best. The Ethernet Alliance projected in 2012 that 10GbE port shipments would exceed 1GbE in 2014, reaching around 25M year in 2015. As noted, in 2014 it was reported that Facebook's target for data center interconnect was $1/Gb/s, or a 10GbE port would be around $10, which equates roughly to $250M market at the end-product level (i.e. AOCs or other systems).

Also as noted, it has also been rumored that Intel's current price is around $5/Gb/s for the product they are sampling. If we take these 10 Gb/s ports as all potential market for Silicon Photonics (as well as further higher rate ports at 25 Gb/s and 40 Gb/s), then the market potential expected in 2012 was around $1B in 2015, but also with prices dropping precipitously; at $1/Gb/s that TAM becomes only $250M. Forbes ran an article in 2012, interviewing Peter De Dobbelaere of Luxtera, under the headline "Why IBM and Intel are chasing the $100B Opportunity in Nanophotonics." While we understand that nanophotonics is a much larger umbrella than Silicon Photonics, we are not sure where the additional two orders of magnitude in sales come from. The article itself was silent on that point. There was enough hype in the trade press at that time (2013) that LightCounting, another important source of primary photonics research, published a post entitled "Is Silicon Photonics Real?" stating "it has yet to be tested commercially by the market." In the same year, Stephen Hardy, Editorial Director and Associate Publisher of Lightwave magazine, wrote "Silicon photonics is still in its infancy. It may indeed change the course of the optical communications market, but not before it grows up first."

Heading into 2015, Yole updated their model, showing Silicon Photonics sales starting to take off in 2018, and over $300M by 2020. In other words, 20 years into a Herculean development effort around the globe, the market will only be a few hundred million dollars. Nonetheless, a bellwether event occurred in 2014 when Finisar announced products using Silicon Photonics, demonstrating "the first fully integrated silicon photonics transceiver operating above 40Gb/s". In April (2016), the earnings call for optical Telecom component maker NeoPhotonics struck high notes for record revenues and outlook, and pointed to 100Gb/s data center markets as a driver. Given that NeoPhotonics provides InP lasers into Silicon Photonics applications, including for Mellanox, such results are superficially positive. Nonetheless, on NeoPhotonics website they note: "Silicon Photonic devices can be made in standard CMOS fabs, leading to potentially very low costs when the volumes approach electronics scale. *For now, however, most Silicon Photonics devices are made in semi-specialized fabs on wafers with diameters of 8-12 inches.*" (*emphasis* added) Notably at Intel's Investor Meeting held in Santa Clara, CA in November 2015, Diane Bryant, Intel Senior Vice President & General Manager, Data Center Group showed a Silicon Photonics TAM of $5B in 2020.

Seemingly keeping options open in a dynamic and emerging market, in March, at OFC 2016, NeoPhotonics launched a product line of InP-based "High Power DFB Lasers for 100G Silicon Photonics Applications", which were noted as part of the same efforts that provide Mellanox with lasers for their Silicon Photonics product lines. Only two months earlier, industry research firm LightCounting reported "Many in the industry have predicted that Silicon Photonics (SiP) will enable inexpensive, mass produced optical connectivity, radically changing the optical components and modules industry. Our analysis suggests this will not happen in the next 5 years, but sales of SiP-based optical products may reach $1 billion by 2020, accounting for about 10% of the market. This is in contrast to LightCounting's December 2016 forecast for Active Optical Cables and Embedded Optical Modules which combined total to $918M for 2021; the implication that the component photonic device market is the largest of the three segments, and there is a large upside for Silicon Photonics to gain even more market share. Indeed, that is the position of Vladimir Koslov, CEO of LightCounting. In an article in PIC Magazine in December 2016, he wrote that in 2016, "SiP vendors made progress in penetrating two of the fastest growing segments of the market: 100G DWDM and 40/100GbE optics."

Finally, using available data for numbers of servers, internet traffic, port speeds and other factors, we bracket the 2020 Silicon Photonic opportunity in data centers between $0.4 and $2.2B. Summarizing, the market forecasts and their evolution indicates renewed optimism. This probably tracks the latest technical developments, especially from Intel and IBM. We do not venture a forecast here, but we collated available data as an illustration of the range of speculation.



Various forecasts for Silicon Photonics shipments, identified by the year the forecast was released. Note the jump in optimism last year (2016), likely the result of Intel's announced shipment of Silicon Photonic 100G modules. Source: EAF analysis.

Value Chain Implications

If we now consider the value chain for the Silicon Photonics market in the mid to late 2000s and we assume someone is going to disrupt the market for data center interconnect with Silicon Photonics, then there are three potential points of view. First, if you were a buyer of optical interconnects, then it might have been time to start waiting to see what happened. This viewpoint is troublesome because you would need to buy something to complete projects, but you would be aware that a paradigm shift might occur soon. Facebook is in this situation: they have defined an architecture for the switching/routing in their data centers, but the market isn't ready to provide the $1/Gb/s price point. They have to keep building to keep up with demand in their system.

Second, if you are were in the data center hardware business, integrating you own solution for Silicon Photonics could give you a significant pricing advantage over competitors. Intel is in this position. Although there is a market to sell interconnect products based on their in-house Silicon Photonics, the end game is to retain and grow share of as much of the data center core hardware as possible. In addition to a cost advantage, Intel and IBM are both in position to create further disruption by integrating photonics back to the processors and memory, and to enable a dis-aggregated sever/storage/memory design. In addition, there has been activity in the development community at the chip interconnect level, such as a 2015 publication from NTT describing "lambda-scale embedded active-region photonic-crystal (LEAP) lasers at room temperature, which we fabricated on a Si wafer. The on-Si LEAP lasers exhibit a threshold current of 31 μA, which is the lowest reported value for any type of semiconductor laser on Si. This reveals the great potential of LEAP lasers as light sources for on- or off-chip optical interconnects with ultra-low power consumption in future information communication technology devices including CMOS processors." The requirements for chip-level optical interconnect are different from Silicon Photonics in server-level interconnects, and we will not devote much more comment to this area. Nonetheless, it is important to understand what the (un-stated) roadmap may be, and that there is already evidence that the chip-scale problem can be addressed with aspects of Silicon Photonics technology.

Unlike pure-play interconnect vendors, the vertically integrated vendors like Intel can offer a substitute server design in the future, once the technology is ready. As noted earlier, there is some indication Intel is also working on leveraging Silicon Photonics at the chip level. The need and expectation of this migration was highlighted in the EUROLAB-4-HPC Report on Disruptive Technologies for 2022-2030: "The next step is to use optical interconnects to connect chips on the same circuit board. For future devices, also intra-chip connections may be optical. In general, the trend is going towards photonics integrated with electronics and closer to the chips and cores." Likewise, in a Next Platform article by Nicole Hemsoth in October 2016 regarding the IEEE Rebooting Computing initiative, quoted co-chair Elie Track: "This end of CMOS scaling, coupled with the explosion of big data and the need for more compute power for both civilian and military applications, requires the kind of exponential growth we have enjoyed for so many years. But that is the challenge; this is a crisis. This is an inflection point. Incremental improvements are not the solution, but the improvements we need might come from other areas in computing." A possible way out of the crisis is to dramatically increase data rates between basic functionalities with photonics, allowing more parallel cores at lower power, with

much higher memory I/O rates. Silicon Photonics is one of the only routes to this solution, at present.

Then we have the third view--that of pure play optical interconnect vendors. We think those vendors may need to think about their business models because of the threat of substitution by the vertically integrated competitors. The situation is complicated not only by the potential substitution of Silicon Photonics for InP and LiNbO3 but potentially other changes, such as the introduction of Graphene. Graphene could be used in place of Ge for detectors, as well as in modulators and other aspects of PICs. The potential impact of Graphene was reviewed in some detail in August 2016 by Michael Wheeler, Managing Editor of photonics.com. He quoted Stefan Preble, Ph.D., director of Rochester Institute of Technology's Integrated Photonics Group: "These electronic-photonic chips will represent a new paradigm in circuit design and enable a wide range of future applications including: high bandwidth, low power interconnects within chips and between them." Any market undergoing a paradigm shift is a risk to incumbents and removes barriers to entry for new entrants, in the short term, unless the incumbents drive the shift.

In a similar vein, Roy Rubenstein writing for fibre-systems.com in June 2016 suggested Silicon Photonics had reached a tipping point, where venture capital and other investment becomes very attractive. He cited the acquisition of Aurrion by Juniper networks as evidence; in a related article published on telecomlead.com, market analyst Patrick Filkins noted that the acquisition would allow Juniper to " integrate silicon photonics into its cloud networking portfolio", which although possibly self-evident, the premium paid implied a sense urgency. In an interview by Network World in October 2016, Juniper CEO Rami Rahim said "we are potentially on the cusp of a real breakthrough that will transform the economics of the optics in networking equipment, which obviously will be of great interest to anybody that is building a large, mission-critical network."

Acacia's IPO showed there is appetite in the market for photonics investments--share price reached a $1B valuation on the opening day, well above the upper pricing target (at $30/share), and subsequently reached over $4B market cap, although now around $2.3B. There are only a few other potential acquisitions available, in fact. In the PE side of the market, two examples are Ayar Labs receiving $2.5M funding in May 2016, and Sicoya reaching a total of about $4.7M by October 2016.

There are some other aspects that may contribute to market motivation to push for more Silicon Photonics. As data centers become larger, or "hyperscale", there is, for a given generation of servers, a limited amount of front plane and backplane area for interconnect. To continue scaling the number of bits per second a data center can handle, higher physical area density of connections is required or a point of no returns is hit. This same argument applies at the board level (at some point, chip to chip interconnect density becomes limiting) etc. Shifting to photonic interconnects has the potential for higher bits/s/area density. Silicon Photonics also offers the potential to have higher density than other photonic interconnect solutions, although this remains to be proven.

Another source of motivation is energy consumption in general, and thermal density in particular. Regarding data center energy use, Dr. Cijek Cavdar (KTH Royal Institute of

Technology) reported recently (May 2016) in a blog that the energy consumption of ICT (Information and Communication Technology) is forecast to double its share of energy consumption globally by 2020, from 2% to 4%. She said "This somewhat dire portrait should instill urgency in everyone working in the Green ICT arena – we really are in a race against time". It has been reported that from 15% to 30% of the energy consumption of data centers is used by interconnects, thus there are needs to minimize interconnect power consumption as much as possible, and Silicon Photonics may be able to achieve some reduction. However, at present there are some challenges for Silicon Photonics due to higher intrinsic losses in at silicon PIC compared to InP or LiNbO3 (Lithium Niobate). In an interview, trade website gazettabyte (www.gazettabyte.com) asked Joris van Campenhout (program director of the Optical I/O industry-affiliation program at imec) about the issue of insertion loss issue. van Campenhout stated "That is a show-stopper, because it prevents us closing link budgets." The issue comes down to energy per bit, and certainly isn't completely resolved. That notwithstanding, there are several companies, including Mellanox, Luxtera, and Intel achieving the QSFP28 specification of < 3.5W for a 100G module capable of supporting km interconnect distances.

The total energy consumption is enough of a consideration that it impacts where companies choose to locate hyperscale data centers and how they plan the sources of power for them, or even how they fit into the power grid. Facebook recently announced it will build a data center in Odense, Denmark, that will be powered exclusively by renewable energy. It already has a data center in Lulea, Sweden, less than 100 miles from the Arctic Circle. The Lulea data center can bring in naturally cold air to use for cooling, and Facebook founder Mark Zuckerberg recently posted pictures from the site to share "some rare photos of the most advanced technology Facebook is building around the world", as reported by The Verge. Microsoft has been researching underwater data centers to capitalize on the naturally cold environment in ocean water below the warm surface water. In another project, Microsoft's Cheyenne, Wyoming (USA) data center has arranged to sell electricity from its backup diesel-electric generators to the grid during peak load periods. This will allow the energy company to avoid building another power plant. Amazon announced in September 2016 the construction of their fifth renewable energy site, a 1 million megawatt hour per year wind farm in western Texas (USA). In Amazon's case, some of the projects are offsetting their energy consumption elsewhere, as is the case for the new wind farm. Including the latest project, Amazon has five renewable energy sites, with generation of 2.6 million megawatt hours per year.

Regarding the thermal issues, as the density of systems increase, the challenge of getting heat out becomes more of a concern. While the nano/micro scale of Silicon Photonics offers higher densities, careful design is needed to optimize not only data throughput but thermal management and total energy consumption. This will be more challenging at higher data rates (e.g. future 200 Gb/s and 400 Gb/s modules). In many potential implementations of Silicon Photonics transceivers, thermal tuning is used to control microring or racetrack resonators. This adds to the thermal load on the system, making the situation more challenging. Near-term responses include novel thermal management designs in data centers, including water cooling designs from Dell, or immersive cooling proposed by LiquidCool Solutions. A measure of data center efficiency from the cooling standpoint is PUE (Power Usage Effectiveness--the ratio of total power to the power used for the servers, storage, etc.) Liquid cooling may reduce cooling power costs if implemented correctly, thereby reducing PUE (lower is better) as well as address

higher thermal loads, but does not directly solve the problem. Facebook has pursued other new approaches, such as using naturally cool ambient air as noted above, and a two-story design where the air handling is on the upper floor, and cold air flows down through the servers, assisted by natural convection (i.e. cold air sinks). Other approaches include changing the power conversion architecture to line to 48V to point of load, distributing power through the servers at 48V vs. 12V; (Google has used this for several years), more efficient power supplies, energy efficient lighting (consider a hyperscale data center might cover 750,000 square feet (~70,000 square meters)), and software to optimize power distribution and to manage cooling usage. None of these address the power consumption of the core hardware, however.

Summary of Implications

Given what may be a modest market for some years to come, we return to the question of what is the real motivation. We think the information to-date points to a few things:

1) Silicon Photonics in some form can disrupt current on-offer data center interconnects. This includes at least some of the existing Silicon Photonics products from Molex, Mellanox (Kotura), Infinera, Luxtera and others. The latter view stems from the expectation that higher levels of integration and lower costs will render some of the early offerings obsolete, in a very standard refresh cycle as occurs in most semiconductor markets.
2) The current market leaders are in good positions to ride the cost curve down somewhat, but the Intels and IBMs are better positioned because they have vertically integrated fabs (we assume IBM has "better than most" access to the assets transferred to Global Foundries) and if changes are needed they may be best situated to make them. In addition, companies like Intel and Cisco, for example, occupy large positions in the data center value chain, as compared to pure-play photonic rivals.
3) Nonetheless, a significant share of the market likely will be served by fabless companies leveraging commercial foundries. The relatively low barrier to entry once design rules and simulation tools are available, means the market will be chaotic for some time. The issue is that these rules are far from well-known today and will continue to evolve as the fab-based learning curves are overcome.
4) Intel, IBM, NTT, Cisco, Fujitsu, Oracle and others are likely looking at long-term roadmaps with more integrated photonics of their own designs or sourced. Intel can benefit from deeper integration with other chipsets. Cisco has already designed in their own Silicon Photonics solution leveraged from their 2012 Lightwire acquisition.
5) Interconnect specialists are in the situation of either controlling their own destiny or watching prices get crushed anyway. Luxtera is in a good position in this supplier group. The entry of Finisar into Silicon Photonics validates their stated plan to source technology when needed (their initial demos were based on ST Microelectronics Silicon Photonics process). The challenges in a sourcing model are whether there is enough margin to support profitability through the extended value chain.
6) The long-term market, considering integration into switch gear, high-performance computing, new photonic interconnects from processors, and other deep applications likely make the total market larger than it appears looking only at interconnect ports in today's architectures. Thus the TAM might be in the billions of dollars in the next 10 years. This appears to be enough, combined with the other factors mentioned, to keep all the

big semiconductor players, switch and server providers, and a long list of universities engaged.

7) The fragmentation of the market poses a challenge to get enough share of the TAM. As noted some players are more focused in integration of Silicon Photonics into a broader offering, so they have leverage. For pure-play interconnect companies, small market share and many competitors are likely issues for 5 or more years.

What This Technology Means to You

Silicon Photonics refers to a range of technologies targeted to integrate photonic circuits with or into Silicon-based electronic circuit technologies (frequently referred to as "CMOS" or "CMOS-compatible"). At present, most photonics circuits (photonic integrated circuits or PICs) are not made in Silicon, rather materials such as InP and other platforms are used. These InP and similar photonic systems, which include those used for metro and long-haul telecom and data transport, are mainly separate from and additional to the data processing, switching, and storage in data centers. Those functions are connected largely by copper-based Ethernet connections. A vast infrastructure exists to manufacture integrated circuits using Silicon-based processing. This infrastructure is operated by companies who have a huge resource of accumulated knowledge in optimization of these processes. However, not all major fab operators can make Silicon Photonics circuits, as there is significant work and learning required to bring up a Silicon Photonics IC line. Some companies that have invested to have Silicon Photonics fab capability are Intel, GlobalFoundries (from IBM), STMicroelectronics, and Fujitsu. For such companies, Silicon Photonics offers leveraging that base while positioning to benefit from new markets for Silicon Photonics, displacing legacy Ethernet/copper. The promise is to gain market share and new market by increasing the interconnect speed and maximum distance while lowering costs.

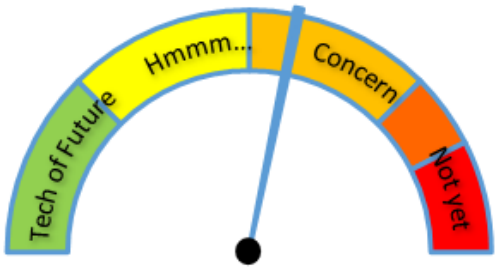
Trying to leverage the sunk costs in process development, production facilities (fabs), and institutional learning is a strong motivator to develop integrated photonic-electronic devices (IPE devices). Integrating everything into a system that could be made on existing semiconductor lines is expected to lead to low cost and minimization of new capital investment and new learning curves. However, as will become clearer in later sections of this report, the short-term goals are to manufacture silicon-based PICs in foundries and processes developed for microelectronics manufacturing, and possibly integrate light sources and other active functions in additional steps, and then add the control electronics in a final package. As noted, the term "CMOS compatible" appears nearly ubiquitously in discussions of Silicon Photonics, which may be misleading in the current case. Nonetheless, there may be good reasons to integrate the control electronics and logic in separate chips and integrate them into a final package with the silicon-PICs. That is a topic of discussion and the final configuration(s) are far from settled.

In our discussions of risk we at times will use the term risk*impact, meaning a conceptual product of a risk measure with the impact if the negative outcome occurs. This, as we discuss elsewhere, is in part motivated by the fact that the risk is not that Silicon Photonics will not be deployed, as there are already commercial examples. The risk is that generations of technology will advance quickly enough that early adopters may over-pay or be saddled with lower-performing hardware. Thus the impact part of the risk*impact metric contains some measure of the net negative impact on such early adopters.

To keep this in perspective, put PICs in contrast to Electronic ICs. In the latter, the trend described by Moore's Law (not a law, in fact) has described the rapid launch of higher density ICs over time. For much of this trend, the performance also went hand in hand with density, a trend which may be nearing its end, but for at least 30 years there were steady improvements in

integration density and performance. If the same is true for photonic integration in Silicon Photonics then very early adopters may not get the full economic benefits. There is also risk, especially to the design, manufacture, and sales of the IPE products that schedules may slip, performance targets may not be met, and other factors that my increase costs and/or delay revenue. We capture these factors in a risk meter.

Building Block --> / exposed to risk	light source	modulation	waveguides	photo-transduction	control	fab	chip to fiber	packaging	form factor	assembly	test
silicon providers	90	20	50	20	75	100	85	90	75	75	80
packaging house	75	10	10	10	50		95	95	95	95	80
early adopters	85	50	0	0	75	85	80	80	65	65	70
cloud providers	75	50	0	0	40	75	75	75	40	40	50
enterprises	20	0	0	0	10	20	20	20	20	20	20
cloud consumers	35	10	0	0	30	35	35	35	30	30	35



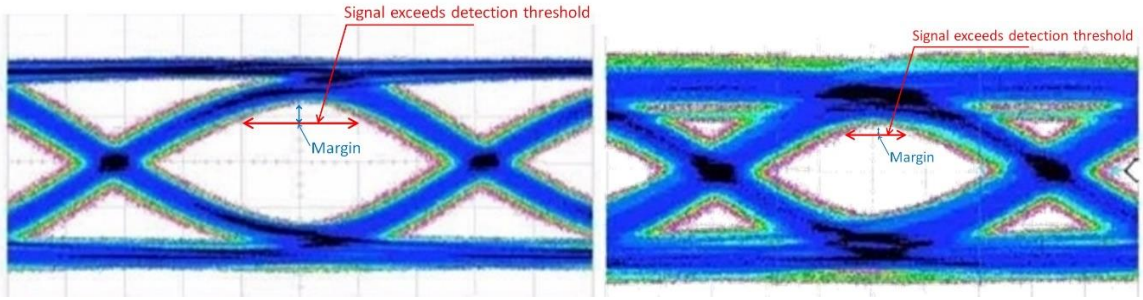
Risk meter for Silicon Photonics. We arrive at the above by looking across 11 key elements needed to deploy a Silicon Photonics solution (see below) and across the perspective of various stakeholders from Silicon Providers to Cloud Consumers. In all, the 66 factors, represented as values from 0 (no risk) to 100 (certainty of loss), are included in the overall risk meter.

In fact, as we have already noted, the term Silicon Photonics is imprecise, as it may mean integration into CMOS, or some other derivative process. In many examples in the research literature, so-called Silicon-on-Insulator substrates are used as the starting point, while in other examples work is focused on working on Silicon as the substrate. There are more subtleties, such as processes using "buffer layers" or "filter layers" between Silicon and some other processes, but they are technical details. There are even "back end" concepts where the wafers go through their complete process to make the desired chips, then are subjected to some additional steps, which might be in a separate line, in order to complete the photonic integration. For the most part, we will refer to Silicon Photonics as the collection of technical advancements that could lead to a viable commercial process and product at some point. It is worth noting as well that there are many individual components required to make an integrated photonic solution. We will focus on some important groups of functionality as follows: (1) light source (laser), (2) modulation, (3) waveguides, (4) photo-transduction (detector), (5) chip to fiber coupling, (6) packaging scheme (meaning the physical integration approach of all components needed for a given chip or "package"), (7) control, (8) test.

The Elephant in the Room: Why do this?

The question remains, why do this? Why pursue the R&D and process development to try to achieve Silicon Photonic devices? The basic answer has to do with signal integrity, losses, energy consumption, data rates, and costs. In general, the longer the line over which electrical signals (which have been modulated to encode data) are transmitted, the more degradation there is in the received signal compared to the original, both in terms of the signal (data) vs. noise, and in terms of loss of power (due to inevitable losses, regardless of the conduction

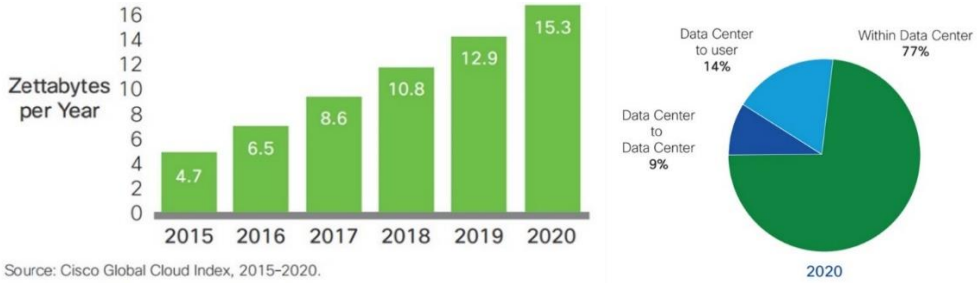
medium). The higher the data rate (often stated in giga bits-per-second: Gb/s; typical values today are 10 Gb/s or 25 Gb/s on one line) the more sensitive the system is to signal degradation. The performance of a given data communication system is commonly viewed using so-called eye diagrams--the more noise, distortion, etc. in the signal, the smaller the eye (clear space in the center of the figures below); at some point there isn't enough margin to reliably send data.



Eye diagrams of a data communication system. On the left is a relatively clean signal--the up and down of the cycle represent the 1s and 0s of the data. The signal is measured many times and all are overlaid; the thickness of the trace then indicates bit to bit noise (jitter, distortion, etc.). To ensure error-free data transmission the signal needs to have enough margin over the noise. On the right, a similar signal with more noise is illustrated with the attendant closing of the eye. Figures adapted from (Sun, 2007).

In addition, longer lines incur more losses in signal power, which reduces the signal to noise ratio. At some point, increasing the power in will no longer work, and intermediary nodes ("repeaters") must be added to receive the signal, clean it up, re-amplify it, and send it on. So for any transmission technology, the greater the distances, the more power is consumed, the more signal degradation occurs, the more difficult it is to operate at high data rates, and/or the more capital is required.

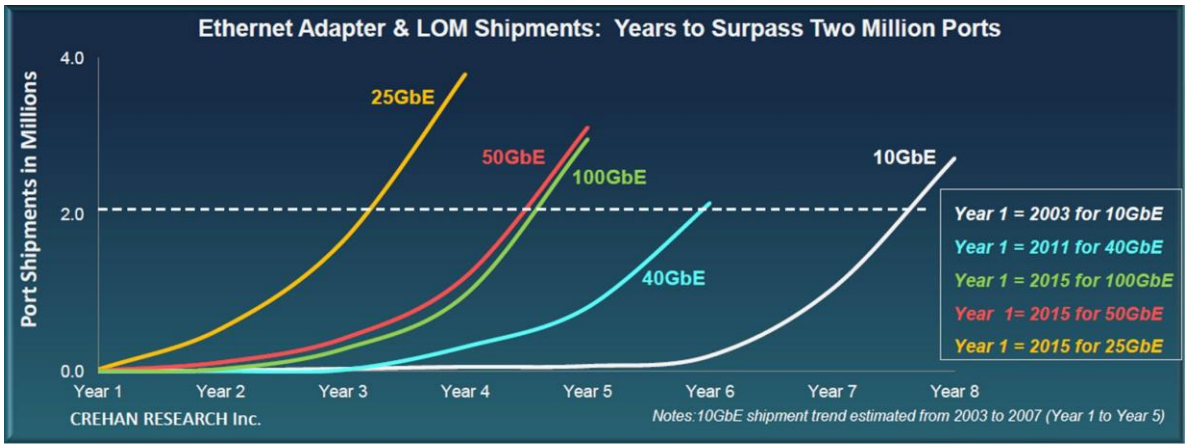
Much of the effort upgrading networks (wired and wireless) and data centers and the underlying electronics is to increase data rates and capacity in as little physical space as possible, while using as little power as possible. On the other hand, the relentless pressure of the end markets is demanding more and more data capacity every moment.



Relentless growth of data traffic will only be met using photonic communications. On the left is Cisco's 2016 forecast for cloud data traffic growth. For data centers the situation is amplified as shown on the right, because for every gigabyte of user data, there are more than 5 times as much data moving within data centers. The traffic staying within the data center include movement to and from storage and other non-user data movement. Interesting, within the rack there are 2x more movement than within the data centers. This will drive photonic communication directly from server to server within racks in the long term (until new de-aggregated servers become a reality--more on that later in the report).

The telecom industry adopted fiber optics to address these needs in the core network part of the ecosystem. In general, photonic transmission technology allows greater distances with lower losses at lower power and higher data rates than electronic transmission over copper wires. The cost-benefit trade off of transmitting electronically vs. photonically has, until now, led to a fairly clear demarcation based on distance. Thus so-called metro area and wide-area ("transport") networks have migrated to photonic transmission, and only more recently have photonic interconnects migrated into data centers. However, the future is very clear that large or hyper-scale data centers will have to be built using photonic communications.

The case that a photonic shift is taking place is also supported by a dramatic change in the uptake of newer, faster Ethernet ports as compared to the transition from 1GbE to 10 GbE. In figure 4, Crehan Research shows that 25GbE ports are ramping about three times as fast as 10 GbE, with 50GbE and 100GbE about 12 months behind. Given the kilometer-scale spread of hyper-scale data centers and the roughly 100m max length for GbE copper, it is clear that these trends contain significant demand for photonic/fiber connections.



Estimates of adoption rates for various Gigabit-class Ethernet ports. Figure source from 2550100.com Alliance, original attribution Crehan Research.

Another data point, regarding the fast ramp of 100GbE, was provided by LightCounting in February 2017, who stated "Total sales of 100GbE transceivers reached $1.15 billion in 2016 up 150% from $460 million in 2015. The number of units shipped was close to 1 million, including more than 700,000 QSFP28 modules. Half of these were shipped in Q4 2016."

Key Point 1:

> *Relentless increases in data traffic drive huge increases in data movement within cloud data centers. This drives pressure to increase communication speeds farther back into the data center, down to the servers themselves. In addition, while 10 Gb Ethernet has been significantly adopted including photonic implementations in data centers, it is likely that 25 Gb Ethernet will deploy much faster, and in parallel to 50 Gb and 100 Gb Ethernet. At these higher speeds and given the physical scale of hyperscale data centers, photonic communication is the only feasible solution at present.*

Today, the photonics, including lasers, PICs, and associated electronics are separated from the data and logic, even at a physical level: there are separate components, such as lasers, photonic integrated circuits (PICs), and electronics. Thus, in a current telecom switch, the data

are all manipulated and routed by traditional computer electronics, then the outgoing signals are converted to photonic data and sent over optical fibers. However, photonic switches have entered the market which allow routing of the photonic signals without the conversions to and from electronic signals.

In contrast, within data centers, the connections between many of the servers, and especially between the servers and the rack switches, are electrical--Cat 6A 10 Gb Ethernet, Cat 8 40 Gb Ethernet etc. Pictures of these massive networks of Ethernet cables are emblematic of today's data centers. The reason data centers are wired and telecoms are fiber has to do with the distances as noted above. At short distances found in typical data centers, electrical network cabling has been adequate. In addition, there are many hybrid configurations deployed to use existing copper Ethernet infrastructure and extend the distances beyond 100m; for instance optical media converters (OMC) integrate to copper CX4 cables, are powered over the copper, and use fiber to extend the range to 300m without additional hardware.

The key factors

But over long distances, the losses and other issues with electrical networking are too large and fiber has become the only solution. The issue is that with increasing data rates and higher data volume, the data centers are reaching limits of electronically handling the data. In fact, data centers are evolving to be larger and larger, pushing the limits of data transmission between servers. Connection distances over 2km may be needed in hyperscale data centers soon; beyond the limit to use copper at the high data rates required.

Another issue facing data center designers, operators, and owners is the server architecture is reaching limits of power density and cooling effectiveness. Server rack architecture has become denser over time, and the blade architecture used in modern data centers allows a very high density of servers per rack. Recently, HPE has offered their "Moonshot" system which further miniaturizes individual servers to "cartridges", allowing 45 servers in one 4.3 U chassis with as many as 180 server nodes.

In fact, server racks have consumed an increasing amount of power rising from 10kW per rack in the early 2000s to 35kW per rack in 2013. Recent improvements have reduced per-rack power consumption, but 20kW per rack is common in high-performance data centers and computing centers. Recent press regarding Facebook's state of the art servers suggests about 17kW per rack of 192 servers. Considering a Facebook data center might have 600,000 servers that is on the order of 50 MW just for the servers. Cooling consumes more power, adding to the total demand.

As well, the power consumption has come under scrutiny for the carbon footprint as well as the scale of total power consumed by data centers. For example, the American Society of Heating, Refrigerating and Air-Conditioning Engineers (ASHRAE) released standard 90.4 2016 in September (2016) which requires detailed design calculations and demonstration of compliance for energy consumption and efficiency of every aspect of data centers from the building systems to server cooling. Emphasizing the issue, the US Ernest Orlando Lawrence Berkeley Laboratory published an update of their report "United States Data Center Energy

Usage Report" stating that current energy consumption by all data centers in the US is over 70B kWh per year, or about 5% of commercial electricity usage. A widely used (albeit controversial) measure of data center energy efficiency is PUE (power usage effectiveness), which is the ratio of total power used by the data center to the power used for the computing equipment, where lower values closer to 1 are better. Facebook's state of the art data centers have PUE < 1.1, and most large data center designs are very focused on efficiency. Nevertheless, in a new data center park in Singapore, Telin-3, it is reported that 17 MW of power is reserved for computing equipment and 8 MW for cooling. With no other losses, and if the reserved power ratio is representative of PUE, then the PUE will be about 1.5, meaning there is a long way to go to get typical data center builds to energy targets.

Thus for economic, environmental, capacity, and cooling limit considerations, there is an urgent need to reduce the power consumption and allow higher density as data demand continues to increase. Silicon photonics is one part of the needed roadmap to solve these issues. We stress that a tremendous amount of effort has been devoted and continues to be devoted to designing and cooling more dense and higher performing cloud data centers, regardless of the interconnect technology. An example is a possible approach using liquid cooling in some parts of the server cooling systems, including a collaboration between Intel (a major Silicon Photonics protagonist), Dell, and eBay.

In fact, the challenge is deeper than only the data movement between server racks--within the server hardware data are moved in electrical form over circuit boards. For example, data out from the CPU routes to the communication module via copper transmission lines. Above 25 Gb/s it becomes a problem to send data over these circuits even for a meter or less, as losses can be very high. For example, using standard FR4 and copper lines, losses at 25 Gb/s can be over 1 dB per inch. Losses can be reduced with lower loss board, thicker copper, and processing to make lines very smooth--all such approaches add significant costs. Thus, this situation leads to looking into photonic transmission within the servers themselves. There are solutions being deployed to implement optical backplanes, adding additional hardware layers and cost. Finally, even higher data rates, such as 100 Gb/s on one channel, are pushing the limits of the interconnects at the chipset level. In these cases, there is no stop-gap solution, as the photonic interconnect needs to be directly integrated with the electronic chipset. Silicon photonics is viewed as the only roadmap for this evolution.

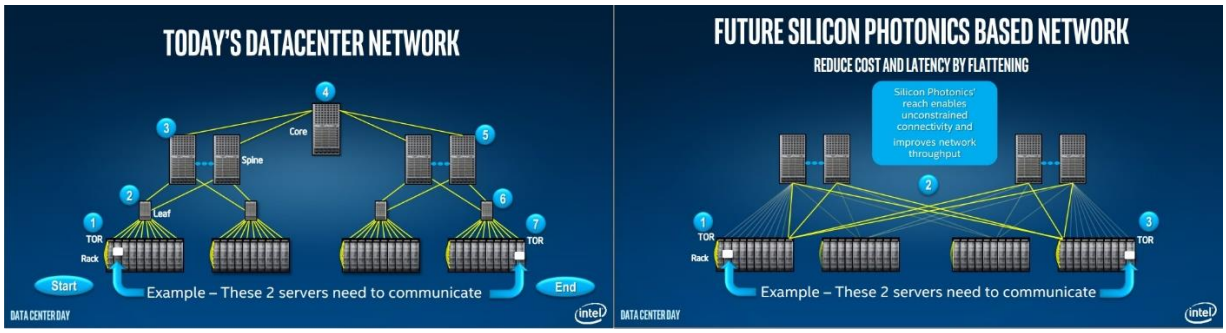
Key Point 2:

> *Telecom networks have used photonic transmission for a long time. As data rates constantly increase, data centers will need to migrate to photonic data connections throughout the architecture. The key tradeoffs are cost, signal integrity, losses, and energy consumption vs. data rates and distance. Before long, even the transmission of data within the servers will need to be photonic, and eventually from chip to chip. Silicon photonics is viewed as a path to integrate the needed photonic functionality with the electronics (processing etc.) without incurring large cost penalties and while lowering energy consumption.*

The situation is evolving as the amounts of data increase and equipment makers respond with faster servers--in fact there has always been a combination of speed and distance that drives

the hardware solutions. Gigabit Ethernet was developed to address demands for increased data rates; before there was commercial equipment to generate data at these rates, older technology was fine. The two sides of this equation: demand vs. capability have been on a see saw from the beginning--increased demand pushes development of faster technology, faster technology leads to more demand. The demand now is pushing development of 100 Gb/s technology. As noted above, limits are being reached even in the server hardware; 25 Gb/s and above transmission requires using more exotic materials for the circuit boards (e.g. PTFE vs. phenolic), more precise about interconnect design, and so forth, all of which increase costs. Yet all these incremental improvements may not be enough as the industry moves to 100 Gb/s channels and above in data centers.

So, it is believed that the connections between all the servers--all the cables--will have to be replaced with fiber optic cables, which means every server blade will require a set of lasers, PICs, etc. to convert electronic data to photonic and vice-versa. Likewise, to communicate within the servers photonically will require integration of photonics into the server boards. However, even with state-of-the-art solutions today, the size and cost and power demand to convert the entire interconnect system of a data center to fiber optics are not acceptable. Silicon Photonics is perceived to be a solution where all the integration of the electrical and photonic signals occurs at the chip level or board level instead of externally, dramatically lowering costs and complexity, and, perhaps most importantly, lowering power demand. This is made clear by Intel's publicly shared plans from an August 2015 Data Center Day.



Two slides from Intel presentation by Alexis Bjorlin Vice President, General Manager, Silicon Photonics Solutions Group, at Data Center Day, August 27, 2015. Intel's position is that Silicon Photonics, and Intel's first product of a 100 Gb/s 2km link, is enabling to future, flatter, lower latency architectures, needed to enable the ever higher intra-data center data rates. Source: Intel.

Key Point 3:

> *Silicon Photonics can enable a new design paradigm for data center and server design. To fully benefit from the paradigm, significant changes to the core hardware will take place, meaning products are more likely to appear in new data centers sooner than upgrades.*

Large server and data center consumers like Facebook, Tencent, eBay, Amazon, Google, Baidu, Microsoft and others are early targets for products using these technologies. Facebook proposes to go even further, having announced a partnership with Intel aimed at separating functionalities like CPU, memory, switching, communications etc. into distinct modules within

servers. Advantages of such an approach could be to allow easier upgrade paths (i.e. just replace the CPU modules), more design flexibility at the data center deployment level, and possibly cost advantages if more of the content in a server rack becomes standardized. However, for such approaches to work, the components that are disaggregated will require photonic interconnect to enable the interconnect speeds to minimize latencies and losses, as well as to reduce the power required to run such servers. While all these possibilities exist, in the near team the main target is to replace the copper Ethernet connections within the data center between all the servers/switches with fiber optics driven by integrated photonic-electronic devices, as well as in any switches.

As IPE (integrated photonic-electronic) devices reach mass production and deployment, systems designed and produced with these devices will have cost and performance advantages. The cost equation for data centers includes not only the capital expenditure (capex) but the ongoing operation costs (operations expenses, or opex). Opex is driven by power and cooling costs, software costs, and personnel costs. Since software is usually quoted per core, these costs will continue to scale more or less linearly with capacity. Personnel costs are subject to some economies of scale and thus scale non-linearly slower than capacity. Minimizing power usage, which also reduces cooling requirements, and reducing facility footprint per core are therefore key points of control. It is expected that IPE will reduce the power consumption of the servers, allowing even more dense packing of server blades into racks, with attendant further reductions in capex.

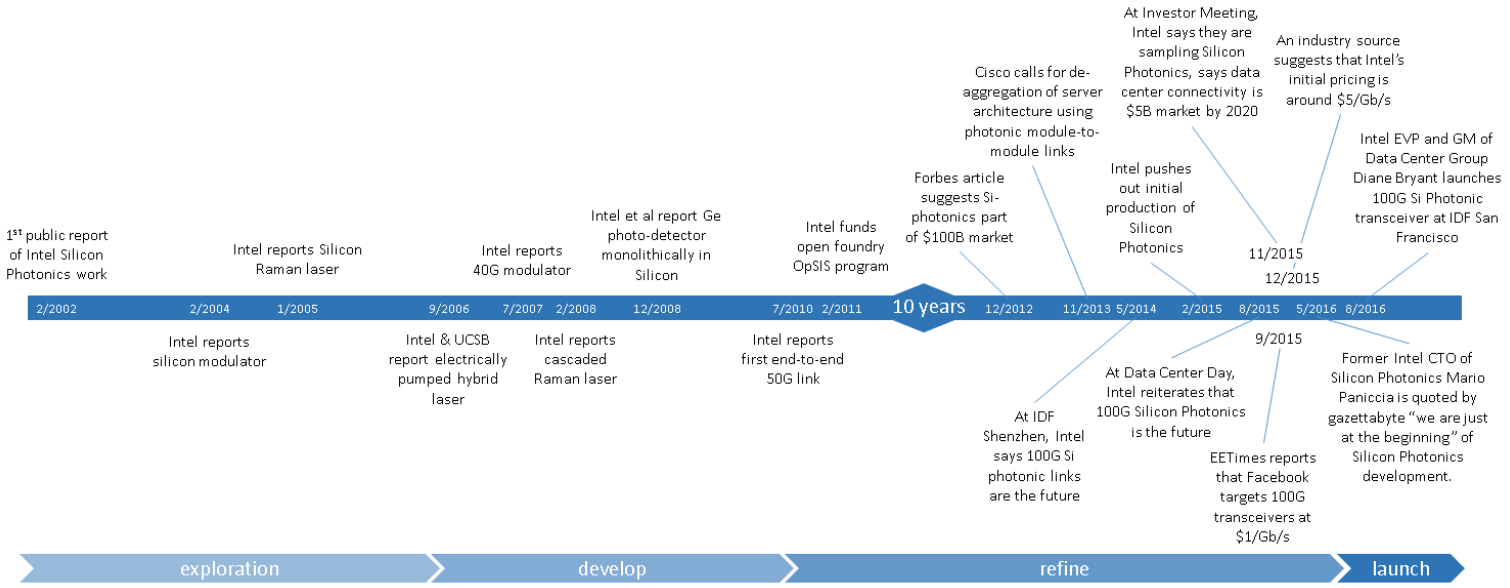
Key Point 4:

> *Once a generation of photonically enabled servers is commercialized, costs will fall rapidly. In addition, prices for "traditional" data center hardware may fall in response. Enterprises and data center operators will need to make decisions even while the technology is still evolving.*

This report will assist you in considering the impact of the evolution of technologies, performance, and costs. Many of the above statements apply equally to the large enterprise data centers as well as cloud providers, although migration of enterprise to the cloud is already occurring. IT business units will have to develop a strategy about deployment of new technologies and weigh the risk/cost/benefits. It may make sense both financially and from an obsolescence-risk avoidance viewpoint to migrate to the cloud sooner. The information here should help with those thought processes as well. Services which depend on these technological transformations will likely decline in cost per performance metric, creating pressure on smaller providers as well as enabling early adopters to offer even more performance. On the other hand, as the technology of Silicon Photonics is rapidly evolving, early adopters will be exposed to risk that early-fielded technology may not be the long-term best solution.

Intel's work in Silicon Photonics has been widely reported. Looking at the timeline in Figure 5, we can see that Intel has about 15 years of R&D invested in Silicon Photonics *so far*. An obvious question, given Intel's main role in data centers as providing processors for serves and compute workloads, is "why?". The answer is hinted at by the Forbes' reference to a $100B market, as compared to Intel's own statements of a $5B market. Intel's data center strategy is to own as

much of the silicon as possible, and to transform the connectivity architecture by dramatically changing the cost/performance of the photonic interconnects. Longer term, we think Intel expects to integrate photonics back to processors and other modules, leveraging the technology developed for discrete interconnect.



Timeline of Intel Silicon Photonic development. The huge investment in R&D cost and time argues that Intel is looking at the opportunity much more broadly than existing interconnect markets.

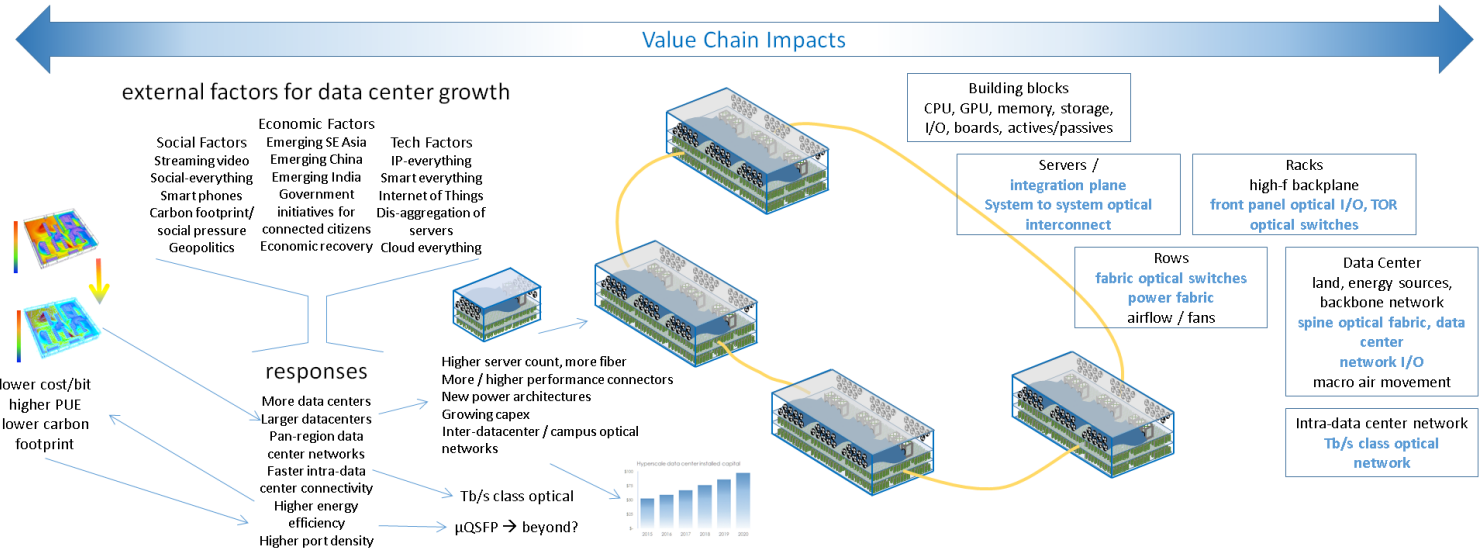
Key Point 5:

Data center connectivity architecture needs to change to meet future traffic demands. Lower cost Silicon Photonics is an enabler to a flatter connectivity paradigm. In addition, the technology will continue to evolve and integrate deeper into servers, enabling another paradigm shift in server design. In essence, Silicon Photonics will be at the heart of data center design, but that may take another 10 years.

Value Chain Impact

It is worth considering at this point the potentially vast impact IPE devices may have. A highly simplified macro-economic model of the value chain might look as shown in Figure 6. From the data capacity and speed viewpoint, deploying Silicon Photonics in a data center will reduce the energy cost per bit and/or increase the throughput per dollar. For the data center owner/operator, this translates directly into lower operating costs at a given capacity. Note there are other impacts, such as more flexibility of location (large data centers today are located near power sources) or reputation effects by lowering carbon footprint. If new data centers are significantly less costly per bit to operate, the rate of build of new data centers will increase, vs. applying stop-gap upgrades to existing centers (this build out can be taken to include replacing servers in existing facilities), since demand is forecast to keep increasing for some time. If new hyperscale data centers have large cost advantages, migration of enterprise

data centers to the cloud will accelerate. This increased build out leads to more spend in the supply chain for data center construction and deployment. There are potential negative implications as well; we will explore these further later in the report. As we will discuss later, the actual value chain incorporating Silicon Photonics is large and complex. If this technology spreads across many different aspects of a larger value chain, the cumulative impact is proportionately larger.



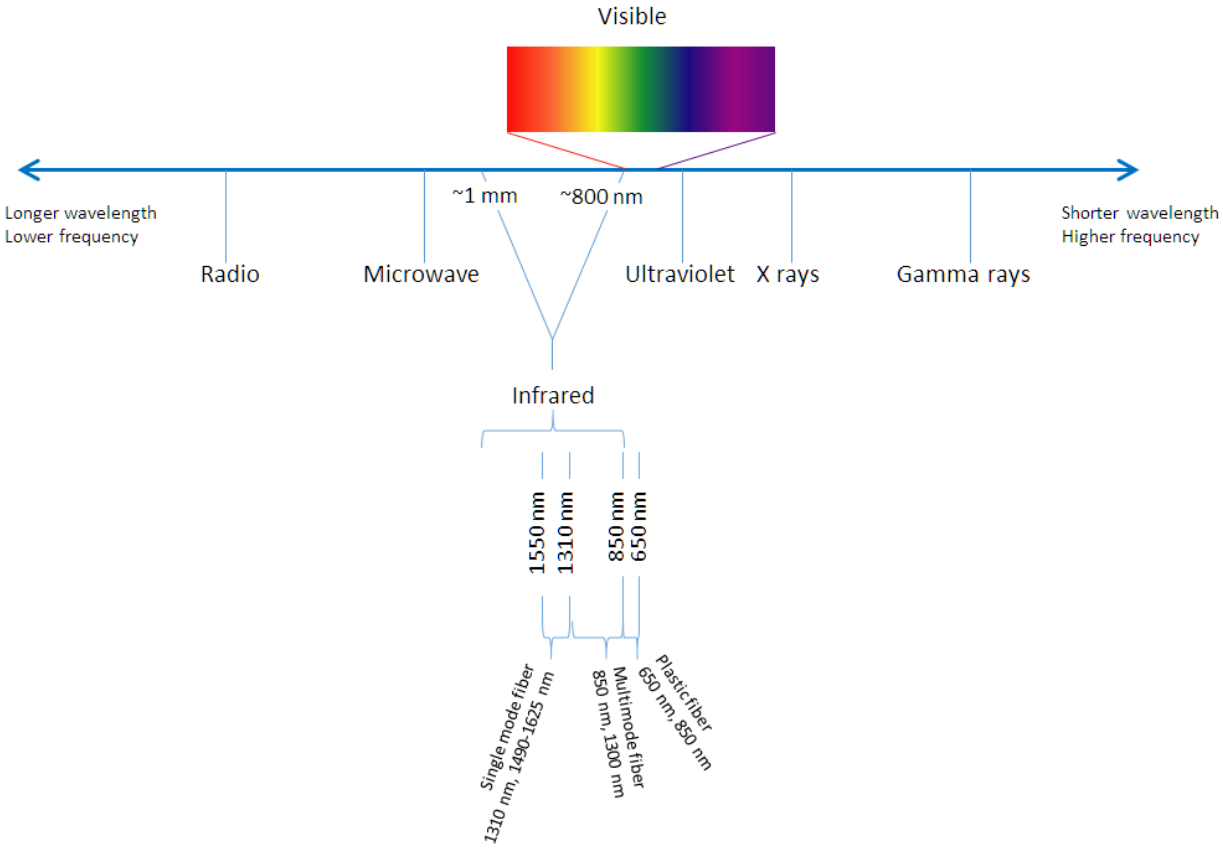
A simplified depiction of the impacts of acceleration of bandwidth increases in data center connections, enabled by low-cost Silicon Photonics.

Key Point 6:

Whether you are an IT consumer of hardware or services, or in some other part of the value chain, this report will help you frame your thinking and reduce the risk to your strategy of being unaware of possible huge shifts.

Photonic Integrated Circuits

In this section we review the motivation and development of Photonic Integrated Circuits (PICs), then explain the case for Silicon Photonics as the path to Integrated Photonic Electronic (IPE) Circuits. In general, a PIC is the combination of multiple functionalities such as filters, resonators, modulators, waveguides, polarization rotators, etc. that are necessary to manipulate photons such that data can be encoded and communicated over optical fibers. Most PICs use Indium Phosphide (InP) or Lithium Niobate (LiNbO3) as the platform. Silicon Photonics aims to use silicon/silica as the platform. To be practically useful, PICs must operate at particular wavelength ranges that coincide with the wavelengths of lowest loss in optical fibers. As shown in the figure, these are in the near-infrared from 850 nm to 1550 nm. Some plastic fiber operates in the visible using red light but such fiber is not used for high-throughput data transmission. Thus, for the purposes here we are talking about infra-red light.



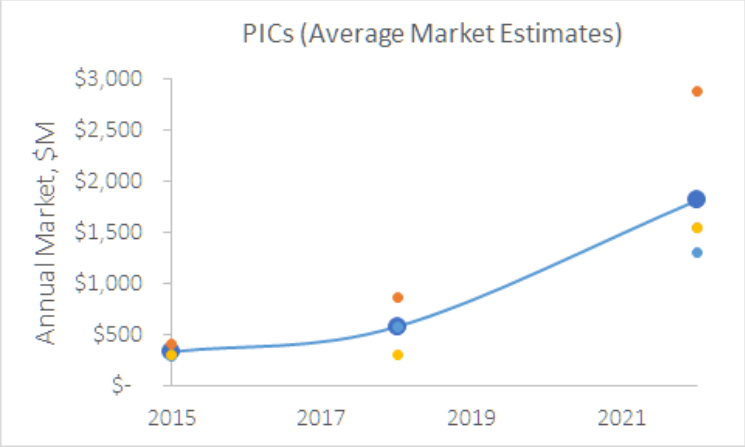
It is popular to make statements like "Photonic Integrated Circuits (PICs) are the equivalent of electronic integrated circuits (EICs) except with photons instead of electrons" or similar. Although from a behavioral point of view that may be acceptable (at least for some behaviors), from an historical point of view as well as a physics point of view such a description leaves room for improvement. Importantly, electrons are charged, being the basis for electric current, which is the flow of electrons as a result of a voltage difference (in the case of a wire). Photons are not charged, and are relatively immune to electric (and magnetic) fields which is a plus in terms of signal immunity to EM (electro-magnetic) noise, but a challenge if you want to truly make a PIC that does the same functions as an electronic integrated circuit, such as switching or diode

behavior of photons, or photonic transistors. (Note--progress is ongoing developing EIC functionalities with photons, but most of that is outside the scope of this report.) Thus, at the functional component level, there are important differences between PICs and EICs, and there are useful similarities.

Ivan Kaminow, lifetime IEEE fellow (deceased in 2013), long-time Bell Labs employee with both BS and MS degrees in Electrical Engineering and a PhD in applied physics, related that the idea of a PIC existed nearly from the year the transistor was invented. Meint Smit and his colleagues at Technische Universiteit Eindhoven showed that the first realization of a PIC was in 1988 or 1989. It took only 11 years to realize the first EIC after the transistor (from ca 1947 to ca 1958), and another 10 to realize the first microprocessor (ca 1958 to ca 1968). Yet for PICs it took 40 years from the conception of the PIC for one to be commercially realized. At this pace, we might see photonic processors in a commercial product by 2028 (not a forecast, only an observation). Since the architecture of photonic communications can be embodied by combining discrete photonics with controlling electronics, it is commercially useful to integrate multiple photonic components into PICs which integrate with EICs and microprocessors to form systems. The PIC market really took off in the 2000s with companies like Infinera, 2000s Photonics, Finisar and others providing innovative products.

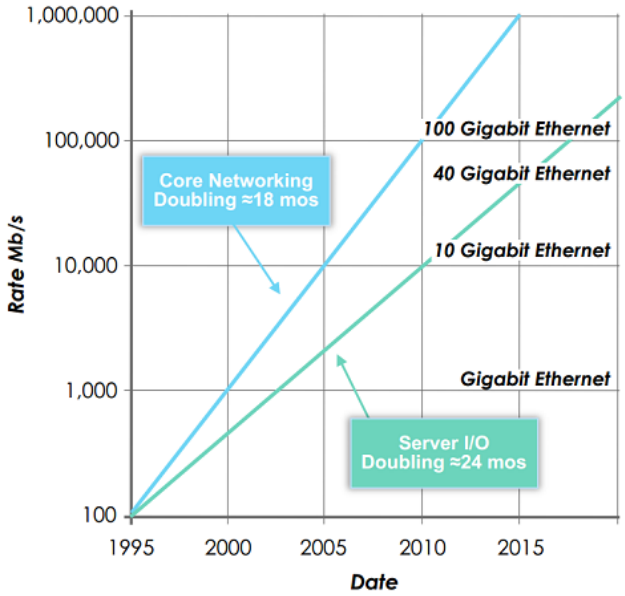
It is important to note that development of a design and manufacturing ecosystem has been occurring for InP PICs for some time, and has a good level of maturity. A good overview of the state of the art in InP PIC integration was published by Eindhoven University of Technology in August 2015. The authors noted at that time that "More than 250 custom chips have now been produced at Oclaro, Fraunhofer HHI, and Smart Photonics using JePPIX Open Access brokering." While significant effort has been devoted to developing similar maturity for Silicon Photonics, in some sense Silicon Photonics is behind and catching up. At present, it is unrealistic to think Silicon Photonics PICs can displace existing applications in all cases, at least for many years.

By 2015 the PIC market was over $300M, and forecast to be nearly $600M by 2018 and over $1.8B by 2022. As we noted in the introduction, markets estimates for Silicon Photonics are in the same range, primarily from penetration of the data center market. The implication is that Silicon Photonics will significantly increase the total PIC market.



Average of published market estimates. Source: EAF.

The growth of the PIC market is self-reinforced by the advances in technology. By this we mean that as technology becomes available to allow higher bit rates, lower costs, and lower power consumption, the market quickly evolves to demand more bandwidth. This is a Moore's Law situation--the market now expects ongoing performance gains for communications (both fixed and mobile, but increasingly mobile), and achieving such gains implies upgrades to the underlying infrastructure. Thus a first mover advantage accrues to any supplier who can launch a product with improved performance first. As perspective, consider that in the 1980s tens of Megabits per second was state of the art for photonic data transmission, by the early 2000s Gigabit (Gb/s) Ethernet was available, and today there is 40 Gb/s Ethernet, and 100 Gb/s solutions are being released.



Source: The Ethernet Alliance, "Bandwidth Growth and the Next Speed of Ethernet".

Silicon is a semiconductor material and is used as the basis for most EICs. Silicon-based electronics manufacturing has matured and a set of processes are used across the industry--the so-called CMOS (Complementary Metal-Oxide Semiconductor) process is well understood throughout the electronics manufacturing industry globally. Silicon photonics may mean a number of things, but for our purposes here can be viewed as accomplishing photonic integration in a process compatible with existing CMOS foundries (thereby leveraging decades of learning and billions of dollars of investment). In this context the goal for Silicon Photonics would then be to integrate all optical functions currently carried out in PICs, with the added feature of directly or closely integrating the PIC and the electronics. The goal also includes an electrically driven laser source integrated into the package.

Light source integration

A significant challenge is that any integrated photonic solution needs a laser light source for transmission, and photo-detectors for reception. As noted elsewhere, Silicon has an indirect band gap structure and cannot (easily) be made to emit light. This leads to various approaches to create or integrate a light source in a Silicon process. One approach is to create a laser using

crystal materials that can emit light (the same as existing PICs), and *assemble* it to the in-process Silicon wafer--this is called heterogeneous integration and departs from standard CMOS, although may be considered CMOS-compatible. A large and growing body of research is devoted to finding monolithic pathways to a light source in CMOS-compatible (or nearly so) processes. Nevertheless, heterogeneous processes are commercialized (Luxtera, Skorpios, IBM, Aurrion, and others) and more are coming (e.g. Intel). To understand the importance of the milestone of a complete integrated photonic process in CMOS, it is useful to consider the benefits that have already accrued from photonic integration.

PIC Material Platform

There are a number of material platforms used for PICs; the most commercially used today are InP (Indium Phosphide) and $LiNbO_3$ (Lithium Niobate) yet there are many others such as GaAs (Gallium Arsenide), InGaAs, and others. The choice of material depends on many factors; using a so-called III-V material (InP is a member of that group of materials, for example) has the added benefit that such materials can be made to generate light. In many cases, more complex crystal materials are used made from three, four, or more elements. To create a PIC requires processing similar to that used for electronic semiconductors, starting from crystal wafers then proceeding through a variety of processes to "grow" desired material on the wafer and use lithography to create the desired features (e.g. waveguides).

Consider the problem of encoding electronic (digital) information into modulated (controlled) light and sending it over a fiber optic cable then decoding it back into electronic signals. The idea of sending information over an optical waveguide dates well back into the 1800s. The realization from around the 1950s that data could be sent over long distances at lower cost using fiber optics and lasers instead of copper wires transformed the telecommunications industries and allowed development of the Internet as we know it today. It is well documented that both fiber optic communication as well as modern photonics "began" with the invention of the solid state ruby laser in 1960. As with other photonic developments already noted, it took 10s of years to commercially realize an effective fiber optic data link after the basic ideas were in place, with significant commercial applications appearing in the 1970s. These systems relied on expensive discrete components to handle all the different functionalities needed to encode and decode data.

Returning to the design of such systems, the key requirements are a light source (laser), the power source and pump for the laser, a modulation scheme (to convert continuous wave (CW) light into information encoded into pulses) and the electronics to drive that, electronics to generate the encoded information, and a coupling scheme to couple a fiber optic to the output of the laser. In 1977 the first commercial systems were used, by General Telephone and Electronics in Long Beach, CA (achieving 6 Mbit s) and by AT&T in Chicago (achieving 45 Mbit/s). These systems used GaAlAs lasers and had limited range due to losses in the optical fibers of several dB per kilometer. Technology advanced (relatively) rapidly from those early demonstrations to the situation today where long-haul and metro-distance telecommunications are sent predominately over fiber optics. It is worth pointing out that the wavelength of the light used had to match the points where the fiber optics had low loss; in other words system designers are not free to arbitrarily choose a source and a fiber independent of one another.

Advanced modulation formats

As demand for faster speeds and higher bandwidth have grown continuously since the late 1970s, pressure arose to use spectrum as efficiently as possible, add more channels, reduce crosstalk between channels, miniaturize the systems, and reduce power consumption. There are various ways to split up a given light source into multiple channels. Importantly, the optical system must separate out narrow wavelength bands so that separate data streams can be sent on each narrow band (channel) without interfering with other channels (crosstalk). Modulation schemes may also be used to increase the total capacity of a system. Limits arise, for example, from the dispersion of a given wavelength as the light travels along a fiber and other processes. For a given channel spacing, there is some maximum distance beyond which the information cannot be decoded correctly. Systems used today employ schemes such as CWDM (Coarse Wavelength Division Multiplexing) and DWDM (Dense Wavelength Division Multiplexing) to increase the amount of data that can be transported.

In addition to limits on the channel spacing and distance, since information is encoded as bits, dispersion also places bounds on the bit rate, since the higher the rate, the shorter the on/off cycles are in time, which again means at some distance the bits cannot be properly decoded. This is an ongoing area of development as owners of existing fiber optic cable seek to extend their capacity. Techniques such as deterministically correcting for distortion or adding additional electronics, for example, are being studied to increase fiber capacity. The modulation schemes already use properties such as phase angle and polarization to encode more information in a given fiber. Thus, these complex modulation schemes and channel multiplexing are targeted to be implemented in Silicon Photonics.

It is somewhat intuitive to think that if the discrete hardware used in the 1970s could be integrated into one or a few modules, it would save costs. However, to compare those primitive examples to later systems isn't really illustrative due to the rapid advancements in laser and fiber optic technology that took place. Nonetheless, at some point having hundreds of lasers, multiplexers, filters, modulators, detectors, and all the other necessary components in a space of reasonable size and of acceptable power consumption becomes problematic. This, then, is part of what motivates developing PICs--modern telecommunications and data communications depend on integration of hundreds of components in PICs, which are then integrated with the necessary electronics, thermal management, and fiber optics to create end to end systems.

Motivation to develop PICs was illustrated by an example from PIC leader Infinera in a 2007 white paper. "Large-scale photonic integration on InP has since shown promise for enabling even greater functional integration. For example, R&D efforts have demonstrated a DWDM transmit PIC which integrated ten DFB lasers with ten modulators operating at 40Gb/s with associated control devices and WDM multiplexer, having a total data transmission capacity of 400Gb/s on a single chip.

"This component, which unpackaged is the size of a fingernail, would typically require two to three racks of discrete optical devices in a conventional DWDM system to provide the same capacity. In parallel other R&D activities have shown the ability to increase PIC channel counts,

such as integrating twenty or more DWDM channels into a single device, or increasing the degree of functional integration by integrating additional optical functions into a PIC."

The potential for orders of magnitude improvements was further detailed in a November 2011 presentation by PIC market player Luxtera that detailed the needs of data centers:

"Data Center Needs at 100Gbps

Low cost transceivers
- Very low cost at ~ 150m
- Low cost at ~2, 000m

Low power consumption

Small form-factors
- High front panel density

Multi-sourcing
- Multi-vendor interoperable"

In the same presentation, Luxtera points out some targets regarding a fully integrated Silicon Photonics solution with an ASIC:

"100G Silicon Photonics Integration with ASICs

Power per 100G
- Parallel: < 3pJ/bit
- WDM: < 10pJ/bit

Cost for 100G Transceiver
- ~90% lower than conventional
- Optically compatible to modules and embedded optics"

To summarize, getting to fully integrated Silicon PICs could result in a cost 1/10 or less of that available in the market, with potentially lower power consumption, and dramatically smaller form factors to enable higher server rack back panel density (to allow more connections at higher bit rates in a given area).

Although we have referred mainly to telecommunications, and the need to send information over long distances, we can consider the combination of data rate, capacity, and distance to be the driver to use photonics and electronics vs. just copper wire and electronics. Thus, at high enough data rates and high enough capacity, even at relatively short distances photonics will be preferred over electronics alone. Optical networks are often described in distance tiers or segments. For example, long-haul may describe distances over 1000 km. Distances from 500 km to 1000 km are described as Metro-Regional, then Metro-Core and Metro-Access bounded by < 500km and < 100km, respectively. Past the short distance end of the distance hierarchy lie data centers, which can have data cable reaches up to 2 km. Data centers are characterized by high processor and interconnect density, both of which are increasing steadily. Until the internet era, data centers were small by comparison to telecom network distances (more likely to be called the server room or network closet at that time).

As platforms like Google, eBay, and Facebook emerged, new classes of data centers were constructed which were quite large by comparison. Like many manufacturers looking to use excess capacity, companies like Amazon created AWS (Amazon Web Services) and the cloud era emerged in parallel to the e-commerce and social media explosions. Data centers require high-throughput, high-capacity, and low-latency (delay) connections between servers to provide the customer experience desired. As is documented ubiquitously, demands for Internet capacity are growing exponentially, driven by mobile data traffic, streaming music and video services, and cloud virtualization of everything from data to applications to infrastructure.

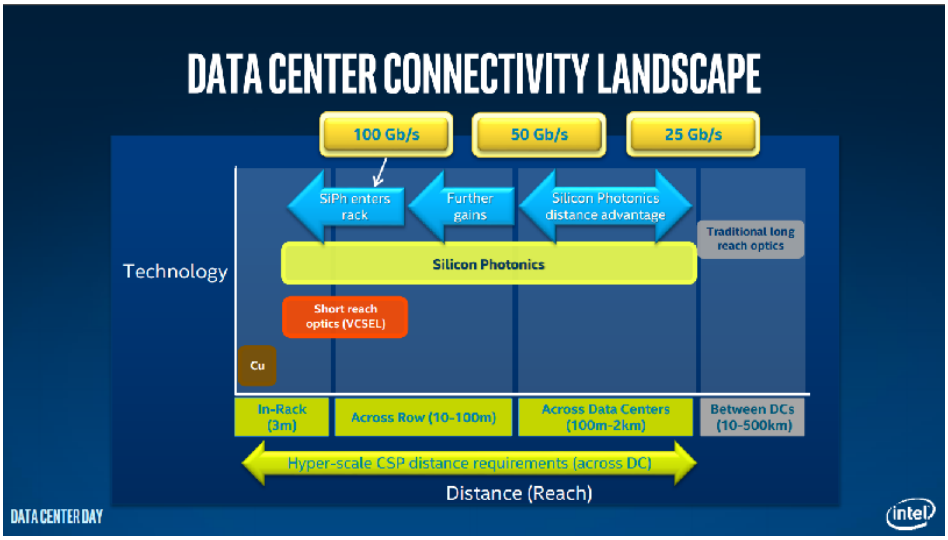
Given these trends, we find ourselves in the -aaS era: "as a service" now applies to cloud-based applications, or "AaaS", all the way to infrastructure, or "IaaS". The latter development, which allows businesses to house all their software and data in the cloud, is something of a seismic shift: servers and network equipment that formerly resided in enterprise data centers is now concentrated in cloud data centers (although there are plenty of enterprise data centers and more continue to be built, including hybrid systems with some on premise and some in the cloud). Thus, thousands of enterprise servers are located in mega-data centers operated by provides such as Microsoft (Azure), Amazon (AWS), IBM (Bluemix), Google (Google Cloud Platform), and RackSpace (Public Cloud), among others.

Source: Gartner, June 2015

This demand in turn has led to construction of ever larger data centers, with even higher data rate, capacity, and lower latency requirements. These requirements have in turn led to deployment of ever higher-speed interconnect in data centers, including optical interconnects. (Note: there are other users of high-performance data centers than the internet and cloud services, including financial networks, trading networks, high-performance computing, and government uses. All of these applications create similar pressure on interconnect performance.)

The challenge for data centers, even with optical interconnect, has some unique characteristics over the predecessor telecom requirements. As noted, data centers have high interconnect density. Servers have also become denser to keep up with demand; in fact a single server rack in a large data center may have hundreds of CPUs and consume kW of electrical power and cooling power. Intel, among others, has pointed out that data centers are undergoing a transformation, driven by "unprecedented" growth in capacity, number of servers, and interconnects, very large physical scale (2 km in a single building) and migration of vast amounts of data to the cloud. This leads to a key tenet driving integration beyond that achieved in PICs alone--the need for Silicon Photonics to enable optical interconnect not only between racks and across rows, but within racks themselves.

While at present Silicon Photonics may not be considered the only solution for server interconnects, links to switches, and switch architecture (given the potential for PIC-based interconnects to continue improving in performance), the bandwidth requirements will force the need for optical interconnects within a server rack and eventually within a single processor board. At that point, Silicon Photonics may be the only feasible solution. To reach that level of integration, Silicon Photonics may be used first in the longer distance interconnects, and likely compete with current PIC approaches for 100G connections.



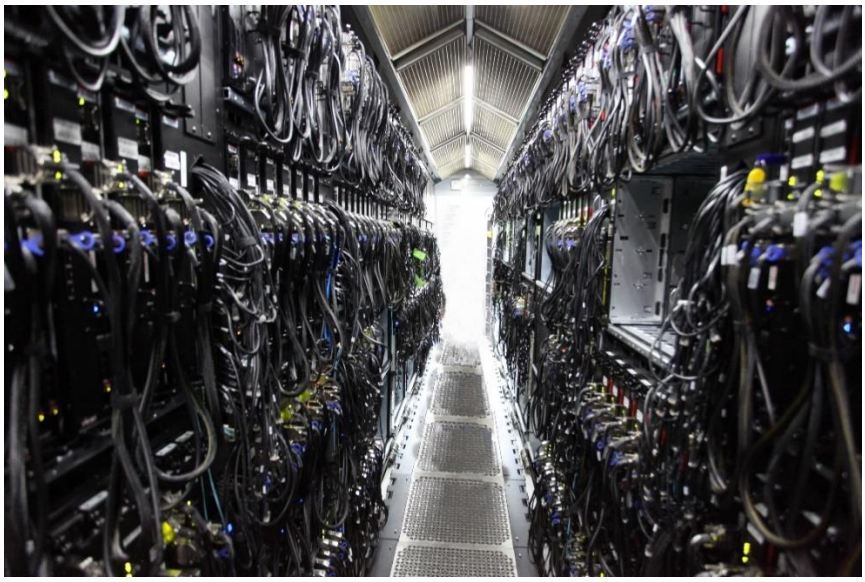
Source: Intel

The intent here is not to provide a complete history or description of Photonic Integrated Circuits, but rather to help you understand why Silicon Photonics is different and important. Silicon also has many desirable properties for photonic circuits, including allowing for extreme miniaturization of components such as resonators, filters, waveguides, couplers, and others. Due to the large difference in refractive index between Si and its natural oxide (SiO2, also known as silica) (3.5 vs. 1.45, respectively), structures like waveguides are also very narrow. As waveguides for photonics are the analogue of circuit traces for electronics, narrow waveguides mean they can be very close together and turn sharp corners, both highly desirable features for a commercial device. However, Silicon photonic circuits on their own do not compare favorably to, for instance, InP platforms. Among a variety of design factors, Silicon Photonic circuits incur relatively high losses of the optical signals, and cannot directly support light generation in a way

useful for off-chip communications. Thus, if this were the entire story, the chapter would be closed on Silicon as a photonic material; however, there is more to the story.

(Too?) Many Material Choices

The diversity of materials and processes under the PIC umbrella is a stumbling block for integration of photonics with electronics and achieving economies of scale. Having so many materials and processes for PICs multiplies the learning curve and exposes any proposed integrated photonic-electronic device to high capital costs. On the other hand, it is difficult for a given technology to scale in volume to reach the economies of scale already achieved in CMOS electronics production. Thus, to leverage existing infrastructure and capacity, Silicon Photonics may be the most attractive route to fully integrate PIC capability with IPE devices, using the definition of Silicon Photonics that it is made in a CMOS fab.



Source: "Explore a Google data center with Street View", https://www.youtube.com/watch?v=avP5d16wEp0.

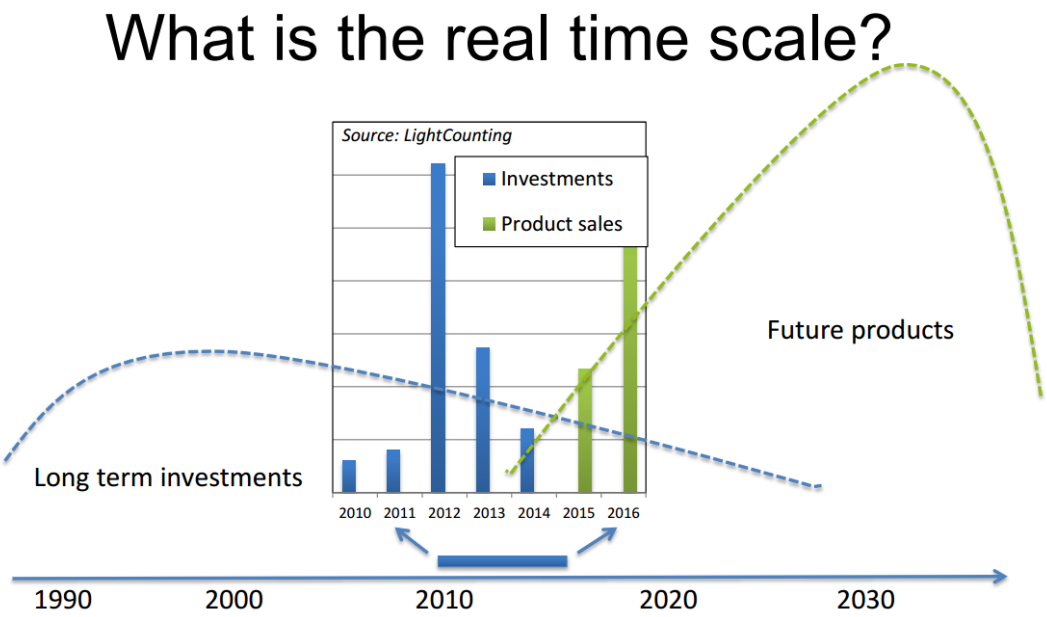
If we look at connectivity in data centers, nearly everyone has seen pictures of huge warehouses of servers with cables everywhere. One of the challenges with data centers is that there is a certain physical size of the server blades, for example, which, although it has shrunk significantly, may run up against a limit to how many connections (to other servers, switches, storage, etc.) can fit in the physical plane (the "front" or the "back" plane of the server enclosure). In modern data centers, it is important to be able to plug in new blades, swapping for ones in need of repair, as well as to unplug and plug the connections. There are minimum sizes of pluggable interconnects for a given data rate. Thus, as the capacity and speed of the CPUs increases to meet the demands of cloud performance and throughput, there is a need to increase the density of the connections as well as their speed. Although performance is increasing quickly, a typical blade might offer 4 x 10 GbE ports on the panel. Systems are being upgraded and EIC exchanging 1 GbE for 10 GbE or 40 GbE. The net of this is that the connections need to get smaller as well as increase in performance and reduce power consumption. Silicon Photonics is viewed as a way to address these needs.

So we started out talking about the history of Photonic Integrated Circuits and how Silicon Photonics might evolve. We essentially set a baseline that we want all the PIC capability available today in discrete PICs combined with an in-package light source and fiber connection. We wrapped up with a simple conclusion that data center needs in the future could be met with integrated Silicon Photonics providing more capability than current solutions. We will show in the next section that Silicon PIC integration has already reached the number of components achieved in InP PIC integration, and is increasing at a higher rate than that for InP platforms. Combining all the factors we have reviewed shows there is considerable momentum to bring Silicon Photonics to widespread commercialization and we should expect rapid increases in integration level and product performance.

Silicon Photonics Technology Development—Status and Risk

Technology development loves hype cycles, to borrow a term from research firm Gartner. In an environment where early risk is often the burden of startups, hype brings in funding, and increases multiples when it comes time to monetize. Silicon Photonics is no exception. As reported by Yole Developpement, a premier research firm that follows photonics, during the first part of the 21st century, billions of dollars have been paid out to acquire Silicon Photonic startups. Billions more have been spent on R&D. This in a market that is forecast by several research firms to be worth less than $1B even by 2020 or later.

So, it is fair to ask "will it ever be finished" or "will it ever reach mass commercialization"? As with many highly technical developments in electronics, part of that answer requires science, R&D, and technology development perspectives to answer. Part of the answer certainly comes from whether enough money is ultimately available at the right time, and if the money goes to the right places. As interesting as that is, in this section the goal is to inform, if possible, the first part of the answer. An interesting perspective is that of premier market analysis firm LightCounting, from September 2016, as shown in the following figure.



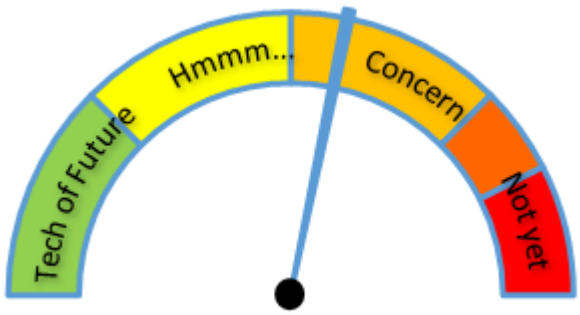
An analysis of the time horizon for the Silicon Photonics market, presented by LightCounting at ECOC 2015. The message is that the sales market is nearly at the beginning of a multi-decade life cycle. Source: LightCounting, used with permission.

The notion of risk depends heavily on your perspective. What may seem unacceptably risky to a well-established corporation might seem just fine for a start-up, especially if the start-up is well funded. Risk looks different from an investment perspective than from a cash point of view. Here, we loosely define risk as "the likelihood of overpaying, being saddled with obsolete deployments, losing money on dead-end developments" and other things of this nature. Note that we are not defining risk as "the likelihood it won't work"; given that there are already commercial deployments of some forms of Silicon Photonics (not the least of which are Intel's

new products just announced) (August 17, 2016), we think that perspective isn't useful at this point. Instead, most of the risk, in our view, is that the technology is evolving so fast, and will continue to do so, that products will come to market with very short life-cycles, only to be replaced by products with more features, lower costs, better performance, or all three. A good perspective regarding the notion that Silicon Photonics is still in the early adopter phase might be comments published recently by imec's Phillipe Absil, who noted that it is "not yet clear that those solutions today can scale down to have optical engines directly integrated into switches for instance, where maybe different packaging solutions would be yet required to mimic what exists today in CMOS technologies."

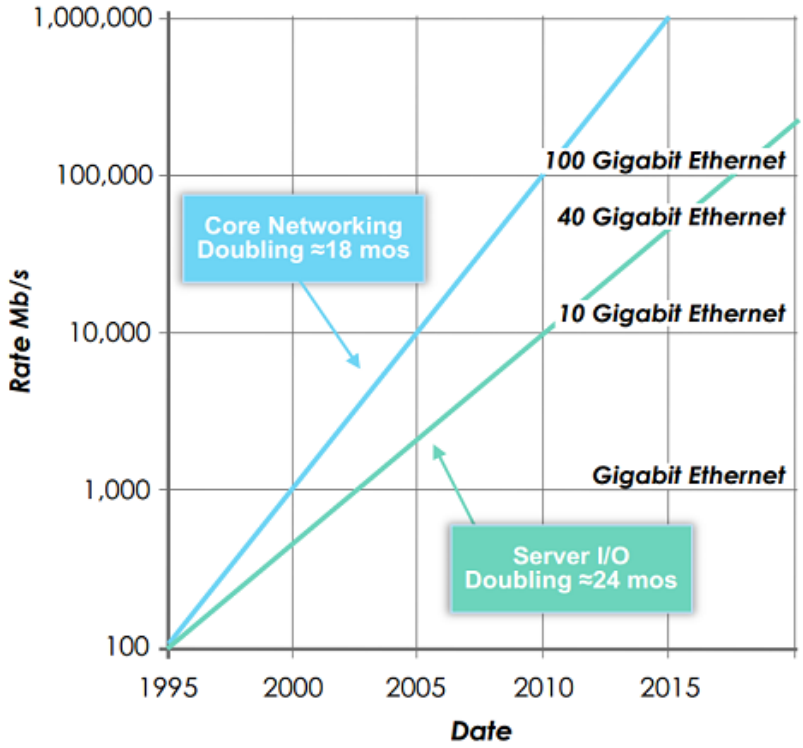
This situation is very akin to the situation that was faced in buying computer hardware 30 years ago. While the trend known as Moore's law continues, at a certain point a degree of certainty surrounded road maps. In the early years of microprocessor development, the changes in performance were so significant that they enabled entirely new capabilities, not just faster operation of existing ones. Modern GUIs depend on huge amounts of processor power and especially memory; by comparison the UIs of 1990 were not just "less", but crude. The situation now is different; faster processors and faster and cheaper memory continue to flow into the market, but they are well anticipated, and the products in the market continue to have life-cycle as they are fully useful for various desired levels of performance.

With this in mind, we refer back to our risk-meter. To remind, the concept is simple--the higher the risk as measured by the aforementioned definitions, the further into the red the needle goes. Here is what we think it should look like right now, in the overall market sense:



Risk meter for Silicon Photonics as a whole. The main driver is the early position of Silicon Photonics in the likely life cycle. The risk comes from adopting a solution early (like Intel) while a competitor takes a different path and gains market adoption (share). With so many possible choices of design, early movers may be at significant risk, offsetting an early mover advantage. Source: EAF analysis

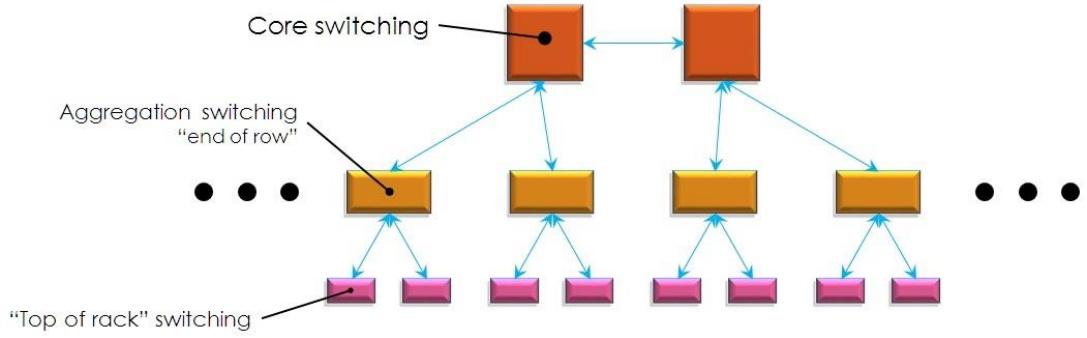
While IPE (Integrated Photonic Electronic) devices can be used to serve many data communication needs, and will likely have application across a range of applications, the near-term driver to develop silicon based IPEs is data center demand. The figure below from the Ethernet Alliance dates from 2012, and shows that even 4 years ago it was evident that core data center demands needed 100 Gb/s throughput and that data rates would continue increasing at exponential pace. This disparity of bandwidth growth between core and server led to the IEEE 802.3 Higher Speed Study Group choosing 100 Gb/s and 40 Gb/s to standardize in order to efficiently meet these needs.



Source: The Ethernet Alliance, "Bandwidth Growth and the Next Speed of Ethernet".

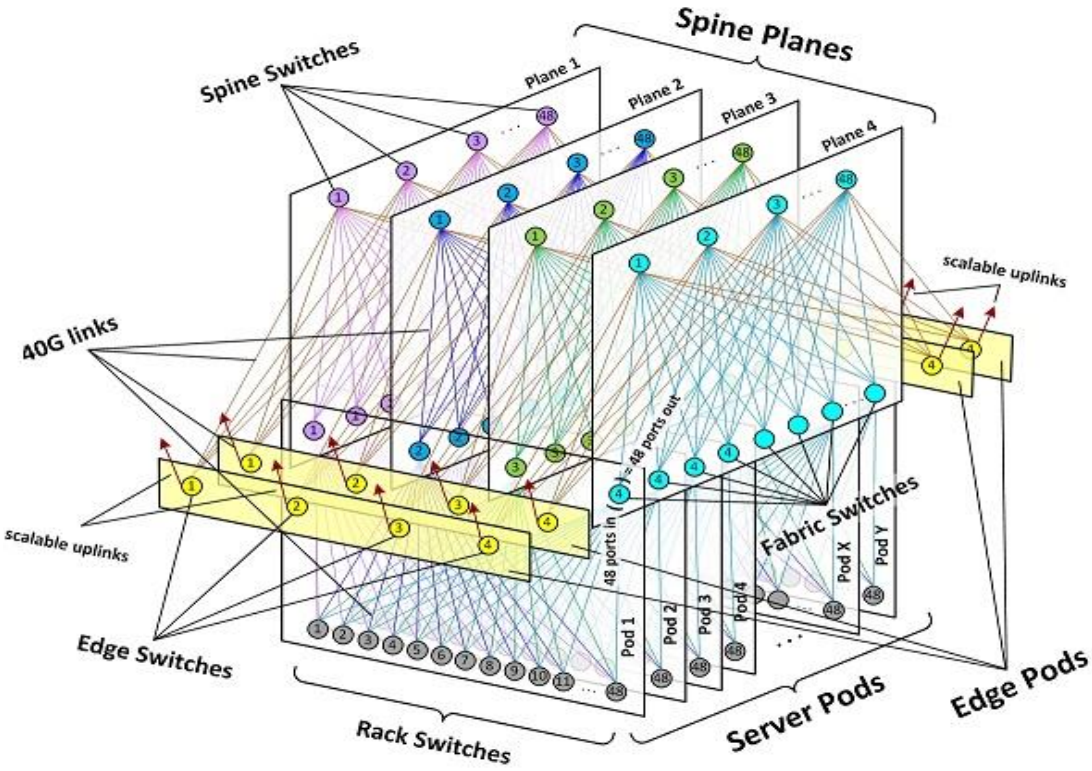
Data center fabric

Data center ports from server blades are now at 10 and 25 Gb/s per channel. If we look at a generalized architecture for data routing in a data center, it is immediately apparent that from the racks to the core network, the data throughput increases dramatically due to consolidation. In fact the situation is even more demanding as workloads move to the cloud as well as data; cloud applications and data create movement along the core in addition to that from the servers and aggregation switches. Silicon Photonics will be used initially at the front of the server rack (the layer below the lowest level shown below), then over time may migrate upward. There are some challenges there in the range and throughput, but likely they will be solved sufficiently for the migration of Silicon Photonics to more and more demanding (throughput) links in the data center.



Adapted from "Photonics and Future Datacenter Networks", presentation by Hewlett Packard and the University of Utah.

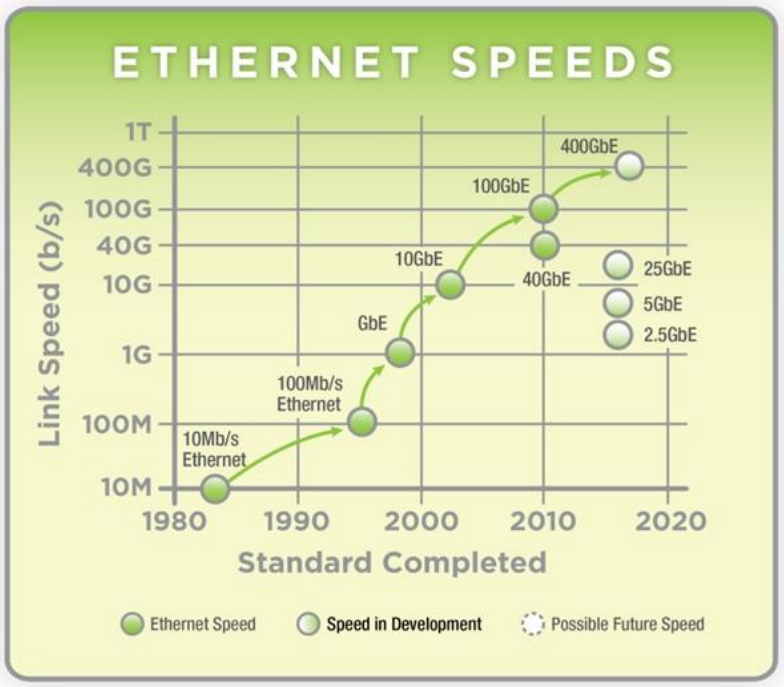
This architecture has been further optimized by Facebook with their Data Center Fabric:



Facebook Data Center Fabric. Source: Facebook.

To fulfill this design, Facebook was working on a 100G top of rack switch by 2015, with an assumption that they could drive down the price of 100G optical ports. Google as well has articulated the need for higher-speed links to flatten and simplify the architecture. In a paper for SIGCOMM 2015, the (Google) authors wrote "In one ToR configuration, we configured each chip with 48x10G to servers and 16x10G to the fabric." With so many 10G lanes, an obvious scaling path is to update to 25G lanes, cost and power permitting. By 2015, the 10G lanes were already migrating to optical vs. copper Ethernet. Similarly, reviewing talks from the 2015 Hot Interconnects conference, Alan Weissberger (viodi.com) reported "InfiniBand is used to interconnect equipment … in large DC networks where extremely low latency is required. We had thought that 100% of DCs used 1G/10G/40G/100G Ethernet…"; the point being that high-speed and low latency had already become requirements for large data centers.

To meet future (near-future most likely) needs within the Ethernet standards family, the IEEE is already working on a 400 Gb/s standard:



Source / credit: The Ethernet Alliance

The question of interest here then is what technologies will be needed and will be available to meet these needs, such as 100 Gb/s channel speeds in a QSFP or smaller form factor? While for many years the lines were somewhat clear between the "Silicon Photonics" camp and the "III-V" camp, those lines are definitely blurred today. In part this is because data center demands are pushing not only the total bandwidth envelope, but the port density envelope. As recently as 2013, 4 10G Ethernet ports per blade was state of the art. Standards for pluggable optical cables have increased this density to the QSFP form factor already in use, but it seems clear that while products in the QSFP form factor will feature increasing bit rates from 4 x 10 Gb/s, which is commonplace, to 4 x 25 Gb/s, which is state of the art commercially available, to 4 x 50 Gb/s and 4 x 100 Gb/s in the next several years. Yet those improvements alone will not satisfy the needs of data centers. Already there is a micro-QSFP on the drawing boards to increase port density, but it seems likely that is only the beginning.

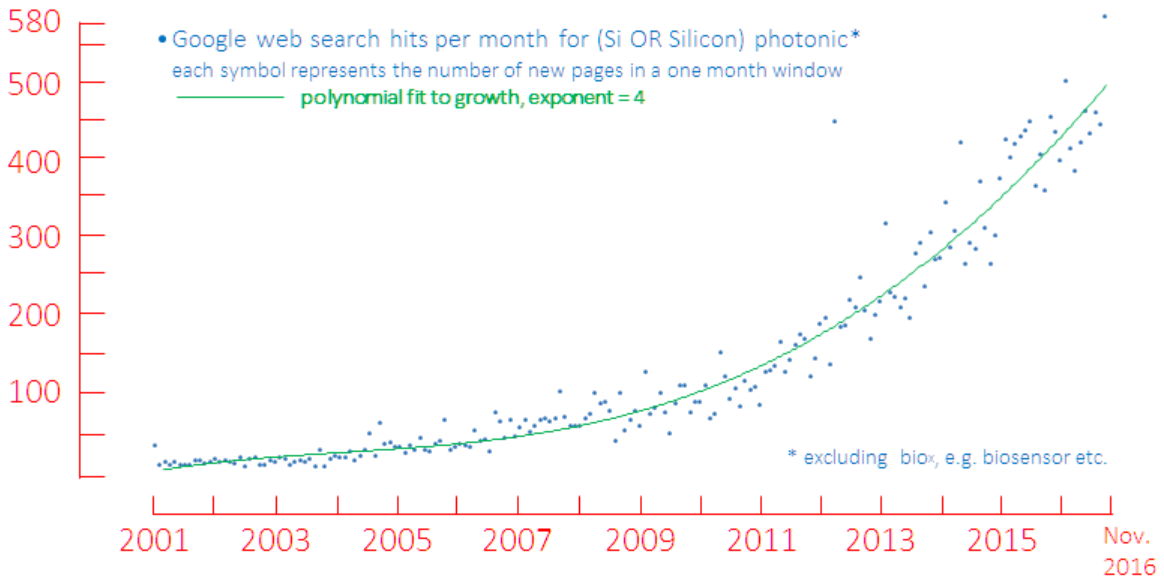
As the port density and data rate per channel increase, this puts pressure on the technology used due to the power density and thermal loads. Thus, just achieving higher channel rates and more channels per cm^2 is not scalable--the heat load rises to unacceptable levels. This is where many in the industry see Silicon Photonics, in some form, as being critical versus just one of many options. The particular needs in future hyper-scale data centers not only create demand but define the life cycle as different from in traditional telecom uses of optical communications. In the program notes for 2016 OIDA / OSA workshop on high-volume packaging for integrated photonics, a senior manager at Facebook notes "Data center requirements differ from those of the traditional Telecommunication equipment central offices in many ways—making it possible to optimize for shorter life-times, relaxed environmental conditions (e.g. temperature, humidity,

and mechanics), and also reduced link budgets." This could well give Silicon Photonics a much-needed jump start.

There is a strong correlation between performance in one part of the entire server network and the other links. This is stated very well by Arlon Martin, Sr. Director, Marketing at Mellanox Technologies, as quoted in a Next Platform interview: "the main thing is to maintain a balance between the servers and the switches. Datacenters have typically run 10 Gb/sec down to the servers and 40 Gb/sec between the switches. Where we are headed is keeping the same symmetric architecture, but having 25 Gb/sec at the server and 100 Gb/sec between the switches, and we will have 200 Gb/sec switches that mesh very nicely with 50 Gb/sec on the servers."

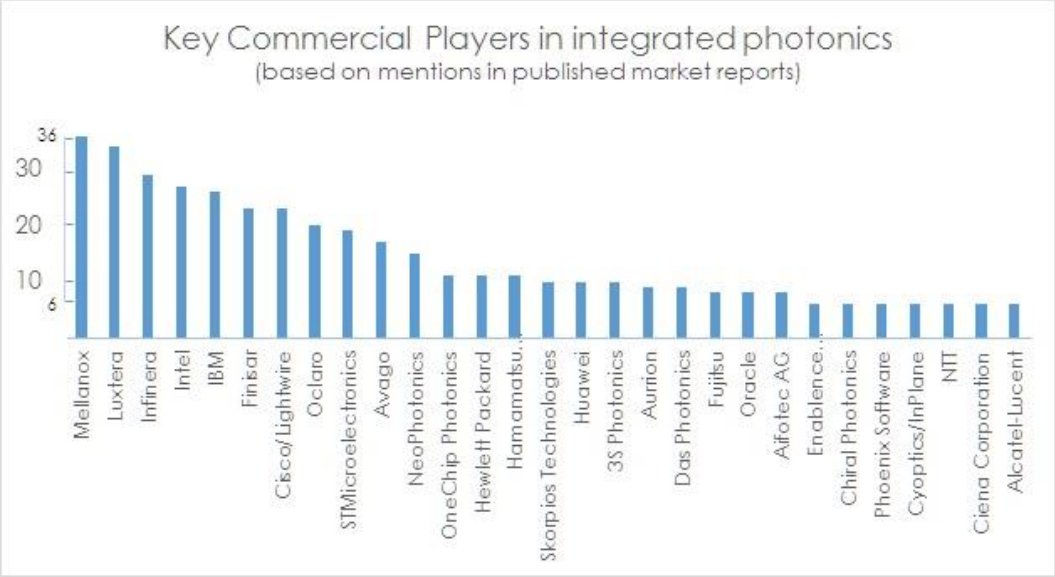
Maturity Metrics

To understand how far things may be from maturity, it is helpful to understand how much work has been done to move Silicon Photonics technology forward. Equally important is to understand that significantly more work has been and continues to be done in Universities or government sponsored research than in the few industry players. As one measure of this, consider publications in the Silicon Photonics field. Using Google search hits for Silicon Photonics as a proxy shows that the number of papers published each year has increased every year since at least 2001. The rate of increase has generally become larger over time, a strong indicator that the pace of work is increasing. This is one indicator that there remain a wide range of aspects of Silicon Photonics that require more R&D and engineering.



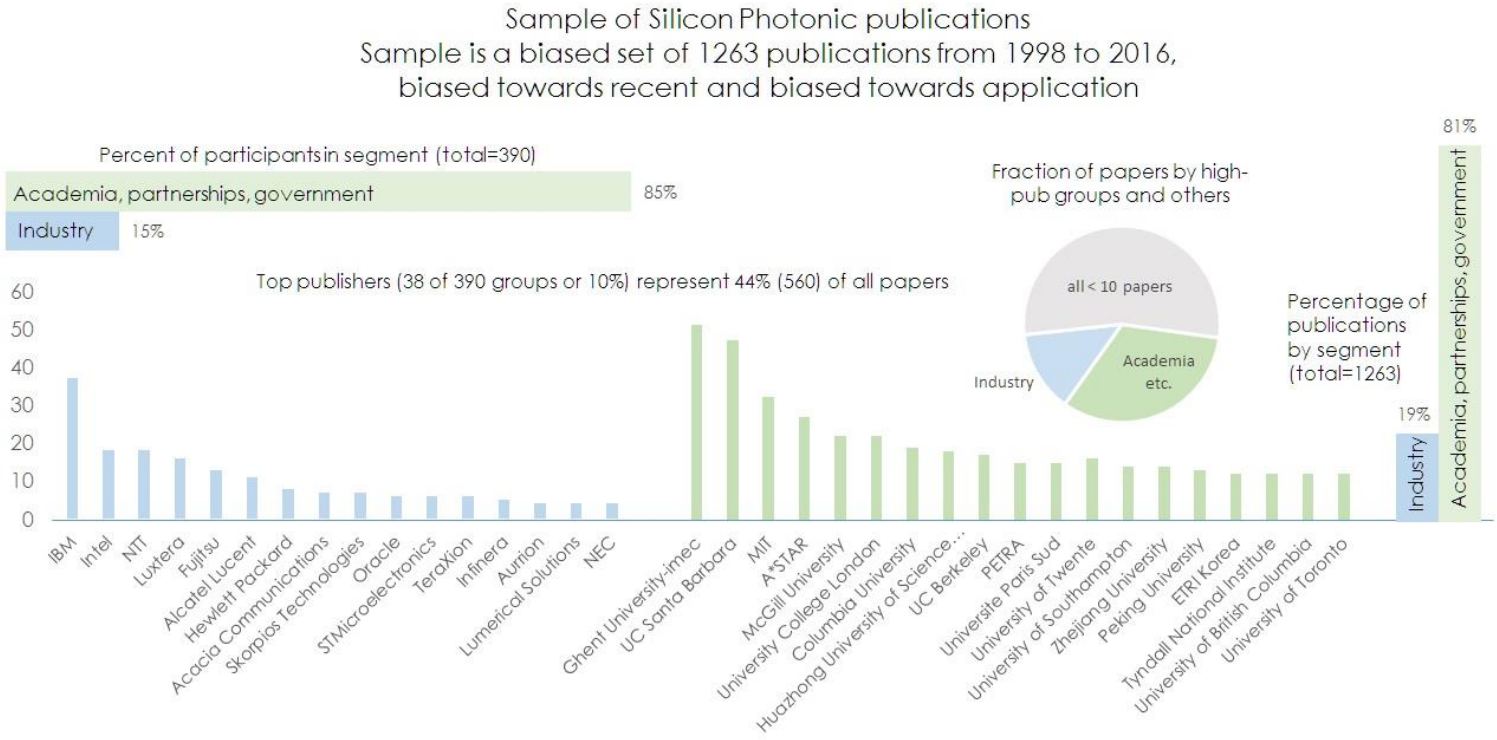
Google search hits for (Si or Silicon) photonic excluding bio related results. The monthly values are the number of hits dated in the given month determined using time-gated search. (These data track publications based on our analysis. Google Scholar results are close except for the most recent two years, where there seems to be some lag in the reported papers in Google Scholar. For that reason we use the web hits as a better proxy. There is considerable work being done using photonic crystals in silicon as the basis for bio-sensors and other non-communication applications, which is why we exclude those hits.) Source: EAF analysis.

Another metric can be extracted from mentions in market research reports. In the following chart, all "market players" mentioned in summaries of available market research through Q3 2016 are summed and charted.



Number of mentions of a particular firm in market research report summaries publicly available through mid-2016. Source: EAF analysis.

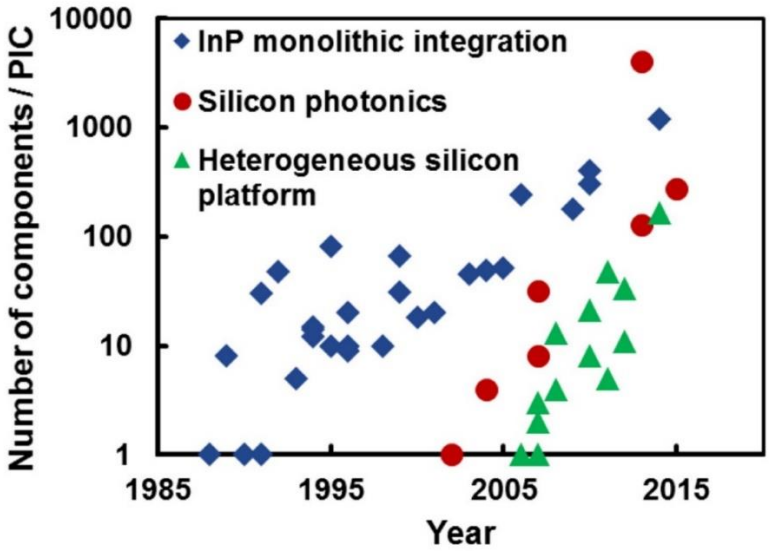
As noted, however, much of the work is being done outside of industry, albeit with industry-university partnering in many cases. Thus, it bears scrutiny to see what are the lead organizations on publications. The chart below shows relative number of publications in which the given organization was the lead. This was generated by review a sample of nearly 1300 important papers and articles (out of about 12,000 total identified). It is evident that in recent years, Universities play a major role. In the dataset as a whole, 81% of publications are University-led; while of the nearly 400 unique groups 85% are University/Government. There is also a long tail (we show only the ~top 15-20 of each group in the chart)--the remaining 375 entries represent 681 publications, with 219 groups with only 1 publication.



Source: EAF analysis.

So we can see that the pace of research continues to increase and that much of the research is in early-stage University work. These indicators argue for concluding Silicon Photonics is relatively far from industrial maturity. As will be seen below, in many building blocks there continue to be new alternatives demonstrated in research labs. This means that the situation is relatively far from a dominant solution or solutions. All of these indicators mean there are risks to system designers to spec in and develop around early chipsets. It will be beneficial to explore the roadmap with suppliers and ensure the thinking is aligned.

Researchers at UC Santa Barbara first pointed out in 2013 that Silicon Photonic integration is increasing much faster than InP PIC integration. The updated figure here indicates that it is still the case; this is one indirect indicator that Silicon Photonics may well be a key platform of the future:



Source: Heterogeneous Silicon/III-V Semiconductor Optical Amplifiers, 2016, M. Davenport et. al. and Heterogeneous III-V / Si Photonic Integration, 2016, John E. Bowers.

Silicon Photonics does not mean just one thing. Silicon Photonics most generally means implementation of some level of photonic integrated circuit in silicon (see below for a more structured definition). As most commonly used, it means leveraging silicon semiconductor foundries--so called CMOS compatible processes--to get high yield, low cost, and access to a vast knowledge and experience and installed capital base in manufacturing semiconductors. As used in reference to commercial devices, Silicon Photonics is a finished product that includes use of silicon PICs and whatever else is needed to complete the desired product (a 25 Gb/s transmitter, for instance). Owing to the need of a light source most systems include not only photonics in silicon but also a gain material, typically III-V material, somehow integrated into the device, or a discrete semiconductor laser integrated.

Not just Silicon

Compared to this (rough) definition, there are a myriad of other potential approaches, both competitive and complementary to Silicon Photonics, pursued by research groups. Some use other crystal substrates, some seek to use group IV materials for light sources, and some pursue even more novel approaches to the light source or other aspects. Examples of other materials and light sources include:

- Hydex Glass and amorphous silicon (INRS-EMT, RMIT University, Infinera University of Sydney, ColorChip, Hamburg University of Technology, and others),
- Germanium on Silicon (MIT, Dartmouth College, US AFRL, Politecnico di Bari, and others),
- Silicon-Germanium on Silicon with process tunable SiGe composition for detectors and modulators in CMOS (University of Southampton),
- Lithium Niobate-silicon hybrid (UC San Diego, Sandia National Labs, University of Central Florida, Stanford University, University of Delaware, and others),
- Gallium Nitride on Silicon (HRL Laboratories, University of Michigan, National Cheng Kung University, Yale University (GaN on Si(100)), University of Electronic Science and Technology of China, Ecole Polytechnique Federale de Lausanne, National Chiao Tung University, Northwestern University, IBM, and others),

- Dilute Nitride (InxGa1 − xAs1 − yNy) vertical semiconductor optical amplifier requiring very low injection current (University of Essex),
- Lead Zirconate Titanate on silicon (ferroelectric capacitors, Instituto de Ciencia de Materiales de Madrid),
- Atomic Layer Deposition of tantalum pentoxide and polyimide onto silicon slot waveguide to tune the performance of a modulator (Aalto University),
- Perovskite nanowire lasers (University of Wisconsin-Madison, Columbia University),
- Silicon Nitride (Sun Yat-sen University, Ghent University (microdisks), Purdue (resonators), University of Illinois, Johns Hopkins University, A*STAR, University of Sydney, Singapore University of Technology and Design, and others),
- Erbium-doped waveguide DBR and DFB lasers in ultra-low-loss silicon nitride platform (UC Santa Barbara),
- Erbium-doped aluminum oxide layer on SiN waveguide in CMOS resulting in 75 mW CMOS compatible laser (MIT),
- Rare-earth-doped ridge channel Al2O3 waveguide lasers with a peak gain of 2 dB/cm at 1533 nm and a gain bandwidth of 80 nm (KTH-Royal Institute of Technology),
- Erbium-doped spiral amplifiers with 20 dB of net gain on silicon (University of Twente),
- Rare-earth silicates (ErxY2 − xSiO5 and ErxYbyY2 −x− ySiO5) as gain medium in a Silicon Photonic system (University of Electro-Communications),
- Graphene (University of Tokyo, Zhejiang University, Vienna University, Columbia University, Fudan University, MIT, Institute of Physics (Beijing), Cornell University, Advanced Microelectronic Center Aachen, Institute of Photonic Sciences Barcelona, and others),
- Nanotubes (Northeastern University, Karlsruhe Institute of Technology, McMaster University, University of Illinois Urbana, McGill University, Université Paris Sud, Jamia Millia Islamia, George Washington University),
- MoS2 (Ecole Polytechnique Federale de Lausanne, Soochow University, University of Shenzhen, The Australian National University, and others), and
- Compact GaSb/silicon-on-insulator 2.0x µm widely tunable external cavity lasers (Ghent University-imec).

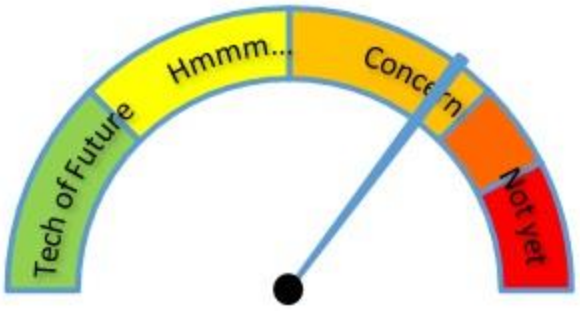
Note that the last work is in the 2 µm range whereas the majority of efforts for data center optical interconnect is in other bands such as 1.3 µm, but we include it as yet another example of Silicon Photonic applications using alternate materials and designs. Many of the above are in conjunction with Silicon substrates and reflect branches of the tree that may ultimately bear fruit for Silicon Photonics, and many are alternative platforms. It should be clear that a final solution is yet to be demonstrated. Thus, in addition to a number of open issues or lack of clear set of "winning" solutions in Silicon Photonics, there remains the question as to whether this is the platform of the future. As we dig deeper into the status of things, keep in mind that the main driving force behind Silicon Photonics is the goal to use existing, low cost fabrication facilities, with low-cost (relative) raw materials. In addition, using silicon as the passive optical platform brings advantages of high miniaturization with relatively low losses. Because fabrication processes (for existing microelectronics) are very advanced, components in silicon can be made with extremely high precision, needed as features get smaller. Miniaturization is important because it results in high wafer utilization.

Fab node paradox

On the point of low cost, there is a so-called "paradox" described in Optics & Photonics News: low cost requires large, high-volume fabs, but the market for integrated photonics (IPE devices) may be too small to warrant the huge investment in a high-volume fab for process development. An example is given of requiring a $2B market to provide sufficient ROI, and as noted earlier the total Silicon Photonics market may not reach that level for years. This creates two important situations: fabless design companies targeting Silicon Photonics are likely to be challenged on cost, and vertically integrated suppliers with existing, possibly idle fabs may have a large early advantage. Thus Intel may effectively be far ahead commercially at this stage of the market. In the words of Intel's General Manager of the Connectivity Group (quoted by Semiconductor Engineering) "We invested in a methodology to bond light-emitting III-V indium phosphide to silicon so that the lasers are defined in silicon. This is the Holy Grail of silicon photonics." In other words, Intel has made significant changes to a standard CMOS flow to achieve their initial products. This has in fact been evident since early progress had been made on Silicon Photonic integration. As an example, in a 2013 review for Leti innovation days, STMicroelectronics showed several cases of "More than CMOS processes" they had integrated into the Silicon Photonics process flow. The list included silicon patterning, patterned Ge epitaxy, Ge implantation, PIPIN modulator slot implantation, curved structures, exclusion window for optical fiber, and other steps. An important point from this is that, although much installed investment in CMOS foundries can be leveraged, enough unique processing is required that few foundries will likely have Silicon Photonics capabilities for some time. Another key point to consider is that exiting Silicon Photonics has been run on sub-100 nm nodes (i.e. 45 nm, 60 nm) using smaller wafers than state-of-the-art electronics. This may imply that integrated control electronics would have to be made on older nodes as well, impacting cost and size. If, as discussed elsewhere, the end game for companies like Intel is chip to chip photonic interconnect, then they may envision an as-yet-to-be-revealed solution to integration with advanced process nodes.

To begin understanding where things stand, then, we frame up the basic building blocks needed for a completely integrated Silicon Photonic (IPE) device. This has been reported variously to be five to ten major areas. Intel has suggested "Six things are required for optical systems: light source, guide channel, modulation, photo detection, low-cost assembly, and intelligence" (note: intelligence = electronic control). In fact, for a practical realization of a Silicon Photonics device, at least two more things are required: chip to fiber interface and test process. The latter arises from the fact that although the goal may be to achieve these devices in "standard CMOS", it is inescapable that some additional process steps, materials, and structures will be introduced, which then require a new test process. In addition, optical/photonic testing is new compared to electrical IC testing processes.

Manufacturing (fab process)



Risk meter for Silicon Photonics fabs. The level of risk reflects the high investment in process changes and learning curve to use an existing or new fab to produce integrated Silicon Photonics devices. If a competitor implements a different solution using different processes, and gains a cost or performance or other advantage, then existing investments may be lost to change over to a new solution. Source: EAF analysis.

At a high level, there are only a handful of foundries globally capable to run Silicon Photonics, and several of those are in-house for large OEMs like Intel or IBM. Since one of the objectives with Silicon Photonics is to bring costs down, it needs to run in large fabs, ideally. However, as reported by IC Insights, 98% of global 300 mm wafer processing capacity is held by the top 15 suppliers, and the trend is for more consolidation. Looking across 300 mm, 200 mm, and <150 mm wafer sizes, IC Insights data show that, except for Intel, GlobalFoundries and STMicroelectronics, it is likely that Silicon Photonics will be relegated to smaller wafer sizes. This situation may present a barrier or increase costs for new fabless Silicon Photonics startups or in-house development at fabless OEMs.

The other main goal for Silicon Photonics is embodied in the often-used descriptive term "CMOS compatible", which is a moving target in the sense of allowable materials. If we just consider the materials proposed in various implementations, as demonstrated by research groups, we can contrast that to the semiconductor industry roadmap in the ITRS (International Technology Roadmap for Semiconductors) roadmap. The 2013 Edition of the ITRS, contains a chapter on "Emerging Research Materials" (ERM) and in that chapter there is a table "ERM15 ITWG Earliest Potential ERM Insertion Opportunity Matrix", or when various materials might be introduced into production foundries.

Table ERM15 ITWG Earliest Potential ERM Insertion Opportunity Matrix

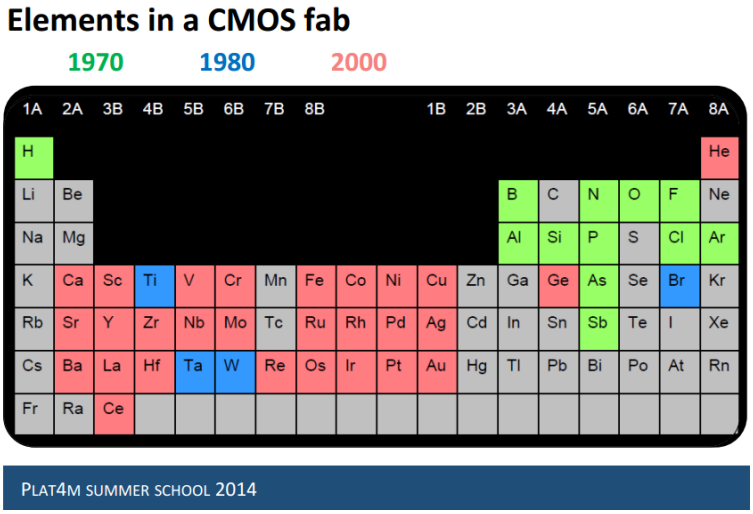
Application	Ge & III-V	Carbon Nanotubes and other Metal Nanotubes	Nanowires	Graphene	Oxide Nanoparticles	Metal Nanoparticles	Novel Macromolecules	Self Assembled Materials	Complex Metal Oxides	Spin Materials (Fe, Co, Mn, Ni, etc.)
Process Materials										
Lithography										
Device: Memory										MRAM
Device: Logic										
Interconnect										
Packaging							*			

LEGEND
Earliest Potential Insertion | Current Apps | 3-5 yrs | 6-10 yrs | 10-15 yrs | 16+ yrs | Not on the Roadmap

source: ITRS 2013 ERM

Inspection of this table indicates that Ge and III-V materials could appear in 5-10 years, or around 2019 at the earliest, nanotubes are another 5 years out at best (as part of the main device flow), as well as Nanowires and Graphene based materials. In his article on the Semiconductor Manufacturing & Design Community, Sr. Editor Ed Korczynski pointed out that there are relatively few players in the Logic IC foundry world today, and they may not disclose their plans to integrate new material flows. Thus, the above, in Mr. Korczynski's words, might be considered a "scouting report" of things the industry would like to bring into their processes. It is good to keep this in mind as you review some of the impressive demonstrations covered below. We also note that the 2015 Edition of the ITRS represents a transition year as the entire roadmap process was restructured and reorganized into seven international working groups, and renamed ITRS 2.0. In the 2015 ERM report, addressing III-V materials, carbon nanotubes, graphene, and other advanced materials and approaches is reflected in both the near-term (2015-2022) and longer term (2023-2030) "difficult challenges".

For one other perspective, it is of interest to review the historical introduction of materials into "CMOS" foundries that has occurred in the past. The following figure was presented in 2014 specifically with regard to the question of what can be used in a CMOS foundry:



Elements that have been used in CMOS foundries by decade. From "Light sources in silicon photonics", presented by Gunther Roelkens, Ghent University-imec, at the PLAT4M 2014 summer school.

This view is more sanguine with regard to the potential introduction of materials, and the current situation isn't completely dire, albeit that the number of fabless routes to Silicon Photonics is much more limited than that for various EICs. There have been advances in foundry capability in the last 10+ years to support Silicon Photonics. In support of development, the OpSIS program (now closed) was supported by Intel at the University of Washington to provide research groups access to foundry services. The ePIXfab program in Europe has over 50 members cooperating with the goal to develop "the design and fabrication of SOI and SiN-based photonic devices using standard lithographic techniques compatible with CMOS-processing." ePIXfab members include Universiteit Gent, CEA-Leti, imec, TNO (Netherlands), Tyndall National Institute, and VTT. As an extension of ePIXfab, imec offers ISIPP25G, which is a "state-of-the-art performance, design flexibility and superior CD and thickness control. It is a fixed process technology (130nm) with a

validated device library. The offered integrated components include low-loss waveguides, efficient grating couplers, high-speed silicon electro-optic modulators and high-speed germanium waveguide photo-detectors." Also supporting European participants, Europractice offers a Silicon Photonics multi-project wafer (MPW) service enabling development of commercial Silicon Photonics products.

European leadership

The to-date effort and advanced status of the European programs to commercialize photonics in general, and Silicon Photonics in particular, should not be underestimated. From 2008 to 2012, the EU funded HELIOS (pHotonics ELectronics Integration on cmOS program resulted in a number of building blocks for Silicon Photonics. STMicroelectronics has worked closely with various EU efforts and has essentially a complete flow available to fabless IPE designers. One of the first companies to take advantage of STMicroelectronics capabilities was Luxtera, who announced an agreement in 2012 between them and STMicroelectronics to produce Luxtera's designs. Additional programs are underway to further develop upon the STMicroelectronics base process, which may yield even greater cost reductions and performance increases. In addition, imec announced a partnership with the University of Central Florida in July 2016, "to establish fabrication facilities for the development and production of III-V-on-silicon devices for a range of applications including terahertz and lidar sensors, high-speed electronics and photonic devices."

A number of coordination efforts have also been carried out in Europe, which is critical to leverage a broad range of capabilities. SECPHO (Southern European Cluster in PHotonics and Optics) is a business-oriented cluster that began from 2009, funded mainly by the Spanish Ministry of Industry. ASPICE (Action to Support Photonic Innovation Clusters in Europe) was funded from 2011-2013 as the need to coordinate clusters was recognized. PhotonFAB was started in 2008 as a support action to facilitate access to advanced CMOS-oriented centres of expertise and foundries for development of Silicon Photonic integrated circuits. ePIXfab markets services and organizes multi-project wafer runs, which lowers the barrier to bring designs to market. Following on from HELIOS, the PLAT4M (Photonic Libraries And Technologies 4 (for) Manufacturing) is focused on bringing the complete Silicon Photonics research platform to a state that transition to industry is possible. The ACTPHAST (Access CenTer for PHotonics innovAtion Solutions and Technology) is funded by the EC to support European companies with photonics innovation, acting as an accelerator. The PIX4LIFE program began in 2016 to establish a validated CMOS compatible Silicon Nitride (SiN) technology platform for densely integrated PICs.

Rest of the World

Beyond Europe, recently, (September 2015) Singapore's A*STAR and Lumerical Solutions announced a Calibrated Compact Model Library for their Silicon Photonics Platform, and a Process Design Kit. A*STAR in July (2016) launched the "Silicon Photonics Packaging consortium (Phase II)" to "develop a broad spectrum of silicon photonics packaging methodology." In September (2016) VTT Technical Research Center (Finland) announced with PhoeniX Software a development kit and MPW service for Silicon Photonics: "Supported by the EU-funded ACTPHAST project, VTT Technical Research Centre of Finland Ltd. and PhoeniX Software have developed an extensive and improved process design kit (PDK) that supports the development of silicon photonics". In October (2016) Cadence Design, Lumerical, and PhoeniX Software hosted a 2-day Summit on Integrated Photonics and showed a complete design flow supporting Silicon

Photonics. At the Summit GLOBALFOUNDRIES presented a keynote address and established that they will support integrated photonics.

In May (2016) Amkor and Cadence announced a Package Assembly Design Kit (PADK) for Amkor's SLIM and SWIFT Packaging Technologies. Also in July (2016) the University of British Columbia, with Lumerical and Cadence Design Systems followed up their May 2016 paper and published "A Novel and Scalable Design Methodology for the Simulation of Photonic Integrated Circuits". UBC has been an important player in the development of Silicon Photonics, including hosting "Summer Schools" to educate interested players in industry and academia. Regarding their design approach, they say it is "a novel design methodology for silicon photonic integrated circuits (PIC) that integrates Cadence's Spectre with Lumerical's INTERCONNECT. It supports parametric analysis of bidirectional, multi-mode PICs, with electrical feedback." Also supporting North America, the Center for Integrated Access Networks is a cooperation between "the University of Arizona (Lead) and its partner institutions, the University of California at San Diego, the University of Southern California, the California Institute of Technology, the University of California at Berkeley, Columbia University, the University of California at Los Angeles, Norfolk State University and Tuskegee University." As part of the program, the US National Science Foundation awarded $18.5M to establish an Engineering Research Center at The University of Arizona. The CIAN website notes "the CIAN vision would lead to the creation of the PC equivalent of the optical access network by employing optoelectronic integration to enable affordable and flexible access to any type of service, including delivery of data rates approaching 10 Gb/sec to a broad population base anywhere and at any time." An important part of the work is supporting Silicon Photonics Manufacturing.

Commercially, a number of companies offer services supporting Silicon Photonics assembly, packaging, and design services. An example of the former is PLC Connections, who states their "goal is to offer a quick turnaround and cost effective packaging service to silicon designers for validation of design, process, and function. PLCC offers fiber arrays, fiber probes, and other custom solutions for launching from telecom fiber into silicon waveguides via grating coupler or edge couplers." INO in Canada "offers silicon photonics packaging and wafer post-processing services. We have the ability to deliver silicon photonics devices showing very low insertion losses and submicronic optical alignment repeatability." Another North American offering is Analog Photonics, who offer both design and foundry support, stating "We offer the best silicon photonics fabrication capability in the U.S to the public." EPIC (European Photonics Industry Consortium) maintains a PIC Value Chain document that lists a number of other companies supporting assembly and packaging including Samtec, Bay Photonics, XiO Photonics, AIFOTEC, optocap, and Technobis ipps.

Along with the progress in design tools, fab support, and packaging, various groups have reported successful manufacture of Silicon Photonics in existing commercial-grade CMOS foundries. Examples include:

- Monolithic Silicon Photonics in a sub-100 nm SOI CMOS Microprocessor Foundry (University of Colorado, MIT, UC Berkeley),
- Open foundry platform (45 nm) for high-performance electronic-photonic integration (MIT, University of Colorado),

- Silicon Photonic transceivers with microring resonator bias-based wavelength stabilization in a 65 nm generic CMOS process (Texas A&M University),
- Monolithic (55 nm and 90 nm CMOS) Silicon Photonics at 25 Gb/s and 56 Gb/s (IBM),
- Silicon photonic receiver and transmitter at 36 Gb/s for 1550 nm using 65 nm bulk CMOS process (ETRI Korea),
- Waveguides and GHz responsivity photodetectors in 180 nm CMOS without post processing (Rice University),
- InGaAs nanopillar lasers grown on silicon-based MOSFETs (and characterized for functionality after processing) (UC Berkeley),
- 25 Gb/s Silicon Photonics Platform Development in a 0.18 um CMOS Manufacturing Foundry Line (A*STAR/GlobalFoundries)
- Electrically programmable microring resonator-based wavelength filter in package integrating Silicon Photonics with non-volatile memory built in a CMOS line (A*STAR),
- Silicon Photonic IC with flip-chipped CMOS driver IC for FDMA-PON (CEA-Leti), and
- Monolithically integrated 56 Gb/s transceiver with integrated CMOS drivers for PAM-4 modulation built in sub-100 nm CMOS,

to mention only a few.

The first work is important in that all the processes were carried out in a "standard" 45-nm CMOS foundry, without introduction of additional materials or steps. The focus was to demonstrate a direct photonic processor to memory photonic interface, and as such is somewhat differently focused than most of the technology in this report. We feel that the risks for full integration targets are still high and decision-makers should be aware of this. Nonetheless, it is of great value to see that the development community still pursues long-term goals which will be natural progressions in later generations. IBM's work has demonstrated foundry integration as an ongoing focus, and the noted work is at the reference design level of maturity. In the work cited, published in March 2016, IBM showed a 4x25 Gb/s reference design monolithic transceiver. Leveraging both the MIT and Stanford knowledge bases, APIC Corporation has developed a doped Ge laser approach that can integrate into standard SOI processes. PhotonIC Corporation plans to take the approach and use it with their existing knowledge base of photonic interconnect manufacturing to deliver fully integrated products.

The Promise of Fully Integrated Solutions

As more and more component designs are proven (e.g. microring resonators, Mach Zehnder Interferometers, grating couplers, phase rotators, mode converters, etc.) some groups have already begun looking to the future of fully integrated solutions. In a recent review by The Hong Kong University of Science and Technology, the authors suggest there are several "grand challenges" remaining, including energy consumption, thermal management, integration of new materials into CMOS flow, and some others. Nonetheless, in some regards basic Silicon Photonics integration has matured to a pre commercial state (our opinion). The challenges around thermal and energy consumption are noteworthy; although it is expected that Silicon Photonics will allow faster, more highly integrated, and efficient communications, researchers at Peking University recently published a review of the thermal and energy consumption remaining challenges.

Other notable work demonstrating complete integrations includes:

- Demonstration of Silicon Photonics in a 300mm platform (ST Microelectronics),
- Demonstration of a 4x20 Gb/s WDM transceiver (imec-Ghent),
- 25 Gb/s error-free operation of a chip-scale optical transmitter at 70C (PETRA Japan),
- 50 Gb/s Silicon Photonics platform for short reach optical interconnects (imec),
- Silicon Photonics optical transceiver with low-power integration to LSI (Fujitsu),
- 25-Gb/s 5 x 5 mm^2 Chip-Scale Silicon-Photonic Receiver Integrated with 28-nm CMOS Transimpedance Amplifier (NEDO [Japan]),
- A 3×60 Gb/s Transmitter/Repeater Front-End in a 28nm UTBB FD-SOI Technology (University of Toronto), and
- Glass interposer with laser scribed waveguides to interconnect (optically) Silicon Photonics chips (McGill University).

The last two works are interesting due to the use of, in one case, an interposer to closely couple the LSI to the photonics reducing losses, as an option to full integration of the electronics and photonics, and in the other case, an easily manufactured photonic interposer, which could be used in future designs where, for example, Silicon Photonics was integrated into a processor, and connected photonically to memory.

In some cases "Silicon Photonics" is used to mean full integration of all control electronics and photonics in one chip. This is likely to occur, if at all, in a second or later generation of the technology. In other words, using CMOS-like foundry processes to make Silicon Photonic PICs, even with heterogeneous integration of the light source, provides sufficient size and cost reduction as to be attractive and commercially viable without the additional integration. In addition, as we will lay out below, there are many options for the various building blocks of the IPE and we think more time will be needed to find sufficiently optimal solutions that pushing for full integration now carries a high degree of commercial risk. Nonetheless, programs to increase integration are underway, including the DIMENSION program funded by the EU Horizon 2020 program, with the stated goal to integrate electronics and photonics in a single chip in the next few years. Also, startup company Sicoya says they will launch a commercial product in 2017 integrating the electronics and photonics using optical connections. Another Horizon 2020 program called COSMICC is working on better structures for chip to fiber interfacing, and will work on electronic integration as part of aggressive cost reduction targets.

One other important aspect of Silicon Photonics integration into existing or adapted CMOS foundries has to do with the silicon wafer. Most examples in this report are based on so-called Silicon on Insulator, which is a silicon layer on top of a so-called buried oxide (BOX) layer. As noted in a 2014 review led by authors from the National Research Council of Canada, "standard" SOI is generally 220 nm of silicon on a thick (1 um) buried oxide (silica) layer, yet optimal Silicon Photonics performance may benefit from different silicon thickness. In many cases in the literature, different BOX thicknesses may be used, which could present barriers to entry into existing foundries. Thus, there may be some issues to address before a widely available fabless design model is in place.

For the purposes here, we consider as necessary elements, in addition to manufacturing, to be: (1) light source (laser), (2) modulation, (3) waveguides, (4) photo-transduction, (5) chip to fiber coupling, (6) packaging scheme (meaning the physical integration approach of all components needed for a given chip or "package"), (7) control, and (8) test. Note that we have left out the connector/socket category here, as it is not inherently related to the Silicon Photonics process development.

Item (1) has only recently been achieved in a workable hybrid process--that means the lasers or the gain medium used in existing and near-term products are made separately (i.e. a separate process of different wafers processed to provide the laser/gain material, which is joined with the Silicon Photonics wafer in various ways) from the rest of the photonic circuit, then assembled in some way. Building blocks (2) and (3) are in a good status, although there are many options and more configurations and optimization will occur over time. In addition, (5) needs to be demonstrated in a full production scale environment, (6) has a number of options but again the "best" approach is yet to be settled, and is in some ways intimately tied to the light source/gain medium integration approach, and (8) may pose challenges to achieve in high volume. The last remark means that although the "goal" is to develop a technology that runs in "standard CMOS", there are changes introduced compared to existing foundry process flows for any near-term implementations, and there is not yet sufficient experience in most cases to say definitively that these changed flows will be manufacturable to normal semiconductor manufacturing standards (i.e. better than six sigma). Our distinction between packaging and assembly is mainly about the process flow, but is intended to capture any additional steps needed such as assembly of a final hermetic package, as one example. Finally, regarding control (7), as noted there will be evolution of the degree of integration. However, the concepts and design approaches for control electronics are already fairly well known.

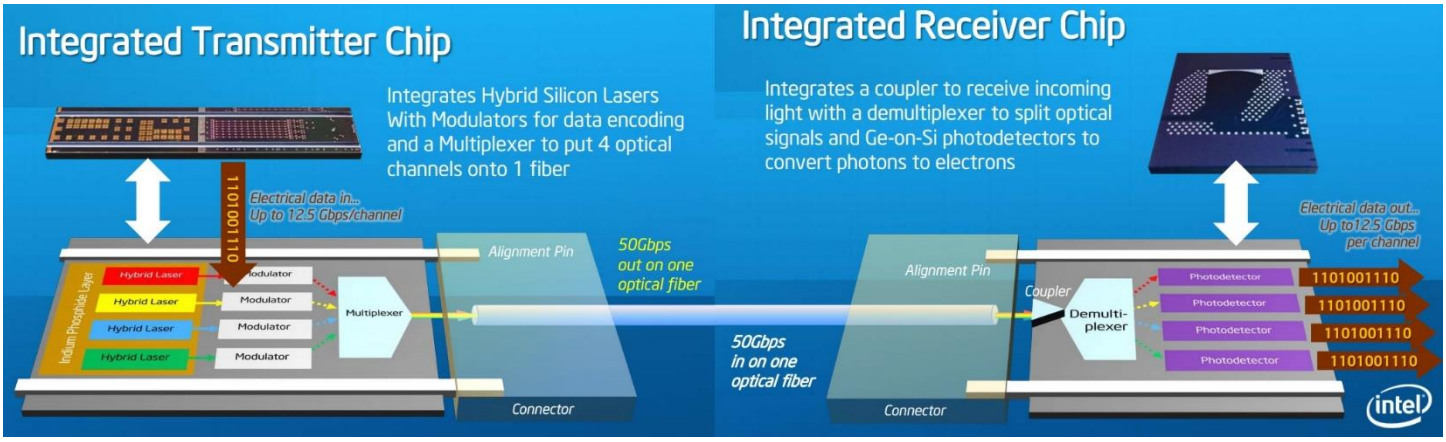
R&D perspective

Before breaking down the remaining building blocks, the perspective of the research and development community helps set the stage. Over the last several years a number of review papers have been published by different research groups. As an example, last summer (2016) the Hong Kong University of Science and Technology (HKUST) published the review mentioned earlier that included some targets the authors believe are necessary for definitive solutions. An important one is the power consumption--HKUST suggested that around 400 fJ bit needs to be met, and in their review only one example came close, a particular implementation of a light source by NTT Photonics Laboratories called a distributed feedback laser (DFB) created in a packaging scheme called Membrane Buried Heterostructure and using direct modulation. The HKUST team points out that in addition most light source solutions to date have issues at elevated temperatures (70 degrees C) including performance degradation and wavelength shift, among others. A practical system to meet cost targets needs to operate at such temperatures to avoid expensive cooling additions. At present Quantum Dot lasers appear to be the best solution to the temperature issue for monolithically integrated solutions. Finally, HKUST comments that improvements in photonic switch fabric port count are needed (for using Silicon Photonics in the rack and network switches in data centers), more maturity of new material and process integration to CMOS, and more realistic integration of Silicon Photonics to electronics (i.e. integration of the photonic functionality to the control and logic functionality) are all needed.

imec in Europe is probably one of the most open organizations that is also in direct contact with many key developments in Silicon Photonics, in part due to the close relationship with the Photonics Research Group at Ghent University. In an interview by tech website gazettabyte of Joris Van Campenhout, Program Director for Optical I/O at imec, gazettabyte noted that one focus for imec regarding Silicon Photonics is to "reduce the overall insertion loss of Silicon Photonics circuits for short-reach interconnect applications. Such short-reach links span distances of up to a few meters, a market segment currently addressed using advanced copper cabling or VCSEL based optical interconnects. Because of the relatively high insertion loss of silicon photonics designs, it is not possible to achieve a sufficiently low-power consumption for such links." Dr. Van Campenhout said "That is a *show-stopper* because it prevents us closing link budgets." (*emphasis* added) This is in contrast to the thinking that simply miniaturizing and integrating the systems into Silicon Photonics would result in lower power use.

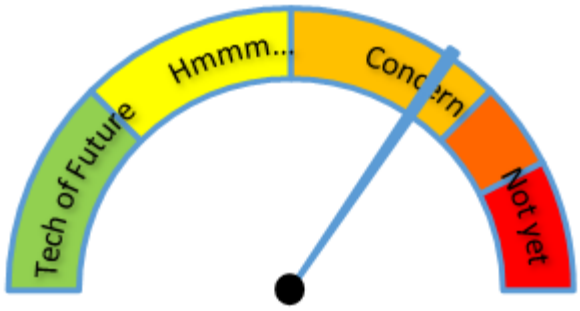
Progress in reducing power consumption is occurring, however; an example are "optical cores" demonstrated by PETRA (Japan) which consumed 5 mW/Gb/s, or about 0.5 W for 100 Gb/s, which is well below the current specification of 100 Gb/s (4 x 25) QSFP pluggable modules (3 Watts). As another example, NTT Nanophotonics Center has developed a photonic-crystal detector as an alternative to the nearly ubiquitous Ge avalanche photodiodes. The NTT researchers note that "The power consumption of a conventional photoreceiver is dominated by that of the electric amplifier connected to the photodetector (PD)", and show that their nanodetector allows operation without an amplifier. Recently (June 2016) Université Laval demonstrated microring modulators operating at 45 Gb/s at only 1 fJ/bit, and 80 Gb/s PAM-4 modulation at only 7 fJ/bit.

Now let's look at the remaining blocks. Here are two images from Intel that describe the 5 physical components. We begin by looking at the light source.



Source: Intel.

Light Source



Risk meter for light source. The high level of risk is a direct result of, in our assessment, a high likelihood of better solutions coming from R&D which lower power consumption, allow increased data rates, lower costs, or other factor of advantage over earlier solutions. Source: EAF analysis.

We feel the light source is the most critical element of the platform because so far, there are only a few fully integrated (so-called "monolithic integration") solutions and none of those are close to commercialization. Also, the issue of integrating a laser to a silicon substrate has been known and solutions sought for a long time. An early patent was granted in 1990 entitled "Method of making monolithic integrated III-V type laser devices and silicon devices on silicon", granted to Paul M. Zavrakcy and assigned to Kopin Corporation. Given that 25 years have passed and the "final" solution is not settled, this is an area of concern. To emphasize this point, we quote Richard Soref from a gazettabyte.com interview in 2015: "Considerable investment is required to make monolithic real. Once actual, it should be more cost-effective than hybrid." Likewise, PIC magazine said in September 2016 "As of now there is no a clear winner for the choice of cw light source with hybrid vs. monolithically integrated lasers in contention. On-going research aims at finding the sweet spot for laser efficiency, power consumption, and reliability."

The basic technological problem is that Silicon, while having benefits for many photonic integrated circuit components, is not a material for which it is simple to fashion a laser. The slightly more complicated reason is that Silicon does not have a direct band gap electronic structure, which makes it infeasible to create a conventional laser directly from silicon. In current photonic technology, lasers are made from so-called III-V materials like InP or GaAs. (III-V comes from the internationally defined material descriptions group 13 and group 15.) Other materials may be used in some cases for other components, such as Lithium Niobate ("LN") for waveguides. An obvious solution then might be to simply process a III-V device as part of semiconductor manufacturing to add a laser source to a Silicon Photonic integrated circuit. There are several large obstacles to this approach, including that there are material mismatches between Silicon and III-V materials, so simply adding process steps to grow layers of the appropriate materials during wafer processing doesn't work as the resulting materials have defects. However, recent developments may point the way(s) around these obstacles.

As will be clear from what follows, there are a myriad of creative approaches being pursued around the world to find ways to directly integrate light sources into Silicon Photonics. However, it is almost certain that initial volume commercializations of highly integrated solutions will be so-called heterogeneous or hybrid integrations of the light source. Heterogeneous integration

means that gain material is manufactured separately then assembled to a photonic integrated circuit which in the case of Silicon Photonics is a silicon-based platform. Optical communication leader Neophotonics suggested this is the best route in their blog in April 2016, stating "Silicon Photonics needs an Indium Phosphide laser", which of course supported their launch of flip-chip integrate-able InP lasers for Silicon Photonics and other applications.

Heterogeneous and hybrid integration approaches range from assembling entire wafers to each other, to "flip chip" assembly methods where the III-V package is assembled with the top side "down" onto the silicon platform, with variations including adhesive bonding, soldering, self-assembly, metal contacts, and many other nuances. The issue with all of these is that, while it may be feasible to perform heterogeneous integration in high-volume semiconductor fabrication lines at acceptable yields, the complexity of the process raises costs, which is counter to the main tenet of pursuing Silicon Photonics: develop a system that can "drop in" to a "standard CMOS" fabrication line. Nonetheless, recent demonstrations of heterogeneous integration with lower costs are to be found, such as a recent creative approach by Tyndall National Institute. In a July 2016 paper the authors demonstrate integration of existing VCSELs (vertical cavity surface emitting lasers) to grating couplers on Silicon Photonics PICs, achieving the optimal tilt angle (10°) by a combination of etched features and solder ball size to tilt the bonded laser. The authors report that the passive alignment is within a 1 dB loss range which they report translates to +/- 1.6 µm, within the capability of existing flip chip tooling.

A wide range of possible solutions

A brief review of possible solutions, including hybrid, heterogeneous, and monolithic, illustrates the range of open options. In this summary list, both various integration approaches as well as a wide range of light generation strategies are represented. The approaches include:

- Laser micro-bench with late step integration to the Silicon Photonics (Luxtera),
- Template Assisted Bonding ("Skorpios Template Assisted Bonding", STABTM, Skorpios), with demonstrated 100 Gb/s Tx and Rx integrated chips,
- Discrete III-V laser packages to be "flip chip" installed to a silicon wafer and soldered or bonded, or using microbumps of copper or gold with pressure/thermal bonding or soldering (Northrup Grumman, Texas A&M, CEA-Leti, IBM, NeoPhotonics, and others),
- Placement of III-V laser packages using optoelectronic tweezers, in a massively parallel process (University of Glasgow),
- Wafer (whole) bonding of III-V wafers in some intermediate processed state with subsequent processing (University of Tokyo, A*STAR, Rochester Institute of Technology, and others), including SiO2 bonding with subsequent construction of a dual-cavity heterocore microdisk laser coupled to the silicon waveguide (A*STAR),
- Wafer to wafer transfer of III-V coupons/dies to a Silicon Photonics wafer with "modest" (our interpretation) alignment requirements (Ghent University-imec, Tyndall National Institute, A*STAR, and others),
- Transfer of epitaxially processed III-V dies onto Silicon Photonic wafers, using the same material for lasers and Electro Absorption Modulators, with demonstration to 32 Gb/s (III-V lab),

- Transfer of III-V active stacks to a Silicon Photonics wafer with "minimal" (our interpretation) alignment requirements due to the cavity being etched in the silicon (UC Santa Barbara, and others),
- Monolithic growth of InAs GaAs quantum dot (QD) lasers on Ge, Si, and Ge on Si using and AlAs nucleation layer to confine dislocation flaws and increase photoluminescence (University College London),
- Ultra-small microdisk and microring lasers based on InAs/InGaAs/GaAs quantum dots (St. Petersburg Academic University),
- High-speed 1310-nm Al-MQW buried-hetero laser having 29-GHz bandwidth (Finisar),
- Growth of group IV alloys, including Sn alloys with GeSi on silicon coupled with strain engineering to achieve a direct bandgap (Peter Grunberg Institute 9),
- Growth of metallic-group IV alloy shapes, predominately microdisks but also nanowires, pillars, inverted cones and others, such that they are waveguide coupled to drive them (Peter Grunberg Institute 9, Walter Schottky Institut, Max Planck Institute for the Science of Light, Huazhong University of Science and Technology, Stanford University, and others),
- Selective small-area growth of III-V regions on a Silicon Photonics wafer to avoid strain-induced flaws in the III-V material (Ghent University-imec),
- Monolithic growth of III-V material using a multitude of "buffer layers" to achieve a strain gradient with low-enough layer-to-layer strain to avoid most or all flaws (University College London),
- Monolithic growth of III-V material by MOVPE (metal-organic vapor phase epitaxy) in patterned grooves on silicon, where the lattice mismatched-induced defects are constrained within the groove area, and the III-V material grown above the groove is defect free, which is then used as the support for quantum wells (Ghent University-imec),
- Growth of defect-free Ge on silicon by creating Si nano tips on which Ge preferentially deposits (IHP/Xi'an Jiaotong University),
- GaAs-AlGaAs coaxial shell-core nanopillar lasers grown monolithically on top of a GaAs nanowire connection to the silicon layer (Walter Schottky Institut),
- 2-dimensional (disk) excitonic laser on silicon using Si3N4, monolayer WS2, and HSQ sandwich creating whispering gallery confinement modes (UC Berkeley),
- Cascaded silicon-Raman lasers (Intel),
- Distributed feedback evanescent lasers (UC Santa Barbara, Peking University),
- Mode locked evanescent lasers (UC Santa Barbara),
- Lasers using carbon nano-tubes (CNTs) (Université Paris Sud, George Washington University, University of Florence, FOTON (UMR CNRS), Kyushu University, Karlsruhe Institute of Technology),
- Rolled-up semiconductor tube lasers (McGill University, University of Illinois at Urbana-Champaign),
- Electrically pumped GaAsBi/GaAs QW diode laser (University of Surrey),
- Strain engineered Ge on Si (University of Michigan, University of Glasgow, Nanyang Technological University, MIT, Fudan University, Stanford University, and others),
- Phosphorous ion implantation into Ge on Si to enhance light generation efficiency 12-30% (Yonsei University),
- Doped III-V nanopillars grown on silicon as laser cavities (UCLA),
- Heterogeneous integration of III-V lasers and SOAs coupled with multiple ring resonators (UC Santa Barbara),

- Electrically pumped AlGaInAs-based multiple quantum wells (MQW) lasers bonded on SiO_2 interlayer on Si substrate, with an etched facet mirror metalized during the electrode formation step (A*STAR),
- Narrow linewidth and tunable lasers formed by loop-mirror cavity bounding an integrated III-V gain section, using an external cavity in silicon waveguide to narrow the linewidth and thermal tuning of a micro-ring resonator/phase section for tuning (UC Santa Barbara),
- Demonstration of 1.3 μm InAs/GaAs quantum dot lasers epitaxially grown on silicon by molecular beam epitaxy, with record output power (UC Santa Barbara),
- InAs microdisk lasers grown epitaxially on industrial silicon (Hong Kong University of Science and Technology),
- Silicon-Nitride microdisk integrated with colloidal quantum dots (Ghent University-imec),
- Single Ge quantum dot embedded in a silicon photonic crystal cavity (Huazhong University of Science and Technology),
- DFB laser monolithically integrated with a mirror and a lens, which is called a lens-integrated surface-emitting laser (LISEL) (Hitachi),
- Silicon quantum dot/SiO2 multilayer on Pt-coated Si nanopillars, with enhanced electroluminescence due to localized-surface-plasmon (Nanjing University of Posts and Telecommunications),
- Erbium-doped Silicon or Erbium compounds (MIT, University of Twente, KTH-Royal Institute of Technology),
- Tensile strained Ge quantum dots (Shanghai Institute of Microsystem and Information Technology),
- Flip-chip bonding of InP waveguide with a total internal reflection mirror to an SOI system with a grating coupler (Boston University, UC Santa Barbara, Oracle),
- Direct bandgap created by strain-engineered Si-Ge nanowells on silicon (University of Glasgow),
- Lasing in GaAs-AlGaAs core-shell nanowires in an Si/SiO2 system (Walter Schottky Institute),
- Directly modulated sub-wavelength InAsP InP nanowire laser on silicon photonic crystal with direct modulation to 10 Gb/s (NTT Nanophotonics Center),
- Flip-chip assembly of III-V laser assemblies onto an SOI interposer with micromachined mirrors (Oracle),
- λ-scale embedded-active region photonic crystal (LEAP) laser fabricated using buried regrowth of the active region (NTT Device Technology Laboratories),
- Three-terminal hybrid III–V-on-silicon laser with a metal-oxide-semiconductor (MOS) capacitor integrated into the laser cavity, allowing direct tunability of the wavelength and output, facilitating WDM (HP Labs),
- Sampled Grating Distributed Bragg Reflector (SGDBR) III-V laser directly bonded to silicon, tunable using the thermo-optic effect, supporting WDM schemes (Université Grenoble Alpes),
- Multi-frequency lasers using individual III-V gain sections with each channel controlled by its own ring resonator (Ghent University-imec),
- Multi-wavelength lasers using flip-chip metal bonded III-V evanescently coupled to silicon waveguide with different waveguide widths used to generate different wavelengths with good manufacturing tolerance (Peking University),
- Vernier comb laser using individual III-V gain sections with each channel feeding one ring resonator coupled to a shared ring as a vernier (Oracle),

- Semiconductor optical amplifier assisted extended reach EA-DFB laser (AXEL) (NTT Device Technology Laboratories), and
- Monolithically grown 1.3 um QD lasers using on-axis (001) p-doped Si, n-doped Si homoepitaxial buffer, 45 nm thick n-doped GaP nucleation layer followed by growth of 7 active layers to form a GRINSCH laser (UC Santa Barbara),

among others. We present this very long list to emphasize the point that the light source is an extremely active R&D area, and that we expect new solutions to emerge and be adopted commercially for at least the next 10 years.

Luxtera's approach is the most commercially successful to date; the company announced in September 2016 the shipment of the one millionth product containing their solution. Early in the life of their product, Luxtera noted on their website "Luxtera's CMOS Photonics™ technology will scale with Moore's law for electrical functionality and faster than Moore's Law (through DWDM for communications bandwidth". We think that newer approaches will likely supersede Luxtera's design. Currently, heterogeneous integration of III-V gain material onto the silicon platform is one preferred approach, as it has been well developed and appears to be reliable and stable enough for production. Recent research results have demonstrated techniques using coupled ring resonators as reflectors and tuning devices, achieving broad tunability and narrow linewidths, both of which are important to DWDM modulation approaches. Longer-term the development of quantum dot monolithic integration appears to be the most promising, but with so many potential directions, it is difficult to be certain.

As early as 1990, work had been done on monolithic integration of III-V materials on silicon, as illustrated in the patent issued to Kopin Corporation. Over the next 10 years various approaches were taken to try to implement lasers on silicon. Texas Instruments was awarded a patent using doped thin films to create a silicon laser in 1994. In 2003, Dr. John Sajeev and colleagues at the University of Toronto received a patent wherein synthetic silica opals were grown as a template to grow pure silicon "inverse silicon opals" which had a direct band gap at 1.46 μm. Patents appeared in 2003 for Quantum Dot methods and novel silicon photonic crystals formed by silicon ion implantation in silica.

Light from Silicon

In 2005, Intel announced a silicon Raman laser, saying that it "represents an important step towards producing practical continuous-wave optical amplifiers and lasers that could be integrated with other optoelectronic components onto CMOS-compatible silicon chips". Nonetheless, working with UC Santa Barbara, by 2006, Intel and UCSB reported an electrically pumped hybrid AlGaInAs silicon evanescent laser. That development and variations using other III-V materials became the basis for various commercial efforts. Over the next few years, other approaches such as mode-locked and distributed feedback (DFB) lasers were demonstrated using similar evanescent coupling to the silicon waveguide structures.

Work continued to seek paths to lasers on silicon. In 2010, demonstration of rolled-up semiconductor tubes housing Quantum Dots was reported by McGill University. Other work focused on "traditional" quantum dots and quantum wells as light sources. In addition, some reports of strain-engineered group IV materials, especially Ge and Si-Ge, were published. In

2014, McGill reported coupling of the rolled up semiconductor quantum dot laser to a silicon waveguide, and in 2015 demonstrated electrical pumping (but only at low temperatures so far). More exotic approaches were reported, including work from Peter Grunberg Institute 9 on direct band gap GeSn alloys (but optically pumped), Shanghai Institute of Microsystem and Information Technology with strain engineered Ge QDs, Huazhong University of Science and Technology with Ge QDs in silicon nanocavities, UCLA showing arrays of III-V nanorods grown on silicon as laser cavities, and Ghent University reporting on SiN microdisks. The Rochester Institute of Technology demonstrated in late 2015 high-performance InAs quantum dot lasers by constructing the laser heterostructure on GaAs wafers, then wafer bonding the resulting lasers to a SOI system, using a Pd mediated low-temperature bonding which resulted in low interfacial resistance and commensurate high laser performance.

As with many difficult technological problems, the most recent work is the most promising, indicating a possible path forward to true monolithically grown laser sources. Both University College London and University of California Santa Barbara have reported long continuous operation results with monolithically grown III-V QD lasers. The challenge of threading dislocations that occur when III-V material is grown directly on silicon may have a solution, in a combination of using Quantum dots with highly-developed engineering of transition layers and other approaches. It is interesting to note that QD emission occurs from many highly-localized sources (the dots) which helps overcome the problem of defects (the threading dislocations), as localized defects only impact one or a small number of dots, leaving the rest to produce high quality light. This points towards QDs as a better option than quantum wells, for example, unless/until the dislocation defect issue is solved. A review by UC Santa Barbara of progress in heterogeneous Silicon Photonics in August 2015 provides a good summary of design approaches, with one point being that new and novel approaches continue to appear. More recently (December 2016), UC Santa Barbara demonstrated another monolithically grown QD laser approach, using n-doped Si as a single buffer layer.

On the front of solving the dislocation defect issue in monolithic III-V growth on SOI, very recent work by Ghent University-imec has shown a novel way to avoid the unwanted defects. The Ghent method involves etching grooves into silicon and growing III-V material into and above the grooves. With suitably narrow grooves, and using metal organic vapor phase epitaxy (MOVPE), the defects are effectively constrained to the groove area, and the material above, which also is grown to a wider dimension than the grooves, is defect free. Ghent University-imec demonstrated this groove-MOVPE approach on 300 mm silicon wafers. The Hong Kong University of Science and Technology, collaborating with UC Santa Barbara and Harvard University, showed a variant of QD integration, demonstrating "the first 1.3 μm room-temperature continuous-wave InAs quantum dot micro-disk lasers epitaxially grown on industrial compatible Si (001) substrates without offcut".

Very recently (July 2016) HP Labs demonstrated that GaAs/InAs QD lasers could be heterogeneously integrated using an O2 assisted plasma bonding in a SOI system. Their approach eliminates three issues with other QD hetero-integration schemes--the devices are directly bonded, eliminating additional layers such as metal layers which incur losses, the system is compatible with SOI using a commercially available buried oxide (BOX) configuration, and the metal contacts are on the III-V stack, avoiding metal in the light-coupling region. The authors

point out that QD lasers have excellent thermal characteristics and by nature of the small variation in the QDs, have a large gain bandwidth, allowing more channels in WDM systems.

Several groups, notably Skorpios, UC Santa Barbara, and NTT Device Laboratories have developed approaches wherein the III-V stack is transferred to the silicon wafer and the critical features are then formed (or are partially formed prior to bonding) using lithography. UC Santa Barbara announced "The World's First Hybrid Silicon Laser" in September of 2006. Skorpios applied for patents on their version beginning in 2011. NTT was working on Silicon Photonics from at least the 2010 time frame, but only recently published a hybrid approach similar to the previous work. All of these approaches reduce the alignment requirement compared to transferring a complete laser with alignment to the silicon waveguide. Skorpios has also taken the approach to create modulators in the III-V material, to result in a system without required thermal tuning as is necessary with most silicon-based modulation schemes. Skorpios showed their lasers in a proof of concept 400G solution in 2014, in commercially available 100 Gb/s transceivers in 2015 and, more recently, reported in August 2016 a 4-wavelength CWDM solution based on the approach. Considering all the factors and the state of the industry, we think this hybrid integration is the main platform commercially at present, although by no means is any approach mature.

On another path, research at TU Munchen has demonstrated monolithic epitaxial growth of GaAs-AlGaAs "core-shell" nanowire lasers, although so far they are optically pumped. (To serve as light sources in IPE devices, electrical pumping is a requirement. Among other reasons, electrically pumped lasers offer the potential for direct modulation, which is discussed below.) The researchers' process involves etching an 80 nm hole in a 250 nm layer of SiO2 deposited on silicon, growing a GaAs nanowire in the hole to form a connection to the silicon layer, then adjusting growth parameters to grow ~470 nm diameter hexagonal GaAs pillars, which are then protected with a thin layer of AlGaAs. Earlier work at UC Berkeley has shown approaches to electrically pump these structures, although this has not been demonstrated for lasing in a GaAs nanopillar on silicon so far. In the TU Munchen work, the authors suggest a path to electrically pumped nanopillar lasers as well. Another interesting possibility using III-V nanowires comes from Paul-Drude-Institut für Festkörperelektronik, who showed (in simulation) that an array of nanowires oriented vertically over a waveguide can be arranged in a grating coupling configuration, directly coupling laser output into a waveguide at 45% coupling efficiency.

On the heterogeneous path, record results have been obtained by UC Santa Barbara and NEC have shown designs using so-called external cavities which are implemented as silicon ring resonators to control the frequency of heterogeneously integrated III-V lasers. These designs also incorporate III-V Semiconductor Optical Amplifiers (SOAs) as part of the structure to improve performance. Related approaches have been reported by NEC, Oracle, and the Huazhong University of Science and Technology. Oracle recently reported a wall plug efficiency of over 12% with their heterogeneous design, which integrates the laser as a component. The other main approach to heterogeneous integration is using so-called flip-chip assembly, wherein laser dies made on III-V wafers are transferred to the silicon platform using high-volume assembly automation. The challenges for these approaches are the alignment of the laser output to the PIC. Even with grating couplers with relaxed tolerance, the requirements are still stringent. IBM has pursued a variety of approaches, always with a key requirement being integration into high

volume manufacturing. In one successful approach IBM demonstrated a flip chip assembly followed by solder melt, and used the surface tension of the molten solder to pull the laser chip against a butt-coupling facet on the PIC.

Alternatively, gain medium has been created by Erbium doping of waveguides, as well as other rare-earth approaches, with promising results shown by KTH-Royal Institute of Technology in early 2016. The University of Twente has also demonstrated in a December 2016 paper integrating gain medium using Erbium doping in a monolithic process. We think these approaches could have merit long-term but the main thrusts in the industry seem to be elsewhere for now.

On the point of using ring or ring-like ("racetrack" and other variants) resonators, it is useful to note that various passive elements in silicon may be integrated to provide laser tunability, narrow line widths, filtering, wavelength division (for WDM) and provide other useful performance characteristics. Of these, the silicon micro-ring resonator is perhaps the most useful. Roughly, consider that the ring is a resonant structure, where it comes into resonance at particular wavelengths (frequencies) based on the size of the ring relative to the wavelength of the light. There are many demonstrations where the frequency of resonance is tuned by changing the temperature of the region of the silicon containing the ring, which changes the size of the ring and thereby the resonant frequency. It has also been demonstrated that resonators can be made with modifications such as TiO2 cladding to virtually eliminate temperature dependence--these developments point the way for more mature product embodiments where components can be removed from fixed-purpose designs. Thus, ring resonators in silicon can provide a multitude of functions and be either tunable or temperature stable ("athermal"). The fact that feature sizes are small in silicon due to the index of refraction difference between silicon and surrounding material, and the relatively low loss in silicon waveguides, has allowed the micro-ring resonator to become the workhorse of many implementations. Note that the actual shape of the structure can be varied from circular, and at times oval shapes (often called racetracks) and a wide range of other designs have been demonstrated.

Wavelength multiplexing

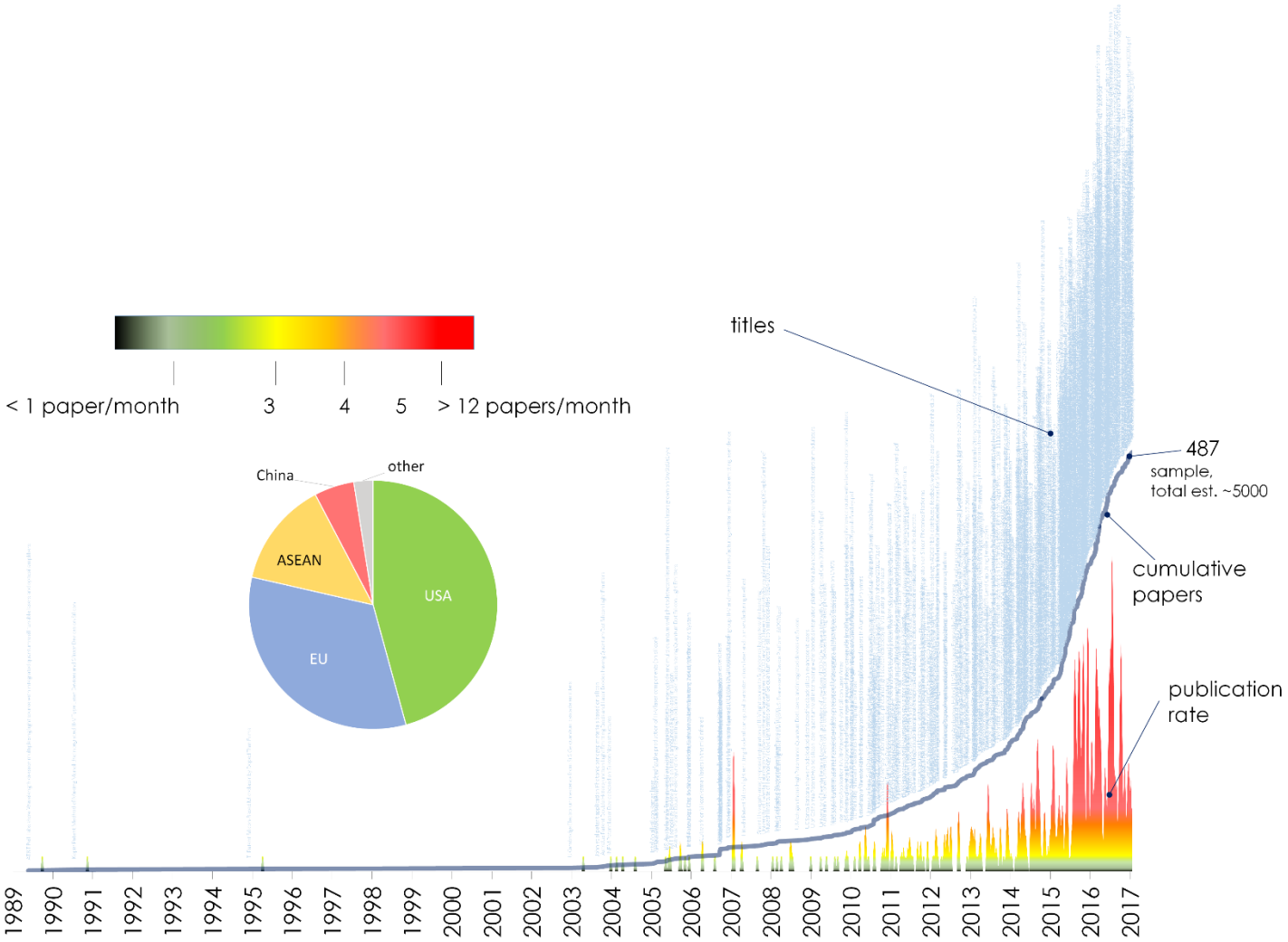
In commercial applications, it is desirable to generate multiple wavelengths in order that multiple signals can be sent on a single fiber, increasing capacity. This multiplexing takes advantage of the fact that different wavelengths of light do not interfere with one another when traveling in the same medium. In practice today, there are two general levels of wavelength multiplexing, Coarse Wavelength Division Multiplexing (CWDM) and Dense Wavelength Division Multiplexing (DWDM). These two multiplexing schemes are characterized by the spacing of the different frequencies of light, and in general CWDM has fewer wavelengths multiplexed onto single fibers than DWDM; CWDM commonly has 4 wavelengths. Given that WDM is needed, there is then the need to generate multiple frequencies of light on the chip. There are a range of approaches, including using sophisticated modulation schemes to generate properly spaced wavelengths; one approach is called a vernier. Oracle showed in August 2016 an approach using one common ring resonator and then separate gain sections and secondary ring resonators to generate the wavelengths. In September 2016, Universite Grenoble Alpes demonstrated that using sampled grating distributed Bragg reflectors to form the laser cavity enabled continuous tuning of a III-V laser across as much as 35 nm, and thus suitable for WDM schemes. As far back as 2013 Ghent University-imec showed a similar

approach using only one ring resonator per wavelength. In 2014, Peking University demonstrated using evanescently coupled distributed feedback lasers coupled to different silicon waveguide widths allowed generation of different wavelengths with good manufacturing tolerance margin and eliminating the need for ring resonators with their requisite thermal tuning (which consumes more power).

As we will note elsewhere, there are some challenges in Silicon Photonics designs resulting from high insertion loss occurring in some components, notably the modulation section. NTT has reported a new design for a modulated Silicon Photonic light source called a "semiconductor optical amplifier assisted extended reach EA-DFB laser (AXEL)". The main feature of the AXEL is that a low power laser is coupled to an electro-absorption modulator, then a SOA is used to amplify the modulated light. By moving the amplification downstream of modulation, losses inherent in the modulator are much less than conventional designs. The authors report in a January 2017 paper that the device uses about half the power of a conventional design for the same data rate and performance, and likewise provides about double the power into the fiber when operated at the same supplied power.

It is evident that a multiplicity of integration schemes are being explored to integrate light sources into Silicon Photonics in a manufacturable way. Nonetheless, until a true monolithic approach is fully successful, some alignment, or bonding, or other additional process or processes are needed to integrate the assembly. In schemes where the laser is formed in a separate III-V process and then attached to the Silicon Photonics platform, light must transfer from the III-V stack to the Silicon Photonics die. We expect this step to always be at the Silicon Photonics wafer level, to leverage existing high-volume flip-chip assembly technology. The actual alignment mismatch between the two stacks can greatly impact the efficiency of transfer. Ghent University-imec have done recent work (June 2016) in the area of creating "Novel adiabatic tapered couplers for active III-V/SOI devices fabricated through transfer printing." Transfer printing refers to a process where a thin polymer is used to pick and place dies onto a wafer in a massively parallel step. This approach had been demonstrated by Tyndall National Institute for GaAs lasers in 2012, but has not seen wide adoption. The challenge is that the resulting alignment tolerance is as tight as 1000 nm (1 μm). Ghent University-imec have shown that combining a thick InP waveguide (in the III-V stack) with an adiabatic taper (in the Silicon Photonics) the required alignment tolerance is sufficiently relaxed as to be adequate for existing processes. They also demonstrated the use of a polymer intermediate layer which eliminates the need for the additional III-V waveguide processing.

Similarly to other metrics we have put forth motivating the case that it is "early days", an integrated light source is one of the most fundamental of building blocks. The figure here illustrates the increasing pace of research by charting the cumulative publications related to light sources and the rate of publication.



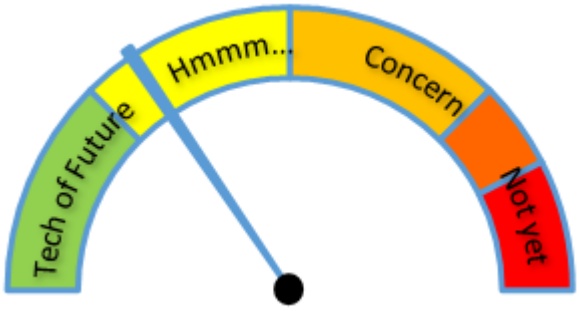
Publications related to potential light sources for integrated Silicon Photonics. The upper trace shows cumulative papers since 1989, with the titles above to show the high publication density in recent years. The lower chart shows the rate of publication, with the evident high peak rates since 2014. Source: EAF analysis of >1800 publications in Silicon Photonics for communication.

The net of this is we feel that solutions implemented in the next 5-10 years are very likely to give way to more integrated and lower-cost platforms. There are also likely to be multiple branches of the evolutionary trajectory, with certain approaches being favored for some applications, and other approaches for other applications. Choices may also be dictated by available foundry capabilities, ownership or licensing of intellectual property, and market demand volume for the product, to name a few criteria. Returning to earlier remarks on energy consumption and the concerns about the current state of Silicon Photonics, Peking University reviewed the energy consumption tradeoffs and issues in an August 2015 publication. The authors conclude with a number of recommendations, and the tradeoffs. As an example, they note "When size is not critical, MZI based devices could achieve athermal performance without extra energy consumption. Microring-based devices have smaller sizes but need high negative-TOC material to eliminate the thermo-optic-related energy consumption, which is still under research.

Athermal microring structure is difficult to design, but it might be an ideal solution to the thermo-optic issue associated with microring-based devices." Again we emphasize that there remains much work to be done towards standard, semi-ubiquitous application of Silicon Photonics for interconnects.

Considering the ongoing evolution of micro-electronics, following Moore's Law for decades, it is not unexpected that integrated photonics, and Silicon Photonics in particular, will see ongoing improvement for some time. The pace of change in the sense of Moore's Law is to be seen, but is very rapid at present.

Modulation



Risk meter for modulation. The main driver of remaining risk is the efficiency of the modulation scheme, as well as the frequency of operation (data rate). There are good solutions using micro-ring resonators, but in the future solutions based on multi-mode interferometers or other approaches may prove more efficient and faster. Direct modulation may also be feasible with some light sources, having been demonstrated at nearly 70 Gb/s in some studies. Source: EAF analysis.

Modulation is simply a term meaning to use a scheme to encode information in a signal. If the goal is to send information on a channel at 100 Gb/s, then a modulation scheme is needed to accomplish that. In the case of Silicon Photonics, a wide range of modulation devices have been developed in silicon. In fact, this is an area where Silicon Photonics might be said to have strength. However, it is also reasonable to expect that ongoing development will occur in this area. Work in this area dates back to the earliest efforts in Silicon Photonics as it was recognized that modulation is a key and essential enabling technology. Intel published the first GHz silicon modulator in a 2004 letter to Nature, and developments have continued apace. A few years later, IBM demonstrated WDM using only silicon waveguides in an SOI wafer having about 3 nm channel spacing.

At present, microring resonators feature in many solutions as they are compact and, importantly, actively tunable via thermal control. Tunability can be implemented by adding heating devices to the design, and varying the temperature of elements such as microrings. This changes the physical dimensions of the elements due to thermal expansion, which changes the frequency of operation. Although we conclude below that the risk around the modulation function is low, there are some concerns. A good example is provided by PETRA (Japan) who point out that some microring modulation schemes could have issues in mass production, as the possible manufacturing variations could lead to excessive temperature requirements to tune the modulation frequency. The authors then describe a potential solution using a Fabry Perot cavity

with a microring resonator inside the cavity, and demonstrate the design can dramatically reduce the temperature range required for tuning. Another interesting development towards robust thermal control and management is the implementation of micro-thermoelectric modules to control the temperature of lasers. It is well known that laser performance tends to degrade at elevated temperature, hence the often-used modifier when reporting new laser developments for Silicon Photonics: "room temperature". Work by Alcatel Lucent Bell Labs has shown the feasibility of integrating thermoelectric devices directly with the laser. Thermoelectric devices allow both cooling and heating in the same device simply by reversing the current flow. Thus, such locally integrated devices can cool the laser and operate on a timescale that, in the words of the authors, "can meet the thermal requirements of active photonics devices in silicon photonics under realistic operating conditions."

If we consider a continuous output laser (CW) to be used in sending information, then as noted the output must be modulated to encode information. Encoding can take the form of simple on/off (OOK, or on-off keying), or can be more complex. For example, when using coherent light (from a laser), then the phase of all the optical waves are aligned. Changing the phase then can be used to encode information, in so-called Phase Shift Keying. Since phase is a continuous variable, PSK is not limited to two values (like the 1s and 0s in a digital signal) and more complex schemes, such as QPSK (quadrature phase shift keying) are used to encode more data in a given signal. Since light also has a polarization (the direction of the oscillations of the electric and magnetic fields), it is also possible to encode different data in different polarizations to further increase the data density.

Light is comprised of a spectrum of wavelengths (colors for visible light), so that the light can be divided into multiple data streams of spaced wavelengths, which is referred to as Wavelength Division Multiplexing (WDM) and allows more data to be sent over a given fiber. Although lasers are commonly thought of as operating at a single wavelength, in practice there is a narrow spectrum of light emitted which can be further subdivided. The acronyms CWDM (Coarse Wavelength Division Multiplexing) and DWDM (Dense Wavelength Division Multiplexing) describe, as the names imply, dividing up the available spectrum into less or more unique frequencies (colors) in order to encode more information on a single fiber. Although the multiplexing isn't a modulation scheme we include it here as part of the general class of operations to allow a given amount of data to be encoded per unit time in an optical communication system. Both WDM and PSK allow multiple streams of data on the same fiber, thereby increasing capacity. We will also cover a number of other circuit elements that are implemented in silicon to support modulation and other functionalities.

Direct modulation

While there are a number of photonic circuits that can be used to achieve the various modulation schemes, there are benefits of directly modulating a light source, in terms of component reduction and loss. Direct modulation refers to applying a modulating signal directly to the power source for the light-emitting component. Since the systems of interest in Silicon Photonics are nearly all electrically pumped semiconductor lasers or a combination of light sources, amplifiers and resonant cavities, the modulation is applied either to the pump current or to the amplifier current. While direct modulation is attractive in principle, the majority of Silicon Photonic devices to date use additional modulation on the light output of the laser.

While effective, all external modulation schemes use additional power and add insertion loss. Before moving on to the main examples of modulation, a few examples of promising direct modulation are:

- Modulator-free quadrature amplitude modulation signal synthesis (University of Southampton),
- Direct phase modulation at 25 Gb/s of semiconductor optical amplifiers in a QD SOA system (Technische Universitaet Berlin),
- Direct modulation of InGaAsP multiple-quantum well membrane buried distributed feedback laser (DFB) on wafer bonded InP up to 40 Gb/s (NTT Photonics Laboratories),
- Directly modulated heterogeneously integrated InP/SOI DFB laser up to 28 Gb/s (INTEC/imec, Ghent University),
- High modulation efficiency (11 GHz/mA$^{1/2}$) GaInAsP/InP membrane DFB laser on silicon at 10 Gb/s (Tokyo Institute of Technology),
- Fast tuning of a laser using two ring-cavities to effect frequency selection (Alcatel-Lucent),
- 69 Gb/s DMT modulation using a directly modulated heterogeneously integrated InP-on-Si DFB laser (Ghent University-imec).

The Alcatel-Lucent work latter isn't direct modulation per-se, but is direct manipulation of a laser and is important to future implementation of schemes like optical packet switching for enhancement of network capacity, the same general goal as advanced modulation schemes.

Turning attention to modulators, there are a range of "components" useful to or related to modulation. These include so-called interferometers, which can be thought of as ways to use two signals, combined in ways that extracts information from small differences, such as phase shifts, between the two. Interferometers feature prominently in Silicon Photonics, especially so-called Mach-Zehnder interferometers. The details aren't critical to understanding the technology status, but the terms appear frequently in results so it is useful to be familiar with them. Other components of interest include splitters, couplers-including multimode interference (MMI) couplers (devices which can be very small and function as splitters and other functions), gratings (also appearing in chip to fiber coupling), tapered waveguides, resonators (ring and other varieties), filters, frequency combs (a group of components splitting a bit of spectrum into several discrete wavelengths), polarization splitters, polarization rotators, tunable cavities (similar in function to ring resonators), disk resonators (as the name implies, small disks of material, sometimes selectively grown, on a pillar and coupled to a waveguide), loop mirrors (related to resonators, these devices "reflect" certain frequencies back to the source and are useful in amplification as well), interleavers (conceptually used to combine narrowly spaced "odd" and "even" channels onto a single stream, or the reverse), coupled resonator waveguide filters (CROW filters--see text), multiplexers/de-multiplexers, and phase shifters.

A note regarding the manipulation of the optical energy--similarly to RF circuits and even acoustic circuits, since the light is confined to waveguides as it is moved around the PIC, and is a wave phenomena, the existence of resonance is used in many different circuits to couple energy from one element to another, or to select only certain frequencies, and other similar behavior. An example is a coupled resonator waveguide filter, or CROW filter. In such a device, a ring of waveguide is passively coupled to another waveguide without a physical connection. The dimensions of the ring determine a characteristic frequency or resonant frequency; at that

frequency the energy is strongly coupled from the waveguide to the ring. Such structures can be combined to narrow the pass-band of a filter, which is the case with the CROW filter. Silicon photonics has the very significant advantage that these features are all very small in the infra-red frequencies of interest used in optical communications.

Some recent advancements in this area include, by general approach:

Rings and racetracks:

- Use of in-track delay lines and in-loop reflection to achieve resonator tunability with a large spectral and tuning range (Ghent University-imec),
- Single-sideband modulation using coupled resonator optical waveguide (CROW) filters comprised of 6 racetrack resonators coupled in series (University of Sydney),
- Reconfigurable optical add-drop multiplexer using thermally tuned ring resonators (R&D Center of Optoelectronics, Institute of Semiconductors)
- Generation of Kerr frequency combs using SiN microring resonators (Purdue),
- Twin coupled microring resonators achieving variable cavity coupling to provide widely tunable frequency combs (Cornell),
- Implementation of a 4x20 Gb/s WDM modulator and integration to CMOS driver (imec),
- Implementation of a DWDM filter using a system of four non-identical ring resonators to create a Vernier (University of British Columbia),
- 40 Gb/s modulation using interleaved P-N doped regions (State Key Laboratory for Integrated Optoelectronics, Institute of Semiconductors),
- Combination of cascaded microring resonators with interleaved P-N doping to achieve up to 50 Gb/s modulation (State Key Laboratory for Integrated Optoelectronics, Institute of Semiconductors),
- III-V laser with integrated ring resonator and electro-absorption modulator with bit rates to 32 Gb/s (III-V Lab),
- Modulation filtering to eliminate most of the ring resonator tuning (heating) power, resulting in total transmitter power of < 0.27 mW/Gb/s for 25 Gb/s operation (PETRA),
- Si3N4 microring based configurable add-drop multiplexer (University of Twente),
- PAM-4 modulation using cascaded microring DAC less modulator with low power consumption (100 fJ/bit, 60 Gb/s) (Université Laval),
- PAM-8 modulation using DAC-less segmented Mach-Zehnder modulator operating up to 114 Gb/s with ultra-low power consumption (Université Laval),
- III-V/Si Hybrid Verniered-Ring Comb Laser (VRCL) with 200 GHz tunability and individually addressable channels using an SOA for each channel (Oracle),
- Frequency comb with output selectable as an integer multiple of the free spectral range of a high Q microring resonator, with automatic thermal compensation using a feedback mechanism (Xi'an Institute of Optics). and
- Microring resonators with "pinched p-n" junction integrated microheaters, resulting in wide tunability and sub µs response time (UC San Diego).

Microdisks:

- Transparent graphene integrated heaters to achieve a thermally tunable silicon microdisk resonators (Zhejiang University),
- Ge microdisks with lithographically tunable strain (Stanford University), and

- Stacked Si/SiO2 microdisk electro-optic modulator up to 15 Gb/s (Georgia Institute of Technology).

Plasmonics:

- Plasmonic phase modulator coupled to a gain assisted (e.g. w/an SOA) resonator for PSK at 10 fj/bit (Kim Il Sung University),
- Indium-Tin-Oxide (ITO) in a plasmonic waveguide for small electro-absorption modulator (Rochester Institute of Technology),
- All plasmonic Mach-Zehnder modulator fit into a Si waveguide and operation up to 70 GHz (ETH Zurich),
- Graphene-based waveguide integrated dielectric-loaded plasmonic electro-absorption modulators (Singapore University of Technology),
- Plasmonic Mach-Zehnder modulator using metal-insulator-metal design (Tokushima University),
- Compact polarization rotator using plasmonic slot waveguides having less than 1 dB insertion loss for TM to TE conversion (Southeast University, Nanjing),
- Plasmonic Electro-Absorption modulator capable of GHz operation (Rochester Institute of Technology), and
- Electro-optic modulator based on hybrid plasmonic micro-ring-disk resonator with embedded electro-optical polymer, with power consumption of only 1fJ/bit (Istituto per la Microelettronica e Microsistemi).

Gratings, polarization, and other approaches:

- Perfectly vertical grating coupler that performs chip to fiber coupling with low loss (5.4 dB) and modulation (Institute of Semiconductors Beijing),
- Dual phase-shift Bragg grating modulator up to 60 Gb/s (Université Laval),
- Low crosstalk Bragg grating Mach Zehnder interferometer OADM (McGill University),
- Implementation of Discrete Multi-Tone modulation achieving 4 x 100 Gb/s (Alcatel-Lucent).
- Compact interleaver using loop-mirror based Michelson-Gires-Tournois Interferometer (Shanghai Jiao Tong University),
- Segmented modulator electro-optic-DAC for 100 Gb/s PAM-4 modulation (McGill University),
- High-Q SiO2 micro-toroid formed by remelt after etching to form a toroid on the inner lip over a cavity (RWTC Aachen),
- Nested Mach-Zehnder modulators with polarization rotators and combiners for DQSPK modulation to 128 Gb/s (Fujikura),
- Mach-Zehnder modulators with Silicon-Insulator-Silicon capacitors for phase modulation achieving 112 Gb/s over nearly 2500 km of single mode fiber (Cisco),
- Mach-Zehnder modulator generation of optical dual binary (ODB) modulation at 56 Gb/s with improved chromatic dispersion (Futurewei Technologies),
- Slow light generation by corrugated waveguide and P-N junction based phase modulation for 40 Gb/s performance (Universitat Politécnica de Valencia),
- Multi-mode interference with slot waveguides as wavelength demultiplexer (Southeast University Nanjing),
- Graphene electro-optic modulator based on resonator loss modulation at critical coupling, achieving 30 GHz bandwidth (Cornell University),

- Lithium Niobate on silicon Mach-Zehnder modulator up to 50 GHz with performance equal to traditional Lithium Niobate modulators in a smaller platform suitable for Silicon Photonics integration (University of Central Florida), and 110 GHz performance using thin-film Lithium Niobate (University of Delaware),
- Vertical slot microring providing minimal wavelength mismatch between TE and TM modes (National Taiwan University),
- Graphene on silicon microrings for wavelength conversion (Huazhong University of Science and Technology),
- Compact Silicon Photonic Interleaver Using an Interfering Loop Containing a Fabry-Perot Cavity Formed by Sagnac Loop Mirrors (Shanghai Jiao Tong University),
- Trench-coupler based silicon Mach-Zehnder thermo optic switch (Beijing University),
- Monolithically Integrated High-Extinction-Ratio MZM With a Segmented Driver in Photonic BiCMOS (IHP Germany),
- Highly linear heterogeneously integrated (InP) Mach-Zehnder modulator on silicon, and Ultra-linear ring-assisted heterogeneously integrated (InP) Mach-Zehnder modulator on silicon, both using III-V (InP) gain material to linearize the silicon phase modulation response (UC Santa Barbara),
- Ultra-high (17 million) Q "finger shaped" SiN resonators with large free-spectral range and low frequency comb power (Purdue University),
- Capacitively tuned, low power consumption silica microtoroid resonator with ultra-high Q (~100 million) (University of Queensland),
- Self-coupled optical waveguide (SCOW) interleaver providing high extinction ratio without thermal tuning (Shanghai Jiao Tong University), and
- Strip-loaded waveguide modulator using hydrogenated amorphous silicon on an etchless SOI layer with 1.6x higher modulation efficiency and 30% lower insertion loss compared to a ring assisted Mach-Zehnder modulator (National Institute of Advanced Industrial Science and Technology).

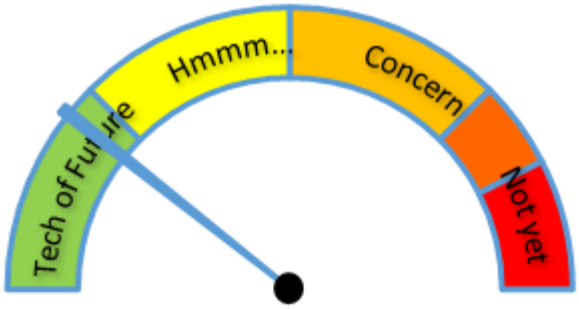
Plasmonics as mentioned in the list are in a class of phenomena where the electromagnetic energy, in this case in the form of photons in the infra-red region of the spectrum, are coupled to fixed charges in metals. Because of the metallic behavior of graphene, many groups are working on graphene plasmonics, but other metals are also used. This photon-metal interaction can allow devices much smaller than diffraction would imply, and thus are very interesting for nano-photonics. This is an area that likely will continue to develop and new classes of integrated plasmonic-photonic devices will appear. An example is given by a study published in March 2016 by CIC NanoGUNE, who conducted a detailed mapping and imaging of plasmons in graphene structures. More recently, the Technical University of Denmark showed in a November 2016 paper an approach to generate graphene plasmonic behavior in the near infrared. In July 2016 Tokushima University demonstrated a Mach-Zehnder modulator based on plasmonics, showing that ultra-compact functional devices are achievable (their devices were on the order of 0.6 x 6 μm and 0.5 x 3 μm). Earlier work includes plasmonic electro-absorption modulators (Rochester Institute of Technology) and polarization rotators (Southeast University, Nanjing). Whereas at the moment (early 2017) the dense integration already provided by Silicon Photonics is very attractive, it seems likely that over the next 5-10 years of development more use of plasmonics will be seen in products.

Modulation and related devices is an area where the toolbox for Silicon Photonic circuit designers is already full of useful circuit elements. We do not see this as a high-risk area, but we also expect ongoing development and novel designs that will integrate more components and allow even more control over the light, as well as reduce losses and lower power requirements (e.g. power used for thermal tuning). For example, the use of BiCMOS as the platform shown by IHP Germany has not been greatly explored (although IBM did recently report some of the work using 0.25 µm BiCMOS and fabricating a 40 Gb/s transmitter); also advanced modulation schemes will be more important as, say, the industry moves towards 400G from 100G designs. Thus, there is some (risk x impact) of obsolescence. The impact would mainly be on the silicon providers (just as today Moore's law has them on a development treadmill) and to some extent on data center owners/operators, in that higher data rates may be hand in hand with new modulation schemes. Note that in some cases upgrades have been available by replacing prior copper Ethernet cables with Active Optical Cables to deliver speed improvements. As the transition to optical becomes more ubiquitous, the architecture of where the conversion from electronic to photonic may impact the availability of pluggable upgrades. Stated another way, there are likely points in the evolution of integrated photonic-electronic devices where a new backplane architecture will emerge. These server-rack architecture changes will present opportunities to introduce newer Silicon Photonics technologies.

We have not discussed in any detail the details of the modulation schemes themselves. While it isn't important to understand details of modulation, it is important to keep in mind that both ends of an optical link must use the same modulation. Thus, upgrades to a given layer in the architecture to use more complex modulation to achieve higher data rates must occur in a holistic way. The modulation scheme is essentially how the binary data--the 1s and 0s are actually encoded, and determines in part the maximum bit rate when using a given wavelength of light. There are schemes noted above to divide a given laser output into multiple, finely divided wavelengths--so called Wavelength Division Multiplexing (which has variants called Coarse WDM (CWDM) and Dense WDM (DWDM). Regardless of the wavelength multiplexing, a modulation scheme is used to encode data on each wavelength. Modulation schemes include Pulse Amplitude Modulation (PAM, such as PAM-4, Differential Phase Shift Keying (DPSK), Phase Shift Keying (PSK), Quadrature Phase Shift Keying (QPSK), and Quadrature Amplitude Modulation (QAM), among others. The different modulation schemes have their own benefits and drawbacks. Also, in general, there are additional variants within a category, such as 16-QAM or 64-QAM which have more unique signaling levels encoding more bits per cycle. Moreover, other schemes are under investigation as there is a pressing need to increase capacity of existing fiber (in long-haul distances, such as inter-data center and longer) to avoid having to install additional fiber, which is very costly. A recent example (July 2016) comes from the University of Science and Technology (Beijing), who demonstrated 112 Gb/s over 80 km of fiber using PDM PAM-4, where PDM is Polarization Division Multiplexing. Just earlier in June 2016, Nokia Bell Labs demonstrated 128 Gb/s over 100 km using a Silicon Photonics Stokes vector receiver. In August 2016 Huawei reported on 180 Gb/s PAM-4 modulated transmission over 2 km fiber, which is considered the benchmark distance for hyper-scale data center interconnect. For standards-based optical communication systems, the modulation scheme is defined in approved documentation which, in part, ensures interoperability of hardware from different vendors. Nonetheless, companies like Facebook may move ahead faster than standards adoption, pushing suppliers to introduce higher-performance products optimized for data centers.

Facebook is pursuing a project called Voyager as part of an industry-led "Telecom Infra Project" that combines DWDM with packet approaches to achieve higher throughput.

Waveguides



Risk meter for waveguides. One motivation of Silicon Photonics are the desirable properties of waveguides in the SOI system. Nonetheless, some research has shown that hybrid systems, such as lithium niobate on silicon and silicon nitride on lithium niobate on SiO2 may offer lower losses or provide advantages in constructing devices such as resonators. Source: EAF analysis.

Silicon is relatively transparent in the infrared region used by communication fiber optics. This needs to be taken in context because the losses per cm depend significantly on the waveguide design and type, the latter decision has tradeoffs such as loss versus minimum bend radius. There are proposals to use other materials in combination with the SOI platform, such as Lithium Niobate which has been studied in detail, for example by Wiegel et al (UC San Diego). Nonetheless, in general, most Silicon Photonic approaches use strip silicon waveguides, ridge waveguides, or silicon photonic crystal waveguides to transport the light through the photonic integrated circuit. Strip waveguides have higher loss (2-3 dB/cm) but can be used in tighter bends (due to strong light confinement) than ridge waveguides, which have much lower loss for straight waveguide (< 0.3 dB/cm). Universite Paris Sud have presented a good analysis of the properties of both forms of silicon waveguides. Other hybrid systems have been proposed to reduce losses or add other functionalities, such as SiN on silicon (University of Toronto, Sun Yat-sen University, NIAIST, and others) and others. Losses of 1.3 dB/cm were reported by University of Toronto for SiN channel waveguides on silicon. NTT reported losses of 1.2 dB/cm at 1500 nm for SiN waveguide fabricated using novel deuterium-based silane in place of normal silane (SiH4) gas in the deposition step. Losses in pure Lithium Niobate can be less than 0.2 dB/cm, but in hybrid systems of interest in Silicon Photonics, the losses are somewhat higher than silicon waveguides. INRS and Infinera demonstrated a high-index glass called Hydex® from which waveguides with losses as low as 0.06 dB/cm can be fabricated in CMOS compatible processing environments.

Recent work, such as shown by PETRA (Japan) and others demonstrates that careful selection of the silicon on insulator (SOI) layer thickness as well as the waveguide dimensions can achieve low losses and control the transmission mode and polarization. The PETRA work also showed that using state-of-the art ArF (Argon-Fluoride) etch created smoother side walls of the waveguide, significantly lowering losses; Losses below 0.5 dB/cm have been shown. This is a good example where a key process may not be available in every foundry, so there could be design and performance tradeoffs based upon the available processes. Work at UC Santa Barbara showed

SiN on silicon waveguides with losses as low as 0.04 dB/cm--another example of a required process to utilize a particular technology path. While such losses may seem trivial given the small dimensions of the circuits, certain components such as delay lines and high-Q resonator structures need ultra-low loss to be used in practical applications.

Polarization effects and control

Losses are not the only important parameter in waveguides at the nano-scale. In many cases controlling the mode (polarization) of the transported waves is important, which can be manipulated with waveguide dimensions and with hybrid materials where the waveguide is composed of two materials with some of the light in one and some in the other. In general, the TE mode (polarization) has been favored in ridge waveguides used in silicon on insulator processes, while the other fundamental mode, TM is not. A very recent (November 2016) result published by the Institute of High Performance Computing (Singapore) used silicon slot waveguide to eliminate the polarization dependence of the waveguide performance. The authors note that the behavior is very sensitive to fabrication tolerances, but may be useful to work around the polarization issues of traditional silicon waveguides.

The majority of work that has been done has used the TE mode and single mode waveguides on Silicon Photonic circuits. This implies that light coming into a Silicon Photonic transceiver via a fiber and having arbitrary polarization needs to have the un-favored mode converted before it is routed around the PIC. A very common approach is to split the modes at the fiber-chip coupling point and convert the TM mode to TE in a separate waveguide. A range of work has been done on polarization management, involving mode converters and rotators as well as polarization selective splitters and combiners. Some recent work is highlighted below. It is worth noting that if a polarization modulation scheme is used, then it may be necessary to convert the un-favored mode then transport that light in parallel to the first mode--such schemes are often called polarization diversity. The important point is the PIC complexity is increased as in many sections there are then two features in parallel, complicating routing and generally increasing the size of the PIC.

Some work on polarization management and related factors includes:

- Compact, efficient, and polarization insensitive conversion between strip and slot waveguide in silicon-on-insulator systems (Peking University),
- Silicon waveguide TE mode converter using a tapered section above a rectangular section having length of only 5 μm (A*STAR),
- High bandwidth TE-mode pass polarizer using shallowly-etched straight optical waveguide,
- Multi-mode interference power splitters/combiners (Universidad Carlos III, U Politecnica de Valencia, Nanyang Technological University),
- Series tunable phase shifters and polarization rotators enabling selectable phase control with 40 dB extinction range in a technology independent fabrication design (Universidad de Málaga),
- Mid-infrared multimode interference splitter based on graphene plasmonic waveguide (Huazhong University of Science and Technology),

- Compact polarization splitter-rotator on silicon using an adiabatic taper, an asymmetric directional coupler (ADC), and a multi-mode interference (MMI) mode filter (Zhejiang University),
- Tapered directional coupler power divider (Huazhong University of Science and Technology),
- Nanotaper integrated with polarization rotation for efficient edge coupling to fiber (Cisco),
- Grating assisted coupler with low insertion loss and increased tolerance to manufacturing variations (Shanghai Jiao Tong University),
- Subwavelength Grating (SWG) TE pass polarizer of compact size (60 μm long) (Carleton University),
- Coupling arbitrary polarization into preferred TE mode using a grating coupler and MZI (University of Toronto),
- Polarization independent silicon-on-insulator slot waveguides (Institute of High Performance Computing), and
- A fabrication friendly SiN polarization rotator employing Augmented Low-Index-Guiding waveguide mode which is robust to SiO2 cladding (University of Toronto).
- Polarization beam splitter using polarization selective grating couplers on two silicon waveguides (Shanghai Jiao Tong University),
- Polarization sensitive directional couplers forming a polarization beamsplitter with broadband performance (University of British Columbia),
- TE pass polarizer using transparent conducting oxides (TCOs) (Southeast University (Nanjing),
- Interlayer Polarization Beam Splitter Based on Asymmetrical Si Wire Directional Coupler (National Institute of Advanced Industrial Science and Technology),
- Arbitrary polarization (fiber) conversion to TE via a 2-D grating coupler and two 3 dB splitters and two 3 dB combiners (University of Toronto),
- Cascaded long-period waveguide gratings mode converters with up to 90% conversion (City University of Hong Kong),
- Polarization Splitter-Rotator with low loss of -0.11 (TM to TE) using 90 degree bends in silicon waveguide (A*STAR), and
- Compact broadband polarizer based on shallowly-etched silicon-on-insulator ridge optical waveguides (UC Santa Barbara).

Although Silicon Photonic PICs are small in general, there are still considerations for further miniaturization to enable denser integration and maximize use of wafer area. We note that the work above by Nanyang Technological University, Universidad Carlos III, U Politecnica de Valencia, Southeast University (Nanyang), Zhejiang University, and others working with multi-mode interference offers promise of significant size reduction.

Optical power loss challenges

Another consideration are the losses associated with both transporting the light and additional losses when the waveguide has a bend. Bends are essential to route the light in a way to keep the PIC small and maximize wafer utilization. However, bends incur losses especially for the TE mode in ridge waveguides. The reason is that the mode distribution in the waveguide results in lower effective index of refraction contrast ratio in ridge waveguide (i.e. the index of refraction effectively of the waveguide, vs. the index of refraction on either side, either air or SiO2 in most cases) on the sides allows light to leak. These losses can requires some other approach to

overcome the losses, such as adding amplifiers to the waveguides to boost the signal. The latter obviously increases complexity and possibly cost, as well as other issues as noted in the light source section (in general amplifiers and lasers will require similar materials and integration). Some recent work by VTT Technical Centre in Finland using a novel conversion from ridge to strip with grooves on both sides and using Euler curvature has demonstrated 180 degree bends below 2 μm having less than 0.1 dB loss.

Approaches using small size and even subwavelength features in silicon waveguide systems are also showing interesting and promising results. Examples include:

- Small footprint (4.8 μm × 4.8 μm) power splitter designed using binary swarm optimization which, although having higher insertion losses than other designs, show unexpected performance uniformity across wafers even when design rules were violated, and point towards future size reduction and optimization.
- Subwavelength grating-based 3dB power splitter using two adjacent variable width gratings in the waveguides (University of British Columbia),
- Frequency selective subwavelength grating filters (McGill University), and
- Plasmonic waveguide using and Al/Si/Al system (NTT Device Laboratories),

among others.

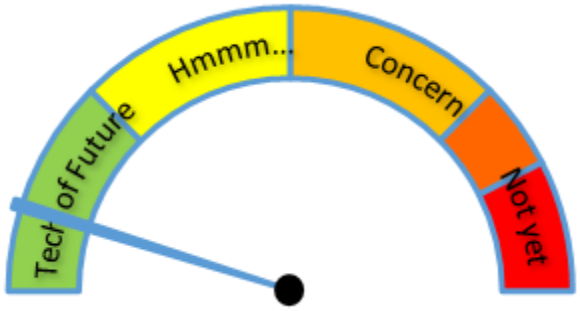
Silicon is not only a useful optical material but it has high thermal conductivity and large thermal coefficient of expansion. These properties enable tuning of waveguide features using heaters to change the temperature of a feature, such as a microring resonator, thereby altering its dimensions and thus the frequency of operation. Metal heaters of various materials such as Ti and Cu are commonly used; however there is a strong interaction between the light at the boundary of silicon waveguides and metals, resulting in high losses. This latter behavior limits how close the metallic heating element can be to the target device; typically an insulating region of SiO2 is used between the heating element and the device, which slows response time and consumes excess power. Graphene appears to be a promising material that can be used as a heating element without the limitations of traditional metals. Some work in this area includes:

- Graphene heaters to tune various features more effectively than metal heaters resulting in faster response times and lower power consumption for modulators etc. (AMO GmbH),
- Transparent graphene heater in direct contact with a silicon microdisk resonator (Zhejiang University),
- Transparent graphene heaters used for tuning in Silicon Photonic circuits (AMO GmbH), and
- Simulation and design of graphene-silicon-silica systems including non-linear behaviors (University of Tokyo, National University of Defense Technology).

We do not see waveguides as a concern for Silicon Photonics, but as with other building blocks there may be improvements in the future. However, there are many design tradeoffs including some that relate to choice of material or process, so designs will continue to evolve. It is also important to note that manufacturing tolerances are important to the performance of Silicon Photonics PICs, and this could impose limits to effective application of some designs. Even the side-wall roughness of the waveguide features, formed using photolithography, has a strong impact on waveguide losses, and the roughness depends on the process, materials, and

targeted geometry. One area of interest is the use of plasmonic behavior versus pure photonic behavior. There are cases studied where plasmonic devices may offer even further light confinement and miniaturization. Plasmonic waveguides differ from photonic waveguides and have different tradeoffs.

Photo-transduction



Risk meter for photo-transduction. Silicon germanium detectors are well developed and the most likely route in the short term. However, there is ongoing development with systems such as InGaAs/AlGaAsSb and more exotic approaches such as graphene-based plasmonic detectors. Source: EAF analysis.

The building block photo-transduction, also known as photodetection is in good shape with various strategies using Ge to make detectors with adequate properties, and more recently using Graphene. This component is needed in the receiver part of a link to translate light back into electrical signals as well as being a useful detector for control purposes. Important properties of such a photodetector are that the response time is fast enough to handle the data rate, that the response is linear enough to not distort the signal, and that the signal to noise is high enough to handle small signals.

As early as 2007, Si-Ge detectors were the transducer of choice for either control or as the primary active element in a receiver. In 2007, IME Singapore demonstrated that using tensile-strained Ge a detector could be made in a CMOS platform. In 2008, Intel (along with many co-collaborators including Numonyx (later Micron), UC Santa Barbara, and the University of Virginia), published results for an avalanche Ge photodiode (APD) with very high performance in terms of sensitivity and speed, thereby becoming an enabling technology for Silicon Photonics receivers. By 2010, UC Santa Barbara and Intel had roughly doubled the performance, realizing Ge-Si APD monolithically grown on silicon with performance in the range of III-V discrete APDs at 1000s of times lower cost.

Beyond Si-Ge APDs

There is nonetheless ongoing work in this area. Some other potential solutions are:

- Monolithic selectively grown Ge-on-SOI PIN mesa photodetector in a Si-CMOS process (A*STAR),
- Monolithically grown germanium/silicon avalanche photodetector (Singapore Institute of Microelectronics, Intel et al.),
- PbTe and PbTe/SnTe thin films lithographically patterned for mid-IR photodetection (MIT et al.),
- Graphene/h-BN/GaAs sandwich diode (Zhejiang University),

- Dual-fed traveling wave photodetector (Alcatel Lucent),
- Suspended membrane silicon/graphene waveguide photodetector with responsivity from visible to infrared (Chinese University of Hong Kong),
- Graphene-Boron Nitride Photodetector (MIT et al.),
- Silicon waveguide integrated metal-doped graphene junction photodetector (Columbia University et al.),
- Ge hybrid photodetector with gold-wire parasitic inductance using wire bonding (Huazhong University et al.),
- Low-voltage Ge waveguide avalanche photodetectors (Ghent University-imec et al.),
- Graphene SiO2 silicon photodetector covering all optical bands (Vienna University of Technology et al.),
- Silicon nanowire phototransistors via plasmon-enhanced two-photon absorption (University of Michigan),
- Using MoS2 in various configurations (Australian National University, and others),
- Amorphous silicon nanowires (University of Waterloo),
- Waveguide coupled silica microtoroid resonators (which would be coupled with detectors) (RWTC Aachen),
- InGaAs metal-semiconductor-metal photodetector integrated with grating coupler (University of Tokyo),
- MoS2 photodetectors enhanced by graphene quantum dots (Soochow University),
- Single-layer graphene deposited on defect-free Ge islands grown on silicon nanotips (IHP Germany),
- CVD grown graphene on Silicon Photonic waveguides with detector performance to 50 GHz (AMO GmbH),
- Photonic crystal nano-photodetector that eliminates an amplifier and lowers power consumption (NTT),
- Silicon waveguide Si-Ge avalanche photo-diode (APD) with operation at 25 GHz (Hewlett Packard),
- Asymmetrically doped wafer-bonded Ge/Si heterojunction photodiode (Tyndall National Institute et al.),
- Lightly doped Si/SiO2-graphene photodetector with fast (400/760 ns rise/fall response (Southeast University, Nanjing), and
- All-silicon photodetector based on microring resonators with zig-zag p-n junctions (State Key Laboratory on Integrated Optoelectronics, Institute of Semiconductors),

to name a few.

In general, the Ge-Si systems are most widely used. There is, as in other functions, considerable interest in other materials, including graphene, perovskites, MoS_2, boron-nitride, and telluride compounds. The last work in the list is noteworthy in that the researchers demonstrated a detector without other materials, which is easy to implement in CMOS.

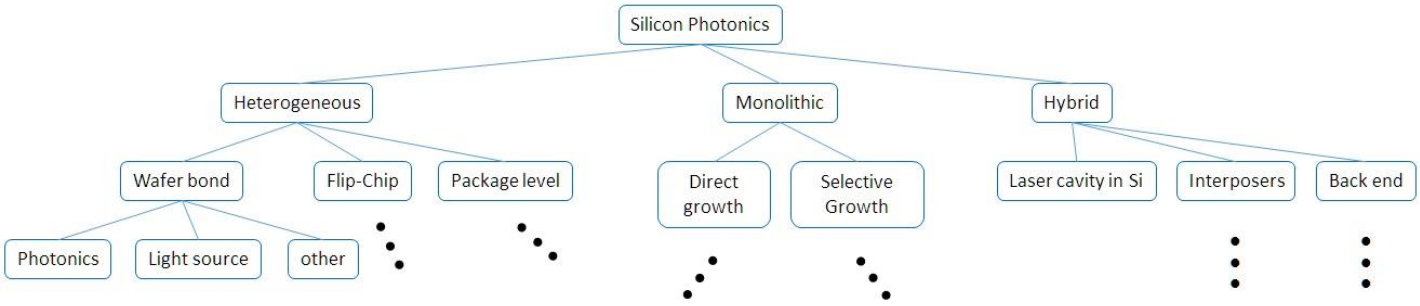
While this building block is likely to continue to evolve, we don't think this is a barrier, and changes will be largely transparent to the end-device performance.

Assembly/Packaging

Risk meter for packaging and assembly. The higher risk in this element is due to the unique processes required to integrate gain materials into the Silicon Photonics platform. At present, heterogeneous integration of some form is used to integrate III-V based light sources. These steps add new and different processing into the fabs, raising costs and investments. The likelihood that early solutions will prove to be the best solution in terms of manufacturing seems low. In addition, yields could be an issue--consider the Intel delay in shipping first samples as a warning flag. Source: EAF analysis.

In the course description for a 2016 Packaging workshop hosted by the University of British Columbia it states "Packaging is viewed by industry as the single biggest technical hurdle to overcome to enable the successful commercialization of silicon photonic integrated circuits." This theme has been echoed in other reviews, such as the recent "Roadmap on Silicon Photonics" review from a group of 9 leading industry and academic players. Those authors state "The cost of a silicon photonics product is dominated by its packaging costs, a significant part of which comes from fiber attach." Six years earlier, a paper from MINATEC® said "The target for CMOS photonics-packaging architecture is to get closer to the microelectronic industry model, i.e., around 20% of the overall cost for packaging." Existing telecom photonics interconnects are high-cost compared to the targets for Silicon Photonics, and a significant part of that are labor intensive and complex packaging processes. In those cases, the value of the products, derived significantly from the huge advantage of fiber optic over copper at long distances, provides room for such costs. If Silicon Photonics is to deliver on the promise, these costs must come down.

Packaging is used to refer to several processes necessary to complete a finished product for sale. In the case of Silicon Photonics, for anything other than purely monolithic integration, it includes additional steps in certain cases due to the choice of heterogeneous integration method for the optical gain medium (e.g. laser, etc.). Logically, all of these aspects can be considered in a tree diagram describing the options to make an IPE device:



Source: EAF

In reality there is more complexity and deeper levels. Regardless, the above only addresses the main process legs wherein the core electronics and photonics capabilities are manufactured. However, for IPE devices, there is at least one additional consideration. For example, considering interconnects used in data centers, the IPE components are typically integrated to a package that provides fiber integration, thermal management, and electrical integration. Further downstream, the IPE and processing and communication chipsets are integrated to boards along with connectors (and a host of other components) or some interfaces to the electronics and IPE, and these are then integrated to other server functionality (memory, storage, etc.), and finally optical cables interconnect to switches etc. In some cases the cables are so-called Active Optical Cables, but that isn't important to understand packaging. AOCs require most of the steps described and then present an electrical interface to the server side and an optical interface to the switch etc.

Adding IPE devices to the framework described so far necessitates that the optical signals be connected from the chipsets having the photonic functionality to fiber optics, and those fibers integrated to a (passive) connector. From there, passive optical fiber cables can be used to connect to the switches etc. Note that the above depiction addresses only the use of IPE for data center interconnections. IPE has likely application to chip-to-chip, board-to-board, and other permutations. Nonetheless, the main "new" as compared to conventional electronics are the choice of photonic packaging and integration from chip to fiber. Even so, there are many possible approaches. We cover more details of the chip-to fiber packaging in the next section; here we review the integration/packaging needs for the chipsets.

For some time in Silicon Photonics development the long-term goal was to intimately integrate the data processing and control electronics (processor, various active electronics, passives, etc.) with the photonics (light source, modulation etc.) thus having optical signals entering and leaving the device, which would also have at least power connections and thermal management. That goal seems to waver in recent discussions, where criticisms are raised of the need to use older electronic device nodes (e.g. 40 nm CMOS) to integrate with the necessary thick oxide lasers and other features needed for the photonics layers. Other issues are noted for monolithic laser integration to CMOS/Silicon Photonics as well. One could also logically separate the most needed control electronics for a Silicon Photonics package, and try to integrate those. Recent work by imec has demonstrated, for example, flip chip assembly of a 40 nm CMOS chip onto a Silicon Photonics package. We can consider there are then permutations on our previous diagram among the now plurality of packaging choices, with the attendant increase in tree branches. PETRA (Japan) have also demonstrated a complete packaging approach integrating the electronics and Silicon Photonics components using flip chip assembly of the CMOS package to the Silicon Photonics package. PETRA also demonstrated a novel package to fiber integration using an optical pin between the fiber interface and the Ge photodiode.

Regardless of the additional choices, the short term goal is to integrate photonic components into a silicon platform for size, cost, and energy use reduction. Along this continuum the next step might be considered either monolithic integration of the laser or integration of the photonic circuit with the electronics. Since there are some solutions in the market heterogeneously

integrating a laser with a silicon photonic circuit, that can be considered "a line in the sand" for reference of further developments. Here we look at the packaging options in this continuum.

Over 10 years ago there was excitement over the achievement of a silicon Raman laser. However that path fell by the wayside and in more recent times a range of technical solutions each with particular packaging needs for a light source have been pursued. These range as:

1. Fully heterogeneous whereby a complete laser is built and integrated: includes assembly of a laser micro-bench with late step integration to the Silicon Photonics, and creation of a III-V laser stack with an included mirror to direct light into the Silicon Photonics,
2. Monolithically integrated III-V quantum well and quantum dot lasers grown on silicon: include a number of approaches sometimes using extra layers to "buffer" the lasing stack again dislocation fractures caused by excessive stress due to crystal lattice mismatch,
3. Other heterogeneous hybrid schemes: includes a variety of approaches bonding III-V material to the Silicon Photonics, which involve a bonding step then additional processing; also includes a range of flip-chip assembly approaches to leverage existing IC assembly capabilities,
4. Homogeneous/Monolithic: includes various techniques to selectively grow III-V material and get around defects or to grow other materials such as group IV alloys (such as Ge-Sn) and engineer them to have a desirable band gap,
5. Other "exotic" heterogeneous approaches including semiconductor tubes, carbon nano-tubes, and others, which involve extra steps to integrate the nano-tubes and connect to/drive them, and
6. Schemes using a secondary substrate to integrate processors, electrical control, and silicon photonic chips, with both electrical and optical substrates used, sometimes called interposers, and sometimes called 3D integration,

among others.

Note that from a packaging viewpoint, 2-4 are essentially equivalent in that they result in gain material into the stack, and 1-5 are more or less equivalent in that the entire photonic package including the light source is on one chip. From the assembly of a laser and lens into a tiny sub-package or micro-bench, then assembling that onto the Silicon Photonics as perhaps the most complex, to the monolithic growth approaches, every option has tradeoffs and impacts.

Beyond the light source implications for packaging, there are a variety of "paradigms" if you will regarding the correct approach to integration in finished devices. These mainly address what is the best platform for the light source, the photonic integrated circuit, and the integration of control electronics. The issues include the fact that microprocessor fabrication is now done in very small node size, 14 nm with 10 nm launched, and 300 mm wafers, heading to 450 mm in the next few years. In contrast, Silicon Photonics has requirements that have limited it to fabrication with only 65 nm or 40 nm CMOS. *The reasons are technical, but it is unlikely in the next 5 years that Silicon Photonics can be monolithically integrated with state of the art CMOS. This gives weight to the argument that the Silicon Photonics and electronics should be integrated after fabrication.* Various approaches are proposed such as integration of electronic dies to Silicon Photonic wafers, using flip chip/solder bump technology. ST Microelectronics has demonstrated an approach of this sort on 300 mm wafers, as well as considering a roadmap for the back end

processes. imec has also demonstrated integration of 40 nm CMOS with Silicon Photonics in this way.

III-V integration additions to CMOS flow

The group of approaches bonding entire or parts-thereof of III-V wafers to the CMOS wafer while conceptually simple, they all involve an additional part flow into the CMOS fab. However, the operations have generally been qualified in existing high-volume so the risk there may be relatively low. The issue with these processes is the addition of some degree of alignment to the manufacturing needs. Although alignment also is not a stranger to microelectronics manufacturing, it raises costs and possible yield and quality issues. We note that Fujitsu, for example, has recently demonstrated flip-chip bonding of SOAs (semiconductor optical amplifiers) at sub-micron tolerances and shown they meet the needs of an integrated assembly. This follows on to Fujitsu's earlier and ongoing efforts using flip chip assembly. Arguments are made on all sides about which is better; for example the mounting of coupons versus wafer bonding is held as lower risk as a contaminant causing poor bonding in one part of the III-V wafer doesn't affect the rest. Wafer bonding critics also point to the fact that III-V wafers are not available in the sizes used in many CMOS fabs, leading to other costs--this fact also supports hybrid or heterogeneous integration (hybrid in this case meaning adding small stacks of III-V material to a Silicon Photonic wafer) as the best choice. Perhaps the least alignment sensitivity comes from a process that forms the laser cavity in lithographically produced wells in the CMOS wafer before the III-V material is added, then finished. Nonetheless all of these have potential pitfalls.

Group IV lasers

The processes striving for group IV lasers (silicon is a group IV material, but as noted variously elsewhere, it does not have a bandgap structure allowing efficient light generation) are interesting and some are promising, but these are a long way from commercialization. Similarly, the team at UC Santa Barbara has recently published some reliability results of InAs/GaAs QD lasers on silicon, stating "devices maintain lasing oscillation after more than 2700 h of constant current stress", but more work is needed to validate reliability at the levels needed for commercial products. University College London has reported over 3100 hours operational data collection in a similar approach, and calculates MTTF over 100,000 hours.

Monolithic solutions (with additions to CMOS flow)

The group of approaches attempting in various ways to monolithically grow a gain medium or device on a CMOS wafer, are to some extent all trying to get around a difficult challenge trying to merge III-V photonics materials with CMOS--the crystal structures and thermal properties do not match, so the materials develop defects which degrade or block performance. It is evident that adding additional layers adds cost to the process, so while buffer layer approaches are interesting, they may not see commercialization. Also, the QD approaches that require assembly bring back into play the concerns around alignment, cost, etc. as well as potentially new issues. Various groups are working on self-alignment schemes, notably IBM has demonstrated a high volume process using flip chip assembly of the light source with self-alignment. The monolithically grown QD approach has been demonstrated to generate good light sources even with post-growth flaws, in part because the QDs are so localized they can

operate even with flaws in nearby material. Nonetheless, it is important to maintain perspective that new developments from the Universities may require years to be produced, if ever.

In general, the back end processes such as adding thermal management, integrating fibers, etc. are not dramatically different from those of existing optical assemblies. However, there are a myriad of possible ways to do the final integration, most of which depend significantly on the packaging and integration achieved with the Silicon Photonics wafer. There is work ongoing here, but we don't consider this a major obstacle, other than chip to fiber coupling which we discuss in the next section. The real concern here is cost; depending on the design there may be time/labor intensive steps here; in some approaches active alignment of some components may be needed (such as the fiber interface) so those need to be avoided or further developed to lower cost.

There are two groups of particular note that have put considerable and important work into the open literature in these other packaging steps, IBM and Tyndall National Institute. In an August 2016 paper, IBM noted: "Silicon photonics leverages microelectronic fabrication facilities to achieve photonic circuits of unprecedented complexity and cost-efficiency. This efficiency does not yet translate to optical packaging, however, which has not evolved substantially from legacy devices. To reach the potential of Silicon Photonics, we argue that disruptive advances in packaging cost, scalability in optical port count, and scalability in manufacturing volume are required." The authors then go on to describe their novel process. The main steps of that are to use a standard cleaved fiber ribbon array and etched v-grooves in the Silicon Photonic chip to align the fibers. As noted earlier IBM has also demonstrated passive alignment of light sources assembled to the Silicon Photonics using flip chip assembly.

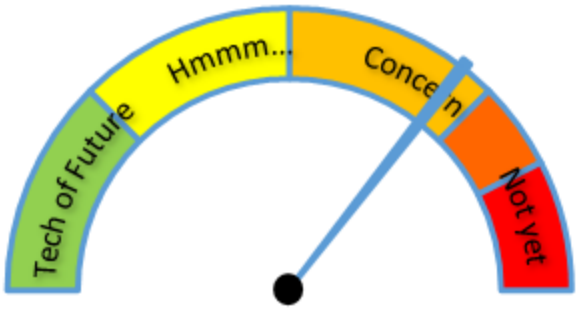
Tyndall National Institute has a Photonics Packaging Group and a dedicated Photonic Integration Laboratory. The Institute is also integrally involved in the EU PLAT4M program which includes photonics packaging development as part of its mission. Among other innovations, Tyndall has developed a method to polish fibers, including a fiber ribbon array, at a 40 degree angle, which acts as a mirror to reflect light from the chip to the fiber core. The 40 degree angle is due to the use of grating couplers which couple the light out of the silicon waveguide and typically exit the light at a 10 degree angle from perpendicular, and 40 degrees achieves total internal reflection down the fiber axis. Tyndall's chip to fiber coupling scheme notwithstanding, in a December 2016 review by Tyndall of the state of the art in photonic IC packaging, the authors conclude "The packaging of a photonic device is often the most expensive element of the overall module fabrication, and can involve major technical challenges that need to be addressed at the PIC design stage. Simultaneously satisfying the optical, electrical, and thermal design considerations for a PIC requires a 'joined up' approach that goes well beyond the most widely recognized issue of Fiber-to-PIC coupling." We believe that these challenges create additional barriers to entry of fabless Silicon Photonics designs, as not only would a design house need to find a suitable foundry, but also a packaging house capable of addressing all the complexities to realize a commercial product vs. a laboratory test device.

Elsewhere in this narrative (see: Test section) we discuss packages using interposers as a platform to integrate Silicon Photonics with other components. Recently (June 2016) MIT proposed a design whereby multiple vertically oriented SiGe photodiodes are integrated into an electronic

package and are illuminated by light exiting the Silicon Photonic platform, in such a way that the assembly alignment can be optimized via control of the differential electrical output of the photodiodes. The researchers demonstrated such a design in GlobalFoundries 45 nm 12SOI platform, and showed that nanometer scale alignment of the optical interconnect was feasible.

While not all the issues noted here are directly related to the packaging scheme, it should be clear that packaging and the underlying design are intimately related. These technologies are not just simple recipe elements to be used or not, which speaks to the low maturity level of Silicon Photonics as compared to microelectronics. Realistically, it will take 5 to 10 years for a stable set of packaging processes and design rules to be available to meet most needs for design houses. While the fabless model has been successful in semiconductor manufacturing, this has been in some degree due to standardization of processes. It stands as a corollary that although there is a high degree of fabless design effort going on in Silicon Photonics (due to the high cost and limited availability of qualified production lines) this does not imply a mature industrial state. On a more positive note, complete integration using secondary substrates as well as optical pins as interfaces have been shown successfully very recently by PETRA in Japan and Fujitsu, and NTT very recently (January 2017) demonstrated optical through hole vias allowing 3D integration of Silicon Photonics with electronics.

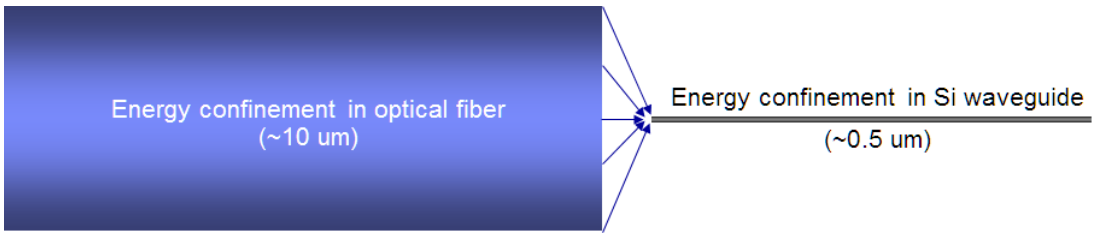
Chip to fiber coupling



Risk meter for chip to fiber coupling. We conclude there is significant risk in this block for several reasons. First, any solution need to be proven in high-volume to assure that problems in this step do not outweigh the benefits of building IPE devices in CMOS fabs. IBM and Intel have demonstrated viable approaches, but until volume production there is risk of issues arising. Second, there is some ongoing development which could lead to lower losses and therefore be advantageous to use in future designs. Third, there are two fundamental approaches at present: some form of vertical grating coupler, or some form of butt coupling. The latter mainly uses lensed fibers due to the significant difference in mode size of the silicon waveguides vs. the fiber. Eliminating the lens as well as reducing assembly tolerance would be a significant step. Further, horizontal butt coupling forces functional test to occur after dicing, adding test complexity and yield impact multiplication. Vertical grating couplers in principal allow wafer level testing of the active and passive parts of an IPE device. However, insertion losses are higher than desired at present. Very recent work (November 2016) by ETRI (Korea) demonstrated lower losses and higher alignment using an optimized coupling using a thin film filter. Source: EAF analysis.

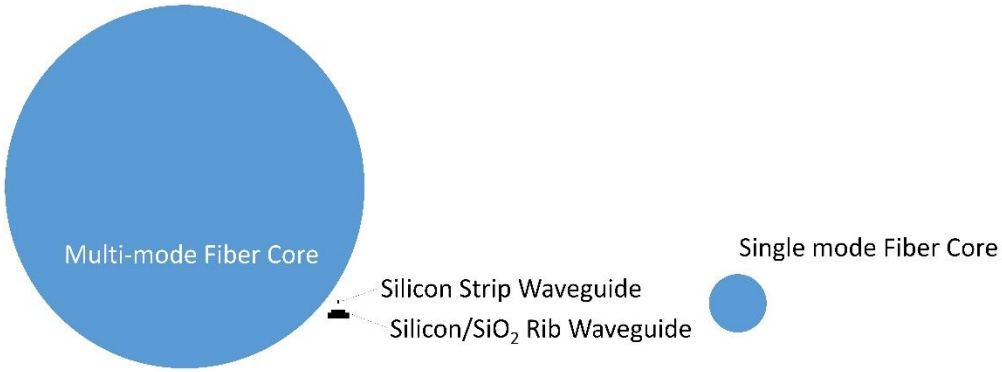
If Silicon Photonics chipsets become as ubiquitous as microprocessors, it will only be if very robust solutions are found to get the photonic signals from the chips to fiber and to connect fiber to fiber (in the data center). In fact it is required to connect to many fibers in a very small space. If

we take 25 Gb/s per fiber as the current benchmark, then 16 fiber-chip interfaces are required for a 400 Gb/s transmitter. If the transmitter (Tx) and receiver are integrated in one chipset, 32 interfaces are required. Now consider the dimensions involved. Depending on the design the chip-level waveguide can have characteristic dimensions from 100s of nm to a few µm. Single mode 1310 nm fiber has core dimensions of 8-10 µm, multimode fiber around 50 µm. The following diagram shows the challenge of getting light from a single mode fiber to a waveguide in a Silicon Photonics circuit. In order to minimize losses, so-called spot-size converters are needed. Misalignment increases loss for the interface.



Source: IBM, used with permission

Alternatively, consider that different waveguide types have different sizes; an embedded Si waveguide is much smaller than a ridge waveguide. In either case, launching into multi-mode fiber presents even more challenges:



Comparison of fiber optic dimensions to waveguide dimensions. Source: EAF.

To couple from Silicon Photonics chips to fiber optics requires transitions, sometimes referred to as mode converters, spot size converters, and other terms. Without these transitions, especially on the receiver side there could be very high losses. Even with properly designed transitions, many issues remain, largely due to needing precise alignment of the fiber optic cores to the mode converters. Further, as noted earlier, since Silicon Photonics promises to reduce the footprint of photonics, a multi-channel transceiver will involve many fiber to chip interfaces, which must somehow be connected to the data center cabling.

To address this, some of the largest proponents of Silicon Photonics technology, including IBM and Intel, have both offered parts of the solution. IBM has shown two options for getting the light off the chip--a flexible polymer waveguide "to mechanically decouple the ferrule from the chip and avoid thermo-mechanical reliability issues such as fiber pistoning and other chip-package interaction" and a direct fiber-to-chip method. The former has worst-case losses of -2.4 dB while

the latter achieves -1.3 dB. IBM concludes that these methods are suitable for existing micro-electronic packaging facilities.

A number of other schemes to integrate Silicon Photonics to fiber optics have been proposed using various types of grating couplers. Some alternatives include:

- Clarkson University: Vector Mode Grating Coupler,
- Universitat Politecnica de Valencia: Sub-mount carrier tilting the integrated photonic package so that angled grating couplers align with horizontal fiber arrays,
- Zhejiang University: inverse taper multi-mode coupler,
- Harbin Institute of Technology: Sub-wavelength-grating slab waveguide structure,
- imec: Compact metal grating coupler using polysilicon overlay ,
- Chiral Photonics/McGill University: Pitch reducing optical fiber array (PROFATM),
- Institute of Semiconductors (Beijing): Curved gratings with non-uniform pitches,
- Kotura: 3D tapered mode transformer,
- Peking University: High-performance compact fiber-to-waveguide, binary blazed subwavelength grating coupler in SOI,
- A*STAR: Suspended tapered SiO2 waveguide and centrally located overlapped Si nano-tapers,
- Tyndall National Institute, A*STAR: Planar fiber to vertical grating coupler with angled fiber polish and passive alignment using vision systems,
- KTH-Royal Institute of Technology: Apodized grating coupler requiring only one lithography/etch step,
- MIT: Adiabatic two-stage in-plane coupler using a rib taper mode size reducer coupled to an inverse taper to couple into silicon waveguide,
- Cisco: Polarization Multiplexing Nanotaper coupling,
- National Tsing Hua University: Combined 3D SU-8 taper and opposite silicon nanotaper butt coupler, providing a +/- 3 μm alignment tolerance and 2.8 dB (TE) and 4.1 dB (TM) insertion loss,
- California Institute of Technology: Nanoscale silicon photonic crystal opto mechanical cavity fiber coupler with in-plane coupling between tapered fiber and opposite adiabatically tapered silicon waveguide, providing 85% total coupling efficiency,
- Technical University of Ostrava: Lensless fiber edge coupler with large mode size using high-index Si3N4 layers in SiO2 (SOI),
- Luxtera: Loss Polarization Splitting Grating Couplers,
- Université Paris Sud: Uniform, apodized, and focusing subwavelength fiber-chip grating coupler implemented in 220-nm thick SOI with efficiency of 56% and potential for 89% with backside metallization,
- Université Grenoble Alpes: Co-integrated bonded III-V laser and silicon Mach Zehnder modulator operating at 25 Gb/s,
- Harbin Institute of Technology: "Barcode" grating designed using numerical optimization using modified direct search which overcomes the off-perpendicular requirement of standard grating couplers, and
- ETRI (Korea): A receiver optical sub-assembly (ROSA) with large (25 μm) coupling alignment tolerance, using a thin-film filter at the fiber-chip interface and novel vertical electrical interconnect.

In these approaches the grating is formed in the chipset and the fiber is integrated in a vertical or angular-coupled configuration. Typical losses have been reported in the -2 dB to -3 dB range, but most have not been tested as rigorously as the IBM work. We feel there is significant risk in this area that can be mitigated by taking the results of the most promising academic studies and demonstrating them in a production-similar system and showing the results in terms of statistical distribution of alignment and losses. It is likely that the integration to fiber optics will be done by either the end product manufacturer or upstream at a sub-board assembly process or possibly upstream at the chip level. It seems unlikely then that wafer-level fiber integration is feasible--in other words, chip to fiber integration is a process limiting step. There are packaging specialty houses available today but not operating at the volume expected (or hoped) for Silicon Photonics. The risk is that difficult assembly processes may not scale, and could multiply costs negating some or all of the cost benefits pursued by Silicon Photonics.

Perhaps not obvious from the above, but some coupling schemes use a lens as part of the spot size conversion. While conceptually simple, adding the intervening component does raise cost and adds another tolerance to the assembly. It is also not possible to add a component in the optical path without some loss. As noted already, typical losses are in the 3 dB range. There are approaches that may offer significantly less loss. For example, in 2006 Kotura (now Mellanox) showed a mode converter that reduced losses to 0.3 dB. More recently, Zhejiang University reported similar results in a multi-mode converter, which is useful if multi-mode fiber is used for the interconnect. Part of the alignment challenge is that coupling from grating couplers and lensless schemes have limited angular tolerance.

Another factor we have noted elsewhere is that the "vertical" grating coupler approaches in fact require the fiber to be 10 degrees off the perpendicular axis for maximum coupling. This presents additional manufacturing challenges. Interestingly, as noted in the modulation section, the Institute of Semiconductors (Beijing) showed in 2013 a unique bi-directional grating coupler that was vertical, and combined the function of a modulator as well, but we have not seen that approach pursued further. The Chiral Photonics design noted above, as well as work by Tyndall National Institute, have achieved off-axis couple of fiber arrays, which is what is needed for most practical applications. However, the work by Harbin Institute of Technology offers a solution, creating a so-called barcode-like grating optimized using numerical methods to create maximum coupling in a true vertical orientation.

Tyndall National Institute has developed over several years a unique method where a vertical grating coupler is coupled to fiber in the plane of the chip, by polishing a fiber array to an angle that reflects light coupled from the grating into the angled, polished surface of the fibers. Tyndall has studied the assembly tolerances and shown that a passive alignment using standard vision systems can be used to assemble the array to the chipset, but the total insertion loss is higher than other methods, up to 9 dB. Nonetheless the Tyndall approach is studied and documented more than most proposals. A*STAR has also developed this approach, and added the process of laser welding the fiber to the IPE chip, eliminating the need for epoxy at that stage of assembly.

One interesting development recently shown by the National Institute of Advanced Industrial Science and Technology (NIAIST) in Japan was the use of Silicon-ion implantation to curve a

silicon waveguide resulting in vertical coupling to fiber with insertion loss of 3 dB for a lens-fiber system. The ion implantation creates stress which bends the waveguide. The advantage of this system is it eliminates most of the wavelength dependence of grating couplers, and achieves a bend radius as low as 3µm, thereby avoiding additional thickness in the design. Nonetheless, it requires special manufacturing steps to create a cantilevered SiO2 clad silicon waveguide beam, which is then curved by the ion implantation. NIAIST also showed, in a July 2016 paper, that a small section of SiN waveguide with a square 310 µm core integrated with tapered silicon waveguide could be used to more closely match the mode size in the optical fiber. Recently Luxtera reported on optimization of Polarization Splitting Grating Couplers (PSGCs) that could reduce losses to the 2d dB range from typically-reported > 3 dB. Another recent advancement was shown by Cisco, who used a coupler fabricated from nanotapered waveguides to decompose light from a fiber into two polarizations then rotate them to the TE mode which is more favorable in silicon waveguides, coupling the light into two silicon waveguides. This approach leads to overall lower losses.

Most edge-coupled systems, where the waveguide in the Silicon Photonics chip is brought to the edge and an optical fiber is butted directly against the chip (or, a lens is used on the end of the fiber, and that is against or near the chip), use so called spot size converters (SSCs) to reduce the mismatch of the mode sizes between the silicon waveguide and the fiber. We believe that an important drawback of edge-coupled designs is that test must be done at the die level (i.e. after the wafer is cut into the individual PICs) instead of wafer level. This increases test cost as well as process yield costs due to more added value in dicing and polishing before test which is lost for each bad die. Thus, while butt coupling fiber to the edge of a Silicon Photonics PIC may seem simple, it may not be the preferred production design. A number of interesting designs have been developed to perform spot size conversion to integrate fiber to the edge of chips:

- Inverse tapered waveguide providing ultra-low loss spot size conversion (< 0.4 dB) (NIAIST, Japan),
- Vertically stacked multiple tapered waveguide SSC (NEC),
- Tapered silicon wire with overlaid rib waveguide (MINATEC Institute),
- Si3N4 thin layer increasing effective refractive index at the junction facet, resulting in large mode size to couple without a lens (Technical University of Ostrava), and
- Spot size converter with SiO2 spacer layer between tapered Silicon and SiON waveguides, (NIAIST, Japan),

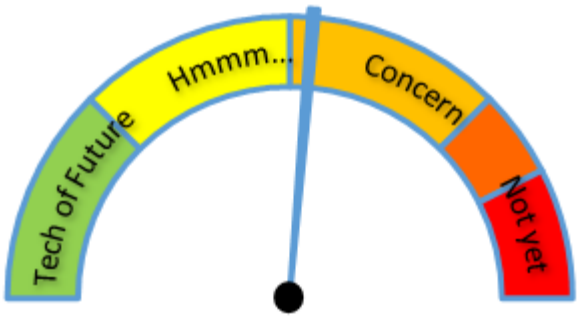
to name a few.

As noted elsewhere, polarization control must be addressed in practical systems. Recently (June 2016) the University of British Columbia showed a design wherein the random polarization from a single mode fiber is automatically converted into the quasi-TE mode of the Silicon Photonics chip. By using a Mach-Zehnder interferometer with two thermally controlled phase shifters the incoming light is all converted to the desired mode with minimal losses.

The fibers coupled to chips as above need to be terminated in a connector so that data center optical cables can be connected easily. In any realistic scheme, the chip to fiber coupling will be permanent and applied as a post-process to the core chipset. This results in a fiber array, likely planar (but not in all designs), exiting the chip/board. That array must be terminated in a

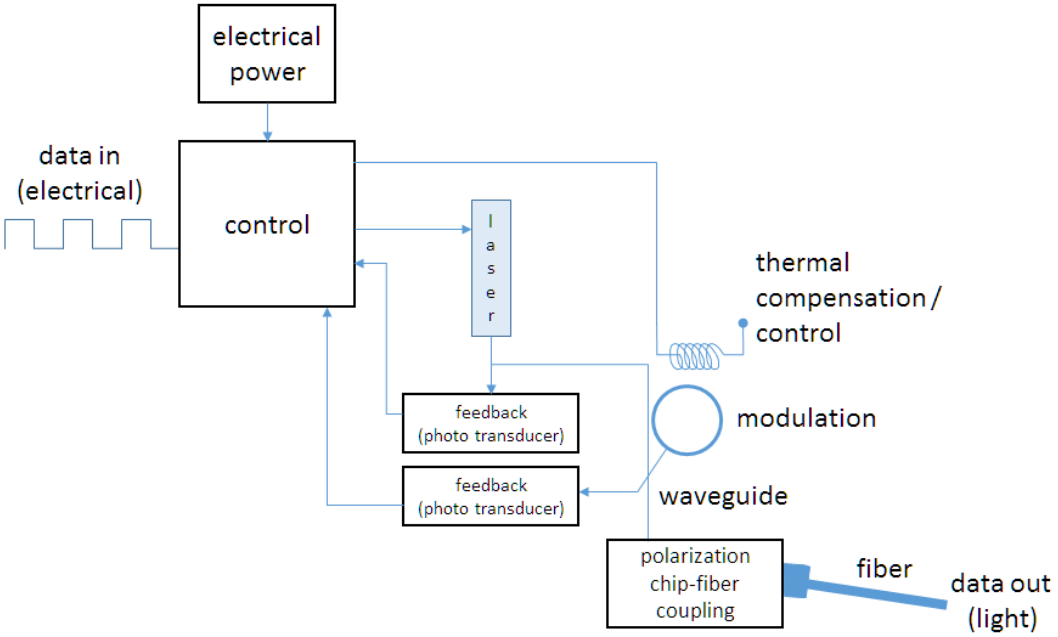
connector, and said connector will be mechanically strain-protected at the board level. This connector interface then provides the pluggable fiber interface to facilitate cabling in a data center. There are a wide variety of mature products for fiber interconnect in the market. Notwithstanding, Intel collaborated with Corning to address this key part of a Silicon Photonics interconnect scheme, namely a connector that can interface to a connector from a Silicon Photonics populated board in a server. The so-called MXC™ connector having up to 64 fiber interfaces was developed by Intel and Corning. The MXC design uses lenses in both connectors to improve performance and increase assembly tolerances. As part of the effort, a new optical fiber was developed as well, dubbed ClearCurve ®. The fiber, optimized for 1310 nm light, is stated to be bend-insensitive, allowing bends 10x sharper than other fiber. Corning has continued fiber development and recently published results regarding a fiber that can support 850 nm multi-mode and 1310 nm single mode transmissions. The new Corning fiber is intended to simplify cable management in data centers.

Control



Risk meter for control integration. We consider the risk here to reflect that the architecture is still very much in flux. A few groups have demonstrated full integration of processors and other electronics with Silicon Photonics. For a given application, full integration would be very desirable.

There are a number of different ways a Silicon Photonic device might be controlled, depending on the light source, modulation scheme, and thermal control needs. Schematically it looks like the figure here:



Simplified control diagram. There are multiple configurations for all the blocks. Frequency splitting of the laser into multiple channels (using so-called frequency combs or other methods) is not shown; in a complete system there would be likely 4 channels multiplexed to achieve the total throughput, multiplying much of the system by 4. The example shows thermal control such as might be used with micro-ring resonator-based modulators but there are other schemes as noted i the narrative. It may be possible to directly modulate the light source for some applications.

As already discussed, some embodiments seek to integrate the control electronics into the same chip as the photonics. In other cases, separate ICs are integrated in some downstream steps. While the case of an integrated light source is indicated, there are commercial devices where the laser may be external as well, and additional control features may be needed. In all cases, the concepts of the electrical control are already well known. Although not simple, controlling a Silicon Photonic-based transceiver is an extension of existing electronic systems. Thus, the main focus is on how and to what level to integrate the control electronics with the photonics package.

Test

Risk meter for test. The main sources of risk are integrating active photonic testing into the fab, and whether testing can be done at wafer level or not.

Test is complicated as compared to existing tests in CMOS processes for making integrated circuits due to the necessity to test the light source, control, modulation, etc. At a high level, there are existing in-process electrical tests the same as or similar to the existing fab knowledge base, then there are additional photonic/electrical tests that are needed. Further abstracting, it is needed to sample the light output of the device while applying known inputs. The light sampling may be at the wafer level or after dicing. Schemes that use vertical grating couplers can in principle be sampled at the wafer level. This has the significant advantage of providing closer feedback to the process and avoiding adding additional value to bad parts. Alternatively, schemes that integrate the laser as a separate component, made outside the Silicon Photonics process, push most of the photonic testing to the laser manufacturing process, Luxtera being a key example.

A further division of test requirements can be made depending on whether the electronics are fully integrated to the Silicon Photonics or are integrated later at the die level. One challenge for fully integrated designs is that the size of the Silicon Photonics integrated circuit is large compared to the necessary die-size for the control electronics. Thus, direct integration of Silicon Photonics with the control electronics, i.e. at the wafer level, gives poor electronic area utilization, driving cost up. This is indirectly indicated by the fact that the CMOS process nodes used to date to create Silicon Photonics are 45 nm up to 180 nm nodes.

One solution, as championed by Luxtera, is to separate the device into 3 sub-systems: Electronics, Silicon Photonics, and InP laser. In such an approach, there are two additional test steps required: testing of the Silicon Photonics (at wafer level) and testing the final assembly at the die level. The last step can be combined with the alignment/bonding step(s) but may also include additional test steps if, for example, an interposer is used in the assembly. Testing of the Silicon Photonics sub-component can be done at wafer level, using standard equipment with new optical probes. This has been demonstrated using 200 mm and 300 mm wafers and has acceptable throughput.

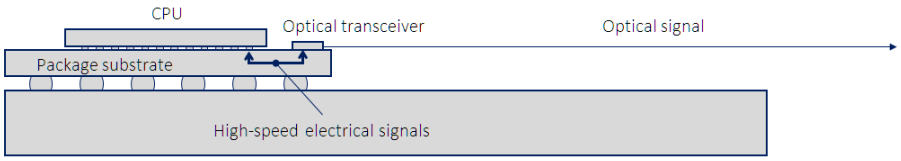
Regardless of the integration scheme, there is the necessity to test the photonic components one or more times in the process. Full integration is advantageous in this case because the entire system may be tested in one step, albeit with the limitations noted already. Assuming the Silicon Photonic functionality is made in a standard CMOS process, it turns out that the Silicon

Photonic device is a small fraction of the total build and test cost of the integrated device. Thus, if test yield is below target, the cost impact is multiplied for a fully integrated design. So, any issue with yield becomes a strong cost driver and impacts early-stage profitability.

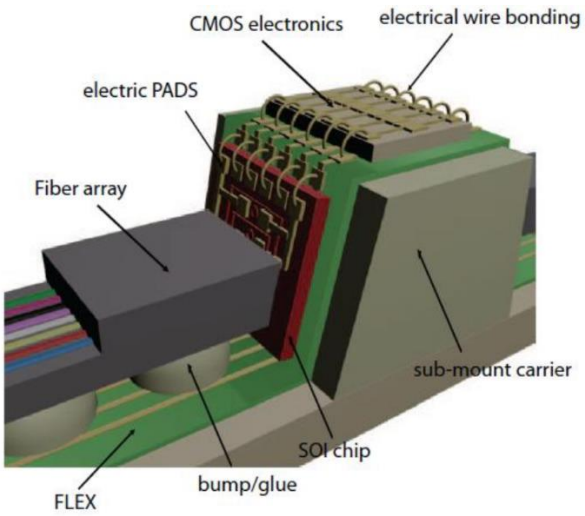
Alternately, a typical case involving sub-component integration would, for the photonic test stage, have 8 fiber interfaces closely spaced on the device. IBM has shown a process wherein the requisite number of parallel fibers are assembled into a standard ferrule, and the other cleaved ends are stabilized using a polymer "lid"; this assembly is then pick and place attached to the Silicon Photonic die. Alignment, within a tolerance of 40 µm is accomplished by etched "V" grooves in the die, Testing (final) can then be done via the ferrule.

In the IBM process, a secondary photonic die, comprising the active (III-V) light source, is bonded to the Silicon Photonic die, using self-alignment features. Thus, in one process the light source is made in III-V material, and tested at the wafer level, then diced and prepared for integration using standard microelectronic flip-chip methods. The silicon photonic component is made in a standard CMOS line and tested at the wafer level. The secondary III-V dies are flip-chipped onto the Silicon Photonic wafer and self-aligned using solder surface tension forces and a butt optical interface. This hybrid wafer may then be tested at the wafer level as well. Part of that test is to ensure the self-alignment step is correct, including in particular that the insertion loss of the junction is within tolerance. Lastly, final test after dicing is needed to verify the fiber alignment. The total process, then, comprises multiple test steps including at least 3 stages of optical testing.

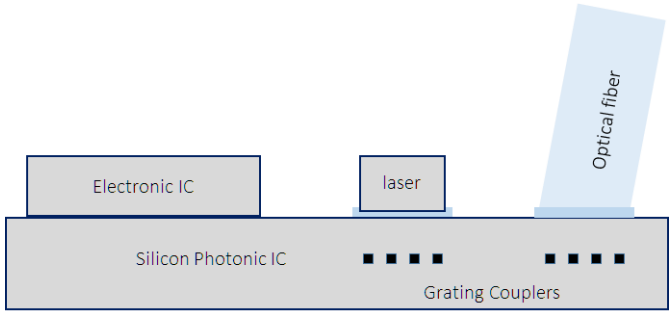
Fujitsu has shown a complete integration including a CPU, optical transceiver, and a package substrate that presents a standard BGA interface to a circuit board. In such a design, the optical package includes the Silicon Photonics with light source, and those packages are flip-chip bonded to the substrate which has the electrical interface to the package. The control electronics/CPU is flip chip attached to the same package substrate, which includes electrical interface through to the lower BGA interface. Thus, a final test step verifies the complete photonic package ready to assemble to a server board, for example.



Integration scheme using a secondary package to integrate the control, logic, and power with a Silicon Photonics package. Adapted from Hayakawa Akinori et al "Silicon Photonics Optical Transceiver for High-speed, High-density and Low-power LSI Interconnect", Fujitsu Sci. Tech, Vol. 52, No. 1, pp 19-26 (January 2016).



Packaging scheme proposed by Universitat Politecnica de Valencia and Technische Universitaet de Berlin that allows wafer-level probing from above but results in a horizontal final packaged geometry. (from: Galan, J. V., et al. "Low Profile Silicon Photonics Packaging Approach Featuring Configurable Multiple Electrical and Optical Connectivity" Group IV Photonics (GFP), 2011 8th IEEE International Conference on (14 Sept. 2016): 377–379.)

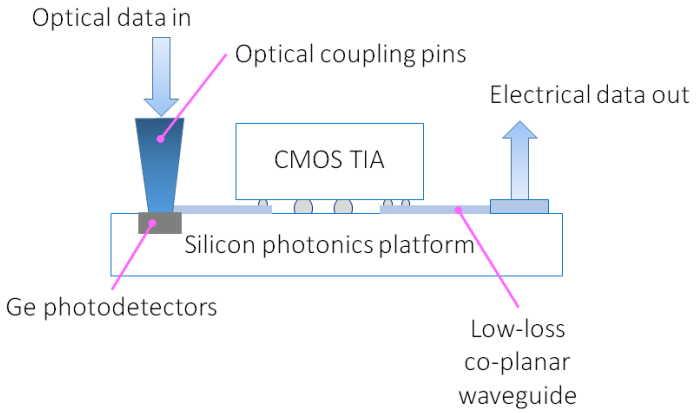


STMicroelectronics packaging approach. Adapted from Boeuf Frederic et al "Silicon Photonics R&D and Manufacturing on 300-mm Wafer Platform", Journal of Lightwave Technology, Volume 34, Issue 2, pp 286-295 (January 15, 2016).

STMicroelectronics has shown another approach wherein the Silicon Photonics IC is the integration platform, with control IC and laser assembled to the photonic IC. Grating couplers are used to transport the light into and out of the IC and out of the laser into the IC. The STMicroelectronics process uses 3D face-to-face integration of the electronics package to the Silicon Photonics wafer, in die-to-wafer fashion, which allows testing the IPE at the wafer level after the bonding step. Otherwise the test requirements for such an assembly would be similar to the Fujitsu example.

PETRA (Japan) demonstrated another approach using the Silicon Photonics chip as the platform. In their design, the light from the fibers is directly coupled to Ge photodetectors that are part of the Silicon Photonics package. Vertical optical waveguides are formed in a two-step lithography defined UV-curable resin process that forms then clads the waveguides directly over the Ge photodetectors. This process relaxes the fiber alignment tolerance, and permits direct butt coupling of MMF to the so-called optical coupling "pins". The potential downside to this

approach is that test may need to occur after the resin steps, adding more process time and value into the wafer before test.



Schematic representation of a receiver assembly proposed by PETRA (Japan). Wafer scale test of the Silicon Photonic platform can be carried out as all interfaces are vertical. Adapted from Okamoto, Daisuke et al. "A 25-Gb/s 5 × 5 mm2 Chip-Scale Silicon-Photonic Receiver Integrated with 28-Nm CMOS Transimpedance Amplifier." Journal of Lightwave Technology 34.12 (12 Nov. 2015).

Wafer scale testing of the photonic component is feasible if vertical grating couplers are used as the photonic interface. Semiconductor equipment and testing company Physik Instrumente of Germany has pointed out that typical semiconductor wafer test probes position with micrometer accuracy, but to properly test Silicon Photonic circuits, nanometer accuracy may be needed. Their solution is to use a semi-active alignment wherein a quick wafer scan is used to locate main coupler modes, then a gradient algorithm provides fine probe alignment. This illustrates the challenges of high-throughput wafer level testing of nano-photonics devices. In reality there will be a significant fab learning curve to implement these new processes. As an example, imec has published results of their photonic test station that has shown measuring the insertion loss of vertical grating couplers to have a six sigma tolerance of 0.07 dB, and a photo detector responsivity measurement six sigma tolerance of 0.02 A/W.

In summary, introduction of new process steps goes hand in hand with new test steps, and such tests are challenging, especially at desired high throughput. Several groups have demonstrated feasibility of wafer scale photonic testing, and commercial equipment is available in the market today (2016).

Summary

We have shown that the market motivation for development of Silicon Photonics is likely down to the chipset level in the long-term, ultimately disrupting sever design and data center design. Viewed as only a sever-level communications sub-component, the Silicon Photonics market, although growing, is of relatively modest size. The market size likely limits economies of scale, especially for smaller, fabless design houses, who have limited choices today to manufacture their designs. On the other hand, vertically integrated suppliers such as IBM and Intel, and to a lesser extend vertically integrated networking suppliers such as Cisco and NTT may have key advantages to deploy Silicon Photonics across a range of data center functionalities, leveraging higher-value sales of processors, servers, and switches incorporating Silicon Photonics to offer price-performance levels component suppliers may be challenged to achieve. This advantage then may be a complement to the interconnect from server out and up into the data center fabric.

Also, we have shown that from the technology viewpoint, Silicon Photonics is not mature, and may not be so for 5-10 years. Hundreds of leading and other Universities are investigating myriad options for better designs, publishing thousands of papers each year. Although Silicon Photonics has been commercialized in limited examples, we think there is a high likelihood that newer innovations will be incorporated rapidly in commercial products, leading to increased performance rapidly becoming available in subsequent design iterations.

These factors create business risk at various points in the Silicon Photonics value chain. Some risk arises from technical sources, such as manufacturing yield and quality issues for cutting edge products. This was already demonstrated when Intel delayed sampling, in 2015, of their first generation Silicon Photonics products, due to quality issues (since resolved, apparently). Addition risk arises from the obsolescence of previous generations of products by newer, dramatically better products. While there is likely a first mover advantage to capture the next round of data center designs using 100 Gb/s (4 x 25) optical communications, there is risk both to the Silicon Photonics suppliers and to the technology adopters, of effectively paying too much for and/or settling for too low performance in early Silicon Photonics products. Consider that Microsoft Azure, Google Cloud Platform, and Amazon Web Services are competing for the cloud compute market, and what are the impacts of (a) adopting best available optical interconnect today, or (b) waiting for the market to mature more. The financial implications of a decision could be catastrophic to business models depending on delivering massive resource scale at competitive costs and performance.

We provide motivation for the argument that packaging and test drive costs, and these areas are in a very nascent stage of development today. Even something as simple as the choice to integrate fiber to the chip vertically (perpendicular to the plane of the wafers, with grating couplers) or horizontally (using butt coupled fiber and spot size converters) can have a large impact on cost. Leaders in the field have stated these areas are not mature and represent "the single biggest technical hurdle to overcome to enable successful commercialization of silicon photonic integrated circuits." (University of British Columbia). IBM noted only last year (2016) that "Silicon photonics leverages microelectronic fabrication facilities to achieve photonic circuits of

unprecedented complexity and cost-efficiency." and "To reach the potential of silicon photonics, we argue that disruptive advances in packaging cost, scalability in optical port count, and scalability in manufacturing volume are required."

We have also painted a picture of an intense level of work being performed, mainly in academia, investigating alternatives to every building block of Silicon Photonic PICs. We showed in some cases there are dozens of different approaches that have been or are being investigated, making choices to fabless designers simply myriad. Limited design rules and process flows available from foundries add barriers to bring designs to market in a cost effective manner. This is another reason the large, vertically integrated players have an advantage today.

In conclusion, we think that Silicon Photonics has earned a place in the next generation data center optical communication solutions. The technology is ready to begin a life cycle similar to the Moore's Law trajectory followed by electronics integration. We expect rapid introduction of new solutions in a very competitive market for the next 10 years, or more. All players in the Silicon Photonics value chain should be making informed decisions today about how and when to participate, from fabless design houses to communication specialists to data center architects. We sincerely hope you find this work enabling in your decision making process.

History of Silicon Photonics: Timeline

What follows is a select set of achievements and work from the literature and other sources. Any effort to create a timeline like this is incomplete, and we admit this is the case. Omission of a given paper or group is not to be taken as diminishing the work. Photonics goal is to help you to get a feeling for the development trajectory to assess the maturity of the industry. In general, we have listed only the lead organization when attributing any given work. The research in Silicon Photonics is multi-disciplinary and often cooperative, so there are often more than one group contributing to a given effort, and often several.

For those that want to dig deeper, the source materials are listed in the bibliography, including associated web addresses (note: in many cases a subscription is required to access he full papers). It should also be noted that publication by private groups is uneven. While Intel or IBM publish many papers and attend many conferences, smaller companies doing extremely important work may not. A good example is Skorpios, a startup running in New Mexico in the US. While very few entries that follow are attributed to that team, nonetheless Skorpios has an important commercial position with their chosen approach. We do not believe this is a large shortcoming given so many groups working in the technology; the timeline will prove useful as noted to gauge the state of affairs.

19860114	Richard Soref and Joseph Lorenzo publish the foundational work leading to Silicon Photonics, stating "single crystal Si will be suitable for building directional couplers, filters, star couplers, optical switches, mode converters, polarizers, interferometers, and modulators that operate at X = 1.3 or 1.6 pm (and beyond)-essentially every integrated-optical component except an optical source" (emphasis added)
20000525	Springer publishes the book "Integrated Silicon Optoelectronics. A similar but updated work by the same author (Horst Zimmerman) is published by Springer in 2004, under the title "Silicon Optoelectronic Integrated Circuits".
20000701	MIT Technology review says "Get ready for optical switching in the telecommunications network backbone, then an all-optical Internet, and finally optical integrated circuits"
20001231	SPIE reports on progress for silicon light sources and photonic switching without MEMS work at Agilent and other labs.
20010415	An Intel self-published article says "Six things are required for optical systems: light source, guide channel, modulation, photo detection, low-cost assembly, and intelligence." The article also refers to a 50 Gb/s Silicon Photonics prototype.
20010601	MIT Technology review notes that a silicon LED was demonstrated in 1996 at the University of Rochester, but efficiency too low to be useful. The article says in March 2001 the University of Surrey demonstrated silicon LEDs only "a factor of three" away from commercial diodes. The article concludes that the future of silicon microphotonics is promising.
20020228	An EE Times article reports that at that year's Intel Developer Forum (IDF) a Silicon based WDM filter (wavelength division multiplexer) is shown that "puts the functionality of today's $10,000 chip onto a $1 chip."
20020408	In an interview with Optical Keyhole, Bookham Technology discusses their ASOC (Application Specific Optical Component) technology, including a 100 GHz WDM silicon chip.
20021213	University of Cambridge shows electroluminescence from Si/SiGe quantum cascade emitters at 150K
20030701	A PC Magazine article highlights Avanex, Cidra Corp., and NeoPhotonics as companies trying to develop Silicon Photonics for cost-effective broadband delivery over fiber.
20031117	The University of Central Florida reports they have integrated Lithium Niobate with a silicon substrate as path towards integrated photonics.
20031229	Aixtron AG, Cambridge Display Technology Ltd, Osram Opto Semiconductors GmbH Philips Lighting BV and Sagem SA, form EPIC (European Photonics Industry Consortium) to promote commercial growth of photonics technology in Europe. (note: by 2015, EPIC has 240 members from 28 countries)
20040223	Intel announces they have achieved a 1 Gb/s Silicon Photonic modulator.

20040305	Wiley publishes the book "Silicon Photonics: An Introduction" by Graham T. Reed and Andrew P. Knights.
20040601	An article in Laser Focus World indicates that wafer-level pick and place is viable for photonics integration (note: this is still not clear and search for monolithic integration continues today (2016)).
20041012	Université Paris Sud does a detailed comparison of strip and rib waveguides in an SOI platform, showing the strip geometry to be very sensitive to wall roughness.
20050101	Intel publishes a white paper on their CW Silicon Raman Laser in CMOS. (note: Intel decided not to use this technology, developed in cooperation with UC Santa Barbara.)
20050131	Market research firm BCC releases a report on Photonic Integrated Circuits and says the PIC market is growing much faster than discrete photonic components.
20050328	Luxtera announces "World's First 10Gbit CMOS Photonics Platform".
20050518	MIT publishes research paper on Silicon Microphotonics, says the key driver is "intrinsic distance*bandwidth limitation of electronic communication links".
20050815	A3PICS article in photonics.com shows 2.5 Gb/s silicon photoreceiver with higher sensitivity and comparable error rate to a GaAs device.
20060121	MIT, Cornell University, BAE Bell Labs, and Columbia University present early results of creating devices such as modulators and filters in a CMOS process using Silicon Photonics, as part of DARPA funded AS-EPIC program.
20060131	An article in SPIE reports that "Silicon poises for disruption" in markets including interconnects.
20060424	Luxtera reports on progress creating integrated Silicon Photonics including fiber to chip coupling and high-speed modulation.
20060630	In an article in IEEE Microwave Magazine, UCLA, Intel, and University of Surrey conclude "The future is looking bright. Silicon photonics could provide low-cost opto electronic solutions for applications ranging from telecommunications down to chip-to-chip interconnects"
20060913	UC Santa Barbara and Intel show an electrically pumped AlGaInAs silicon laser with the resonant cavity completely in silicon, potentially eliminating nano-scale assembly processes for a hybrid light source on silicon.
20061004	Kotura presents some results of CMOS based Silicon Photonics including arrayed waveguide gratings, mode converters for fiber to chip coupling at lower insertion loss, and variable optical attenuators; they predict 100 Gb/s integrated devices will be commercially available "soon".
20061231	In an article in the Journal of Lightwave Technology, UCLA researchers suggest Silicon Photonics could displace III-V photonics and show a commercial silicon-photonics based VOA (variable optical attenuator) from Kotura as one example.
20070122	Mario Paniccia, Director of Intel Silicon Photonics Technology Lab, says Si Photonic modulators or lasers could be commercialized by 2010, says goal is higher integration.
20070131	A paper from Ghent University shows "Highly Efficient Grating Couplers Between Optical Fiber and Nanophotonic Waveguides".
20070329	A paper by IBM researchers demonstrates ultra-compact wavelength division multiplexing (WDM) devices using silicon photonic wires for on-chip interconnects.
20070724	Intel labs demonstrates a 40 Gb/s silicon modulator.
20070912	Ghent University-imec describes proposed processes for die to wafer bonding of III-V lasers to Silicon.
20070919	IME Singapore demonstrates a 15 GHz SiGe photodetector in CMOS.
20071129	Musashi Institute of Technology shows emission in the 1.2 to 1.6 micron band from Ge quantum dots on Silicon/Silica substrate
20071231	OIDA (Optoelectronics Industry Development Association, Washington DC) issues a report discussing opportunities and challenges for Silicon Photonics commercialization. Of interest the report suggests a target of $1/Gb/s, which is later adopted by Facebook at a price target.
20080101	The EU WADIMOS program is started to demonstrate a photonic interconnect layer on CMOS.
20080205	University of Southampton receives an EPSRC Grant to work on Silicon Photonic Interconnects in collaboration with industry
20080221	Kotura announces a partnership with OKI Optical in Silicon Photonics initially for a 10 Gb/s receiver
20080227	Lightwire (formerly SiOptical announces a commercial SFP Active Optical Cable (AOC) with 10Gb s performance based on Silicon Photonics, claims it uses 0.4 Watt vs. 7 W for a 10 Gb/s copper Ethernet or 1-2W for conventional optical components. (note: Cisco acquired Lightwire in 2012 to create the foundation of its Silicon Photonics products.)
20080629	Luxtera and University of Rome show integration of a Ge photodetector in to 130 nm CMOS

20080903	Kotura and Sun awarded $14M from DARPA in part to develop Silicon Photonic interconnects for high performance computing
20081208	Intel announces an avalanche photodiode (APD) in Silicon Photonics
20081218	Intel lays out the road map for the "six building blocks" for Silicon Photonics: Light source, waveguides, modulation, detection, packaging, and integrated intelligent control. (Note: in addition to Intel's six key elements, it is by now clear that chip to fiber coupling is critical for useful Silicon Photonics.)
20090131	A multi-disciplinary team coordinated by Intel, including UC Santa Barbara, Numonyx and others demonstrates detection at 40 Gb/s in a Silicon Photonics Avalanche Photo Diode (APD).
20090603	Luxtera announces partnering with Freescale to produce its Si Photonics platform.
20090729	NEC and OITDA publish results for a tunable laser fabricated with silicon photonic-wire waveguide micro-ring resonators.
20090801	Research and Markets reports the Global Silicon Photonics market was $23M in 2008 and will be around $850M in 2014.
20090804	Kotura announces they are selected by Santur to provide a 10 x 10 100Gb/s Silicon Photonic solution.
20090911	The EU program WADIMOS (Wavelength Division Multiplexed Photonic Layer on CMOS) reports results on CW III-V microdisk lasers on SOI fabricated in a 200 mm CMOS pilot line.
20090922	Ghent University-imec demonstrates viable Silicon waveguides in CMOS.
20091019	McGill University demonstrates rolled-up microtubes of InGaAs/GaAs as quantum dot lasers, albeit optically pumped.
20100107	University of Twente proposes Al2O3-ErEr3 + doped waveguide as an optical gain medium, optically pumped using a laser diode source at 977 nm
20100203	MIT announces a Ge on Si laser operating at room temperature, with optical pumping.
20100317	Kotura announces industry-first Silicon Photonics MUX/DeMUX for 500 Gb/s WDM.
20100409	WADIMOS claims to have adapted III-V processing to be compatible with CMOS and integrated a laser coupled to Si waveguide.
20100429	UC Santa Barbara and Intel report results from lasers made using bonded III-V material on a silicon photonic circuit; bonding is done using low-temperature O2 plasma assisted bonding.
20100616	Université Paris Sud demonstrates intrinsic optical gain at room temperature of single-walled carbon nanotubes.
20100630	Universiti Kegangsan Malaysia demonstrates optimization of a 3x3 optical switch based on integrated Mach-Zehnder Interferometer in LiN
20100708	University of Twente demonstrates a distributed feedback waveguide laser using Al2O-Er3 + waveguide on silicon.
20100721	ETRI Korea reports on a High Sensitivity 10 Gb/s receiver fabricated by Ge on Si, operating at 1.55 microns
20100722	MINATEC Institute reports on progress in Silicon Photonic packaging challenges.
20100727	Intel announces demonstration of a 50 Gb/s Si Photonic link.
20100801	In an early example of a large Chinese effort in Silicon Photonics, Peking University shows a Selective-Area Metal Bonding process to integrate InGaAsP Lasers on Si.
20100925	Ghent - imec spin off Caliopa to commercialize Si Photonic based optical transceivers.
20101104	Luxtera announces a 100 Gb/s Silicon Photonic based data center interconnect.
20101118	A*STAR demonstrates a mode converter useful to implement polarization diversity in Silicon Photonics.
20101130	MIT publishes report of DARPA work "Demonstration of a 10 GHz CMOS-Compatible Integrated Photonic Analog-to-Digital Converter"
20101201	IBM releases some details of its Si Photonic work and says it will be ready in 3 to 5 years.
20101202	Innolume GmbH announces promising results for Silicon Photonics work funded by the Federal Ministry of Education and Research (BMBF)
20110111	Molex acquires Luxtera's AOC business.
20110131	The University of Washington and Intel announce the launch of OpSIS to advance Silicon Photonics including low-cost foundry support for researchers
20110203	The OpSIS multi-project wafer program officially opens at the University of Washington, with backing from Intel, to allow more groups access to a foundry to develop Silicon Photonics.

20110208	Teraxion publishes an article about their development of 100G and 400G solutions, saying "Optical functions can now be integrated using CMOS compatible processes, and packaging these new optical circuits will become critical in making these products cost-effective and reliable.
20110217	University of Twente demonstrates an efficiency of 67% of a diode-pumped Al2O3:Yb3 distributed Bragg reflector channel waveguide laser on silicon.
20110301	Markets and Markets reports the 2010 market for Silicon Photonics was $112M and will grow to $2B in 2015
20110310	Tyndall National Institute shows a planar fiber packaging method for Silicon Photonic integrated circuits.
20110402	SiFontonics announces a CMOS 10 Gb/s receiver using a Ge photodetector and transimpedance amplifier all in CMOS
20110425	MINATEC demonstrates using the 3D geometry of a wafer-bonded Silicon Photonics manufacturing scheme to construct a highly efficient chip to fiber coupler.
20110526	University College London demonstrates electrically pumped InAs GaAs QD lasers monolithically grown on Silicon substrates.
20110608	McGill University reports on integration of single rolled-up InGaAs/GaAs microtubes with silicon-on-insulator (SOI) waveguides.
20110811	Luxtera announces the first single-chip 100 Gb/s Silicon Photonic integrated solution.
20110916	Skorpios, a startup launched in 2009, receives $19M Series B funding from Ericsson, Nokia Siemens Networks, and other investors. Later in the year, another $2M from Deutsche Telekom is received.
20110916	Fujitsu announces progress in athermal modulated light sources, which hold promise to reduce power requirements compared to sources needing thermal tuning.
20110929	BAE hosts the opening of OpSIS CMOS foundry services
20111005	Universitat Politecnica de Valencia demonstrates modulation up to 40 Gb/s using electro-optical modulators enhanced via slow light propagation.
20111101	Skorpios announces they completed a Series B round of funding with another $2M investment from T-Venture.
20111110	Aurrion announces it is awarded $13.9M DARPA project as part of E-PHI for integrated photonics development
20111122	Skorpios applies for a patent for its STAB process (System for Template Assisted Wafer Bonding)
20111219	ETRI Korea shows silicon photonic integrated circuits operating to 30 Gb/s
20120104	University of Paris and collaborators demonstrate a 40 Gb/s Ge photodetector on Si with 120 GHz bandwidth
20120119	The Chinese Academy of Sciences reports a 25 Gb/s silicon microring modulator based on misalignment-tolerant interleaved PN junctions.
20120123	Luxtera opens its Si photonic process to OpSIS community, a foundry service that provides access to optoelectronic integrated circuits to the community at large, at a modest cost.
20120123	University of Toronto researchers report a 28 Gb/s Silicon Microring Modulator.
20120211	Luxtera ships one millionth Si Photonics 10Gb/s channel.
20120223	Leti-HELIOS demonstrates a 40 Gb/s modulator in silicon
20120224	Cisco announces its acquisition of Lightwire.
20120229	Lumerical announces INTERCONNECT Photonic IC design software with support for Silicon Photonics.
20120301	Luxtera and STMicroelectronics announce a partnership whereby STMicroelectronics is granted rights to use Luxtera's Silicon Photonics intellectual property to manufacture products
20120301	Kotura announces a silicon-photonics based low power 100 Gb/s optical engine.
20120302	LightCounting says 100G QSFP is "the next war zone" in data center transceivers and if silicon photonics companies can deliver what they promise and at the right price, these products will be a game changer.
20120304	Teraxion presents an ultra-compact Silicon photonic DQPSK demodulator.
20120305	CEA-Leti and III-V Lab Demonstrate a Fully Integrated Silicon Photonics Transmitter using a bonded III-V laser.
20120329	UC Santa Barbara presents results of novel polarization control devices including asymmetric directional couplers and bent directional couplers. Ultra-low loss waveguides using Si3N4 are also presented.
20120409	Caliopa raises another $1.7M from existing investors to finish and launch its Silicon Photonic product for FTTH and other markets.

20120514	UC Berkeley achieves room-temperature-operating monolithically grown InGaAs lasers on a platform with MOSFETs which retain function, demonstrating proof of concept of full integration of photonics and electronics in a CMOS platform.
20120515	MIT describes Silicon Photonic open foundry platform based on 45 nm SOI-CMOS.
20120520	University of Washington reports a 25 Gb/s low power silicon modulator.
20120620	The Chinese Academy of Sciences and Tsinghua University demonstrate 40 Gb/s silicon modulator based on cascaded microring resonators.
20120620	Chinese Academy of Sciences shows a 40 Gb/s silicon Mach-Zehnder modulator based on interleaved PN junctions, improving on the results of just a few months ago.
20120715	Market Research firm Yole estimates Silicon Photonics to capture $180M but still only 2% of the Optical Components Market.
20120831	Fujitsu announces it has developed a 10 Gb/s Silicon Photonic chip to chip interconnect that does not require thermal control
20120904	IME Singapore, A*STAR, and MOSIS announce Silicon Photonics wafer prototyping service.
20120910	Bell Labs demonstrates 50 Gb/s QPSK using Mach Zehnder modulators in silicon
20120912	University College London describes a CW InAs-GaAs quantum dot laser diodes monolithically grown on Si substrate with low threshold current densities.
20120921	Yole Research says the Silicon Photonics market will be worth $75M in 2012 and grow to $140M in 2015
20120927	Aurrion shows latest results using selective bonding for heterogeneous integration on Silicon.
20121127	Kotura is named to the Deloitte Tech Fast 500
20121203	Molex announces active optical cables using Luxtera Silicon Photonic chips
20121204	Fujitsu demonstrates flip chip bonding of III-V optical amplifiers onto Silicon Photonics circuits to butt couple the SOA to a spot size converter, achieving mW power at a wall-plug efficiency of nearly 8%. The alignment is done using commercially available imaging and alignment equipment.
20121213	IBM shows the first Silicon Photonics in a sub-100 nm process with 25 Gb/s WDM in 90nm CMOS Integrated Nano-Photonics.
20121213	A*STAR demonstrates 4-channel 160 Gb/s Silicon Photonics receiver in a CMOS compatible process.
20121213	A Forbes headline puts nanophotonics at a $100B opportunity.
20121213	A*STAR publishes work on a fiber to Silicon Photonic waveguide interface with over 2 micron alignment margin
20130117	Intel and Facebook announce plans to dis-aggregate server architecture leveraging Silicon Photonic interconnects.
20130118	Finisar stock falls after analyst downgrades Finisar based on Intel's announcement. This is part of an ongoing back and forth between Finisar executives, analysts, and the media over the question of whether Silicon Photonics was necessary to compete in the future.
20130124	Infonetics publishes survey results indicating 75% of data centers will need 100G by 2014.
20130128	Cisco reveals it is working on a 2.5D interposer design for silicon photonic integration.
20130129	EE Times Asia reports Kotura will utilize an un named "large CMOS foundry" to make 100 Gb/s silicon photonic products in 2014.
20130202	Peking University demonstrates 10 Gb/s over 80 km with a Silicon Photonic system.
20130204	IBM and Northwestern University show development of GaN on Si as a possible CMOS compatible photonic substrate.
20130207	Ghent University and imec show heterogeneously integrated III-V SOI single wavelength tunable laser.
20130210	Markets and Markets reports Silicon Photonics was $150M in 2012 and will be $1.55B in 2022.
20130211	Chinese Academy of Sciences shows 45-60 Gb/s low-loss silicon Mach-Zehnder modulators.
20130213	Bar Ilan University shows wafer bonding of InP to Silicon using a low-temperature self-assembled monolayer bonding as step on path to effective integration of III-V active devices to Silicon.
20130227	UC Santa Barbara shows progress on an integrated terabit class silicon photonic transmitter using multiple bandgap quantum wells
20130304	Skorpios announces it has achieved 100 Gb/s with unique wafer-scale integration of III-V lasers to Silicon.

20130308	Fujitsu reports four-wavelength Silicon hybrid laser array with ring-resonator based "mirror" for an efficient CWDM transmitter.
20130308	Peking University shows silicon photonic couplings, beam splitters, reflectors, and filters based on binary blazed gratings.
20130312	Startup Compass-EOS announces 800 Gb/s core router based on Silicon Photonics.
20130315	imec announces that its fully integrated Silicon Photonics platform is available through a multi-project wafer (MPW) process via ePIXfab.
20130317	Acacia reports on progress Silicon Photonic Integrated Circuits for WDM Technology and Optical Switch.
20130317	Bell Labs demonstrates a 224 Gb/s receiver and modulator using Silicon Photonics.
20130317	Cisco and Stanford demonstrate 112 Gb/s over 2427 km using Silicon Photonic Modulator and CMOS driver.
20130317	Cisco announces 100 Gb/s CPAK pluggable transceiver based on Silicon Photonics.
20130317	Kotura announces its 100 Gb/s Silicon Photonic optical engine is available in QSFP form factor.
20130317	UC Santa Barbara and Aurrion report on a 400 Gb/s WDM receiver using low-loss SiN arrayed waveguide grating Integrated with Hybrid Silicon Photodetectors.
20130317	National Tsing Hua University Demonstrates 3D fiber coupler to silicon with 3 micron tolerance and 3 to 4 dB loss
20130321	Fujikura demonstrates QPSK modulation up to 60 Gb/s using a novel design of nested Mach Zehnder Interferometers with multi-mode interferometers used as low loss splitters and combiners. Total optical loss of 10 dB is achieved.
20130321	Rice University reports developing low-loss waveguides and high-speed photodetectors in standard 0.18 µm CMOS with no post-processing.
20130327	Fujikura and A*STAR announce development of first Silicon Photonic 40-60 Gb/s QPSK Modulator.
20130404	University of British Columbia shows a nested racetrack resonator structure as a vernier filter In an SOI platform.
20130411	Intel demonstrates a low-cost 100 Gb/s Silicon Photonic module.
20130412	University of Toronto and IBM show improvements in modulation rates using coupling modulation of microrings.
20130507	MOSIS cooperates with imec, Tyndall National Institute and ePIXfab to offer multi-project wafer service for Silicon Photonics.
20130511	Opsis (University of Delaware), University of Washington, ASTAR and collaborators offer a 30 Gb/s Silicon Photonic multi-project wafer shuttle service.
20130515	Mellanox announces agreement to acquire Kotura.
20130603	UC Davis shows athermal performance of ring modulators clad with titanium dioxide.
20130607	Mellanox announces it will acquire optical interconnect designer IPtronics.
20130609	NTT Nanophotonics Center demonstrates a 25 channel all-optical switch in Si Photonics
20130614	University of Southampton shows 40-50 Gb/s modulators from EU HELIOS and UK Silicon Photonics programs.
20130623	Tohoku University achieves a tuning range of 44 nm using a heterogeneously integrated quantum dot/Silicon Photonics laser diode, suggesting it is "a breakthrough technology for high-capacity data transmission".
20130627	IBM Zurich shows flip-chip optical couplers for Silicon Photonics.
20130702	Nanyang Technological University demonstrates an improved splitter wherein multi-mode interferometers are used as splitters with low loss.
20130703	University of Stuttgart achieves 87 percent efficiency coupling from optical fiber to Silicon waveguide.
20130722	Georgia Institute of Technology integrates SiN films on SOI platform for ultra-high Q resonators
20130731	University College London reports on use of AlAs nucleation layers and GaAs buffer layers to grow InAs QD lasers directly on Silicon, achieving room temperature lasing in some cases.
20130815	Ghent University / imec shows fabrication-tolerant four-channel WDM filter based on collectively-tuned Si microrings.
20130823	BinOptics announces they have integrated etched facet manufacturing into high-yield Silicon Photonics applications. (note: BinOptics was acquired by M/A-Com in November 2014)
20130829	Columbia University shows feasibility of automatic thermal tuning and stabilization of microring resonators.

20130904	California Institute of Technology achieves 85% coupling efficiency from an optical fiber to a nanoscale silicon optomechanical cavity.
20130909	Chinese Academy of Sciences achieves 88% coupling efficiency of an optical fiber to a SOI platform using a non-uniform focusing grating coupler.
20130912	Huawei acquires Caliopa.
20130915	Chinese University of Hong Kong shows a high-responsivity photodetector made using a graphene SOI heterostructure waveguide. Columbia University and the Vienna University of Technology independently report progress in similar systems.
20131007	EE Times reports that Mellanox will ship 100 Gb/s Silicon Photonic-based products in late 2014 or early 2015.
20131008	imec releases fully integrated Silicon Photonics transceiver platform.
20131105	Fujitsu demonstrates a modular server architecture using Intel Silicon Photonics.
20131118	Compass EOS raises additional $42M
20131205	Walter Schottky Instiut demonstrates room temperature lasing from (optically pumped) individual core-shell GaAs-AlGaAs nanowires.
20131218	ST Micro expects to ship Silicon Photonics from 300 mm wafer line in mid-2014.
20140101	Fujitsu reports progress of a terabit per second Silicon Photonics optical transmitter packaged with a CPU.
20140110	University of Delaware demonstrates a novel silicon microring based laser with heterogeneous integration of a III-V optical amplifier.
20140122	Shanghai Jiao Tong University demonstrates on-chip optical power monitoring with interleaved P-N junctions on a silicon waveguide.
20140127	UC Santa Barbara shows record performance of a 1.3 um CW QD laser on silicon.
20140128	UK Silicon Photonics for Future Systems Program awards $10M to bring Silicon Photonics to mass markets.
20140129	University of Southampton demonstrates a 50 Gb/s receiver in silicon using multi-mode interferometers and Ge detectors.
20140201	Institute of Microelectronics and Optoelectronics Huangzho Proposal for a 2×2 Optical Switch Based on Graphene-Silicon-Waveguide Microring
20140204	Huazhong University of Science and Technology demonstrates a photonic switch using electromagnetically induced transparency-like effect in two waveguides coupled to a microdisk resonator.
20140215	IBM demonstrates an 8 x 8 Photonic Switch Fabric integrated with CMOS Logic and Device Driver Circuits.
20140219	Photonics Electronics Technology Research Association shows Ge LED on silicon for very short reach interconnect.
20140301	Technical University of Denmark shows a high contrast grating reflector acting as a mirror and vertical to lateral coupler, achieving ultra-fast laser output into silicon waveguide.
20140306	OpSIS offers a 25 Gb/s Silicon Photonic platform as part of wafer shuttle service.
20140307	Molex promotes Silicon Photonics in PSM4 active optical cables (AOCs) as "future proof" data center solution.
20140309	Skorpios and Ericsson demonstrate 448 Gb/s using a tunable hybrid laser in CMOS Silicon Photonics.
20140310	Skorpios shows a monolithic integration process of bonding III-V material to silicon at wafer scale, butt coupling between III-V and silicon waveguides, and thermal management allowing uncooled operation at high temperatures. At OFC they demonstrate a 448 Gb/s link using the technology.
20140310	Acacia Communications announces the first single-chip Silicon Photonics 100 Gb/s coherent transceiver.
20140310	Mellanox demonstrates 100 Gb/s Silicon Photonics in QSFP at OFC 2014, saying it increases port density 300% over CFP2 or CPAK.
20140310	Skorpios also demonstrates their 100 Gb/s Silicon Photonics solution in QSFP at OFC 2014.
20140311	Lightwaveonline reports that IBM is nearing alpha stage with their 25 Gb/s Silicon Photonics.
20140311	Molex shows 100 Gb/s Silicon Photonics QSFP AOC using 4 x 25 Gb/s channels over a 1 km link at OFC 2014. They also preview a new 28 Gb/s 4 km low power AOCs based on Silicon Photonics.
20140313	A*STAR reports on development of Silicon Photonics manufacturing in GlobalFoundries 0.18 µm CMOS foundry.
20140313	Alcatel Lucent reports a reconfigurable 10 x 10 Gb/s (100 Gb/s total) intra-chip Silicon Photonic network.
20140313	In a post-deadline paper for OFC 2014, IBM and Aurrion report on a 30 Gb/s optical link based on Silicon Photonics in a 32 nm CMOS device.

20140313	Mentor Graphics shows on update toward Building an "EDA" environment for Silicon Photonics.
20140320	University of Shenzhen shows MoS2 can be used as ultra-fast photonic switch.
20140325	IBM reports it expects its sub-100 nm Silicon Photonics 25 Gb/s technology will be fully qualified by 2015.
20140326	Oracle reports a high power (20 mW) widely tunable Silicon hybrid external cavity laser for Silicon Photonics WDM links.
20140402	Hitachi shows a Silicon Photonics light source using a hybrid surface emitting laser and lens fabricated on an SOI substrate.
20140407	Rockley Photonics, a UK based Silicon Photonics startup, closes series A funding. (note: Rockley founder Andrew Rickman is later quoted in the trade press saying the round was "multi-millions of dollars".)
20140414	Tyndall National Institute reports on progress achieving all needed packaging steps, including fiber alignment and bonding, with existing, mature electronic packaging methods and equipment.
20140430	Skorpios presents its Monolithic Silicon Platform for 100G/400G Ethernet Applications at the Ethernet Technology Summit.
20140430	In an article on compoundsemiconductor.net BinOptics (now M/A-Com) promotes their etched facet technology as a route to a light source for Silicon Photonics
20140501	University of Toronto shows a novel design of a grating coupler integrated with a Mach Zehnder Interferometer that can couple light from a fiber at an arbitrary polarization to the desired TE mode of the silicon chip waveguide with ~10% power insertion loss.
20140501	Ecole Polytechnique Federale de Lausanne reports work showing a 700 nm LED made from MoS2 epitaxially grown on Silicon, potentially useful for Silicon photonics.
20140501	McGill University demonstrates thermally controlled coupling of III-V rolled up microtubes to Silicon waveguides, advancing a potentially promising light source for Silicon Photonics.
20140505	University College London demonstrates 1.3 um InAs-GaAs quantum dot lasers monolithically grown on Si substrates using InAlAs-GaAs dislocation filter layers.
20140513	MIT shows monolithic erbium- and ytterbium-doped microring lasers on silicon, with thresholds low enough to be pumped by an on chip diode. The authors conclude such rare-earth doped lasers are a scalable platform for a range of applications including communications.
20140519	MIT shows a CMOS compatible high power (75 mW) Er-doped DFB (distributed feedback) laser.
20140531	NTT demonstrates a monolithic silicon-germanium-silica platform with a 16-channel WDM receiver. The authors note that the platform is well suited to directly integrate control electronics as well.
20140603	Optic2Connect launches a complete software design solution for Silicon Modulators.
20140616	HP introduces The Machine, as a paradigm change in computing. The Machine is variously reported in the media as using Silicon Photonics and memristors for memory.
20140701	A Semiconductor Today article cites Yole Developpement, the leading market research authority in Silicon Photonics, as forecasting Silicon Photonics to be worth $700M USD in 2024. Given the large amount of R&D invested, that is a low potential return. The same article notes that Yole found about $1B had been spent on Silicon Photonic acquisitions in just the last three years.
20140723	EE Times reports that imec is taking orders for the next wafer run of its 28 Gb/s Silicon Photonics platform.
20140813	An Intel article notes that Software Defined Infrastructure needs lots of interconnect bandwidth, which can be satisfied with Silicon Photonics.
20140814	AMO GmbH develops a 50 Gb/s photodetector with wafer-scale CVD deposited graphene that is compatible with Silicon Photonics.
20140831	In a Nature Photonics article, Rockley Photonics founder Andrew Rickman says "Because of its cost competitiveness, silicon photonics is expected to bring single-mode communication into short distance datacentre applications, moving from the periphery of the circuit board towards the switching and processing integrated circuits."
20140908	KTH Royal Institute of Technology proposes Heteroepitaxial lateral overgrowth of InP as a way to integrate a III-V light source to Silicon Photonics free of defects, as an alternative to wafer bonding or other heterogeneous integration approaches.
20140919	Mentor Graphics and Lumerical announce they have unified their optical design and simulation flows.
20140922	Finisar, a long holdout of photonics solutions other than Silicon Photonics, demonstrates a 50 Gb/ optical interface using Silicon Photonics solutions, apparently from Cisco.

20140924	Leveraging STMicroelectronics Silicon Photonics production capability, Finisar demonstrates a hybridly integrated transmitter and receiver operating at 56 Gb/s over 2km of fiber; the authors claim this to be "the first fully integrated silicon photonics transceiver operating above 40 Gb/s."
20140925	University College London reports an InAs/GaAs quantum-dot laser grown on silicon by using InAlAs/GaAs dislocation filter layers to eliminate threading dislocations in the QDs. Lasing up to 110°C is achieved with output power exceeding 100 mW at room temperature.
20140925	University College London and University of Arkansas show an InAs/GaAs QD laser grown directly on silicon operating at room temperature with output to 100 mW at room temperature and operation over 100°C.
20141022	Chiral Photonics demonstrates a Silicon Photonics optical interface with an array of 37 optical fibers accurately integrated to 37 vertical grating couplers with 40 um pitch, having a 1 sigma of coupling loss of only 0.7 dB across the array.
20141030	University of Shenzhen reports MoS2 as an ultra-fast photonic material
20141106	IIT Bombay reports strong interaction of Graphene Quantum Dot emitters on semiconductors
20141110	Technical University of Denmark demonstrates feasibility of lateral emission from vertical cavity lasers on Silicon waveguides
20141111	Luxtera OSS presentation emphasizes importance of packaging and chip to fiber coupling
20141125	M/A-COM acquires BinOptics to gain etched facet laser diode technology
20141203	Huawei and imec announce partnership in Silicon Photonics to amplify work of acquired imec spin off Caliopa
20141204	St. Petersburg Academic University shows microring and microdisk lasers as small as 1.5 μm constructed with active regions of InAs/InGaAs/GaAs QDs. Emission frequency was tunable with the ring/disk size and hole size (for rings) which effectively tunes the whispering gallery modes of the resonant structures. Lasing up to 100°C was achieved.
20141205	Markets and Markets says Silicon Photonics to grow at 24.5% CAGR to 2020
20141209	Purdue University creates CMOS devices on Germanium instead of Silicon
20141211	Ohio University makes a case for wireless (RF, not photonic) short range chip to chip interconnects as part of integrated high-speed connection strategy
20141216	Research firm LightCounting reports that data center demand will drive increased AOC (active optical cable) demand
20141216	Holkar Science College reports on feasibility of creating and manipulating a photonic band gap in a multi-layer LN:MgLN structure
20141217	Nanyang Technological University shows an integrated tunable laser using nano-silicon photonic circuits without MEMS
20141217	Shanghai Jiao Tong University shows a 1 x 2 wavelength selective switch using nested silicon microring resonators and demonstrates dynamic channel routing at 10 Gb/s.
20141219	IBM publishes their work on high throughput microelectronic packaging for Silicon Photonics
20150105	Univesitat Politecnica de Valencia develops a 2x2 optical switch using silicon multi-mode interference couplers using < 25 mW and < 2 us switch time.
20150112	The State Key Laboratory on Integrated Optoelectronics, creates novel all-silicon microring photodetector with 40-Gb/s operation speed based on the defect-assisted subbandgap avalanche mechanism in reverse p-n junctions. This raises the potential of eliminating some Ge-based process steps normally needed for detectors.
20150114	McGill University shows an electrically injected rolled-up semiconductor tube laser.
20150115	PETRA (Japan) develops a Silicon Photonic interposer to enable electronic and photonic integration with athermal performance up to 19 Tb/s/cm2 operating up to 125 °C without compensation.
20150119	Peter Grünberg Institute 9 shows direct bandgap in GeSn allow grown on Si with resulting high Sn concentration.
20150201	IBM and Aurrion show 30 Gb/s optical link combining heterogeneously integrated III-V/Si Photonics with 32 nm CMOS circuits.
20150203	Ghent University-imec demonstrate narrow-linewidth short-pulse III-V-on-silicon mode-locked lasers based on a linear and ring cavity geometry.
20150206	Markets and Markets says Silicon Photonics market to be $498M by 2020.
20150207	Hitachi shows a 25 Gb/s Silicon Photonics fiber link using highly alignment tolerant vertical Ge photodiode.

20150216	Tohoku University reports a Silicon Photonic tunable laser diode with ultra-wide tuning range.
20150223	Companies and Markets reports that Intel has pushed out first commercial shipments of Silicon Photonic products.
20150226	imec-Ghent University show a 4x20 Gb/s WDM Ring-Based Hybrid CMOS Silicon Photonics Transceiver.
20150304	STMicroelectronics shows recent progress in Silicon Photonic 300 mm platform with separate photonics and electronics integrated using 3D flip chip assembly.
20150309	Datacenterdynamics reports that Ericsson is launching the first Rack Scale server design and using Luxtera Silicon Photonics.
20150316	University of Technology Sydney demonstrates electrical excitation of a silicon-vacancy center in single crystal diamond.
20150322	UC Berkeley shows 50 x 50 Si Photonic switch with MEMS-actuated adiabatic couplers sub µ sec switch time.
20150322	McGill University shows a Silicon Photonic enabled 224 Gb/s short-reach optical interconnect, scalable to 400Gb/s/1Tb/s.
20150322	Bell Labs shows four-channel 100 Gb/s per channel discrete multi-tone modulation using Silicon Photonic integrated circuits.
20150322	Texas A&M University reports a 25 Gb/s hybrid-integrated Silicon Photonic Receiver with Microring Wavelength Stabilization.
20150322	PETRA shows 5 mW per Gb/s hybrid-integrated Si-photonics-based optical IO cores and 25 Gb/s error free operation over 300m MMF.
20150322	Research firm Yole reports that there has been nearly $1B in Silicon Photonics related M&A, yet the market for Silicon Photonics is less than $30M in 2014.
20150323	Acacia releases a 400G coherent transceiver using a new generation DSP and Silicon Photonics integration
20150323	Luxtera announces a new PSM4 100G data center solution.
20150323	Mellanox introduces new QSFP pluggable 100 Gb/s Silicon Photonic transceivers.
20150323	Skorpios announces first 100 Gb/s Silicon Photonics transceiver SoCs (System on Chip).
20150323	CrossFiber announces 96 and 144-port photonic switches using 3D MEMS micro-mirrors on Silicon supporting data rates over 400 Gb/s
20150324	The Ethernet Alliance publishes the 2015 Ethernet Roadmap which shows new standards for 400 GbE and discusses Tb/s speeds for the future.
20150326	University of Washington-led team shows an ultrathin Tungsten nanolaser that could lead to a CMOS compatible system using Silicon Nitride
20150326	NEC shows an 8x8 Silicon Photonic switch module with low loss and 150 µ sec switching
20150403	LightReading reports that Facebook thinks "Pluggable modules one day will not be viable." (note: This fits well with Silicon Photonics enabling a paradigm shift in form factor and power requirements.)
20150403	PETRA reports a 1.3 µm Quantum Dot array laser diode and integration details for hybrid integration on silicon
20150413	Columbia University reports Lead Halide perovskite nanowire lasers with low lasing thresholds
20150413	Data Storage Institute of Singapore demonstrates a III-V laser on thin SOI with adiabatic coupling
20150414	UC Santa Barbara reports on reliability of InAs/GaAs QD Lasers epitaxially grown on silicon, shows lifetime of 2700h which is the longest reported so far for epitaxially grown GaAs lasers
20150417	CU Boulder, MIT, and UC Berkeley demonstrate Silicon Photonics manufacture in a 45 nm CMOS microprocessor foundry, without process modification. With a goal to address power consumption of chip to memory interconnects for high performance computing, initial results include 5 Gb/s chip to chip using only 5 fJ/bit.
20150417	Intel and Fujitsu announce the first dis-aggregated server based on silicon photonic interconnects
20150420	The Chinese Academy of Sciences demonstrates a 2x2 thermo-optic switch in SOI with 8 µ sec switch time, and scales to an 8x8 matrix with 20 µ sec switch time. would be better to cite the actual institution
20150421	Hewlett Packard reports on a hybrid silicon microring laser that can be directly modulated and lases up to 105 ˚C.
20150430	California Institute of Technology shows 25 Gb/s 3D integrated CMOS/Silicon Photonic receiver with 0.17 mW/Gb/s efficiency.
20150501	Karlsruhe Institute of Technology shows low power silicon-organic hybrid modulators operating at 112 Gb/s with 19 fJ/bit energy consumption.

20150501	University of Ostrava shows a new fiber-chip edge coupler with large mode size allowing coupling to standard SMF 28 optical fiber in a lensless system.
20150510	MIT shows progress on integrated mode-locked laser using erbium-doped Al2O3 gain medium
20150512	RWTH Aachen University shows Alignment Tolerant Couplers for Silicon Photonics fiber to chip using a beam splitting approach to de-couple alignment design for coupling efficiency and design for high mis-alignment tolerance.
20150513	Johannes Kepler University shows good optical emission results for group IV material using Ge QDs on Silicon after partial amorphization using Ge-ion bombardment.
20150515	UC Santa Barbara demonstrates tunable narrow-linewidth lasers heterogeneously integrated on Silicon including a monolithically integrated external cavity.
20150526	Technische Universitaet Berlin demonstrates direction modulation of QD Semiconductor Optical Amplifiers (SOA) at 25 Gb/s.
20150529	IBM proposes and demonstrates a 4-channel semiconductor optical amplifier integration to a photonics carrier to overcome losses in advanced photonic switch fabrics.
20150608	George Washington University demonstrates a design for a plasmonic MOS-based 2x2 switch with sub-p sec switching times that can integrate into CMOS.
20150610	ETRI Korea proposes a vertical 3D integration architecture and demonstrates a single chip silicon photonic transceiver system operating at 20 Gb/s
20150618	University College London shows InAlAs/GaAs strained layer superlattices can reduce density of threading dislocations for growth of III-V materials on Silicon, enabling QD sources to be monolithically grown on Silicon substrates
20150623	Politecnico di Bari reviews simulation results of Ge Raman lasers for the mid-infrared region.
20150625	Max Planck Institute for the Science of Light shows a new inverted cone all-silicon resonator structure.
20150626	Zhejiang University shows transparent graphene heaters to control micro ring resonators in Silicon Photonics
20150701	Peter Grunberg Institute 9 updates on using GeSn alloys for direct bandgap Group IV material lasers compatible with Silicon substrates.
20150702	Luxtera presents their hybrid integration solution for silicon photonic-based transceivers for 4x25 100G applications, including their InP laser "micro bench".
20150703	Nanjing University of Posts and Telecommunications shows electroluminescense from Si QDs embedded into SiO2 multilayers.
20150703	Soochow University demonstrates MoS2 photodetectors enhanced by graphene QDs.
20150708	Aarhs University demonstrates light emission from Silicon with Sn-containing nanocrystals.
20150715	UC Santa Barbara reviews progress in QD lasers for Silicon Photonics, and demonstrates continuous room-temperature lasing for 2700 hours.
20150720	Michigan Technological University shows that shows Graphene-Boron Nitride nanotube heterojunctions are effective switches.
20150727	ETH Zurich shows a 70 GHz plasmonic MZM modulator integrated to a Silicon waveguide occupying only 10 μm and consuming 25 fJ/bit.
20150804	George Washington University successfully simulates an electrically-driven carbon nanotube-based plasmonic laser on silicon at 1.5 μm with potential to directly modulate at over 100 GHz.
20150806	Peking University presents an analysis of energy consumption in Silicon Photonics systems and promising approaches to lower energy consumption. Among other things, they conclude that Mach Zehnder interferometers can be athermal without additional power while microrings do not have efficient passive athermal solutions. This could be a significant disruption to many designs.
20150806	UC Santa Barbara makes a case for a heterogeneous platform based on a new laser design using heterogeneously integrated SOAs and monolithically integrated external cavity.
20150807	Cornell University demonstrates tunable frequency combs using dual microring resonators in a Silicon Photonics platform.
20150814	Hauzhong University of Science and Technology shows a Ge QD in a silicon nanocavity as a Silicon Photonics light source at telecom frequencies.
20150825	IBM shows methods to integrate fiber arrays to Silicon Photonic systems.
20150831	Ericsson announces a Silicon Photonic switch developed in the Ericsson-led IRIS project; says it will enable integration of thousands of optical circuits on one chip.

20150908	An MIT press release regarding their available Silicon Photonics technology portfolio asserts that Silicon Photonics will use hybrid light-source integration initially, but their Ge laser could be a way forward to fully monolithic integration.
20150912	STMicroelectronics reviews their industrial implementation of a Silicon Photonics platform on 300 mm SOI wafers and results for a 100 Gb/s aggregate data-rate.
20150914	imec demonstrates a Ge waveguide electro-absorption modulator at 56 Gb/s using 12.8 fJ/bit.
20150918	Ghent University-imec review progress on adhesive bonding of III-V light sources onto silicon using DVS-BCB as the adhesive.
20150918	University of British Columbia demonstrates spiral-Bragg grating waveguides propagating TM mode instead of TE, with lower losses and less area requirement.
20150922	UC Davis demonstrates Ti-clad silicon ring resonators with less than 6 pm/°C variation at 1.3 μm.
20150924	Ghent University-imec demonstrate the first example of 28 Gb/s direct modulation of a heterogeneously integrated InP/Si distributed feedback laser.
20150928	EE Times reports that Facebook believes data center photonic interconnect price can be $1/Gb/s in high volume.
20150930	Mellanox announces definitive agreement to acquire EZchip for $811M; increasing market space for Mellanox over $2B.
20151001	Ghent University-imec demonstrate a low-voltage Ge Waveguide APD (Avalanche Photodiode) as part of a high-sensitivity 10 Gb/s Silicon Photonic receiver.
20151001	McGill University shows a low-crosstalk add-drop multiplexer in Silicon Photonics using Bragg grating/Mach-Zehnder interferometer instead of ring resonators.
20151002	Bell Labs Ireland demonstrates a chip-scale thermoelectric laser cooler using electrodeposited bismuth telluride integrated around a hybrid laser suitable for a Silicon Photonics platform.
20151002	Ghent University-imec demonstrate an InP-based quantum well photodiode in the 2 μm wavelength range integrated in a Silicon Photonics platform.
20151006	UC San Diego develops an all Silicon waveguide approach with one back-end step to bond LN as an alternative to III-V hybrid integration.
20151008	Ghent University-imec demonstrate heterogeneous integration of III-V material using DVS BCB bonding to create DFB lasers with operation to 25 Gb/s.
20151013	An article on Time Warner News discusses the debate around leadership of the AIM Photonics Center.
20151014	University of Toronto reports progress in multilayer SiN on Silicon platforms with improved performance of passive photonic components.
20151020	Lawrence Berkeley Lab demonstrates a 2D exitonic laser using monolayer of WS2 on a microdisk resonator, characterized as "a major step towards two-dimensional on-chip microelectronics".
20151022	LightCounting reports that Infinera will use Acacia's Silicon Photonics 100G DWDM after Infinera acquired Transmode who was already using Acacia products.
20151022	University College London reports on progress in Quantum Dot Lasers on Silicon by Direct Epitaxial Growth, indicating that a monolithic Silicon Photonic platform may be expected in the "near future".
20151025	Stanford reports growth of a Ge microdisk with fabrication-level tunable strain in a CMOS-compatible process which may provide a new path for an efficient Ge light source for Silicon Photonics.
20151026	Ghent University-imec demonstrate room temperature lasing from an InP DFB (distributed feedback) laser array grown directly on silicon using a new selective area growth process to get around material mismatch limitations.
20151027	Lomonosov Moscow State University demonstrates an ultra-fast all optical switch using magnetic resonances in dielectric nanostructures with sub-picosecond switch times.
20151105	ETH Zurich demonstrates a 4-channel modulator with capacity of 4 x 36 Gb/s using low power and ultra-small plasmonic Mach Zehnder interferometers. Plasmonic devices may be important at future ultra-dense interconnect nodes. ETH shows integration to a multi-core fiber with spacing of only 50 μm.
20151107	PETRA updates on their successful Silicon Photonics platform on a 300 mm SOI wafer process.
20151112	PETRA (Japan) integrates a Silicon Photonic IC with a CMOS trans-impedance amplifier to create a 25 Gb/s receiver in a 5 mm x 5 mm package. The photonic IC has vertical coupling to fiber facilitating wafer-scale test.
20151113	Shandong University demonstrates that impurity doping to modify the band gap can enable passive silicon optical modulators with advantages over externally driven silicon modulators.

20151118	Politecnico di Bari analyzes Ge on Silicon waveguide engineering for upconversion from 10.6 to 3.53 μm and 6 to 2 μm via 3rd harmonic generation.
20151119	At its Data Center Day, Intel says it is sampling its Silicon Photonics platform with the "Only On-Die Integrated Laser".
20151122	ColorChip raises $25M to continue development of System on Glass photonic products.
20151204	IBM updates on their packaging scheme and integration to optical fiber for their Silicon Photonics platform, says they have a robust manufacturable solution.
20151207	Paul Scherrer Institut demonstrates the first Direct Bandgap GeSn Microdisk Lasers at 2.5 μm for Monolithic Integration on Si-Platform.
20151208	Ghent University-imec demonstrates an on-chip SiN microdisk integrated heterogeneously with colloidal QDs and coupling of the light to on-chip waveguides.
20151214	Intel price point for 100G Silicon Photonics datacenter interconnect is around $500. (Note: this is still 5X the Facebook target but it is early in Silicon Photonics maturation.)
20151217	CMC Microsystems announces general availability of a Multi-Project Wafer service providing access to a suite of Silicon Photonics circuit elements.
20151221	Acacia Communications files for an IPO valued at $125M.
20151224	The European Photonic Libraries And Technology for Manufacturing (PLAT4M) project demonstrates most of the supply chain needed to deliver commercial Silicon Photonics devices by implementing a 16 x 1 Si-PIC Coherent Beam Combiner. The program "highlights the need for a consortium-driven approach to integrated photonics, where all elements of the technology supply chain work together to achieve a single objective."
20151224	UC Berkeley, MIT, and the University of Colorado announce they have integrated a microprocessor and on-chip photonics to communicate from the processor.
20151229	Rochester Institute of Technology demonstrates a low-temperature Pd mediated bonding method to integrate InAs QD lasers to Silicon Photonics, and shows performance comparable to other state of the art QD lasers including operation to 100 C.
20151229	Lightcounting releases a forecast for Active Optical Cables and Embedded Optical Modules that reaches $850M in 2021.
20151231	Columbia University shows first demonstration of real-time firmware controlled switching with Silicon Photonics devices integrated at the chip scale.
20160101	Cisco reports on a new polarization-multiplexing nanotaper chip to fiber coupling with superior performance and compatibility with CMOS processing.
20160101	Cisco demonstrates a silicon nanotaper device which could be used as a polarization multiplexer, overcoming limitations of silicon waveguides.
20160106	Showing the remarkable diversity of research, Kim Il Sung University (North Korea) demonstrates a plasmonic phase modulator with up to π phase shift using loss-overcompensated coupling between a nanoresonator and a waveguide.
20160106	Kim Il Sung University demonstrates a phase modulator using surface plasmon polaritons using only 10 fJ/bit.
20160111	Purdue University demonstrates feasibility of thermally tuning SiN ring resonator-based Kerr Frequency combs.
20160113	UC Berkeley demonstrates a 64 × 64 digital silicon photonic switch with < 4 dB insertion loss and sub μ sec switch time.
20160113	UC Berkeley demonstrates a 64x64 silicon photonic switch with low loss (3.7 dB) and 300 nm bandwidth.
20160114	Technical University of Denmark achieves graphene plasmons operating close to the near-infrared window.
20160115	A*STAR demonstrates a metal-semiconductor plasmonic nanocavity that potentially could be used for on-chip lasers.
20160115	ETH Zurich demonstrates plasmonic Mach-Zehnder Modulators with > 100 Gb/s speed and > 70 GHz bandwidth
20160119	Ciena acquires the InP and Silicon Photonics assets of TeraXion.
20160119	University of Southampton shows a method to selectively grow SiGe based on exposing Si seed regions in an SOI platform.
20160121	Next Platform quotes David Calhoun of Columbia as suggesting Silicon Photonics is at least a few years away; we clarify with Calhoun that this is more about extreme-scale HPC interconnect than general data center applications.

20160125	Sun Yat-sen University demonstrates a low-temperature CMOS compatible SiN process to make low-loss waveguides. Such a process could allow more complex photonic integration schemes.
20160127	Huazhong University of Science and Technology demonstrates a photonic crystal ring resonator in an SOI system with Q approaching 15,000. The photonic crystal is formed with air holes in a silicon ring resonator.
20160131	Fujitsu shows an integrated platform with the control (CPU) electronic and optical transceiver attached to a substrate that can be BGA integrated to a board.
20160205	Zhejiang University shows a microdisk resonator tunable using a transparent graphene heater.
20160210	In an interview with gazettabyte, startup Sicoya's CEO Sven Otte says their "Application Specific Photonic Integrated Circuits" will target chip to chip communication.
20160211	Walter Schottky Institute grows GaAs nanowire lasers directly on a silicon substrate.
20160212	Corning publishes results on new fibers for data center applications, including high-bandwidth multi-mode fiber.
20160213	Lumerical publishes design rules for Silicon Photonics lithography highlighting photonic-unique requirements and high sensitivity to dimensions.
20160216	University of St. Andrews shows new method of creating an on-chip laser using a photonic crystal as an external cavity. Photonic crystals show promise as high Q cavities.
20160218	Walter Schottky Institute shows lasers made from core-shell nanopillars grow on silicon. Although optically pumped, the group says they are working on a path to electrically pump the laser.
20160222	The Australian National University reports enhanced photoluminescence of MoS2 grown using CVD. MoS2 is a promising material for future light sources.
20160222	The Institute of Electronic Materials demonstrates using CVD to grow graphene on silicon; such a process is necessary if graphene is ever to be used in photonics.
20160222	UCLA demonstrates growing InGaAs nanowires in an SOI platform using MOCVD as well as showing the wires to be highly tunable, and emission is strongly coupled into a waveguide, potentially overcoming multiple issues regarding growing lasers in an SOI platform.
20160222	University of Toronto creates high-efficiency quantum dot light emitting diodes in a perovskite matrix. Perovskites are another material class showing promise for photonics applications.
20160229	Technical University of Ostrava demonstrates an edge coupler with large mode size to directly interface a silicon waveguide to a cleaved fiber, without a lens.
20160301	UC San Diego demonstrates hybrid Lithium Niobate-Silicon (LN-Si) waveguide structure using only one back end of line (BEOL) step of bonding un-patterned LN.
20160304	Xi'an Jiaotong University achieves high-quality Ge growth in a CMOS (SOI) process by growing Ge on Si nanotip islands.
20160307	University College London demonstrates electrically pumped CW III-V QD lasers on silicon in a one-wafer process.
20160307	University College London demonstrates growth of InAs/GaAs quantum dot lasers on silicon (011) with extrapolated lifetimes > 100,000 hours at room temperature.
20160311	Peking University demonstrates a silicon-photonic receiver of size 1.3 mm x 1.4 mm operating at 100 Gb/s receiving polarization-division-multiplexed quadrature phase-shift keying (PDM-QPSK) transmissions.
20160311	University of Michigan demonstrates a stable, low noise polariton laser on silicon using a subwavelength grating as the top mirror to achieve single-mode operation.
20160316	In an article on optics.org University College London researchers say they have demonstrated "the first practical III-V laser monolithically and directly grown on silicon substrates"
20160316	Shanghai Jiao Tong University describes a high-extinction ratio polarization beam splitter with good tolerance to waveguide variations.
20160322	Alcatel-Lucent demonstrates a hybrid silicon-photonic laser tunable over 35 nm spectrum using vernier ring cavities.
20160322	IBM presents their CMOS9WG design kit and demonstrates it implementing a 4x25 100Gb/s transceiver.
20160322	imec shows a complete hybrid silicon photonic transceiver operating at 50 Gb/s on a single fiber
20160322	Neophotonics introduces a range of high power, uncooled lasers and laser array sources for both the 1310nm and 1550nm wavelength bands, suitable for flip-chip integration to Silicon Photonics.
20160322	PETRA Japan demonstrates 25 Gb/s error-free operation of a quantum dot laser-based transmitter, operating over a 70C temperature range.
20160324	A*STAR develops an integrated transceiver using 3D integration and Silicon Photonics as an interposer.

20160328	Peking University develops a mode converter using silicon strip-slot waveguide with 96% efficiency for polarization diversity application.
20160402	Tsinghua University demonstrates a wideband mode converter using wedge shaped transitions between waveguides of two different geometries.
20160403	University of Florence demonstrates that single wall carbon nanotubes (SWNTs) can couple to modes at the surface of silicon ring resonators to create emitters in the 1300 nm region.
20160404	UC Berkeley demonstrates a ring resonator tuning scheme of record low power and self-heating cancellation, monolithically integrated with 45 nm CMOS control logic in a single chip.
20160415	Ghent University-imec demonstrates direct modulation of a heterogeneously integrated InP/SOI DFB laser at 28 Gb/s
20160418	Karlsruhe Institute of Technology presents results of narrow band ligt emission from electrically driven carbon nanotubes coupled to a photonic crystal cavity
20160420	UC Santa Barbara demonstrates quantum dot InAs/GaAs lasers on silicon with improved thermal performance and lifetime.
20160428	Huazhong University of Science and Technology demonstrates a new type of Ge photodetector using two parallel regions giving high sensitivity and high speed up to 36 GHz.
20160504	UC Santa Barbara shows a novel 3D hybrid integrated laser design bonding an InP gain region with a mirror onto a silicon PIC with a grating coupler. Thermal performance is drastically improved.
20160505	NTT demonstrates an InGaAs photonic crystal photodetector with low power consumption of < 1fJ bit due to ultra-low capacitance and compact size.
20160513	Acacia Communications shares rise 35% after launch on NASDAQ.
20160513	University of British Columbia shows how to create schematic representations of silicon photonic circuits and then simulate performance including manufacturing tolerance via parameter variation. A design kit is provided.
20160520	A team led by UC Santa Barbara develops the first Quantum Cascade Laser on Silicon operating in the infrared, using a silicon-on-nitride-on-insulator system.
20160527	Aachen University shows a complete Silicon Photonics WDM link using a a semiconductor mode locked laser and an SOA supporting 12 multiplexed channels at 25 Gb/s error free, hybridly integrated to control electronics.
20160603	Université Paris Sud develops subwavelength fiber chip grating couplers in the 1.3 µm datacom wavelength range
20160609	IBM demonstrates a 4-channel WDM transmitter using heterogeneously integrated III-V/Silicon photonics integrated with a 32 nm CMOS driver.
20160609	Université Laval demonstrates and ultra-low power high speed PAM-8 modulator operating at 45 Gb/s using 1 fJ/bit
20160610	NTT demonstrates a lambda scale embedded active region photonic crystal (LEAP) laser on silicon with very low threshold current (57 µA)
20160610	Oracle demonstrates a hybrid III-V/Silicon comb laser using a butt-coupled III-V gain section and multiple vernier ring resonator tuners.
20160711	HP Labs uses a direct bonding of GaAs QD diode laser to silicon waveguide resulting in low-loss coupling and robust operation.
20160711	Tyndall National Institute demonstrates passive alignment and bonding of VCSELs to a silicon PIC as a low cost integrated silicon photonic solution.
20160711	University of Delaware shows that using thin film lithium niobate hybrid silicon waveguides allows increase in modulation speed from 60 GHz to 110 GHz
20160713	UC Santa Barbara demonstrates a fully integrated Silicon Photonic network on a chip including lasers, providing 8 x 8 x 40 Gb/s.
20160715	University of Toronto achieves 97% conversion of polarization using an augmented low-index-guiding scheme with silicon nitride/silicon dual-core waveguide
20160719	UC Santa Barbara demonstrates a heterogeneous III-V/Silicon semiconductor amplifier useful for lasers and other applications
20160720	University College London achieves integrated III-V lasers using MBE deposited GaAs buffer layer and InGaAs/GaAs dislocation filter layers, claiming "the first practical InAs/GaAs QD lasers monolithically grown on a Si substrate".
20160726	Technical University of Denmark demonstrates frequency comb generation using an AlGaAs on insulator platform at 1590 nm.

20160808		Tokyo Institute of Technology achieves direct modulation of an GaInAsP InP membrane DFB laser with only 1 mA bias current at 10 Gb/s.
20160808		University of Tokyo demonstrates direct modulation of a III-V quantum dot laser at room temperature and 10 Gb/s and 6 Gb/s at 60°C without any current adjustment.
20160822		Université Laval demonstrates a Mach Zehnder modulator (MZM) at 114 Gb/s for PAM-8 modulation.
20160831		IBM shows a complete packaging solution including fiber array attach and secondary (active) photonic die assembly that can be carried out with existing facilities and equipment.
20160831		In support of future 3D photonic architectures, Ain Shams University demonstrates a vertical multimode interference coupler in an SOI platform.
20160831		Oracle shows fabless design and integration concepts to produce WDM transceivers using Silicon Photonics, interposers, and III-V external cavity lasers.
20160912		HP Labs shows a new tunable microring laser which is controlled/tuned using an in-cavity MOS capacitor.
20160921		Only 3 months after reporting on their CMOS9WG design kit and a 25 Gb/s transceiver, IBM demonstrates a fully integrated 56 Gb/s silicon photonic transceiver using PAM-4 modulation
20160930		University of Maryland shows that using a silicon nitride (Si3N4/SiO2) waveguide a direct butt-coupled cleaved fiber can be used as the chip to fiber interface with over 90% efficiency with good position tolerance.
20161004		UC Santa Barbara introduce a wafer bonding approach to direct bond a silicon wafer onto a silicon nitride wafer having ultra-low loss passive structures. Subsequent chip bonding of III-V material completes an integrated active device.
20161017		UC Santa Barbara demonstrates a 3D heterogeneous integration using a turning mirror in an InP package to turn the light onto a vertical grating coupler in a Silicon Photonic package; integration is accomplished using flip-chip bonding to the silicon substrate for heat sinking.
20161026		A*STAR shows a novel hetero core microdisk laser using covalently bonded III-V to ultra-thin SiO2 and a hard-mask/deep etch process which couples light directly into waveguides and results in ultra-small (few μm diameter) devices.
20161114		In another graphene advance, UC Berkeley shows modulation of a graphene-based surface normal reflector in a CMOS compatible process.
20161114		Technical University of Denmark experimentally shows graphene nano-disk plasmons operating at 2 um, a step towards graphene-based infra-red devices.
20161115		Université Laval demonstrates a cascaded-microring based modulator operating at 60 Gb/s with PAM-4 modulation.
20161214		Startup Elenion emerged from "stealth mode" stating they have been working on Silicon Photonics for about 2 years and plan to have commercial product in 2017, addressing the $1/Gb/s market price target.

Bibliography

"2013 International Technology Roadmap for Semiconductors, Emerging Research Materials" ITRS, 3 Mar. 2014. Web. <https://www.dropbox.com/sh/qz9gg6uu4kl04vj/AADD7ykFdJ2ZpCR1LAB2XEjla?dl=0&preview=ERM_2013Tables.xls>.

"A*STAR's IME and Lumerical solutions develop a calibrated compact model library for IME's silicon Photonics platform and process design kit" A*STAR (Singapore Agency for Science, Technology, and Research). 23 Sept. 2015. Web. <https://www.a-star.edu.sg/Media/News/Press-Releases/ID/4300/ASTARs-IME-and-Lumerical-Solutions-Develop-a-Calibrated-Compact-Model-Library-for-IMEs-Silicon-Photonics-Platform-and-Process-Design-Kit.aspx>.

"A*STAR's IME kicks off consortia to develop advanced packaging solutions for next-generation Internet of things applications and high-performance wireless data transfer technologies" A*STAR (Singapore Agency for Science, Technology, and Research). 26 July 2016. Web. <https://www.a-star.edu.sg/Media/News/Press-Releases/ID/4831.aspx>.

"About PhotonIC Corp. Commercializing photonic integrated circuits (PICs) for optical networks" photonic-corp.com. 15 Aug. 2016. Web. <http://www.photonic-corp.com/what-we-do.htm>.

"ACACIA COMMUNICATIONS, INC. (ACIA) IPO" Nasdaq. NASDAQ.com, 31 May 2016. Web. <http://www.nasdaq.com/markets/ipos/company/acacia-communications-inc-982199-80038>.

"Active optical cables continue to ramp while embedded optical module road still bumpy" LightCounting Market Research. Marketwire, 21 Dec. 2016. Web. <http://www.marketwired.com/press-release/active-optical-cables-continue-ramp-while-embedded-optical-module-road-still-bumpy-2184871.htm>.

"Analog Photonics: Silicon Photonics Design and Fabrication" analogphotonics.com. Analog Photonics, Web. 15 Aug. 2016. <http://www.analogphotonics.com/>.

"AppliedMicro, MACOM and BrPhotonics demonstrate the world's First 56 Gigabaud (100Gb/s) PAM-4 over single wavelength solution that enables 100Gb/s and 400Gb/s Connectivity in a QSFP family of Transceivers" Omar Hassen. Globe Newswire, 19 Sept. 2016. Web. <https://globenewswire.com/news-release/2016/09/19/872640/0/en/AppliedMicro-MACOM-and-BrPhotonics-Demonstrate-the-World-s-First-56-Gigabaud-100Gb-s-PAM-4-over-Single-Wavelength-Solution-that-Enables-100Gb-s-and-400Gb-s-Connectivity-in-a-QSFP-F.html>.

"Ayar Labs Gets $2.5M to Go After Optical Chips for Data Centers" investorshub.advfn.com. Investors Hub, 16 Aug. 2016. Web. <http://investorshub.advfn.com/boards/read_msg.aspx?message_id=124573287>.

"Breakthrough light-based microprocessor chip could lead to more powerful computers, network infrastructure" CU Boulder Today. University of Colorado, 23 Dec. 2015. Web. <http://www.colorado.edu/today/2015/12/23/breakthrough-light-based-microprocessor-chip-could-lead-more-powerful-computers-network>.

"China's Silicon Photonics Alliance kicks off in Shanghai - Le Cordacord - focus on the fiber optics industry" Zhendong Li. cordacord.com, 28 June 2016. Web. <http://www.cordacord.com/news_view.php?id=20160628041530>.

"CIAN -- Silicon Photonics Manufacturing" Web: The University of Arizona, 25 Sept. 2015. Web. <http://cian-erc.webhost.uits.arizona.edu/silicon-photonics-manufacturing-0>.

"ColorChip Shipping 100G QSFP28 10Km Transceivers" Noa Kotok. PR Newswire, 19 Sept. 2016. Web. <http://www.prnewswire.com/news-releases/colorchip-shipping-100g-qsfp28-10km-transceivers-300329957.html>.

"Corning and Intel collaborate on next-generation silicon Photonics Connectivity" www.corning.com. 4 Sept. 2013. Web. <http://www.corning.com/worldwide/en/products/communication-networks/news-events/news-releases/2013/09/opcomm_nafta_en_news_events_news_releases_2013_2013090401.html>.

"Doors open at new silicon photonics foundry" University of Washington. SPIE, 3 Feb. 2011. Web. <http://optics.org/news/2/1/28>.

"EFFECT Photonics demos 500-Gbps PAM4 TOSA" EFFECT Photonics. lightwaveonline, 19 Sept. 2016. Web. <http://www.lightwaveonline.com/articles/2016/09/effect-photonics-demos-500-gbps-pam4-tosa.html>.

"Electrical engineers break power and distance barriers for fiber optic communication" Nikola Alic. UC San Diego, 25 June 2014. Web. <http://jacobsschool.ucsd.edu/news/news_releases/release.sfe?id=1768>.

"Elenion unveiled as a silicon photonics PIC company" Larry Schwerin. gazettabyte, 27 Dec. 2016. Web. <http://www.gazettabyte.com/home/2016/12/27/elenion-unveiled-as-a-silicon-photonics-pic-company.html>.

"Enterprise spend down - Cisco on top" Synergy Research. 5 Jan. 2017. Web. <http://www.globaltelecomsbusiness.com/article/3650437/Enterprise-spend-down-Cisco-on-top.html#.WHJ0w_krJEY>.

"ePIXfab silicon photonics: Mission, rationale and history" epixfab.eu. web: The European Silicon Photonics Alliance, 26 Mar. 2016. Web. <http://epixfab.eu/index.php/epixfab-2/history>.

"Ethernet industry collaborating on next phase of epic migration to 25Gb, 50Gb and 100Gb" 2550100 Alliance. 2550100.com, 14 Apr. 2015. Online. <http://2550100.com/news/ethernet-industry-collaborating-on-next-phase-of-epic-migration-to-25gb-50gb-and-100gb/>.

"Europractice Silicon Photonics MPW offer" web: Europractice, 15 July 2016. Web. <http://www.europractice-ic.com/SiPhotonics_general.php>.

"Facebook DataCenter, servers and infrastructure FAQ" Facebook. Data Center Knowledge, 16 Sept. 2016. Web. <http://www.datacenterknowledge.com/the-facebook-data-center-faq/>.

"Finisar chairman plays down silicon photonics "threat"" optics.org. 12 Mar. 2013. Web. <http://optics.org/news/4/3/15>.

"Finisar First to publically demonstrate complete end-to-end 50 Gb/s optical interface using silicon Photonics at ECOC 2014 (NASDAQ: FNSR)" finisar.com. Finisar, 22 Sept. 2014. Web. <http://investor.finisar.com/releasedetail.cfm?releaseid=871808>.

"Global market for Photonic integrated circuit technology to reach nearly $866 Million in 2018; optical signal processing moving at 35% CAGR" BCC Research. PR Web, 15 Apr. 2014. Web. <http://www.prweb.com/releases/2014/04/prweb11764528.htm>.

"Global Wafer Capacity 2017-2021" IC Insights, 9 Jan. 2017. Web. <http://www.icinsights.com/data/reports/4/6/brochure.pdf?parm=1483973739>.

"Graphene highly efficient at converting light to electricity" ICFO. Photonics Media, 25 Feb. 2013. Web. <http://www.photonics.com/Article.aspx?AID=53131>.

"Graphene on chip closing the gap with germanium" Columbia University, MIT, IBM T.J. Watson Research Center. Photonics Meida, 17 Sept. 2013. Web. <http://www.photonics.com/Article.aspx?AID=54911>.

"Hybrid single quantum well InP/Si nanobeam lasers for silicon photonics" Optics Letters 38.22 (15 Nov. 2013): 4656–4658. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-38-22-4656>.

"IBM sets data transfer record in Multimode optical fiber" eetiimes.com. EETimes, 27 Feb. 2014. Web. <http://www.eetimes.com/document.asp?doc_id=1321203>.

"Intel, FB team to move Photonics into data centers" Intel, Facebook. Photonics Media, 17 Jan. 2013. Web. <http://www.photonics.com/Article.aspx?AID=52805>.

"Intel, UC Santa Barbara develop world's First hybrid silicon laser" Intel. Intel, 18 Sept. 2006. Web. <http://www.intel.com/pressroom/archive/releases/2006/20060918corp.htm?wapkw=hybrid+silicon+laser>.

"Interconnect market (8%) and silicon Photonics (27%) growth forecasts in new research reports" PRNewswire. MarketWatch, 11 Aug. 2015. Web. <http://www.marketwatch.com/story/interconnect-market-8-and-silicon-photonics-27-growth-forecasts-in-new-research-reports-2015-08-11-220312>.

"International Technology Roadmap for Semiconductors, 2013 Edition, Emerging Research Materials" Semiconductor Industry Association (SIA), 2013. Web. <https://www.dropbox.com/sh/6xq737bg6pww9gq/AACQWcdHLffUeVloszVY6Bkla?dl=0>.

"Is Silicon Photonics Real?" LightCounting, 14 Feb. 2013. WEb. <http://www.lightcounting.com/News_021413.cfm>.

"Juniper networks to acquire Aurrion for $165 million" Juniper Networks. Gazettabyte, 8 Aug. 2016. Web. <http://www.gazettabyte.com/home/2016/8/8/juniper-networks-to-acquire-aurrion-for-165-million.html>.

"Kaiam launches new LightScale platform at ECOC" Derek Milne. Business Wire, 15 Sept. 2016. Weg. <http://www.businesswire.com/news/home/20160915005227/en/Kaiam-Launches-LightScale-Platform-ECOC>.

"KfW invests in Sicoya" Sicoya, 4 Nov. 2016. Web. <http://sicoya.com/2016/11/04/kfw-invests-in-sicoya/>.

"Leti Announces H2020 Project to Develop Si-photonics-based Transceivers for Low-cost, High-speed Data Communications" Leti. Leti, 21 Nov. 2016. Web. <http://www.Leti.fr/en/Press/Press-releases>.

"LightCounting Shares Research Notes from NGON Conference" LightCounting. lightcounting.com, 20 Oct. 2016. Web. <http://www.lightcounting.com/News_102016.cfm>.

"Low-latency data center and financial networking" Infinera, 30 Nov. 2015. Web. <https://www.infinera.com/wp-content/uploads/2015/11/Arista-Infinera-Low-Latency-Application-Brief.pdf>.

"Luxtera Inc. Announces world's First 10Gbit CMOS Photonics platform; ground-breaking technology delivers affordable integration of high-speed optical interfaces in high volume CMOS chips" luxtera.com. 28 Mar. 2005. Web. <http://www.luxtera.com/luxtera/2005328LuxteraWorldsFirst10GbitCMOSPhotonicsPlatform.pdf>.

"Luxtera ships One millionth silicon Photonic Transceiver product" Luxtera. SPIE (optics.org), 19 Sept. 2016. Web. <http://optics.org/press/3356>.

"Macom, AOI to collaborate on 100G data Transceivers" Macom. 28 Jan. 2016. Web. <http://www.photonics.com/Article.aspx?AID=58251>.

"Mario Paniccia: We are just at the beginning" (gazettabyte). 23 May 2016, <http://www.gazettabyte.com/home/2016/5/23/mario-paniccia-we-are-just-at-the-beginning.html>.

"Market Opportunities for Optical Integration Technologies" LightCounting, 29 Jan. 2016. Web. <http://www.lightcounting.com/News_012916.cfm>.

"Marlin Equity partners unveils Elenion technologies, A company focused on driving innovation in silicon Photonics" Peter Spasov. 14 Dec. 2016. Web. <http://www.photonicsonline.com/doc/marlin-equity-partners-unveils-elenion-company-focused-silicon-photonics-0001>.

"Mellanox Launches 25 Gb/s Ethernet SFP28 Optical Transceivers and Active Optical Cables for Data Center Networks" Mellanox. Business Wire, 5 Sept. 2016. Web. <http://www.businesswire.com/news/home/20160905005107/en/Mellanox-Launches-25-Gbs-Ethernet-SFP28-Optical>.

"MicroQSFP (Overview)" microqsfp.com. web: microQSFP MSA Group, 14 Jan. 2016. Web. <http://www.microqsfp.com/>.

"MicroQSFP: Twelve leading global networking companies join forces to define µQSFP for next generation data communications" micro QSFP. 31 July 2015. Web. <http://www.microqsfp.com/press-releases/twelve-leading-global-networking-companies-join-forces-define-uqsfp-next-generation-data-communications/>.

"NeoPhotonics introduces high power DFB lasers for 100G silicon Photonics applications" LouVan Communications. Business Wire, 22 Mar. 2016. Web. <http://www.businesswire.com/news/home/20160322005452/en/NeoPhotonics-Introduces-High-Power-DFB-Lasers-100G>.

"NeoPhotonics' (NPTN) CEO Tim Jenks on Q1 2016 Results - Earnings Call Transcript" NeoPhotonics. Seeking Alpha, 28 Apr. 2016. Web. <http://seekingalpha.com/article/3969277-neophotonics-nptn-ceo-tim-jenks-q1-2016-results-earnings-call-transcript?part=single>.

"New silicon photonics service provides innovators with a proven path to prototyping" cmc.ca. 17 Dec. 2015. Web. <http://www.cmc.ca/en/NewsAndEvents/NewsReleases/NewsReleases/IME.aspx>.

"Newest member of national manufacturing institute" John Maggiore. Infinera, 19 Oct. 2016. Web. <https://www.infinera.com/newest-member-national-manufacturing-institute/>.

"Oclaro showcases products to accelerate transition to 100-400Gb/s single-mode fiber networks" Oclaro. semiconductor Today, 17 Mar. 2006. Web. <http://www.semiconductor-today.com/news_items/2016/mar/oclaro_170316.shtml>.

"Path to 400G" Fujitsu Network Communications Inc., 18 Dec. 2014. Web. <https://www.fujitsu.com/us/Images/Pathto400G.pdf>.

"Perovskite Nanowires yield efficient, Tunable lasers" Song Jin. Photonics Media, 13 Apr. 2015. Web. <https://www.photonics.com/Article.aspx?AID=57348>.

"Photonic Integrated Circuit (IC) & Quantum Computing Market-By Application, Integration, Components, Raw Materials & Geography to 2022" Research and Markets. PR Newswire, 24 July 2013. Web. 30 July 2016. <http://www.prnewswire.com/news-releases/photonic-integrated-circuit-ic--quantum-computing-market-by-application-integration-components-raw-materials--geography-to-2022-216787591.html>.

"Photonic integrated circuit market to grow at 25.3% CAGR to $1.3bn in 2022" semiconductor-today.com. 17 Nov. 2015. Web. <http://www.semiconductor-today.com/news_items/2015/nov/transparency_171115.shtml>.

"Photonic Integrated Circuits, A Technology and Application Primer" Infinera, 31 Aug. 2015. Web. <https://www.infinera.com/wp-content/uploads/2015/08/Photonic_Integrated_Circuits.pdf>.

"Press release: IRT Nanolec Project Integrates Laser Directly on Silicon with a Modulator" ofcconference.org. 18 Mar. 2016. Web. <http://www.ofcconference.org/en-us/home/news-and-press/exhibitor-press-releases/good-afternoon-everyone-the-papers-you-requested/>.

"Q&A with photonics pioneer, Richard Soref - part 1" 26 Jan. 2015. Web. <http://www.gazettabyte.com/home/2015/1/26/qa-with-photonics-pioneer-richard-soref-part-1.html>.

"Q&A with Richard Soref - final part" gazettabyte. 27 Jan. 2015. Web. <http://www.gazettabyte.com/home/2015/1/27/qa-with-richard-soref-final-part.html>.

"Reliable laser on silicon shows photonic integration potential" University College London. SPIE, 16 Mar. 2016. Web. <http://optics.org/news/7/3/20>.

"Richard Soref: The new frontiers of silicon photonics" gazettabyte. 17 June 2016. Web. <http://www.gazettabyte.com/home/2016/6/17/richard-soref-the-new-frontiers-of-silicon-photonics.html>.

"RMIT announces a Turnkey Service for passive Silicon Photonic device prototyping" Luceda. Luceda, 20 Dec. 2016. Web. <http://www.lucedaphotonics.com/en/news/australian-silicon-photonics>.

"Rockley Photonics' Rickman reveals plan for faster data centers" Andrew Rickman. 23 Sept. 2016. Web. <http://optics.org/news/7/9/28>.

"Sampling of Silicon Photonics Acquisitions" Yole Developpment, 28 June 2014. Web. <http://www.yole.fr/iso_album/illustration_sampling_of_silicon_photonics_acquisitions_yole_developpement_june_2014_2.jpg>.

"Shaping the future of optical transceivers: UGent and imec launch silicon photonics spin-off Caliopa" Karsten Verhaegen. Huawei, 25 Sept. 2010. Web. <http://www.caliopa.com/news-and-events/article/ugent-and-imec-launch-silicon-photonics-spin-off-caliopa>.

"SI - CMOS COMPATIBLE PHOTONICS IC PLATFORM" A*STAR, Institute of Microelectronics, 18 Oct. 2007. Web. <https://www.a-star.edu.sg/ime/RESEARCH/NANO-PHOTONICS-PROGRAMME/si_cmos_compatible_photonics_integrated_circuits_platform.aspx>.

"Sicoya wins European Photonics startup challenge" Dr. Torsten Fiegler. 19 Oct. 2016. Web. <http://optics.org/news/7/10/28>.

"Silicon chip with integrated laser: Light from a nanowire" Walter Schottky. phys.org, 11 Feb. 2016. Web. <http://phys.org/news/2016-02-silicon-chip-laser-nanowire.html>.

"Silicon Nanophotonic packaging" IBM, 4 Dec. 2015. Web. <http://researcher.watson.ibm.com/researcher/view_group.php?id=5517>.

"Silicon Photonics - from promise to reality in datacentres" Jose Pozo, Director of Technology, EPIC. Compound Semiconductor, 28 Jan. 2016. Web. <https://www.compoundsemiconductor.net/article/98599-silicon-photonics--from-promise-to-reality-in-datacentres.html>.

"Silicon Photonics 2014" Yole Developpement, 23 June 2014. Web. <http://www.slideshare.net/Yole_Developpement/yole-silicon-photonicsjune2014sample>.

"Silicon Photonics and optical integration" Communication Industry Researchers, 30 Apr. 2007. Web. <http://www.photonteck.com/upfile/2014/05/27/20140527171759_270.pdf>.

"SILICON PHOTONICS FOR DATA CENTERS AND OTHER APPLICATIONS 2016" Yole Developpement, Oct. 2016. Web. <http://www.i-micronews.com/images/Flyers/MEMS/Yole_Silicon_photonics_for_data_centers_and_other_applications_2016_flyer_web.pdf>.

"Silicon Photonics Market Analysis: By Components and By Application (Aerospace & Defense, Healthcare, Telecommunications, Consumer Electronics, Industrial Automation and Others) - With Forecast (2016-2021)" ResearchandMarkets, 12 Jan. 2016. Web. <http://www.researchandmarkets.com/publication/mihtlop/3820803>.

"Silicon Photonics market by component - global forecast to 2022" Dublin, Ireland: ResearchandMarkets, 29 June 2016. Web. <http://www.researchandmarkets.com/reports/3771365/silicon-photonics-market-by-component-global>.

"Silicon photonics market expected to triple in next 5 years" semiconductortoday.com. 2012. Web. <http://www.semiconductor-today.com/news_items/2012/SEP/YOLE_270912.html>.

"Silicon Photonics market worth $410.78 Million by 2020" MarketsandMarkets. PR Newswire, 23 Jan. 2014. Web. <http://www.prnewswire.com/news-releases/silicon-photonics-market-worth-41078-million-by-2020-241636161.html>.

"Silicon Photonics Market", Undisclosed Market Research Professional. 2 June 2014.

"Silicon photonics: Automated packaging and testing" Physics World 2015.June (21 May 2015): <http://live.iop-pp01.agh.sleek.net/physicsworld/reader/#!edition/editions_optics-2015/article/page-7888>.

"Silicon Photonics" PLC Connections. 15 Jan. 2016. Web. <http://www.plcconnections.com/silicon.html>.

"Silicon photonics-imec" imec. 2012. Web. <http://www2.imec.be/be_en/services-and-solutions/silicon-photonics.html>.

"Silicon technology - 100G optical components, coherent, PIC, DWDM" neophotonics.com. web: NeoPhotonics, 22 Mar. 2016. Web. <https://www.neophotonics.com/technology/silicon/>.

"Strain-engineered Direct Gap Ge SnxGe1-x Heterodiode and Multi Quantum Well Photodetectors, Laser, Emitters and Modulators Grown on SnySizGe1-y-z Buffered Silicon" United States Patent: United States of America represented by the Secretary of the Air Force, 24 May 2005. Web. <http://pdfpiw.uspto.gov/.piw?PageNum=0&docid=06897471>.

"SystemOnGlass optical communications firm ColorChip raises a further $20m" ColorChip. semiconductor-today, 17 Aug. 2016. Web. <http://www.semiconductor-today.com/news_items/2016/aug/colorchip_170816.shtml>.

"The ecosystem for silicon photonics starts to take shape" gazettabyte. 26 July 2016. Web. <http://www.gazettabyte.com/home/2016/7/26/the-ecosystem-for-silicon-photonics-starts-to-take-shape.html>.

"The silicon photonics industry is ready for take-off. Objective: a multibillion dollar market" web: Yole Developpement, 8 Nov. 2016. Web. <http://www.yole.fr/SiliconPhotonics_Market_Applications.aspx#.WEyuSPkrJEZ>.

"Thirteen industry leaders collaborate to increase Pluggable module speeds to 400 Gbps" QSFP-DD MSA Group. Business Wire, 21 Mar. 2016. Web. <http://www.businesswire.com/news/home/20160321005276/en/Thirteen-Industry-Leaders-Collaborate-Increase-Pluggable-Module>.

"VTT and PhoeniX software develop kit for Si-photonics developers" optics.org, 1 Sept. 2016. Web. 21 Nov. 2016. <http://optics.org/news/7/8/52>.

"Web hosting servers - dedicated web servers for local applications" hp.com. Hewlett Packard Enterprise, 17 Aug. 2015. Web. <http://www8.hp.com/us/en/products/servers/moonshot/web.html>.

"Will 200GbE be the Real Successor to 100GbE?" IEEE. LightCounting, 10 Nov. 2016. Web. <http://www.lightcounting.com/News_111016.cfm>.

"World silicon Photonics market - opportunities and forecasts, 2014 - 2022" Dublin, Ireland: ResearchandMarkets, 16 Oct. 2016. Web.

<http://www.researchandmarkets.com/reports/3773416/world-silicon-photonics-market-opportunities>.

"Worldwide server market revenues increase 5.2% in the fourth quarter as demand in china once again drives the market forward, according to IDC" IDC. www.idc.com, 9 Mar. 2016. Web. <https://www.idc.com/getdoc.jsp?containerId=prUS41076116>.

Abbasi, Amin, et al. "28 Gb/s Direct Modulation Heterogeneously Integrated C-Band InP/SOI DFB Laser" Optics Express 23.20 (1 Oct. 2015): 26479–26485. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-20-26479>.

Abbasi, Amin, et al. "High Speed Direct Modulation of a Heterogeneously Integrated InP/SOI DFB Laser" Journal of Lightwave Technology 34.8 (15 Apr. 2015): 1683–1687. <http://ieeexplore.ieee.org/document/7384673/?tp=&arnumber=7384673>

Absil, Philippe P, et al. "Silicon Photonics Integrated Circuits: A Manufacturing Platform for High Density, Low Power Optical I/O's" Optics Express 23.7 (6 Apr. 2015): 9369–9378. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-7-9369>.

Agazzi, Laura, et al. "Monolithic Integration of Erbium-Doped Amplifiers with Silicon-on-Insulator Waveguides" Optics Express 18.26 (20 Dec. 2010): 27703–27711. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-18-26-27703>.

Akiyama, Tomoyuki, et al. "A Novel Transmitter Leveraging High-Speed Ultralow-Power Modulation of a Si Microring Modulator by Eliminating Tuning Power" Optical Fiber Communication Conference (20 Mar. 2016): 2–4. <https://www.osapublishing.org/abstract.cfm?uri=OFC-2016-M2C.4>.

Alain, Christine. "Silicon Photonics packaging" ino.ca. web: INO, 14 Feb. 2016. Web. <http://www.ino.ca/en/technologies/silicon-photonics/silicon-photonics-packaging/?gclid=CjwKEAjwlZa9BRCw7cS66eTxlCkSJAC-ddmwbX1z_Cfv3kiioZIs2mPjkHqti4hxu-4VWDWWGM9N-xoCKy3w_wcB>.

Alloatti, L., and R. J. Ram. "Infrared Vertically-Illuminated Photodiode for Chip Alignment Feedback" AIP Advances 6.8 (27 June 2016): 085219. <https://arxiv.org/abs/1606.08870>.

Amkor Technology, Inc. "Amkor technology: Amkor and cadence to develop packaging assembly design kits for Amkor's SLIM and SWIFT packaging technologies" Aamkor.com. 3 May 2016. Web. <http://www.amkor.com/index.cfm?objectid=A8CD2213-CBB2-E8AD-90896203041736A7>.

Anderson, S. P., and M. Webster. "Silicon Photonic Polarization-Multiplexing Nanotaper for Chip-to-Fiber Coupling" Journal of Lightwave Technology 34.2 (15 Jan. 2015): 372–378. <http://ieeexplore.ieee.org/document/7327128/?tp=&arnumber=7327128>

Andreyev, Alexy. "Introducing Data Center Fabric, the Next-Generation Facebook Data Center Network" Facebook. code.facebook.com, 14 Nov. 2014. Web. <https://code.facebook.com/posts/360346274145943/introducing-data-center-fabric-the-next-generation-facebook-data-center-network/>.

Antelius, Mikael, Kristinn B Gylfason, and Hans Sohlström. "An Apodized SOI Waveguide-to-Fiber Surface Grating Coupler for Single Lithography Silicon Photonics" Optics Express 19.4 (14 Feb. 2011): 3592–3598. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-19-4-3592>.

Anthony, Sebastian. "Intel Forges Ahead to 10nm, Will Move Away from Silicon at 7nm" ars Technica. Ars Technica, 23 Feb. 2015. Web. <http://arstechnica.com/gadgets/2015/02/intel-forges-ahead-to-10nm-will-move-away-from-silicon-at-7nm/>.

Assefa, Solomon, et al. "A 90nm CMOS Integrated Nano-Photonics Technology for 25Gbps WDM Optical Communications Applications" Electron Devices Meeting (IEDM) 2012. (13 Oct. 2012): <https://www.infona.pl/resource/bwmeta1.element.ieee-art-000006479162>.

Atsumi, Yuki, et al. "Interlayer Polarization Beam Splitter Based on Asymmetrical Si Wire Directional Coupler" IEEE Photonics Technology Letters 28.14 (15 July 2015): 1545–1548. 25 July 2016. <http://ieeexplore.ieee.org/document/7458852/?tp=&arnumber=7458852>

Autere, A., et al. "Slot Waveguide Ring Resonators Coated by an Atomic Layer Deposited Organic/inorganic Nanolaminate" Optics Express 23.21 (5 Oct. 2015): 26940. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-21-26940&origin=search>.

Babcock, Charles. "Facebook Builds Next-Gen Data Center in Ireland" Information Week. Information Week, 28 Jan. 2016. Online. <http://www.informationweek.com/data-centers/facebook-builds-next-gen-data-center-in-ireland/d/d-id/1324080>.

Babcock, Charles. "Facebook's Data Center: Where Likes Live" NetworkComputing. Network Computing, 28 Feb. 2013. Online. <http://www.networkcomputing.com/data-centers/facebooks-data-center-where-likes-live/1079860267/page/0/2?itc=edit_in_body_cross>.

Baek, Jiwoong, et al. "Phosphorus Implantation into in Situ Doped Ge-on-Si for High Light-Emitting Efficiency" Optical Materials Express 6.9 (1 Sept. 2016): 2939–2946. <https://www.osapublishing.org/ome/abstract.cfm?uri=ome-6-9-2939>.

Baker, Christipher G., et al. "High Bandwidth on-Chip Capacitive Tuning of Microtoroid Resonators" Optics Express 24.18 (5 Sept. 2016): 20400–20412. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-18-20400>.

Bakish, I, et al. "Self-Assembled Monolayer Assisted Bonding of Si and InP" Optical Materials Express 2.8 (1 Aug. 2012): 1141–1148. <https://www.osapublishing.org/ome/abstract.cfm?uri=ome-2-8-1141>.

Barwicz, Tymon, et al. "A Novel Approach to Photonic Packaging Leveraging Existing High-Throughput Microelectronic Facilities" IEEE Journal of Selected Topics in Quantum Electronics (20 July 2016): <http://ieeexplore.ieee.org/document/7517347/?tp=&arnumber=7517347>

Barwicz, Tymon, et al. "Demonstration of Self-Aligned Flip-Chip Photonic Assembly with 1.1dB Loss and >120nm Bandwidth" OSA Technical Digest Frontiers in Optics.2016 (22 Oct. 2016): 3–5. <https://www.osapublishing.org/abstract.cfm?uri=FiO-2016-FF5F.3>.

Barwicz, Tymon, et al. "Enabling Large-Scale Deployment of Photonics Through Cost-Efficient and Scalable Packaging" 2015 IEEE 12th International Conference on Group IV Photonics (GFP) (25 Aug. 2015): <http://researcher.watson.ibm.com/researcher/files/us-tymon/GFP2015_plenary_slides_20150825.pdf>.

Barwicz, Tymon, et al. "An O-band Metamaterial converter Interfacing standard optical fibers to silicon Nanophotonic Waveguides" Yorktown Heights, NY: IBM, 26 Mar. 2015. Web. <http://researcher.watson.ibm.com/researcher/files/us-tymon/OFC2015_fiber_packlite_optical_20141013b_corr.pdf>.

Barwicz, Tymon, et al. "Optical Demonstration of a Compliant Polymer Interface Between Standard Fibers and Nanophotonic Waveguides" Yorktown Heights, NY: IBM, 26 Mar. 2015. Web. <http://researcher.watson.ibm.com/researcher/files/us-tymon/OFC2015_Polymer_Exp_Optical_20141013b.pdf>.

Barwicz, Tymon, et al. "Photonic Packaging in High-Throughput Microelectronic Assembly Lines for Cost-Efficiency and Scalability" Yorktonwn Heights, NY: IBM, 19 Dec. 2014. Web. <http://researcher.watson.ibm.com/researcher/files/us-tymon/OFC2015_Symposium_20141219.pdf>.

Baudot, Charles, et al. "Advanced R&D Perspectives Of Silicon Photonics @ STMicroelectronics" CEA-Leti, 21 May 2013. Web. <(no longer available)>.

Bautista, Jerry, Michael Morse, and Jeffrey Swift. "Microphotonics: Hardware for the Information Age" MIT Microphotonics Center, 18 May 2005. Web. <https://mphotonics.mit.edu/docman/ctr/ctr-1/294-5-ctr2005-silicon/file>.

Bayram, C, et al. "Gallium Nitride on Silicon for Consumer and Scalable Photonics" Proceedings of the SPIE 8631.February 2013 (4 Feb. 2013): 863112. <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=1568447>.

Bedard, K., et al. "Dual Phase-Shift Bragg Grating Silicon Photonic Modulator Operating up to 60 Gb/s" Optics Express 24.3 (8 Feb. 2016): 2413–2419. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-3-2413>.

Benedikovic, Daniel, et al. "Single-Etch Subwavelength Engineered Fiber-Chip Grating Couplers for 1.3 μm Datacom Wavelength Band" Optics Express 24.12 (13 June 2016): 12893–12904. 14 June 2016. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-12-12893>.

Berhane, Amanuel M, et al. "Electrical Excitation of Silicon-Vacancy Centers in Single Crystal Diamond" Applied Physics Letters106.17 (27 Apr. 2015): 171102. <https://arxiv.org/abs/1503.04778>.

Bernabé, S., et al. "HIGH DATA RATE SILICON PHOTONIC - CMOS ELECTRONIC MODULES USING COPPER MICROBUMPS High Data Rate Silicon Photonic - CMOS Electronic Modules Using Copper Bumps" International Symposium on Microelectronics 2015.1 (Nov. 2015): 000616–000620. <http://www.imapsource.org/doi/abs/10.4071/isom-2015-THA34>.

Bernhardi, E. H., et al. "Highly Efficient, Low-Threshold Monolithic Distributed-Bragg-Reflector Channel Waveguide Laser in Al_2O_3: Yb^3+" Optics Letters 36.5 (17 Feb. 2011): 603. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-36-5-603>.

Bernhardi, E. H., et al. "Ultra-Narrow-Linewidth, Single-Frequency Distributed Feedback Waveguide Laser in Al_2O_3: Er^3+ on Silicon" Optics Letters35.14 (8 July 2010): 2394. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-35-14-2394>.

Biccari, F., et al. "Single Walled Carbon Nanotubes Emission Coupled with a Silicon Slot-Ring Resonator" Journal of Luminescence (21 Nov. 2016): n.pag. <http://www.sciencedirect.com/science/article/pii/S0022231316309462>.

Bjorlin, Alexis. "Data Center Day: A Silicon Photonics Update" Santa Clara, CA: Intel, 2015. Web. <http://files.shareholder.com/downloads/INTC/0x0x848159/6DF9CEFD-05A3-43D5-864B-1838ED939466/Data_Center_Day_SiPh_Final_BJORLIN_nn.pdf>.

Black, Doug. "EBay's Liquid Cooled Billion-Transactions-a-Day Data Center" Slider: Datacenter. EnterpriseTech, 29 June 2016. Web. <http://www.enterprisetech.com/2016/06/29/ebays-billion-daily-transactions-cooled-water/>.

Blair, Katie. "Luxtera Debuts 1310nm 100G-PSM4 QSFP28 Module and Silicon Photonics Chipset at OFC 2015" Luxtera. 23 Mar. 2015. Web. <http://www.luxtera.com/luxtera/LuxteraOFC2015PressRelease2232015.pdf>.

Blyler, John. "Embedded Intel® - Silicon Photonics Links Traditional ICs" embeddedintel.com. 15 Apr. 2001. Web. <http://www.embeddedintel.com/from_intel.php?article=1943>.

Boeck, Robert, et al. "Experimental Performance of DWDM Quadruple Vernier Racetrack Resonators" Optics Express 21.7 (4 Apr. 2013): 9103. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-21-7-9103>.

Boeuf, F., et al. "Recent Progress in Silicon Photonics R&D and Manufacturing on 300mm Wafer Platform" Optical Fiber Communications Conference and Exhibition OFC 2015. (26 Mar. 2015): <http://ieeexplore.ieee.org/document/7122015/?tp=&arnumber=7122015>

Boeuf, F., et al. "Silicon Photonics R&D and Manufacturing on 300-Mm Wafer Platform" Journal of Lightwave Technology 34.2 (15 Jan. 2015): 286–295. <http://ieeexplore.ieee.org/document/7274648/?tp=&arnumber=7274648>

Bogaerts, Wlm, et al. "Co-Integration of Photonic Devices on a Silicon Photonics Platform" United States Patent: IMEC, Universiteit Gent, 3 June 2014. Web. <http://pdfpiw.uspto.gov/.piw?PageNum=0&docid=08741684>.

Bovington, Jock, et al. "III-V/Si Tunable Vernier-Ring Flexible Grid Comb Laser" Conference on Lasers and Electro-Optics (10 June 2016): <https://www.osapublishing.org/abstract.cfm?uri=CLEO_SI-2016-JTh4C.2>.

Bovington, Jock, et al. "III-V/Si Vernier-Ring Comb Lasers (VRCLs)" IEEE Journal of Selected Topics in Quantum Electronics (1 Aug. 2016): 1–1. <http://ieeexplore.ieee.org/document/7590006/?tp=&arnumber=7590006>

Bowers, John E. "Heterogeneous III-V / Si Photonic Integration" Conference on Lasers and Electro-Optics 2016. (5 June 2016): <https://www.osapublishing.org/abstract.cfm?URI=cleo_si-2016-SM1G.1>.

Bowers, John E., et al. "High-Gain High-Sensitivity Resonant Ge/Si APD Photodetectors" Infrared Technology and Applications XXXVI (23 Apr. 2010): <http://spie.org/Publications/Proceedings/Paper/10.1117/12.855030>.

Boyle, W S. "Light-Wave Communications [Reprint]" Scientific American 6 Oct. 2009: Web. <http://www.scientificamerican.com/article/light-wave-communications/>.

Bradley, J. D. B., and M. Pollnau. "Erbium-Doped Integrated Waveguide Amplifiers and Lasers" Laser & Photonics Reviews 5.3 (29 Dec. 2010): 368–403. <http://onlinelibrary.wiley.com/doi/10.1002/lpor.201000015/abstract>.

Bradley, J. D. B., et al. "Waveguide amplifiers on a silicon chip" KTH Kista. 8 Jan. 2016. Web. <https://www.kth.se/en/ict/forskning/mnf/fotonik/relid/waveguide-amplifiers>.

Bradley, Jonathan D. B., et al. "Monolithic Erbium- and Ytterbium-Doped Microring Lasers on Silicon Chips" Opt. Express 22.10 (13 May 2014): 12226. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-22-10-12226>.

Bretos, Iñigo, et al. "Active Layers of High-Performance Lead Zirconate Titanate at Temperatures Compatible with Silicon Nano- and Microelecronic Devices" Scientific Reports 6. (3 Feb. 2016): 20143. <http://www.nature.com/articles/srep20143>.

Brimont, A., et al. "High Speed Silicon Electro-Optical Modulators Enhanced via Slow Light Propagation" Optics Express 19.21 (10 Oct. 2011): 20876–20885. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-19-21-20876&origin=search>.

Bryant, Diane. "Investor Meeting, 2015 Santa Clara" Santa Clara, CA: Intel, 19 Nov. 2015. Web. <http://files.shareholder.com/downloads/INTC/1116755691x0x862746/B63C5999-58CD-411E-A2C6-F9D9DF343CAA/2015_InvestorMeeting_Diane_Bryant_WEB.pdf>.

Buca, Dan, et al. "Direct Bandgap GeSn Alloys for Laser Application" OSA Technical Digest (online) (Optical Society of America, 2015) (27 June 2015): 1–4. <https://www.osapublishing.org/abstract.cfm?uri=iprsn-2015-IM4B.1>.

Budd, Russell A., et al. "Semiconductor Optical Amplifier (SOA) Packaging for Scalable and Gain-Integrated Silicon Photonic Switching Platforms" 2015 IEEE 65th Electronic Components and Technology Conference (ECTC) (29 May 2015): <http://ieeexplore.ieee.org/document/7159762/?tp=&arnumber=7159762>

Burt, Jeffrey. "Dell brings water-cooling system to Hyperscale data centers" eweek. QuinStreet enterprise, 2 June 2016. Web. <http://www.eweek.com/servers/dell-brings-water-cooling-system-to-hyperscale-data-centers.html>.

Business Wire. "Global Silicon Photonics Market 2016-2020 with Luxtera & Mellanox Technologies Dominating - Research and Markets" Business Wire. Google+, 18 Aug. 2016. Web. <http://www.businesswire.com/news/home/20160818005474/en/Global-Silicon-Photonics-Market-2016-2020-Luxtera-Mellanox>.

Cardenas, Jaime, et al. "Low Loss Etchless Silicon Photonic Waveguides" Optics Express 17.6 (16 Mar. 2009): 4752–4757. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-17-6-4752>.

Carts-Powell, Yvonne. "Optoelectronics & Communications: Integrating Optics and Electronics Without MEMS" SPIE. spie.org, 30 Dec. 2000. Web. <http://spie.org/newsroom/integrating-optics-and-electronics-without-mems?ArticleID=x18856>.

Caspers, Niklas J, et al. "Active polarization independent coupling to silicon photonics circuit" Silicon Photonics and Photonic Integrated Circuits IV. SPIE Proceedings Vol. 9133: SPIE, 1 May 2014. Web. <http://spie.org/Publications/Proceedings/Paper/10.1117/12.2049713>.

Cavdar, Cicek. "The Increasingly Concerning Carbon Footprint of Information and Telecommunication Technologies" Electronic Component News, 2 May 2016. Web. <https://www.ecnmag.com/blog/2016/04/increasingly-concerning-carbon-footprint-information-and-telecommunication-technologies?et_cid=5262726>.

Chaisakul, Papichaya, et al. "23 GHz Ge/SiGe Multiple Quantum Well Electro-Absorption Modulator" Optics Express 20.3 (30 Jan. 2012): 3219–3224. <https://www.osapublishing.org/oe/abstract.cfm?URI=oe-20-3-3219>.

Chang, Chia-Ming, et al. "High-Power Dual-Fed Traveling Wave Photodetector Circuits in Silicon Photonics" Optics Express 23.17 (24 Aug. 2015): 22857–22866. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-17-22857>.

Chen, Caiyun, et al. "Highly Responsive MoS2 Photodetectors Enhanced by Graphene Quantum Dots" Scientific Reports 5. (3 Mar. 2015): 11830. <http://www.nature.com/articles/srep11830>.

Chen, Chia-Ling, et al. "Integration of Single-Walled Carbon Nanotubes on to CMOS Circuitry with Parylene-C Encapsulation" 2008 8th IEEE Conference on Nanotechnology (2008): <http://www.ece.northeastern.edu/fac-ece/mehmetd/Research/CMOS%20integration/IEEE%20Nano%2008.pdf>.

Chen, Guanyu, et al. "High Speed and High Power Polarization Insensitive Germanium Photodetector with Lumped Structure" Optics Express 24.9 (2 May 2016): 10030–10039. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-9-10030>.

Chen, H T, et al. "Low-Voltage Waveguide Ge APD Based High Sensitivity 10Gb/s Si Photonic Receiver" Optical Communication (ECOC), 2015 European Conference on, (1 Oct. 2015): <http://ieeexplore.ieee.org/document/7341913/?tp=&arnumber=7341913>

Chen, Long. "Silicon Photonic Integrated Circuits for WDM Technology and Optical Switch" OSA Technical Digest OFC 2013. (17 Mar. 2013): <https://www.osapublishing.org/abstract.cfm?uri=OFC-2013-OW1C.1>.

Chen, Qimiao, et al. "A New Route Toward Light Emission from Ge: Tensile-Strained Quantum Dots" Nanoscale 7.19 (10 Apr. 2015): 8725–8730. <http://pubs.rsc.org/en/Content/ArticleLanding/2015/NR/c4nr06821a#!divAbstract>.

Chen, Roger, et al. "Nanolasers Grown on Silicon" Nature Photonics 5.3 (6 Feb. 2011): 170–175. <http://www.nature.com/nphoton/journal/v5/n3/pdf/nphoton.2010.315.pdf>.

Chen, Roger, et al. "Nanophotonic Integrated Circuits from Nanoresonators Grown on Silicon" Nature Communications 5. (7 July 2014): <http://www.nature.com/ncomms/2014/140707/ncomms5325/pdf/ncomms5325.pdf>.

Chen, S. M., et al. "1.3 μm InAs/GaAs Quantum-Dot Laser Monolithically Grown on Si Substrates Operating over 100°C" Electronics Letters 50.20 (25 Sept. 2014): 1467–1468. <http://ieeexplore.ieee.org/document/6908652/?tp=&arnumber=6908652>

Chen, Siming, et al. "Electrically Pumped Continuous-Wave III–V Quantum Dot Lasers on Silicon" Nature Photonics 10.5 (7 Mar. 2016): 307–311. <http://www.nature.com/nphoton/journal/v10/n5/pdf/nphoton.2016.21.pdf>.

Chen, Siming, et al. "Long-Wavelength InAs/GaAs Quantum-Dot Light Emitting Sources Monolithically Grown on Si Substrate" Photonics 2.2 (18 June 2015): 646–658. <http://www.mdpi.com/2304-6732/2/2/646>.

Chen, Yulu, et al. "Plasmon-Gating Photoluminescence in Graphene/GeSi Quantum Dots Hybrid Structures" Scientific Reports 5. (10 Sept. 2015): 17688. <http://www.nature.com/articles/srep17688>.

Chen, Zhitian, et al. "Spiral Bragg Grating Waveguides for TM Mode Silicon Photonics" Optics Express 23.19 (21 Sept. 2015): 25295–25307. 6 Apr. 2016. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-19-25295>.

Cheng, Yongpeng, et al. "Low-Dark-Current Waveguide InGaAs Metal–semiconductor–metal Photodetector Monolithically Integrated with InP Grating Coupler on III–V CMOS Photonics Platform" Japanese Journal of Applied Physics 55.4S (25 Feb. 2016): 04EH01. <http://iopscience.iop.org/article/10.7567/JJAP.55.04EH01/meta>.

Cherchi, Matteo, et al. "Dramatic Size Reduction of Waveguide Bends on a Micron-Scale Silicon Photonic Platform" Optics Express21.15 (29 July 2013): 17814–17823. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-21-15-17814>.

Chirgwin, Richard. "Juniper Networks Grabs Silicon Photonic Developer Aurrion" Pradeep Sindhu, Greg Fish. 3 Aug. 2016. Web. <http://www.theregister.co.uk/2016/08/03/juniper_networks_grabs_silicon_photonic_developer_aurrion/>.

Cho, Chih-Chen, and Walter M. Duncan. "Silicon-Based Microlaser by Doped Thin Films" United States Patent: Texas Instruments, Inc., 29 Nov. 1994. Web. <http://pdfpiw.uspto.gov/.piw?PageNum=0&docid=05369657>.

Chrostowski, Lukas. "Design and simulation of silicon photonic schematics and layouts" Silicon Photonics and Photonic Integrated Circuits V. Proc. SPIE 9891, Silicon Photonics and Photonic Integrated Circuits V: SPIE, 13 May 2016. Web. <https://spie.org/Publications/Proceedings/Paper/10.1117/12.2230376>.

Chrostowski, Lukas. "OpenEBL: Fabrication & Test of Passive Silicon Photonics Devices" University of British Columbia. Linkedin, 21 July 2015. Web. <https://www.linkedin.com/pulse/openebl-fabrication-test-passive-silicon-photonic-lukas-chrostowski?trk=v-feed>.

Chu, Rongming, et al. "An Experimental Demonstration of GaN CMOS Technology" IEEE Electron Device Letters 37.3 (Mar. 2016): 269–271. <http://ieeexplore.ieee.org/document/7373586/?tp=&arnumber=7373586>

Chun, Ik Su, et al. "Tuning the Photoluminescence Characteristics with Curvature for Rolled-up GaAs Quantum Well Microtubes" Appl. Phys. Lett. 96.25 (June 2010): 251106. <http://mocvd.ece.illinois.edu/publications/pubs/APPLAB9625251106_1.pdf>.

Chung, Il-Sug, and Jesper Mørk. "Silicon-Photonics Light Source Realized by III–V/Si-Grating-Mirror Laser" Appl. Phys. Lett. 97.15 (15 Oct. 2010): 151113. 12 July 2016. <http://orbit.dtu.dk/files/5506795/859D1391d01.pdf>.

Ciena Corporation. "Definition of wavelength division multiplexing" ciena.com. web: Ciena Corporation, 28 Feb. 2009. Web. <http://www.ciena.com/technology/dwdm-vs-cwdm/>.

Cisco. "Cisco Global Cloud Index" online: Cisco, 10 Nov. 2016. Web. <https://www.cisco.com/c/dam/en/us/solutions/collateral/service-provider/global-cloud-index-gci/white-paper-c11-738085.pdf>.

Condon, Stephanie. "Intel Launches Silicon Photonics" Intel. ZDNet, 17 Aug. 2016. Web. <http://www.zdnet.com/article/intel-launches-silicon-photonics/>.

Coonrod, John. "Circuit Materials and High Frequency Losses of PCBs" the pcb magazine 16 Feb. 2012: 24–29. Web. <https://www.rogerscorp.com/documents/2244/acm/articles/Circuit-Materials-and-High-Frequency-Losses-of-PCBs.pdf>.

Corkins, Ken. "Max Ethernet connections on 2 socket blade servers" bladesmadesimple.com. Blades Made Simple, 22 Oct. 2013. Web. <http://bladesmadesimple.com/2013/10/max-ethernet-connections-on-2-socket-blade-servers/>.

Creazzo, Timothy, et al. "Integrated Tunable CMOS Laser" Optics Express 21.23 (18 Nov. 2013): 28048–28053. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-21-23-28048>.

D'Ambrosia, John, and Scott Kipp. "Bandwidth growth and the next speed of Ethernet" Beaverton, OR: Ethernet Alliance, 26 Oct. 2012. Web. <https://www.nanog.org/meetings/nanog56/presentations/Tuesday/tues.general.kipp.23.pdf>.

Dai, Daoxin, and Hao Wu. "Realization of a Compact Polarization Splitter-Rotator on Silicon" Optics Letters 41.10 (11 May 2016): 2346. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-41-10-2346>.

Dai, Daoxin, and Mao Mao. "Mode Converter Based on an Inverse Taper for Multimode Silicon Nanophotonic Integrated Circuits" Optics Express 23.22 (2 Nov. 2015): 28376–28388. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-22-28376>.

Dai, Daoxin, Di Liang, and Liu Liu. "Introduction for the Integrated Photonics: Challenges and Perspectives Feature" Photonics Research 3.5 (1 Oct. 2015): IP1. <https://www.osapublishing.org/prj/abstract.cfm?uri=prj-3-5-IP1>.

Dai, Daoxin, Jared Bauters, and John E Bowers. "Passive Technologies for Future Large-Scale Photonic Integrated Circuits on Silicon: Polarization Handling, Light Non-Reciprocity and Loss Reduction" Light: Science & Applications 1.3 (1 Mar. 2012): 1. <http://www.nature.com/lsa/journal/v1/n3/abs/lsa20121a.html>.

Dallesasse, John, and Stephen B. Krasulick. Skorpios, Albuquerque, NM, "Method and System for Template Assisted Wafer Bonding" United States Patent Application, 14 June 2012. Web. <http://pdfaiw.uspto.gov/.aiw?PageNum=0&docid=20120149148>.

Dastjerdi, M H T, M Djavid, and Z Mi. "An Electrically Injected Rolled-up Semiconductor Tube Laser" Applied Physics Letters 106.2 (14 Jan. 2015): 21114. <http://scitation.aip.org/content/aip/journal/apl/106/2/10.1063/1.4906238>.

Davenport, Michael L, et al. "(invited) Heterogeneous Photonic Integration by Direct Wafer Bonding" ECS Transactions 75.9 (4 Oct. 2016): 179–183. <http://ecst.ecsdl.org/content/75/9/179.abstract>.

Davenport, Michael L., et al. "Heterogeneous Silicon/III-V Semiconductor Optical Amplifiers" (19 July 2016): <http://ieeexplore.ieee.org/document/7516667/?tp=&arnumber=7516667>

Davenport, Michael, et al. "A 400 Gb/s WDM Receiver Using a Low Loss Silicon Nitride AWG Integrated with Hybrid Silicon Photodetectors" OSA Technical Digest OFC 2013. (17 Mar. 2013): <https://www.osapublishing.org/abstract.cfm?uri=NFOEC-2013-PDP5C.5>.

Davis, Al. "Photonics and Future Datacenter Networks" 2010 IEEE Hot Chips 22 Symposium (HCS) (22 July 2010): <http://www.hotchips.org/wp-content/uploads/hc_archives/hc22/HC22.22.220-1-Davis-Photonics.pdf>.

De Coster, Jeroen, et al. "Test-Station for Flexible Semi-Automatic Wafer-Level Silicon Photonics Testing" 2016 21th IEEE European Test Symposium (ETS) (27 May 2016): <http://ieeexplore.ieee.org/document/7519306/?tp=&arnumber=7519306>

De Dobbelaere, P., et al. "Silicon Photonics Transceivers for High Speed Optical Interconnect" 2015 Opto-Electronics and Communications Conference (OECC) (2 July 2015): <http://ieeexplore.ieee.org/document/7340289/?tp=&arnumber=7340289>

De Dobbelaere, Peter, et al. "Packaging of Silicon Photonics Systems" Optical Fiber Communication Conference (13 Mar. 2014): <http://ieeexplore.ieee.org/document/6887150/?tp=&arnumber=6887150>

De Dobbelaere, Peter, et al. "Photonics Integration in Si P Platform" IEEE 64th Electronic Components And Technology Conference (ECTC) 64th.2014 (27 May 2014): <https://www.ectc.net/files/64/3%20Tuesday%20PM%20Si%20Photonics%20Session/5%20ECTC%20Si%20P%20Panel%20Session%20-%20De%20Dobbelaere%20-%20Luxtera%20ED.pdf>.

De Dobbelaere, Peter. "Light Source Approach for Silicon Photonics Transceivers" 2014 The European Conference on Optical Communication (ECOC) 2014. (25 Sept. 2014): <http://www.ecoc2014.org/search-results.php?search=luxtera>.

De Groote, Andreas, et al. "Transfer-Printing-Based Integration of Single-Mode Waveguide-Coupled III-V-on-Silicon Broadband Light Emitters" Optics Express 24.13 (27 June 2016): 13754–13762. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-13-13754>.

De Leonardis, Francesco, et al. "Germanium-on-Silicon Waveguide Engineering for Third Harmonic Generation in the Mid-Infrared" Journal of Lightwave Technology 33.24 (15 Dec. 2015): 5103–5113. <http://ieeexplore.ieee.org/document/7312890/?tp=&arnumber=7312890>

De Leonardis, Francesco, et al. "Investigation of Germanium Raman Lasers for the Mid-Infrared" Optics Express 23.13 (23 June 2015): 17237. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-13-17237>.

De Valicourt, Guilhem, et al. "Dual Hybrid Silicon-Photonic Laser with Fast Wavelength Tuning" Optics Express Vol. 23.26 (20 Mar. 2016): 33249–33254. <https://www.osapublishing.org/abstract.cfm?uri=OFC-2016-M2C.1>.

Deng, Qingzhong, et al. "Robust Polarization-Insensitive Strip-Slot Waveguide Mode Converter Based on Symmetric Multimode Interference" Optics Express 24.7 (4 Apr. 2016): 7347–7355. <https://www.osapublishing.org/oe/fulltext.cfm?uri=oe-24-7-7347&id=338537>.

Denoyer, Gilles, et al. "Hybrid Silicon Photonic Circuits and Transceiver for 56Gb/s NRZ 2.2km Transmission over Single Mode Fiber" The European Conference on Optical Communication (ECOC 2014) (25 Sept. 2014): <https://www.finisar.com/sites/default/files/resources/hybrid_silicon_photonic_circuits_and_transceiver_for_56gbs_nrz_2.2km_transmission_over_single_mode_fiber_ecoc2014.pdf>.

Dhindsa, Navneet, et al. "Adjustable Optical Response of Amorphous Silicon Nanowires Integrated with Thin Films" Nanotechnology 27.14 (24 Feb. 2016): 145703. <http://iopscience.iop.org/article/10.1088/0957-4484/27/14/145703/meta>.

Dhoore, Sören, et al. "Novel Adiabatic Tapered Couplers for Active III–V/SOI Devices Fabricated Through Transfer Printing" Optics Express 24.12 (13 June 2016): 12976–12990. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-12-12976>.

Dignan, Larry. "Intel, ARM Forge Foundry Partnership in Bet on Manufacturing Prowess" ZDNet. ZDNet, 16 Aug. 2016. Web. <http://www.zdnet.com/article/intel-arm-forge-foundry-partnership-in-bet-on-manufacturing-prowess/>.

Djordjevic, Stevan S., et al. "CMOS-Compatible, Athermal Silicon Ring Modulators Clad with Titanium Dioxide" Optics Express 21.12 (3 June 2013): 13958. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-21-12-13958>.

Doerr, Christopher. "Silicon Photonic Integration in Telecommunications" Frontiers in Physics 3.37 (5 Aug. 2015): n.pag. <http://journal.frontiersin.org/article/10.3389/fphy.2015.00037/full>.

Domingues, Cristina. "Debate Continues After AIM Photonics Leadership Council Names Leader" twcnews.com. TWC News, 13 Oct. 2015. Web. <http://www.twcnews.com/nys/rochester/news/2015/10/13/bob-duffy-to-lead-aim-photonics-leadership-council.html>.

Dong, P., et al. "Four-Channel 100-Gb/s Per Channel Discrete Multi-Tone Modulation Using Silicon Photonic Integrated Circuits" OFC 2015 (22 Mar. 2015): 1–3. <http://ieeexplore.ieee.org/document/7122147/?tp=&arnumber=7122147>

Dong, Po, et al. "128-Gb/s 100-Km Transmission with Direct Detection Using Silicon Photonic Stokes Vector Receiver and I/Q Modulator" Optics Express 24.13 (27 June 2016): 14208–14214. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-13-14208>.

Dong, Po, et al. "224-Gb/s PDM-16-QAM Modulator and Receiver Based on Silicon Photonic Integrated Circuits" OSA Technical Digest OFC 2013. (17 Mar. 2013): 5–6. <https://www.osapublishing.org/abstract.cfm?uri=OFC-2013-PDP5C.6>.

Duan, Guang-Hua, et al. "Hybrid III--V on Silicon Lasers for Photonic Integrated Circuits on Silicon" IEEE Journal of Selected Topics in Quantum Electronics 20.4 (6 Jan. 2014): 158–170. <http://ieeexplore.ieee.org/document/6697878/?tp=&arnumber=6697878>

Duan, Guang-Hua, et al. "Hybrid III-V Silicon Photonic Integrated Circuits for Optical Communication Applications" IEEE Journal of Selected Topics in Quantum Electronics (2016): 1–1. <http://ieeexplore.ieee.org/document/7593331/?tp=&arnumber=7593331>

Duan, Guang-Hua, et al. "Hybrid III-V/silicon Photonic Integrated Circuits for Optical Communication Applications" 2016 IEEE 13th International Conference on Group IV Photonics

(GFP) (26 Aug. 2016): n.pag.
<http://ieeexplore.ieee.org/document/7739136/?tp=&arnumber=7739136>

Dubé-Demers, Raphaël, Sophie LaRochelle, and Wei Shi. "Low-Power DAC-Less PAM-4 Transmitter Using a Cascaded Microring Modulator" Optics Letters 41.22 (15 Nov. 2016): 5369–5372. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-41-22-5369>.

Dube-Demers, Raphael, Sophie LaRochelle, and Wei Shi. "Ultrafast Pulse-Amplitude Modulation with a Femtojoule Silicon Photonic Modulator" Optica 3.6 (20 June 2016): 622–627. <https://www.osapublishing.org/optica/abstract.cfm?uri=optica-3-6-622>.

Duchesne, David, et al. "Hydex Glass: A CMOS Compatible Platform for Integrated Waveguide Structures for Nonlinear Optics" arXiv arXiv:1505.05953. (16 June 2015): <http://arxiv.org/ftp/arxiv/papers/1505/1505.05953.pdf>.

Dumcenco, Dumitru, et al. "Large-Area Epitaxial Monolayer MoS2" arXiv (1 May 2014): <https://arxiv.org/abs/1405.0129>.

Dumon, Pieter, et al. "Silicon Nanophotonics" Future Fab International 15 Apr. 2005: n.pag. Web. <http://pcphotonics.intec.ugent.be/download/pub_2239.pdf>. Issue 25.

Dunn, Dianne R. "Monthly Energy Review - November 2016" United States Energy Information Adminstration, 30 Nov. 2016. Web.
<https://www.eia.gov/totalenergy/data/monthly/pdf/mer.pdf>.

Duprez, Helene, et al. "Highly Tunable Heterogeneously Integrated III-V on Silicon Sampled-Grating Distributed Bragg Reflector Lasers Operating in the O-Band" Optics Express 24.18 (5 Sept. 2016): 20895–20903. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-18-20895>.

Dupuis, Nicolas, et al. "30-Gb/s Optical Link Combining Heterogeneously Integrated III–V/Si Photonics with 32-Nm CMOS Circuits" Journal of Lightwave Technology 33.3 (1 Feb. 2015): 657–662. <http://www.creol.ucf.edu/Research/Publications/9055.pdf>.

Enright, Ryan, et al. "(invited) Electrodeposited Micro Thermoelectric Module Design for Hybrid Semiconductor Laser Cooling on a Silicon Photonics Platform" ECS Transactions 69.9 (2 Oct. 2015): 37–51. <http://ecst.ecsdl.org/content/69/9/37.short>.

Ericsson . "Next-generation data center infrastructure – making hyperscale available" Stockholm, Sweden: Ericsson, 28 Feb. 2015. Web.
<https://www.ericsson.com/res/docs/whitepapers/next-generation-data-centers.pdf>.

Ericsson. "Ericsson-Backed Research Project Breaks New Ground in Silicon Photonic Integratino" erisson.com. 2015. Web. <https://www.ericsson.com/news/1948557>.

Ethernet Alliance. "2015 Ethernet Roadmap Animated Video" YouTube. YouTube, 21 Oct. 2015. Web. <https://www.youtube.com/watch?v=Gx7bVOLpC0A>.

Ethernet Alliance. "The 2016 Ethernet Roadmap" ethernetalliance.org. 24 Mar. 2015. Web. <http://www.ethernetalliance.org/roadmap/>.

Fairley, Peter. "The Microphotonics Revolution" MIT Technology Review 1 July 2000: n.pag. Web. <https://www.technologyreview.com/s/400745/the-microphotonics-revolution/>.

Fang, Alexander W., et al. "Electrically Pumped Hybrid AlGaInAs-Silicon Evanescent Laser" Optics Express 14.20 (2 Oct. 2006): 9203. <https://www.osapublishing.org/oe/issue.cfm?volume=14&issue=20>.

Fang, Qing, et al. "Cleaved Fiber-to-Nano Waveguide Mode Converter for Silicon Photonics Devices" Photonics Global Conference (PGC) 2012. (13 Dec. 2012): 1–3. 22 Apr. 2016. <http://ieeexplore.ieee.org/document/6457944/?tp=&arnumber=6457944>

Farsaei, Ahmadreza, et al. "A Novel and Scalable Design Methodology for the Simulation of Photonic Integrated Circuits" OSA Technical Digest (18 July 2016): 2–4. <https://www.osapublishing.org/abstract.cfm?uri=Networks-2016-JTu4A.2>.

Fechner, Randy G., et al. "Directional Couplers with Integrated Carbon Nanotube Incandescent Light Emitters" Optics Express 24.2 (12 Jan. 2016): 966. <https://app.refme.com/home#/project/3667786/reference/confirm>.

Feng, Shaoqi, et al. "Athermal Silicon Ring Resonators Clad with Titanium Dioxide for 1.3μm Wavelength Operation" Optics Express23.20 (5 Oct. 2015): 25653–25660. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-20-25653>.

Filkins, Patrick. "How Juniper Strategy Helped Drive Sales in Q3" Rami Rahm. TelecomLead, 26 Oct. 2016. Web. <http://www.telecomlead.com/telecom-equipment/juniper-strategy-helped-drive-sales-higher-q3-2016-72208>.

Fish, Gregory, et al. "Advances in III–V Heterogeneous Integration on Silicon" Photonics Conference (IPC), 2012 IEEE 2012. (27 Sept. 2012): 747–748. <http://ieeexplore.ieee.org/document/6358838/?tp=&arnumber=6358838>

Froeter, Paul, et al. "3D Hierarchical Architectures Based on Self-Rolled-up Silicon Nitride Membranes" Nanotechnology 24.47 (31 Oct. 2013): 475301. <http://iopscience.iop.org/article/10.1088/0957-4484/24/47/475301>.

Fu, Po-Han, et al. "Microring Resonator Composed of Vertical Slot Waveguides with Minimum Polarization Mode Dispersion over a Wide Spectral Range" Applied Optics 55.13 (1 May 2016): 3626–3631. <https://www.osapublishing.org/ao/abstract.cfm?uri=ao-55-13-3626>.

Galan, J. V., et al. "Low Profile Silicon Photonics Packaging Approach Featuring Configurable Multiple Electrical and Optical Connectivity" Group IV Photonics (GFP), 2011 8th IEEE International Conference on (14 Sept. 2016): 377–379. <http://ieeexplore.ieee.org/document/6053822/?tp=&arnumber=6053822>

Gallacher, Kevin, et al. "1.55 μm Direct Bandgap Electroluminescence from Strained N-Ge Quantum Wells Grown on Si Substrates" Applied Physics Letters (19 Nov. 2012): <http://eprints.gla.ac.uk/73084/>.

Gan, Xuetao, et al. "Chip-Integrated Ultrafast Graphene Photodetector with High Responsivity" Nature Photonics 7.11 (15 Sept. 2013): 883–887. <http://www.nature.com/nphoton/journal/v7/n11/full/nphoton.2013.253.html>.

Gao, Ge, et al. "Air-Mode Photonic Crystal Ring Resonator on Silicon-on-Insulator" Scientific Reports 6. (28 Jan. 2016): 19999. <http://www.nature.com/articles/srep19999>.

Gaufrès, Etienne, et al. "Optical Gain in Carbon Nanotubes" Appl. Phys. Lett. 96.23 (8 June 2010): 231105. <http://www.ief.u-psud.fr/~izard/publis/APL(96)231105.pdf>.

Gaufrès, Etienne, et al. "Title: Light Emission in Silicon from Carbon Nanotubes" (5 Aug. 2015): <https://arxiv.org/abs/1508.01015>.

gazettabyte. "Start-up Sicoya targets chip-to-chip interfaces" gazettabyte. 10 Feb. 2016. Web. <http://www.gazettabyte.com/home/2016/2/10/start-up-sicoya-targets-chip-to-chip-interfaces.html>.

geektime. "Israel's ColorChip Raises US$25 Million in Funding" e27 27 Nov. 2015: Web. <https://e27.co/israels-colorchip-raises-us25-million-funding-20151127/>.

Getov, Vladimir, Adoffy Hoisie, and Pradip Bose. "New Frontiers in Energy-Efficient Computing [Guest Editors' Introduction] - IEEE Xplore Document" Computer 49.10 (20 Oct. 2016): 14–18. <http://ieeexplore.ieee.org/document/7598170/?tp=&arnumber=7598170>

Getov, Vladimir, Adolfy Hosie, and Pradip Bose. "New Frontiers in Energy Efficient Computing" online: IEEE, 31 Oct. 2016. Web. <http://ieeexplore.ieee.org/document/7598170/?tp=&arnumber=7598170>

Giuntoni, Ivano, et al. "Light Coupling Between Vertical III-As Nanowires and Planar Si Photonic Waveguides for the Monolithic Integration of Active Optoelectronic Devices on a Si Platform" Opt. Express 24.16 (2 Aug. 2016): 18417. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-16-18417>.

Goi, K., et al. "DQPSK/QPSK Modulation at 40–60 Gb/s Using Low-Loss Nested Silicon Mach-Zehnder Modulator" Optical Fiber Communication Conference and Exposition and the National Fiber Optic Engineers Conference (OFC/NFOEC), 2013 (21 Mar. 2013): 1–3. <http://ieeexplore.ieee.org/document/6533216/?tp=&arnumber=6533216>

Goi, Kazuhiro, et al. "DQPSK/QPSK Modulation at 40-60 Gb/s Using Low-Loss Nested Silicon Mach-Zehnder Modulator" Optical Fiber Communication Conference/National Fiber Optic Engineers Conference 2013 (21 Mar. 2013): <http://ieeexplore.ieee.org/document/6533216/?tp=&arnumber=6533216>

Gokhale, Milind. "Silicon Photonics Needs an Indium Phosphide Laser – NeoPhotonics Blog" NeoPhotonics. 13 Apr. 2016. Web. <http://blog.neophotonics.com/silicon-photonics-needs-an-indium-phosphide-laser/>.

Gokhale, Vikrant J., and Mina Rais-Zadeh. "Uncooled Infrared Detectors Using Gallium Nitride on Silicon Micromechanical Resonators" Journal of Microelectromechanical Systems 29.4 (11 Dec. 2013): 803–810. <http://ieeexplore.ieee.org/document/6680650/?tp=&arnumber=6680650>

Gong, Xiwen, et al. "Highly Efficient Quantum Dot Near-Infrared Light-Emitting Diodes" Nature Photonics 10.4 (22 Feb. 2016): 253–257. <http://www.nature.com/nphoton/journal/v10/n4/full/nphoton.2016.11.html>.

Goovaerts, Diana. "SPACE SAVER, GAME CHANGER: How MicroQSFP Will Revolutionize Data Centers" online: Advantage Business Media, 27 June 2016. Web. <https://abm-website-assets.s3.amazonaws.com/ecnmag.com/s3fs-public/DEG%20i-Report%20Micro%20QSFPs_FINAL.pdf>.

Green, Erin. "Open Compute Project U.S. Summit 2015 – Facebook News Recap" code.facebook.com: Facebook, 10 Mar. 2015. Web. <https://code.facebook.com/posts/1538145769783718/open-compute-project-u-s-summit-2015-facebook-news-recap/>.

Greene, Kate. "Silicon Photonics Comes to Makret" MIT Technology Review 2007: Web. <https://www.technologyreview.com/s/408520/silicon-photonics-comes-to-market/>.

Greene, Tim. "Juniper CEO: On the Cusp of Transforming Economics of Optical Networking" Rami Rahim. Network World, 6 Oct. 2016. Web. <http://www.networkworld.com/article/3128360/lan-wan/juniper-ceo-on-the-cusp-of-transforming-economics-of-optical-networking.html>.

Groblacher, Simon, et al. "Highly Efficient Coupling from an Optical Fiber to a Nanoscale Silicon Optomechanical Cavity" arXiv1309.,1181. (4 Sept. 2013): <http://arxiv.org/abs/1309.1181#>.

Grydlik, Martyna, et al. "Lasing from Glassy Ge Quantum Dots in Crystalline Si - ACS Photonics (ACS Publications)" 3. (4 Feb. 2016): <https://arxiv.org/abs/1505.03380>.

Gu, Qingyuan, et al. "Photonics Based on Carbon Nanotubes" Nanoscale Research Letters 8.1 (26 June 2013): 300. <http://nanoscalereslett.springeropen.com/articles/10.1186/1556-276X-8-300>.

Guerra, Maria. "5 methods for improving data center efficiency" electronic design. 21 June 2016. Web. <http://electronicdesign.com/power/5-methods-improving-data-center-efficiency>.

Guiang, Cynthia. "CrossFiber to Showcase Next-Generation Photonic Switches at OFC 2015" CrossFiber. ofcconference.org, 23 Mar. 2015. Web. <http://www.ofcconference.org/en-us/home/news-and-press/exhibitor-press-releases/exhibitor-press-releases/crossfiber-to-showcase-next-generation-photonic-sw/>.

Gunn, Cary. "CMOS Photonics for High-Speed Interconnects" IEEE Micro 24 June 2006: 58–66. Web. <http://ieeexplore.ieee.org/document/1624327/?tp=&arnumber=1624327>

Guo, Xitao, et al. "High-Performance Graphene Photodetector Using Interfacial Gating" Optica 3.10 (21 Sept. 2016): 1066–1070. <https://www.osapublishing.org/optica/abstract.cfm?uri=optica-3-10-1066>.

Haffner, C., et al. "All-Plasmonic Mach–Zehnder Modulator Enabling Optical High-Speed Communication at the Microscale" Nature Photonics 9.8 (27 July 2015): 525–528. <http://www.nature.com/nphoton/journal/v9/n8/full/nphoton.2015.127.html>.

Hardy, Stephen. "Acacia Communications Offers 400-Gbps Coherent Transceiver Module" Lightwave (lightwaveonline.com). 23 Mar. 2015. Web. <http://www.lightwaveonline.com/articles/2015/03/acacia-communications-offers-400-gbps-coherent-transceiver-module.html>.

Hardy, Stephen. "AEPONYX Enhances MEMS Silicon Photonics Efforts by Joining Silicon Catalyst Incubator" Philippe Bain. lightwaveonline, 15 Sept. 2016. Web. <http://www.lightwaveonline.com/articles/2016/09/aeponyx-enhances-mems-silicon-photonics-efforts-by-joining-silicon-catalyst-incubator.html>.

Hardy, Stephen. "Ciena Buys TeraXion's Indium Phosphide, Silicon Photonics Assets" Ciena Corporation. 19 Jan. 2016. Web. <http://www.lightwaveonline.com/articles/2016/01/ciena-buys-teraxion-s-indium-phosphide-silicon-photonics-assets.html>.

Hardy, Stephen. "Silicon Photonics Doesn't Scare Finisar" Seeking Alpha. 31 Mar. 2013. Web. <http://www.lightwaveonline.com/blogs/lightwave-blog/2013/03/Silicon-photonics-doesnt-scare-Finisar.html>.

Hardy, Stephen. "The Promise & Perils of Silicon Photonics" lightwaveonline.com, 1 Mar. 2013. Web. <http://www.lightwaveonline.com/articles/print/volume-30/issue-2/cover-story/the-promise-and-perils-of-silicon-photonics.html>.

Hatori, Nobuaki, et al. "Quantum Dot Laser for a Light Source of an Athermal Silicon Optical Interposer" Photonics 2.2 (3 Apr. 2015): 355–364. <http://www.mdpi.com/2304-6732/2/2/355>.

Hausken, Tom. "Breaking the Cost Barrier" Optics & Photonics News 1 July 2015: 21. Web. <http://www.osa-opn.org/home/articles/volume_26/july_august_2015/departments/breaking_the_cost_barrier/>.

Hayakawa, Akinori, et al. "Silicon Photonics Optical Transceiver for High-Speed, High-Density and Low-Power LSI Interconnect" Tech. J 52.1 (31 Jan. 2016): 19–26. <https://www.fujitsu.com/global/documents/about/resources/publications/fstj/archives/vol52-1/paper03.pdf>.

Hecht, Jeff. "The Bandwidth Bottleneck That Is Throttling the Internet" News Feature 536.7615 (10 Aug. 2016): 139. <http://www.nature.com/news/the-bandwidth-bottleneck-that-is-throttling-the-internet-1.20392>.

Heck, Martijn J R, et al. "Hybrid Silicon Photonics for Optical Interconnects" IEEE Journal of Seleted Topics in Quantum Electronics17.2 (5 Aug. 2010): <https://www.ece.ucsb.edu/spc/sites/optoelectronics/sites/default/files/publications/%5B10%5D.pdf>.

Heck, Martijn J. R., et al. "Hybrid Silicon Photonics for Optical Interconnects" IEEE Journal of Selected Topics in Quantum Electronics 17.2 (5 Aug. 2010): 333–346. <http://ieeexplore.ieee.org/document/5540250/?tp=&arnumber=5540250>

Heck, Martijn J. R., Michael L. Davenport, and John E. Bowers. "Progress in Hybrid-Silicon Photonic Integrated Circuit Technology" UC Santa Barbara. 4 Feb. 2013. Web. <http://spie.org/newsroom/4730-progress-in-hybrid-silicon-photonic-integrated-circuit-technology>.

Heck, Martijn. "Photonic Technology Is Ready for the Next Bill Gates or Steve Jobs" Linkedin, 19 Oct. 2016. Web. <https://www.linkedin.com/pulse/photonic-technology-ready-new-bill-gates-steve-jobs-martijn-heck?trk=prof-post>.

Hect, Jeff. "Fiber Optic History" Rev. of Fiber Optics Technician's Handbook, by Jim Hayes. <jeffhect.com> 17 Nov. 2006: Web.

Heins, Mitch. "Fabless Photonic Design Flow Takes Shape as Cadence Teams up with Lumerical and PhoeniX" SemiWiki.com, 21 Oct. 2016. Web.

<https://www.semiwiki.com/forum/content/6311-fabless-photonic-design-flow-takes-shape-cadence-teams-up-lumerical-phoenix.html>.

Heins, Mitch. "Fabless Photonics gets a boost with Aurrion acquistion by Juniper networks" SemiWiki.com. SemiWiki.com, 7 Aug. 2016. Web. <https://www.semiwiki.com/forum/content/6059-fabless-photonics-gets-boost-aurrion-acquistion-juniper-networks.html>.

Heins, Mitch. "Si Photonics in a 300mm Fab - This Is Getting Serious!" 13 May 2016. Web. <https://www.semiwiki.com/forum/content/5784-si-photonics-300mm-fab-getting-serious.html#comments>.

Heins, Mitch. "The Fabless Empire Strikes Back, Global Foundries and Cadence Make Moves into Integrated Photonics!" SemiWiki.com, 20 Oct. 2016. Web. <https://www.semiwiki.com/forum/content/6303-fabless-empire-strikes-back-global-foundries-cadence-make-moves-into-integrated-photonics.html>.

Hemsoth, Nicole. "IEEE Reboots, Scans for Future Architectures" IEEE Rebooting Computing group. The Next Platform, 13 Oct. 2016. Web. <https://www.nextplatform.com/2016/10/13/ieee-reboots-scans-future-architectures/>.

Hemsoth, Nicole. "Light at the End of the Silicon Photonics Tunnel" David Calhoun. The Next Platform, 21 Jan. 2016. Web. <https://www.nextplatform.com/2016/01/21/light-at-the-end-of-the-silicon-photonics-tunnel/>.

Heni, W., et al. "108 Gbit/s Plasmonic Mach–Zehnder Modulator with > 70-GHz Electrical Bandwidth" Journal of Lightwave Technology 34.2 (15 Jan. 2016): <http://ieeexplore.ieee.org/document/7293117/?tp=&arnumber=7293117>

Heni, W., et al. "High Speed Plasmonic Modulator Array Enabling Dense Optical Interconnect Solutions" Optics Express 23.23 (5 Nov. 2015): 29746. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-23-29746>.

Höfling, Sven, et al. "An Electrically Pumped Polariton Laser" IEEE Photonics Conference (IPC) (4 Oct. 2008): 613–614. <http://ieeexplore.ieee.org/document/7323743/?tp=&arnumber=7323743>

Hong, Kuo-Bin, and Tien-Chang Lu. "Systematic Characterization of Gallium Nitride Photonic Crystal Surface-Emitting Lasers" SPIE Newsroom (30 Sept. 2015): <http://spie.org/newsroom/6084-systematic-characterization-of-gallium-nitride-photonic-crystal-surface-emitting-lasers>.

Hopkins, F. Kenneth. "Germanium Photonics" SPIE Newsroom (21 Aug. 2013): <http://spie.org/newsroom/4982-germanium-photonics>.

Hosseini, Ehsan Shah, et al. "CMOS-Compatible 75 MW Erbium-Doped Distributed Feedback Laser" Optics Letters 39.11 (1 June 2014): 3106–3109. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-39-11-3106>.

Hsu, Chao-Wei, Yung-Feng Chen, and Yan-Kuin Su. "Quality Improvement of GaN on Si Substrate for Ultraviolet Photodetector Application" IEEE Journal of Quantum Electronics 50.1 (Jan. 2014): 35–41. <http://ieeexplore.ieee.org/document/6674047/?tp=&arnumber=6674047>

Hu, Xiao, et al. "Graphene-Silicon Microring Resonator Enhanced All-Optical up and down Wavelength Conversion of QPSK Signal" Optics Express 24.7 (24 Mar. 2016): 7168. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-7-7168>.

Hu, Yingtao, et al. "High-Speed Silicon Modulator Based on Cascaded Microring Resonators" Optics Express 20.14 (2 July 2012): 15079–15085. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-20-14-15079>.

Huang, Gregory T. "Newly Public Acacia Targets Data Centers, Wants to Be the Next Intel" Acacia Communications. Xconomy, 10 Aug. 2016. Web. <http://www.xconomy.com/boston/2016/08/10/newly-public-acacia-targets-data-centers-wants-to-be-the-next-intel/?single_page=true>.

Huang, Qingzhong, et al. "Electromagnetically Induced Transparency-Like Effect in a Two-Bus Waveguides Coupled Microdisk Resonator" Optics Express 22.3 (4 Feb. 2014): 3219. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-22-3-3219>.

Huang, Zhihong, et al. "25 Gbps Low-Voltage Waveguide Si–Ge Avalanche Photodiode" Optica 3.8 (20 Aug. 2016): 793–798. <https://www.osapublishing.org/optica/abstract.cfm?uri=optica-3-8-793>.

Huang, Zhong-Mei, et al. "Emission of Direct-Gap Band in Germanium with Ge-GeSn Layers on One-Dimensional Structure" Scientific Reports 6. (17 Feb. 2016): 24802. <http://www.nature.com/articles/srep24802>.

Hudait, Mantu K., et al. "Semiconductor Buffer Architecture for III-V Devices on Silicon Substrates" United States Patent Application: Intel Corp., 24 Feb. 2911. Web. <http://pdfaiw.uspto.gov/.aiw?PageNum=0&docid=20110045659>.

Hunyh, Tam N., et al. "Flexible Silicon Photonic Transmitter with Segmented Modulator and 32 Nm CMOS Driver IC" CLEO 2016 (5 June 2016): 1–4. <https://www.osapublishing.org/abstract.cfm?uri=CLEO_SI-2016-STh4E.1>.

Huo, Yijie. "Strained Ge and GeSn band engineering for Si photonic integrated circuits" PhD Dissertation. 31 Dec. 2010. Web. <http://snow.stanford.edu/thesis/Huo.pdf>.

Hurst, Kara. "Our Largest Wind Farm Yet: Introducing Amazon Wind Farm Texas" Amazon: Amazon, 15 Sept. 2016. Web. <https://www.amazon.com/p/feature/ps9c2vfu7fcm4t6>.

Huynh, Tam N., et al. "Four-Channel WDM Transmitter with Heterogeneously Integrated III-V/Si Photonics and Low Power 32 Nm CMOS Drivers" J. Lightwave Technol. 34.13 (9 June 2016): 3131–3137. <https://www.osapublishing.org/jlt/abstract.cfm?uri=jlt-34-13-3131>.

IC Insights. "BulLetin: Number of IC Manufacturers Using 300 mm Wafers Less than Half Using 200 mm Wafers" Web: IC Insights, 16 Dec. 2016. Web. <http://www.icinsights.com/news/bulLetins/Number-Of-IC-Manufacturers-Using-300mm-Wafers-Less-Than-Half-Using-200mm-Wafers/>.

IC Insights. "Research BulLetin, June 5, 2015: Three Trends Driving Optoelectronics Market Growth Through 2019" Scottsdale, AZ: IC Insights, 5 June 2015. Web. <http://www.icinsights.com/data/articles/documents/795.pdf>.

Im, Song-Jin, et al. "20-Gb/s Modulation of Silicon-Integrated Short-Wavelength Hybrid-Cavity VCSELs" IEEE Photonics Technology Letters 28.8 (6 Jan. 2016): <http://ieeexplore.ieee.org/document/7373571/?tp=&arnumber=7373571>

Im, Song-Jin, et al. "Plasmonic Phase Modulator Based on Novel Loss-Overcompensated Coupling Between Nanoresonator and Waveguide" Scientific Reports 6. (6 Jan. 2016): 18660. <http://www.nature.com/articles/srep18660>.

Inc, RANOVUS. "Ranovus demonstrates industry's First 4.8Tb/s DWDM solution for DCI" News. RANOVUS, 19 Sept. 2016. Web. <http://ranovus.com/ranovus-demonstrates-industrys-first-4-8tbs-dwdm-solution-over-80km-dci-link/>.

Indian. "OIDA Workshop on Integrated Photonics and High Volume Packaging" OSA. 19 Mar. 2016. Web. <http://www.osa.org/en-us/meetings/global_calendar/events/integrated_photonics_high_volume_packaging/workshop_program/>.

Inoue, 8, et al. "Low-Bias Current 10 Gbit/s Direct Modulation of GaInAsP/InP Membrane DFB Laser on Silicon" Opt. Express 24.16 (8 Aug. 2016): 18571. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-16-18571&origin=search>.

Intel. "Intel Milestone Confirms Light Beams Can Replace Electronic Signals for Future Computers | Intel Newsroom" Intel. Intel Newsroom, 27 July 2010. Web. <https://newsroom.intel.com/news-releases/intel-milestone-confirms-light-beams-can-replace-electronic-signals-for-future-computers/>.

Intel. "Intel Scientists Develop World's First Continuous Laser From Standard Silicon" Intel. 17 Feb. 2005. Web. <http://www.intel.com/pressroom/archive/releases/2005/20050217tech.htm>.

Intel. "Intel Unveils New Technologies for Efficient Cloud Datacenters | Intel Newsroom" Cloud Computing. Intel Newsroom, 6 Oct. 2016. Web. <https://newsroom.intel.com/news-releases/intel-unveils-new-technologies-for-efficient-cloud-datacenters/>.

Isshiki, Hideo, et al. "Rare Earth Silicates as Gain Media for Silicon Photonics [Invited]" Photonics Research 2.3 (30 May 2014): A45. <https://www.osapublishing.org/prj/abstract.cfm?uri=prj-2-3-A45&origin=search>.

Jalali, Bahram, and Sasan Fathpour. "Silicon Photonics" Journal of Lightwave Technology 24.12 (Dec. 2006): 4600–4615. <http://ieeexplore.ieee.org/document/4063407/?tp=&arnumber=4063407>

Janowski, Davis D. "Broadband: Silicon Photonics" PC Magazine 1 July 2003: n.pag. Web. <http://www.pcmag.com/article2/0,2817,1130818,00.asp>.

Jennings, Richl. "NSA's Huge Utah Datacenter: How Much of Your Data Will It Store? Experts Disagree." James Bamford. Forbes, 26 July 2013. Web. <http://www.forbes.com/sites/netapp/2013/07/26/nsa-utah-datacenter/#3a5342c63cd2>.

Jin, Wei, and Kin Seng Chiang. "Mode Converters Based on Cascaded Long-Period Waveguide Gratings" Optics Letters 41.13 (1 July 2016): 3130–3133. 27 July 2016. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-41-13-3130>.

Johnson, R. Colin. "Intel Reveals Long-Term Goals for Silicon Photonics, Sensors" Intel CTO Patrick Gelsinger. EETimes, 28 Feb. 2002. Web. <http://www.eetimes.com/document.asp?doc_id=1226749>.

Johnson, R. Colin. "Nanolaser Enables on-Chip Photonics" Arka Majumdar. EETimes, 26 Mar. 2015. Web. <http://www.eetimes.com/document.asp?doc_id=1326138>.

Joo, J, et al. "Silicon Photonic Receiver and Transmitter Operating up to 36 Gb/s for λ~1550 Nm" Optics express. 23.9 (15 May 2015): 12232–43. <https://www.ncbi.nlm.nih.gov/pubmed/25969309>.

Judge, Peter. "Think Small, and Dream Big" Microsoft, KPN. DatacenterDynamics, 17 Jan. 2017. Web. <http://www.datacenterdynamics.com/content-tracks/power-cooling/think-small-and-dream-big/97560.fullarticle>.

Jurgensen, Holger, Alois Krost, and Armin Dadgar. "Method for the Production of III-V Laser Components" United States Patent Application: Aixtron SE, 3 Feb. 2005. Web. <http://pdfaiw.uspto.gov/.aiw?PageNum=0&docid=20050025909>.

Justice, John, et al. "Wafer-Scale Integration of Group III-V Lasers on Silicon Using Transfer Printing of Epitaxial Layers" Nature Photonics 6.9 (19 Aug. 2012): 610–614. <http://www.nature.com/nphoton/journal/v6/n9/pdf/nphoton.2012.204.pdf>.

Juvert, Joan, et al. "A Low-Cost Technique for Adding Microlasers to a Silicon Photonic Platform" Proceedings of the SPIE 9752 (14 Mar. 2016): 7–97520. <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=2504320>.

Kahn, Joseph M., and David A. B. Miller. "Communications Expands Its Space" Nature Photonics 11.1 (3 Jan. 2017): 5–8. <http://www.nature.com/nphoton/journal/v11/n1/full/nphoton.2016.256.html?WT.ec_id=NPHOTON-201701>.

Kahn, Joseph. "Modulation and Detection Techniques for Optical Communication Systems" Optical Amplifiers and Their Applications/Coherent Optical Technologies and Applications (2006): n.pag. <https://www.osapublishing.org/abstract.cfm?uri=cota-2006-CThC1>.

Kamada, Shun, et al. "Design Optimization and Fabrication of Mach- Zehnder Interferometer Based on MIM Plasmonic Waveguides" Optics Express 24.15 (25 July 2016): 16224–16231. 5 Aug. 2016. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-15-16224>.

Kaminow, Ivan P. "Optical Integrated Circuits: A Personal Perspective" Journal of Lightwave Technology 26.9 (1 May 2008): 994–1004. <http://ieeexplore.ieee.org/document/4542887/>.

Kang, Yimin, et al. "Monolithic Germanium/silicon Avalanche Photodiodes with 340 GHz Gain–bandwidth Product" Nature Photonics 3.1 (7 Dec. 2008): 59–63. <http://www.nature.com/nphoton/journal/v3/n1/full/nphoton.2008.247.html>.

Karr, Kelly. "Oclaro to Demonstrate 400GBASE-LR8 CFP8 Transceiver over 10km Singlemode Fiber at ECOC 2016 (NASDAQ: OCLR)" Oclaro. Oclaro, 19 Sept. 2016. Web. <http://investor.oclaro.com/releasedetail.cfm?releaseid=989795>.

Keyvaninia, S., et al. "III-V-on-Silicon Multi-Frequency Lasers" Optics Express 21.11 (30 May 2013): 13675. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-21-11-13675>.

Keyvaninia, S., et al. "Narrow-Linewidth Short-Pulse III-V-on-Silicon Mode-Locked Lasers Based on a Linear and Ring Cavity Geometry" Opt. Express 23.3 (2015): 3221. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-3-3221>.

Keyvaninia, Shahram, et al. "Demonstration of a Heterogeneously Integrated III-V/SOI Single Wavelength Tunable Laser" Optics Express 21.3 (7 Feb. 2013): 3784. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-21-3-3784>.

Khilo, Anatol, et al. "Efficient Planar Fiber-to-Chip Coupler Based on Two-Stage Adiabatic Evolution" Optics Express 18.15 (19 July 2010): 15790–15806. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-18-15-15790>.

Khurgin, Jacob B, et al. "On the Origin of the Second-Order Nonlinearity in Strained Si-SiN Structures" arXiv (3 Sept. 2015): <https://arxiv.org/abs/1509.01166>.

Kim, Gyungock, et al. "Single-Chip Photonic Transceiver Based on Bulk-Silicon, as a Chip-Level Photonic I/O Platform for Optical Interconnects" Scientific Reports 5. (10 June 2015): 11329. <http://www.nature.com/articles/srep11329>.

Kim, Hyunseok, et al. "Monolithically Integrated InGaAs Nanowires on 3D Structured Silicon-on-Insulator as a New Platform for Full Optical Links" Nano Letters 16.3 (9 Mar. 2016): 1833–1839. <http://pubs.acs.org/doi/abs/10.1021/acs.nanolett.5b04883>.

Kim, Seonghoon, et al. "Coherent Polariton Laser" Phys. Rev. X 6.1 (11 Mar. 2016): <http://journals.aps.org/prx/pdf/10.1103/PhysRevX.6.011026>.

Kimerling, L C, et al. "Electronic-Photonic Integrated Circuits on the CMOS Platform" Proceedings of the SPIE 6125. (21 Jan. 2006): <http://spie.org/Publications/Proceedings/Paper/10.1117/12.654455>.

Kita, Tomohiro, et al. "Heterogeneous Quantum Dot/silicon Photonics-Based Wavelength-Tunable Laser Diode with a 44 Nm Wavelength-Tuning Range" Japanese Journal of Applied Physics 55.4S (23 Mar. 2016): 04EH11. <http://iopscience.iop.org/article/10.7567/JJAP.55.04EH11/meta>.

Kita, Tomohiro, Rui Tang, and Hirohito Yamada. "Compact Silicon Photonic Wavelength-Tunable Laser Diode with Ultra-Wide Wavelength Tuning Range" Applied Physics Letters 106.11 (16 Mar. 2015): 111104. <http://scitation.aip.org/content/aip/journal/apl/106/11/10.1063/1.4915306>.

Klamkin, Jonathan. "3D Hybrid Integration for Silicon Photonics" Frontiers in Optics 2016. (17 Oct. 2016): 1–5. <https://www.osapublishing.org/abstract.cfm?URI=fio-2016-FF5F.1>.

Klein, E. J., et al. "Reconfigurable Optical Add-Drop Multiplexer Using Microring Resonators" IEEE Photonics Technology Letters 17.11 (7 Apr. 2005): 2358–2360. <http://ieeexplore.ieee.org/document/1522319/?tp=&arnumber=1522319>

Kobayashi, N., et al. "Silicon Photonic Hybrid Ring-Filter External Cavity Wavelength Tunable Lasers" Journal of Lightwave Technology 33.6 (15 Mar. 2015): 1241–1246. <http://ieeexplore.ieee.org/document/6994779/?tp=&arnumber=6994779>

Kobayashi, Wataru, and Masahiro Nada. "Compact Optical Devices with Low Power Consumption" NTT Technical Review 2017.1 (18 Jan. 2017): n.pag. <https://www.ntt-review.jp/archive/ntttechnical.php?contents=ntr201701fa3.pdf&mode=show_pdf>.

Koch, Brian R., et al. "Mode-Locked Silicon Evanescent Lasers" Optics Express 15.18 (3 Sept. 2007): 11225–11233. <https://www.osapublishing.org/oe/fulltext.cfm?uri=oe-15-18-11225&id=140973>.

Komljenovic, Tin, et al. "Heterogeneous Silicon Photonic Integrated Circuits" Journal of Lightwave Technology 34.1 (6 Aug. 2015): 20–35. <https://www.osapublishing.org/jlt/abstract.cfm?uri=jlt-34-1-20>.

Komljenovic, Tin, et al. "Widely Tunable Narrow-Linewidth Monolithically Integrated External-Cavity Semiconductor Lasers" IEEE Journal of Selected Topics in Quantum Electronics 21.6 (Dec. 2015): 214–222. 28 July 2016. <http://ieeexplore.ieee.org/document/7084629/?tp=&arnumber=7084629>

Kopp, C, et al. "Silicon Photonic Circuits: On-CMOS Integration, Fiber Optical Coupling, and Packaging" IEEE Journal of Selected Topics in Quantum Electronics 17.3 (7 Oct. 2010): 498–509. <http://ieeexplore.ieee.org/document/5595485/?tp=&arnumber=5595485>

Kopp, Christophe, et al. "Enhanced Fiber Grating Coupler Integrated by Wafer-to-Wafer Bonding" Journal of Lightwave Technology29.12 (25 Apr. 2011): 1847–1851. <http://ieeexplore.ieee.org/document/5755125/?tp=&arnumber=5755125>

Kopp, Victor I., et al. "Two-Dimensional, 37-Channel, High-Bandwidth, Ultra-Dense Silicon Photonics Optical Interface" Journal of Lightwave Technology 33.3 (1 Feb. 2001): 653–656. <http://ieeexplore.ieee.org/document/6934976/?tp=&arnumber=6934976>

Korczynski, Ed. "Scouting report for materials at end of the road: 2013 ITRS" semiminnd.com. 12 May 2014. Web. <http://semimd.com/blog/2014/05/12/scouting-report-for-materials-at-end-of-the-road-2013-itrs/>.

Kovacevic, G, and S Yamashita. "Waveguide Design Parameters Impact on Absorption in Graphene Coated Silicon Photonic Integrated Circuits" Optics express. 24.4 (26 Feb. 2016): 3584–91. <https://www.ncbi.nlm.nih.gov/pubmed/26907015>.

Kozlov, Vladimir G. "Analysis: Silicon Photonics Establishes a Beachhead in Two of the Fastest Growing Market Segments" LightCounting. PIC Magazine, 23 Dec. 2016, 3 ed. Web. <http://www.publishing.ninja/V2/page/3049/175/168/1>.

Krasulick, Stephen B. "Method and System for Heterogeneous Substrate Bonding of Waveguide Receivers" Albuquerque, NM: Skorpios, Inc., United States Patent, 17 Dec. 2013. Web. <http://pdfpiw.uspto.gov/.piw?PageNum=0&docid=08611388>.

Krasulick, Stephen B., and John Dellesasse. "Method and System for Heterogeneous Substrate Bonding of Waveguide Receivers" Albuquerque, NM: Skorpios, Inc., United States Patent Application, 8 Mar. 2013. Web. <http://pdfaiw.uspto.gov/.aiw?PageNum=0&docid=20120057816>.

Kress, Kurt. "All Will Go down with Moore's Law" Clayton Hallmark. 18 May 2006. Web. <https://www.indybay.org/newsitems/2006/05/18/18240941.php>.

Krishnamoorthy, Ashok, et al. "From Chip to Cloud: Optical Interconnects in Engineered Systems." Journal of Lightwave Technology PP.19 (21 Dec. 2016): 1–1. <http://ieeexplore.ieee.org/abstract/document/7792625/>.

Ku, Kai-Ning, and Ming-Chang M Lee. "Cascade of Two Opposite Tapers for Butt-Coupling Between Fibers and Silicon Photonic Wires with Large Misalignment Tolerance and Low Polarization Dependency" OSA Technical Digest (online) (Optical Society of America, 2013) (17 Mar. 2013): 2–3. <https://www.osapublishing.org/abstract.cfm?uri=OFC-2013-OTu2C.3>.

Kunert, B, et al. "III/V Nano Ridge Structures for Optical Applications on Patterned 300 Mm Silicon Substrate" Applied Physics Letters 109.9 (29 Aug. 2016): 91101. <http://scitation.aip.org/content/aip/journal/apl/109/9/10.1063/1.4961936>.

Kurczveil, Géza, et al. "Robust Hybrid Quantum Dot Laser for Integrated Silicon Photonics" Optics Express 24.14 (11 July 2016): 16167–16174. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-14-16167>.

Lacoursiere, Catherine. "Photonic Integrated Circuits: New Directions" BCC Research, 1 Jan. 2005. Web. <http://www.bccresearch.com/market-research/semiconductor-manufacturing/SMC045B.html>.

Lai, Sinan, et al. "Compact Silicon Photonic Interleaver Based on a Self-Coupled Optical Waveguide" Applied Optics 55.27 (20 Sept. 2016): 7550–7555. <https://www.osapublishing.org/ao/abstract.cfm?uri=ao-55-27-7550>.

Lauermann, M., et al. "High-Speed and Low-Power Silicon-Organic Hybrid Modulators for Advanced Modulation Formats" Integrated Optics: Physics and Simulations II (1 May 2015): <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=2290727>.

Lazear, Alex. "Israel's ColorChip Raises $25 Million in Growth Funding" geektime. Geektime, 22 Nov. 2015. Web. <http://www.geektime.com/2015/11/22/israels-colorchip-raises-25-million-in-growth-funding/>.

Le Maistre, Ray. "Infinera Ups the DCI Ante" Pravin Mahajan. Light Reading, 22 Sept. 2016. Web. <http://www.lightreading.com/data-center/data-center-interconnect-/infinera-ups-the-dci-ante/d/d-id/726309>.

Lee, Andrew D., et al. "InAs/GaAs Quantum-Dot Lasers Monolithically Grown on Si, Ge, and Ge-on-Si Substrates" IEEE Journal of Selected Topics in Quantum Electronics 19.4 (31 July 2013): 1901107. 31 July 2016. <http://ieeexplore.ieee.org/document/6466353/?tp=&arnumber=6466353>

Lee, Chee-Wei, and Qian Wang. "Metal–Semiconductor Square Nanocavity and Light Extraction" IEEE Photonics Technology Letters 28.2 (15 Jan. 2016): 127–130. <http://ieeexplore.ieee.org/document/7293154/?tp=&arnumber=7293154>

Lee, Chee-Wei, et al. "Fabrication and Demonstration of III–V/Si Heterocore Microcavity Lasers via Ultrathin Interlayer Bonding and Dual Hard Mask Techniques" ACS Photonics 3.11 (16 Nov. 2016): 2191–2196. <http://pubs.acs.org/doi/abs/10.1021/acsphotonics.6b00794?journalCode=apchd5>.

Lee, Chee-Wei, et al. "Generic Heterogeneously Integrated III-V Lasers-on-Chip with Metal-Coated Etched-Mirror" Proc. SPIE 9751: Smart Photonic and Optoelectronic Integrated Circuits XVIII (3 May 2016): 8–97510. <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=2521173>.

Lee, Chee-Wei, et al. "Hetero-Core III-V/Si Microlaser" Optics Letters 41.13 (1 July 2016): 3149–3152. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-41-13-3149>.

Lee, Chee-Wei, et al. "Study of Ultrathin SiO 2 Interlayer Wafer Bonding for Heterogeneous III–V/Si Photonic Integration" Materials Research Express 2.9 (10 Sept. 2015): 096201. <http://iopscience.iop.org/article/10.1088/2053-1591/2/9/096201>.

Lee, Jin-Hyoung, et al. "Demonstration of 12.2% Wall Plug Efficiency in Uncooled Single Mode External-Cavity Tunable Si/III-V Hybrid Laser" Opt. Express 23.9 (29 Apr. 2015): 12079. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-9-12079>.

Lee, Wook-Jae, et al. "Nanopillar Array Band-Edge Laser Cavities on Silicon-on-Insulator for Monolithic Integrated Light Sources" Applied Physics Letters 108.8 (24 Feb. 2016): 81108. <http://scitation.aip.org/content/aip/journal/apl/108/8/10.1063/1.4942777>.

Leroy, Sandrine. "Has Silicon Photonics a Huge Market Potential? Silicon Photonics: Big Investmetns, Small Business"" Yole Developpement, 21 Sept. 2012. Web. <http://www.semiconductorpackagingnews.com/uploads/1/PR_Silicon_Photonics__Big_Investments_Small_Business.pdf>.

Lewotsky, Kristin. "Silicon Poises for Disruption" SPIE. Jan. 2006. Web. <https://spie.org/membership/spie-professional-magazine/spie-professional-archives-and-special-content/january-2006/silicon-poises-for-disruption>.

Li, Ang, Qiansheng Huang, and Wim Bogaerts. "Design of a Single All-Silicon Ring Resonator with a 150 Nm Free Spectral Range and a 100 Nm Tuning Range Around 1550 Nm" Photonics Research 4.2 (1 Apr. 2016): 84–92. <https://www.osapublishing.org/prj/abstract.cfm?uri=prj-4-2-84>.

Li, Chao, et al. "Silicon Photonics Packaging with Lateral Fiber Coupling to Apodized Grating Coupler Embedded Circuit" Optics Express 22.20 (6 Oct. 2014): 24235–24240. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-22-20-24235>.

Li, Cheng, et al. "Silicon Photonic Transceiver Circuits with Microring Resonator Bias-Based Wavelength Stabilization in 65 Nm CMOS" IEEE J. Solid-State Circuits 49.6 (June 2014): 1419–1436. <http://ece.tamu.edu/~spalermo/docs/2014_ring_resonator_xcvr_circuits_li_jssc.pdf>.

Li, Feng, and Zetian Mi. "Optically Pumped Rolled-up InGaAs/GaAs Quantum Dot Microtube Lasers" Optics Express 17.22 (26 Oct. 2009): 19933–19939. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-17-22-19933>.

Li, Glenn. "Monolithic Silicon Platform for 100G/400G Ethernet Applications" Ethernet Technology Sumit, 30 Apr. 2014. Web. <http://www.ethernetsummit.com/English/Collaterals/Proceedings/2014/20140430_1C_Li.pdf>.

Li, Guoliang, et al. "100Gb/s CWDM Transmitter and Receiver Chips on a Monolithic Si-Photonics Platform" 2016 IEEE 13th International Conference on Group IV Photonics (GFP) (26 Aug. 2016): n.pag. <http://ieeexplore.ieee.org/document/7739135/?tp=&arnumber=7739135>

Li, Guoliang, et al. "A CMOS Wafer-Scale, Monolithically Integrated WDM Platform for TB/s Optical Interconnects" OFC 2014 (10 Mar. 2014): <http://ieeexplore.ieee.org/document/6886645/?tp=&arnumber=6886645>

Li, Ming-Jun. "Novel Optical Fibers for Data Center Applications" SPIE Proceedings 9772. (12 Feb. 2016): 7–977205. <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=2492486>.

Li, Qing, et al. "Vertical Integration of High-Q Silicon Nitride Microresonators into Silicon-on-Insulator Platform" Optics Express 21.15 (29 July 2013): 18236–18248. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-21-15-18236>.

Li, Wei, et al. "Enhancement of Electroluminescence from Embedded Si Quantum Dots/SiO2multilayers Film by Localized-Surface-Plasmon and Surface Roughening" Scientific Reports 5. (3 July 2015): 11881. <http://www.nature.com/articles/srep11881>.

Li, Xianyao, et al. "40 Gb/s All-Silicon Photodetector Based on Microring Resonators" IEEE Photonics Technology Letters 27.7 (1 Apr. 2015): 729–732. <http://ieeexplore.ieee.org/document/7006639/?tp=&arnumber=7006639>

Li, Xiaoqiang, et al. "Graphene/h-BN/GaAs Sandwich Diode as Solar Cell and Photodetector" Optics Express 24.1 (11 Jan. 2016): 134–145. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-1-134>.

Li, Yu, et al. "Versatile Wideband Polarization-Insensitive Mode Converter Based on Wedge-Shaped Waveguide" IEEE Photonics Journal 8.2 (Apr. 2016): 1–11. <http://ieeexplore.ieee.org/document/7456205/?tp=&arnumber=7456205>

Li, Zhihong, et al. "DSP Free 56Gb/s ODB Generation Using Silicon Photonic Modulator with High Tolerance to CD and MPI" OSA Technical Digest (online) (Optical Society of America, 2016) (20 Mar. 2016): 3–4. <https://www.osapublishing.org/abstract.cfm?uri=OFC-2016-Th3G.4>.

Liang, D., et al. "Integrated Finely Tunable Microring Laser on Silicon" Nature Photonics (12 Sept. 2016): <http://www.nature.com/nphoton/journal/vaop/ncurrent/pdf/nphoton.2016.163.pdf>.

Liang, Di, and John E. Bowers. "Recent Progress in Lasers on Silicon" Nature Photonics 4.8 (30 July 2010): 511–517. <http://www.nature.com/nphoton/journal/v4/n8/abs/nphoton.2010.167.html>.

Liang, Di, Marco Fiorentino, and Raymond G. Beausoleil. "Advanced PIC Development for Large-Scale Data Centres and High-Performance Computers" PIC Magazine 30 Sept. 2016: n.pag. Web. <http://www.publishing.ninja/V4/page/2700/157/168#>.

Liao, Peicheng, et al. "Ultradense Silicon Photonic Interface for Optical Interconnection" IEEE Photonics Technology Letters 27.7 (1 Apr. 2015): 725–728. <http://ieeexplore.ieee.org/document/7006671/?tp=&arnumber=7006671>

LightCounting. "LightCounting Releases Combined Edition of Refreshed Active Optical Cable and Embedded Optical Modules Report" 29 Dec. 2015. Web. <http://www.lightcounting.com/News_122915.cfm>.

Lightwave Staff. "Increased Data Center Deployments Boost Active Optical Cable Market Says LightCounting" LightCounting. Lightwave Online, 16 Dec. 2014. Web. <http://www.lightwaveonline.com/articles/2014/12/increased-data-center-deployments-boost-active-optical-cable-market-says-lightcounting.html>.

Lightwave Staff. "Lightwave Logic Touts Polymer-Based Silicon Photonics Work" Tom Zelibor. lightwaveonline, 14 July 2016. Web.

<http://www.lightwaveonline.com/articles/2016/07/lightwave-logic-touts-polymer-based-silicon-photonics-work.html>.

Liles, Alexandros A., Kapil Debnath, and Liam O'Faolain. "Lithographic Wavelength Control of an External Cavity Laser with a Silicon Photonic Crystal Cavity-Based Resonant Reflector" Optics Letters 41.5 (18 Feb. 2016): 894. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-41-5-894>.

Lim, Andy E, et al. "Path to Silicon Photonics Commercialization: 25 Gb/s Platform Development in a CMOS Manufacturing Foundry Line" OSA Technical Digest (online) (Optical Society of America, 2014) (9 Mar. 2014): 2–51. <https://www.osapublishing.org/abstract.cfm?uri=ofc-2014-Th2A.51>.

Lim, Andy Eu-Jin, et al. "Review of Silicon Photonics Foundry Efforts" IEEE Journal of Selected Topics in Quantum Electronics 20.4 (July 2014): 405–416. <http://ieeexplore.ieee.org/document/6676843/?tp=&arnumber=6676843>

Lin, Pao Tai, et al. "Si-CMOS Compatible Materials and Devices for Mid-IR Microphotonics" Optical Materials Express 3.9 (26 Aug. 2013): 1474. <https://www.osapublishing.org/ome/abstract.cfm?uri=ome-3-9-1474>.

Liow, Tsung-Yang, et al. "28-Gb/s Monolithic Silicon Optical Modulator for Digital Coherent Communication" Fujikura Technical Review 2015. (13 Apr. 2015): <http://www.fujikura.co.jp/eng/rd/gihou/backnumber/pages/__icsFiles/afieldfile/2015/04/13/44e_08.pdf>.

Liow, Tsung-Yang, et al. "Silicon Quadrature Phase-Shift-Keying Modulator for 40-and 100-Gb/s Transmission" Fujikura Technical Review 2014. (4 July 2014): <http://www.fujikura.co.jp/eng/rd/gihou/backnumber/pages/__icsFiles/afieldfile/2014/07/04/43e_01.pdf>.

Lipka, Timo, et al. "Photonic Integrated Circuit Components Based on Amorphous Silicon-on-Insulator Technology" Photonics Research 4.3 (11 May 2016): 126. <https://www.osapublishing.org/prj/abstract.cfm?uri=prj-4-3-126&origin=search>.

Lisesivdin, Sefer, et al. "Optical Gain in 1.3-μm Electrically Driven Dilute Nitride VCSOAs" Nanoscale Research Letters 9.1 (2014): 22. <http://nanoscalereslett.springeropen.com/articles/10.1186/1556-276X-9-22>.

Lister, Katie. "Press Release Luxtera and STMicroelectronics to Enable High-Volume Silicon Photonics Solutions" Luxtera. 1 Mar. 2012. We. <http://www.luxtera.com/luxtera/2012313279thSTLuxtera.pdf>.

Littlejohns, Callum G, et al. "Localised Tuneable Composition Single Crystal Silicon-Germanium-on-Insulator for Low Cost Devices" Advances in Materials Science and Engineering 2016. (18 May 2016): <https://www.hindawi.com/journals/amse/2016/4154256/>.

Littlejohns, Callum G., et al. "50 Gb/s Silicon Photonics Receiver with Low Insertion Loss" IEEE Photonics Technology Letters 26.7 (29 Jan. 2014): 714–717. <http://ieeexplore.ieee.org/document/6728630/?tp=&arnumber=6728630>

Littlejohns, Callum G., et al. "Towards a Fully Functional Integrated Photonic-Electronic Platform via a Single SiGe Growth Step" Scientific Reports 6. (22 Sept. 2015): 19425. <http://www.nature.com/articles/srep19425>.

Liu, Alan Y, et al. "High Performance Continuous Wave 1.3 μm Quantum Dot Lasers on Silicon" Applied Physics Letters 104.4 (27 Jan. 2014): 41104. <http://scitation.aip.org/content/aip/journal/apl/104/4/10.1063/1.4863223>.

Liu, Alan Y., et al. "Quantum Dot Lasers for Silicon Photonics [Invited]" Photonics Research 3.5 (15 July 2015): 1–9. <https://www.osapublishing.org/prj/abstract.cfm?uri=prj-3-5-B1>.

Liu, Alan Y., et al. "Quantum dot lasers on silicon" 11th International Conference on Group IV Photonics (GFP). IEEE, 2015. 205–206. Web. <http://ieeexplore.ieee.org/document/6961926/>

Liu, Alan Y., et al. "Reliability of InAs/GaAs Quantum Dot Lasers Epitaxially Grown on Silicon" IEEE Journal of Selected Topics in Quantum Electronics 21.6 (14 Apr. 2015): 690–697. <http://ieeexplore.ieee.org/document/7085993/?tp=&arnumber=7085993>

Liu, Ansheng, et al. "A High-Speed Silicon Optical Modulator Based on a Metal-Oxide-Semiconductor Capacitor: Abstract: Nature" Nature 427.6975 (12 Feb. 2004): 615–618. <http://www.nature.com/nature/journal/v427/n6975/abs/nature02310.html>.

Liu, Ansheng, et al. "Announcing the world's first 40G silicon laser modulator" Intel labs 24 July 2007, Web. <https://blogs.intel.com/intellabs/2007/07/24/40g_modulator/>.

Liu, Huiyun. "InAs/GaAs Qiantum Dot Lasers Monolithically Grown on Silicon for Silicon Photonics" Integrated Photonics Research, Silicon and Nanophotonics 2016 (17 July 2016): <https://www.osapublishing.org/abstract.cfm?URI=iprsn-2016-ITu3A.2>.

Liu, Jifeng, et al. "Ge-on-Si Laser Operating at Room Temperature" Optics Letters 35.5 (1 Mar. 2010): 679–681. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-35-5-679>.

Liu, Jifeng. "Monolithically Integrated Ge-on-Si Active Photonics" Photonics 1.3 (2 July 2014): 162–197. <http://www.mdpi.com/2304-6732/1/3/162>.

Liu, Ke, and VolkerJ. Sorger. "Electrically-Driven Carbon Nanotube-Based Plasmonic Laser on Silicon" Optical Materials Express5.9 (1 Sept. 2015): 1910–1919. <https://www.osapublishing.org/ome/abstract.cfm?uri=ome-5-9-1910>.

Liu, Ke, et al. "Two-Dimensional Design and Analysis of Trench-Coupler Based Silicon Mach-Zehnder Thermo-Optic Switch" Optics Express 24.14 (5 July 2016): 15845–15853. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-14-15845&origin=search>.

Liu, Ken. "Ultra-Fast Pulse Propagation in Nonlinear Graphene/silicon Ridge Waveguide" Scientific Reports 5. (9 Jan. 2015): 16734. <http://www.nature.com/articles/srep16734>.

Liu, Ming. "Silicon Photonics: Graphene Benefits" Nature Photonics 7.11 (15 Sept. 2013): 851–852. <http://www.nature.com/nphoton/journal/v7/n11/pdf/nphoton.2013.257.pdf>.

Liu, Shuai, et al. "A Double-Balanced down Converter Mixer in GaN-on-Si HEMT Technology" Communication Problem-Solving (ICCP), 2014 IEEE International Conference on 2014. (7 Dec. 2014): <http://ieeexplore.ieee.org/document/7062343/?tp=&arnumber=7062343>

Liu, Zhixin, et al. "Modulator-Free Quadrature Amplitude Modulation Signal Synthesis" Nature Communications 5. (19 Dec. 2014): 5911. <http://www.nature.com/articles/ncomms6911>.

Losio, Giacomo. "Silicon Photonics: A Field That Is Constantly Changing" 16 Jan. 2015. Web. <http://www.photonics.com/Article.aspx?AID=57099>.

Lu, Fanglu, et al. "Nanolasers Grown on Silicon-Based MOSFETs" Optics Express 20.11 (21 May 2012): 12171–12176. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-20-11-12171>.

Lu, Huihui, et al. "Flip-Chip Integration of Tilted VCSELs onto a Silicon Photonic Integrated Circuit" Optics Express 24.15 (25 July 2016): 16258–16266. 17 July 2016. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-15-16258>.

Lu, Zeqin, et al. "Wideband Silicon Photonic Polarization Beamsplitter Based on Point-Symmetric Cascaded Broadband Couplers" Optics Express 23.23 (16 Nov. 2015): 29413–29422. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-23-29413>.

Luo, Xianshu, et al. "High-Throughput Multiple Dies-to-Wafer Bonding Technology and III/V-on-Si Hybrid" Frontiers in Materials 2. (Apr. 2015): <http://adsabs.harvard.edu/abs/2015FrMat...2...28L>.

Luo, Yuchan, et al. "Integrated Dual-Mode 3 DB Power Coupler Based on Tapered Directional Coupler" Scientific Reports 6. (25 Jan. 2016): 23516. <http://www.nature.com/articles/srep23516>.

Lutkowitz, Mark "Juniper's Aurrion Buyout: Tech Nightmare?" Aug. 2016, <http://fibereality.com/blog/junipers-aurrion-buyout-tech-nightmare/>.

Luxtera. "FAQs — Luxtera" 29 Mar. 2005. Web. <http://www.luxtera.com/faqs/>.

Lyubomirsky, Ilya, Brian Taylor, and Hans-Juergen Wolfgang Schmidtke. "An open approach for switching, routing, and transport." code.facebook.com. Facebook Code, 1 Nov. 2016. Web. <https://code.facebook.com/posts/1977308282496021/an-open-approach-for-switching-routing-and-transport/>.

Ma, Minglei, et al. "Silicon Photonic Polarization Receiver with Automated Stabilization for Arbitrary Input Polarizations" OSA Technical Digest Conference on Lasers and Electro-Optics.2016 (5 June 2016): 4–8. 13 June 2016. <https://www.osapublishing.org/abstract.cfm?URI=CLEO_SI-2016-STu4G.8>.

Maegami, Yuriko, et al. "Completely CMOS Compatible SiN-Waveguide-Based Fiber Coupling Structure for Si Wire Waveguides" Opt. Express 24.15 (18 July 2016): 16856. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-15-16856>.

Maegami, Yuriko, et al. "Spot-Size Converter with a SiO_2 Spacer Layer Between Tapered Si and SiON Waveguides for Fiber-to-Chip Coupling" Optics Express 23.16 (5 Aug. 2015): 21287. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-16-21287&origin=search>.

Magee, Laura. "New York State Photonics Board of Officers Welcomes Samtec as Newest Member of AIM Photonics" John Magglore. 23 Nov. 2016. Web. <https://esd.ny.gov/esd-media-center/press-releases/new-york-state-photonics-board-officers-welcomes-samtec-newest>.

Magretta, Joan. "Understanding Michael Porter: The essential guide to competition and strategy" 1st edition ed. Boston, MA: Harvard Business Review Press, 2011. Web.

<https://www.amazon.com/Understanding-Michael-Porter-Essential-Competition/dp/1422160599>.

Mah, Paul. "Taking a Closer Look at Telin-3" Telin Singapore. DatacenterDynamics, 6 Dec. 2016. Web. <http://www.datacenterdynamics.com/content-tracks/design-build/taking-a-closer-look-at-telin-3/97445.fullarticle>.

Mak, Jason C. C., et al. "Binary Particle Swarm Optimized 2 × 2 Power Splitters in a Standard Foundry Silicon Photonic Platform" Optics Letters 41.16 (2016): 3868. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-41-16-3868>.

Malka, Dror, Yoav Sintov, and Zeev Zalevsky. "Design of a 1 × 4 Silicon-Alumina Wavelength Demultiplexer Based on Multimode Interference in Slot Waveguide Structures" Journal of Optics 17.12 (9 Oct. 2015): 125702. <http://iopscience.iop.org/article/10.1088/2040-8978/17/12/125702/meta>.

Marchena, Elton, et al. "448 Gbit/s DP-16QAM Transmission Using Integrated Tunable CMOS Laser Sources" OSA Technical Digest (online) (Optical Society of America, 2014) OFC 2014. (9 Mar. 2014): 3. <https://www.osapublishing.org/abstract.cfm?uri=OFC-2014-Th3J.3>.

Markle, Kim. "Inphi Unveils Highly Integrated Silicon Photonics Technology Platform for 100G Data Center Applications" Inphi. inphi.com, 22 Mar. 2016. Web. <https://www.inphi.com/media-center/press-room/press-releases-and-media-alerts/inphi-unveils-highly-integrated-silicon-photonics-technology-platform-for-100g-data-center-applications.php>.

Marko, Igor P., et al. "Optical Gain in GaAsBi/GaAs Quantum Well Diode Lasers" Scientific Reports 6. (12 Jan. 2016): 28863. <http://www.nature.com/articles/srep28863>.

Mashanovich, G Z, et al. "Silicon Photonic Waveguides for Different Wavelength Regions" Semiconductor Science and Technology23.6 (12 May 2008): 064002. <http://iopscience.iop.org/article/10.1088/0268-1242/23/6/064002/pdf>.

Matsui, Yasuhiro, et al. "28-Gbaud PAM4 and 56-Gb/s NRZ Performance Comparison Using 1310-Nm Al-BH DFB Laser" Journal of Lightwave Technology 34.11 (1 June 2016): 2677–2683. 13 June 2016. <https://www.osapublishing.org/jlt/abstract.cfm?uri=jlt-34-11-2677>.

Matsumoto, Craig. "Ericsson Uses Silicon Photonics to Virtualize Physical Ports" Ericsson. SDxCentral, 19 Aug. 2016. Web. <https://www.sdxcentral.com/articles/news/ericsson-uses-silicon-photonics-virtualize-physical-ports/2016/08/>.

Matsumoto, Takeshi, et al. "In-Line Optical Amplification for Si Waveguides on 1x8 Splitter and Selector by Flip-Chip Bonded InP-SOAs" OSA Technical Digest (online) (Optical Society of America, 2016), (20 Mar. 2016): 1. <https://www.osapublishing.org/abstract.cfm?uri=OFC-2016-Th1C.1>.

Matsuo, S., et al. "40-Gbit/s Direct Modulation of Membrane Buried Heterostructure DFB Laser on SiO2/Si Substrate" Semiconductor Laser Conference (ISLC), 2014 International (7 Sept. 2010): 30–31. <http://ieeexplore.ieee.org/document/6987435/?tp=&arnumber=6987435>

Matsuo, Shinji, et al. "40-Gbit/s Direct Modulation of Membrane Buried Heterostructure DFB Laser on SiO2/Si Substrate" 2014 International Semiconductor Laser Conference (Sept. 2014): n.pag. <http://ieeexplore.ieee.org/document/6987435/?tp=&arnumber=6987435>

Matsuo, Shinji, et al. "On-Silicon Integration of Compact and Energy-Efficient DFB Laser with 40-Gbit/s Direct Modulation" IEEE 12th International Conference on Group IV Photonics 2015. (28 Aug. 2015): 23–24. <http://ieeexplore.ieee.org/document/7305935/?tp=&arnumber=7305935>

Matsuo, Shinji, Koji Takeda, and Takuro Fujii. "Heterogeneously Integrated Photonic Crystal Laser on Si" Conference on Lasers and Electro-Optics (10 June 2016): <https://www.osapublishing.org/abstract.cfm?uri=CLEO_SI-2016-SF1E.5>.

Matthew Streshinsky et al. "The Road to Affordable, Large-Scale Silicon Photonics" Optics & Photonics 1 Sept. 2013: Web. <http://www.osa-opn.org/home/articles/volume_24/september_2013/features/the_road_to_affordable,_large-scale_silicon_photon/#.VnIuWfkrJhE>.

Maximov, Mikhail V, et al. "Ultrasmall Microdisk and Microring Lasers Based on InAs/InGaAs/GaAs Quantum Dots" Nanoscale Research Letters 9.1 (4 Dec. 2014): 657. <https://nanoscalereslett.springeropen.com/articles/10.1186/1556-276X-9-657>.

Mayer, B, et al. "Continuous Wave Lasing from Individual GaAs-AlGaAs Core-Shell Nanowires" Applied Physics Letters 108.7 (18 Feb. 2016): 71107. <http://scitation.aip.org/content/aip/journal/apl/108/7/10.1063/1.4942506>.

Mayer, B., et al. "Monolithically Integrated High-β Nanowire Lasers on Silicon" Nano Letters 16.1 (13 Jan. 2016): 152–156. <http://pubs.acs.org/doi/abs/10.1021/acs.nanolett.5b03404?journalCode=nalefd>.

Mayer, Benedikt, et al. "Lasing from Individual GaAs-AlGaAs Core-Shell Nanowires up to Room Temperature" Nature Communications 4. (5 Dec. 2013): <http://www.nature.com/articles/ncomms3931>.

Mellanox Technologies Ltd. "Mellanox Technologies, Ltd. Announces Definitive Agreement to Acquire EXchip" mellanox.com. 2015. Web. <https://www.mellanox.com/page/press_release_item?id=1610&ssn=jmffb4kvifepu7k7rhqbro80o0>.

Mellanox. "Mellanox Introduces Next Generation 100Gb/s Silicon Photonics Transceivers (NASDAQ: MLNX)" ir.mellanox.com. 23 Mar. 2015. Web. <http://ir.mellanox.com/releasedetail.cfm?releaseid=902825>.

Menezo, Sylvie, et al. "Transmitter Made up of a Silicon Photonic IC and Its Flip-Chipped CMOS IC Driver Targeting Implementation in FDMA-PON" Journal of Lightwave Technology 34.10 (15 May 2015): 2391–2397. <http://ieeexplore.ieee.org/document/7422667/?tp=&arnumber=7422667>

Mercante, Andrew J, et al. "110 GHz CMOS Compatible Thin Film LiNbO3 Modulator on Silicon" Optics Express 24.14 (11 July 2016): 15590–15595. 17 July 2016. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-14-15590>.

Merlo, Juan M., et al. "Wireless Communication System via Nanoscale Plasmonic Antennas" Scientific Reports 6. (6 May 2016): 31710. <http://www.nature.com/articles/srep31710>.

Merritt, Rick. "Facebook likes 100G at $1/G" EE Times. EETimes, 2015. Web. <http://www.eetimes.com/document.asp?doc_id=1327552>.

Merritt, Rick. "Facebook shifts switch to 100G" EETimes.com. EETimes, 19 Nov. 2015. Web. <http://www.eetimes.com/document.asp?doc_id=1328303>.

Merritt, Rick. "Slideshow: Intel lights 100G Interconnects at Facebook summit" EETimes.com. EETimes, 17 Jan. 2013. Web. <http://www.eetimes.com/document.asp?doc_id=1262984>.

Metras, Hughes. "The Promises of Silicon Photonics: Current Status and Future Trends" OFC2015: Yole Developpment, 22 Mar. 2015. Web. <http://www.ofcconference.org/library/images/ofc/2015/Market%20Watch%20and%20SPS/Hughes-METRAS3.pdf>.

Mi, Zetian. "Multi-Wavelength InAs Quantum Dot Microtube Lasers on Si Report Title" United States Army Research Office, 13 Jan. 2010. Web. <http://www.dtic.mil/dtic/tr/fulltext/u2/a535081.pdf>.

Mikkelsen, Benny. "Challenges and Key Technologies for Coherent Metro 100G Transceivers" Maynard, MA: Acacia Communications, 1 Nov. 2012. Web. <http://acacia-inc.com/wp-content/uploads/2013/09/Challenges-and-key-technologies-for-coherent-metro-100G-transceivers-Lightwave.pdf>.

Milivojevic, Biljana, et al. "112Gb/s DP-QPSK Transmission over 2427km SSMF Using Small-Size Silicon Photonic IQ Modulator and Low-Power CMOS Driver" OSA Technical Digest (online) (Optical Society of America, 2013) (17 Mar. 2013): 1. <https://www.osapublishing.org/abstract.cfm?uri=OFC-2013-OTh1D.1>.

Miller, Rich. "Who has the most web servers?" Data Center Knowledge. Data Center Knowledge, 14 May 2009. Web. <http://www.datacenterknowledge.com/archives/2009/05/14/whos-got-the-most-web-servers/>.

Miller, Steven A., et al. "Tunable Frequency Combs Based on Dual Microring Resonators" Optics Express 23.16 (10 Aug. 2015): 21527–21540. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-16-21527&origin=search>.

Mirshafiei, Mehrdad, et al. "Glass Interposer for Short Reach Optical Connectivity" Optics Express 24.11 (30 May 2016): 12375–12384. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-11-12375>.

MIT Microphotonics Center. "Microphotonics: Hardware for the Information Age" MIT, 18 May 2005. Web. <https://mphotonics.mit.edu/docman/ctr/ctr-1/294-5-ctr2005-silicon/file>.

Mogami, T., et al. "A 300mm Si Photonics Platform for Optical Interconnection" 2015 IEEE International Interconnect Technology Conference and 2015 IEEE Materials for Advanced Metallization Conference (IITC/MAM) (21 May 2015): 273–276. <http://ieeexplore.ieee.org/document/7325665/?tp=&arnumber=7325665>

Mogami, Tohru, et al. "High-Performance Optical Waveguide Devices Using 300 Mm Si Photonics Platform" Microelectronic Engineering (20 Apr. 2016): <http://www.sciencedirect.com/science/article/pii/S0167931715300848>.

Mohapatra, P K, et al. "Interaction of Graphene Quantum Dots with Bulk Semiconductor Surfaces" AIP Connference Proceedings1661.1 (15 May 2015): 100008. <http://scitation.aip.org/content/aip/proceeding/aipcp/10.1063/1.4915443>.

Morandotti, Roberto, and David Moss. "Hydex Glass and Amorphous Silicon for Integrated Nonlinear Optical Signal Processing" arXiv (12 May 2015): <https://arxiv.org/abs/1505.02846>.

Morgan, Timothy Prickett. "Intel Leverages Chip Might to Etch Photonics Future" Intel. The Next Platform, 17 Aug. 2016. Web. <https://www.nextplatform.com/2016/08/17/intel-leverages-chip-might-etch-photonics-future/>.

Morgan, Timothy Prickett. "The Road to 200G Networks Starts with the Transceiver" Arlon Martin. The Next Platform, 22 Mar. 2016. Web. <https://www.nextplatform.com/2016/03/22/road-200g-networks-starts-transceiver/>.

Moroni, Stefano T., et al. "Indium Segregation During III–V Quantum Wire and Quantum Dot Formation on Patterned Substrates" J. Appl. Phys. 117.16 (30 Apr. 2015): 164313. <http://aip.scitation.org/doi/abs/10.1063/1.4919362?journalCode=jap>.

Moscoso-Mártir, Alvaro, et al. "Title: Silicon Photonics WDM Transceiver with SOA and Semiconductor Mode-Locked Laser" arXiv(27 May 2016): <https://arxiv.org/abs/1605.08668>.

Moss, D. J., and R. Morandotti. "Nonlinear Optical Signal Processing in High Figure of Merit CMOS Compatible Platforms" Integrated Optics: Physics and Simulations II (1 May 2015): <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=2290726>.

Moss, David J., et al. "New CMOS-Compatible Platforms Based on Silicon Nitride and Hydex for Nonlinear Optics" Nature Photonics 7.2013 (30 July 2013): <http://www.nature.com/nphoton/journal/v7/n8/full/nphoton.2013.183.html>.

Moss, Sebastian. "Dell Reveals "project Triton" Water Cooling Tech, in Use by EBay" DatacenterDynamics, 2 June 2016. Web. <http://www.datacenterdynamics.com/content-tracks/power-cooling/dell-reveals-project-triton-water-cooling-tech-in-use-by-ebay/96312.fullarticle>.

Mostak, Todd. "The Age of the GPU Is Upon Us" MapD. The Next Platform, 31 May 2016. WEb. <http://www.nextplatform.com/2016/05/31/age-gpu-upon-us/>.

Nadovich, Christopher T, et al. "Simulation of Vector Mode Grating Coupler Interfaces for Integrated Optics" 2015 Comsol Conference (5 Nov. 2015): <https://www.comsol.com/paper/download/256671/nadovich_paper.pdf>.

Nah, Jae-Woong, et al. "Flip Chip Assembly with Sub-Micron 3D Re-Alignment via Solder Surface Tension" ECTC 2015 (29 May 2015): <http://ieeexplore.ieee.org/document/7159568/?tp=&arnumber=7159568>

Nakamura, Shigeru, et al. "Compact and Low-Loss 8x8 Silicon Photonic Switch Module for Transponder Aggregators in CDC-ROADM Application" OSA Technical Digest (online) (Optical Society of America, 2015) (22 Mar. 2015): 2–6. <https://www.osapublishing.org/abstract.cfm?uri=OFC-2015-M2B.6>.

nanowerk. "2D Molybdenum Disulfide: A Promising New Optical Material for Ultra-Fast Photonics" Nanowerk Spotlight. 30 Oct. 2014. Web. <http://www.nanowerk.com/spotlight/spotid=37913.php>.

Natural Resources Defense Council. "NRDC: Data center efficiency assessment - scaling up energy efficiency across the data center industry - evaluating key drivers and barriers" 2014. Web. <https://www.nrdc.org/sites/default/files/data-center-efficiency-assessment-IP.pdf>.

Negro, Luca Dal, et al. "Laser Device Based on Silicon Nanostructures" United States Patent: INFM Instituto per la Fislca Della Materia et. al., 9 Dec. 2003. Web. <http://pdfpiw.uspto.gov/.piw?Docid=06661035>.

Neisser, Mark, and Stefan Wurm. "ITRS Lithography Roadmap: 2015 Challenges: Advanced Optical Technologies" Advanced Optical Technologies 4.4 (31 Aug. 2015): 235–240. <http://www.degruyter.com/view/j/aot.2015.4.issue-4/aot-2015-0036/aot-2015-0036.xml>.

Nikitin, A. Y., et al. "Real-Space Mapping of Tailored Sheet and Edge Plasmons in Graphene Nanoresonators" Nature Photonics10.4 (21 Mar. 2016): 239–243. <http://www.nature.com/nphoton/journal/v10/n4/abs/nphoton.2016.44.html>.

Nikolova, Dessislava, et al. "Scaling Silicon Photonic Switch Fabrics for Data Center Interconnection Networks" Optics Express23.2 (20 Jan. 2015): 1159. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-2-1159>.

Nikolova, Dessislava, et al. "Title: A Highly Scalable Fully Non-Blocking Silicon Photonic Switch Fabric" arXiv 1512.09323 (31 Dec. 2015): <https://arxiv.org/abs/1512.09323>.

Niu, Gang, et al. "Dislocation-Free Ge Nano-Crystals via Pattern Independent Selective Ge Heteroepitaxy on Si Nano-Tip Wafers" Scientific Reports 6. (21 Jan. 2016): 22709. <http://www.nature.com/articles/srep22709>.

Niu, Gang, et al. "Photodetection in Hybrid Single-Layer Graphene/fully Coherent Germanium Island Nanostructures Selectively Grown on Silicon Nanotip Patterns" ACS Applied Materials & Interfaces 8.3 (27 Jan. 2016): 2017–2026. <http://pubs.acs.org/doi/abs/10.1021/acsami.5b10336?journalCode=aamick>.

Nizamuddin, M., et al. "Design, Simulation and Comparative Analysis of CNT Based Cascode Operational Transconductance Amplifiers" Nanotechnology 26.39 (5 Sept. 2015): <http://iopscience.iop.org/article/10.1088/0957-4484/26/39/395201/meta;jsessionid=B381C5719D47A9B6F766824A199A92E3.c1#>.

Noury, Adrien, et al. "Controlling Carbon Nanotube Photoluminescence Using Silicon Microring Resonators" arXiv (5 Aug. 2015): <https://arxiv.org/abs/1508.01007>.

Nozaki, Kengo, et al. "25-Channel All-Optical Switches by Integrated Silicon Photonic Crystal Nanocavities" OSA Technical DigestCLEO 2013. (June 2013): <https://www.osapublishing.org/abstract.cfm?URI=CLEO_SI-2013-CM4F.1>.

Nozaki, Kengo, et al. "Photonic-Crystal Nano-Photodetector with Ultrasmall Capacitance for on-Chip Light-to-Voltage Conversion Without an Amplifier" Optica 3.5 (20 May 2016): 483–492. <https://www.osapublishing.org/optica/abstract.cfm?uri=optica-3-5-483>.

O'BrienPeterA, et al. "PLAT4M: Progressing Silicon Photonics in Europe" Photonics 3.1 (24 Dec. 2015): 1. <http://www.mdpi.com/2304-6732/3/1/1>.

O'Brien, Peter. "Packaging of integrated Photonic devices; applications, user foundry services & design rules" Cork, Ireland: Tyndall National Institute, 2015. Web.

<http://www.enas.fraunhofer.de/content/dam/enas/de/documents/Downloads/Chemnitzer%20Seminare/Seminar_22_SP_2015/Packaging%20of%20Integrated%20Photonic%20Devices.pdf>.

O'Shea, Dan. "Optical Feels the Facebook Effect" LightReading. Light Reading, 3 Apr. 2015. Web. <http://www.lightreading.com/optical/100g/optical-feels-the-facebook-effect/a/d-id/714866>.

Offrein, Bert J. "Silicon Photonics for the Datacenter" Optical Fiber Communications Conference and Exhibition (OFC) 2015 2015. (26 Mar. 2015): 1–3. <http://ieeexplore.ieee.org/document/7122018/?tp=&arnumber=7122018>

Okamoto, Daisuke, et al. "A 25-Gb/s 5 × 5mm^2 Chip-Scale Silicon-Photonic Receiver Integrated with 28-Nm CMOS Transimpedance Amplifier" Journal of Lightwave Technology 34.12 (12 Nov. 2015): <http://ieeexplore.ieee.org/document/7328241/?tp=&arnumber=7328241>

Okumura, Tadashi, et al. "25 Gbps Silicon Photonics Multi-Mode Fiber Link with Highly Alignment Tolerant Vertically Illuminated Germanium Photodiode" Silicon Photonics X (27 Feb. 2015): <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=2190879>.

Orcutt, Jason S., et al. "Open Foundry Platform for High-Performance Electronic-Photonic Integration" Optics Express 20.11 (21 May 2012): 12222–12232. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-20-11-12222>.

Orcutt, Jason, et al. "Monolithic Silicon Photonics at 25Gb/s" OSA Technical Digest (online) (Optical Society of America, 2016) (20 Mar. 2016): 1–4. <https://www.osapublishing.org/abstract.cfm?uri=OFC-2016-Th4H.1>.

Ouellette, Jason. "Acacia Communications Introduces Long-Haul CFP-DCO Module" Acacia Communications. GlobeNewswire, 19 Sept. 2016. Web. <https://globenewswire.com/news-release/2016/09/19/872643/0/en/Acacia-Communications-Introduces-Long-Haul-CFP-DCO-Module.html>.

Overton, Gail. "Ranovus Launches 200G Quantum-Dot-Laser-Based Datacenter Interconnect Platform" Hamid Arabzadeh. Laser Focus World, 12 Sept. 2016. Web. <http://www.laserfocusworld.com/articles/2016/09/ranovus-launches-200g-quantum-dot-laser-based-datacenter-interconnect-platform.html>.

Palkert, Tom. "Next Gen 100G Interconnect Technical Feasibility Using Silicon Photonics" IEEE (Luxtera), 8 Nov. 2011. Web. <http://www.ieee802.org/3/100GNGOPTX/public/nov11/palkert_01_1111_NG100GOPTX.pdf>.

Pantouvaki, Marianna, et al. "50Gb/s Silicon Photonics Platform for Short-Reach Optical Interconnects" 50Gb/s Silicon Photonics Platform for Short-Reach Optical Interconnects (20 Mar. 2016): 4. <https://www.osapublishing.org/abstract.cfm?uri=OFC-2016-Th4H.4>.

Papes, Martin, et al. "Fiber-Chip Edge Coupler with Large Mode Size for Silicon Photonic Wire Waveguides" Optics Express 24.5 (29 Feb. 2016): 5026–5038. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-5-5026>.

Parashar, Vyom, et al. "Switching Behaviors of Graphene-Boron Nitride Nanotube Heterojunctions" Scientific Reports 5. (11 Jan. 2015): 12238. <http://www.nature.com/articles/srep12238>.

Park, Gyeong Cheol, et al. "Hybrid vertical-cavity laser with lateral emission into a silicon waveguide" 10 Nov. 2014. Web. 10 Jan. 2017. <https://arxiv.org/abs/1411.2483v1>.

Park, Hyundai, et al. "Hybrid Silicon Evanescent Laser Fabricated with a Silicon Waveguide and III-V Offset Quantum Wells" Optics Express 13.23 (4 Nov. 2005): 9460. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-13-23-9460>.

Park, Hyundai, et al. "Photonic Integration on the Hybrid Silicon Evanescent Device Platform" Advances in Optical Technologies 2008. (12 Mar. 2008): 1–17. <https://www.hindawi.com/journals/aot/2008/682978/>.

Park, Jay. "Designing a very efficient data center" facebook. 14 Apr. 2011. Web. <https://www.facebook.com/notes/facebook-engineering/designing-a-very-efficient-data-center/10150148003778920/>.

Pasternak, Iwona, et al. "Graphene Growth on Ge(100)/Si(100) Substrates by CVD Method" Scientific Reports 6. (22 Feb. 2016): 21773. <http://www.nature.com/articles/srep21773>.

Patel, Chandrakant D, and Amip J Shah. "Cost model for planning, development and operation of a data center" Palo Alto, CA: Hewlett Packard, June 2005. Web. <http://www.hpl.hp.com/techreports/2005/HPL-2005-107R1.pdf>.

Patel, D., et al. "Silicon Photonic Segmented Modulator-Based Electro-Optic DAC for 100 Gb/s PAM-4 Generation" IEEE Photonics Technology Letters 27.23 (1 Dec. 2001): 2433–2436. <http://ieeexplore.ieee.org/document/7185365/?tp=&arnumber=7185365>

Pavarelli, Nicola, et al. "Optical and Electronic Packaging Processes for Silicon Photonic Systems" Journal of Lightwave Technology 33.5 (1 Mar. 2015): 991–997. <http://ieeexplore.ieee.org/document/7042806/?tp=&arnumber=7042806>

Pavarelli, Nicola, Jun Su Lee, and Peter A O'Brien. "Packaging Challenges for Integrated Silicon Photonic Circuits" Proc. SPIE 9133, Silicon Photonics and Photonic Integrated Circuits IV, 91330F (14 Apr. 2014): 9–91330. <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=1868096>.

Peach, Matthew. "OFC 2016: Silicon Photonics Launches for Growing Market" optics.org, 23 Mar. 2016. Web. <http://optics.org/news/7/3/35>.

Peeters Weem, Jan, Gopal Hegde, and Tom Mader. "Market, Technical, Cost and Solution Considerations for HSSG" Intel Corporation, 29 Nov. 2006. Web. <http://www.ieee802.org/3/hssg/public/nov06/peeters_01_1106.pdf>.

Peterson, Tommy. "Intel pushes silicon toward light speed" computerworld.com. Computerworld, 23 Feb. 2004. Web. <http://www.computerworld.com/article/2574245/networking/intel-pushes-silicon-toward-light-speed.html>.

Petousi, Despoina, et al. "Monolithically Integrated High-Extinction-Ratio MZM with a Segmented Driver in Photonic BiCMOS." IEEE Photonics Technology Letters 28.24 (15 Dec. 2016): 2866–2869. <http://ieeexplore.ieee.org/document/7731238/>.

Phare, Christopher T., et al. "Graphene Electro-Optic Modulator with 30 GHz Bandwidth" Nature Photonics 9.8 (13 July 2015): 511–514. <http://www.nature.com/nphoton/journal/v9/n8/full/nphoton.2015.122.html>.

Photonics. "Imec Opens Florida Design Center for PICs, Expands Foundry Services" Photonics Media. 8 July 2016. Web. <http://www.photonics.com/Article.aspx?AID=60867>.

Photonics21. "Towards 2020-Photonics Driving Economic Growth in Europe" ec.europa.eu: Photonics21, 30 Apr. 2013. Web. <http://www.photonics21.org/download/Brochures/Photonics_Roadmap_final_lowres.pdf>.

PI (Physik Instrumente) LP. "Multi-Channel Optical Alignment for Testing and Packaging in Silicon Photonics Devices" web: AZoNano, 10 Apr. 2015. Web. <http://www.azonano.com/article.aspx?ArticleID=4001>.

Plant, David V. "Silicon Photonic Enabled 400G/1T Short Reach Optical Interconnects for Data Center Applications" 2015 IEEE Optical Interconnects Conference (OI) (22 Apr. 2015): <http://www.ieeeexplore.ws/document/7115718/>.

Plummer, Daryl C., et al. "Top Strategic Preditions for 2016 and Beyond: The Future Is a Digital Thing" Gartner, 2 Oct. 2015. Web. <https://www.gartner.com/doc/3142020?aeId=>.

Pollnau, Markus. "Rare-Earth-Doped Lasers on a Silicon Chip" 2015 European Conference on Lasers and Electro-Optics - European Quantum Electronics Conference (21 June 2015): 1–12. <https://www.osapublishing.org/abstract.cfm?uri=CLEO_Europe-2015-CK_12_1>.

Pollnau, Markus. "Rare-Earth-Ion-Doped Channel Waveguide Lasers on Silicon" IEEE Journal of Selected Topics in Quantum Electronics 21.1 (Jan. 2015): 414–425. <http://ieeexplore.ieee.org/document/6883134/?tp=&arnumber=6883134>

Pond, James, et al. "Design and Optimization of Photolithography Friendly Photonic Components" SPIE Proceedings 9751.Smart Photonic and Optoelectronic Integrated Circuits XVIII (13 Mar. 2016): 6–97510. <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=2499879>.

Pool, Rebecca. "The Problem with Packaging" Fibre Systems 15 June 2015: Web. <http://www.fibre-systems.com/feature/problem-packaging>.

Poon, Joyce K. S., et al. "Multilayer Silicon Nitride-on-Silicon Integrated Photonic Platforms" 2015 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS) (14 Oct. 2015): n.pag. <http://ieeexplore.ieee.org/document/7314518/?tp=&arnumber=7314518>

Popović, Miloš A, et al. "Monolithic Silicon Photonics in a Sub-100nm SOI CMOS Microprocessor Foundry: Progress from Devices to Systems" Silicon Photonics X (3 Apr. 2015): 10–93670. <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=2241763>.

Popović, Miloš A., et al. "Monolithic Silicon Photonics in a Sub-100nm SOI CMOS Microprocessor Foundry: Progress from Devices to Systems" Silicon Photonics X (3 Apr. 2015): <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=2241763>.

Pospischil, Andreas, et al. "CMOS-Compatible Graphene Photodetector Covering All Optical Communication Bands" Nature Photonics 7.11 (15 Sept. 2013): 892–896. <http://www.nature.com/nphoton/journal/v7/n11/full/nphoton.2013.240.html>.

Pressman, Aaron. "Intel May Have New Super-Fast Technology To Connect Chips" Christopher Rolland. Fortune, 8 Nov. 2016. Web. <http://fortune.com/2016/11/08/intel-super-fast-technology-to-connect-chips/>.

PRWeb. "Lumerical's 2015b release offers a new laser compact model and improved Graphene simulation capabilities" benziga.com. Benzinga, 20 May 2015. Web. <http://www.benzinga.com/pressreleases/15/05/p5526096/lumericals-2015b-release-offers-a-new-laser-compact-model-and-improved->.

Pu, Jing, et al. "Heterogeneous Integrated III–V Laser on Thin SOI with Single-Stage Adiabatic Coupler: Device Realization and Performance Analysis" IEEE Journal of Selected Topics in Quantum Electronics 21.6 (Nov. 2015): 369–376. <http://ieeexplore.ieee.org/document/7084625/?tp=&arnumber=7084625>

Pu, Minhao, et al. "Efficient Frequency Comb Generation in AlGaAs-on-Insulator" Optica 3.8 (26 July 2016): 823. <https://www.osapublishing.org/optica/abstract.cfm?uri=optica-3-8-823>.

Pyatkov, Felix, et al. "Cavity-Enhanced Light Emission from Electrically Driven Carbon Nanotubes" Nature Photonics 10.6 (18 Apr. 2016): 420–427. <http://palgrave.nature.com/nphoton/journal/v10/n6/full/nphoton.2016.70.html>.

Rabiei, Payam, et al. "Heterogeneous Lithium Niobate Photonics on Silicon Substrates" Optics Express 21.21 (21 Oct. 2013): 25573–25581. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-21-21-25573>.

Rahman, Mohd Syuhaimi Ab, Khaled Mohamed, and Rahmah Mohammad. "An Optimum Design of 3×3 Optical Switch Based on Integrated MZI, Including the Influence of Electro Optic — the National University of Malaysia" WSEAS Transactions on Communications 9.6 (30 June 2010): 354–363. <https://ukm.pure.elsevier.com/en/publications/an-optimum-design-of-33-optical-switch-based-on-integrated-mzi-in>.

Rakowski, M., et al. "22.5 A 4×20Gb/s WDM Ring-Based Hybrid CMOS Silicon Photonics Transceiver" Solid- State Circuits Conference - (ISSCC), 2015 IEEE International (26 Oct. 2015): 1–3. <http://ieeexplore.ieee.org/document/7063099/?tp=&arnumber=7063099>

Ramadan, Tarek A. "A Novel Design of a Wideband Digital Vertical Multimode Interference Coupler" Journal of Lightwave Technology 34.17 (1 Sept. 2016): 4015–4022. <http://ieeexplore.ieee.org/document/7516700/?tp=&arnumber=7516700>

Rattner, Justin, and Mario Paniccia. "The 50Gbps Si Photonics Link A Research Milestone from Intel Labs" Santa Clara, CA: Intel, 27 July 2010. Web. <http://download.intel.com/pressroom/pdf/photonics/50G_Silicon_Photonics_Link.pdf?iid=pr_smrelease_vPro_materials1>.

Ray, Tiernan. "Acacia CEO Shanmugaraj: If It's a Cycle, It's a Long One" Tech Trader Daily. Barrons, 12 Aug. 2016. Web. <http://blogs.barrons.com/techtraderdaily/2016/08/12/acacia-ceo-shanmugaraj-if-its-a-cycle-its-a-long-one/>.

Ray, Tiernan. "Ayar Labs: Ambitious Optical Startup Has Plans for "400-Gig" and Beyond" Alex Wright-Gladstein. Barrons, 15 Sept. 2016. Web. <http://blogs.barrons.com/techtraderdaily/2016/09/15/ayar/>.

Ray, Tiernan. "Intel's "miraculous," "mind-blowing" New Chips, Per Susquehanna" Christopher Rolland. Barrons, 8 Nov. 2016. Web. <http://blogs.barrons.com/techtraderdaily/2016/11/08/intels-miraculous-mind-blowing-new-chips-per-susquehanna/>.

Reed, Graham T., et al. "Silicon Photonics Waveguides" helios, 30 Nov. 2010. Web. <http://www.helios-project.eu/content/download/360/2306/file/ch2%20waveguiding.pdf.>.

Reserbat-Plantey, Antoine, et al. "Electromechanical Control of Nitrogen-Vacancy Defect Emission Using Graphene NEMS" Nature Communications 7. (27 Aug. 2015): 10218. <http://www.nature.com/articles/ncomms10218>.

Richter, J., M. P. Nezhad, and J. Witzens. "Monolithically Integrated Waveguide-Coupled Silica Microtoroids" arXiv 1510.07407. (26 Oct. 2015): <http://arxiv.org/ftp/arxiv/papers/1510/1510.07407.pdf>.

Roelkens, G., et al. "III–V-on-Silicon Photonic Integrated Circuits for Communication and Sensing Applications" 2015 IEEE Photonics Conference (IPC) (8 Oct. 2015): <http://ieeexplore.ieee.org/document/7323470/?tp=&arnumber=7323470>

Roelkens, Günther, et al. "Hybrid Silicon Lasers" Optoelectronic Integrated Circuits XIII (22 Jan. 2011): <http://www.photonics.intec.ugent.be/download/pub_2704.pdf>.

Rohan. "Photonic Integrated Circuit Market Is Growing at an an Estimated CAGR of 26.3% & to Reach $1, 547.6 Million by 2022" MarketsAndMarkets. 22 Jan. 2013. Web. <http://www.prweb.com/releases/quantum-computing/market/prweb10347380.htm>.

Romero-García, S., et al. "Alignment Tolerant Couplers for Silicon Photonics" IEEE Journal of Selected Topics in Quantum Electronics 21.6 (Dec. 2015): 765–778. <http://ieeexplore.ieee.org/document/7105843/?tp=&arnumber=7105843>

Rong, Haisheng, et al. "A Cascaded Silicon Raman Laser: Abstract: Nature Photonics" Nature Photonics 2.3 (24 Feb. 2008): 170–174. <http://www.nature.com/nphoton/journal/v2/n3/pdf/nphoton.2008.4.pdf>.

Rong, Haisheng, et al. "An All-Silicon Raman Laser: Abstract: Nature" Nature 433.7023 (5 Jan. 2005): 292–294. <http://www.nature.com/nature/journal/v433/n7023/abs/nature03273.html>.

Roof, Katie, and Kate Conger. "Acacia Soars 35% in Second Tech IPO of the Year" Nasdaq. TechCrunch, 13 May 2016. Web. <https://techcrunch.com/2016/05/13/acacia-soars-36-in-second-tech-ipo-of-the-year/>.

Rosa, Á, et al. "High Performace Silicon 2x2 Optical Switch Based on a Thermo-Optically Tunable Multimode Interference Coupler and Efficient Electrodes" Optics express. 24.1 (3 Feb. 2016): 191–8. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-1-191>.

Rubenstein, Roy. "European Project Developing Integrated Silicon Photonics Process" Bert Offrein. Optical Connections News, 7 Dec. 2016. Web. <http://opticalconnectionsnews.com/2016/12/european-project-developing-integrated-silicon-photonics-process/>.

Rubenstein, Roy. "The Tipping Point for Silicon Photonics" Fibre Systems 8 June 2016: Web. <http://www.fibre-systems.com/feature/tipping-point-silicon-photonics>.

Rubenstein, Roy. "The Case for Silicon Photonics" Optical Communication News, Sept. 2015. Web. <http://opticalconnectionsnews.com/wp-content/uploads/2015/06/Optical-Connections-2015-Q3-44pp-Final-LR.pdf>.

Rust, Adamson. “Intel Funds Silicon Photonics Foundry Service” Michael Hochberg. TechEye, 11 Feb. 2011. Web. <http://www.techeye.net/chips/intel-funds-silicon-photonics-foundry-service>.

Saeedi, Saman, Sylvie Menezo, and Azita Emami. “A 25Gbps 3D-Integrated CMOS/silicon Photonic Optical Receiver with −15dBm Sensitivity and 0.17pJ/bit Energy Efficiency” 2015 IEEE Optical Interconnects Conference (OI) (30 Apr. 2015): <http://ieeexplore.ieee.org/document/7115663/?tp=&arnumber=7115663>

“Sales of 100GbE Optical Transceivers Exceeded $1.1Billion in 2016.” LightCounting, 23 Feb. 2017. Web. <http://www.lightcounting.com/News_022317.cfm>.

Sapienza, Luca, et al. “Nanoscale Optical Positioning of Single Quantum Dots for Bright and Pure Single-Photon Emission” arXiv1503.07141 (5 Aug. 2015): <https://arxiv.org/abs/1503.07141v2>.

Sarmiento-Merenguel, J. D., et al. “Demonstration of Integrated Polarization Control with a 40 DB Range in Extinction Ratio” Optica2.12 (20 Dec. 2015): 1019–1023. <https://www.osapublishing.org/optica/abstract.cfm?uri=optica-2-12-1019>.

Sarmiento-Merenguel, Jose-Dario, et al. “Silicon-on-Insulator Integrated Tunable Polarization Controller (conference Presentation)” Silicon Photonics and Photonic Integrated Circuits V (13 May 2016): 1–989108. <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=2541467>.

Sarti, Francesco, et al. “Coupling of Semiconductor Carbon Nanotubes Emission with Silicon Photonic Micro Ring Resonators” Silicon Photonics and Photonic Integrated Circuits V (13 May 2016): 8–98910. <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=2523708>.

Schall, Daniel, et al. “50 GBit/s Photodetectors Based on Wafer-Scale Graphene for Integrated Silicon Photonic Communication Systems” ACS Photonics 1.9 (17 Sept. 2014): 781–784. <http://pubs.acs.org/doi/abs/10.1021/ph5001605>.

Schall, Daniel, et al. “Infrared Transparent Graphene Heater for Silicon Photonic Integrated Circuits” Optics Express 24.8 (18 Apr. 2016): 7871–7878. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-8-7871>.

Scheerlinck, Stijn, et al. “Efficient, Broadband and Compact Metal Grating Couplers for Silicon-on-Insulator Waveguides” Optics Express 15.15 (23 July 2007): 9625–9630. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-15-15-9625>.

Schmitt, Sebastian W, George Sarau, and Silke H Christiansen. “Title: Observation of Strongly Enhanced Photoluminescence from Inverted Cone-Shaped Silicon Nanostuctures” arXiv (24 June 2015): <https://arxiv.org/abs/1506.07419>.

Schmitt, Sebastian W., George Sarau, and Silke Christiansen. “Observation of Strongly Enhanced Photoluminescence from Inverted Cone-Shaped Silicon Nanostuctures” Scientific Reports 5. (26 Nov. 2015): 17089. <http://www.nature.com/articles/srep17089>.

Scott, Allyson. “Mellanox Technologies and Oclaro Team up to Connect 100Gb/s PSM4 Silicon Photonics to Next Generation 25Gb/s LR Transceivers for Servers and Storage” Mellanox. Business Wire, 18 Sept. 2016. Web. <http://www.businesswire.com/news/home/20160917005005/en/Mellanox-Technologies-Oclaro-Team-Connect-100Gbs-PSM4>.

Scott, Jodi. "Data Center Standard Published by ASHRAE" 13 Sept. 2016. Web. <https://www.ashrae.org/news/2016/data-center-standard-published-by-ashrae>.

Seeds, Alwyn J, et al. "Quantum Dot Lasers on Silicon by Direct Epitaxial Growth" Frontiers in Optics 2015 (18 Oct. 2015): 3–4. <https://www.osapublishing.org/abstract.cfm?uri=FiO-2015-FTh4B.3>.

Semiconductor Industry Association (SIA). "The International Technology Roadmap for Semiconductors 2.0, 2015 Edition Executive Report"Washington, D.C.: Semiconductor Industry Association, 15 Dec. 2015. Web. <http://www.semiconductors.org/clientuploads/Research_Technology/ITRS/2015/0_2015%20ITRS%202.0%20Executive%20Report%20(1).pdf>.

Seok, Tae Joon, et al. "Large-Scale Broadband Digital Silicon Photonic Switches with Vertical Adiabatic Couplers" Optica 3.1 (13 Jan. 2016): 64. <https://www.osapublishing.org/optica/abstract.cfm?URI=optica-3-1-64>.

Shankland, Stephen. "IBM Chips: Let There Be Light Signals" cnet 1 Dec. 2010: n.pag. Web. <https://www.cnet.com/news/ibm-chips-let-there-be-light-signals/>.

Shao, Zengkai, et al. "Ultra-Low Temperature Silicon Nitride Photonic Integration Platform" Optics Express 24.3 (25 Jan. 2016): 1865. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-3-1865>.

Shcherbakov, Maxim R., et al. "Ultrafast All-Optical Switching with Magnetic Resonances in Nonlinear Dielectric Nanostructures" Nano Letters 15.10 (22 Sept. 2015): 6985–6990. <http://pubs.acs.org/doi/abs/10.1021/acs.nanolett.5b02989>.

Shehabi, Arman, et al. "United States Data Center Energy Usage Report" Ernest Orlando Lawrence Berkeley Natinoal Laborator, 30 June 2016. Web. <https://eta.lbl.gov/sites/all/files/publications/lbnl-1005775_v2.pdf>.

Shi, Kaifeng, and Zhaolin Lu. "Ultracompact Field Effect Electro-Absorption Plasmonic Modulator" arXiv 1509.08828. (22 Oct. 2015): <http://arxiv.org/ftp/arxiv/papers/1509/1509.08828.pdf>.

Shiraki, Tomohiro, et al. "Emergence of New Red-Shifted Carbon Nanotube Photoluminescence Based on Proximal Doped-Site Design" Scientific Reports 6. (18 Apr. 2016): 28393. <http://www.nature.com/articles/srep28393>.

Shiue, Ren-Jye, et al. "High-Responsivity Graphene-Boron Nitride Photodetector and Autocorrelator in a Silicon Photonic Integrated Circuit" arXiv (2 July 2015): <https://arxiv.org/abs/1507.00426>.

Shopov, Stefan, and Sorin P. Voinigescu. "A 3x60 Gb/s Transmitter/repeater Front-End with 4.3 Vpp Single-Ended Output Swing in a 28nm UTBB FD-SOI Technology" IEEE Journal of Solid-State Circuits 51.7 (July 2016): 1651–1662. 25 July 2016. <http://ieeexplore.ieee.org/document/7469814/?tp=&arnumber=7469814>

Shubin, I., et al. "Hybrid III-V/SOI Optoelectronic Laser Module" 2016 IEEE 66th Electronic Components and Technology Conference (ECTC) (10 June 2016): <http://ieeexplore.ieee.org/document/7545557/?tp=&arnumber=7545557>

Shukla, Vishnu, and David R. Stauffer. "Technology Options for 400G Implementation" OIF-Optical Internetworking Forum, 31 July 2015. Web. <http://www.oiforum.com/wp-content/uploads/OIF-Tech-Options-400G-01.0.pdf>.

Siampour, Hamidreza, and Yaping Dan. "Si Nanowire Phototransistors at Telecommunication Wavelengths by Plasmon-Enhanced Two-Photon Absorption" Optics Express 24.5 (7 Mar. 2016): 4601–4609. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-5-4601>.

Simard, A. D., et al. "Segmented Silicon MZM for PAM-8 Transmissions at 114 Gb/s with Binary Signaling" Opt. Express 24.17 (2016): 19467. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-17-19467>.

Singh, Arjun, et al. "Jupiter Rising" Proceedings of the 2015 ACM Conference on Special Interest Group on Data Communication - SIGCOMM '15 (21 Aug. 2015): <http://conferences.sigcomm.org/sigcomm/2015/pdf/papers/p183.pdf>.

Sisodia, Namita. "Theoretical Aspects of Photonic Band Gap in 1D Nano Structure of LN: MgLN Periodic Layer" AIP Conference Proceedings 1665.1 (24 June 2015): 50004. <http://scitation.aip.org/content/aip/proceeding/aipcp/10.1063/1.4917645>.

Skydsgaard, Nikolaj. "Facebook to Build Third Foreign Data Center in Denmark" Niall McEntegart. Reuters, 19 Jan. 2017. Web. <http://www.reuters.com/article/us-facebook-denmark-idUSKBN15310F>.

Smit, M., J. van der Tol, and M. Hill. "Moore's Law in Photonics" Laser & Photonics Reviews 6.1 (20 Sept. 2011): 1–13. <http://onlinelibrary.wiley.com/doi/10.1002/lpor.201100001/abstract>.

Smith, Brad. "Mellanox Launches 200Gb/s HDR InfiniBand AOC and DAC LinkX® Cables" Melanox. Mellanox, 29 Nov. 2016. Web. <https://www.mellanox.com/blog/2016/11/mellanox-launches-200gbs-hdr-infiniband-aoc-and-dac-linkx-cables/>.

Smith, Brad. "100G data center Interconnects" Lightcounting, ethernet alliance, 12 Mar. 2012. Web. <http://www.ethernetalliance.org/wp-content/uploads/2011/12/Brad-Smith_OFC2012_EA_Panel1.pdf>.

Smith, Thomas B, et al. "Fundamentals of silicon Photonic devices" Monterey Park, CA: Mellanox (Kotura), 4 Oct. 2006. Web. <https://www.mellanox.com/related-docs/whitepapers/KOTURA_Fundamentals_of_Silicon_Photonic_Devices.pdf>.

Smolaks, Max. "Huawei Launches Its First Rack Scale Design Servers" Qui Long. DatacenterDynamics, 7 Sept. 2016. Web. <http://www.datacenterdynamics.com/content-tracks/servers-storage/huawei-launches-its-first-rack-scale-design-servers/96900.fullarticle>.

Smolaks, Max. "Rack Scale Architecture – These Are Not the Droids You'Ve Been Looking for" DatacenterDynamics.com. DatacenterDynamics, Mar. 2015. Web. <http://www.datacenterdynamics.com/it-networks/rack-scale-architecture-these-are-not-the-droids-youve-been-looking-for/93524.fullarticle>.

Snell, Addison. "The Hyperscale Effect: Tracking the Newest High-Growth IT Segment" Intersect360 Research. The Next Platform, 26 May 2016. Web. <http://www.nextplatform.com/2016/05/26/hyperscale-effect-tracking-newest-high-growth-segment-computing/>.

Snyder, Bradley, and Peter O'Brien. "Planar Fiber Packaging Method for Silicon Photonic Integrated Circuits" Optical Fiber Communication Conference and Exposition (OFC/NFOEC), 2012 (4 Mar. 2008): 1–3. <http://ieeexplore.ieee.org/document/6476397/?tp=&arnumber=6476397>

Sodagar, Majid, et al. "Compact, 15 Gb/s Electro-Optic Modulator Through Carrier Accumulation in a Hybrid Si/SiO2/Si Microdisk" Optics Express 23.22 (2 Nov. 2015): 28306–28315. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-22-28306>.

Solomon, Howard. "Infinera to Release 2U-Sized Optical Transport Platform" Infinera. IT World Canada, 7 Oct. 2014. Web. <http://www.itworldcanada.com/article/infinera-to-release-2u-sized-optical-transport-platform/98015>.

Song, Bowen, et al. "3D Integrated Hybrid Silicon Laser" Optics Express 24.10 (16 May 2016): 10435–10444. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-10-10435>.

Song, Bowen, et al. "3D Integrated Silicon Photonic External Cavity Laser" Lasers and Electro-Optics (CLEO), 2016 Conference on 2016. (10 June 2016): n.pag. <http://ieeexplore.ieee.org/document/7788761/?tp=&arnumber=7788761>

Song, Shijie, et al. "Optical Single-Sideband Modulation Based on Silicon-on-Insulator Coupled-Resonator Optical Waveguides" Optical Engineering 55.3 (1 Mar. 2016): 31114. <http://opticalengineering.spiedigitallibrary.org/article.aspx?articleid=2466043>.

Sorace-Agaskar, Cheryl M., et al. "Integrated Mode-Locked Lasers in a CMOS-Compatible Silicon Photonic Platform" CLEO: 2015(10 May 2015): <https://www.osapublishing.org/abstract.cfm?uri=cleo_si-2015-SM2I.5>.

Sperling, Ed. "Focus Shifting To Photonics" Semiconductor Engineering 17 Aug. 2016: n.pag. Web. <http://semiengineering.com/focus-shifting-to-photonics/>.

SPIETV. "Philippe Absil: Partnering for Silicon Photonics Prototyping" YouTube. YouTube, 9 Aug. 2016. Web. <https://www.youtube.com/watch?v=cq6ss3EQ4FU>.

Spott, Alexander, et al. "Quantum Cascade Laser on Silicon" Optica 3.5 (20 May 2016): 545. <https://www.osapublishing.org/optica/abstract.cfm?uri=optica-3-5-545>.

Srinivasan, S. A., et al. "56 Gb/s Germanium Waveguide Electro-Absorption Modulator" Journal of Lightwave Technology 34.2 (15 Jan. 2015): 419–424. <http://ieeexplore.ieee.org/document/7264980/?tp=&arnumber=7264980>

Srinivasan, S., et al. "Coupled-Ring-Resonator-Mirror-Based Heterogeneous III–V Silicon Tunable Laser" IEEE Photonics Journal 7.1 (26 May 2016): <http://ieeexplore.ieee.org/document/7111228/?tp=&arnumber=7111228>

Stettner, T, et al. "Coaxial GaAs-AlGaAs Core-Multishell Nanowire Lasers with Epitaxial Gain Control" Applied Physics Letters 108.1 (5 Jan. 2016): 11108. <http://scitation.aip.org/content/aip/journal/apl/108/1/10.1063/1.4939549>.

Stojsavljevic, George (LightCounting), and Vladimir Kozolov (LightCounting). "Impact of Silicon Photonics Technology on the Global Market for Optical Communication Products" 6 Oct. 2016. Private Communication.

Sukhdeo, David S, et al. "Title: Anomalous Threshold Reduction from <100> Uniaxial Strain for a Low-Threshold Ge Laser" arXiv (28 June 2015): <https://arxiv.org/abs/1506.08403>.

Sukhdeo, David S., et al. "Ge Microdisk with Lithographically-Tunable Strain Using CMOS-Compatible Process" Optics Express Vol. 23, Issue 26, pp. 33249-33254.26 (25 Oct. 2015): 33249–33254. <http://arxiv.org/abs/1510.07236>.

Sumita, Ms. "Global Silicon Photonics Product Market Worth US$1.95 Billion by 2014" MarketsandMarkets. online PR media, 16 Mar. 2010. Web. <https://www.onlineprnews.com/news/25920-1268721366-global-silicon-photonics-product-market-worth-us195-billion-by-2014.html>.

Sun, Chen, et al. "A 45 Nm CMOS-SOI Monolithic Photonics Platform with Bit-Statistics-Based Resonant Microring Thermal Tuning" IEEE Journal of Solid-State Circuits 51.4 (4 Apr. 2016): 893–907. <http://ieeexplore.ieee.org/document/7426337/?tp=&arnumber=7426337>

Sun, Chen, et al. "Single-Chip Microprocessor That Communicates Directly Using Light" Nature 528.7583 (23 Dec. 2015): 534–538. <http://www.nature.com/nature/journal/v528/n7583/full/nature16454.html>.

Sun, Tianbo, et al. "Surface-Normal Electro-Optic Spatial Light Modulator Using Graphene Integrated on a High-Contrast Grating Resonator" Optics Express 24.23 (14 Nov. 2016): 26035–26043. <http://dx.doi.org/10.1364/OE.24.026035>.

Sun, X., et al. "Polarization Rotator Based on Augmented Low-Index-Guiding Waveguide on Silicon Nitride/silicon-on-Insulator Platform" Optics Letters 41.14 (15 July 2016): 3229–3232. 27 July 2016. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-41-14-3229>.

Sun, Yu. "RapidIO Technology Applied in Multifunction Phased Array Radar (MPAR)" University of Oklahoma, 30 Dec. 2007. Web. <https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=1&cad=rja&uact=8&ved=0ahUKEwiTytagkLjRAhUqjVQKHdtACXsQFggiMAA&url=http%3A%2F%2Farrc.ou.edu%2F~rockee%2FRIO%2FRapidIO%2520technology2.ppt&usg=AFQjCNHk1WrQMNLDdYGfpbRyfuJOpiwECw&sig2=uFOCh_xNYYtpojNOa5rFlQ>.

Suzuki, Takanori, et al. "1.3-μm DFB Laser μ-Platform; Light Source Suitable for Silicon Photonics Platform - IEEE Xplore Document" OptoElectronics and Communications Conference (OECC) held jointly with 2016 International Conference on Photonics in Switching (PS) 21.2016 (7 July 2016): n.pag. <http://ieeexplore.ieee.org/document/7718552/?tp=&arnumber=7718552>

Takeda, Koji, et al. "Heterogeneously Integrated Photonic-Crystal Lasers on Silicon for On/off Chip Optical Interconnects" Optics Express 23.2 (13 Jan. 2015): 702. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-2-702>.

Takei, Ryohei, et al. "Ultra-Low-Loss Silicon Based Spot-Size Converter Fabricated by CMOS Compatible Process" The 9th International Conference on Group IV Photonics (GFP) (31 Aug. 2012): <http://ieeexplore.ieee.org/document/6324078/?tp=&arnumber=6324078>

Takiguchi, Masato, et al. "10-Gb/s Operation of a Telecom-Band InAsP/InP Sub-Wavelength Nanowire Laser on Silicon Photonic Crystal" Conference on Lasers and Electro-Optics 2016. (5 June 2016): 1–2. <https://www.osapublishing.org/abstract.cfm?URI=cleo_si-2016-SF1E.2>.

Tan, Dawn T H, et al. "Ultra-Silicon-Rich Nitride Devices for CMOS Nonlinear Electronics" Dawn T. H. Tan, et al. SPIE, 12 Apr. 2016. Web. <http://spie.org/newsroom/6326-ultra-silicon-rich-nitride-devices-for-cmos-nonlinear-optics>.

Tan, Kang, et al. "Compact Highly-Efficient Polarization Splitter and Rotator Based on 90° Bends" Opt. Express 24.13 (17 June 2016): 14506. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-13-14506>.

Tan, Qing. "The on-Going Revolution of Datacenter and Intel Silicon Photonics" Intel, 15 May 2014. Web. <http://m.huawei.com/ilink/cnenterprise/download/HW_343606>.

Tanaka, S, et al. "High-Output-Power, Single-Wavelength Silicon Hybrid Laser Using Precise Flip-Chip Bonding Technology" Optics express. 20.27 (25 Dec. 2012): 28057–69. <https://www.ncbi.nlm.nih.gov/pubmed/23263042>.

Tanaka, Shinsuke, et al. "High-Output-Power, Single-Wavelength Silicon Hybrid Laser Using Precise Flip-Chip Bonding Technology" Optics Express 20.27 (4 Dec. 2012): 28057. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-20-27-28057>.

Tang, Mingchu, et al. "1.3-μm InAs/GaAs Quantum-Dot Lasers Monolithically Grown on Si Substrates Using InAlAs/GaAs Dislocation Filter Layers" Optics Express 22.10 (19 May 2014): 11528–11535. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-22-10-11528>.

Tao, Li, et al. "4-λ InGaAsP-Si Distributed Feedback Evanescent Lasers with Varying Silicon Waveguide Width" Optics Express 22.5 (10 Mar. 2014): 5448–5454. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-22-5-5448>.

Tech Events. "Intel Developer Forum 2016 Day 2 Keynote Hightlight" YouTube. YouTube, 17 Aug. 2016. Web. <https://www.youtube.com/watch?v=ebV6TykqgAM>.

Thomson, David, et al. "Roadmap on Silicon Photonics" Journal of Optics 18.7 (24 June 2016): 073003. <https://iopscience.iop.org/article/10.1088/2040-8978/18/7/073003>.

Tian, Zhaobing, et al. "Single Rolled-up InGaAs/GaAs Quantum Dot Microtubes Integrated with Silicon-on-Insulator Waveguides" Optics Express 19.13 (20 June 2011): 12164–12171. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-19-13-12164>.

Timo, Aalto. "VTT and PhoeniX Software Announce a Process Design Kit to Support Silicon Photonics Developers Around the World" VTT. VTT, 22 Aug. 2016. Web. <http://www.vttresearch.com/media/news/vtt-and-phoenix-software>.

Toesland, Finbarr. "Global Silicon Photonics Market Leader Intel Pushes Back Vital Component Module" Yahoo! Finance UK & Ireland. Yahoo Finance UK, 23 Feb. 2015. Web. <https://uk.finance.yahoo.com/news/global-silicon-photonics-market-leader-000000396.html>.

Townes, Charles H. "The First Laser" press.uchicago.edu. The University of Chicago Press, 18 Jan. 2004. Web. <http://www.press.uchicago.edu/Misc/Chicago/284158_townes.html>.

Trader, Tiffany. "Mellanox Readies First 200 Gb/s Silicon Photonics Devices" Mellanox. HPCwire, 22 Mar. 2016. Web. <https://www.hpcwire.com/2016/03/22/mellanox-reveals-200-gbps-path/>.

Triviño, Vico N, et al. "Integrated Photonics on Silicon with Wide Bandgap GaN Semiconductor" Applied Physics Letters 102.8 (1 Mar. 2013): 81120. <http://scitation.aip.org/content/aip/journal/apl/102/8/10.1063/1.4793759>.

Tu, Zhijuan, et al. "Ultracompact 100 Gbps Coherent Receiver Monolithically Integrated on Silicon" Japanese Journal of Applied Physics 55.4S (11 Mar. 2016): 04EC04. <http://iopscience.iop.org/article/10.7567/JJAP.55.04EC04/meta>.

Turvik, John Tarje. "Double Heterojnction Light Emitting Diodes and Laser Diodes Having Quantum Dot Silicon Light Emitters" United States Patent: Astralux, Inc., 14 Oct. 2003. Web. <http://pdfpiw.uspto.gov/.piw?PageNum=0&docid=06632694>.

U.S. Environmental Protection Agency. "Report to congress on server and data center energy efficiency public law 109-431"Washington, D.C.: U.S. EPA, 2007. Web. <https://www.energystar.gov/ia/partners/prod_development/downloads/EPA_Datacenter_Report_Congress_Final1.pdf>.

Undisclosed Industry Expert. "Silicon Photonics Price Target $1/Gb/s" 14 Dec. 2015. . (email conversation).

Ungerer, Theo, Paul Carpenter, and Mike Knebel. "D2.1 Preliminary EuroLab-4-HPC Roadmap" www.eurolab4phc.eu: EuroLab-4-HPC, 2016. Web. <https://www.eurolab4hpc.eu/roadmap/>.

University of British Columbia. "Si-EPIC Workshops" siepic.ubc.ca. 7 July 2015. Web. <http://siepic.ubc.ca/workshops>.

Urino, Yutaka, et al. "First Demonstration of Athermal Silicon Optical Interposers with Quantum Dot Lasers Operating up to 125 °C" Journal of Lightwave Technology 33.6 (15 Mar. 2015): 1223–1229. <http://ieeexplore.ieee.org/document/6994774/?tp=&arnumber=6994774>

Usui, Mitsuo, et al. "Opto-Electronic Hybrid Integrated Chip Packaging Technology for Silicon Photonic Platform Using Gold-Stud Bump Bonding" 2015 International Conference on Electronic Packaging and iMAPS All Asia Conference (ICEP-IAAC) (Apr. 2015): <http://ieeexplore.ieee.org/document/7111096/?tp=&arnumber=7111096>

van Thourhout, Dries, et al. "III-V-on-Silicon Photonic Devices for Optical Communication and Sensing" Photonics 2.3 (18 Sept. 2015): 1004–969. <http://www.mdpi.com/2304-6732/2/3/969>.

Vázquez, Carmen, et al. "Tolerance Analysis for Efficient MMI Devices in Silicon Photonics" Silicon Photonics IX 8990.February 1, 2014 (8 Mar. 2014): 7–89900. <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=1846444>.

Vázquez-Córdova, Sergio A, et al. "Erbium-Doped Spiral Amplifiers with 20 DB of Net Gain on Silicon" Optics Express 22.21 (20 Oct. 2014): 25993–26004. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-22-21-25993>.

Verslegers, Lieven B, et al. "Design of Low-Loss Polarization Splitting Grating Couplers" OSA Technical Digest (online) (Optical Society of America, 2014), (13 July 2014): 2–4. <https://www.osapublishing.org/abstract.cfm?uri=networks-2014-JT4A.2>.

Vincent, James. "Mark Zuckerberg Shares Pictures from Facebook's Cold, Cold Data Center" Facebook. The Verge, 29 Sept. 2016. Web. <http://www.theverge.com/2016/9/29/13103982/facebook-arctic-data-center-sweden-photos>.

Vivien, L, et al. "Comparison Between Strip and Rib SOI Microwaveguides for Intra-Chip Light Distribution" (2004): 6 Apr. 2016. <http://perso.telecom-paristech.fr/~grillot/sdarticle.pdf>.

Vivien, L., et al. "Comparison Between Strip and Rib SOI Microwaveguides for Intra-Chip Light Distribution" Optical Materials 27.5 (Feb. 2005): 756–762. <http://www.sciencedirect.com/science/article/pii/S092534670400223X>.

Vlasov, Yurii A., and Sharee J. McNab. "Losses in Single-Mode Silicon-on-Insulator Strip Waveguides and Bends" Optics Express12.8 (2004): 1622. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-12-8-1622>.

Voss, David. "Silicon Lasers" Lionel Kimerling. MIT Technology Review, 1 June 2001. Web. <https://www.technologyreview.com/s/401061/silicon-lasers/>.

Walace, John. "New 700-Nm-Emitting MoS2 LED Could Be Interesting for Silicon Photonics" Ecole Polytechnique Federale de Lausanne. Laser Focus World, 25 Apr. 2014. Web. <http://www.laserfocusworld.com/articles/2014/04/new-700-nm-emitting-mos2-led-could-be-interesting-for-silicon-photonics.html>.

Wallace, John. "CREOL Researchers Create Integrated Optical Lithium-Niobate-on-Silicon Devices" Laser Focus World 15 Nov. 2013: Web. <http://www.laserfocusworld.com/articles/2013/11/creol-researchers-create-integrated-optical-lithium-niobate-on-silicon-devices.html>.

Wallace, John. "Ge/Si Near-IR CMOS-Compatible Photodetector Has 1 A/W Responsivity" LaserFocusWorld 7 Aug. 2013: Web. <http://www.laserfocusworld.com/articles/print/volume-49/issue-08/newsbreaks/ge-si-near-ir-cmos-compatible-photodetector-has-1-a-w-responsivity.html>.

Wallace, John. "Silicon Photonics: Standard Wire-Bonding Technique Doubles Waveguide Ge Detector Bandwidth" LaserFocusWorld 13 Nov. 2015: Web. <http://www.laserfocusworld.com/articles/print/volume-51/issue-11/world-news/silicon-photonics-standard-wire-bonding-technique-doubles-waveguide-ge-detector-bandwidth.html>.

Wan, Yating, et al. "Sub-Wavelength InAs Quantum Dot Micro-Disk Lasers Epitaxially Grown on Exact Si (001) Substrates" Applied Physics Letters 108.22 (31 May 2016): 221101. <http://scitation.aip.org/content/aip/journal/apl/108/22/10.1063/1.4952600>.

Wang, J., et al. "Integration of Tensile-Strained Ge P-i-N Photodetector on Advanced CMOS Platform" 2007 4th IEEE International Conference on Group IV Photonics (21 Sept. 2007): <http://ieeexplore.ieee.org/document/4347664/?tp=&arnumber=4347664>

Wang, Junjia, and Lawrence R. Chen. "Low Crosstalk Bragg Grating/Mach-Zehnder Interferometer Optical Add-Drop Multiplexer in Silicon Photonics" Optics Express 23.20 (5 Oct. 2015): 26450–26459. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-20-26450>.

Wang, Junjia, Ivan Glesk, and Lawrence R. Chen. "Subwavelength Grating Devices in Silicon Photonics" Science BulLetin 61.11 (29 Apr. 2016): 879–888. <https://link.springer.com/article/10.1007/s11434-016-1077-z>.

Wang, Ting, et al. "1.3-μm InAs/GaAs Quantum-Dot Lasers Monolithically Grown on Si Substrates" Optics Express 19.12 (26 May 2011): 11381–11386. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-19-12-11381>.

Wang, Ting, et al. "13-μm InAs/GaAs Quantum-Dot Lasers Monolithically Grown on Si Substrates" Optics Express 19.12 (26 May 2011): 11381. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-19-12-11381>.

Wang, Weiqiang, et al. "Dual-Pump Kerr Micro-Cavity Optical Frequency Comb with Varying FSR Spacing" Scientific Reports 6. (24 June 2016): 28501. 25 June 2016. <http://www.nature.com/articles/srep28501>.

Wang, Xiaomu, et al. "High-Responsivity Graphene/silicon-Heterostructure Waveguide Photodetectors" Nature Photonics 7.11 (15 Sept. 2013): 888–891. <http://www.nature.com/nphoton/journal/v7/n11/full/nphoton.2013.241.html>.

Wang, Xiaoxi, et al. "Wide-Range and Fast Thermally-Tunable Silicon Photonic Microring Resonators Using the Junction Field Effect" Optics Express 24.20 (3 Oct. 2016): 23081–23093. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-20-23081>.

Wang, Yating, et al. "Optically Pumped 1.3 μm Room-Temperature InAs Quantum-Dot Micro-Disk Lasers Directly Grown on (001) Silicon" Optics Letters 41.7 (1 Apr. 2016): 1664–1667. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-41-7-1664>.

Wang, Zhechao, et al. "Room-Temperature InP Distributed Feedback Laser Array Directly Grown on Silicon" Nature Photonics 9.12 (26 Oct. 2015): 837–842. <http://www.nature.com/nphoton/journal/v9/n12/pdf/nphoton.2015.199.pdf>.

Wang, Zhongli, et al. "Experimental Demonstration of Graphene Plasmons Working Close to the Near-Infrared Window" Optics Letters 41.22 (15 Nov. 2016): 5345–5348. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-41-22-5345>.

Wang, Zihao, et al. "High Performance InAs Quantum Dot Lasers on Silicon Substrates by Low Temperature Pd-GaAs Wafer Bonding" Appl. Phys. Lett. 107.26 (29 Dec. 2015): 261107. <https://www.rit.edu/~w-nanoph/photon/wp-content/uploads/2015/12/High-performance-InAs-quantum-dot-lasers-on-silicon-substrates-by-low-temperature-by-low-temperature-Pd-GaAs-wafer-bonding.pdf>.

Wang, Zihao, et al. "Room Temperature CW Operation of 1.3um Quantum Dot Lasers on a Si Substrate by Pd-Mediated Wafer Bonding" Integrated Photonics Research, Silicon and Nanophotonics 2015 (27 June 2015): 4. <https://www.osapublishing.org/abstract.cfm?uri=IPRSN-2015-IM4B.4>.

Watanabe, Kei, et al. "Recent Progress in Optical Waveguide Technologies Enabling Integration of High-Density Compact Photonics" NTT Technical Review 2017.1 (18 Jan. 2017): n.pag. <https://www.ntt-review.jp/archive/ntttechnical.php?contents=ntr201701fa2.html>.

Weigel, Peter O, et al. "Title: Hybrid Lithium Niobate and Silicon Photonic Waveguides" arXiv (6 Oct. 2015): <https://arxiv.org/abs/1510.01777>.

Weigel, Peter O., et al. "Lightwave Circuits in Lithium Niobate Through Hybrid Waveguides with Silicon Photonics" Scientific Reports 6. (1 Mar. 2016): 22301. <http://www.nature.com/articles/srep22301>.

Weissberger, Alan. "2015 hot Interconnects summary part I – oracle, Intel, and Facebook talks" Viodi. The Viodi View, 3 Sept. 2015. Web. <http://viodi.com/2015/09/03/2015-hot-interconnects-summary-part-i-oracle-intel-and-facebook-talks/>.

Weissberger, Alan. "Silicon Photonics – Cisco and Intel See "Light at the end of the Tunnel"" Joel Goergen. The Viodi View, 8 Nov. 2013. Web. <http://viodi.com/2013/11/08/silicon-photonics-cisco-intel-see-light-at-the-end-of-the-tunnel/>.

Wen, Ke, et al. "Silicon Photonics in Post Moore's Law Era: Technological and Architectural Implications" PMES 2016 : Post-Moore's Era Supercomputing (PMES) Workshop (14 Nov. 2016): n.pag. <http://lightwave.ee.columbia.edu/Publications/Wen2016_PMES.pdf>.

Wen, Xiang, Ke Xu, and Qinghai Song. "Design of a Barcode-Like Waveguide Nanostructure for Efficient Chip–fiber Coupling" Photonics Research 4.6 (5 Oct. 2016): 209. <https://www.osapublishing.org/prj/abstract.cfm?uri=prj-4-6-209>.

Wheeler, Michael D. "For Integrated Photonics, a Tale of Two Materials" Photonics Spectra 31 Aug. 2016: Web. <http://www.photonics.com/Article.aspx?AID=60862>.

Williams, K. A., et al. "InP Photonic Circuits Using Generic Integration [Invited]" Photon. Res. 3.5 (2015): B60. <https://www.osapublishing.org/prj/abstract.cfm?uri=prj-3-5-b60>.

Wirths, S., et al. "Direct Bandgap GeSn Microdisk Lasers at 2.5 μm for Monolithic Integration on Si-Platform" Electron Devices Meeting (IEDM) (7 Dec. 2015): 1–6. <http://ieeexplore.ieee.org/document/7409615/?tp=&arnumber=7409615>

Wirths, S., et al. "Lasing in Direct-Bandgap GeSn Alloy Grown on Si" Nature Photonics 9.2 (19 Jan. 2015): 88–92. <http://www.nature.com/nphoton/journal/v9/n2/full/nphoton.2014.321.html>.

Wirths, S., et al. "Strain Engineering for Direct Bandgap GeSn Alloys" Group IV Photonics (GFP), 2014 IEEE 11th International Conference on (29 Aug. 2014): 13–14. <http://ieeexplore.ieee.org/document/6962004/?tp=&arnumber=6962004>

Witmer, Jeremy D., Jeff T. Hill, and Amir H. Safavi-Naeini. "Design of Nanobeam Photonic Crystal Resonators for a Silicon-on-Lithium-Niobate Platform" Optics Express 24.6 (8 Mar. 2016): 5876. <https://www.osapublishing.org/oe/fulltext.cfm?uri=oe-24-6-5876&id=337065>.

Wolfe, Josh. "Why IBM and Intel Are Chasing the $100B Opportunity in Nanophotonics" Peter De Dobbelaere. Forbes, 13 Dec. 2012. Web. <http://www.forbes.com/sites/joshwolfe/2012/12/13/why-ibm-and-intel-are-chasing-the-100b-opportunity-in-nanophotonics/#336543e43812>.

Wu, Danning, et al. "Reconfigurable Optical Add-Drop Multiplexer Based on Thermally Tunable Micro-Ring Resonators" Optics Communications 367. (1 May 2016): 44–49. <http://www.sciencedirect.com/science/article/pii/S0030401816300189>.

Xia, Fengnian, et al. "Ultra-Compact Wavelength Division Multiplexing Devices Using Silicon Photonic Wires for on-Chip Interconnects" OSA Technical Digest Series (CD) (Optical Society of America, 2007), (25 Mar. 2007): 2. <https://www.osapublishing.org/abstract.cfm?uri=OFC-2007-OWG2>.

Xiao, Jinbao, Xu Liu, and Xiaohan Sun. "Design of an Ultracompact MMI Wavelength Demultiplexer in Slot Waveguide Structures" Optics Express 15.13 (25 June 2007): 8300–8308. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-15-13-8300>.

Xiao, Zhe, et al. "Ultra-Compact Low Loss Polarization Insensitive Silicon Waveguide Splitter" Optics Express 21.14 (2 July 2013): 16331. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-21-14-16331>.

Xie, Weiqiang, et al. "Fabrication and Characterization of on-Chip Silicon Nitride Microdisk Integrated with Colloidal Quantum Dots" Optics Express 24.2 (Dec. 2015): 114–122. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-2-A114>.

Xinhong, Jiang, et al. "Compact Silicon Photonic Interleaver Using Loop-Mirror-Based Michelson-Gires-Tournois Interferometer" OSA Technical Digest (online) (Optical Society of America, 2016) (20 Mar. 2016): 2–5. <https://www.osapublishing.org/abstract.cfm?uri=OFC-2016-Tu2F.5>.

Xiong, Chi, et al. "Monolithic 56 Gb/s Silicon Photonic Pulse-Amplitude Modulation Transmitter" Optica 3.10 (21 Sept. 2016): 1060–1065. <https://www.osapublishing.org/optica/abstract.cfm?uri=optica-3-10-1060>.

Xiong, Chi, et al. "Title: Integrated GaN Photonic Circuits on Silicon (100) for Second Harmonic Generation" arXiv (20 Jan. 2014): <https://arxiv.org/abs/1401.4798>.

Xiong, Y., et al. "High Extinction Ratio and Broadband Silicon TE-Pass Polarizer Using Subwavelength Grating Index Engineering" IEEE Photonics Journal 7.5 (Oct. 2015): 1–7. <http://ieeexplore.ieee.org/document/7286730/?tp=&arnumber=7286730>

Xu, Dan-Xia, et al. "Selecting the Polarization in Silicon Photonic Wire Components" Proc. SPIE 8266 (9 Feb. 2012): 82660–9. <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=1344975>.

Xu, Dan-Xia, et al. "Silicon Photonic Waveguide Biosensor Configurations" United States Patent Application: 1 July 2010. Web. <http://pdfaiw.uspto.gov/.aiw?Docid=20100165351>.

Xu, Hao, et al. "High Speed Silicon Mach-Zehnder Modulator Based on Interleaved PN Junctions" Optics Express 20.14 (2 July 2012): 15093–15099. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-20-14-15093&origin=search>.

Xu, Yin, and Jinbiao Xiao. "Design and Numerical Study of a Compact, Broadband and Low-Loss TE-Pass Polarizer Using Transparent Conducting Oxides" Optics Express 24.14 (11 July 2016): 15373–15382. 25 July 2016. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-14-15373>.

Xu, Yin, Jinbiao Xiao, and Xiaohan Sun. "A Compact Hybrid Plasmonic Polarization Rotator for Silicon-Based Slot Waveguides" IEEE Photonics Technology Letters 26.16 (15 Aug. 2015): 1609–1612. 27 July 2016. <http://ieeexplore.ieee.org/document/6827189/?tp=&arnumber=6827189>

Xu, Yin, Jinbiao Xiao, and Xiaohan Sun. "A Compact Polarization Converter for Silicon-Based Slot Waveguides Using a Hybrid Plasmonic Effect" Journal of Optics (Online) 16.8 (4 Aug. 2014): <http://iopscience.iop.org/article/10.1088/2040-8978/16/8/085502/meta>.

Xue, Xiaoxiao, et al. "Thermal Tuning of Kerr Frequency Combs in Silicon Nitride Microring Resonators" Optics Express 24.1 (11 Jan. 2016): 687–698. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-1-687>.

Yamada, Koji, et al. "Silicon-Germanium-Silica Monolithic Photonic Integration Platform for Telecommunications Device Applications" NTT Technical Review 12.5 (31 May 2014): <https://www.ntt-review.jp/archive/ntttechnical.php?contents=ntr201405ra1.pdf&mode=show_pdf>.

Yamada, Koji. "Silicon Photonics for a Post-Moore Era" Electronics and Photonics Research Institute. PIC Magazine, 23 Dec. 2016, 3 ed. Web. <http://www.publishing.ninja/V4/page/3069/175/168#>.

Yang, Biao, et al. "High-Efficiency Focusing Grating Coupler for Large-Scale Silicon Photonic Integration" International Conference on Optoelectronics and Microelectronics (ICOM) 2013. (9 Sept. 2013): 160–162. <http://ieeexplore.ieee.org/document/6626516/?tp=&arnumber=6626516>

Yang, Longzhi, et al. "Proposal for a 2 X 2 Optical Switch Based on Graphene-Silicon-Waveguide Microring" IEEE Photonics Technology Letters 26.3 (1 Feb. 2014): <http://ieeexplore.ieee.org/document/6665001/?tp=&arnumber=6665001>

Yang, Xuebei, and Aydin Babakhani. "Optical Waveguides and Photodiodes in 0.18μm CMOS SOI with No Post-Processing" (17 Mar. 2013): 2–6. <https://www.osapublishing.org/abstract.cfm?uri=OFC-2013-OTu2C.6>.

Yarris, Lynn. "Exciting Breakthrough in 2D Lasers" News Release. Berkeley Lab News Center, 20 Oct. 2015. Newscenter.Lbl.Gov. <https://newscenter.lbl.gov/2015/10/20/exciting-breakthrough-in-2d-lasers/>.

Yashiki, Kenichiro, et al. "25-Gbps Error-Free Operation of Chip-Scale Si-Photonics Optical Transmitter over 70oC with Integrated Quantum Dot Laser" OSA Technical Digest (online) (Optical Society of America, 2016. (20 Mar. 2016): 1–7. <https://www.osapublishing.org/abstract.cfm?uri=OFC-2016-Th1F.7>.

YASHIKI, Kenichiro, et al. "25-Gbps/ch Error-Free Operation over 300-M MMF of Low-Power-Consumption Silicon-Photonics-Based Chip-Scale Optical I/O Cores" IEICE Transactions on Electronics E99.C.2 (1 Feb. 2016): 148–156. <http://search.ieice.org/bin/pdf_link.php?category=C&fname=e99-c_2_148&lang=&year=2016>.

Yashiki, Kenichiro, et al. "5 MW/Gbps Hybrid-Integrated Si-Photonics-Based Optical I/O Cores and Their 25-Gbps/ch Error-Free Operation with over 300-M MMF" Optical Fiber Communication Conference (22 Mar. 2015): <https://www.osapublishing.org/abstract.cfm?uri=OFC-2015-Th1G.1>.

Ye, Yu, et al. "Monolayer Excitonic Laser" Nature Photonics Letters (19 Oct. 2015): <http://xlab.me.berkeley.edu/pdf/10.1038_nphoton.2015.197.pdf>.

Yoo, S. Ben J., Binbin Guan, and Ryn P. Scott. "Heterogeneous 2D/3D Photonic Integrated Microsystems" Microsystems & Nanoengineering 2. (31 Dec. 2015): <http://www.nature.com/articles/micronano201630>.

Yoshida, T, et al. "Vertical Silicon Waveguide Coupler Bent by Ion Implantation" Optics express. 23.23 (25 Dec. 2015): 29449–56. <https://www.ncbi.nlm.nih.gov/pubmed/26698428>.

Yu, Jinzhong, et al. "Recent Progress of SOI-Based Photonic Devices" Optoelectronic Materials and Devices for Optical Communications (24 Nov. 2005): n.pag. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-41-24-5700>.

Yu, Jinzhong, et al. "Research Progresses of SOI Optical Waveguide Devices and Integrated Optical Switch Matrix" Science in China Series F 48.2 (20 Apr. 2005): 234. <https://link.springer.com/article/10.1360/04yf0311>.

Yu, Jinzhong. "Research Progresses of SOI Optical Waveguide Devices and Integrated Optical Switch Matrix" Science in China Series F 48.2 (20 Apr. 2005): 234. <https://link.springer.com/article/10.1360/04yf0311>.

Yu, Kunzhi, et al. "25Gb/s Hybrid-Integrated Silicon Photonic Receiver with Microring Wavelength Stabilization" Optical Fiber Communication Conference (22 Mar. 2015): <https://www.osapublishing.org/abstract.cfm?uri=ofc-2015-W3A.6>.

Yu, Longhai, et al. "Energy-Efficient Tunable Silicon Photonic Micro-Resonator with Graphene Transparent Nano-Heaters" arXiv (22 June 2015): <https://arxiv.org/abs/1506.06663>.

Yu, Longhai, et al. "Thermally Tunable Silicon Photonic Microdisk Resonator with Transparent Graphene Nanoheaters" Optica 3.2 (20 Feb. 2016): 159–166. <https://www.osapublishing.org/optica/abstract.cfm?uri=optica-3-2-159>.

Yu, Longhai, et al. "Title: Energy-Efficient Tunable Silicon Photonic Micro-Resonator with Graphene Transparent Nano-Heaters" arXiv (22 June 2015): <https://arxiv.org/abs/1506.06663>.

Yu, Mingbin, et al. "3D Electro-Optical Integration Based on High-Performance Si Photonics TSV Interposer" Proceedings Optical Fiber Communications Conference and Exhibition 2016. (24 Mar. 2016): <http://ieeexplore.ieee.org/document/7537454/?tp=&arnumber=7537454>

Yun, Han, et al. "Broadband 2 × 2 Adiabatic 3 DB Coupler Using Silicon-on-Insulator Sub-Wavelength Grating Waveguides" Optics Letters 41.13 (1 July 2016): 3041–3044. 9 July 2016. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-41-13-3041>.

Yushanov, Sergei, Jeffrey S Crompton, and Kyle C Koppenhoefer. "Plasmonic Waveguide Analysis" 9 Oct. 2015. Web. <https://www.comsol.com/paper/download/257551/crompton_paper.pdf>.

Zavracky, Paul M. "Method of Making Monolithic III-V Type Laser Devices and Silicon Devices on Silicon" United States Patent: Kopin Corp., 10 July 1990. Web. <http://pdfpiw.uspto.gov/.piw?PageNum=0&docid=04940672>.

Zeghuzi, A, et al. "25 Gbit/s Differential Phase-Shift-Keying Signal Generation Using Directly Modulated Quantum-Dot Semiconductor Optical Amplifiers" Applied Physics Letters 106.21 (26 May 2015): 213501. <http://scitation.aip.org/content/aip/journal/apl/106/21/10.1063/1.4921785>.

Zeman, Vlado. "Photonics--A Technological Revolution" Science Magazine 18 July 2003: n.pag. Web. <http://www.sciencemag.org/careers/2003/07/photonics-technological-revolution>.

Zeng, Cheng, et al. "Single Germanium Quantum Dot Embedded in Photonic Crystal Nanocavity for Light Emitter on Silicon Chip" Optics Express 23.17 (24 Aug. 2015): 22250–22261. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-23-17-22250>.

Zhang, Chong, et al. "8 × 8 × 40 Gbps Fully Integrated Silicon Photonic Network on Chip" Optica 3.7 (20 July 2016): 785–786. 22 July 2016. <https://www.osapublishing.org/optica/abstract.cfm?uri=optica-3-7-785>.

Zhang, Chong, et al. "Highly Linear Heterogeneous-Integrated Mach-Zehnder Interferometer Modulators on Si" Optics Express 24.17 (22 Aug. 2016): 19040–19047. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-17-19040>.

Zhang, Chong, et al. "High-Speed Hybrid Silicon Microring Lasers" 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS) (21 Apr. 2015): <http://www.hpl.hp.com/techreports/2015/HPL-2015-39.pdf>.

Zhang, Chong, et al. "Ultralinear Heterogeneously Integrated Ring-Assisted Mach–Zehnder Interferometer Modulator on Silicon" Optica 3.12 (8 Dec. 2016): 1483. <https://www.osapublishing.org/optica/abstract.cfm?uri=optica-3-12-1483>.

Zhang, H, et al. "Molybdenum Disulfide (moS2) as a Broadband Saturable Absorber for Ultra-Fast Photonics" Optics Express 22.6 (24 Mar. 2014): 7249–7260. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-22-6-7249>.

Zhang, Jing, et al. "Silicon Waveguide Based TE Mode Converter" Optics Express 18.24 (22 Nov. 2010): 25264–25270. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-18-24-25264>.

Zhang, Qiang, et al. "Single-Lane 180 Gbit/s PAM-4 Signal Transmission over 2 Km SSMF for Short-Reach Applications" Optics Letters 41.19 (20 Sept. 2016): 4449. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-41-19-4449>.

Zhang, Rui, et al. "Electronic Band-Gap Modified Passive Silicon Optical Modulator at Telecommunications Wavelengths" Scientific Reports 5. (13 Nov. 2015): 16588. <http://www.nature.com/articles/srep16588>.

Zhang, Yi, et al. "A Compact and Low Loss Y-Junction for Submicron Silicon Waveguide" Optics Express 21.1 (14 Jan. 2013): 1310–1316. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-21-1-1310>.

Zhang, Yong, et al. "Enhanced Light Emission from Ge Quantum Dots in Photonic Crystal Ring Resonator" Optics Express 22.10 (19 May 2014): 12248–12254. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-22-10-12248>.

Zhang, Yong, et al. "High-Extinction-Ratio Silicon Polarization Beam Splitter with Tolerance to Waveguide Width and Coupling Length Variations" Optics Express 24.6 (21 Mar. 2016): 6586–6593. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-6-6586>.

Zhang, Zanyun, et al. "Bidirectional Grating Coupler Based Optical Modulator for Low-Loss Integration and Low-Cost Fiber Packaging" Optics Express 21.12 (7 June 2013): 14202. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-21-12-14202&origin=search>.

Zheng, Ruiqi, Dingshan Gao, and Jianji Dong. "Ultra-Compact and Broadband Tunable Mid-Infrared Multimode Interference Splitter Based on Graphene Plasmonic Waveguide" arXiv (19 July 2015): n.pag. <https://arxiv.org/abs/1507.05238>.

Zheng, Xuezhe, et al. "A 33mW 100Gbps CMOS Silicon Photonic WDM Transmitter Using Off-Chip Laser Sources" OSA Technical Digest OFC 2013. (17 Mar. 2013): 5–9. <https://www.osapublishing.org/abstract.cfm?uri=nfoec-2013-PDP5C.9>.

Zheng, Xuezhe, et al. "III-V/Si Hybrid Laser Arrays Using Back End of the Line (BEOL) Integration" (19 July 2016): <http://ieeexplore.ieee.org/document/7516614/?tp=&arnumber=7516614>

Zhong, QAiuhang, et al. "Thermally Controlled Coupling of a Rolled-up Microtube Integrated with a Waveguide on a Silicon Electronic-Photonic Integrated Circuit" Optics Letters 39.9 (1 May 2014): 2699–2702. <https://www.osapublishing.org/ol/abstract.cfm?uri=ol-39-9-2699>.

Zhou, Xian, et al. "112 Gb/s Transmission over 80 Km SSMF Using PDM-PAM4 and Coherent Detection Without Optical Amplifier" Optics Express 24.15 (25 July 2016): 17359–17371. 5 Aug. 2016. <https://www.osapublishing.org/oe/abstract.cfm?uri=oe-24-15-17359>.

Zhou, Zhiping, and Li Yu. "Silicon Photonic Devices Based on Binary Blazed Gratings" Optical Engineering 52.9 (8 Mar. 2013): <http://spm.pku.edu.cn/%5Cupload%5Cfckeditor%5C2013-11%5Csilicon%20photonic_grating.pdf>.

Zhou, Zhiping, Bing Yin, and Jurgen Michel. "On-Chip Light Sources for Silicon Photonics" Light: Science & Applications 4.11 (1 Nov. 2015): 358. <http://www.nature.com/lsa/journal/v4/n11/abs/lsa2015131a.html>.

Zhou, Zhiping, et al. "Lowering the Energy Consumption in Silicon Photonic Devices and Systems" Photonics Research 3.5 (5 Aug. 2015): B28–B46. <https://www.osapublishing.org/prj/abstract.cfm?uri=prj-3-5-B28>.

Zhu, Haiming, et al. "Lead Halide Perovskite Nanowire Lasers with Low Lasing Thresholds and High Quality Factors" Nature Materials 14.6 (13 Apr. 2015): 636–642. <http://www.nature.com/nmat/journal/v14/n6/full/nmat4271.html>.

Zhu, Tiecheng, et al. "Ultrabroadband High Coupling Efficiency Fiber-to-Waveguide Coupler Using Si3N4/SiO2 Waveguides on Silicon" IEEE Photonics Journal 8.5 (Oct. 2016): 1–12. <http://ieeexplore.ieee.org/document/7544563/?tp=&arnumber=7544563>

Zhu, Yi, et al. "Strongly Enhanced Photoluminescence in Nanostructured Monolayer MoS2by Chemical Vapor Deposition" Nanotechnology 27.13 (22 Feb. 2016): 135706. <http://iopscience.iop.org/article/10.1088/0957-4484/27/13/135706/meta>.

Zimmermann, Horst. "Integrated Silicon Optoelectronics" Springer-Verlag Berlin Heidelberg, 2000. Web. <https://www.springer.com/us/book/9783662040188>.

Zimmermann, Horst. "Silicon Optoelectronic Integrated Circuits" Springer-Verlag Berlin Heidelberg, 2004. Web. <https://www.springer.com/us/book/9783540405184>.

Zografopoulos, Dimitrios C., Mohamed A. Swillam, and Romeo Beccherelli. "Electro-Optic Modulators Based on Hybrid Plasmonic Micro-Ring-Disk Resonators with Femtojoule Switching Energy." Applied Physics A 122.12 (22 Nov. 2016) <https://link.springer.com/article/10.1007/s00339-016-0529-2>.

Zuffada, Maurizio. "Vision on silicon Photonics for efficient data communications" Photonics 21 - WG6 Workshop. photonics21.org, 30 Apr. 2013. <http://www.Photonics21.Org/uploads/DQcQ0X4ZRv.Pdf>.

Zyga, Lisa. "First-of-its-kind tube laser created for on-chip optical communications" Phys-Org. 23 Jan. 2015. Web. <http://phys.org/news/2015-01-first-of-its-kind-tube-laser-on-chip-optical.html>.

