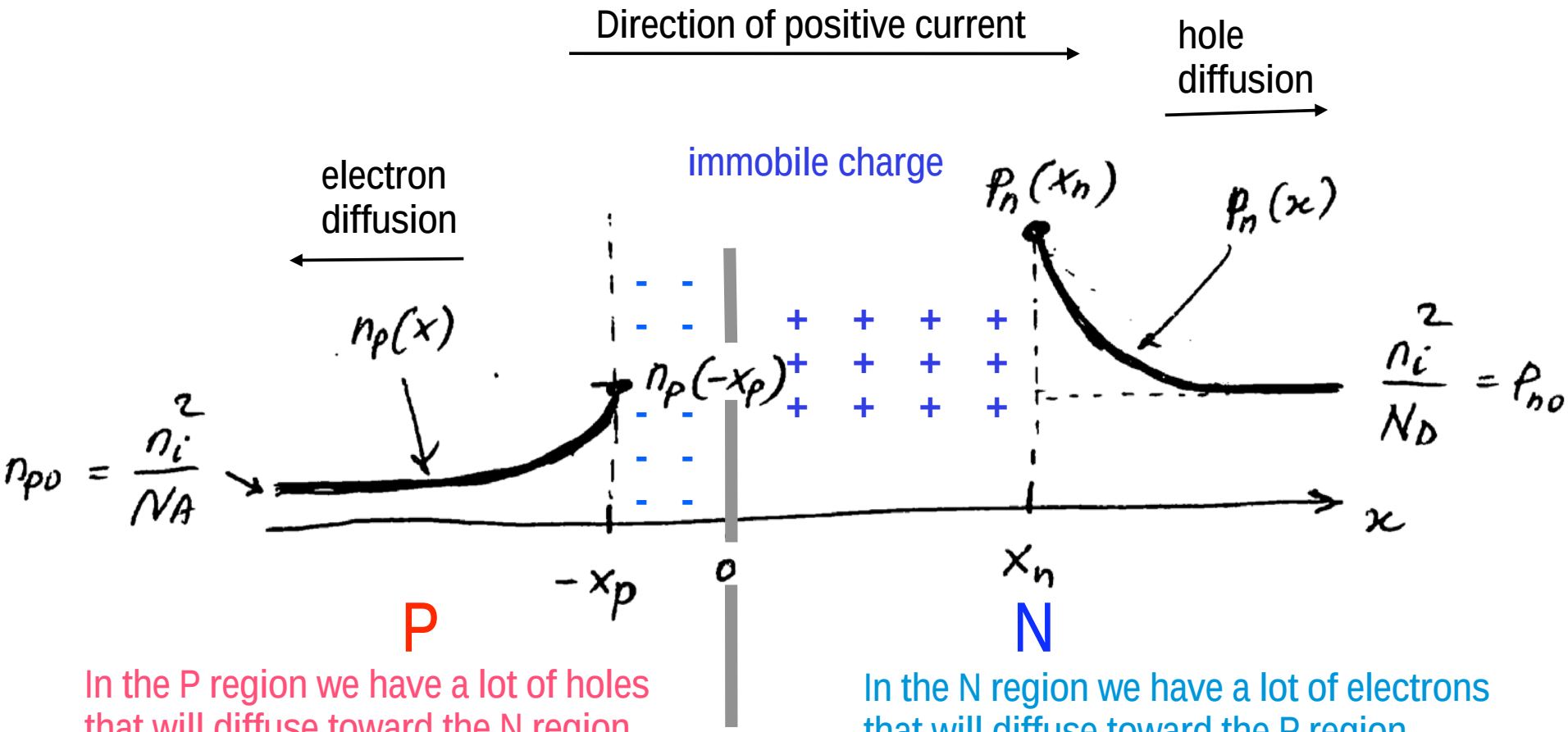
Capacitance of Forward Biased Diode

- When a diode changes from reverse biased (with little current through it) to forward biased (with significant current across it) the charge being stored near and across the junction changes
- Part of the change in charges is due to the change in the width of the depletion region and therefore the amount of immobile charge stored in it ($\rightarrow C_j$)
- An additional change in the charge storage is necessary to account for the excess of minority carriers close to the depletion region edges required for the diffusion current to exists. This component is modeled by another capacitance, called the diffusion capacitance ($\rightarrow C_d$)
- As a diode is turned off (changes from forward biased to reverse biased) for a short period of time a current will flow in the negative direction until the minority charge is removed

Charge of Forward Biased Diode



Total Capacitance of Forward Biased Diode

- It is the sum of the diffusion capacitance Cd and the depletion capacitance Cj

$$C_{total} = C_d + C_j$$

- For a forward biased diode the junction capacitance is roughly approximated by:

$$C_j \approx 2 \cdot C_{j0}$$

$$\left(C_j = 2 \cdot C_{j0} \quad for\, V_D = 0.75 \cdot \phi_0 \right)$$

- The approximation is not critical since the diffusion capacitance is typically much larger than than the depletion capacitance

$$C_d \gg C_j$$

Diffusion Capacitance

- To find the diffusion capacitance we first find the minority charge "close" the depletion edges Qd and then differentiate it with respect to the voltage applied Vd.

Small signal diffusion capacitance

$$C_d = \left[\frac{dQ_d}{dV_d} \right]_{V_D} = \tau_T \frac{I_d(@V_D)}{V_T}$$

The diffusion capacitance of a forward biased diode is proportional to the diode current

Diffusion Charge

excess of minority charge (holes) stored in the N region

excess of minority charge (electrons) stored in the P region

$$Q_d = Q_p + Q_n$$

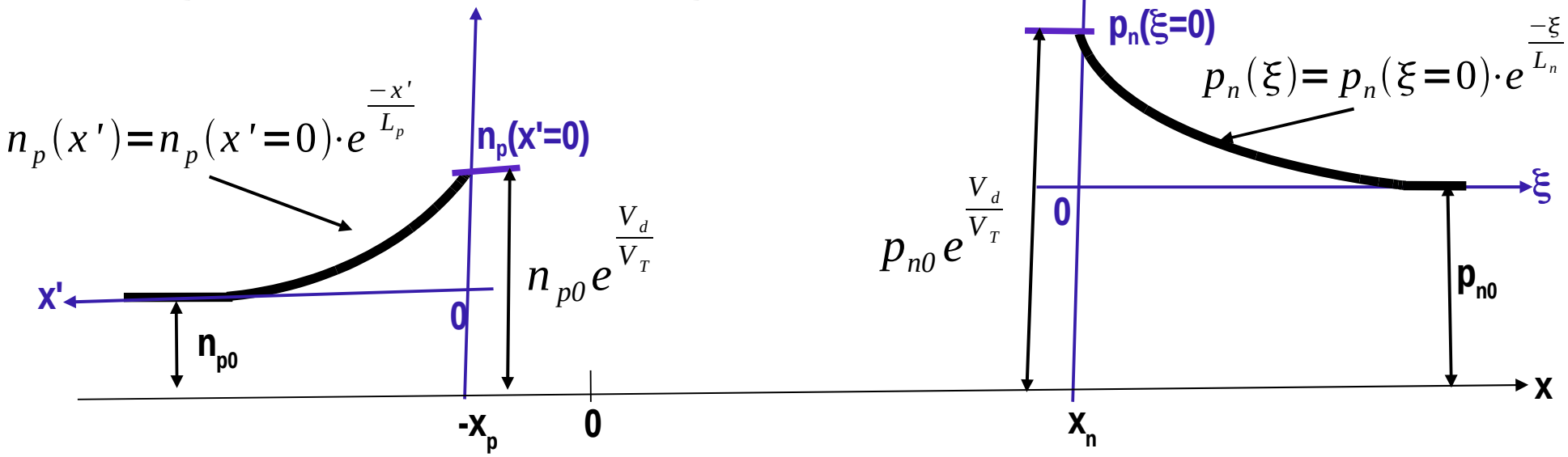
$$Q_p = qA\int_0^\infty n_p(x')\,dx' = qA\int_0^\infty n_p(0)\,e^{\frac{-x'}{L_p}}\,dx' =$$

$$= qA\int_0^\infty n_{p0}\left(e^{\frac{V_d}{V_T}}-1\right)e^{\frac{-x'}{L_p}}\,dx' =$$

$$= qAn_{p0}\left(e^{\frac{V_d}{V_T}}-1\right)\int_0^\infty e^{\frac{-x'}{L_p}}\,dx' =$$

$$= qA\frac{n_i^2}{N_D}\left(e^{\frac{V_d}{V_T}}-1\right)\left[-L_p e^{\frac{-x'}{L_p}}\right]_0^\infty = \frac{qAn_i^2 L_p}{N_D}\left(e^{\frac{V_d}{V_T}}-1\right)$$

$$Q_n = \frac{qAn_i^2 L_n}{N_A}\left(e^{\frac{V_d}{V_T}}-1\right)$$



Diffusion Charge

- The excess hole charge stored in the N region is given by:

$$p_n(x_n) = p_{n0}\left(e^{V_d/V_T} - 1\right)$$

$$Q_p = A q [\, p_n(x_n) - p_{n0}] L_p =$$

$$= A q L_p p_{n0}\left(e^{V_d/V_T} - 1\right) =$$

$$= A J_p \frac{L_p^2}{D_p} = I_p \frac{L_p^2}{D_p} = I_p \tau_p$$

$$J_p = \frac{q D_p}{L_p} p_{n0}\left(e^{V_d/V_T} - 1\right)$$

$$p_{n0}\left(e^{V_d/V_T} - 1\right) = J_p \frac{L_p}{q D_p}$$

$$L_p = \sqrt{D_p \tau_p}$$

- Similarly, the excess electron charge stored in the P region is:

$$Q_n = I_n \tau_n$$

Total Diffusion Charge

- Thus, the total excess minority carrier charge is:

$$Q_d = Q_p + Q_n = I_p \tau_p + I_n \tau_n$$

- Since the diode current is $I_d = I_p + I_n$ it is more convenient to express the excess charge as:

$$Q_d = \tau_T \cdot I_d \qquad (\text{where } \tau_T \text{ is called } \textbf{mean transit time})$$

Diffusion Capacitance

$$C_d = \left[\frac{dQ_d}{dV_d}\right]_{V_D} = \left[\frac{d(\tau_T I_d)}{dV_d}\right]_{V_D} = \tau_T \left[\frac{dI_d}{dV_d}\right]_{V_D} = \frac{\tau_T}{r_d}$$

$$\frac{1}{r_d} \equiv \left[\frac{dI_d}{dV_d}\right]_{V_D} = \left[\frac{d\left(I_s \cdot \left(e^{\frac{V_d}{V_T}} - 1\right)\right)}{dV_d}\right]_{V_D} = \left[\frac{I_s e^{\frac{V_d}{V_T}}}{V_T}\right]_{V_D} = \left[\frac{I_d + I_s}{V_T}\right]_{V_D} \approx \left[\frac{I_d}{V_T}\right]_{V_D}$$

$$C_d \approx \tau_T \left[\frac{I_d}{V_T}\right]_{V_D}$$

Transition Time

- The general expression for τ_T is quite cumbersome:

$$\tau_T = C_d \cdot r_d$$

where $$\frac{1}{r_d} \equiv \left[\frac{dI_d}{dV_d} \right]_{V_D} \qquad \textit{with} \qquad I_d = \left(\frac{qAD_n}{L_n} \frac{n_i^2}{N_A} + \frac{qAD_p}{L_p} \frac{n_i^2}{N_D} \right) \left(e^{\frac{V_d}{V_T}} - 1 \right)$$

$$C_d = \left[\frac{dQ_d}{dV_d} \right]_{V_D} \qquad \textit{with} \qquad Q_d = \left(\frac{qAn_i^2 L_p}{N_D} + \frac{qAn_i^2 L_n}{N_A} \right) \left(e^{\frac{V_d}{V_T}} - 1 \right)$$

Transition Time

- In practice, since usually diodes are single sided (i.e. one side will be much more heavily doped than the other side) the minority charge storage in the heavily doped side can be ignored

$$Q_p = \frac{q A n_i^2 L_p}{N_D}\left(e^{\frac{V_d}{V_T}} - 1\right) \qquad Q_n = \frac{q A n_i^2 L_n}{N_A}\left(e^{\frac{V_d}{V_T}} - 1\right)$$

- Assuming the P side is more heavily doped than the N side:

$$N_A \gg N_D \;\rightarrow\; Q_p \gg Q_n \;\rightarrow\; Q_d \approx Q_p \;\rightarrow\; I_d \approx I_p$$

$$\tau_T \approx \tau_p = \frac{L_p^2}{D_p}$$

NOTE:
- Holes (Qp) are minority carriers on the N side
- Electrons (Qn) are minority carriers on the P side

Single Sided Diodes

- One side of the diode is more heavily doped than the other
- Many of the junctions encountered in integrated circuits are one-sided junctions with the lightly doped side being the substrate or the well.
- Foe single sided diodes the depletion region will extend mostly on the lightly doped side.
- The depletion capacitance is almost independent of the doping concentration on the heavily doped side

Single Sided Diodes

- The PN junctions inside CMOS ICs are single-sided
- NMOS transistors have parasitic diodes with the N side more heavily doped than the P side: $N_D \gg N_A$
- PMOS transistors have parasitic diodes with the P side more heavily doped than the N side: $N_A \gg N_D$

- NOTE: in general within an MOS transistor, it is undesirable to have a forward biased junction, it usually means there is a problem.

Schottky Diodes

- A different type of diode, can be realized by contacting a metal to a lightly doped semiconductor region.
- The use of a lightly doped semiconductor, causes a depletion region to form at the interface between the aluminum anode and the n+ silicon region

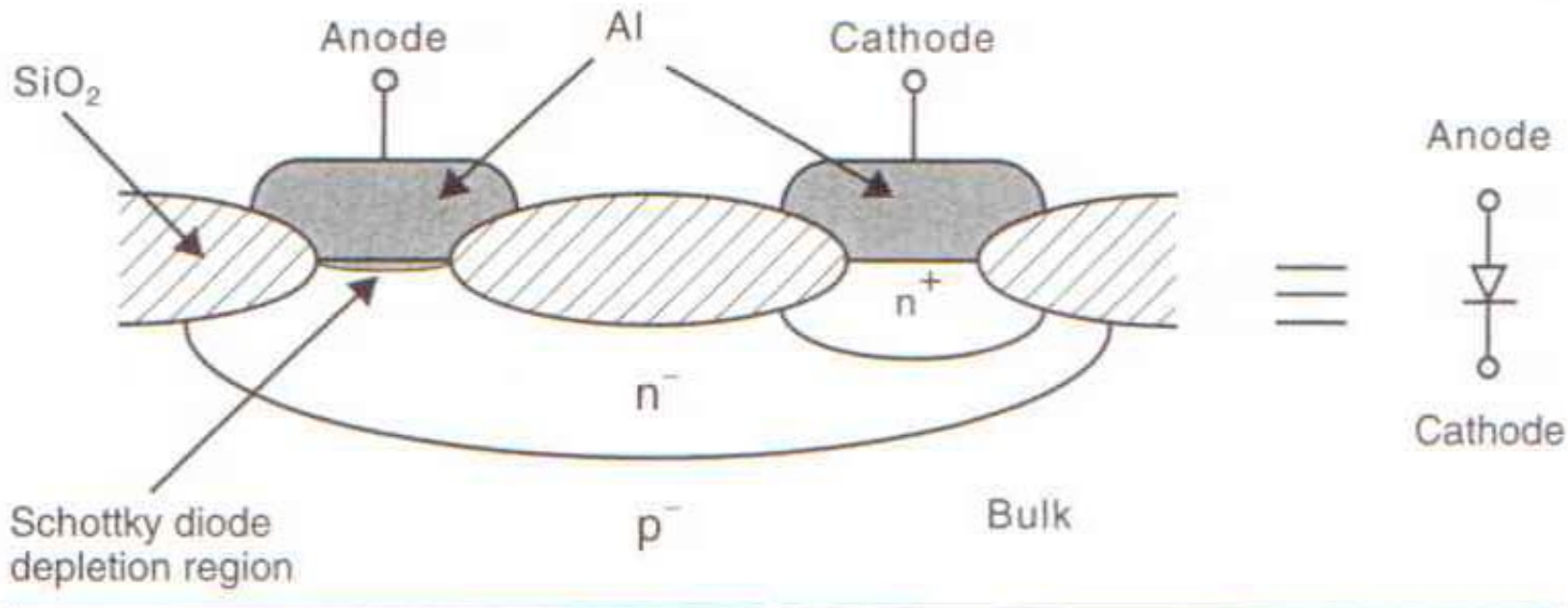


Fig. 1.5 A cross section of a Schottky diode.

Schottky Diodes

- The voltage drop of a forward biased Schottky diode is smaller. The value depends on the metal used. For aluminum is approx 0.5 V
- When the diode is forward biased there is no minority charge storage in the lightly doped n+ region. Thus Cd = 0
- The absence of diffusion capacitance makes the diode much faster.

Diodes realized in CMOS technology

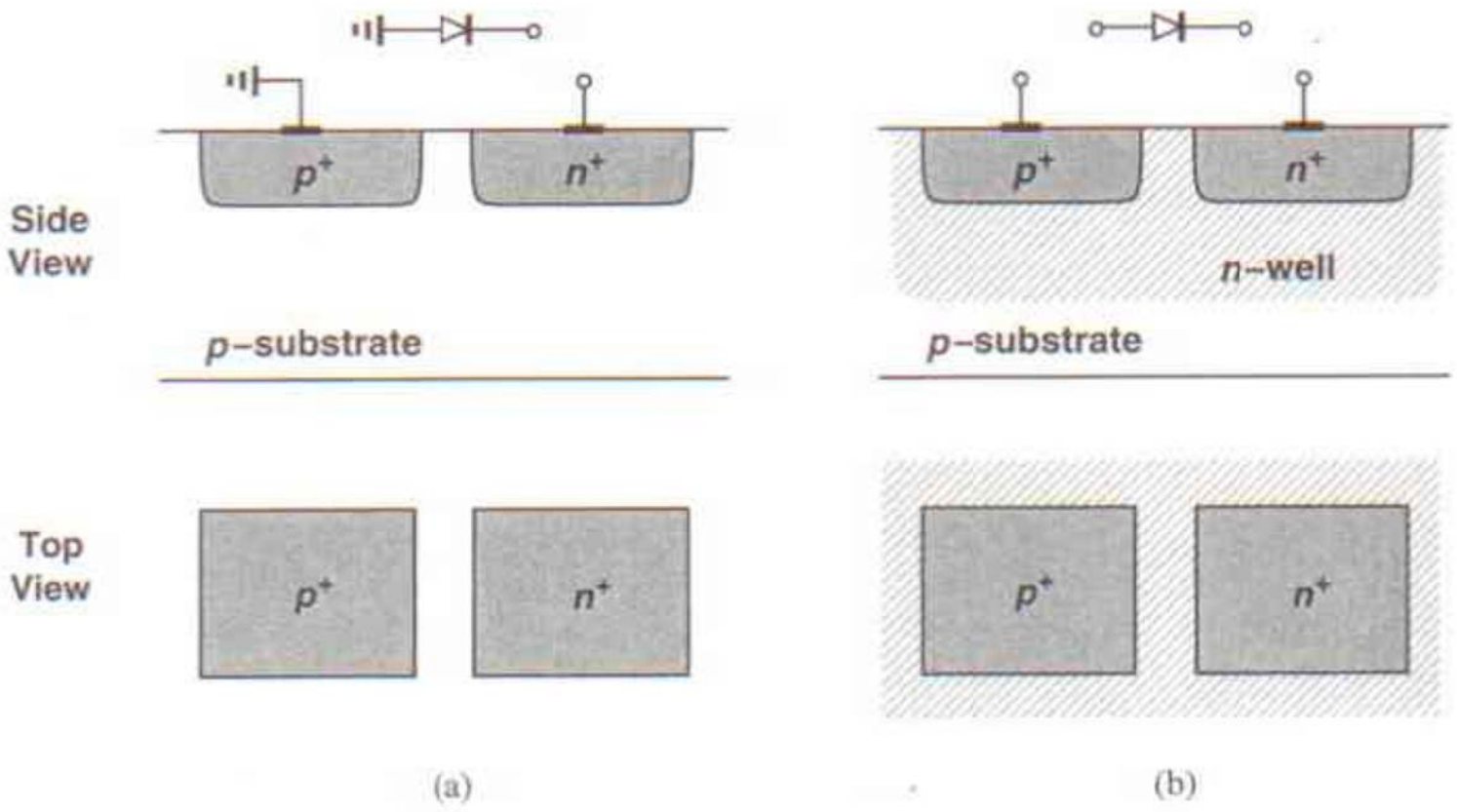


Figure 14.54 Diodes realized in CMOS technology.

NOTE:
For the case of Fig 14.54(a) the anode is inevitably grounded

Diode SPICE model

Parameter	SPICE	Description
I_S	IS	Saturation Current
R_s	RS	Ohmic Series Resistance of the p-n regions and the contacts
n	N	Emission Coefficient
ϕ_0	VJ, PB, PHI	Built-in Voltage
C_{j0}	CJ0, CJ	Zero Bias Junction Capacitance
M_j	MJ, M	Grading Coefficient
τ_T	TT	Transit Time
V_K	BV	Reverse Breakdown Knee Voltage
I_K	IBV	Reverse Breakdown Knee Current

Diode SPICE Modeling

$$I_d = I_s\left[\exp\left(\frac{V_d}{nV_T}\right)-1\right]+\underbrace{GMIN\cdot V_d}_{\text{Convergence Aid}}$$

$$I_d = -I_s\left[\exp\left(-\frac{BV+V_d}{V_T}\right)-1+\frac{BV}{V_T}\right]$$

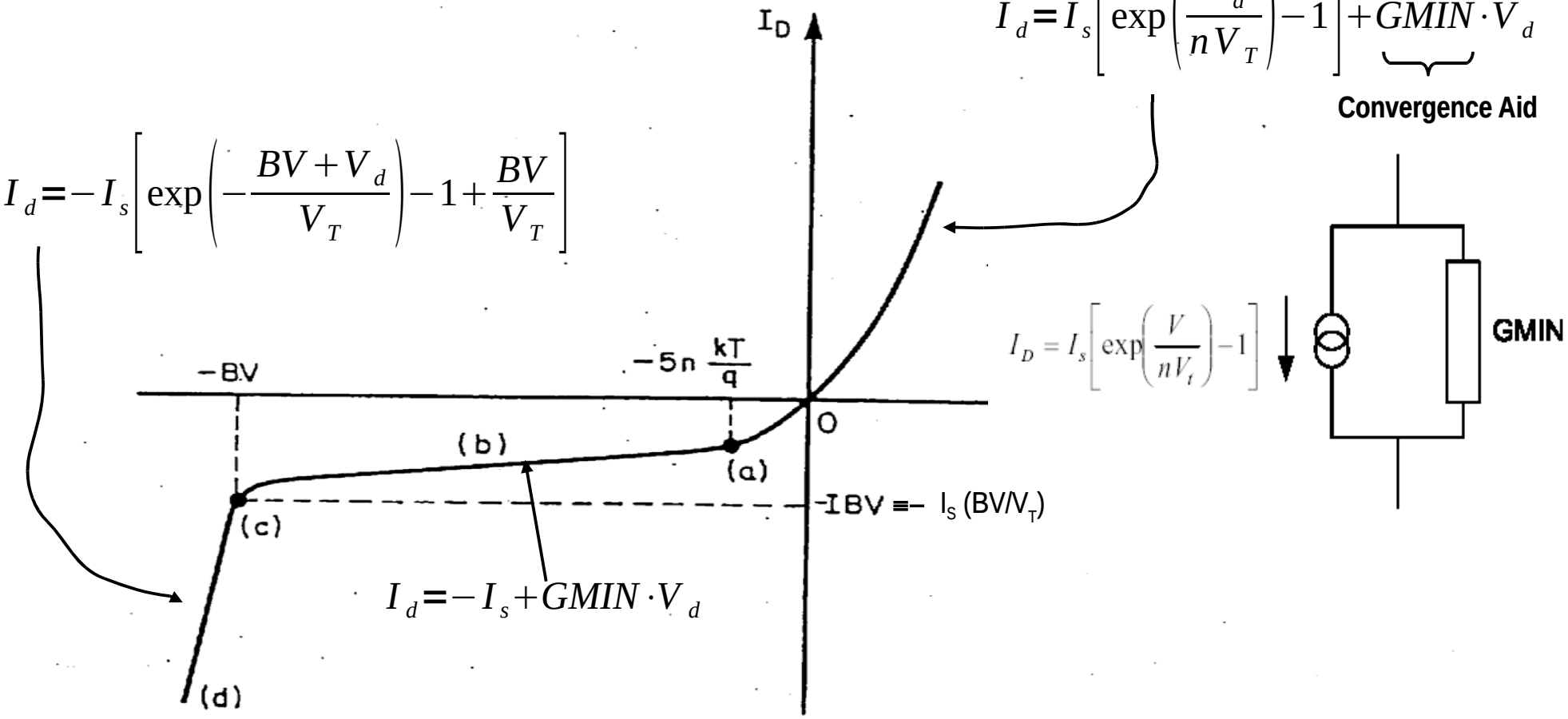


Figure 1-15 Reverse characteristic of the real diode.

From: P. ANTOGNETTI, G. MASSOBRIO
Semiconductor device modeling with SPICE
McGraw-Hill, New York, 1988

MOS physical structure

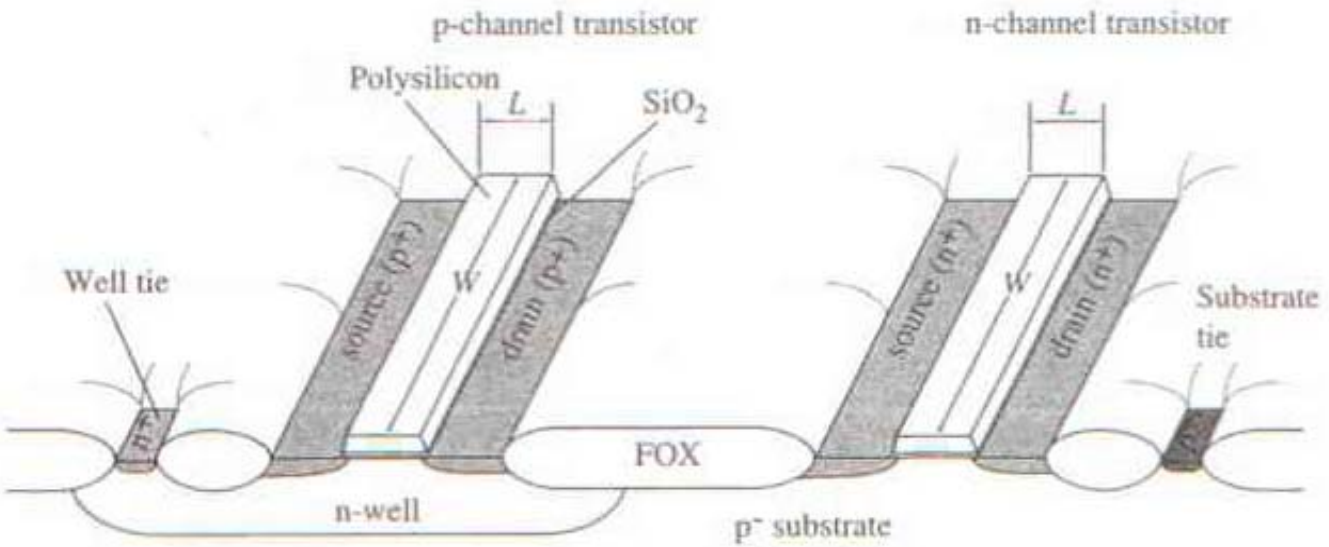


Figure 2.3-1 Physical structure of an n-channel and p-channel transistor in an n-well technology.

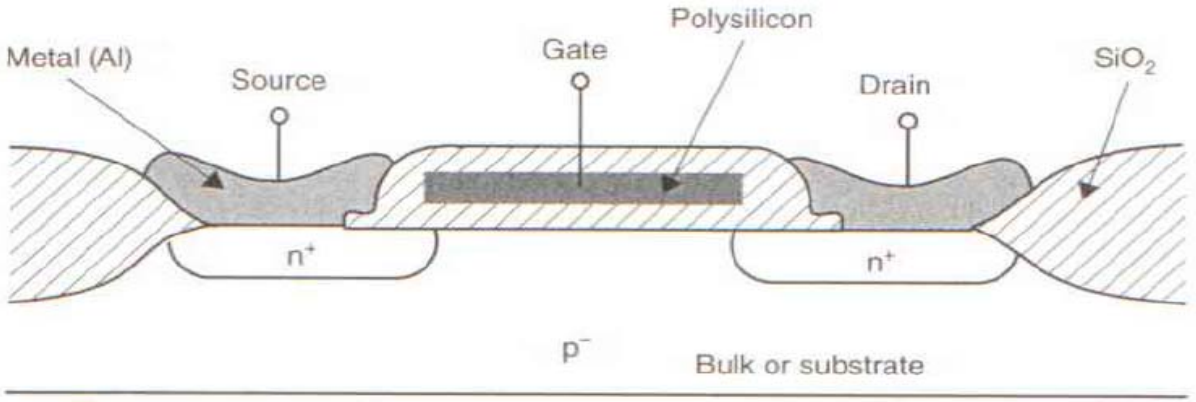


Fig. 1.6 A cross section of a typical n-channel transistor.

Thermal Equilibrium

- Absence of any stimulus to the device
- The populations of electrons and holes are each in equilibrium and, therefore must have zero current densities

$$\begin{cases} 0 = q\, n_0 \mu_n E_0 + q\, D_n \dfrac{Dn_0}{dx} \\ 0 = q\, n_0 \mu_p E_0 - q\, D_p \dfrac{dp_0}{dx} \end{cases} \quad \longleftrightarrow \quad 0 = -n_0 \mu_n \frac{d\phi_0}{dx} + D_n \frac{dn_0}{dx}$$

$$d\phi_0 = \frac{D_n}{\mu_n}\frac{dn_0}{n_0} \quad \longleftrightarrow \quad d\phi_0 = V_T \frac{dn_0}{n_0} \quad \longleftrightarrow \quad \int_{x_R}^{x} d\phi_0 = V_T \int_{x_R}^{x} \frac{dn_0}{n_0}$$

$$\phi_0(x) - \phi_0(x_R) = V_T \ln\left(\frac{n_0(x)}{n_0(x_R)}\right)$$

Thermal Equilibrium

$$\longleftrightarrow \quad \phi_0(x) - \phi_0(x_R) = V_T \ln\left(\frac{n_0(x)}{n_0(x_R)}\right)$$

By convention the reference for the potential is chosen to be the point where the carrier concentration is the intrinsic concentration

$$\phi_0(x_R) = 0 \qquad when \quad n_0(x_R) = n_i$$

$$\phi_0(x) = V_T \ln\left(\frac{n_0(x)}{n_i}\right) \longleftrightarrow n_0(x) = n_i e^{\frac{\phi_0(x)}{V_T}}$$

NOTE:
for N type silicon since $n_0 > n_i$ the electrostatic potential at equilibrium is positive

Thermal Equilibrium

A similar derivation for the hole concentration leads to the following result:

$$\phi_0(x) = -V_T \ln\left(\frac{p_0(x)}{n_i}\right) \longleftrightarrow p_0(x) = n_i e^{\frac{-\phi_0(x)}{V_T}}$$

NOTE:
for P type silicon since $p_0 > n_i$ the electrostatic potential at equilibrium is negative

MOS Capacitor in Thermal Equilibrium

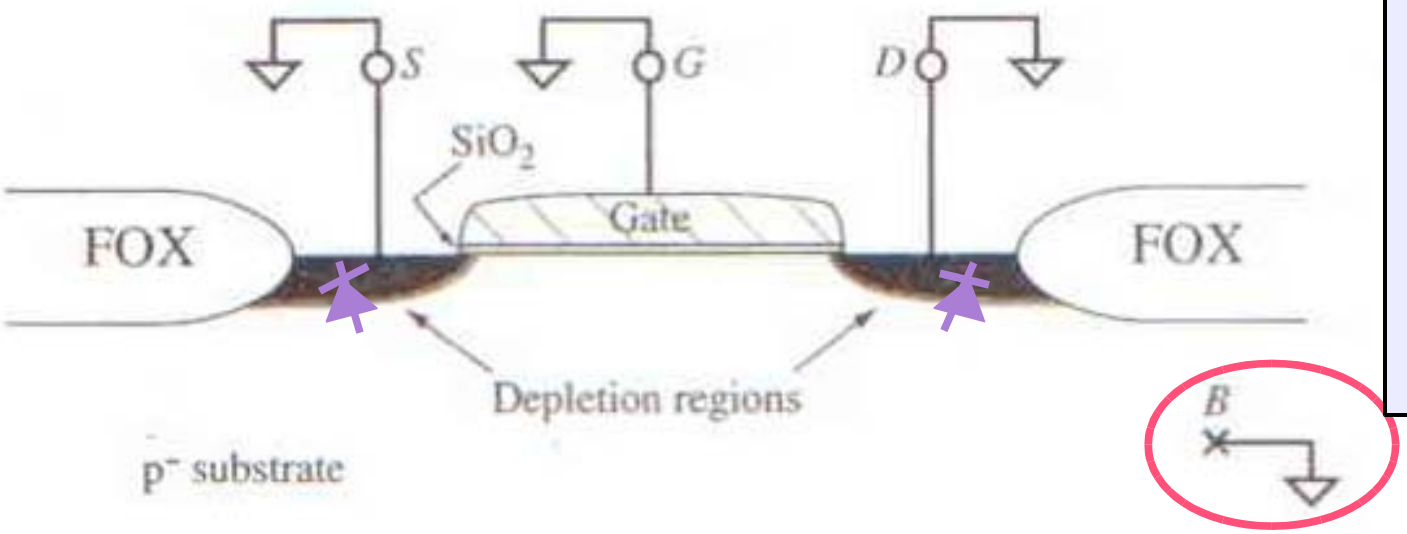


Figure 2.3-2 Cross section of an n-channel transistor with all terminals grounded.

At equilibrium the p-substrate and the n+ source and drain form a pn junction. Therefore a depletion region exists between the n+ source and drain and the p- substrate

Since source and drain are separated by back-to-back junctions, the resistance between the source and the drain is very high (> 10^{12} ohm)

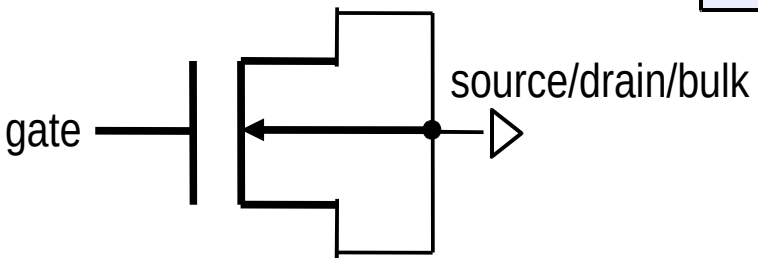
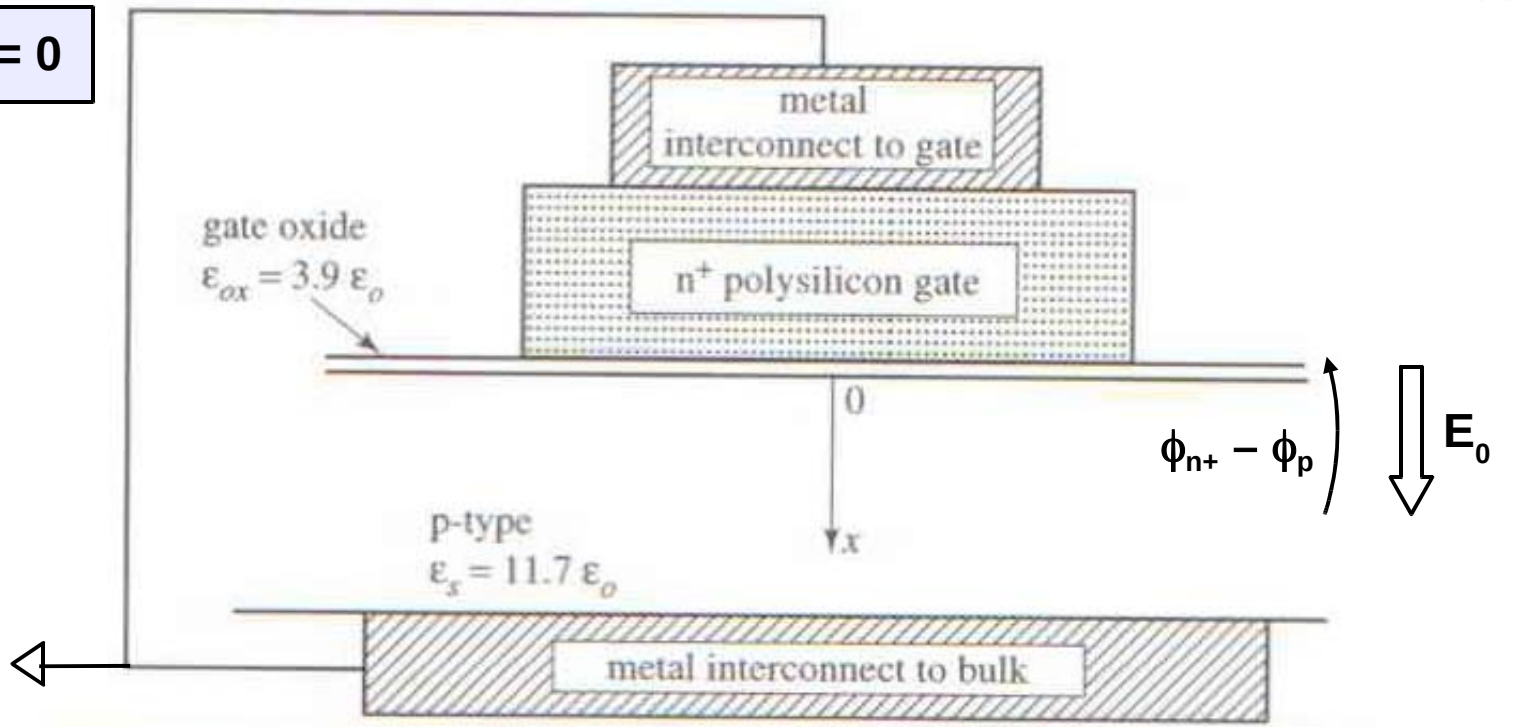


Figure. Using the MOSFET as a capacitor

The gate and the substrate of the MOS transistor form a parallel plate capacitor with the SiO_2 as dielectric

MOS structure in Thermal Equilibrium

$V_{GB} = 0$



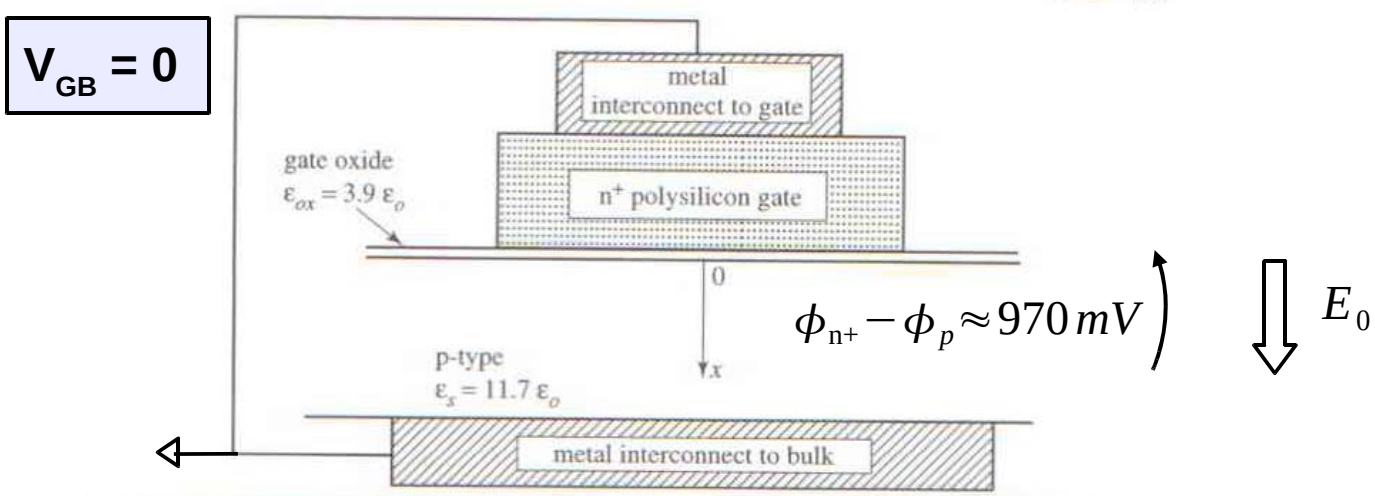
➤ **Figure 3.20** MOS capacitor with p-type substrate. Gate and bulk metal contacts are shorted together for thermal equilibrium.

equilibrium potential in the silicon (bulk=substrate) $\phi_p = -V_T \ln\left(\frac{N_A}{n_i}\right)$

equilibrium potential in the polysilicon (gate) $\phi_{n+} = V_T \ln\left(\frac{N_D}{n_i}\right)$

$N_A = 10^{17}\,cm^{-3}$ $N_D = 3\cdot 10^{19}\,cm^{-3}$ $n_i = 10^{10}\,cm^{-3}$ $\rightarrow$ $\phi_{n+} - \phi_p = 550\,mV - (-420\,mV) = 970\,mV$

MOS in Thermal Equilibrium

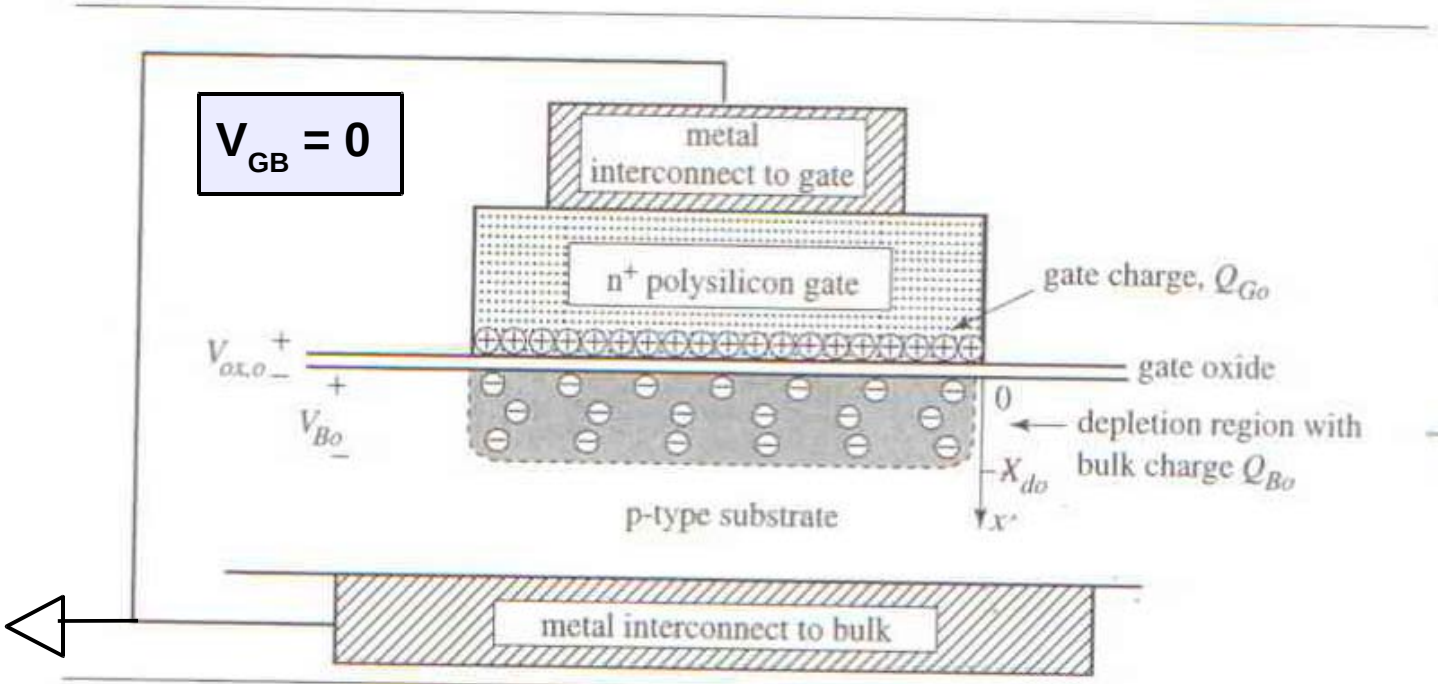


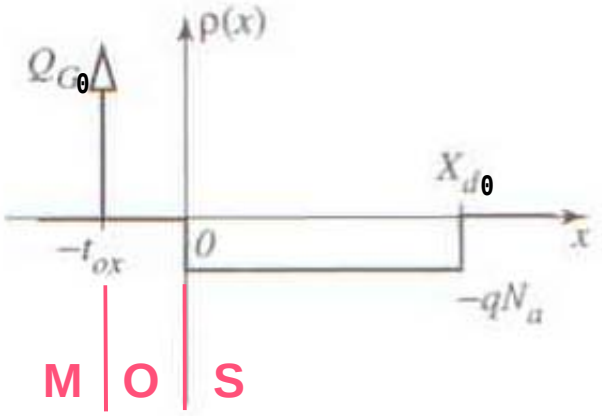
➤ **Figure 3.20** MOS capacitor with p-type substrate. Gate and bulk metal contacts are shorted together for thermal equilibrium.

- From the sign of the potential drop across the MOS structure it follows that the electric field points from gate to bulk.
- Therefore, a positive charge must be present on the polysilicon gate and there must be a balancing negative charge in the p-type silicon substrate (the oxide will be considered a charge-free perfect insulator)

Charge on the MOS in TE

- Since the gate is highly conductive n+ polysilicon the gate charge Q_{G0} can be thought as a sheet charge located at the bottom surface of the polysilicon gate
- The charge on the p-type silicon substrate Q_{B0} is formed by the immobile negatively charged acceptor ions (to a depletion depth of X_{d0}) left behind by the mobile holes repelled by the positive charge on the gate.

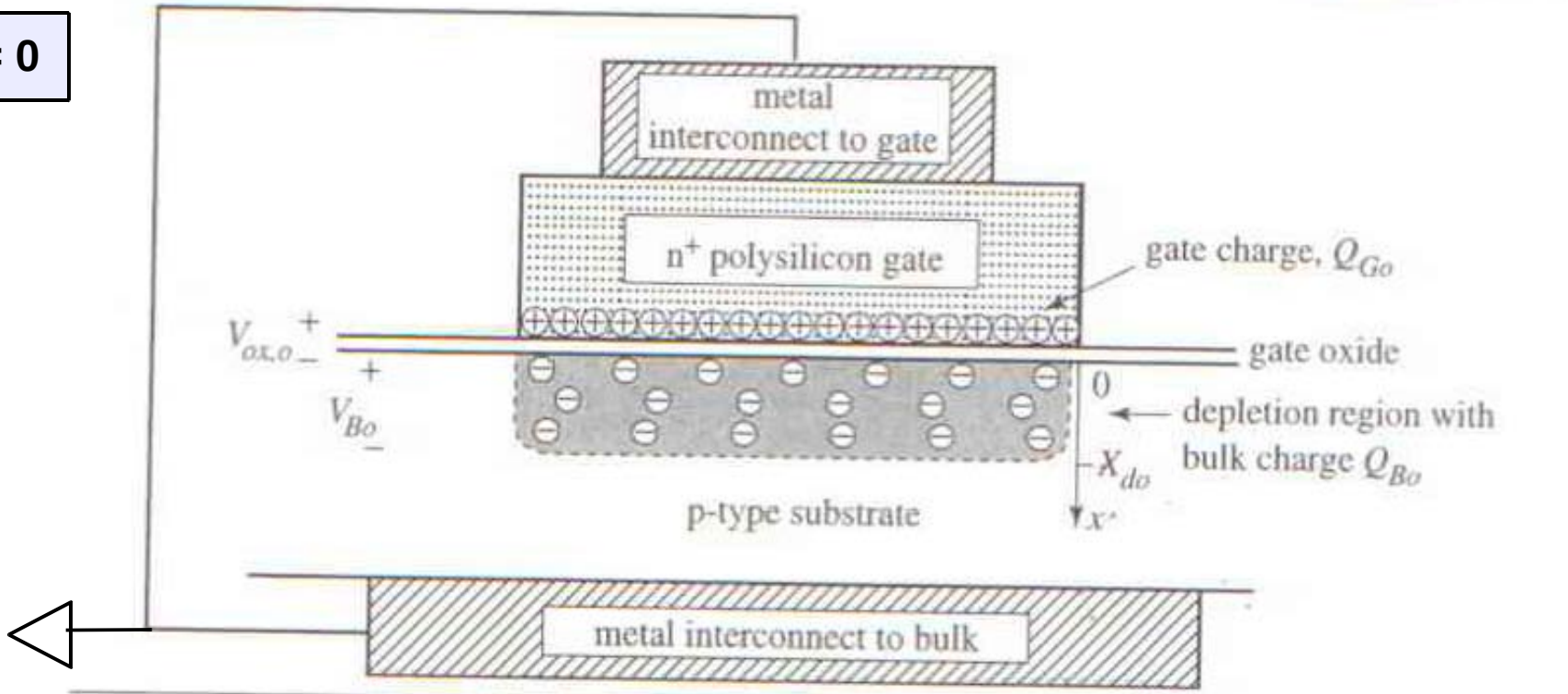




➤ **Figure 3.21** Qualitative picture of charge distribution in an MOS capacitor with p-type substrate in thermal equilibrium.

Charge on the MOS in TE

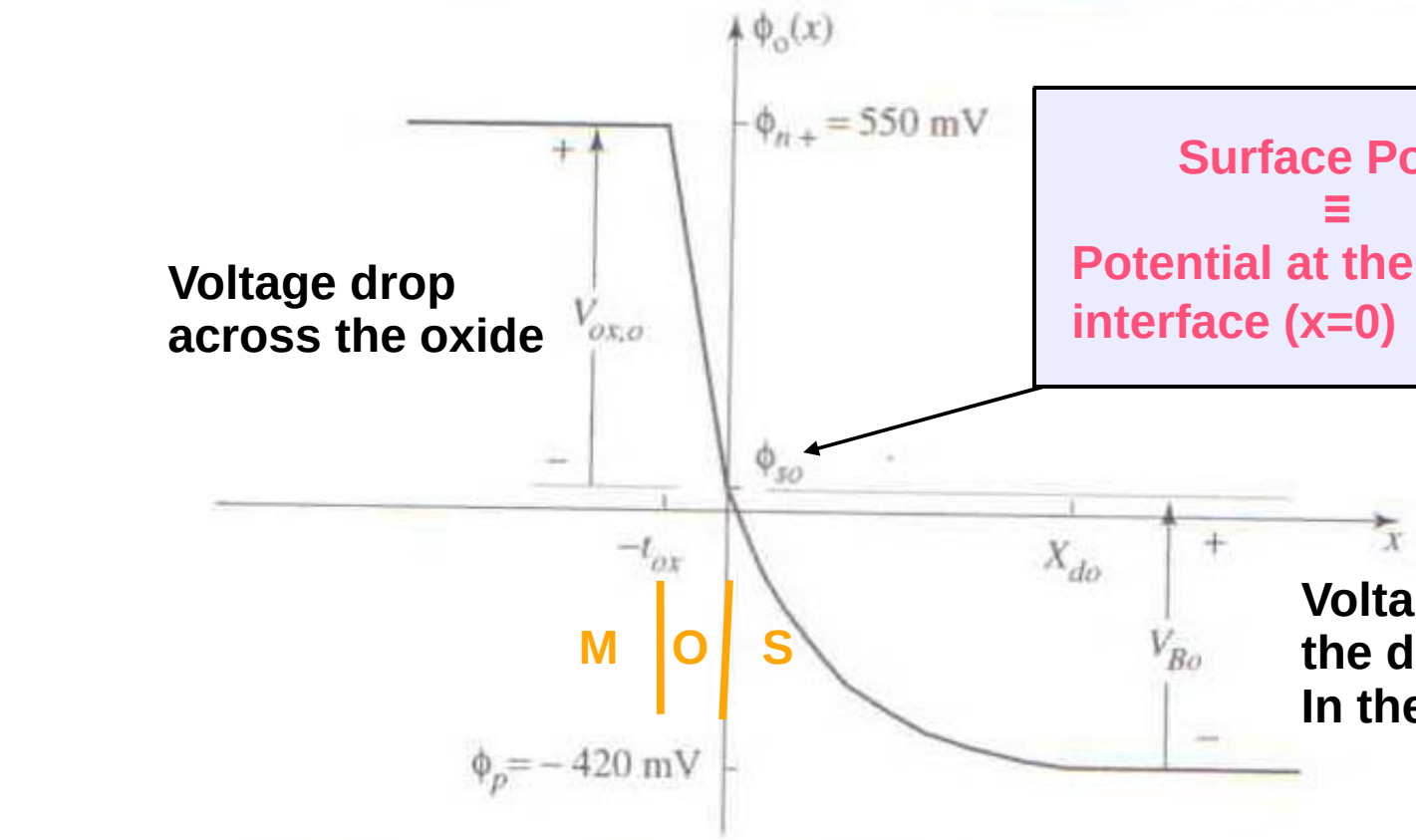
$V_{GB} = 0$



➤ **Figure 3.21** Qualitative picture of charge distribution in an MOS capacitor with p-type substrate in thermal equilibrium.

$$Q_{G0} = -Q_{B0} = q N_A X_{d0} \quad [units: C/cm^2]$$

Potential across the MOS in TE



Surface Potential ≡ Potential at the SiO_2-silicon interface (x=0)

Voltage drop across the oxide

Voltage drop across the depletion region In the silicon

➤ **Figure 3.22** Potential plot for MOS capacitor with p-type substrate in thermal equilibrium. The substrate doping concentration is $N_a = 10^{17}$ cm^{-3}.

Built in Voltage across the MOS structure

$$\phi_{\text{BUILT-IN}} \equiv \phi_{n+} - \phi_p = V_{ox,0} + V_{B,0}$$

Potential across the MOS in TE

- The equilibrium potential of a given material is commonly referred as its Fermi potential

$$\phi_{n+} \equiv \phi_{\text{F-gate}} = V_T \ln\left(\frac{N_D}{n_i}\right) \qquad \phi_p \equiv \phi_{\text{F-bulk}} = -V_T \ln\left(\frac{N_A}{n_i}\right)$$

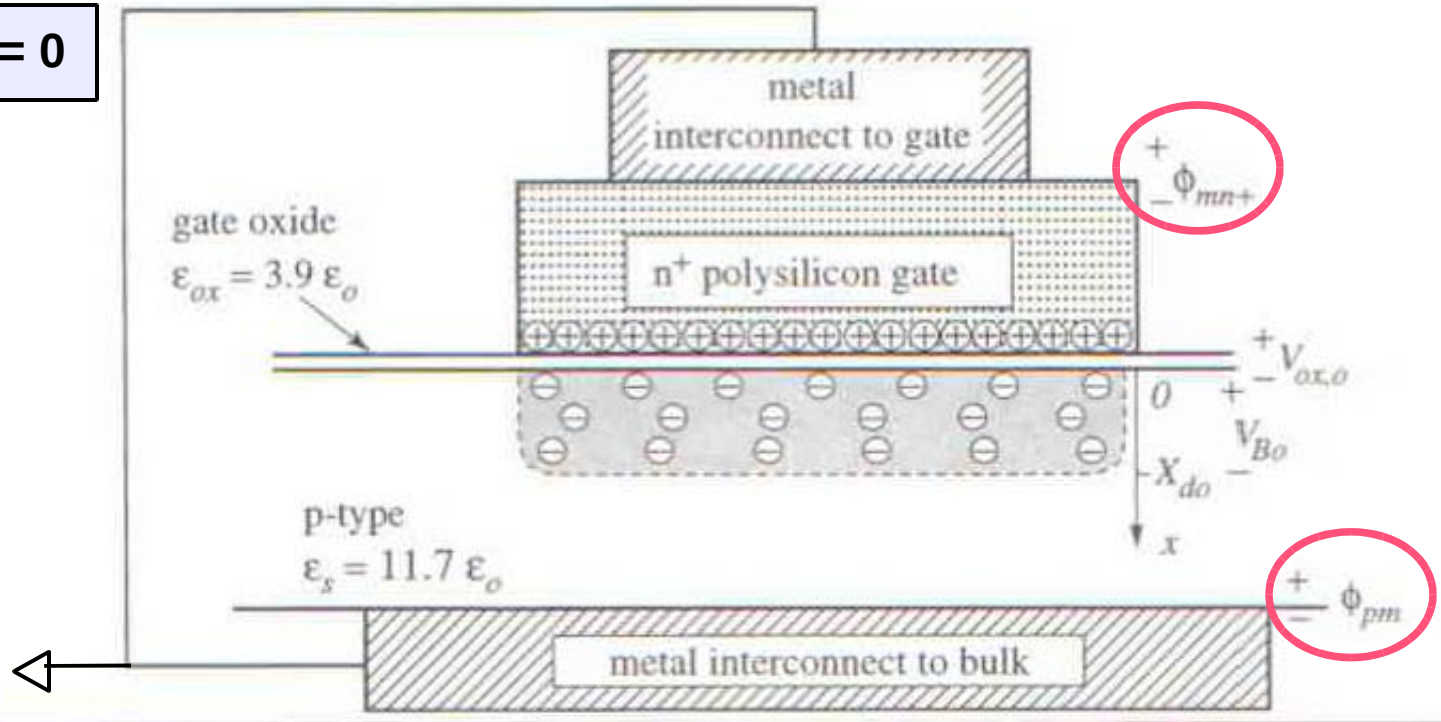
- The Built in voltage across the MOS structure is often expressed in term of the work function between the gate material and the bulk silicon

$$-\phi_{MS} \equiv \phi_{\text{F-gate}} - \phi_{\text{F-bulk}} = \phi_{n+} - \phi_p \equiv \phi_{\text{BUILT-IN}} = V_T \ln\left(\frac{N_D N_A}{n_i^2}\right)$$

NOTE: This term is referred as the metal-to-silicon work function even though the gate terminal is something other than metal (i.e. polysilicon)

MOS in TE: "fixing" KVL

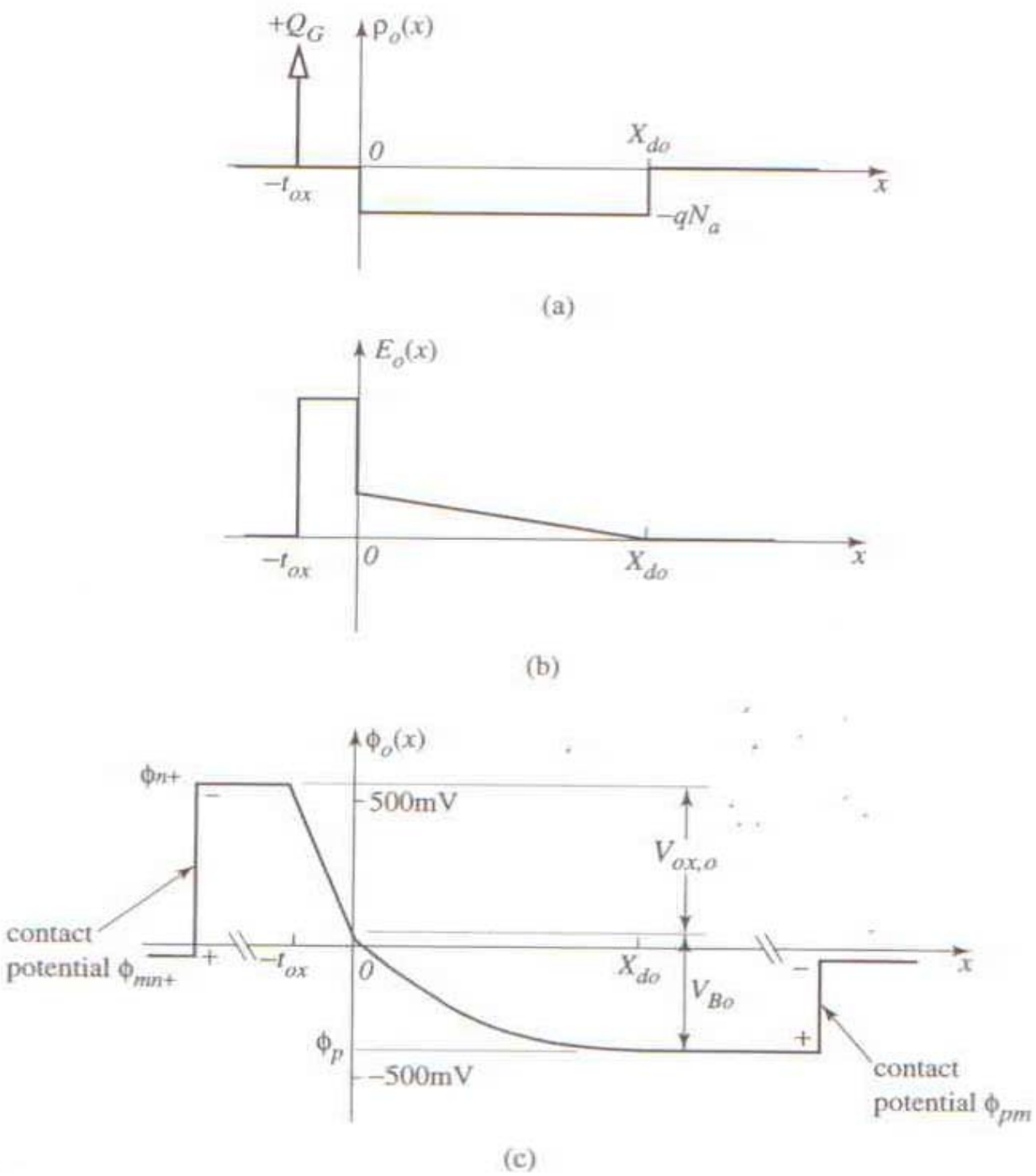
$V_{GB} = 0$



➤ **Figure 3.28** MOS capacitor with p-type substrate, with the charge distribution taken from Fig. 3.21. Gate and bulk metal contacts shorted together for the thermal equilibrium analysis.

$$\phi_{\text{mn+}} + V_{ox,0} + V_{B0} + \phi_{pm} = 0 \quad \longleftrightarrow \quad \underbrace{V_{ox,0} + V_{B0}}_{= (\phi_{\text{n+}} - \phi_p) \equiv \phi_{\text{BUILT-IN}}} = -(\phi_{\text{mn+}} + \phi_{pm})$$

MOS in TE

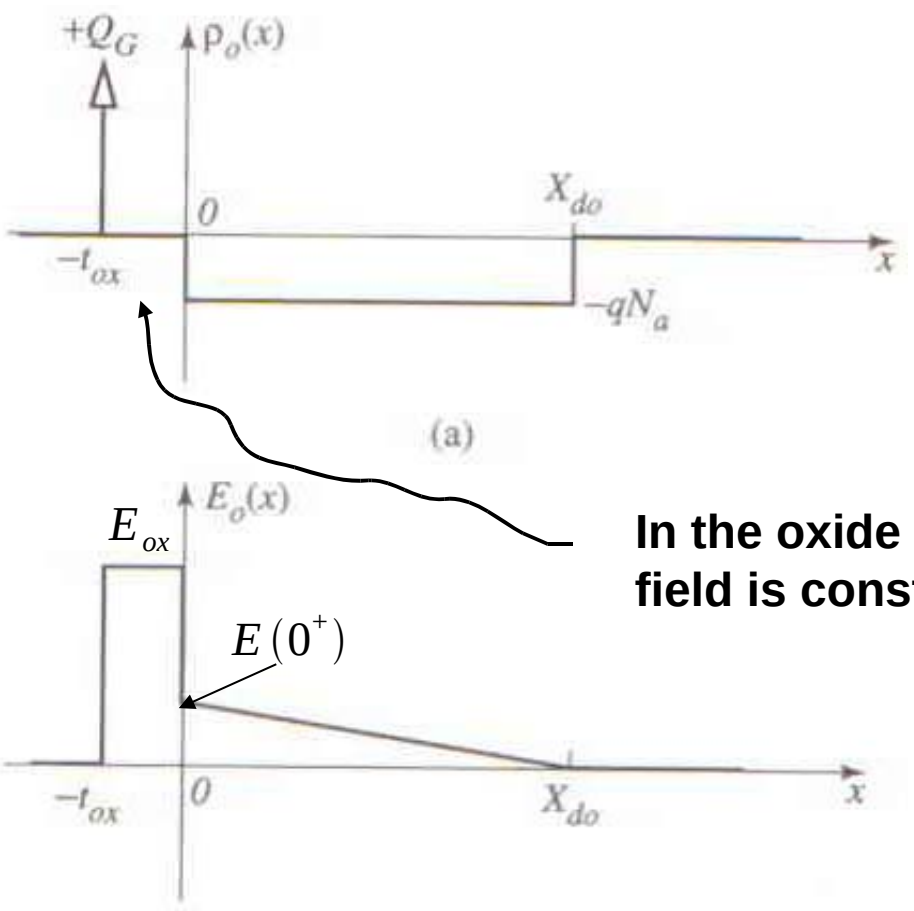


➤ **Figure 3.29** MOS capacitor in thermal equilibrium: (a) charge density $\rho_o(x)$, (b) electric field $E_o(x)$, and (c) electrostatic potential $\phi_o(x)$. The potential jumps at the metal contacts to the n^+ polysilicon gate and to the p-type bulk are both negative quantities in (c).

NOTE:
for the case of TE the gate and the bulk metal contacts are at the same potential

$$\phi_{n+} - \phi_p = -(\phi_{mn+} + \phi_{pm})$$

MOS in TE: Quantitative Analysis



The total excess charge in the region $-t_{ox} \le x \le X_{d0}$ is zero (neutrality of charge)

The electric field is confined in the region $-t_{ox} < x < X_{d0}$

In the oxide ($-t_{ox} < x < 0$) the charge density is zero thus the field is constant (E_{ox}):

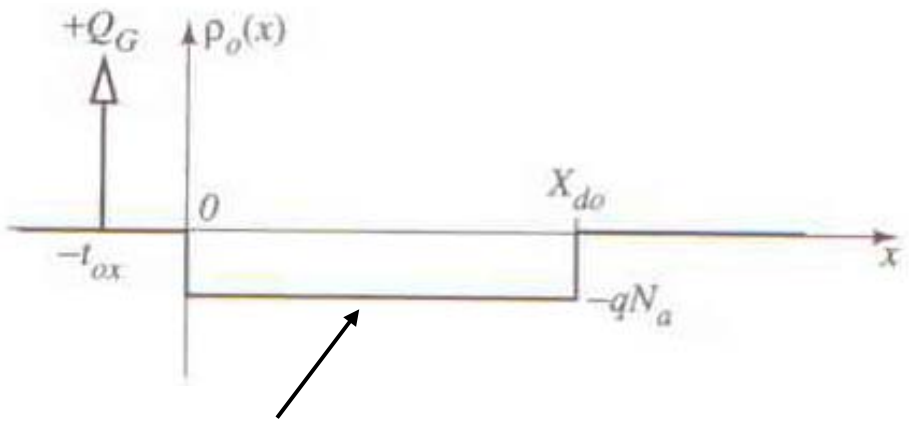
$$Gauss's\ Law: \quad \frac{dE}{dx} = \frac{\rho}{\epsilon}$$ ($\rho \approx 0$)

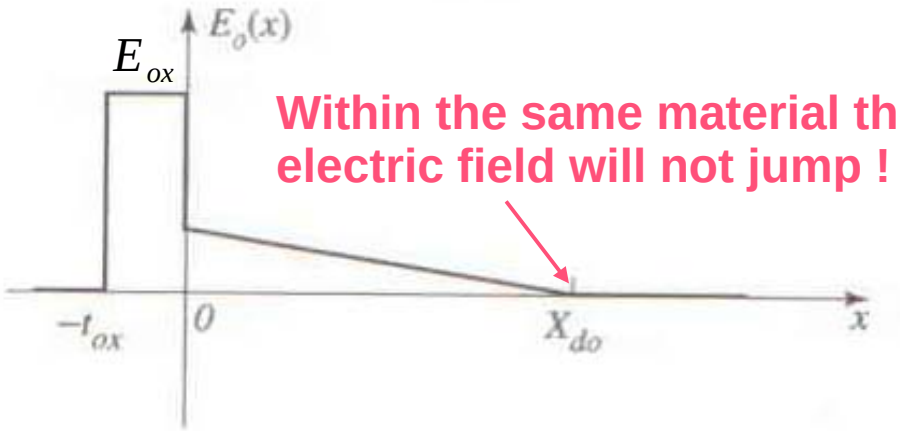
Boundary condition at the oxide/silicon interface ($0^- \le x \le 0^+$):

$$\epsilon_{ox} \cdot E_{ox} = \epsilon_s \cdot E(0^+) \rightarrow E(0^+) = \frac{\epsilon_{ox}}{\epsilon_s} E_{ox} \rightarrow E_{ox} = E(0^+) \frac{\epsilon_s}{\epsilon_{ox}}$$

$\frac{\epsilon_s}{\epsilon_{ox}} \approx 3$

MOS in TE: Quantitative Analysis





Within the same material the electric field will not jump !

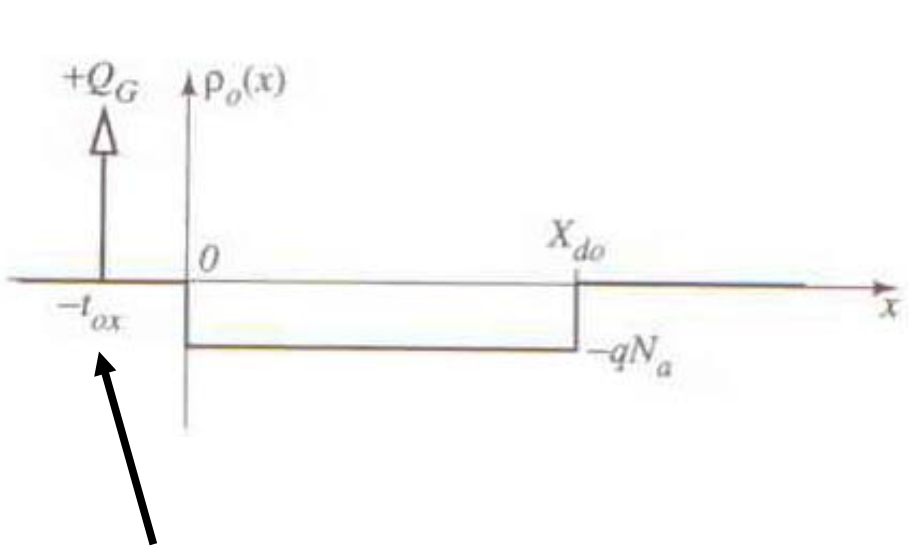
In the charged region of the silicon oxide/silicon interface ($0+ \leq x < X_{d0}$) the charge density is constant:

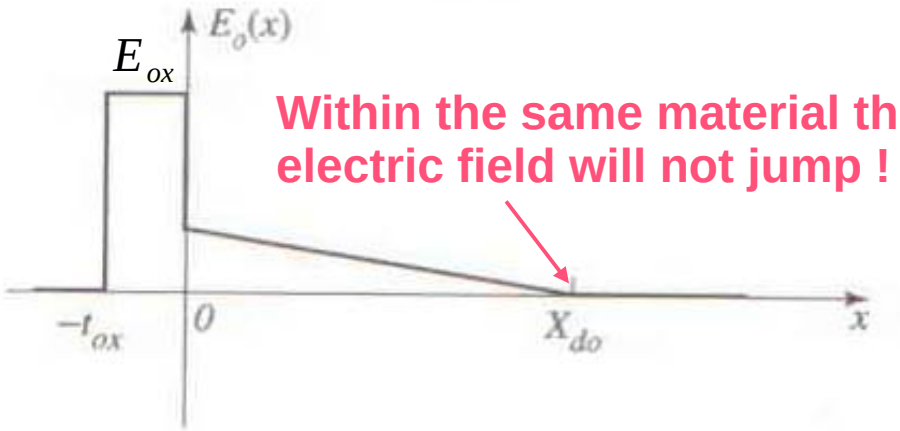
$$dE(x) = \frac{-q N_A}{\epsilon_s} dx \rightarrow \int_{E(0+)}^{E(X_{do})} dE(x) = \frac{-q N_A}{\epsilon_s} \int_{0+}^{X_{do}} dx \rightarrow$$

$$\rightarrow \epsilon_s E(\cancel{X_{d0}}^{0}) - \epsilon_s E(0^+) = -q N_A X_{d0} \rightarrow \boxed{E(0^+) = \frac{q N_A}{\epsilon_s} X_{d0}}$$

$$\boxed{E_{ox} = E(0^-) = E(0^+)\frac{\epsilon_s}{\epsilon_{ox}} = \frac{q N_A}{\epsilon_{ox}} X_{d0}}$$

MOS in TE: Quantitative Analysis



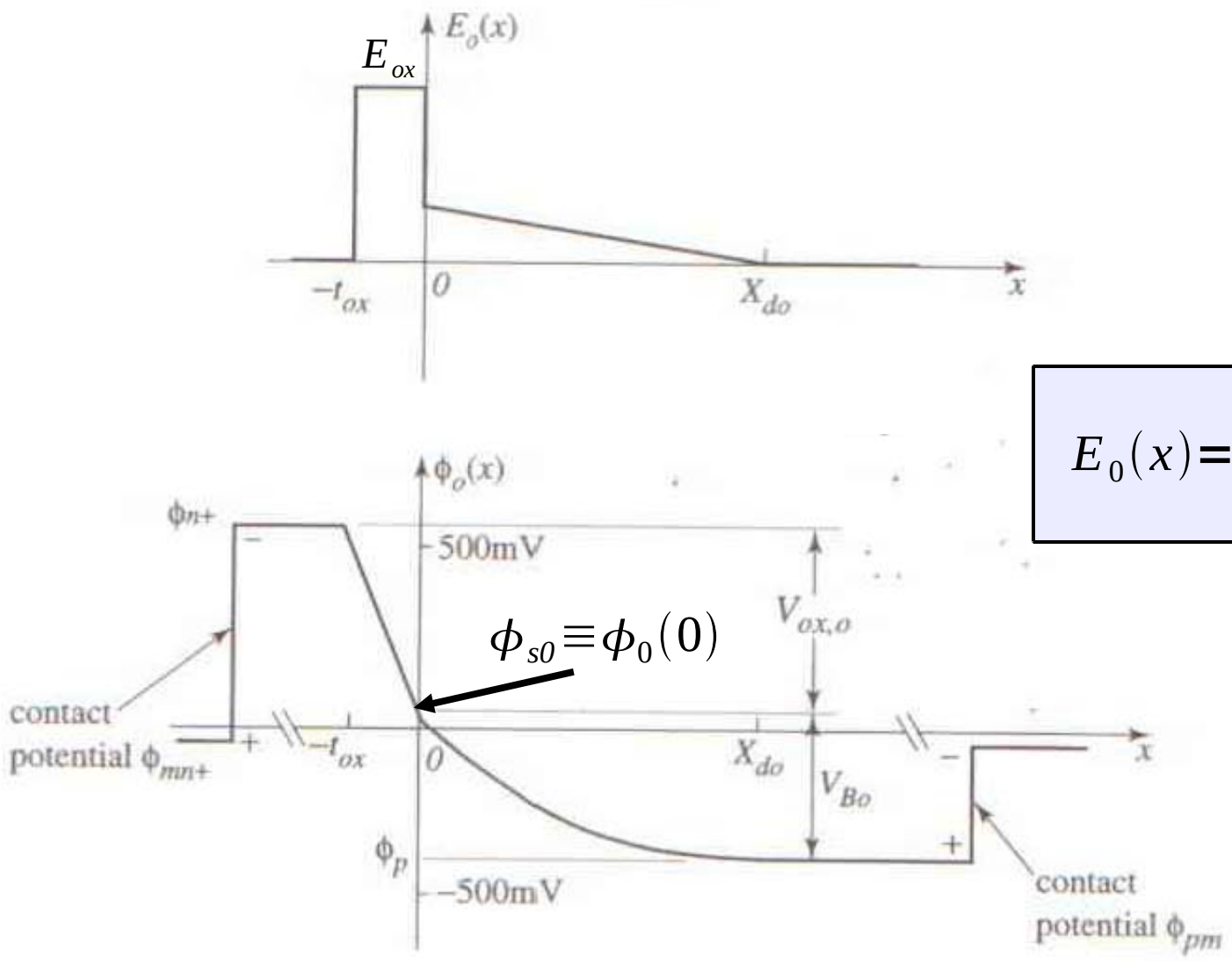


Within the same material the electric field will not jump !

- Just for the sake of double-checking the correctness of the previous result let's also apply the boundary condition at the interface between gate and oxide and see if we get the same result

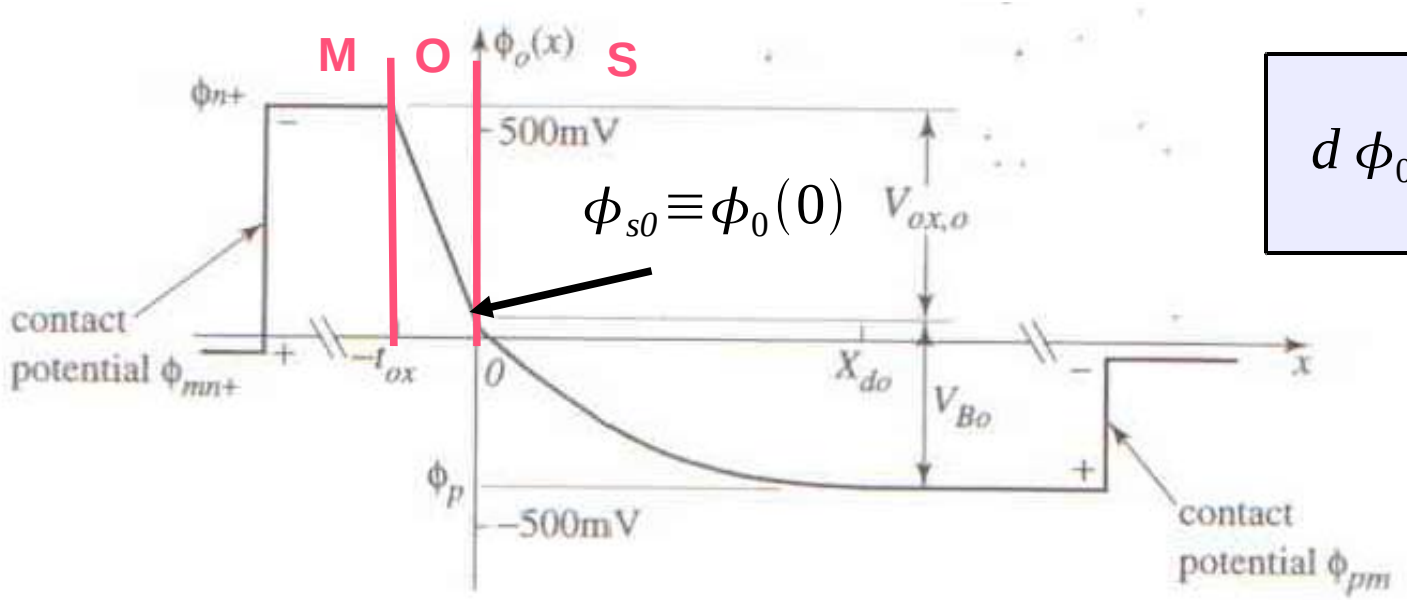
$$\epsilon_G \cdot E(-t_{ox}^-) + \mathbb{Q}_G = \epsilon_{ox} E(-t_{ox}^+) \rightarrow \underbrace{E(-t_{ox}^+)}_{=E_{ox}} = \frac{\mathbb{Q}_G}{\epsilon_{ox}} = \frac{-\mathbb{Q}_B}{\epsilon_{ox}} = \frac{q N_A X_{d0}}{\epsilon_{ox}}$$

MOS Potential in TE



$$E_0(x) = -\frac{d\phi_0(x)}{dx}$$

MOS in TE: Potential in the oxide



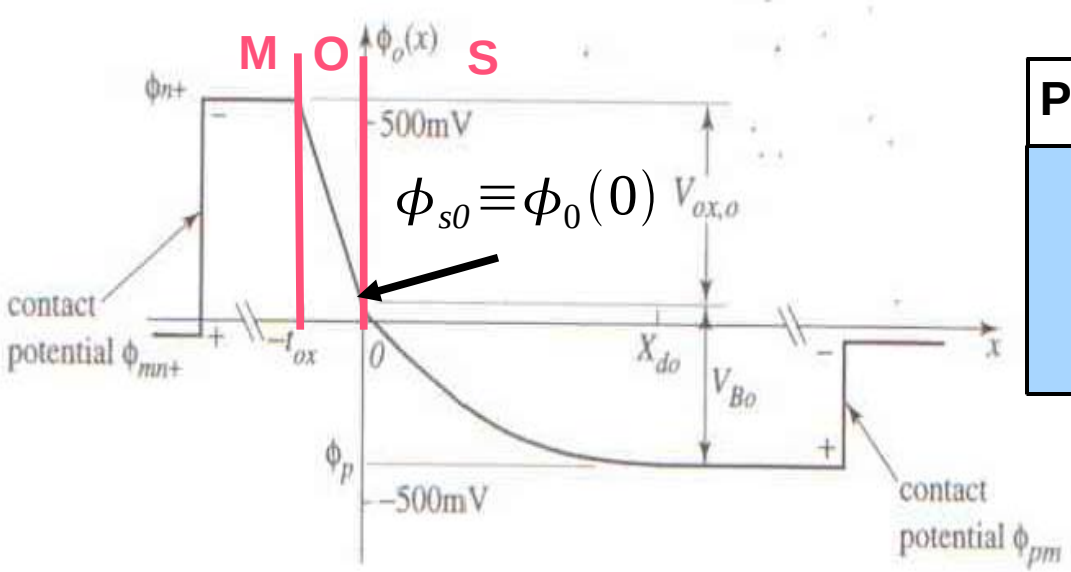
$$d\,\phi_0(x) = -E_0(x)\,dx$$

$-t_{ox} < x < 0$:

$$\phi_0(x) - \phi_{n+} = \int_{-t_{ox}}^{x} -E_{ox}\,dx = -\frac{q N_A X_{d0}}{\epsilon_{ox}} \int_{-t_{ox}}^{x} dx = -\frac{q N_A X_{d0}}{\epsilon_{ox}} (x + t_{ox})$$

Potential in the oxide	
for $-t_{ox} < x < 0$:	$\phi_0(x) = \phi_{n+} - \frac{q N_A X_{d0}}{\epsilon_{ox}} (x + t_{ox})$

MOS in TE: Potential in the oxide



Potential in the oxide

for $-t_{ox} < x < 0$:

$$\phi_0(x) = \phi_{n+} - \frac{q N_A X_{d0}}{\epsilon_{ox}} (x + t_{ox})$$

Surface Potential (Potential at the oxide/silicon interface)

$$\phi_{s0} \equiv \phi_0(0) = \phi_{n+} - \frac{q N_A X_{d0}}{\epsilon_{ox}} t_{ox} = \phi_{n+} - \frac{q N_A X_{d0}}{\mathbb{C}_{ox}}$$

with $\mathbb{C}_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$

Voltage drop across the oxide

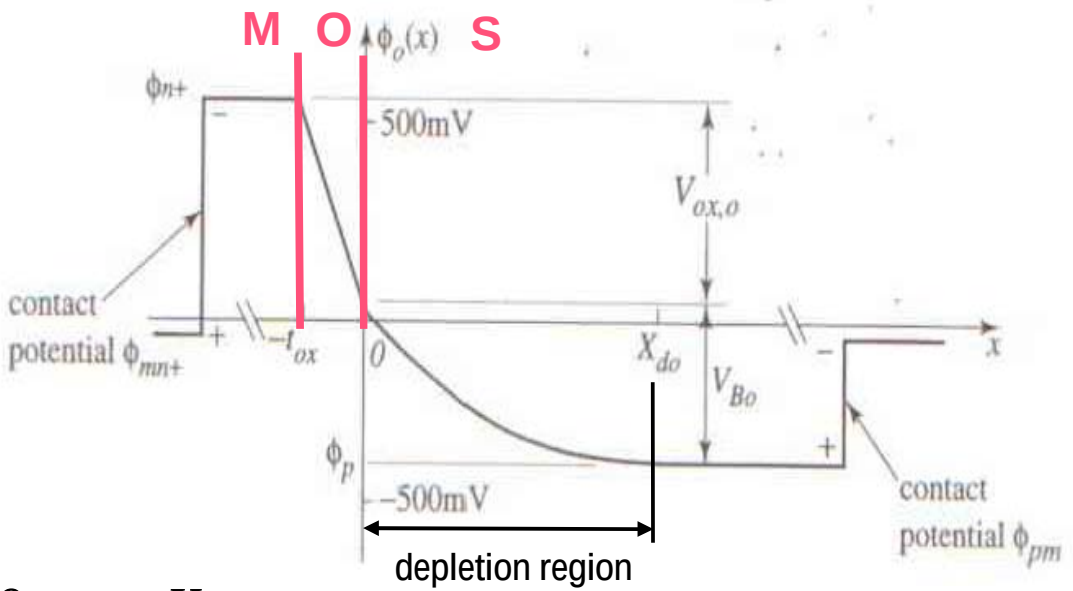
$$V_{ox,0} \equiv \phi_0(-t_{ox}) - \phi_0(0) = \phi_{n+} - \phi_{s0} = \frac{q N_A X_{d0}}{\mathbb{C}_{ox}} = \frac{\mathbb{Q}_{G0}}{\mathbb{C}_{ox}}$$

with:

$$\mathbb{Q}_{G0} = -\mathbb{Q}_{B0} = q N_A X_{do}$$

NOTE: $V_{OX,0}$ is proportional to the charge stored on each side of the oxide

MOS in TE: potential in the depletion region in the silicon substrate



$$dE_0(x) = \frac{\rho(x)}{\epsilon_s}\,dx$$

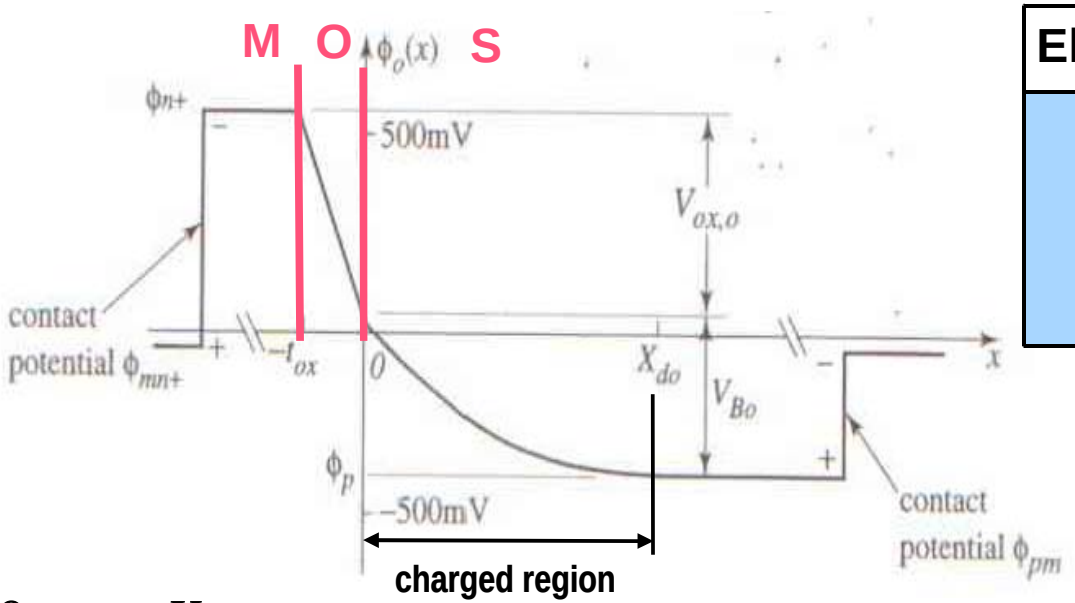
$0 < x < X_{d0}$:

$$\int_{E_0(0+)}^{E_0(x)} dE_0(x) = \int_{0+}^{x} \frac{\rho(x)}{\epsilon_s} \longrightarrow E_0(x) - E_0(0^+) = \int_{0+}^{x} \frac{-qN_A}{\epsilon_s}\,dx = \frac{-qN_A x}{\epsilon_s} \longrightarrow$$

$$E_0(x) = E_0(0^+) - \frac{qN_A x}{\epsilon_s} = \frac{qN_A X_{d0}}{\epsilon_s} - \frac{qN_A x}{\epsilon_s} = \frac{qN_A}{\epsilon_s}\,(X_{do} - x) \longrightarrow$$

$$E_0(0^+) = \frac{qN_A X_{d0}}{\epsilon_s}$$

MOS in TE: potential in the depletion region in the silicon substrate



Electric Field in the Depletion region

for $0 < x < X_{d0}$:

$$E_0(x) = \frac{qN_A}{\epsilon_s}(X_{d0} - x)$$

$$d\phi_0(x) = -E_0(x)\,dx$$

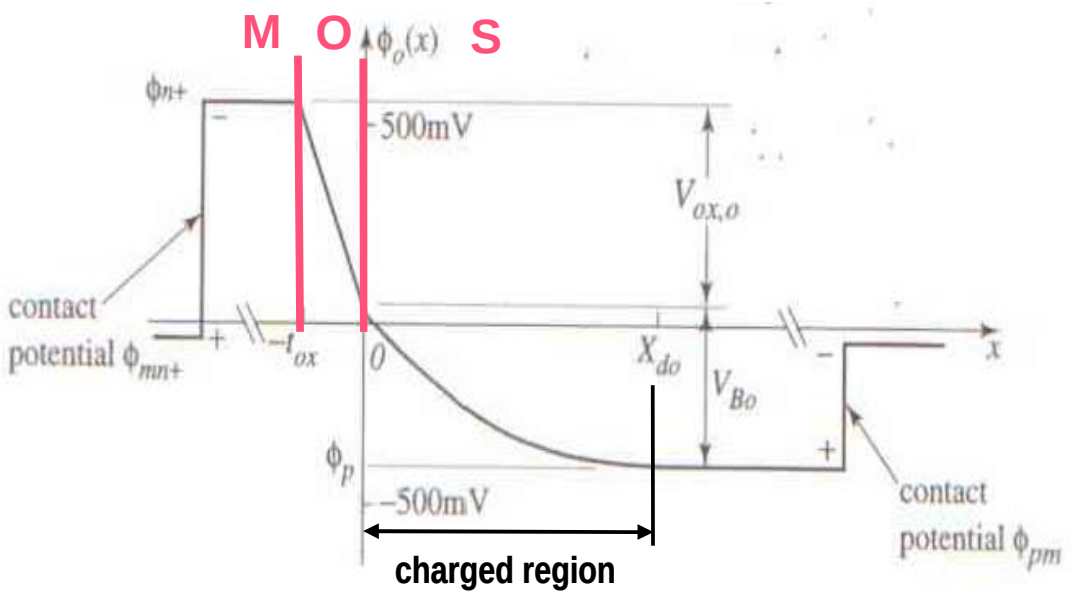
$0 < x < X_{d0}$:

$$\int_{\phi_0(0)}^{\phi_0(x)} d\phi_0(x) = \int_0^x -E_0(x)\,dx \longrightarrow \phi_0(x) - \phi_0(0) = \int_0^x -\frac{qN_A}{\epsilon_s}(X_{do} - x)\,dx \longrightarrow$$

$$\phi_0(x) - \phi_0(0) = -\frac{qN_A}{\epsilon_s} X_{do} \int_0^x dx + \frac{qN_A}{\epsilon_s} \int_0^x x\,dx = -\frac{qN_A}{\epsilon_s}\left(X_{do}\,x - \frac{x^2}{2}\right) \longrightarrow$$

$$\phi_0(x) = \phi_0(0) - \frac{qN_A}{\epsilon_s}\left(X_{do}\,x - \frac{x^2}{2}\right) \longrightarrow$$

MOS in TE: potential in the depletion region in the silicon substrate



Surface Potential

$$\phi_{s0} \equiv \phi_0(0) = \phi_{n+} - \frac{q N_A X_{d0}}{\mathbb{C}_{ox}}$$

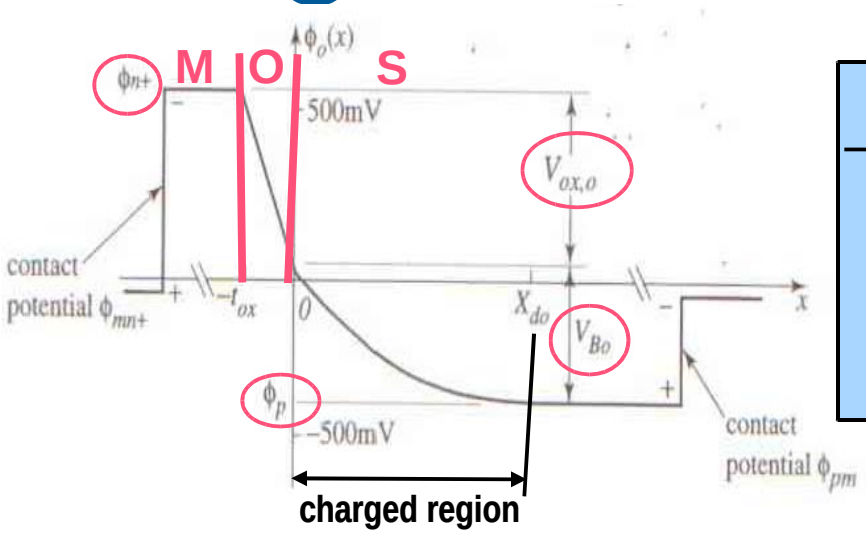
$$0 < x < X_{d0} : \qquad \phi_0(x) = \phi_0(0) - \frac{qN_A}{\epsilon_s}\left(X_{do}\, x - \frac{x^2}{2} \right)$$

Potential in the depletion region in the substrate

for $0 < x < X_{d0}$:

$$\phi_0(x) = \left(\phi_{n+} - \frac{q N_A X_{d0}}{\mathbb{C}_{ox}} \right) - \frac{qN_A}{\epsilon_s}\left(X_{do}\, x - \frac{x^2}{2} \right)$$

MOS in TE: potential in the depletion region in the silicon substrate



Potential in the depletion region in the substrate

for $0 < x < X_{d0}$:

$$\phi_0(x) = \phi_{n+} - \frac{q N_A X_{d0}}{\mathbb{C}_{ox}} - \frac{qN_A}{\epsilon_s}\left(X_{do}\,x - \frac{x^2}{2}\right)$$

$$\phi_0(X_{d0}) \equiv \phi_p = \phi_{n+} - \frac{q N_A X_{d0}}{\mathbb{C}_{ox}} - \frac{qN_A}{2\epsilon_s} X_{do}^2$$

This must be the voltage drop across the charged region of the silicon substrate

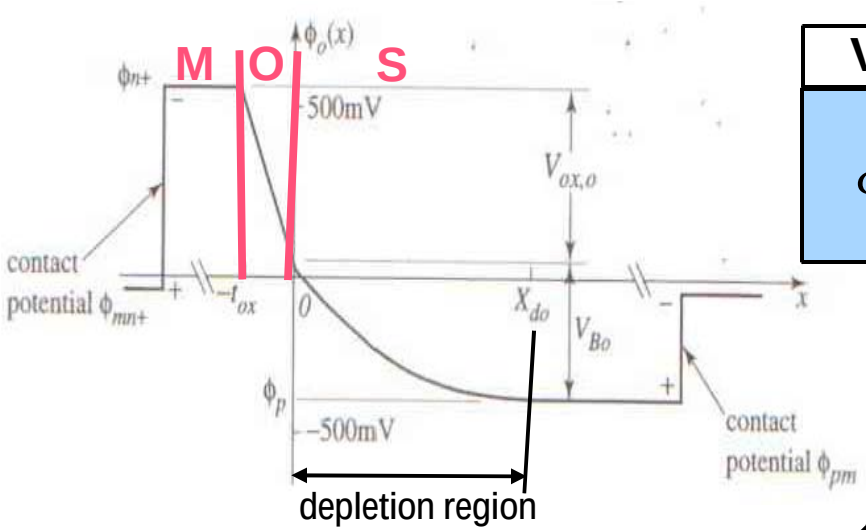
$$= V_{B0}$$

Voltage drop across the MOS structure	$\phi_{n+} - \phi_p = \frac{q N_A X_{d0}}{\mathbb{C}_{ox}} + \frac{qN_A}{2\epsilon_s} X_{do}^2$

Since this is the voltage drop across the oxide

$$= V_{ox,0}$$

MOS in TE: Width of the Depletion region



Voltage drop across the MOS structure

$$\phi_{n+} - \phi_p = V_{ox,0} + V_{B0} = \frac{q N_A X_{d0}}{\mathbb{C}_{ox}} + \frac{q N_A}{2\epsilon_s} X_{do}^2$$

Voltage drop across the oxide

$$V_{ox,0} = \frac{q N_A X_{d0}}{\mathbb{C}_{ox}} = \frac{\mathbb{Q}_G}{\mathbb{C}_{ox}} = \frac{-\mathbb{Q}_B}{\mathbb{C}_{ox}}$$

Voltage drop across the charged region of the silicon substrate

$$V_{B0} = \frac{q N_A}{2\epsilon_s} X_{do}^2$$

$$\frac{q N_A}{2\epsilon_s} X_{do}^2 + \frac{q N_A X_{d0}}{\mathbb{C}_{ox}} - (\phi_{n+} - \phi_p) = 0$$

$$X_{do}^2 + \frac{q N_A}{\mathbb{C}_{ox}} \frac{2\epsilon_s}{q N_A} X_{d0} - \frac{2\epsilon_s}{q N_A}(\phi_{n+} - \phi_p) = 0 \longrightarrow X_{do}^2 + \frac{2\epsilon_s}{\mathbb{C}_{ox}} X_{d0} - \frac{2\epsilon_s}{q N_A}(\phi_{n+} - \phi_p) = 0$$

MOS in TE: Width of the Depletion region

$$X_{do}^2 + \frac{2\epsilon_s}{\mathbb{C}_{ox}} X_{d0} - \frac{2\epsilon_s}{q N_A}(\phi_{n+} - \phi_p) = 0$$

$$ax^2 + bx + c = 0 \longleftrightarrow x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

NOTE: X_{d0} can be only positive

$$X_{do} = \frac{-2\epsilon_s/\mathbb{C}_{ox} \pm \sqrt{(4\epsilon_s^2/\mathbb{C}_{ox}^2) + (8\epsilon_s/q N_A)(\phi_{n+} - \phi_p)}}{2} =$$

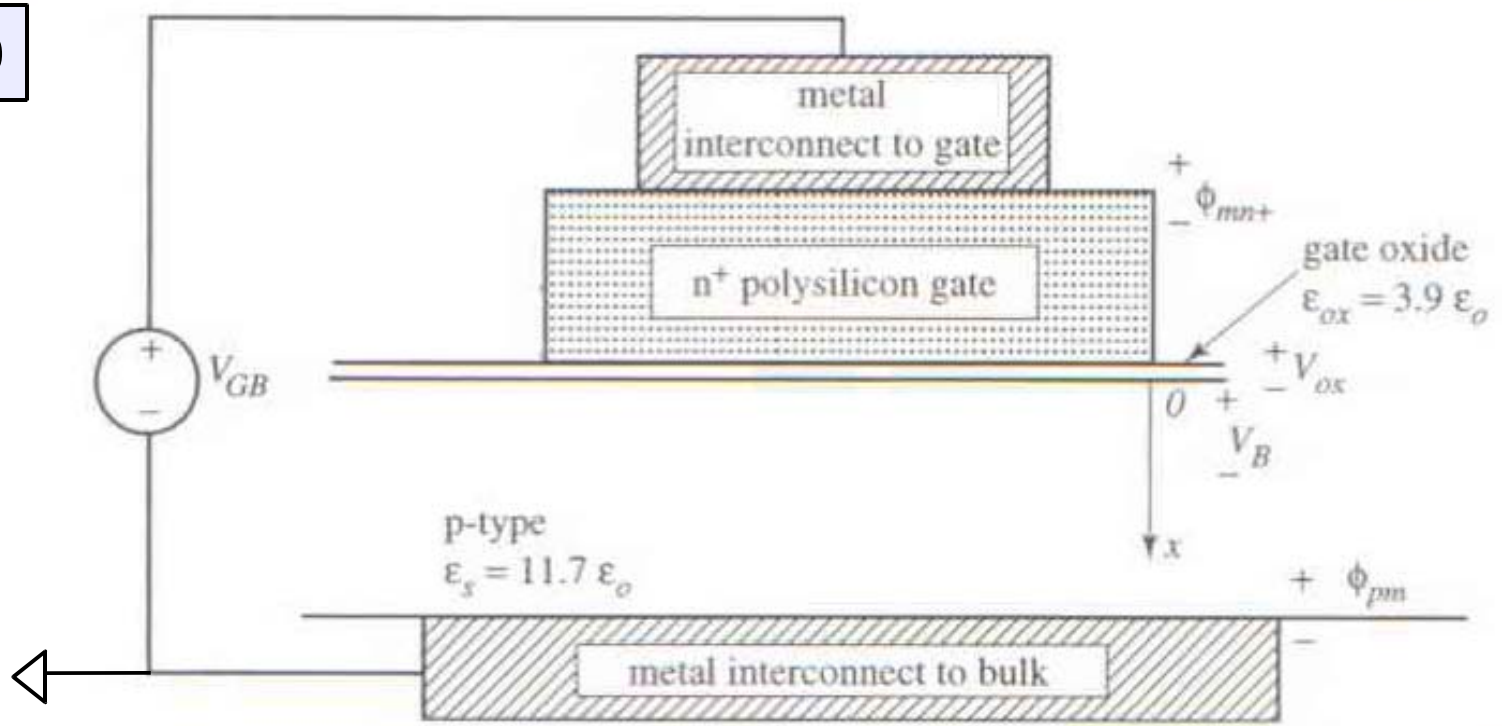
$$= -\epsilon_s/\mathbb{C}_{ox} + \sqrt{(\epsilon_s^2/\mathbb{C}_{ox}^2) + (2\epsilon_s/q N_A)(\phi_{n+} - \phi_p)} = \frac{\epsilon_s}{\mathbb{C}_{ox}} \left(-1 + \sqrt{1 + \frac{2\epsilon_s}{q N_A} \frac{\mathbb{C}_{ox}^2}{\epsilon_s^2}(\phi_{n+} - \phi_p)} \right)$$

Depletion Width:

$$X_{do} = \frac{\epsilon_s}{\mathbb{C}_{ox}} \left(\sqrt{1 + \frac{2\mathbb{C}_{ox}^2}{q N_A \epsilon_s}(\phi_{n+} - \phi_p)} - 1 \right)$$

MOS under Bias

$V_{GB} \neq 0$



➤ **Figure 3.30** MOS capacitor on a p-type substrate for one-dimensional analysis of charge distribution ρ(x), electric field E(x), and potential ϕ(x) for the case of an applied bias V_{GB}.

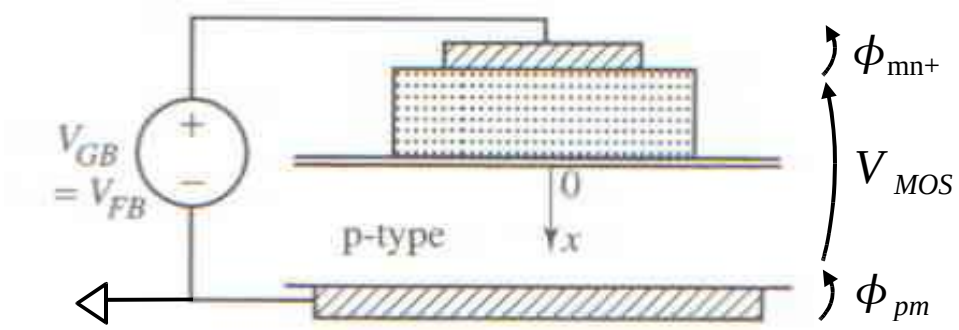
(FLATBAND) – ACCUMULATION – DEPLETION – (THRESHOLD) – INVERSION

Flatband

- We apply a gate to bulk voltage that is opposite to the built-in potential. This special voltage bias is called flat-band voltage

$V_{FB} \equiv -\phi_{\text{BUILT\_IN}} = -(\phi_{\text{n+.0}} - \phi_{p.0})$	Flat-band Voltage

NOTICE:
For an MOS structure with n+ poly-silicon gate and p-type substrate this voltage is negative



$$V_{GB} = \phi_{\text{mn+}} + \phi_{pm} + V_{MOS}$$
$$\downarrow$$
$$V_{GB} = -\phi_{\text{BUILT-IN}} + V_{MOS}$$
$$\downarrow$$
$$V_{GB} = V_{FB} + V_{MOS}$$
$$\downarrow$$

The bulk metal contact is considered fixed $\longrightarrow$ $\phi_p = \phi_{\text{p,0}}$

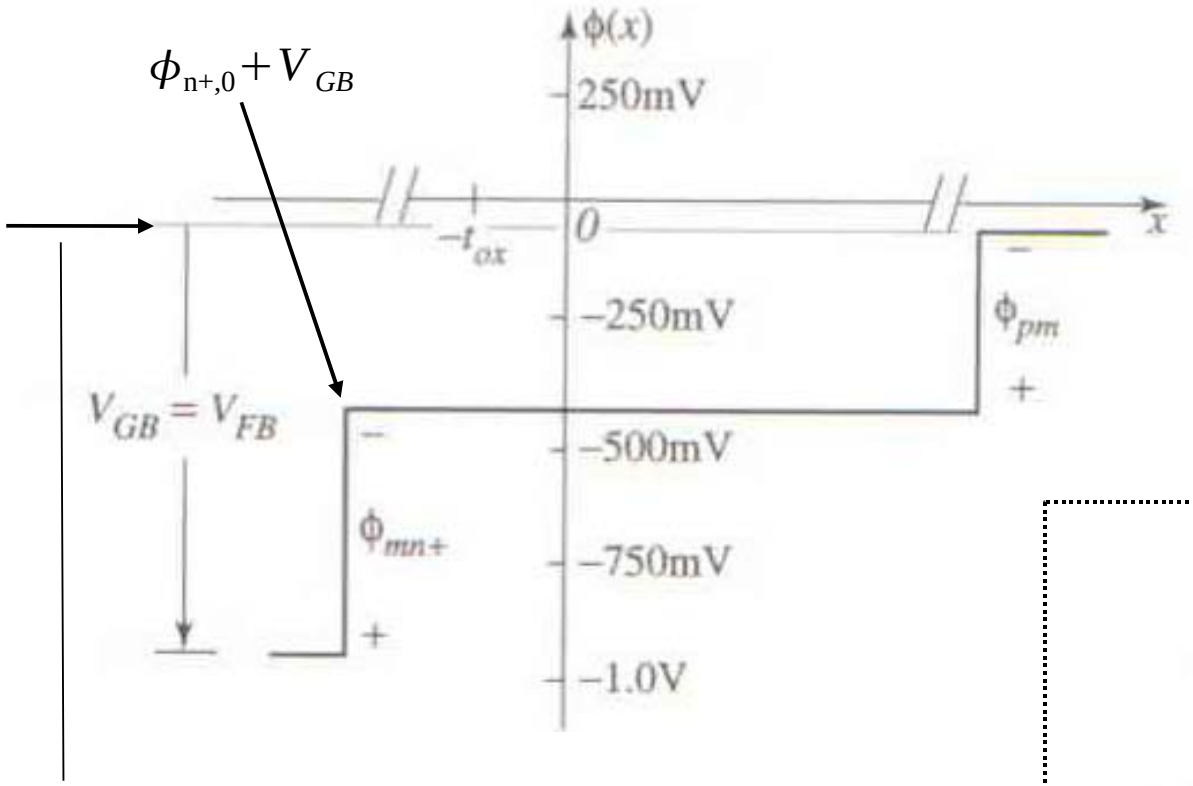
$$\phi_{\text{n+}} = \phi_{\text{n+,0}} + V_{GB}$$

$$\phi_{\text{n+}} - \phi_p = \phi_{\text{n+,0}} + V_{GB} - \phi_p =$$
$$= \phi_{\text{n+,0}} - \phi_{\text{p,0}} + V_{GB} = -V_{FB} + V_{GB}$$

$$if \quad V_{GB} = V_{FB} \rightarrow V_{MOS} = 0$$

Flatband

- In flat-band condition (V_{GB}=V_{FB}) there is no internal voltage drop across the MOS capacitor.

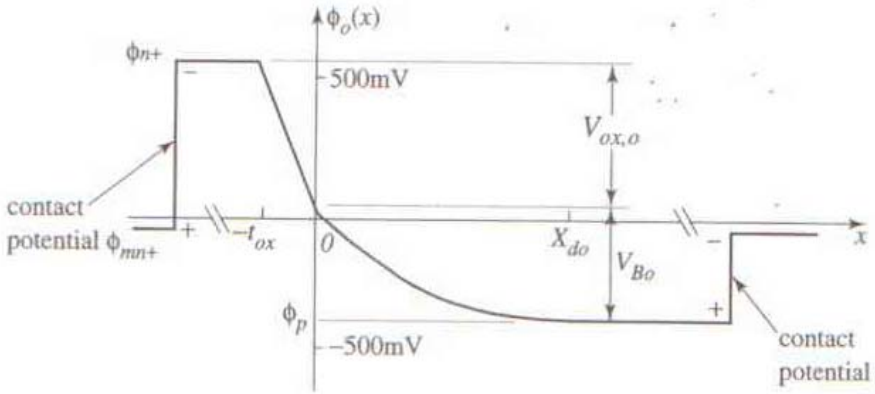


The bulk metal contact is considered fixed

ϕ_p = – 420 mV ($\phi_{n+,o}$ = 550 mV)

Applying V_{GB} = V_{FB} shifts the gate metal contact lower by – 970 mV (=V_{FB})

Thermal Equilibrium



Flatband

- Since in flat-band condition (V_{GB}=V_{FB}) there is no internal voltage drop across the MOS capacitor, as a result the electric field is zero and the gate charge density is zero

$$Q_G(V_{GB}=V_{FB})=0$$