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CAPACITATED NETWORKS AND THEIR APPLICATION TO ELECTRICAL NETWORKS/CIRCUITS

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Abstract

In an electrical network/circuit we know that current flows in a closed circuit and every component has some capacity. We now define some standard concepts in this connection and formulate them in terms of labels and finally apply these to electrical networks/circuits. We define an operation on graphs which results in realizing a capacitated network as a combination of two graphs. In this paper we have shown how theorem 1 on capacitated network finds its natural application in electrical network/circuit (theorem 1.1), of course a large number of definitions have to be introduced for this purpose, this is the price we have to pay. All new/modified definitions are underlined. A generalized electrical network version of theorem 1 is theorem 1.2 applicable to electrical networks with more than one source and one sink. We apply theorem 1.1 to an electrical network/circuit obtained by translating a capacitated network graph. We translate an electrical network/circuit to its corresponding capacitated network and verify theorem 1. We have demonstrated how theorem 2 when applied to electrical network (theorem 2.1) becomes so obvious and clear. A generalized version of theorem 2 is theorem 2.2 applicable to electrical networks/circuits with more than one switch.

Key Words : *Capacity function, Feasible flow, Cutset, Labeled flow, Labeled feasible flow.*

Section 1

1. Introduction

We have studied and defined concepts required for translating a graph to its corresponding electrical network/circuit and recovering the graph for a given circuit. For this purpose we have defined some new concepts in graph theory so as to uniquely represent a graph by a circuit and conversely. In this paper we look at concepts and results in graph theory which are directly applicable to electrical network/circuit. The present work is on translating these concepts and results to the corresponding ones in electrical circuit theory. In this connection we found that the capacitated network along with some theorems are directly applicable to electrical network/circuit.

This paper is organized into 6 sections. In section 2 we recall some definitions from standard books on graph theory and electrical network/circuit along with some important results and then we formulate these in terms of labels which is section 3. In section 4 we apply these definitions to electrical network/circuit. In section 5 we apply these concepts and results on the capacitated/ labeled network to electrical network/circuit followed by the conclusion in section 6.

In this paper for practical purposes labeled graphs are treated quite differently from their usual treatment in graph theory and hence many definitions seems to be similar but are necessary for applications. We state the difference and similarity between the usual treatment and our treatment of graph theory as and when needed. We also note here that in the usual definition of the labeled graphs[3], the labels are just symbols assigned to edge/vertex of a graph but this is not of practical use, specially in electrical circuit theory. Here labels of a graph are defined to be either integers or rational numbers.

Section 2

Definition 2.1 Capacity function [5] : Let $D = (V, E)$ be a digraph, then a mapping $C_E : E \to R$ is called an edge capacity/labeled function. The value $C_E(e)$ is called the edge capacity/label of the edge 'e'. Similarly a mapping $C_v(v) : V \to R$ is called a vertex capacity/labeled function. The value $C_V(v)$ is called the vertex capacity/label of the vertex 'v'. The difference between edge/vertex capacity of a digraph and labels of a digraph is only in the range of the above mapping, while the range of the usual

labels are symbols, the range of the capacity are mostly integers and rational numbers though here we have taken the range as entire R. Further note here that the usual labels can be defined on any graphs but capacity is only defined for directed graphs. To differentiate between a capacity and a labeled function we denote the labeled functions on edge /vertex by L_E/L_V.

Definition 2.2 Capacitated network [5] : A diagraph $(D, C_E)/(D, C_V)$ is called an edge/vertex capacitated network.

A diagraph $\{D, C_E, C_V\}$ is called a mixed capacitated network. Again note here that these are labeled graphs.

Note : We always denote a diagraph by $D = (V, E)$ and the corresponding undirected graph $G = (V, E)$.

Definition 2.3 Edge/Vertex flow [5] : A real valued function $f_E : E \to R$ is called an edge flow function and the value $f_E(e)$ is called the edge flow along the edge 'e'. Similarly a real valued function $f_V : V \to R$ is called a vertex flow function and the value $f_V(v)$ is called the vertex flow at the vertex 'v'.

Note : We have defined two function $C_E(e)$ and $f_E(e)$ on the edge 'e'. $C_E(e)$ is the numerical value that can be associated with edge e and $f_E(e)$ represents the actual value associated with the edge e, satisfying the condition $0 \leq f_E(e) \leq C_E(e)$. An example to see the difference between the capacity and flow on a lighter side is to observe that the capacity(weight) of a six foot tall person say is 70 kgs but the actual flow(actual weight) may be less or more. Let us illustrate the concepts of capacity and flow by the following example.

Consider a capacity flow network (D, C_E, f_E)

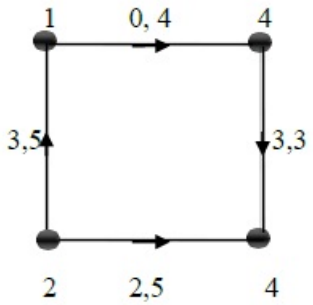

Figure – 1: A capacity flow network

In the above example we see that each edge is associated with two real numbers separated by a comma. The first number indicates the flow along the edge and the second number indicates the edge capacity. The value $C_E(e)$ (capacity of the edge (1,2)) = 5 and the value $f_E(1,2)$ (flow of the edge (1,2)) = 3. Here $C_E(1,2)$ indicates that the edge has a capacity of 5 units on which 3 units flow. Similar explanation holds for other edges of the graph.

From the above example we see that the capacity edge flow network (D, C_E, f_E) can be realized as a combination of two graphs namely an edge flow network digraph and an edge labeled graph as shown in the figure below

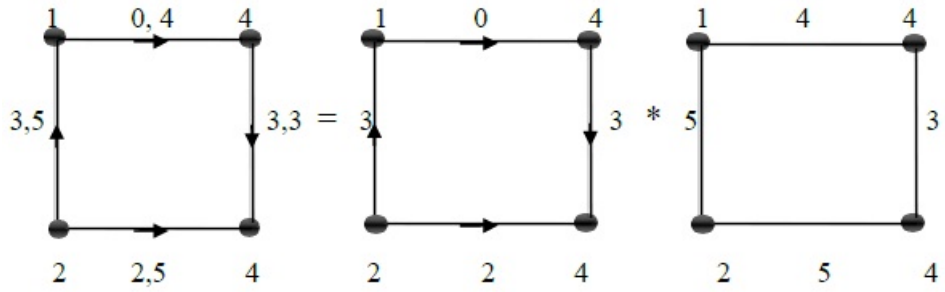

Figure – 2: Capacity edge flow graph as combination of two graphs

This combination is defined by the following rule $(D, C_E, F_E) = (D, f_E) * (G, L_E)$ where '$*$' is defined by $(f_E * L_E) = (f_E, L_E)$, where G is the undirected graph corresponding to the directed graph D and L_E is the edge labeled function on the edge set E. Similarly a vertex flow network (D, C_V, F_V) is a combination of a capacity vertex flow network digraph and a vertex labeled graph. In general this combination is defined by the rule $(D, C_V, F_V) = (D, f_V) * (G, L_V)$ where '$*$' is defined by $(f_V * L_v) = (f_V, L_v)$. This is illustrated in the following example.

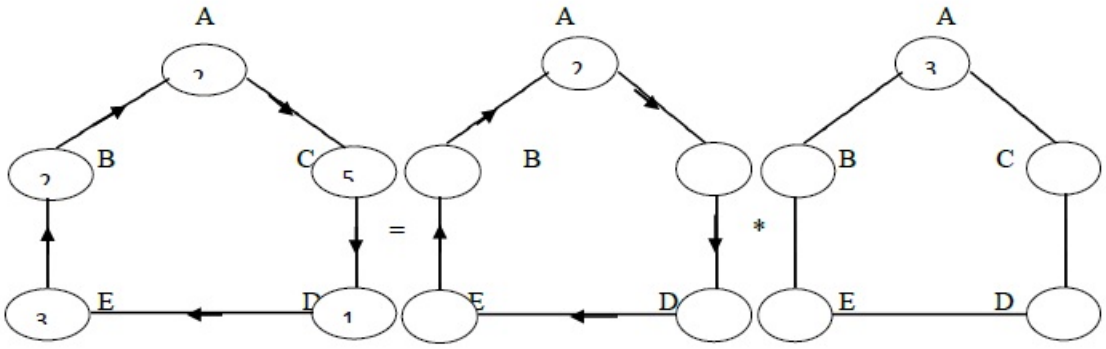

Figure – 3 : Capacity vertex flow graph as combination of two graphs

Here we see that the value $C_V(A)$ (capacity of the vertex A) $= 3$ and the value $f_V(A)$ (flow at the vertex A) $= 2$. The value $C_V(A)$ indicates that the vertex has a capacity of 3 units where as $f_V(A)$ indicates the actual value (Flow at vertex A) is 2 units. Similar explanation hold good for all other vertices of the graph.

Definition 2.4 Source and sink [5] : A vertex in a capacitated network with indegree zero is called a source and the vertex with outdegree zero is called the sink. Observe that the indegree and outdegree are defined only for digraphs. For our purpose we give new definition for these in terms of labels in section 3.

Definition 2.5 Inflow/Outflow [5] : The sum of the flows along all the edges directed to vertex 'i' /directed from a vertex 'i' is called inflow/outflow respectively.

i.e Inflow $= \sum_{e \to i} f(e)$ and Outflow $= \sum_{i \to e} f(e)$.

Definition 2.6 Feasible Flow [5] : A flow in a network is called a feasible flow if the inflow is equal to the outflow. If f is a feasible flow in a capacitated network G, the value $f(G)$ of the flow is the outflow from the source.

Definition 2.7 Edge Cutset [5] : In an edge capacitated network $G = (V, E)$, a subset $(S, T) = \{(i, j)/(i, j) \in E,\ i \in S, j \in T\}$ is called an edge cutest if

(i) S, T are partition of V

(ii) Source is in S and sink is in T

(iii) There is no flow from source to sink if all the edges of the cutset are deleted from G.

Definition 2.8 Capacity of the edge cutset [5] : The edge capacity of the edge cutset (S,T) is denoted as $C_E(S,T)$ and defined by $C_E(S,T) = \sum_{e\in(S,T)} f_E(e)$.

Definition 2.9 Flow of an edge cutset [5] : The flow of an edge cutset (S,T) is denoted as $f_E(S,T)$ and defined by $f_E(S,T) = \sum_{e\in(S,T)} f_E(e)$.

Definition 2.10 Vertex cutset [5] : Let (D, C_v) be a vertex capacitated network. A subset W of V is called a vertex cutset if

(i) W does not contain source and sink

(ii) there is no flow from source to sink if all the vertices of the cutset are deleted from G.

Definition 2.11 Capacity of the vertex cutset [5] : The vertex capacity of the vertex cutset W is denoted as $C_V(W)$ and defined by $C_V(W) = \sum_{v\in W} C_V(v)$.

Definition 2.12 Flow of a vertex cutset [5] : The flow of a vertex cutset W is denoted as $f_v(W)$ and defined by $f_v(W) = \sum_{v\in(W)} f_v(v)$.

Section 3

In order to study electrical network through graphs we redefine these definition in terms of labels (though some of these were used earlier).

Definition 3.1 Dummy labeled Edge/ Vertex capacity function : Let $G = (V, E)$ be a graph, a mapping $L_E : E \to R$ is called a dummy edge labeled capacity function. The value. $L_E(e)$ is called the dummy labeled edge capacity of the edge 'e'.

Observe here that the capacity function C_E is the dummy labeled function L_E, while $C_E(e)$ is the actual capacity of the edge 'e', $L_E(e)$ is the dummy label of 'e.

Similarly let $G = (V, E)$ be a graph, a mapping $L_V : V \to R$ is called a dummy vertex labeled capacity function. The value $L_v(v)$ is called the dummy labeled vertex capacity at the vertex 'v'.

Note : This definition is needed in electrical circuit theory. We note here that the value $L_E(e)$ and $L_v(v)$ (dummy edge/vertex label) is not the actual label. It only indicates the maximum label that can be assigned to an edge/vertex which is a real number. We

again observe here that in case of ordinary labeled graphs an edge/vertex is labeled at random . Hence dummy labeled and labels are synonymous.

Definition 3.2 Dummy labeled capacitated network : A diagraph $(D, L_E)/(D, L_V)$ is called dummy edge/vertex labeled capacitated network. **A diagraph $\{D, L_E, L_V\}$ is called a mixed dummy labeled capacitated network.**

Definition 3.3 Labeled Edge/ Vertex flow : A real valued function $f_{LE} : E \to R$ is called an edge labeled flow function and the value $f_{LE}(e)$ is called the labeled edge flow along the labeled edges. Similarly a real valued function $f_{LV} : V \to R$ is called a vertex labeled flow function and the value $f_{LV}(v)$ is called the labeled vertex flow at the labeled vertex 'v'.

Note : We observe that the value $f_{LE}(e)$ and $f_{LV}(v)$ are the actual value associated with the labeled edge 'e' and the labeled vertex 'v'. For example $L_E(e) = 5$ and $f_{LE}(e) = 3$. The value 5 represents the dummy label of the labeled edge e where as 3 represents its actual label. In the case of usual graph, labels and dummy labels are synonymous as noted early, however for a multi labeled graphs the two labels may be different. If $L_E(e) = 5$ and $f_{LE}(e) = 3$ then we can say that the edge e is multi labeled with labels 3 and 5. For application purpose we consider an edge with two labels, one of them is called the capacity of the edge e and other is called the flow along the edge e.

Definition 3.4 Labeled Inflow/ Outfolw : In a dummy labeled capacitated network the sum of all the labeled flow directed to a vertex 'v'/directed from a vertex 'v'f is called labeled inflow/outflow respectively.

Note : The difference between the sum of the indegree at a vertex 'v' and sum of the labels on these edges at a vertex 'v' is explained by the following example

Figure – 4

From the above example we see that the indegree of the vertex A is 3 (figure - 4 (a)) and the labeled indegree of the vertex A is 7 (figure - 4(b)).

Definition 3.5 (a) Labeled Indegree/Outdegree : **The sum of all the labels on the edges incident with/incident away from a vertex 'v' is called labeled indegree/outdegree**. Labeled indegree and outdegree are defined for digraphs.

Definition 3.5 (b) Labeled feasible flow : A labeled flow is called feasible if $\sum_{e \to v} f(e) = \sum_{v \to e} f(e)$, where vertex v is neither source nor sink.

Definition 3.6 Labeled edge cutest : In a dummy labeled edge capacitated network $G = V, E, L_E$, a subset $(S, T) = \{(i, j)/(i, j) \in E, i \in S, j \in T\}$ is called a labeled edge cutest if

(i) S, T are partition of V

(ii) Source is in S and sink in T

(iii) There is no flow from source to sink if all the labeled are deleted from G.

Definition 3.7 Capacity of the labeled edge cutest : The capacity of the labeled edge cutset (S, T) is denoted by $L_E(S, T)$ and defined by $f_{LE}(S, T) = \sum_{e \in (S,T)} f_{LE}(e)$.

Definition 3.8 Flow of a labeled edge cutset : The flow of a labeled edge cutset (S, T) is denoted as $f_{LE}(S, T)$ and defined by $f_{LE}(S, T) = \sum_{e \in (S,T)} f_{LE}(e)$.

Definition 3.9 Labeled vertex cutset : Let (D, L_v) be a labeled vertex capacitated network. A subset W of V is called a labeled vertex cutset if there is no flow from source to sink if all the labeled vertices of the cutset are deleted from G.

Definition 3.9 Capacity of the labeled vertex cutset : The capacity of the labeled vertex cutset W is denoted as $L_V(W)$ and defined by $L_V(W) = \sum_{v \in W} L_V(v)$. If f is a labeled feasible flow in a dummy labeled capacitated network G then the value $L(G)$ is the outflow from the source.

Definition 3.10 Flow of a labeled vertex cutset : The flow of a labeled vertex cutset (W) is denoted as $f_{LV}(W)$ and defined by $f_{LV}(W) = \sum_{v \in W} f_{LV}(v)$.

Section 4

In this session we first recall some classical definition of electrical networks/ circuits from standard book along with new definition. We apply the definitions from session 3

to electrical network/circuit.

Definition 4.1 Circuit board (CB) : A circuit board is a board on which electronic components can be used to construct an electronic device. The two major kinds of circuit board(CB) are

1. Bread Board (BB)

2. Printed Circuit Boards (PCB).

Definition 4.1 : (a) Bread board (BB) : BB [2] are simple boards which have only terminals which can be used to connect electronic devices. BB is used to make temporary circuit for testing a designed circuit/network. Such boards are also called proto boards.

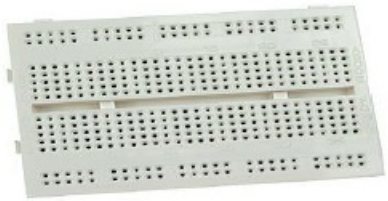

Figure- 5: Bread Board

Definition 4.1 (b) Printed Circuit board (PCB) : A simple PCB [1] is a plastic board which has connecting tracks between terminals.

The PCB's are of two types

- The PCB's which has no embedded components is called Printed Wiring Board. In these boards the printed connecting pathways are marked with the capacity of the components that may be used to built a network/circuit.

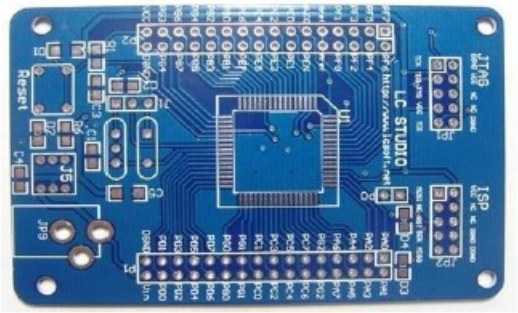

Figure - 6 : A printed wiring board

- The PCB populated with electronic components is called a Printed Circuit Assembly(PCA). In these board the printed connecting pathways are labeled with the capacity of the components are equipped with the electronic component with specified capacity.

Figure – 7: A printed circuit assembly(PCA)

We have defined dummy labeled edges and vertices earlier. We now define these terms in electrical network/circuit.

Definition 4.2 A non labeled PCB : A simple PCB without any electrical component or any indication on the interconnection between two terminals is called a non labeled PCB. Such a PCB, looks like an usual graph as shown in figure 8.

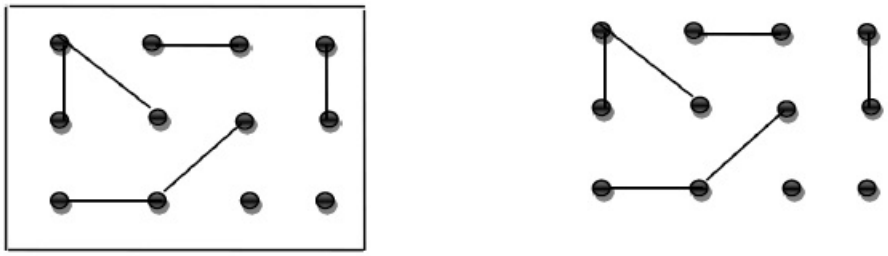

Figure - 8 : A non labeled PCB and its graph

Definition 4.3 Dummy labeled PCB : In a PCB, sometimes there is an indication on the interconnection between the terminals about the capacity of the electrical equipments to be used. In this case the graph is dummy labeled graph.

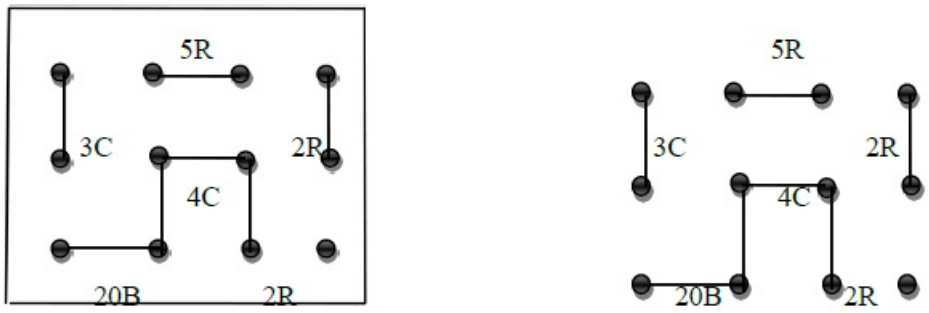

Figure - 9 : A labeled PCB and its graph

In a PCB the interconnection between the terminals are equipped with a electrical component of the specified capacity. Such a PCB is called a printed circuit assembly (PCA) [2]. The graph corresponding to a PCA is called an edge labeled graph . Each edge of the graph has two labels one indicating capacity of the interconnection and the other indicating the capacity of the component. Sometimes the edge labeled graphs has three labels. The first label indicating the capacity of the interconnection, the second indicating the presence of the electrical component(either 0 or 1)and the third indicating the capacity of the component as shown in the figure -10.

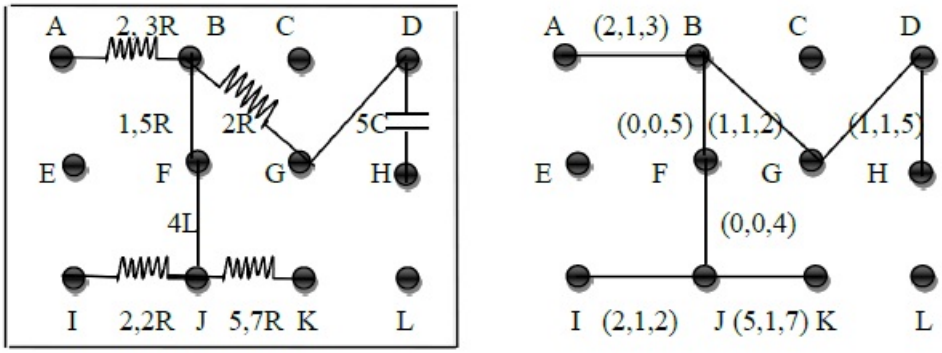

Figure – 10 : A PCA and its graph

Definition 4.4 Dummy edge/vertex capacity function (In electrical network) : In a PCB there are interconnecting tracks that are labeled with numbers (usually integer or real number). The number on the tracks indicates the capacity of the electrical component to be used along the track (edge).

A function E_{cE} : edgeset of the PCB $\rightarrow R$ is the dummy edge capacity function and the value $E_{CE}(e)$ is the capacity of the track (edge).

A function Ec_V : Vertex set of the PCB $\rightarrow R$ is the dummy vertex capacity function and the value $Ec_V(v)$ is the capacity of the junction (vertex).

Note : We note here that the value $E_{CE}(e)$ and $Ec_V(v)$ is not the actual label. $Ec_E(e)$ indicates the maximum capacity of the electrical component that can be assigned between the terminals of the circuit, which is a real number. $Ec_V(v)$ indicates the maximum potentials at the terminals of the circuit.

Definition 4.5 Dummy labeled capacitated network (In electrical network) : A PCB equipped with electrical components is called a dummy labeled capacitated network.

Definition 4.6 Source and Sink(In electrical circuit) : All electrical networks/circuit are energized with dc voltage(battery). The positive terminal of the battery is designated as source and the negative terminal is designated as sink.

Definition 4.7 Edge/vertex flow(In electrical circuit) : When a PCB is energized with dc voltage supply there is flow of current through the circuit. This current flow in the circuit is due to the potential difference between the terminals. Thus there is a real number associated with the terminals of the circuit. An edge flow in a closed network

refers to current (i.e Flow of electrons). Mathematically a flow/current is a function i_E : edge set of a PCB $\rightarrow R$. The value $i_E(e)$ is the current across the track (edge 'e'). A vertex flow in a closed network refers to the potentials at the terminals.
Mathematically its a function P_V : vertex set of a PCB $\rightarrow R$. The value $P_V(v)$ is the potential at the terminal (vertex 'v') of the circuit.
Note : i_E and P_v are the actual values indicating the flow/current along the edge and the potential at the vertex.
Definition 4.8 Inflow/Outflow (In electrical circuit) : The total current entering/leaving a junction (node) is called inflow/outflow in a network.
Definition 4.9 A feasible flow (In electrical circuit) : A feasible flow in a circuit refers to Kirchhoff current law (KCL).
[KCL[2] : The law states that the sum of currents entering a node is equal to sum of currents leaving from that node].
Definition 4.10 Edge cut in an electrical circuit : Let us consider a PCB equipped with electrical components. Let a set V be set of terminals of the PCB and the set E be set of electrical components that are equipped between the terminals of the PCB.
A subset $(S,T) = \{(i,j)/(i,j) \in E, i \in S, j \in T\}$ is called an edge cut, set if

(i) S,T are partitions of V

(ii) Source is in S and sink is in T

(iii) There is no flow from source to sink if all the electrical components from the set (S,T) are removed.

Definition 4.11 Capacity of the edge cutest (In electrical circuit) : The capacity of the edge cutset (S,T) is denoted by $C_E(S,T)$ and defined by $C_E(S,t) = \sum_{e \in (S,T)} Ec_E(e)$.
Definition 4.12 Flow of the edge cutset (In electrical circuits) : The total flow of current through all the edges in the edge cutset (S,T) is called the flow of the edge cutset.
Definition 4.13 Vertex cut in an electrical circuit : In a PCB let E represents the set of electrical components and V represents set of terminals. The removal of terminals

(vertices) from $T \subset V$ (other than source and sink), resulting in no current/flow in the circuit is called vertex cut.

Definition 4.14 Capacity of the vertex cutest (In electrical circuit) : The capacity of the edge cutset T is denoted by $C_v(T)$ and defined by $C_v(T) = \sum_{v \in T} Ec_v(v)$.

Definition 4.15 Flow of the vertex cutset (In electrical circuits) : The total flow of current across all the vertices in the vertex cutset T is called the flow of the vertex cutset.

Section 5

In this session we see that how some theorems of capacitated network and cutsets find their natural application to electrical networks/circuits. Here we verify the theorem by taking a capacitated network graph and represent its corresponding electrical circuit .

Theorem 1[5] : If f is feasible flow in a capacitated network G and if (S, T) is any cut in the network, $f(G) = f(S, T) - f(T, S)$.

Proof : The vertex set is $V = \{1, 2, 3, \cdots, n\}$, S is any set of vertices that contains vertex 1 (the source) and T is its compliment that contains vertex n (the sink). Notice that $\sum_j f(i,j) - \sum_j f(j,i)$ is $f(G)$ when $i = 1$. So $\sum_{i \in S} \sum_j f(i,j) - \sum_{i \in S} \sum_j f(j,i) = f(G)$. If i and j are both in S, the term $f(i,j)$ appears in the first summation $\sum_{i \in S} \sum_j f(i,j)$ as well as in the second summation $\sum_{i \in S} \sum_j f(j,i)$. So it is enough if we let the subscript j vary for all j in T. Hence $\sum_{i \in S} \sum_j f(i,j) - \sum_{i \in S} \sum_j f(j,i) = f(G)$.

Let us verify theorem 1 by taking an example of a capacitated network graph.

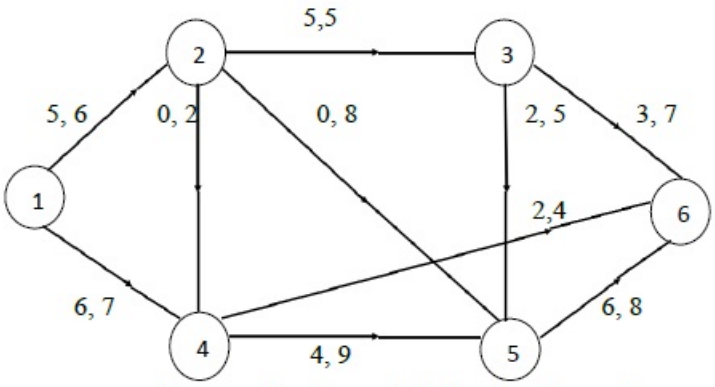

Figure - 11 : Capacitated network graph

Let $V = \{1, 2, 3, 4, 5, 6\}$ be the vertex set of the graph. Let vertex 1 be the source and vertex 6 be the sink. Let $S = \{1, 4, 3\}$ and $T = \{2, 5, 6\}$ be the two partitions of the vertex set V and (S, T) be the cutset of the graph. In this network each edge is associated with two values, the flow value $f_E(e)$ and the capacity value $C_E(e)$.
Flow calculations for the capacitated network graph (figure -11):
The total flow from the source

$$f(G) = 5 + 6 = 11. \tag{1}$$

The total inflow into the sink

$$3 + 2 + 6 = 11. \tag{2}$$

From equations 1 and 2 we observe that

$f(G)$ = the total outflow from the source = the total inflow into the sink.

For the cutset (S, T), the flow $f(S, T) = 5 + 4 + 2 + 3 + 2 = 16$ and for the cutset (T, S) the flow $f(T, S) = 0 + 5 = 12$.
Let us consider the equation

$$f(S, T) - f(T, S) = 16 - 5 = 11. \tag{3}$$

From equations 1 and 3 we observe $f(G) = f(S, T) - f(T, S)$.
Hence verifying theorem 1.
In general theory of capacitated network, capacity and flow along the edges are not important and hence the difference between these two is sense to be artificial. But when we apply this to electrical networks/ circuits the difference becomes predominant and is extremely important. We first formulate theorem 1 in terms of electrical networks and also translate the capacitated network in figure 11 to electrical networks/circuits and see how the theorem holds. In this connection we observe that

(1) Flow along an edge refers to flow of current between two terminals (potential difference between the two terminals).

(2) Capacity of the edge refers to the maximum flow of current along the edge.

(3) The actual capacity flow of current depends on the electrical components used(resistance).

(4) While the general capacitated network can be thought of as two labeled edges, the electrical network is multi-labeled. Further while the capacitated network is not vertex labeled it is so in electrical network. For simplicity of understanding we consider networks with two labeled edges and verify the electrical network theorem as stated below.

The electrical network version of theorem 1.

Theorem 1.1 : A printed circuit assembly (PCA) with a cutset (S, T), the total flow of current from the source is equal to the difference in the total flow of current along the electrical components in the cutset (S, T) and in the cutset (T, S).

Proof : The proof of the theorem is on same lines as of theorem 1.

Note : The condition in the theorem that the flow 'f' should be feasible is automatically satisfied by Kirchhoff current law in a PCB.

We now demonstrate the verification of the theorem 1 by constructing the circuit for the capacitated network graph (figure 11).

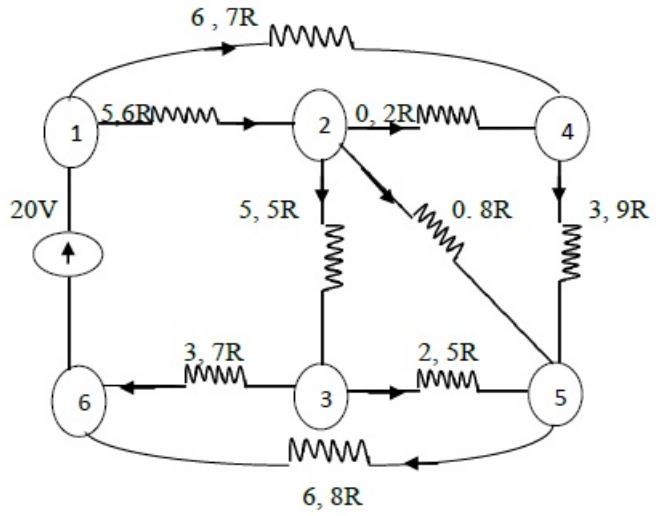

Figure – 12: The electrical circuit for the capacitated network graph(figure 11)

The electrical networks/circuits are energized by a voltage supply. For the network/circuit let us consider the positive terminal of the voltage supply as source and negative terminal as the sink. The terminals of the circuit are defined as the set $V = \{1, 2, 3, 4, 5, 6\}$.

Let $S = \{1, 2, 4\}$ and $T = \{3, 5, 6\}$ be the two partitions of the set V with a cutset (S, T).

Current / Flow calculations for an electrical network (figure 12) :

The total current /outflow from the source

$$f(G) = 5 + 6 = 11. \tag{4}$$

The total current/ inflow into the sink

$$3 + 2 + 6 = 11 \tag{5}$$

From equations 4 and 5 we observe that

$f(G)$ **= the total current/ outflow from the source = the total current/ inflow into the sink.**

For the cutset (S, T), the current/flow $f(S, T) = 5 + 0 + 3 + 3 = 11$ and for the cutset (T, S) the current / flow $f(T, S) = 0$.

Let us consider the equation

$$f(S, T) - f(T, S) = 11 - 0 = 11. \tag{6}$$

From equations 4 and 6 we observe $f(G) = f(S, T) - f(T, S)$. Thus verifying the theorem 1.1.

Let us consider a simple series - parallel circuit, construct its corresponding capacitated network graph and then verify theorem 1.1 for this graph.

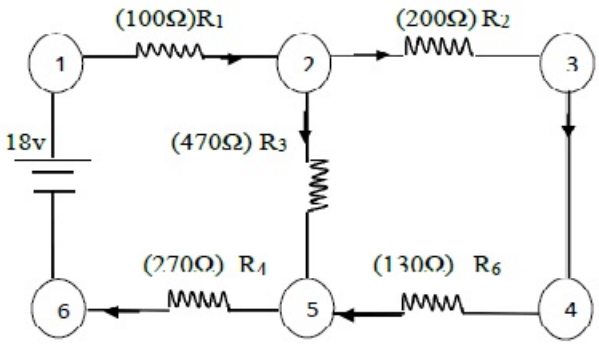

Figure - 13: A series – parallel circuit

The capacitated network graph for the above circuit is as shown in figure 14.

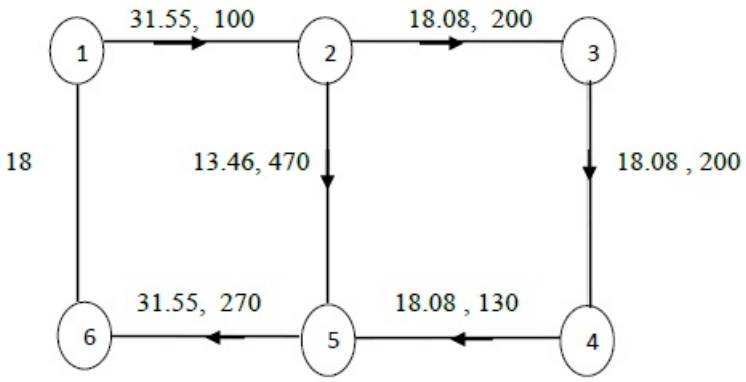

Figure -14 : Capacitated network graph

Let $V = \{1, 2, 3, 4, 5, 6\}$ be the set of terminals of the circuit. Let $S = \{1, 2, 4\}$ and $T = \{3, 5, 6\}$ be the two partitions of the set V with a cutset (S, T).

From the circuit we observe the total current / outflow from the source $f(G) = 31.55$ and the total current / inflow into the sink = 31.55.

Current / Flow calculations for an electrical network (figure 14) :

The total current/flow $f(S, T)$ along the branches (edges) in the cutset (S, T), $f(S, T) = 18.08 + 13.46 + 18.08 = 49.62$.

The total current/ flow $f(T, S)$ along the branches (edges) in the cutset (T, S) $f(T, S) = 18.08$.

Consider $f(S, T) - f(T, S) = 49.62 - 18.08 = 31.55$.

Thus we observe $f(S, T) - f(T, S) = f(G)$. Thus verifying the theorem 1.1.

Note : In theorem 1 we consider a capacitated network with one source and one sink, however the theorem can be generalized to multi source and multi sink capacitated network graphs. We observe here that normally that any electrical network has more one source of power and one source of sink. Let us consider an electrical network / circuit with two source and two sink.The corresponding graph for such an electrical network/circuit can be separated into two capacitated network graphs and we see that theorem 1 holds for these network graphs.

The generalized version of theorem 1 when applied to a general electrical network /circuit having multi - source and multi sink is as follows.

Theorem 1.2 : An electrical network with more than one source and one sink can be separated into two electrical networks and in each network theorem 1.1 holds. The proof of the above theorem is similar to the proof of theorem 1.

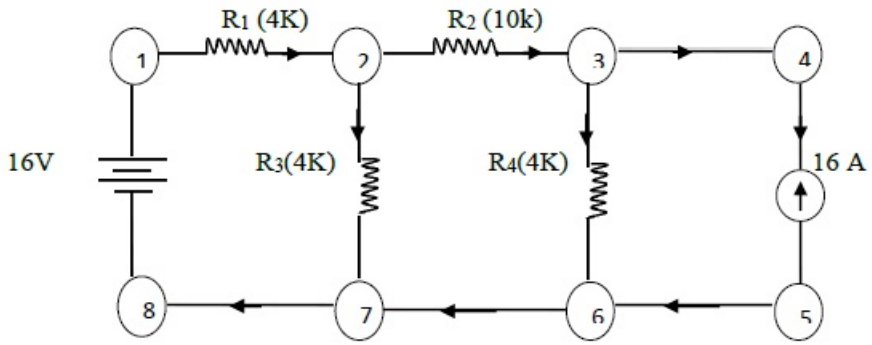

Figure – 15 : An electrical circuit with two voltage supply

Figure 15 represents a circuit with two voltage sources. We can see that the given circuit with two sources and sinks can be represented as two separate capacitated network graphs as shown in figure 16 and figure 17.

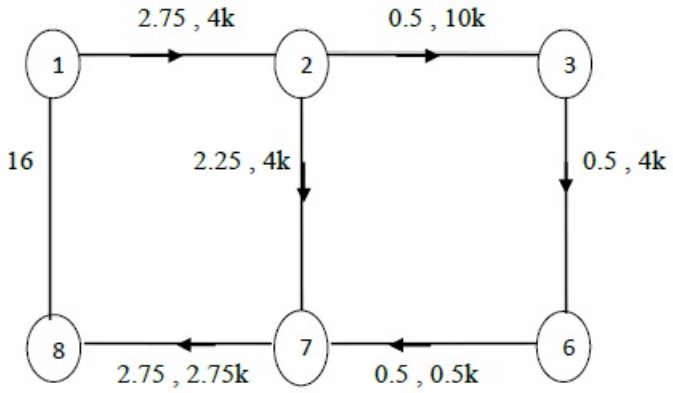

Figure – 16 : A capacitated network graph with one voltage source

The set of terminals is $V = \{1, 2, 3, 6, 7, 8\}$ with vertex 1 as source and vertex 8 as sink. Let $S = \{1, 2, 4\}$ and $T = \{3, 5, 6\}$ be two partition of V with cutsets (S, T) and (T, S). The total flow for the cutset (S, T) is $f(S, T) = 0.5 + 2.25 + 0.5 = 3.25$ and the total flow for the cutset (T, S) is $f(T, S) = 0.5$.

Therefore $f(S, T) - f(T, S) = 3.25 - 0.5 = 2.75 = f(G)$. Thus verifying theorem 1.

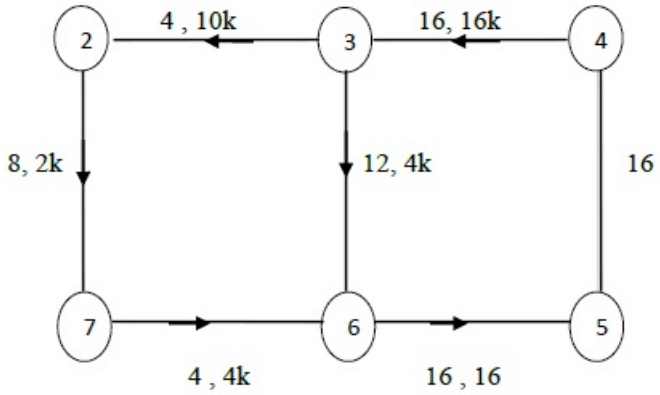

Figure – 17 : Capacitated network graph with other voltage source

The set of terminals for the capacitated network graph is $V = \{4, 2, 3, 7, 6, 5\}$ with vertex 4 as source and vertex 5 as sink. Let $S = \{4, 2, 7\}$ and $T = \{3, 6, 5\}$ be two partition of V with cutsets (S, T) and (T, S). We have $f(S, T) = 16 + 8 = 24$ and $f(T, S) = 4 + 4 = 8$. We have $f(S, T) - f(T, S) = 24 - 8 = 16 = f(G)$. Hence theorem 1.

Now let us consider another theorem in graph theory and look at its application in electrical circuits.

Theorem 2[4] : A vertex W in a connected graph G is a cutvertex if and only if there exists two vertices X and Y in G such that every path between X and Y passes through W.

Let us verify this theorem by taking an example of a simple connected graph G.

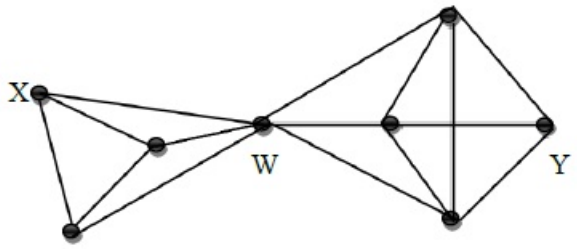

Figure -18 : A connected graph G

From the figure we observe that all the paths from the vertices X and Y passes through the vertex W. Thus if the vertex W is deleted all the edges incident on W are also deleted. Thus clearly we see that vertex W is a cutvertex.

Let us interpret the theorem 2 in terms of electrical circuits and see how the theorem holds.

A switch is an electrical component that can make or break an electrical circuit interrupting the current or diverting it from one conductor to another. The mechanism of a switch removes or restores the conducting path in a circuit when it is operated. Most electronic circuit contains an on/off switch . in addition to on/off switches many circuits contains switches that controls how a circuit works or activates different features of a circuit. A simple on/off switch that connects or disconnects the two terminals when the switch is closed the two terminals are connected and currents flows between them (figure 19). When the switch is opened the terminals are not connected so current does not flow (figure 20).

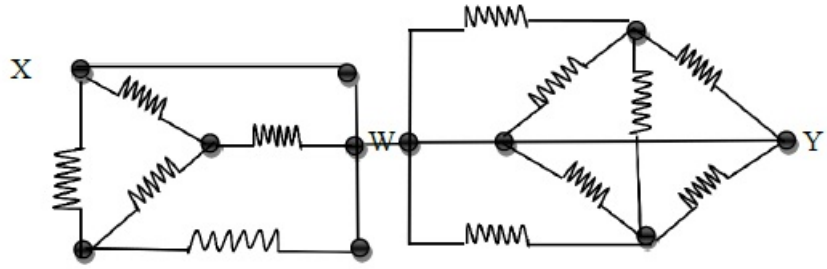

Figure - 19 : A closed circuit

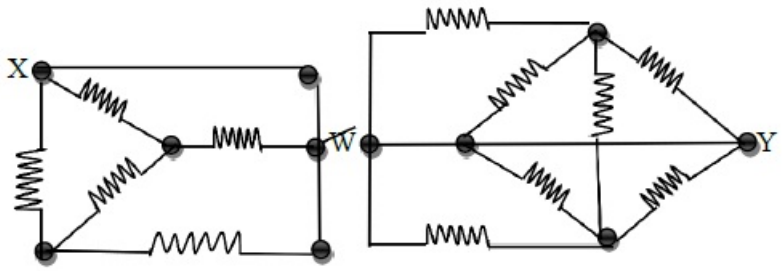

Figure - 20 : A open circuit

Here we see that in an electrical network/circuit a switch in off mode acts as a cutvertex disconnecting all the paths from source to sink and when in on mode there is a flow of current through out the circuit from source to the sink.

The electrical version of theorem 2.

Theorem 2.1 : An electrical network has a switch if and only if every links between two terminals passes through the switch.

The proof of the above theorem is obvious when an electrical network contains only one switch.

Note : For an electrical network with multi switches the set of all switches is a cutset and all the interlinks between two terminals passes through these switches.

The generalized version of theorem 2.

Theorem 2.2 : A set of vertices W in a connected graph G is a cutset if and only if every vertex of W is a cutvertex.

(or)

A set of vertices is a cutset in a connected graph G is a cutvertex set if and only if there exists two vertices x and y such that every path between them passes through every vertex in the cutset.

The proof of the above theorem is obvious.

Conclusion

From this work it can be seen that the capacitated networks in graph theory is directly applicable to electrical networks/circuits. We have demonstrated this for theorem 1. Several other theorems in capacitated network can be interpreted in terms of electrical

networks/circuits. Vertex flow is not dealt with in capacitated networks but in the analysis of electrical network, the flow at a vertex is very important and is interpreted as the potential at the terminals. Hence the numerical difference between the flow at the terminals in an electrical circuit is the flow of current along the interlink between the terminals. This allows us to study Ohm's law, Kirchhoff's law in terms of capacitated networks. We can even formulate new electrical laws. Further, while a capacitated network has only one source and one sink, the electrical networks has multi-sources and multi-sinks. Though they can be separated into capacitated networks containing one source and one sink, in fact theorem 1 can be generalized to networks having more than one source and one sink. Our future work is in this direction.

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