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Media Group

Solder Impurities: How Much is Too Much? p. 38

CIRCUITS ASSEMBLY

The Journal for Surface Mount and Electronics Assembly®

MAY 2007

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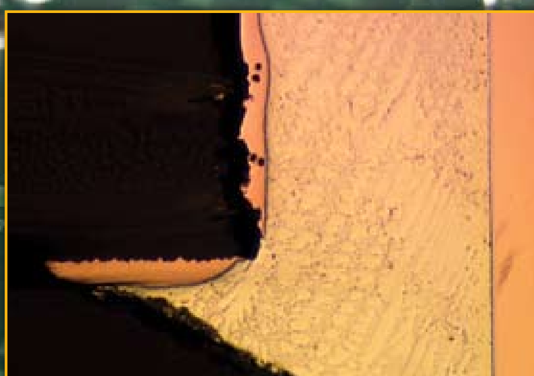
Shortcomings of SAC Alloys

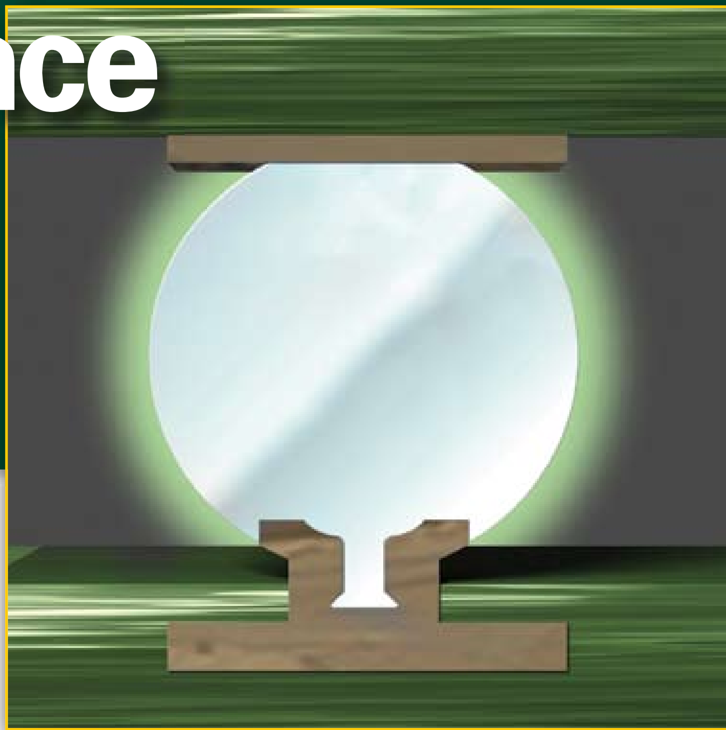
An IBM-Celestica Joint Study on Copper Dissolution

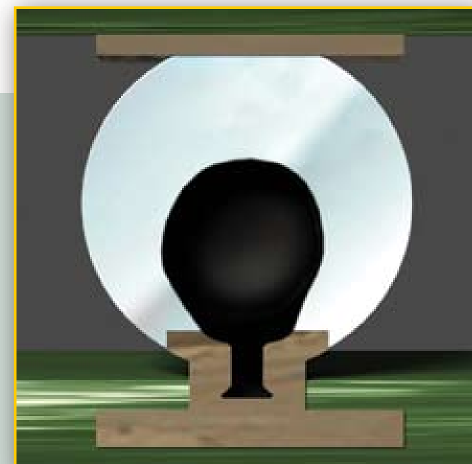


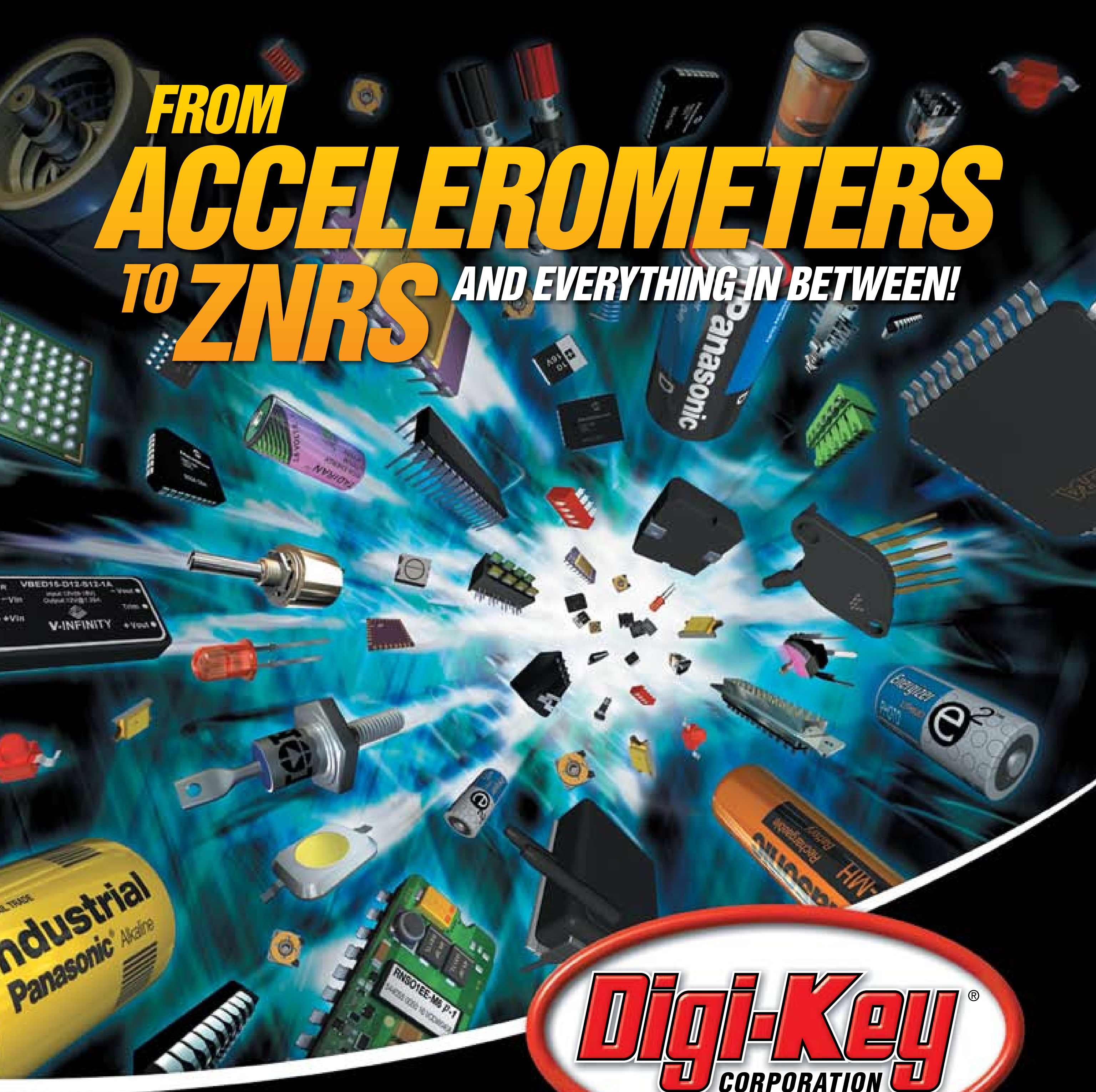
Tomorrow's Testing Techniques

The Newest Package: Chiplets

NPI Methodologies



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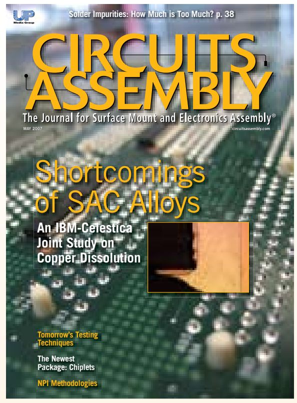
CIRCUITS ASSEMBLY

MAY 2007 – Vol. 18 No. 5



Photos courtesy IBM and Celestica

ON THE COVER: SAC alloy use has been tied to increased copper dissolution.

FIRST PERSON

MONEY MATTERS

TECH TALK

FEATURES

ONLINE at PCDandM.com

DEPARTMENTS

Shot Down?

North America has made a hearty meal out of U.S. defense budgets over the past several years, but it wasn't always this way.

Back in the old days – the 1990s – manufacturers bolted from the military supplier ranks. Working as a DoD subcontractor was too onerous, too paperwork-laden, and, in the wake of utterly remarkable demand for telecom equipment, not profitable. In the wake of the recession, industry eyes turned back to the one market guaranteed not to go to Asia. Solid returns and the promise of future contracts led to a surge in interest not seen since the late 1980s. Building for the military metamorphosized from wallflower to belle of the ball. Companies hustled to obtain military certifications – and the contracts that followed. The current administration and Congress were eager enablers, funding staggering Defense budgets for everything from next-generation warfare systems to replacements for gear and munitions spent in Iraq and Afghanistan. Flush with new programs, military suppliers have enjoyed three straight years of double-digit growth.

The U.S. funds more than half – $522 billion – of global defense spending. National defense contracts are typically closed to foreign suppliers, making the U.S. a lucrative and virtually protected market for U.S. companies. But defense spending tends to be administration-dependent, and the tide may be turning. As reported on circuitsassembly.com in March, analyst Ed Henderson predicts military electronics growth will slow to 2.3% next year, down from 9.5% this year. This is a sharp drop from the 11.4% to 13.3% growth rates from 2004 to 2006.

In its latest proposal, the U.S. Defense Department asked Congress for more than $28.1 billion in funding for fiscal 2008. The monies would support electronics procurement and research for what is known in Washington parlance as CET&I, or communications, electronics, telecom and intelligence technologies. While $28 billion is a lot of government cheese, it's also a 4% drop from fiscal 2007, and many observers cite as reasons a changed climate in Washington, plus other fiscal priorities both chronic (retirement and medical programs) and acute (Hurricane Katrina aid).

And although the drop is not forecast for another year, in some quarters it's already being felt. As Joe O'Neil, president of Hunter Technology, told me in late March, "There's been a dramatic slowdown in contract flow, although not so much for proposals."

Curiously, even as new programs are slowing, the DoD appears more open than ever to new technologies. Says O'Neil, "They are going bonkers on technology. It's no longer, 'If it's not plated through-hole, we don't trust it.'" Kelly Flanders of EMS firm dataCon agrees, saying he sees the military becoming more receptive to commercial parts. "They're testing more COTS. They're forced to look at other technologies in order to get the costs down." But while Flanders and others say they haven't come across requests for lead-free technologies for military applications, a task group made up of Defense primes is investigating just that. The ongoing Joint Council on Aging Aircraft/Joint Group on Pollution Prevention (JCAA/JGPP) project aims to ensure effective repairs can be made to military aircraft assemblies regardless of the solder alloy used. So far, they've learned that solder joint reliability is "very different" for different parts, and that early life failures "may be dominated by special causes of variation" during initial runs. Given that most high-rel military products are built in modest volumes, the latter finding is somewhat worrisome.

The Lead-Free Electronics in Aerospace Project (appropriately nicknamed "LEAP"), a working group of all the major aerospace stakeholders, is going a step further, developing a group of standards that responds to the lead-free electronics wave. Keynoting at the Military Technologies Conference in March, Raytheon engineering fellow and LEAP team member Dr. Anthony Rafanelli asserted that industry needs to "rethink our definition of solder alloy: Does it need to take into consideration the surface finishes …? Should we be thinking of [an] interconnection system?"

LEAP is asking the right questions and moving at the right pace. Warfighters aren't landfilled. Likewise, a missile, by definition, is bad for the environment; hence, there should be no rush to produce a lead-free version. That the technology works should be paramount, regardless of the DoD's push for lower costs.

Recall that the EMS industry has longstanding ties to military contracts. SCI, generally recognized as being a pioneer of outsourced assembly services, has its roots in building for the DoD. In the prime of the recovery, the trick now is to avoid getting shot down.

The following are clarifications to Phil Zarrow's March column:

· XRF analyzers that use the lower-energy region of the x-ray spectrum can quantify a greater range of elements, at lower detection limits, and serve multiple purposes, including tin-whisker screening and counterfeit product identification.

· Signal-to-noise ratios are worse in K-shell x-rays than in L-shell for lead and mercury, and as such a "K-shell only" device may encounter difficulty proving something is not present, which is crucial for reliable RoHS screening.

· Certain XRF analyzers provide quantitative elemental composition at ppm levels.

· Using the lower-energy portion of the x-ray spectrum, it is possible not only to isolate individual small components, but also to set a thickness algorithm permitting greater accuracy on polymers as thin as 0.1 mm.

Circuits Assembly regrets the confusion.

Mike Buetow

Mike Buetow, Editor-in-Chief
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In Brief

EMS provider **SMC** (smcems.com) will add 18,000 sq. ft. to its current 55,000 sq. ft. facility in Lexington, KY. The added capacity will include 16,000 sq. ft. of manufacturing space and 2,000 sq. ft. of office space.

The U.S. Department of Defense has awarded **Endicott Interconnect Technologies** (eitny.com) multiple contracts totaling $164 million to produce card frame assemblies, including organic semiconductor packaging, module assemblies, PCBs and assemblies, and engineering services. The company did not specify what product the assemblies would be used for.

Kyzen Corp. is now providing immediate online customer service support. Users can click on the Live Support icon at kyzen.com and be instantly connected to a service advisor. Online support is available when the Live Support Online icon is green. Visitors can choose from technical support or customer service and can type in technical questions, questions about orders, etc.

Plexus Corp. (plexus.com) is expanding its European design center in Livingston, Scotland, and will add 19 workers to the 12 already employed. The EMS provider received a £159,000 grant, which will help fund the positions.

Indium Corp. (indium.com) purchased a **Koh Young** (kohyoung.com) KT-3020T solder paste inspection system.

Scanfil PLC (scanfil.com), the second largest EMS group in the Nordic region, will shut down its Oulu plant this summer and transfer operations at its Äänekoski plant to other units by end of September. A total of 95 workers will be laid off. Scanfil's EMS operations had 2006 sales of about 240 million euros.

Juki (jas-smt.com) has opened an office in Thailand. Thai Juki SMT Asia is responsible for sales and engineering service.

Indium Corp. (indium.com) named **LFG Micro** (lfgmicro.com) as sales representative in New Jersey, eastern Pennsylvania, and southeastern New York.

Solectron Restructuring: 1,500 Jobs Cut

MILPITAS, CA – Solectron Corp. (solectron.com), one of the world's five largest EMS companies, will lay off about 3% of its employees and take a restructuring and impairment charge of $35 million to $45 million. The company reported second-quarter sales of $2.90 billion fell 3% sequentially but rose 16% year-over-year.

The sales uptick was offset by the company's announced layoff of 1,300 and 1,500 employees during the next 12 months as part of a previously announced restructuring plan.

Solectron will also close or consolidate 400,000 sq. ft. of facilities, mainly in North America and Western Europe. The company reported GAAP profit after tax from continuing operations of $15.6 million, up from $6.6 million in the first quarter and down from $17.1 million a year ago.

Non-GAAP profit was $41 million, down from $47.6 million sequentially and up from $29.7 million last year.

Solectron guided for third-quarter sales of $2.90 billion to $3.10 billion.

Major Solder Vendors Add Paste Surcharges

JERSEY CITY, NJ – A trio of major solder vendors have announced surcharges on certain tin-bearing solder pastes.

On March 30, Cookson Electronics (cooksonelectronics.com) announced a surcharge on Alpha brand Sn-bearing solder pastes, effective 30 days from customer notification. A few days later, Indium Corp. (indium.com) followed with a surcharge on its Ag- and Sn-containing solder pastes, effective immediately. Then on April 4, Kester Solder (kester.com) tacked on a surcharge on Ag- and Sn-containing pastes, effective 30 days from customer notification.

A global shortfall in tin supplies versus forecasted consumption has pushed prices to 19-year highs. Since January, tin has increased to $6.25/lb. from $3.36/lb., and silver has increased to $203/lb. from $133/lb. The metal cost for Pb-free SAC 387 solder alloy rose from approximately $8.27/lb. to $13.68/lb., a 65% increase. Metal costs have been increasing steadily the past year; elevated prices are expected to prevail for the remainder of 2007. (CIRCUITS ASSEMBLY tracks major metals prices in its Market Watch section.)

Kester's surcharges are based on the difference between current metal costs and those from January 2006, and will be eliminated when tin and silver prices return to January 2006 levels. – *Chelsey Drysdale*

CIRCUITS ASSEMBLY Publishes 2007 Directory of EMS Providers

ATLANTA – CIRCUITS ASSEMBLY in April published the latest update to its directory of electronics manufacturing services providers. The *2007* CIRCUITS ASSEMBLY *Directory of EMS Providers* lists more than 1,270 EMS facilities worldwide, from A and M Electronics to Zicon.

The *2007* CIRCUITS ASSEMBLY *Directory of EMS Providers* represents hundreds of man-hours of research into the world of electronics manufacturing services and original design manufacturing. It contains detailed information ranging from facility addresses and contact information, site contact persons, annual sales revenue, number of employees, number and type of assembly lines, size of manufacturing floor, services offered, markets served, and certifications. The price is $999.

"The 2007 DEMS is a must-have guide for OEMs searching for EMS providers, and for suppliers of assembly equipment, materials, components and circuit boards that market to EMS firms," said Mike Buetow, editor-in-chief, CIRCUITS ASSEMBLY.

For ordering information, visit circuitsassembly.com/cms/dems.

In Brief

Nortec Inc. (nortecid.com), a provider of harsh environment ID products, named **The IPS Group** (theipsgroup.com) its manufacturing representative for Texas, Oklahoma, Arkansas, Louisiana, Arizona, New Mexico, Southern California and Mexico; **MarTec Inc.** (martecincorporated.com) as representative and distributor in Alabama, Mississippi, Tennessee and Georgia; and **Tonka Electronics** (tonkaelectronics.com) as representative in North Dakota, South Dakota, Minnesota and northwest Wisconsin.

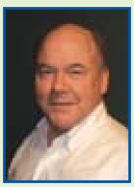
Interplex Industries (interplex.com) acquired the assets of Handy & Harman Electronic Materials and Handy & Harman Ele Asia. The acquired operations perform integrated stamping, electroplating and molding for lead-frames and packaging.

People

Celestica Inc. named **Tony Rakoczy** vice president, global commodity management, based in Hong Kong. The company also named senior vice president of finance **Paul Nicoletti** interim chief financial officer. He supersedes **Tony Puppi**, who retired in April.

LaBarge Inc. named **Amy Hines** material manager for its Tulsa manufacturing facility, and named **Roger O'Kane** engineering manager at its Joplin, MO, operation.

EMS provider NOTE AB named **Kaj Samlin** chief executive officer and president. Samlin is a former CEO of Habia Cable AB, and has experience with the Electrolux group and a Swedish-Chinese JV performing shop fitting.



Valor Computerized Systems named **Ken Horgan** strategic accounts manager, North America. He was a corporate accounts manager at UGS/Tecnomatix, and has a bachelor's in business administration from Boston University.

The Millennia Group named **Ron Cosper** vice president and general manager for its Millennia Technology Division.

Foxconn to Build 2d Czech LCD Plant

PRAGUE – Foxconn (foxconn.com) will invest up to $100 million to build an LCD factory in the Czech Republic. On April 3 *Hospodarske Noviny* said the investment could be lower than $70 million, but possibly more than $100 million, quoting Foxconn Czech Republic chief Jim Chang. The new site would employ 5,000 people, the report said.

An earlier report by a Czech government agency put the figure at $23 million.

The factory would be Foxconn's second LCD plant in the country. Since launching production in 2000, Foxconn has become the CR's second largest exporter.

More Changes in Store for Sanyo Electric?

TOKYO – Is Sanyo Electric Co. (sanyo.com) gearing up to sell its cellphone and digital camera businesses? The Japanese electronics giant already outsourced its TV and home appliances businesses, part of a strategy to focus on energy and green businesses. It is taking bids on its chip division.

In April, as the company ushered in a new president, 30-year veteran Seiichiro Sano, shareholders were telling the company to outsource or spin off its mobile phones and digital camera units, too.

PCB Design Conference East, West to Swap Dates

ATLANTA – UP Media Group announced a seasonal switch in schedule for PCB Design Conference East and West.

Beginning in 2008, PCB West will be held in the fall in the Silicon Valley. PCB East will move to the spring, with the 2008 show being held in the Chicago area. The exact dates and location will be announced soon.

UPMG also made the following announcements for PCB West 2008: A special focus will be placed on printed circuit manufacturers and manufacturing technologies on the exhibition show floor; the conference will feature numerous new courses on the hottest topics; three keynote addresses will take place; a mini, pocket-sized Trakker lead-gathering system for exhibitors will be offered for the show floor.

PCB DESIGN CONFERENCE EAST

PCB East 2007 will be held on Oct. 21-26 at the Durham (NC) Marriott at the Civic Center. For more information, visit www.pcbeast.com.

UPMG (upmediagroup.com) publishes CIRCUITS ASSEMBLY.

AeA Calls for Immediate U.S. Action to Maintain Competitiveness

WASHINGTON – A new report issued in late March by trade group AeA (aeanet.org) reiterates that America must act now to stem the loss of its competitive advantage.

The report, "We Are Still Losing the Competitive Advantage: Now Is the Time To Act," is a sequel to an AeA report two years ago. The original asserted the U.S. was at risk of squandering its preeminence in science, technology and innovation in the face of greater emphasis on those areas by other nations coupled with domestic neglect of the factors that form the basis for its lead.

The latest edition reinforces that conclusion and calls for immediate action. Recommended steps include improving K-12 math and science instruction; increasing federal funding for basic research in the physical sciences, engineering, math and computer sciences; giving green cards to all U.S.-educated masters and doctoral students, and ensuring access to broadband for every American within five years.

The report includes other recommendations for timely action, a timeline of what has happened in the last two years to move the competitiveness debate forward, testimonials from executives in the high-tech industry, and updated data and analysis. To download the report, go to www.aeanet.org/competitiveness. – *Chelsey Drysdale*

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People

RMD Instruments appointed **Steve Glass** business development manager, RoHS/WEEE Division, responsible for the company's line of RoHS-detection instrumentation using XRF technology.

Cogiscan hired **Satoshi Inoue** as Japan sales engineer. He has 10 years' experience as an SMT equipment provider in QA, customer support and software system solutions.

DEK promoted **Nick Crocker** to Americas customer support group manager. He has been with DEK for more than 10 years in technical service and support roles, including Americas service control center coordinator.

Cookson Electronics director of customer technical support **Paul Lotosky** was elected technical committee chair of the IPC's Solder Products Value Council.

Indium Corp. promoted **Seth Homer** to product support specialist for engineered materials. The company also named **Rui "Anny" Zhang** product specialist, solder paste products, responsible for channel support in China including program development and sales readiness. She has a master's in engineering management from Dartmouth College.

EMS company Global Innovation Corp. named **Doug McBride** vice president, director of technology.

EMS provider SMTC Corp. named **Paul Blom** senior vice president, supply chain, responsible for materials planning, strategic procurement and logistics. He was previously senior vice president, global supply chain management operations at Celestica.

H-P Slaps Acer with Infringement Suit

Palo Alto, CA – Hewlett-Packard, the world's top-ranked PC maker, filed suit March 27 against Acer Inc., alleging infringement on five separate patents and seeking an injunction and unspecified damages. H-P (hp.com) claims Acer (acer.com), the fourth largest PC maker, infringed on patents for power management, clock switching, and other technologies.

In a statement, H-P called the suit "necessary because HP believes Acer has been selling computer products that use HP's patented technologies without permission."

Last quarter H-P topped the global PC rankings with an 18.1% share. Acer was fourth at 7.1%, behind Dell and Lenovo, according to research firm IDC.

Delta Acquires Singletec in EMS Merger

ALBUQUERQUE, NM – Delta Group Electronics (deltagroupinc.com) has purchased the assets of Sanford, FL-based electronic manufacturing services supplier Singletec Inc. (singletec.com). No financial terms were disclosed.

Delta, which has acquired three EMS companies during the past two years, will combine the Sanford plant with another factory in Rockledge, FL, by late this year. Singletec president Kurt Storey will become sales and marketing manager for Florida.

Previous acquisitions include Frontier Technologies in California and Assembly Solutions in Texas. The company has six assembly lines and more than 100,000 sq. ft. of manufacturing space across its four current plants, according to the 2007 Circuits Assembly Directory of EMS Companies (circuitsassembly.com/cms/dems).

Intel to Host Technology Interchange this Month

PORTLAND, OR – Intel Corp. (intel.com) invites suppliers to participate in a technology interchange in which the semiconductor company will share its vision and reveal its requirements for the supply chain. The event – Where Are We Going? Where Do We Need to Be? – will be held May 23 at the Holiday Inn Portland Airport.

Intel general manager of systems manufacturing technology development Martin Rausch will keynote the event, speaking on the transition to HDI.

Other topics to be discussed include underlying issues that must be overcome as the industry makes advances in package scaling and associated board density, and what needs to happen to create pull for HDI PCBs from the OEM and ODM communities.

Nine industry suppliers will outline the supply chain's abilities and present gap analyses in the areas of lamination, cost-effective microvias, metallization/etching, embedded passives, board-level underfill solutions, component size and spacing reductions, assembly equipment, rework and alternative alloys. For more information, contact Susan Filz, SusanFilz@ipc.org. – *Chelsey Drysdale*

Solder Suppliers Balver Zinn, Cobar to Merge

BALVE, GERMANY – Solder material suppliers Balver Zinn (balverzinn.com) and Cobar Group (cobar.com) have signed an agreement to merge, a deal that would result in annual company sales of more than $50 million. The deal is expected to close during the second quarter. No financial terms were disclosed.

As a member of the Balver Group, Cobar will lead development solder paste, solder fluxes and related products, while Balver Zinn will focus on the metallurgy of the solder materials.

Balver Zinn is based approximately 30 km south of Dortmund, Germany, and is a major non-ferrous metal producer. Breda, Holland-based Cobar is a global supplier of solder paste, solder fluxes and related materials for electronics assembly.

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Trends in the U.S. electronics equipment market (shipments only).

	% Change			
	Dec	Jan[r]	Feb*	YTD
Computers and electronics products	-6.7	10.7	-4.1	1.4
Computers	-4.1	0.0	8.1	-1.4
Storage devices	1.3	-7.4	1.1	0.5
Other peripheral equipment	0.0	-2.9	-2.9	-2.1
Nondefense communications equipment	-10.0	5.7	6.8	-5.0
Defense communications equipment	-10.2	-7.1	7.3	4.3
A/V equipment	4.0	-2.9	-12.3	-2.4
Semiconductors	-24.4	65.6	-23.3	1.5
Components[1]	-0.1	-2.4	-0.4	3.0
Nondefense search and navigation equipment	1.7	25.2	-9.3	17.8
Defense search and navigation equipment	0.9	3.5	0.5	12.5
Medical, measurement and control	-0.5	-1.7	0.1	1.5

*[r]Revised. *Preliminary. [1]Includes semiconductors. Seasonally adjusted. Source: U.S. Department of Commerce Census Bureau, Apr. 4, 2007*

March Customer Inventories, Orders Down

TEMPE, AZ – Economic activity in the manufacturing sector expanded in March for the second consecutive month, while the overall economy grew for the 65th consecutive month, says ISM (ism.ws).

Indices for new orders and production advanced and employment and inventories declined. The PMI slipped 1.4 points but remained above breakeven, signaling a manufacturing expansion.

Customer inventories fell below 50% for the first time in six months, a development ISM spokesman Norbert J. Ore called "a positive [and] a possible indication that manufacturers' inventories are nearing satisfactory levels." Prices for certain commodities appear to be surging, however, he said.

	Nov.	Dec.	Jan.	Feb.	Mar.
PMI	49.5	51.4	49.3	52.3	50.9
New orders	48.7	51.9	50.3	54.9	51.6
Production	48.5	52.4	49.6	54.1	53.0
Inventories	49.7	48.5	39.9	44.6	47.5
Customer inventories	50.5	50.5	52.0	53.0	48.0
Backlogs	46.5	45.0	43.5	51.5	47.0

Source: Institute for Supply Management, Apr. 2, 2007

Industry Market Snapshot

Book-to-bills of various components/equipment.

	Oct.	Nov.	Dec.	Jan.	Feb.
Semiconductor equipment[1]	0.94	0.96	1.01	1.04[r]	1.05[p]
Semiconductors[2]	9.8%	9.8%	9.0%	9.6%[r]	4.2%[p]
Rigid PCBs[3] (North America)	0.99	0.92	0.92	0.91	0.96
Flexible PCBs[3] (North America)	0.91	0.86	0.90	0.93	0.97
Computers/electronic products[4]	4.99	4.73	4.98	4.90[r]	4.80[p]

Sources: [1]SEMI, [2]SIA (3-month moving average growth), [3]IPC , [4]Census Bureau, [p]preliminary

Printable Electronics Pushes $2B

SURREY, UK – The market for printable electronics subassemblies and components will top $1.7 billion this year, according to BPA Consulting (bpaconsulting.com) estimates. However, growth depends on improvements in materials and printing technology.

During the past 12 to 24 months, printable electronics materials – particularly plastic organic light-emitting displays (OLEDs) – have shown improved efficiency and stability. Yet organic systems for replacing memory chips aren't demonstrating the same gains, the firm said. Robust and cost-effective, high-volume manufacturing equipment remains a major inhibitor to adoption.

Applications that will use printable electronics and materials include organic ICs, display technology, RFID and Smart Active Labels (SAL) for packaging, antennae, batteries and photovoltaics. Cost is the key driver to all of these markets, BPA said.

IP Cameras Looking Good

EL SEGUNDO, CA – Global video surveillance camera revenue is forecast to grow to more than $9 billion by 2011, a CAGR of 13.2% from 2006, according to iSuppli (isuppli.com). Video surveillance unit shipments will more than double to 65.7 million units in 2011, a CAGR of 17.1%.

Electronics Gear Demand Slowing, Will Rebound in '08

LOS ALTOS, CA – Changes in corporate PC purchasing is slowing electronics equipment growth, which will slip this year but recover in 2008, says Henderson Ventures (hendersonventures.com) in its latest newsletter. "Corporations no longer feel compelled to upgrade their systems every three years because hardware and software advances don't offer the productivity improvements that previous upgrades have given," Henderson wrote.

The U.S. has been particularly hard hit: PC unit shipments grew just 1% last year, vs. 9.9% worldwide. Forecasts call for a global slowdown to 7.1% this year before recovering to 10.2% in 2008, Henderson said.

Metals Index

Date	Price per lb. 1/8/07	Price per lb. 2/4/07	Price per lb. 3/12/07	Price per lb. 4/5/07
LME Cash Seller and Settlement for Tin	$4.91	$5.42	$6.28	$6.43
LME Cash Seller and Settlement for Lead	$0.77	$0.77	$0.85	$0.92
Handy and Harman Silver (COMEX Silver)	$178.48	$213.28	$188.29	$245.35
LME Cash Seller and Settlement for Copper	$2.61	$2.50	$2.80	$3.38

Return of the One-Stop Shop

Near extinction in the early 2000s, the vertical model is making a comeback.

While OEMs leave no stone unturned in pursuit of cost-cutting, the trend toward outsourcing initially saw deep splintering of once-vertical factories into distinct operations for design, board fabrication, assembly, box-build and system integration.

That trend, which peaked in the early 2000s, appears to be shifting. Led by a mix of EMS firms ranging from some of the world's largest contractors – including Foxconn (foxconn.com), Flextronics (flextronics.com) and Sanmina-SCI (sanmina-sci.com) – as well as several smaller ones, the one-stop shop, once near extinction, is returning. And some argue it never should have left.

In a presentation at the European Supply Chain Conference last fall, Juergen Seibert, Sanmina-SCI senior director, business development, Central Europe, asserted OEMs will continue to embrace outsourcing by entrusting the right EMS partner with more design and engineering, prototyping, final system assembly and test, supply chain management and other service needs.

Driving the switch is the recognition by OEM procurement staff that it's not the price per piece that matters so much as the total cost of ownership. Once costs like logistics, freight, taxes, overseas engineering support, and so on were tallied, it became clear that chasing labor rates in a highly automated manufacturing environment was a fool's game. (That Wall Street has somewhat eased its demands that public companies have "China solutions" has also been a significant factor.) As a result, Mexico and developing markets such as Eastern Europe have seen a rebound in orders as programs are shifted nearer to OEMs and their end-customers.

Sanmina-SCI has gone so far as to brand its one-stop offering, calling it the Gateway concept. Under the plan, Sanmina-SCI develops local outsourcing solutions and services based on a customer's individual requirements. As Seibert explained, the aim is to provide one local point of contact for commercial representation, technical design and engineering solutions, and at the same time leverage global network and capabilities to offer easy access to volume production in low-cost regions, if required.

With a local point of contact, the OEM benefits from commonality of language, culture and time zone. The design, engineering and technology support offered locally taps into Sanmina-SCI's global resources to provide a tailor-made solution that can change during the product lifecycle as the customer's requirements develop, Seibert says.

The concept is probably most beneficial, he says, to mid-sized OEMs outsourcing for the first time, and to startups looking to open up new export markets.

The Gateway offers a pithy name to an idea that is both far-flung and gaining popularity. Indeed, using a single supplier has several obvious advantages that won't be detailed here. One subtle benefit is in product returns: Instead of the typical process, in which faulty product leads to finger-pointing (and sometimes lawsuits) between the fabricator and assembler, the OEM "knows" who is responsible.

Another is the considerable challenge of producing high-tech boards. Explains Joe O'Neill, president of Hunter Technology (hunterpcb.com), "We assemble as we fabricate" to demonstrate proof-of-concept, he says. "It doesn't do any good to fabricate it if you can't assemble it." Just the difficulty getting around differences in machine software (a problem as old as the industry that yet unbelievably still persists today) is an argument in favor of the single-source factory, where problems of incompatibility don't appear with each new program.

EMS providers following the vertical model include some of the biggest in the world. Besides the aforementioned, others include Endicott Interconnect Technologies (profiled in the January 2007 issue), Viasystems (viasystems.com) and Videoton (videoton.hu). While EI functions on a single, albeit massive campus, the latter companies are true multinationals: Hungary-based Videoton operates 10 locations in three countries, while Viasystems has 15 sites in six countries.

But the model isn't exclusive to the big boys. Several smaller companies follow similar models in offering multiple services on a single campus, including Hunter in the Silicon Valley, One-Source (onesource-group.com) in Dallas, and Printed Circuits Corp. (pcc-i.com) outside Atlanta. One notable difference: PCC's and Hunter's design, fab and assembly divisions share a name, while the One-Source operations are individually branded.

Competitors are coming online all the time. Just last quarter, Design Solutions Inc. (designsolutions.com) jumped into the fray, adding assembly capability via its acquisition of Paradigm Manufacturing Partners, part of a strategy that will see design, fabrication and assembly facilities throughout Eastern Europe and North America. DSI says that, while it is not a "full-fledged EMS," as its assembly operations provide "proof of concept" builds for its customers, "this will expand these capabilities as the company expands."

The guess here is they won't be alone. ■

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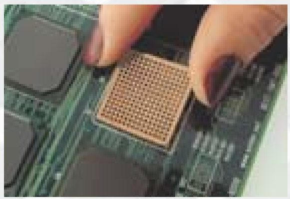
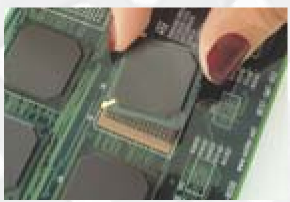

Step 2 - Align and affix the StencilQuik™ onto the PCB


Step 3 - Squeegee paste or flux through the apertures onto the PCB


Step 4 - Align, place part and reflow

StencilQuik™ is the new way to repair mask damage underneath area array or other devices. By simply applying the **StencilQuik™** underneath the area array device, hours of mask repair time can be eliminated. This will prevent the solder from migrating down the "dogbone" to the via. Not only is mask damage repaired quickly but **StencilQuik™** is a simple, easy way to apply solder paste for your area array device rework or initial prototype placements. **StencilQuik™** eliminates the frustration and time consuming nature of metal rework stencils while eliminating the need to repair mask damage underneath the area array device.

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StencilQuik is a patent pending invention from BEST Inc.

Embedded Components: A New Development?

It's an old technology, but the potential for revolution remains.

One hot topic in semiconductor packaging and assembly is embedded components in the IC package substrate or PCB. What are these structures? And is this a new concept, or is the technology finally moving closer to production after years in R&D?

What's an embedded component? IC packages with embedded active or passive components are structures on which the substrate is fabricated on top of the active device and may incorporate resistors, capacitors or inductors. Embedded components in PCBs feature active or passive devices incorporated into internal layers. In this embodiment, embedded passives provide an alternative to issues associated with discrete parts, including cost, handling, assembly time and yield, and board space.

General Electric introduced the "chips first" concept more than two decades ago. Companies including ACET in Taiwan, Casio Micronics in Japan, and Freescale Semiconductor in the U.S. are developing new versions of the technology. In Europe, 3D Plus has patented a stacked module technology that is also considered an embedded component package. The research was part of a four-year European program that ended in 2004 and included STMicroelectronics, CEA/LETI, Thales, Schlumberger, Cards/Axalto, Cybernetics and IBS.[1] Infineon and Imbera have also developed embedded component concepts.

Integrated passives in thin-film-on-silicon or glass substrates were introduced more than 15 years ago by AT&T Bell Labs and used in a desk phone. SyChip, a spinoff of Bell Labs researchers, developed an RF module based on the technology and was purchased by Murata of Japan. Shinko Electric developed a thin-film-on-silicon process with an embedded capacitor. STMicroelectronics and Philips each ship thin-film substrates with integrated passives.

Casio Micronics and CMK Corp. have developed an embedded wafer-level packaging (EWLP) technology. Casio has developed a prototype EWLP module that functions as a digital TV tuner. In the module, a WLP is embedded in the board with a tuner WLP and other components mounted on the board. The EWLP Consortium, formed last April to promote the technology, will work on development and standards.

Freescale developed Redistributive Chip Package (RCP) based on a batch process that features a buildup and metallization constructed on an embedded die.

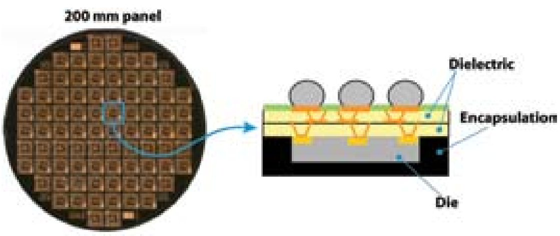

Figure 1. Sample configuration of an embedded semiconductor die.

Freescale is targeting a number of applications with RCP, including DSPs, applications processors, base band processors, power management devices, RF transceivers, and power amplifiers.

The benefits of embedded components are multi-die capability and, in some cases, two-sided construction in which components can be mounted on top of each other. This permits fan-out routing – important as companies look for WLP solutions or higher pin count die. It is also possible to integrate passives in some of the embedded processes, and internal EMI shielding is possible for some designs.

The technology is not without challenges. Although it has been around for decades, it has not been commercialized for IC packages. With some technologies, there have been materials and process issues. Any packaging technology that departs from the traditional infrastructure requires a new infrastructure of material, equipment and service providers. With traditional packages using known good substrates, assembly yields are typically greater than 99%. For the embedded chip in substrate, the advantage of good die will be lost to substrate buildup process yield. Thin-film versions of this technology require serial processing, creating compound yield issues.

PCBs with embedded components. The desire to increase reliability, improve performance and reduce cost has driven a significant amount of effort during the past 20 years to embed resistors and capacitors in PCBs. As with many new technologies, an undeveloped infrastructure, including supply base for materials, experienced fabricators, design tools and test methods, lack of standards, and limited reliability data has slowed widespread adoption. Early adopters implemented the technology to solve major problems.

Historically, resistors buried in PCBs were used in military and aerospace applications where solder joint elimination and weight reduction were the primary

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The Electronic Components and Technology Conference (ectc.net), May 29-June 1, in Reno, NV, will include a session on embedded devices in advanced substrates.

issues. Planar capacitance solutions have been designed in high-end applications to deliver moderate performance improvements. Recently, new solutions and enabling technologies have been extending the use of embedded components to mobile phones, digital cameras and camcorders, and medical applications.

In February 1999, NIST launched its Advanced Embedded Passives Technology (AEPT) project. Motorola introduced a PCB with embedded passive components in its mobile phones in late 1999. The V66 GSM mobile phone reduced the number of SMD components from 89 (51 capacitors, 16 resistors and 22 inductors) to 33 embedded components (18 capacitors, 11 resistors and 4 inductors). It also reduced the board size from 40 x 23 mm to 23 x 23 mm.[2] The AEPT program continues to produce improved technologies. Standards development began in 2003, with the IPC and Japanese Electronics and Information Technology Industries Association (JEITA) focusing on materials, design, dimensions and other specifications for embedded components. Companies that have recently developed laminate boards with embedded components include AT&S, Clover Electronics, CMK (now partnering with Casio Computer), Compeq, DT Circuit Technology, Fujitsu Interconnect Technologies, Ibiden, Matsushita Electric Industrial and Wus.[3] While Motorola is not using the substrate with integrated passives today, it shipped tens of millions of units in its products. Clover says it has supplied more than one million components with an embedded RF device since 2003.

The success of embedded active components in IC packages will depend on investment in tools in the packaging area. Materials used in fabricating the structures are also important. The industry is poised to make significant increases in the use of integrated passives in a broad range of products and applications. Just as microvia technology revolutionized the PCB industry, embedded technology has the potential to do same. ■

Au.: The author gratefully acknowledges contributions from Karen and Richard Carpenter in research for this article.

References

1. C. Val, "Ultra Low Profile 3-D Cube with Wafer Level Packaging Technique," International Wafer-Level Packaging Conference, Nov. 3-4, 2005, pp. 134-137.
2. "Motorola Ships Passive-Embedded PCB for Mobile Phones," Nikkei Electronics Asia, Tokyo, Japan: Nikkei Business Publications, May 2003, pp. 30-39.
3. E. J. Vardaman, "Are Embedded Passives Ready for Prime Time?" Circuits Assembly, July 2003, pp. 12-13.

Screen Printing

网板印刷

0.3 mm CSPs: Closer than You Think

Revealed: The best-suited material set for next-generation chips.

Not only are 0.3 mm CSPs literally closer (as in pitch), they are also figuratively closer (as in entry into mainstream manufacturing) than most would like to think. The truth is that in 12 to 18 months, 0.3 mm CSPs will be incorporated into high-volume SMT production for certain applications – like it or not! Already, major cellphone manufacturers are evaluating these devices and the corresponding manufacturing requirements necessary to push them into the mix for high UPH (units per hour) production.

If you think moving from 0.5 mm to 0.4 mm CSPs was challenging, just wait until your BoM includes 0.3 mm chips. To help customers prepare for the inevitable, we undertook a study to investigate the printing process as it relates to 0.3 mm CSPs. The results were interesting, indeed; some you'd expect, some not so predictable.

To obtain a complete picture of manufacturability and optimum screen-printing parameters, it was important to analyze the entire process – print, place, reflow and build quality – not just look at printing and deposit volumes. Remember, a process like this would have been in the low-volume semiconductor realm not so long ago, so understanding all implications for high-volume SMT assembly was imperative. For solder, we used type 3 and 4 pastes from the same supplier. As type 3 paste is most common in mainstream SMT, we thought it prudent to analyze its behavior, even though we anticipated it would not be a high-volume choice. And, obviously, the type 4 paste's finer particle size was expected to be more conducive to ultra-fine-pitch printing. It also bears noting that we intentionally excluded type 5 paste because, at this point, the cost of the material is likely to outweigh the benefits. Stencil selection included three laser-cut stainless steel stencils (two of superior quality at thicknesses of 50 µm and 75 µm, and one of lesser quality at 75 µm) and a 66 µm electroformed stencil of very high quality. Because stencil production method and laser precision are critical to the overall deposit result – for shape, volume and location – we added the inferior stainless steel stencil as a measure of comparison against the higher quality stencils. Finally, aperture dimensions ranging from 125 µm to 210 µm were used to determine the most efficient ratios.

As stated, many of the results were expected and confirmed experimentally. First, as projected, type 4 solder paste was the clear winner from a materials perspective. The experiment proved that type 3 paste can be used in certain situations (a 50 µm mask thickness with 180 µm aperture dimensions), but it is not a high-volume alternative. The 50 µm stencil would most certainly cause insufficient material volumes with other devices on the board and would not comply with heterogeneous assembly requirements. Second, it became apparent early on that the stainless steel stencil produced using an inferior laser delivered poor results with numerous I/C failures – even with type 4 solder paste – indicating that stencil quality and manufacturing method must be well-defined for a process this precise. We expected the electroformed stencil to give superior results and, in fact, it did deliver outstanding, beautifully spherical and repeatable deposits. But, surprisingly, the well-manufactured stainless steel stencil produced very acceptable results, with a price/performance ratio more in line with low-cost, high-volume production. Finally, the study confirmed that the 0.66 aperture ratio rule can be broken, but only when suitable materials and inputs are used in the print process.

What's the magic recipe? While further analysis is necessary to evaluate the results of varying squeegee blade material types and delve deeper into some inconsistencies we found with nitrogen versus air reflow atmospheres, we have proven that 0.3 mm CSPs can be produced in a repeatable, high-volume environment. The material set that is best suited to 0.3 mm CSP production is as follows:

- Type 4 solder paste.
- 75 µm thick stencil.
- Extremely high-quality stencil – either stainless steel or electroformed.
- Aperture dimensions ranging from 170 – 190 µm.
- Stable, high-accuracy printer platform.

Although we are confident that our "magic recipe" provides the optimum ingredients, putting them together for a five-star result will take tremendous expertise and superior process control. Depositing 170-180 µm dots of material in a high-volume SMT environment is no easy task, especially when you consider all the materials have to be compatible with the other components on the board. Oh yeah, let's not forget that this has to happen at sub-7 sec. cycle times! Pretty incredible when you think about how far we've come in the past few years. Keep looking over your shoulder: 0.3mm CSPs will be on your back in no time and you'd better be ready. ■

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The Methodologies of NPI

Companies that integrate NPI into their routines see less disruption and achieve faster time-to-market.

Ed.: For the complete column, please see circuitsassembly.com.

Most events such as NPI are applied with common sense, which makes it even more surprising that few companies adopt rule-based control methods. There are four fundamentals to successful NPI. As you might expect, these are analysis, concept development, implementation and sustainability. Each can be subdivided so that specialists or appointed teams (**Figure 1**) can concentrate on a topic while knowing their counterparts are working on the others in parallel. NPI is usually time-sensitive, and the ability to run teams in parallel permits necessary work to be carried out in the allotted time. Time control is one of the areas that can easily get out of hand.

The analysis phase can be broken into processes or equipment evaluations and comparison with existing processes or equipment. This also includes any necessary assessments of skill sets. If no dedicated NPI facility exists, it is necessary to build NPI capacity into the planning schedule of the production line(s). At this point, the team should be assembled, in theory at least, ready to identify its tasks and time schedules planned.

That skill sets may need to be evaluated suggests the involvement of HR departments, but you may note the outer ring of other team member activities (Figure 1). This is intended as a catchall for departments such as HR. For example, purchasing may play a particular role in some NPI activities, although it lacks its own section.

Once we know that capacity is available and the skills, technology and processes can cope with the new product (or that measures are being taken to acquire the necessary skills, processes and technologies), we can move to the second phase: the concept.

The team leader and perhaps one or two chosen specialists will have performed all the analyses, but the concept requires the whole team's input. The team must set up regular CAD and product layout reviews; prepare selection procedures for acquiring new equipment, materials and processes, and develop a project plan and define longer-term production and quality goals while ensuring the target time-to-market is met. No single person can be expected to do all this, which is why the team approach is so important. Appropriate time spent preparing the proper concept will speed later activities.

Implementation, as its name suggests, puts into practice all those items documented in the concept phase and embodies pilot schemes, first-off verification programs, and process and equipment program generation. If the concept is well controlled, implementation should run smoothly. Assuming that all new requirements have detailed specifications, and scheduling and planning are accurate, the implementation results should give a green light to immediate production pending only minor changes or modifications.

Figure 1. A typical team core for NPI evaluation.

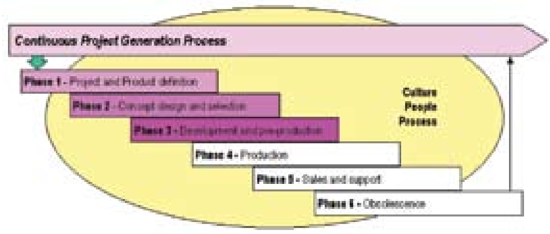


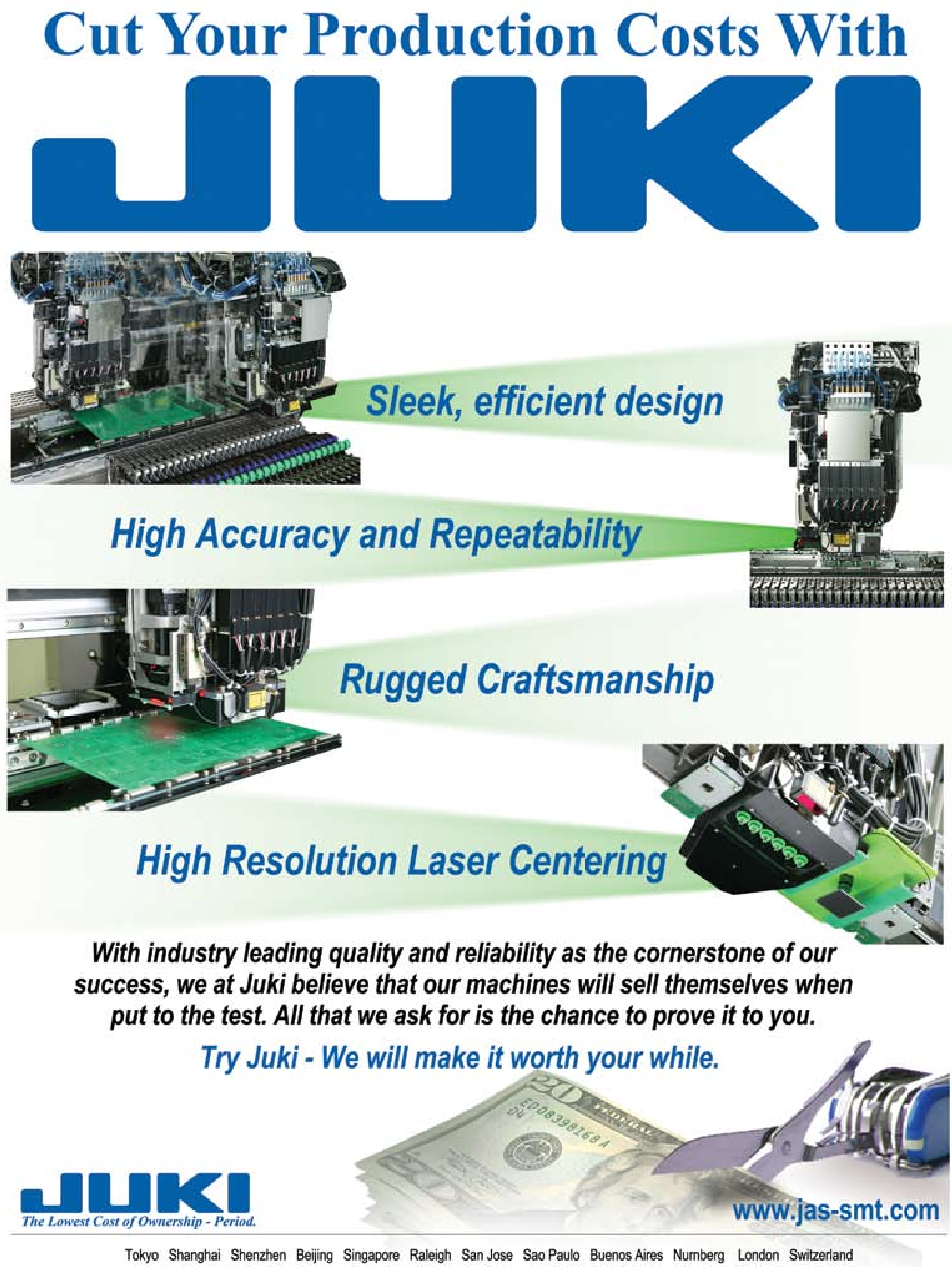
Figure 2. Further development of NPI stages.

At this point, it is necessary to review everything that occurred during NPI to avoid future pitfalls. Document all activities carefully to permit daily production checklists that ensure volume or final product production targets are met.

Sustainability is the fourth stage. Now that we are all supposed to be involved in sustaining our environment, sustainability in this case refers to the ability to maintain production at quality and throughput targets.

Figure 2 shows a typical continuous process for product regeneration and includes sales and service, and obsolescence. Neither plays any real part in NPI, with the possible exception of early input from sales and marketing in the formulation of the product idea and volume. ■

Peter Grundy is director of P G Engineering (Sussex) Ltd. and ITM Consulting (itmconsulting.org); peter.grundy2@btinternet.com. His column appears bimonthly.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Cover Story

同典型的锡/铅合金返工相比，在SAC405 PTH返工过程中印刷电路板暴露于液态焊料下的最长允许累计接触时间最多可缩短50%。允许接触时间的缩短主要是由于在提高工序温度后，SAC合金的铜溶解率提高。这个研究使用SAC合金对复杂的印刷电路板进行返工，如服务器或存储应用中的，确定了铜的溶解率，并建立了优化PTH返工工序窗口和操作参数。

A Study of Copper Dissolution During Pb-Free PTH Rework Using a Thermally Massive Test Vehicle

Craig Hamilton, Matthew Kelly, and Polina Snugovsky, Ph.D.

Adding nickel to the alloy retards copper dissolution almost to the point of SnPb.

The increase in copper dissolution rates using SAC alloys significantly alters the PTH rework process, not to mention the mindset for typical SnPb connector rework. Now, during SAC connector rework (using conventional equipment), it is required to track a board's cumulative contact time to molten solder to ensure against board overexposure and excessive copper dissolution. Previous studies[1] on a smaller, less thermally massive test vehicle with an OSP surface finish determined that a single connector site on the board could be subjected only to a maximum cumulative contact time equating a one-time connector rework attempt. This is of concern for products that require up to a two-time rework within their expected lifetime. Therefore, alternate solutions are required to increase the operating process window to permit a two-time connector rework using conventional solder fountain methods. Otherwise, alternative rework process approaches may have to be considered, such as hot-gas or infrared techniques. However, these two methods also have limitations, as they would permit only PTH connector removal. Another option to reduce copper dissolution occurrence would be to use a Ni-plated surface finish, as the strong nickel layer decreases dissolution. This may not be feasible for some OEMs, and most EMS providers will still require a process to rework a PTH connector on all surface finishes.

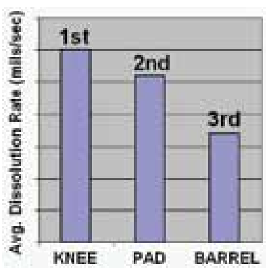

Figure 1. Copper dissolution by geometry.

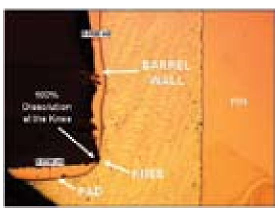

Figure 2. Hidden defect.

Even larger, more thermally massive card assemblies, such as those found in server and storage-type applications, make PTH connector rework more difficult. The combination of tighter process windows and associated reliability requirements for IPC Class 3 assemblies makes Pb-free PTH rework more challenging.

Background. Past studies focusing on copper dissolution during PTH solder fountain rework using a SAC-based alloy highlighted concerns over the ability to rework PTH connectors without significantly dissolving portions of the copper barrel plating[1]. Results showed that a simple one-time rework was possible; however, it pushed the process window, defined by the copper dissolution rate and specified remaining copper thickness. There are no industry specifications on post-PTH rework copper thickness.

It has been determined that the PTH barrel's knee is the most susceptible to dissolution. An established dissolution hierarchy confirmed that the knee location has the highest dissolution rate, followed (in order) by the annular ring (or pad) geometries and the inner barrel wall (**Figure 1**). Because the knee location has an initial plating thickness thinner than that of the pad, the conclusion is the knee location will come to complete (100%) dissolution (**Figure 2**) faster than the pad location (in the majority of cases). It is possible, then, for a hidden defect to be present after reworking a PTH connector, which could result in failures in the field.

There has been little research on precise reliabil-

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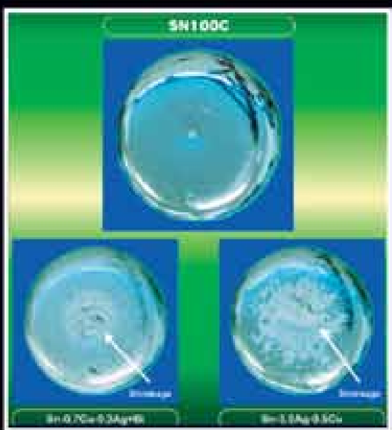
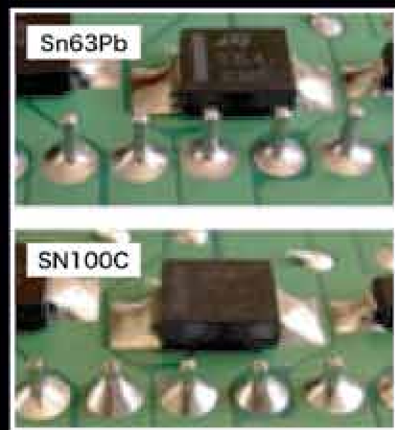
SN100C is a patented alloy comprised of tin, copper, nickel + germanium. The patent also covers tin, copper, nickel alloys. SN100C has been challenged many times and continues to hold up to all challenges as a unique alloy that that offers several advantages as well as a seven year history in the circuit board assembly industry. In today's world of knock-offs and "me too" materials, it is important to remember that this patented, reliable alloy is unique from its imitators. It is also important to understand that a knock-off alloy may change its composition in a solder pot due to dross formation or other contributing effects and may fall into the SN100C patent as a result. What may be saved by purchasing a cheap imitation may cost you in the long-term with legal issues.





Some of the unique advantages of SN100C are listed below:

- Lower copper dissolution/erosion of circuit board traces
- Yields bright shiny solder joints similar to tin-lead
- Better flow and less bridging in wave and selective soldering
- Less wear of contact material in the wave pot or nozzles in selective soldering
- Less voiding in PTH soldering
- No "hot tears" leading to more extensive inspection.
- Compatible with SAC if the solders are mixed
- More resistant to lead contamination reliability issues than SAC alloys
- Easy control of copper levels in the wave pot with the patented top off alloy concept
- Lower voiding in SMT BGA and QFN devices when used as a solder paste

When choosing an alternative alloy to SAC, make sure that you know all the facts. The lack of complete information may lead to reliability issues, process problems and possible legal action. Take the time to educate yourself about the best lead-free alloy for today's wave soldering, selective soldering and surface mount applications.

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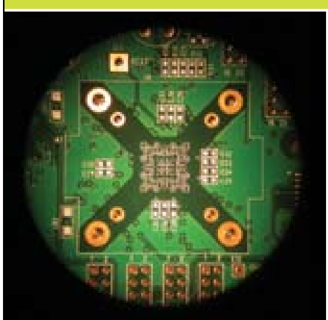
Table 1. Phase 1 DoE Matrix					
Factors	(-) Axial	Low	Mid	High	(+) Axial
Contact time (sec.)	5	13	30	47	55
Preheat temperature (°C)	100	108	125	142	150
Pot temperature	245	252	265	278	285

ity concerns of 100% copper dissolution at the knee. Assuming no bottom layer traces are present, and a good solder joint/fillet exists, it is theoretically possible for an electrical path to continue. The long-term reliability of the joint is unknown. Until this can be characterized, many OEMs are using minimum copper plating thickness specifications[2] to ensure PTH joint strength and reliability.

Test vehicle. The test vehicle (**Figure 3,** online) selected for this study was a current OEM product card. It was selected because of its thermal nature to characterize copper dissolution on a large, thermally massive PCB. The dimensions are 8.9 x 19.4", 0.096" thick. It consists of a 24-layer, high Tg FR-4 board with 1 oz. copper plating with multiple ground connections and has OSP surface finishes. The board is populated with 32 inline DIMM connectors. All results using this TV will be compared to earlier studies[1] performed on a TV less thermally massive in nature (6 x 8", 0.062", two layers of 2 oz. copper, no ground connections). The two TV scenarios will cover the PTH connector rework process representing "consumer" products up to larger "server" products.



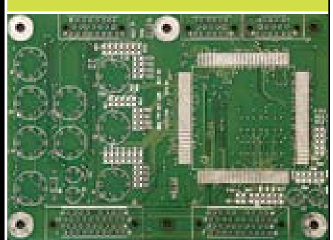


Table 3. Alloy Temperature Details			
Alloy	Melting Temp.*	Pot Temp.*	Superheat
SnPb37	183	233	50
SAC405	217	267	50
SAC305	217	267	50
SnCu0.7Ni0.5	227	277	50
*°C			

Experimental Procedure

Measurement system analysis. An optical microscope with measurement capability was used. To determine the system and operator repeatability, a Gage R&R analysis of the measurement system capability was performed prior to taking any copper thickness measurements. Data analysis confirmed that the measurement system was acceptable, with 98.5% accuracy and a measurement error of ±0.0008".

Phase 1: Copper dissolution DoE (SAC405). To understand significant factors affecting copper dissolution and establish an adequate PTH rework process window when using a SAC405 alloy, a DoE was created and performed. The main factors included were contact time, preheat temperature and pot temperature. The levels selected ranged within typical process settings. The DoE was based largely around center or mid values, with upper and lower axial points (**Table 1**).

A bare board was used for the experiment in this phase, separating individual DIMM locations into the DoE samples (**Figure 4,** online). The total sample size was 20, with each sample consisting of 14 barrel locations. This would equate to 28 separate copper thickness measurements taken per sample (at the knee location).

Phase 2: Effect of alloy. Phase 2 work studied the effect of alloy on copper dissolution rates. Three Pb-free alloys were studied (SnCu0.7Ni0.05, SAC305 and SAC405), with each compared to a eutectic SnPb37 alloy as a control. Similar to Phase 1, a bare board was used and separated into location-specific samples. Each sample was exposed to two contact times (30 and 50 sec.) using each alloy. Copper thickness measurements within this phase of work were collected in a similar fashion to Phase 1. **Table 2** (online) shows the test matrix.

Solder alloy and contact time were the primary factors varied in Phase 2. All other potential variables – flux type, equipment type, preheat method, preheat time, pot temperature – were set as constants. As each alloy has a different melting temperature, the pot temperature was changed for each to keep the superheat (or difference between melting temperature and operating temperature) constant (**Table 3**). This is important because alloy temperature does have an impact on dissolution rates. Therefore, keeping each alloy's superheat consistent was an attempt to remove the variability caused by the differing melting temperatures of each alloy.

Each DoE sample within Phase 1 and Phase 2 was cross-sectioned along the entire length of the sample at a middle row, and copper thickness measurements taken. To correlate findings of copper dissolution rates affected by surface geometry, Phase 1 measurements were taken at three locations (annular ring, knee and barrel wall) similar to earlier studies (**Figure 5**). Phase 2 measurements were focused at the knee location. Pass/fail criteria were determined on an OEM specification of 0.005" of remaining copper plating[2].

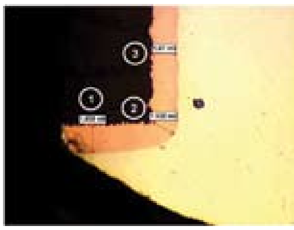


Figure 5. Copper thickness measurement locations.

Results

The results of the knee, pad and barrel wall copper thickness measurements again indicated the PTH barrel knee experienced a higher degree of copper dissolution. Therefore, all statistical analysis was based on the minimum knee measurement taken per sample.

Phase 1: Copper dissolution DoE (SAC405). DoE statistical results showed contact time to be the most significant factor affecting copper dissolution. **Figure 6** shows a main effects plot indicating copper dissolution increases as contact time increases, as expected. The results, however, showed 100% dissolution occurred at the knee after only 47 sec. of contact time.

The results showed that both preheat and pot temperature have little impact or significance on affecting dissolution within the ranges of temperature selected (**Figure 7**). Pot temperature results are trending in the direction expected: Higher pot (or alloy) temperatures increase copper dissolution.

Based on the statistical results and accounting for the specification of 0.005" of remaining copper thickness, an optimized process window was established for the TV. The process window is:

Contact time (max):	47 sec. (cumulative)
Preheat temperature:	140-150°C
Pot temperature:	260-265°C

The results posed an immediate concern since it is known that the typical (cumulative) contact time required to one-time rework the identical DIMM connector during a SnPb process is near 45 to 50 sec. Attempts to physically rework the same connector using SAC405 alloy were similar in overall time and copper dissolution was observed. It is therefore clear, based on the DoE results, that a two-time rework would be impossible to perform without irreparably damaging the PCB. To increase the process window, further studies were required to characterize the dissolution rates of alternative Pb-free alloys. These findings are discussed in the Phase 2 results.

Phase 2: Alloy DoE effect. Figure 8 shows final copper thickness measurement results for each alloy after being exposed to 30 and 50 sec. contact times. The results show that the SnCu0.7Ni0.05 alloy not only set itself apart from the SAC305/405 alloys with respect to improving copper dissolution, but it also appears to be almost comparable to SnPb. The nickel additive has an impact on reducing dissolution. In addition, the SAC305/405 alloys' dissolution slopes or rates are much greater than those of the SnCu0.7Ni0.05 and SnPb alloys. This indicates that longer maximum allowable contact times are possible, which may permit successful one-time – and potentially two-time – rework. The results indicate that an alternative Pb-free alloy (other than SAC305/405) may be required to be able to continue to use conventional PTH rework methods.

Copper dissolution rates and effect of flow rate. Figure 9 shows each alloy's average and maximum copper dissolution rates. The average dissolution rate was calculated using the mean of the average of all knee measurements taken per sample. The maximum dissolution rate was calculated by using the mean of all minimum knee measurements taken per sample. Each copper thickness measurement was first subtracted from the average baseline copper thickness measurement taken at the knee location, which was measured and calculated to be 0.00174". This would provide the amount of copper dissolved. The maximum dissolution rate would be deemed the worst-case scenario of dissolution. The main point of concern would be the minimum knee thickness measurement or the area that experiences dissolution first.

Figure 9 indicates not only a difference in dissolution rates, but also a variation in the rates of copper dissolution across a given sample. The average standard deviation of copper thickness across a sample was calculated to be 0.0022". This proves that some barrels within a connector can experience complete copper dissolution before others. One reason for this occurrence has been linked to varying solder flow rates across the connector during PTH rework. It has been observed that center pins within a larger connector will experience copper dissolution at a faster rate than pins located at the outer edges. This has been correlated to the fact that center pins are exposed to a higher solder flow rate than end pins (**Figure 10,** online). The reason for this is based on typical solder fountain flow well designs, consisting of a single opening in the center through which solder is pumped. The flow of the solder, once making contact with the PCB, is then separated into two horizontal directions of flow running parallel to the PCB. As solder is vertically pumped through the center opening, the center pins will be exposed to a higher turbulent flow of solder compared to the end pins. Another reason for greater dissolution in the center region is due to the center pins' exposure to slightly higher solder temperatures compared to the end pins. This again is correlated to the solder flow, dictated by the current machine/flow well design. Methods of reducing the solder turbulence at the center region will help reduce the copper dissolution rate.[3]

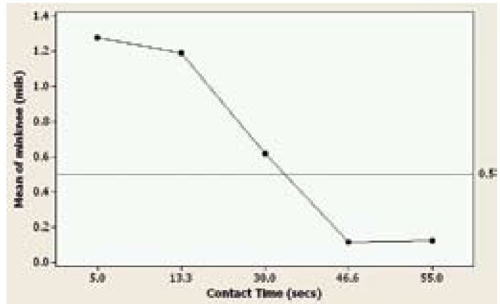


Figure 6. Main effects plot for contact time.

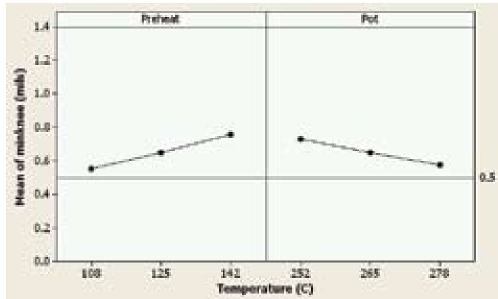


Figure 7. Main effects plot for preheat and pot temperature.

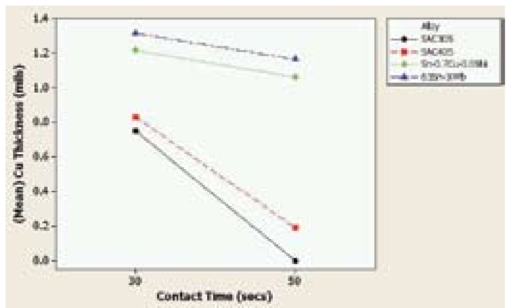


Figure 8. Interaction plot: alloy vs. contact time.

Copper dissolution visual indicators. During the course of experimentation, several PTH solder joint observations were used to help identify possible copper dissolution defects during rework. Visual inspection of reworked PTH solder joints can be used to monitor hidden copper dissolution defects located typically at the solder joint knee. Keep in mind that it is possible for copper dissolution to occur only on a handful of pins within a connector. Focusing inspection first on the center pins is recommended.

The sequence of dissolution follows. **Figure 11** (online) depicts illustrations of each phase.

Stage 1: Dissolution begins at the knee locations of the barrel. At this point, it is still possible for a fillet to exist because of the presence of the pin and remaining copper pad material. A small dip or indentation in the solder fillet will form when the knee is almost completely dissolved. This will typically be the first visible indication of copper dissolution issues and the potential existence of a hidden defect.

Stage 2: Dissolution continues at the knee and also progresses at the annular ring (pad). Typically, the outer edges of the pad begin to dissolve and feather out. At this point, the extent of dissolution will be fairly evident to a trained eye. The knee will be completely dissolved, and portions of the pad will be dissolved, causing an incomplete solder fillet. It is theoretically possible to have electrical continuity at this stage; however, it is unknown as to whether it will be a reliable joint.

Stage 3: At this point the knee and portions of the annular ring will be completely dissolved. This will cause a break in the solder fillet and will be visible during inspection.

Stage 4: The knee, pad and barrel's lower portion will be completely dissolved at this stage. Typically this has occurred over 360° of the PTH barrel. Copper dissolution will be obvious at this point, and the PCB irreparable.

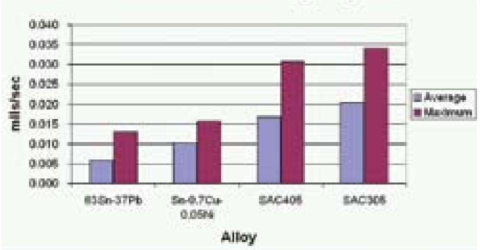


Figure 9. Dissolution rates by alloy.

Conclusions

The overall conclusions obtained from this study were:

1. A smaller process window exists when using SAC for solder fountain rework due to high copper dissolution rates compared to conventional SnPb.
2. SAC405 PTH rework can barely enable a one-time rework on the thermally massive TV used. Therefore, a two-time rework attempt would be virtually impossible to complete without significant damage to the barrel and PCB.
3. SnCu0.7Ni0.05 alloy shows almost comparable dissolution rates to SnPb (**Figure 12**).
4. An alternate Pb-free alloy (other than SAC305/405) may be required for PTH rework to increase the process window when using conventional PTH connector rework methods. Otherwise, alternative rework methods may need to be pursued (e.g., hot gas, IR).
5. Changing to an alloy other than the commonly used SAC305/405 at the PTH rework process may also force a change in the primary attach alloy used to match the selected alloy in rework, to aid process controls. Changing the PTH alloy to an alternative formulation will offer other possible complications in contamination, mixing multiple Pb-free alloys, touchup, etc. However, some initial studies indicate mixing various Pb-free alloys will not affect joint reliability.[4]
6. It is known that when using SAC305 or SAC405 alloy, it is required to either replace or coat some stainless steel parts (e.g., pump assemblies, flow wells) within the solder pot as a result of

Continued on pg. 39

一种新的封装技术涉及在硅片表面蚀刻一个深度和大小合适的蚀坑，然后在蚀坑中插入很小的图形芯片（有时称为“小芯片”）。然后，芯片同旁边的其它芯片互连（图1和图2）。这样做的目的是要在晶圆级建立低成本多芯片模块。作为基板的硅片通常厚度大约500微米，小芯片的尺寸从1 x 1毫米到40 x 40毫米。最困难的工序是对蚀坑深度的控制。

‘Chiplets’ Create Multi-Species MCMs

Keith Gurnett and Tom Adams

An elegant etching and metallization process for inserting and interconnecting tiny chips.

Ed.: For the complete article, visit circuitsassembly.com

A new and somewhat daring method for packaging devices is under development at an unknown number of locations in the U.S. and U.K., and probably in other parts of Europe as well. The new technology involves etching a pit of the correct depth and size in the surface of a silicon wafer, then inserting a tiny patterned chip (sometimes called a “chiplet”) into the pit. The chiplet is then interconnected with other nearby chiplets (**Figures 1** and **2**).

The overall purpose of this approach is to build what amounts to a low-cost multichip module at the wafer level. Some early research has placed silicon chiplets into pits on an unpatterned silicon wafer, but a good deal of work also has been done in inserting chiplets of multiple species – silicon, GaAs, InP – on the same wafer. For applications involving laser, high frequencies, or high power levels, this opens up the possibility of placing silicon and III-Vs chiplets, as well as chiplets of other species, onto the same substrate.

Dr. Vincent Fusco at Queen’s University, in Belfast, Northern Ireland, is carrying out advanced work in this area. He uses 4" silicon wafers, into which he etches pits for inserting the smaller chiplets. To date he has used both GaAs and silicon chiplets. He has concentrated on the key processes – etching the pit, inserting the chiplet, and bonding the chiplet in place – and works at this point with whole wafers, without dicing the wafers into individual die.

The silicon wafer that is the substrate typically has a thickness of around 500 µm. The chiplets are of various sizes. GaAs chiplets range in size from about 1 x 1 mm to 2 x 3 mm; silicon chiplets are more variable in their dimensions. For etching the pits into which the chiplets will be inserted, the thickness of the chiplet is the most important factor, since Dr. Fusco interconnects the chiplets using standard photolithographic procedures for top-level metallization. GaAs chiplets, made by commercial foundries to Dr. Fusco’s design, have a standard thickness of about 100 µm, but silicon chiplets have variable thicknesses and must be measured before etching the pits.

The most difficult process is controlling the etched pit depth. Once the chiplet thickness is known, Dr. Fusco is able to control the depth of the pit to within a few microns, a degree of accuracy sufficient for successful metallization.

Etching precisely the right depth so that the top surface of the chiplet and the top surface of the silicon wafer are vertically within a micron or two of each other is difficult. By thoroughly characterizing the etching process, Dr. Fusco has been able to make the process highly repeatable.

Dr. Fusco selected the metallization process for interconnecting the chiplets because of its inherent simplicity. He notes that the interconnects could also be formed by spinning a relatively thick resist onto the wafer to accommodate greater height differences, and then laser-drilling and plating vias through the resist, but this method would add processing steps and increase complexity. Some researchers have interconnected chiplets with wire bonds, but Dr. Fusco theorizes that the metallization process he uses is less harmful to the chiplets than thermosonic wire bonding.

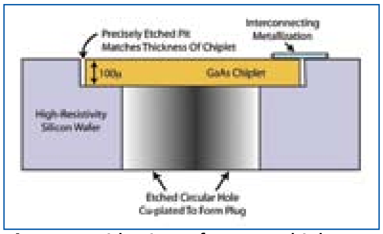


Figure 1. Side view of a GaAs chiplet inserted into a much thicker silicon wafer, and held in place by a copper plug electroplated from the bottom side of the GaAs chiplet. A metallization layer provides interconnects.

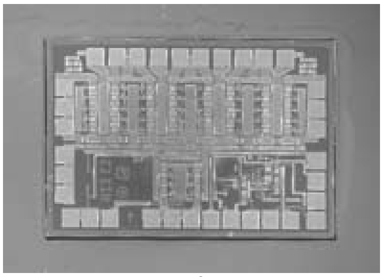


Figure 2. Top view of an 850 x 1270 µm GaAs chiplet inserted into a silicon wafer. The chiplet is slightly askew within the pit, creating gaps ranging from 4 to 18 µm, all of which are successfully bridged by the metallization layer.

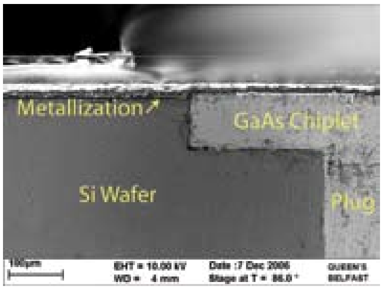


Figure 3. Cross-section through an assembly similar to that in Figure 2. The chiplet is about 100 µm thick, while the silicon wafer is about 500 µm thick.

Another critical step is bonding the chiplet within its pit. In early work, Dr. Fusco etched a hole in the bottom of the pit all the way through the silicon wafer, and then fastened the chiplet with an epoxy, but this bonding method had obvious thermal limitations. Currently, after etching the pit, Dr. Fusco carries out a second etch from the back of the wafer to form a via leading to the bottom of the pit. After the chiplet has been inserted into the pit, and temporarily stabilized by tape, copper is electroplated into the via, using the back metal contact as the seed layer.

The result is what amounts to a copper plug beneath the chiplet (**Figure 3**). The diameter of the plug is roughly half the diameter of the chiplet. The plug performs two functions: It holds the chip in position and acts as a heat removal device.

One of the reasons Dr. Fusco prefers to add a layer of metallization to interconnect chiplets is that the metallization can be laid across the small gap that typically exists between the sides of the chiplet and the walls of the pit. The pit, in other words, needs to be oversized by a few µm to simplify insertion of the chiplet. In actual production, Dr. Fusco doesn't foresee a need to fill this gap. Bridging the gap with metallization is similar to techniques used in MEMS devices to make floating beams. ■

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一种测试战略就是对电路板的大部分进行2维检验，然后对电路板的一小部分进行3维扩大缺陷检验，由于焊接点阴影，这是必要的。这个战略随着电路板的复杂程度提高，很快就失去作用了：一些研究显示，检验的重复率高达40%。提供高处理能力3维检验的X光设备可对电路板整体提供最佳检验，并能降低转换成本，而不必求助于抽样检查技术。本文还讨论了抽样检查技术。

Defect-Detection Strategies

James Benson

Today's operations require a high-speed 3-D approach.

Ed.: This article is abridged. For the complete version, visit circuitsassembly.com.

A system throughput increase has a direct impact on conversion cost by reducing the number of systems required to meet manufacturing volumes. Typically, throughput increases have come incrementally by increased efficiency in panel handling, image acquisition or image analysis. Increases in panel handling efficiency include faster movement of the panel within the system, panel vibration reduction and panel loader use. Image acquisition speed increases can include elements such as reduction in image overlap, parallel image capture, faster detector readout and improved x-ray to light conversion. Image analysis speed is typically addressed by using efficient analysis algorithms and by leveraging Moore's Law. As an alternative to increasing the basic speed of the system, some solutions rely on using a combinatorial approach of 2-D and 3-D x-ray inspection. 2-D x-ray inspection has been traditionally much faster than 3-D. This is achieved by using a large field of view (FOV). For single-sided or simple double-sided boards where the designer has followed strict design-for-x-ray guidelines, 2-D is an effective solution for detecting soldering defects.

A combinatorial strategy is to inspect most of the board with 2-D and then augment defect coverage with 3-D on a small portion of the board as necessary because of joint shading. This strategy breaks down quickly as the complexity of the board increases. In a recent evaluation of different board types, the percentage of overlapping solder joints caused by double-sided boards ranged from approximately 8 to 40%. The 8% was on a typical, low complexity automotive double-sided board. These boards are usually designed to be inspected by 2-D x-ray. This shows how difficult it is to design a double-sided board without overlapping solder joints. The combinatorial strategy can currently provide high throughput and high defect coverage on this type of product. In typical medium-to-high complexity communications products, 25 to 35% of solder joints are overlapping. Using 2-D alone on these products has an immediate and significant coverage loss. Furthermore, these overlapping joints are often spread throughout the board. This requires a significant amount of (much slower) 3-D inspection for coverage.

The general manufacturing trend of increased joint density is in conflict with the overall long-term success of a combinatorial strategy. To meet manufacturing needs then, high-speed 3-D inspection is needed. This approach would provide the necessary throughput to reduce the capital investment while still maintaining the high defect coverage provided by 3-D inspection.

To Sample or Not

Some manufacturers use either board- or device-based sampling techniques to increase automated x-ray inspection (AXI) throughput. The implication of any sampling strategy is that a user is trading off throughput against defect coverage. Several studies[2] have indicated x-ray inspection is the single best step for capturing solder-related defects. In many cases, defects detected cannot be found at any other test step. Therefore, the very nature of sampling in a continuous flow environment means that defects that would have been caught at x-ray are passed to the next test step. This is true of board- or device-based sampling. Thus, sampling can be an effective test strategy when the end product has three characteristics:

- Very high first-pass yield into ICT or functional test.
- High defect coverage at ICT or functional test.
- Low cost/risk associated with field failures.

Typically, repair cycles at either of these steps take longer than x-ray. At functional test, which typically has poor repair diagnostic resolution, repair time can be 10 times greater than repair time at x-ray. The second condition is necessary to reduce the number of escapes that will make their way to the end-user.

Manufacturing defect phenomena have traditionally been categorized as either systematic or random. Systematic defects can be those caused by situations like a clogged stencil at paste deposition or an incorrect reel at the pick-and-place system. These types of defect causes affect multiple boards in sequence. Typically, the earlier in the process that this type of defect cause is detected, the lower the overall repair cost. AOI-based solutions for solder paste or pre-reflow inspection have been developed specifically for finding these structural types of defects quickly and efficiently. As the name suggests, random defects have no readily identifiable cause. The frequency of this class of defect, product cost and overall warranty cost of an escape drive the manufacturing defect containment solution. X-ray has been shown to be an excellent solution for capturing the broadest range of defects. The level of sampling at x-ray directly correlates to the number of random defects that escape to the next test steps. The following formula[3] approximates the turn-on rate based on the number of defect opportunities (n) and the defect rate of the process (DPMO).

$$\text{Yield} = [1-(\text{DPMO}/10^6)]^n$$

This formula is a reliable predictor of yield for totally random defects. **Figure 3** shows the estimated yield of a board with 20,000 solder joints; an excellent solder joint defect rate of 50 DPMO will have a turn-on rate of about 37%. Without a solution to effectively detect these defects, the result will be a large number of boards failing functional test or escaping to the end-customer with the potential for field or warranty failures. ■

James Benson is AXI product marketing engineer at Agilent Technologies (agilent.com); jim_benson@agilent.com.

在最近举行的2007年Circuits Assembly服务优秀奖比赛中，Mack Technologies在营业额为1-5亿美元的电子制造服务供应商级别中，获得4个奖项。在最近的采访中，该公司说明了为什么只获得五个奖项中的四项，意味着公司明年有了明确的目标。客户确定了该公司需要增强服务的几个领域。根据客户的反应，该公司采取了一些步骤，如购买设备以进一步降低制造成本，并增加了一个新职位，确保对询价的答复能够满足客户的期待。

‘If We’re Not Number One, We Have Work To Do’

Chelsey Drysdale

Mack Technologies’ unique brand of customer service.

In the just-held CIRCUITS ASSEMBLY 2007 Service Excellence Awards contest, Mack Technologies collected four awards in categories for EMS providers with revenues between $100 million and $500 million. The company won outright for dependability, manufacturing quality and technology, and tied for value for the price in the program, in which customer responses determine the winners.

In a recent interview with Will Kendall, Mack vice president of sales & marketing, the first comment he made was an incredulous, “Winning four out of five awards means that we have a clear goal for next year!” After speaking to Kendall about Mack’s customer service program, I realized that Mack’s motivation to continuously improve stemmed from an unwavering company goal to please its customers. Being number two is not Mack’s goal. Says Kendall, “If we’re not number one, we have work to do.”

Mack director of sales and marketing Dion Wixted accepts the company’s SEA awards from CIRCUITS ASSEMBLY editor-in-chief Mike Buetow.

Kendall commented that the SEA survey information is diligently reviewed and used to improve the company. Survey responses are shared with the management team, and any areas needing attention are addressed as action plans. After plans are made, the team shares them with the rest of the organization.

“Even though we won three awards in 2006, customers identified several areas for Mack to enhance our services. Based on customer responses, Mack created new positions and invested within the company to strengthen capabilities customers had requested. For instance, we have invested in additional equipment to further drive cost out of our manufacturing processes and have added a new position to ensure requests for quotes are returned within customer expectations. Right now we are in the process of analyzing this year’s survey results to determine if there are any consistent themes,” Kendall said.

Based on points made in last year’s surveys, Mack created new positions within the company to strengthen areas that needed improvement. And on a micro level, Kendall noted that Mack looks at customers who responded to the surveys to address their specific concerns.

Kendall delved deeper, explaining the importance of customer service to his organization. “We have a very formalized customer feedback process. The information we received from the CIRCUITS ASSEMBLY awards surveys was consistent with our internal program.”

Mack’s customer satisfaction program is a top priority that is "ingrained into the culture" of employees. The company solicits feedback with a scorecard every quarter with an extensive series of 20 separate categories. The scorecards are then reviewed as an organization and posted for all employees to see. Kendall explained, "We use our customer feedback process to ensure our priorities are in sync with our customers' priorities."

Mack also performs quarterly business reviews with customers, a way to pause from day-to-day operations to take in the big picture. "What do our customers need and what are we providing for them?" they ask. Mack takes it one step further. The corporate-wide compensation plan is directly linked to customer satisfaction; it is equally weighted to financial performance to determine bonuses. The scorecards and anecdotal feedback help determine how the overall organization is compensated. What better way to make customer needs important?

Management is firmly behind this concept. "Our core belief is that we should partner with companies that have a good long-term fit with our organization, and then work hard to ensure we exceed their expectations for cost and service," Kendall asserted. "We want to be their best supplier in our industry."

EMS companies planning to participate in the 2008 SEA awards take note: Mack has a reputation to uphold and they're out for gold next year. In the meantime, Kendall has ordered extra 2007 plaques to proudly display in all its facilities. ■

Ed.: This is the first in an ongoing series looking at the 2007 SEA winners. For information on the program, visit circuitsassembly.com/sea.

Tech Tips

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Finding the Short

A transistor was failing. What was the cause?

A dual die transistor was shorting between pins 1 and 2 and between pins 4 and 5, (source and gate on both die, **Figure 1**). Shorts between pins 1 and 6 and pins 2 and 6 were present (source and drain and gate and drain on die 1). The drains are located at pins 3 and 6.

Test methods. The failed transistor was removed from the assembly along with a tape section of good components. The pin–to-pin I-V characteristics for the failed and good transistors were confirmed with a curve tracer. The good and failed transistors were soldered upside down (based on the components' wire-bonding, which was bottom-side, per Figure 1) onto HASL-coated copper coupons. They were then decapsulated using a controlled combination of fuming nitric and fuming sulfuric acid. The decapsulated components were examined optically and by SEM to determine evidence of the failure mode and mechanism.

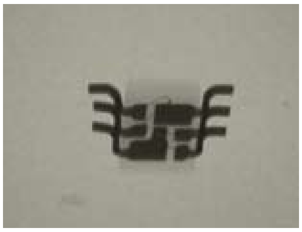

Figure 1. Oblique angle x-ray image of good part indicating typical wire bonding.

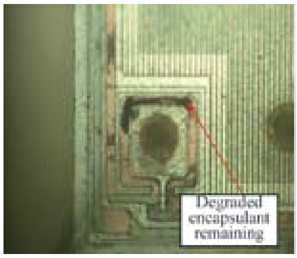

Figure 4. Metallographic microscope image of die 2 from failed transistor after decapsulation.

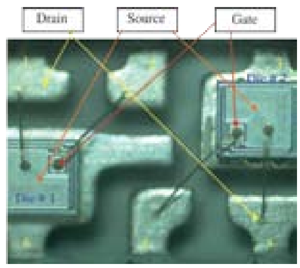

Figure 2. Metallographic microscope image good transistor after decapsulation.

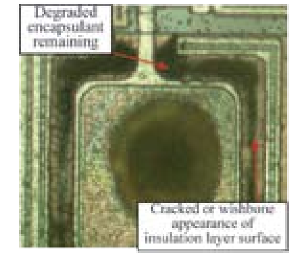

Figure 5. Close-up metallographic microscope image of die 1 from failed transistor after decapsulation.

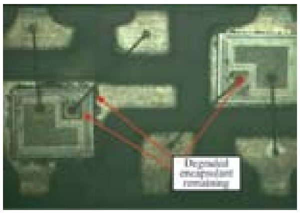

Figure 3. Metallographic microscope image failed transistor after decapsulation.

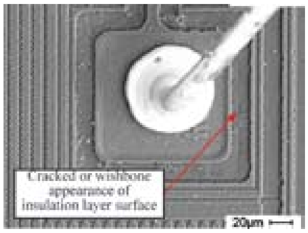

Figure 6. SEM image of die 1 at 450X.

Results

- Based on the component circuit diagram (technical data sheets), the substrate is tied to the source lead.
- Based on x-ray imaging, the wire bonds were oriented from underneath (Figure 1).
- Curve tracer analysis indicated a short between the gate and source, drain and gate, and source and gate on die 1. Die 2 showed a short between source and gate and drain and gate. Drain and source curves for die 2 appeared typical.
- The drains, gates and sources are identified in **Figure 2**.
- Residual degraded encapsulant was present after extensive decapsulating steps, indicating the material in this area was taken past its Tg (glass transition temperature), which is evidence of a thermal excursion (**Figures 3** and **4**).
- It was difficult to determine the presence of a specific failure mechanism (i.e., flash-over) because of the degraded residual encapsulant. However, die 1 appears stressed based on the cracked or wishbone appearance in the insulator layer areas where the degraded encapsulant resided (**Figures 5** and **6**).

Conclusions and recommendations. The shorts observed on the transistors are the result of an electrical overstress (EOS), most likely an overcurrent scenario as indicated by damage observed on the failed transistor. The cause of the EOS could be from a number of the following:

1. Use of the component outside of its recommended specifications.
2. No current limiting designed into the board to prevent a circuit load from damaging the assembly.
3. Transient voltages in the circuit that could cause short durations of currents above specifications.

The encapsulant degradation suggests an overcurrent scenario over an extended period of time.

As part of failure mode analysis, we recommend examining the circuit application for possible sources of overvoltage and overcurrent. In addition, a review of the specification requirements/limits for the transistor in this circuit is recommended. ■

American Competitiveness Institute

The American Competitiveness Institute (aciusa.org) is a scientific research corporation dedicated to the advancement of electronics manufacturing processes and materials for the Department of Defense and industry. This column appears monthly.

Allowable Concentration of Contaminating Elements in Solder

Impurities are harmless unless their level goes too high.

When discussing contaminating elements in solder, we must first make a distinction between the levels in virgin solder delivered by the supplier and solder in use in the solder pot.

In this document, we define "contaminating elements" as those elements not deliberately added to the solder but remain after the solder refining process during production. These contaminating elements are also called impurities. Although the name suggests they are harmful, in fact they are not, unless the level of these elements becomes too high.

For new solder, during the past decades, the level of elements that is not deliberately part of the alloy (impurities) is steadily decreasing to very low values. This is because solder manufacturers are now able to refine solder to a higher purity level.

There was not, however, a direct technical need to reduce these numbers in view of any effect on the solder process or joint reliability. In fact, there are two reasons for better refining: One, new refining technologies make it possible to produce solder with lower impurity levels. Because this might constitute a commercial benefit, these types of solder are promoted to the electronics industries.

The second reason is that, for Pb-free alloys, "impurities" are sometimes deliberately added to give the solder alloy special properties. Since such alloy compositions are in most cases patented, the competition is forced to keep those elements at a very low percentage so as not to infringe the patent.

For these reasons, we find in J-STD-006 for nickel, for instance, a percentage of only 0.01% as maximum impurity in new solder.[1] However, there are patented solders where this element is deliberately added, although only in a low percentage, but well above 0.01%.

A few decades ago, percentages of up to 0.08% of this element were permitted in new solder. Even at that percentage, the solder process could run without difficulty, making perfect and reliable joints.

So much for new solder alloy compositions. What about solder in use in the wave soldering pot?

Regarding the maximum contamination allowable for the solder in use, most suppliers could not provide exact data. If data are provided, then these numbers are always on the safe side. One reason for this is that the solder supplier will not be held responsible for any claim if solder is used with a higher contamination level than what they advise as maximum impurity level. The second reason is that they live by selling solder, so it is also partly in their interest if the solder has to be exchanged.

Exchanging Solder

During use, each solder alloy will, in due time, reach a new equilibrium as a result of dissolving elements introduced by the soldered metals. But at the same time, the joints formed and the dross that is removed also take out this solder. On the other hand, we have the addition with new solder to compensate the solder taken from the pot. In fact, this newly added solder will partly "refresh" the solder in the pot.

In practically all cases, this equilibrium of "contaminated" solder is fine to use without the need to exchange it. Joint formation and reliability will not be affected by minor changes in the solder composition as a result of this "contamination."

An exception might be the copper content in a SAC alloy. If too much copper is added as a result of dissolved material from leads or the board, it might change the melting characteristics of the alloy. Too much copper in the solder might also promote the formation of CuSn crystals. These needle-shaped crystals may increase the risk of solder bridging.

When beginning with a new process, it is normal that within a few months' time, virgin solder will reach its contamination equilibrium in a solder pot. Normally there is nothing to worry about as this happens; it is simply part of the process of using solder for wave soldering.

The results of the soldering process itself should be the decisive factor if one should worry about solder composition. Normally, one should analyze the solder only in cases where the quality of the solder alloy is in doubt.

For more detailed information about the effect of different impurity elements in the solder, see R.J. Klein Wassink, *Soldering in Electronics*, second edition, Chapter 4.4. ■

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References

1. J-STD-006B, *Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications*, January 2006.

Continued from pg. 29

the alloy's highly corrosive nature. But, based on the selection of a new alternative Pb-free alloy, this "part upgrade" step could be eliminated. This in turn would help reduce initial Pb-free capital changeover costs required.

7. Until the reliability of a PTH joint suffering from extensive copper dissolution is known, a minimum copper thickness specification at the knee is essential to ensure highly reliable PTH solder joints.

8. Copper dissolution could occur only on a few barrels within a connector, indicating variation in the degree or amount of copper dissolved, which is dependent on individual barrel characteristics. Typically, barrels within the connector center are first to be affected. This correlates to an increased turbulent flow rate and alloy temperature within this region.

9. It is possible for 100% dissolution to occur solely at the knee location, which represents a hidden defect difficult to locate during visual inspection. There are visual indicators that occur when dissolution occurs. Being able to locate these indicators during visual inspection will help catch any defective boards and out-of-control processes.

Future Work

Results from this study indicate that to replicate conventional SnPb equipment, methods and techniques, a change from SAC305/405 alloy may be necessary during Pb-free PTH rework. Many alternative Pb-free alloys are available; it is necessary to study a larger number to determine the most suitable option. Further studies will examine several other alternative Pb-free alloys, and each will be compared against results of the SnPb, SAC305, SAC405 and SnCu0.7CuNi0.05 alloys studied in this paper. Various aspects of each alloy will be examined, such as composition, melting temperatures, physical properties and cost. The alloy choice will be based on the final copper dissolution rate results, as well as comparing the above alloy attributes.

Future work will also include performing reliability studies, including ATC and mechanical testing, to further understand the impact of copper dissolution on PCB reliability. This will include both pure and mixed conditions. There is a large amount of data available on solder joint reliability using SAC305/405 alloy, but further testing will be required if an alternative Pb-free alloy is chosen for PTH processes.

Acknowledgments

The authors gratefully acknowledge the participation of IBM in this study. Their involvement and collaboration in this project was invaluable and an important part of its success. A special thank you to the following persons for continued support and commitment to this study: Jim Wilcox, Jim Bielick, Phil Isaacs and Eric Kline at IBM; and Linda Scala, Thilo Sack, Irene Sterian, John McMahon, Mursalin Ahmed, Farrukh Ali, Jeffrey Kennedy, Brian Smith, Ivan Tan, Owen Clarke, Heather McCormick and Simin Bagheri at Celestica. ■

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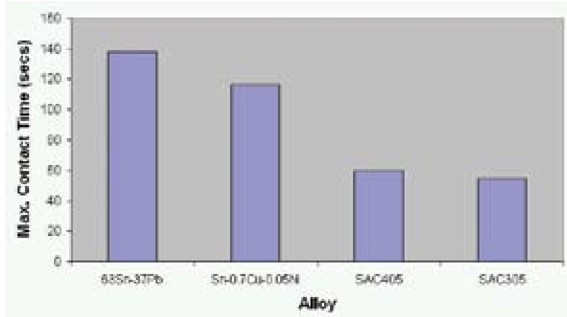

Figure 12. Process window by alloy.

References

1. Craig Hamilton, "A Study of Copper Dissolution during Pb-Free PTH Rework," CMAP, May 2006.
2. IBM Engineering Specification Second Level Assembly Solder Process, specification # 61X7093 EC H86836, November 2005.
3. Craig Hamilton, Laminar Flow-well, patent pending, May 2006.
4. Karl Seelig, "Pb-Free Solder Assembly for Mixed Technology Boards," Circuits Assembly, March 2006.

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The Power of Real-Time and Remote Information

While users stay at home, the technology evolution is taking them to new places.

The other day I heard about an experiment involving a family living without technology for a week. I did not notice the metrics on the experiment because I could not get over the thought of not having a cellphone or Internet access for a week. How would I survive?

I use technology all day almost everyday. It is integrated into my life. When shopping for a new item, I use the Internet for research. I consider everything from the product itself to service and support on the product; regardless, most of my research is done online. Rarely do I go to the store to comparison-shop anymore. By the time I arrive at the store, I know exactly what I am going to buy.

This, of course, applies to customers of all types, including test and inspection customers in the surface mount world. In February, I attended the Apex trade show, and while I have not researched the official attendance numbers, the buzz indicated that it was a bit slower than normal. The hypotheses are endless as to why this might be, but one interesting take was that engineers are using the Internet to do their research and thus did not go to the show for an in-person look at new equipment. While I agree that nothing will ever totally replace face-to-face, I wonder how much merit there is to this idea.

Businesses use the Internet and other remote technologies to add sophistication to their sales process. For a company to lack a Website would be unheard of today. At Apex, it was evident that digital means are in wide use: Precious few brochures and datasheets littered the show aisles. What else are companies doing to take advantage of the technology evolution, and how can it help users of test and inspection equipment?

At the show were several instances where creativity and technology wedded. One OEM conducted a product launch using a Web-camera to show the system in the company's laboratory thousands of miles away. Via the camera, potential customers watched and interacted in real time. Our booth conducted a remote demonstration on our x-ray product. Shipping the system is expensive, so we decided on a remote support services demonstration. We used a PC, via a WebEx online Web conference, to tap into a real system that resided offsite. In this case, we were able to show attendees a real machine doing real inspections. In this case, it saved us money; imagine from a users' perspective how these technologies can be used to save time and money.

The use of remote support services using technologies like WebEx can be a big advantage for a contract manufacturer that lacks certain technical capabilities in-house. EMS firms typically require service and support immediately and often have more than one system to support. Lucent is an example of a company that uses remote support services. It has performed countless product applications remotely. This shortens the development cycle, cuts travel costs and charges, optimizes customer spending, and reduces the time to action.

Vin DiNunno, a supply base engineer at Lucent, had this to say about remote support services: "In addition to cost savings, it has increased flexibility," he said. "There have been times when we would arrange to have an applications engineer fly to a site, only to find the boards not ready for inspection. The AE would have to wait for the boards to be readied." There were also cases, he added, "in which our contract manufacturers would have to ship the boards to an Agilent lab to be inspected for defects, and then shipped back – both costly and time-consuming."

Looking at other ways the Internet is helping test and inspection system users, I've noticed an increase in the use of Web-based trainings or Webcasts, not to mention the podcast boom. The idea of having an unlimited amount of individuals attend a free online seminar is a great one. You can appeal to a broad audience and teach about something they need for success – saving them money and time (no travel)!

The technology boom and its benefits to end-users are infinite. As you read this, some process engineer is receiving an email or text message indicating that a system on a production line is reaching its control limits. Preventing defects by acting on the data real-time will save countless dollars, and it is enabled by technology.

While we will never really know if Apex attendance was influenced by technology's constant reach, we can be certain that test and inspection equipment users will use such means to their advantage to cut costs, build profits and improve efficiency. It is an exciting time to be among technologists enabling users to save time and money as the technology evolution takes capabilities to new places. ■

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NEPCON South China 2007

Pb-Free Lessons Learned

Fictions of Pb-Free Surface Mounting

New components have no SnPb history, making it important to keep process chemistries up to date.

The thing I love most about surface mount is that it never gets boring. The drive for miniaturization continually requires smaller footprints and higher I/O densities. As soon as production technology refines the process for a new package to the point where yields are respectable, a smaller, more challenging product comes online. When I started building circuit boards, in 1990, our advanced manufacturing group was working on developing assembly processes for 0.020" pitch QFPs and 0603/0402 components. Fast forward 17 years and today's advanced manufacturing groups are in wafer-level chip-scale package, dual flat no-lead (DFN) and package-on-package (PoP) devices. And 01005 chips (one-sixth the footprint of those seemingly tiny 0402s) are in full production in some high-end consumer products!

The miniaturization road has been a fun one, but while the supporting technologies – packaging, PWB fabrication, assembly gear and process control tools – have evolved to support the efforts, one thing remained constant: the SnPb solder used to put it all together. Engineers intuitively understood the behavior of SnPb solders, and they could rely on that intuition to manage and improve mass-soldering processes. The SnPb alloy was the cornerstone of those processes. While the switch to Pb-free alloys changes some of the fundamentals of how we build circuits, it can easily cast doubt over all aspects of the new process.

A few months ago we examined some Pb-free wave soldering rumors. Now it's time to tackle similar rumors that have circulated regarding SMT:

Pb-free solder pastes do not print as well as SnPb. Fiction. To the contrary, newer Pb-free pastes often demonstrate better print properties than their SnPb predecessors. With no-clean pastes, material behaviors like stencil life, response to pause, transfer efficiency and volume repeatability now meet or beat those displayed by best-in-class SnPb products against which they are benchmarked. Product developers now have about five years' experience when it comes to working with SAC alloys, and have developed some impressively clever techniques to balance paste performance properties.

While it is true that many first- and second-generation Pb-free solder pastes were deficient in numerous areas, available commercial products are vastly improved. When reviewing print capability studies, note the date of publication or the generation of paste that was the subject of the study. Anything published more than two or three years ago likely reflects a technology state that has since been surpassed.

Pb-free solder pastes produce more voids than SnPb. Fiction. By volume, solder paste is approximately 50% flux and 50% metal. Voiding is predominantly a function of the flux. If certain volatile components of the flux do not completely outgas before the metal melts, voids will be created. But just like print properties, Pb-free pastes' voiding properties have come a long way. A study in Circuits Assembly, January 2007, compared voiding properties of two leading SnPb and Pb-free pastes on a variety of BGAs. Voiding rates observed in the Pb-free system were no greater than in the SnPb control. In most cases, slightly fewer voids were seen in the Pb-free products.

When moving to Pb-free reflow soldering, this basic principle holds true: To burn off volatiles and minimize voiding, some solder pastes perform better under soak profiles in the reflow cycle. Others perform just as well under ramp profiles. It depends on the constituents in the flux. The process engineer needs to understand the voiding sensitivity of a solder paste to its reflow profile prior to developing production processes.

More paste will be needed in intrusive reflow applications due to Pb-free products' lower metal content. Fiction. The 50:50 ratio of flux to metal remains constant in both SnPb and Pb-free solder pastes. The confusion stems from the way metal loading is expressed in product descriptions. It is indicated as a percent weight, not percent volume, because percent weight is a more precise measurement.

SAC alloy is less dense than SnPb alloy, so a certain volume of SAC weighs less than the same volume of SnPb alloy. To maintain the 50:50 ratio of flux to metal, the same volume of SAC solder powder equates to a lower weight percent (88-89%) in the final product than in SnPb (89-90%). Be assured that printing the same volume of paste from the same stencil aperture will provide the same amount of metal to fill the barrel and create the solder joint.

Continued on pg. 46

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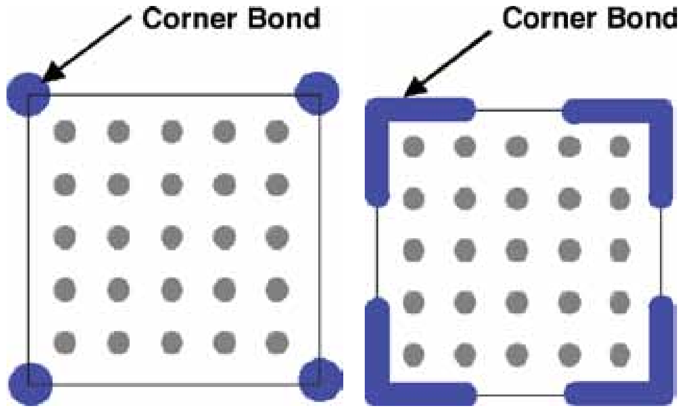
Materials World

使用CSP 边角加固技术节约时间降低成本

在当今竞争激烈的市场环境下，即要降低成本又不牺牲质量，是每个商家共同追求的目标。这对电子封装行业也不例外，使用不同的材料，选择不同的供应商，以及改变生产工艺流程，是许多封装工程师经常考虑并付诸于实践的方法。事实上，即使在每个元器件上节省几分钱都有可能对整个生产成本形成重大影响，特别是对于EMS厂家，这可能意味着赢得或失去订单。

从材料的角度考虑，有几种因素影响一个组装厂的材料成本。当然，首先是原材料的价格，但是同样重要的是应用材料的方法。俗语说，“时间就是金钱。”如果生产周期和生产量得以改进，例如减少一步生产工序，那么该产品的总体成本也随之减少。传统的CSP加固方法使用底部填充剂，需要点胶和固化工序。相对而言，这两个工序都是很慢的过程，而且有可能需要额外的设备投资。与之传统方式相比，CSP边角加固技术(cornerbond)具有节省材料和减少工艺流程等特点，正逐渐赢得各组装厂家的青睐。



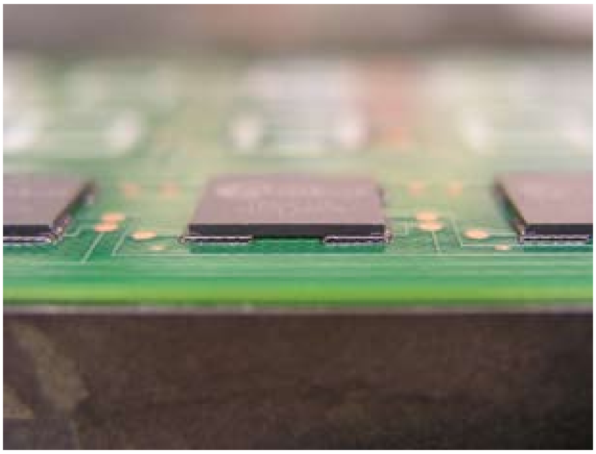


图1显示如何使用CSP边角加固材料。在放置CSP元件前，首先在电路板上点胶，点胶的形式可以是点状或线状，位置可以是在CSP的角、边、或者其他任何可以利用的空间。下步工序是放置CSP元件，最后经过回流炉形成焊点连接，同时在此回流工序，材料完成固化。图2中是使用该技术组装的CSP样本。这种技术的最大优点之一是使用普通的组装工艺流程，利用现有的设备，不需要附加的材料固化设备。另外，最新的边角加固材料具有允许元件自我校正的特性，用以校正元件放置过程中所产生的误差，最终实现改进长期可靠性能和组装产出率。与传统的底部填充剂相比，边角加固工艺省略了组装后的点胶和固化工序，节约了附加的设备费用，并且提高了整个流程的生产效率（UPH）。加之有些材料可以允许返工维修，当只有一个或很少的有缺陷的元件存在时，生产厂家可以不必丢弃整个组装器件。综上所述，由于设备的节约及循环时间的显著减少，边角加固技术使得厂家得以有效地降低总体生产成本。

虽然 CSP边角加固技术有很多优点，但它并不适用于所有的应用。对于某些手持式产品，如移动电话或便携式音乐播放器，需要较高的抗冲击性能，底部填充剂仍然是最好的选择。但是对于其他的可移动产品如笔记本电脑或台式计算机以及游戏机等，采用边角加固技术足以消除产品在运输过程中震动引起的可靠性能的隐患。

正如其他任何工艺一样，使用这项技术时，为了达到预期的效果，一些关键环节必须加以考虑。例如某些边角加固材料需要紫外光来固化，则应该折衷地考虑材料的使用及其他形式的可靠性能的需要。当材料位于元器件之下，即使使用足够强的紫外光，由于元器件的屏蔽作用，光线不能照射到胶体的深部，所以存在材料不能完全固化的可能性，从而导致产品的可靠性能的降低。另外，在使用回流之前点胶的工艺时，焊盘的设计及点胶的准确性尤为关键。然而如果应用得当，这项技术对于CSPs 和BGAs的加固是一种非常理想的解决方案。

总体而言，对于中等应力情况下的CSP元件的组装，边角加固技术提供了优秀的机械保护。它综合了简便、经济以及可直接用于生产线的优点。对于寻求节省开支并要求CSP产品具有较高的长期可靠性能的厂家，边角加固技术是一个理想的选择。 ■

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For the English version, visit circuitsassembly.com.

High Power-to-Board Interconnects

PES/PET Series high power-to-board interconnect system comes in 0.250" pitches; PESC/PETC Series comes with signal pins of 0.100" pitch. Rated for applications up to 28A at 80°C and has up to eight blade style contacts. Forty signal pins are standard and can handle up to 3A of current at 80°C. Powerstrips are available for parallel board spacings of 19 mm, and for perpendicular and coplanar board interface applications. These polarized PTH connectors can be used for rugged applications; right-angle versions have screw-down features for added ruggedness. Are RoHS-complaint and suitable for Pb-free processing.

Samtec, samtec.com

High-End PCB CAD

Board Station XE leverages customers' existing IP, such as libraries, design data, and design capture infrastructure. This extended design flow is added to existing Board Station design environment. Said to offer the productivity design features found in AutoActive placement, routing and manufacturing environment; integrated access to the Topology Planner/Router and XtremeAR and XtremePCB applications. Leverages Board Architect schematic capture tool and is integrated with Library Management System, Data Management System, I/O Designer and the Constraint Editor System. Also integrates ICX Pro, ICX, HyperLynx and Quiet Expert.

Mentor Graphics, mentor.com

1.3 MP Camera SPI

The SI-C1500 SPI is said to be capable of high-speed, accurate post-reflow visual inspection. Features Mosiac color processing software that reportedly enhances detection accuracy and speed. Said to extract color elements from each board and identify defects based on color contrast. Features a 1.3 MP color CCD camera. Can view angle-mounted components.

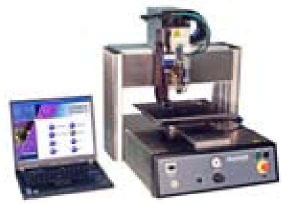
Sony, sonysms.com

Wave Soldering System with Advanced Preheat

VectraES wave soldering system has a new, servo-controlled reciprocating spray fluxer with an air atomized spray head, pressurized tank flux supply system, self-cleaning nozzle and the ability to spray in one or both directions with recipe control. New preheat technology, is a one-piece module said to provide exceptional thermal performance and minimize cross-board and top-to-bottom product temperature differentials. Nozzles are 40% wider, for increased contact and dwell time. Reportedly reduces dross 40%.

Speedline Technologies, speedlinetech.com

Automated Batch Dispenser



DispenseMate D583/585 automated dispensing system is WEEE/RoHS compliant. Designed for batch production dispensing processes, including solder paste, conductive adhesives, surface mount adhesive, gasketing, sealing and silicone/epoxy encapsulation. For labs, new product development and prototyping. The 583 model has a dispense and vision area of 325 x 325 mm; the D-585, 525 x 525 mm. An advanced height sensor automatically checks for warped parts and inconsistencies. Optional pattern recognition and CAD import.

Asymtek, asymtek.com

Pb-free Compatible Underfill

Loctite 3536 high flow underfill fills spaces beneath CSPs and BGAs. Said to cure rapidly at low temperature, minimizing thermal stress to other components and permitting inline curing. Protects solder joints against mechanical strains such as shock, drop and vibration. Is compatible with Pb-free solder materials.

Henkel, www.henkel.com/electronics

2-Way Ionizer

The Stablo EX two-way ionizer reportedly generates a balanced mix of positively and negatively charged ions that eliminate static on lab samples, allowing them to be weighed accurately with high repeatability. Uses AC voltage to power its corona. Said not to create an inverse charge. Weighs 110 g. Can be handheld or attached to adjustable mounting stand.

Shimadzu Scientific Instruments (SSI), ssi.shimadzu.com

SMD Test Probe

The PCB Test Arm Probe provides quick, easy SMD probing. Connects a test instrument, such as an oscilloscope, to a variety of SMDs including PLCC, SOIC, QFP, and VIAS or test point holes. Heavy base and flexible shaft make positioning to a test point simple. Has spring-loaded tip, rotatable head and fine vertical adjustment knob. Comes in 3A and 10A models. Used with a thermal imaging system, can help locate low Ω shorts.

OptoTherm Inc., optotherm.com

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Product SPOTLIGHT 产品

Small Footprint Solder Recovery

EVS 1000 solder recovery system is a smaller, lighter version of the EVS 3000/6000, with all the recovery performance of the standard and Pb-free solder units. Converts waste dross into pure solder in minutes while improving the wave solder machine process. Has a dross capacity of 10 lb. For users with one to three wave solder machines and who regularly dedross or use nitrogen to reduce drossing.

EVS International, solderrecovery.com

3-D Inline Automated X-Ray

Medalist x6000 3-D inline automated x-ray is said to double line throughput. New software incorporates several automatic test development features to facilitate programming development. Handles panels of 4 x 5" to 18 x 24" and up to 0.125" thick. Achievable false call rate of 500-1000 ppm. Minimum feature detection capabilities are 0.012" for joint pitch, 0.0018" for short width and 0.0005" for solder thickness.

Agilent Technologies Inc., agilent.com/see/axi

Pb-Free Lessons Learned

Continued from pg. 42

While on the topic of intrusive reflow, here's another basic principle that carries over directly from SnPb: A paste with a propensity to hot slump is highly undesirable, as it can drip through the holes in the PWB, leaving less metal in the hole to form the solder joint and more in the reflow oven to clean later on. When looking at reflow profiles to minimize voiding, hot slump properties – which can also create solder bridges and mid-chip solder balls – should balance the considerations.

If Sn-rich solders attack stainless steel, are nickel stencil foils and squeegees necessary? No. I have to admit, I chuckled when I heard this one. But it is a good illustration of how such a considerable change can lead us to question some of the basics. Concerns over Sn-rich solders attacking stainless steel apply only to the solders in their molten states; thus it is a concern only for wave-soldered and reworked hardware. Pb-free solder pastes have been printed with stainless stencils and squeegees for years with no signs of accelerated erosion.

Even back in the SnPb era, I was a strong proponent of keeping process chemistries current by requalifying soldering products every two to three years. When the most modern materials available aren't used, the process engineer can waste a lot of time resolving issues that have already been solved by next-generation product. Although the focus of this column is on solder paste, the same principle applies to flux, adhesives, cleaners, rework products, even conformal coatings. Understandably, it is difficult for high-reliability assemblers to convert process chemistries because of the high costs of qualification. However, for the majority of assemblers, costs incurred by the qualification of new materials are quickly recouped by the mitigation of defects that result from the change.

This months' lesson learned? It is more important than ever to keep process chemistries up to date. Nearly all Pb-free soldering products have improved by leaps and bounds during the past three years, and the vast majority of new products in development are Pb-free. Those 01005 chip components mentioned earlier were never soldered with SnPb. They entered production with a Pb-free solder paste that was designed to repeatably print those 0.007" feature sizes and reflow them in air. And the products being designed for WLCSP, DFN and PoP? All Pb-free. It's conservative to predict that by the end of 2008, Pb-free pastes will completely outperform SnPb in every performance category measurable. Except for maybe one: spread on copper. That's one of the unfortunate facts of Pb-free SMT that we'll explore next month. ■

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In Case You Missed It

Conformal Coatings

"Parylene as a Suppressant for Tin Whiskers Growth on Printed Circuit Boards"

Author: Rakesh Kumar, Ph.D.; rkumar@scscoatings.com

Abstract: Numerous studies identified several strategies to mitigate tin whisker risks until a method is found to completely eliminate the problem. One mitigation strategy is conformal coating application. This paper reviews various options and presents a practical solution using Parylene coating technology for suppressing formation of metallic whiskers, OSEs and dendrites. It has been observed that Parylene conformal coatings are more suitable for suppressing metallic whiskers than other conformal coatings or other proposed solutions. (Apex, February 2007.)

Pb-Free Rework

"The New Lead-Free Assembly Rework Solution Using Low Melting Alloys"

Authors: Polina Snugovsky, Ph.D., S. Bagheri, Z. Bagheri and M. Romansky; polina@celestica.com

Abstract: This paper describes a new Pb-free SMT rework process that avoids component overheating, reduces board warpage and cratering, and prevents adjacent components from thermal damage. A solder alloy with a melting range lower than SnAgCu solder is used to replace a BGA on an organic substrate. The Pb-free solder pastes analyzed include two indium-containing alloys, melting range 181-187°C and 138°C, respectively, and a bismuth-containing alloy, melting range 195°-209°C. In this work, CBGA937, PBGA196 and CSP46 components with SAC405 balls were assembled using SAC405 solder. Then, rework was performed with three compositions of low-melt solders using different profiles.

The microstructures of mixed solder joints were analyzed using optical and scanning electron microscopy methods. Two solder pastes and rework profiles were chosen for thermal cycling. A limited ATC study was done in a temperature range of 0-100°C. It was observed that fatigue life was component-dependent, and when fully mixed, solder joints had better or equal reliability to that of the pure SAC405 assemblies. (Apex, February 2007.)

Surface Finishes

"Effect of OSP Chemistry on the Hole Fill Performance During Pb-Free Wave Soldering"

Authors: Bala Nandagopal, Sue Teng and Doug Watson; sue.teng@cisco.com

Abstract: This paper analyzes the differences in plated through-hole fill performance between the regular OSP and Pb-free OSP PCB surface finish chemistries in a Pb-free wave solder process. Variables studied include two board thicknesses (0.093" and 0.125"), three hole sizes (pin plus 0.016", 0.024" and 0.040"), internal copper layer connections (single and three plane layer connections), two pin shapes (circular and rectangular), and two reflow atmospheric preconditions (nitrogen and air). The bare PCBs were initially subjected to 220° and 240°C peak reflow process twice for the SnPb and Pb-free wave soldering samples, respectively. Pb-free wave soldering results indicated that the Pb-free OSP performed better than the regular OSP chemistry by 15% under air and 40% under nitrogen reflow preconditioning. In Pb-free wave soldering, the air preconditioning resulted in better hole fill than nitrogen. Board-to-board variation of hole fill was much lower in the Pb-free OSP chemistry compared to regular OSP. PTH sizes of 0.040" and 0.016" larger than the pin diameter proved to be best and worst designs, respectively, for the 0.125" PCB. The SnPb control almost had greater than 92% average hole fill for every design variable in this experiment. Overall, the results indicated that the regular OSP chemistry in Pb-free wave soldering failed to meet the 50% hole fill required per IPC-A-610, for all the conditions studied. The 0.125"-thick PCB using Pb-free OSP chemistry also failed to meet the IPC requirements for all conditions evaluated. However, the 0.093"-thick PCB using Pb-free OSP chemistry was able to meet this 50% hole fill requirement (although not meeting the general 75% minimum requirement), except when the hole diameter is 0.016" larger than the pin. (Apex, February 2007.)

Test and Inspection

"Improving SMT Yield with AOI and AXI Test Results Analysis"

Authors: An Qi Zhao, Xin Yong Yu, Li Ming Gong, Zhen (Jane) Feng, Ph.D., Mark Evans and Murad Kurwa; jane.feng@flextronics.com

Abstract: This study started with one customer's product, which previously had 100% components covered with AOI and >95% covered by AXI. AOI, AXI, ICT and functional test data were studied for six months, and AXI test coverage reduced for some non-critical components. As a result of the reduction of AXI coverage, AXI test time was reduced to below three minutes from above four minutes. Also investigated were process issues and improvements using daily AOI and AXI test results. An example of one product: AXI test time was reduced by testing only BGAs, fine pitch ICs, RNs and some "critical to function" parts. Therefore, AXI component and pin coverage changed from 98.4% and 98.9% to 13.6% and 50.1%, respectively. AXI test time was reduced to 2 minutes from 4.1 minutes. Meanwhile, the yields of AOI (top), AOI (bottom), AXI, ICT, and FT increased from 98.9%, 97.3%, 88.4%, 98.9% and 100% to 99.6%, 99.0%, 96.2%, 98.9% and 100%, respectively. Cost savings are also discussed. (Apex, February 2007.)

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