
# *PRESS KIT*

## 2006

# ISSCC
# VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

# TABLE OF CONTENTS

# ISSCC 2006
# EXECUTIVE SUMMARY

- **Activities**
- **Conference Theme**
- **Significant Results**

# EXECUTIVE SUMMARY

## ACTIVITIES AT ISSCC 2006

- **Tutorials, presented Sunday, February 5:**
  - Nine independent lectures presented by experts from each of the ISSCC 2006 Program Subcommittees: Analog & RF; Data Converters; Digital; Imagers, MEMS, Medical and Display; Memory; Signal Processing; Technology Directions; Wireless Communications; Wireline Communications.

- **Advanced-Circuit-Design Forums, presented Sunday, February 5 and Thursday, February 9:**
  - Informal all-day linked interaction in which circuit experts exchange information on their current research.

- **Evening Sessions, presented on Monday and Tuesday, February 6 and 8 evenings:**
  - Seven Special-Topic Sessions
  - Three Panel-Discussion Session

- **Technical Paper Sessions, presented Monday through Wednesday, February 6 through 8:**
  - **Three** presentations in the Plenary Session on Monday morning
  - **33** paper sessions, beginning Monday afternoon and continuing through Wednesday afternoon, including:

    **255** regular-length papers

    **73** short papers

- **Social Hour on Monday and Tuesday evenings after the paper sessions:**
  - DAC/ISSCC and ASSCC Student-Design-Contest-winners poster session
  - Technical-book display

- **Short Course, presented Thursday, February 9:**
  - **Four** linked 90-minute lectures given by experts in the field

# CONFERENCE THEME:

## "Multimedia for a Mobile World"

Today, electronic multimedia is an indispensable part of life. Broadband Internet with megabit-per-second capability on copper has replaced the kilobit-per-second modems of the past. Digital music and video, as well as industrial data, run at the speed of light around the globe, for ubiquitous use in new consumer and new professional products and applications. The enablers of this media-revolution have been ever-deeper deep submicron silicon circuits, shrinking to nanometer dimensions, now providing cheaply the gigascale integration of IP in system-on-a-chip multimedia equipment. To mark this major transition, this year's Conference will highlight papers on new circuit techniques and devices supporting this mobile and multimedia tour of triumph for semiconductors.

Advanced semiconductor technology, wireless and broadband interconnection, multimedia applications, and real-time entertainment, are driving the semiconductor business today. But, circuit research is facing new challenges in the deep nanometer regime: CMOS devices with high-leakage gates and low-linearity performance, but with plentiful bandwidth, open new opportunities: Thus, we see converters at 65nm, and even-smaller-featured silicon, along with other devices like carbon nanotubes and large-scale applications of organic materials.

In support of the Conference theme, there are:

**Plenary Session, with three presentations :**

- Where CMOS is Going: Trendy Hype versus Real Technology
- ICs for Mobile Multimedia Communications
- The Future of Computing For Real-Time Entertainment

## Technical-paper sessions, amongst which are included:

- 3 sessions describing high-performance high-frequency ADCs and DACs **[Sessions 3, 12,31]**
- 1 session on new microprocessor developments including single-chip many-multicore processors **[Session 5]**
- 4 sessions on diverse RF applications **[Sessions 6, 11, 17, 25]**
- 3 sessions on DRAM, SRAM and non-volatile memory **[Sessions 7, 8, 34]**
- 4 sessions on low-power multimedia and mobile TV **[Sessions 9, 14, 22, 33]**
- 3 sessions on cellular telephony and WLAN **[Sessions 14, 20, 26]**
- 1 session on large-scale flexible organic ICs **[Session 15]**
- 2 sessions on concerns for power management and distribution **[Sessions 24, 29]**

## Evening Sessions, amongst which sample topics include:

- What is Driving Displays? **[SE1]**
- Power-Aware Signal Processing **[SE2]**
- Analog Scaling **[SE3]**
- CMOS RF Design at 90nm and Beyond **[SE5]**

## Advanced-Circuit-Design Forums, amongst which sample topics include:

- Wireless CMOS Transceivers **[F1]**
- Embedded-SRAM Design **[F2]**
- Multicore Architectures, Designs, and Implementation Challenges **[F6]**

## Tutorials, amongst which sample topics include:

- Data Converter: The Analog and Digital Ins and Outs **[T2]**
- Multi-Level Cell Design for Flash Memory **[T5]**
- Cellular-Phone Applications Trends and DSP Technology **[T6]**
- 3D Integration **[T7]**

# SIGNIFICANT RESULTS

## • ANALOG:

- High-efficiency class-D audio power amplifiers reach to new levels of fidelity at 100W+ power levels **[19.1, 19.3]**
- DC to 2.4 GHz power upconverter employs a multipath mostly-digital technique to cancel unwanted harmonics up to the 17$^{th}$, without filtering **[25.1]**
- Divider circuit in CMOS operates at frequency beyond 70GHz **[32.8]**

## • DATA CONVERTERS:

- Data converters for communication systems move closer to the antenna **[3.2, 3.3, 31.7, 31.8]**
- Nyquist ADCs achieve sub-pJ/conversion-step power efficiency **[12.1, 12.2, 12.3, 12.5, 12.7, 31.3, 31.5, 31.6]**
- 1GS/s ADC with new sampling technique pushes resolution to 11-bits. **[31.6]**

## • DIGITAL:

- Single-chip processors with up to 16 cores and 32-threads **[5.1, 5.2]**
- 65nm processors and processor components **[5.3, 5.7, 24.1, 24.7]**
- 1.2Tb/s aggregate bandwidth from a single chip **[5.6]**
- 9GHz processor components: 64-bit integer execution unit and register file **[5.7,24.7]**
- Circuit techniques for improved PVT tolerance **[24.7, 24.4, 24.5, 29.6]**

## • IMAGERS, MEMS, MEDICAL AND DISPLAY:

- A 32-site 4-channel cochlear-implant microelectrode array with inductively-coupled wireless link and position-sensing capability. **[2.3]**
- Low-power implantable retinal prostheses include a digitally-programmable stimulation scheme with ESD protection, achieving a data rate of 100 kb/s at 1.3 mW. **[2.4, 2.5]**
- A micromechanical silicon-on-insulator accelerometer with low-noise CMOS, achieves micro-gravity resolution in a wide dynamic range of 95dB to enable inertial navigation at micro-scale **[16.1]**

- A thermal oscillator in standard CMOS used as a temperature sensor, achieving an accuracy better than ±0.5°C over the industrial temperature range of-40 to 105°C **[16.5]**
- A 128x128 pixel CMOS image sensor inspired by the human retina images over a wide range of light levels while responding to relative intensity changes in less than 100µs. **[27.9]**

## • MEMORY:

- NROM-based flash memory achieves four bits of storage in a single memory cell **[7.1]**
- Smallest 8Gb multi-level NAND flash memory ever reported **[7.7]**
- 10MB/s program throughput achieved by a sub-60nm Multi-Level NAND flash memory. **[7.7]**
- Powerful 5-bit error-correction scheme embedded into a monolithic Multi-Level NAND flash memory. **[7.6]**
- 5Ghz SRAM design for high-performance CPU **[34.1]**
- Thyristor-based volatile memory in nano-scale CMOS **[34.6]**

## • SIGNAL PROCESSING:

- First-published DSSS UWB baseband transceiver for wireless ad-hoc networks. **[14.5]**
- 5mW MPEG4 video encoder and 160Kgate HDTV video decoder provide low-power and low-cost solutions. **[22.3, 22.6]**
- Vertex processor delivers 120Mvertices/s 3D-geometry performance which is 3x the performance and half the power of previous chips. **[22.4]**

## • TECHNOLOGY DIRECTIONS:

- First demonstration of functional RFID tags built in organics, operating at 13.56MHz **[15.2]**
- Electronic “nose” detects spoilage of wine at levels of 10 parts per million **[15.3]**
- Development of a Braille sheet allows e-books for the blind that update in 2 seconds **[15.4**
- Combination of 2.4GHz BAW resonators and 0.18µm CMOS radio front-end achieving 50dB image rejection with 1.8mW power consumption **[17.7]**
- Demonstrated generation of 1 microwatt of electrical power from a 1 milliCurie of benign Nickel-63 nuclear-energy source. **[23.1]**

- Demonstrated 1 Terabit per second data transfer between 3D integrated chips via inductive coupling over an area of 2 square millimeters and energy consumption of 3 picoJoules per bit. **[23.4]**
- Optical clocking of 5-to-10 GHz with a silicon nano-photodiode. **[23.5]**
- Neuro-interface chips locally process signals captured from 100 electrodes and radio-transmit them outside the body **[30.1, 30.2]**
- Realization of a MEMS-based reusable biosensor for identifying and monitoring cardiovascular-risk biomarkers (that is, C-Reactive proteins) **[30.6]**

## • WIRELESS COMMUNICATIONS:

- Fully-integrated UWB transceivers in CMOS **[6.4, 6.5]**
- A frequency synthesizer covering all the 14 UWB bands in CMOS **[6.7]**
- A 77GHz phased-array system in silicon **[10.1. 10.2]**
- A 60GHz transmitter and receiver in silicon **[10.3]**
- The first single-chip 802.11a/b/g SoC that fully integrates RF front-end, baseband analog, digital baseband, and MAC in one die for embedded applications. **[20.2]**
- A fully-integrated SoC for GSM/GPRS on 0.13μm CMOS **[26.7]**
- RF tuners for all the worldwide mobile TV standards. **[33.1 to 33.6]**

## • WIRELINE COMMUNICATIONS:

- 10Gb/s photonic modulator and WDM Mux/Demux with electronics in 0.13μm SOIC **[13.7]**
- 25Gb/s CDR in 90nm CMOS for high-density interconnects **[18.1]**
- 104Gb/s $2^{11}$-1 and 110Gb/s $2^{9}$-1 PRBS generator in InP HBT technology **[28.10]**

# ISSCC 2006
# CONFERENCE OVERVIEW

- **Events**
- **Paper Statistics**
- **Plenary Session**
- **Technical Highlights**
- **Discussion Sessions**
- **Short Course**
- **Tutorials**
- **Advanced-Circuit-Design Forums**

# *EVENTS*

**TUTORIALS** (SUNDAY, FEBRUARY 5, 2006)

- Nine 90-minute Tutorials, each taught two times, by individual circuit experts from the Program Committee, serve to meet attendees' needs for introductory material in circuit specialties.

**ADVANCED-CIRCUIT-DESIGN FORUMS** (SUN, FEB 5, AND THURS, FEB 9, 2006)

- In six circuit-design forums, circuit experts exchange information on their current research in an all-day informal linked-topic environment.

**TECHNICAL SESSIONS** (MON. TO WED., FEBRUARY 6 THROUGH 8, 2006)

- **Three invited talks** presented in the Plenary Session and **255 technical papers** presented in **33** Regular Sessions, highlight the latest circuit developments.

**EVENING SESSIONS** (SUN, MON. & TUES., FEBRUARY 5 THROUGH 7, 2006)

- Seven Special-Topic Presentations, in which multiple experts provide, linked insights and background on a subject of current importance.
- Three Panel Discussions in which experts debate a selected topic and field audience questions in a semi-formal atmosphere.

**SOCIAL HOURS** (MONDAY, FEBRUARY 6, AND TUESDAY, FEBRUARY 7, 2006)

- Opportunities to network with experts in a wide range of circuit specialties; to meet colleagues in an informal exchange; to view the Poster Session (see below); to browse the technical-book exhibits!

**POSTER SESSION** (MONDAY, FEBRUARY 6, AND TUESDAY, FEBRUARY 7, 2006)

- DAC/ISSCC and ASSCC Student-Design-Contest winners will provide poster presentations during the Social Hours.

**SHORT COURSE** (THURSDAY, FEBRUARY 9, 2006)

- Intensive all-day course on a single topic, taught by world-class instructors, can serve to "jump start" a change in an engineer's circuit specialty.

# *PAPER STATISTICS*

## OVERALL:

- **3** papers invited
- **680** papers submitted to ISSCC 2006
- **255** papers accepted, including:
    - **119** papers from North America, including:
        - **65** Industry papers
        - **54** University papers
    - **81** papers from the Far East, including:
        - **47** Industry papers
        - **34** University papers
    - **55** papers from Europe, including:
        - **26** Industry papers
        - **29** University papers
- **34** Sessions, over 3 days

## INTERNATIONAL SCOPE:

- Americas: **47%**
- Far East: **32%**
- Europe: **22%**

| TECHNICAL COVERAGE: | 2006 | 2005 | 2004 |
|---|---|---|---|
| Analog & RF | **13%** | **13%** | **13%** |
| Data Converters | **10%** | - | **-** |
| Digital | **11%** | **11%** | **12%** |
| Imagers, MEMS, Medical & Display | **11%** | 11**%** | **9%** |
| Memory | **7%** | **10%** | **11%** |
| Signal Processing | **7%** | 9**%** | **9%** |
| Technology Directions | **11%** | **12%** | **11%** |
| Wireless Communications | **15%** | **18%** | **16%** |
| Wireline Communications | **14%** | **16%** | **15%** |

# *PLENARY SESSION*

## [1.1] WHERE IS CMOS GOING: TRENDY HYPE VERSUS REAL TECHNOLOGY

**TZE-CHIANG (T.C.) CHEN**
*IBM Fellow, VP of Science and Technology,*
*T.J. Watson Research Center, Yorktown Heights, NY*

- CMOS approach toward atomistic and quantum-mechanical boundaries has motivated industry pundits to profile Nanotechnology, Bio-electronics, or Quantum Computing as urgently-needed CMOS replacements .
- New materials, coupled with effective circuit design and architecture practices ensure at least another 10 years of CMOS service.
- Power dissipation and variability emerge as first-order concerns which must be addressed effectively in design.
- Stochastic threshold variation caused by dopant implant variation in ultra-small inversion regions will give rise to 3-digit threshold variation by the 25-nm generation in excess of 100mV threshold variation. At the architecture level, initiatives such as self-healing systems, self-biasing substrates, and simultaneous circuit and device diagnostics will extend a circuit's ability to survive and function given a wider range of sensitivities.
- The development of silicon technology has been, and will remain, driven by system needs.

## [1.2] ICS FOR MOBILE MULTIMEDIA COMMUNICATIONS

**Hermann Eul**,
*Member of the Management Board, Infineon Technologies, Munich, Germany*

- At the current growth rate, the number of worldwide subscribers of cellular services is expected to exceed 1.5 billion by 2007. In 2004, 700 million mobile handsets were produced.
- High data-rates such as 7.2 Mb/s HSDPA and corresponding mobility trade-offs, along with different standards like 2G, 3G, Bluetooth, WLAN, GPS, UWB and digital video broadcasting, are leading to multimode requirements. Correspondingly, topics such as coexistence of different technologies must be solved. Beyond all of that, secure data transfer using technologies such as encryption is most important for the networked world.
- Parameters such as data-rate and algorithmic circuit complexity have changed exponentially with time, but there was not been, much improvement in battery capacity. For this reason, a key consideration for mobile products is energy management and power reduction.

- Wafer processes with low leakage and improved analog and RF capabilities are required to achieve the performance targets for ICs.
- Platform concepts, including analog and RF, to provide the most-practical costs power-levels and form-factors, are key requirements for system-on-chip and system-in-package solutions for current and future mobile multimedia terminals.

## [1.3] THE FUTURE OF COMPUTING FOR REAL-TIME ENTERTAINMENT

**Ken Kutaragi**,
*President and CEO, SONY Computer Entertainment, Tokyo, Japan*

- There are two elements in real-timeliness that a human being can intuitively sense. One is the continuity of motion that a human being can cognitively feel to be natural, and the other is response time between action and reaction.
- Lack of both processing power and data-transfer rate using general-purpose microprocessors in achieving this level of real-timeliness has motivated the development of a new breed of more-powerful processors built on a new architecture.
- Today, more than 40 million computer entertainment systems are shipped in a year, and are becoming a leading power in spearheading advancements in semiconductor technology, and in creating demand.
- In the future of real-time computing, massively "Parallel Computing Over the Network" to execute vast amounts of computation, and "Vision Systems" that recognize the real world in real-time from a vast number of sensors over the Network, will lead the next era in real-time computing.

# *TECHNICAL HIGHLIGHTS*

## • ANALOG:

- RF preamplifier with lower noise figure, higher gain and smaller silicon area **[11.5]**
- High-efficiency Class-D Audio Power Amplifiers push to new levels of fidelity at 100W+ power levels **[19.1, 19.3]**
- Fully-integrated synchronous DC-to-DC converter with on-chip LC filter in 0.18µm SiGe technology **[19.7]**
- DC-to-2.4 GHz power upconverter employing a multipath mostly-digital technique to cancel unwanted harmonics up to the $17^{th}$, without filtering **[25.1]**
- New techniques for handling leakage currents in PLLs **[32.5]**
- Divider circuit in CMOS pushes operating frequency beyond 70GHz **[32.8]**

## • DATA CONVERTERS:

- High-bandwidth Delta-Sigma ADCs increase dynamic range **[3.1, 3.2]**
- Data converters for communication systems move closer to the antenna **[3.2, 3.3, 31.7, 31.8]**
- Nyquist ADCs achieve sub-pJ/conversion-step power efficiency **[12.1, 12.2, 12.3, 12.5, 12.7, 31.3, 31.5, 31.6]**
- Advances in power-reduction and improved converter efficiency **[12.1, 12.2., 12.3, 12.5, 12.7, 31.1, 31.5, 31.6]**
- Offset-reduction techniques enable low-power and high-speed Nyquist ADCs **[12.3, 12.5, 12.6, 31.1, 31.2, 31.3]**
- 1GS/s ADC with new sampling technique pushes resolution to 11-bits. **[31.6]**

## • DIGITAL:

- Single-chip processors with up to 16 cores and 32-threads **[5.1, 5.2]**
- 65nm processors and processor components **[5.3, 5.7, 24.1, 24.7]**
- 1.2Tb/s aggregate bandwidth from a single chip **[5.6]**
- 9GHz processor components: 64-bit integer execution unit and register file **[5.7,24.7]**
- Next-generation research on clocking: low skew/jitter resonant techniques **[21.1, 21.4, 21.5, 21.6]**

# *TECHNICAL HIGHLIGHTS (CONTINUED)*

- Advanced adder designs: 64-bit adders 4 to 6 fanout-of-4 (FO4) delay **[24.2, 24.3]**
- Circuit techniques for improved PVT tolerance **[24.7, 24.4, 24.5, 29.6]**
- Real-time high-spatial-resolution power monitoring of modern processor chips **[29.2]**
- Single chip with power management for 20 power domains **[29.4, 29.5]**

## • IMAGERS, MEMS, MEDICAL AND DISPLAY:

- A 32-site 4-channel cochlear-implant microelectrode array with inductively-coupled wireless link and position-sensing capability. **[2.3]**
- Low-power implantable retinal prostheses include a digitally-programmable stimulation scheme with ESD protection, achieving a data rate of 100kb/s at 1.3mW. **[2.4, 2.5]**
- A current-mode 6-bit AMOLED driver using the current-copier technique, achieving 2% accuracy at currents in the 10μA to 10nA range. **[9.2]**
- A micromechanical silicon-on-insulator accelerometer with low-noise CMOS, achieves micro-gravity resolution in a wide dynamic range of 95dB to enable inertial navigation at micro-scale **[16.1]**
- A thermal oscillator in standard CMOS used as a temperature sensor, achieving an accuracy better than ±0.5°C over the industrial temperature range of-40 to 105°C **[16.5]**
- A 1/1.8-inch 6.4M pixel CMOS image sensor for digital still cameras, achieving 60frames/s with photographic performance. **[27.1]**
- A 128x128 pixel CMOS image sensor inspired by the human retina images over a wide range of light levels while responding to relative intensity changes in less than 100μs. **[27.9]**

## • MEMORY:

- NROM-based flash memory achieves four bits of storage in a single memory cell **[7.1]**
- Smallest 8Gb multi-level NAND flash memory ever reported **[7.7]**
- 10MB/s program throughput achieved by a sub-60nm multi-level NAND flash memory. **[7.7]**
- Powerful 5-bit error-correction scheme embedded into a monolithic multi-level NAND flash memory. **[7.6]**
- An 8Gb/s deca-data-rate SDRAM incorporates CRC I/O error-detection **[8.1]**
- A range-matching TCAM with 2.5x data-storage efficiency **[8.6]**
- 5Ghz SRAM design for high-performance CPU **[34.1]**
- Thyristor-based volatile memory in nano-scale CMOS **[34.6]**

# *TECHNICAL HIGHLIGHTS (CONTINUED)*

## • SIGNAL PROCESSING:

- First-published DSSS UWB baseband transceiver for wireless ad-hoc networks. **[14.5]**
- 5mW MPEG4 video encoder and 160Kgate HDTV video decoder provide low-power and low-cost solutions. **[22.3, 22.6]**
- Vertex processor delivers 120Mvertices/s 3D-geometry performance which is 3x the performance and half the power of previous chips. **[22.4]**

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- First demonstration of functional RFID tags built in organics, operating at 13.56MHz **[15.2]**
- Electronic "nose" detects spoilage of wine at levels of 10 parts per million **[15.3]**
- Development of a Braille sheet allows e-books for the blind that update in 2 seconds **[15.4]**
- 71,000 TFT devices integrated on plastic realize cryptographic security RFID **[15.6]**
- 0.15mm x 0.15mm RFID chip with 128-bit ROM and antenna contacts on top and bottom. **[17.1]**
- 3.4Mb/s data rate in a 13.56MHz RFID front-end **[17.2]**
- 50-to-75 GHz 0.13μm CMOS LNA achieves > 20dB gain **[17.8]**
- Combination of 2.4 GHz BAW resonators and 0.18μm CMOS radio front-end achieving 50 dB image rejection with 1.8mW power consumption **[17.7]**
- Demonstrated generation of 1 microwatt of electrical power from a 1 milliCurie of benign Nickel-63 nuclear-energy source. **[23.1]**
- First experimental comparison of comprehensive building blocks in FinFET and Triple-Gate transistor technologies. **[23.2]**
- Demonstrated 1 Terabit-per-second data transfer between 3D integrated chips via inductive coupling over an area of 2 square millimeters and energy consumption of 3 picoJoules per bit. **[23.4]**
- Optical clocking at 5-to-10 GHz with a silicon nano-photodiode. **[23.5]**
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- Realization of a MEMS-based reusable biosensor for identifying and monitoring cardiovascular-risk biomarkers (that is, C-Reactive proteins) **[30.6]**

# *TECHNICAL HIGHLIGHTS (CONTINUED)*

## • WIRELESS COMMUNICATIONS:

- Fully-integrated UWB transceivers in CMOS **[6.4, 6.5]**
- A frequency synthesizer covering all the 14 UWB bands in CMOS **[6.7]**
- A 77GHz phased-array system in silicon **[10.1. 10.2]**
- A 60GHz transmitter and receiver in silicon **[10.3]**
- The first single-chip 802.11a/b/g SoC that fully integrates RF front-end, baseband analog, digital baseband, and MAC in one die for embedded applications. **[20.2]**
- A highly-integrated SoC for low-power ZigBee applications, which includes the radio and the PHY layers. **[20.6]**
- A fully-integrated SoC for GSM/GPRS on 0.13μm CMOS **[26.7]**
- A 1.9GHz single-chip CMOS PHS cellphone **[26.8]**
- RF tuners for all the worldwide mobile TV standards. **[33.1 to 33.6]**

## • WIRELINE COMMUNICATIONS:

- 10Gb/s 5-tap DFE / 4-Tap FFE transceivers in 90nm CMOS **[4.1]**
- 12.5Gb/s single-chip transceiver for UTP Cable in 0.13μm CMOS **[4.4]**
- 9.95-to-11.1Gb/s XFP Transceiver in 0.13μm CMOS **[13.1]**
- 10Gb/s photonic modulator and WDM Mux/Demux with electronics in 0.13μm SOI **[13.7]**
- 10Gb/s burst-mode adaptive gain-select limiting amplifier in 0.13μm CMOS **[13.9]**
- 25Gb/s CDR in 90nm CMOS for high-density interconnects **[18.1]**
- Data recovery and retiming for 4.8Gb/s fully-buffered DIMM serial links **[18.6]**
- 104Gb/s $2^{11}$-1 and 110Gb/s $2^{9}$-1 PRBS Generator in InP HBT technology **[28.10]**

# EVENING SESSIONS

There are ten Evening Sessions in all, three on each of Sunday and Tuesday evenings and four on Monday evening. Of these, there are seven Special-Topic Sessions, providing insight and background in a topical area.

## SUNDAY

**SE1** What is Driving Displays?

**SE2** Power-Aware Signal Processing

**SE3** Analog Scaling

## MONDAY

**E1** Is the Digital-Circuit Designer Dead?

**SE4** Emerging & Disruptive Memory Technologies

**SE5** CMOS RF Design at 90nm and Beyond

**SE6** Highlights of A-SSCC 2005 and the 2005 Symposium on VLSI Technology

## TUESDAY

**E2** Present (and Future) Classic Circuits with Less than 25 Transistors

**E3** What is Next to be Off-Shored, IC Design Jobs or IC Design Futures?

**SE7** Sensors on the Move

# *SHORT COURSE:*

*Thursday, February 9, 2006*

# *ANALOG-TO-DIGITAL CONVERTERS*

## COURSE OBJECTIVE:

This Short Course is intended to provide both entry-level and experienced engineers with practical approaches to the design of analog-to-digital converters. The course provides an overall perspective on the technology considerations, circuit-design issues, and detailed design strategies, for circuit building blocks in analog-to-digital converters. Topics covered address the challenges faced by analog designers in current and future technologies, with an emphasis on detailed circuit-design approaches, and methodologies for deep-submicron integration.

## OVERVIEW:

- Fundamental Limits and Practical Design Issues in A/D Converters

  **Hae-Seung Lee,** *Massachusetts Institute of Technology*

- Pipelined A/D Converters

  **Bang-Sup Song**, *University of California, San Diego*

- ΔΣ ADCs

  **Richard Schreier**, *Analog Devices*

- Sub-1V Analog-to-Digital Converters

  **Un-Ku Moon**, *Oregon State University*

# *TUTORIALS:*

*Sunday, February 5, 2006*

**T1** INTRODUCTION TO FRACTIONAL-N PHASE-LOCKED LOOPS
**Ian Galton**, *University of California, San Diego*

**T2** DATA-CONVERTER INTERFACES: THE ANALOG AND DIGITAL INS AND OUTS
**David Robertson**, *Analog Devices*

**T3** INTRODUCTION TO STATISTICAL VARIATION AND TECHNIQUES FOR DESIGN OPTIMIZATION
**Norman Rohrer**, *IBM*

**T4** INTRODUCTION TO CMOS BIO-SENSORS: ELECTRICAL SPECIFICATIONS, CMOS PROCESSING, CIRCUIT AND SYSTEM DESIGN
**Roland Thewes**, *Infineon*

**T5** MULTI-LEVEL CELL DESIGN FOR FLASH MEMORY
**Mark Bauer**, *Intel*

**T6** CELLULAR-PHONE APPLICATIONS TRENDS AND DSP TECHNOLOGY
**Masafumi Takahashi**, *Toshiba*

**T7** 3D INTEGRATION
**Kerry Bernstein**, *IBM*

**T8** MILLIMETER-WAVE ICS IN SILICON
**Ali Hajimiri**, *California Institute of Technology*

**T9** SIGNAL INTEGRITY FOR HIGH-SPEED CIRCUIT DESIGNERS
**Hong-June Park**, *Pohang University of Science and Technology (POSTECH)*

# ADVANCED-CIRCUIT-DESIGN FORUMS:

*Sunday, February 5, 2006*

## F1 ADVANCED WIRELESS CMOS TRANSCEIVERS

- Introduction
  **Rudolf Koch,** *Infineon*

- Cellular and Short-Range Standards, Key Challenges, and their Impact on Architecture
  **Chris Rudell,** *Intel*

- Highly-Integrated Linear Transmitters
  **Tony Montalvo,** *Analog Devices*

- Receivers for Traditional, MIMO, and Dynamic Bandwidth Radio Systems
  **Bill McFarland,** *Atheros*

- System Design for Multi-Standard Radios
  **Aarno Pärssinen,** *Nokia*

- Transceiver Integration into a Single-Chip Cellular Phone
  **Andre Hanke,** *Infineon*

- Digital RF Processor (DRP) for Cellular Phones
  **Bogdan Staszewski,** *Texas Instruments,*

- Software-Defined Radio
  **Asad Abidi,** *University of California, Los Angeles*

## F2 EMBEDDED-SRAM DESIGN

- Introduction
  **Don Weiss**, *Intel*

- High-Performance Power-Aware SRAM Design
  **Kevin Zhang**, *Intel*

- Low-Power Low-Voltage SRAM Design for Battery Operation
  **Masanao Yamaoka**, *Hitachi*

- Design for Testability (DFT)
  **R. Dean Adams**, *Magma Design Automation*

- Stability/Reliability/Manufacturability Factors in SRAM Design
  **Takayuki Kawahara**, *Hitachi*

- Alternatives to 6T SRAM
  **Hyun-Geun Byun**, *Samsung*

# ADVANCED-CIIRCUIT-DESIGN FORUMS:

*Sunday, February 5, 2006*

## F3 CIRCUIT DESIGN IN EMERGING TECHNOLOGIES

- Introduction
  **Eugenio Cantatore,** *Philips*

- Regular Fabrics for Nano-Scaled CMOS Technologies
  **Larry Pileggi,** *Carnegie Mellon University*

- Multigate MOSFET Design
  **Gerhard Knoblinger,** *Infineon*

- Design with Organic TFTs
  **Eugenio Cantatore,** *Philips*

- Technology Trends and Design with Silicon TFTs
  **Tatsuya Shimoda,** *Seiko-Epson*

- Digital Circuits Using Carbon Nanotubes: Modeling, Design, and Architectures
  **Ali Keshavarzi,** *Intel*

- Analog-Circuit Design with 1D Electronic Devices
  **Donhee Ham and Xiaofeng Li,** *Harvard University*

- Spintronics: Past, Present, and Future
  **Stuart Parkin***, IBM*

# ADVANCED-CIRCUIT-DESIGN FORUMS:

*Thursday, February 9, 2006*

## F4 COLOR IMAGING

- Introduction
  **Albert Theuwissen,** *DALSA*

- Human Vision System
  **Brian Wandell,** *Stanford University*

- Capturing Color Images
  **Tetsuya Kuno,** *Mitsubishi*

- Color-Filter Technology
  **Katsumi Yamamoto,** *Toppan SMIC*

- Color Matrixing
  **Gennady Agranov,** *Micron*

- Color Interpolation
  **Takashi Saito,** *Kanagawa University*

- White Balancing
  **Massimo Mancuso,** *ST Microelectronics*

- Color Coding
  **Charles Poynton,** *ATI*

# ADVANCED-CIRCUIT-DESIGN FORUMS:

*Thursday, February 9, 2006*

## F5 ATAC: HIGH-SPEED INTERCONNECT

- Introduction
  **Wolfgang Pribyl**, *austriamicrosystems & CONPRI*

- High-Speed Interconnect Techniques, Standards and Application Areas
  **Yuriy Greshishchev**, *PMC Sierra*

- Implementing Chip- and Board-Level Protocols on Programmable Platforms
  **Christian Sauer**, *Infineon*

- The Evolution of High-Speed Interfaces into Memory Applications
  **Antony Sanders**, *Infineon*

- Receiver Decision-Feedback Equalization for Multi-Gigabit Server Links
  **Evelina Yeung**, *Intel*

- Tradeoffs of Receive and Transmit Equalization Architectures in 10 to 20Gb/s I/O Systems
  **Bryan Casper**, *Intel*

- A Study of FFE/DFE Performance for Application to 10Gb/s 802.3ap Ethernet over Backplane Channels
  **Troy Beukema**, *IBM*

- Multi-Gigabit Signaling Over UTP Cables
  **Scott Powell,** *Broadcom*

- Silicon Photonics in High-Speed Interconnects – Overview, Results, and Future Perspectives
  **Mario Paniccia**, *Intel*

# ADVANCED-CIRCUIT-DESIGN FORUMS:

*Thursday, February 9, 2006*

## F6 MULTI-CORE ARCHITECTURES, DESIGNS, AND IMPLEMENTATION CHALLENGES

- Introduction
  **Peter Kogge**, *University of Notre Dame,*

- An Introduction to Multicore Chip Design
  **Peter Kogge**, *University of Notre Dame*

- Niagara: Architecture and Physical Design of a 32-Threaded General-Purpose CPU
  **James Laudon**, *Sun Microsystems*

- The Cell Processor's Multicore Architecture: Impact and Influence of Physical Design
  **James Kahle**, *IBM*

- Low-Power Multicore Chips for Mobile Embedded Applications
  **Satoshi Matsushita**, *NEC*

- Challenges of Multicore Processors for Embedded Infrastructure Requiring High-Bandwidth I/O, Memory Interfaces, and On-Chip Accelerators
  **Dan Bouvier**, *Freescale Semiconductor*

- Circuit Technologies for Multicore Processor Design
  **Stefan Rusu**, *Intel*

- Multicore-SoC Test and Yield Enhancement– Challenges and Advancements in a Complex Environment
  **Juan Rosal**, *Texas Instruments*

- How Does Future Technology Scaling Affect a Multicore World?
  **Panel Discussion**

# ANALOG & RF

- **Overview**
- **Featured Papers**
- **Panel**
- **Tutorial**

# ISSCC 2006 – ANALOG & RF

**Subcommittee Chair:** *John R. Long, Delft University of Technology, The Netherlands*

# *OVERVIEW*

## MOST-SIGNIFICANT RESULTS

- RF preamplifier with lower noise figure, higher gain and smaller silicon area **[11.5]**
- High-Efficiency Class-D Audio Power Amplifiers push to new levels of fidelity at 100W+ power levels **[19.1, 19.3]**
- Fully-integrated synchronous DC to DC converter with on-chip LC filter in 0.18μm SiGe technology **[19.7]**
- DC to 2.4 GHz power upconverter employing a multipath mostly-digital technique to cancel unwanted harmonics up to the 17$^{th}$, without filtering **[25.1]**
- New techniques for handling leakage currents in PLLs **[32.5]**
- Divider circuit in CMOS pushes operating frequency beyond 70GHz **[32.8]**

## APPLICATIONS AND ECONOMIC IMPACT

- Wireless handheld devices with improved RX and TX efficiency to extend battery life and enable larger feature set **[11.5]**
- High-efficiency audio power amplifiers drive down the cost and size of home theater and automotive-entertainment systems **[19.1, 19.3]**
- Fully-integrated converter enables complete SoC solution for low-cost production **[19.7]**
- Digital correction techniques are simple and cost-effective ways to improve quality of analog signals in highly-integrated receiver ICs **[25.1]**
- Leakage-control technique opens up the design of PLLs in deep-submicron CMOS **[32.5]**
- CMOS at 70GHz leads to lower costs for millimeter-wave applications **[32.8]**

## PANEL

***Present (and Future) Classic Circuits with Less Than 25 Transistors*** **[EP2]**

## TUTORIAL

**Introduction to Fractional-*N* Phase-Locked Loops [T1]**

# *Art of RF Design*

## A 5GHz Resistive-Feedback CMOS LNA for Low-Cost Multi-Standard Applications [11.5]

*Intel*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Need for wider tuning range, faster settling time, and lower power consumption, for mobile multi-standard radio

## NOVEL CONTRIBUTIONS

- Inductorless LNA at 5Ghz occupies small silicon area **[11.5]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Highly-efficient and small-area circuits enable feature-packed wireless handheld devices **[11.5]**

# *200W+ Monolithic Class-D Audio PA Stage*

## A 240W Monolithic Class-D Audio-Amplifier Output Stage [19.1]

*Texas Instruments; ϕrsted*DTU*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- High-power Class-D output stages typically suffer from high levels of distortion
- High levels of distortion necessitate complicated feedback structures

## NOVEL CONTRIBUTIONS

- An output switching stage with 0.1% THD at power levels up to 240W **[19.1]**
- Power amplifier operates “open-loop” in audio amplifiers, reducing complexity of the highest-fidelity applications **[19.1]**

## CURRENT AND PROJECTED SIGNIFICANCE

- This optimization approach minimizes distortion caused by output-switch “dead-time” **[19.1]**
- Lowers cost and size of amplifiers for home theater and automotive-entertainment systems **[19.1]**

# *Highest-Fidelity Class-D Audio Controller*

## A Digital Input Controller for Audio Class-D Amplifiers with 100W 0.004% THD+N and 113dB DR [19.3]

*Texas Instruments*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Available approaches have been analog with high distortion levels that require external DACs

## NOVEL CONTRIBUTIONS

- The controller accepts a digital-audio input and performs digital-to-analog conversion internal to the IC, while providing a novel analog-feedback architecture to correct distortion produced by the power stage. **[19.3]**
- The controller - in concert with a suitable power stage - achieves 0.004% distortion at the 100W output level. **[19.3]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Lower cost and size of amplifiers for home theater and automotive-entertainment systems **[19.3]**
- Development of a robust feedback architecture opens the door to high-fidelity audio at a very low cost **[19.3]**

# *Integration of LC filter in a DC-DC converter in SiGe technology*

## A Multi-Stage Interleaved Synchronous Buck Converter with Integrated Output Filter in a 0.18µm SiGe Process

**[19.7]**
*Freescale Semiconductor; Arizona State University*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Large filter-inductor and capacitor size makes full integration impossible
- External filter increases the number of I/O pads and PCB interconnects which introduces system noise, delay and power loss

## NOVEL CONTRIBUTIONS

- High switching frequency, multiphase interleaved operation, and fast hysteretic control reduce the filter inductor and capacitor sizes enabling a fully-integrated converter **[19.7]**
- Utilizes a 10µm-thick electroplated copper layer to improve integrated inductor and gate-capacitor performance **[19.7]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Reduces board-level circuit complexity and provides a low-cost product **[19.7]**
- Decreases the size and weight of handheld devices through miniaturization of the power modules **[19.7]**

# *RF/IF CIRCUITS*

## A Multipath Technique for Cancelling Harmonics and Sidebands in a Wideband Power Upconverter [25.1]

*University of Twente*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Complex analog techniques are not easily scalable to deep-submicron technologies

## NOVEL CONTRIBUTIONS

- The polyphase multipath technique allows digital wideband and frequency up-conversion without a filter **[25.1]**

## CURRENT AND PROJECTED SIGNIFICANCE

- A step forward to highly-reconfigurable and adaptive radio **[25.1]**

# *PLLs, VCOs, and Dividers*

## A 6.25GHz 1V LC-PLL in 0.13μm CMOS [32.5]

*Texas Instruments*

## 70GHz CMOS Harmonic-Injection-Locked Divider [32.8]

*University of Tokyo*

### PRESENT STATE OF THE ART *(THE PROBLEM)*

- Charge-pump leakage current in deep submicron processes increases jitter in PLLs
- Limited locking range in high-frequency dividers

### NOVEL CONTRIBUTIONS

- Improved state-of-the-art in the charge pumps for PLLs **[32.5]**
- Record operating frequency with twice the locking range compared to the current state-of-the-art **[32.8]**

### CURRENT AND PROJECTED SIGNIFICANCE

- Enables very-low-voltage low-timing-jitter PLL operation **[32.5]**
- Step forward for millimeter-wave transceivers in CMOS **[32.8]**

# *Panel*

## *Present (and Future) Classic Circuits with Less Than 25 Transistors*

*Organizer:* ***JoAnn Close****, Analog Devices*
*Moderator:* ***Bill Redman-White****, Philips Semiconductors and Southampton University*

## OBJECTIVE

- To illustrate, with specific examples from the last twenty years, key innovations in "small" circuit design.
- To highlight the attributes of a "classic" circuit.
- To identify the pressures that keep circuit innovation going.

## CHALLENGE

- What are the big drivers of innovation in the field of transistor-level design?
  - Demands of higher performance?
  - Meeting demands of new application areas?
  - Demands of shrinking CMOS technologies?

## CONTROVERSY

- Have there been recent significant advances in the field of transistor-level circuit design? Have all the really-good small circuits already been invented?
- What makes a circuit a classic? Is it elegance of design? Is it everyday usefulness? Is it portability among processes and application areas?
- Can we guess which circuits will be classics in the future? Will the requirements be different for future classics?

## PANEL DESCRIPTION:

Some circuits are easily forgotten like cheap wines, but others are instantly classic vintage. These are the sound choices of the past and present, and will be brought to the table for years to come. We ask some connoisseurs for their pick of circuits with fewer than 25 transistors from the last 20 years which best illustrate undiminished creativity in the field of transistor-level design.

Moderator:

**Bill Redman-White, Philips Semiconductors and Southampton University, United Kingdom**

Panelists:

**Klaas Bult, Broadcom, The Netherlands**
**Bob Dobkin, Linear Technology, CA**
**Barrie Gilbert, Analog Devices, OR**
**Tom Lee, Stanford University, CA, USA**
**Takahiro Miki, Renesas Technology, Japan**
**Yannis Tsividis, Columbia University, NY**

# *Tutorial*

# INTRODUCTION TO FRACTIONAL-*N* PHASE-LOCKED LOOPS

*Ian Galton, University of California at San Diego, CA*

## OVERVIEW

This tutorial begins with a brief review of integer-N PLLs, and then, presents a detailed explanation of the additional ideas and issues associated with the extension to fractional-N PLLs for frequency synthesis. Topics include a self-contained explanation of the relevant aspects of $\Delta\Sigma$ modulation, an extension of the well-known integer-N PLL linearized model to fractional-N PLLs, the non-ideal effects of particular concern in fractional-N PLLs such as charge-pump nonlinearities and data-dependent divider delays, and techniques for wideband in-loop digital modulation of the VCO. Case studies of example circuits and applications are presented to illustrate the main concepts.

## SPEAKER BIOGRAPHY

Ian Galton received his Sc.B. from Brown University, in 1984, and his M.S. and Ph.D. from the California Institute of Technology, in 1989 and 1992, respectively, all in electrical engineering. Since 1996, he has been a professor of electrical engineering at the University of California, San Diego, where he teaches and conducts research in the field of mixed-signal integrated circuits and systems for communications. Prior to 1996, he was with UC Irvine, the NASA Jet Propulsion Laboratory, Acuson, and Mead Data Central. His research involves the invention, analysis, and integrated-circuit implementation of critical communication-system building blocks, such as data converters, frequency synthesizers, and clock- recovery systems. In addition to his academic research, he regularly consults at several semiconductor companies, and teaches industry-oriented short courses on the design of mixed-signal integrated circuits. He has served as a member of a corporate Board of Directors, as a member of several corporate Technical Advisory Boards, and as the Editor-in-Chief of the IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing.

# DATA CONVERTERS

- **Overview**
- **Featured Papers**
- **Special-Topic Session**
- **Tutorial**
- **Short Course**

# ISSCC 2006 – Data Converters

**Subcommittee Chair:** *David Robinson, Analog Devices, Wilmington, MA*

# *OVERVIEW*

## MOST-SIGNIFICANT RESULTS

- High-bandwidth Sigma-Delta ADCs increase dynamic range **[3.1, 3.2]**
- Data Converters for communication systems move closer to the antenna **[3.2, 3.3, 31.7, 31.8]**
- Nyquist ADCs achieve sub-pJ/conversion step power efficiency **[12.1, 12.2, 12.3, 12.5, 12.7, 31.3, 31.5, 31.6]**
- Strong emphasis on power-reduction and improved converter efficiency **[12.1, 12.2., 12.3, 12.5, 12.7, 31.1, 31.5, 31.6]**
- Offset-reduction techniques enable low-power and high-speed Nyquist ADCs **[12.3, 12.5, 12.6, 31.1, 31.2, 31.3]**
- 1GS/s ADC with new sampling technique pushes resolution to 11-bits. **[31.6]**

## APPLICATIONS AND ECONOMIC IMPACT

- ADCs that can support higher input frequencies, and DACs that can synthesize higher output frequencies **[3.2, 3.3, 31.7, 31.8]**
- Wider bandwidths are required in data converters to support newer communications standards, including ADSL 2+, 3G, WLAN, and UWB. **[3.4, 3.5]**
- Lower power is critical for battery-powered portable applications, from cell phones to mobile TVs: Sometimes, power efficiency is improved by moving to more-advanced processes, but in many cases, it is realized through circuit innovation. **[12.1, 12.2., 12.3, 12.5, 12.7, 31.1, 31.5, 31.6]**

# SPECIAL-TOPIC SESSION

**Analog Scaling [SE3]**

# TUTORIAL

**Data-Converter Interfaces: The Analog and Digital Ins and Outs [T2]**

# Short Course

***This year's short course is on data-conversion techniques (refer to the Short-Course section of the Press Kit, page 20)***

# *Oversampling ADCs Push Dynamic Range at Higher Bandwidths*

## A 14b 20mW 640MHz CMOS CT ΔΣ ADC with 20MHz Signal Bandwidth and 12b ENOB [3.1]

*Xignal Technologies*

## A 375mW Quadrature Bandpass ΔΣ ADC with 90dB DR and 8.5MHz BW at 44MHz [3.2]

*Analog Devices*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Delta-Sigma converters are known to be very power-efficient. However, due to the required oversampling, they have typically been used on lower-frequency signals (audio, for example). Over the past few years, Delta-Sigma techniques are increasingly being applied to higher-frequency signals, offering a whole new set of challenges.

## NOVEL CONTRIBUTIONS

- One way to push the bandwidth up is to run at high clock rates, but this had traditionally implied very-high power consumption, but newer techniques (and fine-line CMOS processes) allow high sample rate converters to deliver good power efficiency. **[3.1, 3.4, 3.5]**

- Bandpass Delta-Sigma ADCs are pushing to the IF frequencies of consumer RF applications, including Radio and Television **[3.2, 3.3]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Delta-Sigma topologies can provide increased dynamic range, allowing large (and expensive) analog filters to be moved into the digital domain. **[3.1,3.2]**

- Improving power efficiencies allow for longer-battery-life and smaller-form-factor in portable systems. **[3.1]**

# Data Conversion at ISSCC 2006: It's all about Power Efficiency

## A 90nm CMOS 1.2V 10b Power and Speed-Programmable Pipelined ADC with 0.5pJ/Conversion-Step [12.1]

*Philips*

## A 10b 50MS/s Pipeline ADC with Opamp-Current Reuse [12.2]

*University of California, San Diego; Conexant*

## A 30mW 12b 40MS/s Subranging ADC with a High-Gain Offset-Canceling Positive-Feedback Amplifier in 90nm Digital CMOS [12.3]

*Sony*

## A 25 µW 100kS/s 12b ADC for Wireless Micro-Sensor Applications [12.5]

*Massachusetts Institute of Technology*

## A 0.16pJ/Conversion-Step 2.5mW 1.25GS/s 4b ADC in a 90nm Digital CMOS Process [31.1]

*IMEC*

## A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13µm CMOS [31.5]

*University of California, Berkeley*

## A 1GS/s 11b ADC Time-Interleaved ADC in 0.13µm CMOS [31.6]

*Teranetics*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Power Efficiency of High-Speed ADCs is limited to about 1pJ/Conversion-step
- Offset Reduction Techniques primarily used for increasing the resolution

## NOVEL CONTRIBUTIONS

- Offset Cancelation is used to reduce power consumption and increase speed **[12.3, 12.5, 31.1]**
- Offset Calibration by digital means is used to reduce power consumption **[12.6, 31.2]**
- Redundancy is used to select the lowest offset and reduce power consumption **[31.3]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Power saving enables higher levels of integration
- Power saving enables longer battery-life
- Power saving reduces size and weight

# SPECIAL-TOPIC SESSION

# *Analog Scaling*

*Organizer:* **Andrea Baschirotto,** *University of Lecce, Lecce, Italy*
*Chair:* **Robert Neff,** *Agilent Labs, Palo Alto, CA*

## OVERVIEW

The ITRS provides a robust roadmap for technology scaling of digital circuits, while analog circuits strongly suffer from the same trend. This divergence is becoming a crucial bottleneck in the realization of SoCs in scaled technologies, those merging high-density digital parts with high-performance analog interfaces. This results primarily from the reduction in supply voltage, which reduction limits analog performance both in qualitative and quantitative terms. In other words qualitatively, “Is it possible to operate from a low voltage?” and, quantitatively “If it is possible to operate, what performance is achievable?” In fact, the reduced supply voltage and the modified analog performance of scaled devices imply a lower signal swing, and, hence, a reduced dynamic range for analog circuits. This reduction becomes more and more critical in advanced signal-processing systems which require large dynamic range at low supply voltages. Accordingly, analog designers must face challenging trade-offs between supply headroom, device matching, gain, and accuracy.

## OBJECTIVE

This Special-Topic Session is organized as in three talks that deal with these critical issues, giving an overview of the present situation and a forecast of the future. Each talk will deal with one of the following open questions:

- How will the new scaled-technologies be affected by the power consumption of an analog system?
- Which analog topologies will be feasible in scaled technologies?
- What level of performance will be possible in scaled technologies?

# CHALLENGE

To review and propose possible circuit techniques for various blocks in an analog signal-processing unit (such as gain stages, filters, ADCs, etc) for maintaining performance quality in scaled technologies

# STRUCTURE

**Klaas Bult, Broadcom: "The Effect of Technology Scaling on Power Dissipation in Analog CMOS Circuits"**

A general approach to estimating power dissipation in analog CMOS circuits as a function of technology scaling is introduced. As technology progresses to smaller dimensions and lower supply voltages, matching-dominated circuits are expected to see a reduction in power dissipation, whereas noise-dominated circuits will see an increase. A prediction for future analog power scaling will be discussed, using the latest ITRS predictions on power-supply scaling.

**Andrea Baschirotto, University of Lecce: "Analog-Circuit Solutions in Scaled Technologies"**

Technology scaling leads to a reduction of the supply voltage available to analog devices, which can be compensated by a reduction in the MOS-device threshold voltage. However, the threshold-voltage reduction is proportionally less than the power-supply reduction. The effects of this slope difference on analog building blocks will be addressed for several situations.

**Willy Sansen, KU Leuven: "Delta-Sigma Converters in Scaled CMOS Technologies"**

In nanometer CMOS technologies, the supply voltage is reduced to below 1 volt. As a result, the dynamic range of analog blocks, and specifically of Delta-Sigma A/D Converters, is limited by lack of gain and by distortion. Moreover switches have become hard to realize. Specific circuit-design techniques are thus required to achieve high dynamic range, at low voltages for low power.

# RECAP

This session will provide insights into the effects of technology scaling on analog-circuit performance, and into solutions that could guarantee a certain analog-circuit performance quality, even in scaled technologies.

# *Tutorial*

# DATA CONVERTER INTERFACES: THE ANALOG AND DIGITAL INS AND OUTS

David Robertson, Analog Devices, Wilmington, MA

## OVERVIEW

- Data Converters form the critical gateway between "real world" analog signals and the digital signals used by computers
- New circuits, new architectures, and new applications, for converters create new challenges for interfacing to the converters on both the analog and digital sides.
- Higher digital speeds, faster analog signals, smaller supply voltages, and higher levels of integration, all have important implications for Data-Converter interfaces.
- Choices that the converter designer makes have fundamental implications for the "usability" of the data-converter design. Understanding these issues is important to interpreting how the state-of-the-art is advancing in converters.

## SPEAKER BIOGRAPHY

**David Robertson** is a Product-Line Director of the High-Speed-Converter Group at Analog Devices. He received his B.A. and B.E. degrees from Dartmouth College, in 1984 and 1985, respectively, and since 1985 has worked at Analog Devices on a wide variety of D/A and A/D converters on complementary bipolar, BiCMOS, and CMOS processes. Dave currently holds 14 patents on converter and mixed-signal circuits, has participated in two "outstanding-panel" ISSCC evening panel sessions, and was co-author of the paper that received the IEEE Journal of Solid-State Circuits 1997 Best Paper Award.

# DIGITAL

- **Overview**
- **Featured Papers**
- **Panel**
- **Tutorial**
- **Forum**
- **Trends**

# ISSCC 2006 – DIGITAL

**Subcommittee Chair:** *Samuel Naffziger, Intel, Fort Collins, CO*

# *OVERVIEW*

## MOST-SIGNIFICANT RESULTS

- Single-chip processors with up to 16 cores and 32-threads **[5.1, 5.2]**
- 65nm processors and processor components **[5.3, 5.7, 24.1, 24.7]**
- 1.2Tb/s aggregate bandwidth from a single chip **[5.6]**
- 9GHz processor components: 64-bit integer execution unit and register file **[5.7,24.7]**
    - Next-generation research on clocking: low skew/jitter resonant techniques **[21.1, 21.4, 21.5, 21.6]**
    - Advanced adder designs: 64-bit adders 4 to 6 front of 4 (FO4 delay) **[24.2, 24.3]**
    - Circuit techniques for improved PVT tolerance **[24.7, 24.4, 24.5, 29.6]**
    - Real-time high-spatial-resolution power monitoring of modern processor chips **[29.2]**
    - Single chip with power management for 20 power domains **[29.4, 29.5]**

## APPLICATIONS AND ECONOMIC IMPACT

- Multicore multithreaded processors enable higher parallelism, and improved power-performance **[5.1, 5.2, 5.3, 5.4, 5.5 ]**
- Debut of 65nm processor technology marks the next level of integration and performance, cutting chip area and power consumption **[5.3, 5.7, 24.1, 24.7]**
- High-speed I/O links take system bandwidths to a higher level; allowng tight coupling of large numbers of powerful processors **[5.6]**
    - Design for process, voltage and temperature (PVT) variation tolerance will improve manufacturability, reliability, cost **[24.7, 24.4, 24.5, 29.6]**
    - Advances in power-delivery techniques for higher-performance server processors improve power efficiency **[29.2, 29.3, 29.4, 29.7]**

## PANEL

**Is the Digital Circuit Designer Dead? [E1]**

## TUTORIAL

**Introduction to Fractional-*N* Phase-Locked Loops [T1]**

## FORUM

**Multicore Architectures: Designs, and Implementation Challenges [F6]**

# *High-Performance Chips Integrate Multicore, Multithread Processors*

## A Power-Efficient High-Throughput 32-Thread SPARC Processor [5.1]

*Sun Microsystems*

## A 16-Core RISC Microprocessor with Network Extensions [5.2]

*Cavium Networks*

## A Dual-Core Multithreaded Xeon™ Processor with 16MB L3 Cache [5.3]

*Intel*

## A 2.6GHz Dual-Core 64b x86 Microprocessor with DD2 Memory Support [5.4]

*AMD*

## A 64b CPU Pair: Dual- and Single-Processor Chips [5.5]

*IBM*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Processors continue to struggle for additional performance within a given power budget.
- The drive for higher frequency for better performance is fading due to power constraints

## NOVEL CONTRIBUTIONS

- 32 threads available within one chip. **[5.1]**
- 8 and 16 cores per chip enhance the overall power-performance design point **[5.1, 5.2]**
- Frequency is reduced to allow for additional cores per chip **[5.1, 5.2]**
- DDR2 usage becomes standard for high-throughput memory interfaces **[5.1, 5.2, 5.4]**
- Four-thread and two-thread cores effectively use silicon area for increased performance **[5.1, 5.3, 5.5]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Performance enhancements continue for existing architectures **[5.1, 5.3, 5.4, 5.5]**
- Dual-core chips becoming mainstream across many applications. **[5.3,5.4,5.5]**
- Software adaptation will be required to use multicore chips effectively.

# *65nm Processors and Processing Cores*

## A Dual-Core Multi-Threaded Xeon™ Processor with 16MB L3 Cache [5.3]

*Intel*

## A 9GHz 65nm Pentium®-4 Processor Integer-Execution Core [5.7]

*Intel .*

## 4GHz+ Low-Latency Fixed-Point and Binary Floating-Point Execution Units for the POWER6 Processor [24.1]

*IBM*

## An 8.8GHz 198mW 16x64b 1R/1W Variation-Tolerant Register File in 65nm CMOS [24.7]

*Intel*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Electronics consumers continue their demand for products that have more transistor density and integration, higher performance, and greater mobility.
- Due to challenges in processing, the industry has been very concerned over a substantial slowing of the rate of scaling, slower than 1 generation every 2 years.
- Power, in particular that due to leakage, is a critical concern.
- More-deeply-scaled CMOS technologies are exhibiting greater PVT variation.

## NOVEL CONTRIBUTIONS

- Power-management techniques that power up less than 1% of the SRAM cache, and utilize multiple sleep modes with virtual supplies that can be disconnected from all actual supplies. **[5.3]**
- First fully-demonstrated microprocessor and execution cores in 65nm CMOS technology **[5.3, 5.7, 24.1]**

- 9GHz operation of processor functional units, i.e. registers, and integer execution cores, in 65nm. with 30% improvement in speed performance, and 50% reduction in switching power is demonstrated. **[24.1, 24.7]**

- Variation and leakage current compensation embedded in the circuits and architecture of functional blocks using split wordlines and added keeper compensation circuits. **[24.7]**

## CURRENT AND PROJECTED SIGNIFICANCE

- The level of integration afforded by 65nm CMOS indicates an end to single-core processors. **[5.3]**

- The demonstration of a high-performance processor and execution cores indicates the ramp-up of 65nm production **[5.3, 5.7, 24.1, 24.7]**.

- The continued power-speed-performance improvements for individual execution units enable greater functionality for both server and mobile applications. **[5.7, 24.1, 24. 7]**

# *Green Computing: Charge-Recycling Logic Families Exceed 1 GHz Operation Frequencies*

## A 1.1GHz Charge-Recovery Logic [21.5]

*University of Michigan, Ann Arbor*

## A 3.5GHz Rotary-Traveling-Wave-Oscillator Clocked Dynamic-Logic Family in 0.25μm CMOS [21.6]

*Multigig*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Power consumption in high-performance processors is already a critical design issue
- Power delivery, cooling, and compute density are important constraints/parameters for datacenters
- Conventional circuit techniques draw current from a supply to charge load capacitance, then dump charge to ground to discharge loads (in which process, charge flows from supply to ground, and is "lost").
- Circuits to recycle charge (storing energy in an inductor, rather than dumping it to ground) have been proposed in the past, but to-date, operating frequencies have been limited, and required external inductive clock generators.

## NOVEL CONTRIBUTIONS

- Charge-recovery logic circuits fabricated and demonstrated to run at frequencies up to 1.3 GHz, with up to 60% of total energy recovered every cycle **[21.5]**
- 3.5 GHz operation for dynamic logic circuits powered by a charge-recycling oscillator clock **[21.6]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Due to process and frequency scaling, resonant clock generators can now be fully integrated on-chip (LC oscillator, rotary wave) **[21.5, 21.6]**
- Large fractions of the switching energy can be recovered, even at high frequencies. Similar techniques may eventually be used in mainstream-processor design, which would enable significant power reduction **[21.5, 21.6]**

# *On-Die Voltage Regulation for Fine-Grained Power Management and Delivery*

## A Linear Regulator with Fast Digital Control for Biasing Integrated DC-DC Converters [29.2]

*Intel; Silicon Laboratories*

## Hierarchical Power Distribution with Power Domains in 90nm Low-Power Multi-CPU Processor [29.4]

*Hitachi; Renesas*

## A Power-Management Scheme Controlling 20 Power Domains for a Single-Chip Mobile Processor [29.5]

*Renesas Technology; NTT DoCoMo*

## A Signal-Integrity Self-Test Concept for Debugging Nanometer CMOS ICs [29.6]

*Philips*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- The increasing levels of integration of transistors on-chip results in high power dissipation and increased challenges in power delivery.
- Variation due to manufacturing-process effects on transistor features, supply voltage, and temperature, cause degradation of power consumption and frequency of high-performance processing circuits.
- Conventional power-gating schemes only allow for coarse-grained power-domain partitioning.

## NOVEL CONTRIBUTIONS

- An on-die linear regulator achieves 3X speed-power performance by using digital control rather than conventional analog control **[29.2]**
- Fine-grained power gating in a 3G cellular processor is supported by a power tree distribution. Leakage current is reduced up to 4000X using a hierarchical power down scheme. **[29.4,29.5]**
- On-die voltage and temperature monitors are distributed across the chip to provide 10ps/20mV pulse power-supply noise resolution and 4b temperature resolution. **[29.6]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Improving the speed-power performance of the linear regulator improves the power effiiciency of the entire chip. **[29.2]**
- Leakage reduction enables lower overall energy consumption and improved product and battery lifetimes. **[29.4, 29.5]**
- High-resolution on-chip supply-noise and temperature monitors allow for adaptive self-control techniques to increase performance and reduce energy. **[29.6]**

# *Circuit Techniques for Power-Performance Optimization for Dynamic Logic*

## A Leakage-Current Replica Keeper for Dynamic Circuits [24.4]

*Fujitsu*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Dynamic logic is a mainstay in high-performance processing blocks
- Because of the dynamically-held charge in the logic, leakage is a serious issue in the design of dynamic logic. Feedback "keepers", are commonly used to maintain the charge by injecting a compensating current.
- While over-designing the "keeper" ensures robust performance, performance is degraded.

## NOVEL CONTRIBUTIONS

- A keeper device that has a well-controlled current is created by using a replica circuit that produces the optimal current. The technique provides the necessary robustness without excess degradation on performance.**[24.4]**
- The keeper design tracks process/voltage/temperature (PVT) variations. **[24.4]**
- The keeper design is applied to an SRAM. **[24.4]**

## CURRENT AND PROJECTED SIGNIFICANCE

- The technique can be applied to any regular logical structures in addition to memories. **[24.4]**
- The replica-keeper technique provides up to 40% improvements in an SRAM with almost no area penalty. **[24.4]**

# *Circuit and Architectural Improvements in Adder Design*

## A 250ps 64b Carry-Lookahead Adder in 90nm CMOS [24.2]

*University of California, Berkeley; Xilinx*

## A 64b Adder Using Self-Calibrating Differential Output-Prediction Logic [24.3]

*University of Washington; University of Texas, Dallas*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- High-performance processors must maintain <100W ceilings. Speed and energy efficiency of execution cores (i.e. adders, multipliers, etc.) are critical for modern processing ICs.
- A wide range of circuit options and architectural options are available for design. Tradeoffs in the design space is not well understood.

## NOVEL CONTRIBUTIONS

- An optimization framework is introduced to help designers converge to an architecture with optimal power/performance tradeoff. **[24.2]**
- 75pJ-per-addition in a 90nm CMOS technology at 4Goperations/sec and for 64 bits using the architectural optimization. **[24.2]**
- A prediction-based circuit technique using aggressive clock timing is introduced to improve both speed and performance. For improved robustness, a self-timing mechanism increases tolerance to process, voltage, and temperature (PVT) variations. **[24.3]**
- 30pJ-per-addition in a 130nm CMOS technology at 4Goperations/second for 64 bits using a novel circuit technique. **[24.3]**

# CURRENT AND PROJECTED SIGNIFICANCE

- Power-performance tradeoffs in the architecture of an adder are explored via an optimization. The framework which can be applied to future technologies as well as to execution units beyond adders **[24.2]**

- 30 to 75pJ/addition enables the next generation of low-power computing engines for both servers and mobile units. **[24.2, 24.3]**

# *High-Performance Processor Modules*

## A 9GHz 65nm Intel Pentium®-4 Processor Integer-Execution Core [5.7]

*Intel*

## An 8.8GHz 198mW 16x64b 1R/1W Variation-Tolerant Register File in 65nm CMOS [24.7]

*Intel*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- High-speed processor modules, such as the integer-execution core and register file, are key components of current high-performance processors.
- Power dissipation of the processor modules must go hand-in-hand with high-speed design.

## NOVEL CONTRIBUTIONS

- Domino circuits enable 2X frequency operation replacing previous Low-Voltage-Swing technology which did not scale frequency in the reduction to 65nm. **[5.7]**
- Optimized design of arithmetic units and register files leads to 50% reduction in dynamic power. **[5.7]**
- First demonstration of 65nm processor modules. **[5.7, 24.7]**
- Variation-tolerant register files achieve frequencies up to 10GHz, while reducing active leakage to 25mW over a wide range of process, voltage and temperature (PVT) conditions. **[24.7]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Significant power and performance improvements are being achieved on scaled process technologies through choice of logic families, architectural innovation, and power reduction techniques. **[5.7, 24.7]**

# *SPARC Processor expands to a 32-thread chip*

## A Power-Efficient High-Throughput 32-Thread SPARC Processor [5.1]

*Sun Microsystems*

## RESENT STATE OF THE ART *(THE PROBLEM)*

- General-purpose processors are limited in performance by power at high frequency.
- Dual-core chips share I/O infrastructure similar to that used in single-core predecessors.
- For performance, two threads per core are used on high-end chips.

## NOVEL CONTRIBUTIONS

- Eight 64-bit cores, each with four threads, enhance overall performance **[5.1]**
- Increased memory bandwidth is achieved with four dedicated DDR2 interfaces **[5.1]**
- 3MB L2 cache is shared by eight cores **[5.1]**

## CURRENT AND PROJECTED SIGNIFICANCE

- New performance level obtained for a single chip with 32 threads **[5.1]**
- Multicore, multithreaded chips running at a lower frequency obtain better performance **[5.1]**

# *Panel*

## *Is the Digital-Circuit Designer Dead?*

*Organizer:* ***Shannon Morton****, Icera*
*Moderator:* ***Dennis Fischette****, AMD*

## OBJECTIVE

- To determine the future of the digital-circuit designer
- To query whether technology trends will provide more, or less, challenges for digital design
- To question whether CAD tools are evolved enough to replace the digital designer

## CHALLENGE

- CAD tools have improved their design capabilities, and are arguably competent-enough to replace the digital designer for more and more applications and building blocks.
- Increasing leakage and variability issues demand more time and manpower for the design of high-performance and high-reliable circuits; Therefore simple structures with low innovation are proliferating.
- Technologists need to guide their roadmap to successfully manage leakage and variability without compromising key metrics such as performance, power, and reliability.

## CONTROVERSY

- Does life truly still exist in exotic and “exciting” logic styles, or will the digital designer be forced to revert to simpler circuit styles?
- Are those who design complex logic structures merely fooling themselves about the benefits, or, realistically can they still deliver their bang for the buck?
- Will new and emerging technologies provide scope for the evolution of the digital species, or will the species devolve into button-pushing ASIC monkeys?
- Is it beyond the scope of CAD tools to generate sufficiently-fast low-power circuits, or is the digital-circuit designer dead?

# *Tutorial*

# Introduction to Statistical Variation and Techniques for Design Optimization

*Norman Rohrer, IBM Systems & Technology Group, Essex Junction, VT*

## OVERVIEW

Variability is a reality in nanometer semiconductor processes. As lithography struggles to print shrinking devices on large wafers, one is less able to match devices within a chip, and from chip to chip. The variation is directly apparent within the threshold voltage of each FET and the cross-section of interconnects. The impact of this variation can result in poor yield and loss of functionality. This tutorial will cover:

- Sources of systematic and random variation, and methods of reducing their impact.
- Techniques for analysis of circuits using Monte-Carlo and vector-direction analysis.
- Functionality of static circuits, dynamic circuits, and SRAMs.
- Impact on frequency and power due to variation

## SPEAKER BIOGRAPHY

**Norman Rohrer** is a Distinguished Engineer in the PowerPC-Microprocessor Group within the System-and-Technology Group of IBM, located in Essex Junction, VT. Norman received his Bachelor's Degree in physics and mathematics from Manchester College, North Manchester, IN, in 1987. He received his Master's Degree and Doctor of Philosophy degree in electrical engineering from Ohio State University, Columbus, OH, in 1990 and 1992, respectively. Norman has been a lead designer on PowerPC 750 and 970 products for Apple's G3 and G5 chips, and Nintendo's GameCube. His interests lie in the area of high-speed circuit optimization for future technologies. Norman holds 18 patents, and is a co-author of two books titled "*High-Speed CMOS Circuit-Design Styles"*, and *"SOI Circuit-Design Concepts"*.

# *Advanced-Circuit-Design Forum*

## *Multicore Architectures, Design, and Implementation Challenges*

### Objective

This all-day forum is dedicated to the design and architecture of multicore processing chips to meet the needs of virtually all of tomorrow's advanced systems designs. Attendance is limited, and pre-registration is required. This all-day forum encourages open interchange in a closed environment.

### Audience

The targeted participants are circuit designers and chip architects who need to understand what the multicore design space encompasses, and how it affects both circuit and chip layout.

### Scope

Multicore chips, often called "Chip-Level Multi-Processors" (CMP), where more than one processor share the same die with significant parts of the memory hierarchy, are appearing with increasing frequency as standard design practice. This is happening across the board, from commodity designs such as microprocessors, routers, and graphics engines, to application-specific chips for games, cell phones, digital radios, and other SOCs. While the most attention may have been given to 2- to 4-core commodity microprocessors, many of the other multicore applications have long-since made the leap to 10s or even 100s of cores. This forum addresses this trend, and what it means in terms of both chip architectures and design practices. This includes what new circuit and subsystem blocks may be needed, and how all of this may affect the design and fab processes.

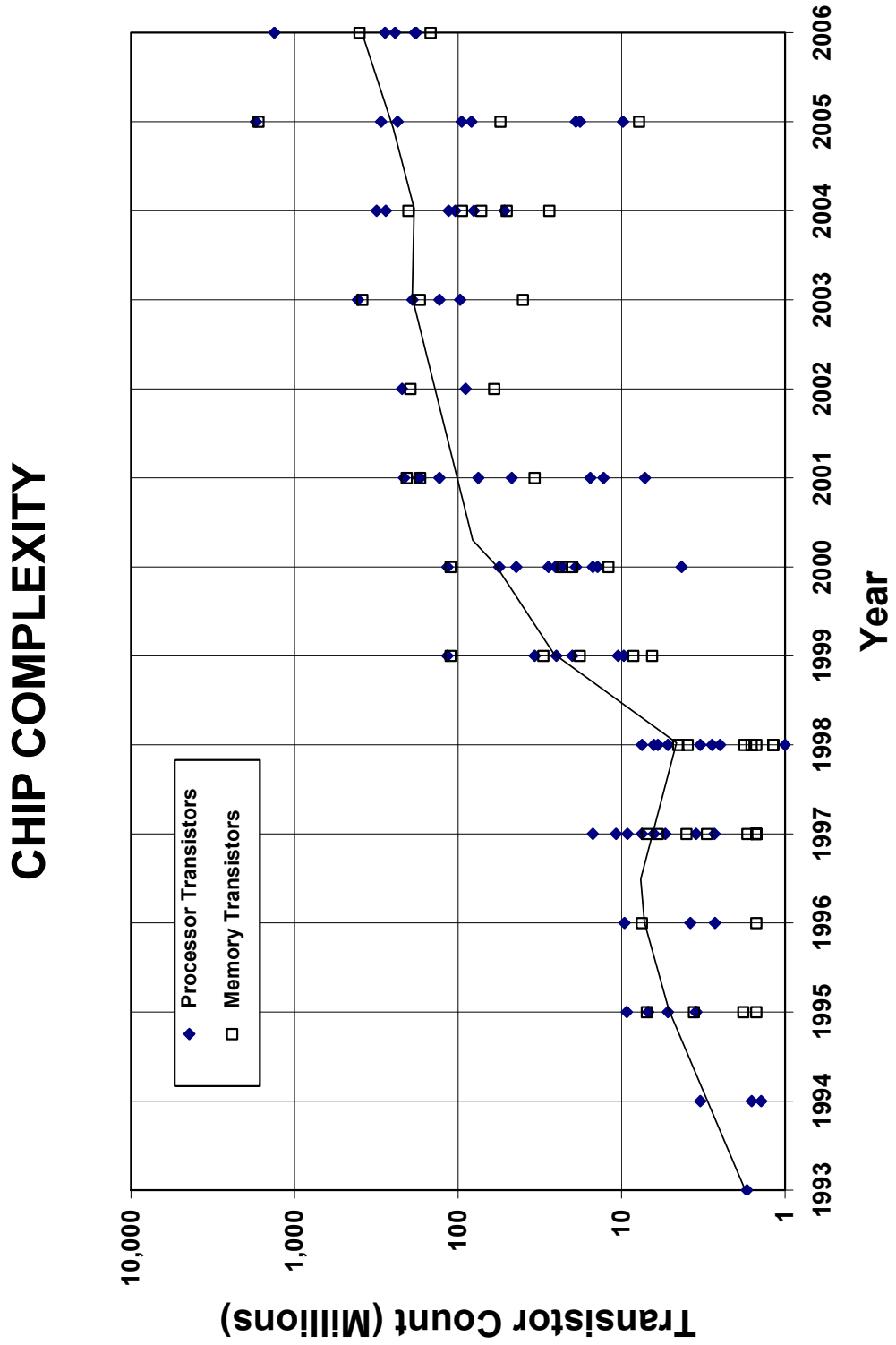
### Program

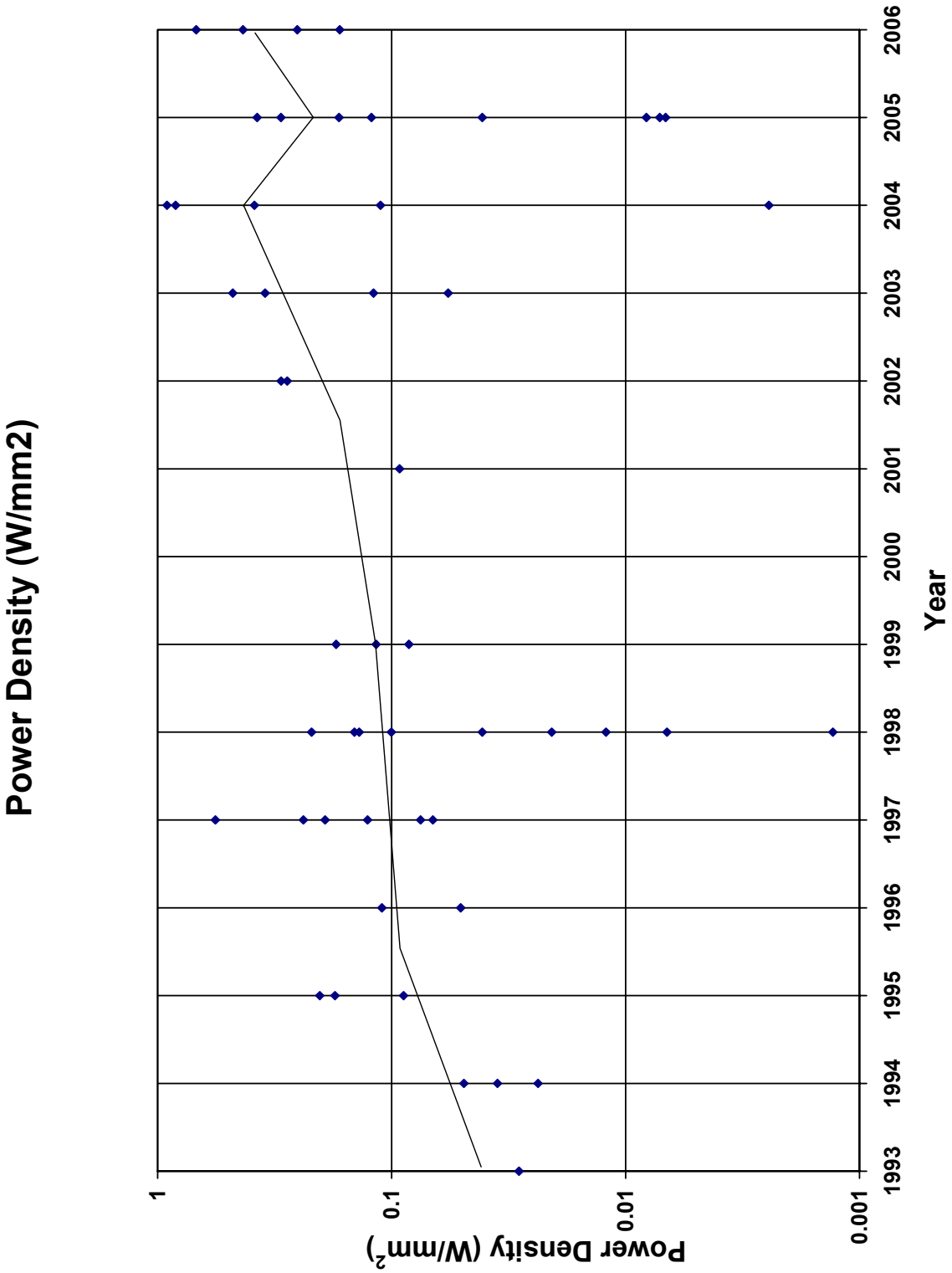
The forum will begin with an overview by **Peter Kogge**, of the University of Notre Dame, on a taxonomy of CMPs, what makes them attractive, and what are key metrics and design issues.

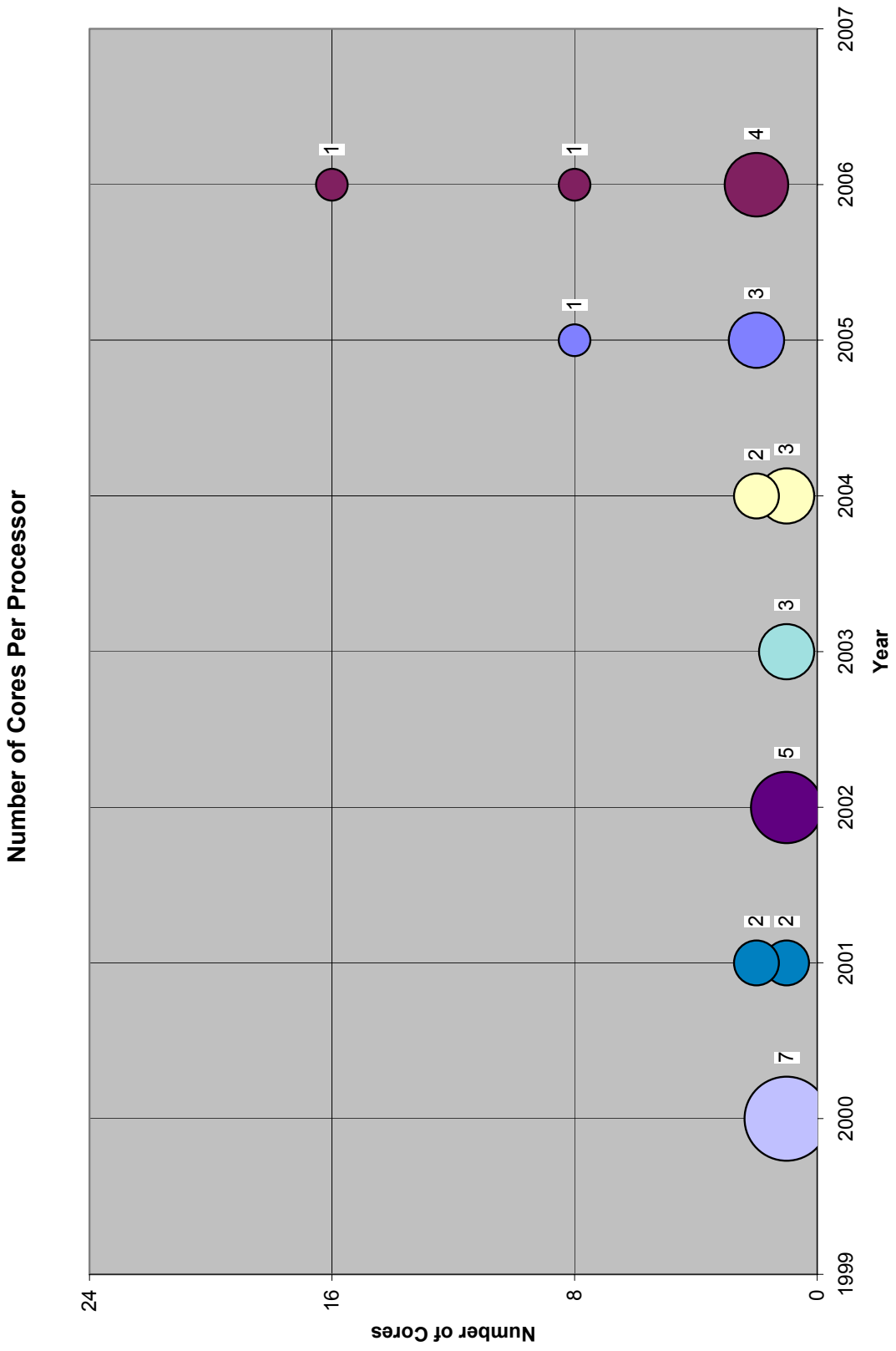
The next three presentations will describe specific points in this design space: **James Laudon**, from Sun Microsystems, will discuss critical issues in designing highly-multithreaded multicore chips such as Niagara, that are specifically designed for commercial server-level systems. **James Kahle**, from IBM, will address heterogeneous CMPs that have particular emphasis on multimedia performance, such as found in the Cell design. **Satoshi Matsushita**, from NEC, will address those unique issues associated with mobile embedded CMPs, where the given power budget is less than one watt.

The second set of talks address topics related to multi-core designs in general, and their effects on overall CAD and design flows. **Dan Bouvier**, of Freescale, will use a high-performance dual-core to highlight the challenges of interconnecting and integrating a wide range of on- and off-chip custom and soft IP. **Stefan Rusu**, from Intel, will cover circuit-technology aspects of multicore microprocessor design, with specific examples from Intel CMPs. Finally, **Juan Rosal**, from TI, will touch on the many challenges, and describe current methodologies, related to yield enhancement and test of multicore SoC products.

A panel at the end of the forum will address the question of how does future technology scaling change in a multicore world?"







# IMAGERS, MEMS, MEDICAL & DISPLAY

- **Overview**
- **Featured Papers**
- **Special-Topic Session**
- **Tutorial**
- **Forums**
- **Trends**

# ISSCC 2006 – IMAGERS, MEMS, MEDICAL & DISPLAY

**Subcommittee Chair:** *R. Daniel McGrath, Eastman Kodak, Rochester, NY*

# *OVERVIEW*

## MOST-SIGNIFICANT RESULTS

- A 32-site 4-channel cochlear-implant microelectrode array with inductively-coupled wireless link and position-sensing capability. **[2.3]**
- Low-power implantable retinal prostheses include a digitally-programmable stimulation scheme with ESD protection, achieving a data rate of 100kb/s at 1.3mW. **[2.4, 2.5]**
- A current-mode 6-bit AMOLED driver using the current-copier technique, achieving 2% accuracy at currents in the 10nA range. **[9.2]**
- A micromechanical silicon-on-insulator accelerometer with low-noise CMOS, achieves micro-gravity resolution in a wide dynamic range of 95dB to enable inertial navigation at micro-scale **[16.1]**
- A thermal oscillator in standard CMOS used as a temperature sensor, achieving an accuracy better than ±0.5°C over the industrial temperature range of-40 to 105°C **[16.5]**
- A 1/1.8 inch 6.4M pixel CMOS image sensor for digital still cameras, achieving 60frames/s with photographic performance. **[27.1]**
- A 128x128 pixel CMOS image sensor inspired by the human retina images over a wide range of light levels while responding to relative intensity changes in less than 100µs. **[27.9]**

## APPLICATIONS AND ECONOMIC IMPACT

- Improved speech perception for profoundly-deaf and severely-hearing-impaired patients while minimizing insertion trauma. **[2.3]**
- Emerging retinal prostheses point the way toward possible restoration of vision to the blind **[2.4, 2.5]**
- Technique eliminates the aging and temperature problems of OLEDs. **[9.2]**
- Cost of accelerometers low enough to be included in cell phones **[16.1]**
- Technique enables accurate on-chip temperature sensing for microprocessors in nanometer technology **[16.5]**
- Low-cost large-format CMOS image sensors enable high-quality low-cost digital cameras. **[27.1]**

## SPECIAL-TOPIC SESSIONS

**What is Driving Displays? [SE2]**
**Sensors on the Move [SE6]**

## TUTORIAL

**Introduction to CMOS Bio-Sensors: Electrical Specifications, CMOS Processing, Circuit and System Design [T4]**

## FORUM

**Color Imaging [F4]**

# *Cochlear-Implant Array with Minimum Insertion Damage*

## A 32-Site 4-Channel Cochlear Electrode Array [2.3]

*University of Michigan, Ann Arbor*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Current cochlear implants stimulate auditory nerves using only 16 to 22 electrodes.
- For better speech perception, more electrode-array sites are required.
- Insertion damage during the implant must be minimized.

## NOVEL CONTRIBUTIONS

- The 32-site 4-channel electrode array permits a better interface to various patterns of nerve survival and allows multi-polar current shaping for improved pitch perception. **[2.3]**
- Embedded position sensors minimize insertion damage during implant. **[2.3]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Use of circuitry on the cochlear array allows access to many stimulating sites for improved pitch perception using only a simple digital interface **[2.3]**
- This array sets the stage for high-density arrays for human use. **[2.3]**
- This is the first time an active cochlear array has been reported. **[2.3]**

# *Emerging Retinal Prostheses*

## A 0.1mm$^2$ Digitally-Programmable Nerve Stimulation-Pad Cell with High-Voltage Capability for a Retinal Implant [2.4]

*sciworx; IIP Thechnologies*

## Minimally-Invasive Retinal Prosthesis [2.5]

*MIT; MEEI; VA; University of California, Irvine; Cornell University*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- The number of implantable stimulating sites is limited, and only a small number of sites can be activated at a time.
- ESD protection of open contacts in the stimulating array is not provided.
- Full deployment of wireless retinal prostheses has not been achieved.

## NOVEL CONTRIBUTIONS

- An autonomous digitally-programmable nerve-stimulation cell is realized on a 0.1mm$^2$ die using 0.35μm high-voltage CMOS. **[2.4]**
- Stimulating electrodes include ESD protection and employ a charge-balancing scheme to prevent electrolysis. **[2.4]**
- A wireless retinal implant delivers a data rate of 100 kb/s at 1.3mW using ASK modulation. **[2.5]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Implantable chip can concurrently stimulate 116 electrodes out of total of 232 electrodes. **[2.4]**
- Important steps forward in the realization of implantable microsystems for helping the blind population. **[2.4, 2.5]**
- The 16-bit commands provide appropriate electrode signals-stimulation up to 930μA in steps of 30μA. **[2.5]**

# *Driving Displays*

## A Current-Drive IC using a S/H for QVGA Full-Color Active-Matrix Organic LED Mobile Displays [9.2]

*Samsung*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Voltage drive diode is not ideal for the diode I/V relationship.
- Previous current-drive solutions have not achieved required accuracy.

## NOVEL CONTRIBUTIONS

- Common current DAC drive an array of current copiers. **[9.2]**
- Improved accuracy of OLED drive. **[9.2]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Moves AMOLEDs from the laboratory to the manufacturing floor. **[9.2]**

# *Micro-g CMOS-SOI Accelerometer*

## A 4.5mW Closed-Loop ΔΣ Micro-Gravity CMOS-SOI Accelerometer [16.1]

*Georgia Institute of Technology*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Low-cost precision accelerometers with small form-factor and low-power level are needed in many applications including inertial navigation.
- Difficulty of achieving micro-g resolution and stability over a large dynamic range while maintaining a small form-factor

## NOVEL CONTRIBUTIONS

- An advanced micromachining process uses on a thick SOI substrate with post-deposition of polysilicon to reduce the capacitive gaps and achieve high-sensitivity and low-noise **[16.1]**
- New signal processing and force-balanced accelerometer architecture **[16.1]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Low-Cost Micro-g Accelerometers **[16.1]**
- Micro-g resolution and stability over a large dynamic range and wide bandwidth **[16.1]**

# *Integrated Thermal Oscillator*

## A CMOS Temperature-to-Frequency Converter with ±0.5°C (3σ) Inaccuracy from -40 to 105°C [16.5]

*Delft University of Technology*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Cost-effective and accurate temperature sensing is needed in many applications.
- Conventional techniques use bipolar transistors which perform poorly in advanced CMOS processes.
- Individual sensor calibration is expensive and calibration-free techniques are highly desired.

## NOVEL CONTRIBUTIONS

- First practical use of thermal oscillators in CMOS as temperature sensors **[16.5]**
- New signal processing architecture for temperature sensing **[16.5]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Calibration-free cost-effective accurate temperature sensors **[16.5]**
- Stable on-chip oscillators and time references **[16.5]**
- Temperature sensoring in advanced CMOS systems **[16.5]**

# *CMOS Image Sensor for Digital Still Cameras*

## A 1/1.8 inch 6.4MPixel, 60frames/s CMOS Image Sensor with Seamless Mode Change [27.1]

*SONY*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Low-cost CMOS image sensors for digital still-camera applications have lower performance than their CCD counterparts.

## NOVEL CONTRIBUTIONS

- New zigzag-shaped 1.75T pixel architecture enables a 2.5μm x 2.5μm pixel in 0.18μm CMOS **[27.1]**
- Full-frame and 2x2 binning modes are seamlessly-interchangeable without an extra invalid frame **[27.1]**
- High-speed digital interface enables 60frame/s operation **[27.1]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Lower-cost digital still cameras with photographic performance **[27.1]**

# *CMOS Image Sensor for Machine Vision Applications*

## A 128x128 120dB 30mW Asynchronous Vision Sensor that Responds to Relative-Intensity Change [27.9]

*ETH*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Wide-dynamic-range sensors are required for many machine-vision applications.
- Edge identification is also required for many machine-vision applications.
- Current machine-vision sensors do not adequately address these issues.

## NOVEL CONTRIBUTIONS

- 120dB dynamic range for a vision sensor **[27.9]**
- Pixels respond in less than 10μs in 1klux scene illumination with less than 10% contrast-threshold **[27.9]**
- Pixels independently and continuously quantizes changes in log intensity **[27.9]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Better understanding of the human visual system **[27.9]**
- Machine vision that mimics the human visual system **[27.9]**

# *SPECIAL-TOPIC SESSION*

## *What is Driving Displays?*

*Organizer:* ***Jed Hurwitz****, Gigle Semiconductors, Edinburgh, UK*
*Chair:* ***Marshall Bell****, National Semiconductors, Phoenix, AZ*

## OVERVIEW

- The display business is a multi-billion dollar market, with a wide range of solutions and technologies from the low-power display on your cellphone to an HDTV home cinema the size of your living room to even a virtual headset display. There are many different core technologies used for the generation and modulation of light, with different merits and challenges. This session will introduce some of those technologies and more importantly for the ISSCC community the role of the associated microelectronics that is an integral part of those applications.

## OBJECTIVE

- To introduce to the semiconductor community, some important display applications, the associated display technologies that address these markets and most importantly the role of silicon within these systems to provide the required electronic drive.

## CHALLENGE

- A display creates a modulated light output that represents the digital or analog version of the electronic input signal, whether analog or digital. The role of electronics in displays is fundamentally associated with getting the required drive signal to the pixel, in the right format for the display technology, and at the right point in time, for the right amount of time for the display technology and the application.

- Each display technology and application has its' own requirement on the signal type, modulation scheme, scanning speed, accuracy and system partition. Silicon plays an important role in these solutions because of its' design flexibility, manufacturability and wide range of capabilities, but the silicon needs to be adapted to the drive scheme and device requirements of the overall display.

- There are potentially many opportunities for 'new' silicon and system solutions for displays, by drawing upon the experience of the electronics community as a whole, but these will only ever be applicable if the silicon designer understands the display technology and application.

## STRUCTURE

- Myunghee Lee, Samsung, Korea. 'TFT-Driver IC Design: What are the Challenges?'

  TFT LCD's are the incumbent dominant display technology. This talk will present two different TFT display applications; driver IC's for mobile applications and driver IC's for HDTV, these devices are both driving similar display technologies, but have been optimized for their different applications

- Arokia Nathan, University of Waterloo, Canada. 'AMOLED Displays and Driving Schemes'

  OLED displays have the potential to become another dominant display technology; they fundamentally differ from TFT displays in that each pixel itself generates the required light. However, they have particular issues that the drive technology needs to overcome to maximize lifetime and resolution. This talk will go through the issues and some of the solutions.

- Mary Lou Jepson, MIT, USA. 'Analog Silicon For Digital Television and Other Oxymorons'

  In contrast with the previous two talks, where the silicon connects to the display through row and column drivers, this talk will discuss the use of silicon itself as a 2-D display in the form of Liquid Crystal On Silicon (LCOS) as a spatial light modulator in rear-projection televisions. This is one of the technologies that has the potential to radically reduce the cost of large format home cinema displays.

- Ian Underwood, MicroEmissive Displays, Scotland. 'CMOS Active-Matrix Backplane Design for Microdisplays'

  Continuing the theme of using silicon in combination with a top layer to create a 2-D micro-display, this talk will focus on the near-to-eye virtual display application. Here the display can reach new level of optimization for size, weight, power and resolution compared with all the previous displays which are direct view and need to be physically large and overcome ambient lighting. The two technologies of LCD and OLED and their required drive will be described.

## RECAP

- This session should serve to introduce an attendee not just to the core display technology and the current state-of-the-art in the display arena, but it should stimulate new thoughts on the opportunities for silicon providers to serve this market.

# *SPECIAL-TOPIC SESSION*

# *Sensors on the Move*

*Organizer:* ***Kofi Makinwa****, Delft University of Technology, Delft, The Netherlands*
*Chair:* ***Herman Casier****, AMI Semiconductors, Oudenaarde, Belgium*

## OVERVIEW

- Modern vehicles rely on sensors to improve engine performance, ensure compliance with environmental standards, and enhance passenger safety and comfort. However, the development of new automotive sensors is extremely challenging. Not only because such sensors must operate reliably in the harsh automotive environment, but because they must also be suitable for mass production at low cost.

## OBJECTIVE

- To highlight new developments in the field of automotive sensors

## CHALLENGE

- To develop sensors that are low-cost, suitable for high volume production, AND are reliable enough to meet the high standards of the automotive market
- To develop completely new types of sensors, specifically for automotive applications: for example, sensors that can detect obstacles, determine oil quality, and monitor tire pressure.

## STRUCTURE

- Jakob Jongsma, Infineon, Graz, Austria. 'Tire Pressure Monitoring Systems'

  This talk discusses the development of a tire pressure monitoring system (TPMS), which consists of MEMS sensors for measuring pressure and acceleration, interface circuitry, and a radio frequency communication link.

- Masaki Hirota, Nissan Motor, Kanagawa, Japan. 'Thermoelectric Infrared Image Sensors'

  This talk presents an un-cooled infrared sensor consisting of a 120x90 element array, and its application to human body detection and climate control systems.

- Bernhard Jakoby, Johannes Kepler University, Linz, Austria. 'Oil Condition Sensors'

  This talk will discuss the development of a miniaturized micro-acoustic viscosity sensor and the associated readout electronics.

- John Geen, Analog Devices, Cambridge, Massachusetts. 'Inertial Sensors for Automotive Applications'

  This talk outlines the development of gyroscopes and accelerometers that are suitable for low-cost mass production.

## RECAP

This session will provide an overview of emerging sensor technologies, which are expected to find wide application in the cars of tomorrow.

# *TUTORIAL*

## Introduction to CMOS Bio Sensors: Electrical Specifications, CMOS Processing, Circuit and System Design

Silicon-based bio sensor and actuator arrays have attracted much attention for a number of years - in particular if equipped with on-chip intelligence, i.e. CMOS circuitry. On the other hand, although there are a number of promising developments in this area, most of them focus on niche applications so far, commercialization of a number of approaches is still going on. It is thus sometimes difficult to distinguish whether a CMOS chip in this area is a "Me-too" demonstrator, competitive to other non-electronic technologies, or indeed provides a unique selling point worth to be further developed.

This talk will present an overview about the current status of CMOS approaches for in-vitro applications in life sciences and biotechnology such as drug screening and medical diagnosis. Starting with a review of the operating principles and applications of the related sensors and actuators, required CMOS processing extensions are considered, electrical specifications and related circuit requirements are derived, concrete circuit designs for the considered purposes are presented, and advantages and drawbacks compared to existing non-CMOS based techniques - if available - are discussed. Chips and data presented in the literature are considered to provide examples for the above mentioned issues.

**Roland Thewes** received his Dipl.-Ing. and Dr.-Ing. in Electrical Engineering from the University of Dortmund, Germany, in 1990 and 1995, respectively. Since 1994, he has been with the Research Laboratories of Siemens and Infineon, where he was active in the design of non-volatile memories and in the field of reliability and yield of analog CMOS circuits. From 1997 to 1999, he managed projects in the fields of design-for-manufacturability, reliability, analog-device performance, and analog-circuit design. Since 2000, he has been responsible for the Laboratory on Mixed-Signal Circuits in Corporate Research of Infineon Technologies, and for the development of CMOS-based biosensors. He lectures at the University of Ulm, and serves as a member of the technical program committees of ESSDERC, IEDM, and ISSCC.

# *FORUM*

## Color Imaging

### Objective

Color Imaging is a very interesting topic, because the signals that are delivered by the image sensor or the imaging system are not colored at all. Color imaging very much relies on all kinds of signal processing tricks and optimizations. On the other hand silicon chips react in a complete different way to color signals than the human visual system. That makes color imaging quite complex and difficult ! To contribute to a better understanding of the color issues and to stimulate creativity in this field, the ISSCC Subcommittee on IMMD is organizing a forum around this theme.

### Audience

Target participants are engineers and managers involved in the development of image sensors and camera systems making use of these devices. Such individuals need to understand the functionalities required in color imaging, and how their requirements can be met in future designs.

### Scope

The speakers at the forum are world experts. They are invited to present up-to-date material on various topics in color imaging. The talks are intended to address the material in all its technical details.

### Program

In the first presentation by **Brian Wandell** (Stanford University), the human visual system will be discussed. Certain aspects of color are quantitatively summarized in standard color spaces, and the experimental and biological basis for these color spaces will be explained. The second presentation by **Tetsuya Kuno** (Mitsubishi) will provide an overview of the color imaging systems and will discuss which is the best sensor to produce beautiful images.

The third presentation by **Katsumi Yamamoto** (Toppan SMIC) will concentrate on the color filter technology. Important characteristics in filter technology are high integration, overlay, making of the thin film, high sensitivity and external issues (transport, storage, ...). The fourth presentation by **Gennady Agranov** (Micron) and the fifith by **Takashi Saito** (Kanagawa University) concentrate on the digital processing of the color signals : color matrixing and demosaicing. The quality of the image obtained with a color camera is depending heavily on the quality of the algorithms during the matrixing operation and the demosaicing operation. Both papers will give an overview of state-of-the-art work in these fields.

It is a property of the human visual system to reduce the effect of the illumination when looking at a scene. This property, known as Color Constancy, is such that a white object is perceived as white independently of the color of the light source. Automatic White Balance (AWB) algorithms aim at providing the image capture device as well with the Color Constancy functionality, and this is the subject of the sixth presentation by **Massimo Mancuso** (ST Microelectronics).

The last presentation by **Charles Poynton** (ATI) will concentrate on color coding. Digital camera systems obviously deliver digital image data, however, there is a wide variety of digital image standards to which that data can be encoded. In this talk, the technical parameters of digital image exchange standards will be reviewed. At the end of the afternoon, all speakers will assemble in a panel format for an open discussion with the audience on the challenges in all aspects of color imaging.

# The Technology Trend of Display Drivers

Flat panel displays such as liquid crystal displays (LCD), plasma display panel (PDP), and organic light-emitting diode (OLED) are the fastest growing market segment of the electronic industry. And the applications of flat panel displays are very wide ranging from mobile phones to large-size (>40in) televisions. Consumers are demanding higher resolution, higher color depth, lower power consumption, lower cost, and higher picture quality. Satisfying this demand requires innovative ideas in the driving electronics such as higher gray scale, higher output counts per chip, smaller die size, low power, and higher accuracy in DACs and output circuits. It also requires a system perspective related to increased integration and novel
fabrication.

The current high-end display product for mobile phone applications employs a driver which is capable of 6-bit gray scale, quarter VGA format, 1/2 LSB accuracy of output channel-to-channel uniformity, and ~15mW power consumption in driving circuits. The rising demand for DMB phone applications will require drivers capable of VGA resolution and 8-bit gray scale. Current high-end monitors require UXGA resolution format and 8-bit gray scale drivers at lower cost. TV applications require higher than 8-bit gray scale (10-bit or 12-bit) drivers. To address system costs of large displays requires movement in the direction of panel-sized circuits made with thin film transistor (TFT) technology.

# Trends in Biomedical systems

- *Smaller is better in the biomedical world.* Following the trend of the IT industry, compact biomedical systems are providing new approaches to diagnosis and therapy. The papers presented this year stress this fact. Electronic DNA detection biochips, avoiding optical set-ups, promise to reduce the size of required equipment and cost of DNA analysis. This opens the way to point-of-care, affordable DNA diagnosis. The social, ethic and economic impact of these new technologies is large, in particular when considering the scenario of individual medication as a standard medical practice arising at the horizon.

- *A bionic world for all of us.* New developments in the area of prosthetic devices promise to defeat some of the most dreaded consequences of an aging society. The papers presented this year show significant advances in the replacement of cochlear and retinal functions with implantable biomedical subsystems. The impact of these technologies is profound since ophthalmic and vision diseases change the lives of millions of citizens in the developed world.

- *Highly integrated data acquisition interfaces for health monitoring.* Continuous monitoring of our health allows us to react quickly to medical emergencies that produce significant damage to the patients if the reaction is not immediate. The need for pervasive monitoring is met by new low-power interfaces presented at the conference that allow to monitor, for instance, the health of heart of the wearer. Coupled to wireless technologies, these devices will help to reduce and prevent the most dreaded aftermaths of strokes and other high-impact traumas.

# Technology Trends in Image Sensors

Image sensors is still one of the largest growth areas in the semiconductor industry today, driven by a huge camera phone market (450 million camera phones estimated in 2006 and 30% growth next year) as well as a rapid move away from film photography to digital cameras (80 million DSC units estimated in 2007).

CMOS imagers have surpassed CCDs in volume because of lower cost, lower power and simpler system integration. In terms of image performance, CMOS sensors have managed to catch up with CCDs and are now starting to take market shares from CCDs in the DSC area as well. This is primarily driven by the challenges associated with reading out large multi-megapixel arrays at relatively high frame rates (60fps and above).

Another high-growth market that is currently driving the imager technology development is the automotive industry where cameras are being used to improve safety (better visibility, airbag sensors, lane tracking, etc). Automotive sensors typically need advanced features such as high dynamic range and distance measurement. Such sensors also operate over a much wider temperature range than consumer sensors. It is expected that these features will eventually be used in other applications.

There are indications that the 'Mega-Pixel War' is starting to calm down, i.e. the rate of increase in pixel resolution (beyond ~8MPixels) is decreasing. One reason for this is system limitations such as bandwidth, optics, processing, etc. Another, is the challenges and costs associated with continuing to reduce pixel size to keep die area and cost down. For these reasons, focus is moving towards other performance parameters such as sensitivity, sharpness, dynamic range, color rendition.

Continued focus on improving light sensitivity is driven by the need to capture pictures in non-daylight conditions without the need for artificial lighting. This is fully possible with today's CMOS and CCD technology by using relatively large pixels (e.g. 4μm x 4μm or above). But further improvements are needed for smaller pixels. Technologies such as backside illumination, hybrid sensors, pixel summation and in-pixel amplification are being introduced at this years conference.

Image sharpness is another parameter that is challenged by small pixels. Pixels have become so small that fundamental physical (diffraction) limits are starting to play a role (the pixel size is in fact only a few times larger than the wavelength of the light). The associated reduction in signal-to-noise performance is partly compensated by increased pixel count which has the effect of averaging out (laterally) the noise.

# Trends in Sensors: The view from 30,000 feet!

Where are sensors going?

- They are getting smarter and finding increasing use in a wide variety of applications. Most sensors will have a digital output. Also increasingly advanced IC technology means that ever more complex algorithms can be implemented at chip level.

- Not everything gets easier in advanced CMOS processes, as the performance of the substrate *bipolar* transistors on which most of today's temperature sensors are based becomes increasingly poor. One promising way around this issue is to create sensors based on thermal oscillators.

- Sensors are beginning to penetrate the worlds of biology and chemistry. Examples of this trend are the development of gas sensors, DNA sensors, cochlear implants, retinal implants, and ultra-low-power circuits that enable battery-powered implantable systems.

- Inertial sensors: Are already appearing in the mass market handheld/portable and gaming markets, but what is going to be the best solution: two-chip or one-chip implementations? This has been a long-standing debate. The advantage of two-chip solutions is that both the MEMS sensor and the electronics can be independently optimized and maybe stacked to reduce the floor space. On the other hand, one-chip solutions minimize stray capacitances and can be simply and cheaply packaged. As far as performance is concerned, the result today seems to be a dead heat, as state-of-the-art two-chip solutions now offer performance comparable to the best one-chip solutions.

- For years, MEMS resonators have been coming, but at last some practical applications are emerging. Some examples are FSK transmitters and miniature frequency references that replace bulky crystal based oscillators.

- New MEMS applications are still being found, as is shown by the development of an advanced electric field sensor for photocopiers.

- While the pure imaging pixel wars rage, two main frontiers remain: stereo imaging and wide dynamic range. These problems are being tackled both at the system level, and the pixel level. A lot can still be achieved with innovative design solutions at the pixel level and this is still an area of academic research.

# MEMORY

- **Overview**
- **Featured Papers**
- **Panel**
- **Special-Topic Session**
- **Tutorial**
- **Forums**

# ISSCC 2006 – MEMORY

**Subcommittee Chair:** *Katsuyuki Sato, Infineon, Tokyo, Japan*

# *OVERVIEW*

## MOST-SIGNIFICANT RESULTS

- NROM-based flash memory achieves four bits of storage in a single memory cell **[7.1]**
- Smallest 8Gb multi-level NAND flash memory ever reported **[7.7]**
- 10MB/s program throughput achieved by a sub-60nm multi-level NAND flash memory. **[7.7]**
- Powerful 5-bit error-correction scheme embedded into a monolithic multi-level NAND flash memory. **[7.6]**
- An 8Gb/s deca-data-rate SDRAM incorporates CRC I/O error-detection **[8.1]**
- A range-matching TCAM with 2.5x data-storage efficiency **[8.6]**
- 5Ghz SRAM design for high-performance CPU **[34.1]**
- Thyrister-based volatile memory in nanoscale CMOS **[34.6]**

## APPLICATIONS AND ECONOMIC IMPACT

- Storing 4 bits of data in a single memory cell reduces overall cost per bit. **[7.1]**
- Powerful 5-bit embedded error correction in a Non-Volatile memory provides high reliability while simplifying memory-system design. **[7.6]**
- Fast write throughput and high density flash memory meets demands of high-resolution digital cameras and mass storage for digital music players. **[7.7]**
- A high-bandwidth with reliable I/O data validates ever-advancing high-speed memory applications. **[8.1]**
- 2.5x data storage efficiency opens an economical packet-classification application. **[8.6]**
- High-performance and high-bandwidth needs met for future microprocessors. **[34.1]**
- An alternative SRAM-replacement technology is demonstrated with compelling density. **[34.6]**

## SPECIAL-TOPIC SESSION

**Emerging & Disruptive Memory Technologies [SE4]**

## TUTORIAL

**Multi-Level Cell Design for Flash Memory [T5]**

## FORUM

**Embedded SRAM Design [F2]**

# *Flash Memory Continues to Aggressively Reduce Bit Cost While Improving Performance*

## A 4b/Cell NROM 1Gb Data-Storage Memory [7.1]

*Saifun Semiconductors; Macronix*

## A 56nm CMOS 99mm$^2$ 8Gb Multi-Level NAND Flash Memory with 10MB/s Program Throughput [7.7]

*Toshiba, SanDisk*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- 63nm is the most-aggressive lithography reported to date for flash memory.
- 2 bits-per-cell Non-Volatile memory currently commercially available.
- 6MB/s Fastest NAND flash write throughput time reported to date.

## NOVEL CONTRIBUTIONS

- NROM achieves 4-bits-per-cell storage **[7.1]**
- Fabricated in a 56nm process lithography **[7.7]**
- 10MB/s program-throughput time achieved. **[7.7]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Advanced lithography and 4-bits-per-cell data storage offer significant reduction in bit cost for mass-storage portable-electronics applications **[7.1, 7.7]**
- 60% improvement in flash memory write-throughput time for mass-data storage applications **[7.7]**

# *Embedded Error-Correction Scheme Improves Memory Reliability and Performance While Simplifying System Design*

## A 4Gb 2b/cell NAND Flash Memory with Embedded 5b BCH ECC for 36MB/s System Read Throughput [7.6]

*ST Microelectronics; Hynix Semiconductor*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Current NAND-flash error-detection and correction done in the system
- Fastest system read-throughput time previously reported before error correction is 23MB/s

## NOVEL CONTRIBUTIONS

- Powerful 5-bit error-correction scheme embedded in a monolithic memory **[7.6]**
- 36MB/s memory-system-throughput time achieved **[7.6]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Powerful embedded error scheme improves memory reliability and simplifies memory-system design. **[7.6]**
- Memory design and architecture advancements achieve fast system-data-download times. **[7.6]**

# An 8Gb/s/pin 9.6ns Row-Cycle 288Mb Deca-Data- Rate SDRAM with an I/O Error-Detection Scheme [8.1]

*Samsung*

## PRESENT STATE OF THE ART

- CRC I/O error detection is creating bubbles between data bursts which are wasting bandwidth. Bandwidth can only be recovered by adding more pins to the memory, complicating system design
- Commodity DRAM Row Cycle time is approaching 40ns
- Row Cycle time in Fast Cycle DRAMs is reaching 20ns

## NOVEL CONTRIBUTIONS

- Deca-Data-Rate enables 100% utilization of bus bandwidth, including I/O-Error Correction by bursting 10bits of data within one clock cycle. Bubble-free transmission is possible without additional pins, greatly simplifying transmission at high data-rates **[8.1]**
- Penta-Phase PLL optimized for clocking 10-bit bursts **[8.1]**
- Row Cycle reduced to 9.6ns with Twin Cell, Shorter Word-lines and Direct Sensing **[8.1]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Enables higher-performance multimedia systems **[8.1]**
- Provides enhanced gaming experience **[8.1]**
- Error correction improves system reliability and chip lifetime **[8.1]**
- Raises the bar for competitive DRAM performance **[8.1]**

# *TCAMs Widen Internet Applications*

## TCAM for IP-Address Lookup Using Tree-Style AND-type Match Lines and Segmented Search Lines [8.6]

*National Chung Cheng University*

## A Storage- and Power-Efficient Range-Matching TCAM for Packet Classification [8.7]

*Seoul National University*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- TCAM is required to be ever more performance-intensive for IP address lookup in network applications.
- Data storage in the TCAM array is inefficient for packet-classification uses.

## NOVEL CONTRIBUTIONS

- A tree-AND structure provides x4 improvement in speed x energy product over past world record. **[8.6]**
- 2.5 times more efficient use of memory by a range-matching memory-cell design. **[8.7]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Fastest search can speed up a wide range of Internet applications **[8.6]**
- Use of economical TCAM cell can realize viable large-scale packet-classification operations. **[8.7]**

# *High-Frequency on-Die SRAM for Future CPUs*

## A 5GHz 64KB Dual-Read Data Cache for Power6™ Processor

**[34.1]**
*IBM*

### PRESENT STATE OF THE ART *(THE PROBLEM)*

- Need for cache to meet demands in frequency and bandwidth from high-performance CPUs

### NOVEL CONTRIBUTIONS

- Novel cache configuration and architecture meets high-performance needs **[34.1]**

### CURRENT AND PROJECTED SIGNIFICANCE

- Enables the cache to meet bandwidth needs of high-performance CPUs **[34.1]**

# *An Emerging Scalable SRAM Technology*

## Thyristor-Based Volatile Memory in Nano-Scale CMOS [34.6]

*T-RAM Semiconductor*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- 6T SRAM in 130nm technology occupies 2.21μm$^2$, with 1ns R/W time
- 6T SRAM in 90nm technology occupies 1μm$^2$, with 0.63ns R/W time is in production today
- 1T1C eDRAM in 90nm technology occupies 0.24 μm$^2$, with, 3.2ns R/W time

## NOVEL CONTRIBUTIONS

- T-RAM projected to provide 4x cell area advantage over 6T SRAM **[34.6]**
- Provides non-destructive read, and hidden refresh **[34.6]**
- Scalable to future SOI and FinFET technologies **[34.6]**
- Combines the density of DRAM with the performance of SRAM **[34.6]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Application to high-speed high-density external and embedded cache memory **[34.6]**
- Impact due to low added-processing cost **[34.6]**
- Competition for eDRAM and SRAM **[34.6]**

# *SPECIAL-TOPIC SESSION*

# *Emerging & Disruptive Memory Technologies*

*Organizer/Chair:* ***Sreedhar Natarajan****, Emerging Memory Technologies*

## OVERVIEW

- Demanding semiconductor industry requirements for low power, high performance and high density are making it imperative to evaluate new memory technologies
- Technology scaling is in addition making it difficult to come with memory solutions to solve the leakage and high density requirements.
- Need for increased storage and terabit based memories are approaching rapidly than expected.

## OBJECTIVE

- To highlight a high scalable resistance change memory using solid electrolytes
- To expose the benefits of SOI for memory technologies at 65nm and below.
- To highlight some of the alternatives to SRAM type memories
- Is flash storage adequate for future or do we need alternative?

## CHALLENGE

- Potential disruptive memory technologies for future to solve the
- Terabit storage limit
- SRAM performance and power requirements
- Scalabiity

# STRUCTURE

- The first two talks will address the scalability of electrolyte based memories and hard disk drive technologies necessary to achieve terabit storage. The final two papers will address new memory technologies and bitcell in SOI and comparison to conventional SRAM.

# Speakers and Specialities

- **Dr. Kazutami Arimoto, Renesas Technology, Osaka, Japan**
  **"SOI Twin Cell RAM technology"**

  A discussion and analysis of the breakthrough Twin Cell SOI Memory technology for 45nm and beyond.

- **Bruce Bateman, T-RAM, San Jose, CA**
  **"Thyristor RAM: An Evolving and Disruptive Memory Technology"**

  A discussion of the first production worthy new high performance random access memory that is inexpensively retrofitted to existing CMOS process and scalable beyond 45nm.

- **Dr. Barry Stipe, Hitachi, San Jose, CA**
  **"Small Hard-Disk Drives versus Solid-State Storage"**

  A discussion of the HDD technologies necessary to achieve greater than a Terabit of memory capacity in a sub-CF form factor and a comparison of Flash and HDD roadmaps are reviewed.

- **Dr. Michael Kozicki, Axon Technology , Scottsdale, AZ**
  **"Highly-Scalable Resistance Change Memory using Solid Electrolytes"**

  This talk describes a scalable resistance memory that involves switching elements which utilize the reduction of nanoscale quantities of metal ions in solid electrolyte films and will discuss technology and design aspects for ultra high density memory and storage

# RECAP

- To educate the audience on new memory technologies like SOI and Thyristor based memories

- To highlight the potential need for terabit storage and solve the scalability issues in current memory technologies

# *Tutorial*

# Multi-Level Cell Design for Flash Memory

*Mark Bauer, Intel, Folsom, CA*

## OVERVIEW

Flash Memory with multi-level-cell was first reported at ISSCC in 1995. Since then it has become commercially available in high volume from many semiconductor manufactures. Multi-level design achieves the storage of more than two analog levels in a flash memory cell. If four analog levels are stored in a single flash cell, two digital bits of information can be programmed into the cell. This essentially reduces the cell area by half relative to single bit storage and can approach the same cost savings from a memory array perspective as a lithography generation. This tutorial explores some of the basic Multi-Level Cell design techniques for Flash Memory and will include:

- Basic concepts of Multi-Level analog storage relative to Single-Bit-Per cell storage
- The need for precise charge placement and precise charge sensing of floating gate memory cells
- Circuit design and chip architectural techniques to achieve multi-level analog storage of more than one-bit-per-cell

## SPEAKER BIOGRAPHY

**Mark Bauer** is currently Senior Principal Engineer at Intel Corporation in Folsom, California, where he is responsible for advanced circuit design and Flash-memory technology development. He received his BSEE in Electrical Engineering in 1985 from the University of California at Davis. Upon graduation, Mark joined Intel's Memory Components Division, working on EPROM design. He started working on Flash-memory design in 1992, and was responsible for circuit-design and technology development for the first Intel StrataFlash™ memory. He has served on the ISSCC memory sub-committee since 1999. He has authored several technical papers, one of which won the Lewis Winner Award for Outstanding Paper at ISSCC (1995). He holds more than 20 patents in the field of Non-Volatile Memory.

# *FORUM*
# Embedded-SRAM Design

## Objective
This all-day forum is dedicated to the design of embedded SRAM, addressing a broad range of issues and solution for both ends of the power spectrum, including scaling and testability in sub-100nm design.

Attendance is limited, and pre-registration is required. This all-day meeting encourages open interchange in a closed environment.

## Audience
The targeted participants are circuit and test engineers working on advanced embedded SRAM development for various performance-oriented microprocessors and system LSIs.

## Scope
Embedded SRAM arrays may be optimized for performance (latency and cycle time), functionality (multi-port and multi-bank designs), and density, but a common limiting factor for embedded applications today is power optimization for applications ranging from a high-performance to mobile. This forum will cover both ends of the power spectrum, scaling issues with sub-100nm designs, and advances in the test of highly-embedded arrays, as well as the horizon for promising new embedded memory technologies.

## Program
**Kevin Zhang** (Intel) will begin by introducing some key architectural options/optimizations for large on-die cache-designs, and then discuss various circuit-design techniques for achieving high performance. Some state-of-the-art design techniques for lowering both dynamic and static power consumption while retaining the high-performance goal will also be discussed in detail.

At the other end of the power spectrum, mobile applications are driving SRAM array design to extremely low power and very low voltages. **Masanao Yamaoka** (Hitachi) will describe advanced low-voltage design techniques and the extra-power-reduction design techniques that are required for low-active power.

Memories require extensive testing to ensure chip quality, since the vast majority of chip area is occupied by memory cells. **R. Dean Adams** (Magma Design Automation) will begin by describing how test-pattern selection requires a deep understanding the memory design to determine how and where defects can exist and result in defective electrical operation. A BIST system applies test patterns to the memory and analyzes the resulting read data. Further DFT techniques are utilized to check margins for memory timing and sense-amplifier signal values.

As device channel lengths shrink down to tens of nanometers, SRAM designs meet new issues and challenges that require changes in the way designs are done.

**Takayuki Kawahara** (Hitachi) will reexamine the scaling issues, their impact on cell operation and stability, and design for manufacturability, within these new constraints. A new design methodology will be presented. Moreover, soft-error issues, especially for cosmic-ray impact and for some new kinds of SRAM cell are discussed.

As high-performance multi core processors are developed along with higher-frequency operation. SRAMs have to cope with high junction temperature, fast random cycle time, and high bandwidth, with higher density requirements. In order to meet those requirements, aggressive shrinking, 3D stacking, and other new memory technologies are being developed.

**Hyun-Geun Byun** (Samsung) will address attractive alternatives to conventional 6T SRAM solutions such as: Pseudo SRAMs, 3D-SRAM, and other new memories such as: UtRAM, CellularRAM, FCRAM or Cosmo RAM for mobile applications, and BEDDR3 for cache memory.

# SIGNAL PROCESSING

- **Overview**
- **Featured Papers**
- **Special-Topic Session**
- **Tutorial**

# ISSCC 2006 – SIGNAL PROCESSING

**Subcommittee Chair:** *Wanda Gass, Texas Instruments, Dallas, TX*

# *OVERVIEW*

## MOST-SIGNIFICANT RESULTS

- First-published DSSS UWB baseband transceiver for wireless ad-hoc networks. **[14.5]**
- 5mW MPEG4 video encoder and 160Kgate HDTV video decoder provide low-power and low-cost solutions. **[22.3, 22.6]**
- Vertex processor delivers 120Mvertices/s 3D-geometry performance which is 3x the performance and half the power of previous chips. **[22.4]**

## APPLICATIONS AND ECONOMIC IMPACT

- UWB digital baseband delivers self-configuring (ad-hoc) networks with more than 450Mb/s data rate **[14.5]**
- Encoders and decoders extend the battery life of mobile phones while sending and receiving video. **[22.3, 22.6]**
- Graphics processor enables life-like games on mobile phones, PDAs, and portable multimedia players **[22.4]**

## SPECIAL-TOPIC SESSION

**Power Aware Signal Processing [SE3]**

## TUTORIAL

**Cellular-Phone Applications Trend and DSP Technology** [**T6]**

# *Ultra-Wide Band (UWB) Enables Higher-Data-Rate Personal-Area Networks*

## A DSSS UWB Digital PHY/MAC Transceiver for Wireless Ad-Hoc Mesh Networks with Distributed Control [14.5]

*Sony*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Today's networks are primarily based on 802.11 with a centrally-managed network infrastructure (access points) and sub-100Mb/s throughput
- New UWB standards are under development with two competing system concepts: MB-OFDM and DSSS

## NOVEL CONTRIBUTIONS

- The first-published DSSS UWB PHY/MAC **[14.5]**
- Low-power implementation: maximum of 181 mW **[14.5]**
- Ad-hoc network without a central controller with a maximum of 64 terminal nodes **[14.5]**
- Ranging accuracy of +/- 7.5 cm for optimal routing **[14.5]**
- Maximum of 378Mb/s throughput **[14.5]**
- DSSS UWB ad-hoc network can coexist with 802.11 narrowband networks **[14.5]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Short-distance (personal-area and intra-room network) with high data-rate **[14.5]**
- Direct peer-to-peer wireless communication without a centrally-controlled network infrastructure **[14.5]**
- Wireless communication of HD video using multiple nodes (to cover larger distance) **[14.5]**

# *A 120 Mvertices/s Vertex Shader for Mobile Applications*

### A 120 Mvertices/s Multithreaded VLIW Vertex Processor for Mobile Multimedia Applications [22.4]

*Korea Advanced Institute of Science and Technology*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Embedded 3D-graphics engine is widely used in multimedia devices such as mobile phones, PDAs, and Portable Multimedia Players (PMP).
- Multimedia systems increasingly require better performance and functionality of the 3D-graphics hardware within limited power consumption.

## NOVEL CONTRIBUTIONS

- A new Vertex processor provides up to 120Mvertices/sec of 3D-geometry performance **[22.4]**
- A new Vertex processor performs geometry transformation in a single cycle **[22.4]**
- The 4-threaded architecture removes data dependencies that causes a pipeline stall **[22.4]**
- The new architecture reduces the total energy consumption to 42.7% of a conventional SIMD **[22.4]**
- The processor supports the Vertex Shader Model 3.0 and the vertex shader of the OpenGL ES 2.0 (except for the texture lookup function) **[22.4]**
- The processor supports all static/dynamic flow controls in VS3.0 without any penalties **[22.4]**
- The new embedded pre- & post-vertex caches reduce the bandwidth of the data bus up to 65%, and improve the performance up to 19.7%, respectively **[22.4]**

## CURRENT AND PROJECTED SIGNIFICANCE

- This vertex shader has the potential for wide incorporation in embedded 3D-graphics applications such as mobile phones, PDAs, and PMPs. **[22.4]**

# *Ultra-Low-Power Video Compression for Mobile Applications*

## A 160Kgate 4.5KB SRAM H.264 Video Decoder for HDTV Applications [22.3]

*National Chung-Cheng University*

## 5mW MPEG-4 SP Encoder with 2D-Bandwidth- Sharing Motion Estimation for Mobile Applications [22.6]

*National Taiwan University; Novatek; Quanta Computer; MediaTek*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Power consumption for motion estimation and DCT needs to be further reduced
- Mobile applications need ultra-low-power to save battery life

## NOVEL CONTRIBUTIONS

- Ultra-low-power architecture design **[22.3, 22.6]**
- Motion estimation with only 32-pixel reference memory **[22.6]**
- Content-aware DCT **[22.6]**
- High-performance content-adaptive entropy decoding **[22.6]**
- Internal memory optimization **[22.3]**

## CURRENT AND PROJECTED SIGNIFICANCE

- The architectures presented can be used for most mobile applications, including mobile phone, PDAs, digital camera, and 3G phones. **[22.3, 22.6]**

# *SPECIAL-TOPIC SESSION*

## *Power-Aware Signal Processing*

*Organizer:* ***Rajeevan Amirtharajah****, University of California, Davis, CA*
*Chair:* ***Wanda Gass****, Texas Instruments, Dallas, TX*

## OVERVIEW

- Implementing the vision of ubiquitous multimedia applications for a mobile world will require incorporating power awareness at all levels of system design. New applications such as mobile digital television demand unprecedented levels of performance. Battery lifetime, size, and device cost are fundamental constraints for consumer products. Power aware digital signal processing will be a major component of next-generation portable multimedia platforms such as cellular phones beyond 3G, handheld gaming devices, MP3 players, and digital cameras. In addition, power awareness will allow wireless sensor networks to implement ambient intelligence.

## OBJECTIVE

- To describe novel approaches to scaling power consumption with processor performance, user requirements, and power availability from batteries or energy harvesting from the environment.

## CHALLENGE

- Managing power consumption while supporting the performance requirements of next-generation mobile multimedia and wireless sensor network applications.

# STRUCTURE

- Rajeevan Amirtharajah, University of California, Davis: "*An Energy Scalable Computational Array for Sensor Signal Processing*"

  Energy scavenging from the environment can extend node lifetime and decrease maintenance costs for wireless sensor networks. This talk describes a computational array targeting energy scavenging sensors, which implements energy scalability for basic signal processing operations.

- Liang-Gee Chen, National Taiwan University: "*Power Aware Multimedia*"

  Reconfigurable hardware can be used to adapt power consumption for multimedia signal processing. This talk presents a design example using video coding to highlight the challenges and opportunities for power adaptation using a reconfigurable datapath.

- Clay Dunsmore, Texas Instruments: "*Power Management for Digital Still Camera*"

  This talk describes techniques to support billions of operations per second of computing performance within 200mW for a consumer digital still camera.

- Richard Kleihorst, Philips Research Laboratories: "*Wireless Smart Vision for Ambient Intelligence*"

  The goal of ambient intelligence is to create environments which are aware of and responsive to the presence of people. This talk discusses hardware and software approaches that enable computationally intensive operations such as facial recognition to be integrated with ambient sensing devices.

# RECAP

- This session will present leading edge work from academia and industry on approaches to implementing adaptive power management for a variety of multimedia and signal processing applications.

# *Tutorial*

# CELLULAR-PHONE APPLICATIONS; TRENDS AND DSP TECHNOLOGY

*Masafumi Takahashi, Toshiba, Kawasaki, Japan*

## OVERVIEW

As the cellular phone market spreads all over the world, the addition of new features is attracting more consumers. These new features are enabled by digital signal processing (DSP), which delivers high performance while keeping the power consumption low. This session will focus on multimedia applications that enable these new features and the DSP technologies that enable high performance, low cost and low power. The topics to be covered include;

- Multimedia applications on cellular phones
- Video and audio processing algorithms
- Multimedia DSP architectures
- Low-power circuits

## SPEAKER BIOGRAPHY

**Masafumi Takahashi** is currently a Chief Specialist at Toshiba Corporation Semiconductor in Kawasaki, Japan, where he is involved in the development of multimedia SoCs for mobile applications, focusing on audio-visual processing architectures and low-power circuit techniques. He joined Toshiba Corporation in 1987, where he was engaged in research on multiprocessor architectures until 1996. He has been a member of the ISSCC Signal Processing Sub-Committee since 2004. He received his ME from the University of Tsukuba, Japan in 1987.

# NOTES

# TECHNOLOGY DIRECTIONS

- **Overview**
- **Featured Papers**
- **Special-Topic Session**
- **Tutorial**
- **Forum**

# ISSCC 2006 – TECHNOLOGY DIRECTIONS

**Subcommittee Chair:** *Anantha Chandrakasan, MIT, Cambridge, MA*

# *OVERVIEW*

## MOST-SIGNIFICANT RESULTS

- Electronic "nose" detects spoilage of wine at levels of 10 parts per million **[15.3]**
- Development of a Braille sheet allows e-books for the blind that update in 2 seconds **[15.4]**
- First demonstration of functional RFID tags built in organics, operating at 13.56MHz **[15.2]**
- 71,000 TFT devices integrated on plastic realize cryptographic security RFID **[15.6]**
- 0.15mm x 0.15mm RFID chip with 128-bit ROM and antenna contacts on top and bottom. **[17.1]**
- 3.4Mb/s data rate in a 13.56 MHz RFID front-end **[17.2]**
- 50-to-75 GHz 0.13μm CMOS LNA achieves > 20dB gain **[17.8]**
- Combination of 2.4GHz BAW resonators and 0.18μm CMOS radio front-end achieving 50dB image rejection with 1.8mW power consumption **[17.7]**
- Demonstrated generation of 1 microwatt of electrical power from a 1 milliCurie of benign Nickel-63 nuclear-energy source. **[23.1]**
- First experimental comparison of comprehensive building blocks in FinFET and Triple-Gate transistor technologies. **[23.2]**
- Demonstrated 1 Terabit per second data transfer between 3D integrated chips via inductive coupling over an area of 2 square millimeters and energy consumption of 3 picoJoules per bit. **[23.4]**
- Optical clocking of 5-to-10GHz with a silicon nano-photodiode. **[23.5]**
- Neuro-interface chips locally process signals captured from 100 electrodes and radio-transmit them outside the body **[30.1, 30.2]**
- Realization of a MEMS-based reusable biosensor for identifying and monitoring cardiovascular-risk biomarkers (that is, C-Reactive proteins) **[30.6]**

# APPLICATIONS AND ECONOMIC IMPACT

- 0.15mm x 0.15mm RFID tag-- a million tags per wafer: silicon cheap enough to tag anything. **[17.1]**
- FBARs integrated directly on silicon. Provide fewer components for smaller lighter longer-battery-life cell phone. **[17.5,17.6,17.7]**
- Long-life energy source for sensor networks and other ultra-low-power systems. **[23.1]**
- Area- and energy-efficient high-bandwidth data communication between 3D integrated chips without the need for high-density through-silicon vias. **[23.4]**
- High-frequency optical interconnect using silicon nano-photodiodes with low power loss, small crosstalk, and reduced EMI interference. **[23.5]**
- Neuro-interface chips enable prosthesis directly controlled by the brain to assist impaired people **[30.1 and 30.2]**
- Wearable health-monitoring microsystems **[30.6]**

# TUTORIAL

**3D Integration [T7]**

# FORUM

**Circuit Design in Emerging Technologies [F3]**

# *Very-Low-Cost Systems*

## A 13.56MHz RFID System Based on Organic Transponders [15.2]

*Phillips Research*

## An Organic FET SRAM for Braille-Sheet Display with Back Gate to Increase Static Noise Margin [15.4]

*University of Tokyo*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Organic devices have produced only small-scale circuits
- Organic devices significantly trail their silicon counterparts in performance
- Low-cost devices are required for many mass markets such as RFID
- CMOS devices require high-temperature processing, preventing use of flexible/low-cost substrates

## NOVEL CONTRIBUTIONS

- 2000 organic transistors demonstrate a high level of integration on a plastic substrate at low cost: highest level of integration reported **[15.2]**
- First demonstration of functional tags built in organics, operating at 13.56MHz **[15.2]**
- Performance of updatable a Braille sheet improved from 34 seconds to 2 seconds, allowing e-books for the blind **[15.4]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Cheap barcode replacements based on organic RFIDs **[15.1, 15.2]**
- Organic Devices, TFT CMOS on plastic **[15.2,15.4]**
- E-books for the blind that can update in seconds **[15.4]**
- Smart RFID cards with encrypted data for personal ID with security **[15.6]**

# Smaller Cheaper Higher-Speed RFID

## An SOI-Based 7.5µm-Thick 0.15x0.15mm$^2$ RFID Chip [17.1]

*Hitachi; Renesas Technology*

## A Passive UHF RFID Tag LSI with 36.6%-Efficiency CMOS-Only Rectifier and Current-Mode Demodulator in 0.35µm FeRAM Technology [17.2]

*Fujitsu*

## A 3.4Mb/s RFID Front-End for Proximity Applications Based on a Delta-Modulator [17.3]

*CEA-LETI*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- RFID chips are small and cheap, but still cost around 10cents each. This means that they are still too expensive for many applications.
- Silicon costs make up a substantial part of this price, and driving the price down requires making the dies smaller.
- Emerging applications of RFID require longer-range communication in addition to higher data rates.

## NOVEL CONTRIBUTIONS

- Use of SOI-based CMOS makes possible RFID chips measuring 0.15mm x 0.15mm x 7.5µm. **[17.1]**
- State-of-the-art RFID tags may be twice this size. **[17.1]**
- A CMOS full-wave rectifier with a ferroelectric capacitor improves power efficiency by more than double enabling 4.3m-range UHF communications at a rate of 129tags/s read-and-write operation. **[17.2]**
- Multilevel-modulation technique in a 13.56MHz RFID achieves ultra-high-speed communications up to 3.4Mb/s. **[17.3]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Low-cost high-speed RFIDs open up new application fields **[17.1, 17.2, 17.3]**

# *Miniaturized Radios*

## A 5.4GHz 0.35µm BiCMOS FBAR Resonator Oscillator in Above-IC Technology [17.5]

*LAAS-CNRS; CSEM; CEA-LETI*

## A Low-Power 2.4GHz CMOS Receiver Front-End Using BAW Resonators [17.7]

*CSEM*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Need for integration of high-Q passive components, such as bulk acoustic wave (BAW) filters, on top of an IC to avoid external components, reduce (BoM), and decrease the transceiver cost.
- Need for new low-power transceiver architectures for multiband and multistandard wireless communication

## NOVEL CONTRIBUTIONS

- First-time demonstration of integrating BAW filters above BiCMOS at 5.4GHz, and connecting them to the IC below **[17.5]**
- Increased integration avoiding off-chip components for single-chip RF transceiver **[17.5,17.7]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Highly integrated miniaturized low-power radios for multiband multistandard wireless **[17.5,17.7]**

# *mm-Wave CMOS is Here to Stay!*

## A 60GHz CMOS VCO Using On-Chip Resonator with Embedded Artificial Dielectric for Size, Loss and Noise Reduction [17.4]

*University of California, Los Angeles*

## A Miniature V-Band 3-Stage Cascode LNA in 0.13μm CMOS [17.8]

*National Taiwan University*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Need for low-cost mm-Wave integrated circuits for high-data-rate communication, and other consumer applications, such as automotive radars for collision avoidance

## NOVEL CONTRIBUTIONS

- On-chip traveling-wave structures for high-Q resonators with reduced area **[17.4]**
- Miniaturized 50 to 75GHz three-stage cascade CMOS LNA achieving 20dB gain with 7.1dB noise figure in a 0.46mm$^2$ die **[17.8]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Innovative CMOS-compatible passive structures and design allow performance traditionally reserved for III-V-compound semiconductors **[17.4,17.8]**

# *Technology and Architecture Directions*

## Active Circuits for Ultra-High Efficiency Micropower Generators using Nickel-63 Radioisotope [23.1]

*Cornell University*

## Circuit Design Issues in Multi-Gate FET CMOS Technologies [23.2]

*Infineon, ATDF, Texas Instruments; Soitec*

## A 1Tb/s 3W Inductive-Coupling Transceiver for Inter-Chip Clock and Data Link [23.4]

*Keio University; NEC; University of Tokyo*

## Optical Interconnect Technologies for High-Speed VLSI Chips Using Silicon Nano-Photonics [23.5]

*NEC*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Emerging technologies and architectures for improved power, energy, and performance.

## NOVEL CONTRIBUTIONS

- Miniature integrated nuclear-to-electrical energy conversion with over 30% efficiency. **[23.1]**
- Experimental comparison of analog and digital building blocks in FinFET and Triple-Gate transistor technologies. **[23.2]**
- 1 Terabit per second data transfer between 3D integrated chips via inductive coupling with an area of 2 square millimeters and energy consumption of 3 pico Joules per bit. **[23.4]**
- Optical interconnection technologies using silicon a nano-photodiode with less than 10aF parasitic capacitance for more-than-5GHz operation. **[23.5]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Long-life energy source for sensor networks and other ultra-low power systems. **[23.1]**
- Enables area and energy efficient high-throughput data communication between 3D integrated chips without the need for high-density through-silicon vias. **[23.4]**
- High-frequency optical interconnect using silicon nano-photodiodes with low power loss, small cross talk, and reduced EMI interference. **[23.5]**

# Neuro-Interface Chips Send Brain-Control Signals to Prosthesis for Impaired People

## Neurons to Silicon: Implantable Prosthesis Processor [30.1]

*Stanford University*

## A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural-Recording System [30.2]

*University of Utah*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Due to accident injuries, half a million people in the USA cannot move properly anymore, and cannot live a normal life, as their spinal cord, connecting the brain to the limbs, is damaged.
- The quality of life for these people would greatly improve if the control signals from the brain cortex could be collected and used to control mechanical limbs, personal computers, and other appliances.
- Implanted circuits capable of recording neural signals (with up to 1000 sensing sites) have been developed in past years. To help people, these systems should be able to send the recorded data outside the body using a radio link. To keep this process low-power-enough for an implantable chip, the large amount of neural data (~100kb/s per neural channel) must be locally processed to transmit only essential information. No fully-integrated solution has been presented yet.

## NOVEL CONTRIBUTIONS

- The first fully-integrated neuro-interface SoC processes neural signals captured by a 100-electrode array and transmits them outside the body using a 433MHz FSK radio. It receives the needed power (13.5mW) via an inductive link. **[30.2]**
- An implantable chip minimizes the power needed to process neural data dynamically, adapting the resolution of its analog front-end. It also exploits beam-forming techniques to optimize inductive power transfer. **[30.1]**

## CURRENT AND PROJECTED SIGNIFICANCE

- These new chips promise to enable prosthetic devices directly-controlled by the brain **[30.1, 30.2]**

# *Silicon for Biology*

## A Wireless Bio-MEMS Sensor for C-Reactive-Protein Detection Based on Nanomechanics [30.6]

*National Taiwan University*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Current bioanalysis methods are commonly based on the optical detection of fluorophore labels. This requires large macroscale platforms and instrumentation.
- Current-biosensing approaches require chemical dissociation or cleaning procedures, and therefore cannot be conveniently reused, particularly in portable and wearable biomonitoring systems.

## NOVEL CONTRIBUTIONS

- MEMS cantilever senses the mass loading of cardiovascular-related proteins (CRP) **[30.6]**
- Soft polymer materials implement microfluidic channels **[30.6]**
- A low-frequency electric field is used to dissociate sensed proteins **[30.6]**
- Biosensing is carried out using a wireless link **[30.6]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Reusable biosensors open the field for new portable/wearable health-monitoring applications **[30.6]**
- Improved biosensors that require minimal human interaction may lead to a higher quality of life **[30.6]**

# *Enjoying Portable Music without Wire*

## A 2Mb/s Wideband Pulse Transceiver with Direct-Coupled Interface for Human-Body Communications [30.4]

*KAIST*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Portable Multimedia System requires WIRED ear-phones
- Wireless interconnection(Bluetooth) consumes high power
- Data transmission using the human body suffers from noise
- Compact and efficient human body communication (HBC) is required

## NOVEL CONTRIBUTIONS

- Very-low-power (0.2mW) and very-high-speed are achieved (2Mb/s) **[30.4]**
- Wideband pulse transmission method for high speed **[30.4]**
- Direct-coupled interface method for low-power/low noise operation **[30.4]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Wireless i-Pod earphones can be realized **[30.4]**
- Cellphones and other portable system will adopt this scheme
- Photograph, and even motion pictures can be enjoyed without wires

Wires for ear connection to portable audio systems are no longer needed. The long wires connecting ear-phones and portable-audio systems are an ever-lasting nuisance and Bluetooth consumes too much power and is too bulky. By using Human Body Communication, wires can be eliminated and large amounts of data can be transmitted through the human body at high speed with low power (2Mb/s and 0.2mW), and interference noise can be reduced.

Wideband Pulse method and Direct-Coupled Interface are used.

Compared to Bluetooth, speed is x2 and power consumption is 1/10.

# *SPECIAL-TOPIC SESSION*

# *Highlights of 2005 A-SSCC and Symposium on VLSI Technology*

*Organizers:* **Takayasu Sakurai**, University of Tokyo, Tokyo, Japan
**Ian Young,** Intel, Hillsboro, Oregon
**Takayuki Kawahara**, Hitachi, Kokubunji, Tokyo, Japan
*Chair:* ***Yoshiaki Hagihara****, Sony, Tokyo, Japan*

## OVERVIEW

- A-SSCC is the international forum for advances in solid-state circuits design in Asia, and is fully supported by the IEEE Solid-State Circuits Society. This Conference was recently initiated in Hsinchu, Taiwan, in 2005, as a result of the recent significant expansion of LSI design activity in Asia. Among the many papers accepted following a rigorous selection process, three have been chosen for presentation at ISSCC 2006. These originate from Korea, Taiwan, and China, and cover several topics: a high-performance-serial link; an extremely wide-range amplifier; and healthcare instrumentation; which represents the totally balanced growth of LSI design in Asia. On the other hand, Symposium on VLSI Technology has celebrated its twenty-fifth anniversary in 2005, in Kyoto, Japan. This Conference offers a unique opportunity for engineers and scientists to share the entire VLSI spectrum from technology to circuits through its pairing with the Symposium on VLSI Circuits. Since the scope of the Technology Symposium includes new concepts and breakthroughs in VLSI devices and processes, we have selected three papers from around the world, related to advanced transistor technology.

## OBJECTIVE

- This Special-Topic Session highlights papers from the A-SSCC 2005 and from the Symposium on VLSI Technology 2005.

## CHALLENGE

- ISSCC operates in the context of many other top-ranked conferences with both geographical and technical specializations
- A specific need exists for interaction with the expanding emphasis of VLSI in Asia

# STRUCTURE

**Won-Jun Choe, Seoul National University, "A 3-mW 270-Mbps Clock-Edge Modulated Serial Link for Mobile"**

A single, DC-balanced differential channel, simple DLL-based clock-edge modulated serial link for mobile display interface is presented. A prototype clock edge modulation transceiver, implemented in a 0.18µm CMOS process, dissipates 3.12mW when operating at 270Mb/s and 1.2V.

**Baoyung Chi, Tsinghua University, "A Low Power Digital IC Design Inside the Wireless Endoscopy Capsule"**

A image compression algorithm based on Bayer image format and its corresponding hardware architecture inside the wireless endoscopic capsule is discussed. The capsule system enables the diagnosis of the whole human digestive tract and provides real time endoscopic image monitoring.

**Chihun Lee, National Taiwan University, "A 0.1-25.5-GHz Differential Cascaded-Distributed Amplifier in 0.18-µm CMOS Technology"**

A differential distributed amplifier employs a loss-compensation L-section to increase the bandwidth of the interstage by a factor of 3.5. The chip, fabricated in a 0.18µm CMOS process, achieves a gain of better than 15dB and a pass bandwidth of 100MHz to 25.5GHz while consuming 171mW from a 1.9V supply.

**Aaron Voon-Yew Thean, Freescale Semiconductor, "Super-Critical Strained-Si Directly On Insulator (SC-SSOI) CMOS Based on High-Performance PD-SOI Technology"**

Superior isolation has enabled partially-depleted SOI devices to achieve high performance for strict power budget embedded microprocessor applications. The presentation will focus on the behavior of aggressively scaled transistors under high biaxial strain and highlights its impact on transistor electrostatics, gate leakage and electronic transport.

**Naohiko Kimizuka, NEC, "Ultra-Low Standby Power (U-LSTP) 65nm node CMOS Technology Utilizing HfSiON Dielectric and Body-biasing Scheme"**

This paper reports 65nm node ultra-low standby power CMOS technology, utilizing reverse body-biasing and a $V_{dd}$ control scheme. By using nitrided hafnium silicate (HfSiON) film as gate dielectric, we have reduced $I_g$ using well-optimized fabrication process, the record $I_{on}/I_{standby}$ ratio, $I_{on}$ of 510/220µA/µm with $I_{standby}$ of 23/23pA/µm, are obtained at $L_g$=55nm.

**Lars-Åke Ragnarsson, IMEC, "High Performing 8Å EOT HfO2 / TaN Low Thermal-Budget n-channel FETs with Solid-Phase Epitaxially Regrown (SPER) Junctions"**

High-performing ultrathin *n*-channel transistors with TaN-gated $HfO_2$ are demonstrated. A low temperature (570°C) process with solid-phase epitaxially regrown junctions are used. The thinnest devices have an EOT of 8.3Å, a leakage current of 2.6A/cm$^2$ at $V_G$=1V, and a drive-current of 815µA/µm at an off-state current of 0.1µA/µm for $V_{DD}$=1.2 V.

# RECAP

- This session will provide ISSCC attendees a glimpse of developments discussed at cognate conferences.

# *Tutorial*

# 3D Integration

*Kerry Bernstein, IBM T.J. Watson Research Center, Yorktown Hts, NY*

## OVERVIEW

Limitations to continued CMOS scaling is motivating interest in technologies which improve performance by reducing latency and increasing bandwidth. 3D chip technologies come in many flavors and styles, but are receiving lots of attention lately as a means of extending power performance in high end systems. Designing for three dimensions, however, forces us to look at formerly-two-dimensional integration issues quite differently. A number of commercial offerings and research programs suggest ways of addressing these challenges. This tutorial will survey important 3D development issues which include:

- The Evolution of 3D Computing
- 3D Technology Structures and Processes
- 3D Computing Architectures
- 3D Integration EDA Enablements
- Present Commercial Offerings

## SPEAKER BIOGRAPHY

**Kerry Bernstein** is a Senior Technical Staff Member at the IBM T.J. Watson Research Center, Yorktown Hts, NY. He is currently responsible for future-product-technology definition, performance, and application. Kerry received his B.S in electrical engineering from Washington University in St.Louis, and joined IBM in 1978. He holds 50 US Patents, and is a co-author of 3 college textbooks and multiple papers on high-speed and low-power CMOS. His interests are in the area of high-performance low-power advanced circuit technologies. He is a staff instructor at RUNN/Marine Biological Laboratories, Woods Hole, MA.

# *ADVANCED CIRCUIT FORUM*

# *"CIRCUIT DESIGN IN EMERGING TECHNOLOGIES"*

## Objective

Limitations in the ability to extend CMOS scaling have motivated interest in alternative novel technologies which offer potential growth directions for high performance logic. New technologies also promise to enable applications outside the CMOS domain like large area and flexible displays. Changes in design practices which accommodate the idiosyncrasies of these emerging technologies need to be anticipated, however. A panel of well- known researchers from academia and industry will describe design techniques which will enable product design in selected proposed processes. New structures discussed will include nano-scale fabrics, organic and polysilicon TFTs, FinFETs and other multi-gate structures, Carbon nanotubes, and spin-based devices.

## Audience

This forum is intended for circuit designers and engineering students willing to gain understanding of basic design issues in the novel technologies presented.

## Scope

For each of the highlighted technologies, speakers will provide a firm understanding of the underlying technology fundamentals, and illustrate design practices that these new devices will require.

## Program

The first lecture, "Regular Fabrics for Nano-scaled CMOS Technologies", by **Larry Pileggi** explores the circuit and design methodologies which best accommodate layout-constrained logic in deeply-scaled CMOS processes. He will describe the variability advantages derived from regular fabrics. In the second talk, "Multi-gate MOSFET Design", **Gerhard Knoblinger** will describe the design paradigm changes which occur when MOSFETs are realized in more than 2 dimensions. Device quantization is an example idiosyncrasy which must be anticipated. **Eugenio Cantatore** will next take attendees through design issues associated with organic thin film devices in his talk "Design with Organic TFTs". Organic devices are already finding their way into market applications, and his talk should not be missed by those preparing to work in this field. In the fourth presentation, "Design with Polysilicon TFTs", **Tatsuya Shimoda** will share with the audience techniques which ensure successful designs in polysilicon TFT device technologies. The fifth and sixth presentations, by **Ali Keshavarzi** and **Donhee Ham** will bring essential insights to the audience on carbon nanotube and nanowire technologies. "Digital Circuits using Carbon Nanotubes: Modeling, Design, and Architectures" will teach fundamental logic digital design approaches, and will be followed by "Analog circuit design with 1D electronic devices". The sixth and final presentation of the forum, by **Stuart Parkin** will provide a glimpse of future computing using electron spin.

# WIRELESS COMMUNICATIONS

- **Overview**
- **Featured Papers**
- **Special-Topic Session**
- **Tutorial**
- **Forum**

# ISSCC 2006 – WIRELESS COMMUNICATIONS

**Subcommittee Chair:** *Trudy Stetzler, Texas Instruments, Stafford, TX*

# *OVERVIEW*

## MOST-SIGNIFICANT RESULTS

- Fully integrated UWB transceivers in CMOS **[6.4, 6.5]**
- A frequency synthesizer covering all the 14 UWB bands in CMOS **[6.7]**
- A 77GHz Phased-Array System in Silicon **[10.1. 10.2]**
- A 60GHz Transmitter and Receiver in Silicon **[10.3]**
- The first single-chip 802.11a/b/g SoC that fully integrates RF front-end, baseband analog, digital baseband, and MAC in one die for embedded applications. **[20.2]**
- A highly-integrated SoC for low-power ZigBee applications, which includes the radio and the PHY layers. **[20.6]**
- A fully-integrated SoC for GSM/GPRS on 0.13μm CMOS **[26.7]**
- A 1.9GHz single-chip CMOS PHS cellphone **[26.8]**
- RF tuners for all the worldwide mobile TV standards. **[33.1 to 6]**

## APPLICATIONS AND ECONOMIC IMPACT

- Complete integration of a UWB PHY in 0.13µm CMOS **[6.6]**
- Transceivers for low-power UWB systems **[6.1,6.2]**
- Wireless Gigabit Ethernet at mm-wave frequencies **[10.3]**
- Low-automotive radar for collision avoidance and autonomous cruise control. **[10.1]**
- Highly-integrated low-cost transceiver SoC has immediate significance, enabling high-volume low-cost WLANs **[20.2]**
- Highly integrated ZigBee SoCs enable low-cost sensor networks for home controls and industrial automation **[20.6]**
- Even-lower-cost, smaller, more-feature-packed cellular phones **[26.7,26.8]**
- In 2009, 150M mobile phones will be sold that are capable of receiving mobile digital broadcast TV. **[33.1 to 33.6]**
- The semiconductor industry has a new $1B opportunity to enable digital broadcast TV in mobile phones.

## SPECIAL-TOPIC SESSION

**CMOS RF Design in 90nm and Beyond [SE5]**

## TUTORIAL

**Millimeter-Wave ICs in Silicon [T8]**

## FORUM

**Advanced Wireless CMOS Transceivers [F1]**

# *UWB Transceivers*

## A 1.1V 3.1-to-9.5GHz MB-OFDM UWB Transceiver in 90nm CMOS [6.4]

*NEC*

## A Fully Integrated UWB PHY in 0.13µm CMOS [6.6]

*Realtek; University of California, Los Angeles*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- The state-of-the-art in UWB has evolved from a proof-of-concept technology to manufacturable and standards compliant SoCs.
- UWB solutions have two major application domains: On the one hand, we have the high- speed communication systems where the emphasis lies on the large-data throughput. On the other hand, UWB can also be used in low-power but lower-data-rate applications. Both domains require specific solutions and dedicated circuits.
- UWB, as its name implies, covers a very-wide frequency range (from 3.1GHz to 10.6GHz). The scarcity of available spectrum is overcome by transmitting at a very low power level and spreading information over a wide frequency range. Interference that can arise when sharing a crowded frequency band is avoided by very quickly hopping to different frequencies. Current transceiver technology for applications such as cellular phones and WLAN is aimed at relatively-narrow-band applications. Therefore, radically new wide-band receiver, transmitter, and frequency-synthesizer circuits are required.
- To become commercially viable, UWB systems have to be cost-effective. Cost-effectiveness can only be guaranteed with CMOS technologies. Until now, this was not feasible for the highest frequency bands. Furthermore, the complete system should be integrated on the one die.

## NOVEL CONTRIBUTIONS

- Low-power CMOS, pulse-based UWB transceivers **[6.1, 6.2]**
- Wide-band fully-integrated CMOS OFDM transceivers **[6.3, 6.4, 6.5]**
- A fully-integrated UWB PHY in 0.13µm CMOS **[6.6]**
- A frequency synthesizer covering the full 14 bands in CMOS **[6.7]**

# CURRENT AND PROJECTED SIGNIFICANCE

- UWB hardware will ultimately allow the wireless connection of new high-definition audio/video equipment. This will eliminate the rat's nest of wires and cables that is currently needed to connect our home-entertainment equipment. **[6.4, 6.6]**

- Low-power UWB systems will open completely new areas of application such as intelligent RFID, telemetry systems and sensor networks. **[6.4, 6.6]**

- It is impossible to imagine the full range of possibilities and conveniences that will be enabled by UWB. One more-obvious example is very-high-rate data transfer over short range to transfer the Gigabytes of information in modern-office and multimedia applications. **[6.4, 6.6]**

# *Millimeter Wave and Beyond*

## A 77GHz 4-Element Phased-Array Receiver with On-Chip Dipole Antennas [10.1]

*California Institute of Technology*

## A 60GHz Receiver and Transmitter Chipset for Broadband Communications in Silicon [10.3]

*IBM*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- While silicon ICs in the low giga-hertz range for wireless LAN and cellular applications have been extensively studied, and are currently in use, there remain several challenges in successful deployment of mm-wave circuits in silicon.
- Silicon transistors suffer from lower gain at higher frequencies, due to their higher parasitic capacitances, and hence are harder to use at mm-wave frequencies.
- Passive components suffer from higher losses at these frequencies due to substrate, radiation and ohmic losses that are exacerbated by the lower skin depth at mm-wave frequencies.
- Propagation losses are more severe at mm-wave frequencies.

## NOVEL CONTRIBUTIONS

- Phased-array system with on-chip antennas at 77GHz. **[10.1,10.2]**
- Demonstration of a complete receiver-transmitter pair in silicon at 60GHz. **[10.3,10.4]**

# CURRENT AND PROJECTED SIGNIFICANCE

- Low-cost beam-forming automotive radar at mm-wave frequencies will add a new dimension to the safety and reliability of next-generation cars. The automobile industry is desperately looking for low-cost solutions to deploy amenities such as self-parking, collision avoidance, preemptive brake boosting, low-visibility driving assist, and autonomous cruise control in cars. Successful demonstration of a phased-array system in silicon with on-chip antennas can make such luxuries available to the masses. **[10.1, 10.2]**

- Successful demonstration of silicon-based systems at mm-wave frequencies will offer low-cost wide-spread gigabit wireless LAN data transmission. More bandwidth is available at these frequencies with lower utilization than the lower GHz frequencies (e.g., 2.4GHz and 5GHz). This will open a plethora of new applications ranging from wireless high-definition TV to ubiquitous deployment of broadband communication systems. **[10.3,10.4]**

# *Breakthrough Wireless SoCs*

## An 802.11a/b/g SoC for Embedded WLAN Applications [20.2]

*Atheros Communications; Jaalaa; H-Stream Wireless; Stanford University*

## A Fully-Integrated 2.4GHz IEEE 802.15.4-Compliant Transceiver for ZigBee Applications [20.6]

*Atmel Germany*

### PRESENT STATE OF THE ART *(THE PROBLEM)*

- Existing transceivers consist of RF/analog IC(s) and baseband/MAC IC(s).
- Existing transceivers require numerous off-chip components.

### NOVEL CONTRIBUTIONS

- The first single-chip 802.11a/b/g SoC that fully integrates the RF front-end, baseband analog, digital baseband, and MAC, in one die for embedded applications. **[20.2]**
- A highly-integrated SoC for low-power ZigBee applications, which includes the radio and the PHY layers is presented. The only external components are a crystal and 3 capacitors. **[20.6]**

### CURRENT AND PROJECTED SIGNIFICANCE

- Highly-integrated low-cost transceiver SoC has immediate significance, enabling high-volume low-cost WLANs **[20.2]**
- Single-chip SoC enables significant reduction of form factor, penetrating mobile and embedded appliances. **[20.2]**
- Broadband connection of consumer electric appliances will result in a seamlessly connected world **[20.2, 20.6]**
- Highly-integrated ZigBee SoCs enable low-cost sensor networks for home control and industrial automation **[20.6]**

# *Cellular Building Blocks and SoCs*

## A Fully Integrated SoC for GSM/GPRS in 0.13μm CMOS [26.7]

*Infineon*

## A 1.9GHz Single-Chip CMOS PHS Cellphone [26.8]

*Atheros; Stanford University*

### PRESENT STATE OF THE ART *(THE PROBLEM)*

- Worldwide, GSM is the most popular cellular standard in use today, with over 75% of the total cellular market. Existing phones, based mainly on bipolar and SiGe technologies, consist of separate transmitter, receiver, and synthesizer chips as well as requiring many external components. More recently, a single-chip transceiver has been demonstrated in a low-cost CMOS technology. However, to implement a typical handset still requires two other ICs to provide the necessary analog and digital processing.

- The demand for low-cost services has spurred the resurgence of personal handy-phone system (PHS) cellular standards in many parts of Asia, such as China, which have more than 100 million subscribers. Existing solutions are based on expensive bipolar and BiCMOS technologies for the RF section, and CMOS for the baseband. The chipset solution incurs unacceptable cost in the current cost-sensitive Asia-Pacific market.

### NOVEL CONTRIBUTIONS

- GSM radio products on the market today are based on multi-chip solutions. However, several single-chip solutions have been announced recently. This chip is the first-published fully-integrated SoC for quad-band GSM/GPRS. It implements not only the RF, but also the analog and digital processing in a low-cost 0.13μm CMOS technology. It achieves the best sensitivity and level of integration on the market, today. **[26.7]**

- First true SoC radio for the PHS cellular standard is implemented in 0.18μm CMOS. The SoC integrates all the RF, analog, and digital processing on a single chip, and achieves the best sensitivity, power, and level of integration on the market, today. **[26.8]**

# CURRENT AND PROJECTED SIGNIFICANCE

- The demand for multimedia handsets with voice, data, and video streaming, will require high-levels of integration in deep-submicron CMOS to implement the increased digital signal-processing functionality for feature-rich handsets. The continued shrink in CMOS feature size will enable the integration of even-more-sophisticated digital processing with high-performance RF and analog circuits for future wireless standards. **[26.7, 26.8]**

# *Mobile TV*

## A 0.18µm CMOS Dual-Band Direct-Conversion DVB-H Receiver [33.1]

*Athena Semiconductors*

## *A 1.8dB-NF 112mW Single-Chip Diversity Tuner for 2.6GHz-DMB Applications* [33.6]

*Future Communications IC (FCI)*

### PRESENT STATE OF THE ART *(THE PROBLEM)*

- TV tuners have been available in a few mobile phones over the last few years; However, the TV feature never took off, because of power and performance penalties inherent in analog TV broadcasting and receivers. New digital-broadcasting technologies solve these technical problems: TV tuners designed for these new technologies are a key enabling component.

## NOVEL CONTRIBUTIONS

- For the first time ever, a single chip DVB-H tuner is presented. In fact, the first three papers all share this world's first distinction. All three feature dual-band support for both European DVB-H requirements in the UHF frequency spectrum, and US DVB-H requirements in the L-Band frequency spectrum. **[33.1, 33.2, 33.3]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Mobile digital-TV tuners for DVB-H, MediaFLO, DMB, and ISDB-T, represent critical enabling technology for including TV as a new feature in mobile phones. This session has examples of all four standards **[33.1, 33.2, 33.3, 33.4, 33.5, 33.6]**

# *SPECIAL-TOPIC SESSION*

# *CMOS RF Design in 90nm and beyond*

*Organizer:* ***David Su,*** *Atheros Communications, Santa Clara, CA*
*Chair:* ***Tony Montalvo,*** *Analog Devices, Raleigh, NC*

## OVERVIEW

- The scaling of CMOS analog and RF circuits traditionally lags that of digital design by one or two technology nodes. For instance, the majority of today's RF CMOS products are still in 0.13 - 0.18µm CMOS technology. However, the increasing integration level for systems-on-a-chip will lead RF designers, willingly or unwillingly, to follow their digital counterparts to 90nm and beyond. What challenges will they face?

## OBJECTIVE

- The objective of the session is to explore the modeling, design, and economic issues that will face designers in the 90nm technology node and beyond.

## CHALLENGE

- What are the features of these scaled technologies and their impact on RF design?
- Can we truly exploit scaling advantages for RF circuits? Does it make sense to simply port existing RF designs or is it desirable or even necessary to use a completely different architecture?
- Does the presence of the RF on the same chip as the DSP slow down the migration?
- In addition to the technical challenges of these scaled technologies, the associated economic issues are equally daunting. The staggering costs and long fabrication cycle times can create project management nightmares. How do we justify a multi-million dollar mask cost?

# STRUCTURE

- **Maarten Vertregt, Philips Research Labs: "Technology Property Exploration for Analog/RF Design in 90nm and Beyond"**

Device properties of deep sub-micron technologies relevant to RF circuit designers are explored. The impact of scaling on the various aspects of device precision is highlighted.

- **Sally Liu, TSMC: "RF Modeling Challenges at Deep Submicron CMOS"**

This talk discusses how nanometer effects (such as leakage and layout proximity) impact the device behaviors and matching properties in RF applications.

- **Behzad Razavi, UCLA: "RF Design Challenges in Deep Submicron CMOS"**

RF designers' perspective on deep submicron CMOS is presented, with emphasis on the challenges of low supply voltage, as manifested in mixers, VCOs, frequency dividers, variable-gain stages, and power amplifiers.

- **Bill Krenik, Texas Instruments: "Case Study on Single-Chip Integration for Wireless"**

This case study presents the motivation, methodology, business case, and technical results of the first GSM SoC. Several key issues associated with a single-chip integration are examined.

# RECAP

- In this Special-Topic Session, experts from academia and industry will describe the challenges that face RF designers as we embrace the inevitable scaling to 90nm and beyond.

# *Tutorial*

# MM-WAVE ICS IN SILICON

*Ali Hajimiri, California Institute of Technology, Pasadena, CA*

## OVERVIEW

- Review of mmWave design challenges and opportunities.
- Passive and active building blocks at mmWave frequencies.
- Phased arrays and radiation efficiency challenges.
- A case study of mmWave system design.

## SPEAKER BIOGRAPHY

**Ali Hajimiri** is currently an Associate Professor of Electrical Engineering and the director of Caltech's Microelectronics Laboratory at California Institute of Technology in Pasadena, CA, USA. He and his group do research in the general area of high-speed and RF integrated circuits with an emphasis on mmWave applications on silicon. He received his Ph.D. in Electrical Engineering from Stanford University, Palo Alto, CA, USA. Dr. Hajimiri holds several U.S. and European patents. He is an Associate Editor of the JSSC.

# *GIRAFE FORUM*

## *Advanced Wireless CMOS Transceivers*

### Objective

This all-day forum will cover the design and architecture of modern wireless transceivers in CMOS technology. These transceivers must be designed to meet the ever increasing demands of low cost, low power, and higher integration levels.

Attendance is limited, and pre-registration is required. This all-day forum encourages open exchange among the attendees.

### Audience

The targeted participants are circuit designers working on wireless transceivers who want to learn about the latest developments in system and circuit design for short range and cellular applications.

### Scope

There has been a paradigm shift in wireless transceiver integration in the last decade. Whereas two-chip solutions and BiCMOS technologies for the RF frontend are still standard for cellular phones, the first all CMOS transceivers are available on the market and even single-chip CMOS solutions are being sampled. The next challenges for transceiver design will be low-cost phones for emerging markets and multi-band, multi-standard terminals for established markets. Reducing form factor, increasing battery life and lowering production cost requirements can only be accomplished by further increasing levels of integration and by re-use and re-configurability of the hardware. Will a software-defined radio be superior over hardware-centric implementations for so many standards? Where is the break-even point?

### Program

The morning sessions address state-of-the art architectures and design of wireless transceivers. After a short introduction and overview by **Rudolf Koch**, the second speaker, **Chris Rudell**, will discuss wireless standards and their impact on architectural choices. The next two speakers will look into these architectures in more detail. **Tony Montalvo** will show latest advances in highly integrated transmitters, e.g. linear I/Q modulators, polar concepts etc. Then **Bill McFarland** will examine receiver architectures and take a close look at the latest trends, i.e. multiple antennas and dynamic channel bandwidth assignment. Finally **Aarno Pärssinen** will address the problems arising from the rapidly changing landscape of multi-standand transceivers and discuss design methodologies supporting quick adaptation to new standards and requirements.

The afternoon sessions will primarily be dedicated to cellular applications. The first two presentations, by **Andre Hanke** and **Bogdan Staszewski**, will look into their companies single-chip CMOS GSM transceivers. The first speaker discusses the integration of a proven stand-alone transceiver into a single-chip phone, while the second speaker promotes a mostly digital approach. Finally **Asad Abidi** will talk about one of the latest visions in this domain, the software (defined) radio.

The forum will conclude with a panel discussion, where the attendees have the opportunity to ask questions and to share their views.

# WIRELINE COMMUNICATIONS

- **Overview**
- **Featured Papers**
- **Panel**
- **Tutorial**
- **Forums**
- **Trends**

# ISSCC 2006 – WIRELINE

**Subcommittee Chair:** *Franz Dielacher, Infineon Technologies, Villach, Austria*

# *OVERVIEW*

## MOST-SIGNIFICANT RESULTS

- 10Gb/s 5-tap DFE / 4-Tap FFE Transceivers in 90nm CMOS **[4.1]**
- 12.5Gb/s Single-Chip Transceiver for UTP Cable in 0.13μm CMOS **[4.4]**
- 9.95-to-11.1 Gb/s XFP Transceiver in 0.13μm CMOS **[13.1]**
- 10 Gb/s Photonic Modulator and WDM Mux/Demux with Electronics in 0.13μm SOIC **[13.7]**
- 10Gb/s Burst-Mode Adaptive Gain-Select Limiting Amplifier in 0.13μm CMOS **[13.9]**
- 25Gb/s CDR in 90nm CMOS for High-Density Interconnects **[18.1]**
- Data Recovery and Retiming for 4.8Gb/s Fully-Buffered DIMM Serial Links **[18.6]**
- 104Gb/s $2^{11}$-1 and 110Gb/s $2^{9}$-1 PRBS Generator in InP HBT Technology **[28.10]**

## APPLICATIONS AND ECONOMIC IMPACT

- Many papers take advantage of further shrinking of CMOS linewidth (90nm), and achieve excellent performance improvements **[4.1, 4.4, 4.5, 18.1, 18.8, 28.2]**
- Enhancing performance for servers and data communication routers is required to meet the current and future data rate demands of the internet **[4.1, 4.6]**
- Many contributions in 10Gb/s optical interfaces indicate that a broad application of these technologies is happening **[13.1, 13.2, 13.3, 13.9]**
- The integration of photonic and transceiver functions in silicon technology will be a key driver for further development in the area of high-speed data communications. A photonic modulator and WDM Blocks are demonstrated at 10 Gb/s **[13.7]**
- Cost-power and space-efficient single-chip CMOS solution for ADSL / VDSL modems is supporting the steady decrease in the cost per installed line **[28.1]**

## PANEL

**What is Next to be Off-Shored, IC Design Jobs or IC Design Futures? [E3]**

## TUTORIAL

**Signal Integrity for High-Speed Circuit Designers [T9]**

## FORUM

**ATAC: High-Speed Interconnect [F5]**

# *GIGABIT TRANSCEIVERS*

## A 10Gb/s 5-Tap-DFE/4-Tap-FFE Transceiver in 90nm CMOS [4.1]

*IBM*

## A 12.5Gb/s Single-Chip Transceiver for UTP Cable in 0.13μm CMOS [4.4]

*Keyeye Communications*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- Need for reliable data transmission over legacy backplanes at data rates up to 6Gb/s
- Need for reduced power consumption of transceivers for copper cables in the Gb/s speed range
- Need for increased memory bandwidth beyond current multidrop bus architecture

## NOVEL CONTRIBUTIONS

- Fully developed 10Gb/s transceiver IC in 90nm CMOS technology **[4.1]**
- Low-power 12.5Gb/s UTP cable transceiver with analog signal processing **[4.4]**
- 9.6 Gb/s complete transceiver for next-generation memory interfaces in 90nm CMOS **[4.5]**

## CURRENT AND PROJECTED SIGNIFICANCE

- Increase in the bandwidth of servers and data-communication routers **[4.1, 4.2, 4.6, 4.7, 4.8]**
- Lower-cost for high-speed data-link solutions (e.g. for data centers) **[4.4]**
- Enhanced throughput while still using low-cost DRAM memory **[4.5]**

# *OPTICAL COMMUNICATION*

## A 9.95 to 11.1Gb/s XFP Transceiver in 0.13μm CMOS [13.1]

*Analog Devices; Cambridge Silicon Radio*

## A 10Gb/s Photonic Modulator and WDM MUX/DEMUX Integrated with Electronics in 0.13μm SOI CMOS [13.7]

*Luxtera*

## A 10Gb/s Burst-Mode Adaptive-Gain-Select Limiting Amplifier in 0.13μm CMOS [13.9]

*NTT*

### PRESENT STATE OF THE ART *(THE PROBLEM)*

- Many separate optical and electrical components assembled into a module
- Current PON has limited bandwidth
- Expensive components needed to build large networks

### NOVEL CONTRIBUTIONS

- Noise is removed from data signal **[13.1]**
- Monolithic optical modulator and driver in a standard CMOS process **[13.7]**
- Burst-receiver enables 8 times higher data rate (10Gb/s) **[13.9]**

### CURRENT AND PROJECTED SIGNIFICANCE

- Inexpensive components now available for large networks **[13.1]**
- Low-cost high-speed computer systems **[13.7]**
- PON is low-cost for very-high data rates (10Gb/s) to the home **[13.9]**

# *CLOCK AND DATA RECOVERY*

## A 25Gb/s CDR in 80nm CMOS for High-Density Interconnects [18.1]

*ETH Zurich; IBM Research*

## Data Recovery and Retiming for 4.8Gb/s Fully-Buffered DIMM Serial Links [18.6]

*Infineon*

### PRESENT STATE OF THE ART (*THE PROBLEM)*

- Increasing data rates in next generation high-speed backplane and chip-to-chip interconnect demand high-performance yet economical serial transceivers.
- Current DDR-2-server memory systems are approaching memory density and bandwidth limits.
- High-performance clock- and data-recovery circuits are too power-hungry or too costly to support wide-scale deployment of serial interconnect technology.

### NOVEL CONTRIBUTIONS

- 25 Gb/s CDR is compact and consumes 2.3X lower power per Gb/s than the currently-fastest CMOS design **[18.1]**
- CDR demonstrates an input sensitivity 3X better than FB-DIMM requirements and a fast locking technique requiring 1/3 the time allowed **[18.6]**

### CURRENT AND PROJECTED SIGNIFICANCE

- Low area enables dense integration of serial links **[18.1]**
- Facilitates the migration from DDR-2 to FB-DIMM server memory systems **[18.6]**

# *WIRELINE BUILDING BLOCKS*

## A 1ps-Resolution Jitter-Measurement Macro Using Interpolated-Jitter Oversampling [28.5]

*NEC*

## 104Gb/s $2^{11}$-1 and 110Gb/s $2^{9}$-1 PRBS Generator in InP HBT Technology [28.10]

*Chalmers University of Technology*

## PRESENT STATE OF THE ART *(THE PROBLEM)*

- 72Gb/s $2^{31}$-1 PRBS in a 150GHz SiGe technology, Paper 18.8 (at ISSCC 2006). High-speed communications require very high speed PRBS for characterization
- On-chip high-resolution jitter measurement is an enabling factor for in-situ characterization. Current approaches rely on histogram-based statistical characterization.

## NOVEL CONTRIBUTIONS

- New phase-oversampling techniques reduce jitter-measurement quantization noise, and allow continuous real-time measurements. **[28.5]**
- Increased PRBS performance through high-speed technology, optimized layout, and half-rate clocking **[28.10]**

## CURRENT AND PROJECTED SIGNIFICANCE

- On-chip jitter characterization allows significant cost reductions through shorter test times **[28.5]**
- Building block for future 100Gb/s communications **[28.10]**

# *Panel*

## *What is Next to be Off-Shored, IC Design Jobs or IC Design Future ?*

*Organizer:* ***Hui Pan****, Broadcom, Irvine, CA*
*Moderator:* ***John Stonick****, Synopsys, Hillsboro, OR*

## OBJECTIVE

- To explore the direction and impact of offshoring IC design.
- To learn how designers should react to offshoring.

## CHALLENGE

- Changing job function and salary expectations for designers in traditional high-tech regions.
- Achieving efficiency with fragmented design teams.
- Maintaining a high level of protection for IP.
- Keeping low-cost regions low-cost.

## CONTROVERSY

- Do engineers in traditional high-tech regions need to stop whining about outsourcing and focus, rather on “raising their game”, and earning their high salaries?
- Will offshoring design lead to a boom in the semiconductor industry similar to that caused by offshoring foundry services?
- Will offshoring necessitate itself by scaring kids in high-tech regions away from entering the engineering field? Will this put traditional high-tech regions’ innovation systems and military security at risk? Are the IC design leaders of today, the followers of tomorrow?
- Low cost = low quality?

# *Tutorial*

# Signal Integrity for High-Speed Circuit Designers

*Hong-June Park, POSTECH, Pohang, Korea*

## OVERVIEW

This tutorial will review the signal integrity issues starting from first principles. The target audience is high-speed circuit designers. The topics will include

- Transmission lines (reflections, terminations, crosstalk, loss of FR4 PCB)
- SPICE parameters of coupled transmission lines, vias, connectors and cables
- Signaling techniques (Multi-drop vs point-to-point, single-ended vs differential)
- Compensation techniques for lossy channels (TX and RX equalizations)
- Crosstalk reduction techniques
- I/O Buffer Information Spec (IBIS) model and power integrity issues

## SPEAKER BIOGRAPHY

**Hong-June Park** is a Professor at the POSTECH (Pohang University of Science and Technology) in Pohang, Korea. He is involved in the design of high-speed CMOS interface circuits and the signal-integrity issues associated with 2 to 5Gb/s DRAM interfaces. He received his PhD in Electrical Engineering from the University of California at Berkeley, in 1989.

# *ATAC FORUM*

# High-Speed Interconnect

## Objective

This all-day workshop is dedicated to the standards, architecture, techniques, design and application areas of high speed interconnect on chip- board and system level. Attendance is limited, and pre-registration is required. This all-day forum encourages open interchange in a closed form.

## Audience

The target participants are circuit and system designers working in the field of high speed interconnects on chip, board and system level, who want to get an overview of the state of the art and future trends in architecture, techniques and design concepts of this field.

## Scope

The field of high-speed interconnects, which has been the domain of high-speed computing, has meanwhile proliferated into personal computing, consumer products, and many other areas. Therefore, making the best technical and economic use of the channel by employing advanced signal processing techniques and integrating into ever shrinking process platforms has become of vital interest to a larger community. This forum discusses selected techniques in high speed interconnects on chip, board and system level from the perspective of architecture, design, performance and cost and gives an outlook to evolving new technologies as the use of silicon photonics on chip level.

## Program

The Forum will begin with a comprehensive overview of high speed interconnect techniques, standards and application areas given by **Yuriy Greshishchev,** (PMC Sierra).

The next two papers will discuss requirements and implementation choices for high speed interfaces in the chip to chip area. **Christian Sauer** and **Anthony Sanders**, (both from Infineon Technologies), will focus on specific challenges in the high performance processor arena and in memory systems for consumer applications, respectively.

A variety of techniques for channel equalization, partly based on traditional communications techniques, are available for this field. **Evelina Yeung** and **Bryan Casper**, (both from Intel) will analyze and compare such techniques as linear and non-linear equalization, decision feedback equalizers, transmit pre-emphasis, continuous time linear equalizers etc. in respect to their performance, power and cost.

The next sequence will deal with deal with 802.3ap 10Gb/s over backplanes presented by **Troy Beukema** (IBM) and over UTP cables **Scott Powell** (Broadcom). Both talks will provide an in-depth analysis of architecture, coding schemes and simulation of those channels and will compare the results with measured performance data.

As electrical interfaces including special signal processing techniques are approaching their limits, new techniques, as optical signaling and integration of photonic and electronic functions on a single silicon chip are gaining more and more interest. **Mario Paniccia** (Intel) will review this field, show recent results and give an outlook on future perspectives and opportunities of this technological field.

A panel discussion with all presenters will conclude the program.

# TRENDS IN WIRELINE COMMUNICATIONS

As CMOS feature size relentlessly diminishes to 90nm and beyond, the trend in wired communication takes a turn from a shear increase in data rate per channel (Figure 1) to more complexity and diversity in applications. This trend is witnessed by many papers that will be presented at the International Solid-State Circuits Conference (ISSCC) 2006 in San Francisco in February.

The latest solutions which target legacy backplanes and unshielded twisted pair (UTP) cables include the implementation of adaptive-equalization techniques at data rates as high as 10 to 12.5Gb/s. For distances less than 10 inches or so, lighter equalization techniques can be implemented to increase the data rates up to 20Gb/s as will be shown at the Conference.

Next generation memory systems require high-bandwidth and low-power interconnects. As will be described in one of the presentations at ISSCC, a data rate of 9.6Gb/s per channel is achieved by a 90nm CMOS chip using 100mW from a 1V supply.

Furthermore, the recent advances made in the integration of optics into CMOS chips open up new horizons for a broad range of optoelectronic applications, ones which have not been realizable until now. The resulting change could be very dramatic, since it would bring typically costly optical-link designs into the realm of silicon-based cost-effective solutions. Again, this is possible because CMOS feature sizes have reduced down to a fraction of commonly-used optical wavelengths, and transistors can reliably support data rates at 10Gb/s and above.

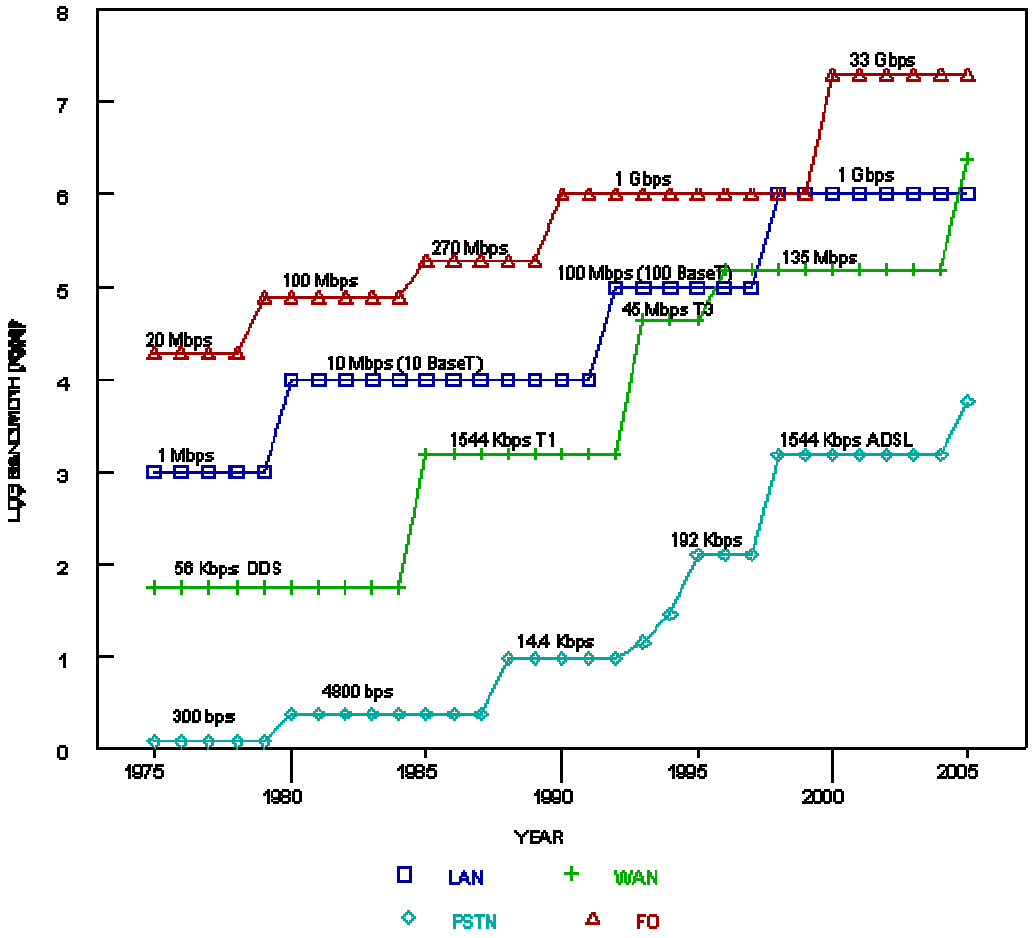



**Figure.1: Speed Evolution of Different Wireline Technologies**

# ISSCC 2006

# SESSION OVERVIEWS
# Press-Release Material

- **Conditions of Publication**
- **Session Overviews**

# CONDITIONS OF PUBLICATION

## PREAMBLE

- **The Session Overviews to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2006 in February in San Francisco.**
- **OBTAINING COPYRIGHT to ISSCC press material is EASY !**
  - You are welcome to use this material, copyright- and royalty-free, with the following understanding:
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## FOOTNOTE

- **From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 53nd appearance of ISSCC, on February 5th to 9th, in San Francisco.**

*This and other related topics will be discussed at length at ISSCC 2006, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 5-9, 2006, at the San Francisco Marriott Hotel.*

# Biomedical Systems

**Chair: Kensall D. Wise**, University of Michigan, MI
**Associate Chair: Euisik Yoon**, University of Minnesota, MN

This session highlights electronic interfaces with bio-molecules and bio-signals. In these applications, solid-state electronic devices must operate in contact with bio-molecules and structures such as the auditory and optic nerves in the liquid phase. Hybrid sensor interface packaging and low-power low-noise analog front-end design combined with wireless data transmission are addressed in these papers for reliable detection of bio-signals.

The first two papers report fully-electronic non-optical CMOS-based DNA array chips. The first chip, described in Paper 2.1, detects bio-molecules by measuring time-resolved charge on the functionalized surface in an 24×16 electrochemical sensor array realized on top of 0.5μm CMOS circuits. The second chip, described in Paper 2.2, exploits label-free capacitive molecular detection on 128 interdigitated sensing electrodes. The sensing elements are integrated on the readout circuitry using post-CMOS processes.

A high-density thin-film cochlear electrode array with integrated electronics has been developed to improve pitch perception in restoring hearing to the profoundly deaf in Paper 2.3. This array offers the site densities needed for a 128-site 16-channel human array with embedded position sensing capability to minimize insertion damage.

Papers 2.4 and 2.5 report wireless retinal implant prostheses. The first chip, described in Paper 2.4, realizes a digitally-programmable stimulation pad cell in $0.1mm^2$ for a 232 electrode stimulation array capable of operating at voltages up to ±15V. The second chip, described in Paper 2.5, achieves a low-power area-efficient implementation to deliver a data rate of 100kb/s using ASK modulation at 1.3mW.

The last two papers in the session address bio-signal acquisition systems. In Paper 2.6, a biopotential readout front-end for extracting EEG, ECG, and EMG signals with a total current dissipation of 20μA from 3V has been implemented with an input referred noise of 60nV/√Hz and CMRR of 120dB. In Paper 2.7, a low-voltage low-power biomedical signal acquisition IC consists of an LNA and an 11-bit ADC dissipating 2.3μW at 1V.

# Oversampling ADCs

**Chair:** *Raf Roovers, Philips Research, Eindhoven, The Netherlands*
**Associate Chair:** *Zhongyuan Chang, IDT-Newave Technology, Shanghai, China*

The increasing data rates in both wired and wireless communication systems constantly demands higher SNR and bandwidth requirements in the receiver and the ADC. Moreover, a clear trend to digitize receivers as much as possible by pushing the ADC towards the antenna, results in even more challenging ADC requirements. During recent years, oversampling ADCs have continuously increased their conversion bandwidth and dynamic range and are becoming a feasible ADC approach for many of the existing and new communication standards. Due to their power efficiency, oversampling ADCs are very suitable for efficient receiver implementation.

In paper 3.1 a power-efficient $\Delta\Sigma$ ADC with a SNDR of 74dB in a signal bandwidth of 20MHz is realized in a 0.13µm standard CMOS technology. The power consumption of only 20mW is achieved with a multi-bit single loop topology using a direct quantizer feedback technique. A PLL is integrated with the $\Delta\Sigma$ ADC to generate the required low jitter clock.

The next two papers demonstrate converters that directly handle IF receiver signals. Paper 3.2 presents a quadrature bandpass $\Delta\Sigma$ ADC that achieves 90dB dynamic range for a universal TV receiver with a bandwidth of 8.5MHz around 44MHz. Paper 3.3 describes a topology, where a mixer is integrated in front of the $\Delta\Sigma$ ADC to achieve 118dB dynamic range for AM and FM radio application in a bandwidth of 3kHz around 10.7MHz.

Paper 3.4 and 5 demonstrate the power efficiency of oversampling ADCs for wireline communication applications such as ADSL. Paper 3.4 introduces a combined analog and digital feedforward topology to achieve an 86dB DR in a 2.2MHz signal bandwidth for only 14mW. Paper 3.5 implements a time-interleaved topology resulting in a DR of 85dB over a 1.1MHz signal bandwidth with only 5.4mW. Both converters are realized in a 0.18µm CMOS technology.

Two papers in this session demonstrate that $\Delta\Sigma$ ADCs can operate from a sub 1V supply. Paper 3.6 describes a $\Delta\Sigma$ ADC operating at a supply voltage as low as 0.5V in a 0.18µm triple-well CMOS technology. Despite this low voltage, a peak SNDR of 74dB is obtained in a 25kHz bandwidth by using body-input circuits. Paper 3.7 presents a 0.9V $\Delta\Sigma$ modulator using a single-phase sampling technique and opamp sharing to achieve an SNDR of 80dB in 10kHz bandwidth with 0.2mW.

Finally, Paper 3.8 demonstrates a multi-bit switched-capacitor $\Delta\Sigma$ ADC in 0.18µm CMOS for digital TV receivers. A new double-sampling scheme is applied that enables the ADC to achieve an SNDR of 76.3dB over a 3.2MHz bandwidth.

# Gigabit Transceivers

**Chair:** *Yuriy Greshishchev, PMC-Sierra, Kanata, Canada*
**Associate Chair:** *Hirotaka Tamura, Fujitsu, Japan*

This session covers recent advances in CMOS gigabit transceivers and equalization techniques for a variety of electrical interconnects: short-distance chip-to-chip, backplane, shielded and unshielded twisted pair (UTP) cables. Each application brings a unique set of bandwidth limitation challenges and equalization requirements. The equalization varies from a simple TX pre-emphasis to an adaptive multi-tap FIR solution in combination with multi-tap DFE receivers. Multi-gigabit signaling over UTP cables requires a PAM-4 modulation while more traditional channels are NRZ-based. Once the data rate starts approaching 10 to 20Gb/s the equalization becomes important in traditional chip-to-chip interfaces.

In Paper 4.1, a 10Gb/s 5-tap-DFE/4-tap-FFE transceiver, addresses up to 20 inch back-plane applications while consuming only 300mW from a 1.2V supply. The main design enhancements are related to the reduction of the DFE response time and the improvement of the timing recovery precision.

The most common equalizers attempt to drive the ISI to zero at the center of the data eye. One question that often arises in transceiver design is whether providing additional equalization at the crossing points is beneficial. This problem is studied for both transmit and receive equalizers in Paper 4.2.

One of the major challenges transceivers must overcome is operation in the presence of crosstalk. One way to mitigate this problem is edge-rate control. An effective 1.5Gb/s to 6Gb/s multi-rate solution is provided in Paper 4.3. Each channel employs analog-type CDR with capacitance multiplication in the charge-pump filter.

The most challenging design problem is achieving multi-gigabit data transmission through the 4 pairs of UTP cable. In Paper 4.4, a 12.5Gb/s analog-based single-chip transceiver for 25m of CAT-6 cable with only a 3.8W power dissipation is discussed.

In Papers 4.5 and 4.6, chip-to-chip interfaces with equalization techniques traditionally used for longer interconnects are discussed. To reduce power dissipation in a 20Gb/s transceiver, Paper 4.6 proposes to forward the clock in a separate channel while data alignment is achieved with a local DLL.

In Paper 4.7, a spectrum-balancing technique for equalizer adaptation at 20Gb/s is explored. It does not require a slicer in the equalization path and reduces power down to 60mW.

Finally, an integrated transformer-based solution to overcome the power-supply limitation of traditional TX pre-emphasis, where low frequencies are de-emphasized, is suggested. Integrated transformers typically are not suitable for a direct data path due to their narrow-band characteristics. However, they are well positioned for implementing TX pre-emphasis within one 8Gb/s data bit interval.

# Processors

**Chair:** *Héctor Sánchez, Freescale Semiconductor, Austin, TX*
**Associate Chair:** *Georgios Konstadinidis, Sun Microsystems, Sunnyvale, CA*

Technology, as we have known it during the golden years of Moore's law, is facing significant challenges related to transistor and metallization scaling, as well as power and thermal control. High-performance transistors exhibit very high leakage and variability. Interconnect delay and power are hurdles for continued single-core processing performance improvements. Dynamic power dissipation and heat removal limit the industry's ability to continue the unprecedented performance gains of the last 20 years. Supply voltage scaling has come to a halt. Technology options used to optimize the power-performance trade-off are running out of steam. Variable voltage and frequency single-core processing can only partially alleviate the situation.

Given all these issues, is it time for a *fundamental* shift in processor computing implementation philosophy? Maybe so. A look at the processor papers this year reveals that all of the major companies involved in high-performance computing are rethinking the way to deliver improved power/performance products. No high-performance single-core processor papers are disclosed, a first for ISSCC. However, there are five multi-core processor innovations by five different companies. How is this new paradigm-shift to deliver Moore's law on performance/power scaling without transistor scaling? The answer lies in the combination of architectural changes, technology improvements, and extensive use of power/performance-efficient multi-core designs. On the architectural side, the increased parallelism allowed by multi-threading alleviates the requirement for high-frequency processing with a consequence of more power-efficient designs. This in turn, reduces the technology requirements for transistor scaling, resulting in less power-hungry transistors. Aggregate computing gains are accomplished by replication of simpler multi-threaded cores whose overall power/performance/cost is substantially superior to single core power/thermal-limited designs.

In Paper 5.1, the first generation of the power-efficient 64b-Niagara SPARC processor comprising 8 cores able to simultaneously handle 32 threads is described. It includes a high-bandwidth crossbar, a 3MB L2 cache and four DDR2 interfaces. The 378mm$^2$ die implemented in a 90nm technology consumes 63W at 1.2GHz. In Paper 5.2, a multi-core RISC processor with a number of security engines and network function accelerators results in a high-performance power-efficient system on a chip. It dissipates 25W at 600MHz and is fabricated in a 1.2V 0.13µm CMOS process with 9 layers of copper interconnects.

The first reported processor implementation in a 65nm technology is presented in Paper 5.3. This 435mm$^2$ dual-core 64b Xeon™ MP processor has 1.328B transistors, operates in excess of 3GHz and executes two threads per core. The chip contains a unified 1MB L2 cache per core and a shared 16-way set-associative unified L3 cache. A microprocessor featuring 2 Hammer cores, an on-chip DDR2 memory controller, and the Pacifica architectural support for virtualization is presented in Paper 5.4. It is processed in a 90nm triple-$V_t$ partially-depleted SOI technology with 9 layers of copper interconnects and operates at 2.6GHz at 1.35V with power dissipation of 95W. Paper 5.5 showcases a 146mm$^2$ dual-core Power™ architecture 64b processor created using a 90nm dual strained-silicon SOI technology with operation up to 3GHz. The dual-core processor has split clock domains and power planes, a 1MB L2 cache per core, and a shared processor interconnect bus.

The fastest integer execution unit reported to date, part of a 4$^{th}$-generation Intel Pentium® 4 processor, is presented in Paper 5.7. The 9GHz operation at 1.3V 70$^o$C is enabled by the use of 65nm technology and circuit design optimization for low latency and power.

The need for high aggregate bandwidth is satisfied by a 170GB/s crossbar for a multiprocessor server realized with only 10 LSIs as described in Paper 5.6. A 1.333Gb/s single-ended signal transmission with a driver using pre-emphasis and a receiver using a novel data-synchronous scheme is discussed. The total bandwidth of the address crossbar LSI is 1.23Tb/s with 704 drivers and 352 receivers.

# UWB

**Chair:** *Masaru Kokubo, Hitachi, San Francisco, CA*
**Associate Chair:** *Mark Ingels, IMEC, Leuven, Belgium*

The resurgence of the telecommunication industry is again reflected by the plethora of wireless data communication devices on offer from the conference's technical program. Of particular note is the continued rise of UWB wireless transceivers, devices that promise half a gigabit per second (or more) of data rate in and out of computers, printers, and home entertainment appliances at short distances. UWB transceivers turn out to present stiff technical challenges and a variety of solutions are presented in this session, that scale the obstacles from different angles.

RF transceivers based on the multi-band OFDM alliance (MBOA) standard continue to make a strong showing this year; with receiver, synthesizer, and transceivers realized in increasing levels of sophistication and CMOS technologies ranging from 90nm to 0.18µm in feature size. The sophistication and integration level are reflected in terms of compliance to WiMedia standard, inclusion of digital PHY on the same chip, or antenna diversity using phased-array techniques. This suggests that UWB is growing into a commercially viable system. A notable trend is that pulse-based or carrier-less UWB receiver and transceiver are making their presence felt this year at the Conference.

Pulse-based UWB systems are addressed in the first two papers of this session. In Paper 6.1, the emphasis is on low power consumption where a 20Mpulses/s receiver is presented that draws an overall current of 16mA from a 1.8V supply. In Paper 6.2, a carrier-less impulse-based transceiver chipset is introduced. It features a measured data-communication rate of up to 200Mb/s while the transmitter has can potentially achieves data rates up to 400Mb/s.

In Paper 6.3, antenna diversity and integrated RF selectivity are combined in a 0.18µm CMOS phased-array transceiver. The transmitter achieves an EVM of -27.2dB for 480Mb/s with an FCC mask-compliant output spectrum without any external bandpass filters.

A 90nm CMOS UWB transceiver, powered from a 1.1V supply, is described in Paper 6.4. The chip includes a 12-band synthesizer and covers the frequencies from 3.1 to 9.5GHz.

A full transceiver that fulfills WiMedia/MBOA requirements is presented in Paper 6.5. It has a noise figure in the range of 3.6 to 4.1dB for bands 1 to 3 and a transmitter $P_{1dB}$ of +5dBm at maximal gain.

The integration goes even further in Paper 6.6 where a fully integrated UWB PHY in 0.13µm CMOS is presented. The chip supports both fixed and frequency-hopped modes in the 3.1 to 4.8GHz bands and achieves measured data rates of up-to 480Mb/s.

The last two presentations focus on important building blocks for UWB applications. Paper 6.7 presents a frequency synthesizer that covers the full 14 bands and is realized in 0.18µm CMOS. Finally, a receiver front-end consisting of the LNA, mixer, and IF bandpass filter is presented in Paper 6.8. It is realized without any on-chip or off-chip inductors, and therefore, occupies an active area of 0.35mm$^2$.

# Non-Volatile Memory

**Chair:** *Giulio Casagrande, STMicroelectronics, Milano, Italy*
**Associate Chair:** *Yukihito Oowaki, Toshiba, Kawasaki, Japan*

The unprecedented demand for low-cost solid-state non-volatile mass storage to support the growing range of pocket communication/entertainment applications keeps accelerating advances in technology development and design to reduce cost and improve performance. This session reports significant steps forward in cost reduction, by introducing the first 56nm NAND Flash to achieve 8Gb below the 100mm$^2$ barrier and by showing the first 1Gb NROM packing 4 bits in a single cell. Performance highlights include 10MB/s programming throughput on the 8Gb 2b/cell and a 36MB/s read throughput on a 4Gb 2b/cell obtained by integrating the ECC hardware into the memory chip.

In the mean time, the quest for the Holy Grail memory technology is continuing, and the session shows strong advances on the whole range of emerging technologies, with a paper reporting on a 100MHz Chain FeRAM and two papers reporting on 16Mb MRAM advances in speed and manufacturability. Phase-change memory, the youngest among the emerging memory technologies, is reporting the largest density with a 256Mb chip in 0.1μm technology.

This session opens with a breakthrough paper reporting the first 1Gb NROM storing 4 bits per cell. A 3.5MB/s write throughput is achieved and a $V_t$ distribution-tracking reference scheme is adopted to improve retention and writing endurance.

In Paper 7.2, a 64Mb chain FeRAM with embedded ECC to improve manufacturability and featuring a 200MB/s burst read and write throughput is described.

There are two 16Mb MRAM papers: in Paper 7.3, a circuit technique and a screening methodology that improves manufacturing yield is reported; in Paper 7.4 an array wiring scheme is described that improves array efficiency, and reports a 100MHz synchronous operating frequency.

Phase-change memory is making another leap forward with a 256Mb 1.8V chip in a 0.1μm technology. The PRAM presented in Paper 7.5 shows a write throughput up to 3.3MB/s, comparable to NAND, together with a NOR-like random read access time of 62ns and 66MHz synchronous performance.

In Paper 7.6, for the first time, the integration of an area/performance optimized BCH error detection and correction engine in a 2b/cell 4M NAND Flash is shown. It relieves the microcontroller from the burden of performing ECC in software, allowing a record read throughput of 36MB/s after ECC. Up to 5 errors per flexible field are corrected at the cost of only 1.3mm$^2$ of die area.

The smallest 8Gb NAND ever presented, with a 99mm$^2$ die size, is reported in Paper 7.7. It is processed on a 56nm technology and achieves an effective bit size of 0.0075μm$^2$. A write throughput of 10MB/s, the fastest reported for a 2b/cell NAND, is achieved by introducing an 8kB page.

# DRAM and TCAM

**Chair:** *Terry Lee, Micron, Boise, ID*
**Associate Chair:** *Young-Hyun Jun, Samsung, HwaSung-City, Korea*

The global demand for bandwidth- and media-rich content has increased in unison with higher penetration rates of broadband Internet. The triple play of voice, data, and video content puts greater demands on CPU performance, graphics processing power, and networking router efficiency. In addition, the consumer appetite for mobile appliances dictates new requirements for power-efficient architectures. These application trends are driving more stringent requirements for memory subsystem performance, and future memory devices must deliver higher data rates, lower latencies, and greater power efficiency. The presentations in this session will report recent advances in DRAM and TCAM technologies that address these challenges.

In Paper 8.1, a deca-data rate DRAM is introduced that effectively hides the CRC overhead thereby enabling secure transmission of 8Gb/s/pin data over a differential I/O interface. This DRAM data rate is 25% higher than previously reported.

Graphic rendering times are very sensitive to memory bandwidth, and the GDDR3 SDRAM delivers this bandwidth with high data rate, single-ended wide I/O devices. The next two papers of the session, Papers 8.2 and 8.3, solve these technical challenges. A 2.0Gb/s/pin 512Mb device has been implemented in a 0.11μm process that improves output jitter by reducing the simultaneous switching outputs (SSO) to one-third through pad-driver averaging. Additional jitter improvements are gained by damping power-supply oscillations. A 2.5Gb/s/pin 256Mb GDDR3 device in a 0.10μm process is also described that implements an improved series pipelined CAS latency control and dual-loop DLL with low-power duty-cycle-correction circuitry.

The next paper of the session, Paper 8.4, provides insight into the next-generation of the main memory technology, DDR3. Dual-core CPUs have been developed to keep up with the higher processing demands, but they require greater memory subsystem bandwidth and lower latencies to realize system performance improvements. Details of a 512Mb DDR3 device that double the data rates over DDR2 and reduce address access time from 11.3ns to 8.4ns, are explored.

Mobile electronics require lower standby-current DRAMs to extend battery life. In Paper 8.5, a low-power embedded DRAM is discussed that includes an extended data-retention sleep mode to improve retention times by 8x and reduce the leakage current to 13% of normal operation. The performance improvement is achieved with a 65nm multi-threshold CMOS process and memory array ECC scrubbing.

High aggregate network traffic requires high-speed IP lookup tables that minimize power during search operations. In Paper 8.6, a new TCAM architecture leverages the use of don't-care bits in the table to implement an improved segmented search-line topology. A 1.1ns search-time with 0.35fJ/bit search energy is estimated. A second TCAM device, in Paper 8.7, uses a range-matching cell with compare operations and a search-line charge-recycling technique to improve storage efficiency by 2.5x compared to conventional TCAMs while reducing the search-line power to 40% of a precharged TCAM.

# Display Drivers

**Chair:** *Oh-Kyong Kwon, Hanyang University, Seoul, Korea*
**Associate Chair:** *Tiemen Zhoa, Relfectivity, Sunnyvale, CA*

At a growth rate of greater than 20% per year, displays are the fastest growing segment of the electronics industry. Ranging from cell phones to 60-inch televisions, consumers are demanding higher resolution, higher color depth, and lower cost. Innovations in the drive electronics for both traditional TFT-LCD displays as well as emerging technologies such as active matrix organic LEDs (AMOLEDs) address this demand.

The first paper, 9.1, describes a power-speed optimized topology for a quarter VGA TFT-LCD display. It produces 12 channels with 256 gray levels for each.

In the second paper, 9.2, an AMOLED display driver is described; it drives the display matrix with current. This eliminates the lifetime and temperature issues associated with the diode I/V relationship when using a voltage drive. The design obtains accuracies of better than 2% (at 10nA) using a common current-mode DAC and a linear array of current copiers.

The third paper, 9.3, uses thin film transistor CMOS devices to create a 6-bit TFT-LCD column driver on a glass substrate. Significant cost savings are achieved by eliminating the printed circuit board and tape automated bonding required for crystalline silicon drivers. The design used copper plating to obtain low-resistance interconnections for critical signals.

# Millimeter Wave and Beyond

**Chair:** *Ali Hajimiri, California Institute of Technology, Pasadena, CA*
**Associate Chair:** *Hiroyuki Sakai, Matsushita Electric Industrial, Osaka, Japan*

The frequency bands at millimeter-wave (mm-wave) frequencies such as 24GHz, 60GHz, and 77GHz offer new opportunities and challenges for gigabit wireless local area networks and automotive radar. Gigabit data rates are becoming an essential necessity due to the emergence of broadband high-quality video and audio applications, as well as high-speed home and enterprise networking. The migration to higher mm-wave frequencies facilitates the integration of more functionality in silicon and allows for spatially reconfigurable communication systems that can reuse bandwidth in a dynamic and more efficient fashion. Millimeter-wave silicon ICs can also enable low cost beam-forming automotive radar at 77GHz that will substantially improve the safety and reliability of next generation cars, enabling features such as self-parking, collision avoidance, preemptive brake boosting, low-visibility driving aid, and autonomous cruise control in both low- and high-end cars. Successful demonstration of a phased-array system in silicon with on-chip antennas can make such luxuries a reality. The propagation challenges at higher frequencies are overcome by using phased-array multiple-antenna systems on both the receiver and the transmitter. The integration of the antenna with the rest of the receiver eliminates the last high-frequency electrical connection to the chip, making it the ultimate fully integrated communication system in silicon. This session explores the most recent developments in mm-wave applications of silicon and offers a broad set of solutions for broadband communications and automotive radar.

Paper 10.1 demonstrates a fully integrated 4-element phased-array receiver with on-chip antennas in silicon, including the entire down-conversion chain, power combining and phase generation functions with no external mm-wave connection. Each of the four elements achieves a noise figure of 8dB over the system bandwidth of 3GHz.

A 77GHz transmitter phased array with continuous phase shifting, where each element has a gain of 34dB and an output power of +10dBm, demonstrating successful beam-steering at 77GHz, is shown in Paper 10.2.

Paper 10.3 describes an integrated receiver-transmitter pair operating at 60GHz in silicon. The receiver has a NF of 6dB and the transmitter has 10 to 12dBm 1dB compression point and 10% PAE in the output stage.

A 60GHz transmitter with integrated tapered-slot antenna is shown in Paper 10.4. It integrates a VCO, a sub-harmonic mixer, and a PA on a chip and achieves 20dB of conversion gain while consuming 281mW of dc power.

Paper 10.5 describes a digitally controlled LC oscillator that is integrated in a digital 65nm CMOS process. The VCO achieves 10% tuning range with a phase noise of -102dBc/Hz at 1MHz offset while drawing 3.3mA from a 1.1V supply.

# RF Building Blocks and PLLs

**Chair:** Bram Nauta, University of Twente, The Netherlands
**Associate Chair:** Marc Tiebout, Infineon Technologies, Germany

RFIC design is a broad, fascinating, and complex topic. Already for many years researchers and designers from academia and industry have invented and proposed new or optimized circuits in silicon technologies. These RF circuits find their way to customers in existing and upcoming applications such as TV, cellular, WLAN, UWB, and radar applications. The ten presentations in this session document recent advances in RF solid-state circuits. The session covers the above mentioned applications in frequencies ranging from 90MHz up to 85GHz through LNA and PA blocks as well as through clock generation issues ranging from small VCO circuits to complete PLLs.

The session starts with an agile auto-tuning synthesizer architecture. The synthesizer achieves a low-power operation of 18mW and wide-tuning range from 90 to 770MHz. It includes a divide-by-3.5 circuit.

In Paper 11.2, differential CMOS LC-tank VCOs with single and double switch pairs are compared. A 0.3µm CMOS VCO is described that operates from 2.15 to 2.35GHz and achieves a record performance with a phase noise of -143.9dBc/Hz @3MHz drawing 4mA from a 2.5V supply.

Two quadrature VCOs are presented in papers 11.3 and 11.4. Paper 11.3 presents a phase-noise reduction technique in quadrature VCOs. The technique shapes the transistor's injected thermal noise and provides a phase-to-amplitude noise-conversion mechanism. The experimental designs are centered at 5.1 and 5.3GHz with phase noise of -132.6dBc/Hz and -134.4dBc/Hz at 1MHz offset, respectively. The 5mW low-power quadrature VCO of Paper 11.4 features a high frequency of 17GHz, low-voltage operation using a 1V supply, and a low phase noise of -110dBc/Hz at 1MHz offset.

The session continues with two CMOS broadband LNA designs. Paper 11.5 presents a 5GHz broadband LNA in a 90nm CMOS technology with an area of 0.025mm² that achieves 25dB gain, 2dB NF, -14dBm IIP3, and -13dB $S_{11}$. In Paper 11.6, a CMOS LNA for UWB based on a method that uses Miller effect for input matching is presented. The technique requires only one extra inductor at the gate besides the source-degeneration inductor to achieve wideband matching and improved noise figure.

A fast-settling PLL frequency synthesizer with frequency presetting is presented in Paper 11.7. The 0.4mm² chip is implemented in a 0.35µm CMOS process. The measured results demonstrate that the settling time is less than 10µs.

Next, two power amplifier designs are proposed. A 2-D propagation medium compatible with IC processes is introduced in Paper 11.8 to design a broadband power combiner, called "funnel". A 4-to-1 combiner based on this concept demonstrates a wideband power amplifier at 85GHz in a 0.13µm SiGe BiCMOS process. In Paper 11.9, a single-chip 0.18µm CMOS linear PA for WLAN applications is proposed. All components, including the input balun and output transformer are integrated and no off-chip components are required.

In the last paper of this session, Paper 11.10, a CMOS low-power digitally controlled oscillator for UMTS is presented. Drawing 3.2mA from a 2.5V supply, it reaches a phase-noise target of -118dBc/Hz at 1MHz offset. A tuning range from 3.45 to 4.45GHz with a maximum frequency step of 200kHz is achieved by using a combination of binary-weighted and thermometer-coded switchable capacitors..

# Nyquist ADCs

**Chair:** *Venu Gopinathan, Texas Instruments, Bangalore, India*
**Associate Chair:** *Aaron Buchwald, Mobius Semiconductor, Irvine, CA*

Analog-to-digital converters continue to play a vital role in virtually all applications ranging from sensor arrays to broadband communication. Power dissipation has always been important, but today is even more so with the emphasis on extended battery life for hand-held multi-media devices. Achieving both low-power dissipation and high resolution simultaneously requires excellent engineering, new circuit techniques, and architectural innovations.

The eight presentations in this session address challenges in ADC design in achieving resolutions of 10 to 14 bits over sample rates from DC to 100MS/s.

The first paper in this session discusses a 10-bit ADC with an energy per conversion-step of 0.5pJ in 90nm CMOS. In addition, this converter is designed to trade power for sampling rate from 25 to 100MS/s to obtain "speed-on-demand" with no sacrifice in energy efficiency.

The session continues with the next two papers highlighting various power-saving techniques. A method of opamp sharing by reusing opamp currents in different pipeline stages is presented in Paper 12.2. Next, simultaneous offset cancellation and positive-feedback gain boosting is discussed in Paper 12.3 that allows the use of smaller devices in comparators.

Paper 12.4 discusses a new method for switched-capacitor circuits using comparators instead of feedback-forcing opamps. A 10-bit 2.5mW 8MS/s ADC is designed in 0.18µm to demonstrate the concept.

The session takes a detour from the 100MS/s range to consider the challenge of achieving micro-watt power dissipation at 100kS/s for sensor applications. In Paper 12.5 an efficient successive-approximation 12-bit ADC is presented that achieves an effective number of bits of 10.5 while consuming only 25µW from a 1V supply.

The final three papers of this session highlight different aspects of achieving good linearity without excess power dissipation. Paper 12.6 discusses a 100MS/s multi-bit pipelined ADC in 0.13µm CMOS that uses calibration to obtain greater than 70dB THD and 66dB SNR while dissipating 224mW. Paper 12.6 is an implementation of a pipeline converter in 0.13µm CMOS that achieves an effective number of bits of 9.3 while consuming only 15mW and occupying an area of 0.2mm$^2$. Finally, a sorting algorithm to re-order capacitors in judicious groupings to minimize random mismatch is applied to the design of a 13-bit pipelined converter in 0.18µm CMOS.

# Optical Communications

**Chair:** *Larry DeVito, Analog Devices, Wilmington, MA*
**Associate Chair:** *Sung Min Park, Ewha Womans University, Seoul, Korea*

Communication using light signals over optical fiber holds great promise to lower costs for data transport over both short and long distances. The huge bandwidth and favorable physical characteristics of optical fiber beg to be exploited: in telecom networks, transmitting high-data-rate signals over long distances becomes practical, and in computer systems, high-capacity interconnect, free-from electromagnetic interference and awkward bulky copper cables, is enabled by parallel optics. However, practical details limit cost-effective commercial solutions. In this session, several advances in the practical art of sending and receiving optical signals are presented. Inevitably, such advances will lead to exciting new cost-effective telecom services and higher-performance computer systems.

The 10Gb/s XFP transceiver in Paper 13.1 covers many protocol data rates. The receiver removes jitter from signals and thus eases the task of other components in the system. Also, the transmitter removes jitter from the host system and creates a low-noise output. This dramatic jitter filtering is enabled by a dual-loop DLL/PLL architecture: this is the first use of this architecture at 10Gb/s.

The multi-chip solution of AFE and digital equalizer ICs in Paper 13.2 is the first 10Gb/s MLSE receiver. A Viterbi detector is used to combat dispersion and nonlinearity in OC-192 metro and long-haul links, resulting in 2200ps/nm of dispersion compensation, approximately doubling the link distance.

To guarantee system reliability, redundant clocks are commonly required for communication networks. In the past, switching two redundant clocks has required bulky and costly components. The circuit presented in Paper 13.3 is a simple cost-effective solution which avoids short-term phase-transients and thus maintains timing integrity in the network.

In Paper 13.4, a negative impedance is used to increase gain to compensate the deleterious effects of both photodiode and ESD parasitic capacitances in a 1.25Gb/s fiber-optical transimpedance amplifier.

A fully monolithically integrated optical receiver including a photodiode with amplifier and additional signal processing which extends the bandwidth and improves the sensitivity is described in Paper 13.5. The enhanced performance, obtained from the photodiode structure, allows high reverse voltage and also shields carriers generated in the substrate from being collected in the signal path.

The first 10Gb/s burst-mode laser driver with both average power and the extinction ratio control is presented in Paper 13.6. Previous laser drivers only applied single-loop automatic power control. However, signal fidelity degrades because the extinction ratio was not adequate due to temperature and aging effects in the laser. This chip is an important step towards building low-cost high-speed burst-mode packet-based networks.

The chip, presented in Paper 13.7 promises to dramatically reduce the cost of optical interconnects by monolithically integrating both photonic and electronic components on a standard SOI CMOS process. An optical modulator is described that matches the velocity of electric and optical waves in a waveguide. Also a WDM multiplexor/demultiplexor uses a similar structure to calibrate optical-path lengths to improve channel separation in an arrayed waveguide grating.

In Paper 13.8, a 10.3Gb/s VCSEL driver is integrated with a complete Ethernet transceiver in a standard 0.13µm CMOS process. A low supply voltage of 1.2V is enabled by using two signal paths which are combined in transmission lines to drive a VSCEL differentially. The resulting optical eye exceeds the 10Gb/s Ethernet mask by 35%.

The 10Gb/s burst-mode limiting amplifier, presented in Paper 13.9, extends the dynamic range by a factor of five beyond results previously obtained. Valid data is obtained in less than 1ns. The optimum tap in a cascade of gain stages is selected by monitoring the signal amplitude throughout the cascade.

# Baseband and Channel Processing

**Chair:** *K. Lawrence Loh, MediaTek Inc., Hsin-Chu City, Taiwan*
**Associate Chair:** *Steffen Paul, Infineon Technologies, Munich, Germany*

Silicon implementations based on DSP technologies continue to advance in both wireless communications and mass storage applications. This session provides a snapshot of advances in baseband and channel signal processing to provide economic and power-saving solutions in cellular feature phones, UWB and digital TV applications. Important digital communication building blocks, including an all-digital spread-spectrum clock generator, and direct digital frequency synthesizer/mixer technologies, are presented to mark the increased performance as well as power efficiency. In the mass storage area, the session reports a variety of highly-integrated SoC solutions to target read/write operations of multiple formats of existing and emerging optical disks.

In Paper 14.1 a mixed-signal 90nm GSM/EDGE baseband processor featuring multimedia enhancements and low power features is presented. Supply gating and dynamic voltage/frequency scaling are used to minimize both the leakage and dynamic power consumption in a given application scenario. A power metric of 0.47mW/MHz is reported.

The authors of Paper 14.2 report on an all-digital spread spectrum clock generator for reducing electromagnetic interference by over 13dB. Their solution is capable of spreading the clock power spectrum both upwards and downwards using a very power/area efficient digital-delay-line-based approach that consumes 7.1mW of power and 0.06mm$^2$ in 0.15µm CMOS.

Two very different approaches for implementing direct digital frequency synthesizers (DDFS) are presented in Papers 14.3 and 14.4. The first paper describes a new multipartite table-based approach that achieves an SFDR of over 90dBc at a clock frequency of 630MHz, a power dissipation of 76mW, and a frequency resolution of 0.15Hz. The second paper integrates a mixer with a DDFS delivering an SFDR over 90dBc, generating 13-bit quadrature outputs. This integrated solution consumes 150mW at 380MHz.

A contribution to DSSS UWB digital transceivers is presented in Paper 14.5. The proposed solution targets ad-hoc wireless mesh networks, providing fast acquisiton (< 8µs), and a ±7.5cm ranging accuracy. Power saving features allow a 4 to 25x reduction in power consumption.

A COFDM receiver supporting DVB-T/H is described in Paper 14.6. It features a 2D linear equalizer, allowing it to overcome a 70Hz Doppler frequency shift. Data rates up to 31.67Mb/s are supported at a power consumption of 250mW.

In Paper 14.7, a 0.13µm read/write channel SoC for all formats of both conventional (CD/DVD) and emerging (HD-DVD/BD) optical disks is integrated with dual processors to assist servo controls and I/O operations. Data rates up to 550Mb/s on the read PRML channel are supported, and a power consumption of 2.7W is reported for a 16x DVD playback.

A highly-integrated mixed-signal SoC for all existing commercial optical storage formats is presented in Paper 14.8. An aggressive power management scheme enables the inclusion of all major functional blocks in a single chip for full-format optical drives including read/write channels, servo controls, 4-LVDS channel write strategies generator, and a 1.5Gb/s serial-ATA PHY.

# Organic Devices and Circuits

**Chair:** *Bill Bidermann, BK Associates, Los Gatos, CA*
**Associate Chair:** *Koji Kotani, Tohoku University, Sendai, Japan*

Rapid advances in organic devices make possible a broad spectrum of circuits and systems that address needs from RFID devices to electronic paper that outputs Braille text for the blind. Though organic electronics will not displace silicon solutions, they promise to become ubiquitous in everyday life. Low cost sensors, flexible displays, electronic labels, smart tickets, anti-counterfeiting technologies and other "electronic paper" applications; all these and many other applications rely on the development of organic devices and circuits characterized in this session. The eight papers in this session portend the huge impact of these devices.

The session begins with two developments in RFID tag technology. Both transponders operate at 13.56MHz. Intended for use as a commercial item-level tag, the proof of concept device presented in Paper 15.1 scavenges its power from the incoming RF signal using organic diodes. The devices operate over distances up to 4.75cm using low cost printable polymers allowing volume production of tags for less than 5 cents per tag. The second paper, 15.2, describes RFID tags manufactured using a pentacene on plastic technology. The tag circuitry also operates at the de facto standard 13.56 MHz frequency. A second tag, using the same technology, incorporates full 64-bit tags and comprises almost 2,000 active devices.

Beyond RFID tags, Paper 15.3 demonstrates the diversity of applications to which organic transistors apply. An electronic "nose" sniffs vapors inside the packages of food and pharmaceutical products, in this case bottles of wine. These devices detect levels of acetic acid associated with wine spoilage at levels of 10 parts per million utilizing a bridge structure. Inkjet printing technology allows the low-cost production of devices required for this application.

Displays in flat panel TV's, laptop computers and many other products have become commonplace. A modifiable Braille display for the blind appears in Paper 15.4. The development of a 5-transistor SRAM cell allows the actuators in the Braille display to improve its update time from 34 seconds to 2 seconds. This exciting technical development allows one to envision a world where the blind can read electronic newspapers and novels in as timely a way as their sighted counterparts, possibly even the Advance Program for ISSCC!

Future products based on organic devices rely on the development of analog building blocks: cascode amplifiers, differential amplifiers, and differential-to-single-ended converters. Despite their performance lag relative to silicon devices, Paper 15.5 develops an empirical model for organic devices used to predict the statistical performance of these building blocks, including amplifiers with 10dB of gain and unity gain frequencies of 1.4kHz. Future development of switched-capacitor circuits will increase the proven topologies available to organic circuit designers.

From basic organic analog circuits, the session moves, with Paper 15.6, to a complete 71,000 device cryptographic security system on a flexible substrate. This device makes use of TFT devices to realize a full CPU, including a 2kB ROM and a 64B SRAM. This plastic cryptographic system is intended for personal identity verification applications and dissipates less than 5mW from an internally generated 1.8V supply.

The session wraps up with two short papers. Paper 15.7, describes full complementary organic circuits (P and N-channel) that operate devices at voltages as low as 2 Volts. The inverter shows a gain of 14 and a noise margin of 0.65V. The final paper in the session, Paper 15.8, describes fabrication of more conventional low temperature polysilicon TFT CMOS circuits but deposits them directly on plastic substrates requiring maximum process temperatures less than 300°C. These 2μm channel-length devices produce ring oscillators operating at 100MHz.

# MEMS and Sensors

**Chair:** Farrokh Ayazi, Georgia Institute of Technology, Atlanta, GA
**Associate Chair:** Hirofumi Sumi, Sony, Tokyo, Japan

This session presents recent advances in microsystems technology for applications in sensing and wireless communication. Advanced micromachined devices combine with CMOS electronics to achieve state-of-the-art performance. Circuit techniques and material properties are exploited to potentially eliminate the need for expensive calibration in sensors. The nine presentations in this session illustrate precision sensing of acceleration, temperature, electrostatic field, magnetic field, and images at low-power and small form factor. In addition, high-performance CMOS interfaces for gas sensing and MEMS-based transmitters are presented. These technologies enable direct and seamless interfacing of digital computers to the real world.

The first paper of the session (16.1) presents significant advances in micro-g acceleration sensing with a large dynamic range. The low noise is achieved using an SOI substrate with thick silicon seismic mass, and high sensitivity is achieved by reducing gaps between sense electrodes through post-release LPCVD polysilicon deposition onto the electrodes, thus realizing an acceleration resolution of 4μg/√Hz. In Paper 16.2, the first programmable MEMS FSK transmitter is realized using a frequency-tunable MEMS resonator in the feedback loop of fractional-N frequency synthesizer. The variable frequency oscillator (2 to 437MHz) outperforms the quartz crystal based oscillator for mobile wireless platform application. The MEMS chip presented in Paper 16.3 demonstrates electrostatic field sensing. This technique is rarely discussed in the context of MEMS and can be applied to xerography, non-contact voltage sensing and precision electrometers. The charge induced on a mico-machined resonant polysilicon shutter, as it cuts through the electrostatic field, is amplified and synchronously demodulated to quantify the electrostatic field. A simple CMOS circuit architecture based on a relaxation oscillator is presented in Paper 16.4 for temperature control of a gas sensor. A ±2.5°C accuracy over the 100 to 400°C range is realized and integrated with the readout circuit to give 0.5% linearity and 114dB dynamic range.

Paper 16.5 presents a new technique of temperature sensing exploiting the temperature dependence of thermal diffusivity in bulk silicon. The sensor accuracy is comparable to the state-of-the-art (±0.5°C), but it only requires low-cost batch calibration rather than expensive trimming of individual devices. An integrated magnetic sensor incorporating digital compensation for package-induced mechanical stress is presented in Paper 16.6.

A record 200dB dynamic range is achieved in the image sensor presented in Paper 16.7. The image sensor presented in 16.8 is back illuminated and achieves 34% better sensitivity than a conventional device. A laser radar imager using two layers of fully depleted SOI circuits integrated with a single photon detector is presented in Paper 16.9.

# RFID and RF Directions

**Chair:** *Vadim Gutnik, Impinj, Inc., Newport Beach, CA*
**Associate Chair:** *Hiroyuki Mizuno, Hitachi, Tokyo, Japan*

Radio frequency identification technology is rapidly becoming commercially significant, with volumes in the billions of units per year predicted for the next few years. In this extremely price-sensitive market, chip size is critical, but at the same time, ever more powerful standards and stringent requirements for reliability require MHz data rates. The papers in this session push the frontiers of RFID size and performance. In the second half of the session, mechanical resonators, integrated FBARs and MEMS, promise to integrate high-quality RF filters and oscillators directly with transistors. Novel physical structures enable extremely high-performance oscillators and LNAs.

A 0.15×0.15mm$^2$ 7.5μm-thick RFID chip in a 0.18μm SOI CMOS technology containing a 128b ROM is presented in Paper 17.1. An SOI buried oxide layer structure acts as an etch stop to enable aggressive thinning. Contact to the antenna is made from both top and bottom of the die.

In Paper 17.2, a passive UHF RFID tag, fabricated in 0.35μm FeRAM CMOS technology, with a 36.6% rectifier efficiency is described. This high efficiency is made possible by a CMOS full-wave rectifier with a ferroelectric capacitor. The chip boasts a read and write range of 4.3m and can support read rates of 129 tags/s.

A 3.4Mb/s 13.56MHz RFID front-end is presented in Paper 17.3. The front end uses multi-level signaling and is fabricated in a 6M 0.18μm 1.8V digital CMOS process technology.

The session continues with Paper 17.4, where a novel artificial dielectric is presented which takes the place of an LC tank in a high-quality oscillator. The 60GHz VCO in 90nm CMOS occupies only 0.015mm$^2$, consumes 1.9mW, and has a measured phase noise of -100dBc/Hz at 1MHz offset.

In Paper 17.5, a 5.4GHz 0.35μm BiCMOS SiGe FBAR oscillator is presented. The resonator is integrated directly above a silicon IC, and achieves a phase noise of -117.7 dBc/Hz at 100kHz offset while drawing 1.7mA from 2.7V.

In Paper 17.6, a single-ended input to balanced output 425MHz electromechanical filter is introduced. The technology provides 1MHz channel-select filtering, while eliminating the need for RF switches and baluns in front-end transceivers, and brings the filter performance to 8dB insertion loss with -50dB stop-band rejection and -48dB common-mode suppression.

A low-power 2.4GHz heterodyne receiver front-end in 0.18μm CMOS using BAW solidly-mounted resonators is presented in Paper 17.7. The resonators, with Qs of up to 580, provide both impedance matching and selectivity. An image rejection of up to 50dB, a noise figure of 11dB and $IIP_3$ of -16.1dBm with a power dissipation of 1.8mW are demonstrated.

In Paper 17.8, a 0.46mm$^2$ V-band (50 to 75GHz) CMOS LNA is described. The three-stage cascade CMOS LNA is implemented in 0.13μm CMOS technology, exhibits better than 20dB measured gain from 51 to 57.5 GHz, minimum noise-figure of 7.1dB at 56.8GHz, $P_{1dB}$ of -22dB, input $IP_3$ of -12dBm, under a 2.4V/33mA bias condition.

# Clock and Data Recovery

**Chair:** *Roger Minear, Wyomissing, PA*
**Associate Chair:** *Robert Payne, Texas Instruments, Dallas, TX*

Applications for multi-Gb/s serial-link technology are expanding beyond optical and backplane communications to memory and chip-to-chip interconnect. As a result, clock- and data-recovery (CDR) circuits are needed that combine high-speed performance with low cost, low power, and smaller area. In addition, applications in passive optical networking (PON) and low-latency memory interfaces require that CDR lock-time improves beyond what is possible using widespread dual-loop CDR architectures.

The 8 papers in this session represent a cross-section of recent advances in CDR techniques, ranging from compact 25Gb/s receivers for high-density interconnects to low-power delay-locked loops (DLLs) for 300MHz DDR timing generation. Applications involving high-speed serial memory interfaces are also included.

In Paper 18.1, a compact 25Gb/s phase interpolator-based CDR in 90nm CMOS occupying only 0.09mm$^2$ is described. The low power (< 4mW/Gb/s), high speed, and compact area lead towards higher levels of integration and higher-density interconnections.

Optical networking applications place strict demands on jitter tolerance and recovered-clock quality. In Paper 18.2, the application of a mixed-signal filter to a CDR is covered. It can be used across a wide range of SONET data rates (OC-3 to OC-48).

As memory bandwidths increase and server applications demand larger capacities, CDR circuits become necessary in memory interfaces. Two papers in this session address techniques to enhance memory system performance. A DLL used for phase alignment and duty-cycle correction for DDR interfaces is described in Paper 18.3. An advanced memory buffer (AMB) with a fast-locking CDR for next-generation fully buffered DIMM standards is presented in Paper 18.6.

The authors of Paper 18.4 explore different methods of phase estimation that are enabled by changes to the phase-control logic of a dual-loop CDR. Three such designs are described which offer improvements in lock time, frequency tracking, and jitter tolerance.

In Paper 18.5, a hybrid of a traditional phase-tracking CDR combined with blind-oversampling is shown to improve low-frequency jitter tolerance by 32x over phase-tracking alone.

In Paper 18.7, a 0.13µm CMOS 10Gb/s receiver that uses a 2.5GHz clock and a quarter-rate linear phase detector to meet OC-192 jitter-tolerance requirements, is detailed.

The 20Gb/s transceiver in Paper 18.8 showcases a quarter-rate bang-bang phase detector that uses a phase summer to replace a digital early-late vote counter.

# Analog Techniques

**Chair:** Axel Thomsen, Silicon Laboratories, Austin, TX
**Associate Chair:** Doug Smith, SMSC, Austin, TX

The field of analog circuit design always yields a wide variety of interesting applications, tricks, and techniques. The papers in this session predominantly deal with the classic challenges of power efficiency and compensation of complex feedback circuits.

The first 3 papers address the area of high-power audio amplifiers. There is a continued drive to achieve higher output power at high efficiency and high level of integration with acceptable levels of distortion. The first paper, 19.1 is a class-D amplifier that offers an output power of 240W. In this open-loop design, the key is the design of the gate drive. Paper 19.2 addresses the unique challenges of compensation of a linear audio amplifier due to the presence of a large gate capacitance of the output device. Paper 19.3 presents a class-D amplifier with digital input that utilizes a closed-loop architecture for improved distortion. While the power stage is external, the controller has to be designed to guarantee stability.

The next 3 papers highlight a variety of interesting details in such classic analog circuit blocks as regulators, filters, and opamps. Paper 19.4 presents an LDO regulator that utilizes an old but unusual technique to achieve unconditional stability when loaded with a wide variety of capacitors with widely varying ESR values. Paper 19.5 offers an interesting simple design for a continuous-time filter. Here the linearity and overdrive voltage of the devices are linked in an unusual manner allowing for a low-power optimization. Paper 19.6 advances the state-of-the-art in the area of chopper stabilized amplifiers. It introduces a notch filter in the signal path that removes the ripple commonly produced by the upmodulation of the chopping artifacts.

The final 2 papers come from the area of switching power supplies. Paper 19.7 shows a benchmark paper for a completely integrated switching power supply. To achieve a competitive power efficiency, extra-thick top-level copper is used and a variety of design techniques applied to enable the elimination of all external devices. Paper 19.8 presents a technique for a boost converter. It aims to eliminate the loss of a diode voltage by replacing it with a driven MOS switch. The circuit achieves a turn-on time of 20ns.

# WLAN/WPAN

**Chair:** *Arya Behzad, Broadcom, San Diego, CA*
**Associate Chair:** *Jan Craninckx, IMEC, Leuven, Belgium*

Mass consumer market wireless applications set strict requirements on cost, dynamic range, power consumption, and the number of external components used in the system. These constraints have already been applied to Bluetooth and 802.11b/g chips and the resultant chips have been reported at previous conferences. This year, we see these trends being applied to many other wireless standards such as multi-band WLAN ICs covering both the 2.4GHz band as well as the 4.9 to 5.8GHz band. At the same time authors present the first implementations of integrated multiple-antenna transceivers. Multiple-antenna techniques are used to increase the effective throughput of a wireless link as well as to increase the reliability and range of the connection. These issues are addressed in Papers 20.1 to 20.4.

On the other hand, Papers 20.5 to 20.8 address a variety of applications requiring very low power consumption for wireless connectivity. These applications include low-power home-control and industrial-automation systems utilizing the ZigBee standard as well as ultra-low-power autonomous sensor networks. In this session, several papers will present ICs addressing both of these markets.

In Paper 20.1, the authors present a 5GHz, 2×2 MIMO transceiver in 90nm CMOS supporting spatial multiplexing and diversity. Data rates of up to 108Mb/s can be achieved. Each RX consumes 120mA from a 1.4V supply. Each 3.3V 5GHz PA can deliver +13dBm average power with -27dB EVM in the 2×2 mode. The system-in-package includes microstrip front-end matching on a flip-chip package and incorporates a die with an area of 18mm$^2$.

An IEEE 802.11a/b/g wireless LAN SoC for low-power embedded applications is implemented in a 0.18µm CMOS technology and presented in Paper 20.2. The IC integrates the RF transceiver, digital PHY and MAC, CPU, and host interface. For 64QAM OFDM, the 5GHz/2.4GHz TX EVM is -27.4dB/-27.5dB at an output power of -5.2dBm/-3.5dBm. Overall 5GHz/2.4GHz RX sensitivity is -73dBm/-76dBm at 54Mb/s.

A transceiver for 802.11a/b/g access points which supports MRC diversity is presented in Paper 20.3. The diversity scheme results in a 3dB static sensitivity improvement over a single-receiver implementation. Receive ADCs and transmit DACs are included, allowing autonomous AGC and transmit power control loops and an all-digital modem/MAC IC. The 25mm$^2$ IC is fabricated in a 0.18µm CMOS process.

A highly linear up-conversion mixer with process insensitive gain control and gain insensitive output offset current is presented in Paper 20.4. A calibration scheme to remove the LO feed-through (LOFT) and I/Q imbalance is also introduced. The prototype achieves 3$^{rd}$-order IMD suppression better than 52dBc, LOFT suppression better than 32dBc, and image-rejection better than 46dBc for all gain settings.

Paper 20.5 presents a 2.4GHz RF transceiver in 0.13µm CMOS for sensor networks. The transceiver operates from 400mV to accommodate a single-solar-cell power supply. The RX consumes 200 to 750µW and achieves a NF of 6.7dB and an IIP3 of -6.2dBm at 330µW. At 300µW output power, the PA is 44% efficient and the overall TX is 30% efficient.

A 0.18µm CMOS low-IF transceiver with integrated baseband processing that is compliant with the 802.15.4 ZigBee standard is described in Paper 20.6. The 5.77mm² die draws 14.7mA (RX) and 15.7mA (TX) while achieving -102dBm RX sensitivity and 3dBm TX power.

A low-power single-chip transceiver for the 430MHz ARIB STD-T67 narrowband systems is implemented in a 0.15µm CMOS technology and is presented in Paper 20.7. The chip integrates the entire radio including filters, a demodulator, and a microcontroller. The receive current of 10.8mA and the sensitivity of -120dBm at 1% BER is achieved in 2FSK operating at 2.4kb/s.

A fully integrated super-regenerative receiver in 0.13µm CMOS with on-chip quench generation is described in Paper 20.8. Auto-calibration improves the selectivity of a Q-enhanced filter and the sensitivity of super-regeneration. The prototype consumes 2.8mW, or 5.6nJ per received bit, at 500kb/s, and has a turn-on time of 83.6µs, a channel spacing of 10MHz, and a sensitivity of –90dBm.

# Advanced Clocking, Logic and Signaling Techniques

**Chair:** *Thucydides Xanthopoulos, Cavium Networks, Marlboro, MA*
**Associate Chair:** *Sohichi Miyata, SHARP, Osaka, Japan*

Clock generation and distribution has traditionally been an area of circuit innovation due to its impact on overall chip performance and cost. In the first half of the session, a series of clocking techniques are presented that address issues such as process independence, power dissipation, low jitter, low skew, and duty-cycle correctness.

Clock-powered logic families have generated interest in the past due to their potential for low power dissipation through adiabatic charge recycling. Clock frequencies in the 100s of MHz though dictated the use of external inductive clock generators. Process and frequency scaling has enabled faster logic and the potential of fully integrating resonant clock generators on chip. In papers in the second half of this session, clock-powered logic families in the 1 to 3GHz range are presented that use integrated LC and transmission-line-based oscillators.

Process and frequency scaling has made wire-inductance modeling a necessary part of the design process. In papers in this session, the exploitation of wire inductance for clock distribution and signal transmission is demonstrated.

Integrated PLLs have been traditionally used for digital clock generation. In Paper 21.1, an alternative method of low-frequency clock synthesis, using a free-running oscillator and digital processing logic, is presented. Controlled-frequency slew rate and spread-spectrum clocking are easily implemented with this technique.

Distributing clocks in large microprocessor chips has always been a challenge. In Paper 21.2, the clock generation and distribution of a dual-core Xeon™ processor are discussed. Multiple clock-domain management is also discussed.

Wire inductance presents multiple issues to the clock designer due to complex modeling, increased wire transit time and signal reflections. In Paper 21.3, a non-traditional clock-tree design is proposed that exploits transmission-line reflection effects for duty-cycle correction and PVT insensitivity of the overall insertion delay.

Wireless on-chip clock distribution can be a low-power low-skew alternative to traditional techniques. In Paper 21.4 a wireless receiver structure that converts an 18GHz RF clock signal to a GHz-range digital clock is discussed; it can be used in this context.

In Papers 21.5 and 21.6, multi-GHz clock-powered logic families that can use a fully integrated resonant clock generator (LC or transmission-line based) are presented. Substantial energy savings are being demonstrated.

Finally, in Paper 21.7 an on-chip interconnect methodology using a negative impedance converter adapted from analog long-distance telephony is presented. The impedance converter provides loss compensation while adding minimal latency to the signal path.

# Low Power Multimedia

**Chair:** *Yiwan Wong, Hong Kong Applied Science & Technology Research Institute, Hong Kong, China*
**Associate Chair:** *Won Namgoong, University of Southern California, Los Angeles, CA*

Multimedia processing is becoming a critical requirement and a major driver of both present day and future consumer electronics equipment such as game consoles, mobile handsets, home entertainment systems, etc. With the availability of increasing data bandwidth, there is a greater demand for much more advanced multimedia processing capabilities, which in turn translates to higher computational and storage requirements on these devices. Compounding this challenge is the ever increasing demand for mobility, dictating that these multimedia functions be performed at the lowest levels of power consumption.

The seven papers in this session focus on recent advances in low power multimedia processing integrated circuits that deliver advanced functionality, such as 3D graphics, high resolution still and video encoding/decoding, and high fidelity audio playback. Results from these papers demonstrate that smart architecture design and implementation techniques, in conjunction with advanced process technology, can deliver very high-performance multimedia functionality at very low power consumption levels.

Paper 22.4, describes a VLIW graphic processor that achieves up to 120Mvertices/sec of 3D geometry. The processor supports OpenGL ES 2.0 and Vertex Shader model 3.0 while consuming approximately 50% of the energy of a conventional SIMD implementation. Paper 22.5 presents a massively parallel SIMD processor based on the Matrix architecture that achieves 40GOPS (16b additions) at 200MHz while dissipating 250mW. The processor occupies 3.1mm$^2$ in 90nm CMOS, and is targeted for consumer-based computer vision and video recognition applications.

Paper 22.2 describes a 345mW JPEG2000 codec in 0.18μm CMOS, capable of achieving a throughput of 124MS/s to support high definition (1920×1080) video encoding and decoding. In their paper, the authors discuss a scheduling scheme that eliminates the 192KB tile memory and techniques to reduce silicon area by 40%.

Low power video encoding and/or decoding chips are described in a trio of papers: Paper 22.6 presents a 5mW MPEG4 Simple Profile encoder in 0.18μm CMOS technology that encodes CIF 30frames/s in real-time at 9.5MHz. Power reduction is achieved by a 2-D bandwidth-sharing ME design, content-aware DCT/IDCT algorithm, and clock gating techniques. Paper 22.3 describes a H.264 video decoder in 0.18μm CMOS that operates at 120MHz for high definition video (HD1080, 1920×1088@30Hz) while dissipating 320mW. The internal memory size and gate-count have also been reduced through appropriate algorithmic and architectural changes. A 0.18μm CMOS MPEG-2/H.264 video decoder is described in Paper 22.1. The decoder, which employs a scalable pipeline and a prediction circuit to reduce memory bandwidth, performs real-time MPEG-2 and H.264/AVC decoding at 108μW and 125μW, respectively.

Paper 22.7 presents a multimedia processor that achieves 6.33mW decoding for MPEG audio in 0.15μm CMOS at 1.1V supply. To reduce power consumption, parallel processing DSP and conditional pre-charge sense-amp based flip-flop are used.

# Technology and Architecture Directions

**Chair:** *Werner Weber, Infineon, Munich, Germany*
**Associate Chair:** *C-K Wang, National Taiwan University, Taipei, Taiwan*

New technology and architecture solutions have the potential to enable exciting and powerful applications. This session introduces several such applications with improved power, energy, and/or performance.

Paper 23.1 demonstrates the generation of 1μW of electrical power from 1 milliCurie of benign Nickel-63 nuclear energy source at over 30% conversion efficiency. Such an energy source has the potential to enable self-powered sensor networks. Measurements show that the energy source can provide about 20nW of continuous power for low-power sensors or up to 40μW of peak power for burst mode computation and communication.

The second paper presents the first comprehensive comparison of digital and analog building blocks in FinFET and Triple-Gate transistor technologies. These multi-gate transistor technologies offer the promise to continue Moore's law of scaling by improving device electrostatics. Ring oscillator modules comprised of various CMOS logic gates, frequency dividers, and operational amplifiers demonstrate the highest level of integration reported to date using these multi-gate devices.

Paper 23.3 presents a low-power low-cost random number generator for embedded security systems. Random number generation is achieved by using the noise due to oxide traps of small area MOSFETs. This concept of random number generation is robust against external process, voltage, and temperature variations.

Papers 23.4 and 23.5 demonstrate fast yet energy efficient data communication concepts. Paper 23.4 introduces high data rate communication between chips that are three-dimensionally stacked without the need for expensive through-silicon vias. The communication between three-dimensionally stacked chips is achieved with inductive coupling. While occupying only $2mm^2$, the chips have 1024 data transceivers with a data rate of 1Gb/s per channel. The high density is achieved by using 4-phase time division multiplexing to reduce cross-talk resulting in a negligible bit error rate. The energy efficiency of the communication is 3pJ/b. The resulting solution provides an aggregate data rate of 1Tb/s and consumes 3W. Paper 23.5 introduces a new approach for realizing high-speed optical interconnects on silicon chips. This concept uses nano-photodiodes on silicon with extremely low parasitic capacitance (less than 10aF) enabling robust communication at very high frequencies. The results demonstrate 5GHz clocking with the promise of up to 20GHz. The authors will also discuss how the silicon nano-photodiode can be used for wavelength-division multiplexing and low-voltage electro-optic modulators for on-chip and off-chip optical communications.

Novel low-power architectures for computation and communication are presented in the next two papers. In Paper 23.6, the authors present the first single-chip globally-asynchronous locally-synchronous reconfigurable processor for DSP applications. The 475MHz reconfigurable processor has been tested for JPEG encoding and 802.11a/g transmitter applications. In Paper 23.7, the authors present a system-in-silicon architecture with 1024b inter-chip bus to provide high-bandwidth low-power connectivity between logic and memory. The highly parallel architecture also allows low frequency (25MHz) operation while achieving real-time motion estimation for 1080HDTV. The solution achieves the required 23.1Gb/s bandwidth and associated processing for motion estimation at a power level of 190mW.

The final paper in this session introduces the first soliton modelocked oscillator in CMOS. The pulse width is reduced by 10X compared to previous non-integrated modelocked oscillators. It is expected that this research will lead to pulse widths as short as 1ps.

# High-Performance Digital Circuits

**Chair:** *David Blaauw, University of Michigan, Ann Arbor, MI*
**Associate Chair:** *Masayuki Mizuno, NEC, Kanagawa, Japan*

With the introduction of 65nm technology, the scaling roadmap for CMOS shows no signs of slowing down. With each new technology node, previously unattainable performance levels come within reach for processor designers. However, every new technology node also brings new challenges for the circuit designers to achieve these performance gains while maintaining robust and reliable designs. Subthreshold and gate leakage currents have become dominant issues in the life of designers. Process and environmental variations have emerged as new critical issues that must be addressed up front in today's design efforts. This session includes seven papers that address new high-performance circuit techniques for robust processor designs. The papers address arithmetic designs, a register-file design, intra-chip communication, and dynamic and static circuit structures.

The first three papers focus on new arithmetic designs, which form the heart of high performance processors. The authors of Paper 24.1 present new 64b fixed-point and floating-point execution units for the POWER6™ processor implemented in 65nm CMOS. The design sets a new benchmark with over 4GHz performance and a latency of 13 FO4 delays for the fixed-point unit and 91 FO4 delays for the double-precision floating-point unit. In Paper 24.2, a trade-off study of different 64b adder designs is described; a sparse radix-4 Ling parallel prefix tree architecture is selected as the optimal design. The proposed adder is implemented in 90nm CMOS with a 250ps cycle time and 311mW measured power consumption. A new implementation of a 64b adder using the recently proposed output-prediction logic (OPL) is discussed in Paper 24.3. This aggressive dynamic logic circuit family is enhanced with self-calibrating local clock generation using dual-rail completion detection. The adder design has a cycle time of 238ps in 0.13µm CMOS and shows a speed improvement of 1.8X over a domino-logic implementation.

A new keeper circuit for dynamic domino gate structures with wide AND-OR evaluation trees is the focus of Paper 24.4. In this design, the keeper strength is dynamically adjusted through a replicated evaluation tree leakage path and current mirror. The new technique compensates for process, temperature and voltage variations and is demonstrated in a 72×1024 3-write/4-read SRAM design in 90nm CMOS.

The authors of Paper 24.5 focus on data synchronization for large global on-chip signals, which has become a difficult issue in high-frequency processor designs. A new latency-insensitive synchronization method using FIFO queues is implemented in 0.18µm CMOS for a 5.4mm bus supporting a bandwidth of 3Gb/s per wire and demonstrates compensation for ±2 clock cycles of data-clock skew.

In Paper 24.6, a fast dynamic 14:1 MUX flip-flop, implemented in 90nm CMOS technology, is described. The circuit uses replication to obtain state retention when all select signals are inactive. This structure achieves a measured clock-Q delay of less than 250ps with a 1.2V supply.

We round out the session with Paper 24.7, in which a new 8.8GHz 16x64b register-file design implemented in 65nm CMOS is presented. The design has a power consumption of 198mW with 25mW active leakage and can achieve 10.1GHz single-cycle read/write at 1.4V. Particular attention is paid to process variation through the use of variation-tolerant keeper compensation. Leakage current is addressed through the use of a leakage-tolerant bitline/wordline architecture and the use of non-minimal channel lengths.

# RF/IF Circuits

**Chair:** Tom Schiltz, Linear Technology, Colorado Springs, CO
**Associate Chair:** Satoshi Tanaka, Hitachi, Tokyo, Japan

Increasing popularity of wireless devices, including cellular phones, wireless LAN and other data services, is placing higher performance demands on the radio portion of these devices. Lower noise and higher linearity are the primary performance improvements needed in the RF and IF circuits to expand the dynamic range, and allow operation in these congested radio channels.

The eight presentations in this session highlight specific RF and IF circuit improvements that enhance dynamic range, thus permitting further growth of wireless. These improvements are realized primarily through novel circuit designs, enabled by silicon processing improvements.

A critical block in radio transmitters, the upmixer, is known to produce a broad spectrum of undesired output frequencies, in addition to the desired output. Expensive filtering is normally employed to attenuate the undesired spurious outputs prior to transmission. Paper 25.1 presents a unique upmixer topology that suppresses these undesired harmonics and sidebands to less than -40dBc, thus allowing relaxed filtering in a transmitter.

Papers 25.2 and 25.3 detail circuit techniques that improve image rejection in receivers. Both techniques incorporate automatic calibration schemes to balance the I- and Q-path gains, and optimize phase quadrature.

Solutions to improve the $2^{nd}$-order rejection in direct conversion receivers are presented in Papers 25.4 and 25.5. Measurements show IIP2 improvements of 18 to 20dB in both cases.

A unique bias-control scheme for an active channel-select filter is presented in Paper 25.6, which adapts the bias current depending on the level of a blocking signal.

The session concludes with two papers that present improved direct I/Q demodulator performance. Paper 25.7 utilizes a local oscillator at one-half the normal frequency to reduce LO leakage at the RF input to -91dBm. Paper 25.8, on the other hand, uses an LO at twice the normal frequency to reduce 1/f noise contributions, resulting in a 9dB NF improvement.

# Cellular Building Blocks and SoCs

**Chair:** *Charles Chien, SST Communications, Marina Del Rey, CA*
**Associate Chair:** *Jacques C. Rudell, Intel, Santa Clara, CA*

Since 1990, we have witnessed a tremendous growth in wireless technology that has positively impacted our daily lives. During the early stages of this wireless revolution, analog cellular and paging technology were widely used. Later these analog systems migrated to digital transmission technology. The so-called second-generation (2G) digital cellular systems include *global system for mobile communications* (GSM), *personal handy-phone system* (PHS), IS95 CDMA, and IS136 TDMA. More recently 2.5G digital cellular systems such as *GSM packet radio system* (GPRS) and 3G cellular systems have emerged to support services for not only voice but also digital images, video streaming, and music downloads. Current penetration of 2G and 2.5G cellular technology has reached a global scale with number of subscribers surpassing 1.5 billion and growing steadily at 7 to 10% every year. One major factor that has spurred this rapid growth is the advent of low-cost semiconductor technology that has made it possible to integrate complex wireless circuits and digital processing on highly integrated low-cost SoCs.

The ten papers in this session represent a snapshot of the recent advances in cellular integrated circuits, ranging from high-performance building blocks to fully integrated cellular SoCs that include both RF/analog and digital processing on the same chip. It is shown in these papers that the continued scaling of silicon technologies can enable increased levels of integration and enhanced performance, while reducing the overall system cost.

Five of the papers in this session cover building blocks for GSM systems. Paper 26.1 describes a highly linear direct-conversion front-end for GSM in 90nm CMOS that achieves 51dBm IIP2. Paper 26.4 presents a 0.25µm CMOS low-IF receiver that achieves greater than 50dB image-rejection ratio based on digital calibration over the entire signal bandwidth at 200kHz IF. Paper 26.5 presents a 0.18µm CMOS fractional-N synthesizer that achieves integrated phase noise of $0.8^{\circ}$ using LMS-based DAC gain calibration. Paper 26.9 presents a 0.13µm CMOS power amplifier that is applicable for GSM. With the Doherty topology, it delivers 1.5W at 1.7GHz. Paper 26.10 presents a 65nm $\Delta\Sigma$ modulator that achieves peak SNDRs of 90dB and 62dB for GSM and WCDMA, respectively.

Two papers in this session cover GPS which are becoming an essential component for modern handsets that must support location-based services and E-911. Paper 26.2 describes a 0.13µm CMOS GPS front-end that dissipates only 5.4mW using current-reuse of the LNA, mixer, and VCO. Paper 26.3 describes a fully integrated GPS receiver in 0.18µm SiGe BiCMOS that addresses the coexistence of GPS with cellular transmissions.

Paper 26.6 presents a 90nm CMOS software-defined radio receiver that covers various bands in the 800MHz to 5GHz frequency range. The tuning over multiple RF bands and 100dB dynamic range are achieved with 5 to 5.5dB of NF, -3.5dBm of IIP3, and 39dBm of IIP2. This radio can receive signals for various standards such as GSM and IEEE 802.11b/g.

Finally, two papers in this session cover cellular SoCs which include not only the RF/analog circuits but also digital processing on the same chip. Paper 26.7 presents the first true SoC for quad-band GSM/GPRS that integrates RF, analog/mixed signal blocks, digital signal processing, application processor, RAM/ROM, and audio circuitry. This SoC is implemented in a low-cost 0.13µm CMOS process, while achieving a sensitivity of less than -110dBm and a transmit power of greater than 3dBm.

Paper 26.8 presents the first SoC for PHS system that include all RF, analog baseband, power management, and digital functions of a handset. This SoC is implemented in a low-cost 0.18µm CMOS process. It draws 81mA from a 1.8V supply, occupies $35mm^2$, and achieves -106dBm sensitivity, +4dBm EVM-compliant transmit power, and 15µs synthesizer settling time.

# Image Sensors

**Chair:** *Boyd Fowler, Fairchild Imaging, Milpitas, CA, USA*
**Associate Chair:** *Makoto Ikeda, University of Tokyo, Tokyo, Japan*

It is estimated that more than 500 million cell-phone cameras and more than 80 million digital still cameras will be sold in 2007. The explosive growth rate of these businesses is being fueled by the development of low-cost high-quality CMOS image sensors. These sensors are being developed by design houses and vertically integrated companies. They are manufactured in both private and publicly available foundries.

The nine presentations in this session represent a snapshot of the recent developments in CMOS image sensors for cell-phone cameras, digital still cameras, HDTV camcorders, and machine vision. It is shown in these papers that the quality of CMOS image sensors is still improving with no clear bound in sight. In addition, the variety of applications for CMOS image sensors is still expanding.

Papers 27.1 and 27.2, present the state-of-the-art in CMOS image sensors for digital still cameras; this include pixel densities greater than 6 million, with pixel sizes less than 2.5μm, and random noise with rms levels less than 8e-. Both of these sensors produce outstanding imagery in both high and low light-level environments.

The next two papers present techniques for improving conversion gain and reducing temporal and fixed-pattern noise in standard 3T active pixel sensors. In Paper 27.3, feedback is used to increase conversion gain by a factor of 5 and reduce reset noise by a factor of 2. Pseudo randomization is used in Paper 27.4 to reduce the peak fixed-pattern noise by more than a factor of 2.

The session continues with two papers that focus on the HDTV market. Paper 27.5 describes a sensor that combines high-speed readout and low-noise operation. It achieves 180 frames per second with 5.2e- rms read noise and 15.9e-/pixel/s dark current at 60°C. Paper 27.6 describes the highest performance analog front-end for HDTV CCD sensors, yet published. It achieves 14-bit 74MS/s performance.

The final three papers present the state of the art in machine vision sensors. In Paper 27.7, the first-published camera-on-a-chip sensor for high-speed industrial cameras is presented. It achieves greater than 1000 frames per second at 516×514 pixel resolution with a standard camera-link interface. Paper 27.8 describes the first-published fully integrated stereo vision sensor that is capable of depth perception at 30 frames per second. It achieves a depth resolution of 0.39m while only consuming 33.6mW. The last paper, Paper 27.9, presents a sensor that is inspired by the human retina. This sensor achieves a dynamic range of greater than 120dB while responding to relative intensity changes in less than 100μs.

# Wireline Building Blocks

**Chair:** *Kevin Kornegay, Georgia Tech, Atlanta, GA*
**Associate Chair:** *Herman Casier, AMI Semiconductors, Belgium*

This session addresses the key issues associated with the design of building blocks to facilitate advances in wireline communications.

Size reduction is an important factor in increasing the line densities in telephone exchanges. Paper 28.1 employs a selectivity booster chip and compact LC low-pass filter to replace the bulky POTS/ADSL splitter.

To meet the performance demands of future high-data-rate communication systems requires high-frequency amplifiers with high gain and large bandwidth. Implementation in CMOS is essential in reducing the cost of the components that make up these systems. In paper 28.2 traditional shunt and series inductive peaking are combined with capacitive bandwidth extension to achieve 44GHz bandwidth with a 19dB gain in 90nm CMOS. Paper 28.3 presents design techniques for an AGC amplifier to accommodate a 35dB dynamic range input signal level at 10Gb/s data rate. The 0.18µm CMOS chip incorporates a peak detector, integrator, and exponential voltage generator in the gain control loop. Paper 28.9 achieves 20Gb/s data demultiplexing in a 0.13µm CMOS technology. A very compact circuit is realized by avoiding the use of inductors.

Bidirectional signaling allows for doubling data capacity of a single twisted-pair line. Paper 28.4 presents a 0.11µm CMOS chip that reaches a maximum data rate per differential pair of 20Gb/s using a resistor-transconductor hybrid circuit for the upstream and downstream signals.

Timing accuracy is a basic challenge in high-speed electrical communication links. The following papers describe advances in clock-jitter measurements, clock duty-cycle control, and clock generation. Paper 28.5 uses an oversampling technique in an on-chip jitter measurement macro to achieve 1ps of resolution. Paper 28.6 presents a high-precision arbitrary timing generator for ATE applications with 40 channels available at 1GHz or 10 multiplexed channels at 4GHz, each with a timing resolution of 1.83ps. Paper 28.7 describes a clock duty-cycle IC capable of correcting a 50±20% clock signal duty-cycle to a 1.25% accurate user selectable duty-cycle.

Process variability has a tremendous impact in maintaining circuit performance. Paper 28.8 demonstrates 66GHz divider operation in 90nm SOI CMOS using a statistical methodology and proves its manufacturability against process variability with comprehensive characterization data.

To support future high-data-rate communications very high-speed PRBS pattern generators are required. Paper 28.10 sets a speed record for on-chip PRBS generation using an advanced InP DHBT technology.

# Power Management and Distribution

**Chair:** *Atila Alvandpour, Linköping University, Linköping, Sweden*
**Associate Chair:** *Hannu Tenhunen, Royal Institute of Technology, Stockholm, Sweden*

Design of power management and distribution is getting significantly more difficult for each new CMOS technology node. Power management and distribution ensures robust and consistent operating voltages to complex ICs independent of their operating conditions and changes to their operational environment (for example, changes to clock frequency). Furthermore effective and systematic control of leakage currents is becoming one of the main challenges especially for circuits used in portable applications.

The eight papers in this session present the current state-of-the-art in power distribution and management, on-chip measurements, voltage-domain stacking for high voltage I/O, and ESD protection to power pins.

In Paper 29.1, spatially-resolved imaging of microprocessor power is shown to be a critical tool for the development of multi-core processors. In Paper 29.2, an on-chip linear regulator for biasing DC-DC converters is introduced. For supporting local stable operating voltages and improved frequency, high-K MIM decoupling capacitors are implemented in Paper 29.3.

For complex and heterogeneous single-chip multi-CPU processors, multiple power domains need to be implemented for controlling both the leakage currents and performance. In Paper 29.4 and Paper 29.5, techniques and implementations of a 20 power domain multi-core CPU is discussed for portable 3G/GSM applications.

Systematic fully-integrated signal integrity self-test with analog monitors and digital test-compatible scan chains is introduced in Paper 29.6 for monitoring chip power distribution performance. In Paper 29.7 an ESD protection design for 1.2V/2.5V mixed-voltage I/O interfaces by using high-voltage-tolerant power-rail ESD clamp circuit realized with low-voltage devices is presented.

When a high-performance processor is changing its operating clock frequency it can introduce large voltage disturbances in power rails. In Paper 29.8, a circuit is proposed which controls the frequency ramp between initial and final operating frequency by periodically masking clock pulses to change incrementally the average clock frequency.

# Silicon for Biology

**Chair:** ***Glenn Gulak****, University of Toronto, Toronto, Canada*
**Associate Chair:** ***Hoi-Jun Yoo****, KAIST, Daejeon, Korea*

The increasing world-wide focus on human healthcare and well-being is providing a major impetus for the development of new types of prosthetic microsystems, diagnostic systems, and body-sensor networking. The technology being brought to bear on this challenge ranges from traditional CMOS circuits to biologically inspired architectures, RF, optics and MEMS. Low cost, small form-factor, low power consumption and reusability are key enablers. Complete integrated microsystems, optimized for specific applications, offers the potential for significant impact on future medical care.

The six presentations in this session provide a broad perspective on recent advances in achieving this vision, ranging from implanted microelectronic devices, human body communications, and reusable diagnostic systems. Wireless technology of various types plays an important role in achieving a convenient, sterile interface between silicon and humans.

In Paper 30.1, an implantable prosthesis processor for sensing and translating neural signals into motor commands is described. The data compression factor is on the order of $10^6$, translating 80Mb/s neural data to < 20b/s for the intended movement signals. In Paper 30.2, a neuron signal-processing IC with 433MHz FSK wireless transceiver is integrated with a 10×10 platinum-tipped silicon electrode array. It can provide neuroprosthetic devices with 330kb/s data rates while consuming 13.5mW.

In Paper 30.3, a mixed-mode cochlear-like preprocessing chip is presented for possible application to speech-recognition systems. Its biomorphic architecture adopts active bidirectional coupling and enhances formant perception in noisy environments.

In Paper 30.4, a convenient short-distance communication scheme uses the human body as the data transmission medium. A 2Mb/s wideband pulse transceiver uses a single electrode structure with low power consumption.

A label-free electrochemical CMOS DNA detector is presented in Paper 30.5. This 25×3mm$^2$ IC, fabricated in 1$\mu$m 2M CMOS process provides quantitative analysis with high sensitivity and accuracy. Paper 30.6 is another label-free detection system for C-reactive protein that makes use of a MEMS/electronic hybrid system with a wireless ASK transceiver. Disease-sensitive anti-CRP is deposited on the tip of the MEMS cantilever, and it's deflection is monitored with laser optics. Concentrations of 1ug/mL to 500ug/mL can be detected; a 1 V, 0.2Hz signal is applied for reuse of the cantilever.

# Very High-Speed ADCs and DACs

**Chair:** Dieter Draxelmayr, Infineon Technologies, Villach, Austria
**Associate Chair:** Gabriele Manganaro, National Semiconductor, Salem, NH

High-speed ADCs and DACs are gaining increasing importance due to the ever increasing bandwidth reqirements of modern communication services. Typical examples of such high-speed applications are serial links, UWB devices, and storage systems. Most of these systems do not require very high resolution, but high speed is of crucial importance. At the same time the power has to be kept low in order to enable single-chip and even portable solutions.

The nine presentations in this session are grouped into six ADC and three DAC papers. ADC resolutions are in the range of 4 to 6 bits with the exception of the last one which is an 11-bit converter. All DACs run at RF frequencies except for the last one, which demonstrates a novel linearization technique for high-resolution DACs.

Paper 31.1 is targeted at high-speed (1.25GS/s) and low-resolution (4 bits) applications and has a superior power efficiency. To achieve this goal the flash-based design uses an unusual comparator architecture that incorporates offset correction and is capable of avoiding the reference ladder.

In contrast to that, the ADC in Paper 31.3 goes up to 4GS/s. It is also based on the flash architecture but incorporates inductors in the comparators to gain an extra kick in speed.

Papers 31.2 and 31.5 describe 6-bit converters which are typically needed for UWB and storage systems. Paper 31.2 incorporates a subranging technology. In order to achieve low power dissipation it uses an offset-calibration technique that accounts for all the errors in the complete signal chain. Additionally, it uses a range-switching scheme that is more insensitive to metastability than the usual approach. The ADC described in Paper 31.5 demonstrates superior power efficiency in using a time-interleaved non-binary SAR architecture. Asynchronous design techniques enable optimized speed performance.

The converter presented in Paper 31.4 runs at 22GS/s, therefore, enabling digital equalization of 10Gb/s serial links. The chip is fabricated in a 0.13µm SiGe BiCMOS technology and has a sufficiently low power that enables the integration of a complete 4-channel solution on one die. It also uses an active offset control.

The ADC papers are concluded by Paper 31.6 that presents a 1GS/s 11-bit ADC running at only 250mW. This is achieved by time interleaving of 4 double-sampled pipelined channels. The paper specifically addresses the problem of sampling-time mismatch in using a distributed double switch.

The last three papers are about DACs. The chip presented in Paper 31.7 incorporates frequency generation, filtering, and up-conversion in a compact building block consisting of a current steering semi-digital filter implemented as an RF-DAC. In contrast to that, the circuit in Paper 31.8 uses a very high-speed DAC (20GS/s) to directly form the output wave of an UWB transmitter.

The last paper, Paper 31.9, concludes the session by discussing a dynamic element matching scheme for binary-weighted structures. The technique is demonstrated for a 14-bit highly linear DAC.

# PLLs, VCOs and Dividers

**Chair:** *Ian Galton, University of California at San DIego*
**Associate Chair:** *Takehiko Nakao, Toshiba, Kawasaki, Japan*

Phase locked loops (PLLs) are critical blocks in virtually all solid-state electronic systems. They frequently determine overall system performance in applications such as cellular radio and high-speed serial communications, and are essential for clock generation in system-on-a-chip (SoC) applications. For example, the phase noise from the RF PLL in a cellular telephone receiver mixes with interfering signals and corrupts the desired signal, so the ability of the receiver to reject interference depends critically on the PLL phase noise.

As communication and storage standards evolve toward higher frequencies and higher bandwidths, the performance limitations of PLLs become increasingly critical. PLLs frequently must be integrated with large digital blocks so there is strong and increasing pressure to implement high-performance PLLs in highly-scaled CMOS technology. The 9 papers in this session present several PLLs and PLL components that incorporate techniques to overcome various analog circuit limitations of highly scaled CMOS technology.

The first five papers present PLLs. Paper 32.1 describes a VHF synthesizer PLL with a high division ratio that does not require an off-chip loop filter and is insensitive to PVT variations. Paper 32.2 presents a 2.5GHz ring-oscillator-based PLL that incorporates techniques to improve power supply rejection and 1/*f* noise performance. Paper 32.3 presents a PLL that generates a 63-phase selectable clock for a DVD write system. It utilizes a compact coupled ring oscillator structure to achieve 32ps phase resolution. Paper 32.4 demonstrates an enhancement based on multiple delayed PFDs and charge pumps to reduce the reference spur. Paper 32.5 presents a 6.25GHz LC-oscillator-based PLL that achieves $0.55ps_{rms}$ jitter from a 1V supply. It demonstrates a new charge pump that addresses problems associated with low-voltage CMOS processes including leakage current and reduced headroom.

The last four papers present critical PLL components. Paper 32.6 demonstrates an 11.4GHz distributed VCO consisting of 12 coupled negative $g_m$ cells to generate 24 clock phases with direction control. Papers 32.7 and 32.8 demonstrate extremely high-frequency CMOS divide-by-4 circuits based on different techniques that each provide new high-water marks in performance. The circuit presented in Paper 32.7 incorporates static and dynamic dividers. It has an input frequency of 40GHz and a power consumption of 3mW. The circuit presented in Paper 32.8 is a harmonic injection locked divider with an input frequency of 70GHz and a power consumption of 2.75mW. Paper 32.9 demonstrates a divide-by-3 injection-locked divider circuit with an input frequency of 16-18GHz and an extended tuning range relative to previous injection locked divide-by-3 circuits.

# Mobile TV

**Chair:** *Bud Taddiken, Microtune, Plano, TX*
**Associate Chair:** *Sang-Gug Lee, Information and Communications University, Daejeon, Korea*

TV on a mobile phone is not new. Analog TV tuners have been used in mobile phones in several countries over the years. However, the technology never took off because of the power and performance penalties inherent to analog TV broadcasting and receivers. Digital broadcasting technologies such as DVB-H, DMB, ISDB-T, and MediaFLO solve these technical problems. In a recent Credit Suisse First Boston forecast[1], it is estimated that 150M handsets per year will ship with digital TV reception capability by 2009 representing a new $1B opportunity for semiconductor manufacturers and many times that for handset manufacturers and mobile phone operators. In some countries these services are already commercially available today while many other countries are completing field trials and preparing for commercial introduction during 2006. The first six presentations in this session represent a snapshot of the recent advances in tuner integrated circuits for all of these mobile digital TV broadcasting technologies.

For the first time ever, a single chip DVB-H tuner is presented in this session. In fact, the first three papers all share this world's first. All three feature dual-band support for both European DVB-H requirements in the UHF frequency spectrum and US DVB-H requirements in the L-Band frequency spectrum. Papers 33.1 and 33.2 accomplish this using CMOS technology, while Paper 33.3 uses a SiGe BiCMOS process. The CMOS chips show smaller die size than that of the SiGe BiCMOS implementation, but the SiGe BiCMOS IC achieves better noise figure performance.

Paper 33.4 describes the world's first tuner IC for MediaFLO. Unlike the DVB-H tuners, it only operates in a narrow frequency range of 698MHz to 746MHz, but it has an extremely low noise figure of 2.6dB, consumes a mere 160mW, and has the smallest die area of any of the other tuners presented in this session.

The last two tuner papers in this session address DMB implementations. In addition to T-DMB operation in VHF Band-III and L-band, Paper 33.5 also demonstrates ISDB-T 1- and 3-segment operation in the VHF and UHF bands. Power consumption is only 100mW in the UHF band. This is the lowest continuous power of all the tuners in this session, and this is critical because DMB and ISDB-T are not able to take advantage of the power-saving feature of DVB-H known as time-slicing. The tuner presented in Paper 33.6 supports the S-DMB system. The previous five papers in this session are terrestrial tuners, but this one is for satellite reception of mobile digital TV. As such, it features the lowest noise figure of any of the six tuners presented in this session.

Finally, Paper 33.7 demonstrates a fully integrated frequency synthesizer for a DBS satellite tuner-demodulator SoC. With 0.3mm$^2$, it has much smaller die area than previous designs yet requires the fewest off-chip components.

[1] "I want my, I want my M(obile)TV," Sandbox Vol. 61, Credit Suisse First Boston Equity Research, May 25, 2005.

# SRAM

**Chair:** Bruce Bateman, T-RAM Semiconductor, San Jose, CA
**Associate Chair:** Jinyong Chung, POSTECH, Pohang, Korea

The demand for SRAM storage is driven by two challenging and often conflicting requirements – the first, being high clock-rate, low latency, and high data-bandwidth for processing and data communications, and the second, being low power for portable battery-powered applications, driving the exploration of extremely low operating voltages on nano-scale process technologies.

Achieving these requirements is made more difficult as process technology scales down to smaller dimensions. Subthreshold leakage currents, gate-oxide tunneling currents, and statistical variations in transistor characteristics make the design of 6T SRAM cells increasingly difficult and solutions tend to increase the memory cell size. Thus, there is a need to find better methods for modeling the electrical characteristics of alternative cell designs and for exploring alternatives to the 6T cell that can offer better density without compromising 6T performance.

The first three papers in this session show advances in the high-performance high-density arena. In Paper 34.1, a 64MB data cache for the POWER6® processor operating at 5GHz in a 65nm SOI process, is described. Cell stability and macro operating power are addressed with the use of dual voltage supplies. A 256kb SRAM block used to build last-level caches in high-performance CPUs is described in Paper 34.2. The 4.2GHz 65nm block uses actively managed dual voltage supplies to reduce power and to provide reliable operation at lower voltages with improved array density. The authors of Paper 34.3 present a 72Mb SRAM with synchronous 144b-wide separate I/Os to achieve a stunning 504Gb/s data bandwidth. The chip offers programmable de-skew and improved input- and output-impedance calibration to assist the board designer in achieving this level of performance.

The fourth paper, 34.4, addresses the need for extremely low power by describing a 256kb SRAM on a 65nm process, operating in the subthreshold regime. A 10T cell design insures subthreshold functionality and low leakage with $V_{DD}$ as low as 0.3V and 0.4V, reducing chip power by 3.8X and 2.4X, respectively, compared to above-threshold operation at $V_{DD}$ of 0.6V.

A new statistical method for determining the write margin of an SRAM cell design is presented in Paper 34.5. The new method takes into account the effects of the feedback in the cell, thus giving a more accurate determination of the cells writability with respect to PVT variation.

The final paper, 34.6, introduces a new thryistor-based memory technology that offers circuit performance similar to SRAM, but at 2X to 3X the density. The technology is demonstrated on a 9Mb test chip on a 0.13µm SOI process with a cell size of 0.562µm$^2$, but it scales well to more advanced processes and future technologies such as FinFET.

# NOTES

# ISSCC 2006

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# TABLE OF FEATURED PAPERS

| Paper Number | Subcommittee | Advance Program Page | Press-Book Page | Press-Copy Page |
|---|---|---|---|---|
| 2.3 | Imagers, MEMS, Medical and Display | 20 | 72 | |
| 2.4 | Imagers, MEMS, Medical and Display | 21 | 73 | |
| 2.5 | Imagers, MEMS, Medical and Display | 21 | 73 | |
| 3.1 | Data Converters | 22 | 43 | 197 |
| 3.2 | Data Converters | 22 | 43 | 197 |
| 4.1 | Wireline Communications | 24 | 148 | 198 |
| 4.4 | Wireline Communications | 24 | 148 | 198 |
| 5.1 | Digital | 26 | 52 | 199, 200 |
| 5.1 | Digital | 26 | 62 | 199,200 |
| 5.2 | Digital | 26 | 52 | 199 |
| 5.3 | Digital | 26 | 52 | 199 |
| 5.3 | Digital | 26 | 53 | 199, 200 |
| 5.4 | Digital | 26 | 52 | 199 |
| 5.5 | Digital | 27 | 52 | 199 |
| 5.7 | Digital | 27 | 53 | 200 |
| 5.7 | Digital | 27 | 61 | |
| 6.4 | Wireless and RF Communications | 28 | 133 | |
| 6.6 | Wireless and RF Communications | 29 | 133 | 201 |
| 7.1 | Memory | 30 | 92 | 202 |
| 7.6 | Memory | 31 | 93 | 203 |
| 7.7 | Memory | 31 | 92 | 204 |
| 8.1 | Memory | 36 | 94 | 205 |
| 8.6 | Memory | 37 | 95 | 205, 206 |
| 8.7 | Memory | 37 | 95 | 205, 206 |
| 9.2 | Imagers, MEMS, Medical and Display | 38 | 74 | |
| 10.1 | Wireless and RF Communications | 39 | 135 | 207 |
| 10.3 | Wireless and RF Communications | 39 | 135 | 207 |
| 11.5 | Analog and RF | 40 | 31 | |
| 12.1 | Data Converters | 42 | 44 | |
| 12.2 | Data Converters | 42 | 44 | |
| 12.3 | Data Converters | 42 | 44 | |
| 12.5 | Data Converters | 43 | 44 | |
| 13.1 | Wireline Communications | 44 | 149 | 208 |
| 13.7 | Wireline Communications | 45 | 149 | 208 |
| 13.9 | Wireline Communications | 45 | 149 | 208 |
| 14.5 | Signal Processing | 47 | 106 | 209 |
| 15.2 | Technology Directions | 48 | 117 | 210 |
| 15.4 | Technology Directions | 48 | 117 | 211 |
| 16.1 | Imagers, MEMS, Medical and Display | 50 | 75 | |
| 16.5 | Imagers, MEMS, Medical and Display | 51 | 76 | |
| 17.1 | Technology Directions | 52 | 118 | 212 |
| 17.2 | Technology Directions | 52 | 118 | 212 |
| 17.3 | Technology Directions | 52 | 118 | 212 |
| 17.4 | Technology Directions | 52 | 120 | |
| 17.5 | Technology Directions | 53 | 119 | 213 |
| 17.7 | Technology Directions | 53 | 119 | 213 |
| 17.8 | Technology Directions | 53 | 120 | |
| 18.1 | Wireline Communications | 54 | 150 | 214 |
| 18.6 | Wireline Communications | 55 | 150 | 214 |
| 19.1 | Analog and RF | 58 | 32 | 215 |
| 19.3 | Analog and RF | 58 | 32 | |
| 19.7 | Analog and RF | 59 | 34 | |
| 20.2 | Wireless and RF Communications | 60 | 137 | 216 |
| 20.6 | Wireless and RF Communications | 61 | 137 | 216 |
| 21.5 | Digital | 63 | 55 | 217 |
| 21.6 | Digital | 63 | 55 | 217 |
| 22.3 | Signal Processing | 66 | 108 | 219 |
| 22.4 | Signal Processing | 66 | 107 | 218 |

# TABLE OF FEATURED PAPERS

| Paper Number | Subcommittee | Advance Program Page | Press-Book Page | Press-Copy Page |
|---|---|---|---|---|
| 22.6 | Signal Processing | 67 | 108 | 219 |
| 23.1 | Technology Directions | 68 | 121 | 220 |
| 23.2 | Technology Directions | 68 | 121 | |
| 23.4 | Technology Directions | 68 | 121 | 221 |
| 23.5 | Technology Directions | 69 | 121 | 221 |
| 24.1 | Digital | 70 | 53 | 200 |
| 24.2 | Digital | 70 | 59 | |
| 24.3 | Digital | 70 | 59 | |
| 24.4 | Digital | 71 | 58 | |
| 24.7 | Digital | 71 | 53 | 200 |
| 24.7 | Digital | 71 | 61 | 200 |
| 25.1 | Analog and RF | 72 | 35 | |
| 26.7 | Wireless and RF Communications | 75 | 138 | 222 |
| 26.8 | Wireless and RF Communications | 75 | 138 | 222 |
| 27.1 | Imagers, MEMS, Medical and Display | 76 | 77 | |
| 27.9 | Imagers, MEMS, Medical and Display | 77 | 78 | |
| 28.5 | Wireline Communications | 78 | 151 | 228 |
| 28.10 | Wireline Communications | 79 | 151 | 228 |
| 29.2 | Digital | 80 | 56 | 199, 223 |
| 29.4 | Digital | 80 | 56 | 199, 223 |
| 29.5 | Digital | 81 | 56 | 199, 223 |
| 29.6 | Digital | 81 | 56 | 223 |
| 30.1 | Technology Directions | 82 | 122 | 224 |
| 30.2 | Technology Directions | 82 | 122 | 224 |
| 30.4 | Technology Directions | 83 | 124 | |
| 30.6 | Technology Directions | 83 | 123 | 225 |
| 31.1 | Data Converters | 84 | 44 | 197, 226 |
| 31.5 | Data Converters | 85 | 44 | |
| 31.6 | Data Converters | 85 | 44 | |
| 32.5 | Analog and RF | 87 | 36 | |
| 33.1 | Wireless and RF Communications | 88 | 140 | 227 |
| 33.6 | Wireless and RF Communications | 89 | 140 | 227 |
| 34.1 | Memory | 90 | 96 | |
| 34.6 | Memory | 91 | 97 | |

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# USING DIGITAL TO FIX ANALOG

Where would analog circuits be without digital? Today's high-performance analog circuits depend on digital circuits to maximize performance. These techniques are exposed at ISSCC 2006.

One perennial problem is that comparators are essential to high-speed analog-to-digital converter design: They are the fundamental building block that converts an analog signal to a digital "1" or "0". To get the required accuracy the devices in a comparator must be large, resulting in excessive power consumption. To overcome this, a digital circuit may measure the offsets of two comparators and select the best one. If that is not good enough, a small auxiliary circuit can compensate the remaining offsets, resulting in perfect performance in a minimum-sized comparator, with an overall ADC-power-consumption benefit. (Papers 31.1 to 31.4)

Can analog amplifiers be done away with completely? One paper considers eliminating the use of amplifiers in a large class of analog circuits, and simplifying the circuit with only a digital-control system and a voltage-comparison circuit. (Paper 12.4)

Traditionally, with high-speed digital-to-analog converters, the unit elements must match to a high accuracy; However, using digital circuits offers the opportunity to switch between mismatched elements at high speed, and hide the inherent analog mismatch of unit elements. (Paper 31.9)

Delta-sigma techniques are well known for replacing complex analog processing with digital filtering to simplify analog-to-digital and digital-to-analog converters. These techniques have been common for audio, but are now becoming pervasive wider-bandwidth applications, including TV and radio. (Session 3).

In all of these cases, the use of digital circuits helps the analog design to perform better, either making the analog circuits themselves perform better, or hiding their non-idealities of the analog circuits.

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# "TEACHING OLD LINKS NEW TRICKS"

With continuing advances in silicon technology, increasing clock rates of processing cores drives the need to push electrical interconnect speeds to higher data rates. As industry-standard data rates pass 5Gb/s, signal degradation from channel effects such as bandwidth loss, reflections and crosstalk, can distort the signal to such an extent that robust data recovery requires complex designs for backplane and cable transceivers.

As highlighted by several presentations at ISSCC 2006, these requirements are currently addressed by transceiver designs using PAM4 signaling for unshielded twisted-pair cables, PAM2 over legacy backplanes, as well as on memory busses. Complete, single-chip realizations in 90nm and 130nm bring up the speed of these solutions beyond 10Gb/s, while reducing power and cost, substantially. On top of that, clever circuit solutions are capable of fully exploiting the benefits of current deep sub-micron technologies.

These approaches, realizing data rates up to 20Gb/s, will be described at ISSCC 2006, in the session on gigabit transceivers. All of these developments indicate that old-style electrical interconnects will have a much longer lifetime than expected. A rare piece of good news! But typical for the solid engineering developments to be disclosed at ISSCC!

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# MULTICORE, MULTITHREADED CHIPS

Despite the increased constraining limits on the growth of microprocessor clock frequencies, Moore's Law for transistor density continues unabated, with the appearance of several-billion-plus-transistor chips. While many of these transistors are used in on-chip memory structures such as caches, the number of transistors that are still available for processor logic has long since passed our ability to design new-single processor cores whose performance increases due to microarchitectural complexity warrant the cost of the additional transistors. The alternative is obvious: implement multiple independent CPU cores on the same die. The technique, called Chip-level Multi-Processing or CMP, is becoming virtually ubiquitous across a wide spectrum of applications, from commodity designs such as microprocessors, routers, and graphics engines, to application-specific chips for game engines, cell phones, digital radios, and other SoCs. While the most public attention may have focused on 2-core commodity microprocessors, many (if not most) of the other multicore applications have long since made the leap to 10s or even 100s of cores. Both homogeneous multicore (where all on-chip cores are of the same design), and heterogeneous multicore (where there is a mix of different core types), designs have appeared, with the newest designs being discussed at ISSCC 2006, at the San Francisco Marriott in February.

Given that each core on such multicore chips is typically capable of independently running a separate program thread, such chips have also naturally evolved to efficiently host programs that are inherently multithreaded, that is programs where many different program fragments can be executed concurrently. This capability has also permeated into many individual core designs, where each core can now contain the state of several different threads, and switch between them when one thread finds a condition requiring a significant delay, such as a long latency memory reference. Again, many of the multicore chips discussed at ISSCC 2006 exhibit such capabilities.

In particular, five papers in the Processors session at ISSCC 2006 discuss multicore chips of both homogeneous and heterogeneous design (Papers 5.1, 5.2, 5.3, 5.4, 5.5). While dual-core, dual threaded, chips were introduced at ISSCC 2004 and 2005, Paper 5.1 in 2006 marks a new advance by introducing a server-level commodity microprocessor chip, Niagara, with eight 64-bit cores, each of which can support four concurrent threads. In contrast, Paper 5.2 addresses a network processor with over 16 cores of several types, both general-purpose processors and security- and network-accelerator engines. Two other Papers, 5.3 and 5.4, address dual-core designs fabricated in leading-edge technologies, where different aspects of the memory hierarchy have received special attention.

Implementations of such multicore architectures have introduced new problems to their designers. Papers 21.2 and 21.3 address clock generation and distribution among cores. Paper 5.5 introduces a high-speed processor-interconnect bus that allows dual cores to share on- and off-chip resources. Paper 29.2 describes temperature- and power-distribution measurements over dual-core chips. Papers 29.4 and 29.5 both address power distribution on multicore SoCs especially designed for low-power applications

The next step beyond multicore, multithreaded, chips are systems made of many such chips. Paper 5.6, in particular, addresses technologies that will allow very-high-bandwidth interconnection within multichip systems.

Finally, this year's Advanced Circuits Forum, entitled "Multicore Architectures: Design and Implementation Challenges," addresses this overall trend, and what it means in terms of both chip architecture and design practices. This forum includes what new circuit and subsystem blocks may be needed, and how all of this may affect the design and fabrication processes to be used.

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# THE EMERGENCE OF 65NM

Moore's Law has predicted a scaling trend for digital CMOS technology of 0.7x the critical feature size (or 2x the density) every 2 years. Remarkably, the rate of scaling has followed or even exceeded this prediction. Twenty years of scaling has led to an exponential growth in the electronics industry that has produced ever- more-highly-integrated and higher-performing products. The computing, mobile, and Internet revolutions are fueled by the continued scaling of CMOS devices, and the high-performance digital processing that has accompanied scaling. However, forecasting services such as ITRS have been increasingly alarmed at the challenges in producing the finer feature sizes. A slowing of scaling is inevitable in order to avoid sacrificing the speed- or power-performance of the devices and wires, substantially. Sessions 5 and 24 at ISSCC 2006 at the San Francisco Marriott, February 5-9, 2006, illustrates a multicore microprocessor and execution cores in 65nm CMOS technology. These announcements, occurring only 2 years after corresponding 90nm announcements, indicate that the trend is still being maintained.

Deeply-scaled CMOS technologies have the potential for higher-speed performance, but also have a greater tradeoff with power dissipation. Leakage currents and process/voltage/temperature (PVT) variations are of even greater concern. Four presentations to be made at ISSCC 2006 [Papers 5.3, 5.7, 24.1, 24.7] describe the various architectural and circuit techniques to address the challenges to advancing the processing core to the next level of scaled performance. Two of them [Papers 5.7, 24.7] describe the first-ever 9GHz processing elements. Circuit architectural enhancements such as greater pipeline depth [Paper 24.1], split-wordlines [Paper 24.7], improved logic design [Paper 24.7] lead to >30% improvements in speed performance. Power management at both the system and circuit levels substantially improve leakage current, with very little impact on speed performance. A dual-core microprocessor [Paper 5.1] utilizes selective activation techniques to power up <1% of the memory to save power. A register file [Paper 24.7] applies compensation keepers to additionally extend leakage reduction.

The techniques described above are enabling lower energy per operation and higher operating frequencies. This will lead to higher performance for high-power server applications, as well as better mobile consumer devices. The 2x increase in integration afforded by the feature size scaling from 90nm to 65nm will lead to substantially higher functionality. These presentations at ISSCC 2006 will provide a first glimpse of the nature of the next wave of more advanced electronic consumer products.

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# UWB TRANSCEIVERS

So you've got your new plasma TV. Would you rather tear up walls and floors to run new cable or would you rather beam the images wirelessly from a box in your closet? If your choice is the latter, new developments to be presented at ISSCC 2006 in February will bring that dream a step closer!

Video images, large files, downloaded movies, and digital photographs, can easily consume GigaBytes and take minutes – or even hours – to transfer, using currently available technologies. But ultra-wide-band (UWB) technology can increase data rates roughly ten-fold. So, the entire wireless industry is feverishly working on technology that can deliver this promise.

In just one year, the state-of-the-art in UWB has evolved from providing proof-of-concept building blocks to presenting a complete UWB system crammed onto a single microchip. Such, complete RF transceivers for UWB will be presented by Infineon [Paper 6.5] and Realtek [Paper 6.6] at ISSCC in February. Implemented in low-cost fine-line CMOS technology, the chips can transmit and receive data at up to 480 mega bits per second.

Time marches on: The days of houses littered with wires are numbered!

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# A NEW BREAKTHROUGH IN FLASH-MEMORY BIT COST

At ISSCC 2006, Saifun Semiconductors will introduce, for the first time, a 4-bit-per-cell Flash memory product. The same NROM technology used to incorporate 2s bit per cell is now allowing this dramatic density-increase technique, by doubling the bit count per memory cell to a total of four. Targeted for mass-storage applications, such as digital still cameras and MP3 players, this now revealed 1Gb device enables a true cost-reduction breakthrough.

Novel developments in circuit design and with internal read and write algorithms, together with a simple low-cost 0.13µ NROM process technology has made a 4-bit-per-cell product a reality.

Details of these developments will be revealed at ISSCC 2006 at the San Francisco Marriot in February.

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# ADVANCEMENTS IN FLASH MEMORY REDUCE DOWNLOAD TIME AND SIMPLIFY SYSTEM DESIGN

Flash-memory developments are keeping up with the unprecedented demand for low-cost mass storage solid-state non-volatile-memory solutions for portable communication and entertainment devices. As will be revealed at ISSCC 2006 in San Francisco in February, ST Microelectronics has developed a 4Gb NAND-Flash memory that reduces memory-system download time over 50%, achieving 36MB/s. To simplify memory-system design, the ST Microelectronics engineers have embedded an error-correction scheme into a monolithic NAND-flash memory. Previously, error- correction algorithms were typically implemented at the system level. At a minimum overhead cost, a very powerful 5-bit error correction scheme has been implemented, in which five bits can be corrected within a selected group of bytes, either 16 bytes, 512 bytes or 2K bytes. Typically memories with embedded error-correction solutions have single-bit correctors. To minimize overall bit cost, the 4Gb NAND-Flash devices utilize multi-level storage techniques, allowing for the storage of 2 bits of data in a single NAND-Flash cell.

Such are the system-on-a-chip (SoC) solutions to many problems, old and new, characteristically revealed at ISSCC in February.

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# FLASH MEMORY CONTINUES TO DRIVE DOWN BIT COST WHILE IMPROVING PERFORMANCE

As will be reported at ISSCC 2006 in February [in Paper 7.7] Toshiba Corporation has developed an 8Gb NAND flash memory on an advanced 56nm process lithography. The design incorporates enhancements in Multi-Level design techniques. Multi-Level storage allows for one physical memory cell to store more than one bit of data, effectively reducing the memory-cell area. For 2-bits-per-cell, as in the Toshiba case, the effective reduction of cell area is by a factor of 2.

Combining the 56nm process lithography with Multi-Level storage techniques results in the smallest-ever memory-bit size, and chip area, to date. The 8Gb NAND-flash memory is well-suited for mass-data- storage applications, such as high-resolution digital still cameras and portable digital music players. New circuit-design techniques have been used to improve programming-throughput time by over 50% of that of commercially-available Multi-Level NAND Flash Memories. Details of these developments will be revealed at ISSCC 2006 at the San Francisco Marriot in February.

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# DECA-DATA RATE SDRAM

System-I/O performance has outpaced memory-core performance. To improve effective bandwidth, data from memory is accessed in large chunks at the relatively slow cycle time of the memory core, and, then, time-multiplexed onto high-frequency I/O. But, High-Speed I/O systems can suffer from transmission errors due to spurious noise or pathological data patterns. Cyclical Redundancy Checking (CRC) can be used to detect these errors, but requires extra bits to be inserted into the data stream. These bits can be transmitted via extra pins, or added to the data burst. Although adding bits to the burst reduces the number of wiring connections, it creates non-binary burst lengths, causing "bubbles" in a binary-length bit stream wasting potential bandwidth.

To minimize the lost bandwidth created by bubbles, a presentation to be given at ISSCC 2006 (Paper 8.1) proposes a "Deca-Data-Rate" I/O system, transmitting data in one 10bit burst per one clock cycle which eliminates bubbles in the bit stream. To support the non-binary burst, the authors propose a penta-phase PLL to divide the system clock into 5 equal phases. Core performance is addressed through a combination of known techniques, including the use of a "twin cell" to store data differentially, shortened word-lines, and direct sensing.

It is anticipated that these innovations will enable higher performance multimedia systems, enhancing gaming and audio-visual entertainment. Error correction will allow the system to operate at higher frequencies while improving reliability and product lifetimes. This work raises the bar for DRAM performance, as one grows to expect from developments reported at ISSCC.

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# TCAM FOR INTERNET APPLICATIONS

High aggregate network traffic requires high-speed Internet-Protocol (IP) address- lookup tables and efficient packet classification that minimize power during search operations.

At ISSCC 2006, new tree-AND TCAM array architecture will be reported [Paper 8.7] leverages the use of don't-care bits in the table to implement an improved segmented search-line topology. A 1.1ns search time with 0.35fJ/bit search energy is estimated, corresponding to 4x improvement in the speed x energy product, over past world record.

Another range-matching TCAM cell and array architecture, presented at ISSCC 2006 [Paper 8.6] facilitate compare operations, while a search line charge recycling improves data-storage efficiency by 2.5x compared to conventional TCAMs, at the same time, reducing search-line power to 40% of that of a precharged TCAM. This TCAM realizes viable large-scale packet-classification applications in an economical way.

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# GIGABIT WIRELESS AND AUTOMOTIVE RADAR AT MILLIMETER WAVE FREQUENCIES

The allocation of several gigahertz of bandwidth for short-range wireless communications at 60GHz offers a broad range of opportunities and challenges for next-generation gigabit wireless- communication systems. Such high bit rates are becoming a necessity due to the emergence of broadband high-quality video- and audio-applications, as well as high-speed home and enterprise networking. The migration to higher mm-wave frequencies will facilitate the integration of more functionality in silicon, and allows for spatially-reconfigurable communication systems which can reuse bandwidth in a dynamic and more-efficient fashion. At ISSCC 2006, Paper 10.3 will demonstrate an integrated receiver-transmitter pair operating at 60GHz in silicon, showing the highest level of integration at this frequency. This is achieved through careful design and modeling of active and passive components at mm-wave frequencies. The system is designed to transmit and receive at rates above1Gb/s over several meters.

Millimeter-wave silicon ICs can also enable low-cost beam-forming automotive radar at 77GHz that will substantially improve the safety and reliability of next-generation cars. This will facilitate features such as self-parking, collision avoidance, preemptive brake boosting, low-visibility driving aids, and autonomous cruise control, in both low- and high-end cars. Successful demonstration of a phased- array system in silicon, with on-chip antennas, will make such luxuries a reality. The propagation challenges at higher frequencies are overcome by using phased-array multiple-antenna systems on both the receiver and the transmitter.

An integrated phased-array system uses the coherent addition of radio signals in space to generate a focused beam of RF energy that can be electronically steered and pointed in different directions very quickly with much higher signal-to-noise ratio at the receiver, and generating a lot less interference for other users. At ISSCC 2006, Paper 10.1 will demonstrate a successful implementation of a fully-integrated phased array with on-chip antennas, in silicon. The integration of the antennas with the rest of the transceiver eliminates the only remaining high-frequency electrical connection to the chip, making it the ultimate fully-integrated communication system in silicon.

As cost reduces in automotive applications, small self-contained radars with built-in active antennas will ultimately lead to revolutionary games and home robotics.

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# (THERE IS) FIBER IN YOUR FUTURE!

Communication using light signals along optical fiber holds great promise to lower costs for all data transport over both short and long distances. The huge bandwidth and favorable physical characteristics of optical fiber beg to be exploited : In telecom networks, transmitting high-data-rate signals over long distances becomes practical; Within computer systems, high-capacity interconnects, free from electromagnetic interference and awkward bulky copper cables, is enabled by parallel optics. But, of course, practical details limit cost-effective commercial solutions. At ISSCC 2006, in February, several advances in the practical art of sending and receiving optical signals will be presented. Inevitably, such advances will lead to exciting new const-effective telecom services and higher-performance computer systems.

A technology will be described by Luxtera [Paper 13.7] which promises to dramatically reduce the cost of optical interconnects by monolithically integrating both photonic and electronic components in a standard SOI CMOS process. Existing optical transmitters and receivers are expensive modules built from separate optical and electronic components. The technology to be presented integrates, in a standard process used for ordinary PCs and microprocessors, all of the pieces needed to transmit and receive optical signals. Since everything is in one piece of silicon, there is no mechanical assembly needed in modules and this leads to lower cost. But, combining optical and electrical components creates a new design challenges. For example, an optical modulator will be described which requires the matching of velocity of electrical waves and optical waves in a combined waveguide. Also, a WDM multiplexor/demultiplexor will be described which uses a similar structure to calibrate optical-path lengths to improve channel separation in an array wave-guide. Without this on-chip calibration, the manufacturing yield of this MUX/DEMUX would be very low, leading to high cost.

A 10Gb/s burst-mode limiting amplifier will be described by NTT, Atsugi, Japan [Paper 13.9]. The application is burst-mode receivers for passive optical networks (PON) to bring high-speed data connectivity to home. Currently, data rate for PON systems is 155Mb/s and the next generation is 1.25Gb/s. This work represents another huge leap in data rate to 10Gb/s. The benefit of PON systems is they allow many users to share one optical fiber as it goes back to the telephone-company central office. So, since the hardware is shared, there is a lower cost per user. However, users must take turns talking on the shared fibers, and their message bursts must be captured quickly by the central office. This burst-mode receiver must handle both large and small signals from users near and far. This is very challenging. The device that will be discussed extends the dynamic range between large and small signals by a factor of five beyond the results obtained by the same group last year. In order not to waste time between message bursts, it is necessary to quickly receive the signals. This device provides valid data in less than one nano-second, which is a thousand times faster than currently installed GE-PON, and 40 times faster than next-generation G-PON.

A 10Gb/s transceiver chip for the XFP optical module standard will be described by Analog Devices, Wilmington, MA [Paper 13.1]. This new optical-module standard is multi-use, embracing a range of protocols and data rates, with the intent of ending the balkanization of these optical interfaces, and concentrating the volume of possibilities into fewer component types with attendant reduction in cost. The receiver portion of this chip eases the task of the host system by removing jitter from signals, thus allowing lower-cost components to be used. Similarly, the transmitter removes jitter created by the host system – including the inevitable dispersion from transmission lines on printed-circuit boards – to create a remarkably-low-jitter output. This dramatic jitter filtering is enabled by a proven dual-loop DLL/PLL clock recovery architecture: This is the first use of this architecture at 10Gb/s.

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# ULTRA-WIDE-BAND (UWB) ENABLES HIGHER-DATA-RATE PERSONAL-AREA NETWORKS

Ultra-wideband (UWB) wireless technology has the potential to revolutionize the way information is shared in the home or office. Over short distances, UWB can deliver transfer rates greater than 100Mb/s with equipment that is low-power, low-cost and requires little or no administration. An added advantage of UWB transceivers is that they can co-exist with WiFi and other narrowband networks.

At ISSCC 2006, Sony will present the world's first, UWB transceiver that supports distributed control of up to 64 terminals in an ad-hoc (self-configuring) network. Its Direct Sequence Spread Spectrum (DSSS) technique delivers sufficient bandwidth to handle today's heavy multimedia and data traffic. Look for such systems in your multimedia-supply shop soon!

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# RADIO FREQUENCY IDENTIFICATION (RFID) TAGS BASED ON ORGANIC SEMICONDUCTORS PRINTED ON PLASTIC

Few technologies will have a more dramatic impact on the electronics and consumer industries than organic semiconductors in the next few decades. Instead of fabricating transistors and circuits within and onto semiconductor substrates, such as silicon, using costly high-temperature processes, organic integrated circuits (ICs) can be directly printed onto polymers — the same way a magazine article is printed on paper. As the technology for such printing improves, and the cost decreases, it is conceivable that such circuits will be manufacturable at a cost of less than one cent per chip.

With the availability of such low-cost ICs, the consumer-electronics possibilities are virtually endless. One of the most prominent applications will be to replace consumer-product bar codes with plastic circuits that transmit product identification (ID) by way of radio-frequency (RF) transmission. For example, consumers will experience automated checkout lines in grocery stores, where products in a shopping cart will be automatically registered as the cart passes by a radio-transceiver scanner. As advances in the performance and integration complexity of low-cost plastic ICs continue, it will be possible to use them for functions far beyond what is possible with a bar code, such as continuous product monitoring using sensors.

Several such exciting advances of organic semiconductor circuits will be introduced at the International Solid State Circuits Conference (ISSCC 2006) that will be held at the San Francisco Marriott Hotel, February 5-9, 2006. Two presentations, from Poly IC of Erlangen Germany and Philips Research of Eindhoven, The Netherlands, will describe, for the first time organic RFID transponders which operate at a 13.56MHz frequency – the defacto standard for item-level RF identification. These batteryless plastic smart-tags offer a viable replacement for bar codes. The presentation by Philips will demonstrate, as well, a 64-bit tag, the most complex organic transponder reported to date.

As RFID tags continue to incorporate more “intelligence,” it will be possible to use them for functions far beyond what is possible with a bar code. As a sample of what is to come, in this same session at ISSCC 2006, researchers from the University of California at Berkeley will describe the integration of vapor sensors with an organic circuit to construct an “electronic nose” that can be used for continuous monitoring of food products, such as wine, to detect spoilage.

Although the capabilities of these RFIDs and organic semiconductors are quite impressive, the eight presentations in this Organic-Circuits session at ISSCC 2006 will demonstrate that the best is yet to come for this nascent technology.

## Key Points

- RFID tags operating at 13.56MHz providing low-cost item-level identification, are destined to replace bar codes.
- Inductive-coupling-powered integrated circuits printed on plastic materials will encourage disposable electronics.
- Organic circuits and sensors for monitoring products will substantially change the processes of delivery, inventory management, and labeling of consumer goods.

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# BRAILLE E-BOOKS

Books on tape or transcribed Braille books represent the current state-of-the-art in publishing for the blind. Though a tremendous assist for the blind, the delay in publication, as well as the expense of publication, means that sighted people have access to newspapers and the latest best sellers, well in advance of their blind counterparts. Text-to-speech conversion provides one means of more speedy access to information but recent advances to be reported ISSCC 2006 promise direct electronic publication of text to "Braille paper".

This advance may make feasible e-books and Braille newspapers that can update themselves in seconds from any electronic text source. This represents a speed increase of more than an order of magnitude over that of the "Braille sheets" previously reported. The development of an organic 5- transistor SRAM and back-gate bias to counteract the changing device characteristics comprise the important advances in making these future products feasible for the blind.

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# ULTRA-SMALL RFID CHIPS ARE COMING!

Radio-frequency identification (RFID) technology is expected to provide "bridging" information between the real world and the virtual world of the Internet. For this to be possible, RFID-tag cost must be reduced. In addition, RFID devices will need to be smaller, have increased data rates for shorter transaction time, embed larger memories to store more information, and include more functionality. Thinner chips are also needed if RFID tags are to be attached to paper media and other small goods. The major applications include supply-chain tracking, ID cards and security, counterfeit protection, and theft protection. Many more applications will be triggered by lower cost and additional functionality.

Three contributions to ISSCC 2006 at the San Francisco Marriott in February, will describe major advances in this field. Hitachi and Renesas, Japan, will present a newly-developed RFID chip operating at 2.45 GHz that is ultra-thin (7.5μm, or more than 10 times thinner than a sheet of paper!) and ultra-small (0.15mm x 0.15mm). It is fabricated in a 0.18μm SOI CMOS technology to reduce the device cost, and increase its mechanical reliability.

Previously, most RFID tags stored only their unique tag ID number. Now, researchers at Fujitsu Laboratories, Kawasaki, Japan will present an FeRAM-based tag with rewritable memory that can store more information, enhancing system performance, security, and cost-effectiveness.

Data rates usually range from some kb/s up to a few hundreds of kb/s. However, some emerging applications, such as national identity cards or multimedia, require larger data files to be downloaded and this implies higher data rates in order to keep an acceptable transaction time. At ISSCC 2006, CEA-LETI will present an innovative RFID architecture a enabling 3.4 Mb/s data rate at 13.56 MHz.

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# RF MEMS AND BAW FOR LOW-POWER WIRELESS COMMUNICATIONS

Wireless-communications systems require high-quality passive resonators for frequency synthesis and signal filtering. They have traditionally been implemented by LC components or surface-acoustic-wave (SAW) resonators. But, LC resonators usually offer only limited quality factor, whereas SAW devices are not appropriate for integration on the silicon chip. Recently, micro-electromechanical systems (MEMS) and bulk-acoustic-wave (BAW) devices have emerged as an alternative technique for implementing high-quality-factor resonators and filters. They can advantageously be integrated together with the electronic chip for achieving a higher level of integration.

Three contributions to ISSCC 2006 at the San Francisco Marriott in February, will describe advances in this field. Cornell University, Ithaca, USA, will present a MEMS filter operating at 425 MHz and eliminating the need for bulky off-chip components in the radio front-end.

CSEM, Neuchâtel, Switzerland, will present an innovative combination of BAW with active CMOS circuits achieving a very-low-power radio front-end for Bluetooth applications.

The same group, together with the LAAS-CNRS and CEA-LETI, France, will demonstrate 5.4 GHz BAW resonators integrated above an RF IC. This approach, allows achieving higher integration, better performance, and potentially lower cost for WLAN applications.

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# ARRESTING A SERIAL (LINK) KILLER

It's a small world, and getting smaller. Nowhere is this truer than in circuit-board real estate where Gb/s serial links are rapidly replacing traditionally-employed parallel links. Well-known examples include the switch from PCI to PCI-express on PC motherboards, and from ATA to SATA for hard-disk drives. This wave is also sweeping over the memory-interface world where the FB-DIMM standard looks to replace the entrenched DDR-2 interface in compute-server applications. A limiting factor in making the switch to serial links is the development of low-power and low-area clock and data recovery. In addition, fiber-to-the-home (FTTH) applications using passive-optical networking require extremely fast-locking clock- and data-recovery circuits.

This year at ISSCC 2006 reflects the importance and breadth of this issue by dedicating an entire session [Session 18] to this vexing problem. The work to be presented includes a 25Gb/s clock- and data-recovery unit occupying only 0.09mm$^2$ and consuming less than 100mW and a clock- and data-recovery and retiming circuit for next-generation fully- buffered DIMM (FB-DIMM) that has 3x the sensitivity and 1/3 the lock-time demanded by the current standard. Additionally, the session highlights circuit techniques and architectures that expand the performance of traditional clock- and data-recovery designs.

And so, optics is leading to faster and faster local-, inter- and intra-system communications,

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# SILICON AUDIO ICS ROCK YOUR WORLD!

Electronic entertainment devices - such as the iPod MP3 player - continue to enchant consumers worldwide. The ability to carry a vast inventory of musical selections and play them on-demand using a wafer thin player is truly and extraordinary demonstration of the power of silicon IC technology and design.

One disadvantage of most audio players is the fidelity and limited audio power output. Audiophiles crave high-power audio amplifiers because the dynamic range in modern digital recordings exposes the flaws in conventional audio systems at even moderate power levels. Apart from the power to reproduce deep bass notes, low distortion must also be achieved for a fully-digital audio signal path so that a feedback loop between the loudspeaker and signal source is not required.

Engineers at Texas Instruments in collaboration with researchers at the Technical University of Denmark will unveil a Class-D audio IC at the upcoming ISSCC in February 2006 with extraordinary power output capability and very low levels of open-loop distortion. This new chip can produce 240 Watts of audio power into a 4 Ohm load with less than 0.1% total harmonic distortion (THD+N). The output current capability of up to ±18 Amperes is unprecedented in a single chip audio amplifier, so overcurrent sensing is built into the IC to protect it from potential meltdown due to a short circuit.

The input to the chip is a pulse-width modulated digital audio signal that is then amplified to the output. A simple L-C filter reconstructs the analog audio signal at the loudspeaker. By carefully designing the control signal sequence to the digital power amplifier, the maximum power of the new design is doubled compared to existing open-loop audio amplifiers of this type.

This chip will allow manufacturers to further shrink the size of their audio equipment such a car stereos, home theater systems or portable music players without sacrificing efficiency or fidelity compared to much larger systems.

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# THE BREAKTHROUGH WIRELESS SOCS

Mass-consumer market wireless applications set strict requirements on cost, dynamic range, power consumption, and the number of external components used in the system. As described at earlier ISSCC meetings, these constraints have already been applied to Bluetooth and 802.11b/g chips, already reported. This year, at ISSCC 2006, we will see these trends being applied to many other wireless standards including WLAN and ZigBee. As such, many of the most-integrated solutions are implemented in submicron CMOS technologies which allow the full integration of the analog/RF and digital functions on the same die. These highly-integrated low-cost low-power ICs open the door for the application of wireless ICs to many new embedded and non-embedded applications, and ultimately to a seamlessly-connected world. WLAN-enabled printers, cable modems, set-top-boxes, digital cameras, cellphones, and game consoles, are just a few examples of integration of WiFi in various types of consumer electronics. At the same time, the intelligent home will extensively utilize ZigBee-based wireless networks to enhance the quality of life. The high level of integration of these systems-on-chip changes the economics of wireless solutions, and enables the continued price reduction of wireless-enabled consumer electronics.

At ISSCC 2006, at the San Francisco Marriott, in February, [Paper 20.2], will present the most- integrated 802.11a/b/g SoC published to date. There are many architectures to achieve such a system. The authors utilize a sliding-IF super-heterodyne architecture which eliminates one of the on-chip phase-locked loops required in traditional super-heterodyne radios. This SoC includes a multiband RF front-end, analog, ADCs, DACs, PHY, MAC, a processor, and power-management functions in a single CMOS die. This receiver achieves sensitivity numbers similar to others previously published, but using multichip and less-integrated solutions. The transmitter is capable of transmitting -4dBm. The die occupies an area of 44.6 $mm^2$.

In Paper 20.6, at ISSCC 2006, the authors present one of the most integrated ZigBee solutions ever published. The 5.77$mm^2$ die contains a direct-conversion receiver, and a direct-modulation transmitter, the required ADCs, voltage regulators, and all necessary digital functions, including the synchronization and modulation/demodulation processes. Using new architecture and circuit techniques, the authors have been able to reduce the power consumption in receive mode by 50% of that in previously published solutions. At the same time, an excellent receiver sensitivity of -102dBm is achieved.

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# GREEN COMPUTING: CHARGE-RECYCLING LOGIC FAMILIES EXCEED 1GHZ OPERATION FREQUENCIES

Power consumption of modern high-speed microprocessor chips has now become a critical design constraint. Not only does increased power consumption lead to higher operating costs as a result of increased energy consumption, it also becomes more and more difficult to keep the processor chips cool enough for reliable operation. In modern data centers containing hundreds or thousands of computers, it can be a major engineering challenge just to supply power to this dense collection of high-power computing systems, while keeping them cool at the same time.

In current microprocessor designs, most of the power is dissipated as current is drawn from the voltage supply in order to charge wires and other capacitive loads on the chip. Current then flows to ground when it is necessary to discharge these wires. As microprocessor frequency has steadily increased, the rate of charging and discharging has also increased proportionately, and ever higher circuit densities have also led to increasing power densities. Techniques have been proposed which would allow recovery of some of this charge (instead of dumping it to ground when wires are discharged). However, in the past, these techniques have typically only worked at relatively low frequencies, and required special off-chip components which limited their practicality.

Two presentations at ISSCC 2006 at the San Francisco Marriott in February, will describe charge-recycling circuit techniques which work at frequencies in excess of 1GHz, using integrated on-chip components. One presentation will report that up to 60% of the energy used during each clock cycle can be recycled for use during the next cycle, while the other presentation will describe a scheme which operates at clock frequencies up to 3.5GHz. Techniques such as these may be the wave of the future, as microprocessor designers seek new and creative ways to cut down on power consumption. Thus, future microprocessors may lend new meaning to the word “recycling”.

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# HIGH-PERFORMANCE GRAPHICS FOR MOBILE APPLICATIONS

Advanced-3D-graphics hardware is being widely incorporated into multimedia devices such as mobile phones, personal digital assistants (PDAs), and portable multimedia players (PMPs). Portable systems increasingly demand high-end graphics performance with limited power consumption all at low cost.

This year, at ISSCC 2006, researchers from the Korea Advanced Institute of Technology (KAIST) will describe a 2.5-billion floating-point-operations-per-second graphics processor supporting the latest graphics standards. The chip can process 3D-geometry data at a rate of 120 million vertices per second, more than three times faster than previous processors. The chip consumes about half the power of conventional parallel-processing solutions.

Chips such as this, which offer cutting-edge performance with low power consumption, will enable a new generation of games. Future games will demand potentially-photorealistic graphics on personal- entertainment devices, portable set-top boxes, and cell phones. Beyond games, next-generation graphics chips will be integrated into near-future consumer products such as high-end televisions and high-resolution automobile displays.

You will see better, soon!

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# ULTRA-LOW-POWER VIDEO COMPRESSION FOR MOBILE APPLICATIONS

Video compression will be widely adopted for mobile applications such as mobile phone, PDAs, digital cameras, and 3G phones. Most mobile devices require ultra-low-power to extend battery lifetime. New video standards have higher compression ratios that demand higher computational complexity. Therefore, reducing power consumption in such systems is crucial.

At ISSCC 2006, in February, National Taiwan University will present an MPEG-4 encoder consuming less power than all the previous designs. One way power is reduced is through a two-dimensional data sharing scheme that dramatically reduces the memory-bandwidth requirement. As well, National Chung-Cheng University will present a low-cost video decoder for HDTV.

Conference attendees will see chips that will enable future mobile-video applications. Lower power consumption, lower cost, and higher performance will lead to the emergence of mobile video systems.

Seeing will be believing!

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# BATTERIES THAT LAST FOREVER!

Has your mobile phone run out of battery when you are about to call your wife and say you are going to be late for dinner? Well, if Prof. Lal from Cornell University has his way, you will not be able to use that excuse in a few years! The research from Cornell combines benign radioactive material with an integrated miniature MEMS cantilever and circuits to convert nuclear energy to electrical energy. The half life of the reported energy source is about 100 years. The breakthrough that will be presented (Paper 23.1) at ISSCC 2006 by the group from Cornell is that the energy-conversion efficiency is over 30%. This is ten times more efficient than previously reported results from the same group.

The work reported generates 1 to10 microwatts of peak power from 1 to 10 milliCurie of benign Nickel isotope. Nickel-63, is a beta energy source with a maximum penetration depth of less than 10 micrometers, making it easy to shield. Nickel-63 is also resistant to flaking, an important safety property making it easier to handle during manufacturing. Measurements show that the energy source can provide about 20 nanowatts of continuous power for low-power sensors or up to 40 microwatts of peak power for burst-mode computation and communication.

While this is not enough to power your mobile phone today, with energy consumption of mobile systems continuing to reduce with Moore's law, you may be able to carry a mobile phone that will never run out of battery, in the future. Additionally, while this technology may be convenient it also raises the question of proper disposal of used radioactive materials. It is unclear if this radioactivity-based energy source, will stay in niche controlled applications or has the potential to enter the mainstream market. Only time will tell! Until then, you are safe with your excuses!

This and other emerging technology and architecture topics will be presented at ISSCC 2006, at the San Francisco Marriott in February.

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# GOT SPEED?

We live in a world where faster is always better. If you have the need for speed and happen to be in the semiconductor industry, you should pay attention to two presentations at ISSCC 2006. These presentations (23.4 and 23.5) from Japanese researchers demonstrate fast, yet energy-efficient, data communication concepts.

The first, presented by Professor Kuroda from Keio University enables high-data-rate communication between chips that are three-dimensionally stacked, without the need for expensive through-silicon vias. In the presentation from Keio University the communication between three dimensionally stacked chips happen via inductive coupling. In 2 square millimeter area the chips use 1024 data transceivers with a per-channel data rate of 1 Gigabits per second. The high density is achieved by using 4-phase time division multiplexing to reduce cross-talk, resulting in a negligible bit-error rate. The energy efficiency of the communication is 3 picoJoules per bit. The resulting solution provides an aggregate data rate of 1 Terabit per second, and consumes 3 Watts. This work was done in collaboration with NEC and the University of Tokyo.

The second presentation, from NEC, introduces a new approach for realizing high-speed optical interconnects on silicon chips. This concept uses nanophotodiodes on silicon with extremely low parasitic capacitance (less than 10 atto-Farads) enabling robust communication at very-high frequencies. The results demonstrate 5 Gigahertz clocking with promise of up to 20 Gigahertz. The developers will also discuss how the silicon nanophotodiode can be used for wavelength-division multiplexing and low-voltage electro-optic modulators for on-chip and off-chip optical communications.

This and other emerging technology and architecture topics will be presented at ISSCC 2006, at the San Francisco Marriott, in February.

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# SINGLE-CHIP CMOS QUAD-BAND GSM/GPRS RADIO

The worldwide subscriber base for cellular services is growing steadily, and is expected to exceed 1.5 billion by 2007, making it the largest market segment for the semiconductor industry. Today, cellular services for voice communications are primarily based on 2G systems, such as GSM and CDMA. Of the two, GSM is the most popular worldwide cellular standard in use today, with over 75% of the total cellular market. With the rising demand for data services, emerging 2.5G and 3G systems, such as EDGE/GPRS and UMTS/CDMA2000, will play an increasingly important role in enabling multimedia services with feature-rich handsets.

To support enhanced functionality in current and future multimedia handsets, RF cellular ICs must provide small-form-factor low-power solutions, while meeting stringent system-level requirements such as sensitivity and linearity. High sensitivity improves the reception of an on-going call, as well as extending the distance range of the handset. High linearity improves the quality of calls in areas with high subscriber density. Existing cellular phones are implemented in multiple-chip sets based mainly on bipolar and SiGe technologies. While current SiGe/bipolar chip-sets achieve adequate system performance, they do not lend well to high levels of integration at low cost.

The increased integration inherent in deep-submicron CMOS can enable the integration of complete RF cellular transceivers as well as digital signal processing in a single chip to dramatically reduce power, for extended battery life, while maintaining adequate system performance. Existing CMOS solutions for RF transceivers are also based on multiple chips. However, several single-chip solutions have been announced recently. Last year, ISSCC 2005 showcased the first fully-integrated quad-band GSM transceiver in a mature low-cost 0.18μm CMOS process, that had the best sensitivity/linearity and power-dissipation tradeoff on the market at the time, for CMOS transceivers. This year, ISSCC 2006 will feature the first true system-on-a-chip (SoC) for quad-band GSM/GPRS, that integrates not only the RF but also all the analog and digital processing required by the handset. This GSM/GPRS SoC achieves the high levels of integration by using a 0.13μm CMOS technology. This single-chip radio achieves a sensitivity of less than -110dBm, and demonstrates that a true SoC solution for high-performance cellular ICs, such as GSM, can be integrated in a low-cost deep-submicron CMOS process.

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# DOWN WITH POWER!

Over the past few years, consumers have taken unprecedented control of the technology in their lives. Camera phones in their hands, videos at their fingertips, 24/7 Internet access, the consumers' appetite for information and entertainment seems to know no bounds. At the same time that consumers demand new features and greater performance, they also expect unlimited mobility and long battery life. Behind the scenes however, engineers have been facing a major roadblock on this information super-highway: unlimited demand for limited power.

Faster wireless downloads and seamless video, for example, demand smarter ways to quickly deliver more power in ever smaller spaces. Processors the size of a postage stamp can, in a fraction of a second, demand as much current as an entire home. At ISSCC 2006, at the San Francisco Marriott in February, two presentations will describe how a novel linear regulator [Paper 29.1] and transient-limiting circuit [Paper 29.7] tackle this problem. A slightly different direction is taken by Paper 29.3. Here a new level of on-chip integration with high-density capacitors is employed to reduce the power that a state-of-the-art processor needs to get the job done. As consumers demand more power-greedy features, they also want their camera phones, video players, etc. to last longer between battery charges. In Papers 29.4 and 29.5 engineers apply novel power-management techniques to reduce OFF-state power and extend battery life for cellular phones.

Despite these innovations, until engineers better understand where the power is going and when, they will continue to be surprised by new power roadblocks. At ISSCC 2006, two working presentations directly address this issue; An on-chip voltage and temperature auto-detection circuit [Paper 29.6] and a unique infrared system [Paper 29.2] allow unprecedented views into a working world smaller than a human hair. This advance in analysis will allow electrical engineers to continue to deliver more and more for less and less.

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# SILICON CHIPS PROMISE TO HELP PEOPLE SUFFERING FROM SPINAL CORD INJURY

Half a million people in the US and almost one million worldwide cannot move properly anymore after being injured in an accident. This is a consequence of damage to their spinal cord, preventing brain- control signals from reaching their limbs. New cases of spinal-cord injury occur at a rate about 10,000 every year in the USA.

To help those suffering from such impairment, researchers have been exploring the possibility of capturing the commands produced in the brain as small electric signals, and using them to control mechanical limbs, electric vehicles, personal computers, or other electrical appliances. Several electronic circuits implanted in the brain and able to record, process, and send outside the body to access brain control signals have been reported in specialized conferences and literature in the past decade. Still, the different tasks of recording, processing and transmitting have yet been integrated in a single, silicon chip.

But, at ISSCC 2006, in February, researchers from the University of Utah will present the first integrated chip able to record signals from the brain (using 100 electrodes), locally reduce the quantity of data, apply a threshold algorithm, and send the data outside the body through a radio link. The chip, that dissipates 1.5mW, is powered using inductive coupling, like that employed in a power transformer. Also, at ISSCC 2006, researchers from Stanford University will present their innovative approach to creating a brain-interface chip that is as much energy-efficient as possible.

These silicon chips can be considered to be the first step in improving the quality of life of people suffering from spinal-cord injury, enabling them to control mechanical and electrical systems under direct control of their brain. Related chips could be used in the future to provide some visual sensation to the blind, or to help those who suffer from drug-resistant epileptic seizures.

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# SILICON FOR BIOSENSING

Current biosensing approaches routinely use fluorophore labels and large optical-readout instrumentation. Attaching fluorophore labels to biomolecules often complicates and limits the ability to detect multiple bio-analytes and target DNA.

At ISSCC 2006 in February, Paper 30.6 presents a novel label-free approach to detecting biomolecular reactions. The researchers use a MEMS cantilever beam coated with probe biomolecules. Upon detection of a conjugate bio-molecule, the cantilever deflects in proportion to the amount of detected bio-analyte. After optical sensing degree of deflection of the deflected cantilever beam, a small electric field is applied to dissociate the reacted biomolecules from the sensor surface, preparing it for the next detection step.

This biosensing approach has been implemented in a wireless technology and has been applied to the repetitive detection of cardiovascular-event-related proteins (CRP).

**Key Points:**

- MEMS cantilever biosensor implements label-free biomarker detection.
- Reusability of the biosensor has been demonstrated.
- Wireless readout of biochemical reactions may enable future wearable biomedical microsystems.

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# GIGA SAMPLING-RATE ADCS FOR PORTABLE EQUIPMENT

High-speed access to magnetic and optical data storage and UWB (Ultra-Wide-Band), WPAN (Wireless-Private-Area-Network) communications for portable equipment are in high demand by consumers. These applications require giga-sampling-rate Analog-to-Digital Converters (ADCs), which are quite power-hungry, to enable signal processing in the digital domain. Despite of the improved performance in conversion rate and resolution, reducing the power consumption is always required, because it directly affects battery life.

Lower power-supply voltage is key, since it effectively reduces the power consumption. This, however, has not been sufficiently achieved in conventional (>0.13um) technology. Applying nanometer technology to analog circuits is a challenge: new analog design techniques are required to realize the technology benefit of deep-sub-micron lithography.

This year, ISSCC features very-high-speed ADCs, establishing the latest benchmarks for ADCs in the Giga-Samples/second (GS/s) region. A 4b 1.25GS/s for 2.5mW ADC will be presented in (Paper 31.1) ISSCC 2006. A new design technique, to overcome mismatch caused by fine pitched elements will be presented.

A 6b 1GS/s 55mW ADC will also be presented (Paper 31.2). Here, a new offset-canceling technique enables implementation of minimum-sized transistors in the analog portion. As a result, 1GS/s 55mW operation is achieved, providing much-lower power consumption than conventional ADCs.

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# MOBILE TV

TV on a mobile phone is not new. Analog TV tuners have been available in mobile phones in several countries over the years. However, the technology never took off because of power and performance penalties inherent in analog-TV broadcasting and reception. Digital-broadcasting technologies such as DVB-H, DMB, ISDB-T, and MediaFLO solve these technical problems. A recent Credit-Suisse First-Boston forecast[1] estimates that 150M handsets per year will ship with digital-TV-reception capability by 2009, representing a new $1B opportunity for semiconductor manufacturers, and many times that for handset manufacturers and mobile-phone operators. In some countries, these services are already commercially available today, while many other countries are completing field trials and preparing for commercial introduction during 2006. The first six presentations in the session on "Mobile TV" at ISSCC 2006, represent a snapshot of the recent advances in tuner integrated circuits for all of these mobile digital-TV broadcasting technologies. Mobile seeing will (lead to) (ec) static believing!

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[1] "I want my, I want my M(obile)TV," Sandbox Vol. 61, Credit Suisse First Boston Equity Research, May 25, 2005.

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# ADVANCES IN WIRELINE TEST AND DIAGNOSIS

Wireline communication requires many building blocks to meet the ever-increasingly insatiable desire for higher data rates. Testing wireline communication systems at these high data rates is a challenging task, primarily due to the precision required and speed of operation. Advances in semiconductor technology and IC design have led to significant developments in on-chip jitter measurement and high-speed pattern generation.

Picosecond-clock-jitter measurement techniques enable on-chip diagnosis for wireline systems with more stringent jitter requirements. High bit-rate pseudo-random bit-stream (PRBS) pattern generation is essential in evaluating the performance of future wireline communication links operating at 100Gb/s and beyond.

At ISSCC 2006 at the San Francisco Marriott, in February, attendees will get a glimpse of the latest developments in high-speed test and characterization of high-performance wireline links.

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