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On the Design of a 4-bit BCD Adder

Reen Paul[1], Shiby.B[2]

Assistant Professor, Dept. of ECE, College of Engineering Munnar, Kerala, India [1]

PG Student [VLSI and Embedded Systems], Dept. of ECE, College of Engineering Munnar, Kerala, India [2]

ABSTRACT: Be it addition, subtraction, multiplication, division or exponentiation the quiddity of computation lies in the 1-bit adder cell. It extends its essence onto designing of myriad processors which elicits its relevance in the electronic platform. While the size of the electronic gadgets shrinks it is equally important to ensure that its speed also satisfies the constraint of High Speed. When we say less area and high speed as the factors to be achieved it is inevitable that we concentrate on the core cell, which we call the adder cell. With the ever rising financial and commercial applications the BCD adder is considered whose performance parameters such as area, power and critical path delay are estimated. The performance of the BCD adder implemented with a Ripple Carry adder and a Carry Skip adder is studied with respect to the two foremost design aspects of reduced area and high speed. The simulations were carried out in Cadence Virtuoso Tool at 90nm technology.

KEYWORDS: Binary Coded Decimal (BCD) Adder, Ripple Carry adder (RCA), Carry Skip adder.

I. INTRODUCTION

Be it telephone billing, electricity billing or water billing we find decimal data everywhere. These curfew the widespread financial and commercial databases containing more and more of decimal data. Moreover financial applications do not tolerate approximate representation of fractional decimal numbers and the corresponding decimal software running on top of the underlying binary hardware makes the entire process all the more slower. This fact has never changed even with the advent of binary data.

The 4-bit BCD adder comprises of two 4-bit full adders and a carry detection logic circuit in its conventional architecture. The two 4-bit full adders are basically Ripple carry adders where the carry output of one full adder cell is propagated onto the succeeding full adder cell at each computational stage. This forces each 1-bit full adder cell to wait for the carry propagation from its preceding cell to compute the sum.

In the conventional design the Ripple carry adder is the protagonist of the logic design. With its simplified structure, the Ripple carry adder occupies less area and performs fast operation. But it is an irony that this fast operation is limited to lower order bits and finds itself unsuitable for higher multiple bit computations. The necessity of carry propagating from preceding stages serves the reason.

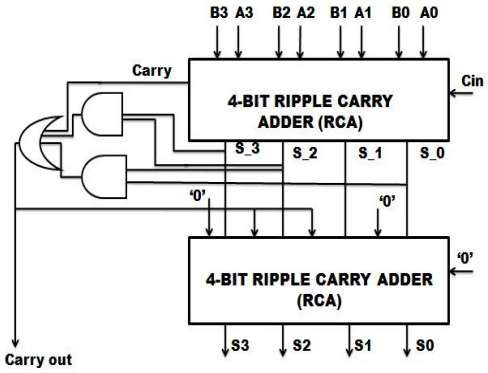

Fig. 1: Conventional 4-bit BCD adder

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The modified BCD adder proposed in this paper aims to work on two prior design aspects of area and speed without any compromise on the power consumption. Hence it is evident that proper selection of the 1-bit adder cell is equally important to serve the need.

The remaining sections of the paper are organized to provide more insight into the design. Next section gives a review on the conventional 1-bit full adder cells namely the 16T, 14T, 10T, SERF adder, 8T and the 6T adder cell followed by a description on the BCD adder. Brief information on fast adder structures is postulated in section III. The simulation results of various adder cells compared against the conventional 28T adder cell at 90nm is depicted in Results and Discussions. The concluding summary of the analysis and the implemented BCD adder is brought about in Conclusion.

II. LITERATURE REVIEW

When we say BCD adder it is the 1-bit adder cell that is pivotal. The full adder designs reported in literature are in profusion, which is based upon different logic styles like, static CMOS, dynamic, transmission gate, or pass transistor logic. Each has got its own pros and cons.

The full adder cell realization of the circuit using 16 transistors [1] as depicted in Fig.2 operates with full output voltage swing but consumes significant amount of power and has more delay compared to other adders having less transistor count which makes it undesirable for compact VLSI applications.

With the goal of further minimizing the number of transistors, XOR and XNOR circuits based on pass transistor logic were used and as a result the 14T full adder circuit [1] as portrayed in Fig.3 was designed. Researchers reveal that this design offers better delay and power performance compared to 16T full adder but it suffers from the threshold loss problem of approximately 0.4V.

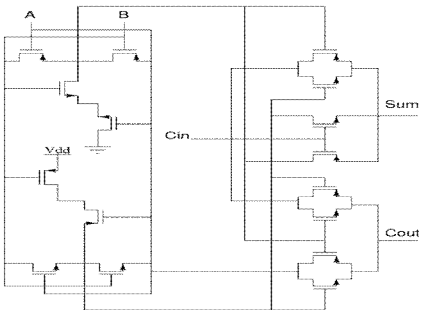

Fig. 2: 16 Transistor full adder cell

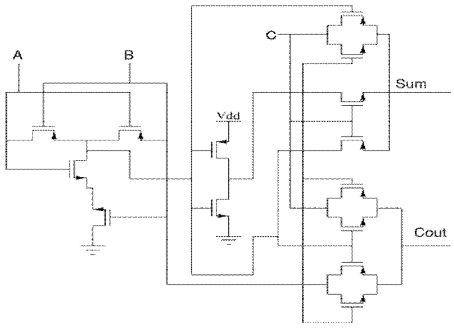

Fig. 3: 14 Transistor full adder cell

The SERF adder [2] comprising of 10 transistors, with no direct path to ground abates power consumption. The reapplication of the charge stored at the load capacitance to the control gates and the elimination of a direct path to ground portrays the SERF adder as an energy efficient design. On the contrary due to multiple threshold loss issues this design cannot be cascaded at low power supply voltage. Fig.4 portrays the SERF adder cell.

The further designed 10T full adder [2] (Fig.5) uses inverter-based 4T XOR gates in its design and shows remarkable improvements in power and delay. It also reduces the silicon area. This reveals better performance than the SERF adder cell. The drawback of this circuit is that it also suffers from threshold loss problem of 0.35V.

The three transistor XOR gate forms the 8T adder [2] cell. It acquires less silicon area. The design of 3T XOR gate is shown in Fig.6. The Sum output function is formed through a cascade of 3T XOR gates while Carry is realized using a wired OR logic in accordance with the equation given. Figure.6 depicts schematic of the above discussed 8T adder cell formed using 3T XOR gate.

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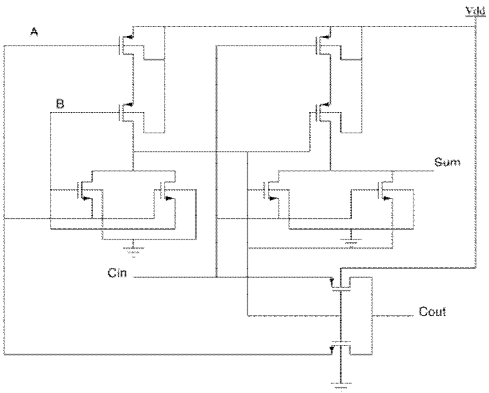

Fig. 4: SERF adder cell

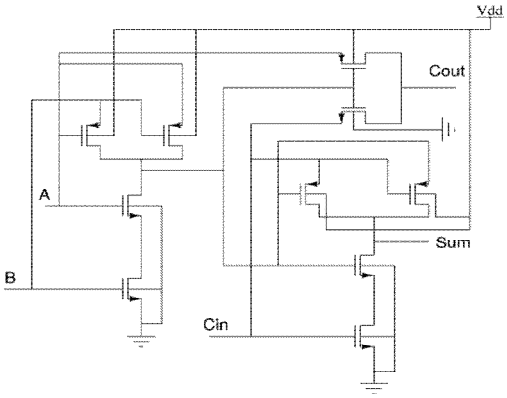

Fig. 5: 10 Transistor full adder cell

To prove that area can still be reduced we have the 6T adder [3] designed with mere three multiplexers. Each multiplexer is designed using only two transistors as shown in Fig.7. The multiplexer can be used as both XOR and XNOR gate. In peer designs of 10 transistor adder the XOR/XNOR gates were designed using four transistors which increased the area. The 6T adder uses three multiplexers in its design making it more area efficient. In the present day world all VLSI devices need to be compact as portability is a main design consideration. This 6T adder is apt for such applications.

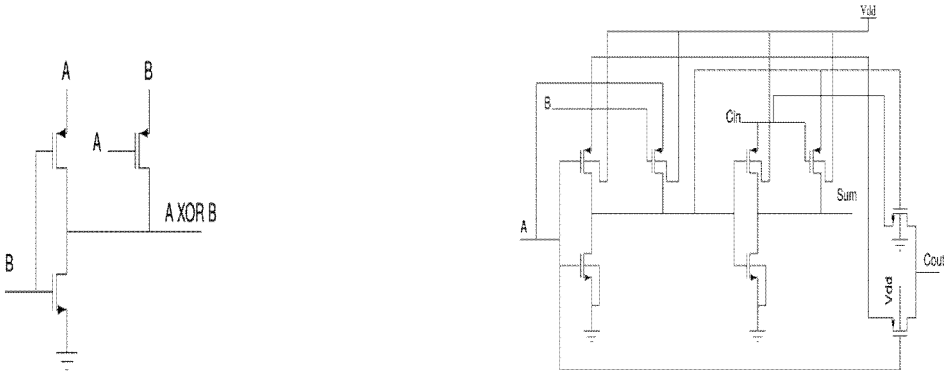

Fig. 6: Eight Transistor full adder cell

The output of MUX1 signal is used as select signal in MUX2 where ‘Cin’ and ‘Cinbar’ are input signals. MUX2 generates the Sum output. The output of MUX1 is also used as select signal for MUX3 where ‘Cin’ and ‘A’ are input signals. The output of MUX3 is carry signal Cout. MUX1 is used to generate (AB) signal. It is used as control signal in both MUX2 and MUX3. MUX2 is used to generate Sum signal and MUX3 is used to generate carry signal.

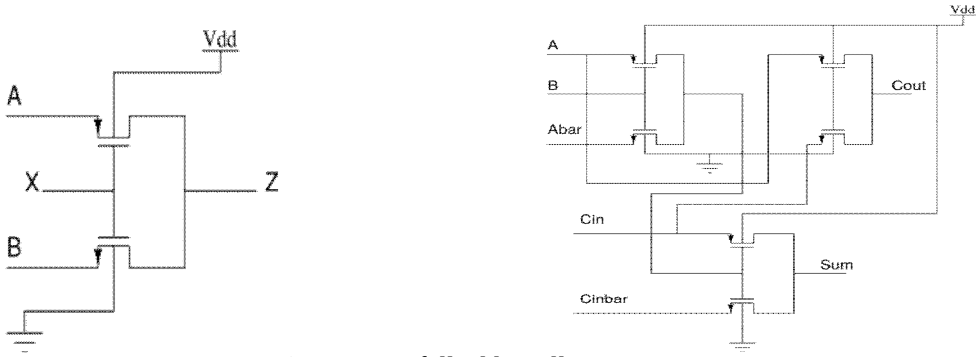

Fig.7: 6 Transistor full adder cell

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We find that many researchers have worked on the BCD adder considering various design aspects. Aiming to abate power consumption and to achieve Low power and Low voltage BCD adder, the author in [4] suggests methods of Clock Gating and Power Gating. The obtained results prove good when compared against the conventional peer designs. Shirazi, et. al., proposes a Redundant Binary coded Decimal (RBCD) adder [5] performing a three step addition operation. Initial stage involves conversion of the BCD input into RBCD. The result of the addition is obtained using the RBCD adder in the second stage followed by conversion into BCD format in the rear stage. As the conversion of RBCD adder result back into the BCD format requires carry propagation the Delay caused due to this becomes highly dependent on the length of the input operands.

III. ALL ABOUT ADDER STRUCTURES

A. *Ripple Carry Adder*

The Ripple carry adder is the basic building block of the BCD adder. Constructing an n-bit ripple carry adder requires n full adder cells.

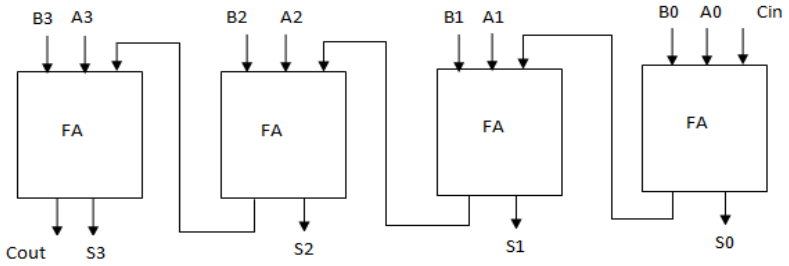

Fig. 8: 4-bit Ripple carry adder

In this design, LSB of the sum bit is produced by the LSB's of two numbers a0 and b0. Carry of these LSB bits is propagated to the next cell. c0 which is initially zero is applied as a third input to the full adder. This carry is computed at each adder cell and propagated to the succeeding stages. This issues the ripple carry adder a compact structure (O (n)) [6] but delay increases linearly (O (n)) with increase in the number of bits making it unsuitable for higher order operations.

B. *Carry Look-Ahead Adder*

In contrast to the ripple carry adder, the carry look-ahead adder (Fig.9) computes the carry signal in parallel rather than rippling through based on the equation given below.

$$C_i = \overline{G_i}.\ \overline{P_i.\ C_{i-1}} \qquad (1)$$

Here, G_i and P_i are defined as complementary generate and propagate signals [7] for the i^{th} bit. At the i^{th} bit a carry gets generated when the G_i term is true whereas a carry-in gets propagated to the carry-in of the $i+1^{th}$ bit when the P_i term turns true. Equations dictated below illustrates the conditions before said.

$$\overline{Gi} = \overline{Ai.Bi} \qquad (2)$$

$$Pi = Ai \oplus Bi \qquad (3)$$

XOR-ing of the carry-in calculated from the previous two bits and the propagate signal of the current two bits is carried out by the sum generator; hence the name carry look-ahead adder.
Sum equation is given by,

$$Sum = P_i \oplus C_{i-1} \qquad (3)$$

C. *Carry Skip Adder*

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Establishing a compromise between a ripple carry adder and a carry look-ahead adder the carry skip adder divides the words to be added into blocks. Within each block the sum and carry bits are produced using ripple carry adders. By skipping over groups of consecutive adder stages the Carry Skip Adder reduces the delay due to the carry computation.

- If each Ai # Bi in a group, then need not to compute the new value of Ci+1 for that block; the carry-in of the block can be propagated directly to the next block.
- If Ai = Bi = 1 for some 'i' in the group, a carry is generated which may be propagated up to the output of that group.
- If Ai = Bi = 0, a carry will not be propagated by that bit location.

The concept of a carry-skip adder is to detect if in each group all Ai # Bi and enable the block's carry-in to skip the block when this happens as shown in fig.10.

The linear growth of delay with the size of the input operands is abated by allowing carries to skip across blocks of bits, rather than rippling through them in contrast to the ripple carry adder. This design proves area efficient (O (n)) and exhibits circuit delay of O (√n) [6].

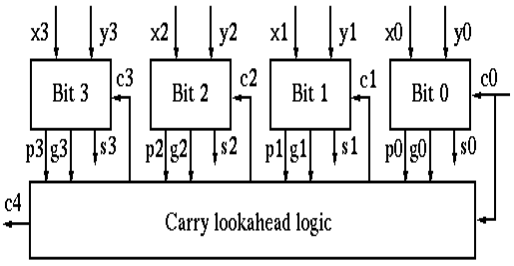

Fig. 9: Carry Look-Ahead adder

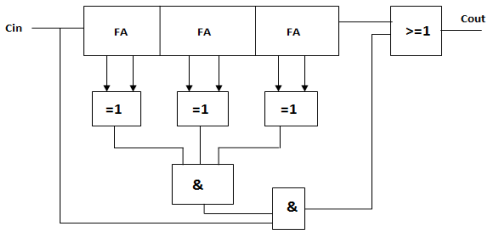

Fig. 10: Carry Skip adder

IV. IMULATION RESULTS AND DISCUSSIONS

The comparative study and analysis was carried out in Cadence Virtuoso tool at 90nm technology. The pivotal design aspects such as transistor count, Average power, Critical path delay and Power delay product are estimated and studied. Aspiring to design a BCD adder that is compact in structure, we have opted for the 6T adder cell whose performance is studied.

TABLE I: SIMULATION RESULT OF 1-BIT ADDER CELLS

Metric	28T adder	SERF adder	10T adder	8T Adder	6T adder
Avg.Power (W)	2.55x 10^{-7}	0.47x 10^{-7}	1.79x 10^{-7}	6.56x 10^{-5}	0.69x 10^{-7}
Delay (ns)	500	550	200	600	400

When compared against the conventional 28T adder cell, the 6T adder elicits 72.56% improvement in average power consumed, 20% less delay, and 78.57% reduction in the number of transistors.

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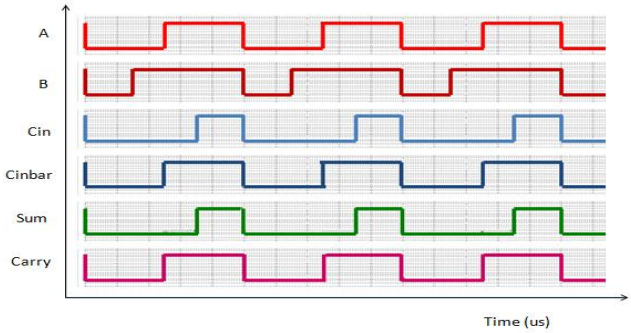

Fig. 11: Waveform of 6T adder cell

As evident from the block diagram of the BCD adder, the primary building block of the 4-bit BCD adder is the 4-bit ripple carry adder. Hence, the 1-bit 6T adder cell is built into a ripple carry adder whose results are studied. The tabulated values proves that the ripple carry adder built from the 6T adder cell is 89.33% power efficient, 20% improvement in delay with 78.57% area efficiency.

TABLE II: SIMULATION RESULTS OF RIPPLE CARRY ADDER

Metric	Conventional RCA	6T RCA
Area (Transistors)	112	24
Avg.Power (uW)	8.671×10^{-7}	0.925×10^{-7}
Delay (ns)	500	400

With Area as the focus, delay and power as indispensable design aspects we find that 6T adder elicits desired performance suiting the need of the hour. The simulation results comparing 4-bit BCD adder designed with 6T adder against the conventional design is tabulated. The proposed design proves 83.64% power efficiency, 37.3% improvement in delay with 76.19% area efficiency. The simulation results are tabulated in Table III.

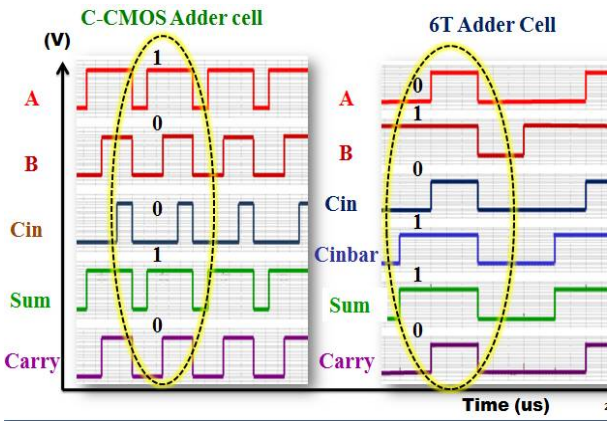

Fig. 12: Waveform of 4-bit Ripple carry adder

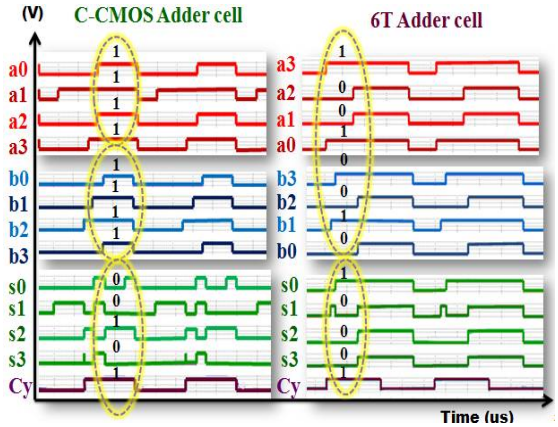

Fig. 13: Waveform of 4-bit BCD adder

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TABLE III:SIMULATION RESULTS OF BCD ADDER

Metric	Conventional RCA	6T RCA
Area (Transistors)	231	55
Avg.Power (uW)	35.85	5.364
Delay (ns)	500	313.5

V. CONCLUSION

With increasing demand for decimal arithmetic hardware support in financial and commercial applications the BCD adder finds its place in today's market. Being an arithmetic tool speed is a factor which we can never give off at a compromise and thereby we focus on speed and compactness. With an effort to meet the technology trends of portable compact VLSI circuits we considered the heart of digital circuits which is the adder. Myriad designs based on varied XOR – XNOR gates namely the SERF adder, 10T adder, 8T and 6T adders were analyzed and compared against the conventional 28T design in terms of Area, Average power, Delay and Power delay product. Power efficiency is achieved through various low power techniques already reported in literature. We therefore focus on area and speed parameters. Simulations proved that the 6T multiplexer based adder showcases area and delay efficiency without compromise in power performance. The performance of the 4-bit BCD adder built on the proposed 6T adder also proves efficient when compared against the conventional realization. On mitigating the issue of carry propagation in ripple carry adder the critical path delay can be improved which is left over for future work. The BCD adder being a mathematical tool holds speed more important than compactness for which we propose the carry skip adder as suggested in this paper.

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