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Emerging III-V Semiconductor Compound Materials for Future High-Speed and Low Power Applications: A Review and Challenges

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ABSTRACT: High mobility III–V semiconductors, along with high-k gate dielectrics, are projected to be key ingredients in future complementary metal–oxide–semiconductor technology. Among these, In0.53Ga0.47As has been intensively studied for their advantages in high electron mobility over their Si-based counterparts. In0.53Ga0.47As metal–oxide–semiconductor field-effect transistors (MOSFETs) have been demonstrated to provide large drive current density. In order to continue the scaling of silicon-based CMOS and maintain the historic progress in information processing and transmission, advanced device structures and advanced materials are required. A channel material with high mobility and therefore increase injection velocity can increase ON state current and reduces the delay. Currently, strained-Si technology is used for designing high performance MOSFETs. However, looking into future high mobility III-V materials can offer several advantages over even very highly strained Si.

KEYWORDS: MOSFET, injection velocity, Electron transport, Mobility .

I. INTRODUCTION

Due to tremendous advances in lithography, the semiconductor industry has followed Moore's law by shrinking transistor dimensions continuously for the last 30 years. The big challenge in VLSI is that continued scaling of planar, silicon, CMOS transistors will be more and more difficult because of both fundamental limitations and practical considerations as the CMOS transistor dimensions approach tens of nanometers. To address the scaling challenge, both industry and academia have been investigating alternative device structure and alternative materials, among which III-V compound semiconductor Materials as a promising candidates for future logic applications because their light effective masses lead to high electron mobility's and high on-currents, which translates into high device performance at low supply voltage. Due to outstanding electron transport properties and high mobility are very actively being researched; group III–V compound semiconductors as channel materials for future highly scaled CMOS devices. The III-V semiconductors can be in the form of different binary, ternary, quaternary and even higher-order compounds mixing different number of III and V group elements. High electron mobility and conductivity in III-Vs give rise to high transistor drive current and low gate delay, which are very important for high-speed logic application. III-V materials in general have significantly higher electron mobility than Si and can play an important role along with Si in future high-speed, low-power applications. The major advantage of using a III-V quantum-well field-effect transistor as a logic transistor is that it can be operated at very low supply voltage (e.g., 0.5 V), and hence, lower power dissipation while still achieving very high speed compared to other emerging high-mobility materials, such as, carbon nanotubes and semiconductor nanowires.

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II. RELATED WORK

A. USE OF III-V COMPOUND MATERIALS IN VLSI DEVICES:

III–V semiconductors, especially InAs, have much higher electron mobility's than Si and therefore considered as promising candidates for n-channel materials for low power CMOS logic applications. Combined with the 3-D structure that enables the gate-all-around (GAA) geometry for superb gate electrostatic control, III–V nanowire (NW)MOSFETs are well positioned to extend the scaling beyond Si[1].

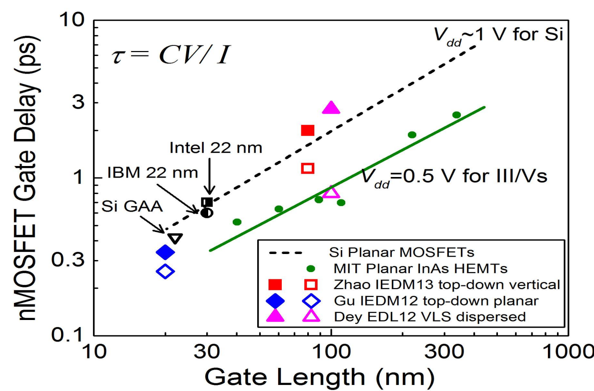

Fig 2.1 :The delays of Si MOSFETs and the state-oftheart planar III–V devices [1]

The simulation results indicate that III–V FETs do not outperform Si FETs in the ballistic regime but deliver very similar performance. However, III–V FETs is one of the most promising candidates because they could operate closer to their airborne limit than Si FETs and therefore provide higherON-state current due to lessperformance squalor from electron–phonon and surfacescatterings[3].

Table 1: Device Performance Parameters For The In0.75ga0.25as And Strained-Si In Single-/Double-Gate Planar FET and Triple-Gate FINFET Configuration [3].

Structure	**Single-gate**		**Double gate**		**Triple-gate**	
Material	InGaAs	Si	InGaAs	Si	InGaAs	Si
SS [mV/dec]	97	91	84	75	69	71
DIBL [mV/V]	234	190	91	93	54	59
I_{ON} [μA/μm]	1033	1196	1747	2020	2490	2629

The interface property ofoxides or insulators on III-V compoundsemiconductors is a very complex problem. Thereasons for these aboveexperimental observations mostly are notwell-understood. A big challenge for material and deviceresearch community to find an excellent dielectricand gate stack on III-V materials in general stillremains [6].

A channel material engineering based investigation hasbeen performed for RingFET architecture. During this courseit is found that for Analog and digital application, GaAsRingFETgives better performance in comparison to silicon.An investigation of tuning oxide for GaAs has also beenperformed. Results reveal that out of three oxides (i.e. SiO2, Ah03, HfO2) HfO2/GaAs gives better performance than othertwo oxides. In addition during investigation it has also beenfound that III-V material suffers less from gate leakage incomparison to Si. Investigation also reveals that high-Kdielectrics material suffers from a serious issue of gateleakage, which is of great importance for device

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reliabilityconcern [7].Finally, III-V materials will need to be integrated selectivelyonto the Si platform. Significant challenges remain formonolithic integration of III-Vs on Si, such as, (i) the anti-phaseboundary defects, (ii) thermal mismatch issues, and (iii) Lattice mismatch problem. III-V materials will notreplace Si; rather, they will need to be integrated onto Si as thechannel material for future high-speed, low-power logictransistors [14].

For III-V compound semiconductors to become applicablefor future high-speed and low-power digital applications, therefore III-V compound is need to be integrated onto large silicon wafers. Aunified, vigorous heterogeneous integration scheme of III-Von silicon will allow high-speed, low-voltage III-V basedtransistors,while avoiding the need for developing large diameter III-V substrates. Besides transistor applications,successful integration of III-V on silicon can give the opportunities for integrating new functionalities and featureson silicon, such as integrating logic circuit, optoelectronic (Photo detector) andcommunication platforms on the same silicon wafer.However, heterogeneous integration of III-V on siliconimposes many significant technical challenges because of thelarge lattice mismatch between the two materials [15]

Fig.2.2 shows Both InSb and InGaAs quantum-well field effect transistors(QWFETs) show significantly improved transistor energydelayproduct.

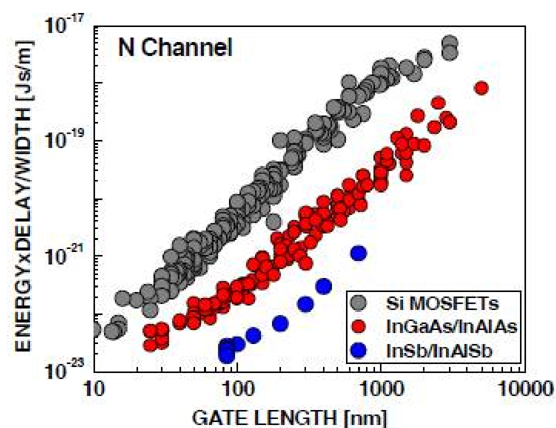

Fig:2.2- Comparison of Energy-delay product of n-channel InSb and InGaAs Material [15]\

III-V compound semiconductors also have the advantageof a lattice matched hetero-structure material system with awide band gaps and materials. Compared to Sibasedhetero-structures such as Si/SiGe, the III-V heterostructuresallow much better tractability in band structureengineering and thereby device design for both highperformanceand low power applications can be possible. Presently, compound III-V materials are mainly preferred forcommunications system and optoelectronic device applications. They havenot received serious consideration for digital applications inthe past years, due to the lack of high excellence native oxides. However, with the end of Sidevice scaling approaching, and non-traditional materialsbeing increasingly incorporated into mainstream Sitechnology, III-Vs are receiving renewed attention as channelmaterials for VLSI logic applications [19].

It is critically analysed the componentsof source/drain (S/D) resistance in InGaAs n-MOSFETswith Ni-InGaAs metal Source/Drain. It is found that Ni-InGaAs has a low resistivity of 250 µohm·cm in a thickness of Ni-InGaAs(TNi-InGaAs) of down to 4 nm. Contact resistance between thecontact pads and Ni-InGaAs (RC) is found to be the most dominantcomponent of source/drain (S/D) resistance in control InGaAs MOSFETs, becauseof the existence of Ni oxides [22]-[23].

The first demonstration of InAsFinFETswith fin width Wfin in the range 25–35 nm, formed by inductivelycoupled plasma etching. The channel comprises defect-free,lattice-matched InAs with fin height Hfin= 20 nm controlledby the use of an etch stop layer incorporated into the deviceheterostructure. For a gate length Lg= 1 µm, peak transconductancegm,peak= 1430 µS/µm is measured at Vd= 0.5 Vdemonstrating that electron transport in InAs fins can matchplanar devices [28].

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Between Si and III–V compound semiconductors, theIn0.53Ga0.47As trigate shows 1.5 times lower total threshold voltage valuemaking it a favorable candidate for Si replacement. A MonteCarlo study of 6T SRAM cell with fin width or body thicknessvariation show that the 3σ value of read static noise margin[3σ (RSNM)] is least in SRAMs with rectangular Si trigate. This work also shows that a 6T SRAM cell at different VCC showsthat a Si trigate has Vccmin below 0.4 V [29]..

B. USE OF III-V COMPOUND MATERIALS IN OPTOELECTRONICS:-

While individual Si MOSFET have become faster by faster, theoverall computational speed is limited by the electrical interconnects.Optical interconnect can possibly provide a solution to thecommunication tailback by replacing electrical wires with fasteroptical waveguides. The intra-chip optical interconnects need tobe fabricated and integrated with Si CMOS devices monolithically tomeet the size and density requirements. Current integration schemeis a silicon-compatible electro-optic modulator with an external III-Vlaser light source. Development on Si-compatible III-V process andintegration on Si-substrate will have great impact on the intra-chipoptical interconnect applications[5].

To report the limitations of existing siliconsolid-state photomultipliers (SSPMs), it is developing newphotodetector elements in III-V material AlGaAs. With 80% aluminiumconcentration in the GaAs compound, the material effectivelybecomes a wide band-gap material with a band-gap energyof 2.1 eV. The wide band-gap characteristic and the relativematurity of GaAs material processing make Al Ga As anoutstanding material for developing better SSPMs with reduced dark current. Materials with larger band gaps have a lower limitin the associated thermally generated dark current [9].Silicon hetero-nanowireswith integrated III-V segments are one of the most favourable candidates forinnovative nano-optoelectronics [12].The Monolithic integration of III–V compound solarcell materials and devices with Si substrates as been adriving force in fundamental photovoltaic materials researchfor decades. The chief instigator for this effort is the potentialfor considerable reduction in fabrication costs of high-efficiencyIII–V solar cells by substituting inexpensive large-area Siwafers in place of expensive smaller area Ge and GaAs wafers,which are the customary substrate materials for III–V photovoltaic.Additionally, porting III–V technology to a Si platformwould provide admittance to the worldwide base of Si manufacturing,which is built upon the ideals of extreme scalability, enablingfast production, high volume, and high throughput.However, aside from the economic benefits, integration ofIII–V photovoltaic on a Si platform also provides importantperformance advantages, including twice the fracture robustnessand thermal conductivity at half the mass density versus traditionalsubstrates, making Si substrates ideal for use in bothhigh-specific-power space systems and concentrator terrestrialsystems [13].
It is described the design, fabrication,analysis, and improvement of the GaAsP top solar cell ina three-terminal GaAsP/SiGe tandem solar cell on a silicon substrate.Uncertified GaAsP top cell efficiencies have been improvedfrom 8.4% to 18.4% with bandgap voltage offsets (Woc) of 0.48and 0.31 V under concentration factors of 1 and 20 ×, respectively.This development is made by enhanced III–V material quality,reduced series resistance, and an addition of antireflection layer.Improving the optics, material quality, and fill factor (FF) shouldfurther improve the efficiency of the GaAsP top cell in this tandemstructure grown on an Si substrate [24].

Epitaxially grown III-V compound semiconductors,such as gallium arsenide (GaAs), can provide greaterphotovoltaic (PV) performance due to many gorgeous materialproperties. However, the high cost of growing device-qualityepitaxial materials has prevented their extensive acceptance inglobal applications. In this regard, decreasing thicknesses ofbasic epitaxial materials without negotiating theirphotovoltaic performance is one of conceptually feasible means tolower the cost. Here it is presented a type of thin film GaAs PVsystem with significantly reduced active layer thickness (~200 nm),where dielectric periodic nanostructures and a metallic reflectiveelement are heterogeneously integrated on the front- and backsurfacesof solar cells for nanophotonic light management toenhance the absorption and photovoltaic performance of ultrathinGaAs solar cells [25]-[26].

C.USE OF III-V COMPOUND MATERIALS IN COMMUNICATIONS

Indium phosphide (InP) has emerged in the past decade as the material of choice for thefabrication of ultra-high speed transistors. Due to higher electron mobility and electronvelocity, circuits fabricated using InP-based transistors have shown higherspeeds and lower power consumptions than their silicon analogues. In particular, the InPbasedheterojunction bipolar transistor (HBT) has been recognized as the fastestoperating transistor with a unity current gain cutofffrequency which is typicallyhigher than 200 GHz [10].

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GaN has attracted substantial amounts of attention as a basis for manufacturing high-speedand high-power electronic devices due to its wide bandgap, high electron saturation velocity, andhigh critical breakdown field. In particular, GaN-based HEMT, in the form of Al(Ga)N/GaNHEMT, has been regarded as the next-generation RF power amplifier for wireless communicationand power converter in utility grid applications. Two main problems associated with GaNHEMTs are gate leakage and DC-RF dispersion (also referred to as knee-voltage walkout), whichcan be mitigated by implementing a metal insulator semiconductor (MIS) structure and propersurface passivation, respectively [15].

CHALLENGES IN IMPLEMENTING III-V COMPOUND MATERIAL FOR MANUFACTURING CMOS

TECHNOLOGY:-

Many significant challenges remain to be overcome before III-V materials become applicable for future high-speed, low-power logic applications. These include (i) Investigating a well-matched high-κ gate dielectric on III-Vs, (ii) demonstrating gate length scalability below 35 nm with acceptable ION/IOFF ratio, (iii) improving the hole mobility in III-Vs (CMOS) configuration, and (iv) integrating III-V materials onto the Si substrate.
The main challenges in implementing III-V Materialfor manufacturing CMOS technology are as follows:
First, III-Vmaterials do not have an effective gate stack solution. UnlikeSi, the native oxides of III-Vs have very meager electricalproperties, which make both the thermal and the depositedoxides difficult due to the strain in completelyremoving the native oxide prior to the gate dielectricdeposition. Despite some progress in recent years ,the problem of forming a high-quality gate insulator remainsa significant barrier to implementing III-V for CMOSapplications.
Second, III-V substrates are expensive, delicate and difficultto make in large sizes. Furthermore, from an economics pointof view, the success of any future CMOS technology withnon-Si channels will depend on its compatibility with thepresent Si manufacturing organization. Therefore, methodsessential to be developed to integrate III-V channels on Sisubstrates, which can be possibly attained through eitherwafer bonding or epitaxial growth. However, both methodsare quite challenging due to large thermal and latticemismatch, and the formation of anti-phase domains.
Third, III-V materials do not have a higher hole mobilitycompared to Si. However, III-Vs still have the net mobilityadvantage over Si for CMOS application due to their muchhigher electron mobility, and lightly lower or comparablehole mobility. Nevertheless, a better integration scheme is toutilize III-V for the NFET and Ge for the PFET due to thehigh hole mobility of Ge. In addition, some III-Vs like GaAsare almost lattice matched to Ge. Other issues such as thelow conduction band density of states and the low n-typedoping are also potential problems for III-Vs.Among all these challenges, perhaps an effective gatestack solution is the most imperative[19].
Fourth, The interface property of oxides or insulators on III-V compound semiconductors is a very complex problem. The reasons for these above experimental results mostly are not well-understood. To find an excellent dielectric and gate stack on III-V materials in general a big challenge for material and device research[6].
The heterogeneous integration of compound material III-V on silicon enforces many important technical challenges because of the large lattice mismatch between the two materials [15].

III. **WHAT IS A COMPOUND SEMICONDUCTOR?**

III-V Compound Semiconductor Materials composed of two or more elements is called a compound semiconductor. The III-Vcompound semiconductors obtained by combining group III elements (essentially Al, Ga, In) with group V elements (essentially N, P ,As, Sb).Typical examples of compound semiconductors include gallium arsenide (GaAs), gallium nitride (GaN), indium phosphide (InP), zinc selenide (ZnSe), and silicon carbide (SiC).
Features of III-V Compound Semiconductor Materials :-

- III-V Compound Semiconductor Materials have much higher electron mobility's than Si.
- III-Vs are promising in many applications that getting Moore law. Process and integration development such as gate stack, low resistance contacts, self-aligned process, scaling and particularly the integration on Si substrate will extremely advantage for current III-V applications.
- III-V Compound Semiconductor Materials have ultra-high speed switching at very low supply voltage.

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- These materials provide higher carrier mobility, intensive heat owing capacity and lower noise induced device degradation etc.
- Direct integration of high-mobility III-V compound semiconductors material with present Si based CMOS processing platforms offering a main challenge to increase the CMOS performance and the scaling trend.
- The Monolithic integration of III–V compound solar cell materials and devices using Si substrates has been a energetic force in fundamental photovoltaic materials research.
- The integration of III-V compound semiconductor materials such as GaAs on Si delivers a unique opportunity to combine the advantages of advanced semiconductor materials with silicon technologies.
- Future work for high-performance Integrated Circuits will require the monolithic integration of CMOS and III-V Compound Semiconductor material devices to enhance the performance of current Si CMOS processes through the addition of III-V materials.
- In future a unique III-V on silicon platform will enable optoelectronics III-V devices to be fabricated on silicon substrates.

IV. CONCLUSION

Group III–V compound semiconductors due to their exceptional electron transport and high mobility are very actively being researched as channel materials for future scaled CMOS devices. To keep enhancing the performance of both III–V and Si FETs in the future technology nodes, their sourceand drain regions should be optimized to reduce the contactseries resistance since the overall device performance will beconquered by the contact resistance. Improvement in transistor performance in nm regime likely to require replacement of silicon by new material like III-V compound materialchannel with high-mobility compound semiconductor (III–V) materials.In addition during investigation it has also beenfound that III-V material suffers less from gate leakage incomparison to Si.III-V materials in general havesignificantly higher electron mobility than Si and can play aimportant role along with Si in future high-speed, low-powercomputing. The important potential advantage of using a III-V, A quantum-well FET can be operated underneath very low supply voltage (e.g., 0.5 V), andhence, lower power dissipation can be achieved while achieving very highspeed.In order to implement III-Vs inmanufacturing CMOS technology, we have to overcome thechallenges including an effective gate stack solution andintegration with Si substrate and GepMOSFETs. The best candidates for these Photovoltaic cellsare III–V compound materialbecause of their wide bandgaps (Eg) and near-idealdiode characteristics. Epitaxially grown III-V compound semiconductors on Si substrate,such as gallium arsenide (GaAs), can provide better photovoltaic (PV) performance due to many attractive materialproperties.

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