The 1st

Asia-Pacific Workshop on FPGA Applications

Xiamen, China, 2012

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Title : The 1st Asia-Pacific Workshop on FPGA Applications, Xiamen, China, 2012

Publisher : Terasic Technologies Inc.

ISSN : 2305-9877

Terasic Technologies Inc.

9F., No.176, Sec.2, Gongdao 5th Rd, East District
Hsinchu City, Taiwan 30070
www.terasic.com

Printed in Taiwan

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Contributing Author

Research Pages

Applying Research Outcomes into Innovation and Technology for Better Health Care and Life Quality

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Abstract — The history of medicine can be traced back to the ancient human societies that related to the beliefs which provide explanations for birth, death, and disease. However, the concepts of diagnosis, prognosis, and medical examination were not formed until introduced by ancient Egyptians in Africa (1600 BC), Babylonians in Mideast (2200 BC) and Chinese in Asia (1600 BC). Preventive medicine was also developed in China at that time. During the Renaissance, knowledge of understanding anatomy and the invention of the microscope led to the 'germ theory of disease', the foundation of modern medicine. Now we are in the 21 century, standing on the summit of modern medicine era, which our ancestry had never dreamed of. Our life has already been extended from an average of 25 years in the Stone Age to around 70 years in the 'Modern Age' due to the help of modern medicine. However, we still face to many incurable diseases, such as cancer, AIDS, cardiovascular disease, psychiatric disease... etc., even our technologies in pharmacology, chemistry, physics, biology, medicine and engineering have tremendously improved than before. How to apply our research outcomes into innovation and technology for better health care and quality of life should be our mission and obligation.

Keywords — History, medicine, disease, technology

I. HISTORY OF MEDICINE

If the expectation of human civilization is to have healthily live with longer life, then there is no doubt that the most contributed aspect is the progress of medicine, especially the achievement of preventing the infectious diseases in the first half of the 20th century. The human life expectancy has been extended from the Stone Age of about 25 years to the 21 century's 70 years due to great improvement in medical diagnosis, treatment and the concept of prevention. There are several milestones of the investigations or inventions in the history that result in the modern medicine. Most of investigators won the Nobel prizes. Here I would like to state their contributions along the time line of the progress in medicine in history and the Nobel prizes award since 1901.

A. Microscope

In 1590, two Dutch lens grinders Hans and Zacharias Janssen make the first microscope by placing two lenses in a tube. The invention of microscope leads to discover and evidence the existence of bacteria which have very tiny size with unit in micrometer and can't be seen by eye

or simple glass magnifier. Some of them played major role of causing serious epidemic diseases or plagues in the Middle Age. Many ancient civilized cities such as Athens of Greek in BC 430 and Rome in 262 AC were almost destroyed by black plague. Nearly five thousands people died from it in a single day. In 1348 AC, the epidemic of black plague came back again and killed almost 1/4 to 3/4 population of Europe. The bacterium is now called Yersinia pestis which is a Gram-negative rod-shaped bacterium. It is a facultative anaerobe that can infect humans and other animals. In 1675, Anton van Leeuwenhoek uses a simple microscope with only one lens to look at blood, insects and many other objects. He was first to describe cells and bacteria, seen through his very small microscopes with, for his time, extremely good lenses. This results in the foundation of microbiology; In 1913, Richard Zsigmondy develops the immersion ultramicroscope and is able to study objects below the wavelength of light. He won The Nobel prize in chemistry 1925. In 1931, Ernst Ruska develops the electron microscope. The ability to use electrons in microscopy greatly improves the resolution and greatly expands the borders of exploration. He shares the Nobel prize in physics in 1986 with Gerd Binnig and Heinrich Rohrer who invent the scanning tunneling microscope that gives three-dimensional images of objects down to the atomic level. Although the last two were awarded in the category of physics, they all are frequently applied in the research of biological science.

B. Antitoxic serum and Vaccine

The invasion of bacteria to the body may cause serious disease such as the black plague mentioned above. However, some bacteria may not directly attack our body to cause illness but the released toxin can, such as diphtheria and tetanus. An antibody forms in the immune system in response to and capable of neutralizing a specific biological toxin. If serum contains antitoxins then it can be used to treat diseases caused by corresponding biological toxins, such as tetanus and diphtheria. Adolf Emil Behring was the discoverer of diphtheria antitoxin in 1890. He won the first Nobel Prize in Physiology or Medicine in 1901 for developing a serum therapy against diphtheria and tetanus. Paul Ehrlich won the same honor in 1908 because of developing a mass productive method of diphtheria antitoxin.

The history of vaccine and immunization should begin with the story of Edward Jenner. He performed the world's first vaccination in 1796. Unlike the diseases caused by bacteria, some of the diseases are caused by virus, which size is much smaller than the bacteria. Most range in size from 5 to 300 nanometers. In other words, it can't be observed under microscope. Cowpox is an example. More than 200 years ago, in one of the first demonstrations of vaccination, Edward Jenner inoculated a young English boy with cowpox material from a dairymaid and showed that the boy became resistant to smallpox. Jenner published a volume that swiftly became a classic text in the annals of medicine: Inquiry into the Causes and Effects of the Variolae Vaccine. His assertion "that the cow-pox protects the human constitution from the infection of smallpox" laid the foundation for modern vaccinology. Now there are many different kinds of vaccine to be used to prevent diseases, such as tuberculosis, yellow fever, poliomyelitis, ... etc.

C. X-ray and imaging technology

The discovery of x-ray by Wilhelm C. Roentgen in 1895 opened a door for medical diagnosis. Although it has been over more than 100 years, this technology is still and frequently in use globally. There is no doubt that Roentgen was awarded Nobel prize in physics in 1901. In 1971, about seven decades later, the first x-ray

computer tomography (CT) has been built by Godfrey Hounsfield (1979 Nobel prize winner in Physiology or Medicine) for brain scan at Atkinson Moreley Hospital in London. Soon after that this technology is applied to whole body scan for diagnosis. The major contribution of this technology is to switch a 2D medical image (x-ray film) to a 3D configuration. In 2003, the Nobel Prize in Physiology or Medicine was awarded jointly to Paul C. Lauterbur and Sir Peter Mansfield "for their discoveries concerning magnetic resonance imaging". Although there are many different imaging modalities recently being developed for medical diagnosis, these two are still commonly used in hospital.

D. Physiological signal recoding

This is an aspect that reflects the function of tissue or organ in a fashion of electrical signal. The first evidence of electrical activity in the nervous system was observed by Luigi Galvani in the 1790s with his studies on dissected frogs. He discovered that you can induce a dead frog leg to twitch with a spark. In 18 century, human started to understand the phenomenon of electrical activity in body and found that the body can conduct current. In 19 century, Rudolph von Kolliker and Heinrich Muller found that heart could generate current when they took out a piece of muscle and its connected nerve from one animal and put the other end of the nerve on the heart of another animal, the muscle contracted. In 1878, a tiny electrode was developed to put on an animal heart to measure the current generated by the heart. In 1903, Willem Einthoven developed an equipment that can measure and recode small current when electrodes put on particular places on chest. This is the first noninvasive recoding of physiological signal, called electrocardiogram (ECG), in functional aspect of heart. In consequence, many protocols of measuring physiological signals at different sites of body were developed such as electroretinogram (ERG) for retina, electroencephalogram (EEG) for brain, and many others. Einthoven won the Nobel prize in Physiology or Medicine in 1924. More than one hundred years later, this technology is still in use for clinical diagnosis.

E. Antibiotics

Moving into the 20 century, it seems that many diseases can be prevented and controlled by vaccination and antitoxin serum therapy. However, there still have problems in medicine caused by infection that can't be solved. In 1928, Alexander Fleming found that one of cultured bacteria bottle was contaminated by green mould when he came back from a vacation. He noted that his cultured bacteria (staphylococcus) were swallowed up by these mould observed under microscope. This kind of green mould is called Penicillium which can be found on rotten orange or apple. In addition to this, he also found that Penicillium can have the same efficacy to the other types of bacteria. After purification, he named this new drug Penicillin. Mass production of Penicillin is carried out 10 years later by the help of two chemists Howard Florey and Ernest Chain. Penicillin provides great contribution to wounded soldiers in World War II. In 1945, Fleming, Florey and Chain won the Nobel prize in Physiology or Medicine.

II. CURRENT TECHNOLOGIES IN HEALTHCARE

A. The human genome project

Thanks to the progresses in current technologies such as electronics, computer science and engineering so that the permutation of DNA sequence can be completed within 13 years (1990-2003). Scientists believe that most of the human diseases are related to the genes. If the secret code of gene can be deciphered, then what sector of

genes that related to particular kinds of diseases can be found. This can probably lead to find a therapeutic way to cure the diseases.

B. Stem cell

Perhaps the most important potential application of human stem cells is the generation of cells and tissues that could be used for cell-based therapies. Today, donated organs and tissues are often used to replace ailing or destroyed tissue, but the need for transplantable tissues and organs far outweighs the available supply. Stem cells, directed to differentiate into specific cell types, offer the possibility of a renewable source of replacement cells and tissues to treat diseases including Alzheimer's diseases, spinal cord injury, stroke, burns, heart disease, diabetes, osteoarthritis, and rheumatoid arthritis.

C. Artificial tissue and organ

In last century, progresses in material science (include biomaterials), solid state and electronics (include bioelectronics) result in that many tissues or organ can be permanently or temperately replaced, such as intraocular lens replaces crystalline lens in eye for cataract surgery, cochlear implant for hearing impairment, artificial knee and artificial bone for severe fractures and disease, artificial skin for severe skin burn, ...etc. Currently, research of artificial retina has shown with great progress that a retina chip with 8x8 pixels resolution has successfully implanted in a blind patient, who is diagnosed retinitis pigmentosa (congenital retinal disease). This allows him to distinguish relative large objects such as door, wall and hallway so that he can walk with the help of a cane.

What we expected on the stem cell research is that it can differentiate to particular organ for organ transplant in the future. Before that, the technology of artificial organ or tissue can temperately take place of the functions of these tissue and organ. This is an idea and could come true.

III. THE ASPECTS OF HUMAN LIFE AND QUALITY OF LIFE IN THE FUTURE

The technologies in modern medicine have moved to the summit in the late 20 century, which has already extended human life from 25 years of the Stone Age to 70 years in the 20th Century, we still face to many unsolvable problems of disease such as cancer, AIDS, psychiatric disease, ... etc. Additionally, severe environmental pollution, unexpected weather change, declined grain yield, the pain factor increases compared to the Age without much help of medication. How to overcome these problems is a big challenge of human being in the 21th century in addition to prolong our life.

Research Papers

Implementing Full HD Video Splitting on Terasic DE3 FPGA Platform

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Abstract — This document introduces the design of HDMI Full HD 1080p splitting processor techniques in detail. It also describes how to design the proper DDR2 Multi-Port Controller to prevent the side effects of image processing like flickering and tearing. In addition to this, it shows how the DDR2 Multi-Port Controller gets the best performance, where the DDR2 can operate easily at 200 Hz with a 148.5 MHz Full HD input source, and hence there is no limit number of screen splitting.

Keywords — video split, DDR2 controller, Multi-Port memory controller, ping-pong buffer, TV wall

I. INTRODUCTION

As televisions are entering into the age of High Definition Television generation, HDTV can be separated into 720p, 1080i, and 1080p under the Rec.709 (ITU-R Recommendation BT.709)[1] protocol, where "i" stands for interlaced scanning and "p" stands for progressive scanning. Under a frequency of 60 Hz, a 1080i HDTV can display 30 complete frames a second, and 1080p can display 60 complete frames per second. Hence, 1080p is the most stable and smooth solution.

Under Full HD resolutions (1920 x 1080), the HDMI connector is an integral part of the interface. Under 720p transmission, 1.485 Gb/s is needed to support uncompressed video and audio content. With HDMI 1.0[2], 24-bit video can transfer at a speed of 165 megapixels per second, with the bandwidth reaching up to 4 Gb/s. This not only meets the requirements for displaying 1080p, it also supports 192 kHz sampling, which is able to transmit an 8-channel 24-bit LPCM audio signal as well.

Under HDMI 1.3[3], transfer speeds were increased from the original 4.96 Gb/s (165 Mpixels) to 10.2 Gb/s (340 Mpixels), and color depth was increased from 24-bit sRGB or YcbCr to 30-bit, 36-bit, and 48-bit xvYCC, sRGB, or YCbCr, which results in an output capacity of more than 100 million colors. With the recent development of the HDMI 1.4[4] standard, in addition to increasing the maximum resolution and expanding support for color spaces, 3D formats and even more features were added.

Under the current progress of HDTV and HDMI specifications, simple image splitting has become quite a challenge on hardware design. In order to split images to reach Full HD standards, video processing core design is the focal point. This paper presents the design methodology for HDMI Full HD1080p video splitting, implemented on a DE3 FPGA platform[5] in particular.

II. SYSTEM ARCHITECTURE

The basic HDMI Full HD 1080p block diagram for video processing core design is shown in Figure 1.

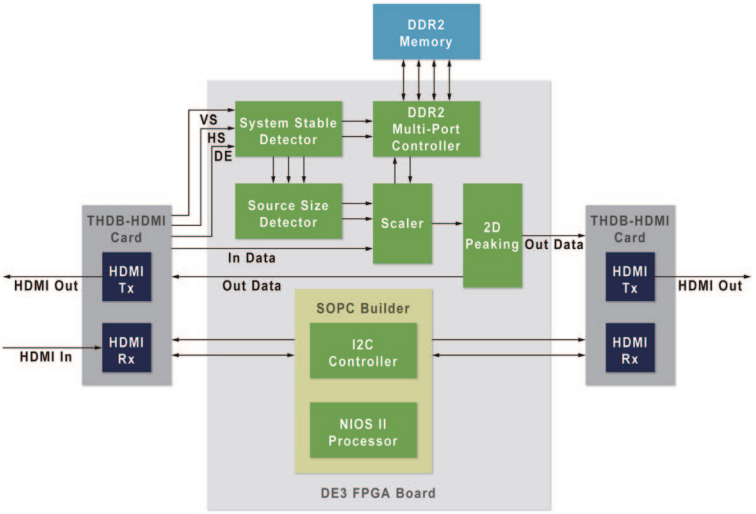

Figure 1. HDMI Full HD 1080p split-screen block diagram

The system receives an HDMI Full HD input, which after FPGA processing, is scaled vertically or horizontally according to the LCD screen. The image is then spanned across two (or four) 1920 x 1080 LCD screens. Figure 2 shows the actual setup of the DE3 FPGA hardware platform along with an HDMI daughter card for input/output, which meets the requirements of HDMI 1.4a.

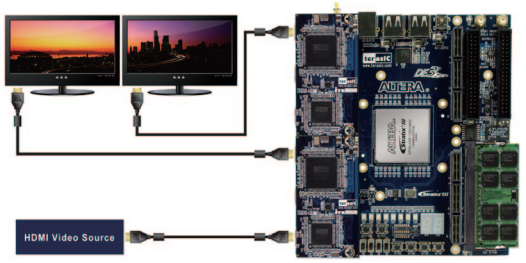

Figure 2. HDMI input/output using DE3 FPGA platform and daughter card under HDMI1.4a

The system is composed of three portions:

- HDMI input/output settings controller
- HDMI control signal generator
- HDMI video streaming processor

III. HDMI INPUT/OUTPUT SETTINGS CONTROLLER

For the first portion, in HDMI input/output settings, the controller core is established via the SOPC Builder in Figure 1. It is built with a combination of the Nios II Processor and I2C Controller, which are in charge of setting and controlling HDMI input/output.

IV. HDMI CONTROL SIGNAL GENERATOR

The second portion is the HDMI control signal generator, which is composed of the System Stable Detector, Source Size Detector, and DDR2 Multi-Port Controller in Figure 1.

A. System Stable Detector

The System Stable Detector is in charge of automatically detecting switching between different resolution sources, so that the whole system can reset to match.

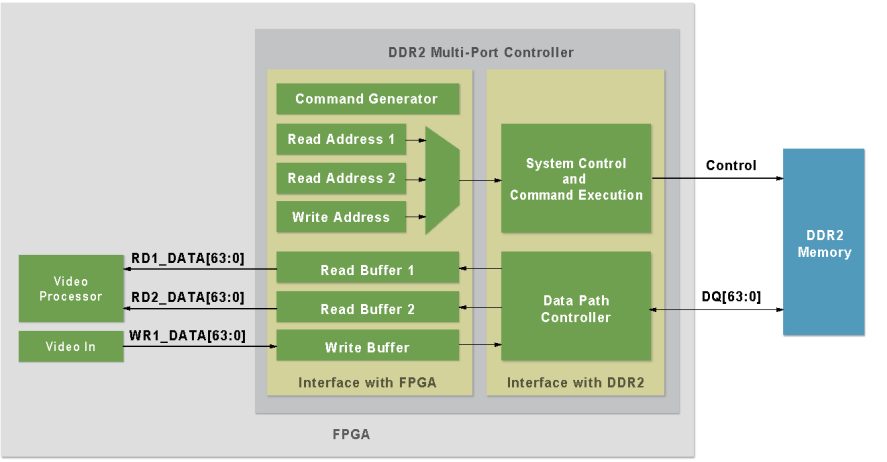

Figure 3. DDR2 Multi-Port Controller block diagram

B. Source Size Detector

The Source Size Detector is responsible for setting the proper scaling factor, frame size, and start position of display according to the ratio of the front-end source and back-end display.

C. DDR2 Multi-Port Controller

The DDR2 Multi-Port Controller is responsible for controlling the frame buffer access as the vertical-splitting mode. The DDR2 memory is set up as ping-pong buffer structure (Figure 4 is an example of vertical-splitting one image into two), utilizing two identical frame buffers. One frame buffer is written, and the other frame buffer is read, which prevents flicker and tearing.

If the screen is vertical split from one frame to two, the DDR2 Multi-Port must be set up as one write port and two read ports. The basic block diagram is shown in Figure 3.

During the writing stage, two starting positions must be identified, one for the top half of the image, and the other for the bottom half of the image, simplifying the read portion of the DDR2 controller architecture. In the design, the timings for the two read ports are equally allocated. As can be seen in Figure 4, only one read port is operation when one line is written, i.e. when the first line is written, only the first line of the top half buffer is read, and when the second line is written, only the first line of the bottom half is read, and so on.

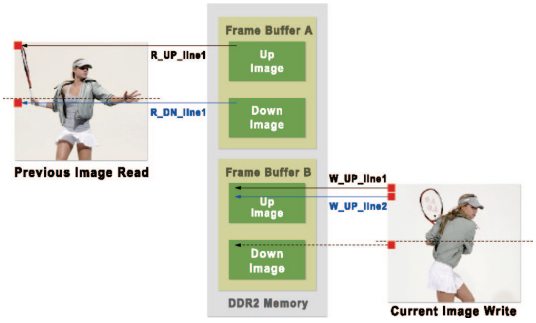

Figure 4. The DDR2 memory forms a ping-pong buffer architecture on the DE3 platform-vertical splitting

As such, the DDR2 bandwidth is allocated for the best performance, where the DDR2 can operate easily at 200 Hz with a 148.5 MHz Full HD input source, and hence there is no limit number of vertical splitting.

V. HDMI VIDEO STREAMING PROCESSOR

The third portion of the HDMI video streaming processor is made up of the Scaler and 2D Peaking unit in Figure 1.

A. Scaler

The Scaler is responsible for adjusting the input video source according to the predetermined-splitting number, either by linear or non-linear scaling up. During interpolation, the more reference points there are, the better quality of resulting image forms. It's better to at least use bi-cubic[6] interpolation. If edge-adaptive can also be considered, the high frequency images will be much clearer.

B. 2D Peaking

The 2D peaking is responsible for increasing the sharpness of the video, as after scale processing, edges appear blurry. It's important to note that if scaling is not performed properly, artifacts such as halos and jagged patterns may appear after 2D peaking operation.

CONCLUSION

The experimental platform is shown in Figure 2, with the DE3 FPGA development kit handling all the functions of receiving and transmitting HDMI. The Sony PlayStation 3 is the input HDMI source, generating a 1920 x 1080 Full HD progressive signal. The FPGA takes the front-end source and partitions it into two images, where it displays them on two separate HDMI monitors. Utilizing the Altera Stratix III 340 kit, with 340,000 logic elements, the experimental platform ran at 148.5 MHz, with the on-board DDR2 running at 200 MHz.

With the above mentioned design methodology, multiple frames (2x2, 2x3, 3x3, 4x4, etc.) can be formed with Full HD. Taking advantage of the re-stackable and modifiable nature of the DE3 platform, any hardware development kit is possible. Figure 5 displays the stacked DE3s and HDMI daughter cards which form a 3 x 3 Full HD HDMI frame split processor. This is suitable for TV Wall applications.

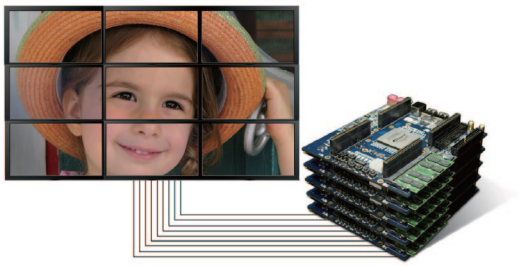

Figure 5. Stacked DE3s and HDMI daughter cards forms a 3 x 3 TV wall

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Design of Large-scale Wire-speed Multicast Switching Fabric Based on Distributive Lattice

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Abstract — Ensuring high quality of service (QoS) of multicast video stream over a next generation network is a challenging issue, and how to implement the wire-speed multicast with hardware logical support in the network nodes of every hierarchy is a key solution to achieve high QoS multicast. Currently, the multicast packets are processed in this way, in which they are copied and then scheduled by ports, lastly, sent respectively. But this approach cannot ensure the high QoS in real-time applications. Moreover, the traditional hardware solutions can`t achieve large-scale scalability well owning to their own bottlenecks. In this project, using distributive lattice theory we have constructed a wire-speed multicast switching fabric based on a multi-path self-routing fabric structure which we developed previously, and implemented it on an Altera StratixIV FPGA chip. Also, we have investigated how the structure is used in large scale multicast switching fabric and designed the signaling system and control mechanism to support the process of self-routing and wire-speed fan-out copy of multicast packets.

Keywords — multicast switching fabric, distributive lattice, Multi-path Self-routing Fabric Structure, FPGA

I. INTRODUCTION

According to a research report [1] published by Arbor company and University of Michigan, the video service becomes the major internet applications. The video stream is characterized by multicast in two ways. One is multiple unicast software scheduling, and the other is wire-speed fanout hardware copy. The former performs poorly in real-time and QoS feature, but, the latter can approve the latency and also achieves excellent performance for multicasting. Therefore, looking for a high QoS multicast solution which can provide hardware logical support in the network nodes of every hierarchy is a key R&D point. Currently, the multicast packets approaches cannot ensure the high QoS in real-time applications because the packets are copied and then scheduled by ports, lastly, sent respectively. Also, the traditional hardware solutions can`t achieve good large-scale scalability. In this paper, using distributive lattice theory we have constructed a wire-speed multicast switching fabric based on a multi-path self-routing fabric structure developed previously by us, and implemented it on an Altera StratixIV FPGA chip.

The rest of the paper is organized as follows. The large-scale wire-speed multicast switching fabric system is described in Section II. The hardware implementation in FPGA is given in

Section III. In Section IV the real multicast stream test of the system is shown, and Section V is our conclusions.

II. THEORETICAL BASIS OF THE SYSTEM

The large-scale wire-speed multicast switching fabric system that we presented mainly consists of two components. One is Multi-path Self-routing Switching Structure based on group theory. The other one is sorting unit, which supports wire-speed multicast, based on distributive lattice.

A. Multi-path Self-routing Switching Structure

Multi-path self-routing switching structure [2] is completely self-routing [3] and modular. In such structure, parameter G indicates the group size, and M indicates the quantity of groups [4]. The packet loss rate caused by traffic fluctuation and sudden flow will exponentially decrease when we increase the parameter G [5]. As shown in figure 1 is a multi-path self-routing switching structure in which M is 16 and G is 8.

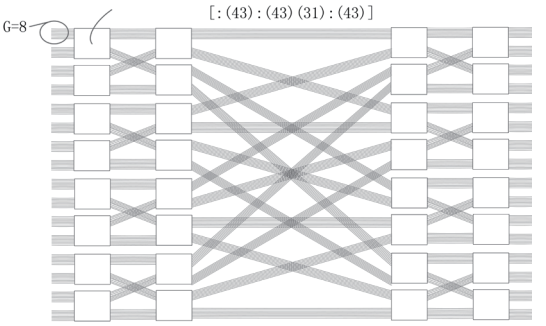


Figure 1. M=16, G=8 Multipath self-routing structure.

B. Sorting unit

Figure 2 describes the normal 2×2 sorting unit. It is the smallest element in switching fabric.

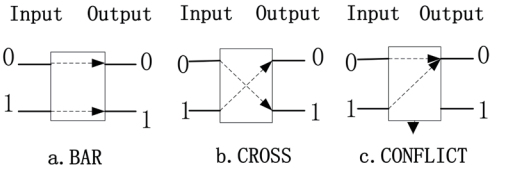


Figure 2. 2×2 sorting unit and its conditions

Such 2×2 sorting unit can act upon this in-band signaling: 10<00<11. The details are shown in Table 1.

TABLE I. Two bits` in-band signaling control mechanism

Conditions		INPUT-1 : A1D1		
		10	00	11
INPUT-0: A1D1	10	CONF	BAR	BAR
	00	CROSS	EITHER	BAR
	11	CROSS	CROSS	CONF

When CONF(CONFLICT), priority decides condition.

Based on distributive lattice, we further defined Ω_{route}*={0-bound,1-bound,idle}*. As a result, the previous ordering relation *10<00<11* equals *0-bound<idle<1-bound*.

When the sorting unit is used for multicast, we should define the multicast condition for the unit, as is shown in figure 3.

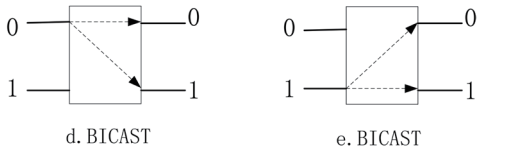


Figure 3. 2×2 sorting unit and its multicast condition

On the basis of the multicast supported sorting unit, we give the new in-band signaling and corresponding control mechanism in Table 2.

TABLE II. 2×2 Control mechanism for multicast sorting unit

Conditions		Input-1			
		0	1	B	I
Input-0	0	CONF	BAR	BAR	BAR
	1	CROSS	CONF	CROSS	CROSS
	B	CROSS	BAR	EITHER	BICAST
	I	CROSS	BAR	BICAST	EITHER

B: BICAST; I: IDLE;

III. SYSTEM DESIGN AND ANALYSIS

The system has been implemented on StratixIV FPGA of Altera. The parameters G and M are 8 and 4 respectively. On the FPGA, the system mainly comprises of user define path and register system.

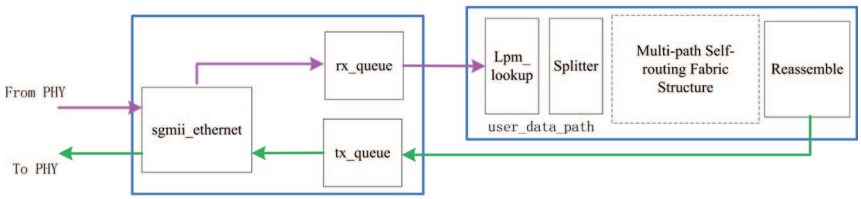


Figure 4. User define path.

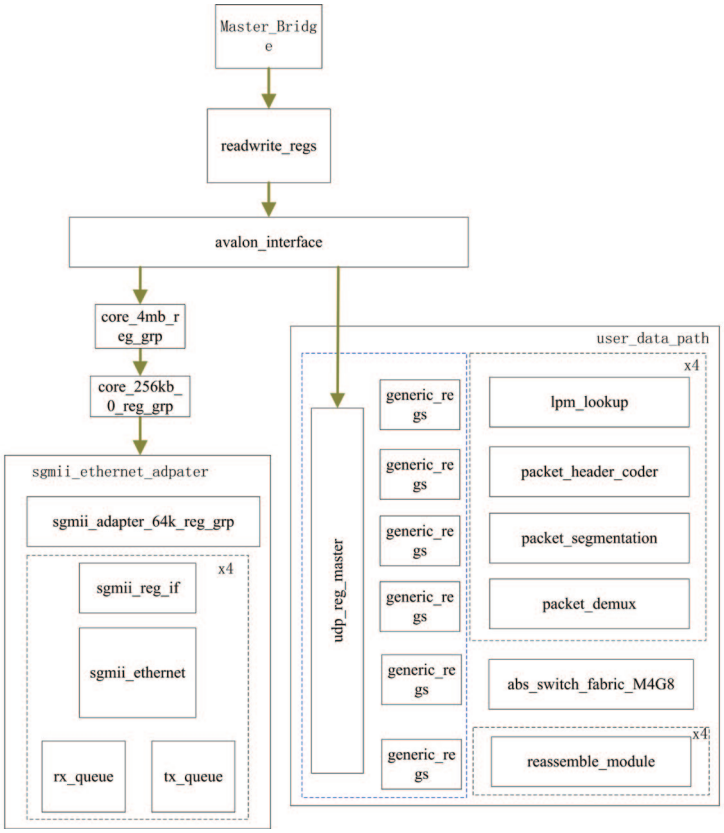


Figure 5. Register system

A. User define path

Figure 4 describes the structure of user define path. It mainly consists of seven sub modules.

Sgmii_ethernet: the interface of system and external PHY chip;

Rx_queue: extract the information of the data packets, such as length, and generate the splitter header;

Lpm_lookup: routing table lookup and generate the lpm header;

Splitter: Split the data packets to cells in certain length and generate the routing control header and cells reassemble header;

Multi-path Self-routing Fabric: Switching fabric;

Reassemble: Reassemble the cells which split in splitter and generate the starting index header;

Tx_queue: Send the data packets to sgmii_ethernet module and complete switching.

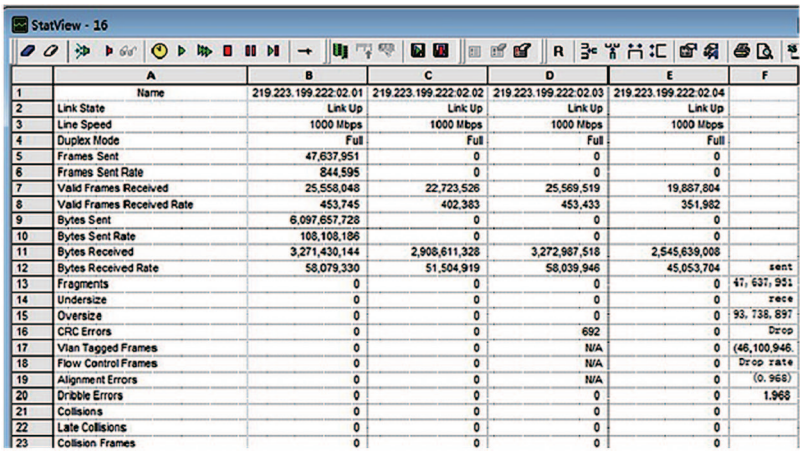
While a packet passing through the system, every sub module will extract the relevant information to generate various headers. The headers will be attached in front of the former packet. Additionally, the system adds two bits` control signal to assist us in data identification and processing. The control signal and packets will transmit in parallel.

B. Register system

The register system not only configures the sub modules in user define path, but also extracts the internal signals of the user define path to help us debug the system. The structure of the register system is revealed in figure 5.

We adopted pipeline architecture to design our register system. Registers are serially connected by specific interface. Every register only responses to the requests which belonging to it. Compared to the star architecture, it is much more convenient when we add another module into the system.

The register system is constructed in Qsys development environment which is attached in Quartus II. We utilized Jtag_Avalon_Master_Bridge and made the register interface for every sub module based on Avalon Bus Specification. Through the register system, we can use a computer to exchange signals with the system on FPGA.


StatView - 16

	A	B	C	D	E	F
1	Name	219.223.199.222:02.01	219.223.199.222:02.02	219.223.199.222:02.03	219.223.199.222:02.04	
2	Link State	Link Up	Link Up	Link Up	Link Up	
3	Line Speed	1000 Mbps	1000 Mbps	1000 Mbps	1000 Mbps	
4	Duplex Mode	Full	Full	Full	Full	
5	Frames Sent	47,637,951	0	0	0	
6	Frames Sent Rate	844,595	0	0	0	
7	Valid Frames Received	25,558,048	22,723,526	25,569,519	19,887,804	
8	Valid Frames Received Rate	453,745	402,383	453,433	351,982	
9	Bytes Sent	6,097,657,728	0	0	0	
10	Bytes Sent Rate	108,108,186	0	0	0	
11	Bytes Received	3,271,430,144	2,908,611,328	3,272,987,518	2,545,639,008	
12	Bytes Received Rate	58,079,330	51,504,919	58,039,946	45,053,704	sent
13	Fragments	0	0	0	0	47, 637, 951
14	Undersize	0	0	0	0	rece
15	Oversize	0	0	0	0	93, 738, 897
16	CRC Errors	0	0	692	0	Drop
17	Vlan Tagged Frames	0	0	N/A	0	(46,100,946
18	Flow Control Frames	0	0	N/A	0	Drop rate
19	Alignment Errors	0	0	N/A	0	(0. 968)
20	Dribble Errors	0	0	0	0	1.968
21	Collisions	0	0	0	0	
22	Late Collisions	0	0	0	0	
23	Collision Frames	0	0	0	0	

Figure 6. Test window

IV. SYSTEM TEST WITH REAL MULTICAST STREAM

We utilized IXIA 400T network tester to test our system. That tester supports 10/100/1000 Ethernet standard and also can generate and count and capture all kinds of streams.

Figure 6 is the test window of the tester. In the test shown in the window, the tester generated a stream from port1 to all the four ports. Now, the system has passed all the normal functional tests including unicast and multicast. Next step, we will implement more complicated tests to figure out the performance of our system in all kinds of network environment.

CONCLUSIONS

This paper constructs multicast sorting unit, on the basis of distributive lattice. Combining with the Multi-path Self-routing Fabric Structure, we constructed the wire-speed multicast switching fabric, implemented the system on StratixIV FPGA, and tested it with real network stream.

The system we implemented on FPGA is not large enough for network size nowadays. However, through it, we get much more familiar with the theoretical basis and development environment. In the near future, we will further research the large-scale utilization of our system.

ACKNOWLEDGMENT

The paper "Design of large-scale wire-speed multicast switching fabric system based on distributive lattice" does not include any other published articles and research achievement excluding the ones listed in the Reference above.

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FPGA Implementation of an Efficient Two-dimensional Wavelet Decomposing Algorithm

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Abstract — As the preferred method for the multi-resolution analysis of the image, discrete wavelet transform has gained more and more attentions. In this paper, a new VLSI architecture is designed to finish two-dimensional all at once. Through further derivation of the transform formulas, line based method is improved and the circuit structure is simplified. The FPGA implementation has been achieved on an Altera Cyclone II EP2C35F672C6. Results show that this improvement results in a considerable performance gain while reducing the consumption of on chip memory space and shortening output latency significantly. Under pure calculation logic, processing speed reaches 157.78MHz.

Keywords — wavelet transform, image processing, FPGA, VLSI, SOPC

I. INTRODUCTION

DWT is the preferred mathematic tool when it comes to observing and processing digital images. The lifting scheme is a fast implementation of wavelet transform, the procedure of filtering can be decomposed to several steps. Thus the amount of computation and memory space are reduced significantly. Also, it is quite suitable for in-place calculation and hardware implementation.

At present, there are two kinds of widely used VLSI architectures to realize 2-D lifting wavelet transform: the line based ones and the frame based ones. As research processes, new VLSI architectures come into being continuously. Although the performance of the circuits advanced gradually, low complexity still conflicts with low cost of memory space. In this paper, we put forward a new VLSI architecture for 2-D lifting wavelet transform which simplifies the circuit complexity and saves memory space greatly. That is how the overall performance of the circuit is improved.

II. WAVELET LIFTING ALGORITHM

A. Lifting Wavelet Transform

To achieve wavelet transform through the lifting scheme, there are three steps: Split, Prediction and Update. In the discrete situation, input data set p_k is split into two subsets to separate the even samples from the odd ones. After lifting scheme processing, the detailed coefficients s_k and the wavelet coefficients d_k are generated. Take Le Gall 5/3 wavelet for instance, the procedure of 1-D integer wavelet decomposition could be described by figure 1.

The lifting 5/3 wavelet algorithm is described as follows:

$$d_k = p_{2k+1} - (p_{2k} + p_{2k+2})/2 \quad (1)$$

$$s_k = p_{2k} + (d_k + d_{k-1} + 2)/4 \quad (2)$$

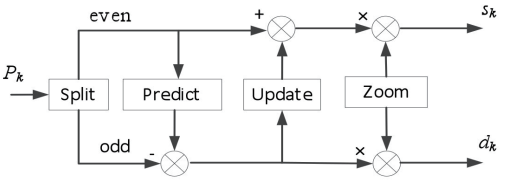

Figure 1. Split, predict and update phases of the lifting based DWT

Where p_k is original pixel data set, d_k is high frequency of transform result and s_k is the low frequency one.

The procedure of accomplishing 2-D transform is as follows: with line transform original image is divided into two sub-bands, and with a column transform they are divided into four sub-bands. Each sub-band is 1/4 size of the initial image. We can realize the next level wavelet transform as long as we do transform to LL sub-band in the same way. Figure 2 shows the procedure of three level wavelet transform.

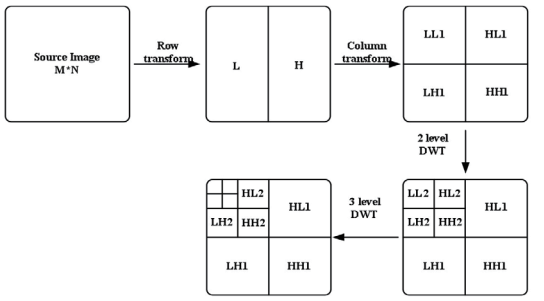

Figure 2. Theory of two-level DWT

For the reason that transform is proceeded in the column direction, he result of row transform must be input column by column. Large amount of middle data must be stored. That is why the cost of hardware is immense and the speed of data processing is limited.

B. Further Derivation for Two Dimensional Transform

We substitute expression (1) into expression (2) to get a 2-D transform VLSI architecture with a better performance:

$$s_k = (-p_{2k-2} + 2p_{2k-1} + 6p_{2k} + 2p_{2k+1} - p_{2k+2} + 4)/8 \quad (3)$$

In order to conduct 2-D wavelet image, further derivations of the transform formulas are necessary. The image pixels at row i and column j will be denoted as $p_{i,j}$. After getting the results of line transform, apply the formula to vertical direction to proceed column transform. Take the results of twice of the low filtering for instance, the correlation is:

$$\begin{aligned} p_{i,j}^{LL} = (&p_{2i-2,2j-2} - 2p_{2i-2,2j-1} - 6p_{2i-2,2j} - 2p_{2i-2,2j+1} + p_{2i-2,2j+2} \\ &-2p_{2i-1,2j-2} + 4p_{2i-1,2j-1} + 12p_{2i-1,2j} + 4p_{2i-1,2j+1} - 2p_{2i-1,2j+2} \\ &-6p_{2i,2j-2} + 12p_{2i,2j-1} + 36p_{2i,2j} + 12p_{2i,2j+1} - 6p_{2i,2j+2} \\ &-2p_{2i+1,2j-2} + 4p_{2i+1,2j-1} + 12p_{2i+1,2j} + 4p_{2i+1,2j+1} - 2p_{2i+1,2j+2} \\ &+p_{2i+2,2j-2} - 2p_{2i+2,2j-1} - 6p_{2i+2,2j} - 2p_{2i+2,2j+1} + p_{2i+2,2j+2})/64 + 1/2 \end{aligned} \quad (5)$$

Take the coefficients into determinant shown in figure 3(1).

Similarly, for the sake of getting the horizontal high frequency-vertical low frequency output (HL), the horizontal low frequency-vertical high frequency output (LH) and the horizontal high frequency-vertical high frequency output (HH), we can apply (1), (3) into 2-D transform in the same way. Determinants are shown as follows:

$$\begin{vmatrix} 1 & -2 & -6 & -2 & 1 \\ -2 & 4 & 12 & 4 & -2 \\ -6 & 12 & 36 & 12 & -6 \\ -2 & 4 & 12 & 4 & -2 \\ 1 & -2 & -6 & -2 & 1 \end{vmatrix}$$ (1)LL

$$\begin{vmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & -2 & -6 & -2 & 1 \\ -2 & 4 & 12 & 4 & -2 \\ 1 & -2 & -6 & -2 & 1 \\ 0 & 0 & 0 & 0 & 0 \end{vmatrix}$$ (2)HL

$$\begin{vmatrix} 0 & 1 & -2 & 1 & 0 \\ 0 & -2 & 4 & -2 & 0 \\ 0 & -6 & 12 & -6 & 0 \\ 0 & -2 & 4 & -2 & 0 \\ 0 & 1 & -2 & 1 & 0 \end{vmatrix}$$ (3)LH

$$\begin{vmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & -2 & 1 & 0 \\ 0 & -2 & 4 & -2 & 0 \\ 0 & 1 & -2 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{vmatrix}$$ (4)HH

Figure 3. Determinants of filter coefficients

III. DESIGN OF ARCHITECTURE

A. System Architecture

For 2-D DWT, we put forward an implementation of the lifting wavelet transform based on the formulas deduced from figure 3. System structure diagram is given in figure 4.Initial image data are read out from external memory, after edge expanding in the expand unit, they are sent into buffer units and then sent into the 2-D DWT processing module, creating four sub-band sets of data. After sampling, the results are sent to the VGA monitor to present. Each part of the system work under a certain timing sequence generated by the control modules of the system.

B. Design of Two-dimensional transformation module

In the process of 2-D wavelet decomposition of a digital image, the 2-D transform processor is the significant unit and influents the timing design of the system and its performance.

From the determinants given in figure 3, we can draw the conclusion that the process of the 2-D transform is in fact weighted summation from a 5×5 sampling window. Calculations in this process are mainly multiplications and additions. For example, equation (4) corresponds to Determinants

$$\begin{vmatrix} p_{2i-2,2j-2} & p_{2i-2,2j-1} & p_{2i-2,2j} & p_{2i-2,2j+1} & p_{2i-2,2j+2} \\ p_{2i-1,2j-2} & p_{2i-1,2j-1} & p_{2i-1,2j} & p_{2i-1,2j+1} & p_{2i-1,2j+2} \\ p_{2i,2j-2} & p_{2i,2j-1} & p_{2i,2j} & p_{2i,2j+1} & p_{2i,2j+2} \\ p_{2i+1,2j-2} & p_{2i+1,2j-1} & p_{2i+1,2j} & p_{2i+1,2j+1} & p_{2i+1,2j+2} \\ p_{2i+2,2j-2} & p_{2i+2,2j-1} & p_{2i+2,2j} & p_{2i+2,2j+1} & p_{2i+2,2j+2} \end{vmatrix}$$

And figure 3(1).

Set a certain column in the sampling window as vector $(p_1, p_2, p_3, p_4, p_5)$, Each clock period, column vectors in the sampling window will move one position to the right, and the most left a list of data will be updated. Set a certain column in determinants in figure 3 as $A=(a_1, a_2, a_3, a_4, a_5)$, the basic calculation will be $(p_1, p_2, p_3, p_4, p_5) \times (a_1, a_2, a_3, a_4, a_5)^T$.

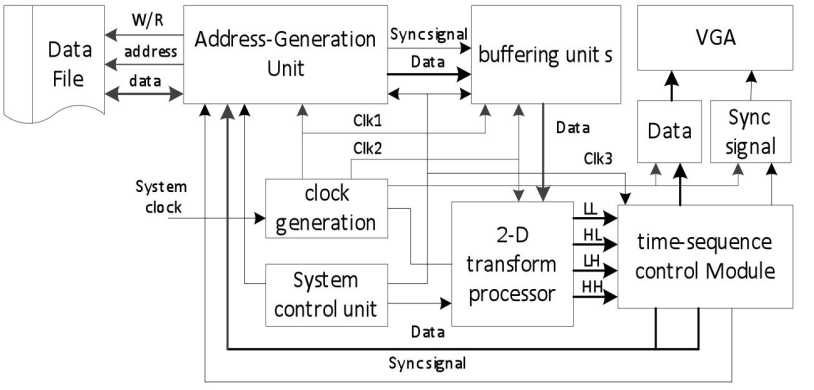

Figure 4. System architecture

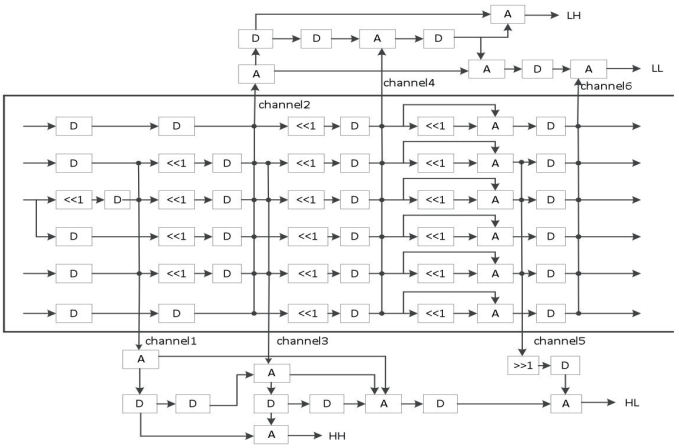

Figure 5. Inner structure of 2-D DWT processor

We can conclude from figure 4 that A has 6 different values: A_1=(1, -2, -6, -2, 1)^T, A_2=(-2, 4, 12, 4, -2)^T, A_3=(-6, 12, 36, 12 ,-6)^T, A_4=(0, 1, -2, 1, 0)^T, A_5=(0, -2, 4, -2, 0)^T, A_6=(0, -6, 12, -6, 0)^T. And A_3= $3A_2$ = -$6A_2$, A_6 = $3A_5$ = -$6A_4$.

On the basis of the determinants in figure 3, the processor's definite structure denotes in figure 5.

Parameter relationships between channels and vectors are:

TABLE I. PARAMETER RELATIONSHIPS BETWEEN CHANNELS AND VECTORS

channel	Vector A
channel 1	A_4 = (0, 1, -2, 1, 0)^T
channel 2	A_1 = (1, -2, -6, -2, 1)^T
channel 3	A_5 = (0, -2, 4, -2, 0)^T
channel 4	A_2 = (-2, 4, 12, 4, -2)^T
channel 5	A_6 = (0, -6, 12, -6, 0)^T
channel 6	A_3 = (-6, 12, 36, 12, -6)^T

This structure includes 15 adders, 18 shifters and 34 delay-units, no more extra multiplying units are needed. It can be estimated that if this 1-D 5/3 wavelet transform architecture is achieved on an FPGA chip, the number of logic units occupied will be 40A (A stands for bit width of the initial data)

$$N_{clk} = L_d + W = L_d + \frac{2}{3}N^2(1-\frac{1}{4^L}) \qquad (5)$$

Where L_d stands for the delay between line transform and column transform, in our design L_d=*0*, in other words, there are no middle data generates, so plenty of memory space is saved and delay between line transform and column transform is eliminated. What's more, although the number of data read operation of the external memory increases by a little, the working time of processor decreases sharply. That is the reason why the system consumption reduces obviously.

IV. RESULTS AND ANALYSIS

In order to test the performance of the architecture we design and observe the result intuitively, we realize simulation of the processor module with MODELSIM 6.5, as figure 6 shows.

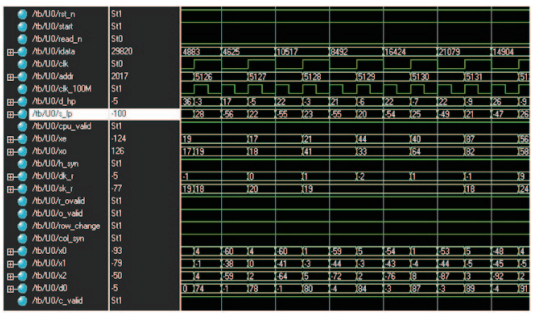

Figure 6. The simulation of 2-D DWT

We compare the 2-D DWT architecture we designed with others in terms of on-chip memory space, control difficulty and hardware complexity in Table II.

TABLE II. PERFORMANCE COMPARISON OF 5/3 2-D DWT ARCHITECTURES

Architecture	Lit. [3]	Lit. [4]	Lit. [5]	Lit. [6]	Our Design
Shifter	16	4	4	4	18
Adders	16	8	8	8	15
Memory on-chip	$5N$	N^2+4N	$6N$	$5N$	5
Memory off-chip	$N^2/4$	0	0	$N^2/4$	0
Computing time	$2N^2(1-4L)/3$	$2N^2(1-4L)/3$	N^2	$2N^2(1-4L)/3$	$2N^2(1-4L)/3$
Output latency	$2N$	$2N$	$2N$	$5N$	0
Utilization rate	100%	100%	50%	100%	50%
Complexity	Medium	Medium	Complex	Simple	Simple

CONCLUSIONS

This paper presents a new VLSI architecture for the lifting wavelet transform, Le Gall 5/3 wavelet taken as example. As a development of line base method, this architecture is advisable for its simple structure, high flexibility and low requirement of memory. Under pure calculation logic, processing speed reaches 157.88MHz.

Function and performance testing are conducted on an FPGA chip Cyclone II EP2C35F672C6, and we come to the conclusion that the intended targets have been achieved.

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FPGA Implementation of a Multi-Core System Architecture for Power Adaptive Computing

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Abstract — By analysing the system requirements of Power Adaptive Computing System, a Multi-core system is designed. The system has one master core for management and four slave cores for computing. A sharing bus structure and a special communication mechanism are designed. Based on the sharing bus and the communication mechanism, master CPU could schedule the tasks and control each slave CPU core. The architecture is simulated by modelsim and is verified based on FPGA. The result shows that the system the whole process of can successfully complete from tasks assigned to the result returned in this system.

Keywords — Multi-Core Architecture, FPGA, Power Adaptive Computing, Bus structure

I. INTRODUCTION

Because of the increasingly tight global energy supplies, governments and research institutions around the world are looking for new energy. [1][2] Using a variety of green energy or emerging energy as the source of energy of the electronic system has become the trend of the development of electronic systems.[3][4][5] Unlike traditional power supply such as batteries or DC power supply, emerging energy is not able considered as a stable and sustainable power for the electronic systems. How to protect modern electronic systems to automatically adapt to different power supply a variety of changes and to ensure the stability of the system and meet the requirements that the task should be processed in time should be focused.[4][5][6]

Task scheduling and power consumption conditioning of multi-core systems is the focus of current research, but most of the researchers are seeking for higher energy efficiency and better performance[7][8]. Only a few researchers began to study how to design the electronic system while the maximum output power of the source is time-varying. [9][10] In the other hand, a research work should be verified on a physical platform. So, how to implement a multi-core system which can used to verify different algorithms for power adaptive is one of the most important things.

In this paper, based on the analysis of the needs of power adaptive computing, a multi-core systems architecture is designed. One master RISC CPU core and four slave RISC CPU core are included in this architecture. The architecture of the sharing bus and the communication mechanism are the key points in this paper. Based on the shared bus and the communication mechanism, master CPU could schedule the tasks and control each slave CPU core. In the other hand every slave CPU core could load tasks, read data and return the result of the tasks by itself. The modelsim is used to simulate this system for the procedure from task loading to result returning. This system is also implemented on FPGA, and is s simply verified.

II. SYSTEM REQUIREMENTS ANALYSIS

According to the type of CPU core, a kind of multi-core systems is called homogeneous multi-core system[11] and the other is called heterogeneous multi-core system.[12] By the division of tasks, the cores of heterogeneous multi-core system are designed and optimized for different purpose in order to improve the performance of the system. For the purpose of implementation of power adaptive computing, one CPU core in this system should be used to executive management and scheduling program. However, it is very difficult to design and optimize a special management unit (MU), and is not necessary to that because management and scheduling program can be executed by a common CPU core. So, a common RSIC CPU could be used as a MU to execute.

This system is designed for doing research of power adaptive computing. So, the power consumption of the hardware can be regulated if it is necessary to do. The slave CPU cores which are executing different tasks could be slow down or speed up of the processing speed in order to regulate the power consumption. So, this system must be designed into a global synchronization local asynchronous (GALS) system. In this system, different slave CPU core could be used for different clock frequency. All the slave CPU cores need to increase necessary peripheral module to become independent subsystems, then the system could be more reliable.

In order to manage the system and schedule the tasks, although the MU which is running management program is the same as other RISC CPU cores which are running computing programs, a special communication mechanism and bus structure should be designed. The MU should have the highest priority of communication procedure for controlling the system. So, one Master RISC CPU core which is used to be MU and four Slave RISC CPU cores which are used to processing tasks are designed in this system.

Bus sharing and network on chip (NoC) are two different structure of the on-chip communication system. Bus sharing is a simple way to implement the on-chip communication system among the CPU cores, but the communication efficiency and flexibility is too low because it is too simple. NoC has become the focus of researchers in recent years because of higher scalability, reliability and reusable, but it is very difficult to implement and is no generally accepted conclusion. For this system, the various subsystems are relatively independent. If the tasks could stay in the subsystem long enough and need not be loaded frequently, the improving bus sharing structure is good enough.

In sum, the system should be designed according to the following rules:

[1]. Master-slave communication standard should be used and a master CPU core should be used to be MU to control this system;

[2]. The slave CPU cores need to increase necessary peripheral module to become independent subsystems and could processing the task independently;

[3]. The improving bus sharing structure will be used.

III. THE DESIGN OF MULTI-CORE SYSTEM

System block diagram in Figure 1. Bus sharing structure is used in this System. MU means Management Unit, and is the controller of this system. It is also the scheduler of the tasks. The CPU cores could process the tasks with different power consumption under the scheduling of MU. The CPU cores have necessary peripheral module

to build up subsystem. Wrapper module is the interface of the bus and is used to load tasks and transmit data.

A. Management Unit

MU could schedule the tasks and manage the system under the conditions that the output power is changeable of the sources. By receiving the information about the prediction of the energy source, MU could schedule the tasks and regular the frequent of the clocks of the subsystems for matching the power consumption of the system and output power of the energy sources. MU could control the slave to load tasks and receive the result by using internal bus. It also can transmit other information to control the subsystems. The MU could communicate with other systems by using Ethernet interface.

The bus is followed AMBA 2.0 protocol. MU is the Master of the bus and other module could be seen as peripherals of MU. Other CPU cores should apply to arbiter if they want to access to the bus. DDR2 SDRAM is the external memory of this system, and the tasks and data is stored in the

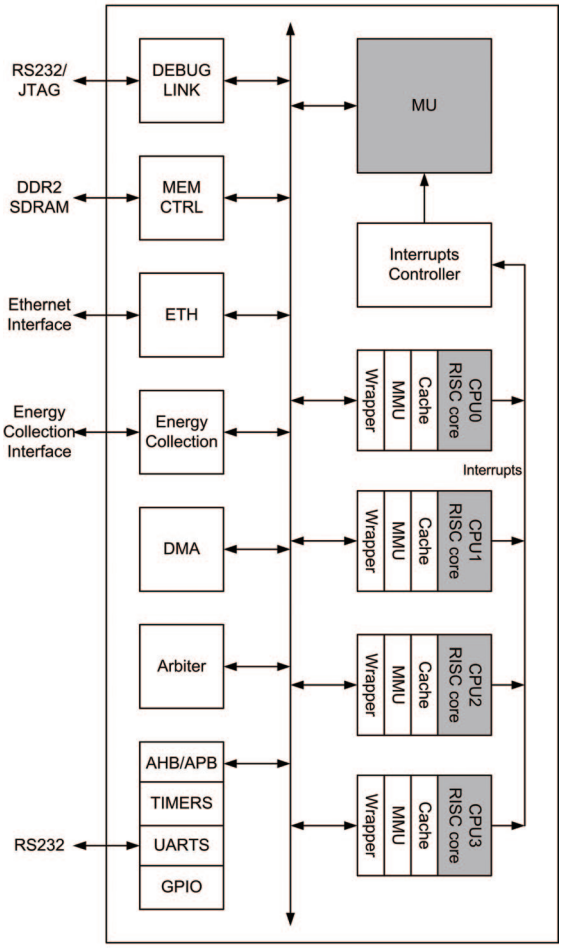

Figure 1. System Block Diagram of This System

memory. The CPU0 to CPU3 could communicate with the DDR2 SDRAM directly by using DMA module. Energy Collection module is the monitor of Power Sources. This module could monitor the change of Power Sources and prediction the trends of power. MU could schedule the tasks and control the whole system followed the information which is got by Energy Collection module. DEBUG LINK is the module which is used to debugging the programmes. This module could be connected with RS232 or JTAG interface, and the user could use this module to monitor each CPU core and the memories. The information could be send out by RS232 or JTAG.

B. Subsystem

A subsystem is build up by a slave CPU core and some necessary peripherals. The block diagram is shown as Figure 2.

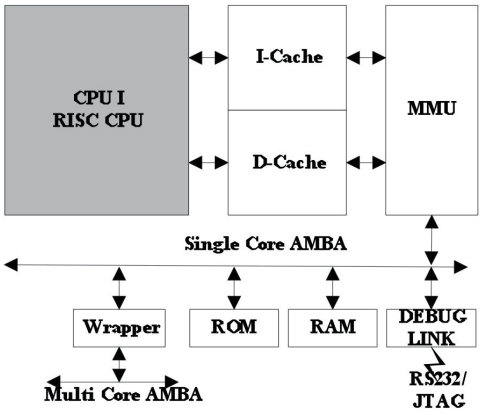

Figure 2. Block Diagram of Subsystem

The subsystem is build up by RISC CPU core, Cache, MMU, ROM, RAM, Wrapper and DEBUG LINK. The subsystem could run programme without any support because it has Cache, MMU, ROM and RAM independently. In other words, the Subsystems have all the characteristics of the smallest computing systems. So, if a task was loaded into the subsystem, it can be executed and need not be loaded frequently. It is very helpful to reduce the needs of bus.

Wrapper is the interface between internal bus of the subsystem and the sharing bus of the whole system. The structure of wrapper will be introduced in part C.

C. Communication Mechanism

Because of the complexity of On-Chip communication, a communication mechanism is defined. The each subsystem is separated from the sharing bus by a wrapper, and the wrapper also can be data buffer of the subsystem. The structure of wrapper is shown as Figure 3

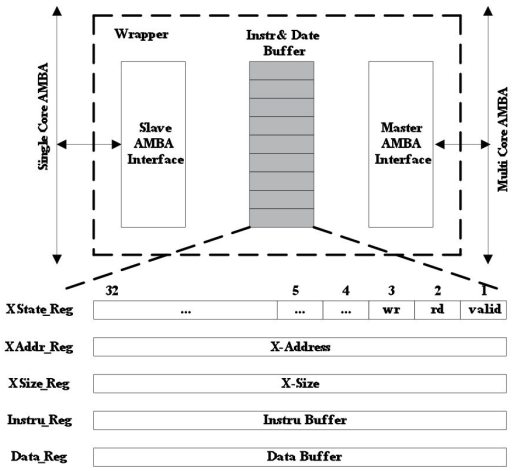

Figure 3. the Structure of Wrapper

The buffer is divided into three types, and the detail of the buffer is shown as Table I.

TABLE I. REGISTER FILE OF BUFFER

Register Name	(Master) W/R	(Slave) W/R	Size
MState_Reg	W/R	R	4Byte
SState_Reg	R	W/R	4Byte
MAddrI_Reg, MSizeI_Reg	W/R	R	4Byte
SAddrI_Reg, MSizeI_Reg	R	W/R	4Byte 4Byte
MAddrD_Reg, MSizeD_Reg	W/R	R	4Byte 4Byte
SAddrD_Reg MSizeD_Reg	R	W/R	4Byte 4Byte
Instru_Reg	W/R	W/R	
Data_Reg	W/R	W/R	

The procedure from loading tasks and returning the result is shown in Figure 4.

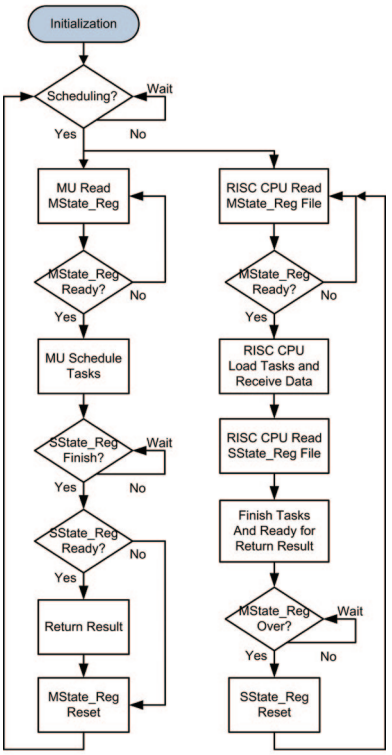

Figure 4. the whole Procedure of Task Scheduling

The register named MState_Reg can only be written by MU, and the other register SState_Reg can only be configured by slave CPU cores. It is very helpful for reducing conflicts of reading and writing of Wrapper.

IV. EXPERIMENTAL RESULTS

The system is simulated by modelsim 6.0 and the simulation results are shown in Figure 5.a and Figure 5.b:

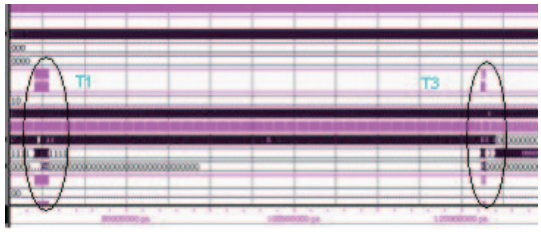

Figure 5.a the simulation results about MU schedule

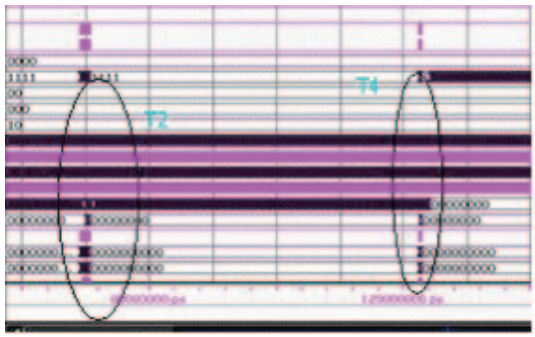

Figure 5.b the simulation results about subsystem loading and executing tasks

The initial software was compiled by Keil and the bin file was used to initial the ROM module by using tools of the software named Quartus II which is designed by Altera Company. The simulation results only show how to load task and return the result in CPU0, because all the subsystem are all the same.

At the time T1, MU sent information to the wrapper of subsystem. CPU0 core read register named MState_Reg at time T2 then got the information from buffer. At the time T4, CPU0

finish the task and return the results, and then the register named SState_Reg was renewed. After that, interrupt signal of MU was triggered by CPU0. MU read the statement about SState_Reg and got the results from the buffer.

The system is implemented based on EP3SE260F1152C2 of DE-3 development board as Figure 6 and the Synthesis Report is shown as Figure 7.

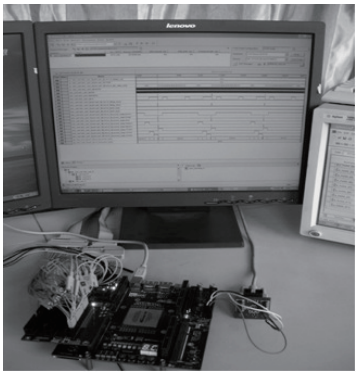

Figure 6. Verification Environment

Fitter Status	Successful - Sun Oct 14 17:41:17 2012
Quartus II Version	9.0 Build 132 02/25/2009 SJ Full Version
Revision Name	arm9_core
Top-level Entity Name	arm9_core_top
Family	Stratix III
Device	EP3SE260F1152C2
Timing Models	Final
Logic utilization	15 %
Combinational ALUTs	19,572 / 203,520 (10 %)
Memory ALUTs	0 / 101,760 (0 %)
Dedicated logic registers	8,513 / 203,520 (4 %)
Total registers	8514
Total pins	7 / 744 (< 1 %)
Total virtual pins	0
Total block memory bits	497,664 / 15,040,512 (3 %)
DSP block 18-bit elements	24 / 768 (3 %)
Total PLLs	2 / 8 (25 %)
Total DLLs	0 / 4 (0 %)

Figure 7. Synthesis Report

CONCLUSIONS

Nowadays, emerging energy is replacing traditional energy. So, to research how to design electronic system when the output power of the energy sources is changeable is a very important significance. Power adaptive computing systems could regulate the power consumption by themselves and could be an important way to solve this trouble. Multi-core system architecture of for power adaptive computing is introduced in this paper. The architecture is simulated by modelsim and is verified based on FPGA. The result shows that the system the whole process of can successfully complete from tasks assigned to the result returned in this system. It could be research platform of power adaptive computing. In the future, the reliability of communications and the corresponding memory consistency problem in the complex case need to research and implementation. In addition, to verify the basis of a variety of scheduling and management algorithm is to improve the system architecture.

ACKNOWLEDGMENT

This work was supported by the Fundamental Research Funds for the Central Universities, National Natural Science Foundation of China (61176025), NLAIC Grants (9140C0901101002 & 9140C0901101003), National Natural Science Foundation of China (61006027), New Century Excellent Talents Program (NCET-10-0297).

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Introduction of the Research Based on FPGA at NICS

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Abstract — This document introduces the research work based on FPGA at Nano Integrated Circuits and Systems Lab, Department of Electronic Engineering, Tsinghua University.

Keywords — WSN Digital Baseband SOC, Two-dimensional Bar Code, Dynamic Time Warping Distance, Real Time Image Processing, FPGA

I. INTRODUCTION

The Nano Integrated Circuits and Systems Lab at the Department of Electronic Engineering, Tsinghua University, Beijing, China focus on the following research fields, Chips for Communications and Digital Media Processing, Electronic System Design Automation, Analog and Mixed-Signal Integrated Circuits Design, and Design of Radio-Frequency and Microwave Integrated Circuits.

In the field of Chips for Communications and Digital Media Process, research activities include ASIC design for wireless communication, digital broadcasting, and digital media applications.

A field-programmable gate array (FPGA) is a chip designed to be configured by a customer or a designer after manufacturing.[1] Hence, "field-programmable" is the biggest advantages, which can let the researcher update the functionality after shipping, partial re-configuration of a portion of their design. Moreover, with the ability of the low non-recurring engineering costs relative to an ASIC design, FPGAs offer advantages for many applications.

The structure of this paper is arranged as follows. Section II introduces the prototype system for our wireless sensor network digital baseband system-on-a-chip design based on DE2-70. Section III presents the implementation of an embedded two-dimensional bar code recognition system based on DE2. A subsequence similarity search algorithm based on Dynamic Time Warping (DTW) distance, is accelerated in Section IV. A hardware platform for a real time image processing system is built in Section V. Finally, the conclusions and acknowledgements are given.

II. BUILDING THE PROTOTYPE SYSTEM FOR WSN DIGITAL BASEBAND SOC DESIGN

Wireless Sensor Networks (WSNs) are widely used as information acquisition and processing platforms in many applications.

In order to design all digital WSN baseband SOC, a prototype based on DE2-70 is built to verify our design, as shown in Figure 1.[2]

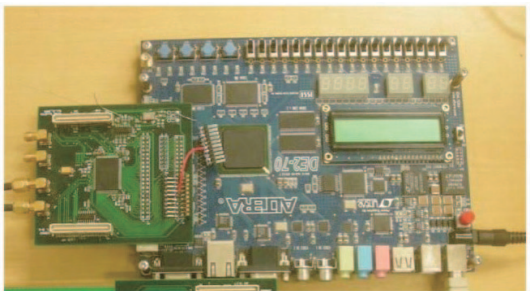

Figure 1. Prototype based on DE2-70[3] for WSN digital baseband SOC design

To meet the requirements of low complexity, low power and high flexibility, many algorithms are proposed, such as modulation, demodulation, spreading and synchronous, digital frequency converter, interpolation and decimation filter. According to the proposed algorithm, the architecture of our baseband circuit design is implemented in the prototype.

As shown in Figure 2, the MCU core 8051 consumes 3427 LUTs, while the baseband circuits consume 3282 LUTs. The resource of DE2-70 is more than enough for our design.

Entity	Logic Cells	Dedicated Logic Reg.	Memory Bits	M4Ks	Pins	LUT-Only LCs	Register-Only LCs
Cyclone II: EP2C70F896C6							
wcu_cov	13830 (8)	7078 (5)	133632	36	142	6752 (1)	1084 (0)
SBGT_LUT_2:SBG7	14 (0)	0 (0)	0	0	0	14 (0)	0 (0)
SBGT_LUT_2:SBG72	14 (0)	0 (0)	0	0	0	14 (0)	0 (0)
SBGT_LUT_2:SBG73	14 (0)	0 (0)	0	0	0	14 (0)	0 (0)
mc8051_top:b2v_inst1	3955 (0)	520 (0)	132096	33	0	3427 (0)	24 (0)
conv2:b2v_inst3	0	0	0	0	0	0	0
spi_baseband:b2v_inst5	9827 (0)	6545 (0)	1536	3	0	3282 (0)	1060 (0)
flash_cov:b2v_inst8	8 (8)	8 (8)	0	0	0	0 (0)	0 (0)

Figure 2. Resource Consumption of Cyclone II

III. IMPLEMENTING AN EMBEDDED TWO-DIMENSIONAL BAR CODE RECOGNITION SYSTEM BASED ON FPGA

A two-dimensional bar code is a symbol in the plane, which has particular shape both in its horizontal and vertical direction. Therefore, it has the ability of carrying more information in smaller area with higher error tolerance as well as better scalability compared to a one-dimensional bar code.[4]

As an open standard, PDF417 code is adopted to design an embedded two-dimensional bar code recognizing system based on FPGA using the NIOS II processor[5], as shown in Figure 3.

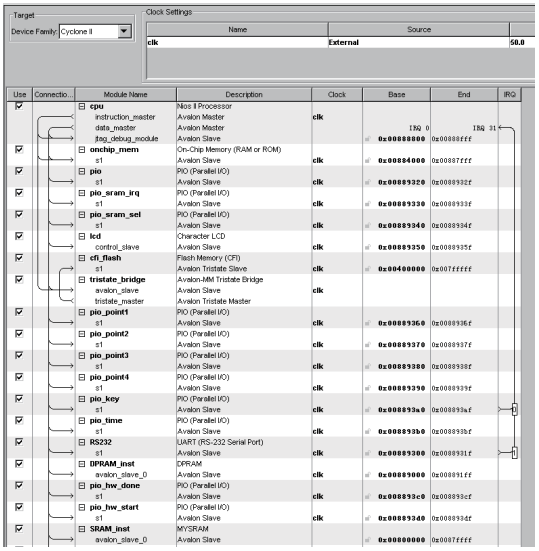

Figure 3. The whole configuration for NIOS II processor

Figure 4 show the report for the resource utility of our design based on DE2. The software-based system can finish the recognition in 28ms with 90% accuracy, given a 320 * 240 two-dimensional bar code image.

Flow Status	Successful - Thu Jun 02 19:47:02 2011
Quartus II Version	7.2 Build 151 09/26/2007 SJ Full Version
Revision Name	DE2_TV
Top-level Entity Name	DE2_TV
Family	Cyclone II
Device	EP2C35F672C8
Timing Models	Final
Met timing requirements	No
Total logic elements	28,631 / 33,216 (86 %)
Total combinational functions	25,378 / 33,216 (76 %)
Dedicated logic registers	14,078 / 33,216 (42 %)
Total registers	14127
Total pins	430 / 475 (91 %)
Total virtual pins	0
Total memory bits	242,256 / 483,840 (50 %)
Embedded Multiplier 9-bit elements	70 / 70 (100 %)
Total PLLs	1 / 4 (25 %)

Figure 4. The report for the resource utility of our design based on DE2[6]

IV. ACCELERATING SUBSEQUENCE SIMILARITY SEARCH BASED ON DYNAMIC TIME WARPING DISTANCE WITH FPGA

Subsequence search, especially subsequence similarity search, is one of the most important subroutines in time series data mining algorithms, and Dynamic Time Warping (DTW) distance is best. Although many software speedup techniques, including early abandoning strategies, lower bound, indexing, computation-reuse, DTW still cost about 80% of the total time for most applications. Moreover, DTW is hard to use parallel hardware to be accelerated because it is 2-Dimension sequential dynamic search with quite high data dependency.

A novel framework for FPGA based subsequence similarity search and a novel PE-ring structure for DTW calculation are proposed.[7] Figure 5 illustrates the framework.

The framework utilizes the data reusability of continuous DTW calculations to reduce the bandwidth and exploit the coarse-grain parallelism, and guarantees the accuracy with two-phase precision reduction. The PE-ring supports on-line updating patterns of various lengths, and utilizes the hard-wired synchronization of FPGA to realize the fine-grained parallelism, which can only be exploited by FPGAs.

Our system is implemented on TERASIC Company's Altera DE4 Board with a Stratix IV GX EP4SGX530 FPGAs.[8]

The resource cost of our system is shown as Figure 6.

Combinational ALUTs	362,568/424,960	(85%)
Dedicated logic registers	230,160/424,960	(54%)
Memory bits	1,902,512/21,233,664	(9%)

Figure 6. The report for the resource cost of our system based on DE4

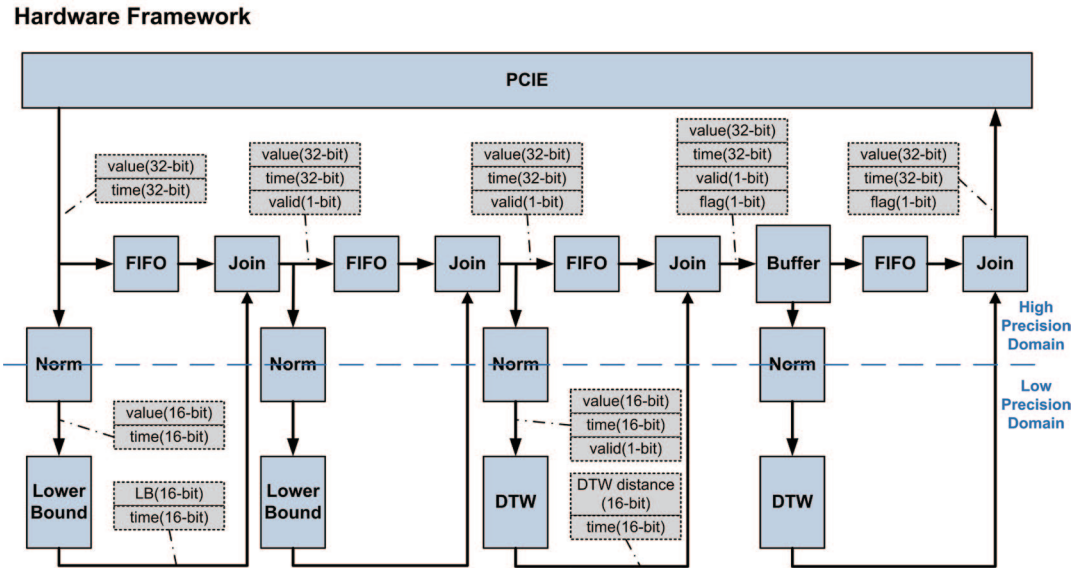

Figure 5. Hardware framework of the DTW system

The experimental results show that this work achieves one to four orders of magnitude speedup compared to the best software implementation in different datasets, three orders of magnitude speedup compared to the current GPU implementations, and two orders of magnitude speedup compared to the current FPGA implementation.

V. CONSTRUCTING A DETECTION AND 3D MEASUREMENT FPGA BASED SYSTEM FOR A REAL TIME IMAGE PROCESSING

Electronic Road Pricing (ERP) system is widely used in the world. The first large scale free flow road pricing system has been successfully in operation in Singapore since April 1998, in which an enforcement system (vehicle detection and license plate recognition) has achieved the performance of success rate of license plate recognition as 96% in 1.5 million pieces of vehicle units. However, the performance is based on lots of high quality of equipments with high cost, such as in-vehicle-units for every vehicle, complex gantries with many sensors, high luminance lighting, and high resolution cameras. As a result, reducing system cost is the most important issue for expanding sales for other countries. [9]

In some markets, the use of only video cameras for the enforcement system to identify the vehicles might be a cost reduction option since complex gantries would be removed. A simple enforcement system with video cameras offers high performance solutions with very low initial investment. Stereo cameras are needed to assure the tolling accuracy. Due to the fact that cameras, especially stereo ones, will provide really large real-time video for the tolling system to detect and classify the vehicles, a real-time and high throughput image processor is very necessary.

FPGA has millions of LEs (Logic Elements) processing at the same time in a parallel way and this feature can achieve high parallelism and throughput which fit for the real-time vehicle detection and classification algorithms from the video. However, in order to achieve high performance and low cost using FPGA, the key problem is how to reasonably analyze the computation cost and computation load allocation of vehicle detection and classification algorithms. Thus, we design the FPGA based detection and tracking processing system.

Based on simulation by ModelSim SE 6.5 and synthesis by Quartus II 10.0, the hardware implementation on Altera Stratix IV FPGA can reach 125MHz. It could achieve about 43 fps for video of 1392*1040 resolution with a large disparity range of 256, and 400 fps for a video of 640*480 resolution with a disparity range of 128. The detection and tracking part only gives the tracked area, so the image for these modules is resized to 320*256. We keep the 1392*1040 resolution for stereo matching in order to achieve more accurate size extraction.

The software results are tested on an i7 930 2.8GHz CPU based on OpenCV library. The results as shown in Table I indicates that our FPGA implementation of the system has 71.38 times speedup than software, and 63.91 times speedup for stereo matching.

TABLE I
SW AND HW RESULTS FOR ONE 1392*1040 IMAGE

Module	Software(ms)	Hardware(ms)	Speedup
Detection	161.42	2.42	66.70
Stereo Matching	1380.40	21.60	63.91
Total	1541.82	21.60	71.38

CONCLUSIONS

In summary, with the outstanding abilities of FPGA, much research work is done based on FPGA at NICS lab.

This paper introduces four projects. The prototype system for our wireless sensor network digital baseband system-on-a-chip design based on DE2-70 helps us to verify our proposed circuits and algorithms. The implementation of an embedded two-dimensional bar code recognition system based on DE2 shows that the proposed design can finish the recognition in 28ms with 90% accuracy, given a 320 * 240 two-dimensional bar code image. A subsequence similarity search algorithm based on Dynamic Time Warping (DTW) distance, is accelerated in DE4. Compared with other software and hardware methods, it can achieve at least two orders of magnitude speedup. A hardware platform for a real time image processing system is built based on DE4, and experimental results demonstrate that our FPGA implementation of the system has 71.38 times speedup than software, and 63.91 times speedup for stereo matching.

ACKNOWLEDGMENT

Many thanks to Altera Corp. for supplying excellent FPGA chips, and TERASIC Company for their powerful DE series boards.

Many thanks to National Science and Technology Major Project of the Ministry of Science and Technology of China, National Natural Science Foundation of China, Microsoft and Mitsubishi Heavy Industries for their financial support.

Many thanks to prof. Huazhong Yang, Yu Wang and Yongpan Liu for their contributions to the research work at NICS.

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SOPC-based VLF/LF Three-dimensional Lightning Positioning System

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Abstract — Lightning monitor technology is developing on the orientation of high accuracy, multi-lightning detect, three-dimensional monitor and lightning positioning. An SOPC-based VLF/LF three-dimensional lightning positioning system is presented in this paper. On the Altera's Cyclone II platform, a Nios II embedded CPU is constructed. Through the AVALON bus, hardware modules, such as the controller of the signal collection board, the AD's controller, the processor of lightning signal, the synchrotimer, the smoothing filter, the Zigbee controller, the network interface and the memory management IP, communicate with the CPU. This hardware-software collaboration structure efficiently decreases the complexity of the design and improves the system's flexibility. Based on the lightning detecting instrument, a three-dimension lightning positioning network is setup. Through the multi-station time difference of arrival (TDOA) algorithm, the network can detect a thunderstorm's generation, progress and attenuation, which is important for both the research and the early forecasting of the thunder.

Keywords — lightning, three-dimensional positioning, time difference of arrival, field programmable gate array, thunderstorm

I. INTRODUCTION

As a strong discharge phenomenon, lightning is an air breakdown, caused by electric charge accumulation of the relative movement of the ice crystal or moisture in cloud. Lightning could kindle a forest, destroy a building, or even hurt a human, which makes a severe influence on the civil and military aircraft of aerospace, communication equipments and electric apparatus. So the research of lightning monitoring and prevention is highly concerned in most countries.

Besides the direct cloud-to-ground (CG) lightning, the intracloud (IC) lightning attracts researchers' attention in these years. Generally speaking, IC lightning is the precursor of the disastrous weathers, such as the thunderstorm, heavy rain. It is the most frequent lightning event, and the first discharge of CG lightning normally also follows IC flashes. So the ultimate aim of lightning detect is the three-dimensional monitoring of both CG flash and IC flash [1]. When it is achieved, the lightning's parameters, such as the three-dimensional position of a lightning, the relationship between the height and frequency of IC lightning, the ratio of the positive lightning to the negative lightning, and the duration of the thunderstorm, can be calculated. Go a step further, the progress of a thunderstorm can be observed, and a trend of thunderstorm on the three-dimensional area can be predicted. It is available

on the monitor of the strong convection disastrous weather, the development of the weather forecast, and the thunder and lightning disasters defense.

Many countries and regions, like America, Europe, Japan, Brazil and Australia, have setup lightning monitor network. From 1984 to 1989, America constructed three separate lightning detect local area network, which based on magnetic direction lightning detect instrument. In 1989, America setup its national lightning detect network (NLDN) [2]. In 1995, NLDN was updated by equipping the VLF/LF time difference direction-finding hybrid detector (IMPACT location method) station [3,4], which realized the detection of CG lightning and the relative return stroke [5]. Nowadays, the lightning detect efficiency of NLDN has over 95%, and the average precision of positioning is 250m. Besides that and in 2011, America prepares to upgrade the NLDN to a three-dimensional lightning detect net by combining the VHF interference measure method and the VLF/LF IMPACT technology. In 2007, the atmospherics research group in the University of Munich developed the Europe lightning detect network (LINET) [6], which was composed of 90 sensor stations, and located in the 17 countries of Europe, such as Germany, France, Belgium, Finland, Poland, Italy, Britain, Spain and so on. Its detect region covers the whole Europe. Besides the detection of CG lightning and IC lightning, it can support the three-dimensional positioning, whose precision achieves 150m.

The study of the lightning monitor in China started at 1960's. At 1970's the direct-finding detection system was developed. At the end of 1980's, the ALDF system was imported from the LLP Company. In 1997, the National Space Science Center of the Chinese Academy of Sciences developed the IMPACT system. By employing it, China Meteorological Administration started the national lightning detect network in 2004, and finished it in 2007. Nowadays, the net has 311 detect stations, which cover the 80% region of China. Comparing with the three-dimensional detect nets of America and Europe, that net can only detect CG lightning and give the two-dimensional positioning, lacking of the ability of IC lightning detect and regional thunder forecast. It must be upgraded!

On the support of the National Science & Technology Pillar Program for the 11th five-year plan of China, the Meteorological Observation Centre of the China Meteorological Administration, the School of Physics and Technology of Wuhan University, and the National Space Science Center of the Chinese Academy of Sciences collaborated to develop a high precision three-dimensional CG&IC lightning positioning system in 2008. Employ FPGA as a controller, the new system's performance and stability are improved. Because of its compact structure, the power consumption is also decreased. Through the test in 2010 and in 2011, the new system is verified. In 2012, the VLF/LF three-dimensional lightning positioning service network of Jiangsu Province has been applied. In that network, 16 VLF/LF lightning detecting instruments setup on 16 meteorological stations, and a lightning data center takes the charge of data process.

II. THREE-DIMENSIONAL POSITIONING ALGORITHM

Time difference of arrival (TDOA) technology [7,8] derives from the "Roland" navigation positioning system, which determined its own position by the signals from three known-position transmitters. But different from it, a TDOA system in lightning detection uses three known-position receivers to determine an unknown-position transmitter.

Through the dealing the data of radiation arrival time from three or more than three observation

stations, TDOA algorithm localizes the radiator's position by hyperbolic curves. The time difference of the radiation arriving two stations can setup a hyperbolic curve, in which the two stations are on the focuses. Adding the third observation station, two hyperbolic curves can be confirmed, and their intersection determines the radiator' position in a two-dimension plane. By that analogy, three hyperboloids can be got if we have four or more than four stations. Using the intersection point of the intersection lines of these hyperboloids, the position of a radiator can be determined.

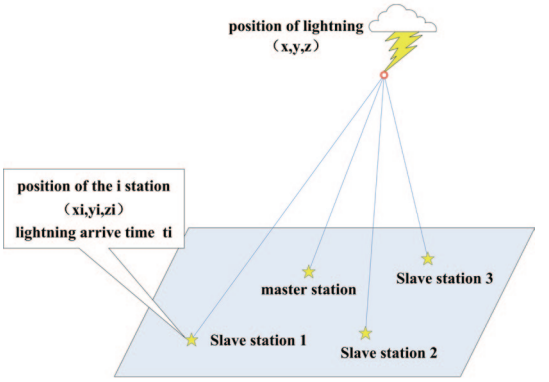


Figure 1. Schematic of a four-station TDOA positioning

As Figure 1 shows, the position of the observation stations are (x_i,y_i,z_i), in which i=0 stands for the master station, and i=1,2,3 stand for the slave stations. The position of the lightning is set as (x,y,z). The distance between it and the master station is R_0, and the distances between it and the slave stations are R_i. The difference between R_0 and Ri is ΔR_i. So TDOA algorithm can be described as,

$$\begin{cases} R_0^2 = (x-x_0)^2 + (y-y_0)^2 + (z-z_0)^2 \\ R_i^2 = (x-x_i)^2 + (y-y_i)^2 + (z-z_i)^2 \quad i = 1,2,3 \\ \Delta R_i = R_i - R_0 = c(t_i - t_0) \end{cases} \tag{1}$$

Submitting the last two equations into the first equation, one can get,

$$(x_0 - x_i)x + (y_0 - y_i)y + (z_0 - z_i)z = k_i + R_0 * \Delta R_i \tag{2}$$

where

$$k_i = \frac{1}{2}\left[\Delta R_i^2 + (x_0^2 + y_0^2 + z_0^2) - (x_i^2 + y_i^2 + z_i^2)\right] \qquad (i = 1,2,3)$$

Eq.2 can be rewrite as the following matrix,

$$\begin{bmatrix} x_0 - x_1 & y_0 - y_1 & z_0 - z_1 \\ x_0 - x_2 & y_0 - y_2 & z_0 - z_2 \\ x_0 - x_3 & y_0 - y_3 & z_0 - z_3 \end{bmatrix} \cdot \begin{bmatrix} x \\ y \\ z \end{bmatrix} = \begin{bmatrix} k_1 + R_0 * \Delta R_1 \\ k_2 + R_0 * \Delta R_2 \\ k_3 + R_0 * \Delta R_3 \end{bmatrix} \tag{3}$$

Eq.3 is a linear equation set about (x,y,z) with parameter R_0, so we can represent (x,y,z) as R_0's function. Submitting it into Eq.1, R_0 can be solved. Then, (x,y,z) can be calculated.

For the case of no solution, we determine a quasi optimum solution for the positioning. It is the point that has the minimum distance sum to the three hyperboloids, determined by the four observation stations. Set that point as T (x,y,z), and its distances to the three hyperboloids are d1(x,y,z), d2(x,y,z), d3(x,y,z), the distance sum is,

$$F(x,y,z) = d_1^2(x,y,z) + d_2^2(x,y,z) + d_3^2(x,y,z) \tag{4}$$

Let the partial differentials of Eq.(4) equal zero, we have,

$$\begin{cases} \dfrac{\partial F(x,y,z)}{\partial x} = 0 \\ \dfrac{\partial F(x,y,z)}{\partial y} = 0 \\ \dfrac{\partial F(x,y,z)}{\partial z} = 0 \end{cases} \tag{5}$$

Form Eq.5, the quasi optimum point T can be calculated.

III. SYSTEM ARCHITECTURE

A. General Framework

Our three-dimensional lightning positioning network absorbs the advantages of the IMPACT-ESC and the LINET. The arrival time of lightning's VLF/LF electromagnetic pulse is accurately measured by using the GPS time calibration. Based on TDOA algorithm and the wideband net communication technology, the lightning's parameters, such as the generation time, the intensity and the three-dimensional coordinate are calculated. Then the three-dimensional positioning is realized.

The lightning positioning network is composed by more than four lightning detecting instruments (setup on four meteorological stations, and the distance between each two stations is more than 70km) and a lightning data center. The lightning detecting instrument takes the charge of collecting the lightning signal and transports signal to the data center. The lightning data center calculates lightning's three-dimensional position based on the data from the lightning detecting instruments, and transports the result to a 3D graphic interface in the form of an UDP package. More than that, the lightning data center saves all lightning data on an Oracle data base, and then the data is used in relative applications. This Framework is shown in Figure 2.

B. Specifications

According to the lightning's characteristics and the requirement of the three-dimensional positioning, the following specifications are pointed out.

[1]. The specifications of the network:

- Lightning type:
  - positive cloud-to-ground flash (+CG)
  - negative cloud-to-ground flash (-CG)
  - positive intracloud flash (+IC)
  - negative intracloud flash (-IC)
- Three-dimensional positioning accuracy:
  - The horizontal error is less than 300m (on the region of the stations).
  - The vertical error is less than 500m (on the region of the stations).

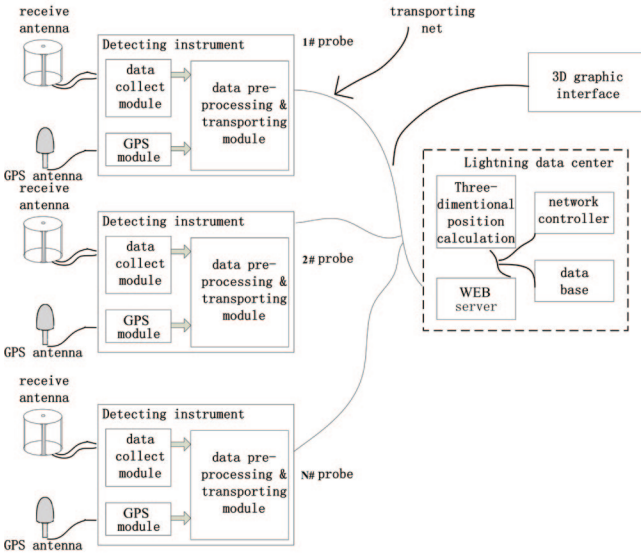


Figure 2. General framework of the three-dimensional lightning positioning network

- Detection efficiency: higher than 90% for CG flash (on the region of the stations).
- Lightning intensity detect error: less than 10%.
- Lightning polarity detect accuracy: higher than 99.9%.
- Lightning detect time: less than 10-4S.
- Lightning detect resolution: smaller than 2mS.
- Operation mode: Auto, Continuous, Real-time, Unmanned.
- Reliability: no-failure working time is longer than 20000 hours.

[2]. The specifications of the detecting instrument:

- Lightning type:
  - positive cloud-to-ground flash (+CG)
  - negative cloud-to-ground flash (-CG)
  - positive intracloud flash (+IC)
  - negative intracloud flash (-IC)
- Lightning intensity detect error:
  - less than 3% when lightning current is between 10kA and 100kA.
  - less than 10% when lightning current is smaller than 10kA or bigger than and 100kA.
- Synchronization time accuracy: higher than 10-7S.
- Direction-finding accuracy: higher than $\pm 1°$ after calibration.
- Lightning detect region: smaller than 600Km.
- Detection efficiency: higher than 95% when the lightning current is bigger than 5kA.
- Lightning process time: less than 1mS.
- Power supply: mans electricity, 85~265V, 50~60Hz, DC electricity, 20~30V.
- Communication: wired network, GPRS/ CDMA network, SATCOM.
- Power consumption: less than 15W.
- Repair time: shorter than 30 minutes.
- Reliability: average no-failure working time is about 30000 hours.
- Environment temperature: -40 °C ~ 50 °C.
- Working temperature: -20 °C ~ 70 °C.
- Environment humidity: 0 ~ 100%.
- Rainfall condition: 7.6cm/h when the wind speed is 65km/h.
- Anti-salinity: available near the sea.

C. SOPC Design of the Lightning Detecting Instrument

The VLF/LF detecting instrument is composed by the pre-NCHP, FPGA chip and its configuration chip, memory chip, digital temperature sensor, constant temperature crystal oscillator (10MHz), debug interface, display module and communication interface, etc. The pre-NCHP includes the signal pre-process module, orthogonal ring antenna interface and self-checking module. A constant temperature crystal oscillator and a high precision GPS [9] insure the accuracy of time measure (100nS). The lightning signal process module eliminates the background noise and the high frequency interference [10]. A wireless Zigbee

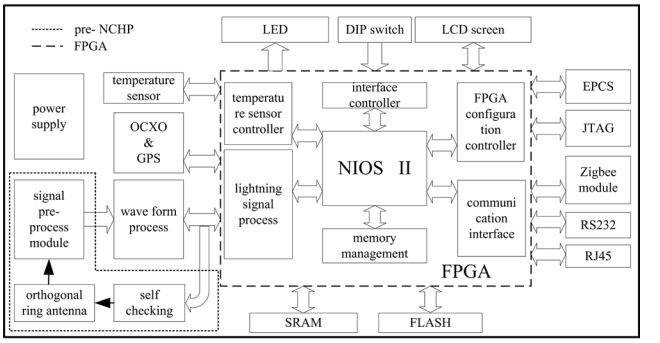


Figure 3. Schematic of the lightning detecting instrument

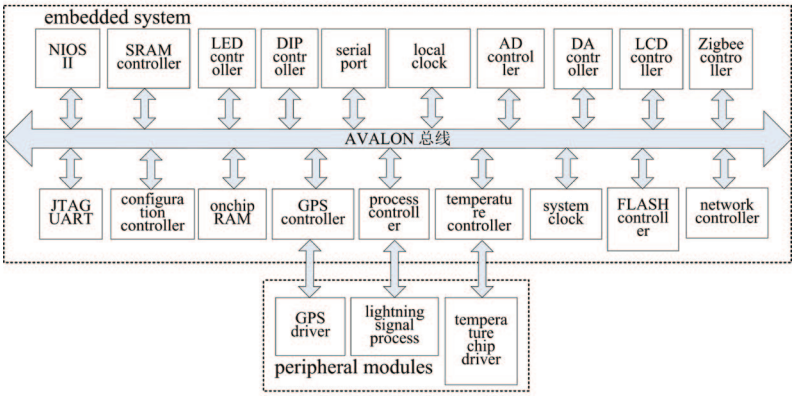


Figure 4. Structure of the SOPC system

module [11] and two wired ports (RS232 & RJ45) are configured for communication. The schematic of the lightning detecting instrument is shown as Figure 3.

FPGA is the key device of the lightning detecting instrument. In a Cyclone II EP2C series chip, the function modules, which are mentioned above, are connected by an AVOLON bus and controlled by NIOS II [12], an embedded CPU. The structure of this SOPC system is drawn in Figure 4.

The embedded software of the SOPC system completes the functions of system operation, such as the system initiation, self checking, interrupt routine, lightning signal judge, GPS time service, local clock management, state management, and communication with the upper computer. The software's flow chart is drawn as Figure 5.

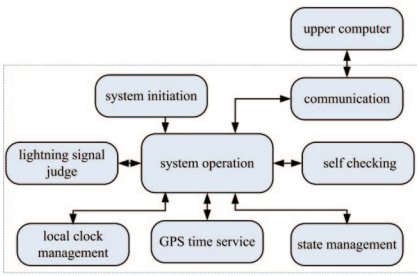


Figure 5. Flow chart of the embedded software

The system initiation function realizes the initial state setup for the whole SOPC system, including the interrupt set, the ADC initiation, the RAM checking, the GPS detecting, the local clock calibration, and so on. The self checking function checks the system's status and calculates the temperature and time compensation [13]. The system operation is the main module, which realizes the analysis of the lightning data and the control of the embedded system.

IV. TESTS AND APPLICATION

A. Consistency Test of the Lightning Detecting Instrument

To verify the lightning detecting instrument's consistency character on the flash receiving time and the flash pluses amplitude, comparison experiment had been done at the Beijing Meteorological Station in 2010. Five lightning detecting instruments were tested by the same lightning signals from the 10 pm. 2010-08-08 to the 10 am. 2010-08-09. During that time, 6083 lightning are monitored. The results of a twice stroke lightning on the experiment are shown as Table I and Table II.

TABLE I. TEST RESULT OF THE FIRST RETURN STROKE

No.	Time*	Angle	Magnetic field intensity	Electric field intensity	Leading edge of lightning	Trailing edge of lightning
0	1.454	193.94	0.46	0.27	26	202
1	1.453	189.70	0.48	0.29	28	205
2	1.453	192.86	0.47	0.29	26	204
3	1.454	188.34	0.44	0.29	26	202
4	1.453	193.79	0.47	0.27	29	209

* Only mS is shown, since the other part of the measured time of the five instruments are the same as 2010-08-09 01:37:57.284.

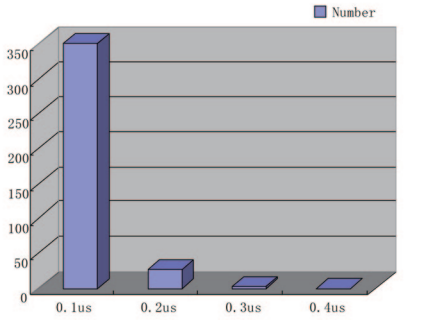
TABLE II. TEST RESULT OF THE SECOND RETURN STROKE

No.	Time*	Angle	Magnetic field intensity	Electric field intensity	Leading edge of lightning	Trailing edge of lightning
0	1.790	194.01	0.43	0.29	21	240
1	1.789	189.21	0.45	0.33	22	243
2	1.789	192.41	0.44	0.32	20	243
3	1.789	187.97	0.40	0.32	21	241
4	1.789	193.96	0.44	0.33	23	259

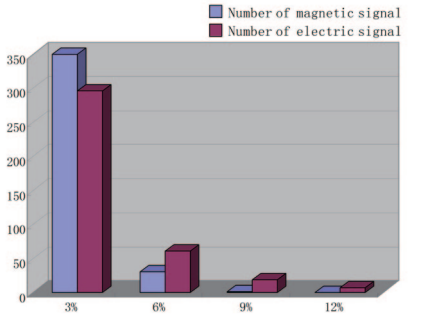
* Only mS is shown, since the other part of the measured time of the five instruments are the same as 2010-08-09 01:37:57.375.

From the above tables one can see, the five lightning detecting instruments have a good consistency for a single lightning. To show the instrument's consistency statistically, 380 data are chosen randomly from the 6083 lightning, and the statistical results of the consistency are drawn in Figure 6.

As Figure 6 shown, on the flash receiving time measure, the 92% data's error is less than 0.1uS, and the 99% data's error is less than 0.2uS. On the magnetic field intensity measure, 92% data's error is less 3%, and the 98% data's error is less than 6%. On the flash pluses of electric field intensity measure, 78% data's error is less 3%, and the 92% data's error is less than 6%. The accuracy of the lightning detecting instrument fulfills the specification. Perhaps the relative low accuracy of the electric field intensity measure is caused as follows. The first reason is that the electric field signal is easy to be disturbed by the background noise. The second one is that the waveform of electric field signal is different with the magnetic field signal, which brings bigger error in waveform judge. The last one is that since the five instruments are lined on the test, the minor differences of the electromagnetic environment between them also bring error.



(a) consistency of arrival time



(b) consistency of magnetic signal and electric signal

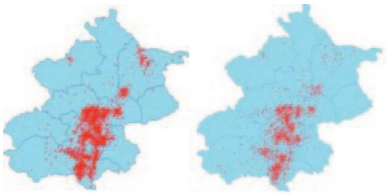
Figure 6. Statistic result of consistency experiment

B. Test of the Network

A test network of the three-dimensional lightning positioning system was setup on July, 2011. The master station was set on the Beijing Meteorological Station in the southern suburb, and five slave stations were set on Fengning, Zhangjiakou, Zunhua, Tianjing and Baoding. The distance between the master station and each slave station is about 150km, which is suitable for a high accuracy.

By the test network, about 200,000 lightning happened have been detected. Through the analysis of these lightning, we find that the highest lighting detect efficiency of the network is near

the master station (station in Beijing). Using the data on 2011-08-26, we verify our test network's efficiency by set the data of China's National Lightning Monitoring Network (CNLMN, A two-dimensional net we mentioned in section I, which is completed in 2007 and it can not detect IC lightning) as a standard. The test network monitored 3202 lightning, while CNLMN monitored only 1921 lightning. The comparison is shown in Figure 7.



(a) data from the test net (b) data from CNLMN

Figure 7. Lightning distribution comparison between the test net and the national net

It shows the lightning distribution regions of the two nets are similar. We believe the extra lightning of the test net is IC lightning, which can not be detected by CNLMN.

To confirm that conclusion, the further analysis is given. Figure 8 illustrates IC flash (the yellow point) and CG flash (the red point) from the data of the test net. In it, there many yellow points upon the red points. It implies the lightning number of the test net (the sum of the yellow points and the red points) shall bigger than the lightning number of CNLMN (the number of the red points), which is compatible with Figure 7.

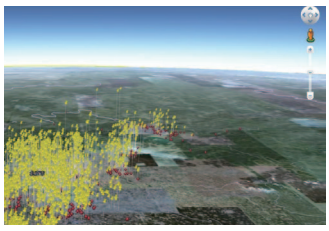


Figure 8. Three-dimensional distribution of the lightning from the test net

As we known, IC flash happens in midair and CG flash happens near the ground. Figure 9 gives a further quantitative research. It shows the height distribution of the lightning. From the statistic, the ratio of the IC lightning and the CG lightning can be known.

From the above analysis, we can affirm that the new three-dimensional lightning positioning network has a good consistency with CNLMN. Besides detect CG flash, it can position IC flash and give the three-dimensional distribution of lightning in a thunder [14], which is a significant improvement for both the lightning study and the thunderstorm forecast.

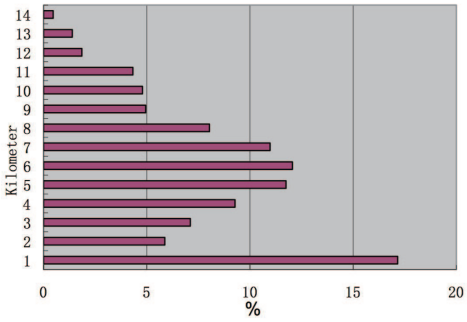


Figure 9. Height distribution of the lightning data from the test net

Besides that, the comparison of the lightning data and the radar echo map also supports our conclusion. The area distribution of the lightning is compatible with the cloud distribution form the radar echo map.

C. Application in thunderstorm forecast

Since the test net's performance has been certificated, a service network is setup on July, 2012. It has 16 lightning detecting instruments in Jiangsu Province. This service net monitored 177940 lightning from 2012-08-15 to 2012-09-15. There were 133598 CG flash and 44342 IC flash, the ratio of IC flash was 24.92%.

Figure 10 gives the lightning data on the south region of the Jiangsu Province. There was a strong thunderstorm in that area at the dusk of 2012-09-08. Follow the above analytical method, we see the data of the national net as CG flash and the data of the service net as the sum of CG flash and IC flash. From it one can see, at the beginning of the thunderstorm, the ratio of IC flash in all lightning is high. With the progress of the storm, the ratio gradually decreased. This trend is compatible with the theory that IC flash happens before CG flash and the decrease of the ratio of IC flash means the enhancement of a thunder [15]. Since IC flash has little influence on people but CG lightning has a heavy effect on our life, so through IC flash monitor by this new three-dimensional lightning positioning system, the disastrous thunders can be forecasted.

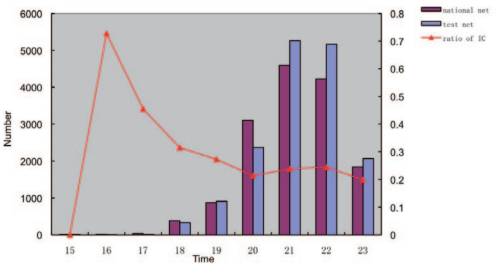
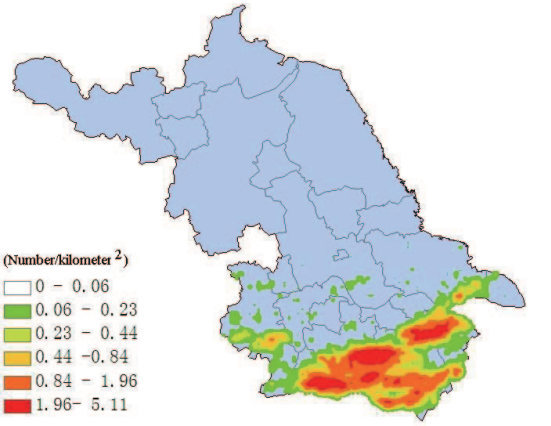
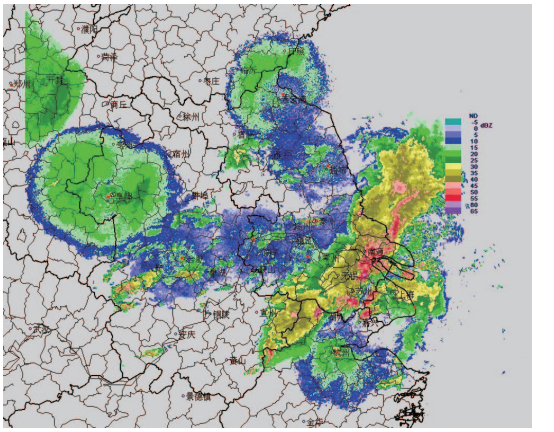


Figure 10. Lightning record of the south Jiangsu Province at 8th Sept. 2012

The comparison of the lightning and the radar echo map in this case also had been done. The area distribution of lightning in Figure 11(a) is compatible with the cloud distribution by the radar echo in Figure 11(b). The lightning happened on the region, in which the radar echo is over 35dBz. For the region that the radar echo is higher than 45dBz, the lightning was intensive. More important, the data of Figure 11 was at the 15:00 pm, 2012-09-08, which is just at the start of the thunderstorm in Figure 10. That supports the three-dimensional lightning positioning system can be used on thunderstorm forecast from another perspective.



(a) lightning distribution map



(b) basic radar reflectivity map of 1.5°

Figure 11. Comparison of the lightning data and the radar echo map

CONCLUSIONS

In this paper, an SOPC-based VLF/LF three-dimensional lightning positioning system is introduced. The system is composed of three-dimensional lightning detecting instruments, a lightning data center and the relative application services. This system ends the history that Chinese lightning detecting cannot monitor the intracloud lightning and cannot measure the three-dimensional position of a lightning.

As the key of the whole system, the three-dimensional lightning detecting instrument is SOPC-based and is implemented on an Altera's Cyclone II FPGA. By the virtue of this platform, the process speed of lightning analysis is increased, the size and the power consumption are decreased. As a result, the stabilization and the reliability of the instrument are improved. Through a series tests, this instrument achieves the international standards.

Besides the above work, we are managing to promote the lightning positioning system in near future. To further improve the positioning accuracy, we are studying a novel positioning technology based on direct 3D least square method. Since the radius of the earth changes with the latitude and the transmission of electromagnetic wave is influent by the surface, the earth's ellipsoid model and the calibration of electromagnetic wave transmission is going to be researched.

The three-dimensional positioning of lightning can be used to analyse the lightning phenomenon. Moreover, combining with the other factors of the weather forecast, the three-dimensional lightning positioning system can monitor the generation, the progress, and the attenuation of a thunderstorm, which is important for both the scientific research and the forecast of the strong convention weather.

ACKNOWLEDGMENT

The research is supported by the National Science & Technology Pillar Program (2008BAC36B05) and the Hubei Provincial Natural Science Foundation of China (2011CDB272).

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3D Position Tracking of Instruments in Laparoscopic Surgery Training

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Abstract — The VR laparoscope surgery training device is for junior hospital students to understand and train the laparoscope surgery. However, those developing training devices use special instruments for their training program, not real instruments. Therefore, this paper developed a surgery instruments' 3D location system for a VR laparoscope surgery training device while using real instruments. Moreover, this paper introduces a new method for hardware design in FPGA. This new method is using MATLAB's tools to develop the algorithm, generating the HDL and verifying the FPGA system. The system in this paper has less 1% error in the central operating area and could calculate two instrument positions every 200ms on the Altera's DE2-115 development platform. Thus, it could be employed in the VR training program.

Keywords — Laparoscope surgery, Laparoscope surgery training, VR Laparoscope surgery, FPGA, 3D locating, HDL coder, FPGA In the Loop, FIL, MATLAB, Simulink

I. INTRODUCTION

The minimally invasive surgery (MIS) is the popular issue in the surgery research, especially laparoscopic surgery. The laparoscopic surgery has lots of benefit for a patient such as reduced pain, smaller incisions and hemorrhaging, and the best advantage - shorter recovery time. However, the laparoscopic surgery is more difficult than traditional open surgery as surgeons cannot directly observe the surgery process directly with their eyes and can only observe the information though the TV monitor captured via an endoscope. Moreover, surgeons need to operate laparoscopic instruments, which are longer and harder for operating compared to traditional instruments. As a result, training a laparoscopic surgeon is very important and there is a need for a suitable training device, too.

In order to addressing the above approach, several researches developed different laparoscopic surgery simulation training systems to reduce the laparoscopic skill's learning time and curve [1]-[4]. The visual reality (VR) simulator is a developing area which provides visual laparoscopic surgery environment and could offer closer training models than traditional box trainer methods [5]-[8]. However, those researches used similar instruments in their training systems but not real instruments. Therefore, this paper introduces a 3D position location method for real instruments in the laparoscopic surgery training system.

This research uses the FPGA Cyclone IV DE2-115 platform which serves as the developing kernel for real-time calculation and cooperation with MathWorks' MATLAB and Simulink[9] for reducing the developing time. Simulink in this system captures two 2D images from the two USB cameras and sends two images to the DE2-115 for calculating the 3D positions of instruments, where

Simulink retrieves position data from the FPGA. After that, Simulink transmits the data to our visual reality laparoscopic surgery training system.

II. BACKGROUND RESEARCH

A. HDL coder & FPGA In the Loop

MATLAB is a widely known software algorithm development tool and can be used in many different areas. Especially, in 2012, the newest MATLAB released two new functions which are HDL coder [10] and FPGA In the Loop (FIL) [11]. HDL coder is a kind of code generator which can convert a Simulink design to portable, synthesizable VerilogHDL and be used in the FPGA design. FIL is a verification tool which can verify the implemented HDL code on FPGA boards. Figure 1 shows the loop of these two functions. The algorithm is designed in Simulink then converted to HDL code. In the end, this generated HDL code is verified in the FPGA in the loop and on hardware platforms, such as the DE2-115.

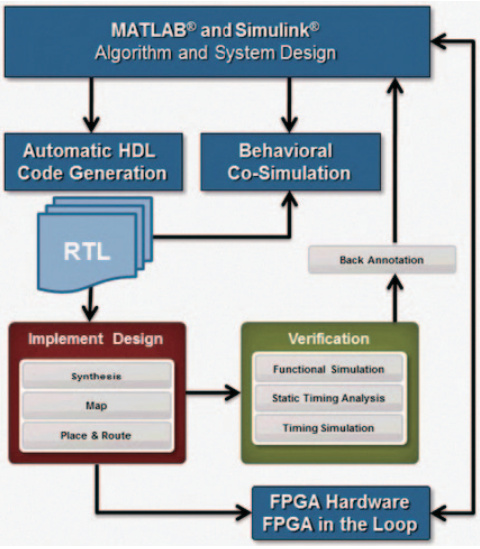

Figure 1. The loop of the hardware algorithm design in the MATLAB [12]

B. 2D to 3D coordinate calculating

This research is based on using two cameras to find the location of instruments which is the technical of 2D to 3D converting. According to stereo imaging theory geometry [13], the 3D point's coordinate could be calculated from two 2D points by formula (1)-(3). Figure 2 displays the simplified stereo imaging system to indicate this principle. The two cameras are similar to human's eyes, having about 6cm distance. The object at (X,Y,Z) point will be captured by this two CCDs at (X1,Y1) and (X2,Y2). After getting position of the two points, the 3D point of the object can be derived.

$$x = b\frac{\frac{X_1 + X_2}{2}}{(X_1 - X_2)} \quad (1)$$

$$y = b\frac{(Y_1 + Y_2)\cdot\frac{f_x}{2}}{(X_1 - X_2)\cdot f_y} \quad (2)$$

$$z = b\frac{f_x}{(X_1 - X_2)} \quad (3)$$

Where the fx, fy are focal length and can be found by using MATLAB's Calibration Toolbox[14].

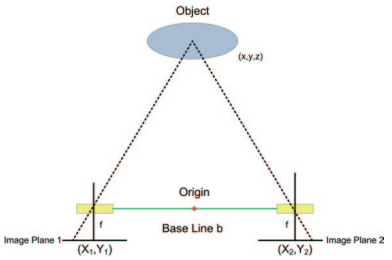

Figure 2. A simplified stereo imaging system

III. SYSTEM ARCHITECTURE

The system architecture is shown in Figure 3. The instruments' photos are taken by the USB cameras and then collected in MATLAB. The MATLAB integrates the FIL interface to transmit data to the FPGA platform, DE2-115 for calculating. In the FPGA, there are image pre-processing parts and coordinate calculating

parts. The pre-processing part includes the color converter, Marker finder and morphology. The coordinate calculating part not only calculates the 2D and 3D coordinates of instruments but also calibrates the coordinates to improve accuracy.

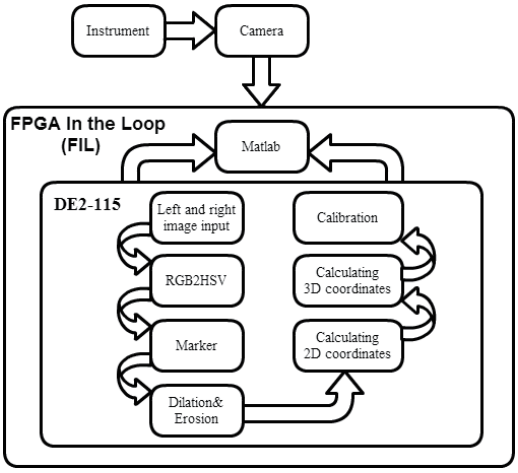

Figure 3. The system architecture of this design

A. Pre-processing part

1) **Instruments & RGB2HSV:** In order to detect the instruments, the instruments have been labled a color sticker as shown in Figure 4. Therefore, the algorithm can identify instruments via different label colors such as red, yellow, green and blue. Moreover, HSV color model means the color is presented as hue, saturation and value, thus it is more suitable for color detection. However the source images are RGB color model therefore the RGB2HSV is used for converting the images from RGB color model to HSV color model.

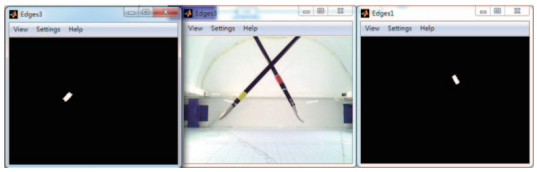

Figure 4. Left: the yellow label's location; Middle: the instruments with label; Right: the red label's location

2) **Marker finder:** After conversion to HSV, the red HSV(0,100,100), yellow HSV (60,100,100), green HSV(120,100,50) and blue HSV (240,100,100) are the basic color data and adopt the range of ±15 for the hue, the range of ±20 for the saturation and value to filtering the different colors in the image. Due to two source images and four colors label, this marker finder block will output eight Boolean data maps for next processing.

3) **Morphology:** The marked Boolean map image still has another problem that is noise.

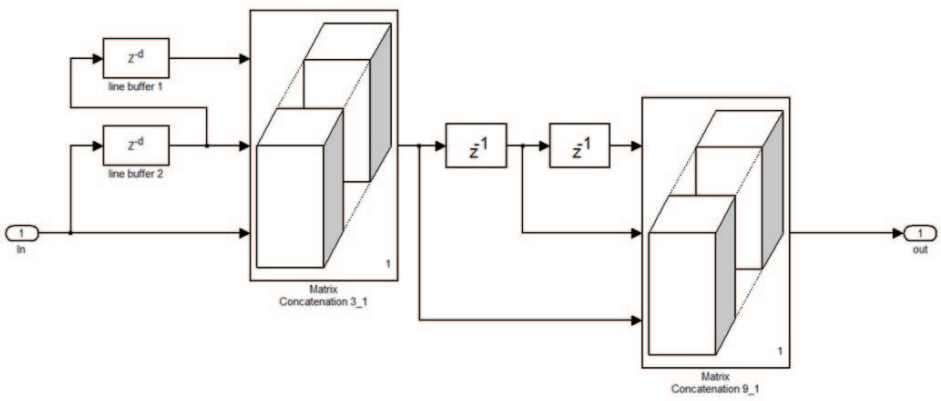

Figure 5. The data restructured to the 3x3 matrix

Although the photo is taken in a stable light source environment, it still can have glitches caused by the CCD sensor noise or other noise sources. Therefore, morphology can solve this problem. Dilation removes the unexpected points then the erosion linking and smoothing the labeled points for further stage.

The dilation and erosion in this design are a 3 by 3 mask but the data from previous stage is a pixel stream. Therefore, the data requires merging to 3x3 matrixes before the morphology. Figure 5 indicates how the pixel stream date be merged to matrix data type. First, the row direction data are delayed for combining to 3x1 arrays. Next, the 3x1 array data are delayed one array for merging 3x3 matrixes.

The Figure 6 demonstrates how the morphology block's function. The noise at upper right is been removed.

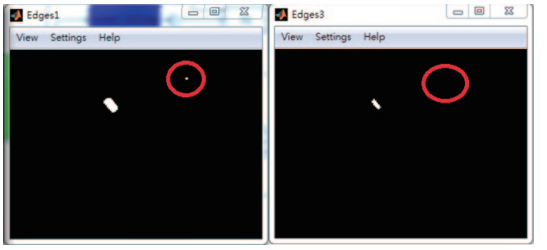

Figure 6. The noise removing by the morphology block

In additional, there are two instruments and four labels in one processing frame that means two 320*240 images and 3 bytes HSV data are compared with four colors mask and then removed noise at morphology block in one frame to find the label. In a software algorithm, the color conversion is pixel by pixel processing which means the two images take two conversion processing. Because there are four colors, the marker finding takes four times for four colors. After marker finding, there are eight Boolean maps needs to be process in the morphology stage. Therefore, these procedures spend much time for pure MATLAB calculation. However, because this design is implemented in a FPGA, the parallel processing could reduce the processing time. The two images are converted in the same time. Also, eight color filters and eight morphology blocks are for the eight Boolean maps' parallel processing. Therefore, the four labels' locating position are calculated out in the same and the processing speed is also increased.

B. Coordinates calculating part

1) **2D coordinates Calculating:** After removing noise, the label's 2D coordinates could start to be located in the Boolean maps. Figure 7 shows how this system finds the label. The truth value is where the label at so this stage could search the truth value area and record the maximum X and Y point also the minimum X and Y point. Then, the central point's (X,Y) should be ((max(X)+min(X))/2, (max(Y)+min(Y))/2). This central point is defined as the label's 2D location in this project. Each label has two 2D locations, because each label has two images. Then, the label's 3D coordinate could be found from the two 2D coordinates.

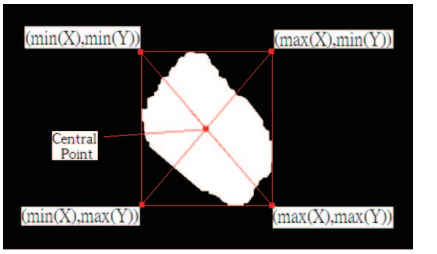

Figure 7. How this system found the central point

2) **3D coordinates Calculating:** This stage is for calculating the four label's 3D coordinate. Last stage has located the label's 2D central points in right and left images. After that, 2D coordinates are substituted in formula (1),(2) and (3) the label's (X,Y,Z) location is determined.

3) **Calibration**: Although the label's 3D coordinate have been observed, the value still

not correct. The curvature of camera's lens may cause this problem and require lens correction. Therefore, this stage is for calibrating the original coordinate and improves the accuracy.

IV. RESULTS

The efficiency is improved by FPGA's cooperation. In the pure MATLAB environment, the throughput of this calculation is about 0.1 frames per second (FPS). On the other hand, the FIL environment raises the FPS to 5 frames. That is 50 times of software's speed.

Figure 8 shows the operating plane's accuracy map. The Blue points are the output of this design and the red points are the standard point. Most points are close to the standard points, however the points at up-right area have more error problem. The maximum error is about 3cm.

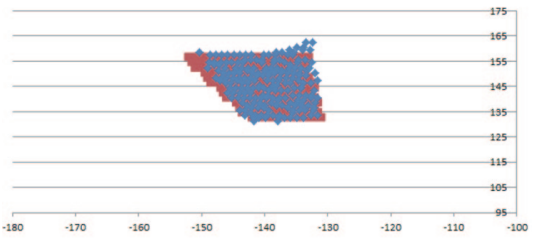

Figure 8. The measured point (blue) VS standard point (red) in the operating area.(X,Y axia is the distance and the unit is CM)

DISCUSSION & CONCLUSION

The accuracy of this system is enough for usage in VR laparoscope training system. The center area has higher accuracy where the error is less than 1% and the surgery area is usually 10*10*10cm therefore the training program could operate at the center area void the error problem.

The 5 FPS calculation time seems to be not quick enough for high speed detection. We deduce the problem may be the communication between MATLAB and FPGA. This design has adopted the parallel blocks to increase the operation and the hardware should have the ability to process the loading. Therefore, the bottleneck probable is the transmitting interface of MATLAB.

This paper firstly designed the 3D coordinates calculating algorithm for locating surgery instruments in a laparoscope training system. Secondly, HDL coder is used to generate the Verilog HDL from the developed algorithm in Simulink. Next, utilization of the FIL is for verification the generated HDL coder and has provided this architecture could be employed in a laparoscope training system.

In the future, generated HDL code can be integrated into a system on programmable chip (SOPC) system for increasing the processing ability such as Altera's Qsys. If the FPGA could control the CCD sensor directly then the data could input to the processing hardware when the data just getting from sensor. Thus, the latency should be reduced and can move from MATLAB's FIL system to a standalone chip. In our estimations, the processing speed could rise to more than 30 FPS. Of course, designer can integrated this SOPC chip with any kind of computer to build a new laparoscope surgery training system.

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Air Guitar on Altera DE2-70 FPGA Architecture

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Abstract — Air guitar is a well-known competition all over the world. It gives us a passion for those who might not play the guitar so well can be indulging in the magic power of guitar as well. However, although one may act so seriously as if he/she has a guitar, the sound would never be produced. Therefore, by capturing the user's movement, we proposed a real-time and equipment-free system to make air guitar not only acting but also an alternative and user-friendly way to play the guitar.

Keywords — Air Guitar, FPGA, Real-Time, Gesture Detection

I. INTRODUCTION

Worldwide air guitar competitions are regularly been held in many countries for years. An "air-guitarist" does not play a real guitar. Instead, he attracts audience by exaggerated motions pretending he is really playing something, together with pre-recorded rock or heavy metal-style music, dazzling lights, and loud singing or lip-synching. Nevertheless, as we have just mentioned, an air-guitarist can only play pre-recorded songs, and thus limiting his performance only a kind of dance. What we are going to do is to endow an air-guitarist the capability of playing a tune impromptu. Besides, we also transform the complicated fingering into simple hand gestures so that even the ones who have never learnt how to play a guitar can easily play our design.

In 2005, students from Helsinki University of Technology developed a system, which translates a performer's hand movements into sounds by recognizing a pair of gloves of specified color via video camera. Today this system is exhibiting at the Helsinki Science Center, and for more details, you may refer to [1] and [2]. Later in 2006, Australian researcher Helmer et al developed Smart Textiles [3], which can be used to sense human movement by embedding sensors within clothes. Its application to the air guitar is an "Air-guitar T-shirt". In 2007, Japanese company Takara Tony introduced a product called "Air Guitar Pro" [4], which is a small device imitating the guitar neck with numerous buttons on it. A performer takes it and selects the tones via the buttons. Besides, there are infrared motion sensors on the bottom of the device, acting as virtual strings, and a performer is able to wave his hand by the sensor to play sounds. Recently, there are also some air guitar applications on the Microsoft Kinect or Apple iOS devices [5], however their functions are limited owing to their frameworks.

We are going to implement our air guitar system on the Altera DE2-70 FPGA architecture. The performer's motion will be captured by a video camera, and then be processed by hardware-level image processing and recognition techniques, which is similar to Helsinki students' work in [1] and [2]. However, we do not require users to wear gloves with specified colors, but detect the skin color instead. Furthermore, our system is able to recognize various hand gestures and performers can easily play music of different styles precisely.

This paper will be organized as follows. First, in section II, we are going to give a detailed description to the features of our system, including a simple tutorial to play our air guitar. Then, starting from section III, we are going to illustrate the technical details, such as platform, system architecture diagrams, and the detailed algorithms applied in each functional block. In the end, we will briefly give the usage of the resources on the FPGA board and then give a conclusion to our design.

II. FUNCTION DESCRIPTION

The Air Guitar aims to provide a new interface for the user who has never played a guitar before to play a virtual guitar like real. Therefore, it is necessary to give the user an experience analogue to how a guitar is played in reality. After observing how one actually plays a guitar, we concluded that the completeness of the guitar performance composes of three parts which include finger positioning, strumming and sound generating from the body. As a result, we designed these parts individually in order to meet our requirements which we mentioned above. That is, we aim to make playing air guitar like real.

The main components are gesture detector, motion detector and audio synthesizer corresponding to finger positioning, strumming and sound generating, respectively. We will give a brief introduction to them as following:

A. Gesture Detection

Guitar is so popular for its ability to play plentiful chords and notes for an accompaniment. The basis of a guitar to be diversifying is the six chords on the neck. The fingers' position for each chord gives a variety of chords. However, it is hard for new comers to memorize so many chords and position the fingers correctly. Therefore, we simplified the gestures so that everyone can play Air Guitar in a very simple way. We support up to twelve different gestures which represent to twelve kinds of chords and notes in Figure 1 (a). To detect the gesture, we may put our left hand in a specified detection area where we recognize which gesture it is.

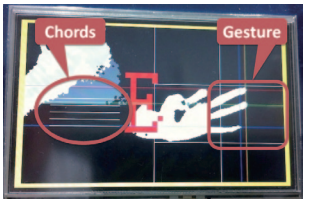

Figure 1. left (a) and right (b)

B. Motion Detection

The most fascinating part when playing a guitar is strumming through the chords and making a harmonious sound. There are 5 thin detection bars which are shown in Figure 1 (b) for our right hand to strum through. Therefore, we may generate sound through 5 detectors and each simulates an independent chord. The sound from them then composed to be a chord, e.g. C major.

C. Audio Synthesizer

It takes two steps for a guitar to make sound which are the vibration of the steel chords and the resonance of the body. This results in a special sound for the guitar. Therefore, to synthesize the sound of the guitar, we need to make the amplitude curve, waveform and pitch to be similar enough as it really is. The audio synthesizer is specially designed to generate a single note of the guitar sound with different pitches. As a result, we may use it to generate a variety of chords by different combinations.

D. Instruction

We can see from Figure 1. To play with the Air Guitar, we simply need both of our hand, one to change gesture and the other to strum the

chords. As show in the display panel, there are two regions. The gesture detector is located in the right area and the motion detector is in the left area with five chords. We need to change our left hand gesture according to Figure 1 to get different kinds of chords and in the meantime strumming our right hand on the other region to get sound. In addition, we may choose single note mode and chords mode to play with more fun. From description above, we have proposed a guitar-free performing system which gives the same user experience as playing it real.

III. ENVIRONMENT & COMPONENTS

Our system is based on the Altera Cyclone II EP2C70 FPGA built on the DE2-70 board. A 500-megapixel D5M camera with 2560×2160 full-resolution is used to capture the performer's motion, and a LTM LCD is for the display with the SDRAM on the DE2-70 board. Besides, the synthesized audio is output to a speaker via the DAC on the DE2-70 board. In addition, in order to make our system work more accurately, sometimes we need some fill lights when the environment light source is not homogeneous.

Figure 2 is the compilation result of our implemen-tation. The compiler we used is Quartus II 10.0. About 21% of logic elements on the FPGA are used.

Flow Status	Successful - Tue Aug 21 19:52:00 2012
Quartus II Version	10.0 Build 218 06/27/2010 SJ Full Version
Revision Name	DE2_70
Top-level Entity Name	DE2_70
Family	Cyclone II
Device	EP2C70F896C6
Timing Models	Final
Met timing requirements	No
◢ Total logic elements	14,559 / 68,416 (21 %)
Total combinational functions	13,836 / 68,416 (20 %)
Dedicated logic registers	2,781 / 68,416 (4 %)
Total registers	2819
Total pins	530 / 622 (85 %)
Total virtual pins	0
Total memory bits	131,240 / 1,152,000 (11 %)
Embedded Multiplier 9-bit elements	41 / 300 (14 %)
Total PLLs	2 / 4 (50 %)

Figure 2.

IV. SYSTEM ARCHITECTURE

In this section, we are going to introduce the design architecture of our system. Figure 3 (a) is the data flow diagram, which provides a simple view to our design. Figure 3 (b) is the detailed system diagram, in which the relationship between each functional block is shown. Our system is composed of three stages, the Pre-processing Stage, the Detection Stage, and the Synthesizing Stage. We are going to give a brief introduction to each stage in the following part.

A. Pre-processing Stage

In this stage, the video signals are being processed to the format that can be dealt with in the next stage. First, the video frames are captured from the D5M camera and down-sampled to 800×600 resolution with 30-bit RGB color space. Then, the video frames are being sent to the skin detector. In the skin detector, heuristics are applied for determining the skin color parts on each frame. After that, the result is filtered to remove noises and interferences so that the detectors in the next stage are able to make their decision based on the clear skin color information.

B. Detection Stage

In this stage, there are various kinds of detectors to figure out what kind of moves the performer is doing. A motion detector is a functional block that detects whether the performer is waving his right hand over the virtual strings. Each virtual string is implemented as an independent module. A gesture detector recognizes the performer's gesture of his left hand, and is composed of four parts: finger detector, palm detector, thumb detector, and a decision agent that collects the information from the previous three parts. Next, their results are sent to the next stage, the synthesizing stage.

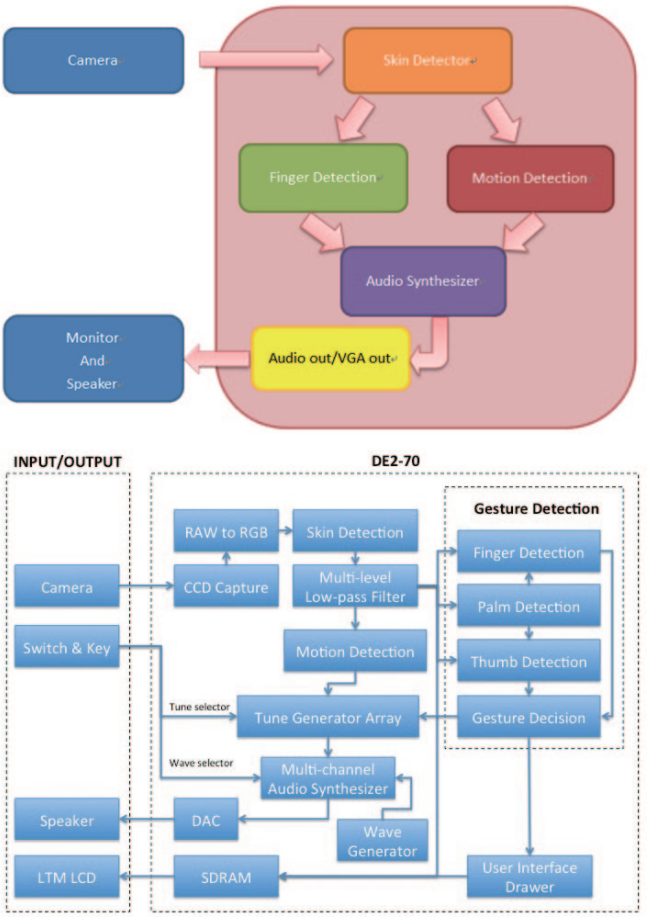

Figure 3. top (a) and bottom (b)

C. Synthesizing Stage

The audio synthesizer generates the tones and output via the DAC and then to the speaker. Just as we have mentioned in the previous sub-section, each string is implemented as an independent module. As long as the user waves his hand over a virtual string, the corresponding motion detector attracts it and then triggers a tune generator. A tune generator will decide the physical properties according to the information given by the gesture detector. After that, the module audio synthesizer collects the information from the tune generator array and then synthesizes the sounds.

V. SKIN DETECTION ALGORITHMS

A. Skin Detection Heuristic

The video frames captured from a D5M camera is firstly transformed into 30-bit RGB color space, in which 10 bits ranging from 0 to 1023 represent each color. In such a color space, we follow the heuristic rule to determine whether a pixel is of skin color.

$$R > 380 \;\&\; G > 160 \;\&\; B > 80 \;\&$$
$$R > G \;\&\; R > B \;\&\; R - G > 60 \;\&$$
$$R - B > 60 \;\&\; (B < 550 \mid R - B > 320)$$

The heuristic is based on [6] and is modified to adapt the skin color of Asian.

B. Filtering

However, we found that with only this heuristic, the noises and interferences will deeply affect the precision of the gesture detector. We apply a filtering scheme, which we call it "multi-level low-pass filter", to eliminate its effect.

The filtering scheme is composed of many levels. In each level, every pixel in a given frame is compared with its eight adjacent pixels which is shown in Figure 4. If there are more than six of them are of skin color, then the pixel is claimed as a skin-colored pixel. The reason for adopting this scheme is that, we find out that pixels of skin color detected from real skin tends to be gathered as a cluster, while skin color pixels from noises and interferences are usually separated as small pieces.

The process mentioned in the above part is done for three times. According to our experiment, repeating the process for three times can filter out about 80% of noise and interference in most cases. And this is the reason that we call this process the "multi-level" filtering.

+1	+1	+1
+1	0	+1
+1	+1	+1

Figure 4.

Figure 5. left (a), middle (b), and right (c)

VI. GESTURE DETECTION ALGORITHMS

The gesture detection algorithm we designed is real-time and non-buffered. Therefore, the algorithm responses fast and it requires no extra memory. The gesture detector is composed of four minor building blocks, which are palm detection, finger detection, thumb detection, and gesture decision. In the gesture decision block, it will collect the information generated by the previous three parts and then make a final decision of which gesture the user is making.

A. Palm Detection

The main purpose of the palm detector is to identify the upper and bottom boundary of a palm. Let us first learn how the video signal is read in. The video signal is read sequentially from left to right as a line, and up to down line by line. Thus, we count the number of skin color pixels in each line. By heuristic, the palm area is defined as the lines with more than 80 skin color pixels. Hence, we are able to find the upper boundary of the palm, which is the first line of the palm area that exceeds the threshold, and we may find the upper y-coordinate of palm. Similarly, the bottom boundary, which is the last line of the palm area, is the lower y-coordinate. The result is shown Figure 5 (a).

B. Finger Detection

The work to detect finger gesture is a relatively hard work. However, for the gesture we defined, they are particularly in the same direction as we showed previously in Figure 1 (a) and the difference between each gesture is basically the number and the presence of fingers. Therefore, we may add the constraint of hand orientation to make the detection in a predictable way. Moreover, we try to reduce the problem to fingertip

identification. The finger detection algorithm has two steps, interest peak identification and fingertip detection policy. In the first step, we are trying to find out all the possible candidates of fingertips. And in the second step, we try to rule out all the misclassified fingertips.

To achieve the first step, we first find the rightmost (largest x-coordinate) skin color pixel in each scanning line. Next, we will compare these rightmost pixels to find interest peaks. The peaks are illustrated in Figure 5 (b). In this step, we may observe that there are still many misclassified fingertips.

In the second step, we set up a policy with two rules to eliminate the wrong fingertips. The first rule is that the difference of y-coordinate between identified peaks must exceed 15 pixels. That is, two peaks which is close in the y-direction should only be counted once since there exists a least distance between two fingers. The final rule is that fingers should have similar x-coordinates except for the little finger when the hand is oriented in the desirable way. As a result, we may see that misclassified peaks are eliminated in this case. The result is shown in Figure 5 (c).

C. Thumb Detection

The purpose that we designed an individual detector for thumb without detecting it in the finger detection is that thumb has a distinct orientation compared to the others. Therefore, we develop another way to deal with thumb. Contrary to finding peaks, thumb detection is trying to count the number of skin color pixels in the thumb area which is the area above the upper boundary of the palm we've been detecting continuously. If the number exceeds a threshold, the thumb is said to be raised. Together with the finger detection, we may support 12 different gestures.

D. Gesture Decision

From the information above we may make a decision for the gesture. The resulting gestures are shown in Figure 1 (a) and the supporting chords and tones are shown in Figure 6.

Chords	Tones	Chords	Tones
C	B.	A	C7
D	C	B	Dm
E7	D	C˙	Em
F	E	D˙	Fmaj7
G	F	E˙	G7
Bm	G	F˙	Am

Figure 6.

VII. MOTION DETECTION ALGORITHMS

To detect the motion of hands, we don't need too much information of the shape and gesture. All we need to do is to detect well on whether a hand actually strum through it. That is, we need each motion to be detected rapidly. On contrary, the detector should detect nothing when there is no hand over it. To meet the requirement we designed a module which checks a specific region at each frame. When the number of the filtered skin color pixels in the region exceeds a threshold, the region is set to be in "covered" state. On the other hand, as the number doesn't the threshold, it is set to be in "uncovered" state. Furthermore, the sound is played if the state transition satisfies from "uncovered" to "covered." The reason is that it is accordance to a chord is really plucked. In addition, the threshold is acquired in a heuristic way. Moreover, the process is non-buffered since we check each horizontal line in each scanning. As a result, the reaction time is rapid and can be said to be real-time.

VIII. AUDIO SYNTHESIZER

We generate the sounds by using a synthesizer instead of recording them in advance. In order to simulate the sounds of a guitar, we generate them according to their physical properties, the timbre, pitch, and the amplitude curve. Besides, each virtual string is implemented as an independent module, which is called a tune generator, and the physical properties are adjusted in it.

A. Timbre & Pitch

Physically, to generate a sound, we have to know its timbre and pitch, or waveform and frequency, in academic terms. Given a waveform in a period, theoretically we are able to generate the sound of any frequency. In digital systems, a waveform is represented as a series of samples over a discrete-time scale. Consider such a periodic waveform of frequency f, given the sampling period T_s, the phase difference between consecutive samples is $2\pi fT_s$. Suppose there are N samples in a period, and we are going to generate a sound of frequency f, we must play the waveform within the time T=1/f, and thus we have a sound with sampling frequency Nf. This means that to play the generated sound with the sampling frequency $1/T_s$, we can just simply down-sample the sound with the sampling frequency Nf.

In our system, we describe the waveform as 64 samples and store them in the module wave generator. Though there are some errors owing to the implementation limitation, the pitch of each tone has been carefully tuned by a tuner, and is made sure that the chords sound harmonically to human ears.

B. Amplitude Curve

According to [7] Curve, source not found], the amplitude curve of a guitar sound can be modelled as exp(k/t), as shown in Figure 7. Further, we can approximate it into two linear parts. The first part is about the 0.3 seconds from the beginning, in which the amplitude diminishes really fast, where the second part lasts from the 0.3 second and decrease on a relatively slow rate. At the end of the first part, the volume is about only one-eighth compared to that in the beginning. We follow this rule to generate the sound. When a second sound is played before the first sound ends, the amplitude curve is reset to the beginning state, which means that a new waveform will overlay the original one.

C. Mixer

There are five virtual strings in our system. Since each string is implemented independently, as we have mentioned in the previous sections, we need a mixer to integrate the five channels. The mixer formula is designed with some considerations. First, we must avoid overflows. Second, owing to the characteristics of human ears, the sounds with higher frequency tend to be louder even if the volumes are identical, they must be weakened. Suppose $\{S_k\}$ is the strength of the sounds in the five channels, on the increasing order of the frequency. The mixer formula is given as the following heuristic:

$$m = S_1 + \tfrac{3}{4} S_2 + \tfrac{1}{2} S_3 + 3/8 (S_4 + S_5)$$

You may notice that this formula is not normalized. In fact, the result is right-shifted so that overflow would not occur.

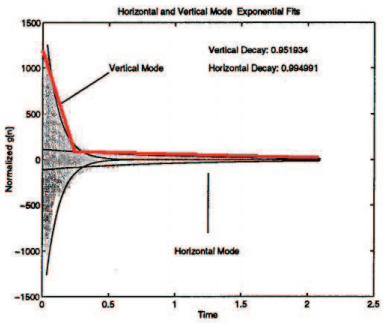

Figure 7.

CONCLUSIONS

With all the detection techniques discussed above and the synthesis of guitar sound, we proposed a real-time, non-buffered and equipment-free Air Guitar system to give users a new experience playing the guitar with bare hand and easy gestures.

ACKNOWLEDGMENT

We wish to acknowledge Altera® Inc. and Terasic® Inc. for their sponsor and hard works holding the competition which provides us with a chance to learn from the project. In addition, we also wish to acknowledge Professor Shao-Yi Chien and National Taiwan University for providing us with a very good environment and training.

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Autostereoscopy Image Display System

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Abstract — The proposed work presents a naked eye 3D display technology programs, including the holographic video acquisition subsystem and 3D rectangular pyramid holographic imaging subsystem. The holographic imaging acquisition subsystem consists of two DE2-70 multimedia development boards which implement real-time multi-angle acquisition of data video and the compositing and output of holographic video; the 3D pyramid holographic imaging subsystem uses the see-though material as the display media. The output holographic video of HVAS is projected onto the respective sides of the quadrangular and then floated image with a 360° viewing range in the quadrangular pyramidal internal. Hence, this display program perfectly matches with the real environment and creates living and stunning visual effects.

Keywords — 3D Pyramid hologram, DE2-70, VIDEO PROCESS, NTSC, MULTI-PORT-SDRAM

I. INTRODUCTION

A. Design Purposes

Human demand is the original motivation for the development of science and technology. In the field of display, 3D technology can truly reproduce the original appearance of world, giving us the immersive visual feast. The strong curiosity of human to restore the real world and the innovative spirit has been accelerating the development of 3D display technology. The current mainstream 3D display technology includes grating 3D display, integrated imaging 3D display, holographic 3D display and so on. The present work gives a naked eye 3D display technology programs, including the holographic video acquisition subsystem and 3D pyramid holographic imaging subsystem. The holographic imaging acquisition subsystem consists of two DE2-70 multimedia development boards which implement real-time multi-angle acquisition of data video and the compositing and output of holographic video; the 3D rectangular pyramid holographic imaging subsystem uses the see-though material as the display media. The output holographic video of HVAS is projected onto the respective sides of the quadrangular and then floated image with a 360° viewing range in the quadrangular pyramidal internal. So it matches the real environment perfectly and creates vivid, stunning visual effects.

B. Application Scope

As a new display medium, the proposed work has a competitive cost and stunning visual effect. So it can be widely used in the information display occasions in business, teaching, medical, communications, industrial and agricultural production, such as, luxury, relics and art works displayed,3D film production, mold making and digital city map.

C. Reasons for Using Altera Components

As we all know, there is a lot of rich multimedia, image processing hardware, software resources, teaching materials and a variety of illustrative

example on DE2-70 multimedia development platform. We thought it would be the ideal solution for handling multimedia applications. In addtion, in a very short time can we achieve our vision and complete the work.

Moreover, SOPC structure is quite flexible and can be customized on demand from the user peripherals of Avalon switch. We can adjust our own system requirements, such as multi-CPU, customized instruction set and hardware accelerators, in order to meet the designed performance requirements for both current and future.

II. FUNCTIONAL DESCRIPTION

As shown for the high-level illustration of our hardware design and organizationin Figure1, the main function of the proposed work includes the browsing and acquisition for static holographic images, the synthesis and playing for the real-time holographic images.

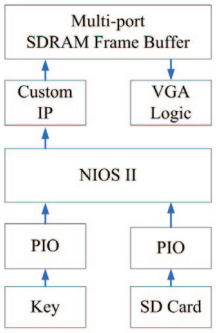

Figure 1. Function block diagram of the static holographic image browsing

With PIO core, we simulate how SPI communication reads the 3D pictures stored in the SD card. User-defined IP core sends the image data to multi-port SDRAM Frame Buffer, and then VGA control logic is responsible for reading and displaying data from the SDRAM Frame Buffer. KEY browses the next picture by PIO interrupt.

A function block diagram for acquisition, synthesis and playing real-time holographic image is shown in Figure2 as follows.

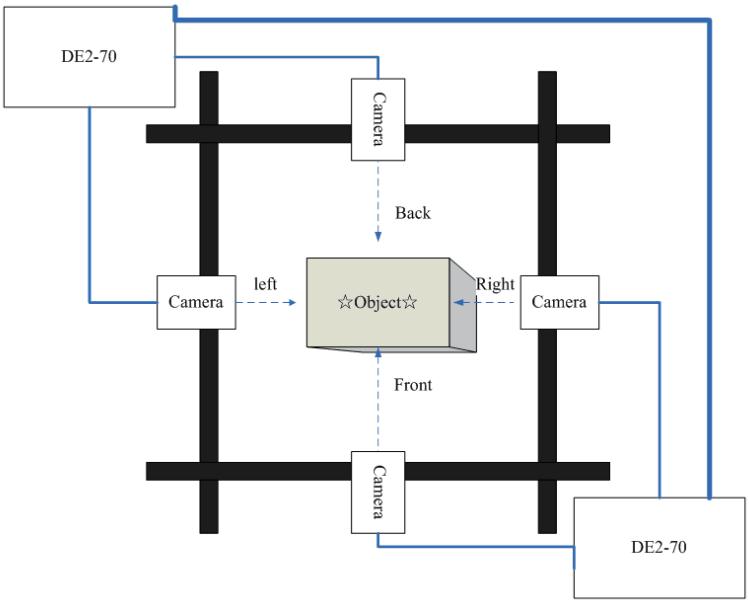

Figure 2. Function block diagram of acquisition, synthesis and play real-time holographic image

The two pieces of DE2-70 multimedia development boards work together, acquiring real-time four-channel camera data from all around, synthetizing 3D video source synchronously, and writing to multi-ported SDRAM Frame Buffer. The VGA control logic is responsible for reading data from the SDRAM Frame Buffer and then displaying them. While, KEY controls the display mode.

III. PERFORMANCE PARAMETERS

A. Image Parameters

- Input original image formats: NTSC system
- Output image formats: 30-bit RGB format
- Input image resolution: 640 × 480 pixels
- Image Color: 30-bit color
- Aspect Ratio: 4:3

B. SD Card Parameters

- SD card capacity: 2GB
- SD card file system: FAT16 file system
- SD card read speed: 165.9KBps

C. Auxiliary Resources

- SD card: 2GB Sandisk SD card
- Projection equipment
- Camera: Four 540 lines NTSC Television System
- Stent and background
- The rectangular pyramid holographic projection film

IV. DESIGN ARCHITECTURE & DESCRIPTION

The principle of the proposed work includes the following two parts:

A. Pyramid Holographic Film Frame

The 3D pyramid holography is shown in Figure 3.Each side of the pyramid is made of half inverse semi-permeable materials in the form of isosceles triangle and shows a 45 degree angle with the bottom surface. Hence each side functions to map the four different screen of 3D video source, respectively.

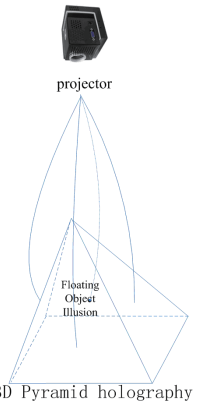

Figure 3. The 3D rectangular pyramid holography

B. 3D Video Source

The production of 3D video source is one of the key of the whole system. By hardware and software means, 3D picture is broken down into four different side of the screen, proceed the frame synchronization synthesis, and then output the video. Four screens in a cruciform arrangement as shown in Figure 4 can realize the synchronous display for four sides of the 3D model screen.

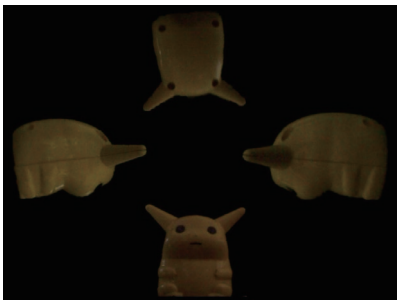

Figure 4. 3D model screen is broken down into four different sides of the screen broken down in a cruciform arrangement

1) Analyze DE2_70_TV module and grasp the NTSC video signal acquisition, processing, and realization method of the VGA display.

The following block diagram and the description of DE2_70_TV design as shown in Figure 5 are taken from Altera's DE2_70 User Manual.

Figure 5 shows the block diagram of the design. There are two major blocks in the circuit, called I2C_AV_Config and TV_to_VGA. The TV_to_VGA block consists of the ITU-R 656 Decoder, SDRAM Frame Buffer, YUV422 to YUV444, YCrCb to RGB, and VGA Controller. This figure also shows the TV Decoder (ADV7181) and the VGA DAC (ADV7123) chips used.

As soon as the bit stream is downloaded into the FPGA, the register values of the TV Decoder chip are used to configure the TV decoder via the I2C_AV_Config block, which uses the I2C protocol to communicate with the TV Decoder chip. Following the power-on sequence, the TV Decoder chip will be unstable for a time period; the Lock Detector is responsible for detecting this state.

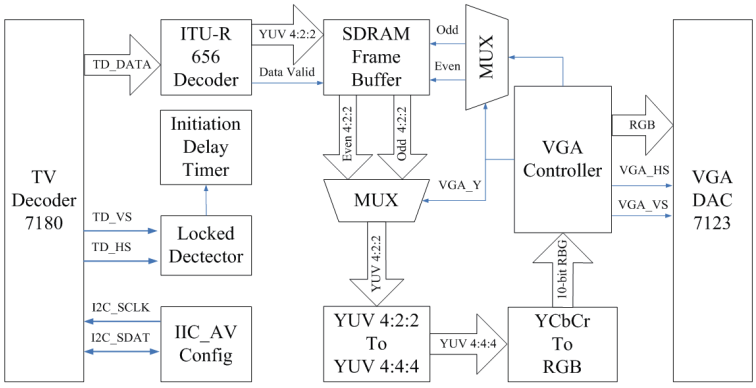

Figure 5. The block diagram design of one-channel

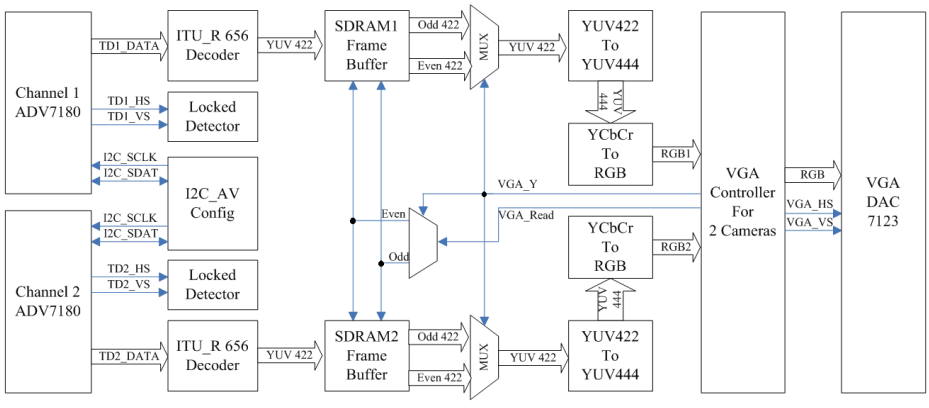

Figure 6. The design schemes of two-channel

The ITU-R 656 Decoder block extracts YCrCb 4:2:2 (YUV 4:2:2) video signals from the ITU-R 656 data stream sent from the TV Decoder. It also generates a valid control signal indicating the valid period of data output. Because the video signal from the TV Decoder is interlaced, we need to perform de-interlacing on the data source. We use the SDRAM Frame Buffer and a field selection multiplexer (MUX) which is controlled by the VGA controller to perform the de-interlacing operation. Internally, the VGA Controller generates data request and odd/even selected signals to the SDRAM Frame Buffer and filed selection multiplexer (MUX). The YUV422 to YUV444 block converts the selected YCrCb 4:2:2 (YUV 4:2:2) video data to the YCrCb 4:4:4 (YUV 4:4:4) video data format.

Finally, the YCrCb_to_RGB block converts the YCrCb data into RGB output. The VGA Controller block generates standard VGA sync signals VGA_HS and VGA_VS to enable the display on a VGA monitor. For more detailed information, please refer to Altera's DE2-70 User Manual.

2) Similar to the DE2_70_TV example, we can realize the acquisition, processing and the VGA synchronous display for 2-channel video signal. The design schemes are detailed in Figure 6.

Different from DE2_70_TV example, proposed work uses the same clock to read video data from 2 pieces SDRAM Frame Buffer synchronously, modifies the VGA logical display, and realizes single-channel video display, switch and synthetic display.

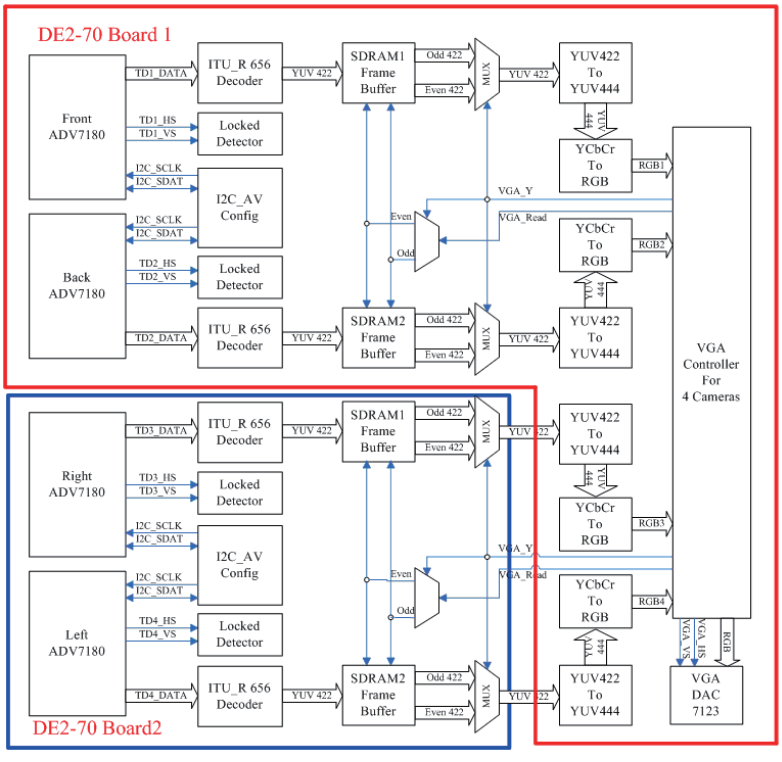

Figure 7. The design schemes of four-channel

3) Using the two pieces of DE2-70 development boards, we can realize the acquisition, processing and the VGA synchronous display for the 4-channel video signal. An implementation block diagram is shown in Figure7.

Unlike the 2-channel video signal processing, the 4-channel video signal processing uses the extended GPIO port to transport synchronous control signal and video data between two pieces of DE2-70 development boards.

4) 3D video source synthesis. In order to synthetize 3D video source, you need to arrange the four-channel pictures into cross-shaped on VGA monitor. Specific display area is shown in Figure8:

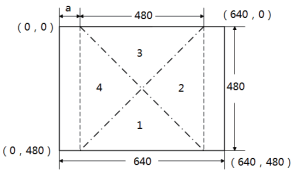

Figure 8. Area partition

The relationship between the pixel coordinates of the respective areas is as follows:

```
Parameter  a = 80;
Parameter  b = a+480;
if ((oCurrent_X < a ) | | (oCurrent_X > b )) //Blank area
else if ( oCurrent_Y>oCurrent_X-a )  // 1 area or 4 area
          begin
            if ( oCurrent_Y+oCurrent_X> b ) // 1 area
            else                            // 4 area
end
else   // 2 area or 3 area
          begin
            if ( oCurrent_Y+oCurrent_X> b ) // 2 area
            else                            // 3 area
          end
```

VGA output data can flexibly switch between the 4-channel video source data in terms of the position of the pixel coordinates.

5) Background eraser algorithm. In order to achieve a better display, we introduce a simple background eraser algorithm. The specific method is: pre-shoot a background in SDRAM Frame Buffer, make the XOR calculation for background and video data capurted in real time, and control the display output threshold in order to eliminate environmental interference.

6) The synthesized image is projected onto a pyramid imaging. In the process of pyramid production, we have tried plexiglass and see-though membrane materials. In the actual test, each side of the plexiglass has a certain thickness, resulting in the imaging ghosting. Eventually we chose see-though membrane material to produce pyramid in order to achieve a better display effect.

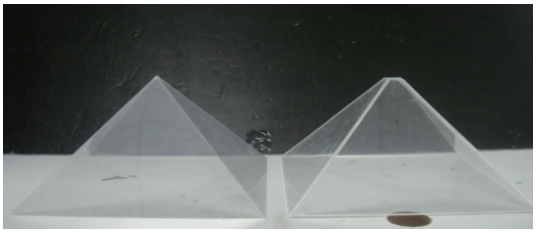

Figure 9. See-though material

V. DESIGN FEATURES

The involved features of the proposed work mainly include:

A. Camera Array

In order to truly represent 3D objects, the proposed work designs a camera array structure, taking pictures from the four directions around the same object, and then providing the signal source for the follow-up image synthesis algorithm.

B. The hardware implementation of image processing algorithms

To ensure the stability, trueness and smoothness of the 3D effect, the proposed works realize

module of image processing algorithms with the hardware description language.

C. Rectangular Pyramid Display Medium

Based on the principle of optical imaging, the proposed works break the shackles of the traditional 2D flat panel display medium and succeed in making the rectangular pyramid display medium, and resorting to the see-though material (computer the Screensavers film). Audiences are able to see images synthesized from each side of the four-sided pyramid, and enjoy the true 3D stereo effect without any auxiliary means (such as 3D glasses).

D. SD Card Browser

In order to easily show, the proposed work has the picture browsing function with SD card. 3D video source files stored in the SD card can be played .

CONCLUSION

The present solution scheme is based on FPGA design using SOPC technology, realizing the image processing and display, and SD card picture browsing function. Because of the high requirements of the real-time processing, the image information acquisition, processing, buffer and display are realized not by software but by hardware circuit module. NIOS II processor is responsible for sending various commands in order to control a variety of peripherals and to coordinate the work between different modules. Combining innovative thinking of SOPC design with the use of NIOS II processor, our works improve the flexibility of the design of system control, reduce the design burden. Hence, a platform could be built more rapidly based on the present solution scheme.

NIOS soft-core processor is an innovative idea for embedded system design. After a few months of practice, we fully appreciate the NIOS soft-core processor as a powerful embedded processor. In the SOPC Builder design system, the user can customize system components in accordance with the system requirements, while the development tools provide many of the most common IP cores for users to directly call. In addition, it also allows users to add custom peripherals in order to simply system hardware design. As a result, we can concentrate on the system function development and algorithm design, which greatly benefits to increase the efficiency of system design .

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Design and Development of 3D Motion Sensing Gaming Platform using FPGA

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Abstract — The most advantage of FPGA is its hardware/software co-design. Based on this advantage, we can make full use of hardware pipeline, multi-core architecture, hardware acceleration technologies to accelerate their applications, in order to mitigate or completely solve high real-time, multi-tasking, big data and a series of other problems. This design aims at completely achieving a 3D Motion Sensing Game System on the FPGA platform. The game system has to support voice and image output, and collects the real-time in-motion data wirelessly through sensors in the mobile phone to produce human limb movement instruction for game control.This system is multi-tasking, massive data and strict real-time. The final results show that the game system designed with FPGA technology, not only runs smoothly, fast response time, but also has good scalability, the ability to easily maintain and upgrade, and therefore has a very good prospect.

Keywords — FPGA, motion sensing game, hardware/software co-design, hardware acceleration, CG

I. INTRODUCTION

It is a big challenge to design 3D motion sensing games for general embedded playform. An excellent game should has efficient and engaging game mechanic, as well as the fluid interactions and real-time response. Therefore, it is a multi-tasking, a large amount of data, real-time system.

1) **Multi-tasking:** Image display, voice output, game scene rendering, sensor data acquisition and analysis. These tasks must be handled in parallel, otherwise it will be difficult to maintain the fluency of the game.

2) **Large amount of data:** Mainly in two points. The first is the need to continuously refresh the screen. Supposing the refresh rate of 60Hz, the data to be read is about 640 * 480 * 4 * 60 = 70M bytes per second . The other point is the need to constantly redraw the animation of the game. In order to keep the game smooth animation, the frame rate (FPS) is at least 30 per second and the data to be written is about 640 * 480 * 4 * 30 = 35M bytes per second. It is difficult for a normal low frequency embedded systems.

3) **High real-time:** The game system will inevitably require friendly human-computer interaction and quick response and action. Sound and images should not have delay and distortion. Therefore not maintaining high real-time nature, the game will not be able to ensure the quality of the game.

FPGA technology has intrgrated the respective advantages of software and hardware to get the highest fluency game experience. Logic complexity and less time-used task can be considered to be implemented in software. But to the time-consuming task with relatively simple logic module, hardware implementation is better, such as high-volume data transmission.

FPGA hardware acceleration's core meaning is that it can be completely independent of a single CPU to build a multi-core system, that is, to build a multi-tasking real parallel environment, rather than a virtual parallel environment which is a timeshare multitasking system in fact. There are many foreseeable problems in this project, such as multitasking requirements of the system, large data processing, demanding strict real-time systems and so on, but all can be solved one by one.

II. ARCHITECTURE

The system will implement a 3D bowling game. The hardware components have five parts: Android phone, BT5701 (Bluetooth wireless serial communication adapter), DE2-70, monitors, speakers, as shown in Figure 1.

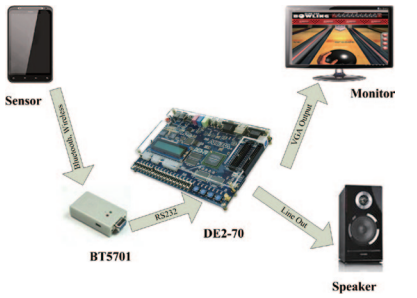

Figure 1. Architecture of game system

This game not only support the basic elements of a bowling game, such as scoring, per-ception of dynamics, movement trail of the ball, the final status of the bottles, etc, and also offers a variety of game options. For example, you can choose two different game scene, and two-player mode or single player mode. In order to enhance the entertainment value of the game, the system increases the function of pitching rating and pitching tips.

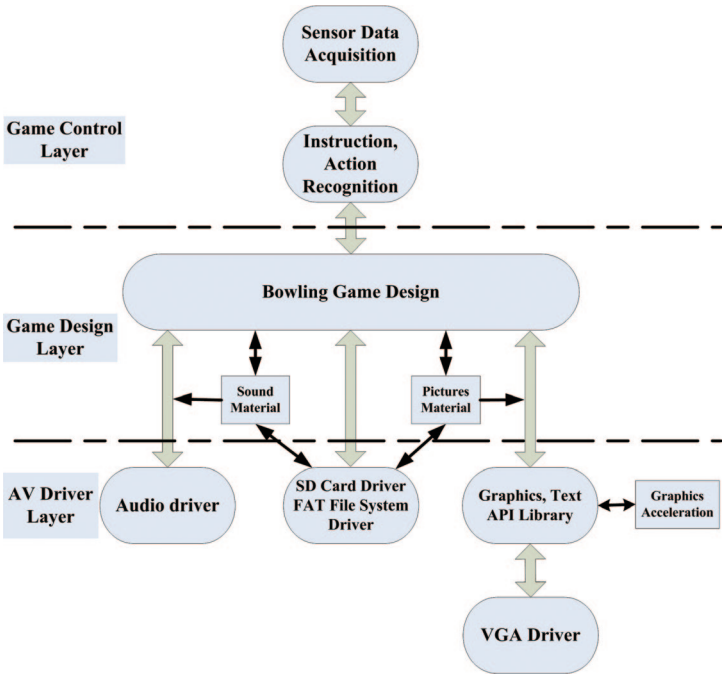

Figure 2. Software structure

This system uses a three-layer structure, the structure diagram is shown in Figure 2.

A. Game control layer

As the control end of the game, this layer acts as the mouse and keyboard. Android phone equipped with a three-axis acceleration sensor and magnetic field sensor collects this information and sends it via Bluetooth to DE2-70. Then our gesture recognition algorithm will give an accurate analysis of gesture on behalf of the instruction, thereby triggering the appropriate response of the game.

B. AV Driver layer

This layer is the basis of the entire game. It not only provides sound driver, VGA driver, SD card driver and FAT file system driver which designed for the SD card read &write operation, but also provides a rich graphics rendering APIs. In order to improve the operating efficiency, we implement the key tasks or key methods in hardware, for example, parts of the methods of the graphics APIs, etc.

C. Game design layer

The part is the core of the entire system to complete the design of the entire bowling game. Its implementation is based on the driver layer, in response to an instruction from the control layer. There has a clear demarcation between it and the control layer, because the driver layer and the control layer provides the interfaces independent of the game. That is to say, we can design a brand new game, without having to change anything of the control layer and the driver layer.

III. SYSTEM DESIGN

The system design is divided into two parts: the hardware and the software. The hardware part of the work is to build a multi-tasking operating environment and provides a control interface for external devices. We design the hardware environment shown in Figure 3.

In the picture, we use SDRAM1 and SDRAM0 to support double buffering mechanism for the video display. The UART module is designed

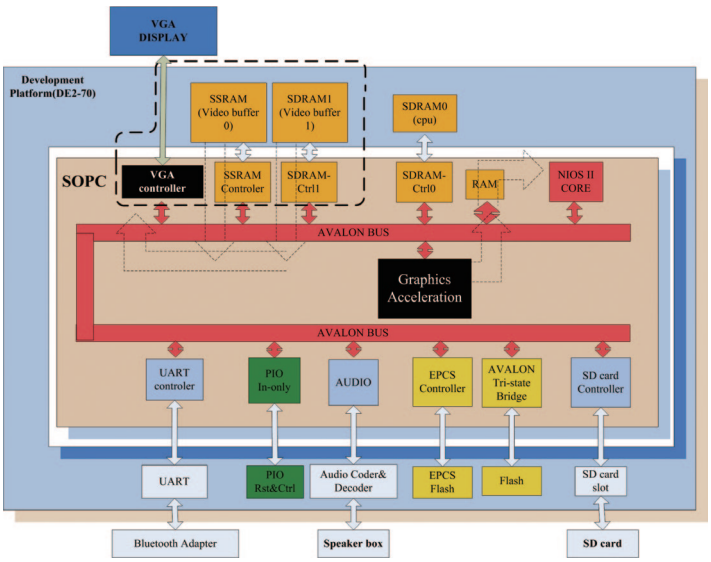

Figure 3. NIOS II system

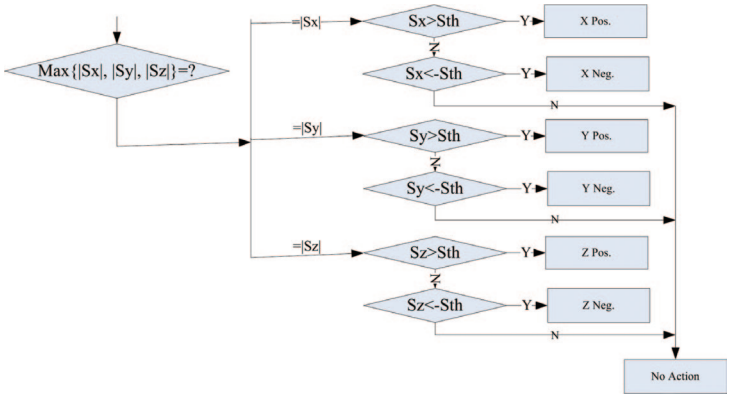

Figure 4. Gestures judge

for receiving the data sent by the phone, and the AUDIO module is for playing the sound effect.

In order to improve the image display and rendering quality, we design a VGA Controller and a Graphics Acceleration IP core, to provide support for the game of high-quality animation.

As described above, the system software uses the three-layer structure design and all details of the respective layers of the system will be elaborated below.

A. The game control layer

The raw data acquired directly by the sensor is, from the physical sense, acceleration, rather than speed, and therefore can not be directly used for determing operation gestures. We denote the speed in the x-direction S_x, and denote two adjacent sampled acceleration A_x0, A_x1, and the time difference between this two samples is ΔT_X, then

$$Sx = \frac{Ax1 - Ax0}{\Delta Tx} \qquad (1)$$

Similarly, we can calculate the speed in the other two directions: S_y and S_z . Then we can identify the gesture command according to the method in Figure 4 and the S_{th} is speed threshold. So, this method can identify six kinds of operation: the X-axis positive direction shaking, the X-axis negative direction shaking, the Y-axis positive direction shaking, the Y-axis negative direction shaking, the Z-axis positive direction shaking and the Z-axis negative direction shaking.

Not only that, in the bowling games we have to know the direction of motion and the ball speed when tossing. According to the previous calculations, the motion direction and ball speed comes directly from the speed vector (S_x, S_y, S_z).

B. The AV driver layer

As the bottom of the system, on the one hand, the upper support of sound and image, this layer provides all kinds of drivers and plays a very important role. Another important function is to provide the picture drawing, text display API library. The effect on implementation efficiency the of the graphics library of games is so important, that we must implement a part of the API in hardware, instead of in software, which greatly improves the game frame rate (FPS).

This layer can be divided into 4 parts: audio driver, VGA driver, SD card driver and FAT file system driver, as well as general purpose graphics text API libraries. SD card driver and FAT file

system driver provide support for reading and writing files on the SD card. There are lots of pictures and sound clips locating on the SD card, and we must loading them into memory before using them. The audio driver can be used to play background music and foreground music. The following paragraphs give the details on the VGA hardware design and some graphics API approach by hardware.

(1) VGA driver design

As previously mentioned, if you want to support a resolution of 640 x 480, refresh rate of 60Hz image display, 70M bytes of data will be transferred in one second. If this transmission is implemented by software, it will be a maximum of 4.5M bytes that we can transfer in one second. This shows that we must consider using hardware approach to accomplish this task, and can not affect the execution efficiency of the software, that is to say, we cannot occupy the CPU time too much.

Avalon specifications provide a variety of interface protocols for custom peripherals. There are a large number of data transmission protocols, such as Avalon-MM Master / Slave and Avalon-ST interface. As memory devices provide read and write interfaces via Avalon-MM Slave interface in SOPC, we have to use the Avalon-MM Master to reading and writing memory devices positivly. VGA IP core hardware module prototypes we design is shown in Figure 5.

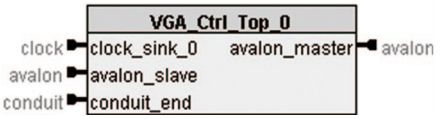

Figure 5. VGA IP core prototypes

1) **Avalon-MM Master:** The working clock of VGA interface is 25M Hz, but that of the Master is 100M Hz. It must take less than 4clocks to complete a read operation (4 bytes), which should be ensured. We also know that the Avalon system uses the slave-side arbitration mechanism, when multiple Master post a read or write requests to the same Slave at the same time. CPU's performing frequently memory read and write will have greatly effects on the work of the VGA IP core. So this IP core should use a line buffer inside.

2) **Avalon-MM Slave:** This interface is used for CPU to control the IP core. You can start and stop the work of the IP core, and set the VGA buffer memory address, which makes it possible to work with double-buffer mechanism by changing the buffer address anytime.

3) **Conduit:** This interface directly faces at the D15 VGA interface signals. Therefore, the important responsibility of this interface is to generate VGA timing with the RGB data provided by the Avalon-MM Master interface. The VGA interface horizontal timing is shown in Figure 6.

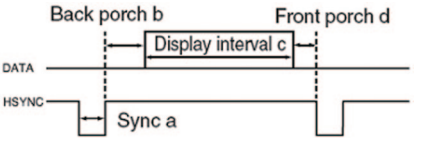

Figure 6. VGA horizontal timing

VGA vertical timing is similar to horizontal timing. Table I gives the length of each part in the horizontal timing and vertical timing.

TABLE I
VGA HORIZONTAL TIMING AND VERTICAL TIMING

Parts	Sync	Back porch	Display interval	Front porch
Horizontal timing (clocks)	96	48	640	16
Vertical timing (lines)	2	31	480	11

(2) Graphics acceleration module design

The IP core module is used to accelerate graphics drawing. Currently supported hardware

operation are displaying images (in transparent or non-transparent way), drawing rectangular boxes(in filled or non-filled way). These operations are the high frequency of use in the scene design. Implementing in hardware way can greatly improve the game frame rate. Figure 7 is the IP core module interface prototype.

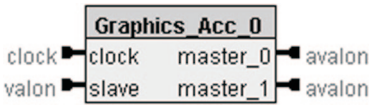

Figure 7. Graphics Acceleration IP core prototype

The IP core uses an Avalon-MM slave interface and two Avalon-MM Master interfaces. Slave interface is used to select the operating mode, and set all the input parameters. There are 10 registers using for storing the input parameters: ParamReg1 ~ ParamReg10. Table 2 shows the registers of the IP core function settings.

TABLE II
GRAPHICS ACCELERATION IP CORE REGISTER TABLE

Address Offset	Name	Access	Display images	Drawing Boxes
0x00	Control	RW	Control and operation mode registers	
0x04	Status	R	Completion status	
0x08	ParamReg1	RW	Image width	Rectangle width
0x0C	ParamReg2	RW	Image Height	Rectangle Height
0x10	ParamReg3	RW	Data address	Start x
0x14	ParamReg4	RW	Start x	Start y
0x18	ParamReg5	RW	Start y	Unused
0x1C~ 0x2C	ParamReg6~10	RW	Unused	

The IP core module also uses the two master interfaces, one for reading image data from the source address, and another for writing data to memory. This is similar to the DMA functionality, but DMA can only write to consecutive addresses, and therefore is not suitable here. After acceleration, Improved performance is shown in Table III(all operations are on the compiler optimizations: GCC-O3).

TABLE III
GRAPHICS ACCELERATION

Operations	Software way	Hareware Way	Ratio
Display Images (non-transparent, full screen)	97.4ms	3.2ms	30.4
Drawing Boxes (filled, full screen)	53.2ms	3.1ms	17.2

Obviously, Implemention in hardware way will greatly enhance the speed of drawing, and ensure the fluency of the game.

C. The game design layer

This layer is the detailed design on the game. It uses the interfaces provided by control layer, and gets gestures instruction, and then calls graphics and voice APIs provided by driver layer to play music and draw game.

There are four big tasks: sensor data acquisition and instruction recognition, image rendering, VGA output, audio output. There is a big problem: these four tasks should concurrent working. Among these tasks, image drawing is our main jobs. Our design combines the advantages of software and hardware to solve the problem.

1) **Data acquisition and instruction recognition:** Data acquisition is in mobile end, and UART works with interrupt mode to receive data and identify gestures.

2) **VGA output:** We introduce detailedly the VGA driver design previously, and it is a whole hardware way. It works fully parallelly with CPU.

3) **Audio output:** Audio output hardware module has a buffer zone, enough to store 5 ms voice data. We trigger a timer interrupt in every 5 ms to fill enough data, so as to ensure the continuous broadcast voice.

4) **Image drawing:** This as our main task, and it shares time with “command recognition” task and "audio output" task, but is completely parallel with "VGA output" task.

In addition to the above four major tasks, bowling game 3D motion trail modeling is another problem.

We adopt the followling physical model : a bowling's initial position is (x0, y0, z0), and initial velocity (the speed when the ball is out of hand) is (vx, vy, vz), and initial acceleration (the acceleration when the ball is out of hand) is (0, 0, g), and the reverse friction force acceleration is (- fa, - fb, 0). Ground bounce coefficient is k, and we assume that z axis speed denotes 0 when z axis speed is less than vzmin, regardless of the air interference.

According to this physical model, we can easily figure out the motion trail, so the relevant calculation is omitted here. It is proved that this model can completely meet the requirements by using Matlab simulation tool.

CONCLUSIONS

We introduce the game design idea and implementation steps in detail, previously. Eventually we implemented the somatosensory game which demonstrated excellent performance: gesture recognition rate is 85% or more, and game frame rate is average of 40fps, and can play background music continuously at the bit rate of 44.1KHz without interfering with other tasks. These benefits are from the hardware and software combination design. Based on the scalability of the system architecture and FPGA devices' reprogramming, we can easily add new game design or just perform maintenance and upgrade. In short, based on the thinking of hardware and software co-design, the use of FPGA technology can facilitate the construction of multi-parallel processing module, multi-processor core hardware system. This design gives full play to the advantage of FPGA hardware technology, and show the FPGA great advantage and potential in the field of video images, somatosensory games.

PROSPECTS

Game designers must find a balance between the complexity of the system, reliability and low cost. However, to be successful in business, game console must be able to provide a variety of functions, such as high-resolution images, the network connection, motion sensing controllers, and IP-based video control, and all of these must be as low price as possible. In order to maintain low-cost characteristics, usually module reuse of methods is encouraged in designing a game console. FPGA hardware flexibility makes the game system to be easy for different regions, model, component redesign. FPGA replaces the role of ASIC in many applications, perhaps it is the time to use it for the next generation of game design.

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Development of EEG-based Intelligent Wheelchair Based on FPGA

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Abstract — In this paper, an intelligent wheelchair control system which can provide auxiliary help for disabled patients based on BCI is proposed. This system is based on 90% of normal brain function people whose wave amplitude of EEG can be significantly enhanced in the short eyes closed. We place two detection electrodes on the occipital and forehead of the brain, pre-amplify the detected signal, and then after a series of signal processing, we can simply and easy control the movement of the electric wheelchair and do not need training or only a small amount of training. Through the TI's ADS1198 analogy front-end circuit, we realize EEG acquisition, amplification, isolation and data pre-processing. Data is processed in the Nios II environments. Finally, the system controls the YIFUCON's wheelchair KB5618 in accordance with the appropriate action.

Keywords — EEG, Nios II, KB5618, ADS1198, wheelchair

I. SYSTEM DESIGN

The United Nations issued that the world aging population is accelerating. The next 50 years, the proportion of the population over the age of 60 is expected to double. Moreover, people with disabilities caused by a variety of disasters and disease have increased year by year. They suffered from different degree of disability, such as walking, vision, hands, and language. At this situation, in order to improve the life quality of the elderly and the disabled people and help them back into social activities, a motion assistance system is needed. Presently, some countries like the United States, Germany, Japan, France, Canada, Spain and China have began to study the intelligent wheelchair which could have a memory map, obstacle avoiding function and walking automatically via user commands.

The smart wheelchair also known as the intelligent wheelchair mobile robot is the electric wheelchair that applies the intelligent robot technology, which integrates a variety of fields including robot navigation and positioning, pattern recognition, multi-sensor fusion and human-machine interface (HCI) involving mechanical, control, sensors, artificial intelligence, communications technology, Its motion achieves in a almost no radius of gyration of the real meaning of the omni-directional motion. Especially, it can adjust position while keeping the body posture unchanged. It is a great step forward for people with weak walking ability, because it makes it posible for the disable people to access to the place they want without others' care. At the same time, If we design out more function (for example, the humanity of the HCI, navigation and obstacle avoidance function) in a wheelchair, this kind of wheelchair will be more promising.The developed

intelligent wheelchair can not simply copy the traditional design methods and theories of the robot. And it must truly set the "people" as the center, focusing on the issue of intelligent human-computer interaction. Unlike industrial robots and electric machines to achieve a specific production tasks, the intelligent wheelchair, all of its service behavior must interact with human to achieve the “man-machine-aware interface”, so that a wheelchair can ‘see’, ‘hear’ and able to integrate a variety of channels of information to perceive the external environment. Human can interact with intelligent wheelchair in a more convenient and natural way such as facial gestures, expressions, gestures and voice and etc. Besides, they can transmit their own knowledge and experience to the wheelchair. It is worth noting that if human-computer interaction issues are not properly resolved, it will become a bottleneck restricting to the development of intelligent wheelchair.

Since Britain started to develop an intelligent wheelchair in 1986, many countries began to allocate more funds to study the intelligent wheelchair, such as US MIT WHEELESLEY project, the project of the University of Ulm in Germany MAID, the European Union TIDE project. Intelligent wheelchair research started late in China, and the complexity and flexibility of the structure have a certain gap when compared with abroad, but there also exist some smart wheelchair close to the international advanced level of technical qualification according to its own characteristics. The domestic research units mainly are the Chinese Academy of Sciences Institute of Automation, National Chung Cheng University, Taiwan Department of Electrical Engineering, Shanghai Jiaotong University.The third Military Medical University. Their researches have made some achievements. However, there are still some problems. It is suggested that the trends of intelligent wheelchair research in the future concentrates on user-friendly, modularity.

In our study, the Nios II embedded processor was used. Compared with other processors like MCU, DSP, ARM, Nios II soft-core processor has the following characteristics. Firstly, SOPC proposed by Altera is a flexible, efficient SOC solution. It integrates Nios II processor, memory, the I/O port and other functional modules into an FPGA which is a programmable on-chip system. It has a flexible design approach and provides a number of available IP cores that can be cut, expanded, upgraded. Secondly, Nios II is a kind of soft-core embedded developments. It is flexible, high-performance, low-cost, long life cycle and provides a lot of technical documents and examples of development. If you are expert, you can design anything you can imagine with FPGA. This is the greatest significance of the Nios II. Nios II supports MicroC / OS-II, uClinux and other real-time operating systems, and also supports lightweight TCP / IP protocol stack, as well as ‘*.Zip’ files system. Nios II allows users to add custom instructions and hardware acceleration unit, and transplant custom peripherals and interface logic seamlessly. It improves the performance as well as facilitates the design for user. Finally, the development of embedded systems on FPGA in Altera is in forefront of the world all the way.

In summary, our design is user-oriented terminal design and provides the aging population, the young people and children (such as accidents, disability, congenital diseases) who rely on technology to sustain life, the advanced cancer or AIDS patients and special healthy crowd (new baby, pregnant women) a convenient and suitable operation family-intelligent wheelchair controlled by EEG.

II. FUNCTION DESCRIPTION

In this paper, an Intelligent wheelchair control system which can provide auxiliary help for

disabled patients based on BCI is proposed.This system is based on 90% of normal brain function people whose α wave amplitude of EEG can be significantly enhanced in the the short eyes closed. We place two detection electrodes on the occipital and forehead of the brain, pre-amplify the detected signal, and then after a series of signal processing, we can simply and easy control the movement of the electric wheelchair however do not need training or only a small amount of training. The system can be extended to more complex multi-option of real-time control system. Through the corresponding experiment,we can prove this based on α brain - machine interface system can be realized, and the system has the potential application value. Through further integration and portability, and the configuration of an appropriate information feedback LCD, we can develope out a specifical new assistive products for those with systemic severe paralyzed but mind functioning is regular.

The system hardware consists of the DE2 development platform, TRDB-the LTM LCD screen, EEG amplifier, wheelchair model. The system can be divided into three functional modules: EEG acquisition, amplification and preprocessing module; EEG signal processing and control module; LCD display, and human-computer interaction and wheelchair control module.

1) **EEG acquisition, amplification and pre-processing module:** We use Texas Instruments (TI) company's fully integrated analog front end (AFE) chip ADS1198 as the core analog front-end circuit for EEG acquisition, amplification, isolation and other pretreatment operations.

2) **EEG signal processing and control module:** This is the part of the algorithm of the system, also the core functionality of the system. We take advantage of the Nios II processor and powerful computing power of a PC, and the most of the algorithm is C code.

3) **LCD display and human-computer interaction module:** We use a digital touch panel LCD TRDB-LTM provided by Altera Corporation and some buttons as display and human-computer interaction respectivly. We use the IP core to add to Avalon to driver the LCD. Button, we choice interrupt mode to trigger reset, start, and closing functions of the control system.

4) **Wheelchair control module:** We use Yifucon KB5618 wheelchair,and then give the control signal to the wheelchair control system we can control wheelchair go straight, turn left, turn right.

III. PERFORMANCE PARAMETERS

This system utilizes the trait of amplitude value of α wave on the cerebral cortex will increase when eyes close. We provide a simple and reliable electronic device switch control method, and we have done some exploratory expansion. We use the assessment principles in its design of the user interface: Effective Human-Computer Interaction Principles by Ben Shneiderman, founder of the Human-Computer Interaction Laboratory of the University of Maryland to measure the BCI system performance assessment:

A. The time of learning to use the system

This system explores and uses the trait of amplitude value of α wave on the cerebral cortex will increase when eyes close, and then finish the control system.And more than 90% of the population has this trait, so almost no learning or only a very short time of learning for us to use this system.

B. The execution speed of the system

It’s real-time online operation, relatively fast. Despite the individual differences, the time required to trigger switch is still relatively short, execution speed is faster.

C. The errors will occur, and the kind of error

This system depend on the data collected from brain electric signal to decide the direcrion for the wheelchair to turn such as left, right and go straight ahead. Due to the complex brain electrical signals and the different levels of testers' training, turn left will be sentenced to turn right and on the contrary, turn right or go straight also mistaken for the other two actions. Accordingly, there are six types of error, the average error rate of approximately 20%, with a further improvement of the design and the increase of the frequency and duration of trainer's training, receiver error rate will be greatly reduced.

D. How long can users keep this knowledge

A long time, because almost do not need training and repeatability is very strong.

E. The user's comfort and satisfaction

Electrode small, easy to install, and in places outside the line of sight, and from the appearance it's equivalent to wear an ordinary hat,. It can reduce the visual signals of the disabled, so it can avoid patients' self-confidence and self-esteem to be hurt.

IV. DESIGN STRUCTURE

A. Hardware system design diagram

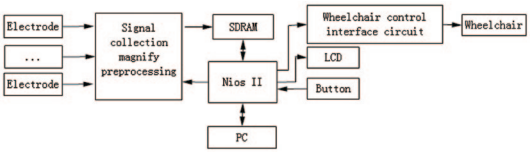

Figure 1. Hardware system design diagram

B. Software system flow chart

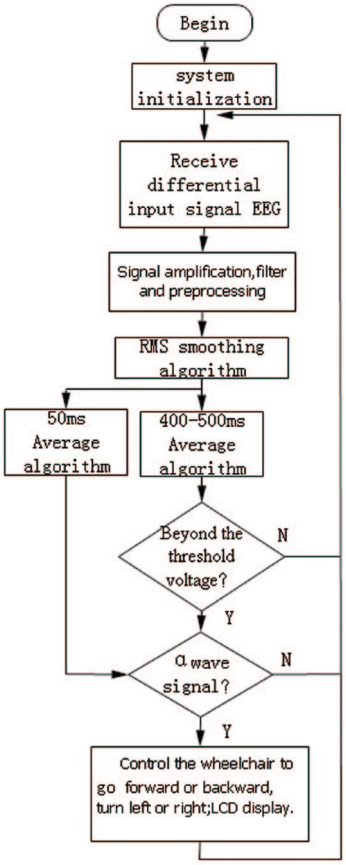

Figure 2.Software system flow chart

V. DESIGN METHOD

A. The design of the hardware platform

1) EEG signal acquisition, amplification and pre-processing module

The system uses the core of TI's ADS1198 as analog front-end circuit. ADS1198 has the following main features :

- 8-channel 16-bit ADC converter chip, the sampling frequency is 125sps ~ 8ksps.

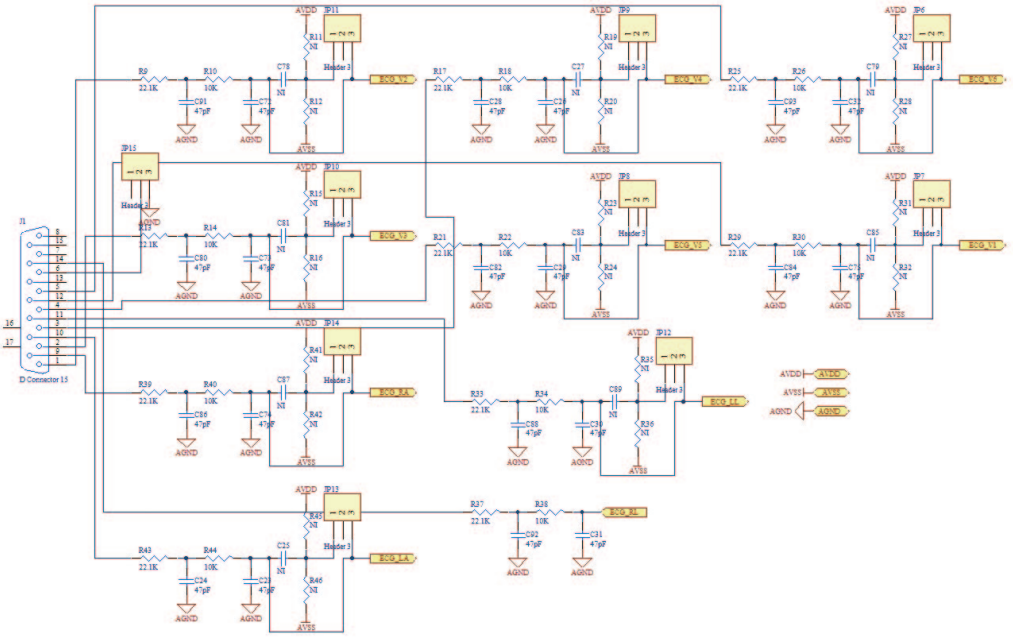

Figure 3.ADS1198 analog front-end input circuitry

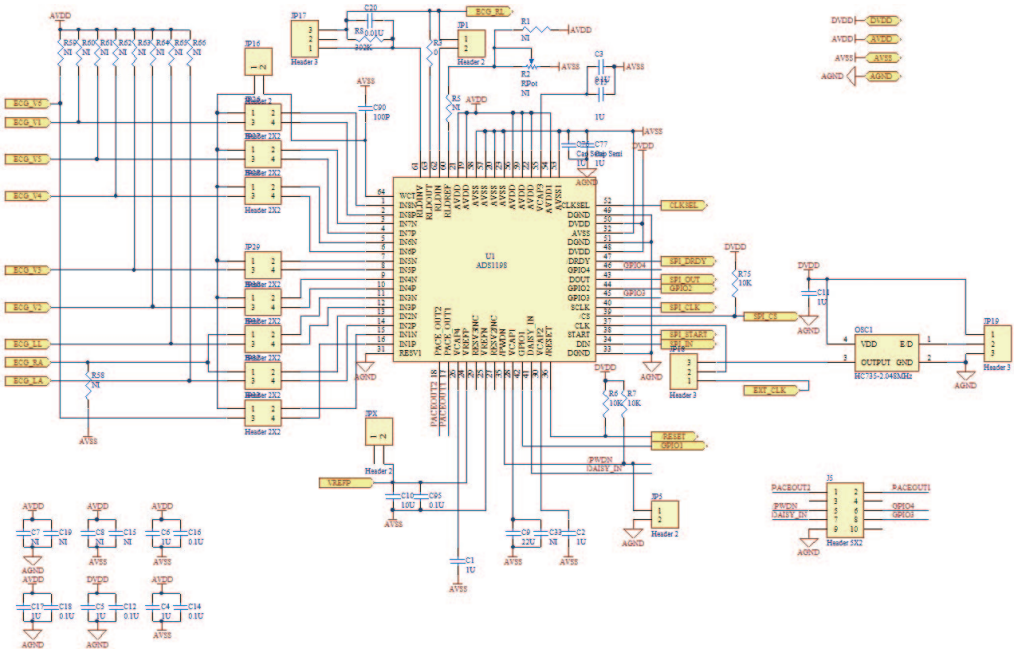

Figure 4.The core of the ADS1198 analog front-end circuit

- Each channel has programmable amplifier, whose magnification is adjustable from 1 to 12 times;when CMRR>100dB, input impedance is approximately 10 MΩ.
- It contains the right leg driver amplifier and Wilson central terminal.

According to ECG or EEG patterns of specific applications, the MCU makes configuration multiplexer (MUX) the internal input end (INPUTS, RLD) on or off,so that programmable amplifier (A1-A8) magnification and AD converter(ADC1-ADC8) sampling frequency. When the chip completes a conversion, Data Ready pin goes low to notice MCU through the SPI bus to read data.

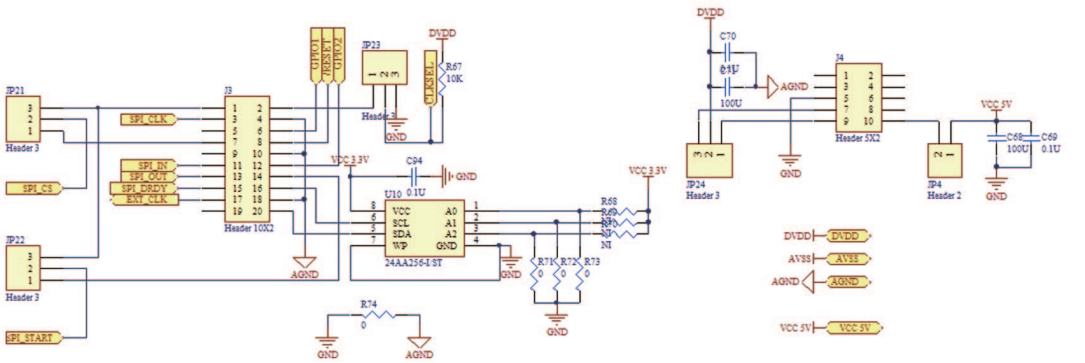

Figure 5.The interface of ADS1198 analog front end and DE2 circuit

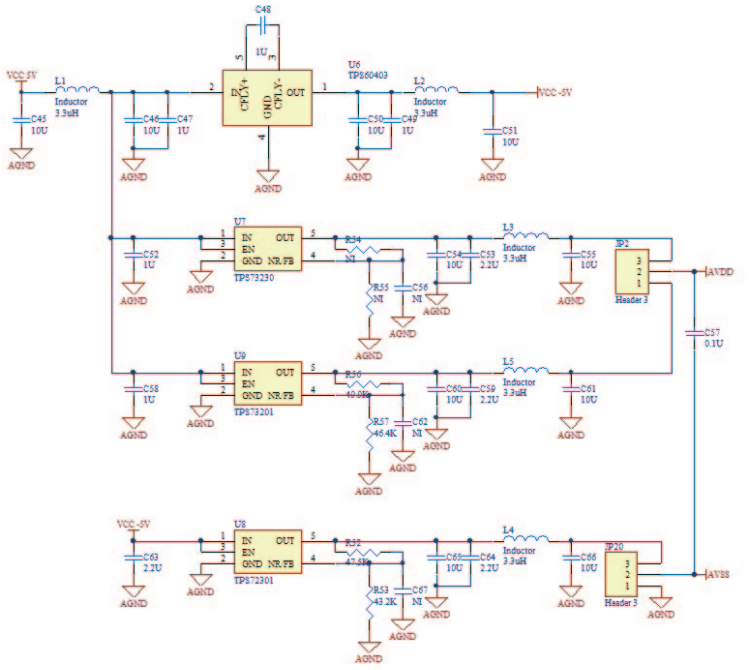

Figure 6.ADS1198 analog front-end power supply circuit

[1]. ADS1198 analog front-end input circuitry
It contains the second-order passive low-pass filter and limiter circuit and play a role in the elimination of high-frequency interference and overvoltage protection.The low pass cutoff frequency is 30 kHz and the amplitude of the voltage range is ± 700 mV.

[2]. The core of the ADS1198 analog front-end circuit
It makes configuration of the ADS1198 peripheral pin, and leads to the control port and SPI command input and data output port.

[3]. The interface of ADS1198 analog front end and DE2 circuit
This completes cohesion analog front-end circuit and DE2 board, so that the brain electrical signals transmit through the circuit to the DE2 board for data processing.

[4]. ADS1198 analog front-end power supply circuit
This contains the TI's TPS60403DBVR, TPS73230DBVR, TPS72301DBVT and TPS73201DBV. These polarity converter and voltage regulator chips converter +5V (DE2 panel) to -5V, +3.0 V,-2.5V and +2.5 V to meet the ADS1198 power supply requirements.

2) The wheelchair and its control module

We choose the YIFUCON's wheelchair KB5618. The wheelchair has two driving wheels (right and left) before passive wheel plus. The rotation of the rear wheel is controlled by two DC motors. The motor controller uses the PG controller. Through communication with PG controller we can control the speed and direction of the wheelchair.

Control system: The British PG controller accelerates smoothly, jitter-free, downhill automatic transmission, energy saving. Through communication with PG controller we can control the speed and direction of the wheelchair.

PG controller: The start of the controller is a high level of 5ms. Both the opcode and data bit is 8bit binary.

Opcode and the format of the data bits: 1 start bit, 8 data bits,1 parity bit and two stop bits. The start bit is low electrical level enabled.The stop bit is two high electrical levels enabled.

Control signal packet format: 5ms HIGH + stall control data +8 bit receiver when the data (transmission 0) + the data about going forward or backward +the data about turning right or left+ checksum data;

The front and rear,and left and right in controller constitute a Cartesian coordinate system.Through the different x and y values, we can achieve any angle of rotation, and we can adapt to different terrain and population adjustment stalls. The wheelchair has a good brake system. The brake signal is generated by the controller to control the motor brake.

We use the FPGA to complete the package of data interface, so that the follow-up call is very convenient. In order to obtain the speed and direction information,we will analyze the EEG data obtained after processing in the FPGA, a certain format of a packet transmitted to the PG controller, completed by the PG controller for the motor control. Taking into account the human EEG sampling time differences, in order to prevent continuously appearing multiple times in one direction deflection, we set brake motors to stop wheelchair walking. So we can guarantee security.

Through the communication with the PG controller, we can easily read the battery information. And we can also read the failure information, including motor failure, brake failure. So we can facilitate the overhaul of our wheelchair easily.

Figure 7.YIFUCON's wheelchair KB5618

3) LCD image display and interactive modules

Most BCI systems need feedback.The most common form of feedback is cursor control. subjects move the cursor to the specified target location, only use the up / down or left / right two sets of commands. Cursor is in the middle of the screen at first, and then each section of the cursor meets the target location or the opposite position. When it comes to the target location, the cursor will blink, indicating success.This feedback can enhance the confidence of the subjects with the idea of operating the cursor. Cursor control provides persistent feedback, so the subjects are able to see their own ideas driving the cursor on the mobile, such as the wrong direction can promptly adjust.For BCI systems, particularly those based on the operating conditions BCI systems, feedback is necessary, subjects need to know which ideas can move the cursor which direction movement.

The LCD image display is actually a feedback platform.The image displayed on the "↑ ↓ ← →", respectively correspond the subjects' controling the wheelchair front, rear, left, and right directions. Combining with the feedback of the success "Success!" we can remind the operator to successfully carry out the operation. The purpose of doing so is to enhance the stability and accuracy of the system in order to focus the attention of the subject and excite continuing experiments power.

The system's LCD display module is TRDB_ LTM, which is provided by Altera Corporation.

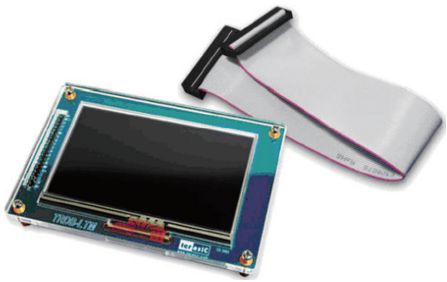

Figure 8.TRDB_LTM uniform look

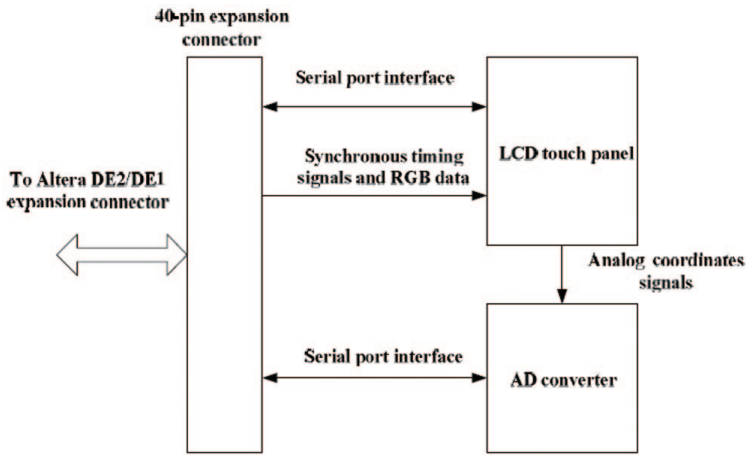

Figure 9.TRDB_LTM overall diagram

TRDB_LTM mainly includes LCD touch panel module AD converter and a 40-pin expansion signal interface module. 40-pin expansion signal interface is used to connect DE2/DE2_70/DE1 development platform reserved for 40-pin expansion port; LCD touch panel module from the FPGA AD converter input control signal and image is displayed on the LCD panel; the coordinates of the touch point value is exported reserved interface of the FPGA to achieve the effect of touch control.

In addition, the system uses the keys on the DE2 to select interrupt mode, trigger control system reset, start up, and shut up and so on.

4) SOPC Builder Construction and QuartusII Hardware Structures

This is SOPC structure of our system.The system clock uses 100M, which is produced by external clock (50M) PLL multiplier. Add cpu, tri_state_bridge, cfi_flash, sdram, epcs_controller, jtag_uart, uart, timer, lcd_16207, led, button_pio, DM9000A, VGA, ISP1362, ADS1198_DRDY, ADS1198_SPI, ADS1198_RESET, ADS1198_START, ADS1198_DATA module components, etc.

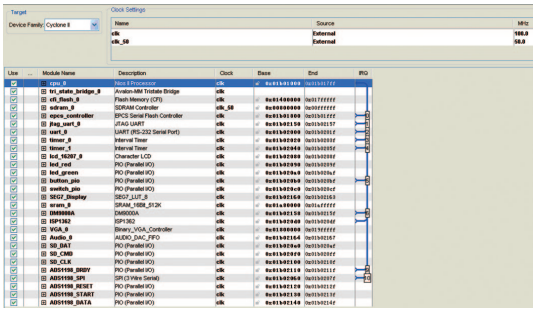

Figure 10.SOPC Builder interface

Then, assign pin and compile in the Quartus II to generate hardware .SOF file.So the hardware platform portion of the works will be designed.

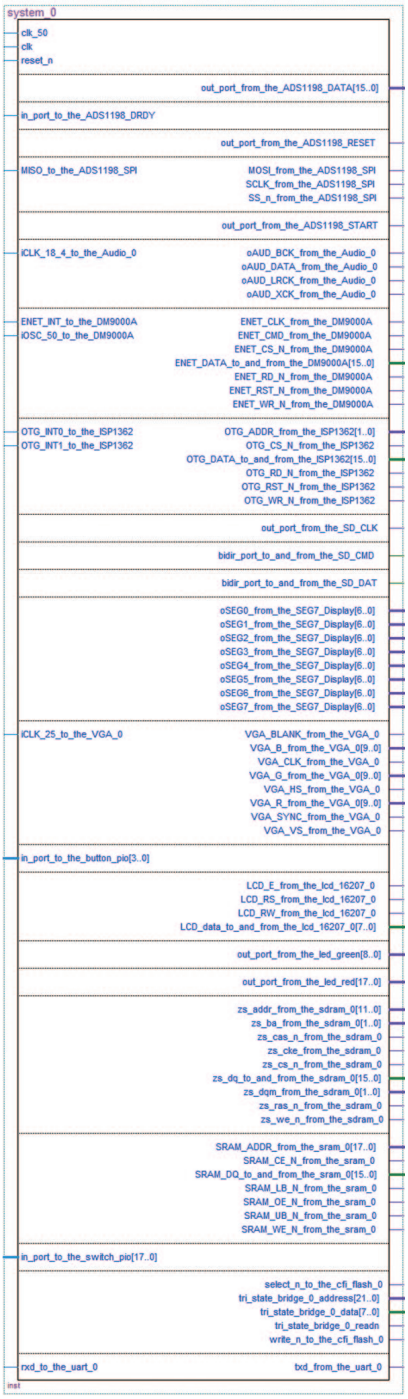

Figure 11.In SOPC Quartus II generated module

B. The design of the software platform

The collected EEG went through a preamplifier, 50Hz notch, 30Hz range signal preprocessing, and the subsequent processing is done in software Nios II platform. The entire software design process: receive differential input signal after pretreatment, and then reserve α wave through the main frequency band of the bandpass filter of 8 ~ 13Hz. After 10ms of the RMS smoothing algorithm,the signal is divided into two:one goes through 400 ~ 500ms (varies) average algorithm, which is the main control path; another goes through a 50ms average algorithm,which is the auxiliary control pathway used to determine alpha wave control signal on the main path is α wave or a noise signal. The signal went through the first path and compared with the threshold voltage.If the signal is beyond the threshold voltage,compare with the signal which went through the second signal path to determine if it is α-wave control signal.If the signal is α-wave, control the wheelchair to go forward or backward, and turn left or right, and control the LCD to display feedback imformation. If the signal is not α-wave,re-read the differential input signal.

C. The determination of the system parameters

Experimental verification should be taken in the entire system: which mainly includes the collecting cap electrode position experiment, setting subjects ssthresh voltage trigger time experiment.The collecting electrode position experiment provides a basis for design of the electrode cap: values and illustrate voltage.The trigger time experiment is to determine the system parameters.

1) **Collecting electrode:** The α wave correspond with idle rhythm of the Visual area. Its frequency is 8 ~ 13Hz and the amplitude is approximately 20 ~ 100uV. It is most obvious wave of rhythmic brain waves.The d wave blocking phenomenon is the theoretical basis of the design. α wave is seen in all Scalp lead, especially the pillow District. Generally, for unipolar lead, showing the highest volatility is the pillow, followed by are the top and prefrontal. The early design select two traditional AgCl electrode to place in the occipital 01, T5 location.The collected EEG and earlobe reference electrode import preamplifier in differential mode. However, the electrode and the hair being in direct contact may cause the electrode junction skin impedance mismatch.What's more, the electrode is placed directly on the hair.For each acquisition, in order to improve the SNR of the signal, the electrode often soaks in physiological saline or contact area coats with a conductive paste,which is very inconvenient. So we designed a EEG acquisition cap.On the condition collected alpha wave has little effect on the system control, explore acquisition proud of some of the flexibility of changing the position of the electrode, making the signal acquisition easier, experimental easier cleaning. The specific approach is: earlobe reference electrode is constant,the collection the electrode by the Ol position of the occipital is moved to no hair forehead FPl, and the electrode positions are fixed in their hats, which simplifies the experimental procedure.Subjects' α volatility value in the 01 position compared to their α volatility value in the FPL position.Use EEGCollection software to collect and measure the α wave data in the steady state of the two positions,and then process it in MATLAB.

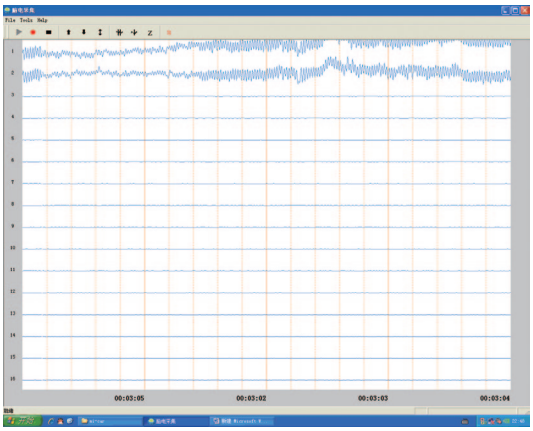

Figure 12. EEGCollection software collects EEG signals

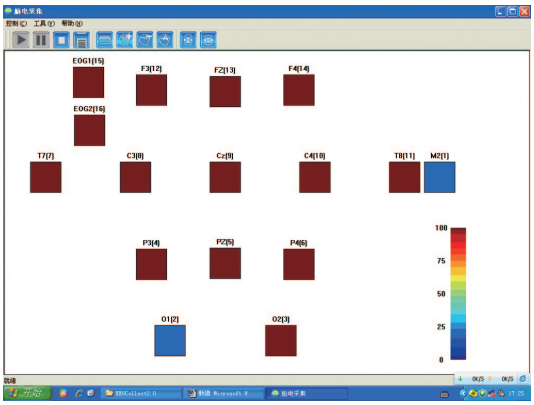

Figure 13. EEGCollection software detects electrode impedance

2) **Threshold voltage:** Each human subject distinguish from each other.The average of the RMS-DC averager voltage Vi imports one of the input terminal of a comparator, while the other input terminal is a predetermined DC threshold value of the threshold voltage Vth, which is man-made based on different subjects' EEG average Vqeo voltage value when they are calm and their eyes are open. Its value set relates to the stability of the system.If it was set too low, there will be a pseudo-positive potential—subjects are not quiet or close their eyes to generate a control signal,so that the input exceeded the threshold potential due to other interference and caused positive voltage, and the whole system is triggered.If it was set too high, it will cause the pseudo negative potential—subjects with eyes closed generate a control signal lower than Vth input potential,in other words, subjects has generated a control signal but has not triggered the normal system . By contrast, the harm of the pseudo negative potential is much smaller than the harm of the pseudo-positive potential, so the threshold is set to avoid the emergence of the pseudo-positive potential. Vth is set as low as possible in the case of the least pseudo positively charged digit.

3) **Cycle time:** subjects operate instructions from the cycle lights on the control panel.The cycle time of looping the lights must match with the time subjects control signal generate, that is, when the light is on, subjects should close their eyes so that the generated control signal time coincides with the lights.While subjects opening eyes to control, cycle lights go out and subjects carry forward to the next control. Adjustable cycle lights cycle regulation is based on the the trigger time that experimenters control the signal.

VI. DESIGN CHARACTERISTICS

The design has the following features:

1) **Design concept:** This product used to help physical disability or aging can't walk crowd, as well as severe paralysis and even brain thinking population, bring these people the convenience of the action. Wearing the electrode cap, users just like put on an ordinary hat and do not have to worry about being ridiculed. Users do not need training or only a small amount of training and can control the movement of the electric wheelchair simply and easy, and the system can be extended to a more complex multi-option of real-time control system.

2) **Product function:** Through the experiment, we can conclude that this based on α brain - machine interface system can be realized, and the system has the potential application value. Human-computer interaction techniques for special groups or special purpose of development in intelligent wheelchair are different from general manual operation of the artificial intelligence technology. It became one of the key technologies (obstacle avoidance, self-positioning, human -computer interaction) of smart wheelchair, and also in a pivotal position in the development of intelligent wheelchair. Through further integration and portability, and the configuration of a appropriate information feedback LCD, we can develope out a specifical new assistive products for those with systemic severe paralyzed but mind functioning is regular.

3) **Hardware design**: SOPC make our design more simple and straightforward, each module can be done individually, but can easily integrate to form a system. we can embed in a system of multiple master devices (including AD, LCD) to achieve data transmission, greatly reducing the burden on the CPU; At the same time we can quickly upgrade hardware module, and an IP can be hooked up to the bus, this can't imagine when in chip-level structures of the SOC system in the past. All IP use Avalon bus architecture and adopt a unified synchronous clock.

4) **Software algorithms:** Our design is relatively complex, not only the design of the module, but also some complex algorithms embedded and the design difficulty is also the characteristics we must explain.

5) **Extremely flexible Nios II processor-based EEG control intelligent wheelchair:** we can configure and upgrade system quickly without having to replace the entire system platform according to the needs of different hospitals, community and family.

CONCLUSIONS

1) Through the study, we have deepened our understanding of SOPC, and acquireed a certain amount of experience in using Nios II CPU for embedded system development. The Altera SOPC gave us the strong design platform, so we can involve in hardware development, drive development and the application procedure development, and make system-level development faster and easier.

2) The project, we get start several months ago, gain is not only the final works, the more important is the experience. From the IP core design, the former after simulation, to optimize the application, we truly appreciate the design ideas, can be said we find the "feel" of the design. The development of embedded system tests our patience sincerely, and debug program is to spend most of the time, but it can benefit a lot.

3) Use embedded logic analyzer, SOPC Builder, nios ii IDE and DSP Builder to design product that can really speed up the development speed. Although individual division of labor is different, but we can learn all knowledge, we really appreciate the strength of the team.

4) Feel the deepest is NIOS and other embedded system difference in its flexibility. In the design process, we can see how a system formed from the lowest level of the realization of the design to the application layer transparently, and can strengthen our system consciousness deeply.This can not be compared to other embedded systems.

5) So far, our work still has a large space for development. For examples how to speed up the interface switching speed, how to enhance the performance of the DSP in the system, and to achieve a more accurate the biomedical signal waveform detection algorithm, we need to continue to work hard.

6) Finally, let us take this opportunity to thanks our teachers and friends for their help, thanks the competition organizers and judges for their hard work.Our lab will march on till victory is won.

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Electric Unicycle from Image Signals

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Abstract — This paper realizes a SoPC system which balances an electric unicycle based on image data from a CMOS camera. Generally, tilt-meters and gyros have commonly been chosen to measure the tilt angle and angle rate of a unicycle. In this paper, a CMOS camera is employed as the tilt angle measurement sensor instead. Through simple image processing techniques, a hardware circuit module for inclination measurement for the unicycle is implemented on the FPGA of a SoPC. By the concept of software hardware co-design, the inclination measurement module is integrated with the double-PD control method on the SoPC to balance the unicycle. Simulation and experimental results confirm that the resulting system meets the design goal.

Keywords — SoPC, FPGA, electric unicycle, double-PD control

I. INTRODUCTION

In order to get rid of petroleum dependency and cost down, the industry and academy have spent lots of efforts on researching and developing electric wheeled vehicles. Among which, electric self-balancing vehicles have also drawn much attention and some products even can be found off the shelf, for instance, RYNO Motor, Segway, and UNO III [1-3]. The main advantage of an electric self-balancing vehicle is that it can keep balancing while moving. Besides, the turning radius and the size of the vehicle are quite small. For achieving these advantages, an accurate and reliable controller is required.

An electric unicycle is a non-linear and unstable system such that, from the viewpoint of control, it has been a challenging system to be well controlled. Ruan et al derived the dynamic model of a unicycle robot, which composed of a wheel, a frame and a disk, by using Euler-Lagrange method [4]. Under state space control method, the unicycle can reach longitudinal stability by appropriate control to the wheel and lateral stability by adjusting appropriate torque imposed by the disk. Jin and Zhang designed a path planning algorithm to control a unicycle according to the POS (Particle Swarm Optimization) method [5]. Lee designed and implemented a PID controller to control an electric unicycle [6]. Chen derived a unicycle mathematical model and designed feedback linearization and sliding mode control methods to verify a real-time hardware-in-the-loop (HIL) platform [7]. Huang designed and realized an unmanned electric unicycle system controlled by pole-placement and LQR (Linear-Quadric Regulator) methods [8]. Tsai et al developed an electric unicycle, which can be ridden by one person, under the control of an adaptive nonlinear control method [9].

The electric unicycle has often used tilt-meters and gyros to measure its angle of inclination and angle rate. In this paper, however, a CMOS camera is employed as the measurement sensor. The function of the camera captures images and there is a reference horizontal line in each image. According to the line in the image the unicycle's

body tilt angle can be computed. Adopting the image processing procedure like the method used in [10], the image processing unit will be designed as a hardware circuit module and implemented inside the FPGA (Field Programmable Gate Array) of a SoPC (System on a Programmable Chip). By the concept of software and hardware co-design, the inclination measurement module will be integrated with a double-PD controller to be realized on the SoPC to balance the unicycle.

The organization of this article is as follows. Mathematical model of the unicycle is derived in Section II. Section III describes the PD control method briefly. Simulation results are demonstrated in Section IV. System architecture of the unicycle is elucidated in Section V, whereas Section VI explains the design of the image processing unit. Section VII shows experiment results. Finally, conclusions and future perspective are drawn.

II. MATHEMETICAL MODEL DERIVATION OF A UNICYCYLE

Figure 1 depicts the basic architecture with parameters of a unicycle. The relative parameters are defined in Table 1.

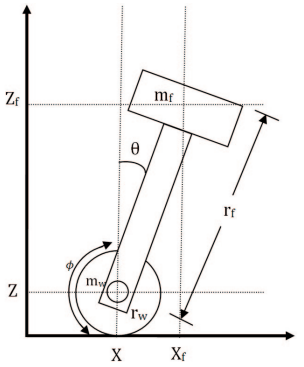

Figure 1. Unicycle architecture

TABLE I.
DEFINITION OF RELATIVE PARAMETERS OF THE UNICYCLE

Symbol	Definition	Unit
θ	Inclination angle of the body	rad
ϕ	Wheel rotation angle	rad
m_f	Mass of the body	kg
m_w	Mass of the wheel	kg
r_f	Length between the wheel axle and center of mass of the body	m
r_w	Radius of the wheel	m
x_f	Distance between center of mass of the body and z axis	m
z_f	Distance between center of mass of the body and x axis	m
x	Distance between the wheel axle and z axis	m
z	Distance between the wheel axle and x axis	m
μ_ϕ	Coefficient of viscous friction between the wheel and ground	Nm • sec/rad
g	Gravitational acceleration	m/sec^2
Im	Moment of inertia of the motor axle	Kgm^2
dl	Reduction ratio of gear	

Euler-Lagrange equations of the unicycle can be written as (1).

$$\begin{cases} \dfrac{d}{dt}\left(\dfrac{\partial L}{\partial \dot{\phi}}\right)-\dfrac{\partial L}{\partial \phi}=-\mu_\phi\dot{\phi}+\tau \\ \dfrac{d}{dt}\left(\dfrac{\partial L}{\partial \dot{\theta}}\right)-\dfrac{\partial L}{\partial \theta}=0 \end{cases} \quad (1)$$

Where Lagrangian function L is defined in (2).

$$L = T - U \quad (2)$$

T and U are kinetic and potential energy, respectively, and are shown in (3) and (4).

$$T=\left(\frac{1}{2}m_w r_w^2+\frac{1}{2}m_f r_w^2\right)\dot{\phi}^2+r_w r_f\dot{\phi}\dot{\theta}\cos\theta+\frac{1}{2}m_f r_f^2\dot{\theta}^2 +\frac{1}{2}I_w\dot{\phi}^2+\frac{1}{2}I_f\dot{\theta}^2+\frac{1}{2}I_m dl^2\left(\dot{\phi}-\dot{\theta}\right)^2 \quad (3)$$

$$U = m_w g r_w + m_f g\left(r_w + r_f\cos\theta\right) \quad (4)$$

Substituting (2), (3), and (4) into (1), we have mathematical model of the unicycle as demonstrated in (5).

$$\begin{cases} \ddot{\phi}=\dfrac{b_2}{b_1}\dot{\theta}^2+\dfrac{b_3}{b_1}+\dfrac{b_4}{b_1}\dot{\phi}+\dfrac{1}{b_1}\tau \\ \ddot{\theta}=\dfrac{c_1b_2}{b_1}\dot{\theta}^2+\dfrac{c_1b_3}{b_1}+\dfrac{c_1b_4}{b_1}\dot{\phi}+\dfrac{c_1}{b_1}\tau+\dfrac{1}{2a_2}m_f g r_f\sin\theta \end{cases} \quad (5)$$

Where

$$a_1 = \frac{1}{2}m_w r_w^2 + \frac{1}{2}m_f r_w^2 + \frac{1}{2}I_w + \frac{1}{2}I_m dl^2 \quad (6)$$

$$a_2 = \frac{1}{2}m_f r_f^2 + \frac{1}{2}I_f + \frac{1}{2}I_m dl^2 \quad (7)$$

$$b_1 = 2a_1 - \frac{1}{2a_2}\left(m_f r_w r_f \cos\theta - I_m dl^2\right)^2 \quad (8)$$

$$b_2 = m_f r_w r_f \sin\theta \quad (9)$$

$$b_3 = -\frac{1}{2a_2} m_f g r_f \sin\theta\left(m_f r_w r_f \cos\theta - I_m dl^2\right) \quad (10)$$

$$b_4 = -\mu_\phi \quad (11)$$

$$c_1 = -\frac{1}{2a_2}\left(m_f r_w r_f \cos\theta - I_m dl^2\right) \quad (12)$$

III. PD CONTROL

A PD controller consists of proportional control and derivative control, as demonstrated in Figure 2. The designer adjusts proportional gain K_p and derivative gain K_d in order that the controller can output appropriate control value u(t) to minimize the error e(t) for achieving expected control performance. The relationship between input and output of a PD controller is as equation (13) shows.

$$u(t) = k_p \cdot e(t) + k_d \cdot \frac{d}{dt}e(t) \quad (13)$$

The PD controller is a SISO (single-input single-output) system. If we want to balance the unicycle and keep the displacement of the unicycle not far away from a certain starting location at the same time, it requires a system composed of two PD controllers, one for controlling the inclination, θ, and another for the wheel angle, ϕ. The structure of the double-PD controller is shown in Figure 3 in which the output of each PD controller is summed up to be the control value, u, in each control step.

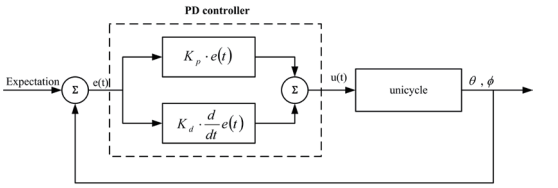

Figure 2. Structure of a PD controller

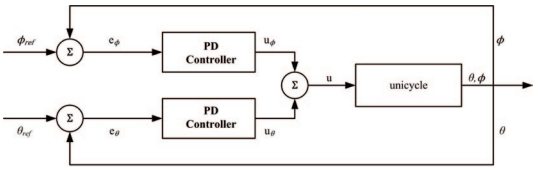

Figure 3. Structure of a double-PD controller

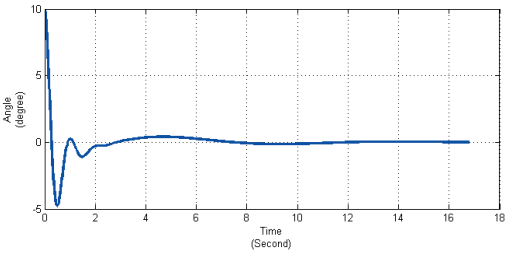

Figure 4. Unicycle inclination variances under double-PD control

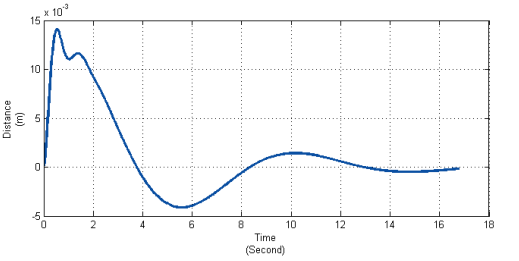

Figure 5. Unicycle displacement variances under double-PD control

TABLE II.
PARAMETERS OF THE UNICYCLE IN SIMULATION

Symbol	Definition	Value
m_f	Mass of the body	11(kg)
I_f	Moment of inertial of the body	2.3467(kg)
r_f	Length between the wheel axle and center of mass of the body	0.8(m)
r_w	Radius of the wheel	0.075(m)
m_w	Mass of the wheel	1(kg)
I_w	Moment of inertial of the wheel	0.5625(m)
μ_ϕ	Coefficient of viscous friction between the wheel and ground	0.001(Nm•sec/m)
g	Gravitational acceleration	9.81(m/sec^2)
I_m	Moment of inertia of the motor axle	0.611x10-4(Kg•m^2)
d_i	Reduction ratio of gear	30

IV. SIMULATION RESULTS

Figure 4 and 5 are simulation results of the unicycle, with initial inclination 10° and other parameters listed in Table 2, under the control of the double-PD control method by choosing Kpθ = 80, Kdθ = 10, Kpϕ = 0.2, and Kdϕ = 0.2. After about 2.9 seconds, the unicycle reached stabilization at round 0 degree of inclination and ±0.5 cm of displacement.

V. SYSTEM ARCHITECTURE

Demonstrated in Figure 6 is the system architecture of the implemented electric unicycle. The operation process of the system starts from that the CMOS image sensor captures an image and sends the image to the image processing circuit and the motor encoder sends pulses to the pulse counting circuit for computing motor speed as well. The image processing result and motor speed are transferred to the balancing controller to calculate the control value. Finally, the D/A converter converts the control value into analog voltage for motor driver module to drive the motor.

Figure 7 is the partition of the FPGA, where the image processing unit and motor speed counter are implemented by hardware, and the rest of the system is implemented in software which is responsible by the Nios II processor. The software and hardware are combined by the design methodology of software/hardware co-design.

Figure 8 shows the resulting structure of the system consisting of a DC servo motor, a COMS camera, a SoPC, a motor driver, a D/A converter, a wheel, and the skeleton with 80cm in height and 11kg in weight.

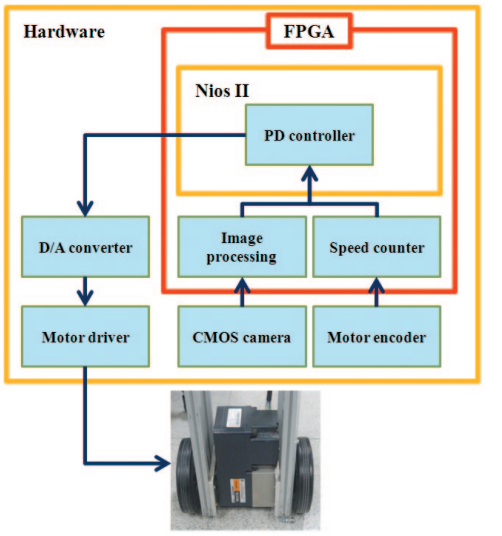

Figure 6. System architecture of the unicycle

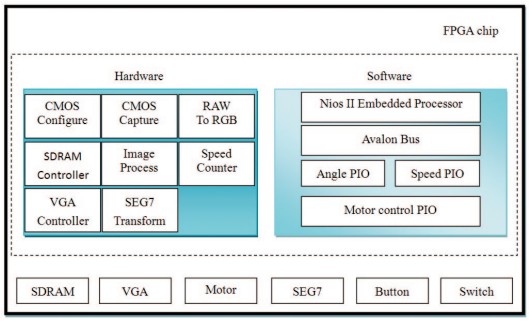

Figure 7. Software and hardware partition of the FPGA

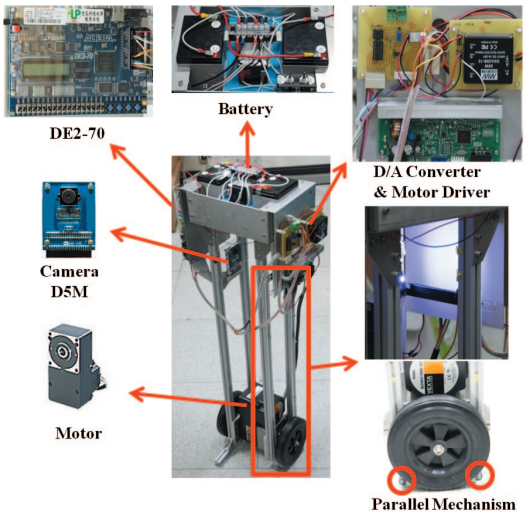

Figure 8. The resulting unicycle

VI. IMAGE PROCESSING

The CMOS camera captures the image of a white horizontal bar for computing the inclination of the unicycle, as can be seen in Figure 9. Images captured versus motions of the unicycle are demonstrated in Figure 10 and the image processing procedure is summarized in Figure 11 and explained as follows.

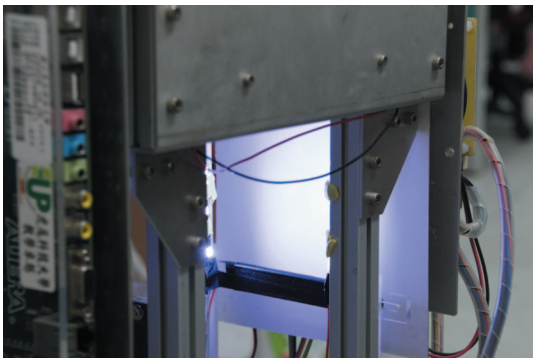

Figure 9. CMOS camera on the top of the unicycle

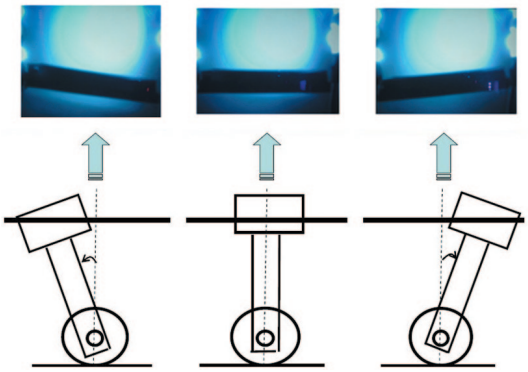

Figure 10. Images captured versus motions of the unicycle

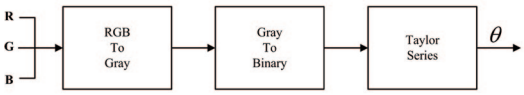

Figure 11. Image processing flow

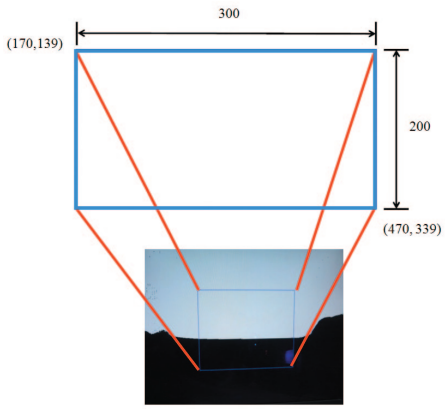

Figure 12. The image with a line in the frame

A. RGB to Gray

Add R, G, and B values of each pixel in the image and average the sum to be the resulting gray value of each pixel.

B. Gray to Binary

The purpose of this step is to filter out the noise of the image. A threshold between 0 and 255 is chosen to determine if a pixel is categorized as

1, when the pixel's gray value is greater than the threshold; as 0, vice versa.

$$\text{Binary}(x,y)=\begin{cases}1 & \text{Gray}(x,y)\geq \text{threshold}\\ 0 & \text{otherwise}\end{cases} \quad (14)$$

C. Body Angle Computation

Draw a 640x480 rectangular frame in the binarized image which has coordinates (0, 0) on the upper left corner and (639, 479) on the lower right corner of the frame. As depicted in Figure 12, the reference line lies in the frame of the image. The vertical pixel distance b and horizontal pixel distance a are employed to calculate the angle θ according to equation (15). Since the implementation of the computation is by hardware circuit, Taylor series has been used in the circuit to approximate $\tan^{-1}(b/a)$.

$$\tan^{-1}\left(\frac{b}{a}\right)=\left(\frac{b}{a}\right)-\frac{\left(\frac{b}{a}\right)^3}{3}+\frac{\left(\frac{b}{a}\right)^5}{5}-\frac{\left(\frac{b}{a}\right)^7}{7}+\cdots \quad (15)$$

VII. EXPERIMENTS

Double-PD control has been employed to balance the unicycle and the experimental results are exhibited in Figure 13-15 which including angle of the body, displacement of the unicycle, and control voltage, respectively. The gains are Kpθ=137, Kdθ=60, Kpϕ=1.3, and Kdϕ=0.06 It can be seen in 60 seconds of experimental time that the unicycle has been well controlled in accordance with the facts that the angle and displacement have been limited within ±3° and ±0.2m, respectively and the control voltage has never exceeded the limitation ±5V.

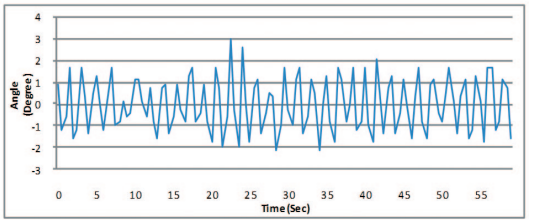

Figure 13. Double-PD experimental result (angle of the body)

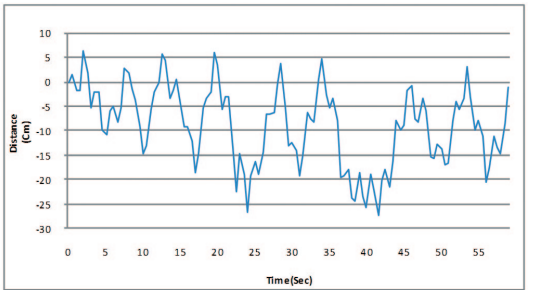

Figure 14. Double-PD experimental result (displacement of the unicycle)

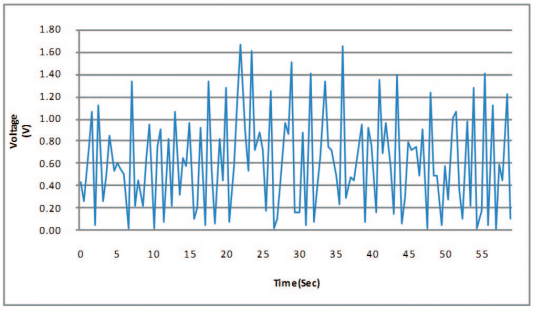

Figure 15. Double-PD experimental result (control voltage)

TABLE III. RESOURCES USAGE OF THE FPGA

FPGA (70,000LEs)						
System			LEs	Total (LEs)	Hardware (LEs)	Resources usage
Hardware	Image Processing	RGB to Gray	93	632	2766	0.9%
		Binarization	60			
		Coordination	33			
		Taylor Expansion	446			
	Encoder Counter		31			0.04%
	Other		2103			3%
Software			3238			4.6%
Total Resources usage						8.6%

CONCLUSIONS AND FUTURE PERSPECTIVE

This article reports the design and implementation of an electric unicycle balanced by a SoPC using the double-PD control method based on image data which is captured by a CMOS

camera. From both simulation and experimental results the resulting system has met the control requirement.

The resources usage of the FPGA is summarized in Table 3. To complete the entire unicycle system it is surprising that the system has merely taken 8.6% of the FPGA resources and the speed of the image processing unit has been up to 60 images per second. According to the test results, it has been confirmed that the system outputs control commands in the speed of 5 commands per second is good enough for controlling a plant like the unicycle as we implemented.

There are still rooms for improvement this work. Firstly, next step we are going to test the control effect by applying other control methods, like back-stepping, sliding mode, and adaptive nonlinear control, to the implemented unicycle. Secondly, in the future we hope to enhance the unicycle with more functions, such as remote control, up and down slopes, carrying objects, and so on.

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Holographic Display System Based on FPGA and DLP Technology

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Abstract — We describe a light field display able to present 3D graphics to multiple viewers around the display. The display consists of a high-speed DLP projector, a spinning mirror and FPGA circuitry to decode specially rendered HDMI video signals. The display uses a customized Nios II processor to rendering 1440 images per second 3D graphics, projecting onto spinning display with 3.75 degree separation up to 15 updates per second.

Keywords — Holographic Display, FPGA, DLP, NIos II, HDMI

I. INTRODUCTION

The rapidly emerging technology in recent years on multi-color, large-screen, high-definition projection system and other new technologies are being actively explored. A new projection manifestation method is being searched to address the needs of the various areas of the three-dimensional display. However, the existing commercial 3D TV still remains in the original binocular "pseudo-three-dimensional" technology. Long-time view can cause visual fatigue and even physical discomfort such as dizziness due to fixed perspective of traditional 3D TV view angle and fixed eye's focal point. Therefore, we are looking forward to a technological revolution to change the drawbacks of traditional 3D display technology so that images could be observed from any angle from the corresponding three-dimensional image.

For this purpose, we have designed and implemented a three-dimensional holographic imaging system. the system is a composition of a holographic image generator, DLP (Digital Light Processing) projector and a high-speed rotating screen. Holographic image generator is the signal source of a DLP projector, real-time and high speed three-dimensional holographic image is sent to the DLP projectors; Under the control of the holographic image generator, the micro mirror array (Digital Micromirror Device, DMD) of the DLP projector reflect light to the rotating display; Angular velocity of high-speed rotating screen is in accordance with the requirements of specific rendering algorithms, to ensure the correct projection frame is synchronized with the high-speed rotating screen. Thus, providing a new direction for three-dimensional, 360-degree, full range static and dynamic images projection technology. The subject being studied differs from traditional 3D TV that utilizing human eye binocular visual posed effect; observer can view the corresponding three-dimensional image from any angle. The designed is based on light reflection to implement a holographic three-dimensional effect, to give a real sense of three-dimensional.

From a market point of view, the design will enjoy a wide range of applications from consumer appliances, entertainment, to medical industrial design as well as scientific research and others. In the early stages of development, this can be applied to high-tech products advertisement. Imagine when Altera announce a now produce

at a conference hall, the light slowly goes out, the center of circular podium emerges a three-dimensional scene of a well fabricated 22nm FPGA, each angle demonstrate a different scenario, the chips then breaks up layer by layer, displaying its shocking internal structure. After the maturity of this technology, especially when the high-speed rotating screen is replaced by other light controlling device, will completely change how mankind access visual information and the traditional flat panel displays will be replaced.

Of course, a long way to go is ahead of us to really implement the technology. We hope that this topic can be used as a guide, diversify our thinking and to explore a more convenient and efficient three-dimensional displaying methods. We believe that the rapid development of integrated circuit and the use of low-power, high-performance optical path controlling technology in holographic display must become a hot area of future technological search and marketing.

In device selection, we choose Terasic DE3 platform equipped with the ALTERA Stratix III family EP3SL340H1152C2NFPGA FPGA chip. The chip contains up to 338,000 logic cells and high-speed external memory interface supporting DDR, DDR2, DDR3, and as much as 1104 user defined interface to meet the demand for high-speed, multi-IP library support in prototype development, suitable for high-speed and large-amount data processing requirements.

II. Functional Description

This system create a holographic image by splice 2D images, we need present a real object visually around all 360 degrees, so the system must process a lot of data in a very short time. The human eye to do a sampling system, based on previous studies, when the sampling frequency is 24 fps and above, we see better image continuity. If the Frame rate is higher the Visual effect is better. If around the 360 degrees output a image one by one degree, and fulfill the need of human eye (above 24 fps), so the system need output 8640 frames in a second (360 * 24 = 8640). It is difficult to complete for a normal projector, the DLP projector system also can't finish this task. Our DLP can only output maximum 4000 fps. So we calculate a balance frame rate number is 1440 fps. And in this fps, the Image quality and the system Performance can be balance. That need us sampled once every 3.75° in the horizontal sampling of the real object 360 degrees, that is, a circumference of 96 samples. Each angle giving the eye within second output 15 frames, the system effect is nice and it looks like a real object. Now more popular on the market of image transfer protocol VGA, DVI, HDMI, they support each pixel 16 \ 24 \ 32-bit color image transmission. Today, any video transmission interface can not be achieved within 1 second transmission of thousands of frame images, the frame rate of the video transmission interface protocol typically between 60 to 80 fps. However, if the use of Each pixel contains 24-bit chroma, sacrificing color, improve the speed, adding a different frame of information in each bit in the frame rate of 60 fps can be transmitted in seconds 60 * 24 = 1440 frame images, can greatly speed up the the ordinary transfer port transmission rate. The TI Lightcrafter development board has save a lot of work, especially at the decoder side, the on-board FPGA has complete the realization of image compression decoding, which been said before. we need to do is to transmit correct video stream via HDMI transmission protocol to the development board, so you can get on the DLP image decompression.

First need to sample imaging object, the object may be the reality of the object can also be rendered 3D computer model. Shooting around the object in the same horizontal plane, every 3.75 ° take a picture, so shooting finished after a week, you can get 96 images of 3D objects. Next binarize the color pictures taken. Compressed into 24 binarized images captured using the HDMI transfer protocol, in each pixel of the frame

constituted by the 24-bit. In order to enhance the clear view of the binarized image, we use the Dithering algorithm, the binarized image obtained by the MATLAB superimposed every 24 binarized images, composed of a new 24-bit color photographs. These original 96 frames become the 4 images by processing.

These images through a computer sequentially stored in the SD card, so that the CPU make these images are sequentially dump DDR2 memory to generate a video stream to take advantage of high-speed access speed of the DDR2 memory. Then the processed video stream input to the HDMI control module, a 608X684 resolution of the frequency of 60 Hz video stream is output to the projector. When the screen out of the projector and the rotational speed of the screen, can be matched. we will obtain a clear stereoscopic image.

III. Performance parameters

The system is a holographic image player, which consists of Image Pusher, High-speed Rotating Screen and DLP projector. The holographic image has a 360-degree viewing angle, so you can watch the 3D image at any direction in horizontal. The image of a resolution of 608*684 pushed by the Image Pusher to the DLP projector in the rate of 1440 fps. So image can update in every 3.75°, and made the frame rate to 15 fps in each angle.

Development platform is DE3, produced by Terasic Technologies, Inc. Because the system include a large number of computing and data transmission. The platform has an Altera Stratix III EP3SL340H1152C2N FPGA, a wealth of on-chip resources, and the speed class is C2, the performance can meet our design requirement.

IV. Design Structure

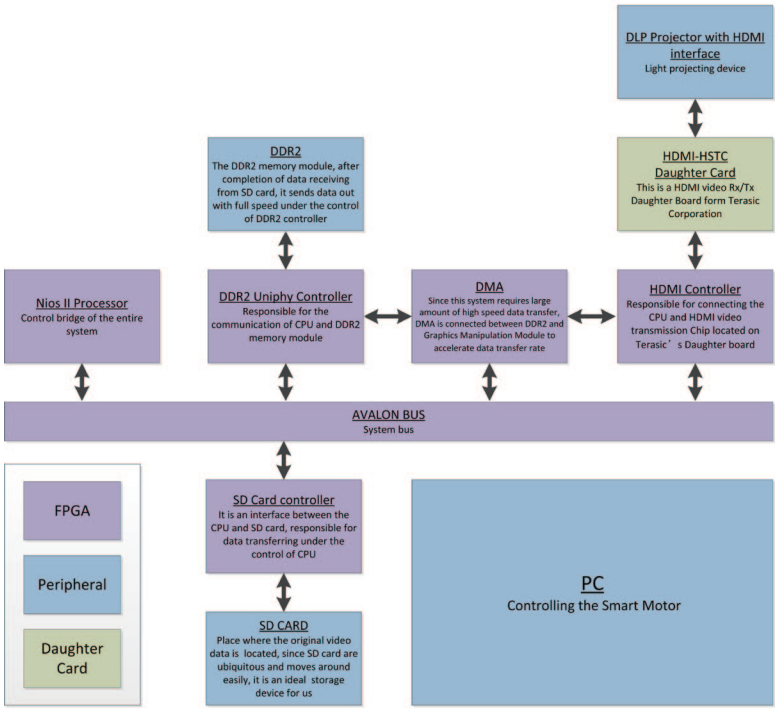

Figure 1. Block diagram

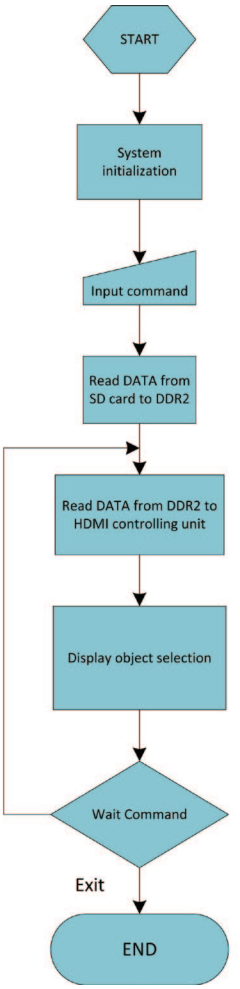

Figure 2. Flow chart

V. Design Method

This design is mainly constituted by Image Processor and Pusher, High-speed Rotating Screen and DLP projector. The FPGA achieve the part of Image Processor and Pusher.

The Image Processor and Pusher constituted by NIOS II processor, SD CARD, SG DMA, THDB-HDMI, DLP and the other hardware. The software includes BSP, driver and other algorithm code.

The process of the design is as follows:

[1]. System Requirements.

[2]. Module division.

[3]. Function implementation of each module, module testing and integrated IP core.

[4]. System testing, NIOSII software design.

[5]. System debugging and verification.

Here we will detail the design process of our system:

[1]. System Requirement Definition: We verified the system requirement through group discussion and meeting. Because 3D image system require large memory resources and high-speed processing to ensure real-time and synchronize, so the requirement is :

- Daughter board with HDMI interface, which used to translate the image date, processed by FPGA, to the DLP via HDMI cable.
- 1GB DDR2 memory, because a holographic image in the horizontal plane includes 96 pictures, this is a large amount of data.
- SD-card, which used to store the image to be displayed.
- DLP, the LIGHTCRAFT series DLP of TI Co. is so fast to meet our requirement of project in a speed of 1440 fps. There is also an Altera FPGA on it.

[2]. Module division: The whole system is divided into the SD CARD Data Storage module, the DDR2 Data Storage module, Image Data Processing module, SG DMA module and HDMI module. And defines the interfaces between the various modules. Decide to use a NIOSII processor to control the data flows. The details refer to our design configuration diagram.

[3]. Function implementation of each module, module testing and integrated IP core: We completed the module one by one. And test them individually. Finally to integrate the IP cores by the avalon bus in the QSYS tools.

[4]. System testing, NIOSII software design: First, use the QYS tool to connect the IP cores together by avalon bus. Second, built our software project and BSP in the NIOSII SBT for Eclipse. Third, add the driver of each module to the NIOSII project and programming. Finally, our system is built up. But you know, a new system is always having a lot of bugs. So we used about a month to debug. During this period, we used Modesim to simulating; used SignalTap tools to observe the waveform, and used TimeQuest Timing Analyzer tools to add timing constraints.

[5]. System debugging and verification: In this period, we have to test and adjust the performance of the entire system, such as adjust the resolution to achieve a better result.

VI. Design Features

Holographic projection is an emerging technology; a wide range of applications is not enough. Universal realization method is use computer to control multiple projectors to imaging in a reflection. Our method is the lowest cost and trying to design a custom dedicated chip to replace the computer.

EP3SL340H1152C2N chip is a high-end product of ALTERA Company. On-chip resources are very rich, and the speed grade is C2. This feature is appropriate to meet the requirement of high-speed data processing. What's more, DE3 platform has a DDR2 interface, which gives a rich memory space to the huge data. Last but not least, the Terasic HDMI-HSTC daughter board is so convenient that we can pusher the image to the DLP projector.

CONCLUSIONS

This contest has a deeply meaning for us, through the design and implementation of a customized system, we have mastered the full set of FPGA design methods, enforced information collection skills, team collaboration innovative thinking, and hard-working spirits.

First, in the system requirement analysis phase, due to the harsh demanding requirements of our system, we did a full survey of all types of ALTERA FPGA devices and Terasic development board and ultimately decided to use Terasic DE3 board with the equipment of STRATIX III family FPGA as our platform. In addition, the selection of the HDMI daughter board and DLP projector have cost a lot of time and effort, meanwhile we also gained a lot of experience in equipment selection resource utilizations.

Secondly, in the process of module design, we refer to the many altera provided IPs, many of the IP cores we need could be found at the official website of the Altera, through simple modifications can we quickly integrate into our system, which greatly reduced our efforts and time in code design. In system synthesis process, we used QSYS a tool, with it's easy to use graphical interface, with only mouse to drag can we to complete the connection between the various modules. Nios II SBT for eclipse tools also provides us with a friendly software development environment to facilitate software development.

Again, I deeply appreciate the longer perfect system must have a variety of bugs, but often the system of testing and bug fixes time is much longer than the development time. With SignalTap tools help, we observe a waveform diagram of the interface data observed every moment needed, and ultimately find the root of the problem. and TimeQuest Timing Analyzer tool allows our system to be able to meet our demanding timing requirements.

Finally, we do appreciate the terasic company's technical support; enthusiastic detailed answers to us when we met the HDMI daughter board cannot

support of our DLP 608 × 684 resolution issues. Though Entire project, the tacit understanding between the members of our team has improved, and also develops our common division of the ability to discuss and resolve the problem. In the commissioning phase of the project, we encountered a lot of problems, thanks to the guidance of our instructor Cao Jian, help us solve many problems. Thank all who concern and support of our project, without your help our project would not be so smooth completed.

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Implementation of a Calligraphy Mechanical Arm Based on FPGA

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Abstract — Dimensional mechanical arm is an important development direction of mechanical arm, which plays a significant role in the industrial and agricultural production. The system is developed based on the platform DE2, which makes full use of FPGA hardware structure and Nios II flexible embedded processing capability. The mechanical arm motion is simplified through analysis of multi-dimension manipulator motion. The related control algorithm and hardware driver are implemented to copy Chinese calligraphy as well as accomplish Chinese calligraphy action as lifting and pressing, writing sketches and other functions. The experiment results proved the efficiency of the design.

Keywords — Mechanical arm, multi-dimensional, calligraphy, NIOS II, FPGA

I. INTRODUCTION

Nowadays little has done on the research of calligraphy demonstration by the mechanical arm. The control effect is more intuitive and attractive by studying the starting, bearing, rotating and folding of calligraphy. More could be done in multi-joint movements on the planar contour through the research of the multi dimension mechanical arm for calligraphy demonstrations. The design is focus on multi-axis motion localization algorithm and Chinese characters font structure. The former is realized by linear interpolation algorithm, the latter is made up of strokes order library, strokes library, location library. By searching the Chinese characters stroke order, stroke and stroke position to form a Chinese character.

The paper is organized as follows. The multi-axis motion localization algorithm is introduced in section 2. The database of Chinese characters font is described in section 3. The experiments realization is given in section 4. Finally, concluding remarks are drawn in the last section.

II. MULTI-AXIS MOTION LOCATION ALGORITHM

The structure of the mechanical arm can be divided into vertical type and horizontal mechanical type. The vertical type comprises four servos and one stepping motor, of which there are three servos driving the mechanical arm to do concertina movements in the vertical plane, whose structure is shown as Figure 1.The horizontal type has 3 stepping motors which drive the mechanical arm to do concertina movements on a horizontal plane, whose structure is shown as Figure 2.

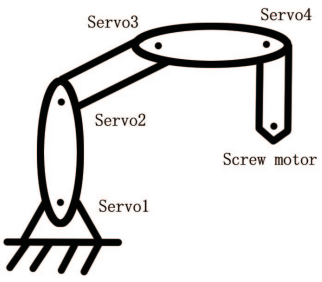


Figure 1. The front view of the vertical type

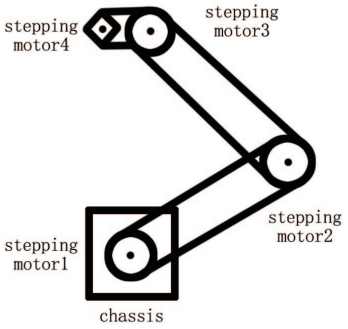


Figure 2. The vertical view of the horizontal type

A. The location algorithm of the vertical type

Among four servos, three of them are in the vertical plane and one in the horizontal plane. We use the polar coordinate system to transform from the X-Y coordinates to obtain simple formula. The structure is shown as Figure 3.

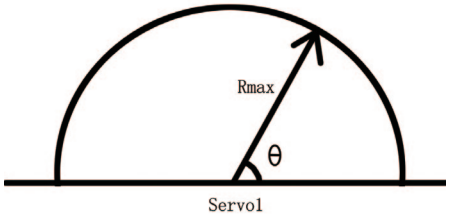


Figure 3. Location of polar coordinate

θ is the range of rotation of servo1. Rmax is the maximum extension of the mechanical arm. By changing the size of R, and angle θ, an arbitrary point in the semi-circular area can be reached. The size of R is determined by servo 2, 3, 4 which belong to the same plane. Because the writing brush is generally perpendicular to the paper, the brush is fixed in the servo 4. The structure is shown as Figure 4.

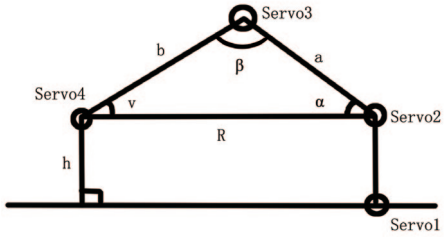


Figure 4 The structure of the vertical type

Servo 2, 3, 4 form a triangle, and the distance between servo1 and servo2 is the same as the distance between the brush and the paper, a, b, R are known, α, β, γ can be obtained as following.

$$\cos\alpha = \frac{R^2 + a^2 - b^2}{2aR} \quad (1)$$

$$\cos\beta = \frac{a^2 + b^2 - R^2}{2ab} \quad (2)$$

$$\cos\gamma = \frac{b^2 + R^2 - a^2}{2bR} \quad (3)$$

The results are:

$$\alpha = \arccos\left(\frac{R^2 + a^2 - b^2}{2aR}\right) \quad (4)$$

$$\beta = \arccos\left(\frac{a^2 + b^2 - R^2}{2ab}\right) \quad (5)$$

$$\gamma = \arccos\left(\frac{b^2 + R^2 - a^2}{2bR}\right) \quad (6)$$

The transform formulas from X-Y coordinates to polar coordinates are:

$$X^2 + Y^2 = R^2 \quad (7)$$

$$\theta = \arccos\left(\frac{X}{R}\right) \quad (8)$$

From the above, if the X-Y coordinates are given, then certain value of R and θ could be acquired, and finally the value of α, β, γ could be determined.

Since the movements of the mechanical arm is inside the semicircle, It is hard to complete vertical operation after locating at a certain point if only the four servos are driven, therefore, a stepping motor with a screw rod is fixed on servo 4 to solve the problem, as shown in Figure 5.

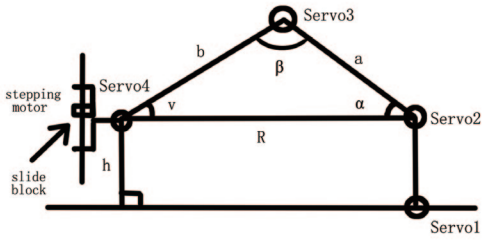


Figure 5. The vertical plane diagram of the mechanical arm with Z-axis

The stepping motor makes the slider up and down through the screw rod.

The servo is driven by the pulse width control, for a given periodic PWM signal, the servo is fixed at a specific angle and torque force is great. If there is large pulse width difference between the pulse trains, the mechanical arm would need large torque force to rotate, which would greatly shorten the expectation of the servo, and such motion does not conform to the smooth and soft of the brush writing. While the stepping motor is driven by the number of pulses, therefore, if the period of pulses is shorten down, the stepping motor's rotation speed will become faster, vise versa, the rotation speed will be slower.

The servos can be controlled by the following steps:

[1]. Loading value A into the register 1 and register 2.

[2]. Comparing the value between the register 1 and the register 2. If B>A then A++ until A=B, if B<A then A– Until A=B.

[3]. Loading value A into the register 2.

[4]. Loading the new value B into the register 1.

[5]. Turn to (2).

The variation of the initial angle is determined by the value A. While the new value B>A, then A is accumulated until A=B, however if B<A, then A is decremented until A=B.

The mechanical arm has four servos, as a result after a servo rotates to a new angle, it couldn't move until the rest motors move to the desired angle, which can guarantee the lag or advanced action not appear among servos.

The step rotation speed can be controlled by 20ms cycle's delay. The shorter delay time, the faster a servo rotates a degree.

B. The location algorithm of the horizontal type

It is more consistent with the human's writing motion path by using the horizontal mechanical arm. The three stepping motors are positioned in the horizontal plane. The polar coordinates are described as Figure 6.

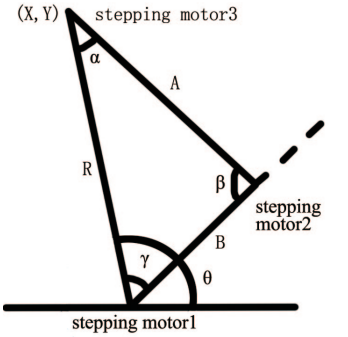


Figure 6. The structure of the horizontal type

The motion range of the stepping motor is larger than that of a servo and the precision of the former is higher too, therefore the coverage area of the horizontal type is larger than that of the vertical one. However, due to the limit of human motion, set 0<=β<=180°, the stepping motor 1, 2, 3 form a

triangle, other angles can be obtained by using the cosine theorem (as eq. (4), (5), (6)), thereby the mechanical arm could be controlled to move to a specific point.

The control of a stepper motor is different from that of a servo, which makes the initialization of the stepping motor be hardly controlled by a program, so the infrared sensors are installed on the mechanical arm joints as the aid of initializing location.

III. CHINESE CHARACTER FONT

Chinese characters font is composed of the stroke order, the stroke and the position table. The traditional way of describing Chinese characters is the lattice. Each Chinese character is formed by dozens or even hundreds of points. To construct a more than 2000 Chinese characters font will need large amount of data, which is a disadvantage for storage. The data redundancy can be greatly reduced as well as the efficiency of Chinese characters is greatly improved through the construction of the three tables.

Three tables are created as following:

A. The Stroke Order Table

Stroke order table records the order of each Chinese character. For example, the stroke order of the Chinese character " 天 " (day) is horizontal(一), horizontal(一), left-falling(丿), right-falling(乀). If 1 stands for across stroke, 2 for left-falling stroke and 3 for right-falling stroke, then the stroke order of " 天 " is "1123".

B. The Stroke Table

There are many kinds of strokes in Chinese characters, among them the most common used basic strokes are: dot, horizontal, vertical, left-falling, right-falling, rising, turning and hook, which are shown in Table1. If the style of calligraphy is the same, then the writing sketches of different Chinese characters are similar, so we can create a stroke table to record the basic strokes of a Chinese character stroke structure. When there is a need to write a Chinese character, the first to do is looking up the strokes in the basic stroke table, and then the mechanical arm will be controlled to move to the desired position and write down the corresponding amplified or lessened strokes.

TABLE I. The commonly used strokes in Chinese Characters

Strokes	Name	Strokes	Name
	dot		right-falling
	horizontal		rising
	vertical		hook
	left-falling		turning

C. The Position Table

The position table describes the location and the size of each stroke of a Chinese Character. The coordinates of the starting point and the end point of each stroke in a Chinese Character are recorded. Taking the Chinese character " 天 " as an example, its location record concludes the starting point coordinates and the end point coordinates of the first horizontal(一), the second horizontal(一), left-falling(丿), right-falling(乀). The size of a stroke is controlled by the distance between the initial coordinates and the end coordinates. The proportional transform algorithm is introduced in the system. While the distance from the starting point to the end point is increasing, the stroke will getting bolder, otherwise if the distance from the starting point to the end point is decreasing, the stroke will getting thinner.

From the above, the contouring motion track of a Chinese character can be output. Linear

interpolation algorithm is also used because the table records only several sampling points of the stroke. The remaining points of the stroke are supplied by applying the interpolation algorithm, which not only reduces the quantity of font data, but also improves the writing accuracy of the mechanical arm.

IV. EXPERIMENT AND RESULTS

The System is divided into three parts: MTL multi-touch LCD screen, FPGA-DE2 and the mechanical arm. The structure of the system is shown as Figure 7.

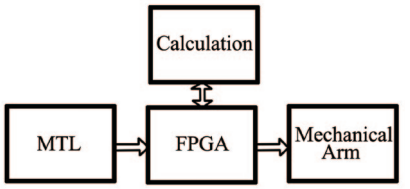


Figure 7. The structure of the system

The external data (Chinese characters) is acquired by multi point touch LCD screen which is specialized for the FPGA application with the full function of the capacitive touch screen supporting for multi-point touch and gesture recognition, then after the calculation of FPGA the mechanical arm will copy the corresponding character.

The system is implemented based on the platform of Altera FPGA-DE2. First of all, the processing ability and the calculation speed of FPGA is superior to that of the ARM, further more with the ability of parallel controlling, the multiple dimension control of the machine arm can be well completed. In addition, the Nios II embedded processor is used as the mechanical arm controller, which is the second generation of on-chip programmable processor with the Harvard structure and 32 bit instruction set. The modular structure makes it become more flexible. Compared with the traditional processors, the number and variety of peripherals could be increased or decreased during the design time while using Nios II system. The designer can use ALTERA development tools such as SOPC Builder to create software and hardware development platform, namely use SOPC Builder to create a CPU soft core and parameterized interface bus Avalon, and quickly integrate hardware system (including a processor, memory, peripheral interface and customized logic circuit) and general software into a single programmable chip. Besides, SOPC Builder also provides standard interfaces, so that the users can attach the peripheral circuit made by themselves to Nios II soft-core, which makes debugging more convenient for our system.

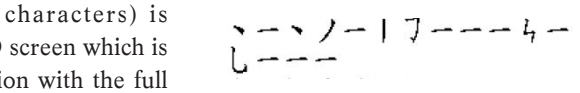
The following is a demonstration of the experiment.

The Chinese character “ 龍 ”(dragon) is used as a demo.

At first, look up the stroke order of “ 龍 ”:

The Chinese character: 龍

Strokes:



The number of strokes: 16

The standard Chinese character is shown as Figure 8.

Figure 8. Chinese calligraphy “龍”

The copy of the mechanical arm is shown as Figure 9.

Figure 9. The copy of mechanical arm

The similarity between the mechanical arm's copy and the standard calligraphy reaches 83%. The error is acceptable considering the artificial font has a certain degree of distortion, and the accuracy of the servos in the mechanical arm is not so high.

CONCLUSIONS

The principle of the servos and the stepping motors is discussed by applying the mechanical arm to write Chinese calligraphy. The location algorithm and model are introduced about two kinds of multi-dimensional mechanical arm. The screw motor is attached to the end of the mechanical arm which provides fine tuning in the vertical direction, thus greatly improves the mechanical arm's flexibility and initiative. The unique Chinese characters font structure makes the mechanical arm personified writing Chinese characters better. The mechanical arm writing brush calligraphy shows smooth and soft with the aid of the interpolation algorithm.

Multi dimensional location model and algorithm makes the mechanical arm adapt to the actual needs (writing Chinese characters) better. The development efficiency is greatly improved by combining the FPGA hardware structure and the flexible processing ability of Nios II.

ACKNOWLEDGMENT

The authors thank gratefully for the colleagues who have been concerned with the work and have provided much more powerfully technical supports. The work is supported by Altera international Limit and You Jing Science and Technology Co. We learn more about the MTL multi-touch LCD and the DE2 development board during the competition. We would also like to thank our teacher Zhou Wei Xing who gives us a strong material support and academic guidance.

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Implementation of a Quad-Rotor Robot Based on SoPC

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Abstract — This work uses a SoPC platform as the flight controller of a quad-rotor aircraft. By CAD/CAM technologies the fuselage of the aircraft is built. The posture of the aircraft is stabilized according to the sensory data from a three-axle gyroscope and a tri-axia accelerometer. Additionally, a CMOS camera mounted on the bottom of the aircraft and an ultra-sonic sensor enables it to detect and track the object of interest on the ground while the aircraft is flying.

Keywords — FPGA, CAD, CAM, gyroscope, accelerometer

I. INTRODUCTION

With the progress of science and technology in recent decades, it is possible for scholars to develop small UAVs (Unmanned Aerial Vehicles). Among which the four-rotor unmanned aerial vehicle (Quad-rotor) has drawn a lot of research attention.

A Quad-rotor helicopter is able to take off and land vertically as well as hanging and horizontally flying, making it becomes an ideal monitoring tool in the sky. It can be utilized in various civil and military operations, for example: search and rescue operation, monitoring the air pollution and traffic condition, etc.

A quad-rotor vehicle has equipped with four brushless motors which divided into two pairs rotated in opposite directions. Contrasting to standard helicopter, the quad-rotor has advantages in security and efficiency, and there even have been remote control toys of quad-rotor helicopters on the market, but they are still lack of stability [1-2]. Many research groups have begun developing quad-rotor vehicles as the targets for robotics research [2-10], and several groups have studied to build quad-rotor UAVs serving as general unmanned aircraft [11-12].

As shown in Figure 1, quad-rotor helicopters have two pairs of propellers (1, 3) and (2, 4) rotating in opposite directions in order to compensate the phenomenon that the helicopter spins, and through changing the turning speed of the motors, the helicopter can create and change lifting force as well as its posture and moving direction. Changing rotational speed of propeller 2 and 4 vary the roll rotation and lateral movement, whereas changing the speed of propeller 1 and 3 produce the pitch rotation. The yaw rotation is the joint result of the forces of the four propellers. For example, Figure 1(c) shows the counterclockwise effect caused by the motors (1, 3) rotate in

moderate speed and the motors (2, 4) rotated in a relative high speed.

In this paper, a SoPC (System on a Programmable Chip) is utilized as the flight control system, on which a three-axis gyro and a tri-axial accelerometer are being the flying robot gesture detector, and an ultra-sonic sensor can estimate the flying height of the aircraft. Furthermore, a CMOS camera mounted on the quad-rotor is employed to enhance the quad-rotor with the function of detecting and tracking objects on the ground. The flight controller adopts the PID control law to do closed-loop control of the flying robot to achieve self-balancing, hovering flight, and object tracking missions.

II. QUAD-ROTOR DYNAMIC MODEL

An ideal dynamic model contains the gyroscopic effect caused by hardware, or rotation caused by propeller, and etc. [4]. The coordinate system E and the body frame B are shown in Figure 2. The center of mass and the origin of the body frame are assumed to be coincident.

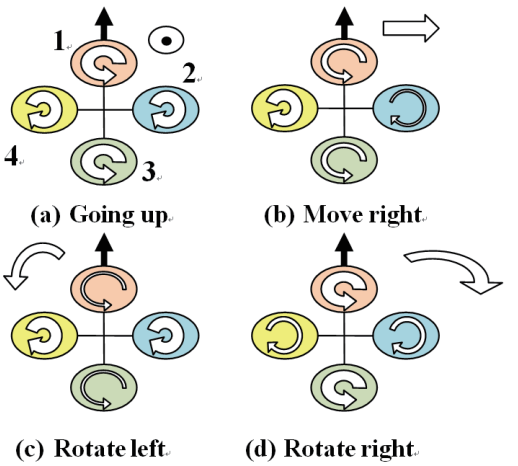

Figure 1. Quad-rotor concept motion description, the arrow width is proportional to propeller rotational speed

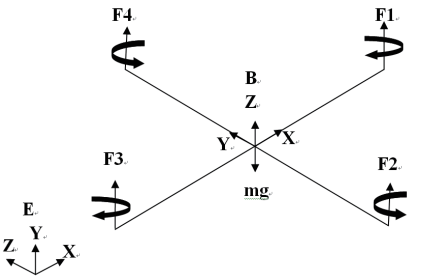

Figure 2. The coordinate system E and the body frame B of the aerial robot quad rotor.

TABLE I. SYMBOL DEFINITIONS IN EQUATIONS

Symbol	Definition
ζ	position vector
ν	speed vector (expressed in E)
R	rotation matrix
$\hat{\omega}$	skew symmetric matrix
ϕ	roll angle
θ	pitch angle
ψ	yaw angle
Ω	rotor speed
$I_{x,y,z}$	body inertia
J_r	rotor inertia
F_b	forces on airframe body
τ_b	torques on airframe body
b	thrust factor
d	drag factor
l	lever
e1, 2, 3	standard basis in R^3
g	acceleration due to gravity

Perform parameterization with Euler angles; in the given space, the rotation matrix for frame B with respect to coordinate E is $R_{B\ni E}$.

$$R_{B\ni E} = \begin{pmatrix} c\psi c\theta & s\varphi s\theta c\psi - c\varphi s\psi & c\varphi s\theta c\psi + s\varphi s\psi \\ s\theta s\psi & s\varphi s\theta s\psi + c\theta c\psi & c\varphi s\theta s\psi \\ -s\theta & s\varphi c\theta & c\varphi c\theta \end{pmatrix} \quad (1)$$

Where c=cos, s=sin.

Sastry[13] and Chriette[14] proposed that the force exerted by the external and acted on the center of the mass in rigid-body dynamics, as shown by the definition of Newton-Euler method:

$$\begin{bmatrix} mI_{3*3} & 0 \\ 0 & J \end{bmatrix} \begin{bmatrix} \dot{V} \\ \dot{\omega} \end{bmatrix} + \begin{bmatrix} \omega \times mV \\ \omega \times J\omega \end{bmatrix} = \begin{bmatrix} F \\ \tau \end{bmatrix} \quad (2)$$

$I \in \Re^{(3*3)}$ is the inertial matrix; V is linear velocity vector of the body; ω is the angular velocity of the body; J is moment of inertia.

The equation [15] of motion of the helicopter can be written as:

$$\begin{cases} \dot{\xi} = v \\ m\dot{v} = RF_b \\ J\dot{\omega} = -\omega \times J\omega + \tau_b \end{cases} \quad (3)$$

The first stage model of a quad-rotor can be written roughly as:

$$\begin{cases} \dot{\xi} = v \\ \dot{v} = -ge_3 + R_{e3}(\frac{b}{m}\sum \Omega_i^2) \\ I\dot{\omega} = -\omega \times I\omega - \sum J_r(\omega \times e_3)\Omega_i + \tau_b \end{cases} \quad (4)$$

Propellers on different axes and different moment differences act on the body.

$$\tau_b = \begin{bmatrix} lb(\Omega_4^2 - \Omega_2^2) \\ lb(\Omega_3^2 - \Omega_1^2) \\ d(\Omega_2^2 + \Omega_4^2 - \Omega_1^2 - \Omega_3^2) \end{bmatrix} \quad (5)$$

The symbol definitions are shown in Table 1.

The integrated dynamic model of the quad-rotor is shown as (6); except yaw, for motion in x, y and z axes, friction is ignored for all body movement.

$$\begin{cases} \ddot{x} = (\cos\varphi \sin\theta \cos\psi + \sin\varphi \sin\psi)\frac{1}{m}U_1 \\ \ddot{y} = (\cos\varphi \sin\theta \sin\psi - \sin\varphi \cos\psi)\frac{1}{m}U_1 \\ \ddot{z} = -g + (\cos\varphi \cos\theta)\frac{1}{m}U_1 \\ \ddot{\varphi} = \theta\psi(\frac{I_y - I_z}{I_x}) - \frac{J_r}{I_y}\dot{\theta}\Omega + \frac{1}{I_x}U_2 \\ \ddot{\theta} = \dot{\varphi}\psi(\frac{I_z - I_x}{I_y}) + \frac{J_r}{I_x}\dot{\varphi}\Omega + \frac{1}{I_y}U_3 \\ \ddot{\psi} = \dot{\varphi}\dot{\theta}(\frac{I_x - I_y}{I_z}) + \frac{1}{I_z}U_4 \end{cases} \quad (6)$$

Suppose U1, U2, U3, U4 and Ω serve as input of the system and a disturbance, we get:

$$\begin{cases} U_1 = b(\Omega_1^2 + \Omega_2^2 + \Omega_3^2 + \Omega_4^2) \\ U_2 = b(\Omega_4^2 - \Omega_2^2) \\ U_3 = b(\Omega_3^2 - \Omega_1^2) \\ U_4 = d(\Omega_2^2 + \Omega_4^2 - \Omega_1^2 - \Omega_3^2) \\ \Omega = \Omega_2 + \Omega_4 - \Omega_1 - \Omega_3 \end{cases} \quad (7)$$

III. SIMULATION

The model derived in section II has been simulated, the quad-rotor flying from coordinate (0, 0, 0) to (40, 50, 3). As can be seen in Figure 3, it has taken about 20 seconds for the quad-rotor to reach the destination and about 40 seconds to reach stable (roll, pitch, yaw) angle, (0, 0, 0).

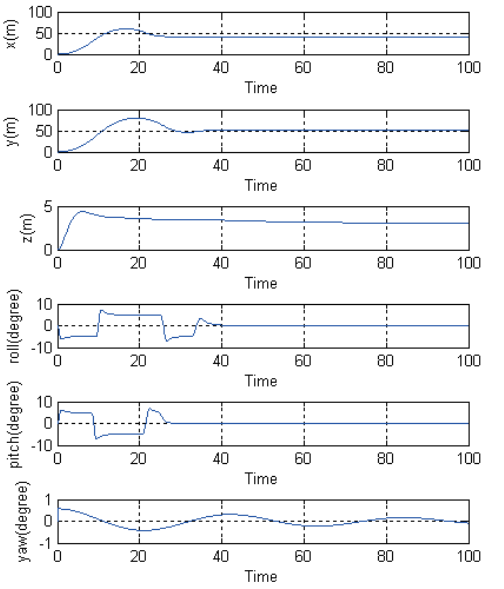

Figure 3. Simulation results of Quad-rotor

IV. MECHANISM DESIGN

This research employs the computer added design and manufacture (CAD/CAM) technologies to produce the fuselage. First, the skeleton consisting of two aluminium bars with a crossing structure are made. The four terminals of the cross are mounted with legs which are made of glass fibreboard material in order to reduce the weight while maintaining the strength. Shown in Figure 4 is the completed structure.

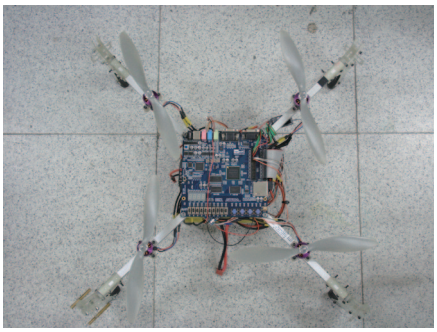

Figure 4. Quad-rotor fuselage

V. SYSTEM ARCHITECTURE

The flight control system of the quad-rotor combines the remote control and automatic stable functions. The aircraft receives remote control commands from the operators together with the multi-sensor signals to perceive its posture and to tune the flying automatically. The system adopts the PID control method to control the vehicle. Systematic structure of the quad-rotor is shown as in Figure 5, consisting of the following sub-system:

A. SoPC

A platform with a FPGA (Field Programmable Gate Array) being its major chip, the user can design and implement his idea in hardware approach as well as in software approach or both on the platform.

B. Sensors

A CMOS camera, a three-axis gyroscope, a tri-axil accelerometer, and an ultra-sonic are the sensors being used for the quad-rotor.

C. Remote control receiving module

The remote control signals received from the PPM (Pulse Position Modulation) module are demodulated and put into the SoPC for control values calculation.

D. Electric Speed Controller

A module transforms control signals from the FPGA into tri-phase signals to control the rotational speed of the motors.

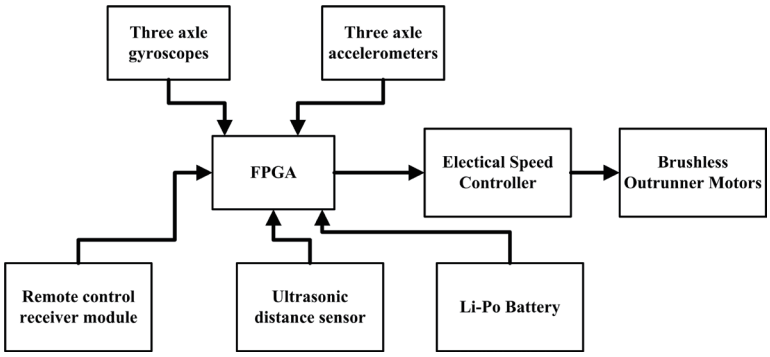

Figure 5. Quad-rotor system

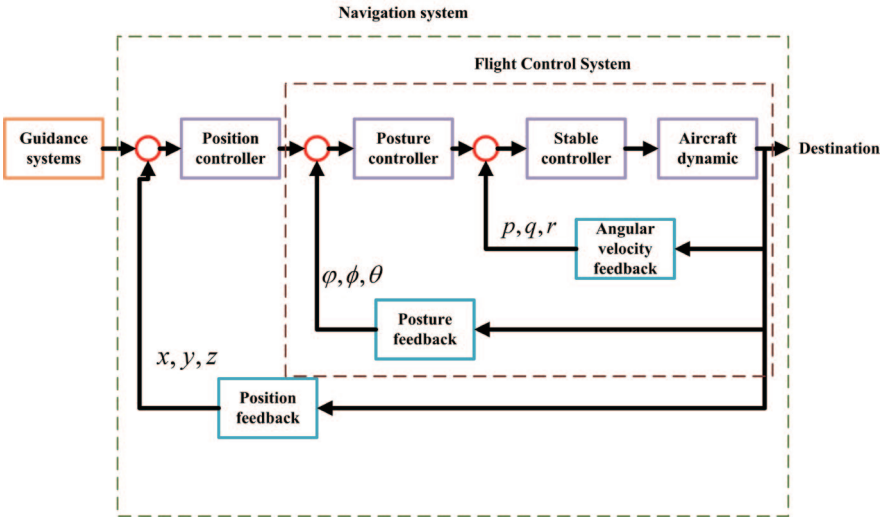

Figure 6. Quad-rotor control system

VI. CONTROL SYSTEM AND SOFTWARE DESIGN

The flight control system, as depicted in Figure 6, is the sour of the quad-rotor. The software design is more complicated than the hardware design for the quad-rotor. Good flight control software makes the quad-rotor flying stably and reliably and being easy to control and tune. The three main control loops are as follows.

A. Angular velocity feedback

The three-axis gyroscope provides the feedback of angular velocities (p, q, and r) to maintain stable flight of the aerial robot and avoid oscillation.

B. Posture feedback

The three rotational angles (θ, ϕ, and ψ) provided by integrating the gyroscope or from the tri-axles accelerometer can be corrected by the flight controller to maintain a stable flight of the quad-rotor.

C. Position feedback

The three-dimensional coordinates (x, y, and z) are getting from image processing unit of the SoPC, (x, y), and ultra-sonic sensor, z, and through the position controller, the position error of the aerial robot can be reduced.

VII. EXPERIMENTS

A. Image processing

In order to detect and track the object on the ground, the system uses a CMOS camera to capture images and performs image processing to find the object location related to the aircraft. Additionally, the system uses an ultra-sonic sensor for measuring the altitude from the ground so the quad-rotor has the coordinate (x, y, z) information about the object of interest from the perspective of the quad-rotor.

Demonstrated in Figure 7 is the image processing experimental result for locating an apron. On the right figure, the coordinate (x, y)

of the midpoint of the blue LED and the red LED is successfully located after the image processing process.

Figure 7. Results of Image processing

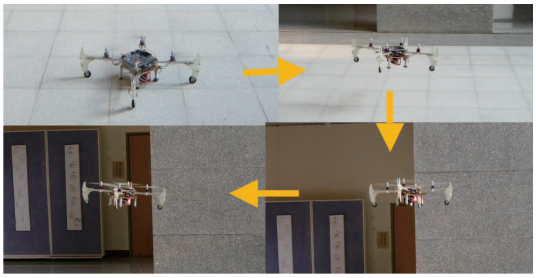

Figure 8. Outdoor flight tests

B. Flying test

The pictures for basic outdoor flying test have been taken and shown in Figure 8. The flying test was performed under the remote control mode and exhibited that the resulting quad-rotor system meets the design goal to some extent.

CONCLUSIONS

A quad-rotor, mounted with a CMOS camera, a three-axil gyroscope, a tri-axle accelerometer, and an ultra-sonic, being capable of performing object detecting and tracking tasks, has been designed and implemented on a SoPC. The critical functions of the aircraft including image processing, feedback of angular velocities (roll, pitch, yaw), PID control, remote control, and hovering, have finished.

However, the resulting system has only met some of the functions of the design goal, i.e. image processing for locating the object of interest, remote control flying. The PID controller of the system exhibits a bit unstable when the vehicle is remotely controlled and causing the automatic flying fails. The problem should be caused by the fact that the three-axil gyroscope is not accurate enough. Hopefully, by replacing the gyroscope with a more accurate one can resolve the control problem and realize the rest of the functions of the deign goal.

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TDTOS – T-shirt Design and Try-On System

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Abstract — In this paper, a new framework for T-shirt design and try-on simulation based on FPGA is presented. Users can not only gain realistic try-on experience, but also design the T-shirts all on their own. The design approach of this system consists of three major parts. First, collect relevant information from the camera and identify the position of the clothes. Second, process the retrieved data and modulate the color of the clothes with folds and shadows remained. Third, place built-in or user-designed pictures onto the clothes and simulate their deformation while the user moves arbitrarily. In comparison with existing virtual clothes fitting systems, our system provides the flexibility of designing customized pictures on the T-shirt with realistic virtual try-on simulation in real-time.

Keywords — virtual clothes try-on, T-shirt design, augmented reality, virtual fitting room, FPGA design

I. INTRODUCTION

In the past, customers could only decide to buy a clothes or not on 2D photos of garments when shopping online. Customers could not know whether the clothes fit them well or whether the clothes look good on them until they get it. This may substantially reduce the willingness of customers to purchase apparel online. Therefore, not being able to feel and try on apparel and accessories items before making a purchase was traditionally regarded as a deterrent to online shopping [1]. However, as some improvements such as free returns and innovative visualization tools have been used, online sales of apparel and accessories have gradually become a success. In recent years, the Internet has emerged as a compelling channel for sale of apparel. Online apparel and accessories sales exceeded $34 billion in 2011, and are expected to reach $73 billion in 2016 [1].

One of the most well-known visualization tools may be virtual try-on systems (or virtual fitting room). Through these systems, customers may have more realistic feel for the details of the garments. Currently, a variety of different kinds of virtual try-on systems is presented, which will be discussed later in Section II. All of them could simulate what we looks like as if we are wearing the clothes to some extent. Nevertheless, they all face the same problem that the results are not real enough. Some systems may not fit clothes on users well, and some may not react to users' motion in real time. In order to solve these problems, we present TDTOS, T-shirt Design and Try-On System.

Different from the existing methods, TDTOS comes up with some brand new ideas. TDTOS not only retrieves users' body information, but also records many useful clothes information,

such as the lightness of the cloth. Through the combination of these data, TDTOS therefore can vividly simulate a real T-shirt with folds, shadows and deformable pictures on it. The virtual try-on results will also response to user's body motion in real-time.

The remaining part of this paper is organized as follow: related work is discussed in Section II. In Section III we present the system architecture. Then, in Section IV, we introduce the core techniques of TDTOS. The results are shown in Section V. Finally, Section VI concludes.

II. RELATED WORKS

In this section, we will discuss some of the recent works and implementation methods on virtual try-on systems (VTS). Zugara[2] first introduced the Webcam Social Shopper, a web cam-based VTS. Using marker detection techniques [3], it detects the marker on a paper to adjust the size and position of the clothes image. JC Penny partnered with Seventeen.com[4] also presented a VTS by attaching the clothes images on a pre-set silhouette on the screen. User can try-on clothes by placing her/himself in the right position. Both of the above two methods require only the camera on a computer to realize a VTS. However, in these cases clothes cannot change its position with user motion. In addition, clothes attached on the screen are 2-D images, so the users cannot fit the clothes in 3-D augmented reality.

Some designs allow virtual clothes to fit on the user when one is moving. Pereira et al. [5] presented a webcam VTS based-on upper body detection. Garcia et al. [6] also proposed a VTS using head detection to fit the clothes. Later version of the Webcam Social Shopper developed by Zugara also adopted head tracking to better place the virtual clothes on the user. Though body tracking techniques enable placing the clothes according to user's position in real time, the lack of 3-D information makes it difficult to create a virtual fitting system with 3-D augmented reality effect. These VTS design can only place a 2-D image on the user's body.

As body modeling techniques keep improving, more virtual try-on systems using robotic modeling or 3-D scanning model are proposed. Fits.me [7] applied the robotic science to create a VTS on the website. Once the user inputs a series of measurements of the body, the try-on results for clothes of different sizes on a robotic mannequin are shown. Instead of creating a real robotic mannequin for virtual try-on, both Styku [8] and Bodymetrics [9] adopt 3-D body scanning techniques using Microsoft Kinect or Asus' Xtion. The scanner creates a 3D virtual model of the user and allows one to analyse the fitness of the try-on clothes results through a color map. Using sophisticated robotic models or accurately measured scanning models produces realistic try-on results. As a trade-off of the accuracy, those systems cannot present try-on results with body motions in real-time.

With a depth and motion capture device, such as Microsoft Kinect or Asus' Xtion, virtual try-on systems that enable real-time clothes fitting can be designed more easily. In addition, various computer graphic algorithms for clothes modeling have been proposed in the past [10]-[15]. Coming both the motion sensing and garment modeling techniques, Swivel [16], AR-Door [17], Fitnect [18], and Fitting Reality [19] all presented their different implementations of VTS. Pachoulakis et al. reviewed some of the recent examples of virtual fitting room and their implementation concepts in [20]. Those try-on systems first capture the user's body motion and then superimposed 3-D clothes models on the user's image. For this reason, although the systems enable virtual try-on in real-time, sometimes the virtual clothes images may not

precisely fit the user. Besides, the only clothes that a user can try-on are limited to the garment model database. It is difficult for a user without computer graphic experience to design one's own wearing clothes.

In this paper, without using a depth and motion capture device, we utilize DE2-70 FPGA board and its camera module, combining both image processing and FPGA hardware implementation techniques to design TDTOS. This system enables real-time virtual try-on with all the folds and shadows on the shirt vividly preserved. Instead of superimposing garment models on the user image, TDTOS precisely modulate the user's clothes image to present the effect of virtual try-on. In addition, user can easily design pictures to put on the shirt by one's own drawing. The picture can also move and deform as the T-shirt is pulled or folded. TDTOS is a new solution for realistic virtual try-on and T-shirt design in real-time.

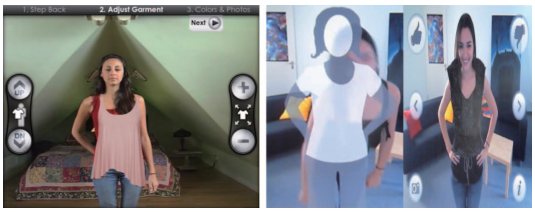

Figure 1. Left: Zugara Webcam Social Shopper. Right: Seventeen.com virtual fitting room.

Figure 2. Fits.me uses robotic models to simulate virtual try-on

Figure 3. Styku body scanning technique and fitness color map

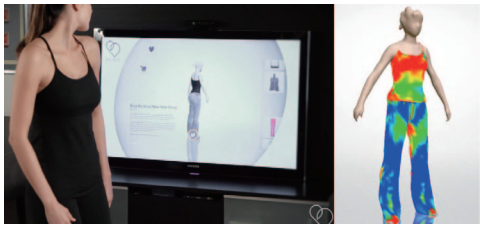

Figure 4. Bodymetrics scanning system and fitness color map

Figure 5. Virtual try-on systems using motion sensing devices. Top Left: Swivel virtual dressing room. Top Right: AR-Door Kinect fitting room. Down Left: Microsoft Fitnect. Down Right: Fitting Reality's VIPodium

III. SYSTEM ARCHITECTURE

In this section, we are going to introduce the design architecture of our system. Figure 6 is the data flow diagram, which provides a simple view of how our system functions. Figure 7 is the system block diagram, in which the relationships between

modules are shown. These modules can be roughly classified into four parts: Image Retrieval, Memory Control, Image Processing and Detection, and Input/output Interface. A brief introduction of each part is as follow:

A. Image Retrieving

A 5-Mega Pixel Camera is used to capture images. Together with modules CCD Capture and RawtoRGB, we could get the RGB values of all pixels, which will be the data of the following process.

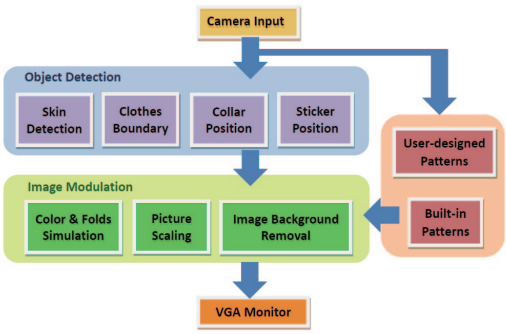

Figure 6. Data flow diagram

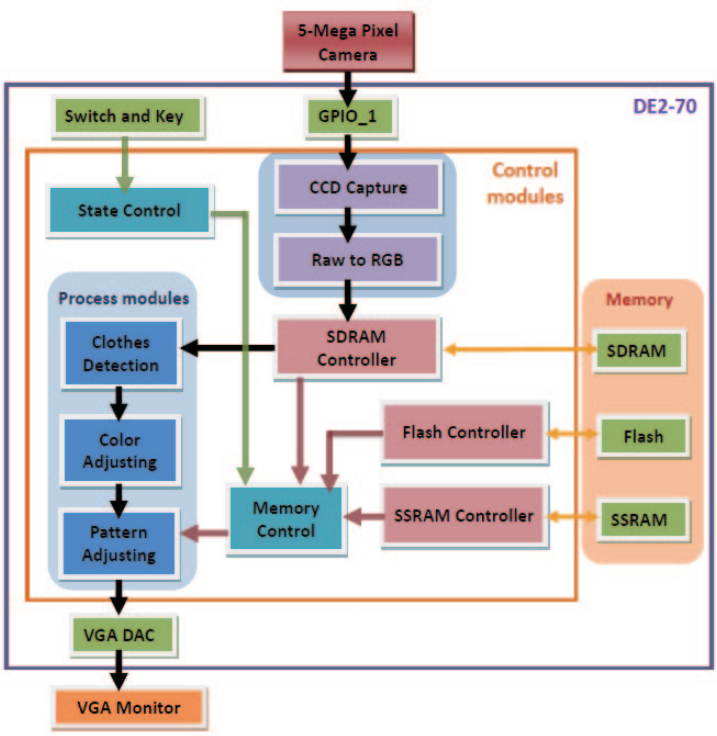

Figure 7. System block diagram

B. Memory Control

The retrieved images mentioned above are temporarily saved in SDRAM, and the built-in pictures are saved in FLASH memory. In order to achieve real-time processing results on VGA output, SSRAM is used as the buffer memory for data to be processed. Both the built-in pictures and the user-designed pictures will be buffered in SSRAM before processing.

C. Image Processing and Detection

This part can be view as three steps. First, Clothes Detection uses skin color to filter out the skin part and identify the boundary of the clothes. Second, after knowing the region of the clothes, Color Adjusting changes the clothes' color with folds and shadows retained. Third, Pattern Adjusting analyzes the customer's motion and adjusts the picture's looks with proper deformation in real-time.

D. Input / Output Interface

Using switches and keys on the DE2-70 FPGA board, users can control the systems with desired command. The final try-on simulation results will be output through VGA controller to the monitor.

IV. TECHNIQUES

A. Key Concept

For the existing wearing try-on simulation systems, one of the major problems is that how to make the clothes moves, rotates, and even folds according to our body motions. The traditional way is to modify an existing target clothes image and superimpose it onto the image of the users, such as how Fitnect and VIPodium do. The outline of the target clothes usually does not match the outline of the user body. Even if the image is scaled to the size of the body, there are still many positions that the outlines do not coincide and the clothes seem weird on the users. What's more, the folds and shadows have to be created according to the body motions, which is extremely difficult and requires lots of computation. The clothes eventually seem unreal because the shapes are mismatched and the folds and shadows are disappeared.

However, we do not need to create the folds and shadows actually. The folds and shadows already exist on the original T-shirt that the users are wearing. Besides, the outline of the original T-shirt is also perfectly matching the body of the users. Therefore, our key concept is that, instead of modifying the target T-shirt to fit the body motions, we combine the folds and shadows information from the original T-shirt with the color and pattern of the target T-shirt to simulate a real T-shirt vividly. As a result, the new T-shirt on the user is perfectly matching and folding according to the body motions.

Figure 8. Key concept for TDTOS's design

B. Skin Detection

To identify the original T-shirt on the users, skin detection is required to filter out the skin part. According to the research of Basilio et al. [21], the color of skin is more explicit in YCbCr color space. Therefore, we transform the color of each pixel to YCbCr color space and determine whether it is skin by the following conditions.

$$\begin{cases} Y > 50 \\ Cb < 120 \; or \; Cb > 150 \\ Cr < 200 \end{cases}$$
$$\text{where } Y, Cb, Cr = [0,255].$$

The thresholds are slightly modified because of the different races. The conditions are designed to work well on the Asians. In Figure 9, the left image is taken from a user and the skin part is detected and colored red in right figure.

Figure 9. Skin detection result. The Skin part is detected red in the right figure.

```
Procedure IdentifyShirtRegion
Input: a Boolean array indicating whether each pixel in a line is clothes' color
Output: Left, Right, two indexes indicating the T-shirt region

sum = 0; max_sum = 0; start = 0; end = 0; Left = 0; Right = 0;
For each pixel in the line from left to right
        If the pixel is clothes' color Then sum += 5
        Else
                If sum> 1 Then sum -= 2
                Else sum = 0
                End-if
        End-if

        If sum == 0 Then
                start = index of the current pixel
        End-if
        end = index of the current pixel
        If sum > max_sum Then
                Left    = start
                Right   = end
                max_sum = sum
        End-if
End-for
Return Left, Right
```

Figure 10. The clothes identification maximum sub-array algorithm.

C. Clothes Positioning

After the skin is detected, the region of the T-shirt could be identified as well. The image is scanned row by row from top to bottom. For each line, after filtering out the background and the skin part, the remaining part is treated as the T-shirt. However, in order to tolerate the inevitable noises and skin on the T-shirt, we apply the maximum sub-array algorithm. Therefore the outline of the T-shirt could be precisely determined even if there is some noise or false detection of skin on the T-shirt. The pseudo code of the maximum sub-array algorithm is shown as Figure 10.

D. Folds and Color Changing

After identifying the region of the T-shirt successfully, we could modify the color according to the target color. As mentioned before, the original color is not simply replaced by the target color. On the contrary, the target color is mixed with the original one by the following formula. The new RGB values of each pixel are calculated by the formula, which considers both the brightness of the shirt image and the target color. Therefore, not only the T-shirt turns out in a new color, the original folds and shadows are also shown as well.

$$New_X = Target_X \times \frac{(Orig_R + Orig_G + Orig_B)/3}{1024},\ X = \{R, G, B\}$$

E. Picture Selection

We provide two ways to choose a pattern of the target T-shirt. The first method is choosing from our built-in pictures. Each picture is 500 pixels in height and width, and is 0.5 MB in total. Therefore an 8MB Flash memory could store 16 pictures. In addition, since built-in pictures are stored in the Flash, reading data from flash has delay problems. Therefore we use the SSRAM as a buffer. After copying the data in Flash to SSRAM once, we could use SSRAM instead of flash to achieve real time performance.

The second way is to use a user-designed picture. One could arbitrary draw its own T-shirt picture in his/her own way, and then use our camera to take a picture of the drawing. After taking the photo, the image will be processed. First, the white background will be removed so that when changing T-shirt color, the image will

not have the white background. Second, we apply a series of complex memory manipulation on SSRAM, sharing the buffer memory resources with both flash and SDRAM, so that the users could still switch between built-in pictures and user-designed picture easily. Finally, the user could put the user-designed picture on the T-shirt.

F. Picture Placement

After choosing a picture, one could place the picture by two ways as well. The first method is using collar detection and hand gestures. In this mode, the picture would be place under the collar by default. We could detect the position of the collar by maximum sub-array algorithm as before. If the skin part is less than 100 pixels and the clothes width is larger than 800 pixels, the center of skin line would be identified as the position of collar. One could also set the position of the picture by gestures. When pointing down with hands, the position of fingers can be detected by a similar method of collar detection. The system will remember the displacement between the position specified by gestures and the collar, so the picture could be placed to the desired place afterward.

In the second method, users could not only move the picture, but also scale the picture to any size simply by 3M stickers. The positions of the stickers could be detected by maximum sub-array algorithm as described before. The top left red stickers specifies the position of the top left corner of the picture, and the right green sticker and bottom red sticker specify the right and bottom edge of the picture. The picture is scaled both in width and height accordingly. To overcome the delay of calculation, we use pipelines to maintain real time performance.

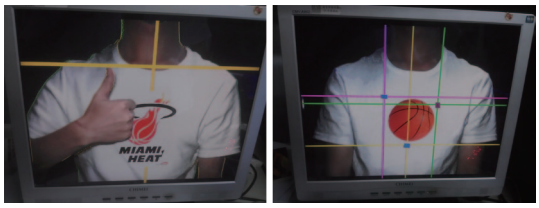

Figure 11. Two ways to place built-in or user designed picture on the T-shirt. Left: Picture placed by collar detection and adjusted by user gesture. Right: Picture placed by sticker detection with deformation simulation

V. RESULTS

A. Color Changing

The color of the T-shirt could be changed to arbitrary color by users. In the demo pictures, Figure 12, we showed how it is changed to the primary colors and their combinations. The simulated T-shirt has the folds and shadows as well. In addition, both hands can move freely in front of the T-shirt and do not affect the coloring effect at all. In Figure 13, it is shown that even when the user turns back, the T-shirt is colored as well.

Figure 12. The original white T-shirt and transformation of different colors.

Figure 13. The back of the user is fully colored.

B. T-shirt Pictures

After color changing, we can choose the picture to put on the T-shirt from built-in pictures and user designed pictures.

1) **Built-on Pictures:** The system provides up to 16 built-in pictures for users to place on to the T-shirt. The pictures are automatically placed on the chest of the users. The following figures show two example pictures. Please note that even the hands are in front of the T-shirts, the pictures are not affected just like a real T-shirts.

Figure 14. Try-on results with built-in pictures

2) **User-designed Pictures:** Users could draw their own pictures and easily put them onto the T-shirts. This feature allows anyone to design its own T-shirt and try it on immediately. By using our system's camera to take a photo of the picture, the picture is saved by the system and placed on the chest by default. The following figure shows one of the designed T-shirt on our own.

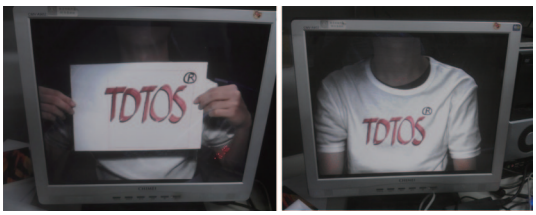

Figure 15. Left: Draw a picture and take a photo by the camera. Right: The user-designed picture is then on the T-shirt.

C. Picture placement

The picture is placed on the chest by default. However, it is convenient to move the picture to the desired position. We provide two ways to move the picture: Using gestures and using stickers.

1) **Placement by Gestures:** This is the simpler way to move the position of the picture. By pointing down the target position, the system will detect and memorize the desired position. After the gesture adjustment, the picture could be placed to the any desired position at any time.

Figure 16. The picture is moved along with the hand gesture.

2) **Placement by Stickers:** In this method, the picture position could be conveniently indicated by three 3M stickers. The picture will be scaled and placed in the sticker-specified area. Therefore, it is easy to shrink or enlarge the picture as well, which makes the design of T-shirts more conveniently. In addition, because that the picture is placed in the stickers, it could moves, shrinks, expands, deforms or even rotates with the body motions of the users. All the folds and shadows in the region of the picture will also retain as the picture deforms, which makes the try-on results highly realistic.

Figure 17. Using stickers to indicate the position and size of the picture

Figure 18. Left: The picture deform with folds and shadows retained. Right: The picture rotate as the user is rotating one's body

CONCLUSIONS

In this paper, we presented TDTOS, a new framework for T-shirt design and try-on simulation based on FPGA implementation. Instead of modifying the existing clothes models to fit the body motions, we utilize the information from the original T-shirt image to simulate the virtual try-on results realistically. The color of the T-shirt could be changed arbitrarily with all the folds and shadows retained. Built-in pictures or user-designed pictures could be placed on the T-shirt by hand gestures or 3M stickers. When we use stickers to locate the picture, all the folds and shadows on the picture will also retained as the picture deforms with user's body motion. Combining the new design concepts with implementation techniques, TDTOS provides the flexibility of designing customized pictures on the T-shirt with highly realistic virtual try-on simulation in real-time.

ACKNOWLEDGMENT

We would like to express our gratitude to Altera® Inc. and Terasic® Inc. for their sponsor and support for our project in the Innovate Asia Altera Design Contest 2012. Moreover, we also wish to acknowledge Professor Shao-Yi Chien and Department of Electrical Engineering, National Taiwan University for the excellent training and providing us with the chance to fulfill this project.

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