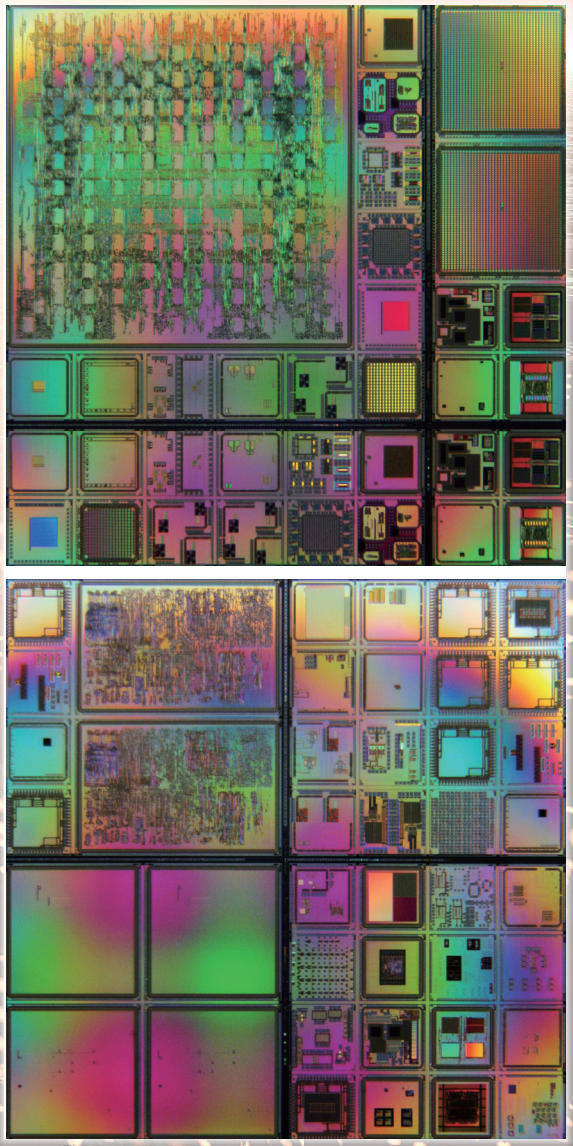
VDEC

平成27年度

東京大学
大規模集積システム設計教育研究センター

年 報

2015
VLSI Design and Education Center, The University of Tokyo Annual Report



VLSI Design and Education Center The University of Tokyo 2015

VLSI Design and Education Center
The University of Tokyo

This is the 2014 Annual Report of VDEC (VLSI Design and Education Center, University of Tokyo).

In 2014 we introduced a high-density assembling system as a tool for enhancing added-value of integrated circuits. Taking into account rapid increase of VDEC cleanroom users, the system consists of a flip-chip bonding and its peripheral apparatuses to implement a high-density chip assembly. High-density boards/chip-carriers, to which bare chips are attached, can be fabricated using the electron beam lithography that is already introduced in the cleanroom. Using the new system we are expecting to efficiently integrate bare chips with other devices for demonstrating highly value-added systems, such like sensor systems, integrated MEMS, Ultra-high frequency systems and so on.

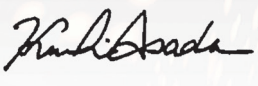
Under the circumstance of hard access to new technologies beyond 40 nm CMOS in Japan, we carried out a test run for 28 nm FDSOI/CMOS technology of ST Microelectronics two years ago, collaborating with CMP. It was successfully finished last year, thanks to a lot of cooperation of VDEC major users. We have already made a new menu of the 28 nm FDSOI/CMOS open for all the VDEC users. Because its price per chip area is, however, considerably high, we received many requests from committee members of the VDEC council for chip fabrication menus with moderate prices between 40 nm and 90 nm. So, we have been discussing in VDEC about a possibility of new foundries for these requests, including oversea companies. Fortunately, it was found that the 65 nm CMOS/SOTB, developed by the national project, LEAP (Low-power Electronics Association and Project), will be available via Renesas Electronics even after the end of the project. We have already included it in the chip fabrication menu of VDEC from this year. Though we have to pay attention to the regulation of VDEC academic CAD licenses, the new technology is open for commercial use and oversea countries, as well. We are expecting that it will be used for seamless research and development from academia to industry. We are also recognizing importance of introducing commercial CAD licenses for direct transfer of research results from academia to industry. Though we have been discussing and negotiating on this matter with persons concerned, it will still take a time before providing them from VDEC. Now, new commercial services, such like the cloud CAD tools, are about starting, along with the second/third CAD vendor tools, almost compatible with the mainstream of CAD tools with reasonable prices. It would be important for academia to establish LSI design environments based on these new comers.

As the annual event of the D2T (Design-to-Test) research division, donated by Advantest Corporation, the 9th symposium was successfully held on August 26th 2014, inviting distinguished lecturers from oversea and domestic institutes. We are scheduling the 10th symposium in August 21st this year, too. The main subject of the 10th symposium will be “Reliability for automotive and other applications.” We would like to express our sincere thanks to invited lecturers, audiences and Advantest Corporation for the continuous support.

We will continue to do our best efforts for the original mission of VDEC, “promotion of education and research in LSI design by means of practical chip-design and implementations”, in order to realize research and education for enhancing the value of the semiconductor technology. We thank you for your continuous supports again.

June 2015

VLSI Design and Education Center, University of Tokyo
Director Kunihiro Asada



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Annual Report 2015

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Chapter 1 Activity Report of VDEC

1. 1 Introduction of VDEC activities and activity report of FY2014

VLSI Design and Education Center(VDEC), University of Tokyo was established in May 1996. VDEC has been operating for the following 3 major roles: "spreading the latest information on VLSI design and education," "providing licenses of CAD tools," and "supporting on VLSI chip fabrications for academic use." The VDEC activity report of FY 2014 is described hereafter according to Fig. 1. 1.

The missions of VDEC are for advancement of researches and education on LSI design in public and private universities and colleges in Japan and send many distinguished VLSI designers into industry. After 18 years of VDEC establishment, educations on CAD software, LSI design and design flow in universities have been well established. On the other hand, advancement on nano-meter CMOS technologies forces design flow and CAD software complicated. We have been continuing CAD tool seminar by the lecturers from EDA vendors for twice a year. We hold the seminar in VDEC and provide distance learning through video streaming. We expect spread of the up-to-date LSI design methodology by using CAD tools.

We assume our LSI design flow seminars as educations on basic LSI design concepts and practical experience of LSI design with CAD tool chain. VDEC holds "LSI design education seminar", a.k.a. VDEC Refresh Seminar, once a year. This year we shifted these seminars from November-January time frame to May-July time frame. We also added "Digital design course" in addition to three courses "Analog design course" and "RF design course", and initiated "MEMS design course". We invite experienced professors among universities as lecturers for the courses to conduct LSI design education courses with practical experience. We also hold "Transistor level design flow in VDEC" and "Digital design flow in VDEC EDA environment" for designers in universities. We

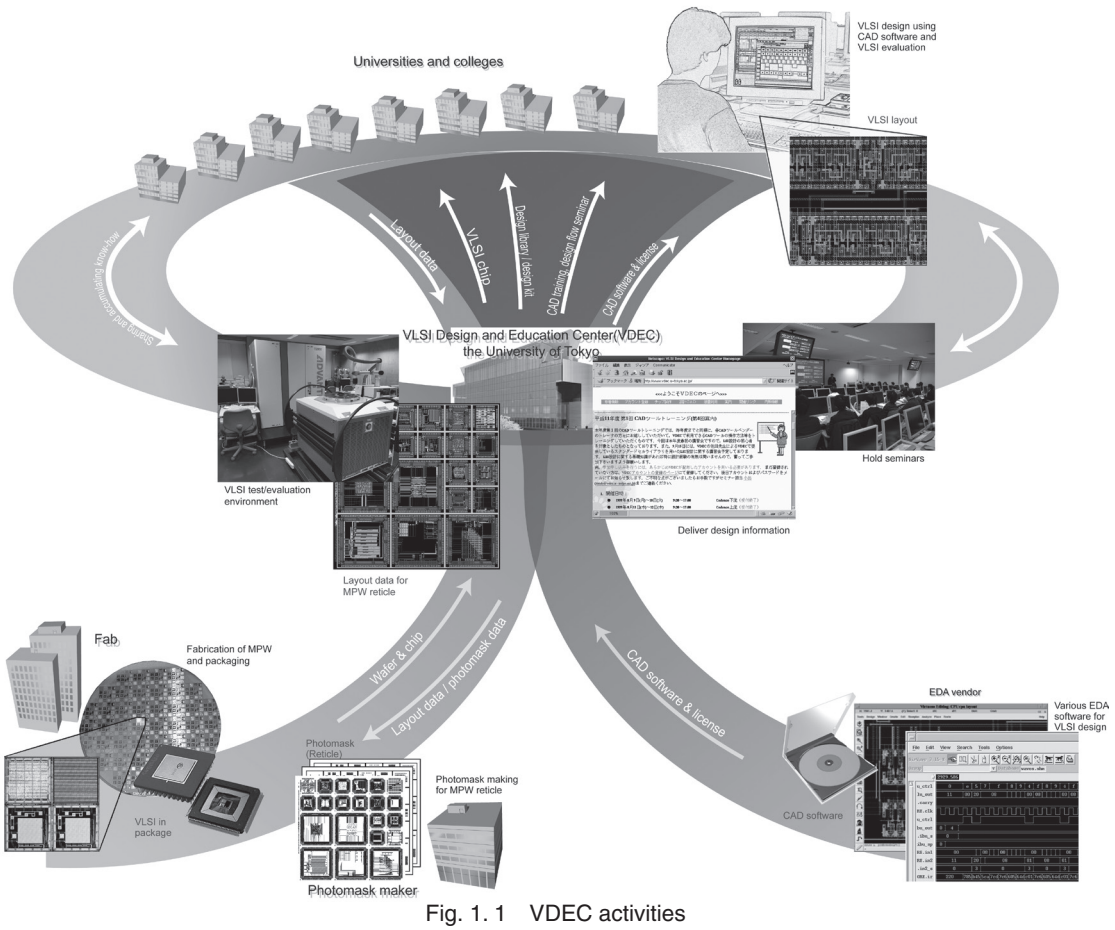


Fig. 1. 1 VDEC activities

started to charge these two LSI design education courses, as well as VDEC Refresh Seminars.

In addition to the above seminars, we hold "VDEC Designer'Forum" among young professors and students annually. This is a workshop that the participants exchange their design examples with not only success stories but also their failure stories, in addition to invited talks. We expect students and professors who will start designs to learn kinds of know-hows. We have initiated "IEEE SSCS Japan Chapter VDEC Design Award" this year, and final examination and awarding have carried out during the "VDEC Designer'Forum". Mr. T. Kawamura(Nara Advanced Institute of Science and Technology (NAIST)) is awarded as "IEEE SSCS Japan Chapter VDEC Design Award" winner, and Mr. C. Monteiro(Gifu Univ.), Mr. T. Yamaguchi(NAIST), Mr. H. Hayami(NAIST), and Mr. T. Usui(Shizuoka Univ.) are awarded as "the best VDEC Design Award", and Dr. S. Wang(Kyushu Inst. of Tech.), Mr. F. Mochizuki(Shizuoka Univ.), S. Yamasaki(Hiroshima Univ.), Ms. A. Oshima(Kyoto Inst. of Tech.), Mr. S. Kanda(Kyoto Inst. of Tech), and Mr. S. Uenohara(Kyushu Inst. of Tech) are awarded as the "VDEC Design Award."

LSI designers come up against various difficulties during actual LSI design scene, even after the basic educations through various seminars and the forum. One of the biggest problems for beginners is the setup of CAD softwares. Many of them also get confused by "Esoteric messages" come out from CAD softwares, even after they successfully setup CAD tools. In such situations, VDEC mailing-lists make significant contributions. VDEC users can register to VDEC mailing-lists on CAD tools, and process dependent groups through VDEC web pages, and can ask questions and helps on their facing issues. It is not a responsibility for the registrant of such mailing-lists to give answers to questions, however, in most cases, replies are given by the experienced users of CAD tools and experienced designers within a couple of hours to a couple of days. Moreover, emails are accumulated and are open to the VDEC users, as shown in Fig. 1. 2, who have registered VDEC accounts, as the important educational assets. We expect all the VDEC users to make the full use of this mechanism to help solve problems.

We continue chip fabrication services on 0.18mm CMOS by Rohm and 0.8 μm CMOS by On-semi Sanyo Semiconductor. And started chip fabrication services on FDSOI CMOS 28 nm by ST Microelectronics in cooperation with CMP.

Our donated division "Design To Test(D2T)", which was founded by donation from Advantest in Oct. 2008, focuses on enrichment of education on LSI testing and bridging between design and testing.

Fig. 1. 4 shows trends of number of papers through VDEC activities. Number of papers is increasing, which means researches in the field of VLSI design have been encouraged after VDEC establishment.

Fig. 1. 5 shows number of papers related to CAD usage, chip fabrications and VDEC facility usages. CAD tools are widely used to write papers. CAD tools are used not only chip designs themselves but also used for preparation of chip fabrication and they contribute to verify fundamental ideas of researches. Advanced CMOS processes are preferred for publications, and not only papers with 65 nm CMOS chips, but also with 45nmCMOS, 32nmCMOS

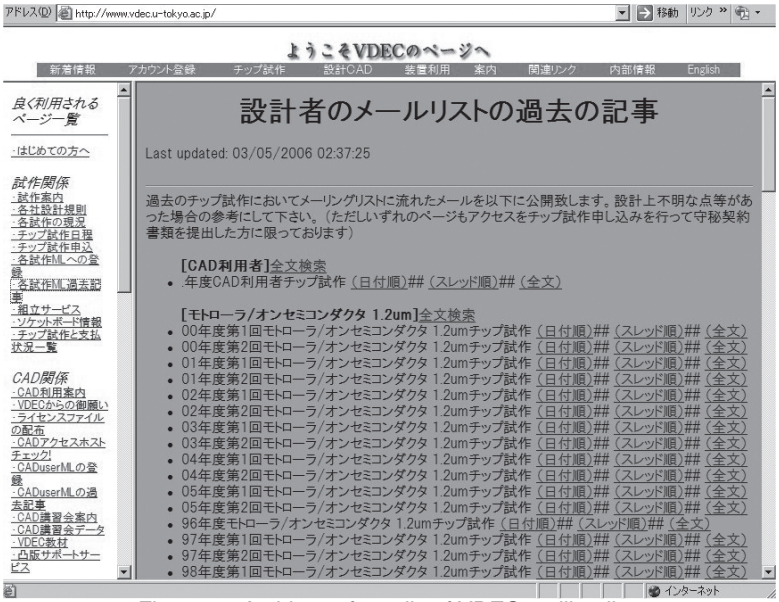


Fig. 1. 2 Archives of emails of VDEC mailing-list.

and 22nmCMOS are emerging in the world. We would like to prepare chip fabrication services for the advanced CMOS processes. In addition, we would like to setup chip fabrication services related to CMOS/MEMS to fulfill the researches for “More than Moore”. We also encourage researchers to fully use of VDEC facilities such like LSI testers, FIB systems and EB writer for the wide spread of research purposes.

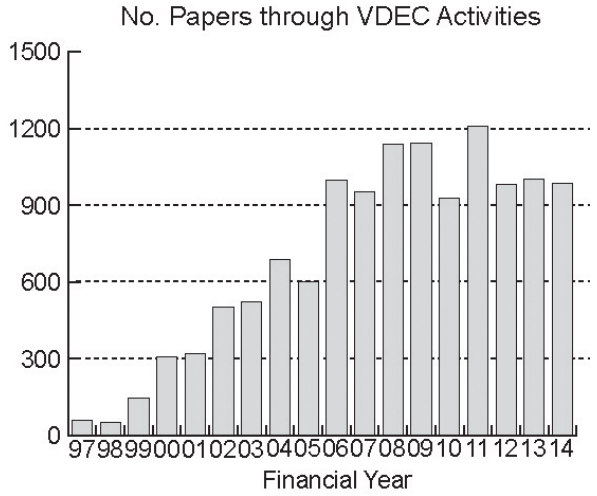


Fig. 1. 3 Trends of number of papers through VDEC activities.

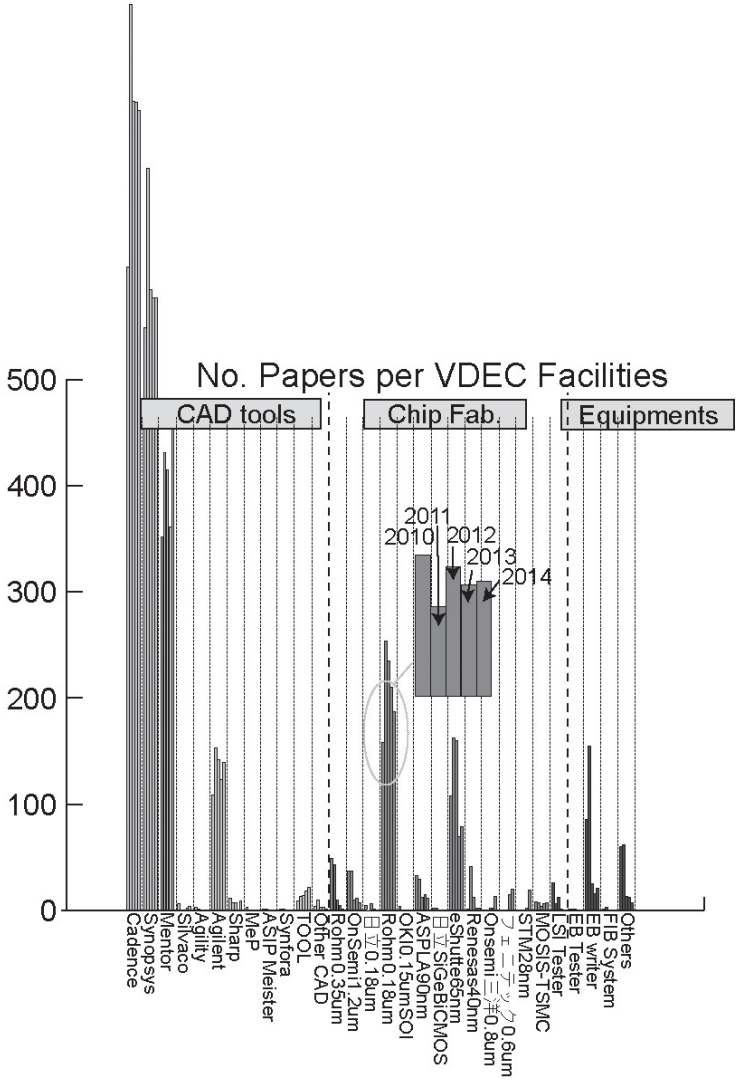


Fig. 1. 4 Number of papers related to VDEC facilities.

1. 2 VDEC CAD Tools

Since 1996, VDEC has provided CAD software licenses to the registered researchers in universities and colleges in Japan. The CAD tools we provided in 2009 are shown in Table 1. 2. 1. The researchers can use those CAD tools when their local machines, whose IP addresses are registered in advance, are authorized by one of VDEC license server located in the ten VDEC subcenters shown in Fig. 1. 2. 1. For each CAD tool, VDEC provides 10-100 floating licenses. Those CAD tools can be utilized only for research and education activities in national universities, other public universities, private universities, and colleges.

When one is going to use VDEC CAD tools and chip fabrication service (the details are described in Section 1-3), some faculty member of his/her research group in a university or a collage needs to do user registration. Fig. 1. 2. 2 shows (a) the number of registrants, (b) the number of distinguished universities/colleges of the registrants, and (c) the number of registrants who applied VDEC CAD tools.

Table 1. 2. 1 VDEC CAD tools

Name	Function	Vendor
Cadence tool set	Verilog-HDL/VHDL entry, Simulation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Interactive schematic and layout editor, Analog circuit simulation, Logic verification, Circuit extraction	Cadence Design Systems, Inc.
Synopsys tool set	Verilog-HDL/VHDK simulation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Circuit simulation, Device simulation	Synopsys, Inc.
Mentor tool set	Layout verification, Design rule check	Mentor Graphics Co. Ltd.
Silvaco tool set	Fast circuit simulation	Silvaco
ADS/Golden Gate	Design and verification of high-frequency circuits	Agilent Technologies
Bach system	BachC-based design, synthesis, and verification	Sharp
LAVIS	Layout visualization platform	TOOL
Laker, Verdi	Layout editor and debugger	Springsoft Inc.

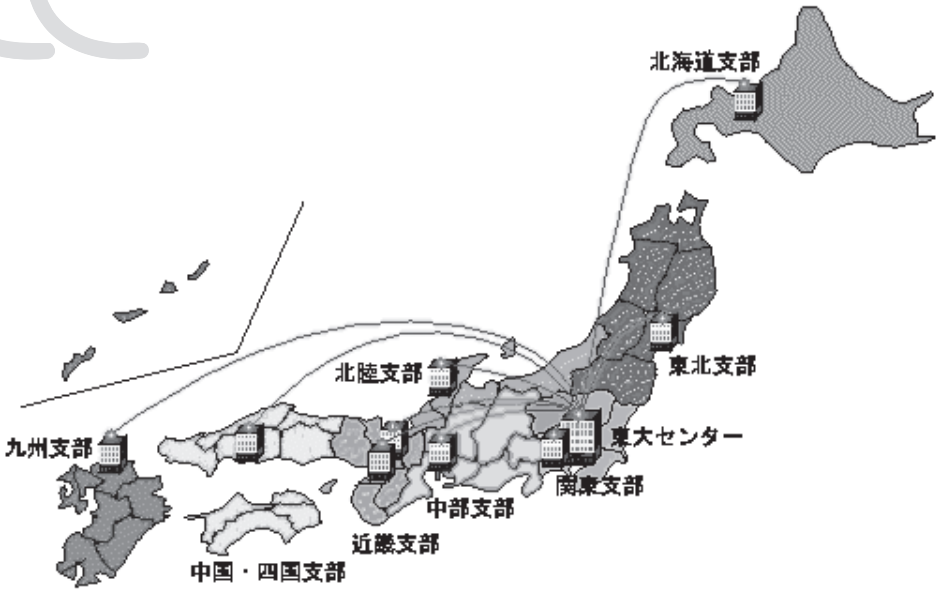
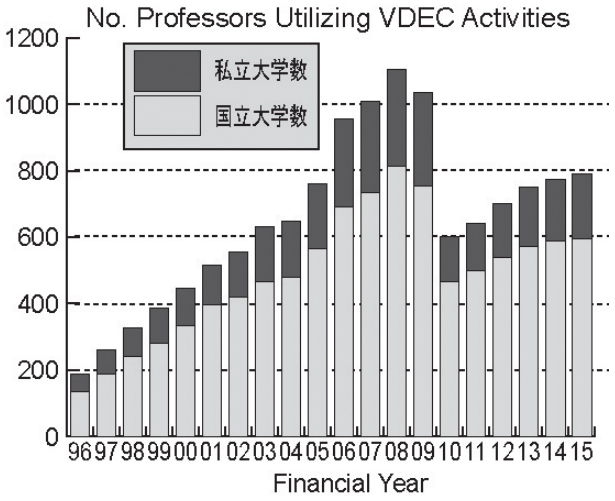
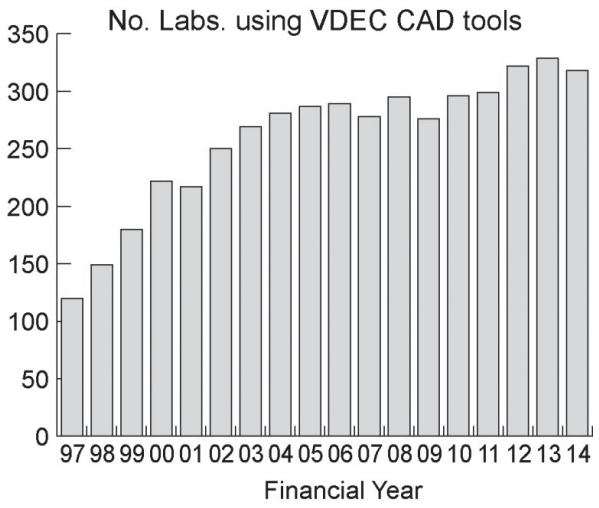


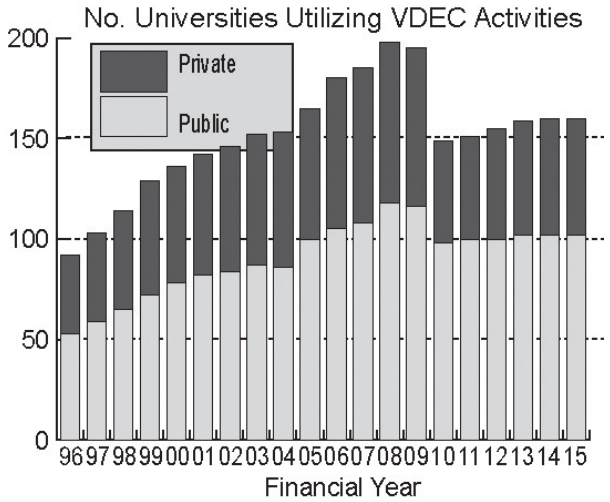
Fig. 1. 2. 1 VDEC Subcenters



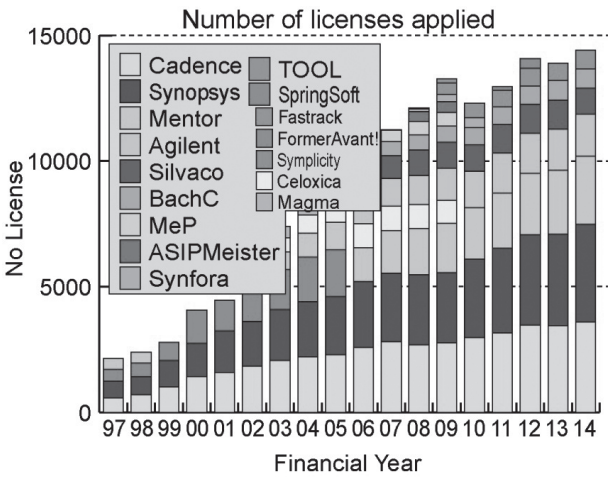
(a) The number of registrants



(c) The number of research group applied CAD tools



(b) The number of universities colleges of the registrants



(d) The number of applied licenses of all CAD tools

Fig. 1. 2. 2 The numbers of VDEC CAD Applications

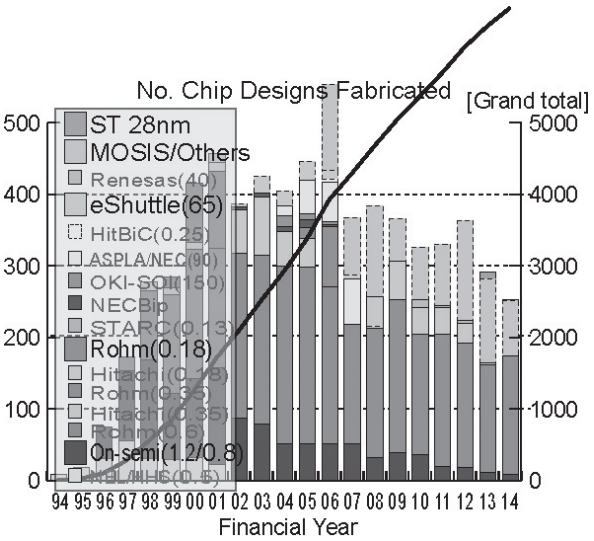
1. 3 VLSI Chip Fabrication

1. 3. 1 Trends of VLSI Chip Fabrication Services

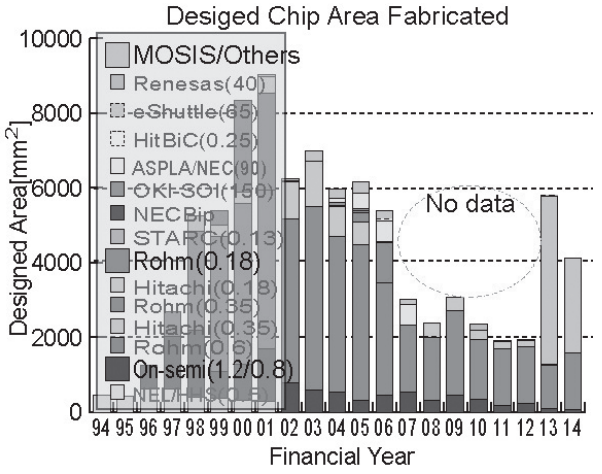
Fig. 1. 3. 1 shows a trend of number of designed chips for VDEC chip fabrication services, including pilot project prior to VDEC establishment.

VLSI chip fabrication is limited to 0.5 μm CMOS provided by NTT Electronics during the pilot project in 1994 and 1995. VDEC chip fabrication had started in 1996 with 1.2 μm CMOS provided by Motorola Japan, which is now On-Semiconductor as well as the 0.5 μm CMOS. In 1997, VDEC received cooperation from Rohm and has started 0.6 μm CMOS process. In 1998, VDEC started chip fabrication services of 0.35 μm CMOS by Hitachi, and in 1999, VDEC started 0.35 μm CMOS by Rohm. We had a test chip fabrication of 0.13 μm CMOS by STARC through "IP development project" in 2001. We added 0.18 μm CMOS by Hitachi into our chip fabrication menu in 2001. From 2002, we started VDEC-MOSIS chip fabrication program initiated by Prof. Iwata of Hiroshima University. Under this program, VDEC member can access to TSMC and IBM processes with lower price. We also started Bipolar chip fabrication by NEC Compound Semiconductor Devices. In 2004, we started 0.15 μm SOI-CMOS chip fabrication by Oki Electric as test chip fabrications. In the same year we started 90 nm CMOS chip fabrication by ASPLA/STARC. In 2006, we started 0.18 μm CMOS by Rohm and 0.25 μm SiGeBiCMOS by Hitachi. In 2008, we started 65 nm CMOS process by eShuttle, after closure of 90 nm CMOS chip fabrication in 2007. In 2010, we started 40 nm CMOS process by Renesas Electronics through "Next Generation Semiconductor Circuits & Architecture" project between METI and STAR. On the other hand, 1.2 μm CMOS chip fabrication program came to end by the September 2011. 40 nm CMOS by Renesas Electronics and 65 nm by eShuttle also come to end by Oct. 2012 and Aug. 2013, respectively. We started CMOS 0.8 μm in Oct. 2012 by On-semiconductor-Sanyo as a test chip fabrication and opened it as the regular chip fabrication menu in 2012. We started FD-SOI 28 nm CMOS by ST-Microelectronics through CMP, France, as the advanced CMOS process in 2013.

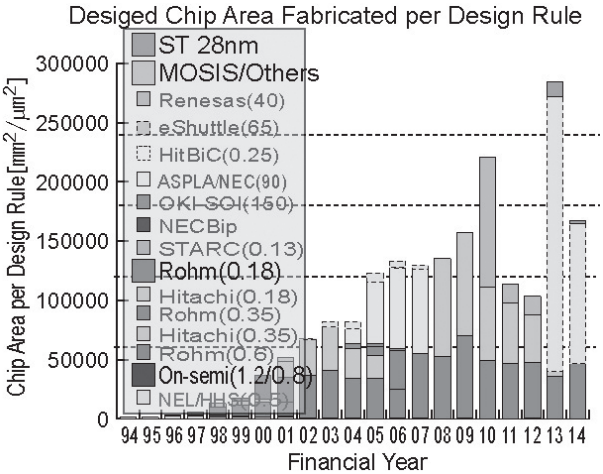
Fig. 1. 3. 1(a) shows trends of number of chip designed for VDEC chip fabrication. For the first 6 years until 2001, the number of designed chips shows steady increase, which means drastic improve of the effectiveness researches and education of LSI design, and we assume drastic increase of number of students related to LSI chip



(a) Trend of number of designs fabricated.



(b) Trend of designed area.



(c) Trend of designed area normalized by design rule.

Fig. 1. 3. 1 Trend of number of designs and designed chip area.

design and education. During few years of stable number around 400 chip designs per year, we can see transition of designs toward finer process. In 2007, we saw a large drop, which was caused by sudden process transition from 0.35 μm CMOS to 0.18 μm CMOS, and in 2008, we also saw another drop by process transition from 90 nm CMOS to 65 nm CMOS.

Fig. 1. 3. 1(b) shows trends of designed chip area, which shows much clear trends of drop by process migration. On the other hand, Fig. 1. 3. 1(c) shows trends of designed chip area normalized by design rule, which assume to be strong relation with design efforts. Coming from the fact that the normalized chip area is still growing, we assume the major reason for decrease of number of chips and designed area is increase of design effort per chip and per unit area due to process scaling.

Fig. 1. 3. 2 shows trends number of professors and universities fabricated chip. Number of professors who have contracted NDA for process technologies to access design rules and design libraries are, 262, and 32, respectively, for 0.18 μm CMOS, and 0.8 um CMOS.

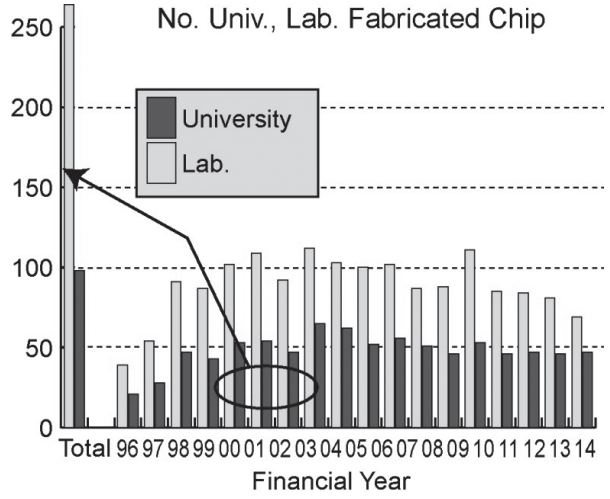


Fig. 1. 3. 2 Trend of number of processors and universities fabricated chip.

1. 3. 2 Overview of chip fabrication in 2014

Table 1. 3. 1 lists chip fabrication schedule in 2014. Please refer to list in Chapter 2 for details of designers and contents of chip designed.

Table 1. 3. 1 Chip fabrication schedule in 2014

○ 0.8 μm CMOS (On-Semiconductor - Sanyo)

	Chip application deadline	Design deadline	Chip delivery
2014 #1	2014/ 7/14	2014/10/ 6	2014/12/18
2014 #2	2014/12/29	2015/ 3/23	2015/6(Schedule)

○ 0.18 μm CMOS (Rohm)

	Chip application deadline	Design deadline	Chip delivery
2013 #5	2013/11/ 4	2014/ 1/27	2014/ 5/14
2014 #1	2014/ 1/27	2014/ 4/21	2014/ 8/ 5
2014 #2	2014/ 4/14	2014/ 7/ 7	2014/10/21
2014 #3	2014/ 6/ 9	2014/ 9/ 1	2014/ 1/28
2014 #4	2014/ 8/25	2014/11/17	2014/ 3/12
2014 #5	2014/11/ 3	2015/ 1/26	2015/5(Schedule)

○ 28 nm CMOS (STMicro/CMP)

	Chip application deadline	Design deadline	Chip delivery
2015 Jan.		2015/ 1/ 5	

1. 3. 3 Libraries and design flows

VDEC have been working to prepare design libraries and design flows for digital design and PDKs for analog design. Table 1. 3. 2 lists libraries available now.

Table 1. 3. 2 Libraries available for VDEC chip fabrication

Technology	Name	Author	Contents
0.18 μm CMOS (Rohm)	Rohm library	Rohm Library Std. Cells, IO cells, RAM (Distributed with CDROM)	Synthesis(Synopsys)
			Simulation(VerilogXL)
			P&R(LEF/DEF)
	Kyodai Library	Onodera Lab., Kyoto University	Synthesis(Synopsys)
			Simulation(VerilogXL)
			P&R(Astro)
	Todai Library	VDEC Design flow based on library prepared by Onodera Lab., Kyoto University	Synthesis(RTL Compiler)
			Simulation(VerilogXL)
			P&R(Encounter)
	PDK	VDEC	PDK(IC6.1)

1.4 Seminar

Seminar is indispensable for the improvement of LSI design technology. Some seminar and forums, such as technical seminar for CAD use, refreshing seminar for working people, designer's forums for young professors and students were held in 2011.

【Technological seminar for CAD use】

In a technological seminar for CAD use, VDEC invites lecturer from each tool vender, such as Cadence, Synopsys and Agilent, to hold the CAD operation course. Moreover, the course concerning the design flow in the VDEC environment was held by the VDEC staff. A technological seminar for CAD use for the beginner was held in The University of Tokyo VDEC in August and September at the year 2014. This seminar took 5 days for 2 kinds of Cadence tools, 5 days for 3 kinds of Synopsys tools, 1 days for 1 kind of Agilent tool. In addition, VDEC teachers gave lecturers on transistor level circuit design course, and digital circuit design course under the VDEC EDA environment. Teachers and students up to 40 people attended a lecture in each course, and master the use of each tool for VLSI design flow that uses the VDEC library. Moreover, another technical seminar for CAD use for matured teachers and students was held in March by Cadence 2 kind and 3 days, Synopsys 3 kinds and 4 days, Agilent 1 kind and 1 days (Table 1. 4. 1). The demand for these CAD technological seminars is very large, and VDEC has maintained the mechanism of a large-scale CAD technological seminar holding corresponding to this situation. So far, the seminar was held at the University of Tokyo OR other VDEC branch, however, we started to distribute the lecture using Web streaming, so that students around VDEC branch can take the seminar at the branch school.

Table 1. 4. 1 CAD technological seminar in summer of the year 2013

2014/08/04-05	Synopsys IC Compiler Seminar	Univ. of Tokyo	9
2014/08/04-06	Synopsys IC Compiler Seminar	Kanazawa Univ.	1
2014/08/04-07	Synopsys IC Compiler Seminar	Nagoya Univ.	2
2014/08/04-08	Synopsys IC Compiler Seminar	Kyoto Univ.	2
2014/08/04-09	Synopsys IC Compiler Seminar	Hiroshima Univ.	1
2014/08/06-07	Cadence OrCAD Seminar	Univ. of Tokyo	13
2014/08/06-08	Cadence OrCAD Seminar	Tohoku Univ.	3
2014/08/06-09	Cadence OrCAD Seminar	Nagoya Univ.	1
2014/08/06-10	Cadence OrCAD Seminar	Nagasaki Univ.	5
2014/08/20	Agilent EMPro Seminar	Univ. of Tokyo	12
2014/08/21	Agilent EMPro Seminar	Nagoya Univ.	3
2014/08/22	Agilent EMPro Seminar	Kyoto Univ.	2
2014/08/23	Agilent EMPro Seminar	Osaka Univ.	3
2014/08/21	Synopsys HSPICE Seminar	Univ. of Tokyo	17
2014/08/22	Synopsys HSPICE Seminar	Tohoku Univ.	2
2014/08/23	Synopsys HSPICE Seminar	Nagoya Univ.	1
2014/08/24	Synopsys HSPICE Seminar	Kyoto Univ.	1
2014/08/25	Synopsys HSPICE Seminar	Osaka Univ.	5
2014/08/26	Synopsys HSPICE Seminar	Nagasaki Univ.	3
2014/09/02-03	Digital Design Flow on VDEC Environment Seminar	Univ. of Tokyo	23
2014/09/04-05	Transistor Level Design Flow on VDEC Environment seminar	Univ. of Tokyo	25

2014/09/17-18	Synopsys Design Compiler+Power Compiler Seminar	Univ. of Tokyo	13
2014/09/17-19	Synopsys Design Compiler+Power Compiler Seminar	Kanazawa Univ.	1
2014/09/17-20	Synopsys Design Compiler+Power Compiler Seminar	Kyoto Univ.	1
2014/09/17-21	Synopsys Design Compiler+Power Compiler Seminar	Osaka Univ.	6
2014/09/24-26	Cadence IC61 Virtuoso Layout Seminar	Univ. of Tokyo	22
2014/09/24-27	Cadence IC62 Virtuoso Layout Seminar	Kanazawa Univ.	3
2014/09/24-28	Cadence IC63 Virtuoso Layout Seminar	Hiroshima Univ.	1

2015/03/06	Synopsys TCAD Seminar	Univ. of Tokyo	10
2015/03/07	Synopsys TCAD Seminar	Tohoku Univ.	7
2015/03/08	Synopsys TCAD Seminar	Kanazawa Univ.	2
2015/03/09	Synopsys TCAD Seminar	Nagoya Univ.	1
2015/03/10	Synopsys TCAD Seminar	Osaka Univ.	4
2015/03/11	Synopsys TCAD Seminar	Hiroshima Univ.	3
2015/03/10	Agilent ADS Momentum Seminar	Univ. of Tokyo	10
2015/03/11	Agilent ADS Momentum Seminar	Tohoku Univ.	4
2015/03/12	Agilent ADS Momentum Seminar	Nagoya Univ.	1
2015/03/11	Synopsys XA+VCS mixed sim Seminar	Univ. of Tokyo	7
2015/03/12	Synopsys XA+VCS mixed sim Seminar	Hokkaido Univ.	5
2015/03/13	Synopsys XA+VCS mixed sim Seminar	Tohoku Univ.	5
2015/03/14	Synopsys XA+VCS mixed sim Seminar	Hiroshima Univ.	1
2015/03/18	Synopsys HSPICE Seminar	Univ. of Tokyo	17
2015/03/19	Synopsys HSPICE Seminar	Hokkaido Univ.	3
2015/03/20	Synopsys HSPICE Seminar	Tohoku Univ.	5
2015/03/21	Synopsys HSPICE Seminar	Nagoya Univ.	1
2015/03/22	Synopsys HSPICE Seminar	Kyoto Univ.	1
2015/03/23	Synopsys HSPICE Seminar	Osaka Univ.	5
2015/03/24	Synopsys HSPICE Seminar	Hiroshima Univ.	1
2015/03/25	Synopsys HSPICE Seminar	Nagasaki Univ.	2
2015/03/26	Synopsys HSPICE Seminar	Miyazaki Univ.	6
2015/03/12-13	Cadence OrCAD Seminar	Univ. of Tokyo	5
2015/03/12-14	Cadence OrCAD Seminar	Hokkaido Univ.	4
2015/03/12-15	Cadence OrCAD Seminar	Tohoku Univ.	3
2015/03/25-27	Cadence EDI Seminar	Univ. of Tokyo	6
2015/03/25-28	Cadence EDI Seminar	Hokkaido Univ.	5
2015/03/25-29	Cadence EDI Seminar	Nagoya Univ.	1
2015/03/25-30	Cadence EDI Seminar	Osaka Univ.	7
2015/03/25-31	Cadence EDI Seminar	Hiroshima Univ.	1

【Refresh Seminar for Working People】

Teachers of universities and designers in the first line of the enterprise were invited to the lecturer at "VLSI design refresh seminar" was held aiming at the latest, advanced knowledge and technical learning concerning VLSI design as a refreshing education for working people involved in the integrated circuit industry (Table 1. 4. 2). Though this seminar started chiefly in year 1998 under the support of Ministry of Education Technical Education Division to give practicing education of the latest VLSI design technology, it continues under many supports from many societies.

Course A: analog integrated circuit design (5/26-5/28), Course D:digital integrated circuit design (6/3-6/5), Course M1: MEMS design (6/12-6/13), Course M2:MEMS fabrication (6/25-6/27), and Course R: RF circuit design (7/3-7/4). Teachers from industry and universities involved in the integrated circuit research and the education were invited as the lecturer, and they introduced a state-of-the-art VLSI design technology including the practice using a lecture concerning VLSI design and the latest CAD tool. The participants for the course A, D, M1, M2, R were 22, 21, 7, 6, 17, respectively.

Fig. 1. 4. 1 Refresh Seminar at VDEC seminar room at the University of Tokyo, VDEC.

Table 1. 4. 2 Refresh Seminar

Course A: Analog Circuit Design (3 days)
Analog Circuit Design and simulation Integrated Circuits Verification (LVS, DRC)
Masahiro Sugimoto (Chuo Univ.), Hidetoshi Onodera (Kyoto Univ.), Koji Kotani (Tohoku Univ.)

Course M1: MEMS Design (2 days)
MEMS Basic 1: Fabrication Process MEMS Basic 2: Operation Principle Structual Design Layout Design
Yoshio Mita (Univ. of Tokyo)

Course M2: MEMS Fabrication (3 days)
CAD Design and Analysis Lithography, Etching, Release Vibration measurement and analysis
Yoshio Mita (Univ. of Tokyo)

Course D: Digital Circuit Design (3days)
Verilog HDL Logic Synthesis, P&R, Layout Verification Embede Analog Macros and SRAM
Makoto Ikeda (Univ. of Tokyo)

Course R: CMOS-RF Circuit Design (3days)
Modulation/Demodulation, Cascaded connection Basic Performace, Tranceiver Architecture Circuit Element, Design Flow
Hiroyuki Ito (Tokyo Institute of Technology)

【Designer's forum for young teachers and students】

VDEC LSI designer forum intended for students and young teachers has been held. The VDEC LSI designer forum has aimed to sharing information that cannot be obtained at a society and a academic society, for example, the failure case and the solution in which LSI designer has a hard time, the inside story of CAD industry, the construction method in the design milieu in the laboratory, and so on. This year, we had the meeting in Noro Hot Spring, in August. No less than 31 participants were flourishing at the gathering.

Table 1.4.3 Program of Designers Forum in 2011.

8/29 (Fri)

Time	
10:30-11:00	Reception
11:00-13:00	VDEC Design Award second selection: Short presentation & Poster session & voting/totaling
13:00-14:00	lunch
14:20-14:30	Opening remark
14:30-15:20	Plenary Talk Toshio Yoshida (Fujitsu) SPARC64 XIfx: Fujitsu's Next Generation Processor for HPC
	break
15:30-18:00	VDEC Design Award presentation by the finalists
18:00-20:00	Design Award final totaling, award ceremony

8/30 (Sat)

Time	
10:00-12:00	Ph.D session

1.5 Facilities

The VDEC has provided the big facilities for universities in Japan from its establishment (1996). Big facilities refer to those which are impossible to acquire and or maintain by an individual research unit. Table 1. 5. 1 shows the available facilities of VLSI testers and some process machines, which are placed at the tester room and the super clean room of the Takeda building. In 2004, the VLSI tester (T2000) and the EB lithography machine (F5112+VD01) were donated to the VDEC by the ADVANTEST. In the year 2012, VDEC joined MEXT (Ministry of Education)'s Nanotechnology platform to enforce its multi-use capability. (For Nanotechnology Platform refer section 1. 8). In the FY 2014, VLSI chip integration apparatuses were installed in the cleanroom. The apparatus include Precision Manual Flip-chip Bonding machine (Finetech Fineplacer Lambda, Fig. 1) that can align two chips face-to-face under TV-camera observation. The precision is XY ± 0.5μm, and θ =1 mrad, Semi-Auto Wire Bodner (Westbond 4700E) that can bond gold bump and or bumped wires. Also, Vapor phase HF machine was installed for stable MEMS releasing process. From April 2014 to March 2015, the EB lithography machine F5112 has been used 2074 times. The increase of number since last year (1,594 times) was very large. The reason was opening the new apparatus (F7000S-VD02) to public, yielding average exposure count increase as well (160->173 exposures/month) The facilities can be used by user after learning how to use the a couple of attended use; use result can directly be obtained by attended use.

Table1. 5. 1 Available facility list

Facility	Equipment name	Description	Status	Contact
Logic LSI test System	EB tester: IDS10000	The chip surface voltage during operation can be measured with the LST tester. The digital circuit with 384 pins, 1 GHz can be tested.	Available	equipment@ vdec.u-tokyo.ac.jp
	LSI tester: ADVANTEST T2000	The digital circuit with 256 pins, 512 MHz can be tested. Analog test is optional.	Available	equipment@ vdec.u-tokyo.ac.jp
	FIB: IDSP2X	Cutting wires of LSIs and depositing Pt wires are available to repair the LSI design errors.	Available	IDSP2X@ vdec.u-tokyo.ac.jp
	Auto prober: PM-90-A	Automated prober for testing LSI wafers, which can be used with the LSI testers. The probe card for LSIs with the VDEC standard pin connections is available.	Available	equipment@ vdec.u-tokyo.ac.jp
Analog/RF measurement system	Analog/RF measurement system: HP4156B, HP4284, etc	DC parameter measurement, Capacitance measurement, Network analyzer, Spectrum analyzer, etc.	Available	equipment@ vdec.u-tokyo.ac.jp
	Low-noize manual prober: Cascade Microtec	6 inch wafer can be measured with six DC probles and two RF probes upto 50 GHz.		
	Low-noize, temperature controlled semi-auto prober: Süss Microtec	8inch wafer can be measured. The chip temperature range is -50 to 200℃.		
Nanotechnology Platform Apparatuses	Mask lithography, Direct lithography: F5112+VD01	Minimum linewidth: 50 nm. Lithography for 5 inch photomask (thickness: 2.3 mm), 2-8 inch wafers, and chips is possible.	Available	nanotech@ sogo.t.u-tokyo.ac.jp
	Rapid Mask and Direct lithography: F7000S-VD02	Minimum linewidth: 1xnm. Lithography for 5 inch photomask (thickness: 2.3 mm), 2-8 inch wafers, and chips is possible. Stencil character projection of non-square shapes such as circle, triangle is possible.	Available	

	Chlorine ICP plasma etcher CE-S	High density plasma etching with Cl_2 and BCl_3 is possible.	Available	
	Silicon DRIE MUC-21 ASE-Pegasus	High speed, high aspect ratio etching of silicon is possible	Available	
FIB system	FIB: SII XVision200TB	Repairment of photomask, sample etching, etc. (Through Nanotech. Platform and LCNet)	Available	
Chip Bonding System	Wedge Bonder: Westbond 7476D	25μm ϕ Al or Au wire wedge bonding machine.	Available	
	Epoxy Die Bonder Westbond7200C	Precision Manupilator system. Epoxy and or Ag paste chip bonding and or glued wiring.		
	Semi-Auto Bonder Westbond4700E	18～25μm ϕ Au Ball bonding or bump creation.		
	Precision Manual Flip-Chip Bonder Finetech Fineplacer Lambda	Face-to-face bonding up to 15 mm square chips. Alignment is through video camera. Bonding is by heating chips with TV camera. (Ultrasonic Unit can additionally be purchased.) XY ± 0.5μm, and θ =1mrad precision.		

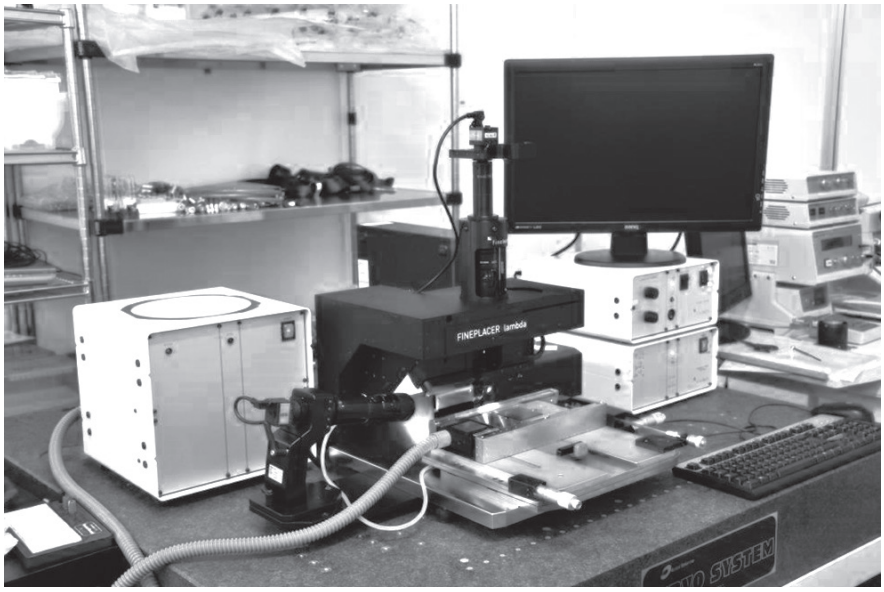


Fig. 1 Precision Manual Flip-Chip Bonder Finetech Fineplacer Lambda

1.6 Activity plan for 2015

VDEC will continue activities on chip fabrication services, CAD tool support, dispatching design related information and donated division "D2T", as has been previous years.

【Design related information dispatching/Seminar】

We will continue holding the following seminars: (1) CAD tools seminars which have been continued since 1997, (2)"Refresh seminar" since 1998, (3)"Designer'Forum" since 1997. We will also continue seminars for LSI tester usage at VDEC and sub-centers, workshops on LSI testing technologies initiated by D2T.

【CAD tool support】

We will continue Cadence tools, Synopsys tools and Mentor tools as the main stream design tools. We will continue analog RF design environment, GoldenGate and ADS by Agilent, C-based design environment, BachC by Sharp. In addition, we continue trial of several CAD tools, such as layout platform, Lavis by TOOL. Design debugging platform from SpringSoft has merged into Cadence tools and will be continued. SmartSpice by Silvaco, will be also continued.

【Chip fabrication services】

We will continue chip fabrication services for 0.18 μm CMOS by Rohm, FD-SOI 28 nm CMOS by ST Microelectronics through CMP and 0.8 μm CMOS by On-semiconductor-Sanyo as the regular services. We will start regular services of SOTB CMOS 65 nm by Renesas Electronics. We will ask packaging for the above chip fabrications to J-Device to meet the diverse needs of the assembly.

Table 1.7.1 Chip fabrication schedule

【CMOS 1.2μm 2P2M】 On-Semiconductor (Former Motorola Japan)

	Chip application deadline	Design deadline	Chip delivery
2015#1	2015/7/6	2015/9/28	2015/12/28
2015#2	2015/12/29	2016/3/22	2016/6/20

【CMOS 0.18μm 1P5M (+MiM)】 Rohm

	Chip application deadline	Design deadline	Chip delivery
2015 #2	2015/4/13	2015/7/6	2015/10/30
2015 #3	2015/6/1	2015/8/24	2015/12/11
2015 #4	2015/8/24	2015/11/16	2016/3/18
2015 #5	2015/11/2	2016/1/25	2016/5/20

【FD-SOI CMOS 28nm 1P10M】 ST Microelectronics

Based on the chip fabrication schedule through CMP.

【SOTB CMOS 65nm】 Renesas Electronics

	Chip application deadline	Design deadline	Chip delivery
2015 #1	2015/6/1	2015/7/13	2016/1/5
2015 #2	2015/12/1	2016/1/12	2016/7/6

1.7 Venture companies related to VDEC

Some professors related to VDEC started venture companies. The following is a list of the venture companies related to VDEC.

[1] AIL Co.,Ltd. (http://www.ailabo.co.jp/)

Related professor : Professor Kazuo Taki, Kobe Univ. (President-Director)

[2] Synthesis Corporation (http://www.synthesis.co.jp/)

Related professor : Professor Emeritus Isao Shirakawa, Osaka Univ. (Director)

Description of business : (1) Hardware/software co-design
(2) System LSI design, design services
(3) Development and sales of IPs
(4) Development of EDA tools

[3] Nanodesign Corporation (http://www.nanodesign.co.jp/)

Related professor :Professor Kazuyuki Nakamura, Kyushu Institute of Technology. (Representative Director)

[4] A-R-Tec Corp. (http://www.a-r-tec.jp/)

Related professor : Professor Emeritus Atsushi Iwata, Hiroshima Univ. (Representative Director)

Description of business : (1) Measurement and analysis of LSI substrate noise
(2) Design of analog-RF mixed signal LSIs
(3) Training of analog design on the JOB method

I. 8 "Nanotechnology Platform": Ultra Small Lithography and Nanometric Observation Site

VDEC is operating an open-use nanotechnology platform "Ultra Small Lithography and Nanometric Observation Site" together with the Institute of Engineering Innovation of Graduate School of Engineering. The site is supported by Japanese Ministry of Education (MEXT)'s Nanotechnology Platform grant. Any researchers in Japanese Universities, Laboratories, and Companies can take full advantage of The University of Tokyo's cutting-edge nanotechnology apparatuses and know-hows. The accessible technology includes Lithography and Etching environment, Ultra High-Voltage Acceleration (1MV) transmission electron microscope (TEM) that is capable of visualizing upto light materials such as Nitrogen. VDEC takes part in the lithography at Takeda Sentanchi Super Cleanroom. Through VDEC's key apparatus F5112+VD01 donated from Advantest Corporation as well as F7000S-VD02 purchased by national budget, VDEC is supporting post-VLSI activities such as MEMS. The machine is capable of rapidly writing patterns on arbitrary-shaped targets sizing from 1cm-sqare chip to 8-inch round wafers. The performance is measured by the number of research reports and machine use. The University of Tokyo site has received 179 (150 for precedent year) research reports including 17 (9) from big companies, 10 (3) from Small and Medium-size Enterprises (SMEs), 36 (32) from other universities, 109 (100) from UTokyo researchers (including external collaboration but excluding VDEC), and 7 (6) from public research institutes. The exposure count was 2074 for 12 months (172.4/month), which is the record since beginning of existing statistics (460 for FY 2000). As shown in the Fig. 1, usage is monotonously increasing. "Open ratio", which is the number of days in which users outside the University of Tokyo came, divided by machine open days, was 99%. Due to the strong support of nanotech. Platform, even a novice user can obtain fine lithography result by using the apparatuses with the Platform Engineering Staffs of VDEC.

URL:http://nanotechnet.t.u-tokyo.ac.jp/

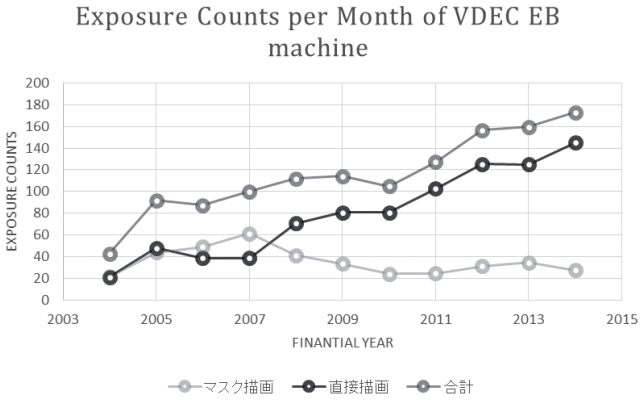


Fig. 1 Monthly Average Exposure Count of EB Machine (s).

2. Activity Report of "ADVANTEST D2T Research Division"

2.1 Introduction of "ADVANTEST D2T Research Division"

2.1.1 Aim of the establishment of "ADVANTEST D2T Research Division"

ADVANTEST D2T research division was established in VDEC in October 2007. As the name of the research division indicates, it is financially supported by ADVANTEST Corporation.

The aim of establishment of ADVANTEST D2T research division is to promote the research and education environment of VLSI testing in all universities and colleges in Japan. "D2T" means that we consider not only design but also test. As the results of our activities, we hope to provide the experts of design and test for industry. In addition, we are exchanging researchers with other universities or research institute in both Japan and overseas. Moreover, D2T research division is in a good environment to make collaboration with industry because testing of VLSI is one of the most practical research topics in industry. Based on those activities, our final goal is to become the center of excellence of VLSI Testing in Japan.

The first phase and the second phase of D2T activities had finished in September 2010 and September 2013, respectively. We are currently in its third phase that started in October 2013 through the courtesy of ADVANTEST Corporation. We have finished the middle year of the third phase with very fruitful achievements in research, education, symposium organization, and so on. Their details are presented in the following sections in this report.

2.1.2 Members of "Advantest D2T Research Division"

Project Lecturer	Rimon Ikeno
Assistant Professor	Nguyen Ngoc Mai Khanh
Researcher	Takahiro Yamaguchi (Advantest Laboratories Ltd.)
Researcher	Masahiro Ishida (Advantest Corporation)
Assistant Clerk	Makiko Okazaki

2.2 Report of “9th D2T Symposium”

“The 9th D2T Symposium” was held on August 26th, 2014 at Takeda Building.

With the main theme of “System, Circuit, and Testing of Ultra-Low Voltage VLSI”, the symposium had eight lectures from wide variety of technical fields like process/device technology, circuit, system, and testing of ultra-low voltage LSI operation. Following these lecture sessions, we had a panel discussion entitled “FD SOI for analog-digital compatibility in ultra-low voltage era” and a reception in the evening. The number of the attendees was more then 180, which made the record through the whole D2T Symposium history. Here we would like to express our warm gratitude again to all these participants at the symposium.

The invited lecturers are distinguished researchers and engineers in each filed. The audience must have made use of such great opportunity to exchange their thoughts with these great lectures at the sessions, the panel, and the reception, we hope.

D2T Symposium will be continuously held in the future. The date of the next, 10th, symposium is fixed in this year in the same season as the 9th symposium. We expect many attendees there again.

9th D2T Symposium Program

10:00	**Opening Remarks** Kunihiro Asada (Director, VLSI Design and Education Center, The University of Tokyo) Yoshiaki Yoshida (Director, Advantest Corporation)
10:15	*"Activities of ADVANTEST D2T Research Division, VDEC"* Rimon Ikeno (The University of Tokyo)
10:25	**Session 1** *"Phase Noise and Jitter in Circuits: Origins, and How They Affect Signals"* Asad A. Abidi (University of California, Los Angeles) *"Numerical and Theoretical Analysis on Voltage and Time Domain Dynamic Range of Scaled CMOS Circuits"* Toru Nakura (The University of Tokyo) *"A Subsampling Stochastic Coarse-Fine ADC with SNR 55.3dB and >5.8TS/s Effective Sample Rate for an on-Chip Signal Analyzer"* Takahiro J. Yamaguchi (Advantest Laboratories)
12:00	**Lunch**
13:15	**Session 2** *"Present Status of Characteristics Variability in Advanced MOSFETs"* Toshiro Hiramoto (The University of Tokyo) *"Process and Design Differentiations at Ultra-Low-Voltage in UTBB FDSOI 28nm"* Philippe Roche (ST Microelectronics) *"Ultralow-Voltage Design and Technology of Silicon-on-Thin-Buried-Oxide (SOTB) CMOS for Highly Energy Efficient Electronics in IoT Era"* Nobuyuki Sugii (Low-power Electronics Association & Project)
15:15	**Coffee Break**
15:45	**Session 3** *"Cross-Layer Approaches for Variation-aware System Design"* Mehdi B. Tahoori (Karlsruhe Institute of Technology) *"30-Gb/s Optical and Electrical Test Solution for High-Volume Testing"* Daisuke Watanabe (Advantest Corporation)
16:50	**Break**
17:00	**Panel Discussion** *"FD SOI for analog-digital compatibility in ultra-low voltage era"* Moderator: Toshiro Hiramoto (The University of Tokyo) Panelists: Asad A. Abidi (University of California, Los Angeles), Philippe Roche (ST Microelectronics), Nobuyuki Sugii (Low-power Electronics Association & Project), Mehdi B. Tahoori (Karlsruhe Institute of Technology)
18:20	**Closing Remarks**
18:30	**Reception**

2.3 Research Activity Reports of "Advantest D2T Research Division"

On-chip Digitizer/On-chip Spectrum Analyzer

Takahiro Yamaguchi, Nguyen Ngoc Mai Khanh,
Rimon Ikeno, Satoshi Komatsu, Kunihiro Asada

A new transition-edge search circuit is introduced which utilizes a stochastic comparator group. By incorporating stochastic properties into the circuit, this design accelerates the accumulation of data and enhances test quality.

We developed a test chip based on a differential-signal comparator which improves symmetry of the offset property. We expect more precise evaluation of the stochastic properties with the chip. Since the chip contains all required components for our sub-ranging ADC architecture, we plan system-level demonstration of the architecture using this test chip.

Power Integrity Evaluation Method

Masahiro Ishida, Akira Matsukawa, Rimon Ikeno,
Toru Nakura, Kunihiro Asada

While a required power supply voltage has become lower due to the advanced miniaturization of the semiconductor process, the power supply current consumed by a semiconductor device has increased because of the huge number of transistors integrated on a single chip. It may increase the power supply noise, and power integrity issues of the device under test in both an ATE and a practical operating environments.

In this research project, we propose two methods for evaluating power integrity at on-chip power supply nodes in semiconductor devices: a power integrity testing method and a power delivery network modeling method.

This year, we have constructed an experimental setup for evaluating a TEG chip which is fabricated to demonstrate the concept of the proposed power integrity testing method for detecting power integrity faults in the DUT. For the power delivery network modeling, we have produced an algorithm for calculating a simple circuit model of the on-chip power delivery network based on power integrity measurements, and confirmed its operation by using computer simulations. Furthermore, in order to demonstrate the feasibility of the proposed method, we have conducted experiments of comparison between an actual power delivery network circuit extracted from laid out CMOS circuit and a simpler circuit model derived from the CMOS circuit.

High-throughput and high-accuracy electron-beam direct writing (EBDW) strategy for wide range of EBDW applications

Rimon Ikeno, Satoshi Maruyama, Yoshio Mita,
Makoto Ikeda, Kunihiro Asada

Maskless lithography by Electron-Beam Direct Writing (EBDW) lithography is expected as a low-cost and short turn-around time (TAT) lithography technology, but it also has some drawbacks like low process throughput and low accuracy against the intended layout shapes. We are pursuing high-speed and high-accuracy EBDW strategy utilizing Character Projection (CP) method to overcome these concerns and to boost EBDW use in arbitrary fields like MEMS, photonics, and so on.

This year, we proposed a layout data conversion methodology that enables high-accuracy CP exposure of arcs and oblique edges, where the conventional Variable Shaped Beam (VSB) exposure might give poor accuracy or considerable roughness in the resultant structures. We demonstrated it with the practical device structures like curved light wave guides, and confirmed its effectiveness in reducing EB shot count.

We are processing test fabrication of the device structures to evaluate both device shapes a performance in cooperation with the other research groups inside/outside the university.

2. 4. Publications

Journals

[1] Satoshi Komatsu, Takahiro J. Yamaguchi, Mohamed Abbas, Nguyen Ngoc Mai Khanh, James S. Tandon, Kunihiro Asada, "A Flash TDC with 2.6-4.2 ps Resolution Using a Group of Unbalanced CMOS Arbiters," IEICE TRANSACTIONS on Fundamentals of Electronics, Communications and Computer Sciences Vol.E97-A No.3 pp. 777-780, March 2014.

[2] Rimon Ikeno, Takashi Maruyama, Satoshi Komatsu, Tetsuya Iizuka, Makoto Ikeda, Kunihiro Asada, "A Structured Routing Architecture for Practical Application of Character Projection Method in Electron-Beam Direct Writing," IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol. E97-A, No. 8, pp. 1688-1698, August 2014.

International Conferences/ Symposiums/Workshops

[1] James S. Tandon, Takahiro J. Yamaguchi, Satoshi Komatsu, Kunihiro Asada, "A subsampling stochastic coarse-fine ADC with SNR 55.3 dB and >5.8 TS/s effective sample rate for an on-chip signal analyzer,"2014 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 93-96, June 2014.

[2] Masahiro Ishida, Takashi Kusaka, Toru Nakura, Satoshi Komatsu, and Kunihiro Asada, "Statistical Silicon Results of Dynamic Power Integrity Control of ATE for Eliminating Overkills and Underkills," IEEE International Test Conference, pp. 1-10, October 2014.

[3] Takahiro J. Yamaguchi, James S. Tandon, Satoshi Komatsu, Kunihiro Asada, "A Novel Circuit for Transition-Edge Detection: Using a Stochastic Comparator Group to Test Transition-Edge,"2014 IEEE 23rd Asian Test Symposium (ATS), pp. 168-173, November 2014.

Chapter 3 Research in VDEC

Asada, Nakura and Iizuka Laboratory

(http://www.mos.t.u-tokyo.ac.jp)

Supply Fluctuation Monitoring, Analysis and Reduction Method

Kunihiro Asada, Toru Nakura, Masahiro Kano and Satoshi Matsukawa

In recent years when nm process and GHz operation are normal, it becomes a problem that power supply noises, such as di/dt noise and resonant power supply noise, are caused by parasitic inductances in package bonding and power supply networks.

We aimed at the mitigation of area penalty with the passive decap widely used to reduce supply noise, so we considered active charge injection with capacitor. We have developed the environment to optimize injection current to minimize the quantity of injection charge under the constraint that power supply voltage fluctuation within a certain level is allowed. As a result, the area penalty of optimized active charge injection became about 40 smaller than that of passive decap.

Also, we have proposed the method for impedance estimation of on-chip power supply networks. In this method, by measuring current flowing in each power supply pin when operating each current load which is placed on the chip in advance, the simple circuit model is created which is composed of resistance, capacitance, and inductance. Determining the parameters of the model by least squares method to minimizing the difference between the response of the chip and it of the model, we can estimate the distribution of impedance. Moreover, we confirmed that the voltage fluctuation on the

power supply network can be estimated by simulating the model.

Reliability Improvement of LSIs with the fine pitch process

Kunihiro Asada, Toru Nakura, Kazuhiro Mori, Maruf Hossain

NBTI degradation is one of the important problems of reliability in nano-scale transistors. We propose an accurate transient simulation method of NBTI degradation based on Reaction-Diffusion model by calculating hydrogen distribution at gate oxide in each transistor according to the gate input level obtained by logic simulations, and an acceleration scheme of NBTI simulation based on the frequency dependence of NBTI degradation. In this method, hydrogen distribution enables simulation from continuance of a place at which input parameter is changed.

And, in an analog to digital converter, comparators are used to decide whether the analog input is greater than or less than the reference voltage. But in an actual comparator circuit, the reference voltage fluctuates and thus has a range of uncertainty. By using a set of stochastic comparators, analog input within this uncertainty range can be converted to digital signal. Therefore, the relations between the parameters of a set of stochastic comparators have been derived analytically. It is showed that effective resolution is inversely proportional to the Probability Density Function (PDF) of the reference voltage fluctuation and the total number of comparators. Then, this configuration is used with traditional comparators to form a sub-ranging ADC. The optimal point of operation of this circuit is found by modeling the PDF as a Gaussian Distribution.

Sub-MMW Pulse Generation using CMOS

Kunihiro Asada, Toru Nakura, Parit Kanjanavirokju

The target of this research is to implement sub-millimeter wave pulse generator for short-range imaging and radar application. Recent literature focus on generating continuous wave oscillator, normally based on push-push technique. As opposed to those continuous wave generator, we have proposed a direct sub-millimeter wave pulse burst generator circuit based on transmission line to realize a wide-band pulse with frequency even higher than Fmax. We have shown that energy conversion efficiency can be increased by our proposed technique. The circuit consist of on-chip trigger and off-chip passive transmission line resonator. A test chip has been verified using standard FR-4 board. The generated pulses by the prototype circuit still has low output power and power conversion efficiency. We are working towards higher frequency by using better board and

flip-chip technique.

Surface magnetic field modeling for LSI security

Kunihiro Asada, Toru Nakura, Yuki Oda

In recent years, side channel attack has been developed to expose the secret data in encryption LSI. Magnetic field from LSI is used to anomaly detection. This method models the magnetic field using the wire layout patterns and the current values estimated by SPICE simulation. However, magnetic field is influenced not only by the current in wire but also by the current in base. In this research, we estimated the effect of base current by using electromagnetic field simulation. This simulation showed in which condition the effect of base current cannot be ignored.

Time-Domain Circuit Design

Kunihiro Asada, Toru Nakura, Toshiyuki Kikkawa, Tomohiko Yano, Takehisa Koga, Takashi Toi

In our research, we employed time domain techniques on some conventional circuits and improved their performances.

First of all, we proposed a fully differential time-mode signal integrator. Having only one buffer-ring to hold a time-mode signal, the proposed integrator has smaller systematic input-referred time offset error compared with previous works.

We also worked on the research of Phase Locked Loop (PLL).

We proposed an on-chip measurement method of PLL transfer function. In our proposed scheme, we modulated the phase of the PLL input in triangular form by Digital-to-Time Converter (DTC) and read out the response on the PLL feedback signal by Time-to-Digital Converter (TDC). By combination of the DTC and TDC, we can derive the transfer function of the PLL both in the amplitude domain and the phase domain. Since the DTC and TDC can be controlled and observed by digital signal, the measurement can be conducted only by slow digital signals.

We also improved a robustness of Pulse Width Controlled PLL (PWPLL) using Soft-Thermometer Code. Conventional PWPLL is not adaptable to process, voltage, and temperature (PVT) variations. Therefore we proposed a PWPLL with frequency calibration function which has a length-variable ring oscillator. Both open-loop and closed-loop transient simulations demonstrated that the proposed PWPLL was adaptable to the PVT variations. We also designed a prototype chip of the PWPLL in 0.18 um CMOS process.

Finally, we worked on an improvement of the Pulse-Shrinking (PS) TDC. PSTDC has some advantages of small area and high resolution. However it has relatively high nonlinearity. The main cause of the nonlinearity is difference between the rise and fall propagation delay of the buffer which shrinks the input pulse. We proposed an architecture that gives offset width of 1ns to the input pulse and completes the time-to-digital conversion when the pulse width gets smaller than 1ns.

Radiation Detector Utilizing Semiconductor Photodiode Based on Standard CMOS Technology

Kunihiro Asada, Toru Nakura, Zhu Hongbo, Yang Xiao, Kai Xu

Scintillation detectors and semiconductor detectors have received wide spread attention since they can specify the nuclide of radiation and estimate the arrival angle. Former research proposed a detector using the cube scintillator, SPAD (Single Photon Avalanche Diode) array image sensors, multi-coated materials, and pinholes and verified the technique to detect the locus of the lighting electron by this detector. However the detect and estimate costs plenty of time. This research proposed a technique to detect the location of the electron emitting light in high speed utilizing the periodicity of the arrangement of the pinholes and SPADS. The result of the simulation verified that by using this technique the location of the electron emitting light in a scintillator could be detected with a spatial resolution of 20 um within 20-40 seconds. About the structures of SPADs we have tested, the p-well/deep-n-well with poly gate SPAD shows the lowest DCR. A summation circuit to count the number of breakdown pixels in SPAD array, and a circuit that only output the address of breakdown pixels had been fabricated. And the functions of these circuits were experiment demonstrated.

Fujita Laboratory

(http://www.cad.t.u-tokyo.ac.jp/)

Partial synthesis and Engineering Change Order (ECO)

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Satoshi JO, Kentaro IWATA

Engineering Change Order (ECO) may happen in a design due to a bug fix or a change in the original specification. ECO is expected to be a small change. Therefore, we want to reuse the previous circuit topology and the layout as much as possible to keep the previous timing optimizations of the design as much as possible. Hence, reducing the overall time of applying the change. In this work, we propose an ECO method that keeps the previous circuit topology of an old circuit and tries to accommodate the new circuit functionality by changing minimum number of gates. We have defined the gate change model using a number of parameter variables. By changing the parameters, a gate type can be converted to another gate type. Experimental results shows that selecting more gates as candidates to be changes results in better ECO success rate. Moreover, more candidate gates results in longer ECO runtime.

Automatic Test Pattern Generation (ATPG) for Multiple and Various Faults

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Naoki TAGUCHI, Satoshi JO

Due to the continuous shrinking of semiconductor technology, there are more and more subtle errors or faults widely distributed in manufactured chips, and traditional "single" stuck-at fault model may become inappropriate. It is definitely better if all combinations of multiple faults can be completely tested. In this work, we present ATPG (Automatic Test Pattern Generation) techniques targeting all multiple stuck-at faults, i.e. all combinations of stuck-at faults. That is, given "n" possibly faulty locations in a circuit, the target set of faults consists of 3n - 1 fault combinations, as each possibly faulty location is under stuck-at 1, stuck-at 0, or normal/non-faulty. Traditional ATPG flows use fault simulators to eliminate all detectable faults by the current set of test vectors. The problem, however, fault simulators represent fault lists explicitly in the sense that all possible faults are enumerated in the fault lists. This prevents us from dealing with ultra large fault lists, such as 3n - 1 faults. We need "implicit" representation of faults in order to deal with such huge numbers of faults or fault combinations. We present SAT based formulations for ATPG of circuits having very large numbers of faults by implicitly eliminating detected faults. We solve a set of SAT problems whose constraints increase pure incrementally (here "pure" means never deleting constraints), and so the entire solving process can be very efficient, as all learnings obtained so far are valid in the following SAT problems. Experiments are performed on combinational parts of ISCAS89 circuits in their AIG (AND-Inverter Graph) representations. We have successfully generated the complete set of test vectors assuming that faults happen only at outputs of gates. Our ATPG techniques can also start with a given set of test vectors. If we start the ATPG processes with a set of test vectors for single stuck-at faults, we can obtain the set of additional test vectors required for multiple stuck-at faults. Results are a little bit surprising in the sense that we need very few additional test vectors for multiple faults, although the numbers of fault combinations are exponentially larger. As far as we know, for the first time, complete test vectors for all stuck-at faults for ISCAS89 circuits where faults happen only at outputs of gates in AIG representations of the circuits have been obtained.

Verification and Debugging of Processor Architectures

Masahiro FUJITA, Amir Masoud GHAREHBAGHI

Processor architectures are becoming more complicated by adopting various functionalities for higher performance and more reliability, such as pipelining, speculative execution, and error recovery. To ensure the correctness of complicated processor architectures, verification and debugging of processor architectures are a key issue. In this work, we present a method for automatic rectification of design bugs in processors. Given a golden sequential instruction-set architecture model of a processor and its erroneous detailed cycle-accurate model at the micro-architecture level, we perform symbolic simulation and property checking combined with concrete simulation iteratively to detect the buggy location and its corresponding fix. We have used the truth-table model of the function that is required for correction, which is a very general model. Moreover, we do not represent the truth-table explicitly in the design. We use, instead, only the required mint-

erms, which are obtained from the output of our back-end formal engine. This way, we avoid adding any new variable for representing the truth-table. Therefore, our correction model is scalable to the number of inputs of the truth-table that could grow exponentially. We have shown the effectiveness of our method on a complex out-of-order superscalar processor supporting atomic execution of instructions. Our method reduces the model size for correction by 6.0x and total correction time by 12.6x, on average, compared to our previous work.

Acceleration of Calculation with FPGA

Masahiro FUJITA, Taro KAWAO

Dedicated hardware is generally faster and more energy-efficient than a general hardware. A circuit optimized for specific calculation can be obtained without chip fabrication using a Field Programmable Gate Array (FPGA), which is a programmable circuit. In this work, we have considered acceleration of simulation of neural network and analysis of electromagnetic field.

Neural network is a mathematical model of the mechanism of a brain. We implemented a highly pipelined circuit on a FPGA to simulate the network composed of 256 spiking neurons and we could accelerate the simulation by 320x compared to real time calculation on a general purpose processor. This circuit is designed to be scalable to the number of neurons. In the future work, we will use multi-FPGA network to simulate tens of thousands of neurons.

Continuous miniaturization and performance improvement of electronic equipment causes more serious electromagnetic interference problems than before. Insufficient performance of current simulators lead to depending on real testing equipment with higher cost. To tackle this problem, we are working on a fast simulator using FPGA that runs several times faster than a sophisticated multi-core software simulator.

Post Silicon Verification and Debugging

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Shridhar CHOUDHARY

Due to increase of the size of VLSI, it has become very hard to detect all design bugs in design phases before fabrication, which increases the number of bugs that escape verification processes before fabrication and are firstly detected by running a chip after fabrication. In addition, a risk of electrical errors is increasing as fabrication processes shrink. In this work, we have focused on post-silicon debugging techniques based on trace buffers. The main problem is that only a limited number of signals can be traced, due to the area overhead that is introduced by trace buffers. Therefore, it is important to select the signals which can restore most of the other ones. There exist researches that try to heuristically select a set of state variables (flip-flops) which maximizes the restorability. Those existing works are not so robust and the cost functions used for selections do not work well in some cases. We have introduced a method that tries to improve the initial selection by repeatedly swapping the flip-flops to be traced. Moreover, we have a hardware based implementation of the method. As the hardware-based swapping is faster than software by 4-5 orders of magnitude, we can swap much more times and can get consistent results even for large circuits. Results shows signal restoration improvement up to 30% for ISCAS89 circuits.

Efficient Topological Matching Among Multiple Circuits

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Hossein IZADI RAD

Recognizing similarities and differences among multiple circuits is very useful for managing and maintaining IP libraries as well as merging circuits, fraud detection, reverse engineering, and redundancy checking. In this work, we address the problem of finding the maximum common subcircuit among two or more logic circuits. Given the gate-level netlists of the circuits, first we represent the circuits as graphs. Then, we try to find the largest common subgraph, following the common approaches that are used for identifying matched graphs. In the first step, we build a conflict graph from the circuit graphs. In the next step, we try to find the largest common subgraph by finding independent sets of the conflict graph, using our proposed near-linear approximation algorithm. Finally, we try to increase the size of the largest common subgraph by considering neighbors of the circuit graph nodes, step-by-step in a controlled manner. We have performed extensive experiments on ISCAS85 circuits as well as a number of IPs from OpenCores. Comparing our results to the optimum solution that is obtained by an exact algorithm, the average size of the identified common subcircuit is

around 10% smaller, but the average processing speed is two to three orders of magnitude faster. For example, our proposed algorithm needs less than 20 minutes for a circuit with 100,000 gates. Moreover, the size of the common subcircuit that is identified by our method is on average 60% larger than the one that is identified by a state-of-the-art graph manipulation tool-set.

Interrupt Analysis for Realtime Software based on HW/SW Co-Testing using Concolic Execution

Masahiro FUJITA, Yusuke KIMURA

As the software of embedded systems become more complex, its verification becomes harder. As a result, we need more sophisticated and more efficient verification methods. Interrupt is one of characteristic functions of real time embedded systems. In this work, we have focused on verification of interruptions in an embedded software. We have proposed a comprehensive analysis method using Concolic Execution. In order to reduce the huge number of required test patterns, we extract the restrictions from the Simulink model of the target embedded system, and apply them during the verification.

Takamiya Laboratory

(http://icdesign.iis.u-tokyo.ac.jp/)

Energy Efficient Extremely Low Voltage VLSI Circuit Design

Makoto Takamiya, Hiroshi Fuketa, and
Takayasu Sakurai

Reducing the power consumption of every electronic device is required to mitigate the global warming. To meet the requirement, VLSI circuit design techniques including logic circuits, memory circuits, analog circuits, power management circuits, and wireless transceiver circuits operating with the 0.5-V power supply voltage are developed with 65/45 nm CMOS process to reduce the power consumption to 1/10 of the conventional VLSI's.

Large Area and Flexible Electronics with Organic Transistors

Makoto Takamiya, Hiroshi Fuketa, Takao Someya, and
Takayasu Sakurai

Large area electronics is a new frontier in electronics where intelligent electronic devices are distributed on a flexible surface, 10 cm to 10 m on a side, for the human interface and the comfortable daily life. Flexible and low-cost organic FETs (OFETs) are suitable for large-area electronics and have great potential as a supplement of solid and expensive silicon MOSFETs for VLSI's. We have proposed and demonstrated several large area and flexible applications including a surface electromyogram measurement sheet for prosthetic hand control, a flexible wet sensor sheet for biomedical applications, and a fever alarm armband.

Ikeda Laboratory

(http://www.mos.t.u-tokyo.ac.jp)

Current Research Projects

Jacob Shearer

3D-range finding based on light-section method by Smart Image Sensors

M. Ikeda, H. Yabe, D. Uehara, J. Shearer

Two chips for 3-D measurement based on light section, where we can measure the shape of the 3-D object using sheet light. The first chip is a dual-core image sensor for high-speed texture mapping. The two pixel arrays on the chip can operate in either 2-D or 3-D mode. In 2-D mode we are using two exposure modes: 1. Under background light, obtain part of the object which is not illuminated by the sheet light, 2. In dark condition, obtain the image by lowering sensitivity. The second chip proposes an image sensor chip which can detect sheet light on the pixel array. Each column of the pixel array of our proposed sensor has two minimum voltage circuits, which can be used to detect the line position without reading out all the pixel intensity values by performing binary section and linear search on the array. Our proposed method can realize a high-speed and highly effective 3-D acquisition.

3D-range finding by Smart Image Sensors

M. Ikeda, T. Matsushima

Time-of-Flight (ToF) method and light-section method are representative of 3-D imaging methods. In ToF method, infra-red light is projected to the object and we obtain the delay time between projected light and

reflected light by the sensor. 3-D information of the object is obtained by this delay time. In light-section method, sheet light is projected to the object and we scan the sheet light on the surface of the object. We acquire 3-D information by triangulation. We study the sensor which can be applied to both ToF and light-section method. The pixel of our sensor consists of a couple of lock-in pixels. It enables improving the efficiency of speed and area in ToF method. Our sensor also realizes fast and accurate position detection of sheet light in light-section method by combining single-slope ADC and priority encoder. We evaluated a trial chip.

Application of electrostatic MEMS scanner integration with image sensor

M.Ikeda, S.Maruyama

We have studied co-integration of MEMS (Micro-Electro-Mechanical Systems) and CMOS image sensors. MEMS micro-mirrors have features that are smaller than galvanometer mirrors, lower driving voltage, and co-integrate with LSIs by micro-fabrication process. PWM (pulse width modulation) driving of MEMS enables to simplify ADC and DAC for controlling MEMS devices. The target of this study is to include capacitance sensor for micro-actuator for mirror position detection and mirror position calibration circuits to realize high-precision, high-speed and low power scanner.

Cryptographic processor by Self-Synchronous Systems

M. Ikeda, M. Tamura, T.Ikeda

Our research theme is implementation of cryptographic algorithm using self-synchronous circuit. Many calculations are needed in encryption and decryption process and in some cases high throughput is required. So we utilize high-speed performance of self-synchronous circuit. Two algorithms are researched in our laboratory. One is RSA and the other is elliptic curve cryptography (ECC). RSA is the cryptography using exponential and modular calculation. In this reserch, self-synchronous RSA circuit using Montgomery power ladder algorithms is desined in different way, and comparing each of them in the point of area and speed reveals the best implementation of RSA. To execute faster modular calculation, Montgomery multiplication method is used for RSA. A RSA circuit has a Montgomery multiplier and there are 3 types of Montgomery multiplication algorithm. Montgomery multiplier using different algorithm has different arithmetic core. Furthermore, there are 9 types of arithmetic core, with different port width in each algorithm so that RSA circuit can be designed in 27 different ways. ECC is the cryptography using elliptic curve over finite field. Elliptic curve digital signature algorithm (ECDSA), one of the ECC, is researched in our laboratory. In ECDSA, private key is used to generate signature and public key is used to authenticate. Scalar point multiplication is performed in those processes. There are a lot of methods to perform scalar point multiplication. First, we have to decide which kind of field is used. There are two kinds of field, binary field and prime field. We use prime filed because of robustness. Second, we have to decide which coordinates are used. In some projective coordinates, modular inversion is not needed so throughput is improved. Finally, scheduling is considered and implemented by using self-synchronous circuit.

Design flow of Self-Synchronous Systems

M. Ikeda, A.Ito

We have studied design flow of the self-synchronous system with gate-level pipelining, to realize automatic design like synchronous systems. Starting with VerilogHDL, obtain netlist with 2-inputs gates by Synopsys DesignCompiler, and translate it into 3 to 4 input gates by ABC developed by UC Berekeley, and insert buffers again by ABC to equalize number of gate stages. We have also studied loop conditions for throughput optimization.

SEU resistivity of Self-Synchronous System based on Dynamic Circuits

M. Ikeda, D. Sai

SEU (Single Event Upset) by radiation becomes critical for the advanced CMOS circuits. We have studied SEU tolerance of the self-synchronous system with dynamic circuits. We carried out spice simulation injecting charges mimicking neutron injection, and classified SEU types for the dynamic circuits. We also realized simple estimation method of collision cross-section of neutron, from netlist. SEU tolerance for the dynamic circuits can be estimated by temporal probability

obtained by simulation, and special area estimation.

Mita Laboratory

(http://www.if.t.u-tokyo.ac.jp)

Study on LSI-MEMS integrated pond-skating robot for energy-autonomous distributed microsystems

Y. Mita, I. Mori, Y. Okamoto, Y. Li,
A.J. Walton (Univ. of Edinburgh)

As one example of integrated MEMS that is expected to open new research and industrial application fields, the authors are trying to show a top-down application of energy-autonomous distributed microrobots. The research belongs to the "top-down" research category and through the research the team looks forward to provide the "Engineered Nature"; the team does not intend to just copy how nature works in implementation level, but to realize with cutting-edge technologies what nature is aiming at in highly-functional level. Recent top-down activities include autonomous distributed mobile robot: "Pond Skater", which to date had not been realized by any other microsystems group. The availability of a leading low voltage technology at the Scottish Microelectronic Centre (SMC) the University of Edinburgh that could electrically change surfaces from hydrophobic to hydrophilic proved to be crucial to achieving this goal as was the previous involvement of SMC staff in wireless technology. The major challenge is propulsion, and it is clear that directly mimicking the pond skating insect's propulsion mechanism would be problematic. The idea that was developed was to propel the device using Electro-Wetting Of Dielectric (EWOD) to move air bubbles, which had the significant advantage that there we no moving mechanical parts, which simplified the construction and helped to minimize the weight which was important if the pondskating device was to float using surface tension. Based on the world's first wireless pond-skating propulsion, the team is developing VLSI control circuit and integration technology for continuous skating. In FY2014, a first experiments of remote EWOD driving was successfully performed by integrating CMOS-post-processed one-chip HV generating photovoltaic cells and Ta_2O_5 EWOD device made at UTokyo Takeda Cleanroom.

LSI-MEMS integrated device by submicron-wide opening deep reactive ion etching technology

Y. Mita, T. Sawamura, I. Mori, A. Hirakawa, K. Yasuda, M. Kubota

Narrow and deep structures such as microholes and trenches are playing key roles in modern electro and mechanical systems. In standard micro fabrication technology, patterns are composed of rectangles and vertically transferred to the depth direction, yielding long-cubic structures. However, just by thinking of lens shape, one can realize that cubic shape is not necessarily the optimum shape for all kinds of applications. Hence it can be said that the ideal micro fabrication technology must be capable of realizing surfaces having arbitral curvatures that are top-down requested by applications. The team aims at acquiring comprehensive study on such "arbitral curvature providing micro fabrication technologies" from three aspects: (1) Top-down concrete applications, (2) Enabling micro fabrication methods by cutting-edge technologies and ideas, and (3) non-destructive profiling method of such surfaces. Top-down applications published in FY 2013 include (1-5) thermal energy harvester that takes full advantage of profile control by DRIE tuning, as well as (2-4) Experimental analyses of trench vertical profile with process parameters were performed.

Smart Blocks II project–Wireless operation UV patterned polyimide microactuator

Y. Mita, N. Sakamoto, Y. Okamoto, K. Kawahara,
J. Malapert (FEMTO-ST), M. Ataka, H. Fujita

In a framework of French national research project (ANR) "Smart BlocksII", Dr. Julien Malapert stayed in Mita Lab., to develop a brand-new thermal microactuator array and control circuit. Following a successful demonstration of the microactuator array with maximum displacement amplitude of 15μm and cut-off frequency of 10 Hz, the team integrated the actuator array into a 2.5 cm-cubic "smart block" demonstration device. The block was with ZigBee-communicating microcontroller and lithium polymer battery. The team was successful in tele-operating the microacauator array. The device was appreciated in the MICRONORA exposition held in Besançon in September.

An LSI probing system with CMOS-MEMS

Y. Mita, R. Setoguchi and M. Kubota

The team is developing a "MEMS" probe card for electron device testing such as VLSI. The originality is to integrate CMOS circuit to provide high functionality. In the year 2014, a piezo-resistive stress measurement circuit was developed to quantify real stress put on the probe. A company-made polysilicon resistor, made by post-processing commercial CMOS 0.6μm 1P2M circuit, was integrated into cantilever and responded to the stress with good gauge factor (around 20).

Design and Development of Micro-Latch Mechanism for Low-Power and Long-Life MEMS Memory

Y. Mita, K. Komeda, M. Kubota, A. Tixier-Mita

A low-power and long-life MEMS memory having data retention time over 1,000 years, write power under pico-Joule, and zero power for data retention. One of the application scenarios is cumulative hazard (such as total exposure to radioactivity and or chemicals) memory. The proposed multi-level memory stores the information in terms of mechanical energy stored in the MEMS spring that may yield low-power writing energy and stable data retention. In the year 2014, a zero hold-power memory device has been realized.

Right-Brain-Computing Integrated Circuits: Associative Processing Systems

B. Ka, N. Yamashita, Y. Mita

Digital computers are dedicated machines for vary fast execution of numerical calculations. However, their performance is extremely poor in such tasks like seeing, recognizing, and taking immediate actions, which are effortless tasks in our daily life. This research aims at building intelligent VLSI systems based on the psychological model of a brain. In our system past experience is stored as template vectors in non-volatile vast memories and the maximum-likelihood event to the current event is recalled in real time by a fully parallel processing. The key ingredient of the system is a new functional device called "Neuron MOS Transistor" (neuMOS or νMOS) which mimics the action of a nerve cell neuron at a single transistor level. Based on such architecture that "association" is the very computing primitive, we are pursuing human-like intelligence system implementation directly in silicon integrated circuits. Currently research is in progress for robust image recognition and classification processing including robust feature extraction. The sate-of-the-art silicon technology has been utilized to implement such associative processors in both analog and digital CMOS VLSI chips.

Micro Wireless Resonant Power Transfer that Enables Metabolism of Fragile MEMS Actuator.

Y. Mita, N. Sakamoto, B. Stefenelli,
A. Kaiser (ISEN/IEMN-CNRS)

The most severe problem of MEMS in which microactuators are exposed to the external world, such as SmartBlocksII demonstrators, is that fragile microactuators are little by little broken during usage, and finally the entire system become unusable. The team proposes a "Metabolism MEMS" concept–the system is composed with detachable two parts: One is fragile MEMS and the other is robust VLSI. The fragile MEMS are replaceable so that the system can have always a "fresh" surface. The key enabling technology is wireless energy and command transfer, with on electrical wiring in between. For that purpose the team tries to use resonance power transfer method in the submillimeter-scale, 1 GHz-range carrier. By Phenitec Semiconductor VDEC run LC oscillator was fabricated. Magnetic power coupling experiments were successful in between the LSI and power receiver with ciliary motion MEMS actuator.

"Sixth Sense" Devices with CMOS-MEMS Technology

Y. Mita, S. Inoue, M. Denoual (ENSI de Caen, France),
Eric Lebrasseur,
Jean-Bernard Pourciel (LAAS-CNRS, France),
Takahisa Masuzawa (professor emeritus UTokyo)

One of the most important application field of MEMS is "sixth sense", which means that sensors that can detect physical and chemical amount that cannot be sensed by human beings'sensors. The team aims at solving this issue by VLSI-integrated compact microdevice. The development includes an integrated bolometer that can detect infrared wave very rapidly and sensitively, and integrated system that can make profiling of very small holes.

Takagi-Takenaka Laboratory

(http://www.mosfet.k.u-tokyo.ac.jp/)

Current Research Projects

III-V/Ge Metal-Oxide-Semiconductor (MOS) FETs

S. Takagi, M. Takenaka, Cai Weili, Yu Xiao, WuKang Kim, Chang Chih-Yu, Kouichi Nishi, Ke Mengan

We have conducted the research on high-peformance III-V/Ge MOSFETs.

We have successfully demonstrated wafer-size scalable III-V-OI wafer by using the direct wafer bonding of III-V epi on Si substrate. By using the III-V-OI, the high-performance InGaAs MOSFETs were obtained. We have also demonstrated InAs/GaSb CMOS by using the wafer bonding.

We have also obtained high-quality Ge-on-Insulator (GOI) wafer by suing high-temperature Ge condensation.

Tunnel FET

S. Takagi, M. Takenaka, Min-Soo Kim, Kouichi Nishi, Sangmin Ji, Daehwan An, Daiki Ueda

For low-power application, tunnel FET, which can exhibit steep subthreshold slope have been investigated. We have found that even in high-indium-content InGaAs channel, a low Ioff and steep subthreshold slope can be obtained by using the InGaAs quantum well structure. We have also developed Ge/s-Si TFET for high Ion operation.

Si CMOS photonics

M. Takenaka, S. Takagi, Y. Kim, J. Han, J. Kang, K. Takeuchi

High-sensitivity Ge photodetectors (PDs) has been investigated. We have successfully developed high-qualitgy Ge-on-Insulator (GOI) by using wafer bonding and splitting. We have also developed carrier-injection strained SiGe-based optical modulators with MZI interferometers and successfully demonstrated the enhanced plasma dispersion effect in SiGe. We have also investigated MOS based SiGe optical modulators. We have revealed the plasm post-nitridation can form high-quality SiGe MOS interface even on the (110) surface.

III-V CMOS photonics

S. Takagi, M. Takenaka, Y. Chen, Y. Ikku, J. Park, S. Takashima

High-performance electronic-photonic integrated circuits using III-V-OI wafer have been investigated. By using Si implantation and SOG Zn diffusion, we have formed low-resistance lateral PIN junction on the III-V-OI wafer. We have also demonstrated low-dark-current waveguide InGaAs photodetector on the III-V-OI wafer by using InAlAs passivation.

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