# Recent developments of CMOS pixel sensors and their applications to high energy physics experiments

## Terzo Incontro sulla fisica con ioni pesanti alle alte energie

Padova

November 25th - 26th, 2021

**Manuel Rolo (INFN)**


Istituto Nazionale di Fisica Nucleare

# Si Pixel sensors: where&when to start?...

ISSCC

FRIDAY, FEBRUARY 11, 1966 ... UNIVERSITY MUSEUM/UNIV. OF PENNSYLVANIA ... 1:30-4:30 P.M.

**SESSION XI: Digital Applications of Field-Effect Transistors**

**FPM 11.4: A Thin-Film Solid-State Image Sensor***

P. K. Weimer, G. Sadasiv, H. Borkan, L. Meray-Horvath, J. Meyer,

RCA Laboratories

Princeton, N. J.

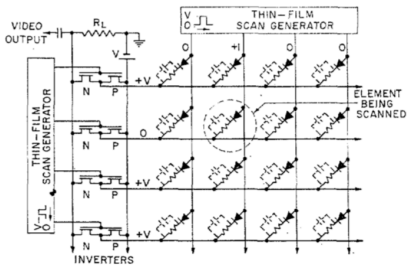



*FIGURE 6*—One method of coupling out the video signal from an array of photoconductor-diode elements. Alternatively, the complementary inverters can be replaced by a single column of transistors.

1965 International Electron Devices Meeting

**4.5 A MONOLITHIC MOSAIC OF PHOTON SENSORS FOR SOLID STATE IMAGING APPLICATIONS,** M. A. Schuster and G. Strull, Westinghouse Electric Corp., Baltimore, Md.

Monolithic silicon mosaics of photosensor elements have been developed for solid state imaging applications. The physical structure, design features, and performance characteristics of these electro-optical devices will be presented.

IEEE ELECTRON DEVICE LETTERS, VOL. EDL-1, NO. 9, SEPTEMBER, 1980

## Amorphous-Silicon Image Sensor IC

M. MATSUMURA, MEMBER, IEEE, H. HAYAMA, Y. NARA AND K. ISHIBASHI

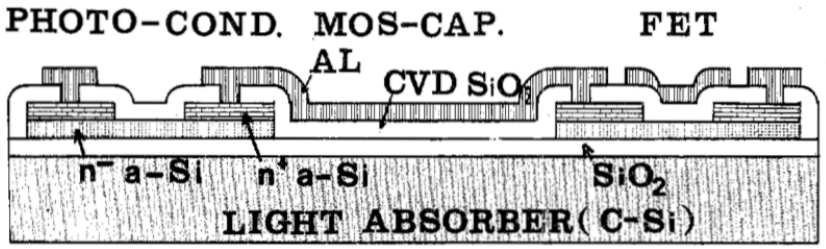



Figure 1. The unit cell structure of the proposed image sensor IC.

IEEE TRANSACTIONS ON PARTS, HYBRIDS, AND PACKAGING, VOL. PHP-10, NO. 3, SEPTEMBER 1974

## A Hybrid Integrated Silicon Diode Array for Visible Earth-Horizon Sensing

FRANK J. BACHNER, MEMBER, IEEE, RONALD A. COHEN, MEMBER, IEEE, ROBERT W. MOUNTAIN, WILLIAM H. MC GONAGLE, AND ARTHUR G. FOYT, MEMBER, IEEE

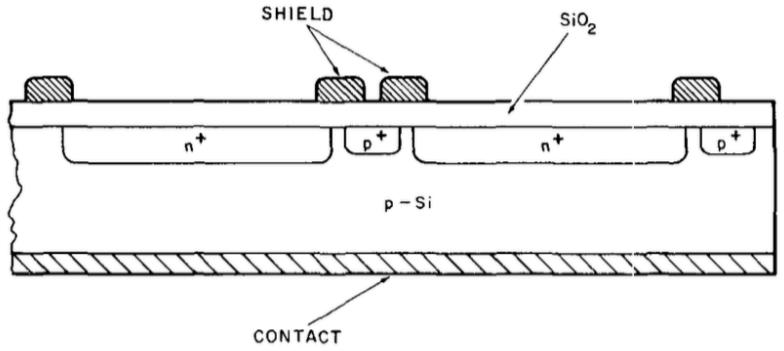
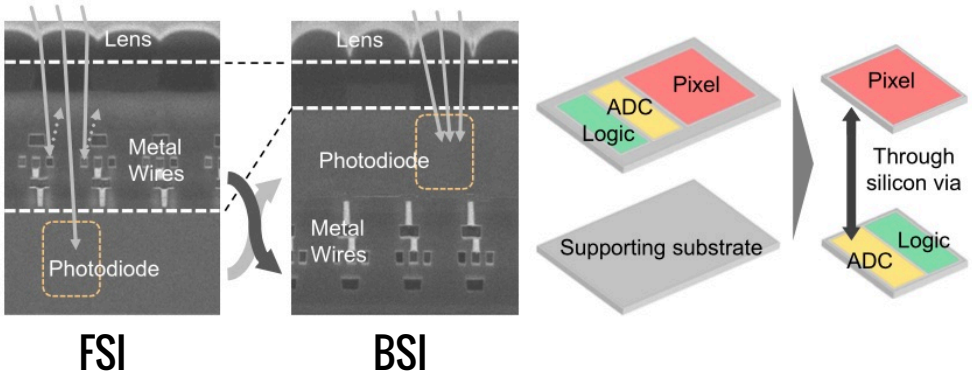
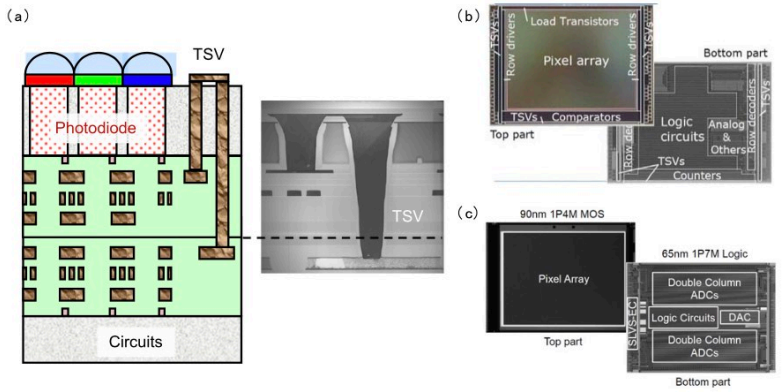



Fig. 2. Cross-section of a portion of an eight diode array showing the $n^+$ active region, the $p^+$ channel stop, the passivating oxide and the metal edge-shields.

# State of the Art on CMOS APS

- CMOS Active Pixel Sensor is today a mature technology and a steady leader in the image sensor market
- Front-side-illumination on state-of-the-art CMOS imager pixels O(1μm) limits light incidence
- BSI devices have BEOL below the photodiode region, avoiding reflection of the incident light
- Ramping up interest on 3D stacked sensors, using TSVs and employing vertical integration of sensor and readout&processing tiers
- Combination of BSI, 3D integration and CMOS deep sub-micron technologies should allow for 100% fill-factor, high-speed signal digitisation and processing on CMOS sensors

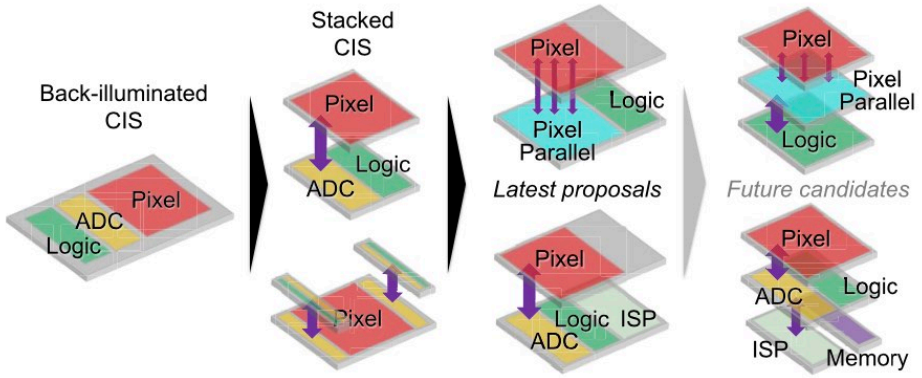


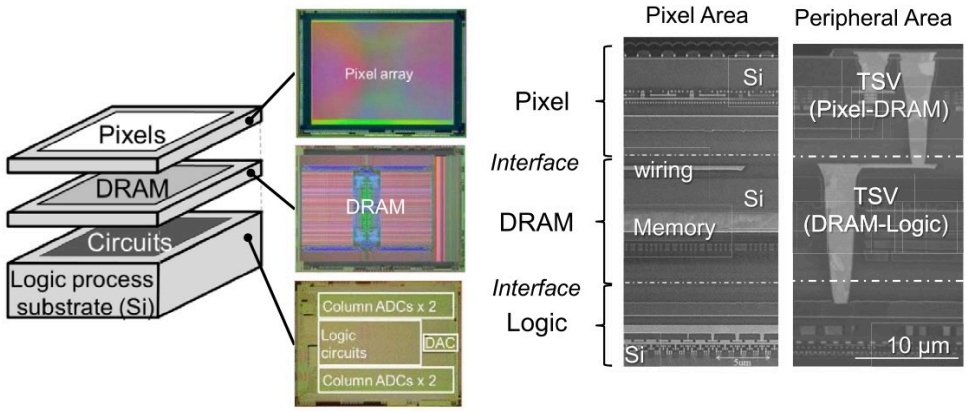

Y. Oike, "Evolution of Image Sensor Architectures With Stacked Device Technologies," in IEEE Transactions on Electron Devices, doi: 10.1109/TED.2021.3097983.

# Outlook for CMOS APS Imagers

- Innovation on image sensor integration technologies mostly driven by the need of higher frame rates and higher pixel resolutions
- Enabled by the use of stacked device structures employing optimised sensor process technologies and advanced CMOS nodes
- Notable recent achievements featuring "pixel-parallel stacked circuitry" and UDSM CMOS circuits with more intelligence on board of the processing units
- ✦ Pixel-pitch Cu–Cu connections, wafer-on-wafer (WoW) bonding or Chip-on-wafer (CoW) when readout circuitry is smaller than the optics,...




Y. Oike, "Evolution of Image Sensor Architectures With Stacked Device Technologies," in IEEE Transactions on Electron Devices, 2021




Y. Kagawa et al., "Novel stacked CMOS image sensor with advanced Cu2 Cu hybrid bonding," in IEDM Tech. Dig., Dec. 2016

(left) A. Jouve et al., "1µm Pitch direct hybrid bonding with <300nm wafer-to-wafer overlay accuracy", 2017 IEEE S3S Conf

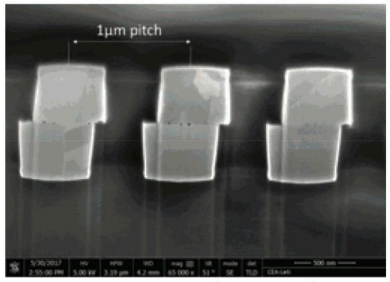



*Figure 5: FIB-SEM X-section of 1µm pitch copper pads after 400°C-2h annealing.*

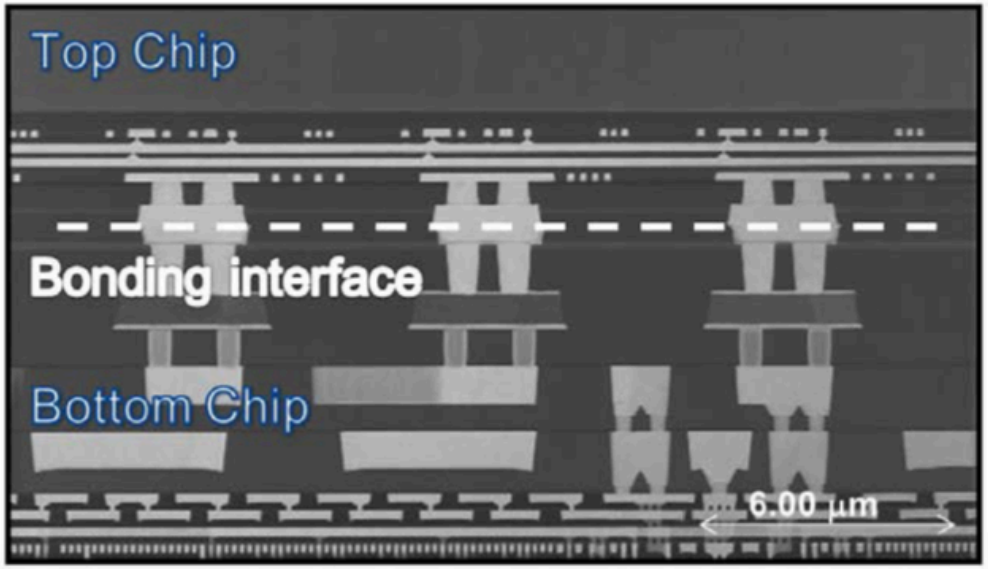
# On the definition of “Monolithic CMOS”

**ISSCC 2018 / SESSION 5 / IMAGE SENSORS / 5.1**

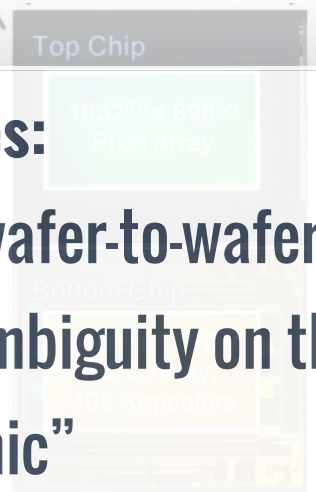
**5.1 A Back-Illuminated Global-Shutter CMOS Image Sensor with Pixel-Parallel 14b Subthreshold ADC**

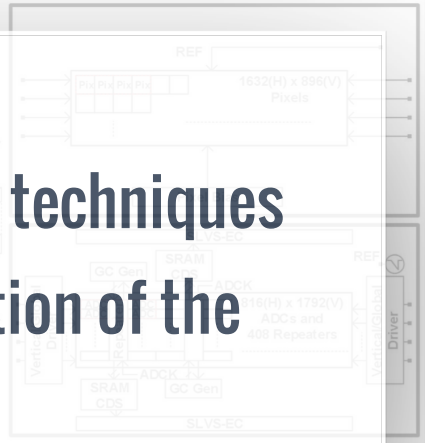

Masaki Sakakibara[1], Koji Ogawa[1], Shin Sakai[1], Yasuhisa Tochigi[1], Katsumi Honda[1], Hidekazu Kikuchi[1], Takuya Wada[1], Yasunobu Kamikubo[1], Tsukasa Miura[1], Masahiko Nakamizo[1], Naoki Jyo[2], Ryo Hayashibara[2], Yohei Furukawa[3], Shinya Miyata[3], Satoshi Yamamoto[1], Yoshiyuki Ota[1], Hirotsugu Takahashi[1], Tadayuki Taura[1], Yusuke Oike[1], Keiji Tatani[1], Takashi Nagano[1], Takayuki Ezaki[1], Teruo Hirayama[1]

[1]Sony Semiconductor Solutions, Atsugi, Japan
[2]Sony Semiconductor Manufacturing, Kumamoto, Japan
[3]Sony LSI Design, Fukuoka, Japan


| Item | Data |
|---|---|
| Process | CIS wafer: 90nm 1 Poly 4 Metal Layer |
| | Logic wafer: 65nm 1 Poly 7 Metal Layer |
| Supply Voltage | 2.8 [V] / 1.1 [V] |
| Num. of pixels | 1632(H) x 896(V) |
| Max frame rate | 660 [fps] |
| Saturation signal | 16.6k [e-] |
| PLS | -75 [dB] |
| Conversion gain | 60 [µV/e-] |
| Power consumption | 654 [mW] 746 [mW] |
| Dynamic range | 65.7 [dB] 70.2 [dB] |
| ADC resolution | 14 [bit] |



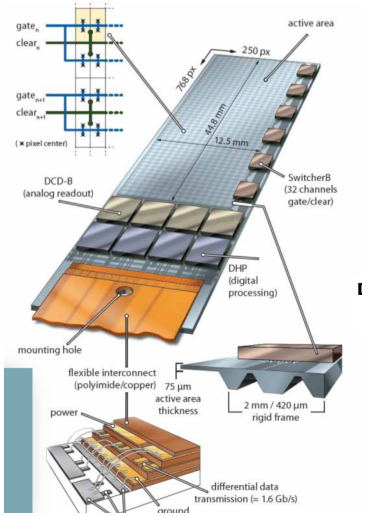
**Disclaimer for the next slides:**

**The availability of advanced wafer-to-wafer bonding techniques will inevitably lead to some ambiguity on the definition of the terms “hybrid” and “monolithic”**

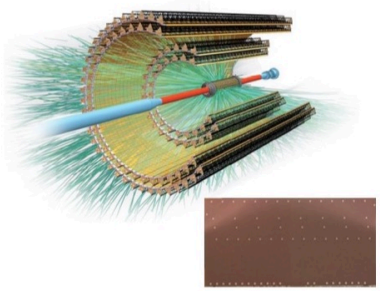
# Monolithic Active Pixel Sensors

- **Sensor and Readout Electronics share the same wafer**
- Enabling technology for low material budget and/or very low power space applications, frontier detectors for particle physics
- Embedded electronics, less components and connectors: Lower cost and increased reliability on assembly and production of detectors:
  - no need for costly fine-pitched flip-chip assembly
  - less (failing) connectors and lower material budget
  - cost reduction for large productions (use of a commercial CMOS foundry): increased die-per-wafer and reduced cost per device

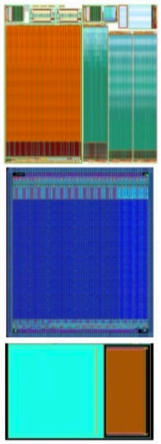
# MAPS: The Evolution of the Species




ULTIMATE in STAR
IPHC Strasbourg
First HEP MAPS system

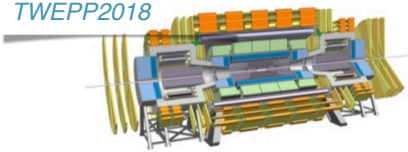


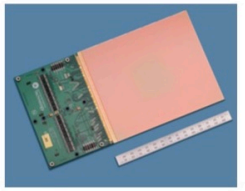
ALPIDE in ALICE
First MAPS with sparse readout
similar to hybrid sensors
Chip-to-chip communication
for data aggregation



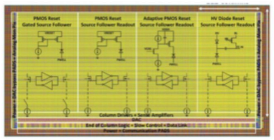
ATLAS CMOS
Depleted radiation hard
MAPS with:
Sparse readout
Chip-to-chip
communication
Serial power
...

*Partially adapted from:*
*W. Snoeys, TWEPP2018*



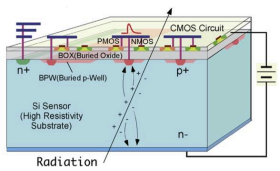


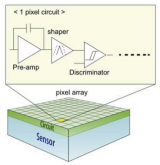
FCC, CLIC, ...
Large stitched fast radiation hard MAPS with:
Sparse readout
Chip-to-chip communication
Serial power

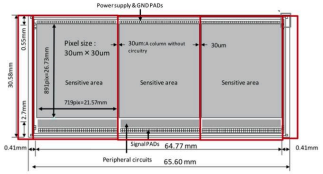


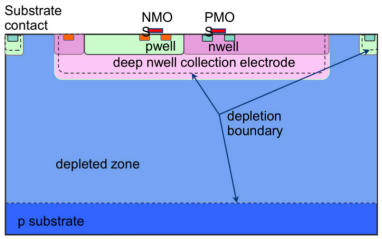
TJ-Monopix: 20 x 10 mm

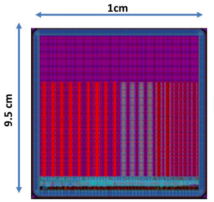

MALTA: 20 x 20 mm



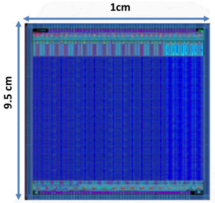



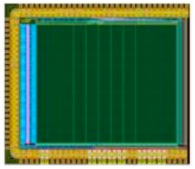



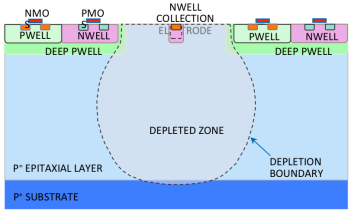

LF-CPIX (Demonstrator)



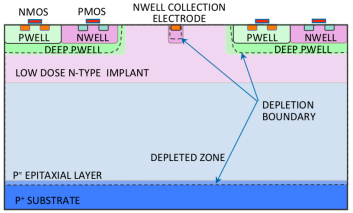

LF-Monopix (monolithic FE-I4)



JadePix2 (IHEP)
3 × 3.3 mm²




Standard: no full depletion

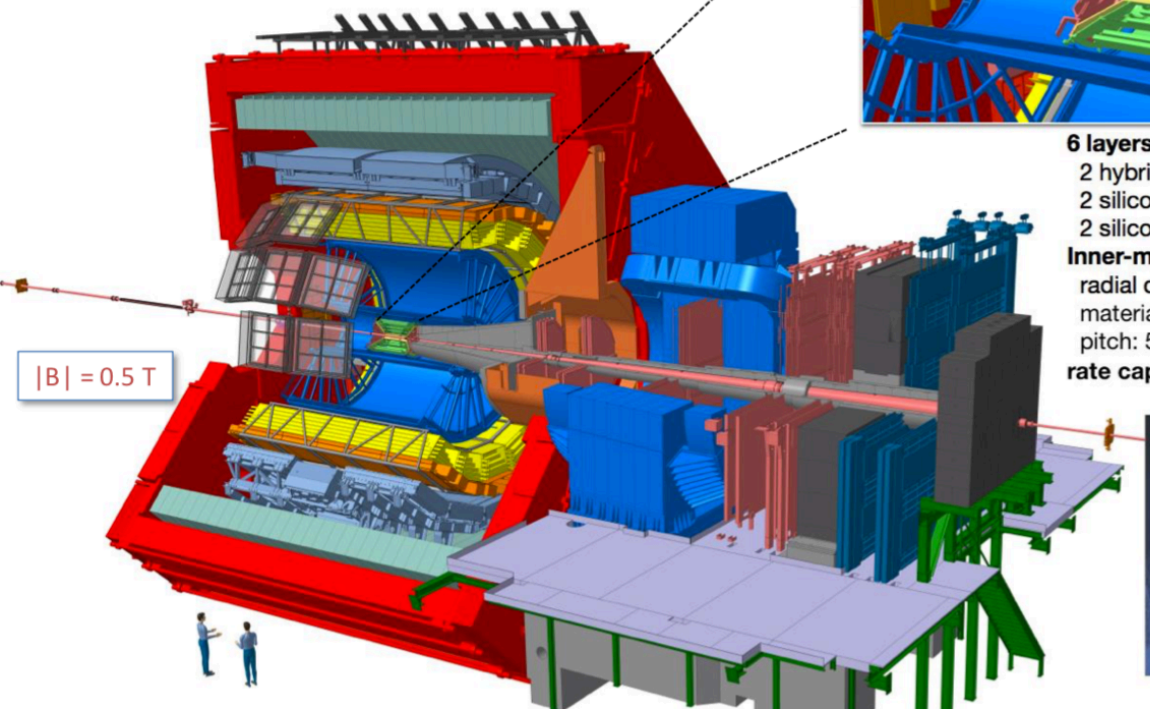


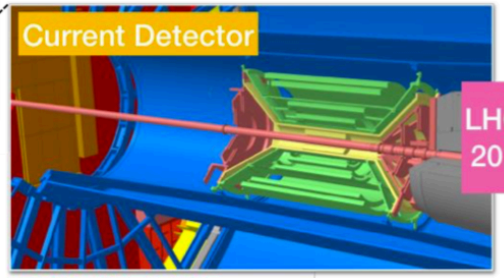

Modified: full depletion, better radiation tolerance

# CMOS sensors for ALICE Inner Tracker

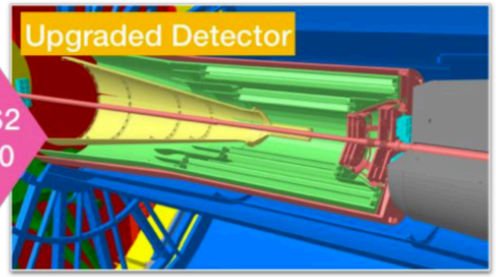
New Inner Tracking System (ITS)
- CMOS Pixels

→ improved resolution, less material, faster readout




LHC LS2
2019/20




**6 layers:**
2 hybrid silicon pixel
2 silicon drift
2 silicon strip

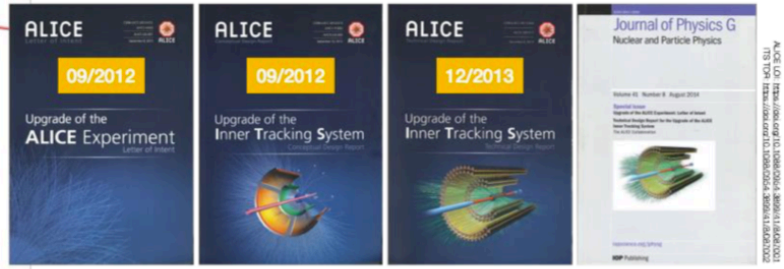
**Inner-most layer:**
radial distance: 39 mm
material: $X/X_0 = 1.14\%$
pitch: $50 \times 425\ \mu m^2$

**rate capability:** 1 kHz

**7 layers:**
all Monolithic Active Pixel Sensors

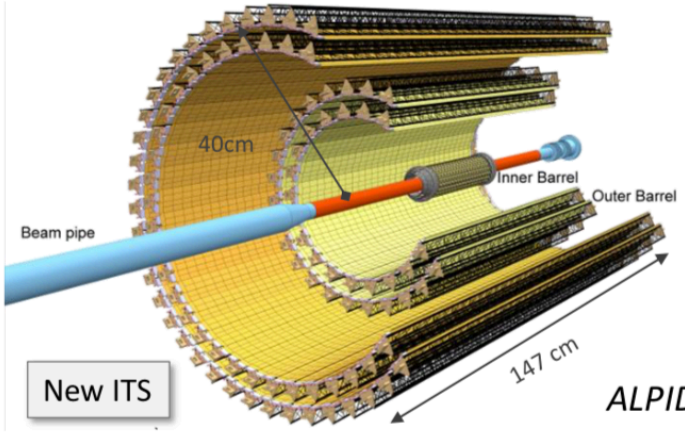
**Inner-most layer:**
radial distance: 23 mm
material: $X/X_0 = 0.3\%$
pitch: $O(30 \times 30\ \mu m^2)$

**rate capability:** 100 kHz (Pb-Pb)




L. Musa – EIROforum, Topical Workshop, CERN, May 2018

# ALPIDE Chip - applications beyond ALICE




Closer to IP: 39mm ➡ 22mm

Thinner: ~1.14% ➡ ~ 0.3% (for inner layers)

Smaller pixels: 50μm x 425μm ➡ 27μm x 29μm

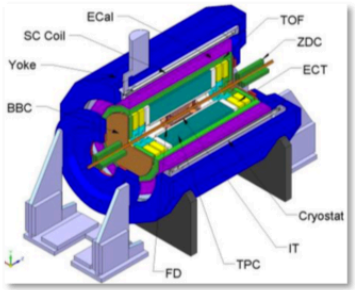
Increase granularity (x $10^3$): 20 chan/$cm^3$ ➡ 2k pixel/$cm^3$

10 $m^2$ active silicon area: 12.5 G-pixels, $\sigma \approx 5\mu m$

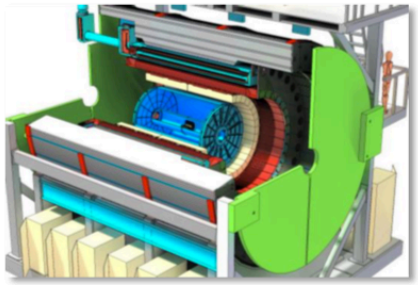
$1.5 \leq \eta \leq 1.5$

*ALPIDE (**ALICE Pixel Detector**) - Developed for the ALICE upgrade (ITS and MFT) will be used (or it is proposed) for several other HEP detectors and non HEP applications*

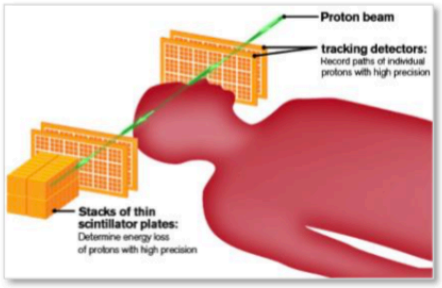
NICA MPD (@JINR)



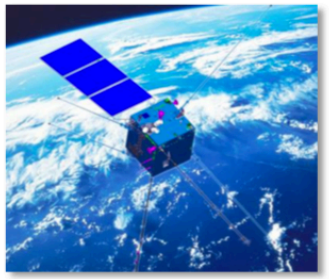

sPHENIX (BNL)



proton CT (tracking)



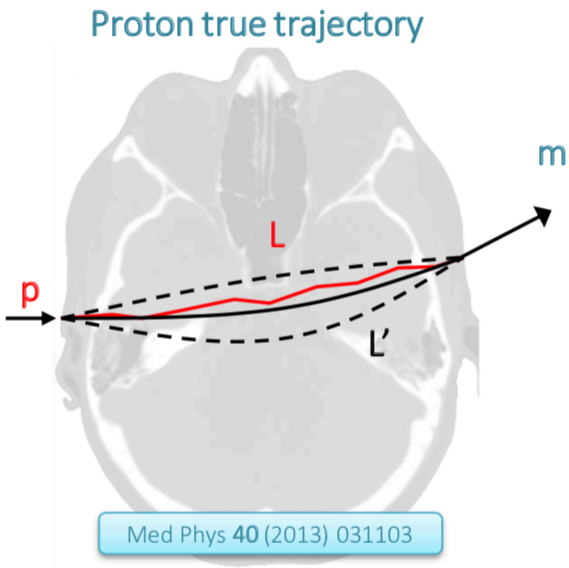

CSES – HEPD2 ...



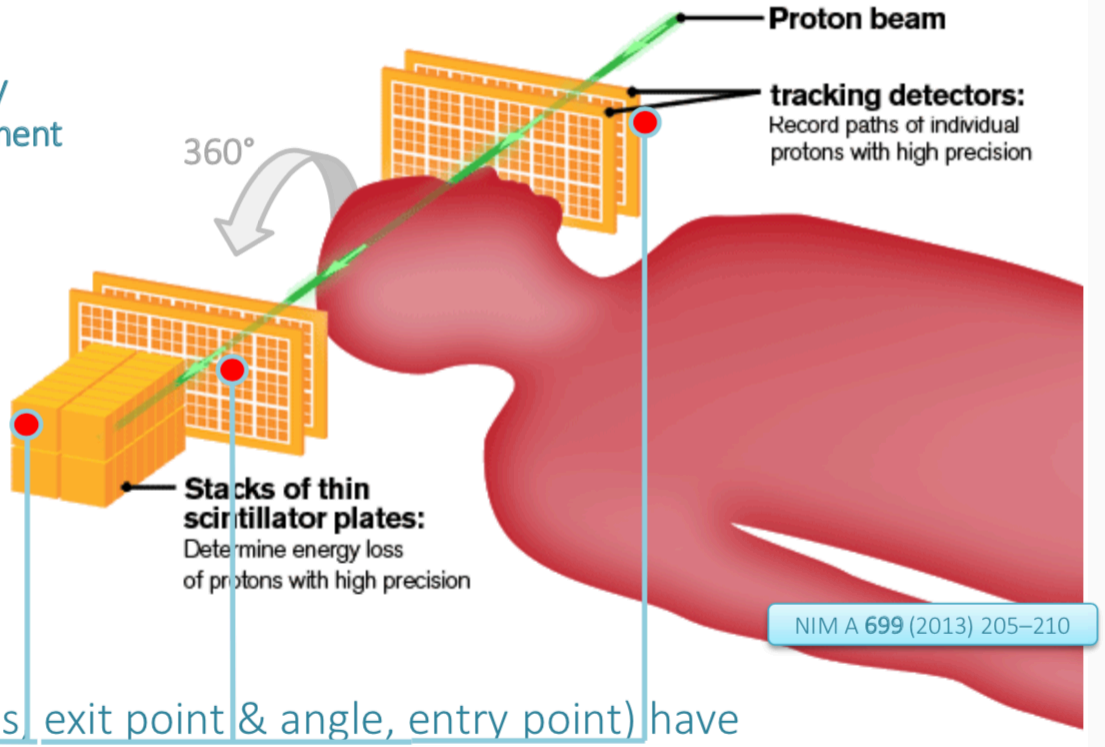
L. Musa – EIROforum, Topical Workshop, CERN, May 2018

# MAPS for Medical Applications

The pCT works on the same principle as a "standard" x-rays CT: recording particles passing through the target from different angles to reconstruct a 3D image. Main difference is that, while photons are simply absorbed, protons also scatters.




Entry and exit points + angle
Most Likely Path calculation

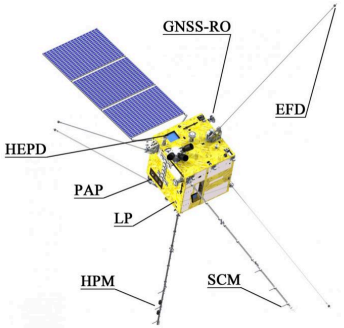


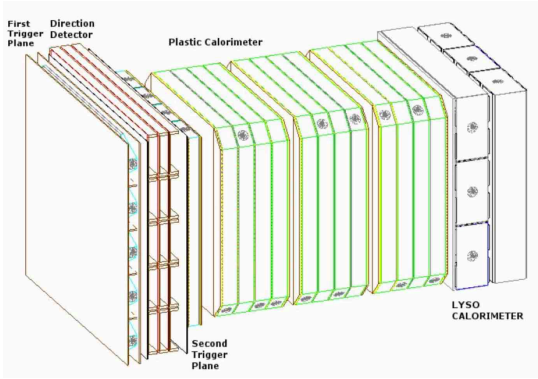

At least $10^9$ proton tracks (energy loss, exit point & angle, entry point) have to be recorded to provide a detailed enough image. This leads to long exposure time (10s minutes) with current state of the art: limited to R&D only.

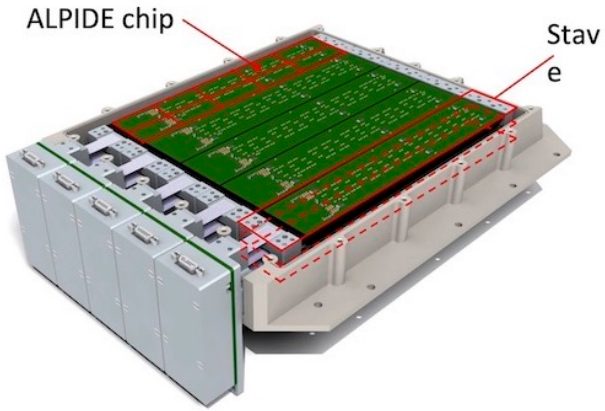
courtesy slide from Piero Giubilato: ERC iMPACT

# ALPIDE chip for space applications

- direction detector DD ("tracker") of the High Energy Particle Detector (HEPD-02) will be onboard of the China Seismo-Electromagnetic CSES-02 satellite (launch scheduled to 2022)
- 5 triple-stacked-stave turrets, stave mounts 10 ALPIDE (50μm)
- Low-power strategy: control line instead of high speed data link for readout and regional clock-gating at system level
- The HEPD-02 silicon tracker will become the **first use case of MAPS technology in space instruments**!

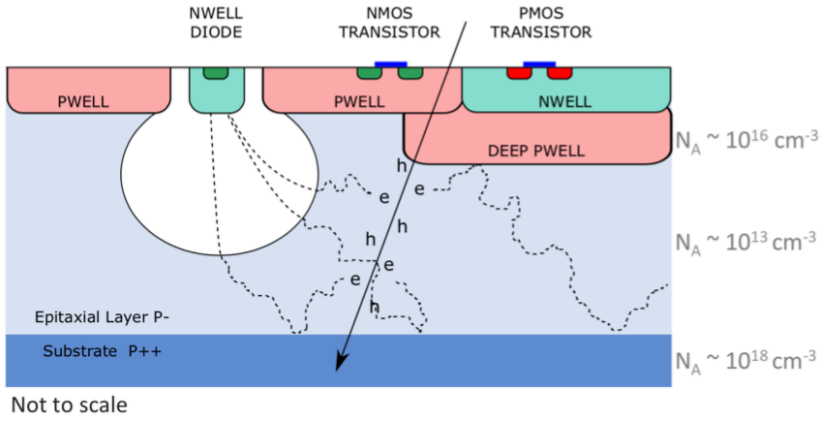


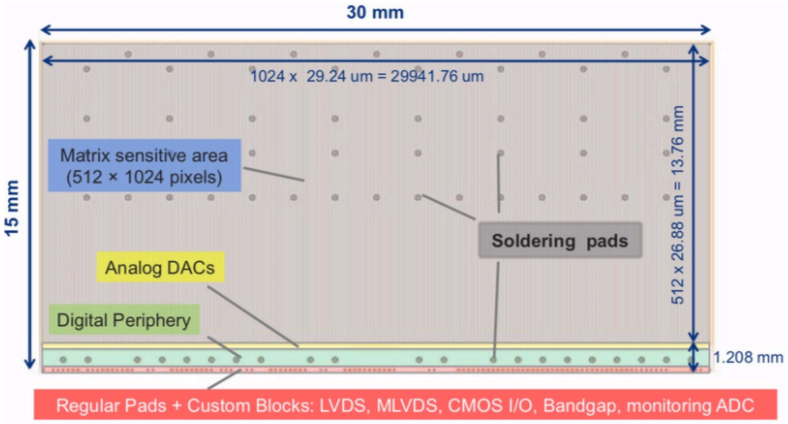




P Zuccon, iWoRiD2021

# The ALPIDE (ALICE Pixel Detector) Sensor

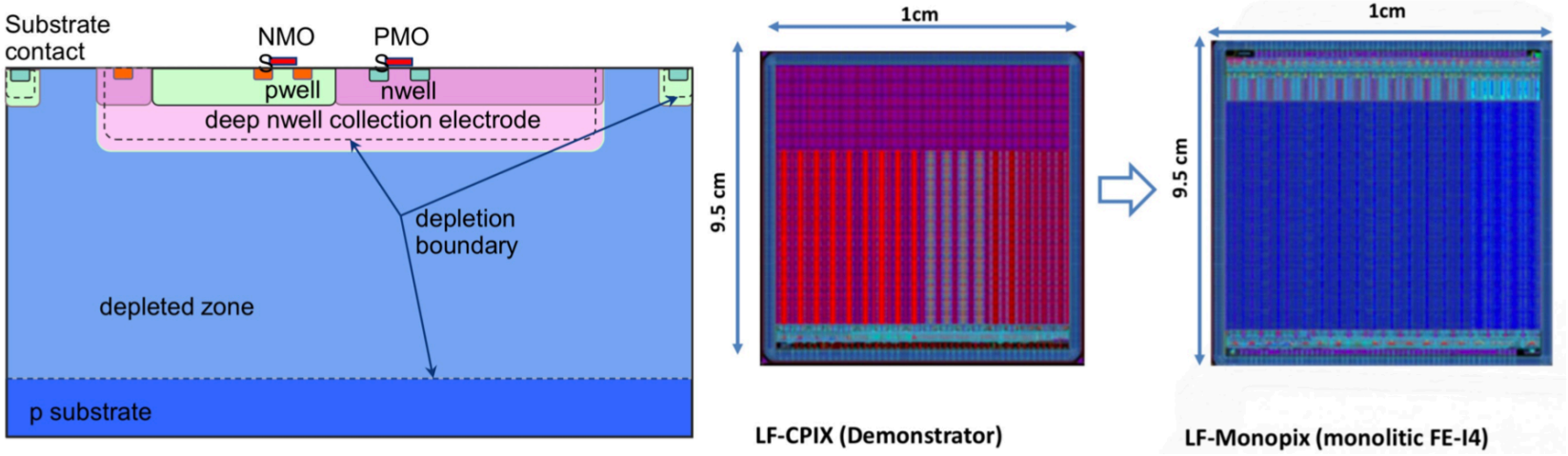



- 180nm TJ CMOS imaging sensor process
- System-grade large scale monolithic sensors with sparse readout
- charge collection by diffusion only - slow signals, unfit for O(ns) timing; sensitive to bulk damage due to collection time
- reverse bias increases depletion volume, sensor is not fully depleted

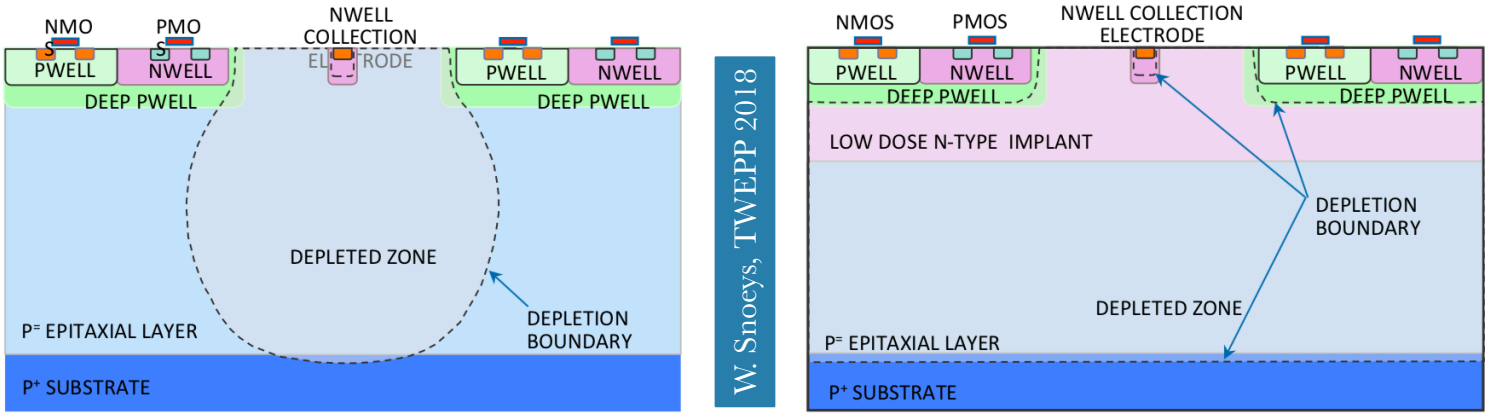
☑ Best in class in terms of system readiness!

# Depleted MAPS, large CE (HV-CMOS)




- e.g. ATLASpix, LF-Monopix, Coolpix, LF2
- Charge is collected by drift - faster signals!
- Uniform electric field and very good radiation tolerance (1E15 $n_{eq}/cm^2$)
- readout circuitry inside the collection electrode degrades input capacitance and hence SNR
- large CE: analog power, sensitivity to coupling of signals
- Initially proposed for ALTAS outer pixel layer Phase 2

# Depleted MAPS with small CE

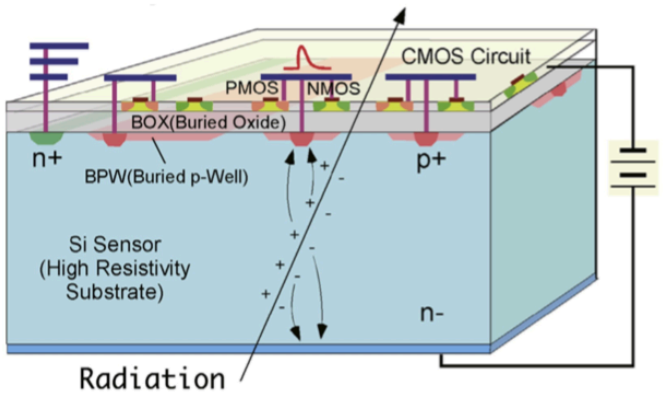


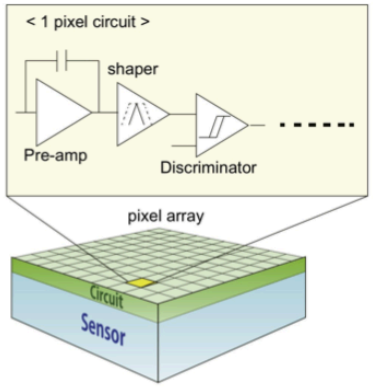

Standard: no full depletion

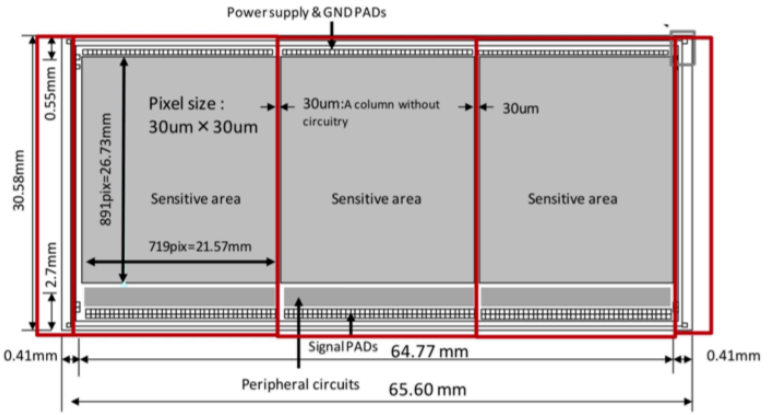
Modified: full depletion, better radiation tolerance

- TJ180nm Investigator Sensor (ALICE) test chip, above 97% eff; 134 pixel sub-matrices of different designs (electrode size, PWELL spacing)
- use of a n-type layer to improve depletion under deep PWELL → better radiation tolerance (Investigator irradiated up to 1E15 $n_{eq}/cm^2$ and 1 Mrad in several steps) and charge collection by drift
- small collection electrode: low capacitance, low power, better isolation electrode/circuit
- depletion depth limited to the epi-layer (about 25 μm)
- Design of two full-scale demonstrators to match ATLAS specifications for outer pixel layers: TJ MALTA (2018) 20 x 22 $mm^2$ and TJ MonoPix (2018) 20 x 10 $mm^2$

# Silicon on Insulator (e.g. PIXOR, SOPHIAS)



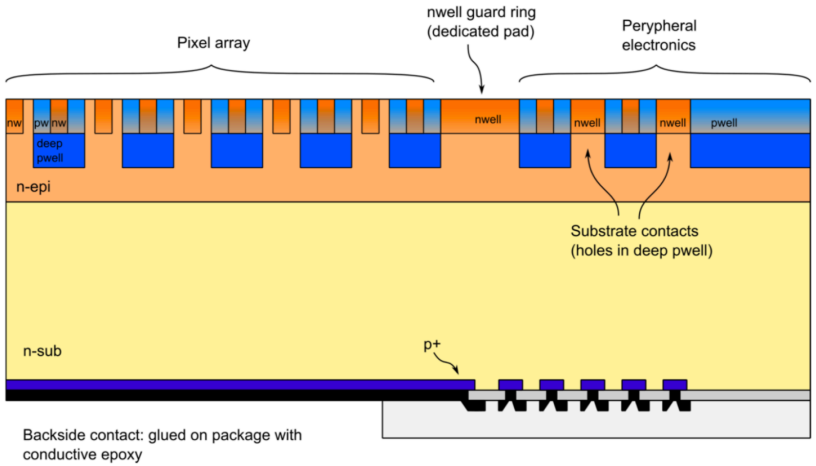

- buried oxide separates silicon layer (front-end circuit) and sensor on high resistivity substrate
- BOX is fairly thick and this increases the sensitivity to the damage caused by ionizing radiation
- high radiation tolerance, large depletion volume
- back-gate effect (causes shift on FET $V_{th}$) solved with Buried P-Well (BPW), but pixel capacitance increases
- SOI wafers cost, single vendor, wafer capability for volume?

# ARCADIA (INFN CSNV Call Project)

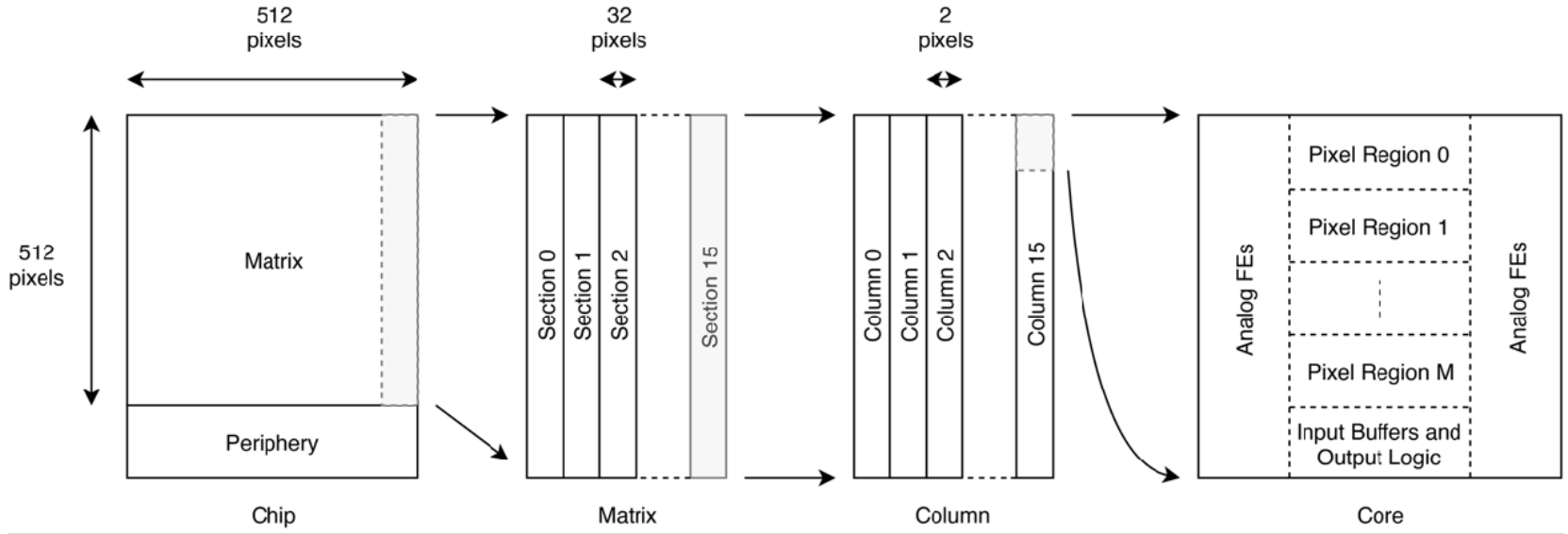
## Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

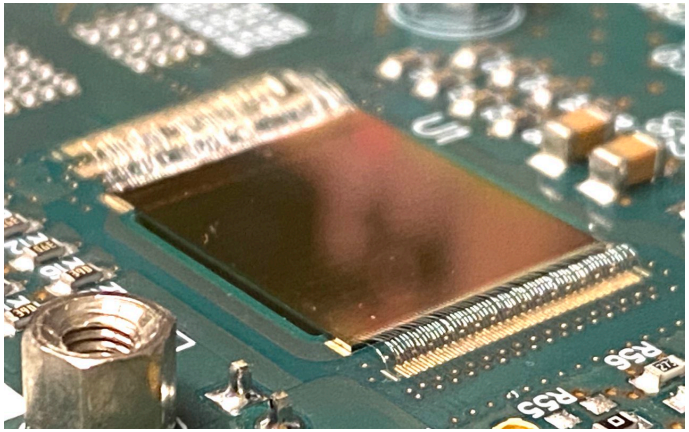
**Creation of a novel platform for the implementation of innovative monolithic sensors compatible with standard CMOS fabrication processes**

- Challenge: deployment of large-area system-grade CMOS sensors implementing scalable readout architectures with ultra-low power capability O(20 mW/cm$^2$)
- Technology: LFoundry 110nm CMOS node, quad-well, high-resistivity bulk
- Active sensor thickness in the range 50 µm to 500 µm
- Operation in full depletion with fast charge collection only by drift, small CE for optimal SNR



# ARCADIA-MD1: Main Demonstrator Chip



- Pixel size 25 µm x 25 µm, Matrix core 512 x 512, 1.28 x 1.28 $cm^2$
- Triggerless binary data readout, event rate up to 100 $MHz/cm^2$
- **First Engineering Run** (SPW) 11/2020, **silicon being tested**
- **2nd full CMOS maskset** mid-2021, fab out expected January 2022
- **3rd SPW mid-2022** with design fixes, explorative sensor and CMOS designs, new architectures with higher data throughput, full chip demonstrator for fast timing (R&D on sensors and electronics already started with 2nd SPW)

# CMOS Embedded Si-strip and readout

- Design and Production of continuous and “pixelised” strips, range 10 - 100µm pitch
- Proof-of-concept: **CMOS monolithic strip block and readout electronics**

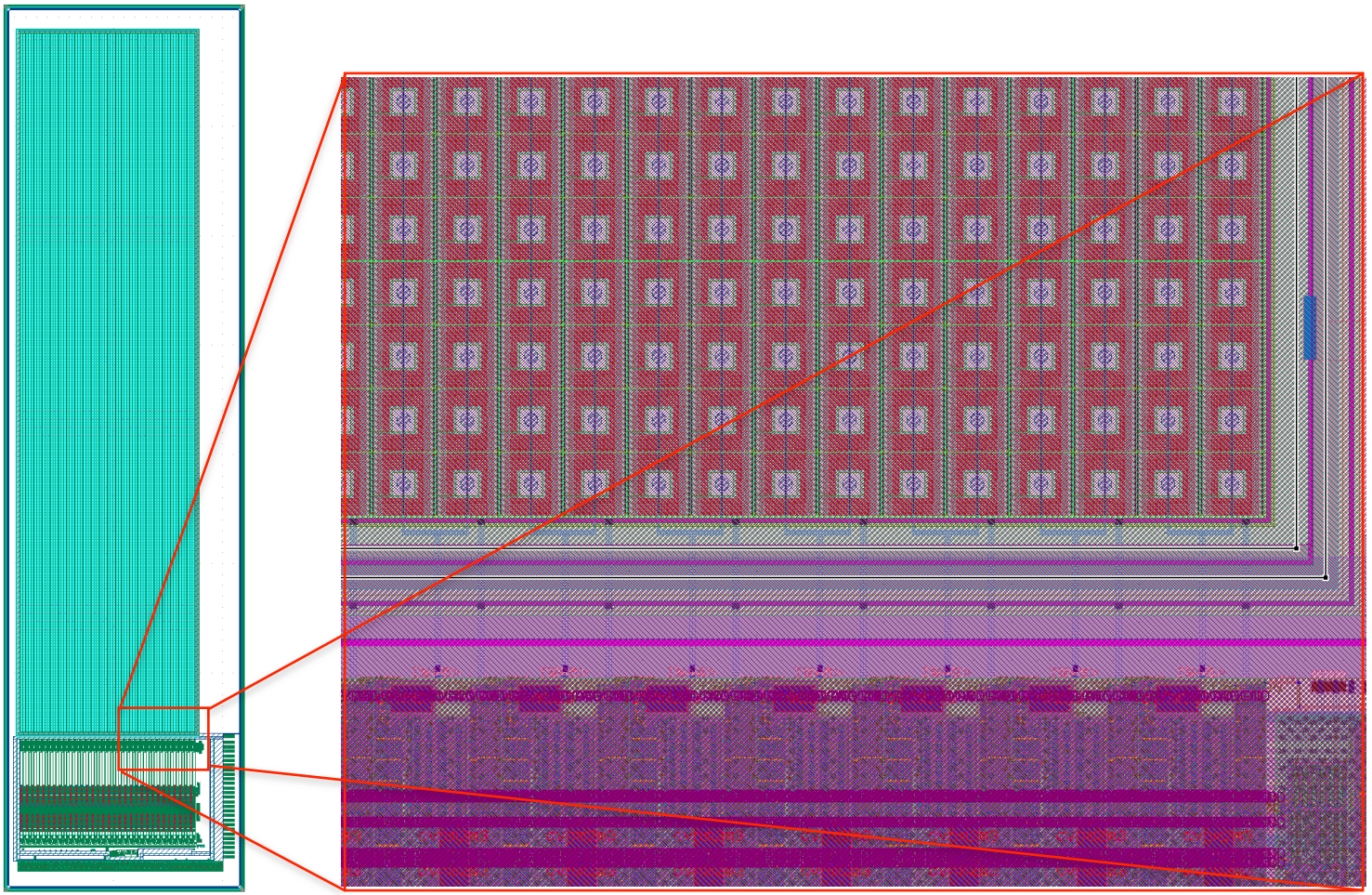


Figure: CAD Layout of 2x32x50µm pixelised strips

Figure: (top) detail of 2x32x50µm pixelised strips and (bottom) 32-channel custom readout

# Depleted MAPS for Future Detectors

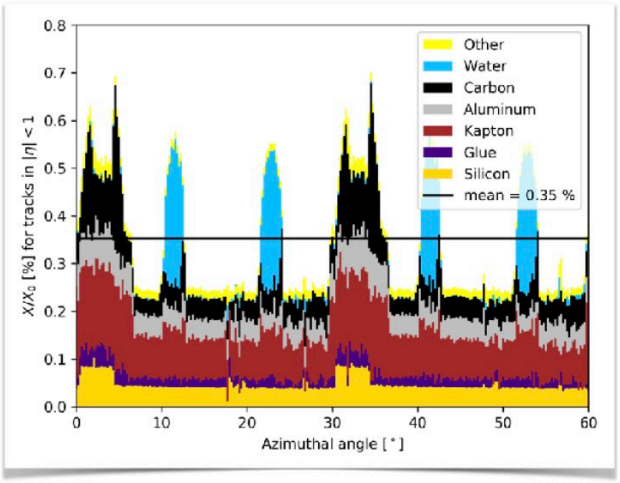
| | RHIC STAR | LHC - ALICE ITS | CLIC | HL-LHC Outer Pixel | HL-LHC Inner Pixel | FCC pp |
|---|---|---|---|---|---|---|
| NIEL [$n_{eq}/cm^2$] | $10^{12}$ | $10^{13}$ | $<10^{12}$ | $10^{15}$ | $10^{16}$ | $10^{15}$-$10^{17}$ |
| TID | 0.2Mrad | <3Mrad | <1Mrad | 80 Mrad | 2x500Mrad | >1Grad |
| Hit rate [$MHz/cm^2$] | 0.4 | 10 | <0.3 | 100-200 | 2000 | 200-20000 |

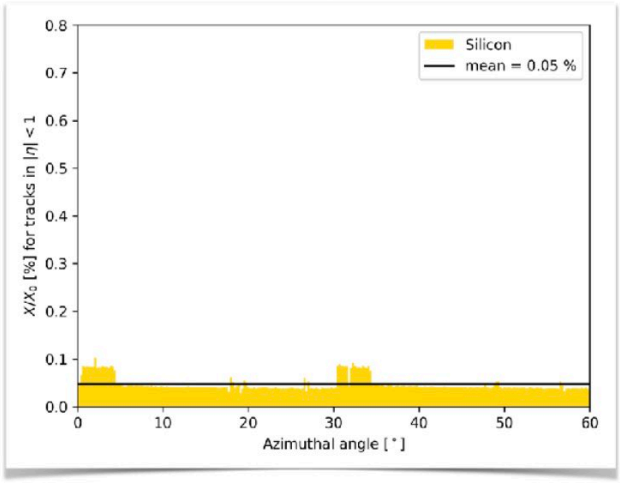
Heinz Pernegger, Vertex 2018

- **Hit rate and radiation hardness for Frontier Detectors could require improvements of ~2 orders of magnitude in respect to the state-of-the-art technology**

- Charge collection by drift: faster signals, better radiation hardness
- New architectures for higher event rate capability
- Advanced integration and interconnect technology for large sensor area and lightweight modules

# Trending up: go "green"




courtesy slide from Magnus Mager

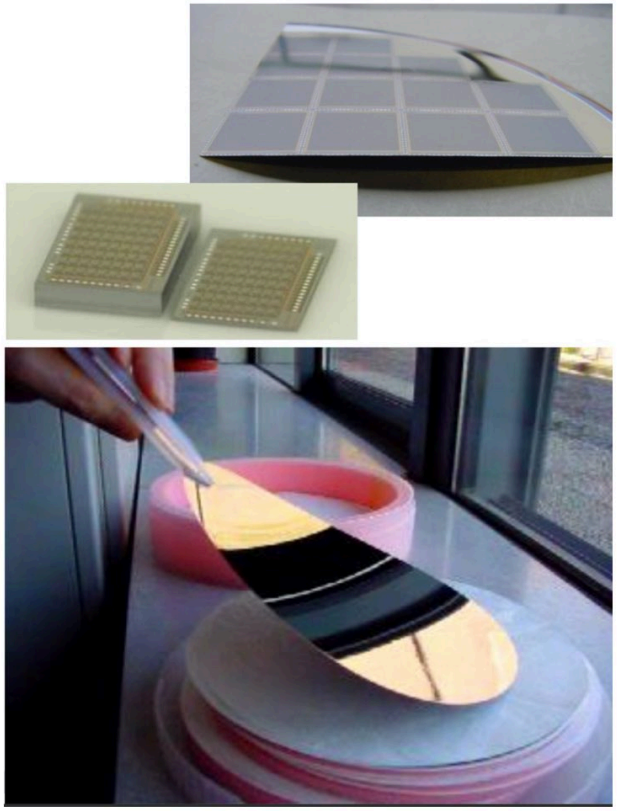
- Observations:
  - Si makes only **1/7th** of total material
  - **irregularities** due to support/cooling
- Removal of water cooling
  - **possible** if power consumption stays below 20 mW/cm²
- Removal of the circuit board (power+data)
  - **possible** if integrated on chip
- Removal of mechanical support
  - **benefit** from increased stiffness by rolling Si wafers

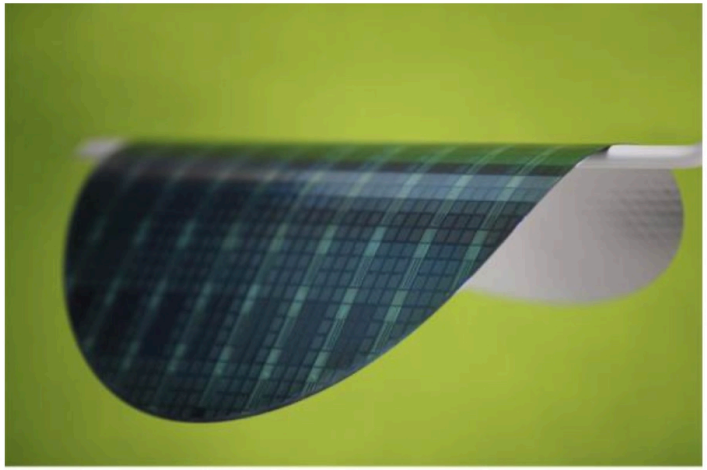
* Power requirement needs to be lowered to O(20mW/cm²)

# Trending up: Thinner Silicon

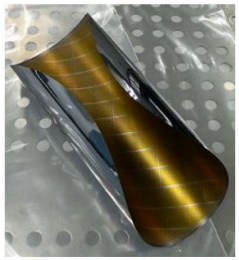
- Technology:
  - Course + fine grinding
  - Critical: thinning damage, impact on devices
- Wafer handling:
  - Very thin wafers (< 100 um): use of carrier wafers and temporary wafer (de-)bonding technology
- IMEC results:
  - Thinning down to 15 um
  - Total thickness variation ~ 2 um on 200 mm wafer

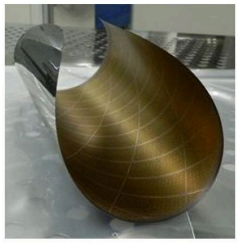
*P. De Moor (IMEC)*

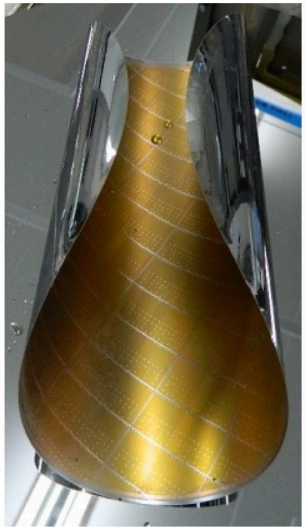




50 µm thin 300 mm Silicon Interposer Wafer with Cu-RDL metallisation. Source: Fraunhofer IZM







* **Wafer-scale ultra-thin (< 20 µm) stitched MAPS could bend into a cylindrical mechanically stable self-supporting shape:**

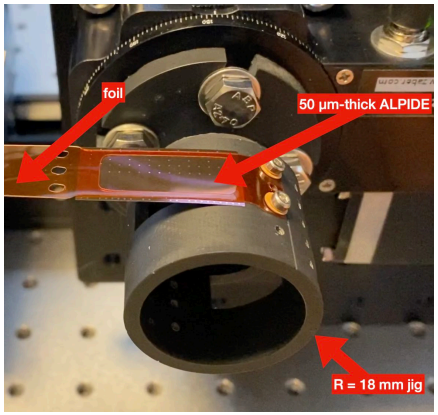
☑ purely Si based collider detector for tracking and PID with a VERTEX with an unprecedented low material budget of < 0.05 % $X_0$ per layer

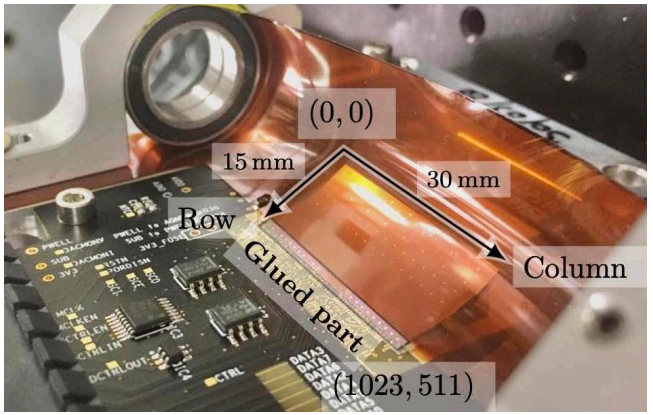
# Wafer Thinning, applied to MAPS

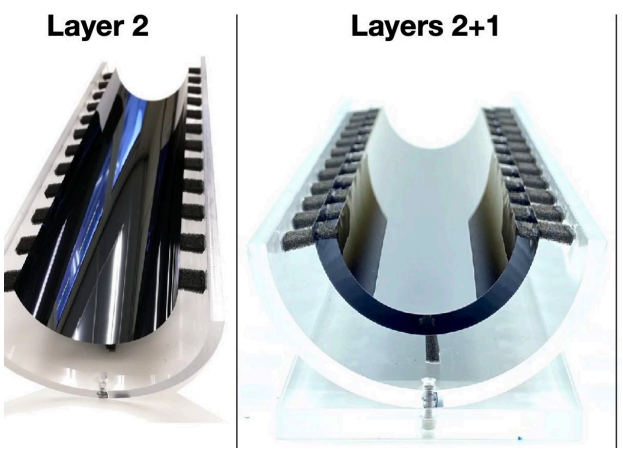
or… µITS3, i.e. 6 ALPIDEs at ITS3 radii

**ALICE ITS3 working group demonstrated the bending, operation and performance of thinned MAPS, using 1.5 cm × 3 cm ALPIDE chips, and system studies towards the integration of wafer-scale sensors**

- bent to radii of about 2cm without any signs of mechanical or electrical damage
- characterisation using a 5.4 GeV electron beam, detection efficiencies above 99.9 % at typical operating conditions
- 3-layer integration successful using 50 µm dummy Silicon



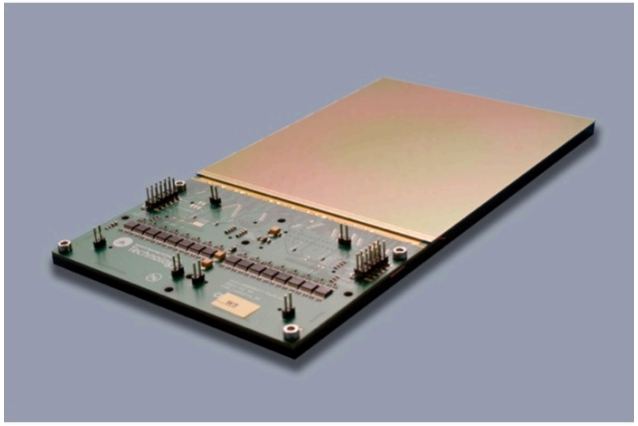



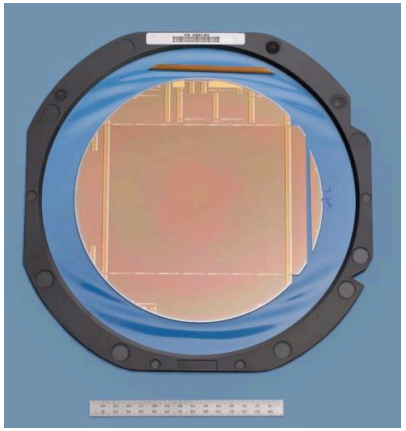



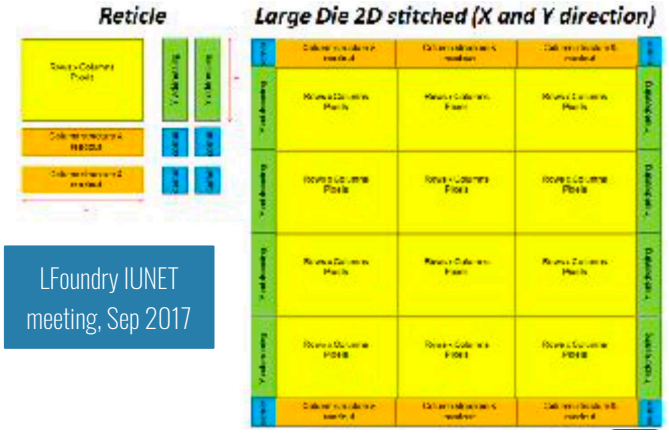

Magnus Mager CEPC2021

arxiv:2105.13000 "First demonstration of in-beam performance of bent Monolithic Active Pixel Sensors"

# Trending up: Bigger, Stitched Silicon





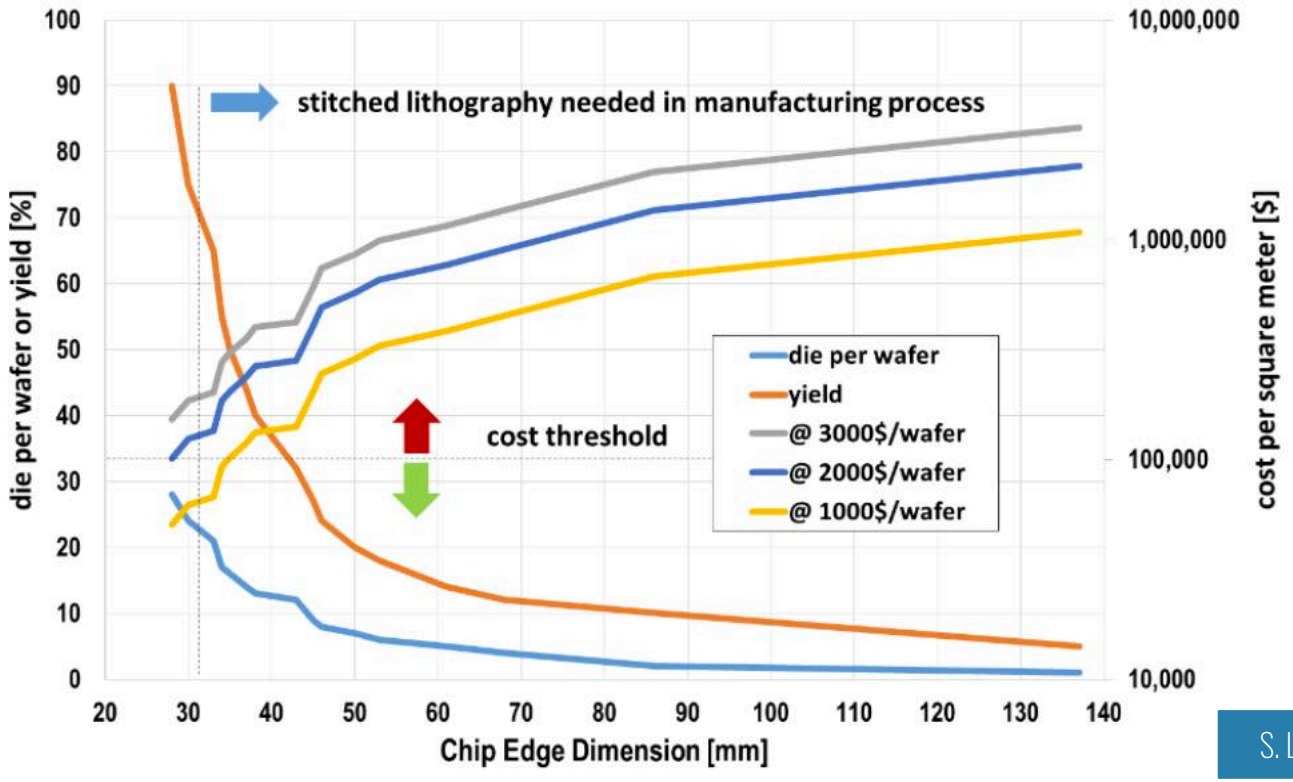



LFoundry IUNET meeting, Sep 2017

- (left) **Example of a wafer-scale imaging sensor chip for X-Ray applications developed at RAL (UK)**
- **139 x 120 mm CIS, Towerjazz 180nm on 200 mm (8'') wafers, 1 sensor per wafer**

- 2D Stitching paves the way for all-silicon CMOS monolithic APS as active interposers: substrate handles signal, power and data interconnects, enabling the development of ultra-low material budget trackers;
- particularly interesting assuming 12" wafers, very low power (no water cooling) and no mechanical support for an only-silicon inner tracker in future HEP colliders. Different considerations may apply for an outer Si-tracker…

# Cost and Yield considerations (my favourite slide on)




S. Lauxtermann, PIXEL2018

**Cost of $100,000/m² tracking area is achievable with the following assumptions**

- **> 75% Yield**
- **No stitching**
- **Wafer cost <$2,000 (only achievable using high volume CMOS manufacturing)**

# Summary and Outlook

- **Monolithic active pixel sensors** are now ubiquitous in **HEP** trackers and are making their inception into (low-power) **space**, (high-rate) **medical** applications. Cost effective reticle scale sensors could also lead their way into homeland security large area detectors
- CMOS Depleted monolithic pixel (and strip) sensors are now a strong candidate both for future low material budget silicon trackers and for timing layers, with investment and R&D mostly focusing on:
  - very low-power architectures O (20 mW/cm$^2$)
  - process engineering for better time resolution O (100 ps) or better
  - larger and thinner chips towards all/only-silicon inner trackers
- We need to foster access to advanced technologies and foundries, and make a good use of the most advanced integration and industry standard wafer stacking/bonding techniques

# Thank you for listening!


Istituto Nazionale di Fisica Nucleare

Manuel Rolo (INFN)

Recent developments of CMOS pixel sensors
and their applications to high energy physics experiments

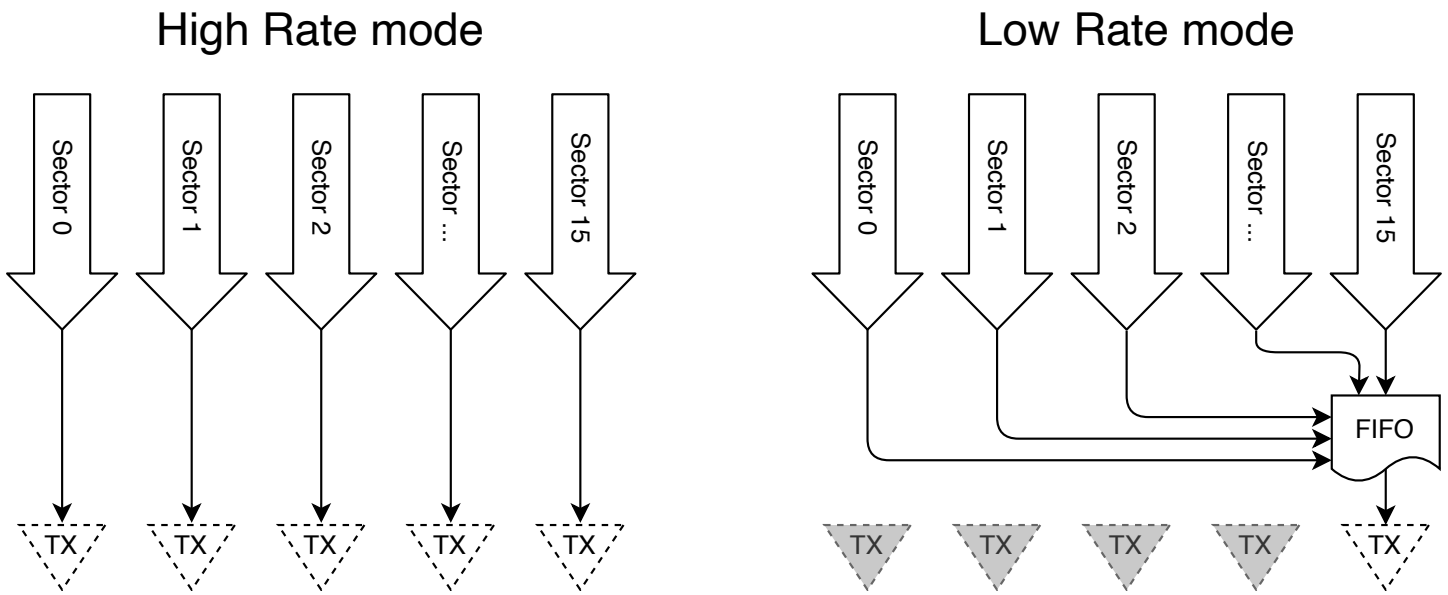
Terzo Incontro sulla fisica con ioni pesanti alle alte energie

Padova

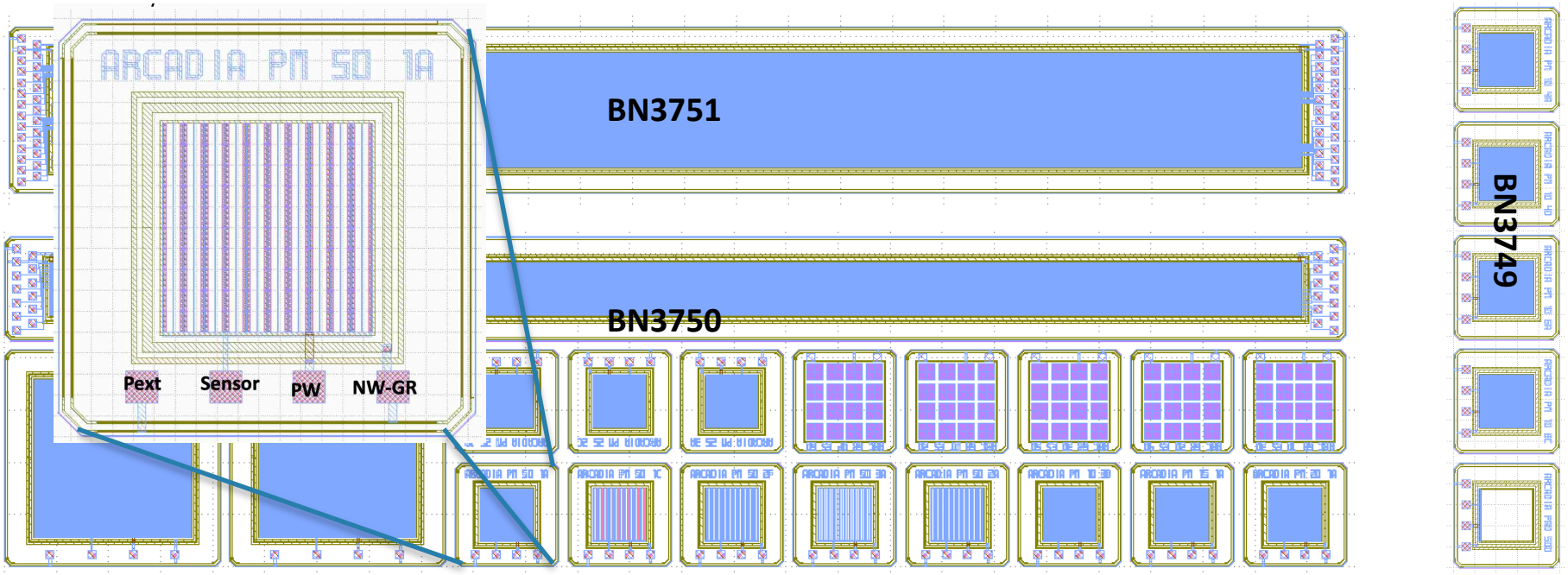
November 25th - 26th, 2021

# ARCADIA-MD1 - Peripheral Dataflow

- Each Column (32x512 pixels) has a readout BW of 443Mbps
- Sector data is sent out (8b10b encoded) via dedicated 320MHz DDR Serialisers
- In Low Rate Mode, the first serialiser processes data from all the sections. The other serialisers and C-LVDS TXs are powered off in order to reduce power consumption.



# ARCADIA Pixel/Strip Test Structures

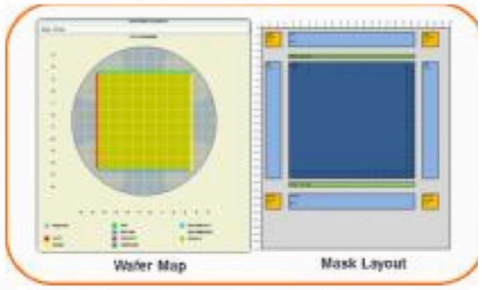



- **strips come in different flavours:**
  - 25 μm pitch pixelated + 25 μm continuous (10+10) [2 variants]
  - 10 μm pixelated (4 groups of 12 strips connected to pads) [4 variants]

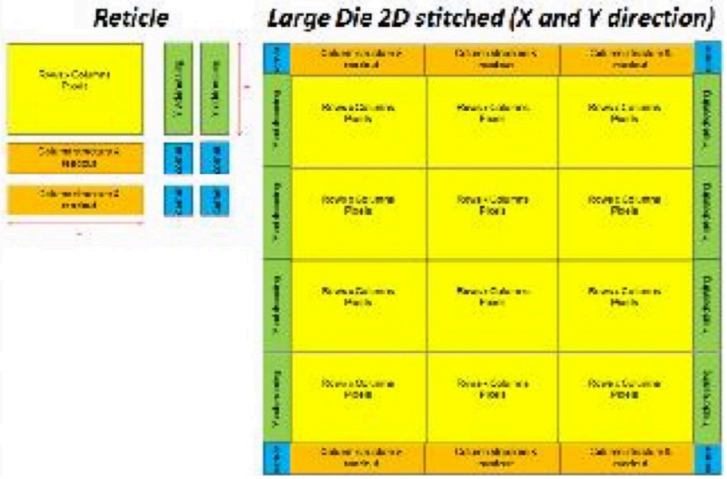
- **and pixels as well:**
  - Pseudo-Matrices of 1x1 and 2x2 $mm^2$
  - 50 μm (5 variants)
  - 25 μm (3 variants)
  - 10 μm (6 variants)

# 2D Stitching

- Need for image sensor sensors with larger size than the field of a semiconductor lithography equipment is not new
- However the challenge is the need of customized solutions for the wide field of different applications i.e.
  - 1D Stitching in low complexity (non CMOS) optical sensors (PDs) for large panels and thus interaction with final assembly concepts
  - 2D Stitching within wafer with high complex circuitry and thus challenge of device/layout optimization on stitching borders

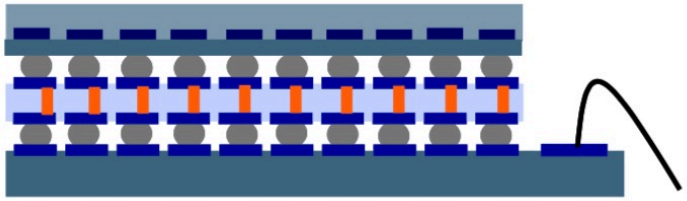







from LFoundry presentation at IUNET meeting, Sep 2017

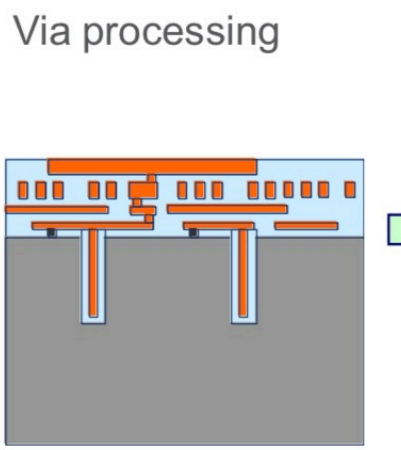
# Basics of CMOS 3D integration



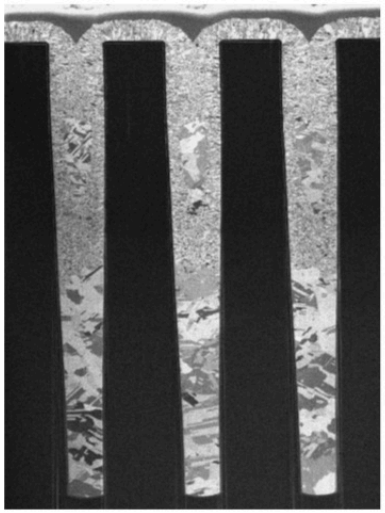
- Concept:
  - Stacking of multiple (>2) layers: detection layer + ROIC layers
    - Example: passive photodetector layer + analog ROIC + digital image processor
  - Using high density bumping + area redistributed TSVs
- Advantages:
  - General: optimization of (CMOS) technology for different layers
  - Imager system:
    - Vertical parallel readout chain allows high speed
    - Triple (n-fold) area per pixel allows complex electronics per pixel
    - Low capacitance interconnect to digital image processor allows high speed and low power
- Challenge: system architecture:
  - Optimal split in different layers of functionality and technology

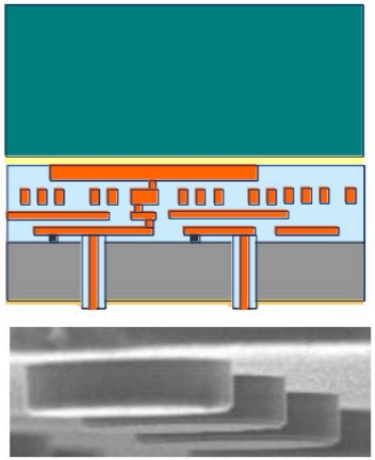
P. De Moor (IMEC)

# Basics of CMOS 3D integration



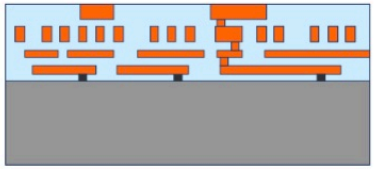
Via processing

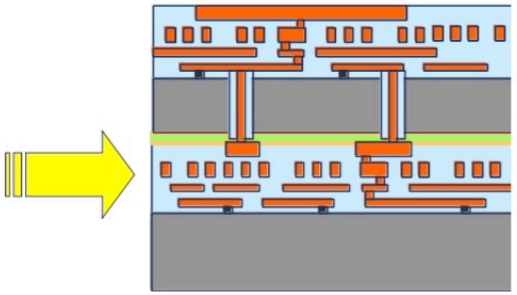


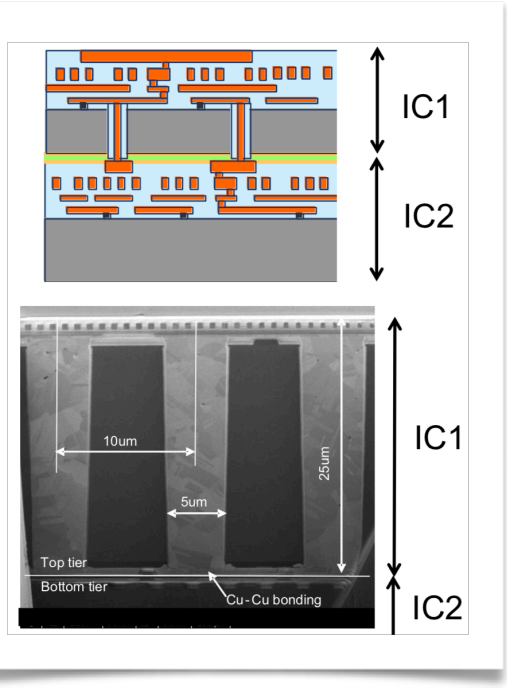


Extreme thinning
(on carrier)

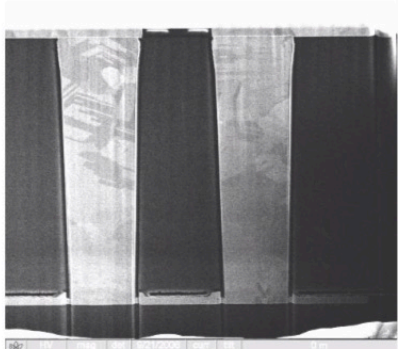









Mixed polymer and Cu-Cu
thermocompression bonding

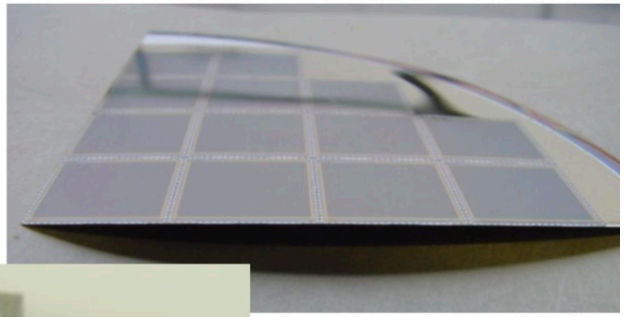


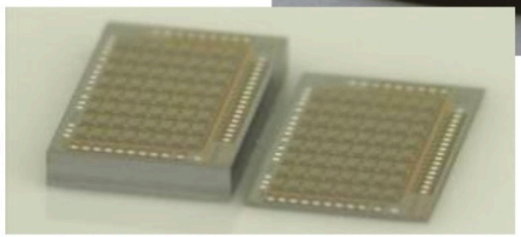
P. De Moor (IMEC)

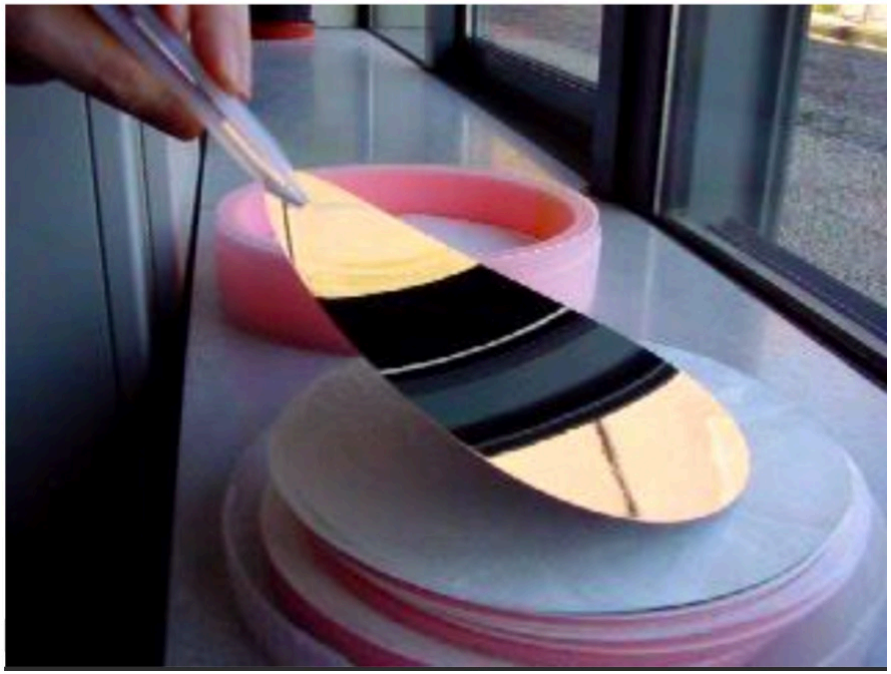
# Wafer Thinning

- Technology:
  - Course + fine grinding
  - Critical: thinning damage, impact on devices
- Wafer handling:
  - Very thin wafers (< 100 um): use of carrier wafers and temporary wafer (de-)bonding technology
- IMEC results:
  - Thinning down to 15 um
  - Total thickness variation ~ 2 um on 200 mm wafer

P. De Moor (IMEC)

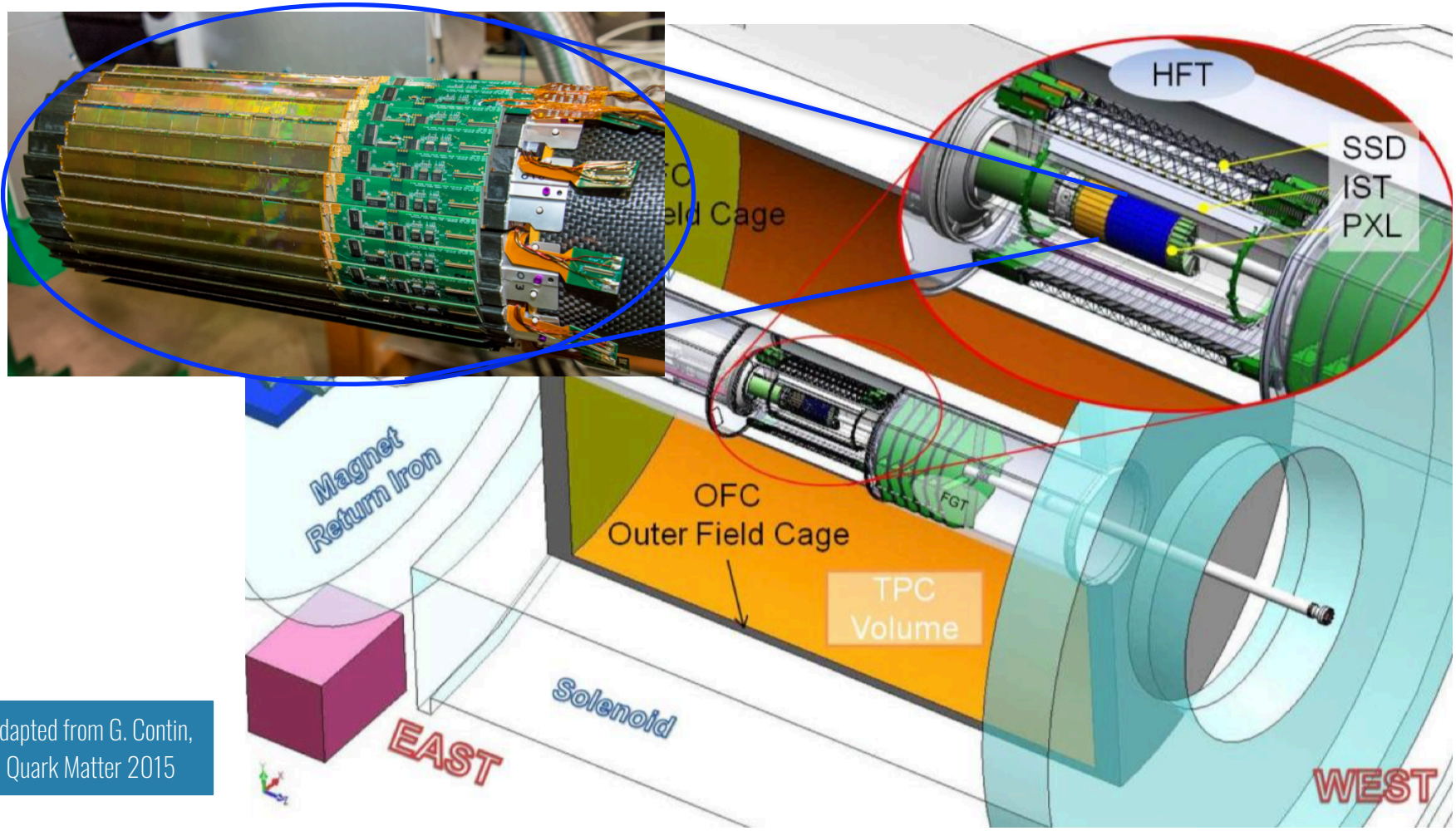






# STAR Heavy Flavour Tracker at RHIC

## First MAPS based vertex tracker at a collider experiment!

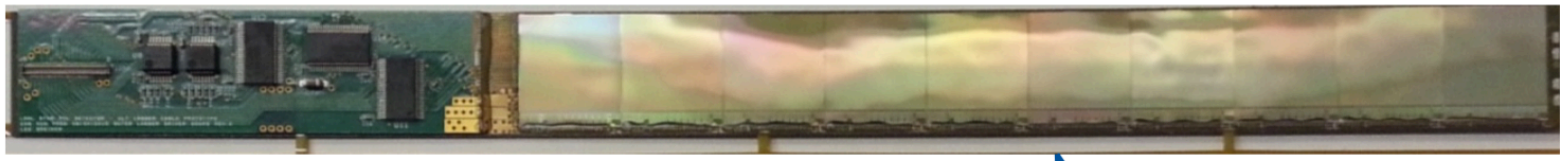



adapted from G. Contin, Quark Matter 2015

# MIMOSA28 in STAR HFT

## Basic Detector Element

Ladder with 10 MAPS sensors (~ 2×2 cm each)



| | |
|---|---|
| DCA Pointing resolution | (10 ⊕ 24 GeV/p·c) μm |
| Layers | Layer 1 at 2.8 cm radius<br>Layer 2 at 8 cm radius |
| Pixel size | 20.7 μm X 20.7 μm |
| Hit resolution | 3.7 μm (6 μm geometric) |
| Position stability | 5 μm rms (20 μm envelope) |
| Material budget first layer | $X/X_0$ = 0.39% (Al cond. cable) |
| Number of pixels | 356 M |
| Integration time (affects pileup) | 185.6 μs |
| Radiation environment | 20 to 90 kRad / year<br>$2*10^{11}$ to $10^{12}$ 1MeV n eq/cm$^2$ |
| Rapid detector replacement | < 1 day |

4 ladders / sector
5 sectors / half
10 sectors total

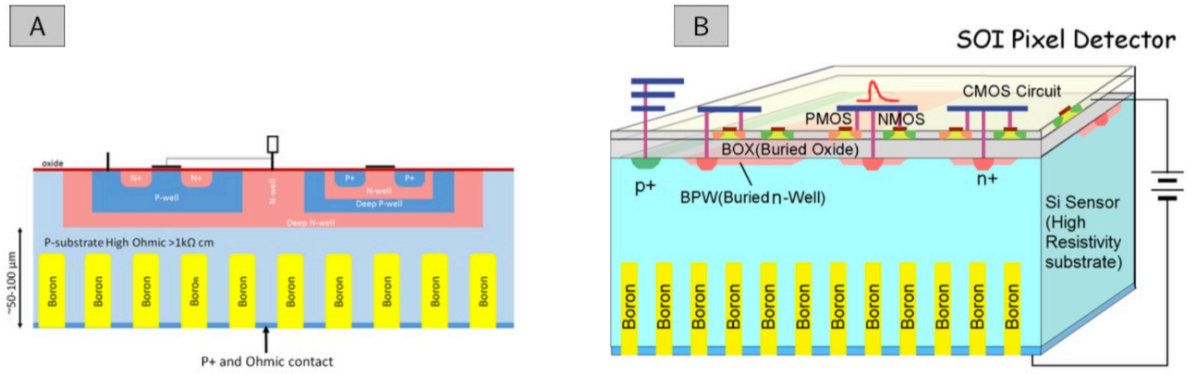
carbon fiber sector tubes
(~ 200 μm thick)

adapted from P. Riedler, CPAD 2018

# MAPS for neutron detection

- Neutron imaging provides information on materials and structures otherwise opaque to X-rays (metal and mechanical structure analysis, automotive and aviation safety-sensitive diagnosis)
- Particularly important for the study of archaeological samples, non-destructive tests with high spatial resolution and low neutron fluxes (avoids material activation)
- Silicon is not sensitive to neutrons, but one could use a conversion material (e.g. lithium fluoride or enriched Boron) and then use a silicon sensor as detector
- use of 3D geometries to increase the probability of detecting reaction products
- Ongoing activity using MAPS on a HR-substrate (A) and SOI technology (B)

Roberto Mendicino, INFN Trento




a monolithic 3D detector would be a turning point for the field of neutron imaging