BUILT-IN SELF-TEST ARCHITECTURE USING LOGIC MODULE

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ABSTRACT

A Built-in self-test technique constitute a class of algorithms that provide the capability of performing at speed testing with high fault coverage, whereas at the same time they relax the reliance on expensive external testing equipment. Hence, they constitute a striking solution to the problem of testing VLSI devices. BIST techniques are typically classified into offline and online Concurrent BIST performs two modes of operations, test mode and normal mode during test mode the test generator (TG) result is compared with higher order bits and the output is given to comparator circuit. During normal operation mode the inputs to the CUT are driven from the normal inputs. The modified Decoder and SRAM is used to reduce the switching activity thus the dynamic power dissipation can be decrease. The output is verified by response verifier (RV) and the fault is recognizedby using testing. The operating speed is faster while the operation is carried out as parallel process and it is suitable for all the type of IC's and VLSI circuits.

KEYWORDS

Built-In Self-Test, Design for Testability, Testing.

1. INTRODUCTION

Built-in self-test methods (BIST) are a vivid and practical solution to the problem of testing circuits and VLSI systems. BIST algorithms are classified offline and online. Autonomous architectures work in the usual or test mode. In the test mode, the input signals generated by the test generator module are applied to the inputs of the tested circuit (CUT), and the results to the response verifier (RV). Therefore, to perform the test, the normal operation of the CUT is inhibited and, consequently, the performance of the system in which the circuit is turned on is deteriorating. [1] To exclude this performance degradation, parallel BIST methods were proposed that use input vectors fed to the CUT inputs during normal operation.BIST uses a test pattern generator (TPG) to generate test patterns that apply to the inputs of the tested circuit (CUT). The block diagram of the input vector controlling the parallel BIST technology is shown in Figure. 1. CUT is combinational, has inputs and outputs, and it is checked exhaustively, hence, the size of the test set is. This method can work in one of two modes - normal and test [2].In normal mode, the CUT inputs, designated as, are controlled from the normal input vector (A [n: 1]). A also connects to the generator and the comparator Active Test set (AGC), where it is compared to a set of active test vectors, called the active test suite. If it is found that A coincides with one of the active test vectors, we say that there was a hit, or that the input vector (A) hit. When a hit occurs, A is removed from the active test set, and the Verifier Response Verifier (RV) [3] captures the CUT response to the input vector. When all the input vectors hit.

The contents of the Verifier Response are checked to decide whether an error has occurred in the CUT. active test set, and the Response Verifier (RV) [3] captures the CUT response to the input vector. When all input vectors have performed a hit.

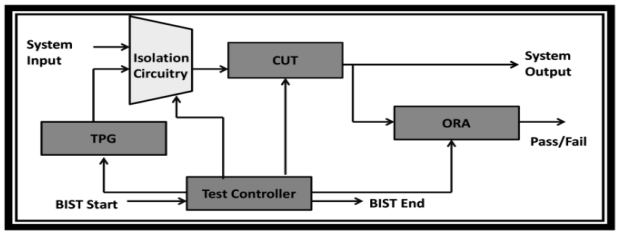

Figure 1. Input vector monitoring of parallel BIST [5].

2. BACKGROUND AND MOTIVATION OF RESEARCH

In the earlier period, several researchers and authors have investigated the BIST testing techniques for the detection of fault coverage. And S Sivanantham, et. al.[1] Proposed an Adaptive Low Power RTPG for BIST based test applications. In this research paper, researcher concerned about the power reduction during testing in scan based tests. But methods to reduce shift power will results in test coverage loss. So Low Power Random Test Pattern Generator (LPRTPG) is presenting to get better the trade-off between shift power reduction and the test coverage loss. For getting the required trade-off, an adaptive type performance is utilizing where the previous test results are given as feedback to a transition controller which is proficient of generating highly correlated test patterns. The tentative results on ISCAS'89 benchmark circuits' shows effectiveness of the work in terms of reduction in test power. And Ioannis Voyiatzis et. al. [2] Proposed an Input Vector Monitoring Concurrent BIST Architecture Using SRAM Cells. In this research article, concurrent built-in self test (BIST) techniques perform testing during the normal operation of the IC's without imposing a require setting the circuit offline to perform the test. These techniques are evaluated based on the concurrent test latency (CTL) and the hardware overhead, whereas the circuit operates normally. In this brief discussion, researcher presents input vector monitoring concurrent BIST technique [4], which is based on the technique of monitoring a set of vectors reaching the circuit inputs during normal operation, and the use of a static-RAM like structure to store the comparative locations of the vectors that attain the circuit inputs in the examined window. After analysis of so many journals and articles we conclude that, there are two main techniques are used in Built-in Self-test (BIST) are On-Line BIST and Off-Line BIST. So in this paper we present an On-line BIST Testing technique operating in normal operation [5].

3. LITERATURE SURVEY

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S Sivanantham, et. al. [1]Proposed an Adaptive Low Power RTPG for BIST based test applications. In this research paper, researcher concerned about the power reduction during testing in scan based tests. But methods to reduce shift power will results in test coverage loss. So Low Power Random Test Pattern Generator (LPRTPG) is presenting to get better the trade-off between shift power reduction and the test coverage loss. For getting the required trade-off, an adaptive type performance is utilizing where the previous test results are given as feedback to a transition controller which is proficient of generating highly correlated test patterns. The tentative results on ISCAS'89 benchmark circuits' shows effectiveness of the work in terms of reduction in test power.

Ioannis Voyiatzis et. al. [2]Proposed an Input Vector Monitoring Concurrent BIST Architecture Using SRAM Cells. In this research paper, Input vector monitoring concurrent built-in self test (BIST) technique perform testing during the normal operation of the circuit without imposing a

require to set the circuit offline to perform the test [2]. These techniques are evaluated based on the hardware overhead and the concurrent test latency (CTL), whereas the circuit operates normally. In this brief discussion, researcher presents a novel input vector monitoring concurrent BIST technique, which is based on the scheme of monitoring a set of vectors reaching the circuit inputs during normal operation, and the use of a static-RAM like structure to store the comparative locations of the vectors that attain the circuit inputs in the examined window.

D. C. Huang et. al. [1] Discussed about An Efficient Parallel Transparent BIST Method for Multiple Embedded Memory Buffers. In this paper, researchers proposed a new transparent built-in self-test (T-BIST) technique to test multiple embedded memory arrays with various sizes in parallel. Also a new transparent test interface is designed to perform testing in the normal mode and to cope with nested interrupts in a real-time manner is discussed. They also developed a very powerful signature analysis technique to eliminate the tedious signature prediction process with almost no hardware cost. Based on the memory background data, an efficient TRSMarch algorithm, March algorithm, has also been developed to generate test patterns and expected test results.

Bernard Courtois et. al. [7] Proposed an On-Line and OFF-Line testing from digital to analog, from circuits to Board. The main goal of this research paper is to survey the design of circuit and system featuring testing capabilities. Design of failsafe reliable of Circuit Board and ASICs is broadly addressed.

Petr Fiser et. al. [8] A study of algorithms in the BIST method for column matching is proposed. Discussion of possible heuristic algorithms that solve the main part of the method of synthesis of BIST, Matching Column. The main part of this research article - the BIST design is an output decoder that converts pseudo-random code words LFSR into deterministic tests, previously calculated with the ATPG.

Jahangiri et. al. [9] have tried to examine test patterns for IC's that are both secure and have very high exposure. Protected applications often require high test quality with rising demands at 65 nanometer and below. A test method that is protected is necessary such that the test can be conducted outside of a costly protected test environment. Logic BIST is the most protected test method. However, for some devices, it doesn't provide a high enough test support or quality recently desired fault models.

Jinkyu Lee et. al. [10] proposed LFSR Reseeding Scheme Achieving Low-Power dissipation during Test. several test data compression schemes are based on LFSR reseeding. A disadvantage of these techniques is that the unspecified bits are contain random values resulting in a large number of transitions during scan-in, as a result causing high power dissipation. This article presents a new encoding technique that can be used in conjunction with any LFSR reseeding scheme to significantly reduce test power and even further decrease test storage. The proposed encoding technique acts as a second stage of compression after LFSR reseeding. There are two goals which are: First, it decreases the number of transitions in the scan chains and second it reduces the number of bits that need to be generated via LFSR reseeding algorithm. An experimental result shows that the proposed scheme significantly reduces test power and in several cases provides greater test data compression than LFSR reseeding technique.

G. Sudhagar et. al. [11]Discussed about the noval architecture for vlsi design. The time, power, and data volume are among some of the most challenging issues for testing IC's and have not been fully determined, but also scan-based scheme is used. A novel architecture, referred to the Selective Trigger-Scan architecture, introduced in this article to address these issues. This architecture reduces switching action in the circuit-under-test (CUT) and increases the clock

frequency of the scanning process. A secondary chain is utilized in this architecture to avoid the large number of transitions to the CUT during the scan in process, also enabling retention of the currently applied test vectors and applying only essential changes to them. It also allows delay fault testing. Using ISCAS-85 and ISCAS-89 benchmark circuits, the efficiency of this architecture for improving SoC. These test such as, time, and data volume is experimentally evaluated and confirmed.

Xijiang Lin et. al [12] proposed an Adaptive Low Shift Power Test Pattern Generator for Logic-BIST. While increasing the correlation between adjacent test stimulus bits can significantly decrease shift power consumption. Though, it often causes test coverage loss when applying it to decrease the shift power consumption in logic Built-in Self-test.In this article, a new adaptive low shift power random test pattern generator (ALP-RTPG) is presented to get better the tradeoff among test coverage loss and shift power reduction in logic-BIST. This is achieved by applying the information derived from test responses to dynamically adjust the correlation between adjacent test stimulus bits. When comparing with an available method, called LT-RTPG, experimental results for industrial designs show that the projected method can significantly decrease the test coverage loss while still achieving dramatic shift power reduction.

Table1. Comparison of literature journals

Author	Proposed Technique	Advantage	Disadvantage
Renju Thomas John	Adaptive Low Power RTPG for BIST	power reduction during testing	reduce shift power will results in test coverage loss
Ioannis Voyiatzis	Input Vector Monitoring Concurrent BIST Architecture Using SRAM Cells	It is more efficient than previouslyproposed input vector monitoring concurrent BIST techniques interms of hardware overhead and CTL	hardware overhead and CTL trade-off
D. C. Huang	Efficient Parallel Transparent BIST Method for Multiple Embedded Memory Buffers	reduce the hardware overhead without losing fault coverage	More Complexity
Jinkyu Lee	LFSR Reseeding Scheme Achieving Low-Power dissipation during Test	Reduce test power and even further decrease test storage.	bits are contain random values resulting in a large number of transitions during scan-in.
G. Sudhagar	Novel architecture for VLSI testing	Reduces switching action in the circuit-under-test (CUT) and increases the clock frequency of the scanning process	delay fault testing

Rinitha.R et. al. [13] discussed about Built in self test and provide a brief information about its test application. As the compactness of system-on-chip increase, it becomes striking to integrate dedicated test logic on a chip. In this survey test applications and its terms, common test methods and analyze the basic test procedure are mainly focused. And time, area, power are the most challenging issues. The concept of Built-in Self-Test (BIST) is introduced and discussed. This BIST technique not only offers economic profit but also provides attractive technical opportunities w.r.t. hierarchical testing and the reprocess of test logic during the application of the VLSI circuit. Recently BIST Research is being highly used in receiver system and wireless transmitter for the detection of mismatch and non-linear parameters. ,

The important task of this paper is testing has been pointed out in this survey. And also discussed about recent research of BIST architecture

4. PROPOSED DESIGN ARCHITECTURE

In this article, consider a CUT with n inputs. The number of possible input vectors for this CUT is N = 2n. The proposed technique is based on the construction of the window vector monitoring, the size of which is W, where W = 2w, where 'w' is an integer w<n. Each moment the test vectors belonging to the window are controlled, and if the vector hits, RV is activated. The number of test vectors that we want to track in parallel is equal to K, the number of words used by RAM (for practical reasons, K is chosen equal to the power of 2, that is, K = 2k). The bits of the input vector are divided into two different sets containing w bits of k bits, respectively, so that

$$w + k = n.$$

The k (high-order) bits of the input vector demonstrate whether the input vector relate with the window under consideration.

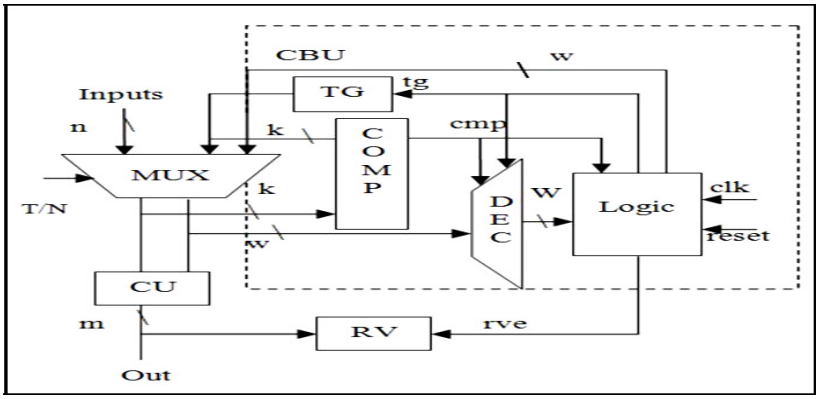

Figure 2. Proposed Architecture [14].

The 'w' remaining bits illustrate the relative location of the incoming vector inthe existing window. If the incoming vector belongs to the current window and has not been received during the examination of thecurrent window, that means the vector has performed a hit and theRV is clocked to capture the CUT's response to the vector. Wheneach and every vector that belongs to the existing window has reached the CUTinputs, we proceed to look at the next window, that response verifier (RV), and output we receive from CUT.

4.1 MODIFIED DECODER

A decoder is a device that performs an inverse operation of the encoder, suppresses the encoding, so that the original information can be restored. A similar method used for encoding is often simply reversed for decoding. This is a combinational logic that converts binary information from n input strings to a highest of 2n unique output lines. In digital electronics, a decoder can receive a logic structure with multiple inputs and multiple outputs (MIMO), which converts encoded logic inputs to coded logical outputs, where the input and output codes are different. For example, N-to-2n, binary-coded decimal decoders. The inclusion of the inputs must be switched on so that the decoder is working, otherwise its output takes one damaged output codeword. Decoding is important in applications such as data multiplexing, a 7-segment display.

4.2 SRAM

SRAM is a type of semiconductor memory in which a bitmap scheme is used to store each bit. The static technique distinguishes it from dynamic RAM (DRAM), which must be periodically updated. SRAM demonstrates the superiority of data, but in the conventional sense it is still volatile, that data eventually disappears when memory is not receiving power. The power consumption of SRAM varies greatly, depending on how often it is used; This can be the same power consumption as dynamic RAM, when used at high frequencies, and some ICs can consume several watts at full bandwidth. Alternatively, static RAM used in applications such as microprocessors with a frequency of moderate frequency, consumes very little power and can have almost insignificant power consumption in the vicinity of several microwaves.

4.3 CUT

In normal mode, the inputs to the CUT are controlled from the normal inputs. The inputs n are also connected to the CBU as follows: w low-order inputs are applied to the inputs of the decoder; Inputs K of high order are fed to the inputs of the comparator. When a vector belonging to an existing window reaches the CUT inputs, the comparator is turned on and any one output of the decoder is activated. During the first half of the clock cycle (clk and cmp are included), the address cell is read, since the read value is zero, the counter of the w-stage is triggered through the NOT gate with the output of the RV enable signal. In the second half of the clock cycle, the left trigger allows the buffers to write the value 1 to the addressed cell and activate the AND gate (the other inputs are clk and cmp).

4.4 RV (RESPONSE VERIFIER)

When all the input vectors hit, Verifier Response will check the contents. During the test mode, the inputs to the CUT are controlled from the CBU outputs labeled TG [n: 1]. The parallel test delay (CTL) of the input vector control method is the average time (also counted in time units or the number of clock cycles) required to complete the test, while the CUT is operating in normal mode. The active test generator and the C-BIST comparator are one linear feedback shift register (LFSR) and a comparator, and thus the active test consists of only one active test vector that is the current LFSR value. Although in normal mode, the input vector is compared with a unique active test vector. If two vectors are equal, LFSR goes to the next state, changing the active test vector, and the response verifier is activated.

5. IMPLEMENTATION AND RESULTS

In this session the simulation and results were shown figure 3. Shows the Block diagram of Top-Module of BIST Architecture. Figure 4. shows RTL block of BIST Architecture. Figure 5. represents the synthesis Simulation Waveform Input Output Waveform of Concurrent BIST Architecture. And Table 1. represents hardware utilization summery of design. Figure3. shows a top level module of BIST Architecture. The inputs are inputs [4:0], T_N, clk (clock), rst (reset), and RV (Response Verifier). The outputs from the top module are Out (output).Figure 4. shows all the connections between the modules of the BIST architecture. It also has the connections of the top module to the actual pins of all other modules.The proposed architecture has been and simulated using Xilinx-ISE 14.7 tool. This software tool of Xilinx used for synthesis and analysis of HDL designs and allow developer to synthesize their design, and perform timing analysis [15], generate RTL diagram and simulate the HDL code in input output waveforms. Input output waveforms of BIST architecture is show in figure 5.

In table 1. We present the successful simulation of BIST architecture, which show the project status and device utilization summary. The best result of this project is to minimize the number of slice register and slice LUT's. Number of slices is 12 and number of LUT's are 25.

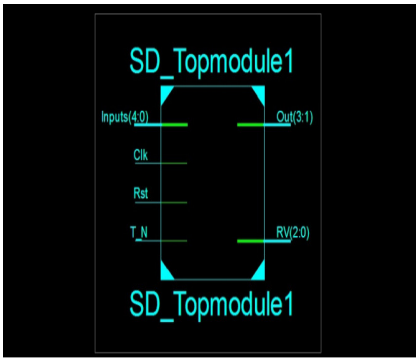

Figure 3. Top level simulated module with input and output ports.

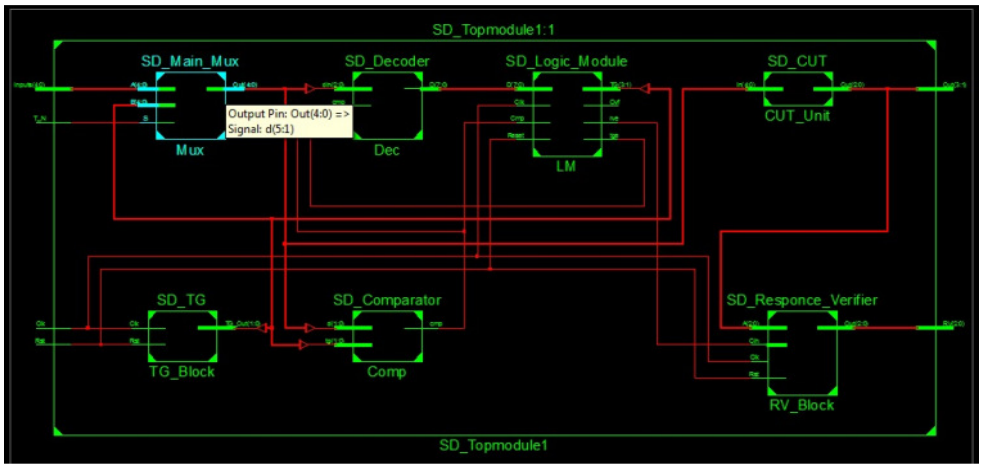

Figure 4. Internal Connections of BIST ARCHITECTURE.

Figure 5. Input Output Waveform of Concurrent BIST Architecture.

Table2. Synthesis report of BIST Archtecture.

SD_Topmodule1 Project Status (06/07/2017 - 00:22:56)			
Project File:	final_bist.xise	**Parser Errors:**	No Errors
Module Name:	SD_Topmodule1	**Implementation State:**	Placed and Routed
Target Device:	xc6slx100-2fgg484	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	52 Warnings (33 new)
Design Goal:	Power Optimization	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	strategy1	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	12	126,576	1%	
Number used as Flip Flops	8			
Number used as Latches	4			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	22	63,288	1%	
Number used as logic	22	63,288	1%	

Table3. Timing Constraints

Met	Constraints	Check	Worst Case Slack	Best Case Achievable	Timing Errors	Timing Score
Yes	TS_CLK = PERIOD TIMEGRP "Clk" 20ns HIGH 50%	SETUP HOLD	7.086ns 0.424ns	5.828ns	0.0	0.0

6. COMPARISONS

To evaluate the presented design, we compare it with the input vector monitoring concurrent BIST techniques proposed by Ioannis Voyiatzis. In C-BIST [4] was the first input vector monitoring concurrent BIST technique proposed, and suffers from long hardware overhead and CTL; therefore modifications have been proposed, Order Independent Signature Analysis Technique (OISAT) [10], Multiple Hardware Sig-nature Analysis Technique (MHSAT) [9], RAM-based Concurrent BIST (RCBIST) [15], Window Monitoring Concurrent BIST (WMCBIST) [3], and Square Windows Monitoring Concurrent BIST (SWIM) [11]. The comparisons will be performed with respect to the hardware overhead. From the above literatures, following conclusions can be drawn.The hardware overhead of the proposed scheme is lower than the other schemes.

7. CONCLUSION

BIST algorithm constitutes an attractive solution to the problem of testing IC's. BIST architecture performs testing during the digital circuit normal operation without imposing a requirement to set the circuit offline to perform the test; as a result they can circumvent problems appearing in offline BIST techniques. The evaluation criteria for this set of schemes are the hardware overhead, i.e., the time required for the test to complete, although the circuit operates normally. In

this paper brief, a concurrent BIST architecture has been presented, based on the SRAM cell like structure for storing the information of whether an input vector has appeared or not in normal operation. The proposed technique is shown to be more efficient than previously proposed input vector monitoring concurrent BIST techniques in terms of hardware overhead.

REFERENCES

[1] R. T. John, K. D. Sreekanth, and S. Sivanantham, "Adaptive Low Power RTPG for BIST based test applications," 2013 Int. Conf. Inf. Commun. Embed. Syst. ICICES 2013, pp. 933–936, 2013.

[2] I. Voyiatzis, C. Efstathiou, C. Sgouropoulou, and D. Magos, "Input vector monitoring concurrent BIST with Low hardware overhead."

[3] P. G. Scholar, "ISSN No : 2348-4845 Design and Implementation of Online BIST Architecture Using SRAM Cells ISSN No : 2348-4845," vol. 2, no. December, pp. 328–332, 2015.

[4] S. Shrivastava, "Testing Technique of BIST : A Survey," vol. 161, no. 3, pp. 22–25, 2017.

[5] K. Keerthika and A. H. Jeeva Oli, "Online and Offline Testing Of C-Bist Using Sram," IOSR J. VLSI Signal Process. Ver. II, vol. 5, no. 1, pp. 50–53, 2015.

[6] I. Introductiok, "Efficient Parallel Transparent BIST Method for Multiple Embedded Memory Buffers," 2000.

[7] B. C. and M. Lubaszewski, "ON-LINE AND OFF-LINE TESTING: FROM DIGITAL TO ANALOG, FROM CIRCUITS TO BOARDS," IEEE, p. 34.

[8] P. Fiser and H. Kubatova, "Survey of the Algorithms in the Column-Matching BIST Method," p. 7695, 2004.

[9] J. Jahangiri and R. Press, "Test patterns for ICs that are both secure and have very high coverage," AUTOTESTCON (Proceedings), no. September, pp. 92–96, 2008.

[10] L. S. A. Low-power, "Short Papers," vol. 26, no. 2, pp. 396–401, 2007.

[11] G. Sudhagar, S. Senthil Kumar, G. Ramesh, and G. Sathish Kumar, "Implementation of a novel architecture for VLSI testing," 2013 Int. Conf. Emerg. Trends VLSI, Embed. Syst. Nano Electron. Telecommun. Syst. ICEVENT 2013, pp. 13–16, 2013.

[12] S. Remersaro, X. Lin, S. M. Reddy, M. G. Corporation, and W. Lafayette, "Low Shift and Capture Power Scan Tests," 2007.

[13] R. Rinitha and R. Ponni, "Testing in VLSI : A Survey."

[14] B. Divyapreethi and T. Karthik, "Input vector monitoring concurrent BIST architecture using modified SRAM cells," ARPN J. Eng. Appl. Sci., vol. 10, no. 9, pp. 4042–4046, 2015.

[15] D. Verification, S. Timing, and X. Device, "Xilinx ISE 6 Software Manuals and Help - PDF Collection," Interfaces (Providence)., no. c, pp. 1–14.

[16] K. K. Saluja, R. Sharma, and C. R. Kime, "Concurrent com-parative built-in testing of digital circuits," Dept. Electr. Comput. Eng., Univ. Wisconsin, Madison, WI, USA, Tech. Rep. ECE-8711, 1986.

[17] I.Voyiatzis, T. Haniotakis, C. Efstathiou, and H. Antonopoulou, "A con-current BIST architecture based on monitoring square windows," in Proc. 5th Int. Conf. DTIS, Mar. 2010, pp. 1–6.

[18] M. A. Kochte, C. Zoellin, and H.-J. Wunderlich, "Concurrent self-testwith partially specified patterns for low test latency and overhead," in Proc. 14th Eur. Test Symp., May 2009, pp. 53–58.

[19] S. Almukhaizim and Y. Makris, "Concurrent error detection methods for asynchronous burst mode machines," IEEE Trans. Comput., vol. 56, no. 6, pp. 785–798, Jun. 2007.

[20] S. Almukhaizim, P. Drineas, and Y. Makris, "Entropy-driven parity tree selection for low-cost concurrent error detection," IEEE Trans. Comput. Aided Design Integr. Circuits Syst., vol. 25, no. 8, pp. 1547–1554, Aug. 2006.

[21] I. Voyiatzis, A. Paschalis, D. Gizopoulos, N. Kranitis, and C.Halatsis, "A concurrent BIST architecture based on a self-testing RAM," IEEE Trans. Rel., vol. 54, no. 1, pp. 69–78,Mar. 200.

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