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Effective Thermal Conductivity of Six Sigma's Copper Reinforced Column Grid Array Interconnect for Ceramic Microelectronic Packages

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Abstract

Thermal management of flip chip style integrated circuits often relies on thermal conduction through the ceramic package and high lead solder grid array leads into the printed wiring board as the primary path for heat removal. Thermal analysis of this package configuration requires accurate characterization of the sometimes geometrically complex package-to-board interface. Given the unique structure of the Six Sigma column grid array (CGA) interconnect, a detailed finite element sub-model was used to numerically derive the effective thermal conductivity with comparisons to a conventional CGA interconnect. Once an effective thermal conductivity value is obtained, the entire interconnect layer can be represented as a fictitious cuboid layer for inclusion in a more traditional "closed-form" thermal resistance calculation. This method allows the package designer a quick and robust method to evaluate initial thermal design study tradeoffs.

1.0 Introduction

Thermal management of flip chip (F/C) or it's acronym, C4 (Controlled Collapse Chip Connection) integrated circuits in high reliability aerospace systems often relies on thermal conduction through the microelectronic package substrate and leads into the printed wiring board (PWB) as the primary path for heat dissipation (refer Figure 1). Thermal analysis of this high-reliability alumina ceramic package style requires accurate characterization of the chip-to-package (i.e. C4) and package-to-board (i.e. C5 or Controlled Collapse Chip Connection Carrier) interfaces. For flipped Silicon die attached to a ≥32 mm square column grid array leaded package; these interfaces are geometrically complex and difficult to model thermally from an overall package level perspective.

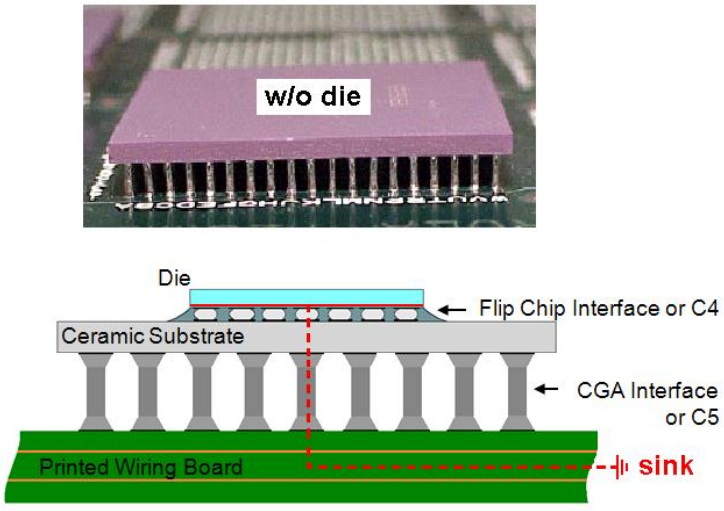


Fig. 1: Assembled Ceramic CGA Package (Top). Package Schematic (Bottom).

Numerical simulations using a commercially available finite element software code [1] have been performed for steady-state thermal conduction; comparing the Six Sigma (henceforth 6σ) copper helix reinforced column grid array (CGA) versus the conventional IBM high lead style interconnect. Both CGA interconnects are shown, substrate down, in Figure 2 prior to PWB assembly. The latter interconnect style has been available via licensing from IBM for over 15 years. The former is owned by Winslow Automation, which acquired the rights in 1996 to the original 1987 Raychem corporation patent [3]. More information on product utility/application can be found at the manufacture's websites and referenced literature [4~5]. For comparison in this paper, both interconnects adhere to industry standard geometry for high-density CGA applications. That is, 1.0/1.27 mm CGA pitch, 0.5 mm column diameter, and a substrate-to-PWB standoff height of 2.2 mm.

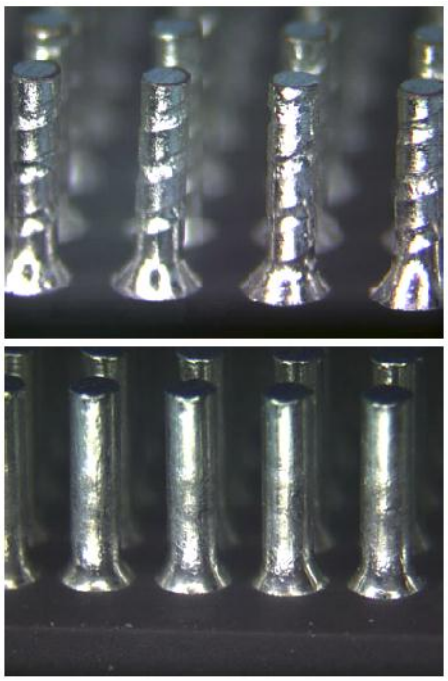


Fig. 2: 6σ CGA (Top). Conventional IBM Style CLASP CGA (Bottom). [2]

Why this interconnect style is favored over other types (e.g. ball grid array) for large area packages is beyond the scope of this paper. But suffice to say, the primary reason is mitigation of the thermal expansion mismatch between the low expansion alumina substrate and the high expansion PWB [6~7].

2.0 Sub/Global Model Methodology

Detailed finite element (FE) models, also known as sub-models, can be used to numerically derive the effective thermal conductivity of these complicated interfaces. Once an effective thermal conductivity value is found, the entire interconnect array can be represented as a fictitious cuboid layer of equal height. This can then be incorporated into a geometrically simpler global model yielding package level ThetaJB (junction-to-board or Θ_{JB}) metrics. A methodology such as this is more robust and faster than the traditional discrete thermal modeling approach when used to compare various package thermal tradeoffs. In contrast, the discrete approach presumes all interconnect geometry is modeled "in detail" as part of the package level thermal model. This methodology captures the correct thermal path but lacks design iteration robustness and can be very time consuming during FE model creation. The sub-modeling approach seeks to overcome these limitations. This concept is shown schematically in Figure 3. Note, the implied simplicity if the interconnects can be represented as cuboid layers.

Historically, the technique was first published by Johnson, et al. [8-9], and later expanded to include organic substrate packages by others [10]. The technique has been shown to provide close agreement with experimental measurements.

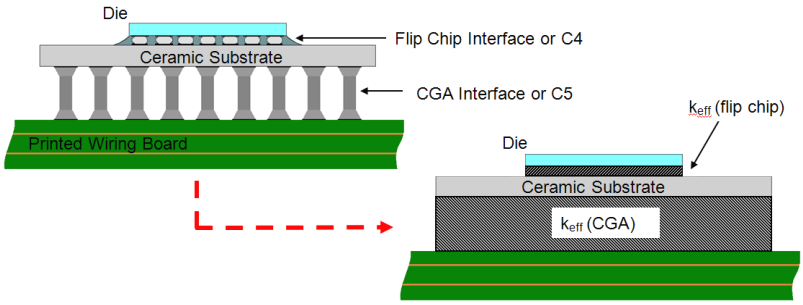


Fig. 3: Proposed Sub-Modeling Concept.

2.1 Methodology Summary:

Step 1: Construct unit pitch-area FE models of C4 and C5 interconnect geometries with all relevant detail included. Model symmetry may be exploited to reduce computational expense. Then proceed to determine the effective through plane thermal conductivity (i.e. $k_{eff} \equiv k_z$) of interconnect if represented by a fictitious solid volume layer of equal height (i.e. cuboid).

Step 2: Construct package/global level model with cuboid representation of the C4/C5 interconnect geometry. Cuboid effective thermal conductivity is assigned based on step 1 results. Interconnect in-plane thermal spreading effects are minimized by setting $k_x = k_y$ (transversely isotropic) to be either polymer underfill thermal conductivity for C4 or still air for C5 cuboid. This ensures only 1D heat transfer through the interconnect layer. Global model can now be solved for Θ_{JB} with a given power density, which for illustrative simplicity, was uniform over the die face.

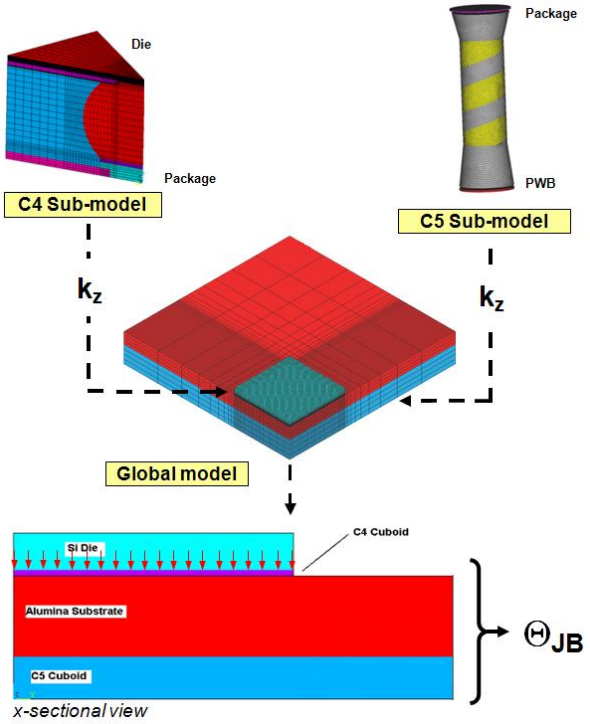


Fig. 4: Thermal Sub-Modeling Methodology.

3.0 Thermal Property Characterization

Past experience has shown that in order to quantitatively predict effective thermal conductivity, the analysis must incorporate accurate thermophysical properties. In the present study, temperature dependent thermal conductivities were used for most of the materials. The source of these properties included Thermophysical Property Research Lab [11] (now CINDAS [12]), reliable vendor measurements, and Kyocera laser flash thermal diffusivity measured data (refer Table 1).

The co-fired tungsten metallization and electroless nickel-plating layers are more problematic to measure experimentally; their thermal conductivities were calculated using measured electrical resistivity and the Wiedemann-Franz relation.

$$\frac{k}{\sigma} = L \times T \qquad (1)$$

where:

k = thermal conductivity (W/m-K)

σ = electrical conductivity (1/ Ω-m)

L = Lorenz Number (2.45E-8 W-Ω/K^2)

T = Absolute temperature (Kelvin)

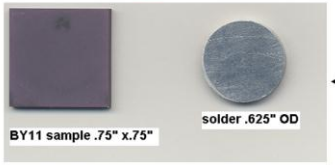
This theoretical approach allows "electron only" metallic conductor thermal conductivity to be estimated from an experimentally easier electrical resistivity measurement via four-point probe Kelvin technique. Of course, the co-fired ceramic conductor is actually in the intermediate regime where both electron and phonon (lattice vibration) conduction contribute.

$$k_{total} = k_{electron} + k_{phonon} \qquad (2)$$

The latter is typically a small contribution of the total, and affords the theoretical foundations upon which metals and insulators differ in thermal conductivity. Thus, it is assumed the values represented are considered conservative. The macroscale theoretical thermal conductivity of the IC (micron level) layers can be found in an earlier paper on the topic [13].

M. Eblen - 1/25/06
all props measured less alumina cp

SAMPLE	TEMP (C)	THERM COND (W/m.K)	THERM DIF (cm^2/s)	COMMENT	THICK (mm)	TIME 1/2 (ms)	HEAT CAP (cal/gK)	DENSITY (g/cc)	No. of AVGS
90% Alumina	24.3	15.2	0.0489	Kyocera 30mil layer tape	1.715	83.536	0.200	3.720	5
46Pb/46Sn/8B	23.7	38.2	0.2453	Cast solder, recommend 41 W/mK	2.034	23.405	0.042	8.951	5
Al ref std	23.8	240.1	0.9840	99.999% Al std TC=237 W/mK	2.548	9.158	0.216	2.702	5



2-1/4 layer alumina sample and cast solder sample. Solder sample checked for internal voiding due to BGA sphere oxidation upon ceramic crucible melting.

Table 1: Measured Thermal Diffusivity Data.

4.0 CGA Sub-Model Geometry

The sub-modeling approach captured a high level of geometrical fidelity in the 6σ interconnect as shown below in Figure 5. The approximated shape of the eutectic solder fillet embrace was obtained from micrographs and relevant IBM design guideline recommendations [5].

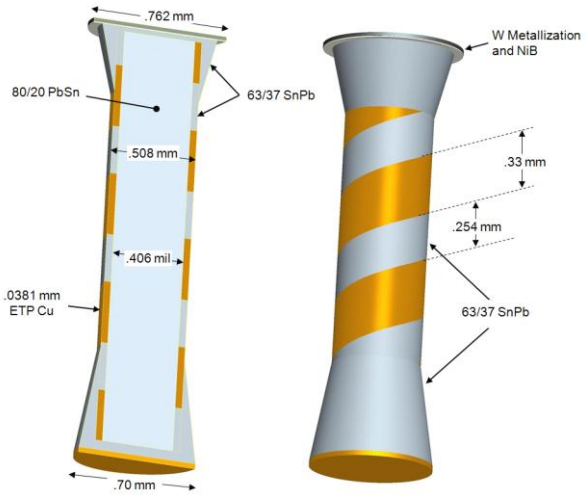


Fig. 5: 6σ CGA Interconnect Pro/E Model.

Also included was the 0.7 mm diameter non-solder mask defined (NSMD) via-in-pad geometry shown in figure 5. Other PWB attachment configurations, such as the more thermally constrictive dogbone-style pad, are also in widespread use. Geometric details on the later can be found in reference [5]. The FE model was meshed with linear tetrahedral elements and is shown in Figure 6. Geometrically thin features were modeled with linear hexagonal elements and then tied together with surface-to-surface contact elements. Solution time for this scalar field problem was less than thirty minutes on a 64-bit workstation.

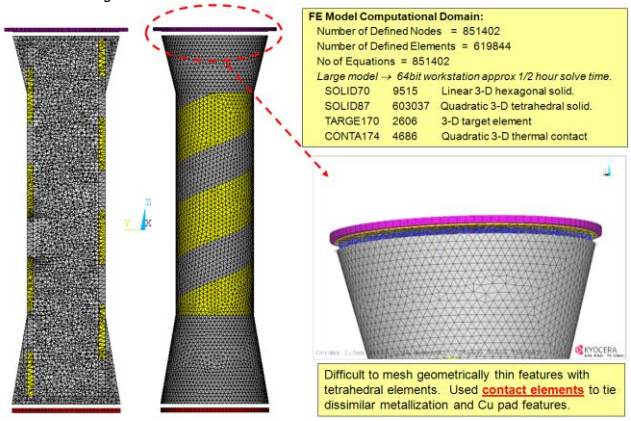


Fig. 6: 6σ Finite Element Sub-Model.

For completeness, Figure 7 illustrates the conventional CGA finite element sub-model used in the comparison. As shown, octant symmetry was exploited to reduce computational expense.

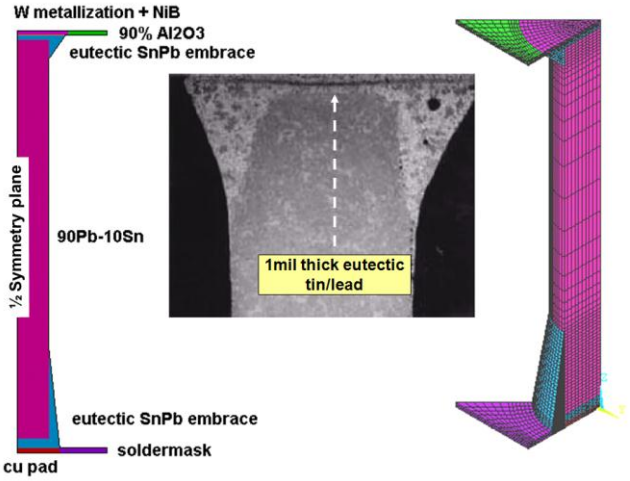


Fig. 7: Conventional CGA Geometry Definition

5.0 Sub-Model Effective Conductivity

From Fourier's law of heat conduction we can write:

$$\dot{q}_z = \frac{k_z \times \text{Area}}{\text{height}} \left(T_2 - T_1\right) \qquad (3)$$

$$\therefore$$

$$k_{eff} \equiv k_z = \frac{\left|\sum_{i=1}^{n} \dot{q}_z\right| \times \text{height}}{(\text{Unit Area}) \times \Delta T} \qquad (4)$$

Hence, for a prescribed and somewhat arbitrary ΔT, the FE sub-model is used to obtain the summed heat flow rate $\dot{q}_z$ (Watt/sec) from bottom nodes. Equation 4 can then be used to solve for the effective thermal conductivity assuming a unit pitch-area or a more technically rigorous and computationally intensive cylindrical approximation. For brevity, only the former will be discussed in this paper. Those calculation details are shown graphically in Figure 8. Additionally, all measured/calculated thermal conductivity values used for both sub-models types are summarized in Table 2.

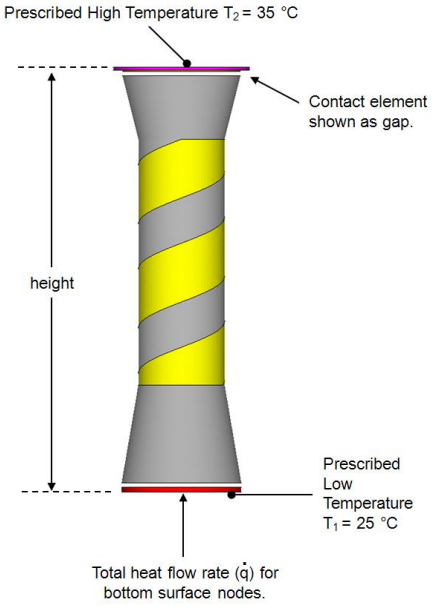


Fig. 8: CGA Sub-Model Effective Thermal Conductivity Calculation Description.

ID	Submodel Type [3]	Component Name	Material Composition	Thermal Conductivity @ 25C (W/mK)	Comments
1	6σ & IBM	Substrate Metallization	90% Al_2O_3 Cofired W	35.3 [1,2]	Lorenz number based on pure W, then calc based on ρ = 25.4 μΩ-cm
2		Substrate Nickel Plating	Electroless NiB	36.5 [1,2]	Lorenz number based on pure Ni, then calc based on ρ = 17 μΩ-cm
3		Eutectic Embrace	63Sn-37Sn	50.7	Thermophysical Property Research Lab (TPRL) recommended
4		PWB Copper Pad	electroplated Cu	360	TPRL
5	IBM	Solder Column	90Pb-10Sn	36	TPRL recommended, elevated temp assume scale with pure Pb
6	6σ	Solder Column Core	80Pb-20Sn	38	
7		Copper Helix	ETP Cu	360	TPRL
8	IBM	Substrate	90% Al_2O_3	15.2	KAI-R&D measured
9		PWB Solder Mask	photodefinable polymide	0.24 [1]	Vendor provided

Nomenclature

1 Property assumed invariant with temperature
2 Wiedemann-Franz Law
3 6σ = Six Sigma CGA & IBM = Conventional IBM CLASP Style CGA

Table 2: Sub-Model Thermophysical Properties.

Figure 9 illustrates the temperature (left) and thermal flux vector sum (right) contour plots for the 6σ sub-model. The thermal flux plot dramatically highlights the preferential thermal path found in the copper helix. This can be understood due to the 10X greater thermal conductivity versus the 80/20 PbSn solder core. The thickness of the tin plated copper ribbon was taken at 38 micron nominal. The tin plating thickness was unknown at the time of this writing and hence excluded from model; but would "only slightly" increase the k_{eff} of this interconnect.

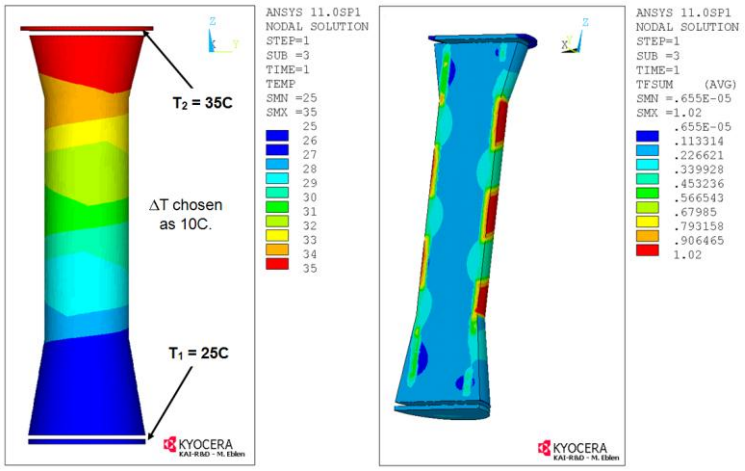


Fig. 9: Sub-model Results. Temp Plot (left), Thermal Flux Vector Sum Plot (right).

As expected, the 6σ interconnect has a more advantageous thermal conductivity due to the copper helix when compared against the conventional IBM style. The quantitative percent increase is 75% and 72% for both the 1 mm and 1.27 mm pitch interconnects respectively (refer Table 3). Although not expanded here, it should be appreciated that a temperature dependent k_{eff} equation would also be obtained such that high die power cases and/or elevated environmental conditions could also be considered.

Case #	CGA Interconnect Style	Interconnect Pitch	Effective Thermal Conductivity @ 25C (W/mK)	Total Sub-Model Height (μm)
1	IBM	1.0 mm	k_z = 7.89 k_x=k_y=.027	2328
2		1.27 mm	k_z = 4.96 k_x=k_y=.027	
3	6σ	1.0 mm	k_z = 13.78 k_x=k_y=.027	
4		1.27 mm	k_z = 8.54 k_x=k_y=.027	

Table 3: Sub-Model Effective TC Results.

6.0 Package Level ThetaJB Results

With the C4/C5 effective thermal conductivity values determined, our attention is now directed to the overall package level thermal resistance determination. In that regard, Table 4 details the ThetaJB results for the two package level scenarios

considered. While figure 10 illustrates the package level temperature contour plot for the IBM case. As expected, ThetaJB is strongly dependent on the C5 thermal resistance, assuming an "idealized" 25˚C infinite sink PWB boundary condition. Although not mentioned previously, the F/C die configuration affords an additional thermal path through the backside of the die (primary path in PC apps). In the present analysis, the die backside surface was taken as adiabatic, which is understandable in terms of weight savings for most aerospace applications.

Silicon Die Size	C4 Pitch	90% Al_2O_3 Pkg Size	CGA Interconnect Style	C5 Pad I/O	C5 Pitch	Θ_{JB} (C/W)
15 mm sq.	225 um, with outer six rows being hex	45 sq. x 1.5 mm	IBM	1936 (44x44)	1.0 mm	1.36
			6σ			1.05

Table 4: Finite Element Global Model Results.

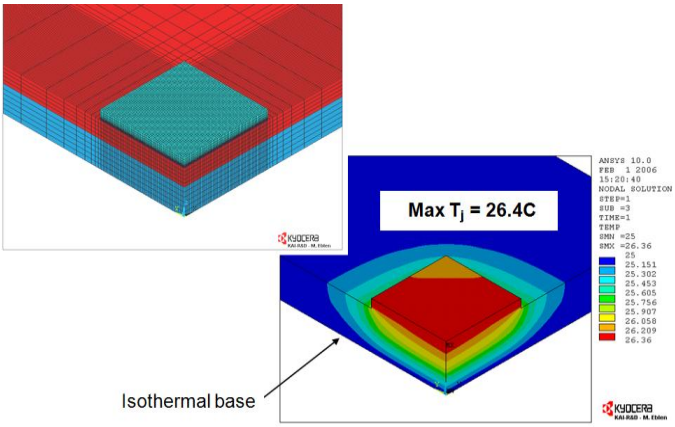


Fig. 10: Typical Global Model Results [13].

If a numerical/FE software program is not readily available to calculate the package level ThetaJB metric; the previously derived sub-model k_{eff} values can still be of utility if used in conjunction with a closed-form thermal spreading resistance equation. In order to contrast this approximation with the previously described FE numerical approach it shall be referred to as the "analytical approach". A popular extension of the original Kennedy derived spreading resistance expression [14], easily implemented in a spreadsheet is the so-called SLA equation [15-16]. Authors, Song and Lee, demonstrated that for most microelectronic "one spreading layer" examples considered, the errors are small and typically less than 5%. Their approximate closed-form analytical solution is presented as Equation 5. All other series summation thermal resistance terms required for ThetaJB are the conventional 1D approximations, less the C5 cuboid layer discussed later. Noteworthy is the electronics industry convention to use the capital Greek letter theta "Θ" instead of the thermal sciences preferred capital letter "R" for thermal resistance notation. The latter style is adopted here for consistency with the published references.

$$R_{sp} = \frac{\sqrt{A_b} - \sqrt{A_s}}{k_b \sqrt{\pi A_b A_s}} \times \frac{\lambda k_b A_b R_{bc} + \tanh(\lambda t)}{1 + \lambda k_b A_b R_{bc} \tanh(\lambda t)} \qquad (5)$$

where :

$$\lambda = \frac{\pi^{\frac{3}{2}}}{\sqrt{A_b}} + \frac{1}{\sqrt{A_s}}$$

A_b = heat spreader area

A_s = heat source area (die)

t = heat spreader thickness

k_b = heat spreader thermal conductivi ty

R_{bc} = thermal resistance for spreader boundary condition. This term is set to zero for isothermal , else equals the convection coefficien t resistance $(\bar{h} \times A_b)^{-1}$.

In order to demonstrate the utility of Equation 5, the calculated package level thermal resistance was compared with the FE model predicted in Table 4. As noted earlier, a major difficulty encountered with the analytical ThetaJB approach is determination of the appropriate 1D area to use with the C5 layer. Thermal spreading from the die to substrate has already been captured in equation five. A useful and pragmatic approximation under isothermal PWB conditions and low substrate thermal conductivity is to assume the interconnect area conducting heat is 1.5X the longest die length squared. In order to place the afore mentioned supposition on a theoretically more rigorous footing, the A_b term in equation five can used to bound the upper limit. The solution of which will provide a data set with the trivial result of zero spreading at $A_s = A_b$ and asymptotic at $A_b \geq 30$ mm. Intuitively, this behavior is just a restatement of the premise that thermal spreading (i.e. area

enlargement) improvements are finite after a certain dimension. The analytically calculated ThetaJB metrics for the IBM and 6σ cases were 1.22 and 0.97 C/W respectively. Compared with Table 4 values, the analytical values are quite close. Of course, caution is again warranted when employing this method, as many factors should be considered. Another option, albeit more mathematically concise and not expanded on here, is the two-layer infinite series equation programmed into a software applet provided online by University of Waterloo Microelectronics Heat Transfer Lab [17].

7.0 Conclusions

The effective thermal conductivity of Six Sigma's copper reinforced interconnect was found to be approximately 75% higher versus the equivalent IBM high lead CGA via finite element modeling. This improvement translated into approximately a 30% lower junction-to-board or Θ_{JB} thermal resistance in a large substrate/die aspect ratio microelectronic ceramic package. A closed-form thermal-spreading resistance solution methodology for calculating Θ_{JB} was also discussed in lieu of a numerical methodology. Caution was warranted with this approach, as calculation errors can be large.

Acknowledgments

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