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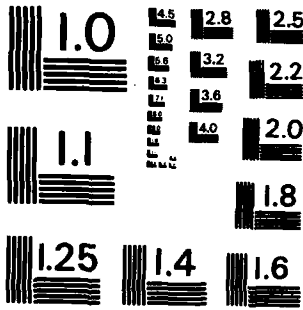

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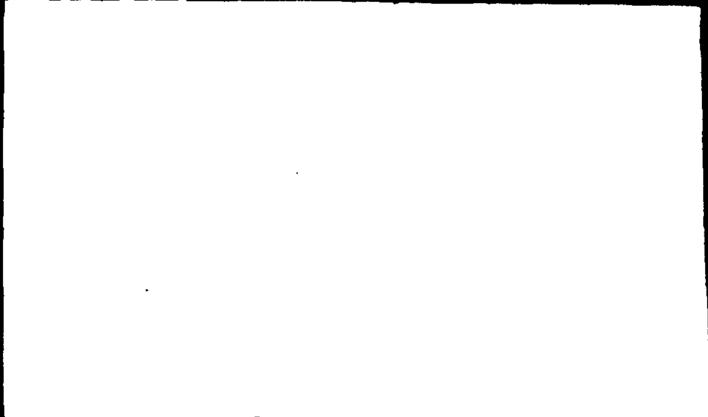

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HETEROJUNCTION SOLID-STATE DEVICES FOR MILLIMETER-WAVE SOURCES

October 1983

Final Report
September 1, 1980 - August 31, 1983

U.S. Army Research Office
DAAG29-80-K-0080

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The use of compound semiconductor and heterojunction devices as millimeter-wave sources through 100 GHz has been investigated. Both IMPATT and MESFET type devices have been considered. A series of comprehensive and accurate theoretical device models have been developed and utilized in this investigation. Both equilibrium and nonequilibrium transport effects have been investigated. Prototype IMPATT device structures have been fabricated in GaAs and GaInAs/InP.

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HETEROJUNCTION SOLID-STATE DEVICES FOR MILLIMETER-WAVE SOURCES

Final Report on

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by

R. J. Trew
Electrical and Computer Engineering Department
North Carolina State University
Raleigh, NC 27650

ABSTRACT

This report summarizes the work performed during the last three years on an ARO sponsored contract with NCSU for the purpose of investigating the potential of compound semiconductor and heterojunction devices for millimeter-wave sources. Both two-terminal IMPATT and three-terminal MESFET structures were considered. A series of theoreticl device models were developed and used to investigate device performance. Non equilibrium effects were considered with the use of a theoretical Monte Carlo transport model. Prototype IMPATT devices were fabricated from GaInAs/InP grown by LPE and GaAs layers grown by MBE and OM-CVD. The results of this program indicate that compound semiconductors should be useful for millimeter-wave sources. In particular, both GaAs and InP IMPATTs should be capable of conversion efficiency exceeding 10% at 100 GHz. Three-terminal MESFET devices fabricated from InP, GaInAs and GaInAsP should be capable of producing useful gain through at least 60-70 GHz. With sub-half micron gate-lengths, the upper frequency of these devices could possibly reach 100 GHz.

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I. SUMMARY OF WORK

The purpose of this research program was to investigate the use of compound and heterojunction semiconductor devices for use as millimeter-wave sources. Both two-terminal IMPATT devices and three-terminal FET type devices were considered. The program consisted of both theoretical and experimental efforts.

A series of comprehensive and accurate theoretical device models were developed and used to investigate the high-frequency potential of devices fabricated from various compound semiconductors. IMPATT devices fabricated from GaInAs/InP, InP, GaAs and Si were investigated and predicted performance compared. Device performance was investigated from the low microwave region to over 100 GHz. In general, our studies indicate that GaAs is the optimum material for maximizing device efficiency to a frequency of about 40 GHz, InP works best from about 40 GHz to 60 GHz and Si produces the greatest efficiency for operation above 100 GHz. The use of heterojunction devices such as GaInAs/InP shows considerable potential for device development and should be further investigated. In the structure we investigated the GaInAs layer was used to reduce the contact resistance to the p-type InP. Such a structure should allow the attractive properties of InP for high-frequency operation to be exploited. Our studies indicate that conversion efficiency greater than 10% should be obtainable at 100 GHz from devices fabricated from both GaAs and InP. Doping profile control, however, is critical and growth technology such as MBE and/or OM-CVD will be required.

Our large-signal, numerical IMPATT device simulations are the first to predict from basic transport phenomenon device conversion efficiency for GaAs Read-profile devices greater than 20% at Ka-band. Raytheon has reported such conversion efficiency for experimental Read-profile devices and previous

theoretical calculations have not been able to achieve the experimentally reported results. Our results are due to an improved method for determining semiconductor material parameters. We use a theoretical Monte Carlo materials simulation program to determine the required parameters. This technique provides a method for investigating various semiconductors and examining material potential. Using this technique we have obtained excellent agreement between the theoretical results and experimentally reported device performance.

A MESFET device model has been developed and used to study the high-frequency operation of three-terminal compound semiconductor devices. Various semiconductors have been investigated including GaAs, InP, GaInAs, GaInAsP, and AlInAs. Generally we find that a high saturation velocity is required for high gain and a high low-field mobility is required for low noise figure. Although InP is capable of high gain it suffers from high noise performance. The optimum material for high frequency FET type devices appears to be GaInAs. At 40 GHz a GaInAs transistor is capable of about 2 db more gain than a comparable GaAs device. In general, our studies indicate that MESFET devices with half-micron gate lengths should be useful to about 60-70 GHz. Quarter micron gate length devices could possibly provide useful gain as high as 100 GHz. For operation above 70 GHz, however, novel device structures need to be investigated and developed.

High-frequency, nonequilibrium transport effects have been investigated with theoretical Monte Carlo device simulations. These calculations have helped provide insight into velocity overshoot and ballistic transport phenomena. We find that ballistic or near-ballistic transport effects are not likely to result in improved device performance. Our studies of the planar-doped barrier transistor, for example, reveal that this device is not

capable of performance comparable to that achieved from standard submicron gate FETs. Nonequilibrium effects, however, may lead to novel device structures. For example, the "ensemble effect" revealed in our calculations (see paper 9 in the appendix) can be used to increase the average carrier velocity. By using multiple acceleration regions high average velocity over a significant distance can be maintained. This subject is currently being examined in more detail.

Experimentally, we have grown epitaxial semiconductor layers of GaAs by MBE and OM-CVD, and InP and GaInAs by OM-CVD and LPE. These layers have been used for both characterization and device fabrication. We have fabricated GaAs IMPATT diodes from MBE and OM-CVD material and GaInAs/InP devices from LPE material. These diodes are being tested in a waveguide oscillator circuit and their performance will be compared to commercial GaAs and Si diodes. We have developed the facilities to completely RF characterize the devices.

Circuit design work has also been supported on this contract. Our efforts have concentrated upon the development of circuit design techniques that will optimize component performance in terms of gain-bandwidth tradeoffs and parameter insensitive design. This work is summarized in the publications attached to this report.

II. GRADUATE STUDENTS

The following graduate students have been totally or partially supported by the ARO on this contract:

1. J. M. Golio, Ph.D. awarded Spring 1983.
   Thesis title: Ion-Implanted MESFETs

2. A. N. Riddle, M.S. awarded Spring 1983

3. R. T. Neece, M.S. awarded Fall 1983

4. G. W. Rhyne, M.S. expected Spring 1984

5. P. M. Mock, Ph.D. in progress
   Thesis topic: Millimeter-wave IMPATT Devices

6. M. A. Tischler, Ph.D. in progress
   Thesis topic: Novel High-Velocity Millimeter-Wave Devices

In addition, Dr. M. Steer, a Visiting Assistant Professor at NCSU, was supported during the summer of 1983 on this project.

III. PUBLICATIONS

A total of fourteen papers have been submitted for publication on this project. Of these, twelve have been accepted and two are currently pending. Reference information is listed below and copies of the papers are provided in the appendix.

1. J. M. Golio and R. J. Trew, "Optimum Semiconductors for High-Frequency and Low-Noise MESFET Applications," to be published in IEEE Trans. Electron. Dev., October 1983.

2. M. A. Littlejohn, R. J. Trew, J. R. Hauser, and J. M. Golio, "Electron Transport in Planar-Doped Barrier Structures Using an Ensemble Monte Carlo Method," J. Vac. Sci. Technol. B1(2), pp. 449-454, April-June 1983.

3. A. N. Riddle and R. J. Trew, "A Broad-Band Amplifier Output Network Design," IEEE Trans. Microwave Theory Tech., vol. MTT-30, pp. 192-196, February 1982.

4. A. N. Riddle and R. J. Trew, "Parameter Insensitive Matching Circuits for Low Cost Integrated Circuits," 1983 IEEE MTT-S Digest, pp. 521-523.

5. J. M. Golio and R. J. Trew, "Profile Studies of Ion-Implanted MESFETs," 1983 IEEE Millimeter-Wave Monolithic Integrated Circuits Symposium Digest, pp. 22-26.

6. Y. Takeda, M. A. Littlejohn, J. A. Hutchby and R. J. Trew, "Electron Concentration and Alloy Composition Dependence of Hall Factor in GaInAsP," Electronics Lett., vol. 17, pp. 686-688, September 1981.

7. A. N. Riddle and R. J. Trew, "Odd Order Impedance Matching Networks for Low Cost Microwave Integrated Circuits," 1983 IEEE MTT-S Digest, pp. 459-461.

8. Y. Takeda, M. A. Littlejohn, R. J. Trew and J. A. Hutchby, "Effects of Two Longitudinal Optical-Phonon Modes on Electron Distribution in GaInAsP," Appl. Phys. Lett., vol. 40, pp. 836-838, May 1982.

9. R. J. Trew, R. Sultan, J. R. Hauser and M. A. Littlejohn, "Ensemble Monte Carlo Studies of High Field Spikes and Planar Doped Barrier Devices," accepted for publication in the Proc. on the 1982 Workshop on the Physics of Submicron Structures, Plenum Press.

10. J. M. Golio and R. J. Trew, "Profile Studies of Ion-Implanted MESFETs," to be published in the IEEE Trans. Microwave Theory Tech., January 1984.

11. J. M. Golio, G. N. Maracas, D. Johnson, R. J. Trew and N. A. Masnari, "A Technique for Modeling Ion-Implanted GaAs MESFETs in the Presence of Deep Levels," to be published in the Proc. of the 1983 Cornell Conf. on High Speed Semiconductor Devices and Circuits.

12. J. M. Golio, R. J. Trew, G. N. Maracas and H. Lefevre, "A Modeling Technique for Characterizing Ion-Implanted Material Using C-V and DLTS Data," accepted for publication in Solid-State Electronics.

13. A. N. Riddle and R. J. Trew, "A New Method of Tolerance Enhancement for Filters and Amplifier Matching Networks," submitted to IEEE Trans. Microwave Theory Tech.

14. A. N. Riddle and R. J. Trew, "A Theory of Even and Odd Order Low-Pass Impedance Matching Filters," submitted to IEEE Trans. on Circuits and Systems.

APPENDIX

Optimum Semiconductors for High-Frequency and Low Noise MESFET Applications*

J. M. Golio and R. J. Trew
Electrical Engineering Department
North Carolina State University
Raleigh, NC 27650

ABSTRACT

An analytic MESFET device model has been used to study the optimum velocity-field characteristics of materials that are potentially useful for millimeter-wave and low-noise MESFET applications. Materials of current interest have been characterized and compared. Results explain the relative importance of parameters such as low-field mobility and saturated velocity. Differences between GaAs and Si performance are explained and a number of attractive compound semiconductors for high-frequency and low-noise device fabrications are indicated.

* This work was partially supported by Rockwell International and partially supported by the Army Research Office, under Contract No. DAA G29-80-K-0080.

INTRODUCTION

The GaAs MESFET has been utilized in a variety of low-noise applications at microwave and millimeter-wave frequencies. Although GaAs performance has been demonstrated beyond 30 GHz with corresponding minimum noise figures of about 4.5 dB (1,2), such operation appears to be approaching a limit for practical operation of GaAs MESFET devices. For this reason, interest in the use of other compound semiconductors is growing. Recently, special interest has been given to both InP (3,4,5,6) and $Ga_{.47}In_{.53}As$ (7,8,9). The initial work with these semiconductors has been encouraging.

The purpose of this work is to determine which materials are most likely to result in optimum millimeter-wave and low-noise MESFET performance. The frequency and noise properties of these devices has been examined as a function of electron low-field mobility and high-field velocity. To accomplish this, a one-dimensional analytic model similar to the one reported by Pucel et al. (10) has been employed.

MODEL ASSUMPTIONS AND TECHNIQUE

The model used in this work assumes that the electron transport properties of a material can be simulated by a two-piece velocity-field relationship. The two-piece approximation (Figure 1) is defined from a theoretical velocity-field characteristic determined by Monte Carlo techniques.

For electric fields less than an appropriate saturation field, E_m, the electron velocity is described by a linear expression,

$$v = \mu_o E.$$

For electric fields above E_m the electrons move at a constant, maximum velocity, v_m. The velocity-field curves for several materials are compared in Figure 2. Using this information, a small-signal equivalent circuit can be determined and analysed to obtain RF performance predictions, including power gain and noise figure as a function of frequency.

For the first part of this study the theoretical model was used to determine the relative importance of low-field mobility and high-field velocity on MESFET performance. In particular, a one-micron gate length geometry was assumed and the magnitudes of these semiconductor properties were varied. Other material and geometric properties of the device remained constant. The effects that low-field mobility and maximum velocity have upon device figures of merit were thus determined.

In the second part of the study, materials were characterized according to their Monte-Carlo predicted properties. The Monte Carlo simulations used for this work have been well documented and are in excellent agreement with experimental measurements (11,12).

Low-field mobility for the various materials of interest is obtained directly from Monte Carlo data. Determining the appropriate maximum velocity for materials is more involved.

The importance of developing a systematic, well-justified technique for determining v_m has been discussed in earlier work (13) and in this study, such a method has been developed. The method involves numerical determination of the carrier transit time under the gate using an exact velocity-field relationship. It is then required that the transit time calculated assuming a two-piece approximated velocity-field relationship be equal to that of the exact analysis. This method yields a v_m for GaAs (doped to a level $N_D = 10^{17} cm^{-3}$) in excellent agreement with the value obtained by Pucel (10). Table 1 gives values for both low-field mobility and maximum velocity determined in this way for several important materials. Note that both of these material parameters will be doping dependent.

The relative importance of low-field mobility and maximum velocity upon high-frequency and noise performance was investigated by independently varying these parameters and computing the gain-bandwidth product and minimum noise figure. The gain-bandwidth product, f_T, is a commonly quoted figure of merit for high-frequency devices and can be defined from first-order considerations as

$$f_T = g_m/2\pi C_{gs}$$

where g_m is the device transconductance and C_{gs} is the gate-source capacitance. The minimum noise figure computation is developed after Pucel et al. (10) and represents the minimum theoretical noise of the intrinsic device. Since such noise sources as circuit losses and defect states are ignored, the minimum noise figures here are somewhat lower than those measured for 1μm GaAs devices today.

RESULTS

The variations of f_T and NF_{min} with low-field mobility is presented in Figure 3. The data for the f_T curves is for devices biased with $I_D=I_{DSS}$, while the NF_{min} data is biased for minimum noise figure. Note that as μc is increased, the predicted device gain-bandwidth product increases rapidly for values below about 2000 $cm^2/v{\cdot}sec$. For values in excess of this limit, little or no improvement is observed. This information helps to explain why the frequency response for GaAs is much greater than that for Si, while further increases in mobility might yield little improvement in that area. Note, however, that increased mobilities do continue to significantly decrease the predicted minimum noise figure

The variations of gain-bandwidth product and minimum noise figure with increasing maximum velocity is presented in Figure 4. The increase of f_T with v_m is almost linear showing an order of magnitude increase in f_T with

a corresponding increase in v_m. High maximum velocity semiconductors are therefore the most desirable for improved high-frequency performance. It should be noted, however, that in the range of maximum velocity for practical semiconductors (i.e. $1x10^7$ - $2x10^7$ cm/sec) very little improvement in minimum noise figure is made.

Finally, the material parameters corresponding to the III-V compounds of Table 1 were used to simulate a 0.5 m gate length device. Maximum velocity and low-field mobility were determined as outlined above, while the remaining necessary parameters were determined as described in reference (13). The devices were examined at two different bias levels: biased for minimum noise figure and biased for a drain current of 10 mA. Figure 5 illustrates the available gain of the devices when biased for I_D=10mA and the noise figure when biased for minimum noise figure. Refering to Table 1, it can be seen that ranking of materials by superior gain predictions corresponds exactly to the ranking by highest maximum velocity, while the materials which show superior noise properties are those with highest low-field mobility.

CONCLUSIONS

In conclusion, a number of semiconductor compounds have been characterized and compared. The relative importance of the transport properties as described by low-field mobility and saturation velocity has been examined. The results indicate that for optimum high-frequency response, high-field particle velocity is more critical than low-field mobility. Thus, a material such as InP may be favored. Similarly, for optimum low-noise performance, it is low-field mobility which seems to be most influential. Therefore, a material such as $Ga_{.47}In_{.53}As$ may be preferred.

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Table 1: Low-field mobility, μ., and saturation velocity, vm, for several materials. Values are appropriate for 1 μm devices doped to a level $N_D = 10^{17} cm^{-3}$.

Material	$\mu_o (cm^2/v \cdot sec)$	$vm (10^7 cm/sec)$
Si	500	1.00
Ga As	4660	1.30
InP	3490	1.84
$Ga_{.47}In_{.53}As$	8900	1.31
$Al_{.47}In_{.53}As$	5050	0.99

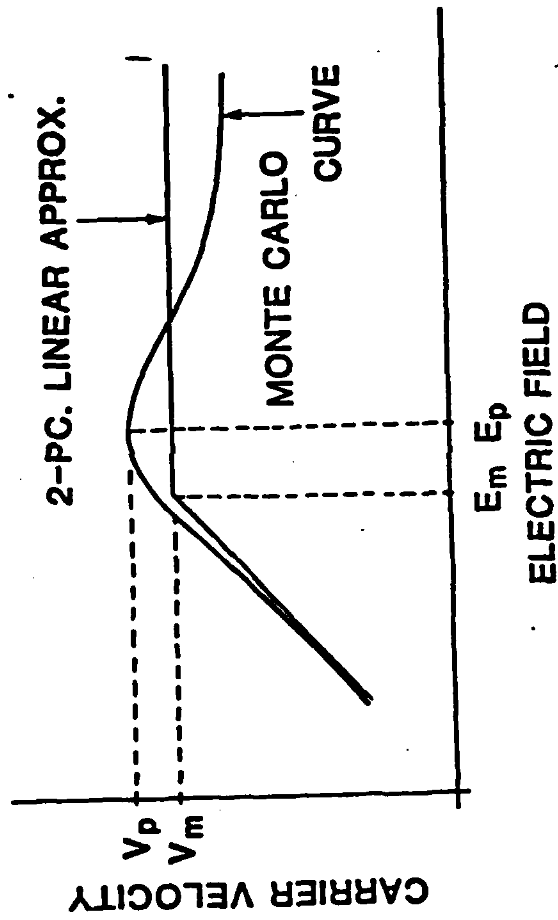
Figure 1 Carrier velocity as a function of electric field for GaAs doped to $N_D = 10^{17} cm^{-3}$.

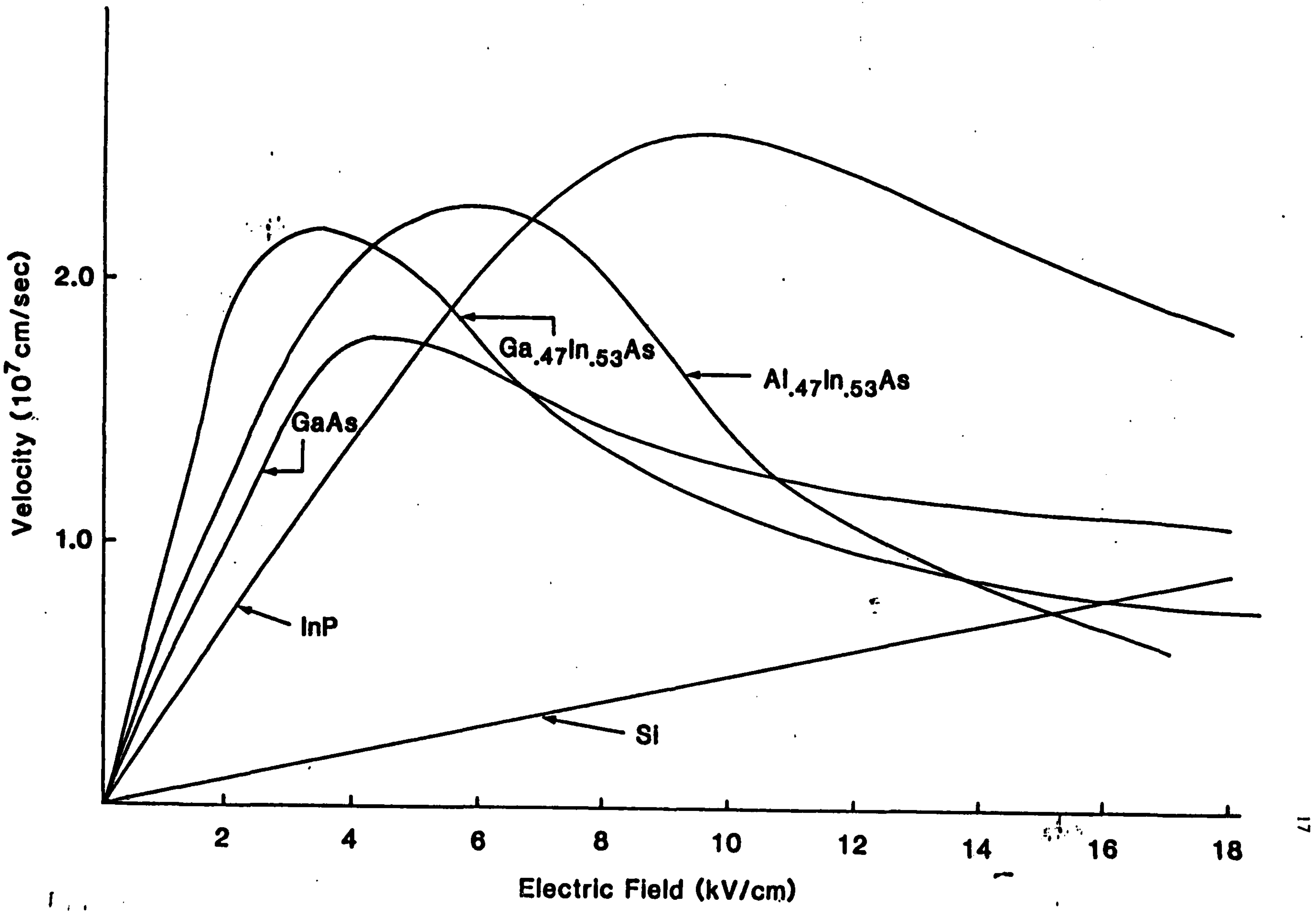
Figure 2 Static velocity - field characteristics for a number of semiconductors of interest. The doping level is $N_D = 10^{17}$ cm^{-3}.

Figure 3 Model predictions of gain-bandwidth product and minimum noise figure as a function of low-field mobility. Other material parameters used are appropriate to GaAs doped to $N_D = 10^{17}$ cm^{-3}.

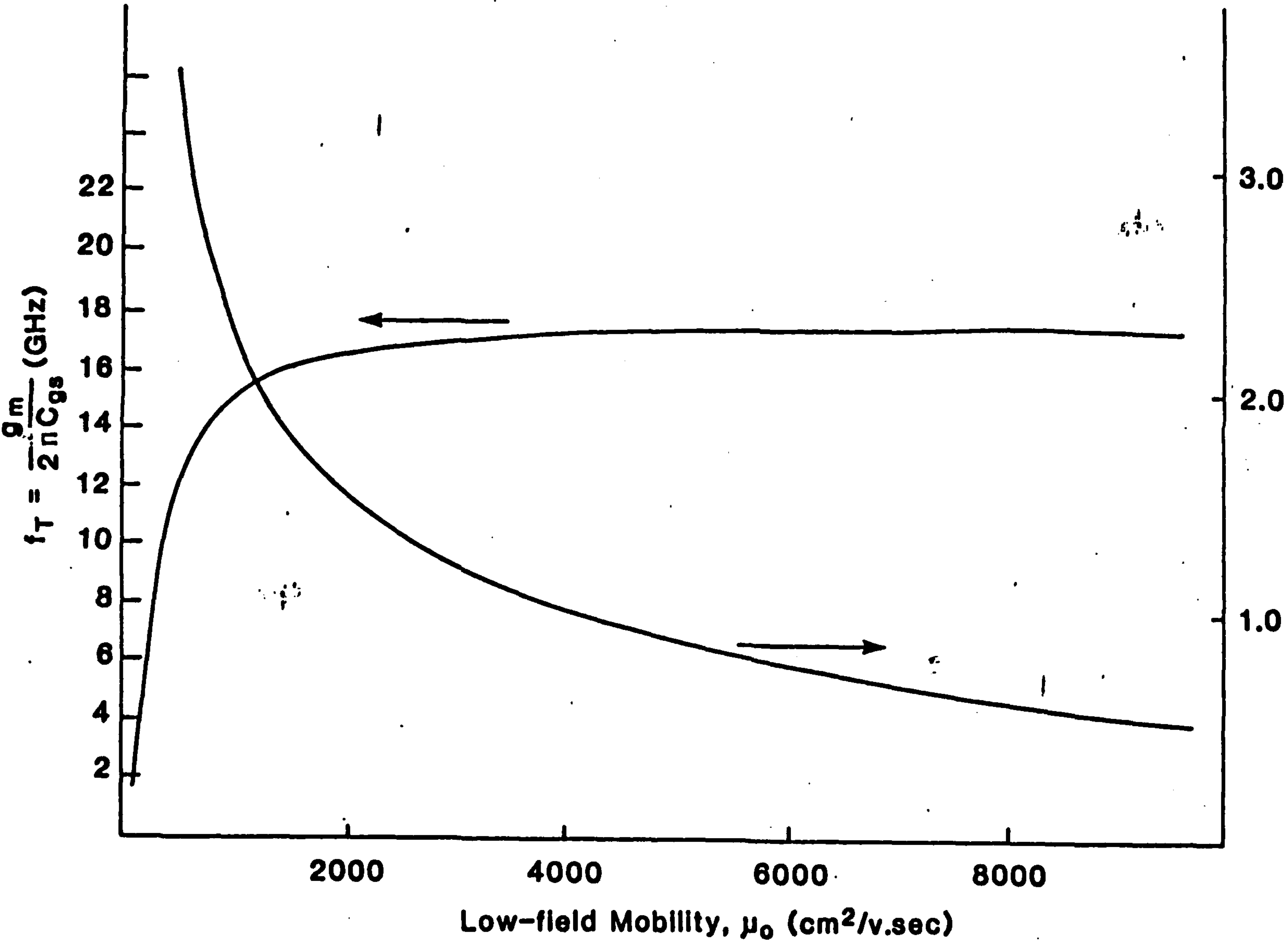
Figure 4 Model predictions of gain-bandwidth product and minimum noise figure as a function of maximum velocity. Other material parameters used are appropriate to GaAs doped to $N_D = 10^{17}$ cm^{-3}.

Figure 5 Model results of minimum noise figure and available gain as a function of frequency for several materials of current interest. The noise figure data is for devices biased to obtain minimum noise figure, and the available gain information is for devices biased at $I_D = 10$ mA.

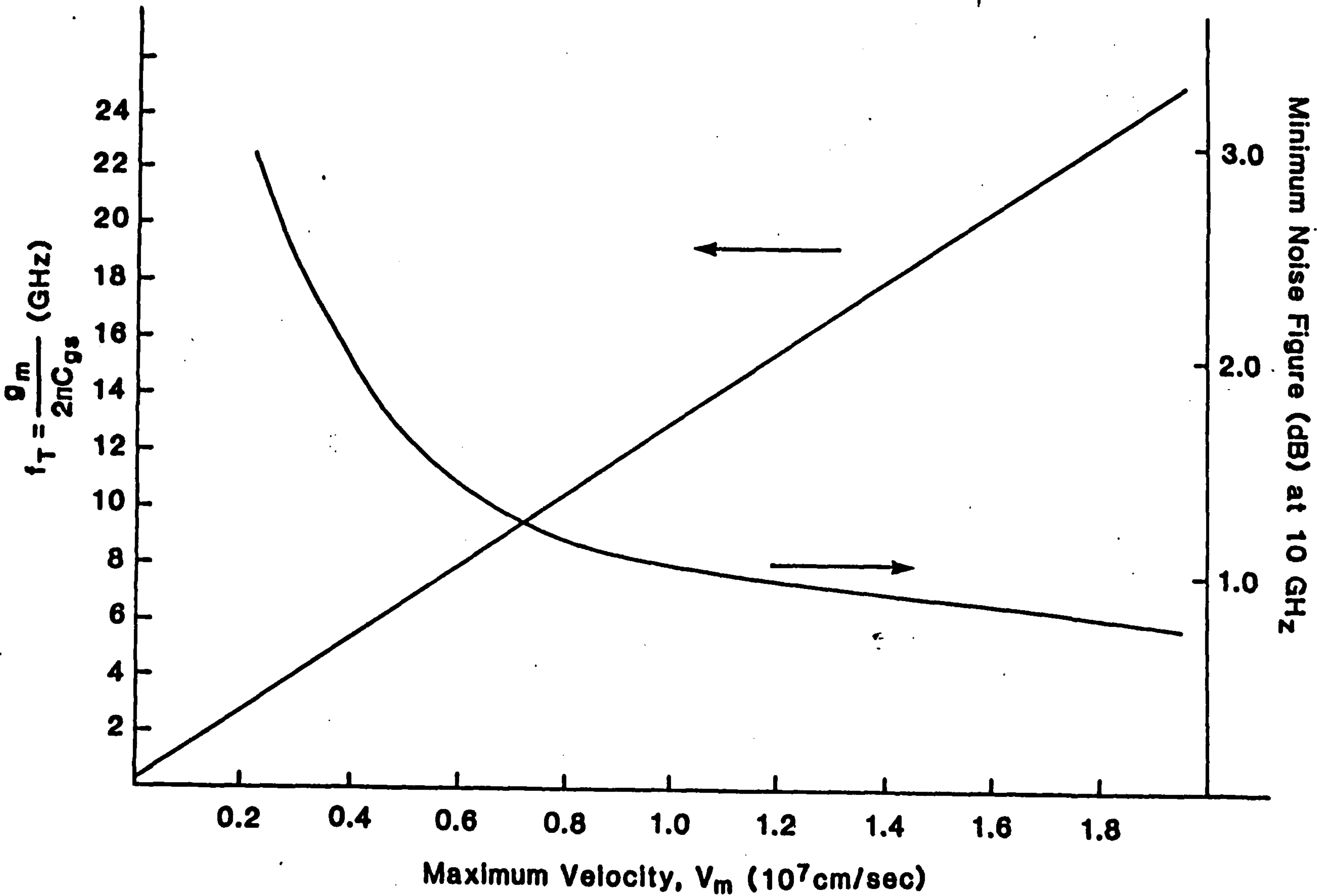

2-PC. LINEAR APPROX.
MONTE CARLO CURVE
E_m E_p
ELECTRIC FIELD
V_p
V_m
CARRIER VELOCITY



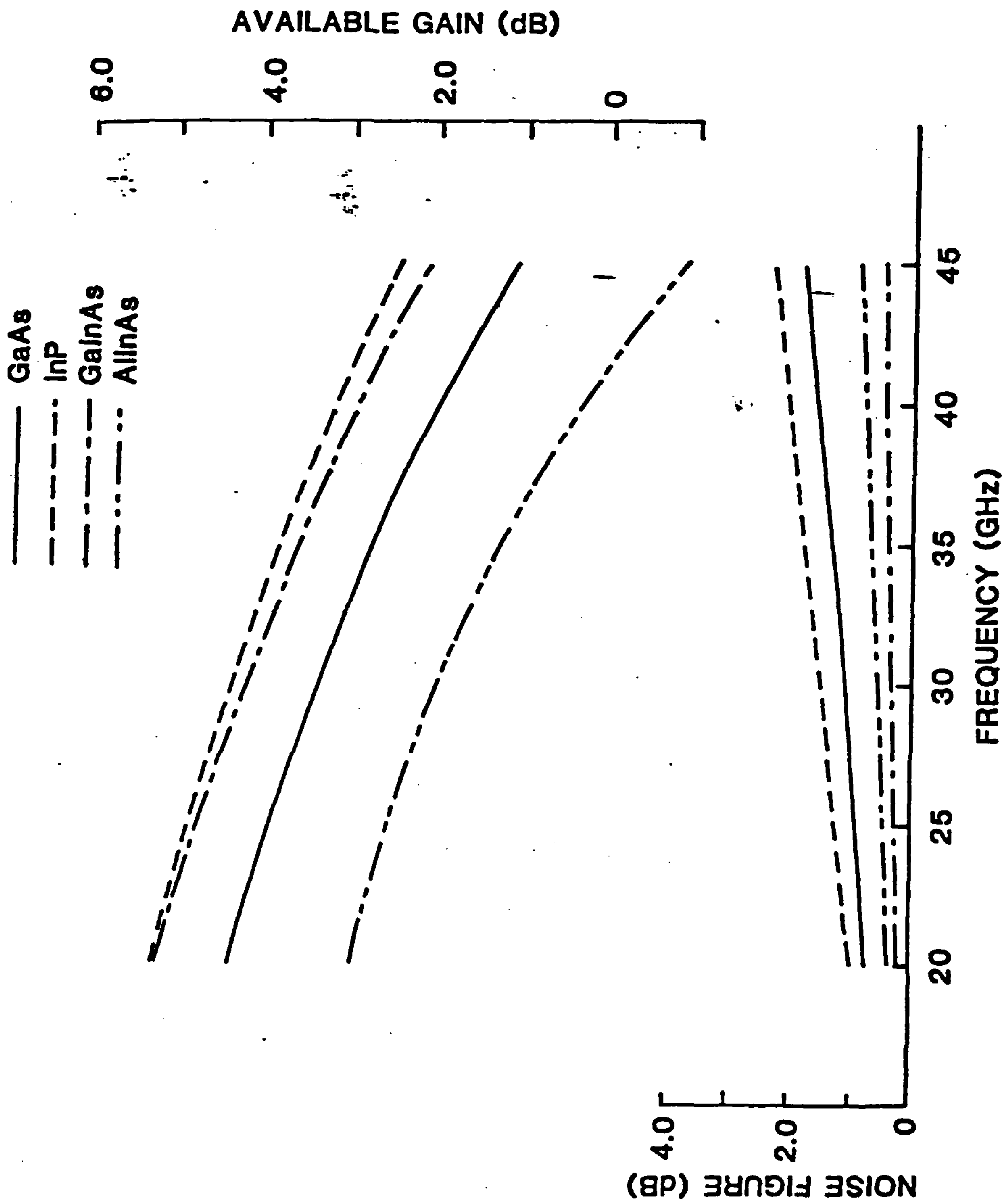
Velocity (10^7 cm/sec)
2.0
1.0
GaAs
InP
Si
Ga.47In.53As
Al.47In.53As
2
4
6
8
10
12
14
16
18
Electric Field (kV/cm)



$f_T = \frac{g_m}{2\pi C_{gs}}$ (GHz)
22
20
18
16
14
12
10
8
6
4
2
2000
4000
6000
8000
Low-field Mobility, μ_o (cm^2/v.sec)
Minimum Noise Figure (dB) at 10 GHz
3.0
2.0
1.0



$f_T = \frac{g_m}{2\pi C_{gs}}$ (GHz)
24
22
20
18
16
14
12
10
8
6
4
2
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
Maximum Velocity, V_m (10^7 cm/sec)
Minimum Noise Figure (dB) at 10 GHz
3.0
2.0
1.0



AVAILABLE GAIN (dB)
6.0
4.0
2.0
0
GaAs
InP
GaInAs
AlInAs
FREQUENCY (GHz)
20
25
30
35
40
45
NOISE FIGURE (dB)
4.0
2.0
0

Electron transport in planar-doped barrier structures using an ensemble Monte Carlo method[a)]

M. A. Littlejohn, R. J. Trew, J. R. Hauser, and J. M. Golio

Department of Electrical Engineering, North Carolina State University, Raleigh, North Carolina 27650

(Received 6 December 1982; accepted 11 January 1983)

An ensemble Monte Carlo method is used to simulate electron transport through narrow high field regions which occur in planar-doped barrier devices. These structures can achieve average velocities substantially higher than the static drift velocity corresponding to average electric field. Increased velocities in these structures arise primarily from two physical mechanisms. These mechanisms are (1) velocity overshoot and related ensemble hot electron effects, and (2) an ensemble effect due to the collecting nature of the low field/high field boundary, which is not due to hot electrons. Ballistic-like transport can occur through narrow high field spikes. However, ballistic transport is not the major contributor to high ensemble average velocities due to scattering in regions adjacent to the high field spike. Ensemble average velocities at a given point in a device are influenced by the field distribution ahead of this point as well as that behind it.

PACS numbers: 73.40.Lq, 85.30.Mn

I. INTRODUCTION

The study of transport in semiconductors on short time ($t \simeq 1$ ps) and distance ($x \simeq 0.1$ μm) scales has identified velocity overshoot[1-6] and ballistic transport[5-9] as potential mechanisms for increasing carrier velocity. Such studies receive impetus from advances in lithography and materials growth techniques, as well as the desire to realize innovations and improvements in high speed, high frequency devices.

The planar-doped barrier is a majority carrier rectifying structure which is potentially capable of high speed applications based on hot electron transport phenomena.[10-13] Since majority carrier transport occurs over dimensions less than 0.1 μm and through narrow high field spikes, the planar-doped barrier can possibly exhibit both velocity overshoot and ballistic transport. Other ensemble effects not specifically due to hot carriers can also enhance the dynamic velocity response.[13] The purpose of this paper is to discuss transport mechanisms in planar-doped barriers using data obtained from ensemble Monte Carlo simulations. The results suggest that the dominant transport effects are velocity overshoot and ensemble effects due to the low field/high field boundaries and the field distribution.

II. TRANSPORT MODEL

The details of the ensemble Monte Carlo method have been described previously.[4] The capability to include nonuniform spatially varying electric field distributions has been incorporated into the Monte Carlo procedure.[14,15] In this paper, we employ a series of electric field "steps," which represent the ideal field distribution in a planar-doped barrier transistor.[11]

The planar-doped barrier is an n^+–n–p^+–n–n^+ structure grown by molecular beam epitaxy.[10,12] The p^+ region is thin enough to be depleted of free carriers. Also, the lightly doped n regions are negligibly doped compared to the p^+ region. The negative charge in the p^+ layer is neutralized by positive bound charge in the two heavily doped n^+ regions. If an impulse charge density is assumed, the resulting step electric field distribution leads to a triangular electron potential energy barrier in the conduction band. Current flow through the barrier is asymetrical with applied voltage when the two n regions have different widths.

Two barriers can be connected to form a three terminal planar-doped barrier transistor.[11,12] The field profile for an ideal planar-doped barrier transistor is shown in Fig. 1. Typical dimensions are specified. The base width is 0.2 μm, the emitter-base junction width is 0.25 μm, and the collector-base junction width is 0.45 μm. The area charge density is 5.5×10^{-8} C/cm^2 for the emitter-base junction p^+ acceptor plane, and 3.8×10^{-8} C/cm^2 for that of the collector-base junction. Figure 1 also shows the field profile which results from an emitter-base forward bias of 0.15 V and a collector-base reverse bias of 0.3 V. The equilibrium barrier heights are 0.2 eV for the emitter-base junction and 0.15 eV for the collector base junction.

III. SIMULATION OF A PLANAR-DOPED BARRIER TRANSISTOR

Field profiles of the form shown in Fig. 1 are used in the simulations. An ensemble of electrons (typically 2000–10 000) is released at $x = 0$. This ensemble is transported across the transistor to the collector boundary. During transport, the electrons undergo scattering according to the normal GaAs scattering mechanisms.[4] The region $0 < x < L$ is subdivided into equally spaced regions of width $\Delta x = L/M$, where M is typically 100. Smaller spacings are used for the very narrow field spikes. Each particle in the ensemble is tracked and the ensemble average velocity in each Δx bin is accumulated. A particle reaching the collector-base junction with a kinetic energy lower than the collector-base barrier height is removed from the ensemble. A particle can initially traverse the collector-base barrier and then be backscattered into the base. If such a particle approaches the collector-base barrier again with less kinetic energy than the barrier height, it is then removed from the ensemble. Thus, the ensemble average velocity of particles which reach the collector is

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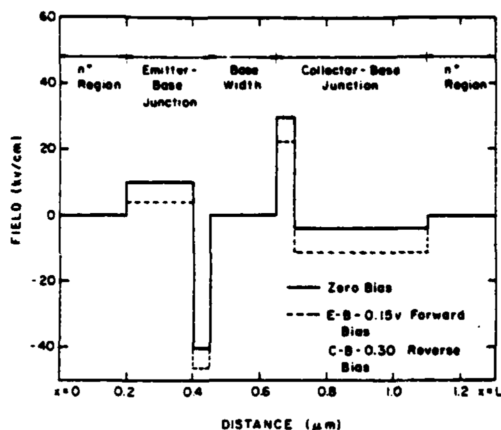

FIG. 1. Electric field distribution vs distance in an ideal planar-doped barrier transistor with and without bias voltages.

TABLE I. Calculated values of transit time (τ), $f=(2\pi\tau)^{-1}$, and ratio of the number of carriers collected to the number lost in the base (N_C/N_B) for two values of collector-base barrier height (ϕ_{BC}).

Base width (Å)	$\phi_{BC}=0.11$ eV τ(ps)	$(2\pi\tau)^{-1}$ (GHz)	N_C/N_B	$\phi_{BC}=0.16$ eV τ(ps)	$(2\pi\tau)^{-1}$ (GHz)	N_C/N_B
2000	6.1	26.1	1.5	6.3	25.3	3.0
1000	5.3	30	3.3	5.6	28.4	6.7
250	4.8	33.2	17	5.1	31.2	31

computed. Unless otherwise stated, all calculations presented will be for GaAs with material parameters used previously.[4]

Figure 2 [curve (a)] shows ensemble average velocity for a planar-doped barrier transistor with 1000 Å base width and 300 Å widths for the emitter and collector high field spike regions. For convenience, the indicated field polarity is positive downward in this and subsequent figures. Also, the emitter-base and collector-base barrier heights are 0.21 and 0.05 eV, respectively and the n^+ regions illustrated in Fig. 1 are assumed to have zero thickness for these simulations. In Fig. 2, there are four regions of interest. The first is the region prior to the emitter-base high field spike where the velocity rapidly rises to above 2×10^7 cm/s. The second is the region within the emitter-base high field spike where the velocity rapidly rises to between $(3–4)\times10^7$ cm/s and then falls to below 2×10^7 cm/s. The third region is the base where the velocity varies slightly, and the fourth region is the base-collector junction where the velocity is well above 2×10^7 cm/s for over 0.1 μm. The details of these regions will be discussed in the next section. Also, curve (c) in Fig. 2 shows the ensemble velocity for a transistor with a base width of 250 Å (all other parameters remain fixed). The results are similar to curve (a), with the velocity in the base increasing to above 2.5×10^7 cm/s in this case.

Using data of the type shown in Fig. 2, the transit time τ across the device has been calculated as a function of base width. Values of τ are shown in Table I for two different values of collector-base barrier height. Also shown in Table I is the value of $f=(2\pi\tau)^{-1}$. While f is not the true cut-off frequency for the device, it represents a lower bound to the cut-off frequency. The values of τ in Table I properly reflect the emitter- and base-transit times. However, the actual collector transit time will be shorter. Thus, GaAs planar-doped barrier transistors should operate above 30 GHz with base widths less than 0.1 μm. Table I also shows corresponding values of N_C/N_B, where N_C is the number of carriers reaching the collector and N_B is the number with insufficient energy to cross the base-collector barrier. The values of N_C/N_B can be equated with the d-c common emitter current gain based on a simple transport model.[13] In the simulations, current gain greater than ten can be achieved in planar-doped

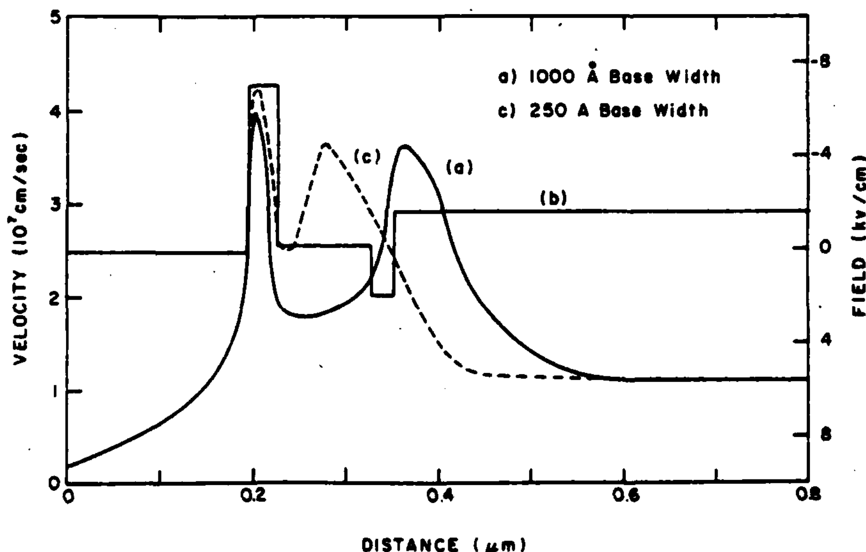

FIG. 2. Ensemble average velocity [curve (a)] and electric field distribution [curve (b)] vs distance for a GaAs planar-doped barrier transistor with a base width of 1000 Å. Curve (c) shows ensemble average velocity for a device with a base width of 250 Å.

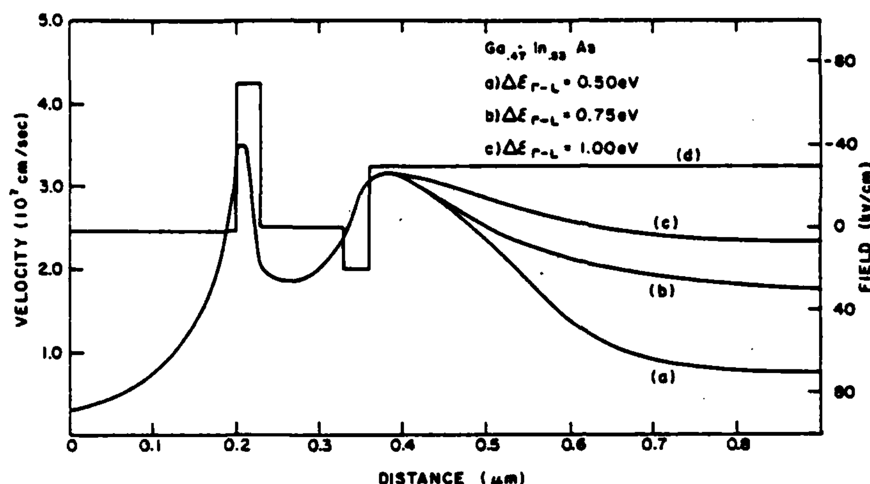

FIG. 3. Ensemble average velocity [curves (a), (b), and (c)] and electric field distribution [curve (d)] vs distance for a $Ga_{0.47}In_{0.53}As$ planar-doped barrier transistor. Results for three values of intervalley energy separation ($\Delta_{\Gamma L}$) are shown.

barrier transistors with base widths less than about 1000 Å.

Figure 3 shows the ensemble average velocity for a structure with material parameters the same as $Ga_{0.47}In_{0.53}As$[16] for three different values of intervalley energy separation $\Delta\epsilon_{\Gamma L}$. The device parameters are the same as those in Fig. 2 with base width = 1000 Å. Until the final field step in the collector region, the transport in this material is not drastically different from that of GaAs. In the collector, the velocity transition and final velocity value is greatly influenced by $\Delta\epsilon_{\Gamma L}$. This illustrates that transport in this region is influenced by velocity overshoot.[17] Also, increased speed and frequency performance can be expected in planar-doped barrier transistors fabricated from such central valley dominated materials as GaInAs.[18]

IV. DISCUSSION OF TRANSPORT MECHANISMS

In the region to the left of the emitter-base high field spike there is a large increase in the ensemble average velocity. This velocity increase has been shown to be due to the collecting nature of the emitter-base high field boundary.[13] A carrier which crosses into the region $x > 0.2$ μm has a low probability of being scattered back into the low field region $x < 0.2$ μm. The probability for such backscattering decreases as the barrier height of the emitter-base high field spike region increases. This is illustrated in Fig. 4, which shows the ensemble average velocity for high field spikes with barrier heights of 0.06, 0.12, and 0.3 eV. The Monte Carlo data points for an ideal collecting barrier are also shown. These data points were generated in a separate Monte Carlo simulation for which all particles reaching $x = 0.2$ μm were removed. The 0.06 eV barrier is not quite an ideal collecting boundary, while the 0.12 and 0.3 eV barriers are essentially ideal. Our simulations have shown that a barrier height of 0.1 eV or greater acts as an ideal collecting boundary in planar-doped barrier structures. For barrier heights greater than 0.1 eV, there are very few particles at the boundary which have negative velocities.

The data shown in Fig. 4 also relates to transport in the base region of the planar-doped barrier transistor. The ensemble velocities reach a maximum of between 2.7×10^7 and 3.8×10^7 cm/s within the high field region, depending on the field value. Also, the ensemble velocities decrease rapidly before the high-to-low field transition occurs. Outside the high field region, the ensemble velocities for step field values of 20 and 40 kV/cm stay above the steady state velocity (V_{ss}) for the 1 kV/cm background field. This behavior is unexpected based on the expected quick acceleration propsoed for the planar-doped barrier transistor.[11] In this picture, the emitter-base-high field region is kept small enough (≃150–300 Å) so that collisions are unlikely. These electrons are then ballistically launched into the base region where they are expected to travel up to 0.3 μm before losing a large fraction of momentum.[11,12] While Fig. 4 shows that the velocity in the base is higher than V_{ss} for fields of 20 and 40 kV/cm, and that it can stay high for a substantial distance (i.e., a few hundred angstroms), the ensemble velocities are lower

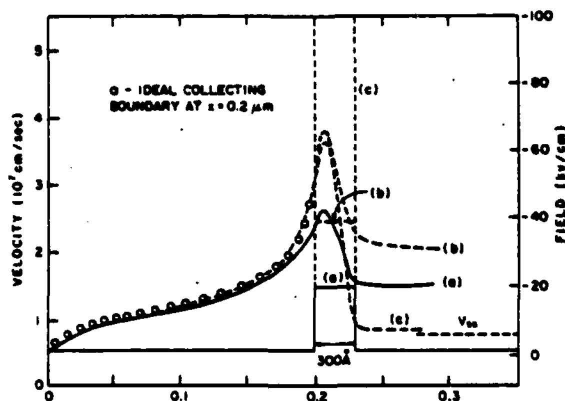

FIG. 4. Ensemble average velocity vs distance for high field spikes. The electric field intensities for the spikes are 20 kV/cm [curve (a)], 40 kV/cm [curve (b)], and 100 kV/cm [curve (c)] over a distance of 300 Å. The values of V_{ss} shown indicates the steady state average velocity in the 1 kV/cm background field.

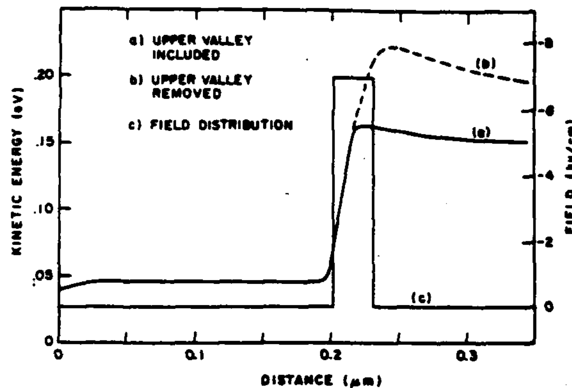

FIG. 5. Ensemble average kinetic energy vs distance for a field spike of 70 kV/cm over 300 Å with and without intervalley scattering.

by a factor of 2 than would be anticipated based on the quick acceleration argument.

As proposed in the quick acceleration model, our simulations show that the ensemble can be accelerated ballistically through the emitter-base high field region. This is illustrated in Fig. 5, which shows ensemble average kinetic energy versus distance through a 70 kV/cm, 300 Å high field spike. When the $L(111)$ conduction band minimum is removed from the simulation, the ensemble average kinetic energy at the edge of the high field spike is 0.21 eV. This is the energy gained ballistically from an electron traveling 300 Å in a 70 kV/cm field. The ensemble actually travels ballistically for a distance of about 350 Å since the energy does not change abruptly when the field changes. However, when the upper (satellite) valley is included, the ensemble is not accelerated to the ballistic energy, but reaches a maximum of about 0.16 eV. In both cases the kinetic energy decay occurs over a relatively long distance, indicating a large energy relaxation time.

In Figs. 4 and 5, the energy which can be ballistically imparted to an electron from the field spikes are less than 0.33 eV, the energy separation between the central (Γ) and satellite (L) valleys ($\Delta\epsilon_{\Gamma L}$) in GaAs.[4] Questions then arise as to why intervalley scattering affects the velocity and energy shown in Figs. 4 and 5, respectively. The energy shown in Fig. 5 is total ensemble average energy for all particles in both Γ and L valleys. We have previously shown that the distribution of carriers in the Γ valley extends to much higher energies than the ensemble average kinetic energy for fields well above the threshold field.[16] This energy redistribution occurs very rapidly ($t \simeq 0.5$ ps) when electrons are injected into a high field region. Thus, for the cases illustrated in Figs. 4 and 5, the energy distribution in the Γ valley extends to energies well above $\Delta_{\Gamma L}$, and intervalley scattering is important in spite of the fact that the ensemble average kinetic energy is well below $\Delta_{\Gamma L}$.

For the fields and dimensions considered, the dominant scattering mechanisms in the GaAs planar-doped barrier transistor are polar optical scattering, ionized impurity scattering, and intervalley scattering.[19] Intervalley scattering is highly isotropic, while polar optical scattering and ionized impurity scattering are primarily small angle scattering events.[19,20] If isotropic scattering becomes a significant fraction of the scattering events in the base there will be a large number of electrons which are backscattered toward and into the emitter-base high field spike region. Since most of these carriers do not cross the barrier back into the emitter region, their negative velocities lower the ensemble average velocity in both the base region and in the emitter-base high field spike region. This is apparently the mechanism for velocity reduction in these regions (Fig. 4). The increase in intervalley scattering is enhanced because the energy relaxation time is large. Since the ensemble average energy in the base region remains high over a substantial distance, the scattering rate for intervalley scattering remains high until the energy decays sufficiently. The scattering rate decreases as the energy decreases, which further prolongs the energy relaxation.[20]

Figure 6 further illustrates these points. The ensemble average velocity is shown for a 20 kV/cm step field occurring

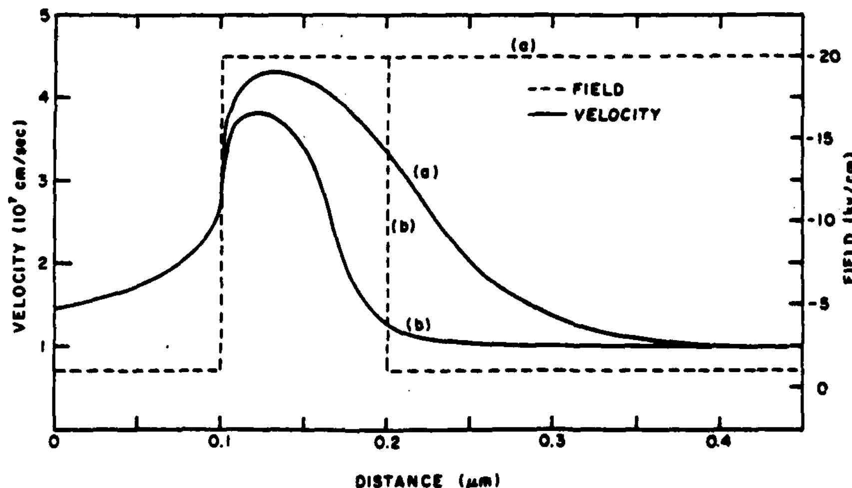

FIG. 6. Ensemble average velocity vs distance for a 20 kV/cm step field [curve (a)] and a 20 kV/cm, 1000 Å field spike [curve (b)].

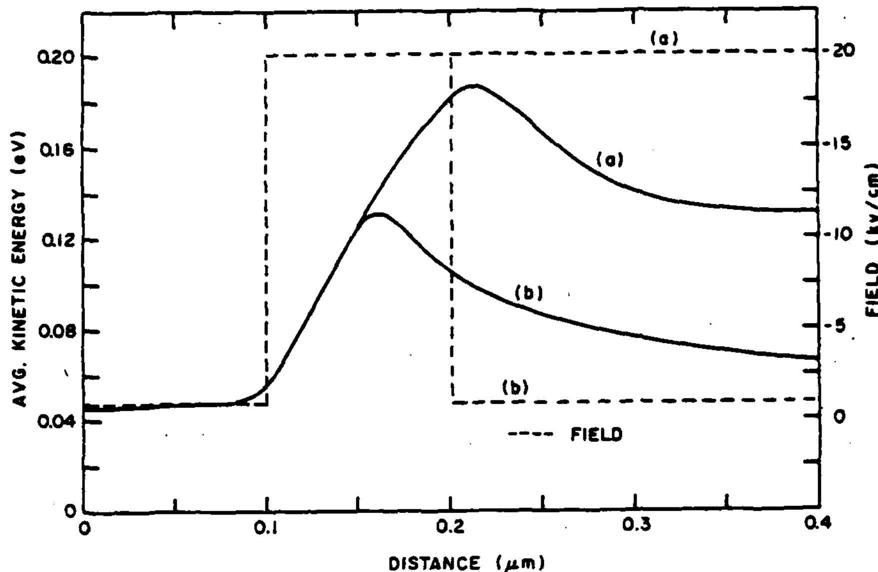

FIG. 7. Ensemble average kinetic energy vs distance for a 20 kV/cm step field [curve (a)] and a 20 kV/cm, 1000 Å field spike [curve (b)].

at $x = 0.1$ μm and for a field spike of 20 kV/cm at $x = 0.1$ μm with a width of 0.1 μm. For $x > 0.1$ μm, the ensemble average velocity for the step field is larger than the ensemble velocity for the field spike. The potential barrier for the field step is 0.2 eV across the 0.1 μm distance, which is more than adequate to prevent backscattered particles from crossing the barrier into the region $x < 0.1$ μm. However, the potential barrier decreases linearly for the field step, and is 0.4 eV at $= 0.3$ μm and 0.6 eV for $x = 0.4$ μm. Thus, carriers in the region $x > 0.2$ μm are more readily backscattered into the region $0.1 < x < 0.2$ μm for the field spike than for the step field. Also, Fig. 7 shows the ensemble average energy for these two field profiles. The ensemble average energy is greater for the step field in the region $x > 0.2$ μm because the carriers gain additional energy from the higher field. The decay to steady state is faster because the amount of energy loss required for the step field distribution to reach steady state is less than for the field spike.

Thus, isotropic scattering plays a major role in real space transfer devices by reducing the ensemble average velocities in the base region and in the emitter-base high field spike region. The effects of isotropic scattering on transport in real space transfer devices and other quick acceleration schemes cannot be eliminated. However, to a first approximation, its effects on velocity reduction in the base region can be minimized by limiting the energy which can be imparted ballistically in the emitter-base high field spike region to less than about one-half the intervalley energy separation. Thus, $qEd < 0.5\Delta_{\Gamma L}$, where E is the emitter-base accelerating field and d is the width of the accelerating field region. This was the case for each value of $\Delta_{\Gamma L}$ in Fig. 3, and is the reason there that the emitter- and base-region transport are not affected by $\Delta_{\Gamma L}$. It is important to realize that transport of a distribution of carriers in a device (ensemble transport) is influenced by the field distribution both behind and ahead of the mean diplacement of the distribution. This is a unique ensemble effect which is not predicted using single particle ballistic or scattering models.

V. CONCLUSIONS

The GaAs planar-doped barrier transistor is a three terminal device capable of operating at frequencies above 30 GHz. Ballistic transport, velocity overshoot, and ensemble effects all play a role in the physics of this device. Based on the results presented here, factors which should be incorporated in device design are (a) the emitter-base barrier height should be greater than about 0.1 eV, (b) the base width should be less than about 1000 Å, (c) the product of field times distance in the emitter-base field spike should be less than one-half the potential due to intervalley energy separation, and (d) materials with high intervalley energy separations should be used to increase the velocity in the collector-base junction.

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A Broad-Band Amplifier Output Network Design

ALFY N. RIDDLE AND R. J. TREW, MEMBER, IEEE

Abstract—An analytic design method for a lossy gain-compensating network is presented and the advantages of lossy networks are discussed. Examples of two-stage amplifiers using FET's and bipolar transistors are presented to show the feasibility of this particular network in low power amplifier designs. These amplifiers obtain gains of 15.4±0.5 dB with a 2.5-dB maximum noise figure in the 4.0–6.0-GHz frequency range and 16.5±1.2 dB with a maximum input VSWR of 1.78:1 over the 1.0–2.0-GHz frequency range, respectively.

I. Introduction

Lossy gain-compensating output networks can provide lower input reflection coefficients, a lower amplifier noise figure, and a more predictable amplifier design [1]. The resistive nature of this type of network may also improve amplifier stability and distortion by reducing standing waves within the amplifier. Although lossy broad-band gain-compensating networks are often used [1]–[4], explicit, analytic design techniques for these networks have not been reported.

This paper presents an output circuit design based upon a π matching network combined with a bandpass/bandstop diplexer. As a result, this network contains both the drain supply inductance and the dc blocking capacitor, which are needed in any output network, as integral elements. Explicit formulas for the element values of this network are derived and presented shortly. This method is different from previous methods [1] because this technique allows the device load to approach 50 Ω as frequency is decreased. However, this network is similar to that used in [2] and [3] in that the supply voltage is inserted through a quarter-wavelength shunt stub and a series resistor. This method results in greater stability and tunability for the amplifier.

A bandpass/bandstop diplexer is more useful than a simple low-pass/high-pass diplexer because it provides an exact match at one frequency, and an arbitrary amount of attenuation (limited only by network element Q's) at any frequency. Diplexing networks may be used in either input or output networks depending

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The authors are with the Department of Electrical Engineering, North Carolina State University, Raleigh, NC 27650.

on noise figure, power output, stability, and other amplifier constraints. This paper considers the characteristics of a resonant diplexer in the output network.

II. Network Design

The output network is designed in two parts. First, a π network matches the transistor output impedance to 50 Ω at the highest frequency of interest f_H. The insertion loss of this network IL_p, at the lowest frequency of interest f_L, is calculated and subtracted from the total loss desired for gain compensation IL_T to give the loss required of the diplexer IL_d. This may be expressed as

$$IL_T(f_L) = IL_d(f_L) + IL_p(f_L) = MAG(f_L) - MAG(f_H) \quad (1)$$

where $IL_T(f_H) = 0 = IL_d(f_H) = IL_p(f_H)$, and $MAG(f)$ is the maximum available gain of the device and input network at the specified frequency. In this paper, insertion loss is in decibels, and is with respect to the maximum power available from a 50-Ω source. This simple two-point method of compensation works well for the gradual gain versus frequency slopes of single-stage amplifiers. The diplexer center frequency is f_H, and the diplexer bandwidth is determined by the required loss IL_d, at f_L.

A standard parallel RC network equivalent circuit is derived for the transistor output impedance. This circuit may be derived in a conventional manner from $S_{22}(f_H)$ in the unilateral case, from the conjugate of the output match reflection coefficient for minimum noise at f_H, or from the conjugate of the complete match reflection coefficient at f_H. In the π matching network shown in Fig. 1, R_0 and C_1 are derived from the transistor output admittance. It is worth noting that L_2 consists, at least in part, of the bonding wire to the transistor chip from the microstrip circuit. The equations for this matching network are derived by separating the network at node A in Fig. 1 and writing expressions for the impedances looking towards R_0 and R_L. Real and imaginary (one direction being conjugated) parts are equated to obtain a match. Thus, we have

$$Q_0 = \omega_H R_0 C_1 \quad (2)$$

$$Q_L = \omega_H R_L C_3 = \left[\frac{R_L}{R_0}(Q_0^2+1)-1\right]^{1/2} \quad (3)$$

$$C_3 = \frac{Q_L}{\omega_H R_L} \quad (3a)$$

$$L_2 = \left[\frac{R_0^2 C_1}{1+Q_0^2} + \frac{R_L^2 C_3}{1+Q_L^2}\right] \quad (4)$$

where $\omega_H = 2\pi f_H$.

The insertion loss for this network may be derived by describing the network as an $ABCD$ matrix seen from R_L. The matrix elements may be converted to S-parameters via the relation [5]

$$S_{21}(j\omega) = \frac{2\sqrt{R_0 R_L}}{A(j\omega)R_0 + D(j\omega)R_L + B(j\omega) + C(j\omega)R_0 R_L} \quad (5)$$

and expressed as an insertion loss in decibels by

$$IL_p(j\omega) = 10\log|S_{21}(j\omega)|^2$$

$$= 10\log\left(\frac{4R_0R_L}{\left[R_0+R_L-\left(\frac{\omega}{\omega_H}\right)^2 X_2(Q_0+Q_L)\right]^2 + \left[\frac{\omega}{\omega_H}\left\{X_2+R_LQ_0+R_0Q_L-\left(\frac{\omega}{\omega_H}\right)^2 X_2Q_0Q_L\right\}\right]^2}\right) \quad (6)$$

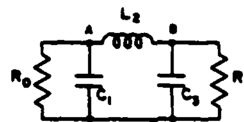


Fig. 1. π matching network. R_0 and C_1 are the transistor output equivalent circuit.

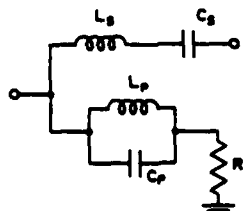


Fig. 2. Resonant diplexer network for lossy gain compensation.

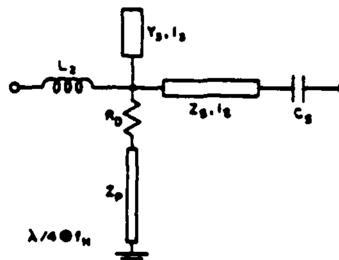


Fig. 3. Distributed form of output network for lossy gain compensation.

where $X_2 = \omega_H L_2$. Since the diplexer presents a constant 50 Ω to this network, this insertion loss is affected mainly by changes in the elements of the transistor output equivalent circuit. The FET design shown later suffered very little from an 85-percent change in its output conductance across the operating frequency range. In these situations an average output conductance weighted toward the top of the frequency range may be useful. The mismatch of the π network at f_L has not been found to disturb the diplexer's characteristics. The desired diplexer loss IL_d, at f_L determines the diplexer bandwidth by the relation

$$BW = \frac{f_H^2 - f_L^2}{f_H f_L (10^{IL_d/10}-1)^{1/2}} \quad (7)$$

which comes from the expression

$$IL_d = 10\log\frac{1}{1+\left[\frac{1}{BW}\left(\frac{f_H^2-f_L^2}{f_Hf_L}\right)\right]^2} \quad (7a)$$

where IL_d is a positive number and the bandwidth BW is normalized. This equation is a rearranged form of the insertion loss for a simple resonant network. The equations presented below for the diplexer in Fig. 2 may be found in any network synthesis text [6]

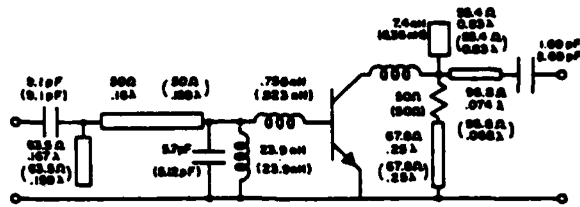


Fig. 4. MRF901 amplifier design for 1.0- to 2.0-GHz frequency range. All line lengths are a fraction of a wavelength to 2.0 GHz. Optimized values are in parenthesis.

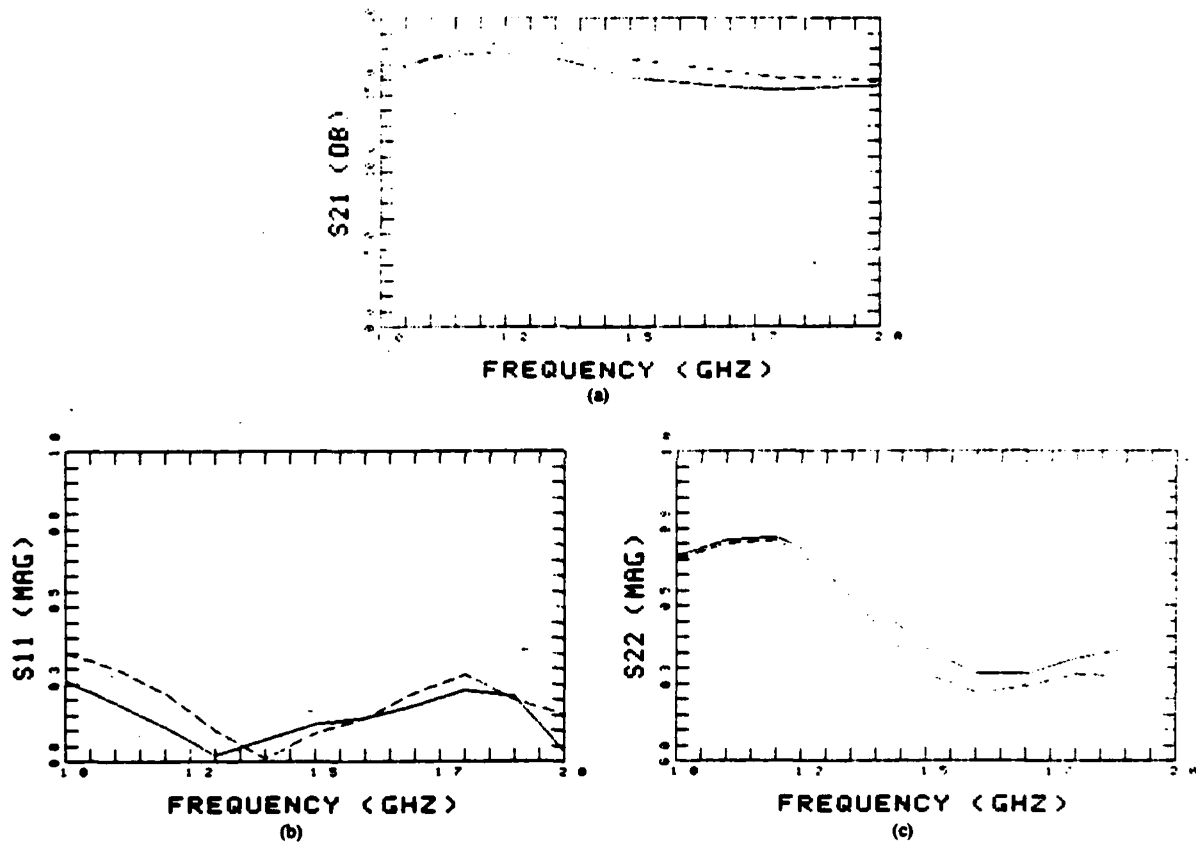


Fig. 5. MRF901 1.0–2.0-GHz amplifier characteristics. (a) S_{21}(db). (b) $|S_{11}|$. (c) $|S_{22}|$.

$$C_S = \frac{BW}{50\omega_H} \tag{8a}$$

$$L_S = \frac{1}{\omega_H^2 C_s} = (50)^2 C_p \tag{8b}$$

$$L_p = \frac{BW(50)}{\omega_H} = (50)^2 C_S \tag{8c}$$

$$C_p = \frac{1}{\omega_H^2 L_p}. \tag{8d}$$

In the final network, the diplexer replaces R_L of Fig. 1 and the output of the amplifier is taken from the diplexer's series LC circuit. Fig. 3 shows the entire output network in distributed form; with $Z_p = 4\omega_H L_p/\pi$, $Z_S = \omega_H L_S/\tan(2\pi l_S/\lambda)$, and $Y_3 = \omega_H C_3/\tan(2\pi l_3/\lambda)$, where l is the transmission-line length. These lumped to distributed network equivalences are derived by equating reactance slopes of the elements at the desired center frequency [7].

III. Examples

Amplifier designs using a Motorola MRF901 and a Hewlett-Packard HFET-1101 are shown in Figs. 4–7. These designs were analyzed and optimized with COMPACT. Figs. 4 and 6 show the

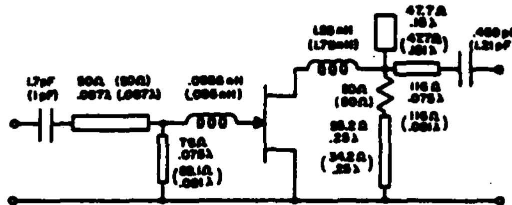
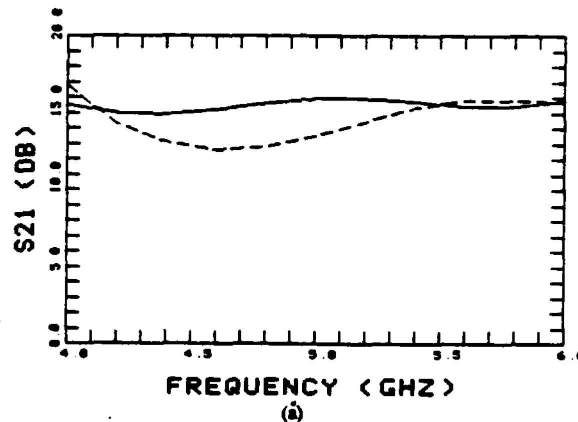
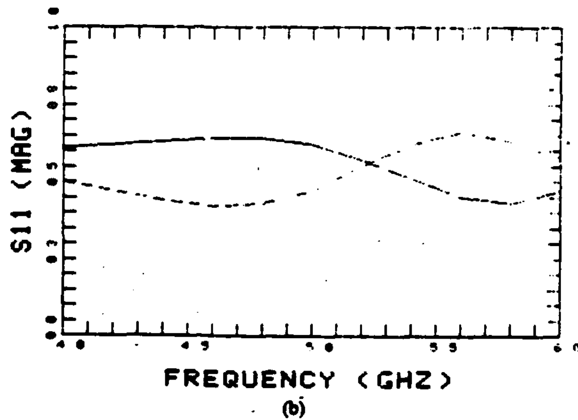


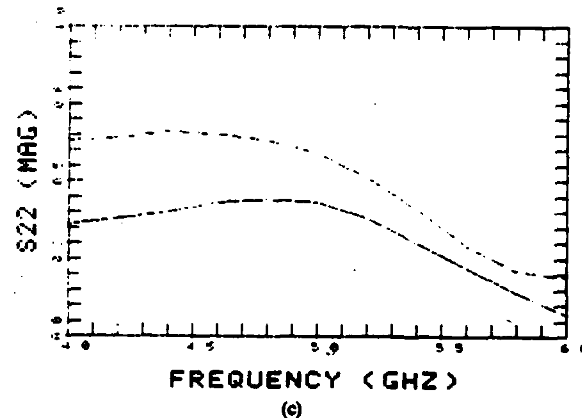
Fig. 6. HFET-1101 amplifier designed for minimum noise figure in the 4.0- to 6.0-GHz frequency range. All lines are given in a fraction of a wavelength at 6.0 GHz. Optimized values are in parenthesis.



(a)



(b)



(c)

Fig. 7. HFET-1101 4.0–6.0-GHz low-noise amplifier characteristics. (a) S_{21}(db). (b) $|S_{11}|$. (c) $|S_{22}|$.

actual designs with optimized element values in parenthesis. Figs. 5 and 7 show the characteristics of a two-stage cascade of each amplifier before and after optimization, with the solid lines representing optimization.

The MRF901 amplifier was designed for minimum input reflection coefficient and maximum flat gain over the 1.0 to 2.0-GHz frequency range. The equivalent circuit for this device was based on a complete conjugate match at 1.0 and 2.0 GHz. Because this transistor's input circuit appeared as a dominantly inductive series-resonant circuit, an iterative Smith Chart procedure was used to design the input network. The output network was designed according to the equations of the previous section. Since the *MAG* of the MRF901 was 8.0 dB at 2.0 GHz and 13.8 dB at 1.0 GHz, 5.8 dB of insertion loss was required of the output network at 1.0 GHz. This insertion loss was composed of 1.05 dB of π network loss and 4.75 dB of diplexer loss. The diplexer loss of 4.75 dB determined a bandwidth of 1.065. Figs. 4 and 5 indicate that this design was easily cascaded and required no optimization. Lossless gain-compensating output networks were tried with this combination of device and input network with less predictable results. Figs. 5(a), (b), and (c) show maximums of ± 1.4 dB of gain variation around 16.8-dB gain, 1.78:1 input VSWR, and 6.2:1 output VSWR.

The HFET-1101 amplifier was designed for minimum noise

figure in the 4.0 to 6.0-GHz frequency range with a maximum flat gain. The analytic approach used in [2] was the basis of the input network design. This input network was designed to match the conjugate of the optimum source impedance for low noise at 5.0 GHz. Interpolation was used to derive this impedance from the published data at 4.0 and 6.0 GHz. The network element values were derived from an $n=3$, 0.01-dB ripple, Chebyshev low-pass prototype [8]. The first impedance inverter (K_{34}) was omitted from the final design because its 50.75 Ω impedance contributed little to the overall match.

The transistor output equivalent circuit was derived from the conjugate of the reflection coefficient for a matched output with minimum noise. The unilateral gain approximation as described in [9] was used to find the maximum amplifier gain at 4.0 and 6.0 GHz. The source reflection coefficient derived from the conjugate of the transistor input equivalent circuit at 4.0 and 6.0 GHz was used in this unilateral gain approximation. This required 3.55 dB of loss at 4.0 GHz. A maximum gain of 8.45 dB at 6.0 GHz was expected for the amplifier. The diplexer network needed to provide 2.85 dB of the 3.55-dB loss, and so a normalized bandwidth of 0.864 was used. Although the cascade of two identical single-stage amplifiers provided acceptable results without adjustment of any of the circuit elements, optimization improved the gain flatness and output reflection coefficient. The noise figures of 2.1 dB and 4.0 GHz and 2.35 dB at 6.0 GHz were changed to 1.9 dB at 4.0 GHz and 2.48 dB at 6.0 GHz during optimization. The relatively high VSWR of this amplifier's input, as shown in Fig. 7(b), is due to providing an optimum source impedance for noise minimization.

The formulas presented in this paper are useful whenever the equivalent circuit of the device is a parallel RC network. Therefore, bipolar transistor amplifiers operating well below the device's f_T may contain the circuit just presented as an input matching network.

IV. Conclusion

A simple output network was shown to simultaneously provide gain-compensation and a predictable amplifier design. The feasibility of this design method was demonstrated by cascading two identical single-stage amplifiers and calculating the total amplifier S-parameters before and after optimization. Although the input and output networks were designed by treating the amplifier as if these networks did not interact, the actual results agreed well with simple theory. Explicit formulas for the design of lumped and distributed output networks were presented.

Acknowledgment

The excellent work of typist Ms. N. Tyson is greatly appreciated by the authors.

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PARAMETER INSENSITIVE MATCHING CIRCUITS FOR LOW COST INTEGRATED CIRCUITS*

A. N. Riddle and R. J. Trew
Electrical Engineering Department
North Carolina State University
Raleigh, North Carolina 27650

(919) 737-2336

ABSTRACT

A new theory for increasing the tolerance of matching networks to load variations is presented. This theory is based on matching the angles of the changes in $S_{11}(f)$ due to frequency and load variations, and its use can double allowed device tolerances in many cases. As a byproduct, this theory also shows why Chebyshev matching filters have poor tolerances. Examples are given showing as much as an order of magnitude improvement in circuit tolerances.

INTRODUCTION

The manufacture of microwave amplifiers, mixers and oscillators must include component and device tolerances in the design procedure if lower cost and more reliable circuits are to be produced. A new theory for maximizing the tolerance of matching networks to load variations is presented here. The tolerance of $S_{11}(f)$ to variations in the load, or any other component, is maximized when the variations cause a change in $S_{11}(f)$ that is perpendicular to the direction of $S_{11}(f)$. Knowledge of the angles of the differential changes in $S_{11}(f)$ with frequency and load variations allow the design of matching networks with a maximum tolerance over a band of frequencies.

The concern here is to maximize the tolerance of a circuit to variations in the active device used. For the lossless networks discussed here, it has been found that the magnitude and frequency variation of the input reflection coefficient determines the sensitivity to load variations. Simple formulae are presented for both differential and large change sensitivities in terms of S-parameters. These formulae, along with the nature of matching networks allows us to establish worst case tolerances, and show how matching networks capable of doubling the typical worst case load tolerance may be designed. Also, the rapid changes with frequency due to the ripples of a Chebyshev network will be shown to decrease its tolerance relative to what is possible with matching networks using a flat mismatch equal to the peak of the Chebyshev. Simulations of narrowband and broadband feedback FET amplifiers illustrate these conclusions.

THEORY

By using an ABCD matrix representation of a matching network, we may see the transformation from the load immittance to the input reflection coefficient as two bilinear transformations. This means that since changes in the real and imaginary parts of the load are orthogonal, resulting changes in the input reflection coefficient will be orthogonal. Since we usually want to increase the tolerance of the circuit to reactive variations in the load, we may exploit this orthogonality to increase our tolerance. The following equation will prove useful, and is derived assuming $Z_L(f) = R + j\,X(f)$:

$$\frac{\partial S_{11}(f)}{\partial X(f)} = j\,\frac{S_{21}(f)\,S_{12}(f)}{2\,Z_L(f)}. \qquad (1)$$

Figure 1 shows the center of the reflection coefficient plane with a circle enscribing the maximum tolerable reflection, Γ_{max}. A point, $S_{11}(f_o)$ is located inside this circle and represents a point on the curve of input reflection coefficient versus frequency for the amplifier. Increases and decreases in the device reactance, typically the input capacitance, will cause the point $S_{11}(f_o)$ to move. This differential movement is given exactly by equation (1) for any network describable via S-parameters.

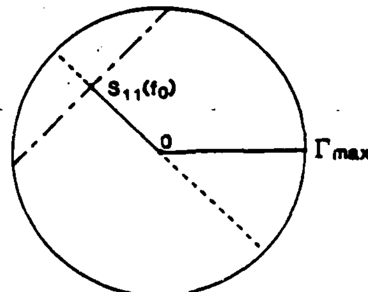

Figure 1. Reflection plane. The circle of maximum tolerable reflection, Γ_{max}, and the circuit reflection coefficient at f_o, $S_{11}(f_o)$ are shown. The dashed and alternating lines show the minimum and maximum absolute changes in $S_{11}(f_o)$, respectively.

The alternating line of Figure 1 shows the maximum symmetric tolerance about the point $S_{11}(f_o)$. The dashed line of Figure 1 shows an asymmetric tolerance which for practical purposes should be limited to its maximum symmetric variation. This shows how variations in the device capacity will have a minimum tolerance if they cause radial excursions in $S_{11}(f_o)$ and a maximum tolerance if they cause excursions of $S_{11}(f_o)$ along the alternating line of Figure 1. As a reminder, the tolerance in the device capacity would be that percentage change which caused $S_{11}(f_o)$ to lie on the Γ_{max} circle.

The next step toward a more tolerant network lies in the expression of the change in $S_{11}(f)$ with frequency as given by the equation

$$\frac{\partial S_{11}(f)}{\partial f} = j\,\frac{S_{21}(f)S_{12}(f)}{2Z_L(f)}\cdot\frac{\partial X}{\partial f} + \frac{S_{21}{}^2(f)}{2Z_L(f)}\cdot\left[\left(C\frac{\partial A}{\partial f} - A\frac{\partial C}{\partial f}\right)Z_L{}^2(f) + \left(C\frac{\partial B}{\partial f} + D\frac{\partial A}{\partial f} - A\frac{\partial D}{\partial f} - B\frac{\partial C}{\partial f}\right)Z_L(f) + \frac{D\partial B}{\partial f} - \frac{B\partial D}{\partial f}\right]. \qquad (2)$$

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where A, B, C, and D are the parameters of the ABCD matrix for the input matching network. Equation (2) shows that for all low Q or resistive matching networks the absolute direction of $\partial S_{11}(f)/\partial f$ is exactly the same as that of $\partial S_{11}(f)/\partial X$, depending only on the sign of $\partial X/\partial f$. For these networks reactive variations in the load have their maximum tolerance when the $S_{11}(f)$ is a constant over the passband, i.e. the matching filter has a flat mismatch response. While practical networks are not resistive and rarely low Q, equation (2) leads to the conclusion that matching networks should provide a flat mismatch at least over the center of the band and snould not have large ripples such as a Chebyshev filter. These conclusions will be elaborated on via examples on Chebyshev and Butterworth matching filters, as well as a broadband FET feedback amplifier.

Another result of this study is given by equation (3) which gives the maximum percentage tolerance of a series or parallel load capacitance assuming that $S_{11}(f_o) = 0$, the matching network is lossless, the network is also reciprocal, and the percentage change in the capacitance is small:

$$\%\text{ tolerance} = \frac{200}{Q_f} \cdot \frac{\Gamma_{max}}{\sqrt{1-\Gamma_{max}^2}} \quad (3)$$

where Q_f is the Q of the load at f_o.

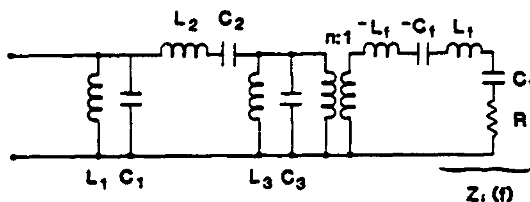

Figure 2. Idealized bandpass matching filter for testing tolerances to load, $Z_L(f)$ and circuit variations. See Table I and Figures 3 and 4.

RESULTS

The network of Figure 2 was used to examine the tolerance of ideal Chebyshev and Butterworth responses to variations in the load capacitance. The load is a narrowband model of the input impedance of a 250 μ wide FET used in the 3.7 to 4.2 GHz range. Note that ideal responses were obtained by neutralizing the load reactances with negative components and using an ideal transformer. Figures 3 and 4 are plots of third order Cnebyshev and Butterworth bandpass filters with a normal and 2% high FET capacitance. These plots are only from 3.75 to 4 GHz for clarity, and have the normal capacitance, .3 pF, as the circled points and the high value as triangular points. These filters were designed for peak reflections less than .26 from 3.7 to 4.2 GHz.

The problem with the Chebyshev filter is not only that the reactance variation causes a change in $S_{11}(f)$ that is not quite tangent to $S_{11}(f)$ at the ripple peaks, but that the change in $S_{11}(f)$ due to reactive load variations becomes tangent to the curve of $S_{11}(f)$ at higher frequencies. This means that the rapid magnitude change in $S_{11}(f)$ causes reactive variations in in the load to cause near radial variations in $S_{11}(f)$ and thus a lower tolerance. Chebyshev responses are only optimal when passband and stopband responses are considered. As can be seen from Figures 3 and 4, the mismatched Butterworth response has a greater tolerance in the midband even though its smallest reflection is equal to the peak reflection of the Chebyshev. The Butterworth filter's tolerance is reduced at the band edges because variations in the load reactance cause changes in $S_{11}(f)$ which begin to be normal to the variation in $S_{11}(f)$ with frequency. Since the Butterworth filter has near ideal tolerance properties in its midband, modifying its band edge response will lead toward optimally load tolerant filters.

The subject of load tolerant filters in lossless reciprocal structures demands selecting filter properties that yield the highest tolerance to variatons in reactive or resistive variations in the load. Reciprocal structures must rely on loss or angular relations for tolerant design, as seen via the $S_{21}(f)$ and $S_{12}(f)$ terms in equations (1) and (2). The $S_{12}(f)$ term in equation (1) shows how circulators and isolators allow tolerance to load variations in nonreciprocal networks.

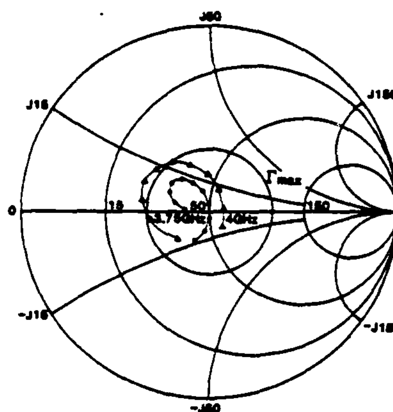

Figure 3. Plot of Chebyshev filter response (circles) and response with load capacitance, C_f, increased by 2% (triangles). Also shown is the maximum allowable reflection, Γ_{max} = .333. Only 3.75 to 4 GHz of the 3.7 to 4.2 GHz response is shown for clarity. Note response variation to load capacitance becomes tangent to the response curve as frequency is increased (dashed lines). See circuit in Figure 2.

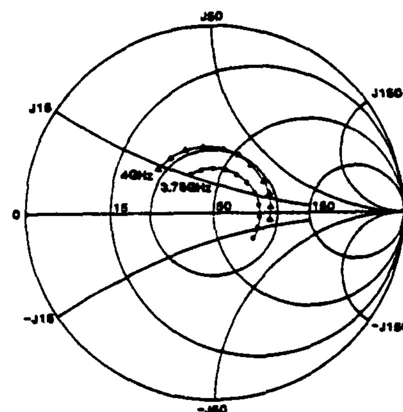

Figure 4. Plot of Butterworth filter response (circles) and response with load capacitance, C_f, increased by 2% (triangles). Also shown is the maximum allowable reflection, Γ_{max} = .333. Only 3.75 to 4 GHz of the 3.7 to 4.2 GHz response is shown for clarity. Note response variation to load capacitance becomes tangent to response curve in the midband (dashed lines). See circuit in Figure 2.

TABLE I

BANDPASS MATCHING FILTER TOLERANCES

Circuit Parameters			Allowed Element Tolerances (%) for Γ_{max} = .333 and BW = 3.7-4.2 GHz (see Figure 2)		
Filter	Q	ρ max	Device C_f	Circuit 1	Circuit 2
Chebyshev	6.25	.278	1.2%	>.5% L_2	>.5% C_2
Butterworth	4	.28 (.25 midband)	.8%	>1% C_3	>1% L_3
Butterworth	4	.21 (.164 midband)	2.1%	>3% C_1	>4% L_2
Butterworth	.25	.278	2.2%	>6% n	>8% L_f
Ideal (eqtn 3)	0	0.0	3.9%		

TABLE II

MATCHING FILTER TOLERANCES

Broadband FET Amplifier (1-9 GHz)

Filter	Matching Filter C_1(pF)	Matching Filter L_2(nH)	Allowed Element Tolerances (%) for Γ_{max} = .333 and S_{21}>1.75: Device C_f	Circuit 1	Circuit 2
Tuned	.37	.92	>.5%	>.5% L_2	>1% g_m
Flattest	.2	.7	>6%	>11% g_m	>13% R_{FB}

A second point of clarification concerns the straight lines drawn in Figure 1. Of course, the bilinear property of networks causes all variations to have a finite curvature. This is most familiar to those using the MAP function of COMPACT. The result of this is to cause the calculations based on the straight lines of Figure 1 to be approximate.

Various bandpass networks represented by Figure 2 were tested for their tolerance characteristics over the 3.7 to 4.2 GHz band with Γ_{max} = .333. Table I provides information not only about load variations, but also about tolerances to filter components and the results of equation (3). The tolerance information is given for a maximum $S_{11}(f)$ = .333 with only one component being varied. The additional tolerances in Table I are for the first and second most sensitive network elements, as labeled, and their actual tolerance is less than the next higher integer.

Table II gives the tolerance results for a broadband FET feedback amplifier. This amplifier used a 750 μ wide FET of C_f = .6pF and g_m = .065 mhos with an LC matching filter (C_1, L_2) and a feedback resistor (R_{FB}) of 180 ohms. The FET model included source inductance and other pertinent components. Two different different matching filters were used with this amplifier, and have responses shown in Figure 5. The first design was "tuned" to provide zero reflection near 7 GHz, and results in a familiar humped response. The second response was designed to give a finite but flatter VSWR across the entire band. This latter design is less straightforward, but results in a much greater tolerance to both the FET and the circuit elements.

Acknowledgement

The excellent work of Ms. Kathy Julian, the typist, is greatly appreciated by the authors.

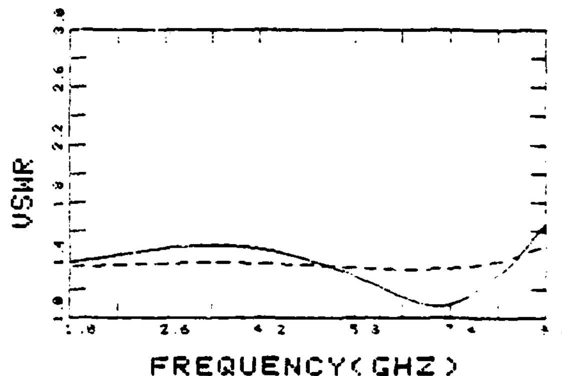

Figure 5. Input VSWR of 1-9 GHz FET feedback amplifier. Solid line is response with a tuned matching filter, ρ_{max} = .248. Dashed line is with a flat matching filter, ρ_{max} = .2.

CONCLUSION

In addition to the presentation of several equations useful for designing more tolerant circuits, it has been shown that the peaks and rapid magnitude changes of a Chebyshev filter create a low tolerance response. The use of matching filters which have a flat mismatch across most of the band was shown to provide a large improvement in device and circuit tolerances in all but the large reflection with high Q cases. High tolerance reciprocal networks are achieved by designing the circuit response so element variations cause response variations which are perpendicular to the response vector. The response should also be as flat as possible. The synthesis of maximally tolerant filters will aid the production of microwave circuits by simplifying the tuning procedure.

PROFILE STUDIES OF ION-IMPLANTED MESFETs*

J. M. Golio and R. J. Trew

Electrical Engineering Dept.
North Carolina State University
Raleigh, North Carolina 27650

ABSTRACT

A study of ion-implanted MESFET performance as a function of the implantation energy and fluency and including the effects of deep-level trap concentrations in the substrate has been conducted. Carrier concentrations as a function of depth are determined through the use of LSS theory and a profiling model. An analytic device model, which computes both DC and RF characteristics, is then employed to predict MESFET performances. The study includes the effects of depth dependent transport properties and has indicated a number of design rules for the fabrication of optimized ion-implanted devices.

INTRODUCTION

The performance of FETs fabricated by ion-implantation depends greatly on carrier concentrations and velocity-field characteristics as a function of depth into the active device layers. The presence of deep-level traps in the semiconductor contributes to the complexity of problems associated with the characterization of ion-implanted devices.

This work is targeted mainly at determining design rules for high-frequency ion-implanted MESFETs. The study utilizes theoretical models of both material properties and device characteristics. This information is combined with experimental material characterization to provide improved quantitative accuracy of the model.

Initially, the determination of typical ranges for concentrations of deep-level traps, $N_T(x)$ (normally due to chromium in the GaAs substrate) was made from a novel measurement technique using both differential capacitance and conductance DLTS data. Shallow-level donor concentrations, $N_D(x)$, were then determined from LSS theory as a function of implantation paramerers. These concentrations as a function of depth were then used in a profiling model to determine the free-carrier profile, $n(x)$, for the material. Carrier transport properties were also determined from the trap and donor profiles. This was done through the use of Monte Carlo particle simulations and a model to account for the effects of compensation in the semiconductor.

An analytic model which utilizes all of this information is then used to assess performance potential. The distinction between free-carrier and donor profiles, the effect of deep-level traps, and the depth dependance of mobility and velocity are shown to be important considerations which have been ignored in previous models. The DC characteristics and small-signal S-parameters along with figures of merit are computed by the model.

MATERIAL CHARACTERIZATION

Figure 1 shows free-carrier, background donor, and deep-level trap profiles typical of ion-implanted semiconductor material. Deep-level trap centers and free-carrier diffusion from highly doped to lowly doped regions will cause the free-carrier profile to differ from that of the ionized

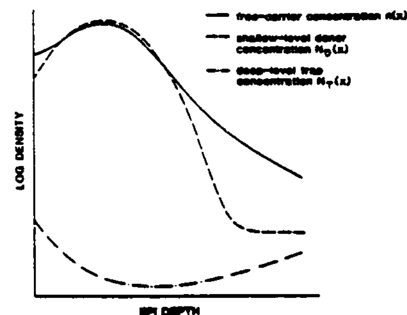

Figure 1 Typical concentraion profiles for ion-implanted material.

donors. Our studies show that as much as an order of magnitude difference can exist between these two profiles for ion-implanted materials typically used in the fabrication of GaAs MESFETs. The deep-level sites will also have a degrading effect on carrier transport properties.

Determination of the various profiles present in a sample is a difficult problem. Traditional C-V analysis measures the free-carrier concentration if traps are not present [1]. When traps are present, however, knowledge of the trap concentration profile is neccessary to extract the free-carrier information [2]. Likewise, DLTS data can give trap concentration information if the free-carrier profile is known. For this work,

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these two methods were combined to determine the free-carrier, shallow-level donor and deep-level trap concentrations for a typical ion-implanted device. The details of this technique are discussed elsewhere [3]. Needed for the technique is the low-field mobility of the material as a function of donor density and background compensation. This is obtained using the theoretical results of Walukiewicz et al. [4] in conjunction with Monte Carlo velocity-field predictions. Our own Monte Carlo results [5] were used to determine the mobility as a function of background donor density with no traps present, and the Walukiewicz values were then normalized to the Monte Carlo numbers. The normalized data was finally curve fit to obtain an empirical expression for mobility as a function of background donor density and compensation ratio. The resulting expression is

$$\mu_0 = \frac{\mu_{max}}{1 + \left(\frac{\log N_D}{N_0}\right)^c} \cdot (1-\theta)^b \qquad (1)$$

where

$\mu_{max} = 8380$ (cm2/v*sec),
$N_0 = 23.2553$,
$c = 23.0$,
$\theta = N_T/N_D$,

$b = A(\log N_D)^2 - B(\log N_D) + C$ for $N_D > 10^{21}$ (m^{-3}),
$b = 0.114992$ for $N_D < 10^{21}$ (m^{-3}),

with

$A = 0.025$,
$B = 0.817278$,
$C = 6.252838$

and where N_D is given in (m-3). Expression (1) is plotted against the normalized Walukiewicz values

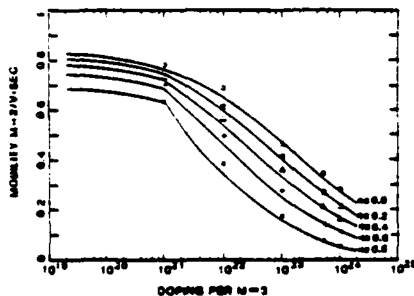

Figure 2 Low-field mobility as a function of doping and deep-level compensation. The solid lines are computed from equation (1) for θ=0.0, 0.2, 0.4, 0.6, 0.8. The data points are from the normalized theoretical computations [4].

in Figure 2. As can be seen from the plot, the agreement is quite good.

A one micron gate length MESFET along with a differential capacitance pattern were fabricated on Silicon implanted Cr-doped GaAs substrate. Conductance DLTS and C-V measurements were performed on these devices and a dominant deep-level trap state was identified 0.736 eV below the conduction band. The measurements were used as input data to a computer simulation which computes the desired profiles as mentioned above.

The final resulting free-carrier, shallow-level donor, and deep-level trap concentrations as a function of depth into the material are shown in

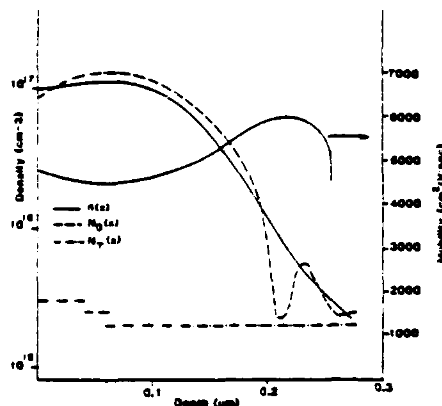

Figure 3 Resulting concentration profiles and low-field mobility profile for one device.

Figure 3. Notice that deep into the channel there is some scatter of the shallow-level donor data. This begins to occur when the trap concentration and the shallow-level donor concentration are of the same order of magnitude. The uncertainties in the exact shallow-level concentration at this depth into the channel are not critical to the profile predictions. This is true since the magnitude of all the profiles of interest are small at this depth when compared to their magnitudes near the implantation peak.

The low-field mobility profile obtained from this analysis is also shown in Figure 3. The curve can be compared to the results of Das and Kim [6], and is in good qualitative agreement.

THE DEVICE MODEL

The device model used here is a one-dimensional model with a small-signal analysis. One-dimensional models offer a number of advantages for a study of this type over more elaborate two-dimensional models. For example, the form of the results obtained from one-dimensional analysis is more useful in terms of many device optimization and design problems. Also, information needed to examine circuit/device interface phenomena can easily be obtained from one-dimensional results. Of critical importance here, however, is the cost difference between one- and two-dimensional simulations. In these studies, over one-hundred different device geometries were examined at ten to twenty different bias levels. To obtain this

information from two-dimensional simulations would have been at least an order of magnitude more costly in terms of both time and money.

The model assumes that the electron transport properties of a material can be simulated by a two-piece velocity-field relationship. The two-piece approximation is defined from a theoretical velocity-field characteristic determined by Monte Carlo techniques. For electric fields less than an appropriate saturation field, E_m, the electron velocity is described by a linear expression,

$$v = \mu_0 E. \quad (2)$$

For electric fields above E_m the electrons move at a constant, maximum velocity, v_m. Using this information, a small-signal equivalent circuit as shown in Figure 4 can be determined and analyzed to obtain RF performance predictions, including power gains as a function of frequency.

Low-field mobility as a function of depth for the model is obtained directly from equation (1). Determining the appropriate maximum velocity for the material is more involved, however.

The importance of developing a systematic, well-justified technique for determining maximum velocity, v_m, was discussed in earlier work [7,8] and in this study, such a method has been developed. The method involves numerical determination of the carrier transit time under the gate using an exact velocity-field relationship. The assumed field distribution for this calculation is obtained from two-dimensional simulation results. It is then required that the transit time calculated assuming a two-piece approximated velocity-field relationship be equal to that of the exact analysis. This method yields a v_m for GaAs (doped to a level $N_D = 10^{17} cm^{-3}$) in excellent agreement with the value obtained by Pucel et al. [9]. The resulting data was curve fit and expressed as

$$v_m = v_0 - A \log [(1-y)^2 + By] \quad (3)$$

where

$y = (N_D(x)/N_0)^{2.5}$,
$N_0 = 1.5 \times 10^{22}$,
$A = 0.0262$,
$B = 0.4$,
$v_0 = 1.40$.

Equation (3) gives v_m in 10^5 m/sec when $N_D(x)$ is expressed in m^{-3}. The expression is also assumed to have the same dependence on compensation ratio, θ, as equation (1). Thus, the factor $(1 - \theta)^b$ is multiplied with equation (3) to obtain v_m in the presence of traps. The exponent, b, is defined in equation (1).

Equations (1) and (3) in conjunction with knowledge of the three profiles, $n(x)$, $N_D(x)$ and $N_T(x)$, allow for the derivation of a device model which includes the effects of varying transport properties as a function of epi-depth.

The current-voltage predictions of the model for a one micron ion-implanted device are compared

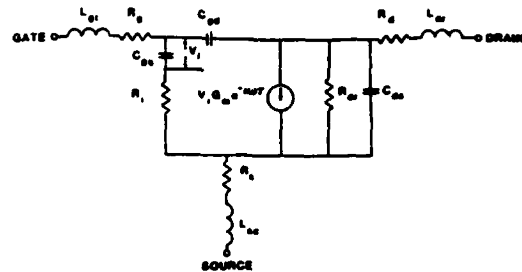

Figure 4 The equivalent circuit for an FET used in the analysis.

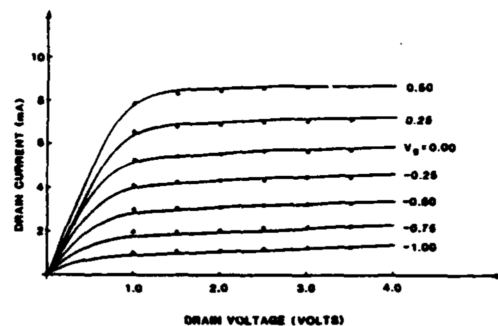

Figure 5 Comparison of model predicted and measured I-V characteristics for a one micron ion-implanted device.

in Figure 5 with the measured I-V curves. The agreement is excellent. It should be noted that without the inclusion of the effects of traps on carrier transport, this agreement could not be obtained. The traps have a tendency to "soften" the pinch-off characteristics of the device (ie. when traps are included in the simulation, the slope dI_D/dV_g is not as great near pinch-off). For all of the devices studied in this work, this "softening" effect was required to obtain best agreement with measured I-V characteristics.

RESULTS AND CONCLUSIONS

The results that follow were obtained following the modeling steps outlined in the Introduction. Three parameters were varied independently. They are 1) implantation energy, $\mathcal{E}$, 2) peak doping density, N_{max}, and 3) trap concentration, $N_T(x)$. The implant species was assumed to be Si in GaAs and the activation was assumed to be 100% for all devices. The trap concentration was assumed to be constant as a function of depth for these studies. Note that the peak doping density can be converted to a corresponding ion fluency through the simple relationship

$$\phi = \sqrt{2\pi}\, \sigma_p N_{max} \quad (6)$$

where σ_p is the standard deviation of the

projected range.

For the implant energy and peak doping studies, the trap level was left constant at N_T=2.0 x 10^{15} cm^{-3}. This number was chosen to be in general agreement with the results shown in Figure 3. The implant energy was varied from 50 to 150 keV while the peak doping took values between 8 x 10^{16} and 4 x 10^{17} cm^{-3}.

Figures 6a and 6b illustrate the effects these parameters have on the gain-bandwidth product, f_T,

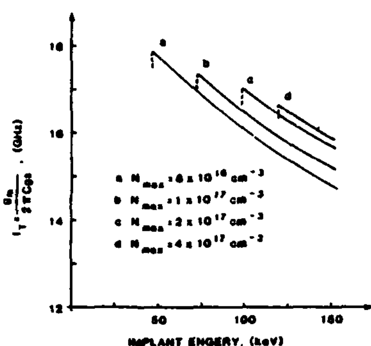

Figure 6a Predicted gain-bandwidth product, f_T, vs. implantation energy, ε. The peak doping, N_{max}, is used as an independent parameter.

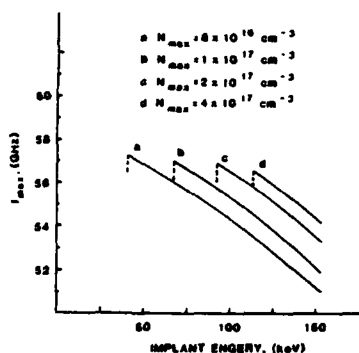

Figure 6b Predicted maximum frequency of oscillation, f_{max}, vs. implantation energy, ε. The peak doping, N_{max}, is used as an independent parameter.

and the maximum frequency of oscillation, f_{max}. The value for f_T is computed from first order considerations to be given by

$$f_T = g_m/2\pi C_{gs}. \quad (7)$$

The quantity f_{max} is obtained by noting the frequency at which Mason's unilateral gain (as predicted by the model) goes to unity. The results clearly indicate the superiority of low-energy implants for high-frequency operation.

All of the devices considered in compiling Figures 6a and 6b were compared at a bias of I_D=10 mA. The dashed line falling off rapidly at the low-energy end of the curves indicates that for energies lower than this, I_{DSS}<10 mA.

For the trap study, an implant energy of 70 keV and a peak doping density of 2 x 10^{17} cm^{-3} was assumed. The background trap concentration was varied from 0 to 10^{16} cm^{-3}.

Figure 7 illustrates the effects traps have on the zero gate bias current, I_{DSS}, and the pinch-off potential, W_{oo}. Figure 8 shows the pinch-off "softening" effect mentioned in the previous

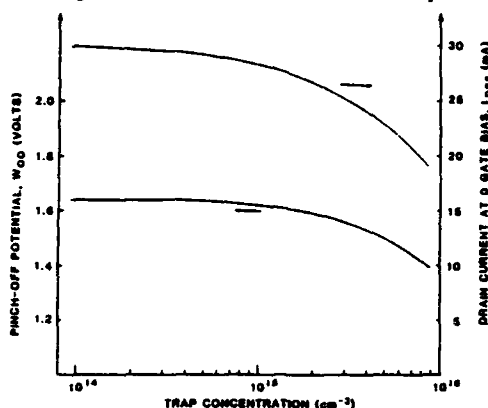

Figure 7 Predicted effects of varying trap concentrations on DC characteristics.

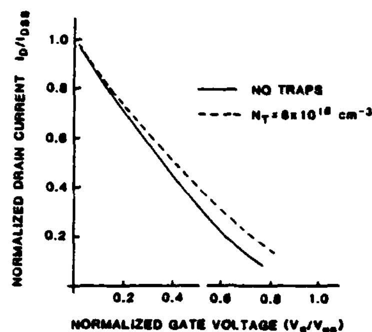

Figure 8 Normalized drain current predictions vs. normalized gate voltage with and without traps.

section for one particular device.

Deep-level traps also have some effect on the RF performance of the device as illustrated in Figures 9 and 10. Figure 9 shows clearly the decrease of f_T and f_{max} associated with increasing trap concentrations.

In Figure 10 note that for low bias currents f_T increases when few traps are present while it decreases for higher trap concentrations. This is easily explained in terms of the degrading effects traps have on mobility and velocity. As the gate bias restricts current flow, a larger fraction of the carriers are forced deeper into the channel.

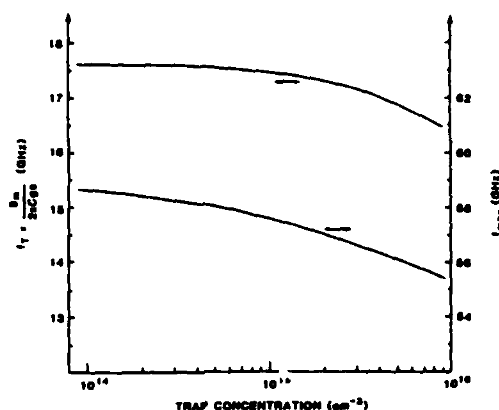

Figure 9 Predicted gain-bandwidth product, f_T, and maximum frequency of oscillation, f_{max}, vs. background trap concentration.

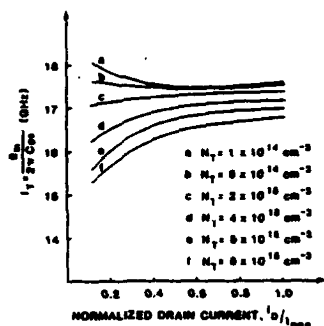

Figure 10 Predicted gain-bandwidth product, f_T, as a function of normalized drain current. The background trap concentration is used as a variable parameter.

This corresponds to the more lightly doped regions of the device. If the compensation ratio is fairly small (ie. few traps) then from equations (1) and (3) the transport properties are superior, and f_T increases. If, on the other hand, the trap level is on the same order of magnitude as the shallow-level donor concentration, then the compensation ratio approaches one. This corresponds to extreme degradation of mobility and velocity and, thus, forces f_T to decrease.

In conclusion, deep level traps in ion-implanted devices degrade carrier transport properties in the semiconductor material. The degradation is more severe near the tail of the implant profile than near the peak. Thus, the transport properties of the device will be depth — or bias — dependent. A modeling technique which accounts for this dependence has been used to study device properties as a function of fabrication parameters and deep-level trap concentrations. The results indicate that low energy implants should posess superior high-frequency properties and that lowering the trap levels in the material should improve device performance.

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ELECTRON CONCENTRATION AND ALLOY COMPOSITION DEPENDENCE OF HALL FACTOR IN $Ga_xIn_{1-x}As_yP_{1-y}$

Indexing terms: Semiconductor devices and materials, Hall effect, III-V semiconductors

The Hall factor is calculated by the iterative method over the whole composition range of $Ga_xIn_{1-x}As_yP_{1-y}$ lattice-matched to InP. The electron concentrations used are 1×10^{16} cm^{-3} and 1×10^{17} cm^{-3}, with carrier compensation ratios $(N_D + N_A)/n$ 1, 2, and 5, which are commonly observed in grown GaInAsP alloys. The Hall factor decreases with increasing alloy content y for relatively low electron concentrations, but this is not the case in compensated alloys because of varying predominance of scattering mechanisms with composition and ionised impurity concentration.

There is rapidly growing interest in the transport properties of GaInAsP alloys lattice-matched to InP.[1-10] Improved FET performance is expected for GaInAsP because of its higher electron mobility[1-3,5-10] and higher electron drift velocity[2,3,8,9,11] than those of GaAs. In the analyses of these transport properties the measurement of low-field mobilities is one of the essential evaluations. The mobility is usually derived from a combination of the resistivity and the Hall-effect measurement, and the thus derived mobility is the Hall mobility. On the other hand, the slope of the velocity/field curve at a

low electric field strength, which is equal to the drift mobility, is very often normalised by, or compared with, the measured Hall mobility. However, the Hall mobility μ_H is not generally equal to the drift mobility. The ratio μ_H/μ_D is the Hall factor r_H. This factor also correlates the carrier concentration n and the Hall coefficient R_H through the equation $n = r_H/eR_H$ where e is the electronic charge. In the limit of high magnetic fields, and/or carrier degeneracy, r_H approaches unity, $\mu_H = \mu_D$ and the carrier concentration can be derived directly from a measured Hall coefficient. However, it is not practical to attain the high magnetic field limit, and so for many applications nondegenerate semiconductors are of interest.

There are a few experiments of the determination of the Hall factor r_H in GaInAsP from comparisons of Hall mobilities at low and high magnetic field.[5,12] Although measured values are close to unity, one paper[5] reported that it was equal to or less than 1, and others[12] observed it equal to or greater than 1. Since the Hall factor has a dependence on scattering mechanisms, its value varies with the carrier concentration and the composition of GaInAsP alloys. There are no reports of the Hall factor covering the whole alloy composition of GaInAsP which show the carrier concentration dependence.

In this letter, we show the calculated Hall factors in GaInAsP over the whole alloy composition lattice-matched to InP in a moderate electron concentration range between 1×10^{16} cm^{-3} and 1×10^{17} cm^{-3} at 300 K.

The calculation method is an iterative technique in which the Boltzmann equation is solved by numerical iteration.[13-15] Both the drift mobility and the Hall mobility are calculated to any arbitrary degree of convergence without using the relaxation time approximation,[16] Matthiessen's rule, or complicated mathematical expressions.[17-19] All the calculations in this letter are carried out within 0·5% error. The allowed scattering mechanisms are polar-optical phonon scattering, acoustic phonon scattering, piezoelectric scattering, ionised-impurity scattering and alloy scattering. The quaternary alloy scattering rate proposed by Littlejohn *et al.*[20] is used with the Phillips electronegativity difference for the scattering potentials.[20,21] The material parameters for the quaternary alloy were evaluated by the linear interpolation between InP and $In_{0.53}Ga_{0.47}As$. Some of the parameters of InP and $In_{0.53}Ga_{0.47}As$ used in the calculations are listed in Table 1. The electron distribution function is the Fermi–Dirac function because the electron distribution in $In_{0.53}Ga_{0.47}As$ may degenerate at a relatively low electron concentration ($n = 2 \times 10^{17}$ cm^{-3} at 300 K).

Figs. 1a–c show the calculated Hall factor as a function of the alloy composition y in $Ga_xIn_{1-x}As_yP_{1-y}$. Carrier compensation ratios $(N_D + N_A)/n$ are 1, 3 and 5, respectively. Here, N_D, N_A and n are the donor concentration, the acceptor concentration, and the free-electron concentration, respectively. In the model both the donor and acceptor are assumed to be fully ionised, so that n is equal to $(N_D - N_A)$ and $(N_D + N_A)$ is the total ionised impurity concentration. As a general tendency in a purer alloy semiconductor, the Hall factor decreases with increasing alloy composition y. This comes from the decreasing phonon energy with composition y, as can be seen from Table 1. The value of the Hall factor for

Table 1 SOME OF THE MATERIAL PARAMETERS OF InP AND $In_{0.53}Ga_{0.47}As$ USED IN THE CALCULATIONS†

	InP	$In_{0.53}Ga_{0.47}As$
Effective mass ratio m^*/m_0	0·08	0·041
Static dielectric constant ε_0	12·35	13·77
Optical dielectric constant ε_∞	9·52	11·38
Optical phonon Debye temperature (K)	504	396
Energy gap at 0 K (eV)	1·42	0·812
Acoustic deformation potential (eV)	6·5	5·89
Piezoelectric constant (C/m^2)	0·035	0·099

† Linear interpolations between the two were used for material parameters of GaInAsP

The effective masses are found in Reference 24. Dielectric constants, energy gap at 0 K, acoustic deformation potential and piezoelectric constant of InP are found in Reference 13. Optical phonon energies are reported by Reference 25. Other parameters of $In_{0.53}Ga_{0.47}As$ are linearly interpolated between GaAs and InAs

polar-optical phonon scattering is a maximum at a temperature close to the Debye temperature of the polar optical phonon.[14,22] As the ambient temperature increases r_H falls. For GaInAsP the Debye temperature of the polar optical phonon varies from 504 K to 396 K with increasing y, so that at room temperature the value r_H decreases with increasing y. However, in a combination of several scattering mechanisms this general tendency is modified. Besides polar optical phonon scattering, alloy scattering and ionised-impurity scattering are the influential scattering mechanisms in a moderately doped alloy at room temperature. The combination of alloy scattering flattens the temperature dependence of the Hall factor, but the value at 300 K is little changed.[23] On the other hand, the combination of ionised impurity scattering and polar-optical phonon scattering tends to make the total scattering rate less momentum-dependent, so that the value of the Hall factor decreases. When the scattering rate is independent of carrier momentum, the Hall factor is equal to 1. Because of the varying importance of the scattering mechanisms with the alloy composition y, the Hall factor does not necessarily decrease monotonically with increasing y in a moderately doped alloy. In the Figure the Hall factor has the lowest value 1·02 near $y = 0{\cdot}2$ at $n = 1 \times 10^{17}$ cm^{-3} and $R = 2$.

At a higher carrier compensation ratio the Hall factor increases because of the predominance of ionised-impurity scattering which has a Hall factor as large as 1·93.

In summary, the Hall factor in $Ga_xIn_{1-x}As_yP_{1-y}$, dependent on electron concentration and alloy composition, has been calculated by the iterative method. In a moderate electron concentration range the Hall factor is greater than 1 over the whole composition. The results should be useful in the calculation of drift mobility and electron concentration from the resistivity and the Hall effect measurements in which the Hall mobility and the Hall coefficient are obtained.

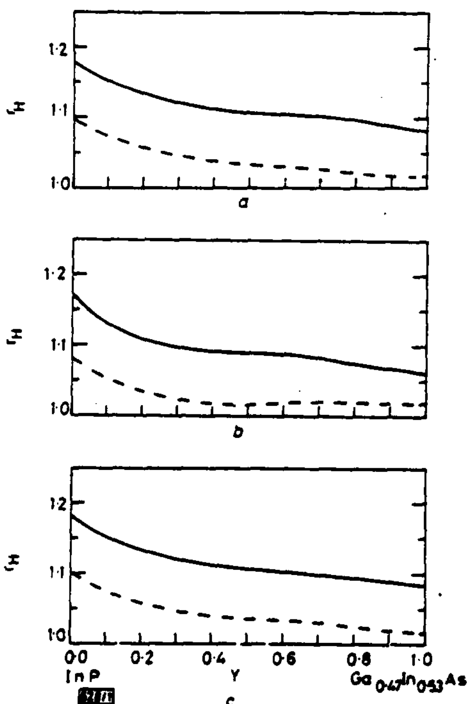

Fig. 1 *Alloy composition dependence of Hall factor in* $Ga_xIn_{1-x}As_yP_{1-y}$ *at 300 K*

Electron concentrations are 1×10^{16} cm^{-3} (solid lines) and 1×10^{17} cm^{-3} (dashed lines). Carrier compensation ratios $(N_D + N_A)/n$ are 1, 2 and 5, respectively

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Y. TAKEDA*
M. A. LITTLEJOHN
J. A. HUTCHBY**
R. J. TREW

5th August 1981

Electrical Engineering Department
North Carolina State University
Raleigh, NC 27650, USA

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* On leave from the Department of Electrical Engineering, Kyoto University, Kyoto 606, Japan
** Research Triangle Institute, Research Triangle Park, NC 27709, USA

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W-4

ODD ORDER IMPEDANCE MATCHING NETWORKS FOR LOW COST MICROWAVE INTEGRATED CIRCUITS*

A. N. Riddle and R. J. Trew
Electrical Engineering Department
North Carolina State University
Raleigh, NC 27650

(919) 737-2330

ABSTRACT

A new odd order impedance matching network with reduced sensitivity to active device capacitance variations is presented. A synthesis procedure for these networks is presented and experimentally verified with the construction of a microwave amplifier. These networks are useful in the development of low cost microwave integrated circuits since they reduce the harmful effects of device variations.

Introduction

In this paper a general analytic method is presented that extends network synthesis to include both even and odd order low-pass impedance matching filters. Previous network synthesis procedures for impedance matching filters were based on the use of even order filter structures. These odd order networks are important since they are relatively insensitive to variations in the capacity associated with a load impedance lower than the generator impedance. The insensitivity of these networks to capacitance variations can minimize or eliminate the costly tweaking of circuits caused by variations in the active devices. Two classes of polynomials are presented so that both broad-and narrow-band circuits may be designed.

Discussion

The development of even order matching filters [1] has proved very useful in amplifier design. It will be shown in this paper that odd order filters are unique in that they provide an insensitive circuit element instead of broadening the bandwidth of the impedance match.

The design procedure is based upon consideration of the fundamental relationship

$$|S_{11}(\omega)|^2 + |S_{21}(\omega)|^2 = 1, \qquad (1)$$

with

$$S_{11}(p) = \frac{D(p)}{E(p)}, \qquad (2)$$

$$S_{21}(p) = \frac{1}{\sqrt{\epsilon}\, E(p)}, \qquad (3)$$

and

$$\epsilon = \frac{(R_g - R_\ell)^2}{4 R_g R_\ell} \qquad (4)$$

where $p = \sigma + j\omega$. The terms R_g and R_ℓ are the generator and load resistances, respectively. The characteristic function, $D(p)$ may be defined by

$$D(p) = (1+bp)M(p^2), \qquad (5)$$

where the parameter b is proportional to the square of the parasitic capacity associated with the device to be matched. This parameter is set to zero for even order networks. The even polynomial, $M(p^2)$, may be defined according to the transformation presented in [1] for broad-band matching, or it may use the coefficients of the binomial expansion for narrow-band matching. During synthesis, the polynomial $M(p^2)$ determines the bandwidth and ripple of the impedance match, and approximate formulas for b in terms of the load capacity may be derived which thus define $S_{21}(p)$. Once $S_{21}(p)$ is defined, the derivation of a network is straightforward.

Theoretical Results

The relative insensitivity of the odd order low pass matching filters to variations in a shunt capacitor on the low impedance side of the filter may be demonstrated both analytically and experimentally. For the analytic case, the circuit of Fig. 1a was designed from a Cebysev prototype with b=1 and a fractional bandwidth of 31%. The VSWR plots in Fig. 1b were then obtained from the input of the filter as the capacitor on the low impedance side was varied ±50%. Fig. 2a shows an even order (n=4) Cebysev matching filter with the same parameters as the circuit in Fig. 1a except that b=0. By comparing Figs. 1b and 2b one may see that the synthesized filters give nearly identical response (solid curves), but that the ±50% variations in the component nearest the load causes much greater variations in the VSWR of the even order filter. For example, the midband VSWR is designed as 1.1, but reaches 1.67±.08 under variations in the even order filter while only becoming 1.34±.05 under variations in the odd order filter. The odd order matching filter thus uses the additional element for insensitivity instead of bandwidth.

Experimental Results

An amplifier using a Motorola MRF 901 bipolar transistor has been designed using a fifth order Cebysev matching network for the input circuit, and the lossy gain equalization circuit described in [2] for the output circuit. Fig. 3a shows the amplifier designed for operation from 650 MHz to 900 MHz at a bias current of 5 mA and 5v V_{CE}. The parameters of the input circuit design were b=3, R_ℓ = 13 ohms, f_o = 800 MHz and A = .3115. This circuit design produced a theoretical and experimental gain of 15.9±.8 db from 650 to 900 MHz.

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The insensitivity of the odd order matching network to changes in the device's input capacity is illustrated in Figs. 3b,c which compares the odd order matching network with an ideal transformer. Fig. 3b shows the VSWR of the amplifier with an odd order matching network in theory and experiment as well as with an ideal transformer of 1.58:1 turns ratio. The curves are represented by solid, dashed and alternating lines, respectively. While Fig. 3b shows reasonable VSWR response in all cases, it is Fig. 3c which shows the need for odd order matching filters. Fig. 3c shows the change in VSWR when a 5 pF capacitor, giving approximately 30% more input capacity, is placed in parallel with the transistor's base-emitter junction. The change in VSWR for the ideal transformer matched amplifier is obviously greater, and thus more sensitive, than the changes in both the theoretical and experimental odd order matching filter. This is because the shunt capacitor on the low impedance side of the filter does not contribute to the impedance increase needed for matching.

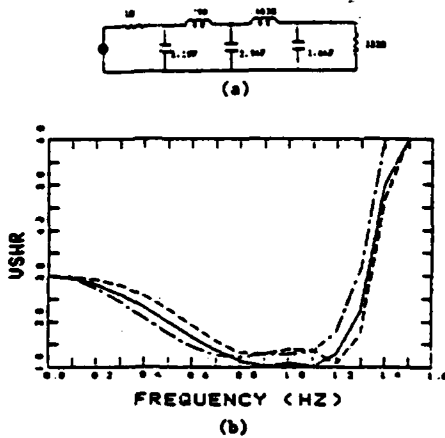


Fig. 1 (a) Odd order (n=5) Cebysev low-pass matching filter with a bandwidth parameter, A, of .31.
(b) The input VSWR of this network as the 1.64F capacitor, C_5, is varied ±50%. The solid dashed and alternating lines are for C_5 = 1.64F, 2.46F and .82F respectively.

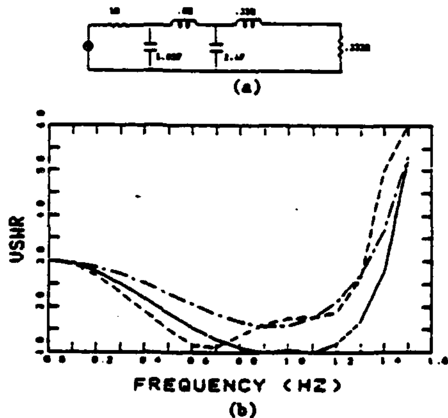


Fig. 2 (a) Even order (n=4) Cebysev low-pass matching filter with a bandwidth parameter, A, of .31. This is the filter of Fig. 1(a) with b=0.
(b) The input VSWR of this network as the .35H inductor, L_4, is varied ±50%. The solid, dashed and alternating lines are for L_4=.35H, .525H and .175H respectively.

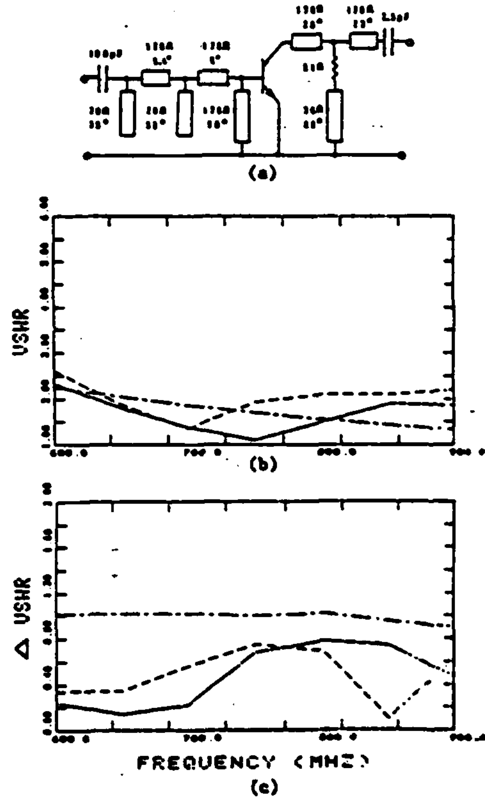
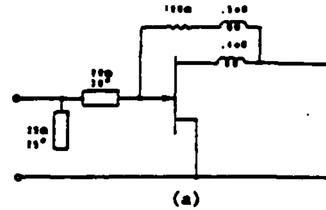
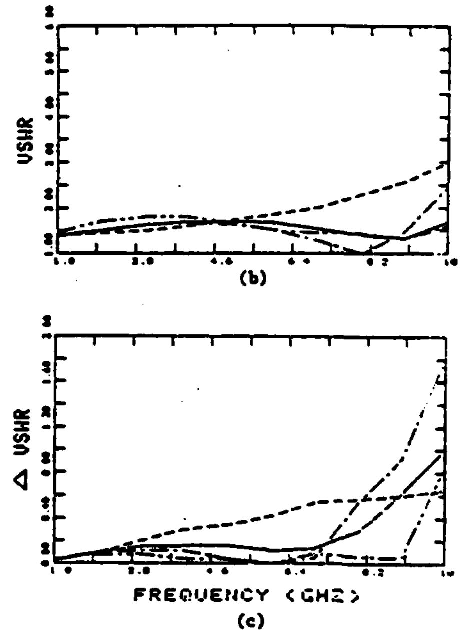


Fig. 3 (a) MRF-901 amplifier with distributed fifth order matching filter. Note the 100 pF blocking capacitor and 90° long transmission line are for the bias network only.
(b) VSWR of MRF-901 amplifier in theory (solid line), experiment (dashed line) and when the input network is replaced by a 1.58:1 ideal transformer (alternating line).
(c) Change in VSWR of MRF-901 amplifier as a 5 pF capacitor is placed across its base-emitter junction. Same line equivalences as in (b).

These networks can also be used to improve the insensitivity of broadband F.E.T. feedback amplifiers. Such an amplifier was designed using an Avantek AT-8111 F.E.T. chip biased at approximately 35 mA and 4v V_{DS}. The circuit shown in Fig. 4a produces 5±.3 db gain from 1 to 10 GHz and an input VSWR shown by the solid curve in Fig. 4b. The dashed, alternating and double alternating curves in Fig. 4b represent variations of the circuit in Fig. 4a with no matching network, a Smith chart matching network design, and a fifth order Cebysev matching filter; respectively. Note how the circuit exhibits a rising VSWR versus frequency with no matching network (dashed curve), and a VSWR which goes to 1:1 and then rises sharply above 8.2 GHz for the tuned characteristics of the Smith chart matching network (alternating curve). The analytic matching networks of third and fifth order both exhibit smooth VSWR curves oscillating around 1.5:1 and never exceeding 1.82:1. The capacitor in the matching network nearest the device is actually the intrinsic device capacity, and thus is accounted for in the design but not present in the circuit layout. The Smith chart design method inherently accounts for the device input capacity, and so forms an odd order matching network albeit of nonoptimal design. The curves of Fig. 4c show the change in VSWR of each circuit when the F.E.T. input capacitance is raised by 30% (.195 pF). Note how the circuit with no matching network exhibits a rising change in VSWR versus frequency, while all the odd order matching networks exhibit a very low change in VSWR up to some break frequency. Thus, these matching networks trade insensitivity at most frequencies for an increased sensitivity at very high frequencies. The Smith chart matching netwrok (alternating curve) has the lowest break frequency and highest sensitivity at 10 GHz as shown in Fig. 4c, and so is not the optimal matching network. The fifth order network (double alternating curve) shows a very low VSWR change up to 9 GHz which makes it the optimum network for increases in capacity. The poor performance of the fifth order network for reductions in capacity may make this network less than optimum in some situations. The analytically designed third order network gives an overall improvement over the Smith chart matching network, and no matching network in all capacitance variations. Thus, this method of analytic matching network design is shown to yield improved and relatively insensitive circuit designs.


(a)



(b)

(c)

Fig. 4 (a) Avantek AT-8111 broad-band F.E.T. amplifier with a distributed third order matching filter.
(b) VSWR of AT-8111 amplifier for input networks consisting of third order matching filter (solid line), no matching network (dashed line), Smith chart designed matching network (alternating line), and fifth order matching filter (double alternating line).
(c) Change in VSWR of AT-8111 amplifier as a .195 pF capacitor is placed across its gate-source leads. Same line equivalences as in (b).

Conclusion

In conclusion, the theory of low pass matching filters is extended to include odd order networks. The analytic theory presented here should be of particular use in designing internal matching networks for bipolar transistors and F.E.T.'s. These odd order networks offer reduced sensitivity to parasitic capacity variations in active devices, thus potentially reducing the cost of monolithic circuits by eliminating tuning.

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Effects of two longitudinal optical-phonon modes on electron distribution in $Ga_xIn_{1-x}As_yP_{1-y}$

Yoshikazu Takeda,[a] M. A. Littlejohn, and R. J. Trew
Electrical Engineering Department, North Carolina State University, Raleigh, North Carolina 27650

J. A. Hutchby
Research Triangle Institute, Research Triangle Park, North Carolina 27709

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GaInAsP quaternary alloys are known to have two or three longitudinal optical (LO)-phonon modes. The two-LO-phonon model was employed for the electron distribution and drift mobility calculations. Perturbation distribution has sharp drops due to the two-LO phonons and these drops cause a further downward bowing of the mobility along the arsenic composition compared with a one-LO-phonon model which has mostly been used.

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There has been a great interest in GaInAsP alloys lattice matched to InP for their applications to optoelectronic devices[1-3] and potential applications to high-speed logic devices.[4-6] Better performance in GaInAsP than GaAs of high-frequency field-effect transistors and high-speed logic devices is expected because of its higher electron mobility[4,5,7-9] and higher drift velocity[4,10-11] than GaAs. Though the experimental verification of these electron transport properties is being carried out, the mechanism of the electron transport in this alloy is not very clear. There are two main problems. One is alloy scattering due to the random arrangement of atoms in the alloy, and the second is the multiphonon modes observed in this alloy.[12,13] The problem of alloy scattering in this alloy has been discussed by several authors.[4,5,7,8,11,14] However, they assumed the one-longitudinal optical (LO)-phonon model in this alloy except for Ref. 14, and this assumption contradicts the experimental observation. We have reported the theoretical calculation of the electron Hall mobility using the two-LO-phonon model and have shown a good agreement between the calculation and experiments.[14]

In this letter, we report the effects of the two LO-phonon modes on the electron distribution, especially on the perturbation distribution in GaInAsP, and clearly illustrat[e] the reason the electron mobility calculated for the two-LO phonon model is lower than that for the one-LO-phonon model.

The calculation method of the mobility is the iterativ[e] technique.[15,16] The electron distribution function $f(\mathbf{k})$ unde[r] the influence of a small electric field can be expressed as $f(\mathbf{k}) = f_0(k) + \cos\theta g(k)$, where $f_0(k)$ is the equilibrium distri[bu]tion, $\cos\theta$ is the cosine between the momentum $\mathbf{k}$ and elec[tric] field $\mathbf{F}$, and $g(k)$ is the perturbation distribution. The Boltzmann equation is solved for $f(\mathbf{k})$. After substituting $f(\mathbf{k})$ with $f_0(k) + \cos\theta g(k)$, the Boltzmann equation is multiplie[d] by the first-order Legendre polynomial $\cos\theta$ and integrate[d] over θ. The remaining equation for the one-LO-phonon model is

$$S_0 g(k) = S^{+}_{ipo} g(k^{+}) + S^{-}_{ipo} g(k^{-}) - \frac{eF}{\hbar}\frac{\partial f_0(k)}{\partial k}, \quad (1)$$

where S_0 is the total scattering rate and consists of the scat[tering]-out rate by the LO-phonon absorption (S^{+}_{opo}), and by the LO-phonon emission (S^{-}_{opo}), and the differences betwee[n] the scattering-in rate and scattering-out rate for all elastic scattering processes of piezoelectric scattering (S_{pe}), acousti[c] phonon scattering (S_{ac}), ionized impurity scattering (S_{ii}), an[d] alloy scattering (S_{al}). Thus $S_0 = S^{+}_{opo} + S^{-}_{opo} + S_{pe} + S_{ac} + S_{ii} + S_{al}$. These scattering rates for the elastic process ar[e]

[a]Present address: Department of Electrical Engineering, Kyoto University, Kyoto 606, Japan.

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equal to the inverse of the relaxation times. $S^{+}_{ipo}(S^{-}_{ipo})$ is the scattering-in rate by the LO-phonon emission (absorption). The electron in the state of $k^{+}(k^{-})$ which is the momentum evaluated at the energy corresponding to E plus (minus) the energy $\hbar\omega_{po}$ of the LO phonon may be scattered into the momentum state k by the phonon emission (absorption). The expressions for all these scattering rates are found in Refs. 15 and 17 for alloy scattering.

For the two-LO-phonon model the scattering process by the LO phonon can be separated into two, i.e., the scattering by the InP-like phonon and by the GaInAs-like phonon.[12] If $S^{+}_{opoI}(S^{+}_{opoG})$ represents the scattering-out rate of the electron in the momentum state k by the absorption of the InP-like (GaInAs-like) LO phonon, the scattering rate includes a weighting factor of $(1-x)(1-y)(y)$.[12,14] The coupling strength between the electron and the LO phonon is assumed to be proportional to the concentration ratio of InP and GaInAs in the quaternary alloy $Ga_xIn_{1-x}As_yP_{1-y}$. The Raman scattering intensity by the InP-like and the GaInAs-like LO phonon was observed to be proportional to the concentration.[12] Similarly, the scattering-out rates by the emission of the LO phonons $(S^{-}_{opoI}, S^{-}_{opoG})$ and the scattering-in rates by the emission or absorption of the LO phonons $(S^{+}_{ipoI}, S^{+}_{ipoG}, S^{-}_{ipoI}, S^{-}_{ipoG})$ are weighted by the corresponding concentration ratios. Thus, the Boltzmann equation for the two-LO-phonon model leads to

$$S_0 g(k) = S^{+}_{ipoI} g(k^{+}_{I}) + S^{+}_{ipoG} g(k^{+}_{G}) + S^{-}_{ipoI} g(k^{-}_{I}) + S^{-}_{ipoG} g(k^{-}_{G}) - \frac{eF}{\hbar}\frac{\partial f_0(k)}{\partial k}, \quad (2)$$

where $S_0 = S^{+}_{opoI} + S^{-}_{opoI} + S^{+}_{opoG} + S^{-}_{opoG} + S_{pe} + S_{ac} + S_{ii} + S_{al}$. The mode frequency of the InP-like LO phonon varies linearly from 350 cm^{-1} and that of the GaInAs-like LO phonon increases from 200 to 275 cm^{-1} with increasing y.[12] The drift mobility is calculated from the integration

$$\mu = \frac{1}{n}\frac{V}{3\pi^2}\int_0^{\infty}\frac{\hbar k^3}{F m_0 d} g(k)\, dk, \quad (3)$$

where n is the free-electron concentration,

$$d = \frac{m\, \partial E/\partial k}{\hbar^2 k}$$

is the augmented density of states,[15] and V is the crystal volume.

The calculated drift mobilities at 300 K for the one-LO-phonon model and the two-LO-phonon model are compared in Fig. 1. The electron concentration n is 1×10^{16} cm^{-3} and the carrier compensation ratio $(N_D+N_A)/n$ is 1. Here, N_D and N_A are the donor concentration and acceptor concentration and are assumed to be fully ionized. These curves should be compared with the previous calculation which predicted an upward bowing of the dirft mobility along the alloy composition y.[3] This was caused by the lower effective mass which was estimated by the interpolation method. The experimentally determined linearly varying effective mass gives the downward bowing of the mobility curve which is the general observation in experiments. A further bowing is observed in the two-LO-phonon model and it is very close to the experimental results.

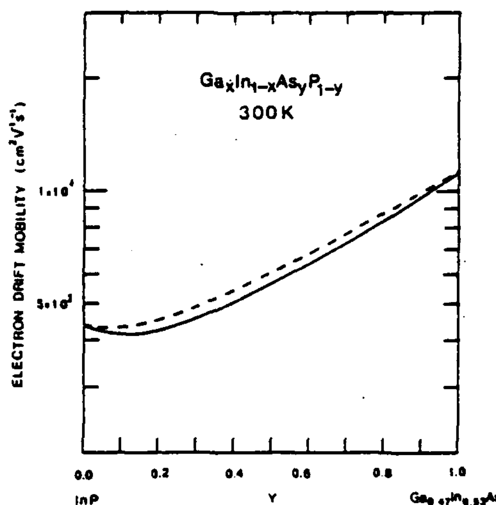

FIG. 1. Electron drift mobilities calculated by the iterative technique for the one-LO-phonon model (dashed line) and for the two-LO-phonon model (solid line). The electron concentration n is 1×10^{16} cm^{-3} and the carrier compensation ratio $(N_D+N_A)/n$ is 1.

Since the difference in the mobilities for the two models is largest at $y=0.2\sim0.3$, $y=0.3$, i.e., $Ga_{0.14}In_{0.86}As_{0.3}P_{0.7}$ is chosen to discuss the effects of the two LO-phonon modes on electron distribution. Some of the material parameters at $y=0.3$ used in the calculation are listed in Table I. These values are estimated from the linear interpolation between those of InP and $Ga_{0.47}In_{0.53}As$. In Fig. 2 the perturbation distribution $g(k)$ for the one-LO-phonon model (dashed line) and for the two-LO-phonon model (solid line) is shown as a function of the normalized momentum

$$X = \left(\frac{\hbar^2 k^2/2m^*}{k_B T}\right)^{1/2}$$

at 300 K. When the electron energy is equal to or greater than the phonon energy, the electron will lose its energy by emitting the phonons. In the one-LO-phonon model a sharp drop at $X=1.26$ is observed due to the LO-phonon emission of the energy 40.64 meV. In the two-LO-phonon model drops at $X=1.10$ (GaInAs-like phonon, 28.33 meV) and $X=1.30$ (InP-like phonon, 42.60 meV) are clearly illustrated. The fall in the curves at around $X=1.18$ is the perturbation due to the emission of two LO phonons. Since the drift

TABLE I. Material parameters at $y=0.3$ used in the calculation.

Parameter	Value
Effective mass ratio m^*/m_0	0.0683
Optical dielectric constant ϵ_∞	10.08
Static dielectric constant ϵ_0	12.78
Energy gap at 0 K (eV)	1.24
Optical phonon energy (K)	
one-LO-phonon model	471.6
two-LO-phonon model InP-like	494.4
GaInAs-like	360.3

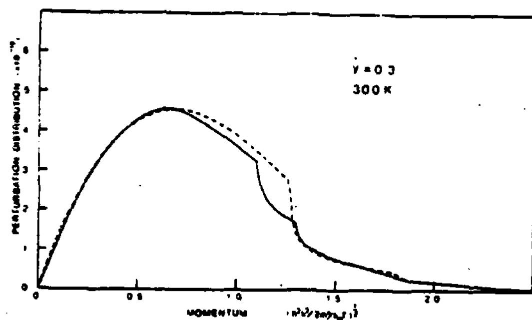

FIG. 2. Perturbation distribution as a function of the momentum. The one-LO-phonon model is the dashed line and the two-LO-phonon is the solid line. The sharp drops in the distribution are due to the phonon emission. In the two-LO-phonon model it has two drops corresponding to InP-like and GaInAs-like phonons.

mobility is proportional to the integral of the perturbation distribution as is clear from Eq. (3), the difference of these curves gives us the drift mobility differences; 5545 $cm^2V^{-1}s^{-1}$ for the one-LO-phonon model and 5132 $cm^2V^{-1}s^{-1}$ for the two-LO-phonon model. For the calculation of these mobilities the electron concentration 1×10^{15} cm^{-3} and the carrier compensation ratio 1 were used. The degree of a drop depends on the strength of the electron-phonon coupling. It will be straightforward to extend the model to the three or more LO phonons as observed by the far-infrared reflectivity study,[13] although the coupling strength of the electron to these phonons is still in question.

In summary, the electron drift mobility and the electron distribution in $Ga_xIn_{1-x}As_yP_{1-y}$ lattice matched to InP have been calculated by the iterative technique. The electron mobility is lower for the two-LO-phonon model than for the one-LO-phonon model over the whole composition y. The perturbation distribution in the two-LO-phonon model shows two sharp drops at the energies equal to the two LO-phonon energies which result with the lower electron mobility compared with the one-LO-phonon model.

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ENSEMBLE MONTE CARLO STUDIES OF HIGH FIELD SPIKES AND PLANAR DOPED BARRIER DEVICES*

by

R. J. Trew, R. Sultan, J. R. Hauser and M. A. Littlejohn
North Carolina State University
Raleigh, North Carolina 27650

ABSTRACT

This paper presents a study of the spatial ensemble velocities of electrons in GaAs which result from abrupt changes in electric fields occurring internal to a device. Calculations are presented for single field spikes as well as the complex field configuration which occurs in planar doped barrier transistor type devices. The calculations provide estimates of current gain and carrier transit times for PDB transistor structures. High current gains are found to require very narrow base widths.

INTRODUCTION

The ability to grow very thin semiconductor layers with accurately controlled doping has brought about new device concepts in recent years [1,2]. To improve high frequency performance many of the new device concepts attempt to use non steady-state electron dynamics such as ballistic transport or velocity overshoot which occur over short distances when charge carriers are subjected to large electric fields. The GaAs planar doped barrier (PDB) illustrated in Fig. 1 is a rectifying junction [2] which, when fabricated with an accurately controlled doping profile, should demonstrate hot electron characteristics.

By combining two barriers, a PDB transistor structure can be formed as shown in Fig. 2. The basic idea is that carriers injected by forward bias over the larger of the two barriers will become hot carriers in the heavily doped base. Most of these carriers should have high velocity and sufficient energy to traverse the smaller collector barrier. Interest in such device structures has provided the motivation for the present ensemble Monte Carlo study of carriers subjected to abrupt changes in electric field.

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ABRUPT FIELD CHANGES AND HIGH FIELD SPIKES

Ensemble velocity profiles near an abrupt change in the electric field are shown in Fig. 3. Three examples are shown with the field for $x > 0$ being 20 kV/cm and for $x < 0$ taking on the three values of 2, 5 and 8 kV/cm. The curves in Fig. 3 show the general behavior of velocity overshoot expected as carriers enter a high field region. The high velocity transient, however, begins a considerable distance before the carriers enter the high field region with the velocity exceeding 2×10^7 cm/sec. Since the carriers cannot have their energy changed by the high field before exposure to the high field, this initial velocity increase cannot be due to hot carrier effects.

A detailed study of this pre-overshoot effect has demonstrated that it is not a hot carrier effect, but an ensemble effect on the carriers for $x<0$ due to the carrier boundary condition established by the high field region beginning at $x=0$. Basically, the low-field/high-field interface acts as an ideal carrier collecting boundary to the low field region. Thus, any carrier reaching the high field region has an extremely low probability of being back scattered into the low field region. The velocity distribution for x slightly less than zero must have essentially no particles with negative velocities.

The above discussion provides a simple explanation for the ensemble average velocity near the low-field/high field interface. Consider a drifted Maxwellian velocity distribution function with a mean velocity of v_o. A calculation of the ensemble average velocity of only the positive velocity particles yields

$$\langle v \rangle_+ = \sqrt{\frac{2kT}{\pi m^*}} \; \frac{\exp(-\mathcal{E}_o/kT)}{1 + \mathrm{erf}(\sqrt{\mathcal{E}_o/kT})} + v_o \qquad (1)$$

where $\mathcal{E}_o = (1/2)m^*v_o^2$. This simple expression has been found to give very good agreement to the low-field/high-field interface ensemble velocity when evaluated with appropriate v_o and kT parameters.

Confirmation of the above model is provided in Fig. 4 which shows the ensemble velocity for a high field spike of width 300Å beginning at $x = 0$. The circular points are velocities calculated for $x < 0$ when the $x = 0$ interface is replaced by an ideal collecting contact. The close agreement between the two curves verifies that the low-field/high-field boundary is acting like an ideal collecting boundary. The value of $\langle v \rangle_+ = 2.5 \times 10^7$ cm/sec calculated from (1) is in excellent agreement with the interface ensemble velocity. It is also noted in Fig. 4 that the velocity to the right of the high field spike is about 2×10^7 cm/sec and considerably above the 1 kV/cm steady state value (V_{ss}) of about 0.8×10^7 cm/sec. Thus, the high field spike has imparted a considerable component of x directed momentum to the ensemble of particles and this persists for a considerable distance beyond the high field spike.

PLANAR DOPED BARRIER TRANSISTORS

The assumed field profile and the resulting velocity profile for a PDB transistor structure is shown in Fig. 5. This particular structure has an emitter barrier height of 0.31 volts and calculations are shown for three collector barrier heights of 0.05, 0.10 and 0.15 volts, which give barrier height differences of 0.16, 0.11 and 0.06 volts. These calculations are for a base width of 2000Å. Other calculations have been made for base widths of 250Å and 1000Å.

The carrier velocity within the base region (0.03 μm $< z < .23$ μm) is lower than might be expected from simple ballistic arguments on single carriers. The velocity profile around the emitter field spike is similar to that for a single field spike as shown in Fig. 4. There is an initial rise to above 2×10^7 cm/sec before the high field region followed by a very narrow

peak in the velocity. The velocity within the base layer is lower than that following a single field spike because of some additional trapping of carriers between the two energy barriers within the base layer.

The collector region in the present calculations was taken as 18 kV/cm and of length 5000Å. The velocity shows a second peak in this region ($x > 0.25\ \mu m$) which is followed by a region of low velocity as carriers transfer to the upper (L) valley. The velocity in the collector region is found to depend on the height of the collector barrier as shown by the three curves.

Some carriers lose sufficient energy within the base layer to become permanently trapped there. (Carriers which transfer to the L valley will become temporarily trapped until they transfer back to the Γ valley). In the present calculations the trapped carriers constitute the base current and were removed from the ensemble as soon as they reached the collector barrier with insufficient energy to traverse it.

Fig. 6 shows calculated beta values as a function of base width for two barrier height differences. As would be expected, beta is a strong function of both base width and barrier height difference. The solid curves are based upon a simple model which assumes that $I_c = I_e \exp(-x_B/L)$ where L is a phenomenological parameter which was evaluated from the 1000Å base width calculations. The Monte Carlo calculations at 250Å and 2000Å are seen to agree reasonably well with this simple model. Beta values above 10 have been found to require base widths below 1000Å.

The average electron transit time for the transistor structures shown in Fig. 5 were in the range of 5-6 psec yielding gain-bandwidth products of $f_T \sim 30$ GHz.

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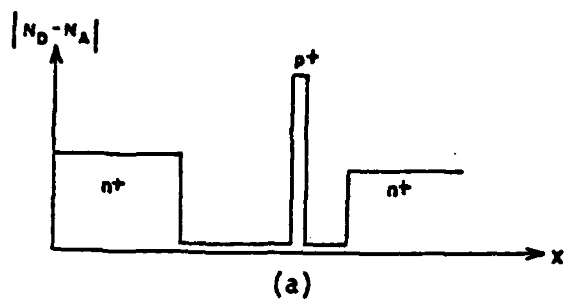

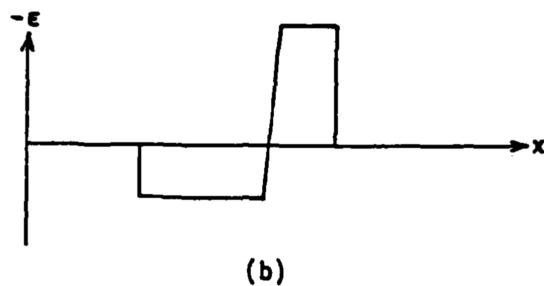

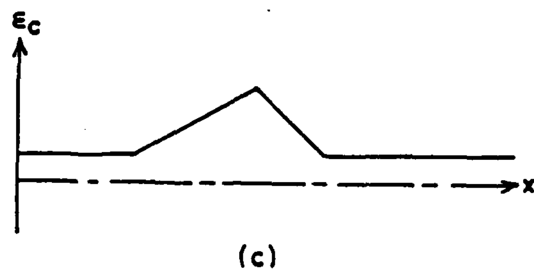

Figure 1. (a) Doping, (b) Electric Field, and (c) Conduction Band Profiles

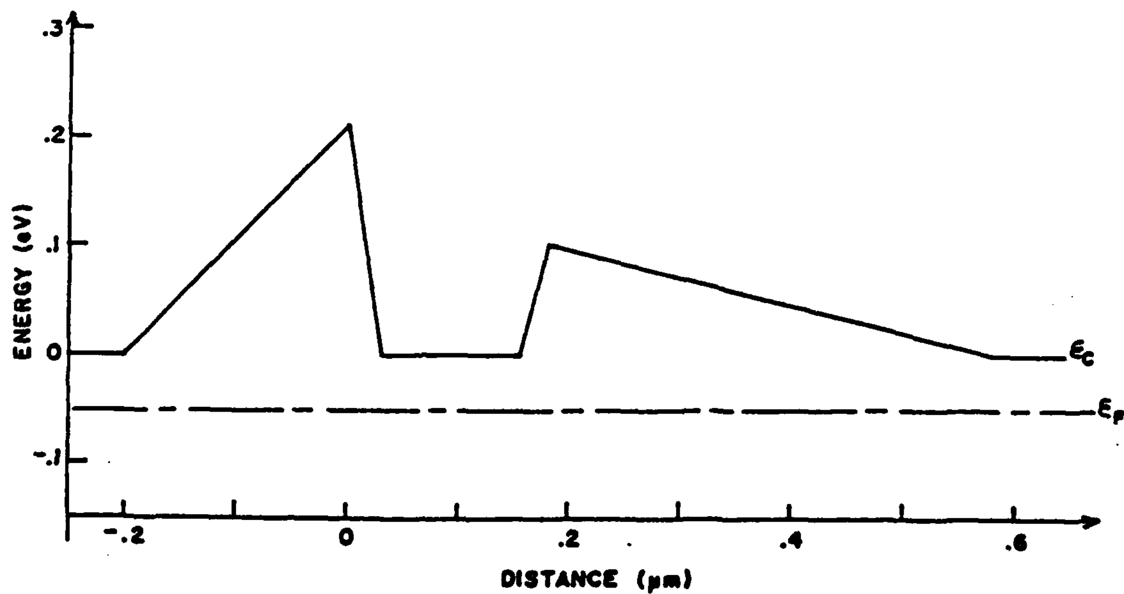

Figure 2. Energy Band Diagram for Planar Doped Transistor

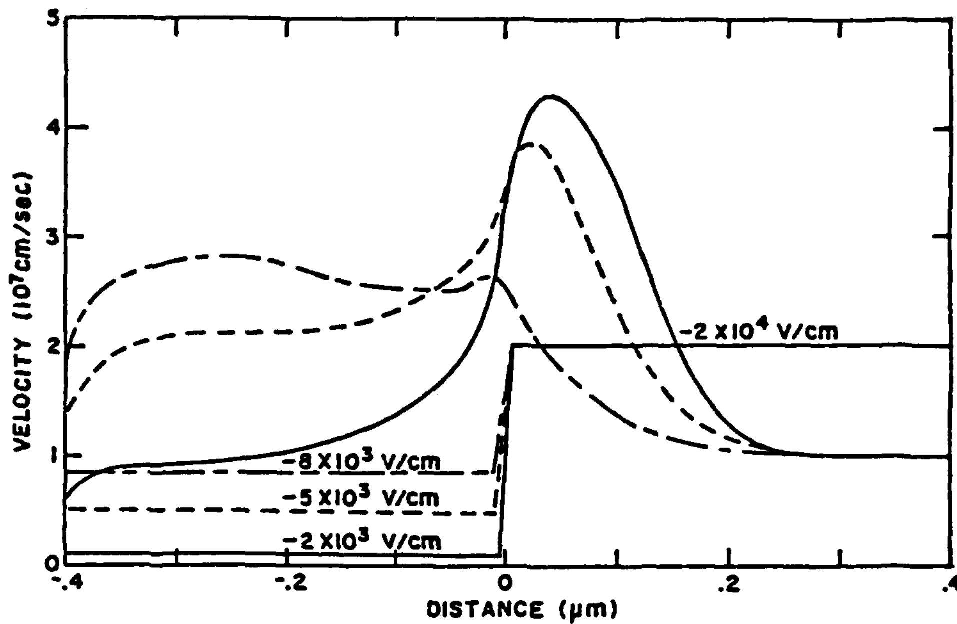

Figure 3. Ensemble Electron Velocity Near a Step in Electric Field

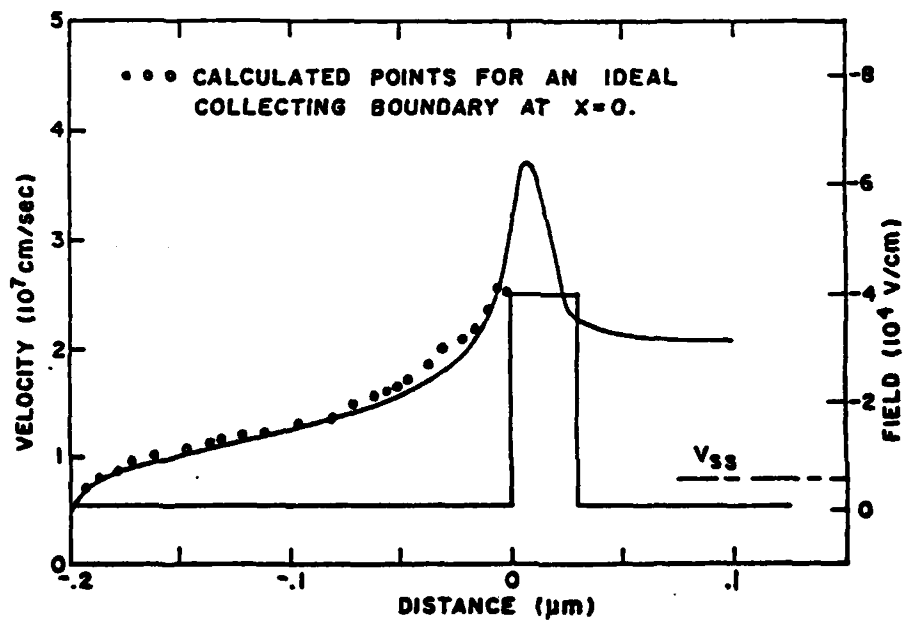

Figure 4. Typical Ensemble Velocity Profile Near a High Field Spike

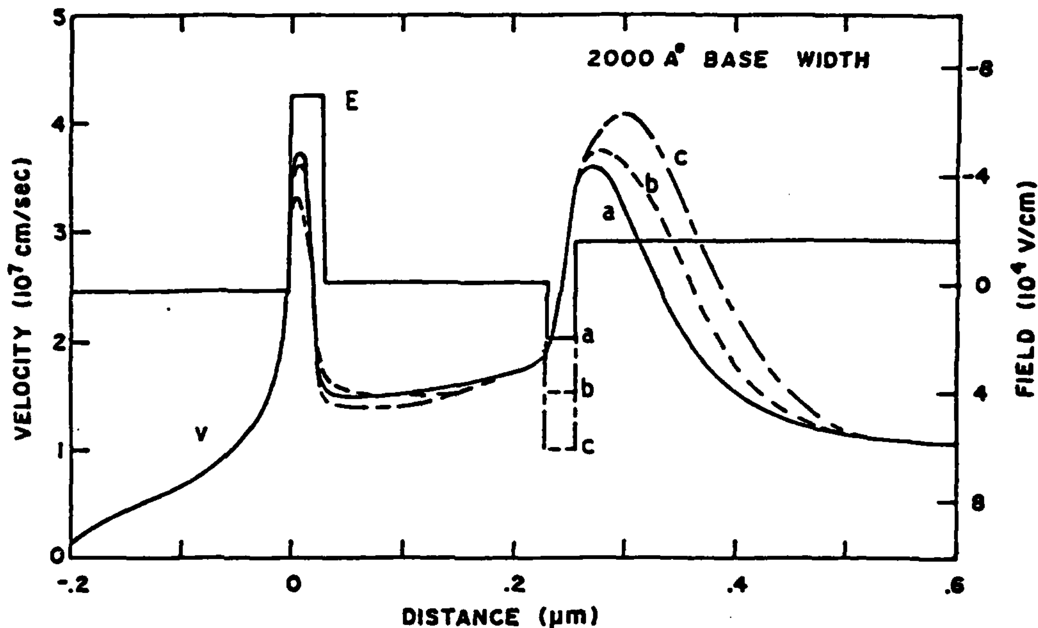

Figure 5. Ensemble Electron Velocities for the PDB Transistor with Collector Barrier Heights of 0.05 volts (curve a), 0.1 volts (curve b) and 0.15 volts (curve c) and an Emitter Barrier of 0.21 volts.

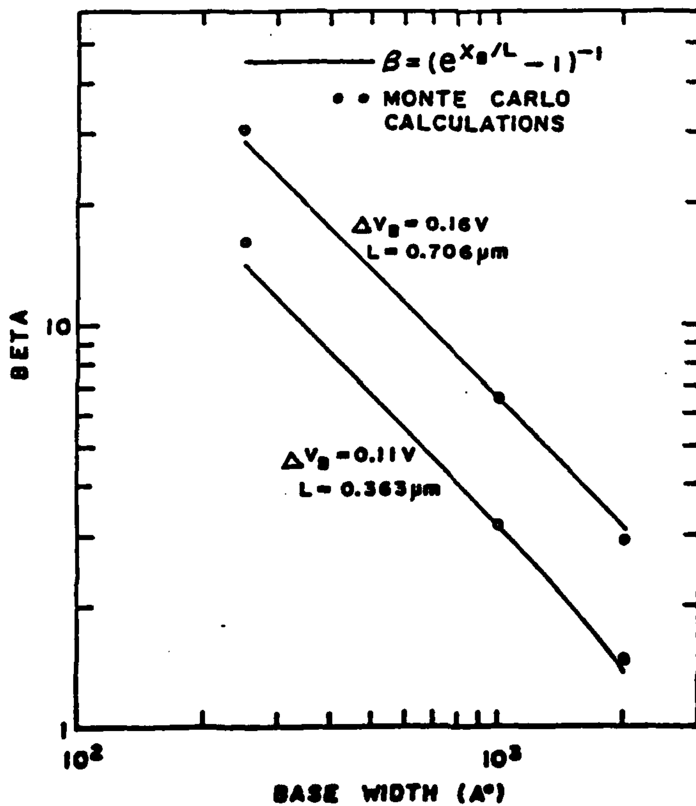

Figure 6. Calculated Curren Gains for the PDE Transistor as a Function of Base Width

PROFILE STUDIES OF ION-IMPLANTED MESFETs*

J. M. Golio and R. J. Trew

Electrical and Computer Engineering Department
North Carolina State University
Raleigh, North Carolina 27650

ABSTRACT

A study of ion-implanted MESFET performance as a function of the implantation energy and fluency and including the effects of deep-level trapping state concentrations in the substrate has been conducted. Carrier concentrations as a function of depth are determined through the use of LSS theory and a profiling model. An analytic device model, which computes both DC and RF characteristics, is then employed to predict MESFET performances. The study includes the effects of depth dependent transport properties and has indicated a number of design rules for the fabrication of optimized ion-implanted devices.

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INTRODUCTION

The performance of FETs fabricated by ion-implantation depends greatly on carrier concentrations and velocity-field characteristics as a function of depth into the active device layers. The presence of deep-level traps in the semiconductor contributes to the complexity of problems associated with the characterization of ion-implanted devices.

This paper presents the results of a study to determine the effects of various concentration and transport profiles upon device performance. The study utilizes theoretical models of both material properties and device characteristics. This information is combined with experimental material characterization to provide improved quantitative accuracy of the model.

Figure 1 outlines the modeling steps involved in obtaining the results to be presented. Initially, the determination of typical ranges for concentrations of deep-level trapping states, $N_T(x)$, was made from a novel measurement technique using both differential capacitance and conductance DLTS data. Shallow-level donor concentrations, $N_D(x)$, were then determined from LSS theory as a function of implantation parameters. These concentrations as a function of depth were then used in a profiling model to determine the free-carrier profile, $n(x)$, for the material. Carrier transport properties were also determined from the trap and donor profiles. This was done through the use of Monte Carlo particle simulations and a model to account for the effects of compensation in the semiconductor.

An analytic model which utilizes all of this information is then used to assess performance potential. The DC characteristics and small-signal S-parameters along with figures-of-merit are computed by the model. The distinction between free-carrier and donor profiles, the effect of deep-level traps, and the depth dependence of mobility and velocity are shown to be important considerations which have been ignored in previous models.

THE DEVICE MODEL

A one-dimensional analytic device model with a small-signal analysis has been developed and utilized for this work. The model is based upon the principles presented by Pucel [1] but has been generalized for arbitrary doping profiles and includes differences in the free-carrier and shallow-level donor profiles and the effects of deep-levels.

The model assumes that the electron transport properties of a material can be simulated by a two-piece velocity-field relationship. The two-piece approximation is defined from a theoretical velocity-field characteristic determined by Monte Carlo techniques. For electric fields less than an appropriate saturation field, E_m, the electron velocity is described by a linear expression,

$$v = \mu_o E. \tag{1}$$

For electric fields above E_m the electrons move at a constant, maximum velocity, v_m.

The low-field mobility as a function of depth into the channel is determined from the equation [2],

$$\mu_o = \frac{\mu_{max}}{1 + [\frac{\log N_D^1}{N_o}]^C}\,(1-\theta)^b, \tag{2}$$

where

$N_D{}^1 \;= N_D \cdot m^3,$

$\mu_{max} = 8380$ cm/Vsec,

$N_o = 23.2553,$

$C = 23.0,$

$\theta = N_T/N_o$

and

$$b = \begin{cases} A(\log N_D)^2 - B(\log N_D) + C & \text{for } N_D > 10^{21}\ m^{-3} \\ 0.114992 & \text{for } N_D < 10^{21}\ m^{-3}, \end{cases}$$

with $A = 0.025$,

$B = 0.817278$,

$C = 6.252838$,

and where N_D is given in m^{-3}.

Equation (2) gives the low-field mobility as a function of donor density and background compensation. To derive equation (2) the theoretical results of Walukiewicz et al. [3] were used in conjunction with Monte Carlo velocity-field predictions [4]. The Monte Carlo results were used to determine the mobility as a function of background donor density with no traps present, and the Walukiewicz values were then normalized to the Monte Carlo numbers. The normalized data were finally curve fit to obtain equation (2). Very good agreement is obtained when equation (2) is plotted against the normalized Walukiewicz values as shown in Figure 2.

The technique for determining the maximum velocity v_m has been previously presented [5,6,7]. The saturation velocity can be described by the expression

$$v_m = v_o - A \log [(1-y)^2 + B_y], \qquad (3)$$

where

$y = [N_D(x)/N_o]^{2.5}$,

$N_o = 1.5 \times 10^{22}\ m^{-3}$,

$A = 0.0262$,

$B = 0.4$,

and $v_o = 1.40 \times 10^5$ m/sec.

Equation (3) gives v_m in 10^5 m/sec when $N_D(x)$ is expressed in m^{-3}. The expression is assumed to have the same dependence upon compensation ratio θ as equation (2). Thus, the factor $(1-\theta)^b$ is multiplied with equation (3) to obtain v_m in the presence of traps. The exponent b is defined in equation (2).

Equations (2) and (3) in conjunction with knowledge of the three profiles, n(x) - the free-electron concentration, $N_D(x)$ - the donor concentration and $N_T(x)$ - the deep-level concentration, allow for the derivation of a device model which includes the effects of varying transport properties as a function of epi-depth. The profiles of interest are determined with a novel characterization technique [2] that combines experimental capacitance-voltage (C-V) and conductance deep-level transient spectroscopy (DLTS) data. The experimental equipment and procedure is discussed elsewhere [8].

For this work an ion-implanted one micron gate length device [9] was analyzed. The experimental characterization revealed the presence of a dominant deep-level donor state 0.736 eV below the conduction band. The level is probably EL2 [10,11] in agreement with the findings of Martin et al. [12]. The resulting free-carrier, shallow-level donor, and deep-level concentrations as a function of depth into the material are shown in Figure 3. Despite the scatter of the data near the tail, it is evident that diffusion of the electrons has caused the free-carrier and shallow-level donor concentrations to differ significantly. The low-field mobility versus depth obtained from this analysis is also shown in Figure 3. In regions of relatively high donor concentration the mobility varies inversely with doping, as expected. Near the tail of the implanted region, however, the deep-levels seriously degrade the mobility acting to confine the active device channel.

The dc I-V characteristics for the device as determined from the model are compared in Figure 4 with the measured I-V curves. It should be noted that without the inclusion of the effects of traps upon the carrier transport characteristics the excellent agreement shown in Figure 4 could not be obtained. The traps have a tendency to "soften" the pinch-off characteristics

of the device (i.e., when traps are included in the simulation, the slope dI_g/dV_g is not as great near pinch-off). For all of the devices studied in this work, this "softening" effect was required to obtain best agreement with the measured I-V characteristics.

The model allows the element values for a small-signal equivalent circuit as shown in Figure 5 to be determined. The equivalent circuit can be analyzed to obtain RF performance predictions as a function of the various implantation parameters and material characteristics.

RESULTS

The results that follow were obtained following the modeling steps outlined in the Introduction and illustrated in Figure 1. Three parameters were varied independently. They are 1) implantation energy, ε, 2) peak doping density, N_{max}, and 3) trapping state density, $N_T(x)$. The implant species was assumed to be Si in GaAs and the activation was assumed to be 100% for all devices. The gate length of the simulated devices is one micron with a gate width of 300 microns. The trapping state density was assumed to be constant as a function of depth for these studies. Note that the peak doping density can be converted to a corresponding ion fluency through the simple relationship

$$\Theta = \sqrt{2\Pi}\, \sigma_p N_{max} \tag{4}$$

where σ_p is the standard deviation of the projected range. The value for σ_p can be obtained from LSS theory when the implant schedule is known.

Figure 6a shows computed carrier profiles for the same 75 keV implant with $N_{max} = 2x10^{17}$ cm^{-3}, but for three different trapping state concentrations. The low-field mobility and maximum velocity profiles corresponding to these three cases are shown in Figure 6b. It is clear from the figures that the trapping state concentration in the material has a significant effect on both the free-carrier concentration and the transport

properties of the implanted material. The equivalent circuit element values that correspond to these cases are shown in Table I. The deep-level concentration has the most effect upon the device transconductance which decreases as the trap concentration increases and the gate delay time which increases with the trap concentration.

Table I

Ion-Implanted MESFET
Equivalent Circuit Element Values

$\varepsilon = 75$ keV, $N_{peak} = 2x10^{17}$ cm^{-3}
$V_{ds} = 3.0$ V, $I_d = I_{dss}$

Element	Deep-Level Concentration		
	$1x10^{14}$ cm^{-3}	$2x10^{15}$cm^{-3}	$1x10^{16}$cm^{-3}
g_m(mmho)	46.4	45.6	41.5
C_{gs}(pF)	0.419	0.417	0.399
Rdr(kΩ)	1.22	1.20	1.35
R_i(Ω)	3.337	3.423	3.680
τ(psec)	8.00	8.16	8.41
f_{max}(GHz)	66.1	64.5	61.8

The remaining parameters were constant with the values $C_{ds} = 0.0577$ pF, $C_{gd} = 0.0432$ pF, $R_d = 1.214$ Ω and $R_s = 1.214$ Ω.

For the implant energy and peak doping studies, the trapping state density was left constant at $N = 2x10^{15}$ cm^{-3}. This number was chosen to be in general agreement with the results shown in Figure 3. The implant energy was varied from 50 to 150 keV while the peak doping took values between $8x10^{16}$ and $4x10^{17}$ cm^{-3}.

The value for f_T is computed from first order considerations to be given by

$$f_T = \frac{g_m}{2\pi C_{gs}} . \quad (5)$$

The quantity f_{max} is obtained by noting the frequency at which Mason's unilateral gain (as predicted by the model) goes to unity . Mason's unilateral gain at a frequency of 10 GHz is plotted as a function of energy in Figure 8. The results clearly indicate the superiority of low-energy implants for high-frequency operation.

The information plotted in Figure 8 indicates the importance of implant energy to achieve optimum high frequency performance. Notice that for a peak doping of $4x10^{17}$ cm^{-3}, a decrease of implant energy from 150 to 50 keV results in better than a 9% increase in the unilateral power gain, from 16.2 dB to 17.7 dB. The superior high frequency performance of low energy implants is easily understood in terms of the device physics. The available charge carriers lie closer to the surface (gate contact) for low energy implants. Thus, the gate potential required to alter the depletion width is smaller than for deep implants and the transconductance of the device should rise. High transconductance is important to the high frequency performance of these devices. All of the devices considered in compiling Figures 7 and 8 were compared at a bias of $I_D = 10$ mA. The dashed line falling off rapidly at the low-energy end of the curves indicate that for energies lower than this, $I_{DSS}<10$ mA.

The trapping state concentration in ion-implanted semiconductor material can vary over a wide range of values. The quality of the initial semi-insulating substrate, the temperature characteristic of the various processing steps used, and the type of annealing implemented all affect the

kinds and relative concentrations of deep-levels in the final device [13,14]. For the trap study in this work, an implant energy of 75 keV and a peak doping density of 2×10^{17} cm^{-3} was assumed. The background trapping state concentration was varied from 0 to 10^{16} cm^{-3}. For trapping state concentrations above 10^{16} cm^{-3}, the device would be normally pinched-off.

Figure 9 illustrates the effects traps have on the zero gate bias current, I_{DSS}, and the pinch-off potential, W_{oo}. The trapping state density of the figure ranges between 10^{14} and 10^{16} cm^{-3}. Over this range the zero gate bias current varies between 30 and 18 mA, while the pinch-off potential varies between 1.62 and 1.38 volts. This large range of DC characteristics indicates that reproducibility will be a problem unless consistency of the trapping state density in the substrate can be maintained. It should be further noticed that for deep-level concentrations below a level of about 10^{15} cm^{-3}, very little change in the characteristics occurs. As the trapping state concentration increases above the low 10^{15} cm^{-3} level, however, the current and pinch-off potential begin to fall rapidly.

Figure 10 shows the pinch-off "softening" effect mentioned in the previous section for one particular device. Notice that the figure plots normalized current and voltage. Thus, the trapping state density affects the DC characteristics of the device in a qualitative as well as a quantitative way.

Deep-level traps also have some effect on the RF performance of the device as illustrated in Figures 11 and 12. Figure 11 shows clearly the decrease of f_T and f_{max} associated with increasing trapping state concentrations—especially for deep-level concentrations above the low 10^{15} cm^{-3} range. In Figure 12 note that for low bias currents f_T increases when few traps are present while it decreases for higher trap concentrations. This is easily explained in terms of the degrading effects traps have on

mobility and velocity. As the gate bias restricts current flow, a larger fraction of the carriers are forced deeper into the channel. This corresponds to the more lightly doped regions of the device. If the compensation ratio is fairly small (i.e., few traps) then from equations (1) and (3) the transport properties are superior, and f_T increases. If, on the other hand, the trapping state density is on the same order of magnitude as the shallow-level donor concentration, then the compensation ratio approaches one. This corresponds to extreme degradation of mobility and velocity and, thus, forces f_T to decrease.

CONCLUSIONS

It has been shown how deep level traps in ion-implanted devices degrade carrier transport properties in the semiconductor material. The degradation is more severe near the tail of the implant profile than near the peak. Thus, the transport properties of the device will be depth—or bias—dependent. A modeling technique which accounts for this dependence has been used to study device properties as a function of fabrication parameters and deep-level concentrations. The results indicate that low energy implants should possess superior high-frequency properties and that lowering the trapping state density in the material should improve device performance. For the 75 keV implant studied in this work, a critical deep-level concentration of about 10^{15} cm^{-3} was identified. For trapping state concentrations above this level performance degradation becomes increasingly severe. Decreasing deep-levels in ion-implanted devices below this critical trapping state concentration should improve device performance. It should be noted, however, that for a different implant schedule than the one considered here (i.e., 75 keV with $N_{max} = 2x10^{17}$ cm^{-3}) the critical trap density may be different.

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Figure 1 Flow-chart of modeling steps required to obtain study results.

Figure 2 Low-field mobility as a function of doping and deep-level compensation. The solid lines are computed from equation (2) for θ = 0.0, 0.2, 0.4, 0.6, 0.8. The data points are from the normalized theoretical computations [3].

Figure 3 Resulting concentration profiles and low-field mobility profile for one device.

Figure 4 Comparison of model predicted and measured I-V characteristics for a one micron ion-implanted device.

Figure 5 The equivalent circuit for an FET used in the analysis.

Figure 6a Concentration profiles for a 75 keV implant with $N_{max} = 2\times10^{17}$ cm^{-3} and with $N_T = 1\times10^{14}$, 2×10^{15}, 1×10^{16} cm^{-3}. The solid curve is the donor density while the dashed curves are free-carrier densities appropriate for the various trapping state densities.

Figure 6b Transport property profiles for the three 75 keV implants of Figure 6a. The solid curves give low-field mobility as a function of depth. The dashed curves give maximum velocity as a function of depth.

Figure 7a Predicted gain-bandwidth product, f_T, vs. implantation energy, ε. The peak doping, N_{max}, is used as an independent parameter.

Figure 7b Predicted maximum frequency of oscillation, f_{max}, vs. implantation energy, ε. The peak doping, N_{max}, is used as an independent parameter.

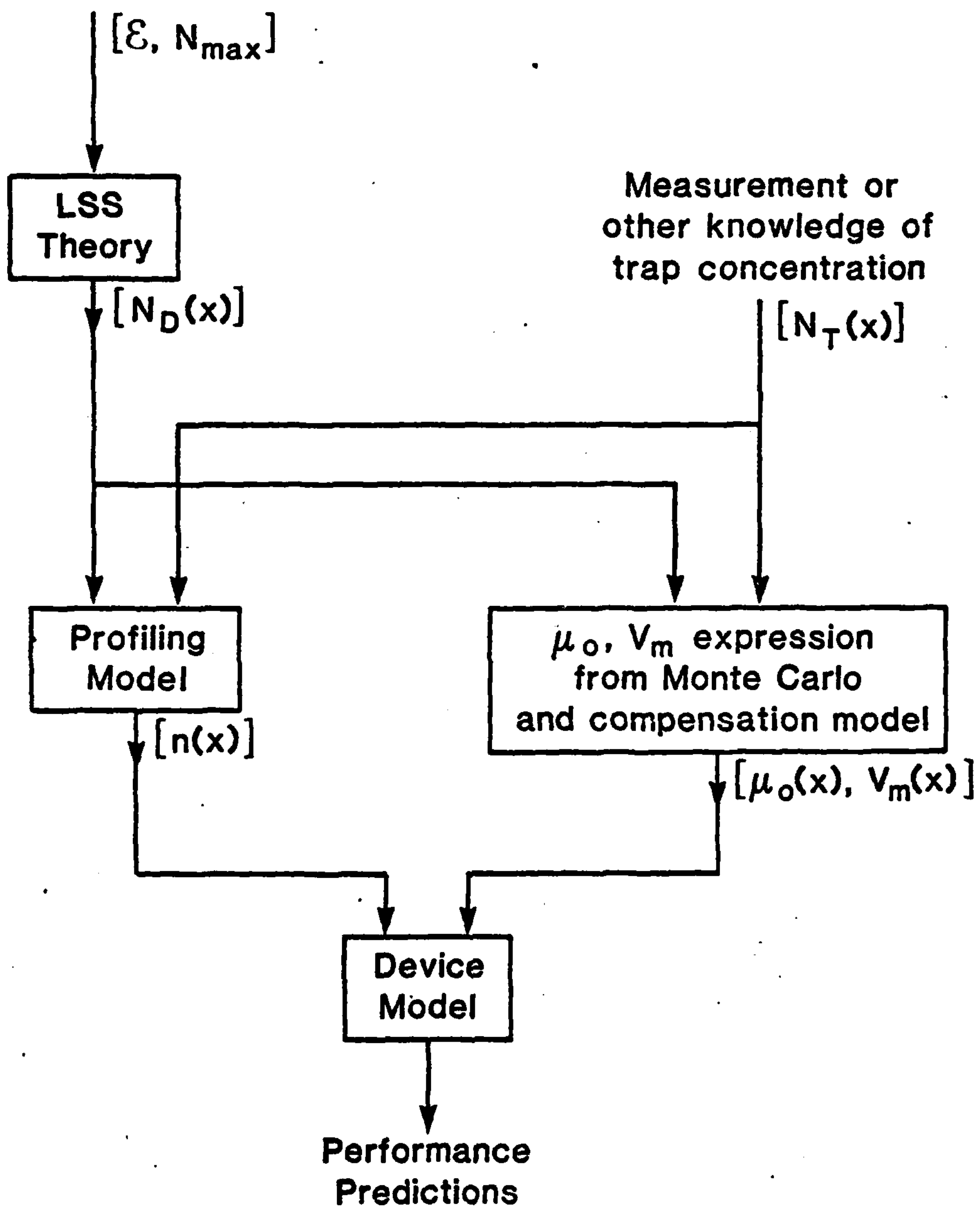
Figure 8 Mason's unilateral gain, U, at 10 GHz vs. energy, ε. trapping state density is constant at $N_T = 2\times10^{15}$ cm^{-3}.

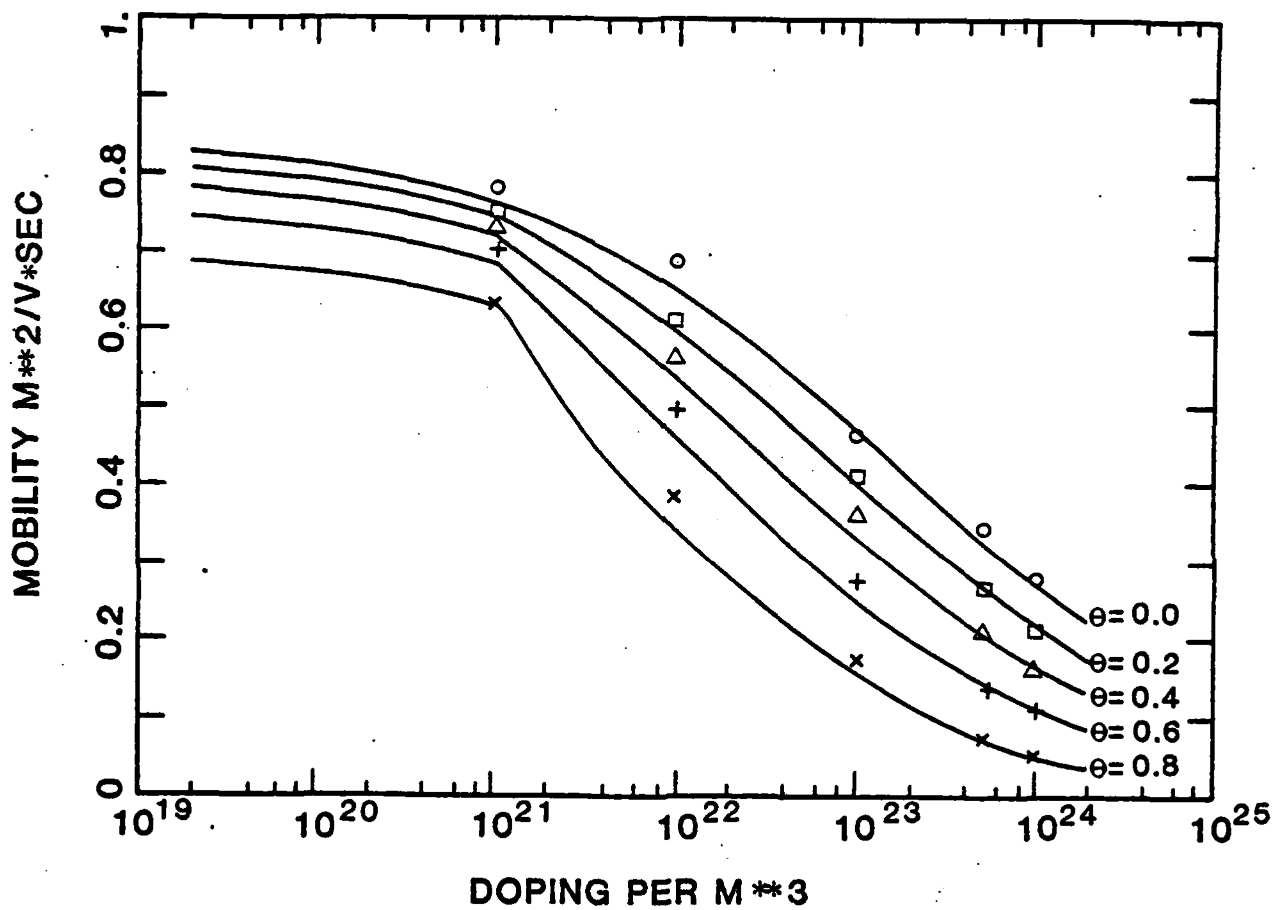
Figure 9 Predicted effects of varying trapping state concentrations on DC characteristics.

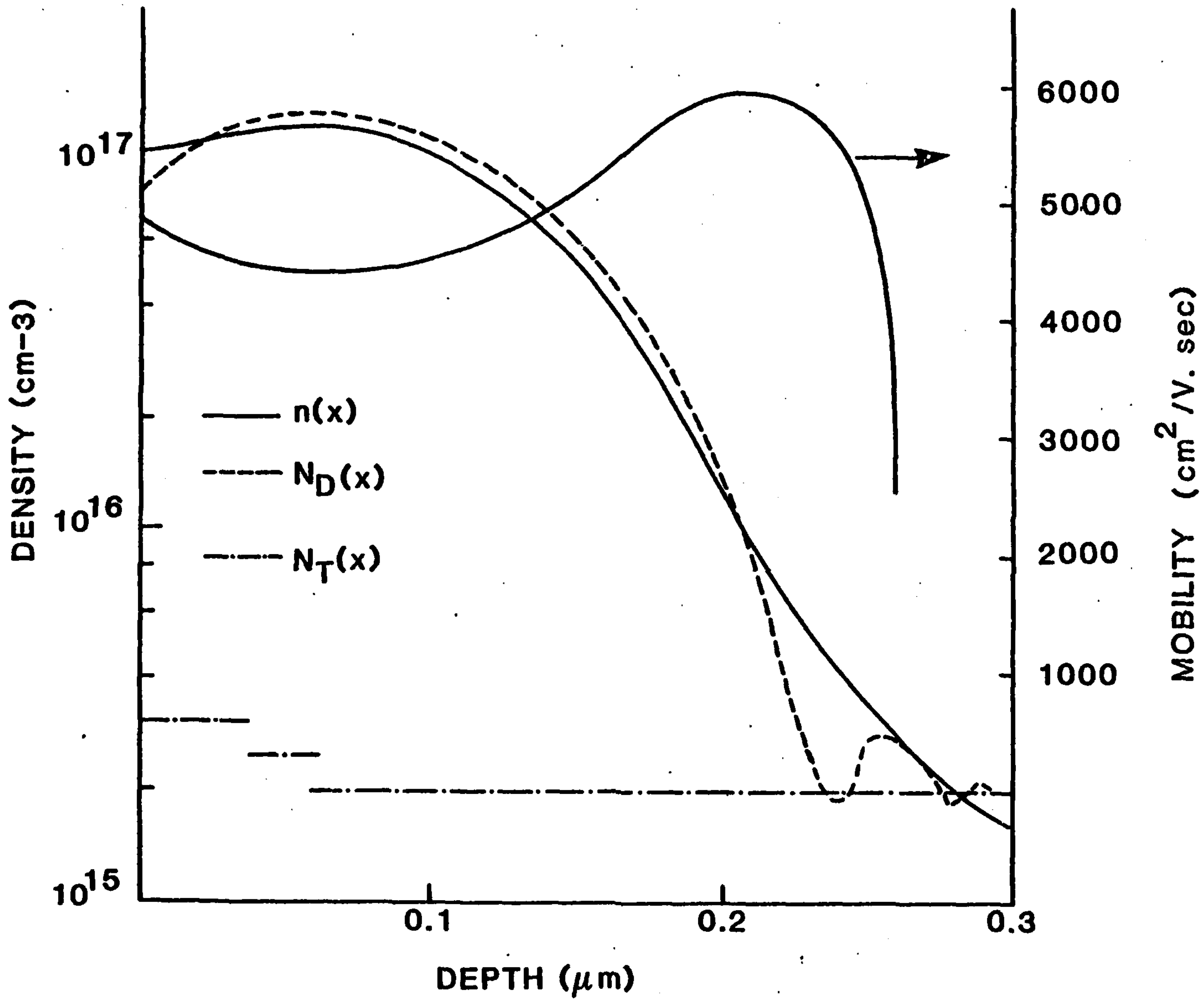
Figure 10 Normalized drain current predictions vs. normalized gate voltage with and without traps.

Figure 11 Predicted gain-bandwidth product, f_T, and maximum frequency of oscillation, f_{max}, vs. background trapping state concentration.

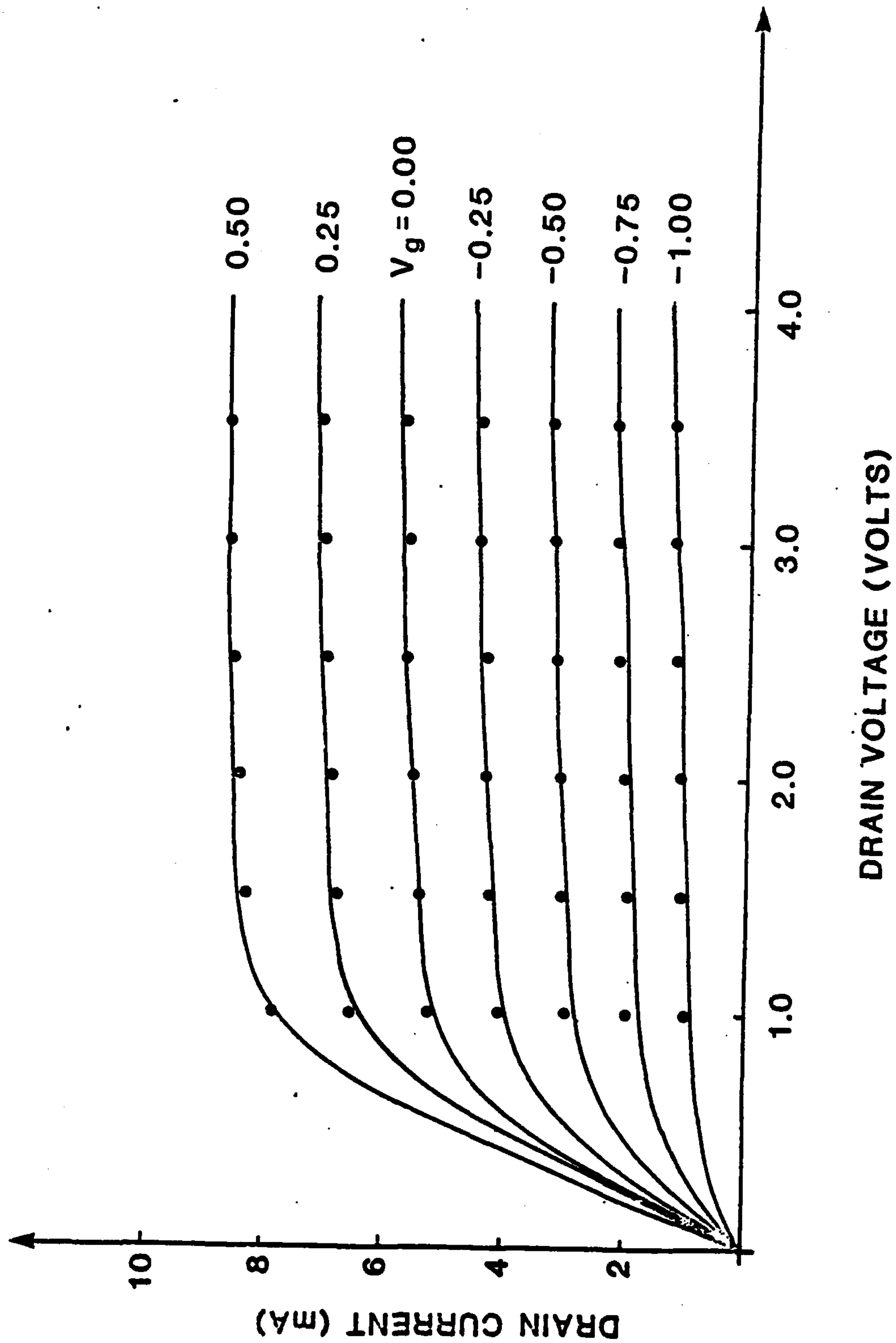
Figure 12 Predicted gain-bandwidth product, f_T, as a function of normalized drain current. The background trapping state concentration is used as a variable parameter.


Implant Energy,
Peak Doping, and
Implant Species
[$\mathcal{E}$, N_{max}]
LSS
Theory
[$N_D(x)$]
Measurement or
other knowledge of
trap concentration
[$N_T(x)$]
Profiling
Model
[$n(x)$]
μ_o, V_m expression
from Monte Carlo
and compensation model
[$\mu_o(x)$, $V_m(x)$]
Device
Model
Performance
Predictions

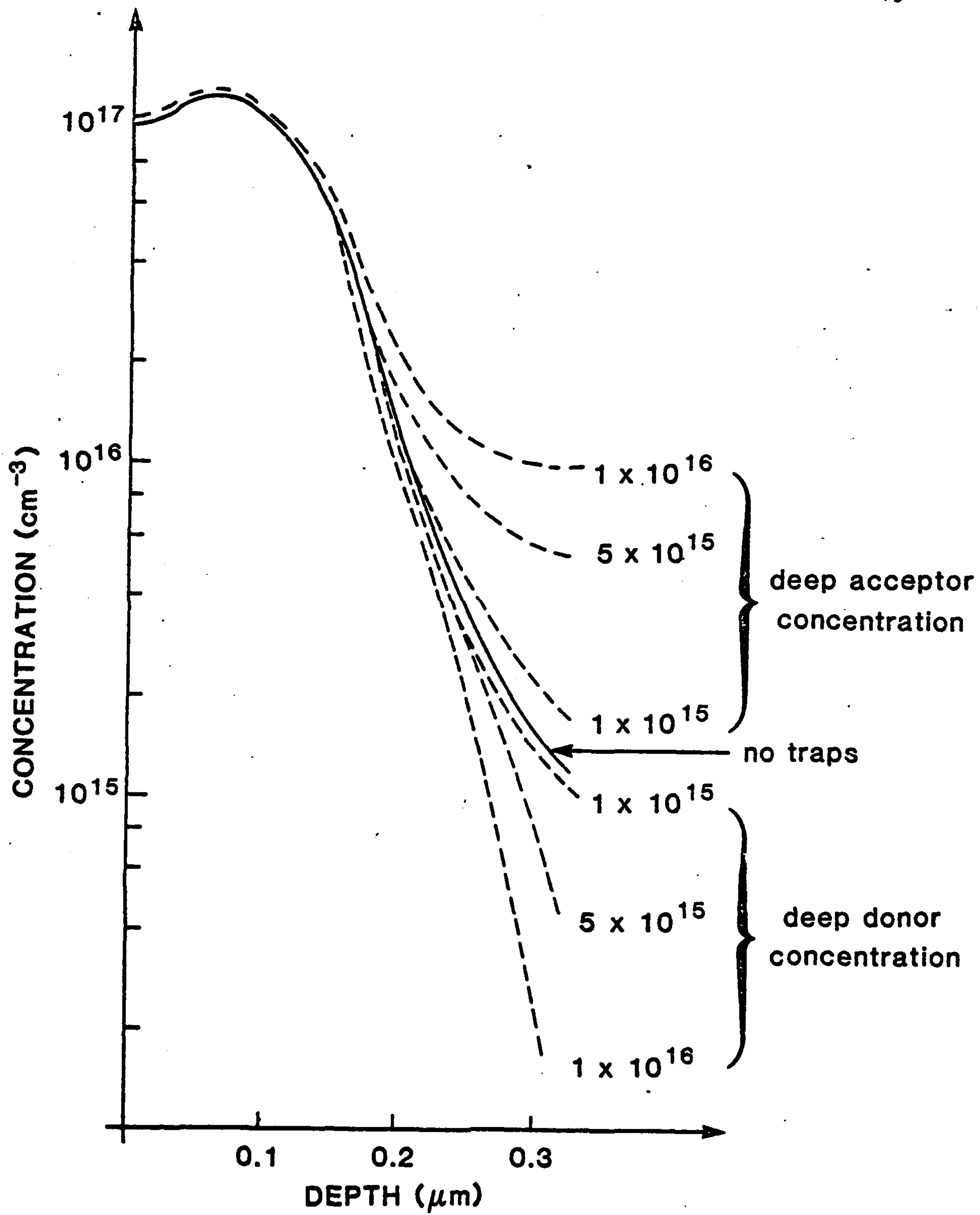

MOBILITY M**2/V*SEC
0
0.2
0.4
0.6
0.8
1.
10^{19}
10^{20}
10^{21}
10^{22}
10^{23}
10^{24}
10^{25}
DOPING PER M**3
θ= 0.0
θ= 0.2
θ= 0.4
θ= 0.6
θ= 0.8



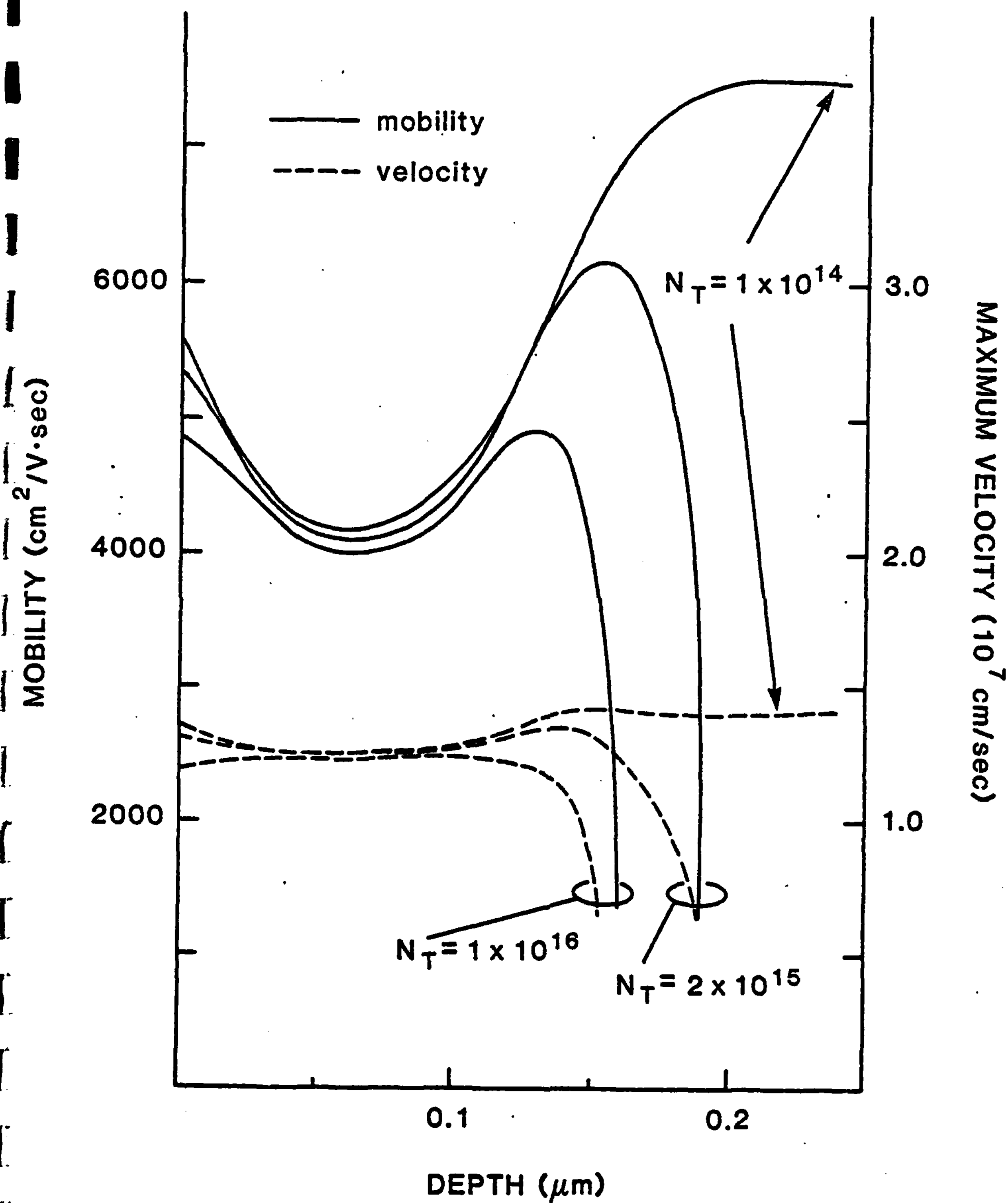
DENSITY (cm-3)
10^{17}
10^{16}
10^{15}
MOBILITY (cm^2/V. sec)
6000
5000
4000
3000
2000
1000
n(x)
$N_D(x)$
$N_T(x)$
0.1
0.2
0.3
DEPTH (μm)

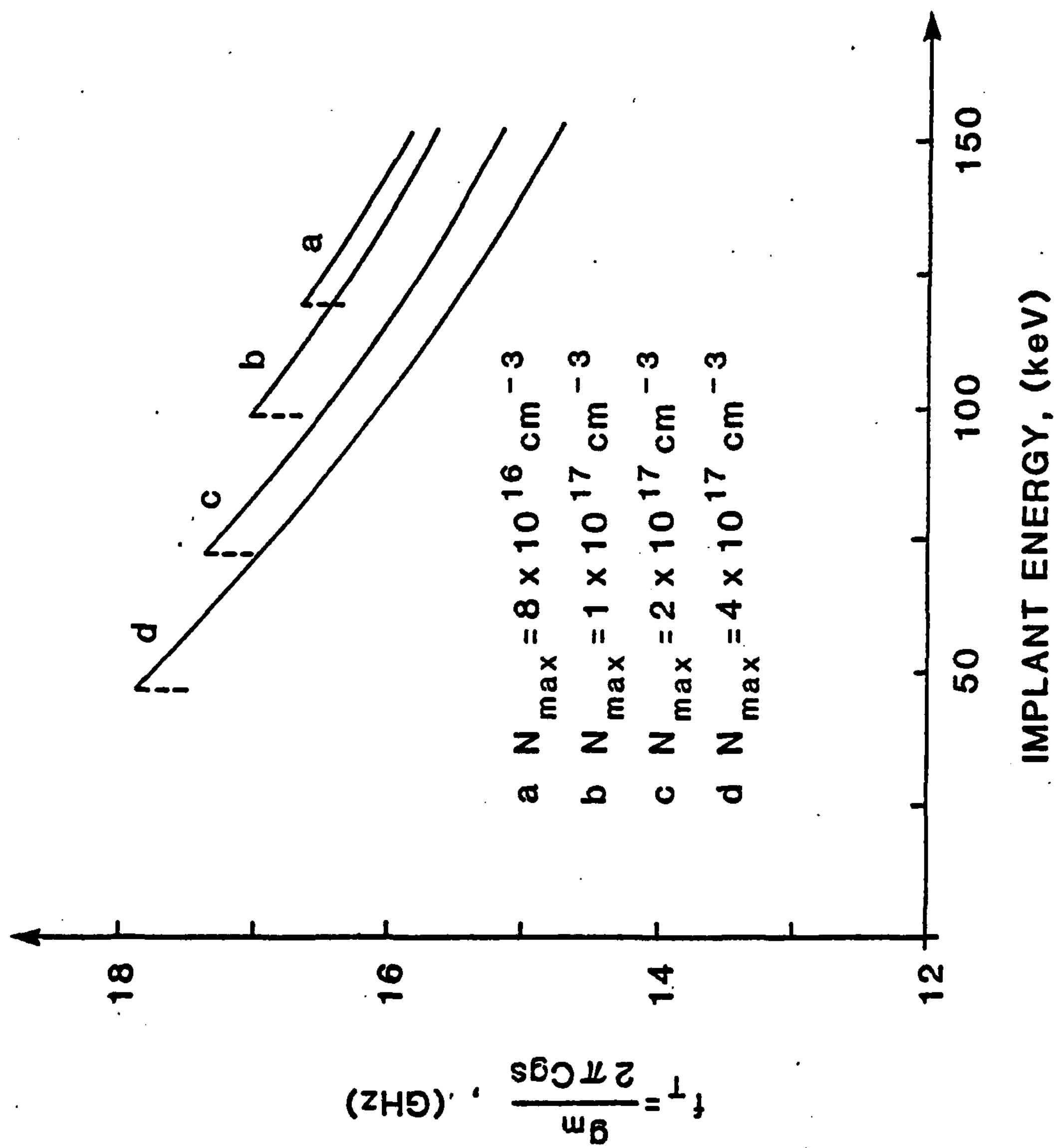


DRAIN CURRENT (mA)
10
8
6
4
2
DRAIN VOLTAGE (VOLTS)
1.0
2.0
3.0
4.0
0.50
0.25
$V_g = 0.00$
−0.25
−0.50
−0.75
−1.00

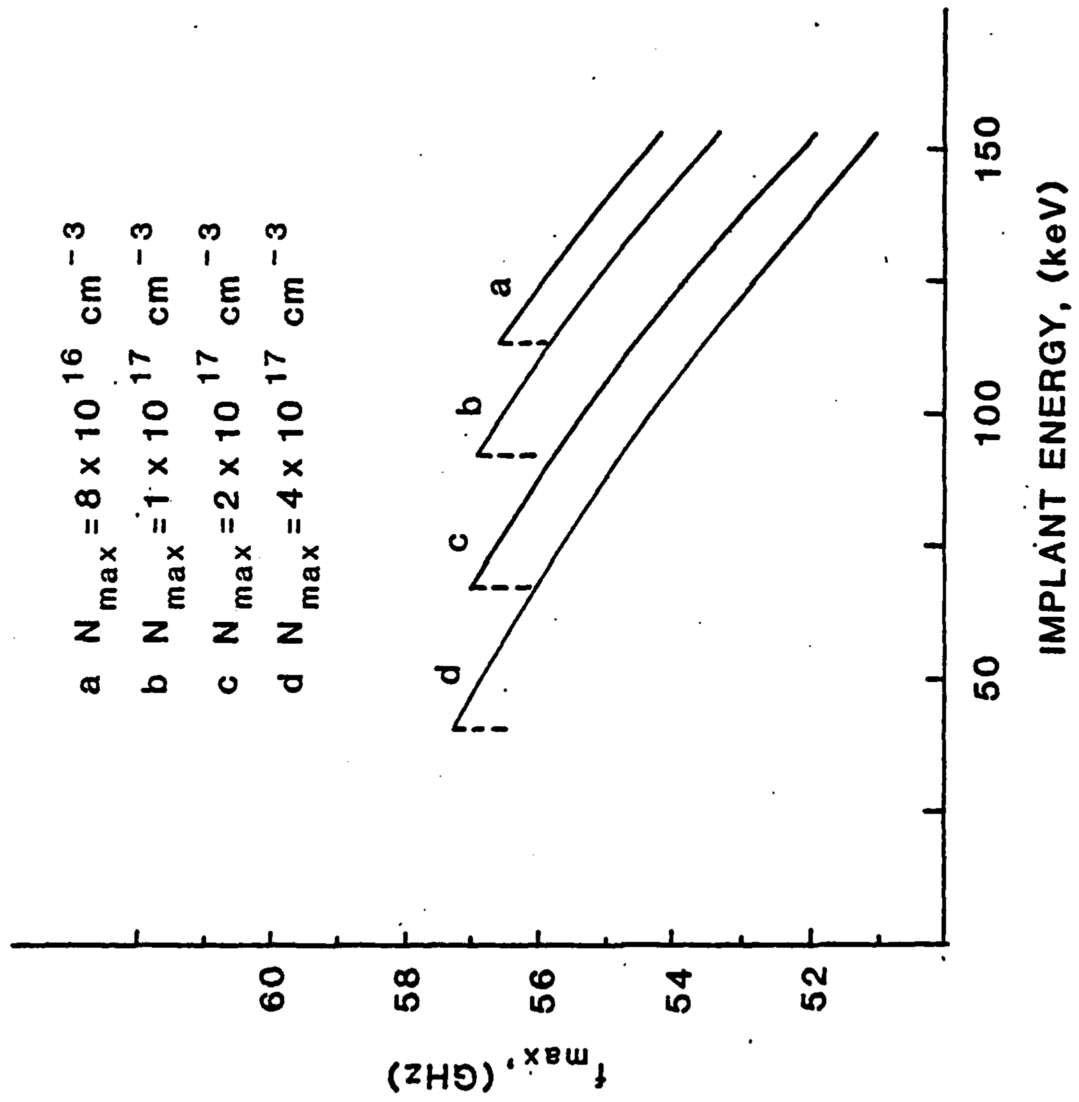


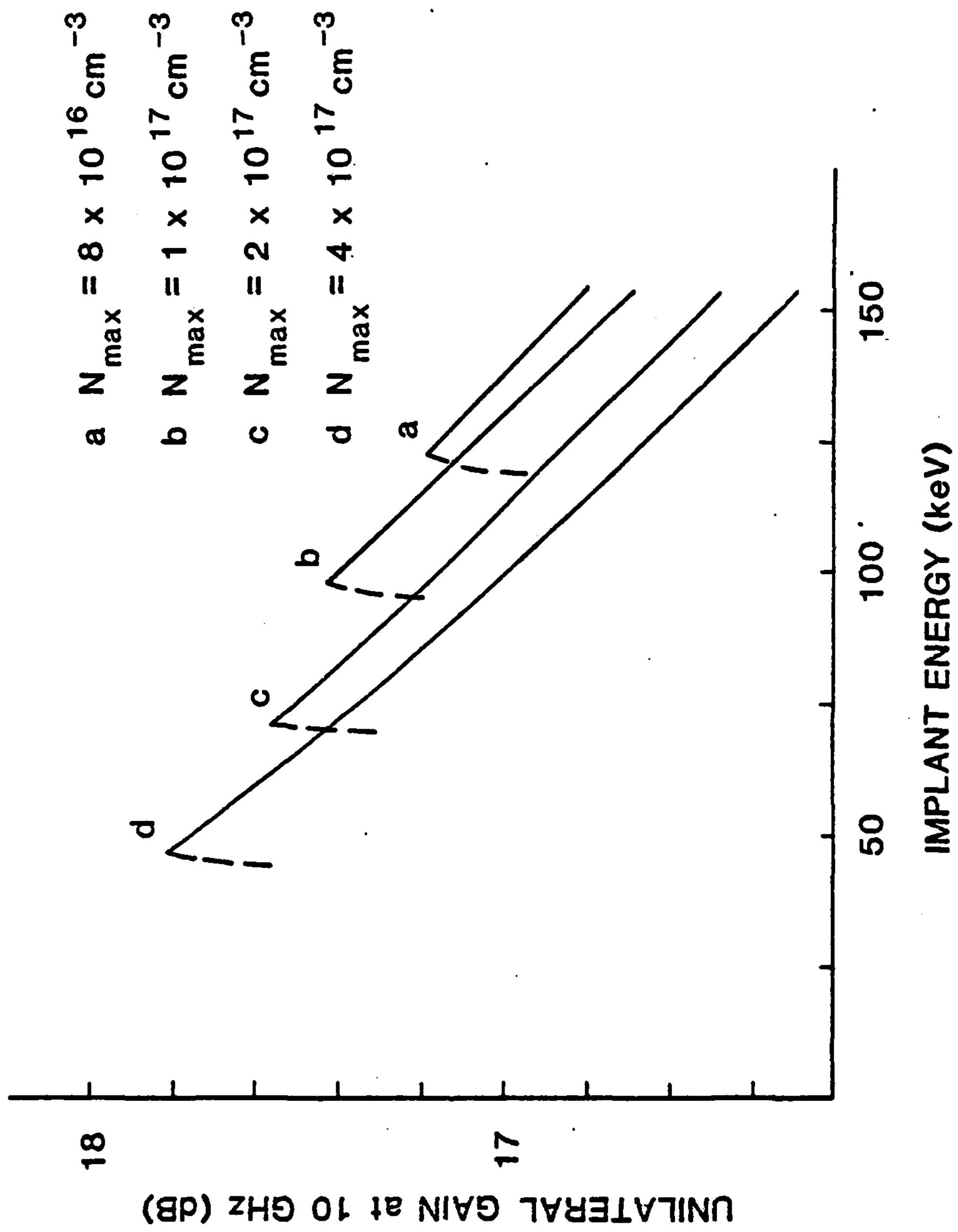
10^{17}
10^{16}
10^{15}
CONCENTRATION (cm^{-3})
0.1
0.2
0.3
DEPTH (μm)
1×10^{16}
5×10^{15}
1×10^{15}
deep acceptor concentration
no traps
1×10^{15}
5×10^{15}
1×10^{16}
deep donor concentration


mobility
velocity
6000
4000
2000
MOBILITY (cm²/V·sec)
3.0
2.0
1.0
MAXIMUM VELOCITY (10⁷ cm/sec)
N_T = 1 x 10^14
N_T = 1 x 10^16
N_T = 2 x 10^15
0.1
0.2
DEPTH (μm)

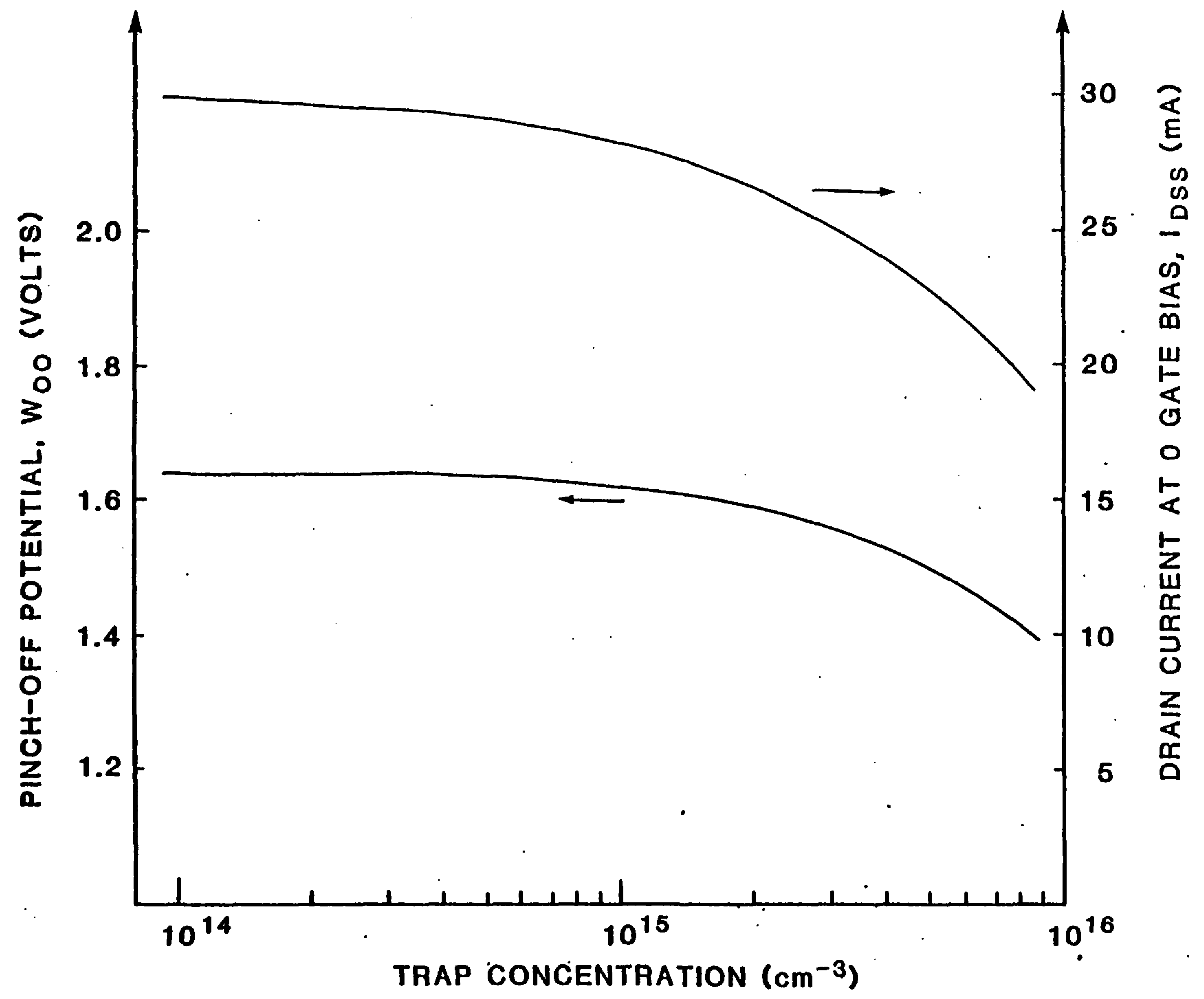


a
b
c
d
a $N_{max} = 8 \times 10^{16}$ cm^{-3}
b $N_{max} = 1 \times 10^{17}$ cm^{-3}
c $N_{max} = 2 \times 10^{17}$ cm^{-3}
d $N_{max} = 4 \times 10^{17}$ cm^{-3}
18
16
14
12
$f_T = \frac{g_m}{2\pi C_{gs}}$, (GHz)
50
100
150
IMPLANT ENERGY, (keV)

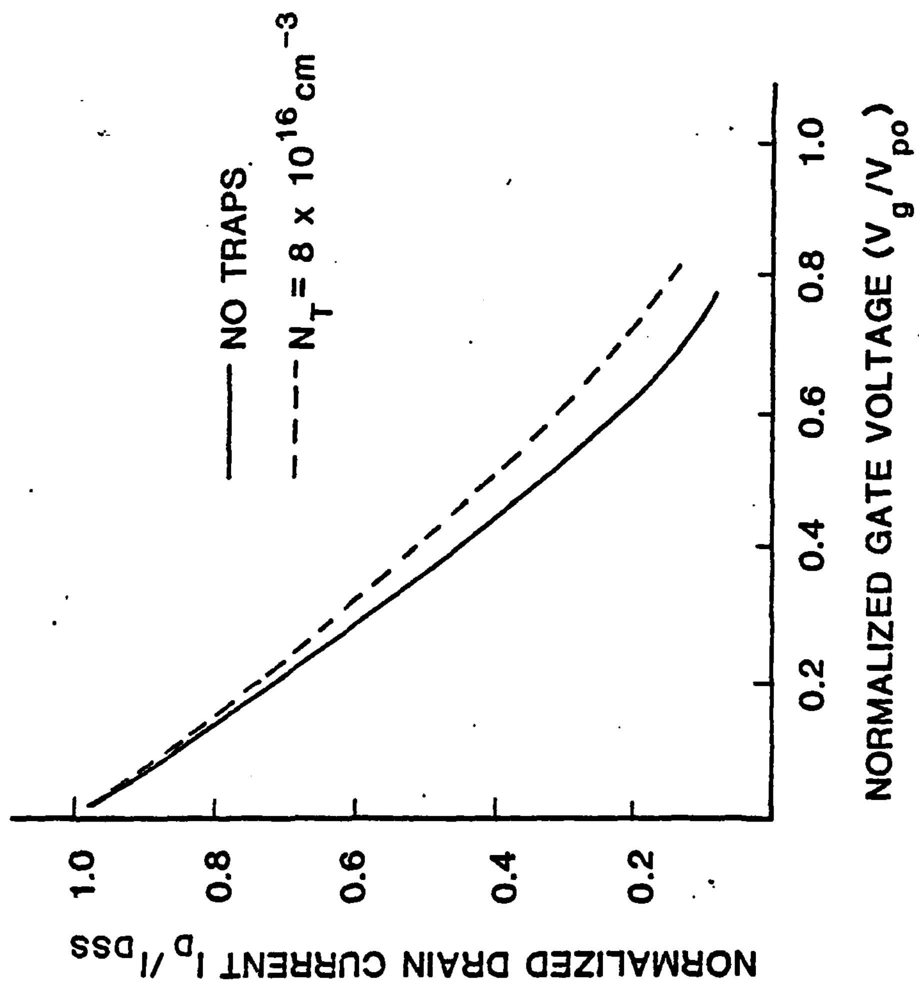

a $N_{max} = 8 \times 10^{16}$ cm^{-3}
b $N_{max} = 1 \times 10^{17}$ cm^{-3}
c $N_{max} = 2 \times 10^{17}$ cm^{-3}
d $N_{max} = 4 \times 10^{17}$ cm^{-3}
a
b
c
d
60
58
56
54
52
f_{max}, (GHz)
50
100
150
IMPLANT ENERGY, (keV)



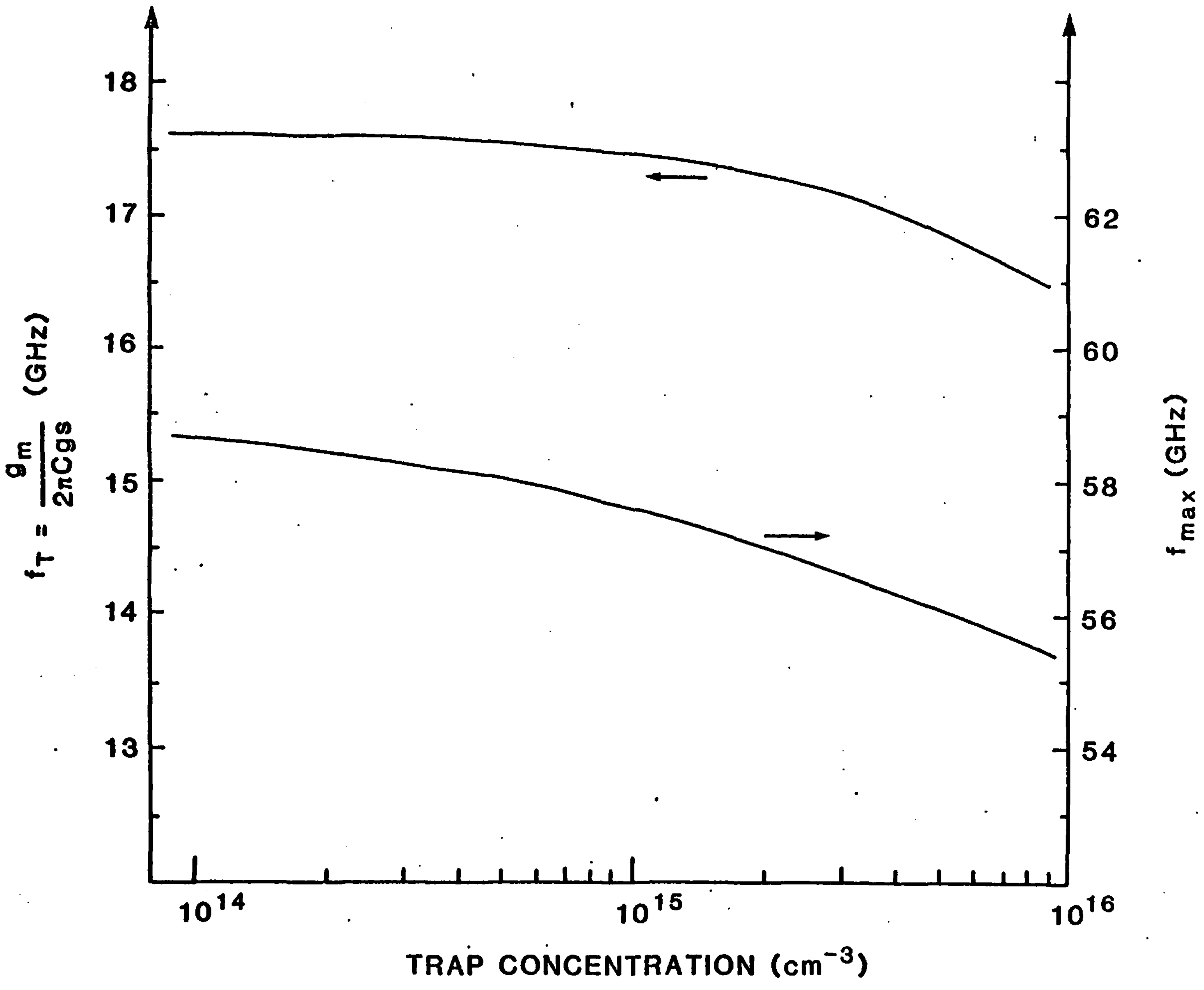
a $N_{max} = 8 \times 10^{16} cm^{-3}$
b $N_{max} = 1 \times 10^{17} cm^{-3}$
c $N_{max} = 2 \times 10^{17} cm^{-3}$
d $N_{max} = 4 \times 10^{17} cm^{-3}$
a
b
c
d
18
17
UNILATERAL GAIN at 10 GHz (dB)
50
100
150
IMPLANT ENERGY (keV)



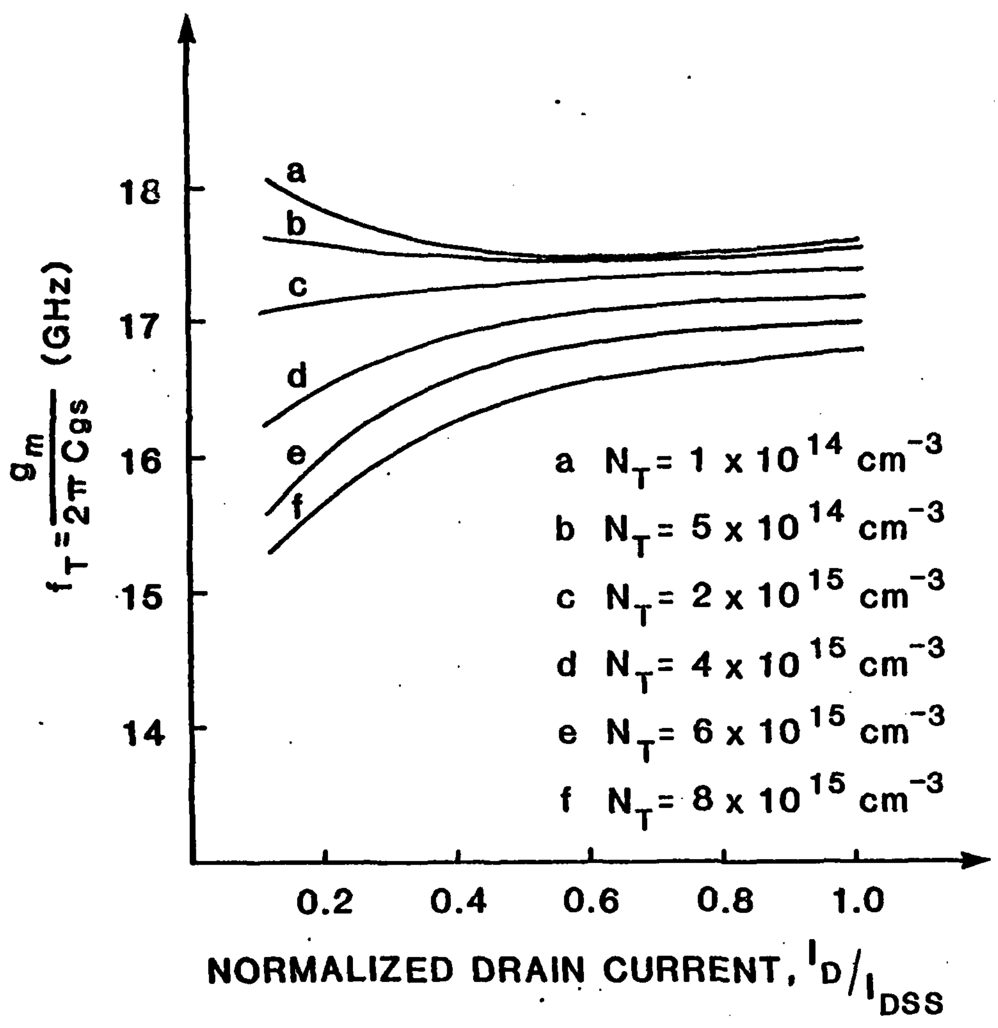
PINCH-OFF POTENTIAL, W_{OO} (VOLTS)
2.0
1.8
1.6
1.4
1.2
DRAIN CURRENT AT 0 GATE BIAS, I_{DSS} (mA)
30
25
20
15
10
5
10^{14}
10^{15}
10^{16}
TRAP CONCENTRATION (cm^{-3})



NO TRAPS
$N_T = 8 \times 10^{16} cm^{-3}$
1.0
0.8
0.6
0.4
0.2
NORMALIZED DRAIN CURRENT I_D/I_{DSS}
0.2
0.4
0.6
0.8
1.0
NORMALIZED GATE VOLTAGE (V_g/V_{po})



18
17
16
15
14
13
$f_T = \frac{g_m}{2\pi Cgs}$ (GHz)
62
60
58
56
54
f_{max} (GHz)
10^{14}
10^{15}
10^{16}
TRAP CONCENTRATION (cm^{-3})



18
17
16
15
14
$f_T = \frac{g_m}{2\pi C_{gs}}$ (GHz)
a
b
c
d
e
f
a $N_T = 1 \times 10^{14}$ cm^{-3}
b $N_T = 5 \times 10^{14}$ cm^{-3}
c $N_T = 2 \times 10^{15}$ cm^{-3}
d $N_T = 4 \times 10^{15}$ cm^{-3}
e $N_T = 6 \times 10^{15}$ cm^{-3}
f $N_T = 8 \times 10^{15}$ cm^{-3}
0.2
0.4
0.6
0.8
1.0
NORMALIZED DRAIN CURRENT, I_D/I_{DSS}

A TECHNIQUE FOR MODELING ION-IMPLANTED GaAs MESFETS IN THE PRESENCE OF DEEP LEVELS

J. M. Golio, G. N. Maracas, D. Johnson, R. J. Trew
and N. A. Masnari
North Carolina State University
Electrical and Computer Engineering Department
Raleigh, North Carolina 27650

INTRODUCTION

Recent interest in developing GaAs integrated circuits for both microwave [1] and high-speed logic [2] applications has stimulated the development of ion-implanted MESFETs. Obtaining performance predictions for ion-implanted FETs, however, presents several problems unique to these devices. Free-carrier and shallow-level donor concentrations will not be equivalent within the channel of an ion-implanted device, and both concentrations will vary as a function of channel depth. Deep-levels will also exist within the energy gap of the channel material. These levels will act to decrease the number of carriers available for conduction and also to degrade transport characteristics. In order to obtain accurate performance predictions, therefore, it is first necessary to quantitatively characterize each of these depth dependent material properties. In many cases traditional characterization techniques will not provide sufficient information for an accurate material characterization.

This paper presents a modeling technique for determining free-carrier, shallow-level donor, deep-level and low-field mobility profiles. The technique makes use of differential capacitance (C-V), conductance DLTS and channel mobility profile data. The effect of this more accurate modeling on performance prediction is also examined.

DIFFERENTIAL CAPACITANCE

Typical free-carrier, background donor, and deep-level profiles for a sample of ion-implanted semiconductor material is shown in Figure 1. Free-carrier diffusion from highly doped to more lowly doped regions in the material causes the free-carrier profile to differ from that of the shallow-level donor profile. This effect is most pronounced in shallow implants and can lead to as much as an order of magnitude difference between the two concentrations for implants typically used in the fabrication of GaAs MESFETs.

Traditional C-V analysis establishes the distribution of majority carriers rather than the distribution of ionized impurity atoms [3]. The actual impurity distribution in a measured sample can then be computed from the free-carrier distribution [4]. In the C-V measurement process, the capacitance is normally measured with a small oscillating voltage superimposed over a fixed applied bias. The fixed voltage bias translates

into a depletion length into the material through the use of the abrupt depletion approximation. The oscillating voltage induces a current due to an incremental charge being alternately covered and uncovered near the depletion region edge.

The presence of deep-levels in the material adds complications to the analysis. The traps allow the incremental charge which is measured to come not only from free-carriers in the conduction band, but also from carriers trapped in the deep-level sites. The interpretation of C-V data under these conditions has been examined in detail by Kimerling [5]. The analysis considers the relationship between the frequency of the oscillating voltage, the electron emission rate associated with the deep energy site, and the rate of change of the dc bias as well as the type of trap site present. Following Kimerling, expressions to accurately interpret C-V data and obtain the free-carrier distribution can be developed provided the dominant trap site can be accurately described [6,7]. The effect that traps have on the interpretation of C-V data is shown in Figure 2. The solid curve in the figure represents the computed free-carrier concentration using traditional C-V analysis and assuming no deep-levels are present in the material [3]. The dashed curves represent what the actual free-carrier distribution in the material would be for various constant deep-acceptor and deep-donor trap densities. In actual ion-implanted material the trap distribution will not be constant with depth so that more detailed analysis is necessary.

DEEP-LEVEL TRANSIENT SPECTROSCOPY

Conductance DLTS similar to that proposed by Adlerstein [8] has been utilized in this work. In the measurement process the source-drain conductance of an FET structure is monitored while a gate voltage pulse is applied repetitively. Band diagrams which correspond to times before, during and after the gate pulse are shown in Figure 3. A dc reverse bias voltage has the channel nearly pinched-off before the gate pulse is applied. The drain-source voltage is kept small to insure that the device remains in the linear region. Thus, a small steady-state conductance is measured. When the gate pulse is applied, it acts to decrease the depletion width and causes empty electron traps formerly in the depletion region to be filled (see Figure 3b). Immediately after the pulse, the depletion region is deeper than before the pulse since the filled traps carry the added negative charge of trapped electrons. This decrease in depletion width corresponds to a measured decrease in the source-drain conductance. Because the time constants of deep-levels are relatively long compared to capacitance time constants, the total change in conductance immediately after the pulse is not difficult to determine. The more traditional DLTS analysis which monitors the rate of decay of the trapped carrier charge as function of temperature is used only independently in this technique to determine the trapping state energy level. Finally, by using several gate pulses of different magnitudes, information about the density of the deep energy levels as a function of depth can be obtained.

It should be noted that calculation of conductance and change of conductance requires that low-field mobility and free-carrier distributions be known. For this work mobility was calculated using the theoretical results of Walukiewicz et al. [9] in conjunction with Monte Carlo [10] velocity-field simulations. The data obtained in this way was then curve fit to obtain an empirical expression for mobility as a function of ionized impurity density and compensation ratio. The resulting expression is given in reference [11] and plotted against normalized Walukiewicz values in Figure 4. The figure illustrates the excellent agreement between the two. A further check on the mobility calculation can be made by comparing the computed mobility with that obtained from a magnetotransconductance measurement [13].

MEASUREMENT APPARATUS

Figure 7 is a schematic diagram of the MCNC/NCSU electrical properties characterization laboratory. All measurements are controlled by an LSI 11/23 computer which stores the data and can transmit it to larger mainframe computers and remote users. This system will be described more completely at a later time.

I-V characteristics of devices are obtained with an HP4145A semiconductor parameter analyzer which is connected to an automatic probe station for on-chip measurements. 1 MHz C-V/GV data is extracted with a PAR 410 capacitance-voltage profiler. This is also used for capacitance and conductance DLTS measurements. Fast A/D converters digitize the DLTS transients and store them for later analysis [13]. The Air Products Helitran, which is capable of attaining liquid Helium temperatures (4.2°K) can be inserted between the poles of the laboratory electromagnet for experiments in magnetic fields such as mobility and magnetoresistance as a function of temperature. The cryostat also has quartz windows allowing optical excitation of the samples.

Since all measurements are completely automated, new experiments can be performed simply by writing specialized software routines. This increases the flexibility of the system by increasing the number of measurements possible.

PROFILE SOLUTION

Differential capacitance data allows for the calculation of free-carrier distribution if the deep-level distribution is known. Likewise, DLTS data allows for the calculation of deep-level distributions provided the free-carrier distribution is known. The combination of the two measurements when coupled with appropriate device equations provides sufficient information for determining the profiles of interest. References [6] and [7] outline a method for obtaining solutions to the set of highly non-linear integral and differential equations which must be solved simultaneously. The method involves assuming a deep-level distribution in the material and then

using the C-V data to compute the DLTS results. The actual DLTS measurement data can then be compared to the predictions for the assumed trap density profile. By modifying the assumed trap density profile good agreement between the change in conductance predicted and that which is measured can be obtained.

EXPERIMENTAL RESULTS

Measurements were performed on a 1 μm gate length MESFET and a fat FET (250 x 200 μm) adjacent to it on the same chip. The active channel was formed by implanting silicon into a Chromium doped GaAs substrate. Conductance DLTS and 1 MHz C-V measurements were performed on these devices and a dominant deep-level donor site was identified at 0.736 eV below the conduction band. This trap is probably (EL2). The findings of Martin et al. [12] also indicate that an (EL2) dominance is to be expected.

The measurement data was input into a computer simulation which calculates the desired profiles as discussed in references [6] and [7]. For a first guess at the deep-level distribution, constant density profiles were assumed. The solid lines of Figure 5 show the resulting conductance predictions for various trap densities along with measured data. Note that small values of V_a-V_p correspond to regions deep in the active channel while larger values represent areas close to the surface. Using simple step function approximations for the trap density profile results in considerable improvement in the obtained agreement.

Figure 6 illustrates free-carrier, ionized donor and deep-level concentrations which result from the analysis. Note that some scatter of the ionized donor data begins to occur deep in the channel. This begins to occur when the trap density and ionized donor density are of the same order of magnitude. The uncertainties in the exact shallow-level concentration at this depth are not critical to profile predictions. This is true since the magnitude of all the quantities of interest are small at this depth when compared to their magnitudes near the implant peak. Despite the scatter of the data, it is evident from Figure 6 that the free-carrier and shallow-donor concentrations differ significantly. For lower energy (shallow) implants, this distinction between the two profiles is even greater.

The low-field mobility profile obtained from this analysis is also shown in Figure 6. The curve can be compared to an experimentally obtained mobility and is in good agreement. The low field mobility profile in the channel is obtained experimentally by monitoring the magnetic field dependence of the 1.6 μm gate device transconductance [13].

EFFECT ON DEVICE PERFORMANCE

The effects which depth dependent concentrations and transport properties have on device performance have been studied through the use of a device model which is described in references [7] and [11]. The model is a

one-dimensional model with small-signal analysis which accounts for depth dependent carrier concentrations and transport properties.

The I-V predictions of the model for a 1.6 micron ion-implanted device are compared in Figure 8 with measured I-V curves. The agreement is excellent. It should be noted that without the inclusion of depth dependent transport due to traps, this agreement could not be obtained. The deep-levels have a tendency to "soften" the pinch-off characteristics of the device. For all of the devices studied in this work, this "softening" effect was required to obtain best agreement with measured I-V characteristics. This pinch-off softening effect is also illustrated in Figure 9 for one particular device. In addition to the qualitative effect of Figure 9, the inclusion of depth dependent transport properties also has considerable quantitative effect. Figure 10 shows the zero gate bias drain current and the pinch-off potential as a function of trapping state concentration. The trapping state density of the figure ranges between 10^{14} and 10^{16} cm^{-3}. Over this range the zero gate bias current varies between 30 and 18 mA, while the pinch-off potential varies between 1.62 and 1.38 volts.

CONCLUSION

A modeling technique for determining free-carrier, shallow-level donor, deep-level and mobility profiles of ion-implanted devices has been illustrated. Experimental results obtained from C-V, conductance DLTS and channel mobility profile measurements on a 1.6 μm device are shown and have been incorporated into the model. Agreement between the measured and calculated device parameters is extremely good indicating the importance of including basic material parameters into a device model.

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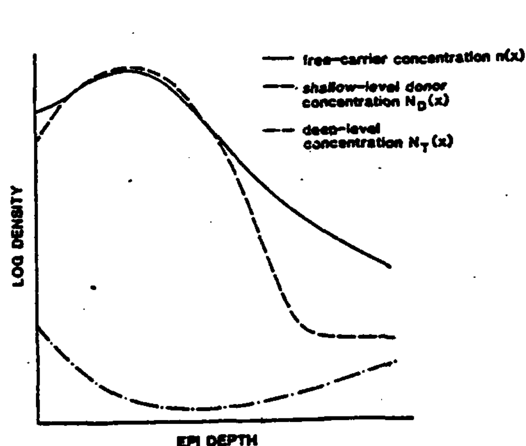

Figure 1. Typical concentration profiles for ion-implanted material. Shown are the free-carrier, shallow-level donor, and deep-level trapping state profiles.

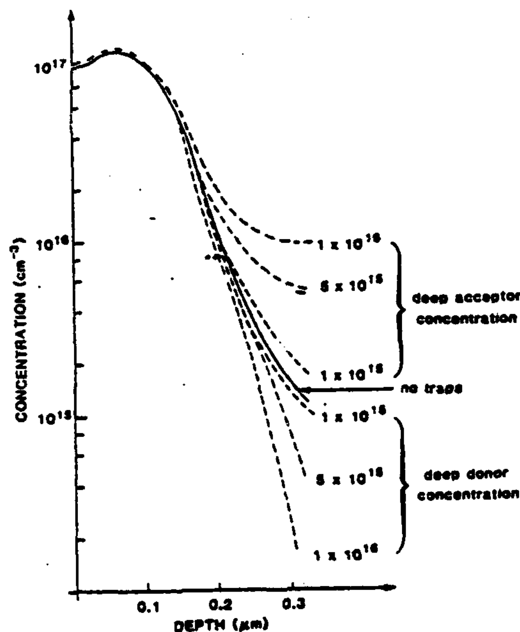

Figure 2. Effect of deep-levels on C-V interpretation. The solid line represents the computed free-carrier profile if no trapping states are present. The dashed curves are resulting profiles for various constant trap densities.

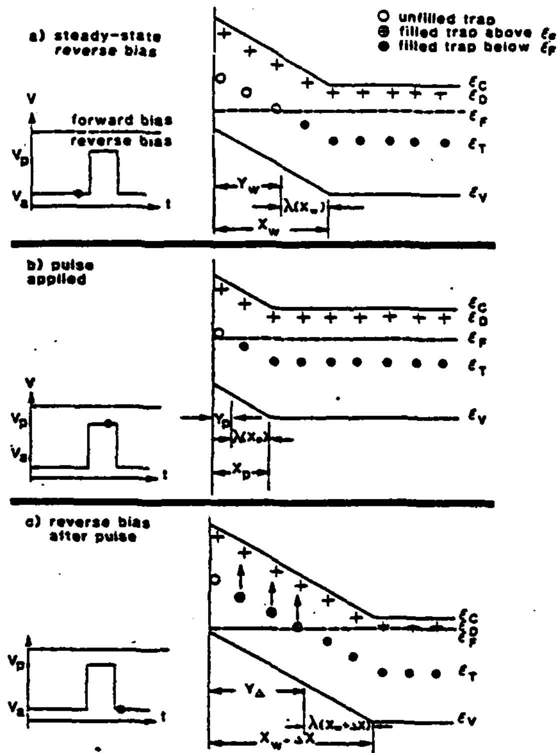

Figure 3. Band diagrams appropriate to conductance *DLTS* measurements. The figures correspond to times a) before the pulse is applied, b) during the pulse, and c) immediately after the pulse.

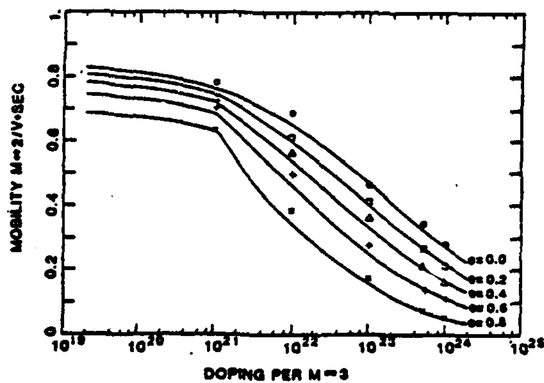

Figure 4. Low-field mobility as a function of doping and deep-level compensation. The solid lines are computed from an empirical expression for $\theta = 0.0$, 0.2, 0.4, 0.6, and 0.8. The data points are from normalized theoretical computations [9].

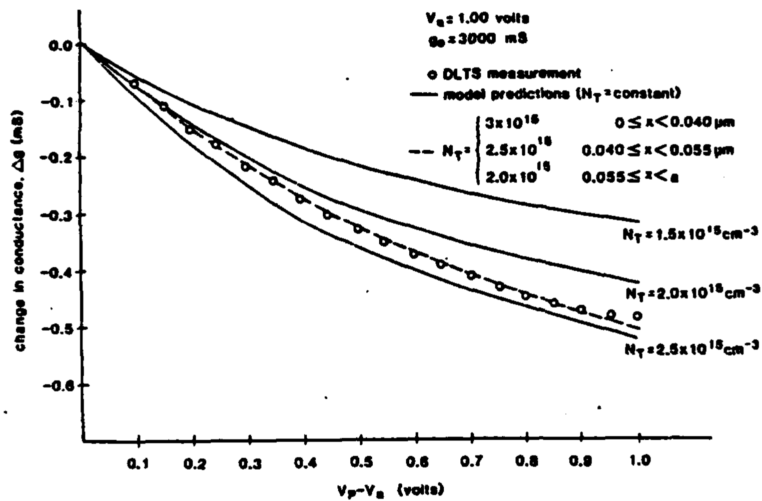

Figure 5. Change in conductance as a function of pulsed voltage. Data points are from conductance DLTS measurements. The solid lines are model predictions with N_T = constant. The dashed line is predicted for the three level step profile defined in the figure.

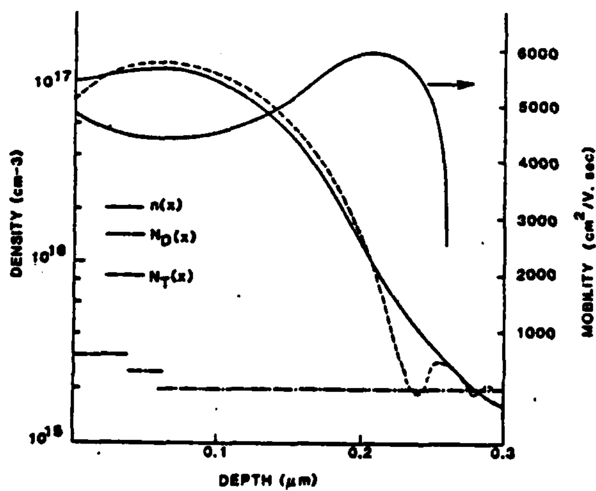

Figure 6. Resulting concentration profiles and low-field mobility profiles.

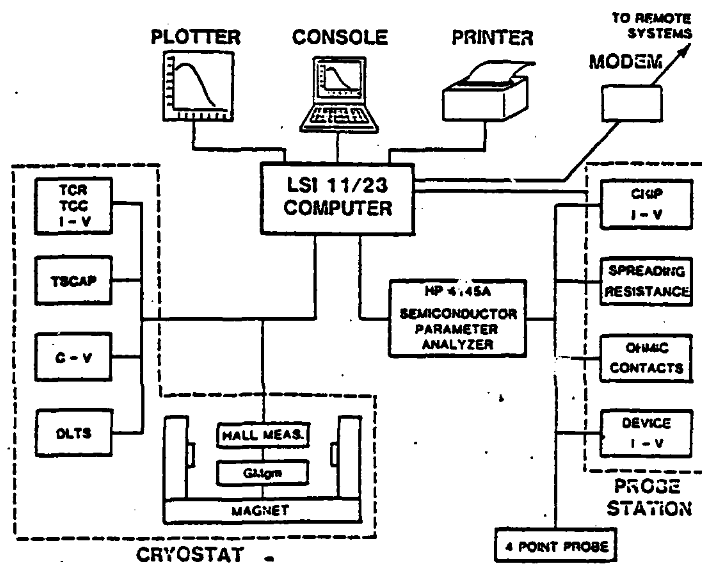

Figure 7. Measurement system.

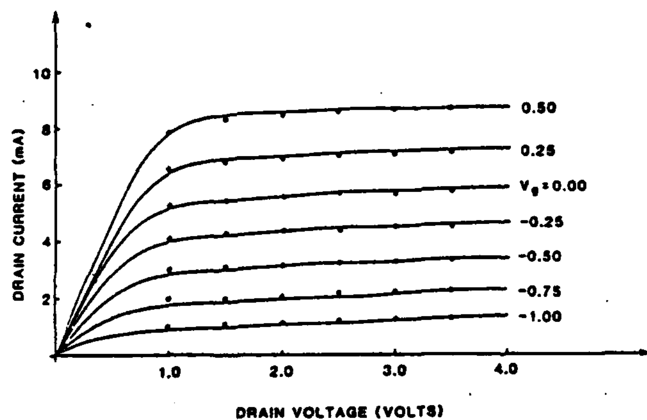

Figure 8. A comparison of model predicted and measured I-V characteristics for a 1.6 micron ion-implanted device. The lines are measured I-V curves. The data points are predicted by the model.

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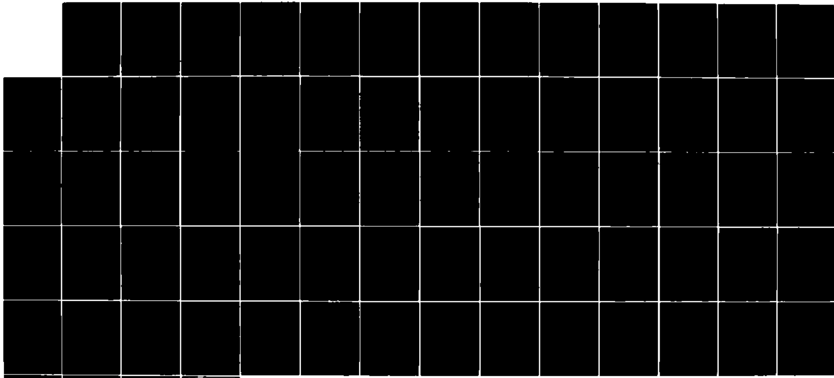

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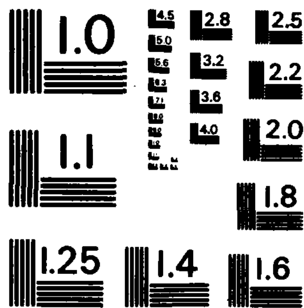

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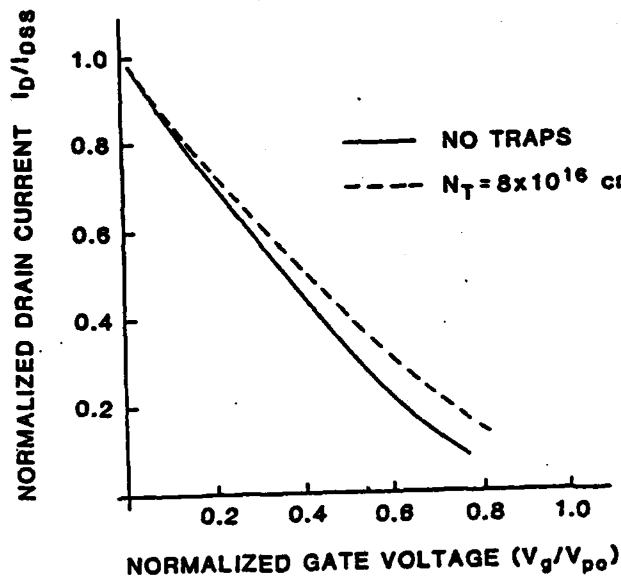

Figure 9. Normalized drain current vs. normalized gate bias with two different trapping state densities.

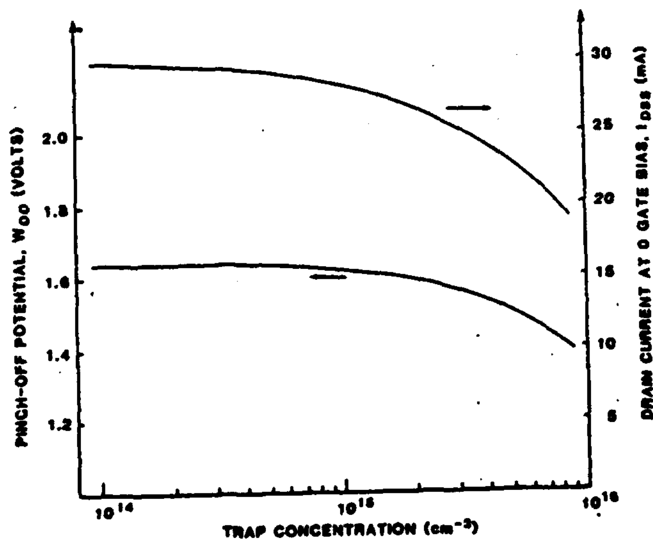

Figure 10. Zero gate bias drain current and pinch-off potential vs. trapping state concentration. The implant energy is 75 keV and the peak doping density is 2×10^{17} cm^{-3}.

A MODELING TECHNIQUE FOR CHARACTERIZING ION-IMPLANTED MATERIAL USING C-V AND DLTS DATA*

J. M. Golio, R. J. Trew, G. N. Maracas and H. Lefevre

Electrical Engineering Department
North Carolina State University
Raleigh, North Carolina 27650

ABSTRACT

A new modeling technique for determining free-carrier, shallow-level donor, trap and mobility profiles of ion-implanted GaAs MESFETs is presented. This technique uses the results of C-V and conductance DLTS measurements to calibrate a theoretical model. The model eliminates assumptions commonly made in other simple characterization techniques. A sample case is presented which indicates the importance of this more rigorous treatment.

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NOTATION

Symbol	Meaning
a	epi-layer thickness
D_n	electron diffusion coefficient
$_c$	conduction band energy
$_D$	shallow-level donor energy
$_F$	Fermi energy level
$_T$	deep-level trapping state energy level
$_v$	valance band energy level
E	Electric field
J_n	total electron current density
k	Boltzmann's constant
L	gate length
n	free-carrier concentration
N_C	conduction band density of states
N_D	ionized impurity concentration
N_T	deep-level trapping state concentration
q	electronic charge
T	temperature
x_w	depletion width
Δx	change in depletion width
y_w	Fermi level cross point of the trap level
Δy	change in the Fermi level cross point
Z	gate width
ε_r	dielectric constant of semiconductor
ε_o	permittivity of free-space
μ_o	low-field electron mobility
V_{BI}	built in potential of Schottky-barrier

1. INTRODUCTION

An attractive technology for the development of GaAs integrated circuits for microwave, millimeter-wave and high-speed logic applications involves ion-implantation of conductive regions directly into high-resistivity, bulk grown semiconductor substrates [1,2]. The performance of FETs fabricated in this manner depends strongly upon carrier concentration profiles and transport characteristics as a function of depth into the device active layer. The determination of these quantities, however, is complicated by the presence of impurity compensation in the form of deep-levels within the channel and by free carrier diffusion due to non-uniform impurity profiles.

Generally, C-V techniques that assume charge neutrality conditions throughout the undepleted semiconductor are utilized to analyze semiconductor profiles. Also, the effects of deep-levels are often neglected. These assumptions are generally not valid for the case of ion-implanted material typically used for GaAs MESFETs. When diffusion and compensation effects must be considered the transformation from bias dependent to depth dependent parameters is complicated. In general, it is not possible to accurately determine the various profiles of interest for non-uniformly doped semiconductors solely from C-V measurements.

In this paper we present a modeling and characterization technique for determining free carrier, shallow-level donor, deep-level and carrier mobility profiles. This technique is applicable for the analysis of material with arbitrary deep-level and doping profiles. This method combines experimental differential capacitance (C-V) and conductance deep-level transient spectroscopy (DLTS) measurements with a theoretical characterization model. The combination of the C-V and DLTS measurements allows the carrier mobility as a function of depth to be accurately determined in an indirect manner.

The profiles obtained with this method have been used in a theoretical MESFET device model to analyze the effects of various profiles upon device performance [3]. Excellent agreement between the theoretical and experimental device performance was obtained. Such agreement offers indirect evidence of the accuracy of the characterization technique.

2. GENERAL DEVICE EQUATIONS

Figure 1 shows typical free-carrier, background donor, and deep-level profiles for a sample of ion-implanted semiconductor material. Typically, peak doping ranges from about $9\times10^{16}cm^{-3}$ to $4\times10^{17}cm^{-3}$. The deep-level concentrations vary with material growth technology and generally range from low $10^{15}cm^{-3}$ to as high as $5\times10^{16}cm^{-3}$. Even in the absence of deep trapping centers, free-carrier diffusion from highly doped to more lowly doped regions will cause the free-carrier profile to differ from that of the ionized donors as shown in Figure 1. This effect, also known as Debye tailing, can be significant. Our studies show that as much as an order of magnitude difference can exist between these two profiles for ion-implanted materials typically used in the fabrication of GaAs MESFETs.

The relationship between the free-carrier, donor, and deep-level profiles can be obtained by combining the current density equation for electrons with Poisson's equation in the direction into the channel. The appropriate form for the one-dimensional current density equation in n-type material is

$$J_n = 0 = q\{\mu_o n(x)E(x) + D_n\frac{dn}{dx}\} . \quad (1)$$

To write the charge balance equation appropriate for bulk semiconductor material, the deep-level characteristics must be known. For the case where

deep-level acceptors act as the dominant electron trap in the semiconductor material, Poisson's equation is written as [4]

$$\frac{dE}{dx} = \frac{q}{\varepsilon_r \varepsilon_o} \{N_D(x) - n(x) - N_T(x)\}. \quad (2a)$$

When deep-level donors constitute the electron traps in the material, equation (2a) must be modified. In undepleted semiconductor material, deep-level donor states will normally lie below the Fermi level. Thus, they will be filled and carry no charge. The appropriate form of Poisson's equation for this case is [4]

$$\frac{dE}{dx} = \frac{q}{\varepsilon_r \varepsilon_o} \{N_D(x) - n(x)\}. \quad (2b)$$

Equation (1) and the appropriate form of equation (2) can be combined to express one of the profiles in terms of the other two. In the deep-acceptor trap case, the background donor concentration can be written as

$$N_D(x) = n(x) + N_T(x) - \frac{kT\varepsilon_r \varepsilon_o}{q^2} \frac{d}{dx}\left[\frac{1}{n(x)}\frac{dn}{dx}\right] \quad (3a)$$

where the Einstein relation has been used. Likewise, when the traps consist mainly of deep-donors, the shallow-level donor concentration can be written

$$N_D(x) = n(x) - \frac{kT\varepsilon_r \varepsilon_o}{q^2} \frac{d}{dx}\left[\frac{1}{n(x)}\frac{dn}{dx}\right]. \quad (3b)$$

The relationships (3a) and (3b) are identical to that derived by Kennedy and O'Brien [5] if trap centers were not present. The last term in both equations (3a) and (3b) represents the local charge imbalance that will, in general, exist within the material. The importance of this local steady-state charge imbalance in terms of the device measurements will be discussed in more detail in the following sections.

3. DIFFERENTIAL CAPACITANCE MEASUREMENT (C-V)

Using the depletion approximation, the differential capacitance (C-V) measurement can be considered as a parallel-plate capacitor problem. The capacitance, C, is normally measured with a small oscillating voltage, ΔV, superimposed over a fixed applied bias, V_a. The oscillating voltage induces a current due to an incremental charge, ΔQ, being alternately covered and uncovered near the depletion region edge, x_w. Kennedy et. al. [6] have shown that in the absence of deep states, traditional C-V analysis estimates the free-carrier concentration since only the free-carriers can participate in the differential change in the device charge ΔQ.

If deep trapping states are present, then the incremental charge, ΔQ, is due to free-carriers in the conduction band and electrons trapped in the deep-level sites. The interpretation of C-V data under these conditions is dependent on the relationship between the frequency of the oscillating voltage, $\omega(\Delta V)$, the electron emission rate associated with the deep energy site, e_n, and the rate of change of the dc bias, $\omega(\Delta V_a)$. Both deep-level donors and acceptors modulated at various speeds with respect to e_n have been examined by a number of workers [7-9]. For simplicity, however, this paper will examine only the case where

$$\omega(\Delta V) >> e_n >> \omega(\Delta V_a).$$

The band diagrams for this case are shown in Figure 2. These conditions are chosen since they would commonly hold for C-V measurements on bulk GaAs substrates ion-implanted with n-type dopants.

Kimmerling [9] has shown that when acceptor type traps make up the deep-levels the free-carrier concentration under the previously stated assumptions can be expressed as

$$n(x_w) = n_{C-V}(x_w) - N_T(y_w)\frac{y_w \Delta y}{x_w \Delta x} + N_T(x_w). \tag{4a}$$

For donor type traps the corresponding expression is

$$n(x_w) = n_{c-v}(x_w) - N_T(y_w)\frac{y_w \Delta y}{x_w \Delta x} . \tag{4b}$$

In equations (4a) and (4b), the term n_{c-v} is given by

$$n_{c-v}(x) = -\frac{C^3}{q\,\varepsilon_r\,\varepsilon_o}\left(\frac{dC}{dV}\right)^{-1} , \tag{5}$$

and represents the traditional C-V expression. The Fermi level cross-point y_w can be derived from the band bending if the background donor concentration is known. Referring to Figure 2a and applying Poisson's equation gives

$$\varepsilon_F - \varepsilon_T = \frac{q^2}{\varepsilon_r\,\varepsilon_o}\left[\overline{\overline{N_D(x_w)}} - \overline{\overline{N_D(y_w)}} - \lambda(x_w)\overline{N_D(x_w)}\right] \tag{6}$$

where the notation

$$\overline{N(a)} = \int_o^a N(x)dx$$

and

$$\overline{\overline{N(a)}} = \int_o^a \int_o^x N(z)dzdx$$

is adopted. Knowledge of the value $\varepsilon_F - \varepsilon_T$ is also required to determine y_w from equation (6). Normally, $\varepsilon_c - \varepsilon_T$ is determined through independent measurement [10,13] and the relation

$$\varepsilon_c - \varepsilon_F = kT\ell n(N_c/n(x)) \tag{7}$$

is then used with this information to determine $\varepsilon_F - \varepsilon_T$.

Equations (4a), (4b) and (6) can also be written in terms of the quantity $\lambda(x_w)$ through the relationship

$$\lambda(x_w) = x_w - y_w . \tag{8}$$

Differentiation of equation (8) with respect to x_w and substitution into equation (4a) results in the expression

$$n(x_w) = n_{C-V}(x_w) - N_T(y_w)\frac{y_w}{x_w}\left(1-\frac{d\lambda}{dx_w}\right) + N_T(x_w). \qquad (9a)$$

To obtain this expression small perturbations are assumed so that $\frac{\Delta y}{\Delta x} \approx \frac{dy}{dx}$. Likewise, equation (4b) becomes

$$n(x_w) = n_{C-V}(x_w) - N_T(y_w)\frac{y_w}{x_w}\left(1-\frac{d\lambda}{dx_w}\right). \qquad (9b)$$

Figure 3 shows a profile calculated from traditional C-V analysis along with corresponding free-carrier profiles calculated from equations (9a) and (9b) for various constant deep-level acceptor and donor trap densities. The deep levels have a significant effect upon the shape of the free carrier profile, especially near the tail of the implant. Since low noise devices are typically biased so that the conducting channel is in the tail region, the deep-level concentration is expected to have a significant influence upon device performance.

4. CONDUCTANCE DLTS

Capacitance deep-level transient spectroscopy (DLTS) was originally proposed by Lang [10] and described in various forms by others [11-12] as a technique to characterize traps in semiconductors. Similar information can also be obtained from conductance DLTS [13], and it is this method that has been utilized in this work. The technique involves monitoring the source-drain conductance of an FET structure while a repetitive gate voltage pulse is applied. The band diagrams corresponding to times before, during and after the gate pulse are illustrated in Figure 2. Before the pulse, a reverse bias V_a has the channel nearly pinched off so that only a small steady-state conductance, g_o, is measured. The pulse acts to decrease the depletion region

and causes empty electron traps formerly in the depletion zone to be filled (see Figure 2b). Immediately after the pulse, the depletion region is deeper than before the pulse since the filled traps carry the added negative charge due to the trapped electrons. This increase in depletion width—signified as Δx in Figure 2c—causes a decrease in the source-drain conductance, Δg. The non-equilibrium change in conductance decays as the filled traps emit electrons back into the conduction band. The decay process is very slow compared to gate capacitance time constants, however, so that Δg due to filled traps immediately after the pulse is not difficult to determine. This change in conductance from the steady-state value immediately after the pulse is of interest here. The actual rate of decay as a function of temperature which characterizes more traditional DLTS analysis [10-13], is used independently to determine the trapping state energy level. Finally, by using several gate pulses of different magnitudes, information about the deep energy levels as a function of depth can be obtained.

Under the steady-state condition of Figure 3a, the conductance g_o can be computed from

$$g_o = \frac{qZ}{L} \int_{x_w}^{a} \mu_o(x) n(x) dx. \tag{10}$$

Likewise, the change in conductance immediately after the pulse can be written from Figure 2c as

$$\Delta g = -\frac{qZ}{L} \int_{x_w}^{x_w+\Delta x} \mu_o(x) n(x) dx. \tag{11}$$

The conductance quantities expressed by equations (10) and (11) represent only the conductance beneath the gate. For short channel devices, the parasitic source and drain resistances will also contribute to the measured conductance. For this work, the parasitic resistances were determined and subtracted from the measured terminal conductance.

Equations (10) and (11) require that mobility be known as a function of donor density and background compensation. This information was obtained using the theoretical results of Walukiewicz et al. [14] in conjunction with Monte Carlo velocity-field predictions. The mobility as a function of background donor density with no traps present was determined from theoretical Monte Carlo calculations [15], and the Walukiewicz values were then normalized to the Monte Carlo numbers. The normalized data was used to obtain an empirical expression for mobility as a function of background donor density and compensation ratio. The resulting expression is

$$\mu_o = \frac{\mu_{max}}{1 + \left[\dfrac{\log N'_D}{N_o}\right]^c} (1-\Theta)^b \tag{12}$$

where

$N'_D = N_D \cdot m^3$,

$\mu_{max} = 8380$ (cm^2/V*sec),

$N_o = 23.2553$,

$c = 23.0$,

$\Theta = N_T/N_D$,

$$b = \begin{cases} 0.025*(\log N'_D)^2 - 0.817278*(\log N'_D) + 6.252838 & \text{for } N_D > 10^{21}\ (m^{-3}), \\ 0.114992 & \text{for } N_D < 10^{21}\ (m^{-3}), \end{cases}$$

and where N_D is given in (m^{-3}). Expression (12) is plotted against the normalized Walukiewicz values in Figure 4. As can be seen from the plot, the agreement is quite good.

Another restriction which applies to the situations illustrated in Figure 2 is that Poisson's equation must hold. As noted in section 2, a non-zero charge density exists within the channel independent of bias which gives rise to a potential gradient. This potential is not the quantity of interest for this analysis. Rather, it is the relationship of the change in applied potential to the depletion width which must be described. These quantities are related through the charge which can be moved—$n(x)$ and $N_T(x)$—and are therefore independent of $N_D(x)$. Thus, the appropriate form of Poisson's equation to describe Figure 2a is

$$V_a = \frac{q}{\varepsilon_r \varepsilon_o} \{\overline{\overline{n(x_w)}} - (\overline{\overline{N_T(x_w)}} - \overline{\overline{N_T(y_w)}}) - x_w\overline{n(x_w)} + \lambda(x_w)(\overline{N_T(x_w)} - \overline{N_T(y_w)})\} - V_{BI} \quad (13a)$$

for deep acceptors, and

$$V_a = \frac{q}{\varepsilon_r \varepsilon_o} \{\overline{\overline{n(x_w)}} + \overline{\overline{N_T(y_w)}} - x_w\overline{n(x_w)} - y_w\overline{N_T(y_w)}\} - V_{BI} \quad (13b)$$

for deep donors. The applicable equation for Figure 2b is obtained by changing V_a to V_p, x_w to x_p and $\lambda(x_w)$ to $\lambda(x_p)$ in the appropriate form of equation (13). Similarly, from Figure 2c for the case of deep acceptors

$$V_p = \frac{q}{\varepsilon_r \varepsilon_o} \{\overline{\overline{n(x_w+\Delta x)}} - (\overline{\overline{N_T(x_w+\Delta x)}} - \overline{\overline{N_T(y_p)}}) - (x_w+\Delta x)\overline{n(x_w+\Delta x)} + (x_w+\Delta x-y_p) \cdot (\overline{N_T(x_w+\Delta x)} - \overline{N_T(y_p)})\} - V_{BI}, \quad (14a)$$

while the case for deep donors is described by

$$V_p = \frac{q}{\varepsilon_r \varepsilon_o} \{\overline{\overline{n(x_w+\Delta x)}} - \overline{\overline{N_T(y_p)}} - (x_w+\Delta x)\overline{n(x_w+\Delta x)} - y_p\overline{N_T(y_p)}\} - V_{BI}. \quad (14b)$$

It can be noted from Figure 2 that only the trap sites within a distance of $x_w-\lambda(x_w)$ from the surface can alternately be filled and emptied by the pulse V_p. For the case studied here, this corresponds to a depth of about 0.1 micron. For distances into the device greater than this, the trap concentration enters into the computations through the free-carrier concentration as specified by equation (9), and through carrier mobility as expressed in equation (12).

5. METHOD OF SOLUTION

The differential capacitance data, conductance DLTS data, and measurement of the trapping state energy level when coupled with the equations of the preceding sections provide sufficient information for determining the profiles of interest. Certain problems exist, however, in utilizing the data and equations together.

Equation (10) requires that a value for the maximum epilayer depth be known. With ion-implanted profiles, however, this is a difficult quantity to determine. For the low-energy (70 - 140 keV) Si implants studied here, it was found that a good value for epi-thickness was on the order of 0.3 to 0.35 micron. This corresponds to a depth into the material where free-carrier density reaches a level a little more than two orders of magnitude below the peak free-carrier density in the structure.

The limitation of the C-V measurement technique to obtain data near the surface of the sample creates another difficulty in the analysis. Equations (3), (9), (13) and (14) all require knowledge of the free-carrier concentration throughout the active layer. This difficulty is overcome by requiring that equations (10) and (13) hold simultaneously. In fact, if the

C-V data were available throughout the active layer, then either equation (10) or (13) would be redundant and the problem would be overspecified. In collecting conductance DLTS data, both the reverse bias, V_a, and the steady-state conductance, g_o, are measured. Also, from C-V analysis and equation (4), a value for free-carrier concentration is obtained from some minimum obtainable depletion width, x_{min}, to the maximum epi-layer extent, a. For values of x between the material surface and x_{min}, the free-carrier profile can only be estimated. The initial estimate of the free-carrier concentration near the surface can be made by assuming that the profile should be approximately gaussian in this region with the slope of the profile flat at the surface. Once a profile has been established over the entire active region, equation (13) can be used to calculate the depletion width, x_w, corresponding to applied bias, V_a. Likewise, equation (10) can be used to compute x_w for a steady-state conductance, g_o. Any discrepancy between the two values for x_w obtained by these equations must be due to inaccuracies in the built-in potential used or in the free-carrier concentration estimate between the surface and x_{min}. Adjustments can then be made to either of these quantities until the two values for depletion width agree.

It should be noted that this method produces only an equivalent built-in potential/ free-carrier profile pair near the surface. However, since under normal device operation of an ion-implanted MESFET this region would always be depleted, this information is usually adequate.

To solve the equations of the preceding sections simultaneously in a rigorous fashion is difficult. Equations (11) and (14) must hold for each pulse used in the conductance DLTS measurement. Thus, if twenty different pulse heights were used, there would be over forty integral and differential equations that must be solved simultaneously.

An alternative to this method is to assume that the background trap profile is known, and to compute the resulting conductance DLTS data. The actual DLTS measurement data can then be compared to the predictions for the assumed trap profile. By making modifications on the assumed trap profile good agreement between the change in conductance predicted and that which is measured can be obtained.

This latter method was chosen for the work presented here. The system of equations was solved iteratively: each equation being solved individually to update only one quantity at a time. To begin, the trap concentration was assumed equal to some constant value throughout the device. The depletion width, x_w, corresponding to the steady-state bias, V_a, was determined using equations (10) and (13) as outlined above. Equation (3) was used to update the shallow-level donor profile. The function $\lambda(x_w)$ was then obtained from equation (6) and the free-carrier profile determined through the use of equation (9). Normally, three to six iterations through the equations were required before convergence was achieved.

Once the free-carrier and shallow-level donor profiles were determined, equation (14) was used to compute the depletion width change, Δx, as a function of pulse bias, V_p. This calculation requires the mobility to be determined as a function of depth through use of equation (12). This information is then easily utilized with equation (11) to predict conductance DLTS data. Finally, the results were compared to the DLTS data actually measured on the device. At this point, adjustments could be made to the trap profile originally assumed, and the process repeated until good agreement was obtained.

6. RESULTS

A 1.6 micron gate length MESFET and a differential capacitance test pattern were fabricated on a Silicon implanted GaAs substrate [16]. Conductance DLTS and C-V measurements were performed on these devices and a dominant deep-level donor state (electron trap) was identified at 0.736 eV below the conduction band. Although positive identification of this trap is difficult, the level is probably EL2 [17,18]. The dominance of this level agrees with the findings of Martin et. al. [19]. The C-V and DLTS data was used as input to a computer simulation which calculates the desired profiles as outlined in the preceding sections.

As a first guess, the trap concentration was assumed constant. The solid lines of Figure 5 give the resulting conductance DLTS predictions for various trap densities along with the measured data. Notice that small values of $V_a - V_p$ represent areas deep in the device while larger values represent areas close to the surface. The use of simple step function approximations for the trap profile results in improved agreement between the model and experimental results. A step-profile defined by

$$N_T = \begin{cases} 3.0\times10^{15}\ \text{cm}^{-3} & 0.0 < x < 0.040\ \text{micron} \\ 2.5\times10^{15}\ \text{cm}^{-3} & 0.04 < x < 0.055\ \text{micron} \\ 2.0\times10^{15}\ \text{cm}^{-3} & 0.055 < x < a \end{cases}$$

was used to obtain the results shown by the dashed line of Figure 5. Here the agreement between model predictions and measurements is excellent.

The resulting free-carrier, shallow-level donor, and deep-level trap concentrations as a function of depth into the material are shown in Figure 6. Notice that deep into the channel there is some scatter of the shallow-level donor data. This begins to occur when the trap concentration and the

shallow-level donor concentrations are of the same order of magnitude. The uncertainties in the exact shallow-level concentration at this depth into the channel are not critical to the profile predictions. This is true since the magnitude of all the quantities of interest are small at this depth when compared to their magnitudes near the implantation peak. Despite the scatter of the data, it is evident from Figure 6 that diffusion of the electrons has affected free-carrier and shallow-level donor concentrations. For lower energy (shallow) implants, this distinction between the two profiles is even greater.

The low-field mobility profile obtained from this analysis is also shown in Figure 6. It should be emphasized that the mobility versus depth profile is determined indirectly with the use of equation (12). Since this technique requires only the C-V and DLTS measurements it allows the various profiles to be determined in an efficient manner.

The mobility profile shown in Figure 6 is in good agreement with the results presented by Das and Kim [20], Hobgood et al. [21] and Jay and Wallis [22]. In addition, this technique has been used to determine profiles for use in a theoretical device model to study the effects of the various profiles upon device performance [3]. Excellent agreement between the theoretical predictions and experimental device performance was obtained [3].

From Figure 4 it should be noted that when the deep-level density is less than about $10^{15}cm^{-3}$, the C-V data can be interpreted in the traditional manner and the $N_T(x)$ terms in the equations can be neglected. Under these special conditions n(x) is also known and the entire analysis is simplfied. Even for this special case, however, the shallow-level donor and free electron concentrations must be treated as separate functions in order to accurately determine the carrier mobility profile.

7. CONCLUSIONS

A modeling technique for determining the free-carrier, shallow-level donor, deep-level and mobility profiles of ion-implanted GaAs material suitable for MESFET fabrication has been presented. The technique involves non-destructive electrical C-V and conductance DLTS measurements coupled with the solution of the applicable device equations. The appropriate equations have been developed and a solution method presented. Parameter profiles as a function of depth suitable for device characterization and modeling are easily determined. Deep-levels and free-carrier diffusion are shown to have significant effects upon free-carrier transport characteristics. The use of this technique on a sample case has been presented.

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Figure 1 Typical concentration profiles for ion-implanted material. Shown are the free-carrier, shallow-level donor, and deep-level trapping state profiles. The distinction between free-carrier and shallow-level donor concentrations will exist even without the presence of deep-levels.

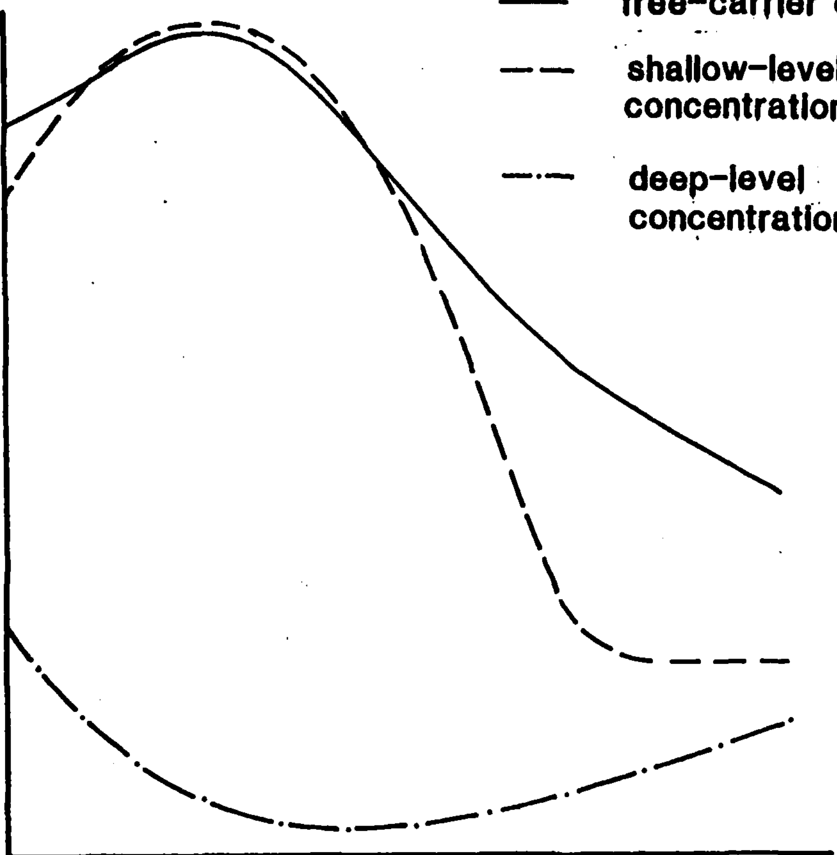
Figure 2 Band diagrams appropriate to conductance DLTS measurements. The figures correspond to times a) before the pulse is applied, b) during the pulse, and c) immediately after the pulse.

Figure 3 Effect of deep-levels on C-V interpretation. The solid line represents the computed free-carrier profile if no trapping states are present. The dashed curves are resulting profiles for various constant trap densities.

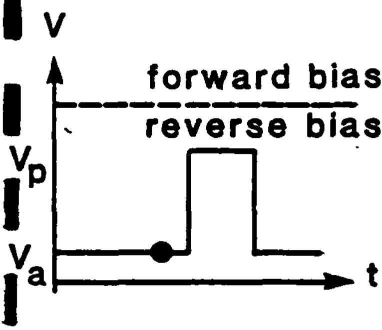
Figure 4 Low-field mobility as a function of doping and deep-level compensation. The solid lines are computed from equation (12) for $\Theta = 0.0, 0.2, 0.4, 0.6$, and 0.8. The data points are from normalized theoretical computations [14].

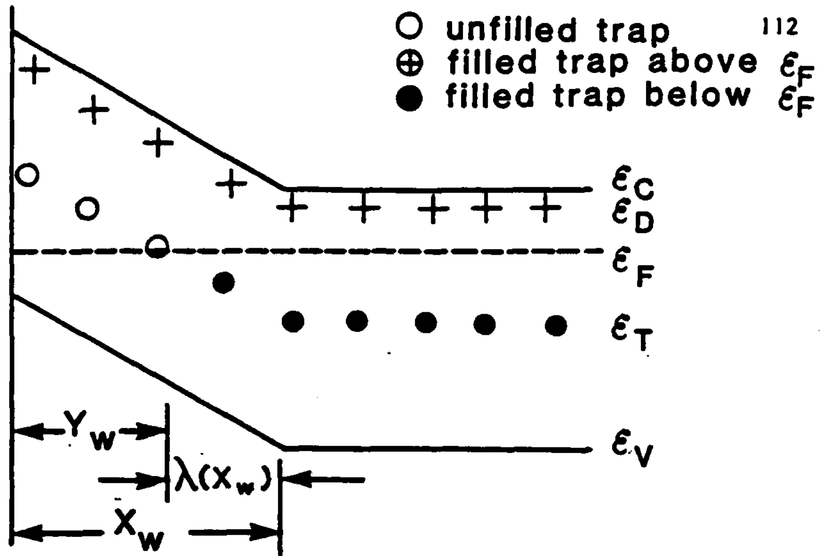
Figure 5 Change in conductance as a function of pulsed voltage. Data points are from conductance DLTS measurements. The solid lines are model predictions with N_T = constant. The dashed line is predicted for the three level step profile defined in the figure.

Figure 6 Resulting concentration profiles and low-field mobility profiles.

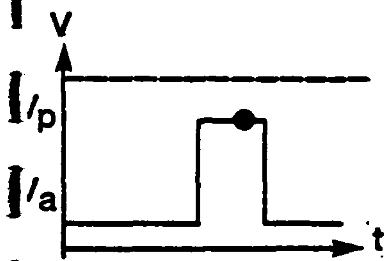

free-carrier concentration n(x)
shallow-level donor concentration $N_D(x)$
deep-level concentration $N_T(x)$
LOG DENSITY
EPI DEPTH

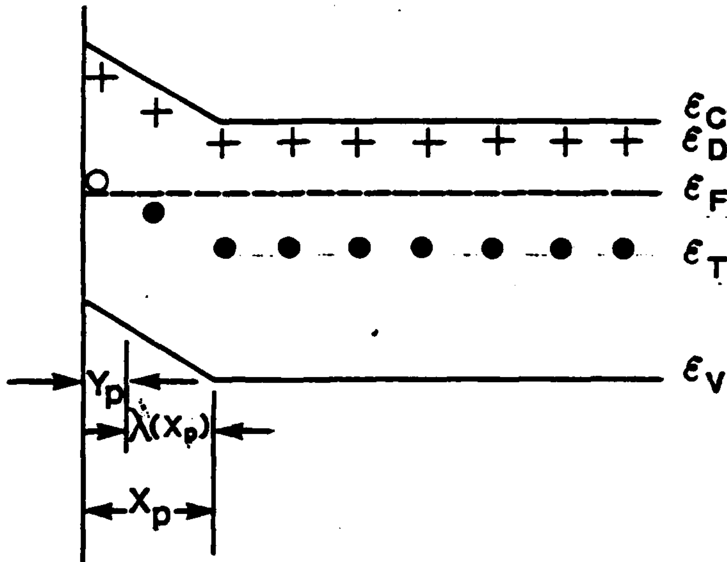
a) steady-state reverse bias



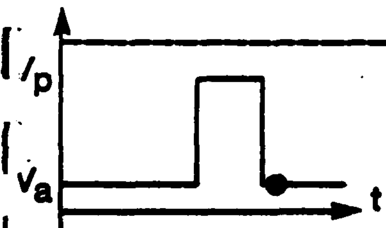


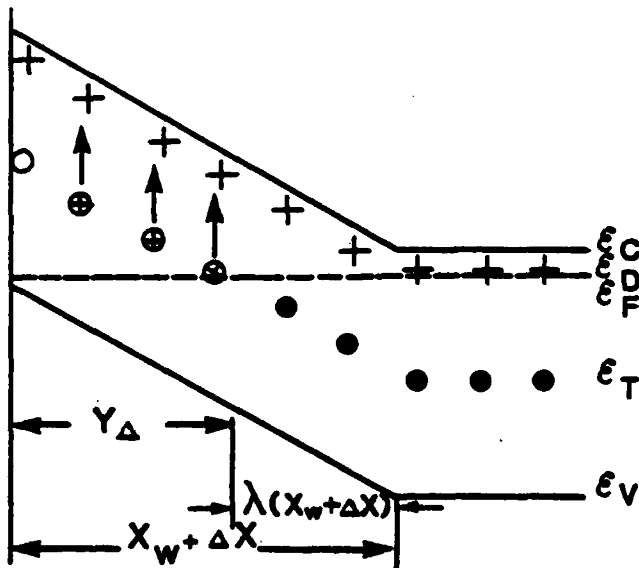
b) pulse applied

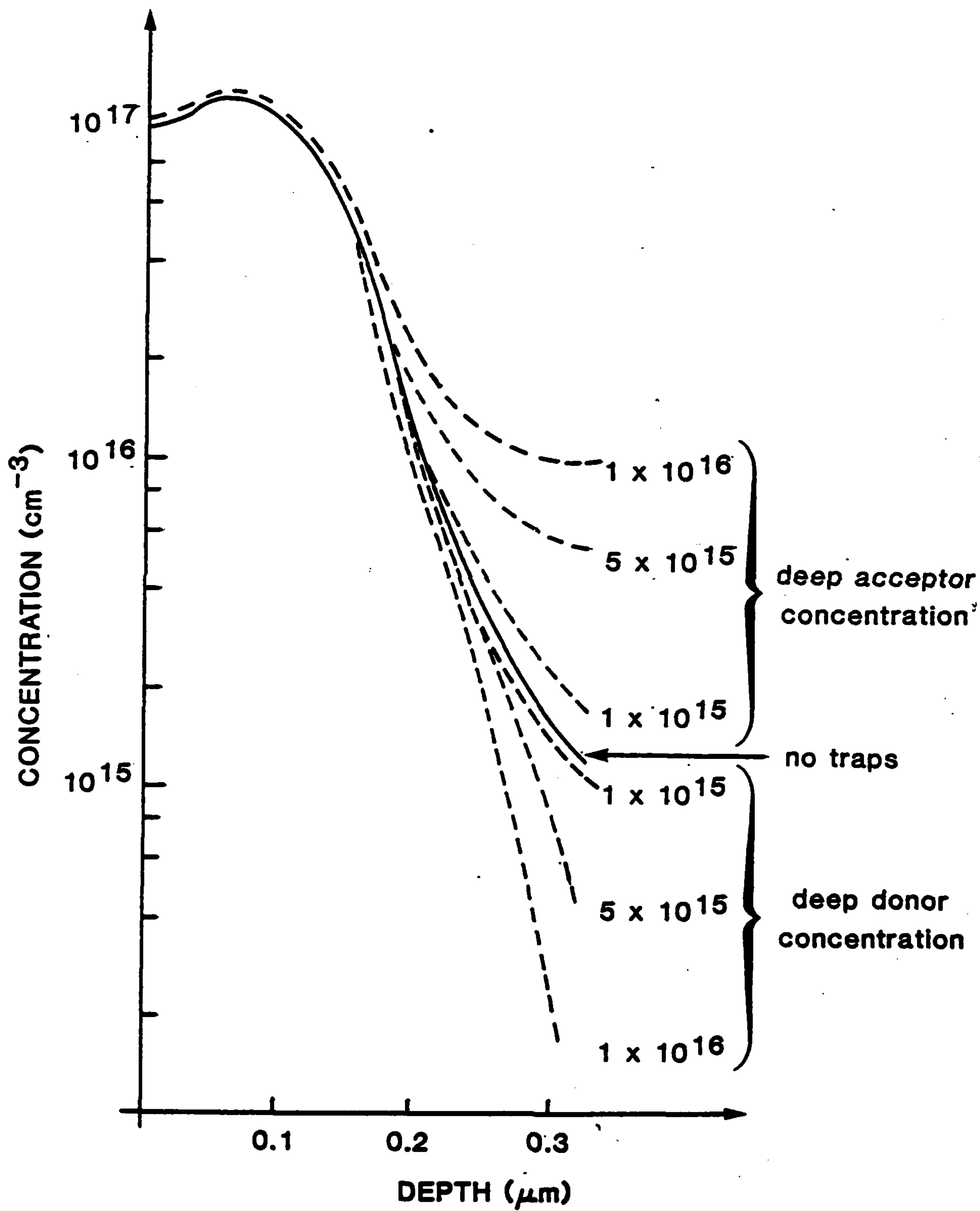




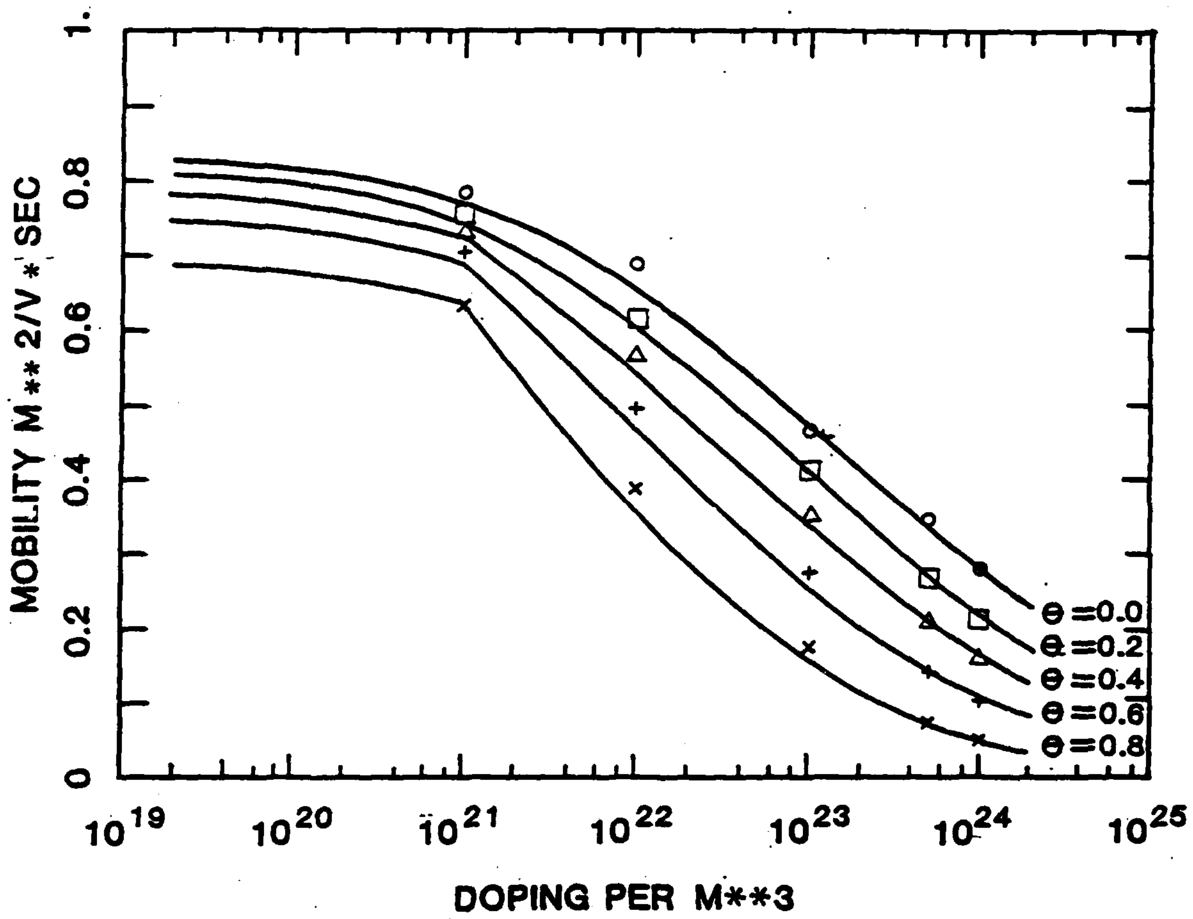
c) reverse bias after pulse

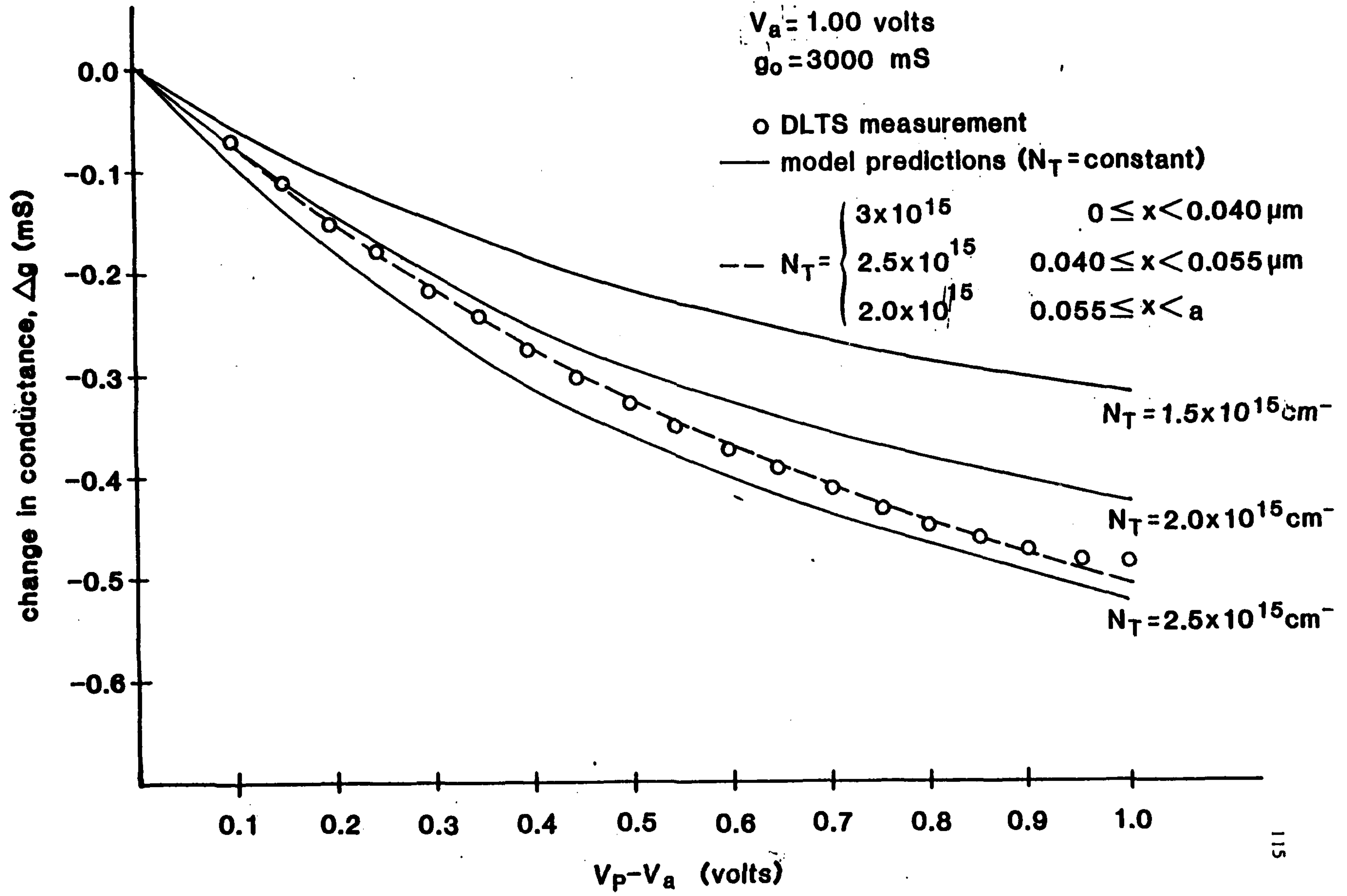




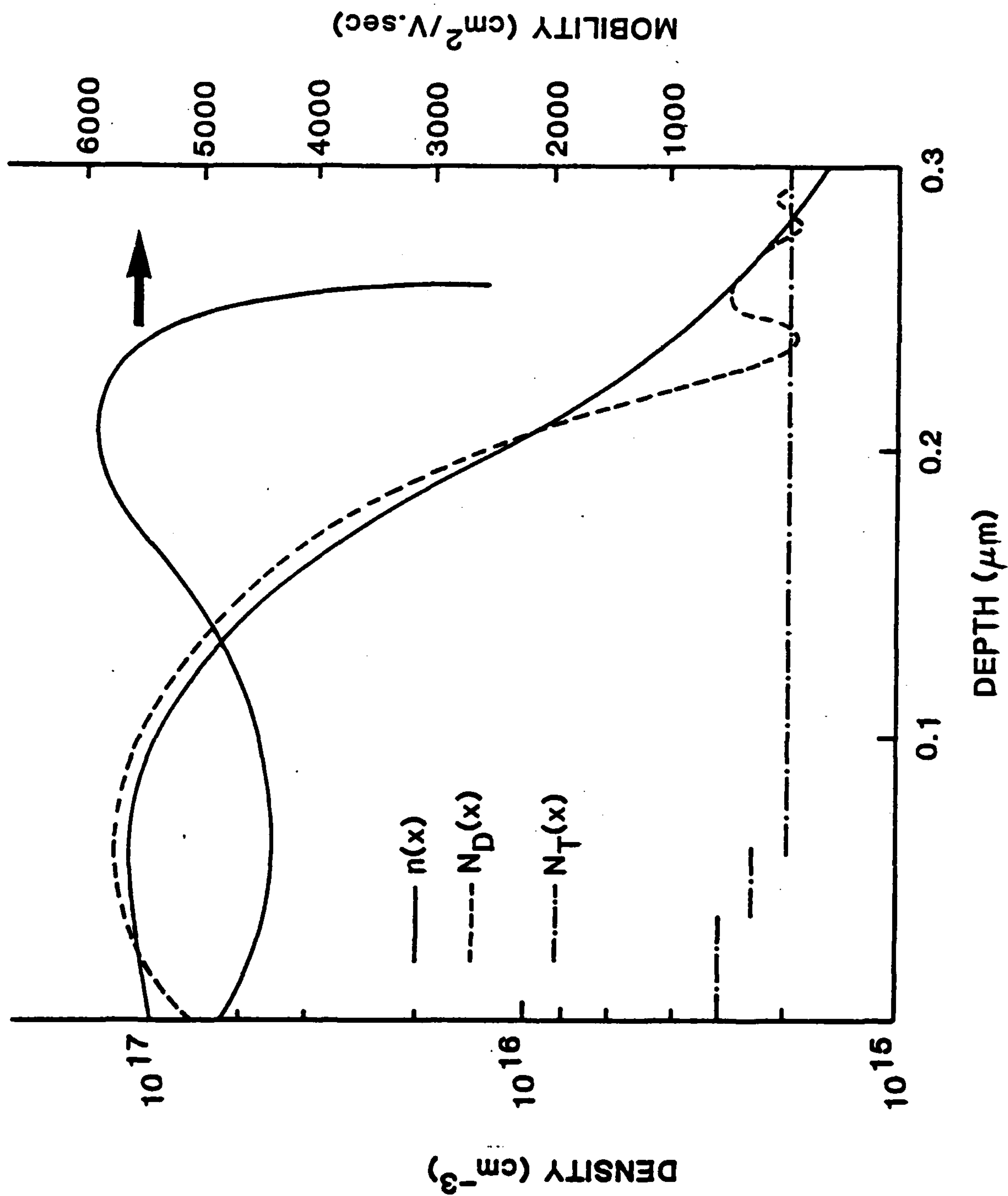


CONCENTRATION (cm^{-3})
10^{17}
10^{16}
10^{15}
0.1
0.2
0.3
DEPTH (μm)
1 x 10^{16}
5 x 10^{15}
1 x 10^{15}
deep acceptor concentration
no traps
1 x 10^{15}
5 x 10^{15}
1 x 10^{16}
deep donor concentration


MOBILITY M ** 2/V * SEC
0
0.2
0.4
0.6
0.8
1.
10^{19}
10^{20}
10^{21}
10^{22}
10^{23}
10^{24}
10^{25}
DOPING PER M**3
Θ =0.0
Θ =0.2
Θ =0.4
Θ =0.6
Θ =0.8



Va = 1.00 volts
go = 3000 mS
o DLTS measurement
— model predictions (NT = constant)
— — NT = 3x10^15 0 ≤ x < 0.040 μm
2.5x10^15 0.040 ≤ x < 0.055 μm
2.0x10^15 0.055 ≤ x < a
NT = 1.5x10^15 cm⁻
NT = 2.0x10^15 cm⁻
NT = 2.5x10^15 cm⁻
change in conductance, Δg (mS)
0.0
-0.1
-0.2
-0.3
-0.4
-0.5
-0.6
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
VP-Va (volts)


MOBILITY (cm²/V.sec)
6000
5000
4000
3000
2000
1000
DENSITY (cm⁻³)
10¹⁷
10¹⁶
10¹⁵
DEPTH (μm)
0.1
0.2
0.3
n(x)
N_D(x)
N_T(x)

A New Method of Tolerance Enhancement for Filters and Amplifier Matching Networks*

A. N. Riddle and R. J. Trew
Department of Electrical and Computer Engineering
North Carolina State University
Raleigh, NC 27650
(919) 737-2336

Abstract

A new method for increasing the tolerance of passive networks to complex load variations is presented. The method is based upon utilization of the angular relationship between a network's reflection coefficient and the corresponding changes with component variations. A new filter polynomial that produces a response which has a greater tolerance to loss, component variations and load reactance variations than Butterworth, Chebyshev or Elliptic structures has been developed using this method. Examples using this new filter for tolerance enhancement of matching filters and FET feedback amplifiers are presented.

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Introduction

One method for the development of low-cost microwave integrated circuits involves the design of passive networks that are tolerant of component and load impedance variations. Such networks when used, for example, in amplifier circuits would produce essentially uniform terminal characteristics while allowing for typical device-to-device parameter variations. While this technique has considerable potential for use in designing low cost MICs, very little work has been reported on appropriate design procedures. A new method for determining suitable matching networks is presented in this paper. In particular, a solution to the approximation problem for deriving filters with greater tolerances to load parasitics, loss and element tolerances is presented. A polynomial is developed for synthesizing a network with less sensitivity to parameter variations than Butterworth, Chebyshev or Elliptic structures. Examples of circuits utilizing this new filter polynomial are presented and compared with conventional filter designs. The method presented in this paper is intended to be used with the synthesis procedures discussed elsewhere [1,2]. Only lumped element prototypes are considered so that the effects of the filtering function, rather than a particular realization method, may be studied.

The first detailed consideration of ideal responses for matching filters was presented by Fano [3]. Although Fano demonstrated that a low ripple Chebyshev response approximating a constant mismatch was superior to a large ripple Chebyshev response with the same peak mismatch, he did not explore filter responses other than Butterworth, Chebyshev and Elliptic types. The filter polynomial developed in this paper results in a response which maximizes the tolerance of the filter to load reactance variations such as in the input capacity of an FET. This response is derived by realizing that the

tolerance of a filter to an element variation is maximized when that variation causes a change in $S_{11}(f)$ which is perpendicular to the direction of $S_{11}(f)$ [4]. Therefore, a filtering polynomial is developed which causes the change in $S_{11}(f)$ with load reactance variations to be perpendicular to the direction of $S_{11}(f)$ at the peaks of $S_{11}(f)$. When the angle factor (defined as the angle between the direction of $S_{11}(f)$ and the change in $S_{11}(f)$ due to a variation in any component) is an odd multiple of 90 degrees the response is maximally tolerant to variations in that component [4]. Consideration of the angle factor leads to a filter response which has a relatively flat mismatch over most of the band and a small dip in $S_{11}(f)$ at the band edge. Such a characteristic has improved performance over traditional filters.

Theory

The transformation from the load imittance plane to the input reflection coefficient plane and the reverse process are both bilinear transformations. Therefore, since changes in the real and imaginary parts of the load are orthogonal, resulting changes in the input reflection coefficient will be orthogonal. This property can be exploited to increase the tolerance of filter networks to reactive variations in the load. If the filter network is characterized with an ABCD matrix and a load impedance of the form

$$Z_L(f) = R + j\,X(f)$$

is assumed, the change in a reflection coefficient due to load reactance variations can be written as

$$\frac{\partial S_{11}(f)}{\partial X(f)} = j\,\frac{S_{21}(f)S_{12}(f)}{2\,Z_L(f)}. \qquad (1)$$

If the load is described as an admittance the corresponding equation is

$$\frac{\partial S_{11}(f)}{\partial B(f)} = -j\,\frac{S_{21}(f)S_{12}(f)}{2Y_L(f)}, \qquad (2)$$

where $Y_L(f) = G + jB(f)$.

Since equations (1) and (2) define a derivative from only one circuit evaluation, they provide efficient tolerance analysis.

Figure 1 shows the center of the reflection coefficient plane with a circle enscribing a maximum tolerable reflection, Γ_{max}, for a circuit such as an amplifier input matching network. A point, $S_{11}(f_o)$, is located inside this circle and represents a point on the curve of input reflection versus frequency. Increases and decreases in the device reactance, typically the input capacitance, will move the point at $S_{11}(f_o)$. This differential movement is given exactly by equation (1) for any network described by S-parameters with load impedance Z_L.

The alternating line of Figure 1 shows the maximum symmetric tolerance about the point at $S_{11}(f_o)$. The dashed line of Figure 1 shows an asymmetric tolerance which for practical purposes should be limited to its maximum symmetric variation. This shows how variations in the device input capacitance will have a minimum tolerance if they cause radial excursions in $S_{11}(f_o)$ and a maximum tolerance if they cause excursions of $S_{11}(f_o)$ along the alternating line of Figure 1. The tolerance in the device input capacitance would be that percentage change which caused $S_{11}(f_o)$ to lie on the Γ_{max} circle.

The change in $S_{11}(f)$ with frequency is given by the equation,

$$\frac{\partial S_{11}(f)}{\partial f} = j\,\frac{S_{21}(f)S_{12}(f)}{2Z_L(f)}\,\frac{\partial X}{\partial f} + \frac{S_{21}{}^2(f)}{2Z_L(f)}\left[\left(C\,\frac{\partial A}{\partial f} - A\frac{\partial C}{\partial f}\right) Z_L{}^2(f) + \left(C\,\frac{\partial B}{\partial f} + D\,\frac{\partial A}{\partial f} - A\,\frac{\partial D}{\partial f} - B\,\frac{\partial C}{\partial f}\right) Z_L(f) + D\,\frac{\partial B}{\partial f} - B\,\frac{\partial D}{\partial f}\right], \qquad (3)$$

where A, B, C, and D are the ABCD matrix parameters for the matching network. Equation (3) shows that for all low Q or resistive matching networks the absolute direction of $\partial S_{11}(f)/\partial f$ is exactly the same as that of $\partial S_{11}(f)/\partial X(f)$,

depending only on the sign of $\partial X/\partial f$. For these networks reactive variations in the load have their maximum tolerance when the magnitude of $S_{11}(f)$ is a constant over the passband, i.e. the matching filter has a flat mismatched response. While practical networks are not resistive and rarely low Q, equation (3) leads to the conclusion that matching networks should provide a flat mismatch at least over the center of the band and should not have large ripples. For this reason a Butterworth filter has a midband tolerance to load reactance variations greater than a Chebyshev filter even when the Butterworth response has a flat mismatch greater than the peak of the Chebyshev (Figure 2 and Table II). The superior performance of the Butterworth response in its midband is due to its 90 degree angle factor.

A classical approximation for the tolerance of a filter to load variations is given by [5,6]

$$\%\ \text{classical tolerance}\ (f) = 100 \cdot \frac{\Gamma_{max} - |S_{11}(f)|}{|S_{11}(f)|\,|S_x^{S11}|}, \quad (4)$$

where S_x^{S11} is the classical sensitivity defined as:

$$S_x^{S11} = \frac{X(f)}{S_{11}(f)} \frac{\partial S_{11}(f)}{\partial X(f)} .$$

Note that equation (1) may be used to compute the classical sensitivity without the need for a derivative.

This approximation gives the minimum bound on the load reactance tolerance as the tolerance goes to zero. A better approximation to the load reactance tolerance uses the angular relationship between $S_{11}(f)$ and its change with respect to a load reactance to give

$$\%\ \text{corrected tolerance}\ (f) = 100 \cdot \frac{d_{min}}{|S_{11}(f)|\,|S_x^{S11}|} \quad (5)$$

where

$$d_{min} = \text{minimum } \{S_{11} \cos(\phi - \theta) \pm \sqrt{\Gamma_{max}^2 - [S_{11} \sin(\phi - \theta)]^2}\ \}$$

and $S_{11} = |S_{11}(f)|$, $\phi = \angle S_{11}(f)$, $\theta = \angle \frac{\partial S_{11}(f)}{\partial X(f)}$.

The difference between θ and ϕ is the angle factor, and maximum tolerances occur at odd multiples of 90°. This tolerance measure will always be greater than or equal to the classical first order tolerance approximation because the classical tolerance uses the minimum radial distance from $S_{11}(f_o)$ to the Γ_{max} circle, as seen by the dashed line in Figure 1, while the corrected tolerance includes the angle of response variation. It will be demonstrated in the results section that this corrected tolerance gives a better approximation to the tolerance magnitude and the frequency where the circuit first falls out of specification.

Because the Butterworth filter has optimal midband tolerances, and poor tolerances at the band edges, a more tolerant filter can be derived from a response which has a wide, flat mismatch at the midband and small dips in $S_{11}(f)$ toward the band edges. It is important that the dips in $S_{11}(f)$ do not go to zero so that they cause only a small ripple in the response. An increase in band edge tolerances results. This new response appears as a mismatched second order Chebyshev filter. The filtering polynomial, however, is not a Chebyshev polynomial. The new filter polynomial has two ripples for all orders and exists only for third and higher order filters. A Chebyshev polynomial, however, may be considered as a degenerate case for a second order filter. The filtering polynomial has a larger tolerance to load variations over its passband than a Butterworth, Chebyshev, or a mismatched version of either. For a third order filter the polynomial is:

$$F_{3\alpha}(p) = \frac{\beta}{\alpha^2} p^3 + \frac{1}{\alpha^2} p^2 + \beta p + 1, \qquad (6)$$

where α is the distance to the $S_{11}(f)$ zeros (matched case) in the normalized filter,

$$\beta = \frac{\sqrt{2\alpha^2-1}}{1-\alpha^2}$$

and $p = \sigma + j\omega$. The characteristics of this filter are:

$$F_{n\alpha}(0) = 1.0,$$

$$F_{n\alpha}(j\alpha) = 0.0,$$

and $F_{n\alpha}(j) = 1.0$ for the matched case.

This may be used to construct a fourth order filter with the same α as a third order, and higher orders may be obtained from the recursion formula:

$$F_{(n+1)\alpha} = (p^2 + 1)F_{(n-1)\alpha} + pF_{n\alpha}, \tag{8}$$

where n is the order of the filter*

Results

The network of Figure 3 was used to examine the tolerances of Butterworth, Chebyshev and the new filter to variations in a series load capacitance. In order to give a fair comparison between the filter types, each filter is designed to have a bandwidth such that

$$\int_0^\infty \ln\left|\frac{1}{S_{11}(f)}\right| d\omega = K \tag{9}$$

where K is the same for all filters. All filters, therefore, have the same ability to absorb complex load reactances.

The maximum percentage tolerance of a series or parallel load capacitance assuming that $S_{11}(f_o) = 0$, the matching network is lossless, the network is reciprocal and the percentage change in the capacitance is small is calculated

*A fourth order polynomial is:

$$F_{4\alpha}(p) = \frac{p^4}{\alpha^2} + \frac{1}{1-\alpha^2}p^3 + \frac{\alpha^2+1}{\alpha^2}p^2 + \frac{\alpha^2}{1-\alpha^2}p + 1$$

with the expression,

$$\% \text{ tolerance} = \frac{200}{Q_f} \cdot \frac{\Gamma_{max}}{\sqrt{1-\Gamma_{max}^2}} , \qquad (10)$$

where Q_f is the device input Q at f_o. This expression establishes an upper limit for circuit tolerancing and aids in device selection.

In the network shown in Figure 3 the load is a narrowband model of the input impedance of a 250μ wide FET used over the 3.7 to 4.2 GHz range. L_f, C_f and R are 1.4 nH, .3 pF and 8 ohms respectively. Note that ideal responses were obtained by neutralizing the load reactances with negative components and using an ideal transformer. In practice, Youla's broadband equalization theory [7] would be used to neutralize the load reactances and the ideal transformer could be absorbed into the filter by Norton's transformation or the use of imittance inverters. Figures 3 and 4 show plots of third order Chebyshev and Butterworth filters with a normal and 2% high FET capacitance. These plots are only from 3.75 to 4 GHz for clarity, and have the normal capacitance, .3 pF, as the circled points and the high value as triangular points. These filters were designed for peak reflections less than .26 from 3.7 to 4.2 GHz. Note how the Chebyshev filter violates its specifications in the midband while the mismatched Butterworth filter fails at the band edges. The Butterworth filter also had a higher K than the Chebyshev which shows that for a given value of K a Chebyshev response is a better choice than a Butterworth response.

The Chebyshev filter is less tolerant because the reactance variation causes a change in $S_{11}(f)$ that is not quite tangent to $S_{11}(f)$ at the ripple peaks (the angle factor is not 90 degrees), and the change in $S_{11}(f)$ due to reactive load variations becomes tangent to the curve of $S_{11}(f)$ at higher frequencies. This means that the rapid magnitude change in $S_{11}(f)$ allows

reactive variations in the load to cause nearly radial variations in $S_{11}(f)$ thereby degrading the tolerance. Chebyshev (and Elliptic) responses are only optimal when both passband and stopband responses have tight specifications. As can be seen from Figures 4 and 5, the mismatched Butterworth response has a greater tolerance in the midband even though its smallest reflection is equal to the peak reflection of the Chebyshev. The Butterworth filter's tolerance is reduced at the band edges because variations in the load reactance cause changes in $S_{11}(f)$ which begin to be tangent to the $S_{11}(f)$ vector. Since the Butterworth filter has nearly ideal tolerance properties in its midband, modifying its band edge response will lead toward optimally tolerant filters.

As shown in equation (1), the design of load tolerant filters in lossless reciprocal structures involves only the manipulation of the $S_{21}(f)$ vector. Reciprocal structures must rely on angular relationships or loss for tolerant design, as seen via the $S_{21}(f)$ and $S_{12}(f)$ terms in equations (1) and (3). The $S_{12}(f)$ term in equation (1) shows how circulators and isolators allow tolerance to load variations in nonreciprocal networks. A second point of clarification concerns the straight lines drawn in Figure 1. The bilinear nature of networks causes most variations to have a finite curvature. This causes the calculations in equations (4), (5) and (10), which are based on the straight lines of Figure 1, to be approximate.

Various bandpass networks represented by Figure 3 were characterized by their tolerances to load reactance variations, element variations and loss over the 3.7 to 4.2 GHz range. Table I gives the element values for a Chebyshev filter of .5 GHz bandwidth and $\rho_{max} = .26$, a mismatched Chebyshev filter of .5617 GHz bandwidth, $\rho_{max} = .23$ and $\rho_{min} = .115$, and a mismatched version of the filter of equation (6) with .53 GHz bandwidth, $\alpha = .78$, $\rho_{max} = .23$ and $\rho_{min} = .115$. All of the filters have a center frequency of 3.942 GHz.

All of the above filters also have a K, as defined by equation (10), of approximately 7.4×10^9. This was done to ensure a physical basis of comparison since K relates directly to the load reactance which may be absorbed by the filter [1]. For lossy filters, the conductances and resistances of Table I appear in parallel or series with their respective resonant circuits shown in Figure 3. A large bandwidth Butterworth filter with large mismatch, $\rho_{min} = .278$, was included to show how it is the combination of the angle factor and the reflection coefficient magnitude that determine the tolerance to load variations. As shown in Table II, this Butterworth filter has a larger tolerance than the Chebyshev filter, yet its reflection coefficient is always greater than the Chebyshev. However, the Butterworth filter shown here is not comparable to the other filters, because of its bandwidth of 2 GHz which makes its K far too large for comparison (see Figure 2).

Table II gives the tolerances of the various filter types to load reactance variations. The additional tolerances in Table II are for the first and second least tolerant filter elements, as labeled. The tolerance information is given for a maximum $S_{11}(f) = .333 = \Gamma_{max}$ with only one component being varied. This table shows that the mismatched Chebyshev and the new filter have up to a fifty percent increase in device tolerance and a three hundred percent increase in element tolerances over a Chebyshev filter. Furthermore, the new filter shows a greater increase in device tolerance and most sensitive element tolerance than the mismatched Chebyshev. These increases in tolerance can make circuits much easier to tune and even eliminate tuning in some cases. The mismatched Butterworth response is tabulated only to illustrate the effect of the angle factor on circuit performance. This wide bandwidth filter has a nearly constant reflection

coefficient of $\rho = 0.278$ across the 3.7 to 4.2 GHz band, and an angle factor around 90 degrees. Although the reflection coefficient of this Butterworth response is higher than the peak reflection coefficient of the Chebyshev response, the Butterworth filter has a larger tolerance to load variations. The larger tolerance is due to the 90 degree angle factor of the broadband Butterworth filter, and so demonstrates the importance of the angle factor in tolerant filter design. The improvement of the mismatched Chebyshev response over the normal Chebyshev response may be attributed to the reduction of its maximum reflection coefficient, while the improvement of the new filter over the mismatched Chebyshev is because the new filter has an angle factor nearer to 90° at the peak of $S_{11}(f)$. Thus, the new filter is the most tolerant design. The ideal tolerance of equation (9) is included in the table as an approximate upper limit for the device tolerance.

Table III compares the tolerances of the new filter to load reactance variations using the first order classical [equation (4)] and angle factor corrected [equation (5)] methods. The classical method gives a minimum device tolerance of 1.3% at 3.94 GHz, while the corrected method gives a minimum device tolerance of 1.7% at 3.85 and 4.05 GHz. The actual device tolerances are 1.83% at 3.85 GHz and -1.8% at 3.7 and 4.05 GHz simultaneously. This demonstrates that the corrected response gives a better measure of the device tolerance and the frequency where the specification is violated.

It is well known that monolithic microwave circuits are lossy compared to hybrid circuits. Therefore it is important to noise figure and circuit performance that the filters be affected as little as possible by loss. Figures 6 through 9 demonstrate the effects of uniform element Qs of 25 on the three filter types discussed. In both reflection and transmission, the new filter is least affected by loss. The new filter gives .7 and 2.5 db less loss at the band edges and .4 and 1.3 db less loss at the band center than the

mismatched and normal Chebyshev filters, respectively. Note that predistortion would help the band edge response but hurt the band center response. The end result is that the new filter would give a better noise figure than either of the Chebyshev filters. Table IV compares the tolerances of the lossy filters. Again, the new filter gives an overall higher tolerance to both element and device (load) variations.

Table V gives the tolerance results for a broadband FET feedback amplifier. This amplifier used a 750 μ wide FET of C_f = .6pF and g_m = .065 mhos with an LC matching filter (C_1, L_2) and a feedback resistor (R_{FB}) of 180 ohms, as shown in Figure 10. The FET model included source inductance and other pertinent components. Two different matching filters were used with this amplifier, and have responses shown in Figure 11. The first design was "tuned" to provide zero reflection near 7 GHz, and results in a familiar humped response. The second response was designed to give a finite but flatter VSWR across the entire band. This latter design is less straightforward, but results in a much greater tolerance to both the FET and the circuit elements.

Conclusion

The consideration of the angle between the $S_{11}(f)$ vector and the change in $S_{11}(f)$ due to load reactance variations has been used to design a more tolerant filter characteristic. This angle factor also explains why Chebyshev filters have a low tolerance for a given mismatch. A corrected first order approximation to load reactance tolerance was given which has greater accuracy with no additional circuit calculations. While the filter was designed specifically for a greater tolerance to load reactance variations, the filter showed increased tolerances to element variations and the effects of loss. Since insensitivity to loss and the greatest possible tolerances are essential

to designing lower cost and easily tuned microwave circuits, the design techniques described above should aid the production of all microwave circuits, especially monolithic circuits.

The basic concepts of this paper are given in equations (1) and (5). These may be generalized to state that the sensitivity of any element in a filter is proportional to the product of the amount of power delivered to it from the source and the amount of power it may deliver back to the source; and that since circuit respones are vectors, it is useful to view the problem of maximizing a tolerance as that of maximizing the distance the response must travel before it violates a specification. These concepts are best satisfied in reciprocal filtering networks by using a mismatched response and making the angular relationship between the response and its perturbation due to any one element variation equal to an odd multiple of 90 degrees.

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TABLE I

FILTER ELEMENT VALUES
f_o = 3.942 GHz

Type	BW (GHz)	n	C_1(pF)	L_1(nH)	G_1(mΩ)	L_2(nH)	C_2(pF)	R_2(Ω)	C_3(pF)	L_3(nH)	G_3(mΩ)
Chebyshev	.5	2.5	8.729	.1867	8.648	18.11	.09	17.94	8.729	.1867	8.64
Chebyshev (mismatched)	.5617	2.228	8.585	.1899	8.51	13.99	.1165	13.86	7.005	.2327	6.94
New filter ($F_{3.78}$ mismatched)*	.53	1.978	8.594	.1897	8.52	12.49	.131	12.37	5.138	.3173	5.09
Butterworth** (mismatched)	2.0	1.879	.5735	2.842		.447	3.64		.213	7.64	

*This denotes a third order filter with reflection zeros at .78 of the filter bandwidth.
**The Butterworth response has too large a bandwidth and is used only for illustrating the importance of the angle factor.

TABLE II

BANDPASS MATCHING FILTER TOLERANCES

Filter	Circuit Parameters: BW(GHz)	ρ_{max}	Device C_f	Allowed Element Tolerances (%) for Γ_{max} = .333 and 3.7-4.2 GHz range (see Figure 3): 1	2
Chebyshev	.5	.26	1.22%	.64% L_2, C_2	1.96% C_1, L_1
Chebyshev	.5617	.23	1.43%	2.02% L_2, C_2	3.39% C_1, L_1
New Filter	.53	.23	1.8%	2.9% C_1, L_2	3.05% L_2, C_2
Butterworth*	2.	.278	2.2%		
Ideal (eqn 10)			3.9%		

*The Butterworth response has too large a bandwidth for meaningful comparison and is used only to illustrate how the angle factor allows a relatively high tolerance even when the reflection coefficient is large.

TABLE III

LOAD REACTANCE TOLERANCE OF LOSSLESS FILTERS

	Classical (eqn 3) Tol (%)	Classical (eqn 3) Freq (GHz)	Corrected (eqn 4) Tol (%)	Corrected (eqn 4) Freq (GHz)	Actual Tol (%)	Actual Freq (GHz)
Chebyshev	.9	3.825	1.3	3.825	1.2	3.83
Chebyshev (mismatched)	1.2	3.8	1.4	3.825	1.43	3.825
New Filter (mismatched)	1.3	3.94	1.7	3.85	1.83	3.85

TABLE IV

ELEMENT TOLERANCES OF LOSSY FILTERS

element Q = 25

Allowed Element Tolerances (%) for Γ_{max} = .333 and 3.7-4.2 GHz range (see Figure 3 and Table I)

Filter	Circuit Parameters BW(GHz)	Circuit Parameters ρ_{max}	Device C_f	Circuit 1		Circuit 2	
Chebyshev.	.5	.26	1.1%	.4%	C_1, L_1	1.2%	L_2, C_2
Chebyshev	.5617	.23	1.6%	.9%	C_1, L_1	2.2%	L_2, C_2
New Filter	.53	.23	1.8%	.9%	C_1, L_1	2.4%	L_2, C_2

TABLE V

MATCHING FILTER TOLERANCES

Broadband FET Amplifier (1-9 GHz)

Allowed Element Tolerances (%)

for Γ_{max} = .333 and S_{21}>1.75

Filter	Matching Filter C_1(pF)	L_2(nH)	Device C_f	Circuit 1	2
Tuned	.37	.92	>.5%	>.5% L_2	>1% g_m
Flattest	.2	.7	>6%	>11% g_m	>13% R_{FB}

Figure 1. A Smith chart containing the maximum tolerable reflection, Γ_{max}, and the input reflection coefficient at f_o, $S_{11}(f_o)$. The dashed radial line represents the direction of minimum absolute variation in $S_{11}(f_o)$. The alternating line perpendicular to the $S_{11}(f_o)$ vector represents the direction of maximum absolute tolerance since the distance between $S_{11}(f_o)$ and the Γ_{max} circle is maximized.

Figure 2. A plot of VSWR versus frequency for a third order Chebyshev filter (solid line) with a peak reflection of .258, a mismatched Chebyshev filter (dashed line) with maximum and minimum reflection of .23 and .115 respectively, and a large bandwidth mismatched Butterworth filter (alternating line) with a midband reflection coefficient of .278.

Figure 3. The third order lumped filter network used in examining the tolerances of filter responses. Inductors and capacitors one through three represent lossless filter elements. R, C_f and L_f represent a narrowband model of an FET input impedance. The ideal transformer and negative elements are used to equalize the filter for the complex FET impedance without disturbing the filter components. This enables filter and device component variations to be analyzed.

Figure 4. Input reflection plot of a narrowband mismatched Butterworth filter versus frequency. The circles represent the true response, and the triangles represent the response with C_f designed to cover 3.7 to 4.2 GHz, but only 3.75 to 4 GHz is shown for clarity. The Γ_{max} circle is for a reflection coefficient of .333. Note how the Butterworth filter fails at the band edge and has ideal tolerance characteristics in its midband.

Figure 5. Input reflection plot of the Chebyshev filter in Figure 2. Only 3.75 to 4 GHz of the 3.7 to 4.2 GHz passband is shown for clarity. Again, the Γ_{max} circle is at a reflection of .333, the circles represent the true response, and the triangles represent the response for a 2% increase in C_f. Note how the Chebyshev response is moved in a nearly radial direction at the response peak. This radial variation causes the Chebyshev to have a poor tolerance to load variations.

Figure 6. VSWR versus frequency plot for three of the filters described in Tables I through IV. The solid line is the Chebyshev with a peak reflection of .258. The dashed line is a mismatched Chebyshev with reflection maxima and minima of .23 and .115 respectively. The alternating line is the new filter with reflection maxima and minima of .23 and .115 respectively. All of the filters have the same return-loss bandwidth product, which means they all have the same ability to equalize a complex load.

Figure 7. VSWR versus frequency plot for the filters described in Figure 6 having lossy elements with Q's of 25. Note the narrow bandwidth of the Chebyshev (solid line) and the flat response of the new filter (alternating line).

Figure 8. Gain versus frequency plot for the lossless filters described in Figure 6. Note the Chebyshev (solid line), mismatched Chebyshev (dashed line), and mismatched $F_{3.78}$ (alternating line) responses. The new filter has a double peaked response for all orders.

Figure 9. Gain versus frequency plot for the filters described in Figure 6 having lossy elements with Q's of 25. The Chebyshev response (solid line) is severely rounded and has the greatest loss. The mismatched Chebyshev response (dashed line) has less loss, but the lowest loss is in the $F_{3.78}$ response (alternating line). The $F_{3.78}$ response is relatively flat and has one to two db less loss than the Chebyshev response. This allows less tuning and a lower noise figure.

Figure 10. Model of an FET feedback amplifier.

Figure 11. VSWR versus frequency plot for the FET feedback amplifier with a tuned input matching network (solid line), and a flat response matching network (dashed line).

IMPEDANCE COORDINATES—50-OHM CHARACTERISTIC IMPEDANCE

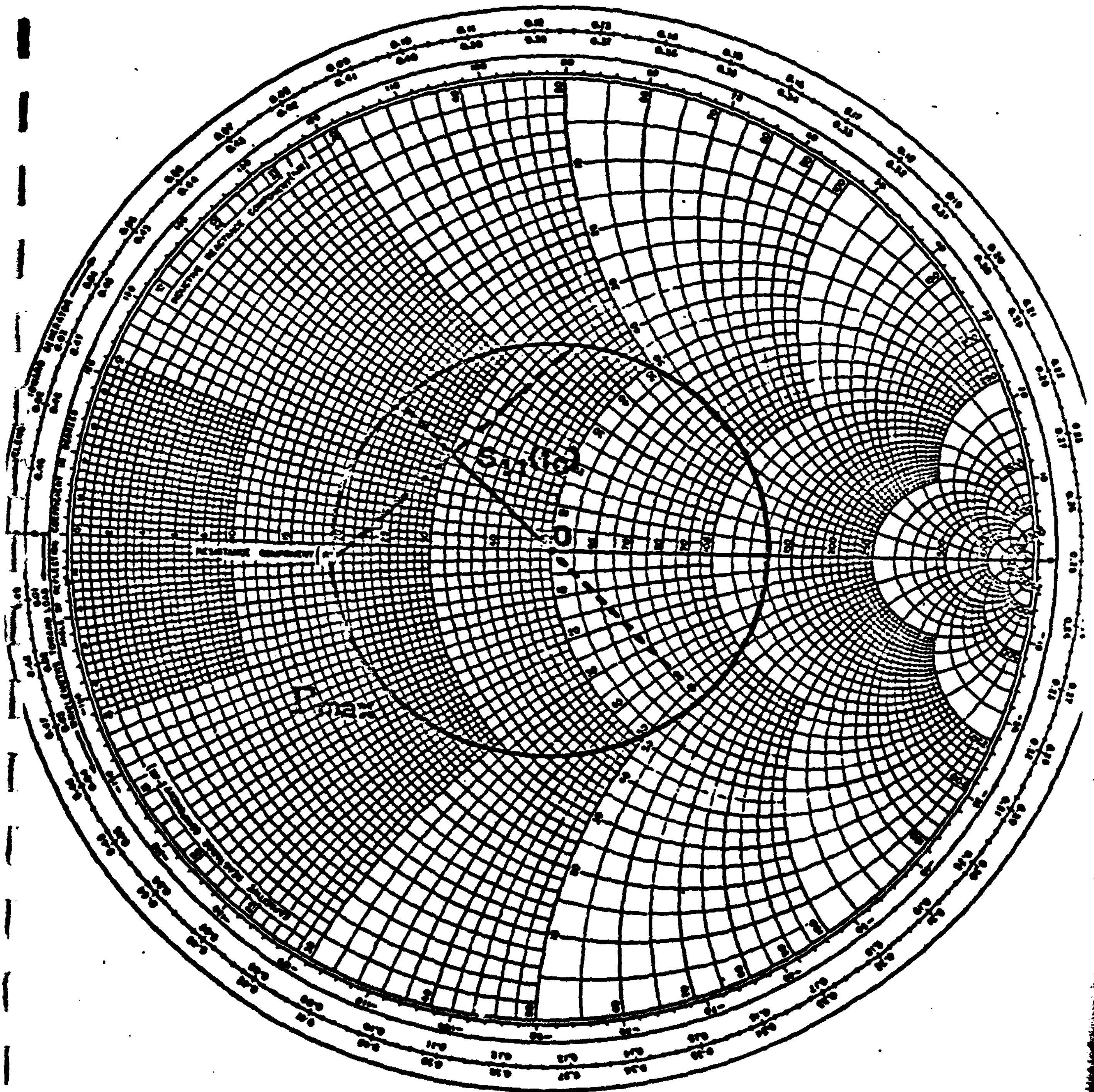
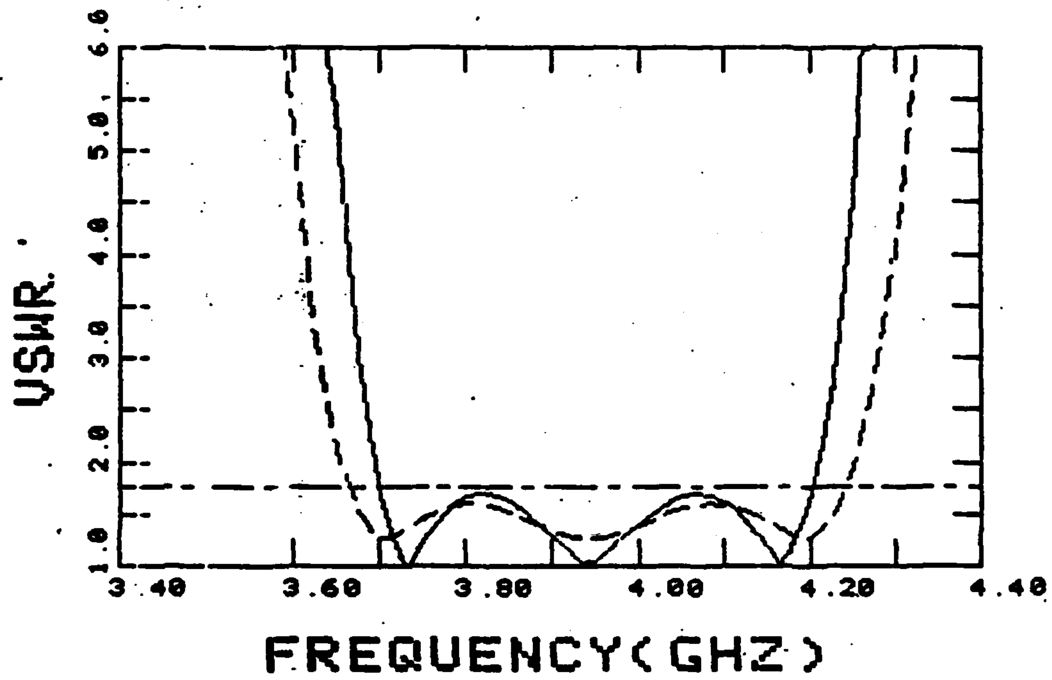
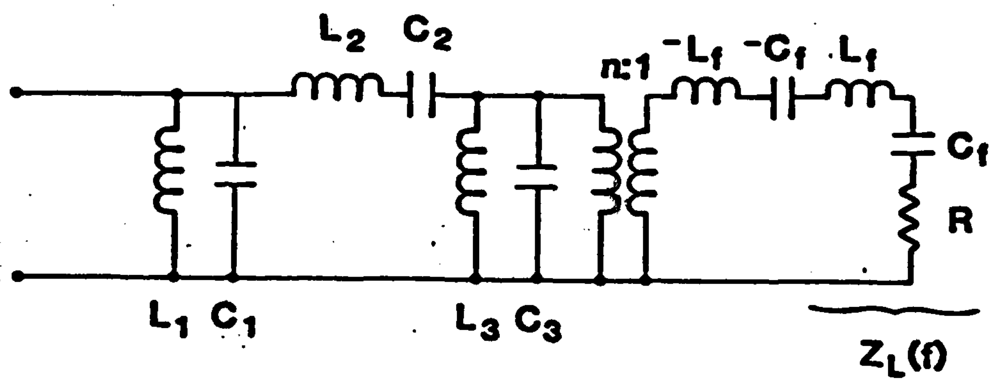


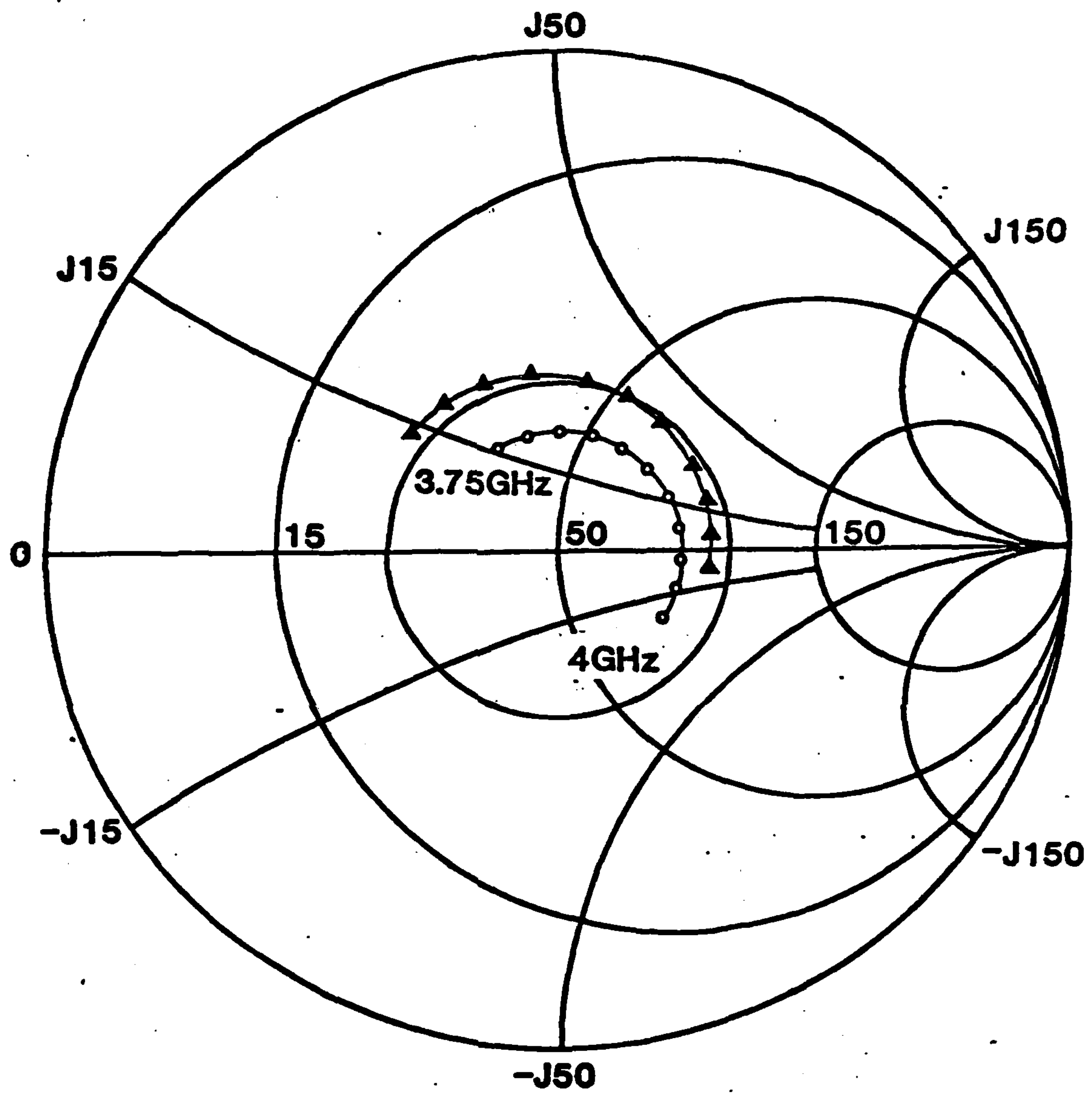
Fig 2

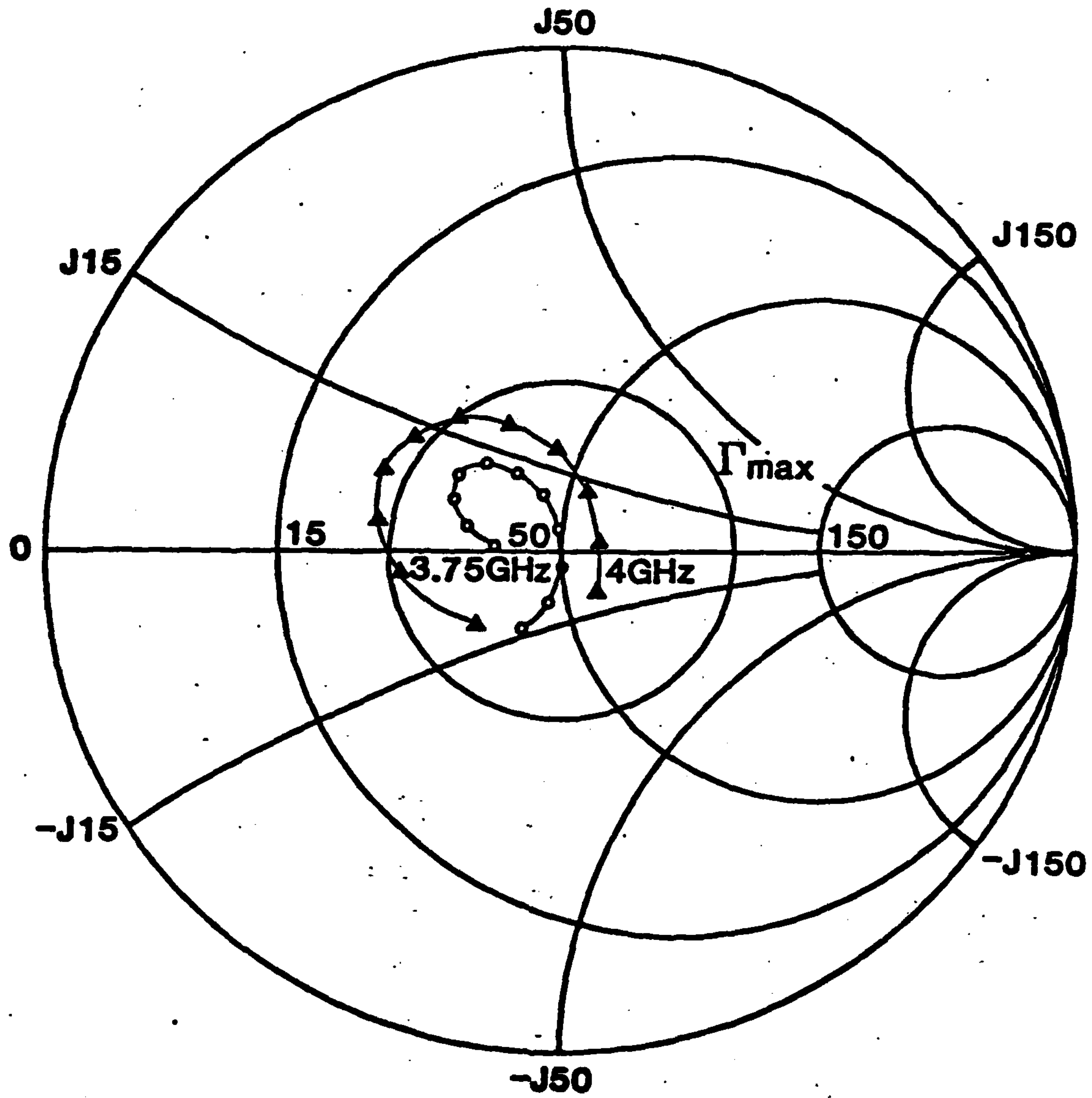


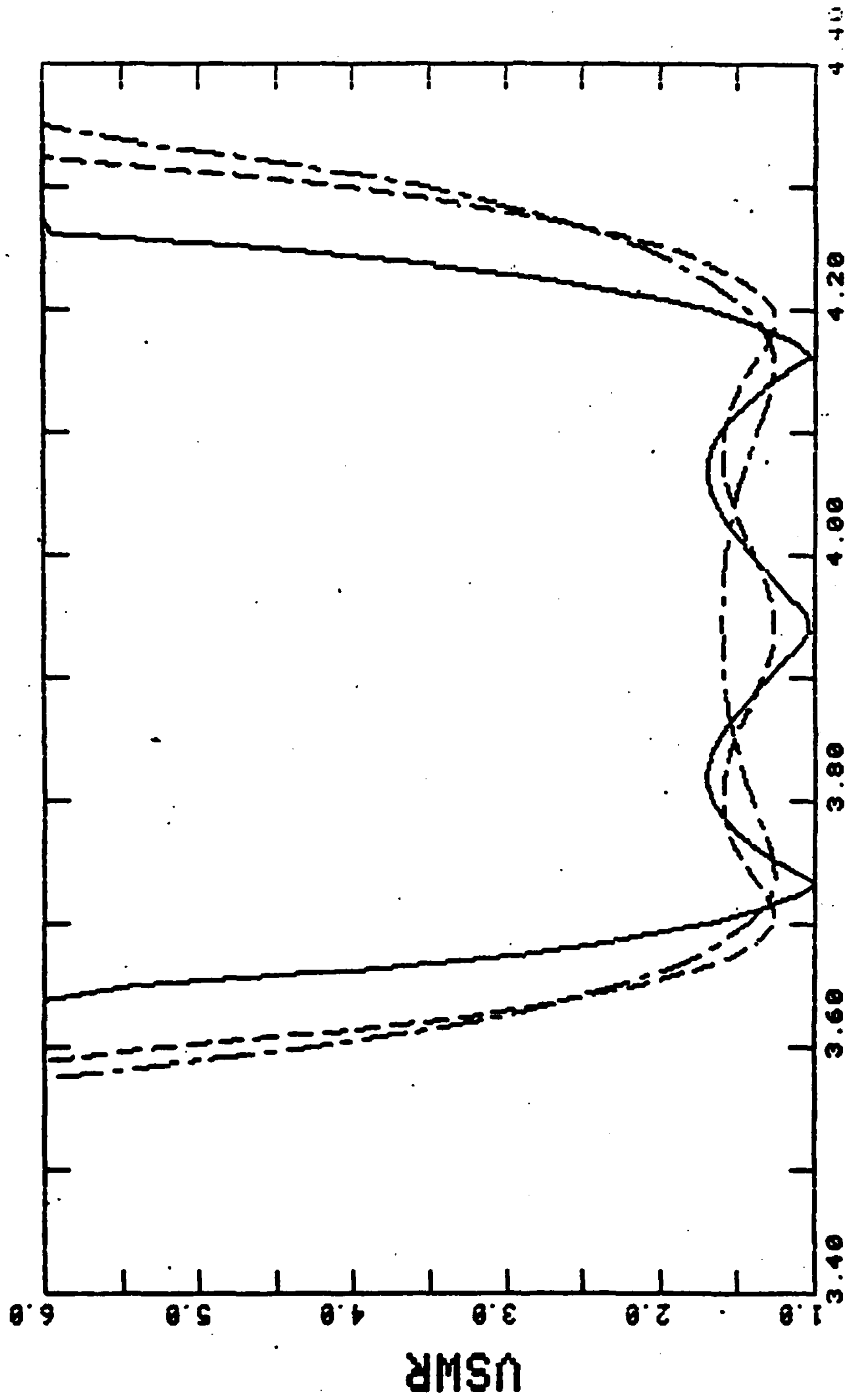
VSWR
1.0
2.0
3.0
4.0
5.0
6.0
3.40
3.60
3.80
4.00
4.20
4.40
FREQUENCY(GHZ)



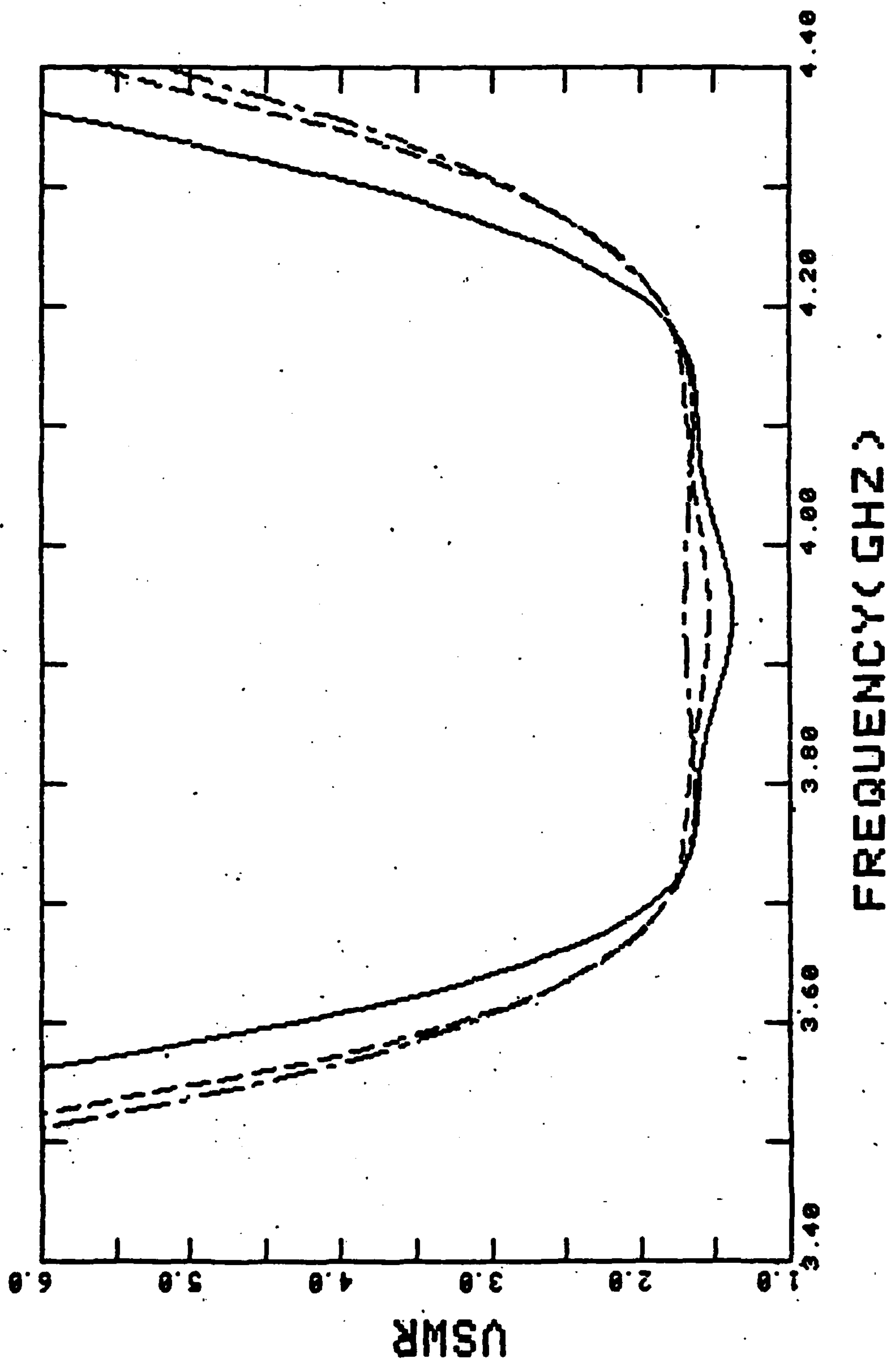
L2
C2
n:1
-Lf
-Cf
Lf
Cf
R
L1
C1
L3
C3
ZL(f)


J50
J150
J15
3.75GHz
0
15
50
150
4GHz
-J15
-J150
-J50

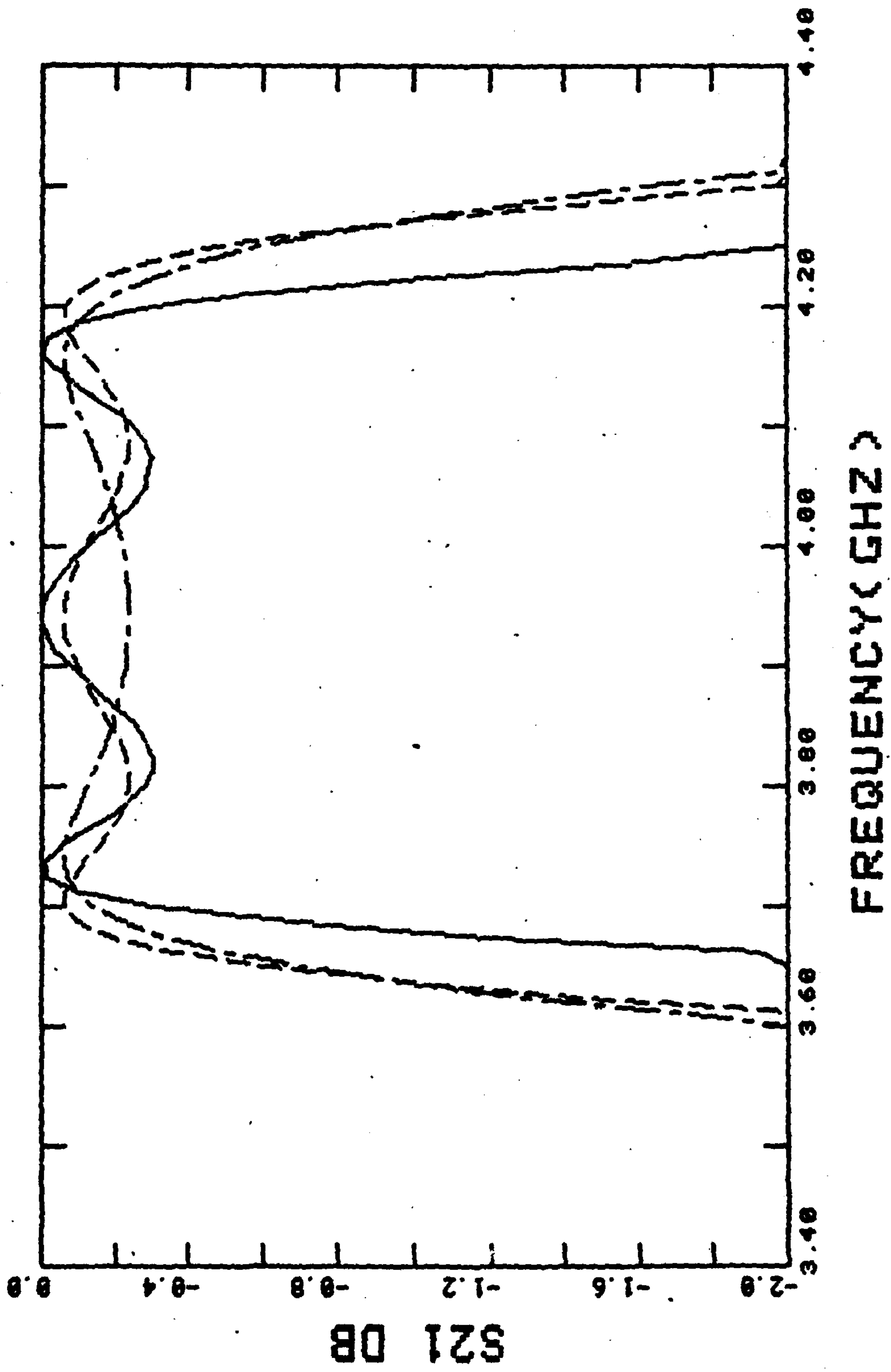

J50
J15
J150
Γ_{max}
0
15
50
150
3.75GHz
4GHz
-J15
-J150
-J50

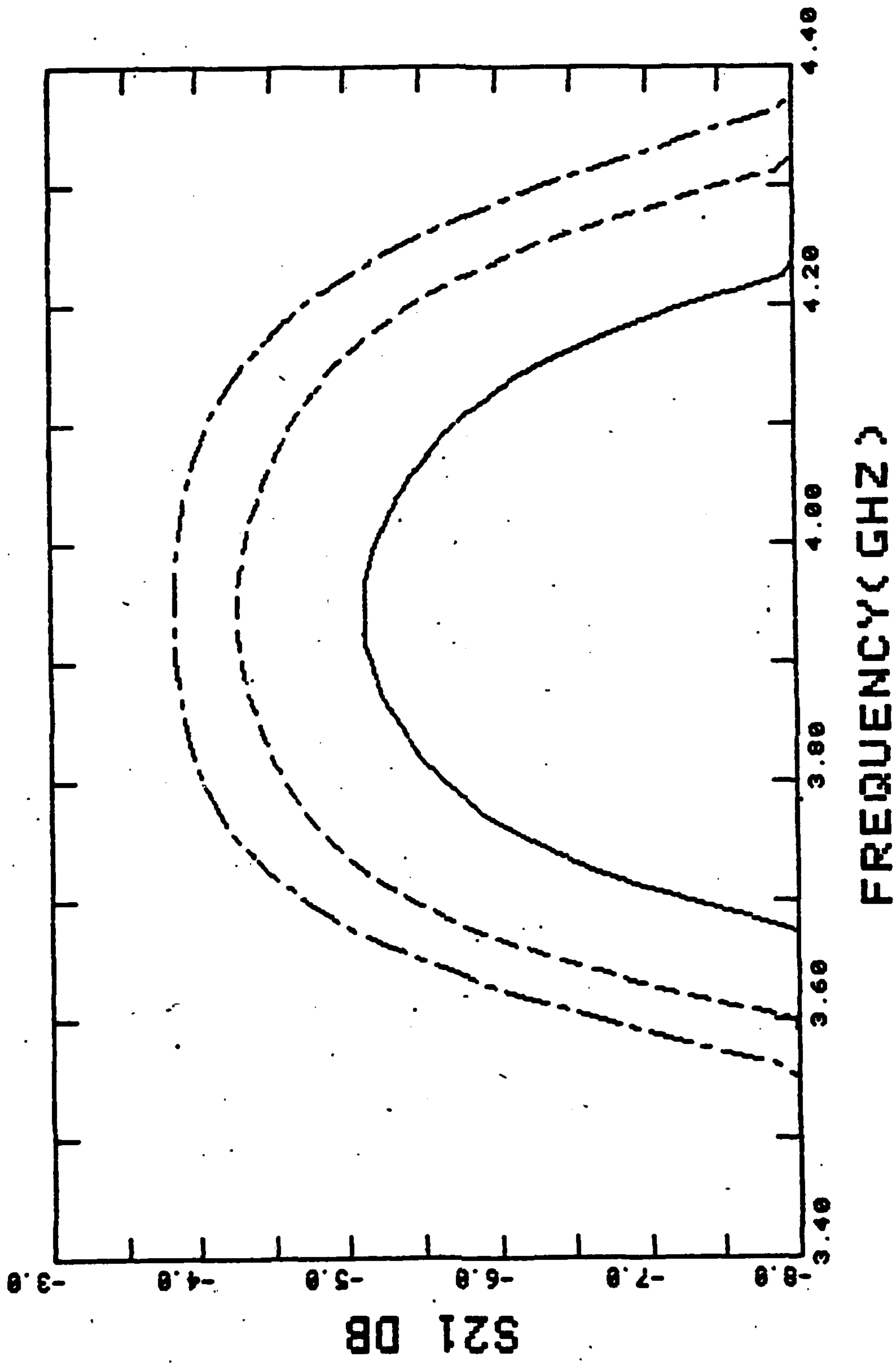


VSWR
1.0
2.0
3.0
4.0
5.0
6.0
FREQUENCY(GHZ)
3.40
3.60
3.80
4.00
4.20
4.40

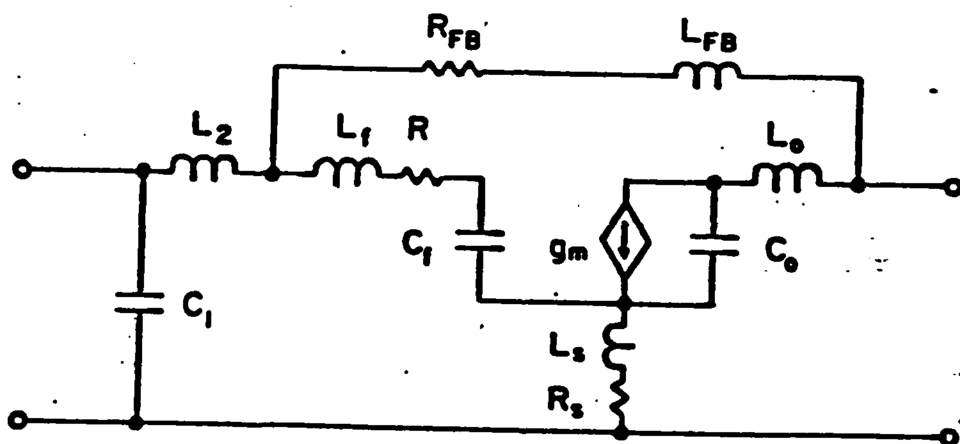


FREQUENCY(GHZ)
3.40
3.60
3.80
4.00
4.20
4.40
USWR
1.0
2.0
3.0
4.0
5.0
6.0

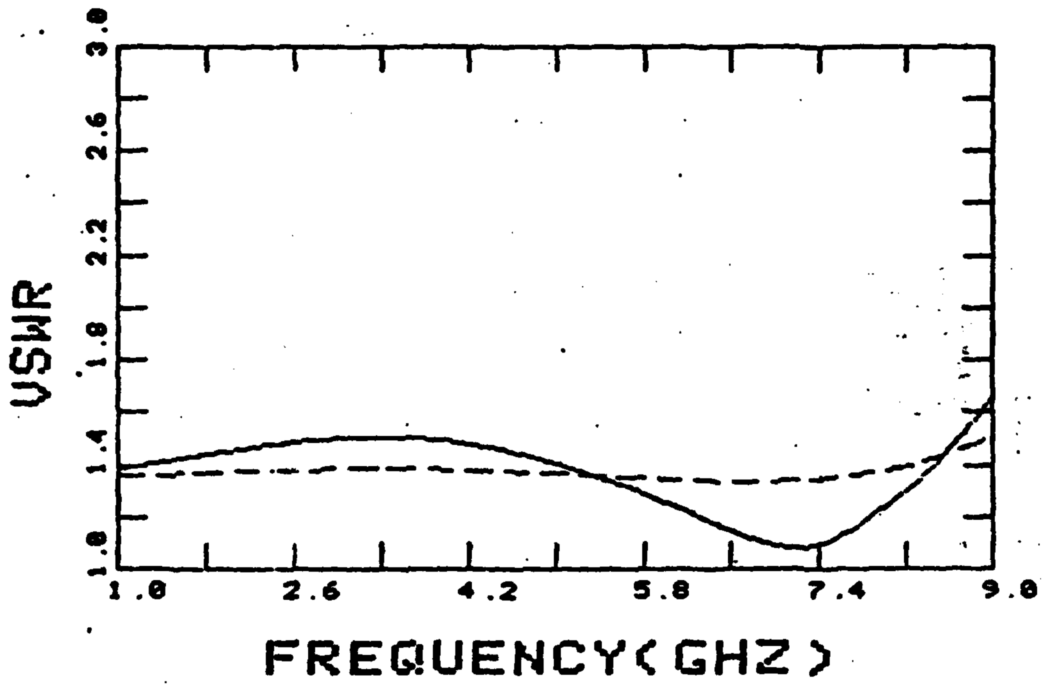

S21 DB
0.0
-0.4
-0.8
-1.2
-1.6
-2.0
FREQUENCY(GHZ)
3.40
3.60
3.80
4.00
4.20
4.40



FREQUENCY(GHZ)
3.40
3.60
3.80
4.00
4.20
4.40
S21 DB
-3.0
-4.0
-5.0
-6.0
-7.0
-8.0



R_{FB}
L_{FB}
L_2
L_f
R
L_o
C_f
g_m
C_o
C_i
L_s
R_s


VSWR
1.0
1.4
1.8
2.2
2.6
3.0
1.0
2.6
4.2
5.8
7.4
9.0
FREQUENCY(GHZ)

A Theory of Even and Odd Order Low-Pass Impedance Matching Filters*

A. N. Riddle and R. J. Trew
Electrical and Computer Engineering Department
North Carolina State University
Raleigh, North Carolina 27650
(919) 737-2336

ABSTRACT

A theory of impedance matching with low-pass filters is presented which includes both even and odd order networks. It is shown that the odd order networks contain an insensitive element which should prove useful in minimizing the tuning (and thus the cost) of microwave amplifiers. A fifth order Chebyshev network is used as an example in which the last shunt capacitor in the matching network is varied ±50% while maintaining a VSWR < 1.5:1 over nearly an octave.

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INTRODUCTION

Low-pass LC filter networks have formed the basis of many useful impedance matching networks [1-5]. This is because low-pass networks resemble the topology of most devices (especially bipolar transistors), low-pass networks allow bias current to pass to the device, and low-pass networks are less sensitive to component variations than band-pass networks. Various impedance-transforming low-pass networks (matching filters) have been designed [2-4] using a low-pass filter prototype with a transformation which results in an even order low-pass matching filter with twice the number of components as the original filter. Tables of these networks have proved useful in amplifier design [6]. It should be emphasized that the networks described in [2-4] are true impedance matching devices which are capable of zero reflection coefficients and unity gains at specific frequencies. These networks accomplish this by virtue of the frequency transformation used in their filtering function. The filtering function is typically of a Butterworth, Chebyshev or Elliptic function form. The frequency transformation maps ω to a function of ω^2 which creates an even order filter with an even number of components. The resulting filtering function has twice the order of the filtering function before application of the frequency transformation. While odd-order matching filters [7] are at least as useful as even-order matching filters, a derivation of the odd-order filtering function has not been reported. This paper presents an extension to the theory of low-pass

impedance matching filters by including a derivation of the filtering function for filters with even and odd numbers of components.

Since definitive treatments of broadband equalization networks already exist [8,9], this paper will not discuss those methods. Rather, this paper describes the derivation of the impedance matching polynomials to be used in Youla's method of equalization. A simple method of reactance equalization is described in this paper to illustrate the usefulness of odd-order, low-pass matching filters. The filters described in this paper should not be confused with those in [8] since the latter achieved impedance matching with ideal transformers and this paper describes low-pass filters capable of impedance transformation.

A main point in this paper is the demonstration of how the symmetry of odd-order networks allows a certain component to vary with little influence on the impedance matching properties of the network. The insensitive component is the reactance in series with the larger terminating resistance, or the reactance in parallel with the smaller terminating resistance. This means that the shunt capacity of a bipolar transistor input impedance may be used as part of the matching network, and yet device-to-device variations will cause negligible change in circuit performance. This property results because the first component in series with a low load impedance (with respect to the generator impedance) has a greater influence on impedance matching than the component in parallel with the load impedance. Therefore, such circuits have an inherent insensitivity to device variations. This inherent insensitivity is very important in the development of low-cost microwave amplifiers using on-chip matching networks.

Traditionally, impedance matching networks are divided into classes which do [1] and do not [2] use ideal transformers. This paper considers the insertion-loss theory of low-pass impedance matching networks without ideal transformers. Two classes of polynomials are presented in order to demonstrate the use of this theory in both narrow- and broad-band matching networks.

Throughout this paper, network frequency and impedance scaling notation [7] is used so that $R_1 = 1\ \Omega$ and $\omega_1 = 1$ Hz.

THEORY

The following method for synthesizing matching networks is based on what is loosely termed "insertion-loss" theory. This theory uses the ideas of a lossless network and the conservation of energy. Consider a generator, lossless network, and a load resistance as shown in Fig. 1. It is assumed that the generator is capable of delivering one unit of power, and it follows that the sum of the power reflected from the network and the power transmitted to the load must equal unity, the power available from the generator. In S-parameter notation [10],

$$|S_{11}(p)|^2 + |S_{12}(p)|^2 = 1, \tag{1}$$

where generally $p = \sigma + j\omega$ and $S_{12}(p) = S_{21}(p)$ (from reciprocity). $S_{11}(p)$ and $S_{21}(p)$ are represented by the polynomial functions $D(p)$ and $H(p)$ as shown in equations (2) and (3),

$$S_{11}(p) = \frac{D(p)}{H(p)} \tag{2}$$

$$S_{21}(p) = \frac{1}{\sqrt{\epsilon}\ H(p)} . \tag{3}$$

The polynomial which describes the characteristic function of the matching filter, $D(p)$, must allow the transfer function of the network, $S_{21}(p)$, to have a loss at $p=0$ which is dependent upon the generator and load resistances, and zero loss at some specified frequencies. Using S-parameter notation, and $p=j\omega$,

$$S_{21}(p)S_{21}(-p) = \frac{1}{\epsilon D(p)D(-p) + 1} + \frac{1}{\epsilon H(p)H(-p)}, \qquad (4)$$

where, with reference to Fig. 1,

$$\epsilon = \frac{(R_1-R_2)^2}{4R_1R_2} \qquad (5)$$

and

$$D(p) = (1 + bp)M(p^2), \qquad (6)$$

where $M(p^2)$ satisfies certain conditions, and b is a parameter. The conditions on $M(p^2)$ are that

$$M(0) = 1, \qquad (7)$$

and for some given ω_i, the matching frequencies,

$$M(-\omega_i^2) = 0. \qquad (8)$$

The parameter b is a real number which is approximately proportional to the square of the Q of the load resistance and the component nearest the load. An empirical expression for b in the case of a fifth order Chebyshev network, which is given in the synthesis example, is

$$b = \left(\frac{C_5\ R_2}{.42(1 + \frac{.095}{R_2})}\right)^2 . \qquad (9)$$

Note that for b=0, the C_n in Fig. 1 becomes zero (i.e., an open circuit), the network is of even order and the expressions reduce to those described by existing theory [8].

The narrow-band case may be satisfied by allowing $M(p^2)$ to be a polynomial (in p^2) with the binomial coefficients. This allows

$$M(0) = 1$$

and,

$$M(-\omega_o^2) = 0 \Big|_{\omega_o = 1}.$$

For example, a sixth order function using the binomial coefficients would be:

$$M(p^2) = 1 + 3p^2 + 3p^4 + p^6 \quad (10)$$

so,

$$M(0) = 1$$

and,

$$M(-\omega_o^2) = 1 - 3\omega_o^2 + 3\omega_o^4 - \omega_o^6$$

$$= 0 \Big|_{\omega_o = 1}.$$

The broad-band matching filter is developed collateral with [2] and [3]. This development uses the transformation

$$w = \frac{\omega^2-\omega_o^2}{A} \quad (11)$$

with the well known Chebyshev polynomials, $C_n(w)$[12], where n is the degree of the polynomial. The variables in (7) are

$$\omega_o = \frac{\omega_U^2+\omega_L^2}{2}, \text{ the center radian frequency,} \quad (12)$$

and

$$A = \frac{\omega_U^2-\omega_L^2}{2}, \text{ a bandwidth parameter} \quad (13)$$

where

ω_U = the upper passband edge, and

ω_L = the lower passband edge.

Then,

$$M(-\omega^2) = \frac{C_K(w)}{C_K(w_z)} \qquad (14)$$

where
$$K = \begin{cases} \frac{n-1}{2} & n \text{ odd} \\ \frac{n}{2} & n \text{ even} \end{cases}, \qquad (15)$$

and

$$w_Z = w \Big|_{\omega=o} .$$

SYNTHESIS

It will prove useful to give an example of matching filter synthesis. This example will consist of a fifth order Chebyshev matching filter. A fifth order network is chosen so that the zeros of the Chebyshev function will be evident and the insensitivity of the element nearest the load can be demonstrated. Note that impedance and frequency scaling have been used.

Consider the matching filter of Fig. 2 terminated with

$$R_1 = 1.0\ \Omega$$

$$R_2 = .3333\ \Omega\ .$$

Via equation (5) it is found that

$$\varepsilon = .3333\ .$$

Let us take $\omega_o = 1$ and choose a bandwidth of approximately 31%. Therefore it is chosen that

$$A = .3115,$$

since A is a paremeter roughly equal to the fractional bandwidth. Once A and ω_o are known, both ω_U and ω_L may be found by using equations (12) and (13), so,

$$\omega_U = 1.145$$

$$\omega_L = .8295 \quad .$$

Since n = 5 is odd, K = 2 from equation (15), and so the second order Chebyshev polynomial found in [12] may be combined with equation (11) to yield,

$$M(-\omega^2) = \frac{C_2(w)}{C_2(w_z)} = \frac{2w^2-1}{2w_z^2-1}, \qquad (16)$$

$$= \frac{A^2}{2\omega_o^4}\left(\frac{2\omega^4}{A^2} - \frac{4\omega_o^2\omega^2}{A^2} + \frac{2\omega_o^4}{A^2} - 1\right), \qquad (17)$$

$$M(-\omega^2) = \frac{1}{19.615}(20.615\ \omega^4 - 41.229\ \omega^2 + 19.615) \qquad (18)$$

and

$$M(p^2) = 1.051\ p^4 + 2.102\ p^2 + 1.$$

Then, letting b=1,

$$D(p) = (1+p)M(p^2)$$
$$= 1.051\ p^5 + 1.051\ p^4 + 2.102\ p^3 + 2.102\ p^2 + p + 1. \qquad (19)$$

The matching filter is synthesized from this characteristic function by using the relations,

$$S_{21}(p)S_{21}(-p) = \frac{1}{\epsilon D(p)D(-p)+1} = \frac{1}{\epsilon H(p)H(-p)}$$

$$= 1 - S_{11}(p)S_{11}(-p) \ .$$

These relations reduce to

$$S_{11}(p) = \frac{D(p)}{H(p)}, \tag{20}$$

where the quadrantal symmetry of the zeros of $\varepsilon D(p)D(-p)+1$ may be used to efficiently derive $H(p)$ within a constant multiplier. This constant multiplier is found by recognizing that since these are low-pass filters,

$$\lim_{p\to\infty} S_{11}(p) = \lim_{p\to\infty} \frac{D(p)}{H(p)} = \pm 1, \tag{21}$$

so,

$$\lim_{p\to\infty} H(p) = \pm \lim_{p\to\infty} D(p) \tag{22}$$

with the positive sign generally used.

The network elements are then derived by a continued fraction expansion of

$$Y(p) = \frac{1 + S_{11}(p)}{1 - S_{11}(p)}. \tag{23}$$

Substituting equation (19) into equations (4), (1), and (20) gives the result of equation (23) as

$$Y(p) = \frac{2.1\ p^5+3.87\ p^4+7.45\ p^3+8.58\ p^2+5.77\ p+3}{1.76\ p^4+3.24\ p^3+4.38\ p^2 + 3.77\ p+1}. \tag{24}$$

A continued fraction expansion of equation (24) gives the elements of Fig. 2 as

$C_1 = 1.19$ F

$L_2 = .79$ H

$C_3 = 2.94$ F

$L_4 = .463$ H

and $C_5 = 1.64$ F.

It should be recognized that if C_5 was the parasitic capacity of a load impedance, then equation (9) could have been used to calculate b so that the synthesized network would achieve a C_5 of the desired value. In the previous example,

$$b = \left(\frac{C_5 R_2}{.42(1+\frac{.095}{R_L})}\right)^2 = \left(\frac{(1.64)(.3333)}{.42(1+\frac{.095}{.3333})}\right)^2 = 1.03$$

which is so close to the chosen b=1 as to give an excellent approximation.

SENSITIVITY

In order to demonstrate the insensitivity of the matching characteristics of this network to variations in C_5, where C_5 may be taken as the parasitic parallel capacity associated with the load, the VSWR of the network was calculated as C_5 was varied $\pm$ 50%.

The solid, dashed, and alternating lines in Fig. 3 indicate the network's input VSWR for $C_5 = 1.64$ F, $C_5 = 1.5\,(1.64)$F and $C_5 = .5\,(1.64)$F, respectively. Note that the variation of C_5 shifts the center frequency of the network, and increased the input VSWR (Fig. 3); however, the network obtains a VSWR <1.5 for almost an octave in all cases.

The insensitivity of these networks is a general property which can be deduced from the Chain (ABCD) matrix representation [13]. This representation shows that the use of different resistors in a doubly terminated network will cause the transfer function to be less dependent on the last element at one end of the filter. For the odd-order filter with shunt elements at the input and output, the element nearest the low resistance termination is least sensitive. Thus, the odd-order filter is the only network which is capable of a desensitized shunt capacitor on the low impedance side of the network.

This desensitization may be heuristically explained by noting that the basic matching circuit is in the form of an L-network. A match between two unequal resistances is mainly dependent upon the first element shunting the larger resistance, and the first element in series with the lower resistance. Because of this, elements in shunt with the lower resistance and in series with the higher resistance play a lesser role in the matching circuit.

Conclusions

A general form for the characteristic function of a low-pass matching filter has been introduced. This characteristic function allows both even and odd-order networks to be derived. Furthermore, it has been shown that the odd-order networks can minimize the sensitivity of the matching filter to variations in the parallel capacity of a low impedance load. This property should be useful for monolithic circuits and the internal matching networks of packaged transistors. In the interest of generality, two different classes of polynomials have been given which satisfy the requirements of the characteristic function for narrow-band and broad-band applications.

It should be noted that the parameter b is roughly proportional to the square of the Q of the last element and the termination in the matching filter. Therefore, as b is reduced, the bandwidth of the filter will increase slightly as the odd order filter degenerates to an even order filter.

This analysis is presented to further the understanding of impedance matching networks. Since impedance matching is sine qua none in microwave amplifiers and antennas, the microwave engineer should have as many tools as is possible.

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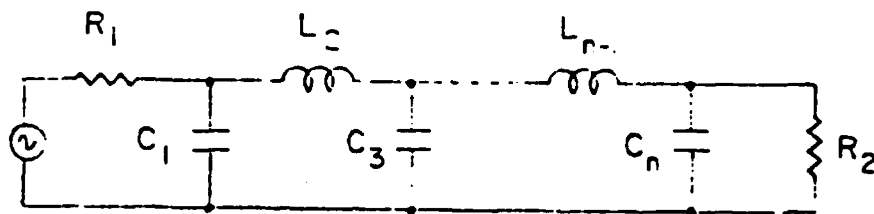

Fig. 1 General odd order low-pass network with source resistance, R_1, and load resistance, R_2.

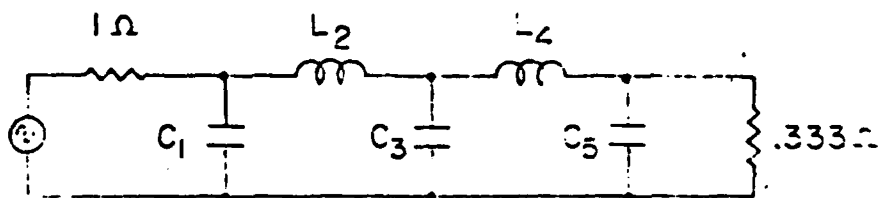

Fig. 2 Fifth order low-pass matching filter with element values given in the text.

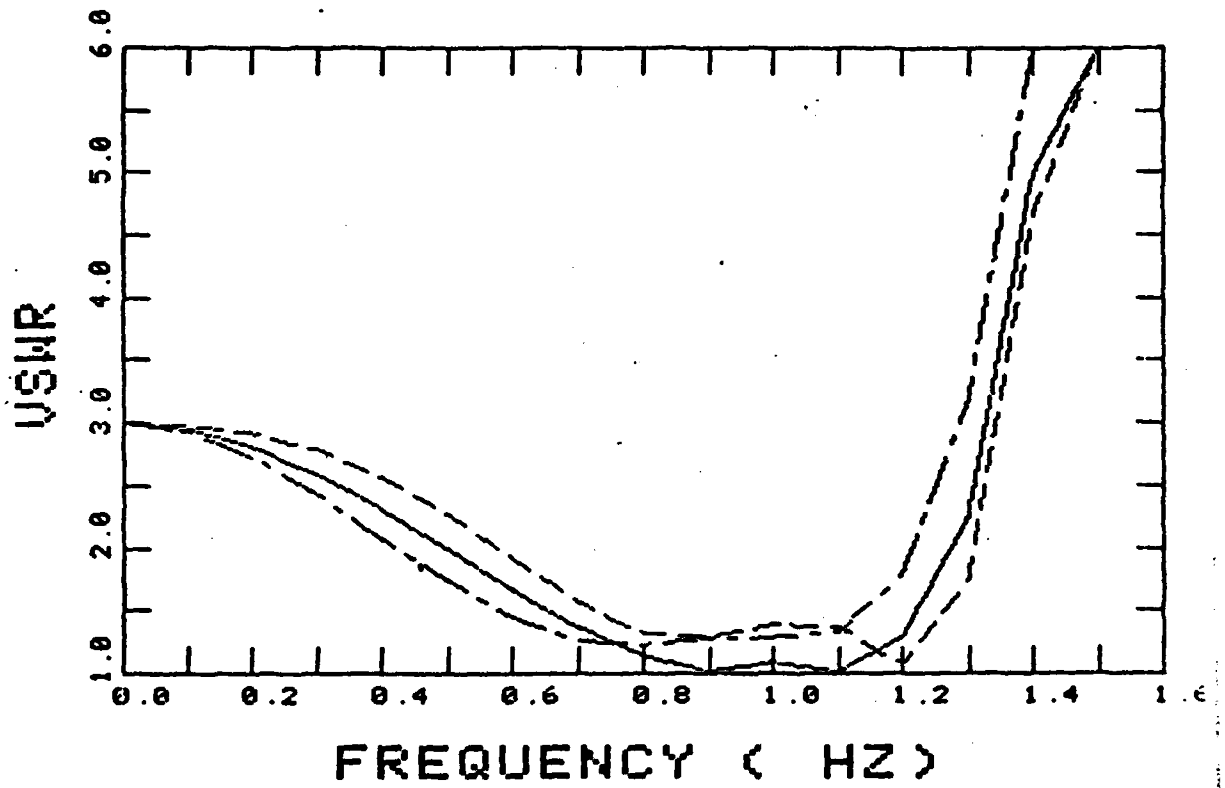

Fig. 3 Input VSWR of circuit in Fig. 2 as C_5 is varied ±50%. The solid line represents the original filter.

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