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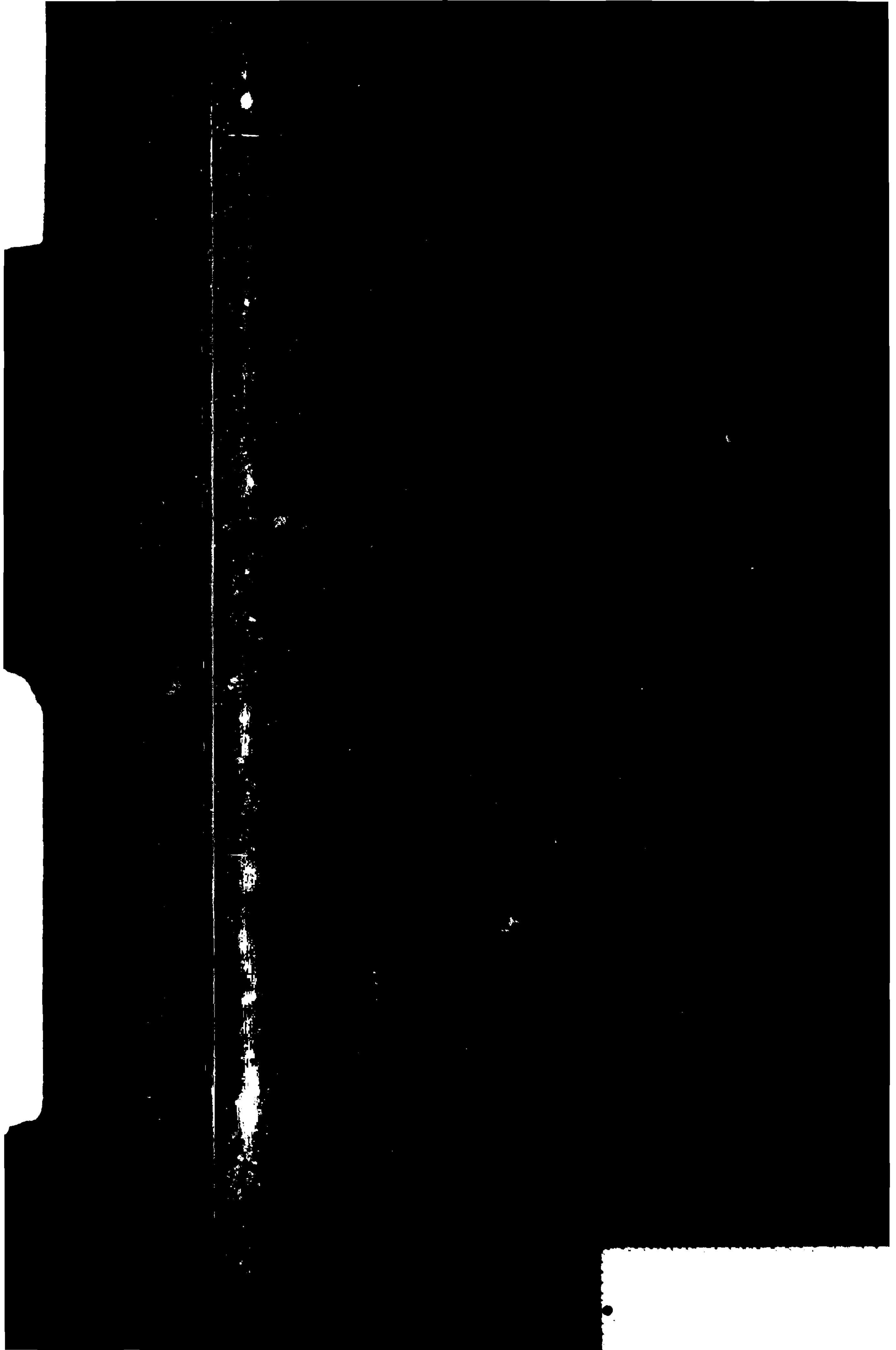

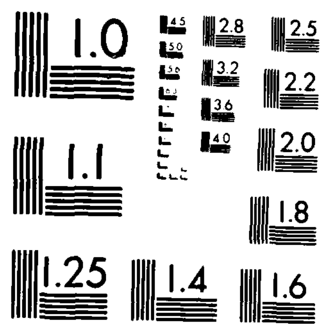

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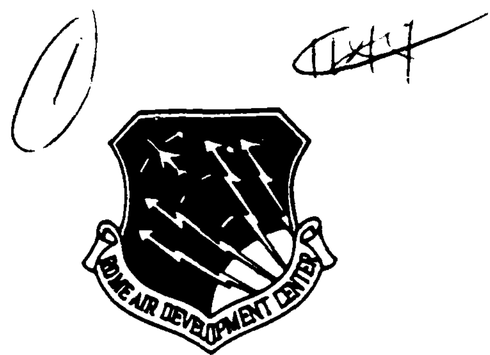

RADC-TR-84-32
Final Technical Report
February 1984

AD-A150 237

PARALLEL TEST METHOD FOR LSI MICROPROCESSORS

McDonnell Douglas Corporation

Raymond M. Koenig, Jr.

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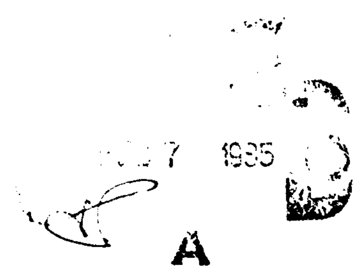

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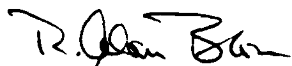
APPROVED: 

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The parallel testing concept consists of connecting together the corresponding inputs and outputs of devices-under-test to perform monitored testing. Failures are detected by changes in supply current to the paralleled set and isolated by differences in individual device currents. The parallel testing concept was first presented by R. Alan Blore of the Rome Air Development Center (RADC) at the International Symposium for Testing and Failure Analysis in 1980.

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The purpose of this investigation was to evaluate, refine, and demonstrate the parallel testing technique for application to LSI microcircuit reliability evaluations. This report describes the investigation of various areas that required definition for parallel testing, such as current detectors, failed device identification, interconnect schemes, noise, and latch-up. The results show that for the implementation studied in the report, a number of trade-offs must be made in the test parameters and circuit configuration to achieve a successful parallel test, due to interactions between paralleled devices. These trade-offs included: (a) latch-up vs. noise, hardware cost, elevated temperature level, and instruction set, (b) clock cycle time vs. noise, and (c) potential damage to failed devices left on test vs. hardware cost.

We successfully demonstrated the parallel testing concept for two selected device types, a 6504 4K static RAM and an 1802 8-bit microprocessor, by conducting a 500-hour elevated temperature lift test while continuously monitoring device functional operation and periodically simulating faults. Further refinements of the parallel test concept focused on improved techniques to avoid latch-up and damage to failed devices left on test.

EVALUATION

Increasingly complex devices are increasingly more difficult to test both electrically and for reliability. The time necessary to perform functional evaluation on an electrical tester quickly becomes unaffordable. Adequate stress testing is far more demanding. New approaches and techniques to device characterization must be developed. Because of the time available during the burn-in and life tests, device functional characterization has increased at the stress chamber. This has taken the form of monitored stress testing.

Monitored testing couples device output verification with the dynamic exercise pattern to check device functionality. It allows the use of the longer stress test times for device evaluation increasing the amount of functional verification that can be performed and decreasing the amount of electrical testing that need be performed. Monitored testing of devices in the stress chamber is becoming commonplace.

Monitored testing today uses XOR gates for each and every output to monitor the device functionality. For memory devices with multiplexed outputs, good chamber densities with moderate amounts of hardware can be achieved since the monitor hardware is shared by multiple banks of devices under test.

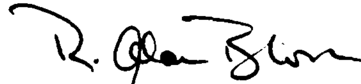
For the vast majority of digital logic part types such sharing is not possible. To monitor 100 devices with 19 outputs each requires 1900 signal lines to the outside world. Clearly, the density of devices under test (as well as the reliability of the test hardware) diminishes rapidly. The parallel test addresses the need for monitored testing of high pin count devices while reducing the number of connections to the outside world and the amount of support hardware required to perform the monitoring. In short, the input and the output signal lines of the devices under test are bussed to like pins on the other devices under test forming out of many devices effectively a single device with the ability to detect failure via changes in the supply currents. Any and every part is functionally verified on all pins by all other devices under test. From note 2 to Table 6-1, page 83, it can be concluded that of the three possibilities examined, parallel testing is the only potentially feasible means to perform monitored testing on such sample sizes.

This report documents a first step to transition the parallel test from concept into a useable test method. The reader will find many avenues open to alternative implementations. There are many alternatives with excellent prospects for addressing difficulties identified in this study. Some of those alternatives are presented in Section 6. The reader is encouraged to pursue those ideas and others. Work at RADC subsequent to this contract has shown operation of six 1802s at 15V with a 2MHz clock without latch up. Output stuck at faults as well as input and internal logic faults have been simulated and detected. Work is progressing on alternate current detectors. The concept is also being tried with TTL.

There are many applications for parallel testing. In this study the demonstration test was dynamic. Parallel testing will work for static also. Be it static or dynamic, for go/no-go testing such as burn-in,

identification of part failure may be sufficient. Once the part is identified as a failure no additional electrical testing need be performed. The availability of current monitoring resistors in the supply lines of each device and the ability to measure the voltage across those resistors provides the opportunity to track the stability of each device under test during the stress test. Information on population homogeneity is available since significant differences in device timing will show as propagation mismatches in response. Hence, parallel testing can provide functional and parametric (leakage and timing differences) information during the stress test. Work at RADC has also shown that parallel testing may have application in device characterization, device design analysis, majority voting and fault tolerant circuits, and in-circuit fault detection.

Finally, a quote from page 90 of the report. "This study has served to illuminate these problems and to suggest possible solutions for these so that future studies of the parallel test method may focus attention where most needed."



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PREFACE

The work described in this report was performed between October 1981 and April 1983 by the Parts Application Branch of the McDonnell Douglas Astronautics Company - St. Louis Division (MDAC-STL) Effectiveness Engineering Department. The work was performed for the USAF Rome Air Development Center under Contract Number F30602-81-C-0269. Mr. R. Alan Blore, the government's technical monitor, provided helpful suggestions for improving the parallel test hardware that are discussed in this report. In addition to the many MDAC-STL personnel who contributed to the program, special thanks are extended to Messrs. Lance Lombardo, Roy Maurer, and Gary Keller. Additional thanks are due to Mr. Alvin Sasaki and Dr. Clovis Hale for providing the engineering management needed to complete the program.

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1.0 INTRODUCTION

The objective of this program was to develop and formalize a parallel technique for Complementary Metal Oxide Semiconductor (CMOS) Large Scale In (LSI) devices such that the technique is usable for reliability characteriz studies and capable of being transferred to users. This program was initia because the parallel testing technique offers potential for reducing the co monitored testing of microcircuits.

Our approach consisted of four stages. In Stage I, we procured and tes CMOS LSI device types: a 4K memory and an 8-bit microprocessor. In Stage evaluated and made necessary refinements to a baseline concept previously i gated by R. Alan Blore of the USAF Rome Air Development Center (RADC). Usi refined concept, we conducted demonstration testing in Stage III. Finally, Stage IV, we evaluated the results of the demonstration tests and proposed refinements.

The details of our study are provided in this report, which is divided the following sections: 1) Introduction, 2) Background, 3) Initial Program Activities, 4) Evaluation and Refinement of the Basic Concept, 5) Demonstra Testing, 6) Further Evaluation and Refinement, and 7) Summary and Conclusio

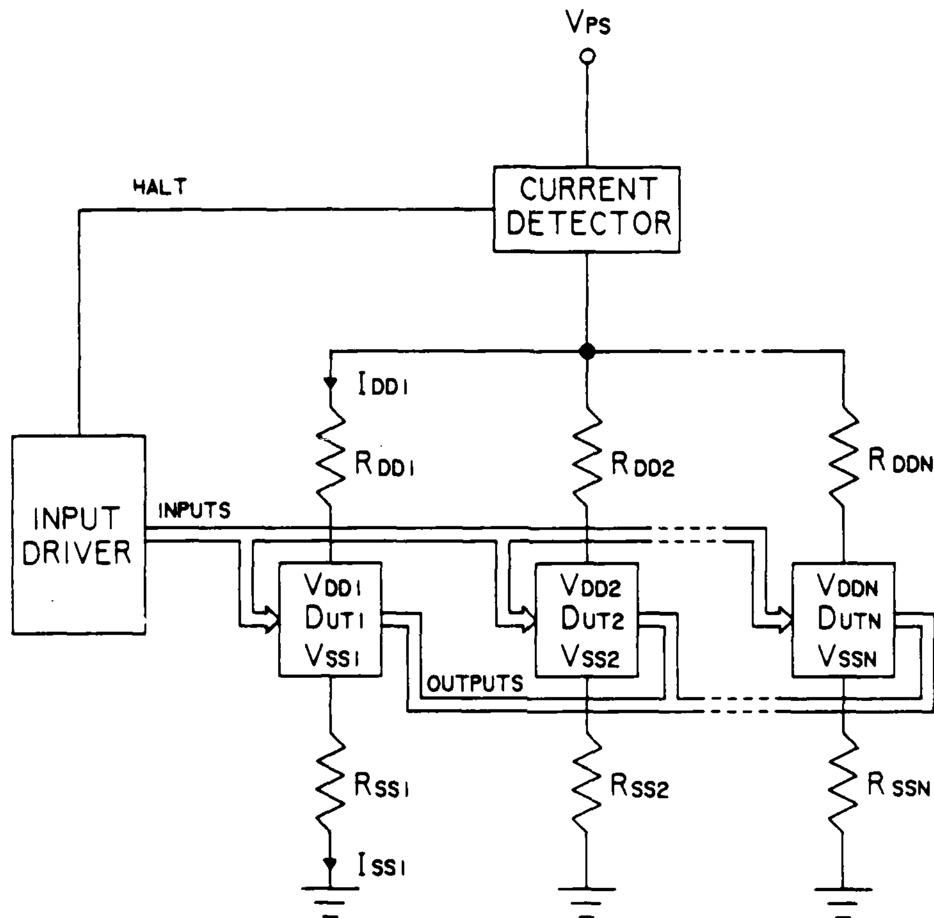
2.0 BACKGROUND

As LSI devices become more complex, it becomes too costly to conduct time-consuming and comprehensive functional tests using expensive automated test equipment. Therefore, a more cost effective method for functionally testing complex microcircuits is needed.

RADC reported a parallel test method in 1980 that utilized CMOS small-scale (4001 NOR gate) and medium-scale (1852 input/output port) integrated circuits (References 1 and 2). The parallel technique, as illustrated in Figure 2-1, connects the corresponding inputs and outputs of "N" devices in parallel. Correct operation of all "N" devices is verified by monitoring the total power supply current to the "N" devices while operating all devices in a functional manner. If all devices are operating correctly, all outputs will be at the same voltage levels and total supply current will be nominal. If a single device output is different from the other "N-1" devices in parallel, the resulting increase in supply current will be noted by the current detector shown in Figure 2-1. To determine which specific device exhibited an incorrect output voltage level requires measuring the current in individual I_{DD} and I_{SS} lines. Resistors (R_{DD} and R_{SS}) are utilized to measure the I_{DD} and I_{SS} currents in individual devices.

Preliminary experiments performed by RADC showed that the parallel technique worked well with small and medium complexity devices at relatively low operating speeds (100 Hz). It was a promising technique for reducing the cost of comprehensive functional testing of CMOS LSI microcircuits. Additional details of the RADC work may be found in Appendix A, which is a reproduction of Reference 1. The objectives of the study described herein were to refine the parallel test method (PTM) proposed by RADC and demonstrate its functionality, practicality and usefulness for testing CMOS LSI microcircuits.

The approach used in this study is outlined in Figure 2-2. Details of the four stages noted in Figure 2-2 are presented in the four major sections that follow.



NOTE: CORRESPONDING INPUTS AND OUTPUTS ARE PARALLELED

FIGURE 2-1. BASELINE PARALLEL CONCEPT

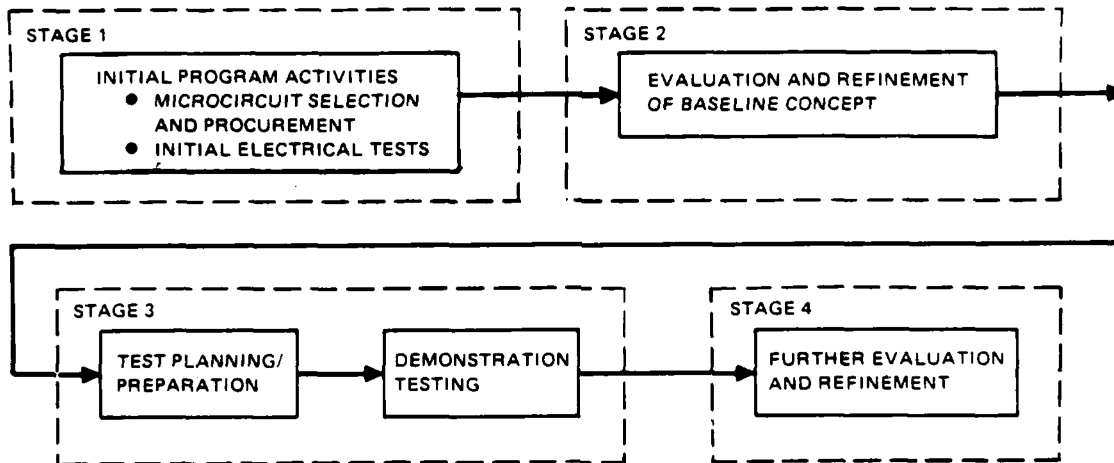


FIGURE 2-2. PROGRAM OVERVIEW

3.0 STAGE I: INITIAL PROGRAM ACTIVITIES

The primary objectives during Stage I were to select and obtain the program test devices, conduct visual examinations and hermeticity tests, update test software, and perform initial electrical tests.

3.1 MICROCIRCUIT SELECTION AND PROCUREMENT

The device types selected for this program were the Harris HM1-6504-2, 4K CMOS static RAM, and the RCA CPD1802D, 8-bit CMOS microprocessor. (These device types will be referred to as the 6504 and 1802 throughout the remainder of this report.) The 6504s and 1802s were originally procured to the manufacturer's catalog specifications. The 6504s are sealed in an 18-pin cerdip package and specified over the full military temperature range (-55°C to 125°C). The 1802s are sealed in a 40-pin side brazed package with guaranteed performance characteristics over the industrial temperature range (-40°C to 85°C).

Some of the devices used in the subsequent experiments and demonstrations had a history of prior environmental stress and accelerated temperature aging. However, the prior test history of devices in no way adversely affected the results obtained during this program.

Table 3-1 shows the number of devices allocated for each activity. Note that in addition to the devices used in the experiments/simulations and demonstration tests, five unstressed devices were assigned as "controls" to verify the automated test system stability.

3.2 INITIAL INSPECTIONS AND TESTS

External visual inspections of the 6504s and 1802s were performed to check device type, package style, lead finish, and markings. We then examined each device at 10X magnification for damage to the package, package seals, and leads, per MIL-STD-883, Method 2009. All devices were satisfactory.

Following the visual inspections, we subjected all 6504s and 1802s to hermeticity testing according to MIL-STD-883, Method 1014, Conditions A1 and C2.

TABLE 3-1. PROGRAM ACTIVITY DEVICE ALLOCATION

ACTIVITY	QUANTITY/PART TYPE	
	6504	1802
CONTROL GROUP	5	5
EVALUATION/REFINEMENT	30	30
DEMONSTRATION TEST	25	25
TOTAL	60	60

For the 6504s, we changed the failure criteria of the military standard to accept a *high fine-leak rate* ($>5 \times 10^{-8}$ cc/sec) as well as an apparent "fizzing" from the package seal area during the gross leak tests. The 6504 device manufacturer used a porous glass lead seal that trapped helium/fluorocarbon during hermeticity testing, and subsequently caused a "fizzing" that stopped after a few seconds (Reference 3). All 6504s passed the leak tests with the changed failure criteria.

All 1802s passed the fine leak test, but a single part (S/N 35) failed the gross leak test. The S/N 35 part later passed initial electrical tests and was used for demonstration testing to increase the probability of having a failure during the demonstration test.

3.3 INITIAL ELECTRICAL TESTS

Initial electrical tests consisted of the Group A inspections of the MIL-M-38510/239 (6504) and /470 (1802) specifications with exceptions as listed in Appendix B. Sixty devices of each part type were subjected to initial electrical testing at 25°C, 125°C, and -55°C. All 6504s passed the tests. However, five 1802s failed various parameters (such as I_{DD}, I_{OH}, I_{IH}, or V_{IC} at 25°C, 125°C, or -55°C) and were used only in experiments or simulations.

4.0 STAGE II: EVALUATION AND REFINEMENT OF THE BASIC CONCEPT

A review of the parallel test technique as described in Reference 1 indicated that the following questions needed to be addressed:

1) What features are required in the fault-current detector?
2) How should failed devices be identified?
3) Are latch-up, noise, or damage due to excessive fault currents problems in parallel testing? If so, how can these problems be minimized or eliminated?
4) What is the optimum number of devices that can be tested in parallel?
5) How do clock rate and temperature affect the other test conditions? What are the clock rate and temperature limitations on parallel testing?

These questions and resulting refinements to the basic concept discussed in Section 2.0 are addressed in the next section. In the course of evaluating the various factors in parallel testing, exercise patterns were established and values were selected for clock rate, test temperature, support hardware such as resistors and capacitors, and voltage levels for the demonstration test. The selected test conditions are summarized in Section 4.2.

4.1 AREAS IDENTIFIED FOR FURTHER EVALUATION

The following areas were identified for evaluation: current detectors, failed device identification, latch-up, noise, potential device damage, number of parallel devices on test, failure simulations, current and voltage limiting, background current as a function of clock rate, background current as a function of temperature, and temperature effects on source and sink output current. These evaluations were not completely independent nor were they conducted in the order presented. For these reasons, test conditions are listed for each experiment conducted in the evaluations.

Before proceeding with the evaluations or discussing refinements to the basic concept, it will be helpful to establish a structure for subsequent discussions. Such a structure is provided in the parallel test circuit of the

previous Figure 2-1. The basic manner in which parallel testing is performed was briefly described in Section 2. Additional aspects of parallel testing now need to be introduced, including the input driver (Figure 2-1) and methods of failed device identification.

The input driver provides the functional test patterns at the selected clock rate and signal levels. The driver can also be instantaneously halted by a current detector signal. Thus, the current detector senses a fault condition and signals the driver to "halt" and retain the input conditions which resulted in the fault. The failed device will source or sink currents different from good devices and may therefore be isolated by measuring the drain and source currents on every device.

Measuring the individual device drain and source currents may be rapidly performed by measuring the voltage across current sensing resistors (R_{DD} and R_{SS} in Figure 2-1) using an automated system. Our Dynamic Life Test System (DLTS) described in Appendix C is capable of performing this function. The DLTS is an 8080 microprocessor based system designed to exercise and continuously monitor microcircuits undergoing burn-in or life testing. In addition, the DLTS is capable of measuring all the current sensing resistor voltages and processing the measured voltages with a software routine to identify the failed device.

The next section describes the current detector evaluations.

4.1.1 Current Detector Evaluation

The purpose of the current detector is to accurately detect faults (abnormal current levels) and generate an alarm when faults occur. Faults must be detected rapidly in order to generate the "halt" signal sufficiently fast to stop the driver while the inputs are still in the state that resulted in the fault. The current detector is required to perform this fault detection function at clock rates of interest, to have sufficient threshold stability and noise immunity to avoid excessive false alarms, and have minimum impact on the circuits being measured. Minimal current sensing resistor values are desirable to avoid large V_{DD} voltage transients due to current switching transients. Latch-up may occur if the voltage

transient lowers the V_{DD} voltage below the input voltage. The current detector must also be capable of triggering if the current either exceeds a maximum threshold or falls below a minimum threshold. In addition, the thresholds must be easily adjustable to allow for flexibility in the selection of items which affect the error-free background current, such as clock rate, temperature, and device type.

Our initial current detector requirements were as follows:

Clock Rate	100 Hz to 1 MHz
Stability	100 uA over 200 hours
Upper Current Threshold Limit	62.5 mA
Lower Current Threshold Limit	100 uA

This section discusses the evaluation of four current detectors, including: the baseline detector (Reference 1), two types of level/window (comparator) detectors, and an operational amplifier detector. Also, a Hall effect device was evaluated as a means of eliminating the current sensing resistor (R_{PS}) and its associated undesirable effects.

The operational amplifier window detector was selected for this program because it came the closest to meeting all the requirements. Its primary disadvantage was that it required a current sensing resistor with attendant switching transient noise and latch-up potential. Noise and latch-up potential can be minimized by optimizing the choice of the current sensing resistor value. Refinements were added to the operational amplifier detector to provide finer threshold adjustments and to prevent triggering on switching transients.

The baseline current detector, shown in Figure 4-1, was designed to discriminate between microamperes of background current and milliamperes of fault current. This detector works satisfactorily for devices when the background current is in the microampere range. However, at higher clock rates the background current is large enough to trigger the detector. For example, the background current for the 6504s and 1802s will be approximately 1 mA per device at 200 KHz (measurements discussed in Section 4.1.9), which is multiplied by the number of devices in

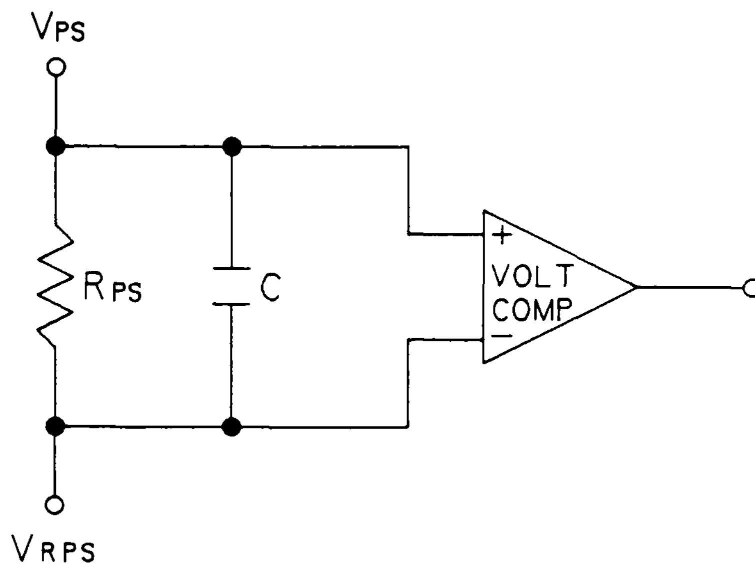


FIGURE 4-1. BASELINE CURRENT DETECTOR

parallel at the detector. Further, the baseline detector could not detect a reduction in background current and hence could not respond to an open V_{DD} line. Therefore, since the baseline detector had a nonadjustable threshold and could not detect a decrease in current, it was eliminated from further consideration.

The level detector, shown in Figure 4-2, provides the capability for adjustable threshold levels and thus allows for higher background current. Also, by using two level detectors as a window detector (Figure 4-3), an alarm can be generated if the V_{RPS} voltage level is outside the preset threshold levels (V_1 and V_2). The problems with this detector were that the thresholds were not sufficiently stable and the detector was highly susceptible to false triggering from noise. The two level detector also has the inherent problem associated with a current sensing resistor, i.e., the large switching transients that could cause latch-up.

The operational amplifier window detector shown in Figure 4-4 was more stable and had a higher noise immunity than the two comparator detector (Figure 4-3). The operational amplifier window detector provides for setting the high comparator (Hicomp) threshold level and then setting the window width to obtain the low comparator threshold level. The detector operates as follows: The variable resistor voltage of the Hicomp is adjusted so that the output of U1 (Operational Amplifier 1) changes polarity when the algebraic difference between the V_{RPS} voltage and the Hicomp voltage changes sign. Positive or negative feedback occurs through diode D_1 or D_2 to maintain the negative input terminal of U1 at or near ground potential. The second operational amplifier determines whether the output of the first operational amplifier has changed polarity and whether it exceeds the window-width setting. When the input is more positive than the Hicomp voltage level, a negative output of U1 controls U2 (Operational Amplifier 2) through steering diode D_2 to cause the output of U2 to be negative. When the polarity change occurs, U2 switches its output level from negative to positive. U2 remains positive until the output of U1, through the steering diode D_1, exceeds the window-width setting. U2 then reverts to its negative value. The operational amplifier detector met all of our requirements and had a higher noise immunity than the simple comparator detector. However, this detector also requires a current sensing resistor with its accompanying undesirable potential for noise-induced latch-up.

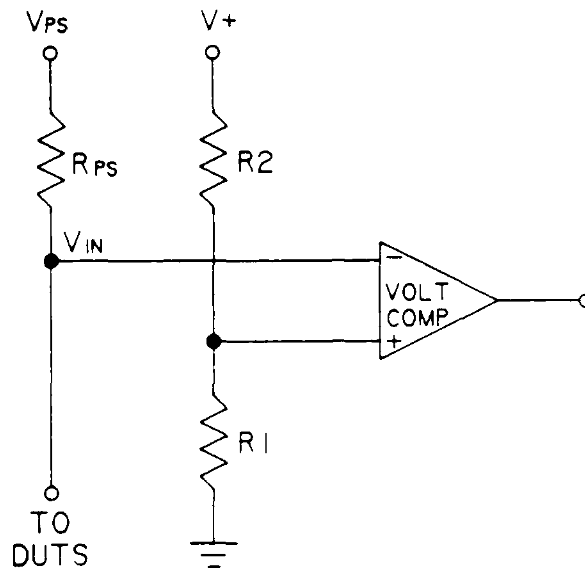


FIGURE 4-2. LEVEL (COMPARATOR) DETECTOR

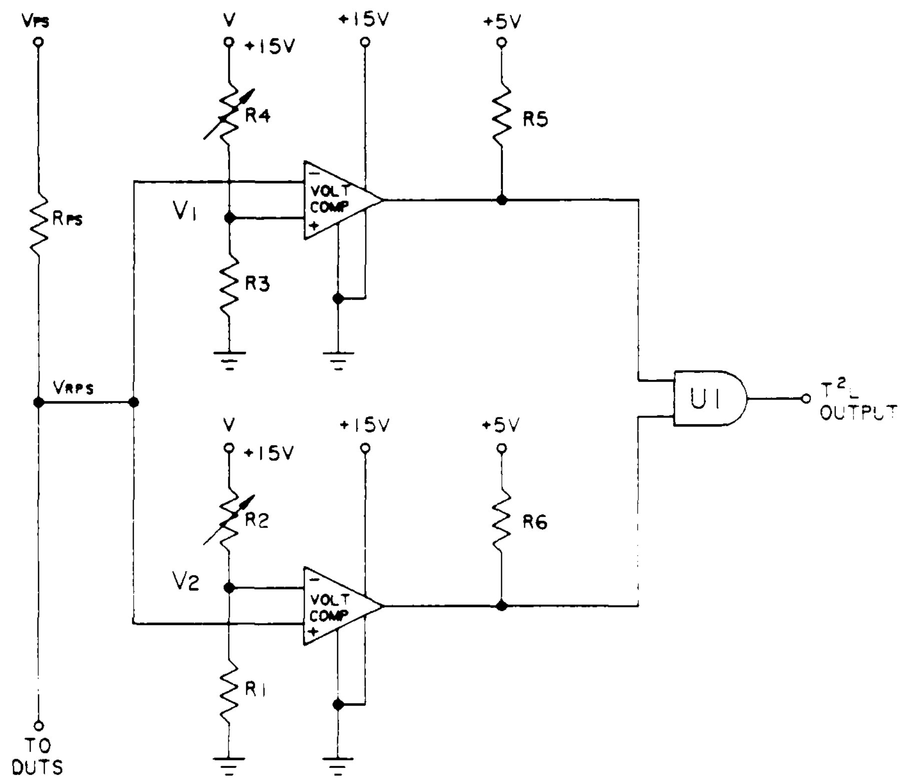


FIGURE 4-3. INITIAL WINDOW (COMPARATOR) DETECTOR

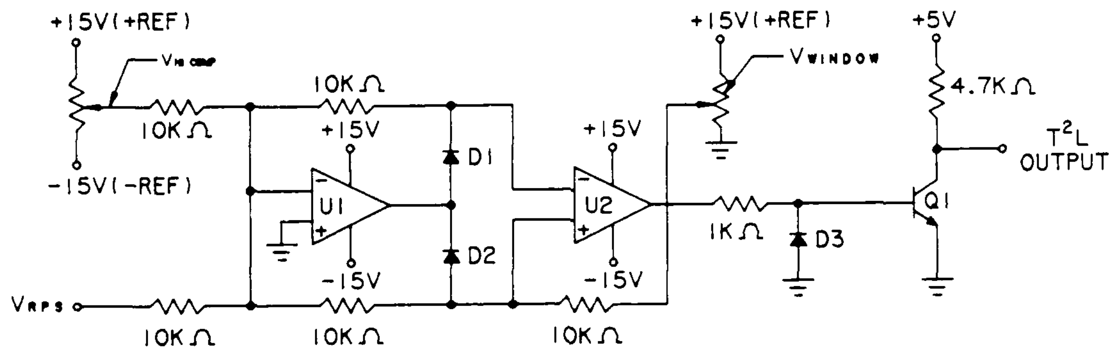
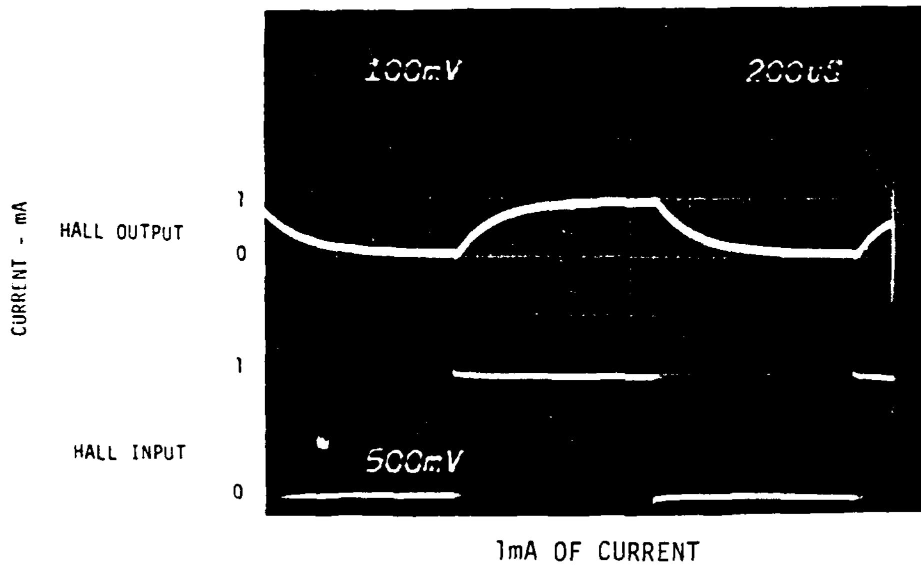


FIGURE 4-4. OPERATIONAL AMPLIFIER WINDOW DETECTOR

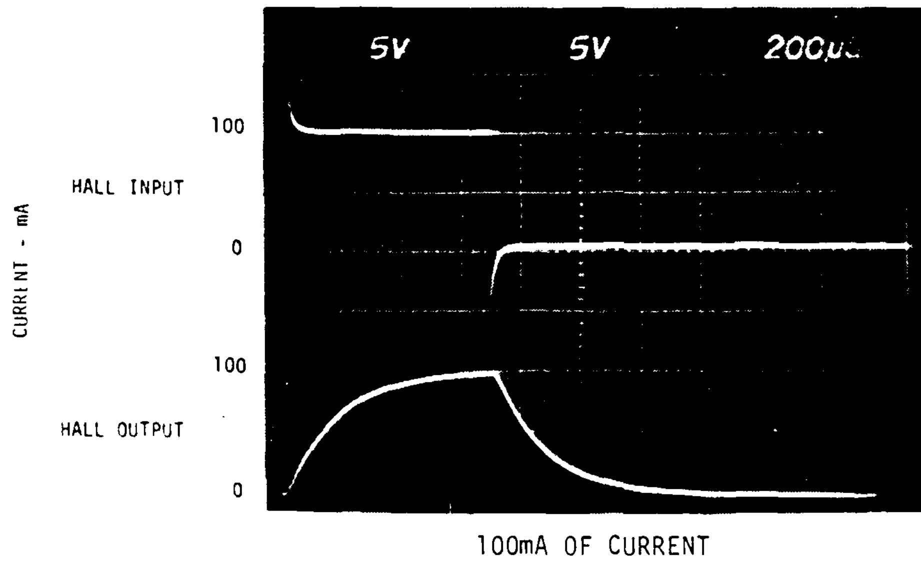
We also evaluated a Hall effect sensor to eliminate the current sensin resistor and its associated undesirable effects. Our survey of Hall effect sensor manufacturers disclosed that only F. W. Bell produced a device whose current range met our requirement (100 uA to 62.5 mA). The IL-150 1A devic detects dc or ac currents in the 100 mA range. All other manufacturers mak sensors for high current (10 A - 1000 A) applications. However, the F. W. sensor was too slow, and could successfully operate only at clock rates bel 500 Hz. As shown in Figure 4-5, settling times of 400 us and 600 us were r for the Hall effect sensor to reach its final value following respective st changes of 1 mA and 100 mA in the sensed current. The upper frequency limi 500 Hz was derived from the measured response time. Consequently, despite desirable features, the Hall effect device was eliminated from further cons ation because of its inadequate frequency response.

As previously stated, the operational amplifier window detector shown Figure 4-4 was selected as the best compromise of all the current detectors evaluated because it has most of the desired features. Subsequently, three refinements were made to this window detector to improve testing effectiven and to aid in troubleshooting. The refinements, as depicted in the 6504 an current detectors shown in Figures 4-6 and 4-7, included the capability to: 1) mask the current detector output, 2) manually halt the driver, and 3) fi tune the comparator voltage levels. The first two refinements are closely related to features of our Dynamic Life Test System; however, the three cap bilities should be generally applicable in any parallel test implementation

The capability to mask the current detector output was added so that t drivers would not be halted under three conditions. First, to prevent dete triggering on transition noise spikes from halting the driver, an ERROR PUL signal was provided to mask the detector output during input transitions. Second, to allow completion of a functional pattern, the HALT DISABLE signa provided to mask the detector output from the time the driver is halted unt the next cycle. Finally, the DLTS MASK WINDOW DETECTOR signal was provided that the driver would not operate in an essentially static state which woul exist if one DUT continuously failed (See Appendix C for details). An esse tially static state can occur because the time to run a functional test pa is much shorter than the time for the Dynamic Life Test System to isolate failed device.

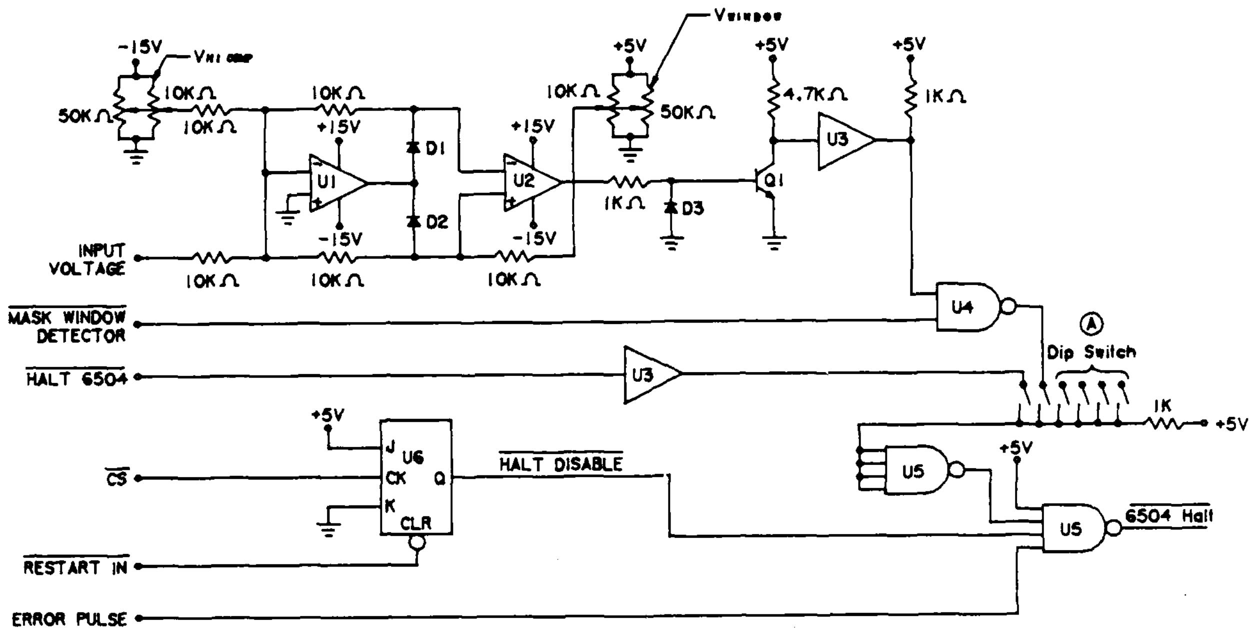


1mA OF CURRENT



100mA OF CURRENT

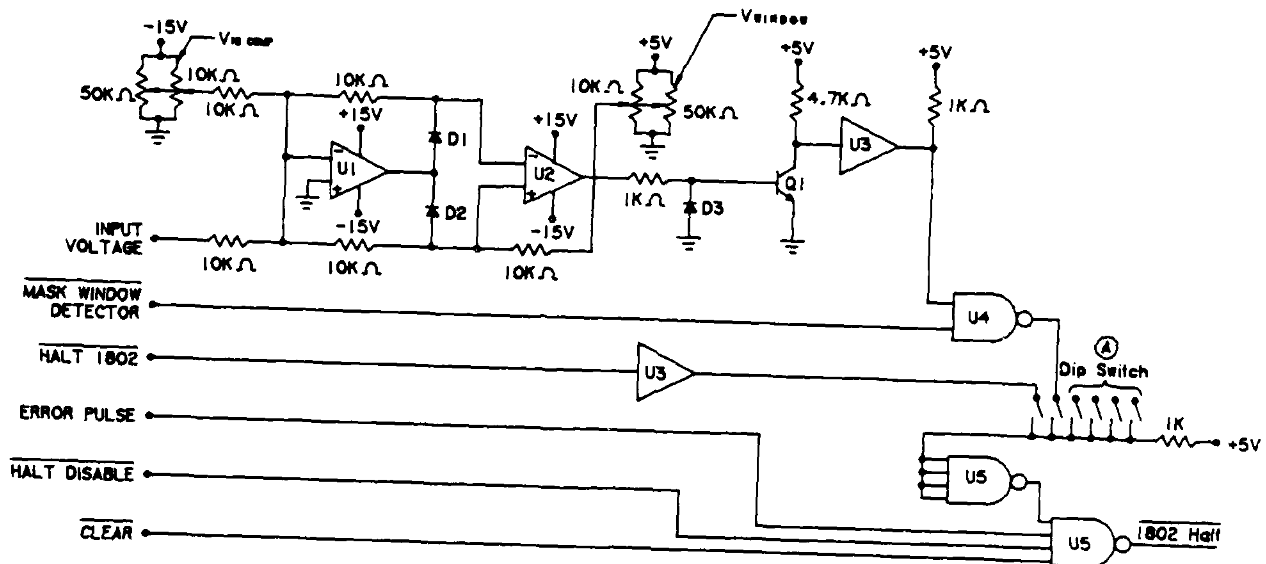
FIGURE 4-5. HALL DEVICE RESPONSE TIME



CIRCUIT DESIGNATION	PART NUMBER
U1, U2	OP-15
U3	7407
U4	7403
U5	7420
U6	7473
D1, D2, D3	IN914
Q1	2N2222

(A) OUTPUT FROM THE OTHER 4 CURRENT DETECTORS ARE CONNECTED TO THE OTHER POSITIONS OF THE DIP SWITCH.

FIGURE 4-6. 6504 ENHANCED CURRENT DETECTOR CIRCUITRY



CIRCUIT DESIGNATION	PART NUMBER
U1, U2	OP-15
U3	7407
U4	7403
U5	7420
D1, D2, D3	IN914
Q1	2N2222

(A) OUTPUT FROM THE OTHER 4 CURRENT DETECTORS ARE CONNECTED TO THE OTHER POSITIONS OF THE DIP SWITCH.

FIGURE 4-7. 1802 ENHANCED CURRENT DETECTOR CIRCUITRY

The ability to manually halt the driver was also added to the basic window detector to establish the no-fault voltage levels for use in the fault isolation software. The fault isolation software uses the no-fault voltage levels to quickly determine that a "false halt" has occurred without searching for a failed DUT. The capability of the system to determine that a false halt has occurred without performing a search for the failed DUT reduces the fraction of test time that devices are in a static or halted condition due to noise-induced false halts.

Fine tuning for the comparator voltage levels was needed to allow adjustment of the current threshold to within ± 10 uA. This capability was provided by altering the configuration of the window current detector. A 50K ohm variable resistor was placed in parallel with each 10K ohm variable resistor. Then the V_{Hicomp} +15V supply point was set to ground to increase the resolution of V_{Hicomp}. Also, the V_{WINDOW} +15V supply was reduced to 5V to increase the V_{WINDOW} voltage resolution. In addition, a switch was added between the current detector outputs and the HALT signal to aid in setting the comparator voltage levels. The switch prevents halting by other detectors and helps isolate hardware problems by isolating the detector output.

4.1.2 Failed Device Identification

The parallel testing technique must include a way to isolate failed devices economically when failures occur. Two techniques were evaluated for this purpose. The first technique (Figure 4-8) utilizes two current detectors per device, one to detect an abnormal drain current (I_{DD}) and one to detect an abnormal source current (I_{SS}). The second technique (Figure 4-9) is fundamentally the same as the baseline concept described in Section 2. It utilizes one current detector for several devices in parallel (a matrix). A "smart" system (such as our Dynamic Life Test System) is then used to isolate the failed device by making individual device current measurements.

The second technique (single-detector-per-matrix) was selected for this study primarily because of hardware simplicity compared to the other technique (two-detector-per-device) and because it could isolate a larger number of faults and fault combinations.

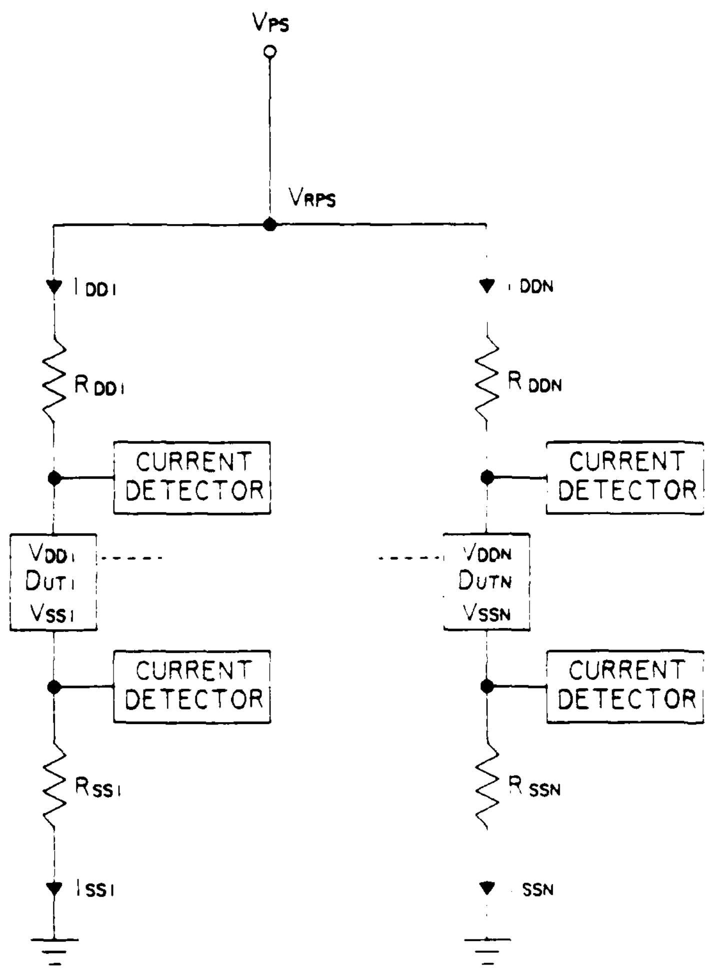
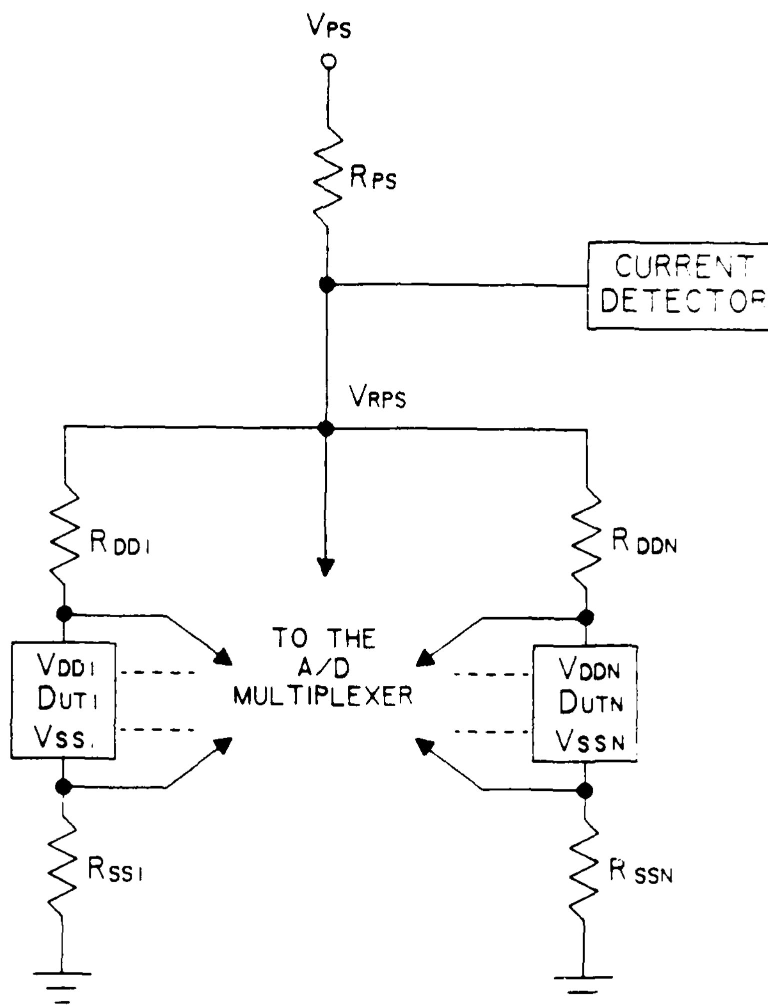


FIGURE 4-8. TWO-DETECTORS-PER-DUT PARALLEL TEST CONCEPT



NOTE: CORRESPONDING INPUTS AND OUTPUTS ARE PARALLELED

FIGURE 4-9. ONE-DETECTOR-PER-MATRIX PARALLEL TEST CONCEPT

The two-detectors-per-DUT technique operates as follows. If all devices are operating normally and corresponding outputs agree, then the I_{DD} and I_{SS} currents fall within a normal range which depends on clock rate, ambient temperature and supply voltage. If one device fails such that one of its outputs is different from the corresponding outputs of the other parallel devices, it will sink or source an abnormal current. The I_{DD} or I_{SS} current detector for the failed device instantaneously detects the abnormal current and provides an output signal to note this fact.

Further details of the operation of the two-detectors-per-DUT method are illustrated in Table 4-1. The voltage at V_{DD} and V_{SS} for five parallel devices with various output stuck conditions are listed in Table 4-1. (Note that the V_{DD} operating voltage with no monitor error was set at 11.0 Vdc.) The detector at V_{DD} has its upper threshold set to 10.0 volts, and under conditions of a single stuck-at-zero (S-A-0), two S-A-0s, or one S-A-0 and one stuck-at-one (S-A-1), all five DUTs trip the 10 volt threshold setting. The additional information from the I_{SS} detectors is required to isolate the failed device.

The primary advantage of the two-detectors-per-DUT technique is its ability to isolate a failed DUT instantaneously, while its primary disadvantages are hardware complexity, high cost, and inability to isolate all failures. Because two detectors per DUT are required, a 50-device test capacity would require 100 detectors (at an estimated hardware cost of $60.00 per detector). The inability of this technique to isolate all combinations of functional failures can be concluded from the experimental data of Table 4-1 discussed earlier. Note the example in Table 4-1 where two devices fail in opposite states. The S-A-1 device does not have V_{DD} and V_{SS} levels sufficiently different from the corresponding levels for nonfailed devices to be detected by exceeding upper or lower current thresholds. The additional logic required for the two-detector-per-DUT method to isolate failed devices is a major disadvantage.

The one-detector-per-matrix concept (Figure 4-9) operates as follows. A halt signal from the detector instantaneously halts the driver due to an abnormal current at V_{RPS} (the DUTS are stopped in the state that the fault occurred). Next, the DLTS measures the V_{DD} and V_{SS} voltages of each DUT and processes

TABLE 4-1. 1802 V_{DD} AND V_{SS} VOLTAGE LEVELS DURING S-A-0 AND S-A-1 CONDITIONS AT 125°C

CONDITIONS	VOLTAGES	DUT IN THE MATRIX				
		1	2	3	4	5
1 S-A-0	V_{DD} (V)	9.13	8.95	8.94	9.00	8.94
	V_{SS} (mV)	273	38	44	39	40
1 S-A-1	V_{DD} (V)	9.75	10.96	10.96	10.96	10.96
	V_{SS} (mV)	28	38	32	32	39
1 S-A-1 and 1 S-A-0	V_{DD} (V)	8.27	8.39	8.37	8.42	8.53
	V_{SS} (mV)	53	64	68	65	207
2 S-A-0s	V_{DD} (V)	8.44	8.24	8.22	8.47	8.21
	V_{SS} (mV)	176	45	54	157	49

NOTES:

V_{SS} IS UNDERLINED TO INDICATE THE S-A-0 DUT.

V_{DD} IS UNDERLINED TO INDICATE THE S-A-1 DUT.

TEST CONDITIONS APPLY TO FIGURE 4-20

THE V_{DD} CURRENT DETECTOR LOCOMP VOLTAGE LEVEL = 10.V (THE DETECTOR TRIGGERS IF V_{DD} < 10.0V).

THE V_{SS} CURRENT DETECTOR HICOMP VOLTAGE LEVEL = 100 mV (THE DETECTOR TRIGGERS IF V_{SS} > 100 mV).

V_{DD} (NO ERROR OPERATING VOLTAGE) = 11.0V.

R_{PS} = 51 OHMS, R_{DD} = 1K OHMS, AND R_{SS} = 100 OHMS.

C_{PS} = .033 μF AND C_{SS} = .01 μF.

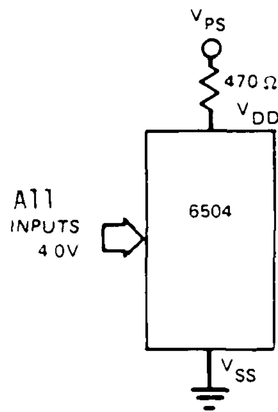
V_{IH} = 11.0V.

the data through a software routine to identify the failed device. The ability to analyze the measured V_{DD} and V_{SS} levels by an automated system allows all single and most multiple faults to be isolated. Failures are also distinguishable as a S-A-0 or a S-A-1 by this method. Although the two-detector-per-DUT method has the advantage of speed, the one-detector-per-matrix method has the advantages of less hardware complexity, reduced cost, and more comprehensive failed device isolation capability. Therefore, the one-detector-per-matrix method was selected as the best compromise between effectiveness and hardware cost.

4.1.3 Latch-Up

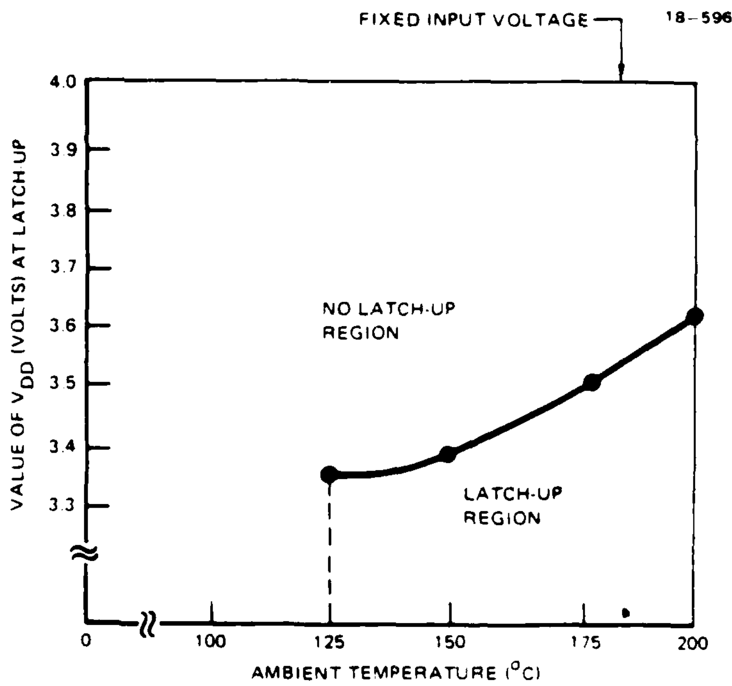
CMOS devices are known to have a tendency toward latch-up (Reference 4). A device in this condition could be destroyed by excessive currents or cause other testing problems. It was therefore considered necessary to characterize the 6504 and 1802 devices for latch-up to avoid the conditions that cause it. Two static experiments were performed for the 6504s and a static and a dynamic experiment was performed for the 1802s. One 6504 experiment determined as a function of temperature the amount V_{DD} could fall below the input high level (V_{IH}) without latch-up. The other 6504 experiment determined as a function of temperature the amount the input low level (V_{IL}) could be below V_{SS} without latch-up. The static 1802 experiment was similar to the 6504 test to determine allowable V_{DD} levels with respect to V_{IH}. No 1802 latch-up occurred in the static test, so a dynamic test was performed. Again, no latch-up occurred. However, after test conditions were established for the demonstration test, 1802 latch-up did occur. Additional 1802 experiments were then performed to eliminate the latch-up. Latch-up prevention for the 6504 was straightforward and made use of the experimental results presented below. Latch-up prevention for the 1802s was also easily accomplished but required undesirable changes in the demonstration test conditions.

6504 Latch-Up Experiments - The first 6504 experiment was designed to measure as a function of temperature the amount V_{DD} could fall below V_{IH} without latch-up. To obtain this data, all inputs of a single device were held at 4.0 Vdc and V_{DD} was slowly lowered as shown in Figure 4-10A until the onset of latch-up was observed as a sudden decrease of V_{DD} to approximately 2.0 Vdc. The results are shown in Figure 4-10B. It is noted in Figure 4-10B that the amount V_{DD} may drop below V_{IH} without latch-up is about 0.6 volts at 125°C and decreases to less than 0.4 volts at 200°C.



V_{PS} CONNECTED TO THE CHANGING POWER SUPPLY

A) CIRCUIT DIAGRAM



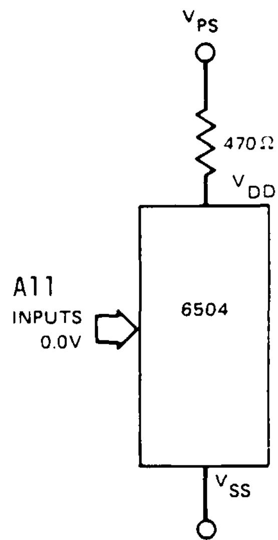
B) LATCH-UP RESULTS

FIGURE 4-10. 6504 LATCH-UP AS A FUNCTION OF V_{DD} AND AMBIENT TEMPERATURE

Another experiment was performed on the 6504 to determine as a function of temperature the amount V_{SS} could be above V_{IL} without latch-up occurring. For this experiment, all inputs of a single device were held at 0.0 Vdc (Figure 4-11), and V_{PS} was adjusted to yield a V_{DD} value of 5.5 Vdc with V_{SS} equal to 0.0 Vdc. V_{SS} was then raised in 100 mV increments from 0.0 Vdc to 1.0 Vdc, and V_{DD} was measured at each value of V_{SS}. The results are shown in Table 4-2. Note that V_{DD} drops when V_{SS} exceeds the input voltage even though latch-up has not occurred. (The fact that latch-up did not occur was indicated by V_{DD} returning to 5.5 Vdc when V_{SS} was decreased to zero, without removal of V_{PS}.) Under normal operation, the input signals would consist of levels between zero and 4.0V. If the background level of V_{SS} were higher than V_{IL}, the background level of V_{DD} could drop below V_{IH} and result in latch-up. These conditions could occur for multiple-input devices where inputs may be at combinations of low and high levels. The results of Table 4-2 were combined with the results of Figure 4-10B to obtain the maximum value V_{SS} can exceed the input low voltage level without latch-up. This computed value of (V_{SS} - V_{IL}) for no latch-up is provided in Figure 4-12. Note in Figure 4-12 that the amount V_{SS} can exceed V_{IL} decreases from about 0.6 volts at 125°C to about 0.4 volts at 200°C.

The latter result concerning allowable V_{SS} levels with respect to V_{IL} was not needed for establishing demonstration test conditions, because it was later determined that 6504 S-A-0 faults could be isolated by using only the V_{DD} levels. Therefore, a current sensing resistor (R_{SS}) was unnecessary. However, the results of the former experiment indicated that latch-up on the 6504 could be prevented by insuring that the input voltages never exceeded V_{DD} by 0.5V or more.

Several drive networks (Figure 4-13) were evaluated for the 6504 to insure that the DUT input voltages not exceed V_{DD} to avoid latch-up. Our final selection (Figure 4-13C) for the drive network minimizes false triggering of the current detector, and maintains driver operation if a DUT input shorts to ground. In addition, there are no space constraints of adding components to the driver board.



V_{SS} CONNECTED TO THE CHANGING POWER SUPPLY

FIGURE 4-11. TEST CIRCUIT FOR 6504 LATCH-UP AS A FUNCTION OF V_{SS}

TABLE 4-2. V_{DD} VS. V_{SS} FOR GROUNDED INPUTS AS A FUNCTION OF TEMPERATURE

V_{SS}	V_{DD}				
	25°C	125°C	150°C	175°C	200°C
0 mV	5.51 V	5.51 V	5.51 V	5.51 V	5.51 V
100 mV	5.51 V	5.51 V	5.51 V.	5.52 V	5.51 V
200 mV	5.51 V	5.51 V	5.51 V	5.51 V	5.47 V
300 mV	5.51 V	5.50 V	5.47 V	5.37 V	5.13 V
400 mV	5.51 V	5.33 V	5.15 V	4.77 V	4.12 V
500 mV	5.51 V	4.60 V	4.04 V	3.56 V	2.78 V
600 mV	5.35 V	3.33 V	2.64 V	2.00 V	0.71 V
700 mV	4.64 V	1.70 V	1.15 V	0.83 V	0.72 V
800 mV	2.91 V	0.65 V	0.64 V	0.67 V	0.71 V
900 mV	1.25 V	0.63 V	0.67 V	0.72 V	0.76 V
1000 mV	0.55 V	0.67 V	0.73 V	0.78 V	0.82 V

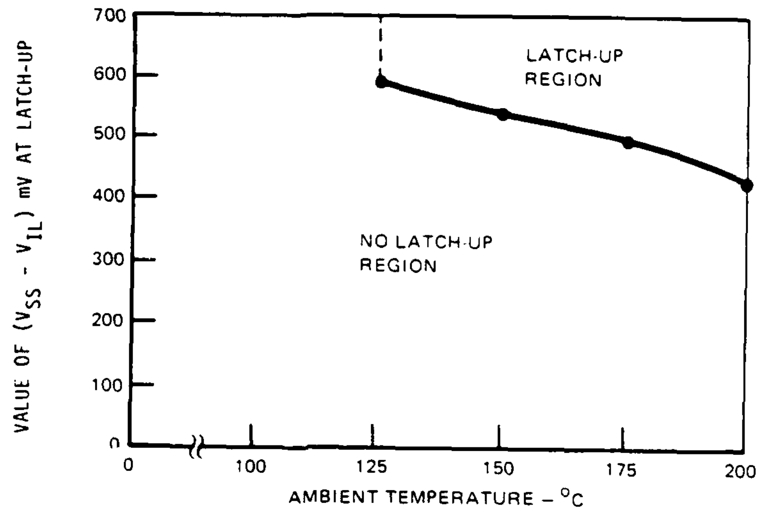
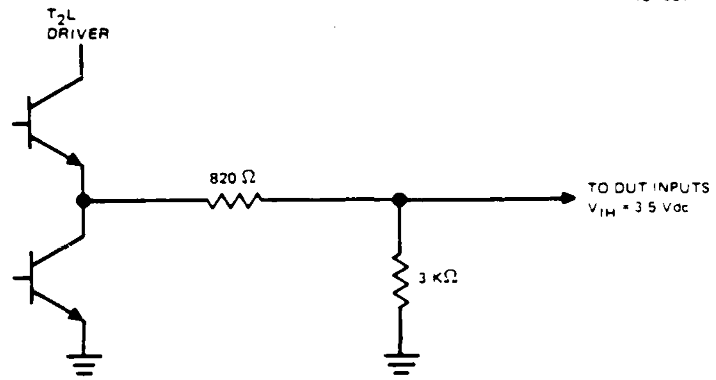
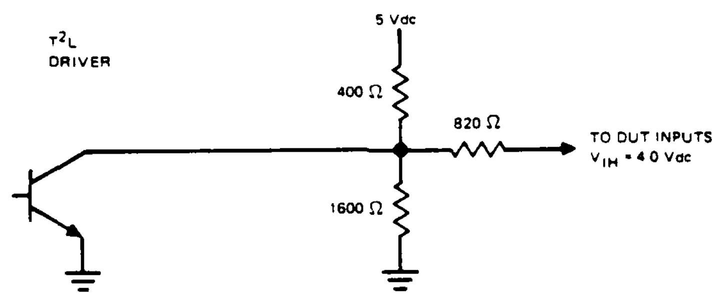


FIGURE 4-12. 6504 LATCH-UP AS A FUNCTION OF V_{SS} AND AMBIENT TEMPERATURE

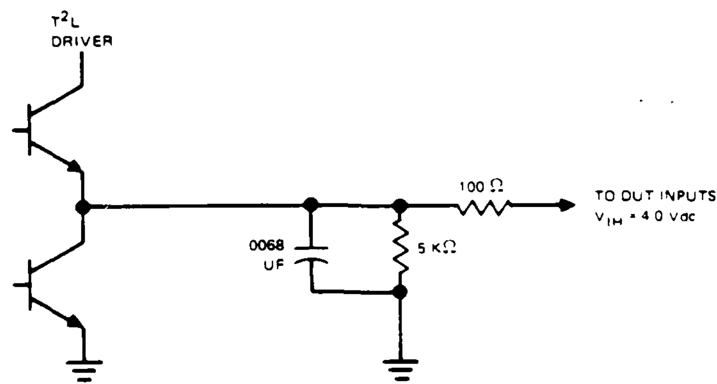
18-681



A) TOTEM-POLE DRIVE NETWORK



B) OPEN-COLLECTOR DRIVE NETWORK



C) SELECTED DRIVE NETWORK

FIGURE 4-13. 6504 DRIVE NETWORK USED TO REDUCE THE POSSIBILITY OF LATCH-UP

Initially, in evaluating the input networks to prevent 6504 latch-up, the main concern was to guarantee that at least 3.5 Vdc was available at the DUT inputs. However, preliminary experiments showed that the Figure 4-13A circuit was not acceptable because noise at the current detector (V_{RPS}) consistently caused the detector to falsely trigger. Although the manufacturer guarantees proper operation with the input voltage at 3.5 Vdc, we conservatively estimated that 4.0 Vdc was required for the parallel test application. As a result we evaluated the Figure 4-13B input network circuit. This circuit provides satisfactory results but requires additional space because it requires open collector driver outputs as well as the load resistors. Therefore, because the input network of Figure 4-13C provided satisfactory operation and did not pose a board space problem, it was selected for the demonstration test.

1802 Latch-Up Experiment - Latch-up on 1802s was investigated by performing an experiment similar to the first 6504 experiment to determine the amount V_{DD} could be below V_{IH} without latch-up. The static experiment was performed using the test setup of Figure 4-14 by providing a fixed buffered input voltage V_{IH} at 10.0 Vdc and slowly reducing the supply voltage below V_{IH}. No latch-up occurred at any temperature, and the largest difference between V_{IH} and V_{DD} was approximately 0.7V. This is a result of current flow from inputs to V_{DD} through forward biased diodes of the input protection network.

A dynamic test was then performed with the same result--no latch-up. The dynamic experiment was performed with the following test conditions: the high input voltage (V_{IH}) level was set to 10.0V with the ambient temperature at 200°C and the 1802 clock (Pin 1) of 1 MHz. V_{DD} was then slowly lowered. Latch-up was to be noted as a sudden voltage drop in the supply line to about 3V, but no latch-up occurred.

As noted earlier, 1802 latch-up did occur after the initial demonstration test conditions were established. The initial demonstration test conditions which resulted in 1802 latch-up were the combination of high ambient temperature (200°C), long clock cycle time (80 us), certain input sequences (idle instruction), both V_{DD} and V_{IH} set to the same level (11.0 volts), and a large value for the R_{DD} resistor (1000 ohms). Under these test conditions, a large voltage ripple appeared on V_{DD} and the magnitude of the ripple was significantly larger during the idle

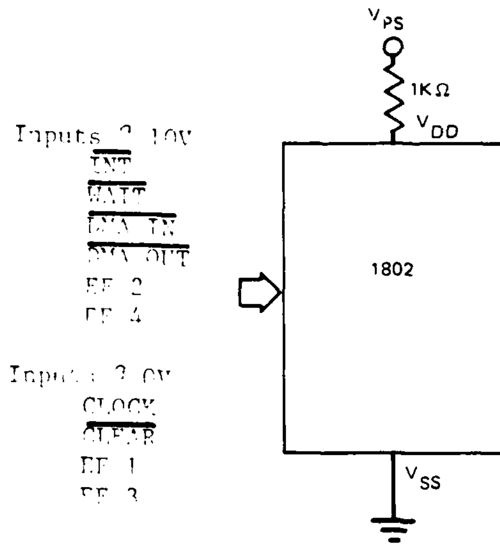


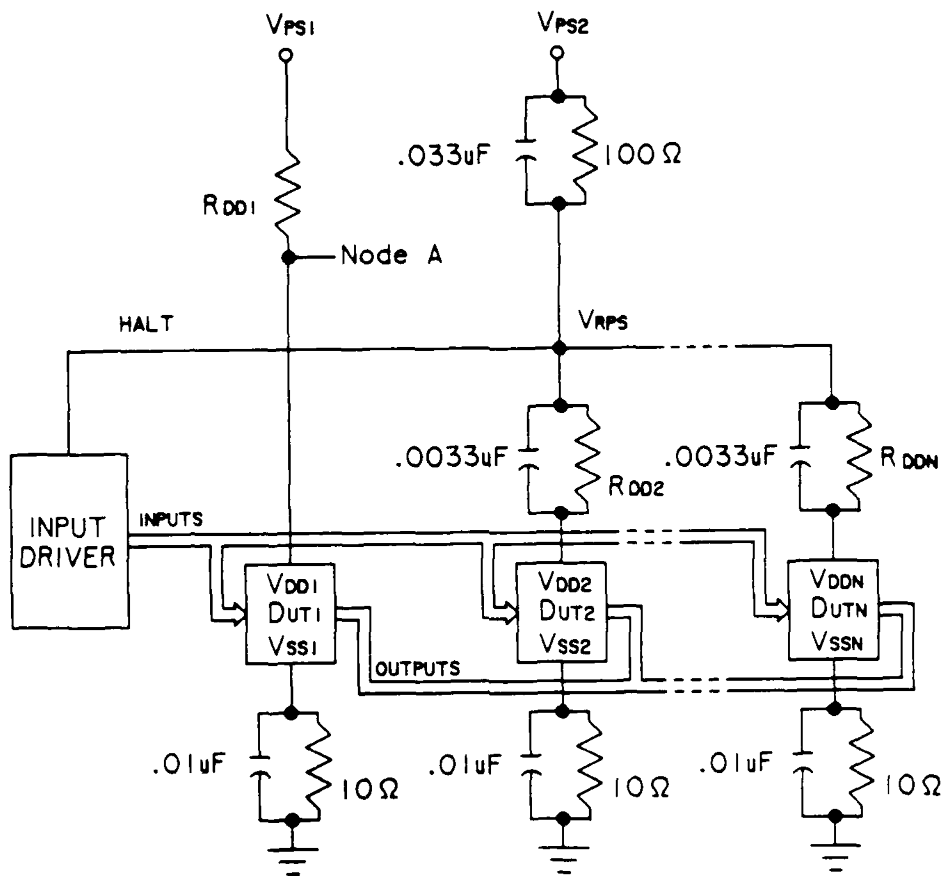
FIGURE 4-14. 1802 CIRCUIT USED DURING THE LATCH-UP EXPERIMENTS

instruction. Experiments were performed to eliminate the latch-up by lowering the ambient temperature, reducing V_{IH} to a level below V_{DD}, reducing the value of R_{DD}, and eliminating the input sequence which caused the largest switching currents (idle instructions). Values of these parameters which assured no latch-up were: 125°C ambient temperature, V_{IH} set to 10.0 volts, V_{DD} set to 11.0 volts, an R_{DD} value of 100 ohms, and elimination of the idle instruction. These changes worked for error-free operation, and provided the ability to detect one S-A-0 and one S-A-1.

4.1.4 Noise

Noise is an important issue in the parallel test technique because it can cause faulty operation or be the source of momentary signal levels that provide the conditions for latch-up. Four sources of noise were investigated: 1) output propagation delay mismatch, 2) V_{IH} signal level compared to V_{DD}, 3) voltage spikes on R_{SS} due to switching currents, and 4) noise as a function of clock rate. It was concluded from this investigation that: 1) noise due to propagation delay mismatches was not a problem for the 6504 and was easily controlled for the 1802, 2) the best V_{IH} level compared to V_{DD} was found to be a compromise between high values for low noise and low values for latch-up prevention, 3) voltage spikes on R_{SS} were large but easily controlled, and 4) noise was found to be constant as a function of clock rate. Details of the experiments performed that led to these conclusions are presented in the following paragraphs.

Propagation mismatch noise on the 6504 was anticipated to occur during output high-to-low transitions that commence 100 ns after chip enable goes low and that last approximately 80 ns. Variability in these transitions from device to device would be expected to cause some DUTs to sink or source a large current momentarily, conditions which would appear as a noise voltage at V_{DD}. To evaluate this hypothesis, the following experiment was performed at 25°C. A single device (DUT1, Figure 4-15) was operated from a separate power supply to eliminate background noise normally present at V_{RPS}. The bypass capacitor across the R_{DD} resistor connected to this single device was also removed to permit observation of the noise at the V_{DD} pin. The noise level present at the V_{DD1} pin (Node A, Figure 4-15) of this single device was noted when operated with no other devices in parallel. Then the noise level was noted when 22 additional devices were



NOTE: CORRESPONDING INPUTS AND OUTPUTS ARE PARALLELED
ALL R_{DDS} = 100Ω FOR THE 6504 AND 1000Ω FOR THE 1802

FIGURE 4-15. TEST CIRCUIT FOR EVALUATING PROPAGATION DELAY NOISE ON THE 6504 AND THE 1802

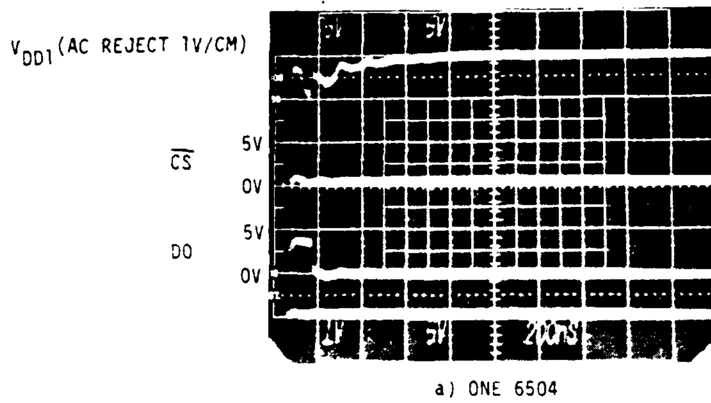
operated in parallel as shown in Figure 4-15. A comparison of the two oscilloscope photos shown in Figure 4-16 indicates that the increase in noise from one DUT to 23 DUTs in parallel is negligible. Thus, it is concluded that propagation delay mismatches should not be a major source of noise for the 6504 in parallel testing.

A similar experiment with 1802s using the same circuit (Figure 4-15) showed a small increase in noise due to propagation delay mismatches. The upper oscilloscope photo of Figure 4-17 indicates approximately 700 mV of switching noise at V_{DD} (Node A, Figure 4-15) for one 1802. The lower oscilloscope photo shows the slight increase in noise (about 100 mV) at V_{DD} when three other 1802s are added in parallel. If the increase in noise from this source is linear, it could be 800 mV for 25 DUTs in parallel. Although an 800 mV noise level is a concern for latch-up or proper device operation, additional capacitance across V_{DD} will easily reduce the noise to acceptable levels.

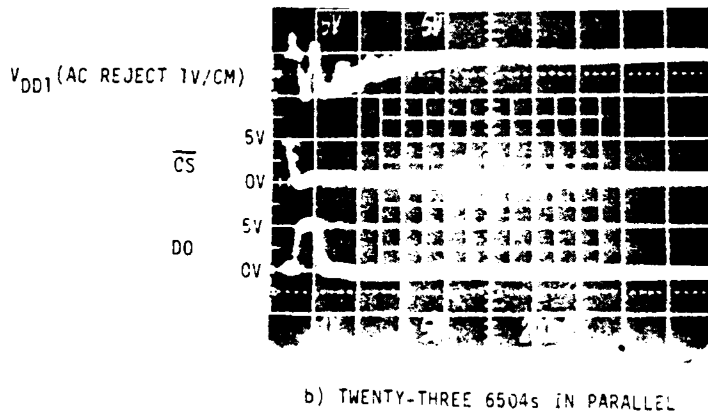
Subsequent to these findings, the circuit element (R_{DD}, R_{SS}, R_{PS}) values shown in Figure 4-15 were modified for other purposes, and experiments with up to 25 1802s in parallel did not indicate a need for capacitance across R_{DD}.

The second noise source investigated occurs when the input high level (V_{IH}) is significantly lower than the V_{DD} level. The magnitude of this noise source is important because the selected V_{IH} levels will be a compromise between high values for low noise and low values to reduce the probability of latchup.

An experiment with five paralleled 6504s with V_{DD} = 5.5 Vdc and ambient temperature at 25°C indicated I_{DD} noise levels of 260 uA peak-peak for V_{IH} = 4.0V, and 425 uA peak-peak for V_{IH} = 3.0 V. This noise resulted in false triggering of the current detector at the lower value of V_{IH}. Other experiments with five paralleled 1802s resulted in proper detector operation for $V_{IH} \geq$ 10.0V with V_{DD} set to 11.0 Vdc. A satisfactory compromise between noise-induced false current detector triggering and latch-up was achieved by setting the 6504 V_{IH} level to 4.0V with V_{DD} at 5.5 Vdc and setting the 1802 V_{IH} level to 10.0V with V_{DD} at 11.0 Vdc.

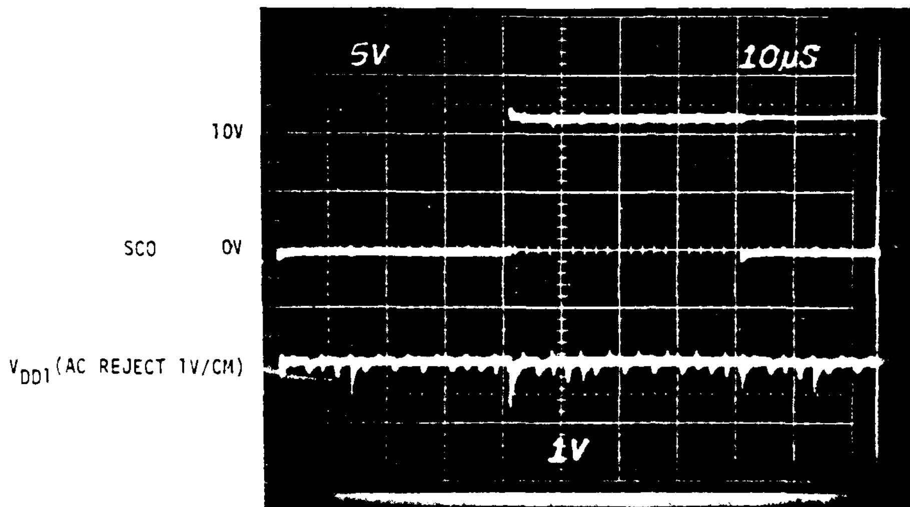


a) ONE 6504

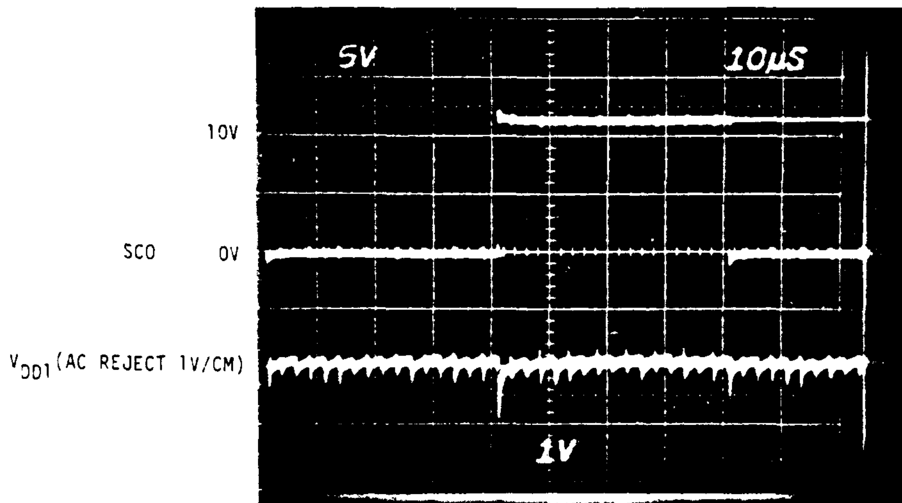


b) TWENTY-THREE 6504s IN PARALLEL

FIGURE 4-16. 6504 NOISE ON V_{DD} DUE TO INCREASED NUMBER OF DEVICES AT 125°C



a) ONE 1802



b) FOUR 1802s PARALLEL

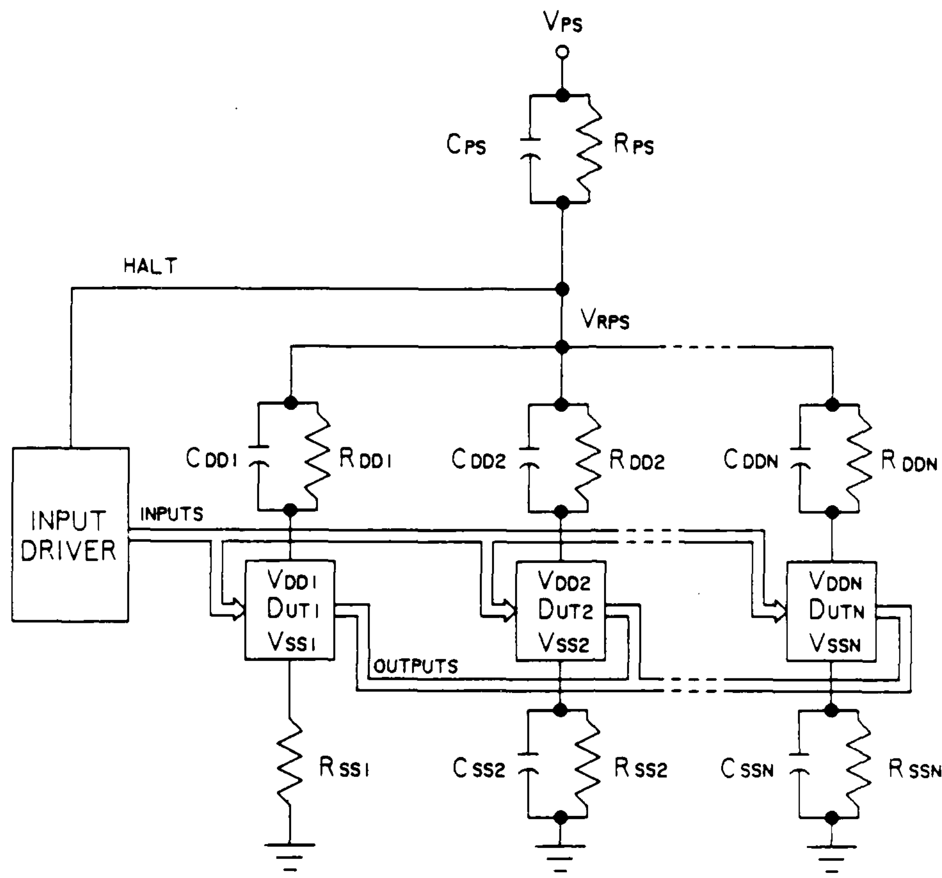
FIGURE 4-17. 1802 NOISE ON V_{DD} DUE TO PROPAGATION DELAY MISMATCHES AT 25°C

The third source of noise investigated is caused by large switching current transients and was observed using a 10 ohm current sensing resistor (R_{SS}) in the V_{SS} line as shown in Figure 4-18. With five 6504s in parallel as shown in Figure 4-18, one volt peak-peak voltage spikes were noted across R_{SS} (Figure 4-19A). Two approaches were tested to eliminate this noise. First, a diode was placed across R_{SS1} and it had a negligible effect on the noise (Figure 4-19B). The diode was then removed and a 0.01 uF capacitor was placed across R_{SS1}, which eliminated the noise (Figure 4-19C).

The noise level as a function of frequency was determined by using the circuit of Figure 4-20. For twenty-three 6504s in parallel, the noise level did not vary with frequency, and was about 1.5 volt peak-peak measured at V_{RPS} at 500 Hz, 20 kHz, and 200 kHz. Circuit values for the 6504 experiment were: V_{DD} = 5.5 Vdc, R_{PS} = 100 ohms, R_{DD} = 100 ohms, R_{SS} = 10 ohms, C_{PS} = .03 uF, C_{DD} = .0033 uF, and C_{SS} = .01 uF, except that the C_{DD1} for the first DUT was zero. For twenty-one 1802s operated in parallel, the noise level was also invariant with frequency and was 1.5 volt peak-peak measured at V_{RPS} at frequencies up to 200 KHz. Circuit values for the 1802 experiment were the same as for the 6504 experiment, except that V_{DD} = 11.0 Vdc and R_{DD} = 1000 ohms. Therefore, it was concluded that noise level is not a frequency-limiting factor for parallel testing.

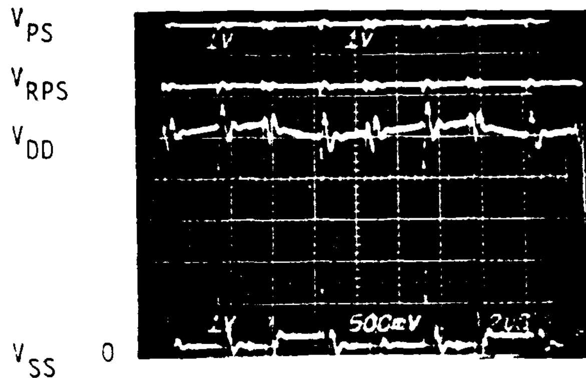
4.1.5 Evaluation of Potential Device Damage

Damage to a test device is possible if it is stuck at zero (S-A-0) or stuck-at-one (S-A-1) because it will source or sink large currents to or from the other device outputs paralleled with it. The magnitude of the stuck fault current increases with matrix size (number of paralleled devices). Therefore, experiments were performed to determine the extent of device damage due to stuck faults as a function of matrix size. These experiments consisted of two phases. The first phase determined worst case conditions of output power dissipation (voltage and current levels) for different matrix sizes under static S-A-0 and S-A-1 output states. The second phase consisted of operating 6504s and 1802s at elevated temperatures and applying the fault currents measured during the first phase. The results indicated that 6504 damage was unlikely but that 1802s would be damaged if S-A-0 and left on test for times on the order of 60 to 300 hours.

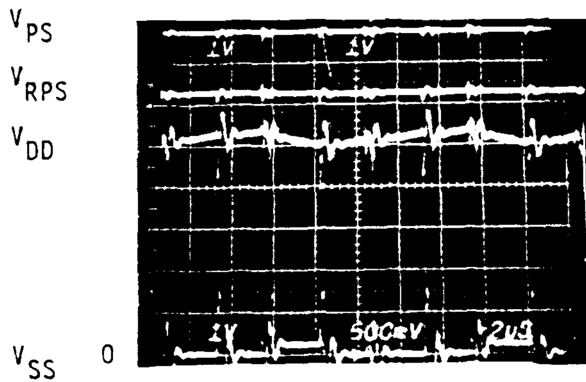


NOTE: CORRESPONDING INPUTS AND OUTPUTS ARE PARALLELED
$V_{DD} = 5.5V$
$R_{PS} = 100\Omega$, $R_{DD} = 470\Omega$, $R_{SS} = 10\Omega$
$C_{PS} = .03uF$, $C_{DD} = .0033uF$, and $C_{SS} = .01uF$

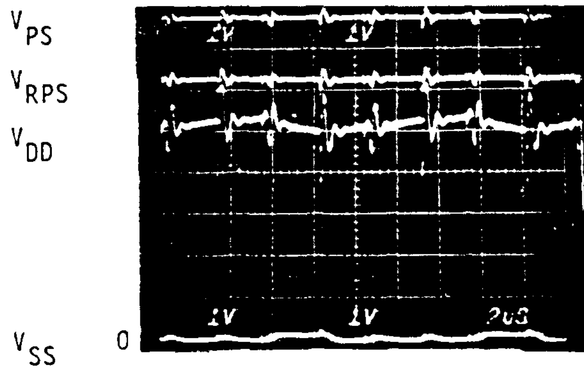
FIGURE 4-18. CIRCUIT FOR CHECKING NOISE AT V_{SS}



a) NO CAPACITOR OR DIODE ACROSS R_{SS1}

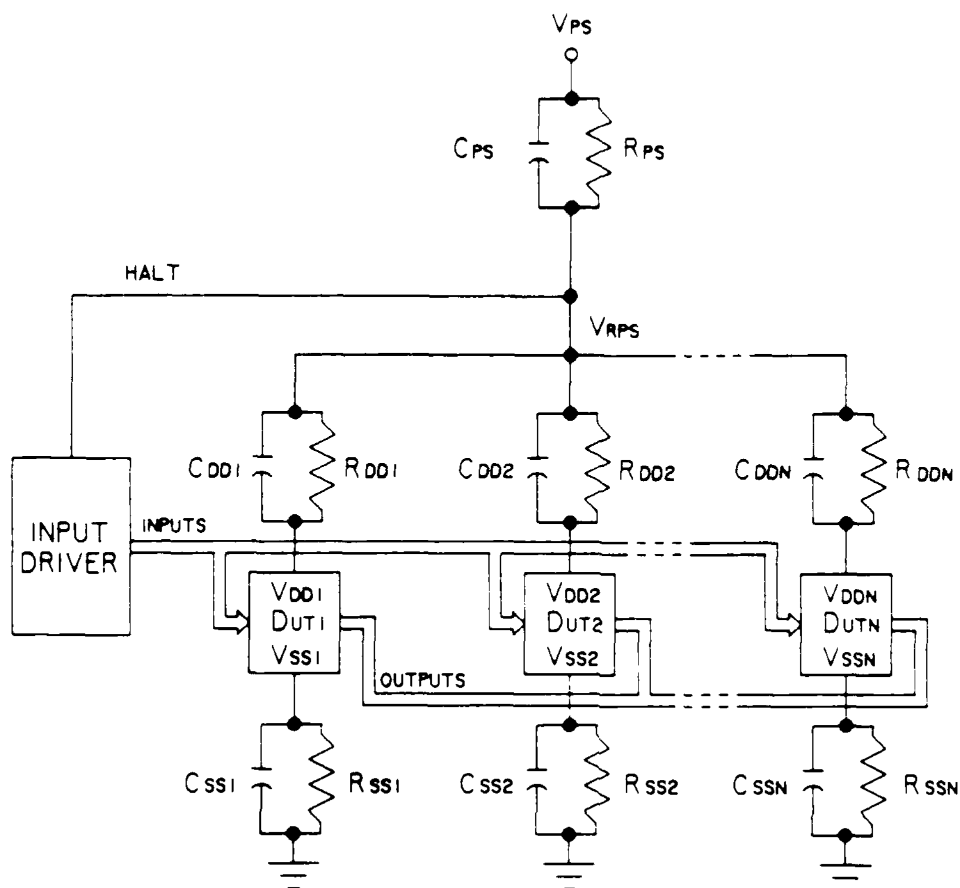


b) DIODE ACROSS R_{SS1}



c) .01μF CAPACITOR ACROSS R_{SS1}

FIGURE 4-19. 6504 WAVEFORMS OF V_{SS} NOISE



NOTE: CORRESPONDING INPUTS AND OUTPUTS ARE PARALLELED
$R_{PS} = 100\Omega$, $R_{DD} = 100\Omega$, $R_{SS} = 10\Omega$
$C_{PS} = .03uF$, $C_{DD} = .0033uF$, and $C_{SS} = .01uF$

FIGURE 4-20. NOISE MEASUREMENT CIRCUIT.

The measured output currents and the computed output power dissipations due to a S-A-0 and a S-A-1 for the first phase 6504 and 1802 experiments are shown in Tables 4-3 and 4-4. It is noted that the output current of stuck devices exceeds the manufacturer's specifications for output low and output high currents, 2 mA and -1 mA respectively for 6504s, and 1.7 mA and -0.54 mA respectively for 1802s. The subsequent phase two damage experiments were performed at 175°C for the 6504s and at both 150°C and 200°C for the 1802s. Two to three devices were tested at each S-A-0 and S-A-1 condition. Test results (Table 4-5) indicate no damage or degradation to the 6504s after 280 hours of operation with the worst case (25 device matrix) S-A-0 and S-A-1 conditions. The "no damage or degradation" conclusion was based on before and after electrical measurements and high magnification optical examinations of the die. Test results for 1802s operated at 200°C indicated no damage or degradation for the S-A-1 condition but damage in every case for the S-A-0 conditions. Typical damage to 1802s in the stressed areas is shown in the Figure 4-21 die photographs. Table 4-5 also includes 1802 results for two added experiments, one for a simulated matrix size of three at 200°C and one for a simulated matrix size of 25 at 150°C. The latter two experiments were added to determine if a smaller matrix size or lower operating temperature would eliminate the occurrence of damage. As noted in Table 4-5, damage occurred at these conditions also.

In conclusion, no damage or degradation due to S-A-0 or S-A-1 faults was observed in 6504s, but was observed in 1802s. The severity of the damage to 1802s at 200°C was more pronounced in devices that were stressed with higher S-A-0 currents, i.e., simulating matrices of thirteen and twenty-five devices. The devices that were operated at 150°C showed similar open and degraded outputs as the 1802s operated at 200°C, but required a longer time before the failures were observed. The experiment showed that the S-A-1 condition is not likely to damage a test device, but that the S-A-0 condition is highly likely to damage a device, even with a matrix size as small as three devices in parallel, if the test time is sufficiently long.

4.1.6 Matrix Size

The number of paralleled DUTs (matrix size) to be used for the demonstration test was selected after evaluating the following characteristics: 1) potential for latch-up, 2) potential for damage to failed devices left on test, 3) testing

TABLE 4-3. COMPARISON OF 6504 OUTPUT CURRENT AND POWER DISSIPATION FOR DIFFERENT MATRIX SIZES (SINGLE ERROR) AT 175°C

TEST PARAMETER	MATRIX SIZE		
	FIVE DUTS IN PARALLEL	THIRTEEN DUTS IN PARALLEL	TWENTY-FIVE DUTS IN PARALLEL
MAXIMUM OUTPUT SINK CURRENT THROUGH A DEVICE STUCK-AT-ZERO	20.3 mA	22.2 mA	28.0 mA
MAXIMUM OUTPUT SOURCE CURRENT THROUGH A DEVICE STUCK-AT-ONE	4.3 mA	4.4 mA	4.4 mA
MAXIMUM OUTPUT POWER DISSIPATION ON THE OUTPUT CIRCUITRY FOR A STUCK-AT-ZERO	46.7 mW	57.7 mW	86.8 mW
MAXIMUM OUTPUT POWER DISSIPATION ON THE OUTPUT CIRCUITRY FOR A STUCK-AT-ONE	19.7 mW	20.7 mW	21.2 mW

NOTE: TEST CONDITIONS APPLY TO THE CIRCUIT OF FIGURE 4-9
V_{DD} (NO ERROR, OPERATING VOLTAGE) = 5.5V
R_{PS} = 100 ohms, R_{DD} = 470 ohms, and R_{SS} = 10 ohms

TABLE 4-4. COMPARISON OF 1802 OUTPUT CURRENT AND POWER DISSIPATION FOR DIFFERENT MATRIX SIZES (SINGLE ERROR) AT 200°C

TEST PARAMETER	MATRIX SIZE		
	FIVE DUTS IN PARALLEL	THIRTEEN DUTS IN PARALLEL	TWENTY-FIVE IN PARALLEL
MAXIMUM OUTPUT SINK CURRENT THROUGH A DEVICE STUCK-AT-ZERO	15.9 mA	23.6 mA	24.1 mA
MAXIMUM OUTPUT SOURCE CURRENT THROUGH A DEVICE STICK-AT-ONE	3.8 mA	3.8 mA	3.8 mA
MAXIMUM OUTPUT POWER DISSIPATION ON THE OUTPUT CIRCUITRY FOR A STUCK-AT-ZERO	53.0 mW	125.0 mW	140.0 mW
MAXIMUM OUTPUT POWER DISSIPATION ON THE OUTPUT CIRCUITRY FOR STUCK-AT-ONE	21.0 mW	21.0 mW	21.0 mW

NOTE: TEST VALUES APPLY TO THE CIRCUIT OF FIGURE 4-9
V_{DD} (NO ERROR, OPERATING VOLTAGE) = 11.0 Vdc
R_{PS} = 100 OHMS, R_{DD} = 1K OHMS, R_{SS} = 10 OHMS

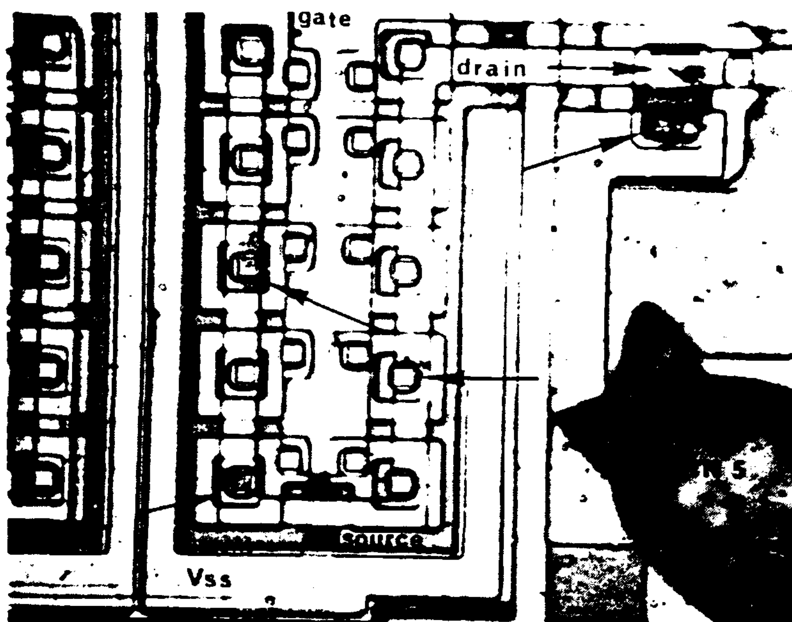
TABLE 4-5. EXPERIMENTAL DAMAGE RESULTS FOR S-A-0 AND S-A-1 AT HIGH TEMPERATURES

DEVICE	TEMPERATURE	OUTPUT STATE	SIMULATE MATRIX SIZE	OUTPUT CURRENT	TEST DURATION (HOURS)	OUTPUT DAMAGE (HOURS)
6504	175°C	S-A-1	25	-4.4 mA	280	NONE
	175°C	S-A-0	25	28.0 mA	280	NONE
1802	200°C	S-A-1	25	-3.75mA	400	NONE
	200°C	S-A-0	3	8.6 mA	360	283
	200°C	S-A-0	5	16.0 mA	400	160
	200°C	S-A-0	13	23.6 mA	400	136
	200°C	S-A-0	25	24.1 mA	400	64
	150°C	S-A-0	25	29.8 mA	400	192

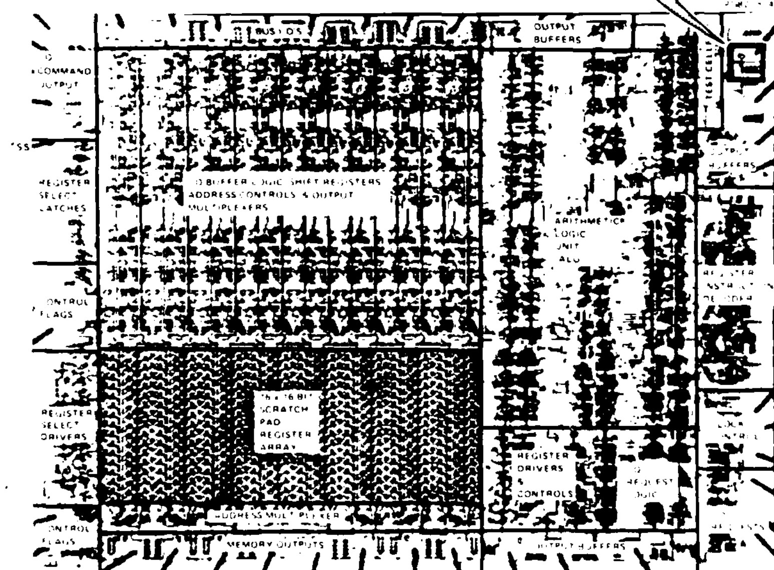
NOTE: TEST CONDITIONS APPLY TO THE CIRCUIT OF FIGURE 4-9.

6504: V_{DD} (NO ERROR OPERATING VOLTAGE) = 5.5V
R_{PS} = 100 OHMS, R_{DD} = 470 OHMS, R_{SS} = 0 OHM

1802: V_{DD} (NO ERROR OPERATING VOLTAGES) = 11.0V
R_{PS} = 100 OHMS, R_{DD} = 1000 OHMS, R_{SS} = 10 OHMS



S-A-O OUTPUT DAMAGE (ARROWS)



1802 DIE PHOTO AND FUNCTIONAL BLOCKS

FIGURE 4-21. OPTICAL PHOTOGRAPH OF 1802 OUTPUT DAMAGE

effectiveness, 4) detectable errors, 5) number of chassis input wires, and 6) number of voltage measurements required to isolate a failed device. The objective was to maximize the number of DUTs in parallel, up to the program requirement of 25 DUTs, while ensuring proper device operation at elevated temperatures. Five DUTs in parallel was the minimum number considered, as fewer than five would probably eliminate the benefits of parallel testing. Three matrix sizes were evaluated: 5, 13, and 25 devices in parallel. A chassis configuration of five matrices of five paralleled devices was selected for both the 6504 and the 1802 for the following reasons, given in descending order of importance:

6504 - 1) Minimize latch-up potential
2) Minimize potential damage to failed devices
3) Minimize driver halts
4) Minimize measurements to isolate failed devices

1802 - 1) Minimize potential damage to failed devices
2) Minimize latch-up potential
3) Minimize driver halts
4) Minimize measurements to isolate failed devices

The characteristics affected by matrix size are discussed further in the following paragraphs.

To prevent latch-up, the value of V_{DD} must be maintained above some critical value. For the 6504 test conditions noted in Table 4-6, the five-device matrix is clearly the best choice, because for the other choices, V_{DD} falls below the critical value when errors are present (an error occurs when one DUT output is different from the other device outputs in the matrix). Considerations of latch-up prevention also led to the choice of a small R_{DD} value in order to prevent V_{DD} from falling too low. The value of R_{DD} based on the criteria of preventing latch-up did not provide sufficient resistive current limiting to insure no damage to stuck devices.

Potential damage to failed devices left on test was discussed in detail in the previous Section 4.1.5. It was noted that the output current for a device S-A-0 increased with matrix size and exceeded the manufacturer's specification

TABLE 4-6. 6504 MATRIX SIZE COMPARISON

CHARACTERISTIC	MATRIX SIZE			COMMENTS
	FIVE DUTS IN PARALLEL	THIRTEEN DUTS IN PARALLEL	TWENTY-FIVE IN PARALLEL	
MINIMUM V_{DD} VOLTAGE WHEN ERRORS ARE PRESENT	4.4 V	3.9 V	3.49 V	LATCHING MAY OCCUR IF $V_{DD} \leq 4.0V$

NOTE: VALUES APPLY TO THE CIRCUIT OF FIGURE 4-20
V_{DD} (NO ERROR, OPERATING VOLTAGE) = 5.5 Vdc.
R_{PS} = 51 ohms, R_{DD} = 100 ohms, R_{SS} = 10 ohms.
C_{PS} = .03 uF, C_{DD} = .003 uF, and C_{SS} = .01 uF

even for five devices in parallel, for both the 6504 and the 1802. Therefore, the choice of a matrix of five paralleled devices minimized but did not eliminate the potential for damage.

Another reason for the selected configuration relates to testing effectiveness. A failed device causes frequent driver halts, which could occur every clock cycle for some stuck faults. Measuring the supply pins of the DUTs to isolate the failure may take 10 to 50 seconds depending on the settling time, the number of failed devices, and the number of parts in each matrix. Ten to 50 seconds is long compared to the clock cycle time (up to 100 us). Therefore, a failed device left on test could cause all other devices in the chassis to operate basically in a static state. To keep the driver from staying in this static state, the capability of masking the window detectors was added to the software and hardware. This capability was combined with separate input buffering (1802 only) for the inputs of each matrix to make it possible for DUTs in matrices containing no failed DUTs to function normally. The choice of five groups of five matrices therefore minimizes the effect of continuous halting for 80% of the DUTs. (Further details of how the current detector masking is applied are provided in Appendix C.)

Considerations that include detectable errors, number of chassis input wires, and number of voltage measurements to isolate a failed device as a function of matrix size are summarized in Tables 4-7 and 4-8. These considerations were important to test efficiency and hardware cost, but were not driving factors in the choice of matrix size. In these comparisons, the number of matrices required to make up a chassis count of 25 DUTs were important to the results. For example, 5 matrices of 5 paralleled devices, 2 matrices of 13 paralleled devices, or 1 matrix of 25 paralleled devices are required to make up the chassis count of 25 devices on test. Error detection efficiency was slightly lower for the five DUT matrix configurations, but failed device isolation efficiency was by far the best for this configuration. The greater number of wires through the oven interface for the five DUT matrix configuration is a clear disadvantage over other matrix sizes, but this is true only if the matrix inputs are separately buffered. Separately buffered matrix inputs were used for the 1802s to reduce latch-up potential, but were not required for the 6504s.

TABLE 4-7. COMPARISON OF 6504 CHASSIS CONFIGURATION

CHARACTERISTIC	CHASSIS CONFIGURATION 5 MATRICES, EACH CONTAINING 5 DUTS	2 MATRICES, EACH CONTAINING 13 DUTS	1 MATRIX CONTAINING 25 DUTS	COMMENTS
IF THE COMPARE DATA SIGNAL 1/ IS SENT TO THE DLTS 2/ THE MAXIMUM NUMBER OF DETECTABLE ERRORS PER CHASSIS DURING:				
a) ONE CHIP ENABLE CYCLE	20	24	24	ASSUMES NO LATCH-UP AND AT MOST FOUR FAILURES PER DUT CYCLE
b) DIFFERENT CYCLES	25	26	25	
IF THE COMPARE DATA SIGNAL IS NOT SENT TO THE DLTS, THE MAXIMUM NUMBER OF DETECTABLE ERRORS PER CHASSIS DURING:				
a) ONE CHIP ENABLE CYCLE	10	12	12	ASSUMES NO LATCH-UP AND LESS THAN ONE HALF OF THE DUTS FAIL PER DUT CYCLE
b) DIFFERENT CYCLES	25	26	25	
NUMBER OF INPUT WIRES THROUGH OVEN DOORS	14	14	14	ALL DEVICE INPUTS IN CHASSIS PARALLELED
	70	28	14	SEPARATE PARALLELED INPUTS FOR EACH MATRIX
NUMBER OF VOLTAGE MEASUREMENTS TO ISOLATE FAILED DEVICE	10	15	26	ASSUMES NO R_{SS} RESISTOR AND ONE MATRIX CONTAINS FAILED DUT(S)

NOTES:

1/ THE COMPARE DATA SIGNAL IS DISCUSSED IN APPENDIX B.
2/ THIS TECHNIQUE WILL ONLY WORK WITH A ONE OUTPUT DEVICE.

TABLE 4-8. COMPARISON OF 1802 CHASSIS CONFIGURATION

CHARACTERISTIC	CHASSIS CONFIGURATION 5 MATRICES, EACH CONTAINING 5 DUTS	2 MATRICES, EACH CONTAINING 13 DUTS	1 MATRIX CONTAINING 25 DUTS	COMMENTS
MAXIMUM NUMBER OF DETECTABLE ERRORS/CHASSIS DURING:				
a) ONE CLOCK CYCLE	10	12	12	ASSUMES NO LATCH-UP AND AT MOST FOUR FAILURES PER DUT
b) DIFFERENT CYCLES	25	26	25	
NUMBER OF WIRES THROUGH OVEN INTERFACE	90	36	18	SEPERATE PARALLELED INPUTS FOR EACH MATRIX
NUMBER OF VOLTAGE MEASUREMENTS TO ISOLATE FAILED DEVICE	15	28	51	ASSUMES ONE MATRIX CONTAINS FAILED DUTS

4.1.7 Failure Simulations

Stuck-at-zero (S-A-0), stuck-at-one (S-A-1), and open circuit simulations were performed to identify the functional failures detectable by the parallel test method. Tests were performed with five devices operated in the parallel configuration shown in the previous Figure 4-20. Test conditions for 6504s included a chip enable time of 5 us and the circuit element values listed in Figure 4-20, except that R_{DD} was 470 ohms. For the 1802 tests, the clock cycle time was 2 us, R_{DD} was 1000 ohms and C_{DD} was removed. Generally, this simulation showed that the detectable faults included input opens, output shorts, inputs or outputs stuck high, and all faults for dual purpose input/output pins. Input shorts and output opens are not detectable (except for dual purpose input/output lines) with devices paralleled in the Figure 4-20 configuration. In this configuration, corresponding inputs and outputs are directly connected in parallel without buffering or isolation. Thus, an input short on one device shorts the corresponding inputs of all paralleled devices, and no detectable error is produced.

To determine the 6504 functional failures detectable by the parallel method, the pins on one of the paralleled devices were shorted to ground (V_{SS}), opened, and shorted to the supply voltage (V_{DD}), one pin at a time. As shown in Table 4-9, an error was not detected for an address, control, or data signal shorted to ground. In addition, an open control or data out signal did not result in an error indication. Finally, all combinations of 6504 signals shorted to V_{DD} caused latch-up in other devices in the matrix. Latch-up occurred when the shorted signal's voltage level was higher than the other V_{DD} voltage levels (the shorted signal's voltage level is transferred to the other devices in the matrix because all corresponding input signals are wired in parallel).

The 1802 functional failures detectable by the parallel method were simulated in the same manner as above. As shown in Table 4-10, except for the $\overline{\text{WAIT}}$ signal, all control signals shorted to ground as well as open outputs could not be detected. Also, for V_{DD} open, no error was detected because at least three input signals were always high, keeping the input protection diodes (Figure 4-22) forward biased. However, an error was detected each time an 1802 input line was shorted to V_{DD}.

TABLE 4-9. 6504 FAULT SIMULATION RESULTS

6504 PIN FUNCTION	FAULT SIMULATIONS 1/		
	SHORTED TO GROUND	6504 PIN OPENED	6504 PIN SHORTED TO V_{DD} 2/
	ERROR DETECTED	ERROR DETECTED	ERROR DETECTED
$A_0 - A_{11}$	4/	X	X
$\overline{E}$			X
$\overline{W}$			X
D		X	X
Q	X		X
V_{DD}	X	X	N/A 3/
V_{SS}	N/A 3/	X	X

NOTES:

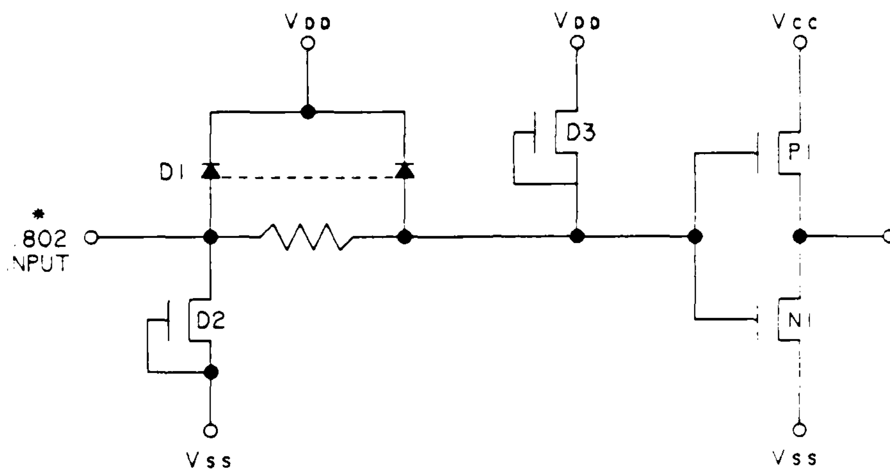
1/ GALPAT OR CHECKERBOARD PATTERN PROVIDE SAME RESULTS
2/ 6504 LATCH-UP
3/ N/A - NOT APPLICABLE
4/ DECODER PROBLEMS ARE DETECTABLE

TABLE 4-10. 1802 FAULT SIMULATION RESULTS

1802 PIN FUNCTION	FAULT SIMULATION 1/		
	1802 PIN SHORTED TO GROUND	1802 PIN OPENED	1802 PIN SHORTED TO V_{DD}
	ERROR DETECTED	ERROR DETECTED	ERROR DETECTED
CLOCK		X	X
$\overline{WAIT}$	X	X	N/A
$\overline{CLEAR}$		X	X
Q	X		X
SC0, SC1	X		X
$\overline{MRD}$	X		X
BUS 0-7	X	X	X
V_{CC}	X		N/A
$N_0 - N_2$	X		X
V_{SS}	N/A		X
EF1, EF2	X	X	3/
EF3, EF4	4/	X	X
MA0-7	X		X
TPA, TPB	X	X	X
$\overline{MWR}$	X		X
$\overline{INT}$		X	X
$\overline{DMA - IN/OUT}$		X	X
$\overline{XTAL}$	X		X
V_{DD}	X	X	N/A

NOTES:

1/ SIMILAR TO MIL-M-38510/47001 DRIVER CIRCUIT
2/ N/A - NOT APPLICABLE
3/ PIN FUNCTION CONNECTED TO V_{DD}
4/ PIN FUNCTION CONNECTED TO GROUND



$\overline{\text{DMA-IN}}$, $\overline{\text{DMA-OUT}}$, $\overline{\text{INTERRUPT}}$, & $\overline{\text{CLEAR}}$ INPUTS

FIGURE 4-22. 1802 INPUT PROTECTION CIRCUIT

4.1.8 Current and Voltage Limiting

Standard laboratory provisions for current and voltage limiting for protecting the devices-under-test were used during the demonstration test. Current limiting was provided by the combination of the R_{PS} and R_{DD} resistors (Figure 4-9), while voltage limiting was provided by the built-in voltage limiting feature of the Lambda power supply.

The initially selected values of R_{PS} and R_{DD} provided sufficient current limiting (except for S-A-0s). However, higher priority considerations to prevent latch-up and detect S-A-1 faults as discussed in Sections 4.1.3 and 4.1.11, drove the choice of values for R_{PS} and R_{DD} to a combination of values that provided insufficient current limiting. Therefore, for the parallel test implementation used in this project, damage prevention was to be accomplished by removing power from the affected DUTs.

Voltage limiting was provided by the Lambda voltage supplies, which have built-in voltage limiting capability. The 6504 and 1802 driver and DUT over-voltage cutoffs were set 0.5V above their demonstration test settings. Therefore, if a voltage supply increased above the over-voltage level for any reason, the supply would turn off and the DUTs would be protected.

4.1.9 Background Current as a Function of Clock Rate

Characterizing the operating current as a function of clock rate is important because detecting errors is performed by noting changes from the error-free supply current level. This data was needed to assist in selecting resistor values (R_{PS}, R_{DD}, R_{SS}) to control V_{DD} level changes and set the current detector sensitivity. The V_{DD} voltage level will rise when a false halt occurs (the driver stops when no functional error is present) and must be controlled so that V_{DD} does not exceed the manufacturer's maximum operating supply voltage level. The V_{DD} voltage level will also drop when a functional error occurs, and to prevent latch-up the V_{DD} voltage level must not be allowed to fall to a level lower than the input high voltage level.

The results of our experiments to characterize device operating current as a function of frequency are shown in Figure 4-23. These graphs were obtained by measuring the operating current (I_{DD}) in a single device at room temperature while varying the operating frequency between dc (driver halted) and 200 kHz. It is noted that the device current increases approximately one order of magnitude as the operating frequency is increased from dc to 200 KHz.

4.1.10 Background Current as a Function of Temperature

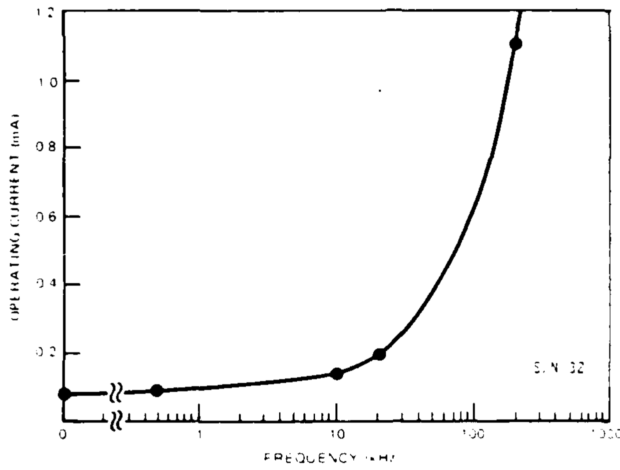
As ambient temperature increases from 25°C, the background current will at first decrease and then rise for both the 6504 and the 1802. These background current changes are important because the comparator voltage levels in the detector must be set after D[illegible]s reach the test temperature and V_{DD} supply levels are set.

The experimental results shown in Figure 4-24 for the 6504 were obtained for a chip enable (CE) cycle of 5 us. Current values were computed from the voltage drop across a 470 ohm R_{DD} resistor. Subsequent to these tests, a CE cycle time of 100 us was established for the demonstration test, which results in a downward shift of the background current vs. temperature function by a factor of 2.5 from the Figure 4-24 levels.

Figure 4-25 shows the 1802 experimental results. These results were obtained for a clock cycle of 1 us with the current computed from the voltage drop across a 1000 ohm R_{DD} resistor. Subsequently, a clock cycle time of 80 us was established, resulting in a downward shift of the background current vs. temperature function by a factor of 14 from the Figure 4-25 levels.

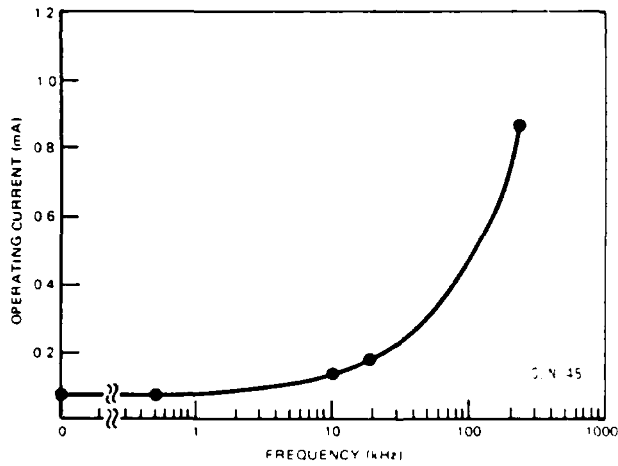
4.1.11 Temperature Effect on the Source and Sink Output Current

As the ambient temperature rises above 25°C, a CMOS output is unable to source or sink as much current as it did at 25°C. It is important to know the magnitude of these current changes because they result in reduced error currents for stuck faults and the current detector must be sufficiently sensitive to detect the reduced error currents at elevated test temperatures.



6504 OPERATING CURRENT

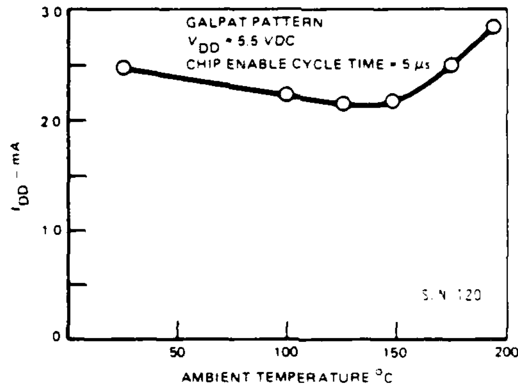
NOTE: VALUES APPLY TO THE CIRCUIT OF FIGURE 4-9
V_{DD} = 5.5 V_{dc}, V_{IH} = 4.0 V_{dc}
R_{PS} = 0 OHMS, R_{DD} = 470 OHMS, R_{SS} = 10 OHMS



1802 OPERATING CURRENT

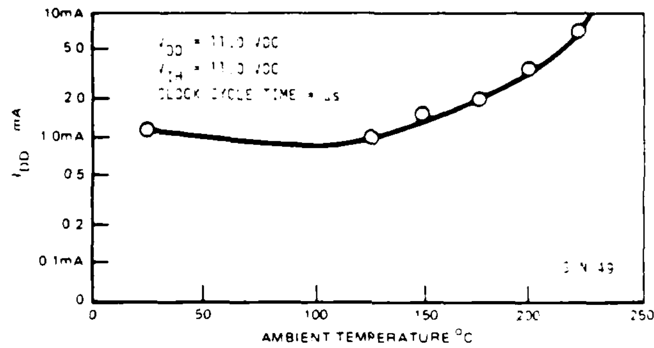
NOTE: VALUES APPLY TO THE CIRCUIT OF FIGURE 4-9
V_{DD} = 11.0 V_{dc}, V_{IH} = 11.0 V_{dc}
R_{PS} = 0 OHMS, R_{DD} = 1000 OHMS, R_{SS} = 0 OHMS

FIGURE 4-23. 6504 AND 1802 OPERATING CHARACTERISTICS



NOTE. VALUES APPLY TO THE CIRCUIT OF FIGURE 4-20
R_{PS} = 0 OHMS, R_{DD} = 470 OHMS, R_{SS} = 0 OHMS
C_{PS} = 0μF, C_{DD} = .033μF, C_{SS} = 0μF

FIGURE 4-24. 6504 BACKGROUND CURRENT VS. TEMPERATURE



NOTE VALUES APPLY TO THE CIRCUIT OF FIGURE 4-9
R_{PS} = 0 OHMS, R_{DD} = 1k OHMS, R_{SS} = 0 OHMS

FIGURE 4-25. 1802 BACKGROUND CURRENT VS. TEMPERATURE

For a 6504 matrix of 25 devices at 25°C, the output is able to source an
sink 5.2 mA and 49 mA, respectively. At 175°C, these values drop to 4.4 mA a
28 mA respectively. For an 1802 matrix of 25 devices at 25°C, the output is
to source and sink 4.7 mA and 50 mA, respectively. However, at 200°C, these
drop to 3.79 mA and 24.1 mA, respectively. Test conditions for these measure
were previously noted in Tables 4-3 and 4-5. These results indicate that the
required current detector sensitivity is established by device source current
capability at elevated temperature. We obtained the required current detecto
sensitivity by setting the current sensing resistor R_{PS} to 270 ohms for 6504s
and to 150 ohms for 1802s. These resistance values resulted in reliable dete
of S-A-1s at elevated temperatures.

4.2 DEMONSTRATION TEST CONDITIONS

Table 4-11 presents a summary of the selected demonstration test conditi
for each part type. Also, the selected bias circuits for the 6504 and 1802 a
shown in Figures 4-26 and 4-27, respectively. The various choices required f
the demonstration test and rationale for their selected values were:

Number of Paralleled Devices and Chassis Configuration - The configurati
of five groups of five paralleled devices was a compromise between small numb
of paralleled devices to prevent latch-up and minimize damage to failed devic
left on test, and large numbers of paralleled devices to minimize test hardwa

Ambient Test Temperature - The maximum ambient temperature for error-fre
operation was initially selected for both device types. However, for the 180
latch-up occurred at the initially selected 200°C temperature. The maximum
ambient test temperature that assured no 1802 latch-up, 125°C, was then selec

Input High Voltage (V_{IH}) Levels - Values were selected based on a com-
promise between low values for latch-up prevention and high values for minimu
noise.

Cycle Time - The minimum values were selected that would assure adequate
circuit settling time such that a fault could be detected and the driver halt
to preserve the input conditions that resulted in the fault.

TABLE 4-11. 6504 AND 1802 DEMONSTRATION TEST CONDITIONS

CONDITION	6504	1802
QUANTITY TESTED	25	25
MATRIX SIZE	5	5
AMBIENT TEST TEMPERATURE	175°C	125°C
SUPPLY VOLTAGE (V_{DD}) 1/	5.5 Vdc	11.0 Vdc
INPUT VOLTAGE (V_{IH})	4.0 V	10.0 V
CYCLE TIME	100 us	80 us
PATTERN OR INSTRUCTION SEQUENCE	GALPAT	EXERCISES ALL ODD NUMBER INSTRUCTIONS
TEST CIRCUIT COMPONENTS 2/		
RESISTORS		
R_{PS}	270 ohms	150 ohms
R_{DD}	100 ohms	100 ohms
R_{SS}	N/A 3/	10 ohms
CAPACITORS		
C_{PS}	.003 uF	.003 uF
C_{DD}	.0039 uF 4/	N/A 3/
C_{SS}	N/A 3/	.01 uF

NOTE:

1/ VOLTAGE LEVELS FOR NO FAULTS OR ERRORS.
2/ REFER TO FIGURE 4-20.
3/ NOT APPLICABLE.
4/ IN ADDITION TO C_{DD}, A 1000 pF CAPACITOR IS CONNECTED FROM V_{CC} TO GROUND IN THE 6504 BIAS CIRCUIT, FIGURE 4-26.

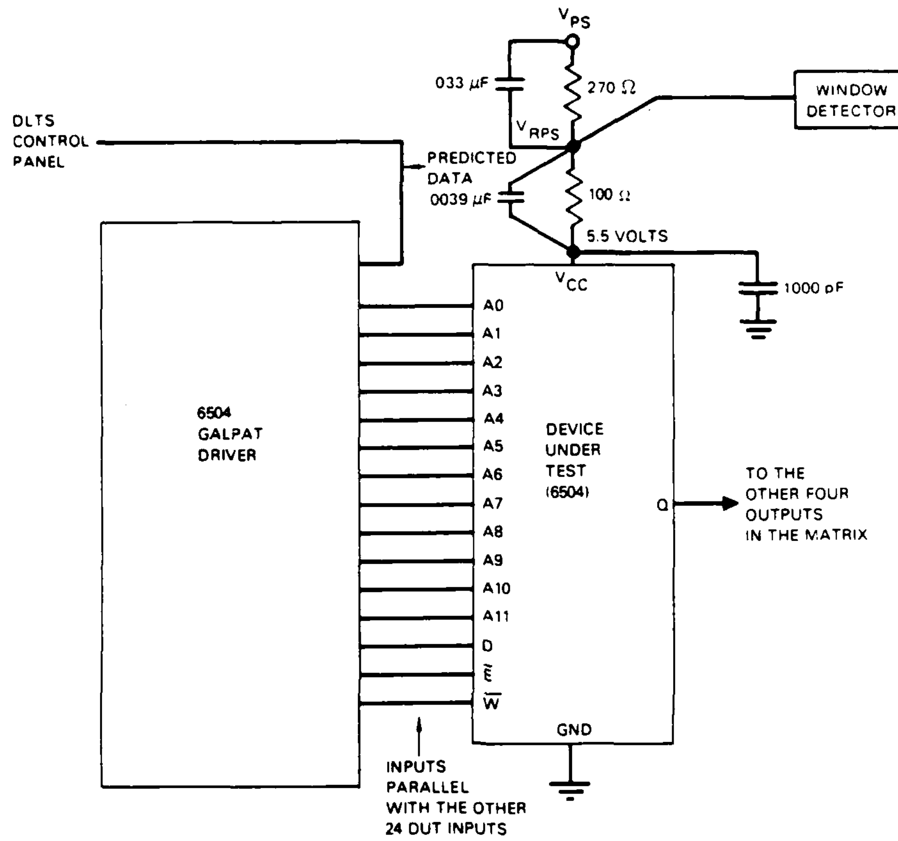
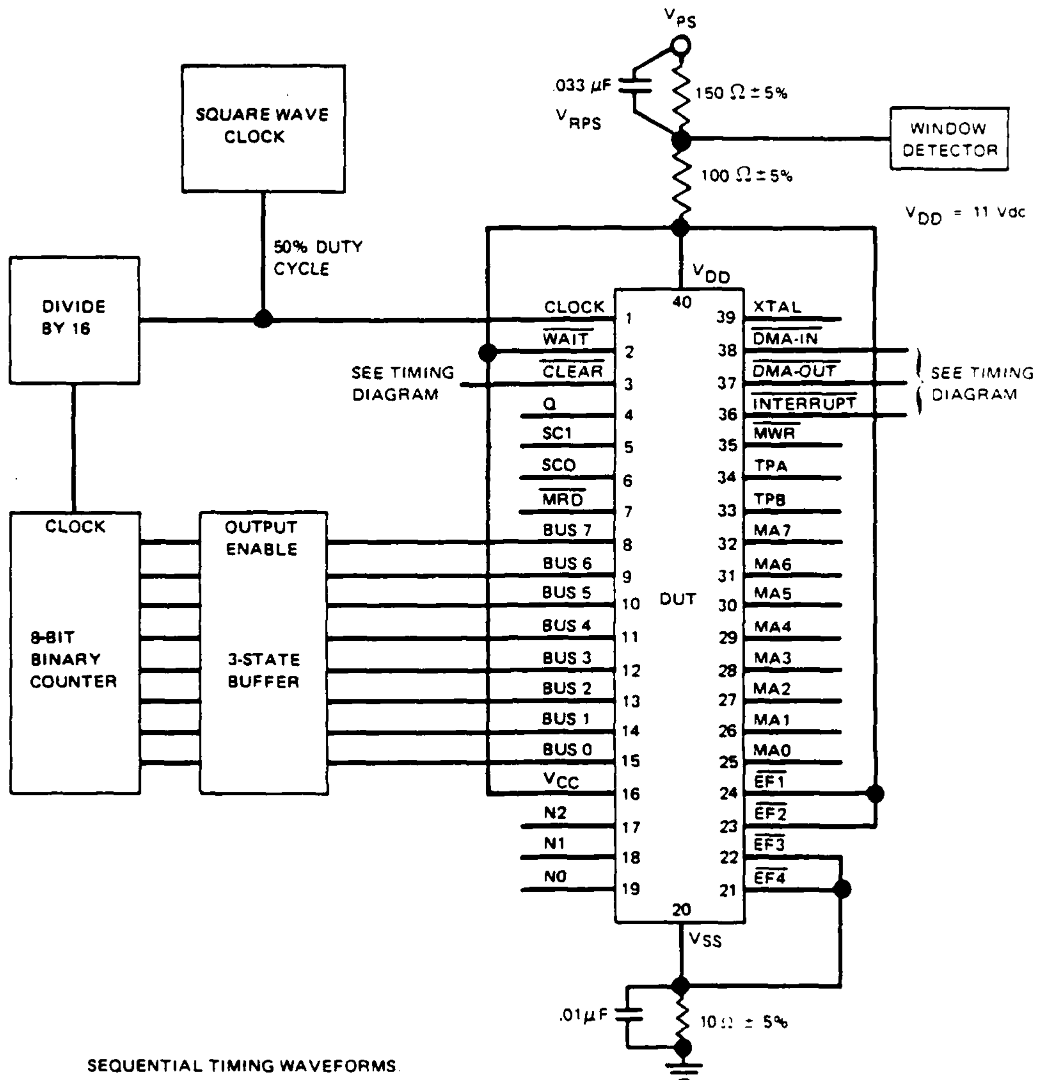


FIGURE 4-26. 6504 BIAS CIRCUIT



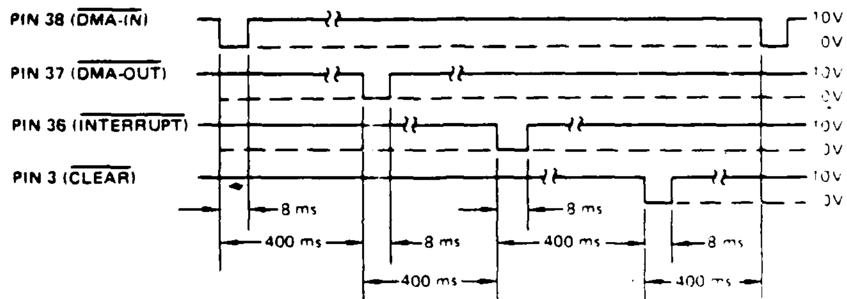


FIGURE 4-27. 1802 BIAS CIRCUIT

Patterns or Instruction Sequence - The GALPAT (N2) pattern was selected for the 6504 as the most comprehensive test pattern and because test time was not limited. The MIL-M-38510/47001 burn-in circuit instructions were initially selected for the 1802, but the even-numbered instructions were subsequently deleted to eliminate the idle instruction (00_H), which caused large switching currents and contributed to 1802 latch-up.

Test Circuit Resistor and Capacitor Values - Values for R_{PS} were the minimum values which permitted reliable detection of stuck high faults. Values for R_{DD} were the maximum values which allowed latch-up free operation. The value for R_{SS} was the minimum value for reliable isolation of stuck low failed devices. Capacitance values were based on a compromise between large values for minimum noise and small values for short clock cycle time.

5.0 STAGE III: DEMONSTRATION TESTING

Demonstration tests were performed to examine the functionality of parallel testing for reliability characterization and burn-in of CMOS LSI microcircuits. Improvements and refinements of the basic concept that were identified in Section 4 were incorporated for the demonstration tests.

5.1 APPROACH

Our approach to the test objectives was to conduct a 500-hour demonstration test at elevated ambient temperatures while continuously monitoring device-under-test status with our Dynamic Life Test System (DLTS). Interim electrical measurements of device performance and simulations of stuck-at-zero (S-A-0) and stuck-at-one (S-A-1) faults were also performed.

The demonstration test consisted of a single elevated-temperature dynamic bias test cell for each device type using the bias circuits of previous Figures 4-26 and 4-27. Twenty-five of each device type that passed initial electrical tests were operated for 500 hours at the conditions previously stated in Table 4-11. Interim 125°C electrical tests were performed at 72, 168, and 500-hours after cool-down with bias applied. The interim electrical tests were performed at 125°C to obtain worst case device parametric changes with a single electrical test. After test completion (500 hours), the electrical tests were also performed at 25°C and -55°C. In addition, five unstressed control devices were subjected to the interim electrical tests just prior to performing the measurements with the demonstration test devices. The control sample measurements provided a measure of the automated test system stability.

Continuous monitoring of device-under-test status was accomplished with the Dynamic Life Test System (DLTS) described in Appendix C, programmed to isolate and identify failed S-A-0 and S-A-1 devices. Daily data printouts of device voltage/currents and device functionality were obtained.

Periodic simulations of S-A-0 and S-A-1 faults were performed to demonstrate that such faults could be detected at the life test temperatures and to verify the integrity of the error detection system. The fault simulations were performed

twice: 1) at each interim electrical test interval after the devices were inserted into the test chambers, and 2) prior to removing them from the test chambers. The 6504 and 1802 circuit voltage levels are provided in Figures 5-1 to 5-4 when "DUT 1" is at a simulated S-A-0 or S-A-1 to show typical voltage levels that may be expected under fault conditions in parallel testing.

5.2 TEST RESULTS

The demonstration test results included the data from the interim electrical tests, the Dynamic Life Test System (DLTS) daily printouts, and the results of periodic fault simulations. The interim electrical test and the DLTS monitoring system revealed no 6504 or 1802 failures during the 500-hour operating period. The stuck-at-zero and stuck-at-one fault simulations indicated complete success in detecting such faults in both 6504s and 1802s. However, false halts occurred on three occasions during the 6504 demonstration test and will be discussed in the following section.

5.3 DATA ANALYSIS

All of the demonstration test data were evaluated to assess the reliability of the parallel technique. Specific objectives of the data evaluations were to assess parameter stability and the effectiveness of continuous monitoring for error-free operation at the demonstration test temperatures.

Parameter Stability - Electrical parameter stability is one measurement of the reliability of a monitoring technique. If device parameters are stable during the test, then one may conclude that parallel testing itself does not degrade the devices on test. Therefore, to check the reliability of the test method, the device parametric data collected during demonstration testing was examined for stability.

Individual device as well as group performance was examined for both the 6504 and 1302. With the exception of quiescent supply current, all 6504 measured parameter values for demonstration tests were stable and no degradation trends were observed. The mean data values of the quiescent supply current shifted, but followed the mean shifts of the control device data, indicating that the changes were due to drifts in the automated test system. The 1802 data showed that all the measurements were stable and no degrading trends were noted.

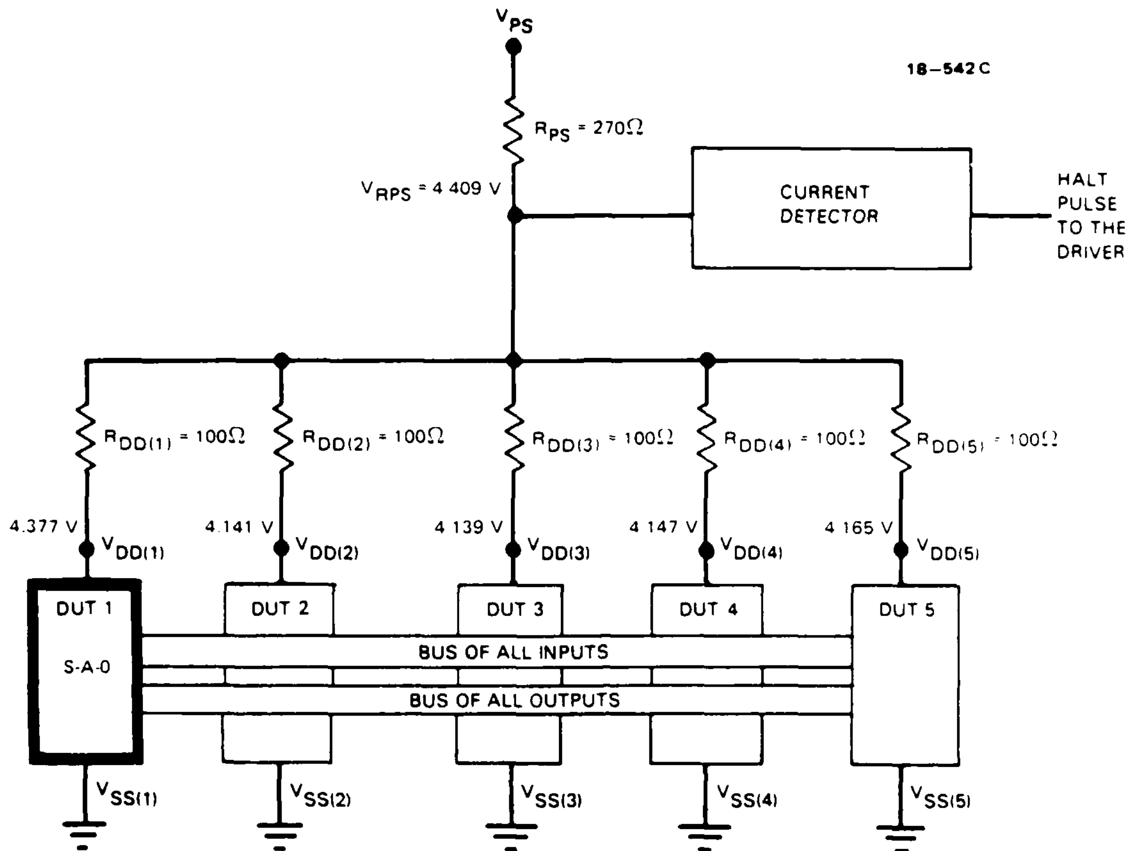


FIGURE 5-1. 6504 MATRIX SIMULATING ONE S-A-0 AT 175°C

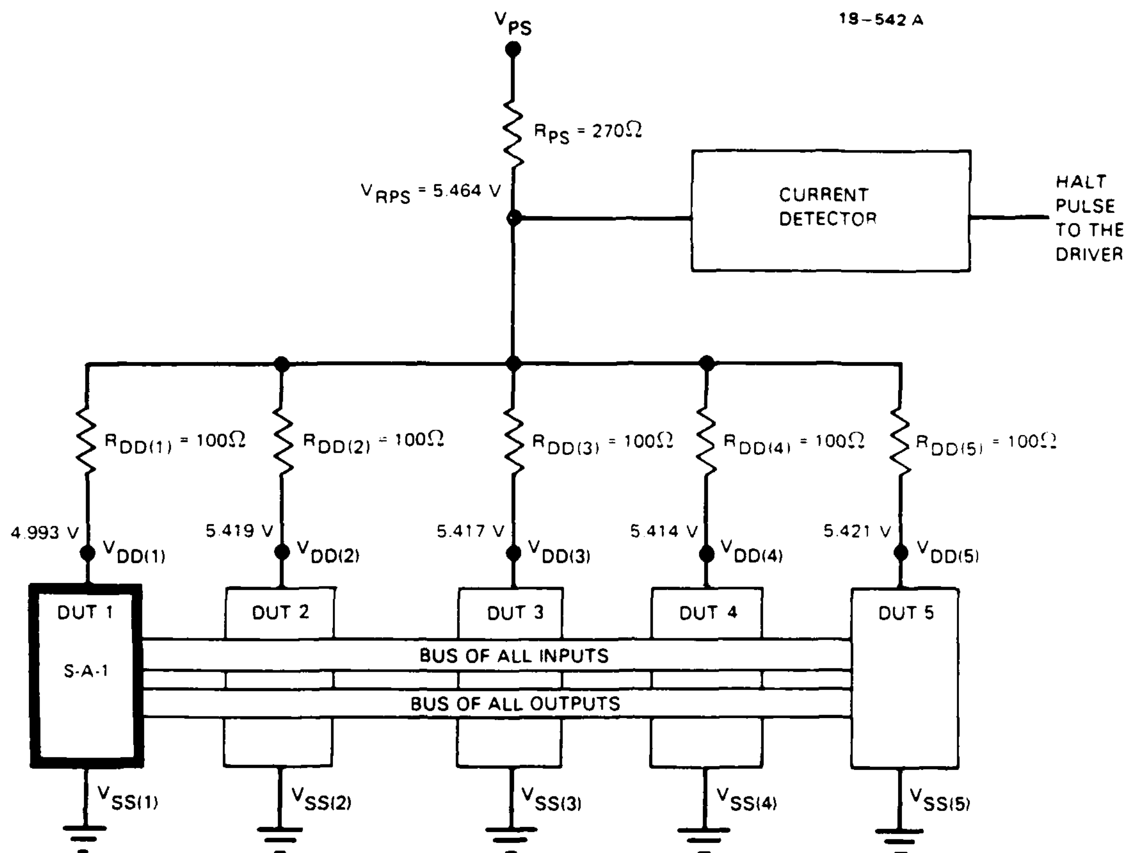


FIGURE 5-2. 6504 MATRIX SIMULATING ONE S-A-1 AT 175°C

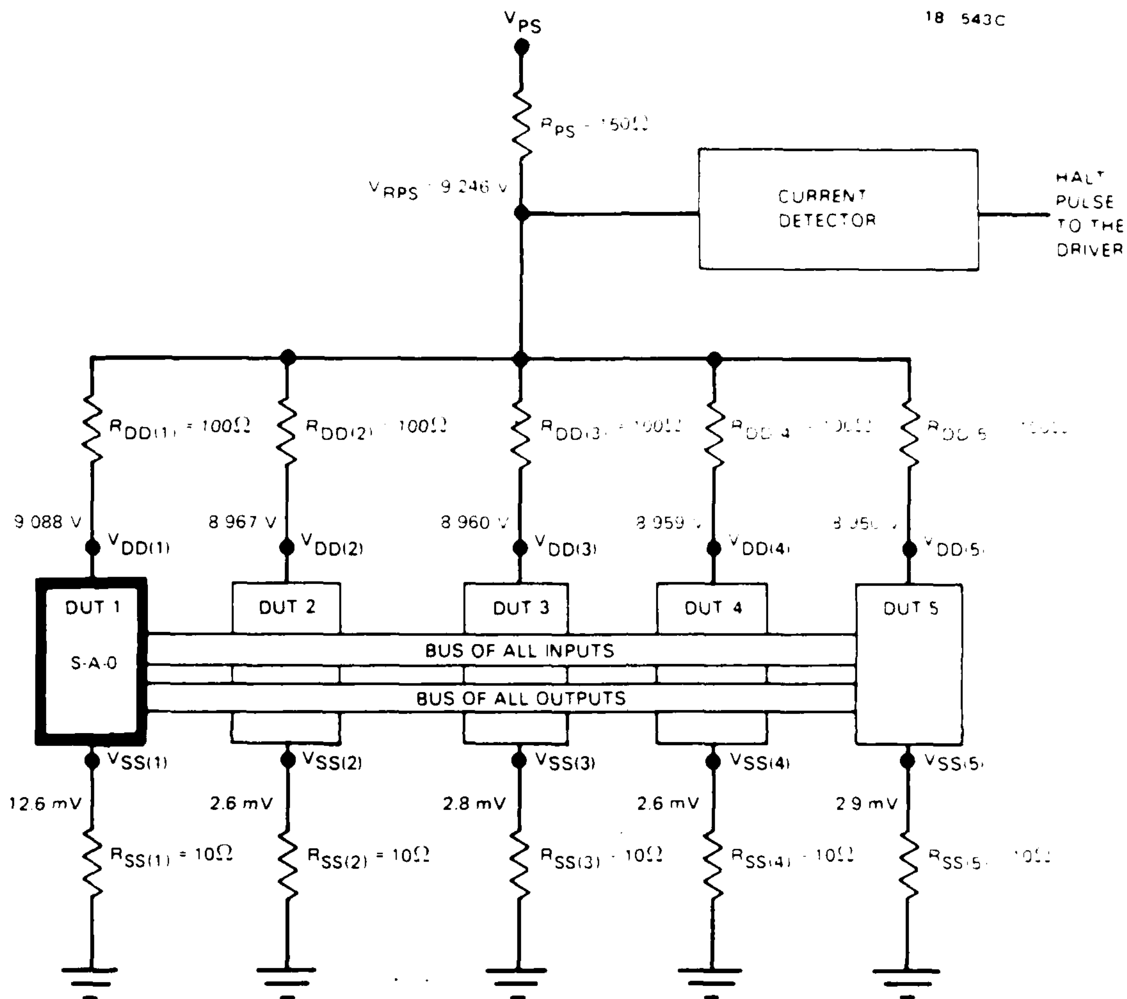


FIGURE 5-3. 1802 MATRIX SIMULATING ONE S-A-0 AT 125°C

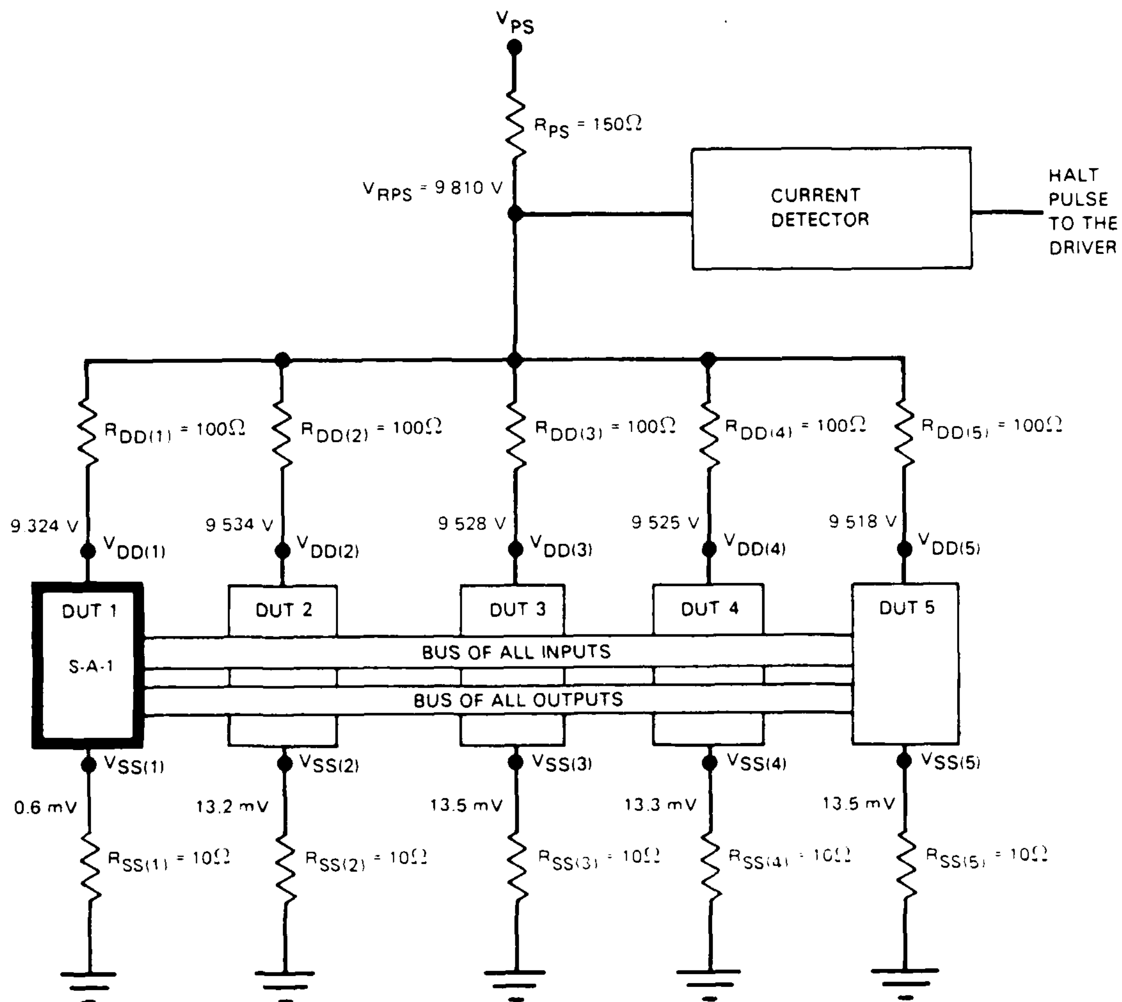


FIGURE 5-4. 1802 MATRIX SIMULATING ONE S-A-1 AT 125°C

Plots were made of sample parameters that were likely to degrade during the demonstration test. Plots of 6504 access time (TELQV), quiescent current (IDD2 and ISS2), and operating current (IDDOP) during 500 hours of 175°C demonstration testing are shown in Figures 5-5 to 5-8. Plots of 1802 Interrupt Hold at 10.0 Vdc (Int.Hold.2), quiescent current at 5.0 Vdc (ISS1), and propagation delay time at 5.5 Vdc (TPLH1-MWR) during 500 hours of 125°C demonstration testing are shown in Figures 5-9 to 5-11. The average parameter values ($\bar{x}$) and the average plus or minus one sigma values ($\bar{x} \pm \sigma$) annotated on the plots were computed using the data for all parts. Individual device performance by serial number is also illustrated in the plots. The two devices selected for plotting are those that exhibited the minimum and maximum values of the plotted parameters at the 168-hour interval of the demonstration test. Similar data ($\bar{x}$ and σ) is tabulated in Appendix D for all measured parameters of the demonstration test devices.

It is apparent from these plots (in conjunction with the control data shifts) that device parameters were stable throughout the demonstration test. Therefore, it is concluded that the parallel testing technique does not produce electrical overstress conditions which degrade device parameters with one possible exception. If a stuck-at-zero output failure occurs, the failed device could be further degraded due to excessive output current if it is left on test (See Section 4.1.5).

Continuous Monitoring - Initially, it was hoped that the DLTS continuous monitoring results could be used to determine whether there was any correlation between the interim/final device electrical measurements and the continuous monitoring results. Unfortunately, the lack of electrical test failures precluded any studies of potential correlation. However, no device that passed the electrical tests was flagged as a failure by the DLTS, which is evidence of the effectiveness of parallel continuous monitoring for error-free operation.

Although there were no failures flagged by the DLTS during the demonstration tests, the periodic S-A-0 and S-A-1 simulations provided assurance that the DLTS monitoring system was operating correctly. The monitoring system accurately detected and correctly displayed every 1802 and 6504 error that was simulated. However, on three occasions during the demonstration test, the monitoring system triggered on noise and produced "false halts." False halts are defined as occurrences of the detector triggering on noise when there is no device fault. The

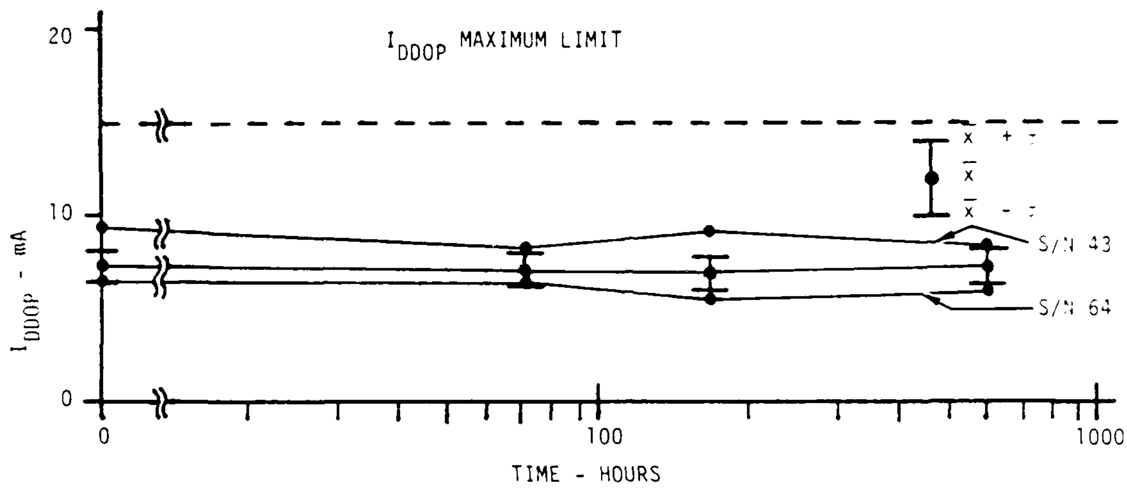


FIGURE 5-5. 6504 OPERATING CURRENT AT 5.5 Vdc AND 175°C

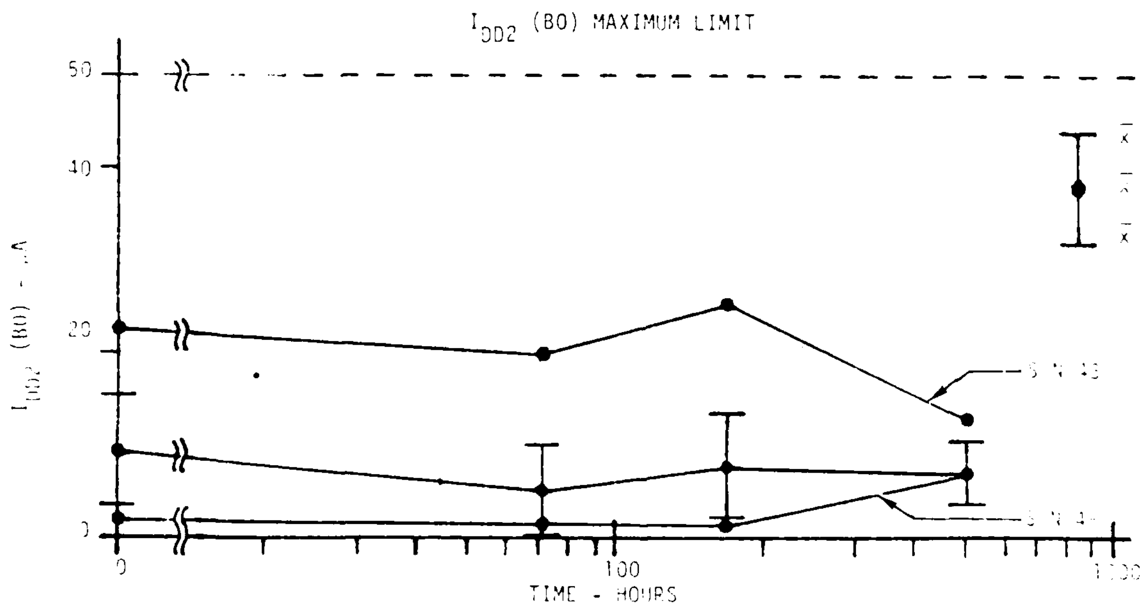


FIGURE 5-6. 6504 QUIESCENT CURRENT AT 5.5 Vdc AND 175°C

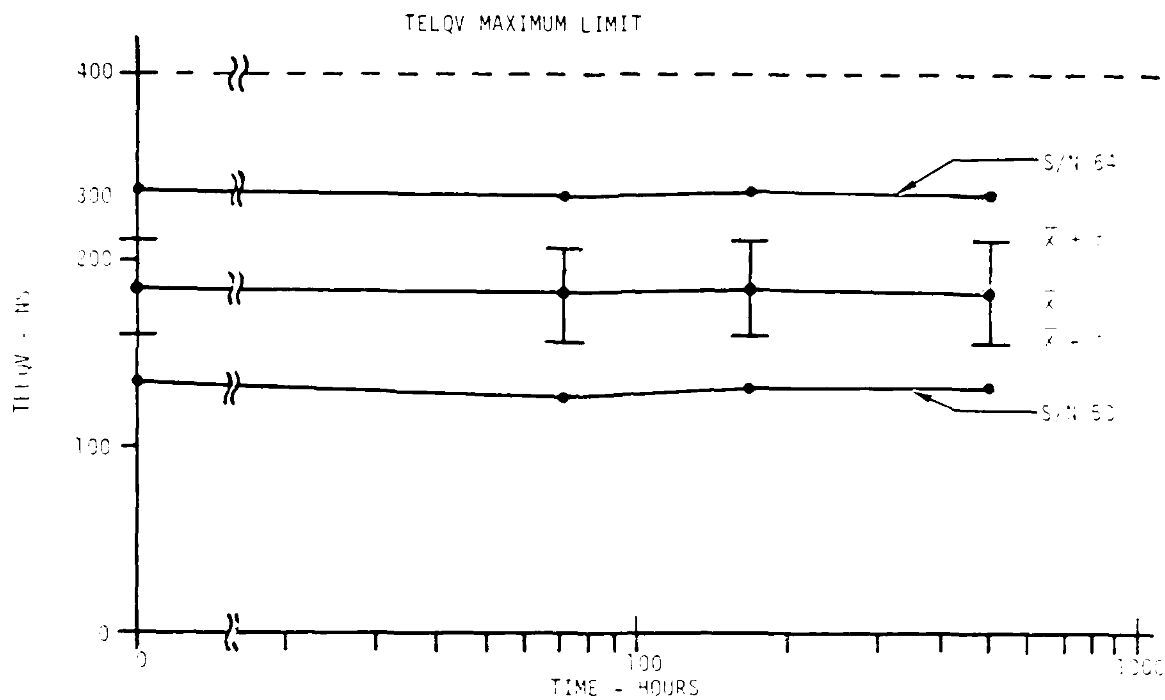


FIGURE 5-7. 6504 CHIP ENABLE ACCESS TIME AT 5.5 Vdc AND 175°C

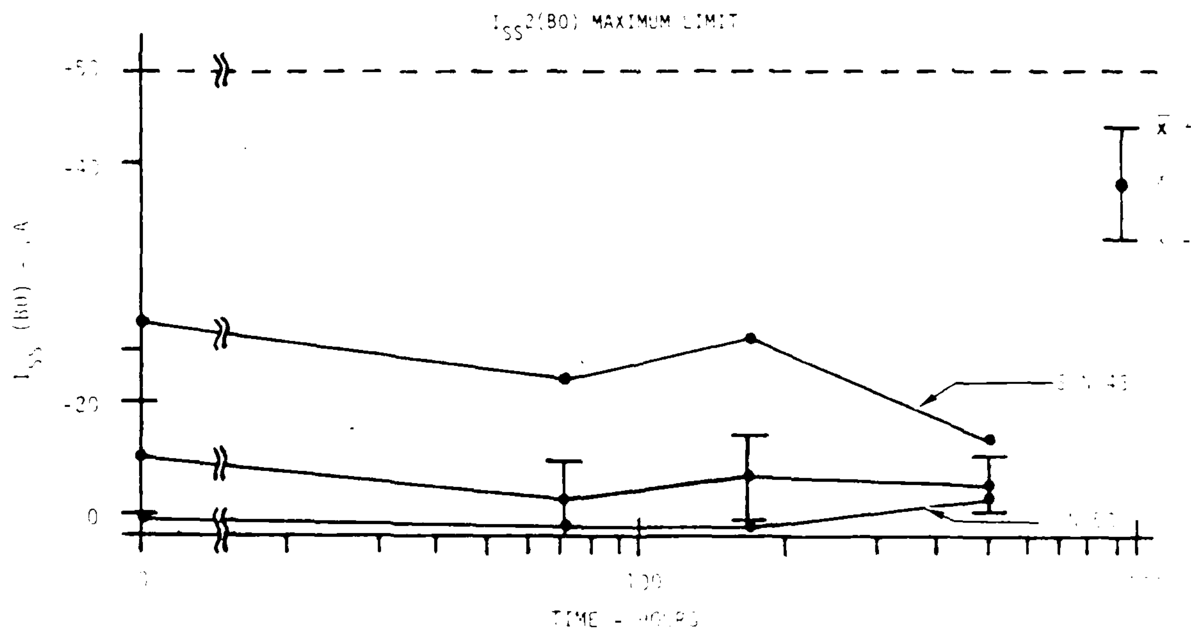


FIGURE 5-8. 6504 I_{SS2} (BO) CURRENT AT 5.5 Vdc AND 175°C

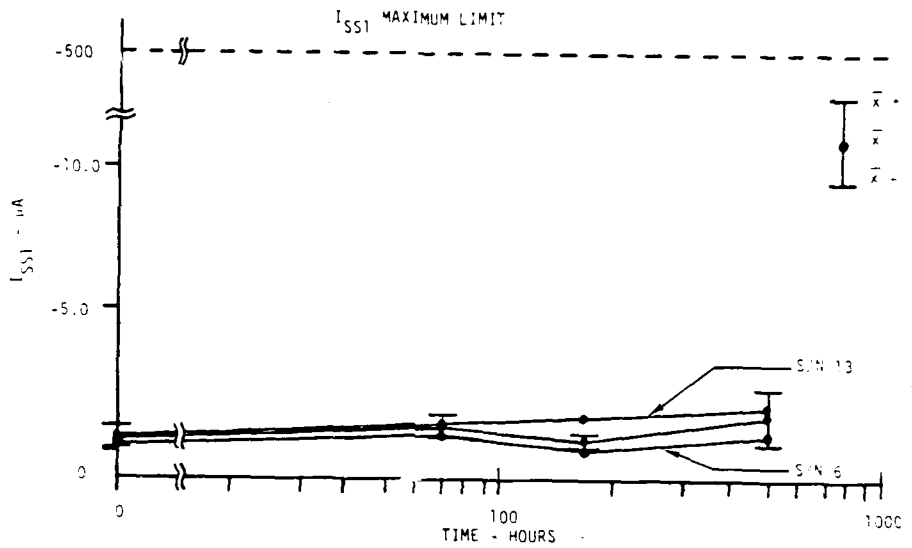


FIGURE 5-9. 1802 QUIESCENT CURRENT AT 5 Vdc AND 125°C

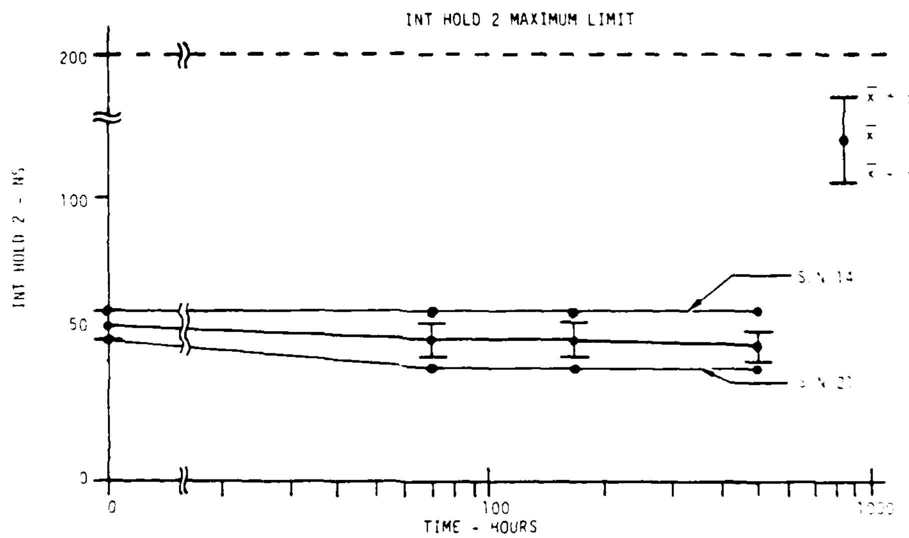


FIGURE 5-10. 1802 INTERRUPT HOLD AT 10 Vdc AND 125°C

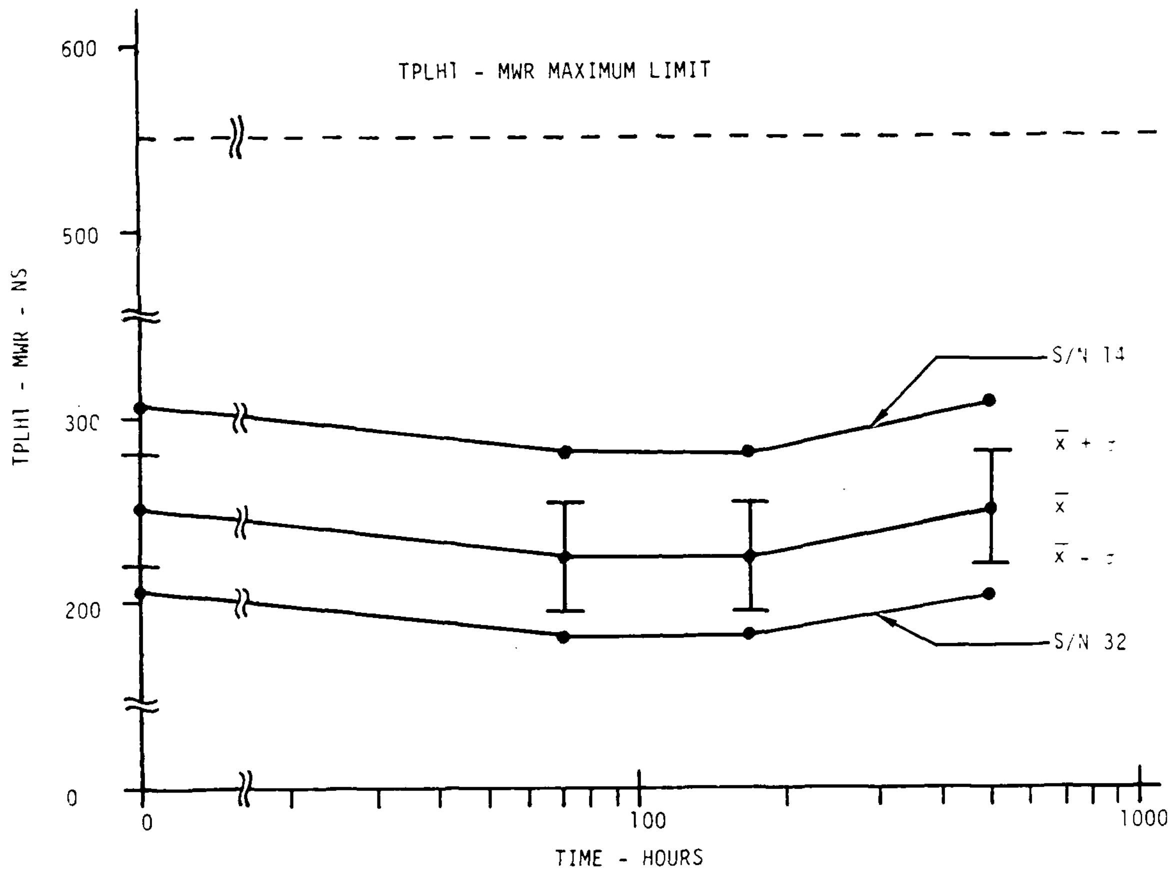


FIGURE 5-11. 1802 TPLH1-MEMORY WRITE AT 5.5 Vdc AND 125°C

false halts were due to a combination of: 1) the small 37 uA margin between the S-A-1 trigger level and the error-free background level, 2) slight drift in the current detector reference level, and 3) the noise level.

6.0 STAGE IV: FURTHER EVALUATION AND REFINEMENT

Results from the evaluations (Section 4) and the demonstration test (Section 5) were used to identify potential limitations of the parallel test method as implemented in this study. Other possible implementations of parallel testing not used in this study are also discussed. The hardware costs of parallel testing are compared to those for the standard comparator method and finally, steps to perform a parallel test are described.

6.1 POTENTIAL LIMITATIONS OF PARALLEL TESTING

Several potential limitations of parallel testing were noted in this study, some of which were related to the particular implementation of the parallel testing technique that was used for demonstration testing. The potential limitations noted during the study included latch-up and the severe test limitations required to prevent it, potential damage to failed devices left on test, difficulty in detecting open V_{DD} lines or open outputs, and stability of the current detector. These issues and the issue of unique test conditions for each device type are discussed in the following paragraphs.

Latch-Up Prevention - Latch-up was considered the most serious potential limitation, and preventing it required steps that reduced the effectiveness of parallel testing 1802 microprocessors. Prevention of latch-up for the 1802s required a reduction of the test ambient temperature from 175°C to 125°C, elimination of the NOP instruction, and limiting the matrix size to five parallel devices. Such severe restrictions were not necessary for parallel testing 6504 memories, and further evaluations are needed to establish suitable latch-up prevention techniques that will not limit the utility of the parallel test concept.

Damage to Failed Devices - Damage to failed devices left on test was another potential limitation. The possibility of device damage was reduced but not eliminated during this study by choosing a small matrix size.

Difficulty in Detecting Open Lines - Open power supply (V_{DD}) and device output lines were failure modes that were not detectable at the selected clock rates. Open V_{DD} lines were not detected because the difference between error-free background current (50 uA for the 1802) and zero current was too small to be distinguished by the detector. At higher clock rates, the background current would be large enough to be distinguished from zero current. The maximum clock rate is limited by a) detector speed and noise, which in turn are related to circuit time constants, and b) allowing sufficient time between clock cycles to freeze input signals at the conditions which resulted in an error detection.

Current Detector Stability - Although not anticipated at the onset, the demonstration test results suggested a need for greater stability in the current detector than was established during the pre-test evaluations. The need for greater stability arose from the small 37 uA margin between the 6504 S-A-1 level and the 6504 error-free background level. A change of 10 mV in the current detector voltage reference was enough to shift the current detector trigger level by 37 uA and this occurred three times during the demonstration test. The need for a highly stable current detector is expected to be a general requirement for parallel testing and not unique to the 6504 or the demonstration test configuration employed during this study.

In addition to the aforementioned potential limitations to the parallel test concept, the apparent requirement for tailoring test conditions to individual device type characteristics needs further evaluation. During this study, tailoring required numerous experiments to converge on test conditions and circuit values that allowed proper test and device operation. Parallel testing has not yet reached the point that a recipe may be used in lieu of judgment because of the contradictory and interdependent requirements (e.g., latch-up prevention and fault detectability).

Possible solutions to the first four problem areas in this section are described in Section 6.2.1.

6.2 IMPROVEMENTS AND ALTERNATIVES

Several refinements to the demonstration parallel test hardware and software were suggested by the evaluations (Section 4) and the demonstration test (Section 5). These refinements, if fully developed, may resolve the parallel test limitations noted earlier. In addition, other implementations of the parallel test method not used in the demonstration test are discussed in this section.

6.2.1 Suggested Improvements

This section describes solutions to problems noted in Section 6.1. Included are improvements for latch-up prevention, protecting failed devices from damage, detecting open power supply or DUT outputs, and current detector stability and utility. A buffered output technique which solves many of these problems but introduces others is also described.

Improvements to prevent latch-up must take a high place on the priority list. One technique for latch-up prevention suggested by RADC is to use an emitter follower in place of the R_{PS} resistor. The emitter follower would maintain its emitter voltage at a set value despite current fluctuations until the current reaches a set high level so that the transistor is saturated, at which time the current would be limited and the emitter voltage would drop. The emitter follower transistor base would be connected to a voltage divider or other voltage reference to establish the desired V_{DD} level. A resistor in the collector circuit would establish the current saturation level and also serve as a current sensing resistor. This technique shows promise and should receive further evaluation.

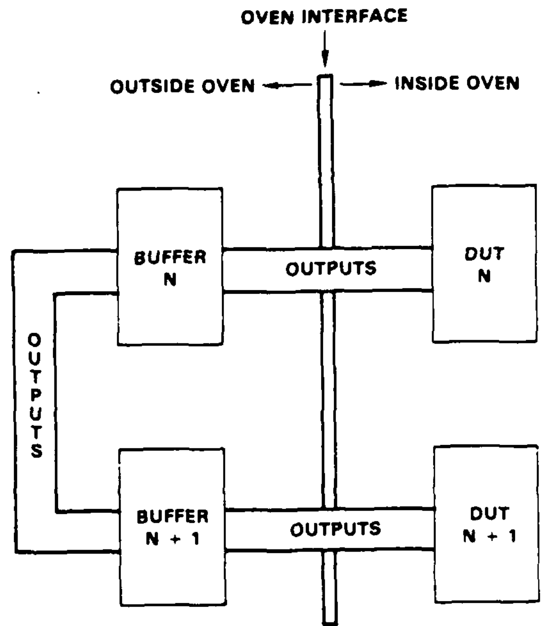
Protecting failed devices from damage due to excessive currents could be done by limiting the output current. The buffered output, discussed later, is one such method. Another is to insert resistors in the outputs before they are connected together. This method was considered for the demonstration test and dismissed because of the large number of resistors required--one per output for the 1802 results in 675 resistors for a single test chassis of 25 DUTs. However, this approach may now be practical since high temperature sockets with provisions for mounting resistors vertically on the socket have recently become available. The output resistor approach is feasible with or without the special sockets but it results in added high temperature board complexity and cost.

The detection of power supply opens can be accomplished by temporarily increasing the clock rate under software control. As noted in Section 4.1.9, the background current increases with clock rate, reaching relatively high values. The DUT V_{DD} and V_{SS} voltages could be measured sequentially and the values processed to identify an open power supply. This method requires a "smart" system to automatically increase the clock rate, make the voltage measurements, and process the data.

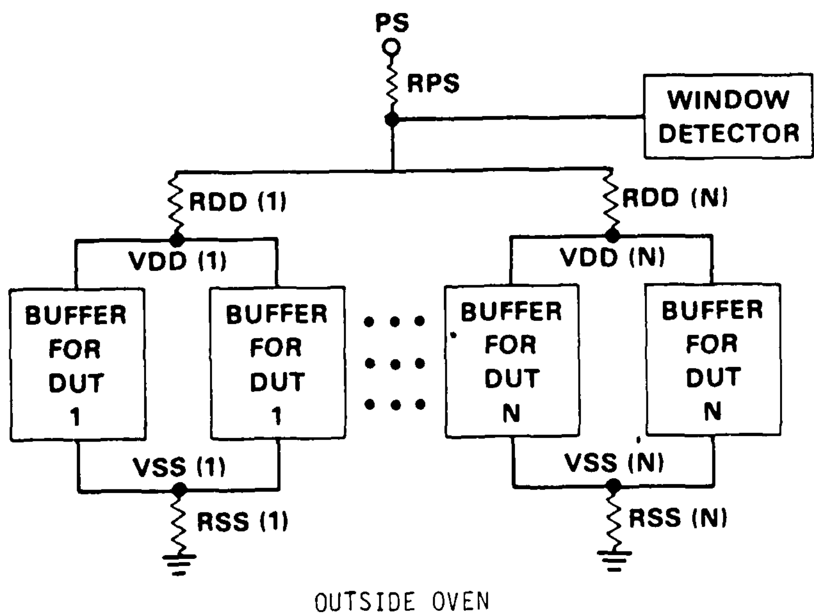
Open device outputs could be detected by adding output buffers and by using the following procedure. First, a separate buffer output is connected to each set of corresponding output pins. Next, the driver is halted to a preset instruction cycle such that the correct output states are known. Then each buffer is individually forced to its complement logic state on its corresponding outputs. If the correct output state is low, the complement buffer will source current to the devices whose outputs are correctly low. If the correct output state is high, the complement buffer will sink current from the devices whose outputs are correctly high. In either case, the I_{DD} or I_{SS} currents for the device whose output is open will be different and can be identified by measuring I_{DD} and I_{SS} currents for all DUTs.

The current detector could be improved by stabilizing the power supply, providing a more stable reference voltage, and providing a false halt indicator. The threshold for detection of S-A-1s in the demonstration system was so critical that 10 mV drifts in power supply or voltage reference caused false halts during the 500-hour demonstration test. An on-board power supply regulator and a stabilized voltage reference for the detector comparators should eliminate this problem. Finally, a false halt indicator is needed to flag the particular detector (out of five or ten on a chassis) that requires adjustment and to aid in test setup.

Both latch-up and device output damage may be prevented by buffering the outputs as shown in Figure 6-1. In this technique, each output line is connected to a buffer. Then the corresponding buffer outputs are connected together. Operation is the same as for the one-detector-per-matrix method described in Section 4.1.2 except that V_{DD} and V_{SS} voltages are measured on the buffers rather than the DUTs.



BLOCK DIAGRAM



OUTSIDE OVEN

FIGURE 6-1. BUFFERED PARALLEL CONCEPT

A primary advantage of the buffered technique is that technologies other than CMOS can be tested, provided that they are compatible with the CMOS buffers. Also, DUT latch-up is reduced or eliminated because the V_{DD} voltage level on the DUTs will not be pulled down during S-A-0s or S-A-1s (V_{DD} for the buffers will be pulled down). In addition, S-A-0 and S-A-1 DUT output damage is eliminated because the CMOS buffers isolate the corresponding DUT outputs (the buffer outputs could be damaged, but operating the buffers at a lower ambient temperature (25°C) should reduce the potential for damage). Another advantage is that experiments to establish the circuit conditions for all combinations of detectable faults (to be used by the fault detecting isolation system) are reduced because these need only be performed on the buffers once for each different number of DUT outputs. The buffered technique is also less expensive than the comparator method for multi-output devices (see Section 6.3).

Disadvantages of using the buffered parallel technique are that it is costly (each output line must be buffered) and it may require large numbers of wires through the oven interface. There would be 675 wires required for twenty-five 1802s. Although the number of wires through the oven interface could be reduced by placing the buffers inside the oven, this is not recommended because it would subject the buffers to high temperature stress.

6.2.2 Other Interconnect Schemes

Interconnect schemes different than the one used in the demonstration test may eliminate some of the problems previously discussed. However, all of these would require an evaluation similar to the one described in Sections 4 and 5 of this report. The term "interconnect schemes" as used here refers primarily to failure detection and isolation. The interconnect schemes discussed below are the Column/Row Scheme (suggested by RADC), the Two-Detectors-Per-Device Technique, and the Multiplexed Detector Scheme.

The distinguishing feature of the column/row interconnect scheme is that there are column current detectors and row current detectors. The DUTs are arranged in a N by M matrix so that each matrix column is formed by connecting appropriate DUT V_{DD} lines to a current detector and each matrix row is formed by connecting appropriate DUT V_{SS} lines to a current detector (Figure 6-2). Both the failure indication and identification of the failed device would be noted by the simultaneous

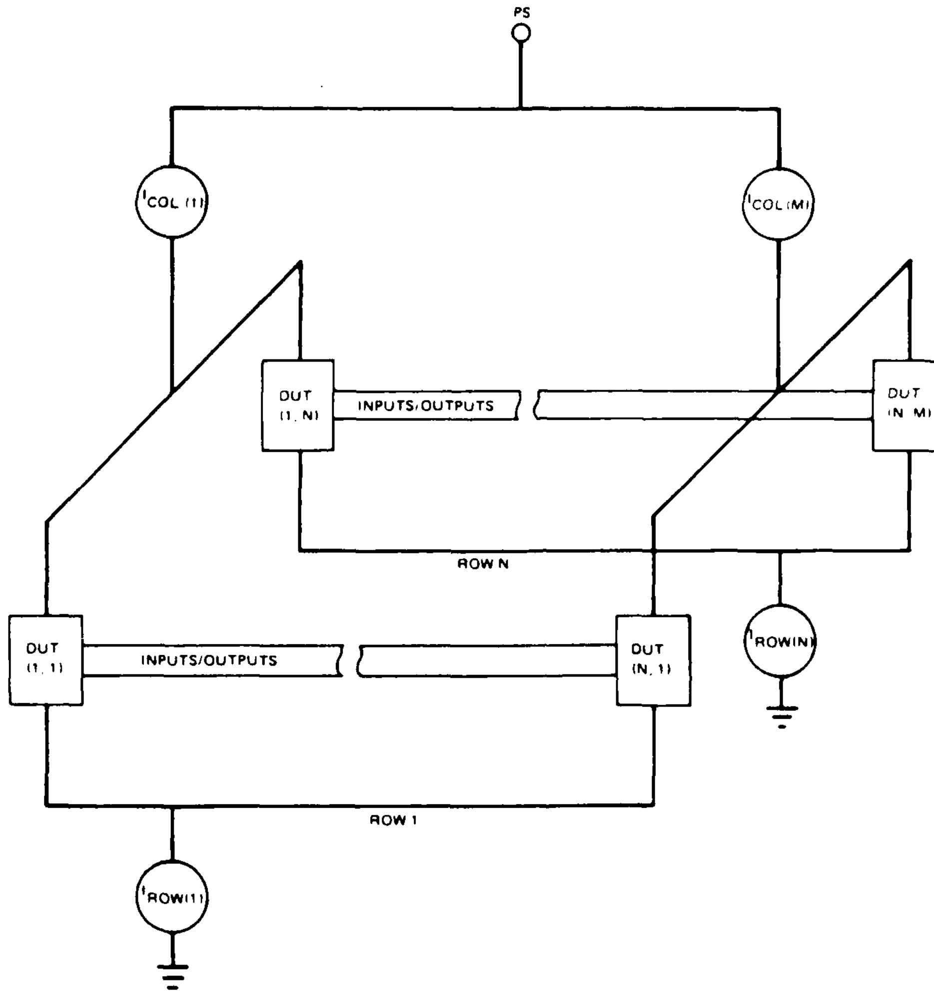


FIGURE 6-2. COLUMN/ROW INTERCONNECT SCHEME

detection of abnormal currents on specific row(s) and column(s). Failure identification could be performed by high speed logic on the test chassis or the individual detector indications could be latched for future interrogation and analysis by a "smart" system. One could also halt the driver so that the failed state is preserved, sequentially measure the voltage levels on each DUT at V_{DD} and V_{SS}, and then process this information in the "smart" system to identify the failed DUT. Further investigation of hardware cost, software cost, and the effectiveness of each of these variations is required to select the best method.

The advantages of the column/row method are speed and potentially low cost. The number of required detectors increases only as the square root of the number of DUTs. For example, a 25 device column/row scheme would require 10 detectors, but a 100 device scheme would require only 20 detectors. However, this method will have many of the same difficulties we encountered in the one-detector-per-matrix scheme. These include the difficulty in detecting S-A-0s on certain device types (such as the 6504), latch-up problems, and potential output damage to failed devices left on test. Still, the column/row scheme's potential speed and cost advantages warrant further investigation.

The two-detector-per-device method, as the name implies, utilizes two current detectors, one on the V_{DD} line and one on the V_{SS} line of each DUT. This method was discussed in Section 4.1.2 where it was noted that under some multiple failure conditions, a S-A-1 would not be detected, a clear disadvantage of the method. To fully develop the method would require a similar process of component and test condition evaluation as performed in Section 4. The advantages of this method include minimum software for failure detection/identification and speed. The disadvantages include hardware complexity, hardware cost (two detectors per DUT at approximately $60 per detector), and possible inability to detect certain kinds of failures. Overall, we do not consider this method to be as cost-effective as the one used in this study.

The multiplexed-detector scheme must be used in conjunction with an interconnect scheme similiar to the one-detector-per-matrix technique. In the one-detector-per matrix technique, we used one detector to sense an abnormal supply current to five paralleled devices. Once the current detector halted the

driver, the DLTS sequentially measured the V_{DD} and V_{SS} levels, then processed this information to identify the failed device. In the multiplexed detector scheme, the driver would be halted as before, but a current detector would examine the device current levels (I_{DD} and I_{SS}) and provide an output for each abnormal individual device current. This method provides direct identification of the failed device, but it has the same shortcoming in terms of failed device identification for multiple failures as the two-detector-per-device method. While this approach has about the same hardware complexity as the failure identification method we used, it cannot identify as many multiple failures, so it is not recommended.

6.3 COST COMPARISONS

The hardware costs of two parallel testing methods were compared with the equivalent costs for the conventional (comparator) method in order to estimate the cost advantage, if any. Two parameters were varied for the cost comparisons: number of DUTs per chassis and number of outputs per device. The results show that parallel testing offers: a) a large cost advantage for multiple output devices, b) an increasing cost advantage as number of DUTs per chassis increase, and c) little or no cost advantage for single output devices. The methods used to compute the hardware costs and make the comparisons are provided in the following paragraphs.

Normalized costs for the components which make up the chassis hardware for the comparator, one-detector-per-matrix*, and buffered parallel methods are listed in Table 6-1. The costs of each component in Table 6-1 are based on the estimated number of manhours needed to build that component. The estimated cost percentage values for each component listed in the table are expressed as a percent of total chassis cost for each test method. The normalized total cost is computed by dividing the total cost for each chassis by the total cost for the 25-part comparator method.

*The cost of the column/row Interconnect Scheme discussed in Section 6.2.2 would be similar to the cost of the one-detector-per-matrix scheme except for a small added cost for the additional current detectors.

TABLE 6-1. ESTIMATED COST PERCENTAGE PER COMPONENT FOR DIFFERENT CHASSIS TYPES

6504								
	25 DUTs					100 DUTs		
COMPONENT	COMPARATOR	PARALLEL		BUFFERED PARALLEL 1/		COMPARATOR	PARALLEL	BUFFERED PARALLEL
	25	5x5	25x1	5x5	25x1	100	100x1 1/	100 x1 1/
DRIVER	15.9	14.8	15.9	12.9	13.6	8.8	10.9	7.3
CONTROL	3.2	3.0	3.2	2.6	2.7	1.8	2.2	1.5
MONITOR	12.7	9.3	3.2	18.5	14.3	22.0	2.2	25.2
MULTIPLEXER	6.3	5.9	6.3	7.0	8.2	11.0	8.7	14.7
INTERFACE/ERROR	0.0	8.9	9.5	7.8	8.2	0.0	6.5	4.4
CABLE	2.4	2.2	2.4	1.9	2.0	1.3	1.6	1.1
CHASSIS	59.5	55.9	59.5	48.5	51.0	55.1	67.9	45.8
TOTAL 3/	1.0	1.1	1.0	1.2	1.2	1.8	1.5	2.2

1802								
	25 DUTs					100 DUTs		
COMPONENT	COMPARATOR	PARALLEL		BUFFERED PARALLEL 1/		COMPARATOR	PARALLEL	BUFFERED PARALLEL
	25	5x5	25x1	5x5	25x1	100 2/	100x1 1/	100x1 2/
DRIVER	4.1	13.2	14.8	6.0	6.3	1.3	8.4	2.4
CONTROL	0.8	2.6	3.0	1.2	1.3	0.3	1.7	0.5
MONITOR	51.5	9.9	3.7	23.7	21.7	64.4	2.1	31.1
MULTIPLEXER	1.6	5.3	5.9	3.6	3.8	1.5	8.4	4.8
INTERFACE/ERROR	0.0	10.6	7.4	4.8	3.1	0.0	4.2	1.2
CABLE	0.6	2.0	2.2	0.9	0.9	0.2	1.3	0.4
CHASSIS	41.4	56.4	63.0	59.8	62.9	32.2	73.9	59.6
TOTAL 3/	3.3	1.2	1.1	2.6	2.5	12.3	1.9	6.6

NOTES:

1/ HAVE NOT BEEN EXPERIMENTALLY DEMONSTRATED.
2/ NOT FEASIBLE DUE TO THE LARGE NUMBER OF WIRES NEEDED TO MONITOR ALL OUTPUTS.
3/ TOTAL RELATIVE COST BASED ON CONVENTIONAL 6504 CHASSIS WITH 25 PARTS.

The comparator method is treated as the baseline for monitored testing. In the comparator method, the outputs of each DUT are compared with known good outputs by means of comparators, which output a signal if an error occurs.

For a multiple-output device (1802), the table indicates a substantial cost advantage for parallel testing over the comparator method, as shown by the following example. The "Total" line for 1802s indicates that a 25-part 1802 chassis using comparators costs 3.8 times as much as a 25-part 6504 chassis using comparators. Similarly, a parallel method (one-detector-per-matrix) chassis for the five groups (matrices) of five paralleled DUTs would cost 1.2 times the 6504 25-part comparator chassis. A savings of 71% is thus indicated for the parallel method over the comparator method for a 25-part chassis, i.e., (1.0-1.2/3.8) x 100 = 71%. By similar arguments and calculations, it can be shown that the buffered parallel method saves 31% over the comparator method for a 25-part 1802 chassis.

For all of the monitoring methods, and for both single and multiple output devices, the results of Table 6-1 indicate that the hardware cost per DUT decreases as the number of DUTs per chassis increases. This may be seen by comparing the 25-DUT and 100-DUT normalized total costs for any of the monitoring methods.

For a single-output device, such as the 6504, there is very little hardware cost difference between monitoring methods for a 25-part chassis. However, for a 100-part chassis, the parallel method offers a small (17%) savings over the comparator method.

For the component percentage values for each monitoring method, the following explanation and observations will assist in interpreting the Table 6-1 entries:

1) The components have both fixed and variable costs. The fixed cost items include the driver board, control board, and cable, whose costs are constant for up to 100 DUTs. The variable cost items include the monitor board (comparators or current detectors), A/D multiplexer board, interface/error board, and chassis fabrication, whose costs vary as a function of number of DUTs and test method.

AD-A150 237 PARALLEL TEST METHOD FOR LSI (LARGE SCALE INTEGRATION) 2/2
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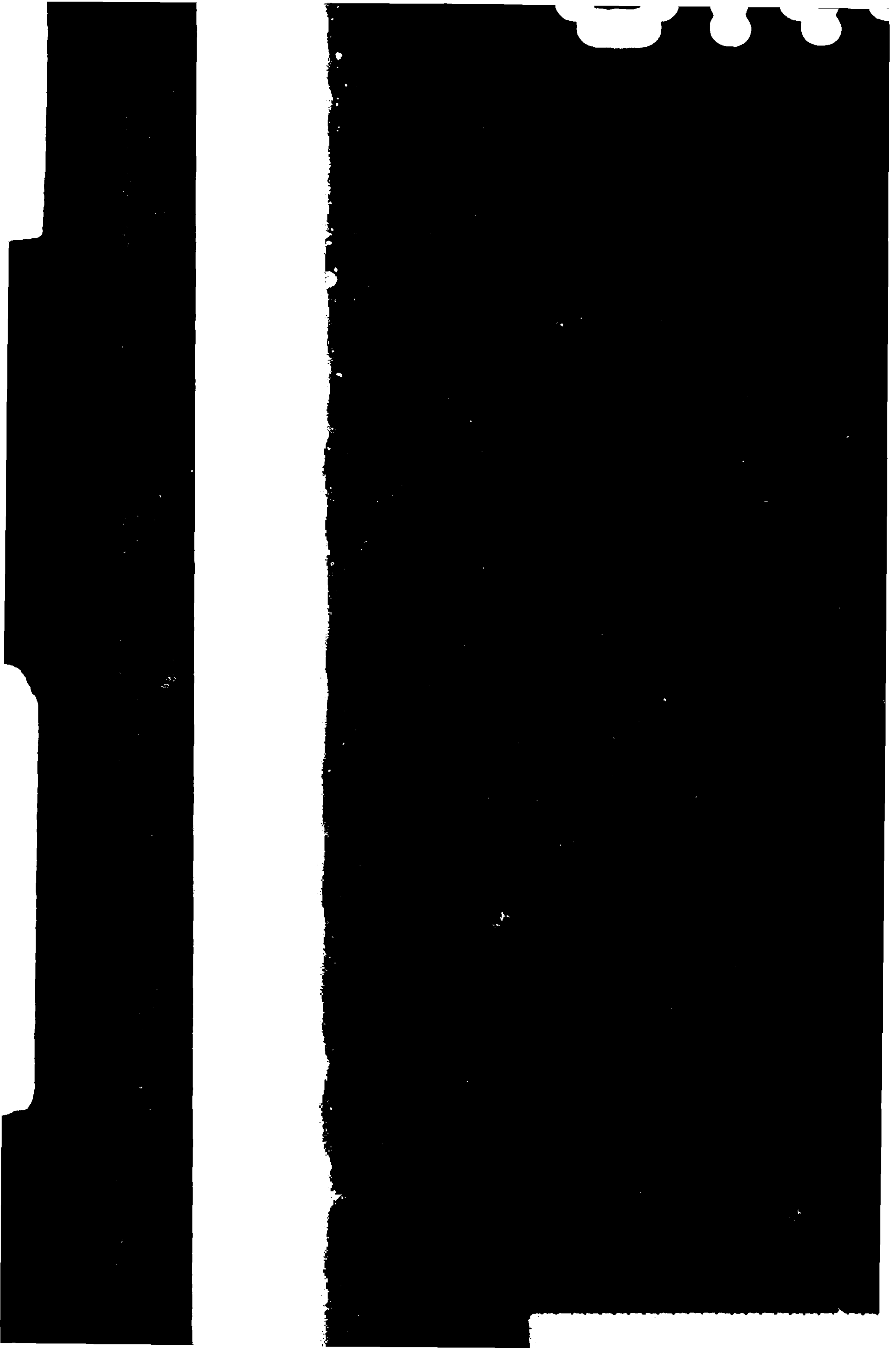

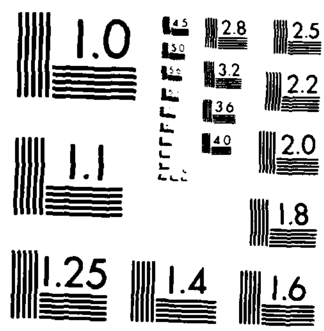

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

2) For chassis that use the comparator test architecture, the cost to build the monitor component was one of the largest expenses. This was especially true for the 25 part and the 100 part 1802 comparator chassis, where 52% and 64% of the total chassis cost was for the monitor component.

3) Compared to the comparator method, the one-detector-per-matrix method gains most of its savings from the less complex monitor board (no comparators) and from reduced chassis fabrication. This savings is slightly offset by the increased cost of adding the interface/error board, more A/D multiplexers (1802 only), and window detectors.

6.4 A SEQUENCE OF STEPS FOR PERFORMING PARALLEL TESTING ON A PARTICULAR DEVICE

One objective of this program was to formulate a procedure that could be used to determine parallel test conditions. A suggested procedure is shown in the flow chart of Figure 6-3. The flow chart can be divided into three parts: the initial experiments, the adjustment of test conditions, and the optional worst case output circuit potential damage experiment.

The initial experiments include six tasks: 1) building the hardware (the driver, the current detector, and the error simulator), 2) characterizing operating current as a function of clock rate and temperature, 3) characterizing latch-up with temperature, 4) characterizing output currents with temperature, 5) characterizing device output damage, latch-up, noise, and ability to detect failures as a function of matrix size, and 6) selecting initial matrix size, V_{DD}, clock rate, input levels, resistor values, and temperature.

The test circuits should be designed so that it is easy to replace resistor and capacitor components. Also, the chassis should be wired for the maximum number of DUTS that are desired per matrix. The number of DUTS in a matrix can easily be reduced later if necessary to meet revised test conditions.

When characterizing the operating current as a function of temperature, the experiment should be performed over a wide range of clock rates. Also, the output current characterization should be performed using R_{DD} resistor values ranging from 2 ohms to the maximum expected R_{DD} value. The initial matrix

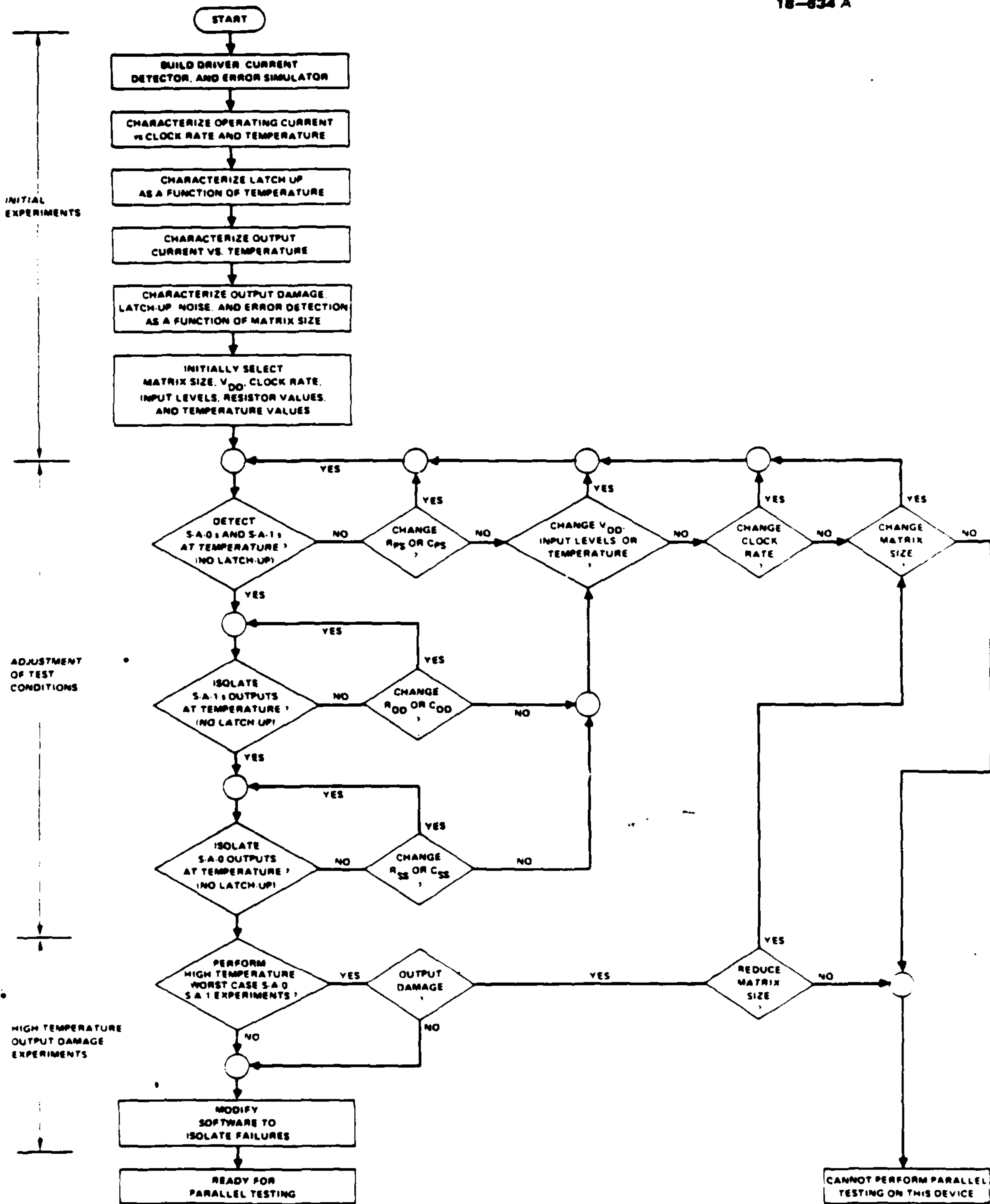

FIGURE 6-3. A SEQUENCE OF STEPS FOR PERFORMING PARALLEL TESTING ON A PARTICULAR DEVICE

size should be as large as possible while also consistent with prevention of device output damage and latch-up, acceptable noise levels, ability to thoroughly exercise the devices, and ability to detect and isolate failures. The initial V_{DD} and input voltage levels, resistor values, and temperature should be determined using methods that are followed for other types of high temperature functional testing (Reference 5).

The second division of the flow chart pertains to adjusting the non-component items (the matrix size, clock rate, V_{DD} voltage level, ambient test temperature, and high input voltage levels), resistor values (R_{PS}, R_{DD}, and R_{SS}), and capacitor values (C_{PS}, C_{DD}, and C_{SS}).

The matrix size represents the number of devices in the chassis whose corresponding inputs and outputs are connected in parallel. After combinations of the other items mentioned above have been exhausted for latch-up prevention, the matrix size could be reduced to decrease the amount V_{DD} will fall during a fault state. The clock rate could be reduced if the time constant for changes in the V_{RPS} voltage level was too long for V_{RPS} to reach its error level and be detected as an error during the cycle in which it occurred. Next, the V_{IH} levels should be set at a voltage level so that the DUTS will operate correctly yet avoid latch-up by staying below the V_{DD} voltage level under the worst case output error condition. The V_{DD} voltage level and the ambient test temperature may be adjusted to prevent latch-up but should be the last parameters changed because these conditions provide the maximum stress to the DUT.

The R_{PS}, R_{DD}, and R_{SS} values affect the supply voltage levels, ability to detect faults, and latch-up threshold. The R_{PS} value should be increased if functional errors have not been detected by the current detector. The value of R_{PS} should be the minimum value required to reliably detect functional errors. Next, the R_{DD} resistor value could be adjusted if required. To provide maximum current limiting, R_{DD} should be selected as the largest value possible without causing V_{DD} to drop below the latch-up threshold. R_{DD} must also be sufficiently large that S-A-1 failures can be isolated. Next, the R_{SS} resistor value may need to be increased to isolate a stuck-at-zero condition. R_{SS} should be the minimum value required to isolate S-A-0s.

Capacitance values affect the noise on the voltage lines and the V_{RPS} voltage decay time when a functional error occurs (assume the capacitors are tied to ground). Increasing any capacitance value (C_{PS}, C_{DD}, and C_{SS}) will reduce the amount of noise where it is connected. Decreasing the C_{PS} and C_{DD} values will allow the V_{RPS} voltage to discharge faster, which may be necessary so that a functional error can be detected in the cycle in which it occurs. This choice must be traded off against the choice of clock rate, which in turn affects the ability to detect V_{DD} opens.

The third division of the flow chart consists of the optional, high temperature, worst case S-A-0 and S-A-1 experiment needed for burn-in and life testing. This experiment need not be performed for burn-in if damage to device outputs is not a concern. On the other hand, the experiment is necessary for life testing because damage to the device outputs may prevent isolating the failure mechanism, an essential feature of life testing. If damaging failed device output currents are measured in this experiment, then other circuitry must be added to limit them or a provision must be made to remove failed devices from test.

7.0 SUMMARY AND CONCLUSIONS

This study has shown that parallel testing works for the CMOS memory and microprocessor used to evaluate the method. However, there were problems with latch-up prevention and potential damage to failed devices left on test for the implementation selected for this study.

Twenty-five 4K memories were operated in a parallel configuration of five groups of five devices for 500 hours at 175°C. Similarly, twenty-five 8-bit microprocessors were operated in a parallel configuration of five groups of five devices for 500 hours at 125°C. The fault detection and isolation system worked for single S-A-0 and S-A-1 failures as demonstrated by simulations. However, on three occasions during the demonstration test, the monitoring system triggered on noise and produced false halts. The false halts were due to a combination of: 1) the small 37 uA margin between the S-A-1 trigger level and the error-free background level for the memory devices, 2) slight drift in the current detector reference level, and 3) the noise level. The current detector stability required to eliminate this false halt problem is achievable and should not be a fundamental limitation to parallel testing.

Preventing latch-up on the microprocessor required limiting the test temperature to 125°C and deleting the NOP instruction. Latch-up was prevented in the memory by limiting the number of paralleled devices to five and by providing sufficient noise margin between the input high voltage level and the operating error-free supply level.

The high probability of damage to failed devices left on test was determined from simulation of worst case currents expected for the selected parallel test configuration. These currents exceeded the manufacturer's output current ratings on both the memory and the microprocessor, but tests showed that only the microprocessor was likely to be damaged. Protection to failed devices was not provided in the demonstration test except to remove the failed device from the test. However, no failures occurred and therefore no devices were damaged. The issue of preventing further damage to failed devices is crucial in a life test because further damage could prevent determination of the cause of failure.

The particular implementation of the parallel test method selected for this study was based primarily on the maximum interaction between paralleled devices that could be tolerated. The interaction between paralleled devices (such as noise and fault current) was a function of the number of paralleled devices, clock rate, and circuit voltage, resistance, and capacitance values. The choices for these parameters (number of parallel devices, clock rate, and circuit values) were driven primarily by such considerations as fault detectability, latch-up prevention and minimization of damage to failed devices. Other implementations of the parallel test method, other methods for detecting and isolating faults, and other methods for latch-up and damage prevention were noted in the course of this study. The most promising of these methods, discussed in Section 6, should be evaluated.

Achieving broad applicability for the parallel testing method will require that economical solutions be found for the latch-up and potential damage problems. This study has served to illuminate these problems and to suggest possible solutions for them so that future studies of the parallel testing method may focus attention where needed most.

8.0 REFERENCES

1. R. A. Blore, "Parallel Technique for Reliability Testing of CMOS Microcircuits," Government Microcircuit Applications Conference, November 1980.

2. R. A. Blore, "Parallel Testing for CMOS Microcircuits," International Symposium for Testing and Failure Analysis, October 1980.

3. V. A. Weissflug and M. C. Roberts, "Reliability Assessment of CMOS LSI Memories," (Contract No. F30602-79-C-0194) RADC-TR-82-146, May 1982.

4. M. Simons, "Transient Surface Damage and Latch-Up in CMOS Devices," RTI 43U-991, June 1975.

5. G. M. Johnson, "Evaluation of Microcircuit Accelerated Test Techniques," RADC-TR-76-218, July 1976, Section 4.

REFERENCE MILITARY DOCUMENTS

MIL-M-38510 - Military Specifications, Microcircuits, General Specifications.

MIL-M-38510/239 - Military Specification, Microcircuits, Digital, CMOS 1024 Bit Random Access Memory (RAM) Monolithic Silicon, dated 2 January 1980.

MIL-M-38510/470 - Military Specification, Microcircuits, Digital, CMOS (Fixed Instruction), Monolithic 8-Bit Microprocessor, dated 16 April 1979.

MIL-STD-833B, Military Standard; Test Methods and Procedures for Microelectronics.

APPENDIX A

RE-PRINTED PAPER

PARALLEL TECHNIQUE FOR RELIABILITY TESTING
OF CMOS MICROCIRCUITS

GOMAC-80

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Parallel Technique for Reliability Testing of CMOS Microcircuits

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Summary

A technique for performing continuously monitored reliability stress tests with greatly reduced hardware requirements is presented. This paper includes concept, implementation, experimental results, and applications.

Introduction

Screening and reliability stress testing are essential elements of producing and procuring reliable semiconductors. While the military has been the primary mover there is a growing concern even in consumer oriented goods for reliability assurance of semiconductors before they enter systems or become field failures. This increased interest and the increased capabilities and complexities of modern semiconductors have created a significant challenge for testing. Requirements to test two input NOR gates have now evolved to testing microcomputers. Fortunately, the time required to perform parametric tests such as leakage and output drive measurements has remained essentially constant and relatively short. However, verification of functionality is no longer trivial. To run a GALPAT pattern on a 16K RAM with a cycle time of 375ns can take six to seven minutes for one pass. To measure even a small number of parts with different voltages and patterns is consequently very expensive. Functional testing can, however, be performed during burn-in time. While only a few minutes can be afforded on an automated tester the devices are captive in a burn-in chamber for perhaps 168 hours. Such testing requires the capability to monitor the device outputs hence the term "monitored testing".

One method useful for performing monitored testing involves a comparator on every output line of every device allowing concurrent and continuous monitoring of the devices under test. While this approach satisfies the requirement for monitoring, it quickly involves a lot of hardware and expense. Generally, the more complex the device, the more output lines there are to be monitored and the more comparators are required. An increase in the number of devices under test multiplies the number of comparators again. Unless the comparators are contained in the stress chamber along with the devices the outputs of each device must be brought out of the test chamber. This approach quickly involves significant amounts of hardware. As the future holds VHSIC devices of perhaps 128 or 256 pins the comparator approach will become very awkward.

The key element of the comparator approach is the comparator which performs two functions: (1) comparison of two signals and (2) provision of an indicator when the two signals disagree. Parallel testing is a technique which performs the same functions but significantly reduces the support hardware.

Concept

In the parallel technique all corresponding inputs and outputs of all devices under test are tied in parallel. This is illustrated in Figure 1. Every output of any one of the n individual devices under test is therefore constantly compared to the corresponding output of the other n-1 devices. When all devices agree on all lines the supply current will be minimal. However, a disagreement, i.e. a failure, will result in a potential difference and significantly increased current. The key features of comparison of signals and indication of a disagreement are thereby accomplished without the use of external comparators.

There are some important features of such a technique.

1. As opposed to the comparator approach which requires a comparator for each output, the parallel technique is essentially independent of device size. Testing a device such as a microprocessor with eighteen outputs requires no more hardware than testing a NOR gate.

2. In the comparator technique a failure of the comparator is a failure of the support electronics and will cause the loss of data on the devices under test. For the parallel technique, a failure of the "comparator" is in fact what you are testing for since it is actually the device under test.

3. Since the devices under test are also the comparators the outputs of each device under test need not be brought out of the test chamber.

Implementation

At RADC this technique is being developed utilizing CMOS devices. CMOS has three features particularly suitable for the implememtation: (1) low standby power supply current, (2) relatively low impedance balanced output drive, and (3) static circuitry.

The supply leakage current of a CMOS LSI circuit is expected to be on the order of microamperes. The current drive capability is usually milliamperes. It is apparent that even for a large number of devices under test there are perhaps two orders of magnitude difference in currents between conditions of agreement and disagreement.

The third feature, static circuitry, is useful in attempting to "freeze" the conditions relating to the failure situation for real time analysis and verification.

The implementation at RADC thus far has taken the form illustrated in Figure 2. Corresponding inputs and outputs have been tied together. The power supply

lines, VDD and VSS, through which all the currents for each device must flow have also been tied together. In the common VDD supply line is a current detector which is capable of differentiating between normal currents and currents resulting from a failure situation. The current detector, illustrated in Figure 3, consists of a differential voltage comparator monitoring the voltage across a 1 ohm, one percent, carbon film resistor. The output of the detector toggles states in response to the increased current through the sense resistor when a failure occurs.

Referring to Figure 2 again, note the inclusion of sense resistors in the VDD and VSS supply lines of each device. On error, a voltage is developed across one of these sense resistors. A multiplexed analog to digital (A/D) converter is used to measure the voltage drop. It is thereby possible to determine which device is the failed unit and furthermore which logic state the failure is.

An example should clarify the operation. If device n_i fails by having a logic low state on a given output line when the other n-1 devices have a logic high state then a failure current, I_f, will flow through the current detector causing an alarm and initiating the A/D routine. The n-1 good devices will each source the current $I_f/(n-1)$. However, device n_i will singularly sink the total failure current, I_f, through its VSS sense resistor. Results from the A/D identify device n_i as at fault and by determining that the VSS sense resistor was identified indicates that the fault is a logic low which should have been high.

A similar construct can be made for a faulty device pin being high when the corresponding pins on the other n-1 devices are low.

Experimental Results

Experiments have been performed on 4001 and 1852 type CMOS devices. The 4001 is a quad two-input NOR circuit and the 1852 is an input/output port of the 1800 series microprocessor family. There were two 4001 experiments. In the first, a single 4001 was used with the outputs of all four gates tied together. The inputs were configured to force one output to the alternate logic state of the other three. The supply voltage was then varied and the supply current monitored. Results are shown in Table 1. Note that currents for both logic faults are comparable.

The second 4001 experiment utilized nineteen devices configured in parallel. A switch was included to cause the output of one gate (one of 76) to: (1) operate normally, (2) be forced high, or (3) be forced low. This experiment conducted at room temperature and 5 volts indicated standby currents of <0.05 milliamperes and failure currents of 2-4 milliamperes; two orders of magnitude difference. These two experiments indicated that it is possible to differentiate standby and failure currents and that both polarities of errors will be detected, i.e. that parallel testing is possible.

Four 1852 devices were tested at room temperature and [illegible] volts. Table 2 presents the data, one of the devices had a fault causing its DO4 and DO5 [illegible] high. Whenever either one or both [illegible] these lines were supposed to be low an error occurred. The data demonstrate two to three orders of magnitude difference in the currents. Note also that double bit errors resulted in twice the current as single bit errors.

An experiment was also performed at 5 volts and elevated temperatures on eight 1852 devices. Standby supply currents were <0.1 milliamperes at 175C and <0.3 milliamperes at 207C. This test indicated that for these devices configured in parallel, supply leakage would not be a problem at elevated temperatures.

It should be noted that the support hardware to perform the constant monitoring of the 4001 and 1852 devices is the same, one sense resistor in each power supply line and a current detector. The requirement for comparators for each output line of each device under test has been eliminated.

Applications

The implementation of the parallel test concept at RADC includes a computer based measurement and control system. This provides the test bed with some "intelligence" for monitoring and controlling of experiments.

An experiment was performed on sixteen 1852's utilizing the computer system's pseudo random number generator capability to supply the data word which was clocked to all devices in parallel by a software generated timing sequence. The output of the current detector was used to interrupt the computer which would be normally exercising the devices under test. Upon interrupt the exercise program was halted in step and data gathered via the multiplexed A/D capability.

These data also included measurement of the voltage across the sense resistor of the current detector to establish if the fault had been frozen. The intent was to capture the conditions down to the clock cycle for verification and analysis of the fault.

Tests were conducted simulating faults of about one and a quarter milliamps by shorting to the sense resistor on any device with a resistor. The computer was quite able to detect and identify the faulty device and logic state.

Utilization of the computer enabled data acquisition and management plus verification and analysis of the fault. However, allowing the computer to generate the timing waveform through software resulted in a very slow exercise rate. While various means could be used to drive the devices under test at more reasonable rates, the parallel test technique suggests one.

In a parallel test the following conditions should be true: (1) although there are n devices under test they are in parallel and appear as one device (albeit with increased input capacitance and output drive capability), and (2) for sufficiently large n (which in reality need not be very large - see Table 1) a failure of one device will not inhibit the output signals from being acceptable logic levels. Therefore, it appears that a semiconductor device on a board or system could be replaced by a parallel set of devices and that system made to operate at speeds and with patterns approaching nomimal operating conditions. This approach would

greatly simplify the input hardware and pattern support and should be particularly significant in testing devices which operate in a feedback arrangement such as microprocessor components. Extending the concept to board level testing also suggests that all the components on a board may be tested simultaneously each in their own parallel chain.

Other applications suggest themselves as a result of n devices appearing functionally as one device. One such application is the potential to perform shmoo characterizations on n devices at a time thus generating operating boundaries for an entire population at one time.

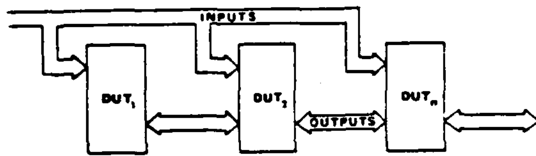


Figure 1. Parallel Test Concept

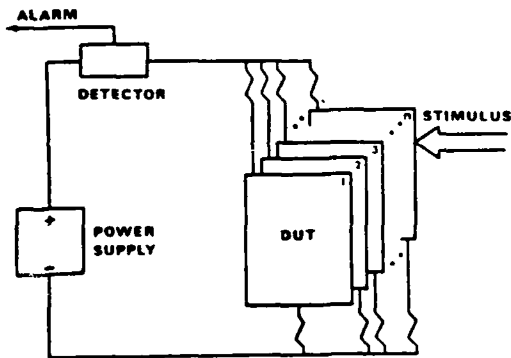


Figure 2. Implementation

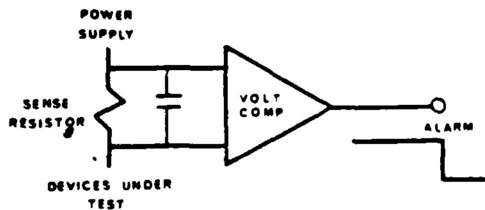


Figure 3. Current Detector

Conclusions

Key features of the parallel technique are:

1. Constant monitoring of all devices under test.
2. Simplicity of test bed requiring only a current detector and one set of input drive signals to perform monitored testing.
3. The devices under test form the "comparators".
4. There are n-1 "comparators".
5. With the addition of sensing in the power supply lines to each device the failed device and logic state in error can be determined.
6. Independent of device complexity.
7. Appropriate for dynamic testing.

SUPPLY VOLT.(V)	SUPPLY CURRENT(mA)	OUTPUT VOLT.(V)
3 INPUTS VDD - 1 INPUT VSS		
5	5.2	0.4
8	14.6	0.6
10	21.0	0.7
3 INPUTS VSS - 1 INPUT VDD		
5	4.7	4.3
8	14.4	6.5
10	20.0	8.0

TABLE 1 - INITIAL DATA

	DATA DO7...........DO0	CURRENT(mA)
PASS:	1 1 1 1 1 0 1 1	-0.20 (NOISE)
	0 0 1 1 0 1 1 1	0.22
	0 0 1 1 1 0 0 0	-0.16
	0 0 1 1 1 1 0 0	0.08
FAIL:	0 0 1 0 1 0 1 1	15.3
	0 1 0 1 1 1 0 1	15.7
	1 1 0 1 0 0 1 1	15.6
	0 1 0 0 1 1 0 1	29.4

TABLE 2 1852 DATA - FAULTY DEVICE

APPENDIX B
ELECTRICAL MEASUREMENTS

ELECTRICAL MEASUREMENTS

The electrical test conditions for the 6504 and 1802 are as specified in the MIL-M-38510/239 specification dated 2 January 1980 and the MIL-M-38510/470 specification dated 16 April 1979. However, several changes were required for both device types and are described below.

6504 CHANGES:

1) Terminal conditions for input pins not being tested during the V_{IC} tests were changed from ground to open.

2) I_{DD} MAX test limit at 25°C and -55°C was changed from 1.0 uA to 5.0 uA.

3) I_{SS} MAX test limit at 25°C and -55°C was changed from -1.0 uA to -5.0 uA.

4) The power-down (V_{DDR}) test was performed at 25°C, 125°C, and -55°C instead of only at 125°C.

5) Input capacitance (C_i) tests were not performed.

6) The ADCOMP functional test was not performed.

7) TAVQV, TELQX, and TEHQZ tests were not performed.

8) Pattern test for the chip enable access time (TELQV) measurement was changed from GALPAT to CHECKERBOARD, MARCH, and SLIDING DIAGONAL.

9) TELQV MAX test limit at 125°C was changed from 250 ns to 300 ns.

10) Input threshold (VTH and VTL) tests were added.

1802 CHANGES:

1) I_{OH2} MAX test limits were changed from -850 uA, -540 uA, and -950 uA (at 25°C, 125°C, and -55°C) to -550 uA, -550 uA, and -550 uA, respectively.

2) TPHL1 (TPA/TPB) limits were changed from 50 ns to 45 ns at -55°C.

3) Input and output capacitance (C_i and C_o) tests were not performed.

For brevity, the slash sheets for both device types will not be reproduced in this appendix. However, the 6504 and 1802 parameter symbols used in Section 6.4 and Appendix D are defined in Table B-1 and B-2, respectively. For reference, the parameters test limits used for initial and interim electrical testing are included in Tables B-3 and B-4.

TABLE B-1. 6504 SYMBOLS AND DEFINITIONS

SYMBOL	DEFINITION
VIC(POS)-V	POSITIVE INPUT CLAMP VOLTAGE IN VOLTS
VIC(NEG)-V	NEGATIVE INPUT CLAMP VOLTAGE IN VOLTS
IIH1-A	HIGH LEVEL INPUT CURRENT (ALL INPUTS) IN AMPS
IIH2-A	HIGH LEVEL INPUT CURRENT (SINGLE INPUT) IN AMPS
IIL1-A	LOW LEVEL INPUT CURRENT (ALL INPUTS) IN AMPS
IIL2-A	LOW LEVEL INPUT CURRENT (SINGLE INPUT) IN AMPS
IOHZ-A	HIGH IMPEDANCE STATE OUTPUT CURRENT IN AMPS
IOLZ-A	HIGH IMPEDANCE STATE OUTPUT CURRENT IN AMPS
IDD2(PU)-A	QUIESCENT SUPPLY CURRENT AT POWER-UP (5.5 VDC) IN AMPS
IDD2(B1)-A	QUIESCENT SUPPLY CURRENT WITH BACKGROUND OF "1"s (5.5 VDC) IN AMPS
IDD2(BO)-A	QUIESCENT SUPPLY CURRENT WITH BACKGROUND OF "0"s (5.5 VDC) IN AMPS
ISS2(PU)-A	QUIESCENT SUPPLY CURRENT AT POWER-UP (5.5 VDC) IN AMPS
ISS2(B1)-A	QUIESCENT SUPPLY CURRENT WITH BACKGROUND OF "1"s (5.5 VDC) IN AMPS
ISS2(BO)-A	QUIESCENT SUPPLY CURRENT WITH BACKGROUND OF "0"s (5.5 VDC) IN AMPS
VOL1-V	LOW LEVEL OUTPUT VOLTAGE (2 mA LOAD) IN VOLTS
VOL2-V	LOW LEVEL OUTPUT VOLTAGE (NO LOAD) IN VOLTS
VOH1-V	HIGH LEVEL OUTPUT VOLTAGE (-1 mA LOAD) IN VOLTS
VOH2-V	HIGH LEVEL OUTPUT VOLTAGE (NO LOAD) IN VOLTS
IDDOP-A	OPERATING SUPPLY CURRENT IN AMPS
PWRDNVDD-V	POWER DOWN SUPPLY VOLTAGE IN VOLTS
VTH-V	INPUT THRESHOLD VOLTAGE IN VOLTS
VTL-V	INPUT THRESHOLD VOLTAGE IN VOLTS
TA-EW-4.5-S	CHIP ENABLE ACCESS TIME - EARLY WRITE (VARIOUS PATTERNS) AT 4.5 VDC IN SECONDS
TA-EW-5.5-S	CHIP ENABLE ACCESS TIME - EARLY WRITE (VARIOUS PATTERNS) AT 5.5 VDC IN SECONDS
TA-RMW-4.5-S	CHIP ENABLE ACCESS TIME - READ/MODIFY/WRITE (VARIOUS PATTERNS) AT 4.5 VDC IN SECONDS
TA-RMW-5.5-S	CHIP ENABLE ACCESS TIME - READ/MODIFY/WRITE (VARIOUS PATTERNS) AT 5.5 VDC IN SECONDS

TABLE B-2. 1802 SYMBOLS AND DEFINITIONS

SYMBOL	MIL SPEC SYMBOL	DEFINITION
1. VICP-VDC	VICP	POSITIVE INPUT CLAMP VOLTAGE TO V_{DD} IN VOLTS.
2. VICN-VDC	VICN	NEGATIVE INPUT CLAMP VOLTAGE TO V_{SS} IN VOLTS.
3. ISS1-AMP	ISS1	QUIESCENT DEVICE CURRENT WITH V_{DD} = 5V IN AMPS.
4. ISS2-AMP	ISS2	QUIESCENT DEVICE CURRENT WITH V_{DD} = 10V IN AMPS.
5. ISS3-AMP	ISS3	QUIESCENT DEVICE CURRENT WITH V_{DD} = 13V IN AMPS.
6. IIH-AMP	IIH	HIGH LEVEL INPUT LEAKAGE CURRENT IN AMPS.
7. IIL-AMP	IIL	LOW LEVEL INPUT LEAKAGE CURRENT IN AMPS.
8. IZH-AMP	IZH	HIGH LEVEL HIGH IMPEDANCE OUTPUT LEAKAGE CURRENT IN AMPS.
9. IZL-AMP	IZL	LOW LEVEL HIGH IMPEDANCE OUTPUT LEAKAGE CURRENT IN AMPS.
10. IOL1-AMP	IOL1	LOW LEVEL OUTPUT DRIVE CURRENT WITH V_{DD} = 5V IN AMPS.
11. IOL2-AMP	IOL2	LOW LEVEL OUTPUT DRIVE CURRENT WITH V_{DD} = 10V IN AMPS.
12. IOH1-AMP	IOH1	HIGH LEVEL OUTPUT DRIVE CURRENT WITH V_{DD} = 5V IN AMPS.
13. IOH2-AMP	IOH2	HIGH LEVEL OUTPUT DRIVE CURRENT WITH V_{DD} = 10V IN AMPS.
14. IOLX-AMP	IOLX	LOW LEVEL $\overline{XTAL}$ OUTPUT CURRENT IN AMPS.
15. IOHX-AMP	IOHX	HIGH LEVEL $\overline{XTAL}$ OUTPUT CURRENT IN AMPS.
16. VOHX-VDC	VOHX	HIGH LEVEL CLOCK $\overline{XTAL}$ OUTPUT VOLTAGE IN VOLTS.
17. VOLX-VDC	VOLX	LOW LEVEL CLOCK $\overline{XTAL}$ OUTPUT VOLTAGE IN VOLTS.
18. VTNX-VDC	VTNX	NEGATIVE $\overline{XTAL}$ THRESHOLD VOLTAGE IN VOLTS.
19. VTPX-VDC	VTPX	POSITIVE $\overline{XTAL}$ THRESHOLD VOLTAGE IN VOLTS.
20. VIH1-VDC	VIH1	HIGH LEVEL INPUT THRESHOLD VOLTAGE WITH V_{DD} = 5V IN VOLTS.
21. VIH2-VDC	VIH2	HIGH LEVEL INPUT THRESHOLD VOLTAGE WITH V_{DD} = 10V IN VOLTS.
22. VIL1-VDC	VIL1	LOW LEVEL INPUT THRESHOLD VOLTAGE WITH V_{DD} = 5V IN VOLTS.
23. VIL2-VDC	VIL2	LOW LEVEL INPUT THRESHOLD VOLTAGE WITH V_{DD} = 10V IN VOLTS.
24. FUNCTIONAL	FUNCTIONAL	DETAILED OPERATIONAL CHECK OF THE DEVICE AT VARIOUS VOLTAGE LEVELS AND DEVICE SPEEDS.
25. EF.SETUP.1	TSLH3,TSHL3 ($\overline{EF}$)	MINIMUM SETUP TIME FOR EF INPUTS WITH V_{DD} = 5V IN SECONDS.
26. EF.SETUP.2	TSLH3,TSHL3 ($\overline{EF}$)	MINIMUM SETUP TIME FOR EF INPUTS WITH V_{DD} = 10V IN SECONDS.
27. EF.HOLD.1	THLH3,THHL3 ($\overline{EF}$)	MINIMUM HOLD TIME FOR EF INPUTS WITH V_{DD} = 5V IN SECONDS.
28. EF.HOLD.2	THLH3,THHL3 ($\overline{EF}$)	MINIMUM HOLD TIME FOR EF INPUTS WITH V_{DD} = 10V IN SECONDS.
29. DATA.SETUP.1	TSLH1,TSHL1 (DATA)	MINIMUM SETUP TIME FOR DATA INPUTS WITH V_{DD} = 5V IN SECONDS.
30. DATA.SETUP 1	TSLH1,TSHL1 (DATA)	MINIMUM SETUP TIME FOR DATA INPUTS WITH V_{DD} = 10V IN SECONDS.
31. DATA.HOLD.1	THLH1,THHL1 (DATA)	MINIMUM HOLD TIME FOR DATA INPUTS WITH V_{DD} = 5V IN SECONDS.
32. DATA.HOLD.2	THLH1,THHL1 (DATA)	MINIMUM HOLD TIME FOR DATA INPUTS WITH V_{DD} = 10V IN SECONDS.
33. INT.SETUP.1	TSHL2 ($\overline{INTR}$)	MINIMUM SETUP TIME FOR INTERRUPT INPUT WITH V_{DD} = 5V IN SECONDS.
34. INT.SETUP.2	TSHL2 ($\overline{INTR}$)	MINIMUM SETUP TIME FOR INTERRUPT INPUT WITH V_{DD} = 10V IN SECONDS.
35. INT.HOLD.1	THLH2 ($\overline{INTR}$)	MINIMUM HOLD TIME FOR INTERRUPT INPUT WITH V_{DD} = 5V IN SECONDS.
36. INT.HOLD.2	THLH2 ($\overline{INTR}$)	MINIMUM HOLD TIME FOR INTERRUPT INPUT WITH V_{DD} = 10V IN SECONDS.
37. DMAI.SETUP.1	TSHL2 ($\overline{DMA}$)	MINIMUM SETUP TIME FOR DMA-IN INPUT WITH V_{DD} = 5V IN SECONDS.
38. DMAI.SETUP.2	TSHL2 ($\overline{DMA}$)	MINIMUM SETUP TIME FOR DMA-IN INPUT WITH V_{DD} = 10V IN SECONDS.
39. DMAI.HOLD.1	THLH2 ($\overline{DMA}$)	MINIMUM HOLD TIME FOR DMA-IN INPUT WITH V_{DD} = 5V IN SECONDS.
40. DMAI.HOLD.2	THLH2 ($\overline{DMA}$)	MINIMUM HOLD TIME FOR DMA-IN INPUT WITH V_{DD} = 10V IN SECONDS.
41. DMAO.SETUP.1	TSHL2 ($\overline{DMA}$)	MINIMUM SETUP TIME FOR DMA-OUT INPUT WITH V_{DD} = 5V IN SECONDS.
42. DMAO.SETUP.2	TSHL2 ($\overline{DMA}$)	MINIMUM SETUP TIME FOR DMA-OUT INPUT WITH V_{DD} = 10V IN SECONDS.
43. DMAO.HOLD.1	THLH2 ($\overline{DMA}$)	MINIMUM HOLD TIME FOR DMA-OUT INPUT WITH V_{DD} = 5V IN SECONDS.
44. DMAO.HOLD.2	THLH2 ($\overline{DMA}$)	MINIMUM HOLD TIME FOR DMA-OUT INPUT WITH V_{DD} = 10V IN SECONDS.
45. WAIT.SETUP.1	TSHL4 ($\overline{WAIT}$)	MINIMUM SETUP TIME FOR WAIT INPUT WITH V_{DD} = 5V IN SECONDS.
46. WAIT.SETUP.2	TSHL4 ($\overline{WAIT}$)	MINIMUM SETUP TIME FOR WAIT INPUT WITH V_{DD} = 10V IN SECONDS.
47. PW.CLK.1	TWL1,TWH1 (CK)	MINIMUM PULSE WIDTH FOR CLOCK INPUT WITH V_{DD} = 5V IN SECONDS.
48. PW.CLK.2	TWL1,TWH1 (CK)	MINIMUM PULSE WIDTH FOR CLOCK INPUT WITH V_{DD} = 10V IN SECONDS.
49. PW.CLR.1	TWL2 (CLEAR)	MINIMUM PULSE WIDTH FOR CLEAR INPUT WITH V_{DD} = 5V IN SECONDS.
50. PW.CLR.2	TWL2 (CLEAR)	MINIMUM PULSE WIDTH FOR CLEAR INPUT WITH V_{DD} = 10V IN SECONDS.
		PROPAGATION DELAY TIME MEASURED FROM:
51. TPLH1-TPA	TPLHL (TPA)	THE FALLING EDGE OF CLOCK PULSE TO THE LOW TO HIGH TRANSITION OF TPA WITH V_{DD} = 5V IN SECONDS.
51. TPLH1-TPB	TPLH1 (TPB)	THE RISING EDGE OF CLOCK PULSE TO THE LOW TO HIGH TRANSITION OF TPB WITH V_{DD} = 5V IN SECONDS.
51. TPLH1-MWR	TPLH1 ($\overline{MWR}$)	THE FALLING EDGE OF CLOCK PULSE TO THE LOW TO HIGH TRANSITION OF MWR WITH V_{DD} = 5V IN SECONDS.
52. TPLHL-MRD	TPLH2 ($\overline{MRD}$)	THE FALLING EDGE OF CLOCK PULSE TO THE LOW TO HIGH TRANSITION OF MRD WITH V_{DD} = 5V IN SECONDS.

TABLE B-2. 1802 SYMBOLS AND DEFINITIONS (CONTINUED)

SYMBOL	MIL SPEC SYMBOL	DEFINITION
53. TPLH1-N	TPLH4 (N)	THE FALLING EDGE OF CLOCK PULSE TO THE LOW TO HIGH TRANSITION OF NO-N2 WITH V_{DD} = 5V IN SECONDS.
54. TPLH1-Q	TPLH8 (Q)	THE RISING EDGE OF CLOCK PULSE TO THE LOW TO HIGH TRANSITION OF Q WITH V_{DD} = 5V IN SECONDS.
55. TPHL1-TPA	TPHL1 (TPA)	THE FALLING EDGE OF CLOCK PULSE TO THE HIGH TO LOW TRANSITION OF TPA WITH V_{DD} = 5V IN SECONDS.
55. TPHL1-TPB	TPHL1 (TPB)	THE RISING EDGE OF CLOCK PULSE TO THE HIGH TO LOW TRANSITION OF TPB WITH V_{DD} = 5V IN SECONDS.
56. TPHL1-MWR	TPHL3 ($\overline{MWR}$)	THE FALLING EDGE OF CLOCK PULSE TO THE HIGH TO LOW TRANSITION OF MWR WITH V_{DD} = 5V IN SECONDS.
57. TPHL1-MRD	TPHL2 ($\overline{MRD}$)	THE RISING EDGE OF CLOCK PULSE TO THE HIGH TO LOW TRANSITION OF MRD WITH V_{DD} = 5V IN SECONDS.
58. TPHL1-N	TPHL4 (N)	THE FALLING EDGE OF CLOCK PULSE TO THE HIGH TO LOW TRANSITION OF NO-N2 WITH V_{DD} = 5V IN SECONDS.
59. TPHL1-Q	TPHL8 (Q)	THE RISING EDGE OF CLOCK PULSE TO THE HIGH TO LOW TRANSITION OF Q WITH V_{DD} = 5V IN SECONDS.
60. TPLH2-TPA	TPLH1 (TPA)	THE FALLING EDGE OF CLOCK PULSE TO THE LOW TO HIGH TRANSITION OF TPA WITH V_{DD} = 10V IN SECONDS.
60. TPLH2-TPB	TPLH1 (TPB)	THE RISING EDGE OF CLOCK PULSE TO THE LOW TO HIGH TRANSITION OF TPB WITH V_{DD} = 10V IN SECONDS.
60. TPLH2-MWR	TPLH1 ($\overline{MWR}$)	THE FALLING EDGE OF CLOCK PULSE TO THE LOW TO HIGH TRANSITION OF MWR WITH V_{DD} = 10V IN SECONDS.
61. TPLH2-MRD	TPLH2 ($\overline{MRD}$)	THE FALLING EDGE OF CLOCK PULSE TO THE LOW TO HIGH TRANSITION OF MRD WITH V_{DD} = 10V IN SECONDS.
62. TPLH2-N	TPLH4 (N)	THE FALLING EDGE OF CLOCK PULSE TO THE LOW TO HIGH TRANSITION OF NO-N2 WITH V_{DD} = 10V IN SECONDS.
63. TPLH2-Q	TPLH8 (Q)	THE RISING EDGE OF CLOCK PULSE TO THE LOW TO HIGH TRANSITION OF Q WITH V_{DD} = 10V IN SECONDS.
64. TPHL2-TPA	TPHL1 (TPA)	THE FALLING EDGE OF CLOCK PULSE TO THE HIGH TO LOW TRANSITION OF TPA WITH V_{DD} = 10V IN SECONDS.
64. TPHL2-TPB	TPHL1 (TPB)	THE RISING EDGE OF CLOCK PULSE TO THE HIGH TO LOW TRANSITION OF TPB WITH V_{DD} = 10V IN SECONDS.
65. TPHL2-MWR	TPHL3 ($\overline{MWR}$)	THE FALLING EDGE OF CLOCK PULSE TO THE HIGH TO LOW TRANSITION OF MWR with V_{DD} = 10V IN SECONDS.
66. TPHL2-MRD	TPHL2 ($\overline{MRD}$)	THE RISING EDGE OF CLOCK PULSE TO THE HIGH TO LOW TRANSITION OF MRD WITH V_{DD} = 10V IN SECONDS.
67. TPHL2-N	TPHL4 (N)	THE FALLING EDGE OF CLOCK PULSE TO THE HIGH TO LOW TRANSITION OF NO-N2 WITH V_{DD} = 10V IN SECONDS.
68. TPHL2-Q	TPHL8 (Q)	THE RISING EDGE OF CLOCK PULSE TO THE HIGH TO LOW TRANSITION OF Q WITH V_{DD} = 10V IN SECONDS.
69. DO.DELAY.1	TPXX1 (DATA)	WORST CASE PROPAGATION DELAY TIME MEASURED FROM THE TRANSITION OF THE CLOCK PULSE TO THE HIGH OR LOW TRANSITION OF DATA-OUT FROM THE HIGH Z STATE OR VICE VERSA WITH V_{DD} = 5V IN SECONDS.
70. DO.DELAY.2	TPXX1 (DATA)	WORST CASE PROPAGATION DELAY TIME MEASURED FROM THE TRANSITION OF THE CLOCK PULSE TO THE HIGH OR LOW TRANSITION OF DATA-OUT FROM THE HIGH Z STATE OR VICE VERSA WITH V_{DD} = 10V IN SECONDS.
71. SC.DELAY.1	TPLH7,TPHL7 (SC)	WORST CASE PROPAGATION DELAY TIME MEASURED FROM THE FALLING EDGE OF CLOCK PULSE TO THE TRANSITION OF SCO/SC1 WITH V_{DD} = 5V IN SECONDS.
72. SC.DELAY.2	TPLH7,TPHL7 (SC)	WORST CASE PROPAGATION DELAY TIME MEASURED FROM THE FALLING EDGE OF CLOCK PULSE TO THE TRANSITION OF SCO/SC1 WITH V_{DD} = 10V IN SECONDS.
73. ADHI.DELAY.1	TPLH5,TPHL5	WORST CASE PROPAGATION DELAY TIME MEASURED FROM THE FALLING EDGE OF CLOCK PULSE TO THE TRANSITION OF THE MEMORY HIGH-ADDRESS BYTE WITH V_{DD} = 5V IN SECONDS.
74. ADHI.DELAY.2	TPLH5,TPHL5	WORST CASE PROPAGATION DELAY TIME MEASURED FROM THE FALLING EDGE OF CLOCK PULSE TO THE TRANSITION OF THE MEMORY HIGH-ADDRESS BYTE WITH V_{DD} = 10V IN SECONDS.
75. ADLO.DELAY.1	TPLH6,TPHL6	WORST CASE PROPAGATION DELAY TIME MEASURED FROM THE RISING EDGE OF CLOCK PULSE TO THE TRANSITION OF THE MEMORY LOW-ADDRESS BYTE WITH V_{DD} = 5V IN SECONDS.
76. ADLO.DELAY.2	TPLH6,TPHL6	WORST CASE PROPAGATION DELAY TIME MEASURED FROM THE RISING EDGE OF CLOCK PULSE TO THE TRANSITION OF THE MEMORY LOW-ADDRESS BYTE WITH V_{DD} = 10V IN SECONDS.

TABLE B-3. 6504 ELECTRICAL TEST LIMITS

PARAMETER	TEST LIMITS 25°C MIN	MAX	125°C MIN	MAX	-55°C MIN	MAX	UNITS
VIC	200.0M	2.000	200.0M	4.000	200.0M	4.000	V
VIC	-2.000	-200.0M	-4.000	-200.0M	-4.000	-200.0M	↓
IIH1	-3.000N	100.0N	-3.000N	50.00U	-3.000N	50.00U	A
IIH2	-3.000N	10.00N	-3.000N	100.0N	-3.000N	1.000U	│
IIL1	-100.0N	3.000N	-50.00U	3.000N	-50.00U	3.000N	│
IIL2	-10.00N	3.000N	-100.0N	3.000N	-1.000U	3.000N	│
IOHZ	-5.000N	100.0N	-5.000N	1.000U	-5.000N	100.0N	│
IOLZ	-100.0N	5.000N	-1.000U	5.000N	-100.0N	5.000N	│
IDD2	-3.000N	5.000U	-3.000N	50.00U	-3.000N	5.000U	│
ISS2	-5.000U	3.000N	-50.00U	3.000N	-5.000U	3.000N	↓
VOL	10.00N	400.0M	10.00N	400.0M	10.00N	400.0M	V
VOL	10.00N	100.0M	10.00N	100.0M	10.00N	100.0M	│
VOH	2.400	6.000	2.400	6.000	2.400	6.000	│
VOH	4.400	6.000	4.400	6.000	4.400	6.000	↓
IDDOP	10.00N	50.00M	10.00N	15.00M	10.00N	50.00M	A
VDDR	0.000	2.000	0.000	2.000	0.000	2.000	│
VTH	1.500	3.500	0.000	6.000	0.000	6.000	│
VTL	8.00M	2.000	0.000	6.000	0.000	6.000	↓
TA-EW-4.5	25.00N	250.0N	25.00N	300.0N	25.00N	250.0N	S
TA-EW-5.5	25.00N	250.0N	25.00N	300.0N	25.00N	250.0N	│
TA-RMW-4.5	25.00N	250.0N	25.00N	300.0N	25.00N	250.0N	│
TA-RMW-5.5	25.00N	250.0N	25.00N	300.0N	25.00N	250.0N	↓

TABLE B-4. 1802 ELECTRICAL TEST LIMITS

PARAMETER	TEST LIMITS 25°C MIN	25°C MAX	125°C MIN	125°C MAX	-55°C MIN	-55°C MAX	UNITS
1. V_{ICP}	0.000	1.500	-1.000	1.000	-1.000	1.000	V
2. V_{ICN}	-1.500	0.000	-1.000	1.000	-1.000	1.000	V
3. I_{SS1}	-50.00U	1.000N	-500.0U	1.000N	-50.00U	1.000N	A
4. I_{SS2}	-100.0U	1.000N	-1.000M	1.000N	-100.0U	1.000N	
5. I_{SS3}	-200.0U	1.000N	-1.500M	1.000N	-200.0U	1.000N	
6. I_{IH}	-1.000N	300.0N	-1.000N	2.000U	-1.000N	300.0N	
7. I_{IL}	-300.0N	1.000N	-2.000U	1.000N	-300.0N	1.000N	
8. I_{ZH}	-1.000N	300.0N	-1.000N	2.000U	-1.000N	300.0N	
9. I_{ZL}	-300.0N	1.000N	-2.000U	1.000N	-300.0N	1.000N	
10. I_{OL1}	1.500M	100.0M	950.0U	100.0M	1.800M	100.0M	
11. I_{OL2}	2.800M	100.0M	1.700M	100.0M	3.300M	100.0M	
12. I_{OH1}	-100.0M	-350.0U	-100.0M	-230.0U	-100.0M	-420.0U	
13. I_{OH2}	-100.0M	550.0U	-100.0M	-550.0U	-100.0M	-550.0U	
14. I_{OLX}	100.0U	10.00M	66.00U	10.00M	120.0U	10.00M	
15. I_{OHX}	-10.00M	-50.00U	-10.00M	-33.00U	-10.00M	-60.00U	
16. V_{OHX}	4.500	5.100	-1.000	1.000	-1.000	1.000	V
17. V_{OLX}	-1.000M	500.0M	-1.000	1.000	-1.000	1.000	
18. V_{TNX}	300.0M	2.750	-1.000	1.000	-1.000	1.000	
19. V_{TPX}	-2.750	-300.0M	-1.000	1.000	-1.000	1.000	
20. V_{IH1}	0.000	3.500	0.000	3.500	0.000	3.500	
21. V_{IH2}	0.000	7.000	0.000	7.000	0.000	7.000	V
22. V_{IL1}	1.200	5.000	1.200	5.000	1.200	5.000	
23. VIL_2	3.000	10.00	3.000	10.00	3.000	10.00	
24. FUNCTIONAL	-500.0M	500.0M	-500.0M	500.0M	-500.0M	500.0M	N/A
25. t_{SLH3}, t_{SHL3} $(\overline{EF})$	-500.0M	50.00N	-500.0M	50.00N	-500.0M	70.00N	S
26. t_{SLH3}, t_{SHL3} $(\overline{EF})$	-500.0M	80.00N	-500.0M	30.00N	-500.0M	100.0N	
27. t_{HLH3}, t_{HHL3} $(\overline{EF})$	-500.0M	250.0N	-500.0M	350.0N	-500.0M	250.0N	
28. t_{HLH3}, t_{HHL3} $(\overline{EF})$	-500.0M	150.0N	-500.0M	200.0N	-500.0M	150.0N	
29. t_{SLH1}, t_{SHL1} (DATA)	-500.0M	0.000	-500.0M	0.000	-500.0M	50.00N	
30. t_{SLH1}, t_{SHL1} (DATA)	-500.0M	50.00N	-500.0M	50.00N	-500.0M	80.00N	
31. t_{HLH1}, t_{HHL1} (DATA)	-500.0M	350.0N	-500.0M	450.0N	-500.0M	300.0N	
32. t_{HLH1}, t_{HHL1} (DATA)	-500.0M	200.0N	-500.0M	250.0N	-500.0M	150.0N	
33. t_{SHL2} $(\overline{INTR})$	-500.0M	30.00N	-500.0M	30.00N	-500.0M	50.00N	
34. t_{SHL2} $(\overline{INTR})$	-500.0M	70.00N	-500.0M	70.00N	-500.0M	90.00N	
35. t_{HLH2} $(\overline{INTR})$	-500.0M	250.0N	-500.0M	300.0N	-500.0M	250.0N	
36. t_{HLH2} $(\overline{INTR})$	-500.0M	150.0N	-500.0M	700.0N	-500.0M	150.0N	
37. t_{SHL2} $(\overline{DMA})$	-500.0M	30.00N	-500.0M	30.00N	-500.0M	50.00N	
38. t_{SHL2} $(\overline{DMA})$	-500.0M	70.00N	-500.0M	70.00N	-500.0M	90.00N	

TABLE B-4. 1802 ELECTRICAL TEST LIMITS (CONTINUED)

PARAMETER	TEST LIMITS						UNITS
	25°C		125°C		-55°C		
	MIN	MAX	MIN	MAX	MIN	MAX	
39. t_{HLH2} ($\overline{DMA}$)	-500.0M	250.0N	-500.0M	300.0N	-500.0M	250.0N	S
40. t_{HLH2} ($\overline{DMA}$)	-500.0M	150.0N	-500.0M	200.0N	-500.0M	150.0N	
41. t_{SHL2} ($\overline{DMA}$)	-500.0M	30.00N	-500.0M	30.00N	-500.0M	50.0N	
42. t_{SHL2} ($\overline{DMA}$)	-500.0M	70.00N	-500.0M	70.00N	-500.0M	90.00N	
43. t_{HLH2} ($\overline{DMA}$)	-500.0M	250.0N	-500.0M	300.0N	-500.0M	250.0N	
44. t_{HLH2} ($\overline{DMA}$)	-500.0M	150.0N	-500.0M	700.0N	-500.0M	150.0N	
45. t_{SHLH} ($\overline{WAIT}$)	-500.0M	70.0N	-500.0M	70.0N	-500.0M	100.0N	
46. t_{SHLH} ($\overline{WAIT}$)	-500.0M	100.0N	-500.0M	100.0N	-500.0M	150.0N	
47. t_{WL1}, t_{WH1} (CK)	-500.0M	190.0N	-500.0M	250.0N	-500.0M	190.0N	
48. t_{WL1}, t_{WH1} (CK)	-500.0M	80.00N	-500.0M	110.0N	-500.0M	80.00N	
49. t_{WL2}, (CLEAR)	-500.0M	400.0N	-500.0M	500.0N	-500.0M	350.0N	
50. t_{WL2}, (CLEAR)	-500.0M	200.0N	-500.0M	250.0N	-500.0M	200.0N	
51. t_{PLH1}, (TPA, TPB)	0.000	450.0N	0.000	550.0N	0.000	400.0N	
52. t_{PLH2}, ($\overline{MRD}$)	0.000	450.0N	0.000	600.0N	0.000	400.0N	
53. t_{PLH4} (N)	0.000	800.0N	0.000	1.000U	0.000	700.0N	
54. t_{PLH8} (Q)	0.000	600.0N	0.000	750.0N	0.000	500.0N	
55. t_{PHL1} (TPA, TPB)	130.0N	450.0N	160.0N	550.0N	100.0N	400.0N	
56. t_{PHL3} ($\overline{MWR}$)	0.000	450.0N	0.000	550.0N	0.000	400.0N	
57. t_{PHL2} ($\overline{MRD}$)	0.000	450.0N	0.000	600.0N	0.000	400.0N	
58. t_{PHL4} (N)	0.000	800.0N	0.000	1.000U	0.000	700.0N	
59. t_{PHL8} (Q)	0.000	600.0N	0.000	750.0N	0.000	500.0N	
60. t_{PLH1} (TPA, TPB	0.000	250.0N	0.000	300.0N	0.000	220.0N	
61. t_{PLH2} ($\overline{MRD}$)	0.000	300.0N	0.000	350.0N	0.000	270.0N	
62. t_{PLH4} (N)	0.000	400.0N	0.000	450.0N	0.000	350.0N	
63. t_{PLH8} (Q)	0.000	300.0N	0.000	350.0N	0.000	270.0N	
64. t_{PHL1} (TPA, TPB)	60.00N	250.0N	70.0N	300.0N	45.00N	220.0N	
65. t_{PHL3} ($\overline{MWR}$)	0.000	250.0N	0.000	300.0N	0.000	220.0N	
66. t_{PHL2} ($\overline{MRD}$)	0.000	300.0N	0.000	350.0N	0.000	270.0N	
67. t_{PLH4} (N)	0.000	400.0N	0.000	450.0N	0.000	350.0N	
68. t_{PHL8} (Q)	0.000	300.0N	0.000	350.0N	0.000	270.0N	
69. t_{PXX1} (DATA)	0.000	600.0N	0.000	700.0N	0.000	550.0N	
70. t_{PXX1} (DATA)	0.000	400.0N	0.000	450.0N	0.000	350.0N	
71. t_{PLH7}, t_{PHL7} (SC)	0.000	650.0N	0.000	850.0N	0.000	550.0N	
72. t_{PLH7}, t_{PHL7} (SC)	0.000	350.0N	0.000	400.0N	0.000	300.0N	
73. t_{PLH5}, t_{PHL5}	0.000	1.200U	0.000	1.550U	0.000	1.100U	
74. t_{PLH5}, t_{PHL5}	0.000	600.0N	0.000	700.0N	0.000	500.0N	
75. t_{PLH6}, t_{PHL6}	170.0N	550.0N	220.0N	650.0N	140.0N	500.0N	
76. t_{PLH6}, t_{PHL6}	80.00N	350.0N	100.0N	400.0N	70.00N	300.0N	

APPENDIX C

MDAC-STL DYNAMIC LIFE TEST SYSTEM

MDAC-STL DYNAMIC LIFE TEST SYSTEM

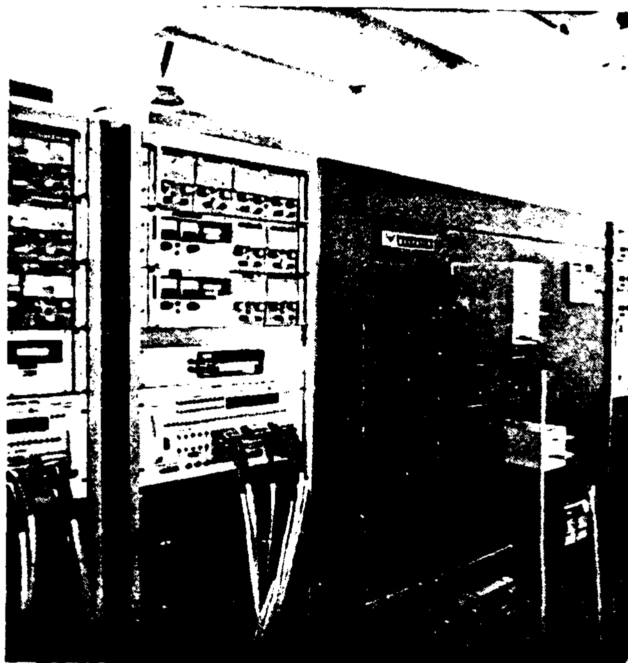
The MDAC-STL Dynamic Life Test System (DLTS) is an 8080 microprocessor-based system designed to perform parallel testing, dynamic/static burn-in at high temperatures, and continuous monitoring of microcircuits. Figure C-1 shows the operational configuration of the DLTS system. The block diagram in Figure C-2 illustrates the four major components of the DLTS. They are the chassis, control panel, Fluke 8600 multimeter, and printer. The following discussion addresses the operational aspects of the high temperature chassis and the control panel.

CHASSIS DESCRIPTION

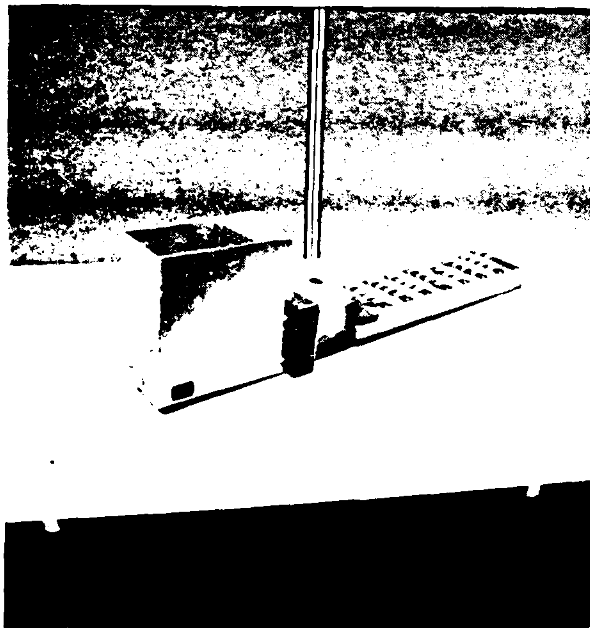
As shown in Figure C-3, the parallel test chassis consists of the following component blocks: control, voltage monitor, window detector, interface/simulated fault, and driver. In addition, the portion of the chassis in the oven contains high temperature sockets for DUTs. Each matrix's corresponding inputs and outputs of each DUT are paralleled and only the wire for each input signal passes through the high temperature interface to the DLTS chassis. However, corresponding inputs of the 6504 matrices are wired together. This approach reduces the need for high temperature materials and components.

The control circuitry determines which DLTS chassis is being addressed by the control panel. It also generates control signals for the driver and monitor sections of the chassis. The voltage monitor section multiplexes specific voltages of interest, such as the device-under-test (DUT) supply voltage, for readout by the Fluke multimeter.

The window detector determines by an increased/decreased current through a detector resistor that outputs of the devices connected in parallel are not in compliance and that a failure has occurred. The interface board buffers all the input signals from the driver to the DUTS. The simulated fault board insures that stuck-at-zero (S-A-0) and stuck-at-one (S-A-1) faults can be detected during demonstration testing.



PARALLEL TEST SYSTEM



PARALLEL TEST CHASSIS

FIGURE C-1. DLTS CONFIGURATION

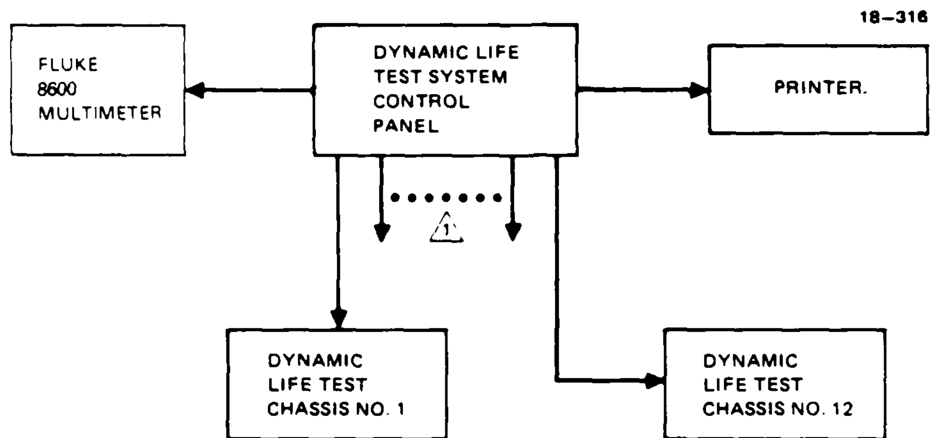


FIGURE C-2. DLTS BLOCK DIAGRAM

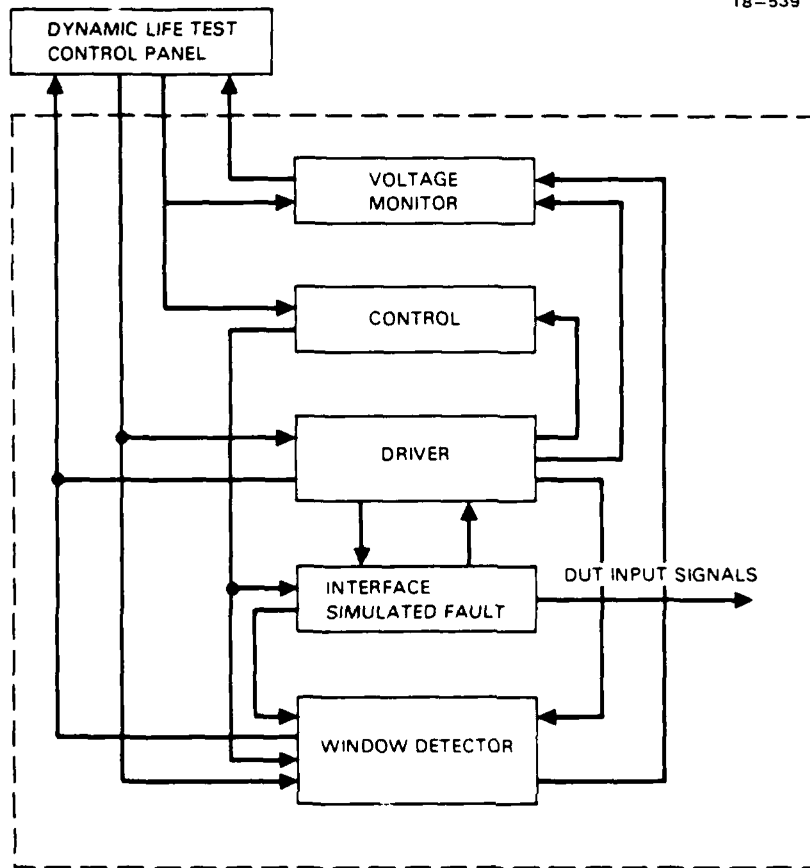


FIGURE C-3. PARALLEL TEST CHASSIS BLOCK DIAGRAM

The driver creates the dynamic stimuli for the DUTs. The 6504 driver generates a GALPAT pattern, reading and writing the pattern to every DUT each cycle. The 1802 driver generates instructions executed by the microprocessor in the same sequence each cycle.

CONTROL PANEL DESCRIPTION

The control panel operates in eight modes. For clarity, the modes may be subdivided into three categories of initialization, operation, and data display. The initialization modes are CHASSIS SELECT, SERIAL NUMBER SELECT, and TIME SET. The CHASSIS SELECT mode is used to select the chassis that have been connected to the control panel. DLTS chassis locations 2 and 3 are dedicated to the 6504 and 1802 parallel test chassis, respectively. By selecting only active chassis, the monitor interrogating cycle time is minimized. The interrogating time is less than 8 ms for a parallel test chassis when no error is present. When a 6504 error occurs, the chassis cycle time varies from ten to thirty seconds and is dependent on the number of matrices that contains an error. In contrast, the 1802 requires twenty-five seconds of settling time before interrogating the chassis for a failed device. An additional ten to thirty seconds are required to isolate the failed device. The SERIAL NUMBER SELECT mode is used to select the DUT sockets that have devices installed and thereby disregard output data for empty DUT sockets. The TIME SET mode is used to set a real time clock with date and time.

The operational modes are RESET and CONTINUOUS MONITOR. RESET clears the software registers in the control panel and restarts the driver in the test chassis. In the CONTINUOUS MONITOR mode, selected chassis are sequentially interrogated. When the 6504 parallel test chassis is interrogated, a HALT pulse is transmitted to the DLTS control panel. If the HALT signal is high, no error was detected and the next selected chassis is interrogated. However, if the HALT signal is low, the chassis detected an error. The DLTS then performs five V_{RPS} voltage (Figure C-4) measurements. A matrix has an error when the V_{RPS} voltage is less than 5.525V. If the V_{RPS} measurement indicates no matrix error, then the window detector has falsely triggered. Next, the false HALT (no error) register is incremented. The false halt register stores the number of false triggers between resets.

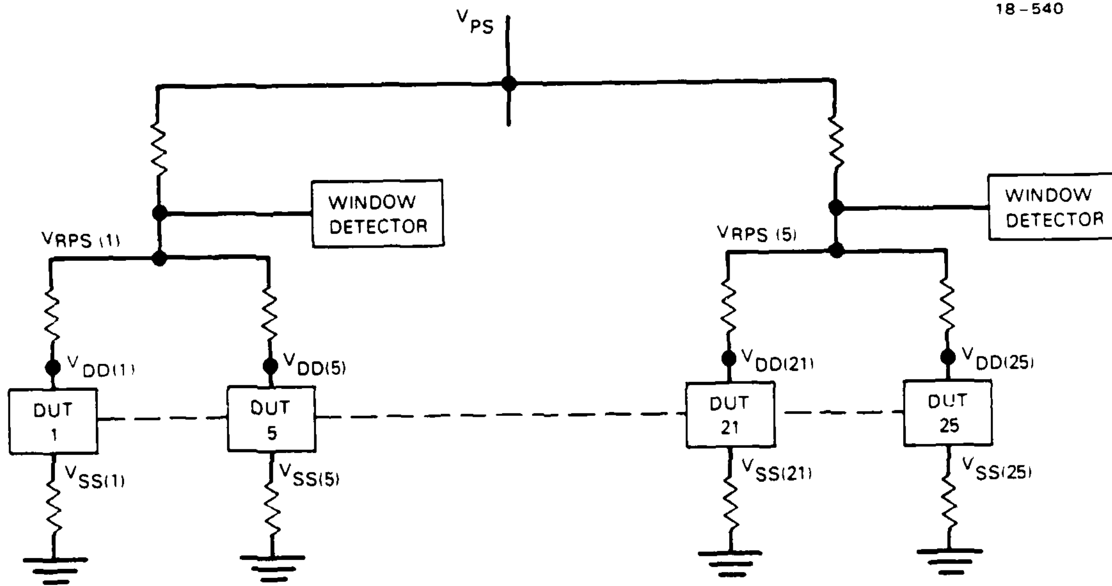


FIGURE C-4. PARALLEL TEST METHOD MATRIX CONCEPT

The COMPARE DATA (CD) signal from the 6504 chassis then cues the DLTS that a failed 6504 has a S-A-0 or S-A-1 fault. Then the V_{DD} voltages with the driver in a static state are measured to isolate a failed device in a matrix.

During parallel testing four bad DUTs in each matrix of five devices can be detected as failures during the same cycle. If all five 6504s had incorrect output data during the same cycle, then the errors would appear transparent to the window detector (all the 6504s outputs would be in the same state with no large output current flow).

A software subroutine insures that the driver has an approximately 25% duty cycle if all matrices have failures at different address locations. After a matrix has its first error (ERROR COUNT = 1) and if no additional failure occurs within the chassis for 90 seconds, the ERROR COUNT is reset to zero. After a 6504 matrix has two failures (ERROR COUNT = 2) within 180 seconds of each other, the matrix is masked (unable to halt) for 130 seconds. During each failed chassis cycle, ten seconds per matrix are required to isolate the failed devices.

The 1802 parallel procedure is similar to the 6504 procedure except for the following: a) in a matrix of five devices,fewer than two failed 1802s can be isolated per cycle, b) there is no COMPARE DATA signal since the device has multiple outputs, c) the V_{DD} and V_{SS} voltages are measured to isolate the failed devices, and d) three of the five 1802s are assumed as good devices.

After an 1802 matrix has two failures within 240 seconds of each other, the matrix is masked for 210 seconds. However, after a matrix has its first error and no additional failure occurs within the chassis for 120 seconds, then its error count is reset to zero. Window detectors are masked before the restarting of the driver to insure that the failed 1802 is reinitialized. Reinitializing is necessary after a failure has occurred because the failure may effect sequential instructions. The 1802 driver will run at least 17% of the time if all matrices fail different instructions over the 210 seconds of masking.

Finally, the remaining control panel modes are in the data display category. They are: VOLTAGE MONITOR, PRINT, and PRINT FUNCTIONAL DATA. When the VOLTAGE MONITOR mode is selected, voltages of interest (such as the DUT supply voltages) are monitored. The voltages are displayed on the Fluke 8600 digital voltmeter. Serial numbers and chassis numbers are also displayed on the control panel. In the parallel chassis PRINT mode, a voltage printout (Figure C-5) is obtained. When the PRINT FUNCTIONAL DATA is selected, a printout is obtained without the DUT voltage/current measurements. Because the voltage measurements for a single chassis take approximately one minute, a faster printout of the DUT functional data is available with PRINT FUNCTIONAL DATA mode.

6504 TEST

TEMPERATURE :	175 C	AVG. VDD VOLTAGE	5.492 V
		AVG. IDD CURRENT	1.055 mA
CELL NUMBER :	133	CHASSIS SUPPLY	5.252 V
		FALSE HALT COUNT	0
DATE :	21-FEB-83	LOW COMPARE	[illegible].105 V
TIME :	14 : 16		

HIGH COMPARE VOLTAGE	1	2	3	4	5
	7.363	7.292	7.195	[illegible]	[illegible]

SERIAL NUMBER	DYNAMIC VOLTAGE V	DYNAMIC CURRENT mA	S-A-1 ERROR COUNT	S-A-1 FIRST ERROR ADDRESS	S-A-0 ERROR COUNT	S-A-0 FIRST ERROR ADDRESS	MASK COUNT	FAIL ORDER
1	5.605	1.360	1	1	1	10001	5	1
2	5.611	1.300	1	1	1	10001	5	2
3	5.670	.630	1	1	1	10001	5	3
4	5.624	1.170	1	1	1	10001	5	4
5	5.670	.710	1	1	1	10001	5	5
6	5.501	1.420	0	0	0	0	1	2
7	5.582	.610	1	1	1	10001	1	1
8	5.527	1.160	0	0	0	0	1	2
9	5.565	.780	0	0	0	0	1	2
10	5.532	1.110	0	0	0	0	1	2
11	5.453	.890	0	0	0	0	1	2
12	5.438	1.040	0	0	0	0	1	0
13	5.405	1.370	1	1	1	10001	1	1
14	5.421	1.210	0	0	0	0	1	2
15	5.394	1.480	0	0	0	0	1	2

FIGURE C-5. TYPICAL PARALLEL TEST PRINTOUT

APPENDIX D
DEMONSTRATION TEST DATA SUMMARIES

INTRODUCTION

This appendix contains the data summaries of the demonstration test devices and control group for the 6504 4K memory and the 1802 8-bit microprocessor. The data summaries include the parameter means and standard deviations (sigmas) for all electrical test measurements performed at 125°C. Tables D-1 and D-2 present the demonstration test data summaries for both device types. The control group data summaries are included in Tables D-3 and D-4. For reference, the parameter symbols and test limits for the 6504 and 1802 were previously defined in Appendix B.

TABLE D-1. 6504 PARAMETER SUMMARIES OF THE DEMONSTRATION TEST DEVICES (175°C CELL/125°C DATA)

PARAMETER	CUMULATIVE HOURS							
	INITIAL		72 HOURS		168 HOURS		500 HOURS	
	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA
VIC(POS)-V	872.0M	43.72M	900.4M	111.9M	882.8M	71.47M	880.6M	44.96M
VIC(NEG)-V	-801.7M	47.10M	-815.3M	113.9M	-803.4M	82.29M	-794.3M	48.83M
IIH1-A	2.817N	352.5P	2.200N	207.4P	2.835N	293.7P	2.950N	446.6P
IIH2-A	691.3P	114.5P	617.4P	395.9P	641.0P	399.3P	643.8P	337.0P
IIL1-A	-6.554N	5.191N	-3.163N	6.353N	-4.508N	4.395N	-4.854N	6.803N
IIL2-A	-414.4P	449.1P	-108.6P	457.6P	-202.2P	356.8P	-225.1P	482.1P
IOHZ-A	4.434N	2.524N	2.761N	1.117N	3.434N	2.206N	3.436N	2.072N
IOLZ-A	-6.959N	9.150N	-2.177N	3.576N	-4.861N	8.881N	-3.802N	5.674N
IDD2(PU)-A	10.47U	6.745U	5.347U	5.123U	8.070U	5.790U	6.971U	3.510U
IDD2(B1)-A	9.566U	5.943U	4.786U	4.722U	7.580U	5.612U	6.251U	3.200U
IDD2(BO)-V	10.74U	7.247U	5.082U	4.965U	7.862U	5.532U	7.139U	3.426U
ISS2(PU)-A	-8.623U	5.817U	-4.123U	4.173U	-6.327U	4.503U	-5.589U	2.621U
ISS2(B1)-A	-8.460U	5.771U	-4.086U	4.139U	-6.290U	4.456U	-5.547U	2.724U
ISS2(BO)-A	-8.492U	5.792U	-4.108U	4.157U	-6.319U	4.465U	-5.574U	2.742U
VOL1-V	227.9M	20.16M	220.3M	16.93M	224.9M	21.37M	221.7M	20.40M
VOL2-V	1.412M	86.33U	1.794M	185.1U	1.740M	321.6U	1.824M	191.9U
VOH1-V	3.859	51.73M	3.877	47.14M	3.863	52.54M	3.867	53.91M
VOH2-V	4.504	1.381M	4.498	0.000	4.498	0.000	4.498	2.584M
IDDOP-A	7.345M	876.5U	7.129M	816.3U	7.058M	949.3U	7.356M	967.2U
PWRDNVDD-V	622.5M	332.9M	595.0M	305.0M	600.5M	314.5M	619.7M	317.2M
VTH-V	1.939	118.4M	1.943	119.3M	1.940	118.1M	1.940	120.0M
VTL-V	1.535	115.9M	1.545	115.7M	1.539	115.5M	1.541	117.9M
TA-EW-4.5-S	220.2N	33.76N	215.5N	33.09N	218.8N	34.32N	217.9N	34.44N
TA-EW-5.5-S	182.6N	25.17N	179.9N	26.80N	181.8N	25.79N	180.9N	25.92N
TA-RMW-4.5-S	220.6N	33.19N	218.2N	33.39N	221.4N	34.80N	220.3N	34.78N
TA-RMW-5.5-S	184.4N	25.10N	181.2N	24.96N	184.1N	25.93N	182.9N	26.29N

TABLE D-2. 1802 PARAMETER SUMMARIES OF THE DEMONSTRATION TEST DEVICES (125°C CELL/125°C DATA)

PARAMETER	CUMULATIVE HOURS							
	INITIAL		72 HOURS		168 HOURS		500 HOURS	
	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA
ISS1-AMP	-475.3N	345.1N	-896.9N	401.4N	-481.8N	226.1N	-1.237U	874.1N
ISS2-AMP	-2.364U	7.791U	-4.094U	12.29U	-3.328U	12.31U	-3.518U	8.555U
ISS3-AMP	-6.265U	20.74U	-8.673U	29.95U	-8.286U	30.38U	-6.961U	20.61U
IIH-AMP	4.814N	27.12N	4.135N	26.32N	3.547N	25.76N	4.359N	28.54N
IIL-AMP	-4.606N	28.80N	-5.390N	26.87N	-4.045N	26.31N	-5.670N	27.78N
IZH AMP	2.807N	1.793N	2.275N	2.840N	1.753N	2.342N	2.263N	3.202N
IZL-AMP	-3.973N	1.383N	-5.794N	1.542N	-3.733N	1.279N	-5.891N	2.201N
IOL1-AMP	2.049M	211.1U	2.007M	213.8U	2.044M	212.4U	2.011M	205.0U
IOL2-AMP	3.649M	348.8U	3.574M	355.1U	3.639M	351.6U	3.587M	339.9U
IOH1-AMP	-527.8U	64.26U	-524.1U	63.41U	-530.7U	64.00U	-525.0U	62.50U
IOH2-AMP	-933.1U	142.8U	-931.0U	136.0U	-942.2U	137.4U	-932.7U	134.5U
IOLX-AMP	227.8U	16.05U	225.8U	16.02U	227.8U	16.24U	225.5U	15.75U
IOHX-AMP	-166.5U	11.22U	-165.1U	10.95U	-166.4U	11.17U	-165.1U	10.86U
VIH1-VDC	2.640	138.5M	2.656	141.6M	2.656	141.6M	2.668	131.8M
VIH2-VDC	4.632	140.6M	4.652	138.9M	4.652	138.9M	4.656	132.9M
VIL2-VDC	3.912	124.3M	3.916	128.6M	3.916	128.6M	3.912	124.3M
EF.SETUP.1	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000
EF.SETUP.2	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000
EF.HOLD.1	136.0N	20.39N	139.2N	17.87N	138.4N	19.94N	138.8N	18.83N
EF.HOLD.2	63.60N	7.418N	66.00N	7.483N	66.00N	7.483N	64.80N	7.547N
DATA.SETUP.1	-49.60N	11.13N	-50.80N	10.93N	-50.40N	11.13N	-50.40N	11.13N
DATA.SETUP.2	-17.60N	5.122N	-19.20N	6.274N	-18.80N	6.524N	-18.80N	6.524N
DATA.HOLD.1	208.4N	27.37N	209.2N	28.27N	207.6N	27.17N	209.2N	27.56N
DATA.HOLD.2	98.00N	10.58N	98.00N	10.58N	96.00N	11.31N	97.60N	10.69N
INT.SETUP.1	-125.2N	18.79N	-124.0N	17.66N	-124.4N	18.35N	-124.4N	18.35N
INT.SETUP.2	46.80N	6.144N	-44.40N	4.964N	-44.40N	4.964N	-44.40N	4.964N
INT.HOLD.1	124.8N	17.00N	120.0N	16.73N	119.6N	16.85N	119.6N	16.85N
INT.HOLD.2	54.80N	4.995N	50.00N	6.324N	49.60N	6.621N	48.00N	5.656N
DMAI.SETUP.1	-163.2N	23.10N	-160.0N	22.80N	-160.4N	22.36N	-160.4N	22.36N
DMAI.SETUP.2	-63.60N	7.939N	-59.20N	7.440N	-58.80N	7.652N	-58.40N	7.838N
DMAI.HOLD.1	121.6N	16.41N	116.4N	17.18N	117.6N	17.50N	117.2N	18.00N
DMAI.HOLD.2	51.20N	5.879N	45.60N	5.713N	47.20N	6.013N	46.00N	5.657N
DMAO.SETUP.1	-168.4N	23.44N	-163.2N	23.10N	-162.4N	23.20N	-164.0N	23.49N
DMAO.SETUP.2	-66.80N	7.858N	-61.20N	8.158N	-60.80N	7.440N	-60.40N	7.200N
DMAO.HOLD.1	128.8N	17.73N	120.0N	17.20N	119.6N	17.32N	119.2N	17.42N
DMAO.HOLD.2	58.80N	6.524N	49.60N	5.986N	49.20N	6.223N	47.20N	6.013N
WAIT.SETUP.1	-150.0N	0.000	-150.0N	0.000	-150.0N	0.000	-150.0N	0.000
WAIT.SETUP.2	150.0N	0.000	-150.0N	0.000	-150.0N	0.000	150.0N	0.000
FW.CLK.1	120.4N	15.61N	119.2N	16.71N	119.2N	16.71N	120.8N	15.98N
FW.CLK.2	53.20N	4.664N	51.20N	5.154N	50.40N	5.986N	51.60N	5.425N
FW.CLR.1	23.20N	4.665N	23.20N	4.665N	22.80N	4.490N	23.20N	4.665N
FW.CLR.2	20.00N	0.000	20.00N	0.000	20.00N	0.000	20.00N	0.000

TABLE D-2. 1802 PARAMETER SUMMARIES OF THE DEMONSTRATION TEST DEVICES (125°C CELL/125°C DATA) (CONTINUED)

PARAMETER	CUMULATIVE HOURS							
	INITIAL		72 HOURS		168 HOURS		500 HOURS	
	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA
TFLH1-TFA/B	265.4N	38.11N	264.7N	39.35N	263.0N	39.15N	265.8N	40.19N
TFLH1-MWR	251.9N	31.16N	224.9N	28.77N	224.3N	28.67N	249.2N	30.77N
TFLH1-MRD	298.2N	36.88N	300.8N	36.94N	301.1N	36.69N	278.9N	35.91N
TFLH1-N	446.7N	105.6N	445.0N	105.1N	442.4N	105.0N	444.7N	105.3N
TFLH1-Q	520.1N	65.34N	518.9N	65.34N	515.9N	64.67N	519.7N	65.24N
TFHL1-TFA/B	250.3N	36.64N	252.1N	36.88N	250.3N	36.77N	252.9N	37.27N
TFHL1-MWR	254.9N	34.15N	242.2N	32.99N	240.8N	32.81N	253.7N	34.40N
TFHL1-MRD	266.2N	36.09N	266.1N	36.27N	264.2N	35.88N	255.8N	34.81N
TFHL1-N	384.7N	68.34N	385.1N	70.07N	382.3N	69.92N	385.2N	70.38N
TFHL1-Q	421.5N	54.46N	422.9N	54.35N	419.8N	53.85N	423.8N	54.28N
TFLH2-TFA/B	117.7N	13.39N	116.5N	14.14N	115.8N	14.01N	117.5N	14.59N
TFLH2-MWR	112.5N	10.87N	94.44N	9.864N	93.94N	9.653N	108.9N	10.64N
TFLH2-MRD	130.6N	12.57N	131.1N	12.71N	131.3N	12.56N	116.0N	12.15N
TFLH2-N	200.3N	43.13N	198.3N	43.74N	197.1N	43.65N	198.2N	43.72N
TFLH2-Q	235.3N	23.70N	231.5N	23.79N	229.9N	23.47N	232.1N	23.70N
TFHL2-TFA/B	103.5N	12.08N	104.0N	12.31N	103.2N	12.16N	104.5N	12.40N
TFHL2-MWR	102.7N	11.35N	94.34N	10.92N	93.46N	10.80N	99.84N	11.39N
TFHL2-MRD	114.2N	12.80N	112.9N	12.75N	112.2N	12.66N	107.9N	12.32N
TFHL2-N	170.8N	27.25N	169.3N	28.48N	168.1N	28.29N	169.5N	28.50N
TFHL2-Q	185.6N	19.21N	186.1N	19.24N	184.5N	19.03N	186.5N	19.24N
DO.DELAY.1	438.6N	54.69N	439.0N	54.84N	434.2N	52.76N	438.6N	53.95N
DO.DELAY.2	214.6N	21.25N	215.8N	21.53N	212.2N	19.50N	216.2N	21.60N
SC.DELAY.1	468.6N	59.99N	470.2N	60.61N	465.4N	58.68N	469.4N	59.26N
SC.DELAY.2	209.8N	21.00N	209.4N	21.18N	207.4N	20.64N	208.2N	21.11N
ADHI.DELAY.1	885.4N	112.9N	892.2N	112.2N	883.8N	111.3N	891.0N	111.6N
ADHI.DELAY.2	382.2N	40.05N	386.2N	41.11N	381.8N	39.46N	385.8N	39.69N
ADLO.DELAY.1	312.6N	40.13N	318.6N	38.77N	312.2N	39.65N	318.2N	39.26N
ADLO.DELAY.2	152.2N	15.88N	154.6N	15.36N	152.2N	14.56N	154.6N	15.36N

TABLE D-3. 6504 PARAMETER SUMMARIES OF THE DEMONSTRATION TEST CONTROL GROUP (125°C DATA)

PARAMETER	CUMULATIVE HOURS							
	INITIAL		72 HOURS		168 HOURS		500 HOURS	
	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA
VIC(POS)-V	908.9M	93.28M	929.5M	101.2M	921.1M	99.07M	919.3M	92.77M
VIC(NEG)-V	-859.9M	132.3M	-865.6M	141.1M	-855.8M	135.5M	-851.8M	126.5M
IIH1-A	2.860N	336.6P	2.446N	572.2P	2.734N	368.4P	2.840N	361.0P
IIH2-A	782.0P	121.2P	658.9P	402.2P	689.9P	392.6P	674.9P	327.2P
IIL1-A	-8.618N	3.452N	-4.840N	4.682N	-5.367N	3.545N	-5.517N	3.730N
IIL2-A	-675.3P	825.0P	-256.1P	524.5P	-315.5P	705.3P	-305.3P	662.5P
IOHZ-A	3.990N	1.340N	2.750N	1.185N	2.830N	971.6P	2.850N	892.5P
IOLZ-A	-6.496N	3.569N	-1.993N	1.505N	-3.364N	2.985N	-2.939N	2.343N
IDD2(PU)-A	7.114U	3.894U	4.505U	4.415U	4.960U	3.910U	4.921U	3.902U
IDD2(B1)-A	5.853U	2.504U	3.556U	3.989U	3.783U	2.392U	3.862U	2.789U
IDD2(BO)-A	5.968U	2.577U	3.619U	4.061U	3.859U	2.453U	3.952U	2.871U
ISS2(PU)-A	-6.505U	3.472U	-3.785U	3.102U	-4.398U	3.263U	-4.237U	3.084U
ISS2(B1)-A	-6.495U	3.497U	-3.806U	3.111U	-4.422U	3.260U	-4.256U	3.085U
ISS2(BO)-A	-6.517U	3.503U	-3.819U	3.115U	-4.437U	3.262U	-4.273U	3.090U
VOL1-V	240.8M	20.11M	230.0M	22.40M	233.3M	22.25M	233.6M	19.58M
VOL2-V	1.470M	87.17U	1.670M	107.7U	1.630M	67.80U	1.740M	115.8U
VOH1-V	3.851	61.32M	3.871	69.67M	3.862	66.75M	3.864	61.07M
VOH2-V	4.505	0.000	4.498	1.953M	4.497	1.953M	4.498	1.953M
IDDOP-A	6.792M	722.4U	7.090M	527.9U	6.912M	720.4U	6.846M	536.7U
PWRDNVDD-V	567.5M	181.4M	650.0M	168.4M	581.3M	173.9M	622.5M	177.2M
VIH-V	2.021	147.1M	2.027	153.8M	2.023	147.8M	2.023	150.4M
VIL-V	1.629	137.8M	1.644	145.5M	1.638	139.5M	1.636	136.4M
TA-EW-4.5-S	235.8N	21.43N	230.9N	22.00N	234.3N	19.98N	234.4N	18.96N
TA-EW-5.5-S	196.4N	17.49N	192.2N	18.26N	193.7N	18.15N	198.1N	25.52N
TA-RMW-4.5-S	236.7N	21.40N	233.4N	21.97N	236.1N	22.05N	235.7N	20.95N
TA-RMW-5.5-S	198.1N	17.26N	194.8N	18.25N	196.2N	18.37N	196.3N	17.83N

TABLE D-4. 1802 PARAMETER SUMMARIES OF THE DEMONSTRATION TEST CONTROL GROUP (125°C DATA)

PARAMETER	CUMULATIVE HOURS							
	INITIAL		72 HOURS		168 HOURS		500 HOURS	
	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA
ISS1-AMP	-325.2N	63.72N	-732.1N	66.55N	-606.7N	398.0N	-342.4N	335.5N
ISS2-AMP	-2.415U	3.447U	-2.809U	3.274U	-2.580U	3.669U	-2.481U	3.460U
ISS3-AMP	-11.14U	18.44U	-11.30U	17.78U	-10.90U	17.95U	-11.35U	18.71U
IIH-AMP	2.021N	714.7F	1.082N	501.8F	990.3F	453.7F	852.8F	496.1F
IIL-AMP	-2.078N	849.7F	-3.319N	1.885N	-2.354N	1.536N	-1.624N	1.486N
IZH-AMP	1.787N	260.7F	465.6F	220.2F	487.5F	188.3F	400.0F	176.8F
IZL-AMP	-4.109N	751.4F	-6.706N	703.9F	-4.606N	1.069N	-3.537N	1.920N
IOL1-AMP	1.716M	187.7U	1.690M	181.0U	1.711M	175.9U	1.730M	180.4U
IOL2-AMP	3.397M	343.7U	3.342M	335.5U	3.382M	328.1U	3.414M	339.5U
IOH1-AMP	-697.6U	97.69U	-693.9U	96.99U	-700.5U	95.60U	-707.4U	98.68U
IOH2-AMP	-1.273M	216.2U	-1.267M	216.6U	-1.279M	214.1U	-1.292M	219.6U
IOLX-AMP	274.9U	34.63U	273.5U	33.84U	275.6U	33.79U	276.0U	33.66U
IOHX-AMP	-197.0U	23.56U	-195.7U	23.35U	-197.3U	23.26U	-197.8U	23.62U
VIH1-VDC	3.100	70.70M	3.100	70.70M	3.100	70.70M	3.100	70.70M
VIH2-VDC	6.225	108.9M	6.225	108.9M	6.225	108.9M	6.225	108.9M
VIL2-VDC	4.150	111.8M	4.175	82.90M	4.150	111.8M	4.150	111.8M
EF.SETUP.1	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000
EF.SETUP.2	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000
EF.HOLD.1	155.0N	20.62N	162.5N	21.65N	160.0N	22.36N	157.5N	19.20N
EF.HOLD.2	72.50N	8.292N	75.00N	5.000N	75.00N	5.000N	72.50N	8.292N
DATA.SETUP.1	-65.00N	11.18N	-65.00N	8.660N	-65.00N	8.660N	-65.00N	8.660N
DATA.SETUP.2	-27.50N	4.330N	-27.50N	4.330N	-27.50N	4.330N	-27.50N	4.330N
DATA.HOLD.1	245.0N	25.98N	245.0N	25.98N	242.5N	23.85N	245.0N	25.98N
DATA.HOLD.2	112.5N	8.291N	112.5N	8.291N	112.5N	8.291N	112.5N	8.291N
INT.SETUP.1	-145.0N	16.58N	-145.0N	16.58N	-145.0N	16.58N	-145.0N	16.58N
INT.SETUP.2	-55.00N	5.000N	-55.00N	4.999N	-55.00N	4.999N	-55.00N	4.999N
INT.HOLD.1	137.5N	12.99N	130.0N	12.25N	130.0N	12.25N	130.0N	12.25N
INT.HOLD.2	65.00N	5.000N	55.00N	5.000N	55.00N	5.000N	55.00N	5.000N
DMAI.SETUP.1	-190.0N	21.21N	-190.0N	21.21N	-187.5N	19.20N	-187.5N	19.20N
DMAI.SETUP.2	-80.00N	10.00N	-72.50N	8.292N	-72.50N	8.292N	-72.50N	8.292N
DMAI.HOLD.1	137.5N	12.99N	135.0N	16.58N	135.0N	16.58N	135.0N	16.58N
DMAI.HOLD.2	60.00N	7.070N	55.00N	5.000N	55.00N	5.000N	55.00N	5.000N
DMAO.SETUP.1	-197.5N	19.20N	-192.5N	17.85N	-190.0N	21.21N	-190.0N	21.21N
DMAO.SETUP.2	-82.50N	8.292N	-72.50N	8.292N	-72.50N	8.292N	-72.50N	8.292N
DMAO.HOLD.1	147.5N	12.99N	137.5N	12.99N	137.5N	12.99N	137.5N	12.99N
DMAO.HOLD.2	65.00N	5.000N	55.00N	5.000N	55.00N	5.000N	55.00N	5.000N
WAIT.SETUP.1	-150.0N	0.000	-150.0N	0.000	-150.0N	0.000	-150.0N	0.000
WAIT.SETUP.2	-150.0N	0.000	-150.0N	0.000	-150.0N	0.000	-150.0N	0.000
PW.CLK.1	137.5N	12.99N	137.5N	12.99N	137.5N	12.99N	137.5N	12.99N
PW.CLK.2	65.00N	5.000N	57.50N	4.329N	57.50N	4.329N	57.50N	4.329N
PW.CLK.1	20.00N	0.000	20.00N	0.000	20.00N	0.000	20.00N	0.000
PW.CLK.2	20.00N	0.000	20.00N	0.000	20.00N	0.000	20.00N	0.000

TABLE D-4. 1802 PARAMETER SUMMARIES OF THE DEMONSTRATION TEST CONTROL GROUP (125°C DATA) (CONTINUED)

PARAMETER	CUMULATIVE HOURS							
	INITIAL		72 HOURS		168 HOURS		500 HOURS	
	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA
TPLH1-TFA/B	294.3N	34.77N	294.3N	35.74N	291.3N	34.85N	293.4N	35.77N
TPLH1-MWR	260.9N	25.27N	243.8N	24.77N	241.9N	23.88N	258.7N	24.68N
TPLH1-MRD	330.6N	30.76N	334.0N	31.14N	332.3N	29.86N	315.3N	29.76N
TPLH1 N	398.0N	42.93N	397.7N	43.00N	394.4N	42.25N	394.8N	42.07N
TPLH1 Q	421.3N	39.74N	421.5N	39.67N	418.5N	38.33N	419.6N	38.63N
TPHL1-TFA/B	300.3N	37.83N	303.3N	38.19N	300.0N	37.23N	301.9N	37.87N
TPHL1-MWR	301.8N	32.70N	287.8N	31.62N	284.9N	30.75N	300.6N	32.23N
TPHL1 MRD	298.9N	32.93N	299.9N	33.11N	297.3N	32.02N	285.3N	30.89N
TPHL1-N	413.1N	48.37N	413.1N	49.35N	409.2N	48.25N	410.5N	48.21N
TPHL1-Q	430.0N	45.82N	431.6N	46.13N	427.5N	44.60N	429.8N	44.70N
TPLH2-TFA/B	129.3N	14.29N	127.9N	14.67N	126.7N	14.19N	127.7N	14.76N
TPLH2-MWR	112.4N	10.60N	99.88N	10.07N	98.88N	9.691N	108.6N	10.28N
TPLH2-MRD	143.9N	12.71N	143.5N	12.56N	142.9N	11.99N	131.4N	12.35N
TPLH2-N	179.3N	18.20N	177.0N	18.22N	175.3N	17.92N	175.5N	17.71N
TPLH2-Q	192.1N	16.29N	189.4N	16.24N	187.5N	15.53N	188.2N	15.59N
TPHL2-TFA/B	125.6N	14.74N	126.2N	14.93N	124.6N	14.50N	125.8N	14.68N
TPHL2-MWR	123.9N	13.32N	114.7N	12.89N	113.3N	12.52N	120.5N	13.19N
TPHL2-MRD	127.9N	13.46N	126.8N	13.55N	125.5N	12.94N	120.0N	12.53N
TPHL2-N	183.6N	19.07N	181.9N	19.78N	180.0N	19.21N	180.7N	19.17N
TPHL2-Q	189.3N	17.67N	189.6N	17.75N	187.4N	17.00N	188.5N	17.13N
DO.DELAY.1	467.5N	43.23N	470.0N	46.09N	462.5N	44.37N	465.0N	46.37N
DO.DELAY.2	220.0N	20.61N	220.0N	20.61N	220.0N	20.61N	217.5N	17.85N
SC.DELAY.1	432.5N	44.37N	432.5N	44.37N	427.5N	39.60N	430.0N	41.53N
SC.DELAY.2	187.5N	17.85N	187.5N	17.85N	185.0N	15.81N	187.5N	17.85N
ADHI.DELAY.1	835.0N	89.16N	840.0N	88.74N	835.0N	89.16N	832.5N	86.42N
ADHI.DELAY.2	355.0N	36.74N	357.5N	33.45N	352.5N	34.91N	357.5N	33.45N
ADLO.DELAY.1	340.0N	41.53N	342.5N	38.32N	337.5N	39.61N	340.0N	41.53N
ADLO.DELAY.2	152.5N	12.99N	152.5N	12.99N	152.5N	12.99N	152.5N	12.99N

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