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Monolithic Microwave Integrated Circuits (MMIC) Broadband Power Amplifiers

by John E. Penn

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14. ABSTRACT

A broadband power amplifier design approach was used to design several monolithic microwave integrated circuits (MMICs) using a 0.13-μm gallium arsenide (GaAs) pseudomorphic high electron mobility transistor (PHEMT) process from TriQuint Semiconductor. The design and fabrication of these circuits were performed as part of the fall 2011 Johns Hopkins University (JHU) MMIC Design Course, taught by the author. The design approach is taught by Dale Dawson in the JHU Power MMIC Design Course. This approach is useful for designing relatively broadband amplifiers that are limited only be the active transistor's "Q".

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1. Introduction

A broadband power amplifier design approach was used to design several monolithic microwave integrated circuits (MMICs) using a 0.13-µm gallium arsenide (GaAs) pseudomorphic high electron mobility transistor (PHEMT) process from TriQuint Semiconductor. The design and fabrication of these circuits were performed as part of the fall 2011 Johns Hopkins University (JHU) MMIC Design Course, taught by the author. The design approach is taught by Dale Dawson in the JHU Power MMIC Design Course, and is useful for designing relatively broadband amplifiers that are only limited by the initial "Q" of the active transistor. This fundamental limitation to the design bandwidth will be a function of the electrical characteristics of the starting device. This same double Q matching technique was used to successfully design two high power broadband MMIC amplifiers at 3–5 and 4–6 GHz using TriQuint's 0.25-µm gallium nitride (GaN) process (see ARL-TR-5987[1] and ARL-TR-6090[2]).

2. Broadband Power Amplifier Device Limitations ("Q")

The design approach starts with the limiting characteristics of the active device for the power amplifier. A single standard-sized pseudomorphic high electron mobility transistor (PHEMT) (6x50 µm) is used for a broadband Class A (or mildly AB) power amplifier centered around 8 GHz, and later 4 GHz for a second design. The simple "Cripps" approach, named after Steve Cripps, models the ideal "Class A" output (drain) power match of the PHEMT as a parallel resistance (Rcripps) and parallel capacitance (CDS). To maximize the output voltage and current swings, the Rcripps value is determined from a DC current-voltage (I-V) load line (figure 1). The nonlinear shunt output capacitance is assumed to be close to the linear output capacitance, which is determined by fitting the output match to a parallel resistance (RDS) and a parallel capacitance (CDS) (figure 2). RDS is not actually needed and will be replaced by Rcripps. The output matching circuit is then designed based on the parallel combination of CDS and Rcripps obtained from these first two steps. Rcripps is approximately 50 Ω (6.5 V swing/130 mA) and the output capacitance is approximately 400 fF at 8 GHz. It should be noted that the PHEMT was already stabilized with a series gate resistance of 18 Ω plus a shunt resistance of 120 Ω. There may be a subtle difference between the match of the stabilized PHEMT versus an unstabilized PHEMT, but then the Cripps method is an approximation, and I prefer to stabilize

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[1]Penn, John E. *Broadband, Efficient, Lineaer C-Band Power Amplifiers Designed in a 0.25-µm Gallium Nitride (GaN) Foundry Process from TriQuint Semiconductor*; ARL-TR-5987; U.S. Army Research Laboratory: Adelphi, MD, 2012.

[2]Penn, John E. *Testing of Two Broadband, Efficient, Lineaer C-Band Power Amplifiers Designed in a 0.25-µm Gallium Nitride (GaN) Foundry Process from TriQuint Semiconductor*; ARL-TR-6090; U.S. Army Research Laboratory: Adelphi, MD, 2012.

the device at the start. If the active device was unilateral (S12=0), then the output match would not change due to stabilizing resistors on the input (gate). The ratio of the complex impedance to the real impedance of the output match is the "Q" or limiting factor to bandwidth.
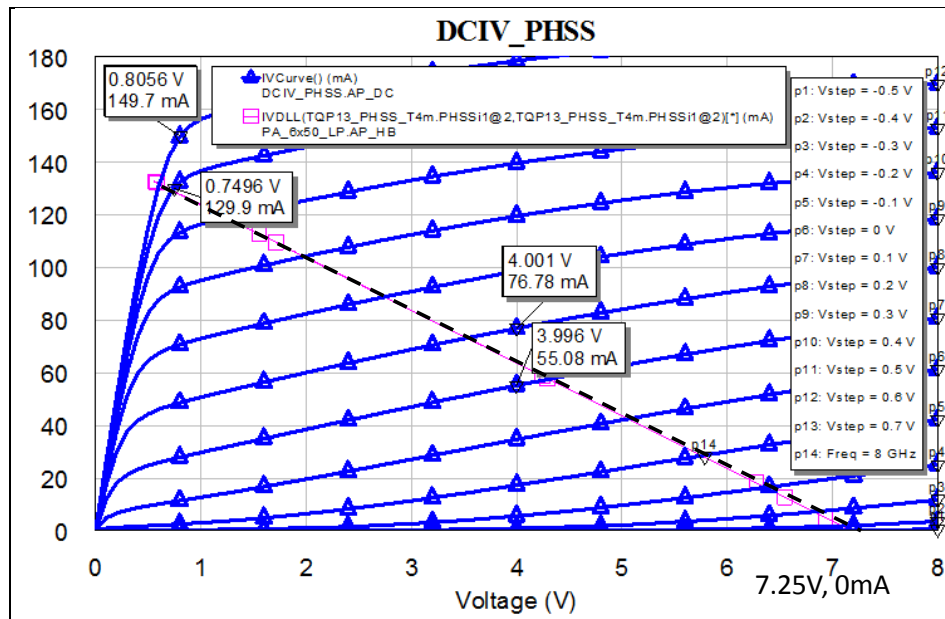

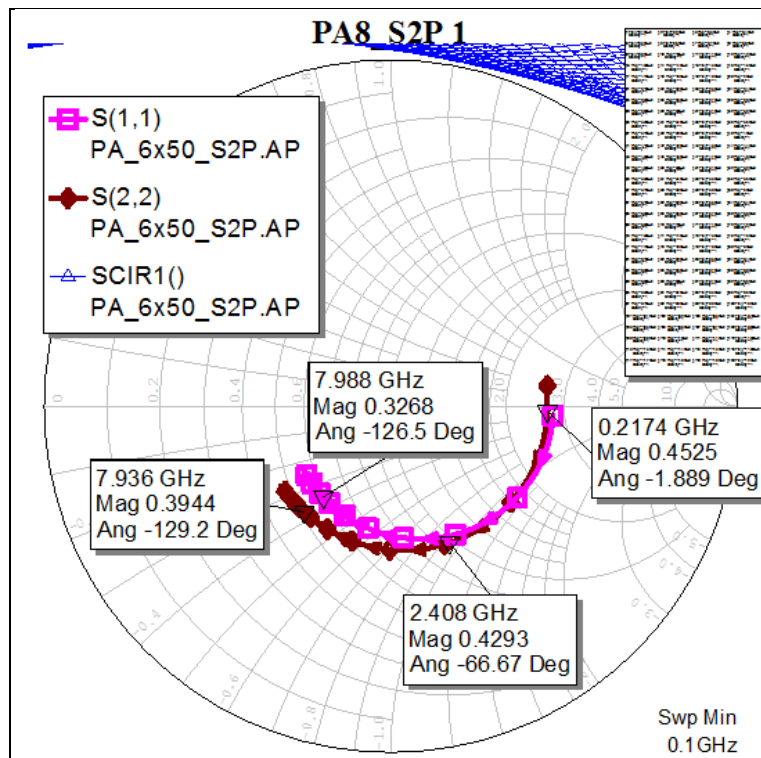Figure 1. DC I-V characteristics of 6x50 μm PHEMT (TQP13 process).

Figure 2. Small signal S22 (output impedance) of 6x50 μm PHEMT.

3. Nonlinear "Software" Load-pull Simulations

The beauty of the Cripps approach is that the design can start with just DC I-V curves and S-parameters, which are usually easy to obtain or measure. If a good nonlinear model exists, the Cripps approach is still useful as a starting point for the design, and then nonlinear simulations can be performed to iterate and optimize the amplifier design. Many of the computer-aided design (CAD) tools such as Microwave Office (MWO) have a software load-pull simulation capability. These load-pull simulations emulate actual load-pull measurements, which require costly test equipment, accurate measurements, and time to perform the measurements over the desired frequencies, power levels, and DC bias conditions. One can quickly perform simulations similar to a load-pull system at different DC biases, frequencies, and power levels, with the limitation set by the accuracy of the nonlinear model provided to the designer.

Using the nonlinear TOM4 model for the 6x50 µm PHEMT at a DC bias of 4 V on the drain and 0 V on the gate, two CAD load-pull simulations are performed to generate contours of output power and power added efficiency (PAE) at 8 GHz (figures 3 and 4). For best output power (Pout), the output match is approximately 41.3 Ω in parallel with 198 fF, for a "Q" of 0.4. Using the two sets of contours, the best output power match would yield 21.5 dBm of output power at 48% PAE. For best PAE, the output match is approximately 72.5 Ω in parallel with 183 fF, for a "Q" of 0.7. Again, interpolating both load-pull simulations, the best efficiency should yield 20.7 dBm of output power at 53% PAE. Choosing a compromise match, between best PAE and best Pout, of 58 Ω in parallel with 200 fF for a "Q" of 0.6, should yield 21.1 dBm of output power at 52% PAE—based on the nonlinear model at the simulated conditions with ideal lossless matching elements.
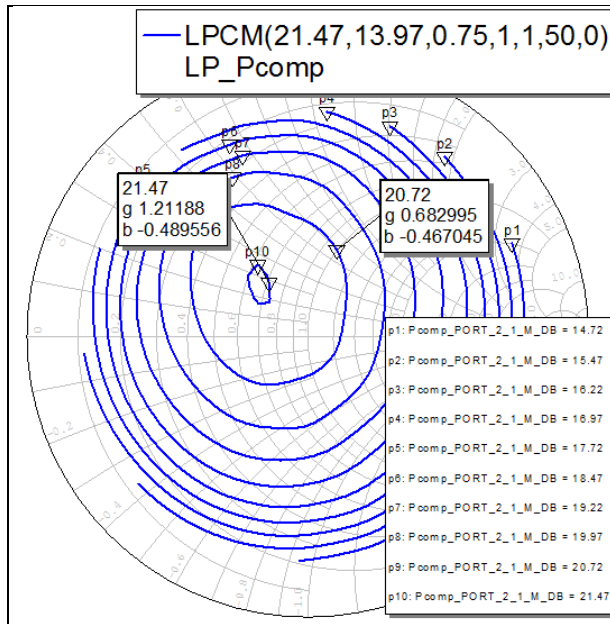
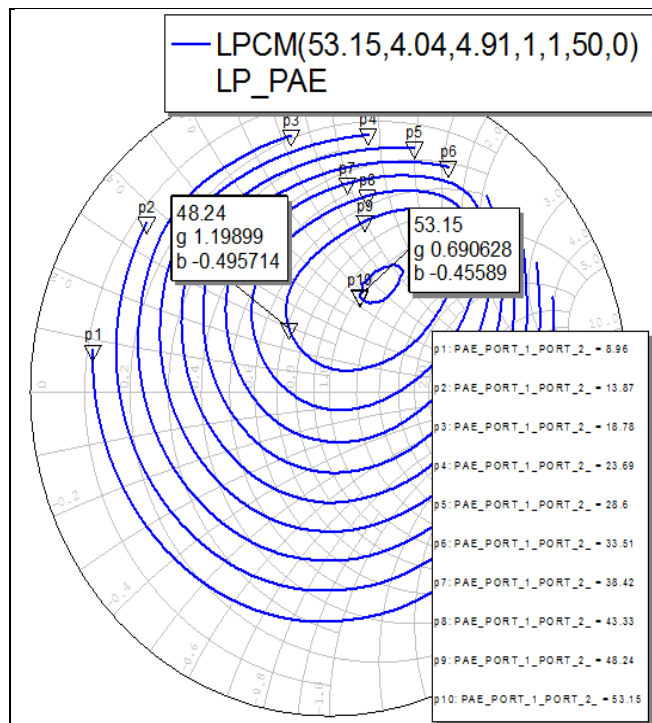Figure 3. An 8-GHz load pull-simulation of output power (Pcomp-6x50 µm PHEMT).

Figure 4. An 8-GHz load-pull simulation of PAE (6x50 µm PHEMT).

4. Double-Q Broadband Output Match

The lower the "Q" of the device, the broader the bandwidth can be—assuming ideal matching elements. The details of the approach taught in the Johns Hopkins University (JHU) Power Monolithic Microwave Integrated Circuits (MMIC) Design Course is summarized as a combination of a filter techniques and impedance transforms. After creating the initial ideal element output match, each ideal element is transformed into an equivalent MMIC "lossy" lumped element. This is where the science blends into "art" as each ideal element is replaced with a non-ideal element and the design is "re-tuned." Results will vary with each design and will likely increase in difficult with higher "Q"s and at higher frequency.

Figure 5 shows an initial ideal match, which consists of a parallel inductor (Lpar) to resonate out CDS at 8 GHz, then a series inductor/capacitor pair at twice the "Q" value, followed by a parallel output of the Rcripps, CDS, and Lpar. After a couple of transforms and replacing ideal elements with "lossy" MMIC lumped elements, the final matching circuit to 50 Ω is shown in figure 6, followed by the actual layout in figure 7. While the ideal match to the parallel RC model has little mismatch loss, the actual MMIC match has 0.5 to 0.75 dB of insertion loss over a large 5-GHz bandwidth around 8 GHz, as shown in figure 8 (note markers).
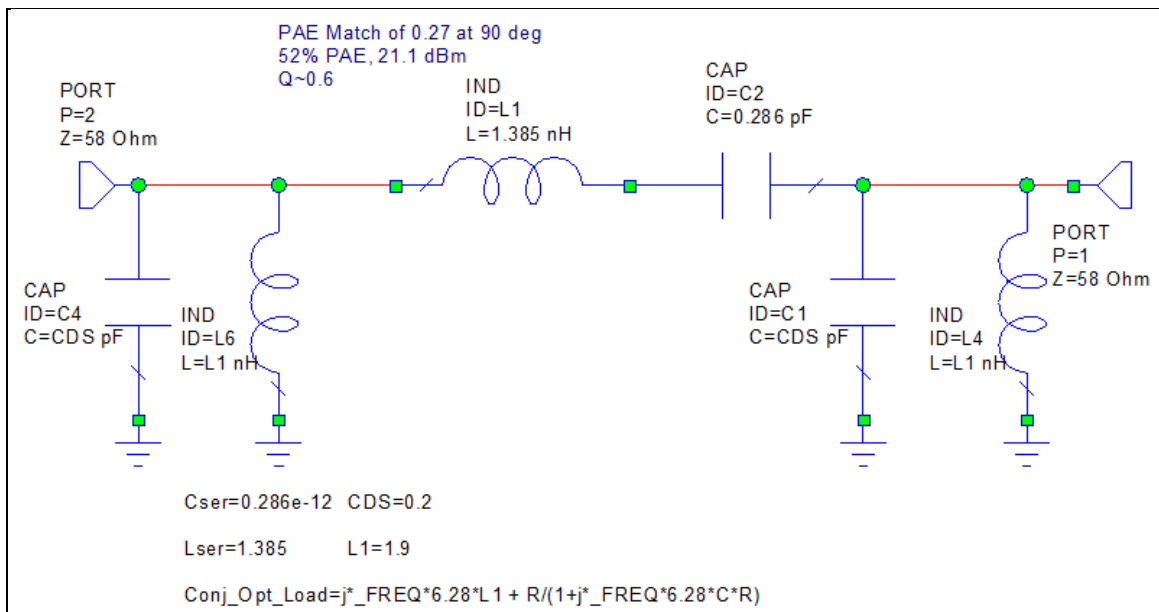

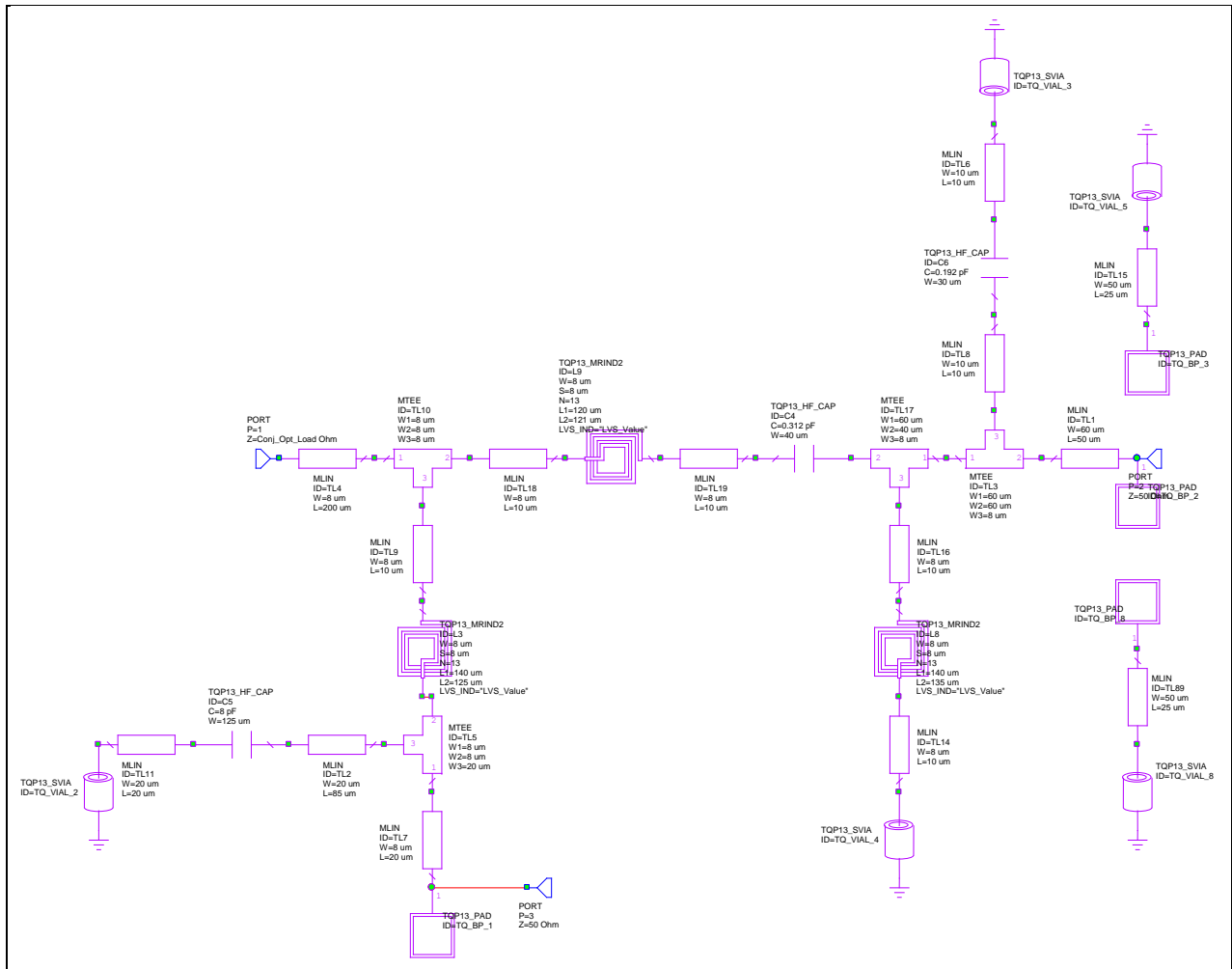Figure 5. Ideal double-Q matched output.
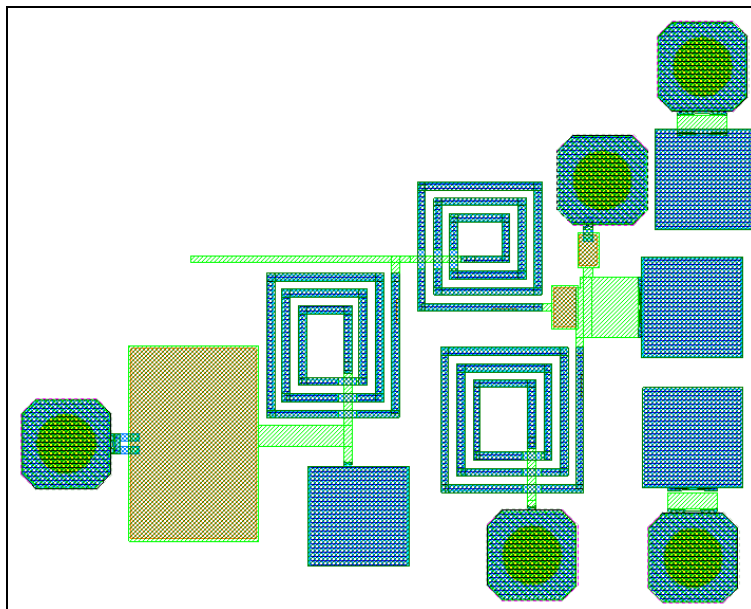
Figure 6. An 8-GHz MMIC output match schematic.

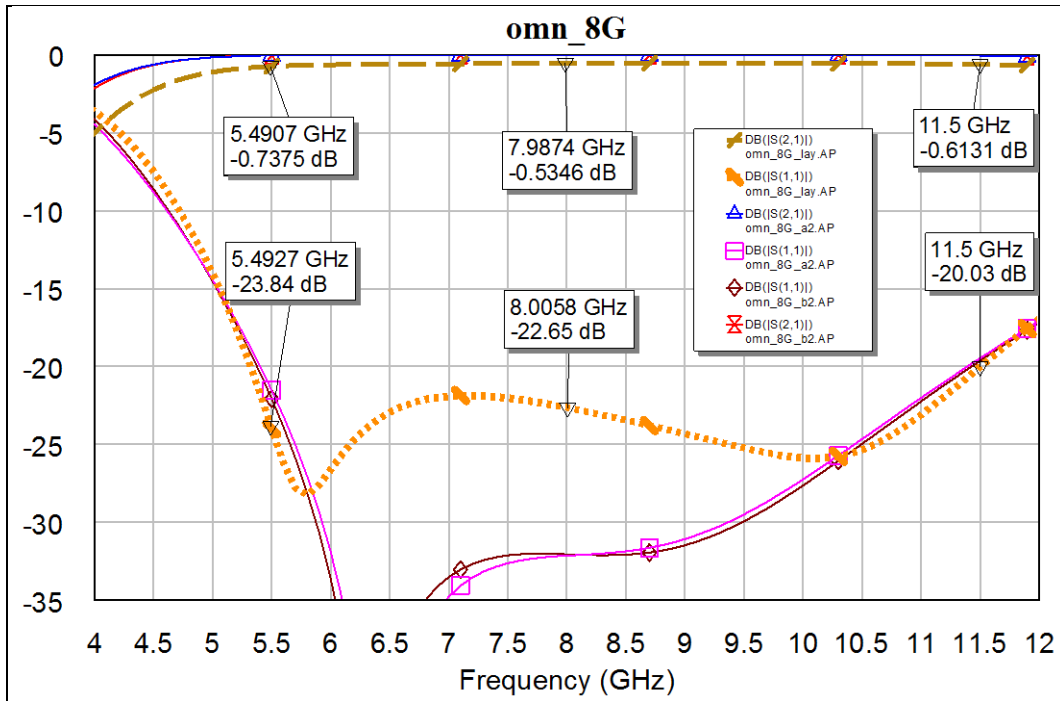Figure 7. An 8-GHz MMIC output match layout.

Figure 8. An 8-GHz MMIC broadband output match simulation.

5. Broadband Input Match

For a power amplifier, the output match is designed first. Next, the input match is designed so that it is not the bandwidth limiting factor for the power amplifier. With the broadband amplifier load attached to the stabilized PHEMT, the input S11 at 8 GHz is about 26 – j20.5 Ω for a Q of about 0.7—similar to the output Q. A simple four element high pass, low pass matching circuit is used to transform a 50-Ω input into a good broadband match for the amplifier. Once again, an ideal input match is replaced with "lossy" MMIC lumped elements one at a time and re-tuned, resulting in the broadband performance shown simulated in figure 9. The MMIC input match schematic including stabilizing resistors is shown in figure 10, followed by the layout in figure 11. A nonlinear simulation of the 5–11 GHz MMIC with expected output power and PAE at 7, 8, and 9 GHz predicts better than 21 dBm of output power (125 mW) and greater than 42% PAE (figure 12). DC Bias is 4 V on the drain and 0 V on the gate (Class AB, but simple to implement with only a single bias pad [Vdd] required, see layout figure 13).
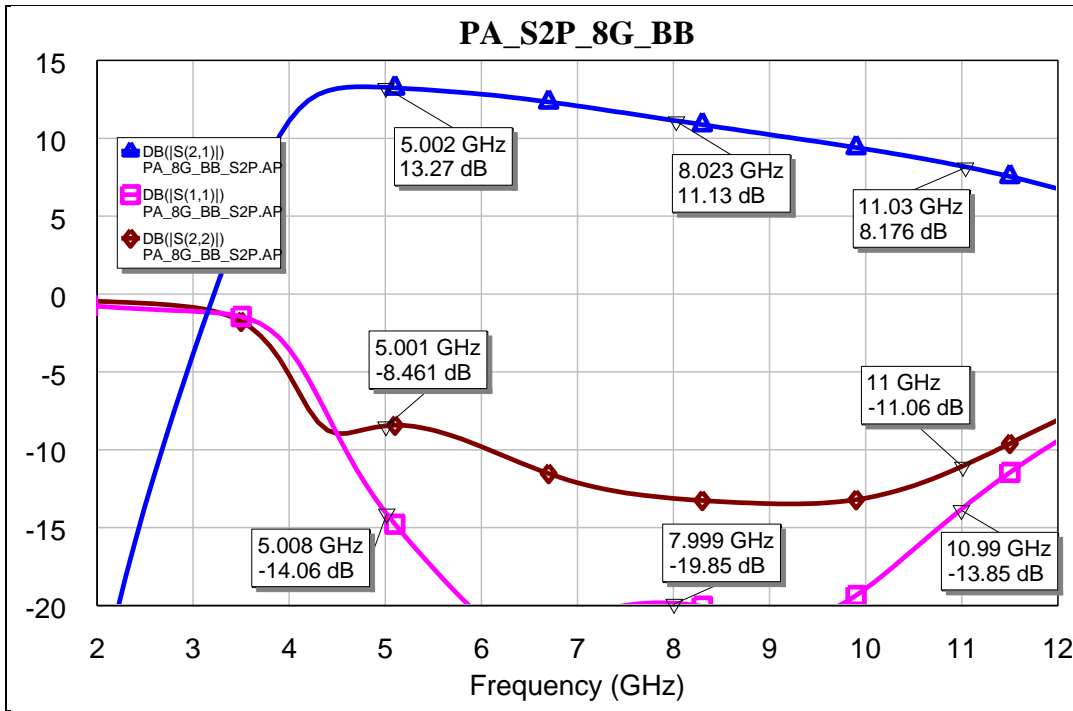
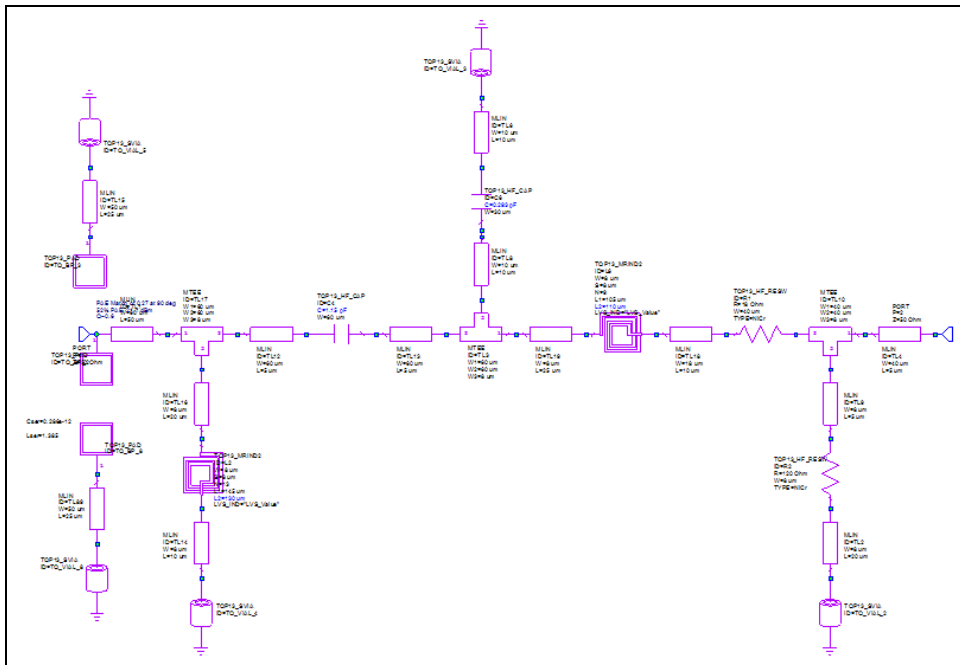Figure 9. MMIC 5–11 GHz broadband power amplifier linear simulation.

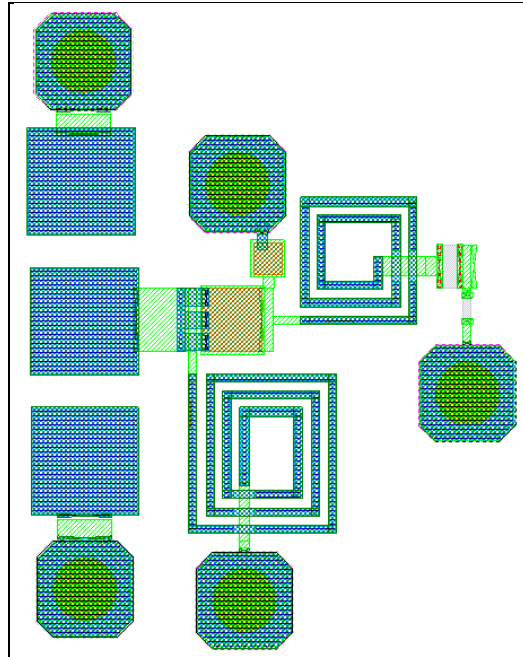Figure 10. MMIC 5–11 GHz input match schematic.

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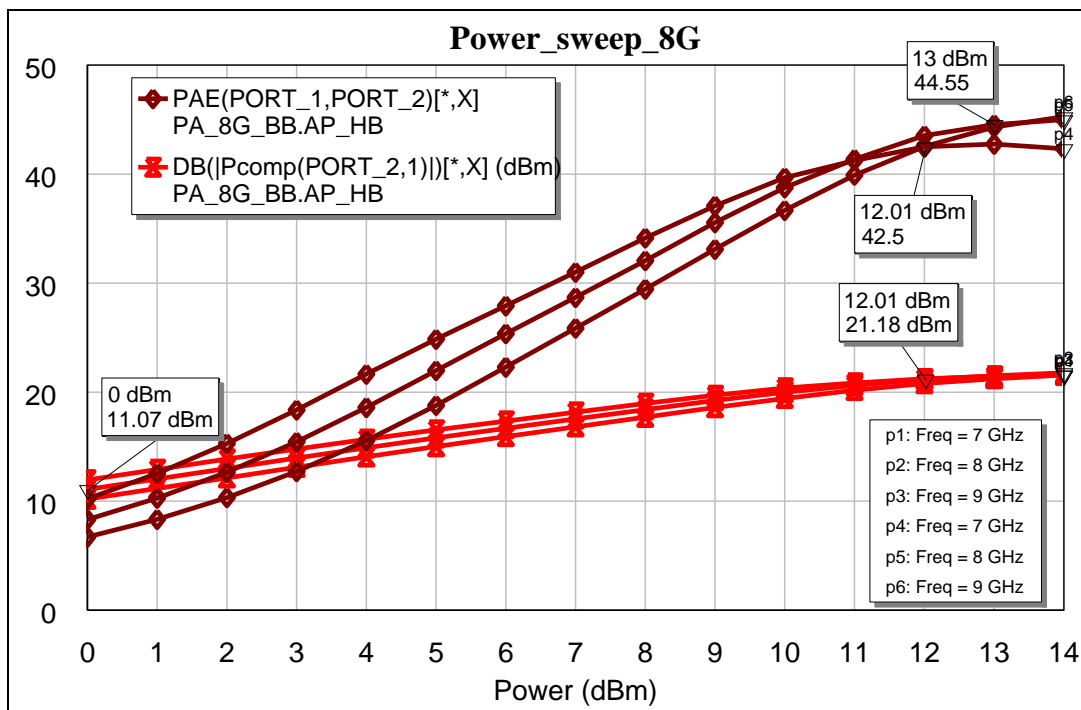Figure 11. MMIC 5–11 GHz input match layout.

Figure 12. MMIC 5–11 GHz output power and PAE performance simulation (7, 8, and 9 GHz).
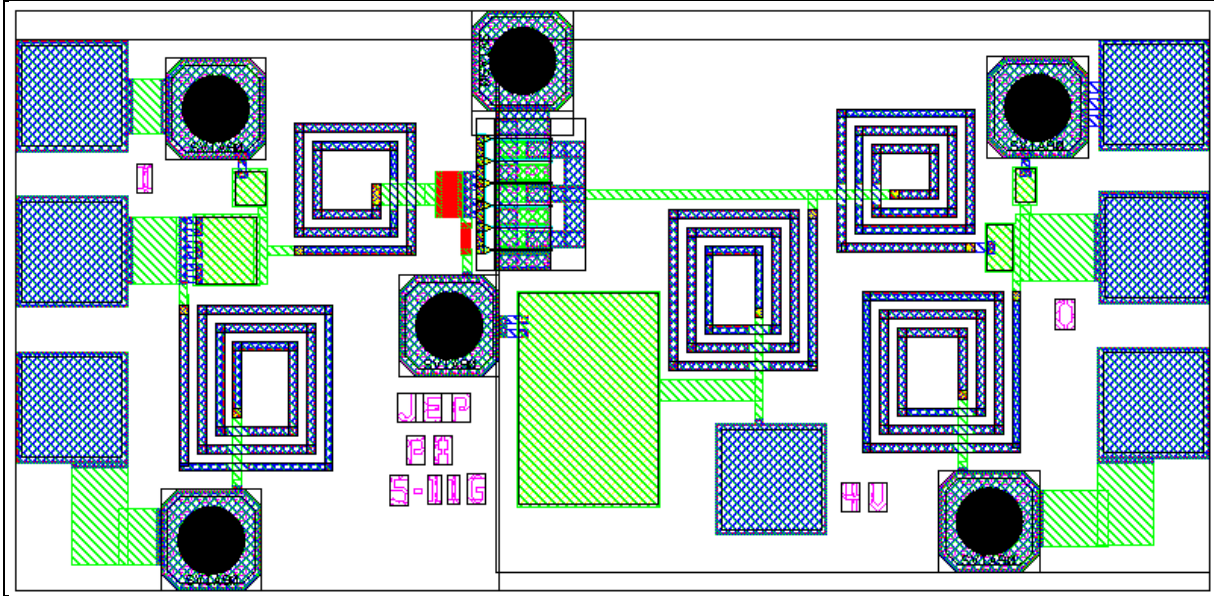
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Figure 13. Layout plot of the 5–11 GHz power amplifier (~1.1x0.55 mm).

6.   A 2–6 GHz Broadband Power Amplifier

The same design approach was used to center a design at 4 GHz. Topology and design steps are identical, resulting in a slightly larger layout at the lower frequency, as shown in figure 14. Again, a compromise was struck between the best output power and best efficiency using the nonlinear load-pull contours (figures 15 and 16). Best output match is approximately 45 Ω in parallel with 320 fF, for a "Q" of 0.4. Using the two sets of contours, the best output power match would yield 21.1 dBm of output power at 52% PAE. For best power added efficiency, the output match is approximately 132.5 Ω in parallel with 194 fF, for a "Q" of 0.65. Again, interpolating both load-pull simulations, the best efficiency should yield 19.3 dBm of output power at 59% PAE. Choosing a compromise match, between best PAE and best Pout, of 58 Ω in parallel with 290 fF for a "Q" of 0.45, should yield 20.8 dBm of output power at 54% PAE— based on the nonlinear model at the simulated conditions with ideal lossless matching elements.
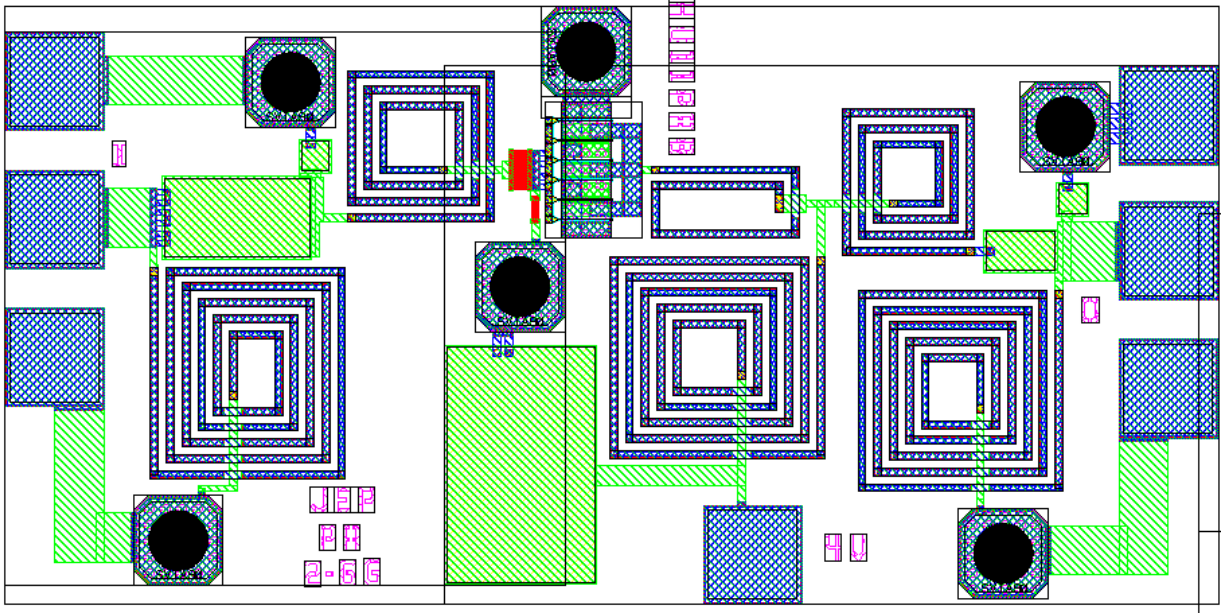
Figure 14. Layout plot of the 2–6 GHz power amplifier (~1.2x0.6 mm).
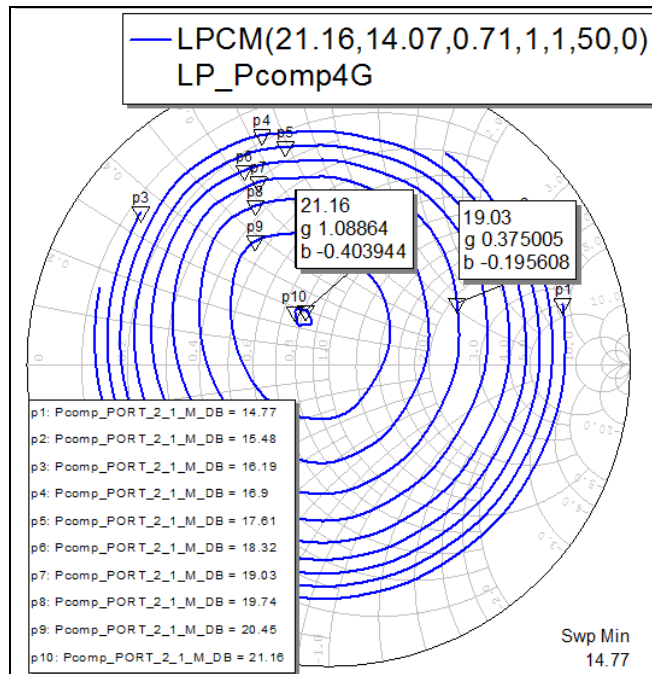
Figure 15. A 4-GHz load-pull simulation of output power
(Pcomp-6x50 μm PHEMT).
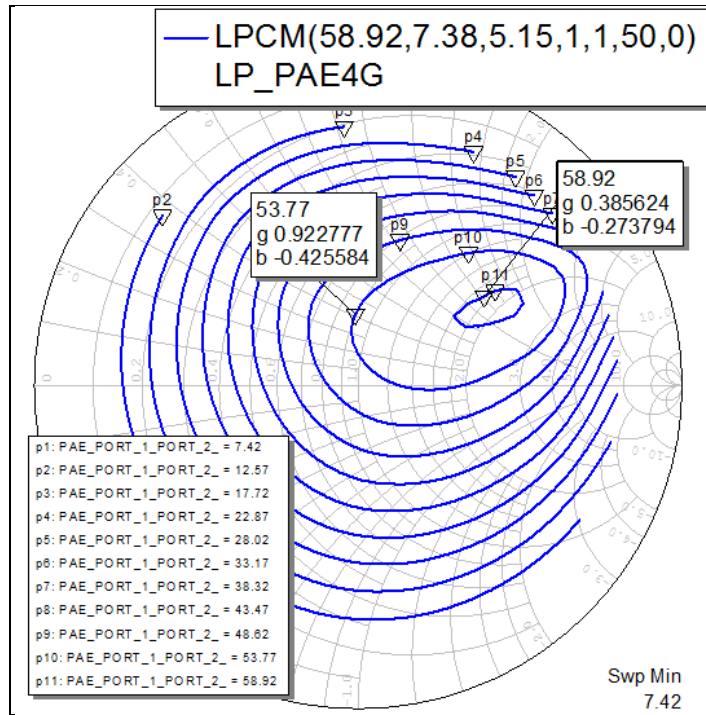
Figure 16. A 4-GHz load-pull simulation of PAE (6x50 μm PHEMT).

An input match and output match are created similarly to create a 2–6 GHz broadband amplifier with the expected linear performance shown in figure 17. A nonlinear simulation of the 2–6 GHz MMIC with expected output power and PAE at 3, 4, and 5 GHz predicts better than 20.9 dBm of output power (120 mW) and greater than 44% PAE (figure 18). Since gain falls off with increasing frequency for GaAs PHEMTs, the 2–6 GHz amplifier has slightly more gain than the 5–11 GHz version, and slightly higher PAE.

Figure 17. MMIC 2–6 GHz broadband power amplifier linear simulation.

Figure 18. MMIC 2–6 GHz output power and PAE performance simulation (3, 4, and 5 GHz).

7. Measured Results and Sonnet EM

Sonnet electromagnetic (EM) simulations were performed based on the actual physical layouts of both amplifier designs to look for parasitic coupling that might be un-simulated in a linear simulator, but the differences were slight. The S-parameter measurements agree very 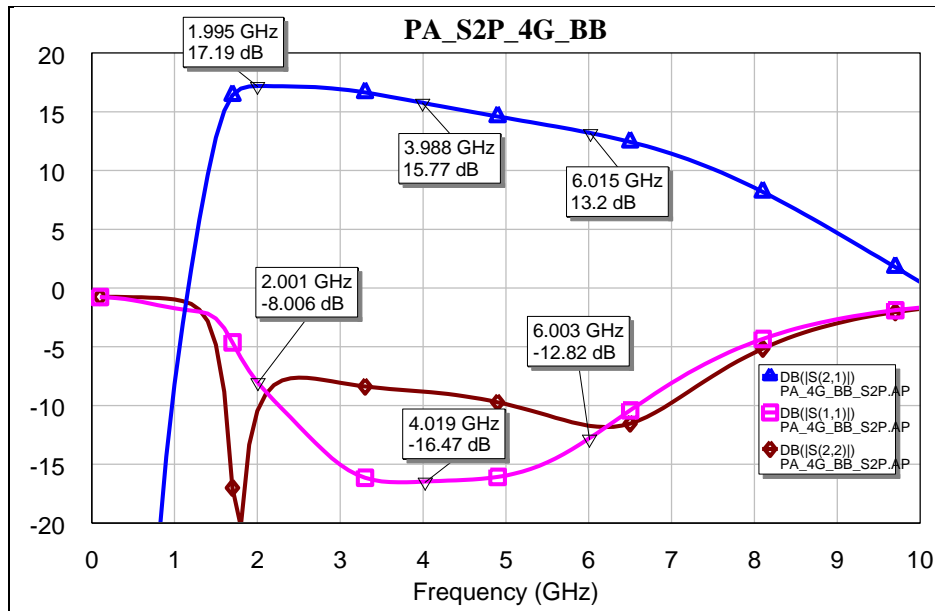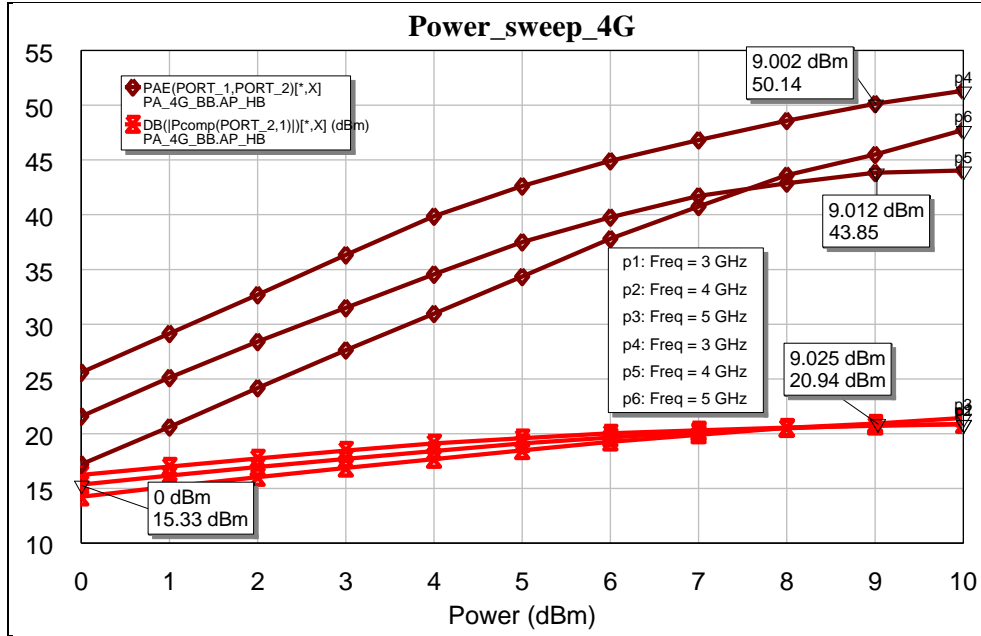well with the original MWO simulations. Figures 19 and 20 show the measured versus MWO versus Sonnet EM simulations, showing good agreement. Power performance was lower than predicted. Measurements were taken at the designed for bias of 4 V yielding slightly less output power and lower PAE, though the results compared similarly across the broadband. Efficiencies were slightly better with the higher gain 2–6 GHz broadband power amplifier. Additionally, performance was measured with a supply voltage of 3.5, 4, and 4.5 V, showing more output power with a higher DC supply but better PAE at 3.5 V—as might be expected. This was true of both amplifiers; the only real difference was the operating frequency, either 2–6 or 5–11 GHz. Table 1 and figure 21 summarize the performance of the 2–6 GHz amplifier at midband (4 GHz). Likewise, table 2 and figure 22 summarize the performance of the 5–11 GHz amplifier at 7 GHz. Plots of performance at 3.5, 4, and 4.5 V for the 2–6 GHz amplifier at 4 GHz are shown in figure 23, with more output power at the higher voltage but better efficiency at the lower voltage. Likewise, plots of performance at 3.5, 4, and 4.5 V for the 5–11 GHz amplifier at 8 GHz are shown in figure 24, with more output power at the higher voltage but better efficiency at the lower voltage. Both amplifiers worked well with the broadband matching techniques and acted similarly in performance over their band of operation.
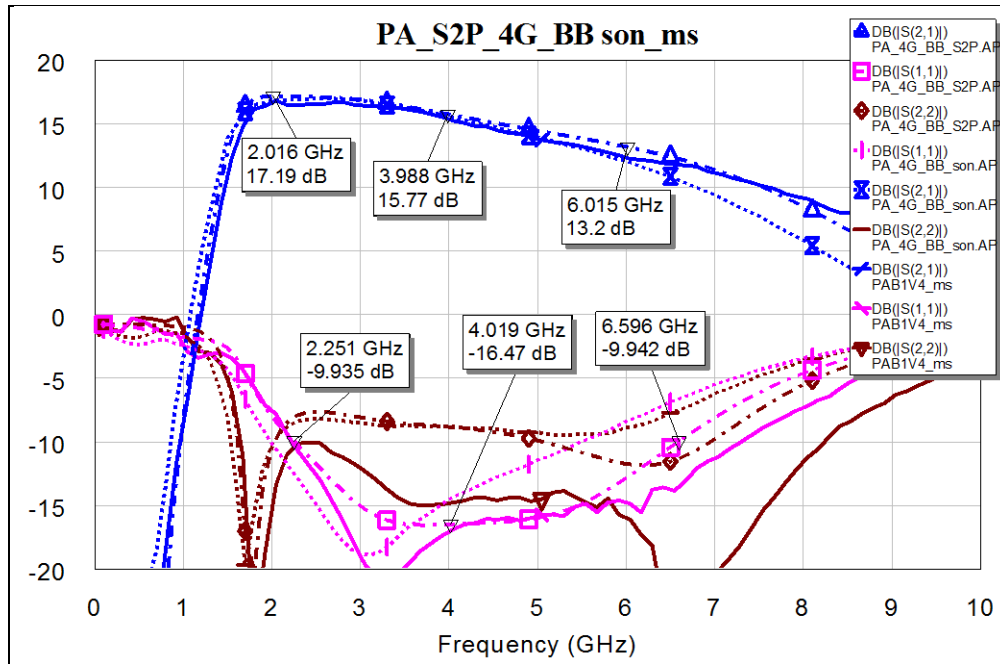
Figure 19. S-parameters of the 2–6 GHz broadband power amplifier (measured-solid, MWO-dot/dash, and sonnet--dotted).
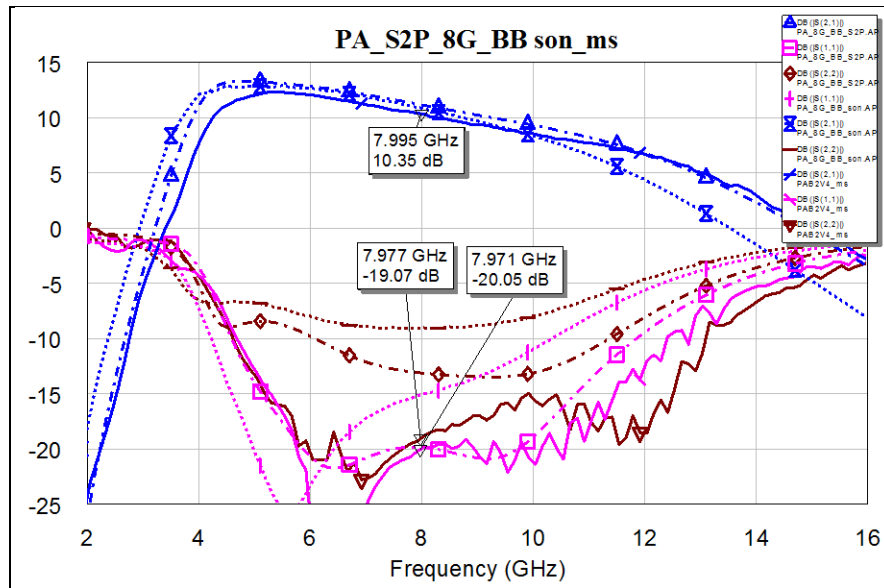

Figure 20. S-parameters of the 5–11 GHz broadband power amplifier (measured-solid, MWO-dot/dash, and Sonnet--dotted).

Table 1. Power performance at 4 GHz (midband) for the 2–6 GHz broadband amplifier.

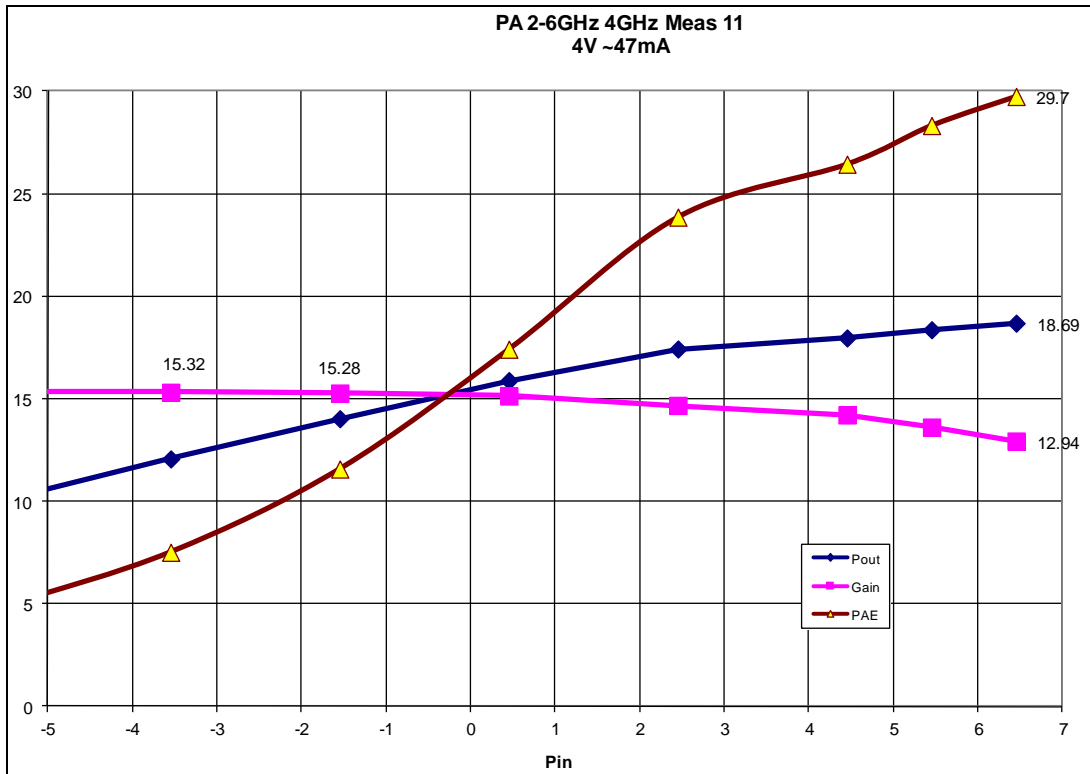| 4 GHz	Die#1	2-6 GHz Fall11 TQP13				4V ; 51 mA			
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(4V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-4.0	8.82	-5.25	10.07	15.32	51	204.0	10.16	5.0	4.8
-2.0	10.82	-3.25	12.07	15.32	52	208.0	16.11	7.7	7.5
0.0	12.78	-1.25	14.03	15.28	53	212.0	25.29	11.9	11.6
2.0	14.64	0.75	15.89	15.14	54	216.0	38.82	18.0	17.4
4.0	16.18	2.75	17.43	14.68	56	224.0	55.34	24.7	23.9
5.0	16.72	3.75	17.97	14.22	57	228.0	62.66	27.5	26.4
6.0	17.12	4.75	18.37	13.62	58	232.0	68.71	29.6	28.3
7.0	17.44	5.75	**18.69**	**12.94**	59	236.0	**73.96**	**31.3**	**29.7**

Figure 21. Power performance of the 2–6 GHz amplifier at 4 GHz (4 V).

Table 2. Power performance at 7 GHz (~midband) for the 5-11 GHz broadband amplifier.

| 7 GHz	Die#1	5-11 GHz Fall11 TQP13				4V ; 53 mA			
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(4V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-6.0	-0.05	-8.40	2.35	10.75	53	212.0	1.72	0.8	0.7
-4.0	2.00	-6.40	4.40	10.80	53	212.0	2.75	1.3	1.2
-2.0	3.92	-4.40	6.32	10.72	53	212.0	4.29	2.0	1.9
0.0	5.96	-2.40	8.36	10.76	54	216.0	6.85	3.2	2.9
2.0	7.97	-0.40	10.37	10.77	54	216.0	10.89	5.0	4.6
4.0	9.97	1.60	12.37	10.77	54	216.0	17.26	8.0	7.3
6.0	11.93	3.60	14.33	10.73	55	220.0	27.10	12.3	11.3
8.0	13.85	5.60	16.25	10.65	56	224.0	42.17	18.8	17.2
10.0	15.57	7.60	17.97	**10.37**	57	228.0	62.66	**27.5**	**25.0**
11.0	16.15	8.60	18.55	**9.95**	57	228.0	71.61	**31.4**	**28.2**
12.0	16.65	9.60	19.05	**9.45**	58	232.0	80.35	**34.6**	**30.7**
13.0	17.03	10.60	**19.43**	**8.83**	58	232.0	87.70	**37.8**	**32.9**
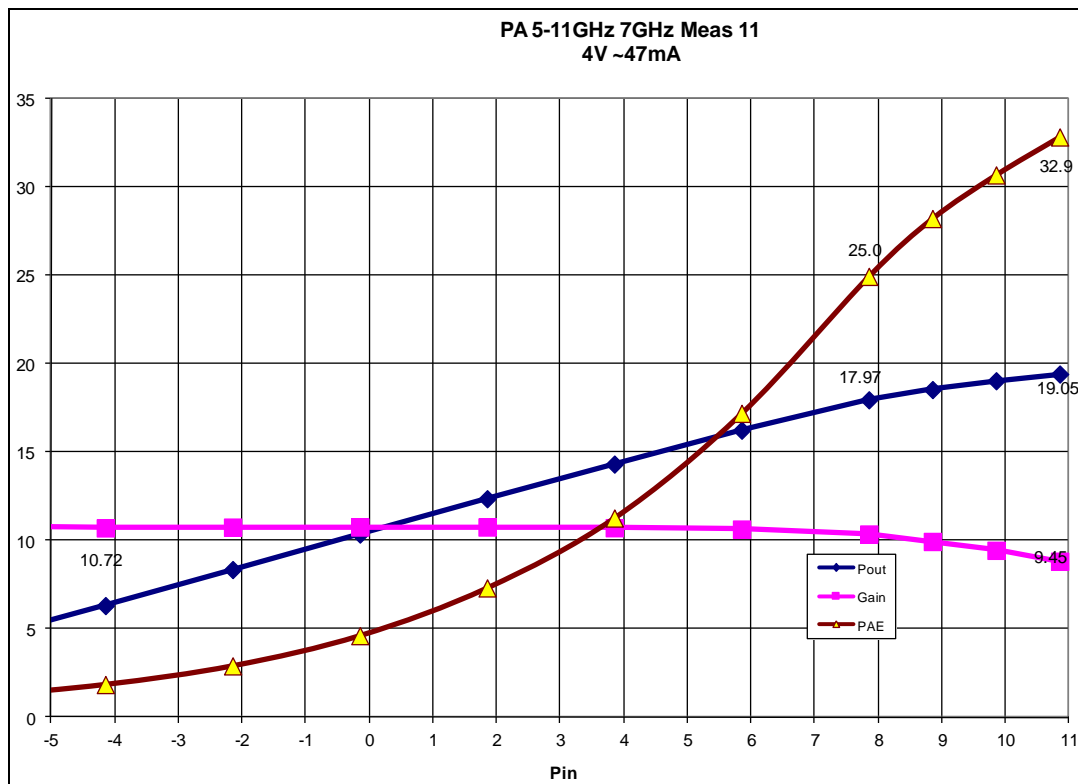
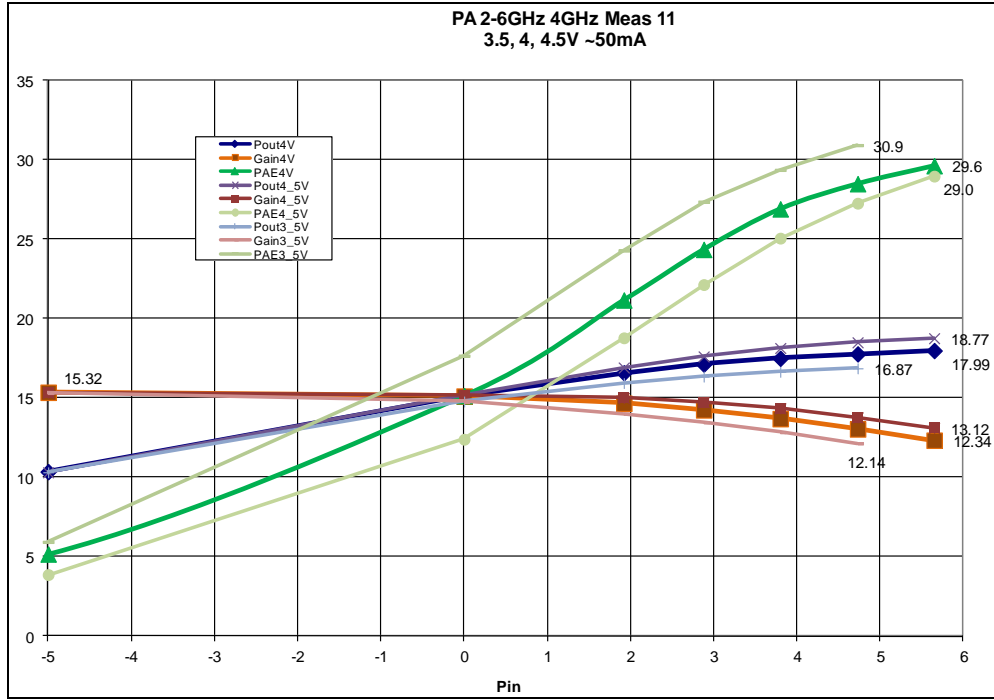Figure 22. Power performance of the 5–11 GHz amplifier at 7 GHz (4 V).

Figure 23. Power performance of the 2–6 GHz amplifier at 4 GHz (3.5, 4, and 4.5 V).
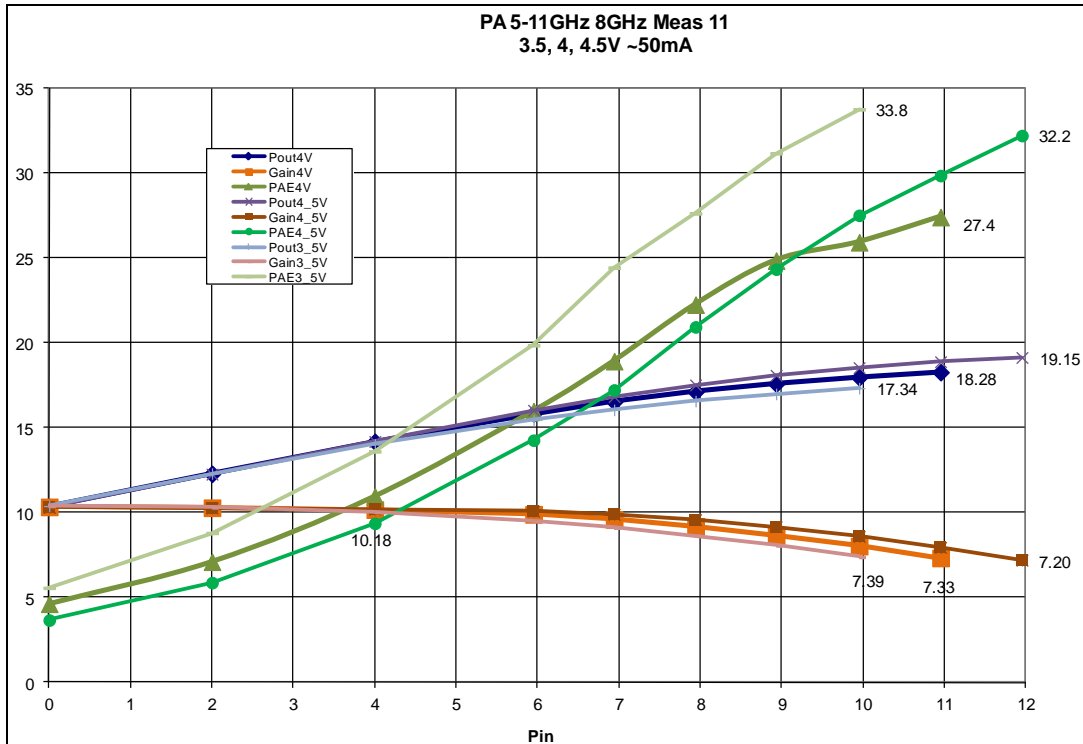

Figure 24. Power performance of the 5–11 GHz amplifier at 8 GHz (3.5, 4, and 4.5 V).

8. The Challenge of Higher Frequency: 28-GHz Broadband Power Amplifier

The same design approach was used to attempt a broadband design around 28 GHz. Several issues conspire to make this design much harder. Gain tends to fall off with frequency with GaAs transistors, so there will be less gain and PAE at the higher frequency. To minimize the impact in gain when stabilizing the same 6x50 µm PHEMT device used for the previous two amplifier designs, a parallel resistor and capacitor combination is used in series with the gate where the resistor helps the stability at low frequency and as the frequency increase, the capacitor increasingly bypasses the resistor so that available gain at the higher frequencies is increased. For stability, the same 120-Ω shunt resistor is used on the gate but the series resistor becomes 25 Ω in parallel with a 1.2-pF capacitor.

A second challenge is that the "Q" of the PHEMT increases at higher frequencies resulting in a narrower bandwidth. Third, the higher the frequency and Q increases the harder it is to convert ideal elements into lossy MMIC elements while maintaining good performance. Initially, the ideal matching topology and design steps are identical to the 4- and 8-GHz designs. A load-pull simulation based on the nonlinear model of the stabilized 6x50 µm PHEMT is performed (see schematic in figure 25). Again, the load-pull contours are used to find a compromise between the best output power and best efficiency (figures 26 and 27). An output load equivalent to 58 Ω in parallel with 143 fF, for a "Q" of 1.5, should yield ~19 dBm of output power at 35% PAE, assuming ideal lossless matching elements. The schematic of the final matching circuit to 50 Ω is shown in figure 28. Note the much narrower bandwidth and increased mismatch loss of the broadband "lossy" MMIC output match around 28 GHz, as shown in figure 29 (note markers).
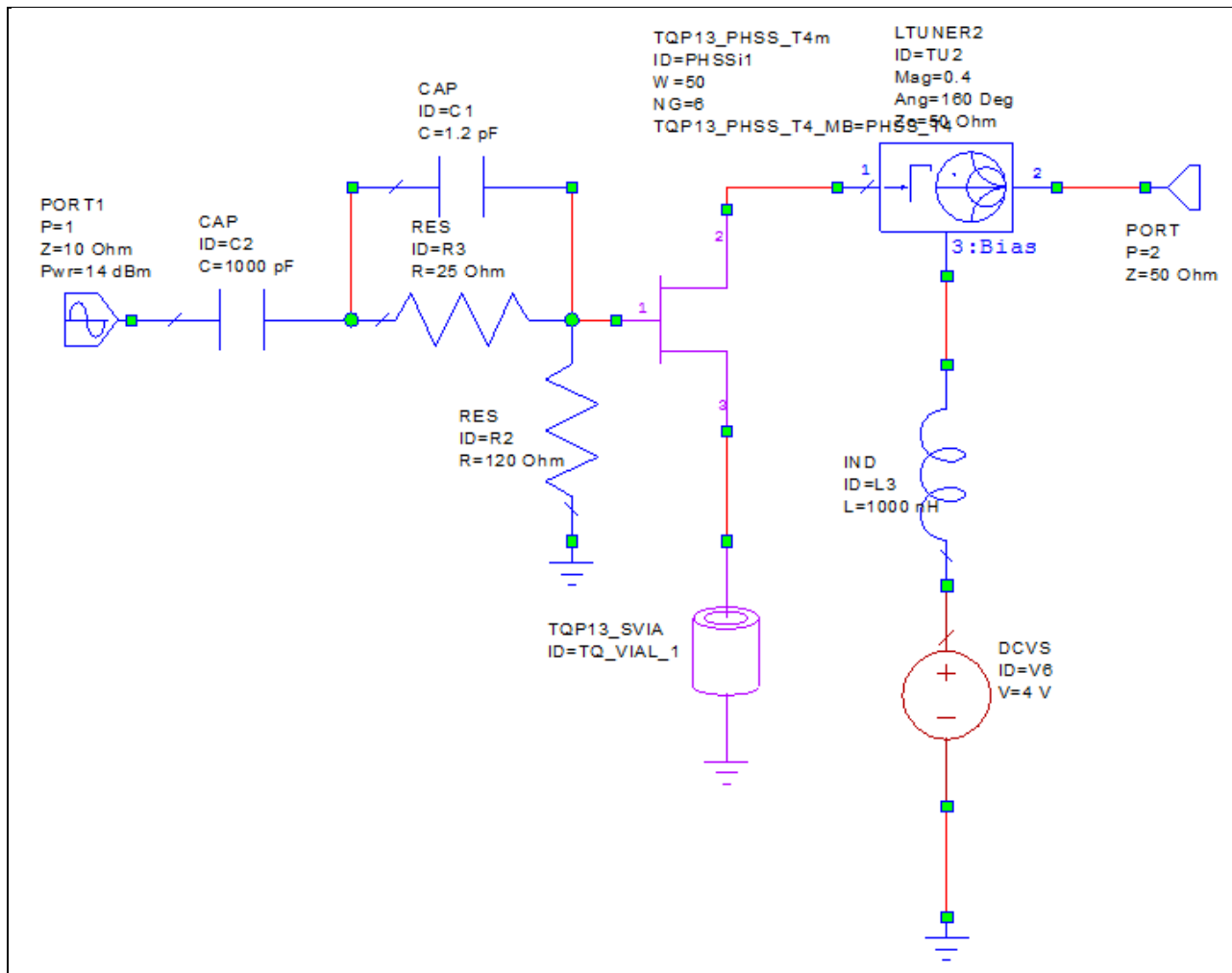
Figure 25. Schematic of the stabilized 6x50 µm PHEMT for a 28-GHz amplifier load-pull simulation.
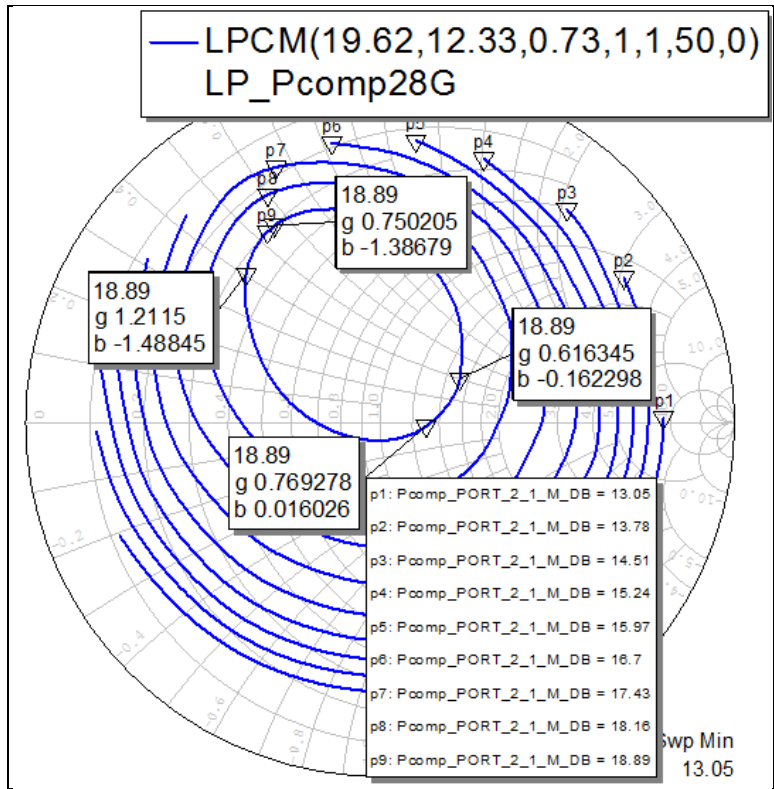
Figure 26. A 28-GHz load-pull simulation of output power (Pcomp-6x50 µm PHEMT).

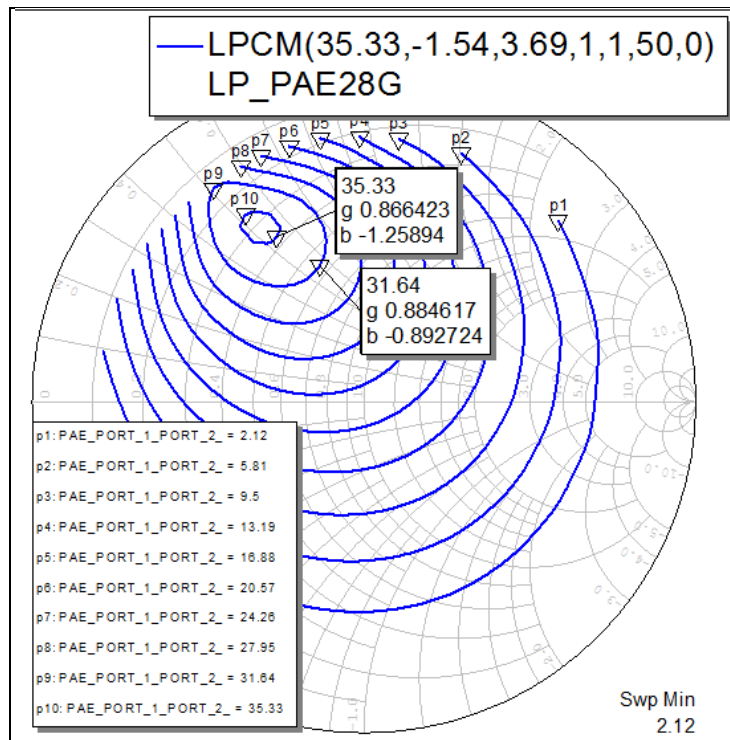

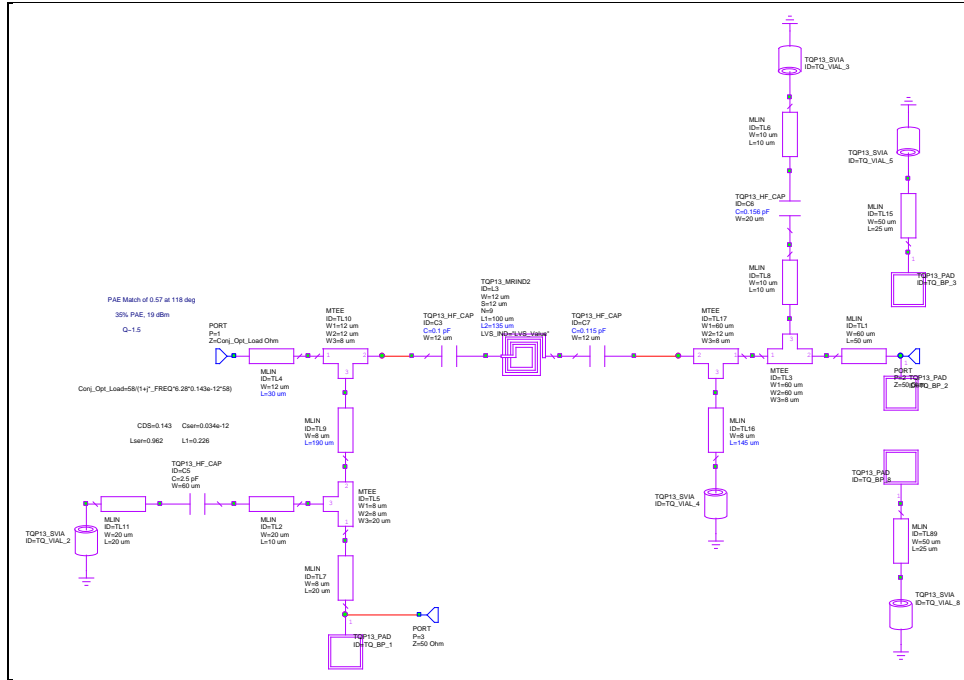Figure 27. A 28-GHz load-pull simulation of PAE (6x50 µm PHEMT).

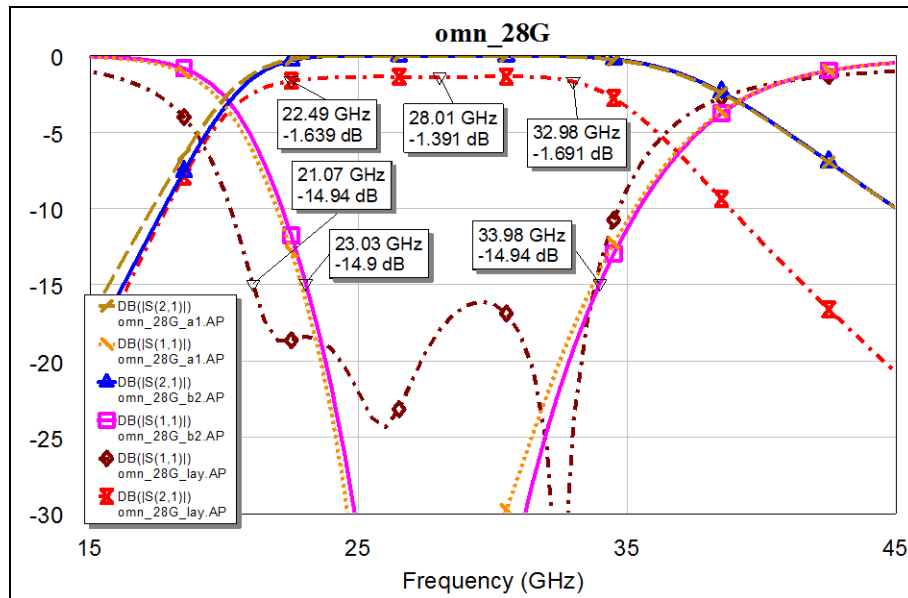Figure 28. A 28-GHz MMIC output match schematic.

Figure 29. A 28-GHz MMIC broadband output match simulation.

Sonnet EM simulations of the layout were performed and tended to indicate less bandwidth than the original MWO design. The actual performance was even narrower band than either simulation but was closer to the Sonnet simulation, as shown in figure 30. A final layout of the broadband 28-GHz amplifier is shown in figure 31. When the performance was re-simulated with lossy MMIC elements, the output power, gain and efficiency are much lower than the ideal case (figure 32). Performance measurements at 25.3 GHz are much closer to these re-

simulations. With such low gain, 6 dB or less, the PAE drops quickly as the power amplifier is compressed. The results indicate the difficulty and complexity of designing a broadband power amplifier at higher frequencies. As the "Q" of the device increases, the bandwidth reduces and it may also be difficult to achieve the desired impedance match with real lossy lumped elements compared to the ideal desired match.
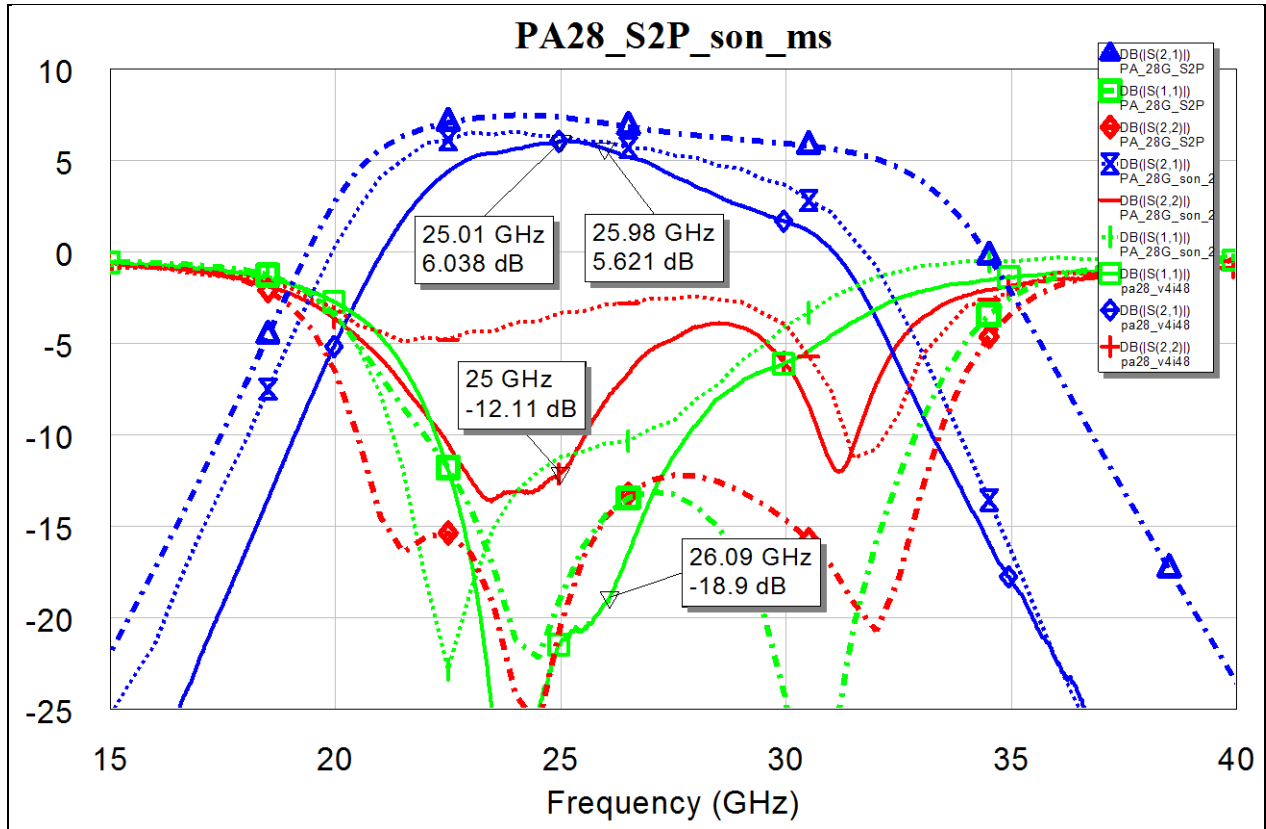

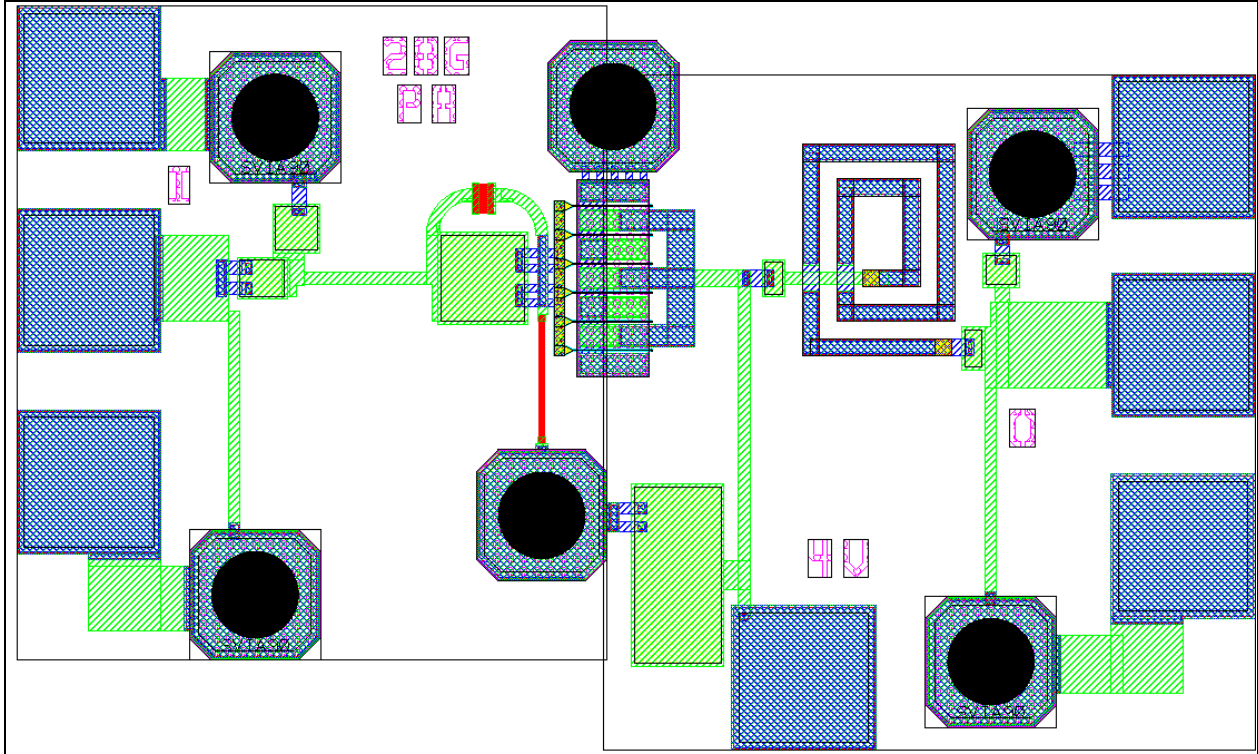Figure 30. 28 GHz broadband power amplifier—measured vs. simulation (MWO and Sonnet).

Figure 31. Layout plot of the 28-GHz broadband power amplifier (~0.9x0.5 mm).
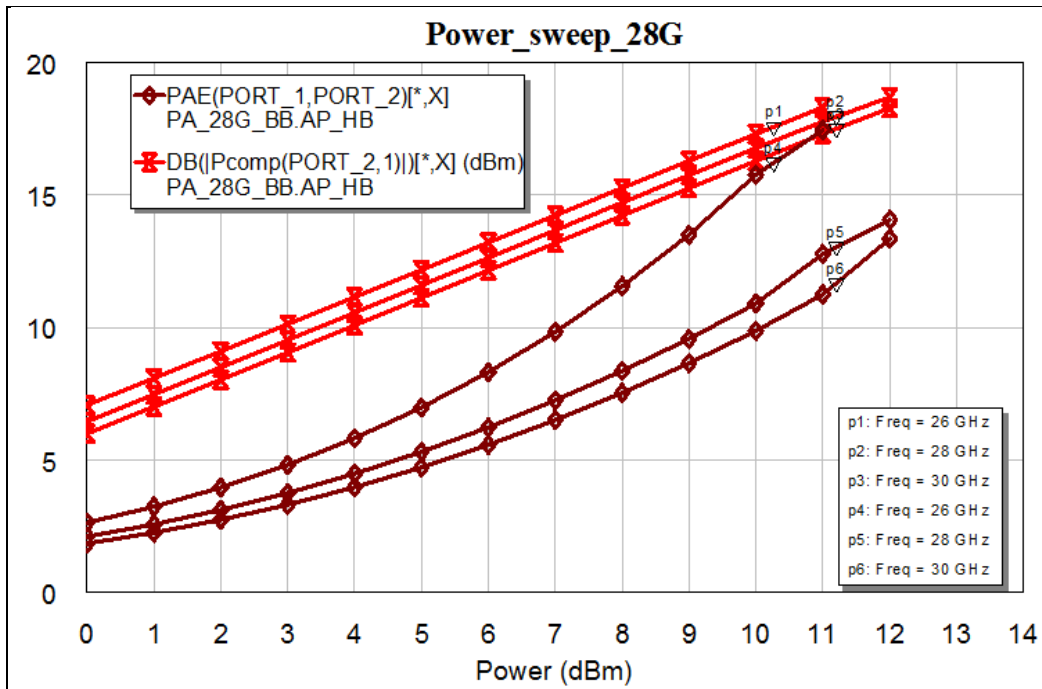

Figure 32. MMIC 28-GHz output power and PAE performance simulation (28, 30, and 32 GHz).
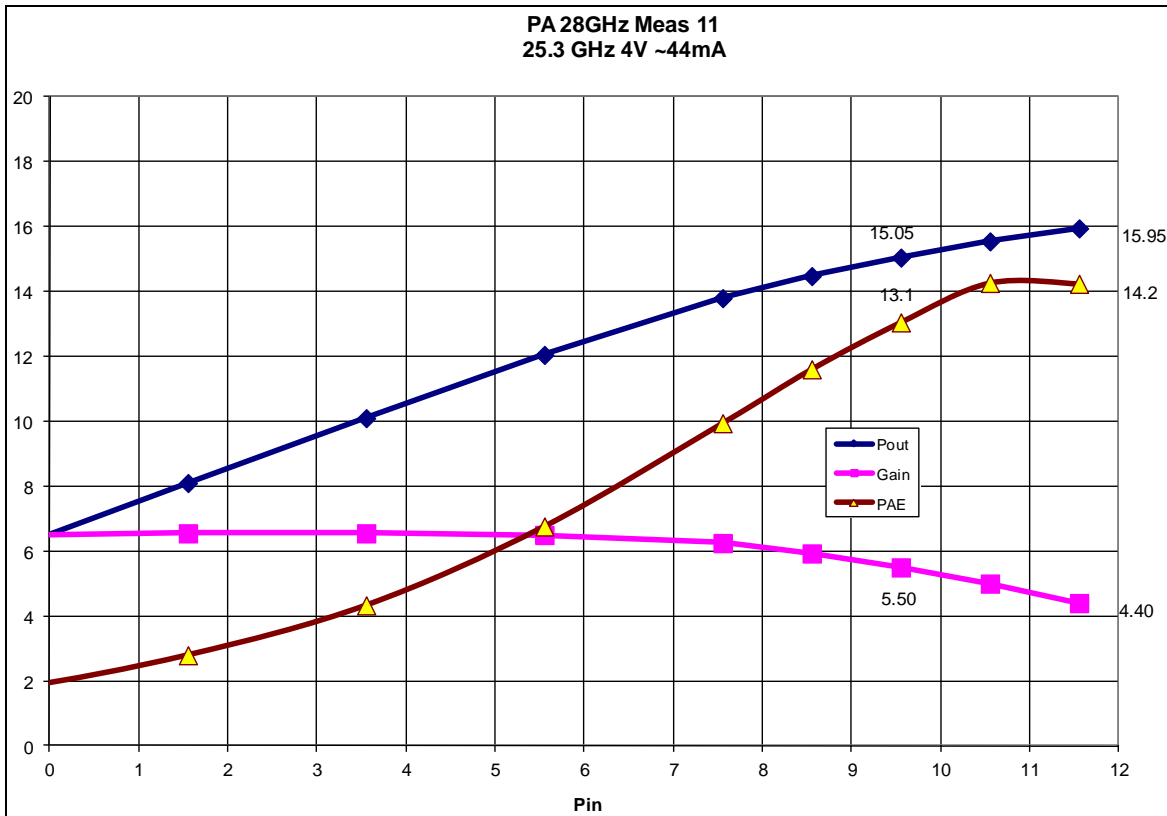
Figure 33. Power performance of the 28-GHz amplifier at 25.3 GHz (4 V).

9. Conclusion

These broadband medium power amplifier MMICs were designed using some of the techniques taught by Dale Dawson in the JHU Power MMIC Course. These are the first designs that I have performed, fabricated, and tested since helping Dr. Dawson teach the course in spring 2011. These filter and matching techniques could be applied to parallel combinations of transistors to increase power, but these simple one-transistor single-stage designs are a good start to prove out the concepts and validate with actual measurements. It should be noted that these broadband techniques were also used to successfully design two high power broadband MMIC amplifiers at 3–5 and 4–6 GHz using TriQuint's 0.25-µm gallium nitride (GaN) process (see ARL-TR-5987[1] and ARL-TR-6090[2]). These MMIC amplifiers illustrate the broadband design approach and the limitations that start with the device parasitic, the quality of the nonlinear and linear models available, and the quality of the MMIC fabrication process. They also illustrate the occasional necessity for an EM simulator, such as Sonnet, to accurately predict the actual layout parasitics, particularly at higher frequencies.

While the designs were part of a JHU course, the design techniques and Microwave MMICs would be of interest to Army and Department of Defense (DoD) communications systems, sensors, and wireless systems.

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