
# NAVAL POSTGRADUATE SCHOOL

**MONTEREY, CALIFORNIA**

# THESIS

**IMPROVED DATA ACQUISITION ARCHITECTURE FOR AN LLC CONVERTER**

by

Gilnam Oh

September 2014

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# REPORT DOCUMENTATION PAGE

*Form Approved OMB No. 0704–0188*



| **1. AGENCY USE ONLY** *(Leave blank)* | **2. REPORT DATE** September 2014 | **3. REPORT TYPE AND DATES COVERED** M.S. thesis |
|---|---|---|

**4. TITLE AND SUBTITLE**
IMPROVED DATA ACQUISITION ARCHITECTURE FOR AN LLC CONVERTER

**5. FUNDING NUMBERS**

**6. AUTHOR(S)** Gilnam Oh

**7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)**
Naval Postgraduate School
Monterey, CA 93943-5000

**8. PERFORMING ORGANIZATION REPORT NUMBER**

**9. SPONSORING /MONITORING AGENCY NAME(S) AND ADDRESS(ES)**
N/A

**10. SPONSORING/MONITORING AGENCY REPORT NUMBER**

**11. SUPPLEMENTARY NOTES** The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government. IRB protocol number ____N/A____.

**12a. DISTRIBUTION / AVAILABILITY STATEMENT**
Approved for public release; distribution is unlimited

**12b. DISTRIBUTION CODE**
A

**13. ABSTRACT (maximum 200 words)**

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| **14. SUBJECT TERMS** LLC Converter, A/D converter, V/f converter, voltage and temperature sensing, field programmable gate array, asynchronous | **15. NUMBER OF PAGES** 119 |
|---|---|
| | **16. PRICE CODE** |

| **17. SECURITY CLASSIFICATION OF REPORT** | **18. SECURITY CLASSIFICATION OF THIS PAGE** | **19. SECURITY CLASSIFICATION OF ABSTRACT** | **20. LIMITATION OF ABSTRACT** |
|---|---|---|---|
| Unclassified | Unclassified | Unclassified | UU |

NSN 7540–01-280-5500

Standard Form 298 (Rev. 2–89)
Prescribed by ANSI Std. 239–18

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# IMPROVED DATA ACQUISITION ARCHITECTURE FOR AN LLC CONVERTER

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Submitted in partial fulfillment of the
requirements for the degree of

**MASTER OF SCIENCE IN ELECTRICAL ENGINEERING**

from the

**NAVAL POSTGRADUATE SCHOOL**
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# ABSTRACT

The goal of this thesis is to replace a voltage-to-frequency (V/f) converter in the given inductor-inductor-capacitor (LLC) converter with an analog-to-digital (A/D) converter to prevent a field-programmable gate array (FPGA) from needing to monitor signals continuously. The proposed signal and sensor design alternative is to use A/D converters for the voltage and the battery temperature measurements, and to send only one gate signal that can be used to drive both MOSFETs in the LLC converter. Two candidates are considered for the A/D converter. The first solution is the AD7792/7793 A/D converter, which can monitor both the voltage and the temperature simultaneously. The AD7792/7793 transmits one data signal to the FPGA and receives three data signals from the FPGA. The second solution is the ADS1000, which uses the $I^2C$ protocol to communicate with the FPGA. The ADS1000 receives the read/write command and clock data from the FPGA and sends converted digital data to the FPGA. For efficient processing, we recommend the use of the ADS1000, since the FPGA and the A/D converter have bidirectional communication capabilities and the AD7792/7793 requires more optocouplers, more space, and more wires in the circuit.

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# LIST OF ACRONYMS AND ABBREVIATIONS

| | |
|---|---|
| A/D | Analog-to-Digital |
| ADC | Analog-to-Digital Converter |
| CLK | AD7792/7793 Clock |
| CS | AD7792/7793 Chip Slot |
| DIN | AD7792/7793 Data In |
| DOUT/RDY | AD7792/7793 Data Out/Ready |
| FPGA | Field-Programmable Gate Array |
| $I^2C$ | Inter-Integrated Circuit |
| LLC | Inductor Inductor Capacitor |
| MOSFET | Metal-Oxide Semiconductor Field-Effect Transistor |
| OPTO | Optical |
| PCB | Printed Circuit Board |
| PGA | Programmable Gain Amplifier |
| SCL | ADS1000 Serial Clock |
| SCLK | AD7792/7793 Serial Clock input |
| SDA | ADS1000 Serial Data |
| SLR | Series-Loaded Resonant |
| SRC | Series-Resonant Converter |
| USB | Universal Serial Bus |
| V/f | Voltage-to-frequency |
| ZVS | Zero-Voltage Switching |

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# EXECUTIVE SUMMARY

The inductor-inductor-capacitor (LLC) converter is popular for DC to DC power conversion. Presently, the LLC converter uses a voltage-to-frequency (V/f) converter to monitor the DC output battery voltage and the battery temperature. The V/f converter used in the laboratory is the LM231 [1]. The V/f converter creates a square-wave digital signal, where the frequency of the square-wave is proportional to the input DC voltage. The fact that the V/f converter digital signal is asynchronous presents a problem in the implementation, which is the problem this thesis addresses.

Since the output of the V/f converter is an asynchronous digital square-wave independent of all system clocks, it must be constantly monitored to find transitions so that the frequency can be measured. This process is very time consuming, and we propose to develop a field-programmable gate array (FPGA) implementation so that voltage and temperature can be measured in real-time. The given LLC converter is shown in Figure 1.

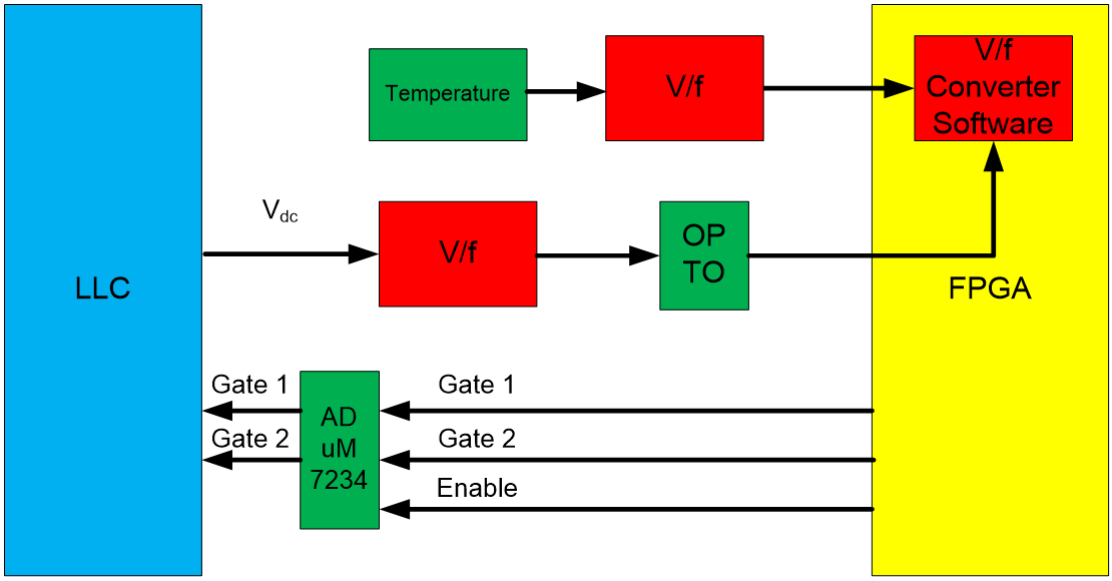


Figure 1. The existing LLC converter with V/f converters used for data acquisition.

The goal of this thesis is to replace V/f converters in the given circuit with an analog-to-digital (A/D) converter to prevent the FPGA from needing to monitor signals continuously. The circuit has two V/f converters to monitor both the voltage and the temperature. The proposed signal and sensor design alternative is to use A/D converters for the voltage and temperature measurements. The control signals are modified to send only one gate signal that can be used to drive both MOSFETs in the LLC converter.

Two solutions are proposed for the A/D converter. The first solution is based on the AD7792/7793 [2] A/D converter, which has the capability of monitoring both the voltage and the temperature simultaneously. In this way we need only one AD7792/7793, which transmits one converted digital data to the FPGA and receives three digital data from the FPGA. The AD7792/7793 application to the LLC is shown in Figure 2.

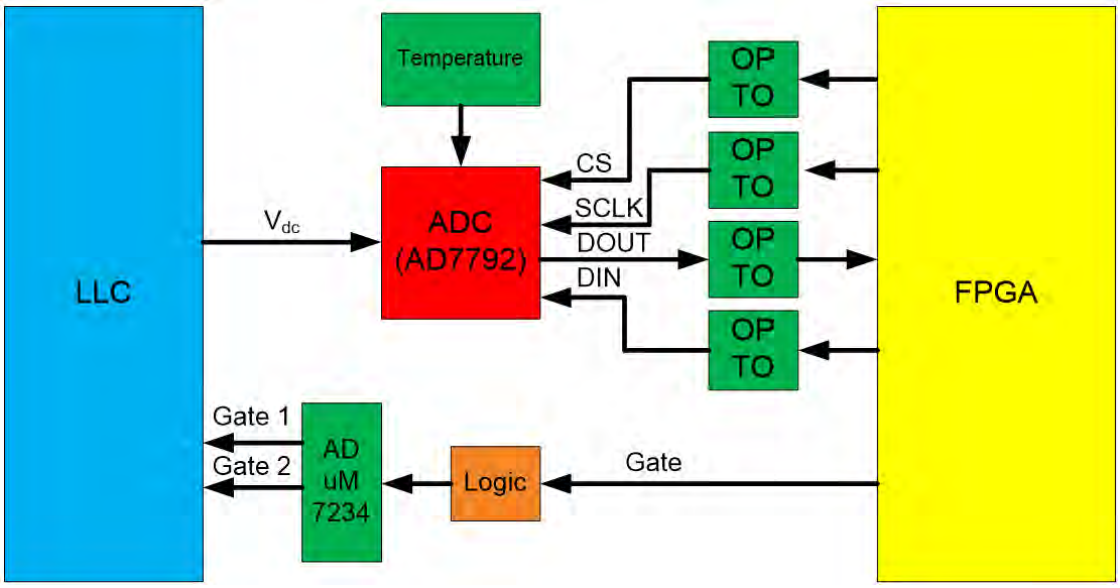


Figure 2. The proposed data acquisition architecture using the AD7792/7793 for the LLC converter.

The second solution is based on the ADS1000 [3], which communicates with the FPGA by an Inter-Integrated Circuit ($I^2C$) interface. The ADS1000 receives the read/write command and clock data from the FPGA and sends a converted digital data to the FPGA. The ADS1000 application to the LLC is shown in Figure 2.

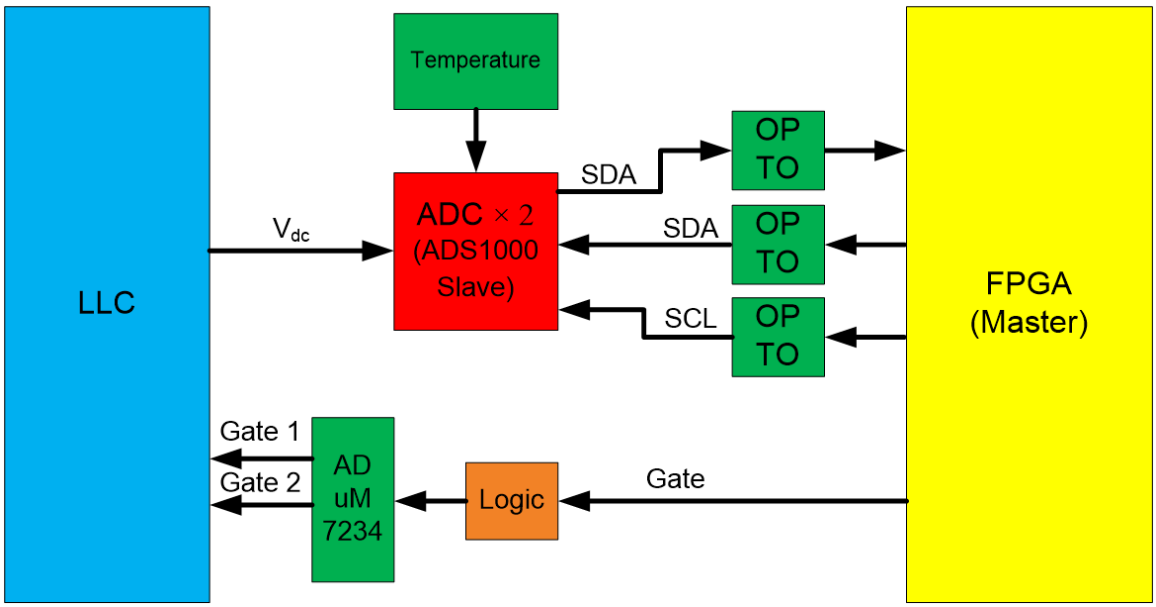


Figure 3. The proposed data acquisition architecture using the ADS1000 for the LLC converter.

The second solution has the advantage of being more efficient. For this reason, and based on our results, we recommend the use of the ADS1000 not only because the FPGA and the A/D converter have bidirectional communication capabilities but also in view of the fact that the AD7792/7793 requires more optocouplers and more space in the circuit.

**List of References**

[1] National Semiconductor. (1999, June). Precision voltage-to-frequency converters. [Online]. Available: http://eeclasses.usc.edu/ee459 /library/datasheets/LM331.pdf .

[2] Analog Devices Inc. (2004). 3-channel, low noise, low power, 16-/24-bit ∑-Δ ADC with on-chip in-Amp and reference. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/AD7792_7793.pdf.

[3] Burr-Brown Products from Texas Instruments Inc. (2004). Low-power, 12-bit analog-to-digital converter with $I^2C$ interface. [Online]. Available: http://www.ti.com/lit/ds/sbas357a/sbas357a.pdf.

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# ACKNOWLEDGMENTS

I would like to thank my family, Yunjung and Channy, for their efforts in supporting me and my school life.

I would also like to thank Dr. Julian for teaching and guiding me in the development of this thesis and giving me the opportunity to learn about the power converter and the analog-digital converter.

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# I. INTRODUCTION

## A. BACKGROUND

In the past twenty years power electronic converters have become widespread beyond the traditional industry applications such as motor drives. Since power converters have become the enabling technology for large markets such as consumer electronics, automotive and renewable energy sources, the need to increase their power density and reliability has grown together with the requirement of lower cost. Integration of control and sensing functions into the design of a power converter reduces cost and improves both reliability and performance. Microchip Inc. [1] is one of the many manufacturers that have made a significant effort to add these features to their products, which makes them more attractive to customers. An example is the integration of digital control techniques into the power system, which replaces the standard analog implementation. The advantage is that it provides efficient management of functions in the power system. An improved signal processing architecture to control an inductor-inductor-capacitor (LLC) power converter is displayed in Figure 1.

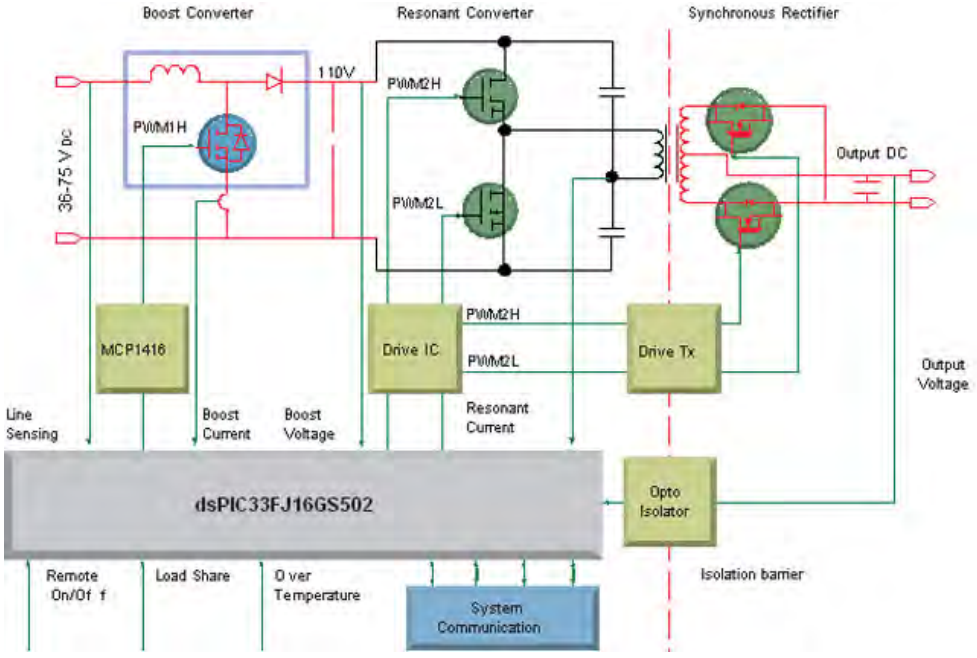


Figure 1. Improved signal processing architecture (from [1]).

According to its website [1], the Level 4 integration goals of Microchip are stated as follows: “for various power conversion and power control applications, they offer higher power density, lower system costs, improved reliability, and lower manufacturing and maintenance costs” [1].

It turns out that their microprocessor does achieve these goals; however, it has a number of redundant functions, not necessary in many applications. To build a circuit which performs a specific function, the integration of control and sensing functions should be part of the power converter’s design.

In this thesis, sensor integration is used to build specific functions for an LLC power converter used in a multi-cell battery charger as shown in Figure 2. The laboratory prototype shown in the photograph was implemented on a custom printed circuit board (PCB) using commercial-off-the-shelf components to minimize the cost of the design. The LLC converter was designed to trickle charge individual battery cells in a multi-cell battery string while monitoring each cell’s voltage and temperature. The goal is to equalize the battery charging level, which provides increased reliability and total stored charge for the battery pack.

The battery stack setup is shown in Figure 3. In this circuit, the LLC converter was used to charge each battery so that they are all charged to the same level, improving their reliability. The block diagram of the given LLC converter’s control circuit is shown in Figure 4.

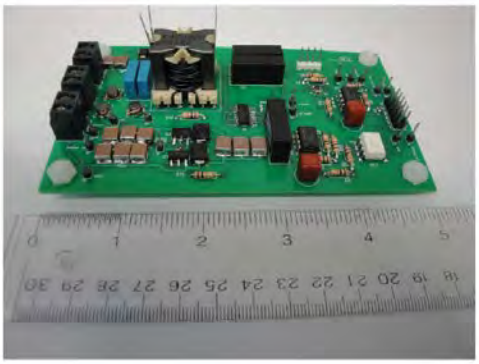

Figure 2. An LLC converter implemented on a custom PCB (from [2], [3]).

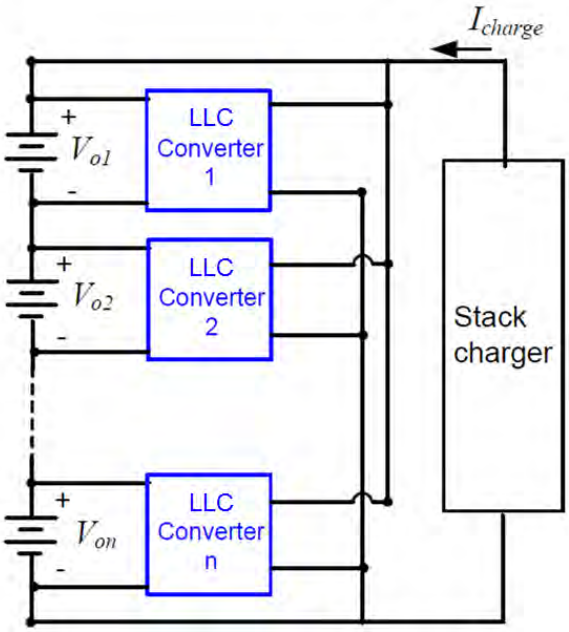


Figure 3. Multi-cell battery stack setup (from [2], [3]).

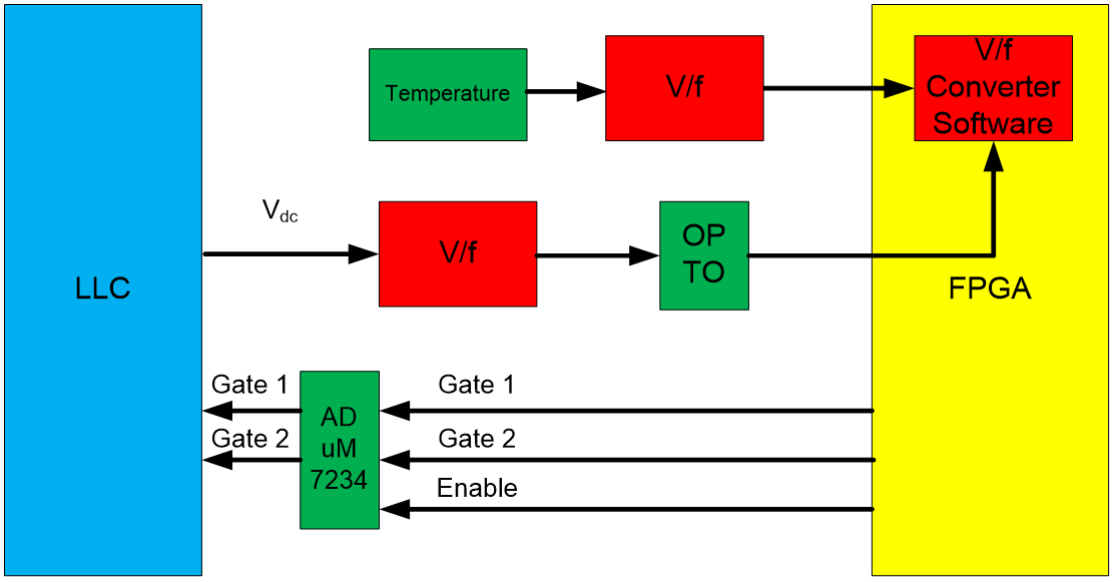


Figure 4. Block diagram of the existing LLC converter with V/f converters.

In the existing implementation, two voltage-to-frequency (V/f) converters (LM231 [4]) are used in the LLC converter to measure two analog signals because the V/f converter cannot receive two signals simultaneously. The V/f converters convert the DC output battery voltage and the battery temperature to digital signals and transmit them

to a field-programmable gate array (FPGA). The FPGA reads those digital signals from the V/f converters. In addition, the FPGA controls the operation of the whole circuit with three signals, which are Enable, Gate1, and Gate2 as shown in Figure 4.

The Half-Bridge Driver in Figure 4, (the ADuM7234 [5] chip), is for turning the Metal-oxide Semiconductor Field-effect Transistors (MOSFETs) on and off and provides the MOSFET with up to 4.0 A peak current and enough gate voltage to keep them fully on. The MOSFETs are the power devices in the LLC converter (blue box in Figure 4). Three signals are sent to the LLC converter: the enable signal and two gate drive signals. The enable signal makes the gate signals activate, and the gate signals are the voltage signals that drive the power switches (MOSFETs). The control signals sent by the FPGA are isolated from the LLC converter by the ADuM7234.

An optocoupler (OPTO in Figure 4) is used for feedback from the LLC converter to provide electrical isolation between the battery stack and the FPGA. The temperature sensor does not need an optocoupler since it has self-isolation because it is a plastic packaged sensor. Six LLC converters control the six cells in the battery stack as shown in Figure 5. Each has a twelve pin interface to the main control board, resulting in a large number of wires as can be noticed in Figure 5.

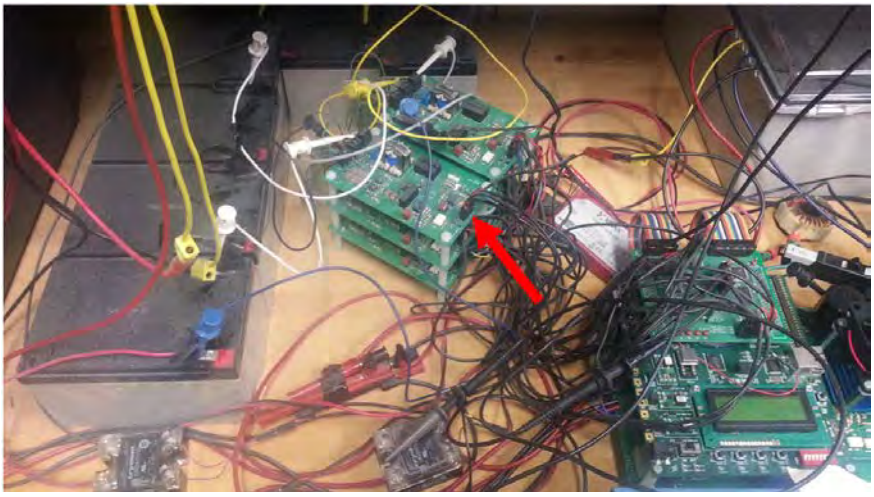

Figure 5. This photograph shows that many wires are needed to interface the six LLC converters (red arrow) to the FPGA controller.

In the conversion of voltage-to-frequency, the digital signal of the V/f converter is asynchronous and presents a problem in the implementation. Since the output of the V/f converter is an asynchronous digital square-wave independent of all system clocks, it must be constantly monitored to find digital signal transitions so that the frequency can be measured. This process is very time consuming, and alternative solutions are discussed. The sensor circuitry for the LLC converter, as currently implemented, is shown in Figure 6.

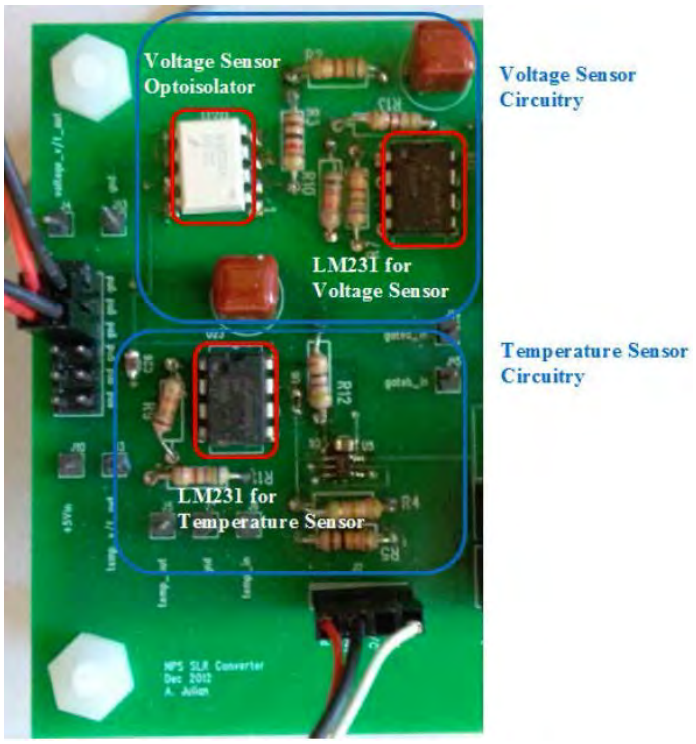


Figure 6. Sensor circuitry (from [6]).

The frequency is determined by properly sampling the voltage and temperature signals and is processed in the FPGA. The flow chart of the software which is used in the LLC power converter is shown in Figure 7. The frequency is computed by the edge detector which creates rising edge signals and makes the clock cycles decide the signal period. This period is the V/f signal period and is saved in the FPGA [6].

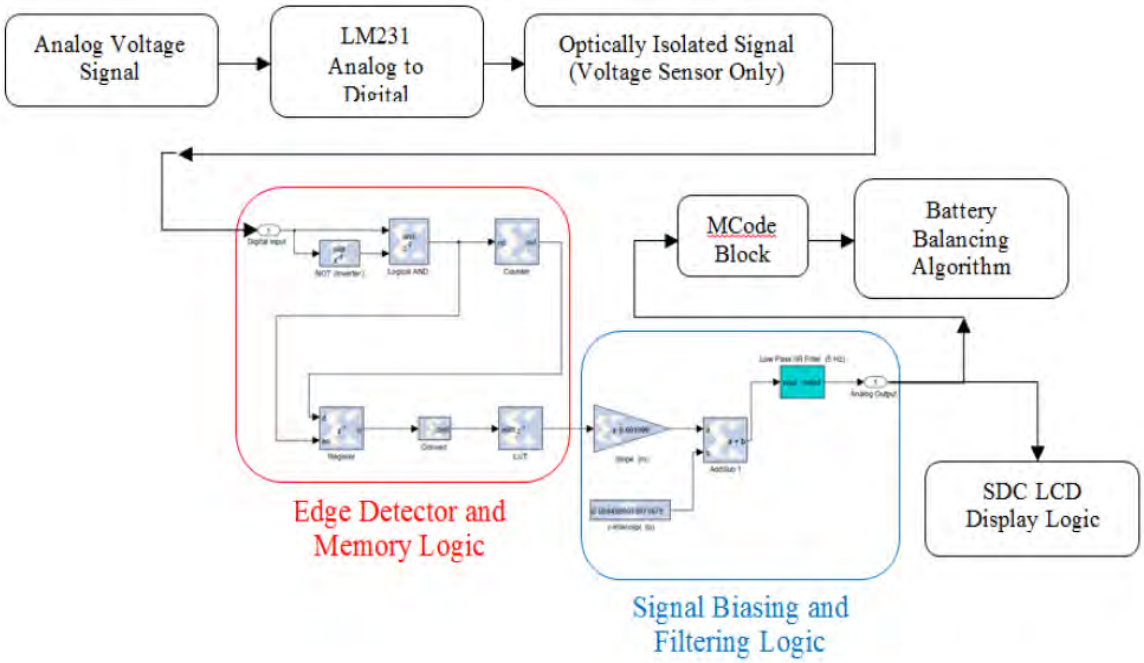


Figure 7. V/f converter software algorithm (from [6]).

## B. OBJECTIVES

The goal of this thesis is to replace the two V/f converters shown in Figure 4 with a two-channel analog-to-digital (A/D) converter in the given LLC power converter circuit. This can eliminate the need for the FPGA to monitor signals continuously, thus reducing its signal processing burden. This reduces the size and cost of the FPGA compared to the existing implementation. Two candidate A/D converter solutions are investigated in this thesis.

## C. APPROACH

By replacing the two V/f converters with an A/D converter, we can eliminate the need for the FPGA to monitor the signals continuously. The proposed signal and sensor design alternative is to use A/D converters for the voltage and the temperature measurements and to send only one gate signal that can be used to drive both MOSFETs in the LLC converter. When the gate signal is idle, the converter is disabled, which also eliminates the need for a separate enable signal.

This interface requires one control signal and one or three data signals for the A/D converter, depending on which A/D converter is chosen. One advantage is that the A/D can be queried by the FPGA anytime. In addition, A/D converters have multi-input channel capability; therefore, the given circuit needs only one A/D converter to measure both the voltage and the temperature. This is an improvement with respect to the existing V/f converters, which must be monitored continuously so that the frequency can be detected from the voltage transitions.

## D. THESIS ORGANIZATION

Chapter II includes the LLC topology to help explain the circuit operation, and a general A/D converter explanation to provide the basic concept of an A/D converter. Detailed explanations of two candidate A/D converters are included in Chapter III, in addition to the results and the experimental analysis of the A/D 7792/7793 converter. Conclusions and recommendations are presented in Chapter IV.

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# II. THE LLC TOPOLOGY AND A/D CONVERTER THEORY OF OPERATION

An LLC converter is a solid state switching power converter, which is generally used for "higher efficiency, higher power density, and higher component density" [7]. The LLC converter behaves like an ideal current source and reduces the stress and loss of the solid state switching devices because of its resonant operation [8].

Two continuous analog signals, the battery voltage and the temperature, need to be converted to digital signals to control the power converter. An A/D converter is a device for sampling and converting a continuous analog voltage to a discrete-time digital signal. The LLC topology is explained in section A to help understand the circuit operation. A general A/D converter explanation is given in section B to provide the basic concept of an A/D converter.

## A. LLC TOPOLOGY

The LLC power converter topology, which is shown in Figure 8, is used in a battery charger because it behaves like an ideal current source. The LLC converter also reduces the losses of the MOSFET power devices because it operates in a resonant mode so that the devices can be turned on and off when zero current is flowing in the devices. An LLC tank is made of two inductors and a capacitor on the primary side of the transformer, as shown in Figure 8. If it did not have the magnetization branch of the transformer $L_m$, it would be identical to a series-loaded resonant (SLR) converter [8].

The primary side of this circuit could be a half-bridge or a full bridge. A half-bridge is used presently and includes two MOSFET switches ($Q_1$ and $Q_2$) in a switching bridge to excite the LLC tank; a full bridge has four. The secondary side is a center tapped rectifier after a capacitive filter. The resonant components $L_r$, $C_r$, and $L_m$ are the passive elements in this circuit where $L_r$ is a resonant inductance, $L_m$ is the magnetizing inductance and $C_r$ is the resonant capacitor [8].

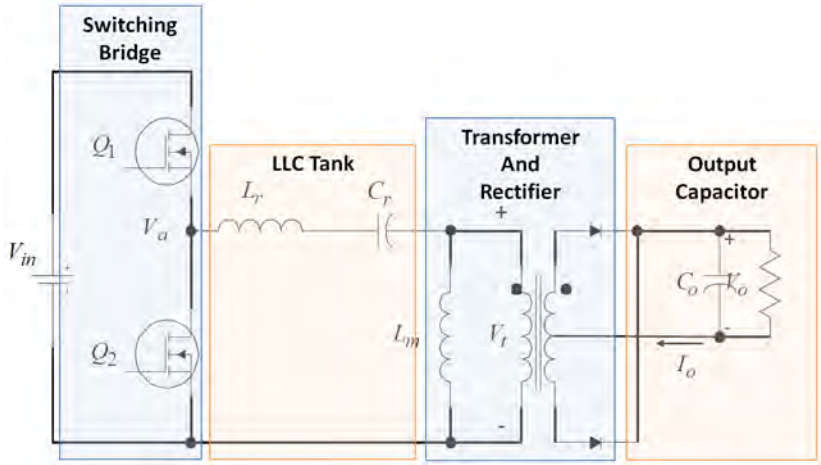


Figure 8. The LLC converter (after [8]).

This power converter works with various frequencies. It is very important to control the switching frequency in the power converter because its efficiency is related to the switching frequency.

In the circuit shown in Figure 8, "there are two resonant frequencies, one determined by $L_r$ and $C_r$, the other determined by $L_m$, $L_r$ and $C_r$" [8]. The two resonant frequencies can be calculated as [8]

$$f_1 = \frac{1}{2\pi\sqrt{LrCr}} \tag{1}$$

and

$$f_2 = \frac{1}{2\pi\sqrt{(Lr+Lm)Cr}} \ . \tag{2}$$

The simulated waveform of the LLC converter is shown in Figure 9. This power converter works at a switching frequency between the resonant frequencies defined in (1) and (2). The voltage $V_a$ is the voltage applied to the resonant converter (shown in Figure 9) using the DC source $V_{in}$ as shown in Figure 8. The variables $I\_L_r$ and $I\_L_m$ are the currents in the inductors $L_r$ and $L_m$ shown in Figure 8. The current $I_o$ is the output current on the secondary side of the transformer and $V_t$ is the transformer primary voltage. The whole operation can be analyzed by breaking it down into three different modes as explained in the next three subsections [8].

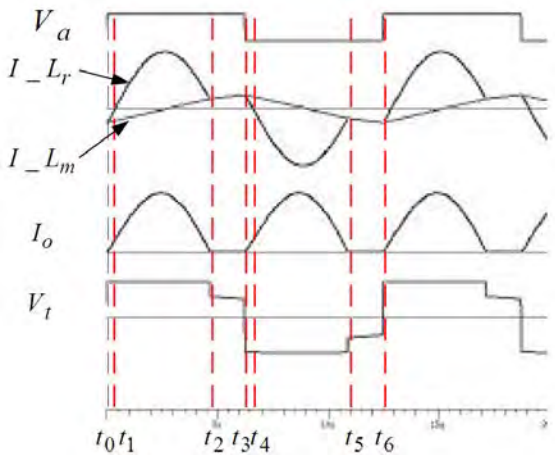


Figure 9. Simulated waveform of the LLC converter (from [8]).

### 1. Mode 1 ($t_0$ to $t_1$)

This mode initiates at $t_0$. At this moment, the switch $Q_2$ is turned off, and the $I\_L_r$ flows to the left in Figure 10, which is a negative current in Figure 9. This negative $I\_L_r$ flows to the body diode of $Q_1$, which provides a zero-voltage switching (ZVS) condition for $Q_1$. When the $I\_L_r$ flows through the body diode of $Q_1$, the $I\_L_r$ increases and makes the secondary diode $D_1$ conduct and $I_o$ increases, as shown in Figures 9 and 10. At this moment, the transformer sees the output voltage, which is the voltage across $C_o$, the output capacitor of the secondary side, as shown in Figure 8. The inductor $L_m$ is driven with a constant voltage source during this mode [8].

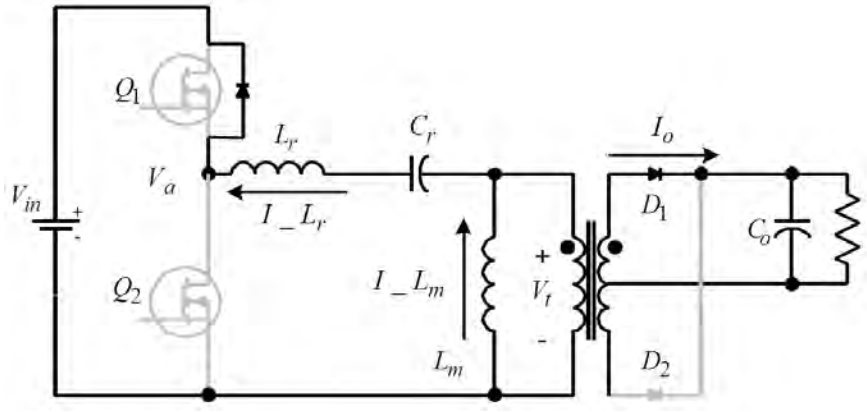


Figure 10. The LLC converter operation mode 1 (from [8]).

### 2. Mode 2 ($t_1$ to $t_2$)

The resonant current $I\_L_r$ flows to the right as shown in Figure 11 during this mode of operation. The current is positive in $L_r$, as shown in Figure 9, after $t_1$ and before $t_2$. This is the beginning of mode 2. The current $I\_L_r$ flows through the MOSFET $Q_1$ body diode during mode 1. The current becomes positive and then decreases in the MOSFET during mode 2. During mode 2, the output rectifier diode $D_1$ conducts, and the transformer secondary voltage is fixed at the output voltage $V_o$. The magnetizing inductor $L_m$ is linearly charged by the output voltage, so it does not participate in the resonant action during this period. In mode 2, the circuit works like a series-resonant converter (SRC) with $L_r$ and $C_r$ as the resonant components at the frequency in (1). This mode ends when the $I\_L_r$ is the same as $I\_L_m$. The output current $I_o$ reaches zero at the end of this mode [8].

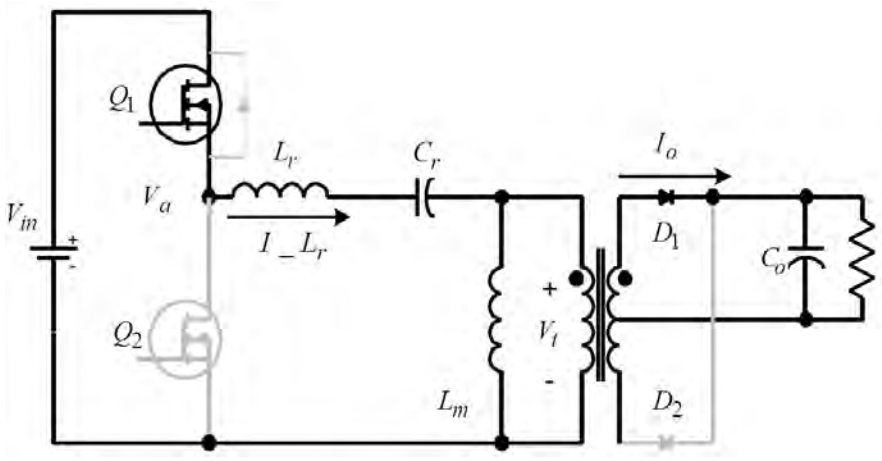


Figure 11. The LLC converter in operation mode 2 (from [8]).

### 3. Mode 3 ($t_2$ to $t_3$)

The circuit operation in mode 3 is shown in Figure 12. The resonant current $I\_L_r$ is the same as the $I\_L_m$ and $I_o$ reaches zero at $t_2$, as shown in Figure 9. Both the output rectifier diodes $D_1$ and $D_2$ of the secondary circuit are reverse biased, and the

transformer's secondary voltage is lower than the $V_o$, as shown in Figure 9. In this mode, the output is decoupled from the transformer. Thus, the output is not connected to the primary, and $L_m$ participates in the resonant oscillations as defined in (2). The magnetizing inductance $L_m$ forms a resonant tank in series with $L_r$ and $C_r$. This mode ends when $Q_1$ is turned off. As can be seen from the waveform in Figure 9, $Q_1$ turns off its current at $t_3$; this current is small compared with the peak current, which reduces the switching losses [8]. The next half cycle of operation is the same as analyzed above where modes 1 through 3 repeat [8].

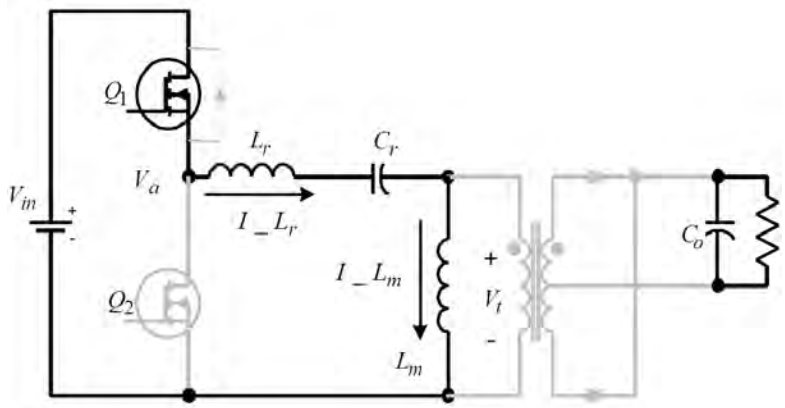


Figure 12. The LLC converter in operation mode 3 (from [8]).

## B. A/D CONVERTER DESCRIPTION

An A/D converter is a device for sampling and converting a continuous analog voltage to a discrete time digital signal. At each sample, the relation between the analog voltage $V_{in}$ and its numerical representation is given by [9]

$$\gamma\ (\mathrm{V}) = 2^n \cdot G \cdot \frac{V_{in+} - V_{in-}}{V_{ref+} - V_{ref-}} = 2^n \cdot G \cdot \frac{V_{in}}{V_{ref}} \tag{3}$$

where $\gamma$ is the digital code of output in volts (V), $n$ is the number of output bits, $G$ is the gain factor, $V_{ref}$ is the reference voltage and $V_{in}$ is the input signal to the A/D converter. Figure 13 is a block diagram of a typical A/D converter circuit.

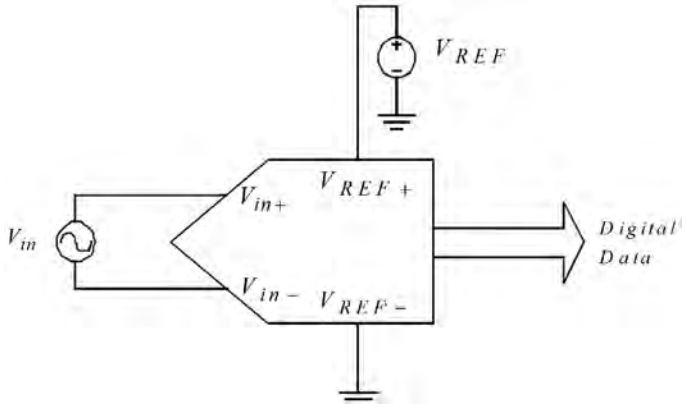


Figure 13. A typical A/D converter block diagram (from [9]).

Two pins are used for $V_{in+}$ and $V_{in-}$ signal inputs, and the A/D converter reference voltage is provided with internal or external power. The accuracy of the converted value is determined by the reference voltage, which should be constant and not sensitive to temperature changes. The ideal transfer function of a 3-bit A/D converter is displayed in Figure 14. In this example, the A/D converter uses eight different digital output codes to represent the analog input voltage. The largest number from the A/D converter is $(N-1)/N$, where $N$ is the number of digital output codes. In the case of the 3-bit A/D converter, the largest number is 7/8, since the number of bits is three [9]. The smallest value represented by the output is zero.

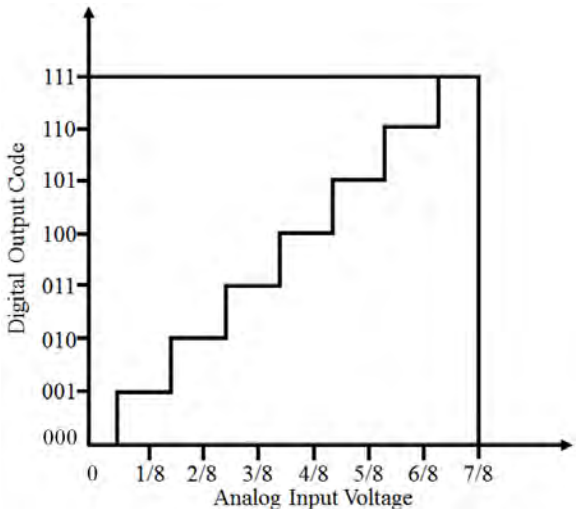


Figure 14. Transfer function of a general 3-bit A/D converter (after [9]).

Many factors affect the capability of an A/D converter and are described in reference [9]. In this thesis, two A/D converters are studied as possible solutions to replace the V/f converters for this data acquisition problem. Both A/D converters have similar functions, however, they have different interfaces and different communication protocols. Characteristics of the two candidate A/D converters and some measured test data are presented in the next chapter to find a viable solution for our data acquisition architecture.

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# III. A/D CONVERTERS FOR IMPROVED DATA ACQUISITION

The data acquisition system is required to measure two voltages, the battery voltage and the temperature sensor voltage, and report this data to the FPGA. Two possible solutions for data acquisition are explained in this chapter.

## A. AD7792/7793 A/D CONVERTER DESCRIPTION

The first proposed solution is based on the AD7792/7793 A/D converter that has "low power, low noise, and complete analog front-ends for high precision measurement applications" [10]. This chip contains a "16/24 bit ∑-Δ analog-to-digital (ADC), a low noise instrumentation amplifier, an internal clock, and a low noise, low drift internal band gap reference" [10]. This chip can work with an external clock. The functional block diagram of the AD7792/7793 is shown in Figure 15 [10].

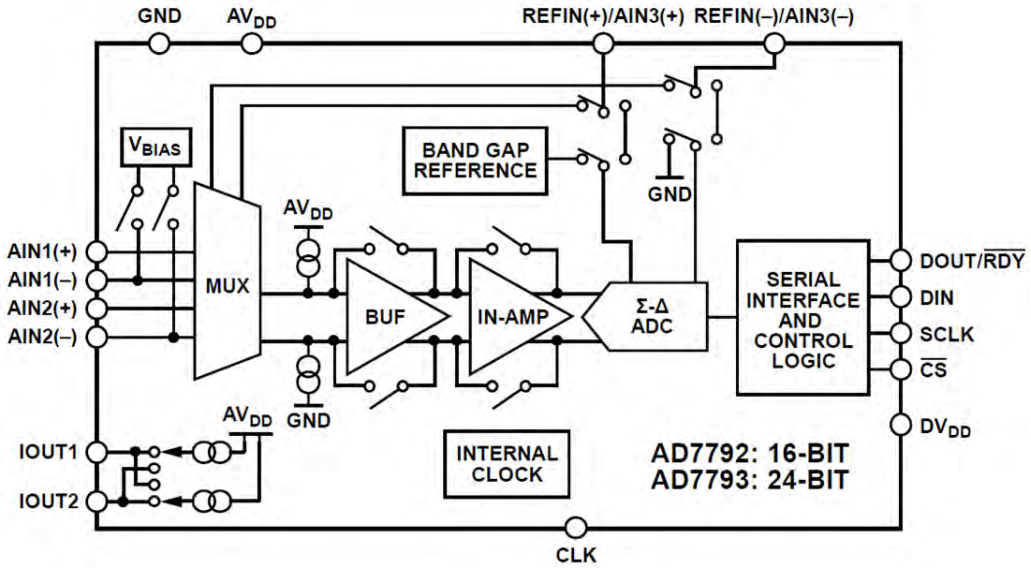


Figure 15. The AD7792/7793 functional block diagram (from [10]).

### 1. The AD7792/7793 Theory of Operation

The AD7792/7793 has the capability of measuring three channel inputs simultaneously, including ± analog input 1, ± analog input 2, and ± reference input (or ±

analog input 3). The serial clock (SCLK) is the serial clock input that is the clock signal for the data transfer to and from the ADC. The serial clock has a Schmitt triggered input that provides a suitable interface with the OPTO isolation. The clock signal (CLK), shown in Figure 16, is the clock in/out trigger that drives the ADC from a common clock and achieves simultaneous conversions. The signal CS is the chip select input for the interface that activates the ADC and can be used to select the SCLK, data input (DIN), and data output (DOUT). The internal output 1 (IOUT1) and IOUT2 are the outputs of the internal excitation current source and are not used for this application. The $AV_{DD}$ is the supply voltage from 2.7 V to 5.25 V. The $DV_{DD}$ is the digital interface supply voltage and is used by the serial interface pins. The $DV_{DD}$ is independent of the $AV_{DD}$ [10].

The data out and ready (DOUT/RDY) pin shown in Figure 16 is the serial data output and data ready output, which functions not only as the serial data output pin to access the ADC output but also as the data ready pin to report conversion completion. For example, the pin stays high if the data is not read after the conversion, which indicates that data is ready to be read. The DIN is the serial data input and controls the register selection bits to identify proper register settings. The pin configuration of the AD7792/7793 is shown in Figure 16 [10].

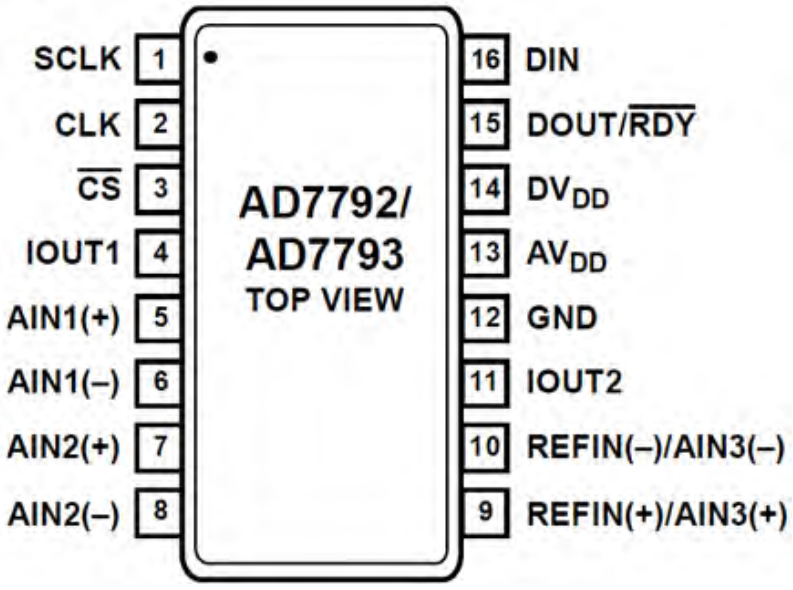


Figure 16. The AD7792/7793 converter pin configuration (from [10]).

## 2. Experimental Observations

In this thesis, a demonstration board was used to evaluate the AD7792/7793 converter operation. The demonstration board used, the EVAL-AD7792, is powered by a 5 V power supply through a USB connection from a computer. This USB connection facilitates the communication between the computer and the board. The AD7792/7793 demonstration board is shown in Figure 17. Analog input signals from a signal generator were connected to the right side of the pin pairs that are marked AIN1(+) and AIN1(-), as displayed in Figure 18. The left side of the pin pairs is ground. The output signals (DIN, DOUT/RDY, CS, and SCLK) were connected to an oscilloscope to monitor the signals, as displayed in Figure 19 [11].

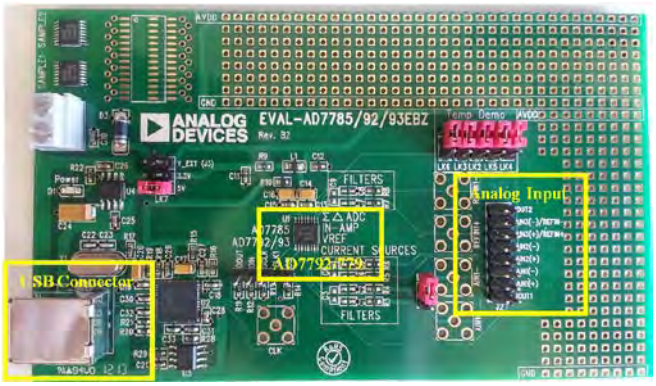


Figure 17. The AD7792/7793 demonstration board.

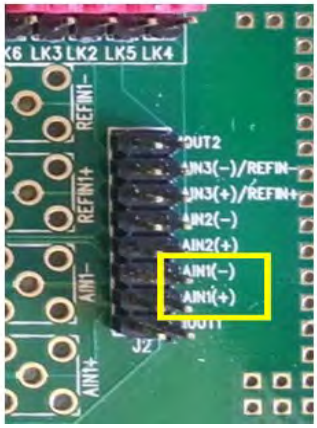


Figure 18. The AD7792/7793 demonstration board analog input pin connection.

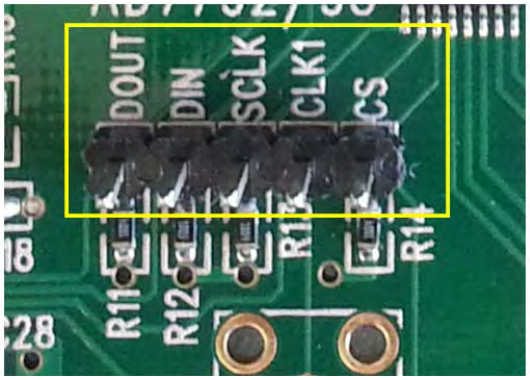


Figure 19. The AD7792/7793 demonstration board digital output pin connection.

The AD7792/7793 emulation software tool graphical user interface is shown in Figure 20. Using this software tool, we can measure the input signals with various update rates, gains, and number of samples. Internal and external clock settings can be used [11]. The software tool displays a converted signal with the voltage plotted versus the samples, which can be easily converted to the time-domain because the sample rate is known.

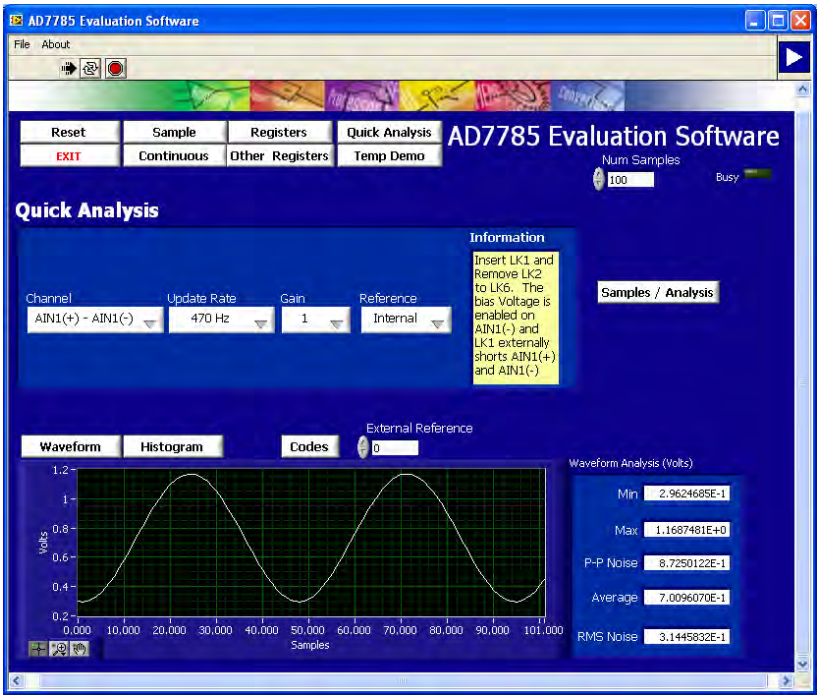


Figure 20. The AD7792/7793 converter emulation software tool graphical user interface.

To operate the demonstration board, an input channel must be selected using the software tool. Although the AD7792/7793 has a simultaneous measurement capability of all three inputs, the demonstration board cannot monitor all three signals simultaneously, so it must measure them one-by-one; thus, the multi-input measurement is not shown and is not required for this application.

### 3. Analysis of the Experimentation Results

The measured waveform picture that was exported from the software tool is shown in Figure 21. The AD7792/7793 accepts bipolar signals or unipolar signals; since the target application is a unipolar signal the results shown here are unipolar [10]. The input signal is DC with a superimposed AC oscillation as expected for this application.

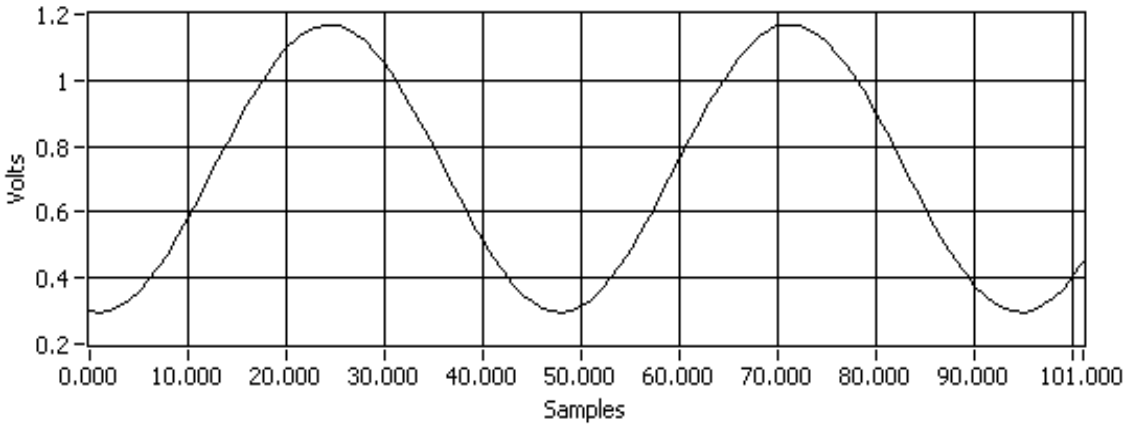


Figure 21. The exported waveform from the software tool.

The *y*-axis indicates the voltage of the input signal, and the *x*-axis is the sample number. Neither the *y*-axis nor the *x*-axis can be modified in the software tool, but the user can see the binary-coded numbers in the software tool when this setting is selected. The offset binary output of the A/D converter goes from 00000000 for a negative full-scale input to 11111111 for a positive full-scale input, and zero volts is represented by 10000000 [10]. An applied signal from a signal generator is 10 Hz with 0.56 $V_{pp}$ added to 0.746 $V_{dc}$ offset. The input signal waveform which appears on the oscilloscope is shown in Figure 22. The mean value, the peak-to-peak voltage and the frequency of the waveform were measured by the oscilloscope, and the measurements appear in Figure 22.

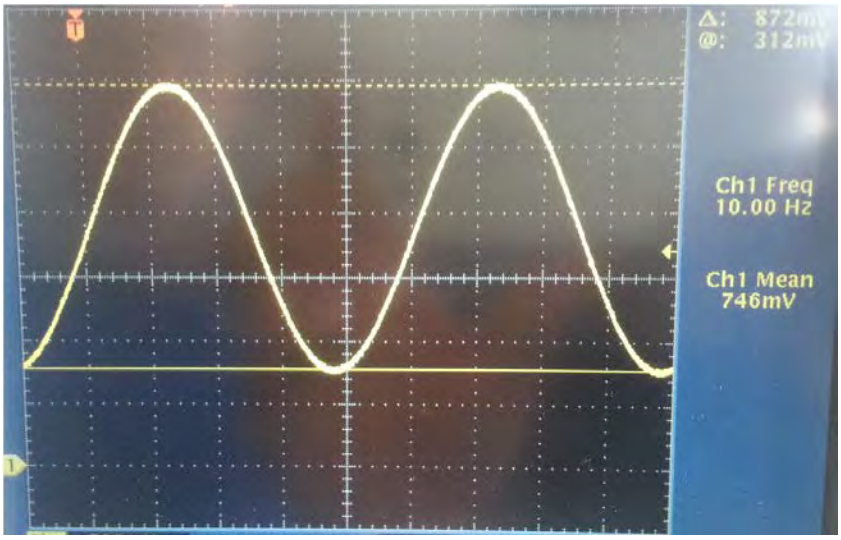


Figure 22. The input signal measured on an oscilloscope.

For the example shown here the sample rate is 470 Hz and the gain is one, which is set by the software tool. It should be noted that the sample rate of the A/D converter is referred to as the "update rate" in Figure 20. One hundred samples are recorded by the computer. In this example, the software tool displays two cycles of the signal with 100 samples. Since the frequency is 10 Hz and the period is 100 ms, the duration of two cycles is 200 ms. The exported data is plotted by Matlab to generate a graph with time on the *x*-axis as shown in Figure 23.

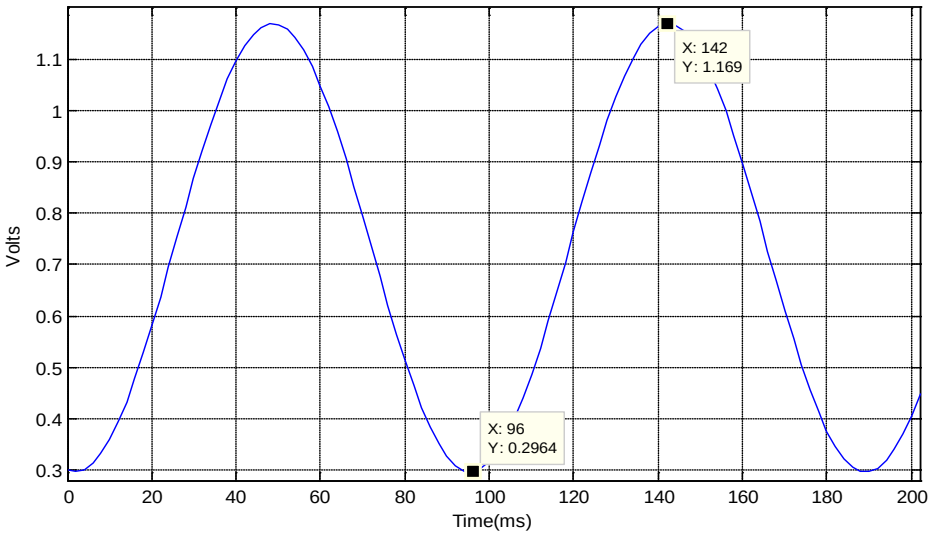


Figure 23. Matlab graph from exported data.

The next analysis shows the behavior of the A/D converter when the input signal exceeds the allowable voltage constraints. The results also show that the A/D converter can process bipolar inputs even though the A/D converter is powered by a unipolar supply voltage. The bipolar input capability demonstration is not needed for this application.

The maximum output of this demonstration board is constrained to +/- 1.17 V by the internal reference voltage; thus, in this example, the input signal is over 1.17 V, and the output data is saturated at +/- 1.17 V (Figures 24 and 25). To show this saturation, a signal at 10 Hz and 2.8 $V_{pp}$ with no offset voltage was used. The input signal waveform is a bipolar signal feeding the A/D converter even though a unipolar power supply of 5 $V_{dc}$ was used for the A/D converter. The bipolar input is allowed because the AIN- is biased by an internal supply of 1.17 $V_{dc}$. For an external reference, the maximum output data can be up to +/- 2.5 V; however, an experiment with an external reference was not executed.

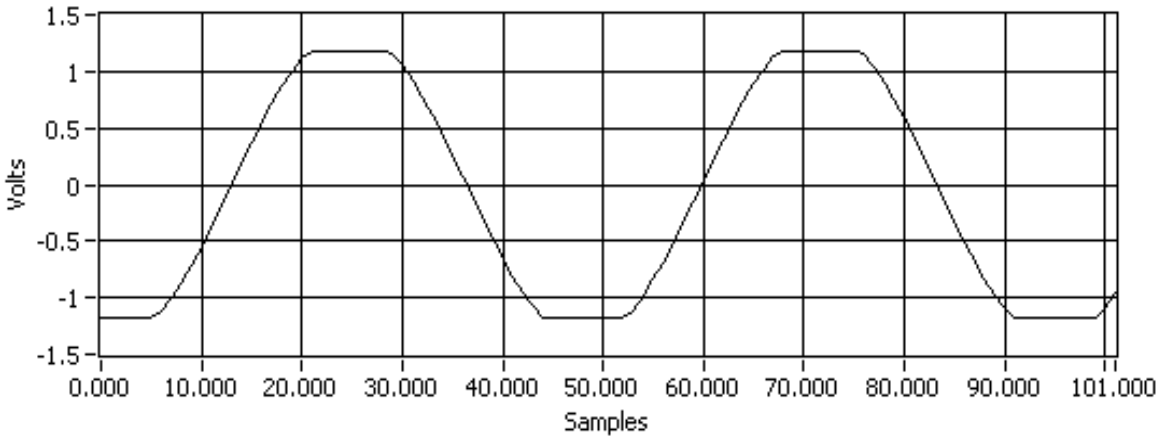


Figure 24. Example of saturation of 10 Hz, 2.8 $V_{pp}$ input signal.

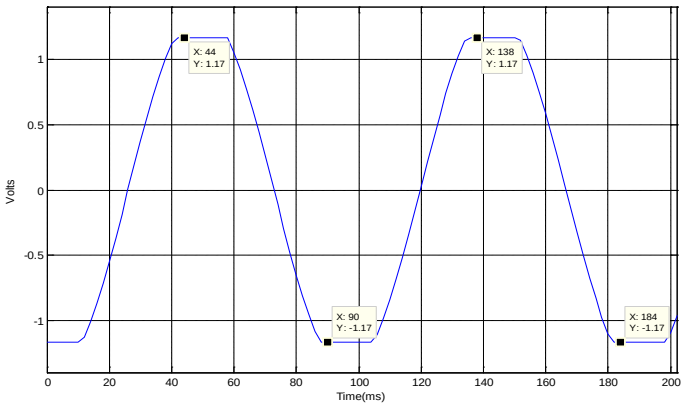


Figure 25. Matlab graph of 10 Hz, 2.8 $V_{pp}$ output data with no DC offset.

The AD7792/7793 has both a single and continuous conversion mode; however, only the continuous conversion mode, which is appropriate to accommodate the continuous sampling requirement of the LLC converter, was used. There are four signals that must be checked with the AD7792/7793 converter: CS, DIN, DOUT/RDY, and SCLK. The CS chooses the device, SCLK determines the serial clock input for the device and controls each data transfer. The DIN is used for the data transfer to the on-chip registers, and the DOUT/RDY provides an access to the on-chip registers containing the converted signal data. These four output signals from experimental measurements are shown in Figure 26.


Figure 26. Digital output signals (CH1:DIN, CH2: DOUT, CH3: CLK, CH4:CS).

An example of the expected waveforms is shown in Figure 27, which was taken from the AD7792/7793 datasheet. Similar signal patterns are displayed in Figures 26 and 27.

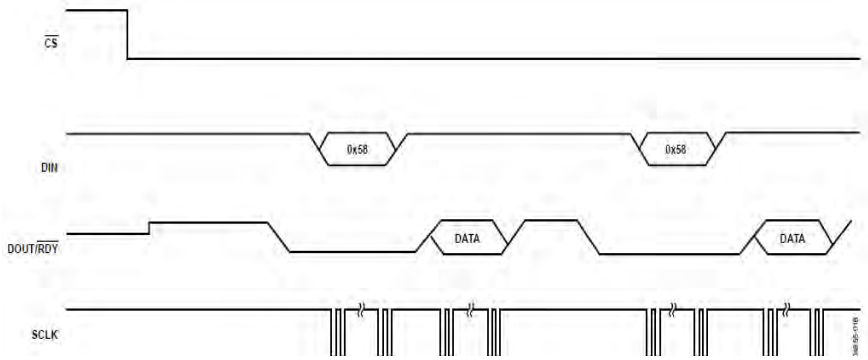


Figure 27. Output signals from the datasheet (from [10]).

In Figure 26, the green line that displays the CS goes low, and the yellow line that displays the DIN has two signal pulses. The data DIN is compared with the purple line (the SCLK) that presents the binary numbers. The data DIN is valid on the rising edges of SCLK. In Figure 28, which zooms in on the DIN signal, the yellow line represents 01011000 [10]. This number represents 58 hex, which is shown in Figure 27 for the DIN signal. From the AD7792/7793 datasheet, this means that the A/D converter is exiting the continuous read mode of operation.

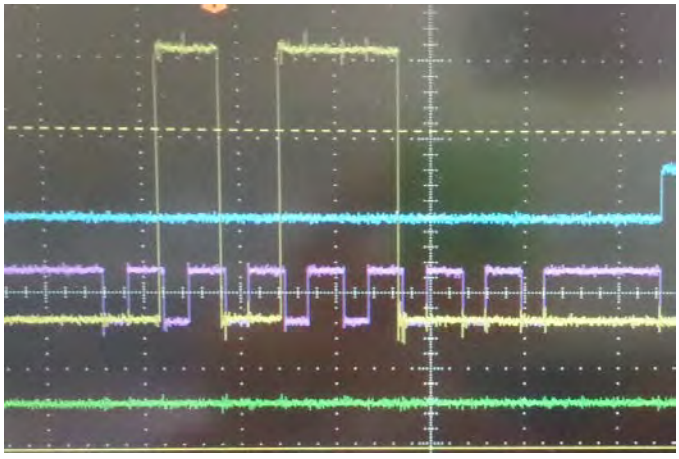

Figure 28. DIN exiting the continuous read command (the yellow line) (CH1:DIN (01011000), CH2: DOUT, CH3: CLK, CH4:CS).

The output data activity on the DOUT/RDY signal is shown in Figure 29. When the DIN line goes low, the DOUT/RDY signal, which is displayed as the blue line in Figure 29, transmits the data. The activity on the DOUT/RDY signal in Figure 29 shows the data representing one sample event. The oscilloscope was AC coupled in Figure 29 for channel 1 so it does not display zero volts for channel 1.

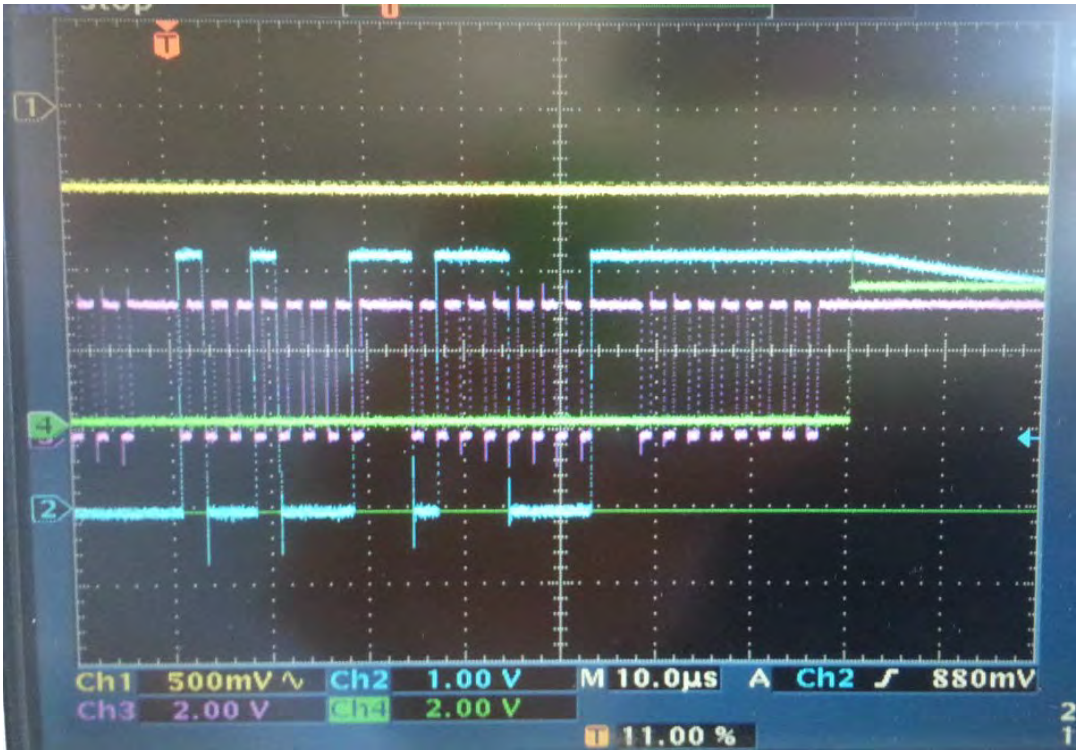


Figure 29. DOUT(the blue line) transmitting data (CH1:DIN, CH2: DOUT, CH3: CLK, CH4:CS).

In this experimental result, the update rate was set to 470 Hz with the software tool, as previously shown in Figure 19. Using the software tool, the update rate was selected from the range 4.17 to 470. It is seen in Figure 30 that the period of data activity is 2.13 ms, which is 1/470. The two vertical lines in Figure 30 show the period of the data activity on the communication lines, and the distance between the markers for the two lines are 2.13 ms. It is shown in Figure 30 that the data is transmitted at 470 Hz by the activity of the DOUT/RDY, which is channel 2 in Figure 30.

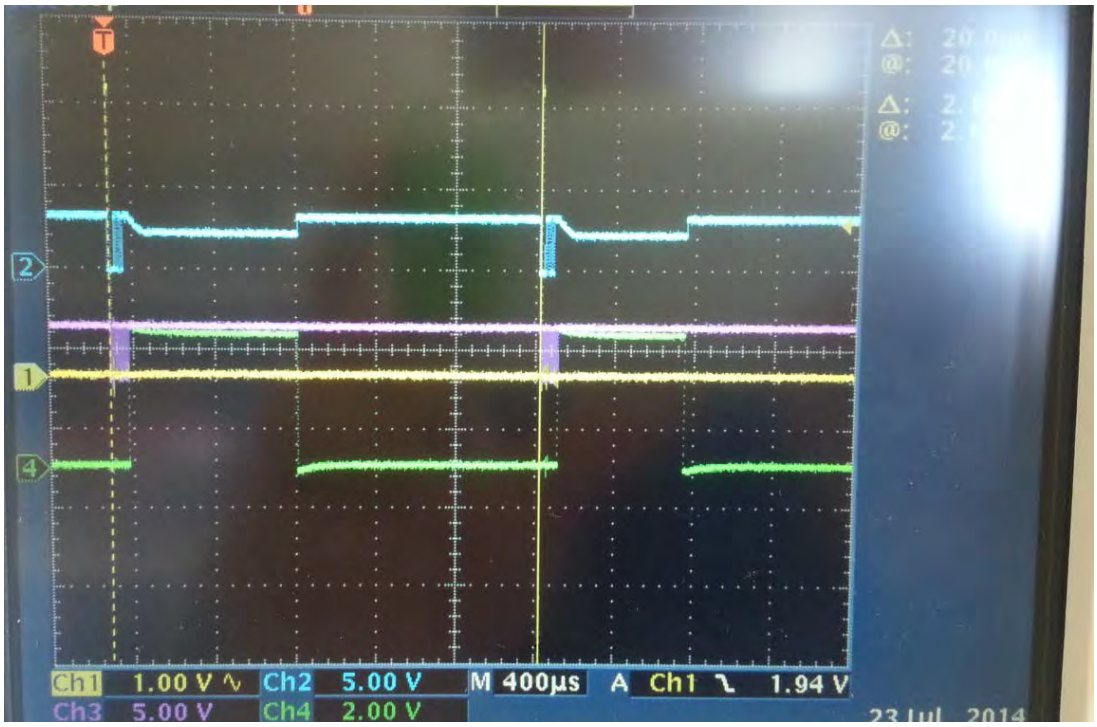


Figure 30. An example of the sample rate (CH1:DIN, CH2: DOUT, CH3: CLK, CH4:CS).

## 4. AD7792/7793 Application to the LLC Converter

Since the A/D converter is a two-channel A/D converter and has the capability to monitor both the voltage and the temperature signals simultaneously, the LLC circuit data acquisition system needs only one A/D converter. The FPGA does not need the software to monitor both the voltage and the temperature signal; however, the FPGA is required to monitor one converted digital data from the A/D converter, DOUT/RDY. The FPGA receives one signal (DOUT) and sends three signals (CS, SCLK, and DIN) to the A/D7792/7793 converter. The LLC converter circuit needs four optocouplers to isolate the signals from the battery. A proposed data acquisition architecture using the AD7792/7793 for the LLC circuit is shown in Figure 31 where four optocouplers are used.

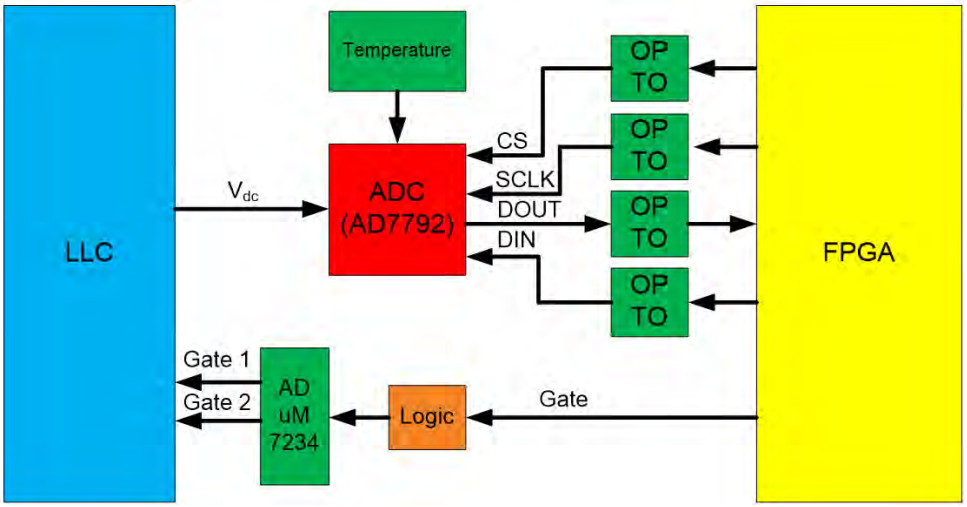


Figure 31. Proposed data acquisition architecture using the AD7792/7793 for the LLC circuit.

## B. ADS 1000 A/D CONVERTER EXAMINATION

The second solution considered for the data acquisition system is based on the ADS1000 A/D converter that uses the Inter-Integrated Circuit ($I^2C$) compatible serial interface. The ADS1000 is designed for applications including voltage monitors, battery management, and temperature measurement. This chip includes an A/D converter, the $I^2C$ interface, the programmable gain amplifier (PGA), and the clock oscillator. The PGA offers voltage gains up to eight, and amplifies small signals to measure them more precisely. The ADS1000's functional block diagram is shown in Figure 32 [12].

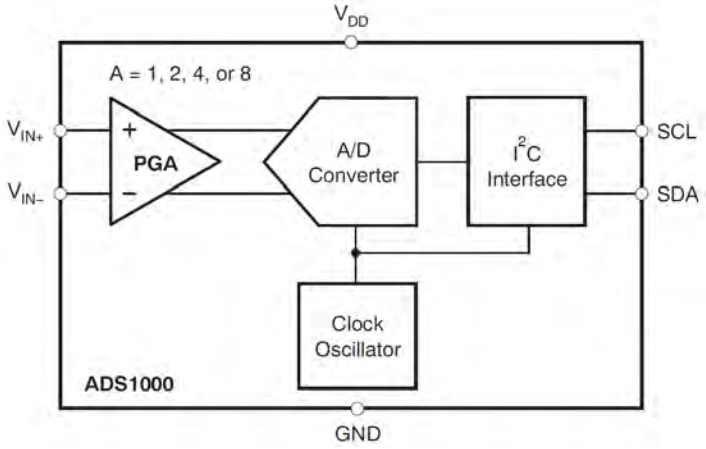


Figure 32. The ADS1000 functional block diagram (from [12]).

The ADS1000 can be applied to the LLC converter for a precise measurement result and an easy circuit design solution with less effort and time. The ADS1000 chip configuration is shown in Figure 33 [12].

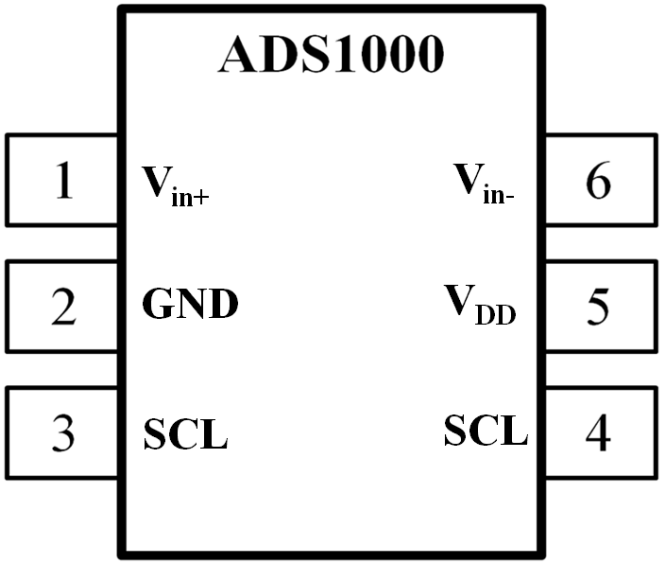


Figure 33. The ADS1000 pin configuration (from [12]).

### 1. Operation Mode

The ADS1000 has two operation modes: continuous and single conversion mode. In this thesis, only the continuous conversion mode is studied for the two A/D converters needed. The ADS1000 continuously converts the input analog signal to a digital signal. When the conversion is finished, the final data is transferred to the output register by the ADS1000, and the chip starts another conversion immediately after the transfer. Bit 7 in the configuration register is "1" for continuous conversion mode [12].

### 2. $I^2C$ Interface

The ADS1000 uses an $I^2C$ bus interface for communication between a master device and slaves. The communication in the $I^2C$ is always formed between two devices, usually a master and a slave. In this communication, both the master and slave can read or write; however, only the slave can communicate with the master. The ADS1000 is just

a slave device. The $I^2C$ interface has a two-wire connection, including a bidirectional serial data line (SDA) and a serial clock line (SCL). The SDA carries data, and the SCL is clock information. The $I^2C$ uses groups of eight bits to transmit the data. The SDA can be used to both transmit data and receive data. When a master receives data from a slave, the slave uses the data line; when a master transmits a data to a slave, the master uses the SDA. Only the master drives the SCL. Because the ADS1000 is a slave, the SCL is always an input to the ADS1000 [12].

During no communication, both the SDA and the SCL lines are high and the communication is idle. To begin a communication, the master causes a start condition for communications when the SCL is low. The start condition is indicated by the SCL being high and the SDA changing from high to low. A stop condition is indicated by the SCL being high and the SDA changing from low to high. After the start condition, the master sends the address byte, which identifies the slave it wants to communicate with. It also sends the slave the read/write bit together.

Data of the $I^2C$ bus always includes an acknowledge bit in the transmitted byte. After a master sends a byte to a slave, the master stops driving the SDA and waits for the slave's recognition. If the slave recognizes the acknowledge bit, it pulls the SDA to low. In the situation of non-acknowledge, the slave leaves the SDA high during acknowledge cycle, and the master sends the stop condition to finish communication. A timing diagram of ADS1000 is shown in Figure 34, and the parameters for this diagram are shown in Table 1 [12].

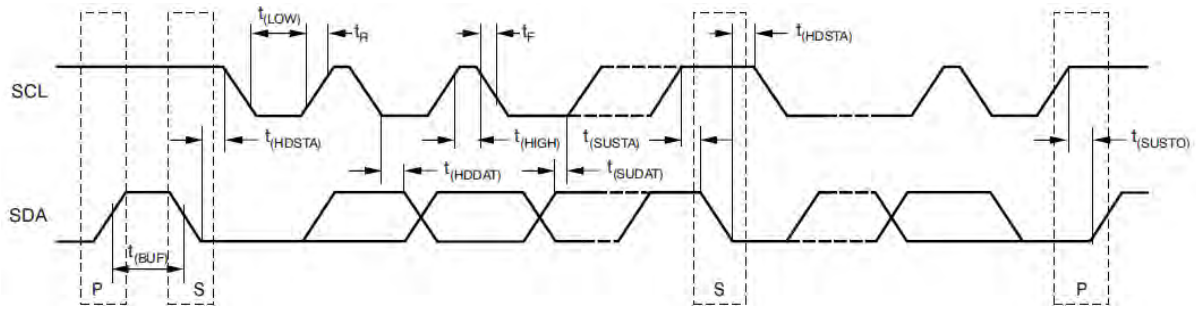


Figure 34. The $I^2C$ timing diagram (from [12]).

Table 1. The $I^2C$ timing diagram definitions (from [12]).

| PARAMETER | | FAST MODE | | HIGH-SPEED MODE | | UNITS |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| SCLK Operating Frequency | $f_{(SCLK)}$ | | 0.4 | | 3.4 | MHz |
| Bus Free Time Between STOP and START Condition | $t_{(BUF)}$ | 600 | | 160 | | ns |
| Hold Time After Repeated START Condition. After this period, the first clock is generated. | $t_{(HDSTA)}$ | 600 | | 160 | | ns |
| Repeated START Condition Setup Time | $t_{(SUSTA)}$ | 600 | | 160 | | ns |
| STOP Condition Setup Time | $t_{(SUSTO)}$ | 600 | | 160 | | ns |
| Data Hold Time | $t_{(HDDAT)}$ | 0 | | 0 | | ns |
| Data Setup Time | $t_{(SUDAT)}$ | 100 | | 10 | | ns |
| SCLK Clock Low Period | $t_{(LOW)}$ | 1300 | | 160 | | ns |
| SCLK Clock High Period | $t_{(HIGH)}$ | 600 | | 60 | | ns |
| Clock/Data Fall Time | $t_F$ | | 300 | | 160 | ns |
| Clock/Data Rise Time | $t_R$ | | 300 | | 160 | ns |

## 3. Reading from the ADS1000

The output register and data of the configuration register can be read at some designated point from the ADS1000. The ADS1000 uses three bytes for reading the address. The first two are used for the output register data, and the last byte of the three bytes is used for the configuration register data. It is not necessary for all three bytes to be read; only two bytes of the output register need to be read. Reading more than three bytes is meaningless. A reading timing diagram for the ADS1000 is shown in Figure 35 [12].

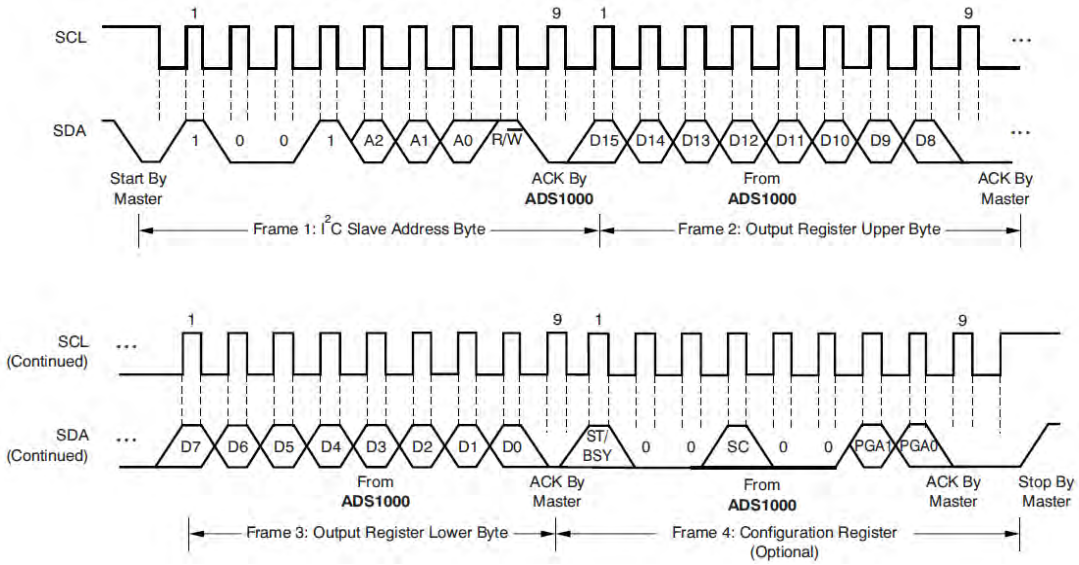


Figure 35. Reading timing diagram for the ADS1000 (from [12]).

## 4. Writing to the ADS1000

When addressing the ADS1000 to write, new data can be written to the configuration register. Writing more than one byte is meaningless, since the ADS1000 neglects bytes after one byte and only recognizes the first byte. The writing timing diagram for the ASD1000 is shown in Figure 36 [12].

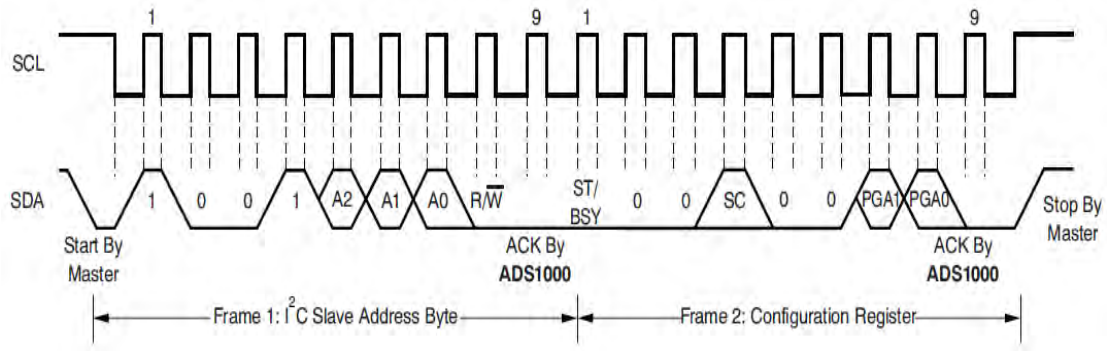


Figure 36. Writing timing diagram for the ASD1000 (from [12]).

## 5. Basic Concept of the ADS1000 Application

The ADS1000 application contains fully differential voltage inputs $V_{in+}$ and $V_{in-}$, where both must be positive. A typical connection of the ADS1000 is shown in Figure 37. Any type of microcontroller or microprocessor can be connected directly to the ADS1000. In any case, ADS1000 will not act as a master, so it never drives the SCL low. Using pull-up resistors for both the SDA and the SCL is very important since the $I^2C$ interface has an open drain feature to support multiple devices. High valued resistors offer less consumption of power; but cause a time delay on the bus and limit the bus speed. Low valued resistors offer a higher bus speed with more power consumption [12]. Since our data acquisition system is slow, the response does not need to be fast and larger pull-up resistors can be used.

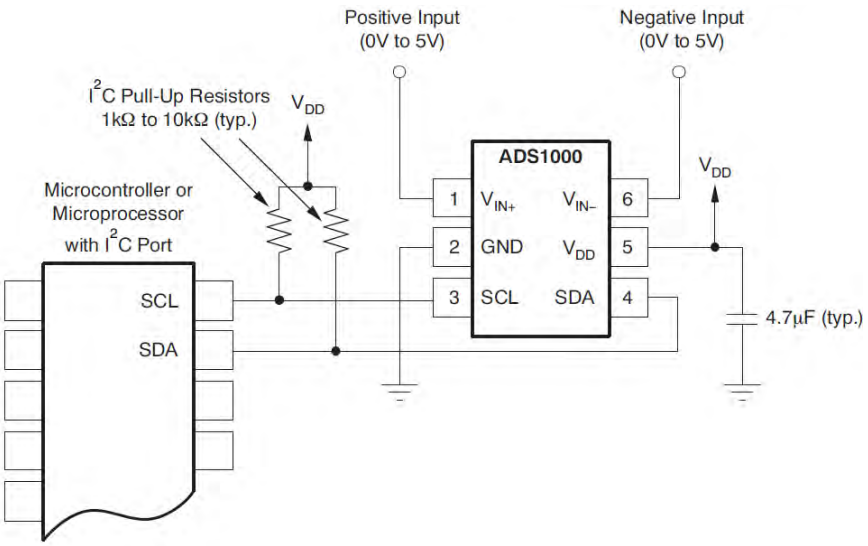


Figure 37. Example of the typical connection for the ASD1000 (from [12]).

Only single-ended inputs are used because our data acquisition system has two single-ended signals to be measured. Even though the ADS1000 has a fully differential input, it can measure single-ended signals also. Voltage and temperature inputs are connected to pin 1, and the ground is connected to pin 2 as shown in Figure 38. Negative voltage cannot be connected to the inputs since the ADS1000 only accepts positive voltage. The single-ended connection is shown in Figure 38 [12].

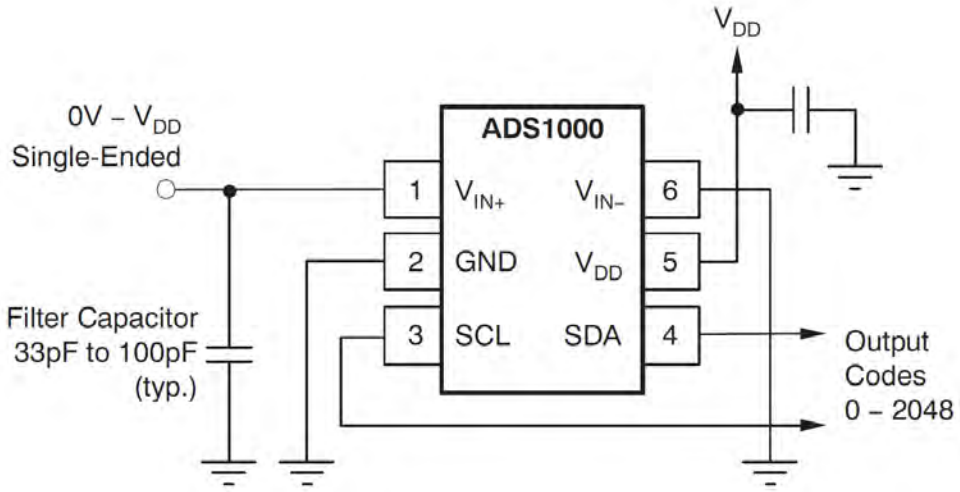


Figure 38. Example of single-ended input connection for the ASD1000 (from [12]).

## 6. ADS1000 Application to the LLC Converter

A proposed data acquisition architecture using the ADS1000 for the LLC converter is shown in Figure 39. It can be noted that there are two analog input signals into the A/D converter shown in Figure 39. One analog signal goes to each ADS1000. In the current example, the FPGA is a master and the ADS1000 is a slave. The FPGA is a microcontroller that has the capability of the $I^2C$ communication. When the FPGA receives the voltage and temperature data from the ADS1000, the ADS1000 uses the #1 SDA line in Figure 39. When the FPGA transmits read/write data to the ADS1000, the FPGA uses the #2 SDA line in Figure 38. Only the FPGA uses the # 3 SCL line in Figure 39. The ADS1000 never uses the SCL, since it cannot be a master. The SCL is always an input to the ADS1000 from the FPGA.

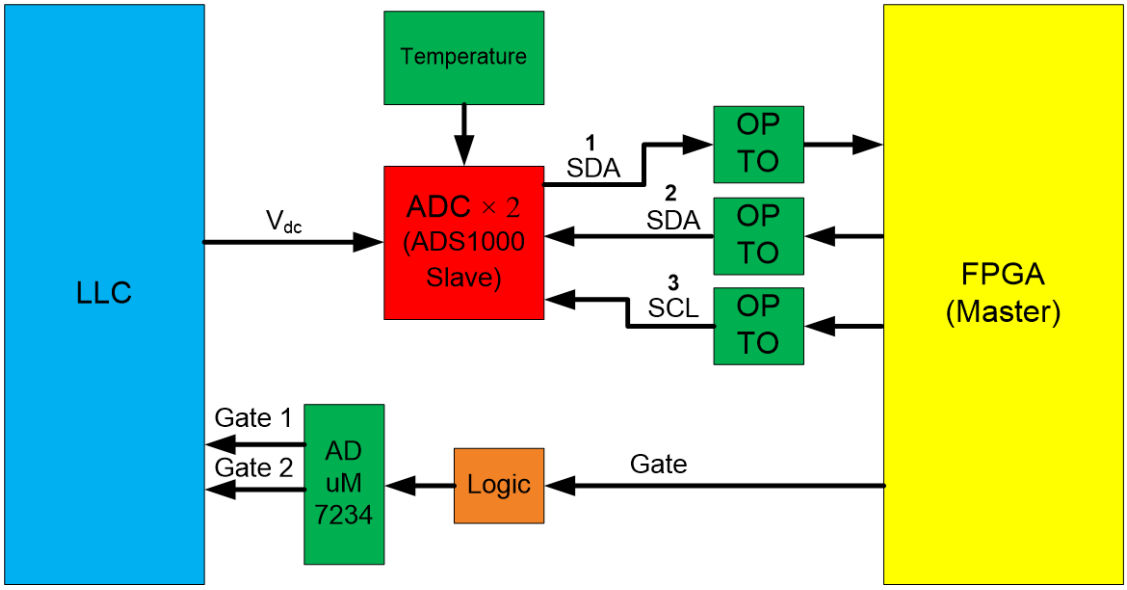


Figure 39. Proposed data acquisition architecture using the ADS1000 for the LLC converter.

The FPGA causes the start condition for the communication when the SCL is low. After the start condition, the FPGA sends the read/write bit to the ADS1000. After the FPGA sends a byte to the ADS1000, the FPGA stops driving the SDA and waits for the ADS1000's recognition. If the ADS1000 recognizes the acknowledge bit, it pulls the SDA low. In the situation of non-acknowledge, the ADS1000 leaves the SDA high

during the acknowledge cycle. The FPGA sends the stop condition to finish communication.

The FPGA transmits a command byte to the ADS1000 as a master. In the example of the ADS1000, even though it has the capability of bidirectional SDA communication, the circuit requires three optocouplers because it has a unidirectional communication (as shown in Figure 39). The ADS1112 is a dual channel A/D converter that operates just like the ADS1000 and works for two analog inputs, but the analysis presented in this thesis focuses on the operation of the ADS1000 that has only one input channel. Two ADS1000 A/D converters can be used or just one ADS1112 for this data acquisition system.

This study shows that when using A/D converters, the FPGA computational burden is greatly reduced compared to using two V/f converters. When using V/f converters, the FPGA receives converted digital signals and monitors them continuously since the V/f converters are asynchronous. On the other hand, with A/D converters the FPGA receives the information periodically, thus it does not have to work as much.

In conclusion, both A/D converters are viable solutions to reduce the FPGA computational load in comparison to the V/f solution used in the existing LLC converter. However, the ADS1000 is a preferred solution not only because the FPGA and the A/D converter have bidirectional communication capabilities but also in view of the fact that the ADS1000 requires fewer optocouplers and fewer pin connections than the AD7792/7793. In addition, in case the LLC converter needs better functions, the $I^2C$ bus interface, which is applied to the ADS1000, offers more flexibility without adding more A/D converters.

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# IV. CONCLUSIONS AND RECOMMENDATIONS

In the existing data acquisition architecture, the output of the V/f converters are asynchronous digital square-waves independent of all system clocks and must be constantly monitored to find the transitions so that the frequency can be measured. This process is very time consuming, and we propose to replace it on an FPGA with a fixed frequency sampling system using A/D converters so that voltage and temperature can be measured in real-time more easily. The asynchronous and continuous monitoring problems are easily solved with an A/D converter.

The FPGA transmits one signal to the ADS1000 converter at a given time. The FPGA transmits three digital signals to the AD7792/7793 A/D converter at a given time. From the experiment conducted, it was found that a sampling time of 10 Hz is sufficient to monitor these signals for the target application circuit.

For efficient processing, we recommend the use of the ADS1000 since the FPGA and the A/D converter have bidirectional communication capabilities. Furthermore, the ADS1000 requires less optocouplers, less space and fewer wires than the AD7792/7793 in the LLC circuit. In addition, $I^2C$ bus interface, which is applied to the ADS1000, offers more extensibility to the LLC converter without connection waste.

A viable alternative data acquisition strategy that has fewer interconnections and reduces the processing burden on the FPGA by making the signals synchronous was identified in this thesis.

The given multi-cell charger has 12-pin interfaces between the LLC converters and the FPGA as was mentioned in Chapter I.B. Though this charger works well at this time, if many batteries (i.e., 20 or 30) must be charged, it could become a serious problem to interconnect everything. Increased number of batteries means more cables. If the circuit has 20 batteries, the circuit needs 240 cables; thus, future work should focus on reducing the number of cables, which was not accomplished in this thesis. This thesis proposes a solution to improve the hardware design of the LLC converter. Future work

should investigate the software for communication between an A/D converter and the FPGA.

# APPENDIX A. AD7792/7793 DATASHEET

ANALOG DEVICES

# 3-Channel, Low Noise, Low Power, 16-/24-Bit Σ-Δ ADC with On-Chip In-Amp and Reference

## AD7792/AD7793

### FEATURES

- Up to 23 bits effective resolution
- RMS noise
  - 40 nV @ 4.17 Hz
  - 85 nV @ 16.7 Hz
- Current: 400 µA typical
- Power-down: 1 µA maximum
- Low noise programmable gain instrumentation amp
- Band gap reference with 4 ppm/°C drift typical
- Update rate: 4.17 Hz to 470 Hz
- 3 differential inputs
- Internal clock oscillator
- Simultaneous 50 Hz/60 Hz rejection
- Programmable current sources
- On-chip bias voltage generator
- Burnout currents
- Power supply: 2.7 V to 5.25 V
- −40°C to +105°C temperature range
- Independent interface power supply
- 16-lead TSSOP package
- Interface
  - 3-wire serial
  - SPI®, QSPI™, MICROWIRE™, and DSP compatible
  - Schmitt trigger on SCLK

### APPLICATIONS

- Thermocouple measurements
- RTD measurements
- Thermistor measurements
- Gas analysis
- Industrial process control
- Instrumentation
- Portable instrumentation
- Blood analysis
- Smart transmitters
- Liquid/gas chromatography
- 6-digit DVM

### FUNCTIONAL BLOCK DIAGRAM

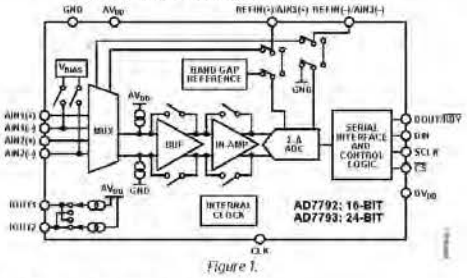


*Figure 1.*

### GENERAL DESCRIPTION

The AD7792/AD7793 are low power, low noise, complete analog front ends for high precision measurement applications. The AD7792/AD7793 contain a low noise 16-/24-bit Σ-Δ ADC with three differential analog inputs. The on-chip, low noise instrumentation amplifier means that signals of small amplitude can be interfaced directly to the ADC. With a gain setting of 64, the rms noise is 40 nV when the update rate equals 4.17 Hz.

The devices contain a precision low noise, low drift internal band gap reference and can accept an external differential reference. Other on-chip features include programmable excitation current sources, burnout currents, and a bias voltage generator. The bias voltage generator sets the common-mode voltage of a channel to $AV_{DD}/2$.

The devices can be operated with either the internal clock or an external clock. The output data rate from the parts is software-programmable and can be varied from 4.17 Hz to 470 Hz.

The parts operate with a power supply from 2.7 V to 5.25 V. They consume a current of 400 µA typical and are housed in a 16-lead TSSOP package.



One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
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# IMPORTANT LINKS for the AD7792_7793*

Last content update 12/19/2013 07:18 pm

## DOCUMENTATION

**UG-518** AD7792/AD7793 Key Sheet | AD7792/AD7793 Condensed Rev

**AN-968:** Current Sources: Options and Circuits

**AN-880:** ADC Requirements for Temperature Measurement Systems

**AN-607:** Selecting a Low Bandwidth (Less than 15 kSPS) Sigma-Delta ADC

**AN-615:** Peak-to-Peak Resolution Versus Effective Resolution

**AN-101:** Cross Plot Generator Allows Quick A/D Converter Evaluation

**AN-397:** Electrically Induced Damage to Standard Linear Integrated Circuits

**AN-347:** Shielding and Guarding

**AN-202:** An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change

**AN-388:** Using Sigma-Delta Converters-Part 1

**AN-389:** Using Sigma-Delta Converters-Part 2

**AN-283:** Sigma-Delta ADCs and DACs

**MS-2210:** Designing Power Supplies for High Speed ADC

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FAQs for the AD779x family.

**FOR THE AD7793 ONLY**

**CN-0326:** Isolated Low Power pH Monitor with Temperature Compensation

**CN-0172:** High Accuracy Multichannel Thermocouple Measurement Solution

**CN-0206:** Complete Type T Thermocouple Measurement System with Cold Junction Compensation

**CN-0067:** Fully Isolated Input Module Based on the AD7793 24-Bit Sigma-Delta ADC, the ADuM5401 Digital Isolator, and a High Performance In-Amp

**CN-0066:** Fully Isolated Input Module Based on the AD7793 24-Bit Sigma-Delta ADC and the ADuM5401 Digital Isolator

**UG-181:** PLC Demo System User Guide

PLC Evaluation Board Simplifies Design of Industrial Process Control Systems

Simplifying Design of Industrial Process-Control Systems with PLC Evaluation Boards (Part 1 of 2)

Simplifying Design of Industrial Process-Control Systems with PLC Evaluation Boards (Part 2 of 2)

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Sigma Delta ADCs (Less than 15 kSPS)

**Product Recommendations and Companion Products**

## DESIGN TOOLS, MODELS, DRIVERS & SOFTWARE

Sigma-Delta ADC Tutorial

Digital Filter Model Spreadsheets

AD7792 - Microcontroller No-OS Driver

AD7793 - Microcontroller No-OS Driver

AD7793 IIO Low Power Sigma-Delta ADC Linux Driver (Wiki Site)

## EVALUATION KITS & SYMBOLS & FOOTPRINTS

View the Evaluation Boards and Kits page for the AD7792

View the Evaluation Boards and Kits page for the AD7793

Symbols and Footprints for the AD7792

Symbols and Footprints for the AD77923

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**Quality and Reliability**
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**AD7792**

**AD7793**

- View Price & Packaging
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ANALOG DEVICES

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# SPECIFICATIONS

$AV_{DD}$ = 2.7 V to 5.25 V; $DV_{DD}$ = 2.7 V to 5.25 V; GND = 0 V; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

Table 1.

| Parameter | AD7792B/AD7793B[1] | Unit | Test Conditions/Comments |
|---|---|---|---|
| ADC CHANNEL | | | |
| Output Update Rate | 4.17 to 470 | Hz nom | |
| No Missing Codes[2] | 24 | Bits min | $f_{ADC}$ < 242 Hz, AD7793 |
| | 16 | Bits min | AD7792 |
| Resolution | | | See Output Noise and Resolution Specifications |
| Output Noise and Update Rates | | | See Output Noise and Resolution Specifications |
| Integral Nonlinearity | ±15 | ppm of FSR max | |
| Offset Error[3] | ±1 | µV typ | |
| Offset Error Drift vs. Temperature[4] | ±10 | nV/°C typ | |
| Full-Scale Error[3, 5] | ±10 | µV typ | |
| Gain Drift vs. Temperature[4] | ±1 | ppm/°C typ | Gain = 1 to 16, external reference |
| | ±3 | ppm/°C typ | Gain = 32 to 128, external reference |
| Power Supply Rejection | 100 | dB min | AIN = 1 V/gain, gain ≥ 4, external reference |
| ANALOG INPUTS | | | |
| Differential Input Voltage Ranges | $\pm V_{REF}$/Gain | V nom | $V_{REF}$ = REFIN(+) − REFIN(−) or internal reference, gain = 1 to 128 |
| Absolute AIN Voltage Limits[6] | | | |
| Unbuffered Mode | GND − 30 mV | V min | Gain = 1 or 2 |
| | $AV_{DD}$ + 30 mV | V max | |
| Buffered Mode | GND + 100 mV | V min | Gain = 1 or 2 |
| | $AV_{DD}$ − 100 mV | V max | |
| In-Amp Active | GND + 300 mV | V min | Gain = 4 to 128 |
| | $AV_{DD}$ − 1.1 | V max | |
| Common-Mode Voltage, $V_{CM}$ | 0.5 | V min | $V_{CM}$ = (AIN(+) + AIN(−))/2, gain = 4 to 128 |
| Analog Input Current | | | |
| Buffered Mode or In-Amp Active | | | |
| Average Input Current[7] | ±1 | nA max | Gain = 1 or 2, update rate < 100 Hz |
| | ±250 | pA max | Gain = 4 to 128, update rate < 100 Hz |
| Average Input Current Drift | ±2 | pA/°C typ | |
| Unbuffered Mode | | | Gain = 1 or 2. |
| Average Input Current | ±400 | nA/V typ | Input current varies with input voltage |
| Average Input Current Drift | ±50 | pA/V/°C typ | |
| Normal Mode Rejection[2] | | | |
| Internal Clock | | | |
| @ 50 Hz, 60 Hz | 65 | dB min | 80 dB typ, 50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010[8] |
| @ 50 Hz | 80 | dB min | 90 dB typ, 50 ± 1 Hz, FS[3:0] = 1001[8] |
| @ 60 Hz | 90 | dB min | 100 dB typ, 60 ± 1 Hz, FS[3:0] = 1000[8] |
| External Clock | | | |
| @ 50 Hz, 60 Hz | 80 | dB min | 90 dB typ, 50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010[8] |
| @ 50 Hz | 94 | dB min | 100 dB typ, 50 ± 1 Hz, FS[3:0] = 1001[8] |
| @ 60 Hz | 90 | dB min | 100 dB typ, 60 ± 1 Hz, FS[3:0] = 1000[8] |
| Common-Mode Rejection | | | |
| @ DC | 100 | dB min | AIN = 1 V/gain, gain ≥ 4 |
| @ 50 Hz, 60 Hz[9] | 100 | dB min | 50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010[8] |
| @ 50 Hz, 60 Hz[9] | 100 | dB min | 50 ± 1 Hz (FS[3:0] = 1001)[8], 60 ± 1 Hz (FS[3:0] = 1000)[8] |

| Parameter | AD7792B/AD7793B[1] | Unit | Test Conditions/Comments |
|---|---|---|---|
| REFERENCE | | | |
| Internal Reference | | | |
| Internal Reference Initial Accuracy | 1.17 ± 0.01% | V min/max | $AV_{DD}$ = 4 V, $T_A$ = 25°C |
| Internal Reference Drift[2] | 4 | ppm/°C typ | |
| | 15 | ppm/°C max | |
| Power Supply Rejection | 85 | dB typ | |
| External Reference | | | |
| External REFIN Voltage | 2.5 | V nom | REFIN = REFIN(+) − REFIN(−) |
| Reference Voltage Range[2] | 0.1 | V min | |
| | $AV_{DD}$ | V max | When $V_{REF}$ = $AV_{DD}$, the differential input must be limited to 0.9 × $V_{REF}$ /gain if the in-amp is active |
| Absolute REFIN Voltage Limits[2] | GND − 30 mV | V min | |
| | $AV_{DD}$ + 30 mV | V max | |
| Average Reference Input Current | 400 | nA/V typ | |
| Average Reference Input Current Drift | ±0.03 | nA/V/°C typ | |
| Normal Mode Rejection | Same as for analog inputs | | |
| Common-Mode Rejection | 100 | dB typ | |
| EXCITATION CURRENT SOURCES | | | |
| (IEXC1 and IEXC2) | | | |
| Output Current | 10/210/1000 | µA nom | |
| Initial Tolerance at 25°C | ±5 | % typ | |
| Drift | 200 | ppm/°C typ | |
| Current Matching | ±0.5 | % typ | Matching between IEXC1 and IEXC2; $V_{OUT}$ = 0 V |
| Drift Matching | 50 | ppm/°C typ | |
| Line Regulation ($V_{DD}$) | 2 | %/V typ | $AV_{DD}$ = 5 V ± 5% |
| Load Regulation | 0.2 | %/V typ | |
| Output Compliance | $AV_{DD}$ − 0.65 | V max | 10 µA or 210 µA currents selected |
| | $AV_{DD}$ − 1.1 | V max | 1 mA currents selected |
| | GND − 30 mV | V min | |
| TEMPERATURE SENSOR | | | |
| Accuracy | ±2 | °C typ | Applies if user calibrates the temperature sensor |
| Sensitivity | 0.81 | mV/°C typ | |
| BIAS VOLTAGE GENERATOR | | | |
| $V_{BIAS}$ | $AV_{DD}$/2 | V nom | |
| $V_{BIAS}$ Generator Start-Up Time | See Figure 10 | ms/nF typ | Dependent on the capacitance on the AIN pin |
| INTERNAL/EXTERNAL CLOCK | | | |
| Internal Clock | | | |
| Frequency[2] | 64 ± 3% | kHz min/max | |
| Duty Cycle | 50:50 | % typ | |
| External Clock | | | |
| Frequency | 64 | kHz nom | A 128 kHz external clock can be used if the divide-by-2 function is used (Bit CLK1 = CLK0 = 1) |
| Duty Cycle | 45:55 to 55:45 | % typ | Applies for external 64 kHz clock; a 128 kHz clock can have a less stringent duty cycle |
| LOGIC INPUTS | | | |
| $\overline{CS}$[2] | | | |
| $V_{INL}$, Input Low Voltage | 0.8 | V max | $DV_{DD}$ = 5 V |
| | 0.4 | V max | $DV_{DD}$ = 3 V |
| $V_{INH}$, Input High Voltage | 2.0 | V min | $DV_{DD}$ = 3 V or 5 V |

| Parameter | AD7792B/AD7793B[1] | Unit | Test Conditions/Comments |
|---|---|---|---|
| SCLK, CLK, and DIN (Schmitt-Triggered Input)[2] | | | |
| $V_T(+)$ | 1.4/2 | V min/V max | $DV_{DD}$ = 5 V |
| $V_T(-)$ | 0.8/1.7 | V min/V max | $DV_{DD}$ = 5 V |
| $V_T(+) - V_T(-)$ | 0.1/0.17 | V min/V max | $DV_{DD}$ = 5 V |
| $V_T(+)$ | 0.9/2 | V min/V max | $DV_{DD}$ = 3 V |
| $V_T(-)$ | 0.4/1.35 | V min/V max | $DV_{DD}$ = 3 V |
| $V_T(+) - V_T(-)$ | 0.06/0.13 | V min/V max | $DV_{DD}$ = 3 V |
| Input Currents | ±10 | μA max | $V_{IN}$ = $DV_{DD}$ or GND |
| Input Capacitance | 10 | pF typ | All digital inputs |
| LOGIC OUTPUTS (INCLUDING CLK) | | | |
| $V_{OH}$, Output High Voltage[3] | $DV_{DD}$ − 0.6 | V min | $DV_{DD}$ = 3 V, $I_{SOURCE}$ = 100 μA |
| $V_{OL}$, Output Low Voltage[3] | 0.4 | V max | $DV_{DD}$ = 3 V, $I_{SINK}$ = 100 μA |
| $V_{OH}$, Output High Voltage[3] | 4 | V min | $DV_{DD}$ = 5 V, $I_{SOURCE}$ = 200 μA |
| $V_{OL}$, Output Low Voltage[3] | 0.4 | V max | $DV_{DD}$ = 5 V, $I_{SINK}$ = 1.6 mA (DOUT/$\overline{RDY}$)/800 μA (CLK) |
| Floating-State Leakage Current | ±10 | μA max | |
| Floating-State Output Capacitance | 10 | pF typ | |
| Data Output Coding | Offset binary | | |
| SYSTEM CALIBRATION[4] | | | |
| Full-Scale Calibration Limit | +1.05 × FS | V max | |
| Zero-Scale Calibration Limit | −1.05 × FS | V min | |
| Input Span | 0.8 × FS | V min | |
| | 2.1 × FS | V max | |
| POWER REQUIREMENTS[5] | | | |
| Power Supply Voltage | | | |
| $AV_{DD}$ to GND | 2.7/5.25 | V min/max | |
| $DV_{DD}$ to GND | 2.7/5.25 | V min/max | |
| Power Supply Currents | | | |
| $I_{DD}$ Current | 140 | μA max | 110 μA typ @ $AV_{DD}$ = 3 V, 125 μA typ @ $AV_{DD}$ = 5 V, unbuffered mode, external reference |
| | 185 | μA max | 130 μA typ @ $AV_{DD}$ = 3 V, 165 μA typ @ $AV_{DD}$ = 5 V, buffered mode, gain = 1 or 2, external reference |
| | 400 | μA max | 300 μA typ @ $AV_{DD}$ = 3 V, 350 μA typ @ $AV_{DD}$ = 5 V, gain = 4 to 128, external reference |
| | 500 | μA max | 400 μA typ @ $AV_{DD}$ = 3 V, 450 μA typ @ $AV_{DD}$ = 5 V, gain = 4 to 128, internal reference |
| $I_{DD}$ (Power-Down Mode) | 1 | μA max | |

[1] Temperature range is −40°C to +105°C. At the 19.6 Hz and 39.2 Hz update rates, the INL, power supply rejection (PSR), common-mode rejection (CMR), and normal mode rejection (NMR) do not meet the data sheet specification if the voltage on the AIN(+) or AIN(−) pins exceed $AV_{DD}$ − 1.6 V typically. When this voltage is exceeded, the INL, for example, is reduced to 18 ppm of FS typically while the PSR is reduced to 69 dB typically. Therefore, for guaranteed performance at these update rates, the absolute voltage on the analog input pins needs to be below $AV_{DD}$ − 1.6 V.
[2] Specification is not production tested, but is supported by characterization data at initial product release.
[3] Following a calibration, this error is in the order of the noise for the programmed gain and update rate selected.
[4] Recalibration at any temperature removes these errors.
[5] Full-scale error applies to both positive and negative full-scale and applies at the factory calibration conditions ($AV_{DD}$ = 4 V, gain = 1, $T_A$ = 25°C).
[6] FS[3:0] are the four bits used in the mode register to select the output word rate.
[7] Digital inputs equal to $DV_{DD}$ or GND with excitation currents and bias voltage generator disabled.

## TIMING CHARACTERISTICS

$AV_{DD}$ = 2.7 V to 5.25 V, $DV_{DD}$ = 2.7 V to 5.25 V, GND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = $DV_{DD}$, unless otherwise noted.

Table 2.

| Parameter[1, 2] | Limit at $T_{MIN}$, $T_{MAX}$ (B Version) | Unit | Conditions/Comments |
|---|---|---|---|
| $t_3$ | 100 | ns min | SCLK high pulse width |
| $t_4$ | 100 | ns min | SCLK low pulse width |
| Read Operation | | | |
| $t_1$ | 0 | ns min | $\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time |
| | 60 | ns max | $DV_{DD}$ = 4.75 V to 5.25 V |
| | 80 | ns max | $DV_{DD}$ = 2.7 V to 3.6 V |
| $t_2$[3] | 0 | ns min | SCLK active edge to data valid delay[4] |
| | 60 | ns max | $DV_{DD}$ = 4.75 V to 5.25 V |
| | 80 | ns max | $DV_{DD}$ = 2.7 V to 3.6 V |
| $t_5$[5, 6] | 10 | ns min | Bus relinquish time after $\overline{CS}$ inactive edge |
| | 80 | ns max | |
| $t_6$ | 0 | ns min | SCLK inactive edge to $\overline{CS}$ inactive edge |
| $t_7$ | 10 | ns min | SCLK inactive edge to DOUT/$\overline{RDY}$ high |
| Write Operation | | | |
| $t_8$ | 0 | ns min | $\overline{CS}$ falling edge to SCLK active edge setup time[4] |
| $t_9$ | 30 | ns min | Data valid to SCLK edge setup time |
| $t_{10}$ | 25 | ns min | Data valid to SCLK edge hold time |
| $t_{11}$ | 0 | ns min | $\overline{CS}$ rising edge to SCLK edge hold time |

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of $DV_{DD}$) and timed from a voltage level of 1.6 V.
[2] See Figure 3 and Figure 4.
[3] These numbers are measured with the load circuit shown in Figure 2 and defined as the time required for the output to cross the $V_{OL}$ or $V_{OH}$ limits.
[4] SCLK active edge is falling edge of SCLK.
[5] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit shown in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.
[6] $\overline{RDY}$ returns high after a read of the ADC. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while $\overline{RDY}$ is high, although care should be taken to ensure that subsequent reads do not occur close to the next output update. In continuous read mode, the digital word can be read only once.

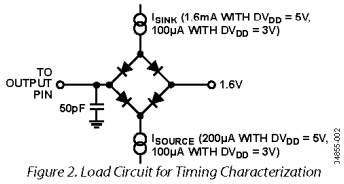
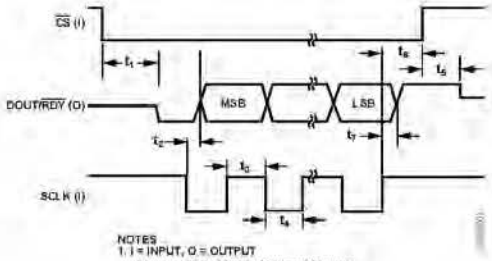


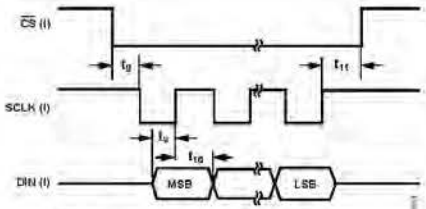

*Figure 2. Load Circuit for Timing Characterization*

## TIMING DIAGRAMS




NOTES
1. I = INPUT, O = OUTPUT

*Figure 3. Read Cycle Timing Diagram*




NOTES
1. I = INPUT, O = OUTPUT

*Figure 4. Write Cycle Timing Diagram*

## ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

Table 3.

| Parameter | Ratings |
|---|---|
| $AV_{DD}$ to GND | −0.3 V to +7 V |
| $DV_{DD}$ to GND | −0.3 V to +7 V |
| Analog Input Voltage to GND | −0.3 V to $AV_{DD}$ + 0.3 V |
| Reference Input Voltage to GND | −0.3 V to $AV_{DD}$ + 0.3 V |
| Digital Input Voltage to GND | −0.3 V to $DV_{DD}$ + 0.3 V |
| Digital Output Voltage to GND | −0.3 V to $DV_{DD}$ + 0.3 V |
| AIN/Digital Input Current | 10 mA |
| Operating Temperature Range | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Maximum Junction Temperature | 150°C |
| TSSOP | |
| $\theta_{JA}$ Thermal Impedance | 128°C/W |
| $\theta_{JC}$ Thermal Impedance | 14°C/W |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

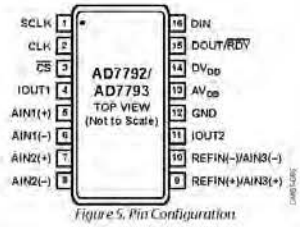



*Figure 5. Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | SCLK | Serial Clock Input. This serial clock input is for data transfers to and from the ADC. The SCLK has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the ADC in smaller batches of data. |
| 2 | CLK | Clock In/Clock Out. The internal clock can be made available at this pin. Alternatively, the internal clock can be disabled, and the ADC can be driven by an external clock. This allows several ADCs to be driven from a common clock, allowing simultaneous conversions to be performed. |
| 3 | $\overline{CS}$ | Chip Select Input. This is an active low logic input used to select the ADC. $\overline{CS}$ can be used to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device. |
| 4 | IOUT1 | Output of Internal Excitation Current Source. The internal excitation current source can be made available at this pin. The excitation current source is programmable so that the current can be 10 µA, 210 µA, or 1 mA. Either IEXC1 or IEXC2 can be switched to this output. |
| 5 | AIN1(+) | Analog Input. AIN1(+) is the positive terminal of the differential analog input pair AIN1(+)/AIN1(−). |
| 6 | AIN1(−) | Analog Input. AIN1(−) is the negative terminal of the differential analog input pair AIN1(+)/AIN1(−). |
| 7 | AIN2(+) | Analog Input. AIN2(+) is the positive terminal of the differential analog input pair AIN2(+)/AIN2(−). |
| 8 | AIN2(−) | Analog Input. AIN2(−) is the negative terminal of the differential analog input pair AIN2(+)/AIN2(−). |
| 9 | REFIN(+)/AIN3(+) | Positive Reference Input/Analog Input. An external reference can be applied between REFIN(+) and REFIN(−). REFIN(+) can lie anywhere between $AV_{DD}$ and GND + 0.1 V. The nominal reference voltage REFIN(+) − REFIN(−) is 2.5 V, but the part functions with a reference from 0.1 V to $AV_{DD}$. Alternatively, this pin can function as AIN3(+) where AIN3(+) is the positive terminal of the differential analog input pair AIN3(+)/AIN3(−). |
| 10 | REFIN(−)/AIN3(−) | Negative Reference Input/Analog Input. REFIN(−) is the negative reference input for REFIN. This reference input can lie anywhere between GND and $AV_{DD}$ − 0.1 V. This pin also functions as AIN3(−), which is the negative terminal of the differential analog input pair AIN3(+)/AIN3(−). |
| 11 | IOUT2 | Output of Internal Excitation Current Source. The internal excitation current source can be made available at this pin. The excitation current source is programmable so that the current can be 10 µA, 210 µA, or 1 mA. Either IEXC1 or IEXC2 can be switched to this output. |
| 12 | GND | Ground Reference Point. |
| 13 | $AV_{DD}$ | Supply Voltage, 2.7 V to 5.25 V. |
| 14 | $DV_{DD}$ | Digital Interface Supply Voltage. The logic levels for the serial interface pins are related to this supply, which is between 2.7 V and 5.25 V. The $DV_{DD}$ voltage is independent of the voltage on $AV_{DD}$; therefore, $AV_{DD}$ can equal 5 V with $DV_{DD}$ at 3 V or vice versa. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 15 | DOUT/$\overline{RDY}$ | Serial Data Output/Data Ready Output. DOUT/$\overline{RDY}$ serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, DOUT/$\overline{RDY}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs.<br>The DOUT/$\overline{RDY}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/$\overline{RDY}$ pin. With $\overline{CS}$ low, the data/control word information is placed on the DOUT/$\overline{RDY}$ pin on the SCLK falling edge and is valid on the SCLK rising edge. |
| 16 | DIN | Serial Data Input. This serial data input is to the input shift register on the ADC. Data in this shift register is transferred to the control registers within the ADC; the register selection bits of the communications register identify the appropriate register. |

# OUTPUT NOISE AND RESOLUTION SPECIFICATIONS

## EXTERNAL REFERENCE

Table 5 shows the output rms noise of the AD7792/AD7793 for some of the update rates and gain settings. The numbers given are for the bipolar input range with an external 2.5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table 6 and Table 7 show the effective resolution, with the output peak-to-peak (p-p) resolution shown in parentheses for the AD7793 and AD7792, respectively. It is important to note that the effective resolution is calculated using the rms noise, while the p-p resolution is based on the p-p noise. The p-p resolution represents the resolution for which there is no code flicker. These numbers are typical and are rounded to the nearest LSB.

Table 5. Output RMS Noise (μV) vs. Gain and Output Update Rate for the AD7792 and AD7793 Using an External 2.5 V Reference

| Update Rate (Hz) | Gain of 1 | Gain of 2 | Gain of 4 | Gain of 8 | Gain of 16 | Gain of 32 | Gain of 64 | Gain of 128 |
|---|---|---|---|---|---|---|---|---|
| 4.17 | 0.64 | 0.6 | 0.29 | 0.22 | 0.1 | 0.065 | 0.039 | 0.041 |
| 8.33 | 1.04 | 0.96 | 0.38 | 0.26 | 0.13 | 0.078 | 0.057 | 0.055 |
| 16.7 | 1.55 | 1.45 | 0.54 | 0.36 | 0.18 | 0.11 | 0.087 | 0.086 |
| 33.2 | 2.3 | 2.13 | 0.74 | 0.5 | 0.23 | 0.17 | 0.124 | 0.118 |
| 62 | 2.95 | 2.85 | 0.92 | 0.58 | 0.29 | 0.2 | 0.153 | 0.144 |
| 123 | 4.89 | 4.74 | 1.49 | 1 | 0.48 | 0.32 | 0.265 | 0.283 |
| 242 | 11.76 | 9.5 | 4.02 | 1.96 | 0.88 | 0.45 | 0.379 | 0.397 |
| 470 | 11.33 | 9.44 | 3.07 | 1.79 | 0.99 | 0.63 | 0.568 | 0.593 |

Table 6. Typical Resolution (Bits) vs. Gain and Output Update Rate for the AD7793 Using an External 2.5 V Reference

| Update Rate (Hz) | Gain of 1 | Gain of 2 | Gain of 4 | Gain of 8 | Gain of 16 | Gain of 32 | Gain of 64 | Gain of 128 |
|---|---|---|---|---|---|---|---|---|
| 4.17 | 23 (20.5) | 22 (19.5) | 22 (19.5) | 21.5 (19) | 21.5 (19) | 21 (18.5) | 21 (18.5) | 20 (17.5) |
| 8.33 | 22 (19.5) | 21.5 (19) | 21.5 (19) | 21 (18.5) | 21 (18.5) | 21 (18.5) | 20.5 (18) | 19.5 (17) |
| 16.7 | 21.5 (19) | 20.5 (18) | 21 (18.5) | 20.5 (18) | 20.5 (18) | 20.5 (18) | 20 (17.5) | 19 (16.5) |
| 33.2 | 21 (18.5) | 20 (17.5) | 20.5 (18) | 20 (17.5) | 20.5 (18) | 20 (17.5) | 19 (16.5) | 18.5 (16) |
| 62 | 20.5 (18) | 19.5 (17) | 20.5 (18) | 20 (17.5) | 20 (17.5) | 19.5 (17) | 19 (16.5) | 18 (15.5) |
| 123 | 20 (17.5) | 19 (16.5) | 19.5 (17) | 19 (16.5) | 19.5 (17) | 19 (16.5) | 18 (15.5) | 17 (14.5) |
| 242 | 18.5 (16) | 18 (15.5) | 18 (15.5) | 18 (15.5) | 18.5 (16) | 18.5 (16) | 17.5 (15) | 16.5 (14) |
| 470 | 18.5 (16) | 18 (15.5) | 18.5 (16) | 18.5 (16) | 18 (15.5) | 18 (15.5) | 17 (14.5) | 16 (13.5) |

Table 7. Typical Resolution (Bits) vs. Gain and Output Update Rate for the AD7792 Using an External 2.5 V Reference

| Update Rate (Hz) | Gain of 1 | Gain of 2 | Gain of 4 | Gain of 8 | Gain of 16 | Gain of 32 | Gain of 64 | Gain of 128 |
|---|---|---|---|---|---|---|---|---|
| 4.17 | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) |
| 8.33 | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) |
| 16.7 | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) |
| 33.2 | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) |
| 62 | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (15.5) |
| 123 | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 165 (15.5) | 16 (14.5) |
| 242 | 16 (16) | 16 (15.5) | 16 (15.5) | 16 (15.5) | 16 (16) | 16 (16) | 16 (15) | 16 (14) |
| 470 | 16 (16) | 16 (15.5) | 16 (16) | 16 (16) | 16 (15.5) | 16 (15.5) | 16 (14.5) | 15.5 (13.5) |

## INTERNAL REFERENCE

Table 8 shows the output rms noise of the AD7792/AD7793 for some of the update rates and gain settings. The numbers given are for the bipolar input range with the internal 1.17 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table 9 and Table 10 show the effective resolution, with the output peak-to-peak (p-p) resolution given in parentheses for the AD7793 and AD7792, respectively. It is important to note that the effective resolution is calculated using the rms noise, while the p-p resolution is calculated based on p-p noise. The p-p resolution represents the resolution for which there is no code flicker. These numbers are typical and are rounded to the nearest LSB.

Table 8. Output RMS Noise (μV) vs. Gain and Output Update Rate for the AD7792 and AD7793 Using the Internal Reference

| Update Rate (Hz) | Gain of 1 | Gain of 2 | Gain of 4 | Gain of 8 | Gain of 16 | Gain of 32 | Gain of 64 | Gain of 128 |
|---|---|---|---|---|---|---|---|---|
| 4.17 | 0.81 | 0.67 | 0.32 | 0.2 | 0.13 | 0.065 | 0.04 | 0.039 |
| 8.33 | 1.18 | 1.11 | 0.41 | 0.25 | 0.16 | 0.078 | 0.058 | 0.059 |
| 16.7 | 1.96 | 1.72 | 0.55 | 0.36 | 0.25 | 0.11 | 0.088 | 0.088 |
| 33.2 | 2.99 | 2.48 | 0.83 | 0.48 | 0.33 | 0.17 | 0.13 | 0.12 |
| 62 | 3.6 | 3.25 | 1.03 | 0.65 | 0.46 | 0.2 | 0.15 | 0.15 |
| 123 | 5.83 | 5.01 | 1.69 | 0.96 | 0.67 | 0.32 | 0.25 | 0.26 |
| 242 | 11.22 | 8.64 | 2.69 | 1.9 | 1.04 | 0.45 | 0.35 | 0.34 |
| 470 | 12.46 | 10.58 | 4.58 | 2 | 1.27 | 0.63 | 0.50 | 0.49 |

Table 9. Typical Resolution (Bits) vs. Gain and Output Update Rate for the AD7793 Using the Internal Reference

| Update Rate (Hz) | Gain of 1 | Gain of 2 | Gain of 4 | Gain of 8 | Gain of 16 | Gain of 32 | Gain of 64 | Gain of 128 |
|---|---|---|---|---|---|---|---|---|
| 4.17 | 21.5 (19) | 20.5 (18) | 21 (18.5) | 20.5 (18) | 20 (17.5) | 20 (17.5) | 20 (17.5) | 19 (16.5) |
| 8.33 | 21 (18.5) | 20 (17.5) | 20.5 (18) | 20 (17.5) | 20 (17.5) | 20 (17.5) | 19 (16.5) | 18 (15.5) |
| 16.7 | 20 (17.5) | 19.5 (17) | 20 (17.5) | 19.5 (17) | 19 (16.5) | 19.5 (17) | 18.5 (16) | 17.5 (15) |
| 33.2 | 19.5 (17) | 19 (16.5) | 19.5 (17) | 19 (16.5) | 19 (16.5) | 18.5 (16) | 18 (15.5) | 17 (14.5) |
| 62 | 19.5 (17) | 18.5 (16) | 19 (16.5) | 19 (16.5) | 18.5 (16) | 18.5 (16) | 18 (15.5) | 17 (14.5) |
| 123 | 18.5 (16) | 18 (15.5) | 18.5 (16) | 18 (15.5) | 17.5 (15) | 18 (15.5) | 17 (14.5) | 16 (13.5) |
| 242 | 17.5 (15) | 17 (14.5) | 17.5 (15) | 17 (14.5) | 17 (14.5) | 17.5 (15) | 16.5 (14) | 15.5 (13) |
| 470 | 17.5 (15) | 17 (14.5) | 17 (14.5) | 17 (14.5) | 17 (14.5) | 17 (14.5) | 16 (13.5) | 15 (12.5) |

Table 10. Typical Resolution (Bits) vs. Gain and Output Update Rate for the AD7792 Using the Internal Reference

| Update Rate (Hz) | Gain of 1 | Gain of 2 | Gain of 4 | Gain of 8 | Gain of 16 | Gain of 32 | Gain of 64 | Gain of 128 |
|---|---|---|---|---|---|---|---|---|
| 4.17 | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) |
| 8.33 | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (15.5) |
| 16.7 | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (15) |
| 33.2 | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (15.5) | 16 (14.5) |
| 62 | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (15.5) | 16 (14.5) |
| 123 | 16 (16) | 16 (15.5) | 16 (16) | 16 (15.5) | 16 (15) | 16 (15.5) | 16 (14.5) | 15.5 (13.5) |
| 242 | 16 (15) | 16 (14.5) | 16 (15) | 16 (14.5) | 16 (14.5) | 16 (15) | 16 (14) | 15 (13) |
| 470 | 16 (15) | 16 (14.5) | 16 (14.5) | 16 (14.5) | 16 (14.5) | 16 (14.5) | 15.5 (13.5) | 14.5 (12.5) |

## TYPICAL PERFORMANCE CHARACTERISTICS

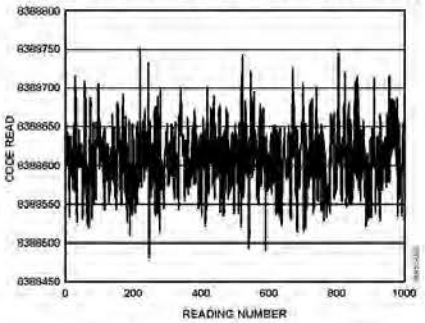



Figure 6. Typical Noise Plot (Internal Reference, Gain = 64, Update Rate = 16.7 Hz) for AD7793

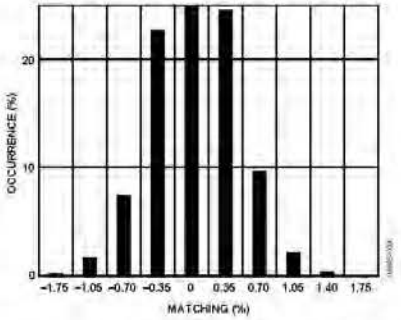



Figure 9. Excitation Current Matching (1 mA) at Ambient Temperature

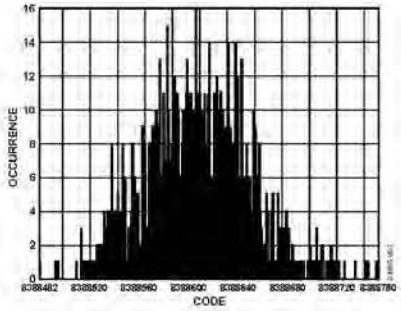



Figure 7. Noise Distribution Histogram for AD7793 (Internal Reference, Gain = 64, Update Rate = 16.7 Hz)

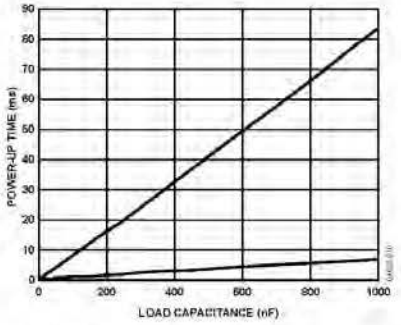



Figure 10. Bias Voltage Generator Power-Up Time vs. Load Capacitance

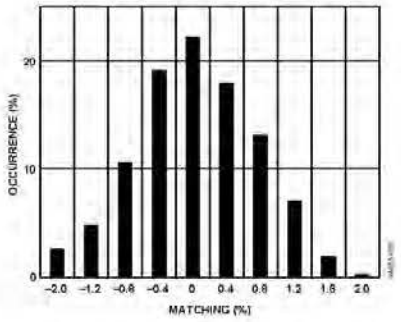



Figure 8. Excitation Current Matching (210 µA) at Ambient Temperature

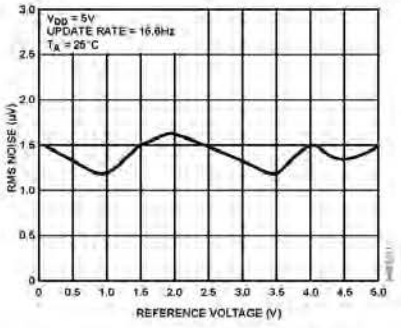



Figure 11. RMS Noise vs. Reference Voltage (Gain = 1)

# ON-CHIP REGISTERS

The ADC is controlled and configured via a number of on-chip registers, which are described on the following pages. In the following descriptions, *set* implies a Logic 1 state and *cleared* implies a Logic 0 state, unless otherwise stated.

## COMMUNICATIONS REGISTER

***RS2, RS1, RS0 = 0, 0, 0***

The communications register is an 8-bit write-only register. All communications to the part must start with a write operation to the communications register. The data written to the communications register determines whether the next operation is a read or write operation, and to which register this operation takes place. For read or write operations, once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the communications register. This is the default state of the interface and, on power-up or after a reset, the ADC is in this default state waiting for a write operation to the communications register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high returns the ADC to this default state by resetting the entire part. Table 11 outlines the bit designations for the communications register. CR0 through CR7 indicate the bit location, CR denoting the bits are in the communications register. CR7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

| CR7 | CR6 | CR5 | CR4 | CR3 | CR2 | CR1 | CR0 |
|---|---|---|---|---|---|---|---|
| $\overline{WEN}$(0) | R/$\overline{W}$(0) | RS2(0) | RS1(0) | RS0(0) | CREAD(0) | 0(0) | 0(0) |

Table 11. Communications Register Bit Designations

| Bit Location | Bit Name | Description |
|---|---|---|
| CR7 | $\overline{WEN}$ | Write Enable Bit. A 0 must be written to this bit so that the write to the communications register actually occurs. If a 1 is the first bit written, the part does not clock on to subsequent bits in the register. It stays at this bit location until a 0 is written to this bit. Once a 0 is written to the $\overline{WEN}$ bit, the next seven bits are loaded to the communications register. |
| CR6 | R/$\overline{W}$ | A 0 in this bit location indicates that the next operation is a write to a specified register. A 1 in this position indicates that the next operation is a read from the designated register. |
| CR5 to CR3 | RS2 to RS0 | Register Address Bits. These address bits are used to select which of the ADC's registers are being selected during this serial interface communication. See Table 12. |
| CR2 | CREAD | Continuous Read of the Data Register. When this bit is set to 1 (and the data register is selected), the serial interface is configured so that the data register can be continuously read. For example, the contents of the data register are placed on the DOUT pin automatically when the SCLK pulses are applied after the $\overline{RDY}$ pin goes low to indicate that a conversion is complete. The communications register does not have to be written to for data reads. To enable continuous read mode, the instruction 01011100 must be written to the communications register. To exit the continuous read mode, the instruction 01011000 must be written to the communications register while the $\overline{RDY}$ pin is low. While in continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit continuous read mode. Additionally, a reset occurs if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device. |
| CR1 to CR0 | 0 | These bits must be programmed to Logic 0 for correct operation. |

Table 12. Register Selection

| RS2 | RS1 | RS0 | Register | Register Size |
|---|---|---|---|---|
| 0 | 0 | 0 | Communications Register During a Write Operation | 8-bit |
| 0 | 0 | 0 | Status Register During a Read Operation | 8-bit |
| 0 | 0 | 1 | Mode Register | 16-bit |
| 0 | 1 | 0 | Configuration Register | 16-bit |
| 0 | 1 | 1 | Data Register | 16-/24-bit |
| 1 | 0 | 0 | ID Register | 8-bit |
| 1 | 0 | 1 | IO Register | 8-bit |
| 1 | 1 | 0 | Offset Register | 16-bit (AD7792)/24-bit (AD7793) |
| 1 | 1 | 1 | Full-Scale Register | 16-bit (AD7792)/24-bit (AD7793) |

## STATUS REGISTER

***RS2, RS1, RS0 = 0, 0, 0; Power-On/Reset = 0x80 (AD7792)/0x88 (AD7793)***

The status register is an 8-bit read-only register. To access the ADC status register, the user must write to the communications register, select the next operation to be a read, and load Bit RS2, Bit RS1, and Bit RS0 with 0. Table 13 outlines the bit designations for the status register. SR0 through SR7 indicate the bit locations, and SR denotes that the bits are in the status register. SR7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

| SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 |
|---|---|---|---|---|---|---|---|
| $\overline{RDY}$(1) | ERR(0) | 0(0) | 0(0) | 0/1 | CH2(0) | CH1(0) | CH0(0) |

Table 13. Status Register Bit Designations

| Bit Location | Bit Name | Description |
|---|---|---|
| SR7 | $\overline{RDY}$ | Ready Bit for ADC. Cleared when data is written to the ADC data register. The $\overline{RDY}$ bit is set automatically after the ADC data register has been read or a period of time before the data register is updated with a new conversion result to indicate to the user not to read the conversion data. It is also set when the part is placed in power-down mode. The end of a conversion is indicated by the DOUT/$\overline{RDY}$ pin also. This pin can be used as an alternative to the status register for monitoring the ADC for conversion data. |
| SR6 | ERR | ADC Error Bit. This bit is written to at the same time as the $\overline{RDY}$ bit. Set to indicate that the result written to the ADC data register has been clamped to all 0s or all 1s. Error sources include overrange and underrange. Cleared by a write operation to start a conversion. |
| SR5 to SR4 | 0 | These bits are automatically cleared. |
| SR3 | 0/1 | This bit is automatically cleared on the AD7792 and is automatically set on the AD7793. |
| SR2 to SR0 | CH2 to CH0 | These bits indicate which channel is being converted by the ADC. |

## MODE REGISTER

***RS2, RS1, RS0 = 0, 0, 1; Power-On/Reset = 0x000A***

The mode register is a 16-bit register from which data can be read or to which data can be written. This register is used to select the operating mode, update rate, and clock source. Table 14 outlines the bit designations for the mode register. MR0 through MR15 indicate the bit locations, MR denoting the bits are in the mode register. MR15 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit. Any write to the setup register resets the modulator and filter and sets the $\overline{RDY}$ bit.

| MR15 | MR14 | MR13 | MR12 | MR11 | MR10 | MR9 | MR8 |
|---|---|---|---|---|---|---|---|
| MD2(0) | MD1(0) | MD0(0) | 0(0) | 0(0) | 0(0) | 0(0) | 0(0) |
| **MR7** | **MR6** | **MR5** | **MR4** | **MR3** | **MR2** | **MR1** | **MR0** |
| CLK1(0) | CLK0(0) | 0(0) | 0(0) | FS3(1) | FS2(0) | FS1(1) | FS0(0) |

Table 14. Mode Register Bit Designations

| Bit Location | Bit Name | Description | | |
|---|---|---|---|---|
| MR15 to MR13 | MD2 to MD0 | Mode Select Bits. These bits select the operational mode of the AD7792/AD7793 (see Table 15). | | |
| MR12 to MR8 | 0 | These bits must be programmed with a Logic 0 for correct operation. | | |
| MR7 to MR6 | CLK1 to CLK0 | These bits are used to select the clock source for the AD7792/AD7793. Either an on-chip 64 kHz clock can be used, or an external clock can be used. The ability to override using an external clock allows several AD7792/AD7793 devices to be synchronized. In addition, 50 Hz/60 Hz is improved when an accurate external clock drives the AD7792/AD7793. | | |
| | | **CLK1** | **CLK0** | **ADC Clock Source** |
| | | 0 | 0 | Internal 64 kHz Clock. Internal clock is not available at the CLK pin. |
| | | 0 | 1 | Internal 64 kHz Clock. This clock is made available at the CLK pin. |
| | | 1 | 0 | External 64 kHz Clock Used. An external clock gives better 50 Hz/60 Hz rejection. See specifications for external clock. |
| | | 1 | 1 | External Clock Used. The external clock is divided by 2 within the AD7792/AD7793. |
| MR5 to MR4 | 0 | These bits must be programmed with a Logic 0 for correct operation. | | |
| MR3 to MR0 | FS3 to FS0 | Filter Update Rate Select Bits (see Table 16). | | |

Table 15. Operating Modes

| MD2 | MD1 | MD0 | Mode |
|---|---|---|---|
| 0 | 0 | 0 | Continuous Conversion Mode (Default).<br>In continuous conversion mode, the ADC continuously performs conversions and places the result in the data register. RDY goes low when a conversion is complete. The user can read these conversions by placing the device in continuous read mode, whereby the conversions are automatically placed on the DOUT line when SCLK pulses are applied. Alternatively, the user can instruct the ADC to output the conversion by writing to the communications register. After power-on, a channel change, or a write to the mode, configuration, or IO registers, the first conversion is available after a period of $2/f_{ADC}$. Subsequent conversions are available at a frequency of $f_{ADC}$. |
| 0 | 0 | 1 | Single Conversion Mode.<br>When single conversion mode is selected, the ADC powers up and performs a single conversion. The oscillator requires 1 ms to power up and settle. The ADC then performs the conversion, which takes a time of $2/f_{ADC}$. The conversion result is placed in the data register, RDY goes low, and the ADC returns to power-down mode. The conversion remains in the data register, and RDY remains active low until the data is read or another conversion is performed. |
| 0 | 1 | 0 | Idle Mode.<br>In idle mode, the ADC filter and modulator are held in a reset state, although the modulator clocks are still provided. |
| 0 | 1 | 1 | Power-Down Mode.<br>In power-down mode, all the AD7792/AD7793 circuitry is powered down, including the current sources, burnout currents, bias voltage generator, and CLKOUT circuitry. |
| 1 | 0 | 0 | Internal Zero-Scale Calibration.<br>An internal short is automatically connected to the enabled channel. A calibration takes 2 conversion cycles to complete. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel. |
| 1 | 0 | 1 | Internal Full-Scale Calibration.<br>A full-scale input voltage is automatically connected to the selected analog input for this calibration.<br>When the gain equals 1, a calibration takes 2 conversion cycles to complete. For higher gains, 4 conversion cycles are required to perform the full-scale calibration.<br>RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel.<br>Internal full-scale calibrations cannot be performed when the gain equals 128. With this gain setting, a system full-scale calibration can be performed.<br>A full-scale calibration is required each time the gain of a channel is changed to minimize the full-scale error. |
| 1 | 1 | 0 | System Zero-Scale Calibration.<br>User should connect the system zero-scale input to the channel input pins as selected by the CH2 to CH0 bits. A system offset calibration takes 2 conversion cycles to complete. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel. |
| 1 | 1 | 1 | System Full-Scale Calibration.<br>User should connect the system full-scale input to the channel input pins as selected by the CH2 to CH0 bits.<br>A calibration takes 2 conversion cycles to complete. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel.<br>A full-scale calibration is required each time the gain of a channel is changed. |

Table 16. Update Rates Available

| FS3 | FS2 | FS1 | FS0 | $f_{ADC}$ (Hz) | $t_{SETTLE}$ (ms) | Rejection @ 50 Hz/60 Hz (Internal Clock) |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | x | x | |
| 0 | 0 | 0 | 1 | 470 | 4 | |
| 0 | 0 | 1 | 0 | 242 | 8 | |
| 0 | 0 | 1 | 1 | 123 | 16 | |
| 0 | 1 | 0 | 0 | 62 | 32 | |
| 0 | 1 | 0 | 1 | 50 | 40 | |
| 0 | 1 | 1 | 0 | 39 | 48 | |
| 0 | 1 | 1 | 1 | 33.2 | 60 | |
| 1 | 0 | 0 | 0 | 19.6 | 101 | 90 dB (60 Hz only) |

| FS3 | FS2 | FS1 | FS0 | $f_{ADC}$ (Hz) | $t_{SETTLE}$ (ms) | Rejection @ 50 Hz/60 Hz (Internal Clock) |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 16.7 | 120 | 80 dB (50 Hz only) |
| 1 | 0 | 1 | 0 | 16.7 | 120 | 65 dB (50 Hz and 60 Hz) |
| 1 | 0 | 1 | 1 | 12.5 | 160 | 66 dB (50 Hz and 60 Hz) |
| 1 | 1 | 0 | 0 | 10 | 200 | 69 dB (50 Hz and 60 Hz) |
| 1 | 1 | 0 | 1 | 8.33 | 240 | 70 dB (50 Hz and 60 Hz) |
| 1 | 1 | 1 | 0 | 6.25 | 320 | 72 dB (50 Hz and 60 Hz) |
| 1 | 1 | 1 | 1 | 4.17 | 480 | 74 dB (50 Hz and 60 Hz) |

## CONFIGURATION REGISTER

***RS2, RS1, RS0 = 0, 1, 0; Power-On/Reset = 0x0710***

The configuration register is a 16-bit register from which data can be read or to which data can be written. This register is used to configure the ADC for unipolar or bipolar mode, enable or disable the buffer, enable or disable the burnout currents, select the gain, and select the analog input channel. Table 17 outlines the bit designations for the filter register. CON0 through CON15 indicate the bit locations; CON denotes that the bits are in the configuration register. CON15 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

| CON15 | CON14 | CON13 | CON12 | CON11 | CON10 | CON9 | CON8 |
|---|---|---|---|---|---|---|---|
| VBIAS1(0) | VBIAS0(0) | BO(0) | U/$\overline{B}$(0) | BOOST(0) | G2(1) | G1(1) | G0(1) |
| **CON7** | **CON6** | **CON5** | **CON4** | **CON3** | **CON2** | **CON1** | **CON0** |
| REFSEL(0) | 0(0) | 0(0) | BUF(1) | 0(0) | CH2(0) | CH1(0) | CH0(0) |

Table 17. Configuration Register Bit Designations

| Bit Location | Bit Name | Description | | | | |
|---|---|---|---|---|---|---|
| CON15 to CON14 | VBIAS1 to VBIAS0 | Bias Voltage Generator Enable. The negative terminal of the analog inputs can be biased up to $AV_{DD}/2$. These bits are used in conjunction with the boost bit. | | | | |
| | | **VBIAS1** | **VBIAS0** | **Bias Voltage** | | |
| | | 0 | 0 | Bias voltage generator disabled | | |
| | | 0 | 1 | Bias voltage connected to AIN1(−) | | |
| | | 1 | 0 | Bias voltage connected to AIN2(−) | | |
| | | 1 | 1 | Reserved | | |
| CON13 | BO | Burnout Current Enable Bit. When this bit is set to 1 by the user, the 100 nA current sources in the signal path are enabled. When BO = 0, the burnout currents are disabled. The burnout currents can be enabled only when the buffer or in-amp is active. | | | | |
| CON12 | U/$\overline{B}$ | Unipolar/Bipolar Bit. Set by user to enable unipolar coding; that is, zero differential input results in 0x000000 output, and a full-scale differential input results in 0xFFFFFF output. Cleared by the user to enable bipolar coding. Negative full-scale differential input results in an output code of 0x000000, zero differential input results in an output code of 0x800000, and a positive full-scale differential input results in an output code of 0xFFFFFF. | | | | |
| CON11 | BOOST | This bit is used in conjunction with the VBIAS1 and VBIAS0 bits. When set, the current consumed by the bias voltage generator is increased. This reduces its power-up time. | | | | |
| CON10 to CON8 | G2 to G0 | Gain Select Bits.<br>Written by the user to select the ADC input range as follows: | | | | |
| | | **G2** | **G1** | **G0** | **Gain** | **ADC Input Range (2.5 V Reference)** |
| | | 0 | 0 | 0 | 1 (In-amp not used) | 2.5 V |
| | | 0 | 0 | 1 | 2 (In-amp not used) | 1.25 V |
| | | 0 | 1 | 0 | 4 | 625 mV |
| | | 0 | 1 | 1 | 8 | 312.5 mV |
| | | 1 | 0 | 0 | 16 | 156.2 mV |
| | | 1 | 0 | 1 | 32 | 78.125 mV |
| | | 1 | 1 | 0 | 64 | 39.06 mV |
| | | 1 | 1 | 1 | 128 | 19.53 mV |

| Bit Location | Bit Name | Description |
|---|---|---|
| CON7 | REFSEL | Reference Select Bit. The reference source for the ADC is selected using this bit. |
| CON6 to CON5 | 0 | These bits must be programmed with a Logic 0 for correct operation. |
| CON4 | BUF | Configures the ADC for buffered or unbuffered mode of operation. If *cleared*, the ADC operates in unbuffered mode, lowering the power consumption of the device. If *set*, the ADC operates in buffered mode, allowing the user to place source impedances on the front end without contributing gain errors to the system. The buffer can be disabled when the gain equals 1 or 2. For higher gains, the buffer is automatically enabled. With the buffer disabled, the voltage on the analog input pins can be from 30 mV below GND to 30 mV above $AV_{DD}$. When the buffer is enabled, it requires some headroom, so the voltage on any input pin must be limited to 100 mV within the power supply rails. |
| CON3 | 0 | This bit must be programmed with a Logic 0 for correct operation. |
| CON2 to CON0 | CH2 to CH0 | Channel Select Bits. Written by the user to select the active analog input channel to the ADC. |

| REFSEL | Reference Source |
|---|---|
| 0 | External Reference Applied between REFIN(+) and REFIN(–). |
| 1 | Internal Reference Selected. |

| CH2 | CH1 | CH0 | Channel | Calibration Pair |
|---|---|---|---|---|
| 0 | 0 | 0 | AIN1(+) – AIN1(–) | 0 |
| 0 | 0 | 1 | AIN2(+) – AIN2(–) | 1 |
| 0 | 1 | 0 | AIN3(+) – AIN3(–) | 2 |
| 0 | 1 | 1 | AIN1(–) – AIN1(–) | 0 |
| 1 | 0 | 0 | Reserved | |
| 1 | 0 | 1 | Reserved | |
| 1 | 1 | 0 | Temp Sensor | Automatically selects gain = 1 and internal reference |
| 1 | 1 | 1 | $AV_{DD}$ Monitor | Automatically selects gain = 1/6 and 1.17 V reference |

## DATA REGISTER

***RS2, RS1, RS0 = 0, 1, 1; Power-On/Reset = 0x0000(00)***

The conversion result from the ADC is stored in this data register. This is a read-only register. On completion of a read operation from this register, the $\overline{RDY}$ bit/pin is set.

## ID REGISTER

***RS2, RS1, RS0 = 1, 0, 0; Power-On/Reset = 0xXA (AD7792)/0xXB (AD7793)***

The identification number for the AD7792/AD7793 is stored in the ID register. This is a read-only register.

## IO REGISTER

***RS2, RS1, RS0 = 1, 0, 1; Power-On/Reset = 0x00***

The IO register is an 8-bit register from which data can be read or to which data can be written. This register is used to enable and select the value of the excitation currents. Table 18 outlines the bit designations for the IO register. IO0 through IO7 indicate the bit locations; IO denotes that the bits are in the IO register. IO7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

| IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 |
|---|---|---|---|---|---|---|---|
| 0(0) | 0(0) | 0(0) | 0(0) | IEXCDIR1(0) | IEXCDIR0(0) | IEXCEN1(0) | IEXCEN0(0) |

Table 18. IO Register Bit Designations

| Bit Location | Bit Name | Description | | |
|---|---|---|---|---|
| IO7 to IO4 | 0 | These bits must be programmed with a Logic 0 for correct operation. | | |
| IO3 to IO2 | IEXCDIR1 to IEXCDIR0 | Direction of current sources select bits. | | |
| | | **IEXCDIR1** | **IEXCDIR0** | **Current Source Direction** |
| | | 0 | 0 | Current Source IEXC1 connected to Pin IOUT1, Current Source IEXC2 connected to Pin IOUT2. |
| | | 0 | 1 | Current Source IEXC1 connected to Pin IOUT2, Current Source IEXC2 connected to Pin IOUT1. |
| | | 1 | 0 | Both current sources connected to Pin IOUT1. Permitted when the current sources are set to 10 µA or 210 µA only. |
| | | 1 | 1 | Both current sources connected to Pin IOUT2. Permitted when the current sources are set to 10 µA or 210 µA only. |
| IO1 to IO0 | IEXCEN1 to IEXCEN0 | These bits are used to enable and disable the current sources along with selecting the value of the excitation currents. | | |
| | | **IEXCEN1** | **IEXCEN0** | **Current Source Value** |
| | | 0 | 0 | Excitation Current Disabled. |
| | | 0 | 1 | 10 µA |
| | | 1 | 0 | 210 µA |
| | | 1 | 1 | 1 mA |

## OFFSET REGISTER

***RS2, RS1, RS0 = 1, 1, 0; Power-On/Reset = 0x8000 (AD7792)/0x800000 (AD7793)***

Each analog input channel has a dedicated offset register that holds the offset calibration coefficient for the channel. This register is 16 bits wide on the AD7792 and 24 bits wide on the AD7793, and its power-on/reset value is 0x8000(00). The offset register is used in conjunction with its associated full-scale register to form a register pair. The power-on reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user. The offset register is a read/write register. However, the AD7792/AD7793 must be in idle mode or power-down mode when writing to the offset register.

## FULL-SCALE REGISTER

***RS2, RS1, RS0 = 1, 1, 1; Power-On/Reset = 0x5XXX (AD7792)/0x5XXX00 (AD7793)***

The full-scale register is a 16-bit register on the AD7792 and a 24-bit register on the AD7793. The full-scale register holds the full-scale calibration coefficient for the ADC. The AD7792/AD7793 have 3 full-scale registers, each channel having a dedicated full-scale register. The full-scale registers are read/write registers; however, when writing to the full-scale registers, the ADC must be placed in power-down mode or idle mode. These registers are configured on power-on with factory-calibrated full-scale calibration coefficients, the calibration being performed at gain = 1. Therefore, every device has different default coefficients. The coefficients are different depending on whether the internal reference or an external reference is selected. The default value is automatically overwritten if an internal or system full-scale calibration is initiated by the user, or the full-scale register is written to.

# ADC CIRCUIT INFORMATION

## OVERVIEW

The AD7792/AD7793 are low power ADCs that incorporate a Σ-Δ modulator, a buffer, reference, in-amp, and an on-chip digital filter intended for the measurement of wide dynamic range, low frequency signals such as those in pressure transducers, weigh scales, and temperature measurement applications.

The part has three differential inputs that can be buffered or unbuffered. The device can be operated with the internal 1.17 V reference, or an external reference can be used. Figure 12 shows the basic connections required to operate the part.

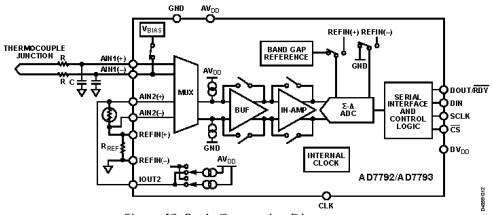



*Figure 12. Basic Connection Diagram*

The output rate of the AD7792/AD7793 ($f_{ADC}$) is user-programmable. The allowable update rates, along with their corresponding settling times, are listed in Table 16. Normal mode rejection is the major function of the digital filter. Simultaneous 50 Hz and 60 Hz rejection is optimized when the update rate equals 16.7 Hz or less as notches are placed at both 50 Hz and 60 Hz with these update rates. See Figure 14.

The AD7792/AD7793 use slightly different filter types, depending on the output update rate so that the rejection of quantization noise and device noise is optimized. When the update rate is from 4.17 Hz to 12.5 Hz, a Sinc3 filter, along with an averaging filter, is used. When the update rate is from 16.7 Hz to 39 Hz, a modified Sinc3 filter is used. This filter provides simultaneous 50 Hz/60 Hz rejection when the update rate equals 16.7 Hz. A Sinc4 filter is used when the update rate is from 50 Hz to 242 Hz. Finally, an integrate-only filter is used when the update rate equals 470 Hz.

Figure 13 to Figure 16 show the frequency response of the different filter types for several update rates.

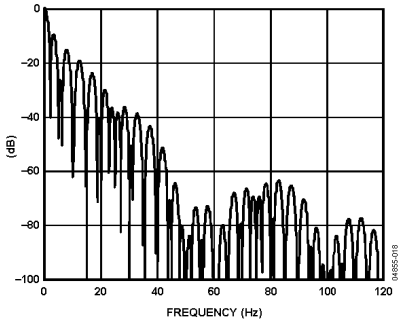



*Figure 13. Filter Profile with Update Rate = 4.17 Hz*

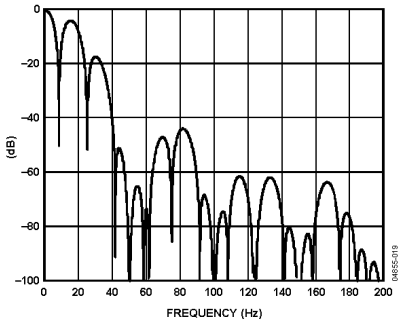



*Figure 14. Filter Profile with Update Rate = 16.7 Hz*

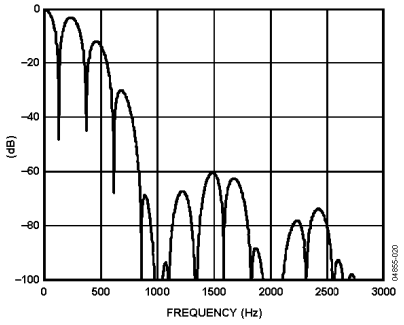



*Figure 15. Filter Profile with Update Rate = 242 Hz*

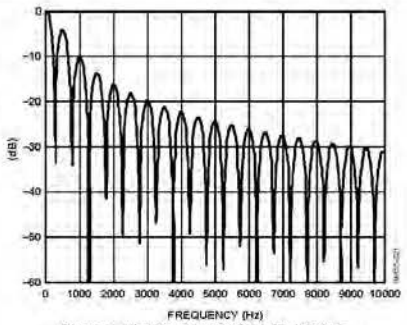



*Figure 16. Filter Response at 470 Hz Update Rate*

## DIGITAL INTERFACE

The programmable functions of the AD7792/AD7793 are controlled using a set of on-chip registers. Data is written to these registers via the serial interface of the device; read access to the on-chip registers is also provided by this interface. All communications with the device must start with a write to the communications register. After power-on or reset, the device expects a write to its communications register. The data written to this register determines whether the next operation is a read operation or a write operation and determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part begins with a write operation to the communications register followed by a write to the selected register. A read operation from any other register (except when continuous read mode is selected) starts with a write to the communications register followed by a read operation from the selected register.

The serial interfaces of the AD7792/AD7793 consist of four signals: $\overline{CS}$, DIN, SCLK, and DOUT/$\overline{RDY}$. The DIN line is used to transfer data into the on-chip registers, and DOUT/$\overline{RDY}$ is used for accessing from the on-chip registers. SCLK is the serial clock input for the device, and all data transfers (either on DIN or DOUT/$\overline{RDY}$) occur with respect to the SCLK signal. The DOUT/$\overline{RDY}$ pin operates as a data-ready signal also, the line going low when a new data-word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the data register to indicate when not to read from the device, to ensure that a data read is not attempted while the register is being updated. $\overline{CS}$ is used to select a device. It can be used to decode the AD7792/AD7793 in systems where several components are connected to the serial bus.

Figure 3 and Figure 4 show timing diagrams for interfacing to the AD7792/AD7793 with $\overline{CS}$ being used to decode the part. Figure 3 shows the timing for a read operation from the AD7792/AD7793 output shift register, and Figure 4 shows the timing for a write operation to the input shift register. It is possible to read the same word from the data register several times, even though the DOUT/$\overline{RDY}$ line returns high after the first read operation. However, care must be taken to ensure that the read operations have been completed before the next output update occurs. In continuous read mode, the data register can be read only once.

The serial interface can operate in 3-wire mode by tying $\overline{CS}$ low. In this case, the SCLK, DIN, and DOUT/$\overline{RDY}$ lines are used to communicate with the AD7792/AD7793. The end of the conversion can be monitored using the $\overline{RDY}$ bit in the status register. This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port pin. For microcontroller interfaces, it is recommended that SCLK idle high between data transfers.

The AD7792/AD7793 can be operated with $\overline{CS}$ being used as a frame synchronization signal. This scheme is useful for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{CS}$, because $\overline{CS}$ would normally occur after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers, provided the timing numbers are obeyed.

The serial interface can be reset by writing a series of 1s on the DIN input. If a Logic 1 is written to the AD7792/AD7793 line for at least 32 serial clock cycles, the serial interface is reset. This ensures that the interface can be reset to a known state if the interface gets lost due to a software error or some glitch in the system. Reset returns the interface to the state in which it is expecting a write to the communications register. This operation resets the contents of all registers to their power-on values. Following a reset, the user should allow a period of 500 µs before addressing the serial interface.

The AD7792/AD7793 can be configured to continuously convert or to perform a single conversion. See Figure 17 through Figure 19.

### Single Conversion Mode

In single conversion mode, the AD7792/AD7793 are placed in shutdown mode between conversions. When a single conversion is initiated by setting MD2, MD1, MD0 to 0, 0, 1 in the mode register, the AD7792/AD7793 power up, perform a single conversion, and then return to shutdown mode. The on-chip oscillator requires 1 ms to power up. A conversion requires a time period of 2 × $t_{ADC}$. DOUT/$\overline{RDY}$ goes low to indicate the completion of a conversion. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ goes high. If $\overline{CS}$ is low, DOUT/$\overline{RDY}$ remains high until another conversion is initiated and completed. The data register can be read several times, if required, even when DOUT/$\overline{RDY}$ has gone high.

### Continuous Conversion Mode

This is the default power-up mode. The AD7792/AD7793 continuously converts, the $\overline{RDY}$ pin in the status register going low each time a conversion is completed. If $\overline{CS}$ is low, the DOUT/ $\overline{RDY}$ line also goes low when a conversion is complete. To read a conversion, the user writes to the communications register indicating that the next operation is a read of the data register. The digital conversion is placed on the DOUT/ $\overline{RDY}$ pin as soon as SCLK pulses are applied to the ADC. DOUT/$\overline{RDY}$ returns high when the conversion is read. The user can read this register additional times, if required. However, the user must ensure that the data register is not being accessed at the completion of the next conversion, otherwise the new conversion word is lost.

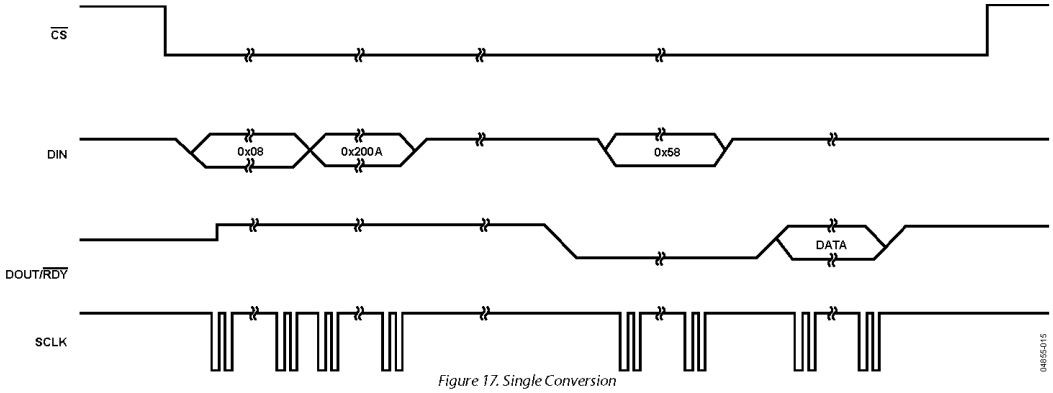



*Figure 17. Single Conversion*

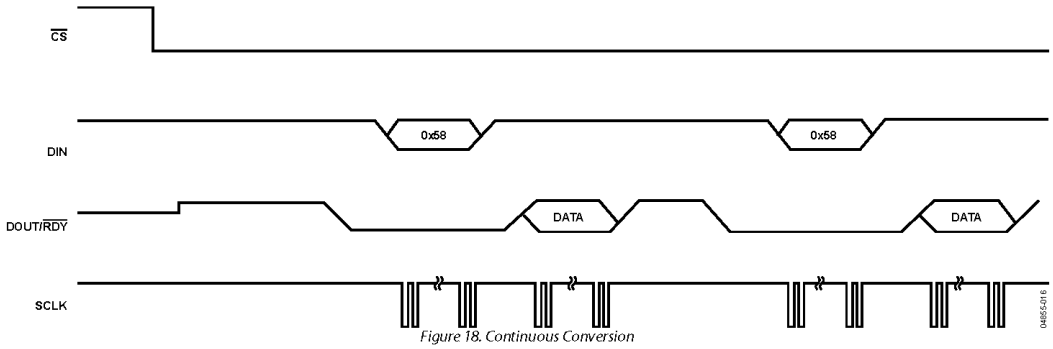



*Figure 18. Continuous Conversion*

### Continuous Read

Rather than write to the communications register each time a conversion is complete to access the data, the AD7792/AD7793 can be configured so that the conversions are placed on the DOUT/$\overline{RDY}$ line automatically. By writing 01011100 to the communications register, the user needs only to apply the appropriate number of SCLK cycles to the ADC, and the 16/24-bit word is automatically placed on the DOUT/$\overline{RDY}$ line when a conversion is complete. The ADC should be configured for continuous conversion mode.

When DOUT/$\overline{RDY}$ goes low to indicate the end of a conversion, sufficient SCLK cycles must be applied to the ADC, and the data conversion is placed on the DOUT/$\overline{RDY}$ line. When the conversion is read, DOUT/$\overline{RDY}$ returns high until the next conversion is available. In this mode, the data can be read only once. In addition, the user must ensure that the data word is read before the next conversion is complete. If the user has not read the conversion before the completion of the next conversion, or if insufficient serial clocks are applied to the AD7792/AD7793 to read the word, the serial output register is reset when the next conversion is completed, and the new conversion is placed in the output serial register.

To exit the continuous read mode, the instruction 01011000 must be written to the communications register while the DOUT/$\overline{RDY}$ pin is low. While in the continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit the continuous read mode. Additionally, a reset occurs if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is written to the device.

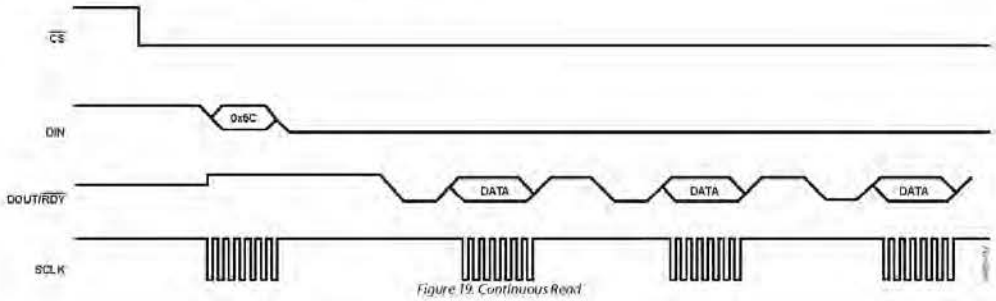



Figure 19. Continuous Read

# CIRCUIT DESCRIPTION

## ANALOG INPUT CHANNEL

The AD7792/AD7793 have three differential analog input channels. These are connected to the on-chip buffer amplifier when the device is operated in buffered mode and directly to the modulator when the device is operated in unbuffered mode. In buffered mode (the BUF bit in the mode register is set to 1), the input channel feeds into a high impedance input stage of the buffer amplifier. Therefore, the input can tolerate significant source impedances and is tailored for direct connection to external resistive-type sensors, such as strain gauges or resistance temperature detectors (RTDs).

When BUF = 0, the part is operated in unbuffered mode. This results in a higher analog input current. Note that this unbuffered input path provides a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the input pins can cause gain errors, depending on the output impedance of the source that is driving the ADC input. Table 19 shows the allowable external resistance/capacitance values for unbuffered mode such that no gain error at the 20-bit level is introduced.

**Table 19. External R-C Combination for No 20-Bit Gain Error**

| C (pF) | R (Ω) |
|---|---|
| 50 | 9 k |
| 100 | 6 k |
| 500 | 1.5 k |
| 1000 | 900 |
| 5000 | 200 |

The AD7792/AD7793 can be operated in unbuffered mode only when the gain equals 1 or 2. At higher gains, the buffer is automatically enabled. The absolute input voltage range in buffered mode is restricted to a range between GND + 100 mV and $AV_{DD}$ − 100 mV. When the gain is set to 4 or higher, the in-amp is enabled. The absolute input voltage range when the in-amp is active is restricted to a range between GND + 300 mV and $AV_{DD}$ − 1.1 V. Take care in setting up the common-mode voltage so that these limits are not exceeded to avoid degradation in linearity and noise performance.

The absolute input voltage in unbuffered mode includes the range between GND − 30 mV and $AV_{DD}$ + 30 mV as a result of being unbuffered. The negative absolute input voltage limit does allow the possibility of monitoring small true bipolar signals with respect to GND.

## INSTRUMENTATION AMPLIFIER

Amplifying the analog input signal by a gain of 1 or 2 is performed digitally within the AD7792/AD7793. However, when the gain equals 4 or higher, the output from the buffer is applied to the input of the on-chip instrumentation amplifier. This low noise in-amp means that signals of small amplitude can be gained within the AD7792/AD7793 while still maintaining excellent noise performance.

For example, when the gain is set to 64, the rms noise is 40 nV typically, which is equivalent to 21 bits effective resolution or 18.5 bits peak-to-peak resolution.

The AD7792/AD7793 can be programmed to have a gain of 1, 2, 4, 8, 16, 32, 64, and 128 using Bit G2 to Bit G0 in the configuration register. Therefore, with an external 2.5 V reference, the unipolar ranges are from 0 mV to 20 mV to 0 V to 2.5 V while the bipolar ranges are from ±20 mV to ±2.5 V. When the in-amp is active (gain ≥ 4), the common-mode voltage (AIN(+) + AIN(−))/2 must be greater than or equal to 0.5 V.

If the AD7792/AD7793 are operated with an external reference that has a value equal to $AV_{DD}$, the analog input signal must be limited to 90% of $V_{REF}$/gain when the in-amp is active, for correct operation.

## BIPOLAR/UNIPOLAR CONFIGURATION

The analog input to the AD7792/AD7793 can accept either unipolar or bipolar input voltage ranges. A bipolar input range does not imply that the part can tolerate negative voltages with respect to system GND. Unipolar and bipolar signals on the AIN(+) input are referenced to the voltage on the AIN(−) input. For example, if AIN(−) is 2.5 V, and the ADC is configured for unipolar mode and a gain of 1, the input voltage range on the AIN(+) pin is 2.5 V to 5 V.

If the ADC is configured for bipolar mode, the analog input range on the AIN(+) input is 0 V to 5 V. The bipolar/unipolar option is chosen by programming the U/$\overline{B}$ bit in the configuration register.

## DATA OUTPUT CODING

When the ADC is configured for unipolar operation, the output code is natural (straight) binary with a zero differential input voltage resulting in a code of 00...00, a midscale voltage resulting in a code of 100...000, and a full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = (2^N \times AIN \times GAIN)/V_{REF}$$

When the ADC is configured for bipolar operation, the output code is offset binary with a negative full-scale voltage resulting in a code of 000...000, a zero differential input voltage resulting in a code of 100...000, and a positive full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = 2^{N-1} \times [(AIN \times GAIN / V_{REF}) + 1]$$

where *AIN* is the analog input voltage, *GAIN* is the in-amp setting (1 to 128), and $N = 16$ for the AD7792 and $N = 24$ for the AD7793.

## BURNOUT CURRENTS

The AD7792/AD7793 contain two 100 nA constant current generators, one sourcing current from $AV_{DD}$ to AIN(+) and one sinking current from AIN(−) to GND. The currents are switched to the selected analog input pair. Both currents are either on or off, depending on the burnout current enable (BO) bit in the configuration register. These currents can be used to verify that an external transducer is still operational before attempting to take measurements on that channel. Once the burnout currents are turned on, they flow in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. If the resultant voltage measured is full scale, the user needs to verify why this is the case. A full-scale reading could mean that the front-end sensor is open circuit. It could also mean that the front-end sensor is overloaded and is justified in outputting full scale, or the reference may be absent, thus clamping the data to all 1s.

When reading all 1s from the output, the user needs to check these three cases before making a judgment. If the voltage measured is 0 V, it may indicate that the transducer has short circuited. For normal operation, these burnout currents are turned off by writing a 0 to the BO bit in the configuration register. The current sources work over the normal absolute input voltage range specifications with buffers on.

## EXCITATION CURRENTS

The AD7792/AD7793 also contain two matched, software configurable, constant current sources that can be programmed to equal 10 μA, 210 μA, or 1 mA. Both source currents from the $AV_{DD}$ are directed to either the IOUT1 or IOUT2 pin of the device. These current sources are controlled via bits in the IO register. The configuration bits enable the current sources, direct the current sources to IOUT1 or IOUT2, and select the value of the current. These current sources can be used to excite external resistive bridge or RTD sensors.

## BIAS VOLTAGE GENERATOR

A bias voltage generator is included on the AD7792/AD7793. This biases the negative terminal of the selected input channel to $AV_{DD}/2$. It is useful in thermocouple applications, because the voltage generated by the thermocouple must be biased about some dc voltage if the gain is greater than 2. This is necessary because the instrumentation amplifier requires headroom to ensure that signals close to GND or $AV_{DD}$ are converted accurately.

The bias voltage generator is controlled using the VBIAS1 and VBIAS0 bits in conjunction with the boost bit in the configuration register. The power-up time of the bias voltage generator is dependent on the load capacitance. To accommodate higher load capacitances, the AD7792/AD7793 have a boost bit. When this bit is set to 1, the current consumed by the bias voltage generator increases, so that the power-up time is considerably reduced. Figure 10 shows the power-up time when boost equals 0 and 1 for different load capacitances.

The current consumption of the AD7792/AD7793 increases by 40 μA when the bias voltage generator is enabled, and boost equals 0. With the boost function enabled, the current consumption increases by 250 μA.

## REFERENCE

The AD7792/AD7793 have an embedded 1.17 V reference that can be used to supply the ADC, or an external reference can be applied. The embedded reference is a low noise, low drift reference, the drift being 4 ppm/°C typically. For external references, the ADC has a fully differential input capability for the channel. The reference source for the AD7792/AD7793 is selected using the REFSEL bit in the configuration register. When the internal reference is selected, it is internally connected to the modulator. It is not available on the REFIN pins.

The common-mode range for these differential inputs is from GND to $AV_{DD}$. The reference input is unbuffered; therefore, excessive R-C source impedances introduce gain errors. The reference voltage REFIN (REFIN(+) − REFIN(−)) is 2.5 V nominal, but the AD7792/AD7793 are functional with reference voltages from 0.1 V to $AV_{DD}$. In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the part, the effect of the low frequency noise in the excitation source is removed because the application is ratiometric. If the AD7792/AD7793 are used in a nonratiometric application, a low noise reference should be used.

Recommended 2.5 V reference voltage sources for the AD7792/AD7793 include the ADR381 and ADR391, which are low noise, low power references. Also note that the reference inputs provide a high impedance, dynamic load. Because the input impedance of each reference input is dynamic, resistor/capacitor combinations on these inputs can cause dc gain errors, depending on the output impedance of the source that is driving the reference inputs.

Reference voltage sources like those recommended above (such as ADR391) typically have low output impedances and are, therefore, tolerant to having decoupling capacitors on REFIN(+) without introducing gain errors in the system. Deriving the reference input voltage across an external resistor means that the reference input sees a significant external source impedance. External decoupling on the REFIN pins is not recommended in this type of circuit configuration.

## RESET

The circuitry and serial interface of the AD7792/AD7793 can be reset by writing 32 consecutive 1s to the device. This resets the logic, the digital filter, and the analog modulator while all on-chip registers are reset to their default values. A reset is automatically performed on power-up. When a reset is initiated, the user must allow a period of 500 μs before accessing any of the on-chip registers. A reset is useful if the serial interface becomes asynchronous due to noise on the SCLK line.

## $AV_{DD}$ MONITOR

Along with converting external voltages, the ADC can be used to monitor the voltage on the $AV_{DD}$ pin. When Bit CH2 to Bit CH0 equal 1, the voltage on the $AV_{DD}$ pin is internally attenuated by 6, and the resultant voltage is applied to the Σ-Δ modulator using an internal 1.17 V reference for analog-to-digital conversion. This is useful, because variations in the power supply voltage can be monitored.

## CALIBRATION

The AD7792/AD7793 provide four calibration modes that can be programmed via the mode bits in the mode register. These are internal zero-scale calibration, internal full-scale calibration, system zero-scale calibration, and system full-scale calibration, which effectively reduces the offset error and full-scale error to the order of the noise. After each conversion, the ADC conversion result is scaled using the ADC calibration registers before being written to the data register. The offset calibration coefficient is subtracted from the result prior to multiplication by the full-scale coefficient.

To start a calibration, write the relevant value to the MD2 to MD0 bits in the mode register. After the calibration is complete, the contents of the corresponding calibration registers are updated, the $\overline{RDY}$ bit in the status register is set, the DOUT/$\overline{RDY}$ pin goes low (if $\overline{CS}$ is low), and the AD7792/AD7793 revert to idle mode.

During an internal zero-scale or full-scale calibration, the respective zero input and full-scale input are automatically connected internally to the ADC input pins. A system calibration, however, expects the system zero-scale and system full-scale voltages to be applied to the ADC pins before the calibration mode is initiated. In this way, external ADC errors are removed.

From an operational point of view, a calibration should be treated like another ADC conversion. A zero-scale calibration (if required) should always be performed before a full-scale calibration. System software should monitor the $\overline{RDY}$ bit in the status register or the DOUT/$\overline{RDY}$ pin to determine the end of calibration via a polling sequence or an interrupt-driven routine.

Both an internal offset calibration and a system offset calibration take two conversion cycles. An internal offset calibration is not needed, as the ADC itself removes the offset continuously.

To perform an internal full-scale calibration, a full-scale input voltage is automatically connected to the selected analog input for this calibration. When the gain equals 1, a calibration takes 2 conversion cycles to complete. For higher gains, 4 conversion cycles are required to perform the full-scale calibration. DOUT/$\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete.

The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. Internal full-scale calibrations cannot be performed when the gain equals 128. With this gain setting, a system full-scale calibration can be performed. A full-scale calibration is required each time the gain of a channel is changed to minimize the full-scale error.

An internal full-scale calibration can be performed at specified update rates only. For gains of 1, 2, and 4, an internal full-scale calibration can be performed at any update rate. However, for higher gains, internal full-scale calibrations can be performed when the update rate is less than or equal to 16.7 Hz, 33.2 Hz, and 50 Hz only. However, the full-scale error does not vary with update rate, so a calibration at one update rate is valid for all update rates (assuming the gain or reference source is not changed).

A system full-scale calibration takes 2 conversion cycles to complete, irrespective of the gain setting. A system full-scale calibration can be performed at all gains and all update rates. If system offset calibrations are being performed along with system full-scale calibrations, the offset calibration should be performed before the system full-scale calibration is initiated.

## GROUNDING AND LAYOUT

Because the analog inputs and reference inputs of the ADC are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part removes common-mode noise on these inputs. The digital filter provides rejection of broadband noise on the power supply, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD7792/AD7793 are more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7792/AD7793 is so high, and the noise levels from the AD7792/AD7793 are so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD7792/AD7793 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes because it provides the best shielding.

It is recommended that the GND pins of the AD7792/AD7793 be tied to the AGND plane of the system. In any layout, it is important to keep in mind the flow of currents in the system, ensuring that the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. Avoid forcing digital currents to flow through the AGND sections of the layout.

The ground planes of the AD7792/AD7793 should be allowed to run under the AD7792/AD7793 to prevent noise coupling. The power supply lines to the AD7792/AD7793 should use as wide a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, and signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. $AV_{DD}$ should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to GND. $DV_{DD}$ should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to the system's DGND plane, with the system's AGND to DGND connection being close to the AD7792/AD7793.

To achieve the best from these decoupling components, they should be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 µF ceramic capacitors to DGND.

# APPLICATIONS INFORMATION

The AD7792/AD7793 provide a low cost, high resolution analog-to-digital function. Because the analog-to-digital function is provided by a Σ-Δ architecture, the parts are more immune to noisy environments, making them ideal for use in sensor measurement and industrial and process control applications.

## TEMPERATURE MEASUREMENT USING A THERMOCOUPLE

Figure 20 outlines a connection from a thermocouple to the AD7792/AD7793. In a thermocouple application, the voltage generated by the thermocouple is measured with respect to an absolute reference, so the internal reference is used for this conversion. The cold junction measurement uses a ratiometric configuration, so the reference is provided externally.

Because the signal from the thermocouple is small, the AD7792/AD7793 are operated with the in-amp enabled to amplify the signal from the thermocouple. As the input channel is buffered, large decoupling capacitors can be placed on the front end to eliminate any noise pickup that may be present in the thermocouple leads. The AD7792/AD7793 have a reduced common-mode range with the in-amp enabled, so the bias voltage generator provides a common-mode voltage so that the voltage generated by the thermocouple is biased up to $AV_{DD}/2$.

The cold junction compensation is performed using a thermistor in the diagram. The on-chip excitation current supplies the thermistor. In addition, the reference voltage for the cold junction measurement is derived from a precision resistor in series with the thermistor. This allows a ratiometric measurement so that variation of the excitation current has no effect on the measurement (it is the ratio of the precision reference resistance to the thermistor resistance that is measured).

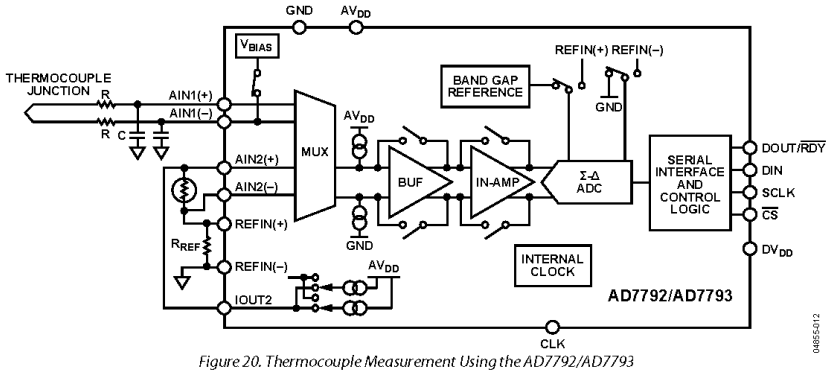



*Figure 20. Thermocouple Measurement Using the AD7792/AD7793*

## TEMPERATURE MEASUREMENT USING AN RTD

To optimize a 3-wire RTD configuration, two identically matched current sources are required. The AD7792/AD7793, which contain two well-matched current sources, are ideally suited to these applications. One possible 3-wire configuration is shown in Figure 21. In this 3-wire configuration, the lead resistances result in errors if only one current is used, as the excitation current flows through RL1, developing a voltage error between AIN1(+) and AIN1(−). In the scheme outlined, the second RTD current source is used to compensate for the error introduced by the excitation current flowing through RL1. The second RTD current flows through RL2. Assuming RL1 and RL2 are equal (the leads would normally be of the same material and of equal length), and IOUT1 and IOUT2 match, the error voltage across RL2 equals the error voltage across RL1, and no error voltage is developed between AIN1(+) and AIN1(−). Twice the voltage is developed across RL3 but, because this is a common-mode voltage, it does not introduce errors. The reference voltage for the AD7792/AD7793 is also generated using one of these matched current sources. It is developed using a precision resistor and applied to the differential reference pins of the ADC. This scheme ensures that the analog input voltage span remains ratiometric to the reference voltage. Any errors in the analog input voltage due to the temperature drift of the excitation current are compensated by the variation of the reference voltage.

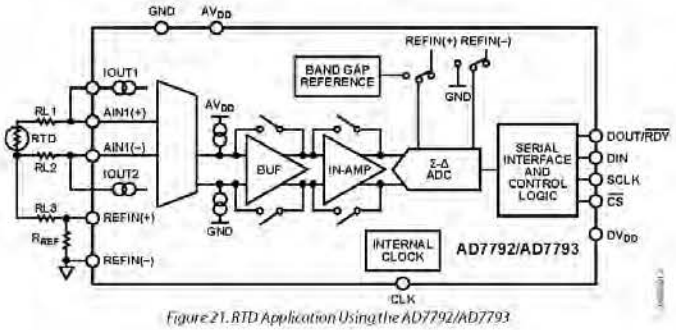



*Figure 21. RTD Application Using the AD7792/AD7793*

## OUTLINE DIMENSIONS

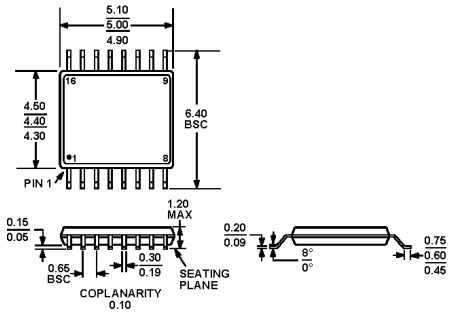



*Figure 22. 16-Lead Thin Shrink Small Outline Package [TSSOP]*
*(RU-16)*
*Dimensions shown in millimeters*

### ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD7792BRU | –40°C to +105°C | 16-Lead TSSOP | RU-16 |
| AD7792BRU-REEL | –40°C to +105°C | 16-Lead TSSOP | RU-16 |
| AD7792BRUZ[1] | –40°C to +105°C | 16-Lead TSSOP | RU-16 |
| AD7792BRUZ-REEL[1] | –40°C to +105°C | 16-Lead TSSOP | RU-16 |
| AD7793BRU | –40°C to +105°C | 16-Lead TSSOP | RU-16 |
| AD7793BRU-REEL | –40°C to +105°C | 16-Lead TSSOP | RU-16 |
| AD7793BRUZ[1] | –40°C to +105°C | 16-Lead TSSOP | RU-16 |
| AD7793BRUZ-REEL[1] | –40°C to +105°C | 16-Lead TSSOP | RU-16 |
| EVAL-AD7792EBZ[1] | | Evaluation Board | |
| EVAL-AD7793EBZ[1] | | Evaluation Board | |

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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# APPENDIX B. ADS1000 DATASHEET



## LOW-POWER, 12-Bit ANALOG-TO-DIGITAL CONVERTER with I²C™ INTERFACE

### FEATURES

- **Complete 12-Bit Data Acquisition System in a Tiny SOT-23 Package**
- **Low Current Consumption: Only 90µA**
- **Integral Nonlinearity: 1LSB Max**
- **Single-Cycle Conversion**
- **Programmable Gain Amplifier Gain = 1, 2, 4, or 8**
- **128SPS Data Rate**
- **I²C Interface with Two Available Addresses**
- **Power Supply: 2.7V to 5.5V**
- **Pin- and Software-Compatible with 16-Bit ADS1100**

### APPLICATIONS

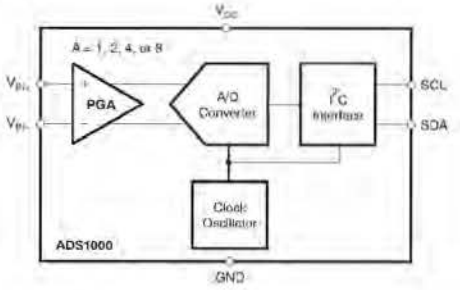
- **Voltage Monitors**
- **Battery Management**
- **Industrial Process Control**
- **Consumer Goods**
- **Temperature Measurement**

### DESCRIPTION

The ADS1000 is an I²C-compatible serial interface Analog-to-Digital (A/D) converter with differential inputs and 12 bits of resolution in a tiny SOT23-6 package. Conversions are performed ratiometrically, using the power supply as the reference voltage. The ADS1000 operates from a single power supply ranging from 2.7V to 5.5V.

The ADS1000 performs conversions at a rate of 128 samples per second (SPS). The onboard programmable gain amplifier (PGA), which offers gains of up to 8, allows smaller signals to be measured with high resolution. In single-conversion mode, the ADS1000 automatically powers down after a conversion, greatly reducing current consumption during idle periods.

The ADS1000 is designed for applications where space and power consumption are major considerations. Typical applications include portable instrumentation, consumer goods, and voltage monitoring.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this datasheet or see the TI website at www.ti.com.

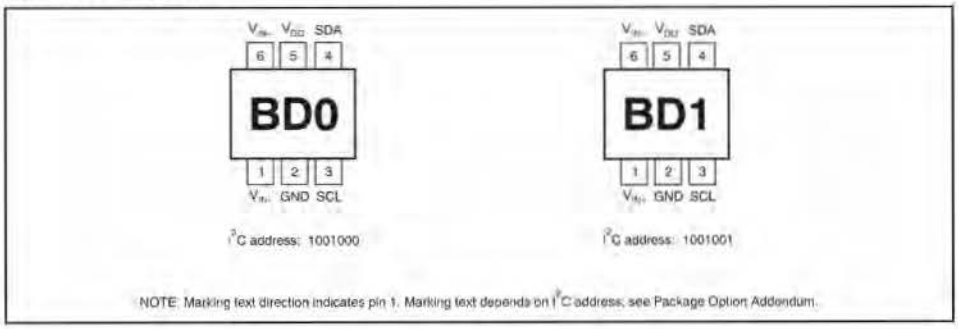
## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

| | ADS1000 | UNIT |
|---|---|---|
| $V_{DD}$ to GND | –0.3 to +6 | V |
| Input Current (Momentary) | 100 | mA |
| Input Current (Continuous) | 10 | mA |
| Voltage to GND, $V_{IN+}$, $V_{IN-}$ | –0.3 to $V_{DD}$ to +0.3 | V |
| Voltage to GND, SDA, SCL | –0.5 to +6 | V |
| Maximum Junction Temperature, $T_J$ | +150 | °C |
| Operating Temperature | –40 to +125 | °C |
| Storage Temperature | –60 to +150 | °C |
| Lead Temperature (soldering, 10s) | +300 | °C |

(1) Stresses above those listed under ***Absolute Maximum Ratings*** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## PIN CONFIGURATIONS




NOTE: Marking text direction indicates pin 1. Marking text depends on I²C address; see Package Option Addendum.

## ELECTRICAL CHARACTERISTICS

All specifications at –40°C to +85°C, $V_{DD}$ = 5V, GND = 0V, and all PGAs, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS1000 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **ANALOG INPUT** | | | | | |
| Full-Scale Input Voltage | $(V_{IN+}) - (V_{IN-})$ | | $\pm V_{DD}$/PGA(1) | | V |
| Analog Input Voltage | $V_{IN+}$, $V_{IN-}$ to GND | GND – 0.2 | | $V_{DD}$ + 0.2 | V |
| Differential Input Impedance | | | 2.4/PGA | | MΩ |
| Common-Mode Input Impedance | | | 8 | | MΩ |
| **SYSTEM PERFORMANCE** | | | | | |
| Resolution | No Missing Codes | 12 | | | Bits |
| Data Rate | | 104 | 128 | 184 | SPS |
| Integral Nonlinearity (INL) | | | ±0.1 | 1 | LSB |
| Offset Error | | | 1 | ±2 | LSB |
| Gain Error | | | 0.01 | 0.1 | % |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Level | | | | | |
| $V_{IH}$ | | 0.7 VDD | | 6 | V |
| $V_{IL}$ | | GND – 0.5 | | 0.3 $V_{DD}$ | V |
| $V_{OL}$ | $I_{OL}$ = 3mA | GND | | 0.4 | V |
| Input Leakage | | | | | |
| $I_{IH}$ | $V_{IH}$ = 5.5V | | | 10 | µA |
| $I_{IL}$ | $V_{IL}$ = GND | – 10 | | | µA |
| **POWER-SUPPLY REQUIREMENTS** | | | | | |
| Power-Supply Voltage | $V_{DD}$ | 2.7 | | 5.5 | V |
| Supply Current | Power-Down | | 0.05 | 2 | µA |
| | Active | | 90 | 150 | µA |
| Power Dissipation | | | | | µA |
| | $V_{DD}$ = 5.0V | | 450 | 750 | µW |
| | $V_{DD}$ = 3.0V | | 210 | | µW |

(1) Each input, $V_{IN+}$ and $V_{IN-}$, must meet the absolute input voltage specifications.

## TYPICAL CHARACTERISTICS

At $T_A$ = 25°C and $V_{DD}$ = 5V, unless otherwise indicated.

SUPPLY CURRENT vs TEMPERATURE

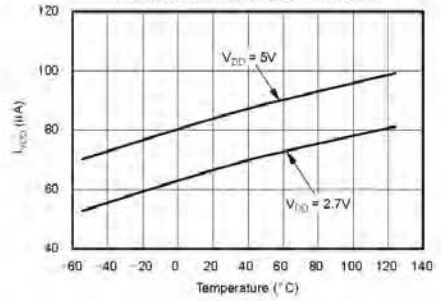



Figure 1.

SUPPLY CURRENT vs I²C BUS FREQUENCY

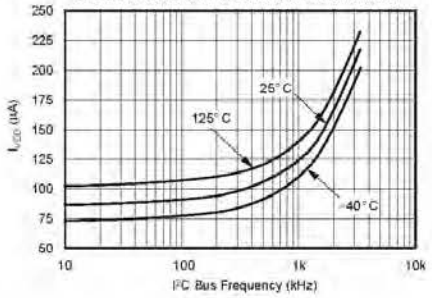



Figure 2.

OFFSET ERROR vs TEMPERATURE

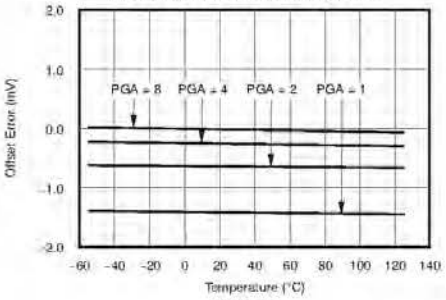



Figure 3.

GAIN ERROR vs TEMPERATURE

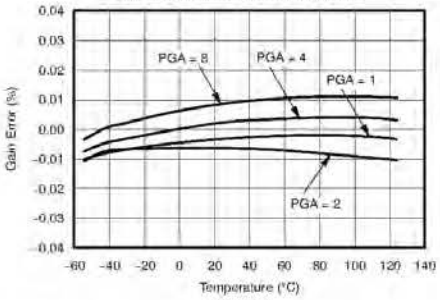



Figure 4.

DATA RATE vs TEMPERATURE

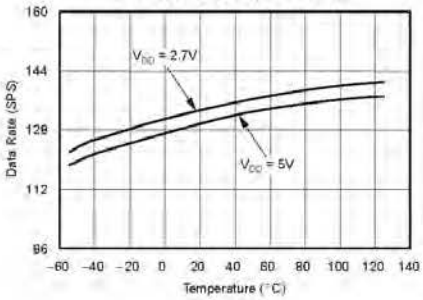



Figure 5.

## THEORY OF OPERATION

The ADS1000 is a fully differential, 12-bit A/D converter. The ADS1000 allows users to obtain precise measurements with a minimum of effort, and the device is extremely easy to design with and configure.

The ADS1000 consists of an A/D converter core with adjustable gain, a clock generator, and an $I^2C$ interface. Each of these blocks are described in detail in the sections that follow.

### ANALOG-TO-DIGITAL CONVERTER

The ADS1000 uses a switched-capacitor input stage. To external circuitry, it looks roughly like a resistance. The resistance value depends on the capacitor values and the rate at which they are switched. The switching clock is generated by the onboard clock generator, so its frequency, nominally 275kHz, is dependent on supply voltage and temperature. The capacitor values depend on the PGA setting.

The common-mode and differential input impedances are different. For a gain setting of PGA, the differential input impedance is typically 2.4MΩ/PGA.

The common-mode impedance is typically 8MΩ.

### OUTPUT CODE CALCULATION

The ADS1000 outputs codes in binary two's complement format. The output code is confined to the range of numbers –2048 to 2047, and is given by:

$$\text{Output Code} = 2048(\text{PGA})\left(\frac{V_{IN(+)} - V_{IN(-)}}{V_{(REF)}}\right)$$

### CLOCK GENERATOR

The ADS1000 features an onboard clock generator. The Typical Characteristics show variations in data rate over supply voltage and temperature. It is not possible to operate the ADS1000 with an external clock.

### USING THE ADS1000

#### OPERATING MODES

The ADS1000 operates in one of two modes: continuous conversion and single conversion.

In continuous conversion mode, the ADS1000 continuously performs conversions. Once a conversion has been completed, the ADS1000 places the result in the output register, and immediately begins another conversion. When the ADS1000 is in continuous conversion mode, the ST/BSY bit in the configuration register always reads '1'.

In single conversion mode, the ADS1000 waits until the ST/BSY bit in the conversion register is set to '1'. When this happens, the ADS1000 powers up and performs a single conversion. After the conversion completes, the ADS1000 places the result in the output register, resets the ST/BSY bit to '0' and powers down. Writing a '1' to ST/BSY while a conversion is in progress has no effect.

When switching from continuous conversion mode to single conversion mode, the ADS1000 will complete the current conversion, reset the ST/BSY bit to '0' and power-down the device.

#### RESET AND POWER-UP

When the ADS1000 powers up, it automatically performs a reset. As part of the reset, the ADS1000 sets all of the bits in the configuration register to their respective default settings.

The ADS1000 responds to the $I^2C$ General Call Reset command. When the ADS1000 receives a General Call Reset, it performs an internal reset, exactly as though it had just been powered on.

#### $I^2C$ INTERFACE

The ADS1000 communicates through an $I^2C$ (Inter-Integrated Circuit) interface. The $I^2C$ interface is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the $I^2C$ bus only drive the bus lines low, by connecting them to ground; they never drive the bus lines high. Instead, the bus wires are pulled high by pull-up resistors, so the bus wires are high when no device is driving them low. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the $I^2C$ bus always takes place between two devices, one acting as the master and the other acting as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some $I^2C$ devices can act as masters or slaves, but the ADS1000 can only act as a slave device.

An $I^2C$ bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data is transmitted across the $I^2C$ bus in groups of eight bits. To send a bit on the $I^2C$ bus, the SDA line is driven to the bit level while SCL is low (a Low on SDA indicates the bit is '0'; a High indicates the bit is '1'). Once the SDA line has settled, the SCL line is brought high, then low. This pulse on SCL clocks the SDA bit into the receiver shift register.

The $I^2C$ bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line. The master always drives the clock line. The ADS1000 never drives SCL, because it cannot act as a master. On the ADS1000, SCL is an input only.

Most of the time the bus is idle, no communication takes place, and both lines are high. When communication takes place, the bus is active. Only master devices can start a communication. They do this by causing a start condition on the bus. Normally, the data line is only allowed to change state while the clock line is low. If the data line changes state while the clock line is high, it is either a *start* condition or its counterpart, a *stop* condition. A start condition is when the clock line is high and the data line goes from high to low. A stop condition is when the clock line is high and the data line goes from low to high.

After the master issues a start condition, it sends a byte that indicates with which slave device it wants to communicate. This byte is called the *address byte*. Each device on an $I^2C$ bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the $I^2C$ specification for details.) The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the $I^2C$ bus, whether it be address or data, is acknowledged with an *acknowledge* bit. When a master has finished sending a byte, eight data bits, to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA low. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA low to acknowledge to the slave that it has finished reading the byte. It then sends a clock pulse to clock the bit. (Remember that the master always drives the clock line.)

A *not-acknowledge* is performed by simply leaving SDA high during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it will receive a not-acknowledge because no device is present at that address to pull the line low.

When a master has finished communicating with a slave, it may issue a stop condition. When a stop condition is issued, the bus becomes idle again. A master may also issue another start condition. When a start condition is issued while the bus is active, it is called a *repeated start condition*.

A timing diagram for an ADS1000 $I^2C$ transaction is shown in Figure 6. Table 1 gives the parameters for this diagram.

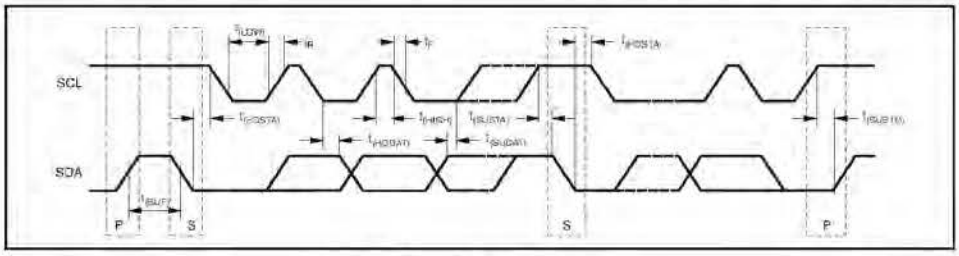



**Figure 6. I²C Timing Diagram**

**Table 1. Timing Diagram Definitions**

| PARAMETER | | FAST MODE | | HIGH-SPEED MODE | | UNITS |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| SCLK Operating Frequency | $f_{(SCLK)}$ | | 0.4 | | 3.4 | MHz |
| Bus Free Time Between STOP and START Condition | $t_{(BUF)}$ | 600 | | 160 | | ns |
| Hold Time After Repeated START Condition. After this period, the first clock is generated. | $t_{(HDSTA)}$ | 600 | | 160 | | ns |
| Repeated START Condition Setup Time | $t_{(SUSTA)}$ | 600 | | 160 | | ns |
| STOP Condition Setup Time | $t_{(SUSTO)}$ | 600 | | 160 | | ns |
| Data Hold Time | $t_{(HDDAT)}$ | 0 | | 0 | | ns |
| Data Setup Time | $t_{(SUDAT)}$ | 100 | | 10 | | ns |
| SCLK Clock Low Period | $t_{(LOW)}$ | 1300 | | 160 | | ns |
| SCLK Clock High Period | $t_{(HIGH)}$ | 600 | | 60 | | ns |
| Clock/Data Fall Time | $t_f$ | | 300 | | 160 | ns |
| Clock/Data Rise Time | $t_r$ | | 300 | | 160 | ns |

### ADS1000 I²C ADDRESSES

The ADS1000 I²C address is either 1001000 or 1001001, set at the factory. The address is identified with an A0 or an A1 within the orderable name.

The two different I²C variants are also marked differently. Devices with an I²C address of 1001000 have packages marked **BD0**, while devices with an I²C address of 1001001 are marked with **BD1**. See the Package/Ordering Information Table for a complete listing of the ADS1000 I²C addresses and tape and reel size.

### I²C GENERAL CALL

The ADS1000 responds to General Call Reset, which is an address byte of 00h followed by a data byte of 06h. The ADS1000 acknowledges both bytes.

On receiving a General Call Reset, the ADS1000 performs a full internal reset, just as though it had been powered off and then on. If a conversion is in process, it is interrupted; the output register is set to zero, and the configuration register returns to its default setting.

The ADS1000 always acknowledges the General Call address byte of 00h, but it does not acknowledge any General Call data bytes other than 04h or 06h.

### I²C DATA RATES

The I²C bus operates in one of three speed modes: *Standard*, which allows a clock frequency of up to 100kHz; *Fast*, which allows a clock frequency of up to 400kHz; and *High-speed* mode (also called Hs mode), which allows a clock frequency of up to 3.4MHz. The ADS1000 is fully compatible with all three modes.

No special action needs to be taken to use the ADS1000 in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001XXX following the start condition, where the ***XXX*** bits are unique to the Hs-capable master. This byte is called the *Hs master code*. (Note that this is different from normal address bytes; the low bit does not indicate read/write status.) The ADS1000 will not acknowledge this byte; the I²C specification prohibits acknowledgment of the Hs master code. On receiving a master code, the ADS1000 will switch on its High-speed mode filters, and will communicate at up to 3.4MHz. The ADS1000 switches out of Hs mode with the next stop condition.

For more information on High-speed mode, consult the I²C specification.

### REGISTERS

The ADS1000 has two registers that are accessible via its I²C port. The output register contains the result of the last conversion; the configuration register allows users to change the ADS1000 operating mode and query the status of the device.

### OUTPUT REGISTER

The 16-bit output register contains the result of the last conversion in binary two's complement format. Since the port yields 12 bits of data, the ADS1000 outputs right-justified and sign-extended codes. This output format makes it possible to perform averaging using a 16-bit accumulator.

Following reset or power-up, the output register is cleared to '0'; it remains zero until the first conversion is completed. Therefore, if a user reads the ADS1000 just after reset or power-up, the output register will read '0'.

The output register format is shown in Table 2.

**Table 2. OUTPUT REGISTER**

| BIT | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NAME | D15(1) | D14(1) | D13(1) | D12(1) | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

(1) D15–D12 are sign extensions of 12-bit data.

## CONFIGURATION REGISTER

A user controls the ADS1000 operating mode and PGA settings via the 8-bit configuration register. The configuration register format is shown in Table 3. The default setting is 80H.

**Table 3. CONFIGURATION REGISTER**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ST/BSY | 0 | 0 | SC | 0 | 0 | PGA1 | PGA0 |

### Bit 7: ST/BSY

The meaning of the ST/BSY bit depends on whether it is being written to or read from.

In single conversion mode, writing a '1' to the ST/BSY bit causes a conversion to start, and writing a '0' has no effect. In continuous conversion mode, the ADS1000 ignores the value written to ST/BSY.

When read in single conversion mode, ST/BSY indicates whether the A/D converter is busy taking a conversion. If ST/BSY is read as '1', the A/D converter is busy, and a conversion is taking place; if '0', no conversion is taking place, and the result of the last conversion is available in the output register.

In continuous mode, ST/BSY is always read as '1'.

### Bits 6 - 5: Reserved

Bits 6 and 5 must be set to zero.

### Bit 4: SC

SC controls whether the ADS1000 is in continuous conversion or single conversion mode. When SC is '1', the ADS1000 is in single conversion mode; when SC is '0', the ADS1000 is in continuous conversion mode. The default setting is '0'.

### Bits 3 - 2: Reserved

Bits 3 and 2 must be set to zero.

### Bits 1 - 0: PGA

Bits 1 and 0 control the ADS1000 gain setting; see Table 4.

**Table 4. PGA Bits**

| PGA1 | PGA0 | GAIN |
|---|---|---|
| 0(1) | 0(1) | 1(1) |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 8 |

(1) Default setting.

## READING FROM THE ADS1000

A user can read the output register and the contents of the configuration register from the ADS1000. To do this, address the ADS1000 for reading, and read three bytes from the device. The first two bytes are the output register contents; the third byte is the configuration register contents.

A user does not always have to read three bytes from the ADS1000. If only the contents of the output register are needed, read only two bytes.

Reading more than three bytes from the ADS1000 has no effect. All of the bytes beginning with the fourth byte will be FFh. See Figure 7 for a timing diagram of an ADS1000 read operation.

## WRITING TO THE ADS1000

A user can write new contents into the configuration register (the contents of the output register cannot change). To do this, address the ADS1000 for writing, and write one byte to it. This byte is written into the configuration register.

Writing more than one byte to the ADS1000 has no effect. The ADS1000 ignores any bytes sent to it after the first one, and will only acknowledge the first byte. See Figure 8 for a timing diagram of an ADS1000 write operation.

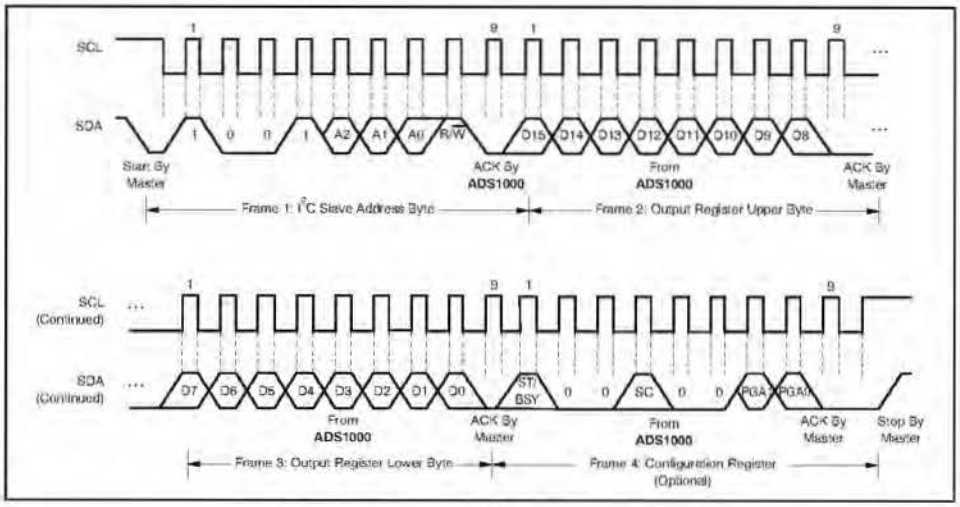



**Figure 7. Timing Diagram for Reading from the ADS1000**

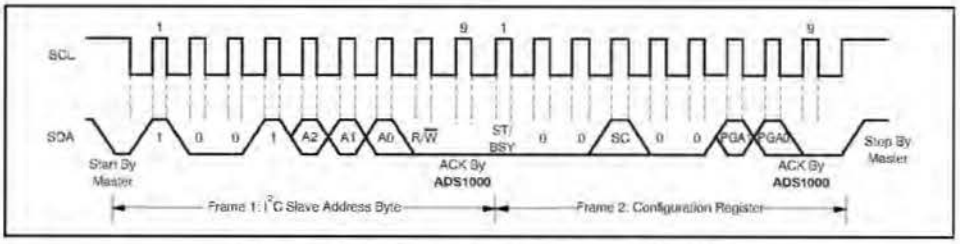



**Figure 8. Timing Diagram for Writing to the ADS1000**

## APPLICATION INFORMATION

### BASIC CONNECTIONS

For many applications, connecting the ADS1000 is extremely simple. A basic connection diagram for the ADS1000 is shown in Figure 9.

The fully differential voltage input of the ADS1000 is ideal for connection to differential sources with moderately low source impedance, such as bridge sensors and thermistors. Although the ADS1000 can read bipolar differential signals, it cannot accept negative voltages on either input. It may be helpful to think of the ADS1000 positive voltage input as noninverting, and of the negative input as inverting.

When the ADS1000 is converting, it draws current in short spikes. The 0.1µF bypass capacitor supplies the momentary bursts of extra current needed from the supply.

The ADS1000 interfaces directly to standard mode, fast mode, and high-speed mode $I^2C$ controllers. Any microcontroller $I^2C$ peripheral, including master-only and non-multiple-master $I^2C$ peripherals, will work with the ADS1000. The ADS1000 does not perform clock-stretching (that is, it never pulls the clock line low), so it is not necessary to provide for this unless other devices are on the same $I^2C$ bus.

Pull-up resistors are necessary on both the SDA and SCL lines because $I^2C$ bus drivers are open-drain. The size of these resistors depends on the bus operating speed and capacitance of the bus lines. Higher-value resistors consume less power, but increase the transition times on the bus, limiting the bus speed. Lower-value resistors allow higher speed at the expense of higher power consumption. Long bus lines have higher capacitance and require smaller pullup resistors to compensate. The resistors should not be too small; if they are, the bus drivers may not be able to pull the bus lines low.

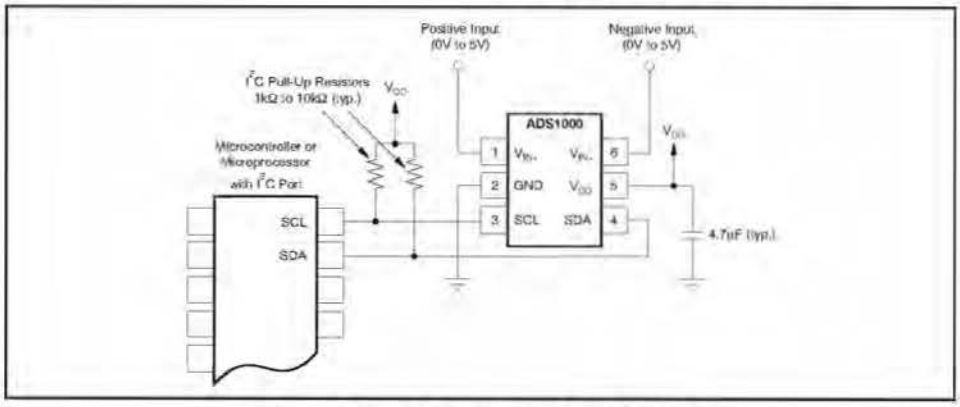



**Figure 9. Typical Connections of the ADS1000**

## CONNECTING MULTIPLE DEVICES

Connecting two ADS1000s to a single bus is almost trivial. An example showing two ADS1000s and one ADS1100 connected on a single bus is shown in Figure 10. Multiple devices can be connected to a single bus (provided that their addresses are different).

Note that only one set of pull-up resistors is needed per bus. A user might find that he or she needs to lower the pull-up resistor values slightly to compensate for the additional bus capacitance presented by multiple devices and increased line length.

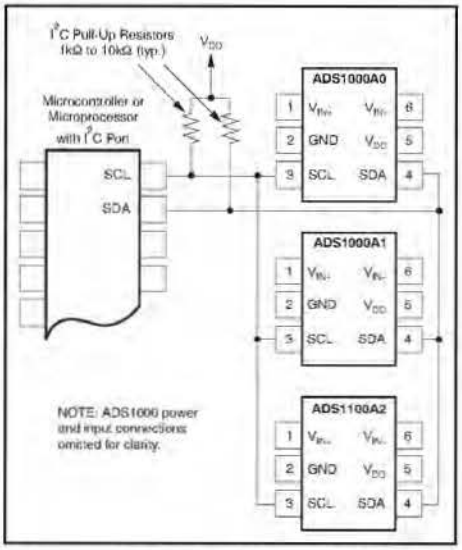



**Figure 10. Connecting Multiple ADS1000s**

## USING GPIO PORTS FOR I²C

Most microcontrollers have programmable input/output pins that can be set in software to act as inputs or outputs. If an I²C controller is not available, the ADS1000 can be connected to GPIO pins, and the I²C bus protocol simulated, or bit-banged, in software. An example of this for a single ADS1000 is shown in Figure 11.

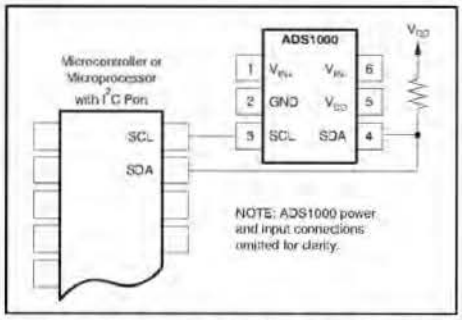



**Figure 11. Using GPIO with a Single ADS1000**

Bit-banging I²C with GPIO pins can be done by setting the GPIO line to zero and toggling it between input and output modes to apply the proper bus states. To drive the line low, the pin is set to output a '0'; to let the line go high, the pin is set to input. When the pin is set to input, the state of the pin can be read; if another device is pulling the line low, this device will read as a '0' in the port input register.

Note that no pull-up resistor is shown on the SCL line. In this simple case, the resistor is not needed; the microcontroller can simply leave the line on output, and set it to '1' or '0' as appropriate. It can do this because the ADS1000 never drives its clock line low. This technique can also be used with multiple devices, and has the advantage of lower current consumption resulting from the absence of a resistive pull-up.

If there are any devices on the bus that may drive their clock lines low, the above method should not be used; the SCL line should be high-Z or zero and a pull-up resistor provided as usual. Note also that this cannot be done on the SDA line in any case, because the ADS1000 does drive the SDA line low from time to time, as all I²C devices do.

Some microcontrollers have selectable strong pull-up circuits built into the GPIO ports. In some cases, these can be switched on and used in place of an external pull-up resistor. Weak pull-ups are also provided on some microcontrollers, but usually these are too weak for I²C communication. If there is any doubt about the matter, test the circuit before committing it to production.

## SINGLE-ENDED INPUTS

Although the ADS1000 has a fully differential input, it can easily measure single-ended signals. A simple single-ended connection scheme is shown in Figure 12. The ADS1000 is configured for single-ended measurement by grounding either of its input pins, usually $V_{IN-}$, and applying the input signal to $V_{IN+}$. The single-ended signal can range from –0.2V to $V_{DD}$ + 0.3V. The ADS1000 loses no linearity anywhere in its input range. Negative voltages cannot be applied to this circuit because the ADS1000 inputs can only accept positive voltages.

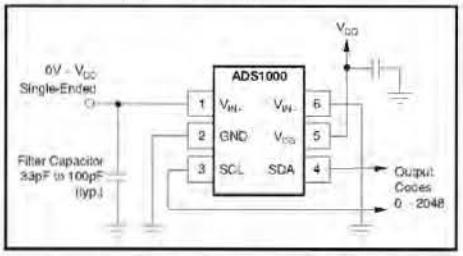



**Figure 12. Measuring Single-Ended Inputs**

The ADS1000 input range is bipolar differential with respect to the reference, that is, $V_{DD}$. The single-ended circuit shown in Figure 12 covers only half the ADS1000 input scale because it does not produce differentially negative inputs; therefore, one bit of resolution is lost. The DRV134 balanced line driver can be employed to regain this bit for single-ended signals.

Negative input voltages must be level-shifted. A good candidate for this function is the THS4130 differential amplifier, which can output fully differential signals. This device can also help recover the lost bit noted previously for single-ended positive signals. Level-shifting can also be performed using the DRV134.

## LOW-SIDE CURRENT MONITOR

Figure 13 shows a circuit for a low-side shunt-type current monitor. The circuit reads the voltage across a shunt resistor, which is sized as small as possible while still giving a readable output voltage. This voltage is amplified by an OPA335 low-drift op-amp, and the result is read by the ADS1000.

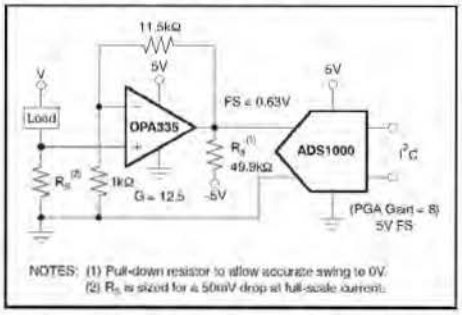



**Figure 13. Low-Side Current Measurement**

It is recommended that the ADS1000 be operated at a gain of 8. The gain of the OPA335 can then be set lower. For a gain of 8, the op amp should be configured to give a maximum output voltage of no greater than 0.75V. If the shunt resistor is sized to provide a maximum voltage drop of 50mV at full-scale current, the full-scale input to the ADS1000 is 0.63V.

## ADDITIONAL RECOMMENDATIONS

The ADS1000 is fabricated in a small-geometry low-voltage process. The analog inputs feature protection diodes to the supply rails. However, the current-handling ability of these diodes is limited, and the ADS1000 can be permanently damaged by analog input voltages that remain more than approximately 300mV beyond the rails for extended periods. One way to protect against overvoltage is to place current-limiting resistors on the input lines. The ADS1000 analog inputs can withstand momentary currents of as large as 10mA.

The previous paragraph does not apply to the $I^2C$ ports, which can both be driven to 6V regardless of the supply.

If the ADS1000 is driven by an op amp with high voltage supplies, such as ±12V, protection should be provided, even if the op amp is configured so that it will not output out-of-range voltages. Many op amps seek to one of the supply rails immediately when power is applied, usually before the input has stabilized; this momentary spike can damage the ADS1000. Sometimes this damage is incremental and results in slow, long-term failure—which can be distastrous for permanently installed, low-maintenance systems.

If using an op amp or other front-end circuitry with the ADS1000, be sure to take the performance characteristics of this circuitry into account; a chain is only as strong as its weakest link.

Any data converter is only as good as its reference. For the ADS1000, the reference is the power supply, and the power supply must be clean enough to achieve the desired performance. If a power-supply filter capacitor is used, it should be placed close to the $V_{DD}$ pin, with no vias placed between the capacitor and the pin. The trace leading to the pin should be as wide as possible, even if it must be necked down at the device.

## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (September 2006) to Revision A | Page |
|---|---|
| • Changed logic level min value from (0.7GND) to (0.7VDD) | 3 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS1000A0IDBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | BDQ | Samples |
| ADS1000A0IDBVRG4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | BDQ | Samples |
| ADS1000A0IDBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | BDQ | Samples |
| ADS1000A0IDBVTG4 | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | BDQ | Samples |
| ADS1000A1IDBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | BDR | Samples |
| ADS1000A1IDBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | BDR | Samples |
| ADS1000A1IDBVTG4 | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | BDR | Samples |

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category of the device.



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10-Jun-2014

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ADS1000 :

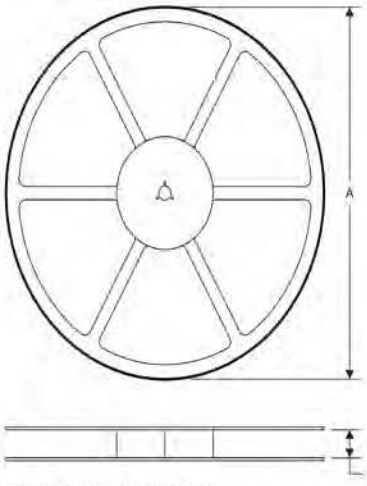
- Automotive : ADS1000-Q1

NOTE: Qualified Version Definitions:

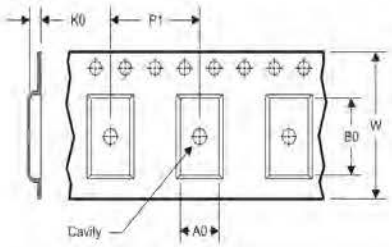
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

REEL DIMENSIONS




TAPE DIMENSIONS



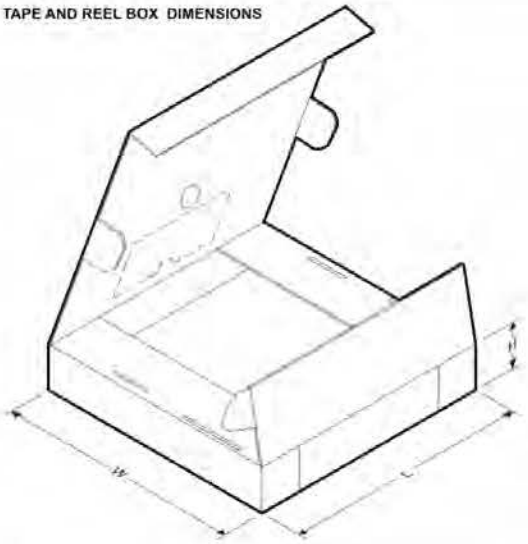

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS1000A0IDBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| ADS1000A0IDBVT | SOT-23 | DBV | 6 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| ADS1000A1IDBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| ADS1000A1IDBVT | SOT-23 | DBV | 6 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |

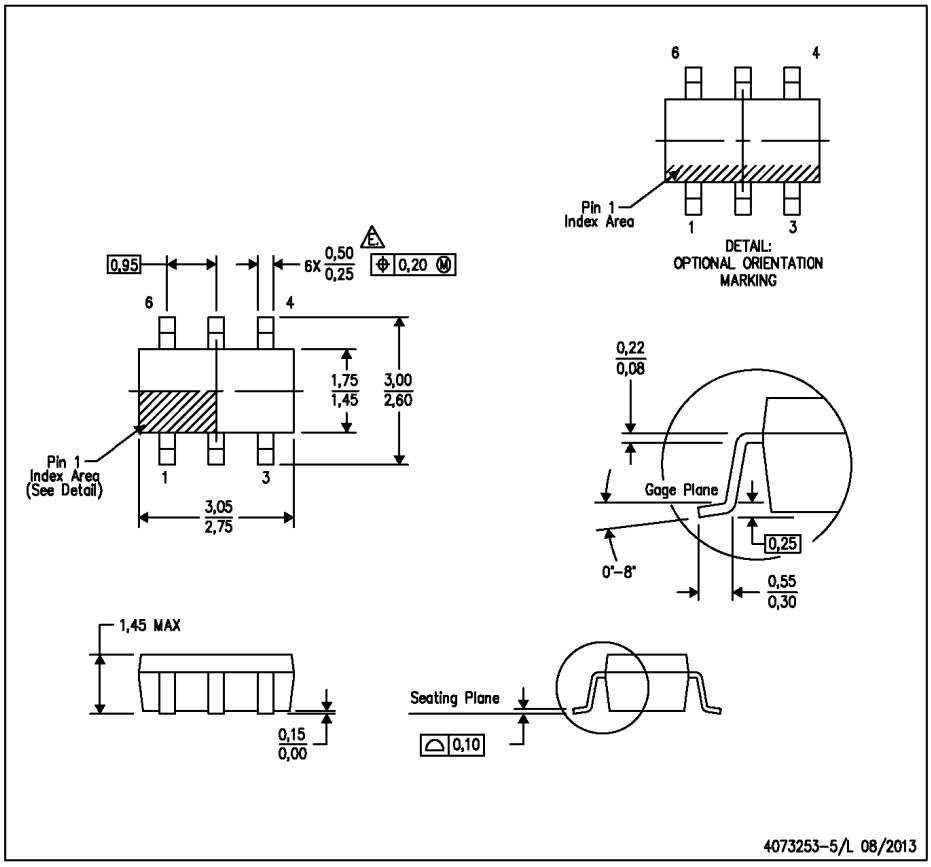
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

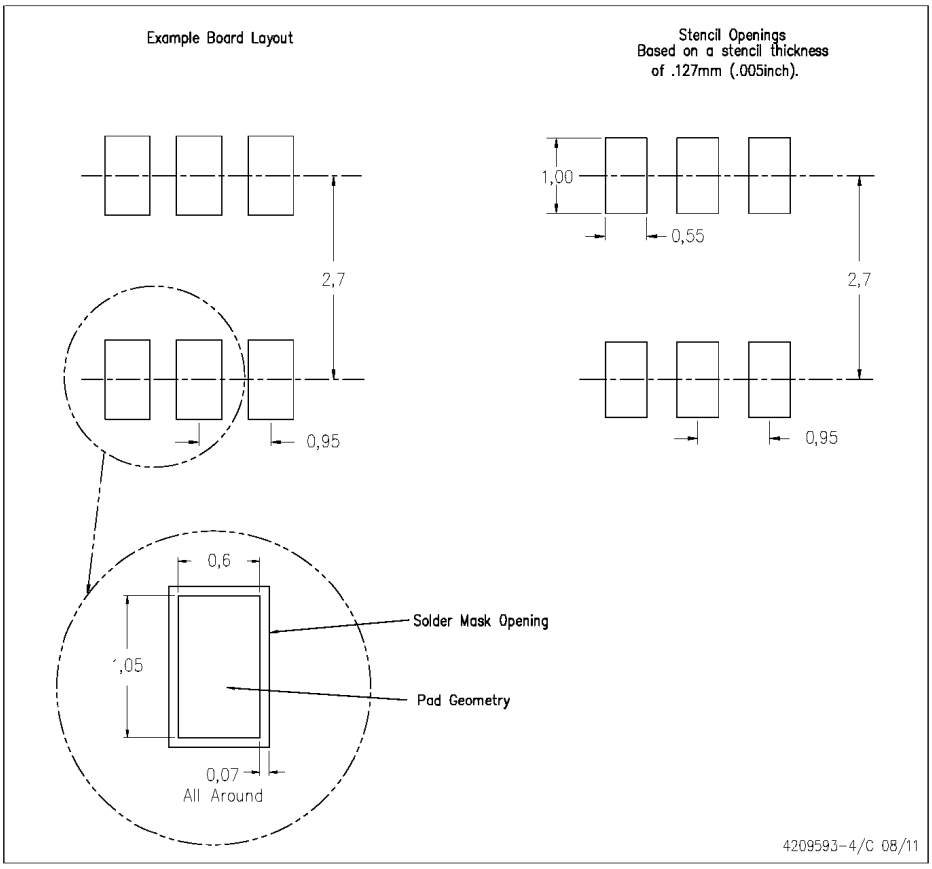
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADS1000A0IDBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| ADS1000A0IDBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 180.0 | 18.0 |
| ADS1000A1IDBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| ADS1000A1IDBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 180.0 | 18.0 |

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
A Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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# LIST OF REFERENCES


[1] Microchip Technology. (1998). Intelligent power integration. [Online]. Available: http://www.microchip.com/pagehandler/en-us/technology/intelligentpower/integration-level4.html

[2] A. L. Julian, O. Giovanna and M. E. Pfender, "SLR converter design for multi-cell batter charging," *Proc. of the IEEE 5th Energy conversion Conference and Expo*, pp. 743–748, 2013.

[3] M. E. Pfender, "Simulating and testing a DC-DC half-bridge SLR converter," M.S. thesis, Department of Electrical and Computing Engineering, Naval Postgraduate School, Monterey, CA, 2013.

[4] National Semiconductor. (1999, June). Precision voltage-to-frequency converters. [Online]. Available: http://ee-classes.usc.edu/ee459/library/datasheets/LM331.pdf

[5] Analog Devices. (2010). Isolated, precision, half-bridge driver, 4 A output, ADuM7234. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/ADuM7234.pdf

[6] P. L. Norgaard, "Integration and control of a battery balancing system," M.S. thesis, Department of Electrical and Computing Engineering, Naval Postgraduate School, Monterey, CA, 2013.

[7] H. Huang. (2010). Designing an LLC resonant half-bridge power converter. [Online]. Available: http://www.ti.com/lit/ml/slup263/slup263.pdf

[8] B. Yang and F. C. Lee, "LLC resonant converter for front end DC/DC conversion," *Applied Power Electronics Conference and Exposition*, pp. 1108–1112, 2002.

[9] Microchip Technology. (2000). Understand A/D converter performance specifications. [Online]. Available: http://ww1.microchip.com/downloads/en/appnotes/00693a.pdf

[10] Analog Devices. (2004). 3-channel, low noise, low power, 16-/24-bit ∑-Δ ADC with on-chip in-Amp and reference. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/AD7792_7793.pdf

[11] Analog Devices Inc. (2004). Evaluation board for the AD7792 16-bit, low power sigma-delta ADC (3 Channels). [Online]. Available: http://www.analog.com/static/imported-files/eval_boards/EVAL-AD7792.pdf

[12] Burr-Brown Products from Texas Instruments Inc. (2004). Low-power, 12-bit analog-to-digital converter with $I^2C$ interface. [Online]. Available: http://www.ti.com/lit/ds/sbas357a/sbas357a.pdf

[13] Burr-Brown Products from Texas Instruments Inc. (2004). 16-bit analog-to-digital converter with input multiplexer and onboard reference. [Online]. Available: http://www.ti.com/lit/ds/sbas357a/sbas357a.pdf

[14] N. Mohan and W. Robbins, "Resonant converters," in *Power Electronics, Converters Application and Design*, 3rd ed. New York, John Wiley and Sons, 2003.

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