Introduction to FPGA Circuits

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École ARCHI
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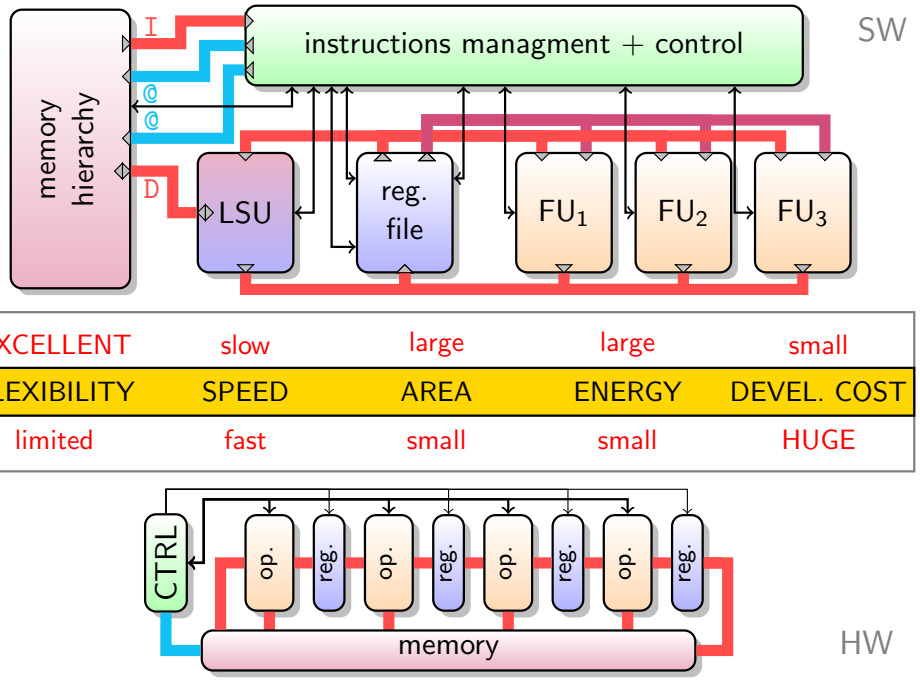
Summary

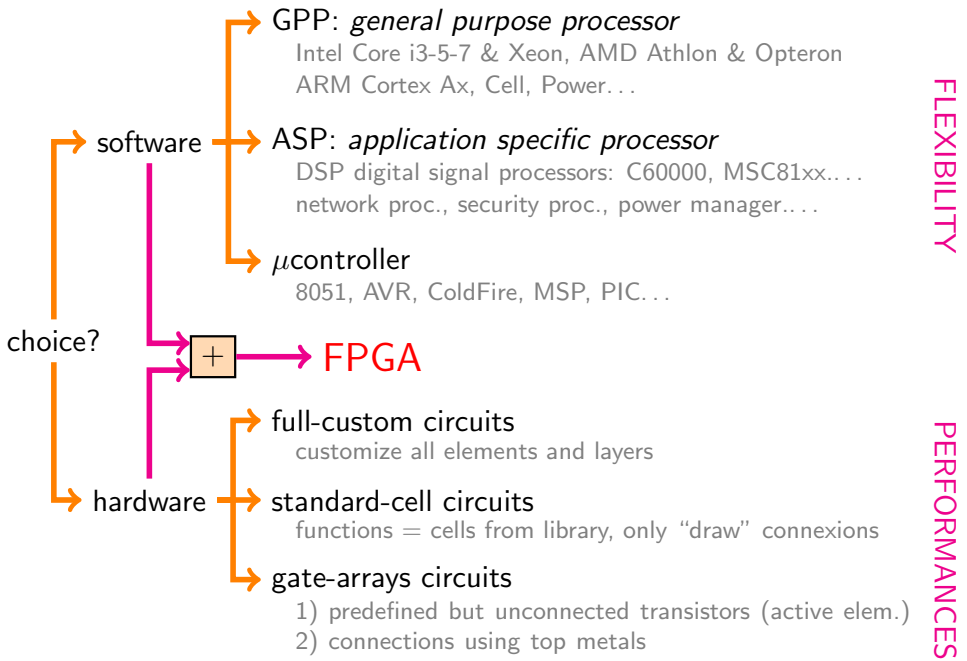
Part I

Introduction

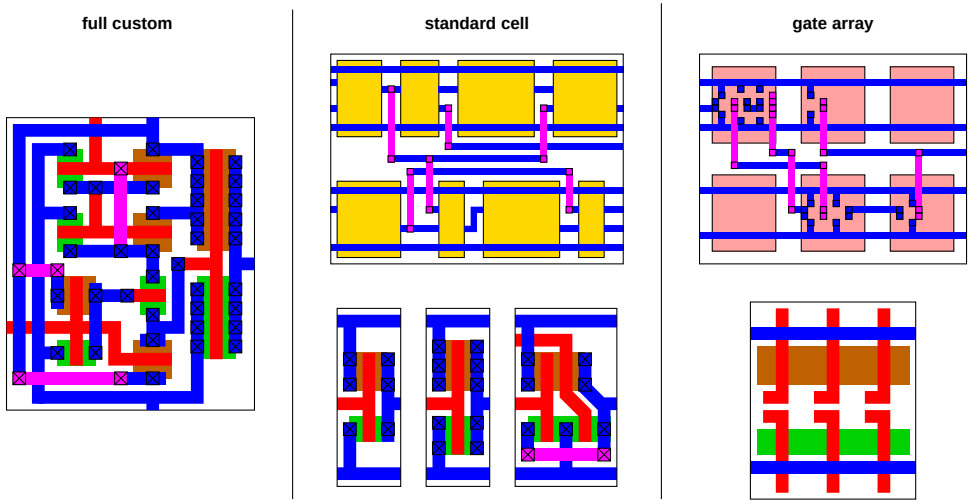
Software versus Hardware Implementation



Implementations Targets



Full-Custom vs. Standard Cell vs. Gate Arrays



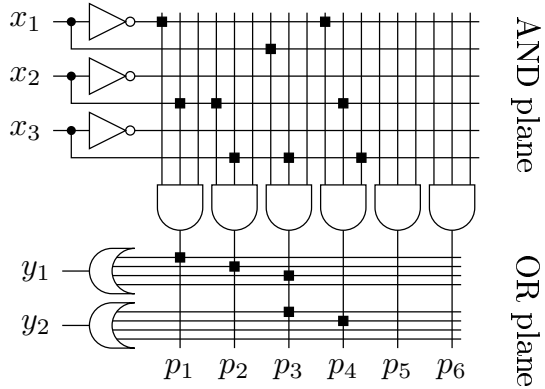
full custom	standard cell	gate array
perfs +++	perfs ++	perfs +
costs +++	costs ++	costs +

PLA: Programmable Logic Array

- User programmable device for combinational logic (197x)
- Sum-of-product canonical form
- Crossing planes of wires before configuration
- Configuration (programming): (un)set (un)wanted connections
- Inputs x_i ($\overline{x_i}$), outputs y_j

$$p_1 = \overline{x_1}x_2$$
$$p_2 = x_2x_3$$
$$p_3 = x_1x_3$$
$$p_4 = \overline{x_1}x_2x_3$$

$$y_1 = \overline{x_1}x_2 + x_2x_3 + x_1x_3$$
$$y_2 = x_2x_3 + \overline{x_1}x_2x_3$$



NORs / NANDs are used in practice for CMOS circuits.

Terminology

acronym	*type*	*prog.*
ASIC	application-specific integrated circuit	N
MPGA	masked programmable logic array	Y
PROM	programmable read-only memory	Y
EPROM	erasable PROM	Y
EEPROM	electrically EPROM	Y
PAL	programmable array logic	Y
PLA	programmable logic array	Y
GAL	generic array logic[1]	Y
PLD	programmable logic device	Y
EPLD	erasable PLD	Y
SPLD	simple PLD	Y
CPLD	complex PLD	Y
FPGA	field-programmable gate array	Y

[1] GALs ≠ GALS (globally asynchronous locally synchronous)

From Gate-Arrays to FPGAs

End of book:

Bob Hartmann, Paul Newhagen and Michael Magranet
Gate Arrays: Implementing LSI Technology, 1982

> " *The probabilities are high that someone will produce an electrically alterable logic array.*"

June 3rd, 1983:

Foundation of the Altera society by
Bob Hartmann[1], Paul Newhagen[1], Michael Magranet[1],
Jim Sansburry[2] and Jim Hazle[1]

Source: "*Altera: A History of Innovation*" from Altera website

[1]previously at Fairchild Semiconductor, [2]previsouly at HP.

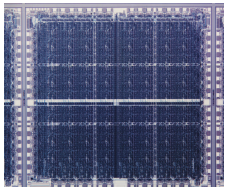
First Commercial FPGA

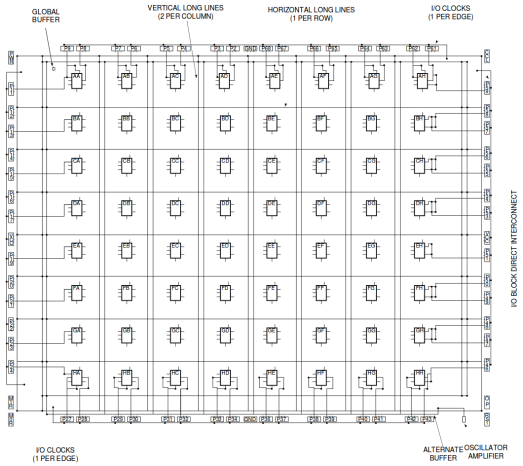
1984:

Xilinx society founded by Ross Freeman and Bernard Vonderschmitt

1985: XC2064

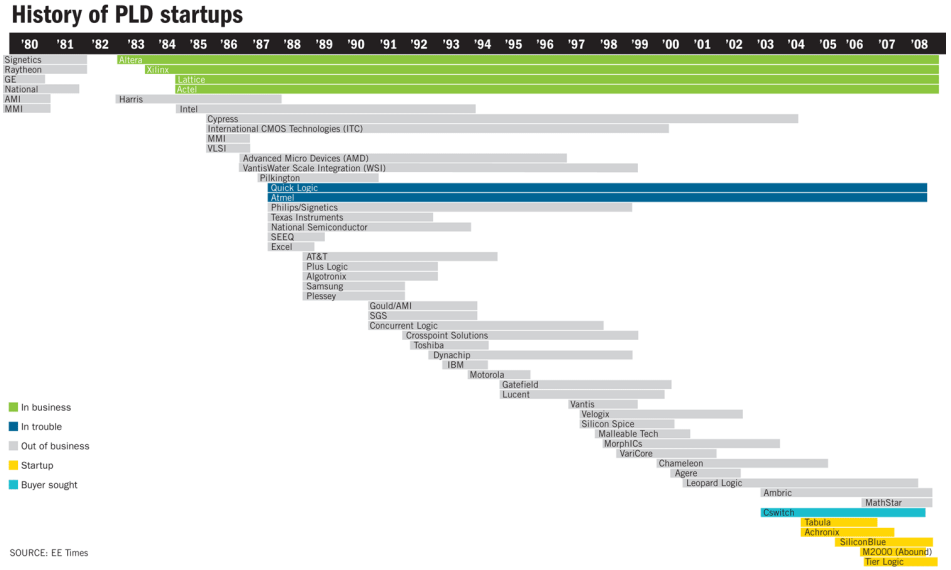
- CMOS 2.5 μm (Seiko), 85 kT
- $\approx$ 1000 gates
- 64 CLBs, 122 FFs, LUT3
- 58 I/O (68-pin PLCC package)
- 18 MHz ext. crystal oscillator
- Config.: 12 038 bits





Source: IEEE SSC Mag. Vol. 3 No. 4 2011 p. 18
& Xilinx Data Sheet

History of PLD Startups



Source: EE Times

FPGAs Application Domains

- ASIC Prototyping
- Audio, video & image processing
- Automotive
- Aviation
- Consumer Electronics
- Industrial
- Test & measures
- Networks, wired and wireless communications
- Data centers, high-performance computing and storage
- Medical
- Security and defense
- Aerospace
- ...

Xilinx FPGAs on MARS!

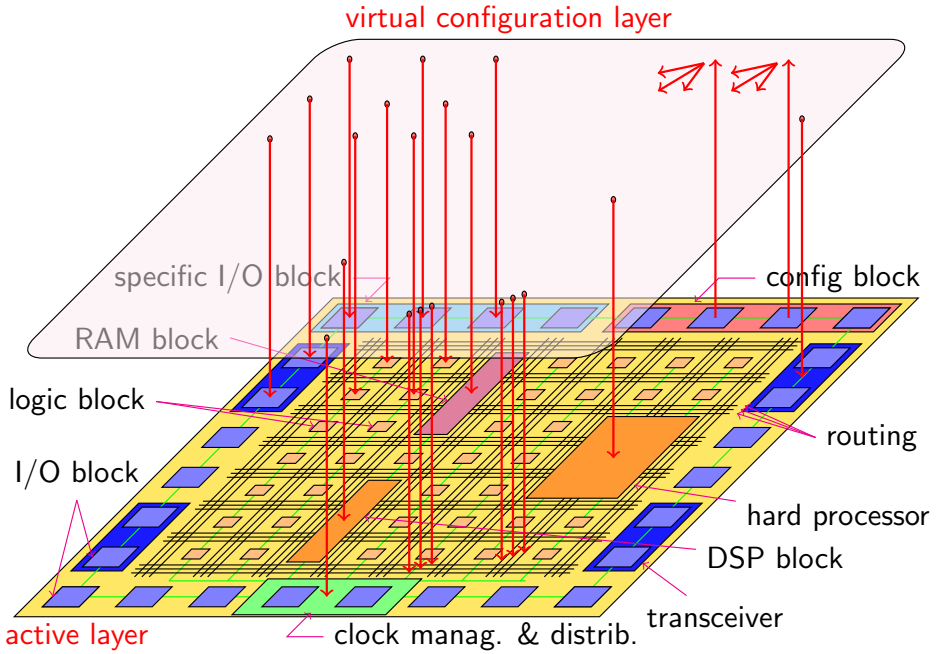
"According to NASA's Jet Propulsion Laboratory in Pasadena, California, the Spirit Mars Exploration Rover (MER) launched June 10, 2003 and the Opportunity MER launched July 7, 2003 will employ some of the most advanced radiation tolerant Xilinx Virtex FPGAs once they reach Mars. The Xilinx devices will be used to control the pyrotechnic devices on the lander, and several motor control functions on the rover, including controllers for the wheels, steering, and antenna gimbals.

Chosen because of their re-programmability and density, the Virtex FPGAs serve as the 'main brain' of the motor control boards. "

SOURCE: Xilinx press release n. 03104, 2003, July 21st, San José, California.

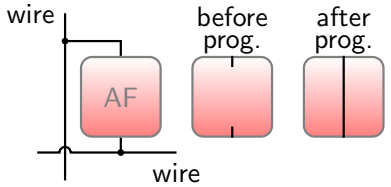
See also: `http://www.xilinx.com/publications/archives/xcell/Xcell50.pdf`

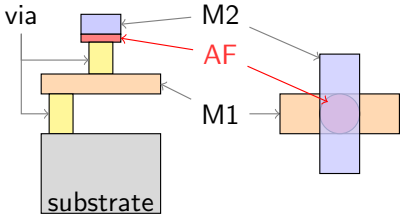
FPGA Overview



Configuration Cell Technology: Anti-Fuse (1/2)

Principle:





Example:

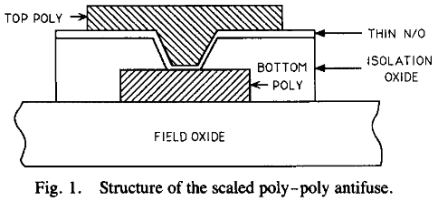


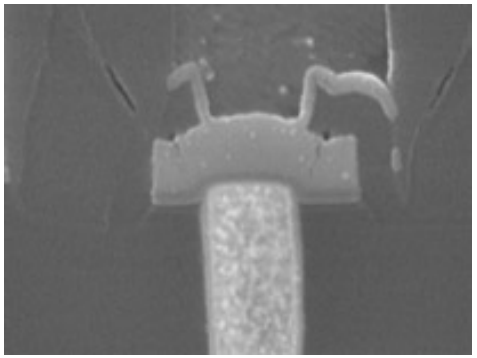
Fig. 1. Structure of the scaled poly-poly antifuse.

- 15-20 Å nitride-oxide (NO) dieletric between 2 polysilicon layers
- 5.5 V circuit supply voltage
- 13.6 V programming voltage
- 0.8 × 0.8 μm cell footprint

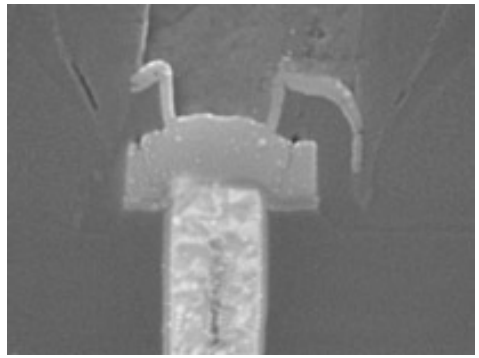
SOURCE: IEEE Electron Device Letters, vol. 12, n. 4, pp. 151–153, 1991 (doi: 10.1109/55.75747)

Configuration Cell Technology: Antifuse (2/2)

Cross section of antifuses in ACTEL (now Microsemi) FPGAs:

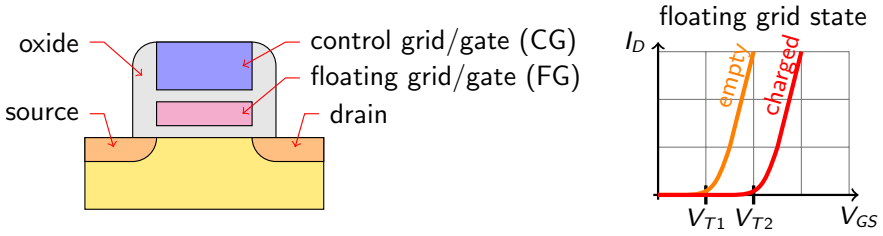


Unprogrammed

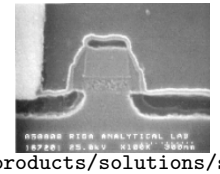


Programmed

Configuration Cell Technology: FLASH (1/2)



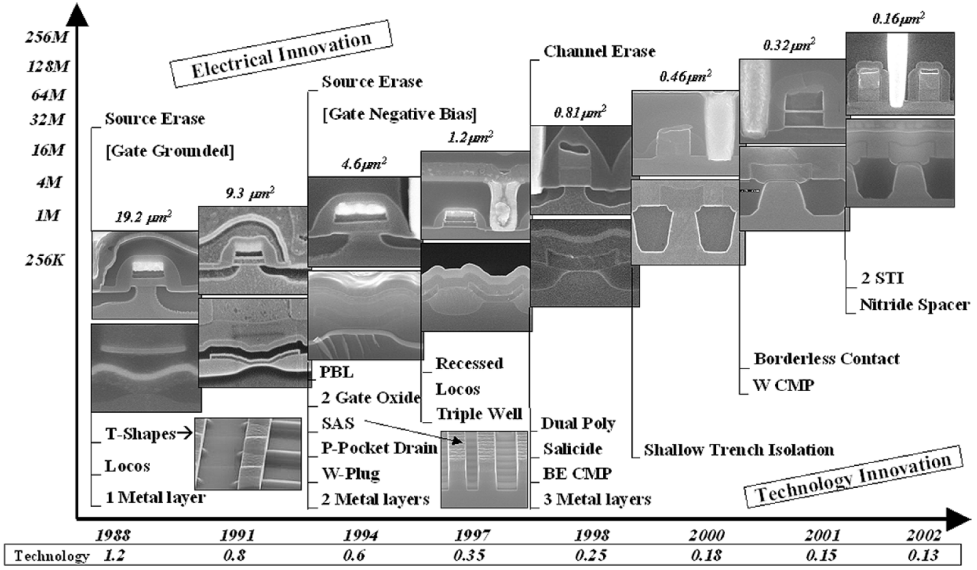
- Electrons can be trapped in the FG
- Threshold voltage (V_T) depends on the charge in the FG
- READ: apply intermediate voltage on the CG, then sense channel
- STORE: inject electrons in the FG
- ERASE: remove electrons from the FG (tunneling)



SOURCE: `http://www.actel.com/products/solutions/security/securitydevicearch.aspx`

Configuration Cell Technology: FLASH (2/2)

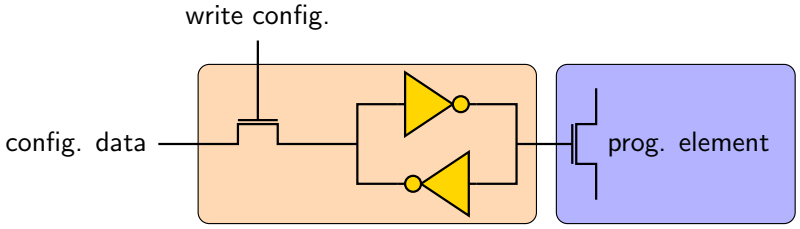
FLASH cell evolution for data storage (not always applicable to FPGAs)

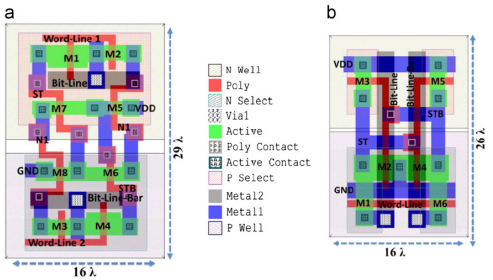


SOURCE: Proc. IEEE, vol. 91, n. 4, pp. 503-522, 2003 (doi:10.1109/JPROC.2003.811703)

Configuration Cell Technology: SRAM

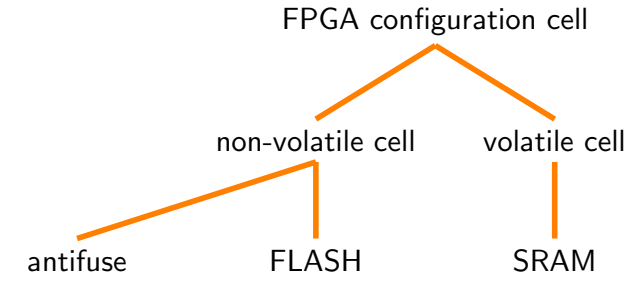
1-bit static RAM cell (std. CMOS techno.) for each programmable element





SOURCE: Microelectronics J., vol. 42, n. 11, pp. 1187-1207, 2011 (doi:10.1016/j.mejo.2011.07.008)

Typical FPGA Configuration Cell Types



	antifuse	FLASH	SRAM
reconfigurable:	no	yes	yes
config. at power down:	saved	saved	lost
fabrication process:	special	FLASH	std. CMOS
radiation tolerance:	very good	good	medium

Overview of IC Production Economics (1/2)

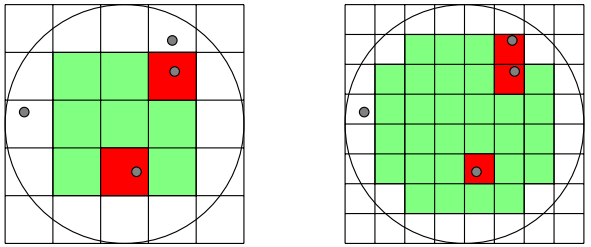
$$C = \frac{F}{N} + V$$

- C cost per circuit
- F fixed costs $F = F_{NRE} + F_{other}$
  - F_{NRE} non-recurring engineering costs: *prototyping, masks, packaging tooling, personnel costs, training, support, CAD tools, computers, ...*
  - F_{other} all other fixed costs: *documentation, marketing, administration, after-sales, ...*
- N number of circuits to sell
- V variable cost per circuit $V = V_{process} + V_{packaging} + V_{test}$
  - $V_{process}$ cost for producing one die
  - $V_{packaging}$ package and "transformations" costs
  - V_{test} cf. specific course (depends on complexity and duration)

Overview of IC Production Economics (2/2)

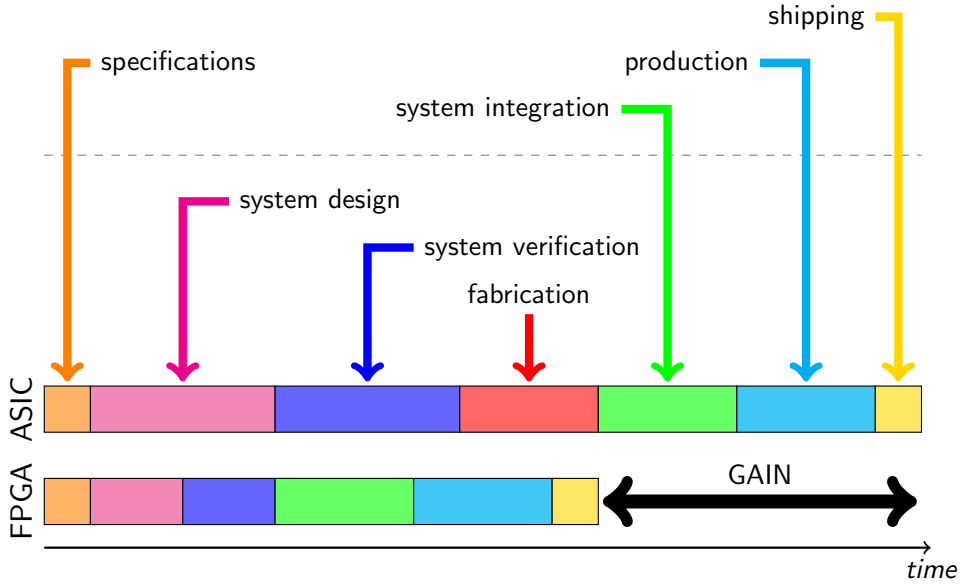
$$V_{process} = \frac{W}{K \cdot Y_W \cdot Y_P} \qquad K = \pi\left(\frac{r^2}{A} - \frac{2r}{\sqrt{2A}}\right)$$

- W wafer cost (depends on process technology and wafer radius r)
- K number of complete die per wafer
- Y_W die yield per wafer
- Y_P packaging yield
- A die area



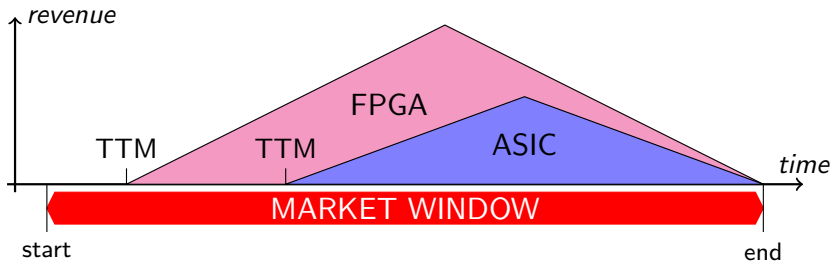
Economic Motivations for FPGAs vs ASICs (1/4)

Time to market (TTM):

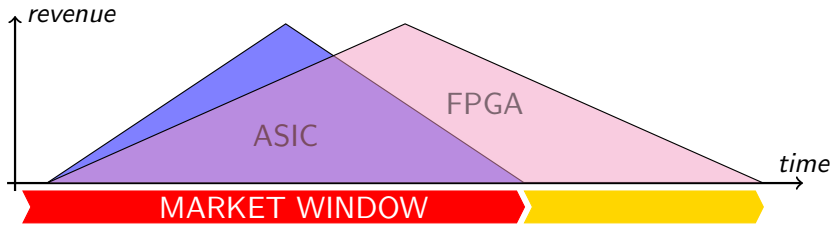


Economic Motivations for FPGAs vs ASICs (2/4)

Early arrival on the market:

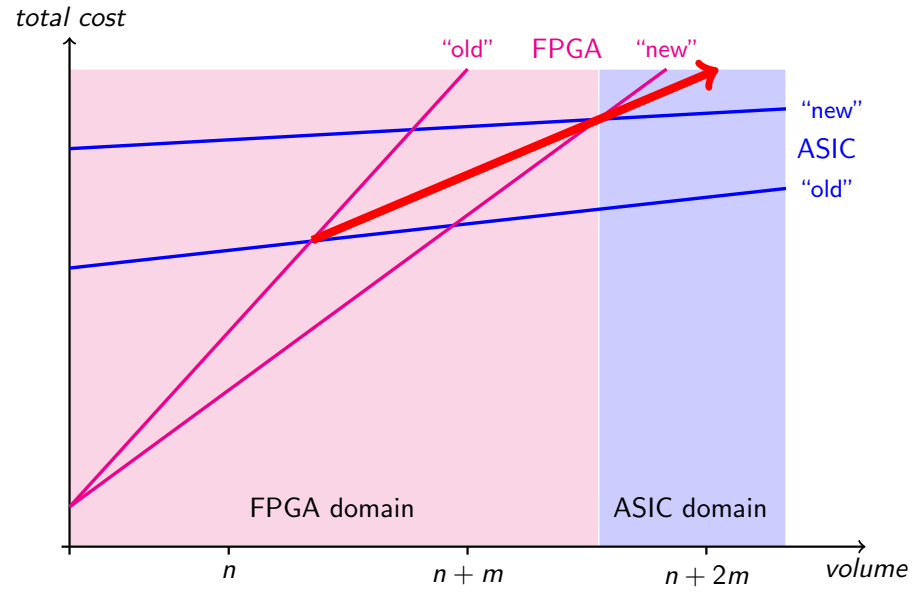


Longer product life due to reconfigurability:



Economic Motivations for FPGAs vs ASICs (3/4)

FPGA domain vs ASIC domain (arbitrary scales):



Economic Motivations for FPGAs vs ASIC (4/4)

ASIC advantages:

- ultra high performances and very low power
- low unit cost
- small form factor

FPGA advantages:

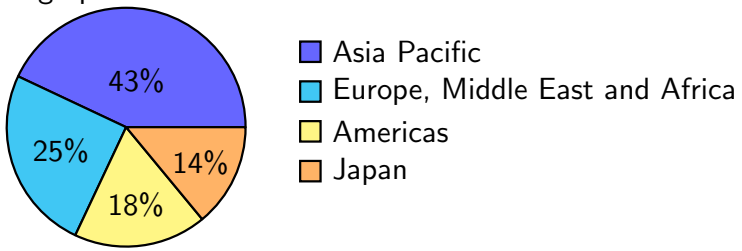
- simple design and verification cycles
- no NRE costs
- low (re)design risk
- fast time to market
- reconfiguration (flexible systems)

Economic Aspects: Altera Corp. Values for 2012 (1/2)

Net sales: 1 783 035 $ $\approx$ 2 600 employees worldwide

Main markets:

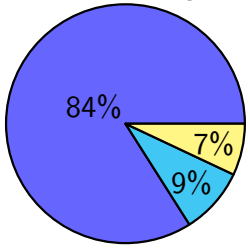
Geographic sales distribution:

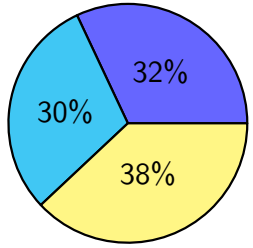


SOURCE: Altera website `http://investor.altera.com/`, News Release

Economic Aspects: Altera Corp. Values for 2012 (2/2)

Products categories:



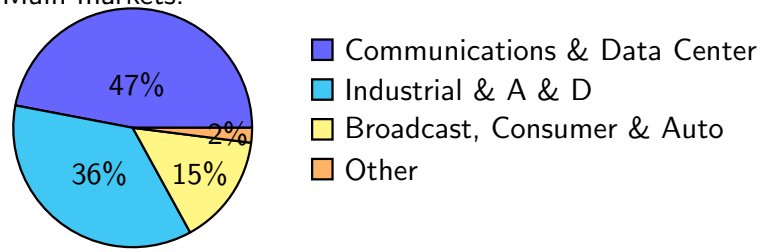


SOURCE: Altera website `http://investor.altera.com/`, News Release

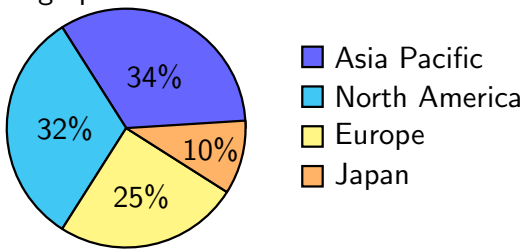
Economic Aspects: Xilinx Corp. Values for 2012 (1/2)

Net sales: 2 240 700 $ ≈ 3 400 employees worldwide

Main markets:

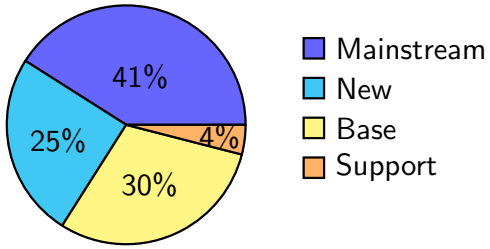


Geographic sales distribution:



Source: Xilinx website `http://investor.xilinx.com/releases.cfm`, Investor Factsheet

Economic Aspects: Xilinx Corp. Values for 2012 (2/2)

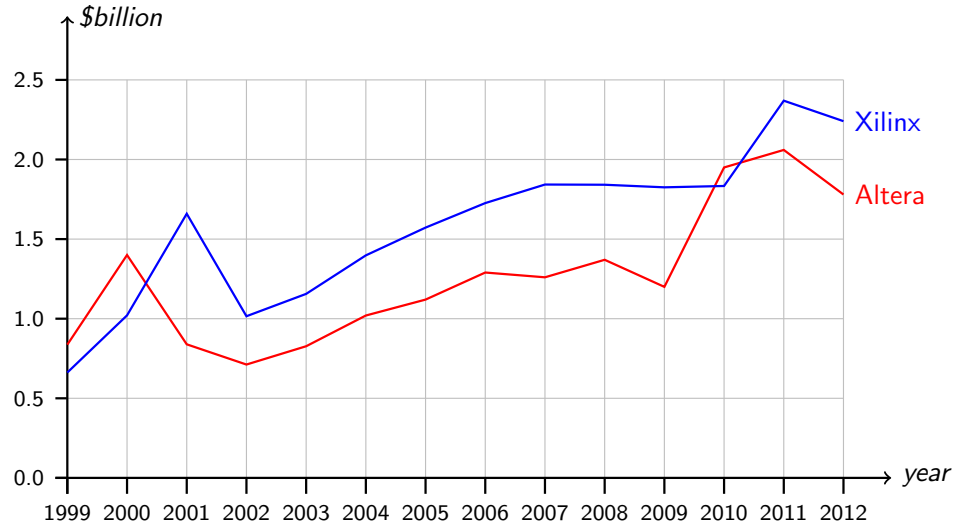


Source: Xilinx website `http://investor.xilinx.com/releases.cfm`, Investor Factsheet

FPGA Companies

Achronix Semiconductor	`www.achronix.com`
Altera	`www.altera.com`
Lattice Semiconductor	`www.latticesemi.com`
Microsemi (previously Actel)	`www.microsemi.com`
QuickLogic	`www.quicklogic.com`
Tabula	`www.tabula.com`
Xilinx	`www.xilinx.com`

FPGA Companies Revenues over 1999–2012



Source: FPGA companies websites

Reconfigurable Architectures

- Fine grain reconfigurable architectures:

  Def.: reconfiguration at the bit/signal/gate level

  Pros.: huge flexibility

  Cons.: high configuration cost (area, time)

  Examples: FPGAs

- Coarse grain reconfigurable architectures

  Def.: reconfiguration at the function/bloc level:

  Pros.: small configuration cost

  Cons.: limited flexibility

  Examples: Tensilica
  Examples: DART (IRISA), Systolic Ring (LIRMM), ...

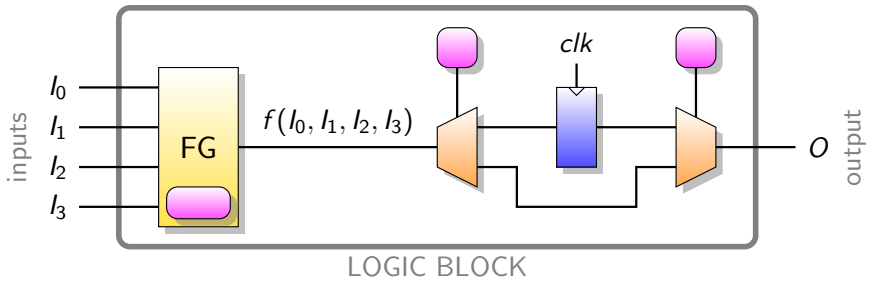
Part II

FPGA Elements

Logic Block

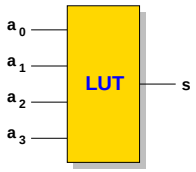
Resources:

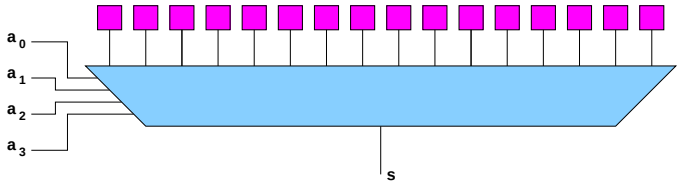
- input and output pins
- configurable logic function generator(s) (FG)
  f is an arbitrary function of the inputs
- flip-flop(s) some intermediate registers and pipelining
- configurable internal selection and routing between resources



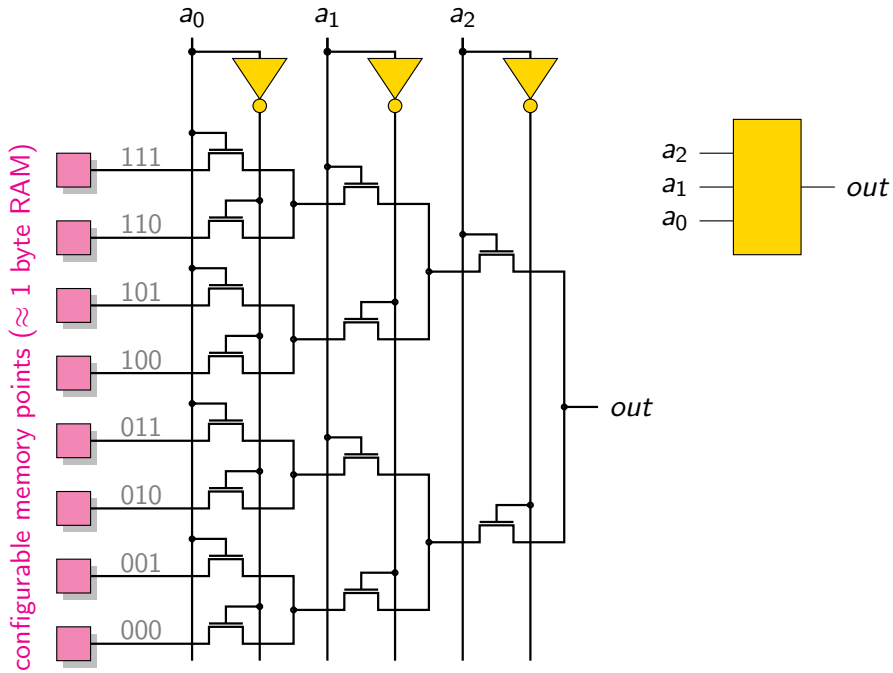
Look Up Tables (LUT)

- Programmable memory cells: configuration of the truth table for all possible values
- Address bits: selection of the truth table line
- Typical LUT types: 1 or 2 outputs, 3 to 6 inputs





One Possible Implementation of a LUT-3



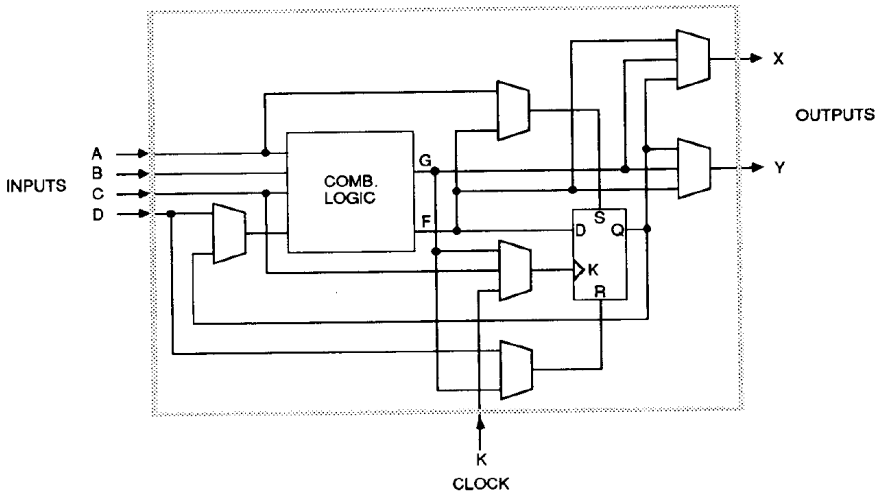
Examples of LUT-4 Configurations

a_3	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
a_2	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
a_1	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
a_0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
f	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

a_3	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
a_2	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
a_1	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
a_0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
f	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

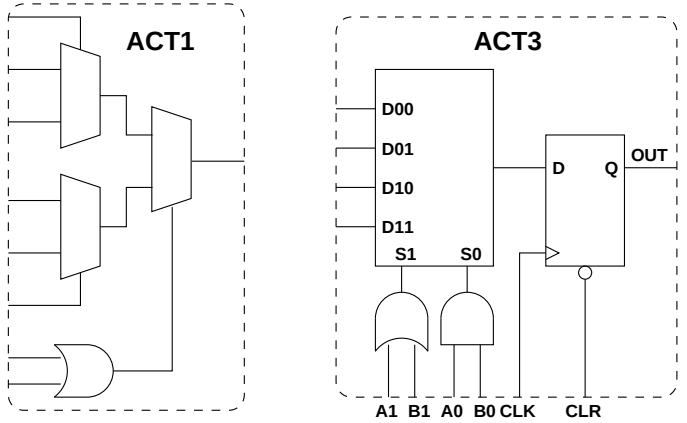
a_3	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
a_2	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
a_1	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
a_0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
f	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0

XC 2064 Configurable Logic Block (CLB)



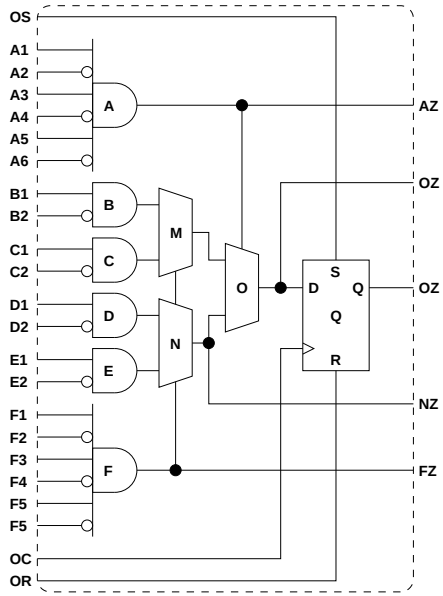
Source: Xilinx data sheet XC 2064/2018 Logic Cell Array p. 2.64

Actel ACT1 and ACT3 Logic Blocks



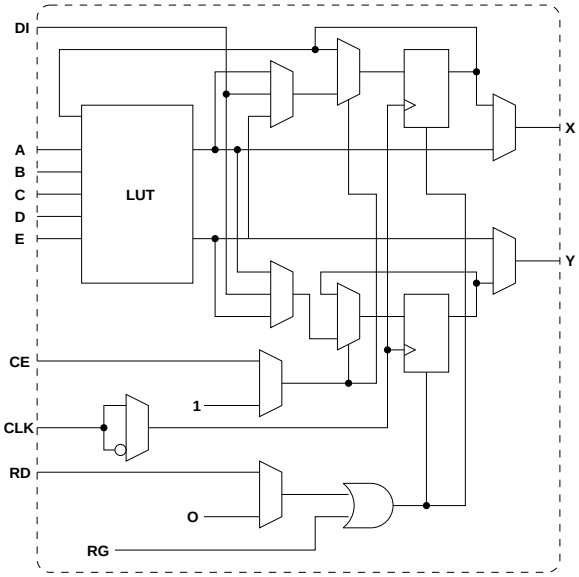
Source: Actel data sheet

Old Quicklogic Logic Block



SOURCE: Quicklogic data sheet

Xilinx XC3000 Logic Block

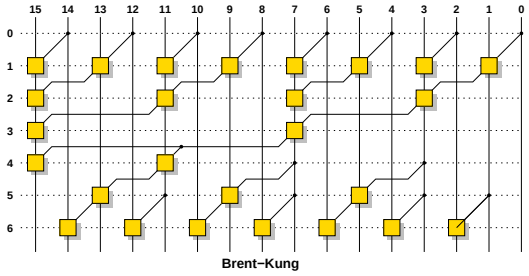


SOURCE: Xilinx data sheet

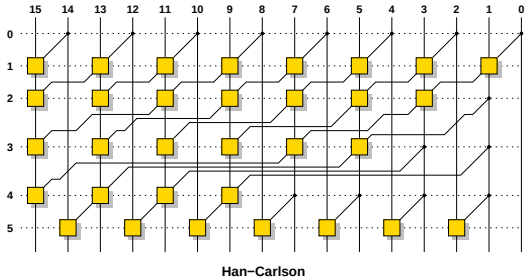
Carry Propagation Problem

Parallel prefix adders:

Building high-speed adders is very costly using flexible logic blocks and general routing resources



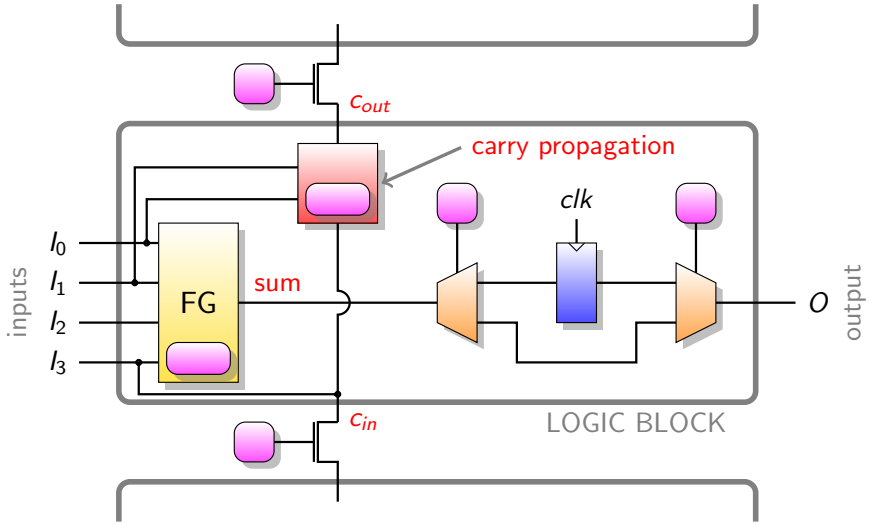
Most of applications use many adders



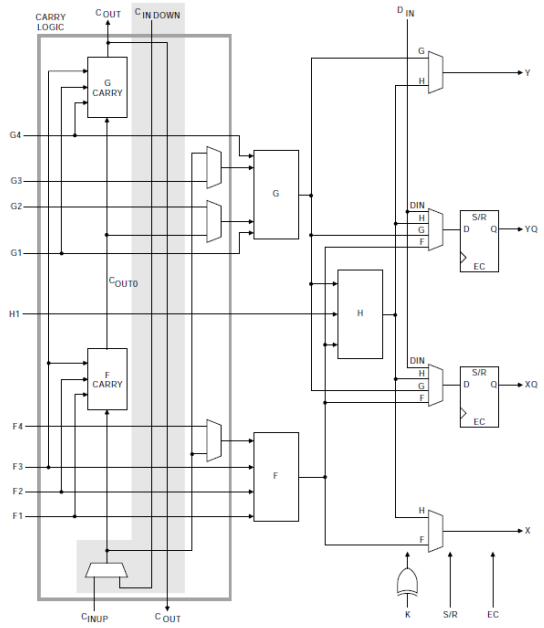
Carry Propagation Solution

Add dedicated resources for high-speed addition

There is a tradeoff between performances, cost and flexibility

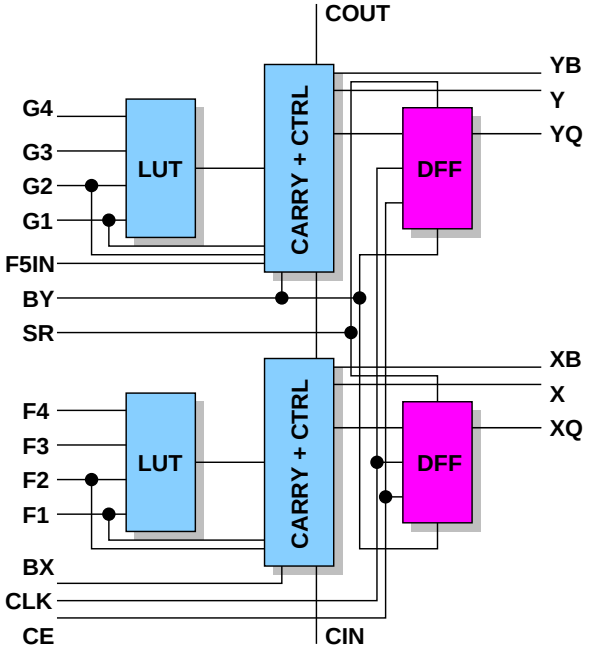


Carry Logic in a Xilinx XC 4000 E

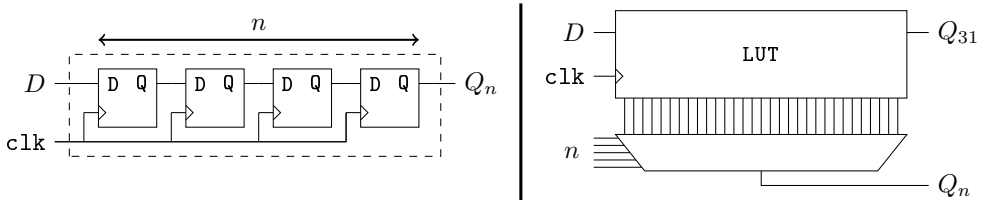


Source: Xilinx data sheet

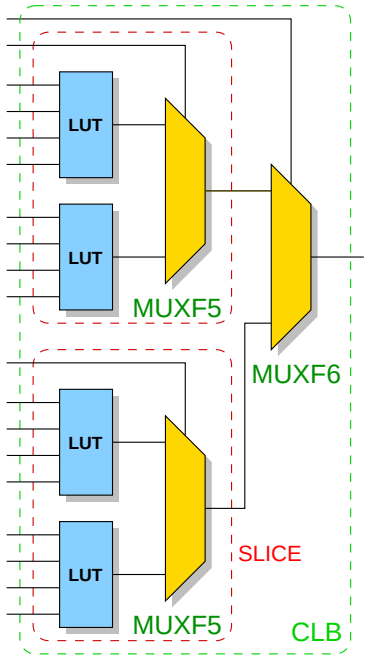
Xilinx Spartan II E Configurable Logic Block



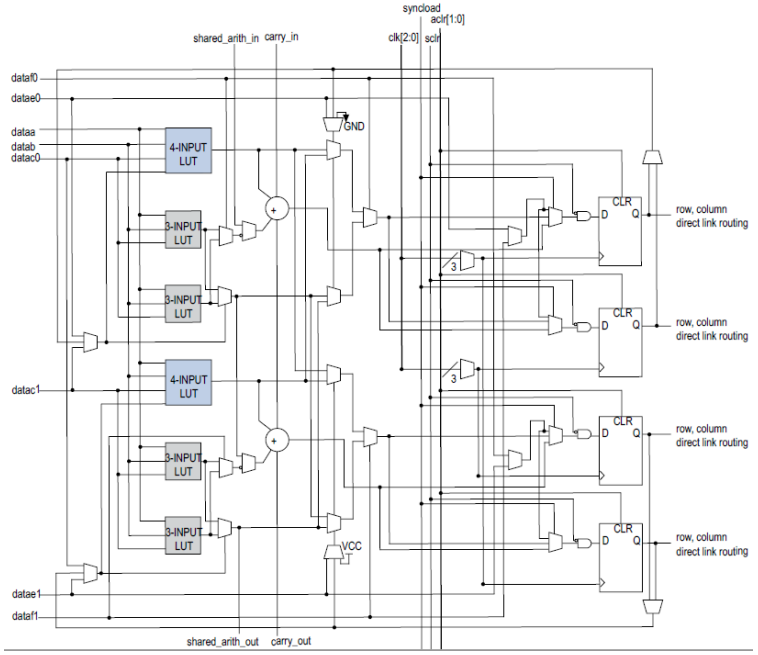
Shift Registers in Logic Blocks



Towards Larger LUTs

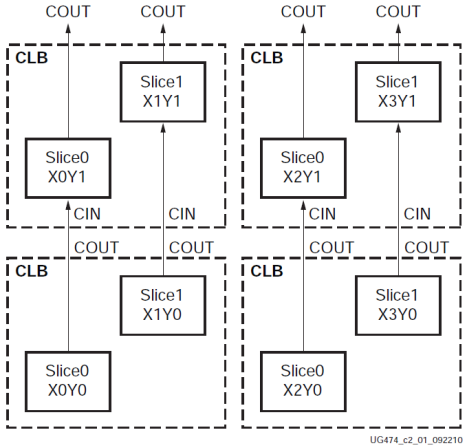


Adaptive Logic Module in a Altera Stratix V



Source: Altera data sheet stx5_51002 p. 1.7

Xilinx Virtex 7 Configurable Logic Block (1/3)

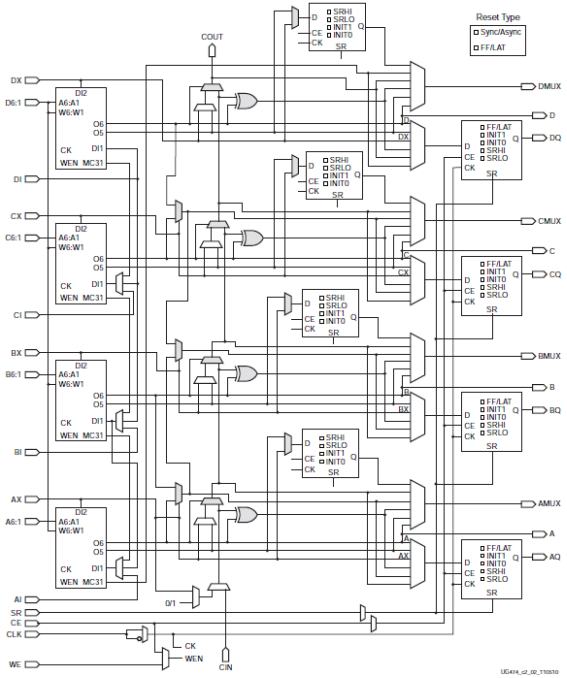


Source: Xilinx data sheet UG474 p. 12

Resources per CLB:

Slices	LUT-6	Flip-Flops	Arithmetic & Carry Chains	DRAM	Shift Register
2	8	16	2	256 bits	128 bits

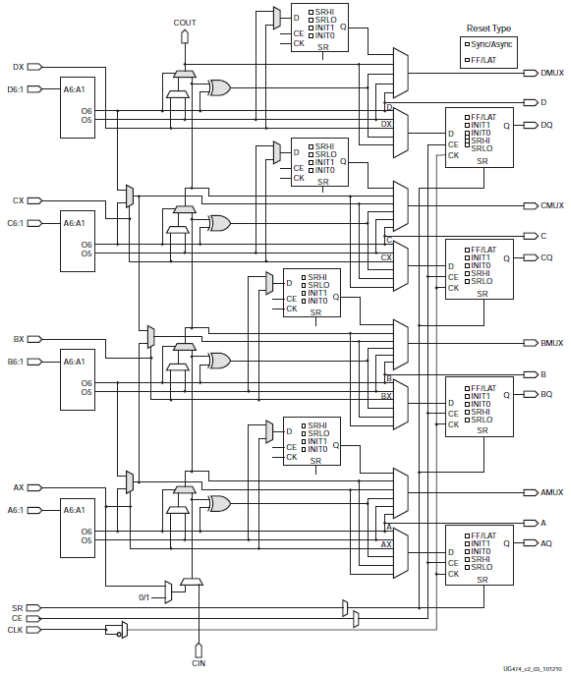
Xilinx Virtex 7 Configurable Logic Block (2/3)



SLICEM

Source: Xilinx data sheet UG474 p. 14

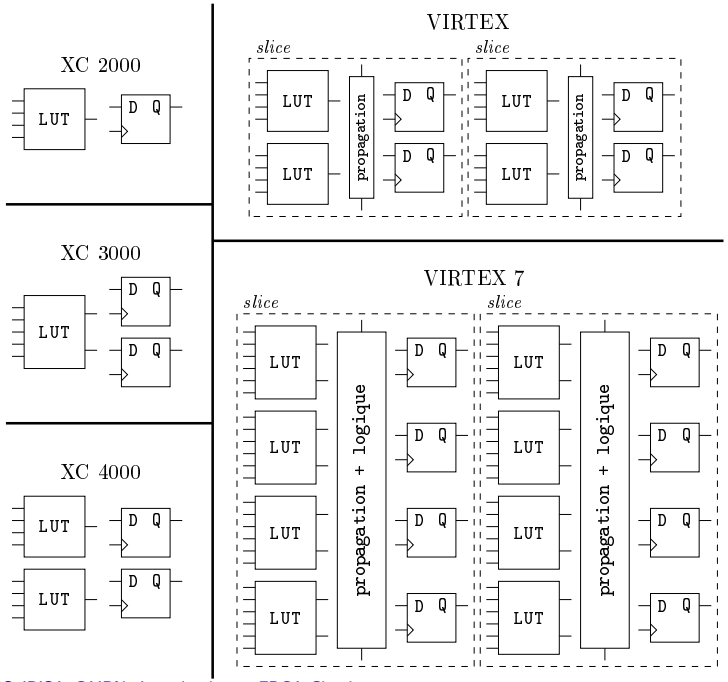
Xilinx Virtex 7 Configurable Logic Block (3/3)



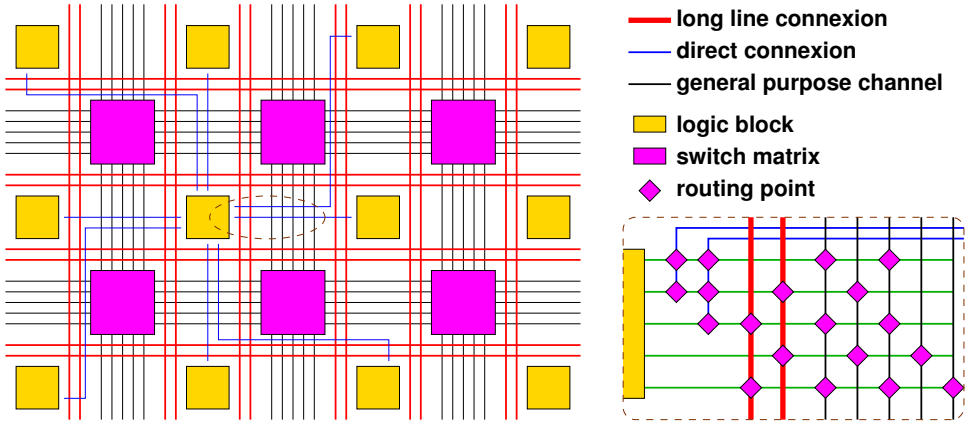
SLICEL

Source: Xilinx data sheet UG474 p. 15

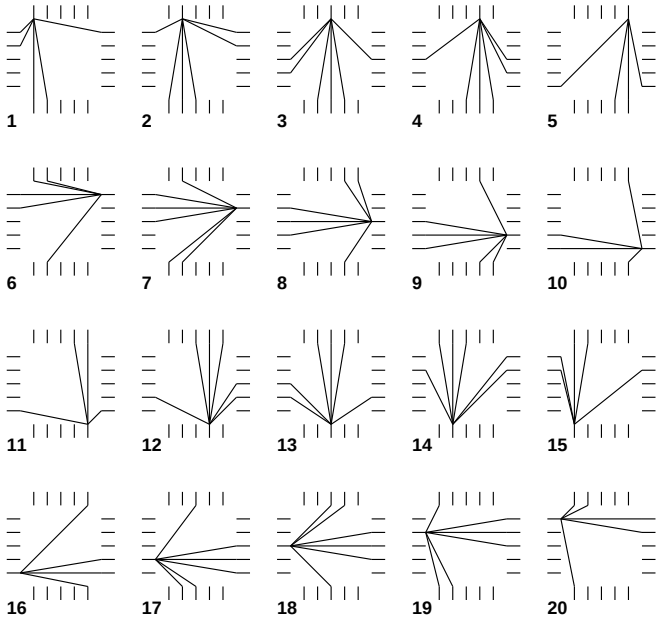
Evolution of Xilinx CLBs



Typical Routing Overview

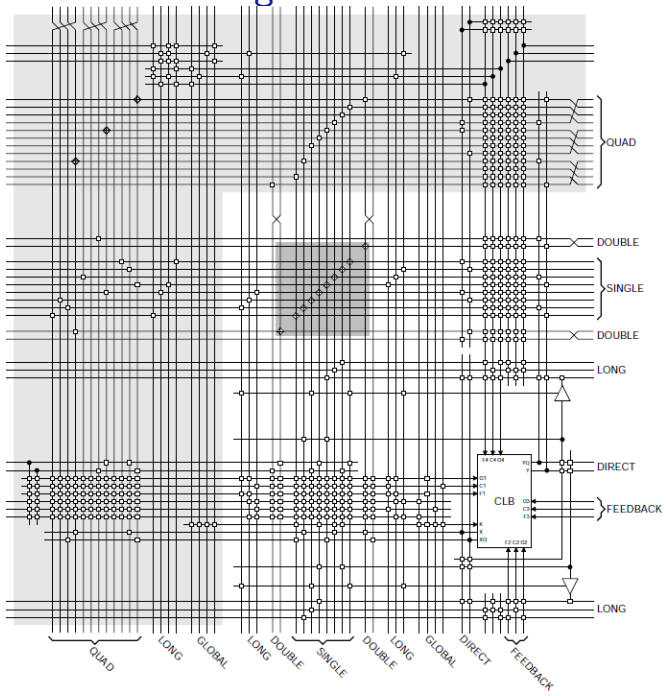


Xilinx XC 3000 Switch Matrix



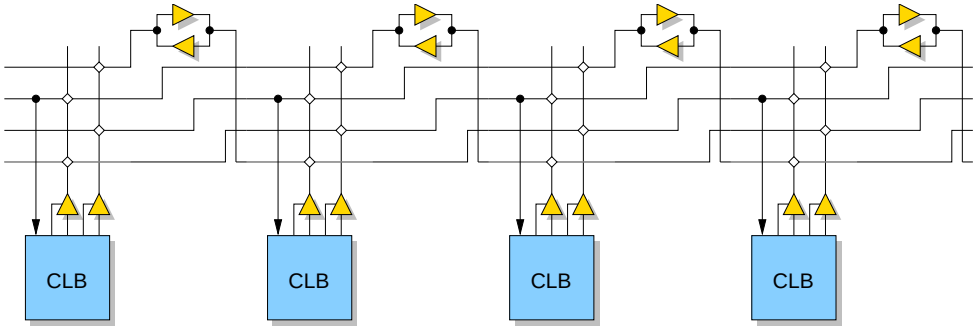
Source: Xilinx data sheet

Routing Elements in Xilinx XC 4000 E



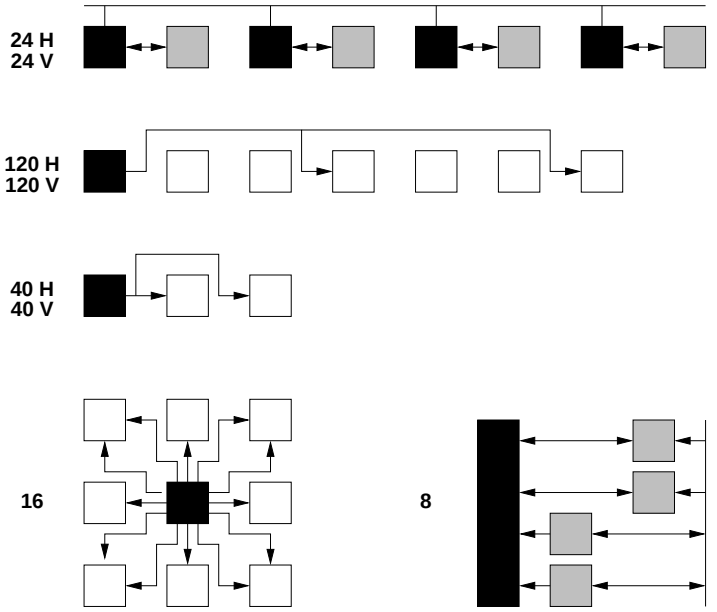
Source: Xilinx data sheet

Routing Elements in a Xilinx Spartan II E



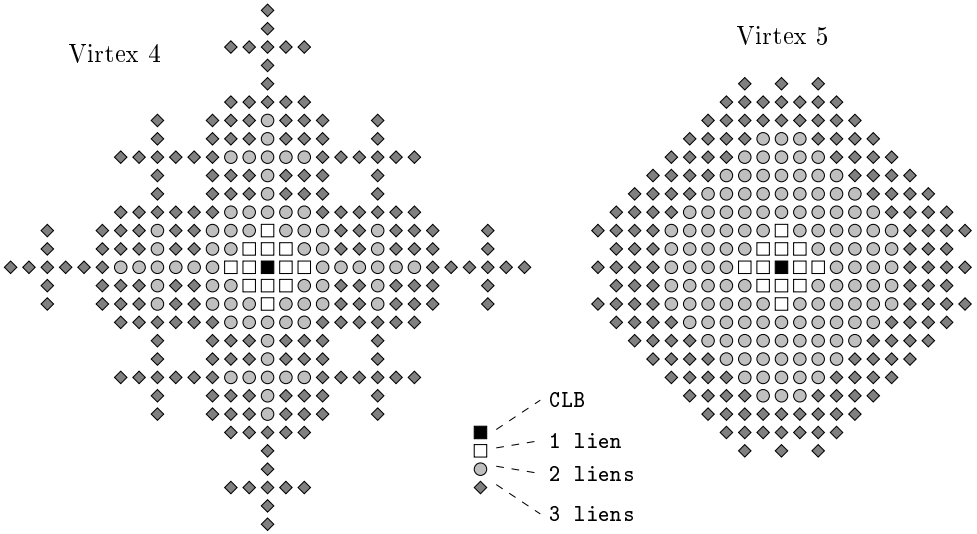
Source: Xilinx data sheet

Routing Elements in Xilinx Virtex II



Source: Xilinx data sheet

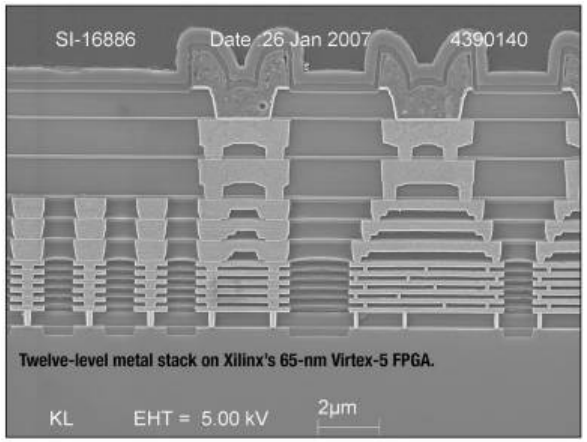
Routing Elements in Xilinx Virtex 4 & Virtex 5



Source: Xilinx data sheet

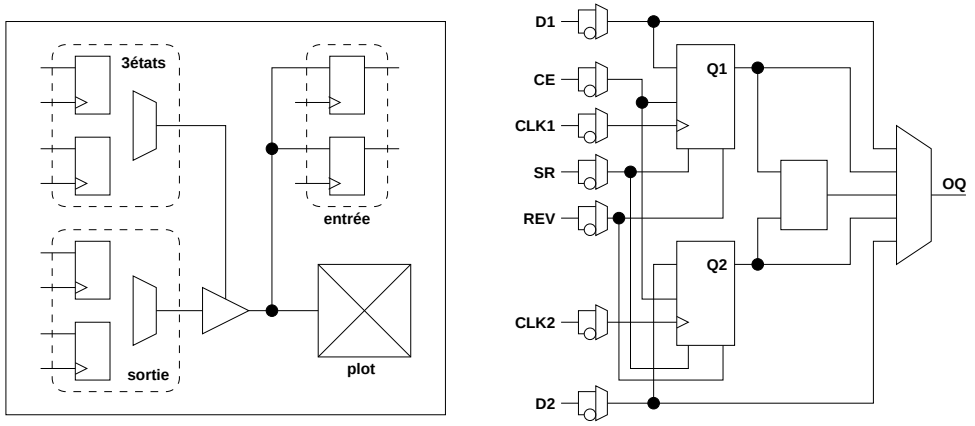
Cross Section of a Virtex 5 FPGA 65 nm

12 metal layers (11 copper, 1 aluminium), 300 mm wafers, 1 V core supply



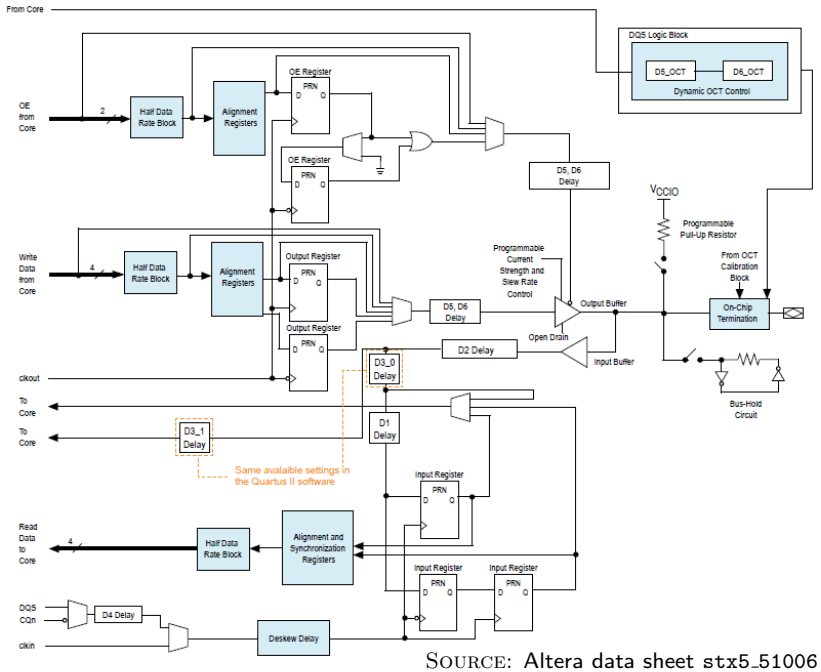
Source: `http://www.eetimes.com/showArticle.jhtml?articleID=197003451`

Input/Output Block in a Xilinx Virtex II



Source: Xilinx data sheet

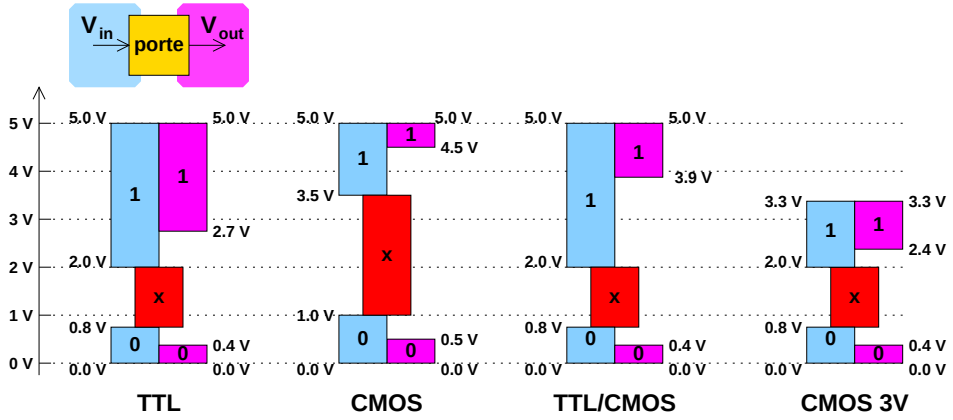
I/O Element in a Altera Stratix V



Source: Altera data sheet `stx5_51006` p. 5.15

I/O Have to Support Various Interface Standards

For "old" FPGAs:



Some of the Supported Interface Standards in Virtex 7

HSTL_I_DCI, DIFF_HSTL_I_DCI, SSTL18_I_DCI, DIFF_SSTL18_I_DCI, HSTL_I_DCI_18, DIFF_HSTL_I_DCI_18, SSTL18_II_DCI, DIFF_SSTL18_II_DCI, HSTL_II_DCI, DIFF_HSTL_II_DCI, SSTL18_II_T_DCI, DIFF_SSTL18_II_T_DCI, HSTL_II_DCI_18, DIFF_HSTL_II_DCI_18, SSTL15_DCI, DIFF_SSTL15_DCI, HSTL_II_T_DCI, DIFF_HSTL_II_T_DCI, SSTL15_T_DCI, DIFF_SSTL15_T_DCI, HSTL_II_T_DCI_18, DIFF_HSTL_II_T_DCI_18, SSTL135_DCI, DIFF_SSTL135_DCI, SSTL135_T_DCI, DIFF_SSTL135_T_DCI, SSTL12_DCI, DIFF_SSTL12_DCI, SSTL12_T_DCI, DIFF_SSTL12_T_DCI

HSTL_I_DCI, DIFF_HSTL_I_DCI, SSTL18_I_DCI, DIFF_SSTL18_I_DCI, HSTL_I_DCI_18, DIFF_HSTL_I_DCI_18, SSTL18_II_DCI, DIFF_SSTL18_II_DCI, HSTL_II_DCI, DIFF_HSTL_II_DCI, SSTL15_DCI, DIFF_SSTL15_DCI, HSTL_II_DCI_18, DIFF_HSTL_II_DCI_18, SSTL135_DCI, DIFF_SSTL135_DCI, SSTL12_DCI, DIFF_SSTL12_DCI

HSTL_II_T_DCI, SSTL18_II_T_DCI, DIFF_SSTL18_II_T_DCI, HSTL_II_T_DCI_18, SSTL15_T_DCI, DIFF_SSTL15_T_DCI, DIFF_HSTL_II__T_DCI, SSTL135_T_DCI, DIFF_SSTL135_T_DCI , DIFF_HSTL_II_T_DCI_18, SSTL12_T_DCI, DIFF_SSTL12_T_DCI

LVDCI_18, HSTL_I_DCI, DIFF_HSTL_I_DCI, SSTL18_I_DCI, DIFF_SSTL18_I_DCI, LVDCI_15, HSTL_I_DCI_18, DIFF_HSTL_I_DCI_18, SSTL18_II_DCI, DIFF_SSTL18_II_DCI, LVDCI_DV2_18, HSTL_II_DCI, DIFF_HSTL_II_DCI, SSTL18_II_T_DCI, DIFF_SSTL18_II_T_DCI, LVDCI_DV2_15, HSTL_II_DCI_18, DIFF_HSTL_II_DCI_18, SSTL15_DCI, DIFF_SSTL15_DCI, HSLVDCI_18, HSTL_II_T_DCI, DIFF_HSTL_II_T_DCI, SSTL15_T_DCI, DIFF_SSTL15_T_DCI, HSLVDCI_15, HSTL_II_T_DCI_18, DIFF_HSTL_II_T_DCI_18, SSTL135_DCI, DIFF_SSTL135_DCI, SSTL135_T_DCI, DIFF_SSTL135_T_DCI, SSTL12_DCI, DIFF_SSTL12_DCI, SSTL12_T_DCI, DIFF_SSTL12_T_DCI, HSUL_12_DCI, DIFF_HSUL_12_DCI

LVDCI_18, LVDCI_DV2_18, HSLVDCI_18, HSUL_12_DCI, LVDCI_15, LVDCI_DV2_15, HSLVDCI_15, DIFF_HSUL_12_DCI

HSTL_I, DIFF_HSTL_I, SSTL15_R, DIFF_SSTL15_R, HSTL_II, DIFF_HSTL_II, SSTL15, DIFF_SSTL15, HSTL_I_18, DIFF_HSTL_I_18, SSTL135_R, DIFF_SSTL135_R, HSTL_II_18, DIFF_HSTL_II_18, SSTL135, DIFF_SSTL135, SSTL18_I, DIFF_SSTL18_I, SSTL18_II, DIFF_SSTL18_II,

Source: Xilinx data sheet `ug471_7Series_SelectIO.pdf`

Packages for Xilinx Virtex II

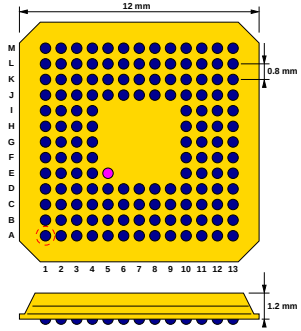
package	CS144	FG256	FG456	FG676	BG575	BG728	FF896	FF1152	FF1517	BF957
pitch (mm)	0.80	1.00	1.00	1.00	1.27	1.27	1.00	1.00	1.00	1.27
size (mm)	12x12	17x17	23x23	27x27	31x31	35x35	31x31	35x35	40x40	40x40
nb. I/O	92	172	324	484	408	516	624	824	1,108	684

FPGA →	XC2V										
package ↓	40	80	250	500	1000	1500	2000	3000	4000	6000	8000
CS144	88	92	92	-	-	-	-	-	-	-	-
FG256	88	120	172	172	172	-	-	-	-	-	-
FG456	-	-	200	264	324	-	-	-	-	-	-
FG676	-	-	-	-	-	392	456	484	-	-	-
FF896	-	-	-	-	432	528	624	-	-	-	-
FF1152	-	-	-	-	-	-	-	720	824	824	824
FF1517	-	-	-	-	-	-	-	-	912	1 104	1 108
BG575	-	-	-	-	328	392	408	-	-	-	-
BG728	-	-	-	-	-	-	-	516	-	-	-
BF957	-	-	-	-	-	-	624	684	684	684	-

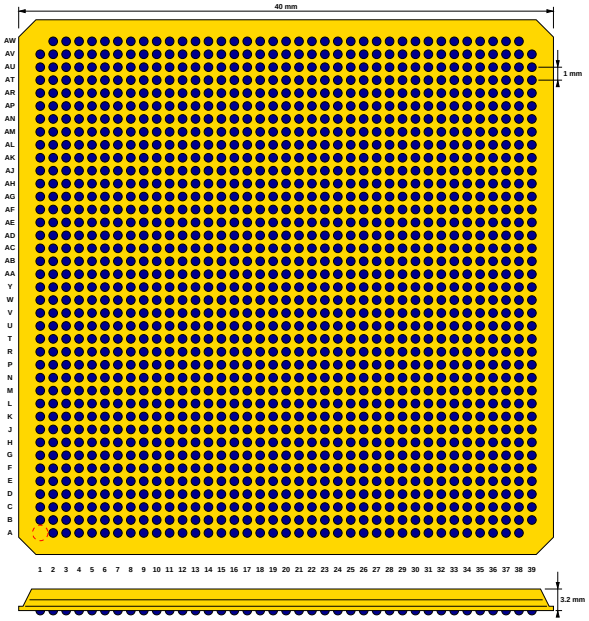
SOURCE: Xilinx data sheet

Some Packages used in FPGAs

CS144 Chip-Scale BGA



FF1517 Flip-Chip Fine-Pitch BGA

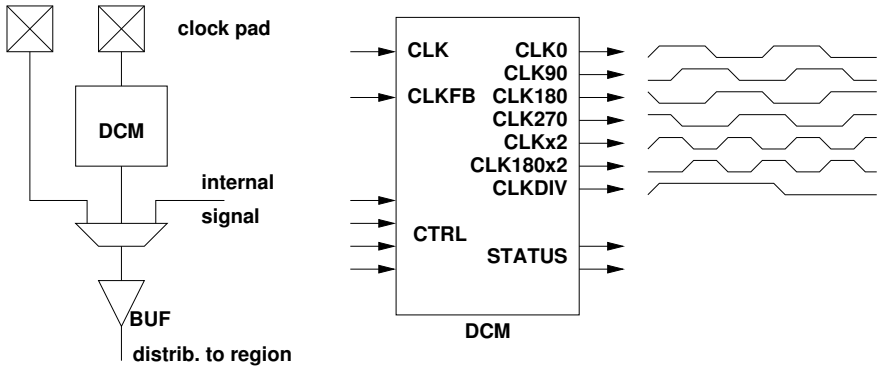


Transceivers in Xilinx Virtex 6 & Virtex 7

Data rates:

type	40 nm		28 nm				
	Spartan 6	Virtex 6	Artix 7	Kintex 7	Virtex 7		
					T	XT	HT
GTP	3.125		6.6				
GTX		6.6		12.5	12.5	12.5	
GTH		11.18				13.1	13.1
GTZ							28.05

Clock Generation in a Virtex II

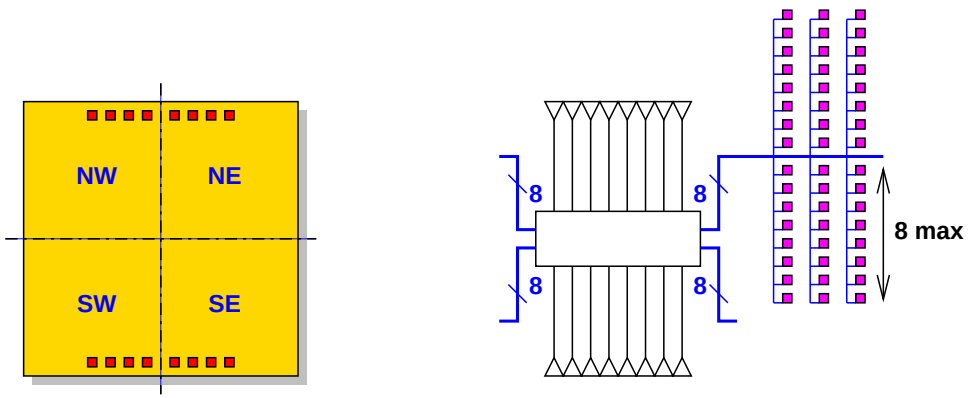


DCM: digital clock manager

Possible clock division in a Virtex II: 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, 16.

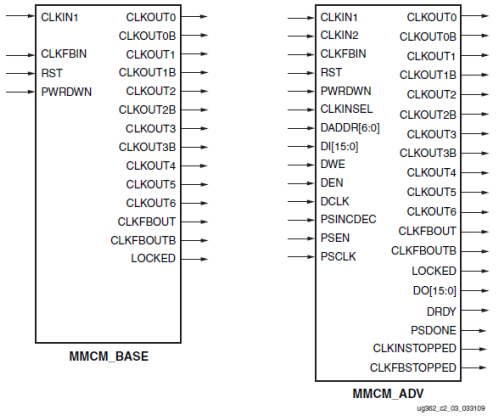
SOURCE: Xilinx data sheet

Clock Distribution in a Virtex II



Source: Xilinx data sheet

Clocking Resources in a Virtex 6 (1/2)



MMCM: Mixed-Mode Clock Manager

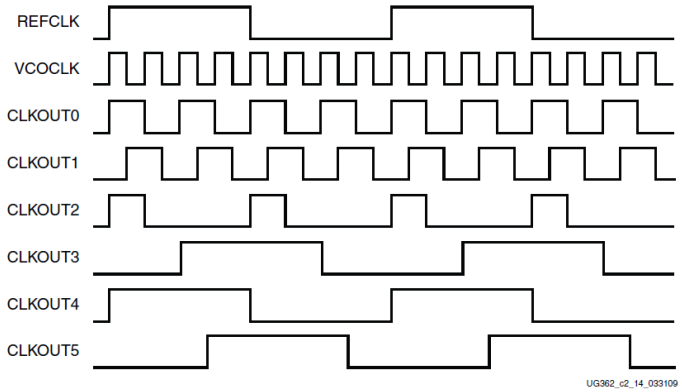
$$F_{out} = F_{in} \times \frac{DI}{DO}$$

6 to 18 clock regions depending on the FPGA size

Source: Xilinx data sheet: Virtex 6 FPGA Clocking Resources (UG362) p. 40

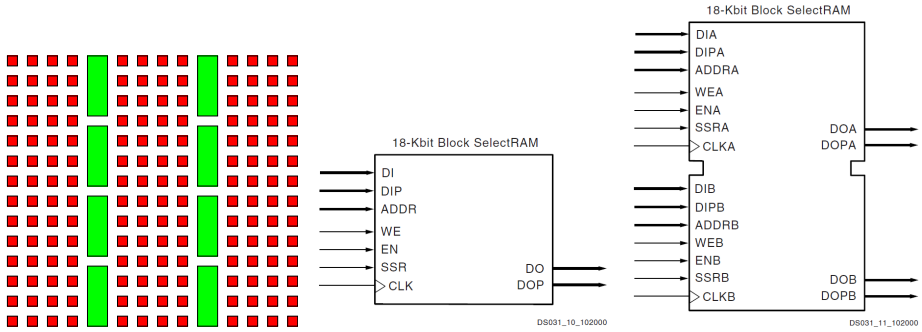
Clocking Resources in a Virtex 6 (2/2)

MMCM Application Example:



Source: Xilinx data sheet: Virtex 6 FPGA Clocking Resources (UG362) p. 61

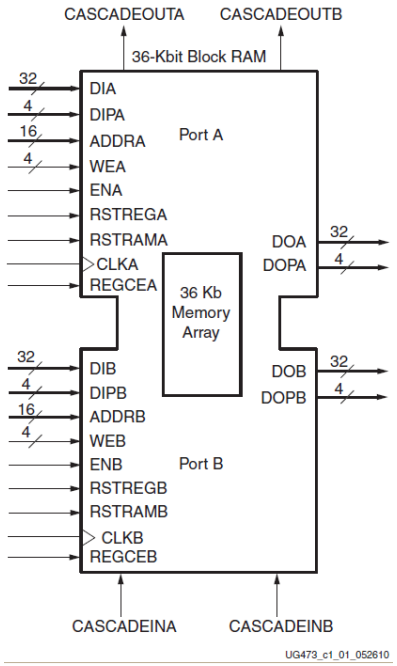
Dedicated Hard Blocks of RAM in a Virtex II



- Single ou dual port 18 Kb BRAM (Block RAM)
- 4 (XC2V40) to 168 (XC2V8000) BRAMs
- Possible configurations for each BRAM:
  16K x 1, 8K x 2, 4K x 4, 1K x 18, 2K x 9, 512 x 36

Source: Xilinx Virtex II data sheet (DS083) pp. 44–46

BRAMs in a Virtex 7



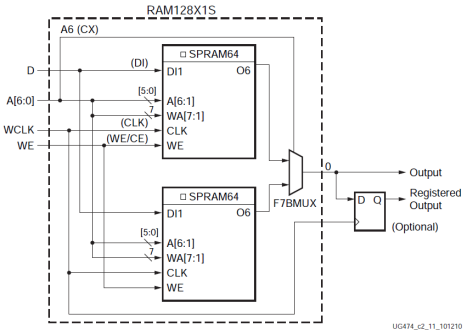
- 36 Kb BRAMs
- 135 (XC7A100T) to 1 880 (XC7VX1140T) BRAMs !!!
- RAM or FIFO configurations
- Cascade of 2 blocks
- ECC configurable support

Source: Xilinx Virtex 7 memory resource data sheet (UG473)

Distributed RAM in a Virtex 7

SLICEMs distributed RAM configuration in a Virtex 7 CLB

#word× wordsize	ports conf.	R	W	# LUT
32×1	S	$@_1$	$@_1$	1
32×1	D	$@_1@_2$	$@_1$	2
32×2	Q	$@_1@_2@_3@_4$	$@_1$	4
32×6	SDP	$@_1$	$@_2$	4
64×1	S	$@_1$	$@_1$	1
64×1	D	$@_1@_2$	$@_1$	2
64×1	Q	$@_1@_2@_3@_4$	$@_1$	4
64×3	SDP	$@_1$	$@_2$	4
128×1	S	$@_1$	$@_1$	2
128×1	D	$@_1@_2$	$@_1$	4
256×1	Q	$@_1@_2@_3@_4$	$@_1$	4



Source: Xilinx Virtex 7 Configurable Logic Block User Guide (UG474)

Yet Another Dedicated Hard Block Type

$$Acc \longleftarrow Acc \pm X \times Y$$

Multiply-and-accumulate is widely used in many applications:

- FIR and IIR filters
- FFT
- Matrix / vector computations
- Polynomial approximations
- Discrete Cosine Transform (DCT)
- ...

$\Longrightarrow$ dedicated blocks

DSP Block Configuration in a Altera Stratix V

Variable precision DSP bloc:

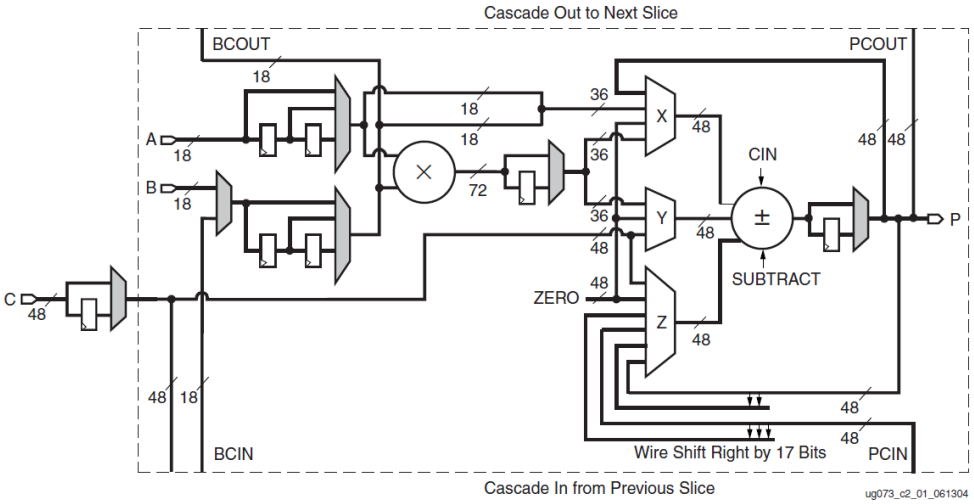
- 2 multipliers 18 × 18 bits per bloc
- pre-adder/subtractor before the multipliers
- adder/subtractor after the multipliers
- e.g. $(a \times b) \pm (c \times d)$
- 64-bit programmable accumulator (split 2 × 32)

in 1 bloc		in 2 blocs	
#op.	op.	#op.	op.
3	$x_{\langle 9\rangle} \times y_{\langle 9\rangle}$	3	$x_{\langle 18\rangle} \times y_{\langle 18\rangle}$
2	$x_{\langle 16\rangle} \times y_{\langle 16\rangle}$	2	$x_{\langle 27\rangle} \times y_{\langle 27\rangle}$
1	$x_{\langle 18\rangle} \times y_{\langle 18\rangle}$ $x_{\langle 27\rangle} \times y_{\langle 27\rangle}$ $x_{\langle 36\rangle} \times y_{\langle 18\rangle}$	1	$x_{\langle 36\rangle} \times y_{\langle 36\rangle}$ $x_{\langle 18\rangle} \times_{\mathbb{C}} y_{\langle 18\rangle}$

$x_{\langle n\rangle}$ denotes a n-bit operand x

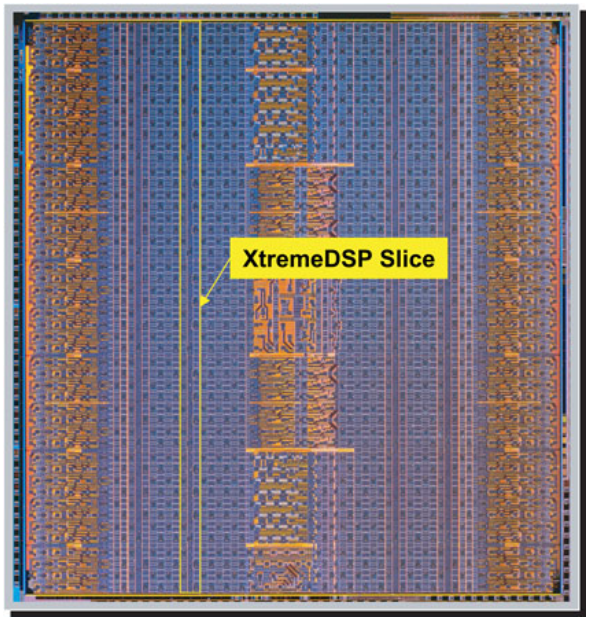
Source: Altera data sheet

Xtreme DSP48 Block in a Virtex 4 FPGA



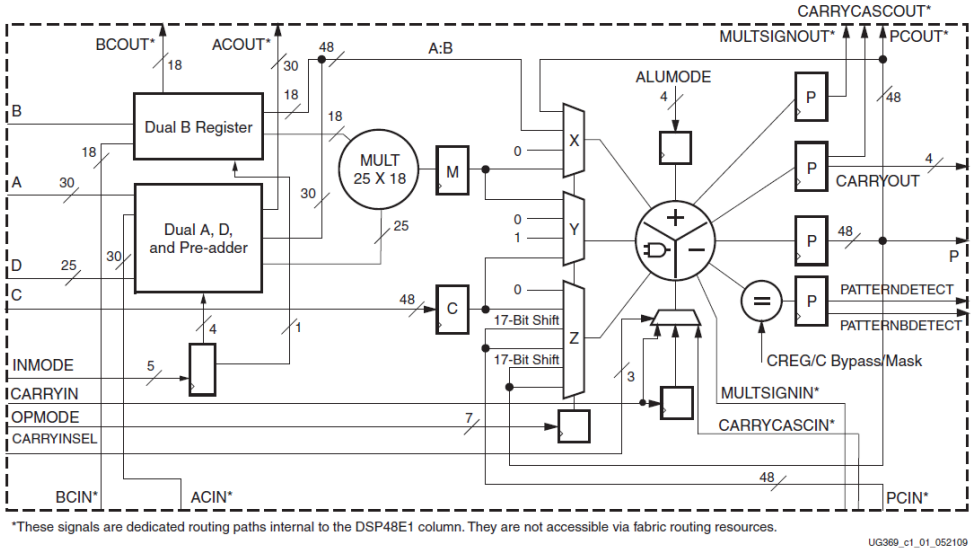
Source: Xilinx XtremeDSP for Virtex-4 FPGAs User Guide (UG073) p. 55

Xtreme DSP Blocks in a Virtex 4 FPGA



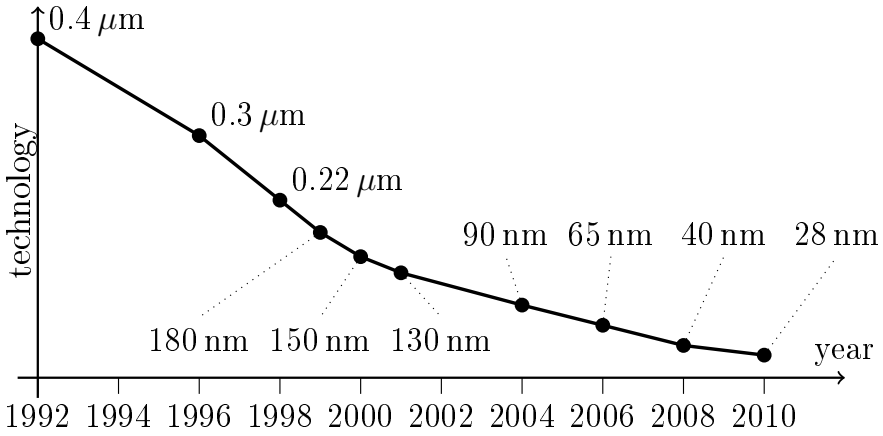
Source: die picture from `http://chipdesignmag.com/display.php?articleId=68&issueId=9`

DSP Block in a Virtex 7 FPGA



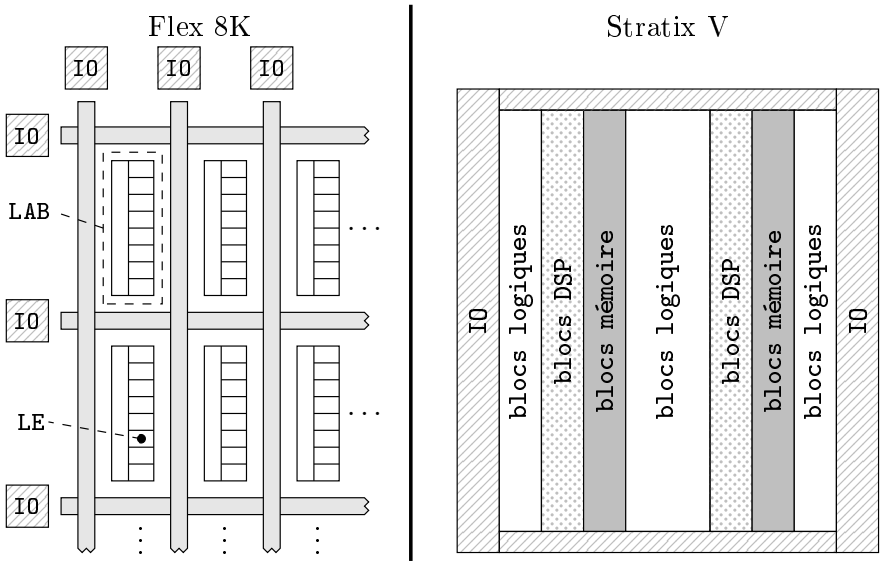
Source: Xilinx 7 Series DSP48E1 Slice User Guide (UG479) p. 12

Technology Evolution for Altera FPGAs



Source: Altera data sheets

Architecture Evolution for Altera FPGAs



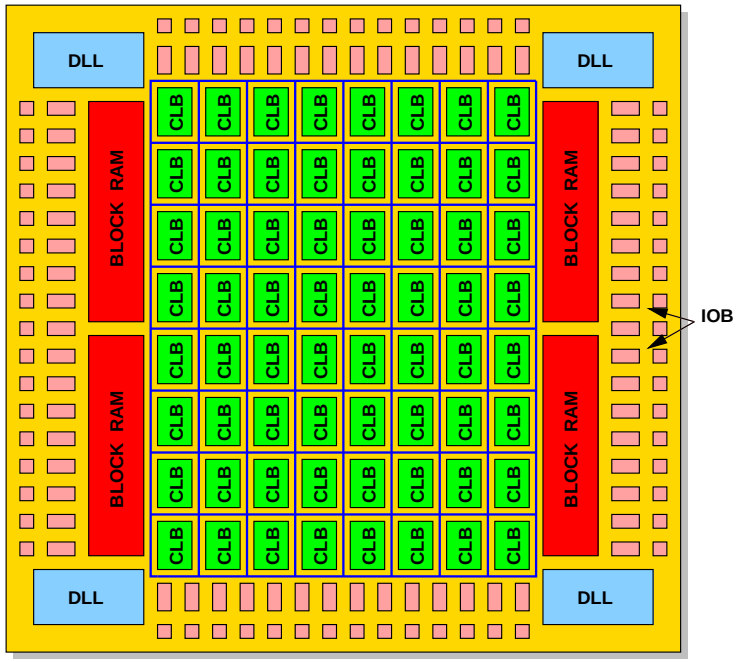
SOURCE: Altera data sheets

Altera FPGAs Evolution

	Stratix				
	I	II	III	IV	V
year	2002	2004	2006	2008	2010
techno. [nm]	130	90	65	40	28
V_{dd} [V]	1.5	1.2	1.1	0.9	0.85
max. freq. [MHz]	350	450	550	600	700
# logic blocks	80 k	180 k	338 k	813 k	950 k
# DSP blocks [18×18]	88	384	768	1 288	4 096
RAM blocks [Mb]	7	9	18	23	33
transceivers	20	20	–	48	66
d.m.t. [Gb·s^{-1}]	3.18	6.37	–	11.3	28
clocks glob./reg.	16/22	16/32	16/88	16/88	16/92

SOURCE: Altera data sheets

Xilinx Spartan II Overview



Xilinx Spartan II FPGAs

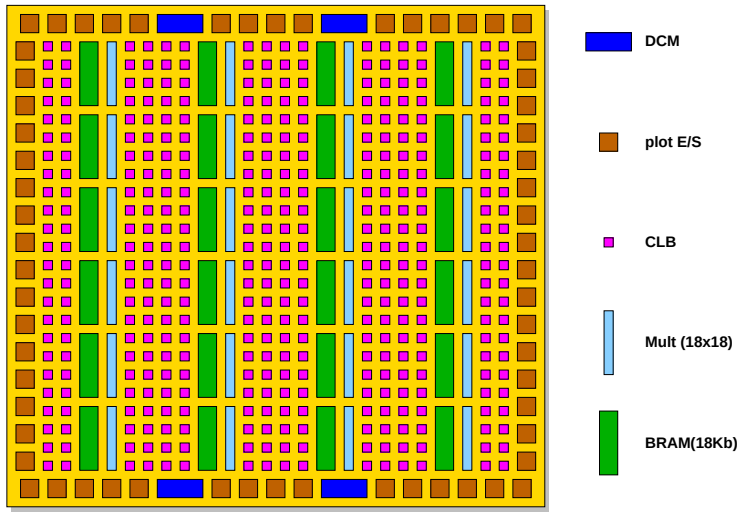
type	# gates	# equiv. gates	matrix L × C	# CLB	# I/O	diff. I/O	DRAM bits	BRAM bits
XC2S50E	1 728	23 000 – 50 000	16 × 24	384	182	83	24 576	32K
XC2S100E	2 700	37 000 – 100 000	20 × 30	600	202	86	38 400	40K
XC2S150E	3 888	52 000 – 150 000	24 × 36	864	265	114	55 296	48K
XC2S200E	5 292	71 000 – 200 000	28 × 42	1 176	289	120	75 264	56K
XC2S300E	6 912	93 000 – 300 000	32 × 48	1 536	329	120	98 304	64K
XC2S400E	10 800	145 000 – 400 000	40 × 60	2 400	410	172	153 600	160K
C2S600E	15 552	210 000 – 600 000	48 × 72	3 456	514	205	221 184	288K

Packages famille Spartan II E : TQ144, PQ208, FT256, FG456, FG676

Configuration bitstream size (in bits):

XC2S50E	XC2S100E	XC2S150E	XC2S200E	XC2S300E	XC2S400E	XC2S600E
630 048	863 840	1 134 496	1 442 016	1 875 648	2 693 440	3 961 632

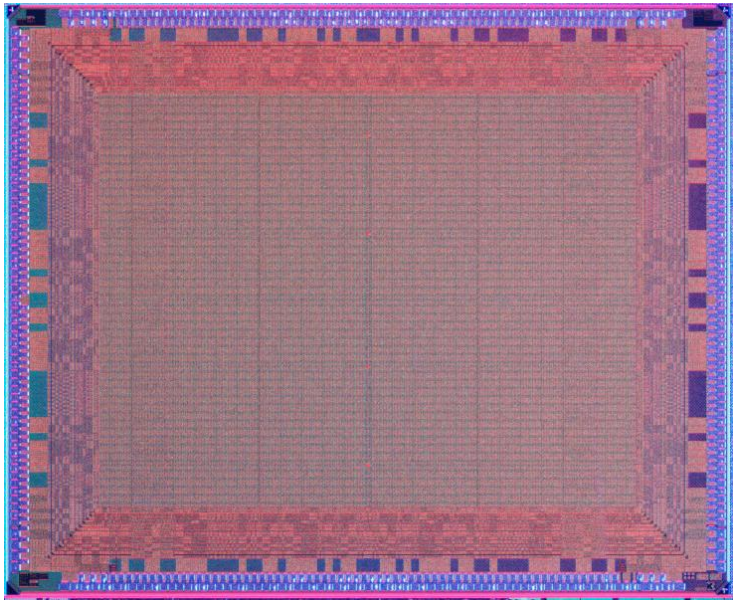
Xilinx Virtex II



Largest device: 112 × 108 CLBs, 168 Mult. 18 × 18 bits, 168 BRAMs, 12 DCMs. Total equiv. ≈ 8 Mgates!

SOURCE: Xilinx data sheets

Xilinx Spartan 3



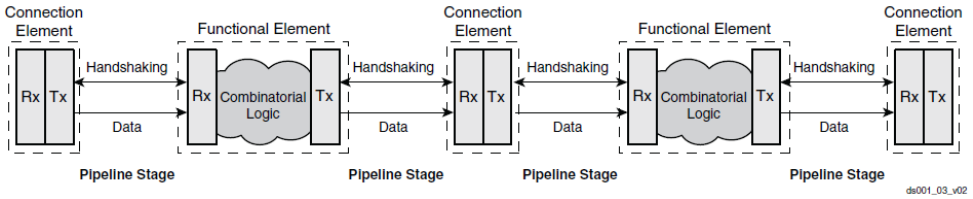
SOURCE: Xilinx web site

Xilinx FPGAs Evolution

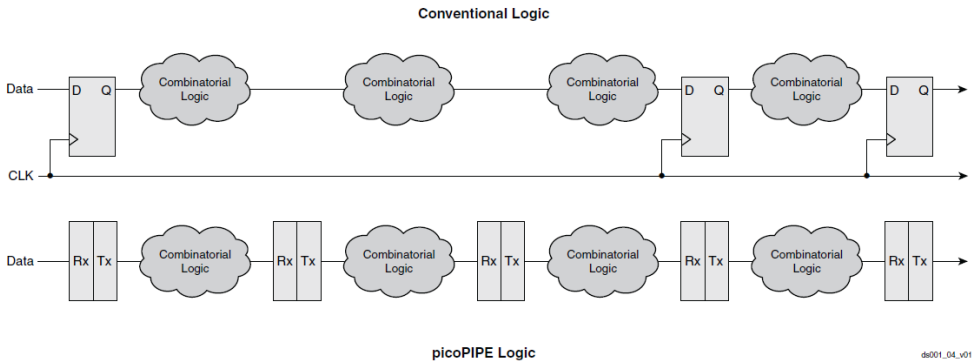
	Virtex					
	—	II	4	5	6	7
year	1998	2001	2005	2006	2009	2011
techno. [nm]	220	130	90	65	40	28
V_{DD}[V]	2.5	1.5	1.2	1.0	1.0	0.9
max. freq. [MHz]	200	400	500	550	600	650
slices	12 k	44 k	89 k	51 k	118 k	178 k
# DSP	—	444	512	1 056	2 016	3 600
blocks RAM [Mb]	0.13	7.9	9.9	18	38	84
# transceivers	—	—	24	48	48	96
throughput [Gb·s^{-1}]	—	—	6.5	6.5	11	28
I/O	512	1 164	960	1 200	1 200	1 200

SOURCE: Xilinx data sheets

Achronix Speedster FPGA 1.5 GHz (1/2)

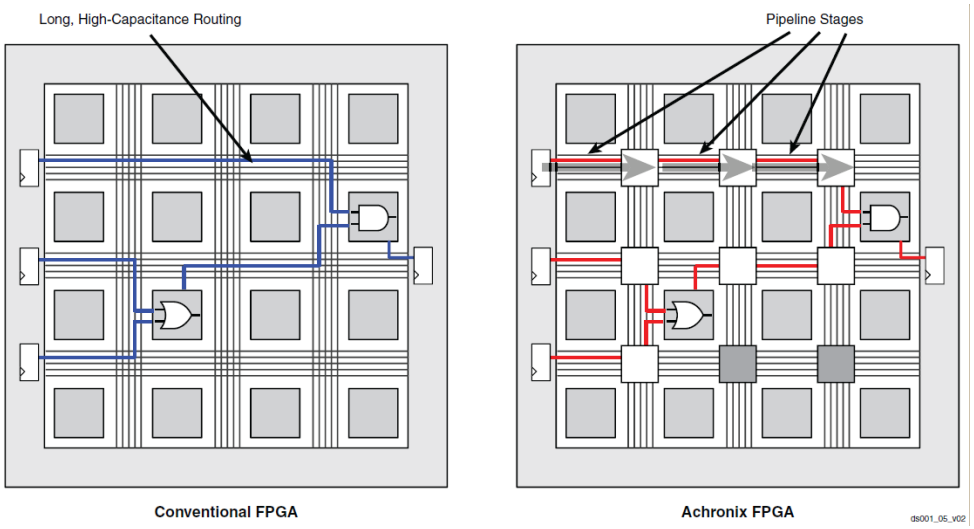


SOURCE: Achronix Speedster FPGA Family (DS001) p. 4



SOURCE: Achronix Speedster FPGA Family (DS001) p. 6

Achronix Speedster FPGA 1.5 GHz (2/2)



SOURCE: Achronix Speedster FPGA Family (DS001) p. 6

Part III

Processors in FPGAs

Processors in FPGAs

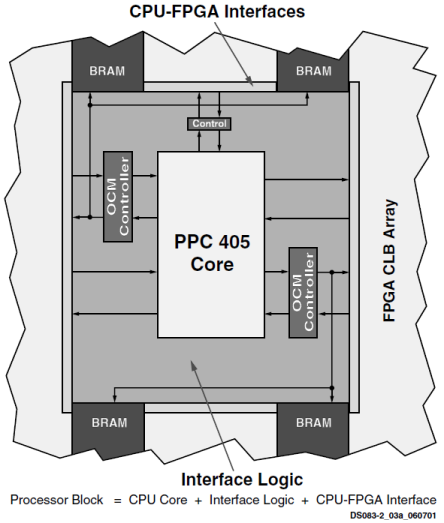
Processors are widely used in electronic systems and FPGAs:

- the main processor at system level (32-bit, MMU, cache, "OS friendly", ...)
- small processors (8/16-bit) used for local control (for coprocessors/accelerators), "smart FSMs"
- FPGAs are larger and larger but implementing embedded processors is still costly (area and design time)
- Embedded and low-power systems $\Longrightarrow$ single chip solution

Two solutions for embedded processors in FPGAs:

- dedicated hard blocks processor core(s)
- soft-core processors (synthezised on the FPGA resources)

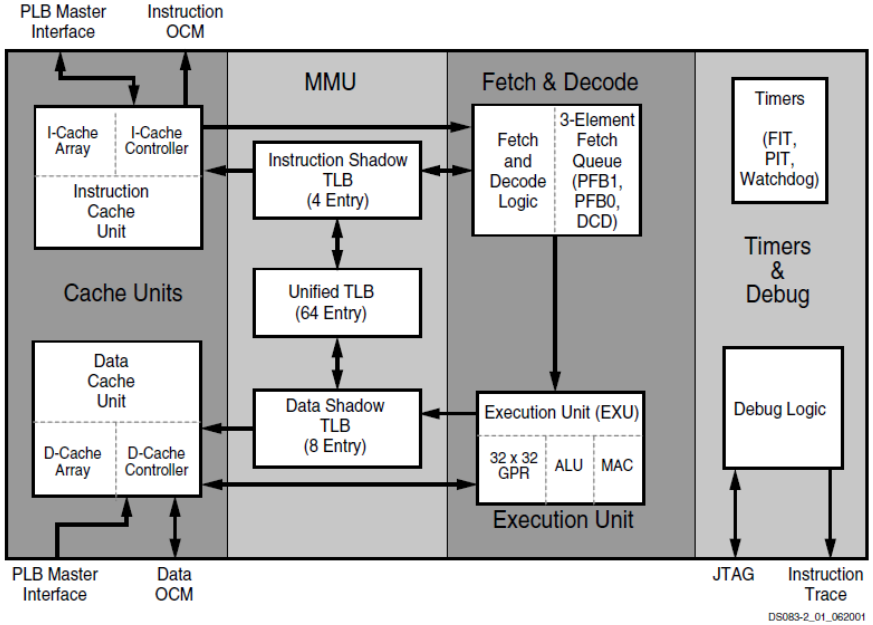
PowerPC 405 in a Xilinx Virtex II (1/2)



- 0.13 μm implementation of the IBM PowerPC 405D4 core
- 300 MHz+
- 32-bit address modes
- 64-bit operations

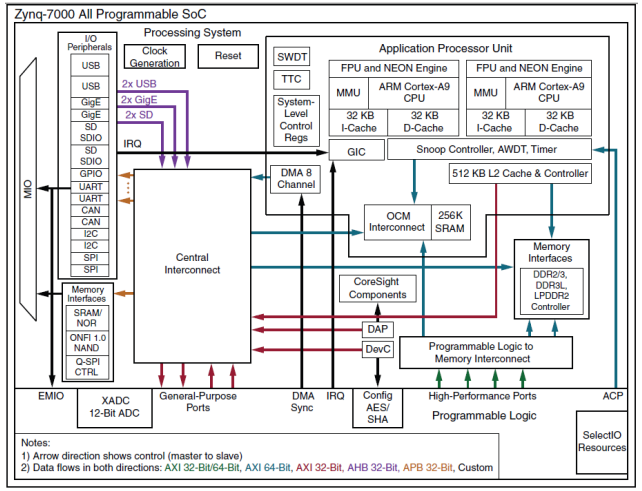
SOURCE: xilinx data sheet (DS083) p. 29

PowerPC 405 in a Xilinx Virtex II (2/2)



SOURCE: xilinx data sheet (DS083) p. 63

Xilinx Zynq 7000



SOURCE: xilinx data sheet (DS190)

- hard block: dual-core ARM Cortex A9
- 28 nm implementation
- 667, 733, 800 MHz and 1 GHz
- 1GB address space
- 64-bit operations
- Cache L1 I 32 KB 4-way set-associative
- Cache L1 D 32 KB 4-way set-associative
- Cache L2 I+D 512 KB 8-way set-associative
- On-chip boot ROM
- 256 KB on-chip RAM

Hard Processors Evolution in Xilinx FPGAs

	Virtex			Zynq
	II Pro	4	5	7000
processor	PowerPC 405	PowerPC 405	PowerPC 440	ARM Cortex A9
#core	1 or 2	1 or 2	1 or 2	1 double
max. freq. [MHz]	300	450	550	800
#pipe. stages	5	5	7	8
L1 [Ko]	16I+16D	16I+16D	32I+32D	32I+32D
L2 [Ko]	—	—	—	512
o.o.o.	no	no	yes	yes
FPU	no	no	no	32/64 b

SOURCE: Xilinx data sheets

Soft-Core Processors

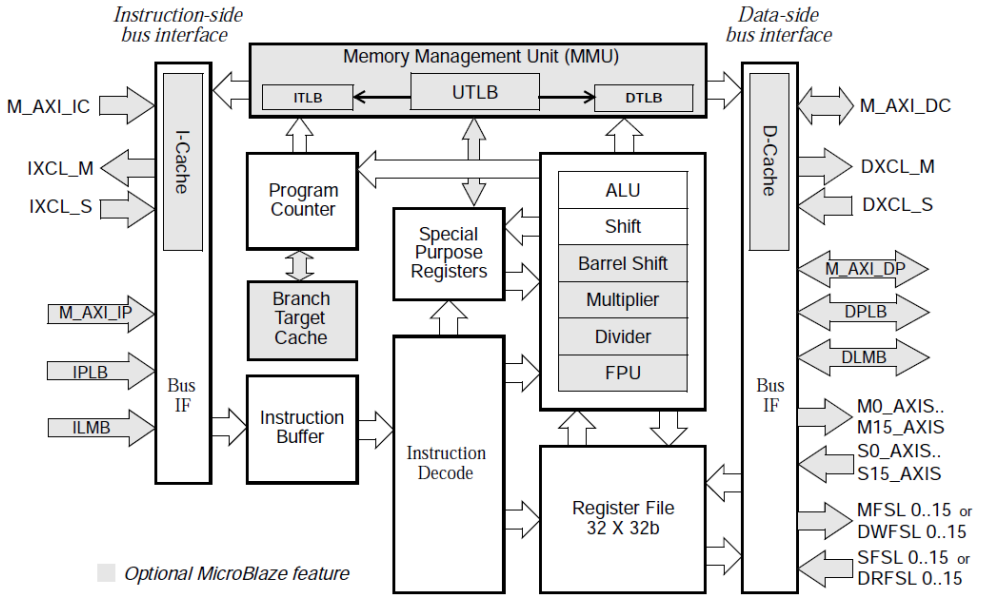
Definition: embedded processor implemented using typical FPGA resources (logic blocks, RAM blocks, DSP blocks,...)

Examples:

processor	archi.	#bit	pipe. stages	CPI	MMU	FPU	license
NIOS II f	NIOS II	32	6	1	yes	opt.	prop. Altera
NIOS II s	NIOS II	32	5	1	no	no	prop. Altera
NIOS II e	NIOS II	32	no	6	no	no	prop. Altera
MicroBlaze	MicroBlaze	32	3 / 5	1	opt.	opt.	prop. Xilinx
PicoBlaze	PicoBlaze	8	no	2	no	no	prop. Xilinx
Cortex M1	ARM V6	32	3	1	no	yes	prop. ARM
LEON 2	SPARC V8	32	5	1	yes	yes	LPGL
LEON 3	SPARC V8	32	7	1	yes	yes	GPL
OpenRISC 1200	OpenRISC 1000	32	5	1	yes	yes	LGPL

▪ ▪ ▪

Xilinx MicroBlaze (1/2)



SOURCE: Xilinx MicroBlaze Processor Reference Guide p. 9

Xilinx MicroBlaze (2/2)

Supported FPGAs: Spartan 3/6, Virtex-4/5/6/7, Artix-7, Kintex-7, Zynq-7000

Various supported and optional features:

- Execution Hardware Acceleration
- Instruction Set Extensions
- Cache size configurable: 2kB to 64kB (BRAM)
- Microcache size configurable: 64B to 1024B (DRAM)
- Direct mapped write-through or write-back operation
- Branch optimizations and prediction logic
- Error Correction Codes (ECC)
- Parity protection on internal BRAMs and caches
- 32-bit Floating Point Unit (FPU) IEEE 754
- Memory Management Unit (MMU)
- MPU mode for region protection for secure RTOS applications
- JTAG control via a debug support core

SOURCE: Xilinx LogiCORE IP MicroBlaze (DS865)

Part IV

References

Journals

- *ACM Transactions on Reconfigurable Technology and Systems* (TRETS)
- *IEEE Transactions on Circuits and Systems* (TCAS)
- *IEEE Transactions on Computers* (TC)
- *IEEE Transactions on VLSI Systems* (TVLSI)
- ...

Conferences

Domain specific conferences:

- FPGA: *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*
- FCCM: *IEEE International Symposium on Field-Programmable Custom Computing Machines*
- FPL: *International Conference on Field Programmable Logic and Applications*
- FPT: *International Conference on Field-Programmable Technology*

Sessions in general conferences:

- DAC: *Design Automation Conference*
- DATE: *Design, Automation, and Test in Europe conference*
- CHES: *Workshop on Cryptographic Hardware and Embedded Systems*

Articles and Chapters I

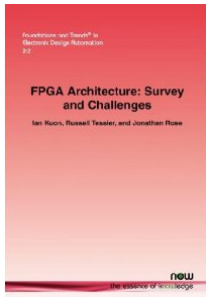
S. Brown.
FPGA architectural research: a survey.
IEEE Design & Test of Computers, 13(4):9–15, December 1996.

I. Kuon, R. Tessier, and J. Rose.
FPGA architecture: Survey and challenges.
Foundations and Trends in Electronic Design Automation, 2(2):135–253, 2008.

O. Sentieys and A. Tisserand.
Architectures reconfigurables FPGA.
In *Technologies logicielles Architectures des systèmes*, number H 1 196, pages 1–22. Techniques de l'Ingénieur, August 2012.

Books on FPGAs (1/2)

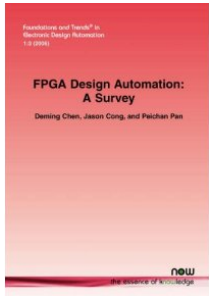
FPGA Design
Best Practices for Team-Based Design
Philip Simpson
2010
Springer
ISBN: 978–1–4419–6339–0



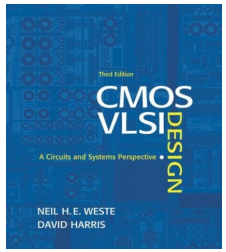
FPGA Architecture
Survey and Challenges
Russell Tessier, Jonathan Rose and Ian Kuon
2008
Now Publishers Inc
ISBN: 978–1601981264

Books on FPGAs (2/2)

FPGA Design Automation
A Survey
Deming Chen, Jason Cong and Peichen Pan
2006
Now Publishers Inc
ISBN: 978-1933019383



Good Books: Circuit Technology & Design



CMOS VLSI Design
A Circuits and Systems Perspective
Neil Weste and David Harris
3rd edition, 2004
Addison Wesley
ISBN: 0–321–14901–7

Micro et nano-électronique
Bases, Composants, Circuits
Hervé Fanet
2006
Dunod
ISBN: 2–10–049141–5

Other Topics on FPGAs

- Configuration
- Partial dynamic reconfiguration
- Low-power aspects
- Security aspects
- Programming
- CAD tools
- FPGA to ASIC conversion solutions
- ...

The end, some questions ?

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- CAIRN Group `http://www.irisa.fr/cairn/`
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Thank you