Semiconductor Industry Conference

October 14–16, 1985
Sheraton El Conquistador
Tucson, Arizona

Nielsen Dataquest

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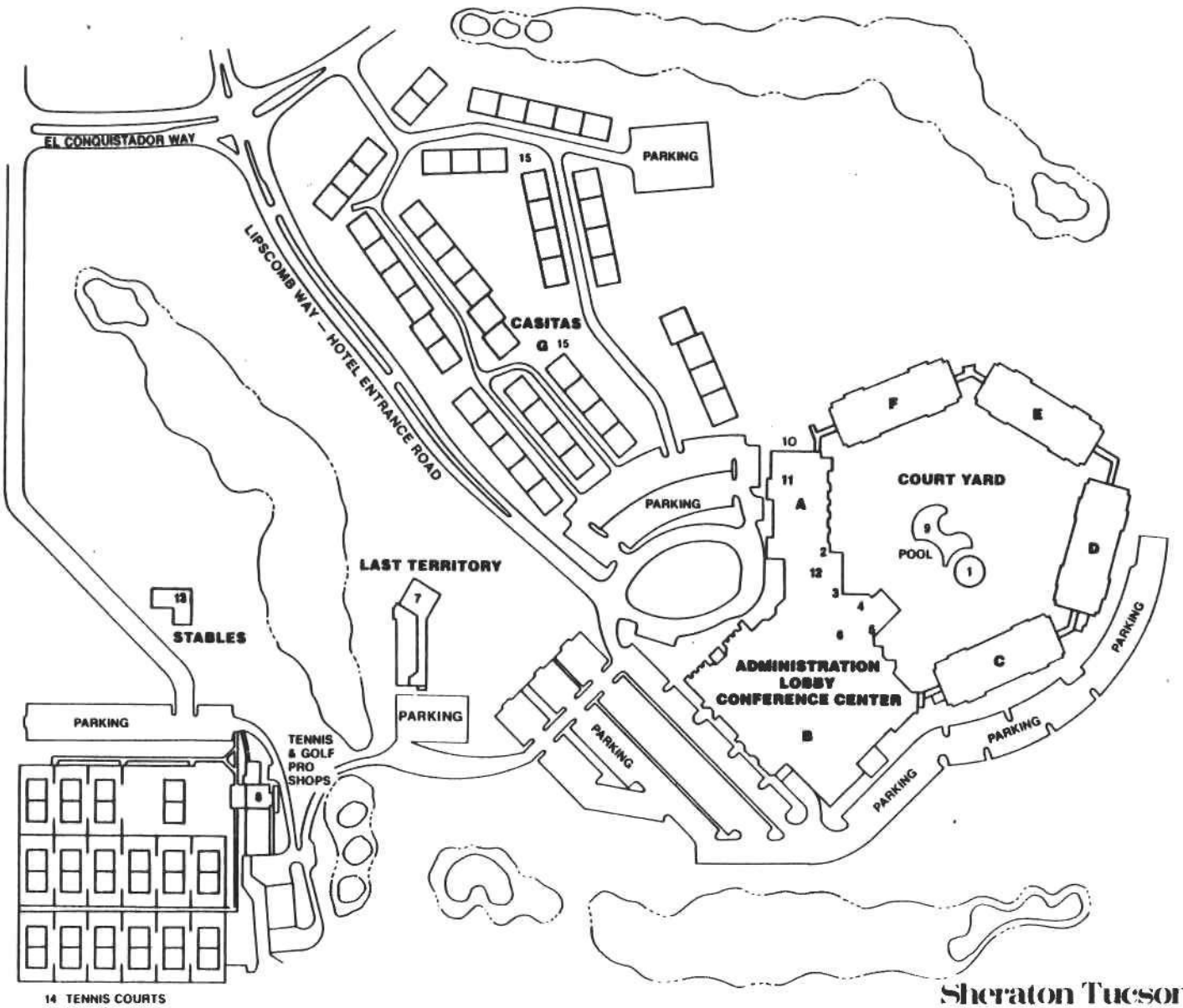

A – Main Lobby
Administrative, Sales, Catering Offices

B. – Conference Center
White Dove Restaurant
Sundance Cafe
Victoria's Lounge
Russell Gallery

C. – Guest Rooms
3100–3126
4100–4127
5100–5127

D. – Guest Rooms
2200–2226
3200–3227
4200–4227

E. – Guest Rooms
1300–1327
2300–2327
3300–3327

F. – Guest Rooms
1401–1427
2400–2427
3400–3427

G. – Guest Room
CASITAS
1500–1586
1600–1686

1. **Pool Snack Bar**
2. **Lobby Lounge**
3. **Russell Gallery Lounge**
4. **Victoria's Lounge**
5. **Sundance Cafe**
6. **White Dove Restaurant**
7. **Last Territory**
8. **Golf/Tennis Snack Bar**
9. **Swimming Pool/Jacuzzi**
10. **Health Club**
11. **Hair Salon**
12. **Budget Rent A Car**
    Indian Village
    Elson's News & Gifts
13. **Stables**
14. **Tennis**
    Racquetball
15. **Casita Jacuzzi's**

Sheraton Tucson El Conquistador
Golf & Tennis Resort

SHERATON HOTELS, INNS & RESORTS WORLDWIDE
10000 NORTH ORACLE ROAD, TUCSON, ARIZONA 85737 (602) 742-7000

Nielsen Dataquest

1985 SEMICONDUCTOR INDUSTRY CONFERENCE
An Industry in Transition

October 14–16

Sheraton El Conquistador
Tucson, Arizona

SUNDAY, October 13

3:00 p.m. to 9:00 p.m.	Registration	*Topaz/Opal Foyer*
7:00 p.m. to 9:00 p.m.	Cocktails	*Coronado Room*

MONDAY, October 14

7:30 a.m.	Buffet Breakfast	*Turquoise Room*
7:30 a.m.	Registration Continues	*Topaz/Opal Foyer*
9:00 a.m.	**Welcome Address** Howard Z. Bogert Vice President and Director Semiconductor Industry Group Dataquest Incoporated Robert McGeary Director Semiconductor Equipment and Materials Service Dataquest Incorporated	*Topaz/Opal Rooms*

INDUSTRY ISSUES

9:15 a.m.	**Consumption, Capacity, Catastrophe** Robert McGeary Howard Z. Bogert Dataquest Incorporated	*Topaz/Opal Rooms*
9:45 a.m.	**ASICs in Japan** K.K. Yawata President Nihon LSI	*Topaz/Opal Rooms*
10:15 a.m.	Coffee Break	*Opal Foyer*
10:45 a.m.	**From Captive to Merchant Supplier** Dr. James Van Tassel Vice President NCR Corporation	*Topaz/Opal Rooms*
11:15 a.m.	**Think Tank and Silicon Crank: Partners In Innovation** Art Collmeyer President Weitek Corporation	*Topaz/Opal Rooms*
11:45 a.m.	**Cost Driven—Customer Driven** F. Joseph Van Poppelen Vice President Semiconductor Marketing National Semiconductor Corporation	*Topaz/Opal Rooms*
12:30 p.m.	Lunch	*Turquoise Room*

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CONCURRENT SESSIONS

FOCUS SESSIONS

2:00 p.m. **Silicon Compiler Panel Discussion** ..... *Topaz Room*

- Andy Prophet
  Senior Industry Analyst
  Semiconductor Industry Service
  Dataquest Incorporated
- Richard N. Gossen, Jr.
  President and CEO
  Silicon Design Labs
- Walter Curtis
  Vice President, Marketing
  Silicon Compilers, Inc.
- Mike Hackworth
  President and CEO
  Cirrus Logic
- Douglas Fairbairn
  Vice President
  Design Technology
  VTI
- George C. Cone
  Senior Vice President
  Seattle Silicon Technology, Inc.

2:00 p.m. **An Industry Transition: An Application Market Perspective** ..... *Opal Room*

- Anthea Stratigos
  Product Manager
  Semiconductor Application Markets
  Dataquest Incorporated
- Howard Z. Bogert
  Dataquest Incorporated

EMERGING TECHNOLOGY

2:00 p.m. **X-ray Lithography** ..... *Juniper Room*
Carrol Fencil
Director of Government Systems
Perkin-Elmer Corporation

2:40 p.m. **Silicon Technology** ..... *Juniper Room*
Haskell Waddle
Vice President, Commercial
Monsanto Electronic Materials Corporation

3:20 p.m. Coffee Break ..... *Opal Foyer*

3:50 p.m. **Image Verification—The Key to High Yields** ..... *Juniper Room*
Kenneth Levy
President
KLA Corporation

4:30 p.m. **Equipment and Materials Frontiers** ..... *Juniper Room*
Robert McGeary
Dataquest Incorporated

6:00 p.m. Cocktails ..... *Last Territory*

7:00 p.m. Dinner—Western Barbecue ..... *Last Territory*

9:00 p.m. Informal discussion and hosted refreshments ..... *Last Territory*

TUESDAY, October 15

7:45 a.m. Buffet Breakfast ..... *Turquoise Room*

EMERGING MARKETS

9:00 a.m. **Directions in VLSI** ..... *Topaz/Opal Rooms*
Dave House
General Manager
Microcomputer Group
Intel Corporation

9:30 a.m. **Application-Specific Memories—The New Memory Market** ..... *Topaz/Opal Rooms*
Alex Au
President
Vitelic Corporation

10:00 a.m. Coffee Break ..... *Opal Foyer*

10:30 a.m. **ASICs in the Analog World** ..... *Topaz/Opal Rooms*
Alan Grebene
President
Micro-Linear Corporation

11:00 a.m. **Strategies for Effective Silicon Use** ..... *Topaz/Opal Rooms*
Eli Harari
President
Wafer Scale Integration, Inc.

11:30 a.m. **Venture Capital in Transition** ..... *Topaz/Opal Rooms*
Wallace F. Davis
General Partner
Alpha Partners

12:15 p.m. Lunch ..... *Turquoise Room*

CONCURRENT SESSIONS

FOCUS SESSIONS

2:00 p.m. **Billion-transistor VLSI Architectures** ..... *Topaz/Opal Rooms*
Panel Discussion

- Mel Thomsen
  Associate Director
  Semiconductor Industry Service
  Dataquest Incorporated
- Stanley Mazor
  Manager
  Applications Engineering
  Silicon Compilers, Inc.
- John Banning
  Independent Computer Consultant
- Skip Stritter
  Vice President, Engineering
  MIPS Computer Systems
- Dan Ling
  Manager, Micro Systems
  IBM Thomas J. Watson Research Center

Industry Athletic Challenge—10K Run

3:30 p.m. Bus Departs ..... *Front Entrance of Hotel*

EMERGING MANUFACTURING

2:00 p.m. **Automated Fabrication** ..... *Seminar Room*
Dr. Hiroyoshi Komiya
Deputy Manager
Mitsubishi Electronics

2:40 p.m. **World-class Manufacturing** ..... *Seminar Room*
Dr. James Burnett
President
Institute for Microcontamination Control

3:20 p.m. Coffee Break ..... *Opal Foyer*

3:50 p.m. **Surface Mount** ..... *Seminar Room*
Nikita Andreiev
Director, Educational Group
AWI Corporation

4:30 p.m. **Computer-integrated Manufacturing** ..... *Seminar Room*
Joseph Grenier
Senior Industry Analyst
Semiconductor Equipment and Materials Service
Dataquest Incorporated

6:00 p.m. Cocktails ..... *Ballroom Foyer*

7:00 p.m. Dinner ..... *Turquoise Room*

8:30 p.m. **Dinner Speaker** ..... *Turquoise Room*
Lawrence Chimerine
Chairman and Chief Economist
Chase Econometrics

9:30 p.m. Informal discussion and hosted refreshments ..... *Topaz Room*

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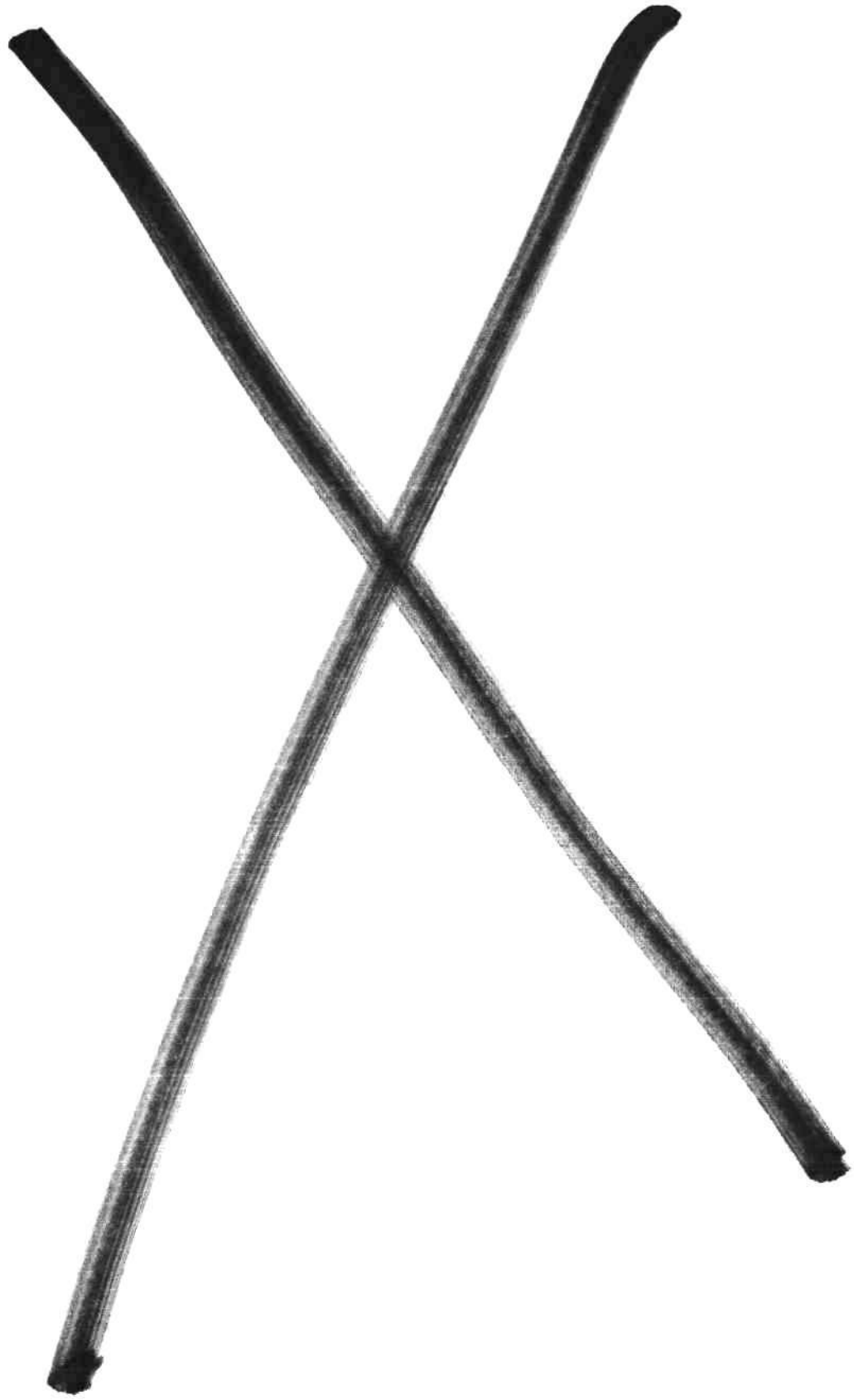
WEDNESDAY, October 16

7:45 a.m.	Buffet Breakfast	*Turquoise Room*
	LONG-TERM ISSUES	
9:00 a.m.	**Trade Issues in Semiconductors** Clyde V. Prestowitz Counselor to the Secretary U.S. Department of Commerce	*Topaz/Opal Rooms*
9:30 a.m.	**SRC and its Role in the Transition** Larry Sumney President Semiconductor Research Corporation	*Topaz/Opal Rooms*
10:00 a.m.	**Challenges in Automotive Electronics** Jerome G. Rivard Chief Engineer Ford Motor Company	*Topaz/Opal Rooms*
10:30 a.m.	Coffee Break	*Opal Foyer*
11:00 a.m.	**Promises and Deliveries—Meeting Semiconductor Commitments** Bengt Soderberg Vice President, Group Purchase Division Telefonaktiebolaget LM Ericsson	*Topaz/Opal Rooms*
11:30 a.m.	**The Future of Gallium Arsenide Integrated Circuits** Anthony Livingston Vice President Gigabit Logic	*Topaz/Opal Rooms*
12:00 Noon	Conference Conclusion	*Topaz/Opal Rooms*
12:15 p.m.	Buffet Luncheon	*Turquoise Room*



Nielsen Dataquest

SEMICONDUCTOR INDUSTRY/SEMICONDUCTOR EQUIPMENT AND MATERIALS INDUSTRY CONFERENCE
Evaluation Questionnaire
Tucson, Arizona
October 13–16, 1985

Thank you for attending our Semiconductor Industry/Semiconductor Equipment and Materials Industry Conference. Would you please assist us in planning our next conference by completing and returning this questionnaire?

1. Please rate each presentation on a scale of 1 to 10 (where 10 is highest in terms of your approval):

	CONTENT (1 to 10)	DELIVERY (1 to 10)	COMMENTS (Use reverse side if necessary)
McGeary/Bogert, *Consumption/Capacity/Catastrophe*			
Yawata, *ASICs in Japan*			
Van Tassel, *Captive to Merchant Suppliers*			
Collmeyer, *Think Tank and Silicon Crank*			
Van Poppelen, *Cost-Customer Driven*			
Focus Sessions: Silicon Compiler Panel Discussion			
Prophet			
Gossen			
Curtis			
Hackworth			
Fairbairn			
Cone			
An Industry Transition			
Stratigos			
Bogert			
Fencil, *X-ray Lithography*			
Waddle, *Silicon Technology*			
Levy, *Image Verification*			
McGeary, *Equipment/Materials Frontiers*			
House, *Directions in VLSI*			
Au, *Application-Specific Memories*			
Grebene, *ASICs in the Analog World*			
Harari, *Strategies/Silicon Use*			
Davis, *Venture Capital in Transition*			

(over)

Dataquest Incorporated, A Subsidiary of A.C. Nielsen Company / 1290 Ridder Park Drive / San Jose, CA 95131 / (408) 971-9000 / Telex 171973

Focus Sessions:
Billion-transistor VLSI Architectures
Panel Discussion

- **Thomsen** _____ _____ _____
- **Mazor** _____ _____ _____
- **Banning** _____ _____ _____
- **Stritter** _____ _____ _____
- **Ling** _____ _____ _____

Komiya, *Automated Fabrication* _____ _____ _____

Burnett, *World Class Manufacturing* _____ _____ _____

Andreiev, *Surface Mount* _____ _____ _____

Grenier, *Computer-Integrated Manufacturing* _____ _____ _____

Dinner Speaker
Chimerine _____ _____ _____

Prestowitz, *Trade Issues* _____ _____ _____

Sumney, *SRC—Role in the Transition* _____ _____ _____

Rivard, *Challenges—Automotive Electronics* _____ _____ _____

Soderberg, *Semiconductor Commitments* _____ _____ _____

Livingston, *Gallium Arsenide ICs* _____ _____ _____

2. Overall Meeting Rating: _____ _____ _____

3. How would you rate the conference facilities (1 to 10)?

   Location ____ Guest Rooms ____ Meals ____ Meeting Rooms ____ Recreational Facilities ____

4. Topics that would be of interest to you for future Semiconductor Industry/Semiconductor Equipment and Materials Industry Conferences:

   _____

   _____

   _____

5. Comments: _____

   _____

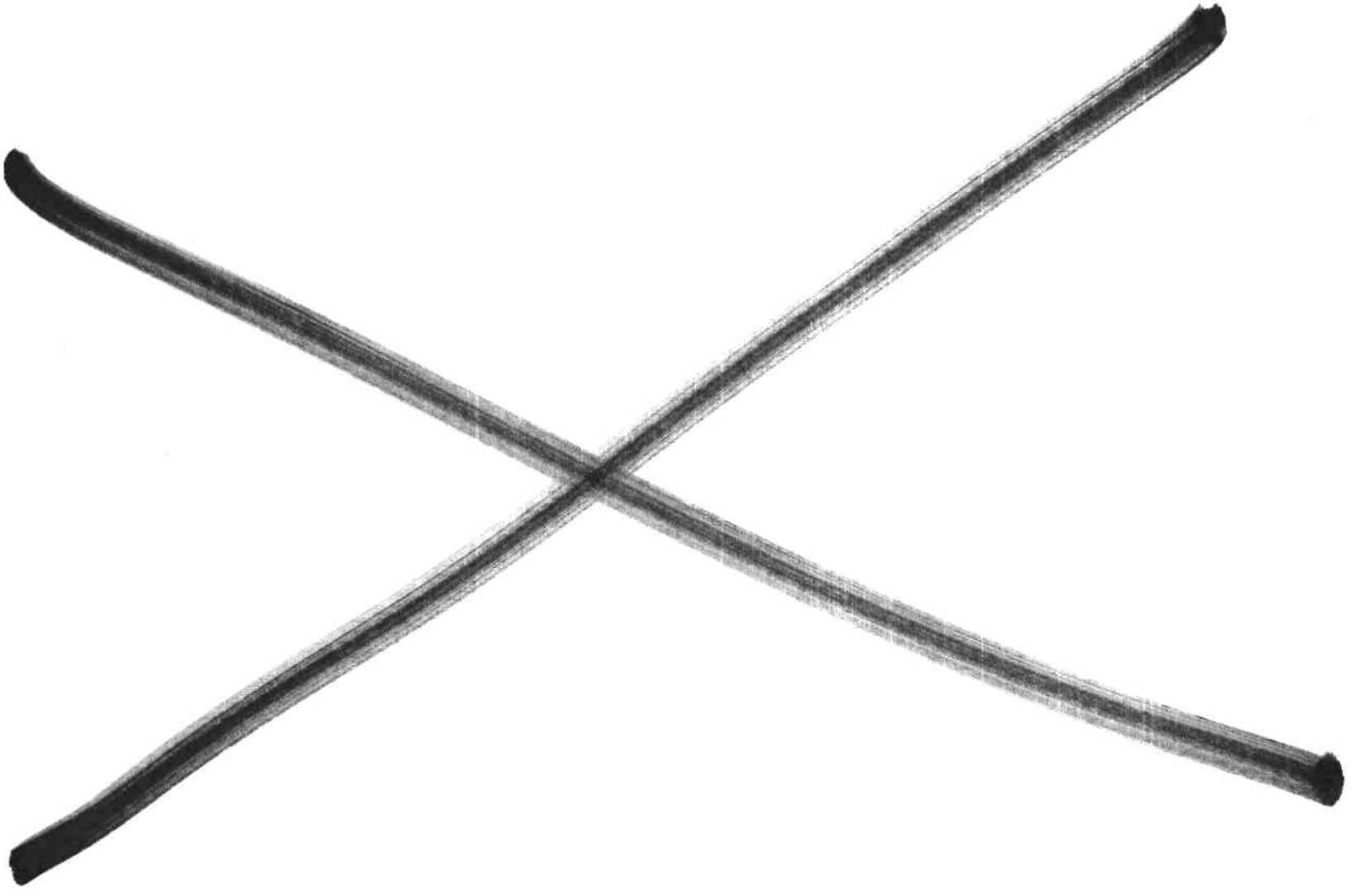
   _____

6. Your primary interest in the Semiconductor Industry/Semiconductor Equipment and Materials Industry Conference is as a:

   Manufacturer _____ Service Vendor _____ User _____ Financial Analyst _____

   Other _____
   (please specify)

_____
Name and Company (optional)



Nielsen Dataquest

SEMICONDUCTOR INDUSTRY SERVICE CONFERENCE
October 14 through 16, 1985
TUCSON, ARIZONA

List of Attendees

AT&T	Stephen Knight, Division Manager, Corporate Strategy
AT&T Bell Laboratories	Y.S. Chen, Deparment Head, Integrated Circuit Customer Service William Evans, Director, Computer Aided Design & Test Laboratory James Goldey, Director Richard Jacobs, Director, VLSI Design Laboratory Robert Melin, Supervisor Ken Poole, Department Head
AT&T Technologies, Inc.	Sara Jane Koperski, Manager, Business Planning Richard O'Malley, Director, Product Line Planning & Management Edward Walker, Jr., Product Manager, Electronic Components
AWI Corporation	Nikita Andreiev, Director, Educational Group
Adler & Company	Dan O'Neill, Venture Manager
Aerospatiale	Pierre Paqueron
Aetna Life and Casualty	Robert Finch, Research Manager
Air Products & Chemicals, Inc.	John Bakey, Regional Marketing Manager Burt Lancaster, Industry Manager Ralph Richardson, Manager Robert Shay, Manager, Research Electronic Gases
Alan Patricof Associates	Lewis Solomon, Executive Vice President Ruth Solomon

Alpha Partners	Wallace Davis, General Partner Lu Davis
Amoco Corporation	Kent Jensen, Program Director
Applied Materials, Inc.	Thomas Bowman, Director, Strategic Marketing Dennis Hunter, Assist to President for Srategic Planning
Applied Micro Circuits Corporation	Marc Friedmann, Strategic Marketing Manager
Arthur Young & Company	Al Crawford, Partner Roger Dunbar, Partner
Associated Venture Investors	Peter Wolken, President
Atom Science	Norbert Thonnard
Bacher GmbH	Willi Bacher, President Ellen Bacher
Bank of America	Timothy Bottoms, Group Vice President, High Tech Division Don Cvietusa, Vice President Mark Verissimo, Vice President
Bank of Boston	Lisa Green, Loan Officer Mark Udem, Vice President
Bank of the West	Eric Jones, Corporate Banking Officer
Borg Warner Chemicals	Richard Haberkoft, Marketing Development Manager, Business Machines
Burr, Egan, Deleage & Company	Shirley Cerrudo, Partner

California Devices, Inc.	Douglas Ritchie, President & Chief Executive Officer
Chase Econometrics	Lawrence Chimerine, Chairman and Chief Economist
Chips and Technology, Inc.	Ronald Yara, Director of Marketing
Cirrus Logic	Kamran Elahian, Senior Vice President, Strategic Operations Mike Hackworth, President
Citibank	Tom Larsen, Vice President, Capital Goods
Citicorp Industrial Credit	Mano Appapillai, Vice President
Cognos Associates	Judith Larsen, President
Commodore Business Machines, Inc.	Robert Bowie, Vice President, General Manager Commodore Semiconductor Group Adam Chowaniec, Vice President, Technology
Corning Glass Works	John Dunphy, Manager, New Business Development Thomas Dwyer, Manager, Technology Development Tom Gardner, Manager, Market Development
Crystal Semiconductor	Allan Hamilton, Vice President, Marketing
Custom Silicon, Inc.	Albert Belle Isle, President
Data I/O Corporation	David Hannaford, Manager, Business Development

Datapoint Corporation	Brian Fullmer, Director Jean Fullmer Rick Sasseen, Semiconductor Contract Specialist
Dataquest Incorporated	Carol Bender, Conference Assistant Betty Bluford, Conference Assistant Howard Bogert, Vice President & Director, Semiconductor Industry Group John Brew, Research Associate, Semiconductor Application Markets Steve Cooper, Manager, Industrial Marketing Bea Destin, Conference Assistant Manny Fernandez, President Frank Florence, Vice President, Industry Sales Karen Foley, Manager, Information Services Joe Grenier, Senior Industry Analyst John Jackson, National Sales Manager Susan Kelly, Research Asociate Bryan Lewis, Research Associate Lane Mason, Senior Industry Analyst Robert McGeary, Director, Semiconductor Equipment & Materials Service Gene Norrett, Associate Director, Semiconductor Industry Group Linda Norrett Andy Prophet, Senior Industry Analyst Janet Rey, Research Analyst Jim Riley, Senior Vice President Frank Sammann, Senior Vice President, Sales Susan Scibetta, Research Associate Lynn Stern, Conference Coordinator Anthea Stratigos, Product Manager Mel Thomsen, Associate Director, Semiconductor Industry Service Peggy Wood, Research Analyst Frederick Zieber, Senior Vice President & General Manager, Technology Operations Libbe Zieber
Dataquest Japan, Ltd.	K. O'Hara, Dataquest Consultant Osamu Ohtake, Associate Director

Dataquest UK Limited	Malcolm Penn, Vice President & Director, European Semiconductor Industry Service
Delco Electronics Division, GMC	Vincent Newson, General Supervisor, IC CAD & Layout
Department of Trade and Industry	J.H. Major J.G. Noyes
Dieli	Gerard Matheron Mr. Roset
Digital Equipment Corporation	Prakash Bhalerao, Manager, ASIC Center Steve Cavicchi, Plant Materials Manager Dan Hamel, Plant Manager
Dow Corning Corporation	Kit Kemp, Market Development Specialist
DuPont Pension Fund	Gene Davis, Portfolio Manager
Dynamit Nobel Silicon, Inc.	Dave Brooks, Vice President, Marketing & Sales Weldon Smith, Director of Sales Peter Suerken, President
Dyne-Sem International, Ltd.	Daniel Camp, Vice President, Sales & Marketing Richard Hernandez, Vice President, Corporate Services
ECAD, Inc.	Peter Whyte, Vice President, Strategic Planning
ERSO/ITRI	Hsing Chih-Tien, Director, IC Product Development Division Albert Huang, Director, IC Product Development Division

Electric Power Research Institute	John Cummings, Department Director Pauline Cummings
Fairchild Camera & Instrument Corporation	Tom Miller, Marketing Manager Chris Newham, Strategic Marketing Manager Richard Phlegar, Memory Products Planner Manager
Fairfield Venture Partners	Thomas Berman, Associate Edmund Olivier, General Partner
Ford Microelectronics, Inc.	Charlotte Diener, Marketing Manager Michael Doyle, Director, Marketing & Business Services John Wallace, President
Ford Motor Company	Jerome Rivard, Chief Engineer, Electrical & Engineering
Fujitsu Microelectronics, Inc.	Robert Freischlag, Senior Vice President, General Manager, IC Division
GCA Corporation	Paul Reagan, Senior Vice President
GMF Robotics	Dr. Warren Hastings, Engineering Manager John Hoshizaki, Senior, Engineer Jim Pelusi, Director, Electronics
General Electric Company	Emory Lane, Manager, Business Development & Planning
General Electric Investments	Dorcas Casey
General Motors Corporation	Carol Johnson, Senior Project Engineer
Genus, Inc.	Ron Dornseis, Product Marketing

Hyundai Electronics America	W.S. Koo, Chief Executive Officer Andrew Procassini, Vice President, Marketing & Sales Marlene Procassini
I.P. Sharp Associates	James Destefano, Business Development Manager, Factory Automation Systems
IBM Corporation	Irv Abzug, GTD Vice President & Director, CCP Harriet Abzug Ed Boerger, Manager, Business Analysis David Jacobs, Buiness Analyst Dan Ling, Manager, Microsystems John Melgavis, Industrial Engineer Dave Royce, Analyst
ICD Austria	Robert Karl, Executive Vice President Monika Pacher, Director
ICI Americas, Inc.	Rick LaFrance, Project Manager
IDA Ireland	Brendan Halpin, Vice President
INMOS Corporation	Richard Riker, Area Sales Manager
Institute for Microcontamination Control	James Burnett, President & Executive Director, IMCC Danielle Burnett
Integrated Logic Systems, Inc.	Jeffrey Jacobsen, Vice President, Marketing & Sales David Taylor, President
Intel Corporation	Leonard Hills, Analyst Dave House, General Manager, Microcomputer Group Jamie Kirk, Marketing Manager Don Knowlton, Product Marketing Manager Mark Varno, Manager

Interfirst Venture Corporation	Mark Masur, Vice President
International CMOS Technology	Drew Osterman, President Stan Patterson, Director of Sales
Intersil, Inc.	Jerry Kiachian, Vice President, Manufacturing
Italtel Telematica	Gianni Bertolini, Director of Corporate Procurement Emilio Dragoni, Market Research Mario Tripputi, Marketing Manager
J. H. Whitney & Company	Harry Marshall, Partner
J.P. Morgan Investment Management	Charles Kimball, Vice President Mary Ann Liberatore
James D. Wolfensohn, Inc.	Peter Levin, Associate
KLA Instruments, Inc.	Harvey Frye, National Sales Manager Karl Harris, Vice President, Microlithographic Process Control Technology Wafer Inspection Robert Hery, Vice President & General Manager, Wafer Inspection Divisio Kenneth Levy, President Gloria Levy Dean Lindholm, Vice President
LM Ericsson Corporation	Bengt Soderberg, Vice President, Corporate Purchasing
LSI Logic Corporation	Perry Constantine, Vice President, North America Marketing & Sales Wilfred Corrigan, Chairman & Chief Executive Officer Bill O'Meara, Vice President, Marketing Joyce O'Meara John Shea, Director, Military Technology & Security George Wells, President

LSI Logic Europe Limited	Robert Blair, President
Lattice Semiconductor Corporation	Rahul Sud, President & Chief Executive Officer
Lehman Management Company	Phillips Lawrence, Vice President
Lex Service, Inc.	Milton Grannatt, III, Vice President, Planning Andrew Johnson, Vice President
MIPS Computer Systems	Skip Stritter, Vice President, Engineering
Marconi Electronic Devices, Ltd.	Roger Jones, Director, Strategic Marketing & Technology
Matrix, Inc.	Rick Hazard, Marketing Manager
Menlo Ventures	Dubose Montgomery, General Partner
Micro Power Systems	Mitch Gooze, General Manager, Custom Products Division
Micro-Linear Corporation	Alan Grebene, President
Microbot, Inc.	Guy Rhodes, President Jean Rhodes
Microelectronic Packaging, Inc.	Joe Ref, Chief Executive Officer
Mitsubishi Electronics	Dwain Aidala, Assistant General Manager & Marketing Manager Hiroyoshi Komiya, Deputy Manager
Mitsubishi International	Ray Phillips, Marketing Manager, Business Development

Mitsubishi Semiconductor America, Inc.	Tad Mizoguchi, Executive Vice President
Monolithic Memories, Inc.	Andy Robin, Corporate Marketing Manager
Monsanto Electronic Material Company	Wendy Grossman, Manager, Market Analysis Liz Isaacs, Business Manager, Photoresist Products
Monsanto Electronic Materials Corporation	Haskell Waddle, Vice President, Marketing
Mostek Corporation	Jim Byrne, Senior Vice President, Business Development Bert Kehren, Director, Strategic Planning
Motorola, Inc.	Bernie Aronson, President, Pico Design Bob Jenkins, Vice President Carolee Jenkins Gerald Lunn, Planning Manager Douglas Powell, Vice President & Director, Strategic Marketing Fred Zlotnick, Marketing Manager
Mullard, Ltd.	Keith Gimson, Manager, Long Range Planning
Mutual of New York	Tony Blenk, Director
NCR Corporation	Dr. James Van Tassel, Vice President, Microelectronics Division Mary Lou Van Tassel
NEC Electronics USA, Inc.	David Carnevale, Manager, Strategic Planning
National Semiconductor Corporation	Manny Naik, Director, Strategic Marketing F. Joseph Van Poppelen, Vice President, Marketing Lien Zayhowski, Market Research Analyst

Nicolet Instrument Corporation	Ronald Lindell, President
Nihon LSI Logic Corporation	Keiske Yawata, President
Nikon Precision	Marc DeLeeuwe, Vice President, Marketing & Sales
Nippon Steel Corporation	Fumihiko Dai, Senior Manager, Corporate Planning Division
Northern Telecom, Inc.	Monte Seifers, Director, Strategic Planning
Northern Telecom, Ltd.	E. Dennis Colbourne, Assistant Vice President, Marketing
Oak Management Corporation	Catherine Pierson, General Partner
Oki Electric Industry Company, Ltd.	Yasuro Kunori, Manager, Marketing & Sales Division, Electron Devices Group Shusaku Sumida, Vice President, Sales & Marketing
Oki Semiconductor	Leonard Distaso, Vice President, Marketing
Omniprise	Ralph Altomare, Chief Executive Officer
Perkin-Elmer Corporation	Mike Archuletta, National Marketing Manager Ron DeLuca, Senior Manager Carrol Fencil, Director, Government Systems Mrs. Fencil Bob McMenamin, Marketing Communications Manager James Nester, Director, Planning Semiconductor Equipment Group

Philip A. Hunt Chemical Corporation	Jack Murphy, Director of Marketing
Pitney Bowes, Inc.	Michael Swaluk, Manager, Electronic Support Lynn Swaluk
Plessey Semiconductors	Gary Smith, Semi Custom Business Manager
Price Waterhouse	James Coriston, Chairman, High Technology
Prudential-Bache Securities	Richard Whittington, Vice President
Quasel, Inc.	Kirk MacKenzie, Vice President, Marketing & Sales
RCA Corporation	Robert Lenz, Administrator, Sales Analysis Lloyd Taylor, Vice President, Solid State Division Karen Taylor
Ramtron Corporation	Robert Venes, Director of Operations
Raytheon Semiconductor Division	Zoaib Rangwala, Product Line Manager
Ricoh Corporation	Kenichi Ichihashi, Vice President, Marketing
Robert Bosch GmbH	Horst Fischer, Director, Semiconductor Product Division Horst Gschwentdner, Manager, Design Center Dr. Gunter Matthai, Manager, Technology Planning
Rockwell International Corporation	Craig Ensley, Director of Marketing

Rosenberg Capital Management	Chen Huachen, Research Analyst
SAI-SEMI Specialists	Ken Chojnacki, Marketing Manager, Semiconductors Allan Schefer, Director, Product Management Semiconductors
SAMES	Geoff Hainebach, Managing Director
SGS Semiconductor Corporation	David Hage, Director, Marketing Planning
San Jose Mercury News	Chris Schmitt, Reporter
Scudder, Stevens & Clark	George Rockwood, Vice President, Research
Sears Investment Management Company	Stephen Dexter, Investment Analyst
Seattle Silicon	George Cone, Senior Vice President Leslie Cone
Security Pacific Venture Capital	Dmitry Bosky, Vice President James McElwee, First Vice President
Semiconductor Microelectronics International	Joseph Curry, Consultant
Semiconductor Research Corporation	Larry Sumney, President
Sentry Schumberger	Cindy Kewnaugh, Market Analysis
Shinko Electric Industries Company	Bill Cruickshank, Executive Vice President
Siemens Components, Inc.	Klaus Bahr, Senior Vice President

Silicon Compilers, Inc.	Walter Curtis, Vice President, Marketing Stanley Mazor, Manager, Applications Engineering
Silicon Design Labs, Inc.	Richard Gossen, Jr., President & Chief Executive Officer James Hammock, Vice President, Market & Sales
Silicon Microsystems, Inc.	Philip Siu, President
Silicon Systems, Inc.	Alan Portnoy, Senior Vice President, Corporate Business Development Clysta Seney, Business Planning Manager
Solitec, Inc.	Donald Winstead, President Myra Winstead
Soros Fund Management	Andy Stallman, Vice President
Sperry Corporation	Wesley Grant, Director, Technology & Engineering
Sprague Solid State	Ed Day, Director, Strategic Marketing & Planning
Standard Microsystems Corporation	Brian Cayton, Director of Marketing Gerald Gollub, Executive Vice President
T. Rowe Price Associates, Inc.	Randolph Kilmon, Research Analyst Carol Napiek
TRW Optoelectronics Division	Kenneth Hagge, Vice President & General Manager
Tektronix, Inc.	Jack Sachitano, Solid State Research Lab Manager

Temescal	Keith Hampe, President
Teradyne, Inc.	Ron Butler, Purchasing Manager. Gordon Padwick, Research Analyst Stratton Smith, Director of Purchasing
Thomson-CSF Communications, Inc.	M. Nghiem Phan, Vice President, Engineering
Tokyo Electron, Ltd.	Takio Itoh, Manager, EC Marketing Department
Toshiba America, Inc.	Jay Litus, Jr., Director of Marketing, ECBS James Townsend, Strategic Marketing Manager, ECBS
Trust Company of The West	Abe Ofer, Research Analyst
U.S. Department of Commerce	Clyde Prestowitz, Counselor to the Secretary Joan Rolf, Industry Specialist
Ultratech Stepper	George Rutland, President
Union Carbide Corporation	John Eads, Region Marketing Manager Anthony Keig, Business Research Manager Charles Krichbaum, Business Manager, Electronics Thomas Nelson, Manager, Market Development Thomas Singman, Marketing Manager, Electronics Walter Willett, Manager, On Site Sales
United Microelectronics Corporation	Ivan Ho, Market Planning Manager
Universal Semiconductor, Inc.	Bill Smithson, Chief Operating Officer George Stephan, President

University of Arizona	Roy Mattson, Chairman, Electrical Engineering & Computer Engineering Department
VLSI Technology, Inc.	Douglas Fairbairn, Vice President Pam Fairbairn Henri Jarrat, President & Chief Executive Officer Ronald Kasper, Vice President, Worldwide Sales
Venture Growth Associates	Jim Berdell, Managing Partner William Welling, Managing Partner
Vitelic Corporation	Alex Au, President Jack Konrath, Marketing Communications Manager Jack Ordway, Vice President, Marketing and Sales
Vitesse Electronics Corporation	James Brye, Vice President, Marketing & Sales
Waferscale Integration, Inc.	Eli Harari, President
Weitek Corporation	Art Collmeyer, President Merlyn Collmeyer Scott Lewis, Director, Strategic Development
Western Digital Corporation	John MacKay, Vice President, LSI Operations
Xerox Corporation	Sei Shohara, Manager, Technical Staff

ZyMOS Corporation

Dave Guzeman, Vice President, Marketing & Sales
Alex Young, Senior Vice President, Engineering

John Banning, Independent Computer Consultant

Bob Lipp

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SEMICONDUCTOR INDUSTRY SERVICE CONFERENCE
October 14 through 16, 1985
TUCSON, ARIZONA

List of Attendees

Irv Abzug Harriet Abzug	IBM Corporation
Dwain Aidala	Mitsubishi Electronics
Ralph Altomare	Omniprise
Nikita Andreiev	AWI Corporation
Mano Appapillai	Citicorp Industrial Credit
Mike Archuletta	Perkin-Elmer Corporation
Ed Armstrong	Hughes Aircraft Company
Bernie Aronson	Motorola, Inc.
Alex Au	Vitelic Corporation
Tom Autry	Honeywell, Inc.
Willi Bacher Ellen Bacher	Bacher GmbH
Klaus Bahr	Siemens Components, Inc.
John Bakey	Air Products & Chemicals, Inc.
John Banning	
Jim Barnett	Xilinx, Inc.
Albert Belle Isle	Custom Silicon, Inc.
Carol Bender	Dataquest Incorporated
James Berdell	Venture Growth Associates
Thomas Berman	Fairfield Venture Partners
Gianni Bertolini	Italtel Telematica
Prakash Bhalerao	Digital Equipment Corporation

Michael Bianco	Hibernia Bank
David Birnbaun	Hewlett-Packard Company
Elizabeth Blaettermann	Hitachi America, Ltd.
Robert Blair	LSI Logic Europe Limited
Tony Blenk	Mutual of New York
Betty Bluford	Dataquest Incorporated
Fred Blum	Gigabit Logic
Ed Boerger	IBM Corporation
Howard Bogert	Dataquest Incorporated
Dmitry Bosky	Security Pacific Venture Capital
Timothy Bottoms	Bank of America
Robert Bowie	Commodore Business Machines, Inc.
Thomas Bowman	Applied Materials, Inc.
John Brew	Dataquest Incorporated
Dave Brooks	Dynamit Nobel Silicon, Inc.
James Brye	Vitesse Electronics Corporation
James Burnett Danielle Burnett	Institute for Microcontamination Control
Ron Butler	Teradyne, Inc.
Jim Byrne	Mostek Corporation
Daniel Camp	Dyne-Sem International, Ltd.
David Carnevale	NEC Electronics USA, Inc.
Dorcas Casey	General Electric Investments
Steve Cavicchi	Digital Equipment Corporation
Brian Cayton	Standard Microsystems Corporation
Shirley Cerrudo	Burr, Egan, Deleage & Company

Y.S. Chen	AT&T Bell Laboratories
Hsing Chih-Tien	ERSO/ITRI
Lawrence Chimerine	Chase Econometrics
Ken Chojnacki	SAI-SEMI Specialists
Adam Chowaniec	Commodore Business Machines, Inc.
E. Dennis Colbourne	Northern Telecom, Ltd.
Art Collmeyer Merlyn Collmeyer	Weitek Corporation
George Cone Leslie Cone	Seattle Silicon
Perry Constantine	LSI Logic Corporation
Steve Cooper	Dataquest Incorporated
James Coriston	Price Waterhouse
Wilfred Corrigan	LSI Logic Corporation
Al Crawford	Arthur Young & Company
Bill Cruickshank	Shinko Electric Industries Company
John Cummings Pauline Cummings	Electric Power Research Institute
Joseph Curry	Semiconductor Microelectronics International
Walter Curtis	Silicon Compilers, Inc.
Don Cvietusa	Bank of America
Fumihiko Dai	Nippon Steel Corporation
Gene Davis	DuPont Pension Fund
Wallace Davis Lu Davis	Alpha Partners
Ed Day	Sprague Solid State
Marc DeLeeuwe	Nikon Precision

Ron DeLuca	Perkin-Elmer Corporation
James Destefano	I.P. Sharp Associates
Bea Destin	Dataquest Incorporated
Stephen Dexter	Sears Investment Management Company
Charlotte Diener	Ford Microelectronics, Inc.
Leonard Distaso	Oki Semiconductor
Ron Dornseis	Genus, Inc.
Michael Doyle	Ford Microelectronics, Inc.
Emilio Dragoni	Italtel Telematica
Roger Dunbar	Arthur Young & Company
John Dunphy	Corning Glass Works
Thomas Dwyer	Corning Glass Works
John Eads	Union Carbide Corporation
Kamran Elahian	Cirrus Logic
Jim Elick	Gould AMI Semiconductors
Craig Ensley	Rockwell International Corporation
William Evans	AT&T Bell Laboratories
Douglas Fairbairn Pam Fairbairn	VLSI Technology, Inc.
Carrol Fencil Mrs. Fencil	Perkin-Elmer Corporation
Manny Fernandez	Dataquest Incorporated
Robert Finch	Aetna Life and Casualty
Horst Fischer	Robert Bosch GmbH
Frank Florence	Dataquest Incorporated
Karen Foley	Dataquest Incorporated
Robert Freischlag	Fujitsu Microelectronics, Inc.

Marc Friedmann	Applied Micro Circuits Corporation
Harvey Frye	KLA Instruments, Inc.
Brian Fullmer Jean Fullmer	Datapoint Corporation
Tom Gardner	Corning Glass Works
Keith Gimson	Mullard, Ltd.
James Goldey	AT&T Bell Laboratories
Gerald Gollub	Standard Microsystems Corporation
Mitch Gooze	Micro Power Systems
Richard Gossen, Jr.	Silicon Design Labs, Inc.
Milton Grannatt, III	Lex Service, Inc.
Wesley Grant	Sperry Corporation
Alan Grebene	Micro-Linear Corporation
Lisa Green	Bank of Boston
Joe Grenier	Dataquest Incorporated
Wendy Grossman	Monsanto Electronic Material Company
Horst Gschwentdner	Robert Bosch GmbH
Dave Guzeman	ZyMOS Corporation
Richard Haberkoft	Borg Warner Chemicals
Mike Hackworth	Cirrus Logic
David Hage	SGS Semiconductor Corporation
Kenneth Hagge	TRW Optoelectronics Division
Geoff Hainebach	SAMES
Brendan Halpin	IDA Ireland
Dan Hamel	Digital Equipment Corporation
Allan Hamilton	Crystal Semiconductor

James Hammock	Silicon Design Labs, Inc.
Keith Hampe	Temescal
David Hannaford	Data I/O Corporation
Eli Harari	Waferscale Integration, Inc.
Karl Harris	KLA Instruments, Inc.
Paul Hart	Hughes Aircraft Company
Dr. Warren Hastings	GMF Robotics
Rick Hazard	Matrix, Inc.
Richard Hernandez	Dyne-Sem International, Ltd.
Robert Hery	KLA Instruments, Inc.
Leonard Hills	Intel Corporation
Ivan Ho	United Microelectronics Corporation
John Hoshizaki	GMF Robotics
Dave House	Intel Corporation
Chen Huachen	Rosenberg Capital Management
Albert Huang	ERSO/ITRI
Dennis Hunter	Applied Materials, Inc.
Kenichi Ichihashi	Ricoh Corporation
Liz Isaacs	Monsanto Electronic Material Company
Kohei Ito	Hitachi Metals, Ltd.
Takio Itoh	Tokyo Electron, Ltd.
John Jackson	Dataquest Incorporated
David Jacobs	IBM Corporation
Richard Jacobs	AT&T Bell Laboratories
Jeffrey Jacobsen	Integrated Logic Systems, Inc.
Henri Jarrat	VLSI Technology, Inc.

Bob Jenkins Carolee Jenkins	Motorola, Inc.
Kent Jensen	Amoco Corporation
Andrew Johnson	Lex Service, Inc.
Carol Johnson	General Motors Corporation
Eric Jones	Bank of the West
Roger Jones	Marconi Electronic Devices, Ltd.
Robert Karl	ICD Austria
Ronald Kasper	VLSI Technology, Inc.
Bert Kehren	Mostek Corporation
Anthony Keig	Union Carbide Corporation
Susan Kelly	Dataquest Incorporated
Kit Kemp	Dow Corning Corporation
Cindy Kewnaugh	Sentry Schumberger
Jerry Kiachian	Intersil, Inc.
Randolph Kilmon Carol Napiek	T. Rowe Price Associates, Inc.
Charles Kimball Mary Ann Liberatore	J.P. Morgan Investment Management
Jamie Kirk	Intel Corporation
Stephen Knight	AT&T
Don Knowlton	Intel Corporation
Dan Koloski	Commodore Business Machines, Inc.
Hiroyoshi Komiya	Mitsubishi Electronics
Jack Konrath	Vitelic Corporation
W.S. Koo	Hyundai Electronics America
Sara Jane Koperski	AT&T Technologies, Inc.

Charles Krichbaum	Union Carbide Corporation
Yasuro Kunori	Oki Electric Industry Company, Ltd.
Rick LaFrance	ICI Americas, Inc.
Burt Lancaster	Air Products & Chemicals, Inc.
Emory Lane	General Electric Company
Judith Larsen	Cognos Associates
Tom Larsen	Citibank
Philips Lawrence	Lehman Management Company
Robert Lenz	RCA Corporation
Peter Levin	James D. Wolfensohn, Inc.
Kenneth Levy Gloria Levy	KLA Instruments, Inc.
Bryan Lewis	Dataquest Incorporated
Scott Lewis	Weitek Corporation
Ronald Lindell	Nicolet Instrument Corporation
Dean Lindholm	KLA Instruments, Inc.
Dan Ling	IBM Corporation
Bob Lipp	
Jay Litus, Jr.	Toshiba America, Inc.
Anthony Livingston Pat Livingston	Gigabit Logic
Gerald Lunn	Motorola, Inc.
John MacKay	Western Digital Corporation
Kirk MacKenzie	Quasel, Inc.
James Mahoney	HLM Management Company
J.H. Major	Department of Trade and Industry

Harry Marshall	J. H. Whitney & Company
Lane Mason	Dataquest Incorporated
Mark Masur	Interfirst Venture Corporation
Gerard Matheron	Dieli
Dr. Gunter Matthai	Robert Bosch GmbH
Roy Mattson	University of Arizona
Stanley Mazor	Silicon Compilers, Inc.
James McElwee	Security Pacific Venture Capital
Robert McGeary	Dataquest Incorporated
Harry McGrath	Hitachi America, Ltd.
Bob McMenamin	Perkin-Elmer Corporation
John Melgavis	IBM Corporation
Robert Melin	AT&T Bell Laboratories
Tom Miller	Fairchild Camera & Instrument Corp.
Tad Mizoguchi	Mitsubishi Semiconductor America, Inc.
Dubose Montgomery	Menlo Ventures
Jack Murphy	Philip A. Hunt Chemical Corporation
Manny Naik	National Semiconductor Corporation
Thomas Nelson	Union Carbide Corporation
James Nester	Perkin-Elmer Corporation
Chris Newham	Fairchild Camera & Instrument Corporation
Vincent Newson	Delco Electronics Division, GMC
Kosei Nomiya	Hitachi Microsystems International
Gene Norrett	Dataquest Incorporated
Linda Norrett	Dataquest Incorporated

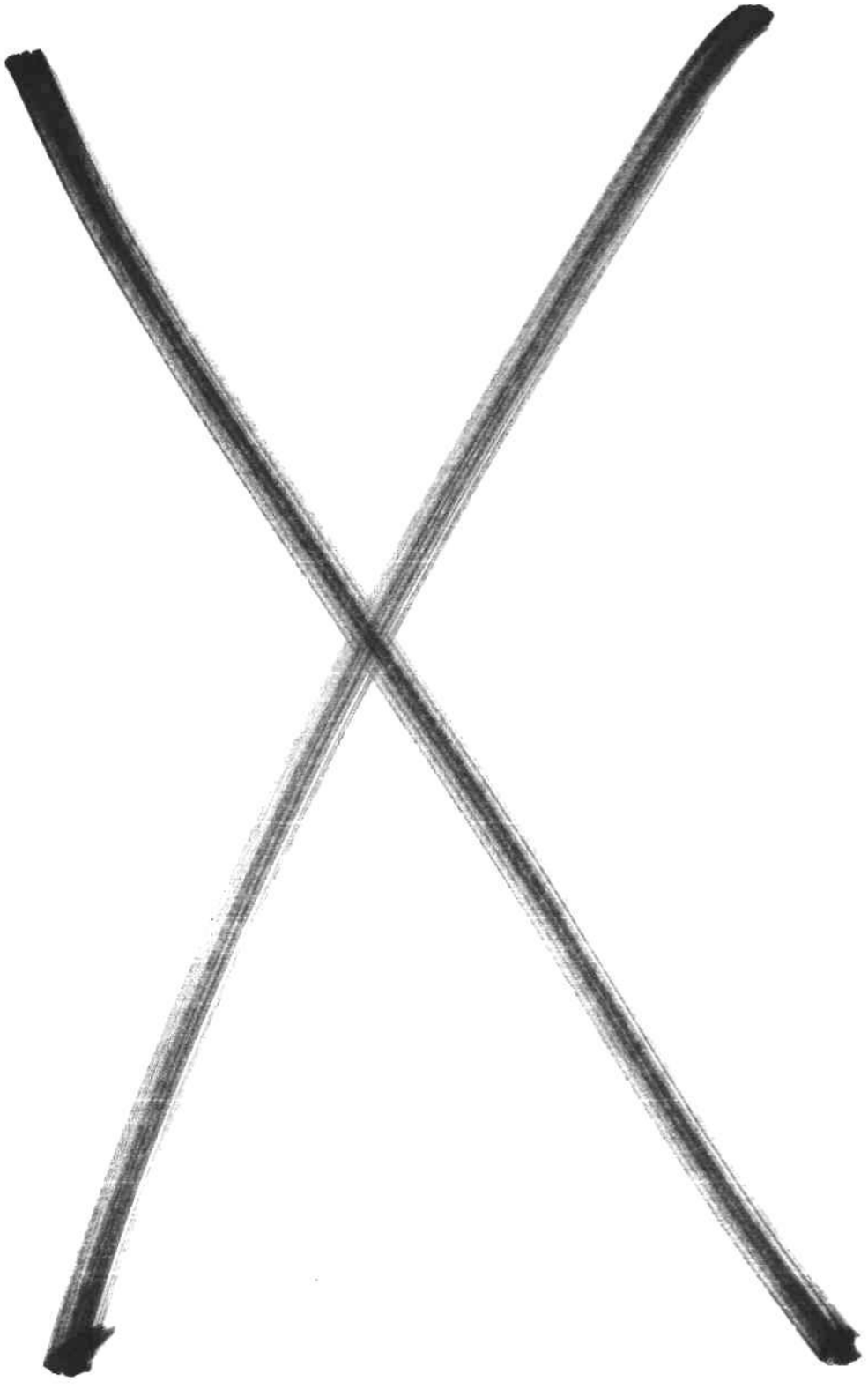
J.G. Noyes	Department of Trade and Industry
Richard O'Malley	AT&T Technologies, Inc.
Bill O'Meara Joyce O'Meara	LSI Logic Corporation
Dan O'Neill	Adler & Company
Abe Ofer	Trust Company of The West
K. O'Hara	Dataquest Japan, Ltd.
Osamu Ohtake	Dataquest Japan, Ltd.
Edmund Olivier	Fairfield Venture Partners
Jack Ordway	Vitelic Corporation
Drew Osterman	International CMOS Technology
Monika Pacher	ICD Austria
Gordon Padwick	Teradyne, Inc.
Pierre Paqueron	Aerospatiale
Stan Patterson	International CMOS Technology
Jim Pelusi	GMF Robotics
Malcolm Penn	Dataquest UK Limited
Robert Penn	Gould AMI Semiconductors
M. Nghiem Phan	Thomson-CSF Communications, Inc.
Ray Phillips	Mitsubishi International
Richard Phlegar	Fairchild Camera & Instrument Corporation
Catherine Pierson	Oak Management Corporation
Ken Poole	AT&T Bell Laboratories
Alan Portnoy	Silicon Systems, Inc.
Douglas Powell	Motorola, Inc.

Clyde Prestowitz	U.S. Department of Commerce
Andrew Procassini Marlene Procassini	Hyundai Electronics America
Andy Prophet	Dataquest Incorporated
Zoaib Rangwala	Raytheon Semiconductor Division
Paul Reagan	GCA Corporation
Joe Ref	Microelectronic Packaging, Inc.
Janet Rey	Dataquest Incorporated
Guy Rhodes Jean Rhodes	Microbot, Inc.
Ralph Richardson	Air Products & Chemicals, Inc.
Richard Riker	INMOS Corporation
Jim Riley	Dataquest Incorporated
Douglas Ritchie	California Devices, Inc.
Jerome Rivard	Ford Motor Company
Andy Robin	Monolithic Memories, Inc.
George Rockwood	Scudder, Stevens & Clark
Joan Rolf	U.S. Department of Commerce
Mr. Roset	Dieli
Dave Royce	IBM Corporation
George Rutland	Ultratech Stepper
Jack Sachitano	Tektronix, Inc.
Frank Sammann	Dataquest Incorporated
Stewart Sando	Gigabit Logic
Rick Sasseen	Datapoint Corporation
Allan Schefer	SAI-SEMI Specialists

Chris Schmitt	San Jose Mercury News
Susan Scibetta	Dataquest Incorporated
Monte Seifers	Northern Telecom, Inc.
Clysta Seney	Silicon Systems, Inc.
Robert Shay	Air Products & Chemicals, Inc.
John Shea	LSI Logic Corporation
Sei Shohara	Xerox Corporation
Thomas Singman	Union Carbide Corporation
Philip Siu	Silicon Microsystems, Inc.
Gary Smith	Plessey Semiconductors
Stratton Smith	Teradyne, Inc.
Weldon Smith	Dynamit Nobel Silicon, Inc.
Bill Smithson	Universal Semiconductor, Inc.
Bengt Soderberg	LM Ericsson Corporation
Lewis Solomon Ruth Solomon	Alan Patricof Associates
Andy Stallman	Soros Fund Management
George Stephan	Universal Semiconductor, Inc.
Lynn Stern	Dataquest Incorporated
Anthea Stratigos	Dataquest Incorporated
Skip Stritter	MIPS Computer Systems
Rahul Sud	Lattice Semiconductor Corporation
Peter Suerken	Dynamit Nobel Silicon, Inc.
Shusaku Sumida	Oki Electric Industry Co., Ltd.
Larry Sumney	Semiconductor Research Corporation
Michael Swaluk Lynn Swaluk	Pitney Bowes, Inc.

David Taylor	Integrated Logic Systems, Inc.
Lloyd Taylor Karen Taylor	RCA Corporation
Mel Thomsen	Dataquest Incorporated
Norbert Thonnard	Atom Science
James Townsend	Toshiba America, Inc.
Mario Tripputi	Italtel Telematica
Mark Udem	Bank of Boston
F. Joseph Van Poppelen	National Semiconductor Corporation
Dr. James Van Tassel Mary Lou Van Tassel	NCR Corporation
Mark Varno	Intel Corporation
Robert Venes	Ramtron Corporation
Mark Verissimo	Bank of America
Haskell Waddle	Monsanto Electronic Materials Corportion
Bob Waite	Hewlett-Packard Company
Edward Walker, Jr.	AT&T Technologies, Inc.
John Wallace	Ford Microelectronics, Inc.
William Welling	Venture Growth Associates
George Wells	LSI Logic Corporation
Richard Whittington	Prudential-Bache Securities
Peter Whyte	ECAD, Inc.
Walter Willett	Union Carbide Corporation
Donald Winstead Myra Winstead	Solitec, Inc.
William Wittmeyer	Grace Ventures Corporation

Noel Wolf	Honeywell Digital Product Division
Peter Wolken	Associated Venture Investors
Peggy Wood	Dataquest Incorporated
Susan Woods	Grace Ventures Corporation
Ronald Yara	Chips and Technology, Inc.
Keiske Yawata	Nihon LSI Logic Corporation
Alex Young	ZyMOS Corporation
Lien Zayhowski	National Semiconductor Corporation
Frederick Zieber Libbe Zieber	Dataquest Incorporated
Fred Zlotnick	Motorola, Inc.



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SEMICONDUCTOR INDUSTRY SERVICE
October 1985

AMP, Inc.
AT&T Bell Laboratories
AT&T Communications
AT&T Resource Management
AT&T Technologies Inc.
Advanced Micro Devices Inc.
Aerospatiale
Air Products & Chemicals, Inc.
Air Products Ltd.
Analog Devices BV
Ando Electric Co., Ltd.
Applied Materials, Inc.
Applied Micro Circuits Corporation
Arrow Electronics, Inc.
Arthur Young & Company
Asahi Microsystems, Inc.
Atcor of California, Inc.
BMC Industries, Inc.
BULL Transac
Burroughs Corporation
CIT Alcatel
CIT Alcatel "CLEM"
CNET
California Devices, Inc.
Calma Company
Calmos Systems, Inc.
Canon, Inc.
Chips and Technologies, Inc.
Cii Honeywell Bull
Commodore Semiconductor Systems
Compagnie IBM France
Crystal Semiconductor
Custom Silicon, Inc.
Cypress Semiconductor Corporation
D.I.E.L.I.
Daewoo Electronics Components Co.
Data General Corporation
Data I/O Corporation
Data One
Department Trade & Industry
Department of Industry, Trade
Digital Equipment Corporation
Dynamit Nobel Silicon, Inc.
E.I. DuPont De Nemours & Company
ERSO/ITRI
Eastman Kodak Company
Electronic Power Research Institute
Ericsson Corporation/RIFA
Ericsson Information Systems
Eurotechnique
Exel Microelectronics, Inc.
Fairchild A Schlumberger Company
Fairchild Camera & Instrument Co.
Fairchild Electronics GmbH
Fairchild Europe(Semiconducteurs)SA
Fairchild Memory Test Systems
Fairchild Research
Fairchild Semiconductor
Ferranti Computer Systems Ltd.
Ferranti Electronics Ltd.
Ferranti Interdesign, Inc.
Fuji Electric Co., Ltd.
Fujitsu Limited
Fujitsu Microelectronics, Inc.
GCA Corporation
GEC Research Laboratories
GTE Microcircuits
GenRad, Inc.
General Electric Company
General Instrument Corporation
General Instruments Int'l., Ltd.
General Motors Corporation
GigaBit Logic
Gold Star Semiconductor, Ltd.
Gould AMI Semiconductors
Harris Corporation
Hewlett-Packard Company
Hitachi America, Ltd.
Hitachi Electronic Components GmbH
Hitachi Ltd.
Hitachi Metals, Ltd.
Hitachi Research Institute
Holt, Inc.
Honeywell, Inc.
Hoya Corporation
Hughes Aircraft Company
IBM Corporation
IBM France
IBM France Compec
IBM Japan, Ltd.
IBM Oesterreich
IBM UK Intl Products Ltd.
IDA Ireland
IKOS Systems

ILSI
ITT Europe
ITT Intermetall GmbH
ITT Semiconductors
Ing. C. Olivetti & C., S.p.A.
Inmos Corporation
Inmos Ltd.
Integrated Device Technology
Intel Corporation
Intel International S.A.
Interlek, Inc.
International CMOS Technology
Intersil, Inc.
Intl Microelectronics Products, Inc.
Italtel SIT S.p.A.
Itau Componentes S.A.
Kanematsu Electronic Components Corporation
Kanematsu-Gosho (USA)
Kyocera Corporation
Kyocera International, Inc.
LEX Service Group
LSI Logic Corporation
LTX Corporation
Lattice Semiconductor Corporation
Lex Service, Inc.
Linear Technology Corporation
MBB Apparate GmbH
MOS Electronics Corporation
Marathon Industries
Marconi Electronic Devices, Ltd.
Matra Design Systems
Matra Harris Semiconducteurs
Megatest Corporation
Mentor Graphics Corporation
MicroPower Systems, Inc.
Microelectronics Technology Company
Micromos, Inc.
Ministerio de Industria y Energia
Mitsubishi Chemical Industries Ltd.
Mitsubishi Corporation
Mitsubishi Electric Corporation
Mitsubishi Electronics America, Inc
Miyazaki Oki Electric Co., Ltd.
Modular Semiconductor, Inc.
Monolithic Memories, Inc.
Monsanto Electronic Materials Co.
Mostek Corporation
Mostek Japan K. K.
Motorola Semiconductor Europe SA
Motorola, Inc.
Mullard Limited
NCR Corporation
NEC Corporation
NEC Electronics USA, Inc.
Narumi China Corporation
National Bureau of Standards Center
National Semiconductor Corporation
Nippon Kogaku K.K.
Nippon Steel Corporation
Nippon Telegraph & Telephone
Nissan Motor Co., Ltd.
Nissei Sangyo Co., Ltd.
Northern Telecom, Ltd.
OKI Electric Industry Co., Ltd.
OKI Semiconductor
Okamoto Machine Tool Works, Ltd.
Olcea-Direzione
Panatech R & D Corporation
Perkin-Elmer Corporation
Perkin-Elmer Electron Beam Tech.
Philips International BV
Philips Taiwan Ltd.
Pitney Bowes, Inc.
Plessey Semiconductors Ltd.
Plessey Solid State
Quasel, Inc.
RCA Corporation
Ramtron
Ricoh Corporation
Robert Bosch GmbH
Rockwell International Corporation
S A M E S, Ltd.
S-MOS Systems, Inc.
S.E.H. America, Inc.
SAI-SEMI Specialists
SEEQ Technology, Inc.
SGS Microelecttronica S.p.A.
SGS Semiconductor Corporation
SID Microelectronica, Ltda.
STACK GmbH
STC Semiconductors Ltd.
STET Societa Finanziaria Telefonica
Sgem
Seattle Silicon Technology, Inc.
Sharp Corporation

Sharp Electronics Corporation
Shin-Etsu Handotai Co., Ltd.
Shinko Electric Industries Co., Ltd.
Siemens AG
Siemens Corporation
Sierra Semiconductor Corporation
Signetics Corporation
Silicon Compilers, Inc.
Silicon Design Labs, Inc.
Silicon Systems, Inc.
Sony Corporation
Sperry Semiconductor Operations
Sprague Solid State
Standard Microsystems Corporation
Suwa Seikosha Co., Ltd.
Synertek, Inc.
T V M GmbH
TRW-Active Components
Takeda Riken America, Inc.
Takeda Riken, Ltd.
Tandem Computers, Inc.
Tatung Company
Tegal Corporation
Tektronix, Inc.
Telefunken Electronik GmbH
Telic Alcatel
Teradyne, Inc.
Texas Instruments, Inc.
Thomas Group
Thomson CSF
Thomson CSF DSD
Thomson CSF Semiconductors
Thomson CSF Telephone
Tokyo Electron Limited
Tokyo Sanyo Electric Co., Ltd.
Toshiba America, Inc.
Toshiba Corporation
Toshiba Europa (I.E.) GmbH
Trilogy Systems Corporation
Tristar Semiconductor, Inc.
U.S. Department of Commerce
Union Carbide Corporation
Union Semiconductor Co., Ltd.
United Microelectronics Corporation
United Technologies Corporation
Unitrode Corporation
Universal Semiconductor, Inc.
VLSI Technology, Inc.
VTC Incorporated
Varian Associates
Vitelic Corporation
Vittessé Electronic Corporation
W & W Enterprises
Waferscale Integration, Inc.
Weitek
Western Digital Corporation
Xerox Corporation
Xicor Inc.
Yamada Seisakusho Co., Ltd.
Zilog, Inc.
ZyMOS Corporation
Zytrex Corporation

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SEMICONDUCTOR EQUIPMENT AND MATERIALS SERVICE
October 1985

Alkan International Corporation
Ateq Corporation
Atom Sciences, Inc.
CIT Alcatel
DIELI
Dai Nippon Printing Co., Ltd.
EMC
Emerson Electric Company
GCA Corporation
Hitachi Metals
Hoechst AG
Indium Corporation of America
Intel Corporation
Kimberly-Clark Corporation
Monsanto Electronic Materials Company
Nippon Kogaku K.K.
Olin Corporation
Perkin-Elmer Corporation
Perkin-Elmer Electron Beam Div.
Philip A. Hunt Chemical Corporation
Plessey Semiconductors, Ltd.
Reid-Ashman, Inc.
Siemens AG
Temescal
Union Carbide Corporation
Wacker Siltronic Corporation
Wacker-Chemitronic GmbH
Weston Sales Company

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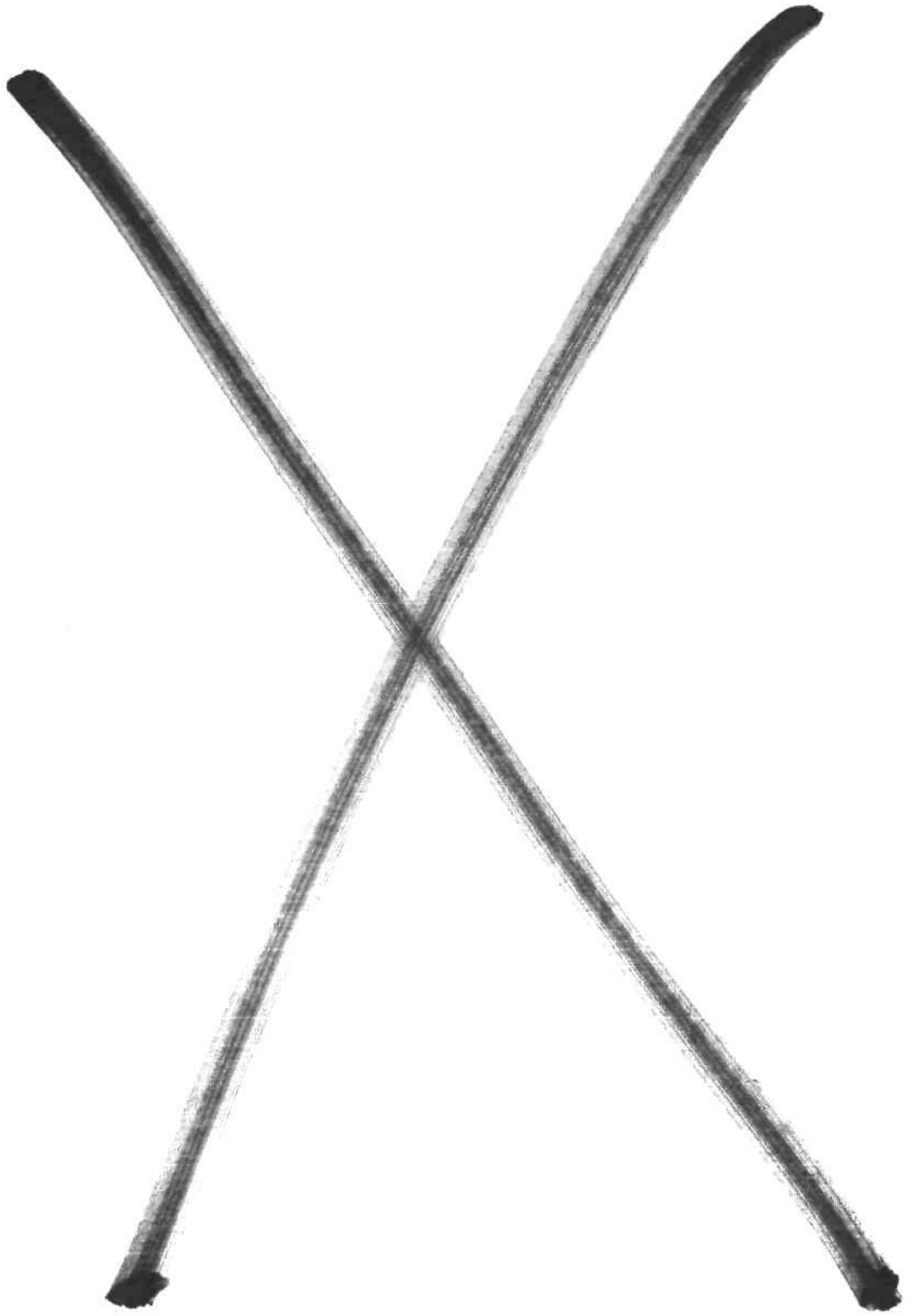
SEMICONDUCTOR APPLICATION MARKETS SERVICE
October 1985

Cirrus Logic, Inc.
Data One
Fujitsu Microelectronics, Inc.
LSI Logic Corporation
Monolithic Memories, Inc.
Motorola, Inc.
RCA Corporation
Siemens AG



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SEMICONDUCTOR INDUSTRY CONFERENCE
SPEAKERS

Howard Z. Bogert
Vice President
Dataquest Incorporated

Andy Prophet
Senior Industry Analyst
Semiconductor Industry Service
Dataquest Incorporated

Robert McGeary
Director
Semiconductor Equipment & Materials Service
Dataquest Incorporated

Richard Gossen, Jr.
President & CEO
Silicon Design Labs, Inc.

K.K. Yawata
President
Nihon LSI

Walter P. Curtis, III
Vice President, Marketing
Silicon Compilers, Inc.

Dr. James Van Tassel
Vice President
NCR Corporation

Mike Hackworth
President & CEO
Cirrus Logic

Art Collmeyer
President
Weitek Corporation

Douglas Fairbairn
Vice President
Design Technology
VTI

F. Joseph Van Poppelen
Vice President
Semiconductor Marketing
National Semiconductor Corporation

George C. Cone
Senior Vice President
Seattle Silicon Technology

Carroll Fencil
Director of Government Systems
Perkin-Elmer Corporation

Anthea Stratigos
Product Manager
Semiconductor Application Markets

Haskell Waddle
Commercial President
Monsanto Electronic Materials Corporation

Kenneth Levy
President
KLA Corporation

Dave House
General Manager
Micro Computer Group
Intel Corporation

Mel Thomsen
Associate Director
Semiconductor Industry Service
Dataquest Incorporated

Alex Au
President
Vitelic Corporation

Alan Grebene
President
Micro-Linear Corporation

Eli Harari
President
Wafer Scale Integration, Inc.

Wallace F. Davis
General Partner
Alpha Partners

Dr. Hiroyoshi Komiya
Deputy Manager
Mitsubishi Electronics

Nikita Andrieiv
Director of Education
AWI Corporation

Clyde V. Prestowitz
Counselor to the Secretary
U. S. Department of Commerce

Jerome G. Rivard
Chief Engineer
Ford Motor Company

Stanley Mazor
Manager
Applications Engineering
Silicon Compilers, Inc.

John Banning
Independent Computer
Consultant

Skip Stritter
Vice President, Engineering
MIPS Computer Systems

Dan Ling
Manager, Microsystems
IBM Corporation
Thoms J. Watson Research
Center

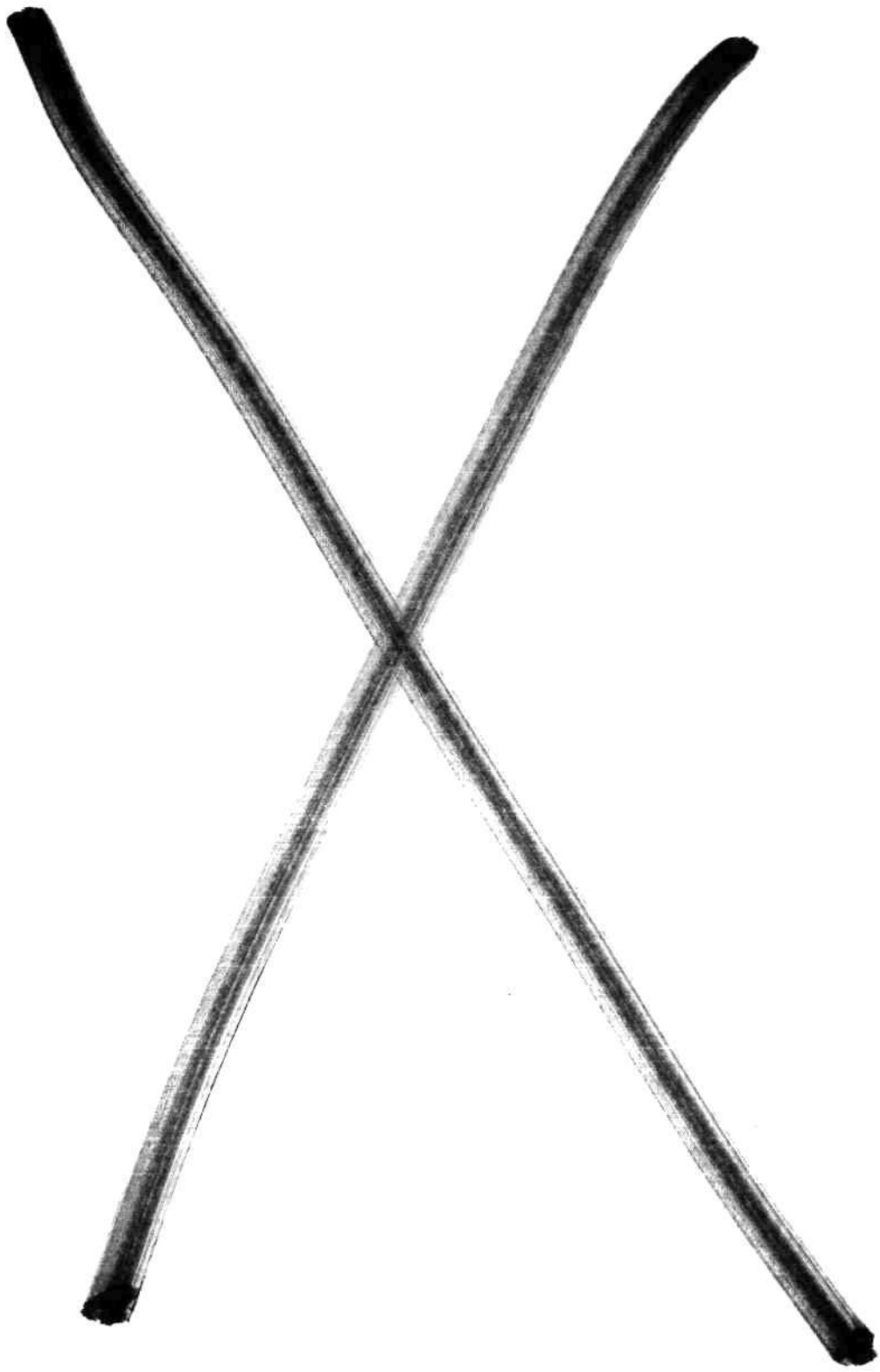
Dr. James Burnett
President
Institute of
Microcontamination Control

Joseph Grenier
Senior Industry Analyst
Semiconductor Equipment &
Materials Service
Dataquest Incorporated

Larry Sumney
President
Semiconductor Research
Corporation

Bengt Soderberg
Vice President
Group Purchase Division
LM Ericsson

Anthony Livingston
Vice President
Gigabit Logic



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CONSUMPTION, CAPACITY, CATASTROPHE

Howard Z. Bogert
Vice President
Dataquest Incorporated

Mr. Bogert is a Vice President of DATAQUEST and Director of its Semiconductor Industry Group. During his 24 years in electronics, Mr. Bogert has held management positions in market research, product planning, long-range planning, research and development, and engineering. Before coming to DATAQUEST, he was a Divisional Vice President of Engineering for Rockwell International. Prior to that, he was Director of MOS Development for Siliconix and Manager of Design for AMI. Mr. Bogert received a B.S. degree in Electrical Engineering from Stanford University, an M.S. degree from the University of Maryland, and an M.B.A. degree from the University of Santa Clara.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
October 14, 15, and 16, 1985
Tucson, Arizona

SEMICONDUCTORS

AN UNUSUAL BUSINESS

Dataquest Incorporated, A Subsidiary of A.C. Nielsen Company / 1290 Ridder Park Drive / San Jose, CA 95131 / (408) 971-9000 / Telex 171973

WHAT DETERMINES SEMICONDUCTOR DEMAND?

- DATAQUEST'S CURRENT FORECAST
- STRATEGIC CONSIDERATIONS

WHAT DETERMINES SEMICONDUCTOR DEMAND?

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THE CONSUMPTION OF ELECTRONIC FUNCTIONS IS NOT LIMITED BY ANY PHYSICAL CONSTRAINT

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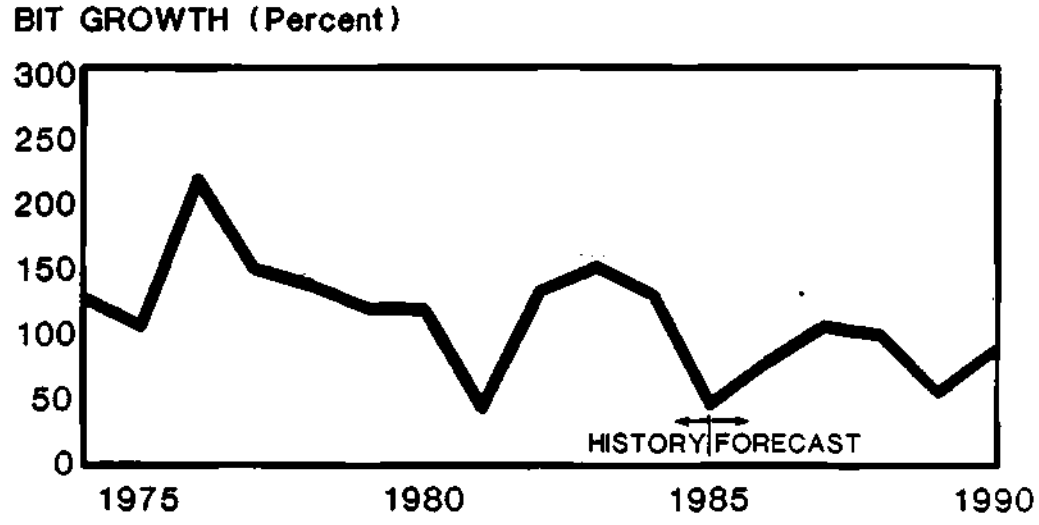
YEAR-TO-YEAR GROWTH IN WORLDWIDE CONSUMPTION OF READ/WRITE MEMORY BITS



Source: DATAQUEST

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WHAT ABOUT 100% CONSUMPTION GROWTH IN:

- CALORIES CONSUMED
- AUTOMOBILES
- AUTOMOBILE MILEAGE
- HOUSES
- DINNERS OUT
- ACCOUNTING SERVICES
- PAPER CLIPS

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WHAT ABOUT 100% CONSUMPTION GROWTH IN: (Continued)

- SHADES OF LIPSTICK
- TYPES OF RESTAURANTS
- JUNK MAIL

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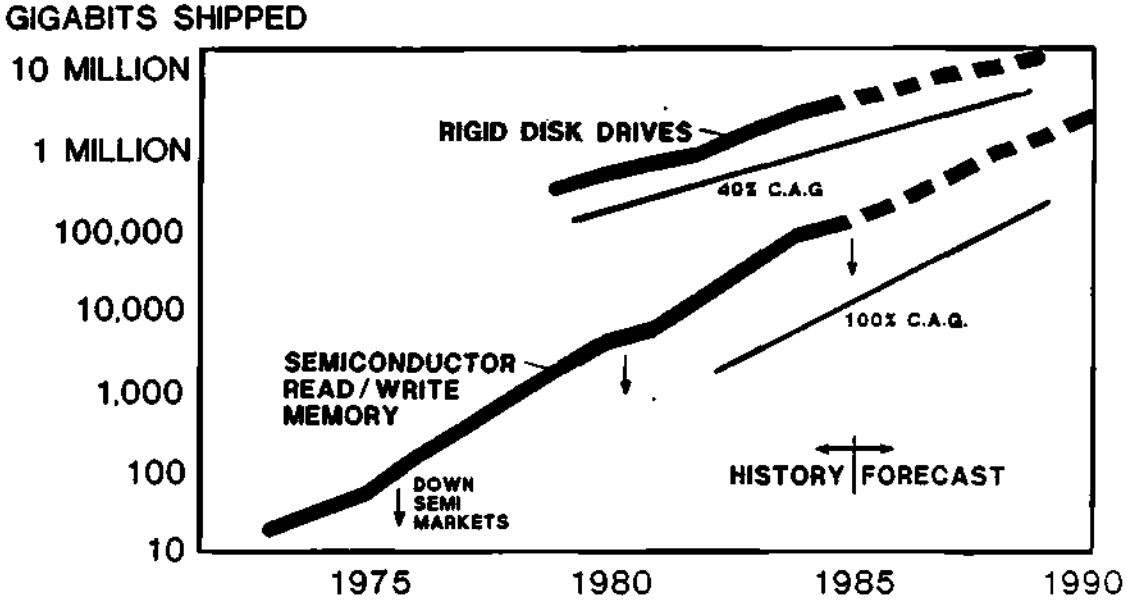
CONSUMPTION COMPARISON OF RIGID DISK AND SEMICONDUCTOR READ/WRITE MEMORY BITS



Source: DATAQUEST

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PRICE COMPARISON OF RIGID DISKS AND READ/WRITE MEMORY BITS

FACTORY PRICES PER MEGABIT

	1980	1985	1990 (EST.)
RIGID DISKS	$6.52	$2.20	$1.03
SEMICONDUCTORS	$350.00	$24.00	$4.38
RATIO	54:1	11:1	4 1/4:1

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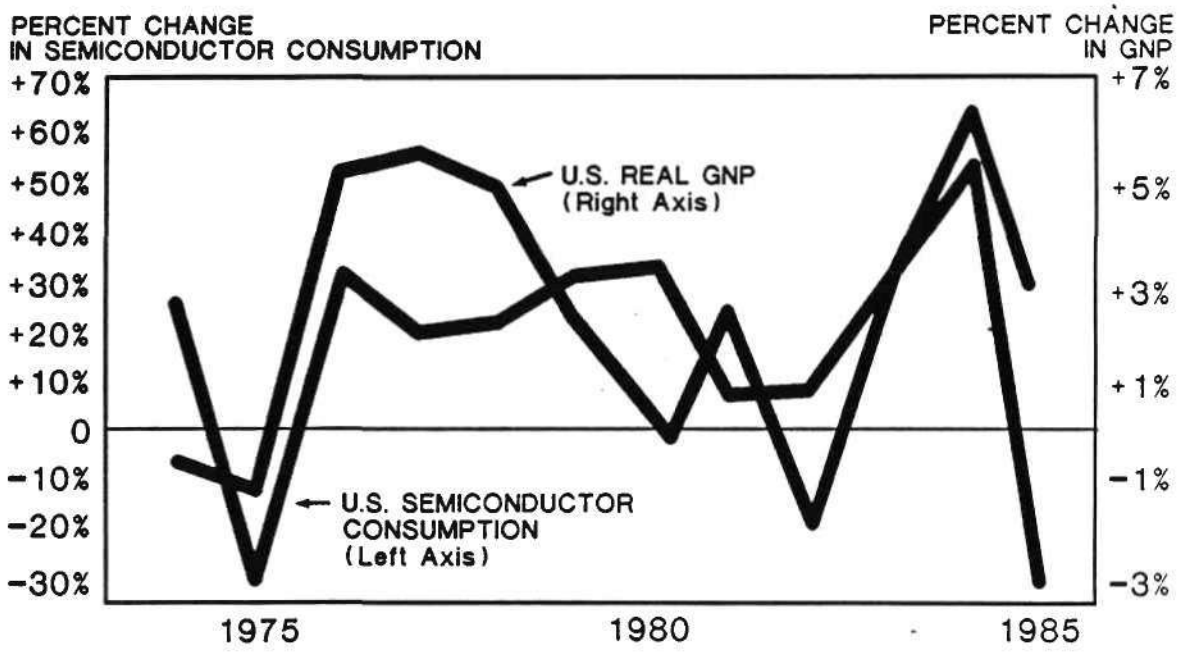
PRICE COMPARISON OF RIGID DISKS AND READ/WRITE MEMORY UNITS

FACTORY PRICES PER UNIT

	1980	1985	1990 (EST.)
RIGID DISKS	$12,880	$3,230	$1,150
SEMICONDUCTORS	$4.53	$1.94	$3.29

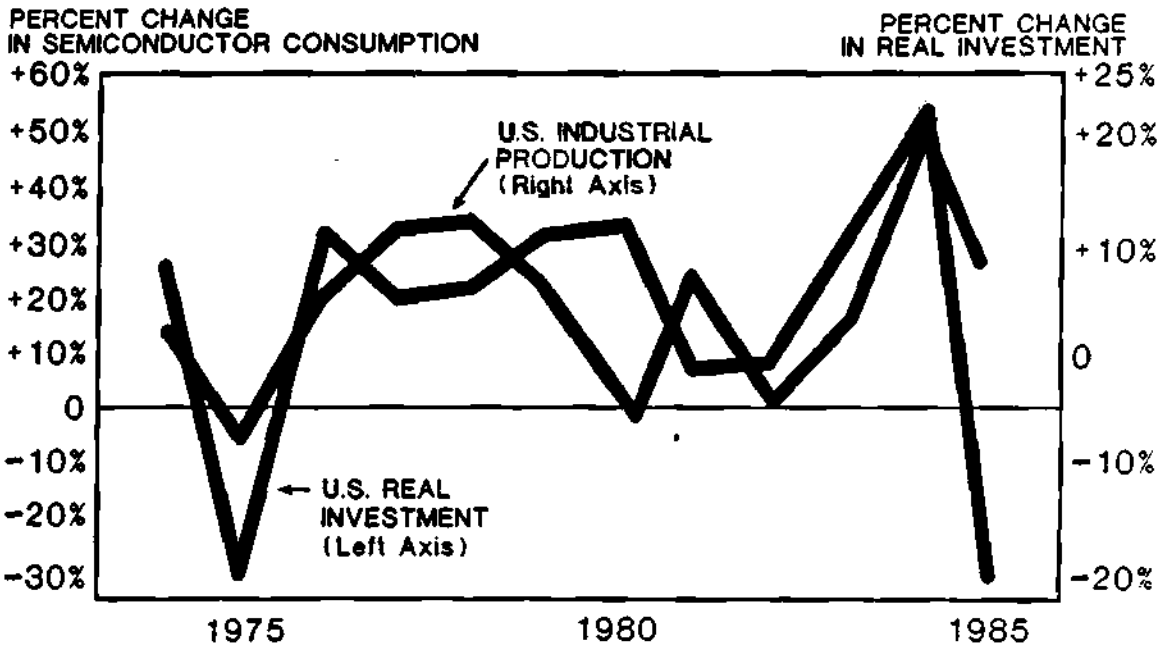
Source: DATAQUEST

COMPARISON OF CHANGES IN U.S. SEMICONDUCTOR CONSUMPTION AND U.S. GNP



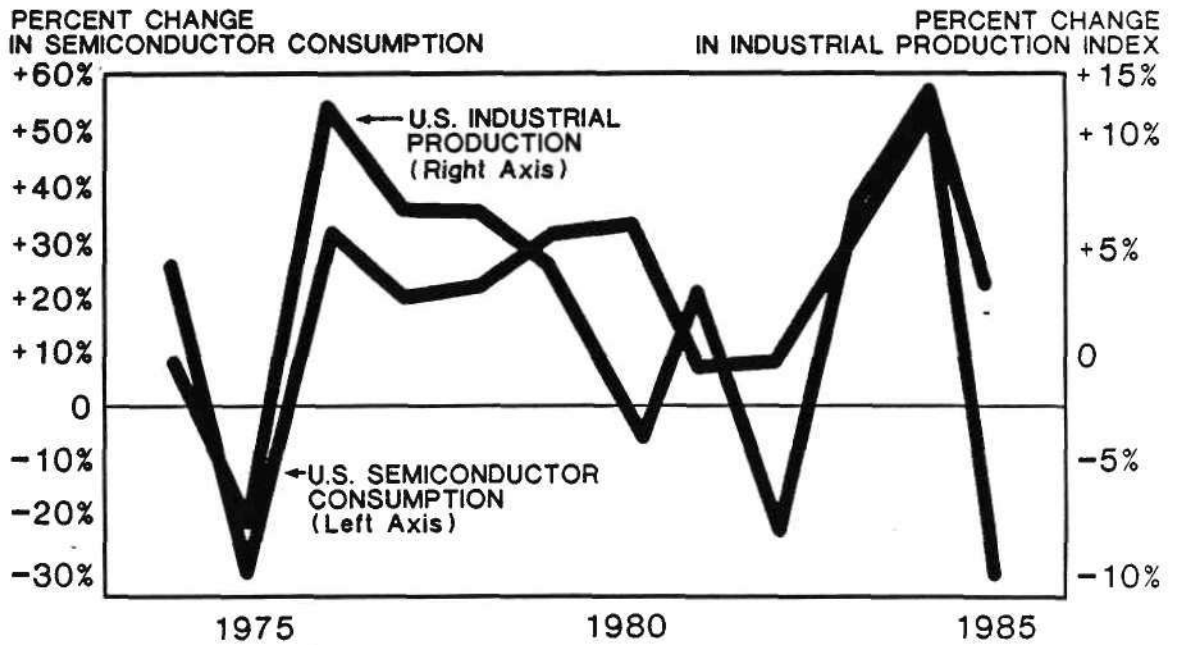
Source: DATAQUEST

COMPARISON OF CHANGES IN U.S. SEMICONDUCTOR CONSUMPTION AND U.S. REAL INVESTMENT



Source: DATAQUEST

COMPARISON OF CHANGES IN U.S. SEMICONDUCTOR CONSUMPTION AND U.S. INDUSTRIAL PRODUCTION INDEX



Source: DATAQUEST

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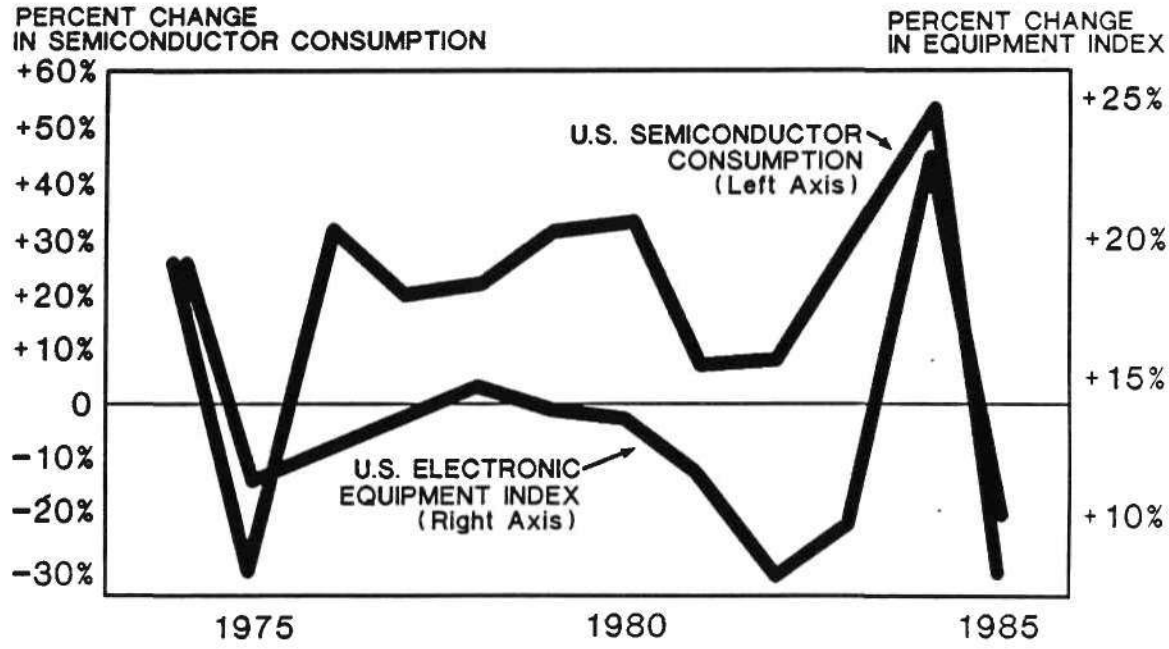
COMPARISON OF U.S. SEMICONDUCTOR CONSUMPTION AND U.S. ELECTRONIC EQUIPMENT INDEX



Source: DATAQUEST

ESTIMATED FUNCTIONAL SEMICONDUCTOR CONSUMPTION PER UNIT IN THE APPLE/ MACINTOSH PERSONAL COMPUTER

	1984	1985
AVERAGE MEMORY SIZE (BYTES)	128K	240K
MICRO DEVICES (PACKAGES)	4	4
LOGIC (PACKAGES)	19	19
PROGRAMMABLE LOGIC (PACKAGES)	5	5
ROM	2	2

Source: DATAQUEST

ESTIMATED DOLLAR SEMICONDUCTOR CONSUMPTION PER UNIT IN THE APPLE/ MACINTOSH PERSONAL COMPUTER

	1984	1985	CHANGE
MEMORY	$48	$24	-50%
LOGIC	112	71	-37%
TOTAL	$160	$95	-41%

Source: DATAQUEST

ESTIMATED SEMICONDUCTOR CONSUMPTION IN THE APPLE/MACINTOSH PERSONAL COMPUTER

	1984	1985	CHANGE
AVERAGE RETAIL PRICE	$2,650	$2,010	-24%
SEMICONDUTORS CONSUMED	$160	$95	-41%
INPUT/OUTPUT RATIO	6.0%	4.7%	-21%

Source: DATAQUEST

ESTIMATED TOTAL SEMICONDUCTOR CONSUMPTION IN THE APPLE/MACINTOSH PERSONAL COMPUTER

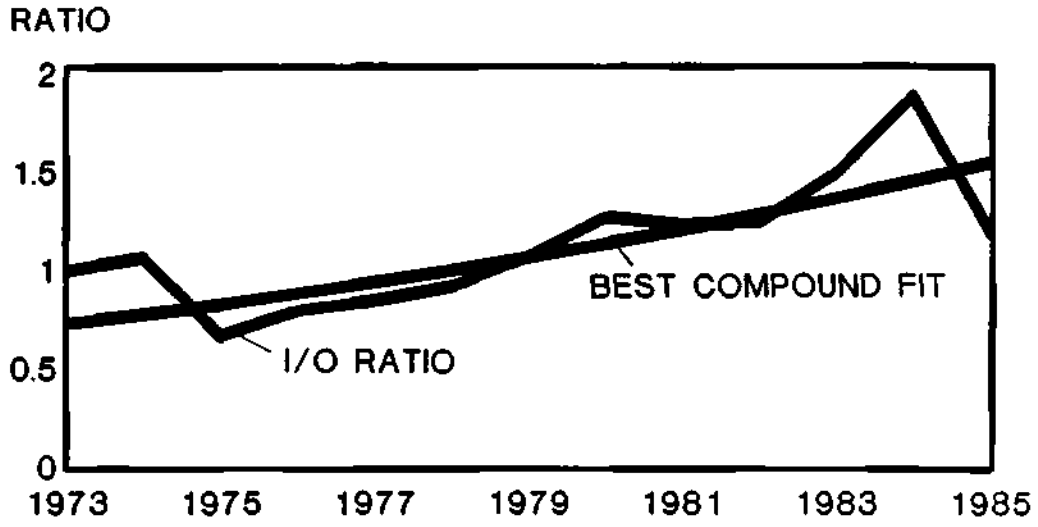
CHANGE IN CONSUMPTION 1985/1984

UNITS SHIPPED	SEMICONDUCTORS PER UNIT	TOTAL SEMICONDUCTOR CONSUMPTION
-10%	-41%	-47%

Source: DATAQUEST

SEMICONDUCTOR TO EQUIPMENT

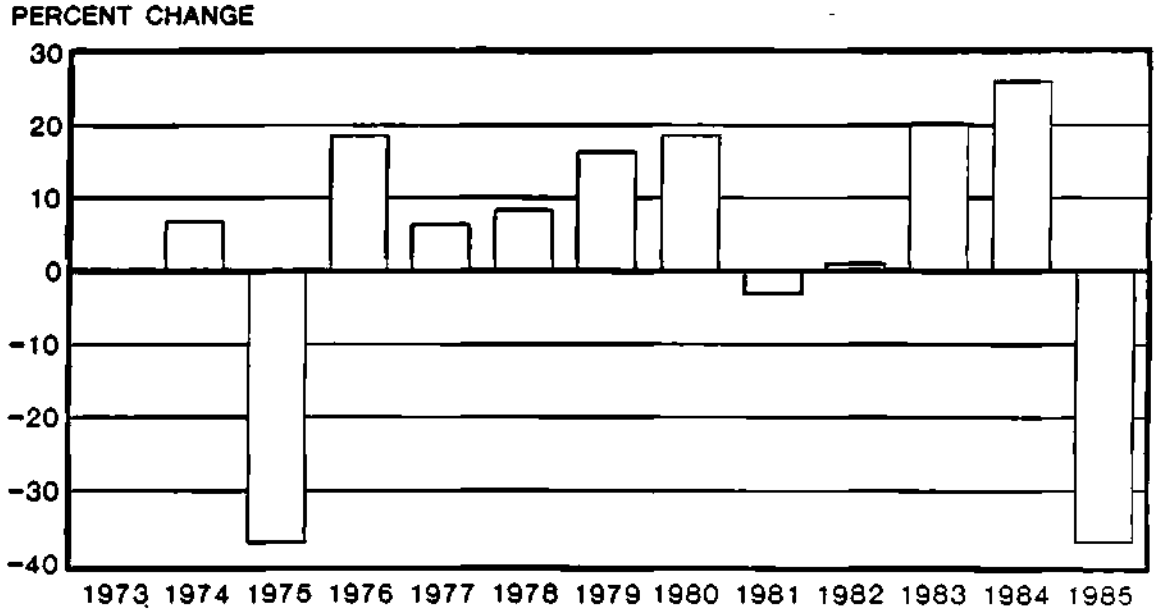
INPUT/OUTPUT RATIO



Source: DATAQUEST

CHANGES IN SEMICONDUCTOR TO EQUIPMENT

INPUT/OUTPUT RATIO



Source: DATAQUEST

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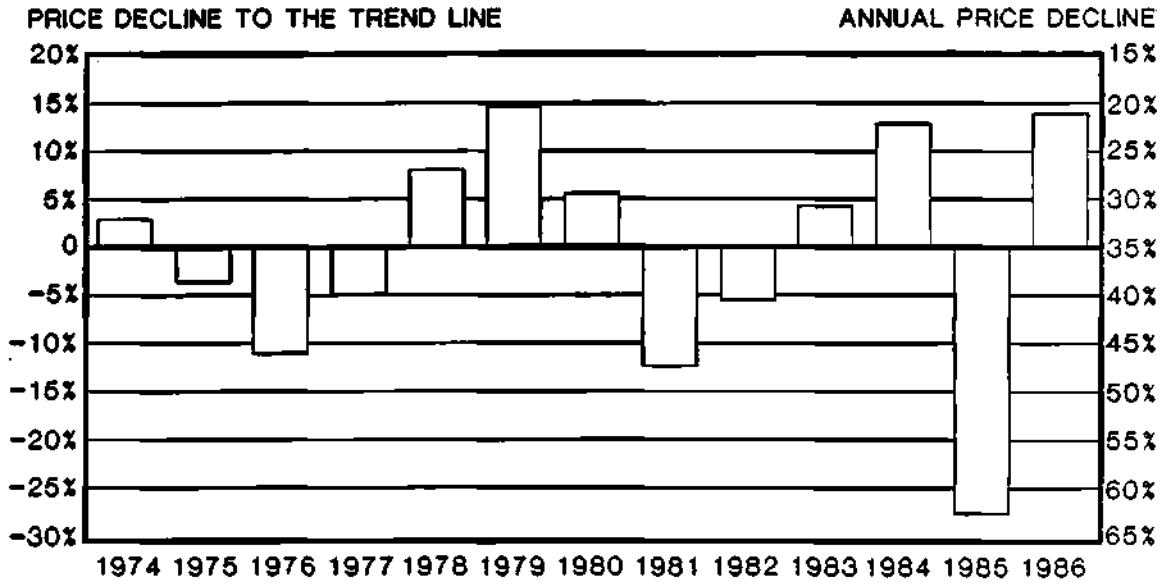
READ/WRITE MEMORY PRICE PER BIT

CHANGES RELATIVE TO TREND LINE



Source: DATAQUEST

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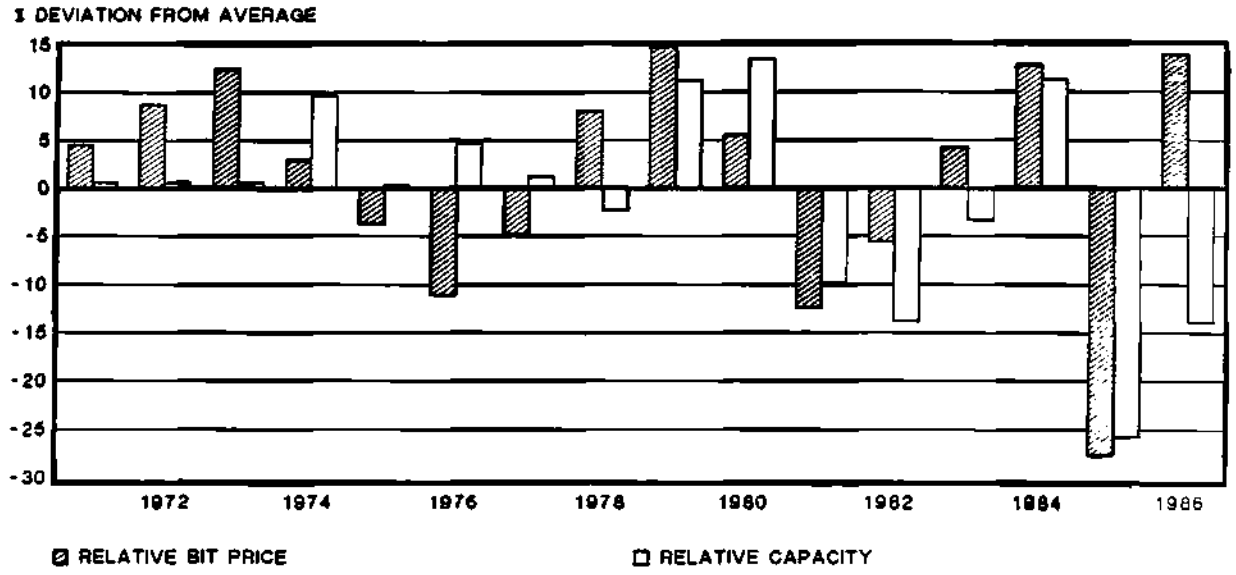
RELATIONSHIP BETWEEN RELATIVE BIT PRICE

AND PERCENT CAPACITY UTILIZATION



Source: DATAQUEST

IMPACT OF FUNCTION PRICE CHANGES

CHANGE IN CONSUMPTION 1985/1984

	FUNCTIONAL UNITS	PRICE PER FUNCTION	MARKET IN DOLLARS
READ/WRITE MEMORY (BITS)	+46%	-63%	-46%
READ ONLY MEMORY (BITS)	+65%	-51%	-19%
MICROPROCESSORS (BYTES)	+ 4%	-21%	-18%
MICROCONTROLLERS (BYTES)	+20%	-33%	-19%
GATE ARRAYS (GATES)	+81%	-35%	+18%

Source: DATAQUEST

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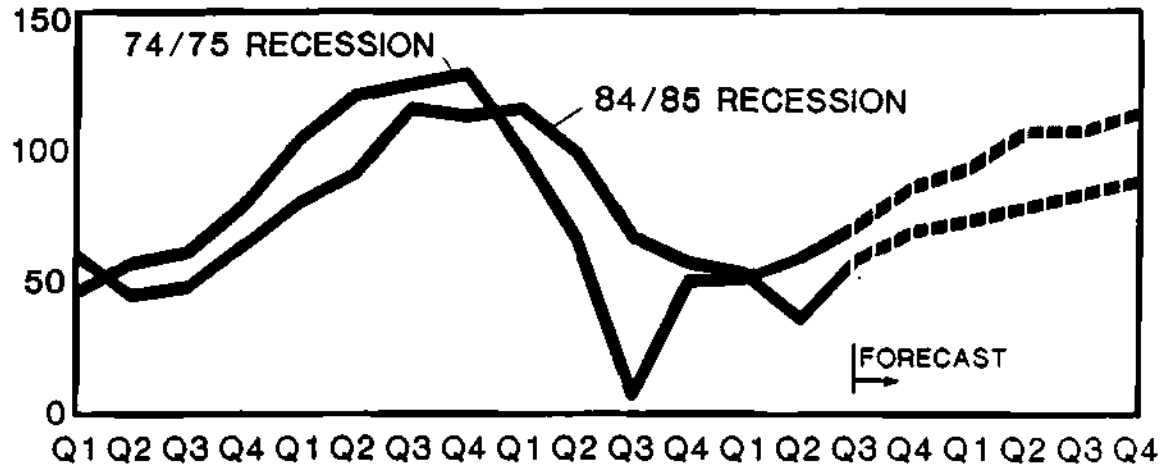
INDUSTRY BOOKINGS

1974/1975 RECESSION AND 1984/1985 RECESSION

PERCENT OF PEAK



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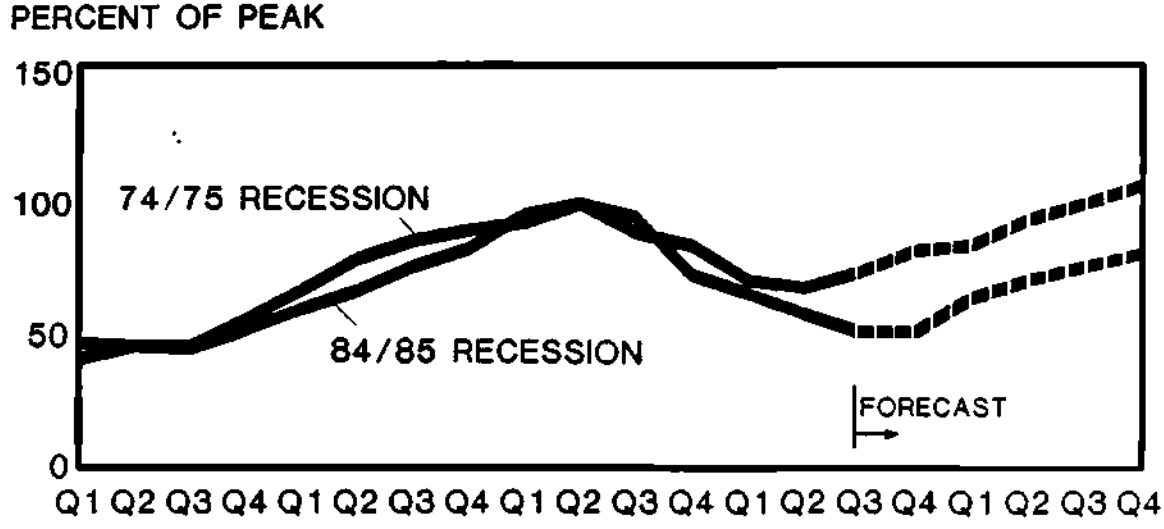
INDUSTRY BILLINGS

1974/1975 RECESSION AND 1984/1985 RECESSION



ESTIMATED QUARTERLY U.S. SEMICONDUCTOR CONSUMPTION

(Millions of Dollars)

	QUARTER 1	QUARTER 2	QUARTER 3	QUARTER 4	TOTAL
1985					
IC	$2,328	$2,068	$1,675	$1,386	$7,457
DISCRETE	448	430	403	407	1,688
TOTAL	$2,776	$2,498	$2,078	$1,793	$9,145
% CHANGE	-19.5%	-10%	-16.8%	-13.7%	-31.4%
1986					
IC	$1,436	$1,824	$2,184	$2,712	$8,156
DISCRETE	431	465	480	510	1,886
TOTAL	$1,867	$2,289	$2,664	$3,222	$10,042
% CHANGE	4.1%	22.6%	16.4%	20.9%	9.8%

Source: DATAQUEST

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STRATEGIC CONSIDERATIONS

- FOCUS ON THE APPLICATION
- ELIMINATE THE NEED FOR SECOND SOURCES
- CORNER ENGINEERING RESOURCES
- GET IN TOUCH WITH THE BILLION-TRANSISTOR ARCHITECTS

STRATEGIC CONSIDERATIONS (Continued)

- CONSIDER ALTERNATE WAFER FABRICATION STRATEGIES
- BUILD NEW PLANTS WHEN EVERYBODY ELSE ISN'T
- GENERATE CASH AT BUSINESS CYCLE TROUGHS

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CONSUMPTION CAPACITY CATASTROPHE

THE SEMICONDUCTOR SAGA

Howard Bogert
Robert McGeary

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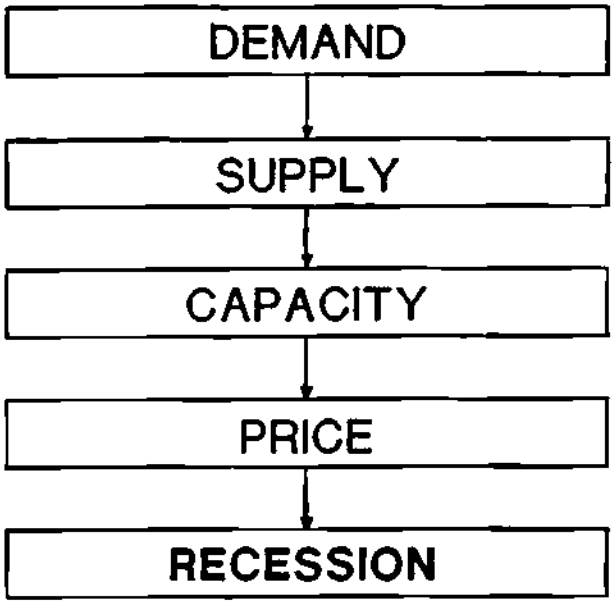
AGENDA



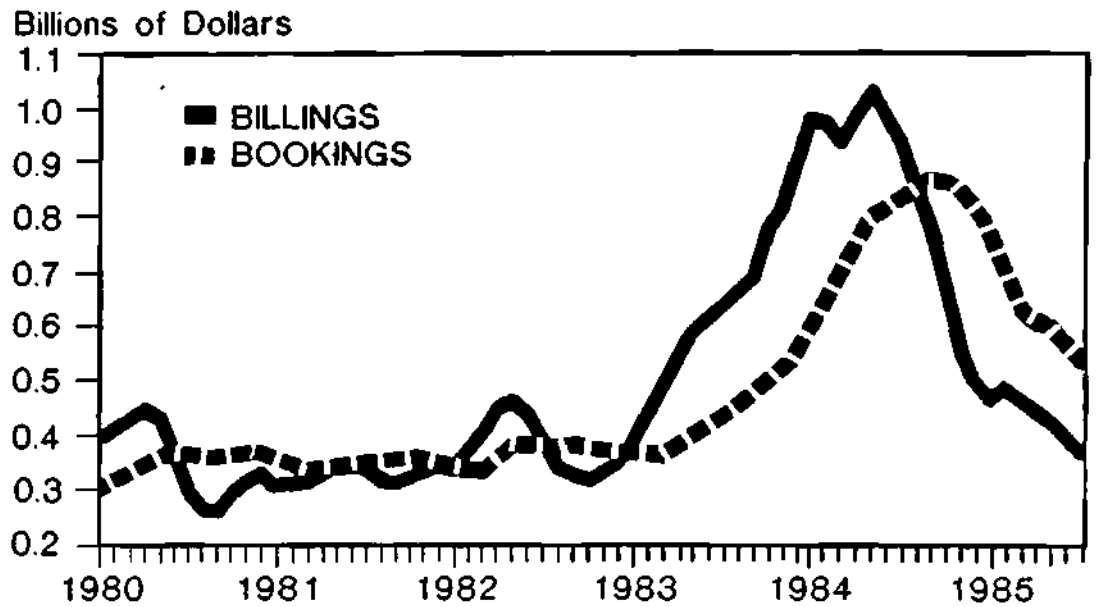
DEMAND

CONSUMER DRIVEN

SAVINGS RATE
INVESTMENT ALTERNATIVES
CREDIT RATE
TAX RATE
MONEY SUPPLY
INVENTORY
ADVERTISING
NEEDS

SEMICONDUCTOR DEMAND MEASURED BY BOOK/BILL RATIO

BOOKINGS VS. BILLINGS BY MONTH (1980-1985)



Source: DATAQUEST

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SEMICONDUCTOR DEMAND

BOOK-TO-BILL RATIO

- IS VERY INELASTIC
- LEADS BILLINGS BY FIVE MONTHS
- AVERAGE IS 1.09
- HAS NO RELIABLE PREDICTOR!

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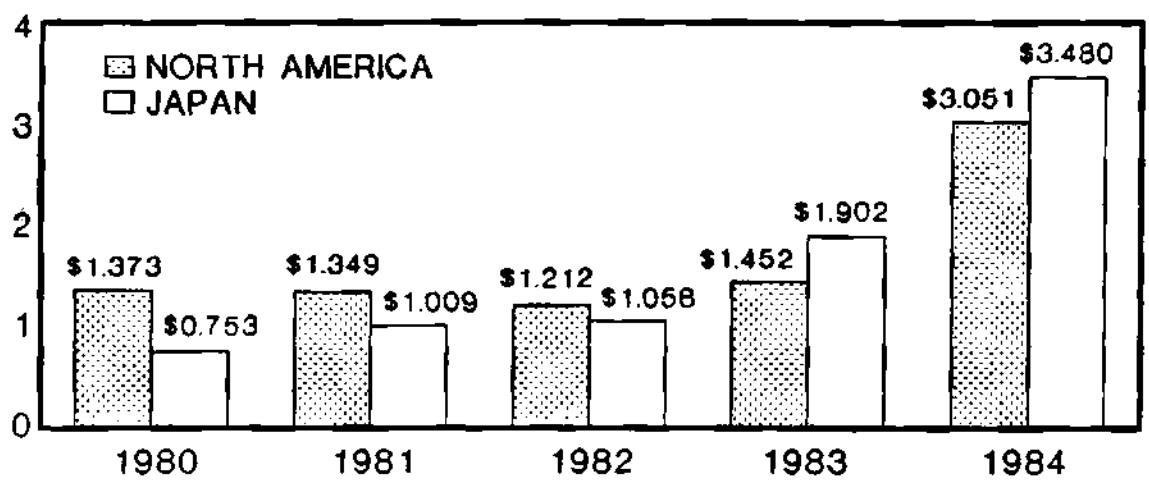
SEMICONDUCTOR SUPPLY--
CAPITAL SPENDING

U.S. AND JAPAN CAPITAL SPENDING
(1980-1984)



Source: DATAQUEST

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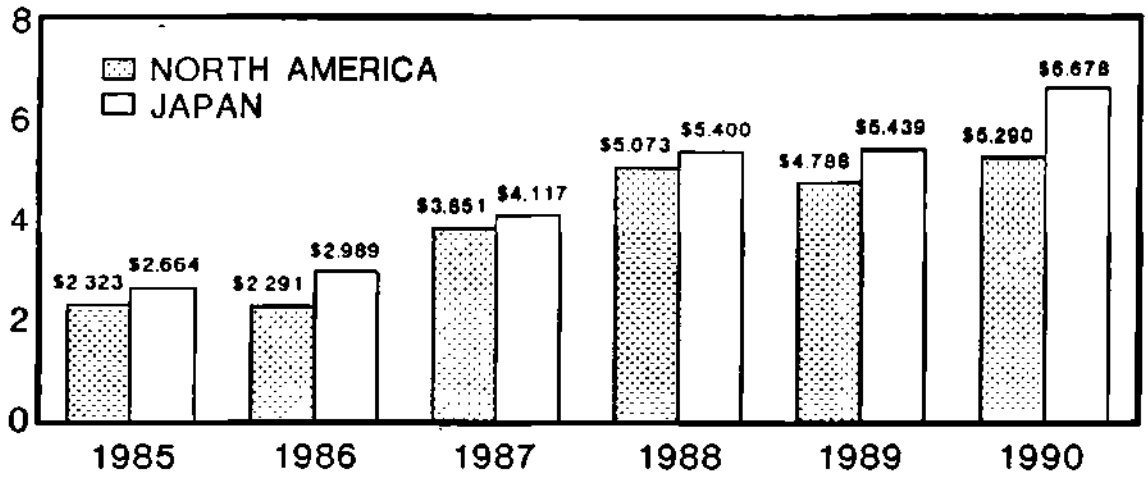
CAPITAL SPENDING

U.S. VS. JAPAN

U.S.	JAPAN
EQUITY	DEBT
LOW DEBT/EQUITY	HIGH DEBT/EQUITY
5% SAVINGS RATE	20% SAVINGS RATE
BANKERS ADVERSARIAL	BANKERS PARTNERS
MARGIN MOTIVE	CASH FLOW MOTIVE
GROW EQUITY	COVER DEBT BURDEN
PROFITABILITY	MARKET SHARE
COST OF CAPITAL 12%	COST OF CAPITAL 6%
INDEPENDENT	CAPTURED

SEMICONDUCTOR SUPPLY--
FORECASTED CAPITAL SPENDING

U.S. AND JAPAN CAPITAL SPENDING
(1985-1990)



Source: DATAQUEST

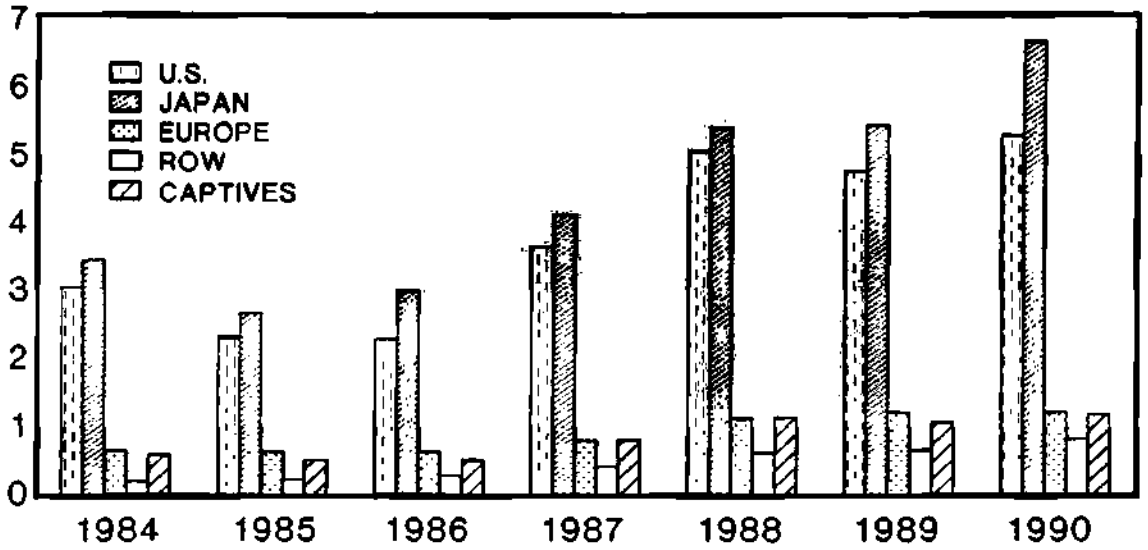
CAPITAL SPENDING

FORECAST ASSUMPTIONS

- DATAQUEST'S FORECAST FOR SEMICONDUCTOR REVENUE
- CAPITAL/REVENUE STEPPED FROM 1975 TO 1985
- TREND CONSTANT AFTER 1985
- U.S. CAPITAL/REVENUE LAGS REVENUE SEVEN MONTHS
- JAPAN CAPITAL/REVENUE COINCIDENT WITH REVENUE

CAPITAL SPENDING WORLDWIDE

1984-1990



Source: DATAQUEST

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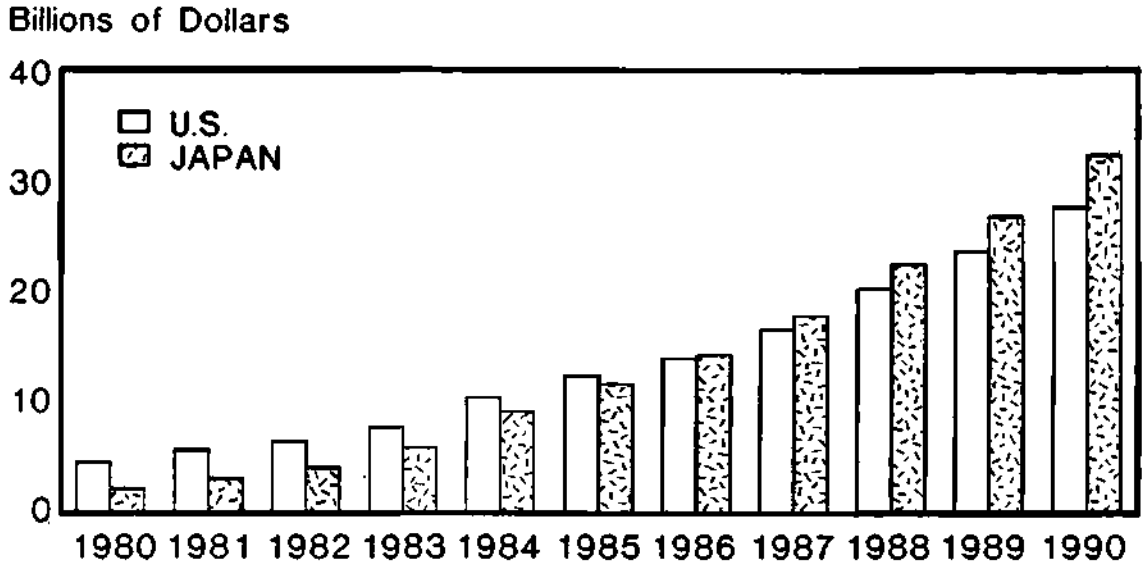
INSTALLED BASE--U.S. VS. JAPAN

PROPERTY, PLANT, AND EQUIPMENT



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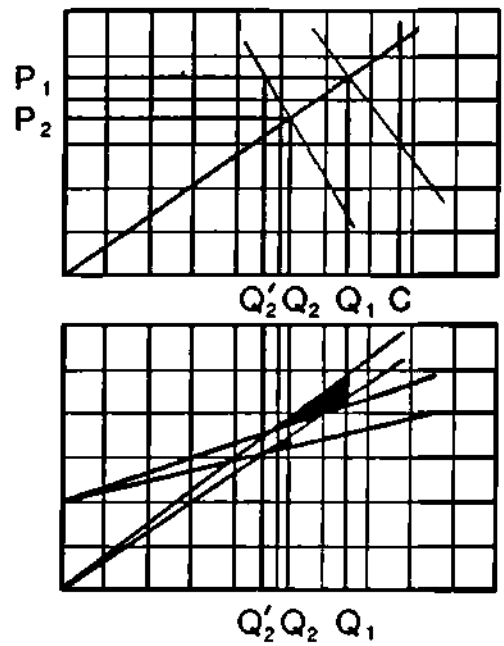
CAPACITY

MANUFACTURING ECONOMICS



BREAKEVEN ANALYSIS

Source: DATAQUEST

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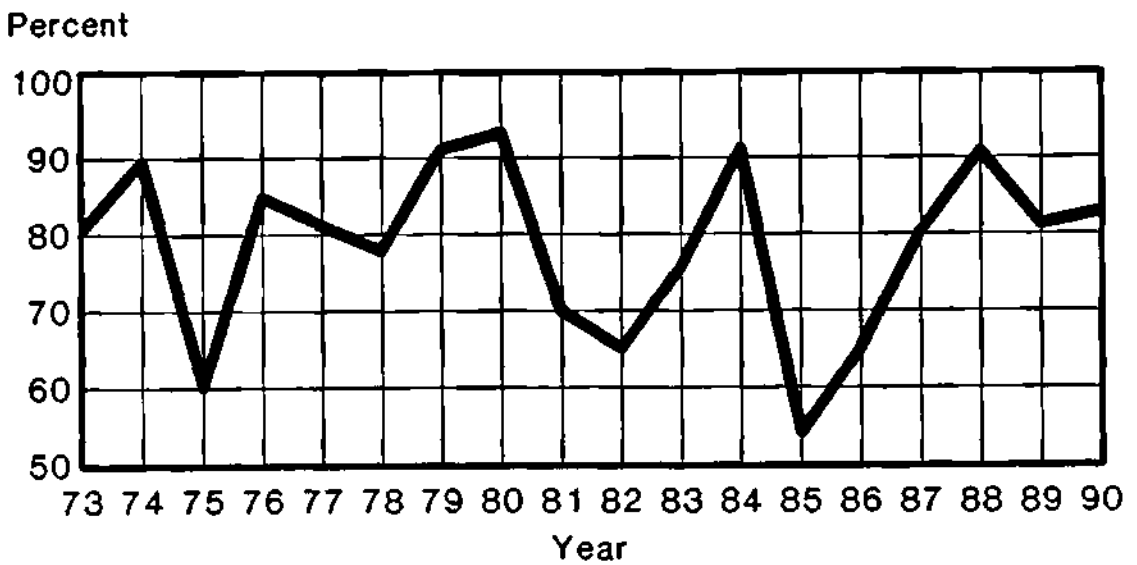
CAPACITY--MANUFACTURING CARDIOGRAM

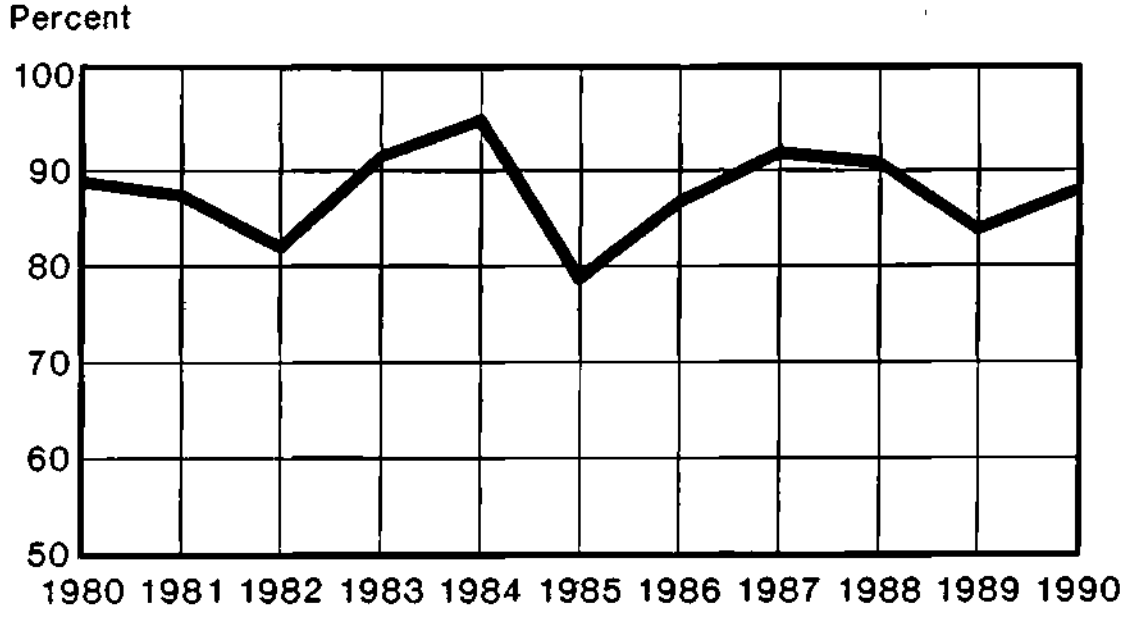
U.S. CAPACITY UTILIZATION
North American Companies



Source: DATAQUEST

CAPACITY--MANUFACTURING KNOW-HOW

JAPAN PERCENT CAPACITY



Source: DATAQUEST

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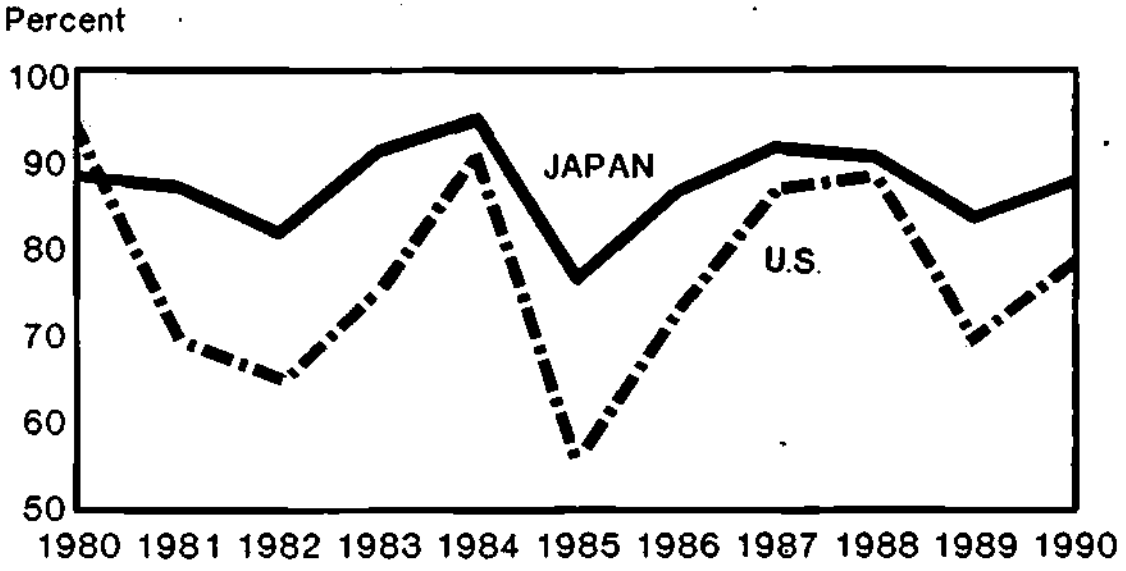
CAPACITY--TWO CULTURES

U.S. VS. JAPANESE CAPACITY UTILIZATION



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Nielsen Dataquest

ASICs IN JAPAN

Keiske Yawata
Chief Executive Officer
Nihon LSI Logic Corporation and
Nihon Semiconductor Inc.

Mr. Yawata is Chief Executive Officer of Nihon LSI Logic Corporation and Nihon Semiconductor Inc., both Japanese affiliates of LSI Logic Corporation of Milpitas, California. Previously, he was President and Chief Executive Officer of NEC Electronics Inc., after having served as General Manager of NEC's International Electron Devices Division. Mr. Yawata received a B.E. degree in Electrical Communication Engineering from Osaka University and an M.E.E. degree from the Electrical Engineering School of Syracuse University, where he attended graduate school on a Fulbright Scholarship.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
October 14, 15, and 16, 1985
Tucson, Arizona

日本ＡＳＩＣ市場　　"ＡＳＩＣ　ｉｎ　Ｊａｐａｎ"

1. Diversification of Application

The appplication of IC initially centered around main frame EDP and telecommunication equipment. As the capacity of memory IC increased, that application grew rapidly in EDP area. The development of microprocessors made EDP and telecom terminals smarter. The application specific IC further increased the use of semi-custom IC in such a way that prototype quantities of ASIC can be economically developed within a few weeks. The CAD software oriented system enables designers to simulate many circuit performance before the circuit is fabricated in silicon. Many ASIC suppliers agree to design and fabricate prototype IC's without a follow-on production contract. It gives researchers and designers more latitude in the use of semicustom IC's in programs such as the 5th Generation Super Speed Computer.
So called "mechatronics" which is a Japanese/English word for the application of electronics in machinery such as robots, printing machines, copying machines, automobiles, video games, precision machinery and many other conventional machines and equipment. These applications are ideally suited for ASIC because the users' needs for a small quantity of custom designed devices with different specifications can easily be fulfilled without a prohibitively high cost.

2. Energy Saving and Reduction in Size

The proliferation of IC's made electronic products shrink in size and consume less power which perfectly matched the popular Japanese saying "Kei-Haku-Tan-Sho" which means lighter weight, thinner, shorter and smaller in dimensions. Some examples of "Kei-Haku-Tan-Sho" are Walkman™, 8 mm video camera, LCD TV, and credit card size calculator, to name a few. Using discrete IC's instead of mechanical and electromagnetic parts and gate-arrays instead of TTL lead the mechatronics to low energy consumption and

Walkman is a registered trademark of Sony Corporation.

Kei-Haku-Tan-Sho. CMOS technology in particular played an important role in energy saving. This slogan or theme ideally suited the situation Japan faced at the time of the energy crisis. By pursuing Kei-Haku-Tan-Sho Japan developed compact cars, compact discs, and many other electronic devices which have a high potential for gate arrays. Because of the popularization of TTL and microprocessors designers commonly used them in the elcetronic circuits designed.

In order to further reduce weight and size TTL and microprocessor components must be eliminated and the entire printed circuit board or even several boards be integrated in a gate array. Sophisticated CAD software exists to replace these boards with gate arrays or other ASIC devices which results in Kei-Haku-Tan-Sho. There are still many opportunities for ASIC to take over from conventional electronic circuits.

3. Oversupply of Commodity IC

The current over capacity situation forced most broad line IC suppliers to shift their product mix toward semi and full custom products because of the abundance of marketing opportunities. The price of a 64K DRAM is as low as 40 cents and a 256K DRAM dropped from 4 dollars earlier this year to 1.70 dollars today and has become unattractive to manufacture. Although the price of ASIC has also declined, it is still at a reasonable level and one can be profitable manufacturing ASIC which invited more competition. ASIC technology is not something which can be developed overnight. It requires CAD software. The lack of CAD software capability drives many salesmen to rely on low prices because they do not have other strenghts to use in selling ASIC. Hopefully buyers and purchasing managers know that ASIC suppliers should first be chosen for their CAD software, not for their price, because good ASIC is designed with good CAD software. There are many other elements which are far more important than price, i.e., variety of packages available to encapsulate an ASIC in, performance and speed of the gate, scale of integration the CAD software may correctly handle, turn around time of proto-typing, first time accuracy of design and the size of the macro-cell library. A price quotation based on a per-gate-price is a ridiculous way to value ASIC.

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4. Diversification of ASIC

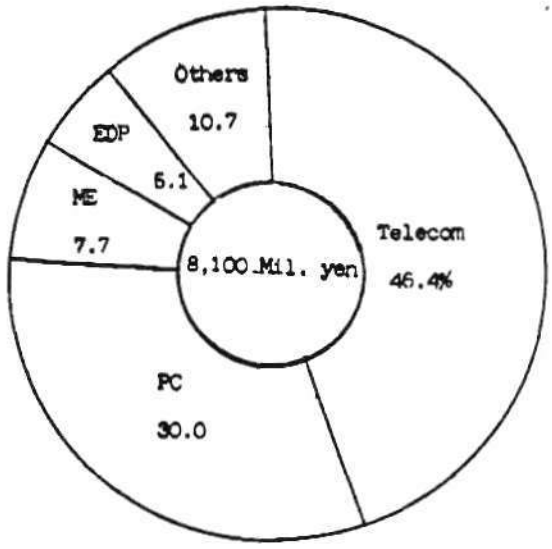
As CAD software becomes more sophisticated and wafer processing technology is more refined, the density of ASIC increases and consequently the circuit performance diversifies. For this to happen the library of macrocells and building blocks must be expanded. Japanese customers expect ASIC suppliers' development support system and product development capability to be reliable, i.e., broad ASIC product line, strong development system and quick turn around time. Major Japanese gate array suppliers are responding to such expectation by building more design centers, developing higher density arrays with new building blocks including ROM, RAM and PLA. The prevailing technology is 2.0 μ Si gate CMOS process with double metal layer, but 1.5 μ technology is emerging. Demand for complex ASIC such as analog functions, CPU and peripheral fuctions integrated with logic circuitry is also popular among ASIC users.

5. Impact of Software Development

Japan is one nation where hardware value is viewed more important than software value. Although the software is beginning to be valued, the level of recognition is not sufficiently high. Design service is often times given away, if there is a significant volume of components. If software is not given sufficient value, the software development activities are discouraged and copyright is not respected. The fact that a copyright legislation has been enacted in Japan may indicate the increase of awareness toward software and if it is a trend, the awareness will be reflected in the marketing andpurchasing activities. When the software is given full citizen ship, the ASIC will really flower in Japan.

(Fig. 1) Application of CMOS Gate Arrays by Sector in Japan

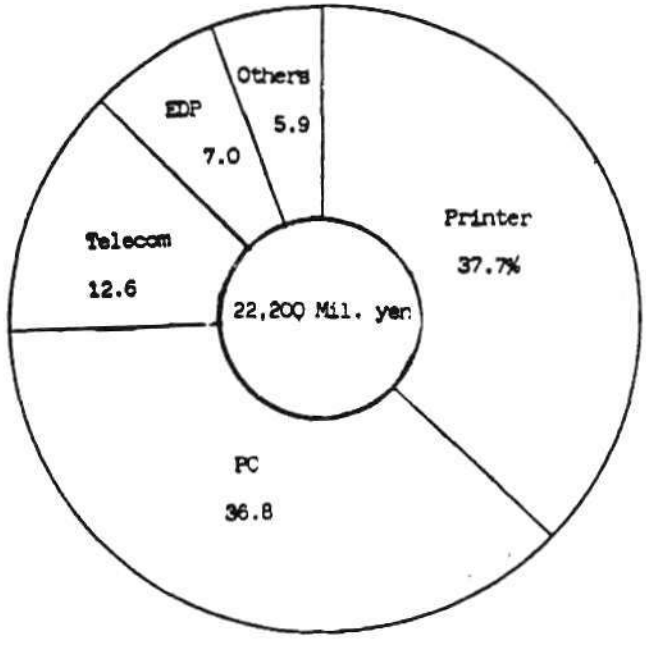
(1982)



(Source: Yano Keizai)

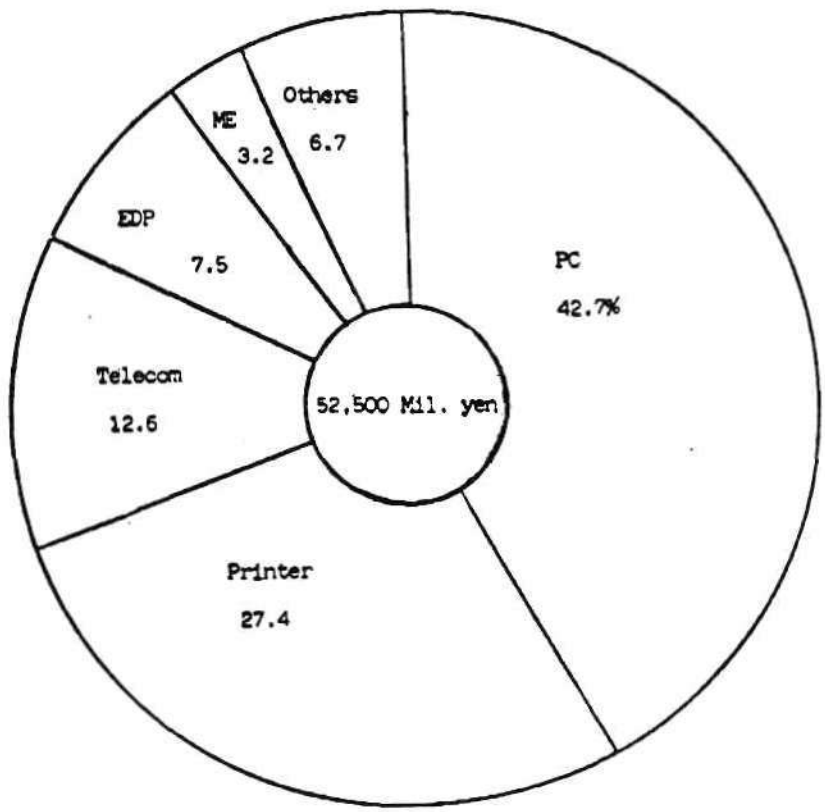
(Fig. 2) Application of CMOS Gate Arrays by Sector in Japan

(1983)



(Source: Yano Keizai)

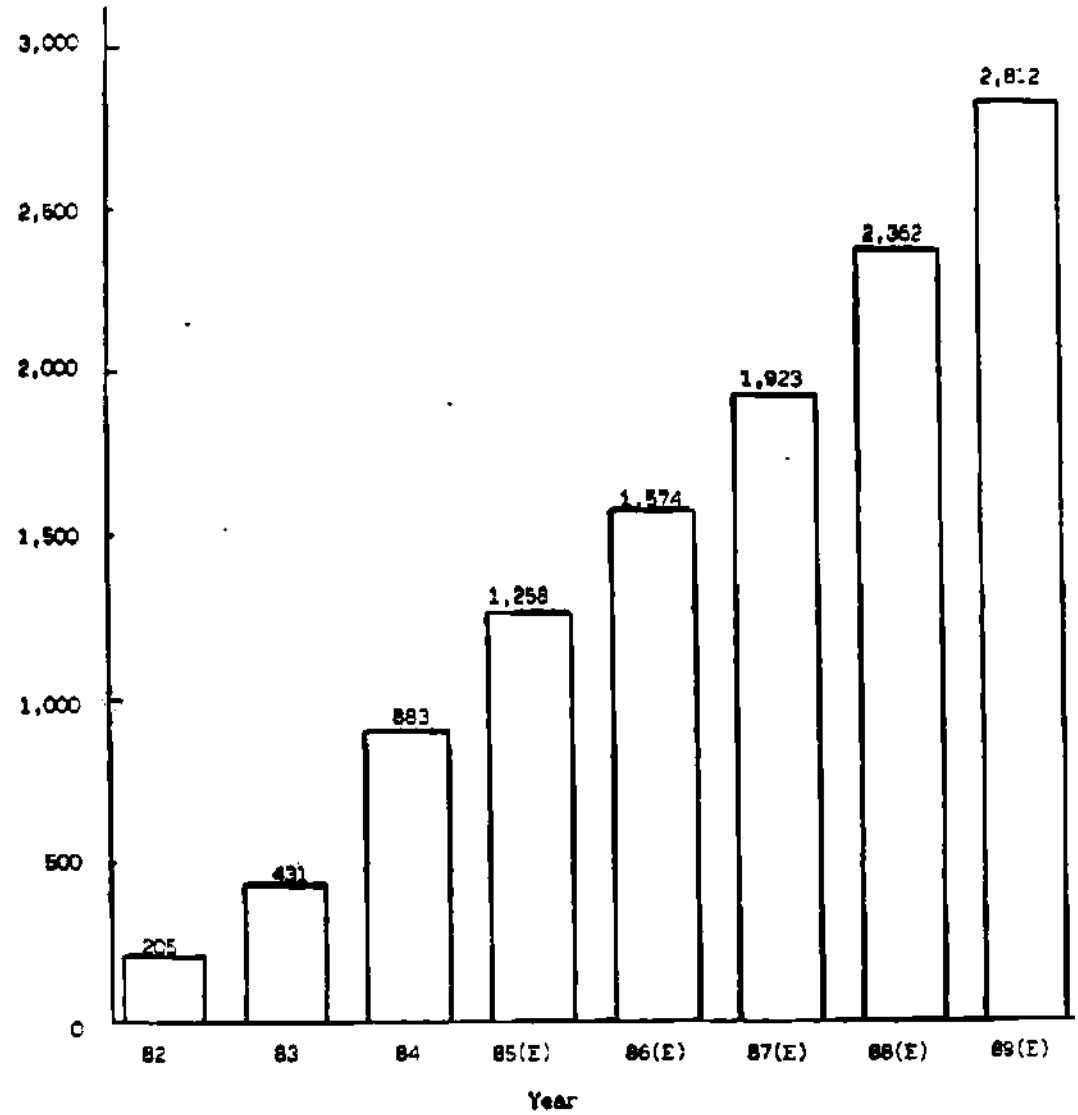
(Fig. 3) Application of CMOS Gate Arrays by Sector in Japan
(1984)



(Source: Yano Keizai)

(Fig. 4) Growth of Japanese Gate Array Shipment

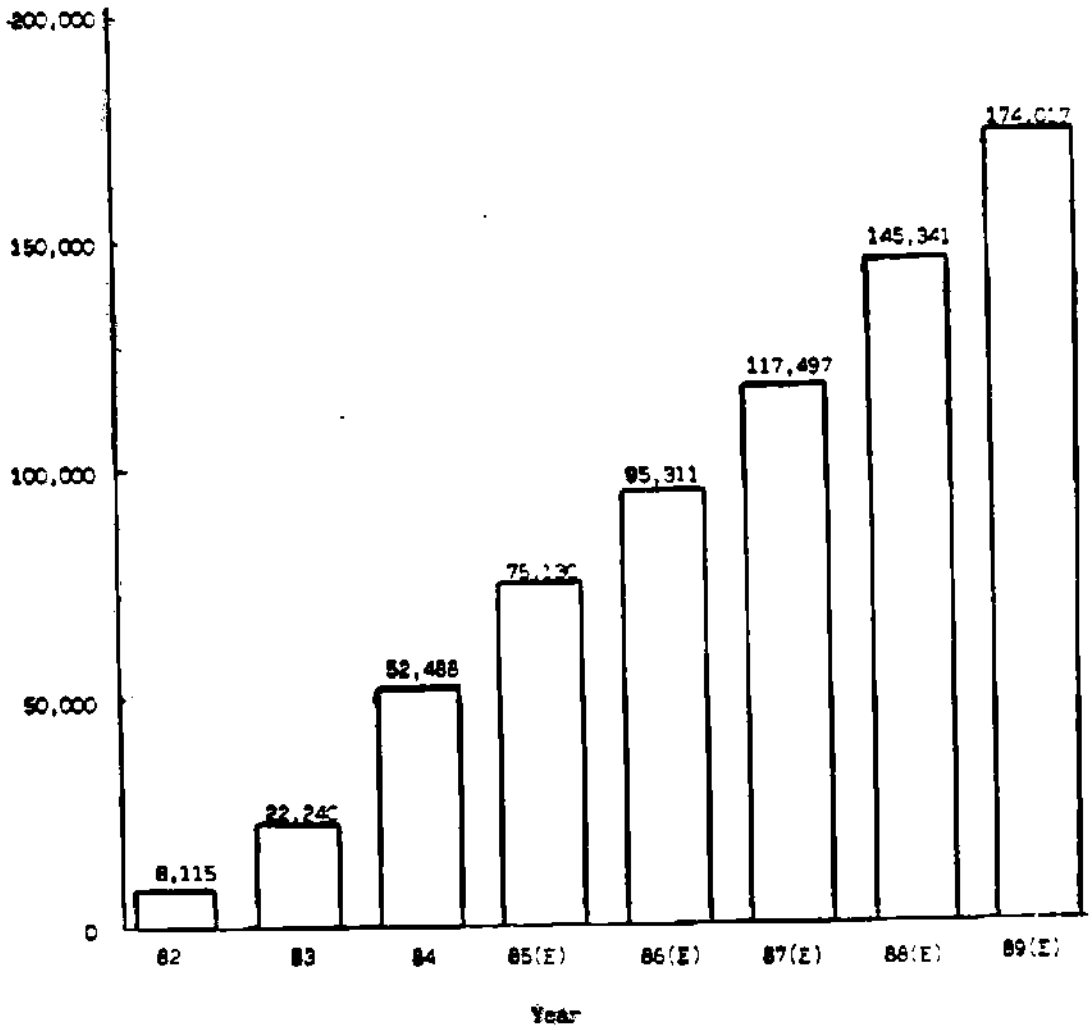
(in 100 Million yen)



(Source: Yano Keizai)

(Fig. 5) Growth of Japanese CMOS Gate Array Shipment

(in Million yen)



(Surce: Yano Keizai)

Nielsen Dataquest

MERCHANT CAPTIVES

James H. Van Tassel
Vice President, Microelectronics Division
NCR Corporation

Dr. Van Tassel is Vice President of the Microelectronics Division at NCR Corporation and is responsible for the development and manufacture of semiconductors. He is co-holder of the patent for hand-held calculators with two former colleagues at Texas Instruments, having joined that corporation in 1960. While at TI, Dr. Van Tassel also served as Process Control Manager for Semiconductor Operations, Technical Director of TI-Europe, and General Manager of MOS Logic and of the TMS 1000 microprocessor organizations. Dr. Van Tassel holds a B.S. degree from the University of Wisconsin-La Crosse, an M.S. degree and a Ph.D. in Chemistry from Texas Tech University, and he has completed postdoctorate work in Chemistry at Princeton University.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
October 14, 15, and 16, 1985
Tucson, Arizona

From Captive to Merchant Supplier

Dr. James H. Van Tassel
Vice President, Microelectronics Division
NCR Corporation

Introduction:

Thank you. I have been asked to discuss our transformation from a classical captive supplier of semiconductor circuits to a large computer company to a full fledged semiconductor company with a broad customer base. To better describe this change, I need to tell you a little bit about NCR to put this move into perspective.

You all know NCR (Figure 2). NCR is a 101 year old manufacturer of business machines and computers. Our early success in the retail and banking fields with complex mechanical machines still pervades the public perception of NCR, but we also were very early in the electronics point-of-sale terminal market and delivered one of the first fully transistorized computers (Figure 3), the 304, in 1959 to the Marine Corps for payroll calculations.

History of Semiconductors at NCR

Semiconductor development was started in the basement of an R&D building in Dayton, Ohio in 1966 (Figure 4). For the first two years the yield was zero. NCR was working on MOS. The choice of MOS at that time was based on projections of circuit density that would allow a small stand-alone counter-top machine. Counter space was a key factor in the markets in which NCR was then a major factor. In 1967, NCR concluded a license with G.I. covering MOS technology know-how, the first of a series of strategic technology relationships, and by 1971 had introduced its first counter-top retail terminal, the 280 (Figure 5). It was built with MOS devices in an NCR plant in Miamisburg, Ohio. More than 500 unique logic circuits were developed in the 4-phase PMOS design methodology. This design technology used an extensive cell library, structured placement, and high level descriptors which were easily used by system engineers to design MOS integrated circuits. If you think back to 1971, you will remember that the first MOS hand calculator had just begun to appear. Mostek was two years old and Intel had just started. So NCR was very early in MOS (Figure 4 repeat).

A prime feature of early cash registers was the retention of totals of transactions made. Originally sold as a method of keeping bartenders honest, this feature had to be incorporated in future machines. Early line powered MOS terminals were equipped with wet battery back-up systems to prevent loss of this information during power outages. Customer and service problems

were strong motivators to develop a solid state solution for data retention and in 1973 NCR was awarded basic patents on cells for non-volatile memories. Both NVRAMs and E^2PROMs were used in equipment designs in the last half of the 70's.

Manufacturing capability was expanded with a second plant established in Colorado Springs in 1975, the second at Silicon Mountain. By 1978, NCR had designed a family of products based on an 8080, 8-bit microprocessors with expanded I/O capabilities. It was instruction set compatible with the Intel 8080 but required its own set of dedicated non-volatile memories and peripherals. There was heavy management pressure to use this device family in systems designs.

Capacity was expanded again in 1979 at Fort Collins, Colorado, with the plant technical charter to develop CMOS processes and products for NCR's use.

NCR was a typical vertically integrated company (Figure 6). Chips were designed for a specific application. As an example, I have used our 32-bit chip set and the 9300 computer. This program was defined before our entry into the merchant market and there have been many other programs I might have used. The processor was combined with the appropriate terminals, operating system and application software as a product offering to be sold by an NCR salesman, a classic example of the total solution sale approach. The cost of the development, the process, the chip, the hardware and software was planned to be amortized only over the volume of a single product.

This example illustrates a prime reason for having a captive semiconductor operation: early access to technology (Figure 7). The chip design was started in 1979 using transistor models based on a process that was projected to exist in late 1981 or early 1982.

NCR was able to deliver the first 32-bit microprocessor based mainframe significantly before competitive offerings and thus gain a market advantage (Figure 8).

In addition to advantages in competitive position, control and security of supply and intellectual assets were prime reasons for NCR's captive efforts and I am sure that each of you who is managing a captive operation has made this same presentation.

The technology base of a captive semiconductor is targeted to the needs of the total company. Much of it is internally developed either with company or government funding and augmented through strategic alliances with merchant market suppliers (Figure 9). I have already mentioned our early G.I. relationship. In the mid-70's we had technical agreements with Mostek which allowed us to manufacture some of our own memories and provided N-channel technology. More recently, we had an agreement with Motorola that also provided N-channel technology at the 16-bit processor

level. I was very pleased with the level of technology when I came to NCR. They had good solid processes, well documented and were producing very large die at very high yields. Captives in general have good technology. At the most recent Custom Integrated Circuits Conference, more than 30% of the papers presented came from companies that are generally considered to be captive.

At NCR, the Microelectronics Division was a member of the Development and Production Group (Figure 10). Other divisions in the group, such as the Retail Systems Division, used our products in equipment transferred at annually established manufacturing transfer prices to the Marketing groups which in turn sold to our end customers. Our products were transferred to the systems division at cost and we were measured on our ability to achieve year to year reductions in that cost in the order of 10% to 15%. In addition to cost reduction, we were measured on service indices that boiled down to a goal of average unit delinquency of four days or less at each month end. Our quality was monitored in our plants and in our receiving plants in conventional fashion. The only real difference between NCR and merchant suppliers was that we maintained traceability on everything and we were subject to a very short feedback loop for all problems (Figure 11).

Our plants were functionally organized with the normal responsibilities. Our R&D organizations were charged with process development to maintain NCR at or near the leading edge of technology, to design products defined by our systems plant users, and to propose and design new products for NCR use. We did far more of the first two than we did of the latter. System and application expertise resided in the systems plants.

Against this background (Figure 12), this ad appeared in the June 1981 trade press. Calls from friends in the industry focused on "What is NCR Up to Now?" This announcement had been preceded by a year of feverish work. Chuck Exley, then President and now Chairman of the Board and President, was determined to convert from a system of conventional vertical integration to a system of commercialized vertical integration (Figure 13). Each level on the pyramid of vertical integration could and was encouraged to compete in the open market with its products. If no one else will buy your products, why should NCR? Are they too expensive? Are they of current technology? Can someone else do it better or cheaper?

The Microelectronics Division was the pilot for this significant change. We have been followed into the market by computers such as the NCR Tower which is sold as a bare box or with an operating system to systems integrators or value-added resellers and also is integrated into larger NCR systems. Also, printers, which are the derivative of the ones on NCR point-of-sale equipment, power suppliers, and controller boards are now sold externally. While revenues from such sales are a small part of the total NCR

corporate revenue, it has had some profound effects on our thinking. It has quickly driven market awareness and competitive pressures into all levels of the integration pyramid.

In preparation to market entry, we first adopted a conventional semiconductor P&L accounting system and we valued our parts sold to NCR at market value. If similar parts could not be identified, prices were established on complexity, die size, and packaging. Our financial system and thinking were transformed to words like revenue, profit and loss, although we didn't use the word profit too often, and return on assets, instead of cost of product transferred and variances. Systems plants no longer were influenced to buy from us and life was one long series of "meet comp" situations.

Please don't think that these actions were taken in any but a positive fashion. They were not taken to shake out unprofitable elements of vertical integration. NCR is committed to semiconductors as the core technology for its businesses. It has funded it liberally from the beginning. It also recognizes the attractiveness of the semiconductor market as a growth and profit opportunity. Competition is healthy. We are a better internal supplier because we are successful outside. Management has adapted well to the fast moving I/C business.

As we prepared for market entry, we assessed our strengths and weaknesses (Figure 14). Our process technology was in good shape and we had committed to a new plant in Colorado Springs with advanced contamination control capabilities and a stepper production line.

We knew the meaning of the word commitment. You learn it quickly when your customer's boss is your boss.

Our quality systems satisfied a very demanding customer.

Most of all, we had worked in a spirit of partnership with our systems plants. Our people wanted to please the customer.

On the other hand, we were woefully weak in marketing and sales skills. We had never defined a product for a broad market. We took the word of our systems plants. Our sales experience was zero. No one had ever sold. The applications expertise for our products was in the user plants. It was not our job to be good at this. And, of course, we lacked credibility in the marketplace.

Our product portfolio was a real problem. I did not see how anyone but NCR would buy 95% of what we made. It had all been designed for a specific spot on a circuit board or had a bus structure that was non-standard. We did have some EEPROMs that could be converted to standard products, we were good at ROMs, and we had an internal standard cell program.

We evolved a set of product strategies (Figure 15) and assigned them to the plants for execution. I knew that we could make reliable E^2PROMs and we quickly came out with a fairly broad range of these products. We think that E^2 technology will make a valuable addition to our standard cell family in the near future.

NCR had used ROM programmable machines for a long time. When we went public, we had more than 1,100 active ROM codes for NCR and it positioned us well for the ROM boom of 1982 and 1983. We participated heavily in the consumer ROM business. It provided us rapid growth and developed good manufacturing disciplines in cycle time and yield. While we rode the ROM market, we developed our standard cell program.

Our early PMOS designs had been done in standard cell format and a program had been initiated in 1979 to find a way to convert system designs from package level designs to silicon designs. Our first internal programs had virtually no CAD support and were done with paste-ons and colored pencils. Our customers taught us a lesson and when we went to market in 1983, we had a very complete CAD system. It appears we are currently the leader in this high growth area. Someone termed us the "unsung" leader which reflects on our ability to merchandise.

We have a class of products we call VIPs, vertically integrated products where we have taken advantage of the application skills of our systems plants to cover one of our basic weaknesses in product definition. The NCR/32 32-bit microprocessor and our family of circuits that support the Small Computer Systems Interface are examples of this. While the 32-bit set has not been as successful as we would like, we have still shipped more full-up at speed 32-bit processors than any company in the industry. The NCR Wichita plant was active on the ANSI committee that developed the SCSI standard and as the standard was being developed, they did the first chip designs using our cell-based design system. Our SCSI set is now approaching 200 design wins. AMD and Western Digital second source members of this family.

We have tried to maintain our entrepreneurial atmosphere where good ideas can emerge as products. An example of this is our geometric array parallel processor we call the GAPP, which is the first systolic processor on the market. We received an IR-100 award for it last month along with Martin-Marietta, our development partner. Innovative products such as this migrate from our Advanced Development organization to product development and then into a business unit for commercialization. Advanced Development is chartered to focus on developments that have potential for commercialization within a four-year timeframe. The people move with the product through this organizational progression to broaden their perspective and enhance the "ownership" of product success spirit.

We also provide foundry and custom-owned tooling services to a variety of markets.

Our conventional plant organizations were not satisfactory for the open market (Figure 16). We added a marketing function and assigned product strategy responsibility to the R&D organization. As this has matured, we have broken the plants into business units with marketing and product development in each unit for better coupling to the market.

During the last five years, we have transitioned from an organization whose primary focus was inward looking to one which is basically outward looking (Figure 17). As a captive, we were primarily concerned with manufacturing processes and design and now we are more concerned with our customers and competition.

While the manufacturing process and its efficient operation remains a competitive requirement, our management thinking has shifted from a total focus on this as a captive to an intermediate phase of product orientation to a market/customer phase as we mature in our market understanding. In the intermediate phase we have been product oriented with concerns for specific markets and their characteristics. What are the strengths and weaknesses of our products and how can they be sold are the kinds of questions that attracted management attention.

Product managers at mid-organizational levels are now given discretion over R&D spending to force a balance between leading edge designs, time to market, and profitability goals.

In the maturing phase of our commercialization, the focus on market and customer is becoming primary. We are gaining an understanding of our customers' industries, their product strategies, and new applications so we can be effectively positioned to intersect them in the future. The understanding we have of NCR is being supplemented by an increasing understanding of our commercial customers. Our investment in marketing has continued to increase and decisions on pricing philosophies and competitive dynamics are occupying more and more of management's attention.

Not all of our managers have been able to make this transition at the same speed and achievement of this evolution has been hastened by a liberal sprinkling of marketing professionals hired from the semiconductor industry.

As we went outside, we formed a network of manufacturing representatives reporting at the Division level, we wrote data sheets, terms and conditions, set up customer service, credit and collection procedures and all the other things a start-up semiconductor company has to do. And on my first sales call ran into, "Hey, I though you guys were in the cash register business" and "you're just selling off excess capacity because your internal requirements are down."

We have come a long way since then. Our strategy of entering the ROM market for quick growth took us to the number three or four supplier spot for 64K ROMs in 1983. Our long term focus on the applications specific market resulted in being credited as being the leader in standard cells in 1984 (Figure 18).

We have gone from a 100% internal supplier in 1980 to one with about 25% of its products consumed by its parent. I imagine we are now about as captive as Texas Instruments, although numbers on this are not publicly available.

One of the substantial changes that has occurred is that we treat NCR like a real customer. We have a sales force, application engineers, and a design center all dedicated to the penetration of NCR.

In the market we have done reasonably well (Figure 19). I have modified a plot from the Integrated Circuit Engineer "Status 85" to compare our revenue with that of other start-ups, only the numbers have been removed to protect the innocent. I have only included our non-NCR revenue in this plot. Perhaps this is not a fair comparison. After all, we were a start-up with ten years internal experience before we went outside.

Our profit performance has not been as good as I would have liked during the start-up time; however, we were able to get into the black the 4th quarter of last year. Contrary to other start-ups, our R&D bill was there in total the day we started as we assumed responsibility for Corporation-funded programs.

NCR is our largest, oldest, and best customer. We are now a better supplier to NCR because we have tested and honed our skills in the open market. We have established significant business relations with a wide variety of customers. I think we are looked on as a valued supplier. We are building a reputation as a solid supplier.

Should others follow this route? Some are trying. AT&T, Honeywell, and DEC have sold a few chips and there are rumors of more. These and many others have the technology skills to do it.

(Figure 20.) Just a word of advice. There are only two key ingredients for success.

1. An in-depth commitment at all levels of management to participation in the growth of the semiconductor market, and

2. An in-depth understanding of the market and what makes it operate.

It is not hard for management to believe in the growth potential of the semiconductor market. Having a good captive facility makes participation in this market an easy means of leveraging investments in R&D and facilities. Going public is tempting.

But you must not forget that going public means giving up one of the prime reasons for having a captive - Control. Now there are many customers and the true meaning of the word commitment can become more difficult to live up to. I have been told to keep every commitment I make, in the order that they are made. I am proud of the integrity of NCR management what that statement implies and our organization practices this at all levels. You can't go half-way public.

Technology, impressive facilities, and transistors per chip do not a successful semiconductor company make. Marketing understanding, resident in good people, is the ultimate determiner of success.

NCR

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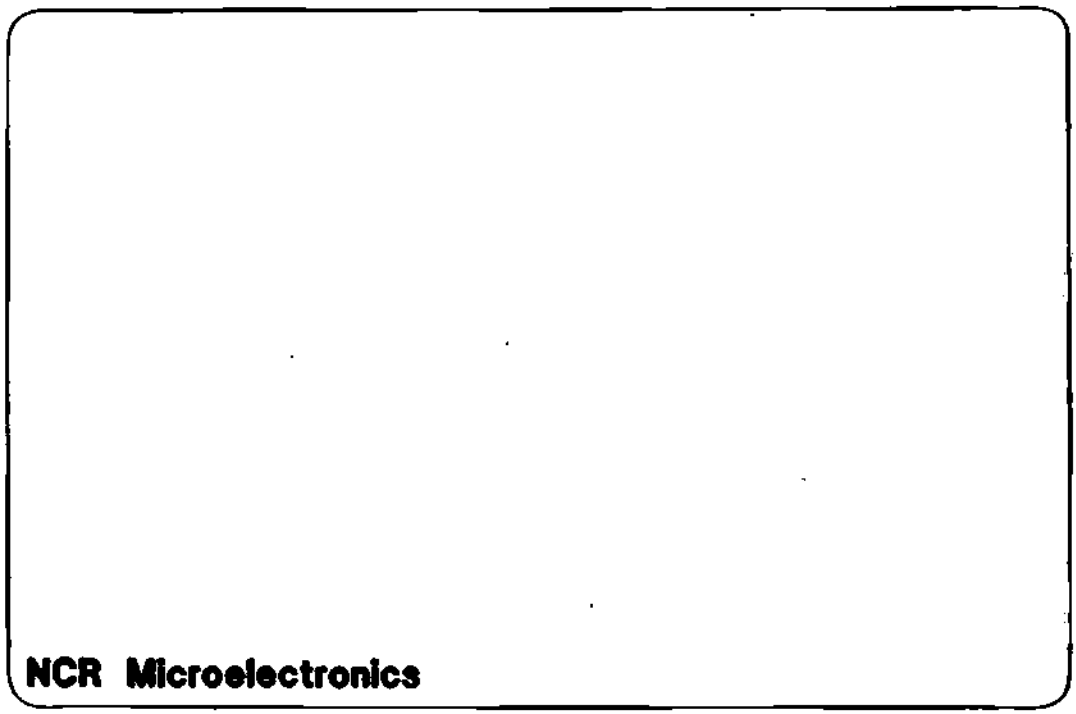

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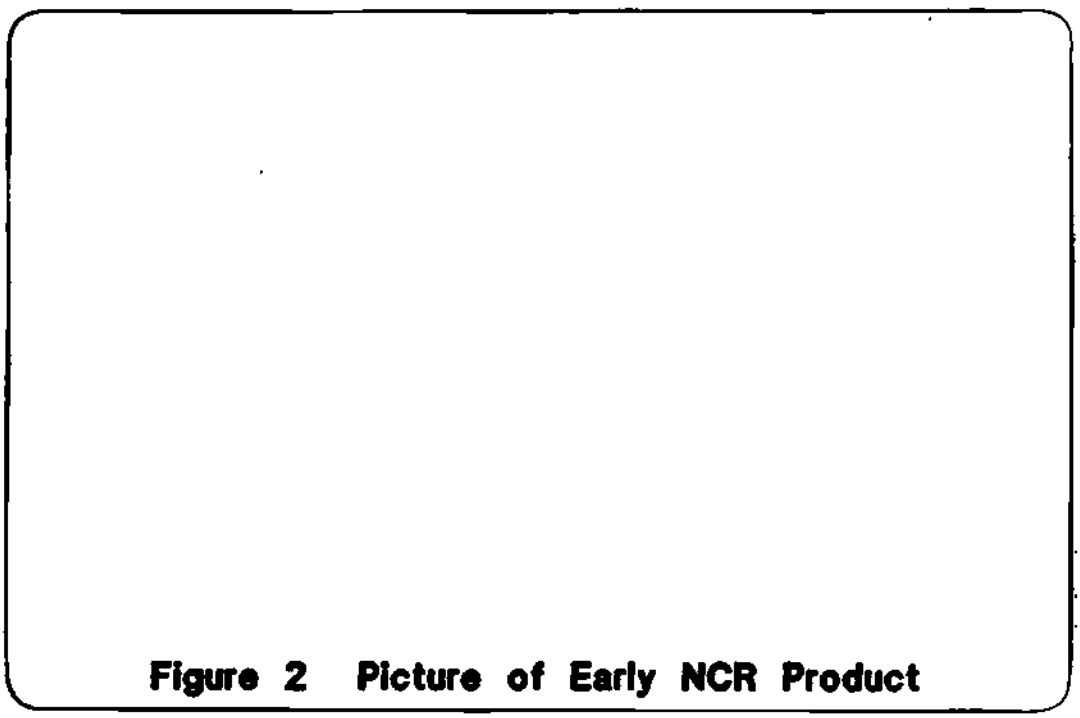

Figure 2 Picture of Early NCR Product

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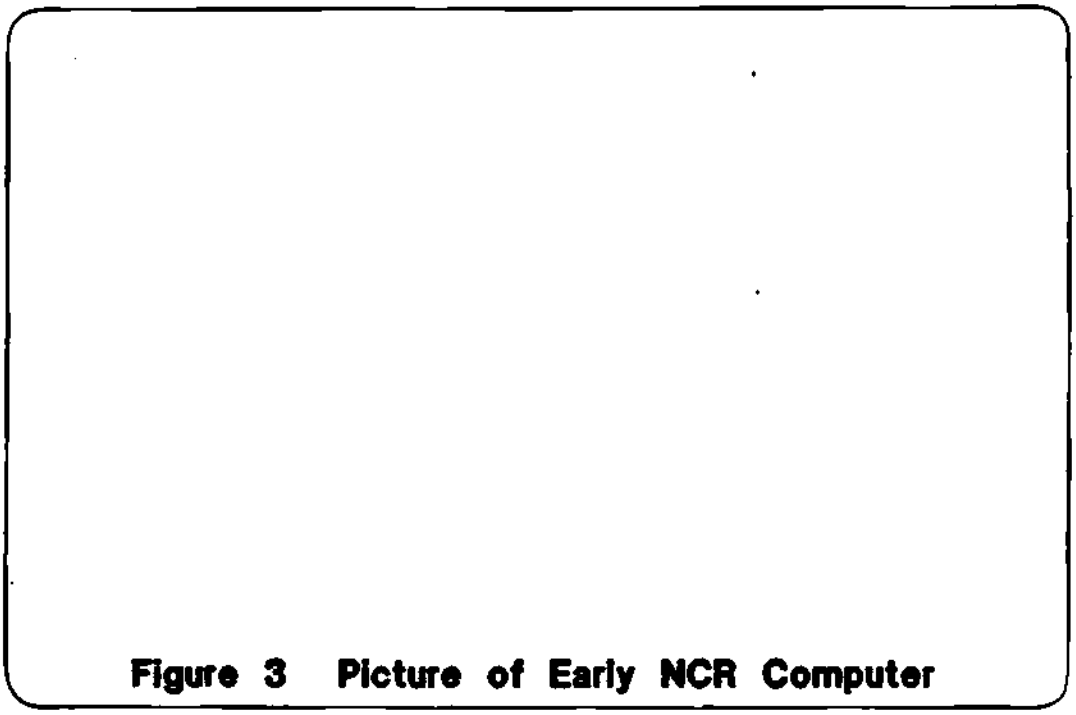

Figure 3 Picture of Early NCR Computer

SERVICE QUALITY SUPPORT

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History of Semiconductors at NCR

1966	**First Research and Development Programs**
1967	**MOS Technology Licensed from General Instruments**
1971	**First Countertop Terminal Shipped**
	Miamisburg, Ohio Factory Opened
1974	**First Non-Volatile Memories Manufactured**
1975	**Colorado Springs, Colorado Factory Opened**
1977	**Proprietary 8-Bit Processor Family Introduced**
1979	**Fort Collins, Colorado Factory Opened**
1981	**Entry into Merchant Market Announced**

SERVICE QUALITY SUPPORT

FIGURE 4

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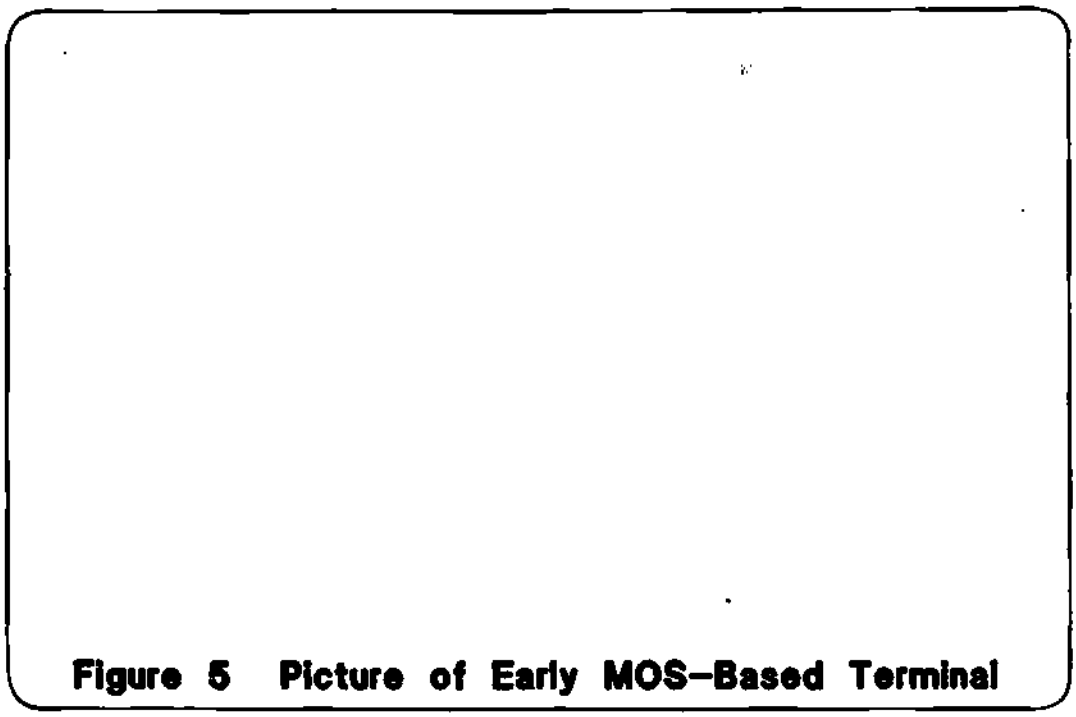

Figure 5 Picture of Early MOS-Based Terminal

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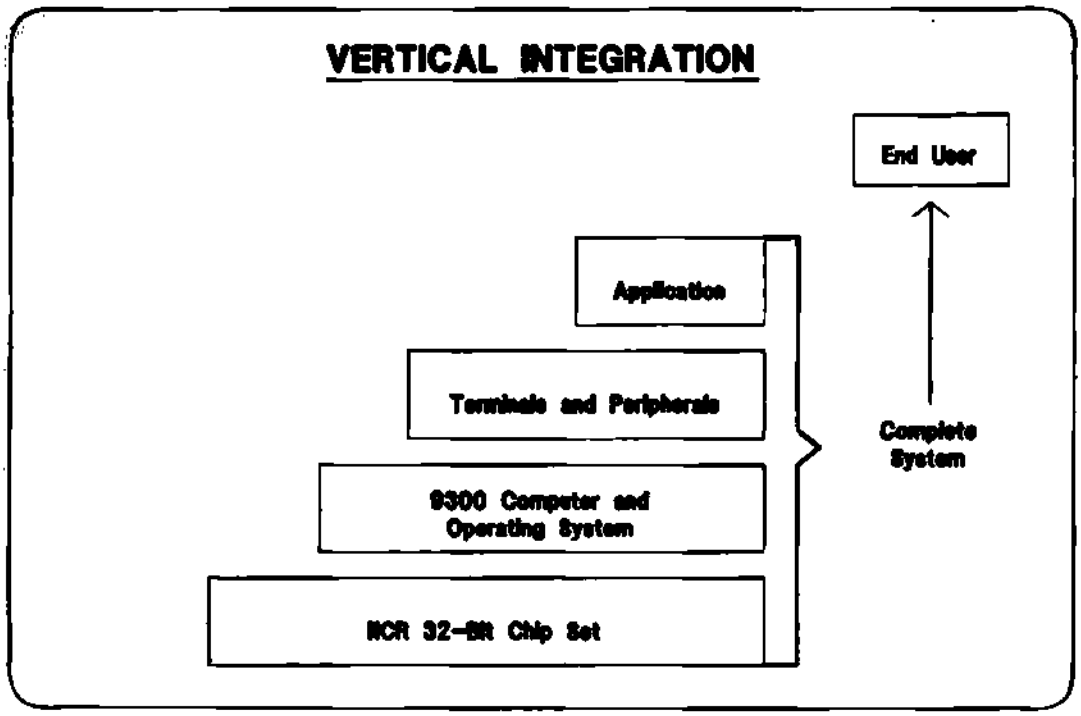

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FIGURE 6

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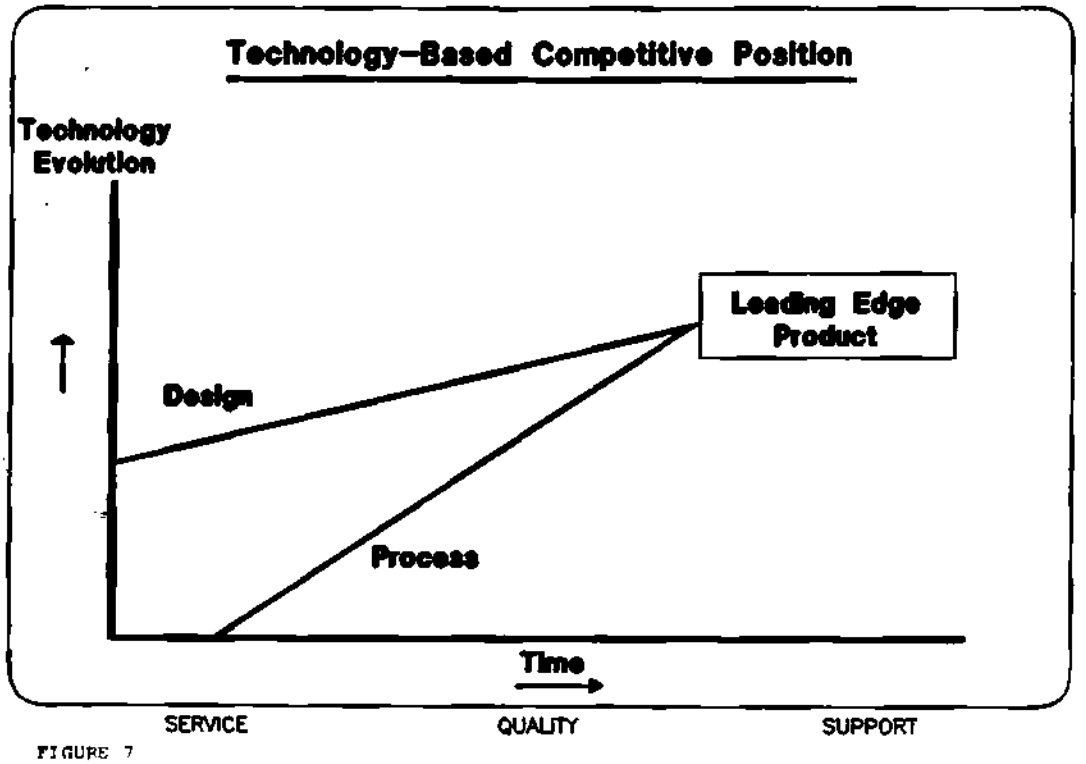

FIGURE 7

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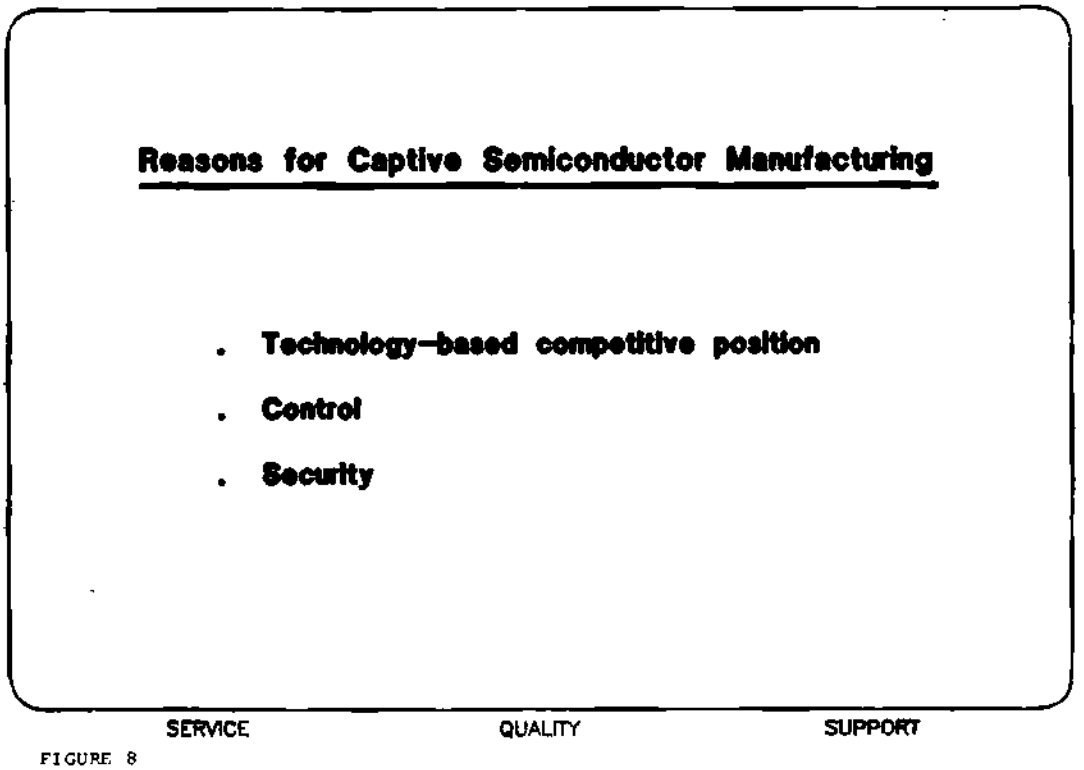

FIGURE 8

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Strategic Technology Alliances

- Late 1960's General Instruments
  P-MOS Technology
- Mid-1970's MOSTEK
  N-MOS Technology
- Early 1980's Motorola
  N-MOS Technology

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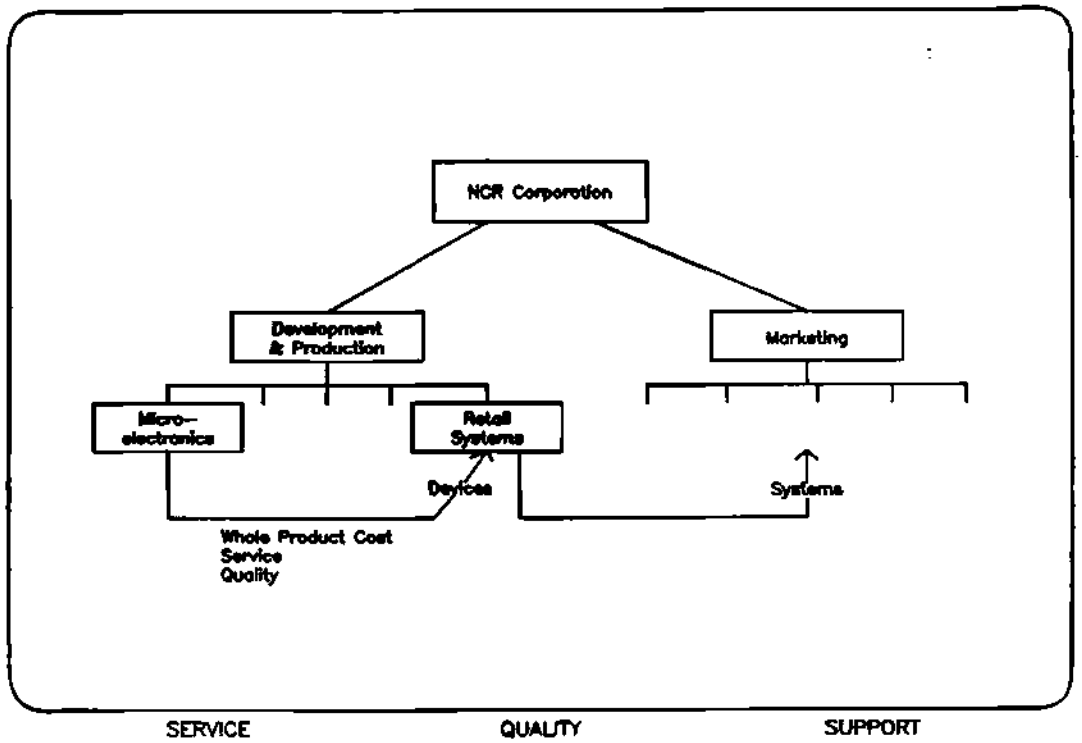

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FIGURE 10

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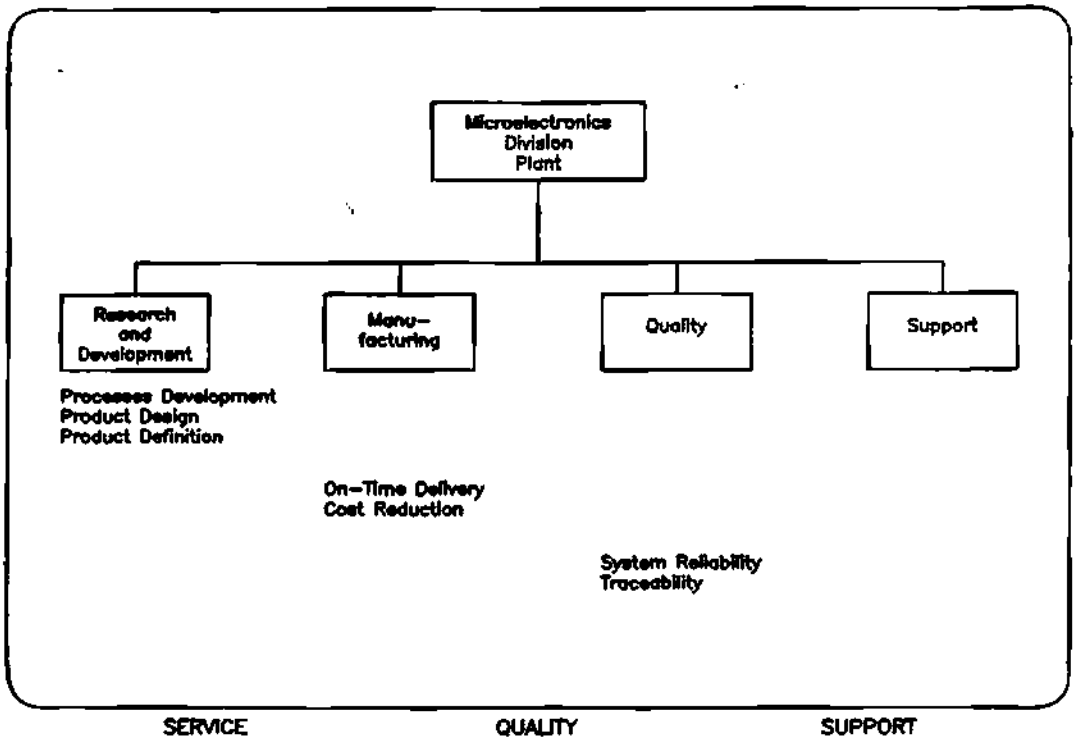

FIGURE 11

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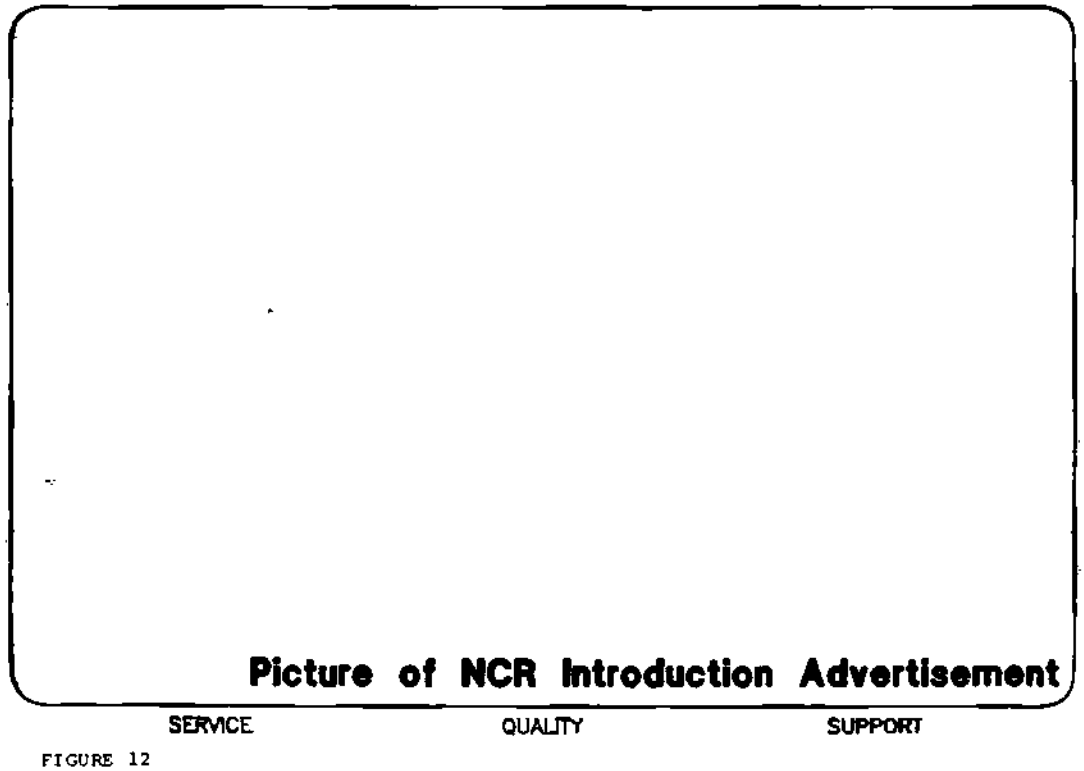

FIGURE 12

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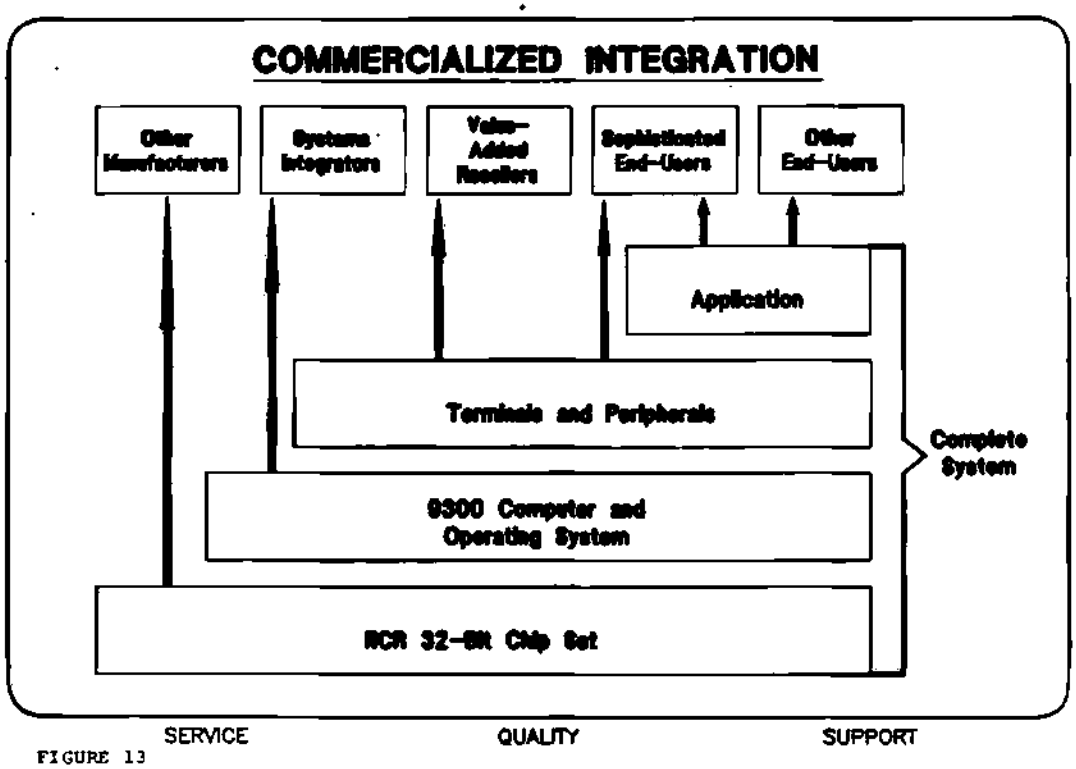

FIGURE 13

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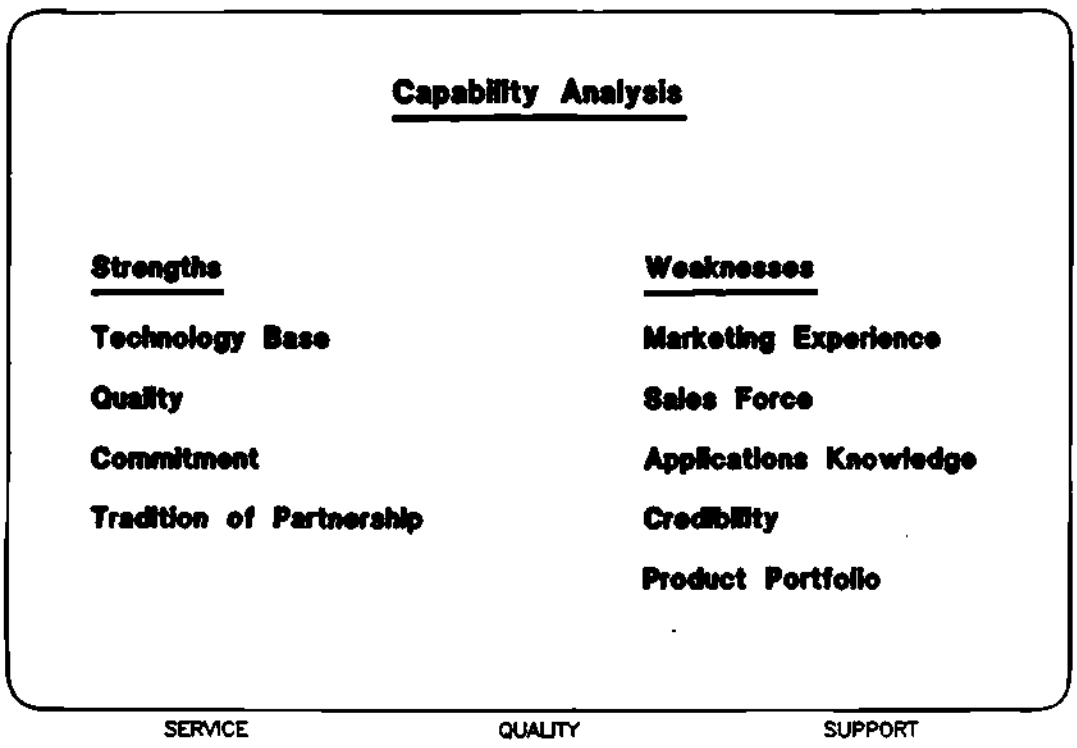

FIGURE 14

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Product Strategies

EEPROM's to capitalize on existing technology

ROM's for quick growth

ASIC standard cells

Vertically Integrated Logic Products

Entrepreneurial products

Foundry services for asset utilization

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FIGURE 15

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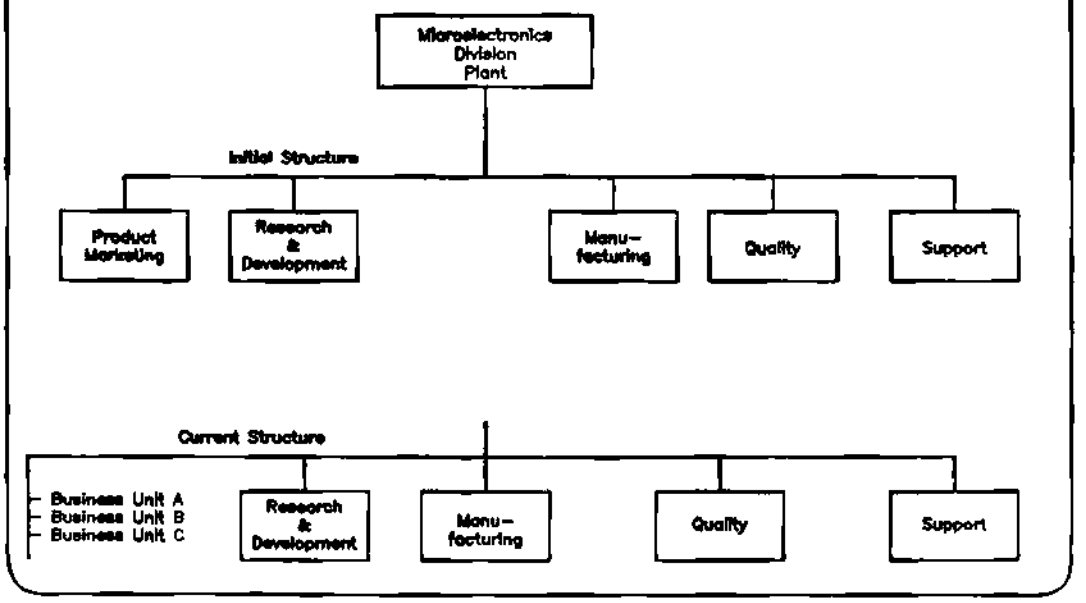
Organizational Evolution



SERVICE QUALITY SUPPORT

FIGURE 16

NCR
MICROELECTRONICS DIVISION

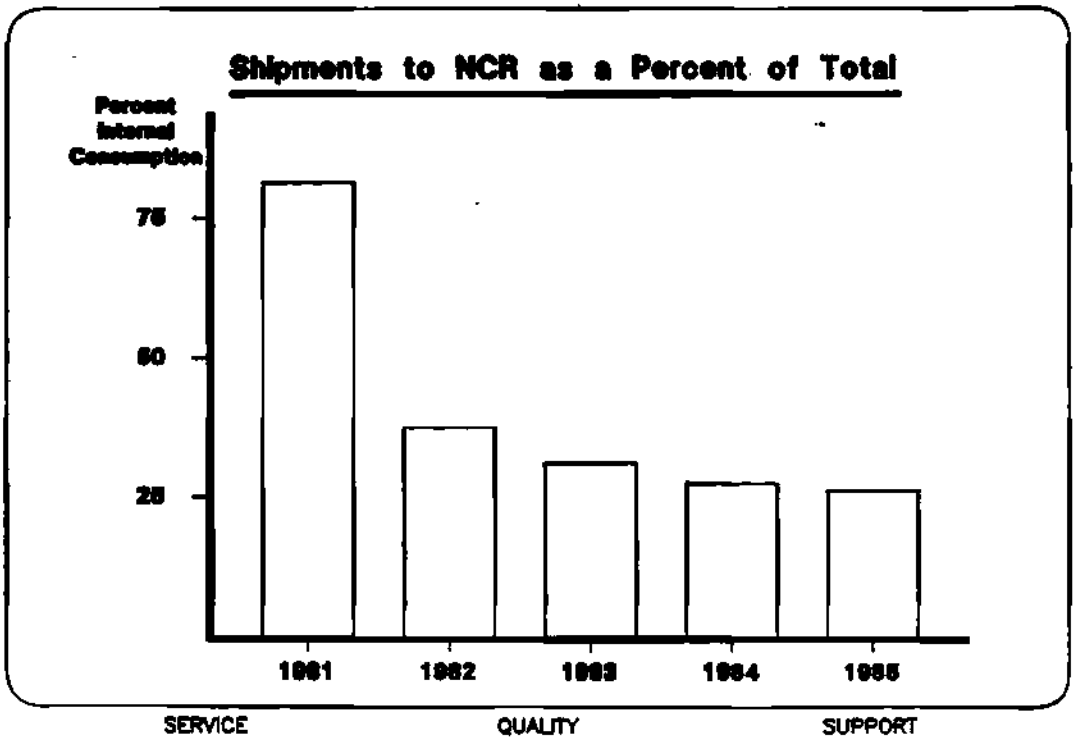


FIGURE 18

NCR
MICROELECTRONICS DIVISION

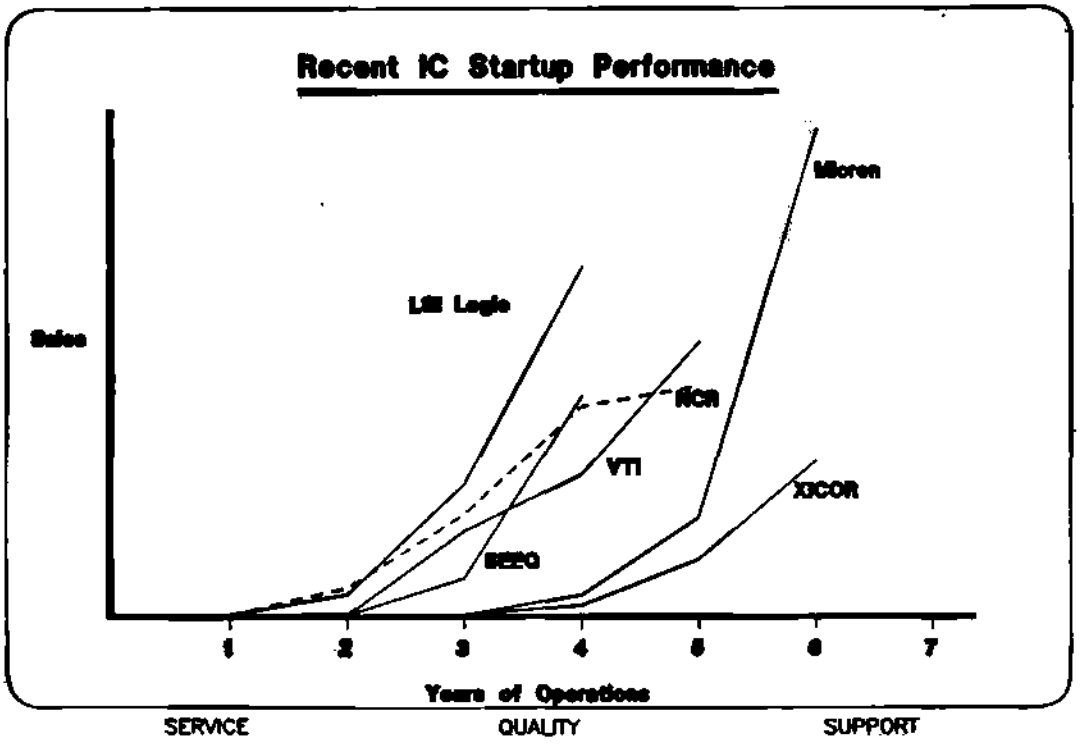


FIGURE 19

NCR

MICROELECTRONICS DIVISION

Success Factors for Market Entry

Strong management commitment to the semiconductor market.

Market understanding.

SERVICE QUALITY SUPPORT

FIGURE 20

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THINK TANK AND SILICON CRANK: PARTNERS IN INNOVATION

Arthur J. Collmeyer
President
Weitek Corporation

Dr. Collmeyer joined Weitek Corporation in 1981 as its first president. Previously, he was Vice President of R&D at Calma Company, and later served as Vice President/General Manager of Calma's Microelectronics Division. Prior to that time, he was employed at Xerox Corporation and Motorola Inc. Dr. Collmeyer received B.S. and M.S. degrees in Electrical Engineering from the University of Illinois and a Ph.D. in Electrical Engineering from Southern Methodist University.

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October 14, 15, and 16, 1985
Tucson, Arizona

THINK TANK AND SILICON CRANK
PARTNERS IN INNOVATION

Arthur J. Collmeyer
President
Weitek Corporation

The midpoint of the 80's finds the semiconductor industry in the midst of the VLSI epoch - an epoch which has redefined the markets for semiconductor products, as well as the structure of the semiconductor industry. The dichotomous influence of VLSI, enabling value-based application-specific products, as well as the new generation of cost-based products, has dramatically extended the base of innovation in the semiconductor industry. With VLSI, the impact of product innovation has equaled, if not surpassed, that of process innovation, with significant contributions coming from the user community. Expanded product opportunities, coupled with the escalating costs of capacity, has led to a new perspective on the structure of the industry: The THINK TANK SILICON CRANK perspective.

While opinions vary as to emphasis and degree, most of us agree that a balanced product portfolio, including cost-based and value-based products, is ideal. In 1985, the business environment has been particularly harsh on those merchant manufacturers with minimal portfolios of value-based products - the SILICON CRANKS. Relief from this imbalance is not easy to come by. Innovative product strategies are difficult to execute, demanding rare combinations of system and circuit design expertise, and - above all - a closeness to the customer, which few semiconductor companies enjoy. The risks can be spread and the benefits multiplied to the extent THINK TANKS, SILICON CRANKS and those who would be a bit of both can cooperate to proliferate value-based products. The growth of value-based products has been, and will continue to be, a stimulant to consumption of cost-based products.

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COST DRIVEN--CUSTOMER DRIVEN

F. Joseph Van Poppelen
Vice President, Semiconductor Marketing
National Semiconductor Corporation

Mr. Van Poppelen is Vice President of Semiconductor Marketing at National Semiconductor Corporation. During his 25 years in the semiconductor industry, he has held various management positions, including Vice President and General Manager at Fairchild Semiconductor, President of ITT Semiconductor, and Vice President and General Manager of Signetics Corporation. Mr. Van Poppelen received a B.S. degree in Administrative Engineering from Cornell University.

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THIS PRESENTATION WAS NOT AVAILABLE AT PUBLICATION TIME.

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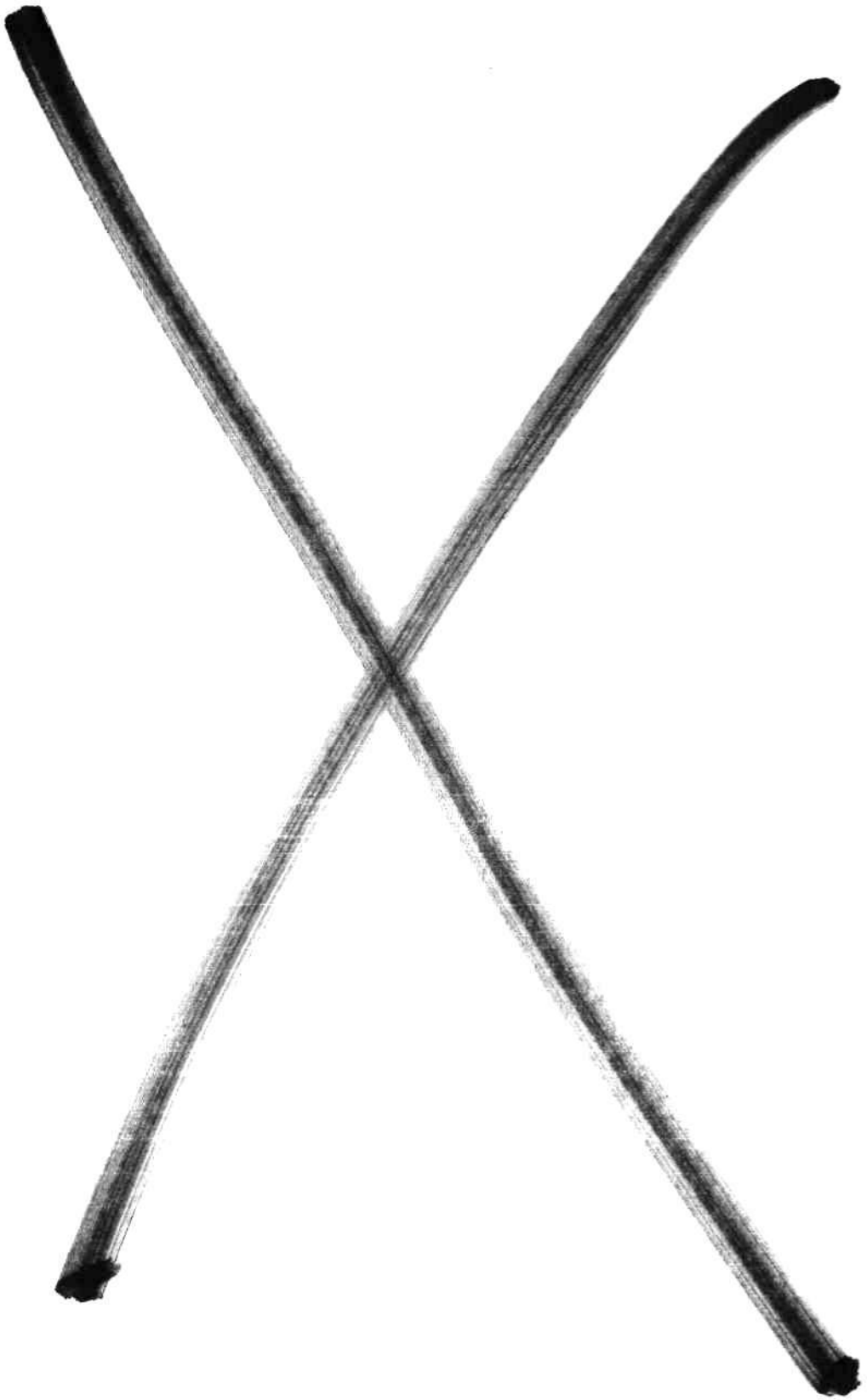
Tucson, Arizona



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X-RAY LITHOGRAPHY COMPETITIVE SUBMICRON PROCESSING IN THE 1980s

Carroll R. Fencil
Director, Government Lithography Programs
Perkin Elmer Corporation

Mr. Fencil is Director of Government Lithography Programs for Perkin Elmer Corporation. He is responsible for the acquisition and conduct of all Perkin Elmer government lithographic contracts, as well as related company development and new business activities. He has more than 25 years of experience in engineering and management of major electro-optical and electronic systems development programs for industrial and aerospace applications. In previous assignments at Perkin Elmer, Mr. Fencil managed laser technology development programs, electro-optical sensing systems, scientific instruments for NASA spaceborne use, and large land-based tracking systems. He was previously employed by Sikorsky Aircraft Corporation; where he was involved in the development of helicopter stabilization systems. Mr. Fencil received a B.S. degree in Electrical Engineering from Michigan State University and an M.S. degree in Control Systems from the University of Connecticut.

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Tucson, Arizona

X-RAY LITHOGRAPHY: COMPETITIVE SUBMICRON PROCESSING IN THE 1980'S

C.R. Fencil
Microlithography Division
Perkin-Elmer Corporation
Norwalk, Connecticut 06856

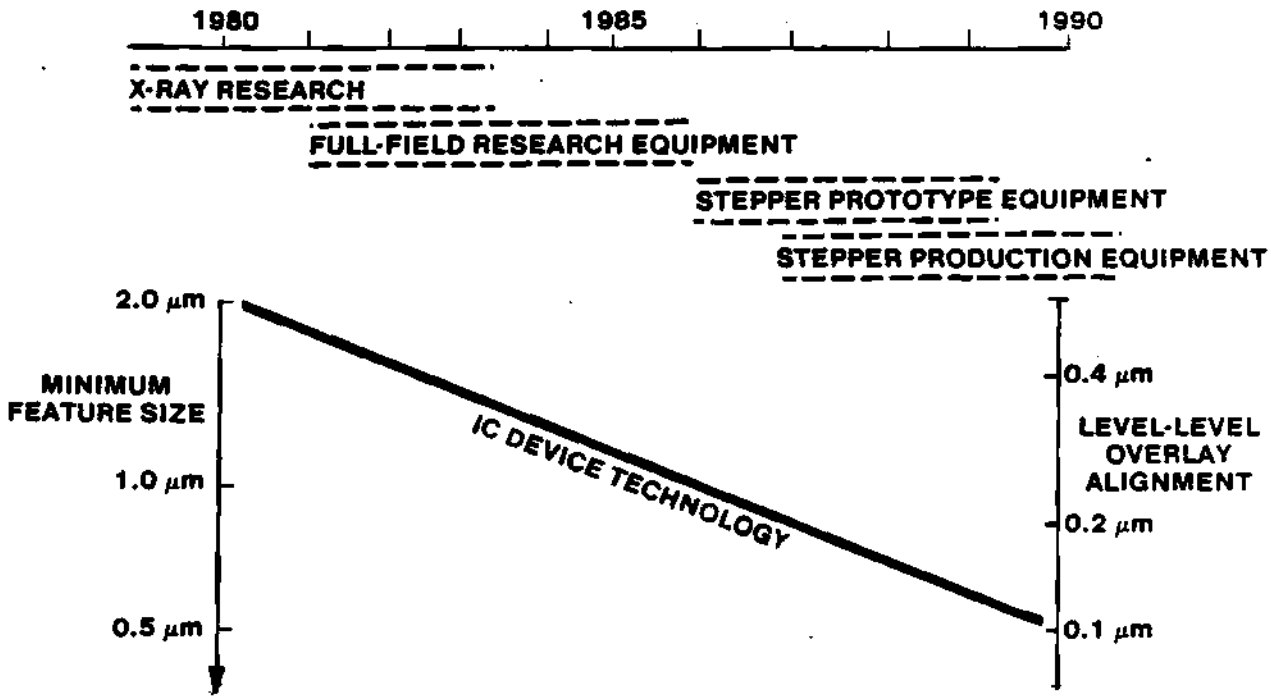
OVERVIEW

This slide presentation discusses X-ray lithographic technology, a competitive, submicron processing approach designed to meet the growing needs of the 1980's for high-density, high-performance integrated circuits. The advantages and capabilities of X-ray technology and the critical issues affecting it are described as well as current market trends. Supporting component technologies such as sources, masks, and resists are also addressed.

OUTLINE OF SLIDES

- o VLSI requirements vs. X-ray technology developments
- o Projected market for X-ray lithography
- o X-ray lithography technical approach and advantages
- o Critical technology issues (including masks and resists)
- o X-ray lithography current equipment status (Perkin-Elmer X-100 Full-Field System)
- o X-ray lithography future equipment status (Perkin-Elmer Step-and-Repeat System)

OUTLOOK FOR THE 1980's



CURRENT SUBMICRON PATTERNING STRATEGY (0.5 < MFS < 0.75 MICRON)

- PATTERN THREE TO FOUR CRITICAL LEVELS USING DIRECT WRITE E-BEAM LITHOGRAPHY
- PATTERN NON-CRITICAL LEVELS OPTICALLY
- EVALUATE X-RAY LITHOGRAPHY FOR HIGH-VOLUME PRODUCTION AS TOOLS AND SUPPORTING TECHNOLOGY BECOME AVAILABLE

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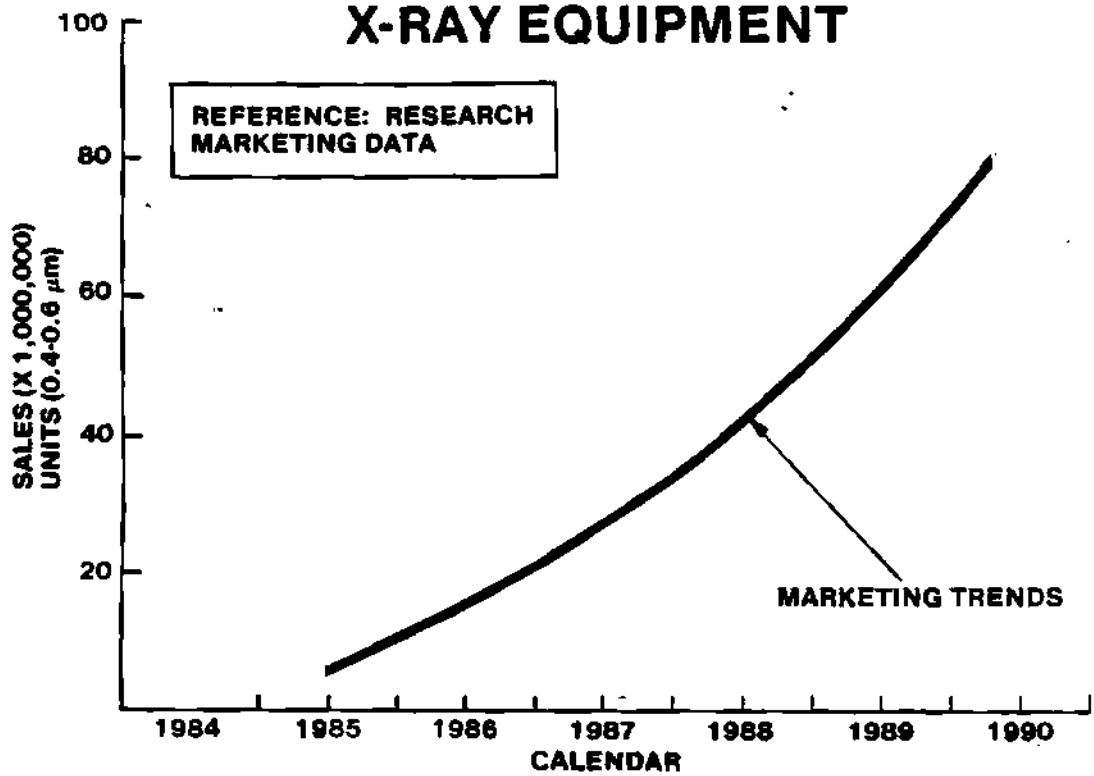
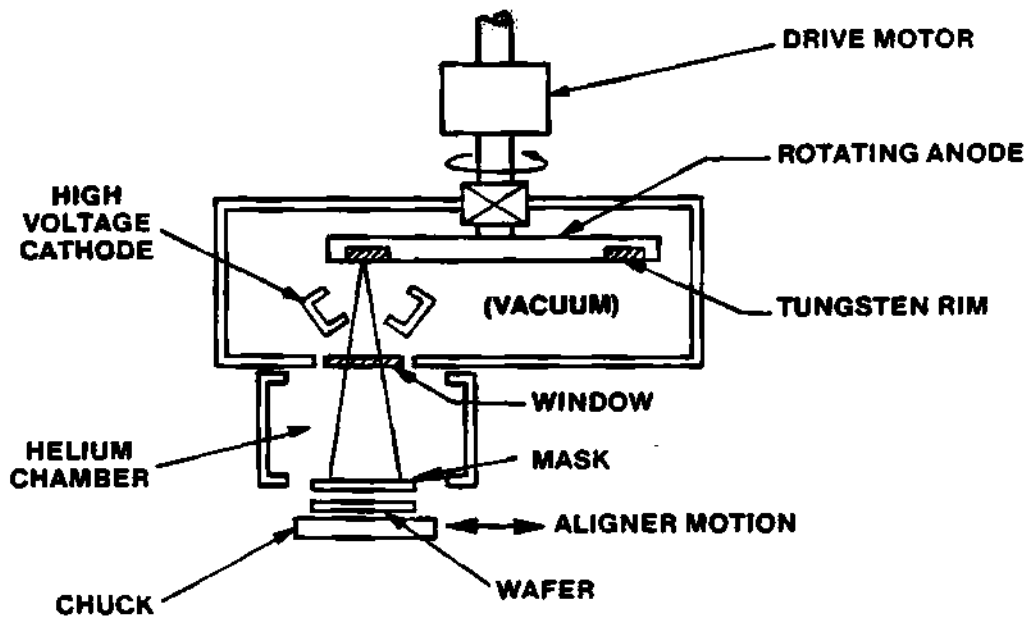
X-RAY EQUIPMENT



X-RAY LITHOGRAPHY PROXIMITY APPROACH



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ADVANTAGES OF X-RAY LITHOGRAPHY

- HIGH RESOLUTION
- COST EFFECTIVE SOLUTION

CRITICAL ISSUES

- X-RAY MASK TECHNOLOGY
- X-RAY RESISTS

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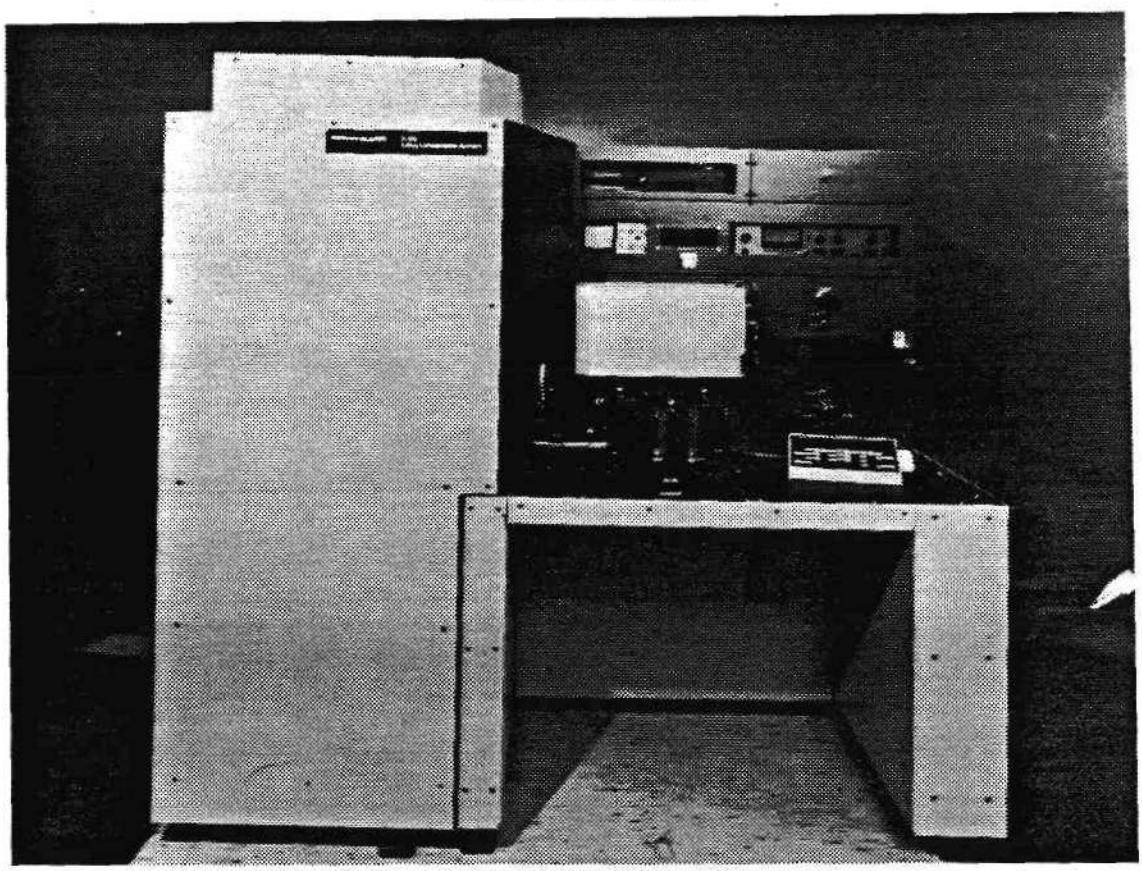
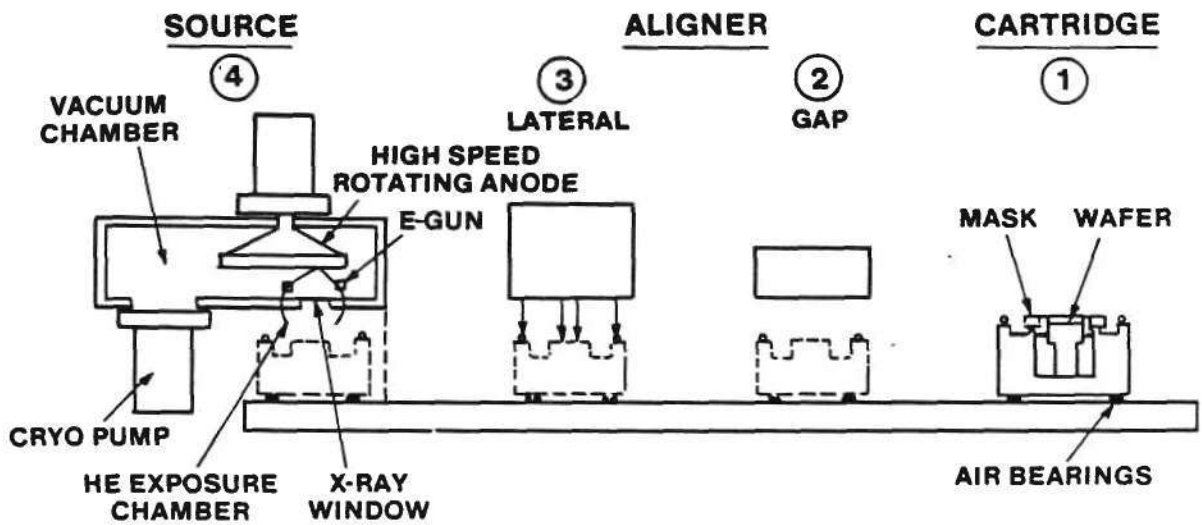
PERKIN-ELMER X-100 LITHOGRAPHY SYSTEM



X-100 CONCEPT



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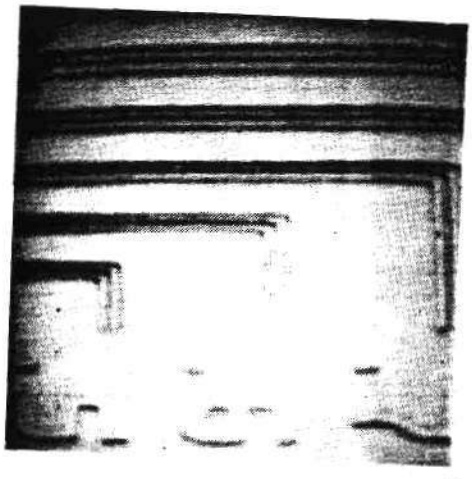
X-100 SPECIFICATIONS

RESOLUTION	**0.5 μm (50 μm PROXIMITY GAP)**
	0.25 μm (25 μm PROXIMITY GAP)
ALIGNMENT ACCURACY	**0.25 μm (2 SIGMA)**
THROUGHPUT	**14-32 (100 mm WAFERS/HR.)**
	19-35 (75 mm WAFERS/HR.)

X-100 LITHOGRAPHY



COURTESY INTEL MAGNETICS 0.5 μm PATTERNS

1.0 μm BUBBLE PATTERNS

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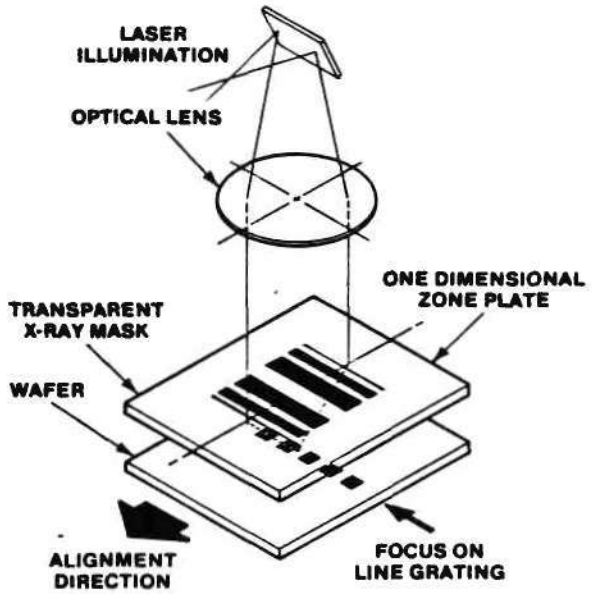
ZONE PLATE WITH LINEWIDTH GRATING ALIGNMENT CONCEPT

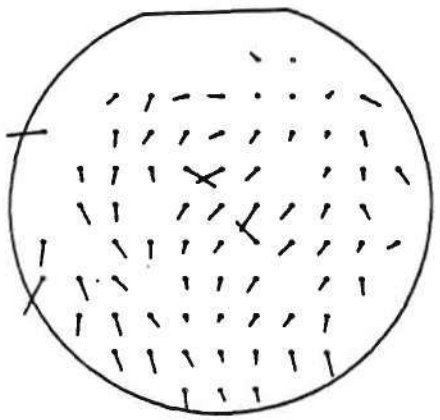


X-100 ALIGNMENT RESULTS

14-JUN-85 A4
18:25:21

FILENAME: DL2:RTST3814.FIX WAFER SIZE : 3 INCH MACHINE S/N 2

MEASURED



— 0.10 MICRONS

COEFFICIENTS — AS MEASURED

TX	:	-0.013	UM
TY	:	-0.000	UM
ROTATION	:	0.000	UM/CM
MAG	:	0.007	UM/CM
KEYSTONE X	:	0.000	UM/CM**2
KEYSTONE Y	:	0.004	UM/CM**2

STATISTICAL SYNOPSIS — OF PLOTTED DATA

TOTAL POINTS : 72

	MEAN	S.D.	MAX
X DIR	-0.010	0.047	0.177
Y DIR	-0.050	0.038	0.174
VECTOR	0.075	0.035	0.185

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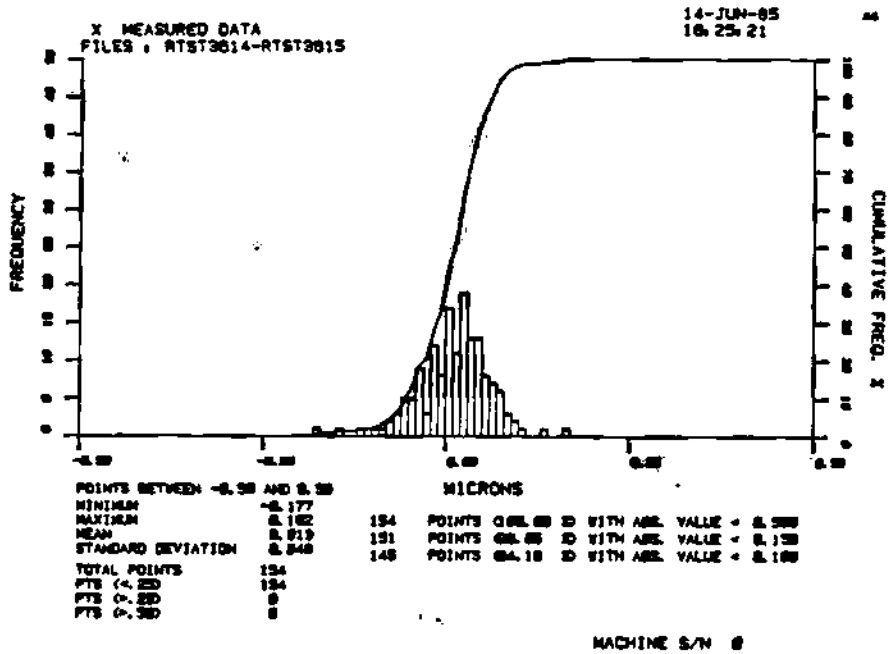
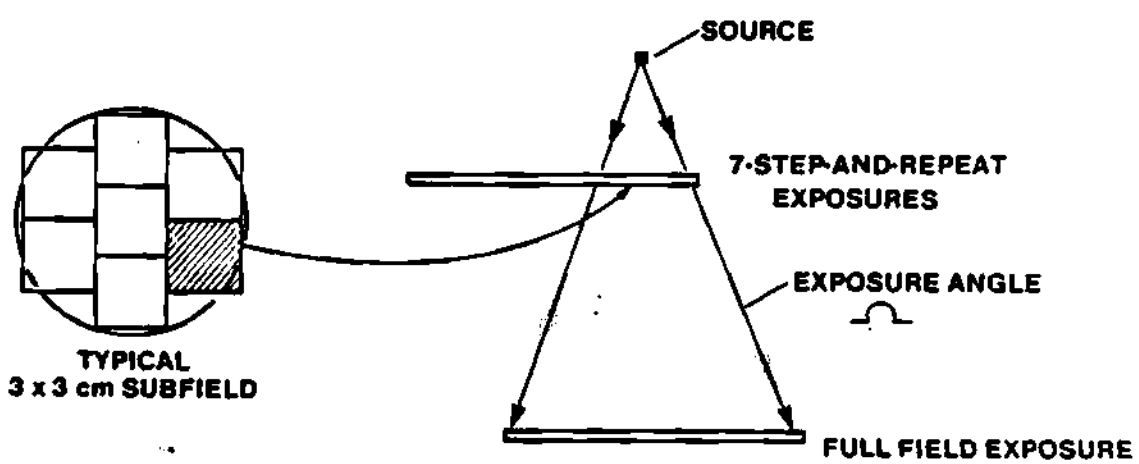
X-100 ALIGNMENT RESULTS



FULL FIELD VS. SUBFIELD EXPOSURES



- EXPOSURE TIMES AND THROUGHPUT IDENTICAL IF ALIGNMENT OVERHEAD NEGLECTED. (O/H > 100 WAFERS/HOURS)
- PROXIMITY GAP MUST BE REDUCED FOR EQUIVALENT RESOLUTION

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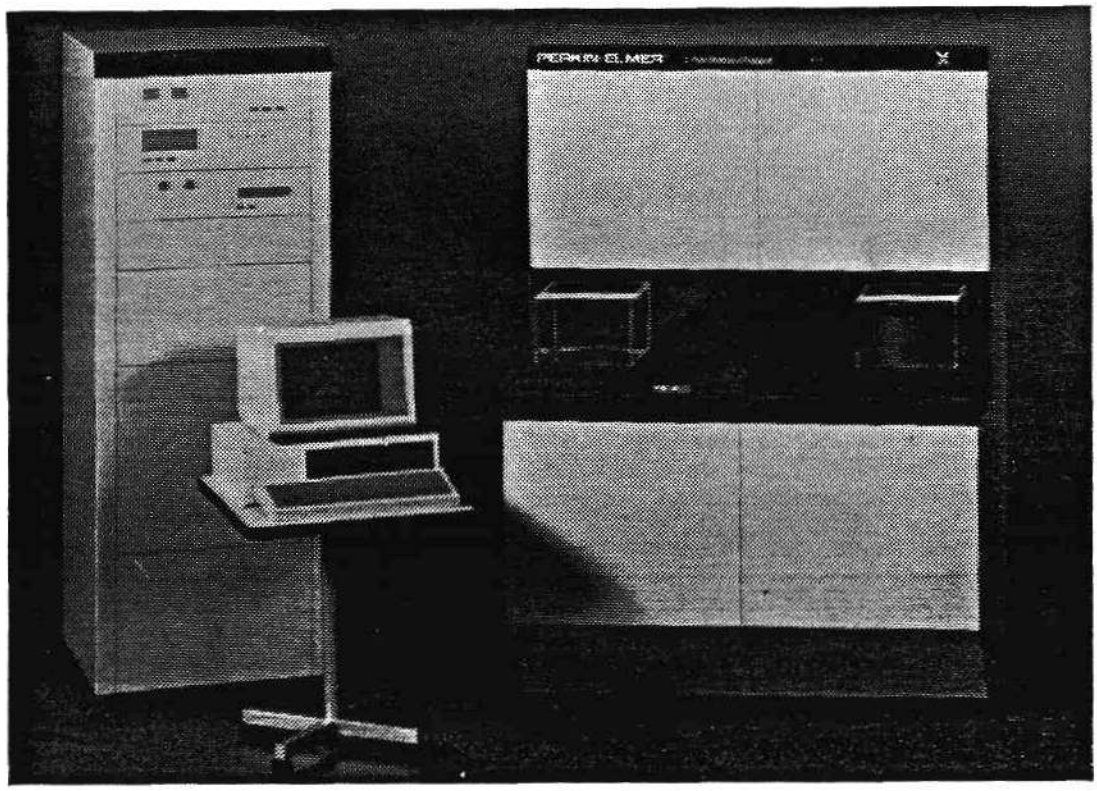
X-RAY STEP-AND-REPEAT PERFORMANCE GOALS

RESOLUTION	**<0.5 μm**	**PENUMBRA <0.25 μm**
FIELD SIZE	**30 mm x 30 mm**	**NOMINAL**
WAFERS	**100 mm to 200 mm**	
OVERLAY	**<0.1 μm**	**2 SIGMA INCLUDING MASK**
THROUGHPUT (ROTATING ANODE)	**>40 W/HR.**	**100 mm WAFERS**

X-RAY STEP-AND-REPEAT SYSTEM



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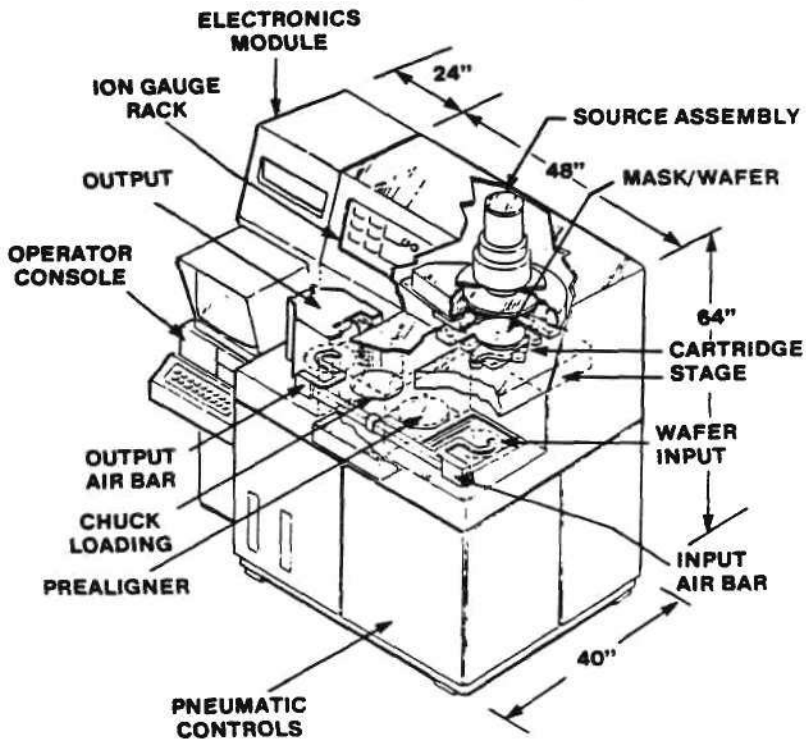
X-RAY STEP-AND-REPEAT SYSTEM CUTAWAY



X-RAY SOURCES

STATIONARY ANODE (MATURE)	- MECHANICALLY LESS COMPLEX - LOW THROUGHPUT - MODERATE RESOLUTION
ROTATING ANODE (MATURE)	- ROTATING MECHANISM REQUIRED - HIGH THROUGHPUT - HIGH RESOLUTION
PLASMA SOURCE (DEVELOPMENTAL)	- COMPLEX HARDWARE - VERY HIGH THROUGHPUT - HIGH RESOLUTION - PRODUCTION FEASIBILITY TO BE DEMONSTRATED
SYNCHROTRON (DEVELOPMENTAL)	- MULTIPLE ALIGNERS - COMPLEX HARDWARE - VERY HIGH THROUGHPUT - HIGH RESOLUTION

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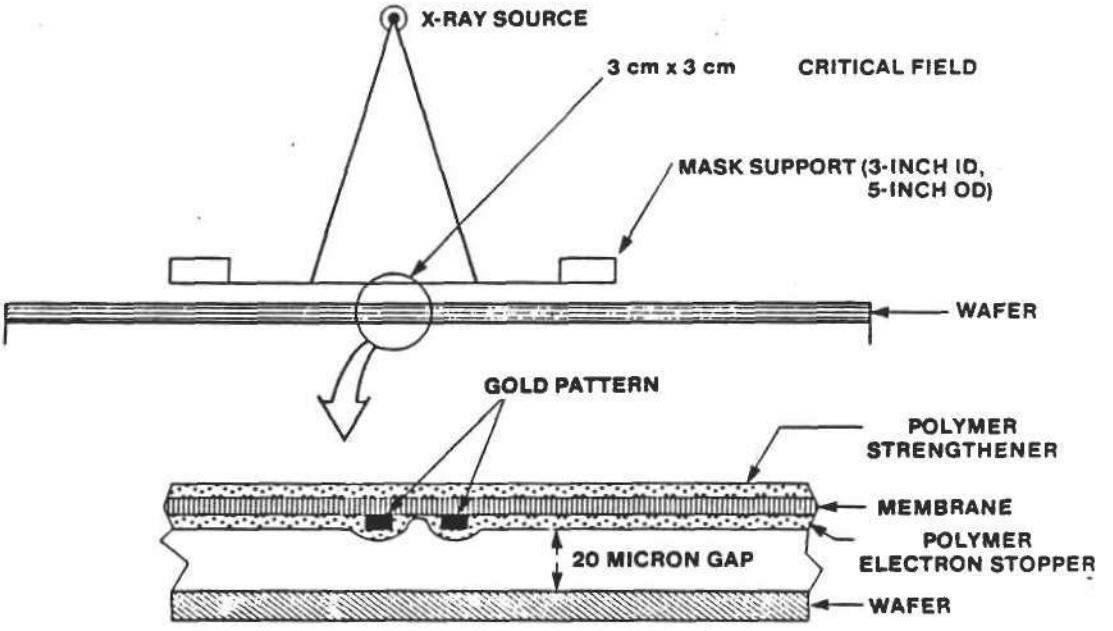
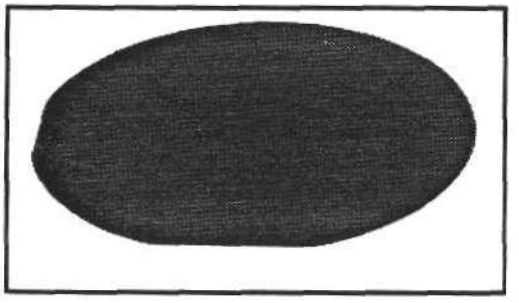
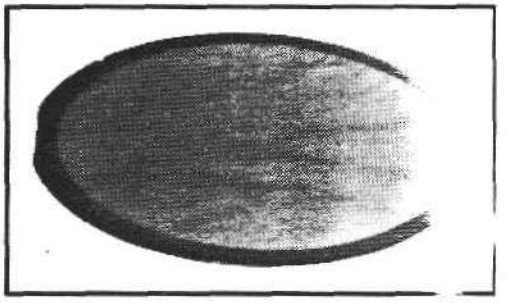
X-RAY MASK MEMBRANE CONCEPT



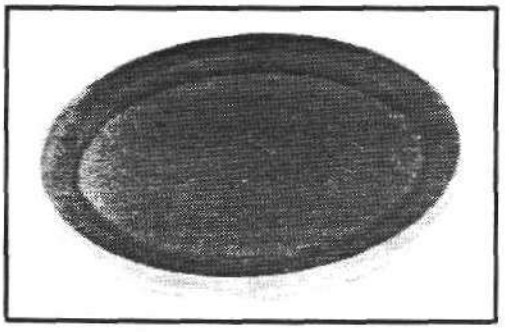
BASELINE COMPRESSIVE PROCESS



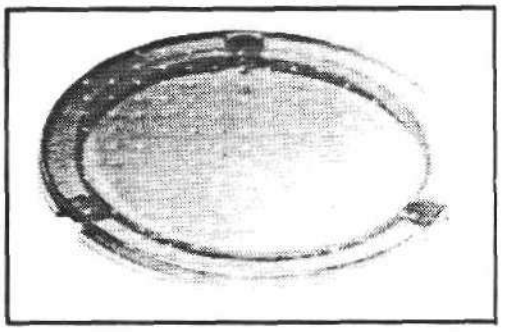
BN on Si



BN AFTER Si ETCH



STRETCHED MEMBRANE



PATTERNED MEMBRANE

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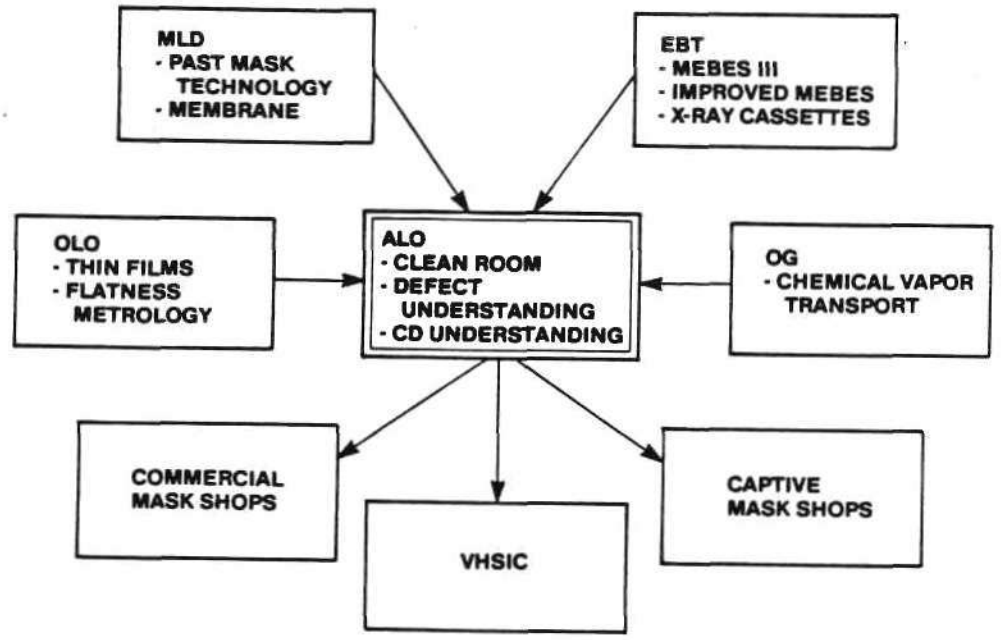
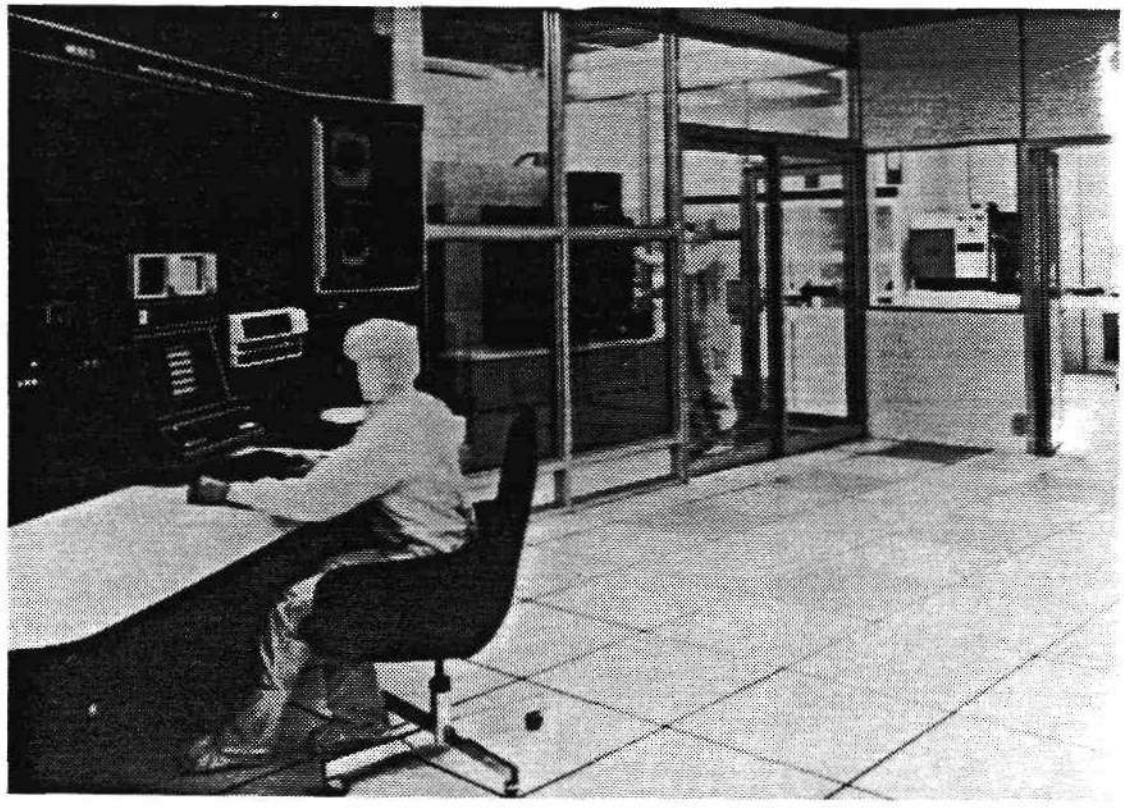
APPLIED LITHOGRAPHY OPERATIONS TECHNOLOGY BASE X-RAY MASKS



MEBES III



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X-RAY RESISTS

- **USES E-BEAM RESISTS WHICH ARE ALSO SENSITIVE TO SOFT X-RAY EMISSION**
- **NEGATIVE TYPE RESISTS**

RESIST/PROCESSING STATUS

		RESOLUTION (μm)	SENSITIVITY (mJ/cm^2)
• COMMERCIALLY AVAILABLE			
- BELL	DCOPA	0.7 - 0.5	27
-	PBS	0.5	300
- KODAK	EK771	0.5	100
- SEL-N		0.8	200
- CMS		0.75	400
- MEAD/HP	PCMS	1 - 0.5	30-50
• R&D DEVELOPMENT			
- BELL	PDXR2	0.5	10
- KODAK	HIGH MW	0.75	70
	LOW MW	0.5	300
- SHIPLEY			
- AMERICAN CYANAMID			200
- GREAT LAKES			

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SILICON FOR VLSI/ULSI CIRCUITS

Haskell T. Waddle
Vice President, Commercial
Monsanto Electronic Materials Company

Mr. Waddle is Vice President, Commercial, of Monsanto Electronic Materials Company, an operating unit of Monsanto Company. Mr. Waddle joined Monsanto in 1964 as a Sales Engineer at a Monsanto subsidiary, Fisher Controls International. He later worked at Monsanto's Commercial Products Company and Optoelectronic Devices Business Group. In 1979, he was named Director of Marketing for the company's Electronics Division. The Electronics Division became Monsanto Electronic Materials Company in 1983, and Mr. Waddle was named Vice President, Marketing, for the company. In 1985, he became Vice President, Commercial. Mr. Waddle graduated from the University of Oklahoma with a B.S. degree in Engineering Physics.

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SILICON FOR VLSI/ULSI CIRCUITS
A Material in Transition

I. Introduction

A. The purpose of this VLSI/ULSI silicon review is to gain a better understanding of trends in silicon specifications and world markets which most impact the eventual outcome of the worldwide semiconductor device competitive race currently underway.

B. Recent silicon geographic consumption trends and investment plans seem to suggest the competitive race may be nearing a conclusion.

C. However, silicon opportunities which can contribute to healthy, balanced worldwide growth of semiconductor device markets do exist and are being aggressively pursued.

II. The Increasing Importance of Silicon

A. Semiconductor devices -- improved circuit performance, increased yield.

B. Engineeered specifically to circuit application needs.

III. Trends in Semiconductors Affecting Silicon

A. VLSI and ULSI circuits.

B. Move to larger diameter, application specific wafers.

C. Automated wafer handling.

D. Geographic market imbalances.

IV. Resulting Demands on Silicon

A. Electronic parameters.

B. Structural characteristics.

C. Chemical characteristics.

D. Mechanical characteristics.

E. Parts-per-million quality levels.

F. Application specific silicon wafers.

G. Worldwide silicon market requirements.

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V. Trends/Developments in Silicon

- A. ULSI wafers.
- B. Epi wafers
- C. Key silicon process developments.
  1. Parts-per-million quality control.
  2. Cleaning and packaging.
  3. Modifications.
  4. High throughput epi reactors.
  5. Single crystal growth.
  6. Poly silicon.

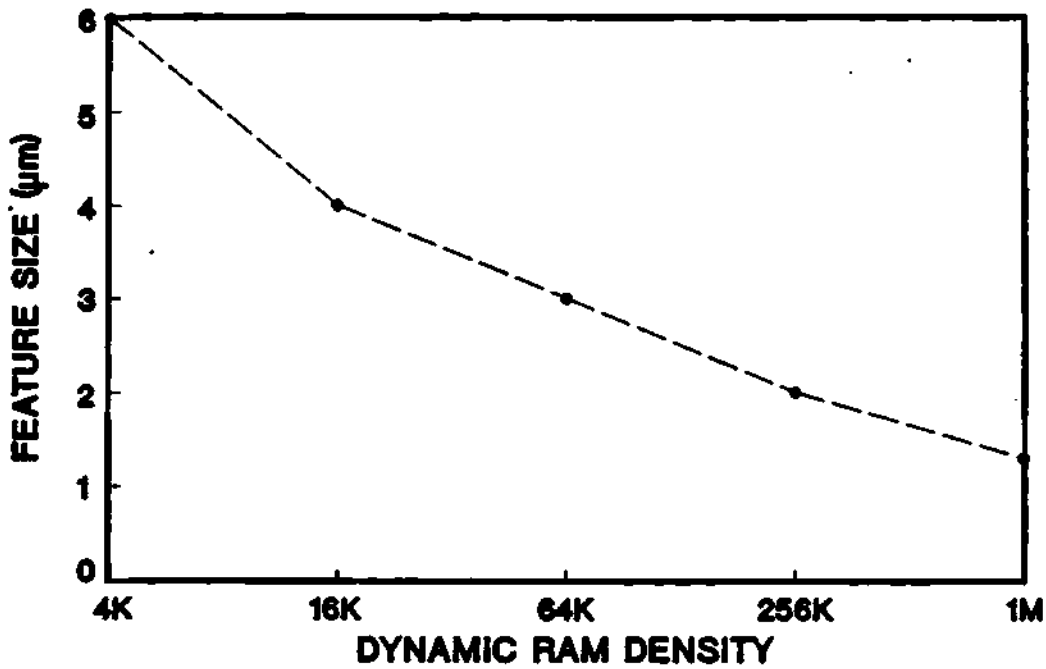
VI. Fab Line Practices

- A. Silicon design parameters.
- B. Joint development programs.
- C. Application specific specifications.
- D. Fab line practices.
  1. Diagnostics.
  2. Wafer handling.
  3. Roll of Incoming Quality Assurance.

VII. Conclusions

- A. Leverages from silicon.
  1. VLSI.
  2. ULSI.

CORRELATION OF MINIMUM FEATURE SIZE WITH DRAM DENSITY



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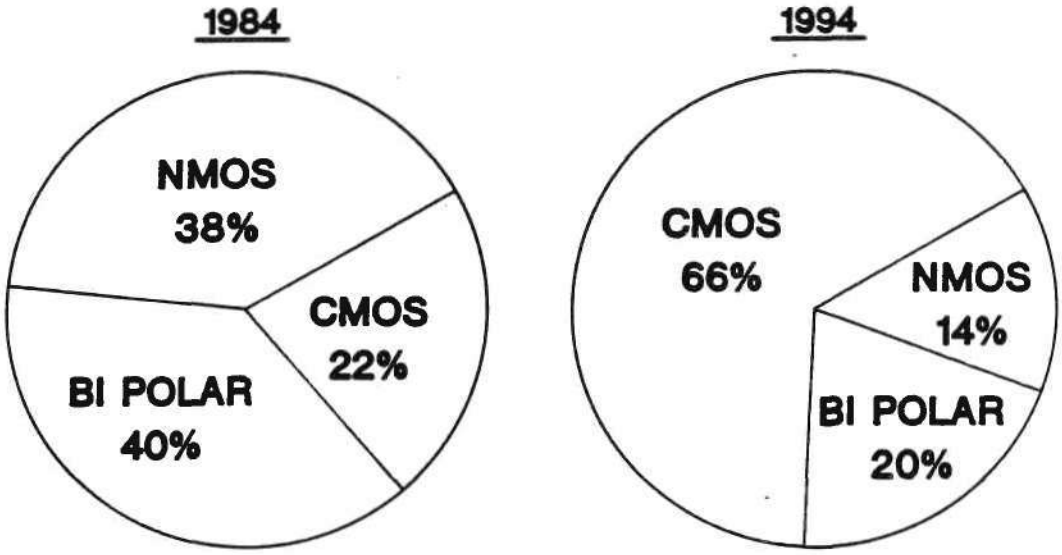
THE SILICON WAFER MARKET

IC Consumption



CMOS WILL BE THE DOMINANT TECHNOLOGY

LSI/MSI APPLICATION SERIES WAFER SCHEMATIC

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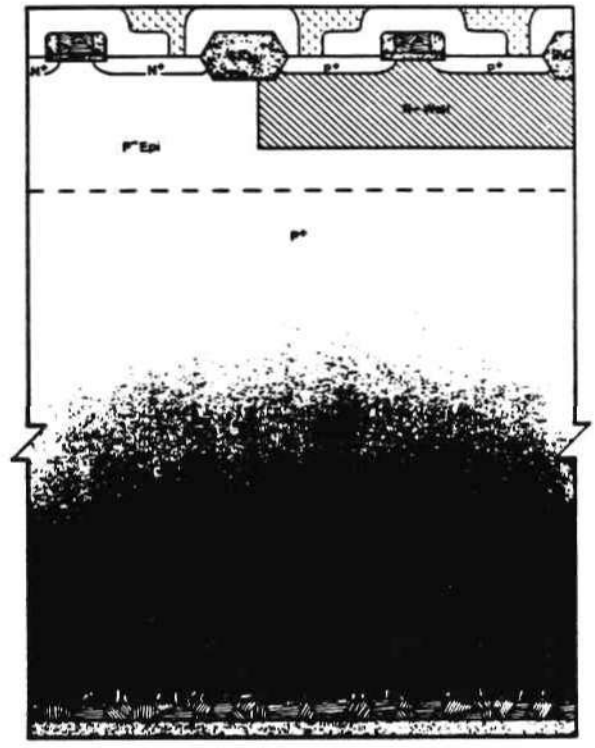
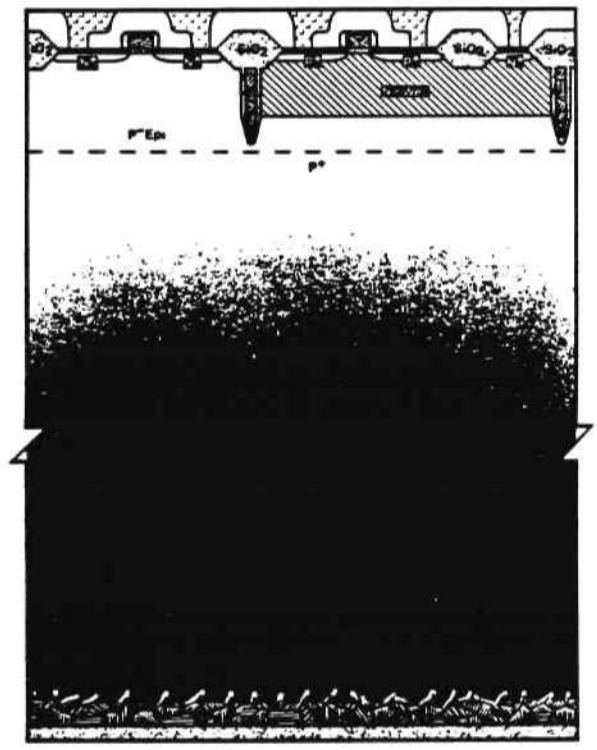
VLSI APPLICATION SERIES WAFER SCHEMATIC



ULSI APPLICATION SERIES WAFER SCHEMATIC



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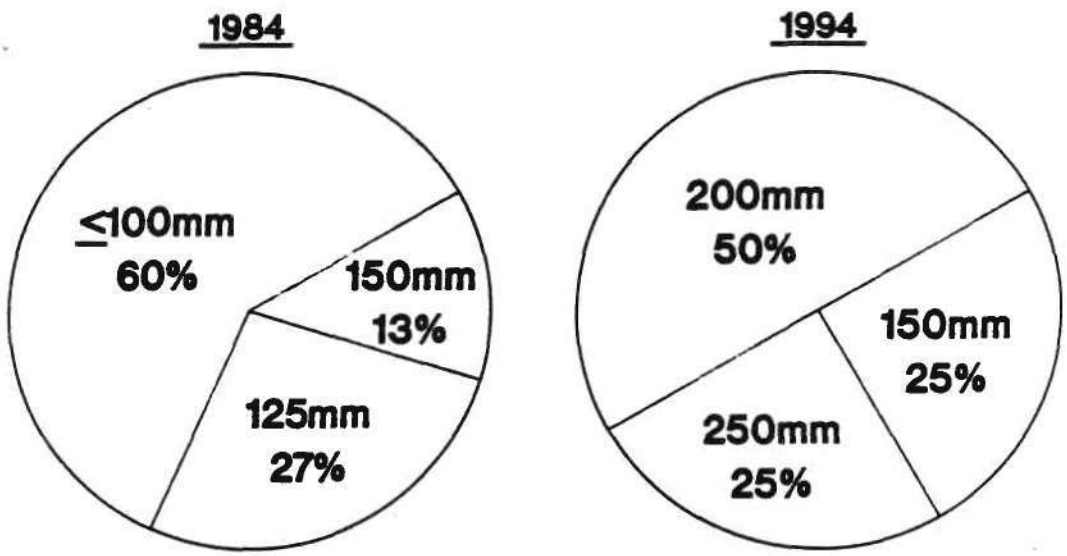
THE SILICON WAFER MARKET

Diameter Mix



DIAMETER WILL CONTINUE TO INCREASE

TEST-DEVICE ELECTRONIC PARAMETERS

PARAMETER	VALUE
- Oxide Leakage Current	$\leq 10^{-12}$ A at 10 V
- Oxide Breakdown Voltage Distribution	≤1% Failure for Electric Field $\leq 5 \times 10^{6}$ V/cm
- Interface State Density	$\leq 2 \times 10^{10} cm^{-2} eV^{-1}$
- Flat-Band Voltage Shift	≤0.2 V
- Minority-Carrier Generation Lifetime	~300-1000 µsec
- Diode Leakage Current	$\leq 10^{-10}$ A at 10 V
- Threshold Voltage Control	Resistivity Variation ≤10%

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STRUCTURAL CHARACTERISTICS

PARAMETER	VALUE
- Wafer Perfection	No X-Ray Resolved Bulk Structural Defects
- Grown-In Dislocations (Etch Pits)	0 cm^{-2}
- Oxidation-Induced Stacking Faults (OISF)	$\leq$3 cm^{-2}
- Micro-Defects (S-Pits)	$\leq$100 cm^{-2}

STRUCTURAL CHARACTERISTICS (Cont'd)

PARAMETER	VALUE
- External Gettering (Recommended)	Back-Surface Polysilicon
- Wafer Uniformity	Reproducibility Within Wafer, Wafer to Wafer, and Crystal to Crystal
- Epitaxial Layer (Recommended for CMOS and Selected NMOS Circuits)	Customer Specified Resistivity and Thickness $\leq$3 OISF cm^{-2}

CHEMICAL CHARACTERISTICS

PARAMETER	VALUE
– Cleanliness	
Front-Surface Particles	≤0.03/cm² (≤0.5 μm)
Back-Surface Particles	≤0.05/cm² (≤1 μm)
Back-Surface Stain/ Residues	None
Front-Surface Chemical (Native) Oxide	Hydrophilic

CHEMICAL CHARACTERISTICS
(Cont'd)

PARAMETER	VALUE
– Oxygen	Customer Specified
Tolerance	±2 ppma
Precipitation	Controlled, Reproducible
Radial Gradient	≤3%
– Carbon	≤0.3 ppma
– Metallics	
Bulk	<0.01 ppba for Specific Metallics
Surface	$\leq 10^{10}/cm^2$

MECHANICAL CHARACTERISTICS

PARAMETER	VALUE
- Diameter	150 mm
Tolerance	$\leq \pm 0.2$ mm
- Orientation Flat Tolerance	$\leq \pm 1.5$ mm
- Thickness	625, 675 µm
Tolerance	$\leq \pm$ 10 µm
- Taper	$\leq$ 10 µm
- Global Flatness	$\leq$ 3 µm

MECHANICAL CHARACTERISTICS (Cont'd)

PARAMETER	VALUE
- Local Site Flatness	$\leq$1.0 µm across a 20 x 20 mm² Field
- Wafer Curvature (Polished Surface)	Convex or Concave Specified by Customer
- Bow	$\leq$10 µm
- Warp	$\leq$10 µm
- Edge Contour	Chip-Free

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Nielsen Dataquest

IMAGE PROCESSING--ITS CHANGING ROLE IN THE SEMICONDUCTOR INDUSTRY OVER THE PAST 20 YEARS

Kenneth Levy
President
KLA Instruments Corporation

Mr. Levy is President and cofounder of KLA Instruments Corporation. He also serves on the Board of Directors of the Semiconductor Equipment and Materials Institute (SEMI) and as a board member for two SEMI companies, Micronix and Therma-Wave Inc. Prior to cofounding KLA, Mr. Levy was employed by Computervision Corporation as President of its Cobilt Division and Director of Computervision. He has been involved in the semiconductor capital equipment field since 1969. In 1983, he and KLA received the SEMMY award from the Semiconductor Equipment and Materials Institute for innovations in high-speed image processing. Mr. Levy received a B.S. degree in Electrical Engineering from the City College of New York and an M.S. degree in Electrical Engineering from Syracuse University.

Dataquest Incorporated
SEMICONDUCTOR EQUIPMENT AND MATERIALS INDUSTRY SERVICE CONFERENCE
October 14-16, 1985
Tucson, Arizona

"IMAGE PROCESSING--ITS CHANGING ROLE IN THE SEMICONDUCTOR INDUSTRY OVER THE PAST TWENTY YEARS"

BY KENNETH LEVY
PRESIDENT & CHIEF EXECUTIVE OFFICER
KLA INSTRUMENTS CORPORATION

INTRODUCTION

IN HIS REPORT ON "YIELD PROBLEMS IN LSI TECHNOLOGY", G.H. SCHUUTTKE OF IBM STATED:

> THE DEGREE OF COMPLEXITY LEVELS ATTAINABLE ON CHIPS WAS RECENTLY STUDIED BY SEVERAL COMPANIES. THESE STUDIES SHOW THAT COMPLEXITY LEVELS ATTAINABLE ARE CLOSELY TIED TO YIELD PROBLEMS. ONE OF THE MAJOR CONCLUSIONS OF THESE STUDIES IS THAT FUTURE CHIP SIZE IS SEVERELY LIMITED BY YIELD PROBLEMS AND THAT OVERALL YIELD IMPROVEMENTS CAN ONLY BE ACHIEVED BY IDENTIFYING MAJOR YIELD LOSS MECHANISMS. MAJOR YIELD PROBLEMS IN LSI TECHNOLOGY ARE CAUSED THROUGH PHOTOMASKING AND METALIZATION PROCESSES. IN ADDITION, IT HAS BECOME APPARENT THAT THE SILICON MATERIAL ITSELF CAN BE A DOMINATING FACTOR IN REDUCING THE YIELD OF GOOD CIRCUITS ON A WAFER.

THIS STATEMENT, WHICH CERTAINLY SOUNDS LIKE IT COULD HAVE BEEN WRITTEN TODAY, WAS MADE IN SCHUUTTKE'S REPORT TO THE AIR FORCE IN 1970. IDENTIFICATION OF THE MAJOR YIELD LOSS POINTS AND THE RAPID IMPROVEMENT OF THE YIELD LOSS POINTS HAS BEEN ONE OF THE KEY POINTS OF SUCCESS FOR THE MANUFACTURERS OF LEADING EDGE DEVICES THROUGHOUT THE HISTORY OF THE SEMICONDUCTOR INDUSTRY.

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IN THIS TALK, I WILL OUTLINE SOME OF THE MAJOR ADVANCES THAT HAVE BEEN MADE OVER THE YEARS AND DISCUSS WHY IMAGE PROCESSING TECHNOLOGY IS DESTINED TO PLAY AN INCREASINGLY IMPORTANT ROLE IN THE MANUFACTURE OF VLSI OVER THE NEXT DECADE.

THE EARLY YEARS

IF ANY ONE TAKES THE TIME TO LOOK AT SOME OF THE OLD LITERATURE DESCRIBING THE ACTIVITIES WHICH WERE TAKING PLACE IN THE LATE 50'S AND EARLY 60'S, IT IS IMMEDIATELY APPARENT THAT THE FIRST YIELD PROBLEMS WITH INTEGRATED CIRCUITS OCCURRED THE DAY AFTER JACK KILBY FILED THE OIRIGINAL PATENT ON FEBRUARY 9, 1959, ON THE INTEGRATED CIRCUIT. THE TECHNLOLGY DEVELOPED BY KILBY AT TEXAS INSTRUMENTS AND NOYCE AT FAIRCHILD LAUNCHED THE ELECTRONICS INDUSTRY INTO THE MODERN ERA OF INTEGRATED CIRCUITS. FROM THAT DAY UNTIL TODAY, THERE HAS BEEN A REMARKABLE CONSISTENCY IN THE INDUSTRY--"ONLY THE MOST COMPETENT MANUFACTURERS CAN SURVIVE THE TREMENDOUS PRICE COMPETITION WHICH INEVITABLY OCCURS WITHIN ONE TO TWO YEARS AFTER A DEVICE IS ANNOUNCED!"- NOTHING MUCH HAS CHANGED IN THE I.C. BUSINESS FROM THE SPRING OF 1961 WHEN FAIRCHILD BOMBED THE PRICE FOR A FLIP-FLOP TO $120, LEAVING T.I.--WHO WAS SELLING THEM FOR $450 EACH--WONDERING WHEN THIS "DUMPING" WOULD CEASE. TEN YEARS LATER, JIM RILEY, PRESIDENT OF INTERSIL, WOULD ISSUE THE FOLLOWING QUOTE TO ELECTRONIC NEWS, "NO SEMICONDUCTOR COMPANY IN THE WORLD CAN MAKE A PROFIT ON A 7400 GATE AT 12 CENTS A PACKAGE."

THAT WERE THE ADVANCEMENTS IN MANUFACTURING PROCESSES AND YIELD ENHANCEMENTS THAT ALLOWED PRICES TO BE REDUCED BY A THOUSAND-FOLD DURING THAT PERIOD? WAS IT DRIVEN BY MATERIALS, PROCESS TECHNOLOGY, OR PHOTOLITHOGRAPHIC TECHNIQUES? WHILE THE ANSWER IS NEVER SIMPLISTIC AND ALL OF THESE FACTORS PLAYED AN IMPORTANT PART, THE YIELD IMPROVEMENT IN THIS TEN-YEAR PERIOD OF THE EARLY 60'S TO EARLY 70'S WAS DOMINATED BY IMPROVEMENTS IN PROCESS TECHNOLOGY AND MATERIALS.

A MASSIVE EFFORT WAS MOUNTED BY THE SILICON MANUFACTURERS TO IMPROVE BOTH THE CRYSTAL AND PHYSICAL PROPERTIES OF THE STARTING SILICON WAFERS. DISLOCATION DENSITY IN CRYSTALS, WHICH HAD A LARGE EFFECT ON PROCESS YIELDS, WAS REDUCED TO ALMOST ZERO, EDGES WERE CHAMFERED, WAFER CROSS SECTION WAS INCREASED TO GREATLY REDUCE BREAKAGE AND WARPAGE, AND MECHANICAL TOLERANCES WERE REDUCED TO ALLOW AUTOMATIC HANDLING.

ADVANCES IN DIFFUSION AND ION IMPLANT ALSO PROGRESSED AT A RAPID RATE. GAS AND CHEMICAL PURITY WERE IMPROVED TO THE POINT THAT YIELD LOSS DUE TO CONTAMINANTS BECAME ALMOST NON-EXISTENT. TEMPERATURES, PRESSURES AND UNIFORMITY IN THE DIFFUSION FURNACES BECAME BOTH CONTROLLABLE AND REPRODUCABLE, AND THOSE DIFFUSIONS THAT COULD NOT BE ACHIEVED IN THE DIFFUSION FURNACE COULD BE AUGMENTED BY THE NEWLY DEVELOPED ION-IMPLANT SYSTEMS.

THE LIST OF AREAS WHERE MAJOR IMPROVEMENTS WERE MADE IN THE PROCESS GOES ON AND ON--METALIZATION, CHEMICAL VAPOR DEPOSITION, PASSIVATION & EPITAXY. IMPROVEMENTS IN THESE PROCESSES WERE NECESSARY TO FABRICATE THE DEVICES THAT THE GROWING ELECTRONICS INDUSTRY WAS REQUIRING AT THE TIME.

PHOTOLITHOGRAPHY

BY NOW, ANY ASTUTE FOLLOWER OF SEMICONDUCTOR PROCESSING HAS GOT TO BE ASKING "WHAT ABOUT PHOTOLITOHGRAPHY? WHY HAVEN'T YOU MENTIONED IT YET?"

THE ANSWER IS: "UP TO THE MID-SEVENTIES, THE SEMICONDUCTOR INDUSTRY WAS NOT PUSHING THE LIMITS OF OPTICAL TECHNOLOGY, AND THEREFORE PHOTOLITHOGRAPHY--WHILE ALWAYS SOME WHAT OF A "PAIN"--WAS NOT THE LIMITING FACTOR IN THE MANUFACTURE OF INTEGRATED CIRCUITS.

IN 1966, THE FOURTH EDITION OF INTEGRATED CIRCUIT ENGINEERING REPORT ON PROCESS CONTROL LISTED THE FOLLOWING TYPICAL YIELD LOSS:

	BASIC OPERATION	REMAINING CIRCUITS (X10)	TYPICAL CAUSES	AVERAGE YIELD
1.	START	2000	----------	---
2.	CHANNEL DIFFUSION	1900	POOR ISOLATION EPI LAYER CONTROL	95%
3.	BASE DIFFUSION	1710	SHEET RESISTANCE OUT OF SPEC.	90%
4.	EMITTER DIFFUSION	1455	"PUNCH THROUGH" EMITTER TO DEEP	85%
5.	METALIZATION	1310	BREAKAGE - POOR HANDLING	90%
6.	WAFER TESTING	980	DEVICES NOT TO SPEC.	75%
			PROCESSING YIELD	49%
7.	WAFER SCRIBING	832	UNEVEN BREAKAGE	85%
8.	DIE AND WIRE BOND	708	DAMAGE IN HANDLING, OPEN WIRES	85%
9.	PACKAGING	672	IMPROPER SEALING	95%
10.	FINAL TEST	505	CIRCUITS NOT TO SPEC.	75%
			ASSEMBLY YIELD	51.5%
			TOTAL YIELD	29.2%

NOTICE THAT MOST OF THE YIELD LOSS COULD BE ATTRIBUTED TO MATERIALS AND PROCESS CONTROL PROBLEMS. YIELD LOSS DUE TO MATERIAL PROBLEMS SUCH AS WAFER BREAKAGE, EPI LAYER CONTROL, SHEET RESISTANCE AND GENERAL OUT OF SPECIFICATION DEVICES CAUSED A LOSS OF ALMOST 50% OF THE UNITS MANUFACTURED. PACKAGING PROBLEMS HALVED THE YIELD AGAIN. LOOKING BACK AT THE PROCESS PROBLEMS AND THE YIELD LOSSES THE PROCESSES CAUSED MEANT THAT SEMICONDUCTOR MANUFACTURERS COULD GAIN GREATLY BY IMPROVING THE BASIC SILICON MATERIAL AND CHEMICAL PROCESSES.

PHOTOLITHOGRAPHY LIMITATIONS DID NOT DOMINATE THIS PERIOD. A LOOK AT THE DIE SIZES, SMALLEST LINE WIDTHS ON THE CIRCUITS, AND THE EXPOSURE METHODS OF THE PRE-1973 ERA EASILY CONFIRMS THIS FACT.

LOOKING BACK AT THE PHOTOLITHOGRAPHIC ARENA OF THE EARLY 1970'S, THE FOLLOWING SITUATION EXISTED:

THE LARGEST DICE WERE ABOUT 125 MILS ON A SIDE, OR ABOUT 300 DICE ON A 3-INCH WAFER, WHICH WAS JUST THEN BECOMING INDUSTRY STANDARD. IF THE WAFERS AND DIE WERE SMALL BY TODAY'S STANDARDS, THE GEOMETRIES WERE HUGE. THE INDUSTRY WAS GOING THROUGH A FEATURE SIZE REDUCTION-- FEATURES WERE BEING REDUCED FROM 10 MICRONS TO 7 MICRONS. THESE LARGE GEOMETRIES WERE

TRANSFERRED FROM A EMULSION MASK TO THE WAFER BY A CONTACT PRINTING PROCESS. THIS IS THE SIMPLEST TYPE OF IMAGE TRANSFER THAT WE CAN IMAGINE. THE WAFER IS PRESSED TIGHTLY AGAINST THE MASK AND A "FLOOD LAMP" IS TURNED ON TO EXPOSE THE PHOTORESIST. WHAT COULD BE SIMPLER--NOT ONLY WAS THE PROCESS SIMPLE (AND INEXPENSIVE--A MASK ALIGNER OF THAT ERA SOLD FOR LESS THAN $10,000) BUT THE PROCESS HAD SEVERAL VERY NICE FEATURES. FIRST, THE LARGE FEATURES (7 MICRON), COUPLED WITH THE INHERENTLY HIGH RESOLUTION LIMIT OF CONTACT PRINTING, MADE LINE WIDTH CONTROL TRIVIAL. PUSHING THE WAFER HARD AGAINST THE MASK IN COMBINATION WITH A HIGHLY COLLIMATED LIGHT SOURCE MADE DEPTH OF FOCUS A NON-ISSUE, AND THE INHERENTLY HIGH MODULATION TRANSFER FUNCTION OF THE CONTACT PRINTING PROCESS ALLOWED ONE TO OVER-EXPOSE THE RESIST, MAKING EXPOSURE CONTROL AND RESIST SENSITIVITY CONTROL A MINOR ISSUE.

THERE WAS ONLY ONE MAJOR PROBLEM WITH THE SYSTEM, AND THAT WAS THAT THE FUNDAMENTAL MECHANISM BY WHICH THE SYSTEM OPERATED--THE HARD CONTACT BETWEEN THE PHOTOMASK AND WAFER DAMAGED THE PHOTOMASK. RESIST WOULD STICK TO THE CLEAR AREAS OF THE MASK, AND EPI SPIKES (YOU OLD TIMERS REMEMBER THESE) WOULD SCRATCH THE EMULSION.

WELL, AS LONG AS THE GEOMETRIES STAYED LARGE, PROCESSES LIKE "DOUBLE MASKING" AND "LOW RESOLUTION RESIST PROCESSES" WOULD

REDUCE THE PHOTOMASK DEFECTS TO AN ACCEPTABLE (NON-YIELD LIMITING) LEVEL.

THE MIDDLE YEARS

ALTHOUGH FEW PEOPLE RECOGNIZED IT AT THE TIME, SEMICONDUCTOR MANUFACTURING AND THE PHOTOLITHOGRAPHIC PROCESS WAS ABOUT TO BE REVOLUTIONIZED IN 1973. THAT WAS THE YEAR THAT PERKIN ELMER ANNOUNCED THE FIRST SUCCESSFUL PROJECTION ALIGNER, THE MICRALIGN 100. FOR THE FIRST TIME, A COMMERCIAL MASK ALIGNER WAS ABLE TO PROJECT THE IMAGE OF A PHOTOMASK ONTO A WAFER WITHOUT BRINGING THE MASK AND WAFER IN CONTACT. THIS ALIGNMENT AND EXPOSURE SYSTEM IS PROBABLY THE SINGLE MOST IMPORTANT ADVANCEMENT LEADING TO THE AGE OF LSI CIRCUITS. FOR NOW, THE SEMICONDUCTOR MANUFACTURER COULD START WITH AN EXCELLENT SET OF PHOTOMASKS AND NOT DESTROY THEM IN THE PROCESS OF TRANSFERRING THE IMAGE TO THE WAFER.

BUT HOW WAS ONE TO GET A GOOD QUALITY PHOTOMASK? THE DEVICE MAKER DID WHAT ANY REASONABLE PROCESS ENGINEER WOULD DO--HE SPECIFIED THE QUALITY TO THE "OTHER GUY", THE MASK MAKER.

AND WHAT DID THE MASK MAKER DO? WELL, HE CONVINCED THE DEVICE MAKER HE SHOULD USE CHROME AND NOT EMULSION PHOTOMASKS. HE STARTED TO EMPLOY LARGE GROUPS OF HIGHLY

TRAINED TECHNICIANS WITH KEEN EYESIGHT AND "THE PATIENCE OF JOB" STARE THROUGH MICROSCOPES FOR HOURS ON END AND INSPECT TO THE PHOTOMASKS TO ASSURE THE END CUSTOMER THAT THE DEFECT DENSITY ON THE PHOTOMASK MET THE SPECIFIED QUALITY--WHICH IT ALWAYS DID BECAUSE NONE OF THE RESULTS OF THESE INSPECTIONS WOULD EVER CORRELATE WITH A SUBSEQUENT INSPECTION (IF ANYONE EVER HAD THE COURAGE TO RUN SUCH A TEST).

WHAT EXISTED IN THIS PERIOD WAS A UNIQUE SITUATION WHICH OCCURS IN INDUSTRY FROM TIME TO TIME--OUR ABILITY TO SPECIFY EXCEEDS OUR ABILITY TO VERIFY.

THIS TECHNICAL IMBALANCE FOSTERS INNOVATION. ARTICLES STARTED TO APPEAR IN THE TECHNICAL PUBLICATION DEALING WITH PHOTOMASK QUALITY. AS THE APPLICATION OF THESE WONDERFUL NEW MICRALIGN SYSTEMS BECAME MORE WIDESPREAD, IT BECAME INCREASINGLY CLEAR THAT DEFECT DENSITY ON THE PHOTOMASKS WERE BEGINNING TO DOMINATE THE YIELD ON THE LARGE AND DENSE SEMICONDUCTOR DEVICES BEING DESIGNED.

IN 1978, AFTER TWO YEARS OF DEVELOPMENT, KLA INTRODUCED THE FIRST COMMERCIALLY AVAILABLE PHOTOMASK INSPECTION SYSTEM. OR THE FIRST TIME, A SYSTEM WAS AVAILABLE THAT COULD RAPIDLY INSPECT AN ENTIRE PHOTOMASK, FIND ALL DEFECTS WITH HIGH PROBABILITY AND PRODUCE AN IMPARTIAL, REPEATABLE REPORT WHICH OUTLINED THE SIZE AND POSITION OF THE DEFECTS ON THE PHOTOMASKS. ARMED WITH THIS SYSTEM, PROGRESS WITH RESPECT TO

PHOTOMASK QUALITY ACCELERATED RAPIDLY. ONCE THE QUALITY PROBLEMS ON THE PHOTOMASKS COULD BE IDENTIFIED QUICKLY AND ACCURATELY, THE ENGINEERS IN THE PHOTOMASK FABRICATION AREAS STARTED TO IDENTIFY THE MAJOR CAUSES OF THE PROBLEMS. IMPROVEMENTS WERE MADE IN GLASS SUBSTRATES, CHROME COATINGS, PHOTORESIST MATERIALS, ETCHING PROCESSES, CLEANING PROCESSES, ETC.

THE RESULTS OF THESE CONCENTRATED AND DIRECTED ENGINEERING EFFORTS ARE EVIDENT. DEFECT DENSITIES ABOVE 2 MICRONS DECREASED BY AN ORDER OF MAGNITUDE IN FIVE YEARS. WHEN THIS EFFORT WAS COMPLETE, THE DEFINITION OF A DEFECT WAS REDUCED FROM 2 MICRONS TO 1 MICRON AND THE QUEST FOR PERFECTION BEGAN AGAIN. ONCE AGAIN, DEFECT DENSITIES WERE REDUCED AND PERFECTION WAS APPROACHED, AND ONCE AGAIN THE SPECIFICATION WAS TIGHTENED.

WITH THE DECREASING GEOMETRIES OF THE SMALLEST FEATURES ON THE CIRCUIT, A DEFECT WAS FURTHER DEFINED TO BE ANY ANOMALY ON THE PHOTOMASK WHICH EXCEEDED 1/2 MICRON IN SIZE. THIS NEW SPECIFICATION REQUIRED A NEW GENERATION OF INSPECTION EQUIPMENT TO BE DESIGNED, THIS NEW EQUIPMENT, WHICH WAS INTRODUCED WITHIN THE PAST YEAR, IS ENABLING THE TECHNICAL COMMUNITY TO PRODUCE PHOTOMASKS WHICH ARE VIRTUALLY DEFECT-FREE TO SUB-MICRON ANOMALIES.

FURTHERMORE, WE HAVE INTRODUCED ION-BEAM REPAIR SYSTEMS THAT CAN TAKE AN "ALMOST" PERFECT PHOTOMASK AND EITHER ADD OR REMOVE OPAQUE AREAS AS SMALL AS 0.2 MICRONS, THEREBY POST-FABRICATING THE MASK TO ABSOLUTELY PERFECT CONDITION. THE ADVENT OF THE WAFER STEPPER IN THE LATE 70'S PRODUCED A NEW TYPE OF PHOTOMASK--THE "SINGLE DIE RETICLE". IF DEFECTS ON PHOTOMASKS COULD CAUSE SEVERE YIELD PROBLEMS, A SINGLE DEFECTON A RETICLE COULD RUIN AN ENTIRE MONTH'S PRODUCTION OF A HIGH RUN DEVICE. ONCE AGAIN, "IMAGE PROCESSING" WAS CALLED UPON TO ALLOW REASONABLE YIELDS FOR THE NEWEST PHOTOLITHOGRAPHIC PROCESSING TECHNIQUES.

SEVERAL YEARS AGO, WE INTRODUCED THE "KLARIS" (KLA'S RETICLE INSPECTION SYSTEM). THIS SYSTEM ACCEPTS THE COMPUTER AIDED DESIGN TAPE AND COMPARES THE ACTUAL IMAGE ON THE GLASS RETICLE TO THE DESIGN DATA ON THE TAPE. THIS SYSTEM IS WIDELY USED BY PHOTOMASK MAKERS TO ASSURE THE QUALITY OF THE PRODUCT BEFORE SHIPPING TO THE USER. IF A DEFECT IS FOUND ON THE RETICLE, IT IS REPAIRED BY THE MASK MAKER ON A LASER OR ION BEAM REPAIR STATION.

WAFER PROCESSING ENGINEERS ALSO USE THE SYSTEM. AFTER PLACING THE RETICLE IN A STEPPER AND PRIOR TO COMMITING THOUSANDS OF DOLLARS OF SILICON TO THIS ONE PIECE OF TOOLING, A SURROGATE WAFER IS PLACED IN THE STEPPER. EXPOSED AND DEVELOPED. THE WAFER SURROGATE IS THEN INSPECTED ON A RETICLE INSPECTION SYSTEM AND COMPARED WITH THE DESIGN DATA.

THUS, THE WAFER PROCESSING ENGINEER IS ASSURED THAT EACH AND EVERY IMAGE THAT IS STEPPED ON THE WAFER IS CORRECT AND HAS THE POSSIBILITY OF PRODUCING A "GOOD" DIE.

THE PRESENT

WHAT NEXT? ARE ALL THE PROBLEMS SOLVED? NOT BY A LONG SHOT. TODAY'S SEMICONDUCTOR MANUFACTURERS ARE FACING ONE OF THE MOST DIFFICULT CHALLENGES TO MANUFACTURING TECHNOLOGY THAT THEY HAVE ENCOUNTERED IN SEMICONDUCTOR HISTORY, AND IT IS DIRECTLY CONCERNED WITH PHOTOLITHOGRAPHIC SYSTEMS. THE REASON FOR THIS HURDLE LIES WITH PUSHING THE THEORETICAL LIMITS OF IMAGING SYSTEMS. LET'S TAKE A MINUTE TO REFRESH OURSELVES ON WHAT THOSE LIMITS ARE.

DUE TO THE WAVE NATURE OF LIGHT, IT IS NOT POSSIBLE TO CONSTRUCT AN OPTICAL SYSTEM WHICH CAN RESOLVE VERY SMALL FEATURES WITH HIGH FIDELITY. IF THE FEATURE SIZE BECOMES SMALL ENOUGH, THERE IS A POINT WHERE IT IS IMPOSSIBLE TO REPRODUCE THE FEATURE AT ALL. ALSO, IN GENERAL THE GREATER THE RESOLVING POWER OF A LENS SYSTEM, THE LESS TOLERANT IT IS TO FOCUS VARIATION.

WHILE THE EXACT LIMITS OF RESOLUTION ARE COMPLICATED MATHEMATICAL FUNCTIONS, A GOOD RULE OF THUMB IS:

A) THE SMALLEST FEATURE THAT CAN BE REPLICATED IN PRODUCTION USING PROJECTION OPTICS IS ABOUT 1 1/2 TO 2 TIMES THE WAVE LENGTH OF THE LIGHT.

B) THE DEPTH OF FOCUS FOR THIS TYPE OF SYSTEM IS ABOUT THREE TO FIVE WAVE LENGTHS OF LIGHT.

NOW LET'S LOOK AT THE CONSEQUENCE OF THESE STATEMENTS. TODAY, SEMICONDUCTORS ARE BEING DESIGNED WITH CIRCUIT DIMENSIONS WHICH ARE PUSHING AS NEAR THE ABSOLUTE LIMITS OF WHAT MODERN OPTICS CAN THEORETICALLY RESOLVE.

NOW THE CONSEQUENCE OF THIS PUSH TO FINER LINE WIDTHS CAUSES THE FAB LINE TECHNICIANS TO EITHER KEEP THE PHOTOLITHOGRAPHIC PROCESS TUNED TO PERFECTION OR THE IMAGE ON THE WAFER WILL NOT CONFORM TO THE DESIGN LIMITS. HERE WE HAVE AN ALMOST SOLID WALL KEEP PERFECT CONTROL OF THE PHOTOLITHOGRAPHIC PROCESS OR SWTICH TO A HIGHER RESOLUTION PRINTING TECHNIQUE SUCH AS X-RAY OR DIRECT WRITE E-BEAM.

TODAY, THE SEMICONDUCTOR MANUFACTURER HAS TREMENDOUS INCENTIVE TO PUSH THE PHOTOLITHOGRAPHY AS FAR AS IT CAN BE PUSHED. HIS FAMILIARITY WITH IT PERMITS OVERWHELMING COST

ADVANTAGES WHEN COMPARED TO ITS POTENTIAL REPLACEMENTS.

A GREAT DEAL OF INVESTMENT IS BEING MADE IN STEPPER LENS TECHNOLOGY AND RESIST TECHNOLOGY TO INCREASE THE RESOLVING POWER OF OPTICAL LITHOGRAPHY. IT IS EXPECTED THAT THIS TECHNOLOGY WILL PERMIT FEATURES AS SMALL AS 3/4 MICRONS (16 MEGABIT RAM TECHNOLOGY) TO BE PRINTED ON OPTICAL STEPPERS.

BUT WHAT ABOUT YIELD? WHAT WILL PUSHING THE THEORETICAL LIMITS OF THE PHYSICS DO TO CONSISTENCY IN PRODUCTION? AGAIN, THE ANSWER IS CLEAR--IF NO CHANGES IN THE CONTROL OF THE PROCESS ARE MADE--YIELDS WILL DROP LIKE A ROCK AS GEOMETRIES GET SMALLER. HOWEVER, IF SUITABLE MEASUREMENTS ARE TAKEN, AND THE INFORMATION IS FED BACK SO THAT IMMEDIATE PROCESS CHANGES ARE MADE IN REAL TIME BEFORE THE INEVITABLE PROCESS VARIATIONS EXCEEDS THEIR LIMITS, THEN PHOTOLITHOGRAPHIC YIELDS NEED NOT LIMIT THE FINAL DEVICE YIELD. ATTENTION CAN THEN BE PUT ONTO OTHER PARAMETERS IN THE PROCESS.

THE FOLLOWING IS A PARTIAL LIST OF THE PHOTOLITHOGRAPHIC PROPERTIES THAT WE WANT TO MEASURE:

- FOCUS
- MISALIGNMENT
- LINE SIZE
- DIRT OR PARTICULATES
- MASK PROBLEM/WRONG PATTERN/MISSING PATTERN
- RESIST NONUNIFORMITY
- UNDEVELOPED RESIST
- BRIDGING RESIST OR UNOPENED WINDOWS
- LIFTING RESIST
- METAL OR FILM DEPOSITION:
  - NONUNIFORMITY
  - THICKNESS VARIATION
  - PARTICLES OR CRACKING
  - RESIDUES
  - UNDER ETCH

HISTORICALLY, ALL VISUAL INSPECTIONS HAVE BEEN MADE BY OPERATORS STARING THROUGH MICROSCOPES AND REPORTING ON OUT-OF-LIMIT CONDITIONS. IF TOO MANY PROBLEMS WERE REPORTED, THEN THE WAFER OR LOT OF WAFERS WERE REWORKED OR DISCARDED. NO ATTEMPT HAS BEEN MADE TO USE THESE INSPECTION RESULTS AS PART OF A CONTROL LOOP TO STABLIZE THE PROCESS.

TODAY INDUSTRY HAS NO CHOICE--THE PROCESS CONTROL FEEDBACK LOOP MUST BE CLOSED. OVER THE NEXT FIVE YEARS, IMAGE PROCESSING WILL IMPROVE THE PHOTOLITHOGRAPHY ON THE WAFER AND IMPROVE THE RESULTS ON WAFERS IN THE SAME MANNER AS PHOTOMASK QUALITY WAS IMPROVED OVER THE PAST FIVE YEARS.

RECOGNIZING THE IMPENDING INDUSTRY PROBLEM, WE SET TO WORK ON A SYSTEM OF WAFER INSPECTION. THIS SYSTEM, THE KLA 2020 INTRODUCED IN THE PAST YEAR, PROVIDES EXHAUSTIVE CHARACTERIZATION IN ORDER TO SIGNIFICANTLY IMPROVE PROCESS CONTROL.

THIS SYSTEM IS THE FIRST OF A FAMILY OF SYSTEMS DESIGNED TO AUTOMATE WAFER INSPECTION. NUMEROUS BENEFITS ARE BEING OBTAINED BY THE FIRST USERS. THIS WILL ENABLE EFFECTIVE FEEDBACK TO BE APPLIED TO THE PROCESS TO ENABLE REPAIR OR ADJUSTMENT OF PROCESS EQUIPMENT AND PARAMETERS TO OBTAIN CONSISTENTLY HIGH YIELDS. BY STATISTICAL SAMPLING, AND WITH PRECISE MEASUREMENTS, PROCESS CHANGES CAN BE DETECTED. THE CONSEQUENCES OF THOSE CHANGES CAN BE PROJECTED AND ACTION TAKEN TO AVOID THE ADVERSE CONSEQUENCES.

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DIRECTIONAL TRENDS AT A TIME EARLY ENOUGH TO COMPENSATE. THE THRUST IS TO OPTIMIZE PRODUCTIVITY, YIELD, AND THROUGHPUT WITH A MINIMUM INVENTORY INVESTMENT THROUGH THE CONTROLLED OPTIMIZATION OF PRODUCTION OF PRODUCTION PARAMETERS. THE INSPECTION SYSTEM IN LITHOGRAPHY STANDS AT THE HEART OF THE PRODUCTION SEQUENCE AND SHOULD THEREFORE BE EXPECTED TO MONITOR NOT ONLY THE CONTROLS WITHIN LITHOGRAPHY BUT ALSO THE FULL VARIABLE SET DESCRIBING THE CLEANROOM.

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EQUIPMENT AND MATERIALS FRONTIERS

Robert McGeary
Director
Semiconductor Equipment and Materials Service
Dataquest Incorporated

Mr. McGeary is Director of Dataquest's Semiconductor Equipment and Materials Service. He was previously a Senior Industry Analyst for Dataquest's Semiconductor Industry Service and was responsible for the Industry and Technology portion of that service. Before joining Dataquest, he was Product Marketing Manager at Applied Materials, Inc., where he managed the worldwide product marketing activities for the Dry Etch Division and managed product support for the European dry etch business. Before that, he worked as Product Marketing Manager at GCA Corporation/IC Systems Group, as an Accelerator Physicist at Lawrence Berkeley Laboratories, as a Nuclear Engineer at Mare Island Naval Shipyard, and as a Reactor Operator at the University of Washington. He received a B.S. degree in Physics and Mathematics from the University of Washington and an M.B.A. degree from St. Mary's College.

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SEMICONDUCTOR EQUIPMENT AND MATERIALS INDUSTRY SERVICE CONFERENCE
October 14-16, 1985
Tucson, Arizona

EQUIPMENT FONTIERS
ANNUAL FORECAST

Robert McGeary

Director,
Semiconductor Equipment
and Materials Service

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ESTIMATED WORLDWIDE CAPITAL SPENDING

(Millions of Dollars)

REGION	1984	1985	1990	CAGR
U.S.	$3,051	$2,323	$5,290	9.6%
JAPAN	3,460	2,664	6,676	11.6%
EUROPE	450	425	1,241	18.4%
ROW	701	220	810	26.1%
CAPTIVES	582	511	1,164	12.3%
TOTAL	7,162	5,632	13,600	11.9%

Source: DATAQUEST

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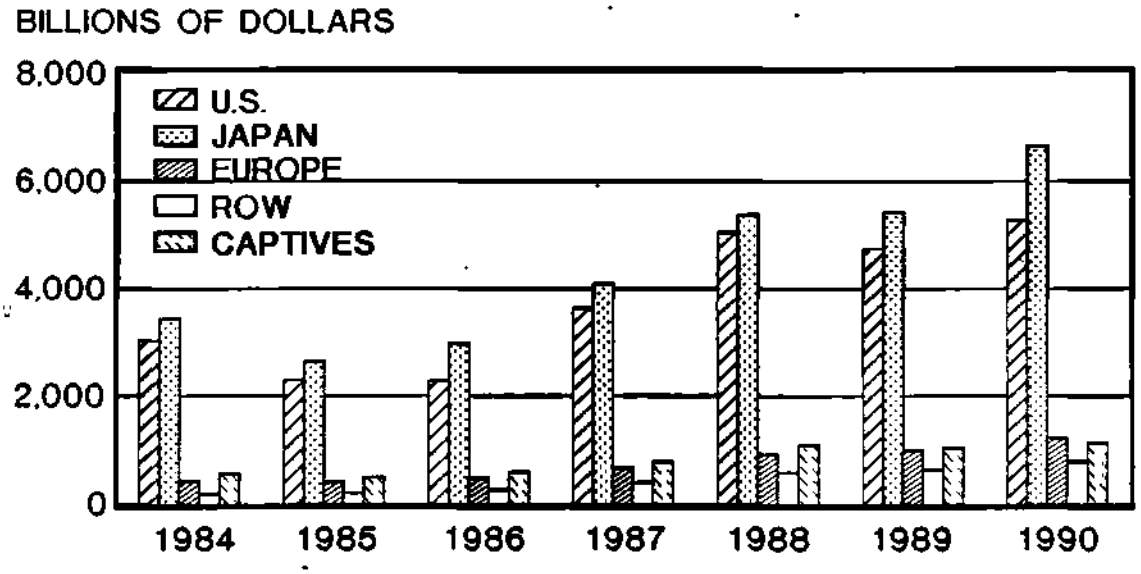
ESTIMATED CAPITAL SPENDING--WORLDWIDE

1984-1990



Source: DATAQUEST

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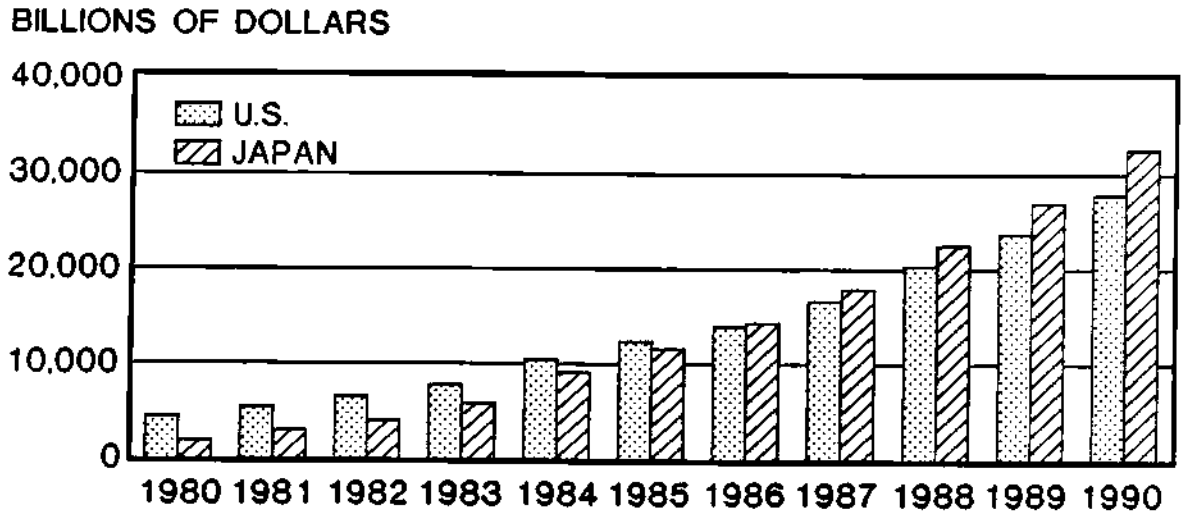
ESTIMATED INSTALLED BASE--
U.S. VS. JAPAN

PROPERTY, PLANT, AND EQUIPMENT



Source: DATAQUEST

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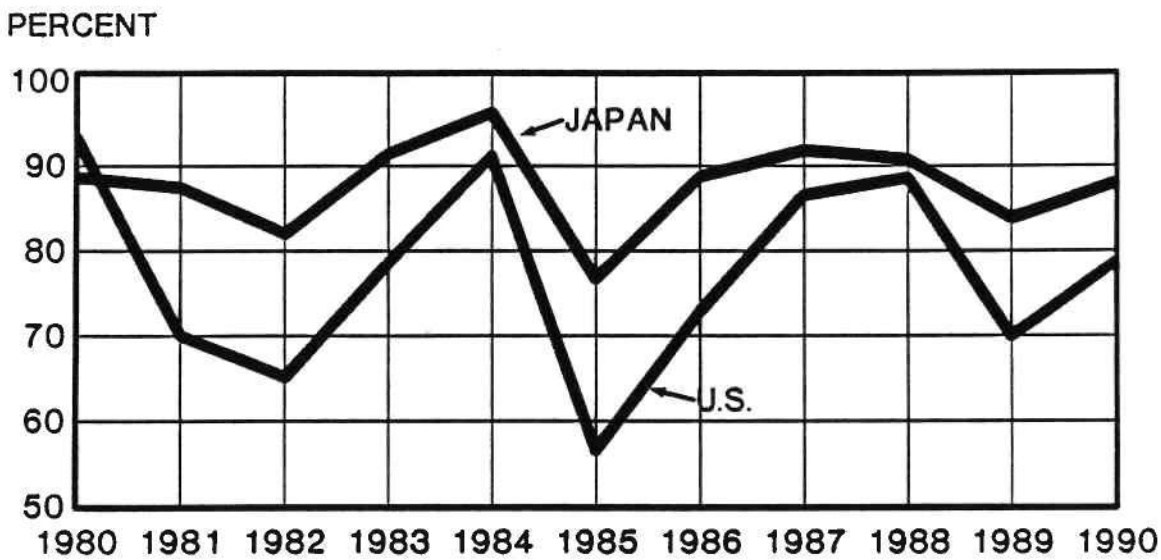
ESTIMATED CAPACITY--TWO CULTURES

U.S. VS. JAPANESE CAPACITY UTILIZATION



Source: DATAQUEST

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ESTIMATED SALES OF LITHOGRAPHY EQUIPMENT

(Millions of Dollars)

TYPE	1984	1985	1990	CAGR
PROXIMITY	$ 77	$ 47	$ 45	(8.5)
PROJECTION	245	192	307	3.8
1X STEPPER	65	55	126	11.7
REDUCTION STEPPER	545	466	1,154	13.3
DW E-BEAM	3	25	110	95.0
X-RAY	2	4	70	80.9
TOTAL	$937	$789	$1,812	11.6

Source: DATAQUEST

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LITHOGRAPHY

SYSTEM	APPLICATION
PROXIMITY/CONTACT	GaAs
PROJECTION STEPPER	1MB DRAM
	4MB DRAM
REDUCTION STEPPERS	1MB DRAM
	4MB DRAM
1X STEPPERS	1MB DRAM
	4MB DRAM
X-RAY	4MB DRAM
	16MB DRAM
DW E-BEAM	ASICs, GaAs
LASER PG	ASICs

Source: DATAQUEST

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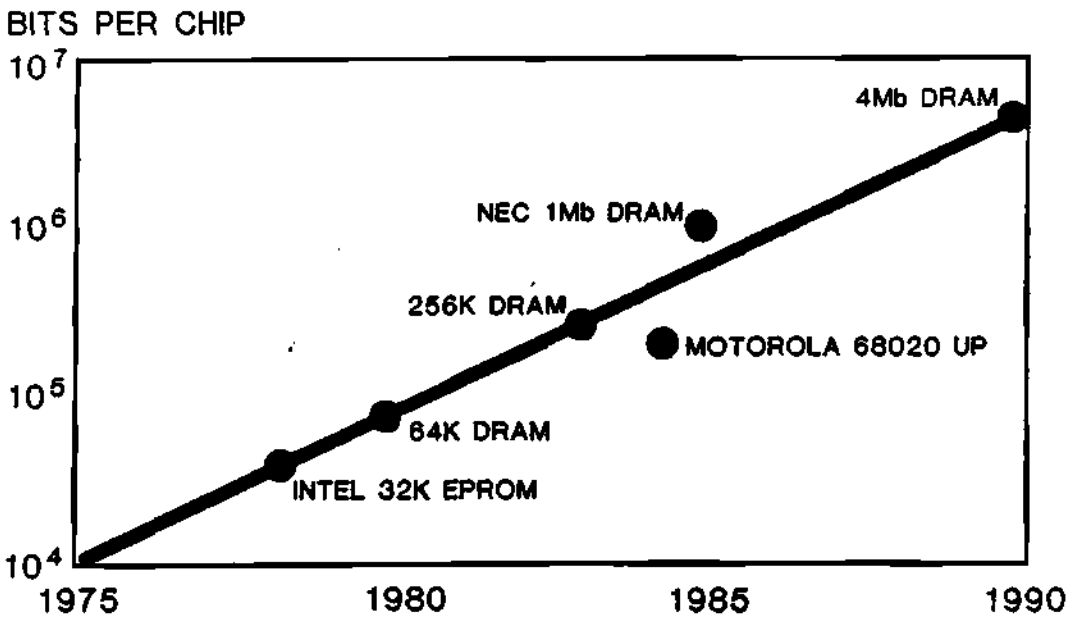
PRODUCT INTRODUCTIONS



Source: DATAQUEST

ESTIMATED SALES OF ETCH EQUIPMENT

(Millions of Dollars)

TYPE	1984	1985	1990	CAGR
WET	$ 79	$ 56	$ 73	(1.3%)
BARREL	44	33	56	4.2%
PLANAR	304	246	631	13.0%
ION MILLING	18	15	13	(4.9%)
TOTAL	$445	$350	$774	9.7%

Source: DATAQUEST

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ESTIMATED SALES OF AUTOMATIC PHOTORESIST EQUIPMENT

(Millions of Dollars)

TYPE	1984	1985	1990	CAGR
TRACK	$144	$109	$202	5.8%

Source: DATAQUEST

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ESTIMATED SALES OF DEPOSITION EQUIPMENT

(Millions of Dollars)

TYPE	1984	1985	1990	CAGR
CVD	$245	$194	439	10.2%
PVD	300	233	481	8.2%
EPITAXY	140	110	236	9.1%
TOTAL	$685	$537	$1,156	9.1%

Source: DATAQUEST

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MOS ON EPITAXY

ADVANTAGES

- ALLOWS TIGHTER DESIGN SPECIFICATION
- PREVENTS LATCH-UP ON CMOS

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CMOS ON EPITAXY

ALTERNATIVES

- PROCESS CONTROL
- ON-CHIP BIAS GENERATOR
- HIGH-VOLTAGE IMPLANT
- NMOS

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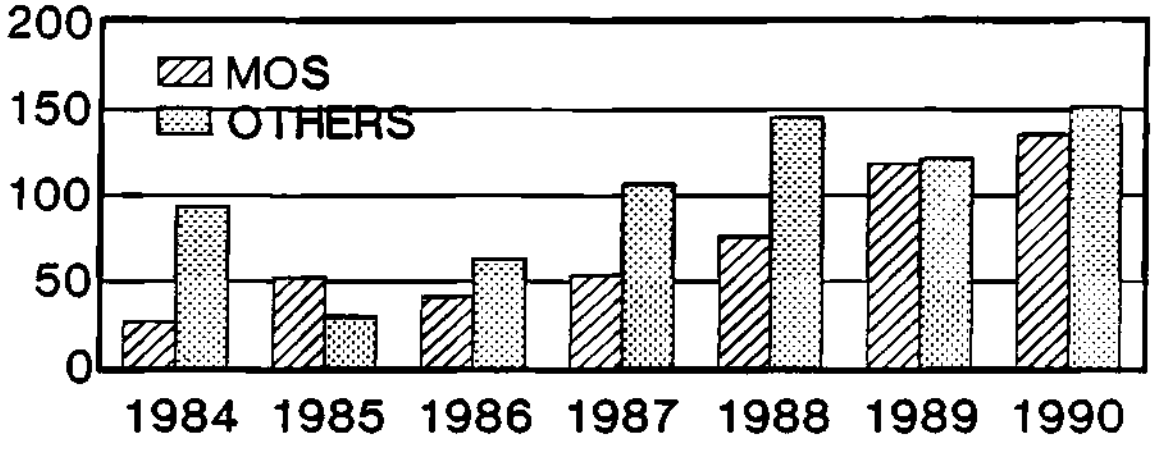
EPITAXY

FORECAST DEMAND
(MOS VS. OTHER)

MILLIONS OF DOLLARS



Source: DATAQUEST

ESTIMATED SALES OF DOPING EQUIPMENT

(Millions of Dollars)

TYPE	1984	1985	1990	CAGR
FURNACE	$150	$110	$156	0.6%
ION IMPLANT	297	239	598	12.4%
TOTAL	$447	$349	$754	9.1%

Source: DATAQUEST

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ION IMPLANTATION

EMERGING APPLICATIONS

APPLICATIONS	ENERGY
SHALLOW JUNCTIONS	<5 keV
CLUSTER BEAM	1 TO 10 eV PER ION
OXYGEN IMPLANT	>200 keV (10^{18} ION/CM^2)
BURIED LAYER	>3 MeV
RETROGRADE WELL	>1 MeV
ROM PROGRAMMING	>1 MeV

Source: DATAQUEST

ION IMPLANTATION FORECAST DEMAND

(Millions of Dollars)

TYPE	1984	1985	1990	CAGR
MEDIUM CURRENT	$140	$117	$203	6.4%
HIGH CURRENT	157	126	329	13.1%
HIGH VOLTAGE	5	5	75	57.0%
TOTAL	$302	$248	$607	12.3%

Source: DATAQUEST

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ESTIMATED SALES OF INSPECTION AND CAM EQUIPMENT

(Millions of Dollars)

TYPE	1984	1985	1990	CAGR
INSPECTION	$350	$290	$832	15.5%
CAM	52	49	281	32.5%

Source: DATAQUEST

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EQUIPMENT FORECAST SUMMARY

TYPE	1984	1985	1990	CAGR
LITHOGRAPHY	$ 936	$ 796	$1,827	11.8%
ETCH	445	350	774	9.7%
AUTO PR	144	109	202	5.8%
DEPOSITION	685	536	1,155	9.1%
DOPING	447	350	754	9.1%
INSPECTION	350	290	832	15.5%
CAM	52	49	281	32.5%
TOTAL	$3,059	$2,480	$5,825	11.3%

Source: DATAQUEST

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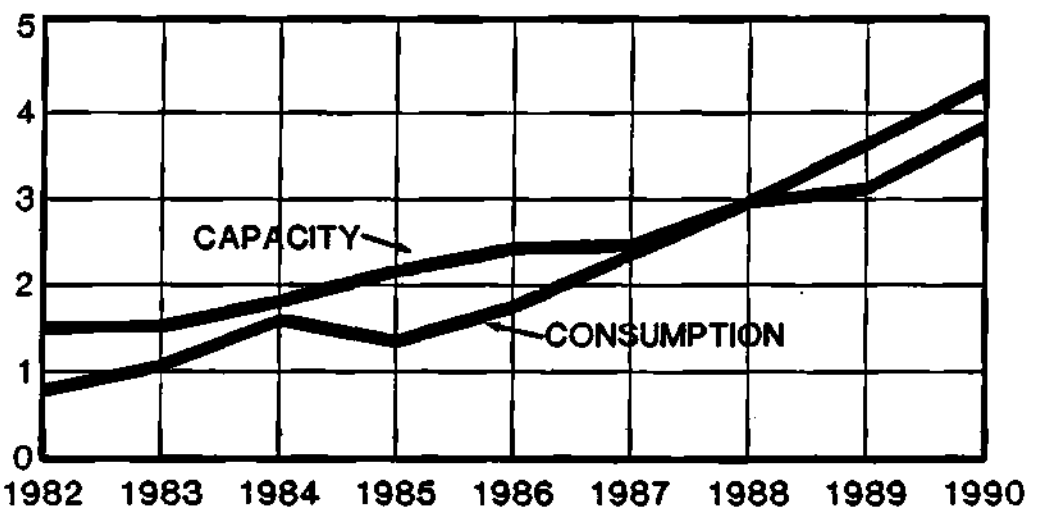
POLYSILICON--ESTIMATED SUPPLY VS. DEMAND

1984-1990



Source: DATAQUEST

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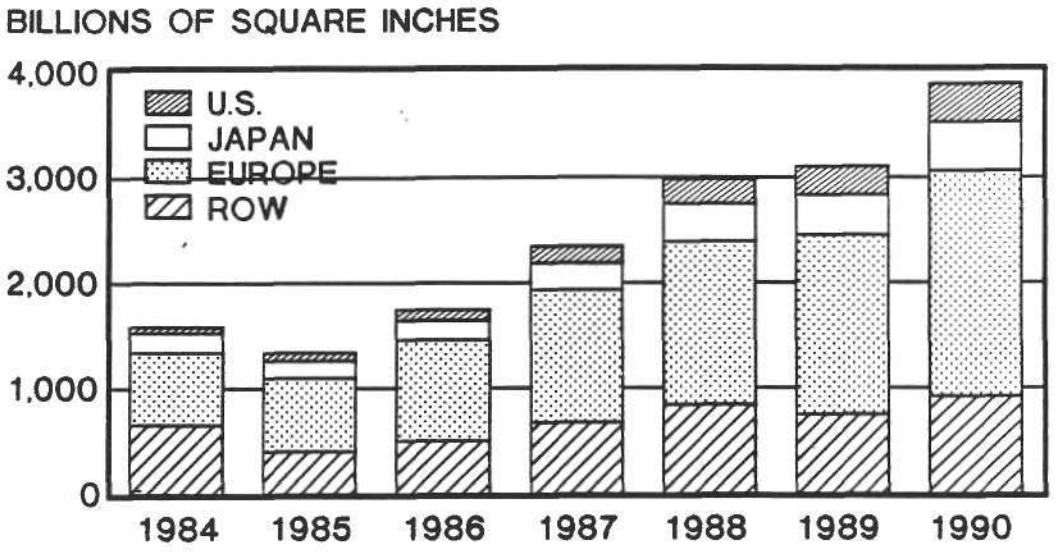
SILICON PROCESS PRODUCTIVITY

ESTIMATED WORLDWIDE CONSUMPTION



Source: DATAQUEST

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OUTLOOK

- EQUIPMENT WILL GROW LESS THAN SEMICONDUCTOR REVENUE
- AUTOMATION AND INSPECTION ARE PARAMOUNT
- MATERIALS AND CHEMICALS ARE PARAMOUNT
- FAB AND EQUIPMENT CLEANLINESS ARE PARAMOUNT
- VERTICAL INTEGRATION IS PARAMOUNT

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SILICON COMPILERS

A panel session on the strategic role of
silicon compilers in designing ASICs

Monday, October 14, 2:00 p.m. to 3:30 p.m.

An emerging group of young companies is challenging some of the more conventional design methods used in the ASIC industry today. Silicon compiler systems were once used only in the most advanced research laboratories. But that is changing. DATAQUEST believes that the emergence of silicon compilers will have a profound impact on the growth of the ASIC markets and that by the end of the decade, they will be the vital tools that will make standard cell and other cell-based markets exceed $2 billion. There will also be a dramatic shift within the design community. What was once the exclusive domain of the IC design engineer is expected to widen to include a very large base of systems engineers. Supporters of the silicon compiler approach believe that the design time can be reduced to a matter of days while at the same time offering area efficiencies approaching handcrafted designs. They also believe that silicon compiler technology can be ultimately used to design far more complex chips than were previously considered practical.

This panel session is composed of semiconductor suppliers and CAD tool makers. Each company has a unique perspective on the role of silicon compilers, and the panel members will present their views on the critical issues that will impact the ASIC industry.

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George W. Cone

Mr. Cone is a Senior Vice President at Seattle Silicon Inc. (SSI) and his career spans 27 years of experience in both bipolar and MOS technology. He holds seven patents that range from semiconductor processing to electrostatic printers. Before joining SSI, he was President and Chief Executive Officer of a start-up called Array Devices Inc. Mr. Cone was also one of the founders of Applied Micro Circuits Corporation, where he held the title of Vice President of Operations and Marketing. During his tenure at Garrett Corporation's Micro Components Division, he was instrumental in growing sales to $50 million.

Walter P. Curtis III

Mr. Curtis is Vice President of Marketing at Silicon Compiler Inc. (SCI). He joined SCI after ten years with National Semiconductor where he was Director of Marketing for the Microprocessor Group. During his tenure at National, he introduced the NS 32000 family of microprocessors and before that he held various management positions in both strategic marketing and field applications engineering. Mr. Curtis has also worked as a design engineer for Addressograph-Multigraph Corporation and was the primary developer of one of the first microprocessor-based, point-of-sale, and transaction processing systems for the banking, travel, and entertainment industries.

Douglas G. Fairbairn

Mr. Fairbairn is the Vice President of Design Technology at VLSI Technology Inc. (VTI). He was a founder of VTI in 1980, and is currently responsible for all IC design tool development, marketing, and support. Before founding VTI, he was founder and publisher of VLSI Design Magazine, which was sold to CMP Publications in 1983. Mr. Fairbairn was with Xerox Palo Alto Research Center from 1972 until 1980. While at Xerox, he served as Architect Project Manager for the development of the first 16-bit portable computer and for an advanced office terminal system.

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Richard N. Gossen Jr.

Mr. Gossen is President and Chief Executive Officer of Silicon Design Labs and his perspective comes from 17 years in the semiconductor industry. He spent 16 years with Texas Instruments (TI), where he participated in some of the early microprocessor development of the late 1960s. More recently, he was responsible for all MOS memory development at TI, including the 64K DRAM. Mr. Gossen joined Environmental Processing Inc. (EPI) in 1983 as Vice President of Business Development. At EPI he participated in the rapid growth that led to a successful initial public offering in July 1984.

Michael L. Hackworth

Mr. Hackworth is President and Chief Executive Officer of Cirrus Logic Inc., and has more than 20 years of experience in the semiconductor industry. As Senior Vice President at Signetics, Mr. Hackworth directed three product divisions, an MOS Technology Development Unit, the Albuquerque MOS Manufacturing Plant, and a total of more than 2,500 employees. In 14 years at Signetics, Mr. Hackworth's achievements included developing the bipolar digital marketing effort and directing and staffing the company's successful entry into MOS technology. He also has held a variety of marketing and sales positions at Motorola and Fairchild.

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Where are semiconductors going?

AN INDUSTRY TRANSITION:
AN APPLICATION MARKET PERSPECTIVE

A Presentation and Workshop

Monday, October 14, 2:00 p.m. to 3:30 p.m.

As semiconductor devices and technology have become more complex, so too have the variety of applications for which these devices are used. For many years, decision makers in the semiconductor industry have grappled with the question, Where are semiconductors going? This year, a fundamental industry transition has made the question more crucial.

DATAQUEST's Semiconductor Application Markets (SAM) service is sponsoring this workshop to more fully examine semiconductor industry trends and issues from an application market perspective. The workshop will begin with an overview of this perspective, followed by an explanation of the research methodology SAM uses to tackle the end-use question. Topics to be discussed include:

- Historical company electronic equipment revenues and their relation to semiconductor consumption
- North American electronic equipment forecasts
- Semiconductor consumption by application market
- Major merchant market buyers
- Forecast and trend information on key equipment industries as identified by other DATAQUEST technology services
- 1986 procurement outlook--What are key buyers saying?

We will have a question-and-answer period following the presentation. Staff members from our European and Japanese Semiconductor Industry Services will be joining us to discuss end use from a worldwide perspective.

We invite you to attend and look forward to an interesting and insightful afternoon.

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October 14-16, 1985
Tucson, Arizona

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If you had a billion transistors what would you do with them?

THE BILLION TRANSISTOR VLSI ARCHITECTURE

A Panel Session on future microprocessor and VLSI architectures

Tuesday, October 15, 2:00 p.m. to 3:30 p.m.

Scientists have predicted that integrated circuits with a billion transistors using current or foreseeable semiconductor manufacturing technology will be possible by the end of the century. The theoretical feature size of 0.2 to 0.4 micron will require a transition from the present optical lithography to more advanced microlithography techniques such as e-beam and X-ray. This transition in device technology will demand an equally significant transition in the application and functional design of such circuits. Given the assumption that this device density will indeed happen, the industry is faced with the perplexing problem of how to use vast numbers of devices effectively on a single die.

The catalyst for this session, "The Billion Transistor VLSI Architecture," was a paper titled "Ultra-Large Scale Integration," by Professor James D. Meindl of Stanford University. (James D. Meindl, "Ultra-Large Scale Integration," IEEE Transactions on Electron Devices, vol. ED-31, No. 11, Nov. 1984.) This topic will be addressed by a panel of industry experts who have experience with integrated circuit or system design. Each panel member has been asked to accept the premise that a billion transistors will be possible and then propose device architectures that will utilize such levels of integration.

Each of the following panel members will give his views of future integrated circuits that will require such integration.

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Stanley Mazor

Mr. Mazor is the Director of Applications Engineering at Silicon Compilers. Previously, he was with Intel Corporation for 15 years, where he worked on the design and specification of all of Intel's early microprocessors. He shares patents on the CMS-4 and 8080 microprocessors. He has also worked on the design of 7 VLSI chips as well as several small systems using VLSI circuits.

John Banning

Mr. Banning was Vice President for software development at Gavilan Computer Corp., where he was in charge of all software development. Before that, he was manager of component architecture at Zilog Inc., where his group designed the architecture of Zilog's new 32-bit microprocessor, the Z80,000 as well as the Z8070 floating point co-processor. Prior to that, he was Senior Computer Architect at Amdahl Corporation, where he participated in the design and construction of a software performance language, compiler, and system. He also worked on an advanced computer architecture design project.

Skip Stritter

Mr. Stritter is Vice President of Engineering and a co-founder of MIPS Computer Systems. Before that, he was Director of Future Products at Nestar Systems, where he was responsible for two generations of local area networks. Previously he was with Motorola, where he was the Chief Architect of the Motorola 68000 and implemented the 68000 Pascal compiler. During his tenure at Motorola, he was an Adjunct Professor of Computer Sciences at the University of Texas.

Dan Ling

Mr. Ling is Manager of Microsystems at the IBM Thomas J. Watson Research Center. He is involved with VLSI designs for display applications, computer-aided design tools, and high-performance microcomputer systems.

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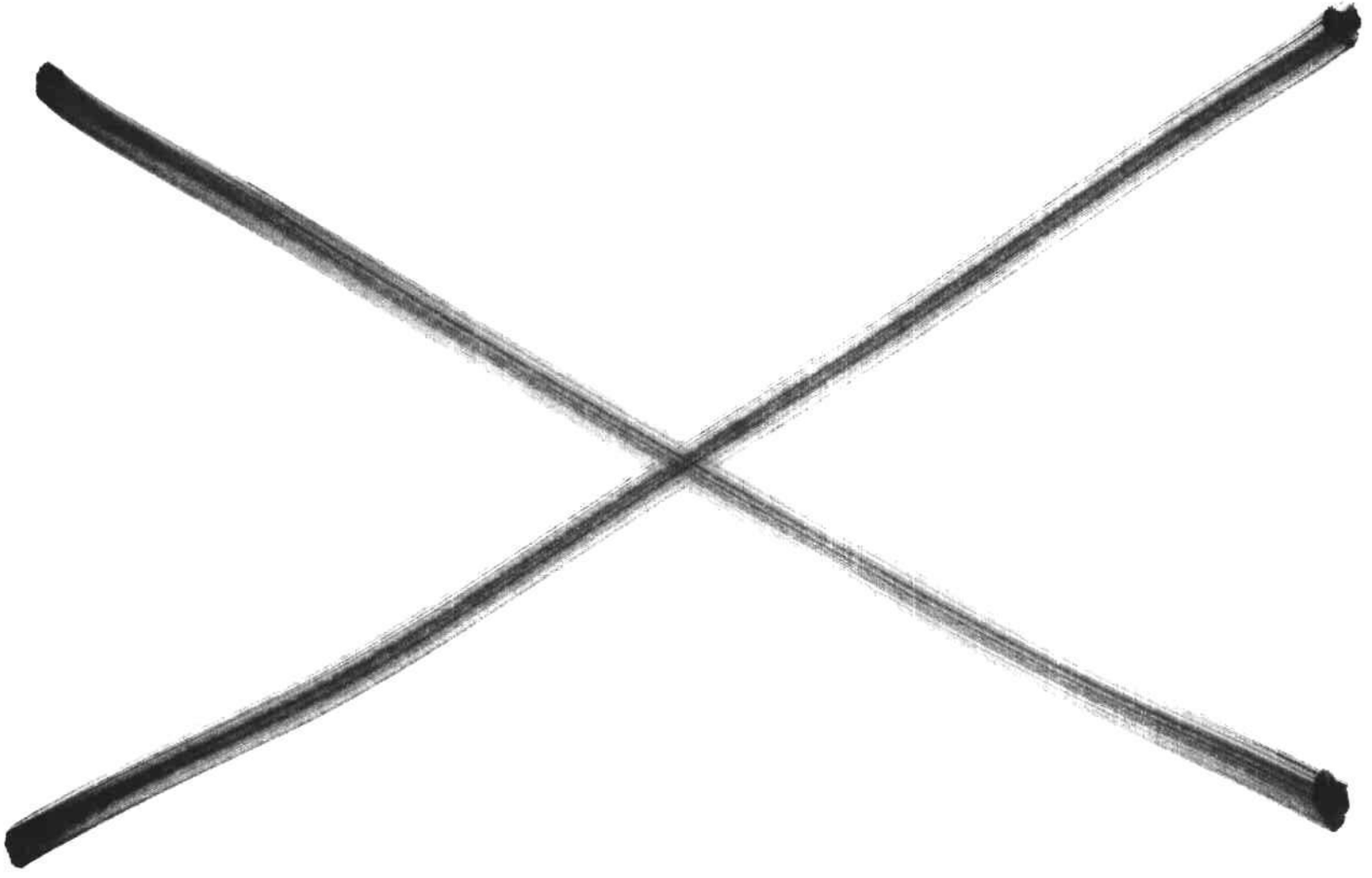

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NEW OPPORTUNITIES IN SEMICONDUCTORS

David L. House
Vice President and General Manager
Microcomputer Group
Intel Corporation

Mr. House is Vice President and General Manager of the Microcomputer Group at Intel Corporation. Previously, he held management positions in applications, product marketing, marketing, and general management at Intel. Most recently, he was General Manager of Intel's Microprocessor and Development Systems Division. Prior to that, he worked for Raytheon, Honeywell, and Microdata. Mr. House received a B.S. degree in Electrical Engineering from Michigan Technological University and an M.S. degree in Electrical Engineering from Northeastern University in Boston, Massachusetts. He also completed course requirements for a doctorate in Computer Science from Worcester Polytechnic Institute in Massachusetts.

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THIS PRESENTATION WAS NOT AVAILABLE AT PUBLICATION TIME.

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October 14, 15, and 16, 1985
Tucson, Arizona

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AN INDUSTRY IN TRANSITION

Alex Au
President and CEO
Vitelic Corporation

Dr. Au is the founder and President of Vitelic Corporation. Previously, he was VLSI Research Manager at Fairchild Semiconductor where he managed the design and manufacturing of a 64K CMOS static RAM, a 16K NMOS EEPROM, and a 64K NMOS dynamic RAM. Prior to that, he was R&D Director at Intersil, a Senior Design Engineer at Fairchild Semiconductor, and a Senior Design Engineer at Hewlett-Packard. He holds four patents on MOS memory circuits. Dr. Au received a B.S. degree in Electrical Engineering from the University of California at Los Angeles, and an M.S. degree and a Ph.D. in Electrical Engineering from Stanford University.

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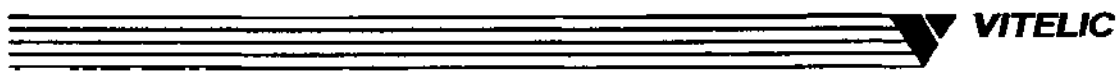
APPLICATION SPECIFIC MEMORIES
THE NEW MEMORY MARKET

Alex Au
President & C.E.O.
Vitelic Corporation



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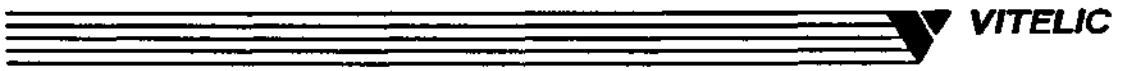
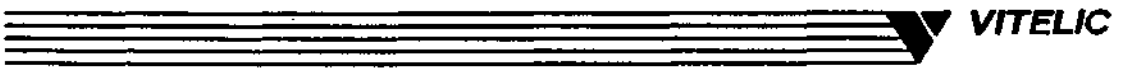
- *The New Memory Market*
- *Products and Applications*
- *Participating in the Market*



FACTORS AFFECTING THE NEW MEMORY MARKET

- *CMOS*
- *Market Fragmentation*
- *Manufacturing Capability*



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CMOS

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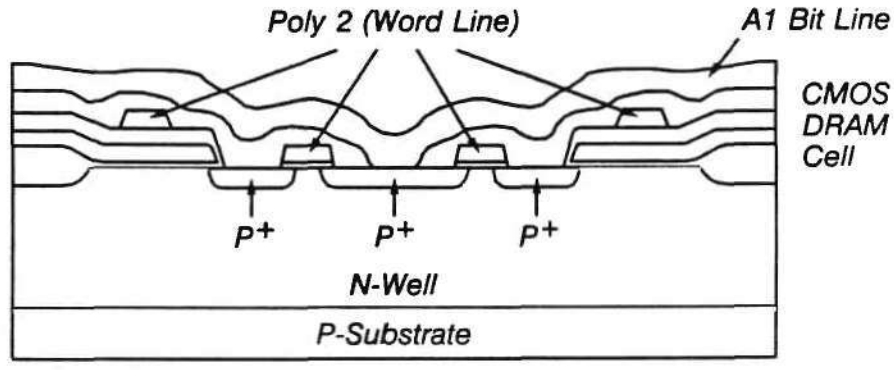
256K DRAM MEMORY CELL
P-Substrate



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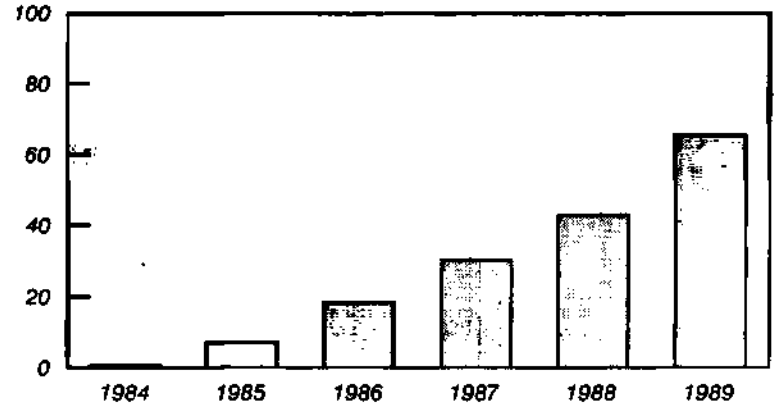
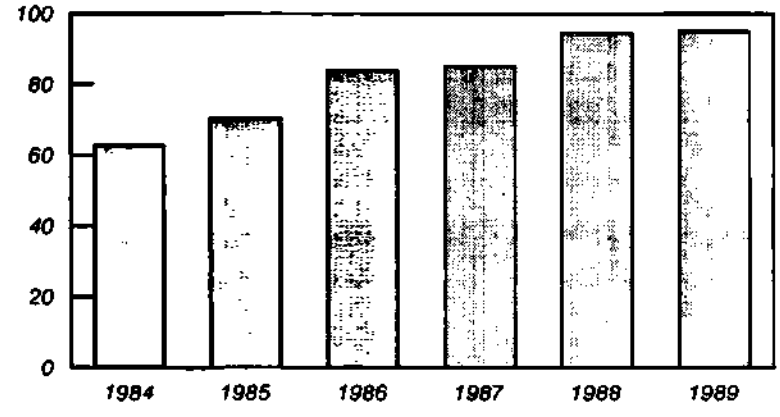
CMOS DRAMS
As a Percentage of Total Dollars



Source: DATAQUEST

VITELIC

CMOS SRAMS
As a Percentage of Total Dollars



Source: DATAQUEST

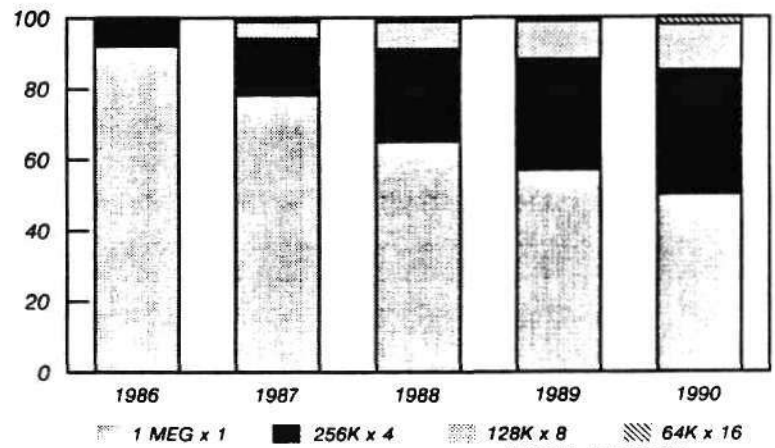
VITELIC

MARKET FRAGMENTATION

Source: DATAQUEST

VITELIC

1 MEGABIT DRAMS, BY ARCHITECTURE
Organization As Percentage of Total Dollars



Source: DATAQUEST

VITELIC

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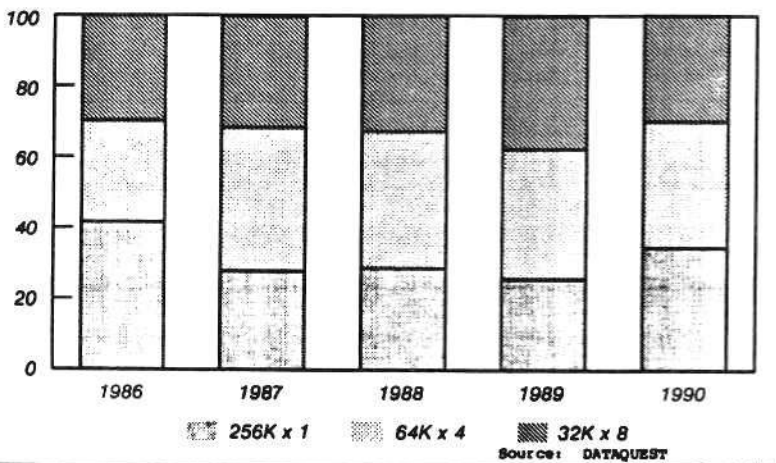
256K SRAMS, BY ARCHITECTURE
Percentage of Total Dollars



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MANUFACTURING

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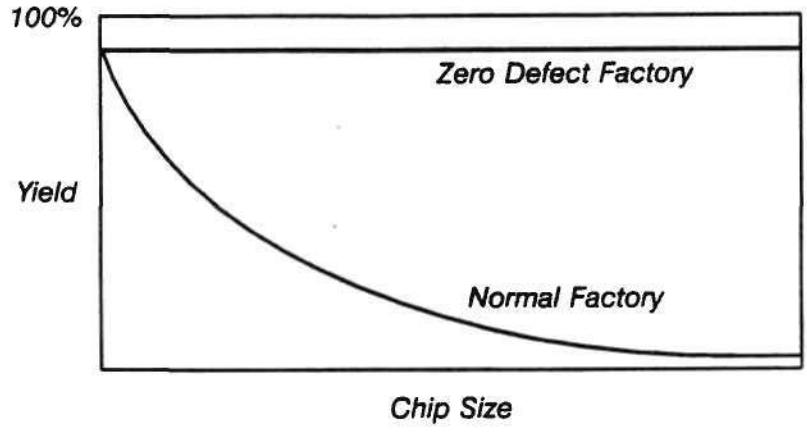
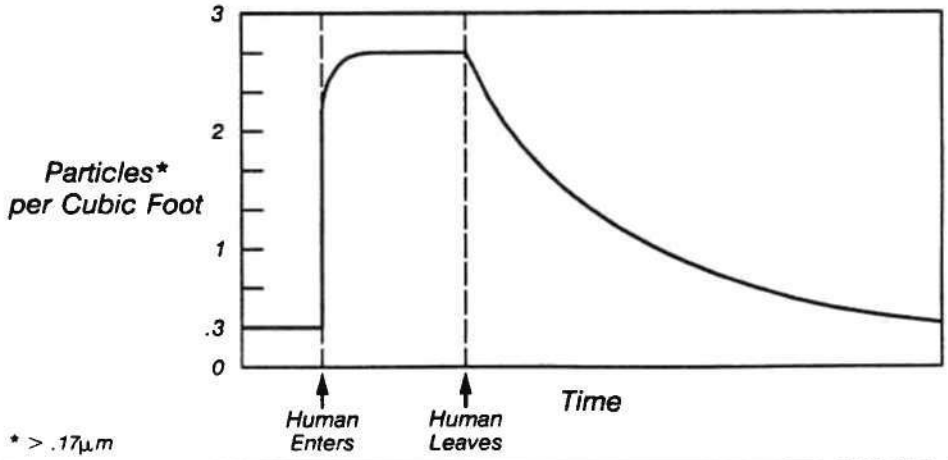
YIELD VS. CHIP SIZE



VITELIC

EFFECT OF HUMAN PRESENCE ON CLEAN ROOM ENVIRONMENT



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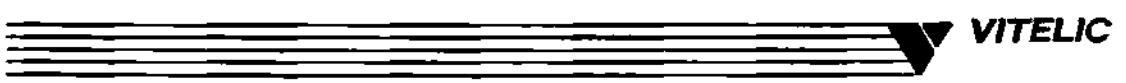
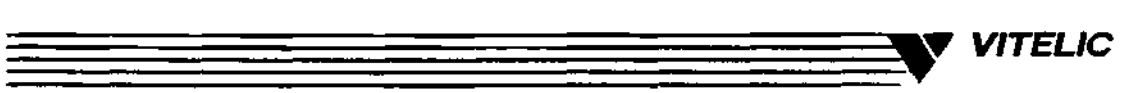
CLEAN ROOM DYNAMIC DUST LEVEL
(Particles Per Cubic Foot)

Active Area (Super Clean Room)	
▼ *Before Entering*	*Average 0.3*
▼ *Before Leaving*	*2 - 3*
Maintenance Area	
▼ *Before Entering*	*2 - 28*
▼ *Before Leaving*	*35 - 85*
Operator Area	
▼ *No Person Near the Measuring Point*	*96 - 140*
▼ *Person Near the Measuring Point*	*160 - 317*



APPLICATION SPECIFIC MEMORY



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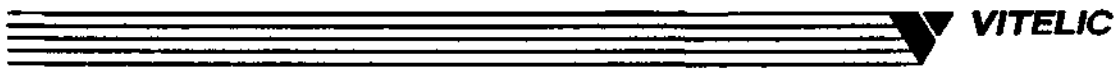
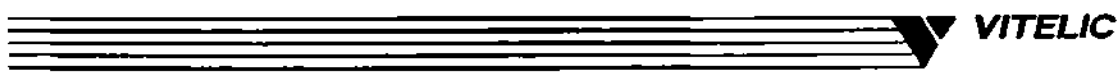
POTENTIAL NEXT-GENERATION PRODUCTS



1 MEGABIT VIDEO RAM FOR DIGITAL TELEVISION

- *Frame Storage May Require One to Four Megabits per Frame*
- *Device Will Have High Speed Logic Functions For Data Processing Before Display*
- *2 High Speed Serial Access Ports*



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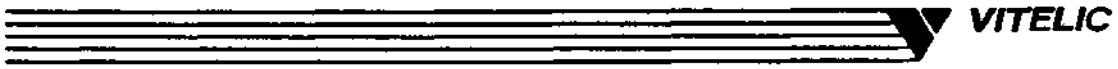
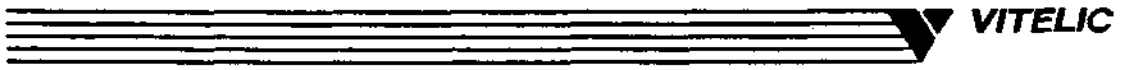
SUPER HIGH SPEED DUAL PORT SRAM

- *2K x 8 to 8K x 8 Required for Buffer Memory Applications*
- *25 nS Access Time*
- *On-Board Anti-Contention Logic*



CONTENT ADDRESSABLE MEMORY FOR ARTIFICIAL INTELLIGENCE APPLICATIONS

- *Fast Search and Match*
- *Large Memory*
- *Logic Capability*
  - *Compare*
  - *Exclusive or*
  - *Invert*



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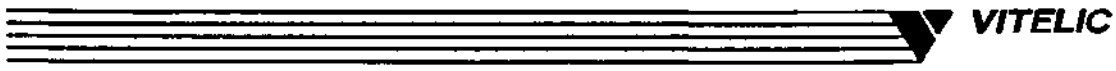
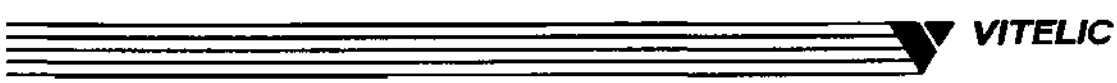
SUPER LOW STANDBY POWER DRAMs FOR SEMICONDUCTOR DISK APPLICATIONS

- *High Density, Low Cost DRAM*
- *Serial and Random Access*
- *Battery Back-Up*
- *Special Packaging*



MEMORY FOR HIGH TEMPERATURE APPLICATIONS

- *150 to 200 Degree Celcius Operation*
- *Designed to Compensate for High Leakage and Vt Reduction at High Temperatures*



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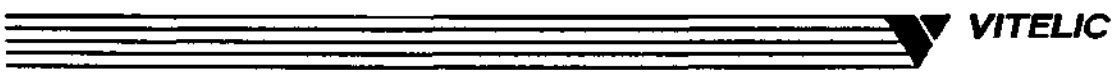
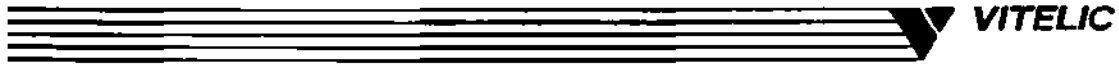
SUPER RELIABLE MEMORIES

- *Organized x9*
- *Internal Error Checking and Correction*
- *On-Chip Functions to Ease Addition of External Error Checking and Correction*



THE CHALLENGE OF THE NEW MEMORY MARKET



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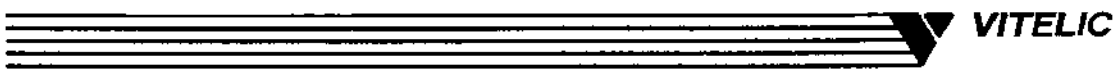
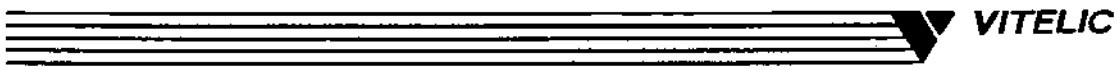
THE CHALLENGES

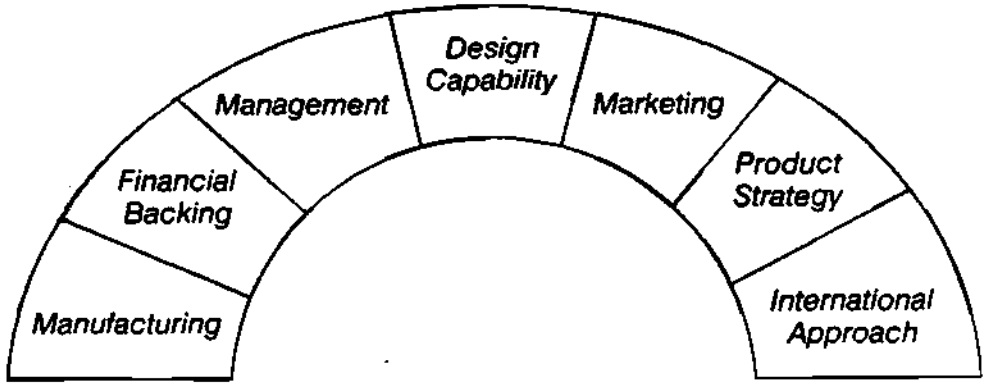
- *Trend to CMOS*
- *Fragmentation of the Market*
- *Manufacturing*



SUCCESSFULLY PARTICIPATING IN THE NEW MEMORY MARKET



BUILDING BLOCKS OF SUCCESS



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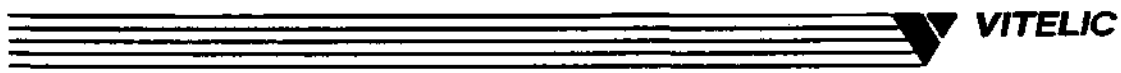
CONCLUSIONS



ASIC's IN THE ANALOG WORLD

Alan B. Grebene

President

Micro Linear Corporation

San Jose, California

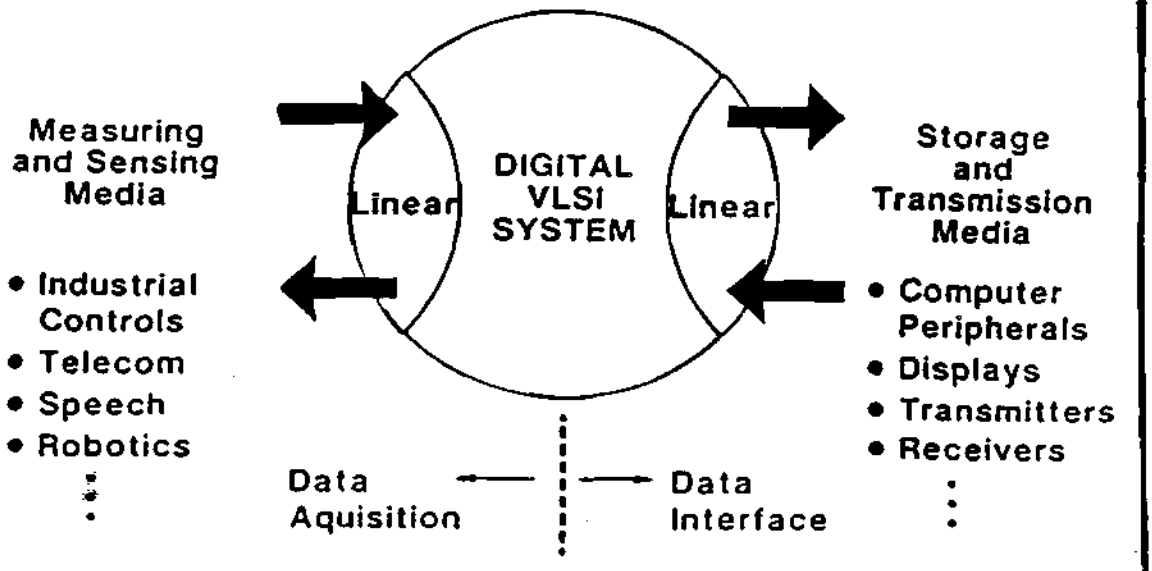
PRESENTED AT

DATAQUEST SEMICONDUCTOR INDUSTRY CONFERENCE

OCTOBER 14-16, 1985

TUCSON, ARIZONA

SYSTEMS IN THE ANALOG WORLD



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TRENDS IN THE LSI WORLD

1 — INCREASING COMPLEXITY:

Component ⟶ Subsystem ⟶ Complete System

2 — SPECIALIZED APPLICATIONS:

Increasing Complexity ⟶ Reduced Versatility (Specialized Applications)

Specialized Applications ⟶ ASIC Solutions

3 — SYSTEM—LEVEL INTEGRATION:

System-on-a-Chip ⟶ Linear/Digital Mix

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IN CUSTOM LSI DESIGN

THREE CRITICAL FACTORS ARE:

- Design Time
- Design Cost
- Design Talent

Micro Linear

LIMITED DESIGN TALENT

- There are over 250,000 Systems Designers, worldwide
- There are less than 250 Expert Linear LSI Designers in the world

RESULT:

There is less than one Linear LSI Expert for every 1000 Systems Designers!

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SOLUTION

Simplify and Automate Custom LSI Design through:

- NEW DESIGN CONCEPTS
  Semicustom
  Modular Design
- NEW CAD TOOLS

This has been done successfully in Digital LSI.
It has not been done in Linear LSI.

Micro Linear

THE PROBLEM

Traditionally Linear LSI circuits are designed at the individual transistor/resistor level.

This approach has the following limitations:

- It requires an Expert LSI Designer
- No two designs are alike
  Each design has to be individually "hand—crafted"

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DIFFICULTIES OF ANALOG LSI DESIGN

- Difficult to specify
- Difficult to simulate
- Difficult to interface
- Sensitive to chip layout
- Difficult to test

Therefore: Difficult to automate

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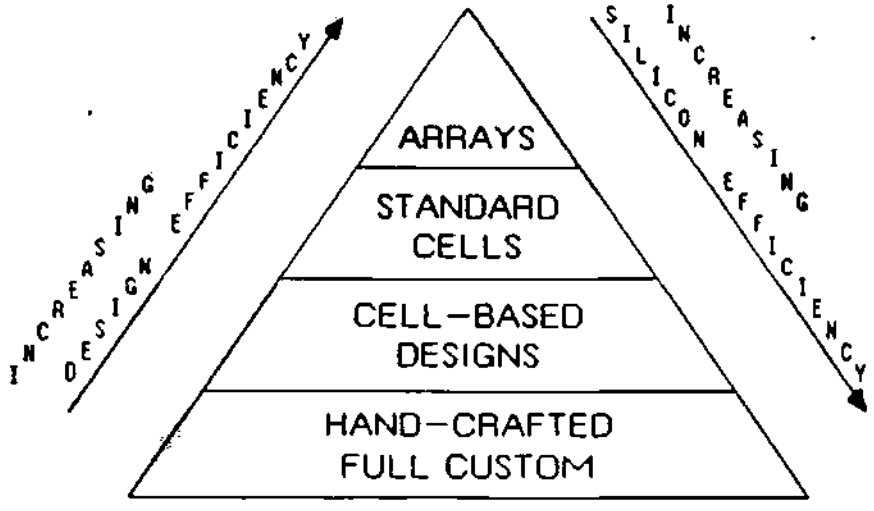
SPECTRUM OF ANALOG ASIC SOLUTIONS



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TWO CLASSES OF LINEAR AND MIXED LINEAR / DIGITAL ASICS

1 — Those requiring unique grouping of relatively standard functions:

BEST SERVED BY SEMICUSTOM

2 — Those requiring very high performance specialized blocks:

BEST SERVED BY FULL-CUSTOM

Micro Linear

CHARACTERISTICS OF LINEAR BIPOLAR TECHNOLOGY

- High performance (gain, bandwidth, noise)
- Less sensitive to chip layout
- Easier off—chip interface
- High power consumption
- Poor silicon efficiency

Best suited to Array Designs

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CHARACTERISTICS OF CMOS TECHNOLOGY FOR ANALOG APPLICATIONS

- Poor performance (gain, bandwidth, noise)
- Very sensitive to chip layout
- Difficult off—chip interface
- Low power consumption
- Sample / hold capability
- High silicon efficiency
- Can mix Linear / Digital functions

Best suited to Standard—Cell Designs

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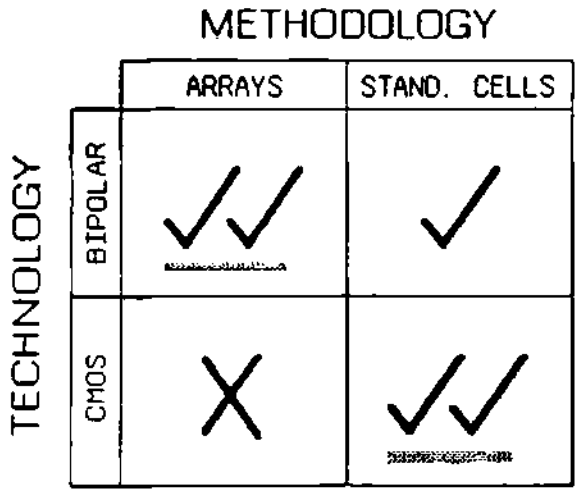
SEMICUSTOM TECHNIQUES FOR ANALOG ASICS



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LINEAR ARRAYS

- RANDOM ARRAYS
  - Random grouping of resistors / transistors
  - Suitable for component—level design
  - Difficult to automate
- STRUCTURED ARRAYS
  - Combinations of mini—arrays
  - Can be used with cell libraries
  - Suitable for function—level design
  - Easy to automate

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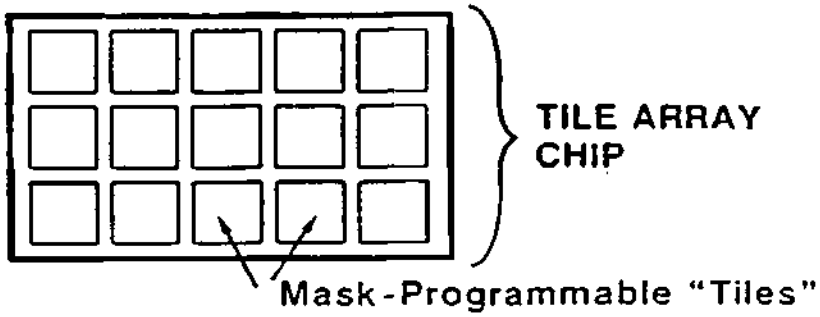
THE TILE-ARRAY CONCEPT
An Array of Mask-Programmable "Tiles"



- Customized with 2-Layers of Metal
- Each "Tile" Mask-Programmable into a Stand-Alone Linear Function
- Allows Automated Design of Linear LSI at Modular Function Level

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CUSTOM LSI DESIGN
Case Study

PRODUCT: Disk Drive Controller ORDER QUANTITY: 20,000 Pieces

	TILE-ARRAY DESIGN	CONVENTIONAL FULL-CUSTOM
Development Time:	10 Weeks	60 Weeks
Development Cost:	$ 12,000.00	$120,000.00
Unit Selling Price:	$ 6.00	$ 5.00
Total Program Cost:	$132,000.00	$220,000.00

Advantages:
- 90% Development Cost Savings
- 83% Reduction in Development Time

Micro Linear

A PARTIAL LIST OF LINEAR CELLS IN THE SC-2000 FAMILY

- Gain Cells (5 Cells)
- Operational Amplifiers (12 Cells)
- Buffer Amplifiers (3 Cells)
- Comparators (2 Cells)
- Sample/Hold (1 Cell)
- Voltage Reference (1 Cell)
- Bias Generators (3 Cells)
- Oscillators (2 Cells)
- Phase-Locked Loops (2 Cells)
- Multiplexers and Modulators (5 Cells)
- Switched-Capacitor Filters (10 Cells)
- Continuous-Time Filters (2 Cells)
- Analog/Digital Converters (3 Cells)
- Digital/Analog Converters (3 Cells)

Micro Linear

ANALOG CAD / CAE TOOLS

SOFTWARE	HARDWARE
• Device Modeling	• Personal Computer Based
• Circuit Simulation	• Workstation Based
• Circuit Synthesis	• Mainframe Based
• Parameter Extraction	
• Cell Compilation	
• Auto Place/Route	

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TWO KEY FACTORS IN ANALOG DESIGN AUTOMATION

- Device Modeling
- Circuit Simulation

⟿ Particularly Critical in MOS Analog ⟿

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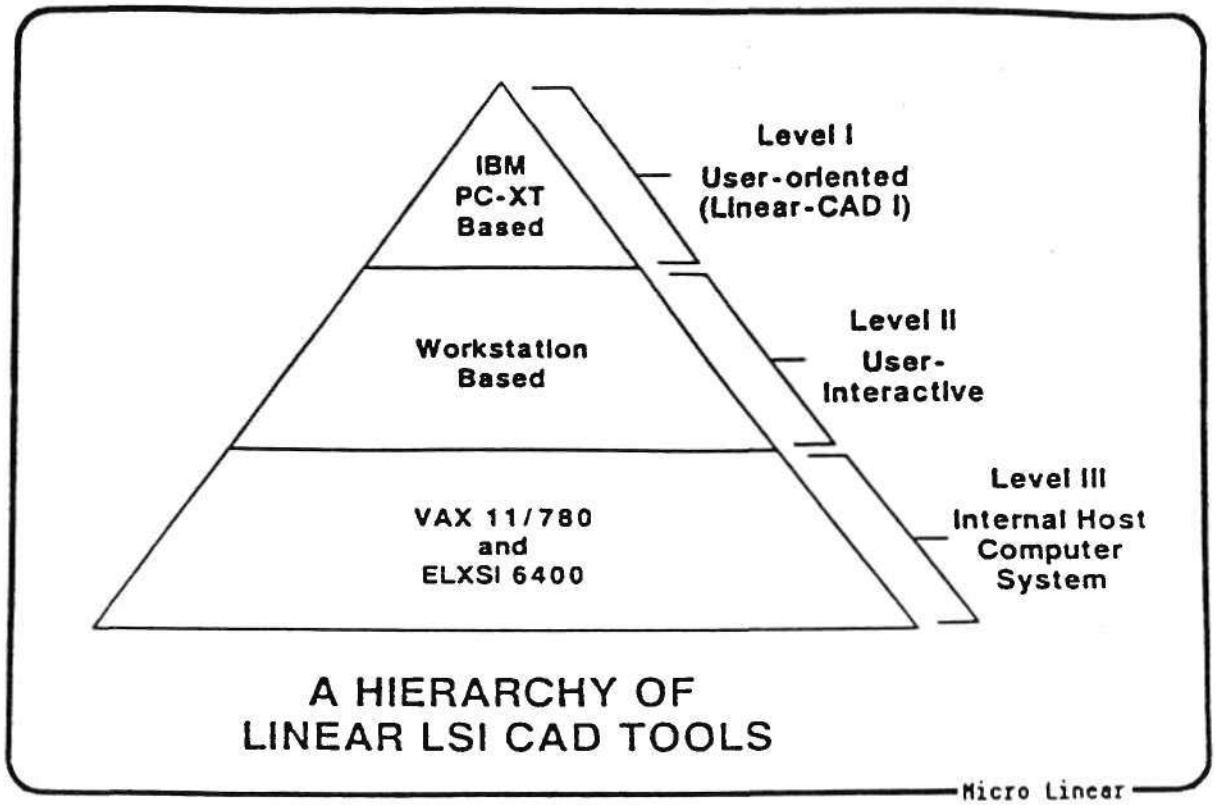

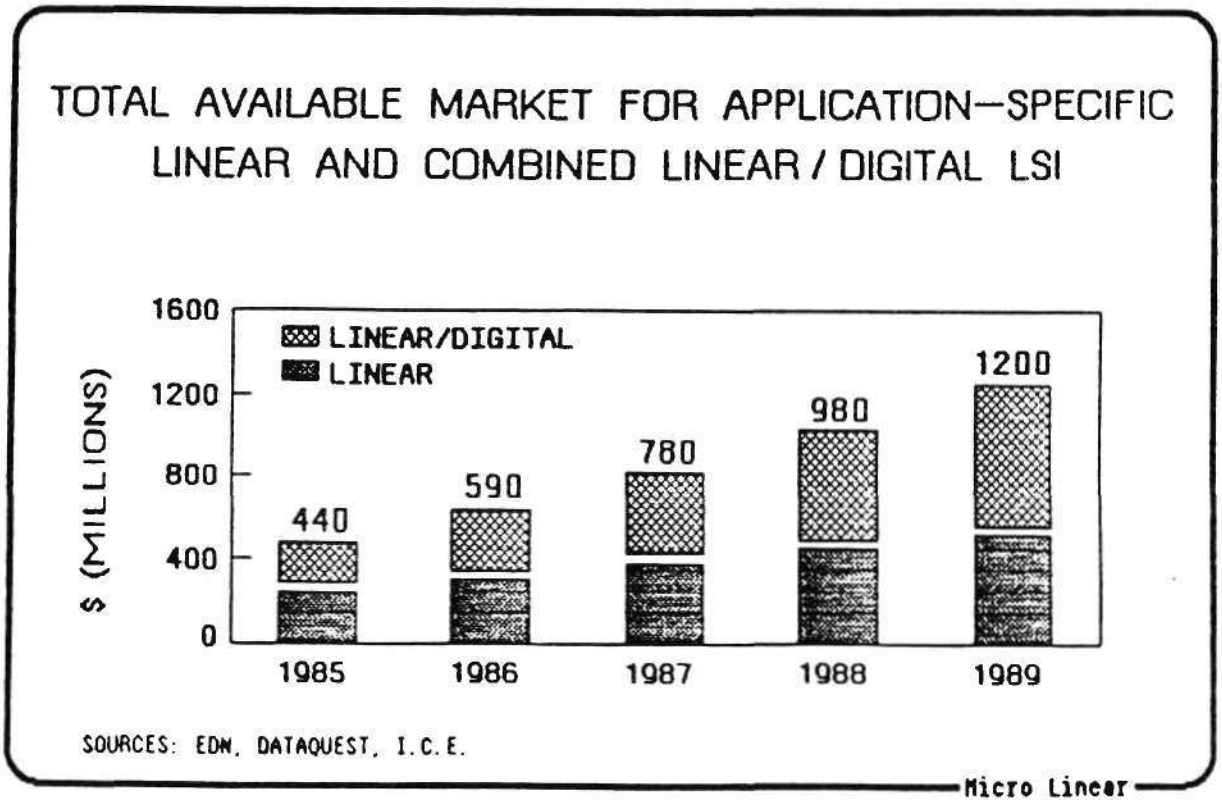

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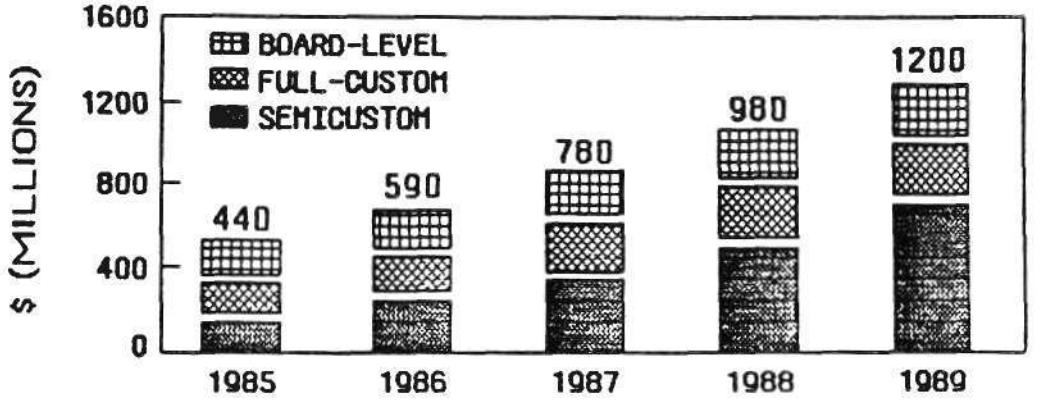
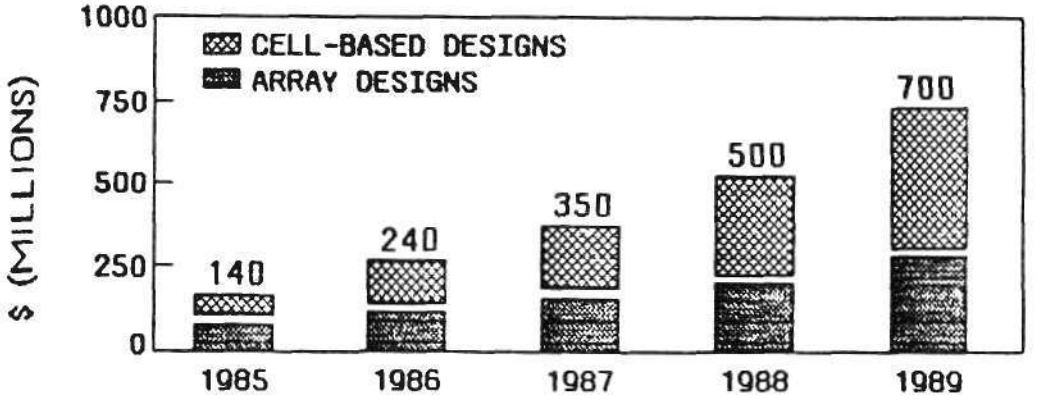
TOTAL MARKET FOR APPLICATION–SPECIFIC LINEAR AND MIXED LINEAR / DIGITAL LSI



SOURCES: DATAQUEST, GNOSTIC CONCEPTS, I.C.E.

Micro Linear

TOTAL MARKET FOR SEMICUSTOM LINEAR AND MIXED LINEAR / DIGITAL LSI



SOURCES: DATAQUEST, GNOSTIC CONCEPTS, I.C.E.

Micro Linear

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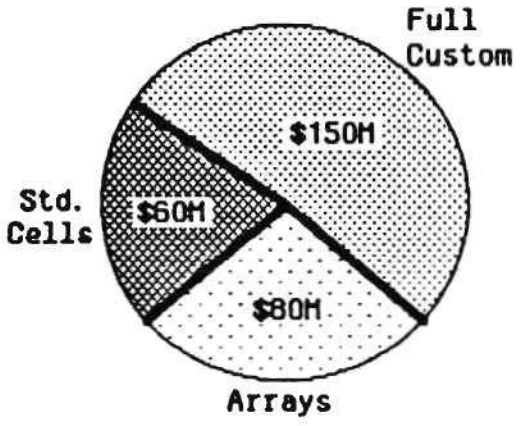
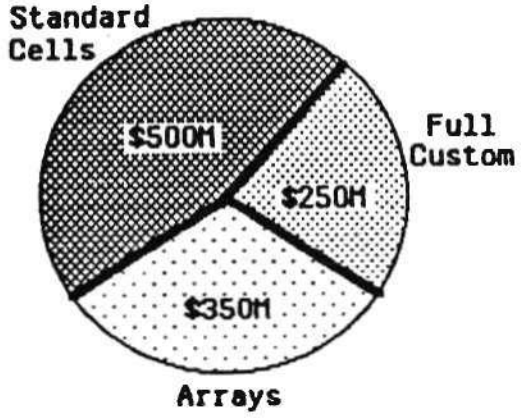
LINEAR AND MIXED LINEAR / DIGITAL ASIC MARKET



1985 = $290 Million



1990 = $1,100 Million

Micro Linear

PRIMARY END–USER MARKETS FOR LINEAR AND MIXED LINEAR / DIGITAL ASICS

- Telecommunications
- Computer Peripherals
- Industrial Controls & Instrumentation
- Military

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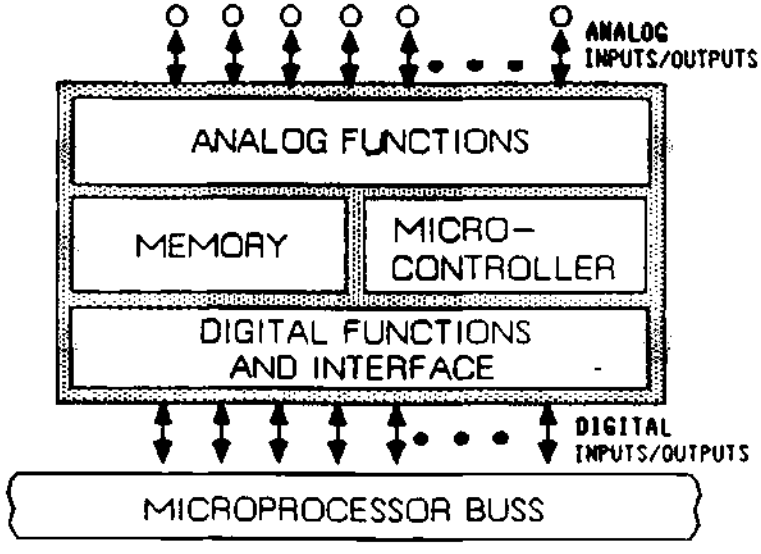
TRENDS IN ANALOG ASICS

- INCREASING SEMICUSTOM CAPABILITY
  - Structured Linear Arrays
  - System—level mixed Linear/Digital ASICS using CMOS Standard Cells
- INCREASING USER INVOLVEMENT IN DESIGN PROCESS
- PROGRAMMABLE ANALOG ASIC'S
  (Software—controlled Analog VLSI)

Micro Linear

SOFTWARE—CONTROLLED ANALOG ASICS



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Nielsen Dataquest

STRATEGIES FOR EFFECTIVE SILICON USE

Eli Harari
President
WaferScale Integration, Inc.

Mr. Harari is the President and Chief Executive Officer of WaferScale Integration, Inc., Fremont, California. Previously, he was Vice President of Operations/Technology at Synertek, Inc.; Manager of Technology Development at Intel Corporation; and Manager of the Microelectronics Research Center at Hughes Aircraft Company. Mr. Harari invented the first commercial CMOS EEPROM and the CMOS NOVRAM. In addition, he holds more than ten U.S. and foreign patents in EEPROM, EPROM, DRAM, SRAM, serial memories, imagers, and semiconductor processing techniques. Mr. Harari received a B.Sc. degree in Physics with honors from Manchester University in England and a Ph.D. degree in Solid State Sciences from Princeton University.

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SEMICONDUCTOR INDUSTRY CONFERENCE
October 14, 15, and 16, 1985
Tucson, Arizona

WaferScale
INTEGRATION, INC.

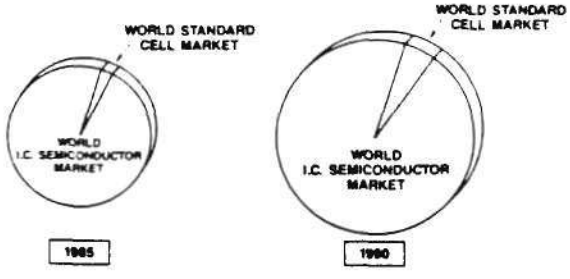
STRATEGIES FOR EFFECTIVE SILICON USE

WaferScale

- Effective Silicon Use Involves Unique Devices for Specialized Functions
- Effective Silicon Use Requires a Systems Perspective
- Tools Are Now Available to Enable the System Designer to Create Unique Devices
- Successful ASIC Companies Will Become the Natural Extension of the System Designer

WaferScale

MARKET OPPORTUNITY



	1985	1990
I.C.	$19.37 B (100%)	$51.54 B (100%)
Standard Cell	$ 0.25 B (1.3%)	$ 3.94 B (7.6%)

Standard Cell Market Will Grow 1546% in 5 Years

Source: Dataquest, June 1985

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WaferScale INTEGRATION, INC.

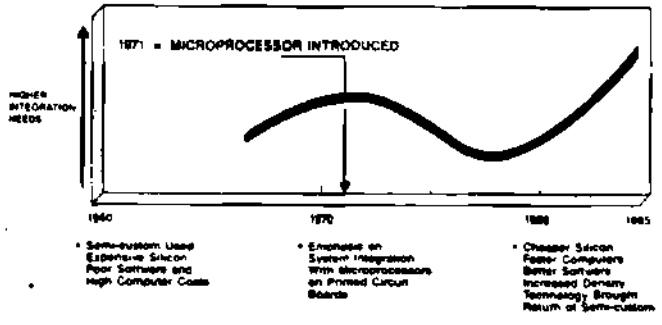
ASIC's Satisfy a Growing Need for System Companies:

- Reduced System Cost
  - —Reduced Components, Boards, Power Supplies, Cooling
  - —Lower Assembly, Test, Burn-In Costs
- Enhanced Product Competitiveness
  - —Higher Performance and Reliability
  - —Smaller Size
  - —Proprietary Design Protection
  - —Feature Differentiation

INCREASED PROFITABILITY

WaferScale

SEMI-CUSTOM EMPHASIS



BASIC BARRIERS ARE FALLING

- Process Technology — CMOS VLSI Here Now, WSI Within Sight
- Manufacturing Yields — Automation Allowing Very Affordable Cost Per Gate, Very Reliable Silicon
- Workstations — Powerful, Affordable, Proliferating

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BASIC BARRIERS ARE FALLING

- **Design Software —** **Correct Design By Construction, Good Simulators and Place/Route, Expanding Large Block Libraries**
- **Time to Market —** **8–16 Weeks Now Normal for VLSI Devices**
- ***Remaining Barrier —*** ***Universal Embrace By System Designers***

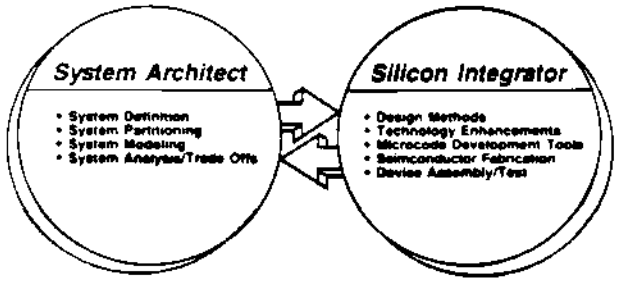
Tools Are Now in Place for Effective Use of Silicon

WHY THE NEED FOR A SYSTEM/SEMICONDUCTOR PARTNERSHIP?

- Systems Must Integrate on Silicon to Survive
- Capital Intensity of Semiconductor Facilities Must Be Diffused Among Users
- System and Semiconductor Complexity Require Scarce Complementing Skills

WaferScale

TODAY'S STRATEGIC ALLIANCE



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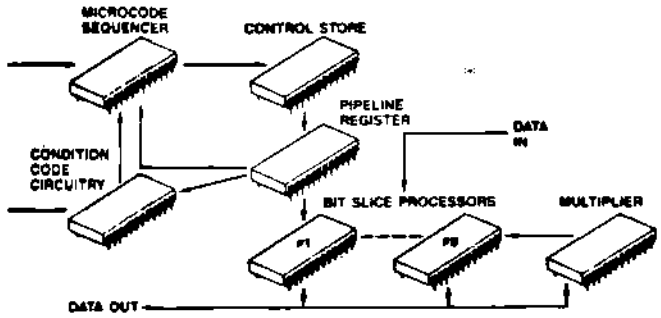
EXAMPLE OF AN EFFECTIVE USE OF SILICON

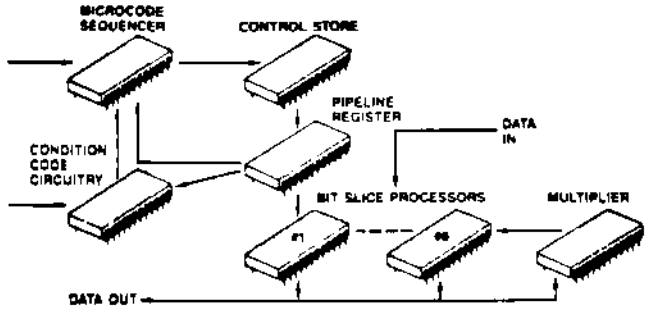
- "System-on-a-Chip" Solution

Bit Slice Architecture System

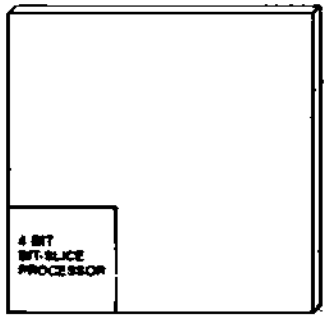


- "System-on-a-Chip" Solution

Bit Slice Architecture System



EFFECTIVE USE OF SILICON



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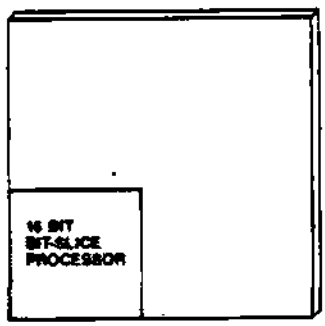
EFFECTIVE USE OF SILICON



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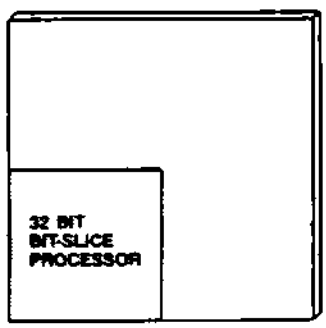
EFFECTIVE USE OF SILICON



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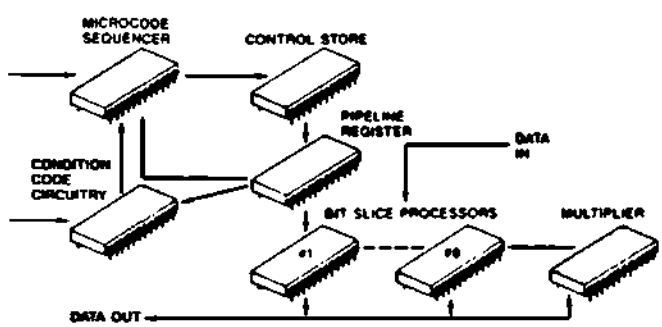
- "System-on-a-Chip" Solution

Bit Slice Architecture System



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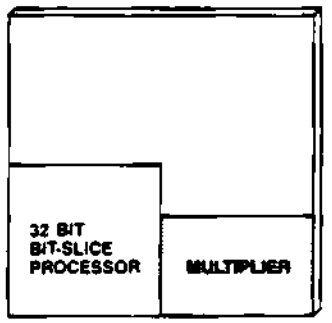

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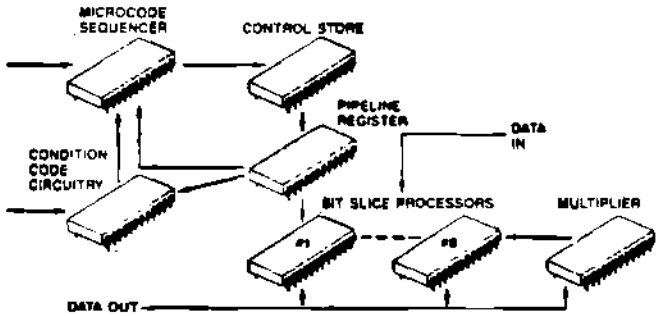
- "System-on-a-Chip" Solution

Bit Slice Architecture System



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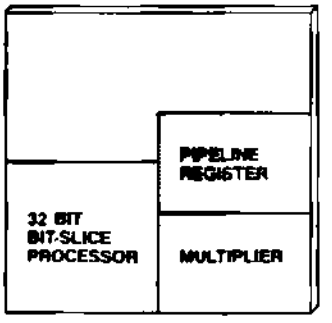

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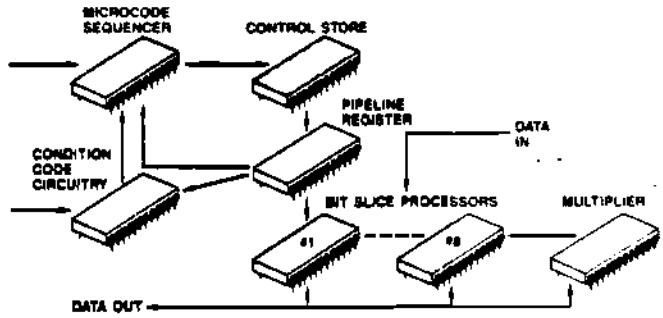
- "System-on-a-Chip" Solution

Bit Slice Architecture System



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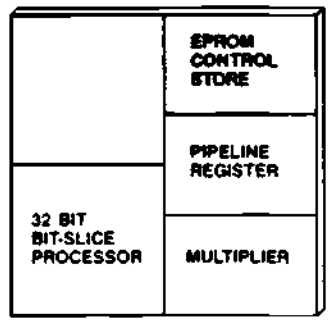

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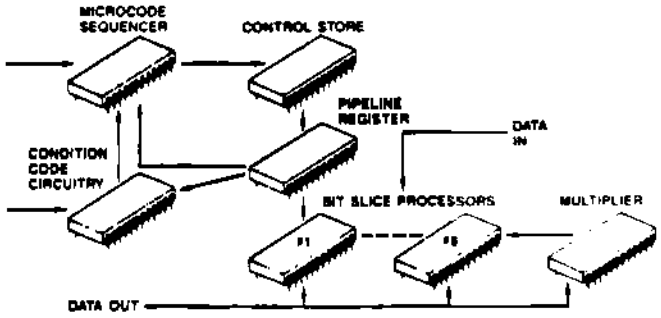
- "System-on-a-Chip" Solution

Bit Slice Architecture System



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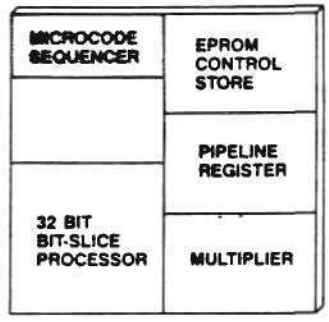

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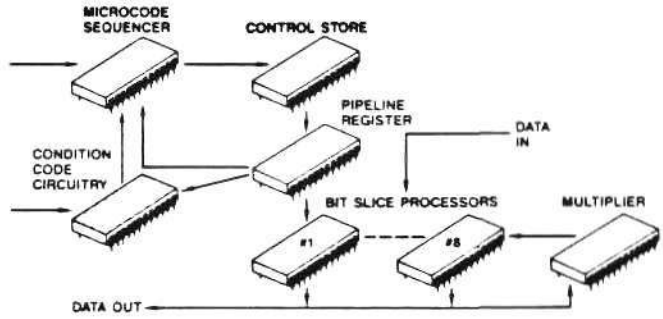
- "System-on-a-Chip" Solution

Bit Slice Architecture System



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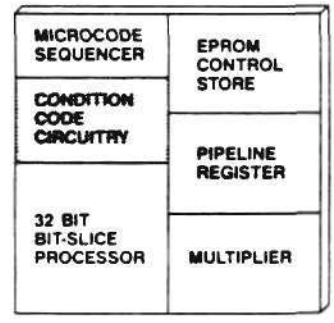

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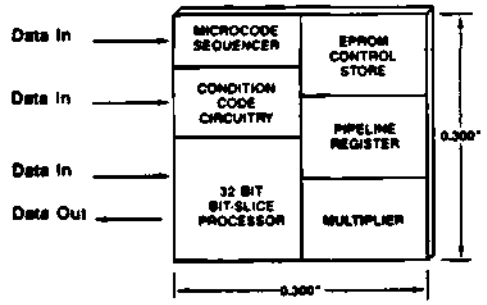
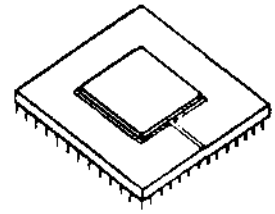


Graphics Processor Engine

- CMOS "System-on-a-Chip"
- 5+ MIPS
- Prototypes in 14 Weeks After Simulation Sign-Off

EFFECTIVE USE OF SILICON



Graphics Processor Engine

- System Architect — Definition
- Silicon Integrator — Creation

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EFFECTIVE USE OF SILICON

- **HIGH PERFORMANCE SEMI-CUSTOM APPLICATIONS:**
  - **CAD/CAE Workstations**
  - **High Resolution Graphics Controllers**
  - **Telecommunications**
  - **Speech Processing**
  - **Image Processing**
  - **Graphics Engine**
  - **Mini-Computers**
  - High Speed Industrial Control
  - Local Area Network Controllers

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WaferScale INTEGRATION, INC.

EFFECTIVE USE OF SILICON REQUIRES:

- Cooperative Business Alliances
- Systems Definition by Systems Architects
- Efficient High Level Design Tools
- Leveraged Manufacturing Sources
- Latest Silicon Technology

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VENTURE CAPITAL IN TRANSITION

Wallace F. Davis
General Partner
Alpha Partners

Mr. Davis is a founder and General Partner of Alpha Partners, a venture capital limited partnership located in Menlo Park, California. Previously, he was a founder and General Partner of Mayfield, another venture capital firm. Prior to that, Mr. Davis was Vice President for R&D at Itek Corporation, which had acquired Vidya, a company of which he was a founder and the President. He was also a Research Engineer and an Engineering Manager at NASA's Ames Aeronautical Laboratory. Mr. Davis received an A.B. degree in Mechanical Engineering and an M.S. degree in Aeronautical Engineering from Stanford University.

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SEMICONDUCTOR INDUSTRY CONFERENCE
October 14, 15, and 16, 1985
Tucson, Arizona

VENTURE CAPITAL IN TRANSITION

Wallace F. Davis
General Partner
Alpha Partners

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Semiconductor industry has become so pervasive that a "transition" period affects many other industries, including Venture Capital

Significance of semiconductor industry to Venture Capital

Offshore competition

Protectionist legislation

Technology transfer

Long-range planning

Cooperation between industry, finance, academia and government

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Example of Venture Capital investment in the semiconductor industry -- Altera Corporation

Origin

Due diligence

"Seed" financing

Subsequent financing

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Venture Capital Operations

- Limited partnerships
- Variations in strategy
- Portfolio performance
- Pay-off

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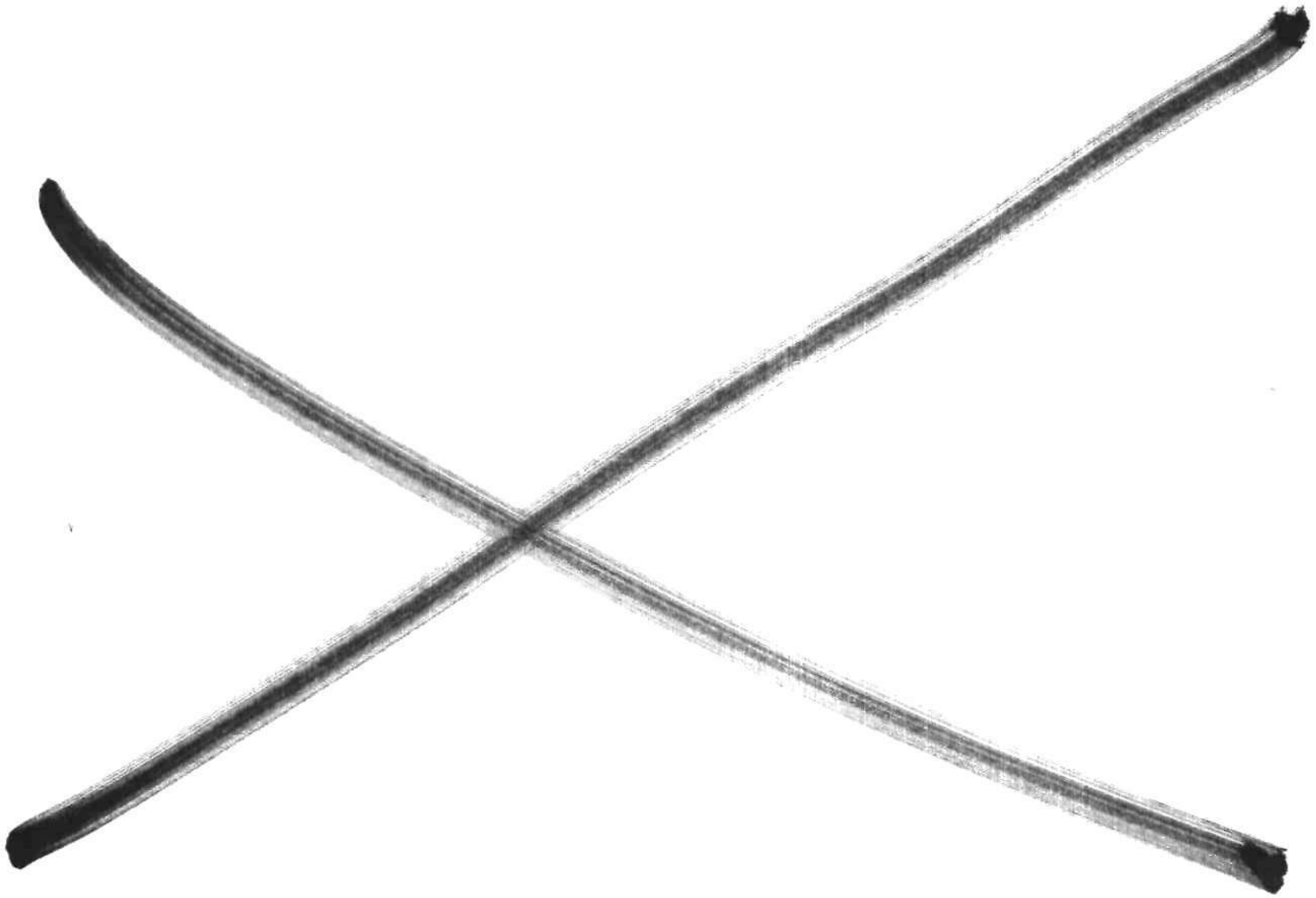
Contributions of Venture Capital

United States

Off-shore



Nielsen Dataquest

AUTOMATION OF LSI MANUFACTURING

Hiroyoshi Komiya
Deputy Manager, Saijo Factory
Mitsubishi Electric Corporation

Dr. Komiya is a Deputy Manager of Mitsubishi Electric Corporation's Saijo Factory, and has general responsibilities for production and technology at the Saijo Factory. Before being transferred to the Saijo Factory, he was a Manager of the Equipment Engineering Department at Mitsubishi's Kitaitami Works, where he managed the design, development, and construction of production lines for the Saijo Factory. Before that, he worked as a Deputy Manager of the Memory and Microprocessor Department at the Kitaitami Works, as a member of the senior research staff for wafer processing technology at the cooperative laboratories of VLSI Research Association, and as a senior research staff member at Mitsubishi's Central Research Laboratories. Dr. Komiya holds a B.S. degree in Physics and a Dr. Science degree from Kyushu University.

Dataquest Incorporated
SEMICONDUCTOR EQUIPMENT AND MATERIALS INDUSTRY SERVICE CONFERENCE
October 14-16, 1985
Tucson, Arizona

DR. HIROYOSHI KOMIYA
DEPUTY MANAGER, SAIJO FACTORY
MITSUBISHI ELECTRIC CORPORATION

AUTOMATION OF LSI MANUFACTURING

INTRODUCTION

AUTOMATION OF LSI MANUFACTURING HAS MADE PROGRESS IN ORDER OF THE AUTOMATION OF INDIVIDUAL PRODUCTION EQUIPMENT, THE DEVELOPMENT AND USE OF THE PRODUCTION MANAGEMENT SYSTEM, AND THE INTEGRATION OF MULTIPLE EQUIPMENTS. RECENTLY, BIG EFFORTS ARE BEING MADE FOR MATERIALIZING A TOTALLY AUTOMATED MANUFACTURING PLANT.

THE AUTOMATED MANUFACTURING LINE OFFERS SEVERAL BENEFITS:

1. THE NUMBER OF WORKERS IS DECREASED.

2. THE YIELD AND QUALITY OF LSI CHIPS BECOME HIGHER AND STABLE BECAUSE THE HUMAN FACTORS, NAMELY, CONTAMINATION FROM PERSONNEL, MIS-OPERATION DUE TO PERSONNEL, ETC., ARE ELIMINATED.

3. IT SIMPLIFIES THE VERY COMPLICATED PRODUCTION MANAGEMENT IN THE MANUFACTURING LINE FOR LARGE VARIETY, SMALL VOLUME PRODUCTS LIKE SEMI-CUSTOM LSI.

4. THE LEAD TIME BECOMES SHORTER AND THE WORK-IN-PROCESS DECREASES, ETC.

ON THE OTHER HAND, THERE ARE SOME DEMERITS:

1. THE INVESTMENT IS INCREASED BECAUSE OF THE CONTROL SYSTEM AND TRANSPORT SYSTEM ADDED.

2. IT BECOMES MORE DIFFICULT TO CHANGE THE LINE STRUCTURE WHEN THE PRODUCTS ARE BEING CHANGED.

3. THE SPACE FACTOR AND THE WORKING RATES OF EQUIPMENT TEND TO DECREASE, ETC.

THIS PAPER WILL DISCUSS SEVERAL PROBLEMS ABOUT THE AUTOMATION OF THE LSI MANUFACTURING LINE.

STRUCTURE OF THE MANUFACTURING LINE

IN THE WAFER PROCESSING LINE, IT HAS BEEN QUITE COMMON THAT ONE EQUIPMENT IS USED FOR SEVERAL PROCESS STEPS SINCE WAFERS PASS MANY TIMES THROUGH SIMILAR PROCESSES AND EQUIPMENT HAS THROUGHPUTS MUCH DIFFERENT FROM EACH OTHER. THE STRUCTURE OF THE AUTOMATED MANUFACTURING LINE, THEREFORE, IS MORE COMPLICATED THAN THAT OF THE LINEAR STRUCTURE, IN WHICH WORK PASSES ONLY ONCE THROUGH EACH PIECE OF EQUIPMENT.

THE OLDEST AND MOST POPULAR STRUCTURE FOR THE WAFER PROCESSING LINE IS THE JOB SHOP STRUCTURE, IN WHICH THE SAME KIND OF EQUIPMENT IS GATHERED AND PLACED IN THE SAME FAB AREA. FIGURE 1 SHOWS THE CONCEPT OF THIS STRUCTURE. SUGIYAMA OF NEC ADVANCED THIS CONCEPT AND HAS PROPOSED THE PROCESS CELL STRUCTURE.[1] THIS TYPE OF STRUCTURE MIGHT HAVE THE HIGHEST FLEXIBILITY FOR CHANGE IN THE VARIETY AND VOLUME OF PRODUCTS, AND TO A MODIFICATION OF THE LINE AND THE HIGHEST RATE OF OPERATION OF INDIVIDUAL EQUIPMENT. ON THE OTHER HAND, IT REQUIRES THE INTER- AND INTRA-SHOP TRANSPORT SYSTEMS TO HAVE VERY HIGH EFFICIENCIES AND QUITE COMPLICATED CONTROLS FOR THE TRANSPORT SYSTEM AND THE EQUIPMENT.

THE OPPOSITE EXTREME OF THE JOB SHOP STRUCTURE IS THE LINEAR STRUCTURE AS STATED BEFORE. IN THIS STRUCTURE, THE TRANSPORT SYSTEM, THE CONTROL FOR THE TRANSPORT SYSTEM, AND THE EQUIPMENT ARE GREATLY SIMPLIFIED. THE FLEXIBILITY AND THE RATE OF OPERATION OF INDIVIDUAL EQUIPMENT, HOWEVER, WILL BE EXTREMELY LOW, AND A PRACTICAL LINE WILL BE EXPECTED FOR THE MASS PRODUCTION.

AS AN INTERMEDIATE STRUCTURE BETWEEN THE TWO TYPES OF STRUCTURES DESCRIBED ABOVE, THERE IS THE BLOCK STRUCTURE, IN WHICH A LONG TRAIN OF PROCESS STEPS IS DIVIDED INTO SEVERAL BLOCKS. THE BLOCKS ARE CONNECTED WITH EACH OTHER INTO THE LINEAR STRUCTURE, AND INSIDE EACH BLOCK, THE LINE IS CONSTRUCTED WITH THE JOB SHOP STRUCTURE. FIGURE 2 SHOWS THE CONCEPT OF THE BLOCK STRUCTURE, WHICH, IN SHORT, IS AN OPTIMUM POINT OF COMPROMISE BETWEEN THE JOB SHOP AND LINEAR STRUCTURES. THAT IS, IF THE NUMBER OF BLOCKS INCREASES, THE BLOCK STRUCTURE WILL COME NEAR THE LINEAR STRUCTURE, AND IF IT DECREASES, THE STRUCTURE WILL COME NEAR THE JOB SHOP STRUCTURE. IT SHOULD BE DECIDED, DEPENDING ON THE CHARACTERISTICS OF THE PRODUCTION LINE, IN WHAT WAY AND INTO HOW MANY BLOCKS THE PROCESS IS TO BE DIVIDED.

IN THE WAFER TESTING, ASSEMBLY, AND FINAL TESTING PROCESSES, THE LINES ARE PRINCIPALLY CONSTRUCTED WITH THE LINEAR STRUCTURE. SOME PARTS OF THE LINE CONSIST OF MULTI-PASSAGE FOR BALANCING THE THROUGHPUT AMONG PROCESS STEPS OR FOR PROCESSING A VARIETY OF PRODUCTS. AFTER THE WAFER TESTING PROCESS IS COMPLETED, THE UNIT OF WORK CHANGES FROM A WAFER TO A CHIP OR DEVICE, AND THE WORK HAS NOT BEEN STANDARDIZED. THE LINE STRUCTURE, THEREFORE, SHOULD BE DECIDED BY THE PRODUCTS OR PACKAGES TO BE MANUFACTURED AND BY THEIR QUANTITIES.

THE CONTROL SYSTEM

THE CONTROL SYSTEM MUST ADDRESS THE FOLLOWING INFORMATION:

1. PROCESS INFORMATION: PROCESS PARAMETERS AND OPERATION OF EQUIPMENT.

2. QUALIFY INFORMATION: COLLECTION, ANALYSIS, AND MANAGEMENT OF THE TEST PLUS INSPECTION DATA RELATING TO THE DEVICE QUALITY.

3. WORK FLOW INFORMATION: CONTROL AND TRACK OF WORK-IN-PROCESS.

4. EQUIPMENT INFORMATION: WARNING OF EQUIPMENT NOT IN PROPER CONDITION PLUS COLLECTION, ANALYSIS, AND MANAGEMENT OF DATA RELATING TO THE STATUS OF EQUIPMENT.

5. MATERIAL INFORMATION: CONTROL OF PURCHASE AND SUPPLY OF DIRECT AND INDIRECT MATERIALS.

THE FUNDAMENTAL DATA BASE, INCLUDING BASIC PARAMETERS AND PROCESS FLOWS THAT BECOME THE BASE OF INFORMATION DESCRIBED ABOVE, MUST BE INPUT MANUALLY BEFORE THE SYSTEM STARTS TO WORK. THE ORDER OF WORK TO BE INPUT AND THE PRIORITY THAT IS BASED ON THE SALES ORDER PLUS MARKETING INFORMATION IS ALSO INPUT MANUALLY. THE DATA OR INFORMATION OTHER THAN THAT DESCRIBED ABOVE IS DESIRABLE TO BE PROCESSED OR TREATED AUTOMATICALLY WITHIN THE SYSTEM.

FIGURE 3 SHOWS AN EXAMPLE OF THE CONTROL SYSTEM ARCHITECTURE THAT HAS A HIERARCHAL STRUCTURE OF FOUR HALVES. THE FACTORY LEVEL PROCESSOR IS IN CHARGE OF MANAGING AND PROCESSING THE DATA FOR THE FACTORY MANAGEMENT LEVEL. THE PROCESSORS CONTROLLING THE PRODUCTION LINE BY THE REAL-TIME BASE ARE THE FIRST AND SECOND LEVEL ONES, AND CONTROLLERS OF INDIVIDUAL EQUIPMENT ARE THE LOWEST LEVEL PROCESSORS. THE INTERFACE BETWEEN THE SECOND LEVEL PROCESSORS AND THOSE OF INDIVIDUAL EQUIPMENT IS BASED ON FIGURE 1.

THE BASIC CONCEPT OF THE CONTROL SYSTEM IS NOT DIFFERENT FROM THOSE FOR MANUFACTURING LINES IN OTHER INDUSTRIES, AS IS UNDERSTOOD FROM THE ARCHITECTURE SHOWN IN FIGURE 3. IN THE CASE OF THE LSI MANUFACTURING LINE, HOWEVER, THE FOLLOWING SPECIAL FEATURES EXIST:

1. THE LINE CONSISTS OF PRODUCTION EQUIPMENT THAT IS SUPPLIED BY A LARGE VARIETY OF EQUIPMENT VENDORS.

2. THE LINE DOES NOT HAVE THE LINEAR STRUCTURE, ESPECIALLY IN WAFER FABRICATION.

3. BOTH THE RELIABILITY OF EQUIPMENT AND THE PROCESS CAPABILITY ARE FAIRLY LOW.

4. THE PERIOD FOR RETURN-OF-INVESTMENT IS VERY SHORT, AND EVEN IN SUCH A SHORT PERIOD, THE EQUIPMENT AND PROCESS ARE OFTEN CHANGED.

THEREFORE, THE FOLLOWING SHOULD BE CONSIDERED WHEN THE CONTROL SYSTEM IS DESIGNED AND CONSTRUCTED:

1. THE SYSTEM DEBUGGING THE ACTUAL PRODUCTION LINE IS TO BE DONE EFFICIENTLY IN A SHORT PERIOD.

2. COMMUNICATION AND MECHANICAL INTERFACES BETWEEN EQUIPMENT AND OTHER SYSTEMS MUST BE STANDARDIZED.

3. TROUBLE IN ONE PIECE OF EQUIPMENT SHOULD AFFECT AS NARROW OF A REGION AS POSSIBLE, AND THE EQUIPMENT CAN EASILY RETURN TO CONTROL THE SYSTEM IN A SHORT PERIOD AFTER THE RECOVERY.

4. UNUSUAL TREATMENTS, SUCH AS REPROCESSING AND EXPERIMENTAL FLOW, CAN BE EXECUTED EASILY.

5. THE SYSTEM MUST BE FLEXIBLE TO CHANGES IN PROCESS FLOW, PARAMETERS, MODIFICATION AND REARRANGEMENT OF THE LINE.

TRANSPORT SYSTEM AND LAYOUT

VARIOUS APPROACHES TO THE INTER-EQUIPMENT TRANSPORT SYSTEM HAVE BEEN PROPOSED.[2] OF THOSE, A SINGLE WAFER TRANSPORT OVER A FIXED TRACK IS CONSIDERED TO BE DIFFICULT TO USE IN THE MASS-PRODUCTION LINE, THEREFORE, A BATCH TRANSPORT WILL BE EMPLOYED BY USING CASSETTES OR MAGAZINE.

THERE ARE MANY TYPES OF TRANSPORT MACHINES: CONVEYERS, AUTOMATED GUIDED VEHICLES, MOVING ROBOTS, CEILING MONORAILS, ETC. WHEN WE CHOOSE THE TRANSPORT SYSTEM, WE MUST TAKE INTO ACCOUNT THE DUST GENERATION, TRANSPORT CAPACITY, WEIGHT AND SIZE OF WORK TO BE TRANSPORTED, POSITION ACCURACY REQUIRED AT TRANSFER POINTS, FLEXIBILITY TO THE CHANGE OF ROUTES AND TRANSFER POINTS, SAFETY, METHOD OF COMMUNICATION, LAYOUT OF THE LINE, ETC.

A TRANSPORT SYSTEM CONSISTS OF A COMBINATION OF TRANSPORT MACHINES AS DESCRIBED ABOVE. TEMPORARY STORAGE SITUATIONS ARE NECESSARY FOR ADJUSTING WORK-IN-PROCESS, BRANCH STATIONS FOR TRANSFERRING WORK BETWEEN TWO TRANSPORT MACHINES, STATIONS FOR REARRANGEMENT OF BATCHES, NUMBER READERS FOR RECOGNIZING LOTS FOR WORK, AND THE CONTROL SYSTEM. BEFORE THE DESIGN OF THE INTER-EQUIPMENT TRANSPORT SYSTEM IS COMPLETED, THE TRANSPORT SIMULATION MUST BE SUFFICIENTLY PERFORMED, INCLUDING THE CASE OF UNUSUAL TREATMENTS DUE TO THE SYSTEM OR EQUIPMENT BREAKING DOWN OR PROCESS TROUBLE.

ONCE THE STRUCTURE OF THE LINE IS DECIDED, THE LAYOUT CAN BE DESIGNED IN BASICALLY THE SAME WAY AS FOR THE CONVENTIONAL LINE, EXCEPT FOR THE INTER-EQUIPMENT TRANSPORT SYSTEM BEING ADDED. THEREFORE, SPACE FOR THE INTER-EQUIPMENT TRANSPORT SYSTEM MUST BE PROVIDED, TRANSFER OF WORK BETWEEN EQUIPMENT AND THE TRANSPORT SYSTEM MUST BE PROVIDED, AND TRANSFER OF WORK BETWEEN EQUIPMENT AND THE TRANSPORT SYSTEM SHOULD BE WELL EXAMINED. FOLLOWING ARE SOME REQUIREMENTS TO BE TAKEN INTO ACCOUNT WHEN A LAYOUT IS DESIGNED FOR THE AUTOMATED LSI MANUFACTURING LINE:

1. THE NUMBER OF CROSSINGS BETWEEN TWO TRANSPORT CHANNELS IS AS FEW AS POSSIBLE.

2. MANUAL OPERATION IS POSSIBLE LOCALLY WHEN ANY PART OF THE CONTROL SYSTEM BREAKS DOWN.

3. REMODELING THE TRANSPORT SYSTEM MUST BE LIMITED TO A PART AS SMALL AS THAT OF MANUFACTURING EQUIPMENT WHEN THE LINE IS REMODELED.

FIGURE 4 SHOWS AN EXAMPLE OF A LAYOUT OF THE WAFER PROCESSING LINE. THERE IS A "MAIN STREET" AT THE CENTER OF THE LINE ON WHICH AUTOMATIC GUIDED VEHICLES (AGV) RUN. THE AGV CARRIES WAFER CASSETTES BETWEEN ANY TWO BRANCH STATIONS THAT ARE UNDER CONTROL OF A SECOND LEVEL CPU AS INDICATED IN FIGURE 3, AND TRANSFERS THEM TO OR FROM THE BRANCH STATION. FROM A BRANCH STATION, A MOVING ROBOT RUNS PERPENDICULAR TO THE "MAIN STREET", AND CARRIES WAFER CASSETTES AMONG THE BRANCH STATION AND LOADERS/UNLOADERS OF EQUIPMENT ALONG THE ROUTE OF THE ROBOT.

EQUIPMENT

AMONG TECHNOLOGIES FOR LSI FABRICATION, ONE WHICH IS DIFFICULT TO BE AUTOMATED IS VISUAL INSPECTION. PARTICULARLY IN RECENT YEARS, REQUIREMENTS ABOUT THE SIZE AND TYPE OF DEFECT TO BE DETECTED HAVE BECOME EXTREMELY SEVERE, AND THOSE ABOUT THE QUALITY AND RELIABILITY OF DEVICES DID, ALSO. THEREFORE, WE WILL HAVE TO GIVE UP THE AUTOMATION OF VISUAL INSPECTION FOR NOW, EXCEPT WITH VERY SIMPLE CASES. THAT IS, THE VISUAL INSPECTION SYSTEM, IN WHICH AN INSPECTION AND A JUDGEMENT ARE DONE MANUALLY, AND THE INCIDENTAL TASKS ARE ALL AUTOMATED, WILL THEN BE A PRACTICAL SOLUTION. THE REMOTE VISUAL INSPECTION SYSTEM, HAVING A HIGH RESOLUTION ITV, HAS ALSO BEEN DEVELOPED FOR KEEPING WORKERS AWAY FROM WAFERS OR CHIPS.

MOST EQUIPMENT FOR WAFER FABRICATION AND WAFER TESTING HAS ALREADY BEEN AUTOMATED IN THE CASSETTE-TO-CASSETTE MANNER. SINCE THE WAFER CASSETTE IS STANDARDIZED, NO LARGE PROBLEM EXISTS, EVEN BY USING COMMERCIALLY AVAILABLE EQUIPMENT FOR THE AUTOMATION OF THESE TWO PROCESSES. A WAFER HANDLER BETWEEN A CASSETTE AND A QUARTZ BOAT FOR A FURNACE, HOWEVER, WILL HAVE TO BE DEVELOPED BECAUSE NO GOOD HANDLER IS AVAILABLE IN THE MARKET.

SINCE THE SHAPE AND SIZE OF WORK CHANGES DEPENDING ON PRODUCTS AND PROCESSES IN FABRICATION BEYOND DICING, THE AUTOMATION OF INDIVIUDUAL EQUIPMENT HAS MADE SLOW PROGRESS. ALTHOUGH SOME EQUIPMENT IS AUTOMATED IN THE MAGAZINE-TO-MAGAZINE MANNER, THE MAGAZINE HAS NOT BEEN STANDARDIZED. THIS SITUATION IS ONE OF THE BIGGEST PROBLEMS WHEN CONSTRUCTING AN AUTOMATED MANUFACTURING LINE FOR THE ASSEMBLY AND FINAL TEST PROCESSES, AND THEREFORE, A CONSIDERABLE AMOUNT OF EQUIPMENT MUST BE DEVELOPED BY SEMICONDUCTOR MANUFACTURERS.

SUMMARY AND COMMENTS

THE STRUCTURE OF THE MANUFACTURING LINE, THE CONTROL SYSTEM, THE TRANSPORT SYSTEM AND THE LAYOUT, AND INDIVIDUAL EQUIPMENT WERE DISCUSSED FROM THE POINT OF VIEW OF THE AUTOMATION OF A LSI MANUFACTURING LINE. THE CONCEPTS SHOWN HERE AS EXAMPLES ARE THOSE FOR THE MANUFACTURING LINE HAVING A CERTAIN PURPOSE, AND IT IS NATURAL THAT THE LINE HAS ITS OWN CONCEPTS DEPENDING ON ITS PURPOSES AND CHARACTERISTICS.

THE LARGEST PROBLEMS IN THE AUTOMATION OF LSI MANUFACTURING LINES ARE:

1. THE RAPID CHANGE IN PRODUCTS, PROCESSES AND PRODUCTION EQUIPMENT.
2. THE LOW RELIABILITY OF PRODUCTION EQUIPMENT.
3. THE LOW PROCESS CAPABILITIES.

SINCE THESE PROBLEMS WILL REMAIN FOR NOW, IT IS ESSENTIAL TO DESIGN THE AUTOMATED LINE ON THE PREMISE OF THIS SITUATION.

IN CONCLUSION, THE ULTIMATE PURPOSE OF AUTOMATION IS TO MAKE THE PRODUCTION COST MINIMAL. THEREFORE, TOTAL AUTOMATION IS NOT ALWAYS THE BEST SOLUTION, BUT THE MOST APPROPRIATE COMBINATION OF AN AUTOMATED SYSTEM AND HUMANS WILL MORE CLOSELY ADDRESS THIS ULTIMATE PURPOSE. IN OTHER WORDS, "MANUALLY ASSISTED AUTOMATED PRODUCTION" WILL BE THE BEST CONCEPT FOR THE AUTOMATED LSI MANUFACTURING LINE.

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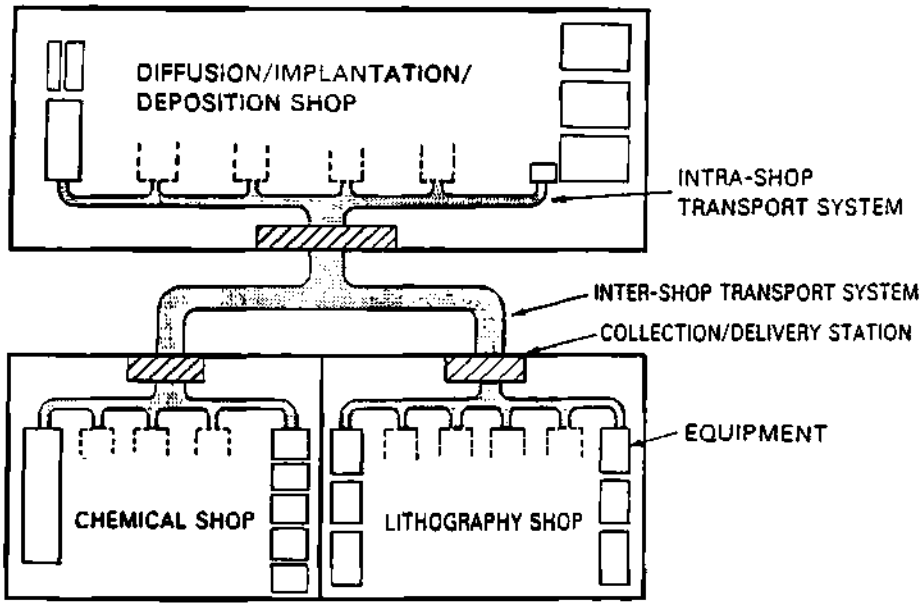

FIG 1. CONCEPT OF JOB SHOP STRUCTURE

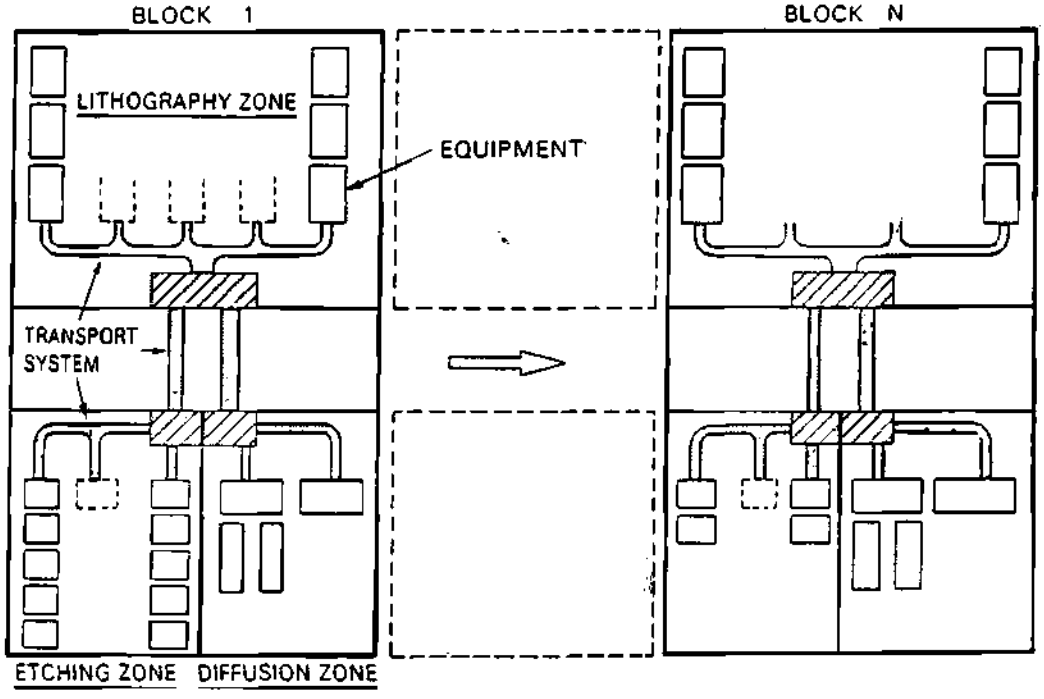

FIG 2. CONCEPT OF BLOCK STRUCTURE

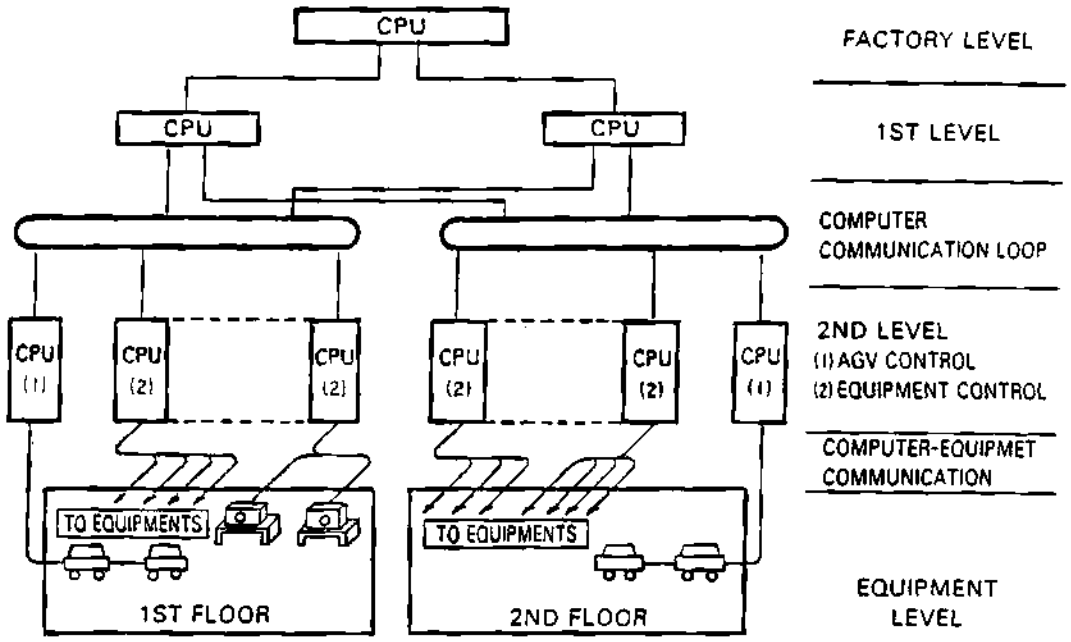

FIG 3. HIERARCHICAL ARCHITECTURE OF CONTROL SYSTEM

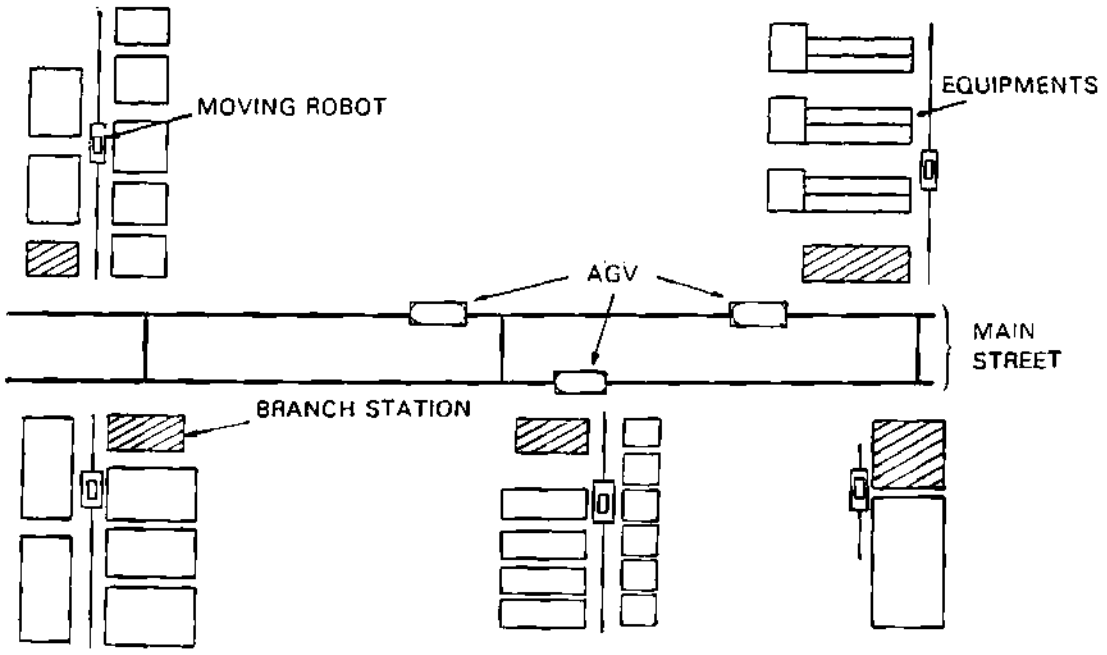

FIG 4. EXAMPLE OF LAYOUT OF WAFER PROCESS LINE

Nielsen Dataquest RESEARCH NEWSLETTER

SEMS Code: 1985-1986 Newsletters: August

THE NEW MITSUBISHI SAIJO FACTORY-- A FULLY AUTOMATED FACILITY

INTRODUCTION

DATAQUEST recently had the exceptional opportunity to visit Mitsubishi Electric Corporation's impressive new semiconductor factory located in Saijo on the island of Shikoku, Japan. DATAQUEST was escorted on the factory visit by Dr. Hiroyoshi Komiya, Deputy Manager of the Saijo factory, and Mr. Shigeru Funakawa, Semiconductor Overseas Marketing Manager for Mitsubishi. This factory, the first semiconductor facility on the island of Shikoku, was completed in early 1984 and is a fully automated front- and back-end facility dedicated to the production of DRAMs. The entire production process from bare silicon wafer start to final packaged and tested part is completely automated.

Dr. Komiya bas been invited to give a talk on the Saijo facility at DATAQUEST's annual Semiconductor Equipment and Materials Conference held October 14 through 17 in Tucson, Arizona. The theme of the Conference will be "An Industry in Transition." Dr. Komiya's talk on the Saijo facility at the Conference should, indeed, be a very interesting topic as attested to by the following brief overview of our visit to the facility.

THE SAIJO FACTORY

Presently, the Saijo factory consists of production buildings B and C, each of which has three floors covering 22,000 square meters of floor space. Building B is dedicated solely to the production of 64K DRAMs and has a capacity of 10 million parts per month. It was constructed at a cost of $127 million, including all capital equipment and automation hardware and software. Volume production of 64K DRAMs on 5-inch wafers began in March of 1984. Building C is dedicated to 256K DRAM production and was constructed at a cost of $190 million. It has a capacity of 7 million parts per month and volume production was scheduled to begin in July 1985. Next to Building C is an empty lot--yes, you guessed it--for a 1-Mbit DRAM facility, which is scheduled to be in production in the near future.

DATAQUEST visited the Building B 64K DRAM facility and the following discussion pertains to that facility. It is our understanding that the 256K DRAM facility is constructed along similar lines.

Device production occurs on two floors. The wafer fabrication area is located on the first floor and is a Class 10/Class 100 facility designed with a "main street" and "side street" concept. Up and down the wide main street move trackless but optically guided, automatically guided vehicles (AGVs) carrying cassettes of wafers. Branching off from main street at right angles are narrower side streets dedicated to the various wafer fabrication processes. For instance, there is a photolithography side street along which are clustered steppers and photoresist processing equipment. Dry etchers are clustered along another side street.

The AGVs in main street transfer their cassettes of wafers to I/O stations located at the junctions of the main and side streets. Robots moving in the side streets transfer the cassettes from the I/O stations to the various pieces of processing equipment located up and down the side street. The entire wafer fabrication production sequence is entirely automated; at no point in the production sequence do operators handle the wafers. Inspection at various points in the production process is done via CCTV by operators outside the clean room.

The first floor also includes the wafer test area laid out in the same main and side street approach. This area was designed to be Class 1000, but because of the reduction of people present (there appeared to be two) Class 100 levels were actually being reached. DATAQUEST noticed that in the wafer test area there were additional stationary robots transferring cassettes among several pieces of equipment clustered about them.

At the completion of wafer fabrication and probing, the wafers are automatically moved in an elevator up to the second floor where assembly and test occurs. On the second floor, overhead robots running on ceiling tracks transfer the devices among the various types of test equipment. All phases of assembly and test are fully automated including encapsulation and burn-in. Optical pattern recognition systems are used for automatic inspection of the marking step.

Communications and Control

The following is a brief overview of the factory automation system. A central factory computer interfaces with two control computers, one for each floor. For the first floor wafer fabrication and test area, the control computer interfaces to several process control CPUs, each of which interfaces with several individual pieces of process equipment. The first floor control computer also interfaces to another CPU for traffic control of the AGVs in main street. The AGVs communicate to the traffic control CPU through the I/O stations. The AGV receives its instructions from the I/O station. This is in contrast to the U.S.-manufactured Veeco and Flexible Manufacturing Systems AGVs, both of which communicate directly to their control computer via an infrared

link. The control computer on the second floor has a similar architecture.

In the factory computer control center, operators sit at a long console and monitor factory status via CRT monitors in the console. In front of the console is a large illuminated electronic board that schematically depicts the entire two-floor production process and the various pieces of equipment. Every bare wafer is marked and, although lots are usually tracked, individual wafers can be called up and located in the factory by the monitoring and tracking system.

Process data are collected by the system and analyzed. Dr. Komiya noted that as the human element has been removed, the process data have tended to exhibit a very tight distribution about the mean. The factory central computer also communicates with Mitsubishi's Kita-Itami Works. For instance, quality control data are sent to Kita-Itami for further analysis, the results of which are fed back to the Saijo factory computer.

Mitsubishi built all robots and AGVs in the factory as well as writing the factory automation software. It took Mitsubishi three years to complete the system.

Results of Automation

DATAQUEST was told that the 64K DRAM facility was obtaining a defect density of 0.1 defects/mask level/cm^2. This should be compared to a world class Class 100 facility that can obtain 0.5 defects/level/cm^2. Mitsubishi has paid much attention to the reduction of particulate levels in the fab. All robotic equipment and AGVs were designed to contribute minimum levels of particulates. Mitsubishi worked closely with the equipment vendors to minimize the equipment particulates and, further, the process equipment was cleaned before it was installed in the clean room.

Cycle time for the wafers for the first floor (wafer fabrication and probing) is about three weeks. This should be compared to the 6 to 10 weeks required for an average U.S. fab cycle, with 6 weeks being a very good cycle time. Cycle time for the second floor (assembly and test) is about one week.

Although Mitsubishi would not disclose its device yields, it indicated that automation resulted in about a 20 percent relative increase in yields. Mitsubishi also believes that the Saijo facility can produce the lowest-cost 64K DRAM in the world. Taking all factors into consideration, DATAQUEST estimates that this facility is obtaining yields of between 85 percent and 90 percent for 64K DRAMs. DATAQUEST also estimates that the factory capacity of 10 million parts per month corresponds to 20,000 wafer starts per month at these yields.

Joseph Grenier

PROCESS EQUIPMENT ISSUES - CLEANLINESS

- MOST PROCESS EQUIPMENT IS NOT WELL DESIGNED REGARDING ABILITY TO BE REGULARLY CLEANED IN PRODUCTION.
- IT IS COMMON THAT EQUIPMENT CANNOT BE CLEANED UP TO MEET ITS NEW CLEANLINESS PERFORMANCE, AFTER IN USE AND HAVING GROUND UP SILICON THROUGHOUT ITS WORKING PARTS.
- SOME PROCESS EQUIPMENT CANNOT BE CLEANED WITHOUT A PROCEDURE MORE LIKE MAJOR OVERHAUL THAN MAINTENANCE.

PROCESS EQUIPMENT ISSUES - CLEANLINESS

- THE INSTITUTE RECOMMENDS THIS EVALUATION PROCEDURE FOR PROCESS EQUIPMENT:
  - A) PASS 5000 WAFERS THROUGH THE MACHINE
  - B) MEASURE THE WAFER BREAKAGE RATE
  - C) CLEAN MACHINE BY MANUFACTURER'S RECOMMENDED MAINTENANCE PROCEDURE, MEASURE DOWN-TIME REQUIRED
  - D) THEN, MEASURE THE PARTICLE CONTRIBUTION PER WAFER-PASS THRU THE MACHINE
- WE BELIEVE JAPANESE DESIGNERS ARE AGGRESSIVELY WORKING ON CLEAN PROCESS EQUIPMENT, AND WILL COMPETE IN THE US MARKET ON THAT STRENGTH.

PROCESS EQUIPMENT - RETURN AIR BLOCKAGE

- THE NEW 100% LAMINAR CLEAN ROOMS HAVE 550 AIR CHANGES PER HOUR, COMPARED TO 150 AIR CHANGES PER HOUR IN OLDER FACILITIES
- PROCESS EQUIPMENT DESIGNERS MUST PROVIDE A RETURN-AIR BATH BENEATH THEIR MACHINES OF AT LEAST 10 INCHES, CLEAR
- BLOCKED RETURN AIR DESTROYS THE AERODYNAMIC BENEFITS OF THE CLASS 1 CLEAN ROOMS
- PERFORATED FLOORS ARE NOT THE ANSWER FOR RETURN AIR, SINCE 75% OF CLASS 1 FACILITIES USE SIDE-WALL RETURNS

PROCESS EQUIPMENT ISSUES - CLEANLINESS

- THE WORST CONTRIBUTOR TO YIELD LOSS WILL BE PROCESS EQUIPMENT THRU WAFER HANDLING AND INTERNAL DIRTINESS.
- MANUFACTURING OF COMPLEX 1-MICRON, LARGE AREA ULSI CHIPS WILL BE MOSTLY PACED BY PROCESS EQUIPMENT CLEANLINESS PERFORMANCE.
- USERS WILL MEASURE PROCESS EQUIPMENT CLEANLINESS BEFORE PURCHASE. WHERE IT DOES NOT MEET SPECIFICATION, THEY WILL NOT BE BUYING IT - REGARDLESS OF ITS PROCESSING PERFORMANCE.

CHARACTERIZATION PROGRESS DOWN THE DEFECT/CM^2/L LEARNING CURVE

- IN ORDER TO SUCCESSFULLY PROGRESS DOWN THE DEFECT/CM^2 CURVE, PLANT MUST BE ABLE TO ROUTINELY MEASURE WHERE THE ON-GOING MANUFACTURING D/CM^2/L IS SITUATED
- PRACTICE IN SMALL OPERATIONS (SUCH AS AEROSPACE) IS REGULAR DAILY PRODUCTION WITH DIE HAVING HIGHLY RECURRING PATTERNS, WHERE CIRCUIT DEFECTS CAN BE RESOLVED IN TESTING. POPULAR DIE IS DRAM IN LATEST MANUFACTURING PROCESS
- MANY PLANTS CONSTANTLY RUN SOME DRAM AS A TOOL FOR MANUFACTURING DIE YIELD IMPROVEMENT, EVEN WHEN IT IS NOT A SOLD PRODUCT

PROCESS EQUIPMENT ISSUES - INTEGRATION

- PREFER PROCESS EQUIPMENT BE INSTALLED PENETRATING THRU CLEAN ROOM WALL INTO SERVICE AISLE
- INTENT IS TO DO SERVICE AND REPAIR ON BACKSIDE, WITHOUT ENTERING CLEAN ROOM SIDE
- ONLY CONTROLS AND CASSETTE LOAD/UNLOAD STATIONS REMAIN IN THE CLEAN ROOMS

PROCESS EQUIPMENT ISSUES - AERODYNAMICS

- CURRENT MACHINE CONFIGURATIONS MAKE IT DIFFICULT TO GET CORRECT LAMINAR FLOW THRU BARE WAFER STATIONS AND TRANSPORT MECHANISMS
- CONTRIBUTES TO POOR PARTICLE PERFORMANCE OF MANY CURRENT MACHINES
- DESIGNERS NEED TO CONDUCT LAMINAR FLOW SMOKE STUDIES AROUND THEIR SPECIFIC MACHINE CONFIGURATIONS TO GET PARTICLE REMOVAL BENEFIT OF THE LAMINAR AIR

IN-PROCESS PARTICLE MEASUREMENTS

- USING NEW SURFACE-SCANNING PARTICLE MEASUREMENTS SYSTEMS TO CHARACTERIZE INCREASE OF PARTICLES ON A WAFER, THRU A PROCESS STEP
- SYSTEMS SEE SUB-MICRON PARTICLES ON BARE WAFERS, OR ON THIN-FILM LEVELS WAFERS WITH A NON-PATTERNED WAFER SURFACES
- SYSTEMS DO NOT WORK STRONGLY ON PATTERNED WAFER SURFACES
- NEXT-GENERATION SYSTEMS MIGHT BE ABLE TO LOOK AT PATTERNED SURFACES
- POSSIBLE TO QUANTITATIVELY MEASURE NUMBER OF PARTICLES PRESENT, BEFORE AND AFTER SOME PROCESS STEP
- USE SYSTEM TO CHARACTERIZE THE INCREASE IN PARTICLES ON A WAFER FOR EACH PROCESS WAFER HANDLING STEP
- PRACTICE IS TO INCLUDE, WITH PRODUCTION WAFER RUNS, A BARE CLEAN WAFER, FREE OF OXIDES AND PATTERNS
- THIS CHECK GOES THRU ALL WAFER HANDLING STEPS, INCLUDING INSERTION/REMOVAL FROM PROCESS EQUIPMENT
- PARTICLE BUDGET LIMITS ARE SET FOR EACH PROCESS EQUIPMENT
- BEFORE AND AFTER EACH PROCESS STEP, THESE WAFERS ARE MEASURED FOR PARTICLE POPULATION
- PARTICLE CONTRIBUTION PERFORMANCE IS MEASURED DAILY FOR EACH PROCESS
- PARTICLE CONTRIBUTION PERFORMANCE IS MEASURED TO REQUALIFY A PROCESS EQUIPMENT AFTER CLEANING OR REPAIR
- NOW BEING USED IN EVALUATING NEW PROCESS EQUIPMENT FOR PURCHASE

AUTOMATION

- STOP REWORK AND EXCESSIVE INSPECTION IN LITHOGRAPHY -- DO IT RIGHT THE FIRST TIME

PRODUCT CYCLE TIME

- SHORTER CYCLE TIMES HAVE SEVERAL BENEFITS
  - FASTER DIE YIELD IMPROVEMENT ON NEW PROCESS AND PRODUCTS
  - MINIMIZES EXPOSURE TIME TO PARTICLES
  - FASTER CUSTOMER RESPONSE IN CUSTOM AND PARTLY CUSTOM MARKET

PRODUCT CYCLE TIMES

- PLANTS ARE BEING PLANNED FOR FAST THRUPUT TIME OF WAFERS IN MANUFACTURING
- THRUPUT TIMES OF EIGHT WEEKS HAVE BEEN COMMON IN PAST
- LONG PERIODS WERE SPENT IN LITHOGRAPHY, WAITING FOR REWORKED WAFERS TO CATCH UP
- NEW PLANTS HAVE THRUPUT GOALS AT BETWEEN TWO AND THREE WEEK WAFER CYCLE TIMES, INCUDING WAFER SORT
- AGGRESSIVE WORK-IN-PROCESS MANAGEMENT WILL BE ADOPTED AS PART OF PHASE, AUTOMATION
- PLANTS ARE PLANNING RAMP-UP WITH 3 SHIFTS TO MINIMIZE THRUPUT TIME, NOT FOR CAPACITY

CHARACTERISTICS OF CLASS 1 ROOMS

- AERODYNAMIC DESIGN PRODUCES SIGNIFICANTLY BETTER ISOLATION BETWEEN OPERATOR TRAFFIC AND BARE WAFER AREAS.
- AERODYNAMIC FLOW OF LAMINAR AIR PROVIDES A HORIZONTAL AIR CURRENT COMPONENT, QUICKLY REMOVING PARTICLES GENERATED BY PROCESS EQUIPMENT.
- BARE WAFER AREA RECOVERS FROM MAJOR PARTICLE EVENT WITH 6 SECONDS
- AISLEWAYS ARE CLASS 10. LOCAL MANUFACTURING WORK-FLOW DONE WITHBOUT "PROTECTIVE" BOXING
- BOXING USED ONLY FOR WIP STORAGE AND LONG-DISTANCE TRAVEL
- CHEMICAL DELIVERY DONE VIA SERVICE AISLES

PROCESS EQUIPMENT AUTOMATION

- EACH PROCESS EQUIPMENT INTRINSICALLY AUTOMATED:
  - CASSETTE TO CASSETTE INTERFACE
  - INTERNAL WAFER TRANSPORT BY MECHANISM, TRACK OR ROBOTIC AS APPROPRIATE
  - MICROCOMPUTER CONTROLLED FOR PROCESS STABILITY
  - BUILT-IN DIAGNOSTICS
- OVERALL FAB WORK-IN-PROCESS COMPUTER MANAGEMENT SYSTEM, WITH DISTRIBUTED WIP CONTROL AND CASSETTE HOLD STATIONS
- CASSETTE TO QUARTZ TRANSFERS BY PRECISION SMART-EYED ROBOT

MEASUREMENTS

- A MAJOR IMPROVEMENT IS ALL PROCESS-CRITICAL FACILITY PARAMETERS ARE CONTINUOUSLY MEASURED AND RECORDED, DETECTING PROBLEMS WHEN THEY START

CLASS 1 CLEAN ROOMS

- THESE NEW PLANTS HAVE CLASS 1 IN THE BARE WAFER AREAS AND CLASS 10 IN THE AISLEWAYS
- ROOMS HAVE 100% LAMINAR COVERAGE, AND AERODYNAMIC FLOW AROUND THE PROCESS EQUIPMENT
- THE ROOMS ARE MUCH CLEANER THAN PRIOR PRACTICE:

CLASS OF PRACTICE	CRITICAL PARTICLE SIZE	CLEANLINESS IMPROVEMENT
CLASS 100 (FED STD 209B)	0.5 MICRONS	1 TIME
CLASS 10	0.5 MICRONS	10 TIMES
CLASS 10	0.2 MICRONS	100 TIMES
CLASS 1	0.2 MICRONS	1000 TIMES

PLANT DESIGN/OPERATION

- THE WORLD-CLASS PLANT DESIGNS ARE APPROACHED AS AN INTEGRATED SYSTEMS PROBLEM
- THE ORGANIZATION OF MANUFACTURING OPERATIONS, MATERIALS HANDLING, PERSONNEL PRACTICES, AND FACILITY DESIGN ARE A SINGLE SYSTEMS PROBLEM
- THESE NEW PLANTS ARE DESIGNED SO THAT THE FACILITY IS REMOVED AS A POSSIBLE PROCESS STABILITY OR DIE-YIELD PROBLEM

KISS

- "KEEP IT SIMPLE"
- FACILITIES NOW ARE DELIBERATELY DESIGNED TO STAY ON SPECIFICATION ALL THE TIME, AND NOT BE A PROCESS-ISSUE
- EXAMPLES OF NON-ISSUE PROCESS-CRITICAL SYSTEMS:
  - oo LITHOGRAPHY RH AND TEMPERATURE ARE HELD CONSTANT REGARDLESS OF OUTSIDE CONDITIONS
  - oo VIBRATION, THROUGHOUT THE FAB AREA
  - oo AIRBORNE PARTICLE CLEANLINESS
  - oo PROCESS GAS PURITY
  - oo DI WATER PURITY
  - oo INCOMING CHEMICALS PURITY

RELATIVE IMPORTANCE OF CONTAMINATION SOURCES IN WORLD-CLASS PRACTICE (CURRENT INSTITUTE OPINION)

0) HANDLING OF WAFERS BY OPERATORS WITH VACUUM WANDS AND TWEEZERS, AND ROLL-OVER CASSETTE-TO-CASSETTE TRANSFER. (NOT ALLOWED IN WORLD-CLASS PRACTICE)

1) MECHANICAL HANDLING OF WAFERS

2) PROCESS EQUIPMENT INTERNAL DIRTINESS

3) PERSONNEL, WHEN NOT FOLLOWING PROCEDURES NEAR BARE WAFERS

4) ULTRAPURE WATER SYSTEM

5) ULTRAPURE CHEMICALS USED IN PROCESS

6) JANITORIAL CLEANING IN ROOMS

7) PERSONNEL, WHEN FOLLOWING PROCEDURES

8) NEW FILTERS

9) TRANSFER OF WAFERS BETWEEN AISLES, BY CLEAN PROTECTIVE BOXING

10) TRANSFER OF WAFERS WITHIN CLASS 1/10 PROCESSING AISLES WITHOUT BOXING

11) CLEAN ROOM LAMINAR ENVIRONMENT

12) ULTRAPURE GAS SYSTEMS

THE YIELD CHALLENGE

- THE PERIOD 1986 TO 1996 WILL SEE AT LEAST THREE MAJOR CYCLES OF TECHNOLOGY UPGRADE IN MANUFACTURING INCLUDING:
  - 1 MICRON BY 1990
  - 0.7 MICRON BY 1995
- THE PLANTS BEING DESIGNED TODAY ARE EXPECTED TO PERFORM COMPETITIVELY ON 1996 TECHNOLOGY, WITH THE SAME FACILITY
- THE GREATEST CHALLENGE WILL BE DEFECT/CM^2 PERFORMANCE IN MANUFACTURING, AS THE INDUSTRY GOES TO 1 MICRON AND BELOW
- DIE YIELD MODELING SHOWS MANUFACTURING TECHNOLOGY MUST BE GREATLY IMPROVED OVER TODAY'S PRACTICE, BY AT LEAST 10 TIMES IN DEFECTS/CM^2 BEFORE 1990
- FIGURE SHOWS TYPICAL CURRENT MANUFACTURING PERFORMANCE OF 0.5 D/CM^2 AT 0.2 MICRONS DROPS BELOW 10% YIELD BEFORE 1.25 MICRONS
- NEXT FIGURE SHOWS D/CM^2 PERFORMANCE REQUIRED TO MAINTAIN 10% DIE YIELD

NEXT GENERATION "WORLD CLASS" PLANTS

- PLANT DESIGN/OPERATION
- CLASS 1 CLEAN AREAS
- AUTOMATION
- PRODUCT CYCLE TIME
- IN-PROCESS PARTICLE AND DEFECT MEASUREMENTS
- DEFECT/CM^2 CHARACTERIZATION

NEW PRACTICES IN LEADING-EDGE MANUFACTURING

- THE CHALLENGE IN MANUFACTURING TECHNOLOGY (YIELD)
- WORLD CLASS PLANT FEATURES
- NEW OPERATING PRACTICES
- PROCESS EQUIPMENT ISSUES

TREND OF INDUSTRY - THE WORLD-CLASS PLAYERS

- INDUSTRY IS NOW BUILDING A NEW LEVEL OF MICROELECTRONIC PLANT, THE "WORLD-CLASS" OR "CLASS 1" PLANT
- PURPOSE IS TO ENABLE LEADING-EDGE MERCHANT MANUFACTURING COMPANIES TO COMPETE PROFITABLY, WORLD-WIDE, ON MICROELECTRONICS COMING UP IN THE NEXT 6 YEARS - THE "ULSI" CHIPS
- THE ESSENCE OF ECONOMIC SUCCESS OF LEADING-EDGE MERCHANT COMPANY IN ULSI PRACTICE IS DIE YIELD AND PROCESS UPGRADE FLEXIBILITY
- ALL INSTITUTE-INVOLVED NEW MICROELECTRONIC PLANTS STARTED IN LAST TWO YEARS HAVE BEEN DESIGNED TO BE WORLD CLASS, I.E., MAXIMUM UNCOMPROMISING EFFORT FOR DIE YIELD
- THIS HAS COVERED OVER A DOZEN MERCHANT COMPANIES FROM THE LARGEST TO THE LATEST START-UPS

Nielsen Dataquest

GROWING PAINS OF SURFACE MOUNT TECHNOLOGY

Nikita Andreiev
Director, Educational Group
AWI

Mr. Andreiev is Director of the Educational Group at AWI. Previously, he was Editor-in-Chief of Electronic Packaging and Production magazine. He is recognized as an authority on the latest advances in SMT, CAD/CAM, and other high-technology packaging and production areas. Mr. Andreiev has also held senior editorial positions with other industry publications including Control Engineering, Assembly Engineering, and EDN. In addition, he has held design engineering positions with several companies and worked on projects such as instrumentation design, high-energy accelerator design, and the lunar module. Mr. Andreiev received a degree in Electrical Engineering from the City College of New York and has worked toward a masters degree in Computer Science at the Polytechnic Institute of Brooklyn.

Dataquest Incorporated
SEMICONDUCTOR EQUIPMENT AND MATERIALS INDUSTRY SERVICE CONFERENCE
October 14-16, 1985
Tucson, Arizona

NIKITA ANDREIEV
AWI CORPORATION

GROWING PAINS OF SURFACE MOUNT TECHNOLOGY

1. What happened to the computer industry and the demand for ICs, and why?

2. The "Death Valley" curve. (Slides 1,2)

3. Wanted: An identification of a future trend, a "fad" if you will, to replace the boom experienced in the past by microprocessor-based products. (Slides 3,4)

4. Current changes are the results of a recognition by industry leaders (IBM, H-P, TEK etc.) that in order to survive, they must change. In particular, the changes must come in the manufacturing environment and methods. (Slides 5,6,7)

5. The technology is here -- it's SMT; what is missing is:
   a. Experience (DO NOT CONFUSE THIS WITH TALENT--PLENTY OF THAT!)
   c. Availability of information
   d. Availability of components
   e. Agreement on standards (e.g. package shapes, pinouts, etc.)

6. Methods to assure growth, or at least the keeping of head above water (also known as survival), in the future:
   a. Automation
   b. Automation
   c. Automation

7. The changes are already singling out future growth markets that will depend on surface mount technology:
   a. Telecommunications
   b. Military electronics
   c. Computers
   d. Consumer electronics
   e. Industrial controls
   (Slides 12,13,14)

8. SMT is not a fad, it is a future fact of life. In fact, the "fads" will be dependent on SMT for commercial viability. (Same goes for COB and TAB.) However, none of these will have the panoramic sweep, and the short life, of a fad but will be the backbone of all future electronics manufacturing until something else comes up (SMT also follows the Death Valley curve law!).

9. In the meantime, what could be the potential future "fad" contest winners?
   Some of the suggested ones are:
   a. GaAs technology and products based on it
   b. Software
   c. PALs
   d. Gate Arrays

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THE GROWING PAINS OF SMT

N. Andreiev

AWI

Before I get to the question of what happened to the computer industry, let me ask you a strange question -- do you think that the electronic high tech industry is a fashion fad? The reason for this question will become apparent in a couple of minutes.

Now, what happened? Why did the bottom fall out of the computer industry with the result that it dragged down with it the semiconductor, the component, the connector industries and many others. Strangely enough, a hint of an answer came from an unexpected quarter -- Great Britain!

We had recently visited the UK (the UK includes England, Wales, Scotland and Nothern Ireland) as guest of the Crown for the purpose of evaluating the UK as a site for American investment. Basically, I was a guest of the Invest-in-Britain folks. While asking a number of questions relating to investment, I also had a chance to ask some of my own. The questions that I wanted answers to were: What caused the recent downturn in the demand for computers?, What is the health of the semiconductor industry? and What is the status of SMT?

Let me get to the first question last. Regarding the other two questions, it was evident that most high-tech companies in the UK that were part of my itinerary, both local and U.S.-owned, were gearing up for automation through very large capital expenditure plans (Prestwick Circuits, for example, is spending upwards of £10,000,000 on an annual gross of about £18 million) to face more bad times ahead, primarily from foreign competition. In fact, most of them say that the automation frenzy is primarily to allow them to keep their European markets in the future; they are not even talking of increasing their market share. But in general, the Brits view SMT technology favorably, especially companies like ICL (the second largest computer manufacturer in the UK). We will come back to that company in a second.

After two full weeks of information gathering, the last stop was at a bank -- the Midland Bank, in fact -- to get some last minute investment information; remember, this was still a part of Invest-in-Britain tour. This is where I was introduced to the "Death Valley" curve that went a long way in explaining what might have happened to the computer industry and why.

Let me share this information with you now.

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(SLIDE 1)

This is the "Death Valley" curve. For those of you who are into finances this is nothing new. What is interesting however, is the fact that both the Brits -- Brian Warnes of the Midland Bank, in particular -- and Uncle Sam (in a 1982 report by the U.S. General Accounting Office to Senator Bentsen on venture capital status in the U.S.) have arrived at exactly the same curve, independently.

Basically, the curve shows a typical venture company equity over a period of 4-5 years. It is assumed that the vertical axis starts at the time when the product has been developed and the owner is starting his own company. Notice, that he starts with $10-20 k (usually borrowed from relatives), and immediately starts losing money. And keeps losing for about three years. Those of you who went through the experience will undoubtedly know that this is also the period when you run out of money and need to borrow from the bank to keep going. Unfortunately, this is also the time when no bank will lend you any. To make a long story short, the Midland Bank is one of those who will because Warnes worked out a plan, that if adhered to will assure that a new venture company eventually gets into the black and, equally important, if a company is floundering the bank will pour money into it and turn it around. Examples are BL and ICL mentioned earlier.

An interesting fact about this bank is that in its portfolio of companies that it guides, there is not a single one that we would consider a high tech company. Let us look again at the "Death Valley" curve to see why. In a normal life cycle of a product, the curve after an initial rise will eventually flatten out as the product matures, then start a gradual downturn until it reaches a plateau. According to the bank, the top part of the curve -- the most profitable part -- can be extended by the introduction of a new product at about the time the original product takes off. This can be repeated as many times as the market will absorb.

(SLIDE 2)

Notice the multiple product introductions that maintain high sales volume. Suppose the products that are introduced are all based on a particular idea, such as a microprocessor! Do you begin to see the connection? Eventually, the companies will run out of ideas and the users will run out of interest. In other words the "fad" will have played itself out. Thus, to the British banks our high tech industry is just a 'passing fad.' There is a lot of truth to that because the Intels, the IBMs, the Ataris etc. have followed this curve to a tee. Because of its volatility (even though the profits could be enormous, for the bank this is too risky a proposition!) the banks will not touch high tech for their portfolios.

By extrapolation of the above idea what is needed now is the identification of the next boom based on as yet unknown idea or a product to get the ball rolling again. We will return to this rather interesting subject at the end of this presentation.

During all this turmoil, chapter 11s, bankrupcies, layoffs etc., a quiet revolution is taking place -- the emergence of surface mount technology. The biggest battle that SMT is facing is the recognition by the industry that in order to survive, it must change. Fortunately, industry leaders like IBM, TEK, Delco, H-P and others, have either taken active steps toward SMT implementation or are in the process of doing it. In particular, the changes must be made in the manufacturing methods.

(SLIDE 3)

SMT is NOT a variation of the familiar through the hole manufacturing and assembly technology, it is a brand new method. Unfortunately, because of the many similarities that SMT shares with the older technology it is replacing it is not treated as new. Let us look at its salient features on the next few slides.

(SLIDE 4,5,6,7)

A positive fact about SMT is that the technology is already here. What is missing however is:

- o EXPERIENCE
- o AVAILABILTY OF INFORMATION
- o AVAILABILITY OF COMPONENTS
- o AGREEMENT ON STANDARDS

Do not confuse experience with talent. There are plenty of knowledgeable manufacturing engineers around, it is just that they are facing a brand new technology. Basically, they are in the same position that the Wright brothers were at Kitty Hawk 82 years ago. They had a plane but there was nobody in the world who could teach them to fly it. But that is changing today with SMT.

Information is beginning to show up in articles, books, conferences etc. A small number of companies are even specializing in educating the industry. For example SMD Technology, AWI, Lake Publishing are all in it.

Components too are on the increase. Three years ago there were about 270,000 individual component numbers for through hole components and a dozen or so numbers for SMT (at least in this country). Last year D. Brown listed over 20,000 SMT components in its book. AWI currently lists about 20,000 discrete SMT components (over 200,000 if passives are included).

Finally, standards seem to be in the process of being developed for different component packaging configuration -- both active and passive ones. So things are looking up.

Because the SMT technology is uniquely suited for automated assembly methods, recognition of the fact that automation is what will let us compete against foreign competition onslaught, cannot be overemphasized. In fact, the use of multiple word AUTOMATION in your program outline is intentional to drive the point home. The similarities between SMT and the traditional technology, unfortunately, are too close as the next slides will show.

(SLIDES 8,9,10,11)

The changes that SMT is forcing are already singling out future growth market.

- o TELECOMMUNICATIONS
- o MILITARY ELECTRONICS
- o COMPUTERS
- o CONSUMER ELECTRONICS
- o INDUSTRIAL CONTROLS

(SLIDES 12,13,14)

Most of them should be familiar to you, except the last one. The last one was a surprise to us at AWI since we found out that fact from our workshop attendance figures.

(SLIDE 14)

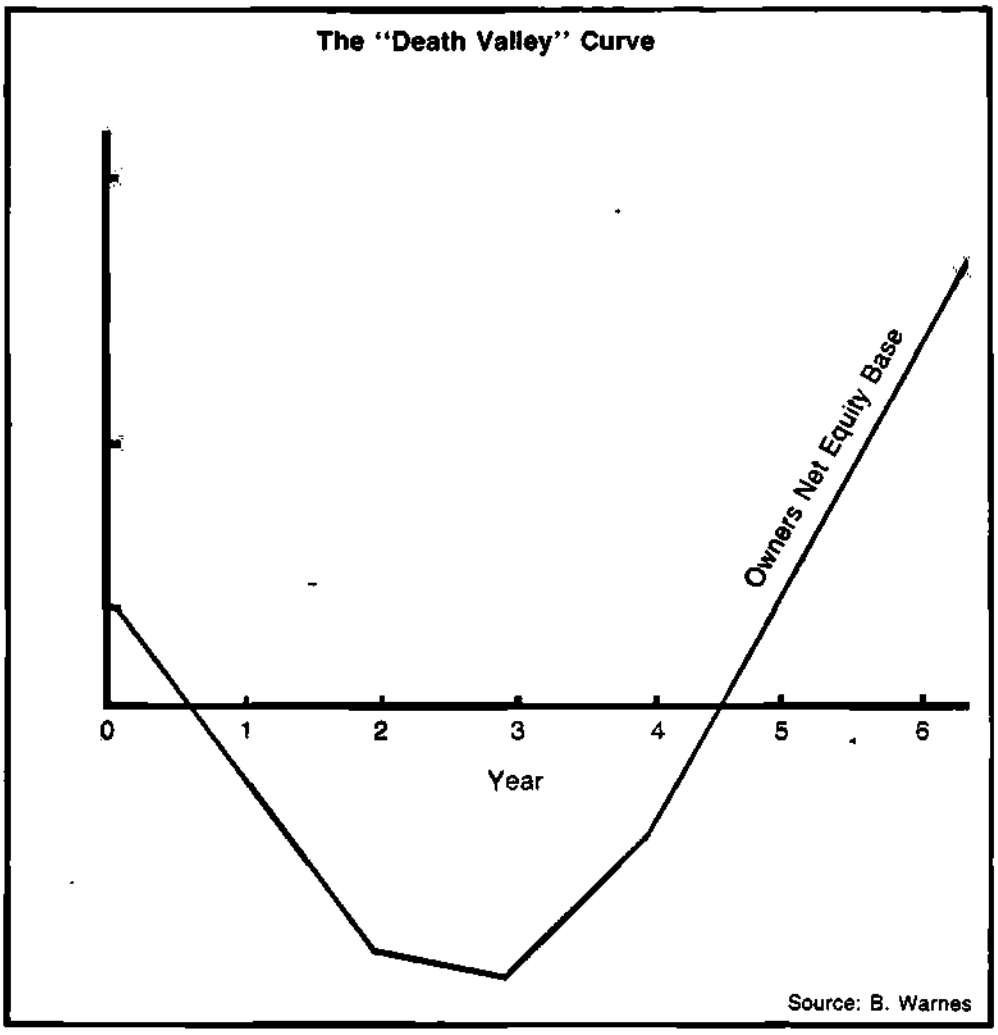
In general, British bank notwithstanding SMT is not a fad -- it is a future fact of life. In fact, all future electronic "fads" will be dependent on SMT for commercial viability and ability to compete. We should take the Japanese quite seriously. COB and TAB technologies will be offshoots of SMT, but none of those will have the panoramic sweep, and the short life, that characterizes a fad. SMT will be the backbone of electronics manufacturing until something else comes up to replace it. Remember, SMT is not immune to the Death Valley curve law and will follow a similar route -- later.

Let us go back for a second to the subject we left off at the very beginning -- that of finding the new boom candidate. Just to give you some food for thought, here are some suggestions on the potential future "fads" contest winners:

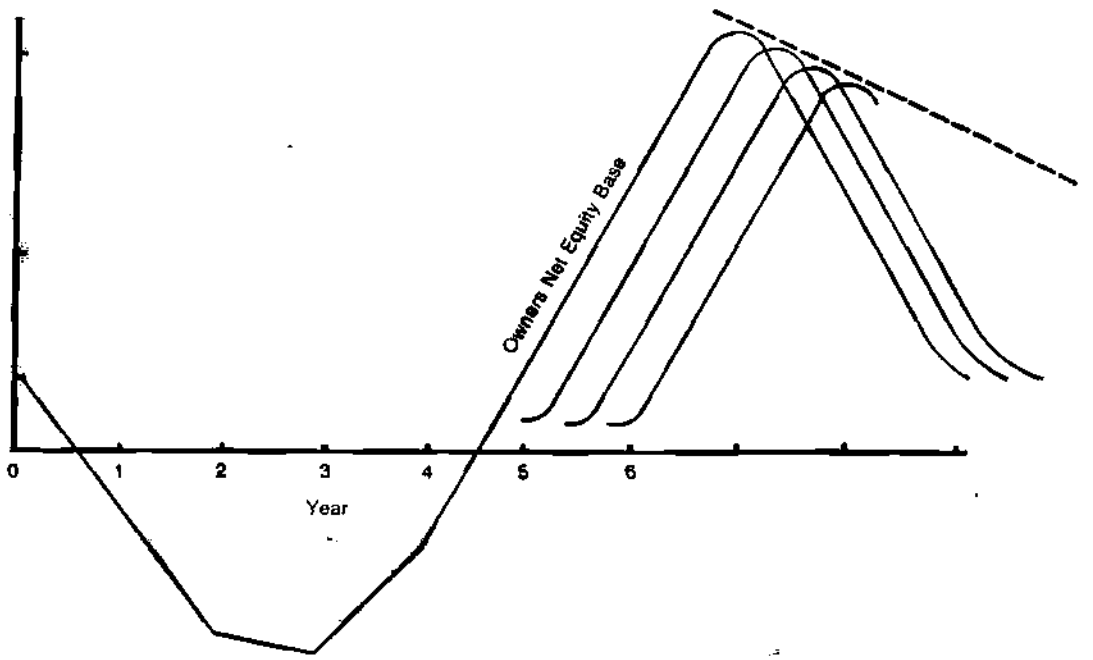
- GaAs TECHNOLOGY AND PRODUCTS BASED ON IT
- SOFTWARE, AND MANUFACTURING SOFTWARE IN PARTICULAR
- PALS AND GATE ARRAYS
- SUPER HIGH INTEGRATION (MAY REPLACE PCBs)

Thank you for listening to this presentation; I believe we have a few minutes left for the Q&A period.

THE END


The "Death Valley" Curve
Owners Net Equity Base
0
1
2
3
4
5
6
Year
Source: B. Warnes

The "Death Valley" Curve



Source: B Warnes

SURFACE MOUNT TECHNOLOGY
IS
NEW COMPONENT PACKAGES
AND
NEW MANUFACTURING
TECHNIQUES

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CHANGES ARE REQUIRED TO ACHIEVE THESE BENEFITS:

- Manufacturing
- Design

COMPETITIVE ADVANTAGES OF SURFACE-MOUNT ASSEMBLY

— Smaller Size

— Increased Functions Per Area

— Greater Profits

— Higher Electronic Performance

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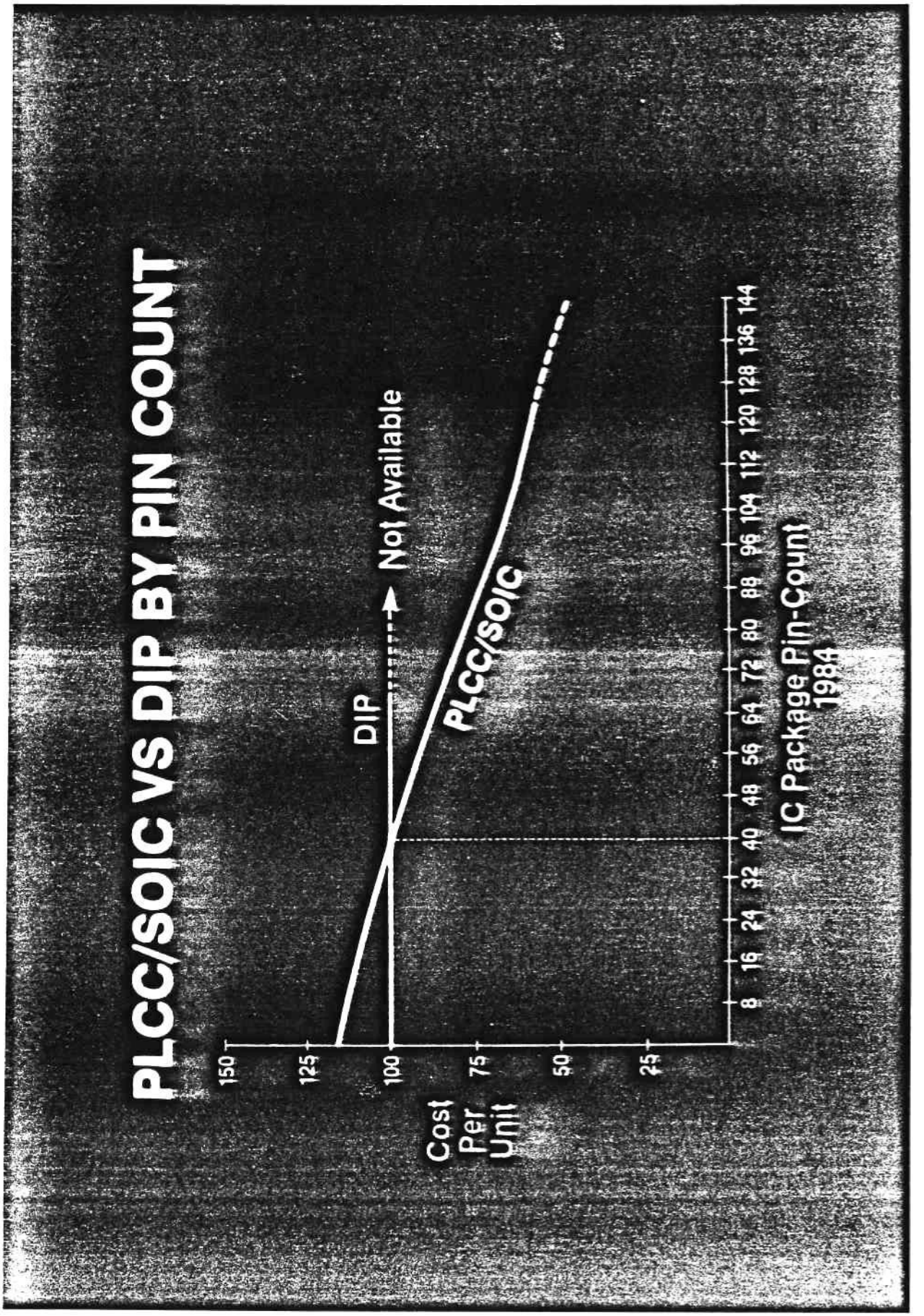
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Cost Per Unit
150
125
100
75
50
25
DIP
Not Available
PLCC/SOIC
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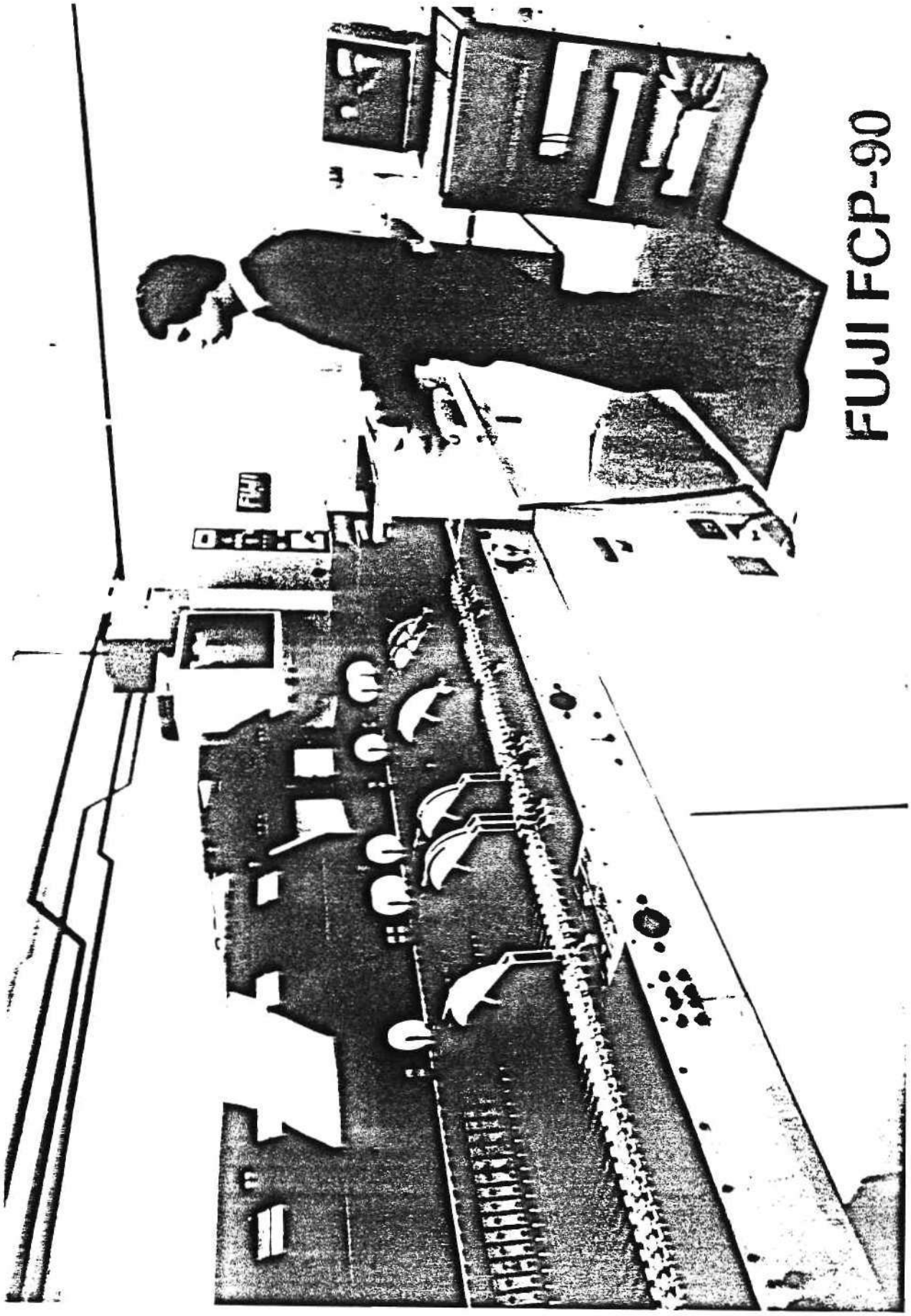
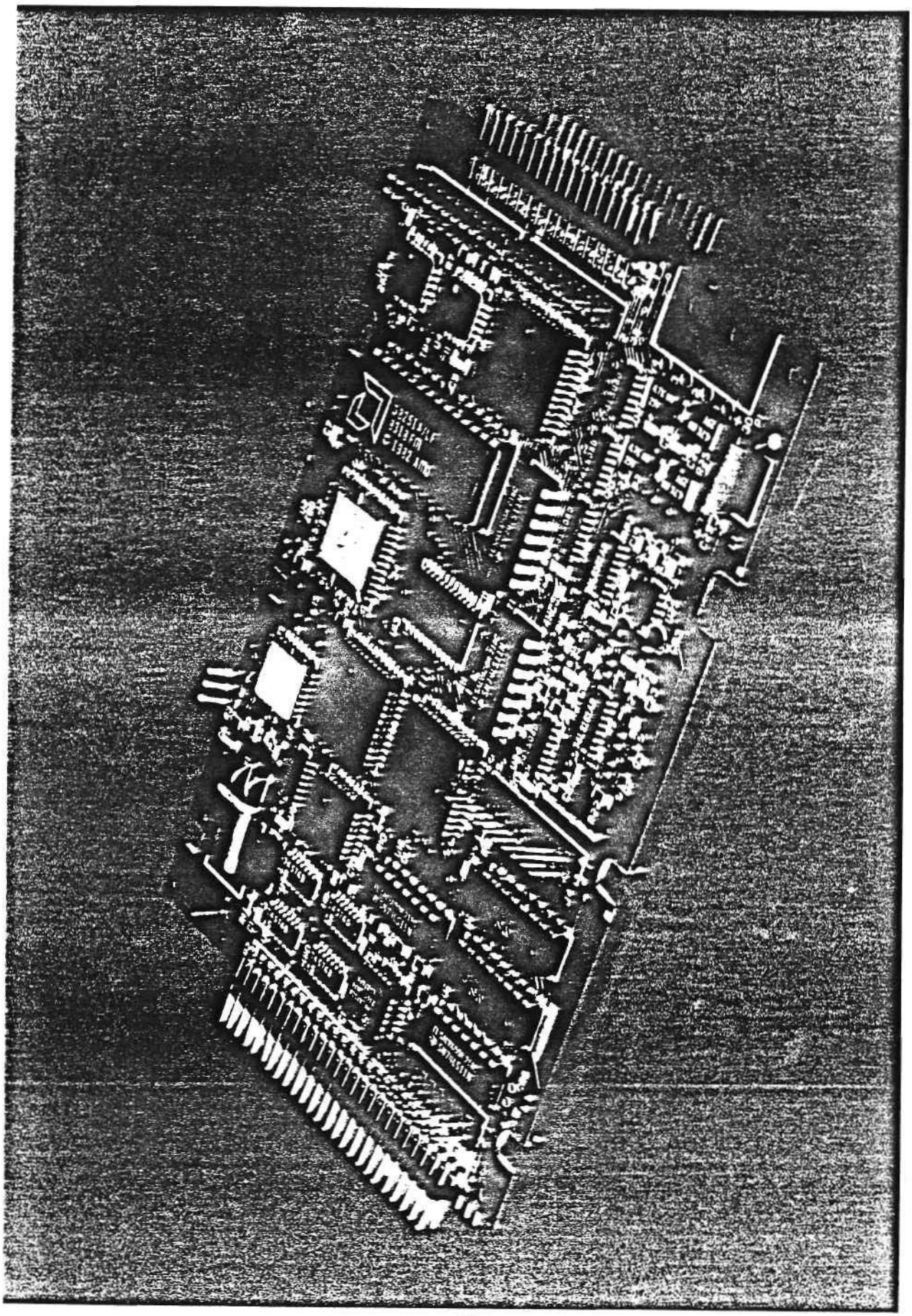
IC Package Pin-Count
1984

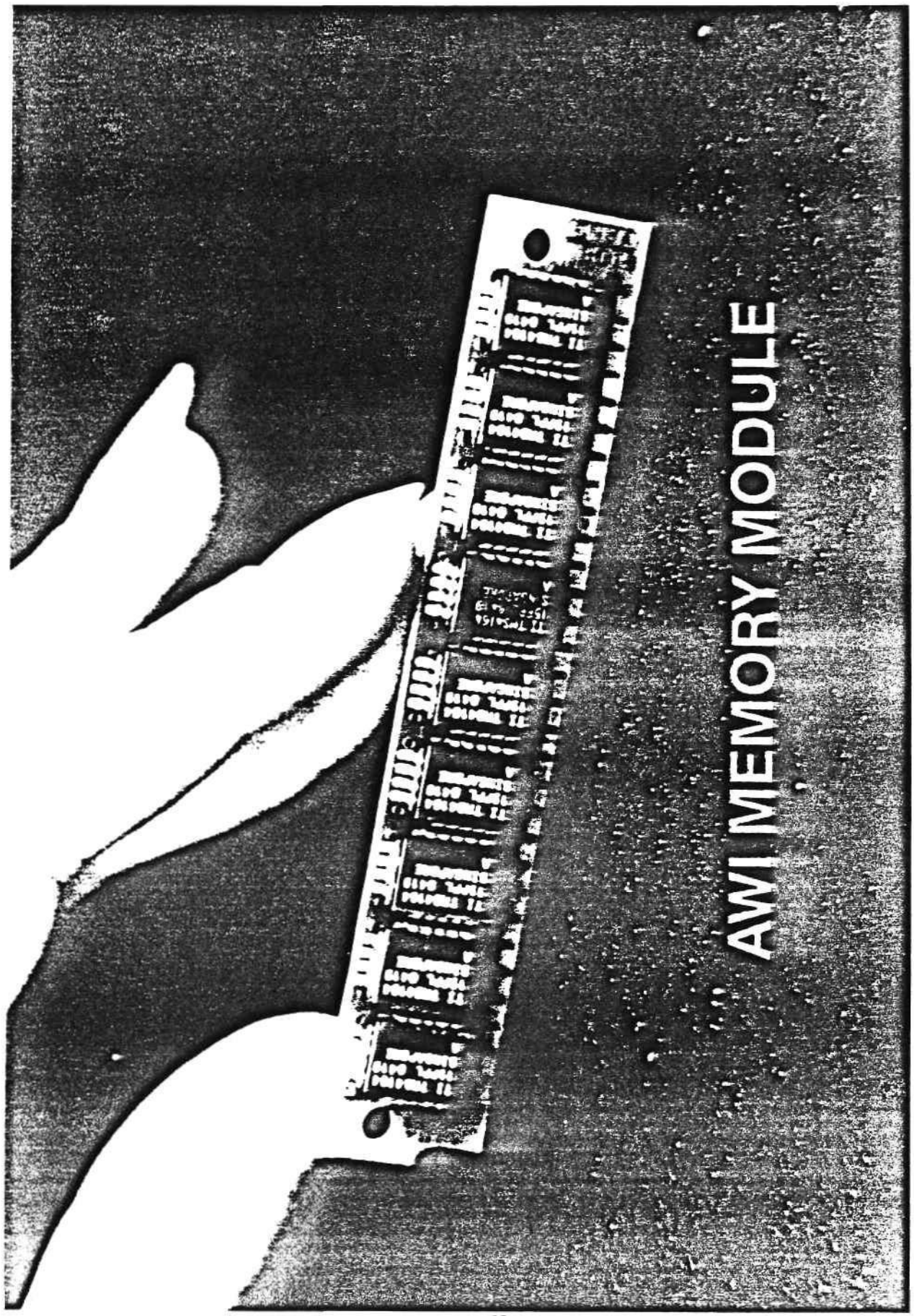
H-P 9920

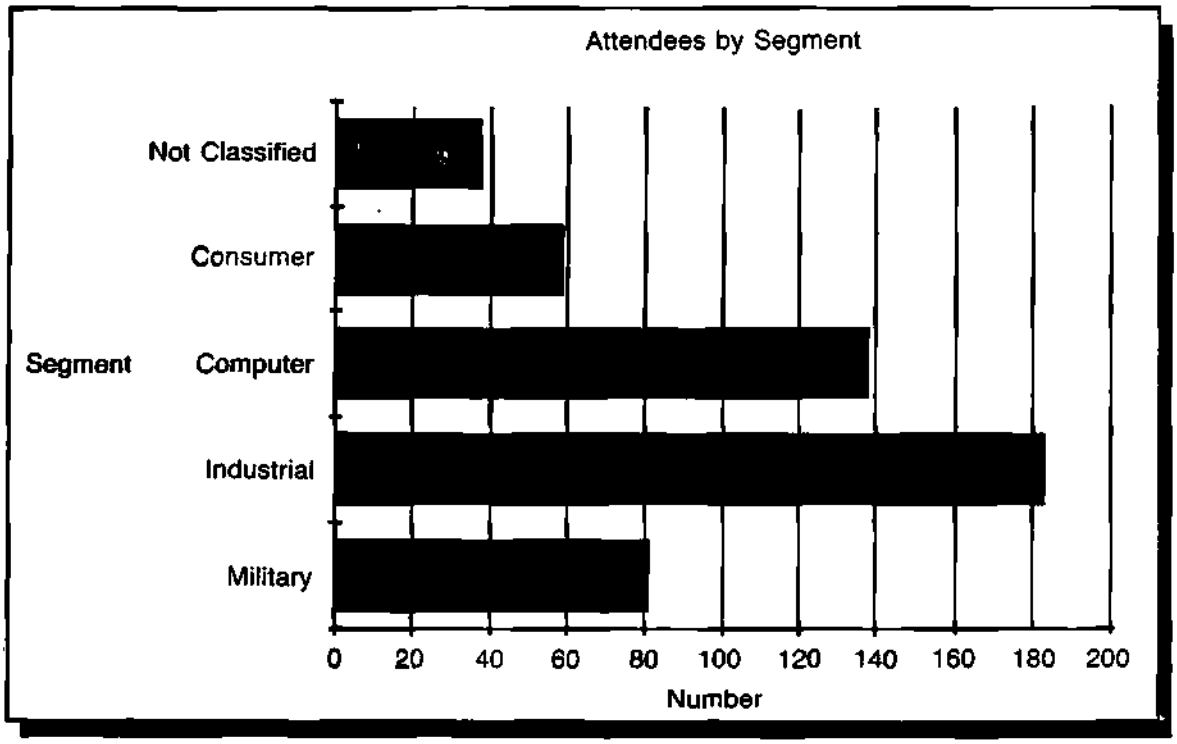
CALAY VO-3


FUJI FCP-90

MPS 500-2
EMHART




AWI MEMORY MODULE


Attendees by Segment
Not Classified
Consumer
Computer
Industrial
Military
Segment
0
20
40
60
80
100
120
140
160
180
200
Number

SORCE: AWI

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SEMICONDUCTOR FACTORY AUTOMATION OVERVIEW

Joe Grenier
Senior Industry Analyst
Semiconductor Equipment and Materials Industry Service
Dataquest Incorporated

Mr. Grenier is a Senior Industry Analyst for Dataquest's Semiconductor Equipment and Materials Service. He is responsible for analyzing the market environment and future technology trends. Prior to joining Dataquest, he was Product Marketing Manager at GCA Corporation, where he managed marketing activities for the reactive ion etch program. He was also International Marketing Manager at GCA, and was responsible for the overseas marketing of wafer processing equipment. Previously, he worked as a Product Manager at Varian Associates/Instrument Division, as a Systems Engineer at the USAF Satellite Test Center, and as a Test Engineer at General Motors' Noise and Vibration Laboratory. Mr. Grenier received a B.S.E.E. degree from the University of Detroit and an M.B.A. degree from the University of Santa Clara.

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AUTOMATION--
WHERE ARE WE?

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AUTOMATION

- SOFT AUTOMATION
  - LEVEL 1--WORK CELL
    (CTX, ISITEC, MICROVAX, QRONOS)
  - LEVEL 2--AREA MANAGEMENT/CIM
    (HP, CONSILIUM, I.P. SHARP, SENTRY, QRONOS)
  - LEVEL 3--CORPORATE/MRP
    (QRONOS)
- HARD AUTOMATION
  - WAFER TRANSPORT SYSTEMS
  - AGVs
  - ROBOTICS

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CIM

- FACTORY AREA MANAGEMENT
- COMPLEMENTS MRP
- PAPERLESS
- GENERALLY MODULAR SOFTWARE PACKAGES
- $500,000 TO $1 MILLION COST

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COMETS MODULES

USED FOR:

- SHOP FLOOR CONTROL
  - COSTING
  - WIP TRACKING
  - INVENTORY TRACKING
  - CAPACITY PLANNING AND SCHEDULING
- QUALITY AND ENGINEERING MANAGEMENT
  - ENGINEERING DATA COLLECTION
  - ENGINEERING DATA ANALYSIS
  - FACTORY COMMUNICATIONS

COMETS MODULES (Continued)

USED FOR:

- EQUIPMENT/FACILITIES MANAGEMENT
  - FACILITY MONITORING
  - NON-LOT TRACKING
  - PARTS INVENTORY TRACKING
- PROCESS CONTROL AND AUTOMATION
  - ON-LINE SPECIFICATIONS
  - PROCESS AUTOMATION MANAGEMENT

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CONSILIUM

- FOUNDED IN 1978
- 1984 SALES $7 MILLION
- COMETS
  - TWELVE MODULES THAT RUN ON VAX SERIES
- CUSTOMERS
  - EIGHT OF TEN TOP SEMICONDUCTOR COMPANIES
  - MANY CAPTIVES
  - MORE THAN 45 CLIENTS
- NEW MARKETS--PHARMACEUTICALS, COSMETICS

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SENTRY / SCHLUMBERGER

- INCYTE II
  - DEVELOPED IN 1980 BY FAIRCHILD ADVANCED RESEARCH LAB
- ELEVEN SOFTWARE MODULES THAT RUN ON VAX SERIES
- TWELVE FAIRCHILD INSTALLATIONS
  - FRONT END--SEVEN, BACK END--FIVE
- LOCATED IN: SOUTH PORTLAND, PUYALLUP, PALO ALTO; WASSERBURG, WEST GERMANY
- COMMERCIAL MARKETING, JANUARY 1985

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HEWLETT-PACKARD

- ACQUIRED SMC IN 1982
  - SEMICONDUCTOR PRODUCTIVITY NETWORK OPERATIONS
- 1984 SALES OF $5 MILLION
- ELEVEN MODULES THAT RUN ON HP COMPUTERS
- HAS 35 CUSTOMERS WITH 93 INSTALLATIONS WORLDWIDE
  - ASSEMBLY IN FAR EAST--20
  - FRONT END--73

HEWLETT-PACKARD

- UNITED STATES--18 COMPANIES
  - INCLUDES AT&T, INTEL, INT. RECTIFIER, NORTHERN TELECOM, RCA
- JAPAN--6 COMPANIES
  - INCLUDES MATSUSHITA, RICOH, SONY, TOKYO SANYO
  - FULLY AUTOMATED FACILITY WITH ROBOTS
- EUROPE--5 COMPANIES
  - INCLUDES AMI, GE, THOMPSON
- ROW--6 COMPANIES
  - INCLUDES AT&T, SAMSUNG, UMC

I.P. SHARP ASSOCIATES

- CANADIAN COMPANY FOUNDED IN 1964
- 1984 SALES $60 MILLION/$4 MILLION
- I.P. SHARP/GE JOINT PROJECT IN 1978→PROMIS
- MULTI-MODULE PACKAGE RUN ON VAX SERIES
- GE, MICROREL, McDONNELL DOUGLAS, ROCKWELL, TI
- $2 MILLION GRANT FROM NRC OF CANADA

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QRONOS

- FOUNDED IN 1984
- ONLY CIM COMPANY TO PROVIDE ALL THREE LEVELS OF SOFTWARE
- RUNS ON IBM COMPUTERS
- FIRST RELEASES DUE MID-1986

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CTX INTERNATIONAL

- FOUNDED IN 1979, ACQUIRED BY MOTOROLA IN 1984
- CTX 4000 CIM SYSTEM
  - OFFERED SINCE 1979
  - PROPRIETARY HARDWARE
  - TEN IN U.S., FOUR IN JAPAN
  - DEEMPHASIZING IN UNITED STATES
- CTX 1000, CTX 2000
  - LEVEL 1 USE
  - INTRODUCED IN 1985
  - FIVE IN UNITED STATES

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OTHER

- BTU ENGINEERING
  - FASTRACK CIM SYSTEM
- KULICKE AND SOFFA
  - INTRODUCED IN 1985
  - LEVEL 1 SOFTWARE/HARDWARE FOR ASSEMBLY WORK CELL
  - INTERFACES TO LEVEL 2 CIM SOFTWARE
- NSC/DEC
  - ANNOUNCED PROJECT ODYSSEY IN 1985
  - UNISECS/UNICYCLE

WAFER TRANSPORT SYSTEMS

- NACOM
- VARIAN
- TRANSLOGIC
- PROGRAMATION
- SHUTTLEWORTH

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WAFER TRANSPORT SYSTEMS

- NACOM
  - CARRIAGE MAGNETICALLY COUPLED TO ELECTRIC CAR
  - EXTRUDED ALUMINUM TRACK
  - INNER/OUTER TUNNEL CONCEPT
  - TEN SYSTEMS INSTALLED
- VARIAN
  - MOTORIZED ELECTRIC CAR
  - STAINLESS STEEL RODS (TWO)
  - TUNNEL
  - INDEFINITELY ON HOLD

WAFER TRANSPORT SYSTEMS

- TRANSLOGIC
  - MOTORIZED ELECTRIC CAR
  - EXTRUDED ALUMINUM TRACK
  - NO TUNNEL
  - MOSTEK (UNDER EVALUATION)
  - SIGNETICS (MASK AREA)
  - CINCINNATI-MILACRON (SILICON MATERIALS)

WAFER TRANSPORT SYSTEMS

- PROGRAMATION
  - START-UP COMPANY
  - BATTERY-POWERED CAR
  - MONORAIL TRACK
  - TUNNEL
  - MOSTEK (UNDER EVALUATION)
  - NORTHERN TELECOM (PHOTOBAY)

WAFER TRANSPORT SYSTEMS

- SHUTTLEWORTH
  - ROLLER CONVEYER SYSTEM
  - DRIVE BELTS FROM POWERED SHAFT ROTATE ROLLERS
  - TUNNEL
  - MOSTEK (UNDER EVALUATION)
  - TI (WAFER POLISHING AREA)
  - FIVE TO TEN INSTALLATIONS WORLDWIDE

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AUTOMATICALLY GUIDED VEHICLES (AGVs)

- FLEXIBLE MANUFACTURING SYSTEMS
- VEECO
- YOKOGAWA HEWLETT-PACKARD
- JAPANESE (DAIFUKU, MATSUSHITA, MITSUBISHI, SHARP)

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FLEXIBLE MANUFACTURING SYSTEMS

- SYSTEM COMPONENTS
  - MOBILE TRANSPORT UNIT
  - DOCKING MODULE
  - CENTRAL CONTROL COMPUTER
  - INTELLIGENT WIP STATION
  - $450,000 (MTU, TWO WIPs, TEN DMs, CCC)
- FIRST SHIPMENT
  - TWO BETA SITE SHIPMENTS, FOURTH QUARTER 1985
  - SIXTEEN PRODUCTION UNITS, 1986

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FLEXIBLE MANUFACTURING SYSTEMS

- MOBILE TRANSPORT UNIT
  - INERTIAL GUIDANCE SYSTEM
  - IR POSITIONING AT DOCKING MODULE
  - SONAR OBSTACLE DETECTION
  - FLEXIBLE ROUTING
  - IR LINK TO CONTROL COMPUTER
  - INTELLEDEX ROBOT
- CENTRAL CONTROL COMPUTER
  - UP TO 5 MTUs AND 50 TOOLS/WIP STATIONS
  - COMPUTER-BASED ROUTE MAPS
  - MTU EASILY REROUTED TO BACKUP TOOL
  - NO HOST COMPUTER REQUIRED

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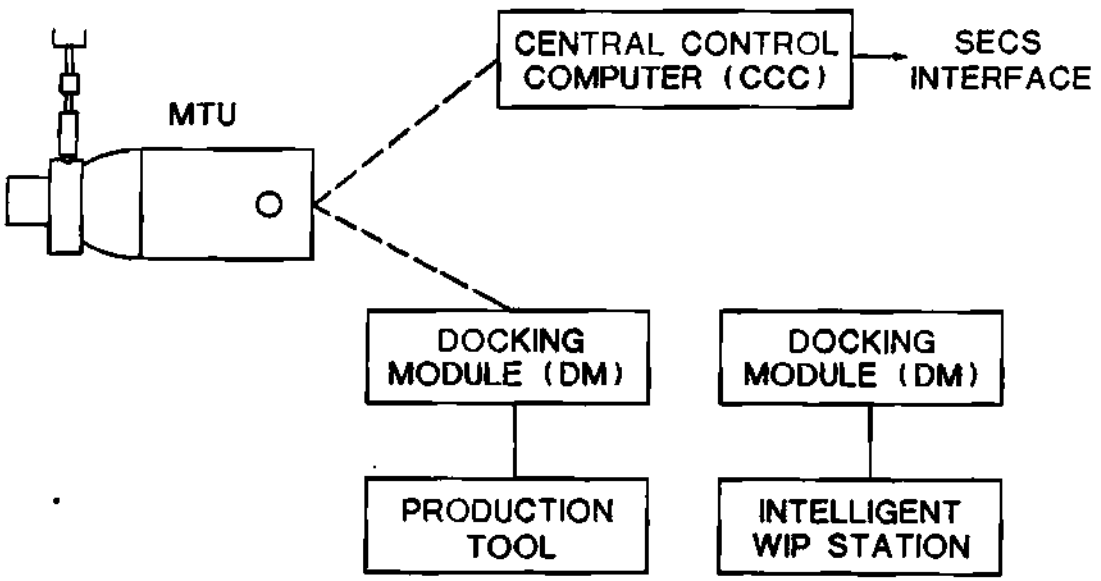
BASIC CIM SYSTEM



VEECO

- SYSTEM COMPONENTS
  - AUTOMATICALLY GUIDED VEHICLES (V1, V2, V3)
  - INTELLIGENT LOCAL AND ZONE WIP STATIONS
  - DEC MICROVAX CONTROL COMPUTER
  - $500,000 (V3, LOCAL WIP, MICROVAX)
- MODULAR APPROACH TO AUTOMATION
  - MANUAL MATERIAL MOVEMENT BETWEEN WIPs
  - AGVs TO MOVE MATERIAL BETWEEN WIPs
  - AGVs TO LOAD/UNLOAD PRODUCTION TOOLS

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VEECO

- AUTOMATICALLY GUIDED VEHICLES
  - PURCHASED FROM LITTON AND ADAPTED
  - OPTICAL SENSORS FOLLOW GUIDE PATH ON FLOOR
  - RF OBSTACLE DETECTION
  - IR LINK TO MICROVAX
  - CAN LOAD SMIF BOXES (V2)

VEECO

- VEEBOT 1
  - CART WITH BINS
  - NO ROBOTICS
  - MATERIAL TRANSFER BETWEEN ZONE WIP STATIONS
- VEEBOT 2
  - FOUR-AXIS TRANSFER MECHANISM
  - MATERIAL TRANSFER BETWEEN LOCAL AND ZONE WIP STATIONS
- VEEBOT 3
  - UNIMATION ROBOTIC ARM
  - LOADS CASSETTES ONTO PRODUCTION TOOLS
  - MATERIAL TRANSFER BETWEEN WIP STATIONS
  - REPORTS LOT DATA
  - TELLS PRODUCTION TOOL TO START ITS PROCESS

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VEECO

- FAIRCHILD
  - MATERIAL TRANSFER BETWEEN PROCESS BAYS
  - MICROVAX, V2, ZONE WIP, FOUR LOCAL WIPs
- MOSTEK
  - MATERIAL TRANSFER
  - MICROVAX, V2, FOUR LOCAL WIPs
  - WILL ADD V3 IN LATE 1985
- SIEMENS
  - MICROVAX, V2/V3, FOUR LOCAL WIPs
- OTHER SYSTEMS ON ORDER FOR DELIVERY IN 1986

WHERE ARE WE?
UNITED STATES

- MANY FABS IN DEGREES OF SOFT AUTOMATION
- NO FULLY INTEGRATED FRONT ENDS
  - THREE TO FIVE YEARS AWAY
- ONLY ISOLATED INSTANCES OF WORK CELL AUTOMATION
  - WET BENCHES
  - DIFFUSION AREA
  - PHOTOBAY
  - ION IMPLANTATION

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U.S. COMPANIES WITH SIGNIFICANT AUTOMATION PROGRAMS

- RCA/SHARP
- NORTHERN TELECOM
- TI
- MOSTEK
- FAIRCHILD
- INT. RECTIFIER
- NATIONAL
- AMD
- INTEL
- IBM (?)
- AT&T (?)

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WHERE ARE WE?
JAPAN

- FULLY AUTOMATED FRONT ENDS
  - MITSUBISHI
  - NEC
  - TOSHIBA
  - FUJITSU
  - HITACHI
  - NMB
  - SHARP
  - MATSUSHITA (?)

UNITED STATES

- CIM SOFTWARE MATURE
- HARD AUTOMATION EMBRYONIC
- FABS HAVE MULTIPLE PRODUCTS/ PROCESSES
- FLEXIBLE APPROACH
- DOWNSIDE RISK
  - LOSS OF HIGH-VOLUME MARKETS TO JAPANESE

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JAPAN

- NO INDEPENDENT SOFTWARE HOUSES
- MITSUBISHI, NEC, TOSHIBA WRITE SOFTWARE
- MATSUSHITA, SONY, TOKYO SANYO BUY SOFTWARE
- JAPANESE CIM SOFTWARE LESS MATURE THAN U.S.
- FABS HAVE SINGLE PRODUCT/PROCESS
- DOWNSIDE RISK
  - FACTORIES ARE DEDICATED

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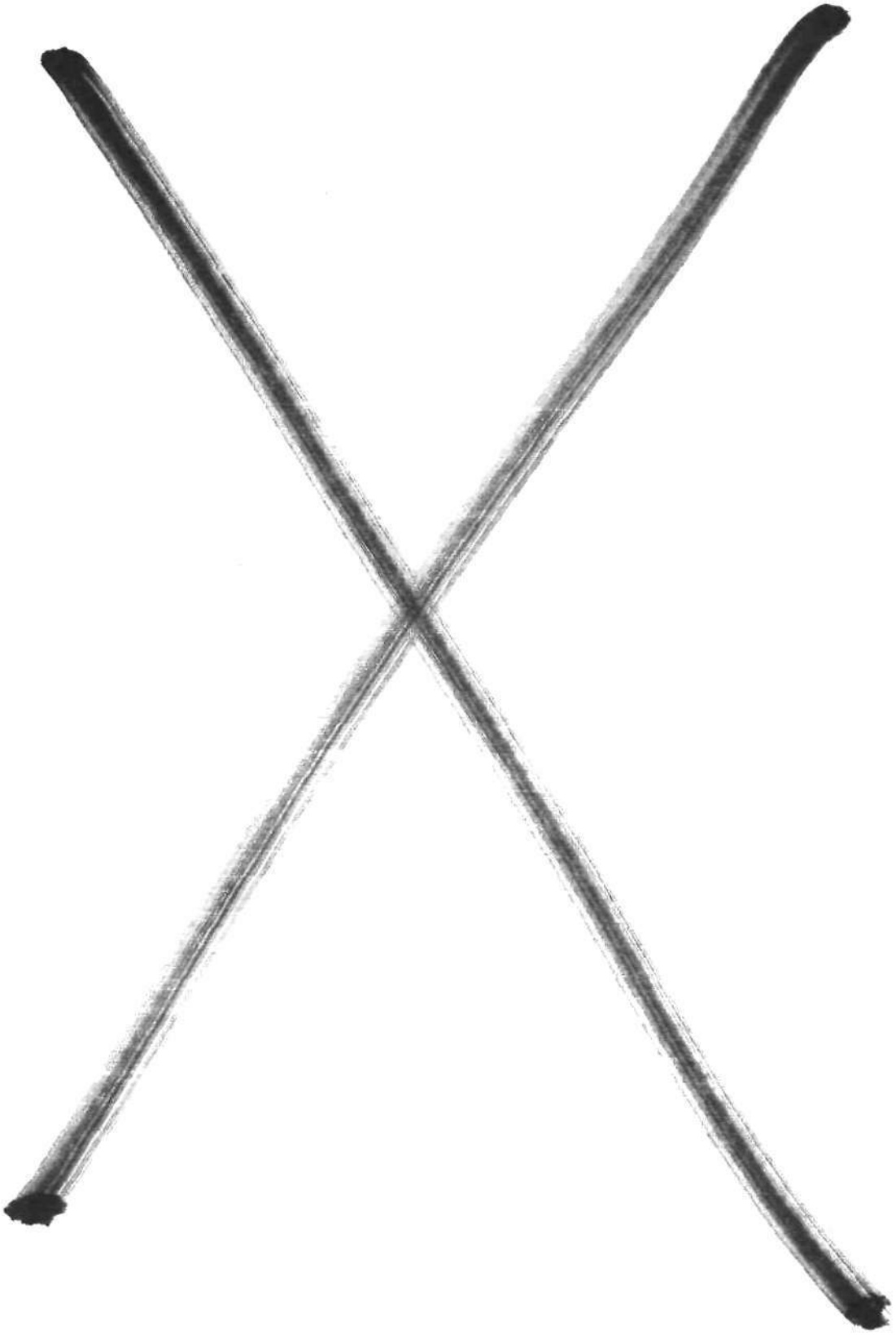

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TRADE ISSUES WITH SEMICONDUCTORS

Clyde V. Prestowitz, Jr.
Counselor to the Secretary of Commerce for Japan
International Trade Administration
U.S. Department of Commerce

Mr. Prestowitz has been Counselor to the Secretary of Commerce for Japan since 1983. Prior to that, he served as Acting Assistant Secretary for International Economic Policy. Previously, Mr. Prestowitz was affiliated with Prestowitz Associates, a consulting and import/export group based in New Canaan, Connecticut, with offices in Tokyo and Brussels. Earlier, he was associated with the American Can Company in Greenwich, Connecticut, Egon Zehnder International Consulting in Japan, and the Scott Paper Company in Philadelphia. Mr. Prestowitz received a B.A. degree from Swarthmore College, M.A. degrees from the East-West Center of the University of Hawaii and Keio University (Tokyo), and an M.B.A. degree from Wharton School of Finance.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
October 14, 15, and 16, 1985
Tucson, Arizona

REMARKS BY CLYDE V. PRESTOWITZ
COUNSELOR TO THE SECRETARY OF COMMERCE
FOR JAPAN AFFAIRS

DATAQUEST CONFERENCE

OCTOBER 14 - 16, 1985

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It is a very great pleasure for me to be here to discuss the status of U.S.-Japan trade in semiconductors.

As we pursue this topic, there are some important points about the competitive posture of our industry, which I would like to emphasize.

-The U.S. semiconductor industry has thrived on intense competition --competition among domestic companies as well as with Japanese and European firms. This competiton has stimulated a continuous search for new devices, reduced production costs, and produced an ever expanding market.

-Our industry has made a substantial investment in R&D to maintain technological leadership. In 1984, these R&D expenditures exceeded $1.8 billion, more than 10 percent of total industry revenues. And in most market segments, this commitment translates into U.S. leadership. In microprocessors, programmable memories, and bipolar logic, American companies set the pace.

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-This industry has achieved startling reductions in unit production costs. Large automated facilities and high-volume manufacturing have combined with technological developments to generate a 20 percent per year decline in the price per semiconductor function. In some parts of the market, this measure of progress--over the long term--runs as high as 40 percent per year.

-Our companies are efficient on a global scale. They have opened product design and development centers in Europe and Japan which tap foreign engineering talent. To lower production costs, they have gone offshore for less skill-intensive production processes. Finally, to improve market access in Japan and in Europe, U.S. chipmakers have established in these countries not only assembly operations, but also the more sophisticated wafer processing facilities.

Deteriorating Domestic and Foreign Market Position

Despite these steps, the U.S. semiconductor industry in 1985 finds itself beleaguered by foreign competition. U.S. semiconductor production will decline this year, falling to $15.0 billion from the $18.0 billion shipped last year. Employment will also be off. A Wall Street Journal article of July 24, 1985 reported the loss of 3,600 jobs in Silicon Valley alone since the beginning of the year.

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This decrease in production and employment is due in large part to the softening of the computer market, the semiconductor industry's largest single end-user, and rising imports. A long-standing multilateral trade surplus turned to a deficit in 1982. By year-end 1984, the figures showed an overall shortfall of over $2.3 billion. The primary reason behind that imbalance was a continuing surge of semiconductor imports from Japan. In 1984, imports from Japan reached $2 billion, more than twice the level of the previous year.

In the first half of 1985, our deficit with Japan continued to climb despite the severe industry recession. Imports from Japan fell by 4 percent during the period, but given the 15 percent drop in total U.S. consumption, this still represented a net gain in market share. Meanwhile, U.S. exports to Japan fell by 28 percent over the same six months, reflecting the continuing market access problems of American manufacturers.

The dramatic overall shift in the trade balance is due almost entirely to slow growth in U.S. exports of completed devices and a long-term increase in imports of foreign-owned devices. Imports of this type have grown at almost 50 percent per year since 1978, while exports have expanded at a rate of only 17 percent per year. Most of this influx is traceable directly to Japan.

From 1980 to 1984, the Japanese share of the world semiconductor market increased by about 25 percent to 27.5 percent, largely at the expense of the market share of U.S. firms. During that same period, the penetration ratio of Japanese imports in the U.S. market tripled, and our bilateral trade deficit with Japan in semiconductors increased nearly eight times to over $1.5 billion. At the same time, the import penetration ratio of our firms in the Japanese market actually declined, and our total share of the Japanese market continues to stagnate at near 10 percent. Despite the removal of formal barriers, despite ostensibly liberal access, and then despite supposed programs to foster imports of U.S. chips, the American share of Japan's semiconductor market stayed remarkably constant, and at depressed levels (never above 13% during the last decade) that bore no relationship to U.S. competitive capabilities.

These developments have taken place against the backdrop of a long-term joint effort by the Japanese Government and industry, to develop a world class position in semiconductor devices. Key elements of the program included:

-Home market protection, including high tariffs, quotas, and restrictions on U.S. investment;

-Substantial financial support for cooperative R&D. Altogether, the Japanese Government funded over 60 different projects. The VLSI project alone, which produced over 1000 patents, was budgeted for $132.3 million between 1976-79.

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-Government efforts to develop a highly integrated, concentrated, interdependent industry structure.

Overt protection of the Japanese market was eliminated by 1976, but the "Third Extraordinary Measures Law for Promotion of Specific Electronic and Machinery Industries," the so-called KIJOHO, continued in effect until the end of June of this year. It provided the legal basis for MITI to continue to foster cooperation among the big six Japanese semiconductor firms on joint R&D projects. It also directed industry effort into specific technologies and directed MITI to see to it that funding would be available for approved research and investment.

Whether or not these efforts were the cause, Japan's success in the semiconductor industry is suggested by the following statistics:

- In 1968, the industry was almost completely dominated by production for consumer electronic products. Sophisticated integrated circuit (IC) production had reached only $24 million out of a total yearly semiconductor production of $252 million, and a total component production of $1.4 billion.

- By 1978, sophisticated, international, state-of-the-art IC production for computer and telecommunications equipment had reached $1.2 billion out of $2.4 billion total semiconductor production and total component production of $8.75 billion.

-Integrated circuits now dominate the Japanese microelectronic world. Random-access memories have clearly become a specialty--Japan holds a 90 percent share of the world 256K DRAM market and will be the first to introduce a 1-Megabit device into the commercial marketplace. But Japanese companies are now also using this commercial base to diversify into a broad variety of chips. Their domestic end-use pattern, while still consumer-intensive, now affords greater opportunities for devices oriented towards telecommunications and computer applications.

Sources of Trade Friction

The sharp differences in the approach of these two industries--a very open U.S. market and a historically protected Japanese market--have led, almost inevitably, to trade conflict.

Early in the life cycle of the 64K RAM, rapid Japanese penetration of this market led to formation of the High Tech Work Group in 1981. The Working Group eventually adopted a series of joint recommendations on semiconductor trade between the two countries which were endorsed by the Japanese and the U.S. cabinets in late 1983. The two governments agreed:

- To mutually eliminate their tariffs on semiconductors;
- To provide protection against the copying of chips; and,

- To establish a Joint Data Collection System to monitor trends in the industry in order to prevent unnecessary friction and misunderstanding.

Each of these goals has been achieved.

At the same time, the Japanese Government undertook to promote imports of U.S.-based semiconductor products, and MITI in fact called in the leading Japanese semiconductor consumers to encourage them to develop long-term supplier relationships with U.S. firms. In this area, we were less successful.

For a brief time, U.S. sales did increase. But this coincided with a period of very strong demand--and tight supplies--in the global market. U.S. suppliers responded to Japanese orders by according Japanese customers priority--even at the expense of long-term domestic buyers.

With the downturn in the world semiconductor market, U.S. sales to Japan have declined--both in absolute value and in terms of market share. In retrospect, it appears that purchases in early 1984 were opportunistic and did not lead to any long-term relationships.

It is clear that any future attempt to open the Japanese semiconductor market must finally solve the question of how we can creat a long-term role for U.S. companies which is consistent with our global competitive position, in this pattern of established

supplier relationships. These are often a matter of private business practices, as much as government policy, but they exist with the approval--or at least the acquiescence--of the Japanese government.

Current Trade Investigations

I will not comment on the merits of the Section 301 Petition filed by the Semiconductor Industry Association. I can report that USTR has advised the Government of Japan that we will pursue the case, and we have recently transmitted to the Japanese Government a list of questions regarding government policies and industry practices which we feel bear on some of the allegations in the petition.

Nor can I comment on the progress of the two dumping petitions--one relating to 64K DRAM and one to EPROMs--which are currently being investigated by the Department of Commerce, or the Department of Justice's investigation of possible possible predatory semiconductor pricing by Japanese subsidiaries in the U.S.

At issue in these petitions and investigations is whether Japan and its semiconductor firms are playing fairly, by the rules of the world trading system, in this industry. This question is basic to the President's trade policy as spelled out in his September 23 announcement. How it works in practice is clear if we look at our comprehensive approach to this industry.

-We are vigorously enforcing existing trade laws. We are moving forward with the 301 investigation, and I interpret the filing of the latest EPROM case as a vote of confidence in this Administration's determination of provide fullest protection of the laws where illegal pricing practices are involved.

-The international protection of intellectual property rights--a key feature of the President's program--is critical to this industry. We have already convinced the Japanese of the need to provide special protection for chip designs, and we will be pursuing this issue with other important East Asian producers, especially the Koreans and Taiwanese.

-To move agressively agasint unfair trade practices the President has established a Strike Force chaired by Secretary Baldrige. The Secretary has asked me to direct the day-to-day work of this group, and I can assure you that problems such as those facing our semiconductor industry will be at the top of our agenda.

Our semiconductor industry is a highly competitive, internationally efficient, high technology industry which is facing stiff--and arguably unfair--foreign competition. The President's trade policy announcement sends a clear message that we will act--and act effectively--in such cases.

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SRC AND ITS ROLE IN THE TRANSITION

Larry Sumney
President
Semiconductor Research Corporation

Mr. Sumney is President of the Semiconductor Research Corporation (SRC), a subsidiary of the Semiconductor Industry Association. Previously, he was Executive Director of SRC. Prior to that, Mr. Sumney was employed by the office of the Under Secretary of Defense for Research and Engineering and was the Director of the VHSIC Program Office. He has also served on numerous technical and management panels. Mr. Sumney received a B.A. degree with honors in Physics from Washington and Jefferson College, an M.A. degree from George Washington University, and has completed course work toward a DSc degree in Systems Engineering.

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SRC AND ITS ROLE IN THE TRANSITION

Larry W. Sumney
President
Semiconductor Research Corporation

OUTLINE

INTRODUCTION

- Transition to stability?
- Anticipation of key developments
- Roles
- U.S. assets and handicaps

TRADITIONAL SOURCES OF TECHNOLOGY

- Technology sources during the growth period
- Decreasing role of the merchants
- The government contribution
- New competition

NEED FOR NEW STRUCTURES

- Old structures and old ways
- Global markets and competition
- Technology maturity
- Forecasting and follow-through

A STEP TOWARD COOPERATION - THE SRC

- Motivations of the founders
- Building a constituency
- Academic research and its limitations

AFTER THE BASICS

- Building on the research base
- Shared knowledge in a competitive environment
- Building a knowledge base
- Providing directions
- Complimentary roles in a mature industry

BEYOND MATURITY

SRC AND ITS ROLE IN THE TRANSITION

Larry W. Sumney
President
Semiconductor Research Corporation

INTRODUCTION

In the words of Dataquest, the semiconductor industry is transitioning from its adolescence to its maturity. I do not wish to dwell on semantics but in my dictionary maturity is defined as fully developed. If this industry is fully developed, or anywhere close to it, I have a serious problem in my perspective. Usually, as an equilibrium state is approached the magnitude of the cyclic swings are reduced and their frequency reduced. The particular cycle which the industry is now riding is as large as any of the past 20 years and the four-year cycle is still with us. A new economic system which resonates with increasing magnitudes rather than being characterized by a damping force may have been created. If so, these cycles will continue with constantly increasing amplitude unless we can detune or dampen the system in some way. In the circuit analogy, a resonant system can be damped by increasing its losses. That we don't want to do.

It is very true however that a transition is occurring. This transition is associated with the nature and size of the industry and the stakes on the table when decisions on new products or technologies are made. The world of production of semiconductor devices now exceeds $20 billion in value and the lineup of the major players is constantly being juggled. When the cost of a fab line reaches $100 million and that of a new product design may be one-third as much, then we don't want to make many mistakes. In a recent book, "Foresight in Science: Picking the Winners" by John Irvine and Ben Martin (Ref), the point is made that because the scale and cost of R&D are increasing and the economic payoffs of R&D appear to depend more and more on the choices made early in the process, governments and industry must increase their abilities to anticipate key developments in science and technology in order to guide their allocation of resources. In this country, recent events have tended to question our ability to anticipate future developments. The book identifies five requirements for successful forecasting: (1) extensive information on worldwide research trends; (2) a combining of scientific and industrial perspectives; (3) attaching prime importance to the views of the working scientists and engineers as opposed to senior executives; (4) specific forecasts being performed by industry with government forecasting of trends; and (5) the involvement of a wide range of individuals and institutions in the forecasting. The last requirement, according to Irvine and Martin, is most important.

Reference - "Foresight in Science: Picking the Winners", by John Irvine and Ben R. Martin. Dover, N.H.: Frances Pinter, 1984, 168 pp.

In meeting these requirements for planning for the U.S. industry in our transitioning high stakes industry, there are roles for many organizations. Dataquest is a respected information source for the industry. Every company in the business, their suppliers and customers, our universities, and the U.S. government have important roles both in the decision making processes and in the follow-through actions that are the real payoffs. In addition, the SRC has an important role that will be examined in detail in this presentation.

The challenge for the U.S. industry is to learn how to compete in a global economy, which we are not now doing as effectively as we should. Our assets are considerable. The U.S. is noted for being a society that is creative -- new ideas and innovations are almost too abundant. Some of our largest corporations actively market their surplus of innovations. In the semiconductor area, the U.S. industry has established through its universities and industry, an integrated circuit design capability that is clearly in the lead. There is no question that the quality of U.S. universities is excellent or that, until now, in almost all areas of integrated circuit R&D, the U.S. either leads or is running neck-to-neck with its competitors. Another advantage is that we have led both in the size of the domestic market for IC's and in the U.S. share of the world market that we have served.

Countering these significant assets has been a seemingly growing list of handicaps to our ability to remain competitive. Basic among these have been such factors as the cost of capital, the cost of labor, the erosion of market share, and the loss of manufacturing skills. Additional handicaps include the lack of effective planning and the difficulty in targeting identified goals. In a more technical category is the traditional difficulty experienced in transitioning technology into products and a basic inefficiency in the R&D process. One may argue with this latter point but it is my observation that due to the nature and structure of our industry, a large percentage of our R&D effort is redundant. Often, a given technical advance will be independently developed by multiple organizations at an unconscionable cost to the efficiency of our R&D system.

In order to consider the role of the SRC in greater detail, some background, beginning with the traditional sources of semiconductor technology must be reviewed.

TRADITIONAL SOURCES OF SEMICONDUCTOR TECHNOLOGY

The U.S. is the source of semiconductor technology. For the decades of the forties and fifties that included the invention of the transistor, the Bell Telephone Laboratories provided the bulk of generic technology

for the industry and to their great credit, made a conscious decision to make this knowledge available to all. No semiconductor researcher in the fifties or early sixties operated without Shockley's book, the two-volume transistor technology books, or a filing drawer filled with the famous Bell Laboratories monographs. By the mid-sixties, the role of Bell diminished with the rapid growth of the industry and in the more recent period, this resource has been effectively destroyed by the breakup of AT&T. From the mid-sixties through the seventies, the merchant semiconductor firms and their entrepreneural offspring filled the role of generating the technology seed-corn of the industry albeit unwillingly. Personnel mobility caused technology advances to propagate rapidly throughout the industry so that vigorous device technology growth occurred. The lack of competition to the U.S. industry provided the markets that generated ample funds for R&D and for plant investments. Through the seventies, the growth of the large merchant semiconductor houses lead the chase with an active pack of entrepreneural foxes continually nipping at their heels. Even as one of the foxes was cornered and slain, others joined the pack because of the substantial rewards for the few survivors. A few have survived the chase but the fray is still active with continuing threats even to the leaders.

The universities have contributed a continued flow of basic research in support of the IC industry but this has been limited by lack of funds and often directed to peripheral areas. Entrepreneurs have also been active players in the technology but most often are engaged in transferring technology from a larger company rather than creating it.

In the decade of the seventies, large integrated companies spawned captive semiconductor operations that were to play an increasingly important role in the industry. As the competition heightened, the merchant semiconductor research perspective became increasingly short-term and the trend-setting, long-range research was relegated to a few of the largest semiconductor device firms and to the vertically integrated captive producers.

During these decades, the sixties and seventies, when the industry was growing rapidly, the government and the associated aerospace firms played an important but peripheral role. Since most of the government funding was associated with space and defense, the tendency was to fund R&D that served primarily unique requirements for performance in these environments. In addition, the government provided a continuing but modest effort in fundamental research. The government participation increased dramatically in the early eighties with the VHSIC program. This provided a major shot in the arm for silicon VLSI technology at a time when it was badly needed by the industry. During the mid-eighties, VHSIC has provided a major thrust in silicon technology closely aligned to commercial objectives.

The problem for the U.S. industry has been that the merchant semiconductor companies that were leading the technical surges to new products have become increasingly restricted as competition has limited their ability to generate funds for R&D. Product design became almost the sole focus of development efforts and advanced device and process development suffered. Manufacturing advances became more dependent on equipment vendors and significant technology areas, such as high performance packages for devices and some processing materials, became dominated by offshore suppliers.

As an industry matures, particularly one that is so important to all of the world, it is not surprising that other countries become aware of this importance and establish competitive positions. What is surprising is that in about one decade, the U.S. with all of its advantages in the semiconductor field has seen these advantages erode as competitors have reaped the benefits of U.S. created technology so effectively and rapidly. This has led to the conclusion that something has to change in the U.S. if we are to continue leadership in IC's with all of the implications of this leadership as the world moves toward an information based economy.

THE NEED FOR NEW STRUCTURES

We see that in the arena of IC technology, the U.S. is creative but has difficulty in transferring the products of this creativity into products and in producing these products. The reasons for this are at least partially rooted in the nature of the companies and industries. First, stemming from the personal competition that is drilled into the U.S. engineer, there is a large measure of the so-called NIH (not-invented-here) attitude wherein the ideas of others, even within the same organization, are discarded in favor of the development of new approaches that may only be marginally better. Second, there is the carry-over from the early days of the semiconductor business when companies failed or succeeded due to their better knowledge about a process or a device. Thus, a large body of know-how has been considered as proprietary by U.S. companies in contrast to competitors who in their efforts to access the vast know-how already existing, were more willing to share what little they did know. Third, is the fundamental structure of the U.S. economy based on vigorous internal competition among similar producers with an accepted but outdated set of rules. Anti-trust laws, taxation, and other carryovers from this insular economy are sometimes too restrictive for global competition with a different set of rules.

The world semiconductor industry is one in which multinational corporations and markets are inherently intertwined with national goals and economies. In many respects, the large U.S. market is more open to foreign competition then other markets and the industries of many countries are more monolithic in their approach to world markets than that of the U.S.

Another factor affecting the industry is the maturity of semiconductor technology. As the complexity of manufacturing tools has increased, the fabrication processes have become more and more dependent on the tools which are available to all users. Also, even as processes have progressed to increased use of new technologies such as ion implantation and dry etching, the changes in the fabrication line are fewer and less frequent. Even if a technique begins as a proprietary process, if it provides an advantage, it soon becomes generic to the industry. Competition then occurs in device design, manufacturing skills, application, and marketing.

A third factor is that, since accurate anticipation of key developments is necessary for success in all of the areas, establishment of a system that provides this capability is an essential to being competitive. While major firms have internal forecasting operations with varying capabilities and analyses are available on a fee basis from a multitude of independent organizations, there is no systematic and complete process for the semiconductor industry that supports forecasting. In fact, the desirability for some collective actions in this regard is under discussion and the limits of such collaboration are not defined. Inherent in any such process is the involvement of enough of the participants in the industry so that credible forecasts are obtained, desirable responses are identified, and appropriate follow-through actions will occur.

A STEP TOWARD COOPERATION - THE SRC

The Semiconductor Research Corporation (SRC) was formed because of the declining competitive posture of the U.S. semiconductor industry. It was envisioned as a cooperative mechanism for undertaking generic research through fees assessed on the members. The research is focused on the defined goals of the industry and has, as an important feature, an increase in the number of relevantly trained scientists and engineers. To this time, almost the sole focus of the SRC has been on the research program that now includes over forty projects and close to 400 graduate students performing research on semiconductor materials, devices, and processes; and on design and manufacturing technologies.

In the three years that the SRC has been operative, a significant activity and constituency has been established. Some 200 faculty members

from the contracting universities are providing an increasing flow of information that is being effectively communicated to the member companies. Products include the demonstration of 1/4 micron transistor performance, a new metallization system for submicron device interconnections, new software packages for design, and a massive flow of research data on every conceivable facet of the technology. Among the 40 or so companies that are members of the SRC, hundreds of engineers are participating in interactions with the research program through meetings, as mentors for the research efforts, or as advisors to the SRC in structuring and managing the program.

It is clear that these academic research activities are productive in terms of graduates who will provide the manpower and in terms of research that will provide many of the seminal ideas for the future of the industry. There are, in addition, a variety of short-term products resulting from the research that contribute to the industry's present efforts, especially in the design area. However, it is apparent that additional contributions can and must be made to the industry in support of its short-range competitiveness, neither the time scale nor the nature of university research equip it to respond to such needs.

AFTER THE BASICS

An expanded role for the SRC in response to these considerations is currently being discussed. The existing academic research program will remain its prime function even when other activities compliment this research and extend the service being performed for the member companies.

At present, companies in the U.S. industry share a large amount of information through publications, technical meetings, or diffusion through professional contacts or personnel mobility. Results from SRC research initially are available to member companies but in time become available to everyone. A key question relates to whether other categories of information can be shared. For example, it has been suggested that information relating to manufacturing equipment specifications, if shared, would permit better targeting for equipment vendors. Questions relating to the types of information that can be shared and the pros and cons of sharing information is a subject that needs to be addressed. In some respects we are building a case for more sharing of technical information in those areas that have little impact on market competition with the expectation that the benefits for a given participant in the information pool would greatly exceed the value of what he contributes. In this function the SRC may act as a catalyst for sharing of information and provide the repository and distribution system.

Enabling more efficient use of existing information, i.e., knowledge enhancement is another possible role for the SRC. This would involve the collection, analysis, and dissemination of existing information. It is based again upon the fact that much duplicated effort is involved in these functions in individual companies and, because of the effort required, essential information is not available when and where needed. The magnitude and complexity of this problem will challenge the architects, particularly the organization and retrieval strategy for the large information base. SRC currently operates an information bank accessible to members which can be expanded to accommodate this function. Both technical and operational information would be considered in this function. One would expect that the data bank, for a given technical subject, would answer questions as to who is doing research? who the equipment suppliers are? what are some of the most recent results? what are the present goals of the research? and what are the present capabilities of the technology? In addition, it might include references to the most significant publications and to current publications of the last year. It could also include some fundamental technical information.

A third role being considered for the SRC is the provision of forums in which members would participate in technology assessments or in the discussion of issues facing the industry. One such activity is already underway in which mutual interests in manufacturing tools is being discussed with the objective of identifying recommendations to the members on actions which will benefit them and the U.S. industry. We expect to see recommendations ensue from this activity in the near future. A technology assessment meeting has also been organized by the SRC in which the status of three current technical areas were examined. The SRC provides a mechanism for extension of this activity to many areas of collective industry interest. In most cases, these forums result in recommendations to the member companies or in information that the member companies can apply in pursuit of their individual objectives. The extent to which the recommendations are followed or the information used will be entirely up to the recipients.

These new roles being considered for the SRC are complimentary to those of the existing organizations serving the U.S. semiconductor industry. The SIA is an effective organization serving the industry by providing market statistics; by serving as a unified voice to the government on regulatory, trade, and taxation issues affecting the industry; and by providing a forum for the discussion of related issues. The SEMI sets equipment and material standards, provides a forum for the discussion of equipment and materials related issues, and sponsors trade shows for the industry. MCC provides a cooperative development effort in the area of computer systems. The government supports fundamental research of interest to the industry; carries out developments related to specific needs of the military and space programs; and provides statistical,

trade, and other supporting services. The industry carries out product development and dependent on the size of the firm may have activities in all of the functions that have been discussed. Finally, a number of technical societies serve the industry by providing technical journals and meetings in which research results are described and critiqued, by undertaking standard setting, and by supporting the continuing education of their members.

BEYOND MATURITY

In this discussion, the needs of the U.S. semiconductor industry in meeting the requirements of global competitiveness have been discussed. The present and possible expanded role of the SRC in helping its member companies to compete better have been described. As the industry develops toward the $100 billion markets of the future, there is little doubt that substantial, additional changes will be occurring in the industry. The SRC expects to also mature in its activities and to be a major contributor to the industry and to the maintenance of a strong position for its members in this industry. Our inexorable position is that the continued success of this industry is key to the success of the U.S. as we move into the information age.

Nielsen Dataquest

CHALLENGES IN AUTOMOTIVE ELECTRONICS

Jerome G. Rivard
Chief Engineer, Electrical and Electronics Division
Ford Motor Company

Mr. Rivard is Chief Engineer for the Electrical and Electronics Division of the Ford Motor Company. Prior to joining Ford, he spent 14 years with the Bendix Corporation, where he was Group Director of Engineering. He has also been associated with Vickers Incorporated, the U.S. Army Ballistic Missile Agency, and the General Motors Technical Center. Mr. Rivard received a B.S.M.E. degree with honors from the University of Wisconsin.

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CHALLENGES IN AUTOMOTIVE ELECTRONICS

Jerome G. Rivard
Chief Engineer
Ford Motor Company

INTRODUCTION

Good Morning. Once again I'm happy to be addressing my colleagues in the electronics community. The past couple of days have been most rewarding in terms of the information that's already been exchanged.

One hundred years ago, in 1885, Karl Benz, a German engineer, built the first workable automobile, a one cylinder, three-wheeled vehicle. We can imagine the challenges faced by Mr. Benz and other auto pioneers. There were basic vehicle needs to start, steer, run, and stop reliably.

Today, we're faced with quite a different set of challenges that I'm hopeful will be met in the near future.

Accordingly, I think the title selected--"Challenges in Automotive Electronics"--is most appropriate for this conference. There's no question that the auto industry's long term viability hinges on our mutual efforts to be innovative, cooperative, and driven by a dedicated commitment to achieve uncompromising levels of quality. I can't emphasize enough that achieving world class quality is our major challenge in the automotive electronics arena. The automotive industry realizes that the vehicle's electronic, electrical and mechanical systems must be in harmony. One system must not fail the other two. It's a little bit like Frank Sinatra's lyrics in the old song about "Love and Marriage"--you know the one where he sings that..."you can't have one without the other." That's domestic harmony that keeps people together. Vehicle harmony keeps people loyal to their car company and it attracts new owners. We know that today's auto buyer has a wide choice in automobiles. We also know that today's consumer will take his business across the street (or across the world) if his vehicle fails to deliver top-notch, world-class performance.

FORD'S LONG TERM QUALITY TARGETS

At Ford, we've established long term quality targets and through the major contributions of the semiconductor industry, we've made good progress over the past few years but much work remains to be done, and we need additional help to achieve our goals.

We can say with certainty that progress in the area of vehicle quality will require new approaches to both engineering and manufacturing motor vehicles. It will also require fresh, new approaches to the manufacturer--supplier relationship. The results of all these activities must make us cost competitive on a global basis while enhancing our quality levels.

Today, I'll discuss the current state of automotive electronics from a quality point of view...look at areas of specific concern that require our attention now...and review some electronic technologies where further development will usher in a host of automotive applications.

I think it's helpful to see where the automobile has progressed in terms of electronic applications.

This slide puts into perspective the significant presence of electronics in the automobile. The influence is rather remarkable when you think back only ten years when less than 20 per cent of these electronic systems were available.

NEED FOR CONSISTENT SUPPLIER QUALITY

Let me say, here, that I think our semiconductor suppliers, overall, can do an excellent job of building quality parts. It's simply a matter of consistency. We need to see quality parts produced each day of the week. I hope some of the suggestions I'll make in the next few minutes will assist our suppliers in meeting quality levels that are consistent, day-in and day-out.

At Ford's Electrical and Electronics Division, we've set some quality goals for ourselves. By 1988, we have a goal to have integrated circuit quality levels of below 50 parts per million and electronic module quality below 400 parts per million.

These quality levels are certainly attainable but, frankly, we need to first resolve some important issues with you, our semiconductor suppliers.

The first area where we need to harmonize our efforts is in the way that quality is measured.

What's happening is this. Our incoming quality level at Ford and I'm sure elsewhere--differs dramatically from what our suppliers are telling us about their outgoing quality levels.

You'll note from the slide that there's quite a difference and what this tells me is that there's a measurement problem that needs to be made right. We're using different methods to measure quality. We're out of step on this issue quite significantly.

It appears that major differences exist in outgoing and incoming test programs...inadequate component specifications related to part application...or several other factors could come into play here. To improve this situation, there are several actions I would like to see our suppliers take.

As a semiconductor supplier, and to help us understand the reasons for early field failures, you should be gathering "burn-in-data" on your components--and have a good idea how this data helps you as a quality screen. I also hope that you would share this data with us. We would like to know, for example, what your "infant mortality" rate is--and how long and at what temperature should we be burning parts in?

During the burn-in process, is it possible that some parts are being damaged by electrostatic discharge? Is burn-in the best screen for all parts? It's essential that we learn the answers to these kinds of questions. Customer satisfaction and loyalty are at stake!

I strongly urge suppliers--who provide Ford Motor Company with complex microcomputers--to utilize computer aids to help develop designs capable of fault elimination that approaches 100 per cent.

We'd like you--our suppliers--to visit our manufacturing plants to see, first hand, how your parts are processed. And, during your visits, pick up some failed parts and take them back to your company for a thorough failure analysis.

Once you've analyzed failed parts, tell us what's been discovered. More importantly, make the design, process, and test program changes required. If you think that we're doing something to damage parts, don't hesitate to tell us. The old days of doing business are gone, I hope, forever. We're not going to "shoot the messenger" for bringing us bad news.

Also, I would like you to insist on "correlation" and to make your test engineers available to work with us. And, please, don't tie our hands with "non-disclosure" agreements for information which is not really secret. Work with us as partners who trust each other and share information.

Another area we need to address is specifications. We have to stop thinking in terms of tolerances but, rather, design circuits to target values. At Ford, our specifications will soon emphasize target values and we'll expect our suppliers to provide parts with very tight distributions around our target values.

This approach will provide for better design margins in Ford products and this means better quality...reliability...and better yields for you.

Something else to consider is electrostatic discharge which is becoming a larger factor in quality and reliability concerns. You probably know that the major problem involving ESD is in the latent damage which shows up in the field. Let's be certain that our people are aware of this problem and that manufacturing plants and integrated circuits are up to the latest standards of ESD protection.

At Ford, we've tightened our requirements to 2000 volts--the industry standard Human Body Model--and we've adopted the so-called Charged Device Model which is widely used in Japan. This last model simulates the effects of charged machinery such as integrated circuit handlers.

Once again, I would ask you to visit our plants and tell us if you think there's an area where we can improve. I would like our suppliers to understand Ford facilities as they relate to ESD considerations. Of course, it works both ways because I continually encourage people from our Division to visit supplier plants. Getting to know each other's facilities makes good business sense for the manufacturer and supplier team to follow. Only good results can be expected from visiting and understanding each other's facilities.

OUR CHALLENGES...AND OPPORTUNITIES

Now, let's look at some specific areas that present us with an array of challenges...and opportunities.

Ford, along with most of the electronics industry, believes that surface mounted devices offer the best potential for improving electronic packaging density. Another benefit of SMD's is enhanced reliability. Ford has, in fact, committed itself to implementing surface mounted device technology and we've initially targeted radios and engine control modules. By the end of 1985, Ford will have placed a cumulative total of 84 million SMD's with an expected increase to a cumulative 3 billion SMD's in the 1990's.

Let me give you a good news-bad news perspective on the current state of surface mounted devices. Looking at advantages, I've mentioned the important benefit of higher component density. To date, board space savings has amounted to one third to one half--and permitted more circuit functions and complexity. In addition, SMD's provide us with a meaningful size and weight reduction at the module level.

The SMD process is highly automatable.

Surface mounted devices also provide improved shock and vibration characteristics and because of the shorter interconnects, there's lower electromagnetic and radio frequency interference susceptibility.

Now, taking a look at the other side of the coin, here are some areas that need to be improved.

Consider the importance of machine compatibility with package tolerances--and the board layout. Time and time again, we've seen that incompatible equipment and parts just don't mix. I'd also like to remind you that electrostatic discharge can be a problem if conductive tapes are not used.

There's a current lack of component availability and standardization. For example, small outline transistor packages vary in footprint and body sizes. This results in various problems with circuit layout and manufacturing.

Plastic "J" leaded quad packs require improved planarity since problems are occurring during subsequent reflow solder operations. We would like to have less than a 2 mil variation across all leads.

We would like to see IC suppliers improve their component reliability by evaluating their components through various soldering processes. These processes include wave soldering, infra-red, and vapor phase. These soldering techniques represent Ford's current and future assembly requirements and assistance is needed in determining the reliability factors.

Moving on, we need to have SMD tape and reel standards because, from a user perspective, the ability to utilize a reel on any given machine is a significant advantage. We should also have a conductive, plastic embossed tape. Basically, I see a need to determine the best tape material for the industry.

We would also consider it to be a positive step to see the development of SMD packaging with lower thermal resistance.

Tape automated bonding offers the potential for quality improvement, size reduction, and better thermal management. We believe that the semiconductor industry needs to bring this technology into the mainline manufacturing system and we strongly encourage the industry's action in this area.

Looking at testability issues, we feel that significant improvements are required for handling equipment involving small outline transistors, small outline integrated circuits, and quad packaging. Currently, the co-planarity of device leads may be distorted by test equipment handlers and burn-in sockets.

There's a need to develop effective methods of applying "burn-in" and other conditioning screens to SMD packaged IC's. When evaluating devices that are packaged as small outline integrated circuits, test sockets are required for quick insertion and removal. These test sockets are very expensive and the handling process results in a high probability of damaging the parts when they're mounted or removed from the sockets. Now, even though this particular problem may be unique to the test equipment makers, we all retain a vested interest in the development of the right equipment.

I hope that the concerns I just presented will be acted upon by our semiconductor suppliers at a quicker pace. I know you're working on many of these concerns already. The resolution of these issues will help bring us the quality products that are demanded in today's global automotive market--and, as a spin-off benefit, answer the needs of the electronics market in general.

BETTER BUSINESS PRACTICES

Next, I'd like to switch gears for a few minutes and talk about better ways of doing business.

Ford Motor Company is encouraging its suppliers to plan for quality through new, improved business and manufacturing practices.

We're encouraging a no-secrets, up-front, open relationship with each supplier. We're reducing our supplier base to those companies who meet "best in quality" credentials from planning to manufacturing. Ford is looking for long term, partnership-type relationships.

One technique we'd like to see all of our suppliers adopt is statistical process control. In what should be considered to be ancient history, most manufacturers used screens to weed out bad parts. No more! This method is both wasteful and costly. Establishing a statistically-controlled process simply means that the quality level can be controlled, maintained, and improved based on reproducible, consistent results. Screening should be practiced primarily for monitoring and feedback purposes, not to eliminate unacceptable parts. Unfortunately, screens are still required to weed out infant mortality.

A key benefit of SPC is the ability to consistently produce product uniformity. As I mentioned earlier, at Ford we're designing to target values and our specifications will soon reflect this. Moreover, we expect tight distributions around these target values--and these target values are attainable through statistical process control and design of experiments.

Let me remind you that by the 1990's, electronic content per vehicle should be about $1400 worldwide. The U.S. electronics content per vehicle today is projected to be $650.

Currently, the overall automotive electronics market is at $2 billion anually. One conclusion we can draw with certainty is the need for technological breakthroughs and a need for the highest product quality to support this expanded electronic content.

Now that we've looked at some areas of mutual concern, I would like to talk about a number of electronic technologies and their automotive applications.

ELECTRONIC TECHNOLOGIES AND THEIR AUTOMOTIVE APPLICATIONS

Memories

The expanded use and sophistication of microprocessors in automobiles has required large amounts of read-only memory, ROM, and the need to turn around new ROM codes quickly. Let me just say that the strides the industry is making toward cost effective EPROM and E^2PROM is most appreciated. In fact, EPROM's are having a major impact on our engine control program in the 1986 model year.

The ability to reprogram the microcomputer after manufacture--using an on-board EPROM or E^2PROM--is also a highly desirable goal. With respect to alterable memory, reprogramming ability will result in a reduction in part inventory for the semiconductor manufacturer and the user and will provide for last minute changes which always seem to be required. Our ongoing concern here is with reliability and quality levels since the EPROM or E^2PROM on board a micro-computer is not as easily tested as a standard memory.

Power Devices

With the continued growth of automotive electronic systems, the use of power devices will increase substantially. Recently, power devices and control circuitry have been combined on a single IC, resulting in a smart power device. This development opens the door to new applications which could include power supplies, electronic relays, multiplex wiring, and actuator drivers.

For these applications to become "real-world," we need lower costs and further reductions in on-resistance. Smart power devices need to be capable of being utilized in a multiplexed wiring system.

For example, we need the following on-resistance performance at 20 amps. A drop of less than one volt on the high side switch--and a drop of less than one half volt on the H Driver. We also need to see costs come down to $2.00 and $6.00 respectively.

Microprocessors

There's no sense in reviewing the obvious--the tremendous advances we've had in microprocessor technology. There are, however, a few areas where certain developments would represent major progress--and make a great deal of sense.

Because today's vehicle applications require large amounts of power, there's an immediate need to improve the basic input-output capability. This improvement may require a combination of device technologies on the same chip, a challenge the semiconductor industry is presently pursuing.

The combination of more powerful computers and drivers will increase the range of control functions, reliability, and will allow direct microprocessor control of such items as electronic instrumentation and audio systems.

Data sharing, among vehicle systems, is another worthy goal that promises many customer benefits including vehicle reliability and added functional content. A good example would be data sharing between the vehicle's engine module and electronic instrumentation. This would eliminate redundant sensors.

We're looking for cost effective Digital Signal Processing for application to our audio products. The fast pace at which design rules are shrinking will hopefully bring the day closer when the DSP complex functions can be implemented on a die size which is cost competitive--on a system basis--with today's analog approaches.

Sensors

Another key technology with strong automotive ties is sensors--and the need for sensors continues to increase. I'm looking for the development of smart sensors--the integration of electronics into sensing elements. This accomplishment would enable us to perform signal conditioning, self diagnostics, and simple vehicle computations.

We also need new sensor developments to meet such automotive applications as fluid level checks and condition, non-contacting rotary and linear position accelerometers for use in ride and handling control, accurate and durable mass air flow management, and in-cylinder engine parameters.

I'd just like to interject a thought here on sensor suppliers. We've found that those companies who have full service capability provide us with the best sensor products. Full service means a sensor supplier who has outstanding capabilities in technology, design expertise, manufacturing, and application experience.

Along with the potential sensor developments and company capabilities I just mentioned, we'll need advances in distributing power and information throughout the vehicle.

Multiplex Wiring

There's no question that the wiring harness has become complex and bulky. Multiplex wiring offers a solution to the ever-growing nest of wires. Our vision calls for a multiplex wiring system that consists of a "bus" that's made up of power and ground wires and a pair of signal wires that interconnect all of the vehicle's modules, actuators or loads. Each of these products would have an intelligent interface to the bus. To achieve this vision, we need continued development of key technologies by our electronic suppliers. These key technologies include smart power high side drivers and H drivers with ratings of 4, 10, and 20 amps which are needed now--while 40 amp versions carry a lower priority. These devices should have overload protection and provide status feedback.

Microcomputer features we would be happy to see include CMOS with a "sleep mode" for low key off current, on-chip E^2PROM to help us minimize the number of unique modules and microcomputer codes, additional on chip RAM (50-100% increment to current RAM availability), and an on-chip serial port for the logic level portion of the multiplex signal bus interface.

There's a need for a line driver with low voltage drop--and an on-chip line receiver, both, which operate from 10 to 16 volts DC.

Finally, on our multiplex wiring "want list," are insulator piercing connectors that are reliable in an automotive environment. This development would, of course, ease the connection to the multiplex wiring bus.

SUMMARY

Over the past several minutes, I've reviewed the key challenges and opportunities facing those of us in the electronics community. I have no doubt that all of these challenges and opportunities will be fully exploited.

I began this talk by emphasizing the need for quality parts and I want to end on the same note.

I urge all of you to consider the issue of quality, its short-term and long range implications.

Quality products--supported by a quality attitude throughout the industry--is the key to the present and the future.

Quality electronics, designed and manufactured to exacting standards, will earn us the worldwide consumer acceptance we all aspire to. This may sound like a philosophy we all learned in Engineering 101, but, unfortunately one that hasn't always been fully embraced.

Ford has the Q1 Preferred Quality Supplier Program that provides recognition to suppliers who have consistent high levels of product quality. These suppliers are rated on a number of criteria that takes into consideration the supplier's overall quality effort. The semiconductor companies rated Ford Q1 are listed on this slide.*

I congratulate the management and employees of these firms for their dedication to quality workmanship.

At Ford, we're committed to make quality an inherent ingredient of our corporate culture. It must be a basic commitment in every employee's work ethic.

I hope that all of our suppliers (and potential suppliers) adopt a similar corporate-wide perspective.

In closing, I'd just like to emphasize that the time to move forward on the worldwide electronics front has never been more pressing.

We can identify our challenges. We can see our opportunities. We can take action to achieve our mutual goals.

The automotive industry and Ford Motor Company welcomes your ideas, innovation, and enthusiasm.

Thank you.

* The Ford Q1 semiconductor companies are:

Cherry Semiconductor; East Greenwick, Rhode Island
General Instruments; Hicksville, New York
Motorola; Phoenix, Arizona
NEC; Fukui City, Japan
RCA; Mountaintop, Pennsylvania
Sprague; Concord, New Hampshire
Texas Instrumments; Dallas, Texas
Toshiba; Kawasaki, Japan

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PROMISES AND DELIVERIES--
MEETING SEMICONDUCTOR COMMITMENTS

Bengt R. Soderberg
Vice President of Corporate Purchasing
L M Ericsson

Mr. Soderberg has been Vice President of Corporate Purchasing at L M Ericsson since 1977. Previously, he was Director of Corporate Purchasing and held positions in marketing management at L M Ericsson. Earlier in his career, Mr. Soderberg was Worldwide Marketing Manager of Svenska Ackumulator AB Jungner. He received a degree in Electrical Engineering at Orebro, Sweden.

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PROMISES AND DELIVERIES - MEETING SEMICONDUCTOR COMMITMENTS

BENGT R SODERBERG
Vice President - Corporate Purchasing
L M Ericsson Telephone Company, Stockholm, Sweden

If this is the reaction from the semiconductor industry to perfectly normal purchase conditions in normal times, if there were ever normal times in that industry, what is it like under extreme conditions?

We know. Let me tell you.

To my knowledge, Dataqeust never took the initiative to thoroughly penetrate the important question of on-time-performance. Even though I have full understanding of the fact that this audience could be what I call Japan-allergic, you cannot deny being familiar with the just-in-time concept. The only time it has been mentioned at a Dataquest conference, apart from my repeated appearances, I believe was in Tuscon where someone made a presentation entitled "How to motivate suppliers to deliver on time". Unfortunately we were only presented with the report on how the suppliers had performed, no comments on how to motivate them, which was indeed a pity because this is just what I have failed to do over all these years I have been in this business.

The reason for the change of his concept might have been that all speakers at Dataquest conferences have to present their papers in written form so early that with the speed the market is changing today, it might very well have been such a drastic change that he completely lost interest in motivating the suppliers.

I have always made a point of Dataquest's importance for the semiconductor market. I might at times even have hinted at the possibility of Dataquest having two difference subscription fees, one for the manufacturer and a lower one for the user, because how else could it be that I always find my price much lower than the one indicated by Dataquest?

A joke of course, but very often that leads you to an interesting piece of information.

What I refer to in this case, though, is how Dataquest's influence proved to be very strong.

Even long after the market turned down, our suppliers continued to perform unsatisfactorily, at least to our standards. Only when I threatened them that at a forthcoming Dataquest conference I would list the suppliers with names and performances, did some of them start to shape up. It even happened that a representative of one of the most important semiconductor manufacturers in this country counted on his fingers to see how many months he had to shape up before the next Dataquest meeting.

The result at one time was such an influx of parts that, even introducing a second shift at our receiving dock, we still fell terribly behind in even registering the receipt, resulting in some unjustified complaints to some suppliers - sorry, Motorola - I apologize.

When I suggested to Dataquest that I would take up this matter at one of their coming meetings and that I would indeed start spilling names and figures, I was in a very mild but ever so firm manner advised that should I make a presentation, it was suggested that I would in no way offend any specific supplier, which meant that I was free to tell what I think of you as a group but not name any individual company or manufacturer.

Living in a country with a strong socialistic tendency, which I oppose and where you are always told to see the value of the group performance rather than the individual one, I was disappointed.

Much to some people's relief I therefore have to adhere to the instructions or else ..... Not that I know what or else would mean in this case but let me be honest while I still have a chance.

I must agree that for once I am late but this time only with the presentation. Preferably, it should have come at last year's October meeting. Seeing the book-to-bill ratio as presented by SIA in this slide where the book-to-bill ratio dropped below 1:1 already in August last year lead us all to be very optimistic that things would shape up pretty soon.

However, with fall falling and early winter approaching, things did not improve, as this slide shows. Very few new orders came in to the industry and that to such a degree that people were laid off and/or sent on unpaid leave. With that I had hoped that the suppliers should have had ample time to carry out the orders that they already had in their books, because our orders were there when the trouble started and they were there when others withdrew.

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Superimposing the book-to-bill curve on the on-time-performance curve shows a very distinct relation between the two. I wonder why, because our orders have been dropping in steadily over the years, come rain or shine, and as long as I have anything to say, it will be continued in the same way.

But let us look a bit at the world around us to put the whole thing in perspective.

May I start with my immediate vicinity? - Ericsson.

We have been in business for over 100 years now and have shown a steady growth at an average of 15% a year, at least looking at the last ten years, and that on a market that has a growth of roughly 7%.

Our overall purchase volumes have shown an annual growth of roughly 21% over a ten year period, and our semiconductor purchases have demonstrated a staggering 45% over the last five years. Even though I believe we are probably among the world's 10-15 largest users of semiconductors, our usage only represents somewhere between 1 and 2% of the world's consumption. I think, though, that with this I have established us a steady customer with little fluctuations in our upward trend as semiconductor buyers.

Looking back, I feel that the computer industry was indeed the basis for mass usage of semiconductors, a market with ever increasing need of new generations of parts.

The need for mass memories in computers certainly made automatic production possible. Very seldom did it happen that the computer market variations had any adverse effect on the shipments of parts to us; perhaps with one or two exceptions, like the ones when Big Blue turned to outside vendors for the famous piggy back 32k memory.

At that time, at least one manufacturer told us that if we insisted on buying from him, the price for the standard part would be roughly twice that of the market, but there were at least ten other manufacturers who could help us.

So much for computer usage.

At the consumer end though, I think we can see the beginning of a problem pattern.

In the beginning, any semiconductor manufacturer with self-esteem had to have a watch on his program and later a calculator. I do not think that anyone ever made a lot of money on those products with few exceptions though. I think, however, it established a pattern that would later prove disastrous. Even though the semiconductor usage of watches and calculators never ever threatened the supplies to other users, the manufacturers of those two products failed to realize two things, actually being two sides of the same coin, viz.that there are such things as market saturation. It very seldom occurs that a number of suppliers can, each of them, secure more than 100% of the market.

When games started to come into the picture, few of the semiconductor makers were directly involved but game manufacturers showed up on the market, everyone with a fantastic ambition. It even went so far as to threaten the traditional Pachinco saloons in Japan's electronic game saloons started to invade the market.

The sophistication grew, and the step from games to home computers was not very far. If you should draw the conclusion from the enormous increase in semiconductor requirements again, everyone was aiming at more than 100% of the market.

The more complicated the home computers grew, and of course even more so after Apple's success and IBM's entering the market, the higher the usage rate of semiconductors was - to a point where personal computers represented roughly 20% of the world's production. Such a rapid growth for a new product naturally attracted every semiconductor manufacturer, and soon everyone was fully booked and overbooked, and I do not hesitate to say that everyone was heading for chaos.

The remedy: allocation. It is a terrible word for anyone operating on the basis of a seriously meant volume purchase agreement with agreed on call-off times and even with confirmed call-offs. We had thought that signing an agreement still meant something but how wrong we were!

This would illustrate what I mean. It is, I repeat, a free translation of a letter I got from a component supplier. Just imagine he had been booking so many orders that he could not respect the orders he had already committed himself to deliver.

Is there a way to analyze the situation?

Why is it that orders that were placed even a year earlier were delayed?

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I know that at times you loose the formula. At other times a whole production run may go wrong but usually, based on statistics, the possibility of this happening should be well covered.

So let us rule this reason out.

At earlier times delays were always blamed on the difficulty of keeping track of production worldwide. Diffusion in one part of the world, assembly in another and final testing in the third followed by centralized shipments from a fourth. With all sophisticated communication systems available everywhere, I think that that excuse could also be ruled out today. That leaves us with very few alternatives.

One is order processing. It seems that, mostly, orders are entered under the black box philosphy. They are keyed into a system, and at best months later products come out at the other end. What happens in between is often intraceable, uncontrollable and because of that often lost. Companies where an Ericsson order could be traced all through the system have shown that they can handle even such things.

The way the orders are booked might be another complication. Salesmen in local offices often accept orders and acknowledge them on general information of the availability of the product. In the meantime things might have changed, and those lead-times no longer apply. I think though, that even that could be overcome.

I think though that we are approaching the heart of the matter. -The salesman.

At least in this country, he is judged by the orders he books now, not what he digs up that might result in substantial orders two or three or five years from now. For all he knows, he might have been promoted because of the short orders he booked or he might very well even work for another company. So to him it is always new business he is after.

One thing is of course <u>when</u> you get shipments, another and certainly not less important <u>what</u> you get.

To my knowledge, the just-in-time concept includes such a good vendor/customer relationship that not only do you get the parts on time but you can also send them straight onto the assembly line without too much testing.

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We all see all kinds of fantastic claims from semiconductor manufacturers, indicating that the quality they deliver in usually is in less than a two-digit count on PPM.

Promises, promises!

We would love to see it but unfortunately sample testing shows a totally different picture.

A recent survey as late as of the second quarter this year shows that no less than 33.8% of all shipments received were rejected after sample testing. This corresponds to 43.4% of the number of components received. Failures were mainly electrical but a minor part also resulted from leakage problems in the hermetically sealed versions we use exclusively.

In normal times those shipments should have been returned to the vendor for replacement. Times being, however, what they were, we could not afford to do that. We had to submit them to a 100% testing, a costly and lengthy process. In the end .71% of the total quantity of the components was rejected which might seem comparatively low but when you consider the cost of testing, it is no longer negligible.

Now let us go back to the SIA book-to-bill ratio.

This is how the number of rejected shipments at the incoming inspection have varied over recent months. There is a very clear tendency that orders booked at the highest point of the book-to-bill ratios show a lower quality when they are delivered. If you add to this that in shortage times the number of partial shipments increase drastically so that in this way you receive about 50% more shipments than asked for, a rough estimation of the increased testing cost, added forwarding cost, invoice handling and all that results in an estimated increase in part cost of up to 6%. Should we calculate the loss of production based on the delay for the testing, the figures would be even higher. Compare that to the total purchasing cost that my department rings up of .7%, and you see how serious the matter is.

On previous occasions I have suggested a certain similiarity between the semiconductor industry and a beautiful woman, never to be fully understood and therefore even more tempting. I even alluded at her not being faithful to you just because you promised to be faithful to her.I still think she was beautiful. I still think she was mysterious but beauty sometimes fades. I know that analyzing a thing like that sometimes make you disappointed.

With medical knowledge now in my family I have slowly and cautiously come to arrive at the diagnostic picture.

Have you heard of the desease anorexia? The one when a girl knows that she has to eat moderately to stay slim and attractive but cannot resist the temptation of grossly overeating all goodies she can lay her hands on at certain intervals, only to realize how wrong it was and then doing everything in her power to throw it all up.

Doctors say, however, that you should not despair. Cure is just around the corner if you only want to listen.

In the case of the semiconductor industry, it is suggested that you look at the track record. It should lead you to realize that all those new products with the phenomenal growth , using semiconductors, are not all going to turn to gold. Have they not all withered to a higher or lesser degree or at least stopped growing while among others the old faithful, the telecommunication industry, continues to grow and will, unlike many other products, be there long after next father's day and next and next and next .....

Nielsen Dataquest

THE FUTURE OF GALLIUM ARSENIDE INTEGRATED CIRCUITS

Anthony Livingston
Vice President, Marketing and Sales
GigaBit Logic Inc.

Mr. Livingston is Vice President of Marketing and Sales at GigaBit Logic Inc., a start-up gallium arsenide IC manufacturer. Previously, he held various positions in marketing management at Intel Corporation. Prior to that, Mr. Livingston was employed by Fairchild Semiconductor. He received his B.S.E.E. degree from the University of Arizona.

Dataquest Incorporated
SEMICONDUCTOR INDUSTRY CONFERENCE
October 14, 15, and 16, 1985
Tucson, Arizona

THE FUTURE OF GALLIUM ARSENIDE IC'S

GBL GigaBit Logic

SILICON: WORKHORSE FOR DECADES

- BASIC MATERIAL FOR SEMICONDUCTORS
- CREATED THE STANDARD INTEGRATED CIRCUIT FAMILIES
- EMERGED AS A MAJOR ECONOMIC FORCE
- ENGINE OF THE INFORMATION AGE

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GALLIUM ARSENIDE: WORKHORSE FOR A NEW ERA

- BASIC MATERIAL FOR HIGH PERFORMANCE IC'S
- CREATION OF NEW HIGH PERFORMANCE STANDARD INTEGRATED CIRCUIT FAMILIES
- EMERGENCE AS A MAJOR ECONOMIC FORCE IN HIGH PERFORMANCE COMPUTER AND ELECTRONIC SYSTEMS MARKETS
- ACCELERATION OF THE INFORMATION REVOLUTION

GBL GigaBit Logic

ADVANTAGES OF GaAs INTEGRATED CIRCUITS

- High Electron Mobility and Velocity
  - Very High Switching Speeds
  - High Speeds Achievable in Low Voltage Operation
- Semi-Insulating GaAs Substrate Material
  - Very Low Parasitic Capacitances
  - Fabrication Simplicity ("Automatic" Isolation, Interconnect Metal Directly on Semiconductor)
- Effective Schottky Barrier Technology
  - MESFET Active Devices
  - Schottky Diodes
- Wide Band Gap
  - High Temperature Operation
  - Radiation Hardness

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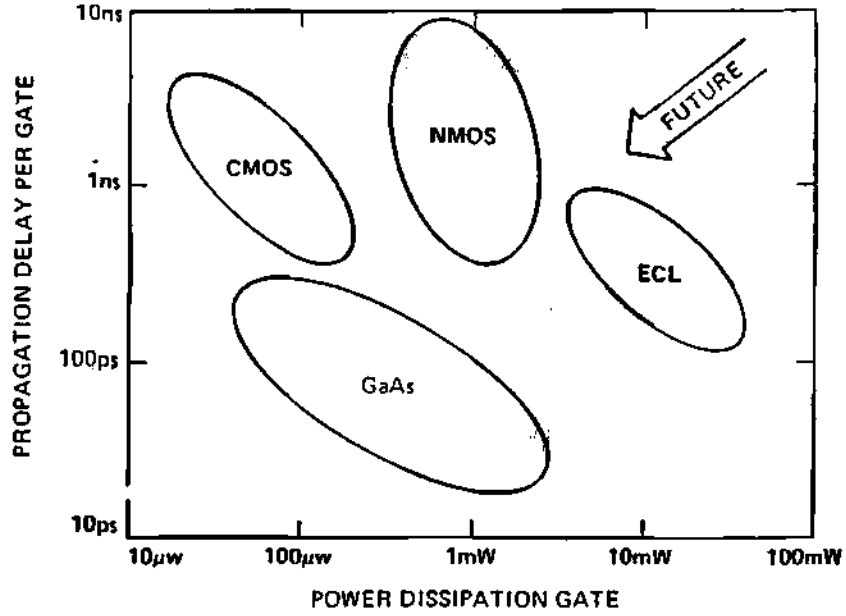
SPEED/POWER PERFORMANCE OF
INTEGRATED CIRCUIT TECHNOLOGIES



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APPLICATIONS AREAS FOR GaAs IC's

- Computers
  - Supercomputers (Scientific), Mainframe Computers (Business)
  - RAMs, Gate Arrays, Multipliers, ALU's, PLA's, ROMs
- High Speed Instrumentation
  - Communications Test Sets, VLSI Testers, Logic Analyzers, Digital Oscilloscopes, μ-Wave Equip
  - RAMs, Flip-Flops, MSI/SSI Logic, Analog Circuits, A/D, D/A

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APPLICATIONS AREAS FOR GaAs IC's

- **Communications**
  - **Communications Systems in Various Media Including Microwave, Coaxial Line, Fiber Optical, VHF/UHF/μW Radio**
  - **Repeaters, R.F., A/D, D/A, Multiplexer/ Demultiplexer**
- **Military/Space (Including Other Signal Processing Applications)**
  - **Satellite Communications, Data Encryption/Decryption, ECM, ELINT**
  - **Multiplier/Accumulators, Correlators, Custom Encryption/Decryption Circuits, Variable-Modulus Dividers, RF Memory**

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GaAs IN PRODUCTION

- 3 Inch GaAs Wafers of Good Quality are Available
- Directly Transferrable Si Processing Techniques and Equipment
  - Dry Processing - Plasma Etching
  - Ion Implantation
  - 1 μM Photolithography
- A Number of System Manufacturers Have Committed Themselves to the Utilization of GaAs IC's (HP, Cray, Tektronix, Hughes,...)

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LARGE MARKET DEVELOPMENT REQUIREMENTS

- Ten Significant Merchant Suppliers Worldwide
- Standardization
  - Power Supplies
  - Logic Levels (ECL Compatible)
  - Packages
- Second Source Agreements
- Acceptance by System OEMs

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COMPETITION
(TODAY)

MERCHANT	AEROSPACE/ CAPTIVE	START-UPS
Harris	Ford	GigaBit Logic
TriQuint (Tektronix)	Honeywell	Pivot III-V
	Rockwell	Vitesse

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COMPETITION
(FUTURE)

JAPAN	UNITED STATES		EUROPE
	Merchant	Aerospace/ Captive	
Fujitsu	GigaBit Logic	Ford	Phillips
Hitachi	Harris	Honeywell	Plessey
NEC	Motorola	Hughes	STC
OKI	TI	Rockwell	Thomson
Toshiba	TriQuint	???	???
???	Vitesse		
	???		

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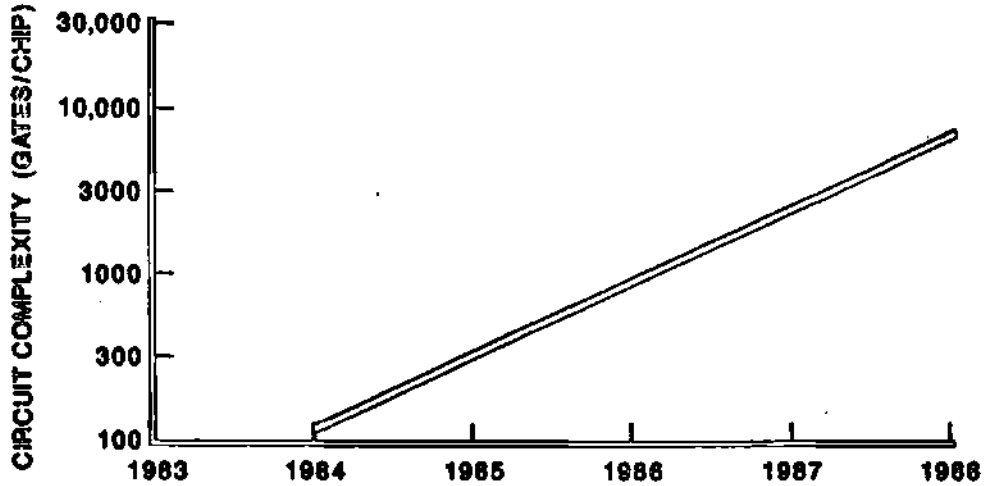
GaAs DIGITAL LOGIC COMPLEXITY (COMMERCIAL INTRODUCTION)



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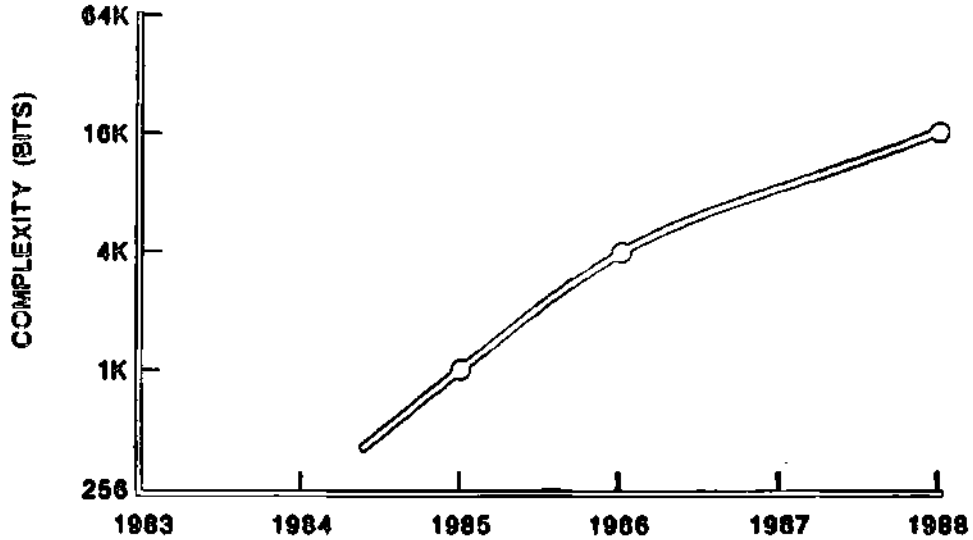
GaAs STATIC RAM COMPLEXITY (COMMERCIAL INTRODUCTION)



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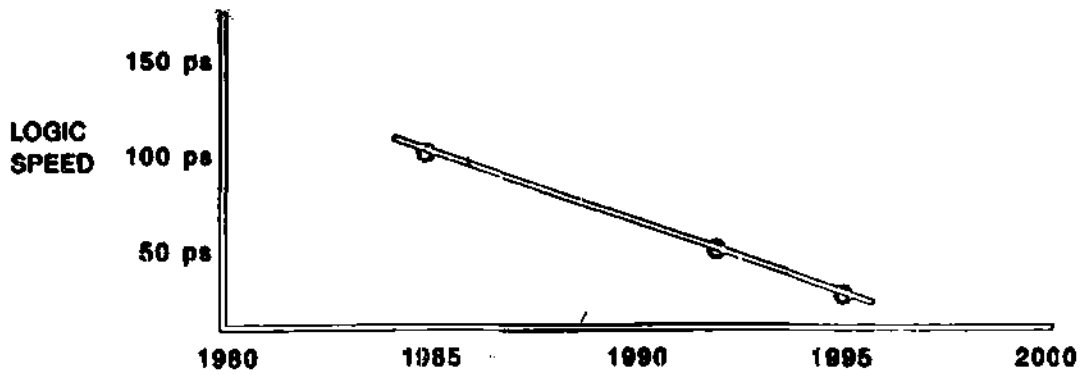
SPEED ENHANCEMENTS



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GaAs PRODUCTION TECHNOLOGY

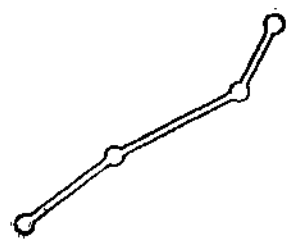
1980 1985 1990 1995 2000

HJ-BIPOLAR

HEMT

E-MESFET

D-MESFET



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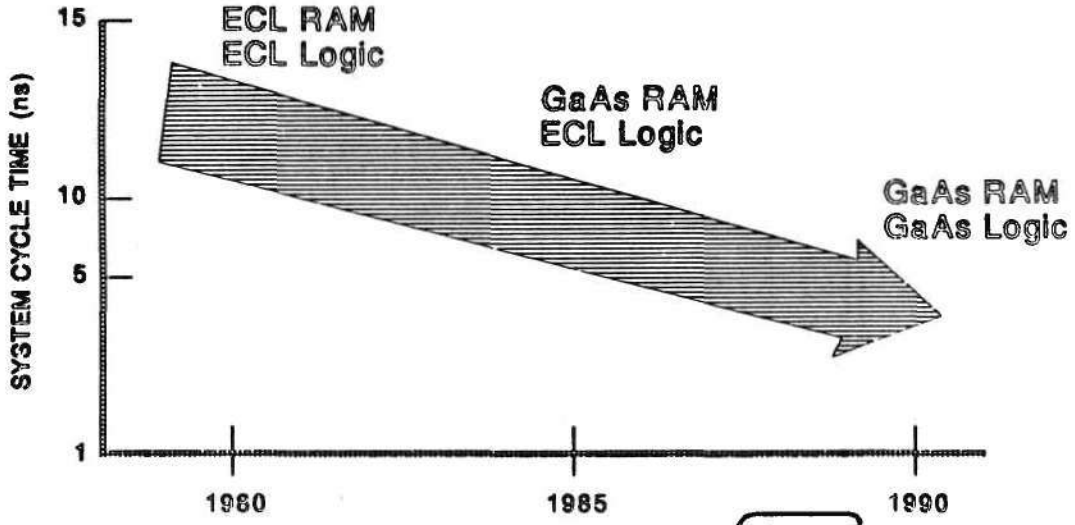
SYSTEM PERFORMANCE TRENDS
UTILIZATION OF GaAs RAM AND LOGIC



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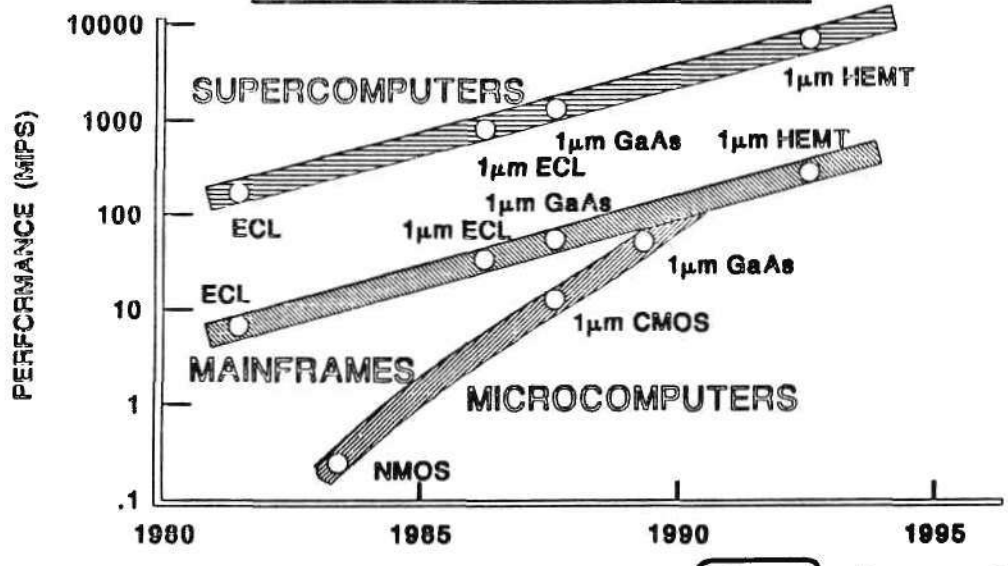
IMPACT OF GaAs IC'S
ON SYSTEM PERFORMANCE



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GaAs IC MARKETS
COMMERCIAL AVAILABILITY ATTRACTS BROAD APPLICATIONS

- COMPUTERS - SUPERCOMPUTERS TO SUPERMINIS
- COMMUNICATIONS - FIBER OPTICS TO MICROWAVE
- INSTRUMENTATION - VLSI TESTERS TO OSCILLOSCOPES
- MILITARY - COUNTERMEASURES TO CONTROLS
- CONSUMER - DIRECT SATELLITE BROADCAST TO VIDEODISKS

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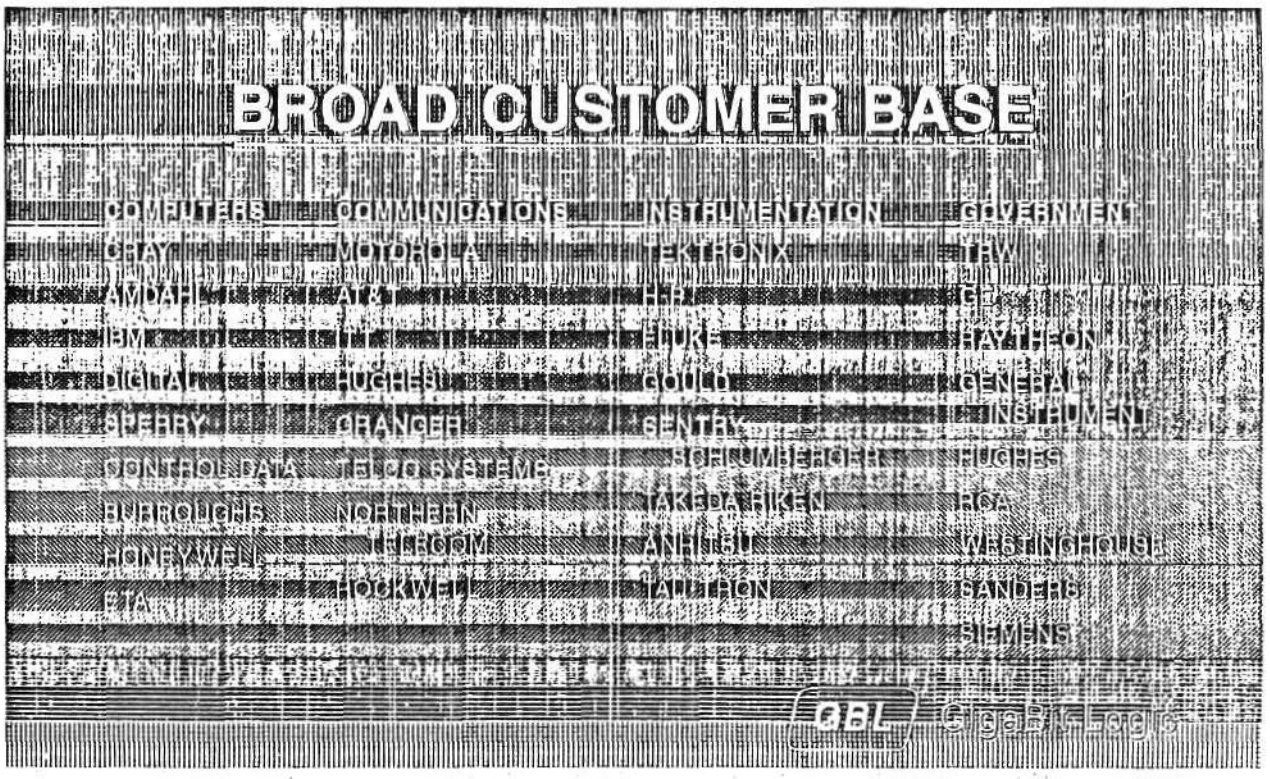

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GaAs IC PRODUCT CATEGORIES
BROAD RANGE OF CAPABILITIES

- STRONG BASE IN ANALOG FUNCTIONS (ESPECIALLY AT MICROWAVE FREQUENCIES)
- DIGITAL LOGIC, MEMORY, AND MICROPROCESSORS GROW TO MAJORITY AS IN SILICON
- INTEGRATED OPTOELECTRONICS OFFERS NEW FUNCTIONS

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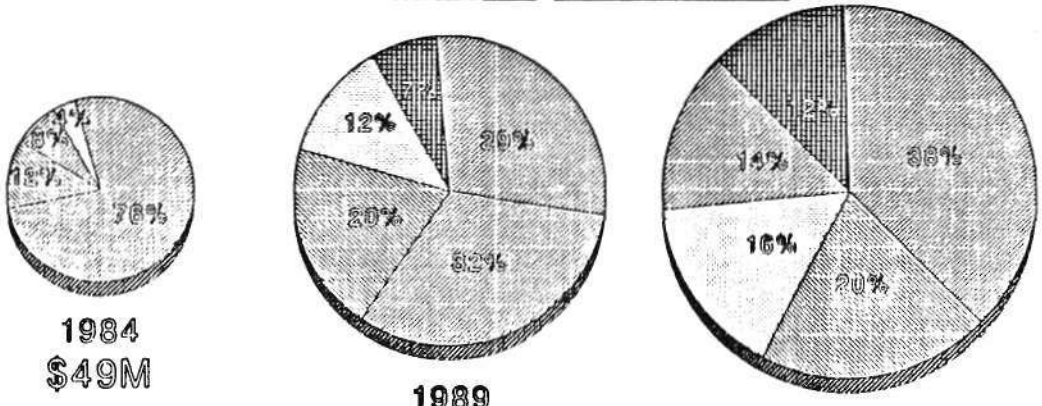
WORLDWIDE GaAs IC MARKETS BY MAJOR PRODUCT SEGMENT



1984
$49M

1989
$1,296B

1994
$13,514B

COMPUTERS
COMMUNICATIONS
INSTRUMENTATION
MILITARY
CONSUMER

SOURCE: STRATEGIC INCORPORATED

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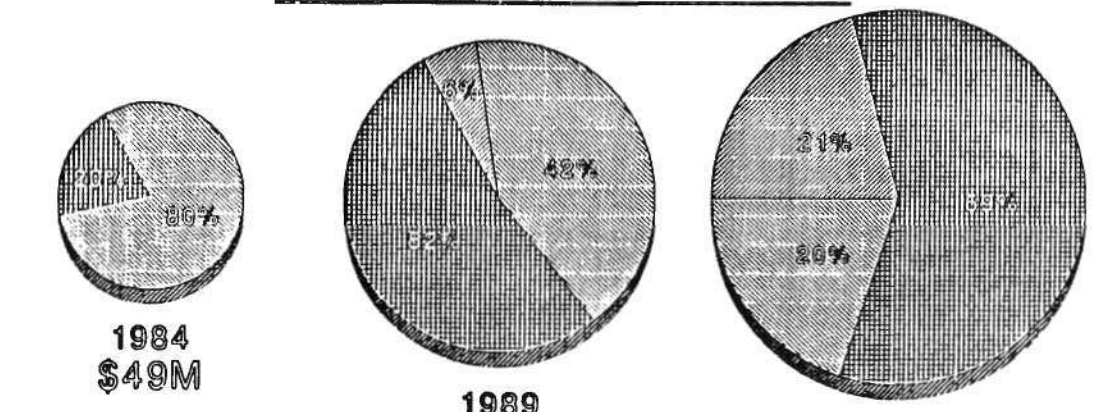
WORLDWIDE GaAs IC MARKETS BY MAJOR PRODUCT CATEGORY



SOURCE: STRATEGIC INCORPORATED GBL GigaBit Logic

GaAs IC'S IN THE EARLY 1990'S

- COMMERCIAL MARKET SEGMENTS WILL DOMINATE
- DIGITAL PRODUCTS WILL BE THE LARGEST PRODUCT CATEGORY
- GaAs WILL CAPTURE OVER 5 PERCENT OF A TOTAL IC MARKET OF MORE THAN $100 BILLION

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