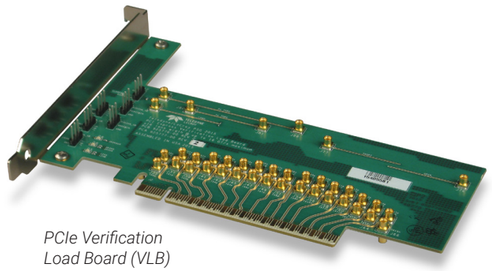
Test Fixtures

Two test fixtures are also available to help with testing PCIe 4.0 devices: a PCIe Verification Load Board (VLB—shown here) for testing PCIe platforms such as server or mother boards, and the PCIe Validation Base Board (VBB) for testing PCIe Add-in Cards. Each of these test fixtures will aid developers in conducting electrical tests.



PCIe Verification Load Board (VLB)

Specifications

Host Machine Minimum Requirements	Microsoft Windows® 10, Windows 8.1, Windows 7, Windows Server 2012, Server 2008R2; 2 GB of RAM; storage with at least 600 MB of free space for the installation of the software and additional space for recorded data; display with resolution of at least 1024x768 with at least 16-bit color depth; USB 2.0/3.0/3.1 port and/or 100/1000 Mbps Ethernet network interface. For optimal performance, please refer to our recommended configuration in the product documentation.
Recording Memory Size	Up to 8GB
Data Rates Supported	2.5 GT/s, 5 GT/s, 8 GT/s and 16 GT/s (PCI Express 4.0)
Ports	Summit Z416 Slot Interposer: Connector to Controller, x16 PCIe Edge Connector (to connect to DUT— requires two CEM-socket space in backplane) Summit Z416 Controller: Connector to Interposer, USB Type-C, 1000BASE-T Ethernet, Sync/Data, DC Power (from supplied adapter)
Display Panel	Eight character alphanumeric display
LEDs	Power LED, Status LED, Trigger LED, Four Data Rate LEDs (2.5 GT/s, 5 GT/s, 8 GT/s, 16 GT/s), 32 Activity LEDs (2 per lane—Tx/Rx—for 16 lanes), Training LED
Dimensions and Weight	Summit Z416 Slot Interposer: 100 x 198 x 170 mm (3.9” x 7.8” x 6.7”), 1.4 Kg (3 lb) Summit Z416 Controller: 114 x 19 x 207 mm (4.5” x 0.76” x 8.15”), 1.0 Kg (2 lb)
Power Requirements	100-240 VAC, 50-60 Hz, 230W
Environmental	Operating: 0 to 55°C (32 to 131°F) Non-operating: -20 to 80°C (-4 to 176°F) Humidity: 10 to 90% non-condensing

Ordering Information

Product Description	Product Code
Summit Z416 (licensed as a Gen4 x16 exerciser, supports host and device emulation, PXP-400 Test Platform required for Gen4 add-in card testing) [Other license options also available]	PE090AGA-X
PXP-400 G4 DVT Test Platform	PXP-400A-X
VLB (Verification Load Board)	PE118UIA-X
VBB (Verification Base Board)	PE119UIA-X

Local sales offices are located throughout the world.
Visit our website to find the most convenient location.
1-800-5-LeCroy • teledynelecroy.com

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TELEDYNE LECROY
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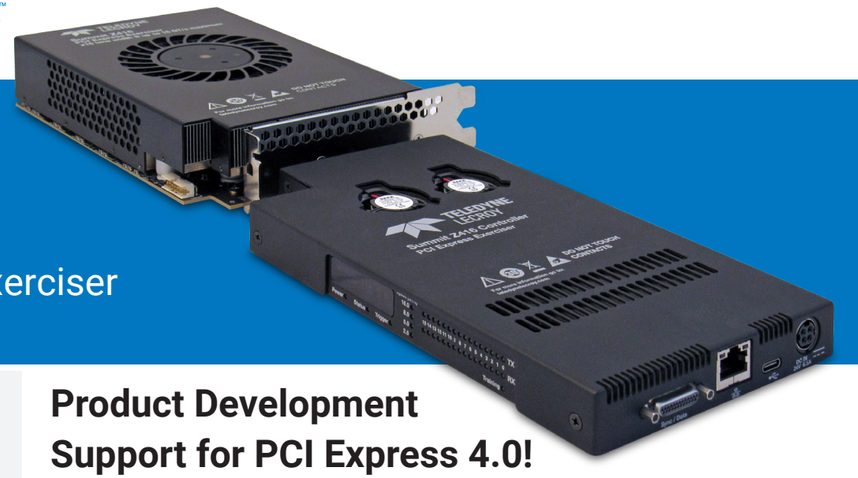
Summit™ Z416

PCI Express® 4.0 Protocol Analyzer Exerciser



Product Capabilities

Exerciser
- x1 to x16 link width
- Data rates to 16 GT/s
- Powerful scripting
- Lane reversal
- Auto-polarity
- Lane scrambling
- Error injection
- Host/Device emulation

Protocol Analysis
- x1 to x16 link width
- LTSSM display
- CATC Trace™ views
- Spreadsheet view
- Trace Expert™ analysis

Test Fixtures
- Verification Load Board (VLB)
- Verification Base Board (VBB)

Test Platform
- x1 to x16 link width
- Data rates to 16 GT/s

Key Features

Find errors fast
- One button error check
- Fast upload speed
- Large trace memory
- Powerful triggering/filtering

See and understand the traffic
- Get useful information
- More choices of data views
- More ways to analyze data
- Verification Script Engine

Accurate data capture
- 100% data capture
- x1 to x16 link widths
- Data rates to 16 GT/s

Product Development Support for PCI Express 4.0!

The Summit Z416 exerciser is designed for developers who need a protocol test system supporting the PCI Express 4.0 specification. Supporting traffic generation at data rates to 16 GT/s with link widths up to 16 lanes, the Summit Z416 is Teledyne LeCroy's fifth generation PCI Express (PCIe) protocol exerciser, leveraging years of experience in providing advanced protocol test tools to the PCI Express community.

In addition to traffic generation, the system also supports protocol analysis capability, featuring the industry-standard CATC Trace as well as a wide variety of other traffic displays and data reports.

The Summit Z416 supports full traffic generation and device/host emulation, as well as providing the industry a platform for development of standardized compliance test suites.

In addition the system provides error injection functions to enable developers to test error recovery routines important to reliable interoperability of PCI Express 4.0 products.

Typical Applications

The Summit Z416 is a critical test and verification tool to assist engineers in development, debug and validation of their PCIe designs (including early stage power-on testing). Because of its rich programmable environment, scripting can be used for full interoperability testing, improving the reliability of systems.

The Summit Z416 can emulate either PCIe root complexes or device endpoints, allowing new designs to be tested against known standards.

PCI EXPRESS®

A Wealth of Features

Intuitive software controls blend sophisticated traffic generation and analysis capability with ease-of-use, allowing test suites to be rapidly customized to meet specific test requirements. One feature that helps troubleshoot PCIe links is the ability to fully exercise the Link Training & Status State Machine (LTSSM) transitions. The powerful scripting language also allows for the creation of Transaction Layer Packets (TLPs) and Data Link Layer Packets (DLLPs) at PCIe 4.0 data rates of 16 GT/s. Flow Control and ACK/NAK's policies and structures can be defined and generated under user control. Features addressing LTSSM structures include providing bus traffic to emulate all the states of the LTSSM from the Detect state, to the L0 state and maintaining the L0 state between the host and device. The exerciser also supports lane reversal and can control all polarity and scrambling configurations. An important feature to note is that traffic emulation supports dynamic equalization and Skip EQ training and can handle autonomous speed switching between all combinations of speeds. The exerciser also has the capability to perform error injection for training sequences, as well as standard traffic, both at the packet level and on a per lane basis.

Packet fields not explicitly specified by the user are generated automatically (such as packet numbering and CRCs). The configuration space can be emulated for any device including endpoints, bridges and switches. Support for all PCIe 4.0 data rates allows the Summit Z416 to produce test cases that test the device's ability to auto-negotiate data rates with other devices.

In addition, the ability of the Summit Z416 to produce a wide variety of programmed traffic allows the user to introduce controlled error conditions. As an example, a trace file captured in the Analyzer can be exported and used as the basis for a test script, with selected programmed errors introduced at critical stages to test the device's ability to recognize and recover from error conditions. This allows for detailed testing of simple error recovery and complex multiple error conditions, creating more resilient products that perform well even under less than ideal conditions.

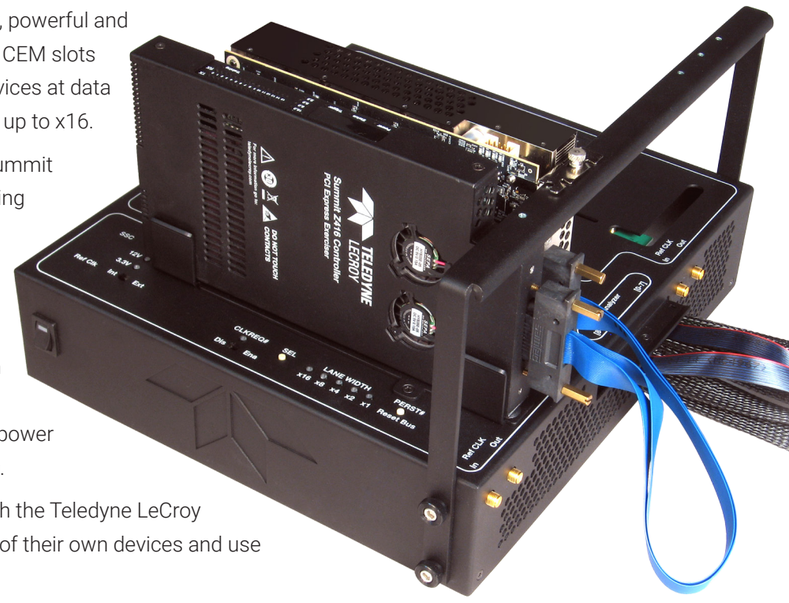
Protocol Analysis Included

The Summit Z416 can also support up to sixteen (16) lanes of protocol analysis. Using its high speed trace memory (up to 8 GB), the Summit Z416 can monitor, capture, decode and analyze PCIe protocols with data rates up to 16GT/s (Gen4). The application display is highly configurable and can be modified to most users' debugging styles. Many features are available including a hierarchical display, protocol traffic summaries, detailed error reports, timing calculators, bus utilization graphs, and the ability to create user-defined test reports allowing developers to troubleshoot intricate problems and finish their projects on time.

PCIe storage decodes such as NVMe, SATA Express (AHCI and ATA), SCSI Express (PQI and SOP), TCG (Trusted Computing Group), Precision Time Measurement (PTM) and virtualization decodes such as Single and Multi-Root I/O Virtualization (SRIOV and MRIOV) as well as Address Translation Services (ATS) are available to broaden its capabilities to many different industry segments.

PXP-400 Test Platform Provides Host Emulation

Teledyne LeCroy's PCIe 4.0 Test Platform for the Summit Z416 Protocol Exerciser provides a convenient, powerful and flexible system (occupying two standard CEM slots on the backplane) for emulating PCIe devices at data rates up to 16 GT/s and with lane widths up to x16.



The PXP-400 Test Platform allows the Summit Z416 to also act as a host system, enabling extensive protocol-level testing of PCIe devices. For use as a host emulator, the Summit Z416 is plugged into one of the PCIe x16 slots on the PXP-400 and connected to the power source, then the Device Under Test (DUT) is plugged into the alternate PCIe x16 slot with slot power provided to the DUT by the Test Platform.

In addition to using the Test Platform with the Teledyne LeCroy Summit Z416, the user can connect two of their own devices and use the Test Platform as a PCIe backplane.

Packet				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols
4	R←	16.0 x1	TS1	0	0	0	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	0 0 15 0	63	63	63	4A 4A 4A 4A 4A 4A

Packet				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	FS	LF	Post-Cursor	TS1 Symbols	Idle
5	R←	16.0 x1	TS1	0	0	0	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	1 0 15 0	63	63	63	4A 4A 4A 4A 4A 4A	10.000 ms

Packet				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	TS2 Symbols	Idle	Time Stamp
6	R←	16.0 x1	TS2	0	0	0	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	32 1 1	45 45 45 45 45 45 45 45 45 45	10.000 ms	0000 . 070 000 600 s

Packet				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	TS2 Symbols	Time Stamp
7	R←	16.0 x1	TS2	0	0	0	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	32 1 1 0 0	45 45 45 45 45 45 45 45 45 45	0000 . 080 000 700 s