Innovative Thinking for Power, Control and Instrumentation

OZDSP1000
TMS320F2812 Control Board
User's Manual
UM-0043

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1. Introduction

This document is intended to provide instruction on how to employ the Oztek OZDSP1000 controller in a power converter hardware system. It describes the electrical connections and interface details.

1.1 Referenced Documents

Ref.	Document	Description
[1]	FS-0001	OZDSP1000 FPGA Functional Specification
[2]	UM-0016	OZDSP1000 Test Application User's Manual
[3]	*SPRS174*	*Texas Instruments: TMS320F2810, TMS320F2812 Digital Signal Processors*

1.2 Definitions

AFE	Active Front End
CAN	Controller Area Network
DSP	Digital signal processor
EEPROM	Electrically Erasable Programmable Read Only Memory
EMC	Electro-magnetic compatibility
EMI	Electro-magnetic interference
GND	Ground, low side of input power supply
GTI	Grid Tied Inverter
GUI	Graphical User Interface
HMI	Human Machine Interface
IPM	Intelligent Power Module
N.C.	Not connected
PCB	Printed Circuit Board
PCC	Power Control Center
PLC	Programmable Logic Controller
PLL	Phase Locked Loop
POR	Power On Reset
PWM	Pulse width modulation
SVM	Space Vector Modulator

2. Functional Description

The OZDSP1000 is a highly integrated DSP control solution for power control applications. Based on the Texas Instruments 150MHz, TI TMS320F2812 Digital Signal Processor, the controller offers the state of the art in digital control capability. Interface circuitry is provided for the following peripherals as illustrated in Figure 1:

- RS232 Communications Port
- Second Selectable RS232/485/422 Communications Port
- CAN Bus Communications Port
- Incremental Encoder Interface
- Hall Effect Position Sensor Interface
- 4 Relay Drivers
- Debug PWM DAC
- 2 EEPROMs
- 512kx16 external SRAM
- 4 OptoIsolated Inputs
- 4 OptoIsolated Outputs
- 2 Semikron Three Phase Power Module Interfaces via:
    - Single "GD" Interface
    - Three "GB" Interfaces
- 1 Semikron Half Bridge or Brake Interface "GB" Interface
- Isolated High Voltage Line Sensing
- Isolated High Voltage Output Sensing
- Oztek Expansion Support
- JTAG Debug Interface

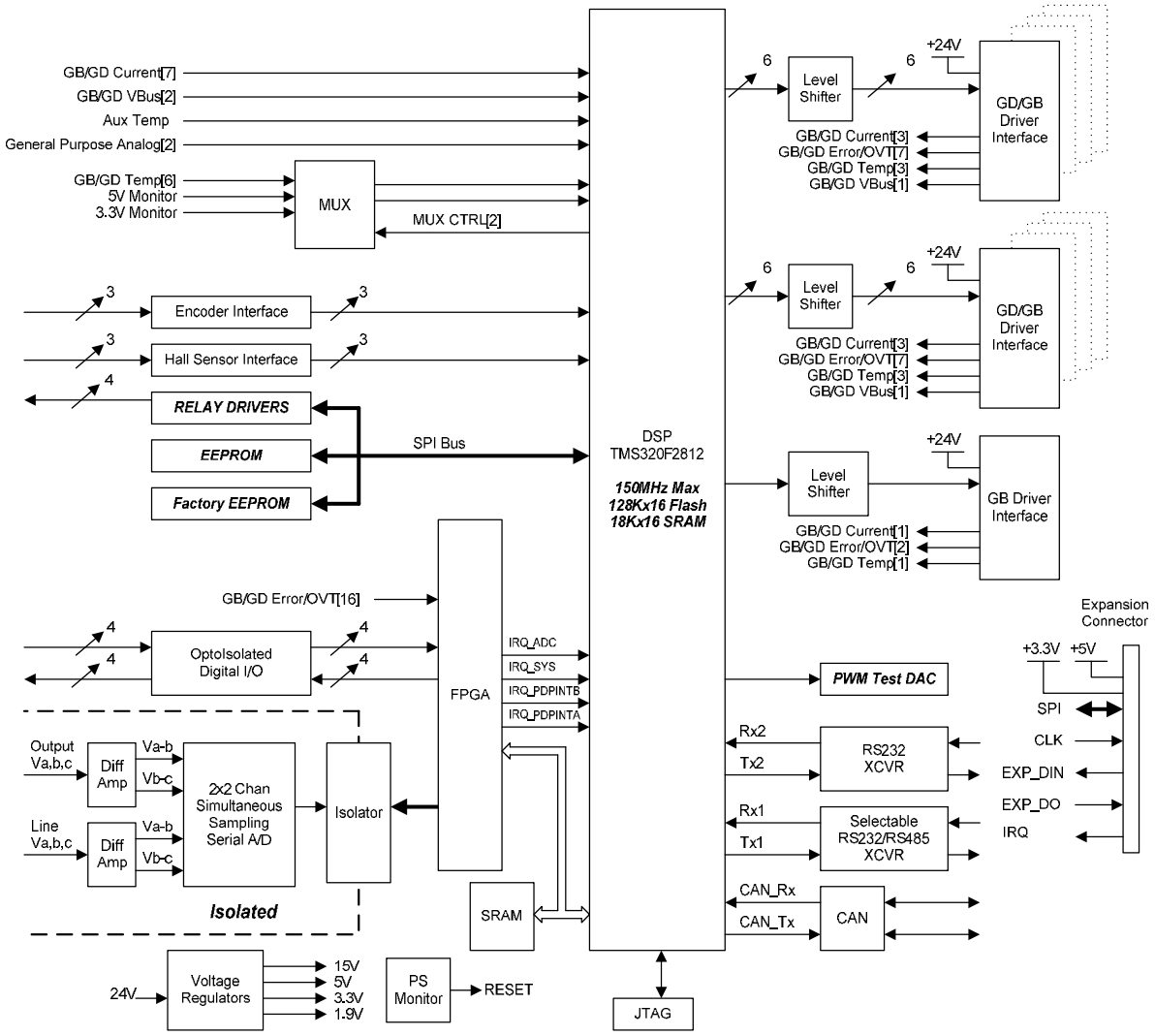


Figure 1 – OZDSP1000 Block Diagram

Typical applications include voltage output inverters, grid-tie inverters, AC induction motor controllers, brushless DC motor controllers, Active Front-End regulators and high power DC/DC converters.

3. Environmental Specifications

3.1 Operating Temperature

The OZDSP1000 is specified for operation within the temperature range of -40°C to +85°C.

3.2 Storage Temperature

The OZDSP1000 is specified for unpowered storage within the temperature range of -40°C to +85°C.

4. Hardware Interface

4.1 Electrical Interfaces

The approximate location of the connectors and jumper blocks are illustrated in Figure 2.

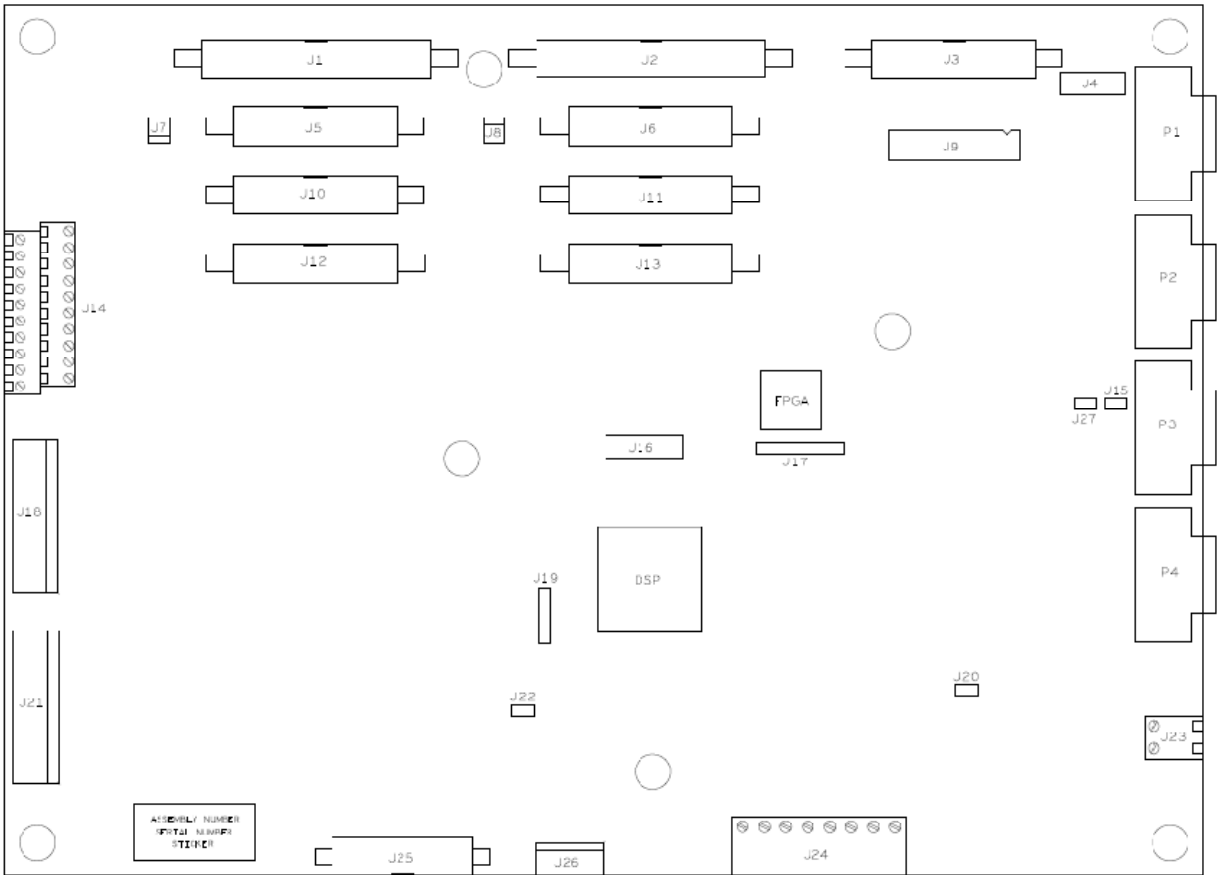


Figure 2 – Approximate Connector and Jumper Locations

Table 1 – Connector Descriptions

Connector	Description
J1	Inverter A Power Module "GD" Interface
J2	Inverter B Power Module "GD" Interface
J3	Half Bridge/Brake Module "GB" Interface
J5	Inverter A Power Module "GB" Interface: Phase U
J6	Inverter B Power Module "GB" Interface: Phase U
J7	Inverter A DC Link Sense
J8	Inverter B DC Link Sense
J9	Oztek Expansion Board Connector
J10	Inverter A Power Module "GB" Interface: Phase V
J11	Inverter B Power Module "GB" Interface: Phase V
J12	Inverter A Power Module "GB" Interface: Phase W
J13	Inverter B Power Module "GB" Interface: Phase W
J14	Isolated Digital Inputs/Outputs & Aux Analog
J16	DSP JTAG Port
J17	FPGA JTAG Port
J18	Isolated Line Voltage Sense Inputs
J21	Isolated Output Voltage Sense Inputs
J23	24V Input Power
J24	Relay Driver Outputs
J25	Encoder Interface
J26	Hall Sensor Interface
P1	RS232/RS485/RS422 Interface (RS485/422 option)
P2	RS232/RS485/RS422 Interface (RS232 option)
P3	CAN Interface
P4	RS232 Interface

Table 2 – Configuration Jumper Descriptions

Jumper	Description
J4	Serial Port Configuration Block
J15 & J27	CAN Termination Enable
J19	Boot Configuration
J20	Watchdog Disable
J22	EEPROM Write Protect Jumper

Table 3 – LED Descriptions

LED	Color	Description
D40	Green	Debug Spare 2
D42	Green	Debug Spare 1

LED	Color	Description
D34	Red	Reset
D43	Red	Inverter B Fault
D44	Red	Inverter A Fault
D45	Red	System Fault
D50	Green	24V Power Present

Table 4 – Test Hook Descriptions

Test Hook	Description
TP2	Analog Ground
TP1, TP8	Digital Ground
TP3	Isolated Ground
TP4	Debug Spare 2
TP5	Debug Spare 1
TP6	Debug DAC 2
TP7	Debug DAC 1

4.1.1 J1/2: SKiiP Power Module Interface "GD" Style

Connectors J1 and J2 provide interfaces to SKiiP "GD" style Semikron power modules. This interface complies with Semikron's required specifications. The OZDSP1000 supplies 24V power to the power module via pins 14 and 15. PWM commands (15V logic level) are supplied to the top and bottom switches of each of the three half bridges via signals INV_TOP_U(V,W) and INV_BOT_U(V,W) respectively. Feedback of phase currents, temperature, and DC link voltage are provided on INV_IOUT_U(V,W), INV_TEMP, INV_UDC signals respectively. Error signals from the module are similarly provided via INV_ERR_U(V,W) and INV_OVT. Please refer to the Semikron datasheet for the particular module being used for more information.

Table 5 – J1/2 SKiiP "GD" Power Module Pin Assignment

Pin #	Description
1	Ground
2	INV_BOT_U (Phase A)
3	INV_ERR_U (Phase A)
4	INV_TOP_U (Phase A)
5	INV_BOT_V (Phase B)
6	INV_ERR_V (Phase B)
7	INV_TOP_V (Phase B)
8	INV_BOT_W (Phase C)
9	IN_ERR_W (Phase C)
10	INV_TOP_W (Phase C)
11	INV_OVR_TEMP
12	n/c

Pin #	Description
13	INV_UDC
14	24V
15	24V
16	n/c
17	n/c
18	Ground
19	Ground
20	INV_TEMP
21	INV_IOUT_U_RTN (Phase A)
22	INV_IOUT_U (Phase A)
23	INV_IOUT_V_RTN (Phase B)
24	INV_IOUT_V (Phase B)
25	INV_IOUT_W_RTN (Phase C)
26	INV_IOUT_W (Phase C)

- **OZDSP1000 Connector Part Number:** (AMP) 499922-6
- **Mating Connector Part Number:** (AMP) 1658621-6
- **Power:** 24V @ 1.5A

4.1.2 Custom Driver Interface Considerations

When attempting to use the OZDSP1000 controller with a custom designed power stage the hardware must be designed to provide the appropriate signals expected at the J1 and/or J2 interface. Generally some sort of custom printed circuit board will be required to interface the J1/J2 signals to the gate drivers, current sensors, etc.

4.1.2.1 Power

The OZDSP1000 supplies 24V on J1/2, pins 14 & 15. This 24Vmay be used to power the electronics on the interface board. The supply is capable of providing 1.5A.

4.1.2.2 Switch Commands

The six switching commands are provided on pins 2, 4, 5, 7, 8, and 10. These switch command signals are driven off of the OZDSP1000 at 15V logic level using MC14504B level shifting devices.

4.1.2.3 Error Inputs

The OZDSP1000 expects three logic level, error inputs; one associated with each phase, on pins 3, 6, and 9. Pull-ups to 3.3V are provided on board and the signals are active high. Depending on the features provided in the custom design, these signals can be used to interface single error sources, multiple protection circuits, or none at all.

The custom interface board should drive the pin with an open-collector style circuit. In the case where no protection is provided, the pins should be grounded to disable the faults.

4.1.2.4 DC Link Voltage Sensing

The OZDSP1000 expects a signal proportional to DC link voltage to be provided on J1/2, pin 13 with respect to pin 21. This signal should be scaled such that 0-10 V represents the measurable DC link voltage range.

4.1.2.5 DC Link Hardware Over-Voltage Protection

When designing a custom interface it is highly recommended that hardware over voltage protection be implemented. This can be implemented with a comparator using the DC link voltage sense output. The output of this comparator can be used to gate off the switch commands as well as assert the Error inputs on each phase.

4.1.2.6 Hardware Over-Current and Desaturation Protection

Semikron SKiiP power modules provide fast hardware over current and desaturation protection. When designing a custom power solution, these additional protection features should also be considered. When including over current, desaturation, and over voltage protection into the design, the fault flags must be logically OR'd together and reported using the open collector Error signal inputs to the OZDSP1000.

4.1.2.7 Current Sense Signals

The OZDSP1000 expects to receive a current sense signal for each half bridge phase output. This should be a bipolar signal where +/-10V corresponds to the full scale current range. The current sense signals should be provided on the following pins:

Table 6 – J1/J2 Current Sense Pin Assignment

J1/2 Pin #	Description
22	Current Phase A (U)
21	Gnd Reference for Current Phase A (U)
24	Current Phase B (V)
23	Gnd Reference for Current Phase B (V)
26	Current Phase C (W)
25	Gnd Reference for Current Phase C (W)

4.1.2.8 Temperature Sense Signals

The OZDSP1000 expects to receive a 0-10V temperature signal on pin 20 that corresponds to the hot spot temperature of the power devices.

4.1.3 J3: SKiiP Half Bridge/ Brake Module "GB" Style Interface

Connector J3 provides an interface to SKiiP "GB" style Semikron half bridge and brake modules. This interface complies with Semikron's required specifications. The OZDSP1000 supplies 24V power to the power module via pins 6 and 7. PWM commands or brake enable/disable commands (15V logic level) are supplied to the top and bottom switches HB_TOP and HB_BOT

respectively. Feedback of current and temperature are provided on HB_IOUT and HB_TEMP. Error signals from the module are similarly provided via HB_ERR and HB_OVT. Please refer to the Semikron datasheet for the particular module being used for more information.

Table 7 – J3 Half Bridge Pin Assignment

Pin #	Description
1	Ground
2	Bottom Switch Command
3	Error
4	Top Switch Command
5	Over Temp
6	24V
7	24V
8	No connect
9	No connect
10	Ground
11	Ground
12	Analog Temperature
13	Analog Current Return
14	Analog Current

- **OZDSP1000 Connector Part Number:** (AMP) 499922-2
- **Mating Connector Part Number:** (AMP) 1658621-2
- **Power:** 24V @ 1.5A

4.1.4 J5/6/10/11/12/13: SKiiP Power Module Interface Alternate "GB" Style

Connectors J5/10/12 and J6/11/13 provide an alternate inverter interface to SKiiP "GB" style Semikron half bridge modules. This particular interface is useful for higher powered applications when it is desirable to parallel multiple half bridges. The OZDSP1000 supplies 24V power to the power module via pins 6 and 7. PWM commands (15V logic level) are supplied to the top and bottom switches INVA(B)_TOP_U(V,W) and INVA(B)_BOT_U(V,W) respectively. Feedback of current and temperature are provided on INVA(B)_IOUT_U(V,W) and INVA(B)_TEMP_U(V,W). Error signals from the module are similarly provided via INVA(B)_ERR_U(V,W) and INVA(B)_OVT_U(V,W). Please refer to the Semikron datasheet for the particular module being used for more information.

Table 8 – J5/6/10/11/12/13 Alternate "GB" Style SKiiP Pin Assignment

Pin #	Description
1	Ground
2	Bottom Switch Command
3	Error
4	Top Switch Command
5	Over Temp
6	24V
7	24V
8	No connect
9	No connect
10	Ground
11	Ground
12	Analog Temperature
13	Analog Current Return
14	Analog Current

- **OZDSP1000 Connector Part Number:** (AMP) 499922-2
- **Mating Connector Part Number:** (AMP) 1658621-2
- **Power:** 24V @ 1.5A

4.1.5 J7/J8: DC Link Sense

Connectors J7 and J8 provide interfaces to low voltage DC Link measurements when using the "GB" style SKiiP power module interfaces.

Table 9 – J7/8 DC Link Voltage Pin Assignment

Pin #	Description
1	DC Link Voltage
2	Signal Return

- **OZDSP1000 Connector Part Number:** (AMP) 640456-2
- **Mating Connector Part Number:** (AMP) 1375820-2
- **Input Range:** (see Section 5.1 for ADC scaling details)

4.1.6 J9: Oztek Expansion Board Connector

Connector J9 allows an Oztek or user designed Expansion Board to be connected to the OZDSP1000.

Table 10 – J9 Expansion Interface Pin Assignment

Pin #	Description
1	15V
2	15V
3	n/c
4	5V
5	5V
6	n/c
7	3.3V
8	3.3V
9	n/c
10	SPI_CLK_DB
11	Ground
12	SPI SIMO
13	Ground
14	SPI SOMI
15	Ground
16	SPI_DB_CSn
17	Ground
18	IRQ_USERn
19	Ground
20	DBIO1
21	Ground
22	DBIO2
23	Ground
24	DB_SPARE1
25	Ground
26	DB_SPARE2
27	Ground
28	DB_SPARE3
29	Ground
30	DB_SPARE4
31	Ground
32	DB_CLK

- **OZDSP1000 Connector Part Number:** (Hirose) FX2-32P-1.27SV(71)
- **Mating Connector Part Number:** (Hirose) FX2-32S-1.27SV(71)

4.1.7 J14: Isolated Digital Inputs, Outputs, and Auxiliary Analog

Connector J14 provides an interface to the four opto-isolated, digital inputs, outputs, as well as the two auxiliary analog inputs.

Table 11 – J14 Isolated Digital Inputs, Outputs, and Auxiliary Analog Pin Assignment

Pin #	Description
1	Aux Analog Input 1
2	Aux Analog 1 Return
3	Isolated Output 4 Emitter
4	Isolated Output 4 Collector
5	Isolated Output 2 Emitter
6	Isolated Output 2 Collector
7	Isolated Input 2
8	Isolated Input 2 Return
9	Isolated Input 4
10	Isolated Input 4 Return
11	Aux Analog Input 1
12	Aux Analog 2 Return
13	Isolated Output 3 Emitter
14	Isolated Output 3 Collector
15	Isolated Output 1 Emitter
16	Isolated Output 1 Collector
17	Isolated Input 1
18	Isolated Input 1 Return
19	Isolated Input 3
20	Isolated Input 3 Return

- **OZDSP1000 Connector Part Number:** Terminal Block
- **Mating Connector Part Number:** n/a
- **Digital Input Range:** Logic high: 0V or floating. Logic low: 3V – 25V
- **Digital Output Range:** Optocoupler Output V_{CEO} = 80V
- **Analog Input Range:** 0V – 10V

4.1.8 J16: DSP JTAG Port

Connector J16 is the DSP JTAG programming port for the board. Pin 6 is cut to avoid the emulator pod being incorrectly connected. Emulator pods used to program the DSP are available through Spectrum Digital and Signum Systems. Figure 3 provides the physical and electrical pinout of the connector.

- **OZDSP1000 Connector Part:** Double row 0.1" vertical pin header, 2x7

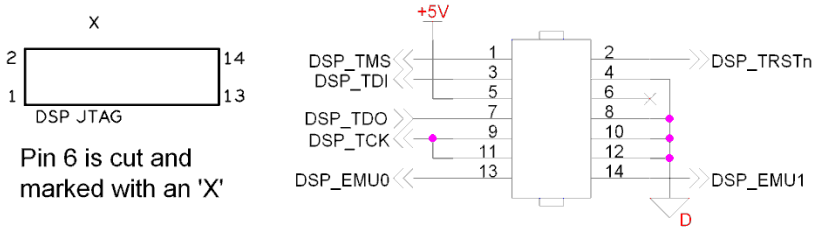


Figure 3 – J16: DSP JTAG Port Pinout

4.1.9 J17: FPGA JTAG Port

Connector J17 is the FPGA JTAG programming port. The OZDSP1000 comes preprogrammed with the latest firmware for the FPGA. Pin 5 is cut to avoid incorrectly connecting the FPGA programming cable. Figure 4 provides the physical and electrical pinout of the connector.

- **OZDSP1000 Connector Part:** Single row 0.1" vertical pin header, 1x8

Figure 4 – J17: FPGA JTAG Port Pinout

4.1.10 J18/J21: High Voltage Line and Output Feedback

J18 and J21 provide an interface to sense three phase AC line voltages. The standard hardware variant is designed to accept 480VAC voltages directly. Interfacing to other AC voltages may require a modification to the gain of the sense amplifier (consult Oztek for more information).

Table 12 – J18/J21 High Voltage Line and Output Feedback Pin Assignment

Pin #	Description
1	Line/Output Voltage Phase A
5	Line/Output Voltage Phase B
9	Line/Output Voltage Phase C

- **OZDSP1000 Connector Part Number:** (Waldom/Molex) 26-60-4090
- **Mating Connector Part Number:** (Waldom/Molex) 26-03-4090

4.1.11 J23: Bias Power Input

The OZDSP1000 requires 24VDC power input on terminal block J23.

Table 13 – J23 RS-485 Pin Assignment

Pin #	Description
1	24 VDC
2	24V Return

- **OZDSP1000 Connector Part Number:** Terminal Block
- **Mating Connector Part Number:** n/a (terminal block style)
- **Voltage:** 24V nominal, 18V min, 28V max
- **Current:** 4.5A maximum (Inrush current while powering three SKiiP modules)

4.1.12 J24: Relay Driver Interface

Connector J24 provides an interface to the four relay driver outputs.

Table 14 – J24 Relay Drive Pin Assignment

Pin #	Description
1	Relay Drive 3
2	Ground
3	Relay Drive 2
4	Ground
5	Relay Drive 1
6	Ground
7	Relay Drive 0
8	Ground

- **OZDSP1000 Connector Part Number:** Terminal Block
- **Mating Connector Part Number:** n/a
- **Output Range:** 24V, 2A continuous, 5A inrush

Please note that when using the relay driver with one or more unused drivers one of the following schemes must be used to deal with the open-load fault detection in the driver IC:

1. Since the open-load faults are only reported once per state, initialize all relays to 'off' twice: once to set them to 'off' and obtain the faults, and the second time to clear the faults. Then open-load faults will only be reported when the state is changed of a specific relay driver, so as long as the unused relays drivers are left 'off', no new faults will be reported.

2. Since the open-load faults are only reported in a low state, initialize the unused drivers to 'on', and subsequently leave them on. Please note that the unused driver pins will be at a 24V state.
3. Terminate the unused relay drivers with a 5kΩ – 20kΩ 1/8 watt resistor.

4.1.13 J25: Incremental Encoder Interface

Connector J25 provides an interface to an incremental, quadrature encoder. The interface provides for the A and B quadrature signals as well as an index input. 5V power and ground are also provided on the connector to power the encoder.

Table 15 – J25 Encoder Interface Pin Assignment

Pin #	Description
1	No connect
2	5V
3	No Connect
4	B Signal - Positive
5	A Signal - Negative
6	A Signal - Positve
7	B Signal - Negative
8	B Signal - Positve
9	Index - Negative
10	Index - Positve

- **OZDSP1000 Connector Part Number:** (Tyco) 2x5 Shrouded Header: 499910-1
- **Mating Connector Part Number:** (Tyco) 2x5 IDC: 1658622-1
- **Power:** 5V, 300mA
- **Differential termination:** 100Ω
- **Electrical Interface:** Differential inputs. Logic high: $V_{ID} \geq 0.2V$. Logic low: $V_{ID} \leq -0.2V$
- **Max Rating:** Input voltage: ±14V. Differential voltage: ±14V

4.1.14 J26: Hall Effect Sensor Interface

Connector J26 provides an interface for three Hall Effect position sensors. Both 5V and 15V power options are available to power the sensors. Table 16 provides the physical and electrical pinout of the connector.

Table 16 – J26 Hall Sensor Pin Assignment

Pin #	Description
1	+5V
2	+15V

Pin #	Description
3	Ground
4	Hall 1 Input
5	Hall 2 Input
6	Hall 3 Input

- **OZDSP1000 Connector Part Number:** (Molex) 6 Header: 22-23-2061
- **Mating Connector Part Number:** (Molex) 6 Receptacle with Ramp: 22-01-2067
- **Power:** 5V @300mA, 15V @300mA
- **Electrical Interface (HALL1,2,3):** 4.75kΩ pull up to 15V. Use with an open collector output that can sink at least 3mA.
- **Input Behavior:** When Hall is enabled and sinking current, HALL input is in low state, while corresponding DSP pin HALLn is in a high state.

4.1.15 P1/P2: Selectable Serial Interface

Connector P1 and P2 provide a configurable, serial communications interface. Depending on the J4 jumper settings this port may be configured one of two ways: RS232 mode, or RS422/485 mode. When in RS422/485 mode, connector P1 is used to access the port. When in RS232 mode, connector P2 is used to access the port.

- **OZDSP1000 Connector Part Number:** (AMP) 747844-5
- **Mating Connector Part Number:** Industry Standard DB9 Male

Table 17 – J4 RS232/RS422/485 Configuration Jumper Settings

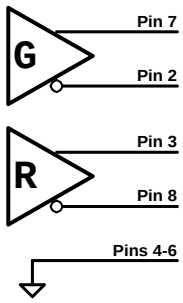
	Jumper Pins					
Mode	1-2	3-4	5-6	7-8	9-10	11-12
RS232	Install	DNP	DNP	DNP	DNP	DNP
RS485 2-wire	DNP	Install	Install	Install	Optional A-B Terminator	DNP
RS485 4-wire	DNP	Install	Install	Install	Optional A-B Terminator	Optional Y-Z Terminator
RS422	DNP	Install	DNP	DNP	Optional A-B Terminator	Optional Y-Z Terminator

4.1.15.1 RS232 Configuration

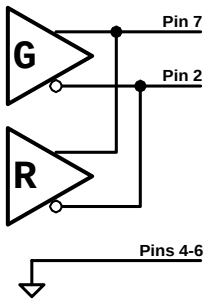
Table 18 – P2 RS232 Pin Assignment

Pin #	Description
2	Tx
3	Rx
5	Ground

4.1.15.2 RS422/485 Configuration



RS422 and RS485 Four-Wire



RS485 Two-Wire

Figure 5 – P1/P2: Selectable Serial Interface Pin Assignment - RS422/485 Configuration

4.1.16 P3: CAN Bus Interface

Connector P3 provides a CAN Bus communications interface. The interface is a shielded, female, DB9 style connector.

Table 19 – P3 CAN Bus Pin Assignment

Pin #	Description
2	CAN Low
3	CAN Ground
7	CAN High

- **OZDSP1000 Connector Part Number:** (AMP) 747844-5
- **Mating Connector Part Number:** Industry Standard DB9 Male

4.1.16.1 J15/27 CAN Termination Jumpers

Jumper blocks J15 and J27 provide a means to terminate the CAN bus lines CAN high (CANH) and CAN low (CANL). Note that termination should only be placed at the end terminals of the CAN communication network, reference Figure 6.

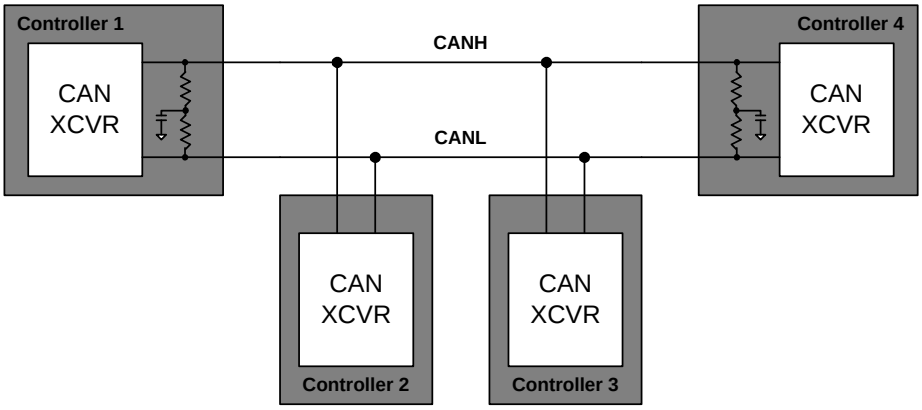


Figure 6 – Multi-Node CAN Network Configuration

Standard 0.1" jumpers should be installed on both J15 and J27 to enable the termination. With no jumpers installed, the lines remain un-terminated. Refer to Figure 7 for the applicable interface circuit.

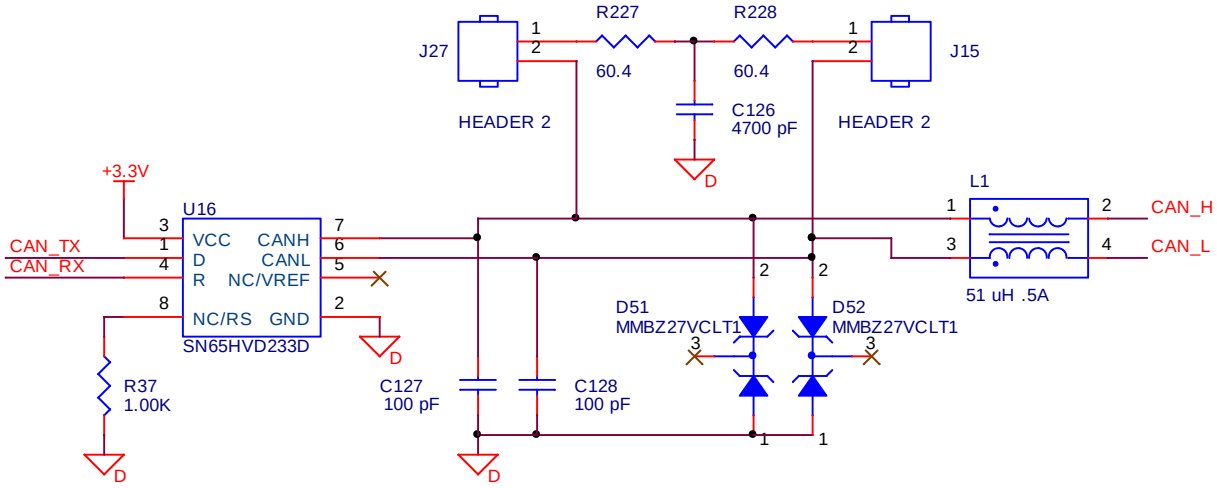


Figure 7 – CAN Interface Circuit

4.2 Mechanical Interface

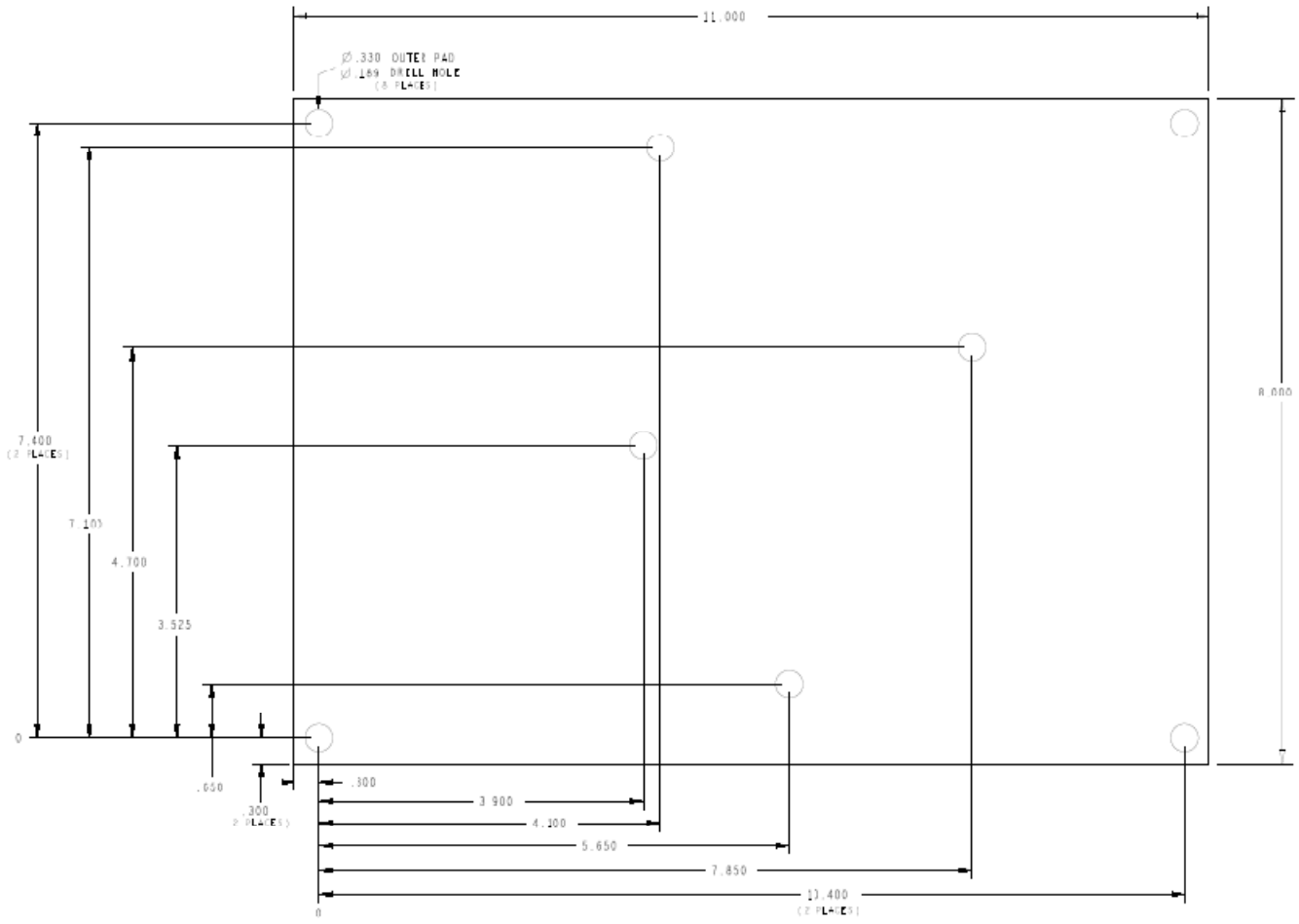


Figure 8 – OZDSP1000 Mechanical Dimensions

5. Analog to Digital Interfaces

5.1 DSP ADC Interface

The TMS320F2812 provides for 16 channels of A/D conversion. In order to increase the number of A/D inputs, the OZDSP1000 uses a multiplexer to switch between different inputs on the slower moving A/D channels. The three Inverter A SKiiP power module temperature sense inputs, along with the 5V bias voltage monitor are multiplexed into channel A4. The three Inverter B SKiiP power module temperature sense inputs, along with the 3.3V bias voltage monitor are multiplexed into channel B4. Figure 9 illustrates this multiplexing scheme. Note that these MUX control lines are sourced by the FPGA device.

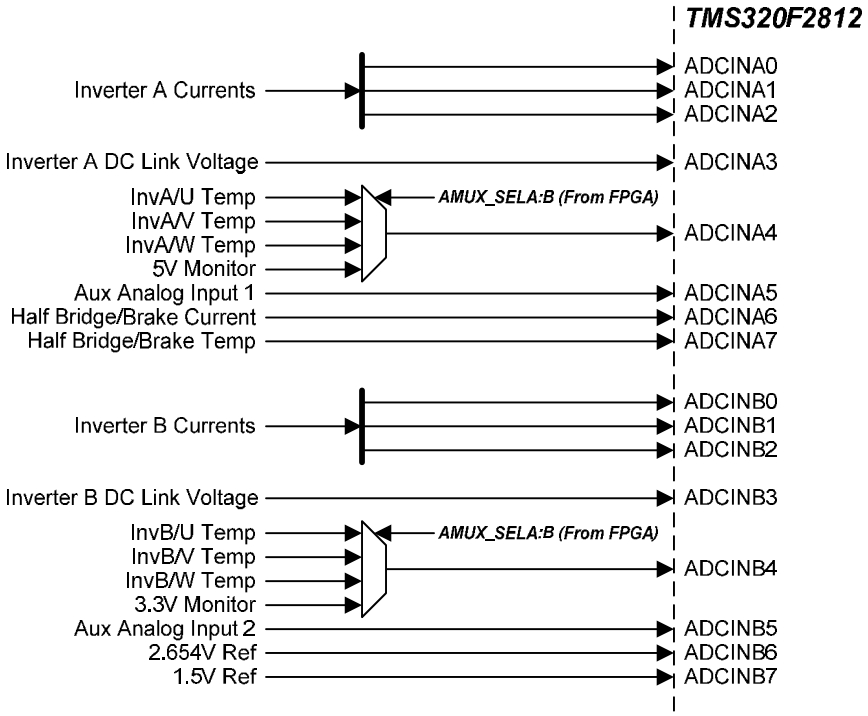


Figure 9 – A/D Multiplexed Interface Block Diagram

Many of the ADC inputs are filtered with a single-pole low-pass filter. Table 20 provides detailed information on the A/D Channel signal assignments, scaling and offset, and the filter cutoff frequency for the direct inputs.

Table 21 provides the detailed information on the analog multiplexer scaling. Refer to the Semikron datasheet as to the specific device scaling for the I_{SENSE}, $V_{SENSE-UDC,}$ and V_{TEMP} measurements.

Table 20 – DSP A/D Channel Assignment and Scaling

DSP			Source	Test Pt	Scaling and Offset	Cutoff Frequency
Pin Name	Pin #	Signal Name				
ADCINA0	174	$I_{SENSE-AU}$	J1 pin 22 *(J5 pin 14)*	XTP4	$V_{adc} = -0.15*V_{in} + 1.5V$	100 kHz
ADCINA1	173	$I_{SENSE-AV}$	J1 pin 24 *(J10 pin 14)*	XTP2	$V_{adc} = -0.15*V_{in} + 1.5V$	100 kHz
ADCINA2	172	$I_{SENSE-AW}$	J1 pin 26 *(J12 pin 14)*	XTP5	$V_{adc} = -0.15*V_{in} + 1.5V$	100 kHz
ADCINA3	171	$V_{SENSE-UDC-A}$	J1 pin 13 *(J7 Pin1)*	XTP10	$V_{adc} = 0.297*V_{in}$	160 Hz
ADCINA4	170	MUX-A	Multiplexor	-	-	-
ADCINA5	169	V_{AUX-A1}	J14 pin1	-	$V_{adc} = 0.30168*V_{in}$	53 kHz

ADCINA6	168	$I_{SENSE-HB}$	J3 pin 14	XTP12	$V_{adc} = -0.15*V_{in} + 1.5V$	100 kHz
ADCINA7	167	$Temp_{SENSE-HB}$	J3 pin 12	-	$V_{adc} = 0.302*V_{in}$	527 Hz
DSP			Source	Test Pt	Scaling and Offset	Cutoff Frequency
Pin Name	Pin #	Signal Name				
ADCINB0	2	$I_{SENSE-BU}$	J2 pin 22 *(J6 pin 14)*	XTP11	$V_{adc} = -0.15*V_{in} + 1.5V$	100 kHz
ADCINB1	3	$I_{SENSE-BV}$	J2 pin 24 *(J11 pin 14)*	XTP7	$V_{adc} = -0.15*V_{in} + 1.5V$	100 kHz
ADCINB2	4	$I_{SENSE-BW}$	J2 pin 26 *(J13 pin 14)*	XTP3	$V_{adc} = -0.15*V_{in} + 1.5V$	100 kHz
ADCINB3	5	$V_{SENSE-UDC-B}$	J2 pin 13 *(J8 Pin1)*	XTP9	$V_{adc} = 0.297*V_{in}$	160 Hz
ADCINB4	6	MUX-B	Multiplexor	-	-	-
ADCINB5	7	V_{AUX-A2}	J14 pin11	-	$V_{adc} = 0.30168*V_{in}$	53 kHz
ADCINB6	8	$V_{REF-2.564V}$	Internal	XTP13	$V_{adc} = V_{in}$	n/a
ADCINB7	9	$V_{REF-1.5V}$	Internal	XTP14	$V_{adc} = V_{in}$	n/a

Table 21 – Analog Multiplexer Channel Assignment and Scaling

Analog MUX U14			Source	Scaling and Offset
Pin Name	Pin #	Signal Name		
1Y0	12	$V_{TEMP-INVA-U}$	J1 pin 20 *(J5 pin12)*	$V_{adc} = 0.30168*V_{in}$
1Y1	14	$V_{TEMP-INVA-V}$	J10 pin12	$V_{adc} = 0.30168*V_{in}$
1Y2	15	$V_{TEMP-INVA-W}$	J12 pin 12	$V_{adc} = 0.30168*V_{in}$
1Y3	11	$V_{SENSE-5V}$	Supply	$V_{adc} = 0.48213*V_{in}$
2Y0	1	$V_{TEMP-INVB-U}$	J2 pin 20 *(J6 pin12)*	$V_{adc} = 0.30168*V_{in}$
2Y1	5	$V_{TEMP-INVB-V}$	J11 pin12	$V_{adc} = 0.30168*V_{in}$
2Y2	2	$V_{TEMP-INVB-W}$	J13 pin 12	$V_{adc} = 0.30168*V_{in}$
2Y3	4	$V_{SENSE-3.3V}$	Supply	$V_{adc} = 0.72752*V_{in}$

5.2 HVADC Interface

The OZDSP1000 also has the capability to measure four differential high voltage channels with 12 bits of accuracy. This is done with an isolated ADC that is automatically controlled serially through the FPGA. Conversions are initiated by setting the ADC_TRIGGER (pin 116 of the DSP) high and then low. When the process is done, an ADC interrupt request line is triggered on the DSP (pin 150) to indicate that the converted data is available for reading. The ADC converts the 0-5V input signal to the 12-bit number according to the table below.

Table 22 – HVADC Conversion Scaling

Description	Input Voltage	Binary Code	Hexadecimal Code
Positive full-scale	5V	0111 1111 1111	7FF
Mid-scale	2.5V	0000 0000 0000	000
Mid-scale – 1LSB	4.29878V	1111 1111 1111	FFF
Negative full-scale	0V	1000 0000 0000	800

For debugging purposes, there are test points on all four differential voltages connected to the ADC.

Table 23 – HVADC Test Point Locations

Description	Location
$Vline_{AB}$	XTP24
$Vline_{BC}$	XTP21
$Vout_{AB}$	XTP22
$Vout_{BC}$	XTP31

Warranty and Product Information

Limited Warranty

What does this warranty cover and how long does it last? This Limited Warranty is provided by Oztek Corp. ("Oztek") and covers defects in workmanship and materials in your OZDSP1000 controller. This Warranty Period lasts for 18 months from the date of purchase at the point of sale to you, the original end user customer, unless otherwise agreed in writing. You will be required to demonstrate proof of purchase to make warranty claims. This Limited Warranty is transferable to subsequent owners but only for the unexpired portion of the Warranty Period. Subsequent owners also require original proof of purchase as described in "What proof of purchase is required?"

What will Oztek do? During the Warranty Period Oztek will, at its option, repair the product (if economically feasible) or replace the defective product free of charge, provided that you notify Oztek of the product defect within the Warranty Period, and provided that through inspection Oztek establishes the existence of such a defect and that it is covered by this Limited Warranty.

Oztek will, at its option, use new and/or reconditioned parts in performing warranty repair and building replacement products. Oztek reserves the right to use parts or products of original or improved design in the repair or replacement. If Oztek repairs or replaces a product, its warranty continues for the remaining portion of the original Warranty Period or 90 days from the date of the return shipment to the customer, whichever is greater. All replaced products and all parts removed from repaired products become the property of Oztek.

Oztek covers both parts and labor necessary to repair the product, and return shipment to the customer via an Oztek-selected non-expedited surface freight within the contiguous United States and Canada. Alaska, Hawaii and locations outside of the United States and Canada are excluded. Contact Oztek Customer Service for details on freight policy for return shipments from excluded areas.

How do you get service? If your product requires troubleshooting or warranty service, contact your merchant. If you are unable to contact your merchant, or the merchant is unable to provide service, contact Oztek directly at:

USA
Telephone: 603-546-0090
Fax: 603-386-6366
Email techsupport@oztekcorp.com

Direct returns may be performed according to the Oztek Return Material Authorization Policy described in your product manual.

What proof of purchase is required? In any warranty claim, dated proof of purchase must accompany the product and the product must not have been disassembled or modified without prior written authorization by Oztek. Proof of purchase may be in any one of the following forms:

- The dated purchase receipt from the original purchase of the product at point of sale to the end user
- The dated dealer invoice or purchase receipt showing original equipment manufacturer (OEM) status
- The dated invoice or purchase receipt showing the product exchanged under warranty

What does this warranty not cover? Claims are limited to repair and replacement, or if in Oztek's discretion that is not possible, reimbursement up to the purchase price paid for the product. Oztek will be liable to you only for direct damages suffered by you and only up to a maximum amount equal to the purchase price of the product. This Limited Warranty does not warrant uninterrupted or error-free operation of the product or cover normal wear and tear of the product or costs related to the removal, installation, or troubleshooting of the customer's electrical systems. This warranty does not apply to and Oztek will not be responsible for any defect in or damage to:

a) The product if it has been misused, neglected, improperly installed, physically damaged or altered, either internally or externally, or damaged from improper use or use in an unsuitable environment
b) The product if it has been subjected to fire, water, generalized corrosion, biological infestations, or input voltage that creates operating conditions beyond the maximum or minimum limits listed in the Oztek product specifications including high input voltage from generators and lightning strikes
c) The product if repairs have been done to it other than by Oztek or its authorized service centers (hereafter "ASCs")
d) The product if it is used as a component part of a product expressly warranted by another manufacturer
e) The product if its original identification (trade-mark, serial number) markings have been defaced, altered, or removed
f) The product if it is located outside of the country where it was purchased
g) Any consequential losses that are attributable to the product losing power whether by product malfunction, installation error or misuse.

Disclaimer

Product

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Return Material Authorization Policy

Before returning a product directly to Oztek you must obtain a Return Material Authorization (RMA) number and the correct factory "Ship To" address. Products must also be shipped prepaid. Product shipments will be refused and returned at your expense if they are unauthorized, returned without an RMA number clearly marked on the outside of the shipping box, if they are shipped collect, or if they are shipped to the wrong location.
When you contact Oztek to obtain service, please have your instruction manual ready for reference and be prepared to supply:

- The serial number of your product
- Information about the installation and use of the unit
- Information about the failure and/or reason for the return
- A copy of your dated proof of purchase

Return Procedure

Package the unit safely, preferably using the original box and packing materials. Please ensure that your product is shipped fully insured in the original packaging or equivalent. This warranty will not apply where the product is damaged due to improper packaging. Include the following:

- The RMA number supplied by Oztek clearly marked on the outside of the box.
- A return address where the unit can be shipped. Post office boxes are not acceptable.
- A contact telephone number where you can be reached during work hours.
- A brief description of the problem.

Ship the unit prepaid to the address provided by your Oztek customer service representative.

If you are returning a product from outside of the USA or Canada - In addition to the above, you MUST include return freight funds and you are fully responsible for all documents, duties, tariffs, and deposits.

Out of Warranty Service

If the warranty period for your product has expired, if the unit was damaged by misuse or incorrect installation, if other conditions of the warranty have not been met, or if no dated proof of purchase is available, your unit may be serviced or replaced for a flat fee. If a unit cannot be serviced due to damage beyond salvation or because the repair is not economically feasible, a labor fee may still be incurred for the time spent making this determination.

To return your product for out of warranty service, contact Oztek Customer Service for a Return Material Authorization (RMA) number and follow the other steps outlined in "Return Procedure".

Payment options such as credit card or money order will be explained by the Customer Service Representative. In cases where the minimum flat fee does not apply, as with incomplete units or units with excessive damage, an additional fee will be charged. If applicable, you will be contacted by Customer Service once your unit has been received.