EE 421/621 Digital IC Design

12/1/2021

Lecture 27

Final for EE 421 Digital Electronics and ECG 621 Digital Integrated Circuit Design
Fall, University of Nevada, Las Vegas

NAME:_____

Show your work to get credit. Open book and closed notes.

Unless otherwise indicated use the following SPICE parameters for hand calculations with ***VDD* = 5 V**. Also, use R'n = 20k, R'p = 40k, and C'ox = 2.5 fF/um^2.

Note that by the book's definition the threshold voltage for the PMOS device is positive (so from the data below V_{THP} = 0.9 V using the book's labeling and equations).

```
.MODEL NMOS NMOS LEVEL   = 3
+ TOX     = 150E-10          NSUB    = 1E17          GAMMA   = 0.5
+ PHI     = 0.7              VTO     = 0.8           DELTA   = 3.0
+ UO      = 650              ETA     = 3.0E-6        THETA   = 0.1
+ KP      = 100E-6           VMAX    = 1E5           KAPPA   = 0.3
+ RSH     = 0                NFS     = 1E12          TPG     = 1
+ XJ      = 500E-9           LD      = 100E-9
+ CGDO    = 200E-12          CGSO    = 200E-12       CGBO    = 1E-10
+ CJ      = 400E-6           PB      = 1             MJ      = 0.5
+ CJSW    = 300E-12          MJSW    = 0.5
*
.MODEL PMOS PMOS LEVEL   = 3
+ TOX     = 150E-10          NSUB    = 1E17          GAMMA   = 0.6
+ PHI     = 0.7              VTO     = -0.9          DELTA   = 0.1
+ UO      = 250              ETA     = 0             THETA   = 0.1
+ KP      = 50E-6            VMAX    = 5E4           KAPPA   = 1
+ RSH     = 0                NFS     = 1E12          TPG     = -1
+ XJ      = 500E-9           LD      = 100E-9
+ CGDO    = 200E-12          CGSO    = 200E-12       CGBO    = 1E-10
+ CJ      = 400E-6           PB      = 1             MJ      = 0.5
+ CJSW    = 300E-12          MJSW    = 0.5
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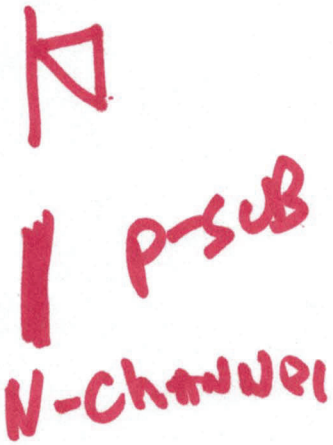

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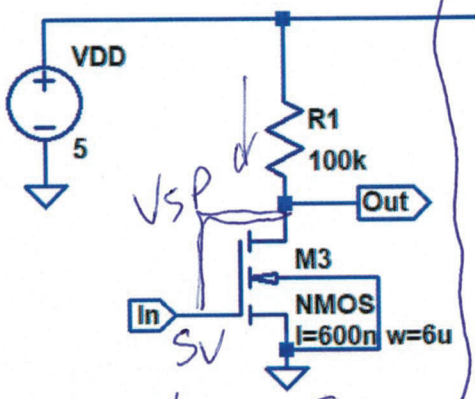
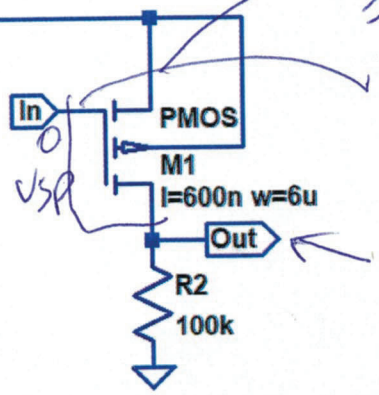
$V_{GS} \geq V_{GS} - V_{tHN}$

$0 \geq -V_{tHN}$ yes

1. Estimate the switching point voltage, V_{SP}, output low voltage, V_{OL}, and output high voltage, V_{OH}, for the following inverters using the square-law equations. Note that your answers are all numbers (not symbolic). Please place a box around each of your 6 answers. (10 points)





source = VDD

$= V_{SB}$

$V_G = V_{SP}$

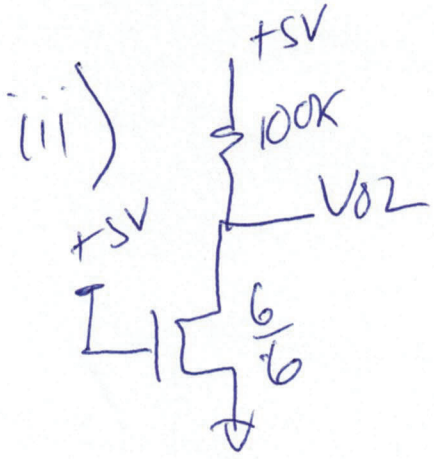
i) $V_{OH} = 5V$

ii) $\frac{5 - V_{SP}}{100K} = \frac{100\mu}{2} \cdot \frac{6}{.6}(V_{SP} - .8)^2$

i) $V_{OL} = 0$

ii) $\frac{V_{SP}}{100K} = \frac{50\mu}{2} \cdot \frac{6}{.6} \cdot (VDD - V_{SP} - .9)^2$

iii)



$\frac{5 - V_{OL}}{100K} = 100\mu \cdot \frac{6}{.6}\left((5 - .8)V_{OL}\right)$

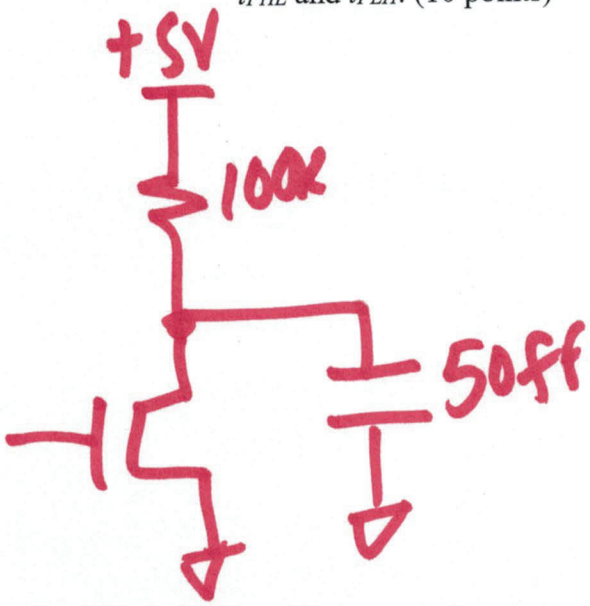
$V_{OL} = ?$

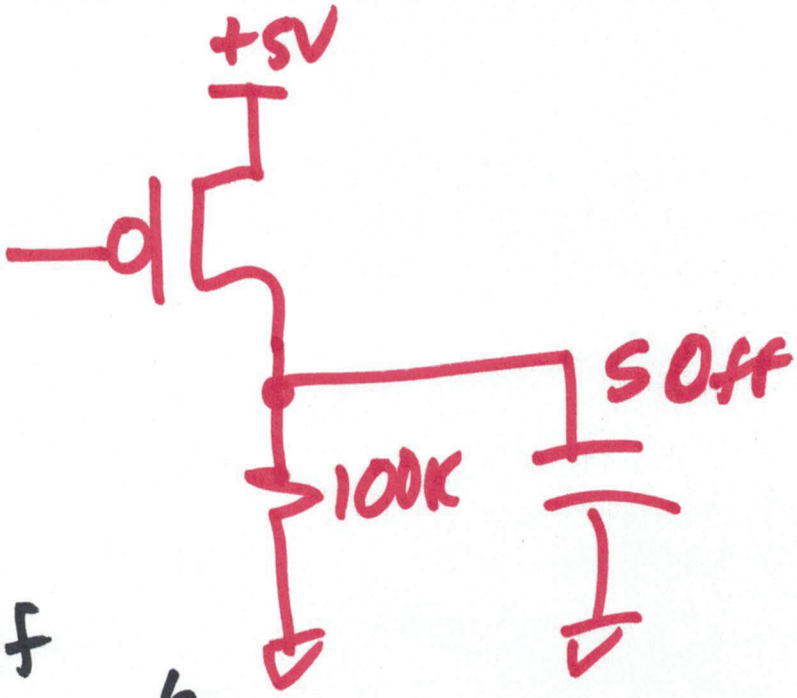
$\frac{V_{OH}}{100K} = 50\mu \cdot \frac{6}{.6}\left((VDD - 0 - .9)V_{OH}\right)$

$V_{OH} = ?$

3

2. Suppose the inverters in problem 1 are connected to a 50 fF load. Estimate both t_{PHL} and t_{PLH}. (10 points)





$t_{pLH} = 0.7 \cdot 100K \cdot 50f$

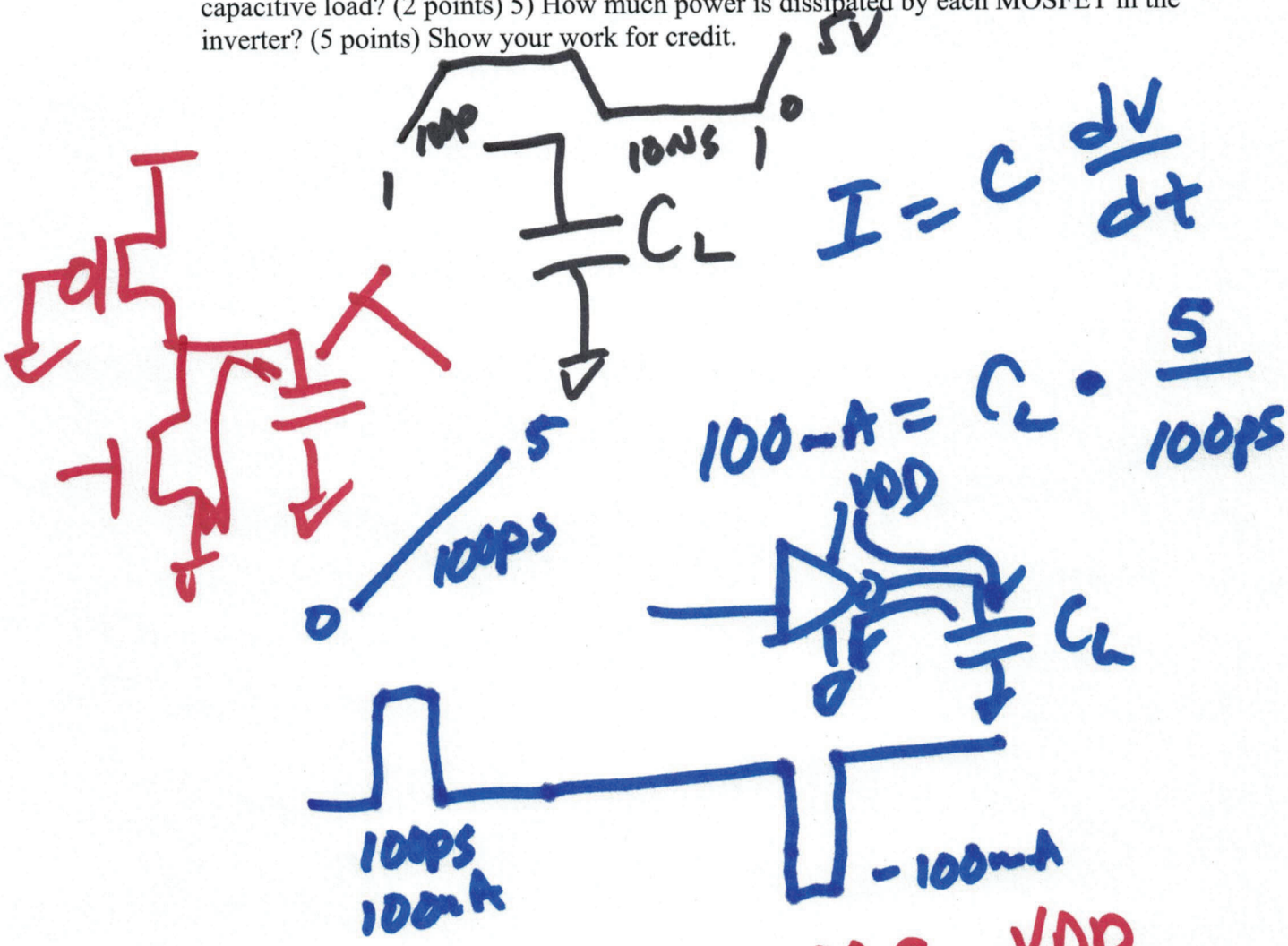
$t_{pHL} = 0.7 \cdot 50ff \cdot 20k \cdot \frac{.6}{6}$

$t_{pHL} = 0.7 \cdot 100K \cdot 50ff$

$t_{pLH} = 0.7 \cdot 50ff \cdot .48K \cdot \frac{.6}{6}$

4)

3. Suppose an inverter drives a capacitive load from 0 to 5 V at a maximum frequency of 100 MHz with 100 ps edge transitions. If the peak amount of current pulled by the circuit is 100 mA: 1) what is the value of the capacitive load? (2 points) 2) What is the average power consumed by the circuit? (4 points) 3) How much power is delivered to the capacitive load? (2 points) 4) What is the peak energy stored by the capacitive load? (2 points) 5) How much power is dissipated by each MOSFET in the inverter? (5 points) Show your work for credit.



$I = C \frac{dV}{dt}$

$100\text{-}A = C_L \cdot \frac{5}{100ps}$

$CV = Q$

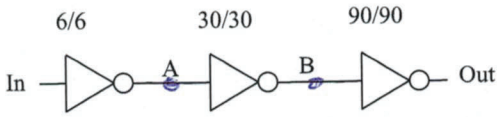
$I_{AVG} = \frac{C_L \cdot VDD}{10\,NS}$

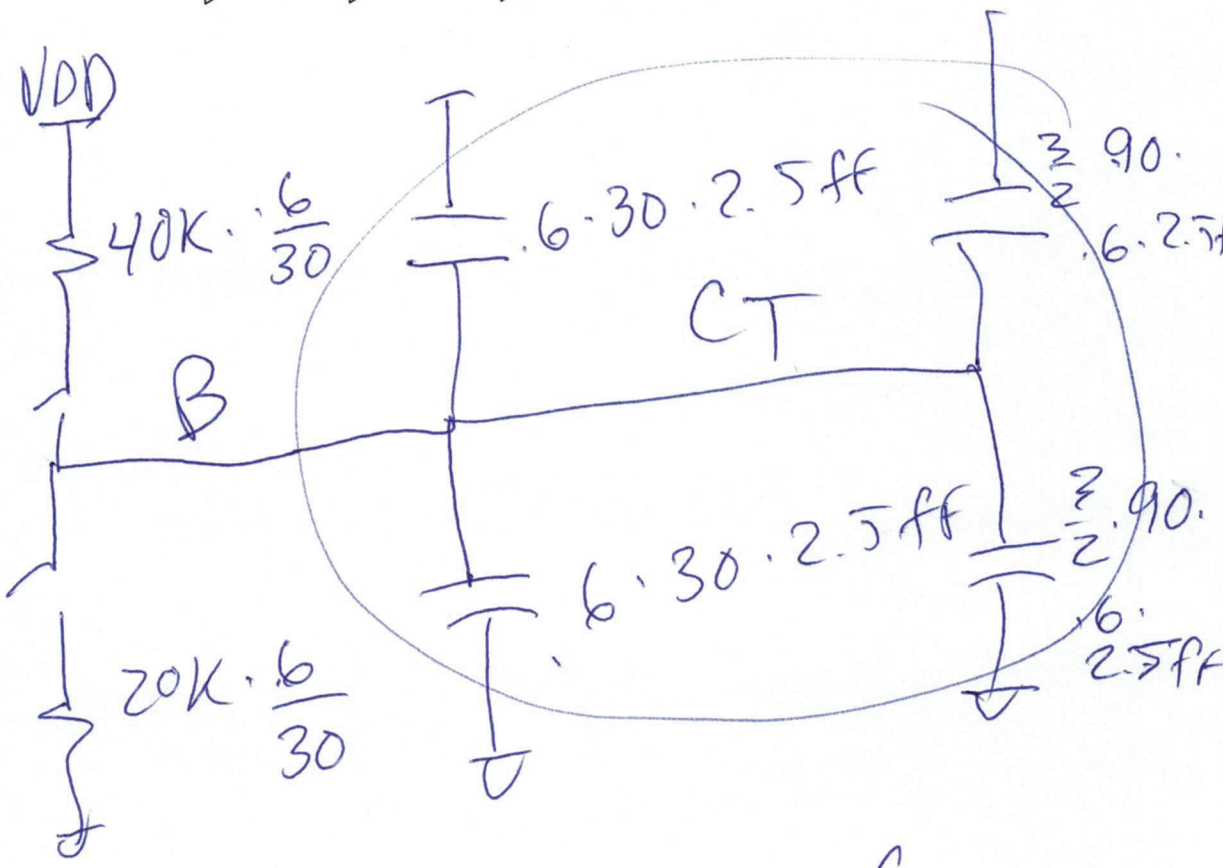
$P_{AVG} = I_{AVG} \cdot VDD$

$\mathcal{E} = \frac{1}{2} C_L V_{DD}^2$

5)

4. Estimate the delays, t_{PHL} and t_{PLH}, from point A to B in the following circuit. All MOSFETs have lengths of 600 nm. Widths of the PMOS and NMOS in each inverter are equal as shown in the figure below. Show your work and place your answers in boxes. (10 points)



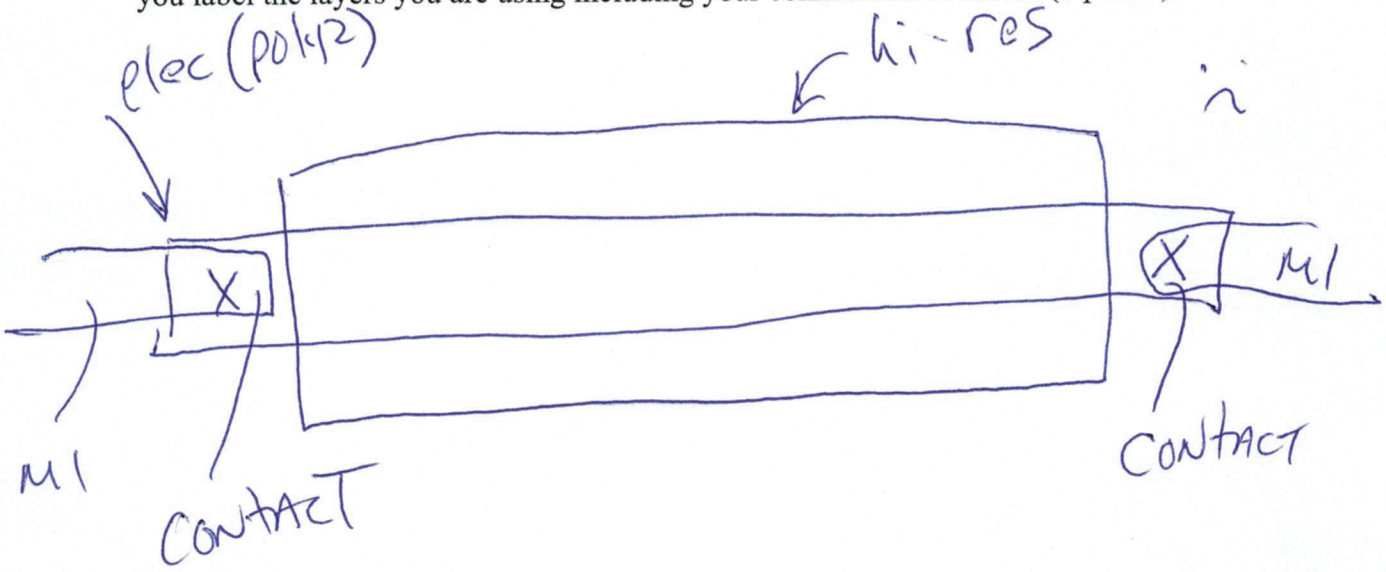


$t_{PLH} = 0.7 \cdot 40K \cdot \frac{6}{30} \cdot C_T$

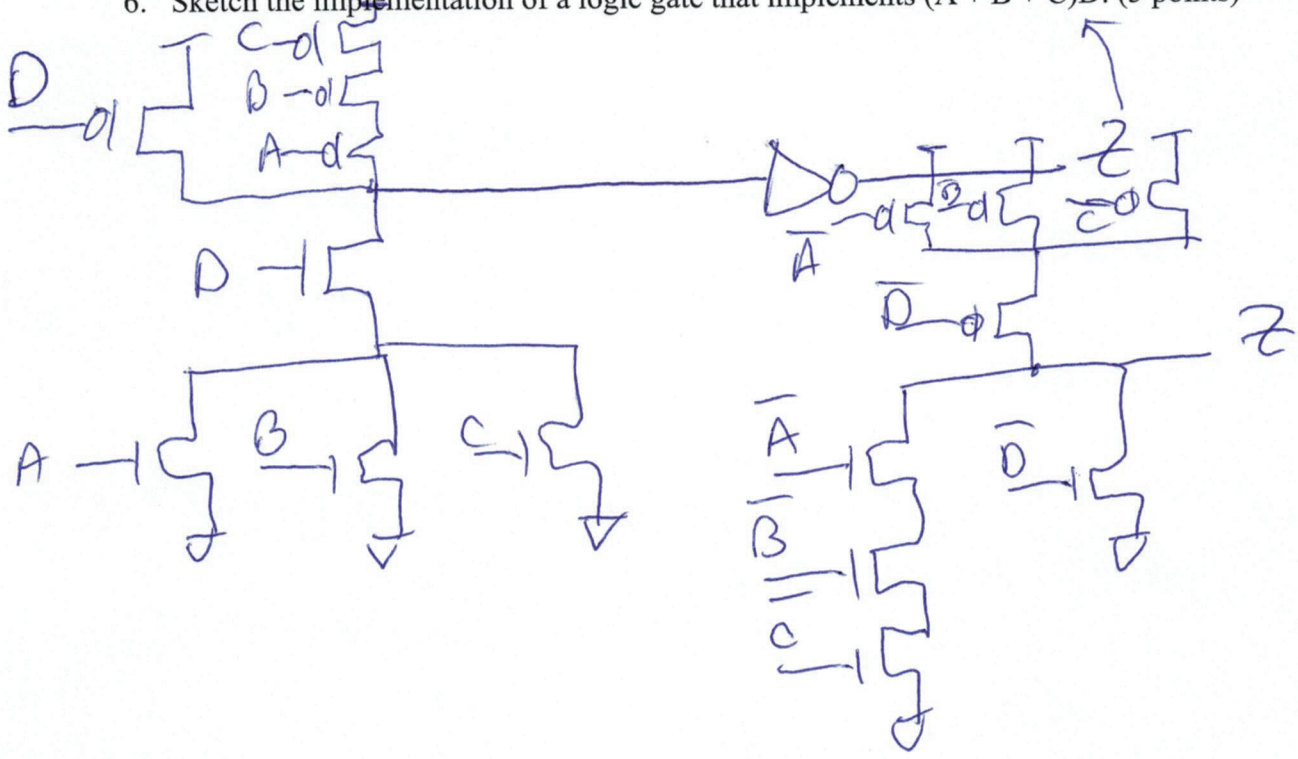
$t_{PHL} = 0.7 \cdot 20K \cdot \frac{6}{30} \cdot C_T$

(6)

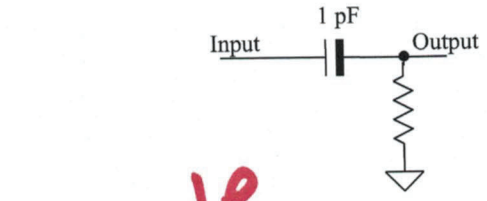
5. Sketch the layout of a poly2 resistor in the C5 process using the hi-res layer. Ensure you label the layers you are using including your connections to metal. (5 points).

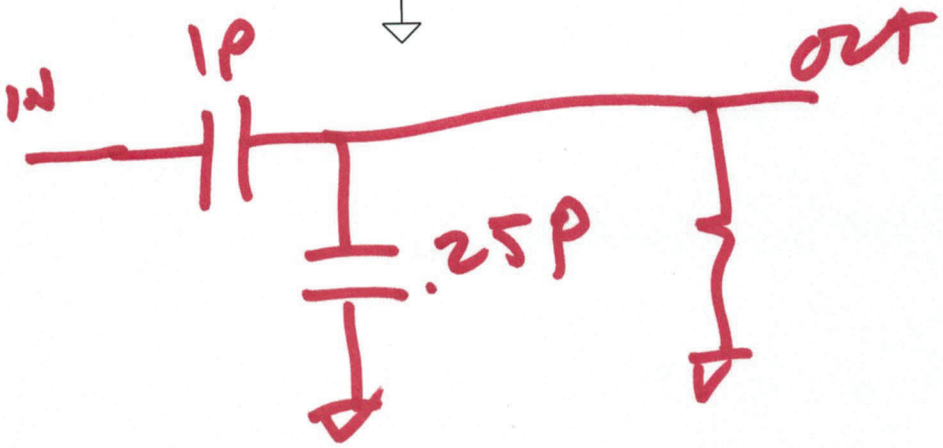


6. Sketch the implementation of a logic gate that implements (A + B + C)D. (5 points)



7. Suppose the bottom plate parasitic in the poly1-poly2 capacitor seen below is 25% of the desired capacitance value (here 1 pF). If the resistor is large so its effects can be neglected estimate the output voltage change if the input voltage changes from 0 to *VDD*. Sketch the schematic of the equivalent circuit. Please place a box around your numerical answer (this means put a box around a number, you know *VDD* from the first page of this exam). (10 points)



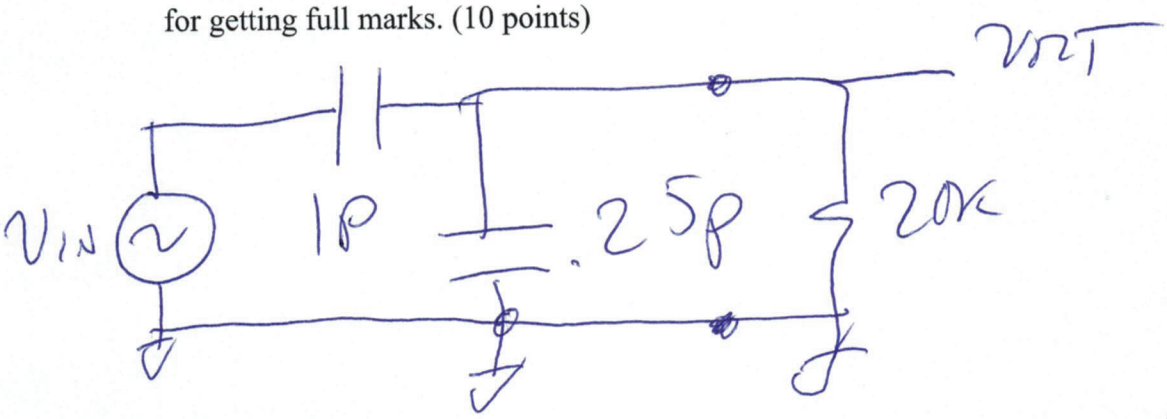


$$V_{OUT} = V_{IN} \cdot \frac{\frac{1}{j\omega .25p}}{\frac{1}{j\omega .25p} + \frac{1}{j\omega 1p}}$$

$$V_{OUT} = 5 \cdot \frac{1}{1 + .25}$$

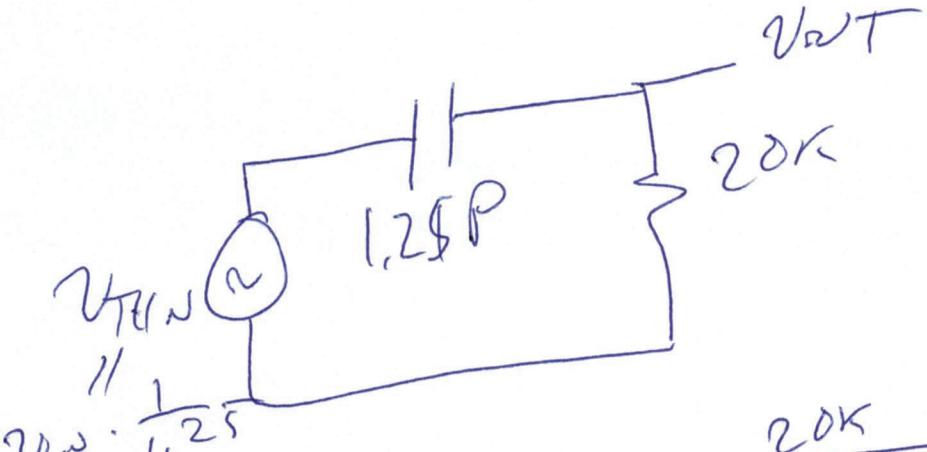
8)

8. If the resistor value is 20k in the previous problem and an AC voltage is applied to the input estimate the frequency where the output AC voltage is half of the AC input voltage. Sketch the schematic of the equivalent circuit ensuring the bottom plate parasitic's location is clear. Please place a box around your numerical answer. As in all of the problems on this exam showing your work is important for getting full marks. (10 points)



$$Z_{TH} = 1.25P$$

$$V_{OC} = V_{THV} = V_{IN} \cdot \frac{1}{1.+.25}$$



$$\frac{1}{j}\cdot\frac{j}{j} = \frac{j}{-1}$$

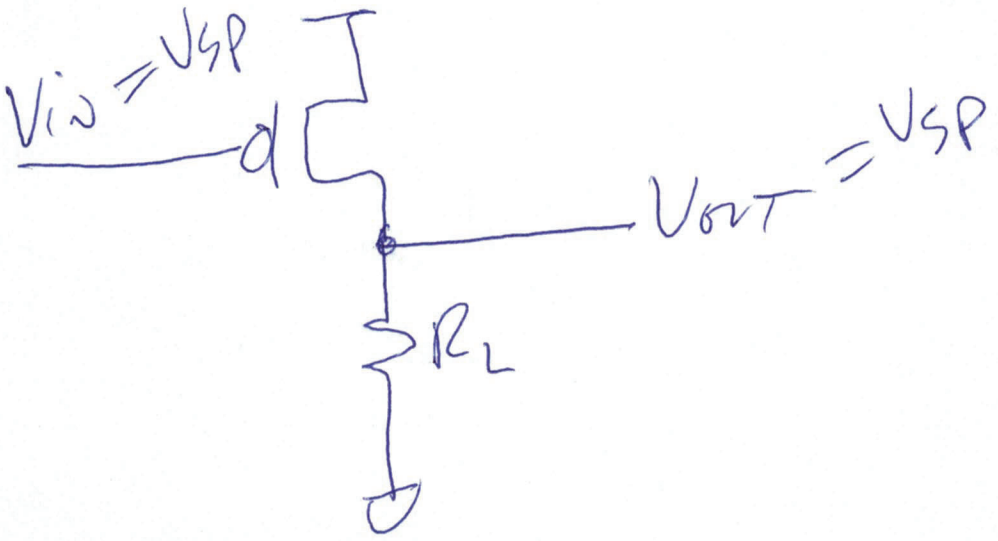
$$\frac{V_{IN}}{2} = V_{OUT} = \frac{V_{IN}}{1.25} \cdot \frac{20K}{20K + \frac{1}{j\omega 1.25P}}$$

$$\frac{-j}{2\pi f\, 1.25P}$$

$$1 = \frac{2}{1.25} \cdot \frac{20K}{\sqrt{20K^2 + \left(\frac{1}{2\pi f \cdot 1.25P}\right)^2}}$$

9

9. Show how to derive the equation for the V_{SP} of an inverter formed using a PMOS device and a resistor. (10 points)



$$\frac{V_{SP}}{R_L} = \frac{KP_P}{2} \cdot \frac{W}{L} \cdot \left(VDD - V_{SP} - V_{THP}\right)^2$$

$$0 = \underbrace{\frac{KP_P}{2} \cdot \frac{W}{L} R_L}_{X}\left(\left(VDD - V_{THP}\right)^2 - 2V_{SP}\left(VDD - V_{THP}\right) + V_{SP}^2\right) - V_{SP}$$

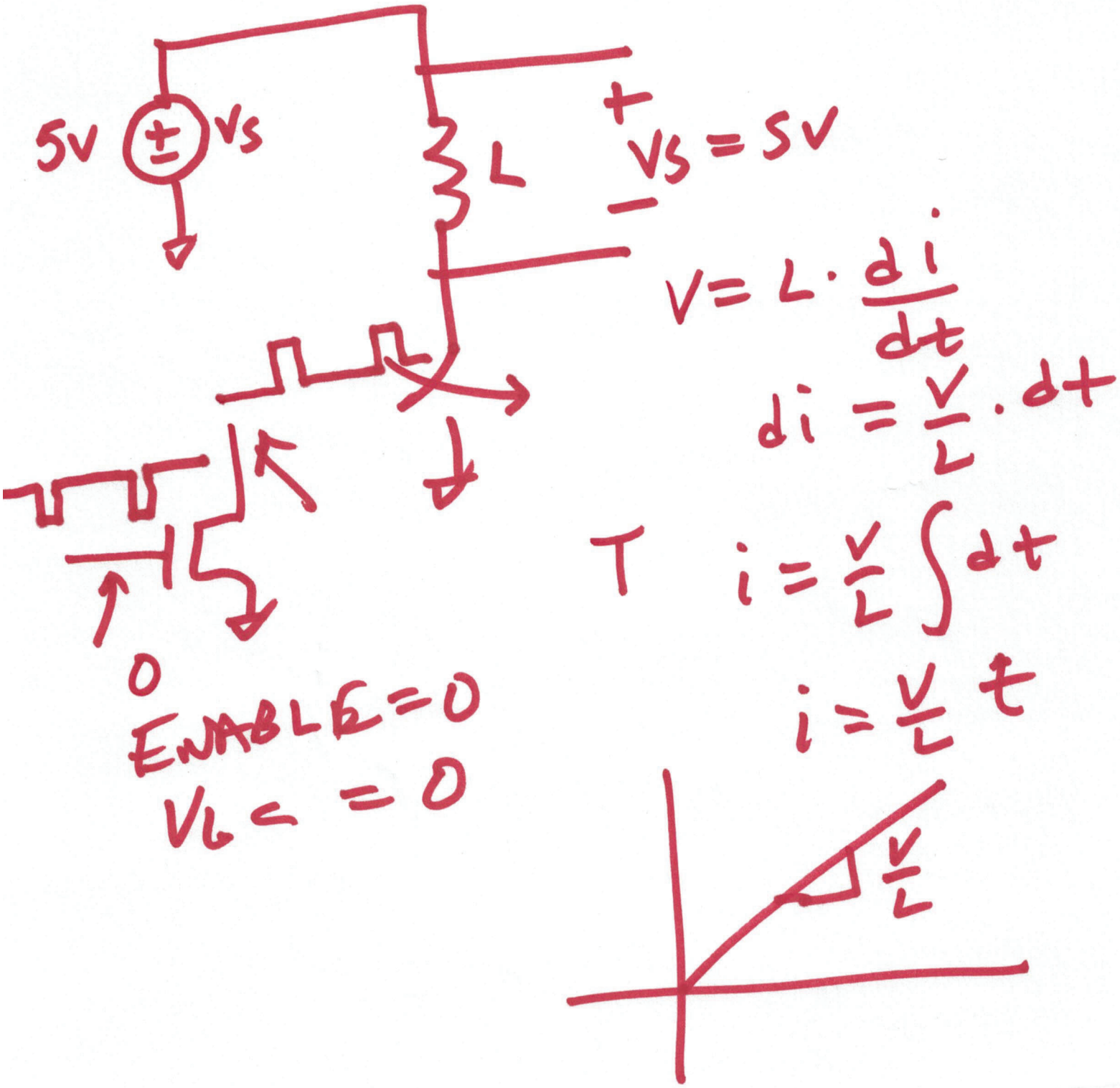
$$0 = X\left(VDD - V_{THP}\right)^2 - \left(2X\left(VDD - V_{THP}\right) + 1\right)V_{SP} + V_{SP}^2 \cdot X$$

$$V_{SP}^2 - \underbrace{\left(2X\left(VDD - V_{THP}\right) + 1\right)}_{X} V_{SP} + \left(VDD - V_{THP}\right)^2 = 0$$

$$V_{SP} = \frac{\left(\underbrace{2X\left(VDD - V_{THP}\right) + 1}_{X}\right) \pm \sqrt{4\left(VDD - V_{THP}\right)^2}}{2}$$

10)

10. What happens to the current in an inductor if a constant voltage is applied across the inductor? Give an example, in your course projects, of when this happens. (15 points)



11)