

ATOMIC LAYER DEPOSITED ALUMINUM OXIDE AND  
PARYLENE C BI-LAYER ENCAPSULATION FOR  
BIOMEDICAL IMPLANTABLE DEVICES

by

Xianzong Xie

A dissertation submitted to the faculty of  
The University of Utah  
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

Department of Electrical and Computing Engineering

The University of Utah

December 2013

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# The University of Utah Graduate School

## STATEMENT OF DISSERTATION APPROVAL

The dissertation of Xianzong Xie  
has been approved by the following supervisory committee members:

<u>Florian Solzbacher</u>	, Chair	<u>09/03/2013</u> Date Approved
<u>Loren Rieth</u>	, Member	<u>08/26/2013</u> Date Approved
<u>Carlos Mastrangelo</u>	, Member	<u>08/26/2013</u> Date Approved
<u>Richard Normann</u>	, Member	<u>08/28/2013</u> Date Approved
<u>Richard Cohen</u>	, Member	<u>08/30/2013</u> Date Approved

and by Gianluca Lazzi, Chair/Dean of  
the Department/College/School of Electrical and Computer Engineering

and by David B. Kieda, Dean of The Graduate School.

## ABSTRACT

Biomedical implantable devices have been developed for both research and clinical applications, to stimulate and record physiological signals *in vivo*. Chronic use of biomedical devices with thin-film-based encapsulation in large scale is impeded by their lack of long-term functionality and stability. Biostable, biocompatible, conformal, and electrically insulating coatings that sustain chronic implantation are essential for chip-scale implantable electronic systems. Even though many materials have been studied to for this purpose, to date, no encapsulation method has been thoroughly characterized or qualified as a broadly applicable long-term hermetic encapsulation for biomedical implantable devices.

In this work, atomic layer deposited  $\text{Al}_2\text{O}_3$  and Parylene C bi-layer was investigated as encapsulation for biomedical devices. The combination of ALD  $\text{Al}_2\text{O}_3$  and CVD Parylene C encapsulation extended the lifetime of coated interdigitated electrodes (IDEs) to up to 72 months (to date) with low leakage current of  $\sim 15$  pA. The long lifetime was achieved by significantly reducing moisture permeation due to the ALD  $\text{Al}_2\text{O}_3$  layer. Moreover, the bi-layer encapsulation separates the permeated moisture (mostly at the  $\text{Al}_2\text{O}_3$  and Parylene interface) from the surface contaminants (mostly at the device and  $\text{Al}_2\text{O}_3$  interface), preventing the formation of localized electrolyte through condensation.  $\text{Al}_2\text{O}_3$  works as an inner moisture barrier and Parylene works as an external

ion barrier, preventing contact of  $\text{Al}_2\text{O}_3$  with liquid water, and slowing the kinetics of alumina corrosion.

Selective removal of encapsulation materials is required to expose the active sites for interacting with physiological environment. A self-aligned mask process with three steps was developed to expose active sites, composed of laser ablation, oxygen plasma etching, and BOE etching.  $\text{Al}_2\text{O}_3$  layer was found to prevent the formation of microcracks in the iridium oxide film during laser ablation. Bi-layer encapsulated iridium oxide had higher charge injection capacity and similar electrochemical impedance compared with Parylene C coated iridium oxide film after deinsulation.

The  $\text{Al}_2\text{O}_3$  and Parylene C bi-layer encapsulation was applied to Utah electrode array (UEA)-based neural interfaces to study its long-term performance. The median tip impedance of the bi-layer encapsulated wired Utah electrode array increased slowly during the 960 days of equivalent soak testing at 37 °C. Impedance for Parylene coated UEA dropped 50% to 75% within 6 months. In addition, bi-layer coated fully integrated Utah array-based wireless neural interfaces had stable power-up frequencies at ~910 MHz and constant RF signal strength of -50 dBm during the 1044 days of equivalent soaking time at 37 °C. This is much longer than lifetime achieved with Parylene C coating, which was about one year at room temperature.

To

My wife Yi Li and my dear family, who made all this possible

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## ACKNOWLEDGEMENTS

Many people deserve credit for assisting me during the past five years of my PhD study. My deepest gratitude goes to my advisor Prof. Florian Solzbacher for his continuous support of my PhD research, for his insight, motivation, and immense knowledge. I would like to sincerely thank my committee members for their guidance: Dr. Loren Rieth, Prof. Richard A. Normann, Prof. Carlos Mastrangelo, and Prof. Richard Cohen.

Special thanks to Dr. Loren Rieth for his insight on scientific problems and article proofreading. Appreciation is extended to Dr. Prashant Tathireddy for invaluable discussion.

I also thank Rohit Sharma, Ryan Caldwell, Dr. Mohit Diwekar, Mahender Avula, Tanya Abaya, Je-Min Yoo, Dr. Xiaoxin Chen, Dr. Sandeep Negi, Dr. Rajmohan Bhandari, Dr. Asha Sharma, and Dr. Layne Williams for their assistance during my PhD research. Gratitude is extended to Microfab staff for their help on equipment maintenance and training.

Finally, I would like to thank my dear wife Yi Li, and my family for their unconditional support and love, which made this long journey possible.

## CHAPTER 1

### INTRODUCTION

Implantable electronic systems and devices have undergone significant development over the past few decades for both research and clinic applications, to monitor, stimulate, and record physiological responses *in vivo*. The progress in implantable devices is made possible by both the accumulating knowledge of human neuron-motor systems, and technology advances in semiconductor industry and microelectromechanic systems (MEMS). Neural interfaces are implantable devices developed for applications such as neuroprosthetics and neuroscience to diagnose and treat neuron-related disorders and diseases. Lack of long-term functionality and stability of these devices has prevented them from widely chronic usage. Various factors could contribute to the failure of implantable devices, including device corrosion and decreased encapsulation impedance caused by coating degradation, connector problems, and/or foreign body responses. Fully integrated, wireless, silicon-based neural interfaces have been developed to eliminate connector problems and remove the risk of infection associated with percutaneous wired connectors. Long-term stable, conformal, biocompatible, and highly insulating coating materials and methods have been investigated to address the failure modes due to encapsulation failure for chronic implantation. Even through a large number of materials have been proposed for encapsulating biomedical implantable devices, they all have

unique drawbacks and limitations. In this work, an atomic layer deposited (ALD)  $\text{Al}_2\text{O}_3$  and chemical vapor deposited (CVD) Parylene C bi-layer encapsulation is studied as a candidate for encapsulating chronic neural interface implants. The ALD  $\text{Al}_2\text{O}_3$  works as a water vapor barrier due to its extremely low water vapor transmission rate; Parylene C thin film serves as an ion barrier. Moreover, Parylene prevents the direct contact of liquid water with ALD  $\text{Al}_2\text{O}_3$ , thus stopping the ALD  $\text{Al}_2\text{O}_3$  dissolution. This bi-layer encapsulation is used to significantly reduce water vapor permeation and separate the substrate surface contaminants (ions, metal particles, etc.) from the penetrated water moisture at the interface between  $\text{Al}_2\text{O}_3$  and Parylene.

The introduction chapter is composed of five sections, starting with various implantable devices and their applications, followed by the requirements for encapsulating implantable devices. Then encapsulation failure modes are discussed for different materials and methods in section 4. The approaches, aims, and results of this work are introduced in the last section.

### 1.1 Implantable Devices

Implantable devices, such as bio-sensors, cardiac pacemakers, implantable cardioverter defibrillators, cochlear implants, deep brain stimulators, and neural interfaces, are being implanted into patients worldwide [1-8] for different research and clinic purposes. Pacemakers utilize implanted electrodes to deliver electrical pulses to control the heart rate. Cochlear implants are electronic implantable devices that directly stimulate the cochlea to enable hearing in profoundly deaf patients. According to the Food and Drug Administration, approximately 219,000 people have received cochlear

implants as of December 2010. Deep brain stimulators are used to treat movement and affective disorders such as chronic pain, Parkinson's disease, epilepsy, tremor, and dystonia, by sending electrical stimulating pulses to the specific parts of the brain [9]. A deep brain stimulator typically consists of three components: the neurostimulator, the lead, and the extension. The extension, essentially an insulated wire, connects the lead, and the neurostimulator. Deep brain stimulation has demonstrated therapeutic benefits for otherwise treatment-resistant diseases [10-13].

Neural interfaces have been developed for neuroprosthetics to restore functions for patients with communication issues between the central and peripheral nervous system or the muscles. The potential of regaining functions using neural prosthesis has been pursued for decades for paralyzed patients [14-18]. Clinical trials of neural interfaces were made possible by major advances in developing implantable systems, which demonstrated the potential efficacy of this technology [8, 19-21]. Combination of neural interfaces with prosthetic devices as therapies for neuronal disorders is very promising.

## 1.2 Electrode Arrays

Two major types of electrodes have been developed for neural interface devices to record or stimulate neural signals: surface electrodes and penetrating electrodes. Surface electrodes are mostly noninvasive or less invasive, thus causing less tissue damage and foreign body response. This is at the cost of low selectivity and sensitivity. They usually measure localized field potentials (LFPs) from relatively large populations of neurons. Also, they lack the ability to access neural signal from deeper in the tissue. Penetrating electrodes can detect smaller signals from a single neuron unit due to high selectivity and

sensitivity, at the cost of tissue damage and foreign body response. Examples of penetrating electrodes for chronic implantation include the iridium wire array [22, 23], the floating microelectrode array (FMA) [24], the Michigan array [15], and the Utah electrode array [25, 26].

The iridium wire arrays have been investigated to have long-term stability for chronic implantation [22, 23]. The good recording performance of the iridium wire array was achieved by the findings that there was negligible connective tissue encapsulation or edema at the active electrode tips and large neurons presented around the active electrode tips. The issue with this handcrafted iridium wire array is the lack of quality control and repeatability. Therefore, they are not suitable for mass production. Floating microelectrode arrays (FMAs) with electrodes made of platinum/iridium 70%/30% have showed the potential for chronic implantation [24]. The advantages of FMAs are the flexibility of electrode length and potential random distribution of individual electrodes. However, the fabrication process is expensive, time-consuming, and also lacks control.

Development of silicon-based micromachined electrode arrays with long-term stability, repeatability, and potential of mass production for commercialization was made possible by the advances in MEMS technology. Even through large numbers of fabrication methods and configurations of microelectrode arrays can be found in the literature for neural recording and stimulation, two major silicon-based electrodes have been commercialized and widely used: the Michigan array and the Utah electrode array (UEA). Active recording sites of the Michigan array are positioned along the silicon electrode shanks. This design enables the Michigan array to be able to record neural signals from variable depths of tissue on each electrode shank. However, tissue damage

during the implantation process decreases the quality of recorded signals. Also, the glial scar formation after insertion can isolate the active sites from adjacent neurons and impair the recording capabilities. The UEA consists of 100 microelectrodes with typical lengths of 1.0 and 1.5 mm and pitch of 400  $\mu\text{m}$ , as shown in Fig 1.1. The encapsulation of the electrode tip was removed to expose the active metal (iridium oxide) electrode sites for recording/stimulation purposes, as shown in Fig 1.2. In contrast with the Michigan array, active sites of the UEA are only available at the electrode tips, where tissue damage is typically minimal. The UEA is also the only FDA-cleared neural interfaces, which has an investigation device exemption (IDE). Clinical research usage of UEA has been reported in recent years [8, 21, 27], demonstrated the efficacy of the UEA-based neural interfaces for neuroprosthetics.

### 1.3 Encapsulation of Implantable Devices

Implantable devices integrated with active electronics need to be protected from the physiological environment in order to perform their designated functions, which is a particular challenge for chronically implanted devices. Encapsulation needs to meet specific requirements for individual applications, but there are some basic requirements that apply to most of the implantable devices, including biocompatibility, biostability, sufficient mechanical strength, high electrical resistance, low dielectric constant, conformal and pin-hole free coating, low process temperatures, and compatibility with sterilization process(es).

- (a) Biocompatibility: The encapsulation materials must be nontoxic, and should have minimal or no contribution to the acute and chronic foreign body responses due to the implantation of the devices, which can be bioinert or bioactive.
- (b) Biostability: There must be no discernible dissolution or degradation of the material and no material property changes in the physiological environment for the intended lifetime of the device.
- (c) Mechanical strength: Sufficient mechanical strength is required to maintain the coating integrity during the handling (surgical and fabrication) and implantation process.
- (d) High insulation resistance and low dielectric constant: Coating with high insulation resistance and low dielectric constant can reduce the signal loss through shunting and capacitive cross-talk between channels, and maximize signal to noise ratio.
- (e) Conformal and pin-hole free coating: Conformal coating helps to maintain the original geometry of the devices, which can affect the surgical process and foreign body response after implantation.
- (f) Low process temperature: Implantable medical systems usually contain multiple components, composed of various materials. Polymers, solders, metal contacts, and integrated circuits are susceptible to high temperature (over 200 °C). The lowest temperature tolerance among all materials in the whole device sets the limit for encapsulation process temperature.



(g) Sterilization: The coating has to be able to withstand one or more sterilization processes, which is essential for an implantable device before implantation. The common sterilization procedures are steam and ethylene oxide gas.

Other than the aforementioned requirements, selective deinsulation of encapsulation without affecting the overall coating performance to expose the localized active sites is necessary for information exchange between the implantable device and the physiological environment. The proper selective etching process has to be developed for the encapsulation.

#### 1.4 Failure of Implantable Devices

There are three main failure mechanisms for implantable devices: connection failure, failure due to foreign body response, and encapsulation failure. Connection failure is ascribed to mechanical stress, handling forces, etc. This failure mode can be solved by developing wireless implantable devices [28-33]. The elimination of tethering forces can also reduce foreign body response [34]. The absence of wires for connection also reduces infection likelihood [35]. Another major failure mode of an implantable device results from the foreign body response. The initial tissue damage due to the implantation process evokes inflammatory response to protect the body from potential hazards. The mechanisms behind this are not fully understood. The foreign body response can be partially alleviated by minimizing surgical trauma. Also, implantation procedures and surgical techniques can be optimized to reduce the foreign body response induced by the implants [36, 37]. The geometry of implanted devices is reported to also have impact on acute immune response [38]. The presence of foreign materials provoke the foreign body

response, leading to formation of scar tissue encapsulating the implants [39]. As the scar tissue grows, it isolates the implant from its surrounding tissue and neurons, thus attenuating the electrical signals. The eventual complete isolation of signals leads to a loss of function for implantable devices. For UEAs, the typical progression of degradation is first decreasing single unit signal intensity, then loss of single unit but continued LFPs and multi-unit recording, with gradually degrading loss of signals. The foreign body response is affected by mechanical flexibility [40] and surface properties of the implants [41]. Coating implantable devices with a noninteractive or antifouling surface [42] to reduce the protein absorption was used to reduce scar tissue formation and enhance biocompatibility. Use of conductive polymers (such as PEDOT and Polypyrrole) combined with agents aimed at promoting neuron growth around recording sites is also utilized to improve the performance of implantable devices [43, 44].

Encapsulation failure is another major failure mode. The primary failure points of implantable devices are the interfaces of various components and the coating layer, where water vapor and ions permeate and accumulate [45]. Moisture ingress can lead to failures such as open circuits [46], short circuits [47-49], corrosion/dissolution of different materials [50], electrical leakage [47], and delamination of coating materials. The consequences are catastrophic and can lead to complete device failure. Tremendous efforts have been devoted to address this issue using different materials and approaches, including silicon carbide, diamond-like carbon (DLC), silicon nitride, urethanes, polyimide, Teflon, silicone, Parylene, *etc.* [51-58]. Most of those materials and methods have their own drawbacks, which make them nonideal candidates for encapsulation of implantable devices. For example, silicon carbide typically requires high deposition

temperature and is prone to have pinholes [59], silicon nitride slowly dissolves in PBS solution [57], and DLC coating has adhesion problems and also delaminates over time [56, 60-62]. Polymeric materials exhibit relative high water vapor transmission rate (WVTR) and poor adhesion [57, 58]. This work is focusing on the encapsulation failure and trying to address this issue by combining atomic layer deposited (ALD)  $\text{Al}_2\text{O}_3$  and Parylene C. The ALD  $\text{Al}_2\text{O}_3$  is used to block water vapor permeation; the Parylene C layer is an ion barrier and also prevents liquid water from contacting with ALD  $\text{Al}_2\text{O}_3$  and dissolving it.

### 1.5 Hypothesis, Approaches and Specific Aims

Encapsulation with low water vapor transmission rate (WVTR) is important to reduce the water vapor permeation and slow down the corrosion process. Typically WVTR for polymers is in the order of  $10^{-2}$  g·mm/m<sup>2</sup>·day, which is too high for moisture sensitive applications [63]. Atomic layer deposited (ALD)  $\text{Al}_2\text{O}_3$  (alumina) has demonstrated extremely low WVTR in the order of  $10^{-10}$  g·mm/m<sup>2</sup>·day [64-67]. The biocompatibility of bulk  $\text{Al}_2\text{O}_3$  is comparable to that of corrosion-resistant metals like titanium [68]. It has been reported that ALD alumina coated glass slides had slight better biocompatibility compared with uncoated glass slides in terms of cell proliferation and cell activity [69]. Also bulk alumina was used as substrate for floating microelectrode arrays for neural recording, suggesting it is reasonable for use with neural tissue, at least if encapsulated [24]. Liquid water is known to corrode ALD  $\text{Al}_2\text{O}_3$  thin films [70] mostly due to the high concentration of hydrogen in the form of hydroxyls in the film [71, 72]; therefore, ALD  $\text{Al}_2\text{O}_3$  alone is not suitable for encapsulation of biomedical implants directly exposed to

physiological environment. A thin-film encapsulation layer that drastically reduces the dissolution kinetics of the alumina film could be highly effective at preserving the integrity of this layer, and allowing it to maintain its ultra-low permeation characteristics. We investigate the use of Parylene-C as the overlayer, due to its demonstrated effectiveness for implantable devices, and in particular the UEA.

Parylene C has been widely utilized in various electronic and biomedical devices to protect them from the harsh environment. Biomedical applications of Parylene include blood pressure sensors, stent coating, bone pins, bio-MEMS, and neural recording/stimulating electrodes [53, 73-78]. Among polymeric materials, Parylene C has a relatively low water absorption (0.1%) [79]. Parylene C has demonstrated thermal and chemical stability [79]. Parylene C is an excellent ion barrier to  $\text{Na}^+$ ,  $\text{K}^+$ ,  $\text{Cl}^-$ , etc. [80], which is critical for devices exposed to physiological environment. Parylene is also believed to be nontoxic after being used in medical devices for many decades with very few negative reports [8, 81-83]. Although Parylene C has relatively low WVTR of  $0.4 \text{ g}\cdot\text{mm}/\text{m}^2\cdot\text{day}$  [84] among polymeric materials, better moisture barrier is needed to significantly reduce the water vapor permeation rate and slow down the condensation of moisture around ion contaminants to form electrolyte, in order to further extend the lifetime of implantable devices [85].

Our hypothesis is that the combination of ALD  $\text{Al}_2\text{O}_3$  and CVD Parylene C can address the encapsulation failure mode by significantly reducing moisture permeation. Moreover, the bi-layer encapsulation separates the permeated moisture (mostly at the  $\text{Al}_2\text{O}_3$  and Parylene interface) from the surface contaminants like ions and metal particles (mostly at the device and  $\text{Al}_2\text{O}_3$  interface), preventing the formation of electrolyte

through moisture condensation.  $\text{Al}_2\text{O}_3$  works as an inner moisture barrier and Parylene works as an external ion barrier, and slows down the kinetics of alumina corrosion. The specific aims of this study are as follows:

- (a) Develop deposition process and optimize process parameters of ALD  $\text{Al}_2\text{O}_3$  at low temperature using plasma-assisted ALD.
- (b) Characterize ALD  $\text{Al}_2\text{O}_3$  thin film and evaluate the  $\text{Al}_2\text{O}_3$  and Parylene C bi-layer encapsulation performance based on interdigitated electrode (IDE) test structures.
- (c) Investigate and compare the effect of temperature, topography, and bias voltage on  $\text{Al}_2\text{O}_3$  and Parylene C bi-layer encapsulation and Parylene C encapsulation on lifetime based on IDE test structures.
- (d) Develop and optimize selective etching process for  $\text{Al}_2\text{O}_3$  and Parylene C bi-layer encapsulated implantable devices to expose active sites for neural recording/stimulation.
- (e) Study the effect of deinsulation process on charge injection capacity (CIC), charge storage capacity (CSC), and electrochemical impedance of the tip metal iridium oxide for neural interface applications.
- (f) Evaluate the long-term impedance stability, device reliability, RF power-up frequency, and signal strength constancy of  $\text{Al}_2\text{O}_3$  and Parylene C bi-layer coated Utah electrode array (UEA)-based neural interfaces.

Chapter 2 reviews the state-of-the-art of coating materials and related deposition techniques. Research background and literature review of different coating approaches are also covered in this chapter.

Chapter 3 is reprinted from the article published in Applied Physics Letter [86]. It includes the deposition, characterization of Al<sub>2</sub>O<sub>3</sub> and Parylene C bi-layer encapsulation. It also reports the *in vitro* soak testing performance of the bi-layer encapsulation based on IDE test structures.

Chapter 4 covers the long-term performance of Al<sub>2</sub>O<sub>3</sub> and Parylene C bi-layer encapsulation for chronic implantable devices [87]. The effects of temperature, topography, and bias voltage on encapsulation performance were studied and comparison between Al<sub>2</sub>O<sub>3</sub> and Parylene C bi-layer encapsulation and Parylene C encapsulation were performed.

Chapter 5 reports a self-masked deinsulation process for Al<sub>2</sub>O<sub>3</sub> and Parylene C bi-layer encapsulated neural interfaces. The effects of deinsulation process on CIC, CSC, and electrochemical impedance of iridium oxide were evaluated.

Chapter 6 assessed the long-term performance of Al<sub>2</sub>O<sub>3</sub> and Parylene C bi-layer encapsulation on neural interfaces. Long-term impedance stability of wired UEAs and RF power-up frequency and signal strength consistency of wireless integrated neural interfaces were assessed.

Chapter 7 concludes the work of this dissertation and proposes future work.

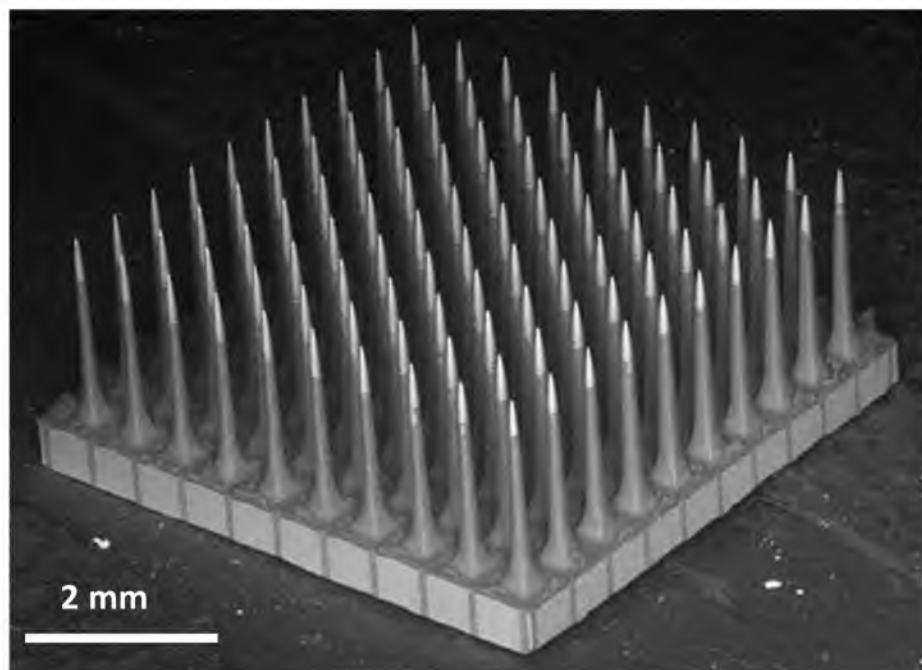


Fig 1.1 Scanning electron micrograph of the UEA with 100 (10 by 10) silicon electrodes. The electrode length is 1.5 mm and space between electrodes is 400  $\mu\text{m}$ .

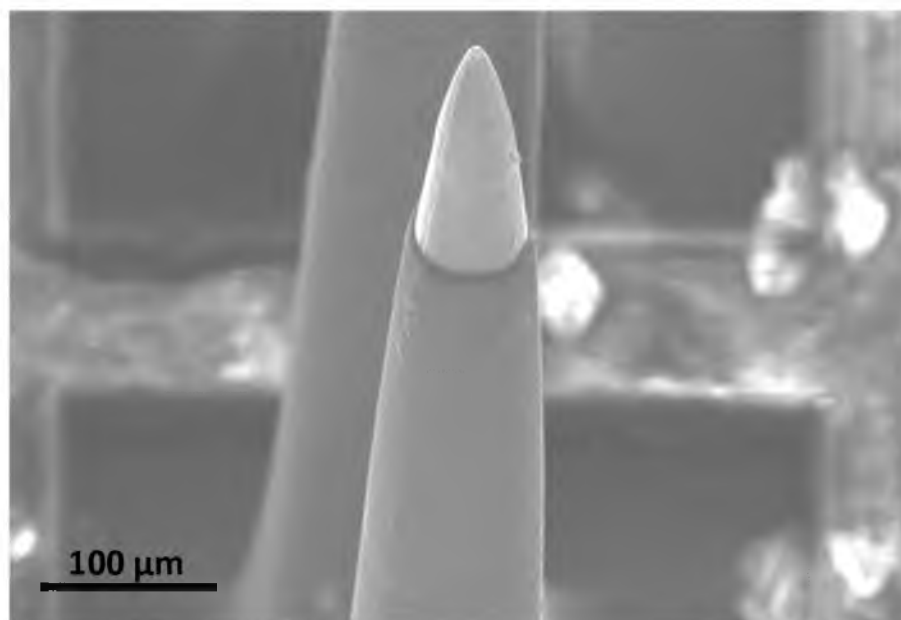


Fig 2.2 Scanning electron micrograph of single exposed electrode of the UEA with exposed active tip.

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## CHAPTER 2

### STATE OF THE ART: NEURAL ELECTRODE ARRAYS, ENCAPSULATION MATERIALS, AND SELECTIVE DEINSULATION

#### 2.1 Introduction

This chapter conveys the state of the art of neural electrode arrays and advances in wireless neural recording and stimulation by integrating active electronics, and existing encapsulation methods for implantable devices. Wireless neural interfaces proposed new challenges for encapsulation, especially for devices under continuous bias voltage in the physiological environment. The methods of traditional hermetic encapsulation and emerging thin-film-based encapsulation are compared. Various encapsulation material candidates that are widely used in both research and industry for biomedical implantable devices and their corresponding application techniques are reviewed. The advantages and drawbacks of each material/deposition method are covered based on the requirements of implantable devices. The last section of the chapter discusses the deinsulation processes for selectively exposing active electrical sites for biomedical applications.

#### 2.2 Neural Electrode Arrays

The technology developed in this work is a platform technology that can likely be applied to many biomedical implantable devices. This work focused on developing



encapsulations for neural interfaces, due to the recognized challenges like sizes, materials compatibility, and complex geometries in these systems. Neural interfaces based on the Utah electrode array (UEA) have been developed for decades as implantable devices for recording/stimulating neurons at the University of Utah [1-3]. Neural interfaces were chosen to evaluate the performance of atomic layer deposited  $\text{Al}_2\text{O}_3$  and Parylene C bi-layer encapsulation because they are widely used in both research and clinical trials and lack of long-term effective encapsulation for chronic implantation. Moreover, UEA-based neural interfaces are very representative of implantable devices because of their complex topography, combination of different materials, and complicated multiple fabrication processes.

### 2.2.1 Microwire Arrays

Microwire arrays for neural recording in cortex was pioneered by Salcman using glass insulated Pt/Ir wire [4] or Parylene insulated pure Ir wire [5]. The use of single microwire was designed to reduce the displacement of microwire after implantation due to the cortical movement. However, single wire can only record from a small area. Therefore, microwire arrays were developed to increase the available recording sites and investigate the arrangement of neural circuits.

Microwire arrays use commercially available corrosion-resistive wires that have enough mechanical strength for fabrication and insertion. Typical materials include tungsten, iridium, or platinum/iridium alloy wires. Williams *et al.* reported a 35- $\mu\text{m}$  tungsten wire-based microelectrode array [6]. The array consists of 2 rows of 11 microwires, electrically connected to a back-end connector, as shown in Fig 2.1. Liu *et*

*al.* fabricated another type of microelectrode array by inserting 16 Ir wires into epoxy backplate to form a 4 by 4 array [7, 8]. Commercially available microwire arrays have been developed similar to aforementioned structures. Microprobe Inc. provides up to 64 channels of stainless steel or Pt/Ir fine wire-based microelectrode arrays with Teflon or polyimide as insulation material [9]. Tucker Davis Technologies uses polyimide insulated tungsten microwires to make arrays up to 64 channels [10]. The assembly process and size constraints limit the mass production of microwire arrays.

### 2.2.2 Silicon-Based Microelectrode Arrays

Compared with microwire arrays, silicon-based micromachined electrodes have many attractive properties. Advantages include precise control of electrode geometry, the elimination of time-consuming assembly processes, potential of mass production with high repeatability, and compatibility with integration of active electronics for wireless implantable systems. Two major and commercially available designs of silicon-based microelectrode arrays are the Michigan array and the Utah electrode array (UEA).

#### 2.2.2.1 The Michigan Array

The University of Michigan has been developing and improving the silicon-based Michigan array for the last four decades [11-13]. A micromachined planar array on a tapered silicon beam was reported by Wise *et al.* [13], shown in Fig 2.2. Silicon oxide was used as insulation materials for the array tip. A revised version of the Michigan multielectrode array was developed by Najafi in 1985 [14]. Advances include the achievement of multiple recording sites on a single shank with 3-mm in length, 50- $\mu$ m in

width, and 15- $\mu\text{m}$  in thickness. Highly boron-doped silicon by diffusion was used as a etch stop during the wet etching. The fabrication process was compatible with metal-oxide semiconductor (MOS) integrated circuit fabrication allowing the addition of circuitry for signal amplification and multiplexing [15, 16]. The development of silicon ribbon cable provided high flexibility between the microelectrode array and back-end connectors [17]. This was further improved by the later-developed Parylene cable [11]. The three-dimensional multielectrode Michigan array was designed and fabricated by Hoogerwerf in 1994 [12], as shown in Fig 2.3. Other major modifications include the change of recording-site metal from gold and platinum or iridium [18], and adding wireless capabilities for eliminating connecting cables [19].

#### 2.2.2.2 The Utah Electrode Array

Other than the aforementioned commercially available Michigan array, the Utah Electrode Array (UEA) is the other popular option for neural interfaces, with commercial availability and food and drug administration (FDA) clearances. Richard Normann first designed and fabricated the three-dimensional UEA for intracortical stimulation [2]. A dicing saw was used to cut silicon wafers and create columns with dimension of 150  $\mu\text{m}$  square, 1.5 mm tall, and pitch of 400  $\mu\text{m}$ . The columns were first thinned and then tapered by wet etching. Platinum was used as electrode active site metallization and the UEA was insulated by polyimide using dip coating.

Later versions of the UEA were improved by the utilization of Pt/Ti/W/Pt as active tip metal [1]. Glass was used as insulation material between individual electrodes to improve the electrical isolation of electrodes and reduce cross-talk [1]. The Utah Slant

Electrode Array (USEA) was later developed by varying the length of electrodes in one direction, which gave the ability of accessing the nerve fascicle across the cross-section of peripheral nerves [20]. The insulation of the UEA was further improved by adopting chemical vapor-deposited Parylene C to replace dip coated polyimide, in order to obtain a conformal and pin-hole free insulation layer [21]. Trials with human patients have been performed and the long-term effectiveness has been demonstrated with UEA-based neural interfaces [3, 22, 23]. Wireless integrated neural interfaces based on UEA have been reported recently to eliminate the wire bundles for electrical connection [24, 25], as shown in Fig 2.4. Compared with microwire arrays and Michigan arrays, the UEA has the advantages of batch process reproducibility and tip recording from undamaged tissue. This work uses UEA-based neural interfaces to evaluate the performance of proposed bi-layer encapsulation.

### 2.3 Hermetic and Thin-film-based Encapsulation

Implantable devices with active electronics must be able to perform their intended functions effectively and stably in the physiological environment over a long period of time. Encapsulation is critical to the success of implantable devices by protecting them from the body fluids. There are two major categories of encapsulation: hermetic and near-hermetic encapsulation. Hermetic encapsulation typically utilizes metal capsules, biocompatible ceramics, and glasses to build up an airtight and waterproof environment and keep the implanted device from being corroded by body fluids [26]. Near-hermetic encapsulation, on the other hand, use thin film layers to slow down or prevent the ingress of body fluids into the devices.

### 2.3.1 Hermetic Encapsulation

Typical materials that provide a hermetic barrier for implantable devices are metals, ceramics, and glasses. Metallic packaging generally uses a biocompatible metal capsule such as titanium. Metal capsule-based hermetic encapsulation has been successfully applied to pacemakers [27], cardioverter defibrillators [27], neuromuscular stimulators [27], and cochlear implants [28]. However, power-receiving coil and communication antenna need to be placed outside of the metallic hermetic packaging to avoid the interference of radio-frequency signal and loss of power through eddy-current formation in the packaging.

Biocompatible ceramics and glass have the advantage of radio-frequency transparency over metallic hermetic packaging. The application includes neuromuscular microstimulators [29], cochlear implants [30], and artificial retina implants [31]. Biocompatible ceramics used for hermetic coating include alumina [32-34], zirconia [35], and ceria stabilized zirconia poly-crystal [36, 37]. Biocompatible glasses, such as borosilicate glass, have been used for encapsulating neuromuscular microstimulators [38].

One of the challenges for hermetic encapsulation is feedthroughs. Conducting wires are necessary for signal entering and exiting the hermetic packaging. Fusion welding methods are usually used to form a hermetic seal between the packaging components and conductive wires, which could potentially go through a high-temperature process and damage the encapsulated device. Additionally, hermetic capsules tend to take more space compared with thin-film-based encapsulation, which conflicts with miniaturization for space-limited applications, such as neural implants.

### 2.3.2 Thin-film-based Encapsulation

There are mainly two different kinds of materials used for thin-film-based near-hermetic encapsulation for implantable devices: nonpolymeric and polymeric materials [26, 39]. Nonpolymeric materials mainly include silicon oxide, silicon nitride, silicon carbide, ultrananocrystalline diamond (UNCD), and diamond-like carbon (DLC); polymeric materials include polytetrafluoroethylene (PTFE), silicone elastomer, polyimide, and Parylene, etc.

Nonpolymeric materials like silicon oxide, silicon nitride, silicon carbide, UNCD, and DLC usually require chemical vapor deposition (CVD) with a relatively high temperature to obtain a uniform coating layer, which makes them incompatible with implantable devices incorporated with active electronics and various polymeric materials. Other drawbacks include dissolution in phosphate saline solution (PBS) (silicon nitride and silicon oxide) [40, 41], structural defects (pin-holes)[42], and nonconformal deposition [43].

On the other hand, polymeric materials are typically flexible and inexpensive. They also tend to have low process temperature. The challenges for polymer encapsulation of chronic implantable devices are relative high water vapor transmission rate (WVTR) (typically  $> 1 \text{ g/m}^2 \cdot \text{day}$ )[44], degradation of the material itself, and difficulties of forming conformal and pin-hole free thin films. The high WVTR makes moisture penetrating through the coated devices easier. A large volume of permeated moisture condenses around ion contaminants to form electrolyte, which corrodes the coated substrate and thus reduces the lifetime of the device. Degradation of materials includes hydrolytic, oxidative, and enzymatic mechanisms that deteriorate the chemical structures of the

polymer [45]. Polymers applied by dip coating or spin coating usually are lack of control of the film quality, such as pin-holes, adhesion, thickness, and its variations.

## 2.4 Nonpolymeric Materials for Encapsulating

### Implantable Devices

#### 2.4.1 Silicon Oxide and Silicon Nitride

Silicon oxide can be easily grown by oxidation process or deposited by CVD process. Silicon oxide has been used as insulation layer for the Michigan array back to 1970 [13]. The silicon oxide was formed by a thermal oxidation process, which requires high temperature ( $\sim 1000$  °C). Later CVD silicon oxide was used for protecting the Michigan array against the physiological environment [14]. SiO<sub>2</sub> passivation has also been applied to retina implants [46]. The major issue with SiO<sub>2</sub> passivation is that it dissolves *in vivo* over time. It has been showed that SiO<sub>2</sub> coating exhibited dissolution and underneath electronics (with 500 nm SiO<sub>2</sub> passivation) were exposed for retina implants after 10 months *in vivo* [40, 46].

Silicon nitride has also been utilized as an encapsulation material for implantable devices. It was used as part of the passivation for the Michigan array through CVD process as an addition to SiO<sub>2</sub> passivation [14]. Also, it was used to encapsulate photodiode in retina implants [42]. Silicon nitride often exhibits pin-holes and chemical reaction with saline solution with a dissolution rate of 1-2 nm per day, which lead to the loss of insulating functions to the underneath photodiode for retina implants [42]. Similar to silicon oxide, silicon nitride dissolves in PBS solution at 37 °C [41], indicating it is not an ideal candidate for encapsulating chronic implantable devices.

### 2.4.2 Ultrananocrystalline Diamond and Diamond-like Carbon

Ultrananocrystalline diamond (UNCD) films were reported to be relatively chemically inert [47], biocompatible, and bio-inactive [48-50], which make them a promising candidate for encapsulating implantable devices. In addition, the unique nanostructure of UNCD leads to a high wear-resistance and low friction surface [51], which facilitate maintaining the integrity of the coating during and after implantation.

UNCD film was developed first by Argonne National Laboratory with microwave plasma-enhanced chemical vapor deposition (MPECVD) [52, 53]. Diamond films were traditionally synthesized by conventional chemical vapor deposition (CVD) using  $H_2/CH_4$ , requiring high process temperature of above 700 °C [54]. MPECVD of UNCD was achieved at 400 °C because of both the change of chemistry from  $H_2/CH_4$  to Ar-rich/ $CH_4$  plasma and reduction of activation energy from 20 kcal/mol to 6 kcal/mol [50, 54, 55]. The crystal orientation and surface morphology can be tuned by controlling nucleation and MPECVD parameters [53]. The usage of MPECVD greatly reduced the synthesis temperature from 700 °C to 400 °C, resulting in a reasonable temperature range that is compatible with most silicon-based devices. However, most of implantable devices contain polymeric materials other than silicon. The ideal process temperature would not exceed 200 °C.

Diamond-like carbon is an alternative with relatively low deposition compared with UNCD. It has similar properties compared with UNCD, including low friction, low wear, chemical inertness, and high biocompatibility [56-58]. DLC have been extensively used for coating biomedical implants [59-61], including orthopedic (e.g., in artificial hips,



knees, and joints) applications, and vascular applications (e.g., in stents, heart pumps, and heart valves) [62, 63].

DLC can be deposited at room temperature or higher [59, 64], depending on the deposition method. Methods that have been used to deposit DLC includes direct ion beam deposition [65], pulse laser deposition [66], filtered cathodic deposition, sputtering [67], and plasma enhance chemical vapor deposition (PECVD) [60]. Different deposition methods and parameters can greatly affect the quality and properties of the DLC film.

Despite wide applications in implantable devices, one of the major issues for DLC is its adhesion to the substrate [63]. Adhesion-promoting interlayers have been developed to address this issue, including Ti, Si, Cr, Si-DLC, etc. [63]. However, dissolution of the interlayer was observed, which caused the delamination of DLC and therefore significantly undermined the coating performance [68].

#### 2.4.3 Silicon Carbide

Silicon carbide can be grown as single crystalline *c*-SiC, polycrystalline *p*-SiC, and amorphous *α*-SiC. Both *c*-SiC and *p*-SiC require a process temperature over 600 °C [69], which is not compatible with most implantable devices.

Amorphous SiC has low dielectric constant (4.2-4.9) and low water intake [70, 71]. It also exhibits chemical inertness due to the strong Si-C chemical bonds [72]. A-SiC<sub>x</sub>:H has been applied in fields such as optoelectronics [73], solar cell technology [74], and surface passivation [74-76]. In addition, the usage of a- SiC<sub>x</sub>:H as biomedical encapsulation material has been reported to improve the hemocompatibility of implanted

stents [77, 78], and reduce thrombosis and restenosis rate after angioplasty [79]. It has also been investigated as insulation for neural interfaces [41, 43].

A few low-temperature deposition techniques have been developed to grow a-SiC in order to meet the temperature requirements for a variety of applications. Those techniques include pulsed laser deposition (PLD) [80, 81], sputter deposition [82-84], and plasma-enhanced chemical vapor deposition [41, 43, 85, 86].

PLD and sputtering deposition both have flux directionalities during the deposition process, leading to nonuniform thickness of the coated film. Moreover, sputtered films tend to have structural defects (pin-holes), which is not acceptable for coating of implantable devices. High compressive stress induced by PLD requires high annealing temperature ( $\sim 600$  °C) to relieve the stress [87].

PECVD is the most commonly used method for depositing SiC at low temperature [43, 88]. Both the plasma and thermal energy are used to dissociate gas precursors and create free radicals for chemical reaction. Therefore, the temperature of PECVD required for dissociating precursors can be significantly lowered than for conventional CVD using thermal energy only [88]. Incorporation of hydrogen into SiC during the growth is almost unavoidable due to the high hydrogen concentration in the precursor.

## 2.5 Polymeric Materials for Encapsulating

### Implantable Devices

Polytetrafluoroethylene (PTFE), best known as Teflon, a trademark of DuPont, is a bioinert, biostable, and low friction material, and has a chemical formula of  $(C_2F_4)_n$ . PTFE does not dissolve *in vivo* [89]. The good biocompatibility of PTFE may be partial

due to its bioinertness and hydrophobic surfaces that minimize foreign-body recognition *in vivo* [89]. PTFE has also been used as a material for vascular grafts [90]. Plasma treatment has been used to improve the cell adhesion of endothelial cell onto PTFE vascular grafts by adding amide functional groups [90]. The surface hydrophilicity, which is favorable for cell adhesion, was also improved by this technique.

PTFE is generally applied by either spraying or dipping coating [91]. It is almost impossible to obtain a uniform coating film using liquid-phase techniques for implantable devices with complex 3-D geometries. Alternative deposition techniques have been investigated to gain uniform PTFE films.

Plasma-enhanced chemical vapor deposition (PECVD) [92] and hot-wire chemical vapor deposition (HWCVD) [93] have been proposed as potential techniques to conformally deposit fluorocarbons that have similar chemical formulas to PTFE. The PECVD deposited PTFE has two major drawbacks. First, it contains byproducts like  $\text{CF}_3$  and  $\text{CF}$  other than  $\text{CF}_2$  groups. Additionally, free radicals were present in PECVD PTFE films, which can potentially react with oxygen and water over time and thus may undermine the coating performance of the film [92, 94].

HWCVD is proposed to overcome the aforementioned drawbacks by minimizing the incorporation of byproducts and free radicals in the deposited films during PECVD [94]. Initiated chemical vapor deposition (iCVD) is one type of HWCVD, which utilizes chemical initiators to initiate polymerization reaction. The usage of initiator enables further decreasing the filament temperature required to dissociate the precursors. Consequently, iCVD requires lower power and has higher deposition rate compared with conventional HWCVD. HWCVD or iCVD fluorocarbon films have better fluorine to

carbon ratio (close to 2) than films deposited by PECVD due to higher percentage of  $\text{CF}_2$  and lower byproduct incorporation.

Silicone has been widely used for biomedical implantable devices [95]. The traditional challenge of applying silicone conformally was overcome by the iCVD technique. Researchers have demonstrated the possibility of conformally depositing siloxane by iCVD [96, 97]. In addition, iCVD siloxane has been used as effective encapsulation for neural probes [98]. One major drawback of silicone coating is that it has relatively higher water vapor transmission rate (WVTR) than polymers like PTFE and Parylene [99]. The large volume of penetrated moisture due to high WVTR can nucleate around interface contaminants to form electrolytes, which corrode the device and significantly reduce its lifetime [100].

Polyimide is another widely used polymeric material for implantable devices. Polyimide has demonstrated its biocompatibility in neural interface devices and retina implants [101-104]. However, it is very challenging to obtain a conformal polyimide coating by the commonly used spin-casting technique. Additionally, polyimide has high water absorption and water vapor transmission rate (WVTR) [49, 99], which can undermine the long-term insulation performance of polyimide. Table 2.1 shows WVTR of commonly used polymers for encapsulating biomedical implantable devices and atomic layer deposited  $\text{Al}_2\text{O}_3$ .

## 2.6 Atomic Layer Deposited $\text{Al}_2\text{O}_3$

Atomic layer deposited (ALD)  $\text{Al}_2\text{O}_3$  is one of the two materials used in this work. Alumina ( $\text{Al}_2\text{O}_3$ ) is known for its high hardness, high abrasion resistance, and

bioinertness [105]. It has demonstrated good biocompatibility *in vivo* in forms of both bulk alumina and ALD alumina thin film [106, 107]. Alumina has been widely used as a bioceramic for dental and bone implants [34, 108-110]. It is also used as a substrate material for floating microelectrode arrays for neural recording [111]. Retina implants utilized alumina as a coating material to insulate the device from physiological environment [112]. What differentiates alumina from other materials is its extremely low water vapor transmission rate (WVTR). Atomic layer deposited (ALD) alumina has been demonstrated as an excellent moisture barrier with WVTR as low as in the order of  $\sim 10^{-10}$  g·mm/m<sup>2</sup>·day [113-116], to prevent the degradation of extremely moisture-sensitive organic light emitting diodes (OLEDs). Another major application of alumina is the passivation of solar cells for higher efficiency [117, 118]. The success of applying alumina for solar cell and OLED passivation is mostly attributed to the ALD process, which generates conformal, dense, and pin-hole free films. Different from bulk Al<sub>2</sub>O<sub>3</sub>, ALD Al<sub>2</sub>O<sub>3</sub> can be easily corroded by liquid water [119], due to the incorporation of hydrogen in the form of OH groups in the film [120, 121].

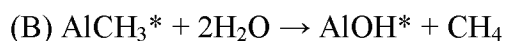
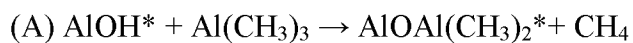
### 2.6.1 The Chemistry of ALD Al<sub>2</sub>O<sub>3</sub>

ALD is able to achieve atomic layer control and conformal deposition using sequential, self-limiting surface chemical reactions [122]. ALD was proposed back to the 1960s and started to gain popularity in the beginning of the 1990s, driving its potential application in scaling down microelectronic devices. A typically ALD cycle is composed of four steps [123]:

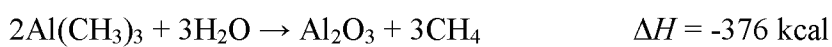
- (a) A self-limiting chemical reaction of the first precursor (precursor A) with the absorbed second precursor from the previous cycle.
- (b) A purge of inert gas to remove excess precursors and byproducts from the chamber.
- (c) A self-limiting reaction of the second precursor (precursor B) with the absorbed precursor A.
- (d) A purge of inert gas.

The growth of material is achieved by repeating of the aforementioned four steps. The characteristics of self-limiting surface reaction lead to the ALD as a surface-controlled process, where parameters other than precursors and temperature have little or no effect on the growth of the film. When sufficient time between precursors is present, gas phase transport of precursors into tight gaps with high aspect ratio is possible, contributing to the very high degree of conformality. Therefore, films grown by ALD are extremely conformal, uniform, and reproducible.

The first report of thermal ALD  $\text{Al}_2\text{O}_3$  using trimethylaluminum (TMA) and  $\text{H}_2\text{O}$  as precursors was back in the late 1980s and early 1990s [124, 125]. The surface chemistry of ALD  $\text{Al}_2\text{O}_3$  using  $\text{H}_2\text{O}$  as oxidant can be described as [122, 126, 127]



where the asterisks denote the surface species. The growth of  $\text{Al}_2\text{O}_3$  happens during the alternating exposures to TMA and  $\text{H}_2\text{O}$ . The overall chemical reaction of ALD  $\text{Al}_2\text{O}_3$  is [122]



The formation of a strong Al-O covalent bond makes the reaction very efficient.

ALD is very similar to chemical vapor deposition (CVD) based on binary reaction format of  $A + B \rightarrow C + \text{byproduct}$ . The distinction between ALD and binary reaction-based CVD is the time of the precursor presence. For CVD, reactants A and B are present simultaneously on the surface and it grows films continuously. On the other hand, reactants A and B are timely separated in the ALD process and only one reactant is present at a time in the form of a monolayer. The growth of the film is more stepwise. It is the separation of precursors in time domain which ensures that the ALD only happens at the surface.

### 2.6.2 The Growth Rate of ALD $\text{Al}_2\text{O}_3$

The plasma-enhanced ALD reaction for  $\text{Al}_2\text{O}_3$  used in this work is illustrated schematically in Fig 2.5. The growth of ALD  $\text{Al}_2\text{O}_3$  is extremely linear with a rate of about 1.1 Å per cycle due to the highly repeatable self-limiting surface chemistry. The deposition rate of ALD  $\text{Al}_2\text{O}_3$  is distinct from the monolayer thickness of  $\text{Al}_2\text{O}_3$ , which is estimated to be 3.8 Å [122]. The surface chemistry, surface species, and precursor coverage limits the possibility of depositing a full monolayer of  $\text{Al}_2\text{O}_3$ .

The deposition rate of ALD  $\text{Al}_2\text{O}_3$  is temperature dependent because the chemical reaction during the ALD growth requires thermal energy to generate free radicals. Higher process temperature leads to the reduction of time needed for each cycle. However, studies have shown that the growth per cycle decreases progressively as temperature increases from 177 to 300 °C, due to less coverage of  $\text{AlOH}$  and  $\text{AlCH}_3$  surface species at

higher temperatures [128, 129]. A typical measurement of ALD  $\text{Al}_2\text{O}_3$  growth with quartz crystal microbalance (QCM) is shown in Fig 2.6.

### 2.6.3 Plasma-enhanced ALD

Other than the widely used  $\text{H}_2\text{O}$  oxidant during ALD process, other oxidants like ozone and oxygen have also started to gain popularity to obtain better dielectric properties and lower leakage current [130-133]. Oxidants like ozone and oxygen make chemical reaction much less likely or even impossible by using only thermal energy due to the lack of free radicals. By creating free-radicals using plasma, plasma-enhanced ALD can deposit  $\text{Al}_2\text{O}_3$  using TMA and  $\text{O}_2$  at temperature as low as room temperature [133]. The low temperature is extremely help for coating of thermal fragile substrate like polymers or microsystems with underfiller materials.

The plasma-enhanced ALD  $\text{Al}_2\text{O}_3$  films exhibit higher electrical breakdown voltage and higher dielectric constant, which are ascribed to the higher density of the deposited films than thermal ALD  $\text{Al}_2\text{O}_3$  films [134]. The improved electrical properties lead to better passivation of silicon substrate [135, 136]. In addition, plasma-enhanced ALD reduces the hydrogen incorporation in  $\text{Al}_2\text{O}_3$  films compared with thermal ALD  $\text{Al}_2\text{O}_3$  films [136, 137], thus improving the film quality and reduce leakage current [138].

## 2.7 Parylene

Poly-para-xylene (Parylene) was first discovered by Szwarc in 1947 using chemical vapor deposition (CVD). Parylene was deposited using para-xylene solvent as precursor. This method had very low yield and high impurities. The deposition process was



improved by Gorham from Union Carbide using vacuum pyrolysis of di-para-xylene precursors [139, 140]. The room temperature deposition process and good chemical and physical properties make Parylene very attractive for many electronics and biomedical applications [21, 141-144].

### 2.7.1 Parylene Variants

The chemical structure of the Parylene monomers is composed of an aromatic group with methylene groups attached at the para positions. Parylene variants are created by replacing the aromatic or aliphatic hydrogen atoms with other side groups. There are three most common variants: Parylene C, Parylene D, and Parylene N. Fig 2.7 shows the chemical structure of those three major Parylene variants and Table 2.2 presents the their properties.

Parylene N and Parylene C have been categorized as USP class VI polymers [145], which requires demonstration of biocompatibility and indiscernible toxicity in the systemic injection test, intracutaneous test, and implantation test. In addition, Parylene C has lower water vapor transmission rate compared with Parylene N (0.4 vs 5.4  $\text{g}\cdot\text{mm}/\text{m}^2\cdot\text{day}$ ) [99]. Parylene C is widely used for biomedical applications.

### 2.7.2 Parylene Deposition

Parylene is deposited by chemical vapor deposition (CVD). The deposition process is composed of three major steps: vaporization, pyrolysis, and polymerization. The chemical reaction of each step is described in Fig 2.8. Di-para-xylene dimer is used as

precursor and is vaporized and then pyrolyzed into free radical monomers, which then undergo polymerization to form poly-para-xylene (Parylene) at lower temperature.

The Parylene deposition system is designed according to the aforementioned three-step polymerization process, composed of vaporization furnace, pyrolysis furnace, and deposition chamber. Additionally, a cold trap and a vacuum pump are included in the system to absorb the unreacted monomer and maintain the required low pressure (around 10 mTorr for base pressure) during the deposition, respectively. Fig 2.9 is a schematic view of the deposition system.

#### 2.7.2.1 Vaporization

The dimer sublimation rate varies with vaporization temperature, affecting the morphology and crystallinity of deposited Parylene [146, 147]. The threshold temperature for dimer sublimation is about 60 °C and sublimation rate increases as the sublimation temperature rises. A typical vaporization temperature is around 130 °C to generate a sublimation rate sustaining sufficient vapor pressure and deposition rate. Other than temperature, the sublimation rate is also dependent on the exposed surface of the dimer (i.e., kinetics factors). The surface area of exposed dimer decreases as a function of sublimation time; therefore, a slight increase in sublimation temperature is needed to compensate the sublimation rate drop and maintain a constant vapor pressure. A constant vapor pressure helps to obtain Parylene films with consistent properties during the whole deposition process.

### 2.7.2.2 Pyrolysis Process

Pyrolysis is the process in which heat is used to dissociate dimers into reactive monomers, which participate in the polymerization process at lower deposition temperature. The required temperature for fully converting dimers into monomers has been reported to be 565 °C [148]. The suggested pyrolysis temperature setting is 670 °C from the vendor and various reports [140].

Complete dissociation of dimers into monomers is needed to reduce the presence of dimer in the deposited Parylene film. High sublimation rate has been reported to reduce the residence time of dimer in the pyrolysis chamber, leading to incomplete dissociation of dimers. The “un-cracked” dimers contained in the reactive monomers presents in the deposited Parylene film without any chemical polymerization process [147]. The short residence time of dimer vapor in the pyrolysis furnace can be compensated by increase the length of the pyrolysis furnace.

### 2.7.2.3 Polymerization

The polymerization process is achieved through free radicals and it happens at temperature lower than 80 °C and typically uses room temperature. The low-temperature deposition process makes it very attractive to coat materials and devices that require a low thermal budget. The essence of the growth of Parylene film is a free radical chemical reaction process. A vapor-deposition polymerization model and surface roughening kinetics have been proposed [149, 150]. The growth of the Parylene film is achieved by two chemical reactions: initiation, in which new carbon chains are formed, and propagation, in which existing carbon chains are extended into higher molecular weight.

Unlike physical vapor deposition, reaction only occurs at the end of the polymer chain instead of many available sites during the vapor deposition polymerization. Surface diffusion, intermolecular interaction, and chain relaxation can occur during the deposition [149].

Pressure, temperature, and deposition rate can affect the polymerization process and thus the film properties. The deposition pressure has been suggested to be lower than 100 mTorr to obtain high-quality films [151, 152]. It is also suggested that low-temperature polymerization process increases the Parylene growth rate and chain length [151]. Longer chain length leads to better thermal stability of the Parylene film.

### 2.7.3 Parylene Adhesion

Parylene is known to have poor adhesion to substrates like polyimide, silicon, glass, and metallic materials. Therefore, surface modification is necessary before Parylene deposition to improve the adhesion. There are mainly three approaches have been proposed to enhance the adhesion:

- (a) Using plasma to remove contaminants and clean the surface [153, 154].
- (b) Using plasma-enhanced chemical vapor deposition to deposit a thin layer of polymer as adhesion promoter [154, 155].
- (c) Using gas or liquid phase silanization process to add an adhesion layer with functional groups to form chemical bonds with both substrate and Parylene [156].

The thin film deposition method has been reported to be more effective in improving adhesion than the plasma cleaning process for a variety of substrates [154]. However, the requirement for additional PECVD system adds more complications.

Silanization process is less complicated and inexpensive compared with the plasma-based techniques for improving adhesion. It utilizes functional groups from organic-silane to provide covalent linkage between substrate and Parylene. Among many potential coupling agents [157], Silquest A-174® silane (Gamma-Methacryloxypropyltrimethoxysilane) is the most common option for improving Parylene adhesion.

Silquest A-174® silane, patented by Union Carbide, has a simplified form of X-R-SiY<sub>3</sub>. Fig 2.10 shows the chemical structure of Silquest A-174® silane. The Y group is a hydrolysable functional group which can form silanol intermediates when reacting with water, which further form covalent bond with substrate. The X group is a vinyl group that can form covalent bond with reactive monomers during the Parylene deposition process.

## 2.8 Tip Deinsulation

Selective removing of encapsulation materials is required to expose the active sites for interacting with physiological environment. Primary methods of selective etching include reactive ion etching and laser ablation in the manner that keeps the encapsulation of the rest of the device intact.

Removal of Parylene by wet etching is challenging due to its chemical inertness. Early era removal of Parylene includes burning out of Parylene by high temperature and electrical breakdown by high-voltage arc [143]. The high temperature introduced by the excessive heat could break down the nearby insulation material and damage the active electronics. The high-voltage arc method led to formation of fractures in Parylene near the deinsulation site. In addition, it is difficult to precisely control the deinsulated area,

which is directly related to the impedance and therefore critical to the performance of the device.

Reactive ion etching (RIE) was developed as an alternative dry etching method to remove Parylene. An oxygen plasma is used to selectively remove Parylene C on the tip of Utah Electrode Array (UEA) [21, 158]. Other groups have also used reactive ion etching to etch Parylene [159, 160]. Anisotropic etching is often preferred in MEMS and integrated circuit (IC) fabrication for precise control; isotropic etching is more suitable for substrate cleaning. For deinsulation of biomedical devices like neural interfaces with complex three-dimensional geometry [21], isotropic plasma etching is desired to identically remove the encapsulation film from all directions while maintaining the original geometries. Therefore, inductively couple plasma is preferred over capacitively coupled plasma due to its more isotropic characteristic.

Masking is required to define the etching area during the plasma etching. Thin aluminum foil has been adopted as a mask layer for Parylene etching [21]. The major drawback of this masking method is the lack of control in exposure area, which leads to big variation in tip impedance. Alternatively, photoresist has been reported as an etching mask for three-dimensional electrodes [161, 162]. However, the usage of photoresist could affect the surface hydrophobicity [163] and therefore the biocompatibility of Parylene film. In addition, applying photoresist to biomedical devices with complex geometry would be very challenging.

In addition to plasma etching, laser ablation has also been demonstrated to effectively remove Parylene [164-166]. The biggest advantage of laser ablation is that no mask is required, which is extremely beneficial for biomedical devices with complex

geometries making them difficult to mask. One of the concerns with laser ablation is the damage to the film/material underneath Parylene [166, 167]. This effect can often be eliminated or minimized by manipulating the power and pulse number of the laser [166]. Another drawback is the carbon redeposition around the ablation spot [165, 168]. A brief oxygen plasma treatment can be used to clean the carbon residual and generate electrode sites that have performance similar to RIE deinsulated sites.

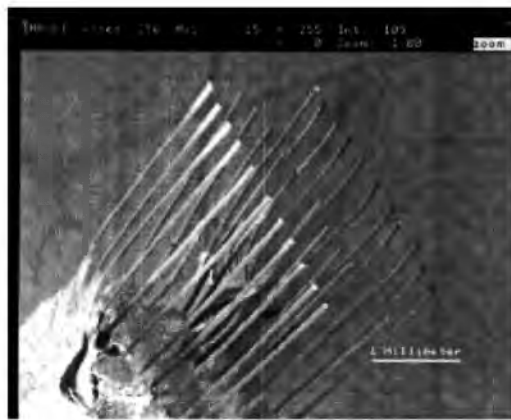


Fig 2.1 Microwire arrays made by Williams *et al.*, 22 tungsten microwires were connected to the back-end connector [reprinted with permission from Elsevier, © 1999, Elsevier].

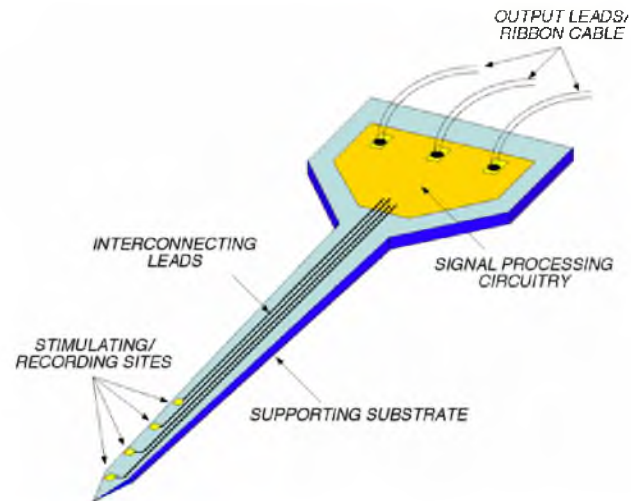


Fig 2.2 Examples of the 2-D Michigan microelectrode array with multiple recording/stimulation sites [reprinted with permission from IEEE © 2008 IEEE].

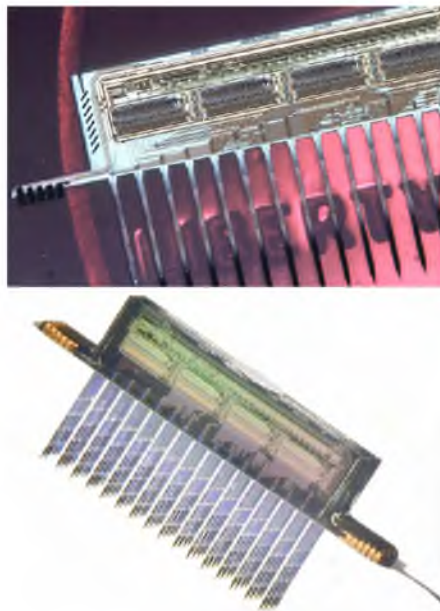


Fig 2.3 3-D Michigan array. At the top, a 64-site 8-channel Michigan array with CMOS electronics; at the bottom, four probes are assembled onto a platform to form a 256-site 32-channel array [reprinted with permission from IEEE © 2008 IEEE].



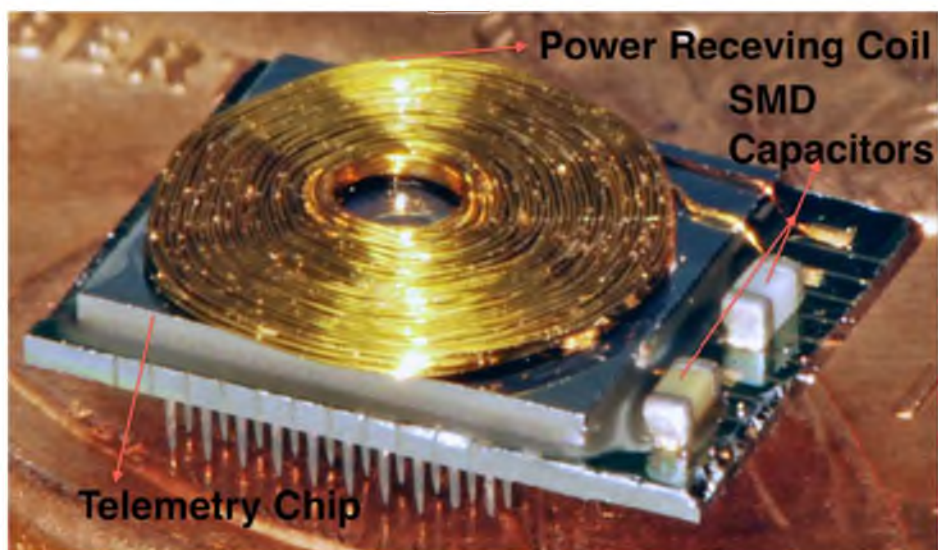


Fig 2.4 Fully integrated wireless neural interfaces based on UEA. An ASIC chip was flip-chip bonded at the backside of UEA. Gold coil was wire-bonded and SMD capacitors were soldered for inductive powering and wireless communication.

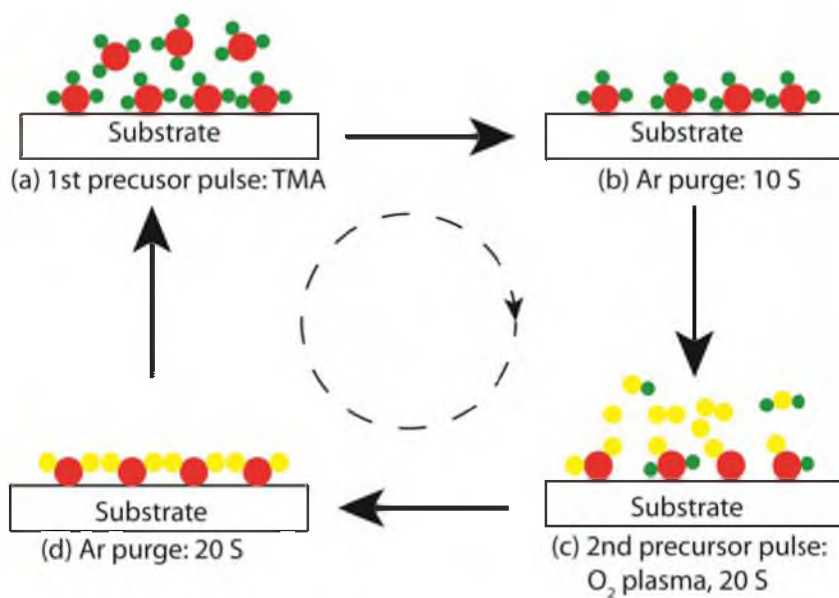


Fig 2.5 Schematic representation of ALD  $\text{Al}_2\text{O}_3$  using self-limiting surface chemistry and an A (TMA) +B (oxygen plasma) binary reaction sequence.

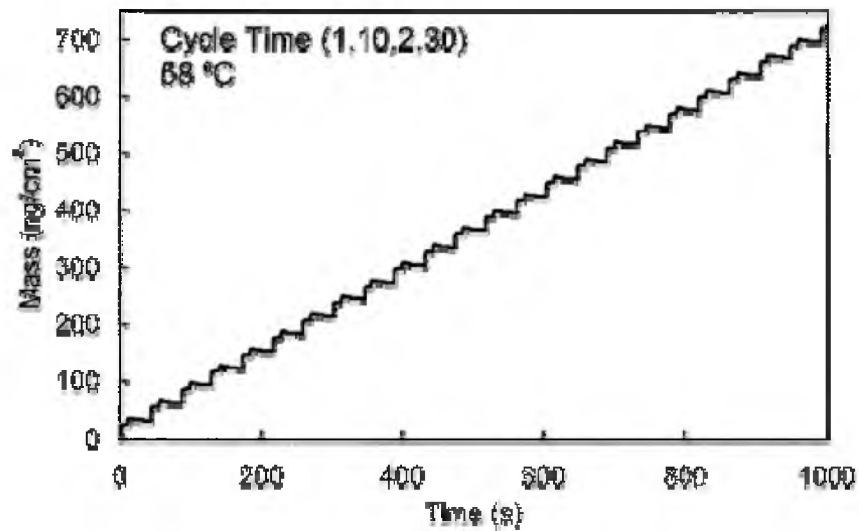


Fig 2.6 QCM measurements for Al<sub>2</sub>O<sub>3</sub> ALD at 58 °C showing the linear growth of the Al<sub>2</sub>O<sub>3</sub> ALD film over many reaction cycles. The average Al<sub>2</sub>O<sub>3</sub> mass gain per ALD cycle is 30 ng/cm<sup>2</sup>. [Reprinted with permission from Chemistry of Materials M. Groner, F. Fabreguette, J. Elam, and S. George, "Low-temperature Al<sub>2</sub>O<sub>3</sub> atomic layer deposition," *Chemistry of Materials*, vol. 16, pp. 639-645. © 2004, American Chemical Society].

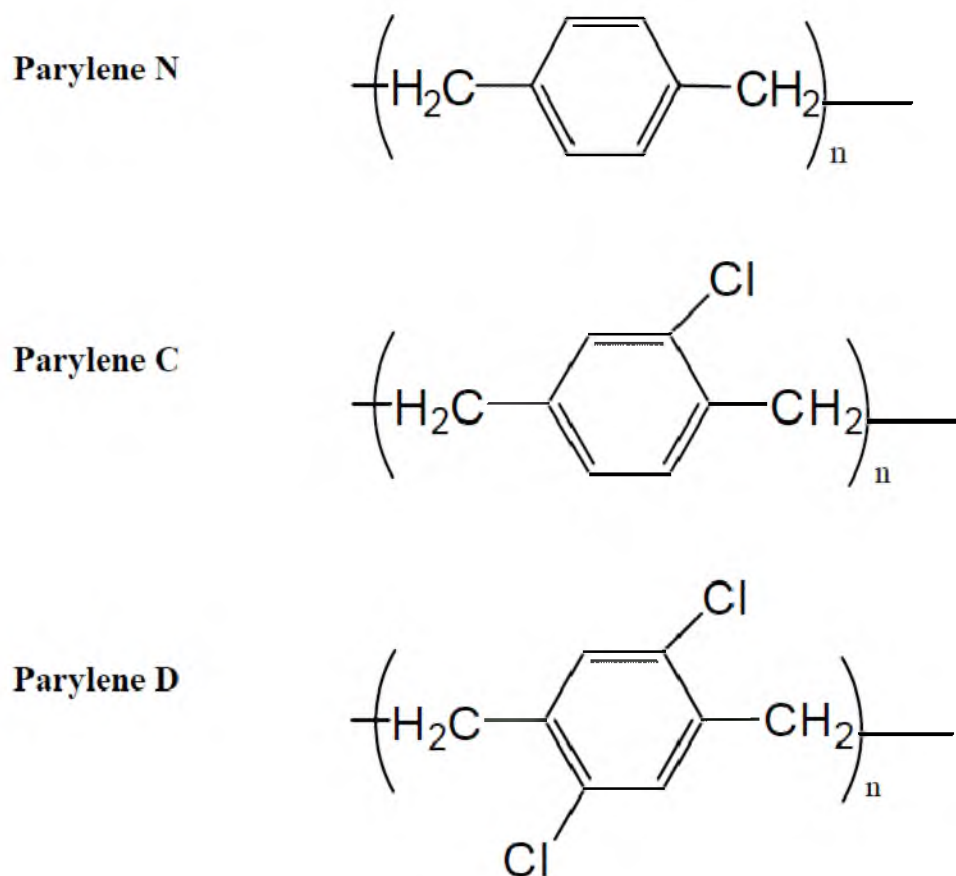


Fig 2.7 Chemical structures of Parylene-N,-C and -D. [reprinted from J. B. Fortin and T. M. Lu, *Chemical vapor deposition polymerization: the growth and properties of Parylene thin films*, Springer, 2004, with permission from Springer].

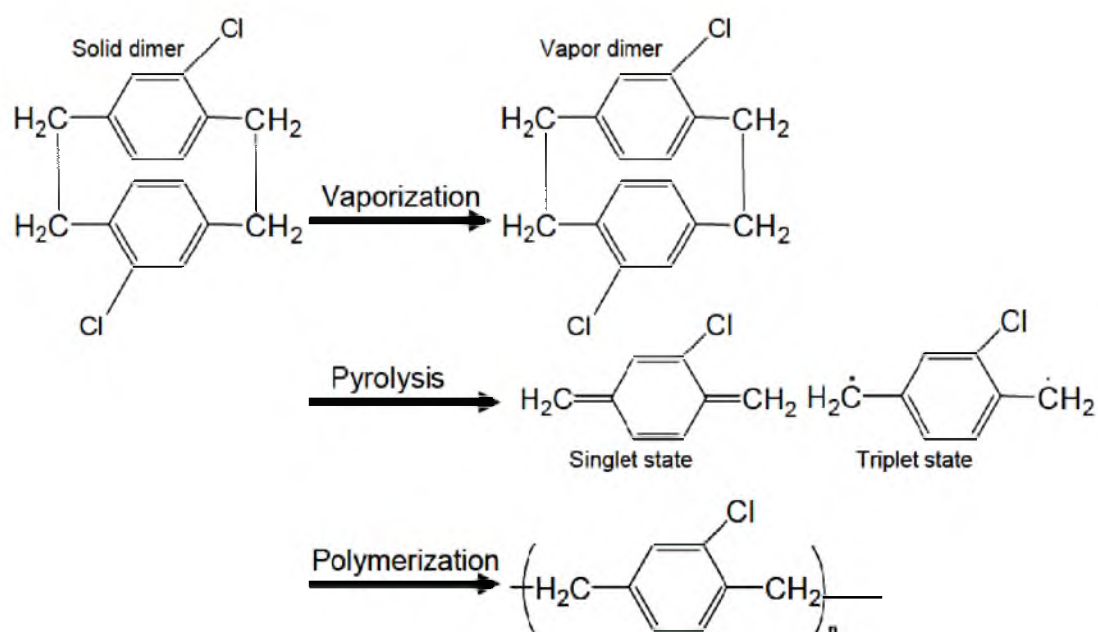


Fig 2.8 The chemical vapor deposition process for Parylene C. The dimer is first vaporized and then dissociated into monomers with free radicals. The monomers undergo polymerization process when cooling down.

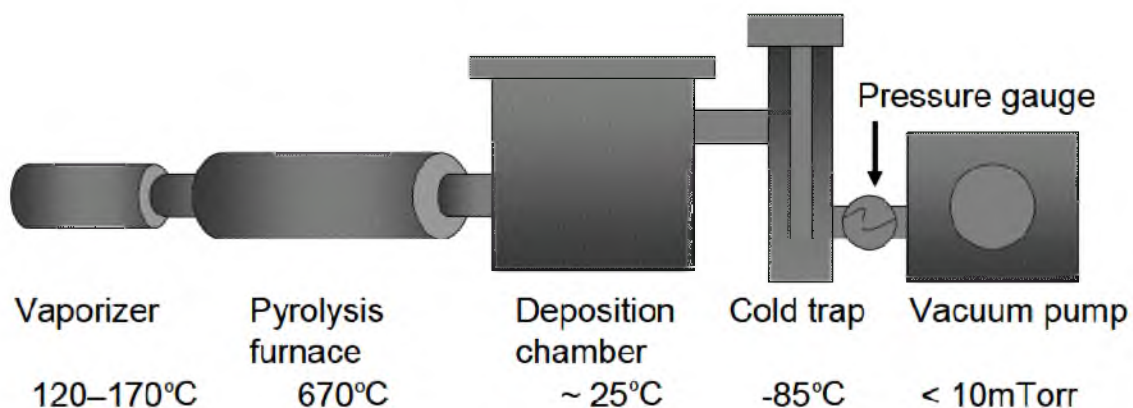


Fig 2.9 Schematic view of a Parylene deposition system. The system is consisted of five major components: a vaporizer, a pyrolysis furnace, a deposition chamber, a cold trap, and a vacuum pump.

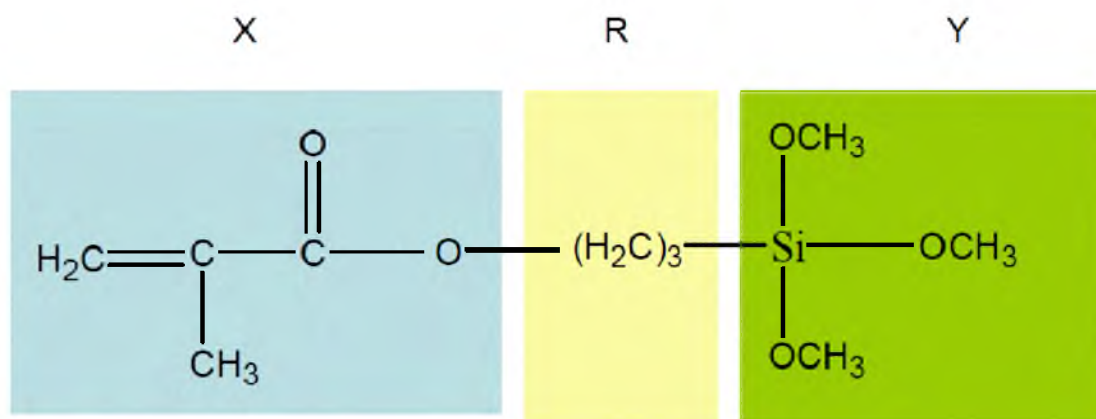


Fig 2.10 The chemical structure of Silquest A-174 ® silane. The functional group X can form covalent bonds with Parylene monomer, and Y (right) can be hydrolyzed and form covalent bonds with substrates.

Table 2.1 Water vapor transmission rate (WVTR) for polymers and atomic layer deposited  $\text{Al}_2\text{O}_3$ .

Material	WVTR ( $\text{g}\cdot\text{mm}/\text{m}^2\cdot\text{day}$ )
Epoxy	0.5-1
Polyimide (DuPont)	1.4
Silicone, RTV	46.8
PTFE (DuPont)	0.1
Parylene C (Specialty Coating Systems)	0.4
Parylene N (Specialty Coating Systems)	5.4
Atomic Layer Deposited Alumina	$\sim 10^{-10}$

Table 2.2 Material properties for Parylene N, C and D [reprinted with permission from J.

B. Fortin and T. M. Lu, *Chemical vapor deposition polymerization*, © 2004 Springer].

Property		Parylene N	Parylene C	Parylene D
<b>Electrical property</b>				
Dielectric Constant	1 MHz	2.65	2.95	2.8
	1 KHz	2.65	3.10	--
	60 Hz	2.65	3.15	--
Dissipation factor	1 MHz	0.0006	0.013	0.002
	1 KHz	0.0002	0.019	--
	60 Hz	0.0002	0.020	--
Dielectric strength (MV/cm)		300	185-220	215
Volume resistivity (23°C, 50% RH)		$1.4 \times 10^{17}$	$8.8 \times 10^{16}$	$2 \times 10^{16}$
Surface resistivity (23°C, 50% RH)		$1 \times 10^{13}$	$1 \times 10^{14}$	$5 \times 10^{16}$
<b>Physical Property</b>				
Melting point (°C)		420	290	380
Glass transition (°C)		13-80	35-80	110
Linear coefficient of expansion ( $25^\circ\text{C} \times 10^{-5}, \text{K}^{-1}$ )		6.9	3.5	--
Heat capacity (25°C, J/gK)		1.3	3.5	--
Thermal conductivity (25°C, kW/mK)		1.3	1.0	--
Density (g/cm <sup>3</sup> )		1.110	1.289	1.418
Refractive index		1.661	1.639	1.669
<b>Mechanical Property</b>				
Tensile modulus (Gpa)		2.4	3.2	2.8
Tensile strength (Mpa)		45	70	75
Yield strength (Mpa)		32	55	60
Elongation to break (%)		30	200	10
Yield elongation (%)		2.5	2.9	--
Static coefficient of friction		0.25	0.29	0.35
Dynamic coefficient of friction		0.25	0.29	0.31
Hardness (Gpa)		0.6 (least)	Moderate	--
<b>Moisture resistant</b>				
Water absorption (%) after 24 hrs		0.1	0.1	0.1
<b>Coating performance</b>				
Crevice penetration		Best	Good	Least
Molecular activity		Highest	Good	Least
Coating uniformity		Best	Good	--
Thickness control		Good	Best	--
Coating speed		Lowest	Moderate	Highest

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## CHAPTER 3

### PLASMA-ASSISTED ATOMIC LAYER DEPOSITION OF $\text{Al}_2\text{O}_3$ AND PARYLENE C BI-LAYER ENCAPSULATION FOR CHRONIC IMPLANTABLE ELECTRONICS<sup>1</sup>

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## Plasma-assisted atomic layer deposition of $\text{Al}_2\text{O}_3$ and parylene C bi-layer encapsulation for chronic implantable electronics

Xianzong Xie,<sup>1</sup> Loren Rieth,<sup>1</sup> Srinivas Merugu,<sup>1</sup> Prashant Tathireddy,<sup>1</sup> and Florian Solzbacher<sup>1,2</sup>

<sup>1</sup>Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, Utah 84112, USA

<sup>2</sup>Department of Bioengineering, University of Utah, Salt Lake City, Utah 84112, USA

(Received 11 July 2012; accepted 14 August 2012; published online 27 August 2012)

Encapsulation of biomedical implants with complex three dimensional geometries is one of the greatest challenges achieving long-term functionality and stability. This report presents an encapsulation scheme that combines  $\text{Al}_2\text{O}_3$  by atomic layer deposition with parylene C for implantable electronic systems. The  $\text{Al}_2\text{O}_3$ -parylene C bi-layer was used to encapsulate interdigitated electrodes, which were tested *in vitro* by soak testing in phosphate buffered saline solution at body temperature (37 °C) and elevated temperatures (57 °C and 67 °C) for accelerated lifetime testing up to 5 months. Leakage current and electrochemical impedance spectroscopy were measured for evaluating the integrity and insulation performance of the coating. Leakage current was stably about 15 pA at 5 V dc, and impedance was constantly about 3.5 M $\Omega$  at 1 kHz by using electrochemical impedance spectroscopy for samples under 67 °C about 5 months (approximately equivalent to 40 months at 37 °C). Alumina and parylene coating lasted at least 3 times longer than parylene coated samples tested at 80 °C. The excellent insulation performance of the encapsulation shows its potential usefulness for chronic implants. © 2012 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4748322>]

There continues to be a strong interest in developing biomedical implantable devices, such as cochlear implants,<sup>1</sup> diaphragm pacing systems,<sup>2</sup> and deep brain stimulators for treating diseases such as hearing loss, respiratory failure, and Parkinson's.<sup>3</sup> Neuroprosthetics systems require chronic implantation of neural interfaces able to perform for years or decades to reduce surgical risks from follow-up surgeries and generate levels of efficacy that justifies the risks associated with the implants. The device has to be protected from the harsh body environment, which allows device to perform its intended use. Therefore, encapsulation of implantable device is critical to its functionality, stability, and longevity. Wireless systems have been widely developed because they typically have less foreign body response than tethered (wired) devices.<sup>4</sup> Soft encapsulation has been preferred for implantable devices over hermetic encapsulation based on metal canisters due to limited space and interference with telemetry communication, especially for wireless systems. The encapsulation has to be biocompatible, conformal, and highly resistive and have a low dielectric constant.<sup>5</sup> Parylene C (Refs. 6–8) has been widely used as encapsulation material for different kinds of implantable devices, based on its low water absorption rate of 0.1% for 24 h,<sup>9</sup> low dielectric constant of 3.15 at 60 Hz,<sup>9</sup> USP Class VI biocompatibility, and chemical inertness. Parylene C is also an excellent ion barrier,<sup>10</sup> which makes it very attractive for implantable devices. Failure of parylene C encapsulation has been reported<sup>11</sup> due to moisture diffusion and interface contamination. Reactive parylene has been developed by adding functional group to improve the adhesion and short-term insulation performance<sup>6</sup>; however, this does not keep water moisture from penetration. In order to prevent this from happening, moisture has to be isolated from the interface with the coated devices.

Otherwise, moisture will condense around hygroscopic interface contaminants, causing devices failure.

Atomic layer deposited (ALD)  $\text{Al}_2\text{O}_3$  has been demonstrated as an excellent moisture barrier<sup>12,13</sup> with water vapor transmission rate (WVTR) of  $10^{-6}$  g/m<sup>2</sup>·day, for preventing degradation of extremely moisture-sensitive organic light emitting diodes (OLEDs). ALD  $\text{Al}_2\text{O}_3$  is superior compared with films generated by other deposition techniques such as sputtered  $\text{Al}_2\text{O}_3$  as a moisture barrier<sup>13,14</sup> because it is highly conformal and pin-hole free. Liquid water is known to corrode  $\text{Al}_2\text{O}_3$  (Ref. 15); therefore,  $\text{Al}_2\text{O}_3$  film alone is not suitable for encapsulation of biomedical implants exposed directly to the body environment. The idea of combining  $\text{Al}_2\text{O}_3$  and parylene is based on the concept that  $\text{Al}_2\text{O}_3$  works as an inner moisture barrier and parylene as external barrier to ions and prevents contact of  $\text{Al}_2\text{O}_3$  with liquid water, and to inhibit the transport of reactants/products involved with corrosion of the  $\text{Al}_2\text{O}_3$  layer.

In this letter, we are reporting the *in vitro* performance of the bi-layer encapsulation scheme based on interdigitated electrodes (IDEs) described below. IDEs coated with 52-nm of plasma-assisted (PA) ALD  $\text{Al}_2\text{O}_3$  and 6  $\mu\text{m}$  of parylene C had leakage currents of 15 pA and impedance of 3.5 M $\Omega$  at 1 kHz after being soaked in 1 $\times$  phosphate buffered saline (PBS) at 37 °C for approximate 5 months without any obvious change. Accelerated soaking tests were also performed at elevated temperature (57 °C, 67 °C, and 80 °C). 80 °C is considered a high temperature for soak testing of polymer materials and might activate new failure modes, compromising the predictive power of those measurements. The measurements are quite useful as a worst-case scenario, since activation of additional failure modes would likely only decrease the device lifetime. Electrochemical impedance

spectroscopy (EIS) and chronoamperometry were performed by Gamry potentiostat (Gamry instruments) to monitor the performance of the encapsulation. IDE test structures were fabricated using standard lift-off lithographic techniques on 500- $\mu\text{m}$  thick fused silica substrate. Electrodes were 130  $\mu\text{m}$  wide with the same spacing in between. The electrodes were composed of Ti(100 nm)/Pt(150 nm)/Au(150 nm) sequentially to match the metallization used for wireless version of Utah Electrode Arrays (UEAs),<sup>16</sup> which are comprised of 10 by 10 silicon-based electrodes with Ti/Pt/Au backside metal for flip-chip bonding. The IDEs were then annealed at 375 °C in forming gas (98% of Ar and 2% of H<sub>2</sub>) for 45 min. Two lead wires were soldered to two bond pads on IDEs for electrical contact (Fig. 1). Thin Al<sub>2</sub>O<sub>3</sub> films were deposited using plasma assisted atomic layer deposition (PAALD) by sequentially exposing IDEs to trimethylaluminum (TMA) vapor and oxygen plasma for 500 cycles at 120 °C using Fiji F200 (Cambridge NanoTech Inc.). The PAALD cycle consisted of 0.06 s TMA pulse, 10 s argon purge (200 SCCM), 20 s O<sub>2</sub> plasma (20 SCCM), and 5 s argon purge (200 SCCM) at 0.3 mTorr. PAALD process was preferred for its lower deposition temperature and shorter purge time comparing with a thermal ALD process. Also, PAALD reduces hydrogen incorporation in Al<sub>2</sub>O<sub>3</sub> films compared to thermal ALD,<sup>17,18</sup> thus improving the film quality.<sup>18,19</sup> The deposition rate was about 1.04 Å/cycle on silicon substrate, measured by using VASE ellipsometer (J.A. Woollam Co., Inc), which is similar to Langercis *et al.* reported.<sup>13</sup> Following the PAALD layer, 6  $\mu\text{m}$  of parylene C were deposited using the standard Gorham process in LabTop 3000 parylene coater (Para Tech Coating).<sup>9</sup> Silane A-174 (Momentive Performance Materials) was employed as adhesion promoter for the interface between Al<sub>2</sub>O<sub>3</sub> and parylene C. IDEs were soaked in 6-ml vials (Fig. 1) with 1 $\times$  PBS

in a customized soaking chamber. The PTFE insulation at the end of lead wires was removed for the purpose of electrical connection to the Gamry potentiostat. PBS was changed every other week to minimize the ion concentration change due to water evaporation. All the leakage current and impedance measurements were done in 1 $\times$  PBS solution under pre-set constant temperature.

AFM micrographs show that the Al<sub>2</sub>O<sub>3</sub> film (RMS surface roughness of 0.17 nm for the fused silica substrate) has RMS surface roughness of 0.48 nm, as shown in Figure 2, indicating highly conformal and uniform film. X-ray photoelectron spectroscopy (XPS) was used to measure the composition of Al<sub>2</sub>O<sub>3</sub> films for as deposited and depth profiled samples. The measurements were collected using a Kratos AxisUltraDLD instrument with monochromatic Al-K $\alpha$  radiation, and Ar-ion sputtering for depth profiling using 4 kV ions. The measured compositions are presented in Table I, and show an O/Al ratio of as-deposited Al<sub>2</sub>O<sub>3</sub> films was 1.41, compared to a stoichiometric value of 1.5. Previous reports in the literature have measured an O/Al ratio of >2.<sup>12,20</sup> No Ar gas was measured by XPS in the film.

Impedance of the encapsulation and its changes with time are very important because it is inversely related to crosstalk and signal loss via shunting with biological fluids, especially for implants with active electronics. EIS is widely utilized to evaluate the longevity and degradation kinetics of coatings.<sup>21,22</sup> Wide spectrum (1 Hz–1 MHz) impedance was measured to provide more information regarding the overall performance of the encapsulation. Impedance was first measured in air before soaking (Figure 3). The measurement results were fitted into a simple constant phase element (CPE) equivalent circuit model based on the relative constant phase. Capacitance of the dry IDEs was about 45 pF. The phase was almost constant at 90° for the whole frequency range, indicating the expected purely capacitive behavior. Then samples were soaked in 1 $\times$  PBS at 37 °C. Impedance dropped about one order of magnitude immediately after the sample was immersed in PBS, and the phase stayed almost constant (90°) at high frequency (>100 Hz) and increased about 5° at low frequency (1–100 Hz). Thereafter, the impedance and phase remained nearly unchanged during the 140-

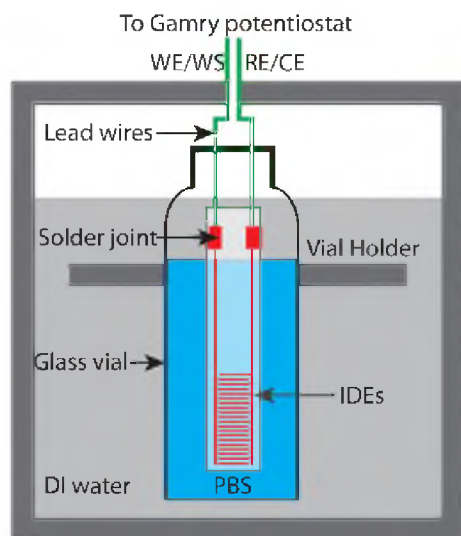


FIG. 1. Schematic of soak testing setup. Two lead wires were soldered to two microfabricated big bond pads on the IDEs for electrical connection, and they came out of the vial through a pre-drilled small hole on the cap. The impedance and leakage current measurements were conducted using a two-electrode configuration by connecting the working sensing to working and counter to reference electrodes, respectively.

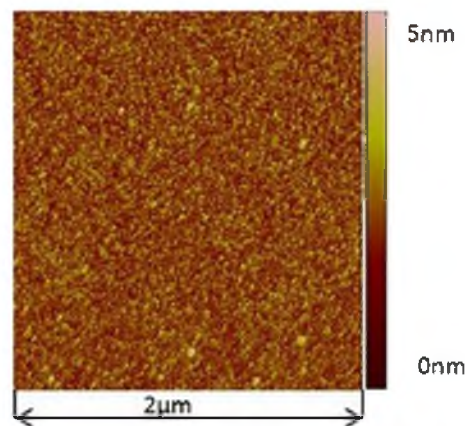


FIG. 2. AFM micrograph of as-deposited 52 nm of Al<sub>2</sub>O<sub>3</sub> on quartz substrate.



TABLE I. XPS analysis of an  $\text{Al}_2\text{O}_3$  layer deposited using PAALD process-500 cycles of TMA +  $\text{O}_2$  gas on fused silica.

Each time(s)	O 1s	C 1s	$\text{Al}_2\text{p}$	$\text{Si}_2\text{p}$
0	51.5	14.5	34	0
300	57.3	0.5	42.2	0
600	58.5	0	41.5	0
900	57.8	0	41.9	0.3
1200	13.2	1.4	7.8	77.6
1500	0.9	0	0	99.1

day soak testing. The consistency of the impedance indicated that the encapsulation was intact. The capacitance based on the CPE model was about 66 pF, which was about a 50% increase compared to measurements in air. This is most likely due change of ambient media from air to PBS. Water has relative permittivity of 80,<sup>23</sup> which is much higher than that of parylene C ( $\epsilon_r = 3.15$ ) and air. This would increase the "equivalent" relative permittivity of the coating, and thus the capacitance of the test structures.

Accelerated lifetime test was performed in order to expedite the validation process of this encapsulation scheme as the films need to encapsulate the devices for years at 37 °C.<sup>7</sup> Body temperature (37 °C) has been chosen as a baseline, and accelerated aging factors (F) are listed in Table II based on a doubling of the reaction rate for each 10 °C increase.<sup>24,25</sup> Impedance and phase of IDEs soaked at different temperatures were almost identical (Figure 4). During the 140-day period of soaking test, samples at higher temperature were expected to fail faster based on Arrhenius equation. No significant changes in the EIS data from degradation in the encapsulation have been observed as expected in most cases since the encapsulation is still almost intact and it is far from failure. Because of this, the accelerated lifetime testing is not able to resolve the characteristics of the encapsulation degradation at this time and determine if they have an Arrhenius character.

The impedance of the encapsulation at 1 kHz is important for a lot of applications, e.g., neural recording and stimulation,

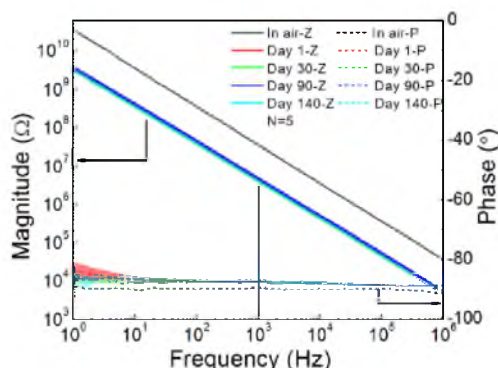


FIG. 3. Bode plots of impedance spectroscopy of 140-day soaking test in 37 °C PBS for alumina and parylene C coated samples. The magnitude was denoted by Z and the phase was denoted by P in the legend. Data was acquired from 5 (N refers to number of samples) samples and shaded areas represent the standard error. There was an initial drop for the impedance from air to PBS; then the impedance and phase remained nearly constant.

TABLE II. Accelerated aging factors and equivalent soaking time for different elevated temperatures relative to 37 °C.

Temperature (°C)	Aging factor (F)	Real soaking time (day)	Equivalent soaking time at 37 °C (day)
37	1	140	140
57	4	140	560
67	8	140	1120
80	20	57	1140

because the frequency of action potentials is about 1 kHz. Figure 5 shows the impedance of IDEs soaked at different temperatures at 1 kHz. The impedance was initially about 36 M $\Omega$  for all samples in air; it dropped to 3.5 M $\Omega$  immediately after immersion in PBS and remained at the same level for the rest of the testing period. This impedance is very high, which is a very good insulation for implantable electronics. This is about one order of magnitude higher than Hsu *et al.*<sup>7</sup> (IDEs with same dimensions used) and Seymour *et al.*<sup>8</sup> reported by using parylene C as encapsulation and also Hsu *et al.*<sup>7</sup> reported using a-SiC<sub>3</sub>H encapsulation.<sup>26</sup> The factor that could possibly contribute the high impedance is that fused silica has higher resistivity than silicon substrate.<sup>27</sup>

Leakage current is another important metric for the performance of encapsulation and was measured by continuously applying 5 V dc bias. The temperature-voltage bias should have significant effect on accelerated failures.<sup>28</sup> Figure 6 shows the leakage current of IDEs soaked at different temperatures. The leakage current was about 1 pA for all the samples in air before soaking; it increased dramatically to about 15 pA (approximately equivalent to  $3.3 \times 10^{11} \Omega$  dc resistance) immediately after being soaked and then remained almost unchanged for the rest of the soaking period for alumina and parylene coated samples. For parylene coating, the leakage current increased dramatically up to nA range after 130 days of soaking at 57 °C, indicating failure of the coating. The parallel dc resistance from CPE modeling ranged from  $10^{11}$  to  $5 \times 10^{11} \Omega$ , which was consistent with the leakage current measured. The initial current increase is mainly because of the dc resistance drop. When IDEs are in air, the effective

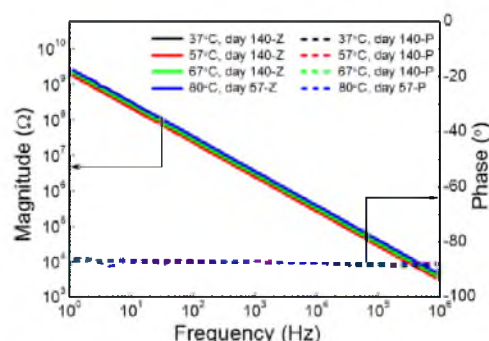


FIG. 4. Impedance spectroscopy plots of IDEs at 37 °C and elevated temperature for accelerated testing in PBS. The magnitude was denoted by Z and the phase was denoted by P in the legend. The time in the plot is the actual soaking time at that specific temperature. No obvious temperature effect has been observed yet. Soak testing of the presented samples continued after the publication of this report.

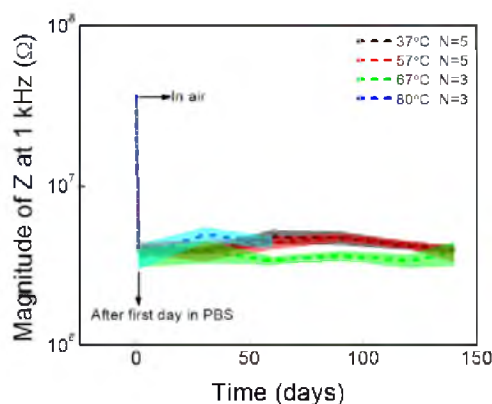


FIG. 5. Magnitude of impedance at 1 kHz for IDEs soaked at different temperatures in PBS. N refers to number of samples. "Day 0" means samples were in air before soak testing.

distance for dc resistance was  $130\ \mu\text{m}$  (distance between two electrodes); after being soaked in PBS, it became about  $12\ \mu\text{m}$  (2  $6\text{-}\mu\text{m}$  thick parylene layer and conductive PBS). The effective distance for dc resistance decreased about 10 times, which leads to the dramatic increase in leakage current. The consistency of leakage current suggests that no obvious corrosion was occurring to the  $\text{Al}_2\text{O}_3$  film. The extremely low leakage current ( $\leq 20\ \text{pA}$ ) was excellent for IDEs after roughly three years of equivalent soaking time at  $37^\circ\text{C}$ . We have to keep in mind that planar test structures tend to have longer lifetime compared with integrated devices for a couple of reasons: (1) complex topography, (2) force from micromotion of the device after being implanted, (3) tethering force from wires of the device, (4) damage due to handling/implantation during surgery. Those factors are not fully presented or activated with IDE test structures. Testing of fully integrated devices with alumina and parylene coating is under way.

In conclusion, we have demonstrated that combination of PAALD  $\text{Al}_2\text{O}_3$  and parylene C has excellent insulation performance for test structures and is a promising near-hermetic encapsulation for implantable microsystems and electronics. IDEs coated with  $\text{Al}_2\text{O}_3$  and parylene C were

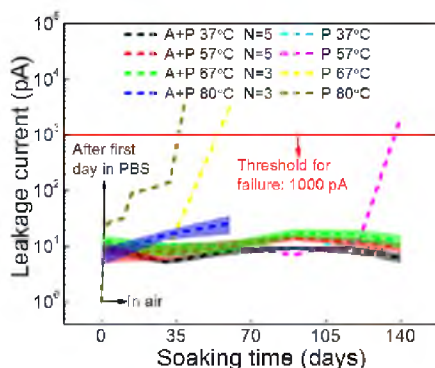


FIG. 6. Leakage current test plots of 140-day test period for parylene (P) coating and alumina and parylene (A+P) coating under 5 V dc bias. N refers to number of samples. "Day 0" means samples were in air before soaking test.

tested at  $37^\circ\text{C}$  and elevated ( $57$  to  $80^\circ\text{C}$ ) temperatures (about three years of equivalent soaking time at  $37^\circ\text{C}$ ) in PBS and the impedance kept at  $3.5\ \text{M}\Omega$  and leakage current was at around  $15\ \text{pA}$ . The initial impedance drop and leakage current increase were analyzed. Temperature effect on the lifetime of the IDEs was studied, and equivalent lifetime was roughly estimated. Alumina and parylene coating lasted at least 3 times longer than parylene coated samples at  $80^\circ\text{C}$ , showing its robustness and superiority. Those results demonstrated the quite excellent potential suitability of combining with  $\text{Al}_2\text{O}_3$  and parylene C as encapsulation for chronic biomedical implants. Long-term *in vivo* test of the encapsulation needs to be performed to further justify this encapsulation scheme.

This work was supported in part by DARPA (Contract No. N66001-06-C-4056) and NIH (Contract No. 1R01NS064318-01A1). The authors gratefully acknowledge Charles Fisher at the Nanofab of the University of Utah for his help of  $\text{Al}_2\text{O}_3$  deposition. Florian Solzbacher has commercial interest in Blackrock microsystems, which manufactures and sells neural interfaces. The views expressed are those of the authors and do not reflect the official policy or position of the Department of Defense or the U.S. Government. Approved for Public Release, Distribution Unlimited.

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## CHAPTER 4

### LONG-TERM BI-LAYER ENCAPSULATION PERFORMANCE OF ATOMIC LAYER DEPOSITED $\text{Al}_2\text{O}_3$ AND PARYLENE C FOR BIOMEDICAL IMPLANTABLE DEVICES<sup>2</sup>

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# Long-Term Bilayer Encapsulation Performance of Atomic Layer Deposited $\text{Al}_2\text{O}_3$ and Parylene C for Biomedical Implantable Devices

Xianzong Xie\*, Loren Rieth, Ryan Caldwell, Mohit Diwekar, Prashant Tathireddy, Rohit Sharma, and Florian Solzbacher

**Abstract**—We present an encapsulation scheme that combines atomic layer deposited (ALD)  $\text{Al}_2\text{O}_3$  and Parylene C for the encapsulation of implantable devices. The encapsulation performances of combining alumina and Parylene C was compared to individual layers of Parylene C or alumina and the bilayer coating had superior encapsulation properties. The alumina–Parylene coated interdigitated electrodes (IDEs) soaked in PBS for up to nine months at temperatures from 37 to 80 °C for accelerated lifetime testing. For 52-nm alumina and 6- $\mu\text{m}$  Parylene C, leakage current was  $\sim 20$  pA at 5 VDC, and the impedance was about 3.5 M $\Omega$  at 1 kHz with a phase near  $-87^\circ$  from electrochemical impedance spectroscopy for samples soaked at 67 °C for equivalent lifetime of 72 months at 37 °C. The change of impedance during the whole soaking period (up to 70 months of equivalent soaking time at 37 °C) over 1 to 10<sup>6</sup> Hz was within 5%. The stability of impedance indicated almost no degradation of the encapsulation. Bias voltage effect was studied by continuously applying 5 VDC, and it reduced the lifetime of Parylene coating by  $\sim 75\%$  while it showed no measurable effect on the bilayer coating. Lifetime of encapsulation of IDEs with topography generated by attaching a coil and surface mount device (SMD) capacitor was about half of that of planar IDEs. The stable long-term insulation impedance, low leakage current, and better lifetime under bias voltage and topography made this double-layer encapsulation very promising for chronic implantable devices.

**Index Terms**—Accelerated lifetime testing, atomic layer deposited (ALD)  $\text{Al}_2\text{O}_3$  (alumina), bias voltage, encapsulation of implantable devices, impedance spectroscopy, leakage current, Parylene C, topography.

Manuscript received February 27, 2013; revised April 8, 2013 and May 18, 2013; accepted May 31, 2013. Date of publication June 6, 2013; date of current version September 14, 2013. This work was supported by Defense Advanced Research Projects Agency under Contract N66001-06-C-4056 and by National Institutes of Health under Contract 1R01NS064318-01A1. Asterisk indicates corresponding author.

\*X. Xie is with the Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, UT 84112 USA (e-mail: xianzongxie@gmail.com).

L. Rieth, M. Diwekar, P. Tathireddy, R. Sharma, and F. Solzbacher are with the Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, UT 84112 USA (e-mail: loren.rieth@utah.edu; diwekar@ecc.utah.edu; p.tathireddy@utah.edu; rohit.sharma@utah.edu; florian.solzbacher@utah.edu).

R. Caldwell is with the Department of Bioengineering, University of Utah, Salt Lake City, UT 84112 USA (e-mail: ryan.caldwell@utah.edu).

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Digital Object Identifier 10.1109/TBME.2013.2266542

## 1. INTRODUCTION

ELECTRONIC biomedical implantable devices have been widely developed and commercialized for different applications, such as pacemakers, cochlear implants, and deep brain stimulators. The commercially available implants typically use hermetically packaging in laser-welded enclosures [1]. Device miniaturization, required for many applications, makes hermetic encapsulation a very challenging solution. Hermetic encapsulation based on cans and microfluids take more space than thin-film-based coating solutions and it can also potentially interfere with telecommunication for wireless systems. Implantable sensing and therapeutic devices require interaction with physiological environment by using fully exposed microfabricated active regions, for drug delivery, neuroprosthetics, etc. [2]. Longevity, long-term stability and functionality of the implantable electronic systems, relying on the encapsulation performance, are very critical to reduce the surgical risks from follow-up surgeries and generate the level of efficacy that justifies the risks associated with the implants. We are developing neural interfaces for neural stimulation and recording based on Utah electrode array (UEA) [3] that incorporate active electronics, and are targeting lifetimes of 70 years, requiring these electrode arrays to be protected from the physiological environment of the body.

The electrical insulation performance, and its change over-time, is one of the main metrics to measure the effectiveness of the encapsulation. A high impedance encapsulation is critical to achieving separation between channels, and achieving good selectivity for neural interfaces. The change of the impedance reflects the degradation of the encapsulation, and can be precisely monitored by electrochemical impedance spectroscopy (EIS) [4]. The encapsulation has to be biocompatible, conformal, highly resistive, and have a low dielectric constant [5]. Inorganic materials, such as silicon nitride and silicon carbide, have been used for encapsulation because of their corrosion resistance and low permeability to water, oxygen, and ions. But they tend to have high deposition temperature, which may not be compatible with implantable devices with active electronics and polymer materials. Silicon nitride slowly dissolves *in vivo* [6], [7], and silicon carbide tends to have relative poor conformality when deposited using low-temperature plasma enhanced chemical vapor deposition (PECVD) [8]. Polymer encapsulation is attractive due to their potential for flexibility, biocompatibility, high impedance, low dielectric constant, and low deposition temperature.

Parylene C has been commonly employed as encapsulation material for implantable devices [9]–[11] because of its many of attractive properties. It is chemically inert and has low dielectric constant ( $\epsilon_r = 3.15$ ) [12]. It has low water vapor transmission rate (WVTR) of  $0.2 \text{ (g}\cdot\text{mm)/(m}^2\cdot\text{day)}$  [13], high resistivity ( $\sim 10^{15} \text{ }\Omega\cdot\text{cm}$ ) and has a USP class VI biocompatibility [14]. Another attractive characteristic is the ability to deposit conformal and pin-hole free films at room temperature. Parylene C is also an excellent ion barrier [15], which is very important for implants exposed to physiological environment. This is also likely to prevent or reduce corrosion since often ions have to be transported during the corrosion reactions. Failure of Parylene C coating has been reported [16] due to moisture permeation and is dramatically exacerbated by interface contamination. Another well-known issue with Parylene C is it has poor adhesion to inorganic and metal substrate materials [17]–[19]. A couple of techniques have been developed to improve the adhesion. Methane plasma treatments have been used to improve the adhesion by creating radical sites for covalent bonding [20]. Heat treatments were also found to be useful for improving adhesion by annealing the polymer and improving mechanical interlock adhesion with the substrate [21], [22]. Reactive Parylene was also found to increase the adhesion by introducing additional functional groups other than Cl to form chemical bonds with the substrates [10].

Moisture condensation on contaminants at the interface can also cause delamination of Parylene films. The failure mode can be minimized by decreasing moisture transport to the interface between the coating and the device, and controlling the interface contamination and chemistry to suppress the nucleation of liquid water. Most polymers can provide WVTR in the range of  $1\text{--}10 \text{ g/m}^2\cdot\text{day}$ , and traditional water barriers such as Al and silicon oxide have WVTR of  $0.1\text{--}0.001 \text{ g/m}^2\cdot\text{day}$ , which cannot provide good enough protection from moisture for organic electronic devices requiring WVTR of  $10^{-6} \text{ g/m}^2\cdot\text{day}$  [23].  $\text{Al}_2\text{O}_3$  films deposited by atomic layer deposited (ALD) has been demonstrated as an excellent moisture barrier with WVTR at the order of  $\sim 10^{-10} \text{ (g}\cdot\text{mm)/(m}^2\cdot\text{day)}$  [24]–[27], for preventing the degradation of extremely moisture-sensitive organic light-emitting diodes (OLEDs). The biocompatibility of  $\text{Al}_2\text{O}_3$  is comparable to that of corrosion resistant metals like titanium [28]. Finch *et al.* [29] reported that ALD alumina-coated glass slides had very similar level of biocompatibility compared with uncoated glass slides. Also bulk alumina is used as substrate for floating microelectrode arrays for neural recording, suggesting it is reasonable for use with neural tissue, at least if encapsulated [30]. ALD  $\text{Al}_2\text{O}_3$  is superior compared with films generated by other deposition techniques such as sputtered  $\text{Al}_2\text{O}_3$  in terms of moisture barrier [24], [31] because it is denser and pin-hole free. Liquid water is known to slowly corrode  $\text{Al}_2\text{O}_3$  thin films [32], mostly likely due to the incorporation of hydrogen in the form of OH groups in the film [33], [34]; therefore,  $\text{Al}_2\text{O}_3$  alone is not suitable for encapsulation of biomedical implants directly exposed to physiological environment. The idea of combining  $\text{Al}_2\text{O}_3$  and Parylene C is based on the concept that  $\text{Al}_2\text{O}_3$  works as an inner moisture barrier and Parylene works as an external ion barrier, preventing contact of  $\text{Al}_2\text{O}_3$  with liquid water, and slowing the kinetics of alumina corrosion.

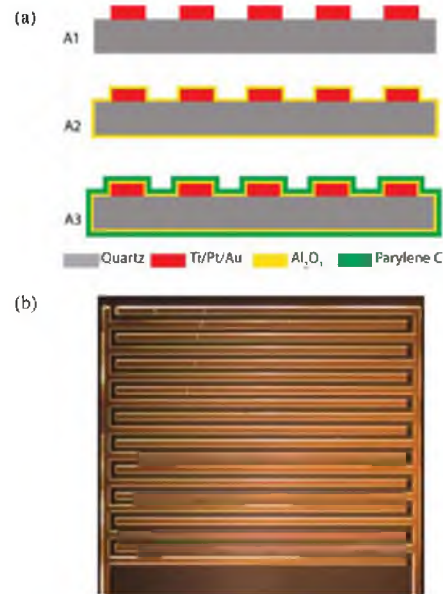


Fig. 1. (a) (A1–A3) Main fabrication process of IDEs. (b) Micrograph of the fabricated IDEs on quartz substrate.

## II. MATERIALS AND METHODS

### A. Interdigitated Electrodes Fabrication

Interdigitated electrodes (IDEs) are widely used as test structures for evaluating coating performance because of their high sensitivity to the degradation of coating [10], [19], [35]. Electrode traces and spaces are  $130 \text{ }\mu\text{m}$  wide and  $2.5 \text{ mm}$  in length, and there are 11 pairs of electrodes in total on fused silica substrates. Standard liftoff lithographic techniques were used to pattern the as-deposited metals. LOR 7B (MicroChem Corp.) and 1813 (Shipley) were spun on  $500\text{-}\mu\text{m}$ -thick fused silica substrates to pattern the later deposited metal. Ti/Pt/Au ( $100/150/150 \text{ nm}$ ) were sputtered using a T-M Vacuum sputter system. The resist was removed with acetone and Shipley developer 352 after metal deposition to get the desired pattern [see Fig. 1(A1)]. The IDEs were then annealed at  $375 \text{ }^\circ\text{C}$  in forming gas (Ar:H<sub>2</sub> 98%:2%) for 45 min in a Linberg furnace. Finally, the fused silica wafer was diced and singlated into individual samples using Disco DAD3220 [see Fig. 1(b)].

### B. $\text{Al}_2\text{O}_3$ and Parylene C Deposition

After singlation, the IDEs were soldered with wires for later electrical measurement and cleaned with acetone, isopropyl alcohol (IPA) and deionized (DI) water, ready for coating.  $\text{Al}_2\text{O}_3$  was deposited by sequentially exposing IDEs to trimethylaluminum (TMA) vapor and oxygen plasma for 500 cycles at  $120 \text{ }^\circ\text{C}$  using Fiji F200 [Cambridge NanoTech Inc.; see Fig. 1(A2)]. Each plasma-assisted (PA)-ALD cycle consisted of a  $0.06 \text{ s}$  TMA pulse,  $10 \text{ s}$  argon purge,  $20 \text{ s}$   $\text{O}_2$  plasma exposure with flow rate of  $20 \text{ sccm}$  at  $300 \text{ W}$  RF power, and a  $5 \text{ s}$  argon purge at  $0.3 \text{ mTorr}$ . Compared to thermal ALD processes,

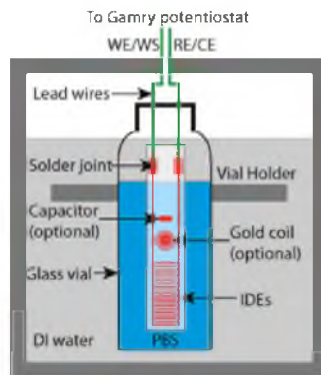


Fig. 2. Schematic of soak testing setup. The impedance and leakage current were conducted using a two-electrode configuration by connecting the working sensing to working and counter to reference electrodes, respectively. Wire-wound gold coils were wire bonded and fixed with silicone to some of the samples to create topography.

PA-ALD process was preferred for its lower deposition temperature and shorter purge time by using reactive oxygen species as oxidizer instead of water. Also, PA-ALD process reduces hydrogen incorporation in  $\text{Al}_2\text{O}_3$  films compared with same temperature thermal ALD process [36], [37], thus improve the film quality in terms of leakage current [37], [38].

Following the alumina coating, the IDEs were silanized with silane A-174 (Momentive Performance Materials) vapor to improve the adhesion between  $\text{Al}_2\text{O}_3$  and Parylene C layer. Then, 6  $\mu\text{m}$  of Parylene C was deposited by standard Gorham process [12] in a LabTop 3000 Parylene coater (Para Tech Coating), using DPX-C dimer (Specialty Coating Systems) [see Fig. 1(A3)].

### C. Soaking Test Setup

The soaking tests were performed in digitally controlled water baths (HH-4, C and A Scientific) at temperatures from 37 to 80 °C. The water baths use a magnetic stirrer for temperature uniformity, and have a temperature precision of  $\pm 0.5$  °C. The 6 mL sample vials containing the test structures immersed in saline were supported in the temperature controlled water bath using an acrylic holder (Fig. 2). The IDEs were submerged during the experiment. The sample vials were filled with 1 $\times$  phosphate buffered saline (PBS) and the solution was changed every two weeks to minimize the sodium concentration variation due to water evaporation. The PBS had composition of 0.0027 M KCl and 0.0137 M NaCl with pH of 7.4. Multiple water baths were used to soak samples at 37, 57, 67, and 80 °C, respectively. In order to investigate the effect of bias voltage on coating performance, active soaking was performed by applying 5 VDC bias to one terminal of the IDEs. The effect of topography on the encapsulation performance was also studied by adding an extra wire-wound gold coil (see Fig. 11) and an SMD capacitor on top of flat IDE test structure (see Fig. 2) to simulate the complex geometries of the real implantable devices. Gold coils were wired bonded and SMD capacitors were soldered

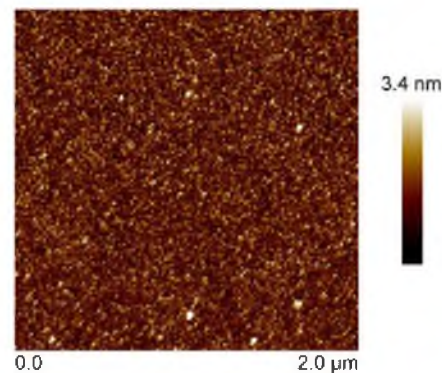


Fig. 3. AFM micrograph of as-deposited 52 nm of  $\text{Al}_2\text{O}_3$  on quartz substrate.

to the IDEs and they were not part of the circuit for electrical measurement. IDEs without gold coil and capacitor were used as control samples to determine the effects of the additional topography.

### D. Impedance and Leakage Current Measurement

EIS has been widely used to evaluate the longevity and degradation of both organic and inorganic coatings [4], [39], [40]. All the EIS and chronoamperometry experiments were carried out using a Reference 600 potentiostat (Gamry Instruments). During EIS measurement, a sine wave of 50 mV was applied from 1 Hz to 1 MHz and 10 data points per decade (3 replicates for each data point) were obtained. A two-electrode configuration was realized by connecting working to working sense electrode and counter to reference electrode, respectively. The 5 VDC (sourced by using the Gamry) leakage current is used to diagnose the integrity of the coating (including pin holes and acceleration of electrochemical corrosion mechanisms) using chronoamperometry. The Reference 600 was calibrated every month to make sure the measurement accuracy.

## III. RESULTS

### A. ALD Alumina Characterization

The  $\text{Al}_2\text{O}_3$  film thickness was about 52 nm and the deposition rate was about 1.04  $\text{\AA}/\text{cycle}$ , which is typical for ALD process [41]. AFM micrographs (Fig. 3) show the surface roughness ( $R_{\text{rms}}$ ) increases from 0.17 to 0.48 nm for the bare substrate and ALD film, respectively. X-ray photoelectron spectroscopy (XPS) was used to analyze the composition of  $\text{Al}_2\text{O}_3$  films. The O/Al ratio of as-deposited  $\text{Al}_2\text{O}_3$  films was 1.41, which was close to stoichiometric value of 1.5, comparing with O/Al ratio of over 2 reported elsewhere [24], [42] when  $\text{O}_3$  was used as oxidizer. Also, no Ar was detected in the film.

### B. Impedance at 37 °C (Body Temperature) Over Time

The impedance was first measured in air before soaking for all samples with different coatings:  $\text{Al}_2\text{O}_3$ , Parylene C, and  $\text{Al}_2\text{O}_3 + \text{Parylene C}$ . The phase is near  $-90^\circ$  for all types

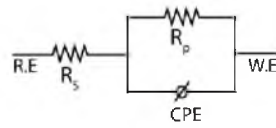


Fig. 4. An equivalent circuit for modeling the electrical characteristics of the IDE test structures. RE denotes reference electrode and WE denotes working electrodes.  $R_s$  is the resistance of the PBS.  $R_p$  is the resistance of the coating film and the substrate, and CPE represents the “imperfect capacitor” characteristics of the IDEs.

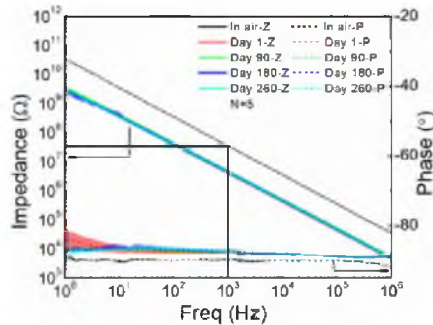


Fig. 5. Bode plots of impedance spectroscopy of 260-day soaking test in 37°C PBS for alumina + Parylene coating. The impedance is denoted by Z and the phase is denoted by P in the legend. Data were acquired from five samples and shaded areas represent the standard error ( $N = 5$ ). There was an initial drop for the impedance from air to PBS; then, the impedance and phase remained nearly constant for the duration of the soaking.

of samples, indicating the expected purely capacitive behavior. The measurement results were fitted into a simple constant phase element (CPE) equivalent circuit model based on the relative constant phase, as shown in Fig. 4. Capacitance of the dry IDEs was about 4.5 pF, and it increased to 51 pF after immersion in PBS. Following the impedance measurement in air, samples were submerged in 1× PBS at 37°C for about nine months, and impedance spectroscopy was performed every week. The impedance and phase are shown in Fig. 5 as a function of time. The impedance declined about one order of magnitude and the phase shifted from  $-90^\circ$  to  $-88^\circ$  almost immediately after sample immersion in PBS. During the 260-day soaking testing, impedance remained nearly unchanged, phase remained relatively constant at higher frequencies ( $> 10$  Hz) and a slight increase of phase was observed (from  $-88^\circ$  to  $-86^\circ$ ) for the frequencies of 1–10 Hz.

### C. Accelerated Lifetime Testing

Accelerated lifetime testing was performed at different temperatures to speed up the validation process for the encapsulation scheme which usually takes years [9]. Body temperature (37°C) was used as the baseline temperature and accelerated aging factors are calculated as shown in Table I based on a doubling reaction rate for each 10°C increase in reaction temperature [43], [44]. The impedance stayed unchanged during the whole period for samples soaked at 37, 57, 67, and 80°C compared with impedance at the first day of soak testing, shown

TABLE I  
ACCELERATED AGING FACTORS AND EQUIVALENT SOAKING TIME FOR DIFFERENT ELEVATED TEMPERATURES REFERRING TO 37°C

Temperature (°C)	Aging factor (F)	Real soaking time (days)	Equivalent soaking time at 37°C (days)
37	1	260	260
57	4	260	1040
67	8	260	2080
80	20	180	3600

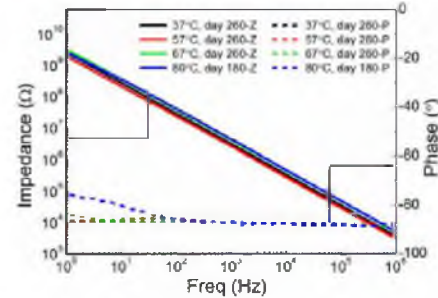


Fig. 6. Impedance spectroscopy plots of IDEs with alumina and Parylene coating at 37°C and elevated temperature for accelerated testing in PBS. The impedance is denoted by Z and the phase is denoted by P in the legend. All the samples are still under testing.

in Fig. 6. The phase remained close to  $-90^\circ$  after nine months of soak testing for samples at 37, 57, and 67°C. A slight increase of phase was observed for samples at 80°C, indicating initial degradation of the encapsulation.

The equivalent soaking time was calculated by multiplying the real soaking time with the corresponding accelerated aging factor at that specific temperature, shown in Table I. Based on this estimation, the samples soaked at 80°C are almost equivalent to ten years at 37°C. It is well known that temperature higher than 57°C could introduce new failure modes that do not exist during normal aging processes at 37°C. However, this measurement is useful as a worst-case scenario, since activation of additional failure modes would likely only decrease the lifetime of devices.

### D. Impedance at 1 kHz

Impedance at 1 kHz is very important for a lot of applications, such as neural recording and stimulation, because action potentials are centered around frequencies of 1 kHz. The impedance was about 36 MΩ for all samples in air; it dropped to around 3.5 MΩ after the first day of soak testing in PBS and remained unchanged for the remaining nine-month testing period as can be observed from the data in Fig. 7. This is about one order of magnitude higher than Hsu *et al.* [9] (with the same geometry) by using Parylene C as encapsulation layer and also higher than Hsu *et al.* [8] reported using *a*-SiC<sub>x</sub>:H encapsulation, most likely due to the contribution from the alumina layer. Further analysis will be performed in Section IV. No measurable



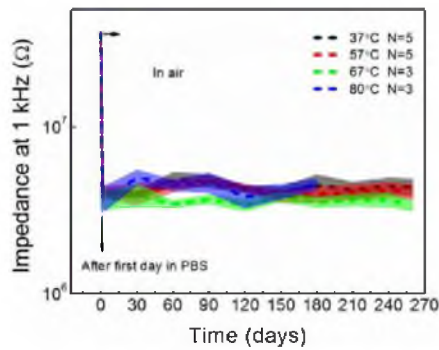


Fig. 7. Impedance at 1 kHz for IDEs soaked at different temperatures in PBS. "Day 0" means samples were in air before soaking test.

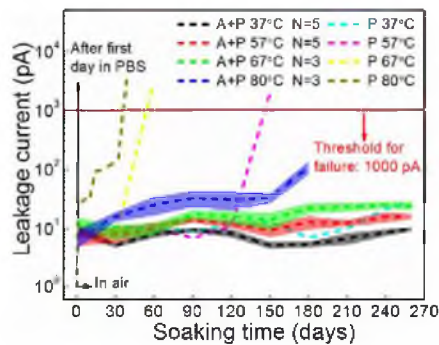


Fig. 8. Leakage current from IDE structures is plotted versus time over the 260-day test period. "Day 0" means samples were in air before soaking test. Higher temperature is prone to have higher leakage current as expected. Also Parylene-coated samples have much higher leakage current compared with alumina and Parylene coating at the same time period for accelerated lifetime testing.

difference was observed between samples soaking at different temperatures.

### E. Leakage Current

Leakage current is another very important metric to quantitatively measure the performance of the encapsulation. Leakage current was measured by applying a 5 VDC bias between the two terminals of the IDEs. Fig. 8 shows the leakage current for IDEs as a function of time, soaking temperature, and encapsulation of Parylene, and alumina with Parylene bilayers. For alumina- and Parylene-coated IDEs, the leakage current was about 1 pA while sample was in air prior to soaking. Then, it increased immediately to around 15 pA after immersion in PBS, due to a shorter effective distance for dc resistance, which is explained further in Section IV. The leakage current remained  $\sim 15$  pA during the 260-day soaking period for samples at 37, 57, and 67 °C. For samples at 80 °C, the leakage current started to increase at a rate of roughly  $\sim 3$  pA/day after 150 days of soaking and reached 100 pA after 180 days. This is consistent with the increase of phase angle at low frequency observed in

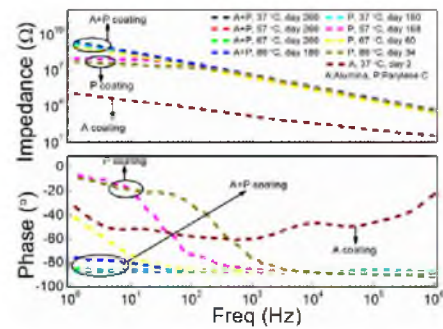


Fig. 9. Impedance comparison of three different encapsulation schemes at different temperatures: alumina only, Parylene only, and alumina + Parylene C. Alumina and Parylene coating has the best insulation performance.

Fig. 6. For Parylene-coated IDEs, leakage current reached over 1 nA (defined as coating failure) after five months of soak testing at 57 °C. IDEs soaked at higher temperature failed earlier due to the temperature effect. Leakage current was in milliamperes level within two days for alumina coating (not shown in Fig. 8). It is noticed that IDEs soaked at higher temperature failed earlier (for Parylene coating) or had higher leakage (for alumina and Parylene coating) after same period of soaking time, due to the temperature aging effect. The extremely low leakage current ( $\leq 20$  pA) was excellent for IDEs with alumina and Parylene coating that have soaked under accelerated conditions for six years of equivalent soaking time at 37 °C with 5 VDC continuous bias.

### F. Encapsulation Scheme Comparison

The accelerated soak test performance of the three different encapsulation schemes, including alumina only, Parylene C only, and alumina and Parylene C were compared. The impedance spectroscopy data collected as a function of time from these samples is presented in Fig. 9. For the alumina-coated samples, the impedance dropped enormously and the phase increased dramatically for the whole frequency range (1 Hz–1 MHz) after two days of soaking at 37 °C and the leakage current reached even the milliamperes level within two days, indicating a rapid and catastrophic failure. The impedance decreased about one order of magnitude for Parylene-C-coated samples and phase deviated from  $-90^\circ$  and increased dramatically even after a relative shorter soaking period of time especially at lower frequencies ( $<100$  Hz) during the accelerated lifetime testing (57, 67, and 80 °C). As the soaking time increases, the impedance kept decreasing even for higher frequency range until it reaches to the impedance of the PBS. The decrease in impedance and increase in phase angle and leakage current (see Fig. 8) indicate a steady failure of Parylene encapsulation. The impedance and phase angle for the alumina- and Parylene-C-coated samples at 1 kHz remained unchanged after the soaking for all different temperatures, with values near 3.6 M $\Omega$  and  $-88^\circ$ , respectively. The double-layer encapsulation maintained a leakage current of less than 20 pA for all temperatures

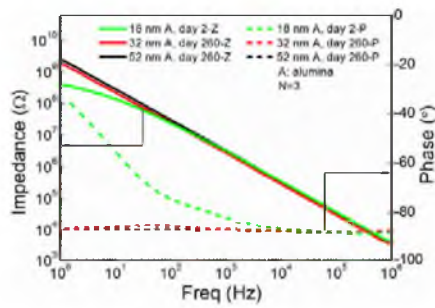


Fig. 10. Effect of alumina thickness on encapsulation performance.  $N$  denotes number of samples. Samples with coating of 18 nm alumina and 6  $\mu\text{m}$  Parylene lasted about two days while thickness of alumina (32 nm and 52 nm) and Parylene lasted about nine months.

(except 80 °C) and time points, which is considerably better than Parylene coating.

#### G. Effect of $\text{Al}_2\text{O}_3$ Thickness

The thickness of the ALD  $\text{Al}_2\text{O}_3$  used as part of the bilayer encapsulation was varied with values of 18, 32, 52, and 70 nm. For coatings of alumina  $\geq 32$  nm and 6  $\mu\text{m}$  Parylene, no changes in the impedance and leakage current were observed at 57 °C (up to date) for nine months of the trial to date. Samples coated with 18 nm alumina and 6  $\mu\text{m}$  Parylene failed within two days of soak testing, as shown in Fig. 10. This lasted even significantly shorter than Parylene-only coated samples.

#### H. Effect of Bias

Implantable devices with active electronics require power. Depending on the voltage and current characteristics, the voltage and current from the power supply can generate an additional factor affecting the encapsulation, which is different than aging mechanism such as electrochemistry and temperature effects [45], [46]. This power can contribute to the electrochemical reactions, corrosion, and degradation modes, move ions, perform electrolysis of water, etc. Alumina, Parylene, and alumina-Parylene bilayer coated samples were tested under continuous 5 VDC bias in PBS. For alumina and Parylene C coating, samples under continuous 5 V bias lasted almost nine months at 57 °C (up to date). However, Parylene C only samples under those conditions lasted only about 50 days, which was only about one third of lifetime of those without dc bias (about 150 days). This suggested that continuous bias voltage accelerated the failure process of the Parylene-coated samples, while it had significantly less effect on the alumina and Parylene bilayer samples.

#### I. Effect of Topography

The soak test results presented thus far were performed with planar IDE test structures, which is a significant difference from the complex structure of actual neural interface devices. In order to begin testing the effects of topography on encapsulation performance, wire-wound gold coils and SMD capacitors [47]

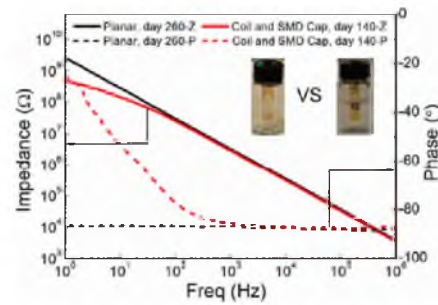


Fig. 11. Effect of topography on encapsulation performance. Alumina- and Parylene-coated samples with coils and SMD capacitors lasted about 140 days while flat samples lasted 260 days at 57 °C.

were added to the surface of the test structures. The alumina and Parylene encapsulation endured about five months at 57 °C. This is shorter than the lifetime of samples without coils that soaked at 57 °C (nine months up to date), as shown in Fig. 11. Parylene-only coated samples with coils and capacitors were also tested, and they lasted about one month (encapsulation failed when leakage current was constantly higher than 1 nA), which also showed that the complex topography had critical negative impact on encapsulation lifetime.

## IV. DISCUSSION

The bilayer encapsulation had leakage current of about 15 pA and impedance of 3.5 M $\Omega$  at 1 kHz after equivalent soak time of about six years at 37 °C. Bias voltage of 5 VDC did not affect the bi-layer encapsulation performance. The excellent soaking performance of the alumina and Parylene coating is ascribed to that Parylene is a good ion barrier with a low but finite water vapor transmission rate (WVTR) (0.2 (g·mm)/(m<sup>2</sup>·day) [13]), and alumina acts as a water barrier (WVTR of 10-10 gmm/m<sup>2</sup>·day [24]–[27]). Failure of Parylene C encapsulation is mainly caused by water penetration and nucleation around surface contaminants [16]. Alumina is an excellent moisture barrier, while it can be corroded when directly exposed to liquid water [48]. Therefore, the order of placing Parylene on top of alumina has been determined by their individual functionalities.

The impedance dropped one order of magnitude immediately after submerging alumina- and Parylene-coated samples in PBS. This initial impedance drop could be partially explained by the change of the environmentally media from air to PBS [49]. The permittivity of PBS solution is 80 [50], which is much higher than that of air ( $\epsilon_r = 1$ ), resulting in higher capacitance of the IDE structure, and the concomitant decrease in impedance. Also, permeation of water through the Parylene C could increase the capacitance due to higher permittivity. This increase of capacitance could also contribute to the drop of the impedance. This is also consistent with the relatively constant phase observed, because a change in capacitance would change the impedance, but the phase would remain close to  $-90^\circ$ . Similar impedance drop was found when samples were soaked in DI water, which

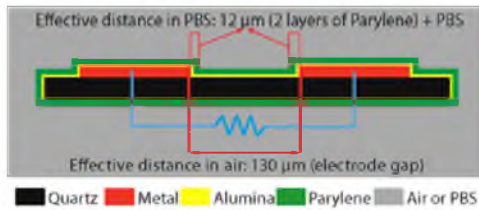


Fig. 12. Cross-sectional schematic of effective distance for dc resistance. The effective distance for dc resistance in air is  $130\ \mu\text{m}$  and in PBS solution it is  $12\ \mu\text{m}$  with highly conductive PBS.

strongly suggested that conductivity of the ambient media did not have significant impact on the impedance change.

Accelerated lifetime tests were performed for alumina and Parylene bilayer samples in order to speed up the evaluation process for this encapsulation method. Those tests were also designed to determine the degradation characteristics of the encapsulation. No obvious difference has been observed for all samples that were soaked at different temperatures in terms of impedance and phase. It is possible that the major shift was below 1 Hz, and we were not able to observe it yet since impedance was not measured for frequencies lower than 1 Hz. Because of this, the accelerated lifetime is not able to resolve the characteristics of the encapsulation degradation at this time, and determine if they have an Arrhenius character. This also suggests that samples are far from failure. The continued performance for the bilayer for beyond 2000 days ( $37\ ^\circ\text{C}$  equivalent) at  $67\ ^\circ\text{C}$  indicated the strong reliability of this bilayer coating for planar test structures.

Fused silica substrates were used in order to eliminate capacitive paths through conductive substrates to improve sensitivity for measuring films with very high impedance [51]. The leakage current increased from 1 to 15 pA when samples were immersed into PBS from air. This initial leakage current is mainly because of the dc resistance drop. When IDEs are in air, the effective distance for dc resistance is about the spacing between two adjacent electrodes, which is  $130\ \mu\text{m}$ . After being immersed into PBS, the effective distance becomes the thickness of two 50-nm alumina layers, two  $6\text{-}\mu\text{m}$  Parylene layers linked by the conductive PBS, which is about  $12\ \mu\text{m}$  of encapsulation, as shown in Fig. 12. Therefore, the effective distance for dc resistance decreased about ten times, which leads to the drastic increase of the leakage current.

The direct exposure of alumina only coated samples to PBS led immediately failure. The direct contact with water led to the dissolution of the alumina [32]. It has been reported that corrosion protection by using alumina only lasted hours in PBS solution [48], [52]. Another main factor is that the stress of bias voltage for impedance and leakage current measurement speeds up the dissolution of alumina, and thus, the failure of the coating.

With regard to the short lifetime of  $<2$  days for the 18 nm alumina and  $6\ \mu\text{m}$  Parylene coating, we believe this resulted from the 5 VDC bias for leakage current measurement exceeding the breakdown voltage of the alumina film. The breakdown voltage (electrical breakdown strength:  $\sim 3.7\ \text{MV/cm}$  [36], [53]) is

$\sim 6.5\ \text{V}$  for 18 nm alumina and  $\sim 10\ \text{V}$  for 32 nm alumina. These samples with 18 nm of alumina coating failed even more quickly than just Parylene films of equivalent thickness. We believe the breakdown of alumina films creates ions and mechanical damage at the interface between the substrate and Parylene layer. For 52 nm alumina coating, the breakdown voltage would be  $\sim 18\ \text{V}$ , which is sufficient for most implantable devices with good tolerances.

Testing Parylene films with continuous bias voltage and accelerated temperatures had a significant effect on their performance, whereas we have not been had failure sufficient to determine a lifetime for ALD alumina ( $>30\ \text{nm}$ ) and Parylene-coated samples. For alumina ( $>30\ \text{nm}$ ) and Parylene coating, the alumina layer prevented the moisture from permeating to the interface between the alumina and substrate where bias voltage was applied. This limits low resistance pathways that support electrochemical corrosion and degradation process. Therefore, bias voltage has very limited or even no effect on the alumina- and Parylene-coated samples. For Parylene-C-coated samples, due to the existence of moisture and possible contamination at the interface between the substrate and coating layer, the bias voltage can accelerate the mobility of contaminants (especially ions) surrounded by nucleated water and expedite the failure process of the Parylene coating. There are a couple of models that have been proposed for predicting the time to failure for the effects of bias voltage on lifetime [45]. The power rule for voltage model is a simplified Eyring model, which states voltage dependency of time to failure:

$$t_f = AV^{-\beta}$$

where  $t_f$  is time to failure,  $A$  is a constant,  $V$  is the voltage, and  $\beta$  is the voltage stress factor. A 5 VDC bias decreased the lifetime by  $\sim 75\%$  and this gives us an estimation of  $\beta$  to be 0.86. More experiments need to be done to study the effect of bias voltage statistically and quantitatively.

The presence of wire-wound gold coils and SMD capacitors introduced complex topography and therefore resulted in significantly shortened lifetimes for the encapsulation. Complex geometries could affect the conformity and uniformity of the chemical vapor deposited films. The thickness variation of Parylene may result in some weak points of the encapsulation. Due to the surface roughness, sites with extruded particles are vulnerable to voltage bias and handling stress. Thicker Parylene layer would alleviate this problem. The conformity and uniformity of the self-limiting ALD process will not be affected since it has been demonstrated to be extremely conformal even for very high aspect ratio (up to 1000) structures [54]. Also, handling stress for the complex geometries could contribute to the relative short lifetime of the coating. Micromotions between the coil and the substrate could shorten the lifetime of the bilayer encapsulation as well.

## V. CONCLUSION

In summary, we have demonstrated the excellent insulation performance for the combination of PA-ALD  $\text{Al}_2\text{O}_3$  and Parylene C for IDEs and its potential suitability as a near-hermetic

encapsulation for implantable devices. EIS and chronoamperometry were used to evaluate the integrity and insulation performance of the alumina and Parylene bilayer encapsulation. Impedance was  $\sim 3.5 \text{ M}\Omega$  at 1 kHz with phase of close to  $-87^\circ$  by using EIS for samples under  $67^\circ\text{C}$  about nine months (approximately equivalent to 72 months at  $37^\circ\text{C}$ ), indicating no significant degradation. The leakage current was  $\sim 20 \text{ pA}$  by applying 5 VDC bias. The encapsulation performances of alumina only, Parylene C only, and alumina and Parylene C coatings were compared and the bilayer coating demonstrated the highest performance of at least five times longer lifetime than the other two coating approaches. Alumina-coated samples had leakage current higher than 1 mA within two days at  $37^\circ\text{C}$  and Parylene-coated samples have leakage current higher than 1  $\mu\text{A}$  with 60-day soak testing at  $67^\circ\text{C}$ . Using 5 VDC bias, no increases in leakage current and drop in insulating impedance were observed for alumina- and Parylene-coated samples at  $57^\circ\text{C}$  for nine months so far, while it shortened the lifetime of Parylene coating by factor of  $\sim 3$  ( $\sim 50$  days with bias VS  $\sim 150$  days without bias at  $57^\circ\text{C}$ ). The lifetime of alumina- and Parylene-coated devices with wire-wound coils and SMD capacitors was about 50% or less of that of planar test structures. The mechanism and possible methods to mitigate the failure modes associated with topography and electric breakdown of alumina are being investigated. The long-term (more than six years of equivalent lifetime) insulation performance of the double-layer encapsulation shows its potential usefulness for chronic implantable electronic microsystems.

#### ACKNOWLEDGMENT

The authors would like to the staff at the Nanofab at the University of Utah for their fabrication support. Florian Solzbacher has commercial interest in Blackrock microsystems, which manufactures and sells neural interfaces. The views expressed are those of the authors and do not reflect the official policy or position of the Department of Defense or the U.S. Government. Approved for public release; distribution unlimited.

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## CHAPTER 5

### SELF-ALIGNED TIP DEINSULATION OF ATOMIC LAYER DEPOSITED $\text{Al}_2\text{O}_3$ AND PARYLENE C COATED UTAH ELECTRODE ARRAY-BASED NEURAL INTERFACES

#### 5.1 Abstract

Tip deinsulation of Utah electrode array-based neural interfaces is challenging due to the complex 3D geometries and high aspect ratios of the devices. The recently developed alumina and Parylene C bi-layer improved the lifetime of neural interfaces. Additionally, the extra alumina layer protected the underneath iridium oxide from being damaged during laser ablation. A three-step self-aligned process was developed for tip deinsulation of bi-layer encapsulated Utah electrode array. The deinsulation process utilizes laser ablation to remove Parylene C,  $\text{O}_2$  reactive ion etching to remove carbon and Parylene residue, and buffered oxide etch to remove alumina deposited by atomic layer deposition, and expose the  $\text{IrO}_x$  tip metallization. The deinsulated iridium oxide area was characterized by scanning electron microscopy, atomic force microscopy, and x-ray photoelectron spectroscopy to determine the morphology, surface morphology, composition, and properties of the deposited layers. The alumina layer was found to prevent the formation of micro cracks on iridium oxide during the laser ablation process, which has been previously reported as a challenge for laser deinsulation of Parylene

films. The charge injection capacity, charge storage capacity, and impedance of deinsulated iridium oxide were characterized to determine the deinsulation efficacy compared to Parylene-only insulation. Deinsulated iridium oxide with bi-layer encapsulation had higher charge injection capacity and similar electrochemical impedance compared to deinsulated iridium oxide with only Parylene coating. Tip impedances were in the ranges of 20 to 50 k $\Omega$ , with median of 32 K $\Omega$  and standard deviation of 30 k $\Omega$ , showing the effectiveness of the self-masked deinsulation process for alumina and Parylene C bi-layer encapsulation. The relatively uniform tip impedance values demonstrated the consistency of tip exposures.

## 5.2 Introduction

Neural interfaces have been developed for therapies applied to neural disorders and diseases [1-4], and in the pursuit of basic neuroscience research. Implanted neural interfaces have a range of invasiveness and for some applications require chronic implantation, and are therefore exposed to physiological fluids for long periods. The long-term exposure of devices to the physiological environment requires high-performance encapsulation, particularly as integration of active electronics on the devices become more common. Hermetic enclosures and polymer encapsulation (bulk and thin-film based) are the dominant techniques, and encapsulation has been preferred for neural interfaces due to many feedthroughs and space limitation. Parylene C has been widely used as encapsulation materials for biomedical implantable devices [5-9] because of its chemical inertness, low dielectric constant ( $\epsilon_r=3.15$ ) [10], low water vapor transmission rate (WVTR) of 0.2 g·mm/m<sup>2</sup>·day [11], high resistivity ( $\sim 10^{15}\Omega\cdot\text{cm}$ ), and USP class VI

biocompatibility [12]. Parylene C is also an excellent ion barrier [13], which is very important for implants exposed to physiological environment. Failures of Parylene coating have been reported [14] because of moisture penetration, interface contamination, and cracking of the material [15]. We have previously reported that atomic layer deposited (ALD) alumina and Parylene C (A+P) bi-layer encapsulation can be an effective encapsulation strategy to prevent the moisture ingress and separate moisture from interface contaminants [16]. In this paper, we report a highly effective self-aligned and maskless process to deinsulate the electrode tips of bi-layer encapsulated Utah Electrode Arrays (UEAs).

Both ALD and the Gorham process for depositing Parylene C generate extremely conformal films due to the nature of the surface reaction that generates the film [10]. This results in high insulation impedance to the physiological environment due to the high resistivity of these dielectric materials, and the pin-hole free character of the films. However, neural recording and stimulation require information exchange between the neural interface and its adjacent neurons. Selective removal of alumina and Parylene C from the electrode tips is required to generate active recording and stimulation sites for the device [17]. Wet etching is not a viable option for Parylene C since it is inert to most solvents. Historically, tip deinsulation of microelectrodes used high temperature to burn off the insulation or high-voltage discharge to ablate the insulation [18]. The heating method could cause damage and degradation to the insulation near the tip and also damage the active electronics. The high-voltage arc-based deinsulation technique led to fractures in the Parylene insulation along the electrodes [18]. Also, it was difficult for those methods to accurately control the tip exposure, which is a critical factor in the



impedance and selectivity of the electrodes. Several dry etching methods have been investigated, including plasma etching, reactive ion etching (RIE), and deep reactive ion etching (DRIE) [5, 19].

Oxygen plasma etching has been used as a standard Parylene C etching process for UEAs for more than a decade [5]. Due to its complex 3D geometries, precise masking for the electrode tips is a challenge. Both Photoresist and aluminum foil have been used as masks for oxygen plasma etching during UEA manufacturing [20-22]. Use of Photoresist is not applicable to individual UEAs, therefore poking the UEA through a thin aluminum foil to expose the tips is the current process. The major drawback with aluminum foil masking is the low precision and accuracy of the tip exposure control, resulting in significant variations in tip impedance. Also, the poking process is labor intensive and decreases yield through mechanical damage and fractures to the electrode tips. Our group and others have previously reported that ablation of Parylene C can be an effective and adaptable method to remove Parylene encapsulation [23-27].

Alumina film at the tip of the UEA also needs to be removed to obtain the desired electrochemical characteristics of iridium oxide for neural recording/stimulation. Plasma etching has been widely used for etching of  $\text{Al}_2\text{O}_3$  [28, 29]. The etching rate was about 1 nm/minutes with RF power of 100 W[30], which is a slow process for a 50 nm thick alumina layer. Alternative wet etching method needs to be adopted to remove alumina. Due to the incorporation of hydrogen in the form of OH groups in the film [31, 32], Liquid water is known to slowly corrode ALD  $\text{Al}_2\text{O}_3$  thin films [33]. Given the facts of dissolution of alumina in liquid water and extreme inertness of Parylene C in wet etching,

buffered oxide etch (BOE, 6:1 volume ratio of 40% NH<sub>4</sub>F in water to 49% HF in water) wet etching can be used to remove alumina by utilizing Parylene C as a mask layer.

Charge injection capacity (CIC), charge storage capacity (CSC), and electrochemical impedance are critical for neural stimulation/recording. The CIC, CSC, and electrochemical impedance of deinsulated iridium oxide were characterized by chronopotentiometry, cyclic voltammetry (CV), and electrochemical impedance spectroscopy (EIS), respectively. The electrochemical properties of deinsulated iridium oxide with bi-layer encapsulation were found to be stable and similar to that of iridium oxide with Parylene C only coating.

### 5.3 Materials and Methods

#### 5.3.1 Deinsulation Process for Alumina and Parylene Coating

A three-step process was investigated to insulate the A+P bi-layer encapsulation from active sputtered iridium oxide film (SIROF) electrode sites. Parylene-only test structures were also deinsulated as control samples. First, KrF excimer laser ablation (248 nm) Optec Micromaster was used to remove Parylene C. A detailed description of excimer deinsulation is reported elsewhere [27]. Fluence and number of pulse during laser ablation are the two variables optimizing the deinsulation process. SIROF test structures were deinsulated by using 100 laser pulses with fluence of 1500 mJ/cm<sup>2</sup> with pulse duration of 5 ns and frequency of 100 Hz, adopted from Yoo *et al.* [27].

Laser ablation of Parylene C results in redeposition of carbon residue on and around the ablation site. In addition, residual Parylene might be present on the SIROF surface due to roughness, and the variability of incidence angles imposed by the UEA tip

geometry, as shown in Fig 5.1. A 2-minute oxygen plasma was used to remove the carbon contamination to improve the electrochemical impedance ( $Z$  ( $\Omega$ )) and CIC ( $\text{mC}/\text{cm}^2$ ) of SIROF. The oxygen plasma etching used an inductively coupled plasma (ICP)-based March Plasmod (March Plasma Systems), with RF power (13.56 MHz) of 150 W and chamber pressure of 400 mTorr. No mask was required for the oxygen plasma etching since it only etches about 500 nm of Parylene C.

The third step in the process is the removal of alumina film to expose the active tip metal (iridium oxide). An 8-minute BOE etch at room temperature was used to remove alumina on the laser-ablated spots. Again, the Parylene acted as a mask for the BOE etch due to its chemical inertness. Alumina was etched only in the area where Parylene was removed by laser ablation. The BOE etch was found not to affect the electrochemical properties of the iridium oxide.

### 5.3.2 Fabrication of SIROF Test Structures and UEAs

The characterization of this three-step self-aligned deinsulation process was first performed on SIROF planar test structures to allow high-accuracy electrochemical impedance spectroscopy measurements. The deposition processes for metal, metal oxide, alumina, and Parylene C on planar test structures are described elsewhere [16, 20, 34, 35]. The test structures were fabricated on a 4 inch Si wafer. 600 nm of silicon nitride was deposited by LPCVD using  $\text{NH}_3$  and  $\text{SiCl}_2\text{H}_2$  at a temperature 825 °C as an insulation layer between the substrate and the subsequent metal traces. A 50 nm titanium film was deposited followed by 200 nm platinum film by DC sputter deposition in Ar ambient (flow rate of 150 sccm) at 10 mTorr with sputtering power of 90 W (T-M

Vacuum Super series). The titanium is an adhesion layer and the platinum is the trace for later electrical measurements. The iridium oxide film was actively sputtered at a pressure of 10 mTorr with power of 100 W in Ar (flow rate of 100 sccm) and O<sub>2</sub> (flow rate of 100 sccm) plasma. Lift-off process was used to pattern the SIROF. SIROF is the active tip metal for UEA electrodes [36]. The test structures were then annealed at 375 °C in Forming gas (Ar: H<sub>2</sub> 98%: 2%) for 45 minutes in a Linberg furnace. 52 nm of Al<sub>2</sub>O<sub>3</sub> was deposited by plasma assisted atomic layer deposition (PAALD) using trimethylaluminum (TMA) and O<sub>2</sub> as precursors at a substrate temperature of 120 °C using a Cambridge Nanotech Fiji 200 ALD reactor. Details of the alumina deposition can be found at [16, 35]. Silane A-174 (Momentive Performance Materials) was used to improve the adhesion between Al<sub>2</sub>O<sub>3</sub> and Parylene C layer. A 6 μm Parylene C film was deposited using the Gorham process [10] in a LabTop 3000 Parylene coater (Para Tech Coating), using DPX-C dimer (Specialty Coating Systems). Silane A-174 (Momentive Performance Materials) was used to improve the adhesion between Al<sub>2</sub>O<sub>3</sub> and Parylene C layer. Fig 5.2 is a SEM picture of a test structure after three-step deinsulation.

UEA was first designed and fabricated by Normann for intracortical stimulation [20]. A dicing saw was used to cut silicon wafer and create columns with dimension of 150 μm square, 1.5 mm tall, and pitch of 400 μm. The columns were first thinned and then tapered by wet etching. The fabrication details of UEAs are described elsewhere [20, 34].

### 5.3.3 Experiments

The three-step insulation process was characterized by scanning electron microscopy (SEM), atomic force microscope (AFM), chronopotentiometry, cyclic voltammetry (CV),

and electrochemical impedance spectroscopy (EIS). The surface morphology after each etching step was characterized by SEM using an FEI Quanta600. SEM was also utilized to examine the deinsulated tips of UEA. AFM was used to characterize the surface roughness and grain size of laser-ablated SIROF to determine the effect of laser irradiation on the surface morphology. Chemical composition analysis was performed by x-ray photoelectron spectroscopy (XPS) using a Kratos Axis Ultra DLD, to confirm the complete removal of alumina and investigate effect of BOE etching on SIROF.

The CIC is used to measure the ability of SIROF to inject charge for stimulation applications in phosphate buffered solution (PBS, 0.01 M phosphate buffer, 0.0027 M KCl and 0.14 M NaCl). CIC is the total amount of charge per unit area that can be injected into the electrolyte without damaging the SIROF. The CIC measurements were performed within the voltage compliance limits of -0.6 to 0.8 V on top of access voltage in order to avoid the dissolution of SIROF [37]. The CIC was measured by chronopotentiometry with biphasic cathodal-first pulses generated by Gamry Reference 600 (Gamry Instruments). Fig 5.3 shows the measured potential of the 100  $\mu$ A cathodal current pulse with a length of 1 ms following by a symmetric anodal current pulse. The access voltage ( $V_{acc}$ ) is the resistive potential drop across the SIROF and electrolyte. The maximum cathodic and anodic electrochemical potentials ( $E_{mc}$  and  $E_{ma}$ ) of the SIROF were calculated by subtracting  $V_{acc}$  from the maximum negative and positive voltage transient, respectively. The details of this polarization method are reported by Cogan *et al.* [38].

The SIROF CSC ( $mC/cm^2$ ) was measured by cyclic voltammetry in PBS solution, from -0.6 to 0.8 V with a scan rate of 50 mV/S. Also, EIS was performed to determine

the impedance of SRIOF after each step of the deinsulation process, using a 10-mV sinusoidal signal from 1 Hz to 1 MHz. All the CIC, CSC, and EIS measurements were conducted in PBS with a three-electrode arrangement, by using a silver-silver chloride electrode as reference electrode, a thick Pt wire as counter electrode, and iridium oxide as working electrode. Impedances of fully deinsulated electrodes of the Utah electrode array (UEA) were measured by a customized automated impedance tester [39] with 10-mV RMS sine wave at 1 kHz.

#### 5.4 Results and Discussion

Test structures and UEA devices were fabricated to investigate the deinsulation of the process, following the procedures outlined above, and in previous reports [20, 27, 34]. The first step in the deinsulation process is to ablate the Parylene layer, using an excimer laser micromachining system. The surface morphology of the etched surface was analyzed using SEM to determine the efficacy of the Parylene remove compared to Parylene-only insulated control samples, and to characterize any damage to the alumina film or underlying layers. Fig 5.4 shows a set of SEM micrographs from laser-ablated SRIOF spots. The alumina and Parylene (A+P) coated SRIOF after laser ablation (Fig 5.4 (b)) was similar to the as-deposited SRIOF (Fig 5.4 (a)). However, microcracks were clearly observed on Parylene coated SRIOF after laser ablation (Fig 5.4 (d)), especially in detailed view (Fig 5.4 (e)). The microcracks are most likely induced by the high temperature achieved during the laser ablation process. Those microcracks were not present in the sample using the A+P bi-layer encapsulation after laser ablation (Fig 5.4

(c)), which suggests that alumina acted as a shield layer preventing the underlying SIROF damage thorough laser irradiation.

Atomic force microscopy (AFM) was also used to characterize the surface roughness and characteristic feature size of SIROF after laser ablation (Fig 5.5). The RMS surface roughness for as-deposited SIROF, and laser-ablated samples using both the A+P and Parylene-only encapsulation process were measured to be 39.0 nm, 38.3 nm, and 41.0 nm, respectively. The surface roughness after ablation was similar to as-deposited SIROF. However, compared with the bi-layer coated SIROF (Fig 5.5 (a)), Parylene-only coated samples (Fig 5.5 (b)) had slightly larger and more rounded “grain” features, consistent with a melted appearance. Both of them were bigger than that of as-deposited SIROF. The heat from laser ablation and lack of shielding alumina layer led to the melting of SIROF and formation of bigger grain size for Parylene coated SIROF.

Following the laser ablation, O<sub>2</sub> RIE process was utilized to remove the carbon residue, and BOE was used to remove alumina to expose the underlying SIROF. XPS was utilized to confirm the BOE etching of alumina. XPS spectra were collected using a Kratos Axis Ultra DLD instrument with monochromatic Al-K $\alpha$  radiation operated at 180 W and 15 kV. The XPS was used in small spot analysis mode to facilitate measurements during depth profiling, and utilized a spot size was  $110 \times 110 \mu\text{m}^2$ . Table 5.1 presents the surface composition (at %) of the alumina coated SIROF as a function of room temperature BOE etching time. Fig 5.6 presents the XPS spectra of alumina coated SIROF before and after BOE etching. For the alumina coated SIROF, presence of Al 2p peak and absence of Ir 4f peak (Fig 5.6 (a)) suggest a pin-hole free and conformal alumina coating. Both alumina and iridium were detected after 5 minutes of BOE etching

(Table 5.1). No Al 2p peak was observed after 8 minutes of BOE etching and Ir 4f peak was detected due to the exposure of SIROF (Fig 5.6 (b)), suggesting that alumina was completely removed. The etch rate of alumina was roughly  $8 \pm 1$  nm/minute. Fig 5.6 (c) and (d) compared the Ir 4f peak for SIROF before (as-deposited) and after BOE etching. The similarity of those two peaks implied that BOE etching did not chemically affect the SIROF. This is consistent with SEM observations, and also consistent with the electrochemical characterizations presented below.

The CIC density ( $\text{mC}/\text{cm}^2$ ), CSC density ( $\text{mC}/\text{cm}^2$ ), and electrochemical impedance ( $Z$  ( $\Omega$ )) of SIROF were measured after each step of deinsulation process: 1) laser ablation, 2) oxygen plasma etching, and 3) BOE etching, and compared to measurements from Parylene-only control samples.

Higher charge injection capacity (CIC) is needed to allow smaller electrodes to evoke a response and induce minimal tissue damage by injecting higher stimulation current while operating within safe voltage limits. Electrode materials with higher CIC can improve selectivity without compromising sensitivity. The CIC of A+P coated SIROF was low after laser ablation and oxygen plasma process steps, and then increased significantly from 100 nC to 325 nC after BOE etching for area of  $2 \times 10^{-4} \text{ cm}^2$  ( $1.6 \text{ mC}/\text{cm}^2$ ), as presented in Table 5.2. The low CIC after laser ablation (100 nC) resulted from the existence of carbon residual and alumina coating on the SIROF surface. A slight increase in CIC after oxygen plasma etching resulted from the removal of carbon residual, and is consistent with previously reported results [40]. The CIC increased significantly after BOE etching (from 100 to 325 nC) due to the complete removal of alumina. For Parylene C coated SIROF control samples with the same area, the CIC was



75 nC after laser ablation. The CIC increased dramatically to 225 nC after oxygen plasma etching because of the successful removal of carbon residual on the surface. The BOE etching did not significantly affect CIC (from 225 to 240 nC ( $1.2 \text{ mC/cm}^2$ )) of Parylene coated SIROF. The higher CIC density of A+P coated SIROF is attributed to protection of the SIROF by alumina during the laser ablation process. Microcracks, reduction, and damage to SIROF films have been observed during laser deinsulation processes. We believe the alumina film is acting as a capping layer to prevent reduction of the  $\text{IrO}_x$  film, and is also absorbing some portion of the laser flux, thereby protection the underlying film.

Charge storage capacity (CSC) is a measure of charge available at near equilibrium condition. The CSC of SIROF using A+P and Parylene-only encapsulation were also measured after each step in the etching process, as presented in Fig 5.7. The CSC was 4.2 mC for fully deinsulated A+P coated SIROF and 3.4 mC for postetched Parylene coated SIROF for an area of  $2 \times 10^{-4} \text{ cm}^2$ . A+P coated SIROF had significantly lower CSC before BOE etching due to the presence of alumina on the surface of SIROF. For Parylene coated SIROF, CSC increased slightly after using oxygen plasma to remove the carbon residual and was identical before and after BOE etching. This indicated that BOE did not impact the electrochemical properties of SIROF.

The impedance of SIROF was also characterized using electrochemical impedance spectroscopy (EIS), and data from all steps of the deinsulation process from both encapsulation methods are presented in Fig 5.8. Impedance at 1 kHz, a characteristic frequency for action potentials, is reported in Table 5.3 at the three different stages of the etching process. For SIROF with Parylene coating and A+P coating, the impedance at 1

kHz after laser ablation of Parylene was 12 k $\Omega$  and 48 k $\Omega$ , respectively, for an area of  $8 \times 10^{-5}$  cm<sup>2</sup>. The relatively high impedance was due to the existence of carbon residual (for both Parylene coating and A+P coating) and alumina (for A+P coating only) on the surface. After oxygen plasma etching, the impedance of Parylene-only encapsulation decreased to 4.5 k $\Omega$ . The impedance for A+P encapsulation only decreased slightly to 41 k $\Omega$ , but it was much higher than Parylene coated SIROF, because of the presence of the alumina layer. After BOE etching, the impedance and its phases for SIROF with two different coatings were almost identical at  $\sim 4.7$  k $\Omega$ , which suggested the effective removal of alumina for A+P coated SIROF. Also, Parylene coated SIROF had almost the same impedance and phase before and after BOE etching, implying BOE did not have an effect on the electrochemical characteristics of the SIROF. This is consistent with the findings from XPS analysis. The fully deinsulated Parylene coated and A+P coated SIROF had very similar impedance and phase.

The tip of the Utah electrode array after laser ablation, oxygen plasma, and BOE etching is shown in Fig 5.9. The tip exposure was about 35  $\mu$ m. The electrode impedance values are presented in Fig 5.10. Impedance values for most of the tips are from 20 to 50 k $\Omega$ , which are good for neural interface applications, and consistent with previously reported data for this tip deinsulation length [5]. The impedance values are relatively stable, with median of 32 k $\Omega$  and standard deviation of 30 k $\Omega$ , compared with what Hsu *et al.* reported with standard deviation up to 50 to 100 k $\Omega$  [5]. The stability of impedance implies the relative consistency of the tip exposure because impedance is very sensitive to tip exposure variation. The ability to control tip exposure is one of the significant

advantages for laser-based deinsulation technique. The variation of tip impedance could result from electrode nonuniformity during the array fabrication.

### 5.5 Conclusion

A self-aligned three-step etching process for alumina and Parylene C coated Utah electrode array, utilizing laser ablation, oxygen plasma and BOE etching, was successfully demonstrated. The alumina was found to prevent the formation of microcracks in the underlying iridium oxide during laser ablation. The removal of alumina and Parylene C was confirmed by XPS spectra, with an etching rate of 8 nm/minute for BOE etching of alumina. Chronopotentiometry, cyclic voltammetry, and EIS were used to characterize the electrochemical properties of deinsulated SIROF. Compared with Parylene-only encapsulation, the SIROF with A+P encapsulation had higher CIC density (240 vs 320 nC), higher CSC (3.4 vs 4.2 mC) and similar impedance (2.5 vs 2.5 k $\Omega$ ) for an area of  $2 \times 10^{-4}$  cm<sup>2</sup>. Three-step deinsulated electrodes of Utah electrode array with bi-layer coating had median impedance of 32 k $\Omega$  with standard deviation of 30 k $\Omega$ . This is more uniform compared with electrode impedance (standard deviation up to 100 k $\Omega$ ) obtained through oxygen plasma etching using aluminum foil as mask. Due to its self-aligning nature, this three-step deinsulation method can be applied to many other biomedical implantable devices that require selective etching of the encapsulation.



Fig 5.1 Scanning electron micrograph of the UEA with 100 (10 by 10) silicon electrodes.

The electrode length is 1.5 mm and space between electrodes is 400  $\mu\text{m}$ .

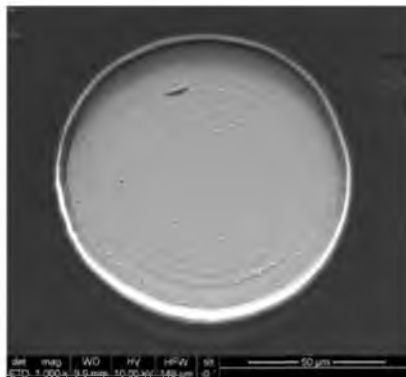


Fig 5.2 SEM picture of a test structure after three-step deinsulation: laser ablation, oxygen plasma etching, and BOE etch.

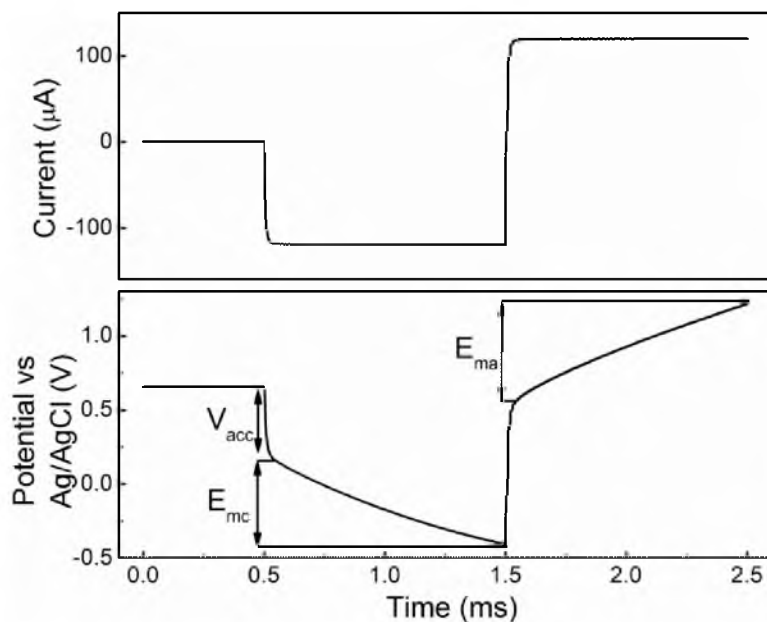


Fig 5.3 Voltage transient of fully deinsulated SIROF in response to the cathodal first, charge balanced biphasic current pulse in PBS. The iridium oxide working electrode, Ag/AgCl reference electrode, and platinum counter electrode were immersed in PBS. The current pulse amplitude was 100  $\mu\text{A}$  with length of 1 ms. The figure illustrates the maximum cathodic potential ( $E_{mc} = -0.6\text{V}$ ) and maximum anodic potential ( $E_{ma} = 0.7\text{V}$ ) during the pulse. The charge injection capacity was obtained by integrating current with time.

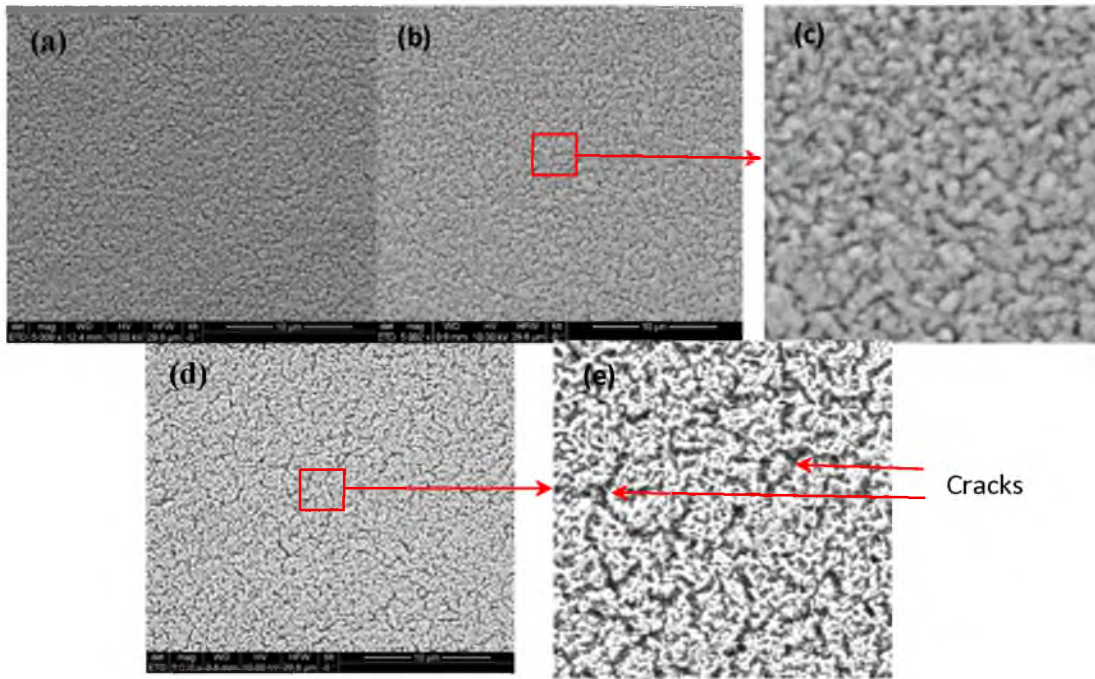


Fig 5.4 SEM micrographs of (a) as-deposited SIROF, (b) alumina, and Parylene C bi-layer coated SIROF after laser ablation and (d) Parylene C coated SIROF after laser ablation. (c) and (e) are the detailed views of (b) and (d), respectively. Microcracks were clearly observed for Parylene coated SIROF after laser ablation.

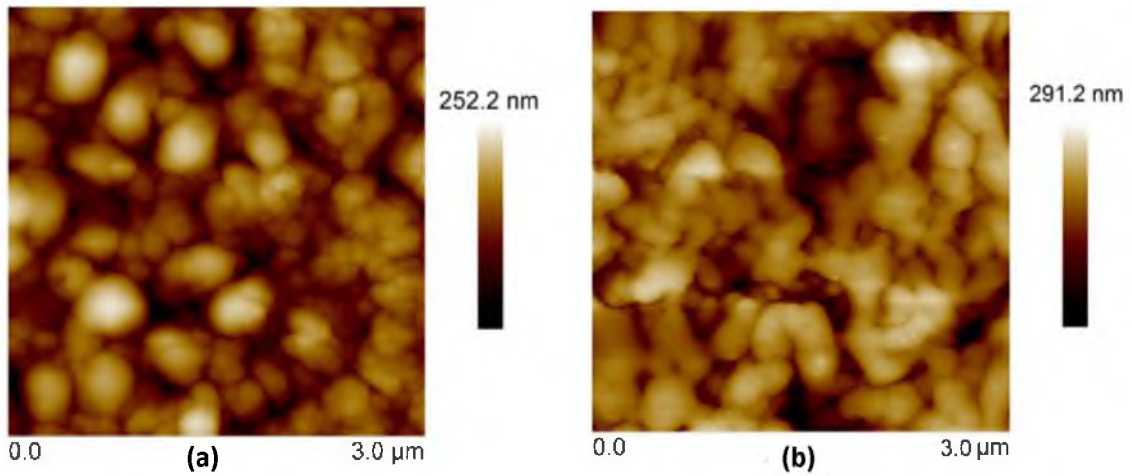


Fig 5.5 AFM micrographs of (a) alumina and Parylene C coated SIROF after laser ablation, and (b) Parylene C coated SIROF after laser ablation. The A+P coated SIROF had smaller grain size and less melt compared with Parylene coated SIROF.

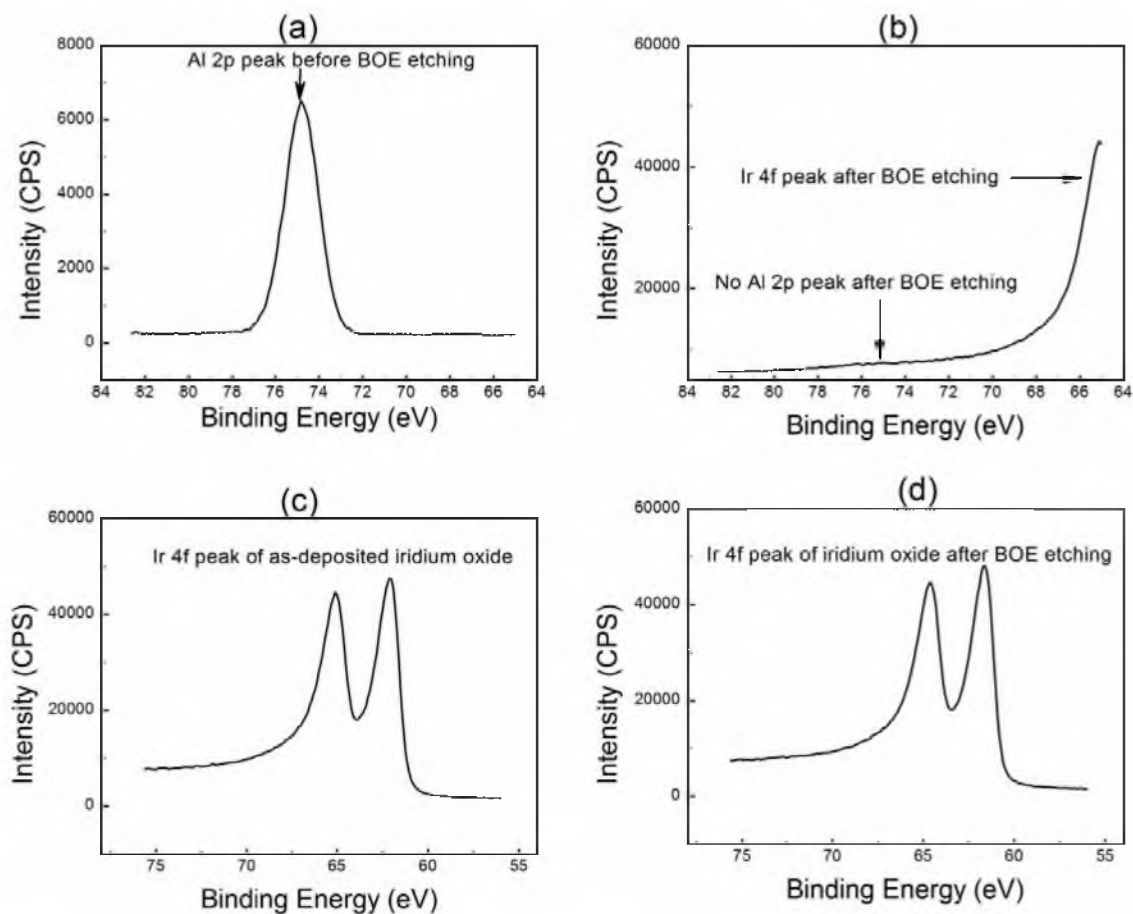


Fig 5.6 XPS spectra of (a) Al 2p peak for alumina coated SIROF, (b) Al 2p peak for alumina coated SIROF after 8 minutes of BOE etching, (c) Ir 4f peak for as-deposited SIROF, and (d) Ir 4f peak for alumina coated SIROF after 8 minutes of BOE etching. Alumina was completely etched away and iridium oxide was exposed after 8 minutes of BOE etching. Also, as deposited SIROF has a similar Ir 4f peak character compared with SIROF after 8 minutes of BOE etching, suggesting that the three-step deinsulation process did not chemically affect the SIROF.



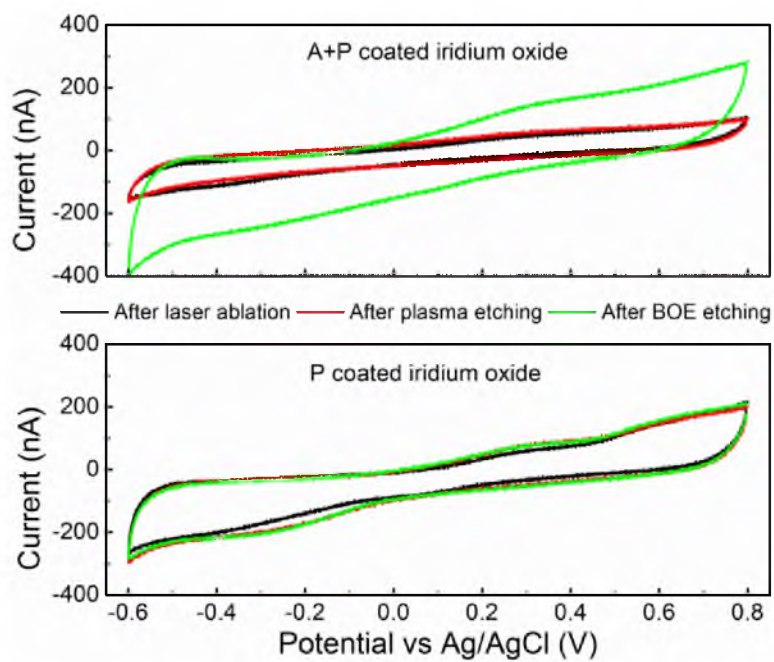


Fig 5.7 The voltammogram of iridium oxide with A+P (alumina and Parylene) and P (Parylene) coating after sequential etching processes of laser ablation (black), oxygen plasma (red), and BOE (green). The scan rate was 50 mV/s.

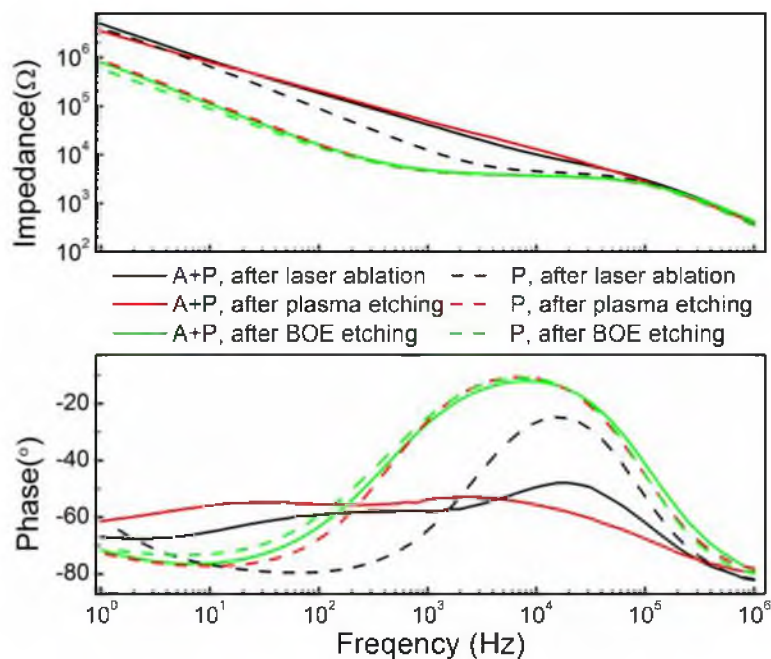


Fig 5.8 Bode plots of electrochemical impedance for SIROF with an area of  $8 \times 10^{-5} \text{ cm}^2$ . Impedance for Parylene coated SIROF dropped significantly after oxygen plasma and stayed almost the same after BOE etching. Impedance for A+P coated SIROF decreased slightly after oxygen plasma and reached the same level with Parylene coated SIROF after BOE etching.

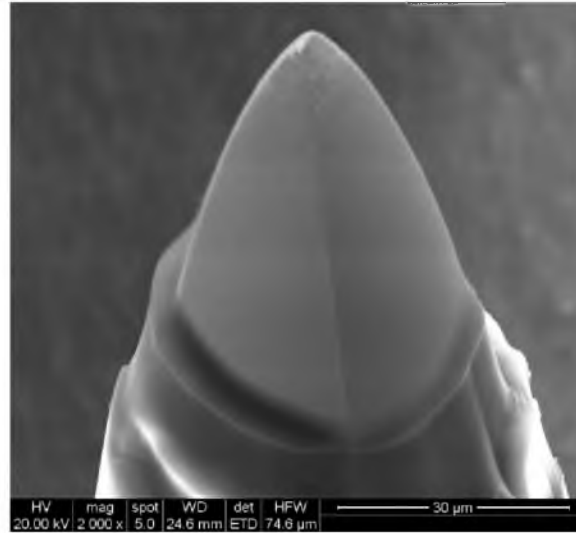


Fig 5.9 Alumina and Parylene C coated tip of Utah electrode array after laser ablation, oxygen plasma etching, and BOE etching.

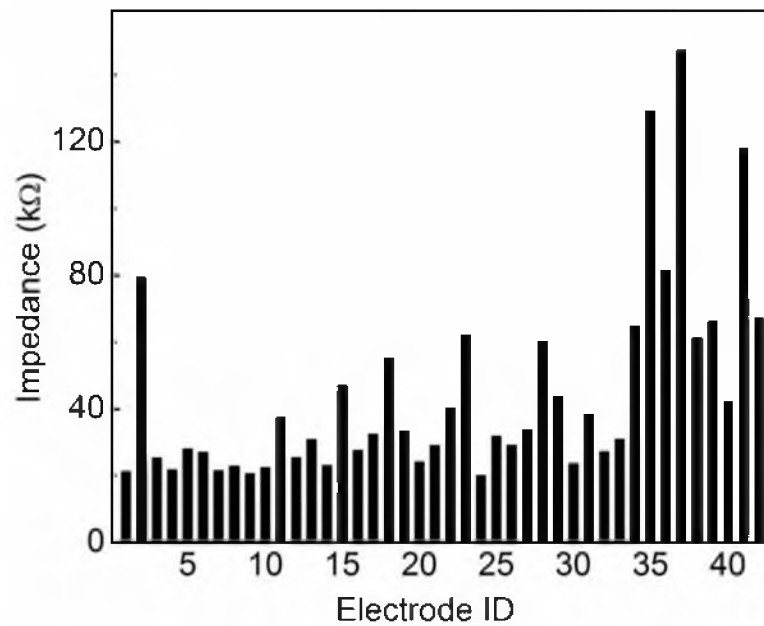


Fig 5.10 Impedance of A+P coated electrodes from Utah electrode array after laser ablation, oxygen plasma, and BOE etching. Typical tip exposure is around 30  $\mu\text{m}$ . The impedances are mostly in the range of 20 to 50  $\text{k}\Omega$ .

Table 5.1 Surface composition (at %) measured by XPS as a function of BOE etching of 52 nm alumina coated SIROF. No Al was detected after 8 minutes of BOE etching.

BOE Etch time (minutes)	O 1s	C 1s	Al 2p	Ir 4f
0	54.41	1.06	44.53	0
5	57.40	0	30	14.70
8	44.98	0	0	55.02

Table 5.2 CIC (in nC) of SIROF with A+P and P coating after sequential etching processes of laser ablation, oxygen plasma, and BOE. The CIC for A+P coated SIROF was higher than that of P coated SIROF. Also, CIC for A+P coated SIROF was increased significantly after BOE etching. The number of samples measured in each condition was 3 (N=3).

Area (cm <sup>2</sup> )	CIC unit	A+P, laser	P, laser	A+P, oxygen plasma	P, oxygen plasma	A+P, BOE	P, BOE
$2 \times 10^{-5}$	nC	8	8	10	23	27	23
$8 \times 10^{-5}$	nC	8	25	8	100	120	110
$2 \times 10^{-4}$	nC	75	220	100	225	325	240

Table 5.3 Impedance at 1 kHz (k $\Omega$ ) of iridium oxide with A+P (alumina and Parylene) and P (Parylene) coating after sequential etching processes of laser, oxygen plasma, and BOE. SIROF with Parylene coating and A+P coating had very similar impedance after BOE etching.

Area (cm <sup>2</sup> )	Impedance	A+P, laser	P, laser	A+P, oxygen plasma	P, oxygen plasma	A+P, BOE	P, BOE
$2 \times 10^{-5}$	k $\Omega$	104	43	34	15	13	14.5
$8 \times 10^{-5}$	k $\Omega$	48	12	41	4.5	4.8	4.6
$2 \times 10^{-4}$	k $\Omega$	7.3	2.9	4.9	2.7	2.5	2.5

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## CHAPTER 6

### LONG-TERM RELIABILITY OF $\text{Al}_2\text{O}_3$ AND PARYLENE C BI-LAYER ENCAPSULATED UTAH ELECTRODE ARRAY-BASED NEURAL INTERFACES FOR CHRONIC IMPLANTATION

#### 6.1 Abstract

The long-term stability and functionality of neural interfaces is a significant challenge for their chronic implantation and use. We evaluated the long-term reliability of Utah electrode array (UEA) based neural interfaces encapsulated by atomic layer deposited (ALD)  $\text{Al}_2\text{O}_3$  and Parylene C, and compared these to devices with the baseline Parylene encapsulation. The wired and wireless UEAs were coated with 52 nm of ALD  $\text{Al}_2\text{O}_3$  and 6  $\mu\text{m}$  of Parylene C and immersed in phosphate saline solution (PBS) at 57 °C for accelerated lifetime testing. The median tip impedance of the bi-layer encapsulated wired UEAs increased from 60 k $\Omega$  to 160 k $\Omega$  during the 960 days of equivalent soak testing at 37 °C, the opposite trend as typically observed for Parylene encapsulated devices. The loss of the iridium oxide tip metallization and etching of silicon in PBS solution contributed to the increase of impedance. The lifetime of wireless UEAs were also tested using accelerated lifetime measurement techniques. The bi-layer coated devices had

stable power-up frequencies at ~910 MHz and constant RF signal strength of -50 dBm during up to 1044 days (still under testing) of equivalent soaking time at 37 °C, indicating their continue function *in vitro*. This is much of a significant improvement over the lifetime of 5 months achieved with Parylene-only encapsulation. The bi-layer coated “active” UEA with a flip-chip bonded ASIC chip had a steady current draw of ~ 3 mA during 228 days of soak testing at 37 °C and was implanted for *in vivo* experiment. The trends for increasing electrode impedance and performance stability of wireless devices support the significantly greater encapsulation performance of this bi-layer encapsulation compared with Parylene-only encapsulation.

## 6.2 Introduction

Implantable neural interfaces have been widely investigated, and also used to diagnose and treat neural disorders in both research and clinical applications [1-6]. The Utah electrode array (UEA) is a well-developed and FDA-cleared example of this technology for stimulating/recording multiple neurons simultaneously with good selectivity [5, 7-9]. Traditionally, UEAs use gold wire bundles and percutaneous connectors to transfer recording/stimulation signals. However, wire bundles are more likely to cause foreign body response [10] and promote infections [11] for chronic implantation. In addition, percutaneous connectors commonly contribute to infections, and have been found to be one of the least reliable elements of neural interfaces [12]. Therefore, tremendous efforts have been devoted to develop neural interfaces with wireless transmission of power and data [13-18] to eliminate wire bundles. Fully

integrated wireless neural interfaces based on UEA have been developed with recording and stimulating capabilities from 100 channels [16, 18].

Both wired and wireless neural interfaces are designed to function *in vivo* for years for chronic implantation. Factors that compromise the performance of chronic neural interfaces can include physiological reasons (such as foreign body responses) and device failure modes (encapsulation failure). Encapsulation failure can lead to short circuits, corrosion of components, and interconnects, which are often catastrophic especially for wireless neural interfaces with integrated active electronics. The significant bias voltages associated with integrated electronics further challenges thin film encapsulation by activating degradation modes and accelerating ion transport. Protecting implanted devices has typically utilized hermetic enclosures and thin film encapsulation approaches. Lids and metal cans are used to seal implantable devices, e.g., deep brain stimulators and pacemakers [19], in order to protect them from the physiological environment. Device miniaturization and electromagnetic power and data schemes raised new challenges for traditional hermetic encapsulation. Thin film encapsulation methods have been widely developed, and can be used for small implants, and compatibility with electromagnetic wireless techniques. Different materials have been investigated for coating of neural interfaces, including polyimide[20], Parylene [21, 22], silicone[23], amorphous silicon carbide [24, 25], silicon nitride [25], and diamond-like carbon (DLC) [26]. Finding one material that meets all the requirements for coating neural interfaces is extremely difficult. For example, silicon nitride slowly dissolves in PBS[25]; amorphous silicon carbide and DLC need relatively high deposition temperatures that are not compatible with devices; polyimide is very difficult to deposit uniformly.

Parylene C has been widely used as coating material for biomedical implantable devices [22, 27-29] due to attractive properties including chemical inertness, low dielectric constant ( $\epsilon_r=3.15$ ) [30], high resistivity ( $\sim 10^{15} \Omega \cdot \text{cm}$ ), and relatively low water vapor transmission rate (WVTR)  $0.2 \text{ g} \cdot \text{mm}/\text{m}^2 \cdot \text{day}$  [31]. It can be deposited by CVD at room temperature to generate a conformal and pin-hole free film that does not require use of solvents to form. Parylene is also a good ion barrier [32], which is critical for neural interfaces exposed to physiological fluids.

Parylene cracking has been observed during *in-vivo* experiment [33]. Failure of Parylene C encapsulation has also been reported [34] due to moisture diffusion and interface contamination. Surface contaminants or voids between substrate and encapsulation are required for the nucleation of moisture into liquid water. To overcome the condensation of moisture around interface contaminants, a highly effective moisture barrier can be introduced between the neural interface and Parylene film. Atomic layer deposited (ALD) alumina is an excellent moisture barrier with WVTR in the order of  $\sim 10^{-10} \text{ g} \cdot \text{mm}/\text{m}^2 \cdot \text{day}$  [35-38], and is extremely conformal, allowing it to passivate difficult to cover surfaces. However, alumina alone is not a suitable encapsulation since it dissolves in water [39], which allows body fluids to contact with encapsulated device easily. The alumina-Parylene C bi-layer encapsulation has demonstrated excellent insulation performance on planar interdigitated electrode (IDE) test structures for years of equivalent lifetime in accelerated soak testing [40]. This approach combines the highly effective moisture barrier properties of ALD  $\text{Al}_2\text{O}_3$ , and Parylene C as an ion barrier and for preventing contact between alumina and liquid water. Test structures are good for optimizing the properties and conditions to get good films, but there are also issues of

how to use this with real systems. The complex geometry (gold coils and SMD capacitors), different materials and surfaces, and additional processing steps (oxygen plasma etching, BOE etching) involved in neural interfaces are not fully represented in IDE test structures and therefore might severely affect the actual lifetime of the bi-layer encapsulated neural interfaces.

In this paper, we evaluated the long-term reliability of ALD  $\text{Al}_3\text{O}_3$  and Parylene C bi-layer coated UEA-based neural interfaces. The bi-layer encapsulated neural interfaces were submerged in PBS at 57 °C for accelerated lifetime testing. The encapsulation performance was evaluated from a few different aspects: electrode tip impedance, wireless powering up frequency and signal strength, and current draw level, using different specifically designed neural interface configurations.

### 6.3 Experimental Details

#### 6.3.1 Integrated Neural Interfaces

Three different configurations of UEA-based neural interfaces were used to evaluate the alumina and Parylene C bi-layer encapsulation performance. Traditional wired UEAs, fully integrated wireless arrays, and *Active Arrays* were used to measure from three different aspects: long-term impedance stability, long-term wireless signal strength and frequency stability, and the level of current draw, respectively. Fabrication and testing procedures used to evaluate the encapsulation are presented in this section.

The UEA was first designed and fabricated by Normann for intracortical stimulation [41]. A dicing saw was used to cut silicon wafers and create columns with dimension of 150  $\mu\text{m}$  square, 1.5 mm tall, and pitch of 400  $\mu\text{m}$ . The columns were first thinned and

then tapered by wet etching. The fabrication details of UEAs are described elsewhere [41, 42]. Wired UEAs were used to evaluate the electrode impedance stability over time. UEAs were wire bonded (West Bond, Inc.) to a 96-channel TDT connector using 1 mil insulated gold wire with a wirebundle length of 10 cm for long-term tip impedance measurements (Fig 6.1). The fabrication details of the UEA can be found elsewhere [41, 42]. Silicone (MED 4211, NuSil Technology) was applied to the backside of the array and the wire bundle to secure the bond connection, increase the strength of the wire bundle, and further protect the array from handling forces and fluid ingress.

The performance of the encapsulation was further tested by using wireless integrated neural interfaces, and soaking these in PBS under accelerated conditions. The ability to power the devices inductively, and the associated telemetry frequency on power-up, and the RF signal strength were used as sensitive metrics for the encapsulation performance and fluid ingress. This device uses a 100-channel wireless neural recording IC, designated as INIR-6 (integrated neural interface recording version-6), that was fabricated with 0.6  $\mu\text{m}$  BiCMOS process (X-fab semiconductors). The details of the chip design, fabrication, characterization, and system integration were reported elsewhere [16, 18, 43]. An INIR-6 chip with capabilities of signal processing and data telemetry was flip-chip bonded to the backside of a 10 $\times$ 10 UEA using Au/Sn reflow soldering. Two SMD capacitors were soldered to the backside of UEA and connected to the chip via backside metal traces. One SMD was part of the resonating circuit for inductive powering and the other was a smoothing capacitor for the DC power supply. A flat spiral coil of 5.5 mm in diameter was manufactured by winding an insulated 2-mil Au (1% Pd) wire [44]. The gold coil was wire-bonded to form the resonating circuit around 2.765 MHz with the

SMD capacitor for inductively powering up the device. The fully integrated wireless INI is shown in Fig 6.2.

An *active array*, another version of neural interfaces, was built to monitor the current draw of neural interfaces over time under soak testing, as show in Fig 6.3. The details of *active arrays* were reported elsewhere [45]. It was similar to the wireless neural interfaces with a flip-chip bonded ASIC for on-site signal processing. Instead of inductive powering and wireless communication, the *active array* used 16 wire-bonded gold wires for data transferring and powering. In this way, the current draw between power rails can be directly monitored through a current meter.

### 6.3.2 Alumina and Parylene C Deposition

52 nm of  $\text{Al}_2\text{O}_3$  was deposited by plasma-assisted (PA) ALD on integrated neural interfaces at a substrate temperature of 120 °C which is within the thermal budget for the materials for the three array variants used. Details of the deposition process have been previously reported [40]. A-174 (Momentive Performance Materials), an organosilane, was used as adhesion promoter between the alumina and Parylene C layer. A 6- $\mu\text{m}$  thick Parylene-C layer was deposited by CVD using the Gorman process [30] on top of  $\text{Al}_2\text{O}_3$  as the external coating layer. For wired neural interfaces, the connectors were covered with aluminum foil to avoid coating the contact pads on the connectors.

### 6.3.3 Tip Deinsulation

The encapsulation must be removed from the active tip electrodes sites for neural recording and stimulation. Traditionally, oxygen plasma reactive ion etching (RIE) was used to remove the Parylene C on the tips by poking the tips through aluminum foil. This

method does not etch alumina. A hybrid method using a combination of laser ablation and O<sub>2</sub> RIE was utilized to etch Parylene C layer and buffered oxide etch (BOE) was used to remove the thin alumina film.

The challenges include controlling the tip exposure with an uneven backside during the poking process, especially for Utah Slant Electrode Arrays (USEAs). An Optec Micromaster excimer laser micromachining system was first used for ablation of Parylene C. 200 laser pulses with fluence of 1400 mJ/cm<sup>2</sup> were applied with 5 ns pulses at 100 Hz to selectively remove the outer Parylene C film from the electrode tips. The alumina layer underneath Parylene acted as a shield layer, protecting the tip metal (iridium oxide) from being damaged by excess heat from laser. The laser deinsulation process results in carbon residual redeposition on the surface, which was removed by utilizing 2 minutes of O<sub>2</sub> RIE. Alumina was etched by dipping the array into BOE for 8 minutes. Parylene C acted as a mask layer for BOE etching and removal of alumina happened only in the area where Parylene was removed by laser, generating a self-aligned process. The tip exposure was about 35 μm. The lifetime metrics of these devices were then tested by placing them in PBS solution under accelerated testing conditions.

#### 6.3.4 Testing Setup

Wired arrays were used for long-term impedance measurements, and were soaked in 1× PBS (0.01 M phosphate buffer, 0.0027 M KCl and 0.14 M NaCl) at 57 °C for accelerated lifetime testing. The estimated aging factor (Q) was 4, based on a broadly recognized trend in accelerated aging, and results in a doubling reaction kinetics for each 10 °C increase in reaction temperature [46, 47]. The PBS solution was changed every other week to minimize changes in the composition (ion concentrations), and their effects



on impedance. Tip impedance was measured by connecting the TDT connector with a customized automated impedance tester (AIT), using two platinum wires as reference and counter electrodes [48]. The tip impedance measurement is obtained by electrically connect all nontested electrodes to ground potential, which is different from conventional impedance, where all nontested electrodes are electrically floating. The impedance tester automatically switches between channels and measures impedance for all channels at 1 kHz with a 10 mV sine wave. The measurable impedance range for AIT is 300  $\Omega$  - 10 M $\Omega$ .

For wireless neural interface testing, the arrays were fully submerged in 6-ml glass vials filled 1 $\times$  PBS solution at  $57 \pm 0.5$  °C in water baths. The wireless neural interfaces were powered by a customized inductive power board at 2.765 MHz that has been previously reported [16]. The presence of the 900-MHz ISM-band telemetry signal, the frequency of that signal on startup, and RF signal strength from INIR-6 chip were monitored using the custom receiver board interfaced through Matlab and with a spectra analyzer [16].

The *active arrays* were also soaked in glass vials filled with 1 $\times$  PBS solution at 57 °C. The *active arrays* were powered up only during the measurement of current draw. The current draw of the ASIC chip was measured with power supply of +1.5 V and -1.5 V to  $V_{dd}$  and  $V_{ss}$ , respectively.

#### 6.4 Results and Discussion

Impedance for the wired array was measured at 1 kHz using a 10-mV sine wave. These wired arrays have gone through the bi-layer process, and the associated hybrid

deinsulation process. Very high impedances (in M $\Omega$  range, 8 out of 50 electrodes) were excluded from the plot since this most often results from chipped-tips or broken electrodes. As shown in Fig 6.4, tip impedances were found to range from 30 to 100 k $\Omega$  for most electrodes, with a median impedance of 60 k $\Omega$ , which are good for neural interface applications, and consistent with previously reported data [22]. The nonuniformity of impedance results mostly from variation in tip exposure and manufacturing differences. The impedance of alumina and Parylene-coated UEAs stayed almost the same during equivalent soaking time of the first 120 days at 37 °C (nonaccelerated conditions), indicating good insulation of individual electrodes. Impedance for Parylene-only control samples consistently dropped significantly within a few weeks to 3 months [7, 49]. Table 6.1 compares the median of tip impedance for Parylene-only and bi-layer-coated UEAs. For the Parylene-only condition, the median tip impedance dropped from 81.9 k $\Omega$  to 40.5 k $\Omega$  within 3 days of soak testing. The significant impedance drop is most likely due to water ingress and degradation of the Parylene coating. For alumina and Parylene bi-layer coating, the median of tip impedance increased slightly from 61.1 k $\Omega$  to 73.8 k $\Omega$  within 3 days. As described below, etching of exposed silicon at the electrode tips and undercutting of the tip metallization is the mechanism for the increased impedance. Because this process is occurring in the Parylene-only condition as well, and the impedances are still found to decrease, this clearly suggests dramatically better performance for the bi-layer encapsulation. Ultimately, the relative change of the impedance is more important than the absolute value of the impedance. The absolute value of the impedance is pre-determined by factors

like the manufacturing process and tip exposure. The change of the impedance during soak testing is affected by the encapsulation performance and lifetime.

The tip impedance started increasing after 120 days of soak testing at 37 °C, as shown in Fig 6.4 and 6.5. The median of tip impedance was about 160 k $\Omega$  after 960 days of soak testing, which is about 2.5 times of the median impedance at the first day (60 k $\Omega$ ). This is the opposite trend of what we have observed from Parylene C coated tip impedance. Typically, impedance of Parylene C coated tips would decrease as a function of soaking time in a relatively short term (from days to a few months) due to water ingress and degradation of the coating [7, 49]. The increase in impedance of alumina and Parylene coated tips could be a combined effect of good encapsulation and loss of tip metal (iridium oxide) due to silicon etching in PBS. The good encapsulation performance of the bi-layer keeps the tip impedance relatively constant. The increase in tip impedance was most likely caused by the etching of silicon and loss of iridium oxide, which were confirmed by SEM images shown in Fig 6.6. It clearly shows that a large portion of the iridium oxide is gone on the deinsulated tip and there is a gap between the iridium oxide and silicon shank. It is well known that PBS etches silicon [50]. The removal of underneath silicon substrate led to free-standing iridium oxide. Loss of the fragile iridium oxide can happen easily due to lack of support. We started to see M $\Omega$  range impedance for ~ 5 electrodes and expect to see further increases in the impedance as more silicon is etched and more iridium oxide is lost. We have measured the impedance of the same silicon electrode tips without the tip iridium oxide metallization and the impedance was about 3-6 M $\Omega$ . This is consistent with what we have observed for those electrodes that have lost iridium oxide. Regarding to Parylene coated electrodes, the degradation of

encapsulation leads to decrease in impedance and loss of iridium oxide due to silicon etching would increase the impedance. The overall impedance drop of Parylene coated UEA indicates that the degradation of encapsulation dominates and offsets the impedance increase from tip metal loss. This also strongly indicates that alumina and Parylene bi-layer coating has better insulation performance than the Parylene-only coating.

Wireless integrated neural interface (INI) devices were soaked at 57 °C in PBS for 261 days, equivalent soak time of 1044 days at 37 °C and are still under soak testing to investigate the long-term reliability of alumina and Parylene C coated wireless INI devices. The experimental setup is shown in Fig 6.7. The receiving antennas for both the spectra analyzer and hand receiver were brought close to the reference wires of the INI device to get better RF reception. The INI device was about 8 mm away from the power coil, and the device was powered up only during testing. The presence of the signal, the startup frequency, and the RF signal strengths of the INI device at different soak time were compared in Table 6.2. If the encapsulation fails and water ingress occurs, then the device shorts out. Limited water ingress can also shift frequency. When the device was in air, the powered up frequency was at 910.5 MHz with RF signal strength of -80 dBm measured using a spectra analyzer. The RF signal strength increased to -75 dBm after the immersion of the device in PBS solution (Table 6.2). The custom-built hand receiver confirmed the increase of RF strength from -61 dBm to -47 dBm after submerging the device into PBS. The initial increase in RF signal strength is most likely due to the change of media from air to PBS solution, and has been observed previously. The discrepancies between the two RF signal strengths measured by spectra analyzer and hand receiver unit were expected due to the differences in antennas and electronics.

The long-term RF signal strengths and their corresponding frequencies are presented in Fig 6.8 as a function of soak time. The power-up frequency was continuously near 910 MHz and the RF signal strength was stable around -73 dBm (Fig 6.8 (b)) during the equivalent soaking time of 1044 days at 37 °C. The small fluctuations in RF signal strengths and respective frequencies could be caused by the environmental noises and different positions and distances between the reference wire and antenna. This represents a considerably longer soak test results compared with what Sharma *et al.* reported of a lifetime of 276 days (lasted ~ 500 days with unpolished data) at room temperature using Parylene as encapsulation [51]. The room temperature soak testing could be considered as a “decelerated” lifetime testing with aging factor of 0.35, which gave an equivalent lifetime of 100 days at 37 °C. The bi-layer coated devices are still under soak testing and are expected to last much longer than the time they have already been under soak testing based on the results for interdigitated electrode test structures [40]. The long-term stability of power-up frequencies and RF signal strengths of the device implied the good insulation of the alumina and Parylene C bi-layer encapsulation for biomedical implantable devices.

The current draw level is an important metric for evaluating the performance of encapsulation for devices with active electronics. The wireless INIs were not capable of measuring the current; therefore, another version of UEAs with flip-chip bonded ASIC chips (without wireless capability) on the backside was used to monitor the current drawing of the device over time under soak testing [45]. From experience, increasing current draw from these devices was a reliable indicator of encapsulation failure, and one of the dominate failure modes for the devices. The device was powered up by a pair of

1.5 V batteries through wire-bonded gold wires.  $V_{dd}$  and  $V_{ss}$  are both 1.5 V away from a common ground potential. The relatively high voltages ( $\pm 1.5V$ ) are more likely to accelerate electrochemical reactions and degradation modes. The current drawing of  $V_{dd}$  and  $V_{ss}$  was measured through a current meter. The current draw was stably about 3 mA for both  $I_{dd}$  (from  $V_{dd}$ ) and  $I_{ss}$  (from  $V_{ss}$ ) during the 228 equivalent days of soak testing at 37 °C, as shown in Table 6.3. Also, all the 96 channels of the neural interface had low noise level. The low but constant current drawing of the INI indicated the good protection of alumina and Parylene coating because failure of encapsulation would induce high current draw due to the formation of leakage current paths and electrochemical corrosion processes.

### 6.5 Conclusion

In summary, we have demonstrated the long-term reliability of ALD alumina and Parylene C coated neural interfaces from three different aspects: impedance, RF signal stability and strength, and current draw, which are all directly affected by the encapsulation performance. Median impedances of alumina and Parylene coated wired arrays increased from 60 k $\Omega$  to 160 k $\Omega$  after 960 equivalent days of soak testing at 37 °C, due to the loss of iridium oxide and etching of silicon in PBS solution. Bi-layer coated wireless neural interfaces incorporated with active electronics had stable power-up frequency and constant RF signal strength over 1044 days of soak testing at 37 °C, showing the excellent insulation performance of alumina and Parylene C coating. Based on the coating performance on neural interfaces, it is believed that this bi-layer

encapsulation can be used for many other chronic biomedical implantable devices to improve the lifetime of those devices.

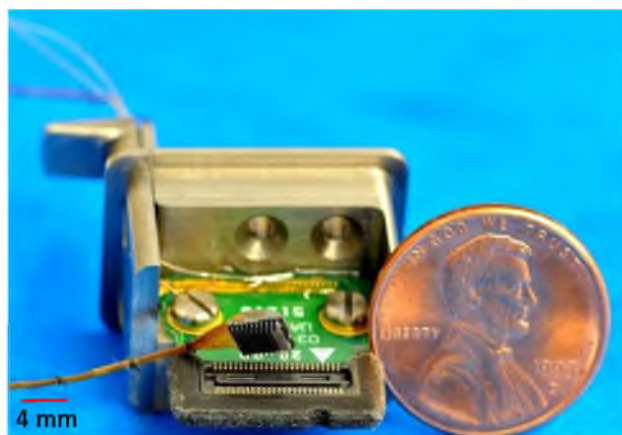


Fig 6.1 Fully assembled wired Utah electrode array with connector for impedance measurement. The Ti pedestal is part of the connector system.

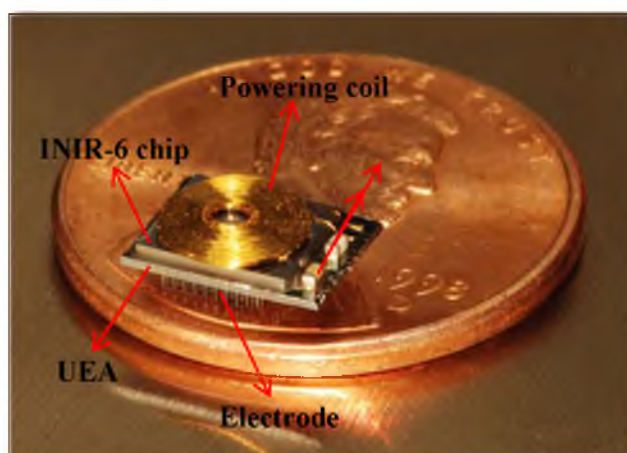


Fig 6.2 Utah array-based fully integrated wireless neural interfaces, with flip-chip bond INIR-6 and gold coil for inductive powering.

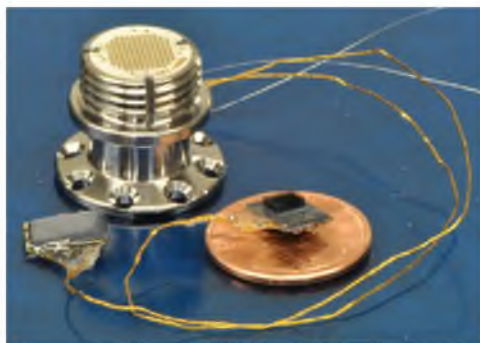


Fig 6.3 An *Active Array Assembly* that includes 2 arrays and 2 reference wires connected to a single Neuroport.

Table 6.1 The median impedance for Parylene coated UEA and alumina and Parylene bi-layer coated UEA for 3 days of soak testing in PBS. The median impedance dropped ~ 50% after 3 days in PBS for Parylene coated UEA while it increased slightly for alumina and Parylene coated UEA.

Soak time	Median impedance for Parylene coated UEA (k $\Omega$ )	Median impedance for bi-layer coated UEA (k $\Omega$ )
1 day	81.9	61.1
3 days	40.5	73.8



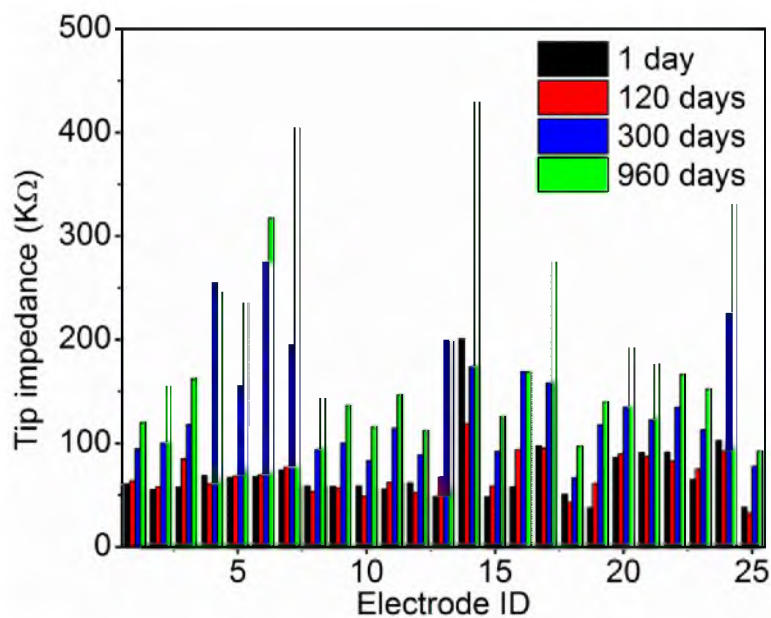


Fig 6.4 Electrode impedance of alumina and Parylene bi-layer coated wired arrays over time. Only 25 out of 50 tip impedances were shown due to the limited space. Median impedance was 60 kΩ. The impedance stayed almost the same for each electrode over the first 120 days at 37 °C, and increased ~ 2.5 times (calculated from median impedance) after 960 days of soak testing in PBS.

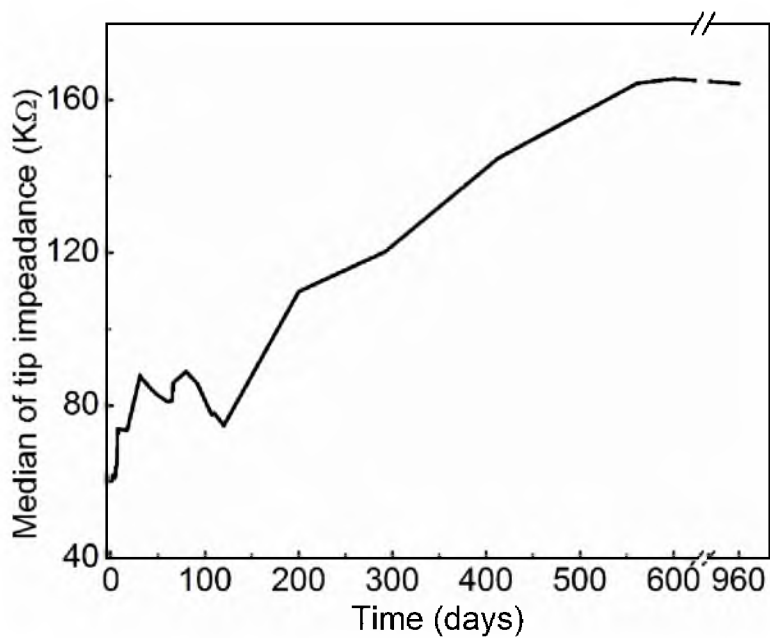


Fig 6.5 Median tip impedance over time at 37 °C in PBS. The median of impedance stayed relatively stable after 120 days of soak testing and then started to increase over soaking time.

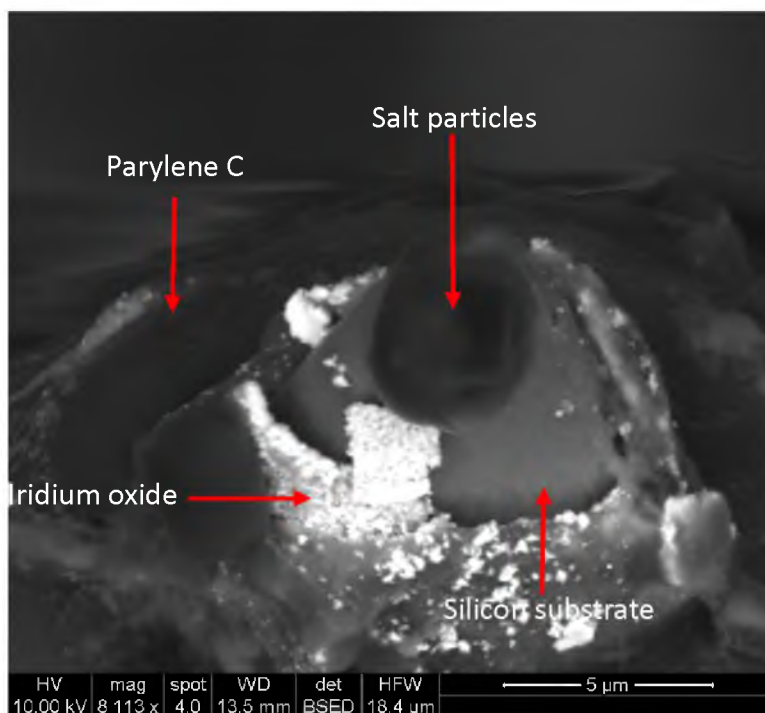


Fig 6.6 Backscattered SEM micrograph of electrode tip after 960 days of soak testing at 37 °C. Silicon underneath iridium oxide (tip metal) was etched by PBS solution and iridium oxide was peeled off from the tip.

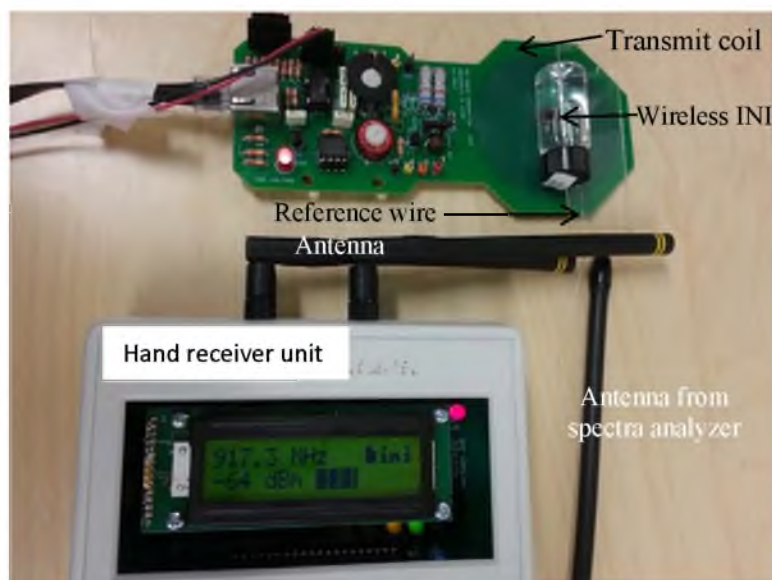


Fig 6.7 Experimental set-up for wireless integrated neural interface testing. The antennas were brought close to the reference wire from the INI device. The device is  $\sim 8$  mm away from the power board.

Table 6.2 Wireless radio-frequency (RF) signal strengths and frequencies of the wireless INIR-6 device measured through PBS solution using a customized wireless hand receiver unit and a spectra analyzer.

Soak time	RF signal from hand receiver		RF signal from spectra analyzer	
	Frequency (MHz)	Signal Strength (dBm)	Frequency (MHz)	Signal Strength (dBm)
0 (in air)	910.5	-80	911.6	-61
1 day	910.5	-75	910.5	-47
300 days	910.3	-71	910.7	-51
1044 days	911	-72	910.8	-50

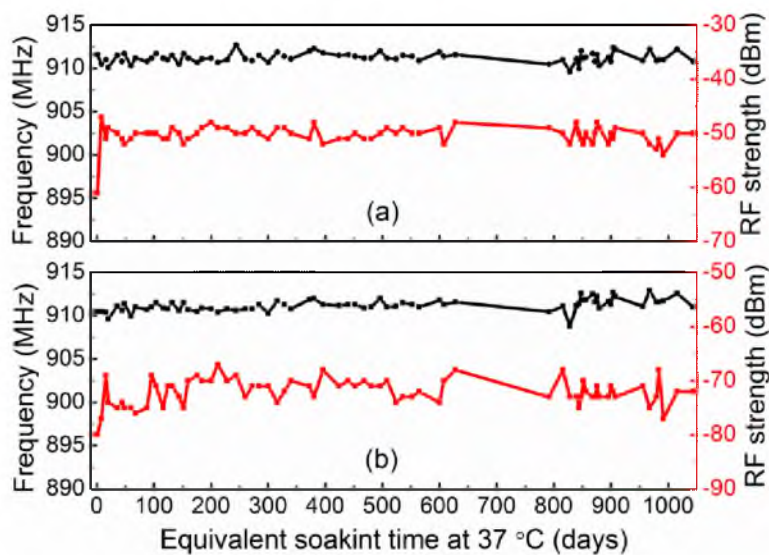


Fig 6.8 Transmitted wireless RF signal strength and frequency monitored as a function of soak time in PBS. (a) Peak RF signal strengths and the respective frequencies as extracted from the spectra measured using a spectrum analyzer. (b) RF signal strengths and the respective frequencies as monitored from a customized wireless hand receiver unit. In both measurement methods, the RF signal strengths and corresponding frequencies stayed relatively stable during the 1044 days of equivalent soak time at 37 °C.

Table 6.3 Current draw of *active array* measured from  $V_{dd}$  and  $V_{ss}$  as a function of soak time at 37 °C in PBS. The current draw was stable at  $\sim 3$  mA for  $I_{dd}$  and  $I_{ss}$  from  $V_{dd}$  and  $V_{ss}$ , respectively.

Soak time	$I_{dd}$ (mA)	$I_{ss}$ (mA)
0 (Agarose)	2.9	2.9
1 day	2.8	2.8
140 days	3.0	2.9
228 days	3.1	2.9

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## CHAPTER 7

### CONCLUSIONS AND FUTURE WORK

#### 7.1 Conclusions

The purpose of the research in this dissertation was to develop an encapsulation scheme that could be widely used for biomedical implantable devices. The requirements for the encapsulation of implantable devices include electrical insulation, corrosion protection, conformal and pin-hole free coating, low water vapor transmission rate (WVTR), low process temperatures, and good biocompatibility and biostability. The bi-layer encapsulation is composed of atomic layer deposited (ALD)  $\text{Al}_2\text{O}_3$  as water vapor barrier and chemical vapor deposited (CVD) Parylene C as an ion barrier as well as corrosion barrier for the  $\text{Al}_2\text{O}_3$  layer. The long-term performance of the bi-layer encapsulation was evaluated with accelerated lifetime test. A self-aligned selective etching process was also developed and optimized for exposing active sites to interact with the physiological environment. The ALD  $\text{Al}_2\text{O}_3$  and CVD Parylene bi-layer was applied to wired and wireless Utah electrode array (UEA)-based neural interfaces and long-term *in vitro* testing was performed.

### 7.1.1 Long-term Performance of ALD Al<sub>2</sub>O<sub>3</sub> and Parylene C Bi-layer Encapsulation

Plasma-enhanced atomic layer deposited (PEALD) Al<sub>2</sub>O<sub>3</sub> and chemical vapor deposited (CVD) Parylene bi-layer encapsulation was investigated as a potential thin-film encapsulation scheme for biomedical implantable devices. The PEALD process parameters were optimized to ensure a pure ALD process and the as-deposited Al<sub>2</sub>O<sub>3</sub> film was characterized. The long-term insulation performance of the bi-layer encapsulation was characterized based on *in vitro* testing of interdigitated electrode (IDE) test structures with accelerated lifetime conditions in phosphate buffered solution (PBS).

The deposition temperature of 120 °C was used to ensure the compatibility with implantable systems incorporated with active electronics and polymeric materials. The purge time for trimethylaluminum (TMA) and oxygen plasma was optimized to be 10 s and 5 s, respectively, to obtain the targeted deposition rate of  $\sim 1 \text{ \AA/cycle}$  through pure ALD process.

The deposition rate for ALD Al<sub>2</sub>O<sub>3</sub> was 1.04 Å/cycle, measured by ellipsometry. The surface roughness was 0.48 nm for 52 nm of Al<sub>2</sub>O<sub>3</sub> film, similar to the substrate surface roughness of 0.17 nm. X-ray photoelectron spectroscopy (XPS) was used to characterize the composition of as-deposited Al<sub>2</sub>O<sub>3</sub> and oxygen to aluminum ratio was 1.41, which is close to the stoichiometric value of 1.5.

The ALD Al<sub>2</sub>O<sub>3</sub> and Parylene C bi-layer encapsulation was evaluated based on IDE test structures. For 52-nm Al<sub>2</sub>O<sub>3</sub> and 6-μm Parylene C coated IDEs, leakage current was  $\sim 20 \text{ pA}$  at 5 VDC, and the impedance magnitude was about 3.5 MΩ at 1 kHz with a phase near -87° from electrochemical impedance spectroscopy after equivalent lifetime of

72 months at 37°C in PBS. The change of impedance during the whole soaking period (up to 70 months of equivalent soaking time at 37 °C) over 1 to 10<sup>6</sup> Hz was within 5%. The stability of impedance indicated almost no degradation of the encapsulation.

The effect of bias voltage on lifetime of the IDEs was studied by continuously applying 5 VDC during the soak testing at 37 °C and it reduced the lifetime of Parylene coating by ~ 75% to about 1 month. However, for the bi-layer encapsulation, there was insufficient degradation under bias and no-bias conditions to assess changes in lifetime of the test structures. With topography generated by attaching a coil and an SMD capacitor identical to those used in our wireless neural interfaces, lifetime of bi-layer coated IDEs decreased roughly 50% compared to planer IDEs.

The stable long-term (9 months under 67 °C) insulation impedance, low leakage current, and better lifetime under bias voltage and topography made this Al<sub>2</sub>O<sub>3</sub> and Parylene C bi-layer encapsulation very promising for chronic implantable devices.

### 7.1.2 Selective Etching of ALD Al<sub>2</sub>O<sub>3</sub> and Parylene C

#### Bi-layer Encapsulated Neural Interfaces

A self-aligned three-step selective etching process was developed to replace the traditional tip-deinsulation process using aluminum foil as a mask layer. The self-masked etching process can be adopted to devices with complex geometries or uneven backside topography where poking is difficult. The exposed area can be controlled more precisely, which improves the uniformity of the impedance.

The self-masked deinsulation process for Al<sub>2</sub>O<sub>3</sub> and Parylene C bi-layer encapsulation is composed of three steps: laser ablation, oxygen plasma etching, and

buffered oxide etch (BOE) etching. The laser ablation is to remove the Parylene C layer and define the exposing area, followed by 2 minutes of oxygen plasma to remove redeposited carbon residual during laser ablation. The complete removal of  $\text{Al}_2\text{O}_3$  is achieved by 8 minutes of BOE, which was confirmed by x-ray photoelectron spectroscopy (XPS). The  $\text{Al}_2\text{O}_3$  layer is found to prevent the formation of microcracks and melt of the sputtered iridium oxide films (SIROFs) underneath during the laser ablation. The Ir 4f peaks between as deposited iridium oxide and postetched iridium oxide were almost identical through XPS spectra.

The electrochemical properties of the bi-layer encapsulated and Parylene C encapsulated iridium oxide after deinsulation were compared. For areas of  $2 \times 10^{-4} \text{ cm}^2$ , the charge injection capacity (CIC) of iridium oxide after etching the bi-layer encapsulation was  $1.6 \text{ mC/cm}^2$ , which is higher than that of Parylene coated iridium oxide ( $1.2 \text{ mC/cm}^2$ ). Additionally, the bi-layer coated iridium oxide had similar charge storage capacity (CSC) and electrochemical impedance compared with Parylene coated iridium oxide after etching. Overall, the three-step deinsulation process did not significantly affect the electrochemical properties of the bi-layer encapsulated iridium oxide.

### 7.1.3 Long-term Reliability of $\text{Al}_2\text{O}_3$ and Parylene C

#### Bi-layer Encapsulated Neural Interfaces

Utah Electrode Array (UEA)-based neural interfaces with different configurations were used to evaluate the performance of  $\text{Al}_2\text{O}_3$  and Parylene C bi-layer encapsulation from different aspects through accelerated lifetime testing. Wired UEAs were used for

long-term impedance stability, fully integrated wireless neural interfaces were used for long-term wireless signal strength and frequency stability, and active neural interfaces were used to monitor current draw of the ASIC chips over time. Devices were coated with 52 nm of Al<sub>2</sub>O<sub>3</sub> deposited by plasma-enhanced ALD, followed by a 6- $\mu$ m thick Parylene-C layer deposited by CVD using the Gorman process.

Impedance for wired array was measured at 1 kHz. Median impedance increased from 61 k $\Omega$  to 160 k $\Omega$  after 960 equivalent soaking days at 37 °C. The typical trend has been for impedances of arrays coated with Parylene to decrease with time [1, 2], likely the result of water ingress. We observed an increase in impedance over time for bi-layer coated UEAs, suggesting that water ingress is minimized. The mechanism for the increased impedance was determined to be etching of the Si under the tip metallization, due to the dissolution of Si in PBS for those areas exposed by damage to the tip metallization.

For the wireless neural interfaces, the power-up frequency was constantly ~ 910 MHz and the RF signal strength was stably around -73 dBm during equivalent soaking time of 1000 days at 37 °C (still under soak testing). This is significantly longer than lifetime achieved through Parylene coating, which was about one year at room temperature (22 °C) [3]. The long lifetime of bi-layer encapsulation was ascribed to the reduction of water vapor permeation and separation of moisture from substrate surface contaminants, like ions, metal particles, etc.

## 7.2 Future Work

### 7.2.1 Long-term In Vivo Experiment

The long-term insulation performance of  $\text{Al}_2\text{O}_3$  and Parylene C bi-layer encapsulation has been demonstrated with *in vitro* soak testing [4]. Accelerated lifetime testing was performed at different temperature in PBS to speed up the validation process for this bi-layer encapsulation.

The ultimate goal of this work is to extend the lifetime of implantable devices *in vivo* up to decades. The most realistic testing is to implant medical devices that are coated with  $\text{Al}_2\text{O}_3$  and Parylene C bi-layer and evaluate the long-term performance of those devices. Comparison can be conducted between bi-layer coated and Parylene coated devices, including signal to noise ratio, long-term impedance stability, wireless signal strength, and lifetime of the implanted devices.

### 7.2.2 Hydrogen Reduction or Elimination in $\text{Al}_2\text{O}_3$ Film

Atomic layer deposited (ALD)  $\text{Al}_2\text{O}_3$  dissolves in liquid water [5], due to the hydrogen incorporation in the form of OH group during the deposition process [6, 7]. The use of trimethylaluminum (TMA) makes the hydrogen incorporation almost unavoidable.

A few methods have been developed to minimize hydrogen incorporation during the ALD process. Increase of deposition temperature can significantly reduce the hydrogen concentration in the film [8]. For low thermal budget applications, plasma-enhanced ALD can reduce hydrogen incorporation at low temperature. Also, new oxidative species like ozone can reduce the hydrogen in the deposited  $\text{Al}_2\text{O}_3$  film [9].



Alternatively, in order to completely remove hydrogen incorporation in the  $\text{Al}_2\text{O}_3$  film, precursor needs to be free of methyl group. New precursors other than TMA need to be developed to achieve hydrogen free ALD  $\text{Al}_2\text{O}_3$  film.

### 7.2.3 Cap Layer for Preventing $\text{Al}_2\text{O}_3$ Dissolution

ALD  $\text{Al}_2\text{O}_3$  film is known to dissolve in liquid water because of the hydrogen incorporation [5, 6]. In order to slow down or prevent the dissolution process, a cap layer can be added to the top of  $\text{Al}_2\text{O}_3$ . ALD  $\text{TiO}_2$  is proven to effectively slow down the  $\text{Al}_2\text{O}_3$  dissolution process [5, 7]. Alternatively,  $\text{Al}_2\text{O}_3$  with a  $\text{TiO}_2$  cap layer converted from oxidation of e-beam sputtered Ti showed similar improved hydrolytic stability compared with  $\text{Al}_2\text{O}_3$  with ALD  $\text{TiO}_2$  cap layer[7]. Therefore, an extra  $\text{TiO}_2$  layer between  $\text{Al}_2\text{O}_3$  and Parylene C could potentially further improve the encapsulation performance.

### 7.2.4 Multilayer Configuration

We have demonstrated the excellent insulation of  $\text{Al}_2\text{O}_3$  and Parylene C bi-layer encapsulation. Multilayer encapsulation can be achieved by repeating this bi-layer encapsulation without significantly increasing the total thickness of each film.

The development of molecular layer deposition (MLD) technique made it possible to control the deposition of organic materials on molecular level [10]. It should be noticed that MLD is not compatible with Parylene for now. A inorganic/organic hybrid multilayer can be fabricated by ALD and MLD [11]. This facilitates the capability of fabrication multilayer encapsulation on atomic and molecular level to eliminate pinholes

and thickness variations. Potential combinations include Al<sub>2</sub>O<sub>3</sub>/Parylene and Al<sub>2</sub>O<sub>3</sub>/Polytetrafluoroethylene (PTFE).

### 7.2.5 Nucleation of Neural Interface Surfaces

The nucleation process is required to start the ALD process. Nucleation process varies from surface to surface and needs to be study individually. Nucleation process of ALD Al<sub>2</sub>O<sub>3</sub> on substrate like Si, carbon nanotubes, graphene, polyethylene, (PMMA), polypropylene, polystyrene, and polyvinylchloride have been studied using methods like *in situ* Fourier transform infrared spectroscopy (FTIR) and quartz crystal microbalance (QCM) [10, 12-15]. For new added inert surfaces from neural interfaces, such as gold and silicone, nucleation process investigation is necessary to ensure the uniform growth of ALD Al<sub>2</sub>O<sub>3</sub>. Functional group treatment might be required for some inert surface.

### 7.2.6 Biocompatibility Improvement

Biocompatibility of the Parylene surface can be improved by surface modifications or surface coating. Generally there are two ways to improve biocompatibility: introducing a nonfouling surface to alleviate protein absorption or a bioactive surface. Extensive efforts have been dedicated to improve biocompatibility, including:

- (a) Coating Parylene surface with biodegradable antirestenotic agents to release over time [16].
- (b) Modifying the polymer surface by grafting photoinduced phospholipids polymer to obtain an antifouling surface [17].

(c) Enhancing the fibroblast cell attachment and growth by introducing surface topography to the Parylene surface [18].

Biodegradable antirestenotic agents have been studied in our group and demonstrated promising result of alleviating foreign body responses. This can be combined with Parylene film to improve the biocompatibility of the coated devices.

#### 7.2.7 Improving Substrate Stability

Scanning electron microscopy (SEM) images of  $\text{Al}_2\text{O}_3$  and Parylene bi-layer coated Utah electrode array (UEA) after 3 years of equivalent soak testing at 37 °C confirmed etching of silicon by PBS. Mechanism behind this remains unknown and needs to be fully studied. Solutions to improve stability of the substrate needs to be proposed based on the etching mechanism. This is one of the key factors to achieve chronic implantation for neural interfaces. Corrosion resistant materials like titanium and conductive silicon carbide can be used to replace the silicon substrate. Additional fabrication processes need to be developed.

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