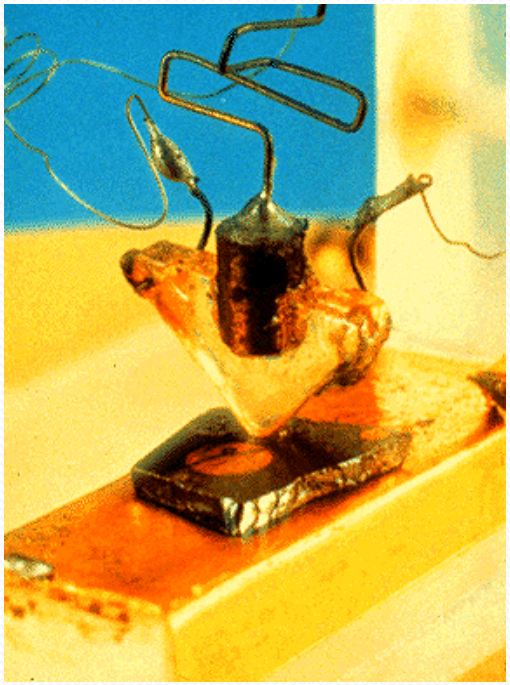
Integrated Circuits

Introduction

Integrated Circuits

- Its importance is well-known
- Invention of Jack Kilby and Robert Noyce



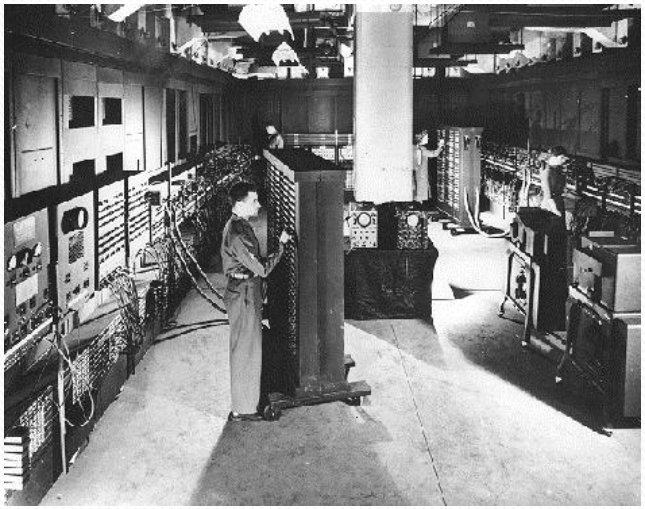
A scientific milestone: first transistor (Bell Labs 1947)

A technological milestone: Kilby's integrated circuit, TI (1959)

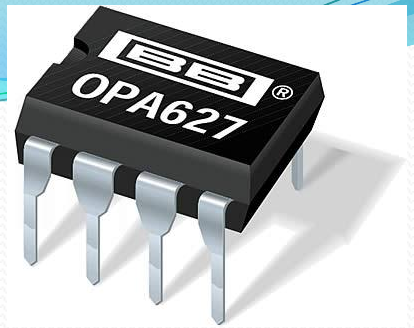
Milestones

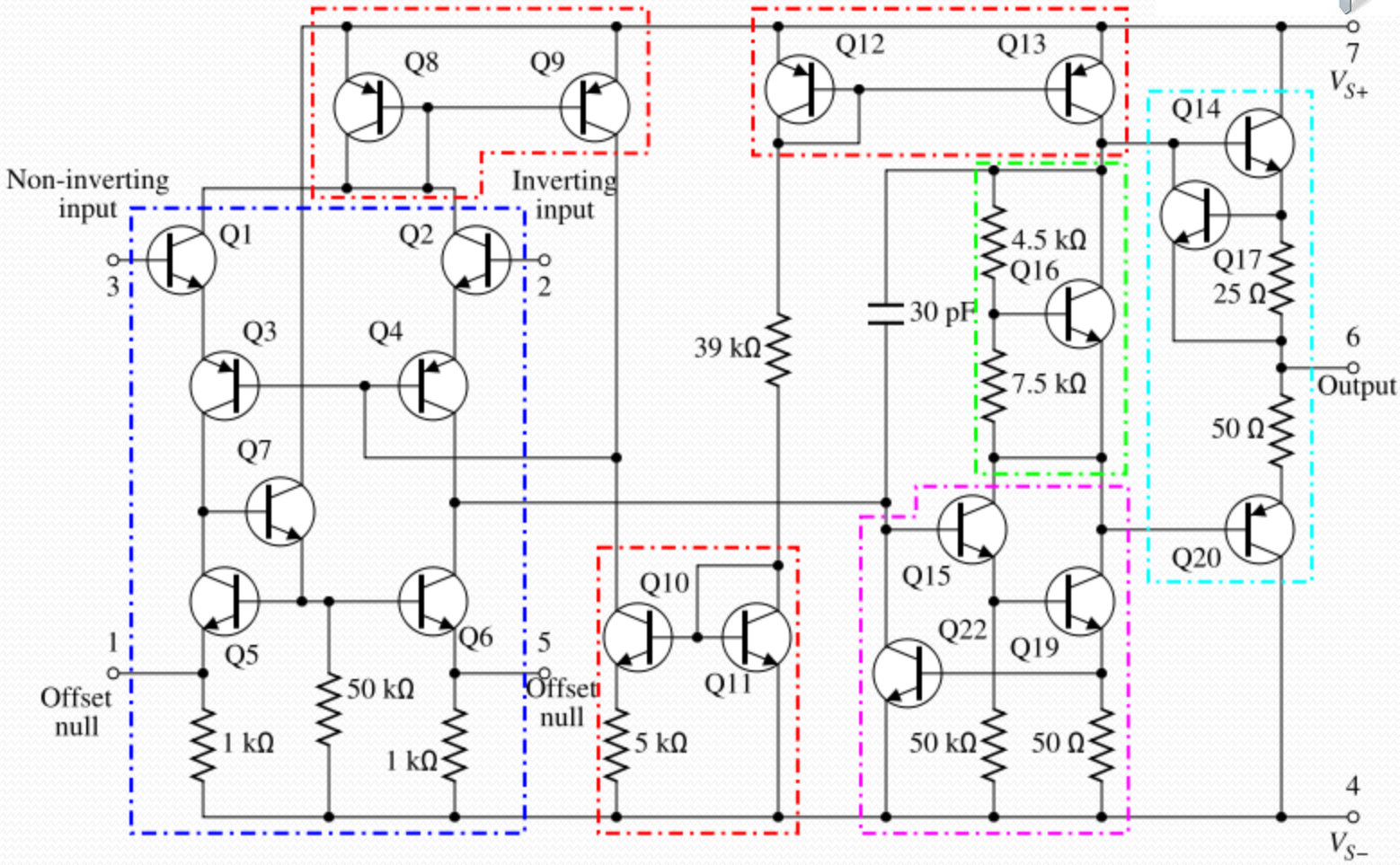
- 1959: First IC
- … then a lot of nice ICs,…but they “can’t change much” (not programmable)

ENIAC

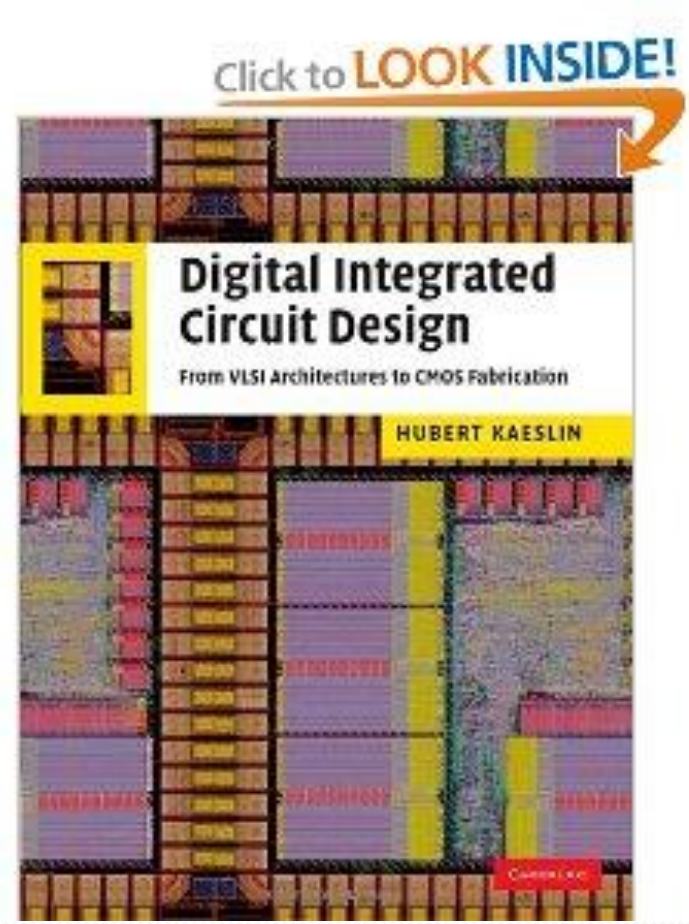


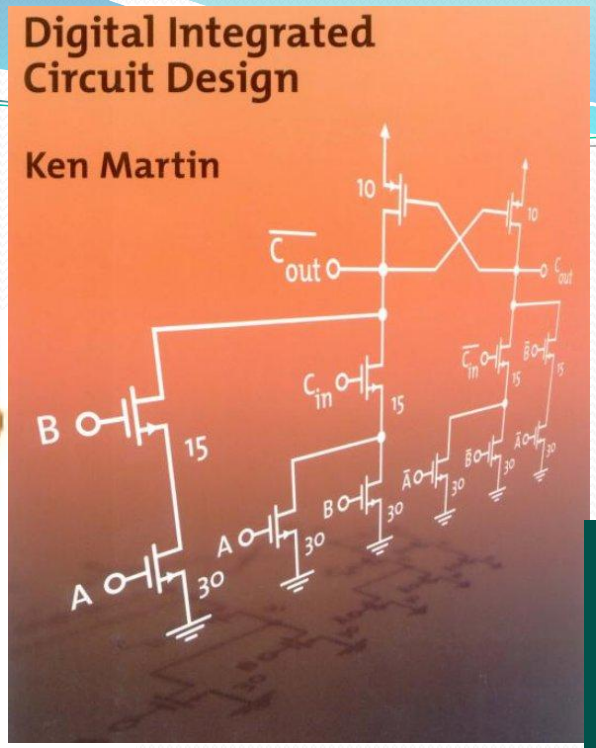
Op Amp

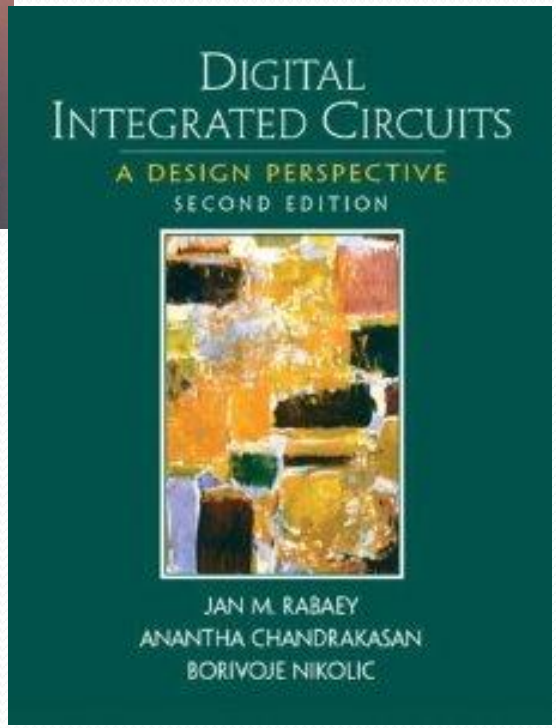




Source: wiki


Click to LOOK INSIDE!
Digital Integrated Circuit Design
From VLSI Architectures to CMOS Fabrication
HUBERT KAESLIN


Digital Integrated Circuit Design
Ken Martin


DIGITAL INTEGRATED CIRCUITS
A DESIGN PERSPECTIVE
SECOND EDITION
JAN M. RABAEY
ANANTHA CHANDRAKASAN
BORIVOJE NIKOLIC

Honeywell kitchen computer

TECHNICAL INFORMATION	
NAME	H316 - Kitchen computer
MANUFACTURER	Honeywell
TYPE	Home Computer
ORIGIN	U.S.A.
YEAR	1969
BUILT IN LANGUAGE	Recipes were programmed into it, but language/software is unknown
KEYBOARD	Small array of buttons and switches
CPU	Unknown
SPEED	2.5 MHz
RAM	4 KB magnetic core, expandable to 16 KB
ROM	Unknown
TEXT MODES	Unknown, probably some kind of text display
SIZE / WEIGHT	150 pounds
BUILT IN MEDIA	Magnetic core memory
POWER SUPPLY	475W at 125vAC
PERIPHERALS	Unless you count the cutting board...unknown
PRICE	$10,600

Milestones

- 1971: Microprocessor: The story of Intel & Busicom, Ted (Marcian) Hoff
  - Silicon-gated MOS
  - 4004 with ~2000 transistors

http://www.pcworld.com/article/243954/happy_birthday_4004_intels_first_microprocessor_turns_the_big_40.html

What drive technology?

Morgan Stanley

Mobile Internet
Next Major Computing Cycle

Source: Mary Meeker

Mainframe **Computing** **1950s**	***Mini*** **Computing** **1960s**	***Personal*** **Computing** **1980s**	***Desktop Internet*** **Computing** **1990s**	***Mobile Internet*** **Computing** **2000s**
				

Technology Cycles - Wealth Creation / Destruction

New Companies Often Win Big in New Cycles

Mainframe Computing 1950s	*Mini* Computing 1960s	*Personal* Computing 1980s	*Desktop Internet* Computing 1990s	*Mobile Internet* Computing 2000s
Winners	**Winners**	**Winners**	**Winners**	?
IBM	Digital Equipment	Microsoft	Google	
NCR	Data General	Cisco	AOL	
Control Data	HP	Intel	eBay	
Sperry	Honeywell	Apple	Yahoo!	
Honeywell	Prime	IBM	Yahoo! Japan	
Burroughs	Computervision	Oracle	Amazon.com	
	Wang Labs	EMC	Tencent	
		Dell	Alibaba	
		HP	Baidu	
		Compaq	Rakuten	

Source: Mary Meeker

Morgan Stanley

Note: Winners from 1950s to 1980s based on Fortune 500 rankings (revenue-based), desktop Internet winners based on wealth created from 1995 to respective peak market capitalizations. Source: Factset, Fortune, Morgan Stanley Research.

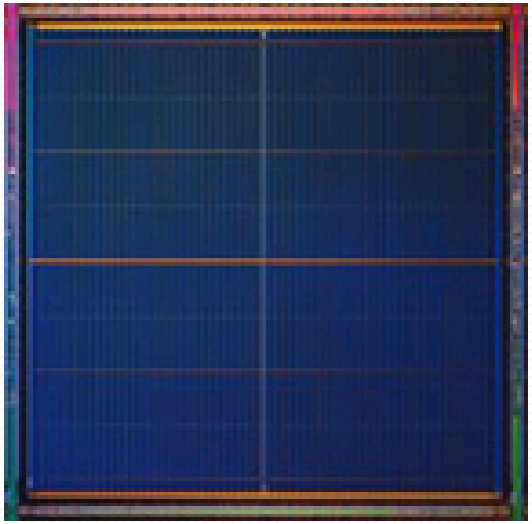
“Smart” ICs

Field Programmable Gate Array (FPGA)

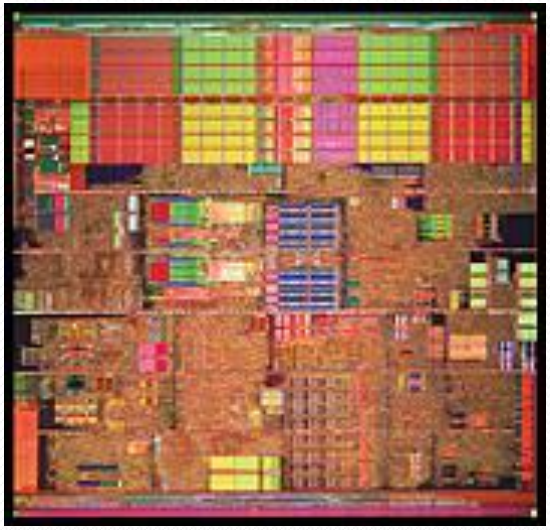
Digital Signal Processor (DSP)

Microprocessor

FPGA vs. Microprocessor



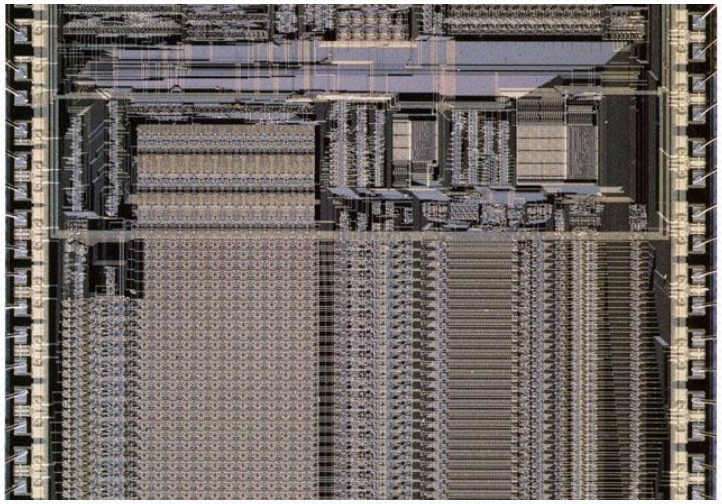
FPGA



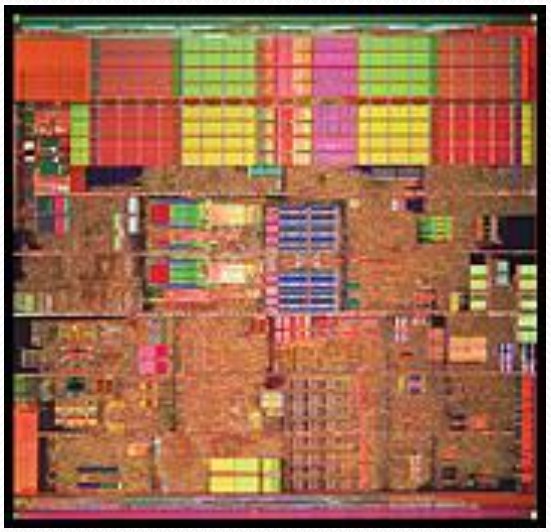
Pentium

- IC technology supports very diverse architecture

The “Old-Time Story” of RISC vs. CISC



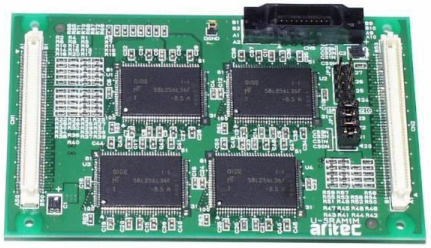
ARM



x86

- Specialized architectures for different applications

Memory IC's

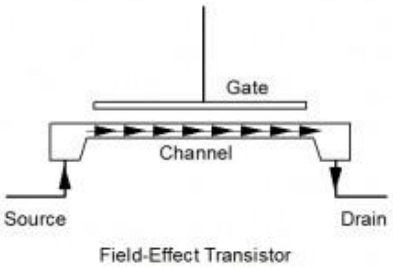


SRAM

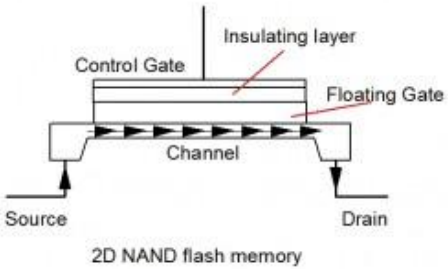
DRAM

Non-volatile RAM

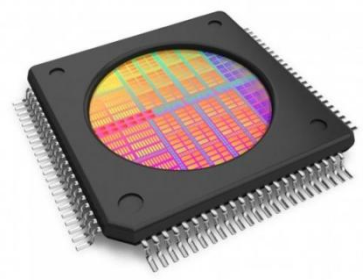
NAND flash SSD

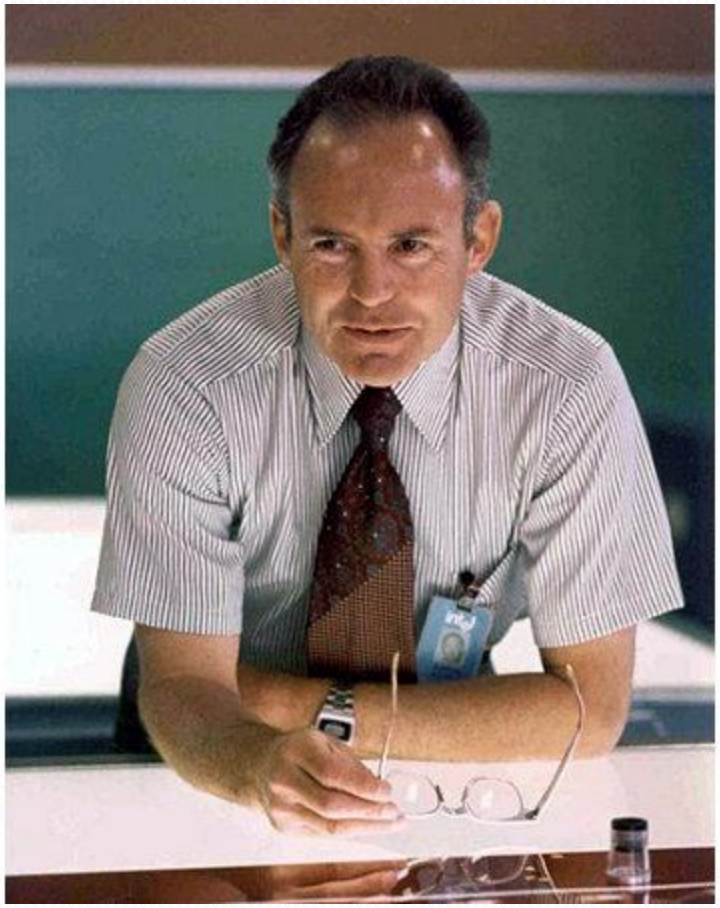


Field-Effect Transistor



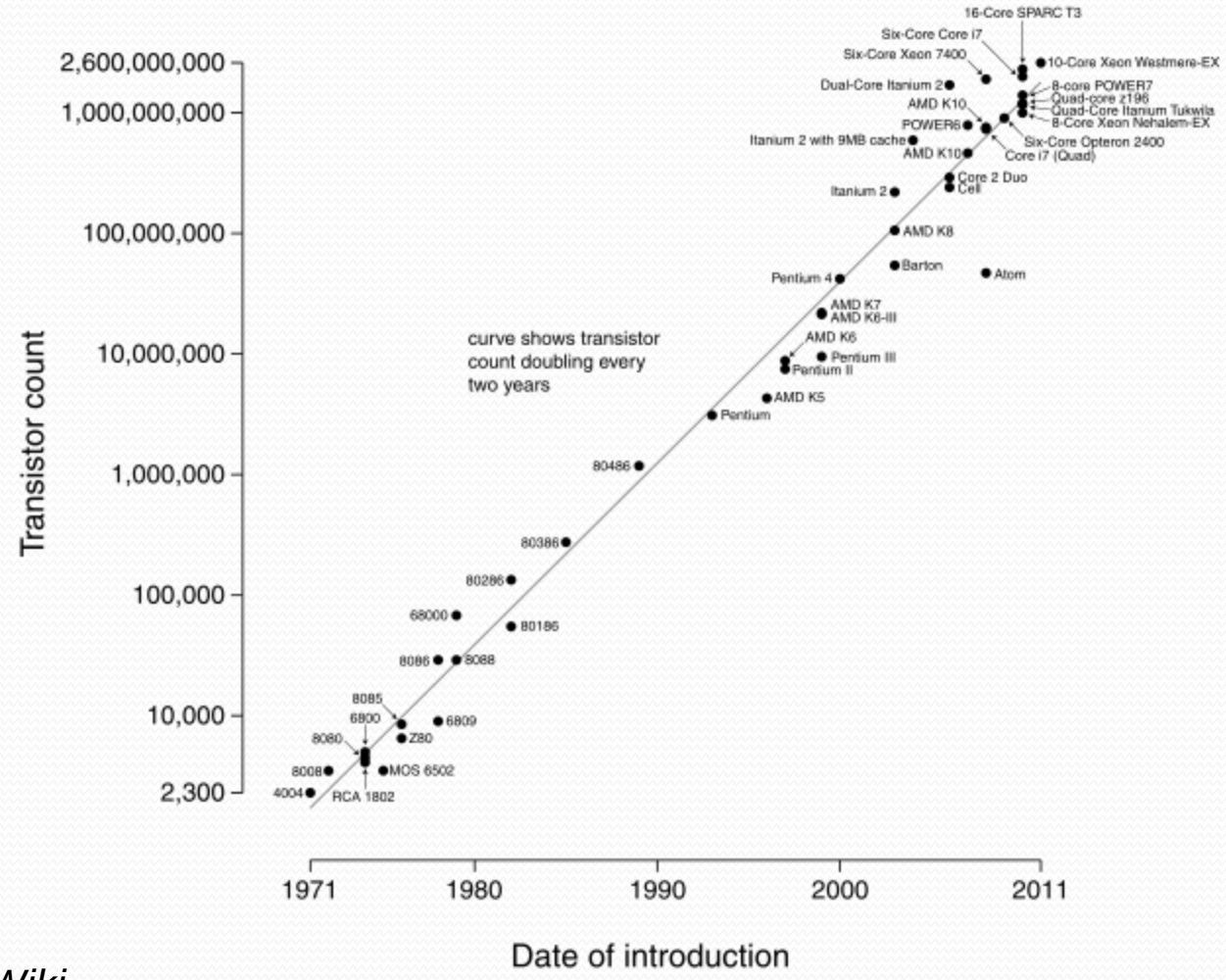
2D NAND flash memory





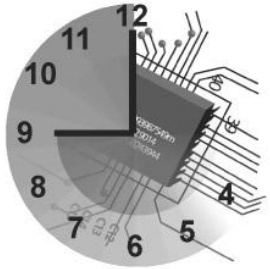
Microprocessor	Year of Introduction	Transistors
4004	1971	2,300
8008	1972	2,500
8080	1974	4,500
8086	1978	29,000
Intel286	1982	134,000
Intel386™ processor	1985	275,000
Intel486™ processor	1989	1,200,000
Intel® Pentium® processor	1993	3,100,000
Intel® Pentium® II processor	1997	7,500,000
Intel® Pentium® III processor	1999	9,500,000
Intel® Pentium® 4 processor	2000	42,000,000
Intel® Itanium® processor	2001	25,000,000
Intel® Itanium® 2 processor	2003	220,000,000
Intel® Itanium® 2 processor (9MB cache)	2004	592,000,000

Moore’s law



Source: Wiki

Microprocessor Cost Per Transistor Cycle



Logarithmic Plot

$/Transistor/Hz

10^{-7}
10^{-10}
10^{-13}
10^{-16}
10^{-19}

1975 1980 1985 1990 1995 2000 2005 2010 2015 2020

Halving time: 1.1 years

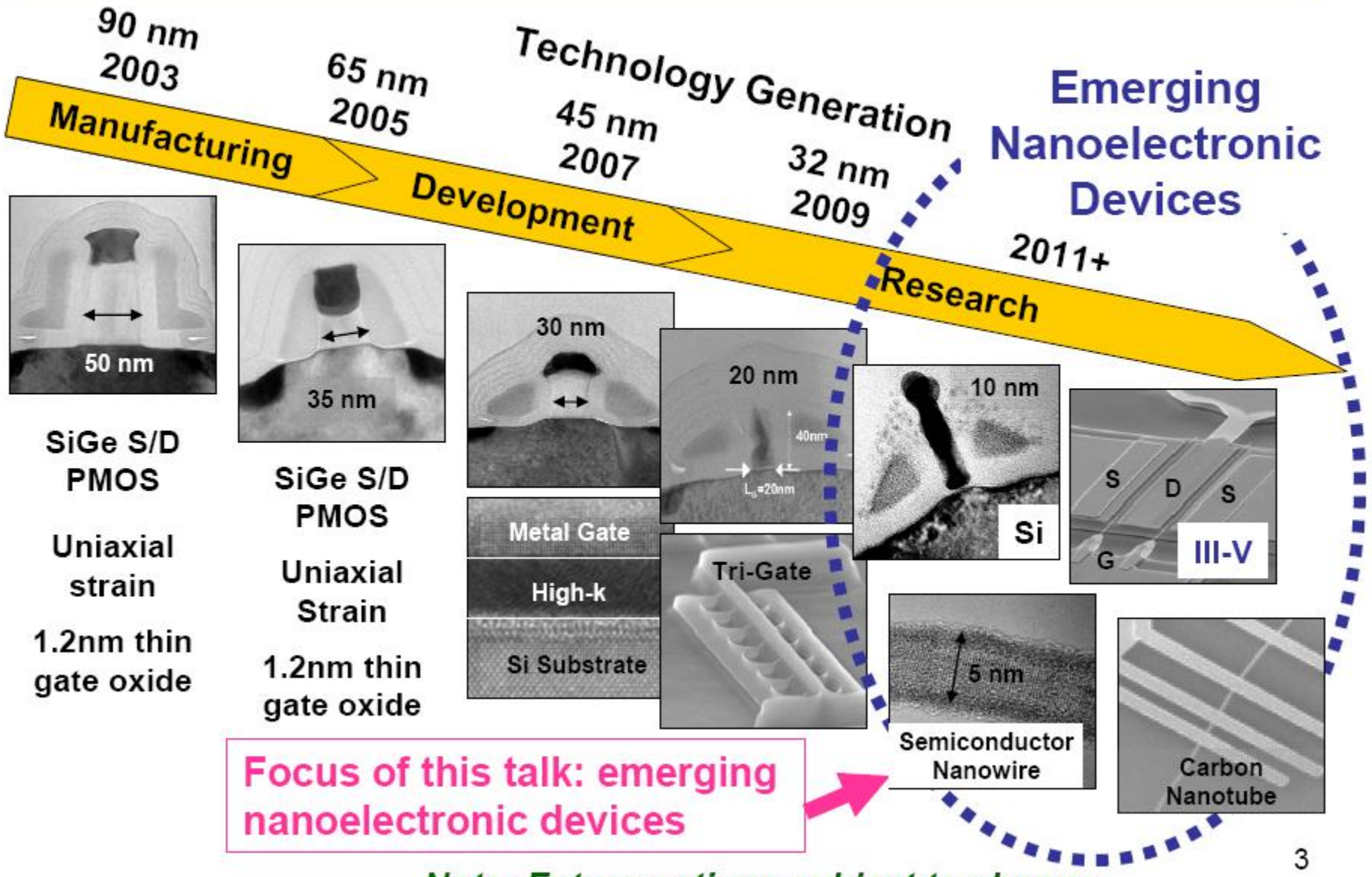
Year

Key Enabling Technologies For ICs

Crucial elements of IC technology

- Devices and materials
  - Transistor design and scaling
  - Semiconductors and advanced materials
- Fabrication technology (Front end):
  - feature size: how small can a transistor gate be?
  - how to pack many T's in a very small area: VLSI, ULSI
  - device structure: beyond planar, 2D constraint
  - how to make high-performance oxides, insulators
  - how to make contact, "wiring"?
  - wafer scaling
- Chip packaging technology (Back end)

Transistor Nanotechnology

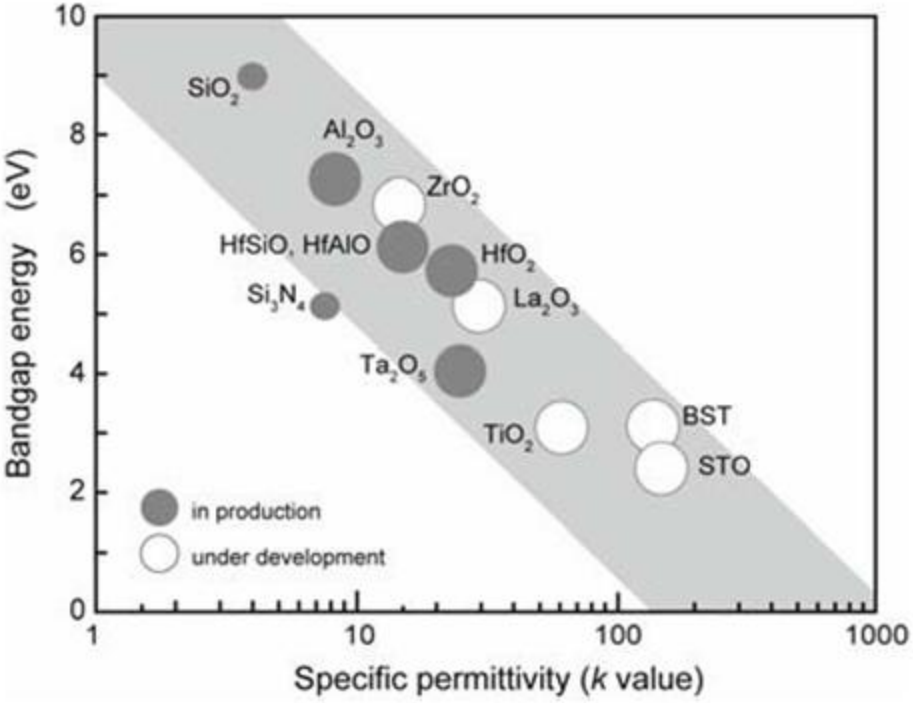


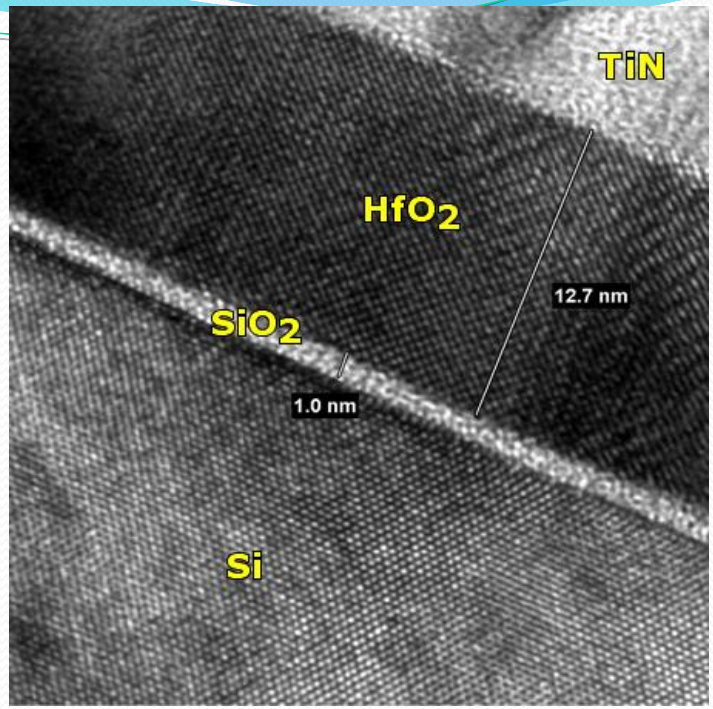
Focus of this talk: emerging nanoelectronic devices

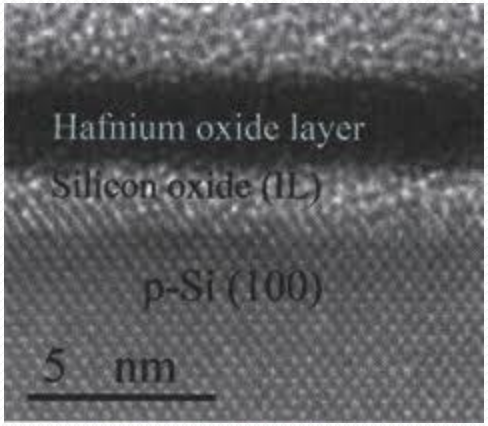
Source: Robert Chau, Intel

Note: Future options subject to change


Moore's Law Requires More Than Just Scaling
130nm
2001
Scaling
Scaling
Materials Science
90nm
2003
65nm
2005
45nm
2007
32nm
2009
22nm
2011
www.semiaccurate.com
Strained Silicon >3yrs
1st Competitor
S|A
High-k Metal Gate >3.5yrs
1st Competitor
Tri-Gate 4yrs?


Bandgap energy (eV)
Specific permittivity (k value)
SiO2
Al2O3
ZrO2
HfSiO, HfAlO
HfO2
Si3N4
La2O3
Ta2O5
TiO2
BST
STO
in production
under development
0
2
4
6
8
10
1
10
100
1000


TiN
HfO2
12.7 nm
SiO2
1.0 nm
Si


Hafnium oxide layer
Silicon oxide (IL)
p-Si (100)
5 nm

How small can the transistor be?

Past prediction

The ultimate limit of the transistor is ~ 10 μm

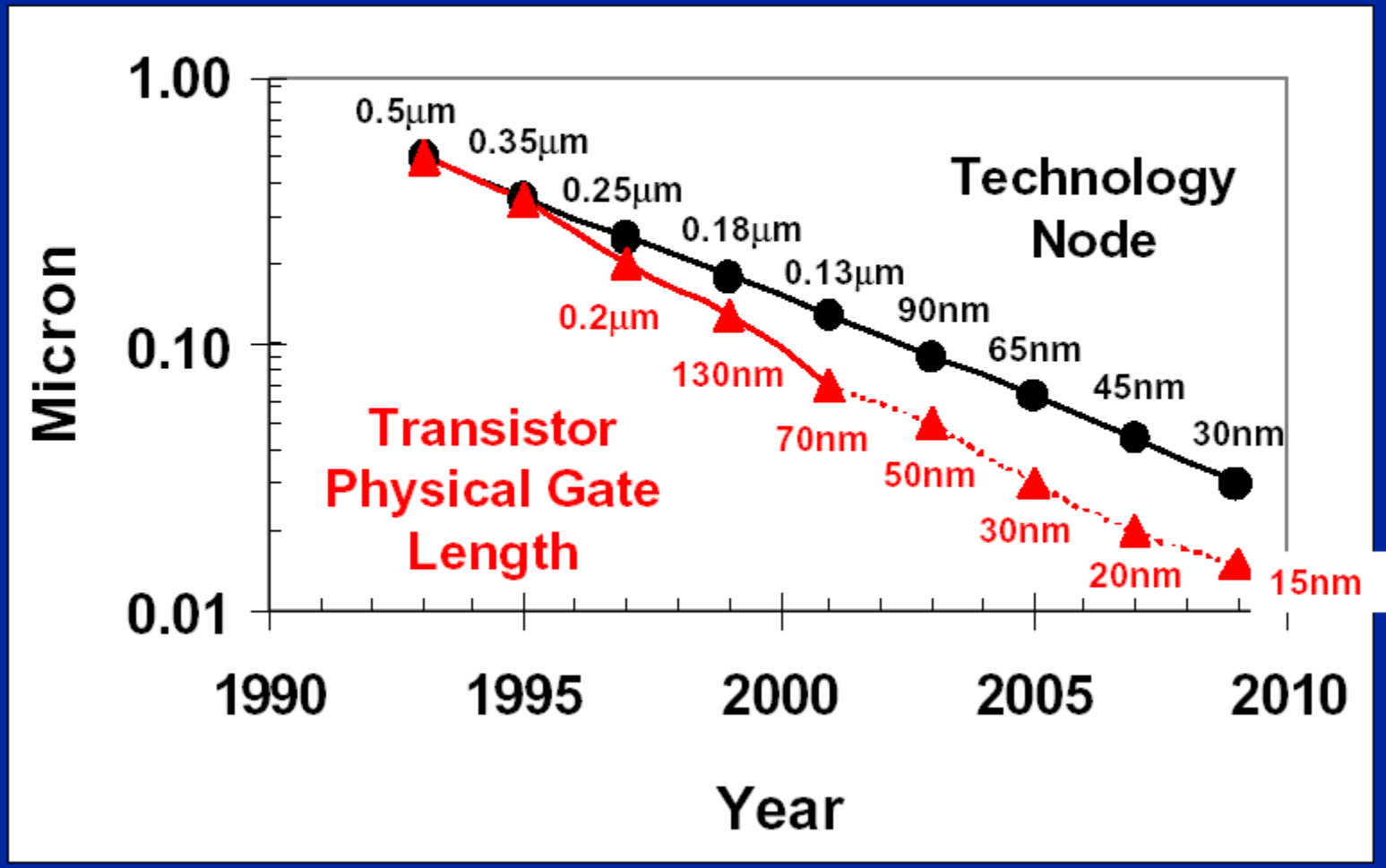
1961

… On a pentium (~2002), it was ~ 0.1 μm

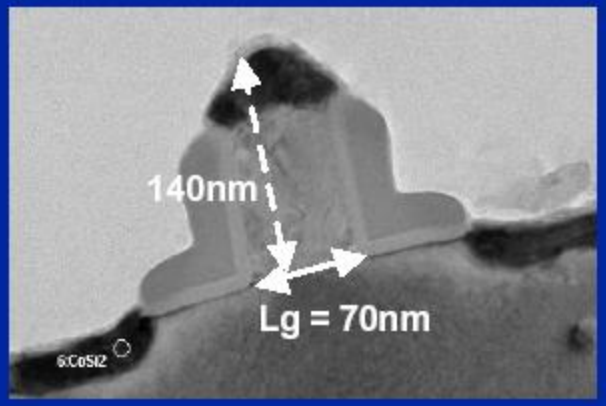
… And they think: 0.015 μm is the ultimate limit

Don't bet your money on it!

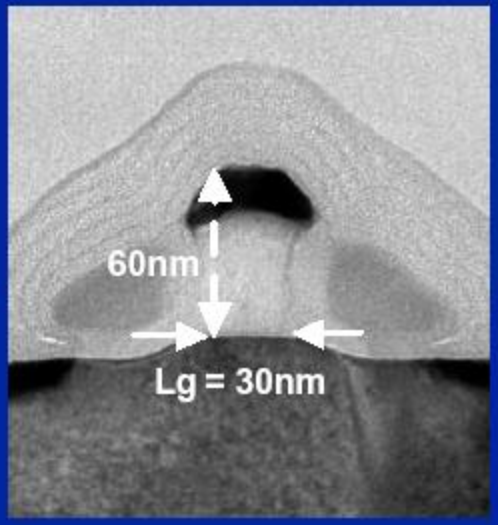
Transistor Physical Gate Length Trend (Lithography generation > L_{GATE})



Transistor Scaling Continues

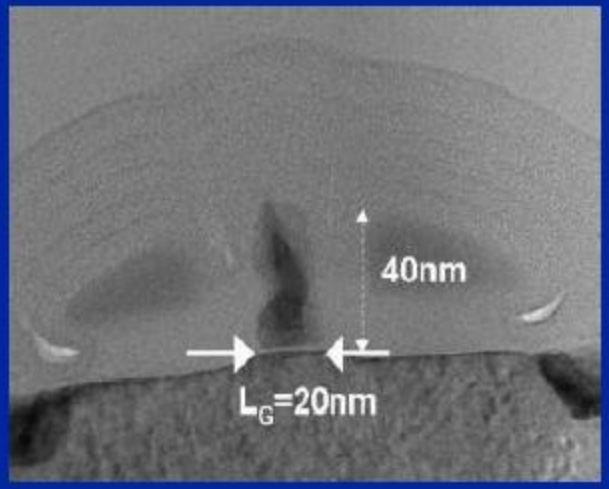


70nm transistor
(in production)



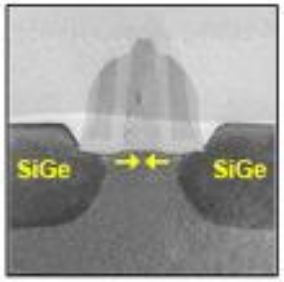
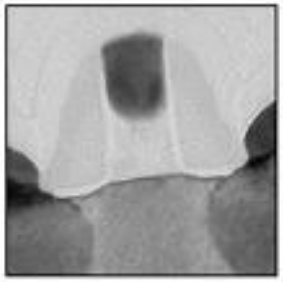
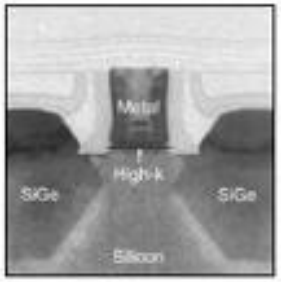
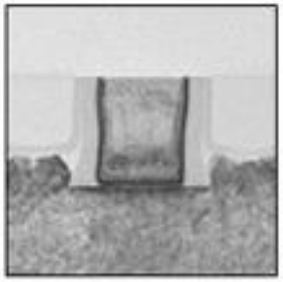
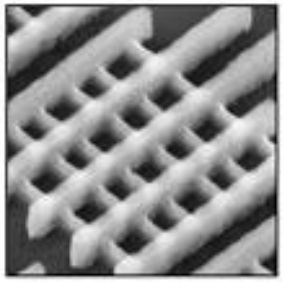
30nm transistor
(production 2005)

In 2005



20nm transistor
(research phase)

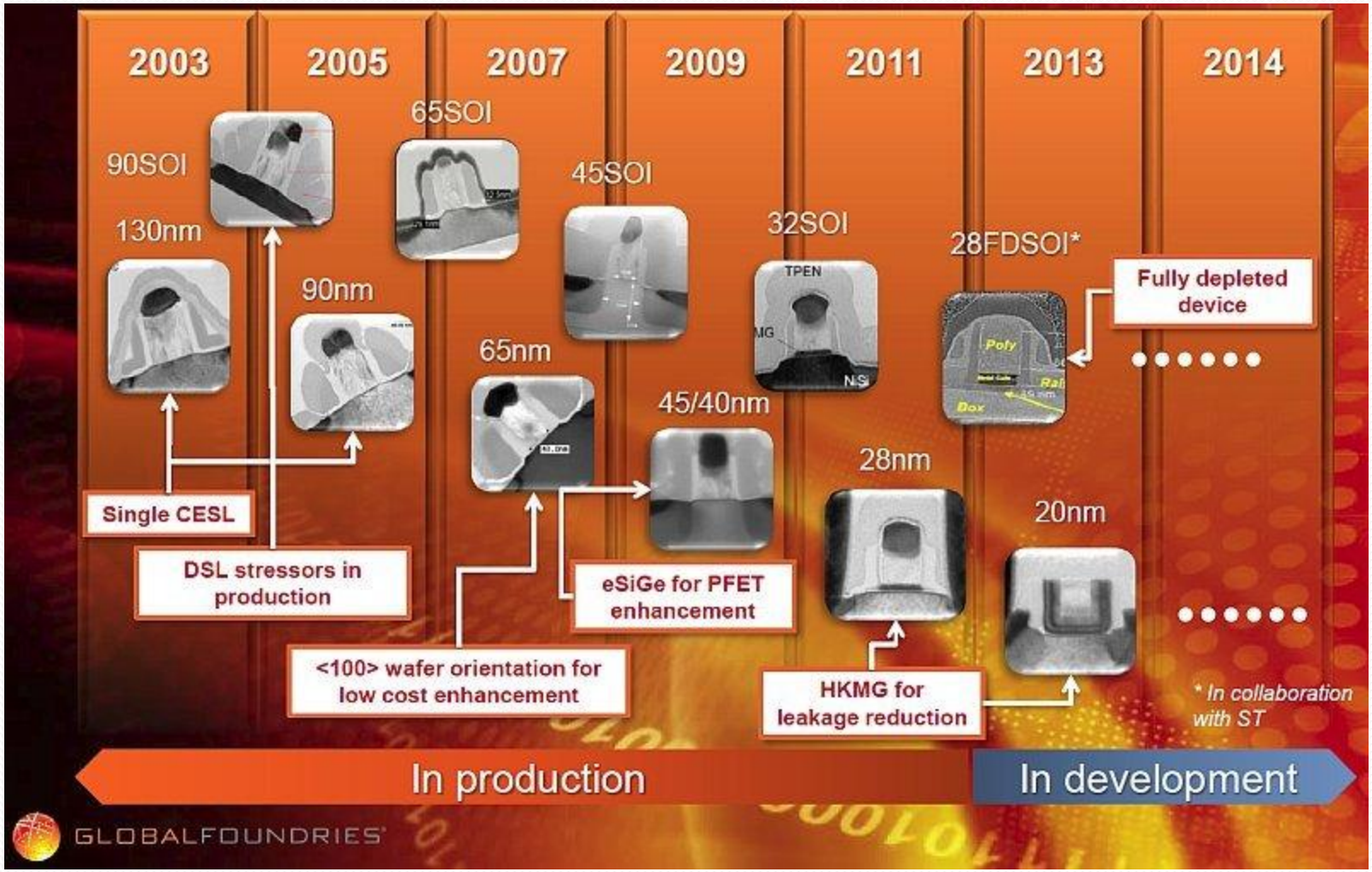
Intel Transistor Leadership

2003	2005	2007	2009	2011
90 nm	65 nm	45 nm	32 nm	22 nm
				
Invented SiGe Strained Silicon	2nd Gen. SiGe Strained Silicon	Invented Gate-Last High-k Metal Gate	2nd Gen. Gate-Last High-k Metal Gate	First to Implement Tri-Gate

Strained Silicon

High-k Metal Gate

Tri-Gate


2003
2005
2007
2009
2011
2013
2014
90SOI
130nm
65SOI
90nm
45SOI
65nm
32SOI
TPEN
MG
N-Si
28FDSOI*
Poly
Box
Fully depleted device
45/40nm
28nm
20nm
Single CESL
DSL stressors in production
<100> wafer orientation for low cost enhancement
eSiGe for PFET enhancement
HKMG for leakage reduction
* In collaboration with ST
In production
In development
GLOBALFOUNDRIES

Introducing 14XM (eXtreme Mobility)

2003	2005	2007	2009	2011	2013	2014
130nm	90nm	65nm	45/40nm	28nm	20nm	14XM

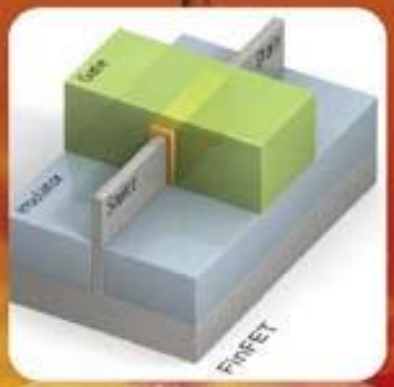
2years 2years 2years 2years 2years

1 year!

Foundry's first innovative 14nm FinFET

Our solution is focused on:

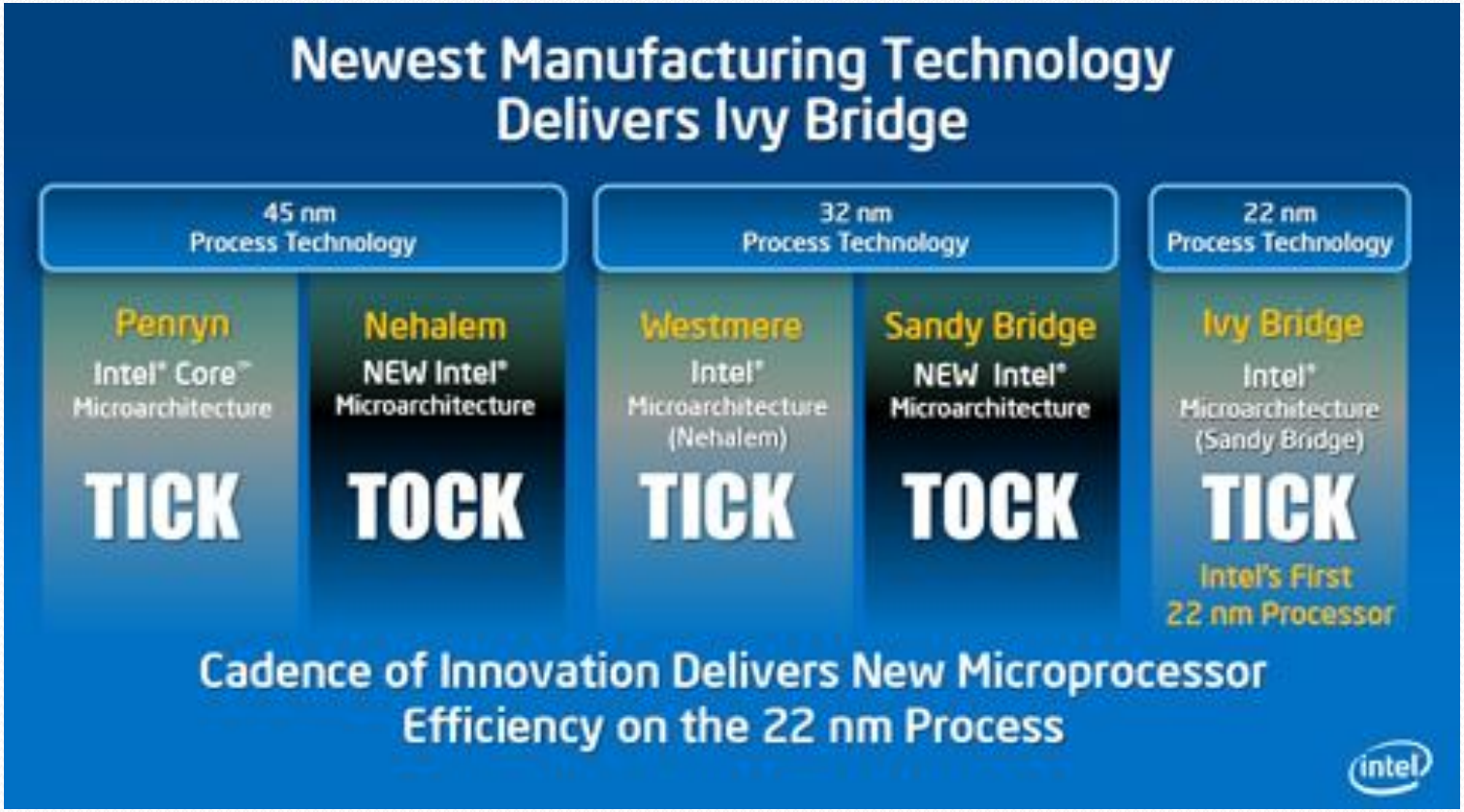
- *Rapid Time to Market (TTM)*
- *Ultra-Low Power*
- *Lowest risk path to high-volume manufacturing*
- *Competitive Cost and Performance*

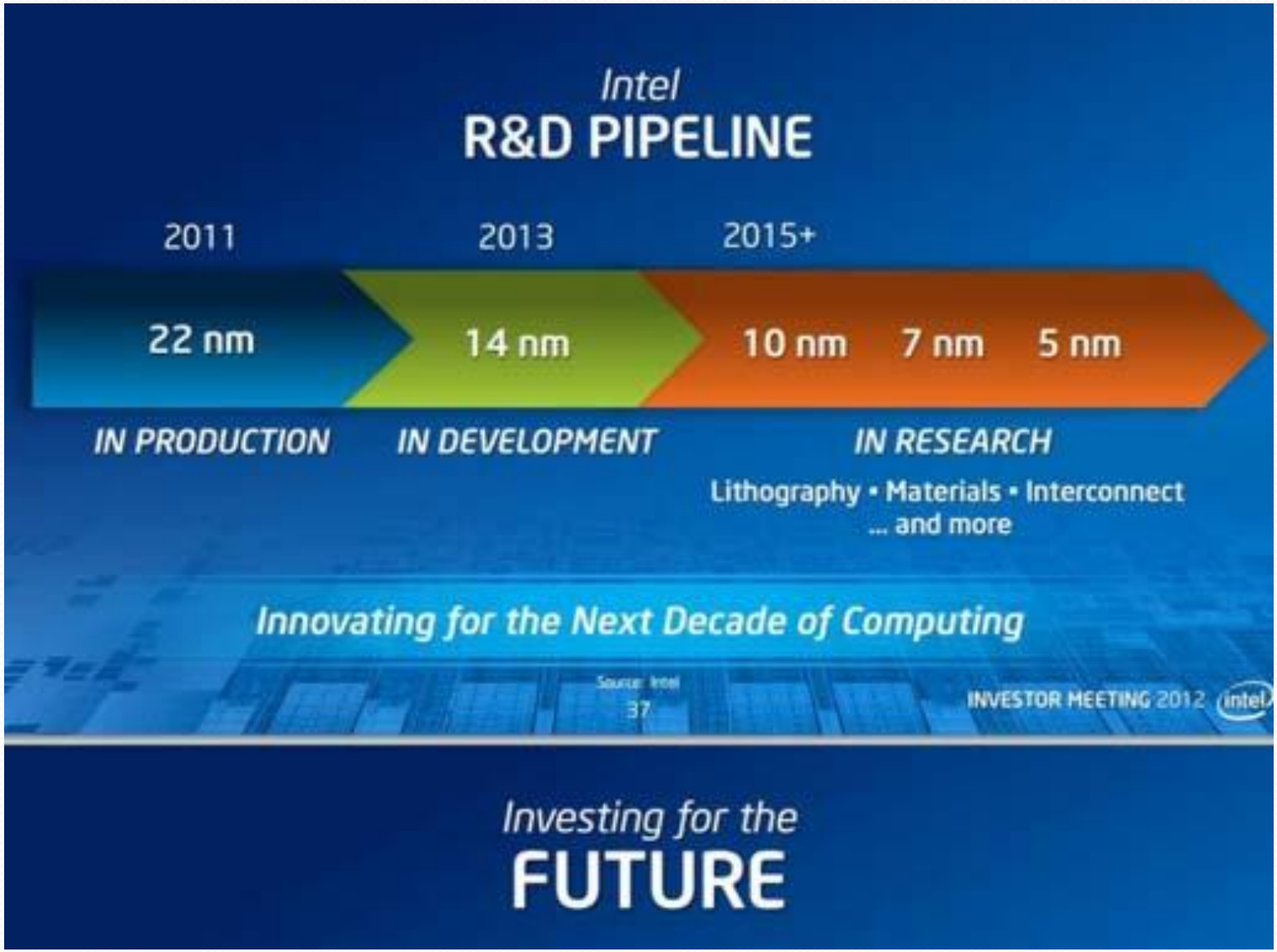


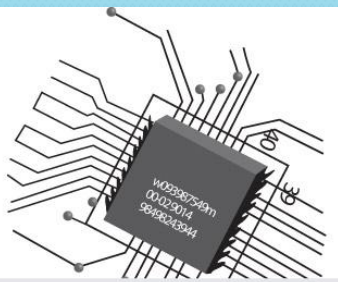
In production

In development

In 2010


Newest Manufacturing Technology
Delivers Ivy Bridge
45 nm
Process Technology
32 nm
Process Technology
22 nm
Process Technology
Penryn
Intel® Core™
Microarchitecture
TICK
Nehalem
NEW Intel®
Microarchitecture
TOCK
Westmere
Intel®
Microarchitecture
(Nehalem)
TICK
Sandy Bridge
NEW Intel®
Microarchitecture
TOCK
Ivy Bridge
Intel®
Microarchitecture
(Sandy Bridge)
TICK
Intel's First
22 nm Processor
Cadence of Innovation Delivers New Microprocessor
Efficiency on the 22 nm Process
intel


Intel
R&D PIPELINE
2011
2013
2015+
22 nm
14 nm
10 nm
7 nm
5 nm
IN PRODUCTION
IN DEVELOPMENT
IN RESEARCH
Lithography • Materials • Interconnect
... and more
Innovating for the Next Decade of Computing
Source: Intel
37
INVESTOR MEETING 2012
intel
Investing for the
FUTURE



Dynamic RAM

Smallest (called “Half Pitch”) Feature Size

Logarithmic Plot

DRAM Half Pitch (nm)

100,000
10,000
1,000
100
10

$r^2 = 0.9901$

Trend Line
Projected Future

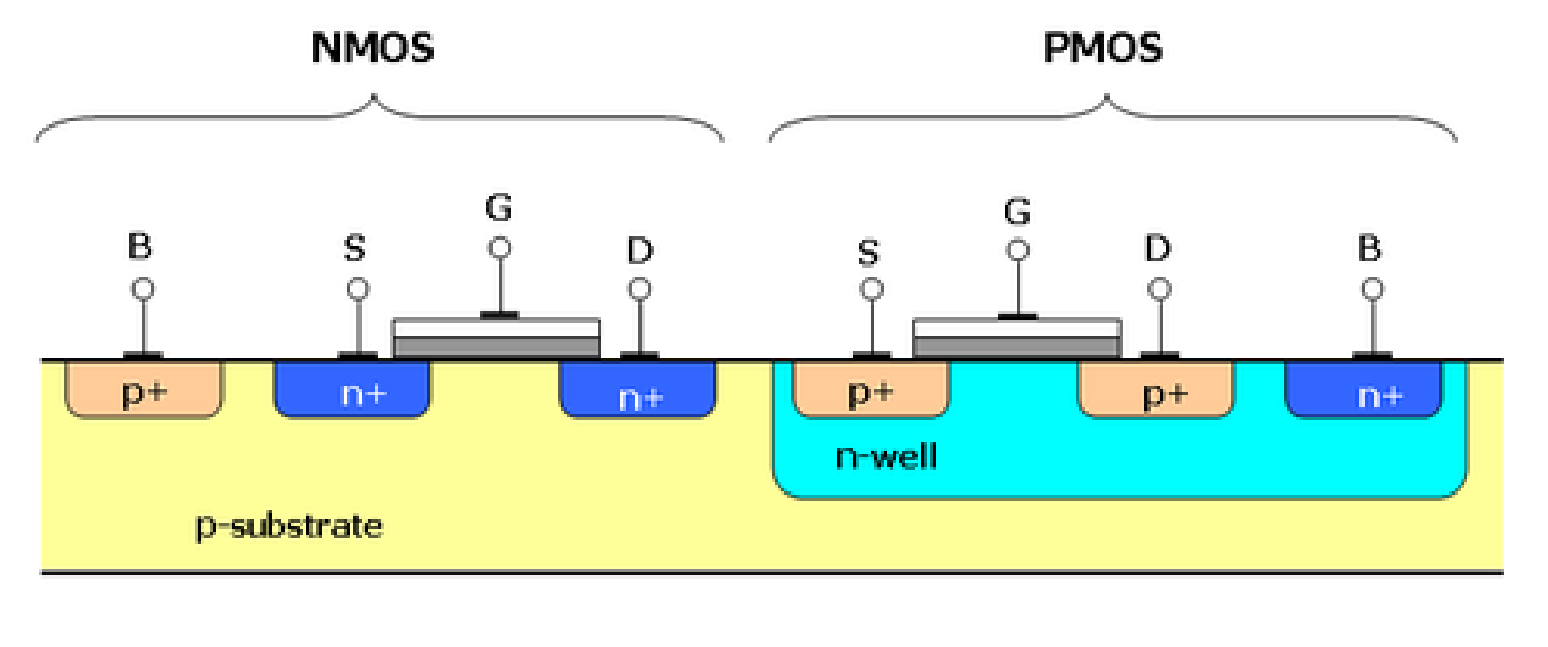
1960 1970 1980 1990 2000 2010 2020

Year

Halving time: 5.4 years

Dual logics: CMOS

CMOS: a key to VLSI/ULSI

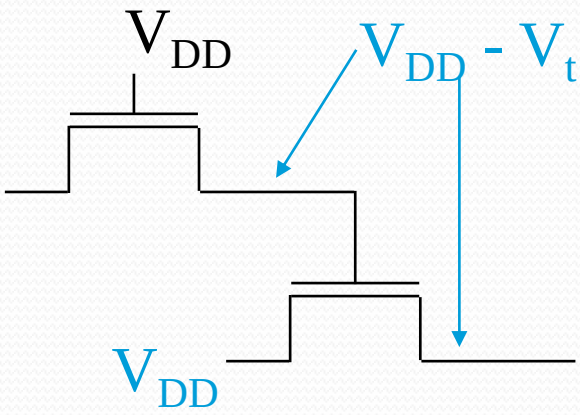


Remember HW on p-channel?

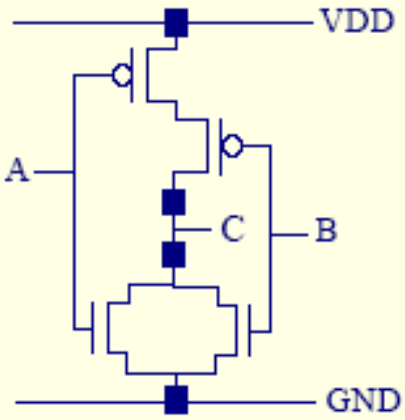
Source: wiki

Why CMOS?

- Threshold voltage requirement: voltage drop in each stage: example: n-channel



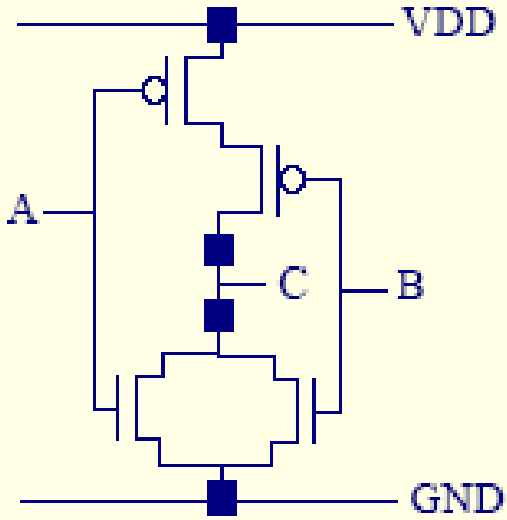
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

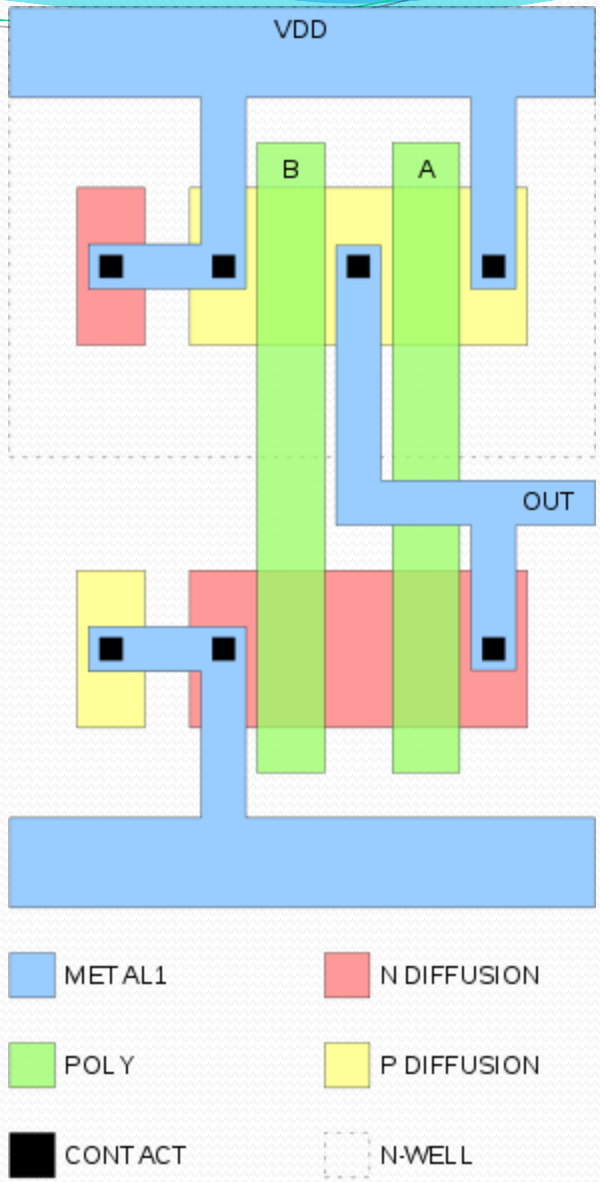


- n-channel MOSFET is “natural” for logic 0 (ex. ON: +5 V) , p-channel MOSFET is “natural” for logic 1 (ex. OFF: +5 V). Together: CMOS

CMOS example: NAND

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0



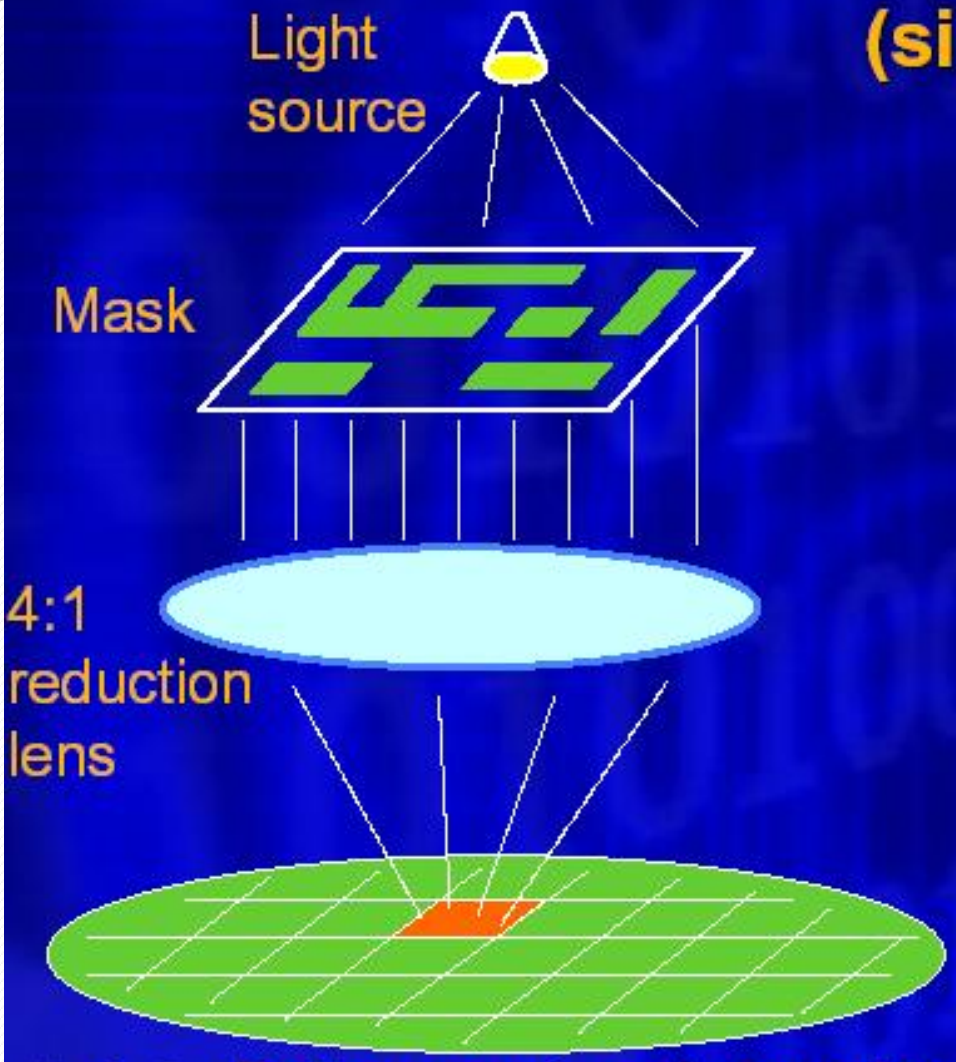


Source: wiki

Shrinking devices require increasing resolution lithography

Conventional Lithography

(simplified)



Conventional lithography has its limits

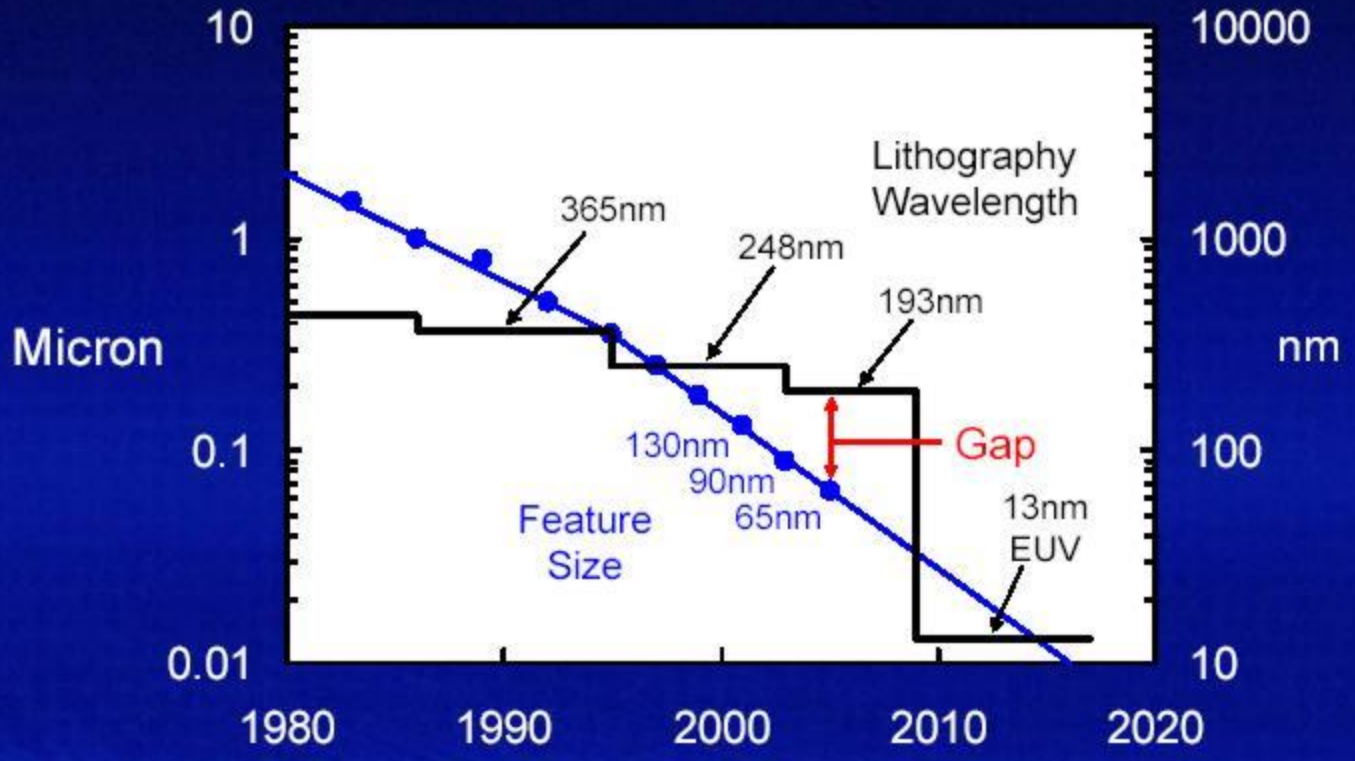
- Resolution adequate for 0.10 μm process, but no further
- Like trying to fill out a checkbook with a crayon

intel

Figure 2 The lens for DUV photolithography with the highest NA: Starlith 1900 from Carl Zeiss. The height of the lens is more than 1 m. The optical design and ray path are schematics and given only as an illustration. The inset depicts a resist structure of 36.5-nm half-pitch, obtained with the lens at full scanning speed. Main image courtesy of Zeiss; inset courtesy of ASML.

http://www.nature.com/nphoton/journal/v1/n11/covers/tech_focus_index.html

Lithography Challenge



Minimum feature size is scaling faster than lithography wavelength

Advanced photo mask techniques help to bridge the gap

What is Extreme Ultraviolet Lithography (EUVL)?

- EUV lithography uses extremely short wavelength light (factor of 20 shorter than today's lithography processes)

Visible light – 400 to 700 nm

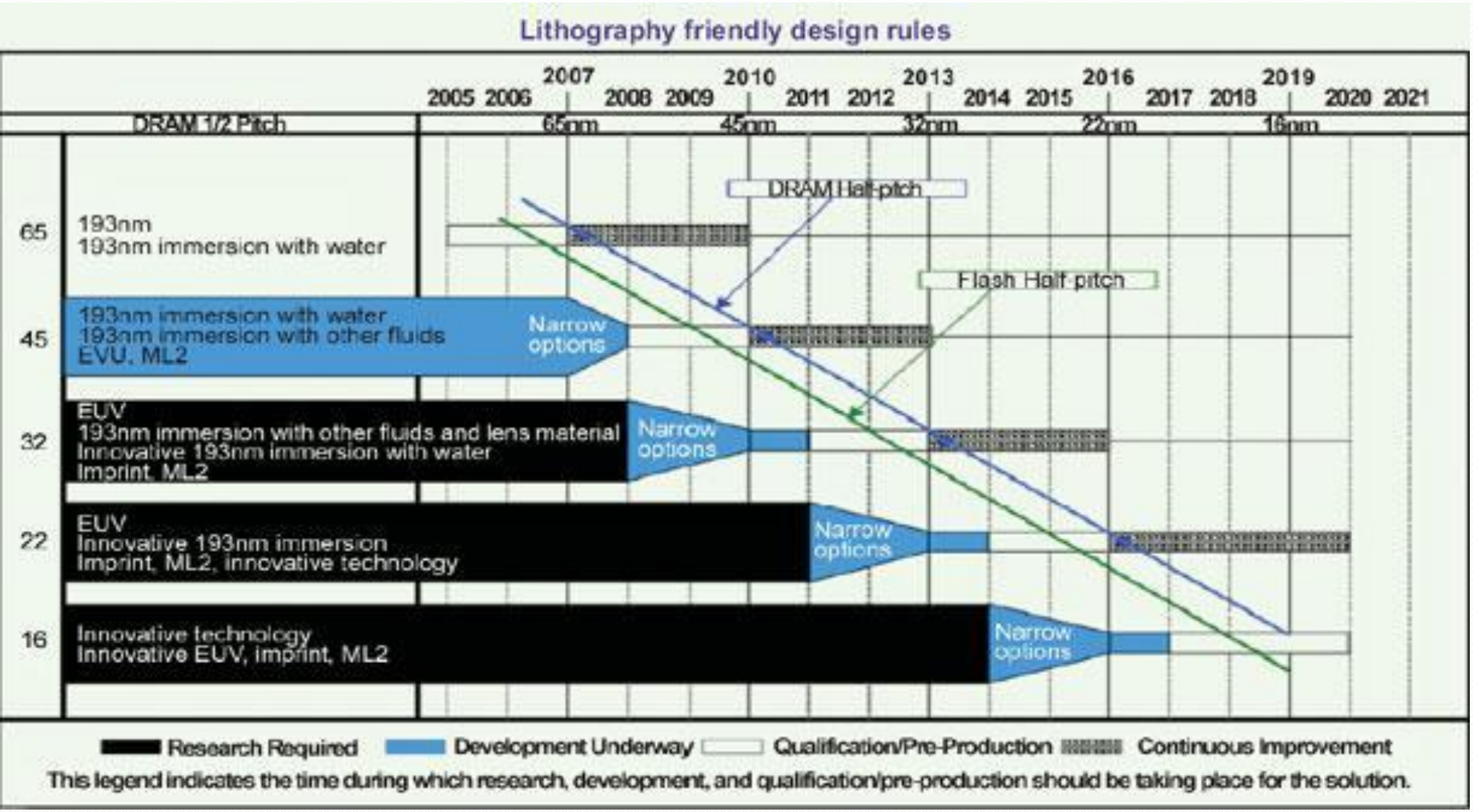
DUV lithography – 193 and 248 nm

EUV lithography – 13 nm

In use today

- Will be used first in 2005 by leading edge companies for critical lithography steps to produce 70 nm patterns for advanced circuit manufacturing to ***Maintain Moore's Law***

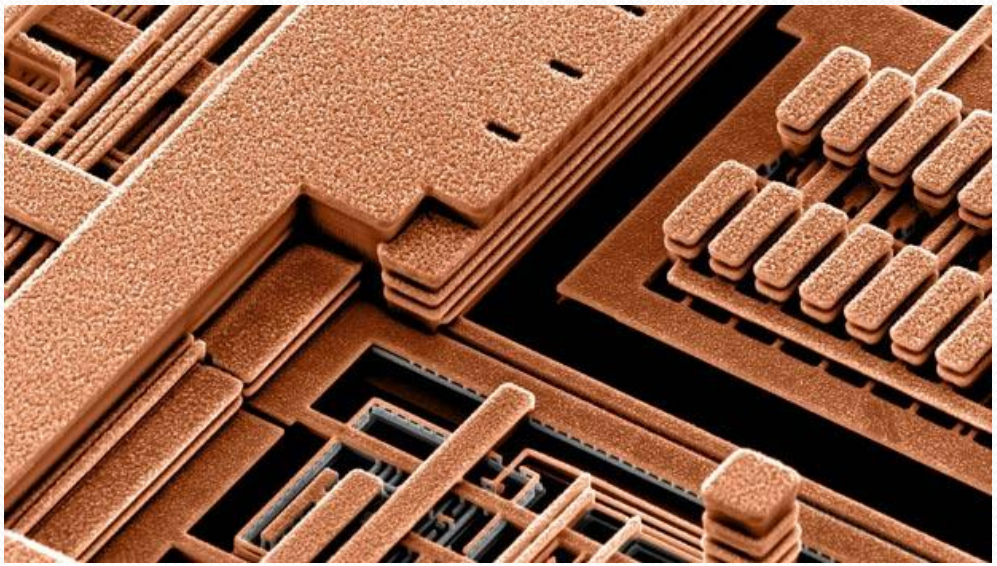
ITRS lithography roadmap



Connecting devices at high density requires good conductor

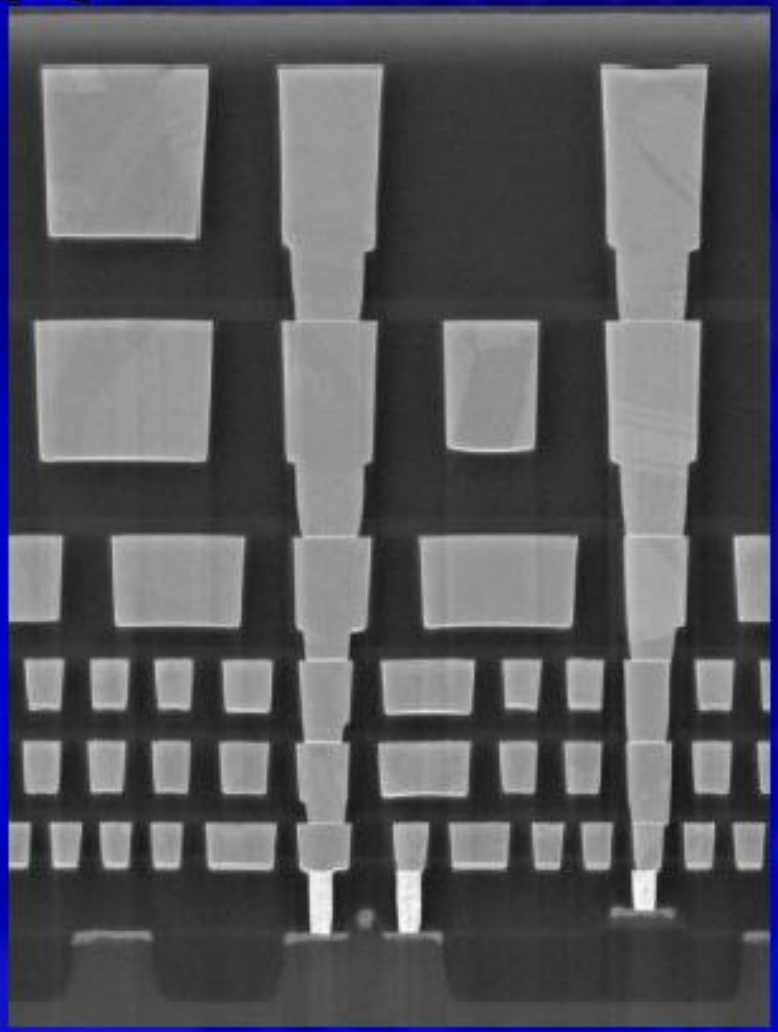
Metal Interconnect

- For many years... It has been aluminum
- 30+ years of research for a better conductor: copper
- Copper technology has finally arrived within the last 20 years...



Source: http://www-03.ibm.com/ibm/history/ibm100/us/en/icons/copperchip/

Copper Interconnects

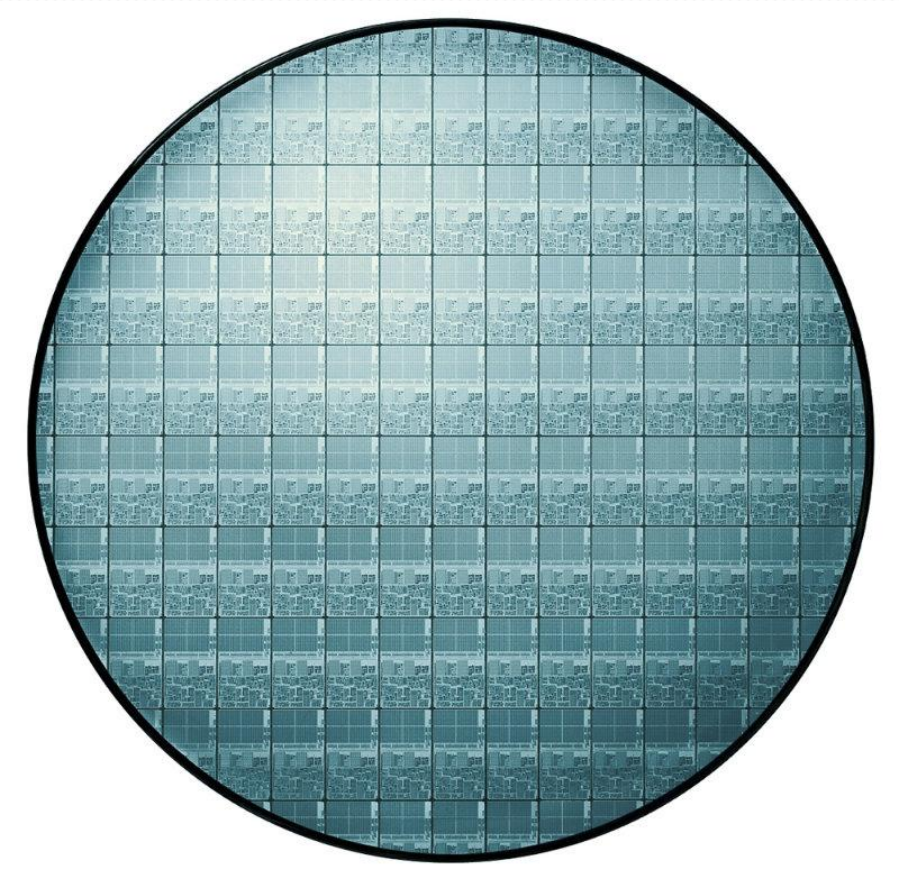


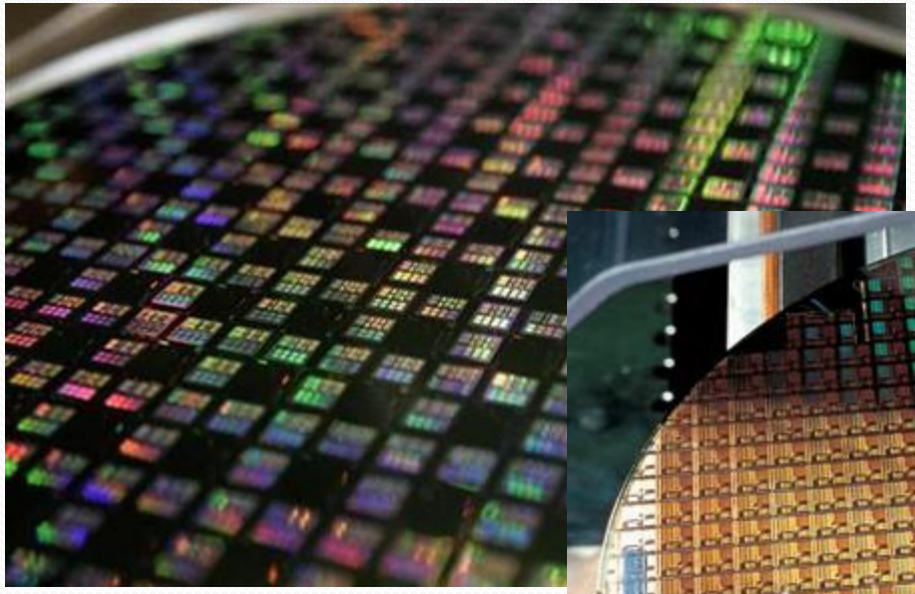
6 Layers of Damascene Copper

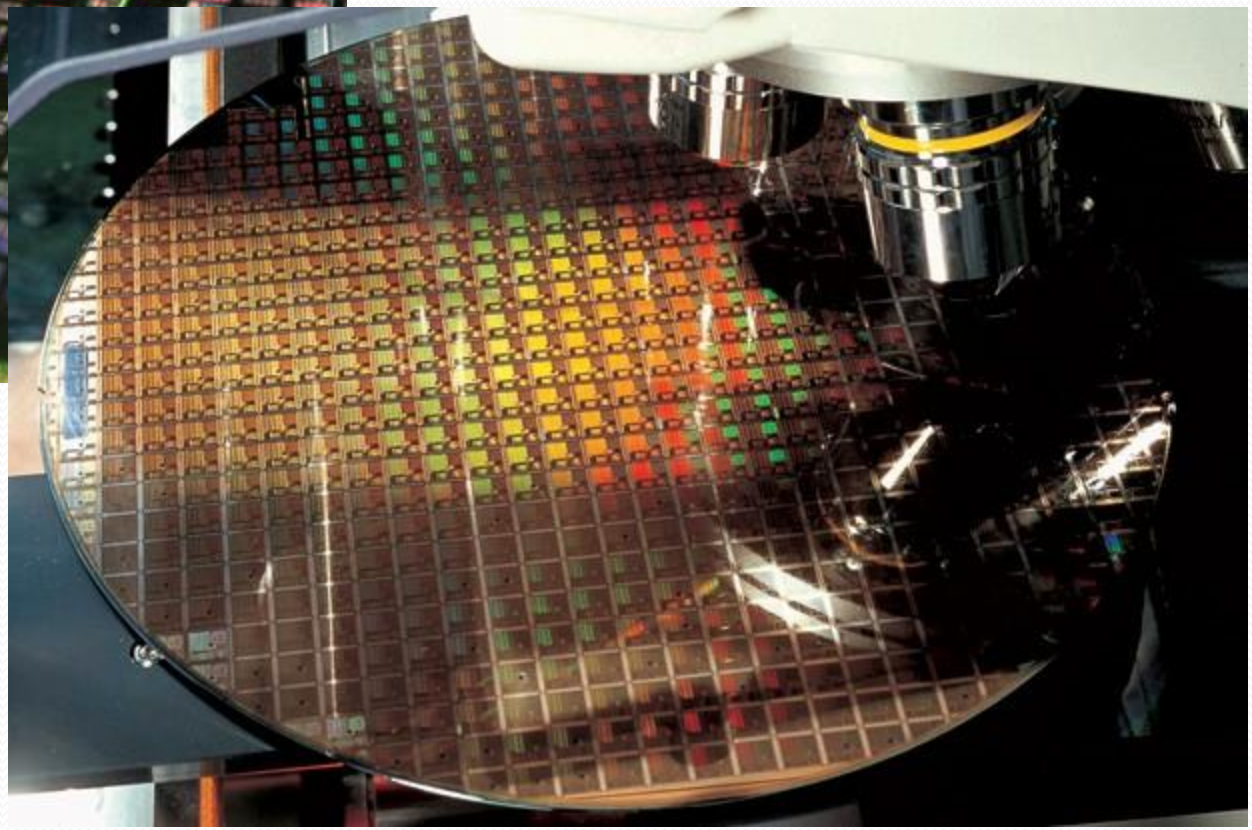
intel.

Price pressure: more devices per wafer – the advantage of economy of scale

More chips per wafer



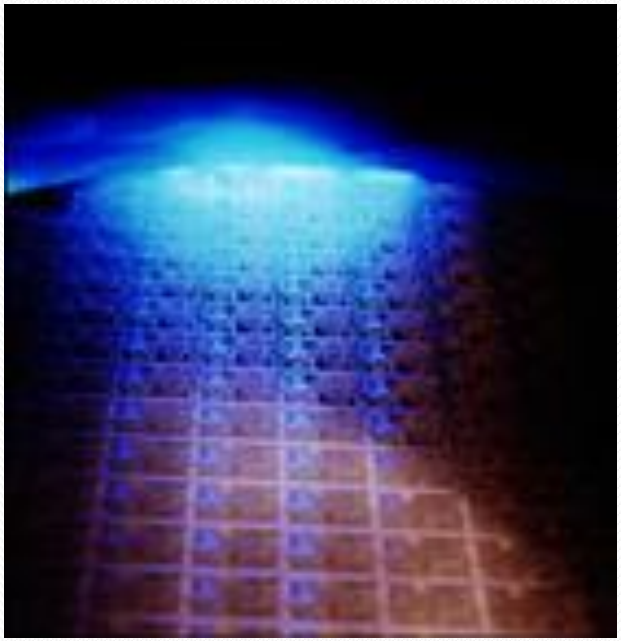




The economy of scales

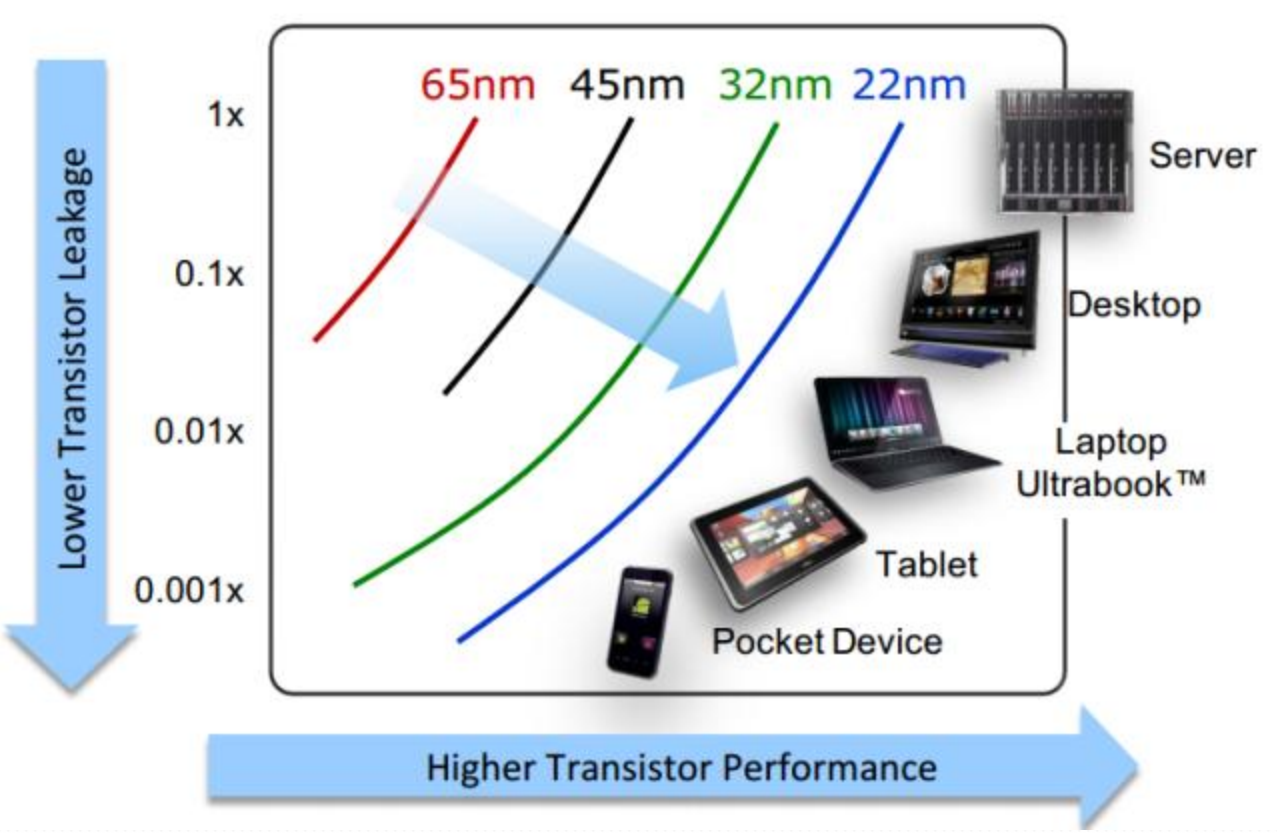
Large wafer…

Lots of chips (require high yield)



Chip architecture

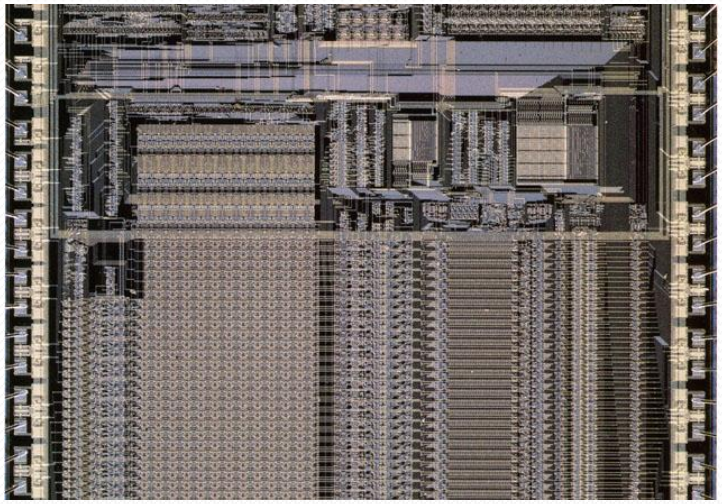
Application/Market-driven



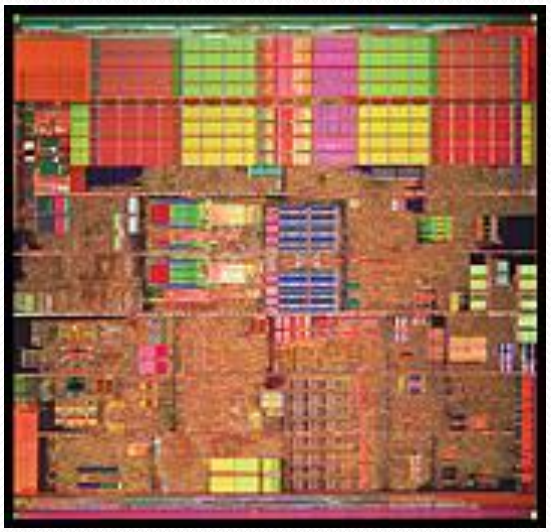
Not just size and integration, architecture is very apps-driven


HIGH PERFORMANCE
>3GHz
CPU
Networking
Games
1-3GHz
DTV
Laptop, Netbooks
MOBILE COMPUTING
Graphics
DIGITAL CONSUMER
Up to 1GHz
Tablets
STB
LOW POWER
Feature phones
Smartphones
Wireless Connectivity
Lower cost
Watts
Desktop
Up to '00s mW
Up to '0s mW
Mobile
Performance

The “Old-Time Story” of RISC vs. CISC



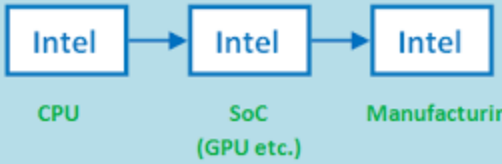
ARM



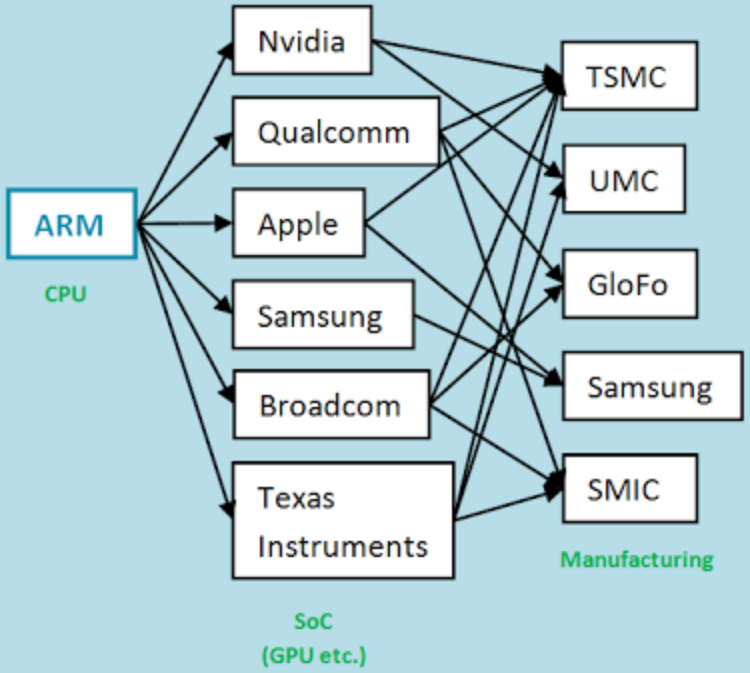
x86

- Specialized architectures for different applications

Intel vs. ARM



Intel Market Cap ~ $140 Billion



ARMy Market Cap > $700 Billion

S. K. Jayanarayanan
kartik.jayan@gmail.com
March 2012

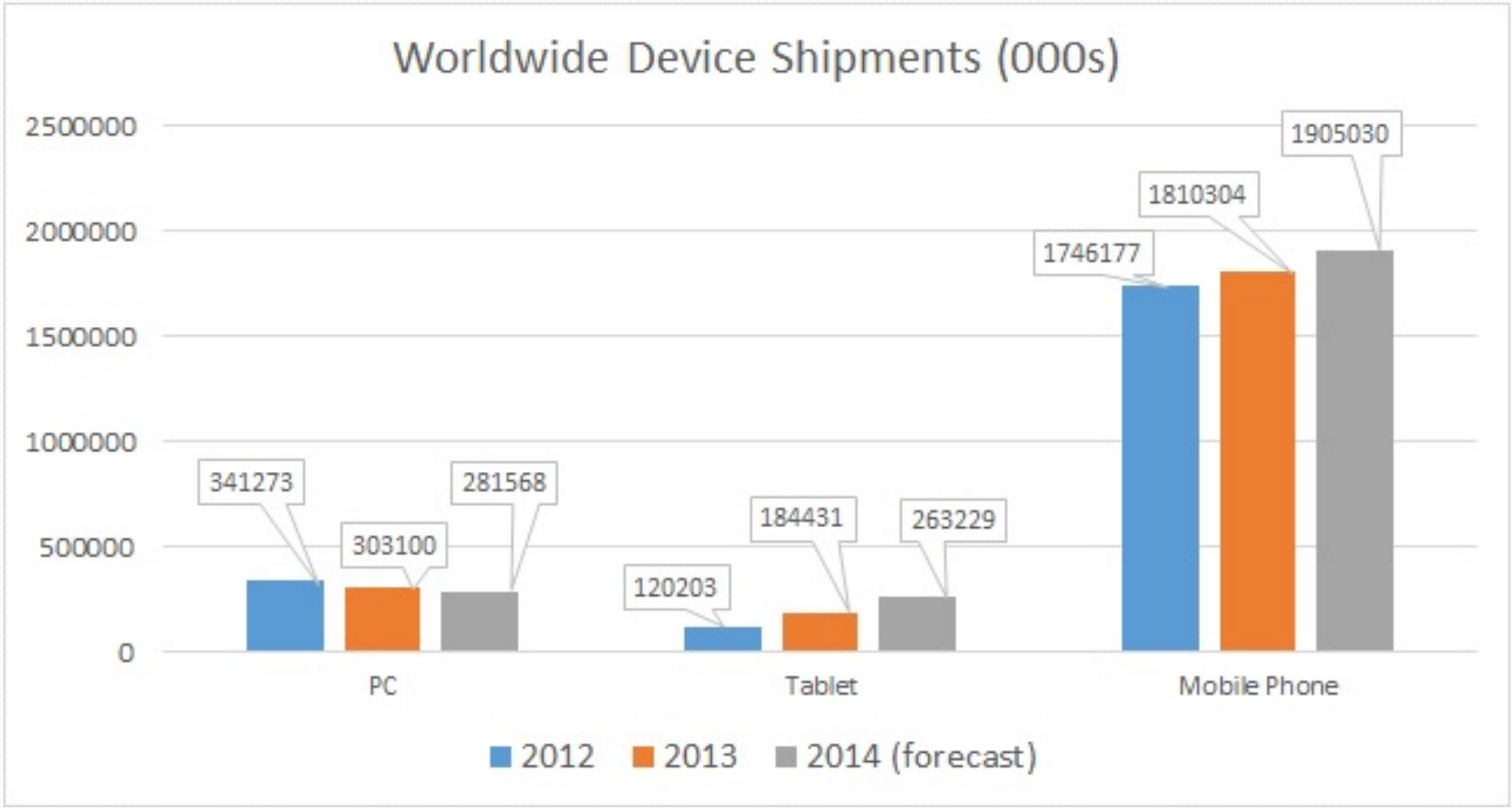
The fast evolving market

Morgan Stanley

Mobile Internet
Next Major Computing Cycle

Source: Mary Meeker

Mainframe **Computing** **1950s**	***Mini*** **Computing** **1960s**	***Personal*** **Computing** **1980s**	***Desktop Internet*** **Computing** **1990s**	***Mobile Internet*** **Computing** **2000s**
				


Worldwide Device Shipments (000s)
2500000
2000000
1500000
1000000
500000
0
341273
303100
281568
120203
184431
263229
1746177
1810304
1905030
PC
Tablet
Mobile Phone
2012
2013
2014 (forecast)

Technology is driven by the market & industrial players

Top 10 IC Wafer Capacity Leaders* as of Dec-2013 (200mm-Equiv. Wafers per Month x1000)

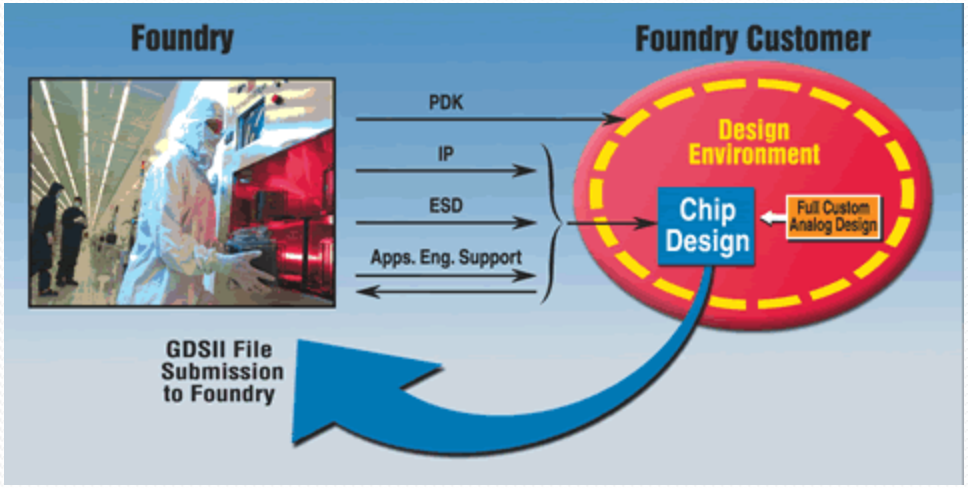
2013 Rank	Company	Headquarters Region	Installed Capacity (K w/m)	% of Worldwide Total
1	Samsung	South Korea	1,867	12.6%
2	TSMC	Taiwan	1,475	10.0%
3	Micron**	Americas	1,380	9.3%
4	Toshiba/SanDisk	Japan	1,177	8.0%
5	SK Hynix	South Korea	1,035	7.0%
6	Intel	Americas	961	6.5%
7	ST	Europe	551	3.7%
8	UMC	Taiwan	520	3.5%
9	GlobalFoundries	Americas	482	3.3%
10	TI	Americas	441	3.0%
—	Total	—	9,889	66.8%

*Includes shares of capacity from joint ventures.

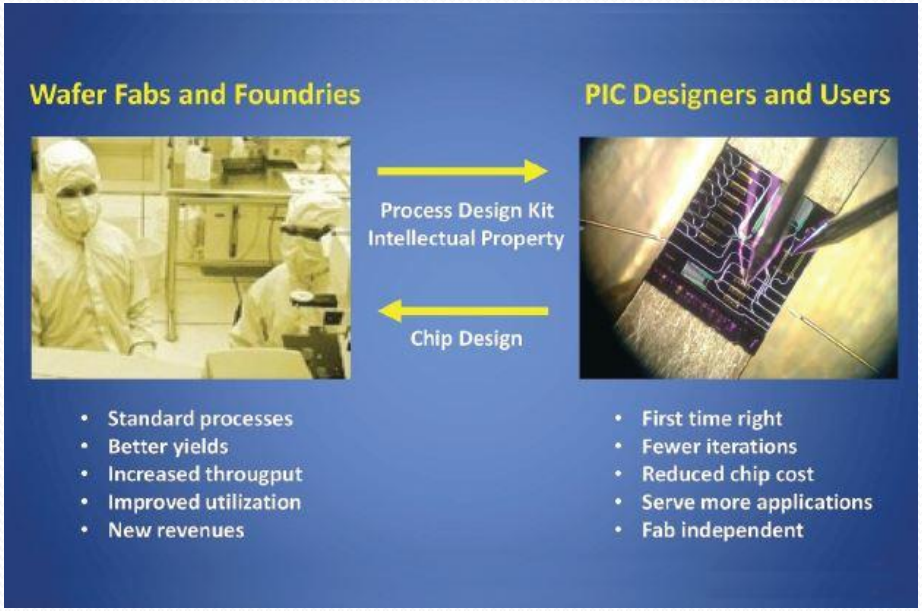
Source: Companies, IC Insights

**Includes the former Elpida and Rexchip fabs.

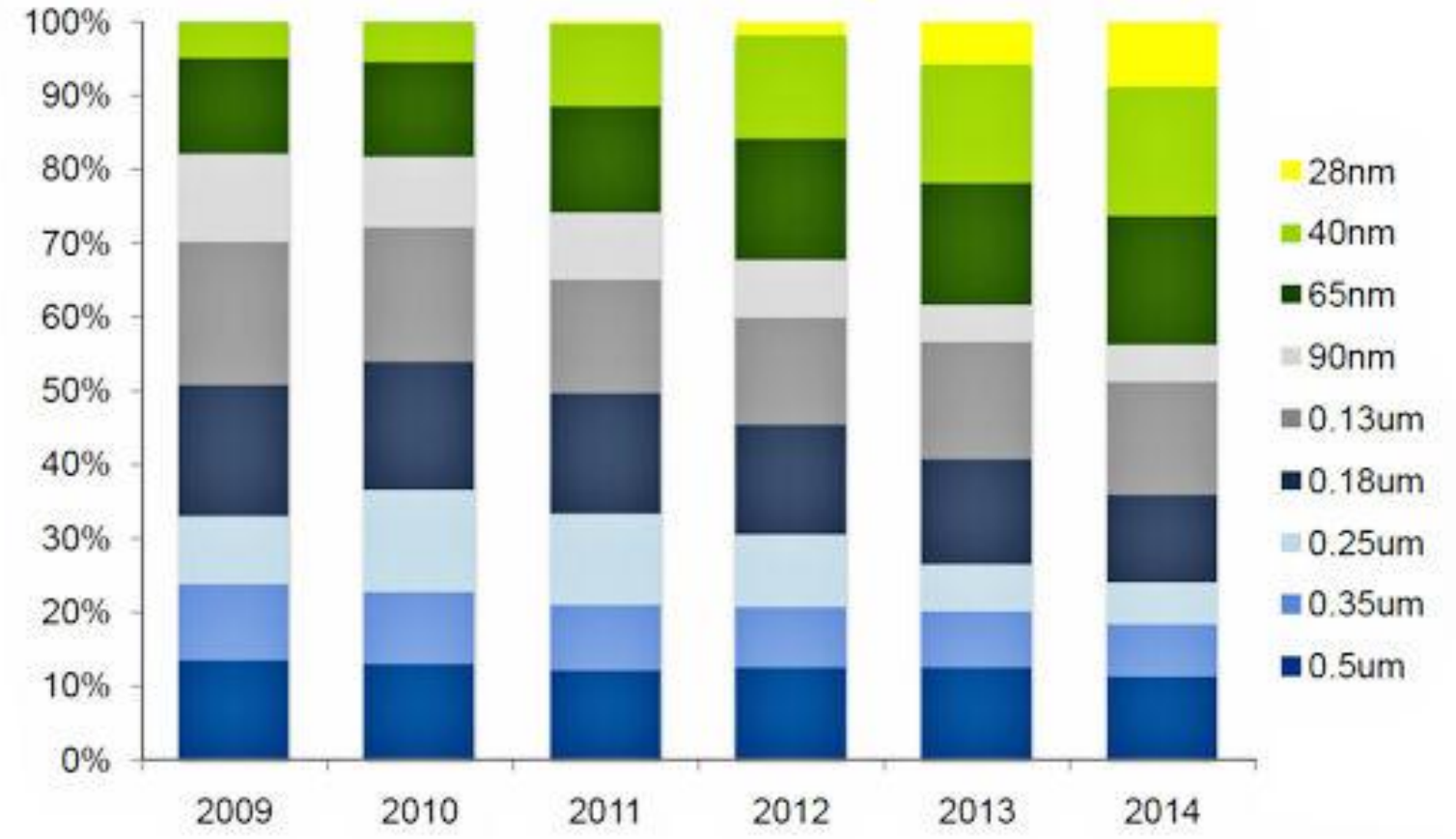
Foundry and Chip Design



http://www.techbriefs.com/component/content/article/15547

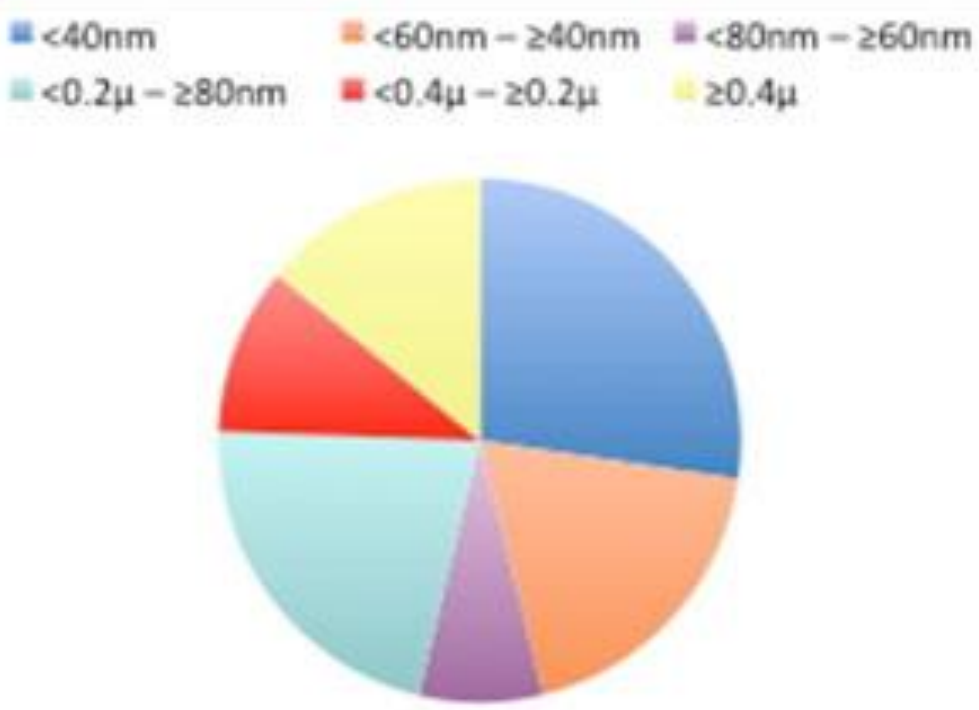


Foundry Capacity by Technologies



Gartner

Worldwide Capacity by Minimum Geometry as of Dec-2012
(Installed Monthly Capacity in 200mm-Equiv. Wafers x1000)



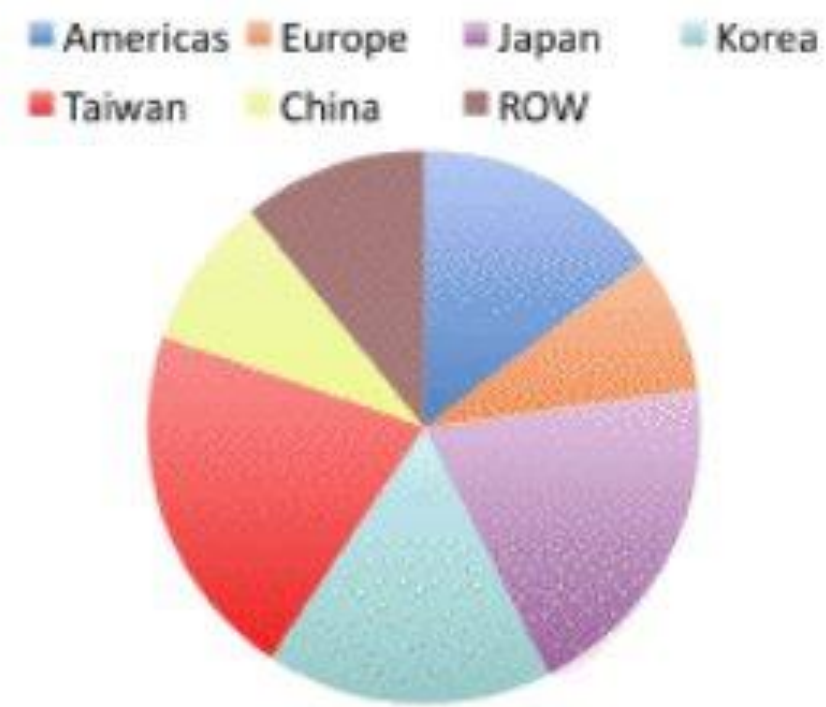
Minimum Geometry	Installed Capacity (K w/m)	% of Worldwide Total
<40nm	3,963.1	27.3%
<60nm – ≥40nm	2,721.0	18.8%
<80nm – ≥60nm	1,106.6	7.6%
<0.2µ – ≥80nm	3,165.5	21.8%
<0.4µ – ≥0.2µ	1,495.8	10.3%
≥0.4µ	2,044.9	14.1%
TOTAL	14,497.0	100%

Source: IC Insights

Figure 1

Worldwide Capacity by Geographic Region as of Jul-2011

(Installed Monthly Capacity in 200mm-Equiv. Wafers x1000)



Region	Installed Capacity (K w/m)	% of Worldwide Total
Americas	1,995.1	14.7%
Europe	1,109.3	8.1%
Japan	2,683.6	19.7%
Korea	2,293.5	16.8%
Taiwan	2,858.3	21.0%
China	1,208.9	8.9%
ROW	1,469.2	10.8%
TOTAL	13,617.8	100%

Source: IC Insights

Perspectives from industrial players

Intel Logic Technology Roadmap

	32 nm		22 nm		14 nm		10 nm	
Name:	P1268	P1269	P1270	P1271	P1272	P1273	P1274	P1275
Product:	CPU	SoC	CPU	SoC	CPU	SoC	CPU	SoC

Manufacturing → Development → Research

Intel develops both CPU and SoC versions of each generation

Brief Update on14nm Status

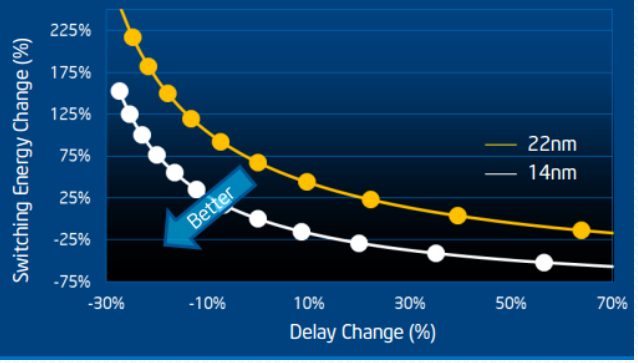
Yield

at the same point in development

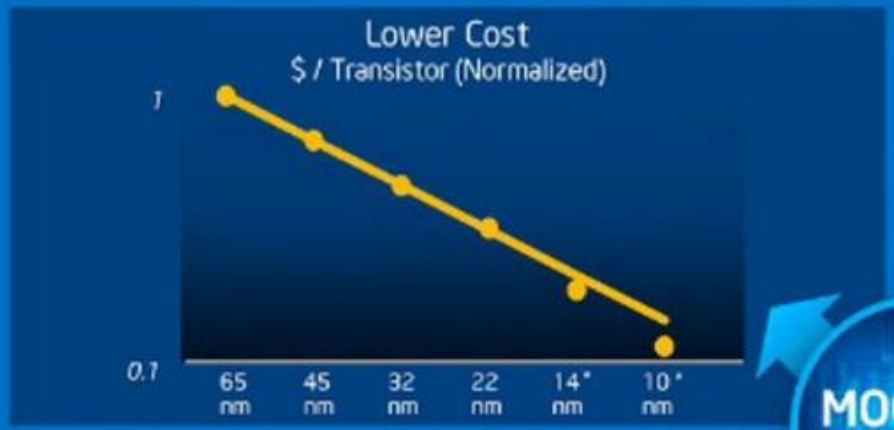
Yield rapidly increasing, on track for matched yield in Q1 '14 *

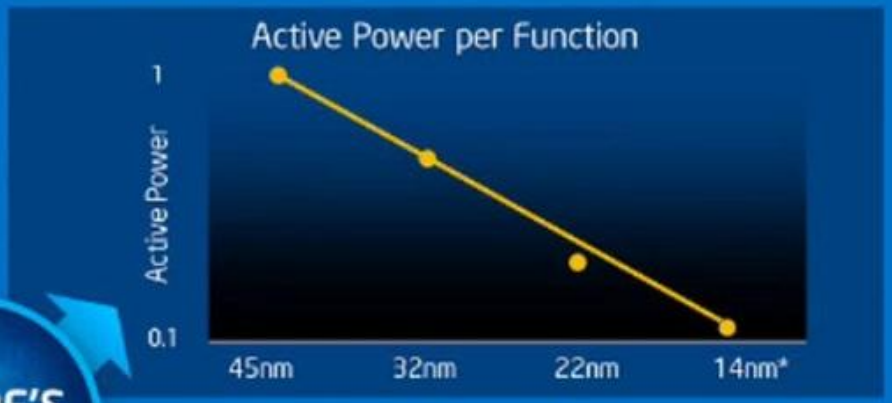
Performance Improvement

Switching Energy vs. Gate Delay

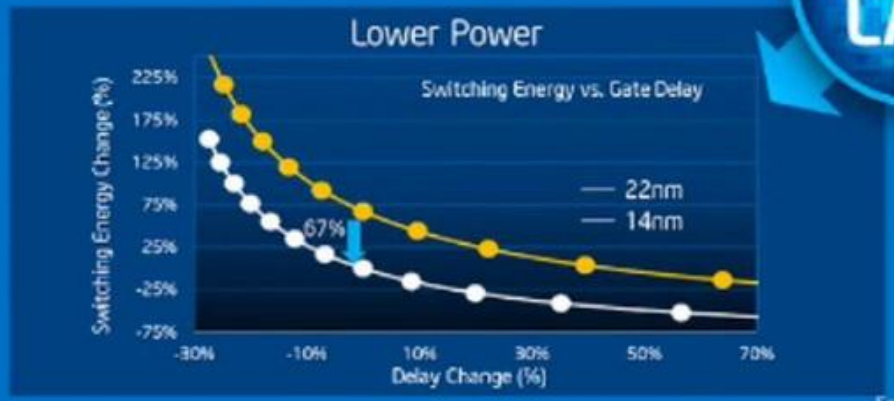


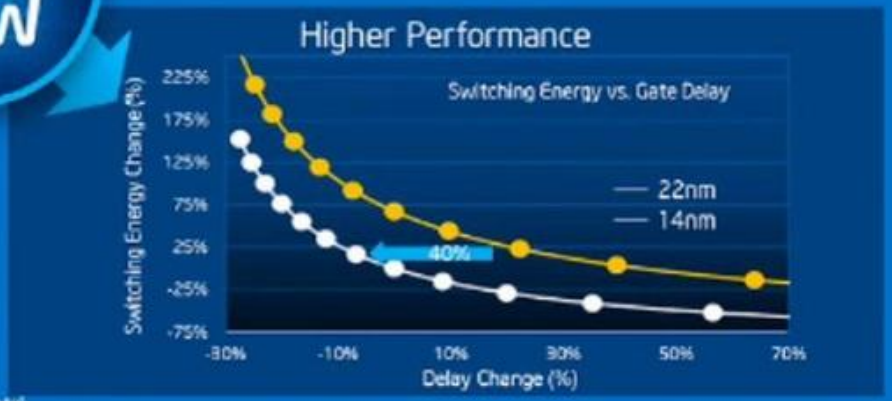
Getting Benefits of Moore's Law Across all Value Vectors



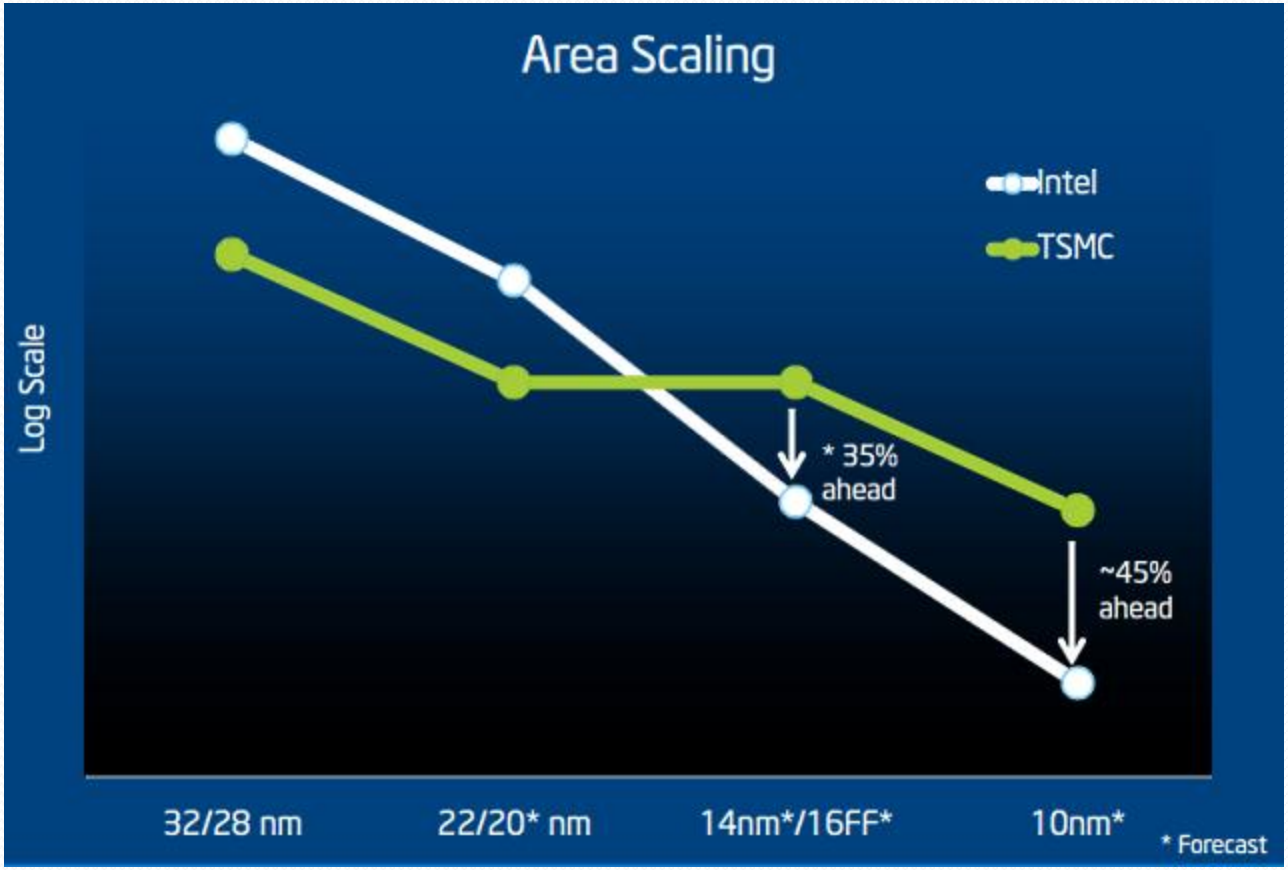


MOORE'S LAW

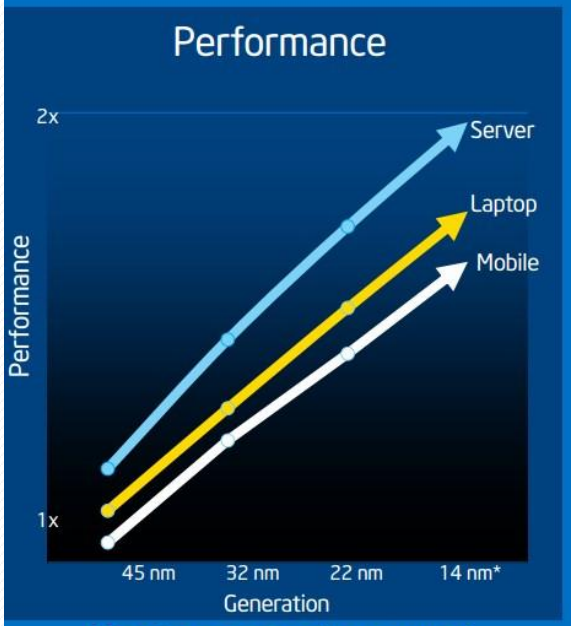




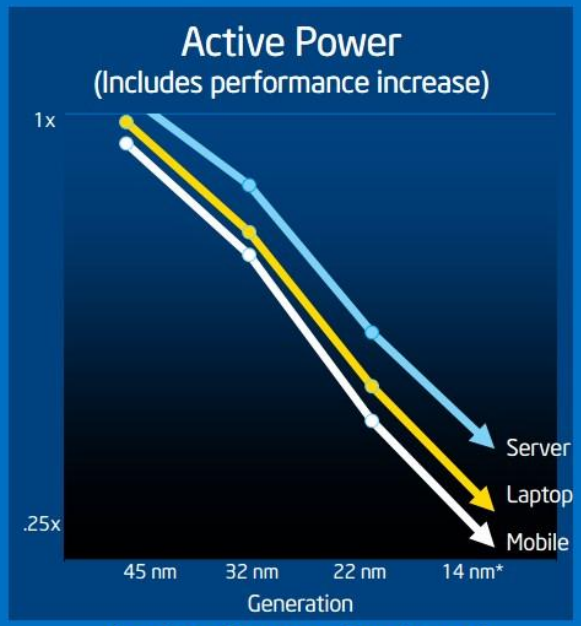
Source: Intel


Area Scaling
Intel
TSMC
Log Scale
* 35%
ahead
~45%
ahead
32/28 nm
22/20* nm
14nm*/16FF*
10nm*
* Forecast

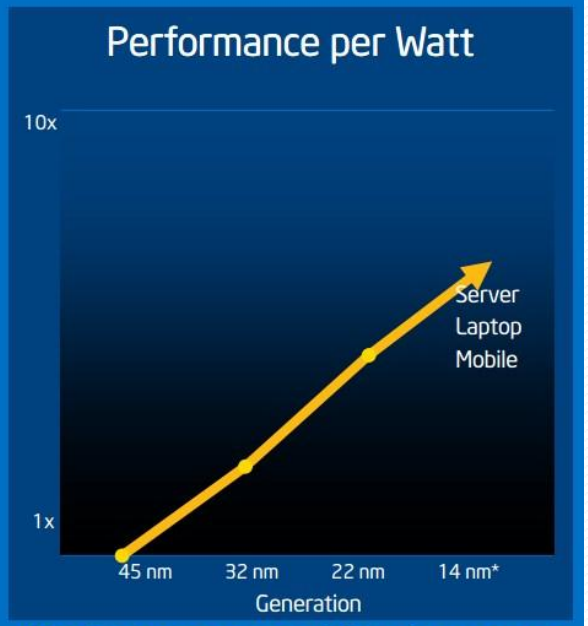
Different Improvement Focus for Different Segments



Performance Improved for All Product Families

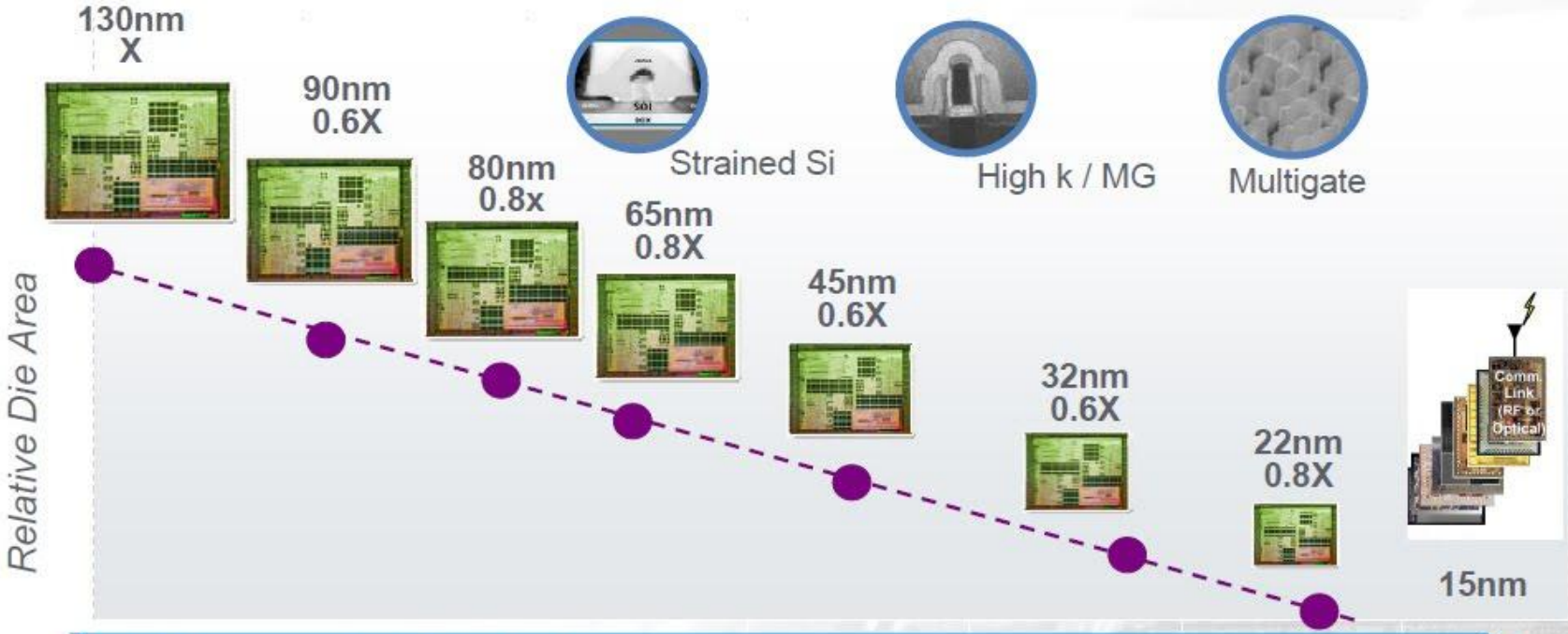


Active Power Reduced for All Product Families



Performance per Watt Improves >1.6x per Generation

Three Key Technology Enablers



Lithography Enabled

- Density
- Power / Performance
- Cost

Materials Enabled

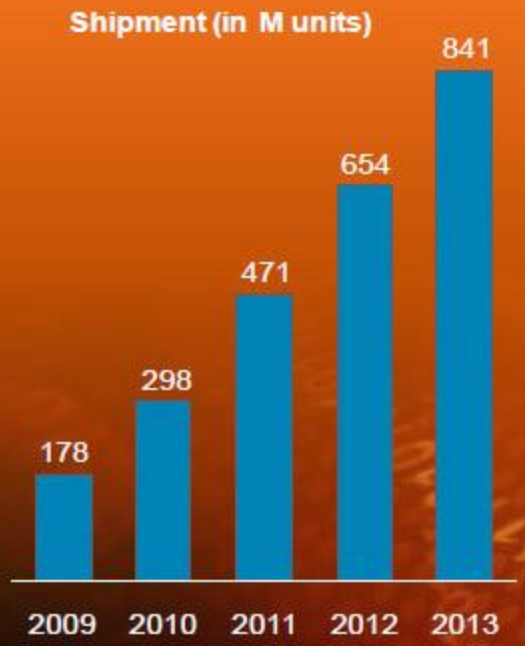
- Power / Performance
- Strained Silicon
- High K / Metal Gates
- FinFETs

3D enabled

- Density
- Functionality
- Integration

Low Power Is Critical For Mobility Market

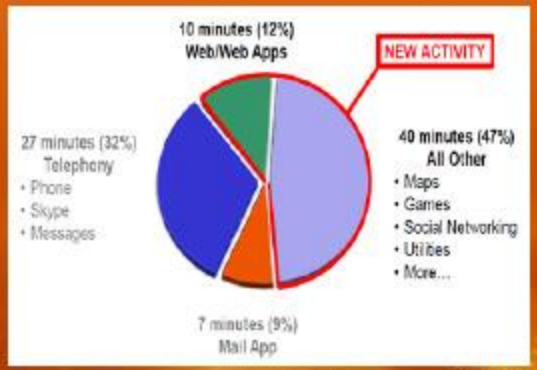
Explosive growth in smartphone sales



Source: Gartner

New consumer appetite , driving more compute

Average daily use of smartphone

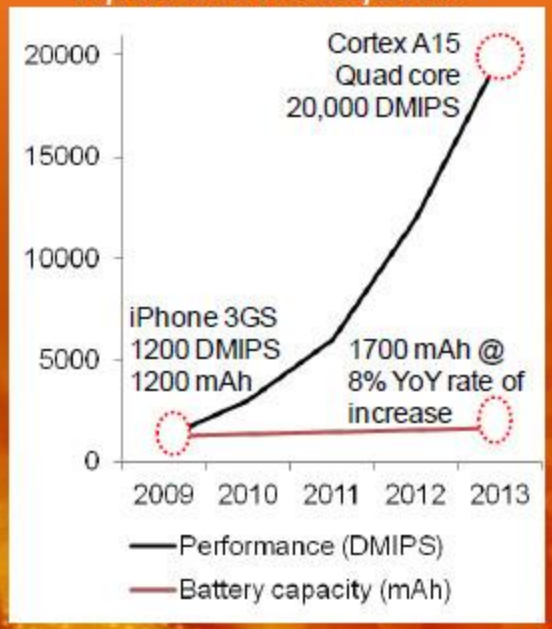


Source: KPCB

60% time spent on smartphones is new activity for mobile users

…However, battery technology fails to keep up with Moore's law

Performance versus battery life improvement in smartphones



Source: GLOBALFOUNDRIES

Product Leadership Is More Than "Just The Fin"

Full suite PDK

FinFET models, advanced extraction, double patterning, DFM, FFM, Ref flows, P&R…

Power/Perf optimized CPU Solutions

Multi Vt, DVFS, power management, CPU POP…

Mobile SoC platform

Optimized libraries , IPs suite, low power flow….

14XM

Multicore GPU solutions

UHD 8T std cells, GPU POP….

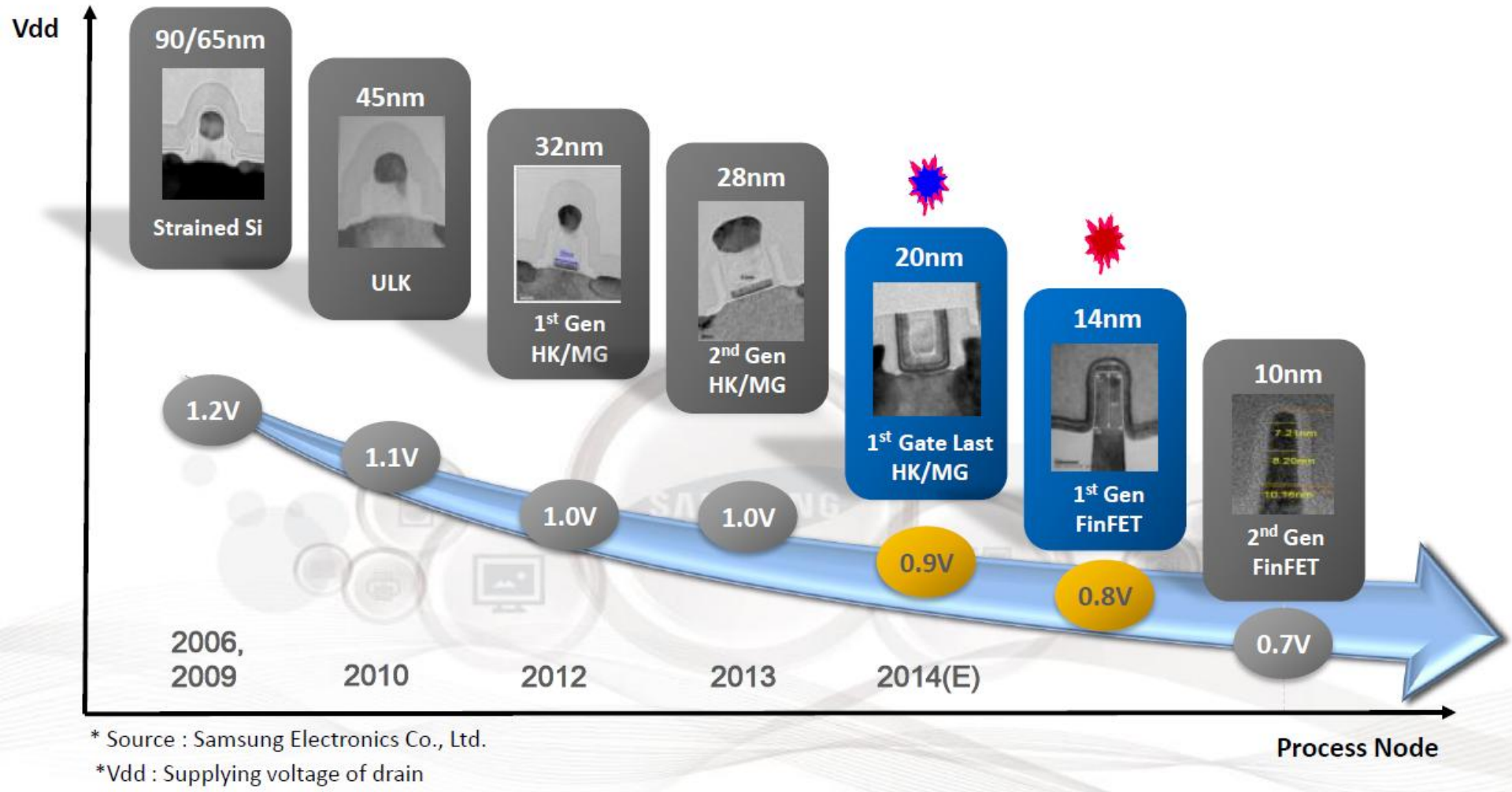
CCS platform

(CCS=Compute, Connect, Storage)

Optimized libraries , IPs suite, HD memory solution, HS SERDES…

2.5D and 3D Packaging

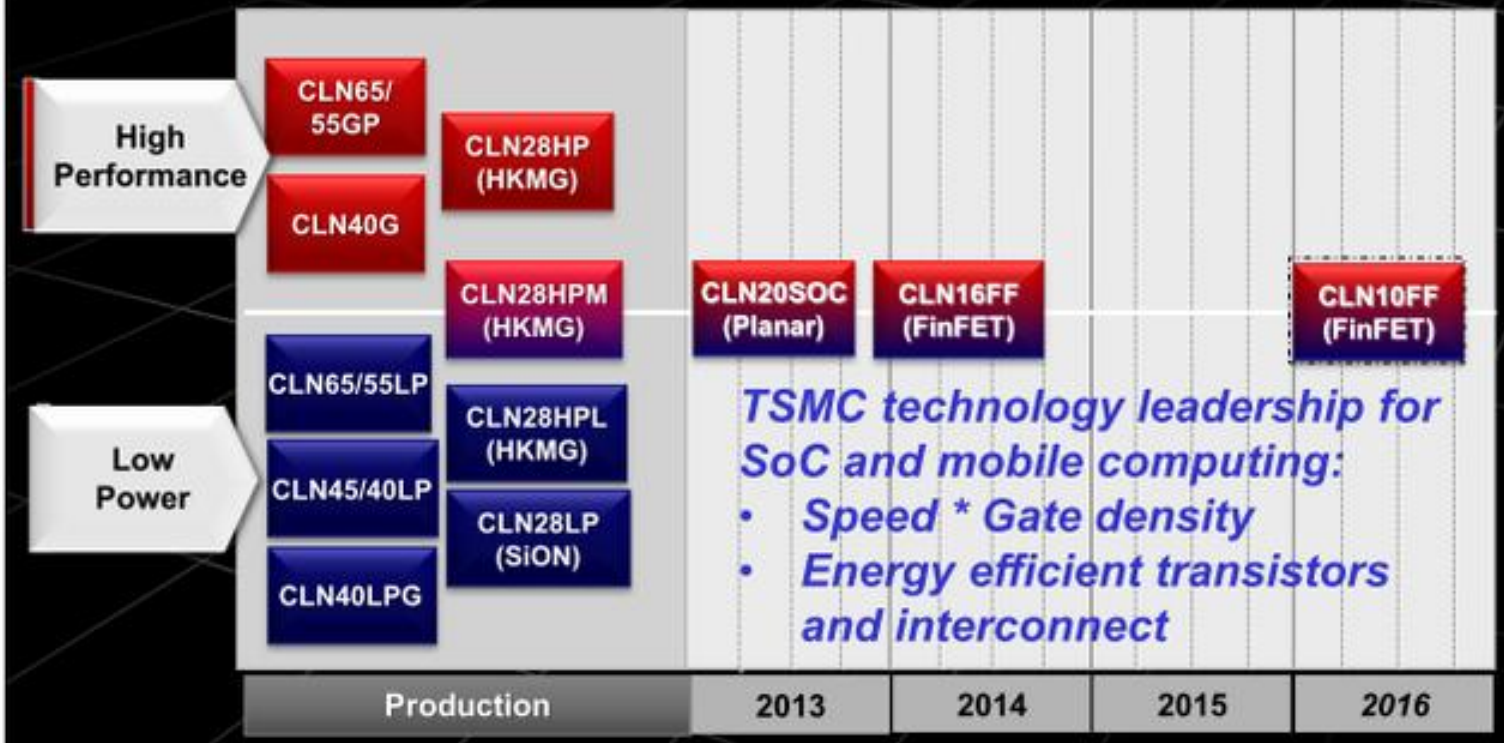
Logic+memory, wide IO , Heterogeneous Stacking …



* Source : Samsung Electronics Co., Ltd.

*Vdd : Supplying voltage of drain

TSMC Technology Roadmap



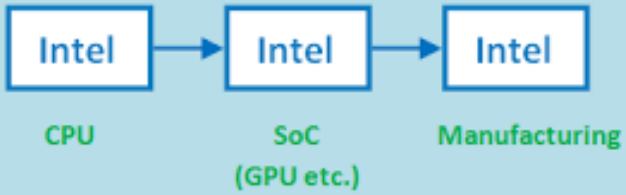
Box left edge: risk production. Right edge: no meaning

10nm preliminary subject to change

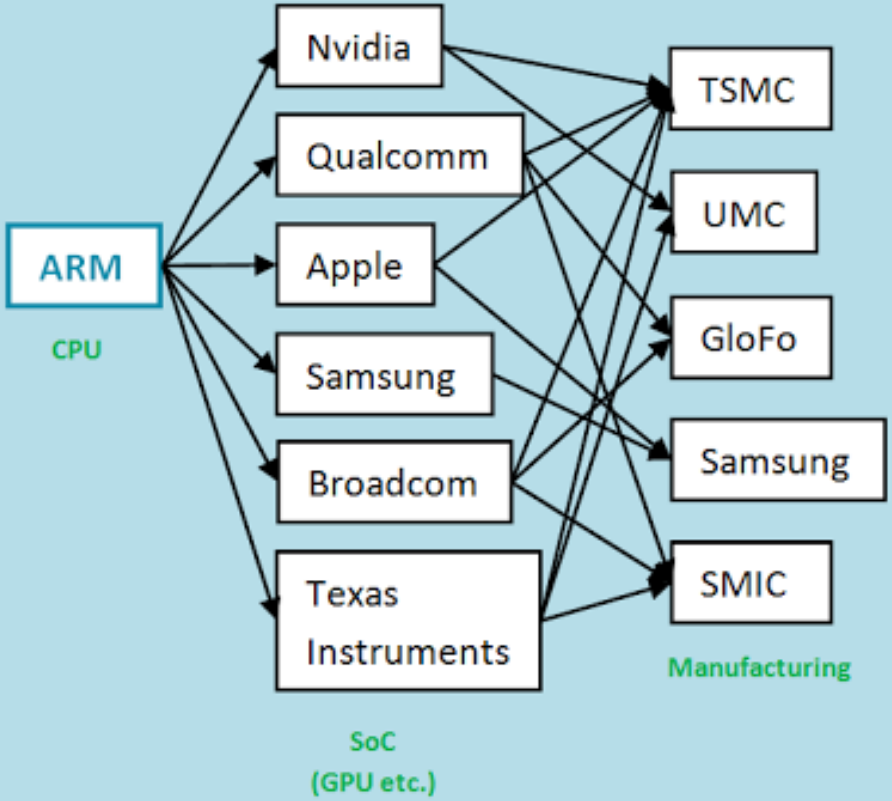
Open Innovation Platform®

The battle of chip architecture

Intel vs. ARM

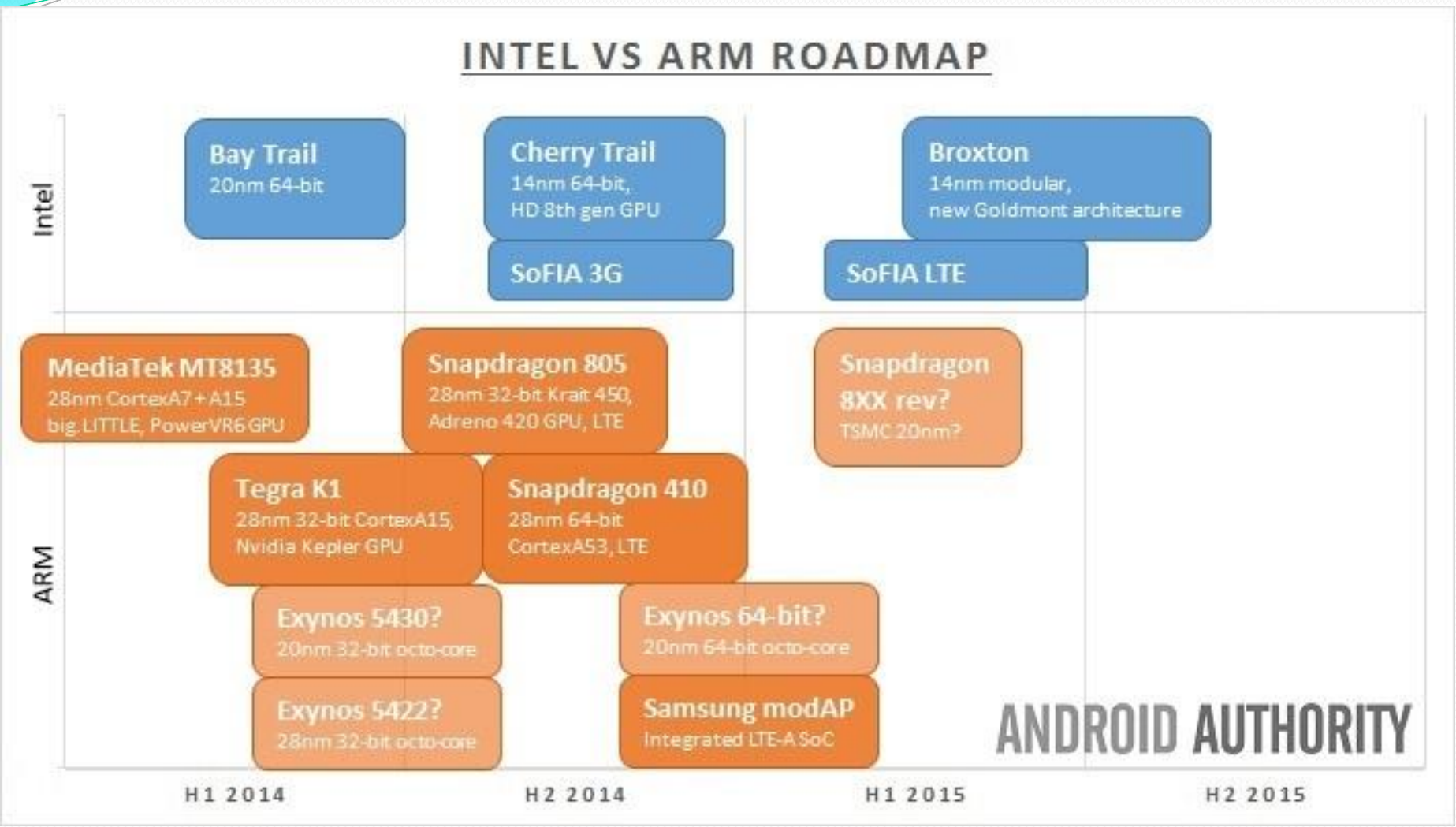


Intel Market Cap ~ $140 Billion

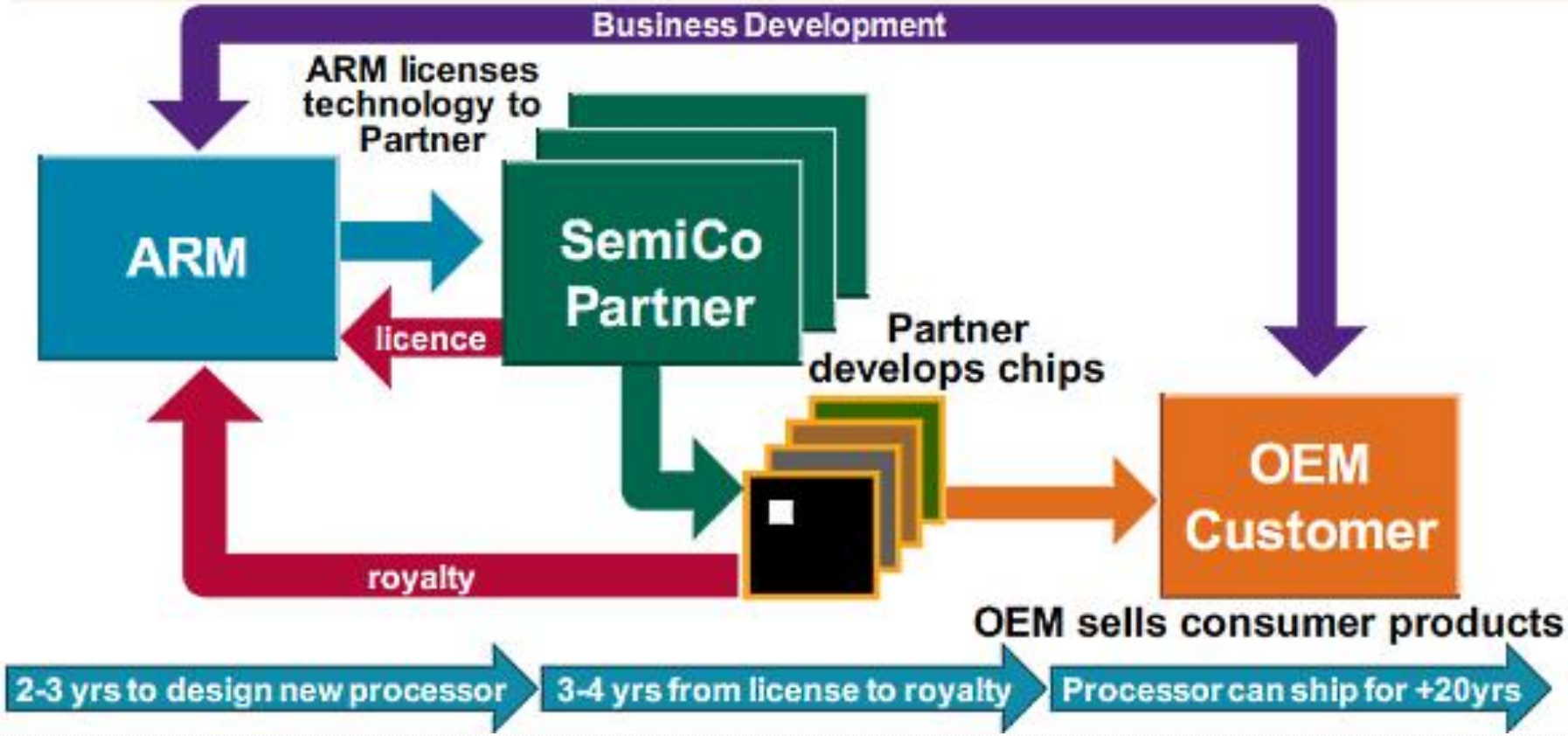


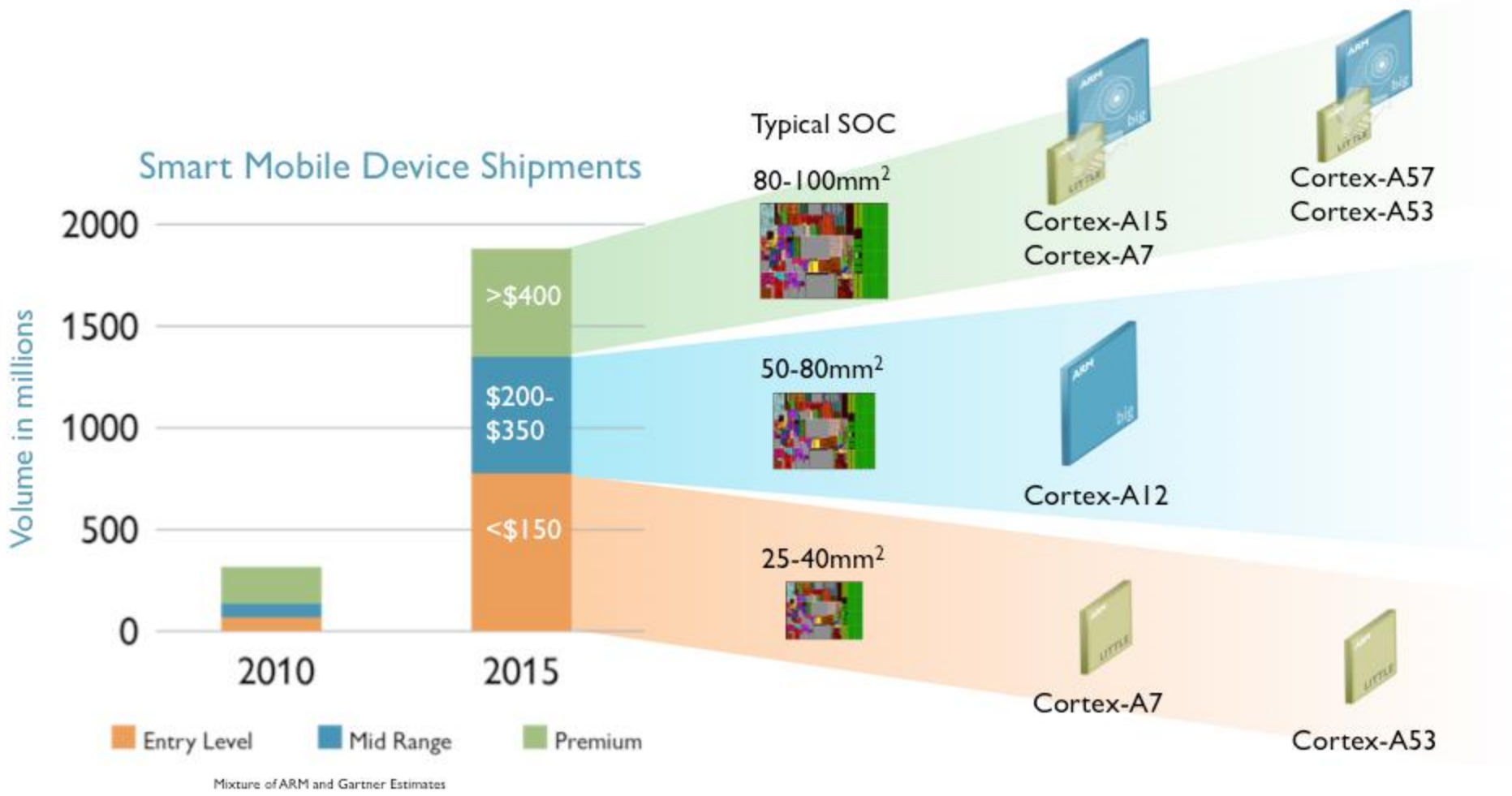
ARMy Market Cap > $700 Billion

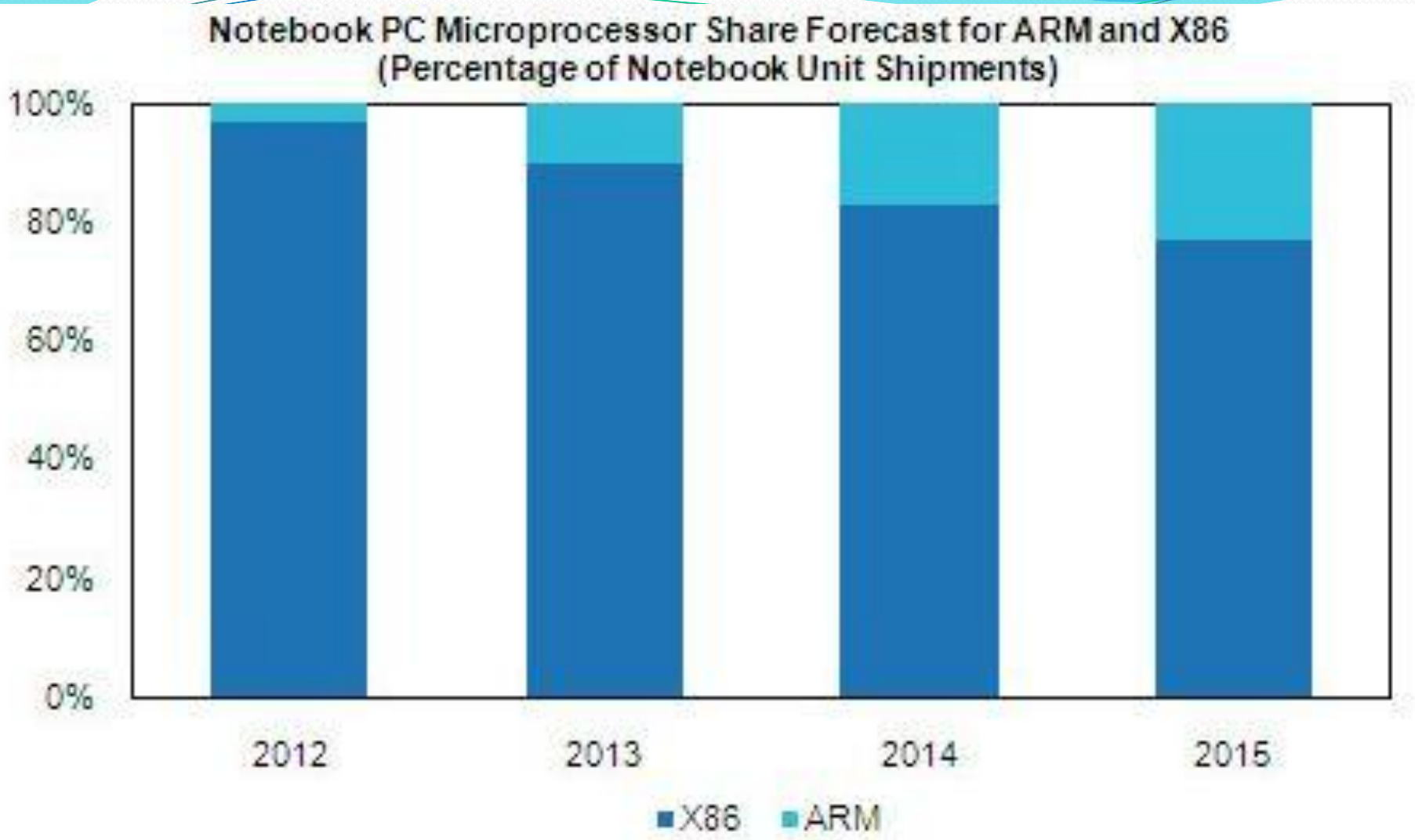
S. K. Jayanarayanan
kartik.jayan@gmail.com
March 2012


INTEL VS ARM ROADMAP
Intel
ARM
Bay Trail
20nm 64-bit
Cherry Trail
14nm 64-bit,
HD 8th gen GPU
SoFIA 3G
Broxton
14nm modular,
new Goldmont architecture
SoFIA LTE
MediaTek MT8135
28nm CortexA7+A15
big.LITTLE, PowerVR6 GPU
Snapdragon 805
28nm 32-bit Krait 450,
Adreno 420 GPU, LTE
Snapdragon
8XX rev?
TSMC 20nm?
Tegra K1
28nm 32-bit CortexA15,
Nvidia Kepler GPU
Snapdragon 410
28nm 64-bit
CortexA53, LTE
Exynos 5430?
20nm 32-bit octo-core
Exynos 64-bit?
20nm 64-bit octo-core
Exynos 5422?
28nm 32-bit octo-core
Samsung modAP
Integrated LTE-A SoC
ANDROID AUTHORITY
H1 2014
H2 2014
H1 2015
H2 2015

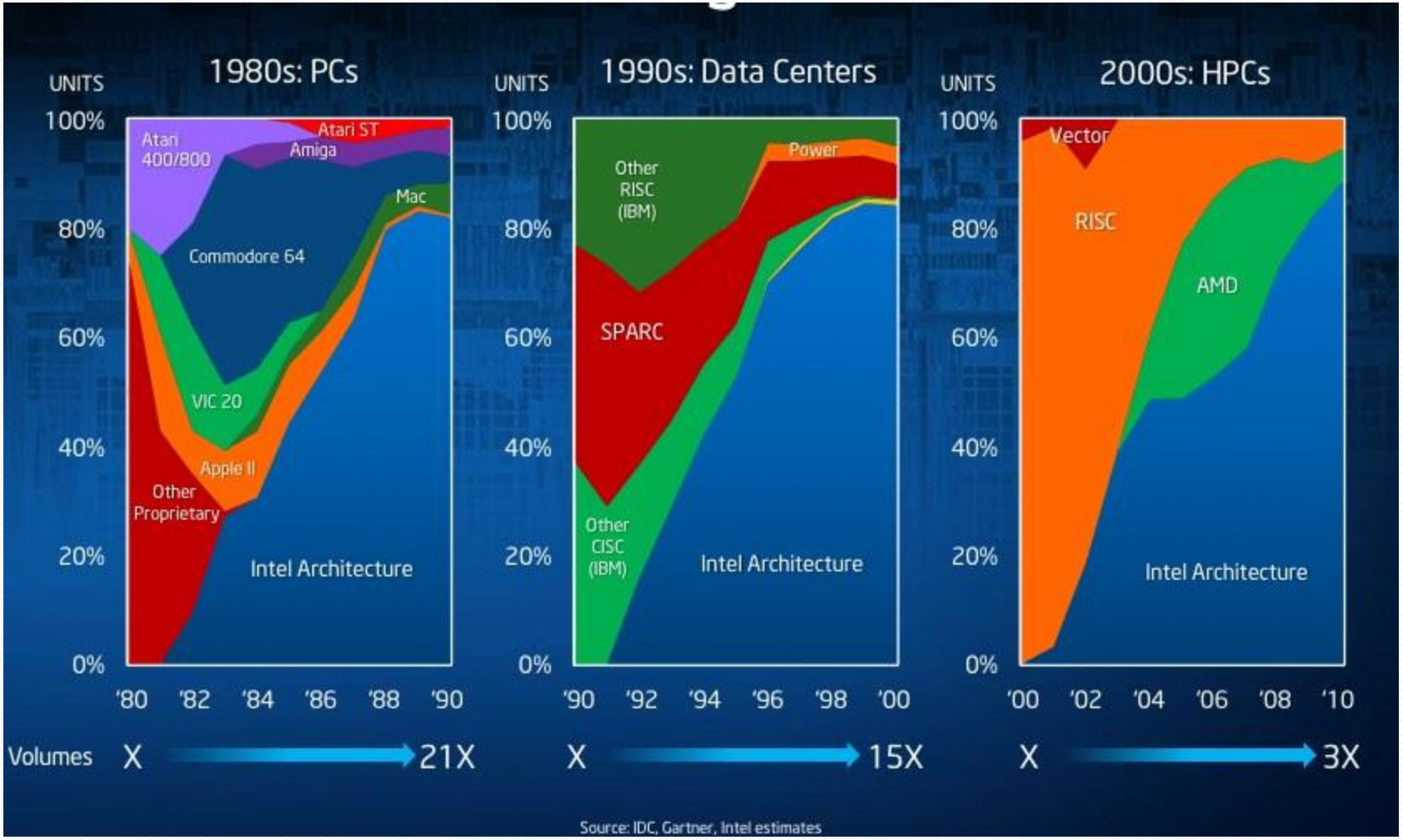
ARM Business Model




Smart Mobile Device Shipments
Volume in millions
2000
1500
1000
500
0
2010
2015
>$400
$200-
$350
<$150
Entry Level
Mid Range
Premium
Mixture of ARM and Gartner Estimates
Typical SOC
80-100mm2
50-80mm2
25-40mm2
Cortex-A15
Cortex-A7
Cortex-A57
Cortex-A53
Cortex-A12
Cortex-A7
Cortex-A53



Source: IHS iSuppli July 2011


1980s: PCs
UNITS
100%
80%
60%
40%
20%
0%
Atari 400/800
Atari ST
Amiga
Mac
Commodore 64
VIC 20
Apple II
Other Proprietary
Intel Architecture
'80
'82
'84
'86
'88
'90
Volumes
X
21X
1990s: Data Centers
UNITS
100%
80%
60%
40%
20%
0%
Other RISC (IBM)
Power
SPARC
Other CISC (IBM)
Intel Architecture
'90
'92
'94
'96
'98
'00
X
15X
2000s: HPCs
UNITS
100%
80%
60%
40%
20%
0%
Vector
RISC
AMD
Intel Architecture
'00
'02
'04
'06
'08
'10
X
3X
Source: IDC, Gartner, Intel estimates

Silvermont Highlights

Better Performance

- Out of Order Execution engine
- New multi-core and system fabric architecture
- New IA instructions extensions (Core™ Westmere level)
- New security and virtualization technologies

Better Power Efficiency

- Wider dynamic operating range
- Enhanced active and idle power management

Full Advantage of Intel® 22nm SoC Process Technology

- 3-D Tri-gate transistors tuned for SoC products
- Architecture and design co-optimized with the process

~3X the Performance Or ~5X Lower Power[1]

sed on the geometric mean of a variety of power and performance measurements across various benchmarks. Benchmarks included in this geomean are measurements on browsing benchmarks and workloads including SunSpider* and page Tests on Internet Explorer*, FireFox*, & Chrome*; Dhrystone*; EEMBC* workloads including CoreMark*; Android* workloads including CaffeineMark*, AnTuTu*, Linpack* and Quadrant* as well as measured estimates on SPECint* rate_base2000 EC1p* rate_base2000; on Silvermont preproduction systems compared to Atom processor 2250. Individual results will vary. SPEC* CPU2000* is a retired benchmark. * Other names and brands may be claimed as the property of others.

ware and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, ware, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the rmance of that product when combined with other products. For more information go to: http://www.intel.com/performance

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Jean-Baptiste
Contributor

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I cover technology innovation and investing from Silicon Valley.
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TECH 10/29/2013 @ 9:46PM | 42,712 views

Exclusive: Intel Opens Fabs To ARM Chips

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As the old adage goes, if you can't beat them, join them. Well, that's exactly what Intel INTC -0.41% finally decided to do relative to its lagging mobile business.

At the ARM developers conference today, Intel partner Altera ALTR +0.32% announced that the world's largest semiconductor company will fabricate its ARM 64-bit chips starting next year. The announcement sent shockwaves through the technology industry as Intel is desperately trying to break ARM's supremacy in the mobile market. Unlike Intel, ARM Holdings of the U.K. doesn't manufacture chips but its designs are licensed

Electronics Weekly.com

Intel to make multi-die 14nm finfet devices with Altera

no comment *richard wilson* *28th March 2014* *Get news by email*

Altera and Intel are working together on the development of multi-die devices which integrate 14nm Stratix 10 FPGAs with memory, processors and analogue components in a single package.

The heterogeneous multi-die devices incorporate 3D silicon technology and Intel's 14nm Tri-Gate (finfet) process technology.

Intel is already manufacturing Altera's Stratix 10 FPGAs and system-on-chip devices (SoCs) using the 14nm Tri-Gate process.

Intel and Altera are currently developing test vehicles aimed at streamlining manufacturing and integration flows.

"Our partnership with Altera to manufacture next-generation FPGAs and SoCs using our 14nm Tri-Gate process is going exceptionally well," said Sunit Rikhi, vice president and general manager, Intel Custom Foundry.

"Our close collaboration enables us to work together in many areas related to semiconductor manufacturing and packaging," said Rikhi.

Together, both companies are building off one another's expertise with the primary focus on building industry-disrupting products."

According to Brad Howe, senior vice president of R&D at Altera, access to Intel's manufacturing and chip packaging capabilities is allowing the FPGA supplier to offer system-in-a-package products which are "critical to meeting overall performance requirements."

Related news:

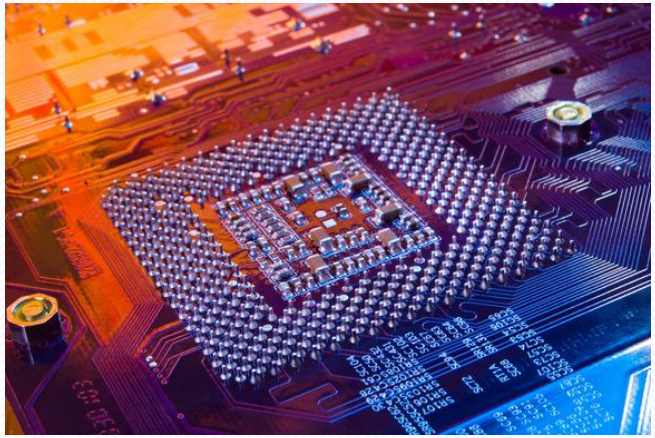
Altera: 14nm Stratix and 20nm Arria FPGA details

PROCESSORS microprocessors

Samsung teams with GlobalFoundries on 3D chips

Agam Shah
@agamsh

Apr 17, 2014 3:15 PM



Samsung is partnering with chip manufacturer GlobalFoundries to increase the supply of low-power, high-speed chips for smartphones and tablets.

GlobalFoundries has licensed Samsung's 14-nanometer FINFET chip making process, which is used to manufacture 3D transistors. Those transistors will allow GlobalFoundries to make chips that are 20 percent faster and use 35 percent less power than chips made using its current 20-nanometer technology, the companies said.

GlobalFoundries doesn't use the chips itself. It's a foundry supplier, which means it makes chips for other companies that outsource their chip production, such as Advanced Micro Devices, Nvidia and Qualcomm.

Chip makers are constantly racing to build faster, more power-efficient chips, and the deal with Samsung will help GlobalFoundries compete better with other foundry suppliers such as Taiwan's TSMC.

In fact, GlobalFoundries had been pursuing its own 14-nanometer technology, which it planned to introduce this year. It has now dropped that technology, apparently deciding that Samsung's FINFET process is a better option.

The big customers

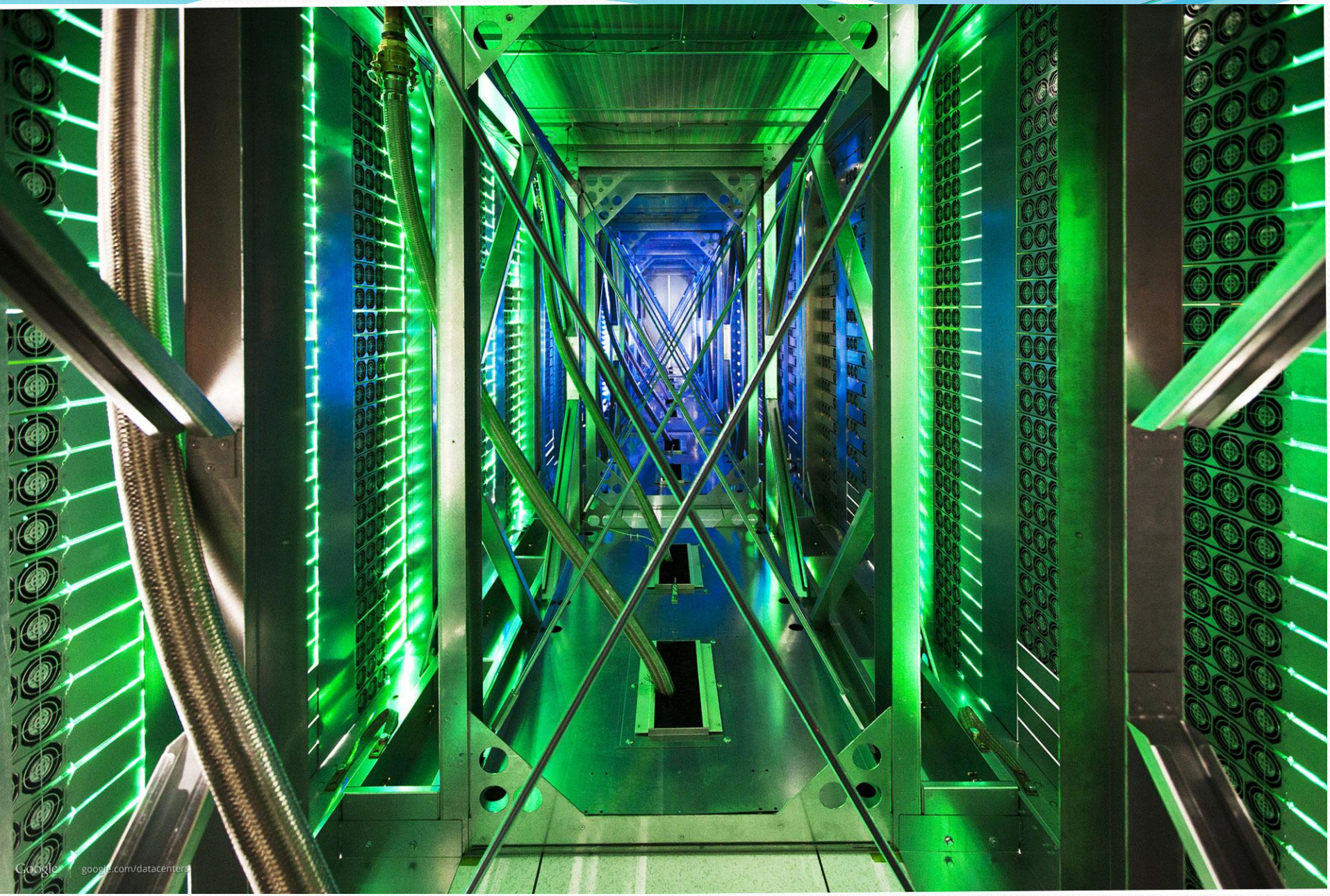
amazon

Google

YAHOO!

Microsoft

salesforce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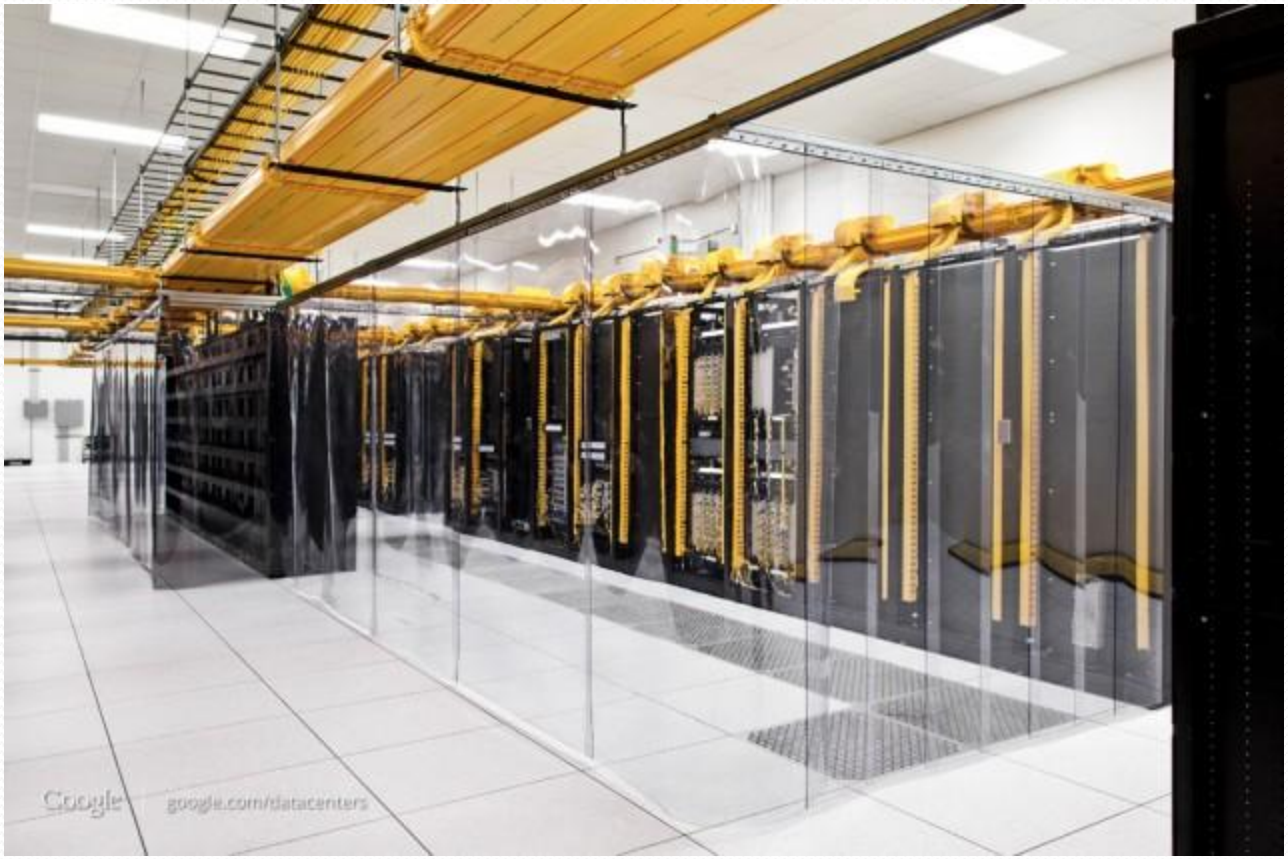
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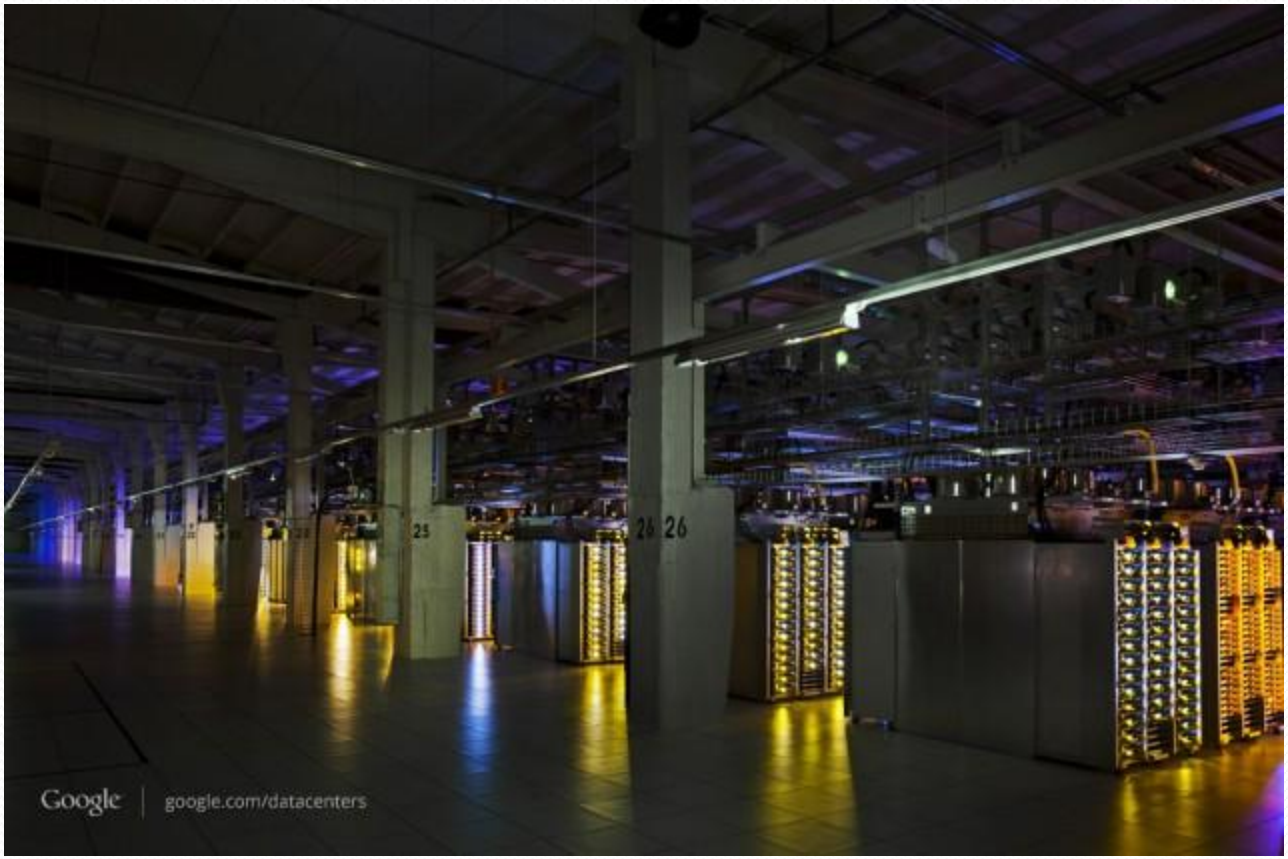
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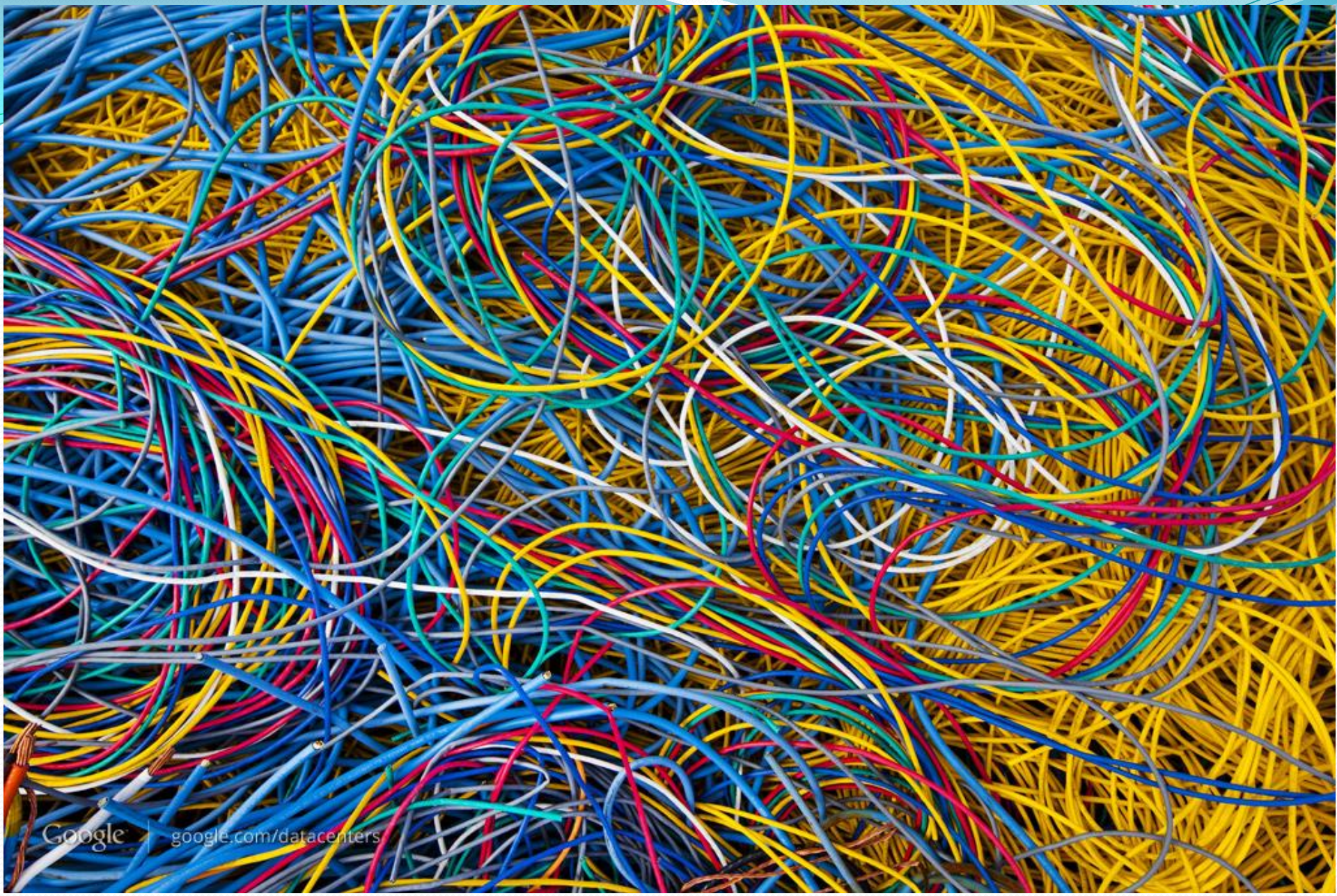
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The growth cycle