



## Statement of Volatility – Dell PowerEdge T630

Dell PowerEdge T630 contains both volatile and non-volatile (NV) components. Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility. Configuration option information (pertinent to options such as microprocessors, remote access controllers, and storage controllers) is available by component separately. The following NV components are present in the PowerEdge T630 server.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
<b>Planer</b>				
PCH Internal CMOS RAM	Non-Volatile	1	U_PCH	256 Bytes
BIOS Password	Non-Volatile	1	U_PCH	16 bytes
BIOS SPI Flash	Non-Volatile	1	U_SPI_BIOS1	8 MB
iDRAC SPI Flash	Non-Volatile	1	U_IDRAC_SPI1	4 MB
BMC EMMC	Non-Volatile	1	U_EMMC1	4 GB
CPU Vcore Regulators	Non-Volatile	2	PAU1, PDU1	512 Bytes
Vmem Regulators	Non-Volatile	2	PBU1, PCU1, PEU1, PFU1	512 Bytes

System CPLD RAM	Volatile	1	U_CPLD1	1 KB
System Memory	Volatile	Up to 12 per CPU	DIMM1 ~ DIMM24	Up to 64GB per DIMM
Internal USB Key	Non-Volatile	Up to 1	N/A	Varies (not factory installed)
Trusted Platform Module (TPM)	Non-Volatile	1	U_TPM1	128 Bytes
CPU	Volatile	1 or 2	CPU1 / CPU2	Various
iDRAC DDR	Volatile	1	U_IDRAC_MEM1	256MByte
iDRAC	Volatile	1	U_IDRAC1	64 kbyte + registers
LOM EEPROM	Non-Volatile	1	U1	8Mb
LOM FLASH	Non-Volatile	1	U3	512Kb
<b>16x2.5" EXP/Backplane (Upstream)</b>				
NVSRAM memory	Non-Volatile	1	U_EXP_NVSRAM	1 Mb
Flash memory	Non-Volatile	1	U_EXP_FLASH	32 Mb
Expander FRU image	Non-Volatile	1	U_EXP_FRU	512 Bytes
BP FRU image	Non-Volatile	1	U_BP_FRU	256 Bytes
<b>16x2.5" EXP/Backplane (Downstream)</b>				
NVSRAM memory	Non-Volatile	1	U_EXP_NVSRAM	1 Mb
Flash memory	Non-Volatile	1	U_EXP_FLASH	32 Mb
Expander FRU image	Non-Volatile	1	U_EXP_FRU	512 Bytes
BP FRU image	Non-Volatile	1	U_BP_FRU	256 Bytes
<b>8x3.5" Backplane</b>				
SEP internal flash	Non-Volatile	1	U_SEP	Flash:32KB+4KB EEPROM: 1KB
<b>18x3.5" Exp/Backplane</b>				
NVSRAM memory	Non-Volatile	1	U_EXP_NVSRAM	1 Mb
Flash memory	Non-Volatile	1	U_EXP_FLASH	32 Mb
BP FRU image	Non-Volatile	1	U_EXP_FRU	256 Bytes
Expander FRU image	Non-Volatile	1	U_BP_FRU	512 Bytes
<b>4x PCIe SSD Backplane</b>				
SEP internal flash	Non-Volatile	1	U_SEP	Flash:32KB+4KB EEPROM: 1KB
<b>H730, H830 PERCs</b>				
NVSRAM	Non-volatile	1	U1033	128KB
FRU	Non-volatile	1	U1019	256B
1-Wire EEPROM	Non-volatile	1	U1004	128B
SPD	Non-volatile	1	U22	256B

SBR	Non-volatile	1	U1020	8KB
Flash	Non-volatile	1	U1031	16MB
ONFI Backup Flash	Non-volatile	1	U1059	4GB
SDRAM	Volatile	5	U1043-U1047	512MB/1GB
<b>H330 PERC</b>				
NVSRAM	Non-volatile	1	U1033	128KB
FRU	Non-volatile	1	U1019	256B
1-Wire EEPROM	Non-volatile	1	U1004	128B
SBR	Non-volatile	1	U1020	8KB
Flash	Non-volatile	1	U3	16MB
<b>PCIe SSD Extension Card</b>				
Switch Configuration EEPROM	Non-Volatile	1	U2	256B
<b>IDSDM</b>				
SPI Flash	Non-Volatile	1	U2	8Mb
MCU	Non-Volatile	1	U6	512KB
<b>Front Panel</b>				
SPI Flash	Non-Volatile	1	U_SPI_FLASH	32Mb
<b>Power Supplies</b>				
PSU FW	Non-Volatile	1 per PSU	Varies by PSU Part Number	Up to 2MB which varies by part number

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
<b>Planer</b>			
PCH Internal CMOS RAM	Battery-backed CMOS RAM	No	Real-time clock and BIOS configuration settings
BIOS Password	Battery-backed CMOS RAM	Yes	Password to change BIOS settings
BIOS SPI Flash	SPI Flash	No	Boot code, system configuration information, UEFI environment, Flash descriptor, ME
iDRAC SPI Flash	SPI Flash	No	iDRAC Uboot (bootloader), server management persistent store (i.e. iDRAC MAC Address, iDRAC boot variables), lifecycle log cache, virtual planar FRU and EPPID, rac log, system event log, JobStore, iDRAC Secure boot code,
BMC EMMC	eMMC NAND Flash	No	Operational iDRAC FW, Lifecycle Controller (LC) USC partition, LC service diags, LC OS drivers, USC firmware
CPU Vcore Regulators	ROM	No	Operational parameters
Vmem Regulators	ROM	No	Operational parameters
System CPLD RAM	RAM	No	Not utilized
System Memory	DRAM	Yes	System OS RAM
Internal USB Key	Flash	Yes	General purpose USB key drive
Trusted Platform Module (TPM)	EEPROM	Yes	Storage of encryption keys
CPU	Cache + registers	Yes	Processor cache + registers
iDRAC DDR	DRAM	No	iDRAC local memory
iDRAC	Cache + registers	No	Processor cache + registers
LOM EEPROM	EEPROM	Yes	Onboard LOM FW
LOM FLASH	Flash	Yes	Onboard LOM FW

<b>16x2.5" EXP/Backplane (Upstream)</b>			
NVSRAM memory	Flash	No	FW config data
Flash memory	Flash	No	Firmware
Expander FRU image	I2C EEPROM	No	FRU
BP FRU image	I2C EEPROM	No	FRU
<b>16x2.5" EXP/Backplane (Downstream)</b>			
NVSRAM memory	Flash	No	FW config data
Flash memory	Flash	No	Firmware
Expander FRU image	I2C EEPROM	No	FRU
BP FRU image	I2C EEPROM	No	FRU
<b>8x3.5" Backplane</b>			
SEP internal flash	Integrated Flash+EEPROM	No	Firmware + FRU
<b>18x3.5" Exp/Backplane</b>			
NVSRAM memory	Flash	No	FW config data
Flash memory	Flash	No	Firmware
BP FRU image	I2C EEPROM	No	FRU
Expander FRU image	I2C EEPROM	No	FRU
<b>4x PCIe SSD Backplane</b>			
SEP internal flash	Integrated Flash+EEPROM	No	Firmware + FRU
<b>H730, H830 PERCs</b>			
NVSRAM	NVSRAM	No	Configuration data
FRU	FRU	No	Card manufacturing information
1-Wire EEPROM	1-Wire EEPROM	No	Holds default controller properties/settings
SPD	SPD	No	Memory configuration data
SBR	SBR	No	Bootloader
Flash	Flash	No	Card firmware
ONFI Backup Flash	ONFI Backup Flash	No	Holds cache data during power loss
SDRAM	SDRAM	No	Cache for HDD I/O

<b>H330 PERC</b>			
NVSRAM	NVSRAM	No	Configuration data
FRU	FRU	No	Card manufacturing information
1-Wire EEPROM	1-Wire EEPROM	No	Holds default controller properties/settings
SBR	SBR	No	Bootloader
Flash	Flash	No	Card firmware
<b>PCIe SSD Extension Card</b>			
Switch Configuration EEPROM	SPI Flash EEPROM	No (requires specialized SW)	Configuration for PLX PCIe switch, setting registers
<b>IDSDM</b>			
SPI Flash	SPI Flash	No	Exclusively used by the controller
MCU	Embedded Flash	FW can be updated via iDRAC which runs on Linux	Firmware
<b>Front Panel</b>			
SPI Flash	SPI Flash	No	For field maintenance. Have License, Service Tag and system information.
<b>Power Supplies</b>			
PSU FW	Embedded microcontroller flash	No	Power Supply operation, power management data and fault behaviors

<b>Item</b>	<b>How is data input to this memory?</b>	<b>How is this memory write protected?</b>	<b>How is the memory cleared?</b>
<b>Planer</b>			
PCH Internal CMOS RAM	BIOS	N/A – BIOS only control	1) Set NVRAM_CLR jumper to clear BIOS configuration settings at boot and reboot system; 2) AC power off system, remove coin cell battery for 30 seconds, replace battery and power back on; 3) restore default configuration in F2 system setup menu.
BIOS Password	Keyboard	N/A	Place shunt on J_PSWD_NVSRAM jumper

			pins 2 and 4.
BIOS SPI Flash	SPI interface via iDRAC	Software write protected	Not possible with any utilities or applications and system is not functional if corrupted/removed.
iDRAC SPI Flash	SPI interface via iDRAC	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.	Not completely user clearable; however, user data, lifecycle log and archive, SEL, fw image repository can be cleared via Delete Configuration and Retire System, accessible in Lifecycle Controller interface
BMC EMMC	NAND Flash interface via iDRAC	Embedded FW write protected	Not completely user clearable; however, user data, lifecycle log and archive, SEL, fw image repository can be cleared via Delete Configuration and Retire System, accessible in Lifecycle Controller interface
CPU Vcore Regulators		NA	Not user clearable
Vmem Regulators		NA	Not user clearable
System CPLD RAM	Not utilized	Not accessible	Not accessible
System Memory	System OS	OS Control	Reboot or power down system
Internal USB Key	USB interface via PCH. Accessed via system OS	No write protect	Can be cleared in system OS
Trusted Platform Module (TPM)	Using TPM Enabled operating systems	SW write protected	F2 Setup option
CPU	Various	Various	Power off
iDRAC DDR	iDRAC Firmware	NA	Power off
iDRAC	iDRAC Firmware	NA	Power off
LOM EEPROM		NA	Not user clearable
LOM FLASH		NA	Not user clearable
<b>16x2.5" EXP/Backplane (Upstream)</b>			
NVSRAM memory	Common Flash memory Interface (CFI)	Hardware strapping	Not user clearable
Flash memory	Common Flash memory Interface (CFI)	Hardware strapping	Not user clearable
Expander FRU image	I2C interface via iDRAC	Hardware strapping	Not user clearable
BP FRU image	I2C interface via iDRAC	Hardware strapping	Not user clearable
<b>16x2.5" EXP/Backplane (Downstream)</b>			
NVSRAM memory	Common Flash memory	Hardware strapping	Not user clearable

	Interface (CFI)		
Flash memory	Common Flash memory Interface (CFI)	Hardware strapping	Not user clearable
Expander FRU image	I2C interface via iDRAC	Hardware strapping	Not user clearable
BP FRU image	I2C interface via iDRAC	Hardware strapping	Not user clearable
<b>8x3.5" Backplane</b>			
SEP internal flash	I2C interface via iDRAC	Program write protect bit	Not user clearable
<b>18x3.5" Exp/Backplane</b>			
NVSRAM memory	Common Flash memory Interface (CFI)	Hardware strapping	Not user clearable
Flash memory	Common Flash memory Interface (CFI)	Hardware strapping	Not user clearable
BP FRU image	I2C interface via iDRAC	Hardware strapping	Not user clearable
Expander FRU image	I2C interface via iDRAC	Hardware strapping	Not user clearable
<b>4x PCIe SSD Backplane</b>			
SEP internal flash	I2C interface via iDRAC	Program write protect bit	Not user clearable
<b>H730, H830 PERCs</b>			
NVSRAM	ROC writes configuration data to NVSRAM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
FRU	Programmed at ICT during production.	Not WP	Cannot be cleared with existing tools available to the customer
1-Wire EEPROM	ROC writes data to this memory	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SPD	Pre-programmed before assembly	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SBR	Pre-programmed before assembly	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
Flash	Pre-programmed before assembly. Can be updated using Dell/LSI tools	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
ONFI Backup Flash	FPGA backs up DDR data to this device in case of a power failure	Not WP. Not visible to Host Processor	Flash can be cleared by powering up the card and allowing the controller to flush the contents to VD's. If the VD's are no longer available, cache can be cleared by going into controller bios and selecting Discard Preserved Cache.
SDRAM	ROC writes to this memory - using it as cache for data IO to HDDs	Not WP. Not visible to Host Processor	Cache can be cleared by powering off the card



<b>H330 PERC</b>			
NVSRAM	ROC writes configuration data to NVSRAM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
FRU	Programmed at ICT during production	Not WP	Cannot be cleared with existing tools available to the customer
1-Wire EEPROM	ROC writes data to this memory	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SBR	Pre-programmed before assembly	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
Flash	Pre-programmed before assembly. Can be updated using Dell/LSI tools	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
<b>PCIe SSD Extension Card</b>			
Switch Configuration EEPROM	The EEPROM image is pre-loaded at factory before assembly. Once assembled on the card, data can be entered via PLX Device Editor or PLX EEP DOS based tool.	Device can be write protected via hardware pin. Alternatively, device contents can be write protected via WPEN bit in status register.	System is not functional as intended if corrupted/removed.
<b>IDSDM</b>			
SPI Flash	SPI interface via iDRAC	Hardware strapping	Not user clearable
MCU	USB3.0 interface via PCH	N/A	Not user clearable
<b>Front Panel</b>			
SPI Flash	SPI interface via iDRAC	Hardware strapping	Not user clearable
<b>Power Supplies</b>			
PSU FW	Different vendors have different utilities and tools to load the data to memory. It can also be loaded by Dell Update Package from LC or OS (Windows and Linux)	Protected by the embedded microcontroller. Special keys are used by special vendor provided utilities to unlock the ROM with various CRC checks during load.	Not user clearable



**NOTE:** For any information that you may need, direct your questions to your Dell Marketing contact.