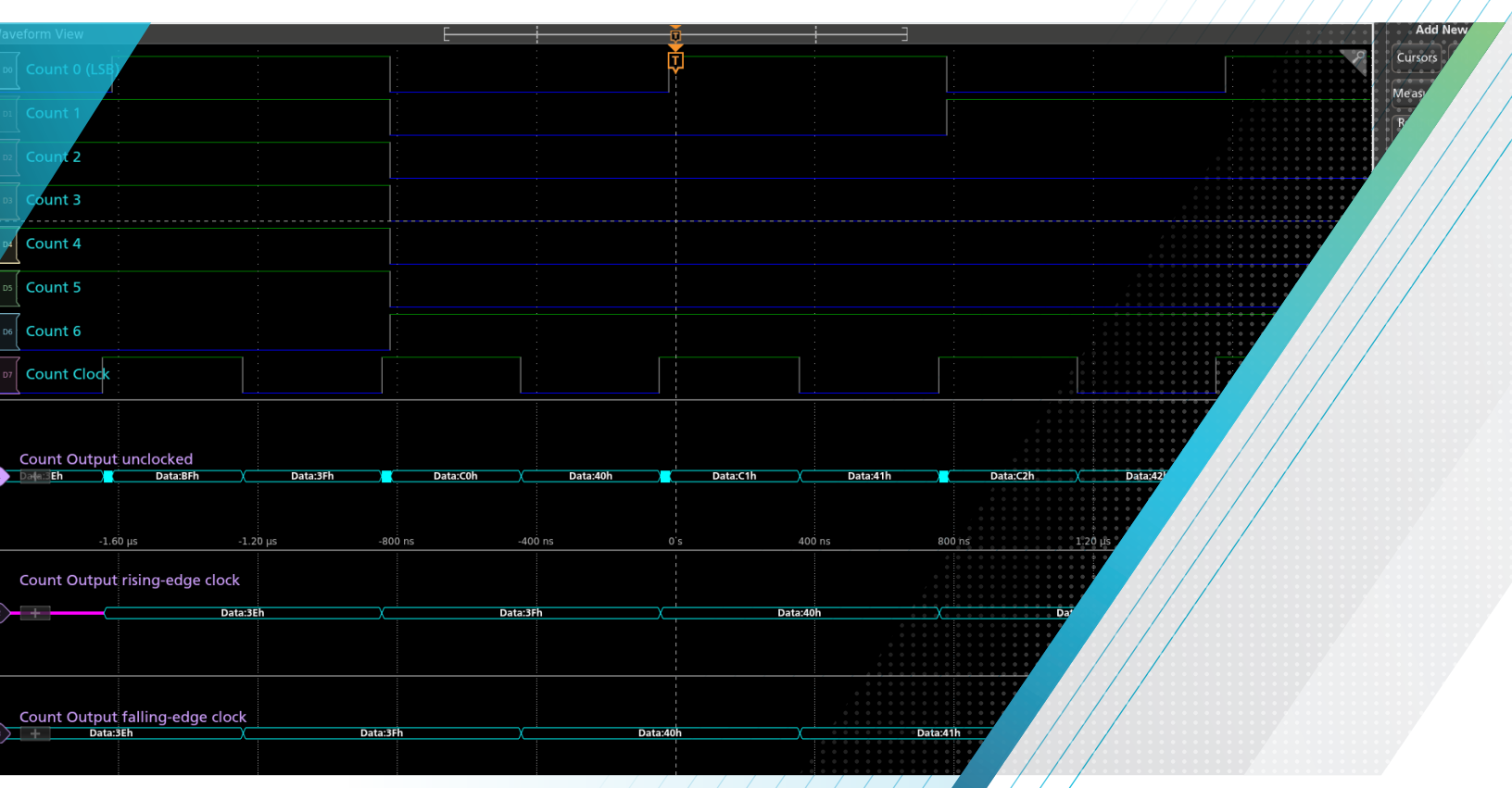
Identifying Setup and Hold Violations with a Mixed Signal Oscilloscope

APPLICATION NOTE



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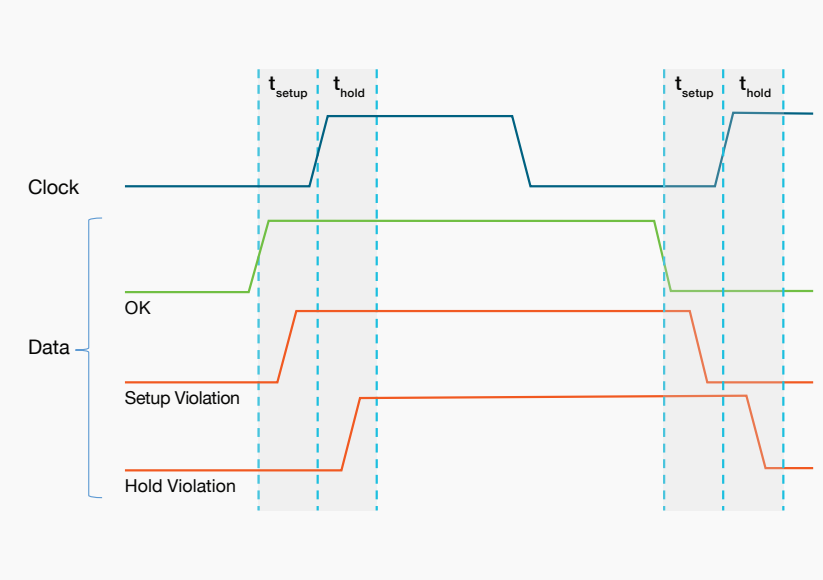
Introduction

Timing relationships between signals are critical to reliable operation of digital designs. With synchronous designs, the timing of the clock signal relative to data signals is especially important.

Using a mixed signal oscilloscope, the timing relationships between multiple logic inputs and a clock signal can easily be determined. Setup & Hold triggering automates this clock-to-data timing determination.



Setup Time is the time the input data signals are stable (either high or low) before the active clock edge occurs. Hold Time is the time the input data signals are stable (either high or low) after the active clock edge occurs. Setup and Hold Times are specified in component data sheets for synchronous devices (such as flip-flops) and must be met to assure that the component will behave correctly and reliably.

Based on their ability to capture both analog and digital representations of signals and display them in a time-correlated format, mixed signal oscilloscopes (MSOs) are ideal for verifying the signal integrity of the digital signals and debugging digital circuits. The Tektronix 5 Series MSO and MSO2000 and MSO5000 Series of mixed signal oscilloscopes combine the performance of a Tektronix oscilloscope with the basic functions of a logic analyzer. The Tektronix MDO3000 and MDO4000 Series mixed domain oscilloscopes also offer 16-channel logic analyzer capabilities. Throughout this application note, any features or capabilities referred to in MSOs are also available in MDO products. For information on the features in each series, please see Appendix A or visit www.tektronix.com.

THIS APPLICATION NOTE

- Explains the basic setup of a mixed signal oscilloscope (MSO)
- Tells how to interpret the logic signal display on a Tektronix MSO
- Explains how to easily identify and measure setup and hold violations in digital designs using an MSO

MSO Setup

UNDERSTANDING DIGITAL TIMING RESOLUTION (DIGITAL SAMPLE RATE)

An important MSO acquisition specification is the timing resolution used for capturing digital signals. The sample rate varies between MSO models. It is important to understand your timing measurement resolution, especially when making judgments on setup and hold times.

		DIGITAL TIMING RESOLUTION	RECORD LENGTH
5 Series MSO		160 ps	62.5 Mpoints, 125 Mpoints opt.
MSO5000 Series	Main acquisition	2 ns	25 Mpoints, up to 250 Mpoints opt.
	MagniVu acquisition	60.6 ps	10,000 points
MDO4000 Series	Main acquisition	2 ns	20 Mpoints
	MagniVu acquisition	60.6 ps	10,000 points
MDO3000 Series	Main acquisition	2 ns	10 Mpoints
	MagniVu acquisition	121.2 ps	10,000 points
MSO2000 Series		1 ns (2 ns when two probes are used)	1 Mpoints

Several Tektronix series offer MagniVu™ high speed acquisition. MagniVu acquisition provides high timing resolution with up to a 10,000 point record length centered on the trigger.

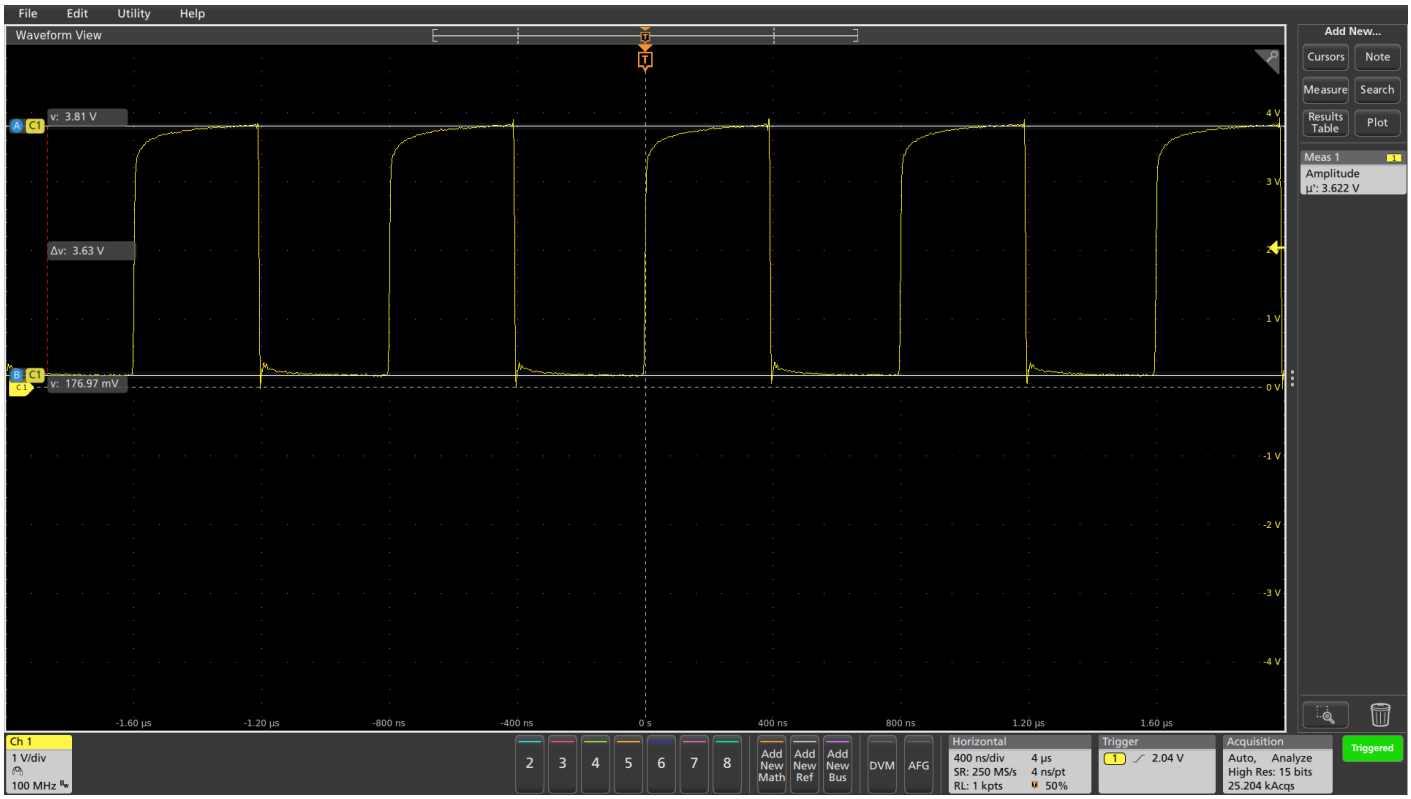


FIGURE 1. Quick verification of the logic signal amplitude using automated measurements.

SETTING DIGITAL THRESHOLDS

A mixed signal oscilloscope's digital channels view a digital signal as either a logic high or logic low, just like a digital circuit views the signal. This means as long as ringing, overshoot and ground bounce do not cause logic transitions, these analog characteristics are not of concern to the MSO. Just like a logic analyzer, an MSO uses a user-specified threshold voltage to determine if the signal is logic high or logic low.

The MSO's analog channel can be used to quickly check the logic swing of your digital signal. In Figure 1, the oscilloscope automatically measures the digital signal amplitude as about 3.6 V. For logic families with symmetrical voltage swings like CMOS, the threshold is at half of the signal amplitude. However, for logic families with asymmetrical voltage swings like TTL (Transistor-Transistor Logic), you typically need to consult the component data sheet and define the threshold as half-way (TTL $V_{threshold}$ = 1.4V) between the logic device's maximum low-level input voltage (TTL V_{IL} = 0.8V) and minimum high-level input voltage (TTL V_{IH} = 2.0V) values.

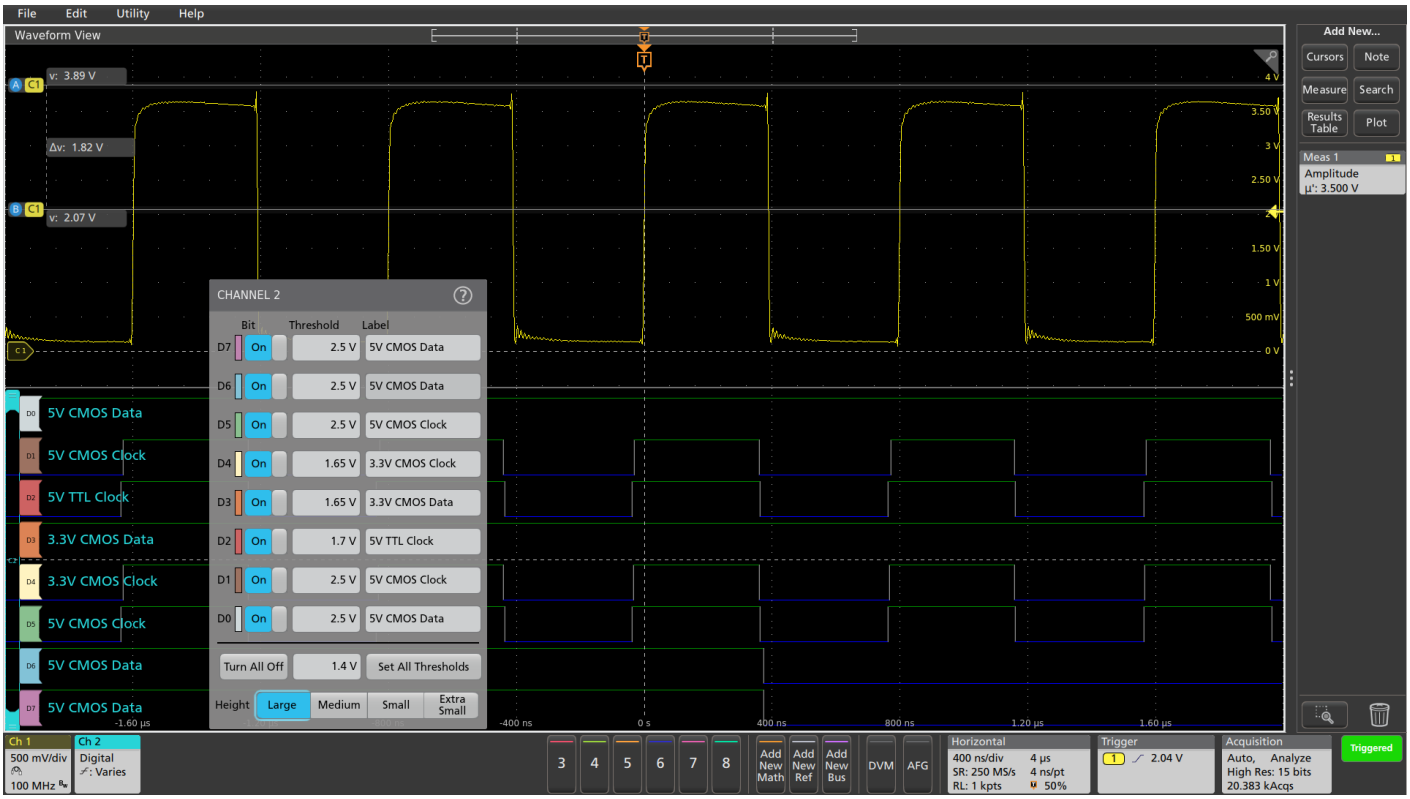


FIGURE 2. Mixed logic families (TTL & CMOS) threshold settings on the same TLP058 digital logic probe pod.

Most Tektronix MSOs provide per-channel threshold settings that are useful in debugging circuits with mixed logic families. Figure 2 shows the 5 Series MSO measuring multiple logic signals with an 8-channel TLP058 probe. The TTL signal threshold is set to 1.7 V, the 3.3 V CMOS signal thresholds are set to 1.65V, and the 5 V CMOS signal thresholds are set to 2.5 V, enabling reliable acquisition of the various logic signals at the same time.

For the MSO2000 and MDO3000 Series, the thresholds are adjusted per probe pod (a grouping of 8 channels) and therefore, the TTL signals would be on one pod while the LVPECL signals would be on the second pod.

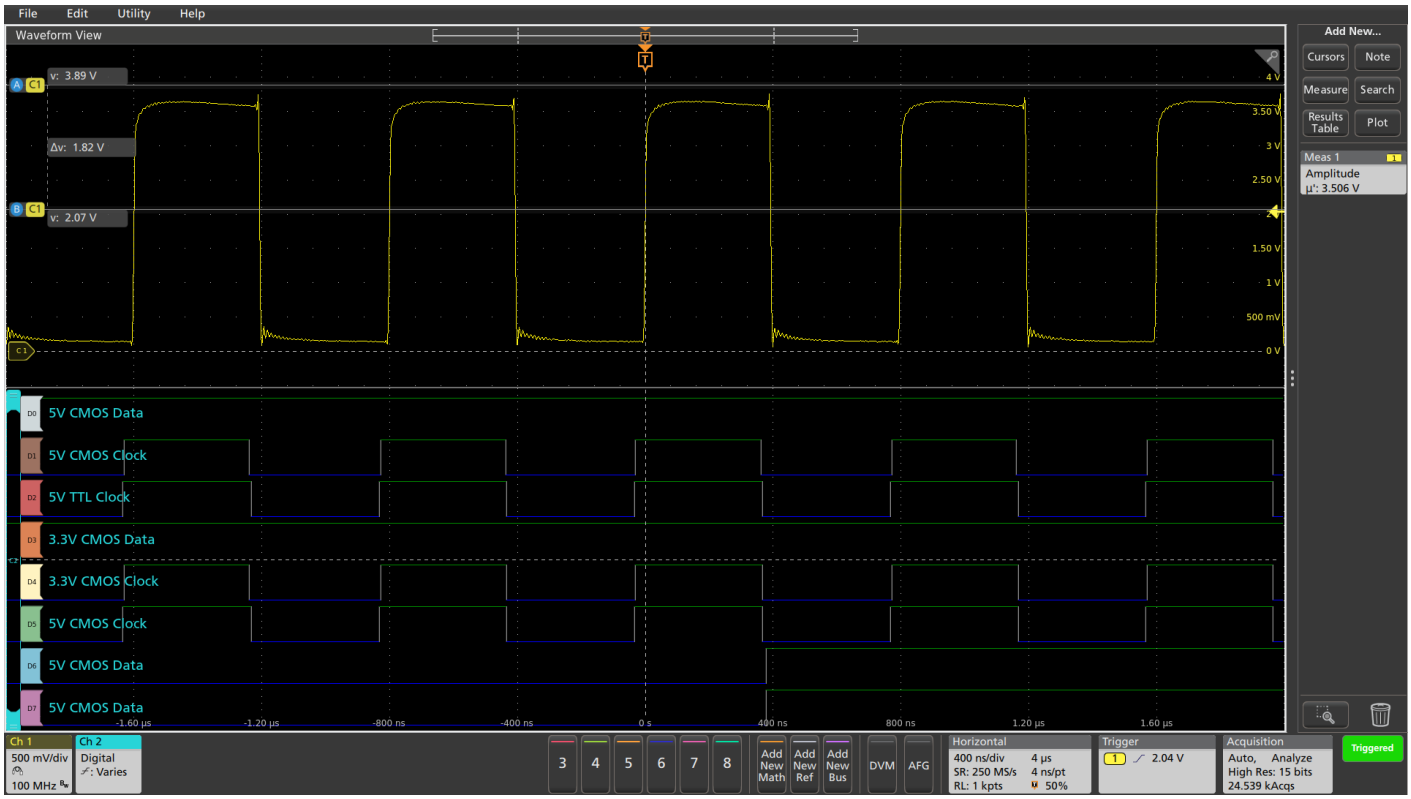


FIGURE 3. Probe color coding matches waveform color coding, making it easier to see which signals corresponds to which test point.

INTERPRETING THE COLOR–CODED DIGITAL WAVEFORM DISPLAY

Digital timing waveforms look very similar to analog waveforms except only logic highs and lows are shown. To make analysis easier, Tektronix MDO/MSO oscilloscopes show logic lows as blue and logic highs as green on the digital waveforms, allowing you to see the logic value even if a transition is not visible. The waveform label color also matches the probe color-coding to make it easier to see which signal corresponds to which test point, as shown in Figure 3.

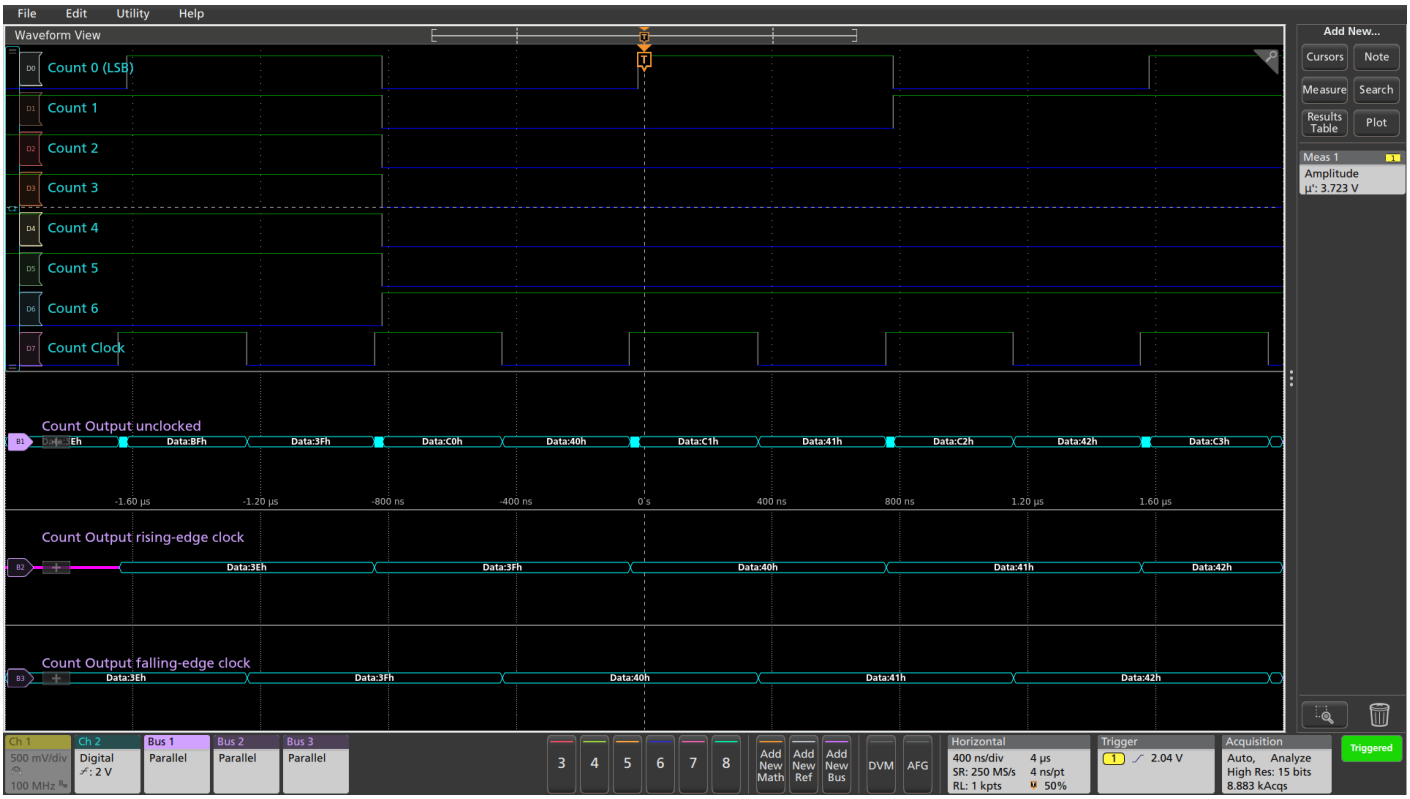


FIGURE 4. Example of a timing acquisition on the MDO/MSO Series. Three parallel buses have been defined and decoded using the device's clock signal.

The digital timing waveforms can be grouped to create a bus. One digital signal is defined as the least significant bit and the other digital signals represent the other bits of the binary value up to the most significant bit. The oscilloscope will then decode the bus into a binary or hex value.

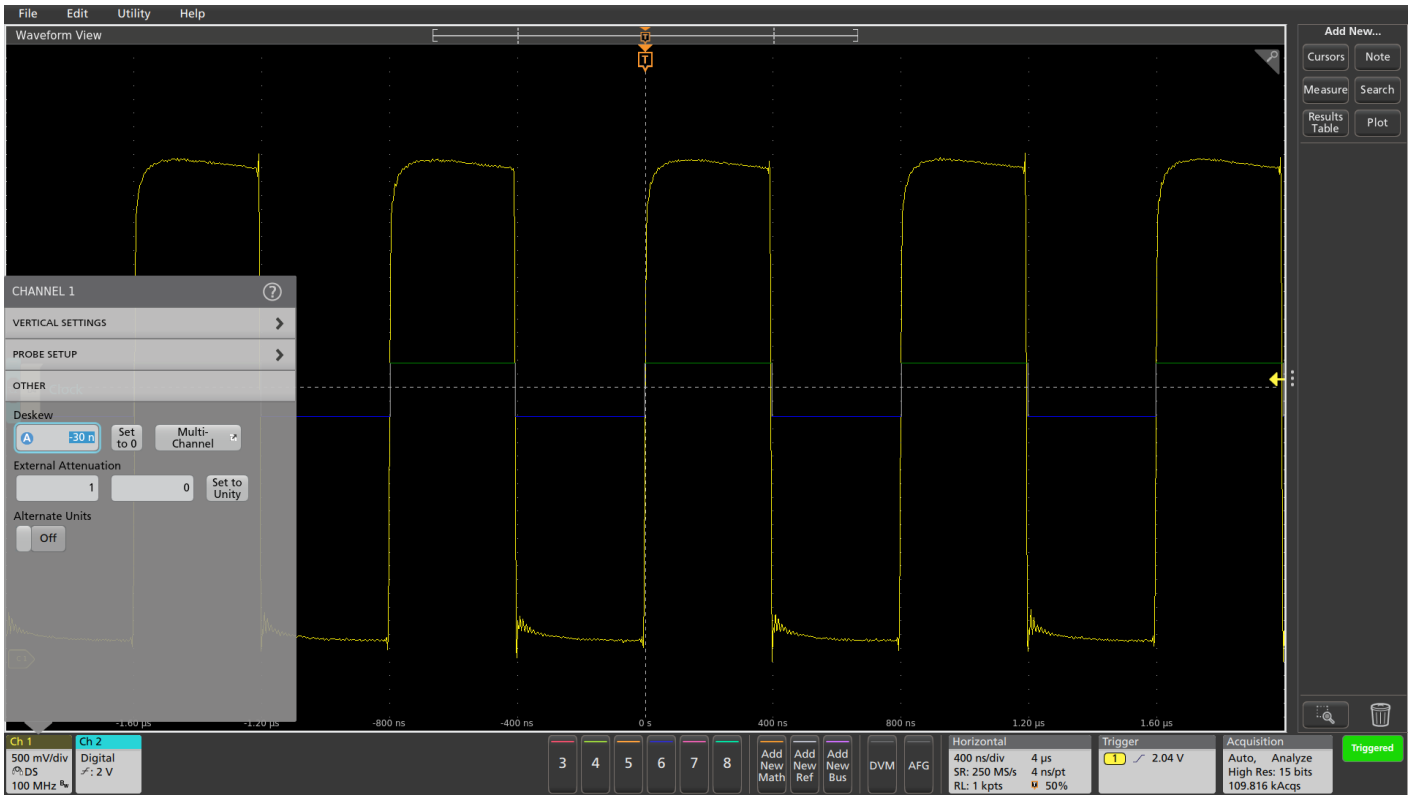


FIGURE 5. Analog channel time aligned with the digital channel.

REMOVING TIMING SKEW BETWEEN CHANNELS

Every Tektronix MDO/MSO Series oscilloscope has a compatible logic probe. To simplify digital measurements, the oscilloscope compensates for the propagation delay of the logic probe. Therefore, there are no digital channel probe deskew adjustments.

However, for better time-correlation measurements between the analog and digital waveforms, it's important to remove the analog to digital time skew. In the example shown in Figure 5, to align the analog channels with the digital channels, the 2 V (50% amplitude) position on the analog waveform is time-aligned with the digital signal transitions which occur at the 2 V threshold. The deskew value is manually adjusted to align the analog channel to the digital channel. This deskew process needs to be repeated for any other analog channels.

Analog channel skews should be checked when the analog probes are changed and the digital thresholds should be checked when measuring a different logic family. With the threshold and skews configured, the oscilloscope is ready for verifying and debugging digital circuits.

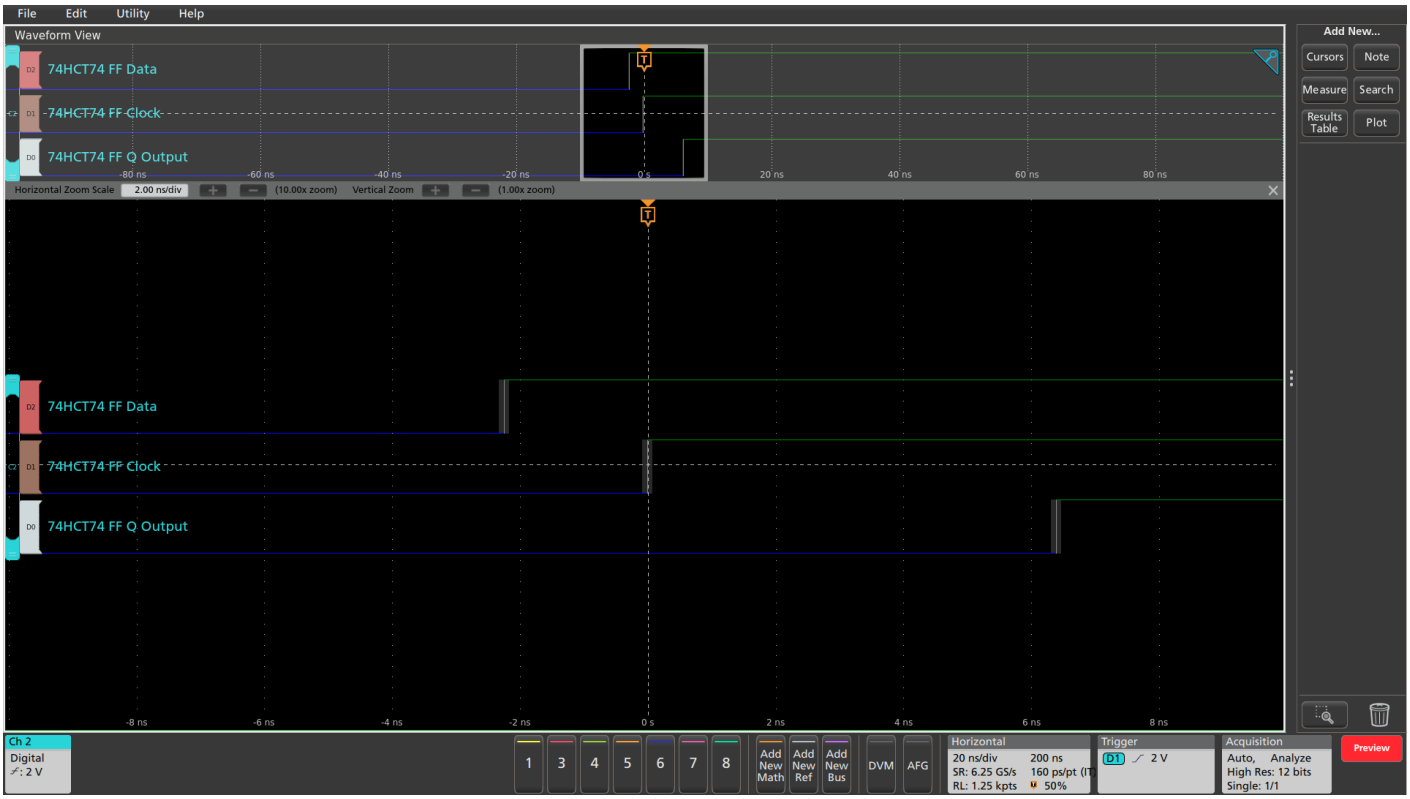


FIGURE 7. This 74HCT74 flip-flop appears to be working as expected.

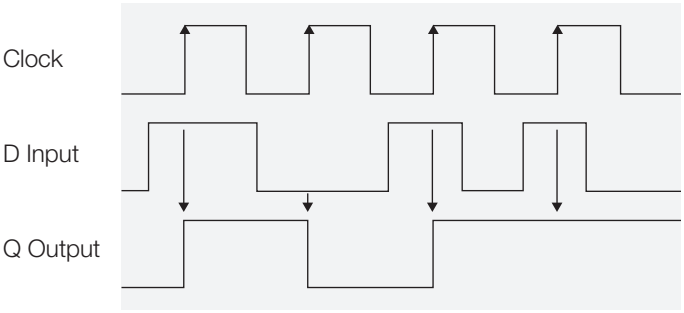


FIGURE 6. Example of flip-flop behavior.

FLIP–FLOP TIMING MEASUREMENTS

The simplest synchronous logic device is a flip-flop. The logic state of the D Input appears at the Q Output only after the rising clock edge (after the D-Flip-Flop propagation delay). An MSO is an ideal tool to verify the operation of a flip-flop and debug digital circuits.

At first glance, as shown in Figure 7, the flip-flop looks like it is working as expected. The data signal has been stable for several nanoseconds before the rising edge of the clock, and the data remains stable for many nanoseconds after the clock edge. The propagation from clock edge to the Q output is about 6 ns.

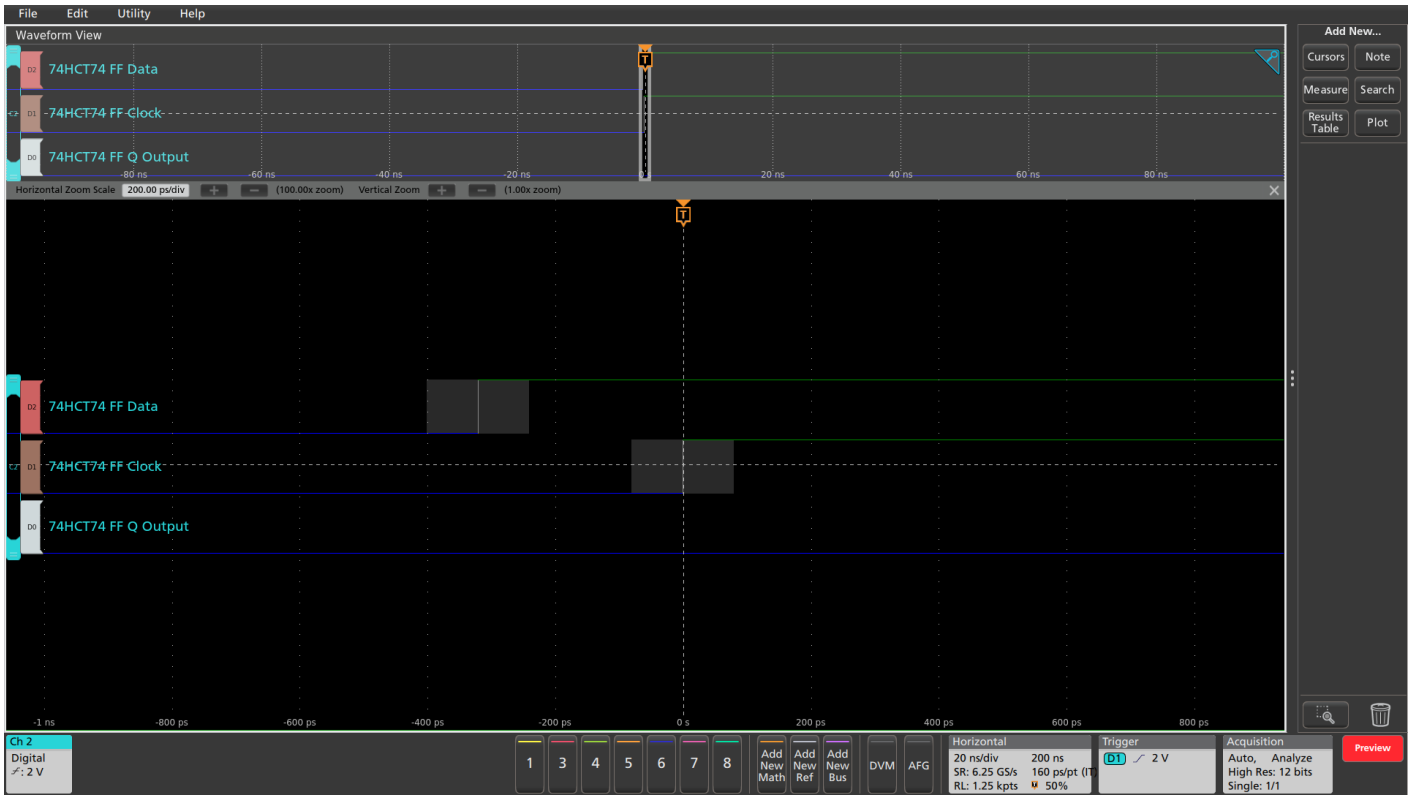


FIGURE 8. Setup time violation on a 74HCT74 flip-flop results in no change in Q output.

But Figure 8 shows an instance where the data signal is transitioning just 300 ps before the clock edge, well below the 15 ns setup time specification – a setup time violation. Notice that the Q output does not change state as expected.

Notice the gray regions around the signal transitions in Figure 8. The MSO displays these regions to indicate the timing uncertainty related to the digital sample rate.

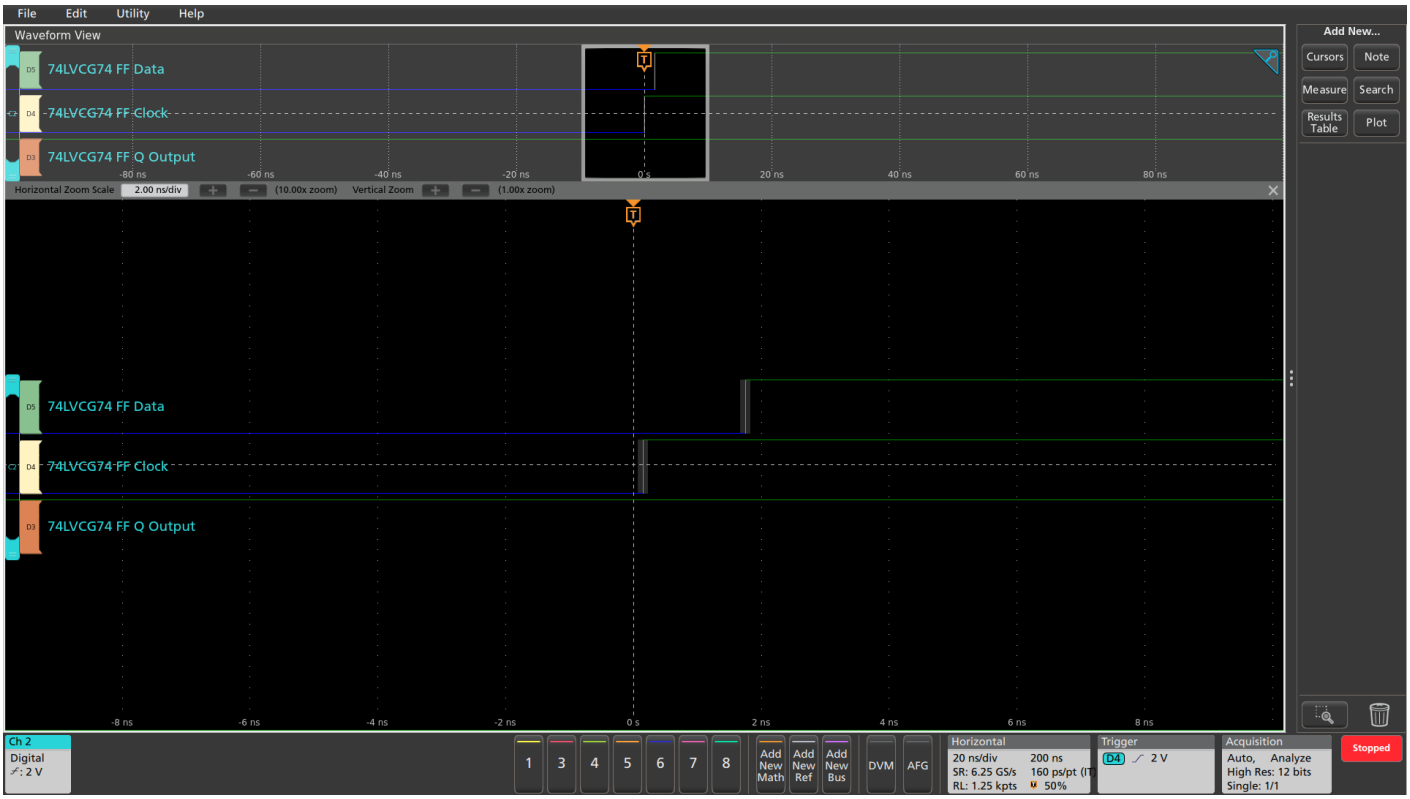


FIGURE 9. Hold time violation on a 74HCT74 flip-flop results in no change in Q output.

Figure 9 shows an instance where the data signal is transitioning about 300 ps after the clock edge. This is well below the 3 ns hold time specification – a hold time violation. Again, notice that the Q output does not change state as expected.

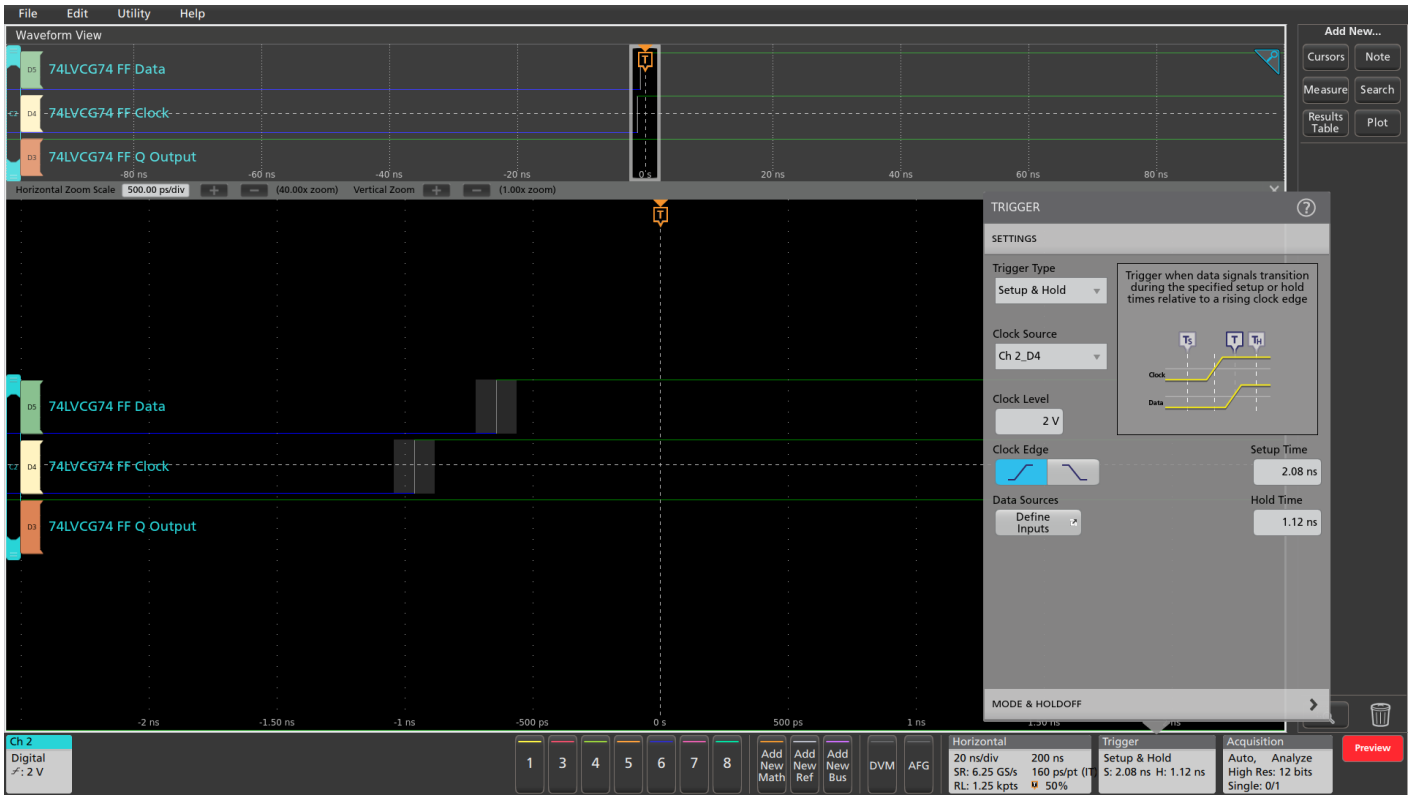


FIGURE 10. Automatic Setup and Hold violation triggering on a 74LVCG74 flip-flop captures many errors.

Capturing Setup and Hold Violations

MSOs have a specialized trigger mode designed to automatically capture every setup and/or hold violation. The setup and hold trigger measures the timing relationship between the clock and data signal (or, with some MSOs, data signals) and captures signals when the setup time or hold time is below the specification. This capability simplifies debug, but also can be used for unattended monitoring of a design.

After consulting the 74LVCG74 component data sheet, the setup and hold trigger parameters (2 ns and 1 ns, respectively) are set to capture any violations, as shown in Figure 10. The MSO automatically triggers on the first input condition that violates the specified parameters.

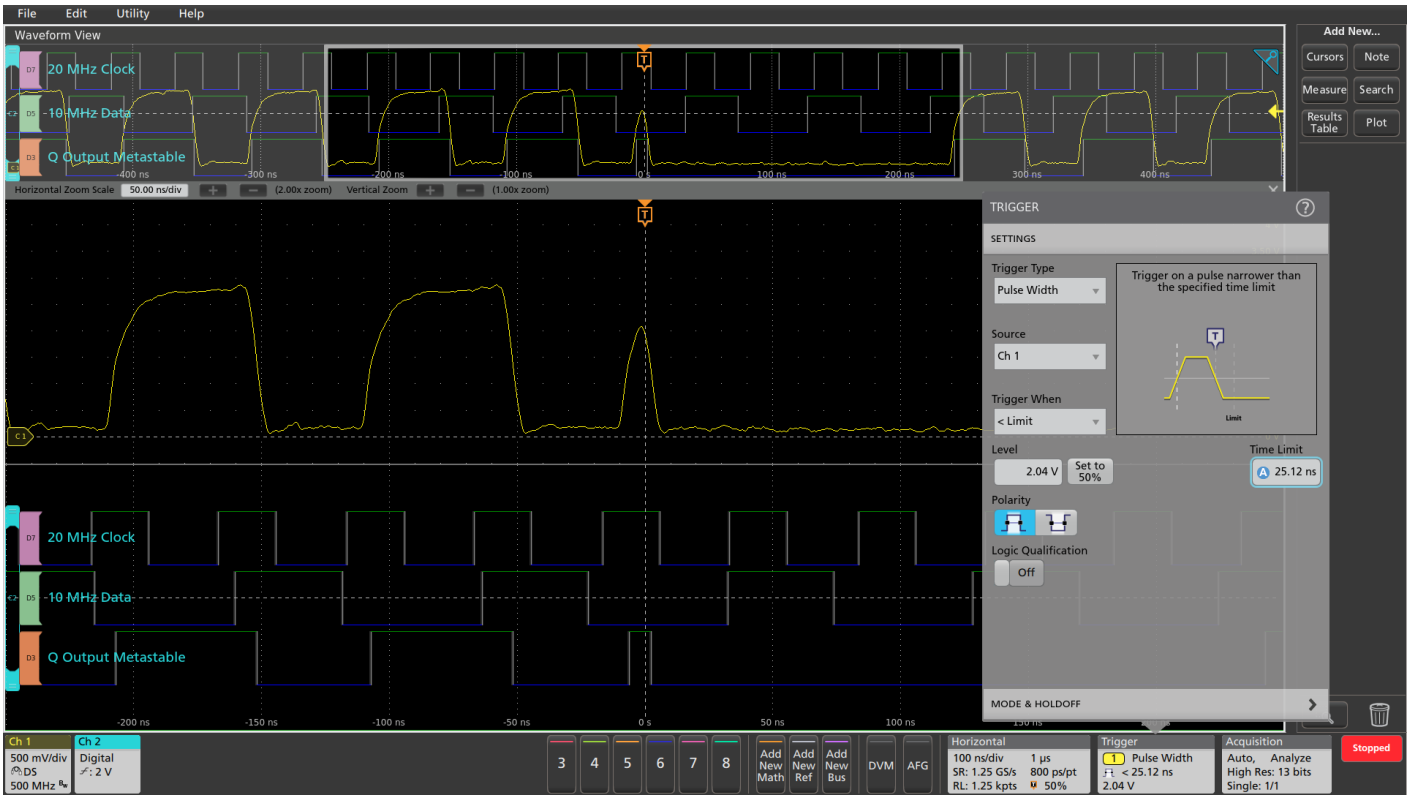


FIGURE 11. Pulse Width triggering captures a narrow glitch on the output of a 74LS74 flip-flop.

In the previous example, setup and hold triggers were used on the inputs to the flip-flop. Another approach is to trigger on signal errors on the output of the device, and capture the input signals for analysis.

In the next example, an older design based on the 74LS74 low-power Schottky TTL technology, is exhibiting intermittent errors. The minimum output voltage for a high is 2.4 V, so all high output signals should be at least that high. The design is based on a 20 MHz clock (50 ns period), so all output pulses should be at least that wide.

Armed with these facts, the oscilloscope can quickly determine if the output signal is behaving as expected, and capture the inputs and outputs if it is not. Figure 11 shows a pulse width trigger finding a glitch, a signal where the pulse width is less than half of the minimum expected pulse width for this design.

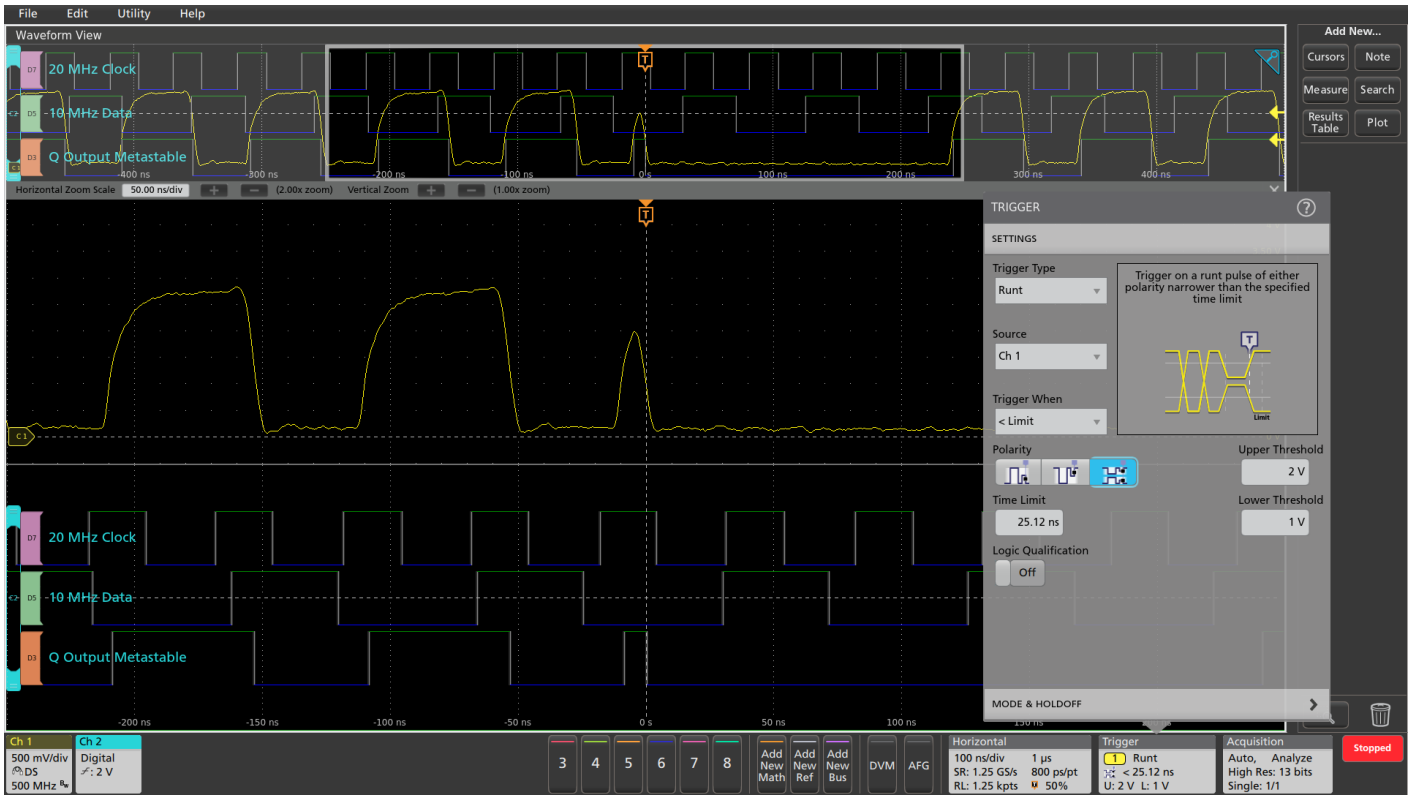


FIGURE 12. Runt triggering easily captures a low-amplitude, narrow pulse on the output of a 74LS74 flip-flop.

Not only are there intermittent glitches on the output of the flip-flop, but some appear to have a low amplitude. Figure 12 shows a runt trigger capturing narrow, low-amplitude pulses which do not meet the component's specification.

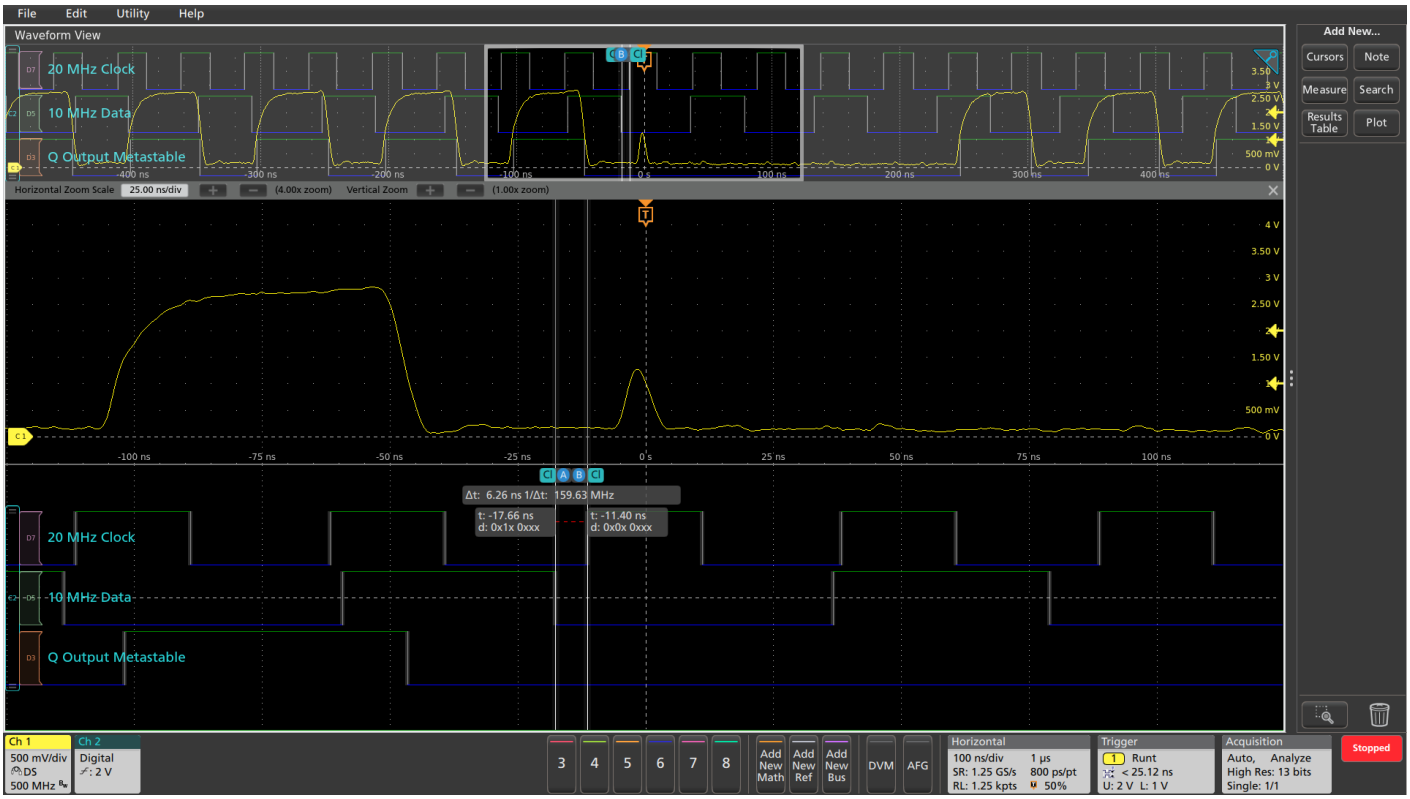


FIGURE 13. Cursor measurement of Setup Time violation triggering on a 74LVCG74 flip-flop.

Using either of these trigger setups, you can capture the input and output signals. Figure 13 shows a setup time measurement with cursors that clearly indicates a setup time violation (about 6 ns, which is much lower than the 20 ns minimum value).

Mixed signal oscilloscopes combine basic logic analyzer functionality with the analog signal analysis of an oscilloscope. Tektronix MSOs and MDOs include setup and hold triggering, pulse triggering, and high resolution digital sampling to facilitate fast digital debugging.

Appendix A

THE TEKTRONIX MSO AND MDO SERIES OFFER A RANGE OF MODELS TO MEET YOUR NEEDS AND YOUR BUDGET

	5 SERIES MSO	MSO/DPO5000 SERIES	MDO4000C SERIES	MDO3000 SERIES	MSO/DPO2000 SERIES
Bandwidth	2 GHz, 1 GHz, 500 MHz, 350 MHz	2 GHz, 1 GHz, 500 MHz, 350 MHz	1 GHz, 500 MHz, 350 MHz, 200 MHz	1 GHz, 500 MHz, 350 MHz, 200 MHz, 100 MHz	200 MHz, 100 MHz, 70 MHz
Analog Channels	4, 6, 8	4	4	2 or 4	2 or 4
Digital Channels	8 to 64 (opt.)	16 (MSO)	16 (opt.)	16 (opt.)	16 (MSO)
Spectrum Analyzer Channels	--	--	1 (opt.)	1	--
Arbitrary/ Function Generator	1 (opt.)	--	1 (opt.)	1 (opt.)	--
Record Length (All Channels)	62.5 M (std.) 125 M (opt.)	25 M (std.) Up to 125 M (opt.)	20 M	10 M	1 M
Sample Rate (Analog)	70 MHz	Up to 10 GS/s	Up to 5 GS/s	Up to 5 GS/s	1 GS/s
Max. Sample Rate (Digital)	6.25 GS/s	500 MS/s (Full Record length) 16.5 GS/s (10 kPoints centered on the trigger)	500 MS/s (Full Record length) 16.5 GS/s (10 kPoints centered on the trigger)	500 MS/s (Full Record length) 8.25 GS/s (10 kPoints centered on the trigger)	1 GS/s (using any of channels D7 – D0) 500 MS/s (using any of channels D15 – D0)
Color Display	15.6 in. HD	10.4 in. XGA	10.4 in. XGA	9 in. WVGA	7 in. WQVGA
Parallel Bus Analysis	Yes	Yes	Yes	Yes	Yes
Optional Serial Bus Triggering and Analysis Applications	I^2C SPI RS-232/422/485/UART CAN LIN FlexRay USB 2.0 10/100BASE-T Ethernet I^2S/LJ/RJ/TDM	I^2C SPI RS-232/422/485/UART CAN LIN FlexRay USB 2.0 10/100BASE-T Ethernet MIL-STD-1553 8b/10b decoding D-PHY MIPI decoding PCI Express decoding	I^2C SPI RS-232/422/485/UART CAN CAN FD LIN FlexRay USB 2.0 I^2S/LJ/RJ/TDM MIL-STD-1553	I^2C SPI RS-232/422/485/UART CAN CAN FD LIN FlexRay USB 2.0 I^2S/LJ/RJ/TDM MIL-STD-1553	I^2C SPI RS-232/422/485/UART CAN LIN
Number of Simultaneously Displayed Serial Buses	Essentially unlimited	16	3	2	2
Additional Application Support	Jitter and Timing	Power Analysis Limit and Mask Testing Jitter and Timing USB 2.0 Compliance Ethernet Compliance BroadR-Reach Compliance MOST Compliance Visual Triggering	Power Analysis HDTV & Custom Video Limit and Mask Testing Advanced RF Power Level Triggering	Power Analysis HDTV & Custom Video Limit and Mask Testing	--

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