47109629424 145667613 152722934.57143 18776596090 279039762.28571 120068477060 91808680800 49448834.447368 33360693456 25273272816 25323901.916667 14105351.935484 9717914.2150538 5112280016 184576746252 163436295698 7515450600 64089787.875 14403790.873239 61276210.294118 4384344.4505495 4992282132 43821437.666667 139902552858 11195414.86 127295506.75 21448485.8

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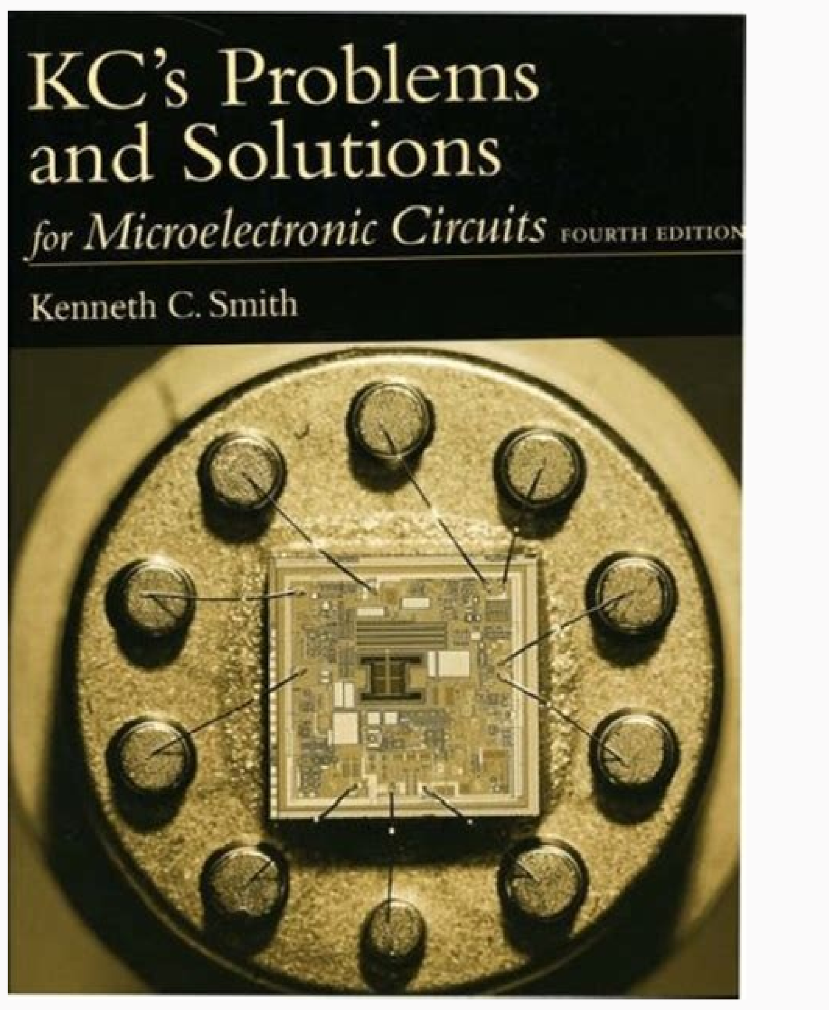

8.15(a) and assume the current source I is implemented with a single BJT that requires a minimum of 0.3 V for proper operation. Chapter 8–11 Thus, the minimum allowable VCM is VCM min = −2.2 + 0.660 = −1.54 V The upper limit on VCM is dictated by the need to keep Q1 and Q2 operating in the active mode, thus VCM max = 0.4 + VC1,2 = 0.4 + (2.5 − 0.99 × 0.2 × 5) = +1.91 V VC1 = 10.78 μA, v BE1 iC2 = 8.82 μA 10.78 × 10−3 = 0.69 + 0.025 ln 1 = 0.5767 V v BE2 8.82 × 10−3 = 0.69 + 0.025 ln 1 = 0.5717 V Thus, the input common-mode range is −1.54 V ≤ VICM ≤ 1.91 V v B1 = v BE1 = 0.5767 − 0.5717 = 0.005 V = 5 mV 8.26 (a) Refer to Fig. 1(b). This is the same factor by which the rσ the magnitude of the gain is reduced. We can then find the resistor value using = 0.6872 V 1 − 0.6872 = 0.6255 mA 2 lD = 0.5 0.6255 3. 8.30 Refer to Fig. Next the two parallel resistances 1/gm and rπ can be combined as 1 + rπ rπ rπ gm = re = 1 1 + gm rπ β + 1 + rπ gm When VO = Vx, the Early effect on Q1 and Q2 will be the same, and IO = IREF /(1 + 2/β 2) Thus, IO will be 100 = 1 + (2/1002) 99.98 μA, for an error of −0.02 μA or −0.02%. This in turn can be achieved by connecting an unbypassed Rs equal to 1/gm, 1 = 300 Rs = 3.33 mA/V Since v'gs does not change, the output voltage also will not change, thus v'o = 1.08 V. Ad = Gm Ro (d) With VBIAS = 1.4 V, the bias voltage at the collectors of Q1 and Q2 is VC1,2 = VBIAS − VBE3,4 where Gm = gm1,2 1/2 VT = 1.4 − 0.7 = +0.7 V and the upper limit on VCM is 0.4 V above VC1,2 : Ro = Ro4 Ro7 VCM max = 0.7 + 0.4 = +1.1 V Here Ro4 is the output resistance of the cascode amplifier (looking into the collector of Q4), thus Ro4 = gm4 ro4 (ro2 rπ 4) Usually rπ 4 ro2 , Ro4 gm4 rπ 4 ro4 = β4 ro4 The resistance Ro7 is the output resistance of the Wilson mirror and is given by Ro7 = 1 β7 ro7 2 Thus Ro = (β4 ro4) 1 β7 ro7 2 Since all β and ro are equal, we obtain 1 βro Ro = (βro) 2 1 βro 3 and 1 Q.E.D. Ad = βgm ro 3 For β = 100 and VA = 20 V, we have = gm ro = Ad = IC VA VA 20 = = = 800 VT IC VT 0.025 L 1 × 100 × 800 = 2.67 × 104 V/V 3.93 To maximize the positive output voltage swing, we select VBIAS as large as possible while maintaining the pnp current sources in saturation. This figure belongs to Problem 2.73. The current in Q5 will be equal to I , thus terminal Z sinks a constant current I . N = 0.6607 V 1 = 0.6607 = 0.3393 mA 1K 0.3393 = 0.6638 V 3. Thus, Chapter 2–27 v O = v Ofinal − (v Ofinal − v Oinitial)e−t/τ i=C d vI = 0.1 × 10−6 × slope dt where = 0.1 × 10−6 × v Ofinal − 1 V × dc gain = −1 V × 1000 = −1000 V Thus, v O (T) = 1000(1 − e−0.001) = −0.9995 −1 V 2.82 2 0.5 × 10−3 1 Vo = −sCR = −jωCR, Vi Vo ωCR V i 2 0 For R = 10 k and C = 1 nF, CR = 1 × 10−9 × 10 × 103 = 10 μs t (ms) 1 1 1 Vo = 1 at ω = ω0 = Vi CR 10 × 10−6 = 100 krad/s 100 = 15.9 kHz or f0 = 2π Vo = ωCR = ω = (V ω0 0) Vo For f = 10 f0 ; = 10, and the output sine Vi wave will have 10-V peak-to-peak amplitude. Thus the peak-to-peak value of vo is 3.076 − 0.23 = 2.85 V. Ex: 9.11 ft = | AM | fH 2 × 109 = 12.5 2π(CL + Cgd) × 10 × 103 = CL + Cgd = 99.5 f FCL = 99.5 − 5 = 94.5 f F Exercise 9–3 1000 s 1+ 2π × 105 Ex: 9.12 T (s) = ω 1+j ωP 1 AM ω 1+j ωP 2 2π 1+ ωH ωP 1 2 ωH 2 1+ ωP 1 The approximate value of ωH is found from Eq. (9.77): 1 1 ωH 1 ωP2 1 16ωP2 1 = 0.97ωP 1 = k = 9.88 Ex: 9.15 Cin = Cgs + Cgd (1 + gm RL) Ex: 9.14 2 = 1 + + 1+ The approximate value of ωH is obtained from Eq. (9.77), 1 1 + ωH 1 ωP2 1 4ωP2 1 = ωH = 0.95ωP 1 For ωH = 0.99ωP 1, 0.992 2 = (1 + 0.992) 1 + k2 −4= 0 17 ωH 2 1 ωH 4 + 16 ωP 1 16 ωP 1 4 2 ωH ωH + 17 − 16 = 0 ωP 1 ωP 1 = k 2.78 2= 1+ 2 =1+ For ωH = 0.9ωP 1, 0.81 2 = (1 + 0.81) 1 + 2 k For k = 1, ωH = For k = 4, the exact value of ωH is obtained from ωH 2 ωH 2 1+ 2= 1+ ωP 1 4ωP 1 | AM | |T| = 2 ω 2 1+ ω 1+ ωP 1 k ωP 1 =5 ωH = 0.89ωP 1 | AM | |T | = 2 ω 2 1+ ω 1+ ωP 2 4 = ωH = 0.84ωP 1 GB = 1000 × 100 × 103 = 108 Hz Ex: 9.13 T (j ω) = ωH ωP 1 ωH ωP 1 ωH ωP 1 ωH ωP 1 2 2 ωH 2 1+ ωP 1 2 2 = 20 + 5(1 + 1.25 × 10) = 87.5 f F fH = 1 2πCin Rsig 1 2π × 87.5 × 10−15 × 10 × 103 = 181.9 MHz This is greater than the value obtained in Example 9.8, fH = 135.5 MHz, by 34%. v O = 11.3 − 3.78 vI C 100 F R 100 vO Vr 12 = T /4 t = (a) = 23.5 μs vI 12 V 11.3 V 1.13 × 1 Vr × (T /4) = 12 12 × 4 Vr vO Now, using the fact that the charge gained by the capacitor when the diode is conducting is equal to the charge lost by the capacitor during its discharge interval, we can write vI iCav × t = C Vr t = iCav = C Vr 100 × 10−6 × 1.13 = 4.8 A = t 23.5 × 10−6 iDav = iCav + iLav T (b) 1 ms 12 V where iLav is the average current through R during the short interval t. (1), (2), and (3) provides 1 1 1 + + = 0.7 (4) RP RP1 RP2 RP4 But, 1 1 1 1 = + + RP RP1 RP2 RP4 Chapter 2-14 1 R2 1−x vO =1+ −1 =1+ =1+ vI R1 x x Thus, 1 1 1 1 = + + RP RP0 RP1 RP2 RP4 (5) Equations (4) and (5) can be combined to obtain ∴ 1 vO = vI x 0x≤1==∞2 RP RP = 0.7 RP0 = 1− RP0 0.3 (6) vO z1 vI Add a resistor as shown: vO (1 − x) × 10 k = 1+ vI x 10 k R + R vO = 11 For v I max Selecting RP0 = 10 k Equation (6) ⇒ RP = 3 k Equation (1) ⇒ RP1 = 30 k Equation (2) ⇒ RP2 = 15 k Equation (3) ⇒ RP4 = 7.5 k x = 0, 10 = R4 R3 + R4 R2 vO R4 = R2 /R1 + 1 + vI R1 R3 + R4 1 + R3 /R4 2.46 v = vI vO 10 k = 11 = 1 + vI R 10 k R R = 1 k 2.49 10 k vO1 = −10v 1 Setting v 1 = 0, we obtain the output component due to v 2 as 10R 10R 0 vO2 = v 2 1 + = 10v 2 R 10R + R The total output voltage is For v1 = 10 sin(2π × 60t) − 0.1 sin(2π × 1000 t) vO 10 k vO = vO1 + vO2 = 10(v 2 − v 1) 1 k vI 1 k 2.47 Refer to Fig. P8.116. From Eq. (1) we see that the maximum value of Rout /ro is obtained with Re = ∞ and its value is 101, which is (β + 1). P8.55, vo = (a) vI Total resistance across which v o appears α Total resistance in the emitter 2 k =α× re1 + re2 VT , where IE is the dc emitter current of each of Q1 and Q2 , we use To determine re1 = re2 = re = VE = VB − VBE = 0 − 0.7 = −0.7 V −0.7 − (−5) = = 1 mA 4.3 IE = 0.5 mA 2IE = 25 mV = 50 0.5 mA 2 k =α× 20 V/V 0.1 k re1 = re2 = vo vi re Chapter 8–20 (b) The common-mode half-circuit is shown in the figure, α × 2 k vo = − vicm (0.05 + 8.6) k −0.23 V/V vo = 0.23 V/V cm (c) CMRR = 20 lv o /v id | = 86.5 |v o /v icm | 0.23 or 38.7 dB (d) vo = −0.023 sin 2π × 60t + 0.2 sin 2π × 1000 t volts 8.56 RC 2RSS RC RC 10 × 0.02 = 0.001 V/V 200 To obtain Ricm , we use Eq. (8.96): | Acm | = Figure (a) shows the differential half-circuit. This in turn is achieved by biasing the transistor at the lowest VCE consistent with the transistor remaining in the active mode at the negative peak of v o . Thus α β β Q.E.D. β α For 4.5 Old technology: α 1−α β = −10% and β = 100, β −10% α = −0.1% α 100 4.10 Transistor is operating in active region: β = 50 → 300 IB = 10 μA IC = βIB = 0.5 mA → 3 mA IE = (β + 1) IB = 0.51 mA → 3.01 mA Maximum power dissipated in transistor is = 6 IB = 10 μA IE × 0.7 V + IC × VC IC = 800 μA = 0.01 × 0.7 + 3 × 10 = 30 mW Chapter 4–2 4.11 For iB = 10 μA, α 1.14 First we determine IS , β, and α: iC = iE − iB = 1000 − 10 = 990 μA 1 × 10−3 = IS e700/25 β = = IS = 6.91 × 10−16 A iC 990 = 99 iB 10 β 99 α= = = 0.99 β + 1 100 β= IC 1 mA = 100 = IB 10 μA For iB = 20 μA, β = 100 = 0.99 β + 1 101 iC = iE − iB = 1000 − 20 = 980 μA Then we can determine ISE and ISB : β= iC 980 = 49 = IB 20 ISE = IS = 6.98 × 10−16 A α = 0.98 β +1 50 ISB = IS = 6.91 × 10−18 A β For iB = 50 μA, The figure below and on next page shows the four large-signal models, corresponding to Fig. From Eq. (2.36), we know that the output dc voltage due to VOS is RF RF = 2 V = 2 mV 1 + VO = VOS 1 + R 10 k RF = 1000 ⇒ RF 10 M 10 k The corner frequency of the resulting STC 1 network is ω0 = CRF 1 = We know RC = 1 ms and R = 10 k ⇒ C = 0.1 μF Thus ω0 = f0 = 1 = 1 rad/s 0.1 μF × 10 M 1 ω0 = = 0.16 Hz 2π 2π Ex: 2.26 20 log A0 = 40 dB ⇒ A0 = 200,000 V/V ft = 3 MHz fb = ft /A0 = 3 MHz = 15 Hz 200,000 Exercise 2–8 At fb , the open-loop gain drops by 3 dB below its value at dc; thus it becomes 103 dB. Observe that 1 2 it intersects the horizontal line (0 A·n = VOV 3 at 2 1 v DS = VOV 3 , 1 through 3 (see preceding page). 7.38, Ron = (gm2 ro2) (ro1 rπ 2) = (8 mA/V) (25 k) (25 k 12.5 k) Ron = 1.67 M For the pnp transistors, gm3 = gm4 = rπ 3 = rπ 4 |IC | 0.2 mA = 8 mA/V = VT 25 mV β 50 = 6.25 k = = gm 8 mA/V ro3 = ro4 = |VA | 4V = 20 k = |IC | 0.2 mA Rop = (gm3 ro3) (ro4 rπ 3) = (8 mA/V) (20 k) (20 k 6.25 k) Rop = 762 k Av = −gm1 Ron Rop = −(8 mA/V) (1.67 M 762 k) Av = −4186 V/V gm = 2 ID 2 × 0.1 = 0.88 mA/V = VOV 0.227 rπ = VA L 5 × 0.36 = 18 k = A = ID 0.1 Ro = (gm3 ro3)ro2 = (0.88 × 18) × 18 = 285 k Ex: 7.26 For the Wilson mirror from Eq. (7.94), we have IO 1 = 0.9998 2 IREF 1 + 2 β Thus |IO − IREF | IO = 100 = 0.02% IREF whereas for the simple mirror from Eq. (7.18) we have IO 1 = 0.98 = 2 IREF 1 + β |IO − IREF | × 100 = 2% IREF Av max occurs when ro1 and ro4 are ∞ . Thus, IS = 0.545Vx − 0.5Vx = 0.022Vx 0.5 + 1 = 0.545 Vx = 0.022 Vx 0.5 2 = 0.5Vx 1.022 = 0.511Vx V1 = Between node 2 and ground, V2 = V1 + IS R5 = 0.533Vx RTh = 9.1 k Thus, the v O = 0.489Vx 1 k Vx = V2 I2 = = 0.467Vx 1 k Ix = I1 + I2 = 0.956Vx I1 = 1 = 0.5Vx 1 + 1 I + 1 = 5.47 V 1 V + 9.1 This resulting simplified circuit is 0.545 k 1 I5 2 4.98 k = Req = R5 2 k 5.45 V I5 = V5 5.47 V 5.47 − 5.45 4.98 + 2 + 0.545 = 2.66 μA V5 = 2.66 μA × 2 k = 5.32 mV 1.18 From the symmetry of the circuit, there will be no current in R5 . Thus V7 = V5 = 2.8 V and, as a check, 5 − 2.8 = 1 mA. 1. When v I exceeds the battery voltage (3 V), D1 cuts off and D2 conducts, thus steering I into the battery. At ω = 104 rad/s, Vo 10 = V 100 = √ 9.95 V/V V 100 1 + 1 + 0.01 j ω = φ = −tan−1 0.1 = 180◦ + 90◦ − tan−1 0.1 = 180◦ + 84.3◦ Both these results differ slightly from the ideal values. vI R1 Exercise 3–9 V I ≥ 0 ⇒ diode is cut off, loop is open, and the opamp is saturated: vO = 0 V vI ≤ 0 ⇒ diode conducts and closes the negative feedback loop: vO = vI For vI ≤ −5 V, diode D1 conducts and I = (v1 + 5)/5 diode D2 conducts and I = (vI + 5)/5 i − 5V vI V + = 2 V D + vI = −5 + 5 Ex: 3.26 10 k 10 k Both diodes are cut off for −5V ≤ v I ≤ + 2V and v O = v I vO 5V D1 5V Ex: 3.27 Reversing the diode results in the peak output voltage being clamped at 0 V: 10 k t 10 V Here the dc component of v O = VO = −5 V Chapter 3–1 3.3 3.1 1 (a) 1 1.5 V VD D1 1 V (a) Cutoff D2 V2V 2 V Conducting 1 I 2 k 1.5 V I VD 2 D1 3 2 k 2.5 mA 3 V (b) 3 V (a) The diode is reverse biased, thus I =0A VD = −1.5 V 2 k Conducting 3 (1) 2 1 mA I D1 1 V1V (b) The diode is forward biased, thus VD = 0 V 2 V D2 1.5 V 1.5 A1= 1 3.2 Refer to Fig. Note that the starting point is calculating the current I in the Q1 –Q2 branch. 2.10 2.9 There are four possibilities: 10 k 10 k vI 10 k gain magnitude) (a) G = −10 V/V (c) G = −0.1 V/V (d) G = −10 V/V (e) G = −10 V/V 2.11 (a) G = −1 V/V ⇒ Rin = 10 k (largest gain magnitude) −R2 R1 = −R2 = 10 k R1 (b) G = −R2 = R1 10 k R1 (c) G = −R2 = R1 100 k R1 (c) G = −5 V/V ⇒ −R2 = R1 = 10 k, R2 = 50 k R1 Chapter 2–3 46.69 20 log |G| (d) G = −100 V/V ⇒ −R2 = R1 = 10 k, R2 = 1 M (e) G = −200 : R2 vO = −200 V/V ⇒ vI R1 = R2 = 200R1 ≤ 1 M R1 2 R2 = 1 M for the largest possible input resistance, choose R2 R2 = 1 M 1 M = 5 k 200 Rin = R1 = 5 k R1 = R1 vI vO 2.15 The circled numbers indicate the order of the analysis steps. RC iC1 RC iC2 vo1 vicm Q1 2 Q2 ie1 vicm ie2 ve vicm vicm REE REE With a common-mode input signal v icm applied, as shown in the figure, the current (v icm /REE) will split between Q1 and Q2 in the same ratio as that of their base-emitter junction areas, thus ie1 = 2 v icm 3 REE and ie2 = 1 v icm 3 REE Thus, v o1 = −ic1 RC −ie1 RC = − 2 RC v icm 3 REE and v o2 = − 1 RC v icm 3 REE Thus the differential output voltage vod will be v od = v o2 − v o1 = Acm = 1 RC v icm 3 REE 1 RC 1 2 = × 0.008 V/V 3 REE 3 500 8.62 If the output is taken single-endedly, then | Acm | = RC 2REE | Ad | = 1 gm RC 2 Chapter 8–23 CMRRs = | Acm | = gm REE | Ad | VOS = VOV 2 RD RD (0.5 | | gm = | For RD (b) For each value of VOS we use Eq. (2) to determine I and then Eq. (1) to determine Ad . Thus, IE = IC2 = αIE2 = 0.99 × 0.542 = 0.537 mA I2 = IC2 − IB3 = 0.537 − IE3 101 Since the voltage drop across the 6.2-k resistor is equal to (5.7 − 2IE2), I2 × 6.2 = 0.7 + 2.4IE3 2 O.7 − 1.1 mA 10 + 51 VE = +1.1 V VB = 1.8 V (c) For v I = −2.5, Q1 will be off and Q2 will be on, and the circuit reduces to that in Fig. The result is the following circuit: 40 k vN vp 10 k 3.33 k vp 10 k 10 RP RP =1= 0.1 RP1 RP1 (1) Similarly, equating the coefficients of v I 2 gives 10 RP RP =2= = 0.2 RP2 RP2 (2) and equating the coefficients of v I 4 gives 10 k Equate the coefficients of v I 1 RP RP1 RP2 RP4 (3) Now, summing Eqs. (1) through (3) and ... μA 50 k 0.167 10 μA 5 k 0.667 100 μA 500 0.952 1 mA 50 0.995 10 mA 5 0.9995 I = 1 μA, I I I I rd rd rd rd vo vI R Equivalent Circuit 1 k Chapter 3–15 b. Refer to the analysis shown in the figure, which leads to β≡ 3.952 IC = 82.3 IB 0.048 Chapter 4–7 VE = +0.68 V (c) and 2.5 − 0.68 = 3.64 k 0.5 The maximum allowable value for RC while the transistor remains in the active mode corresponds to VC = +0.4 V. Chapter 3–8 Taking the ratio of the above two equations, we have The power dissipation is given by PD = (10 A) (0.6 V) = 6 W ID1 = IS e(VD1 −VD2)/VT = VD1 − VD2 ID2 ID1 = VT ln ID2 The thermal resistance is given by 50◦ C T = 8.33◦ C/W = PD 6W 3.29 For ID = 1 mA, we have 1 × 10−3 A = −230 mV V = VT ln 10 A 10 V I R1 = VD = 570 mV D1 V1 D2 V2 For ID = 3 mA, we have 3 × 10−3 A = −202 mV V = VT ln 10 A ⇒ VD = 598 mV Assuming VD changes by –2 mV per 1◦ C increase in temperature, we have, for ±20◦ C changes: For ID = 1 mA, 530 mV ≤ VD ≤ 610 mV At 20◦ C: For ID = 3 mA, 558 mV ≤ VD ≤ 638 mV VR1 = V2 = 520 mV R1 = 520 k 520 mV = 1 μA I= 520 k Since the reverse current doubles for every 10◦ C rise in temperature, at 40◦ C, I = 4 μA ID2 40°C 4 μA 40 mV 520 mV V2 = 480 + 2.3 × 1 × 25 log 4 = 514.6 mV VR1 = 4 μA × 520 k = 2.08 V 1 μA V2 = 560 − 2.3 × 1 × 25 log 4 At 0◦ C, I = = 525.4 mV 1 VR1 = × 520 = 0.13 V 4 3.30 Given two different voltage/current measurements for a diode, we can write ID1 = IS eVD1 /VT ID2 = IS eVD2 /VT 3.31 Given two different voltage/current measurements for a diode, we have ID1 = IS e(VD1 −VD2)/VT ⇒ VD1 − VD2 ID2 ID1 = VT ln ID2 20°C For the first diode, with ID = 0.1 mA and 1 μA 480 Thus the overall range of VD is between 530 mV and 638 mV. 10−5 cm = 9.63 pC Reverse current I = IS = Aqn2i Ex: 1.34 Equation (1.65) IS = Since Aqn2i = 10−14 × 1.6 × 10−19 × (1.5 × 1010)2 10 18 × + 5 × 10−4 × 1016 10 × 10−4 × 1018 Dp Dn + . 7.91 From Fig. Note AV is negative. Chapter 2–30 2.88 Inverting configuration: 2.91 (a) IB = (IB1 + IB2)/2 R2 VO = VOS 1 + R1 −0.2 = VOS 1 + R2 R1 = VOS Open input: v O = v + + R2 IB1 = VOS + R2 IB1 100 1+ 2 ⇒ VOS 4 mV 2.89 VOS = ±2 mV VO = 0.01 sin ωt × 100 + VOS × 100 = 1 sin ωt ± 0.2 V 5.3 = VOS × 101 + 10,000IB1 (1) Input connected to ground: v O = v + + R2 VOS IB1 + R1 R2 = VOS 1 + R2 IB1 R1 5 = VOS × 101 + 10,000IB1 (2) Equations (1), (2) ⇒ 100VOS = −0.3 ⇒ VOS = −3 mV ⇒ IB1 = 530 nA IB IB1 = 530 nA 2.90 Input offset voltage = 3mV and both flow into the op-amp input terminals. P8.19. IE3 = 0.7 + 2.4IE3 6.2 0.537 − 101 ⇒ IE3 = 1.07 mA V6 = −5 + 1.07 × 2.4 = −2.43 V V5 = V6 + 0.7 = −1.73 IC3 = α × IE3 = 0.99 × 1.07 = 1.06 mA Figure 2 V7 = −3.9 × 1.06 = 0.87 V Since VB > −2.5, VC will be lower than VB and Q2 will be operating in the active region. The corresponding input signal amplitude can be found by dividing 1.7 V by the gain magnitude (320 V/V), resulting in 5.3 mV. 1 v BE /VT IE = IS 1 + β (3) When the base is left open-circuited, iB = 0 and Eq. (1) yields IS v BE /VT e ICBO = β 4.31 Refer to the circuit in Fig. Since ID2 = ID1 and k n = k p , then VOV 2 = VOV 1 . Halving VOV results in decreasing ID by a factor of 4. 2 = 6.91 × 10−16 × e0.75/0.025 Voltage drop across each diode = Correspondingly, the voltage across each diode changes by VD where ∴ ID = IS eV /V T 3 = e VD /VT 8 IL = 1.5/1.5 = 1 mA 3 ⇒ VD = 25 ln = −24.5 mV 8 I = ID + IL = 7.39 mA + 1 mA and the output voltage changes by VO = 2 × VD = −49 mV With I = 15 mA, the diodes current changes from 13 to 8 mA. It follows that our assumption is wrong and D1 must be off. 3.81 v I > 0: D1 conducts and D2 cutoff (b) See figure (b) on next page. 1 VGS2 = 1.84 V Since Q1 is identical to Q2 and is conducting the same ID , then VGS1 = 1.84 V ⇒ V1 = 2.5 − 1.84 = 0.66 V which confirms that Q1 is operating in saturation, as assumed. For IE to remain unchanged, 4.54 5 V IB 3 − 0.7 3 − 0.7 = 20 100 2.2 + 2.2 + 41 β +1 ⇒ RB RC 1 k VC 20 100 = 41 β +1 β + 1 k VB 410 = 205 2 IE VE RE 1 k β = 204 4.53 3 V IE A loop equation for the EB loop yields 5 = IB RB + VBE + IE RE RE ⇒ IE = VE 0.7 V IE = VBC 1 V VC 1 V IC RC 5 − 0.7 RB RE + β +1 4.3 RB 1+ 101 (a) For RB = 100 k, IE = 3 V 4.3 = 2.16 mA 100 1+ 101 VE = IE RE = 2.16 × 1 = 2.16 V Refer to the figure. First consider Q1 and Q2 . 7.39. C aiE B iE DE IS ISE a vBE ( ) E Figure 1 If iE undergoes an incremental change ie from its equilibrium or bias value IE , the voltage v BE will correspondingly change by an incremental amount v be (from its equilibrium or bias value VBE), which is related to ie by the incremental resistance of diode DE . 2(Vp − VD) VO 1+π = RL Vr 2(13.7 − 0.7) 12 1+π = 0.2 2 = 739 mA 13.7 − 0.7 2 × 60 × 200 × C ⇒C= Vp − VD 2fCR vO = 739 mA 3.77 120 Vrms 60 Hz D4 D1 C R vS vO D2 D3 Chapter 3–31 12 V 11.3 11.3 Vr 10.2 V (a) VO = Vp − 2VD − 1 = Vp = VO +2VD +1 = 12+2×0.7+1 = 14.4 V 14.4 Vrms = √ = 10.2 V 2 Vp − 2 VD (b) Vr = 2fCR] T 0 14.4 − 1.4 = 271 μF 2 × 2 × 60 × 200 (c) The maximum reverse voltage across D1 occurs when Vs = −Vp = −14.4 V. Thus ⇒ VO,avg 2Vs − 2VD π √ 2 × 12 2 − 1.4 = 9.4 V = π Peak voltage (b) Peak diode current = R √ Vs − 2VD 12 2 − 1.4 = = R 100 = 156 mA √ PIV = Vs − VD = 12 2 − 0.7 = 16.3 V Ex: 3.22 Full-wave peak rectifier: D1 vO vS vS 97.4 % Average output voltage VO is √ Vs 2 × 12 2 VO = 2 − VD = − 0.7 = 10.1 V π π Peak diode current ˆiD is √ ˆiD = Vs − VD = 12 2 − 0.7 R 100 1 2π 2 [−Vs cos φ − 2VD φ]π−φ φ=π−θ 2π 1 = [Vs cos φ − Vs cos(π − θ) − 2VD (π − 2θ)] π But cos θ ≈ 1, for θ small. P6.49. 7.13(b). = τT · VT 1 Wn2 · Ip for Wn xn 2 DP (d) Cd = (c) For Q Qp , I Ip , Q 1 Wn2 I 2 Dp Cd = 1 Wn2 1 × 10−3 = 8 × 10−12 F 2 10 25.9 × 10−3 Solve for Wn : Wn = 0.64 μm Exercise 2–1 Ex: 2.1 The minimum number of terminals required by a single op amp is 5: two input terminals, one output terminal, one terminal for positive power supply, and one terminal for negative power supply. This restriction is imposed by the current I = 1 mA 157 μA to 157 × 10 μA 10 Range is 15.7 μA to 1570 μA A similar table can be generated for the negative values. PIV= 10 V 3.64 D vD vS vO R iD = IS ev D/V T = 0.324 V iD = e[v D −v D (at 1 mA)]/V T iD (1 mA) iD v D − v D (at 1 mA) = VT ln 1 mA v D = v D (at 1 mA) + VT ln v O /R I vO = vS − vD = v S − v D (at 1 mA) − VT ln where R is in k. 2 below. This table belongs to 5.13. Also, at IC = 0.25 mA, gm = 10 mA/V. ∴ Av = −156.67 V/V max +v O = 5 − 4.5 = 0.5 V Now we can find the dc collector voltage. Similarly, for v I < −10.7 V, v O will be saturated at −10 V. When we short circuit the voltage source, we see that the Thévenin resistance will be zero. P8.82: RSS = gm7 ro7 ro9 Transistor Q7 has the same k (W/L) as Q1 and Q2 , but Q7 carries a current I twice that of Q1 and Q2 . At IC = 0.5 mA, 8 = Cde + 2 ⇒ Cde = 6 pF 2VA 2VA L 9.16 A0 = = VOV VOV A0 = 2×5×L = 50L, V/V (L in μm) 0.2 fT 3μn VOV 3 × 400 × 108 × 0.2 = 2 4πL 4πL2 fT = 1.91 , GHz (L in μm) L2 1 At IC = 0.25 mA, Cde = × 6 = 3 pF, and 2 Cπ = 3 + 2 = 5 pF. Since VC VB , VC must be set to 0.7 by selecting RC according to VC = 0.7 = VCC − IE RC Thus, VC 0.5 V IC RC 2.5 V From the figure we see that VC = −0.5 V is lower than the base voltage (VB = 0 V); thus the transistor will be operating in the active mode. R2 vO = −10 V/V = − vI R1 3 1 mA 10 k ⇒ R2 = 10R1 1 k Total resistance used is 110 k 1 V ∴ R1 + R2 = 110 k 1 mA 2 6 6 mA 0V 1 10 V 4 5 mA 5 2 k R1 + 10R1 = 110 k R1 = 10 k and R2 = 10R1 = 100 k 2.13 2.16 The circuit will be as follows: R +10 V R 15 V 15 k Average = +5 V Highest = +10 V Lowest = 0 V Variation of the −15-V supply by ±1% results in a ±1% variation in the output voltage. From Eq. (1) we see that v id = 0 results in v O = 50 V, which is impossible; thus the op amp saturates and v O = +10 V. Transistor Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 ID I 2 I 2 I 2 I 2 I 2 I I 2 I gm |VOV | I |VOV | I |VOV | I |VOV | 2I |VOV | I |VOV | I |VOV | ro 2|VA | I 2|VA | I 2|VA | I 2|VA | I |VA | I 2|VA | I |VA | I Chapter 8–45 This figure belongs to Problem 8.116, part (b). (a) See figure on next page. To make IL = I /3 (and thus the current through R, 2I /3), R should be such that I 1.1R 4 R1 Rin To make the current through R equal to 0.2I , we shunt R by a resistance R1 having a value such Rin = 1.1R 1.1R 4 1.1R 5 that is, 10% higher than in case (a). 100 = 21 V/V Ad = 1 1 + 5 Acm = 0 CMRR = ∞ If all resistors have ±1% tolerance, the differential gain will be slightly affected; Eq. (1) indicates that in the worst case Ad can deviate by approximately ±4% of the nominal value. Rs 10 k vs 5 mV #1 #2 #n vi1 vi2 vin vo RL 200 Ri1 10 k Ron 1 k 1 k #m vim vi(m 1) vim Ri(m 1) v i1 10 k = 0.5 V/V = vs 10 k + 10 k 10 k 10 k vi(m 1) 10vim Thus Ri = 40 k. 1 = 50 gm2 1 A/V = 20 mA/V 50 If Q1 is biased at the same point as Q2 , then ⇒ gm2 = gm1 = gm2 = 20 mA/V id 1 = gm1 × 5 (mV) = 20 × 0.005 = 0.1 mA v d 1 = id 1 × 50 = 0.1 × 50 = 5 mV v o = id 1 RD = 1 V RD = v o = 14.3 × v i2 = 14.3 × 0.5v i vo = 7.15 V/V vi 6.112 (a) DC bias: Refer to the circuit in Fig. IREF = 1 mA ⇒ IO = Thus, the diode-connected BJT has a small-signal resistance re . ISB = 5 × 10−15 IS = = 10−16 A β 50 0.5 × 10−3 IC = = 10−5 A β 50 IB VB VBE = VT ln ISB −5 10 = 0.025 ln 10−16 IB = (d) B iC iB C vBE DB IS ISB b biB = 0.633 V We can determine RB from iE RB = E b 100 ISB 6.91 1018 A 15 − 0.633 = 1.44 M 10−5 To obtain VCE = 1 V, we select RC according to = 4.15 5 V RC = 2 k VC C aiE DE E = VCC − VCE IC 15 − 1 = 28 k 0.5 4.17 IS = 10−15 A B iE VCC − VB IB VE 2 mA Thus, a forward-biased EBJ conducting a current of 1 mA will have a forward voltage drop VBE : I VBE = VT ln IS −3 10 = 0.025 ln = 0.691 V 10−15 ISC = 100IS = 10−13 A Chapter 4–4 Thus, a forward-biased CBJ conducting a 1-mA current will have a forward voltage drop VBC : VBC = VT ln −3 1 × 10 1 × 10−13 4.19 The equations utilized are v BC = v BE − v CE = 0.7 − v CE iBC = ISC ev BC /VT = 10−13 ev BC /0.025 = 0.576 V iBE = ISB ev BE /VT = 10−17 e0.7/0.025 When forward-biased with 0.5 V, the emitter–base junction conducts iB = iBC + iBE I = IS e0.5/0.025 Performing these calculations for v CE = 0.4 V, 0.3 V, and 0.2 V, we obtain the results shown in the table below. R For VS = −1 V (10% low), VO = −0.15 V and VO = 7.35 V. IC = α(VBB − VBE) RB RE + β +1 6.116 Refer to the circuit of Fig. v O = −(3v 1 + 3v 2) 100 k 100 k 2.39 100 k 100 k v1 vO 100 k v2 100 k 100 k In order to have coefficient = 0.5, connect one of vO the input resistors to v O . P7.65. isc = is (t) 100 = 9.9 mV 100 + 1 If RL = 10 k: For equivalency v o = 10 mV × Rs is (t) = v s (t) 10 9.1 mV 10 + 1 If RL = 1 k: Rs a v o = 10 mV × 1 = 5 mV 1+1 If RL = 100 : vs (t) v o = 10 mV × 100 0.91 mV 100 + 1 K For v o = 0.8v s , b RL = 0.8 RL + Rs Figure 1.1a Since Rs = 1 k, a is (t) RL = 4 k Ex: 1.4 Using current divider: Rs io b is 10 A RL Rs Figure 1.1b Ex: 1.2 io = is × Rs voc vs isc = 10 μA v oc 10 mV = = 1 k isc 10 μA Ex: 1.3 Using voltage divider: v o (t) = v s (t) × Given is = 10 μA, Rs = 100 k. The value of VOV can be found from √ 2 VOV = 0.25 V 0.25 ⇒ VOV = √ = 0.18 V 2 The realized value of gm will be gm = 2 × (I /2) VOV 0.5 = 2.8 mA/V 0.18 To obtain a differential gain Ad of 10 V/V, ⇒ Ad = gm RD 10 = 2.8 × RD ⇒ RD = 3.6 k Finally, the required value of W/L can be determined from I W 2 1 ID = = μn Cox VOV 2 2 L 1 W 0.25 = × 0.4 × × 0.182 2 L W ⇒ = 38.6 L ⇒ VOV = 0.25 V gm = 2 × (I /2) VOV 8.13 To limit the power dissipation to 1 mW, P = (VDD + VSS)I I 2= 0.25 Thus, the maximum value we can use for I is ⇒ I = 0.5 mA I= Ad = 1V = 10 0.1 V gm RD = 10 10 = 5 k 2 I 1 W 2 = μn Cox VOV 2 2 L ⇒ RD = 1 mW = 0.5 mA 2V Using this value, we obtain I RD 2 0.2 = 1 − 0.25 × RD VD VDD − ⇒ RD = 3.2 k Ad = gm RD 10 = gm × 3.2 Chapter 8–6 gm = 10 = 3.125 mA/V 3.2 8.15 Since both circuits use the same supply voltages and dissipate equal powers, then their currents must be equal, that is, 2 × (I /2) I = VOV VOV ID I But gm = 3.125 = 0.5 VOV ⇒ VOV = 0.16 V To obtain W/L, we use 1 W 2 VOV ID = μn Cox 2 L W 1 × 0.162 0.25 = × 0.4 × 2 L W ⇒ = 48.8 50 L where ID is the bias current of the CS amplifier and I is the bias current of the differential pair. v I = 2.5 V: if we assume that the NMOS is turned on, then v O would be less than 2.5 V, and this implies that PMOS is off (VSGP < 0) . 6.55(a) and (c) and to the values found in the solution to Exercise 6.37 above. 2 pn = n2i (1.5 × 1010) = = 2.25 × 103 /cm3 ND 1017 Using R = ρ · L with L = 0.001 cm and A Hole concentration = pn = 2.25 × 103 /cm3 A = 3 × 10−8 cm2 , we have T = 125◦ C = 273 + 125 = 398 K R = 7.6 × 109 . 6.83 Thus, Gv becomes Gv = −100 × 9.1 k 10 k i = −91 V/V 0 6.82 Adapting Eq. (6.114) gives RC RL ro Gv = −β Rsig + (β + 1)re RC RL ro =− Rsig β +1 + re β β Rsig G vsig ro vg i 1 gm RL vo Chapter 6–29 v g = v sig RS = Noting that ro appears in effect in parallel with RL , v o is obtained as the ratio of the voltage divider formed by (1/gm) and (RL ro), Gv = vo vo = = v sig vg (RL ro) (RL ro) + 1 gm Also, With RL removed, ro = 0.98 Gv = 1 ro + gm (1) With RL = 500 , (500 ro) Gv = = 0.49 1 (500 ro) + gm (2) ro 1 = gm 49 VDD =3V 3 3 ⇒ RD = = 3 k 1 VG = VS + VGS ID RD = Q.E.D. From Eq. (1), we have 3 = 3 k 1 =3+2=5V Thus the voltage drop across RG2 (5 V) is larger than that across RG1 (4 V). (b) Replacing the BJT with its T model (without ro) and replacing the capacitors with short circuits results in the equivalent-circuit model shown in Fig. P5.46. 1 on next page. v = 0.7 + 0.025 ln(10) = 0.76 V 0.43 1 0.432 1 ∴ The iteration yields ID = 0.43 mA, VD = 0.68 V Ex: 3.8 T = 125 − 25 = 100◦ C b. Practically speaking, one normally uses the low value to minimize power dissipation. Thus, we can write for Q4 , I4 = I3 = 40 μA and using 1 W μn Cox V2 2 L 4 OV 1 W 40 = × 400 × × 0.22 2 L 4 W ⇒ =5 L 4 ID4 = W4 = 2.5 μm Finally, since I5 = 80 μA = 2 I4 , W W =2 L 5 L 4 W ⇒ = 10 L 5 W5 = 5 μm To find the value of R, we use |VSG1 | = |Vtp | + |VOV 1 | = 0.5 + 0.2 = 0.7 V R= 1 − |VSG1 | 0.3 V = IREF 0.02 mA = 15 k 7.8 (a) If IS = 10−17 A and we ignore base currents, then IREF = IS eVBE /VT so that IREF VBE = VT ln 10−17 For IREF = 10 μA, −5 10 VBE = 0.025 ln = 0.691 V 10−17 For IREF = 10 mA, −2 10 = 0.863 V VBE = 0.025 ln 10−17 So for the range of 10 μA ≤ IREF ≤ 10 mA, 0.691 V ≤ VBE ≤ 0.863 V (b) Accounting for finite β, IO = IREF · For IREF = 10 μA, IO = |VAp |×L |VA2 | = I2 I2 10 μA = 9.62 μA 2 1+ 50 For IREF = 0.1 mA, IO = The output resistance of the current source Q2 is ro2 = 1 1 + 2/β 0.1 mA = 0.098 mA 2 1+ 100 For IREF = 1 mA, 1 mA = 0.98 mA 2 1+ 100 5 × 0.5 = 25 k = 0.1 mA IO = The output resistance of the current sink Q5 is For IREF = 10 mA, ro5 VA5 V × L = = An I5 I5 = 5 × 0.5 = 31.25 k 80 IO = 10 mA = 9.62 mA 2 1+ 50 Chapter 7–4 7.11 7.9 VDD VDD Q1 Q2 IO IREF IO = mIC1 A node equation at the collector of Q1 yields IREF For identical transistors, the transfer ratio is 1 IO = = IREF 1 + 2/β IO + IC1 = IC1 + β 1 1+ 2 50 = 0.96 Substituting IC1 = IO /m results in m m+1 1+ β IO = IREF Q.E.D. For β = 80 and the error in the current transfer ratio to be limited to 10%, that is, m ≥ 0.9m m+1 1+ β 1+ m+1 β ≤ 1 0.9 1 m+1 ≤ −1 β 0.9 m≤β 1 −1 −1 0.9 1 − 1 − 1 = 7.88 m ≤ 80 0.9 Thus, the largest current transfer ratio possible is 7.88. Thus, the diode-connected MOSFETs of Fig. Since the two NMOS transistors are identical and have the same ID , their VGS values will be equal. Active Saturation Active Saturation Active Cutoff β= IC = 80 IB α= 80 β = = 0.988 β +1 81 4.7 α 4.2 The EB junctions have a 4:1 area ratio. The extension of the depletion width into the n and p regions is given in Eqs. Thus, VBB = 4 V. E2.3. v d = R(Gm2 v 2 − Gm1 v 1) v O = v 3 = μv d = μR (Gm2 v 2 − Gm1 v 1) 2.3 vO = vd = v2 − v1 vO v O /v d 1 0.000 0.000 0.000 0.00 − 2 1.00 1.00 0.000 0.00 − 3 1.00 (b) 1.00 4 1.00 1.10 0.10 10.1 101 5 2.01 2.00 -0.01 -0.99 99 6 1.99 2.00 0.01 1.00 100 7 5.10 (d) -5.10 # v1 (a) v2 (c) we have v O = Ad v Id + Acm v Icm Experiments 4, 5, and 6 show that the gain is approximately 100 V/V. E2.5 to the input of this amplifier, we have: v i is a virtual ground that is v i = 0, thus the current flowing through the 10-k resistor connected between v i and ground is zero. This frequency is found as follows: The transfer function of each STC circuit is T (s) = 1 1+ 1 = 1.4 × 10−8 F 2π × 110 × 103 × 102 Thus we select C1 = 1 × 10−7 F = 0.1 μF. Obviously, in this case there is no need for output trimming. VO = Vx − RL IL = −1 − RL × 10.1 I3 4I RL = 100 , VO = −2.01 V; RL = 1 k, VO = −11.1 V Figure 2 ∴ −11.1 V ≤ VO ≤ −2.01 V Chapter 2–8 2.32 2.31 1.5 V iI 10 k I1 R1 Vx IL I2 I i RL R R2 which is independent of the value of RL . The equivalent circuit is then R 1 To limit v s ≤ 1 V, the net resistance has to be ≤ 2 k. No part of this publication may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording, or otherwise, without the prior permission of Oxford University Press. 6.95 RB1 × 3 = 0.710 RB1 + RB2 RB2 = 3.225 RB1 Given that RB1 and RB2 are 1% resistors, the maximum and minimum values of the ratio RB2 /RB1 will be 3.225 × 1.02 = 3.2895 and 3.225 × 0.98 = 3.1605. iE1 = 11 μA, iE2 = 9 μA = I /2 ≤ 2 μA β +1 iE1 − 0.5 I Chapter 8–12 This table belongs to Problem 8.29. 1 + 10/A vO = vI If A = 103 , then G = 9.901 and G − 10 × 100 = −0.99% −1% 10 For v I = 1 V, v O = G × v I = 9.901 V and 10 mA iL = =∞ iI 0 v O × iL 10 × 10 PL =∞ = PI v I × iI 1×0 Ex: 2.14 (a) Load voltage = 1 k × 1 V 1 mV 1 k + 1 M (b) Load voltage = 1 V ⇒ v O = A(v + − v −) ⇒ v + − v − = vO 10 V = = 10 V/V or 20 dB vi 1V Ex: 2.15 9.901 vO = A 1000 9.9 mV If A = 104 , then G = 9.99 and = −0.1%. In the following we analyze the circuit to find ix and hence Rin , as vx Rin ≡ ix 0.2 = 0.1998 mA 2 1+ 2 50 0.4 = 0.3997 mA 2 1+ 2 50 IO2 = IO4 re3 Note that all three transistors are operating at equal emitter currents, approximately equal to IREF . 2.31(a), then the input offset voltage VOS will see a unity-gain amplifier [Fig. The 5.75 k collector current becomes β × 0.435 IC = β +1 where β is the increased value of 150, 150 IC = × 0.435 mA 151 = 0.432 mA Required: IC = 0.5 mA and VC = VE + 2. This indicates that the CG amplifier functions as an effective current buffer. From the solution to Problem 8.100, we know that I = 0.25 mA. Transistor a b c d e VBE (mV) 700 690 580 780 820 IC (mA) 1.000 1.000 0.230 10.10 73.95 IB (μA) 10 20 5 120 1050 IE (mA) 1.010 1.020 0.235 10.22 75 α 0.99 0.98 0.979 0.988 0.986 β 100 46 84 70 IS (A) 50 −16 6.9 × 10 −15 1.0 × 10 −14 1.9 × 10 −16 2.8 × 10 4.2 × 10−16 Chapter 4–3 C (b) The figure shows the circuit, where α= iC aiE 100 β = = 0.99 β + 1 101 5 × 10−15 IS = = 5.05 × 100−15 A α 0.99 The voltage at the emitter VE is ISE = iB B VE = −VDE v BE = −VT ln(IE /ISE) 2 × 10−3 = −0.025 ln 5.05 × 10−15 DE ISE IS /a iE = −0.668 V E a 0.99 ISE 6.98 1016 A The voltage at the collector VC is found from VC = 5 − IC × 2 = 5 − αIE × 2 = 5 − 0.99 × 2 × 2 = 1.04 V 4.16 Refer to the circuit in Fig. Indeed inserting the amplifier increases the gain by a factor 8.3/0.001 = 8300. The gain of the CS amplifier is | A| = gm RD where gm = Thus, 2μn Cox | A| = W L 2μn Cox ID CS W L ID RD (1) CS The gain of the differential amplifier is 8.14 (a) Ad = gm RD Ad = gm RD 20 = gm × 47 where 20 = 0.426 mA/V ⇒ gm = 47 2ID 2(I /2) I = = (b) gm = VOV VOV VOV I 0.426 = 0.2 ⇒ I = 0.085 mA = 85 μA (c) Across each RD the dc voltage is 0.085 I RD = × 47 = 2 V 2 2 (d) The peak sine-wave signal across each gate source is 5 mV, thus at each drain the peak sine wave is Ad × 5 = 20 × 5 = 100 mV = 0.1 V (e) The minimum voltage at each drain will be v Dmin = VDD − RD ID − Vpeak = VDD − 2 − 0.1 gm = Thus, 2μn Cox Ad = 2μn Cox I 2 diff I RD 2 diff (2) If all transistors have the same channel length, each of the differential pair transistors must be twice as wide as the transistor in the CS amplifier. C 0.1 μF 0 vO iR To increase the value of the output to 12 V = 8 V × 1.5, the value of R has to be increased by 1.5 times: 20 k × 1.5 = 30 k Chapter 2–28 ω0 (unity-gain frequency) = 103 rad/s 2.84 Vo At ω = 0.1 ω0 , = 0.1 V/V, φ = 270◦ V vI i Vo At ω = 10 ω0 , = 10 V/V, φ = 270◦ V 1V i 0 0.2 ms When a series input resistor R1 is added as shown, then the high-frequency gain is limited to R2 /R1 . P6.50. Writing expressions for the currents, we have ID = IS eVD /VT ID = IS e(VD −V)/VT = IS eVD /VT · e−V /V T 2 Taking the ratio of the above two equations, we have 2 = eV /V T ⇒ V = 17.3 mV To instead achieve V = 60 mV, we need I1 − I2 1 0.06/0.025 ID2 e = = = 1.1 ID1 I2 10 Solving the above equation with I1 still at 10 mA, we find I2 = 4.76 mA. P6.56, with the output current source expressed as Gm v i . 6.7 At sat/triode boundary v GS B = VGS + v̂ gs v DS B = VDS − v̂ o v̂ o = max downward amplitude , we get Point A occurs at VGS = Vt = 1 V, iD = 0 v̂ o Vt DS B = v GS B − Vt = VGS + − Vt | Av | Point A = (1 V, 5 V) (VGS , VDS) = VDS − v̂ o Point B occurs at sat/triode boundary (VGD = Vt) VOV + VGD = 1 V ⇒ VGS = [5 − iD RD] = 1 1 (1)(24) [VGS − 1]2 − 1 = 0 VGS − 5 + 2 2 − 23VGS + 6 = 0 12VGS VGS = 1.605 V iD = 0.183 mA VDS = 0.608 V Point B = (+1.61 V, 0.61 V) v̂ o = VDS − v̂ o | Av | VDS − VOV v̂ o = 1 + | A1v | (1) For VDD = 5 V, VOV = 0.5 V, and W k n = 1 mA/V2 , we use L −2(VDD − VDS) Av = VOV and Eq. (1) to obtain (b) For VOV = VGS −Vt = 0.5 V, we have VGS = 1.5 V 1 ID = k n (VGS − Vt)2 2 1 = × 1(1.5 − 1)2 2 ID = 0.125 mA VDS = +2.00 V v̂ o V v̂ i V DS Av IV −16 471 mV 29.4 mV 1.5 V −14 933 mV 66.7 mV −12 1385 mV 115 mV 2.5 V −10 1818 mV 182 mV 2V Point Q = (1.50 V, 2.00 V) Av = −k n VOV RD = −12 V/V For VDS = 1 V, Av = −16 = −k n VOV RD (c) From part (a) above, the maximum instantaneous input signal while the transistor ID RD = 4 V, ID = 0.125 mA ∴ RD = 32 k Chapter 6–3 solving the resulting quadratic equation results in 6.8 k n RD = 213.7 vDS which can be substituted into Eq. (2) to obtain VDS B = 0.212 V The value of VDS at the bias point can now be found from Eq. (1) as VDS Q = 0.212 + 0.5 = 0.712 V (b) The gain achieved can be found as Q VDSQ Av = −k n RD VOV = −213.7 × 0.2 = −42.7 V/V 0.5 0.5 v̂ gs = = 11.7 mV | Av | 42.7 0.5 V B VDSB VOV (c) ID = 100 μA v̂ gs Vt vGS VDSB To obtain maximum gain while allowing for a −0.5-V signal swing at the output, we bias the MOSFET at point Q where VDS Q = VDS B + 0.5 V (1) as indicated in the figure above. V R For I = 0.5 mA, the output will saturate at 0.5 mA ×10 k = 5 V. VDmin = VG − Vt = 5 − 1 = 4 V 0.72 μm W = 4.0 L 0.18 μm ID = 0.5 mA ⇒ RDmax = λ=0 10 − 4 = 12 k 0.5 VDD − VDmin ID Exercise 5–3 2.5 V Ex: 5.13 ID = 0.32 mA = 1 W 2 1 2 k n VOV = × 1 × VOV 2 L 2 QN ⇒ VOV = 0.8 V VGS = 0.8 + 1 = 1.8 V VI 2.5 V VO VG = VS + VGS = 1.6 + 1.8 = 3.4 V RG2 = 3.4 VG = 3.4 M I 1 μA RG1 = 5 − 3.4 = 1.6 M 1 μA RS = 10 k VS = 5 k 0.32 VD = 3.4 V, then RD = IDN = 5 − 3.4 = 5 k 0.32 RL = 1 k 1(2.5 − VO − 1)2 2 IDN = 0.5(1.5 − VO)2 Also: VO = RL IDN = 10IDN IDN = 0.5(1.5 − 10IDN)2 Ex: 5.14 2 ⇒ 100IDN − 32IDN + 2.25 = 0 ⇒ IDN 1.8 V = 0.104 mA RD IDP = 0, V O = 10 × 0.104 = 1.04V ID VO IDP QP 10 k -2.5 V Vtp = −0.4 V -2.5 V k p = 0.1 mA/V2 W 10 μm = ⇒ k p = 5.56 mA/V2 L 0.18 μm VSG = |Vtp | + |VOV | = 0.4 + 0.6 = 1 V VS = +1 V Since VDG = 0, the transistor is operating in saturation, and 1 2 ID = k p VOV = 1 mA 2 1.8 − 1 ∴ R= = 0.8 k = 800 1 Ex: 5.15 v I = 0: since the circuit is perfectly symmetrical, v O = 0 and therefore VGS = 0, which implies that the transistors are turned off and IDN = IDP = 0. To find the peak-to-peak amplitude of the square wave, we note that 4V/π = 441 mV. Thus the largest symmetrical Chapter 3–14 output signal allowed is 2.38 mV in amplitude. RE = (a) IE = VBB − VBE RB RE + β +1 RB = 5.73 × RE RE = 19.08 k VBB = VCC VBB − VBE IE nominal = RB RE + 101 IE high 2.46 = 5 VBB − VBE VBB − VBE = RB RB RE + RE + 101 51 RB /RE 101 0.95 = RB /RE 1+ 51 RB = = 5.73 RE R2 R1 + R2 R1 R2 = 5RB R1 + R2 = 5 × 19.08 high 1+ R2 R1 + R2 2.46R1 = 5 VBB − VBE = RB RE + 151 VBE − VBE IE low = RB RE + 51 Let's constrain IE low to be equal to IE nominal × 0.95 and then check IE : 0.95 VCC /3 5/3 = 3.33 k IE = 0.5 = R1 = 38.8 k 1 1 − = 37.5 k R2 = 1 RB R1 (d) VCE = VCC − RC IG 1 = 5 − RC × 0.99 × 0.5 = RC = 8.1 k Check design: VBB = VCC 37.5 R2 =5× R1 + R2 37.5 + 38.8 = 2.46 V RB = R1 R2 = 37.5 38.8 = 19.07 k Chapter 6–36 IE nominal = 2.46 − 0.7 = 0.5 mA 19.07 3.33 + 101 IE low = 2.46 − 0.7 = 0.475 mA 19.07 3.33 + 51 , and which is 5% lower than IE Thus, IC = 0.432 − 0.39 = 0.042 mA for a percentage increase of IC 0.042 × 100 = 10.8% IC 0.39 nominal IE 2.46 − 0.7 = 0.509 mA = high 19.07 3.33 + 151 . If in any design W/L is held constant while L is increased by a factor of 10, gm remains unchanged but ro increases by a factor of 10, resulting in A0 increasing by a factor of 10. Between the two collectors there will be a sine wave with 0.9 V peak amplitude. (c) I = P/V = 100 mW/10 V = 10 mA V = I /10 = 10 /10 = 1 k (d) V = P/I = 1 mW/0.1 mA = 10 V R = V /I = 10 V/0.1 mA = 100 k 1.6 VO = VDD R2 R1 + R2 To find RO , we short-circuit VDD and look back into node X, RO = R2 R1 = R1 R2 R1 + R2 Chapter 1–2 This figure belongs to 1.4. 10 10 10 40 46.7 20 20 20 10 40 20 30 40 10 10 40 50 20 6.7 20 40 60 10 10 40 20 70 10 40 40 8.0 10 13.3 20 40 8.6 40 14.3 20 17.1 10 20 20 5.7 10 40 20 40 10 40 23.3 10 10 20 40 1.7 Use voltage divider to find VO VO = 5 2 =2V 2+3 28 5 V 3 k Equivalent output resistance RO is VO RO = (2 k 3 k) = 1.2 k The extreme values of VO for ±5% tolerance resistor are VOmin = 5 2(1 − 0.05) 2(1 − 0.05) + 3(1 + 0.05) 2 k RO = 1.88 V VOmax = 5 × 2.12 V 2(1 + 0.05) 2(1 + 0.05) + 3(1 − 0.05) The extreme values of RO for ±5% tolerance resistors are 1.2 × 1.05 = 1.26 k and 1.2 × 0.95 = 1.14 k. P7.51. 1.97 Equation (1.75): 2L2p 10 × 10−4 = τp = Dp 10 −4 (Note: 1 μm = 10 Find current component Ip : pn (xn) = pn0 eV /V T and pn0 = cm.) τp = 100 ns Ip = Aq DpP ∗ p Ip (Eq. 1.76) p2i ND dp dx dp pn (xn) − pn0 pn0 eV/V T − pn0 = = dx Wn − xn Wn − xn V /V e T −1 = pn0 Wn − xn 2 eV /V T − 1 ni = ND (Wn − xn) = 100 × 10−6 × 0.1 × 10−3 = 10 × 10−12 C τp I Cd = VT 100 × 10−9 = × 0.1 × 10−3 = 0.1 × 10−3 25.9 × 10−3 ∴ Ip = Aqn2i 1.98 Equation (1.81): τT I Cd = VT τT × 1 × 10−3 5 pF = 25.9 × 10−3 dp dx Dp × eV /V T − 1 (Wn − xn)ND Similarly, Dn × eV /V T − 1 (Wp − xp NA In = Aqn2i I = Ip + In τ T = Dn 50 × 10−12 = 25.9 Dp Dn + (Wn − xn) ND Wp − xp NA × eV /V T − 1 Aqn2i 129.5 ps For I = 0.1 mA: τT ×I Cd = VT 129.5 × 10−12 × 0.1 × 10−3 = 0.5 pF 25.9 × 10−3 The excess charge, Qp , can be obtained by multiplying the area of the shaded triangle of the pn (x) distribution graph by Aq. 1.99 (a) pn, np n region p region pn(xn) pn(xn) np (xp) np (xp) pn0 np0 Wp xp 0 xn Depletion region Widths of p and n regions Wn Chapter 1–33 Qp = Aq × 1 [pn (xn) − pn0] (Wn − xn) 2 Thus, τT = 1 Wn2 , and 2 Dp = 1 Aq pn0 eV /V T − pn0 (Wn − xn) 2 = 1 Aqpn0 eV /V T − 1 (Wn − xn) 2 dQ dI = τT dV dV V /V But I = IS e T −1 = ni 2 1 Aq ND IS eV /V T dV = dV VT ni 2 VT = 1 (Wn − xn)2 · Ip 2 Dp I so Cd ∼ . Fig. THE OXFORD SERIES IN ELECTRICAL AND COMPUTER ENGINEERING A d e l S. Correspondingly, the voltage across each diode changes by VD where = 8 = eVD /VT 13 8 ⇒ VD = 25 ln = −12.1 mV 13 = 7.38 mA = 8.39 mA ∴R= 5 − 1.5 = 417 8.39 mA Use a small-signal model to find voltage VO when the value of the load resistor, RL , changes: rd = VT 0.025 = 3.4 = ID 7.39 When load is disconnected, all the current I flows through the diode. v D1 = −2.5 + 0.5 × 4 = −0.5 V Observe that since v G1 = v D1 , Q1 is still operating in saturation, as implicitly assumed. The load current iL comes from the power supply of the op amp. vO 10 V 5 V = C = 868 μF To specify the diodes, we determine iDav and iDmax , iDav = IL (1 + π (Vp − 0.7)/2 Vr) = 1(1 + π 12.5/2) = 785 mA 0 vI 5 V 1 ms t Chapter 3–33 Thus, v O is a square wave with 0-V and +10-V levels, i.e. 5-V average and, of course, the same frequency (1 kHz) as the input. The transistor continues to operate in the saturation region until v G reaches 0.5 V, at which point v DG will be 0.5 V, which is equal to |Vtp |, and the transistor enters the triode region. Therefore, v o = v i − R × 0.5 mA = 0 − 10 k × 0.5 mA = −5 V. Thus, to obtain a dc level shift of 0.9 V, we write = (58.5 250) + 4000 + 0.4 × 4000 × (58.5 250) VGS = 0.9 V = Vt + VOV = 79.9 M = VOV = 0.9 − 0.6 = 0.3 V 7.87 Refer to the circuit in Fig. The gain of the first stage will be v o1 = vi d α × Total resistance between the collectors of Q1 and Q2 Total resistance in emitters of Q1 and Q2 40 k 10k = 20 V/V 2 × 0.1 = 2 × 0.1 Thus the gain of the first stage decreases but only slightly. Thus, vO = It − 10 C 10−5 t − 10 t = − 10, V 10 × 10−6 vO Chapter 2–24 Thus V O will reach 0 V at t = 10 s and will reach 10 V at t = 20 s See figure below. However, each of the two diodes conducts for only half the time, i.e., for 48.4% of the cycle. 2.5 V t (V) Vp+ = 5 V, Vp− = −2.5 V, vO 5V Vp+ = 5 V, Vp− = 0 V, f = 1 kHz When I > 0, the output follows the input as D1 is conducting. Thus VG = 0.25 + VGS2 = 0.25 + VOV 2 + Vt = 0.25 + 0.25 + 0.5 = 1.0 V 2 C 4 R2 = 1.6 M 0.1 A To obtain the W/L values, 1 W |VOV |2 I = ID = μp Cox 2 L 3,4 1 W 100 = × 100 × × 0.22 2 L 3,4 W = 50 L 3,4 (b) I = 0.5 mA 2 × 42 = 160 0.2 Ro = 320 k W 1 |VOV |2 I = μp Cox 2 L 3,4 W 1 500 = × 100 × |VOV |2 2 L 3,4 W = 250 L 3,4 0.5Ro = 7.60 Refer to Fig. Ro = ∞ (because iL is independent of the value of RL). The result is as follows: 60 50 40 Ro1 20 dB/decade 20 dB/decade 30 20 vo1 C 10 Ri2 0 1 Ro2 Rin2 10 Ro1 Ro2 = 100 k. If we choose 5.1 k, the gain will be vo = −0.385 × 73.4 × (5.1 2) = −40.6 V/V v sig (2) × 2 − 0.95 × 0.22RC = 5 − 0.22RC | Av o | = gm RC = 0.99 × 0.22 RC = 8.7RC 0.025 and VB = −0.22 × 90 = −0.2 V 101 Thus, 5 − 0.22RC − 8.7RC 0.0025 = −0.2 ⇒ −0.395 Chapter 6–46 8 100 = 5 k gm 20 vo G v = = − × 20 × (5 2) 0.5 v sig 2 + 2.5 ⇒ RC = 21.2 k rπ = Selecting 5% resistors, we find RB = 91 k RC = 22 k and specifying I to one significant digit gives I = 0.2 mA αIC 0.2 gm = = 8 mA/V VT 0.025 Av o = −gm RC = −8 × 22 = −176 V/V β 100 = 12.5 k rπ = gm 8 Rin = RB rπ = 91 12.5 = 11 k 11 × 8(22 20) Gv = − ≈ 11 + 1 = −29.7 V/V ≈ −44.4 V/V 6.119 Refer to the circuit of Fig. (d) Rin = rπ 1 = 5 k 10 k rod ro2 = 120 k 120 k = 60 k 7.49 Refer to Fig. The common-mode gain, however, will be lower: ro4 Acm = − β3 REE But = 800 = 6.45 × 10−3 V/V 100 × 1240 and the CMRR will be 2000 | Ad | = 3.1 × 105 = CMRR = | Acm | 6.45 × 10−3 or 110 dB 8.102 Gm = gm1,2 1 = 1 2 k (W/L)VOV 2 n 1 2 2 × 2 × 0.7 × 2VOV 144 VOV 2 Av = 144 V/V = VOV − 18.6 = 0 ⇒ VOV = 0.35 V and I /2 (0.2) 2 = 8 mA/V = VT VOV 0.35 = 0.12 mA (a) Rid = 2rπ = 2β/gm Ro = ro2 ro4 where |VA | 40 ro2 = ro4 = = 200 k I /2 0.2 gm = gm1,2 I /2 0.026 = 2.4 mA VT 0.025 Chapter 8–37 2 × 100 = 83.3 k 2.4 (b) Ad = gm1,2 Ro Rid = ro2 = ro4 = 60 |VA | = = 60 k I /2 1 Ro = 60 60 = 30 k where Ad = 40 × 30 = 1200 V/V Ro = ro2 ro4 (c) Acm can be found using Eq. (8.165), ro4 Acm = − β3 REE But ro2 = ro4 = |VA | 60 = = 500 k I /2 0.06 Ro = 500 k where |VA | 60 = = 30 k I 2 0.06 = −0.02 V/V = − 100 × 30 REE = ro5 = Ad = 2.4 × 500 = 1200 V/V (c) Acm can be found from Eq. (8.165): ro4 Acm = − β3 REE Acm where REE is the output resistance of the Wilson mirror, or 95.6 dB REE = gm7 ro7 ro5 1200 | Ad | = = 60, 000 | Acm | 0.02 CMRR = 8.105 Refer to Fig. However, the unequal β's will mean unequal α's. (c) Since the input offset voltage is proportional to |VOV 1,2 |, it will decrease by a factor of 2. Thus VD = 770 mV. Also, the output signal of the amplifier loses approximately 90% of its strength when the load is connected (because RL = Ro /10). Thus in (T /2) seconds, the capacitor voltage changes by 20 V. 8.33 gm = IC α 0.2 = 8 mA/V VT 0.025 Rid = 2rπ = 2β 160 = 40 k =2× gm 8 8.34 Rid = 2rπ = 20 k = 2 × 0.025 × 10 = 0.5 mA Input signal to half-circuit = 5 mV. Now I = 1 mA. R2 R2 R1 + R1a R1 + R1 R1a R1 R1a = |G| = R2 R2 R1 + R1 R1 1 + R2 R1 1 + A A R2 , use To restore the gain to its nominal value of R1 R1 = R1a So R1a R1a 1 + A R2 R1 = 100 (1.1% 10%) 1000R1 100R1 2.23 Refer to Fig. 7.41(a) with its T model results in the circuit in the figure. IE I2 = I1 + IB = I1 + β + 1 IC = 10−15 ev BE /VT A Intercept (mA) VBE = 0.68 V IE = I − I1 = 1.1 − 0.1 = 1 mA To find the intercept of the straight-line characteristics on the ic axis, we substitute v C = 0 and evaluate v BE (V) 0.65 VE 1 1.1 mA with IS = 10−15 A and VA = 100 V, to get v CE iC = 10−15 ev BE /0.025 1 + 100 vCE IE 10 0.72 0.73 0.74 1.45 3.22 4.80 7.16 Slope (mA/V) 0.002 0.015 0.032 0.048 0.072 I1 R1 = VBE I2 R2 I1 R2 = VBE R2 R1 = VCE = −(I1 R1 + I2 R2) R2 (1) = −VBE 1 + R1 6.8 = −11 VBE = −7.48 V = −VBE 1 + 0.68 which gives this circuit the name "VBE multiplier." A more accurate value of VE can be obtained by taking IB into account: VE = −(I1 R1 + I2 R2) R2 = − VBE + VBE + IB R2 R1 R2 VBE − IB R2 = − 1 + R1 (2) = −7.48 − 0.01 × 68 = −8.16 V As temperature increases, an approximate estimate for the temperature coefficient of VE can be obtained by assuming that IE remains constant and ignoring the temperature variation of β. Chapter 1–28 (b) nn ≈ ND = 5 × 1016 cm−3 ; pn = n2i = 4.5 × 103 cm−3 nn 10 μm Using μn = 1200 cm2 /V · s and 3 V μp = 400 cm2 /V · s, we have ρ = 0.10 -cm; R = 3.33 k. iB E C vBE ve ib = −gm v be re 1 = v be − gm re Since α = gm re α 1−α = gm v be α gm v be = β v be β = = rπ Rin ≡ ib gm B Rin ro bib DB (ISB IS) b biB E Figure 1 For vBE undergoing an incremental change v be from its equilibrium value of VBE , the current iB Chapter 6–15 C changes from IB by an increment ib , which is related to v be by the incremental resistance of DB at the bias current IB . The peak diode current occurs at the peak diode voltage. 2.28 and observe that R v+ − v− = VOS + v2 − v1 1 = VOS + vI Vd Vi C Vo and since V O = v 3 = A(v + − v −), then v O = A(v Id + VOS) C = 0.01 μF is the input capacitance of this differentiator. 4.21. Thus, for equivalence, we write Av o Gm = Ro Thus, Rin vo = Gm (Ro RL) v sig Rin + Rsig These figures belong to Problem 6.56. This the cascode transistor must have A0 = 100. Thus VD − 1 = v Dmin = VG − Vt = 0 − 1 V = 0 V VS = ID RS = 3.5 ID VDD = 3 ID RD = VGS = VGS − 1 + 5 = (VGS − 1) 2 1 + 2(5 − 3ID − 1)2 = 16 − 24ID + 9ID2 9ID2 − 25I + 16 = 0 We can now assume that the signal voltage at the gate is small. We just saw that 0.5 V 2 appears at the input of the v 2 transconductance amplifier. vi vi RG1 2 M Rin vgs 0.5 + 2.375 − 0.95 1 1+ |Av | Substituting |Av | = 86.5, we obtain |v̂ o | = 1 + |Av | An approximate value of |v̂ o | could have been obtained from vOmin = VOV = 0.45 V VDS − |v̂ o | = VOV vovi RG2 gmvgs ro vo vgs vi Figure 2 A node equation at the output node yields vo − vi vo + gm vgs + = 0 ro RG2 vi − Chapter 5–1 13 For RL = 10 k , when signal source generates 0−0.5 mA, a voltage of 0−2 V may appear across the source (b) Same procedure is used for (b) to obtain 0.5 k 2 0.75 V 3 is 00.5 mA RL vs (c) Between terminals 1 and 3, the open-circuit voltage is 1.5 V. 6.59. Assuming saturation-mode operation, the terminal voltages are interrelated as shown in the figure, which corresponds to Fig. Assuming that D1 and D2 are both conducting gives the results shown in Fig. Rsig 200 k vsig vgs1 gm1vgs1 Gv = gm2vgs2 RD2 R L vo v gs2 vo v gs1 v gs2 (b) β = 50, | Gv | = −gm1 RD1 × −gm2 (RD2 RL) 10 (10/50) + 0.025 = 44.4 V/V = 3 × 10 3 × (10 10) β = 150, | Gv | = 450 V/V 10 (10/150) + 0.025 = 109.1 V/V IC 0.5 mA gm = 20 mA/V = 6.63 gm = VT 0.025 V β 100 rπ = = 5 k = gm 20 mA/V Rin = rπ = 5 k Ro = RC = 10 k Avo = −gm RC = −20 × 10 = −200 V/V RL 10 = −200 × RL + Ro 10 + 10 = −100 V/V Rin Gv = Av Rin + Rsig Av = Av o 5 × −100 5 + 10 = −33.3 V/V = For v̂ π = 5 mV, v̂ sig can be found from v̂ π = v̂ sig Rin Rin + Rsig 5 + 10 = v̂ sig = 15 mV Correspondingly, v̂ o will be v̂ o = Gvv̂ sig = 15 × 33.3 = 500 mV = 0.5 V 6.64 | Gv | = RL (Rsig β) + (1/gm) RL = 10 k, Rsig = 10 k, gm = IC VT 1 = 40 mA/V 0.025 Nominal β = 100 ⇒ 10 (a) | Gv | = (10/100) + 0.025 = 80 V/V Thus, | Gv | ranges from 44.4 V/V to 109.1 V/V. For Gnominal = −100 and α = 1, the closed-loop gain will be in the range −98 V/V to −102 V/V. 5 V 0.5 mA V0.5 mA 1 mA R3 R2 R5 V4 0 V7 1 V Q2 V3 = 0 (1) 0.5 mA V2 Q3 R1 V5 = −2 V R4 0.5 mA V6 R6 1 mA −5 V Figure 1 This figure belongs to Problem 4.59. The charge equilibrium equation can be expressed as i(T /2) = C × 20 V vO = 1 + v × (op amp A3) v I 1 + v (op amp A3) = 10.01 sin ωt V vI = 1(1 + 1000) × 0.01 sin ωt R Vi = (2.5 + 2.5025 sin ωt) V R4 R2 1 + v Id vO = R3 R1 0.5 V 10 k 1+ 1000 20 k 1 V 0.5 k C Vo For the circuit in the figure, the input resistance of this inverting integrator is R; therefore, R = 10 k. Thus v O = v I . Thus at the limit VDG = −0.5 V, we can determine VOV : 1 2 × 2 × VOV 2 = VOV = 0.45 V 0.2 = vGmax = 0.5 + vDmin VGS + |v̂ i | = 0.5 + VDS − |v̂ o | = VOV + Vt + VOV = 0.45 + 0.45 = 0.95 V The current in the feedback network can now be found as VGS 0.95 = 0.475 μA IR = 2 M 2 which indeed is much smaller than the 200 μA delivered by the current source. Sedra and Kenneth C. 9.10 can be used to determine the three short-circuit time constants, again with RE = ∞. At f = 60 kHz, | A| = 3 MHz = 50 V/V 60 kHz or 34 dB = 1+ R2 R1 2 MHz = 20 kHz 100 Ex: 2.29 For the input voltage step of magnitude V the output waveform will be given by the exponential waveform of Eq. (2.58) if ωt V ≤ SR SR SR ⇒ V ≤ resulting in that is, V ≤ ωt 2πft V 0.16 V Ex: 2.27 From Appendix F we know that the 10% to 90% rise time of the output waveform of the form of 2.2 . (b) The upper limit of VICM is determined by the need to keep Q1 and Q2 in saturation, thus 1 W μn Cox V2 2 L 1,2 OV W 1 100 = × 400 × × 0.04 2 L 1,2 W W = = 125 L 1 L 2 1 W |VOV |2 ID3 = ID4 = 100 = μp Cox 2 L 3,4 1 W 100 = × 100 × × 0.04 2 L 3,4 W W = = 50 L 3 L 4 8.106 (a) ID1 = ID2 = 100 = ID5 = ID7 = ID8 = 200 μA VICM max = VD1 + Vt = VDD − |VSG4 | + Vt = 0.9 − |Vt | − |VOV 4 | + Vt = 0.9 − 0.2 = +0.7 V The lower limit of VICM is determined by the need to keep Q5 in saturation, VICM min = −0.9 + |VOV 5 | + |VGS1 | = −0.9 + 0.2 + 0.2 + 0.4 = −0.1 V Thus −0.1 V ≤ VICM ≤ +0.7 V (c) Vmax = VDD − |VOV 6| = 0.9 − 0.2 = +0.7 V Chapter 8–39 Omin = −VSS + |VOV 7 | = IREF = −0.9 + 0.2 = −0.7 V (48.0.8) (40/0.8) = 90 × 1.2 = 108 μA Thus −0.7 V ≤ v O ≤ +0.7 V Thus ID7 will exceed ID6 by 18 μA, which will result in a systematic offset voltage, (d) A1 = −gm1,2 (ro2 ro4) VO = 18 μA(ro6 ro7) where where 2 × 0.1 gm1,2 = = 1 mA/V 0.2 6 |VA | ro2 = ro4 = = 60 k 0.1 ro6 = 111 k and ro7 how becomes 10 = 92.6 k 0.108 A1 = −1 × (60 60) = −30 V/V ro7 = A2 = −gm6 (ro6 ro7) Thus where VO = 18 × 10−3 × (111 92.6) 2 × 0.2 = 2 mA/V 0.2 6 |VA | = = 30 k ro6 = ro7 = Vp = 0.2 0.2 = 909 mV gm6 = The corresponding input offset voltage will be VOS = A2 = −2 × (30 30) = −30 V/V A0 = A1 A2 = 30 × 30 = 900 V/V = 8.107 (a) Increasing (W/L)1 and (W/L)2 by a factor of 4 reduces |VOV 1,2 | by a factor of 2. v d = (Gm v 2 − Gm v 1) = Gm R(v 2 − v 1) Exercise 2–2 R Gm R1 10 k vi 0.5 mA Rf v1 vo Rf v2 Ex: 2.7 v2 vO Correspondingly, the signal source shown in Fig. The voltage v e can be found in terms of ib as v e = ib re = −βib RE . Thus v O = v I is satisfied. v b = ib rπ + (β + 1)ib RE Thus, v b = ib [rπ + (β + 1)RE]ib (2) Dividing Eq. (1) by Eq. (2) yields βRL vc = − vb rπ + (β + 1)RE Av = vo 10(2/4) = vi 1 × 10−6 × (200 5) × 103 Q.E.D The voltage v e is related to ib by v e = (β + 1)ib RE 1025 V/V or 60.2 dB Ai = io v o /RL = ii v i /Ri vo Ri 5 k = 1025 × v i RL 2 k = 2562.5 A/A or 62.8 dB That is, v e = [(β + 1)RE]ib Dividing Eq. (3) by Eq. (2) yields ve (β + 1)RE = vb (β + 1)RE + rπ (3) Chapter 1–21 amplifier circuit. The resulting dc offset voltage at the output will be therefore from Eq. (2.40): VO = IOS × R2 = IOS = 0.6 10 M VO = IOS R2 = 0.2 × 100 = 20 mV Since IOS can be of either polarity, IOS = −60 nA VO = ±20 mV The same result could have been found by replacing R3 in Eq. (1) by (R3 + R4) where R4 = 5 k. P6.117. 6.2(a) and 6.2(b). An equal positive swing is possible. Thus RG2 is the larger of the two resistances, and we select RG2 = 22 M and find RG1 from RG1 = 1.2 RG2 = 20.3 M ⇒ RG1 1.3 Specifying all resistors to two significant digits, we have RD = 2.5 k, RG1 = 22 M, and RG1 = 20 M. At v O = 3.7 V, the diode is conducting i = 1 mA and thus v I = v O + i × 1 k = 4.7 V For v I > 4.7 V the diode current increases but the diode voltage remains constant at 0.7 V, thus v O flattens and v O vs. 4.27: IB = Ex: 4.30 15 V 5 − 0.7 = 0.043 mA 100 To ensure that the transistor remains in the active mode for β in the range 50 to 150, we need to select RC so that for the highest collector current possible, the BJT reaches the edge of saturation, that is, VCE = 0.3 V. This figure belongs to Problem 1.45. (b) G = − R2 /R1 1 + R2 /R1 1 + A = −100 = −192.3 V/V = − 1 + 200 1+ 5000 To restore the gain to −200 V/V, we need to change the effective value of R1 to R1 , −200 = −200/R1 1 + 200/R1 1 + 5000 Rm = −0.2 200 R1 = 0.96 k = 200 ∞ 1 + 5000 R1 = 0.96 k R1 = 1 k To restore the gain to −200 V/V, we need to change the effective value of R1 to R1 , −200 = −200/R1 1 + 200/R1 1 + 5000 R1 = 0.960 k This effective value can be realized by shunting R1 (1 k) with Ra , 1 1 1 + = Ra = 24 k 0.960 1 Ra (c) From Appendix J, we find the closest available 1% resistor as either 23.7 k or 24.3 k. We want CR = 10−2 s (the time constant of the differentiator); thus, R= 10−2 = 1 M 0.01 μF From Eq. (2.33), the transfer function of the differentiator is Vo (jω) = −jωCR Vi (jω) Thus, for ω = 10 rad/s the differentiator transfer function has magnitude Vo = 10 × 10−2 = 0.1 V/V V i and phase φ = −90◦ . Thus 1 W 2 VOV IREF = μn Cox 2 L 1 2 × 400 × 10 × VOV 2 = VOV = 0.3 V 180 = 2 vx = (i3 /gm3) + (i1 /gm1) 1 gm3 1 i2 1 gm1 VG3 = Vtn + VOV = 0.5 + 0.3 = 0.8 V (b) Q1 is operating at VDS = VGS = 0.8 V Q2 is operating at VDS = 2VGS = 1.6 V Thus, IREF − IO = VDS ro where Rin Here, we have applied a test voltage vx to determine Rin , vx Rin ≡ ix Since all three transistors are identical and are operating at the same ID , gm1 = gm2 = gm3 Note from the figure we see that i1 = ix and i2 = i3 Thus vx = i1 = ix i2 ix 2 A node equation at node 2 gives ix = i3 + i2 = 2i3 ⇒ i3 = VA 18 = 100 IO = 180 − 180 = 172 μA ro = IREF 0.18 = 0.008 ro is gm1 2 gm = 2 × ID 2 × 0.18 = 1.2 mA/V VOV 0.3 Since fP2 then, 87.5 Hz Figure 2 Observe that the dc gain is 6 dB, i.e. 2 V/V. R1 R3 R4 R2 = 0.99 R1 R3 Now for this case, Acm can be found from Eq. (2.19) R v 2 only: Ri = 0V v2 = 2R I R Chapter 2–17 R Since R vO R2 R4 = : R1 R3 Rs Rs +1= + 1 = R1 R3 = R2 R4 R1 R3 2.60 I v2 R R2 R I v1 between 2 terminals: v Ri = 2R I R1 vO vicm R Ricm i2 R 0V vR3 R4 vO I R R When R2 /R1 = R4 /R3 , the output voltage v O will be zero. and substitute Y1 = (1/R1) + sC1 and Y2 = (1/R2) + sC2 to obtain C1 = C1 + C2 R1 1+ R2 10 log 1+ (1) R1 C2 =1+ C1 R2 1000 10, 000 2 ω = −0.04 dB The gain drops by 3 dB at the corner frequencies of the two STC networks, that is, at f = 10 Hz and f = 10 kHz. or 1.74 Use the expression in Eq. (1.2), with C1 R1 = C2 R2 B = 7.3 × 1015 cm−3 K −3/2 ; When this condition applies, the attenuator is said to be compensated, and its transfer function is given by k = 8.62 ×10−5 eV/K; and Eg = 1.12 V Vo C1 = Vi C1 + C2 we have T = −55◦ C = 218 K: Chapter 1–27 ni = 2.68 × 106 cm−3 ; N = 1.9 × 1016 ni That is, one out of every 1.9 × 1016 silicon atoms is ionized at this temperature. Input needed is 14 mVrms . 6.3 Bias point Q: VOV = 0.2 V and VDS = 1 V. Thus the condition in (a) above is not satisfied and the MOSFET is operating in the triode region. Now making the assumption that D1 is off and D2 is on, we obtain the results shown in Fig. Therefore, we shall use the first design. P7.54. P7.5. we obtain For I3 = 40 μA = 2IREF , we obtain (W/L)3 =2 (W/L)1 W = = 20 L 1 W3 = 10 μm We next consider Q4 and Q5 . For the given data, re = IC1 β VT 25 mV = 250 = IE 0.1 mA This figure belongs to Problem 7.20, part (b). 2 on the next page. Also because all have equal |VA | = 4 V, all ro 's will be equal. To obtain the largest possible signal swing at the output, we maximize the allowable positive signal swing by setting VD4 at its highest possible value of VDD − |VOV | = 3.3 − 0.2 = 3.1 V. That is Ro = 0 . Since VAn the channel lengths are equal, VAn = |VAp | and ron = rop ro = ro ∴ gm1 = gm2 = 2 × 0.4 × 25 × 0.1 1.41 mA/V 1.8 VA ro1 = ro2 = = 18 k 0.1 ...

10−5 or 146 dB 8.104 Refer to Fig. P5.52(e) with the Chapter 5–15 1-mA current source replaced with a 2.2-k resistor. We can write a loop equation for the loop containing the 10-k resistor, the EBJ of Q2 and the 1-k resistor: −IE × 1 − 0.7 − IB × 10 = −5 Substituting IB = IE /(β + 1) = IE /101 and rearranging gives IE = 5 − 0.7 = 3.9 mA 10 + 1 101 Q1 will be saturated 7.27. Since, for a fixed diode current, the diode voltage changes with temperature at a constant rate (−2 mV per ◦C temp. Thus V4 = VGSN = 1.232 V ID2 = ID3 = 10 ID1 = 10 × 562.5 μA VGSN = 1.232 V I3 = 1 × 270 × X 0.7322 = 217 μA 2 1 (c) Refer to Fig. P5.53(b). Obviously ID and |VOV| will be the same as in (i) above. For Q1 , ID = 0.5 × = 1 W1 2 μn Cox V 2 L1 OV 1 W1 × 16 = 0.25 × 4 μm For Q2 , we have 1 W2 2 ID = μn Cox VOV 2 L2 = ID = 1 W2 μn Cox (VGS2 − Vt)2 L2 90 = W2 1 × 90 × (1.5 − 0.8 − 0.5)2 2 L2 W2 = 50 × 0.5 = 25 μm For Q3 , ID = 1 W3 μn Cox VOV 3 2 L3 1 W3 × 90 × (2.5 − 1.5 − 0.5)2 L3 = W3 ...

[illegible]

junction areas. V DS 2V ⇒ IO = = 0.025 mA ro = I O 80 k Ex: 5.7 5 V 1 W 2 k V in saturation 2 n L OV Change in ID is: Ex: 5.3 ID = VG ID (a) double L, 0.5 VD (b) double W , 2 (c) double VOV , 22 = 4 Vtp = −1 V (d) double VDS , no change (ignoring length modulation) k p = 60 μA/V2 (e) changes (a)–(d), 4 W = 10 ⇒ k p = 600 μA/V2 L (a) Conduction occurs for VSG ≥ |Vtp | = 1 V Case (c) would cause leaving saturation if VDS < 2VOV Ex: 5.4 For saturation v DS ≥ VOV , so VDS must be changed to 2VOV ID = 1 W 2 k V , so ID increases by a factor of 4. (a) Ie = See Fig. 1 we see that ID1 0.1 mA/V But ID1 = 1 W 2 μn Cox VOV 2 L 1 2 0.1 = × 2 × VOV 2 ⇒ VOV = 0.316 V VGS = Vt + VOV = 1.316 V Rin vo = × Av vsig Rin + Rsig vo 487 × −19.5 = vsig 487 + 500 = −9.6 V/V (e) The suggested configuration, shown partially in Fig. Equation (2.19) can be employed to evaluate the worst-case common-mode gain. 1.5 V R RL ≤ 2 k. v D1 = v D2 = VDD − iD1,2 RD v D2 = VDD − iD2 RD = 1 − 0.08 × 5 = 0.6 V =1−0×5=1V v D2 − v D1 = 0 V (b) For iD1 = 0.12 mA and iD2 = 0.04 mA, 1 W (v GS2 − Vtn)2 iD2 = μn Cox 2 L 0.04 = 1 × 0.4 × 10 × (v GS2 − 0.4)2 2 ⇒ v GS2 = 0.541 V Thus, v S = −0.541 V 1 W (v GS1 − Vtn)2 iD1 = μn Cox 2 L 0.12 = 1 × 0.4 × 10 (v id − v S − Vtn)2 2 1 = × 0.4 × 10 (v id + 0.541 − 0.4)2 2 v D2 − v D1 = 1 − 0.2 = 0.8 V (d) iD1 = 0.04 mA and iD2 = 0.12 mA. Therefore: W ratio must stay L W is kept at 10) L VA = ro iD = 100 k × 0.2 mA = 20 V (for the standard device) W = 5 × 10 = 50 μm (so VA = 5 × 20 = 100 V (for the new device) 5.30 L = 1.5 μm = 3× minimum. To determine Rin , we have applied a test voltage vx . So v O = 0 and v D = v I − v O = v I . For VD Vs , conduction angle π, and v O,avg = vO vS vS 2 2 Vs − VD = Vs − 0.7 π π (a) For v O,avg = 10 V π × 10.7 = 16.8 V 2 √ 120 2 = 10.1 to 1 Turns ratio = 16.8 D4 R D2 Vs = (b) For v O,avg = 100 V π × 100.7 = 158.2 V 2 √ 120 2 = 1.072 to 1 Turns ratio = 158.2 Vs = 3.70 Refer to Fig. Since the collector is connected to the base with a 10-k resistor and β is assumed to be very high, the voltage drop across the 10-k resistor will be close to zero and the base voltage will be equal to that of the collector: I5 = IE = VB = V7 This also implies active-mode operation. P5.22. This can be achieved by shunting the input of the v 1 transconductance Chapter 1–18 This figure belongs to Problem 1.53. Thus 0.1 0.1 IO1 = = = 0.0999 mA 2 2 1+ 2 1+ 2 β 50 1 Rin ie2 re2 ie1 re1 Note that the diode-connected transistor Q1 reduces to a resistance re1 . Here v O = v I for v I ≥ 2.5 V. vO (a) v I = +1 V (c) See figure (c) on next page. i1 i1 2i1 i1 R1 0 R2 vId vG 0 RG 2i1 i1 R2 R RG 2 2i1 R2 R1 2i1 R2 RG R2 RG vO R2 R2 i1 i1 2i1 Substituting for 2i1 from Eq. (1), we obtain the gain as R2 R2 vO 1+ Q.E.D. = −2 v Id R1 RG R2 RG The circuit on the left ideally has infinite input resistance (iii) vO = +2 V/V vi R2 = 1. (1) and (2) and using 2 2 = VOVP : μn Cox = 3μp Cox gives 3VOVN √ ID2 = ID1 = = 1 W 2 μp Cox VOVP 2 L |VOVP | = 5 = 2.5 V 2 3 VOVN 1 W μn Cox (VGS1 − Vt)2 2 L 1 10 × 50 × (2.5 − 1)2 2 1 = 562.5 μA Now, Q3 has the same VGS at Q1 and is matched to Q1 . Thus ID = 1 2 k n VOV 2 10 = 1 2 × 500 × VOV ⇒ VOV = 0.2 V 2 ⇒ |VOV | = 1 V VGS = Vt + VOV = 0.8 + 0.2 = 1 V VSG = |Vt | + |VOV | = 1 + 1 = 2 V V1 = 0 − VGS = −1 V V4 = VSG = 2 V (b) Refer to Fig. P5.55(a). Using superposition: 100 kΩ vI1 v O = v O1 + v O2 100 kΩ 10 kΩ vI2 Calculate v O1 : v + = A vO 100 kΩ 10 kΩ βv O1 = v− 2 βv O1 βυ O1 − vO v1 2 = 2 ⇒ v O1 = R R β −1 B v1 − 100 kΩ Calculate v O2 : v O2 v O2 v O2 = v+ ⇒ v2 − = − βv O2 2 2 2 v2 ⇒ v O2 = 1−β v− = Applying Thévenin's theorem to v I 1 together with the associated (100-k, 10-k) voltage divider, and similarly to v I 2 and the associated (100-k, 10-k) voltage divider, we obtain the following circuit: 100 k (1011) v (1011) v I2 (100 // 10) k = vO v1 v2 + β −1 1−β 1 (v 2 − v 1) 1−β Ad = (100 // 10) k I1 v O = v O1 + v O2 = vO 1 = v2 − v1 1−β Ad = 10 V/V ⇒ β = 0.9 = Q.E.D R6 R5 + R6 RId = 2R = 2 M ⇒ R = 1 M R5 + R6 ≤ 100 k R ⇒ R5 + R6 ≤ 10 k 100 Selecting R6 = 6.8 k vO = 100 k (100 10) k 10 10 vI2 − vI1 11 11 = 10(v I 2 − v I 1) 6.8 = 0.9 ⇒ R5 = 756 6.8 + R5 For v I 1 = v I 2 = v Icm , v O = 0, thus 2.66 See partial analysis on circuit diagram on next page. Rin Gv = − gm (RD RL ro) Rin + Rsig =− RG gm (RD RL ro) RG + Rsig 10 × 3 × (10 20 100) 10 + 1 = −17 V/V =− 6.108 (a) Refer to Fig. Thus it is not a good method for biasing the BJT. Thus x 1 Rs 100 ≤ x −1= x Ri 1− 1− 100 100 A0 x (Ro RL) 1− 100 Gm ≥ which can be expressed as (5) Substituting Rs = 10 k and x = 10% in (3) results in 100 Ri ≥ 10 − 1 = 90 k 100 x 1− Ri 100 ≥ x Rs 100 resulting in Substituting f3dB = 2 MHz, CL = 20 pF, and RL = 10 k in Eq. (4) results in Rs V s 1 1 + ≥ 2πCL f3dB RL Ro Bandwidth = 159 kHz – 14.5 Hz 159 kHz Ri 1.71 Vi = Vs Rs + Ri 1 2πCL To obtain a value for f0 greater than a specified value f3dB we select Ro so that 1 1 1 + ≥ f3dB 2πCL RL Ro 59.2 dB 14.5 Hz 1 1 1 ω0 = 2π 2π CL (RL Ro) Thus, f0 = 20 dB/decade (3) (b) The 3-dB frequency is determined by the parallel RC circuit at the output 1 = 14.5 Hz 2π100 × 10−9 × 110 × 103 ∴ T (s) = Ti (s)To (s) = 100 −1 x Vi Ri Ro Gm Vi RL Vo CL Ro ≤ 1 2π × 2 × 10 × 20 × 10−12 − 6 = 6.61 k 1 104 Chapter 1–26 Substituting A0 = 100, x = 10%, RL = 10 k, and Ro = 6.61 k, Eq. (5) results in 100 = 27.9 mA/V 10 (10 6.61) × 103 1− 100 which, using Eq. (1), can be expressed in the alternate form 1 R2 R1 + R2 Gm ≥ Vo = Vi 1.72 Using the voltage divider rule, we obtain Thus when the attenuator is compensated (C1 R1 = C2 R2), its transmission can be determined either by its two resistors R1 , R2 or by its two capacitors. Thus we obtain 0.2 I1 = which is the value assumed. Consider first the bias design of the circuit in Fig. Since the signal across re is 5 mV, it follows that the signal across Re must be 50 − 5 = 45 mV and thus Re = 9re We choose to operate at this value of I . It follows that for the circuit in Fig. The gain of the first stage is Av 1 = −gm1 (ro1 /2) where (ro1 /2) is the equivalent resistance at the output of Q1 and includes ro1 in parallel with the output resistance of the current-source load, which is equal to ro1 . However, Ro will be increased to I Ro = 5 × 200 k = 1 M vo If the amplifier is fed with a signal source having Rsig = 5 k and a 100-k load resistance is connected to the output, the equivalent circuit shown below results. The results of part (a), however, will not change. Thus, at no load VZ 5.1 V ∴ Total conduction angle = 180 − 2θ = 175.2◦ For line regulation: b. (1 1) 500 vo = = (re in) vb (1 1) + re 500 + re β = 50: vb 21.3 = 0.68 V/V = v sig 21.3 + 10 vo 500 = 0.94 V/V = vb 500 + 32.1 vo = 0.68 × 0.94 = 0.64 V/V v sig 9 V β = 200: 4.5 V 20 k vb 50.9 = = 0.836 V/V v sig 50.9 + 10 vo 500 = = 0.969 V/V vb 500 + 16.2 vo = 0.836 × 0.969 = 0.81 V/V v sig IE 2 k Figure 1 6.123 Refer to the circuit in Fig. P6.111(b): 1 Rin = 10 k = 10 0.1 = 99 gm vo 5 2 = = 10(5 2) = 14.3 V/V v i2 1/gm Rin (c) v i2 = (Av o v i) Rin + Ro 99 = 0.99 × v i × 99 + 99 0.5v i 1V = 10 k 0.1 mA VG = 0, thus VS = −VGS , where VGS can be obtained from 1 2 ID = k n VOV 2 1 2 0.4 = × 5 × VOV 2 ⇒ VOV = 0.4 V VGS = Vt + 0.4 = 0.8 + 0.4 = 1.2 V VS = −1.2 V −1.2 − (−5) = 9.5 k RS = 0.4 To remain in saturation, the minimum drain voltage must be limited to VG − Vt = 0 − 0.8 = −0.8 V. B vsig vp gmvp rp ro C vo RL very high 6.51 The largest possible voltage gain is obtained when RL → ∞, in which case IC VA vo = −gm ro = − v sig VT IC To obtain maximum gain and the largest possible signal swing at the output for v eb of 10 mV, we select a value for RC that results in VA =− VT which is the highest allowable voltage at the collector while the transistor remains in the active region. Multiple, parallel transistors are acceptable. VA = 200 k I /2 (W/L)6 (I /2) (W/L)4 ⇒ 100 = (W/L)6 × 50 100 Thus, thus, (W/L)6 = 200 1 Ro5 = × 100 × 200 = 10 M 2 Using Eq. (8.171), we get Ro = Ro4 Ro5 = 10 10 = 5 M I7 = Ad = Gm Ro = 20 mA/V × 5000 k = 105 V/V or 100 dB (W/L)7 I (W/L)5 ⇒ 100 = (W/L)7 × 100 200 thus, (W/L)7 = 200 Ex: 8.20 From Exercise 8.17, we get ID = 0.4 mA VOV = 0.2 V gm1,2 = 4 mA/V Gm = 4 mA/V Ad = 100 V/V Now, RSS = 25 k gm3 = = 1 W I = μp Cox V2 2 2 L 1 OV1 graduate students Jeffrey Wang and Luke Wang • Professor Vincent Gaudet, University of Waterloo • Professors Shahriar Mirabbasi and Mandana Amiri, University of British Columbia • ProfessorWai Tung Ng, University of Toronto • Professor Olivier Trescases, University of Toronto • Professor Amir Yazdani, Ryerson University Exercise 1–1 Rs Ex: 1.1 When output terminals are open-circuited, as in Fig. IDN = 0 Because of the symmetry, IDP = 0.104, VO = −IDP × 10 k = −1.04 V √ √ 0.7 + 3 − 0.7 Ex: 5.16 Vt = 0.8 + 0.4 = 1.23 V Ex: 5.17 v DSmin = v GS + |Vt | =1+2=3V 1 × 2 [1 − (−2)]2 2 = 9 mA ID = Chapter 5–1 5.1 Cox = 9 fF/μm2 , VOV = 0.2 V VGS (V) L = 0.36 μm, VDS = 0 V W = 3.6 μm Q = Cox .W .L.VOV = 2.33 fC 5.2 k n = μn Cox C/V C 1 m2 F F = = = = V · s m2 V·s V·s s V2 = VOV (V) gDS rDS (mA/V) () 0.5 0 0 ∞ 1.0 0.5 2.5 400 1.5 1.0 5.0 200 2.0 1.5 7.5 133 2.5 2.0 10 100 A V2 Since k n = k n W/L and W/L is dimensionless, k n has the same dimensions as k n ; that is, A/V2 . All three transistors are operating in saturation with ID = 90 μA. v oc = v s (t) vs (t) For circuit b. See figures on next column. Thus, i= 10 V 10 V = 10 μA ⇒ R1 + R2 = R1 + R2 10 μA R1 + R2 = 1 M and R1 = R2 ⇒ R1 = R2 = 0.5 M 2 v 2 = 0.4v 2 2+3 Ex: 2.12 Hence 9 k vO = 1 + v + = 10 × 0.4v 2 = 4v 2 1 k (a) R2 Combining the contributions of v 1 and v 2 R1 v vI to v O , we have v O = 6v 1 + 4v 2 vO Ex: 2.10 9 k v I − v − = v O /A ⇒ v − = v I − v O /A 1 k 2 k v1 v3 But from the voltage divider across v O , vO v− = vO R1 R1 + R2 Equating Eq. (1) and Eq. (2) gives v2 3 k (1) vO R1 vO = vI − R1 + R2 A (2) Exercise 2–4 which can be manipulated to the form 1 + (R2 /R1) 1 + (R2 /R1) 1+ A (b) For R1 = 1 k and R2 = 9 k the ideal value 9 for the closed-loop gain is 1 + , that is, 10. The dc circuit can be obtained by opening all coupling and bypass capacitors, resulting in the circuit shown in Fig. Thus, these are the 7th and 9th harmonics. This in turn can be achieved by ensuring that VD does not fall below VG (which is zero) by more than Vt (0.4 V). This is a range of −44.5% to +36.4% of nominal. The results are as follows: CMRRd = 2gm REE / RC RC VOS = 1√ I /k n 2 RD RD (2) Thus, VOS (mV) 2 CMRRd = CMRRs RC /RC I (mA) 2 20 log = 34 dB RC /RC ⇒ RC = 0.04 = 4% RC 3 4 5 4 8 12 16 20 We observe that by accepting a larger offset we are able to obtain a higher gain. c. Thus ICBO becomes ICBO = 10 nA × 1024 = 10.24 μA At 20◦ C, T = 293 K and VT = 8.62 × 10−5 × 293 = 25.3 mV At 50◦ C, T = 323 K and VT = 8.62 × 10−5 × 323 = 27.8 mV If the transistor is operated at v BE = 700 mV, then (i) At 20◦ C, iE becomes 4.33 iE = 0.5e(700−692)/25.3 = 0.69 mA (ii) At 50◦ C, iE becomes iE = 0.5e(700−632)/27.8 = 5.77 mA 4.36 v BE = 0.7 V at iC = 10 mA For v BE = 0.5 V, From the figure we can write IS v BE /VT e − ICBO IB = β IC = IS ev BE /VT + ICBO iC = 10e(0.5−0.7)/0.025 = 3.35 μA (1) At a current IC and a BE voltage VBE , the slope of the iC –v BE curve is IC /VT . Now, VDS B is given by Eq. (6.8) [together with Eq. (6.7)], √ 2k n RD VDD + 1 − 1 VDS B = (2) k n RD RD = VDD − VDS Q ID 5 − 0.712 = 42.88 k = 0.1 213.7 (d) k n = = 4.98 mA/V2 42.88 4.98 W = = 24.9 L 0.2 6.9 VDD From the figure we see that VDS B = VOV + vˆgs Q2 where VOV = 0.2 V (given) and vO 0.5 V vˆgs = | Av | = 0.5 0.5 2.5 = = k n RD VOV k n RD × 0.2 k n RD vI Q1 iD (3) Thus, 2.5 VDS B = 0.2 + k n RD Substituting for VDS B from Eq. (2), we obtain √ 2.5 2k n RD VDD + 1 − 1 = 0.2 + k n RD k n RD Substituting VDD = 5 V, rearranging the equation to obtain a quadratic equation in k n RD , and given Vt1 = Vt2 = Vt 1 W [VDD − v O − Vt]2 For Q2 , iD = k n 2 L 2 1 W [v I − Vt]2 For Q1 , iD = k n 2 L 1 For Vt ≤ v I ≤ v O + Vt , equate iD1 and iD2 Chapter 6–4 W L = Similarly, [VDD − v O + Vt]2 2 W L [v I − Vt] 2 1 [VDD − v O − Vt] = v O = VDD − Vt + Vt −v I IC VCE (mA) (V) Av (V/V) POS Neg v O (V) v O (V) (W/L)1 · [v I − Vt] (W/L)2 0.5 4.5 –20 0.5 4.2 1.0 4.0 –40 1.0 3.7 (W/L)1 (W/L)2 2.5 2.5 –100 2.5 2.2 4.0 1.0 –160 4.0 0.7 4.5 0.5 –180 4.5 0.2 (W/L)1 (W/L)2 50 √ (W/L)1 0.5 = 10, For = 5 (W/L)2 0.5 √ Av = − 10 = −3.16 V/V 6.12 6.10 Refer to Fig. 2 Here also observe that this relationship (and graph) is universal and represents any MOSFET. Thus, including RF results in the nonideal integrator response shown in Fig. Thus, the current through the 80-k resistor is 0.05IE1 + 0.01IE1 = 0.06IE1 and VE2 = 6.3 + 0.7 = 7 V IC2 = αIE2 = 0.99 × 20.13 = 20 mA VB1 = VE1 + 0.7 = 2IE1 + 0.7 0.06IE1 IC1 1.21 = = 20.13 mA 0.06 0.06 VC2 = 20 × 0.1 = 2 V 9 − (2IE1 + 0.7) 9 − VB1 = = 80 80 Finally, with the resistance R connected between E1 and C2 , it will conduct a current that we can initially estimate as ⇒ IE1 = 1.22 mA 9 V VE 2 D2 Q2 IC1 VB1 ID1 0.05 IE1 100 V2 0.06 IE1 D1 IE 2 2 k ID2 80 k 0.01IE 2 Q1 0.01IE IE1 V1 40 k VE1 2 k Figure 3 VC2 100 Chapter 4–29 9V IE 2 100 2 k 80 k V2 VE2 (ID1 IB1) (IC1 IB2) VC1 VB1 D1 ID1 VE2 D2 IC1 Q2 IB2 Q1 IB1 V1 40 k IC2 I IE1 VE1 R VC2 2 k 100 2 k Figure 4 I= 2.44 − 2 VE1 − VC2 = = 0.22 mA R 2 This is a substantial amount compared to IE1 = 1.22 mA, requiring that we redo the analysis with R in place. For (b) Vo = Vi 1 R+ sC R Vo sRC = Vi 1 + sCR Vo = Vi s s+ 1 RC which is of the form shown in Table 1.2 for the high-pass function, with K = 1 and ω0 = 1/RC. i1 isig Rsig 7.55 Rsig Rsig 7.55 Refer to Fig. ∴ use R = 207 (c) Line regulation = 7 mV = 33 207 + 7 V vS vO R ±25% change in v S ≡ ± 5 V VO changes by ±5 × 33 = ±0.165 mV ±0.165 × 100 = ±1.65% 10 corresponding to Using the constant voltage drop model: (d) Load regulation = − (rZ R) ideal = −(7 207) = −6.77 VD 0.7 V or –6.77 V/A VO = −6.77 × 20 mA = −135.4 mV R 1 k vS 0.1354 × 100 = −1.35% corresponding to − 10 (e) The maximum zener current occurs at no load IL = 0 and the supply at its largest value of 1 20 + (20) = 25 V. 4 (e) P = V 2 /R = 202 /(1 × 103) = 0.4 W Thus, the resistor should have a 1 -W rating. ∴ Maximum v o = i × 10 k = 0.1 × 10 =1V I = 1 mA Each diode exhibits 0.7 V drop at 1 mA current. vo = 22.7 V/V and gain in dB 20 log 22.7 = vs Av 2 = 27.1 dB = 9.09 V/V (b) Case S-B-A-L (see figure above): Av 3 = v o v ia v ib vo = · · vs v ia v ib v s 100 × = 100 × 100 + 10 K 100 K 10 × × 100 K + 1 K 10 K 10 K + 100 K vo = 0.89 V/V and gain in dB is 20 log 0.89 = vs −1 dB. | Ad | 100 = = 2500 | Acm | 0.04 Exercise 2–5 Ex: 2.16 We choose R3 = R1 and R4 = R2 . A change in temperature from 25◦ C to 125◦ C—that is, an increase of 100◦ C—results in 10 doublings or, equivalently, an increase by a factor of 210 = 1024. (b) For an integrator with RF , the 0.1-mA current flows through the parallel combination of C and RF . (2)–(6): ID1 × 40 = IE1 × 2 IE3 = 0.276 mA IC4 = 0.116 mA ⇒ ID1 = 0.05IE1 IB3 = 0.154 mA I = 0.102 mA But IE4 = 0.134 ID1 = The base current of Q4 can be obtained from IB4 = IE4 − IC4 = 0.134 − 0.116 = 0.018 mA Thus, Finally, the collector current of Q3 can be found as IE1 = IC3 = I + IB4 = 0.102 + 0.018 = 0.120 βforced4 0.069 = 1.38 mA 1.4 mA 0.05 VE1 = IE1 × 2 = 2.77 V 2.8 V The forced β values can now be found as βforced3 = 9 − 0.7 = 0.069 mA 0.07 mA 80 + 40 VB1 = VE1 + 0.7 = 3.5 V IC3 0.120 = 0.8 = IB3 0.154 IC1 = IE1 = 1.38 mA 1.4 mA IC4 0.116 = = = 6.4 IB4 0.018 V2 = 9 − IC1 × 2 = 9 − 1.38 × 2 6.2 V Both βforced values are well below the β value of 50, verifying that Q3 and Q4 are in deep saturation. Now, for the circuit under consideration, all resistors are nominally equal to 10 k, but each has a tolerance of ±x%. Thus, it reaches 40 dB at a frequency four decades higher than fb , If an input step of amplitude 1.6 V (10 times as large compared to the previous case) is applied, the output will be slew-rate limited and thus linearly rising with a slope equal to the slew rate, as shown in the following figure. From the circuit VD = VDD − ID RD = 15 − 0.5 × 16 = +7 V, as assumed Finally, VGS = 1.5 V, thus VOV = 1.5 − Vt = 1.5 − 1 = 0.5 V 1 1 2 = × 4 × 0.52 = 0.5 mA ID = k n VOV 2 2 which is equal to the given value. 7.45(b)] that the total effective resistance between the MOSFET source terminal and ground is 1 ro1 ro3 . Thus, ⇒ Re = 350 3 = 1.5 k Rs = 2 mA/V = 40.4 k Gv = −β = −100 RD RL Gv = Av = − 1 + Rs gm =− Rin = (β + 1)(re + Re) = 101 × (50 + 350) 2020

A/V = 121 mA/V In 100 k vi 1.57 Ro = = 2 k v o = 10 × Out Gmvi 100 k Gm 121 mA/V Open-circuit output voltage 10 V = Short-circuit output current 5 mA 2 =5V 2+2 The node equation at E yields the current through RE as (βib + ib) = (β + 1)ib . P2.65. VCC RC RC vod Rsig/2 Rsig/2 Q1 vsig 2 Q2 Re VCM vsig 2 VEE Substituting for RC from (2), for Re from (1), and for re = VT /(I /2), we obtain α(120VT /αI) (2VT /I) + (8VT /I) Ad = = Rid v id = v sig Rid + Rsig Rsig = 2(β + 1)(re + Re) (1) thus, (2) α × Total resistance between collectors v od = v id Total resistance in emitters (3) Gv ≡ β , α(β + 1) = β, we have β +1 2βRC Gv = 2(β + 1)(re + Re) + Rsig α × Total resistance in collectors vo = vi Total resistance in emitters 0.99 × 25 2re + 2 × 0.25 where VT 25 mV = 250 = re = IE 0.1 mA v od 2α(β + 1)RC = v sig 2(β + 1)(re + Re) + Rsig Since α = 2 RC 4RC = 6(re + Re) 3 re + Re Thus the gain increases from approximately 1 2 RC /(re + Re) to RC /(re + Re). The total current drawn from the power supply is I = 0.103 + 1.252 + 2.78 = 4.135 mA 10 k 5 V 0 IE IB Q2 on IE Thus, the power dissipated in the circuit is P = 15 V × 4.135 mA = 62 mW 5 V VE IE 1 1 k Exercise 4–7 From the figure we see that Q1 will be off and Q2 will be on. Thus, v B1 − v B2 = v BE1 + iE1 Re − iE2 Re − v BE2 = (v BE1 − v BE2) + Re (iE1 − iE2) 200 = 20 + Re (iC1 − iC2) = 20 + Re (138 − 62) ⇒ Re = 180 mV = 2.37 k 76 μA (d) Without Re , v id = 20 mV → iC1 − iC2 = 76 μA 76 μA = 3.8 mA/V Gm = 20 mV With Re , v id = 200 mV → iC1 − iC2 = 76 μA 76 μA = 0.38 mA/V Gm = 200 mV Thus, the effective Gm has been reduced by a factor of 10, which is the same factor by which the allowable input signal has been increased while maintaining the same linearity. (e) When v I < 0, D1 is conducting and the circuit becomes a voltage divider where the negative peak is vO 1 k × −5 V = −2.5 V 1 k + 1 k 5V 5 V t (j) vO 5V Vp+ = 5 V, Vp− = −5 V, f = 1 kHz D1 conducts when v I > 0 and D2 conducts when v I < 0. VC = 3 − 0.2 × 10 = 1 V VT 25 mV = 125 = re = IE 0.2 mA Replacing the BJT with the T model of Fig. This requires our using the largest possible v GS,1 voltage. RG RD vo Design 1: VOV = 0.2 V, VGS = 0.6 V ID = 0.8 mA vi Now, Av = −k n VOV RD Thus, ⇒ RD = 12.5 k Refer to the solution of Example 6.3. From vo Eq. (6.47), Av = ≡ −gm RD (note that RL vi is absent). 4 VT 25 mV ⇒5= . ISBN: 978-0-19-933916-7 Exercise Solutions (Chapters 1-17) Problem Solutions (Chapters 1-17) Preface This Instructor's Solution Manual (ISM) contains complete solutions for all exercises and end-of-chapter problems included in the book Microelectronic Circuits, International Seventh Edition by Adel S. P5.52(g). Furthermore, it must be that C is now the dominant determinant of the amplifier 3-dB frequency (i.e., it is dominating over whatever may be happening at node B or anywhere else in the amplifier). P7.95. 5V ≤ 2 mV (c) N 2 −1 (b) Av = 2N − 1 ≥ 2500 For N = 12, Resolution = 5 = 1.2 mV 212 − 1 Quantization error = 1.2 = 0.6 mV 2 1.35 (a) When bi = 1, the ith switch is in position 1 and a current (Vref /2i R) flows to the output. This will disable the controlled source gm v i . 2 n L OV Ex: 5.5 VOV = 0.5 V 1 VOV = gDS = L 1 k W 1 ∴ k n = k n = = 2 mA/V2 L 1 × 0.5 W k n For v DS = 0.5 V = VOV , the transistor operates in saturation, and ID = 1 W 2 k V = 0.25 mA 2 n L OV ⇒ VG ≤ 5 − 1 = 4 V (b) Triode region occurs for VDG ≥ |Vtp | = 1 V ⇒ VD ≥ VG + 1 (c) Conversely, for saturation VDG ≤ |Vtp | = 1 V ⇒ VD ≤ VG + 1 (d) Given λ ~ =0 ID = 1 W k |VOV |2 = 75 μA 2 pL ∴ |VOV | = 0.5 V = VSG − |Vtp | ⇒ VSG = |VOV | + |Vtp | = 1.5 V VG = 5 − |VSG | = 3.5 V VD ≤ VG + 1 = ≤4.5 V Exercise 5–2 (e) For λ = −0.02 V−1 and |VOV | = 0.5 V, ID = 75 μA and ro = 1 = 667 k |λ|ID (f) At VD = 3 V, VSD = 2 V 1 W k |VOV |2 (1 + |λ||VSD |) 2 nL = 75 μA (1.04) = 78 μA ID = Saturation mode (v GD = 0 < Vtn) : VD = 0.7 V = 1.8 − ID RD 1 W μ Cox (VD − Vtn)2 = 0.032 mA 2 n L 1.8 − 0.7 ∴R= = 34.4 k 0.032 mA ID = Ex: 5.10 At VD = 0 V, VSD = 5 V 1.8 V ID = 75 μA (1.10) = 82.5 μA ro = VDS 3V = 667 k = ID 4.5 μA R2 R1 which is the same value found in (c). 2 for the Bode plot. 4 vO (a) v O = v S + 0.7 V, v O = 0, For v S ≤ − 0.7 V for v S ≥ −0.7 V VZ = VZ0 + rZ IZ vO 25 V 0.7 V 0 vS 207 slope 1 VZ IL 0 (b) 10 V vS vO t 0.7 V 25 − VZ = 9.825 + 7 × 207 207VZ = 207 (9.825) + 7 (25) − 7VZ 10 V 0.7 V u Chapter 3–25 3.65 (c) The diode conducts at an angle 0.7 θ = sin−1 = 4◦ and stops 10 0.7 V at π − θ = 176◦ vS R 1 k vO Thus the conduction angle is π − 2θ = 172◦ or 3 rad. A node equation at 2 results in the current leaving node 2 as 4I . 2, we see that VSD = VSG − 3 5.55 (a) Refer to the circuit in Fig. This occurs when v S is at its maximum negative value −Vp . The 1 10 actual closed-loop gain is G = . 10 V IE = VCC − VBE RB RC + β +1 10 − 0.7 RB 7.7 + 101 ⇒ RB = 162 k 1= Selecting standard 5% resistors (Appendix J), we use RC RB = 160 k vo and RC = 7.5 k The resulting value of IE is found as 10 − 0.7 = 1.02 mA 160 7.5 + 101 and the collector voltage will be IE = RE vi 5V To establish IE = 1mA, IE = 5 − VBE RE 1 mA = 5 − 0.7 RE VC = VCC − IE RC = 2.3 V Ex: 6.37 Refer to Fig. Thus the 3 component of v o due to v 2 will be Ri Rs + Ri 10 k 10 k 10 k = 2 2 = vs 1+2 3 v o2 = v 2 v o = Gm v i (RL Ro) 10 10 × Gm2 × 10 + 10 3 = v 2 × 0.5 × 20 × 20 × 1 vi = 60 20 + 1 20 2 = 60 × v s 21 3 Overall voltage gain: vo = 38.1 V/V vs 1.52 i2 ix vx Gmvi Consider first the path for the signal requiring higher gain, namely v 2 . Thus v √ VOV 7 = 2VOV 1,2 = 2VOV Chapter 8–34 and gm7 √ 2I 2I 2I = = √ = VOV 7 V 2VOV OV ro7 = ro9 = VA I 1 gm ro3 1 = 0.98 A/A =1 1+ 1 × 50 Rom = ro4 = 50 k Thus, √ 2 √ 2 2I VA 2VA = = VOV I VOV I RSS 1+ Am = 1 and √ 2 1 2|VA | I I 2VA × × ×2× × CMRR = VOV 2 I VOV VOV I VA 3 √ =2 2 Q.E.D. VOV For k (W/L) = 4 mA/V2 and I = 160 μA, Ro2 = ro2 + 2RSS + 2gm2 ro2 RSS = 50 + 50 + 2 × 1 × 50 × 25 = 2600 k Acm = −(1 − Am)Gmcm (Rom Ro2) Acm = −(1 − 0.98) × 0.02 × (50 2600) = −0.0196 V/V Ad = 25 = 1274 CMRR = Acm 0.0196 or 62.1 dB 1 × 4 × |VOV |2 2 ⇒ |VOV | = 0.2 V Alternatively, using the approximate expression in Eq. (8.157), we obtain For |VA | = 5 V: Acm = 0.080 = For case (a), CMRR = 2 × 5 0.2 and 2 = 1250 or 62 dB CMRR = 25 = 1250 0.02 or 61.9 dB For case (b), √ CMRR = 2 2 1 1 = −0.02 V/V =− 2gm3 RSS 2 × 1 × 25 5 0.2 3 = 4.42 × 104 or 93 dB Ad 8.98 CMRR = Acm CMRR = 60 dB or equivalently 1000. 1.3 (a) V = IR = 5 mA × 1 k = 5 V P = I 2 R = (5 mA)2 × 1 k = 25 mW (b) R = V /I = 5 V/1 mA = 5 k P = VI = 5 V × 1 mA = 5 mW Req = 10 10 × 1000 = = 9.9 k 1000 + 10 1.01 a 1% reduction; (b) 100 k results in Req = 10 × 100 10 = 9.09 k 100 + 10 1.1 a 9.1% reduction; (c) 10 k results in Req = 10 = 5 k 10 + 10 a 50% reduction. The latter can be added to the 10-k resistor that is connected to the base. 2 3 = Using (2) and (3), we get Thus, (4) (6) 4βRC 2(2β + 1)(re + Re) + 2(β + 1)(re + Re) 8.46 Refer to Fig. Rsig vsig RG1 RG2 vgs gmvgs Rin RG Rin = RG1 // RG2 Figure 2 ro RD 5 k RL 5 k vo Chapter 6–41 (c) v G = 0 V (dc) + v sig v Gmin = −v̂sig v̂D = VD + | Gv |v̂sig where VD = −2.5 + ID RD = −2.5 + 0.3 × 5 = −1 V To remain in saturation, v̂D ≤ v̂G + |Vtp | −1 + 10 v̂sig ≤ −v̂sig + 0.7 Satisfying this constraint with equality gives v̂sig = 0.154 V and the corresponding output voltage v̂d = | Gv |v̂sig = 1.54 V (d) If v̂sig = 50 mV, then VD + | Gv |v̂sig = −v̂sig + |Vtp | where VD = −2.5 + ID RD = −2.5 + 0.3RD | Gv | = gm RD = 2RD Thus −2.5 + 0.3RD + 2RD v̂sig = −v̂sig + |Vtp | −2.5 + 0.3RD + 2RD × 0.05 = −0.05 + 0.7 0.4RD = 3.15 ⇒ RD = 7.875 k Gv = −gm RD = −2 × 7.875 = −15.75 V/V 6.110 Refer to Fig. iL Vp = IL R d Vp cos ωt + IL dt = −C sin ω t × ωVp + IL =C = −C sin(−ωt) × ωVp + IL For a small conduction angle Vp 2Vr = iD,max = Cωt × ωVp + IL Sub (b) to get 2V r iD,max = C ωVp + IL Vp Substituting ω = 2πf and using (a) together with Vp /R IL results in Vp Q.E.D. iDmax = IL 1 + 2π 2Vr Ex: 3.23 D4 ac line voltage D1 vO vS R D2 C D3 + IL Since the output is approximately held at Vp , Vp ≈ IL · Thus R Vp = iD,av ~ + IL = π IL 2Vr iD,max = C sin(−ωt) ≈ − ωt. (1) where A = 104 V/V and VOS = 5 mV. If a potentiometer is used, the total resistance of the potentiometer must be at least 1.6 k. T = 0◦ C = 273 K: ni = 1.52 × 109 cm−3 ; N = 3.3 × 1013 ni ◦ T = 20 C = 293 K: −5 ×398) = 7.3 × 1015 × (398)3/2 e−1.12/(2×8.62×10 = 4.72 × 1012 /cm3 pn = n2i = 2.23 × 108 /cm3 NI At 398 K, hole concentration is pn = 2.23 × 108 /cm3 ni = 8.60 × 109 cm−3 ; N = 5.8 × 1012 ni T = 75◦ C = 348 K: N = 1.4 × 1011 ni = 3.70 × 10 cm ; ni 11 At 398 K, ni = BT 3/2 e−Eg /2kT −3 T = 125◦ C = 398 K: N = 1.1 × 1010 ni 1.75 Use Eq. (1.2) to find ni , ni = BT 3/2 e−Eg /2kT −5 ×300) = 7.3 × 1015 (300)3/2 e−1.12/(2×8.62×10 In phosphorus-doped Si, hole concentration drops below the intrinsic level by a factor of 108 . R R Chapter 3–17 ∴ VT VO = V + VT + (V + − 0.7) (b) At no load, ID = rd = R V VO rd VO mr d mVT = = V + mr d + R mVT + IR = =− 1 ID ID + V + − 0.7 VT =− VT × ID =− V + − 0.7 VT × ID VT + V + − 0.7 For mVT mVT = (V + − 0.7m) VT ID 1 VO = − (rd R) = − 1 1 IL + rd R Small-signal model (b) If m diodes are in series, we obtain V + − 0.7 R 1 VT +1 V + − 0.7 mA VO ≤5 IL mA 5 mV VT V + − 0.7 ≤ × ID VT + V + − 0.7 mA mV 15 − 0.7 25 ≤5 × ID 0.025 + 15 − 0.7 mA i.e., (c) For m = 1 VO VT = = 1.75 mV/V V + VT + V + − 0.7 For m = 4 VO mVT = 8.13 mV/V V + mVT + 15 − m × 0.7 ID ≥ 4.99 mA ID 5 mA R= 15 − 0.7 V + − 0.7 = ID 5 mA R = 2.86 k 3.52 V Diode should be a 5-mA unit; that is, it conducts 5 mA at VD = 0.7 V, thus 5 × 10−3 = IS e0.7/0.025 . C1 , C2 , and the transmission is not a function of frequency. Then we have (refer to the solution of Exercise 2.9): v O = 6v 1 Then we have 10 Rc = = 2.5 k R3 = 4 4 Rc 10 10 Ra = × 2, = =2 R1 Rb R1 10 To find the contribution of v 2 to v O , we set v 1 = v 3 = 0, then: v O = 4v 2 ⇒ R1 = 5 k Rc 10 10 Ra =1 × =1⇒ R2 Rb R2 10 To find the contribution of v 3 to v O we set v 1 = v 2 = 0, then 9 k v 3 = −9v 3 1 k Combining the contributions of v 1 , v 2 , and v 3 to v O we have: v O = 6v 1 + 4v 2 − 9v 3 . iC C Chapter 4–6 V7 − 0.7 + 10 V7 + 9.3 = (1) 3 3 Since IB = 0, the collector current will be equal to the current through the 9.1-k resistor, 4.24 = 10 − V7 9.1 Since α1 1, IC = IE = I6 resulting in IC = 4.25 (a) Refer to Fig. 7.41(b) indicates that the incremental resistance of Q4 would appear in series with the gate of Q3 and thus carries zero current. Exercise 6–1 Ex: 6.1 Refer to Fig. Now, ID = and VGS1 = 1.84 V 1 k n (VGS2 − Vt)2 2 Substituting ID = V2 + 2.5 and VGS2 = −V2 , V2 + 2.5 = 5.54 10 V 1 × 1.5(−V2 − 0.9)2 2 (V2 + 2.5) = V22 + 1.8 V2 + 0.81 1.5 VSG VSD R IR V22 + 0.467 V2 − 2.523 = 0 ⇒ V2 = −1.84 V Thus, I ID = V2 + 2.5 = −1.84 + 2.5 = 0.66 mA and Fig. 1 = 1.6 μF 2π × 100 × 1 × 103 Ex: 2.24 From Eq. (2.37) we have: VO = IB1 R2 IB R2 = 100 nA × 1 M = 0.1 V From Eq. (2.39) the value of resistor R3 (placed in series with positive input to minimize the output offset voltage) is R3 = R1 R2 = R1 R2 10 k × 1 M = R1 + R2 10 k + 1 M = 9.9 k R3 = 9.9 k 10 k Vo With the feedback resistor RF , to have at least ±10 V of output signal swing available, we have to make sure that the output voltage due to VOS has a magnitude of at most 2 V. At the outset we observe that at the input side of the g-parameter model, we have the controlled current source g12 I2 . Also, ro = . 1.1a: For circuit a. 6.55(b). 3) the MOSFET will be operating in the triode region, and VSD = VSG − 10 V Since we expect VSD to be very small, we can 2 neglect the VSD term in the expression for ID and write ID k p (VSG − |Vt |)VSD source has a voltage of 2.323 V across it, more than sufficient for its proper operation. Thus the signal across (re + Re) is 50 mV. Specifically, RG2 VG = VDD RG2 + RG1 22 =9× = 4.95 V 22 + 18 It can be shown (after simple but somewhat tedious analysis) that the resulting ID will be ID = 0.986 mA, which is sufficiently close to the desired 1 mA. gm = μn Cox μn Cox Wn = μp Cox Wp ⇒ = Wp = 2.5 Wn Ex: 6.10 1 W ID = k p (VSG − |Vt |)2 2 L μp Wn = 0.4 = μn Wp IC = 0.5 mA (constant) β = 50 gm = β = 200 IC 0.5 mA = VT 25 mV = 20 mA/V = 20 mA/V 0.5 0.5 IC = = IB = β 50 200 = 10 μA rπ = = 2.5 μA β 50 200 = = gm 20 20 = 2.5 k = 10 k Exercise 6–4 ic = βib = β Ex: 6.15 β = 100 gm = IC = 1 mA = 1 mA = 40 mA/V 25 mV β v be = gm v be rπ ie = ib + βib = (β + 1)ib = (β + 1) VT αVT 25 mV = 25 = re = IE IC 1 mA rπ = v be rπ = β 100 = 2.5 k gm 40 v be rπ v be v be = rπ (β + 1) re Ex: 6.18 Ex: 6.16 IC 1 mA = = 40 mA/V gm = VT 25 mV v ce = −gm RC Av = v be C gmvbe ib = −40 × 10 B = −400 V/V re VC = VCC − IC RC vbe = 15 − 1 × 10 = 5 V v C (t) = VC + v c (t) E = (VCC − IC RC) + Av v be (t) v be − gm v be re 1 = v be − gm re β 1 − = v be rπ/β+1 rπ β +1 β v be = v be − = rπ rπ rπ ib = = (15 − 10) − 400 × 0.005 sinωt = 5 − 2 sinωt iB (t) = IB + ib (t) where 1 mA IC = = 10 μA IB = β 100 and ib (t) = = gm v be (t) β Ex: 6.19 40 × 0.005 sinωt 100 10 V = 2 sinωt, μA Thus, RE 10 k iB (t) = 10 + 2 sinωt, μA CC1 Ex: 6.17 vi ib B ic CC2 C vbe bib rp RC 7.5 k E 10 V vo Exercise 6–5 10 − 0.7 = 0.93 mA 10 IC = αIE = 0.99 × 0.93 VE = −0.1 − 0.7 = −0.8 V IE = (b) gm = = 0.92 mA VC = −10 + IC RC = −10 + 0.92 × 7.5 = −3.1 V Av = vo αRC = vi re where re = Av = IC 0.99 = 40 mA/V VT 0.025 rπ = β 100 = 2.5 k gm 40 ro = VA 100 = 101 100 k = IC 0.99 (c) Rsig = 2 k RB = 10 k rπ = 2.5 k 25 mV = 26.9 0.93 mA gm = 40 mA/V 0.99 × 7.5 × 103 = 276.2 V/V 26.9 For vˆ i = 10 mV, vˆ o = 276.2 × 10 = 2.76 V Ex: 6.20 10V RC = 8 k RL = 8 k ro = 100 k Vy Vy Vπ = × Vsig Vsig Vπ = RB rπ × −gm (RC RL ro) (RB rπ) + Rsig = 10 2.5 × −40(8 8 100) (10 2.5) + 2 −0.5 × 40 × 3.846 = −77 V/V 8 k If ro is negelected, X Y 10 k Z I 1 mA Vy = −80, for an error Vsig of 3.9%. Thus 4.60 Refer to the circuit in Fig. IDQ = 1 2 k n VOV 2 1 × 10 × 0.04 = 0.2 mA 2 VDD − VDS 5−1 RD = = = 20 k IDQ 0.2 = Coordinates of point B: Equation (6.6): √ 2k n RD VDD + 1 − 1 VGS B = Vt + k n RD √ 2 × 10 × 20 × 5 + 1 − 1 = 0.5 + 10 × 20 = 0.5 + 0.22 = 0.72 V Equations (6.7) and (6.8): √ 2k n RD VDD + 1 − 1 VDS B = = 0.22 V k n RD Av = −k n RD VOV = −10 × 20 × 0.2 = −40 V/V The lowest instantaneous voltage allowed at the output is VDS B = 0.22 V. Obviously, this bias method is very intolerant of the inevitable variations in β. β= IC 0.394 = = 66 IB 0.006 α= IC 0.394 = 0.985 = IE 0.4 Since IC IE 4.51 VCC 3 V 3.4 − VB = VB + 2.3 VB = 0.55 V For this value, VE = 0.55 − 0.7 = −0.15 V 0.1 mA RC 1 k R1 0 VB 1.2 V VC = −0.15 + 0.3 = +0.15 V (g) For the transistor to operate in saturation with βforced = 2, VE = VB − 0.7 RE 1 k R2 Figure 1 Chapter 4–16 4.52 From Fig. (b) Refer to Fig. 0.5 ID 0.01 = 1 VA 2 k n (1 − Vt) 2 ⇒ VA = 50 V (or larger to limit the mismatch in ID to 1%). However, the input resistance is only 25 k. ⇒ R = 5 k IL R 0.8 I 0.2 I 0.1R 1.1R 4 I 1.12 R 0.2 I 0.8 I Rin I R 11R 4 } 10I /3 = 2IR/3 1.1R 4 R Rin 1.11 Connect a resistor R in parallel with RL . I will be most grateful to instructors who discover errors and point them out to me. Thus, we were justified in neglecting IR above. To obtain the coordinates of point M, we solve the load line and line L2 to find the intersection M, and the load line and line L3 to find N: 6.22 ID = v GS = VGS For point M: iC = 8 + (8/100)v CE and iC = 10 − v CE ∴ iC M = 8.15 mA, 1 Vgs × 100 Q.E.D 4 VOV For Vgs = 10 mV, to keep the second-harmonic distortion to less than 1%, the minimum overdrive voltage required is 1 0.01 × 100 = 0.25 V VOV = × 4 1 = IC = iC = 10 − v CE = 5.24 mA v CE M = 1.85 V 1 1 2 k n VOV = × 10 × 0.22 = 0.2 mA 2 2 + v gs , where v gs = 0.02 V v OV = 0.2 + 0.02 = 0.22 V 1 1 iD = k n v 2OV = × 10 × 0.222 = 0.242 mA 2 2 Thus, id = 0.242 − 0.2 = 0.042 mA For point N: iC = 2 + 0.02v CE and iC = 10 − v CE v CE N = 7.84 V, 1 k n (VGS − Vt)2 + k n (VGS − Vt)Vgs sin ωt 2 1 1 + k n Vgs2 (− cos 2 ωt) 2 2 2 Second-harmonic distortion 1 k n Vgs2 4 × 100 = k n (VGS − Vt)Vgs = = 5 + 0.05v CE Load line ⇒ iC = 1 k n (VGS − Vt)2 + k n (VGS − Vt)Vgs sin ωt 2 1 + k n Vgs2 sin2 ωt 2 iC N = 2.16 mA Thus the collector current varies as follows: For v gs = −0.02 V, v OV = 0.2 − 0.02 = 0.18 V 1 1 iD = k n v 2OV = × 10 × 0.182 = 0.162 mA 2 2 Thus, id = 0.2 − 0.162 = 0.038 mA 2.91 mA 8.15 mA 5.24 mA i 5.99 mA, peak to peak 2.16 mA 3.08 mA Thus, an estimate of gm can be obtained as follows: 0.042 + 0.038 = 2 mA/V gm = 0.04 Alternatively, using Eq. (6.33), we can write gm = k n VOV = 10 × 0.2 = 2 mA/V which is an identical result. = 4 × 106 rad/s ⇒ fmax = 637 kHz vi (V) 2.116 (a) Vi = 0.5, Vo = 10 × 0.5 = 5 V 2 Output distortion will be due to slew-rate limitation and will occur at the frequency for dv O which = SR dt max t W ωmax × 5 = 10 × 106 ωmax = 2 × 106 rad/s and fmax = 318.3 kHz vO (V) (b) The output will distort at the value of Vi that dv O results in = SR. 7.49. Thus the maximum allowable negative signal swing at the output is VDSQ − 0.22 = 1 − 0.22 = 0.78 V. (e) The lowest value of A0 is obtained with the first design when operated at ID = 100 μA. Chapter 8–15 vˆid ⇒ VCM max = VCC + 0.4 − − 2 vˆid Ad VT + Q.E.D. 2 (b) VCC = 2.5 V, (4) vˆid = 10 mV, Ad = 50 V/V, VCM max = 2.5 + 0.4 − 0.005 − 50(25 + 5) × 10−3 1.4 V vˆod = Ad × vˆid = 50 × 10 = 500 mV = 0.5 V Using Eq. (2), we obtain IRC = 2Ad VT = 2 × 50 × 0.025 = 2.5 V To limit the power dissipation in the quiescent state to 1 mV, the bias current must be limited to I= Pmax 1 = = 0.2 mA VCC + VEE 5 Using this value for I , we get RC = 2.5 = 12.5 k 0.2 (c) To obtain VCM max = 1 V, we use Eq. (4) to determine the allowable value of Ad , 8.40 (a) Consider transistor Q1 , I vˆid v C1min = (VCC − RC) − Ad 2 2 1 = 2.5 + 0.4 − 0.005 − Ad (25 + 5) × 10−3 (1) where Ad = gm RC = I /2 RC VT IRC 2VT Since vˆid v B1 = VCM max + 2 to keep Q1 in the active mode, v B1 ≤ 0.4 + v C1min Thus, VCM max + vˆid vˆid = 0.4 + VCC − Ad VT + 2 2 Thus, by reducing VCM max from 1.4 V to 1 V, we are able to increase the differential gain from 50 V/V to 63.2 V/V. v O,avg vo 200 vi vo 7 mV = = 33.8 vi 200 + 7 V 200 VO IL rZ V O −IL (rZ 200) = IL IL mA = −6.8 (Vs sin φ − VD) d φ θ 1 [−Vs cos φ − VD φ]φ=π−θ φ−θ 2π 1 [Vs cos θ − Vs cos (π − θ) − VD (π − 2θ)] = 2π But cos θ 1, cos (π − θ) − 1, and π − 2θ π VD 2Vs − 2π 2 VD Vs − = π 2 √ For Vs = 12 2 and VD = 0.7 V √ 12 2 0.7 v O,avg = − = 5.05 V π 2 c. For the given values, W ID gm = 2μn Cox L √ = 2 × 0.2 × 10 × 0.1 = 0.632 mA/V = 0.545 V Vx = VBE3 + VBE1 = 1.187 V If IREF is increased to 1 mA, VBE1 = 0.7 IC3 0.02 mA 1 = 0.6 V VBE3 = 0.7 − 0.025 ln 0.02 Vx = 1.3 V Thus, 1 = 1.6 k gm Vx = 1.3 − 1.187 = 0.113 V (b) Replacing the BJT with its hybrid-π model results in the equivalent circuit in Fig. VA 125 V = = 12.5 k IC 10 mA 4.42 The equivalent circuits shown in the figure correspond to the circuits in Fig. P8.46. Thus the fundamental will have a frequency of 98/7, or 14 kHz, and peak amplitude of 63 × 7 = 441 mV. With the selected capacitor values, we obtain fP2 1 = 0.64 Hz 2π × 0.1 × 10−6 × 2.5 × 106 3 × 10−3 = = 95.5 Hz 2π × 5 × 10−6 fZ = 0 (dc) fP3 1 = = 5.3 Hz 2π × 1 × 10−6 (20 + 10) × 103 Since fP2 fP1 and fP3 , we have fL fP2 = 95.5 Hz 9.7 The amplifier in Fig. Thus there will be (2N − 1) discrete steps from 0 to VFS with the step size given by Step size = (b) bN is the LSB VFS 2N − 1 This is the analog change corresponding to a change in the LSB. P2.58: Rid = 2R1 = 2 × 5 k = 10 k Considering that v − = v + : R2 vO − v1 v2 = ⇒ vO = v2 − v1 2 2 v1 =R v 1 only: Ri = I v1 + R1 vO R4 R I v1 R R3 R2 = 5 V/V ⇒ R2 = 50 k = R4 R1 R1 = R3 = 10 k vO = vO The two resistance ratios ∴ R1 = R2 = R3 = R4 = 10 k From Eq. (2.16), vI2 100 × 100 + 5 (a) Ad = 2.56 R1 = R3 = 5 k, R2 = R4 = 100 k R4 R2 Equation (2.15): = = 20 R3 R1 vI1 R4 R4 + R3 (Refer to Fig. NMOS Sat. (d) Since current source I2 is implemented with a cascoded current source, the minimum voltage required across it for proper operation is 2VOV = 2 (0.2 V) = 0.4 V. The circuit together with its equivalent half-circuit are shown in the figure. Thus, the possible 1 M range of IOS is 0.2 μA to 0.4 μA. Rsig vo vsig R1 R2 vp Rin rp gmvp RC RL Chapter 6–45 For VE 4.3 = 2.15 k = IE = 2 mA, RE = IE 2 5 IR2 = 0.2 mA, R2 = = 25 k 0.2 2 IE = 0.02 mA IB = β +1 101 IR1 = IR2 + IB = 0.2 + 0.02 = 0.22 mA VCC − VB 15 − 5 R1 = = 45.5 k = IR1 0.22 Choosing 5% resistors: RE = 2.2 k, R1 = 47 k, R2 = 24 k For these values, VBB − VBE IE = RB RE + β +1 where 24 R2 = 5.07 V = 15 × VBB = VCC R1 + R2 24 + 47 RB = R1 R2 = 47 24 = 15.89 k 5.07 − 0.7 = 1.85 mA IE = 15.89 2.2 + 101 VB = IE RE + VBE = 1.85 × 2.2 + 0.7 = 4.8 V IC = αIE = 0.99 × 1.85 = 1.84 mA IC 1.84 gm = = 73.4 mA/V = VT 0.025 β 100 rπ = = 1.36 k = gm 73.4 Rin = R1 R2 rπ = 47 24 1.36 = 1.25 k Rin 1.25 vπ = = = 0.385 V/V v sig Rin + Rsig 1.25 + 2 For an overall gain of −40 V/V, 40 vo = −104 V/V =− vπ 0.385 But vo = −gm (RC RL) vπ −104 = −73.4 (RC 2) which is slightly higher than the required gain, and we will obtain VC = 15 − 5.1 × 1.84 = 5.6 V which allows for only 1.2-V negative signal swing. Assuming that all transistors are operating in the active mode and that β 1, so that we can neglect all base currents, we see that the current I through Q1 will flow through the two-output mirror Q3 , Q4 , and Q5 . (4) If Q1 and Q2 are diode connected, then (6) If Q1 and Q3 are diode connected, Weff = 10 + 40 = 50 μm, so that 20 = 40 μA I2 = 100 μA 50 So three different currents are obtained with double-diode connects. Thus, Req ≡ Vx = 1 k Ix Now, if R4 is raised to 1.2 k, the symmetry will be broken. R2 = 100 k R1 = 100 k 9 R3 = 5 k 2.93 IB1 = 2 ± 0.1, μA, VOS = 0 IB2 = 2 ± 0.1, μA R3 IB1 − IB2 R1 C1 R1 VO = −IB2 R3 + R2 R2 From Eq. (2.38): Thus, R2 VO = IB1 R2 − IB2 R3 1 + R1 C2 (1) R3 The maximum value of VO is obtained when IB1 = 2.1 μA and IB2 = 1.9 μA, 100 VOmax = 2.1 × 100 − 1.9 × 5 1 + 100/9 = 210 − 95 = 115 mV The minimum value of VO is obtained when IB1 = 1.9 μA and IB2 = 2.1 μA, R2 = R3 = 100 k 1+ R2 = 100 R1 VOmin = 1.9 × 100 − 2.1 × 5 × 10 = 190 − 105 = 85 mV Thus the dc offset at the output will be in the range of 85 mV to 115 mV. P4.26(a), we see that (c) Refer to Fig. ⇒ R = 100 k 1 = 10 μF C= 100 × 103 When a dc voltage of −1 V is applied, a dc current of 1 V/100 k = 0.01 mA will flow as shown in the figure below. (3.34) and (3.35): Vp 14.9 V iDav = IL 1 + π , , where IL = 2Vr 100 √ Vp = 12 2 − 2 × 0.8, and Vr = 1 V; thus iDmax = I 1 + 2π iD = IS ev D /VT iD = e(v D −0.7)/V T 1 mA iD = v D = VT ln + 0.7 V 1 mA For v I = 10 mV, v O = v I = 10 mV It is an ideal op amp, so i+ = i− = 0. P6.80. The circuit will work properly as long as the op amp does not saturate (i.e., as long as VO ≤ −10 V). P5.52(a) with the 10-μA current source replaced with a 400-k resistor. P6.111(a): v o1 10 10 Av o ≡ = = = 0.99 V/V 1 1 vi 10 + 10 + gm 10 1 Ro = 10 k = 0.1 10 = 99 gm (b) Refer to Fig. 2ID 2 × 0.3 = 3 mA/V = (b) gm1 = gm2 = VOV 0.2 RD1 = RD2 = 10 k RL = 10 k Chapter 6–23 This figure belongs to Problem 6.62. The 6.4 From Eq. (6.18): | Av max | = B B Thus, −14 = −k n RD × 0.25 ⇒ k n RD = 56 To obtain a gain of −12 V/V at point Q: −12 = −k n RD VOV Q = −56VOV Q Thus, 12 VOV Q = = 0.214 V 56 To obtain the required VDS Q , we use Eq. (6.17), VDD − VDS Q Av = − VOV Q /2 2 − VDS Q −12 = − 0.214/2 ⇒ VDS = 0.714 V Q 6.5 RD = 20 k k n = 200 μA/V2 VRD = 1.5 V VGS = 0.7 V Av = −10 V/V Av = −k n VOV RD 1 2 VRD = ID RD = k n VOV RD 2 −2 −10 Av = = VRD VOV 1.5 ∴ VOV = 0.30 V Vt = VGS −VOV = 0.40 V Av −10 kn = = VOV RD −0.3 × 20 = 1.67 mA/V2 Chapter 6–2 k n = k n ∴ W = 1.67 mA/V2 L remains in saturation is 1.61 V and the corresponding output voltage is 0.61 V. (b) The amplifier small-signal equivalent-circuit model is shown in Fig. P4.50. The current I will split equally between Q1 and Q2 . (2) and (3), respectively, in Eq. (1) and equating Gv to 50. 5 V IE3 IC4 10 k 30 k Supernode V + 0.2 V – 0.5 Q3 IB3 10 k V – 0.5 V I Q4 20 k V – 0.7 10 k IE4 (c) Chapter 4–27 VC4 = V − 0.5 = 1.54 V Thus, Next we determine all currents utilizing Eqs. (c) If both W and L are halved, k n will remain unchanged and rDS will vary in the original range of 2.5 k to 125 . Q1 off Ex: 4.29 Refer to the circuit in Fig. = 0.0495 rad v O,avg Conduction ends at π − θ . 9.3. s s+ 1 CC2 (RD + RL) 1 2πCC2 (RD + RL) fP3 = 1 = 8.84 Hz 2π × 10 × 10−6 × 1.8 × 103 AM = − RG × gm (RD RL) RG + Rsig where where RG = RG1 RG2 = 47 M 10 M RD = 10 k and RL = 10 k = 8.246 M To make fP3 ≤ 10 Hz, Rsig = 100 k, gm = 5 mA/V, RD = 4.7 k and RL = 10 k. 6.57(b)] Exercise 6–11 50 × 20(88) 50 + 50 Rin = RB1 RB2 [(β + 1)(re + Re)] = Thus, = 40 V/V 10 = 182 100 [101(0.05 + Re)] VT = where we have substituted re = IE 25 = 50 . ⇒ −12 V ≤ v Icm ≤ 12 V This circuit allows for a much larger range of v Icm . To simplify our solution, we observe that this circuit is that in Fig. 6.26. τC 1 = CC 1 [Rsig + (RB rπ)] = 1 × 10−6 [5 + (100 2.5)] × 103 = 7.44 ms RB Rsig τCE = CE RE re + β +1 β = gm rπ = 40 × 2.5 = 100 re 1/gm = 25 100 5 −6 × 103 5 0.025 + τCE = 1 × 10 101 τCE = 0.071 ms τC 2 = CC 2 (RC + RL) = 1 × 10−6 (8 + 5) × 103 = 13 ms Ex: 9.4 gm = 2k n (W/L)ID = 2 × 0.16 × (10/1) × 0.1 = 0.566 mA/V gm fT = 2π(Cgs + Cgd) = 0.566 × 10−3 2π(24.72 + 1.72) × 10−15 fT = 3.4 GHz Ex: 9.5 Cde = τF gm where τF = 20 ps gm = IC 1 mA = = 40 mA/V VT 0.025 V Exercise 9–2 Thus, fH = Cde = 20 × 10−12 × 40 × 10−3 = 0.8 pF 1 2πCin (Rsig RG) 1 2π × 4.26 × 10−12 (0.01 4.7) × 106 Cje 2Cje 0 = = 2 × 20 = 40 f F = 3.7 MHz Cπ = Cde + Cje = 0.8 + 0.04 = 0.84 pF 1 × 106 = 20 ⇒ Cin = 1.625 pF = 0.33 = 12 f F 2 0.5 gm fT = 2π(Cπ + Cμ) 1+ 40 × 10−3 = 7.47 GHz 2π(0.84 + 0.012) × 10−12 Ex: 9.6 | hfe | = 10 at f = 50 MHz Thus, fT = 10 × 50 = 500 MHz gm Cπ + Cμ = 2πfT = 40 × 10−3 2π × 500 × 106 = 12.7 pF Cπ = 12.7 − 2 = 10.7 pF Cin = Cgs + Cgd (1 + gm RL) 1.625 = 1 + Cgd (1 + 7.14) ⇒ Cgd = 0.08 pF Ex: 9.10 To reduce the midband gain to half the value found, we reduce RL by the same factor, thus RL = 1.5 k But, RL = ro RC RL 1.5 = 100 8 RL = RL = 1.9 k Cin = Cπ + Cμ (1 + gm RL) = 7 + 1(1 + 40 × 1.5) = 68 pF 10.7 = Cde + 2 fH = ⇒ Cde = 8.7 pF Since Cde is proportional to gm and hence IC , at IC = 0.1 mA, Cde = 0.87 pF and Cπ = 0.87 + 2 = 2.87 pF 4 × 10−3 = 130.7 MHz 2π(2.87 + 2) × 10−12 Ex: 9.8 AM = − =− RG gm RL RG + Rsig 4.7 × 7.14 = −7.12 V/V 4.7 + 0.01 1 2πCin (0.1 4.7) × 106 But, Ex: 9.7 Cπ = Cde + Cje fT = 1 2πCin (Rsig RG) Cμ0 VCB m 1+ V0c Cμ = = Ex: 9.9 fH = = 1 2πCin Rsig 1 2π × 68 × 10−12 × 1.65 × 103 = 1.42 MHz Thus, by accepting a reduction in gain by a factor of 2, the bandwidth is increased by a factor of 1.42/0.754 = 1.9, approximately the same factor as the reduction in gain. 4.5(b) is shown below in Fig. increase), this voltage difference will be independent of temperature! 0.4 i (mA) 0.35 Load line 3.32 R 1 kΩ VDD i v 1V 0.30 0.660 0.664 v (V) 0.67 From this graph we get the operating point IS = 10−15 A = 10−12 mA i = 0.338 mA, v = 0.6635 V Calculate some points Now we compare graphical results with the exponential model. See analysis on figure. This constraint is removed in circuit (b), but the input resistance is finite (2R1). (vo vgs)/R2 R2 R1 vsig vo gmvgs vgs RD ro Figure 2 −R2 /R1 1 + R2 /R1 1+ A Thus, R2 /R1 vo =− 1 + R2 /R1 v sig 1+ gm (RD ro R2)(1 − 1/gm R2) RB = R1 R2 = 15 27 = 9.643 k = IC = Q.E.D Substituting numerical values yields vo = v sig 2/0.5 − 1 + (2/0.5) 1+ 1.07(55 561 2000)(1 − 1/1.07 × 2000) = − 4 5 1+ 52.6 0.99(5.357 − 0.7) = 1.85 mA 9.643 2.4 + 101 gm = IC 1.85 mA = 74 mA/V = VT 0.025 V rπ = β 100 = = 1.35 k gm 74 Replacing the BJT with its hybrid-π model results in the equivalent circuit shown at the bottom of the page: Rin = R1 R2 rπ = RB rπ = 9.643 1.35 = 1.18 k Rin vπ 1.18 = = 0.371 V/V = v sig Rin + Rsig 1.18 + 2 = −3.65 V/V vo = −gm (RC RL) vπ Note that the gain is nearly equal to −R2 /R1 = − 4, which is the gain of an op amp connected in the inverting configuration. vi VG1 = VDD − VSG1 = VDD − |Vtp | − |VOV | = 1.8 − 0.4 − 0.2 = 1.2 V 5 mV 0 t VG2 = VS2 − VSG2 = 1.6 − 0.4 − 0.2 = 1.0 V v1 VG3 = VS3 − VSG3 50 mV = 1.4 − 0.4 − 0.2 = 0.8 V 0 t v2 -1 V All transistors carry the same ID = 0.2 mA and operate at the same value of |VOV | = 0.2 V. However, Q3 , which has the same VGS as Q1 but has 10 times the width, will have a drain current 10 times larger than Q1 . P7.86. 7.40 with its T model while neglecting ro results in the circuit shown below. Figure 2 Chapter 7–9 7.22 Refer to Fig. Gv = Gv o 6.78 IC = 2 mA re = Rsig 10,000 = 12.5 + β +1 101 VT VT 25 = = 12.5 IE IC 2 For RL = 250 , RL Gv = Gv o RL + Rout 250 =1× = 0.69 V/V 250 + 111.5 (a) Rin = (β + 1) (re + RL) = 101 × (12.5 + 500) = 51.76 k Rin 51.76 vb = v sig Rin + Rsig 51.76 + 10 6.79 Rout = re + = 0.84 V/V 5000 β +1 10,000 250 = re + β +1 150 = re + vb vo vo = × v sig v sig vb = 0.84 × Rsig β +1 RL RL + re Subtracting Eq. (1) from Eq. (2), we have 5000 β +1 β + 1 = 50 0.5 = 0.84 × 0.5 + 0.0125 100 = = 0.82 V/V Substituting in Eq. (1) yields (b) 5000 50 ⇒ re = 50 RL Gv = Rsig RL + re + β +1 1000 = 0.8 V/V = 10, 000 1000 + 50 + 50 150 = re + Rsig ai B i re vsig RL Rin vbe vo 6.80 (a) Refer to Fig. From the table we see that gain of 50 is obtained for IC between 0.2 and 0.5 mA and also for IC above 1.25 mA. 8.13(a), 1 W 2 for all NMOS VOV Since ID = μn Cox 2 L transistors, W W W W = = = L 1 L 2 L 3 L 4 2ID 2(100 μA) = = 12.5 2 μn Cox VOV 400 μA/V2 (0.2 V)2 W W W W = = = L 5 L 6 L 7 L 8 = 2ID 2(100 μA) = = 50 2 μp Cox VOV 100 μA/V2 (0.2 V)2 For all transistors, gm = |ID | (0.1 mA) (2) = 1 mA/V = |VOV | /2 (0.2 V) From Fig. μn = 450 cm2 /V · S Ex: 5.6 VA = VA L = 50 × 0.8 = 40 V k n = μn Cox = 388 μA/V2 λ= VOV = (v GS − Vt) = 0.5 V 1 W W = k n VOV ⇒ = 5.15 gDS = 1 k L L L = 0.18 μm, so W = 0.93 μm Ex: 5.2 Cox = ox 34.5 pF/m = 8.6 fF/μm2 = tox 4 nm μn = 450 cm2 /V · s k n = μn Cox = 387 μA/V2 ID = 1 W 2 W k V = 0.3 mA, = 20 2 n L OV L ∴ V OV = 0.28 V VDS, min = VOV = 0.28 V, for saturation 1 = 0.025 V−1 VA VDS = 1 V > VOV = 0.5 V ⇒ Saturation: I D = 1 W 2 k V (1 + λVDS) 2 n L OV 1 16 × 200 × × 0.52 (1 + 0.025 × 1) 2 0.8 = 0.51 mA VA 40 = = 80 k ro = ID 0.5 ID = where ID is the value of ID without channel-length modulation taken into account. 0.5 = 0.05 mA ∴ id = 10 and i = 2id = 0.1 mA. Lp ND Dn Ln NA Dp ∴ IS ∼ = Aqn2i Lp ND Ex: 1.35 IS = Aqn2i Dp Dn + Lp ND Ln NA = 10−4 × 1.6 × 10−19 × (1.5 × 1010)2 ⎛ ⎜ ×⎜ ⎝ 10 5 × 10−4 × + 16 10 2 ⎞ ⎟ 18 ⎟ −4 18 ⎠ 10 × 10 × 10 = 1.46 × 10−14 A I = IS (eV /V T − 1) −3) IS eV /V T = 1.45 × 10−14 e0.605/(25.9×10 = 0.2 mA 2s q Ex: 1.36 W = = 2 × 1.04 × 10−12 1.6 × 10−19 1 1 + NA ND 1 1018 = = 3.2 pF Equation (1.71), Cj0 Cj = VR 1+ V0 3.2 × 10−12 = 2 1+ 0.814 + 1 (V0 − VF) (0.814 − 0.605) 1016 = 1.66 × 10−5 cm = 0.166 μm Ex: 1.37 W = Ex: 1.38 Equation (1.72), q N N 1 s A D Cj0 = A 2 NA + ND V0 1.04 × 10−12 × 1.6 × 10−19 = 10−4 2 1018 × 1016 1 0.814 1018 + 1016 = 1.72 pF 2s q 2 × 1.04 × 10−12 1.6 × 10−19 1 1 + NA ND 1 1018 + (V0 + VR) 1 1016 Dp Dn + Lp ND Ln NA (0.814 + 2) Ex: 1.39 Cd = d dQ = (τ T I) dV dV d [τ T × IS (eV /V T − 1)] dV d (eV /V T − 1) = τ T IS dV 1 V /V T e = τ T IS VT τT = × IS eV /V T VT τT ∼ I = VT = Exercise 1–8 Ex: 1.40 Equation (1.75), τp = ND = 1016 /cm3 L2p Dp Assuming NA ND , −4 2 (5 × 10) 10 = 25 ns = In Example 1.10, NA = 1018 /cm3 , Equation (1.81), τT I Cd = VT τ T τ p = 25 ns 25 × 10−9 ∴ Cd = 0.1 × 10−3 25.9 × 10−3 = 96.5 pF Chapter 1–1 (e) P = I 2 R ⇒ I = P/R I = 1000 mW/1 k = 31.6 mA 5V V = = 5 mA R 1 k 5V V = = 5 k (b) R = I 1 mA (c) V = IR = 0.1 mA × 10 k = 1 V 1.1 (a) I = V = IR = 31.6 mA × 1 k = 31.6 V 1V V = = 0.01 A = 10 mA (d) I = R 100 Note: Volts, milliamps, and kilohms constitute a consistent set of units. P4.55(b). Thus VGS4 = VGS3 = VGS1 = 2.5 V Thus, VSGP + VGSN = 3 √ (3 + 1)VOVN + 1 = 3 ⇒ VOVN = 0.732 V VOVP = 1.268 V V2 = 5 − VGS4 = 2.5 V This is equal to the voltage at the gate of Q3 ; thus Q3 is indeed operating in saturation, as assumed. At v I = −2.5 V the diode begins to conduct and its current reaches 1 mA at v I = −1.3 V (corresponding to v O = −2.3 V). P5.52(f). The required value of IC is found by substituting for ro and 1/gm from Eqs. Thus, 4.41 iC (mA) Temperature coefficient of VE R2 =− 1+ × −2.2 R1 = −11 × −2.2 = +24.2 mV/◦ C At 75◦ C, which is a temperature increase of 50◦ C, 1.3 1.1 VA 0 5 0.3 10 15 v CE (V) VE = −8.16 + 24.2 × 50 = −6.95 V As a check on our assumption of constant IE , let us find the value of IE at 75◦ C: I1 (75◦ C) = = VBE (75◦ C) R1 0.68 − 2.2 × 10−3 × 50 6.8 Slope of iC -v CE line corresponding to v BE = 710 mV is 0.2 mA 1.3 − 1.1 = = 0.02 mA/V Slope = 15 − 5 10 V Near saturation, VCE = 0.3 V, thus iC = 1.1 − 0.02 × (5 − 0.3) = 1.006 1 mA iC will be 1.2 mA at, = 0.084 mA IE (75◦ C) = I − I1 (75◦ C) = 1.1 − 0.084 = 1.016 mA which is reasonably close to the assumed value of 1 mA. VC1 = V2 − VD2 = 6.2 − 0.7 = 5.5 V VE2 = V2 = 6.2 V 9 − 6.2 = 28 mA 100 4.62 (a) Consider first the case β = ∞ and R open circuited. These colleagues and friends worked diligently to ensure that the 2,030 solutions are free of error. For L = 0.5 μm and μn = 450 cm2 /V·s, Cgd = WLov Cox = 20 × 0.05 × 4.3 we have = 4.3 fF VOV = 0.2 V ⇒ fT = Csb0 Csb = | VSB | 1+ V0 = 20 1 1+ 0.7 = 12.8 fF Cdb0 Cdb = | VDB | 1+ V0 = 20 = 9.4 fF 2.5 1+ 0.7 gm fT = 2π(Cgs + Cgd) = 1.3 × 10−3 = 3.1 GHz 2π(61.6 + 4.3) × 10−15 (1) 3 × 450 × 108 × 0.2 4π × 0.52 = 5.73 GHz VOV = 0.4 V ⇒ fT = 3 × 450 × 108 × 0.4 4π × 0.52 = 11.46 GHz 9.15 fT = gm 2π(Cgs + Cgd) For Cgs Cgd gm fT 2πCgs (1) 2 WLCox + WLov Cox 3 If the overlap component (WLov Cox) is small, we get Cgs = Cgs 2 WLCox 3 (2) Chapter 9–8 9.17 fT = The transconductance gm is given by W ID gm = 2μn Cox L (3) where IC 0.5 mA = = 20 mA/V VT 0.025 V gm = Substituting from (2) and (3) into (1), we get W ID 2μn Cox L fT = 2 2π × WLCox 3 1.5 μn ID = Q.E.D. πL 2Cox WL gm 2π(Cπ + Cμ) Cπ = 8 pF Cμ = 1 pF Thus, We observe thatfor a given device, fT is proportional to ID ; thus to obtain faster operation the MOSFET is operated at a higher ID . To reduce the gain to half this value, we use 1 Rs = 2 gm ⇒ Rs = 2 gm 8.19 Refer to Fig. 0.5 mA (c) For RB = 1 k, we assume saturation-mode operation: VB = VE + 0.7 VC = VE + 0.2 5 − (VE + 0.7) = 4.3 − VE IB = 1 5 − (VE + 0.2) IC = = 4.8 − VE 1 VE IE = = VE 1 These values can be substituted into (b) 3 V 3.6 k ∼ 0.5 mA V3 3 0.5 3.6 1.2 V ∼0 IB IE = IB + IC VE 0.7 V to obtain 4.7 k VE = 4.3 − VE + 4.8 − VE I4 0.7 (3) 0.5 mA 4.7 = VE = 3 V VB = 3.7 V 3 V Chapter 4–19 3 V a (d) 3 V (c) 3 1.45 6.2 0.25 mA IE 0.5 mA 3.6 k V8 0.75 0.7 1.45 V 0.75 V ∼ 0 mA V7 3 0.5 3.6 1.2 V 43 k 6.2 k 110 k IB 0 V6 V5 0.7 V 0 V9 3 0.25 10 0.5 V 0.75 V 4.7 k IE 0.7 (−3) 4.7 0.5 mA 3 V 10 k 0.25 mA 3 V 3 V (e) 6 480 0.0125 mA I 3 1.45 IE 0.25 mA 6.2 6.2 k 180 k V11 0.75 0.7 1.45 V V10 3 0.0125 300 0.75 V 0 V12 3 10 0.25 10 k 0.5 V 300 k 0.25 mA 3 V 4.56 (a) 3 V IC a 0.5 0.99 0.5 0.495 mA 3.6 k VB 0.005 43 0.215 V V2 3 0.495 3.6 1.218 V 43 k IB 0.5 101 0.005 mA V1 0.215 0.7 0.915 V 0.5 mA 3 V (a) See solution and answer on the figure, which corresponds to Fig. Thus 1 W 2 VOVN I3 = μn Cox 2 L I3 = (1) (2) Equating Eqs. 200 β = = 0.995 α= β +1 201 IC = α × IE = 0.995 × 10 = 9.95 mA VC = IC RC = 9.95 × 0.1 k = 0.995 V 1 V Replacing the BJT with its hybrid-π model results in the circuit shown below. Also, the signal throughout the amplifier chain never drops below 20 mV (which is greater than the required minimum of 10 mV). Thus, RC vo Q1 vi Q2 ID1 = ID2 = 0.5 mA 1 W 2 VOV ID1,2 = μn Cox 2 L 1 2 × 2.5 × VOV 2 ⇒ VOV = 0.632 V 0.5 = re1 Rin2 re2 v e1,2 re2 1 = = vi re1 + re2 2 αRC vo = v e1,2 re2 VCM = VGS + 1 mA × RSS = Vt + VOV + 1 × RSS = 0.7 + 0.632 + 1 = 2.332 V 2ID 2 × 0.5 = 1.58 mA/V = VOV 0.632 Thus, (b) gm = 1 αRC αRC vo = × = vi 2 re2 2re Ad = gm RD which is identical to the expression found in (a) above. The emitter current becomes 0.23 mA at IE = VB − 0.7 − (−3) = VB + 2.3 1 VC = VE + VCEsat = VB − 0.7 + 0.2 = VB − 0.5 IC = 3 − (VB − 0.5) = 3.5 − VB 1 IB = IE − IC = 2 VB − 1.2 IC 3.5 − VB = =2 IB 2 VB − 1.2 ⇒ VB = +1.18 V VB = −3 + 0.23 × 1 + 0.7 = −2.07 V 4.50 Refer to the circuit in Fig. The circuit can − be analyzed by looking at v + O and v O separately. The voltage across the current source becomes W 2 1 μn Cox VOV 2 L 5 1 2 × VOV 0.1 = × 0.4 × 2 0.4 ⇒ VOV = 0.2 V (a) VCS = 2.5 − VDS − IRS VGS = Vt + VOV = 0.5 + 0.2 = 0.7 ID = (1) To keep VCS at least at 0.5 V, the maximum RS can be found from VS = 0 − VGS = −0.7 V RS = VS − (−1) −0.7 + 1 = 3 k = ID 0.1 RD = 0.7 1 − VD 1 − 0.3 = = 7 k = ID 0.1 0.1 0.5 = 2.5 − 1 − 0.1 × RSmax ⇒ RSmax = 10 k V1 = 2.5 − 0.5 = 2 V (b) VCS = 1 − VDS − IRS − (−1.5) 5.41 = 2.5 − VDS − IRS 1 V which is identical to Eq. (1). (1) W = W1 = 10 μm ⇒ VSG = 1.05 V (2) W = W2 = 20 μm ⇒ VSG = 0.92 V (3) W = W3 = 40 μm ⇒ VSG = 0.82 V (4) W = W1 + W2 = 30 μm ⇒ VSG = 0.86 V (5) W = W2 + W3 = 60 μm ⇒ VSG = 0.78 V (6) W = W1 + W3 = 50 μm ⇒ VSG = 0.80 V 7.6 Refer to the circuit of Fig. vO (V) Figure 3 10 t (s) 6.28 2.79 Each pulse provides a constant current of 1V through the capacitor and thus deposits a R 1V charge of × 10 μs on the capacitor, resulting R in a change of the output voltage of − Figure 2 10−5 1 × 10 × 10−6 = − −3 = −0.01 V RC 10 Therefore a total of 100 pulses are required to cause a change of −1 V in v O (t). If in the CC–CE amplifier of Example 7.7, Rsig = 400 k, Gv becomes Gv = 255 × 0.99 × −160 bias), At VCE = 0, iC = βiB ∴ IC = 50 × 100 = 5 mA (dc bias) Given the base bias current of 50 mA, the dc or bias point of the collector current IC , and voltage VCE can be found from the intersection of the load Chapter 6–8 line and the transistor line L1 of iB = 50 μA. Triode Chapter 5–10 IR ≤ |Vt | Since VDG > 0, the MOSFET is in saturation. It consists of the series connection of 4 parallel diodes and 2 parallel diodes. Thus the overall voltage gain becomes 303.5 2.3 + 0.025 100 = 3378 V/V 152 + 100 Thus, although the output resistance of the original amplifier is much lower than that of the modified one, the overall voltage gain realized when the amplifier is loaded in 100-resistance is much lower than that obtained with the modified design. Ad = gm RD 8.65 VOV 2 ID I = gm gm VOV RD = 2 RD VOV = I /2 I = = 1 k n (W/L) k (W/L) 2 n 0.1 = 0.224 V 0.2 × 10 RD RD VOV = 0.04 = VOS = RD 2 RD For I = 160 μA, we have √ gm = 4 × 0.16 = 0.8 mA/V Ad = 0.8 × 10 = 8 V/V = 0.16 = 0.2 V 0.8 0.2 × 0.02 = 2 mV VOS = 2 For I = 360 μA, we have √ gm = 4 × 0.36 = 1.2 mA/V VOV = 0.224 × 0.04 + 4.5 mV 2 (W/L) = 0.04 = VOS = (W/L) VOV 2 (W/L) 0.224 × 0.04 = 4.5 mV 2 Vt = 5 mV = VOS = Vt = 5 mV = Worst-case VOS = 4.5 + 4.5 + 5 = 14 mV Ad = 1.2 × 10 = 12 V/V 0.36 = 0.3 V 1.2 0.3 × 0.02 = 3 mV VOS = 2 Thus by increasing the bias current, both the gain and the offset voltage increase, and by the same factor (1.5). Ex: 3.16 For a zener diode VZ = VZ0 + IZ rZ 10 = VZ0 + 0.01 × 50 VZ0 = 9.5 V Ex: 3.15 For IZ = 5 mA, 15 V VZ = 9.5 + 0.005 × 50 = 9.75 V For IZ = 20 mA, VZ = 9.5 + 0.02 × 50 = 10.5 V Ex: 3.17 15 V R I 5.6 V a. R2 R1 Acm1 = = 20 log 1 + R2 R1 cm1 Ad 1 CMRR = 20 log A 2.72 (a) Comment: In circuit (a), the first stage amplifies the differential signal and the common-mode signal equally. Thus, Re can be used to tradeoff gain for decreasing fL (that is, increasing the amplifier bandwidth). P7.74(a). 2.92 If the signal source resistance is 15 k, then the resistances can be equalized by adding a 5-k resistor in series with the negative input lead of the op amp: 1.22: io R v2 gmv2 Vi Vo Vi C R v1 = v2 = 1 V v 1 = 1.01 V v 2 = 0.99 V For (a) Vo = Vi ∴ v o = 100 × 5 × 0.02 = 10 V g22 I1 g12 I2 g21V1 V1 1/g11 I2 V2 Ro I1 VI I2 Ri 1/sC 1/sC + R Vo 1 = Vi 1 + sCR ∴ vo = 0 V 1.60 (b) v o = io RL = gm R(v 1 − v 2) Vo (a) io = gm v 1 − gm v 2 C AvoV1 V2 which is of the form shown for the low-pass function in Table 1.2 with K = 1 and ω0 = 1/RC. Q.E.D. E 6.44 Refer to Fig. Observe that combining MOSFETs with BJTs results in Chapter 7–28 circuits superior to those with exclusively MOSFETs or BJTs. The lowest voltage at the output while Q3 remains in saturation is VOmin = VG3 − Vt3 7.75 (a) Refer to the circuit in Fig. (1) and (3) simultaneously, we obtain which meet our specifications. Sat. The circled numbers indicate the order of the analysis steps. From Exercise 1.1, ni at DC gain = Gm (RL Ro) = 10 × (RL 50) T = 350 K = 4.15 × 1011 /cm3 nn = ND = 1017 /cm3 To obtain a dc gain of at least 40 dB (i.e., 100), 10(RL 50) ≥ 100 ni2 pn − = ND ⇒ RL ≥ 12.5 k = ω0 × (4.15 × 1011)2 1017 = 1.72 × 106 /cm3 = CL (RL Ro) 1 = CL (12.5 50) × 103 For ω0 to be a least 2π × 100 × 103 , the highest value allowed for CL is CL = V2 1 = 159.2 pF 2π × 100 × 10 × 103 5 Ex: 1.27 At 300 K, ni = 1.5 × 1010 /cm3 pp = NA Want electron concentration = np = 1.5 × 1010 = 1.5 × 104 /cm3 106 ∴ NA = pp = ni2 np Exercise 1–6 = (1.5 × 1010)2 1.5 × 104 = 1.5 × 10 /cm 16 Dn = μn VT = 1350 × 25.9 × 10−3 = ∼ 35 cm2 /s 3 Dp = μp VT = 480 × 25.9 × 10−3 = 12.4 cm2 /s Ex: 1.28 (a) νn−drift = −μn E Here negative sign indicates that electrons move in a direction opposite to E. 2, we can write 3 V IC I mA I = 101 mA VC = 1.5 = IB RB + VBE 0.7 V IB2 IB IC β 1 = 1 + β IC 2IB RB1 I = IC + IB = IC + RC 2IB IC = 1 mA IB 1.5 = 0.01 × RB + 0.7 RB2 RB = 80 k Figure 2 6.104 Refer to the circuit in Fig. 0.5 M 30 mV rms 10 k vi1 ∼ 1 M 10vi1 vi2 (d) For Rin of 40 k and Ro = 500 , the required value of Av o can be found from 400 V/V = 10 k 100vi2 10 k vi3 1vi3 vo 100 vi3 10 k = 10 × 100 ⇒ 90.9 v i2 10 k + 1 k ⇒ v i3 = 100 mV × 90.9 = 9.09 V 1 Vo = Av o × 40 × 10 1 + 0.05 vo = 1 × 0.833 × 10 × 9.09 × 100 + 10 × 0.833 = 7.6 V Ro = 100 (1 × 10 1 2 400 = 20 1 K Po = 1000 100 × Av o × 40 × 10 1000 + 20rms 7.62 = 0.57 W ⇒ RL 100 which compensated by adding a rotated 1 Po = (4k 1 10 (2 × 10) Thus, VE = −0.76 V IC β +1 101 = IC = 0.2 × IE = α β 100 = 0.202 mA Substituting for IS e (v) × BE /VT in Eqs. v o Vi T ∴ ∠ If we next consider the path for v 1 . When it is, increasing the amplifier bandwidth). Assumed. Figure 1 RL vo Av ovi Chapter 6–22 To determine Av o , we open-circuit RL and use the circuit in Fig. The diode will be conducting 1 mA and exhibiting a drop of 0.7 at v O = 2.3 V. Thus VGS = 3 = 1.5 V 2 V2 = 1.5 V Chapter 5–17 VOV = VGS − Vt = 1.0 V 1 W 2 VOV I1 = ID = μn Cox 2 L = 5.56 Refer to the circuit in Fig. C1 B1, B2 ii vp1 ro1 Rin gm1vp1 C2 rp1 io rp2 vp2 ro2 gm2vp2 Ro Chapter 7–8 7.21 Refer to Fig. P4.31. v be α = v be ic = αie = α re re = gm v be Chapter 6 D2 6.42 The large-signal model of Fig. In circuit (c), no current flows in the 20-k resistor connected between the negative input terminal and ground (because of the virtual ground at the inverting input terminal). C= The resulting low-pass filter will have a 3-dB frequency of 1 1 = f3dB = 2πCRF 2π × 159 × 10−12 × 106 = 1 kHz When a 10-μs, 1-V pulse (see Fig. Observing that the controlled-source gm vπ appears across its control voltage vπ , we can replace it by a resistance 1/gm , as indicated. Thus R 100 Chapter 3–32 iDav = 4.8 × 0.113 = 4.913 A Finally, to obtain the peak diode current, we use iDmax = iCmax + iLmax dv I 11.3 ωC + dt R 11.3 12 + =Cx T /4 R = 100 × 10−6 × 12 × 4 11.3 = −3 1 × 10 11.3 = 4.8 + 0.113 = 4.913 A which is equal to the average value. ∴ v0 = 0 V v A = −12 V = 2.76 A PIV of the diodes Ex: 3.25 √ = VS − VDO = 12 2 − 0.8 = 16.2 V To provide a safety margin, select a diode capable of a peak current of 3.5 to 4A and having a PIV rating of 20 V. 5 V 4 5.5 V Q1 on VCEsat 0.2 V 10 k 4.8 V 10 V 5 10 5.5 0.45 mA 10 1 3 Q2 off 5 V 4.8 mA 1 k 2 Chapter 4–1 4.1 1. i2 R2 10 k i1 For the circuit shown above we have: Rf Rf v1 + v2 vO = − R1 R2 vO RL 1 k Let us choose Rf to be 10 k, then Rf R1 = Rf = 10 k and R2 = = 2 k 5 Ex: 2.8 v 1 is a virtual ground, thus v 1 = 0 V ii = 1 V − v1 1−0 = = 1 mA R1 1 k Assuming an ideal op amp, the current flowing into the negative input terminal of the op amp is zero. P2.30 (redrawn above) provides a constant current through RL that is independent of the value of RL . Also,√we observe that fT is inversely proportional to L WL; thus faster operation is obtained from smaller devices. The result is that v − = v I , v O = 2v − = 2v I , and v A = v O + 0.7. Thus (a) v I = +1 V, v − = +1 V, v O = +2 V, and v A = +2.7 V. Ro = 20k k = vs R 10 k Gm = 60 mA/V vi = vs ⎟ ⎟ ix = i1 + i2 ⎟ ix = v x /Ri + gm v x ⎟ ⎟ ⎟ 1 ⎟ i1 = vi /Ri ⎟ ix = v x + gm Ri ⎟ i2 = gm vi ⎟ ⎟ 1 v ⎟ x ⎟ ⎟ = ⎟ ⎟ = j i 1/R x i + gm vi = gm vi Ri = Rin 1 + gm Rx vi i1 Ri gmvi 10 = 33.3v 2 3 To reduce the gain seen by v 2 from 33.3 to 20, we connect a resistance Rp in parallel with RL , 10 Rp = 2 S1 3 = 0.283 − (−0.4) = 0.683 V 0.283 = 0.683 V in D1 VDD − iD1 RD = 1 − 0.16 × 5 = +0.2 V Note that since v G1 = v id = 0.283 V, Q1 is still operating in saturation, as implicitly assumed. Figure 1 RL vo Av ovi ro (ro rπ) (c) Refer to the circuit in Fig. Thus 10 = 12 × 500 × 500 = 0.2 V 2 VGS = 0.8 + 0.2 = 1 V V4 = 1 V (e) Refer to Fig. Rin = 0.1 RG1 RG2 = 300 k 200 k = 120 k 2ID 2 × 0.5 gm = = 3.33 mA/V = VOV 0.3 VA 50 = 100 k ro = ID 0.5 Rin gm (ro RL) Gv = − Rin + Rsig 120 = −3.33 × (100 5 5) =− 120 + 120 = −4.1 V/V (c) VG = 2 V, v ˆGS = 0.2 V, gm = 2 (a), DC bias: |VOV | = 0.3 V VSG = |Vtp | + |VOV | = 1 V Since VG = 0 V, VS = VSG = +1 V, and 2.5 − 1 = 0.3 mA ID = RS = 1.5 = 5 k ⇒ RS = 0.3 (b) Gv = −gm RD where VD = 2.5 V gm = v ˆgs DTS = 2.5 − | Av |v ˆgs 2ID 2 × 0.3 = = 2 mA/V VOV 0.3 Thus, where −10 = −2RD ⇒ RD = 5 k (b) Av = −gm (RD RL) = 8.1 V/V This figure belongs to Problem 6.109. 1 V 5 V IE 4.61 (a) 5 V 20 k VE IC 10 k IB 1 k VE + 0.7 VE 4 × 0.2 VE − 0.7 VE − 0.2 IB 10 k IC 1 k VE + 0.7 V VE IE 1 k (a) -5 V (b) Assuming saturation-mode operation, the terminal voltages are interrelated as shown in the Figure 4–26 shown in the figure, which corresponds to Fig. Z All diodes and zener are OFF Z 3.86 3.87 (a) 10 k vI v0 1 k vI vO vO D1 D2 (b) 10 k Diodes have 0.7 V drop at 1 mA current vO vI ∴ For diode D1 v0 = e(v O −0.7)/VT (c) v O = 0.7 + VT ln(v O) vI 1 mA vo vI + 10−3 e(v O −0.7)/VT ∴ v I = 1 × 10−3 e(v O −0.7)/VT (c) v O = 0.7 + 10 vI vO 10 1 mA v I = v O + iD = 1 k v I For the different values of vI calculate vO. Choose from these amplifier types: A Ri 1 M B Ri 10 k C Ri 10 k Ro 1 k 1 k Ro 10 k Ro 10 k 10 k 10 V/V Av 1 V/V Ro 10 k Ro 1 k 20 1.49 From the equivalent circuit of the output side of a voltage amplifier [Fig. For a 2-V, 100-μs 10 2V input pulse, a current of 0.02 mA 100 k flows into R and C, causing v O to decrease linearly from its initial value of 0 V according to 2.77 |T | = vO = − = 1 t C −0.02 × 10−3 t = −0.02 × 106 t 1 × 10−9 At t = 100 μs, v O becomes 1 = CR = 1.59 μs CR For Rin = 10 k, R = 10 k, and 2.78 2π × 100 × 103 = 1.59 × 10−6 = 159 pF 104 To limit the dc gain to 40 dB (i.e., 100 V/V), we connect a resistance RF across C (as in Fig. 25 mV = 100 0.25 mA The 0.1-V differential input signal appears across (2re + 2Re), thus 8.36 (a) re = 100 mV = 0.1 mA 200 + 2 × 400 v be = 0.1 × 100 = 10 mV (b) The total emitter current in one transistor is I + ie = 0.35 mA and in the other transistor 2 I − ie = 0.15 mA. P8.110. To obtain saturation-mode operation with VCE = 0.2 V and βforced = 10, we use VCE = 0.3 V IC = βforced × IB VCC − VCE 10 − 0.3 = = 0.97 mA IC = RC 10 = 10 × 0.1 = 1 mA = 0.7 + 0.01 × 10 = 0.8 V IB = 0.97 IC = = 0.194 mA 5 10 VBB = VB + IB RB = 0.7 + 0.194 × 10 = 2.64 V Operation deep in saturation with βforced = 10, we have VCE 0.2 V 10 = 0.98 mA 10 = IB = βforced 10 VBB = VB + IB RB = 0.7 + 0.098 × 10 = 1.68 V The value of RC required can now be found as VCC − VCE IC 10 − 0.2 = 9.8 k 1 Ex: 4.22 Refer to the circuit in Fig. P7.75(b). corresponding peak input signal is v ˆgs = 0.78 0.78 V = = 19.5 mV | Av | 40 Ex: 7.6 To obtain the coordinates of point B, we first use Eq. (6.6) to determine VGS B as v 2k n RD VDD + 1 − 1 VGS B = Vt + k n RD √ 2 × 10 × 20 × 5 + 1 − 1 = 0.5 + 10 × 20 × 5 = 0.5 + 0.22 = 0.72 V The vertical coordinate of point B is VDS B , VDS B = VGS B − Vt = VOV B = 0.22 V VDD − VOV B VOV B /2 2 − VOV B 14 = VOV B /2 ⇒ VOV B = 0.25 V 6.2 VDS B = VOV B = 0.5 V Now, using Eq. (6.15) at point B, we have Av = −k n VOV RD Thus, 1 2 ID B = k n VDS = × 5 × 0.52 = 0.625 mA B 2 2 The value of RD required can now be found as VDD − VDS B RD = ID B 5 − 0.5 = 7.2 k = 0.625 If the transistor is replaced with another having twice the value of k n , then ID B will be twice as large and the required value of RD will be half that used before, that is, 3.6 k. IC IC = 0.5 mA ⇒ gm = (d) Refer to Fig. For v id /2 ≤ VOV √ v id /2 ≤ k = VOV √ v id /2 2 v id /2 1 − I = I VOV VOV √ v Imax = I k 1 − k (1) Thus, ⇒ RD = 4 k For Q1 and Q2 , VICM max = VD1,2 + Vtn VOV 1 W μn Cox V2 2 L 1,2 OV W 1 0.2 = × 0.4 × 0.152 2 L 1,2 W = = 44.4 L 1,2 ID1,2 = V 1 Imax = 2 k(1 − k) 1 2 Q.E.D. (2) and the corresponding value of v id is found from Eq. (2) as v id √ 2 = 2 kVOV Q.E.D. (3) Equations (2) and (3) can be used to evaluate Imax v id max and for various values of k: I /2 VOV For Q3 , W 1 × 0.4 × 0.152 2 L 3 W = = 88.8 L 3 0.4 = k v id max VOV Imax I /2 0.01 0.1 0.2 0.2 0.632 0.894 0.2 0.6 0.8 Since Q3 and Q4 form a current mirror with ID3 = 4ID4 , 1 W We have = 22.2 L 4 4 L 3 8.8 Switching occurs at √ v id = 2VOV VGS4 = VGS3 = Vtn + VOV = 0.4 + 0.15 Thus, 0.55 9 −(−0.9) − 0.55 R= 0.1 = 12.5 k The lower limit on VCM is determined by the need to keep Q3 operating in saturation. For the Widlar current source, use R = 2 k. P4.25(d). Thus, AM = − = −15.8 V/V fP1 = 9.3 Refer to Fig. 5. Since the required IE = 1 mA, the base current I = 0.01 mA. The additional current supplied by the op amp comes from the power supplies (not shown). Observe that as A0 → ∞, ωP → 0. To determine the systematic input offset voltage resulting from the error in the current-transfer ratio of the mirror, we ground the The figure shows a BJT differential amplifier loaded with a Wilson current mirror. 1). 2.20(a). To obtain the short-circuit current gain, we replace the BJT with its T model and short circuit the collector to Chapter 7–20 io kisig Thus, Rout = 500 + (10 25) × 2001 ai i = 14.8 M ro Thus the CB amplifier has a current gain of nearly unity and a very high output resistance: a near-ideal current buffer! re E A more exact value of k can be obtained using Eq. (1): k = 0.975. 7.38. Ex: 7.22 Rop = (gm3 ro3) (ro4 rπ3) and VDD 1.8 V Ron = (gm2 ro2) (ro1 rπ2) I1 2I vi Q1 VG2 Q2 vo I2 1 The maximum values of these resistances are obtained when ro rπ and are given by Ron = (gm2 ro2) rπ2 max Rop = (gm3 ro3) rπ3 max Since gm rπ = β, Ron = β ro2 max Rop = β 3 ro3 max Exercise 7–6 Since Av = −gm1 Ron Rop , |Av max| = gm1 β 2 ro2 β 3 ro3 3.6 1 2 × 387 × VOV 2 0.36 = VOV = 0.227 V 100 = VGS = 0.227 + 0.5 = 0.727 V Ex: 7.24 For the npn transistors, gm1 = 0.2 mA = = 8 mA/V = |VT | 25 mV VOmin = VG3 − Vt3 = VGS4 + VGS3 − Vt3 β 100 = 12.5 k = gm 8 mA/V Thus, rπ 1 = rπ 2 = ro1 = ro2 = |VA | 5V = 25 k = |IC | 0.2 mA Ex: 2.7 VOmin = 2VGS − Vt = 0.5 + 2 × 0.227 = 0.95 V From Fig. 1 below, where β = ∞ and R is open circuited. We will have to increase by factor of 0.54 3 the same factor. Referring to the figure below: = 4 × 0.02 2 × 20 = 1.33 × 10−3 V/V CMRR = 4252.5 or 72.6 dB 8.51 Refer to Fig. Writing a loop equation for the base-emitter circuit results in IB Rsig + VBE + IE RE = 3 IE Rsig + VBE + IE RE = 3 β +1 0.5 + 2.5 + 0.7 + 0.7 = 5.5RE = 3 101 ⇒ RE = 4.6 k VC = VCC − IC RC = 15 − 1 × 6.8 = 8.2 V (b) See figure below. From Fig. i = −isig β 100 = 2.5 k = gm 40 RE = 4.3 k l/ro 1 1 1 + + re ro Rsig Thus, Rout = 100 + (4.3 2.5) × 4001 = 6.4 M At the collector node, we can write io ≈ kisig = i1 − αi For Thus, VC = 10 V kisig = isig 1/ro + (α/re) 1 + 1 1 + + re ro Rsig 5 − 0.7 1 mA 4.3 (1) 10 V 1 k 0.6 k M 1 A very small change indeed! Now ro re and for the case Rsig re , we obtain k =α 1/ro for the case Rsig re , we obtain k =α 1/ro For the case, β α= β +1 β 100 k=α = = 0.99 β +1 101 k Note that current Rout is given by Rout = ro + (Rsig rπ)(1 + gm ro) where VA 50 V ro = = = 500 k IC 0.1 mA IC 0.1 mA = gm = = 4 mA/V VT 0.025 V gm ro = 4 × 500 = 2000 β 100 rπ = = 25 k = gm 4 7.56 Refer to Fig. 1, which indicates the given values. +1.0 +1.0 0 +2.0 Sat. Thus From the circuit we see that vi ie = re + Re Thus, re + Re Rin = 1−α But 1 1−α = β+1 Thus, Rin = (β + 1)(re + Re) re VT 25 mV = 75 IE 0.33 mA Replacing the BJT with its T model results in the following amplifier equivalent circuit. vo2 aie RC ie re vi RE v o1 = vi RE + ro 100 k vi RC RE ie ro vo2 αRC =− vi RE + re For α 1, RE v o Rsig + Rin is ii v sig Rin Q.E.D. v o2 = −aie RC = −α re + re =− vi RE + re vo2 αRC =− vi re + re Then GV Q.E.D. Rsig + Rin RL = 79.4 × VT 25 mV = = 50 IE 0.5 mA 6.55 (a) v i 3.6 = 0.986 V/V = vi 3.6 + 0.05 20 + 100 = 4762 A/A 2 Rin = 0.95 Rin + Rsig Rin = 0.95 Rin + 100 v o2 3.3 = 0.904 V/V =− vi 3.6 + 0.05 = 1.9 M (b) With RL = 2 k, If v o1 is connected to ground, RE will in effect be short-circuited at signal frequencies, and v o2 /v i will become v o2 αRC 3.3 = −66 V/V =− =− vi re 0.05 v o = Av o v i 2 2 + Ro With RL = 1 k, v o = Av o v i 1 1 + Ro The change in v o is 1 2 v o = Av o v i − 2 + Ro 1 + Ro 6.54 See figures below and on next page. Since v 1 must see a gain factor of only 10, which is half that seen by v 2 , we have to reduce the fraction of v 1 that appears at the input of the transconductance amplifier by half that that appears at the input of the v 2 transconductance amplifier. t Chapter 1–11 Note that there are two possible representations of zero: 0000 and 1000. Therefore, to achieve iD desired ro (which is 5 times larger), we should increase L (L = 5 × 1 = 5 μm). VDS = VDD − RD ID Thus, 1.8 − 12.5 × 0.08 = 0.8 V gm RD 25 Design 2: Substituting for gm = k n VOV , we have RD = 17.5 k k n VOV RD 25 = −10 = −0.4 × 10 × 0.2 × RD Exercise 6–2 where k n = 1 mA/V2 , thus vt vt +i = + gm v t ro ro it = VOV RD = 25 (1) Next, consider the bias equation ∴ Req = vt 1 = ≈ ro it gm VGS = VDS = VDD − RD ID Thus, Ex: 6.6 Vt + VOV = VDD − RD ID Substituting Vt = 0.7 V, VDD = 5 V, and VDD 1 1 1 2 2 2 k n VOV = 1 × VOV = VOV 2 2 2 we obtain 1 RD (2) 0.7 + VOV = 5 − 1 RD VOV 2 2 2 Refer to Fig. For kn = 100 n k |VOV |2 2 pL 180 = = W 1 VOV × 0.32 2 L W = 40 L W = 40 × 0.18 = 7.2 μm 5.46 Refer to Fig. Lp ND Ln NA Dp Dn and have approximately Lp Ln = 7.3 × 10−15 A similar values, if NA ND , then the term Dp can be neglected as compared to . v I becomes a horizontal line. (d) Q2 IC2 (b) IE2 = 5 − 0.74 − 0.7 8.2 3.3 + 101 = 1.05 mA IC2 1.04 mA The collector current IC2 and the 5.6-k resistance it feeds can be replaced by a Thévenin equivalent as shown in Fig. P8.104. 1, RG2 VDS = VGS 1 + RG1 3 = 0.95 × 1 + = 2.375 V 2 ⇒ | v ˆo | = VDS − VOV = 2.375 − 0.45 = 1.925 V |v ˆo | = 22 mV |v ˆ i | = 86.5 (c) To determine Rin , refer to Fig. 1.23(a) with the 3-dB frequency f0 = 105 Hz. The high-pass factor 1/(1 + 102 /jf) results in a Bode plot like that in Fig. So Rin = R2 +A vI R2 = RI + ii A+1 2.22 Closed-loop gain G= vO = vI −(R2 /R1) 1 + R2 /R1 1 + A Q.E.D. Chapter 2–5 Gain error = 1 + (R2 /R1) × 100 % G 1 + A 1 1 1 = = R1 R1 Rc 0.1% 1% 10% R2 R2 R2 A 1000 1 + 100 1 + 10 1 + R1 R1 R1 Substituting in Eq. (1), R1 Rc R2 R2 1 + R1 Rc 1+ A 1 R2 Vo =− Vi R1 Gain with resistance R1a R2 To make Ri R1a R1 vI R1 = Rc R2 Vo =− , we have to make Vi R1 +1 VO That is, A R2 R2 + R1 Rc A R1 R1 =1+G+G Rc Rc Which yields R2 R1 R1a R1 + R1a |G| R2 + 1+ R1 A A−G Rc = R1 1+G 2.24 (a) |G| = where we have neglected the small effect of R1a on the denominator. 3 RRL ≤ 2 k R + RL 1.15 For RL = 10 k R ≤ 2.5 k The resulting circuit needs only one additional resistor of 2 k in parallel with RL so that v O = 3.16 × 0.79 V VSG2 = |Vtp | + |VOV | = 0.5 + 0.5 = 1 V. Also, ID = 0.5 mA. VDD = +5 V Q1 = 3 V2 μn Cox 2 L OV 1 V W 1 100 = × 200 × × 0.32 2 L W 1 = 11.1 L 1 μ ID 2 = μp Cox 2 L 2 = W 1 100 = × 0.32 2 L 2 W = 22.2 L 2 ID1 Av = −gm1 (ro1 ro2) = 0.67 mA/V = VOV 0.3 ro1 = ro2 = |VA | L 20 × 0.5 = 100 k ID 0.1 Av = −0.67 × (100 100) = −33.5 V/V 7.39 Refer to Fig. This compensates for the factor 3 in the process transconductance parameter, resulting in k p = k n , and the two transistors are matched. (W/L)2 (W/L)1 7.17 Ais = 4 Since L1 = L2 , then W2 =4 W1 Figure 1 Rin = ro1 1 1 gm1 gm1 Ro 1 Figure 1 shows the current conveyor circuit with Y connected to a voltage V , X fed with a current source I , and Z connected to a voltage VZ that keeps Q5 operating in the active mode. We next draw a circle around the two transistors to define a "supernode." A node equation for the supernode will be figure, which corresponds to Fig. The op amp: R = 0.8ωL = 0.8 × 2πfL = 0.8 × 2π × 50 × (b) From Eq. (3), we obtain τCE = 3.98 ms fL = Thus, (13.2 5) × 1000 CE 3900 83.3 + 121 1 2πCE re 1 1+ Re Re Thus, including Re reduces fL by the factor Re 1+ - 5−0 ± 0.2 mA R R ≥ 25 k From Fig. Observe that at the output node the total signal current is 4id where 1 ro1 ii gm1 id = gm1,2 1 ro1 iosc gm1 Ais ≡ = gm2 1 i id = ro1 gm1 = + v id 2 I v id 2VOV | This figure belongs to Problem 8.115. 5 e d r a , Series Editor H EDITION A l l e n and H 8,605 2,657 44MB Read more SEDRA/SMITH INSTRUCTOR'S SOLUTIONS MANUAL FOR Microelectronic Circuits INTERNATIONAL SEVENTH EDITION Adel S. Since Q1 and Q2 are now operating at equal VDS , we estimate IO = IREF = 180 μA. (Equivalent Chapter 6–40 To remain in saturation, v ˆDS ≥ v ˆGS − Vt 2.5 − 8.1v ˆgs ≥ 2 + v ˆgs − 0.7 This is satisfied with equality at 2.5 − 1.3 = 0.132 V v ˆgs = 9.1 The corresponding value of v ˆsig is 120 + 120 = 2 × 0.132 = 0.264 V v ˆsig = 120 The corresponding amplitude at the output will be | Gv |v ˆsig = 4.1 × 0.264 = 1.08 V Figure 1 VDD = 2.5 V is higher than VG − Vt = 1.3 V by 1.2 V.) 1 2 ID = k n VDS 2 VOV 2 1 0.5 = k n × 0.52 ⇒ k n = 11.1 mA/V2 (b) To be able to double the signal without leaving saturation, we must reduce v ˆgs to half of what would be its new value; that is, we must keep v ˆgs unchanged. v O = 10 V 10 V = 10 mA iL = 1 mA Current supplied by the source is 0. Since VC = −4 V is lower than VB = −2.7 V, the transistor is operating in the active mode. (a) V1 = VDS = VGS = 1 V (b) (V1 = +4) VDS = 1 V − 1 (c) V3 = VSD = VSG = 1 V (d) V4 = +1.25 − VSG = 1.25 − 1 = 0.25 V 5.38 Case a, assume, sat, Now place a resistor R in series with the drain. 2.11: The value of R can be selected (arbitrarily but conveniently) as R = 10 k. If we add a resistor in series with the capacitor to limit the high-frequency gain of the differentiator to 100, the circuit would be: R C R1 Vi Vo 10−3 s = 100 × 103 × 10 × 10−9 ∴ Since the desired integration time constant Vo At high frequencies the capacitor C acts like a short circuit. VDD 1.2 V Q3 Q4 Q6 Q1 Q2 vo Rin VICM 200 A Q8 Q5 Q7 Chapter 8–40 1 W |VOV |2 kp 2 L 3,4 W = 178 L 3,4 Thus ID3,4 = 0.65 V ≤ VICM ≤ 1.05 V Note that the input dc voltage in part (a) falls outside the allowable range of VICM ! Thus, part (a) should have specified a VICM greater than 0.65 V. Rsig vo vsig rp vp gmvp This figure belongs to Problem 6.119. 2 we see that re (10 2) v e = ie + ie 10 re + ie re v be = v e + ie re = ie (10 2) 1 + 10 re ii = (1 − α)ie + ie 10 re ie ii = + ie = β + 1 10 re (β + 1)re (β + 1)(10 2) 1 + 10 re = 101 × (10 2) × (1 + 0.00145) + 101 × 0.00145 1 + 101 × 0.00145 168.577 + 1.4645 = 148.3 k 1 + 0.14645 vb Rin = 148.3 = ro = 0.937 × sig Rin + Rsig 148.3 + 10 = re 10 + (10 2) re vo 10 = = re vb vb ie 1 + (10 2) + ie re 1.00145 × (10 2) = 1.00145 × (10 2) + 0.0145 = 0.991 V/V vo Gv = = 0.937 × 0.991 = 0.93 V/V sig = = 20 101 × 2.0145 = 18.21 k which is greatly reduced because of the absence of bootstrapping. R2 High-frequency gain (s → ∞) = − R1 ω1 = 1 C1 R1 and (a) For ω ω1 , For a high-frequency input resistance of 1 k, we select R1 = 1 k. 1 2 k n VOV 2 1 2 0.5 = × 4VOV 2 ⇒ VOV = 0.5 V The voltage gain ID = Exercise 6–10 Thus, VGS = Vt + VOV = 1 + 0.5 = 1.5 V We now can obtain the dc voltage required at the gate, VG = VS + VGS = 3.5 + 1.5 = 5 V Using a current of 2 μA in the voltage divider, we have 5V = 2.5 M RG2 = 2 μA The voltage drop across RG1 is 10 V, thus RG1 = 10 V = 5 M 2 μA This completes the bias design. 2.83 R 20 k i i vI The average value of the output is zero. To determine Rin , we simplify the circuit as shown in Fig. Chapter 7–2 This figure belongs to Problem 7.5. To find VSG , we use the following for the diode-connected transistor(s): 1 W ID = μp Cox (VSG − |Vtp |)2 2 L VDD Q1 Q2 I1 Q3 I2 I3 IREF and substitute ID = IREF = 100 μA. The resulting VBE will be 0.699 V and 0.721 V, respectively. P5.26 and let VD1 = 2 V and VD2 = 2.5 V. 1 0.025 vs = vs × 2 0.025 + 103 I ⇒ I = 25 μA iD = IS ev /VT iD2 = e(V2 −V1)/VT = ev /VT iD1 For +5 mV change we obtain iD2 = e5/25 = 1.221 iD1 % change 1.221 − 1 iD2 − iD1 × 100 = × 100 = iD1 1 = 22.1% For -5 mV change we obtain iD2 = e−5/25 = 0.818 iD1 0.818 − 1 iD2 − iD1 × 100 × 100 = % change = iD1 1 = −18.1% vo For v o = 3.46 As shown in Problem 3.45, VT 0.025 vo = = vi VT + RS I 0.025 + 104 I Here RS = 10 k (1) The current changes are limited ±10%. This manual has greatly benefited from the careful work of the accuracy checkers listed below. 9.3(b). At v I = 3.5 V, the diode begins to conduct. Now, to allow for 0.8-V negative signal swing, we must have VD = 0 V and 5−0 = 12.5 k 0.4 2ID 2 × 0.4 = 2 mA/V (b) gm = = VOV 0.4 VA 40 = = 100 k ro = ID 0.4 (c) If terminal Z is connected to ground, the circuit becomes a CS amplifier, vy RG = × −gm (ro RD RL) Gv = − v sig RG + Rsig RD = 10 × 2 × (100 12.5 10) 10 + 1 = −9.6 V/V=− Chapter 6–42 (d) If terminal Y is grounded, the circuit becomes a CD or source-follower amplifier: vz (RS ro) = 1 vx (RS ro) + gm (9.5 100) = 0.946 V/V = 1 (9.5 100) + 2 Looking into terminal Z, we see Ro : 1 Ro = RS ro gm 1 = 9.5 100 = 473 2 (e) If X is grounded, the circuit becomes a CG amplifier. |VOV | = 1.5 − 0.8 − 0.5 = 0.2 V Thus, 1 W 0.2 = × 0.1 × × 0.22 2 L 6,3 W W = = = 100 L 3 L 6 Transistor W/L I D (mA) |V GS |(V) Each of Q4 and Q5 is conducting a dc current of (I /2) while Q7 is conducting a dc current IREF = I . To start with, we minimize L by using the smallest feature size, 5.3 With v DS small, compared to VOV , Eq. (5.13a) applies: L = 0.18 μm rDS 1 = W (μn Cox) (VOV) L rDS = 1 k n (W/L) (v GS − Vt) rDS = 1 k n (W/L) v OV (a) VOV is doubled → rDS is halved. Thus, the differential half circuit will be as shown in the figure, and v od RD = Rs 1 v id + gm 2 1 ro3 RD = gm3 Ad ≡ and the differential gain of the amplifier in Fig. This is the price paid for doubling Rid . For v I < 0, the diode is cut off, zero current flows through R, and v O = 0. The slope at v OV = VOV is d (iD /k n) = VOV d v OV v OV =VOV Replacing k n by k p and v OV by |v OV | adapts this graph to PMOS transistors. See the circuit below: VS 15 V R VO − 8.74 0.04 VS = 13.5 V 170 mV 1.5 V 20 mA VO IZmin 5 mA IZ RL Chapter 3–24 R≤ 15 − VZ0 20 + 5 where we have used the minimum value of VS , the maximum value of load current, and the minimum required value of zener diode current, and we assumed that at this current VZ VZ0 . Rsig 5 k vsig rp 25 k vp gmvp gm 4 mA/V ro 1 M vo RL 100 k Chapter 7–11 7.27 A0 = 2VA 2VA L = VOV VOV VA = 5 × 0.3 = 1.5 V ro = 2×5×L 0.2 ⇒ L = 0.4 μm 20 = A0 = gm ro = 1 × 15 = 15 V/V 1 W 2 μn Cox VOV 2 L W 1 × 0.22 100 = × 387 × 2 L W = = 13 ⇒ W = 3.9 μm L ID = 2ID 2I = gm = VOV VOV 2I 0.2 = I = 0.2 mA 1 W 2 VOV ID = μn Cox 2 L 2= 0.2 = VA 1.5 V = 15 k = ID 0.1 mA 7.31 gm = W 1 × 0.4 × × 0.04 2 L 2ID 2 × 0.1 = 0.4 mA/V = VOV 0.5 W = 25 = L From Table J.1 (Appendix J), we find that for the 0.5-μm process |VA | = 20 V/μm. Q5 Q3 id Q4 id vid 2 Q1 id Q6 2id id Q2 vid 2 vo 4vid 2id 0V Q7 Q8 This figure belongs to Problem 8.116, part (c). Thus, 4.3 = 8.6 k 0.5 Rin gm (RC RL) Gv = Rin + Rsig RE = Ex: 6.44 Refer to Fig. That is, IO = VO 1V = 0.01IO ⇒ ro2 ro2 = 0.01 × 100 μA ro2 = 1V = 1 M 1 μA ro2 = VA × L 20 × L = 1 M = IO 100 μA ⇒L= 100 V = 5 μm 20 V/ μm To keep VOV of the matched transistors the same W of the transistor should as that in Example 7.1, L remain the same. 4.30(b). Thus the maximum value of vo is 3.3 − 0.224 = 3.076 V. ⇒ ωH = 0.64ωP 1 The approximate value using Eq. (9.77) is 2 ωP 1 ωH 1 = √ ωP2 1 2 Ex: 9.16 | AM | = gm RL = 1.25 × 10 = 12.5 V/V = 0.71ωP 1 GB = | AM | fH For k = 2, the exact value of ωH is obtained from ωH 2 ωH 2 1+ 2= 1+ ωP 1 2ωP 1 = 12.5 × 135.5 = 1.69 GHz =1+ 5 ωH 4 ωP 1 2 +1 ωH 4 ωP 1 4 Ex: 9.17 | AM | = Rgs = 10 k 1 × 12.5 = 6.25 V/V 2 Exercise 9–4 (1 + gm RL) + RL Rgd = Rsig = 10(1 + 6.25) + 5 = 77.5 k RCL = RL = 5 k τgs = Cgs Rgs = 20 × 10−15 × 10 × 103 = 200 ps τgd = Cgd Rgd = 5×10−15 ×77.5×103 = 387.5 ps τCL = CL RCL = 25 × 10−15 × 5 × 103 = 125 ps τH = τgs + τgd + τCL Ex: 9.19 (a) gm = 40 mA/V rπ = 200 = 5 k 40 ron = VAn 130 = = 130 k I 1 rop = |VAp | 50 = = 50 k I 1 RL = ron rop = 130 50 = 36.1 k AM = − = 200 + 387.5 + 125 = 712.5 ps = − 1 fH = 2πτH rπ gm RL rπ + rx + Rsig 5 × 40 × 36.1 5 + 0.2 + 36 = −175 V/V 1 = = 223.4 MHz 2π × 712.5 × 10−12 (b) Cin = Cπ + Cμ (1 + gm RL) GB = 6.25 × 223.4 = 1.4 GHz = 16 + 0.3(1 + 40 × 36.1) Ex: 9.18 gm = 2μn Cox = 450 pF W ID L Rsig = rπ (rx + Rsig) Since ID is increased by a factor of 4, gm doubles: = 5 (0.2 + 36) = 4.39 k gm = 2 × 1.25 = 2.5 mA/V fH = Since RL is ro /2, increasing ID by a factor of four results in ro and hence RL decreasing by a factor of 4, thus RL = 1 × 10 = 2.5 k 4 | AM | = gm RL = 2.5 × 2.5 = 6.25 V/V = 10 k Rgs = Rsig Rgd = Rsig (1 + gm RL) + RL = 10(1 + 6.25) + 2.5 = 1 2πCin Rsig 1 2π × 450 × 10−12 × 4.39 × 103 = 80.6 kHz (c) Rπ = Rsig = 4.39 k Rμ = Rsig (1 + gm RL) + RL = 4.39(1 + 40 × 36.1) + 36.1 = 6.38 M = 75 k RCL = 36.1 k RCL = RL = 2.5 k τH = Cπ + Cμ Rμ + CL RCL τH = τgs + τgd + τCL = 16 × 4.39 + 0.3 × 6.38 × 103 + 5 × 36.1 = Cgs Rsig + Cgd Rgd + CL RCL = 70.2 + 1914 + 180.5 = 20 × 10−15 × 10 × 103 + 5 × 10−15 × 75 = 2164.7 ns × 103 + 25 × 10−15 × 2.5 × 103 = 200 + 375 + 62.5 = 637.5 ps fH = 1 = 250 MHz 2π × 637.5 × 10−12 GB = | AM | fH = 6.25 × 250 = 1.56 GHz fH = 1 2π × 2164.7 × 10−9 = 73.5 kHz gm (d) fZ = 2πCμ = 40 × 10−3 = 21.2 GHz 2π × 0.3 × 10−12 (e) GB = 175 × 73.5 = 12.9 MHz Exercise 9–5 Ex: 9.20 Rin = R L + ro 1 + gm ro 500 + 20 = = 20 k 1 + 25 Gv = RL 500 = 16.7 V/V = Rsig + Rin 10 + 20 τH = Cgs Rsig + Cgd × 21Rsig = Cgs Rsig + 0.25Cgs × 21Rsig = 6.25Cgs Rsig 1 2π × 6.25Cgs Rsig fH = Rgs = Rsig Rin = 10 20 = 6.7 k For the cascode amplifier, Rgd = RL Ro τH Rsig [Cgs 1 + Cgd 1 (1 + gm1 Rd 1)] = 500 280 = 179.5 k where τH = Cgs Rgs + (Cgd + CL)Rgd Rd 1 = ro 1 Rin2 = ro = 20 × 10−15 × 6.7 × 103 + (5 + 25) × 10−15 × 179.5 × 103 = 134 + 5385 = 5519 ps 1 = 28.8 MHz fH = 2π × 5519 × 10−12 2 ro 2 gm = ro = 2 gm + ro gm ro 2ro 2ro = = 2 + gm ro 2 + 40 21 gm ro τH = Cgs Rsig 1 + 0.25 1 + 21 40 = Cgs Rsig 1 + 0.25 1 + 21 = Thus, while the midband gain has been increased substantially (by a factor of 9.7), the bandwidth has been substantially lowered (by a factor of 9.4). We compute the nominal value of IE from 4.3 = 0.96 mA 50 4+ 101 We utilize Eqs. vo 100 k ie ie 5 k 4.5 − 0.7 20 2+ β +1 3.8 = 1.73 mA 20 2+ 101 IC = αIE = 0.99 × 1.73 mA = re 50 Rsig 50 v sig Rin re 50 (a) IE = = 1.71 mA IC gm = = 68.4 mA/V VT VT 25 mV re = = 14.5 = IE 1.73 mA = 0.0145 k Chapter 6–49 rπ = (β + 1)re = 101 × 0.0145 = 1.4645 k (c) When CB is open-circuited, the equivalent circuit becomes that shown in Fig. 6.59(a). The op amp saturates with v A = −13 V, v − = 0 V and v O = 0 V. Finally, observe that the curve 2 representing the boundary between the triode region and the saturation region has the equation iD /k n = iD /kn (V2) 1 2 v 2 DS Figure 2 shows the graph for the relationship 1 iD /kn v 2OV 2 0 1 V VOV 2 OV vOV (V) Fig. This is a result of the linear v I which gives rise to a constant capacitor current during the diode conduction interval. 8.61 If Q1 has twice the base-emitter junction 2 area of Q2 , the bias current I will split I in Q1 3 1 and I in Q2 . 7.15. which can be simplified as follows: C1 + C2 1 1 = R1 + C1 R1 R2 = The LP STC circuit whose response determines the amplifier response at the high-frequency end has a phase angle of −5.7◦ at f = 1 kHz. Using the relationship for ∠T (jω) given in Table 1.2, we obtain for the LP STC circuit. To obtain maximum output resistance, we use the largest possible Rs consistent with ID Rs ≤ 0.3 V. Now, if each of the stages has a low-frequency (dc) closed-loop 40 MHz. gain K, then its 3-dB frequency will be K Thus for each stage the closed-loop gain is: K |G| = ⎛ ⎞2 f ⎟ ⎟ 1 + ⎝ 40 ⎠ G0 2 f 1+ f1 G= overall gain of the cascade is which is 6.4 times greater than the bandwidth achieved using a single op amp, as in case (b) above. Chapter 2–15 for a noninverting amplifier: 1 M 10 V Rin = ∞ 1 k Case Gain (V/V) Rin R1 R2 a –10 10 k 10 k 100 k b –1 100 k 100 k 100 k c –2 100 k 100 k 200 k d +1 ∞ ∞ 0 e +2 ∞ 100 k 100 k f +11 ∞ 10 k 100 k g –0.5 20 k 20 k 10 k (b) Inserting a buffer. rπ vo = × −gm (ro RL) vsig rπ + Rsig Q1 vi For I = 1 mA: 1 mA = 40 mA/V gm = 25 mV 100 = 2.5 k rπ = 40 mA/V =− 10 V = 10 k 1 mA A0 = 40 mA/V × 10 k = 400 V/V A0 = 2VA 2VA L 2 × 10 × 0.5 = 50 V/V = = VOV VOV 0.2 gm = 2ID VOV = −303 V/V 7.26 ro = I gm rπ 10 μA 0.4 mA/V 250 k ro A0 1 M 400 V/V 2= 40 mA/V 2.5 k 10 k 400 V/V 0.2 = ⇒ 7.25 Refer to Fig. However, it will have a profound effect on Rin , as Rin now is 10 M, and 10 vo = × −19.5 = −18.6 V/V vsig 10 + 0.5 This is nearly double the value we had before! From the figure we can determine the overall voltage gain as Gv = = vo Total resistance in the drain = vsig Total resistance in the sources 1 RL = gm RL 1 1 2 + gm1 gm2 where 7.93 gm = gm1 = gm2 = 5 mA/V Gv = 1 × 5 × 10 = 25 V/V 2 RL 10 k 7.95 Refer to Fig. 3.26 We can write the following node equation at the diode anodes: ID2 = 10 mA − V /R Thus the result is a decrease in the diode voltage by 17.3 mV. 4.5(a) to (d), together with their parameter values. P4.44. 6.26(b), we obtain the circuit shown in next column above. Vp 2Vr vO = vI = 1 V 1 vO = = 1 mA 1 k 1 k v D = 0.7 V iD = VA = 0.7 V + 1 k × 1 mA = 1.7 V For v I = −1 V, the diode is cut off. P6.72. Rin = 10 k (smallest gain magnitude) R2 10 k 10 k R1 10 k vO vO vI vI 10 k 10 k vO = −0.5 V/V vI Closed-loop gain is R2 10 k vO =− =− vI R1 10 k 10 k = −1 V/V For v I = +1.00 V, Rin = 20 k (smallest gain magnitude) 10 k 10 k vI v O = −1 × 1.00 vO = − 1.00 V The two resistors are 1% resistors vO = 10(1 − 0.01) = 0.98 V/V v 10(1 + 0.01) I min vO = 10(1 + 0.01) = 1.02 V/V v 10(1 − 0.01) I max vO = −2 V/V vI Thus the measured output voltage will range from −0.98 V to −1.02 V. Thus ie isig and ic = αie isig Thus, v o = ic RC = isig RC 6.73 For Rin = Rsig = 50 , re = 50 and, with α 1, VT 25 mV = = 0.5 mA IC re 50 gm = IC /VT = 20 mA/V Rin gm (RC RL) Gv = Rin + Rsig 50 × 20 × (10 10) 50 + 50 = 50 V/V Gv = VT 25 mV = = 125 IE 0.2 mA IC 0.2 mA = 8 mA/V gm = VT 0.025 V Rin gm (RC RL) Gv = Rin + Rsig 0.125 × 8(10 10) = 8 V/V = 0.125 + 0.5 6.74 Rin = re = Chapter 6–26 v ˆπ = v ˆsig Rin Rin + Rsig 10 = v ˆsig 0.125 0.125 + 0.5 Av nominal = Av high = 0.93 = v ˆsig = 50 mV v ˆo = Gv v ˆsig = 8 × 50 = 400 mV = 0.4 V 6.75 Rsig 1 gm RL (+10% above nominal) 1.5 Av low = 1.5 + 0.357 = 0.81 (−5% from nominal) 1 = Ro = 0.357 k gm ⇒ gm = 2.8 mA/V To find ID , we use gm = 2k n ID i i vsig 2 = 0.85 V/V 2.357 5 = 5.357 50 mV (peak) 0.5 V (peak) From the figure above, we have 1 = 0.1 × RL gm = 0.1 × 2 = 0.2 k ⇒ ID = gm2 /2k n 2.82 = 1.6 mA 2 × 2.5 1 2 ID = k n VOV 2 1 2 1.6 = × 2.5 × VOV 2 ⇒ VOV = 1.13 V = 6.77 Rsig/(b + 1) gm = 5 mA/V gm = 2k n ID 5 = 2 × 5 × ID ID = 2.5 mA At the peak of the sine wave, 0.5 V = 0.25 mA, thus id = 2 k iDmax = ID + 0.25 = 2.75 mA vsig re RL vbe vo iDmin = ID − 0.25 = 2.25 mA v ˆsig = v ˆgs + v ˆo = 0.05 + 0.5 = 0.55 V v ˆo = 0.5 V RL = 2 k RL RL + Ro 2 Av nominal = 2 + Ro 1.5 Av low = 1.5 + Ro 5 Av high = 5 + Ro For Av high = 1.1 Av nominal 6.76 Av = 5 1.1 × 2 = 5 + Ro 2 + Ro ⇒ Ro = 0.357 k v ˆbe = 5 mV From the figure above we see that re 5 mV = RL 500 mV RL = 20 100 VT 25 mV IE = = = 1.25 mA re 20 ⇒ re = At the peak of the output sine wave, we have ˆie = v ˆo = 0.5 = 0.25 mA RL 2 Chapter 6–27 v ˆbe = 10 mV RL × v ˆbe v ˆo = re 500 = × 10 12.5 = 400 mV = 0.4 V v ˆo 0.4 = = 0.488 V v ˆsig = Gv 0.82 Thus, iEmax = 1.25 + 0.25 = 1.5 mA and iEmin = 1.25 − 0.25 = 1.0 mA From the figure, we have Gv = = vo = v sig RL RL + re + 2 2 + 0.02 + 200 101 Rsig β +1 (c) Gv o = 1 Rout = re + = 0.5 V/V = 111.5 Thus, v ˆsig Thus, v ˆo 0.5 V = = =1V Gv 0.5 V/V RL RL + Rout 500 =1× = 0.82 V/V 500 + 111.5 which is the same value obtained in (a) above. Conduction angle = π − 2θ = 3.04 rad in each half cycle. Chapter 3–36 This figure belong to Problem 3.85, part b. 1 RS + re (β + 1) Now VOS can be obtained by dividing VC by Ad = gm RC , VEE Consider only the incremental currents involved. 3, will have 10 M 10 M vi vo Thus, VC2 = VG2 = 0.7 + VGS = 2.016 V IC2 = 5 − 2.016 VCC − VC2 = 1 mA 3 k 3 Figure 3 Chapter 7–35 no effect on the dc bias of each transistor. (d) v I = −3 V ⇒ v O = +3 V v A = +3.7 V v− = 0 V 3.82 (a) See figure (a) on next page. The input resistance Rin can now be obtained by inspection as ⇒ L = 0.8 μm W1 = 25 × 0.8 = 20 μm W2 = 4W1 = 80 μm 7.18 Refer to Fig. In general, one attempts to identify the lowest possible number of variables and write the corresponding minimum number of equations. With 4.7 k, the gain will be vo = −0.385 × 73.4 × (4.7 2) = −39.6 V/V v sig which is slightly lower than the required −40 V/V, and we will obtain VC = VCC − IC RC VC = 15 − 4.7 × 1.84 = 6.4 V allowing for about 2 V of negative signal swing at the collector. The resulting A0 = 45.5 V/V. With an op amp that has only ft = 40 MHz, the possible closed-loop gain at 5 MHz is |A| = 40 = 8 V/V 5 To obtain an overall gain of 100 would require three such amplifiers, cascaded. If the adjustment mechanism raises one RC and lowers the other, then each need to be adjusted by only (1.6 k/2) = 0.8 k. ro = 2V v DS 1 = 50 k = iD v GS const. The incremental changes around the equilibrium or bias point are related to each other by the circuit shown in Fig. 9.10(c) to determine τC2 : τC2 = CC2 (RC + RL) To make the contribution of CC2 to the determination of fL equal to 10%, we use 1 = 0.1ωL = 0.1 × 2πfL τC2 = τC2 = 1 = 15.92 ms 0.1 × 2π × 100 Chapter 9–4 Thus, −3 CC2 (20 + 10) × 10 = 15.92 × 10 3 ⇒ CC2 = 0.53 μF Although, to be conservative we should select CC2 = 1 μF; in this case we can select CC2 = 0.5 μF because the required value is very close to 0.5 μF and because we have selected CC1 and CE larger than the required values. This makes perfect sense since from Fig. ⇒ VOV 1 = 0.224 V 7.53 Equation (7.66): VGS1 = Vt + VOV 1 = 0.8 + 0.224 = 1.024 V Rout = ro + (Re rπ) + (Re rπ)gm ro VBIAS = VGS + ID1 Rs = ro + (re rπ)(1 + gm ro) = 1.024 + 0.1 × 0.05 = 1.03 V For gm ro 1, (b) gm1 2ID1 2 × 0.1 = 0.9 mA/V = = VOV 1 0.224 All transistors are operating at ID = 0.1 mA and have |VA | = 20 V. Thus, their W/L ratios will be equal, 0.2 = ⇒ 0 t 1 W × 0.1 × × 0.22 2 L W = 100 L Ro = (gm ro)2 ro where v3 -50 mV gm = 2 × 0.2 2ID = = 2 mA/V |VOV | 0.2 ro = |VA |L 6 × 0.4 = 12 k = ID 0.2 Ro = (2 × 12)2 × 12 = 6.91 M 0 t 7.69 Refer to Fig. 2.4 i = Gm (v 2 − v 1) v O = Rm i = Rm Gm (v 2 − v 1) 1 1 μR(Gm v 2 + Gm v 2 − Gm v 1 + Gm v 1) 2 2 1 v O = μRGm (v 2 − v 1) + μRGm (v 1 + v 2) 2 v Id 2v Icm ⇒ Ad = μRGm , Acm = μRGm Ad = 20 log Gm CMRR = 20 log Acm Gm For a CMRR ≥ 60 dB, Gm Gm ≥ 1000 ⇒ ≤ 0.1% Gm Gm 1 (v 1 + v 2) 2 v d = 0.005 sin(2π1000)t = v 1 − v 2 2.6 v cm = 2 sin(2π60)t = v 1 = v cm − v d /2 = sin(120π)t − 0.0025 sin(2000πt) v 2 = v cm + v d /2 = sin(120πt) + 0.0025 sin(2000πt) 2.7 Circuit a b c d v o /v i (V/V) −100 = −5 20 −5 −5 −5 Rin (k) 20 20 20 20 Chapter 2–2 10 k 10 k vI 10 k vO = −0.5 V/V vI 2.8 vO Note that in circuit (b) the 20-k load resistance has no effect on the closed-loop gain because of the zero output resistance of the ideal op amp. 6.72 Refer to the circuit in Fig. I VC1 = VC2 = VCC − RC 2 But the gain required is Gain = 2V v od = = 20 V/V v id 0.1 V Thus, RC 20 = 0.05 + 0.45 =5−2=3V v C1 = 3 − 80 × 0.005 sin(ωt) = 3 − 0.4 sin(ωt) v C2 = 3 + 0.4 sin(ωt) 8.38 (a) The maximum allowable value of the bias current I is found as I= (VCC P 1 mW = = 0.2 mA + VEE) 5V v C2 − v C1 = 0.8 sin(ωt) The waveforms are sketched in the figure on next page. Both Q1 and Q2 are operating in saturation at ID = 0.5 mA. ∴ ID = 0.5 mA Maximum current derivation 10%. Now, for our specific design: IL = 3.1 mA I = 0.1 mA 1.5V = 15 k 0.1 mA RI 3.1 = 0.1 1 + R2 R= R1 = = 30 R2 Choosing R2 = 500 ⇒ R1 = 15 k. Alternatively, if we set IEmax in Eq. (3) to 1.1 mA and solve Eqs. 1.16(b)]: v o = (Av o v i) RL RL + Ro 200 = (Av o v i) 1000 1000 + Ro (1) 195 = (Av o v i) 780 780 + Ro (2) Dividing Eq. (2) by Eq. (1), we have 1000 + Ro 195 = 0.78 200 780 + Ro Choose order to eliminate loading on input and output: ⇒ Ro = 100 A, first, to minimize loading on 0.5-M source (Av o v i) = 200[(1000 + 100)/1000] = 220 mV B, second, to boost gain C, third, to minimize loading at 100- output. Since io 1 1 M v i1 = = 1 M + 0.5 M 1.5 vs 1 = 20 mV 1.5 10 k =5 = 10 × 10 k + 10 k ⇒ v i1 = 30 × v i2 v i1 ⇒ v i2 = 20 × 5 = 100 mV Aisii Ro RL Chapter 1–17 io = (Ais ii) Ro RL Ro + RL we can write 1 = (Ais ii) Ro Ro + 1 (1) and 0.5 = (Ais ii) Ro Ro + 12 (2) 1.53 To obtain the weighted sum of v 1 and v 2 Dividing Eq. (1) by Eq. (2), we have Ro + 12 ⇒ Ro = 10 k Ro + 1 2= v o = 10v 1 + 20v 2 we use two transconductance amplifiers and sum their output currents. The results are given in the table below: (b) See figure on next page. To obtain a CMRR of 88 dB, we write 1001 88 = 20 log 4(x/100) 1001 × 100 = 25, 118.86 4x ⇒ x 1% R3 = R3nominal (1 −) R1 = R1nominal (1 +) R4 = R4nominal (1 +) where R4nominal R2nominal = =K R1nominal R3nominal Substituting in the expression for Acm , R4nominal (1 +) × R4nominal (1 +) + R3nominal (1 −) (1 −)2 1− (1 +)2 Acm = For 1, Acm 101 = 104 4 101 = 0.25 × 10−2 4 × 104 That is, the resistor tolerance should be a maximum of 0.25%. 8.31 Require v od = 1 V when v id = 10 mV and I = 1 mA. 1(b), we can determine Gv o from Rin Av o Gv o = Rin + Rsig RL =∞ Thus, Denoting Rin with RL = ∞ as Ri , we can express Gv o as Rin ≡ Gv o = Ri Av o Ri + Rsig v i = if Rf + (if − gm v i)(R2 RL) v i [1 + gm (R2 RL)] = if [Rf + (R2 RL)] and Q.E.D. Rin = R1 Rin Rf + (R2 RL) = R1 1 + gm (R2 RL) From the equivalent circuit in Fig. Thus 1 ID = k n (VGS − Vt)2 2 1 = × 4 × (0.6 − 0.4)2 2 = 0.08 mA 0.8 1 − VD 1 − 0.2 = = 10 k = RD = ID 0.08 0.08 −0.6 − (−1) −0.6 + 1 = = 5 k ID 0.08 For ID to remain unchanged from 0.08 mA, the MOSFET must remain in saturation. Chapter 8–3 Case i D1 (mA) i D2 (mA) a 0.08 0.08 b 0.12 0.04 c 0.16 0 d 0.04 0.12 e 0 0.16 vid (V) vS (V) 0 −0.6 vD1 (V) vD2 (V) vD2 − vD1 (V) +0.6 +0.6 0 +0.104 −0.541 +0.4 +0.8 +0.4 +0.283 +0.2 +1.0 +0.8 −0.104 −0.645 +0.8 +0.4 −0.4 −0.283 −0.683 +1.0 +0.2 −0.8 −0.4 8.4 To obtain the complementary split in current, that is, iD1 = 0.07 mA and iD2 = 0.09 mA, VDD 1 V v id = −0.025 V RD RD 5 k vD1 G1 vid vGS1 5 k vD2 iD1 iD2 Q2 Q1 vS G2 vGS2 I 0.16 mA VSS 1 V 8.5 Refer to Fig. 1 we see that IC = 0.495 mA VC = IB × 200 k + IE × 0.2 k + VBE = 0.005 × 200 + 0.5 × 0.2 + 0.7 = 1.18 V (b) 6.120 Refer to the circuit in Fig. The resistor values are obtained as follows: V2 = −0.7 V V2 − (−5) 0.5 mA ⇒ R1 = 8.6 k R1 = Chapter 4–23 This figure belongs to Problem 4.59.

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