THE ELECTRONICS RESURGENCE INITIATIVE

COMMON HETEROGENEOUS INTEGRATION AND INTELLECTUAL PROPERTY (IP) REUSE STRATEGIES (CHIPS)

ANDREAS OLOFSSON
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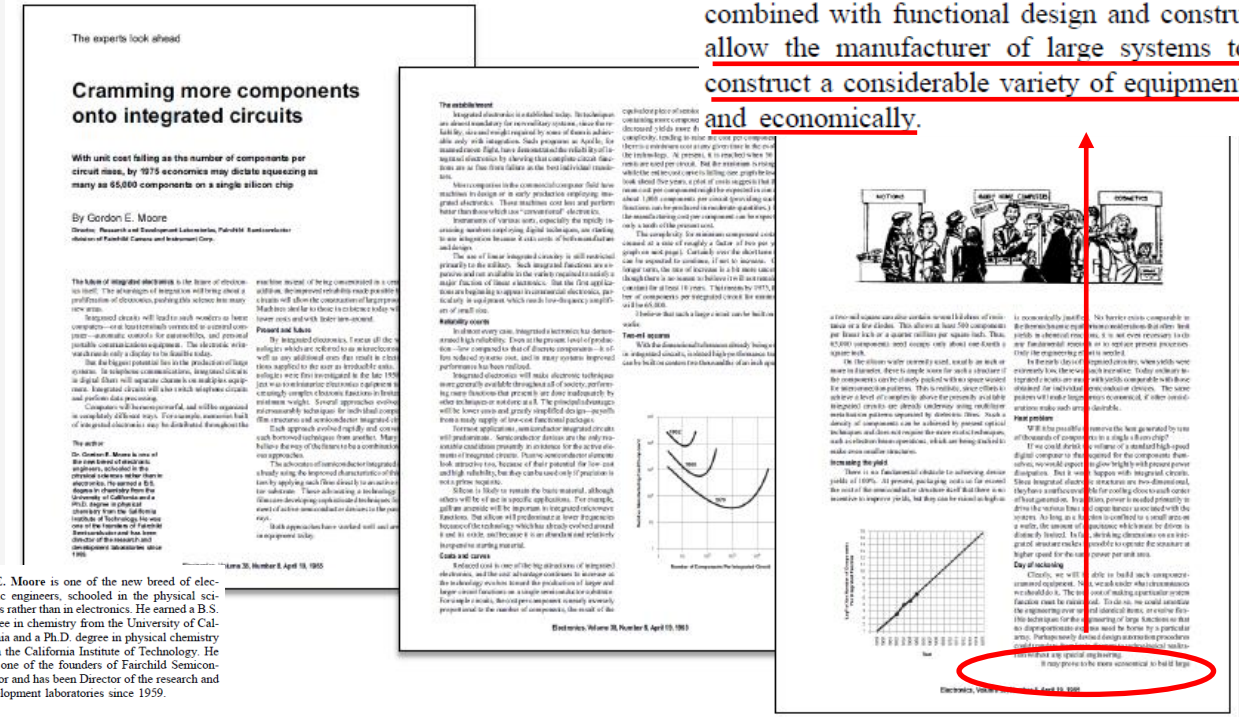
HETEROGENEOUS INTEGRATION RESCUING MOORE'S LAW

It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.



The experts look ahead

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

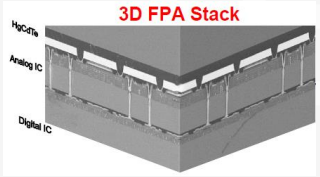
G. E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been Director of the research and development laboratories since 1959.

Source: *Electronics* magazine

DARPA'S HISTORY OF INTEGRATION INNOVATION

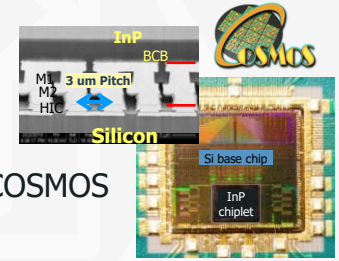
ASEM

VISA

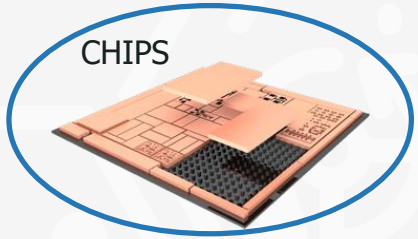


3D-IC

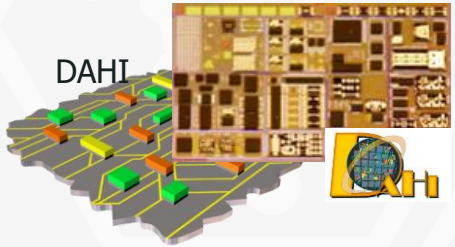
COSMOS



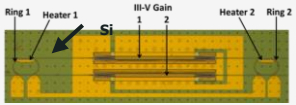
CHIPS



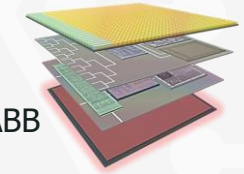
DAHI



E-PHI



MOABB

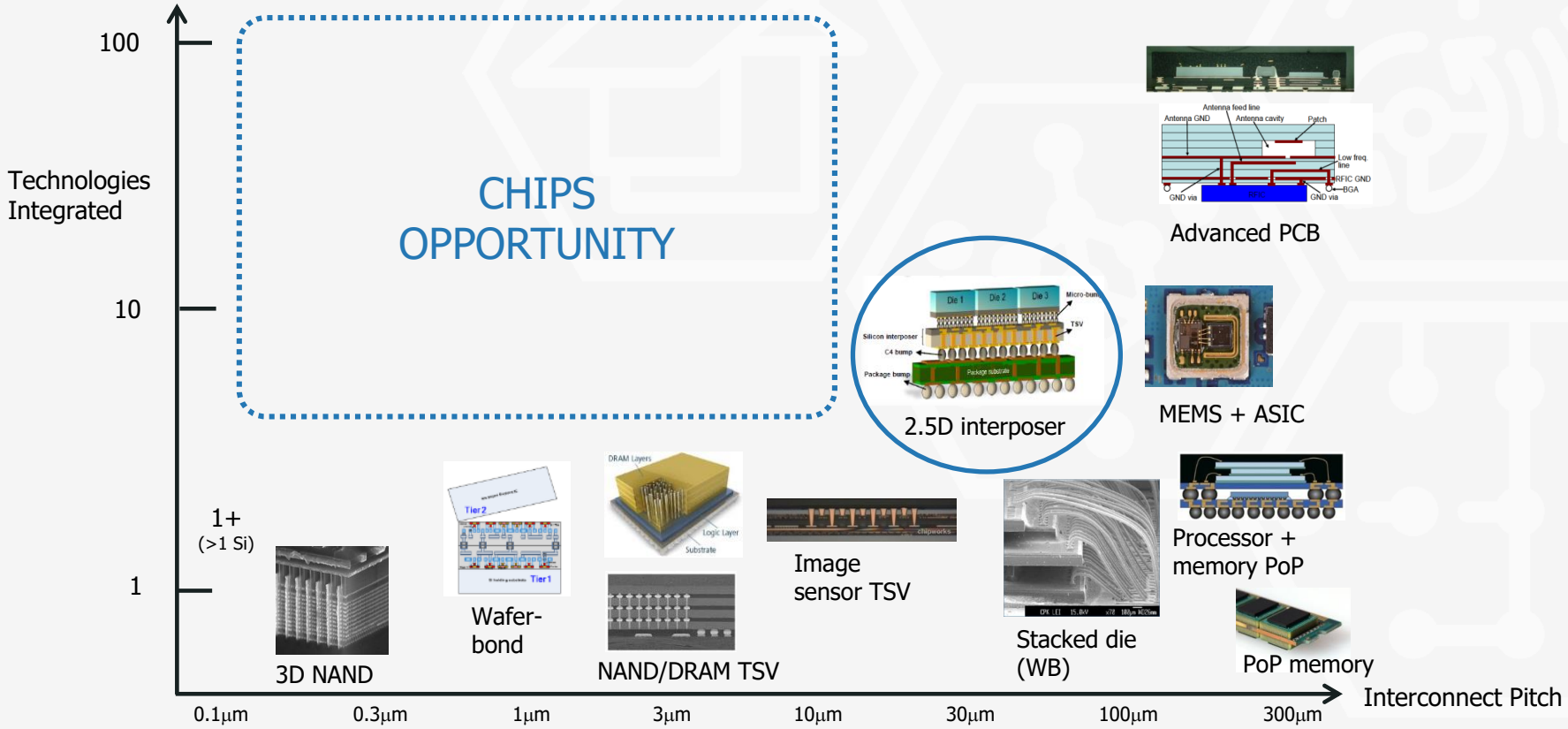


ASEM: Application Specific Electronic Modules
E-PHI: Electronic-Photonic Heterogeneous Integration
VISA: Vertically Integrated Sensor Arrays
COSMOS: Compound Semiconductor Materials on Silicon
DAHI: Diverse Accessible Heterogeneous Integration
MOABB: Modular Optical Aperture Building Blocks
CHIPS: Common Heterogeneous Integration and IP Reuse Strategies

1990s 2000s 2010s 2020s

Sources: DARPA, Smithsonian Chips

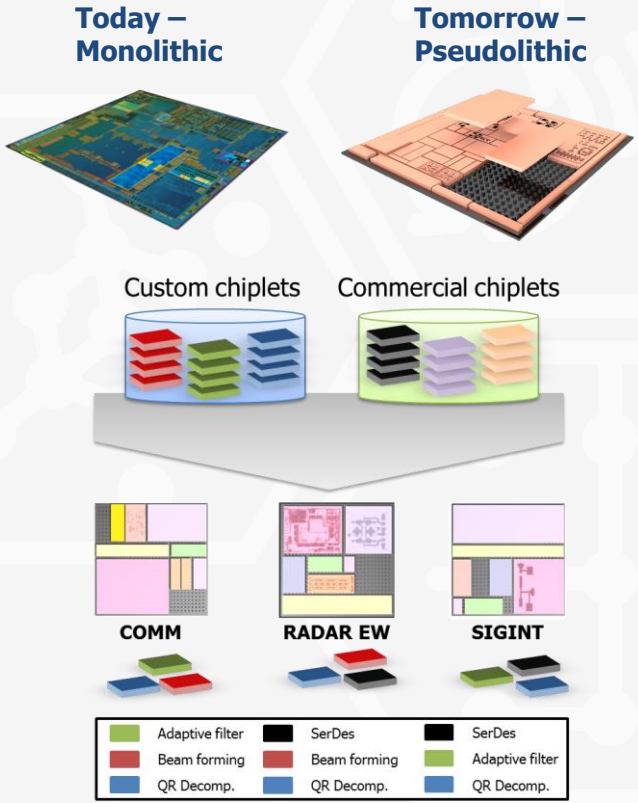
INTEGRATION DIVERSITY VS DENSITY



Sources: Samsung, Tezzaron, Micron, Hynix, Sony, TSMC, Prismark, STATS ChipPAC, Georgia Tech, IEEE, STMicro, Finetech

WHAT IS CHIPS?

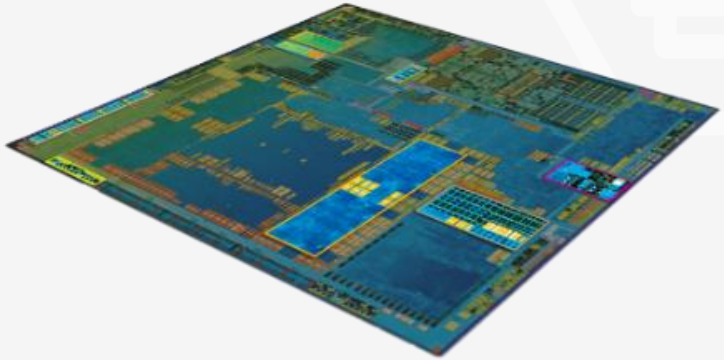
CHIPS will develop **design tools**, **integration standards**, and **IP chiplets** required to demonstrate **modular** electronic systems that can leverage the best of DoD and commercial designs and technology.



Sources: DARPA, Intel

CHIPS PSEUDOLITHIC DISRUPTION

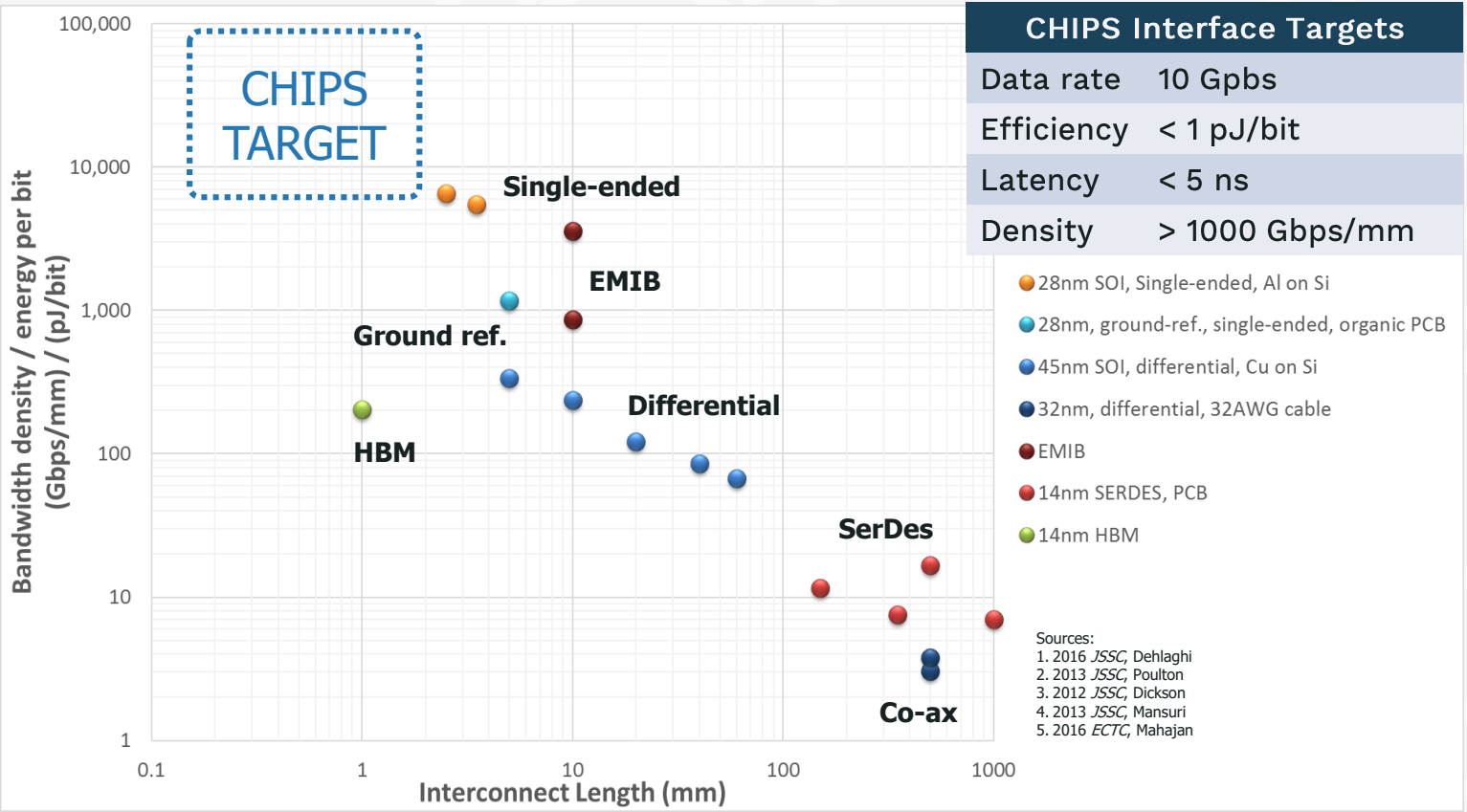
CHIPS: "Near monolithic performance at board design time scales"



MONOLITHIC		BOARD DESIGN
$100M	COST	$10K
MONTHS→YEARS	TIME	DAYS→WEEKS
1000	INTERCONNECT DENSITY	1

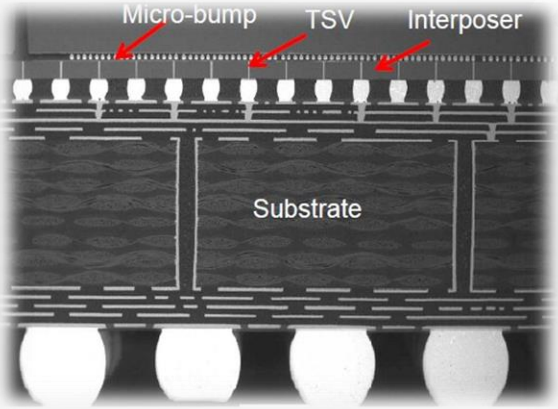
Sources: Raspberry Pi, Intel

CHIPS INTERFACE STANDARD

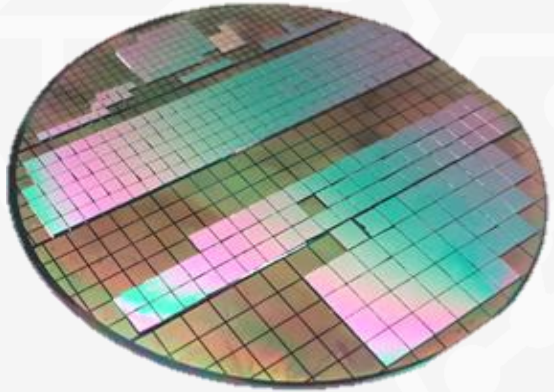


CHIPS Interface Targets	
Data rate	10 Gpbs
Efficiency	< 1 pJ/bit
Latency	< 5 ns
Density	> 1000 Gbps/mm

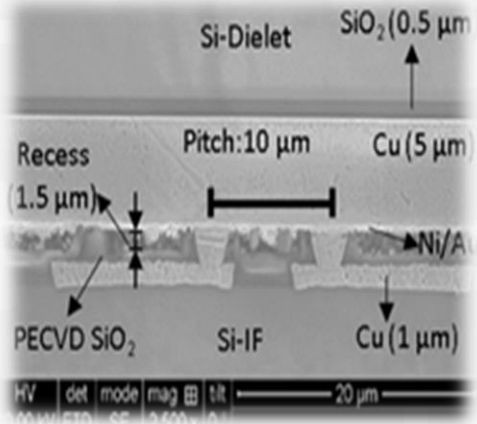
CHIPS MANUFACTURING RESEARCH VECTORS



Low Cost
Interposers



Micron Scale
Chiplet Placement



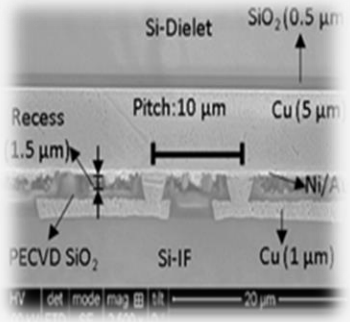
10-55um
Bump & Bond

CHIPS is targeting solutions suitable for low volume (<100K units) trusted manufacturing needed for national security needs

Sources: Xilinx, UCLA

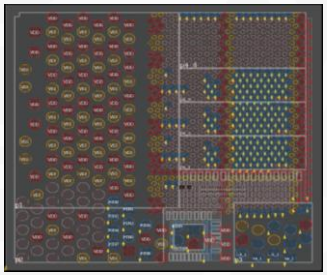
CHIPS PERFORMER SUMMARY

Manufacturing



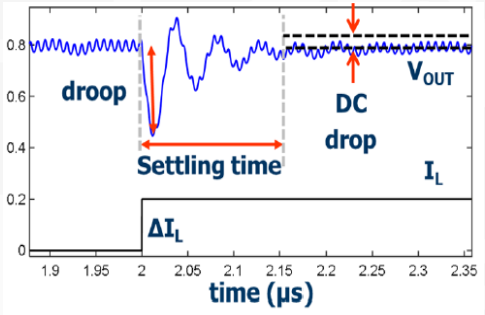
Intel
Northrop Grumman
Micross
UCLA

Chiplets



Jariet
Synopsys
Micron
Intrinsix
Lockheed Martin
Michigan
NCSU
Ferric

Tools

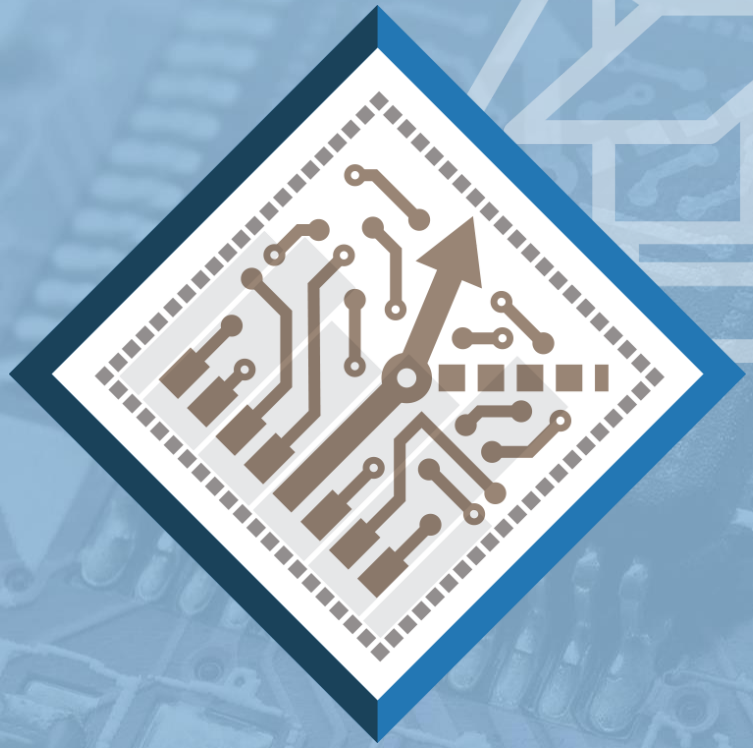


Cadence
Georgia Tech

Sources: UCLA, Michigan, Georgia Tech

THE CHIPS VISION

- **Modularity**: A ubiquitous chiplet interface standard "Ethernet for chiplets"
- **Speed**: Board manufacturing time scales (days→weeks) possible with a library of hundreds of COTS chiplets
- **Performance**: 1pJ/bit and 1Tbit/mm WILL disrupt the computing landscape
- **Security**: CHIPS disaggregation offers a pathway to high assurance electronics



CHIPLET ECOSYSTEM: PLATFORM AND PARTNERS

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA).

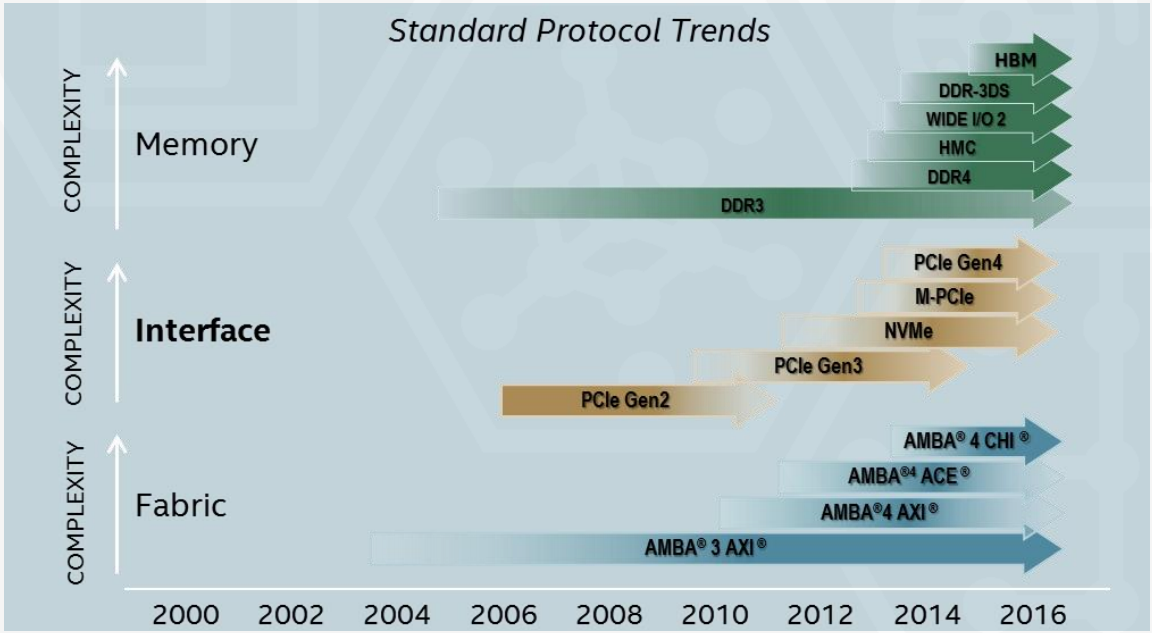
SERGEY SHUMARAYEV

SENIOR PRINCIPAL ENGINEER
INTEL PSG CTO OFFICE

RAPIDLY CHANGING WORKLOADS AND APPLICATIONS

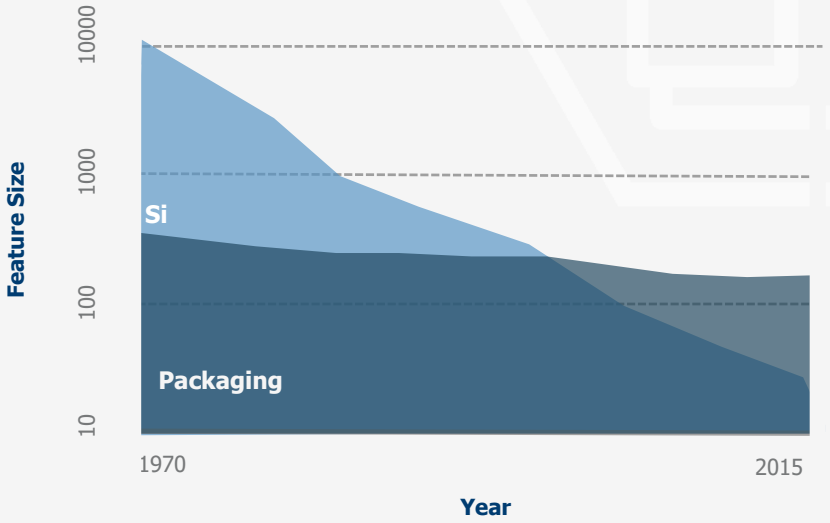
Data, AI, and Infrastructure

I/O Higher Complexity, Shorter Life, More Variety



Source: Cadence

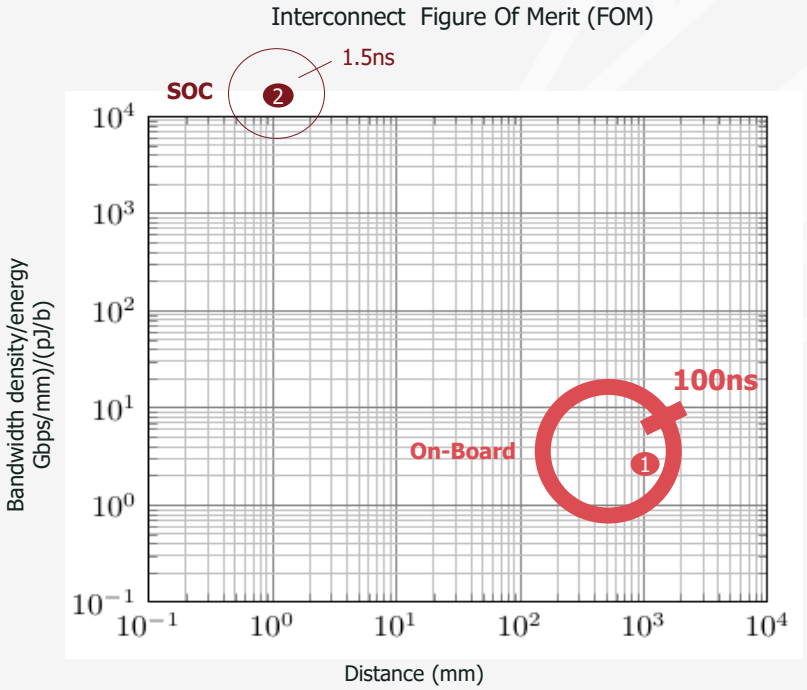
COST & PERFORMANCE DISPARITY IN SCALING



Technology Disparity Drove

- SERDES needs to connect the dies
- Increased complexity, system latency, and power
- Long & coupled development cycles for analog + digital on same monolithic die

COST & PERFORMANCE DISPARITY IN SCALING



Legend:

On-Board interconnect (e.g. PCI-E PMA + PCS):

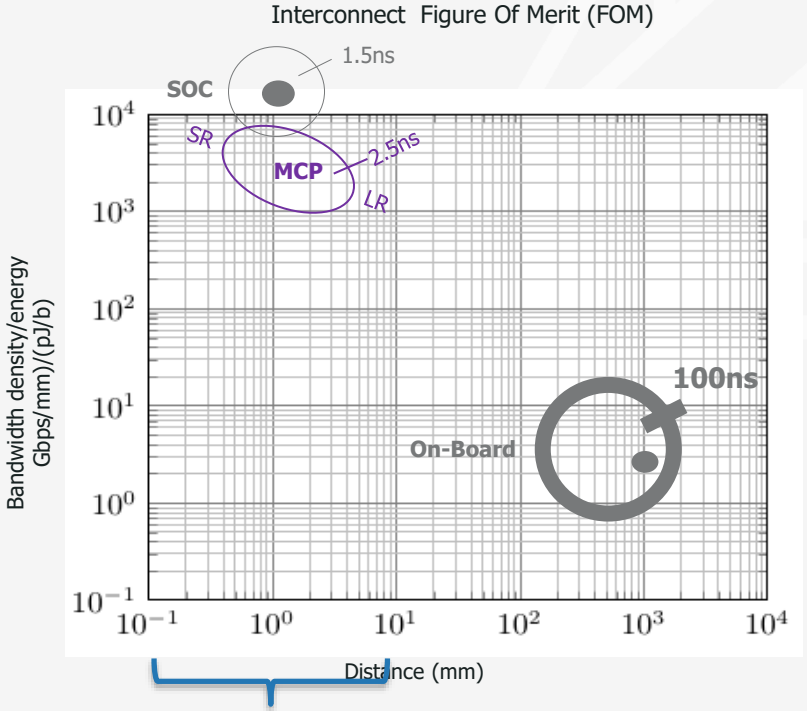
- ~1000mm; ~0.3mm shoreline; 20pJ/bit; 16Gbps:
- FOM=(16Gbps/0.3mm)/(20pJ/bit)=2.7
- Latency=100ns

SOC (12invs+2DFF+2mux):

- ~1mm; ~1um shoreline; 0.1pJ/bit; 2Ghz:
- FOM=(2Gbps/0.001mm)/(0.1pJ/bit)=20,000!
- Latency=1.5ns

10,000x FOM
100x Latency

COST & PERFORMANCE DISPARITY IN SCALING



Legend:

High Density Multi Chip Packaging interconnect

- 0.1-10mm; 500IO/mm shoreline; 0.1-1.0pJ/bit
- $FOM_{LongReach}$=(1Tb/mm)/(1pJ/b)=1,000
- $FOM_{ShortReach}$=(1Tb/mm)/(0.1pJ/bit)=10,000
- Latency=2.5ns

CHIPS

SOC-like FOM

INDUSTRY HAS REACHED AN INFLECTION POINT

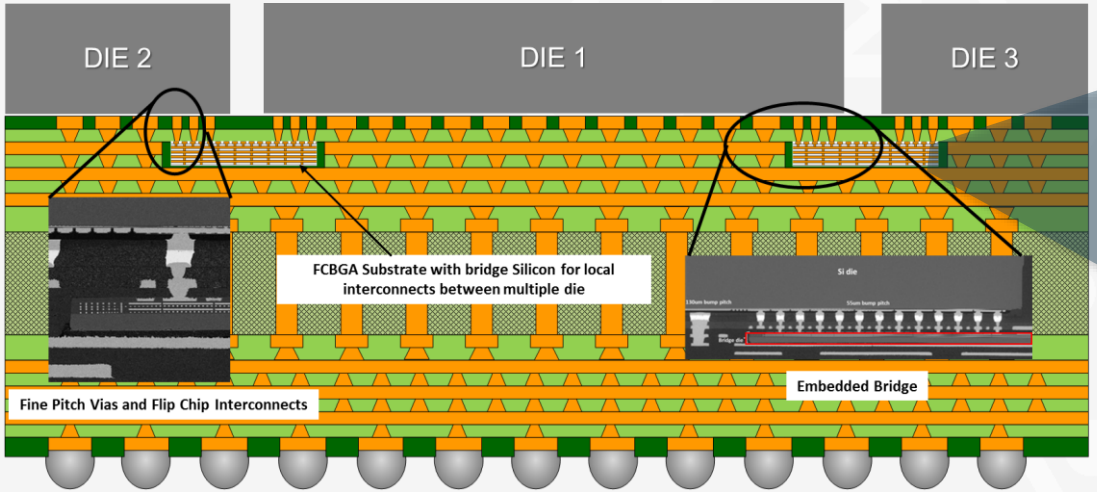
"…It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected."

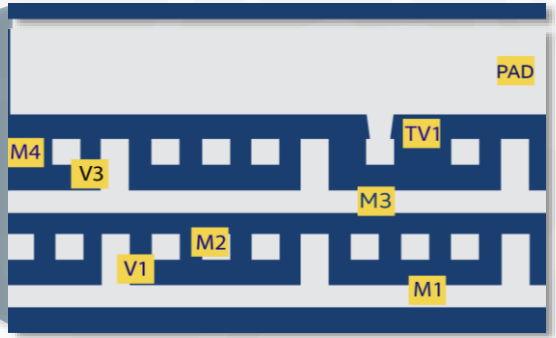
Gordon E. Moore

INDUSTRY HAS REACHED AN INFLECTION POINT

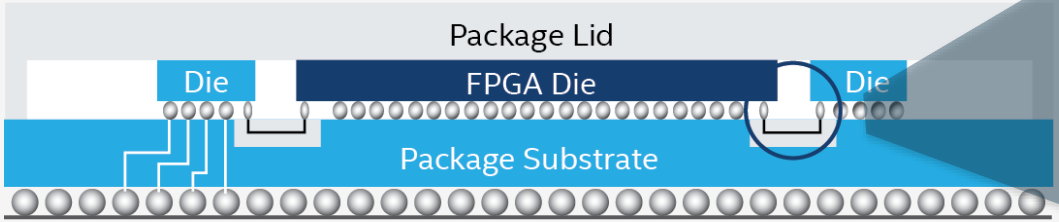
High Density Packaging Technology Enables Heterogeneous Integration at SoC-like FOM

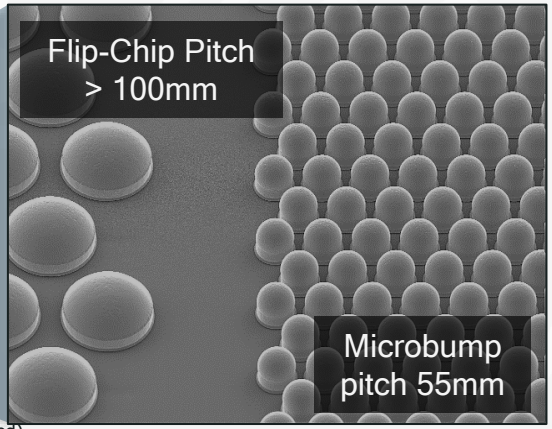
WHAT IS HIGH DENSITY PACKAGING TECHNOLOGY?



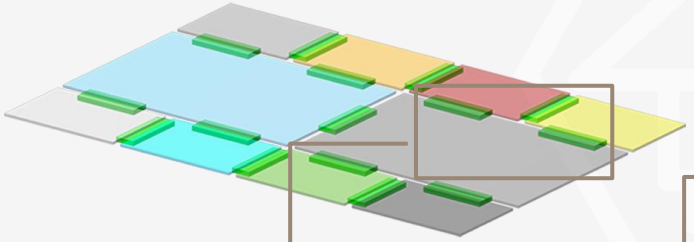


Intel® Stratix® 10 FPGAs and SoCs with Intel EMIB



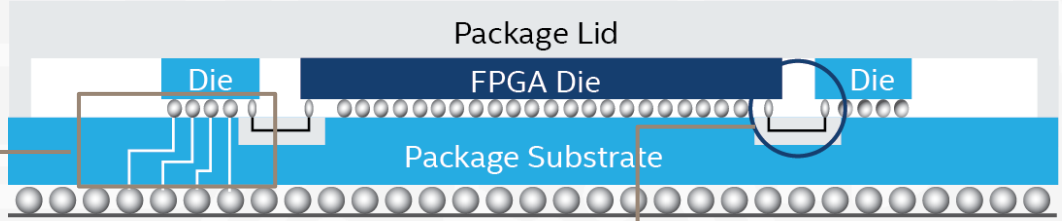


DENSITY PACKAGING TECHNOLOGY OFFERINGS



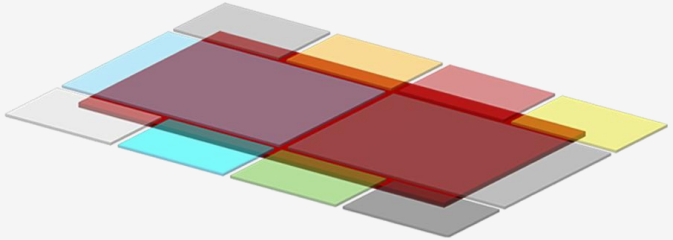
Multiple bridges possible

Intel® Stratix® 10 FPGAs and SoCs with Intel EMIB

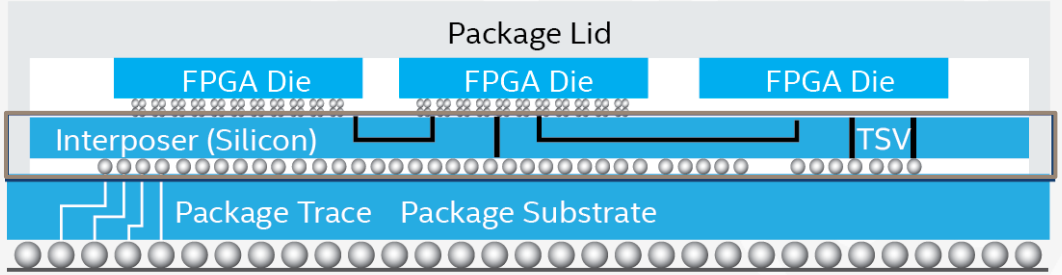


The rest of the package: RF, other I/Os, and power are unaffected

Localized high density die-to-die interconnect

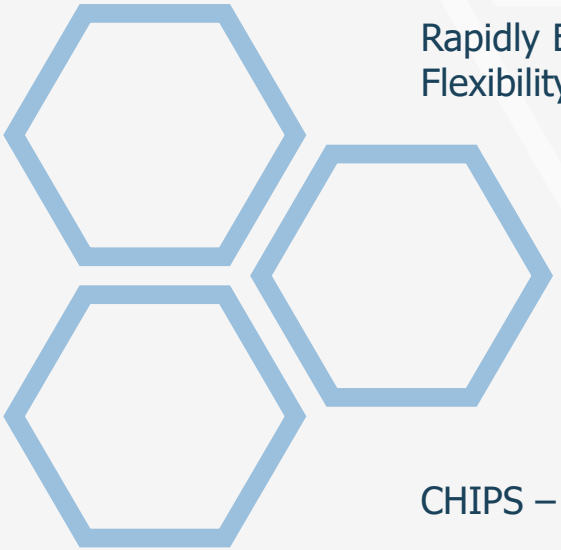


Other Multi-Die Integration



All signals have to travel through the Interposer, including RF signals

INDUSTRY HAS REACHED AN INFLECTION POINT

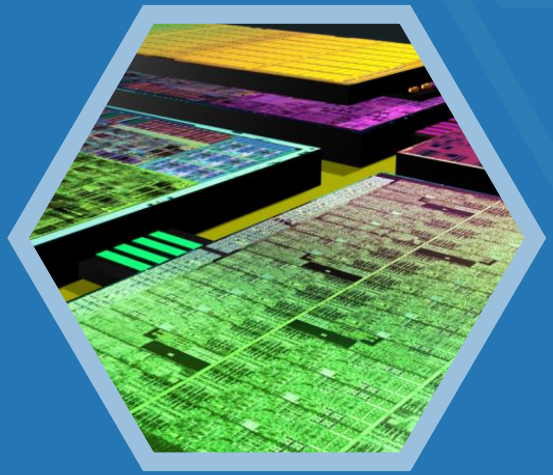


Rapidly Emerging Workloads Demands
Flexibility & Interoperability

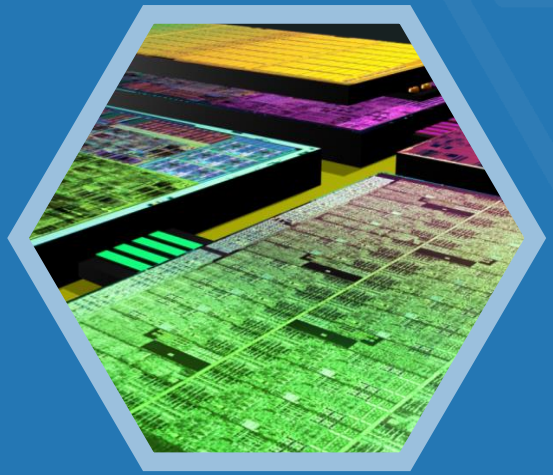
Breakthrough Packaging Technologies
Approach On-Die Capabilities

CHIPS – Innovation Through Chiplet Ecosystem!

WHAT IS A CHIPLET

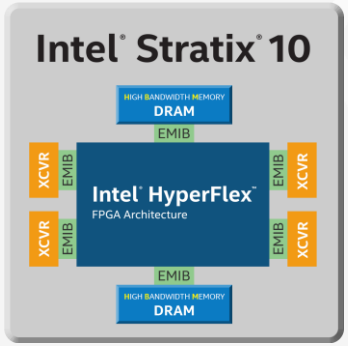


A physical IP block designed to integrate with other chiplets through **package level integration** and **standardized interfaces**

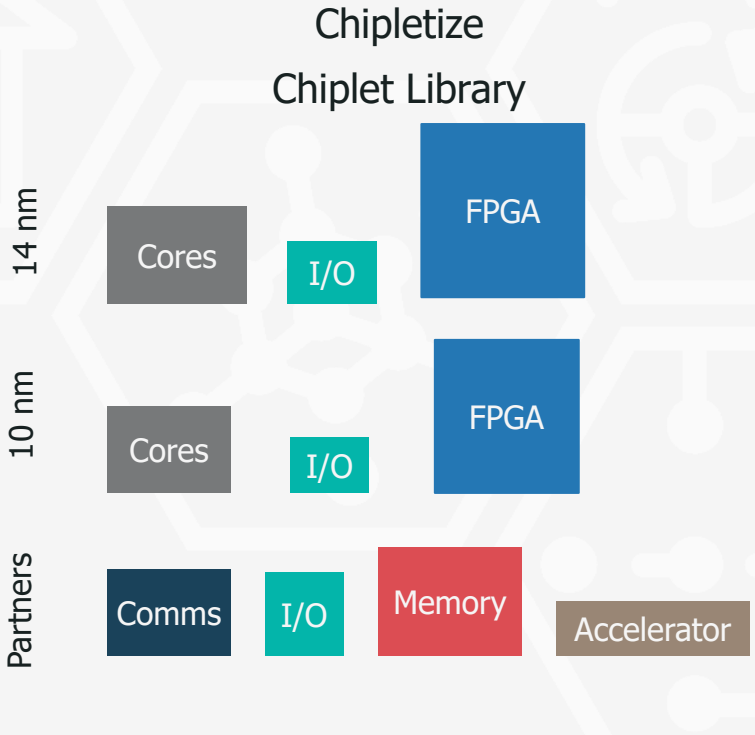


To create new products with
greater functionality,
improved agility
and faster time to market.

AN EXAMPLE OF HOW THIS WORKS



- Mixes process nodes and system functions into a single device
- Superior noise isolation for analog vs. monolithic
- FPGA + transceivers (XCVRs) + High-Bandwidth Memory (HBM) = 3 foundries



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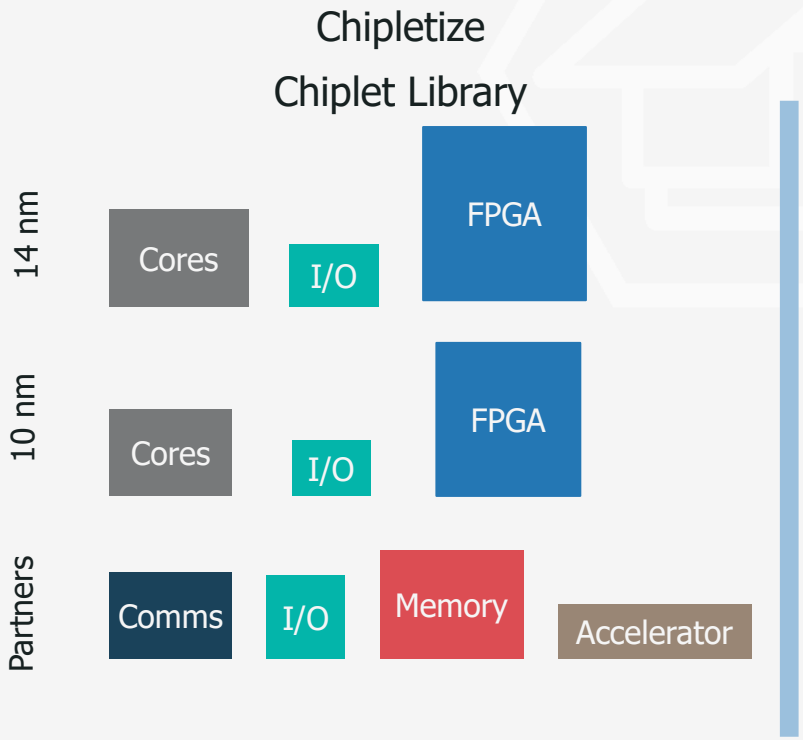
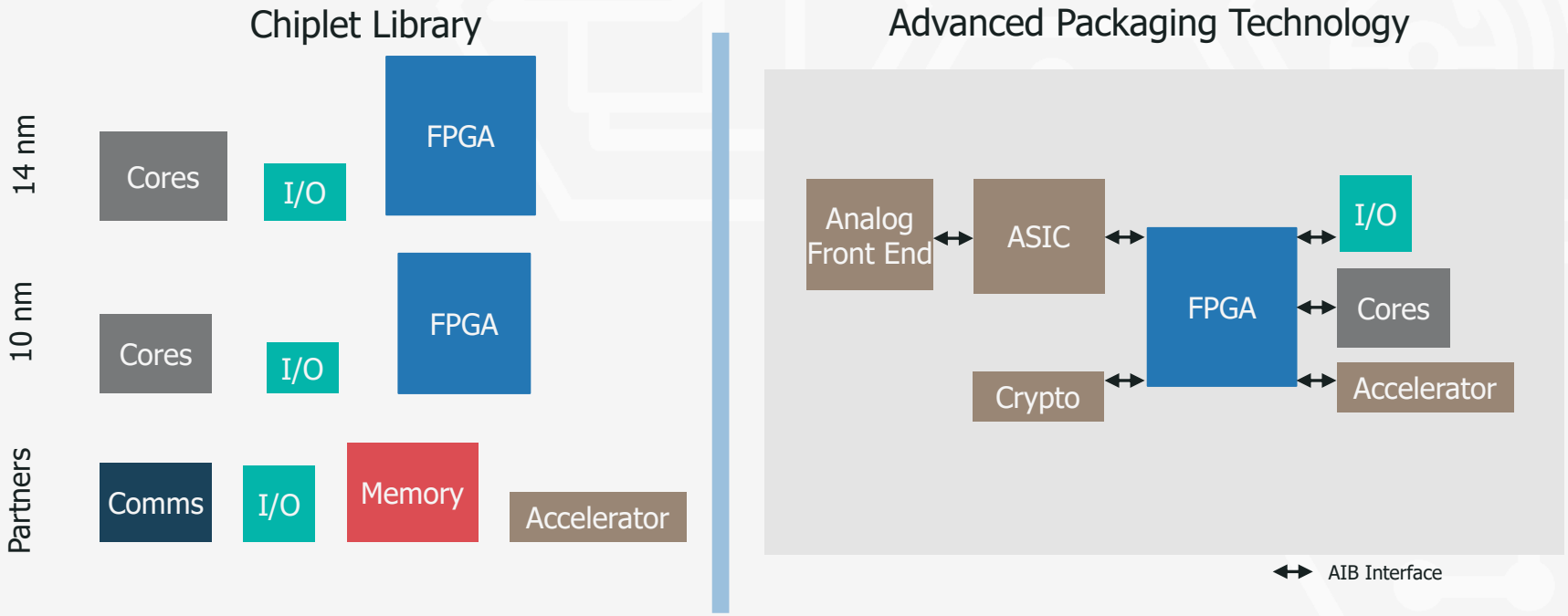


AN EXAMPLE OF HOW THIS WORKS



THE AIB DIE-TO-DIE INTERFACE STANDARD

AIB (ADVANCED INTERFACE BUS) is a PHY-level interface standard for **high bandwidth, low power** die-to-die communication

AIB Promoters agreed to promote AIB as a die-to-die interface standard

AIB Promoters:

-Boeing
-Intrinsix
-Synopsys
-Intel
-Lockheed Martin
-NTESS
-Jariet Technologies
-North Carolina State University
-University of Michigan

AIB PLANS FOR STANDARDIZATION

Licensing Program

Today

Intel 1:1 with others

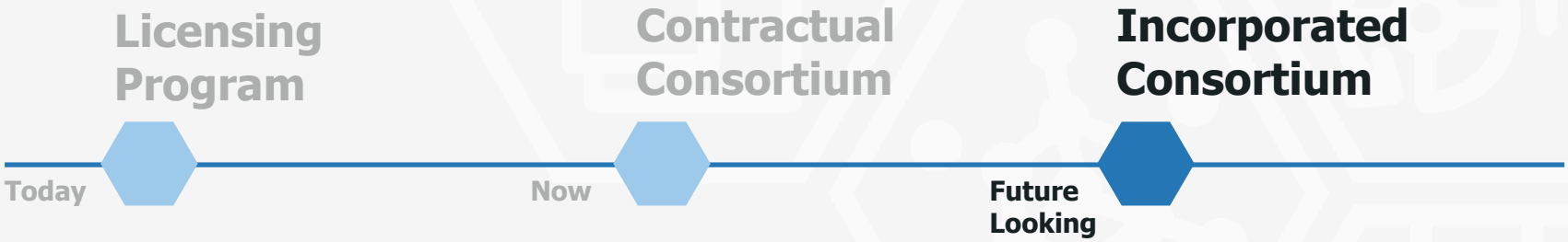
AIB PLANS FOR STANDARDIZATION

Intel 1:1 with others

Promoters Group
e.g. 25G Ethernet

- Consortium model builds engagement and trust
- Equal votes of members vs. Intel or other full control

AIB PLANS FOR STANDARDIZATION



- Under consideration
- Standard setting organization
- Path taken by 25G Ethernet

CONCLUSIONS

Platform for innovation through ecosystem

Explore new business models

Seeking to develop new partnerships

ADC/DAC
Machine Learning Memory
Processors
Adjacent IP
…Your Ideas

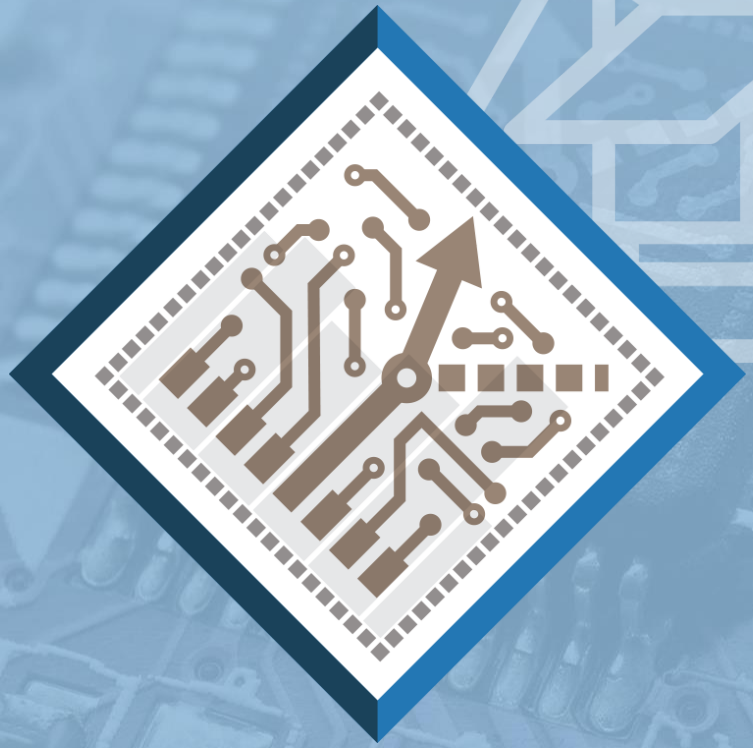
HOW TO GET INVOLVED

Start here for more information, specifications, and more:
https://intel.ly/2LlSZcr

ERI ELECTRONICS RESURGENCE INITIATIVE

SUMMIT

2018 | SAN FRANCISCO, CA | **JULY 23-25**



ULTRA-HIGH SPEED DIRECT RF SAMPLING ADC'S AND DAC'S FOR HETEROGENEOUS 2.5D INTEGRATION

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA).

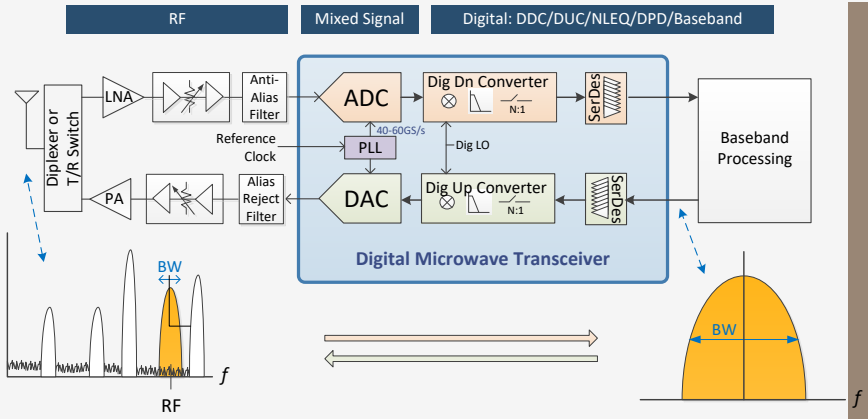
CRAIG HORNBUCKLE

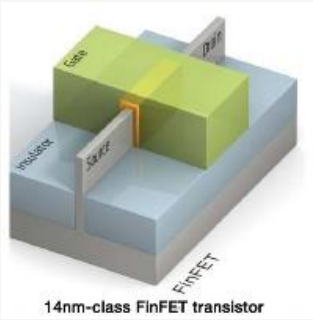
CHIEF TECHNOLOGY OFFICER

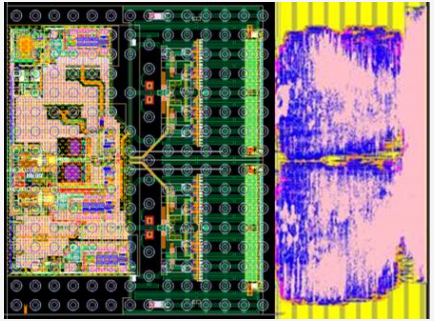
JARIET TECHNOLOGIES, INC.

DIRECT RF SAMPLING / SYNTHESIS

- **"Digital Microwave"** replaces conventional RF/analog systems with millimeter wave ADC's and DAC's enabling digital frequency conversion and filtering operations
- Permits digitally tuning of one or more frequency bands within Nyquist zone
- **Direct RF-sampling** of microwave / millimeterwave signals
- **Concurrent system operation** in multiple bands & beams



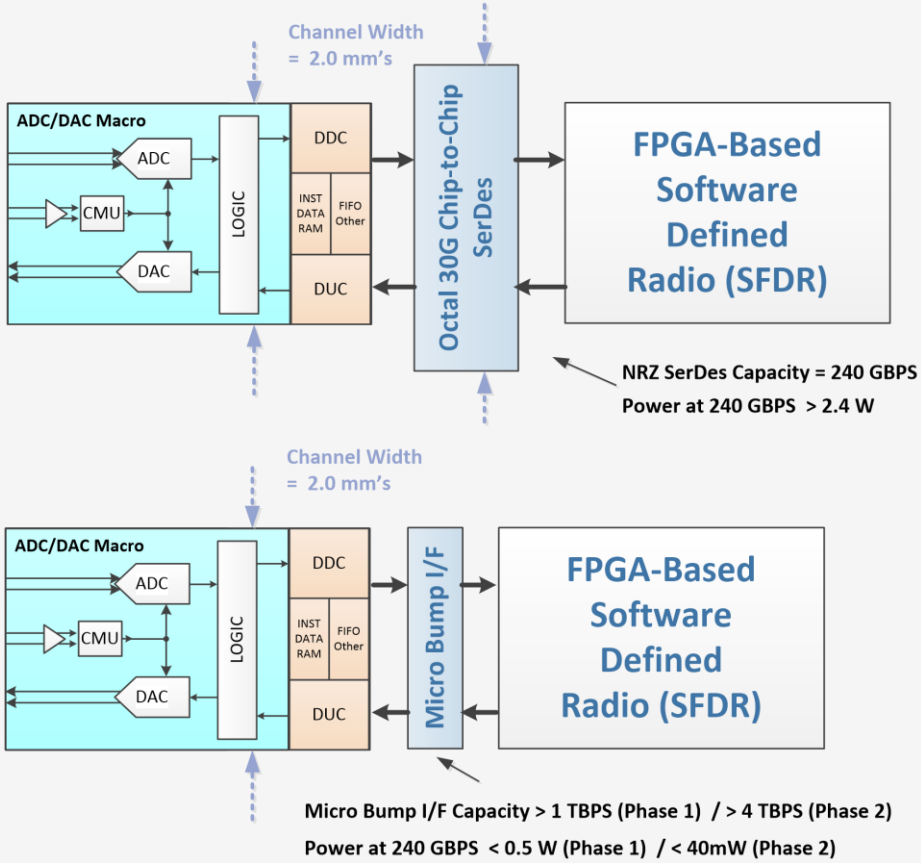




Source: SemiWiki, Jariet

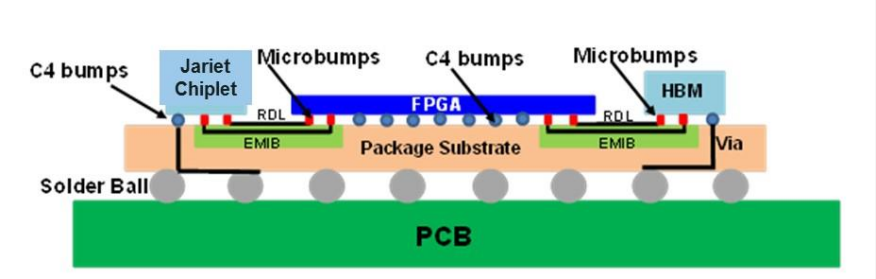
SOFTWARE DEFINED RADIO USING DARPA "CHIPS"

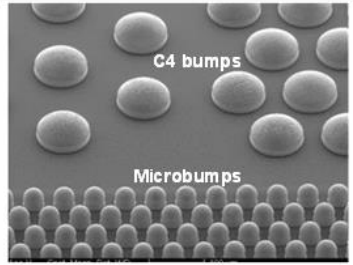
- Digital Microwave systems require a wideband data bus for each receive and transmit channel to connect to modems or other DSP functions
- The required data interface rate increases as the instantaneous bandwidth increases
- For systems desiring access to the full available Nyquist bandwidth, **bus capacities as high as 3 TBPS** in each direction are needed
- Use of **traditional SerDes** for these interfaces **results in high power consumption, large circuit area**, and high IP costs
- SerDes cannot handle the full bandwidth available at the raw ADC/DAC data interfaces



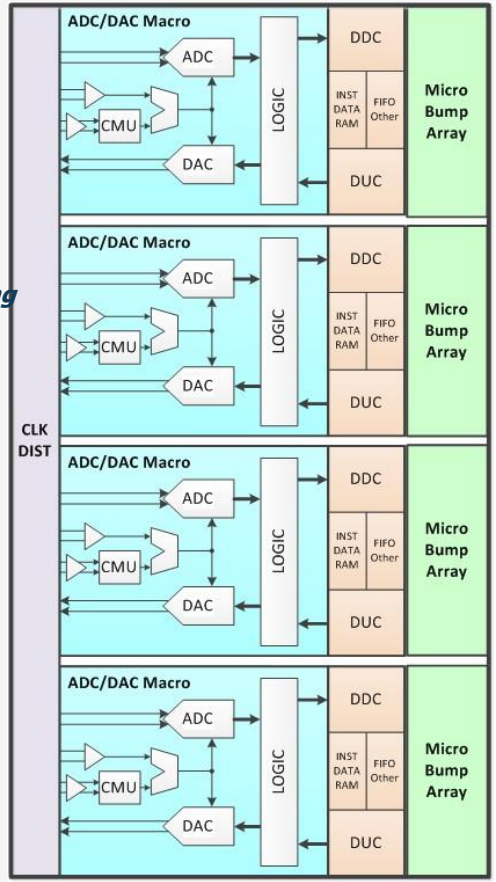
Source: Jariet

ENABLING TECHNOLOGIES





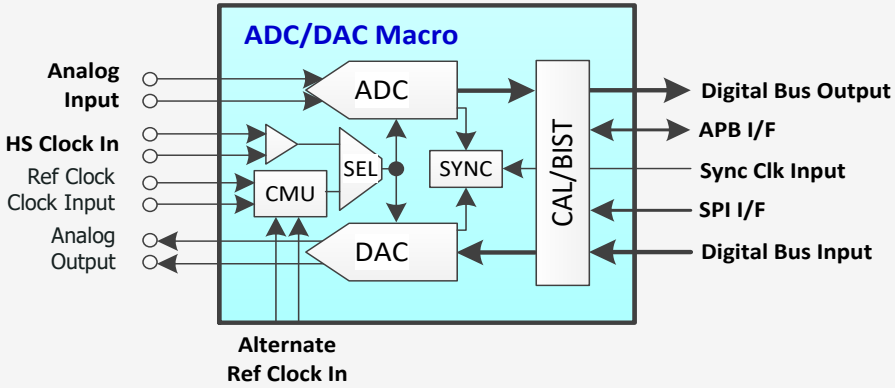
Ultra-fine pitch wafer bumping

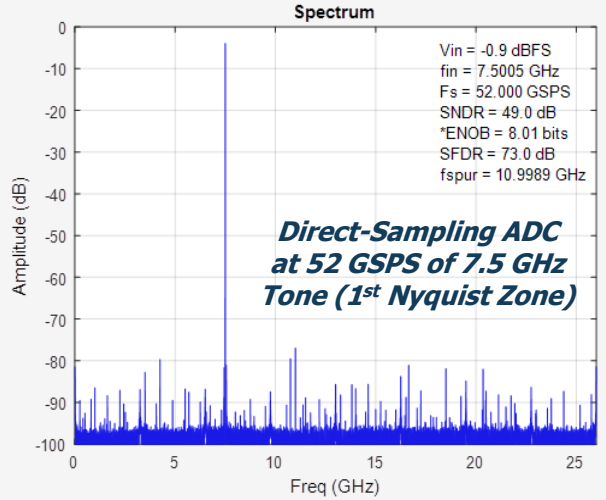


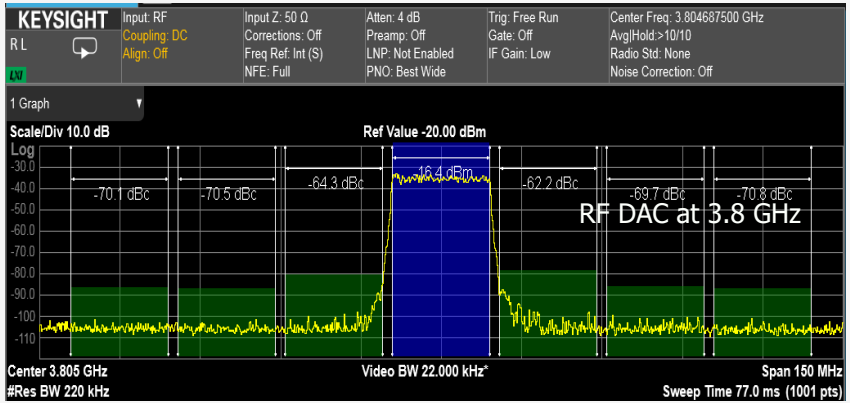
- **Direct RF sampling with Jariet's proven ADC/DAC performance**
  - 10-bit, 40-64Gsps ADC/DAC macrocell
  - Wide analog bandwidth permits operation to > 36 GHz
  - Instantaneous bandwidth >5 GHz per channel
- **High level of RF/Digital Integration in 14LPP SOC**
  - 4x ADC/DAC macrocells
  - Per-channel digital pre-processing (~40M gates/channel)
  - **Standardized AIB low-power in-package parallel interface**
- **System-in-Package applies advanced MCM packaging techniques**
  - High density parallel bus eliminates high power Serdes
  - Modularity-by-design facilitates reuse & upgrade
  - Enables technology node migration & heterogeneous integration

Source: 3D InCites, Jariet

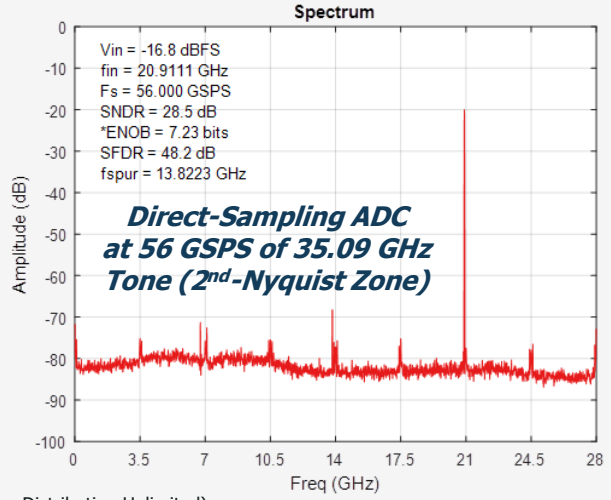
ADC & DAC RF PERFORMANCE







31.46GSPS DAC ACPR Performance with 20MHz LTE waveform; RF Output at 3.805GHz, Non-Adj. ACPR = 70 dB



Source: Jariet

IMPACT

- **Key benefits for next generation systems**
  - Higher integration = **lower SWAP**
  - Reconfigurable capability (SWDR) eliminates entire specialized systems
  - **Flexible and modular architecture reduces new system development NRE and timeline**

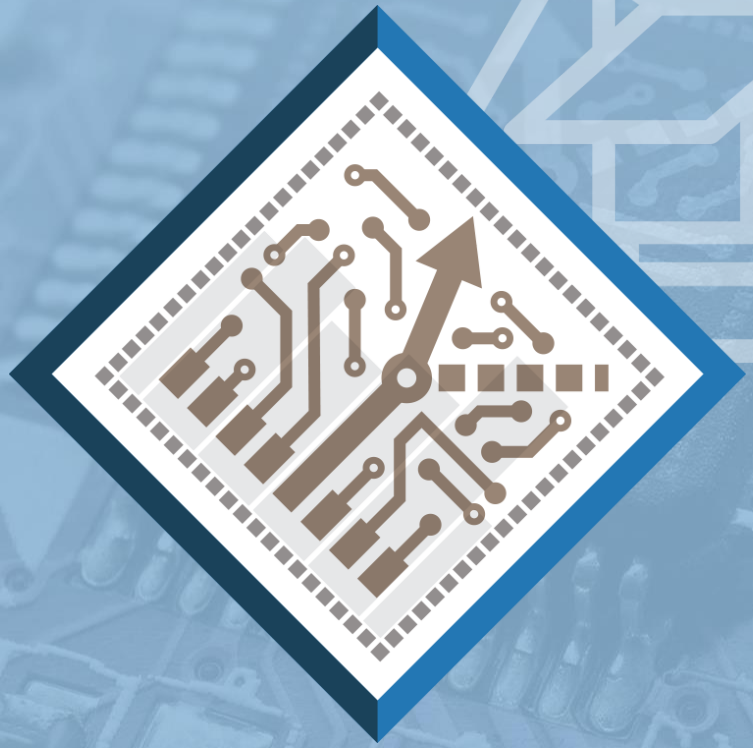
- Massive MIMO improves system spectral efficiency and increases throughput in 5G mobile/FWA (commercial)
- **Dynamically reconfigurable antenna arrays for air traffic control (ATC), weather RADAR, and mil-aero**
- **Dual-use technology building blocks leverage commercial volumes** for better DoD affordability

Source: nssl.nasa.gov; pcmag.com

ERI ELECTRONICS RESURGENCE INITIATIVE

SUMMIT

2018 | SAN FRANCISCO, CA | **JULY 23-25**

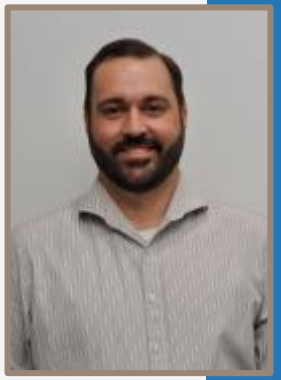


MICROSS ADVANCED PACKAGING SOLUTIONS FOR CHIPS & HI-REL ELECTRONICS

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA).

JOHN M. LANNON, JR., PHD

RICHARD KINGDON,
CEO

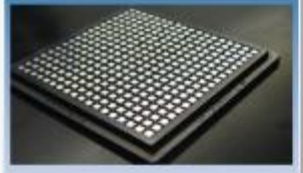


JEREMY ADAMS,
VP OF PRODUCTS & SERV.

MICROSS SERVICE OFFERING

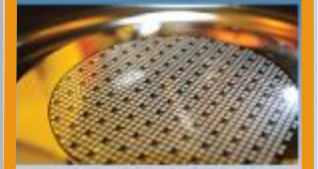
Micross provides microelectronic component supply, packaging and test services in support of Hi-Rel applications for the Space, Medical and Industrial sectors

Bare Die and Wafers



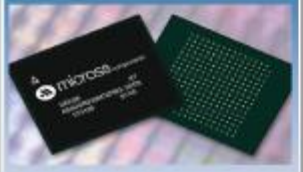
- Wafer Processing: Saw, Sort, Inspect
- Wafer Probe
- Wafer Bumping & RDL
- Wafer Thinning
- Die Characterization, Qualification, KGD
- Lot Acceptance Test
- BOM Management: Long-Term Die Storage

Advanced Interconnect Technology



- Wafer Bumping and Wafer Level Packaging
- Novel Microfabrication and Engineering
- Flip-Chip & Multi-Chip Module Assembly
- 2.5D & 3D Integration
- Development and Prototyping Services

Packaging and Assembly



- Custom Packaging: Plastic, Metal, Ceramic
- Chip Scale Packaging
- Multi-Chip Modules
- Memory, Digital, Analog and Power
- Flows: SCD, MIL-STD-883 (Class B & S), MIL-PRF-38535 (Class Q and V-Assembly & Test)

Component Modification

- BGA Reballing and Ball Attach
- CGA Attach
- Lead Attach
- Trim and Form
- GEIA-STD-0006 Robotic Hot Solder Dipping and Exchange
- Tape & Reel
- 3D Lead Scan

Electrical Testing

- Turnkey Test Services
- Device Characterization Testing: FPGA, ASIC (28NM), RF (80 to 110GHZ)
- High-Speed Digital
- Environmental Burn-In
- PEM-Quals
- Element Evaluation
- Failure Analysis: Engineering and Analytical Services

Environmental Testing

- Electrical / Mechanical / Environmental Reliability Tests
- Life Test / Burn-In (HTOL / LTOL)
- Pre-Conditioning / MRT
- Temperature & Power Cycling
- Temp. Humidity Bias (THB)
- HAST, Thermal Shock
- Mechanical –Shock, Vibration, Acceleration and Gross / Fine Leak

Proprietary Micross Products

SMD/5962 ◦ Hi-Rel Memory ◦ Analog & Power ◦ Retail+

Source: Micross

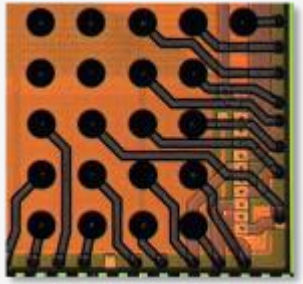
ADVANCED INTERCONNECT TECHNOLOGY (AIT)

Micross advanced/research assembly capabilities are centered on Micross AIT – a 60,000 sq. ft. facility in RTP, NC

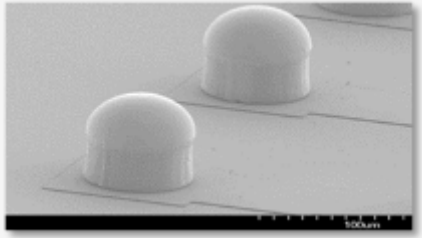
- Acquired from RTI International in 2016
- 30+ Year History in microelectronics technology development
  - CMOS, MEMS and Advanced Packaging
  - Flip-chip bumping development & commercialization
  - (Unitive Electronics spinout – Acquired by Amkor)
- ITAR-Registered (pursuing Trusted Source status)
- AS9100D / ISO9001 Certified
- 20 Degreed Engineers
- Experienced DARPA Contractor – 10 different 3DHI Programs originating from 2001; current active initiatives are CHIPS and ReImagine

Source: Micross

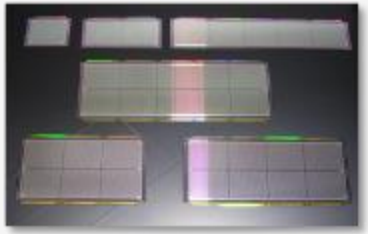
ADVANCED INTERCONNECT IMPLEMENTATIONS



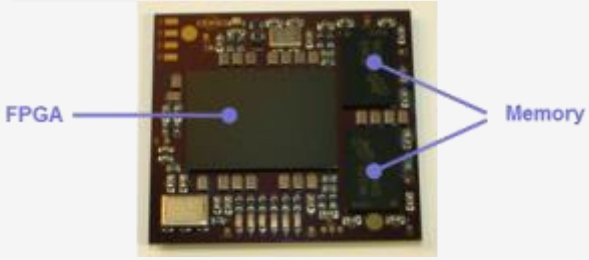
WLP (RDL & Bump)



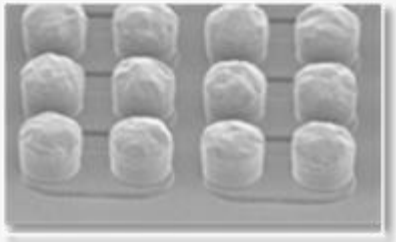
Cu Pillar on I/O for Si photonics



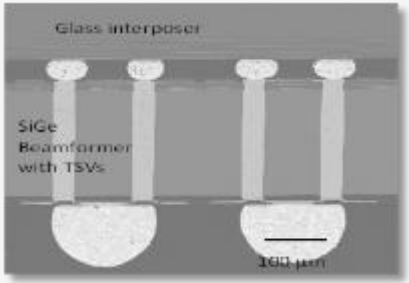
Flip-chip MCM Assemblies for HEP Detectors



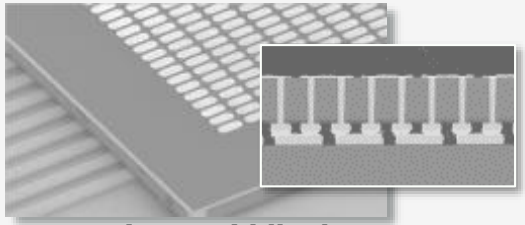
ECM on Si Interposer for SiXis



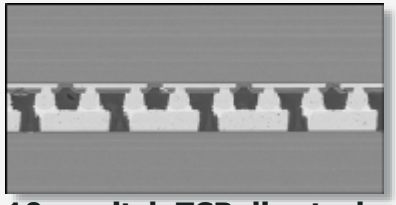
Sub-20μm pitch bumping for IR Detectors for DARPA AWARE with DRS



3DIC Vias last – 3D Radar Tile for DARPA MFRF (with NGMS)



3DIC Vias – middle demo for DARPA AFP

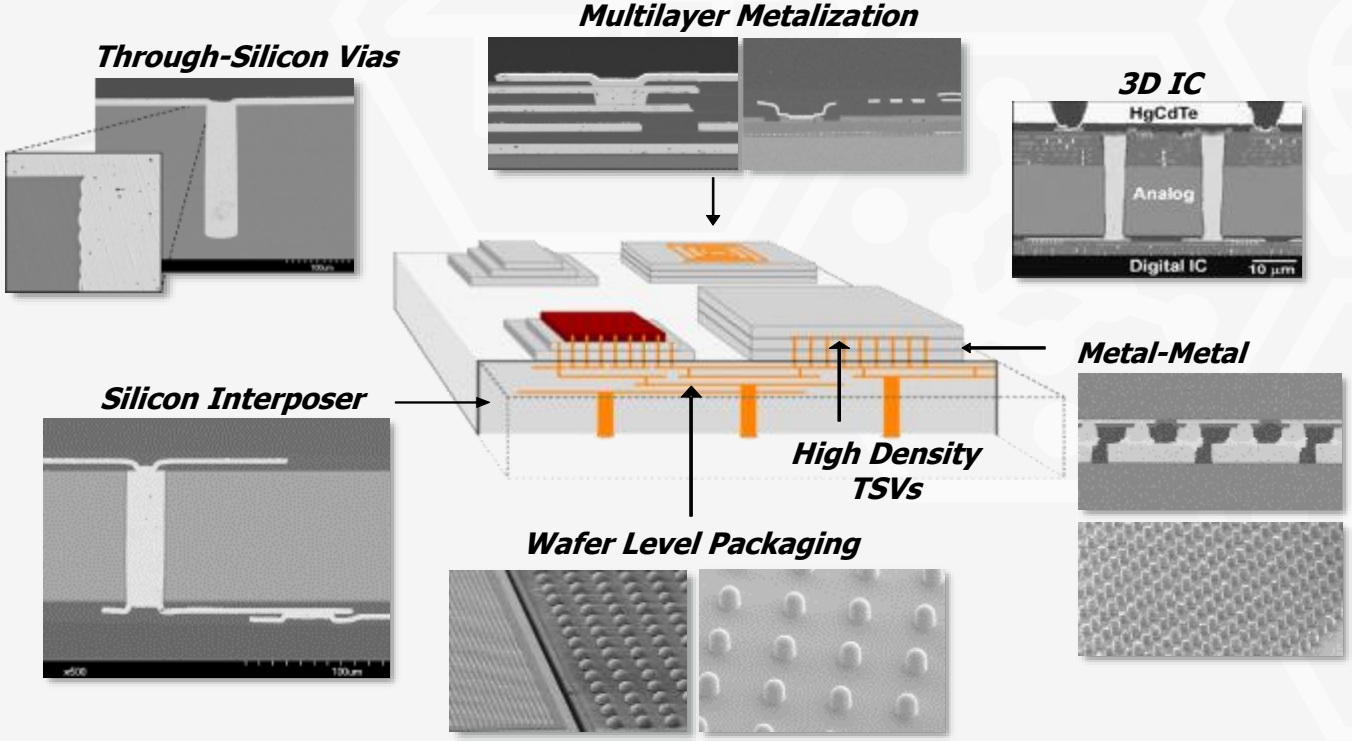


10μm pitch TCB die stacks for 3DTASS Program

Source: Micross

MICROSS AIT FOCUS: WAFER-LEVEL MICROSYSTEM INTEGRATION & PACKAGING

AIT's Toolbox facilitates prototyping of custom integration solutions for a wide array of applications



Source: Micross

MICROSS AIT TECHNOLOGY MRL

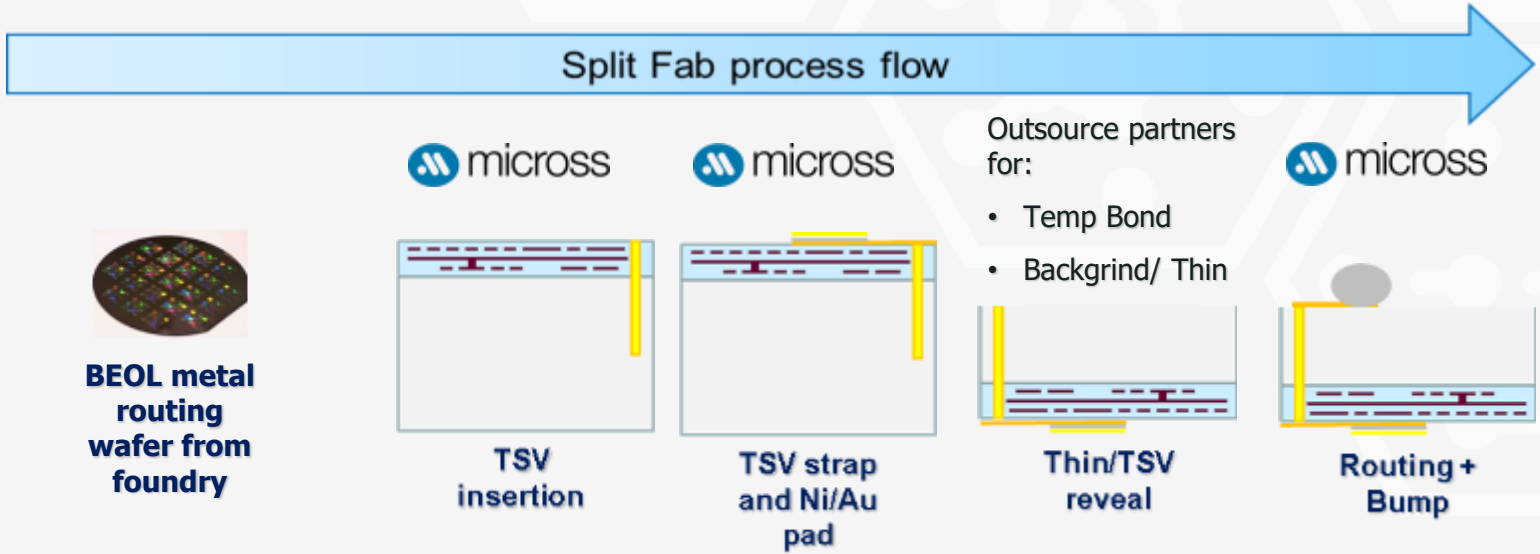
Technology	Typical feature sizes	Materials	MRL	Other Comments
Wafer bumping	50 um pitch min. and up	Pb-Sn eutectic, Pb-free	8-9	Sufficient MRL for DoD volumes
Cu pillar	45 um pitch minimum; typical 50-55 um pitch	Cu with solder cap	8-9	
Sub-20um pitch microbumping	Typically 8-10 um pitch	Cu, Cu/Sn, Au, In	7-8	5 um pitch demonstrated
Si interposers	10-20 um TSVs, 100-200 wafer thickness; 10 um L/S RDL in-house*	Cu RDL, Cu TSVs,	5-6	*Fab partnerships allow BEOL routing density; Filled and barrel coated TSVs available
3DIC- Vias last integration	4-50um TSV diameter demonstrated	Cu TSVs	5	Must design for TSV insertion (keep out zones)
3DIC- Vias middle integration	Wafer finishing of foundry TSV wafers	Cu RDL, bump/pad	5	Only if TSVs available from CMOS foundry
Flip-chip assembly	Typically 25um bumps on 50um pitch for HEP programs	N/A	8-9, Includes Orlando capability for assembly	Single chip and multi-chip assemblies on Si substrates done routinely
Precision assembly	Detector hybridization of microbumped devices, optical bench assemblies	N/A	5	TC bonder with high precision, but low throughput

Source: Micross

CHIPS ECOSYSTEM – SI INTERPOSER

- Limited options for Si Interposer Fabrication on-shore
  - Access to foundries only if purchasing other devices

- Split fab interposers (NGMS-Micross approach) possible through front-end routing by foundry and 3rd party TSV & wafer finishing services

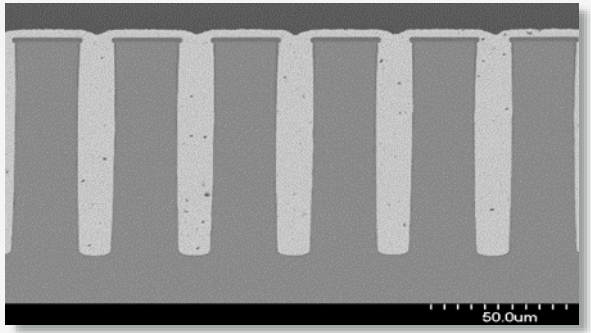


Source: Micross

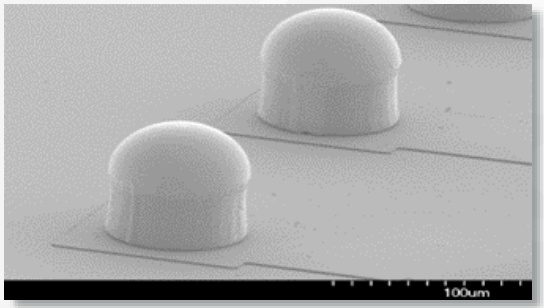
MICROSS INTERPOSER SUPPORT FOR CHIPS

Integration Technology in Support for Northrop Grumman (NGMS) CHIPS effort

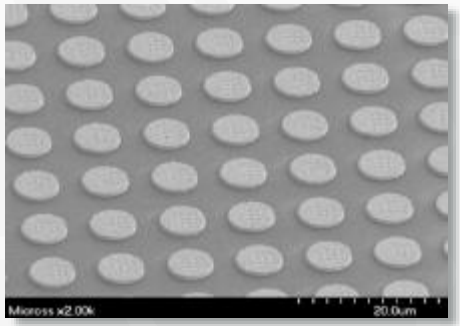
- Post-processing of multiple foundry wafers for heterogeneous integration
- TSV insertion, RDL, UBM/bumps, microbumps and wafer thinning
- Fine pitch bonding development down to 10um pitch



Micross TSVs for Silicon Interposer



Cu Pillar



Au Microbumps

Micross can provide TSV and other post-processing of foundry wafers (IC or interposer)

Source: Micross

APPROACHES FOR FINE PITCH BONDING

Material	Commercial?	Pitch Limit	CMP required?
Cu pillar	Yes- widely adopted	40-60 µm: production 20-30 µm: development	No
Cu/Sn-Cu SLID[1]	(extension of Cu pillar)	5-10 µm	No
Au-Au diffusion	Larger pitch / limited use (Au stud bump, display backplanes)	5-10 µm (less?)	No
Direct/Hybrid Bond (metal and oxide)	CMOS image sensors (wafer bond)	< 5 µm	Yes, requires precise planarity

1- Solid-liquid interdiffusion bonding (scaled Cu pillar, but all Sn is converted to eutectic)

Cu/Sn Advantages: Similarities to Cu pillar, lower bond force than Au or Cu diffusion bond

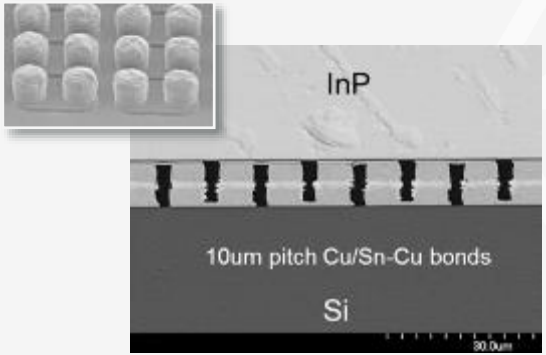
Au Advantages: Ductile / no IMCs (good reliability), no solder to melt / flow (allows further scaling), oxidation / corrosion resistance (possibly avoid underfill need)

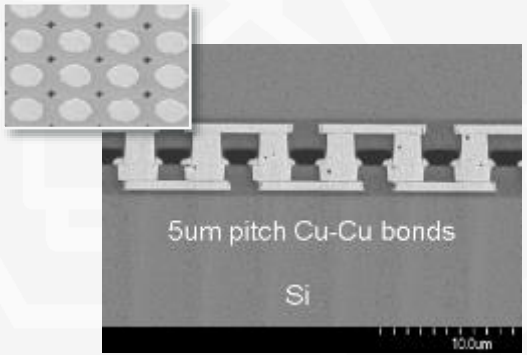
Direct/hybrid bond Advantages: Low bond force, no underfill/chip gap, higher throughput (wafer bond)

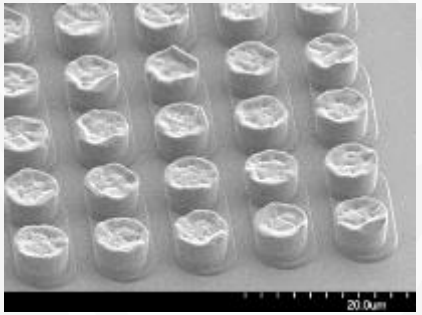
Other Options: Cu-Cu: scalable, but high bond force, requires CMP

Source: Micross

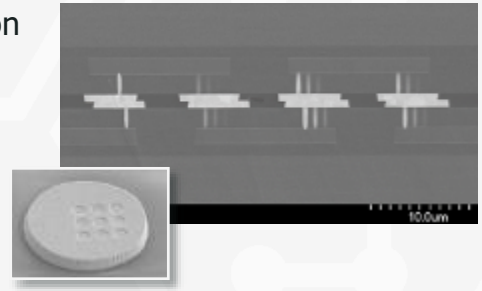
AIT FINE PITCH TECHNOLOGIES







10µm pitch In (top) and Au (bottom)



- Cu pillar for pitches down to 40 microns
- Cu/Sn microbumps for pitches as small as 10 microns for area array detector hybridization
- Cu microbumps demonstrated to 5 micron pitch
- In microbumps fabricated down to 10 micron pitch for detector application
- Au microbumps feasibility demonstrated down to 4 and 7 micron pitch; focused on 10 micron pitch for manufacturability and performance reasons in CHIPS
- Die-to-die and die-to-wafer precision bonding with SET FC-150 Bonder

Source: Micross

SUMMARY

- Micross can offer a broad range of DOMESTIC US services in support of the development and production of advanced Hi-Rel microelectronic components and sub-systems

- Micross AIT has a long history of working with DARPA to develop advanced packaging capabilities that have later been transitioned to volume production
  - Flip-chip bumping (Unitive/Amkor)
  - MEMS (Cronos/JDSU/MEMSCAP)

- As Micross, our goals moving forward:
  - Transition the more developmental technologies (Si Interposer, TSV insertion, fine pitch bonding & assembly) to true DoD capabilities
  - Continue to push the state-of-the-art, next-gen advanced packaging
  - Provide advanced packaging solutions to the Aerospace/Defense community

APPENDIX

PACKAGING & ASSEMBLY

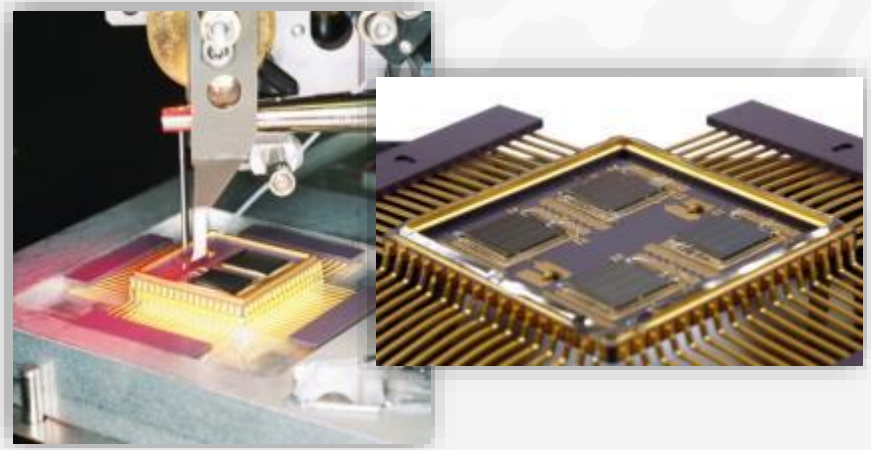
Micross Orlando has an advanced process engineering team skilled in supporting a broad range of packaging technologies in production volumes. Most recently, Micross has started assembling optical transceivers.

Complete Packaging Capabilities

- Hermetic Packaging: Ceramic & Metal Can
- Wafer-level Vacuum/Hermetic Packaging
- Plastic Packaging: CSP/BGA/QFN
- Custom Packaging
- FlipChip/MCM/SiP
- Die Stacking 2.5D /3D

Services & Support

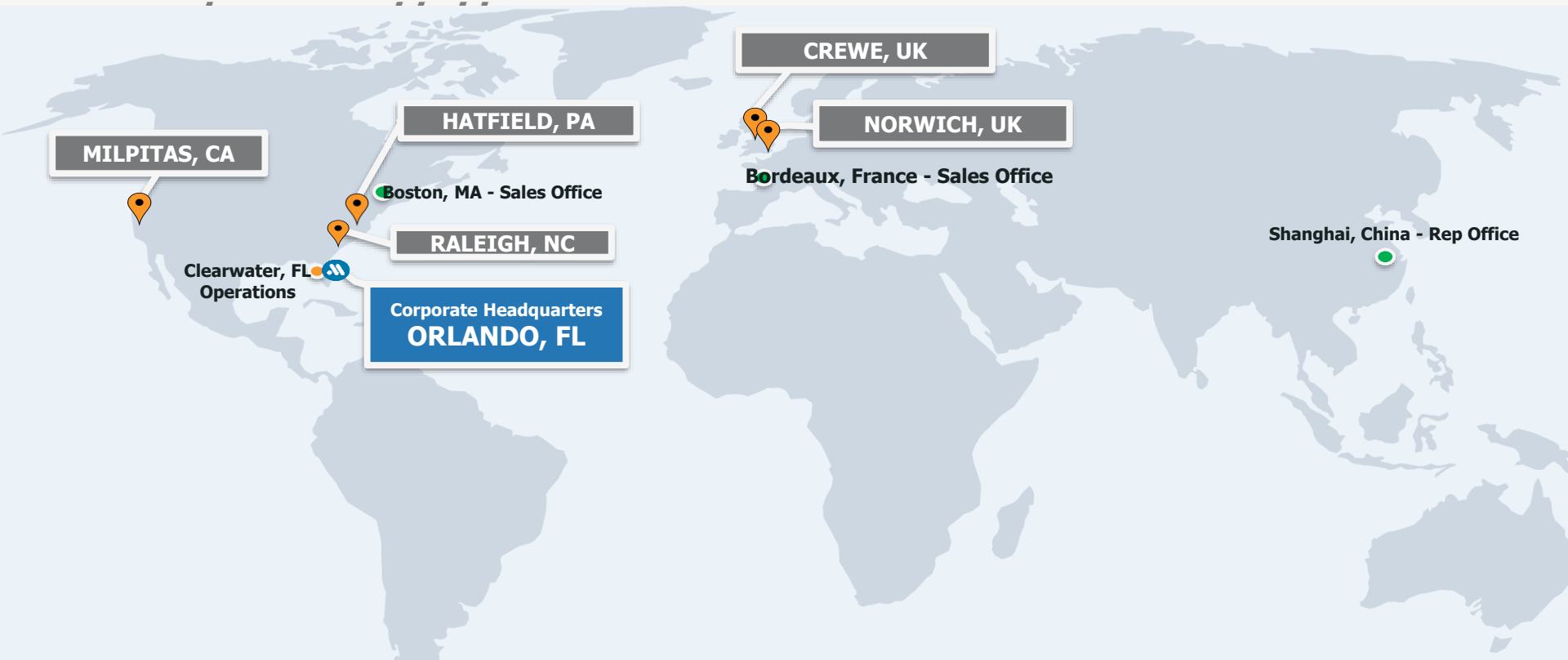
- Package Design
- Full Package Characterization
- Turnkey Assembly & Test
- Reliability Testing & Failure Analysis



Source: Micross

GLOBAL LOCATIONS

Micross operates out of 10 locations across 3 continents, with more than 400



Source: Micross

QUALITY ACCREDITATIONS

Micross has the Quality Processes and Security Controls in place to support its full range of service offerings.

- **AS9100**
- **ISO 9001**
- **DLA Lab Suitability (MIL-STD-883)**
- **MIL-PRF-38535 Q and V (Assembly & Test)**
  - ***Crewe UK (QML Q, V, Y for Column Attach)***
- **MIL-PRF-38534 Class H**
- **ITAR-Registered**
- **Trusted Source (DMEA)**

Source: Micross

RECENT MICROSS-SUPPORTED DARPA PROGRAMS

Program Title/Description	Contract Dates	Sponsoring Agency	Program Manager(s)
Common Heterogeneous Integration and Intellectual Property Reuse Strategies **(CHIPS)**	8/2017 to present	DARPA MTO	Andreas Olofsson, Dan Green
Reconfigurable Imaging **(ReImagine)**	6/2017 to present	DARPA MTO	Whitney Mason, Jay Lewis
Advanced Scanning Technology for Imaging Radars **(ASTIR)**	8/2015 to 10/2015	DARPA STO	Bruce Wallace
Multifunction RF **(MFRF)**	11/2013 to 3/2017	DARPA STO	Bruce Wallace
Advanced Wide FOV Architectures for Image Reconstruction and Exploitation **(AWARE)**	10/2012 to 2016	DARPA MTO	Nibir Dhar
Low Cost Thermal Imager Manufacturing **(LCTI-M)**	2/2012 to 2015	DARPA MTO	Nibir Dhar
Advanced Focal Plane Array Processor **(AFP)**	8/2008 To 11/2013	DARPA MTO	Carl McCants
3D Technology for Advanced Sensor Systems **(3DTASS)**	4/2008 To 5/2012	DARPA MTO / SPAWAR	Cynthia Hanson
Vertically Interconnected Sensor Arrays **(VISA)**	11/2002 to 8/2007	DARPA MTO	Ray Balcerak, Stuart Horn
Advanced Processing Techniques for Fabrication of 3D Microstructures **(3DM)**	9/2001 to 7/2008	DARPA MTO / SPAWAR	Cynthia Hanson

Source: Micross

WAFER BUMPING & FLIP CHIP ASSEMBLY

Mature Technology / Commercial Services

- 100 to 200 mm wafers or cored 300 mm
- Primarily low volume Aerospace & Defense, R&D and small commercial
- Bumping of wafers directly for clients or possibly through MOSIS

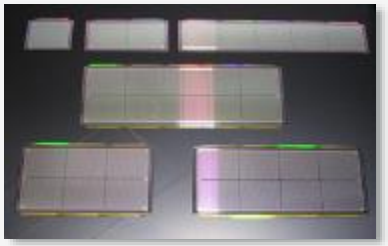
C4 Wafer Bumping & Assembly

- Pitch Range: >200 µm down to 50 µm

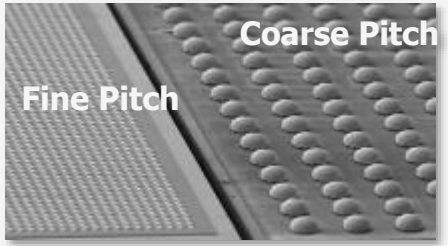
Cu Pillar Technology

- Able to support 55 µm commercial pitch
- Development to 30-40 µm pitch or less

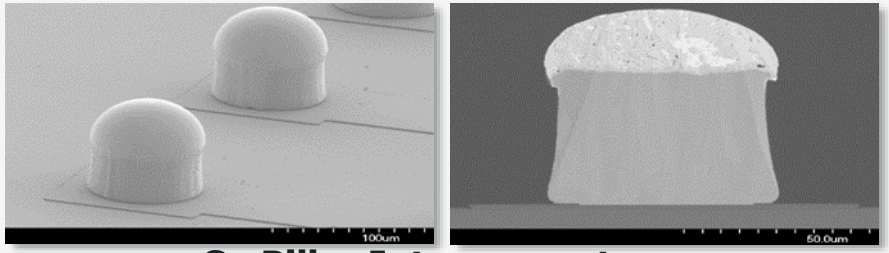
Redistribution (RDL) – electroplated Cu



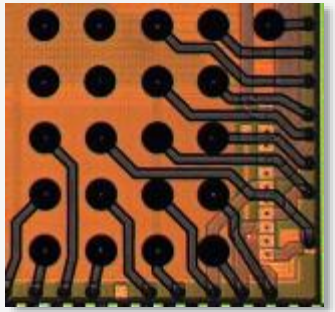
Bonded Flip-chip/ MCM Assemblies



C4 Solder Bumps



Cu Pillar Interconnects



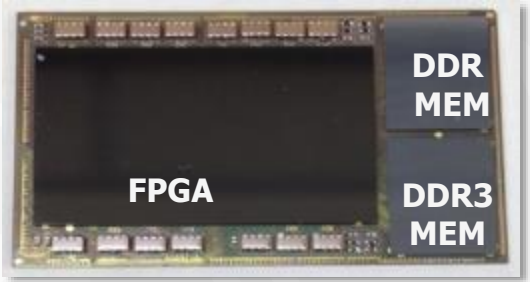
Redistribution (RDL)

Source: Micross

2.5 & 3D INTEGRATION TECHNOLOGY

Developmental Technology (15+ Years)

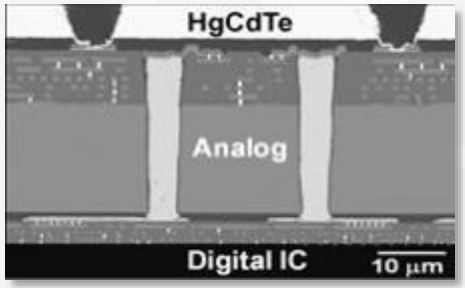
- Support for demonstration, prototype, development lots
- Additional infrastructure required for commercial capability



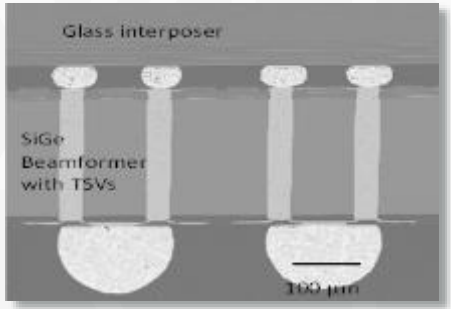
ECM on Silicon Interposer (with SixiS)

Advanced 2.5D & 3D Integration Demonstrations

- Post-processing of TSVs in IC wafers (CMOS, SiGe)
- Functional 3D device stacks demonstrated in multiple development programs
- Si and glass interposer fabrication and 2.5D assemblies



3D ROIC/FPA- DARPA VISA & AFP (with DRS)



Hetergenerous 3D Radar-Tile DARPA MFRF

Source: Micross

INTERPOSER WAFER PREP / FABRICATION CAPABILITIES

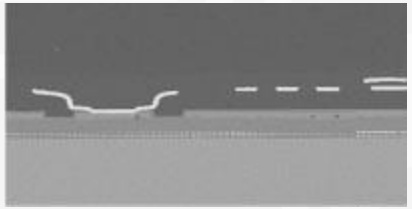
Interposer Processing Options:

1. Wafer finishing: BEOL + TSVs from foundry
2. Split-fab: Micross TSV-last in foundry BEOL wafers
3. Micross full interposer fab (TSV+metal layers)

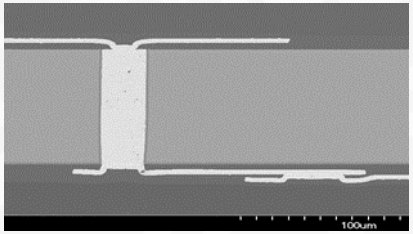
} ***High density interposer options***

(Examples below)

3a. Cu RDL + spin-on dielectric: Limited to ~10 µm L/S, 2-3 layers

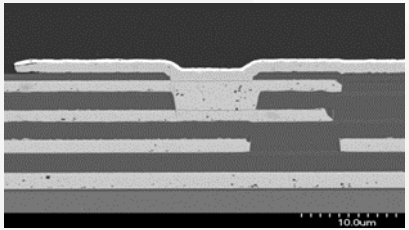


Cu RDL Multi-level metal

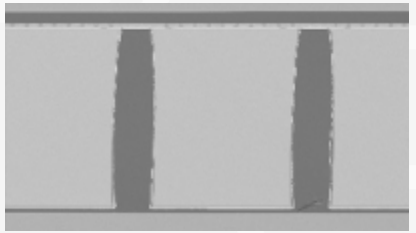


Cu RDL interposer w/TSVs

3b. Cu dual-damascene: Limited development (higher cost & cycle time)



Cu DD multi-level metal



Cu DD interposer w/TSVs

Source: Micross

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