Wideband Amplifier

Ruben Miguel Gomes Machado, *Student 67710, MEEC IST*

***Abstract*—In System on a Chip integrated circuits, the integration of several circuits into only one package leads to noise that some circuits introduce in the power supply to impact the operation of other circuits. Thus, to evaluate the power supply noise sensitivity, the measurement of PSRR and line transient parameters is necessary. Testing and profiling these parameters is accomplished through the use of an amplifier. In this work, the project for a wideband amplifier is carried out. The development of all its building stages is presented: the architecture choice, simulation, layout of the printed circuit board and the necessary setup for its physical implementation. The output of this amplifier has a demanding specifications the bandwith, low output impedance and variable gain. It is designed with the purpose of powering analog and mixed integrated circuits, to assess their power supply disturbances rejection. The wideband amplifier, in addition to amplifying signals and providing the necessary current to the system in test without entering in unstable behavior, this is, the amplifier will need to adapt to different conditions without compromising neither performance nor reliability. Due to the expected temperature increase during circuit operation, a cooling system that maintains its correctness is taken into consideration. The amplifier is then designed using the metal substrate printed circuit board technology, designated by Insulated Metal Substrate (IMS).**

***Index Terms*—Amplifier, Stability, PSRR, PCB, IMS**

I. Introduction

Nowadays, due to the advance of integrated circuit technologies, that lead to a continuous decrease of voltage and currents during operation and accentuated the noise presence, it is paramount that electronic systems are tested for different settings as to ensure they do not compromise their correct operation. The PSRR specification measures a system's tolerance to power supply voltage changes, and its determined using the expression 1.

$$PSRR[dB] = 20log_{10}(\frac{\triangle Vsupply}{\triangle Vout}) \quad (1)$$

The base method for measuring a system's PSRR consists in using a direct voltage source (VDC) to establish the operation mode, and an alternate voltage source (VAC) to add noise to the power supply [1]. However, the frequency range is limited by the inductor and the capacitor. Typically, this setup only allows for measurements in the medium frequency range (approximately from 1kHz to 500kHz).

An alternative approach uses a large wideband amplifier to power the system to be used, allowing PSRR measurement for both low and high frequencies. However, capacitive loads at the amplifier's output might lead to instability. Therefore, achieving stability is one of the great challenges in *driving* a capacitive load.

In this context, the current work involves the project, simulation and layout of a wideband amplifier with specifications as indicated in Table I. This amplifier must be capable of powering analog and mixed integrated circuits with the aim of assessing their power supply noise rejection, more specifically, their PSRR and line transient.

Parameter		Unit
Bandwith	DC a 10M	Hz
Power	150	W
Output Voltage	$\pm$6	V
Output Current	25	A
Gain	1 a 4	-
Input Voltage	$\pm$10	V

TABLE I
WIDEBAND AMPLIFIER SPECIFICATIONS.

This document is structured as follows: section 2 presents available market solutions; section 3 presents the proposed solution, followed by methodology used for architecture simulation and validation; section 4 presents a comparative study about the existing PCB manufacture and cooling technologies. All the steps and decisions taken during the layout process are also here detailed; section 5 compares the achieved results with the initially set goals, finishing with future work suggestions.

II. Solutions on the Market

The manufacturer Accel Instruments has three amplifier models. The TS200 is a power supply module with DC bandwith at 1MHz. This instrument allows several laboratory tests like PSRR measurement for LDOs, battery simulation, transient response assessment and can also operate as a power supply, providing an direct or alternate output voltage (from -10 to +70V in the TS200-3B version). This module can work as a current amplifier, providing a current above 4A in the TS200-0A version or power up to 65 Watts. The TS200 model accepts function generator signals inside the $\pm$20V range, with the possibility to amplify them up to a factor of 10 for some model versions [2].

There is also a slightly better model, the TS250, which can generate waveforms, and as such, does not need function generator input. The main differences to the above mentioned model relate to the output voltage, current and power ranges. More specifically, a voltage output range from -40V to 40V for the TS250-3 and from -6V to 65V for the TS250-7 and a maximum current output of 6A for the TS250-0A. This model has a maximal power output of 75 Watts[3].

A more recent model, the TS400, has the closer characteristics to the wideband amplifier developed in this work, and so, its specifications are partially different from the above mentioned models. The bandwith is much larger comparing to the previous Accel Instruments models, allowing DC signals at 10Mhz, which in the previous modules was ten times inferior, allowing an output tension range of $\pm$15V and current of $\pm$5A

[4]. However, no more detailed information about this model was made available by the manufacturer.

The Krohn-Hite Corporation manufacturer also offers a range of wideband amplifiers, specifically the models 7500, 7600M and 7602M [5]. Model 7500 has a 1MHz DC bandwith, with maximum output power of 75 watts, output voltage range from 0V to ±200V, variable gain from 10 to 100 and a maximum output current of 884mA [6].

Models 7600M and 7602M have identical specifications, 1Mhz DC bandwith, variable gain from 0 to 125 with a maximum output current of 200mA. The power for one of these modules is different, being 17Watts for 7600 and 34 Watts for 7602M. The voltage output tension for the former might range from 0 to ±200V while from 0V to ±400 for the latter [7].

III. Wideband Amplifier

A. Architecture

Operational Amplifiers have continuously improved their performance, specifically the response time and bandwidth. The most recent, as known as high-speed amplifiers, can reach bandwidths in the range of hundreds of Mhz, which, given their performance, must be taken into consideration during dimensioning, to assure stability. It is important to highlight that previously design architecture for low frequencies, when used with high-speed op-amps, have to be revised with greater detail [8].

The wideband amplifier architecture projected for this work presented in Figure 1 consists of 64 blocks in parallel, each one equal to the one presented inside the dashed line. The op-amp used in this architecture is the integrated circuit THS6012. The process that lead to the creation of this schematic now follows.

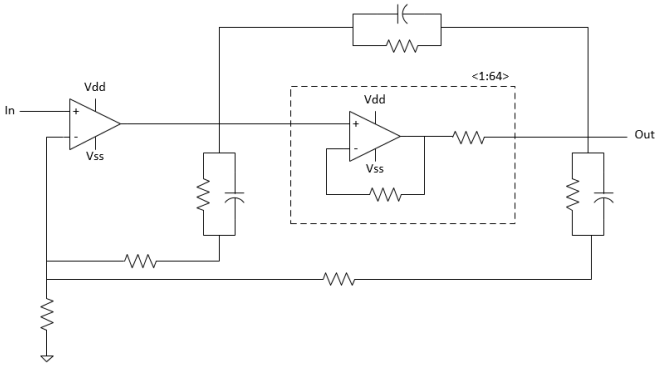

Fig. 1. Wideband Amplifier schematic.

The chosen IC, the THS6012 manufactued by Texas Instruments, consists of two independent op-amps, with current feedback topology, design to operate in high-speed and made specifically to provide a minumum output current of 400mA and maximum of 800mA [9]. The current feedback topology op-amps are a type of transimpedance amplifiers, that is, the output voltage is dependent on the inverting input current. These have advantage over voltage feedback amplifiers because of gain and bandwidth independence [10].

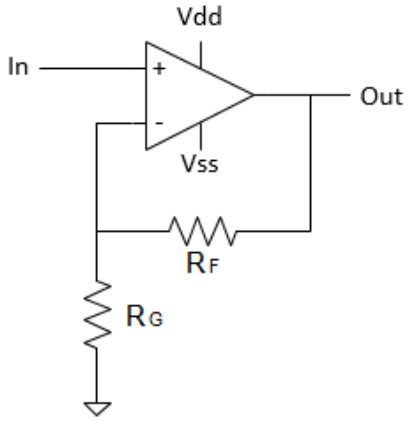

Fig. 2. Non-inverting configuration.

Consider the non-inverting configuration presented in Figure 2, with the goal of studying the op-amp behavior in relation to the resistors R_F e R_G values.

The operational amplifier bandwidth is inversely proportional to the feedback resistor value (R_F). Given the wideband amplifier, will be used to supply power to integrated circuits, the operational amplifiers will have a load at their outputs. As the load resistance increases, the op-amp's output resistance becomes less dominant, specifically in the low frequency range. To balance this effect, the feedback resistor should change accordingly with the load increase[9]. However, for most applications, the manufacturer's recommended feedback resistor value for a better tradeoff between bandwith and phase margin, leading to a stable amplifier, is 1kΩ [9], and thus this is the value fixed in the circuit dimensioning.

The best option for gain adjustment is through adjusting the gain resistor's value, (R_G), the resistor at the inverting op-amp input [11]. Similarly, the gain can also be adjusted through the feedback resistor, but as above mentioned, this resistor also defines the bandwidth, and modifying it for adjusting gain would also change the bandwidth. It should also be mentioned that by increasing the feedback resistor's value, a decrease on the closed-loop gaind would ensue, which would generate an increase in distortion[9]. As such, having amplifier gain control to be bandwidth independent is one of the biggest advantages of current feedback topology amplifiers [12].

Taking into a count the amplifier purpose, it is necessary to take the proper care relative to the performance impact of the op-amps for different output loads, specifically the capacitive loads, which can lead to instability [13].

The THS6012 op-amp is internally configured for maximum bandwidth and high slew rate. However, with a capacitive load higher than 10pF at its output, this creates a response with oscillations [9]. This happens due to the capacitive load (C_L) combined with the op-amp's output resistor (R_O) creating a pole in the feedback loop. This pole generates a phase shit in the closed-loop, decreasesing the phase margin and thus bringing the system out of stability [8]. Using the imposed pole's frequency, (f_p), which can be obtain using equation 2, and unitary gain frequency (f_u), one can determine the phase shift, using the equation 3.

$$f_p[Hz] = \frac{1}{2\pi R_O C_L} \tag{2}$$

$$phaseshift = tan^{-1}\frac{f_u}{f_p} \tag{3}$$

Therefore, to maintain op-amp stability, external counterbalance is needed resorting to the capacitive load isolation method: a resistor (R_X) is applied at the op-amp's output. The manufacturer recommends a value of 10Ω for the compensation resistor [9], and this was the value used for the dimensioning. This resistence introduces a zero in the transfer function, with the goal of reducing the phase shift in higher frequencies [14].

To ensure that the wideband amplifier provides a current up to 25A to a charge at its output, it was decided to make a parallel of 64 follower blocks, with R_X resistor balancing each one. In Figure 3, the follower block is presented, with the dimensioned resistor values R_F=1kΩ and R_X=10Ω.

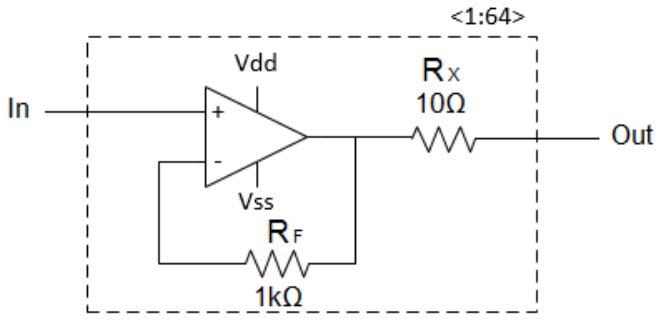

Fig. 3. Follower block with isolated load resistor.

In order to lower the control voltage impedance, to force the input voltage of the follower blocks, an amplification stage dependent on R_G is added .

In Figure 4 the wideband amplifier architecture is presented, consisting of two stages, a delay loop and two feedback loop. The delay loop, named Nested-Miller compensation, allows phase margin control [15]. The feedback loops, consisting of a resistor in series with the parallel of a resistor and a capacitor, increase the circuit's response time for high frequencies, followed by a resistor in series, the resistor for tension gain adjustment, R_G, with descriminated values from 1 to 4 according with the Table II.

R_G (Ω)	Gain
100k	1
3k	2
1.5k	3
1k	4

TABLE II
GAIN ADJUSTMENT WITH RESISTANCE.

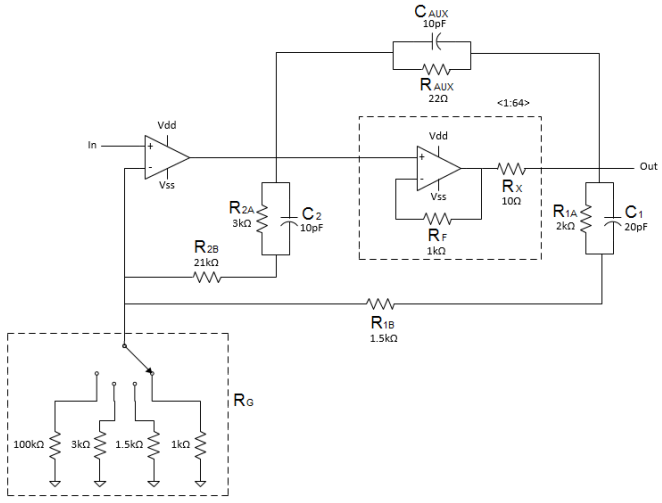

Fig. 4. Wideband Amplifier Architecture.

B. Simulation

The analysis of the architecture's required parameters demands the use of different stimuli signals. Other important factors for the amplifier characterization are the used frequencies, gain, output load and current load that may have different consequences on the wideband amplifier behavior.

1) Transient Response: With the intent of analyzing all the frequency, gain and applied load variants, simulations are presented with input signal frequency at 100kHz, 1MHz and 10 MHz, with resistive and capacitive loads of variable value at the wideband amplifier's output.

By setting a sine wave signal with 2V of amplitude and 100kHz frequency, depicted in Figure 5, in a load free situation, it is possible to verify in Figure **??** that the amplifying criteria is achieved.

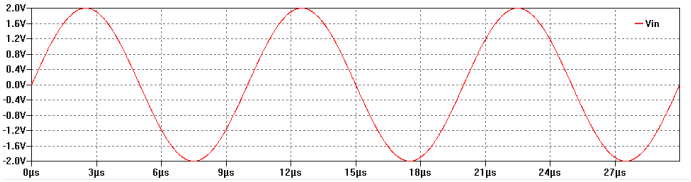

Fig. 5. Sine wave signal with 2V of amplitude and 100kHz frequency.

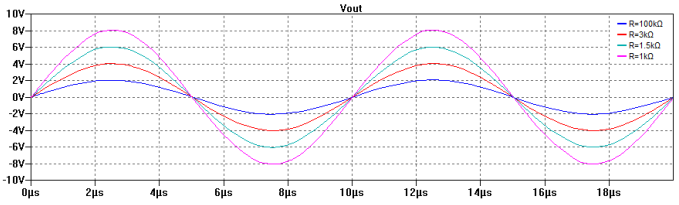

Fig. 6. Time simulation without load at 100kHz.

Given that the amplifier is to be used to supply analog and mixed integrated circuits, resistive loads were considered (R_L), ranging from 1 to 10 Ω and capacitive loads ranging

from 1 to 10 μF, to evaluate their operation, set at the amplifier's output as shown in Figure 7.

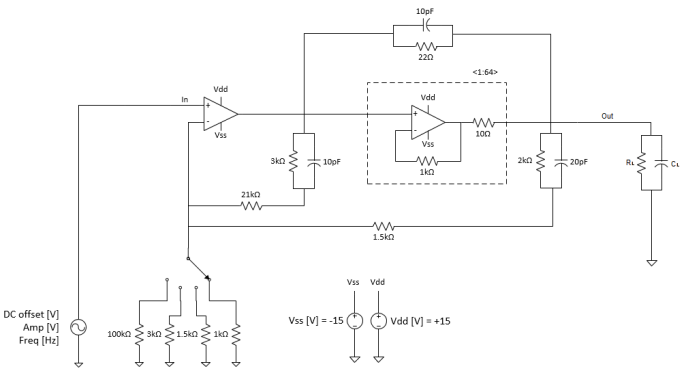

Fig. 7. Circuit configuration with load for test simulation.

Maintaining the same amplitude and input signal frequency, 2V e 100kHz, in Table III are presented the maximum absolute errors referring to the difference between maximum expected output voltage and maximum measured output voltage, for the different gains, considering the configurations with and without loads.

	Absolute Error (V)				
	W/o	R_L=1Ω	R_L=10Ω	R_L=1Ω	R_L=10Ω
Gain	Load	C_L=1Ω	C_L=1μF	C_L=10μF	C_L=10μF
1	0.048	0.034	0.03	0.002	0.03
2	0.010	0.084	0.01	0.09	0.02
3	0.020	0.114	0.02	0.09	0.001
4	0.067	0.118	0.01	0.01	0.008

TABLE III
ABSOLUTE ERROR FOR TIME SIMULATIONS FOR F=100KHZ WITH AND WITHOUT LOAD.

By analyzing Table III, in the open circuit configuration, the mean absolute error is 36mV. By using the architecture with gain equal to 2, a closer waveform to the expected signal is obtained at the output.

In the circuit with load configuration, the smaller absolute errors occur for the maximum load values, with a maximum error of 118mV for the configuration of smaller capacitive and resistive loads with gain 4.

As previously described, there are three factores that can influence the wideband amplifier operation. By sweeping the available gain range for different output loads and applying a sine wave signal with 100 kHz frequency the expected circuit operation was achieved, in order to analyse the frequency range, a higher frequency signal must be applied.

As such, an input signal with the same amplitude is used, but with at a frequency of 1MHz, as depicted in Figure 8.

In Table IV, maximum absolute errors for different loads and gains are presented. The mean absolute error for the configuration without load is 63.5mV, slightly higher than in the 100kHz situation, recording smaller errors for gains 1 and 2 and bigger errors for gains 3 and 4. When capacitive and resistive load are present, one can verify that with the gain increase the voltage output also increasingly differs from the

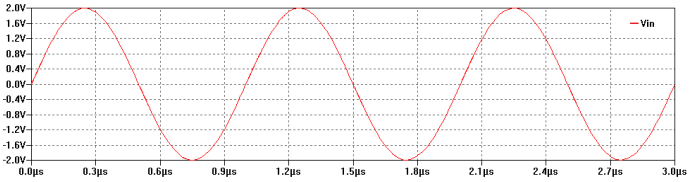

Fig. 8. Input Signal with 2V amplitude and 1MHz frequency.

expected, with gain 4 and output load R_L=1μF and C_L=1μF recording a superior attenuation of 0.35 V.

	Absolute Error (V)				
	W/o	R_L=1Ω	R_L=10Ω	R_L=1Ω	R_L=10Ω
Gain	Load	C_L=1Ω	C_L=1μF	C_L=10μF	C_L=10μF
1	0.044	0.02	0.02	0.014	0.024
2	0.045	0.16	0.1	0.16	0.091
3	0.070	0.23	0.15	0.25	0.14
4	0.095	0.35	0.21	0.34	0.19

TABLE IV
ABSOLUTE ERROR FOR TIME SIMULATIONS FOR F=1MHZ WITH AND WITHOUT LOAD.

Given that the intended bandwidth for the amplifier is 10MHz, to verify the amplifier operation, an input signal of 2V amplitude as above used is applied, but with frequency of 10Mhz, as depicted in Figure 9.

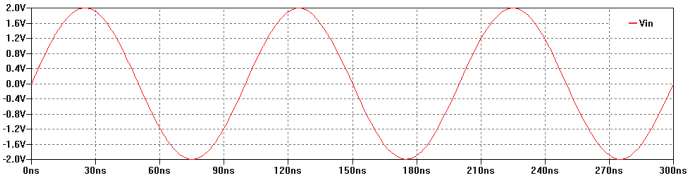

Fig. 9. Input signal with 2V amplitude and 10MHz frequency.

In Table V the simulations maximum absolute errors are presented. In the configuration without load, the lower absolute error occurs for unit gain, and one can verify that for higher gains the attenuation is much more accentuated than in the previous approaches. With load the behavior is similar but not so accentuated, with largest error for the minimum load of 0.35V.

	Erro Absoluto (V)				
	W/o	R_L=1Ω	R_L=10Ω	R_L=1Ω	R_L=10Ω
Gain	Load	C_L=1Ω	C_L=1μF	C_L=10μF	C_L=10μF
1	0.13	0.016	0.02	0.037	0.024
2	1.16	0.016	0.096	0.16	0.092
3	2.12	0.23	0.15	0.25	0.15
4	3.08	0.35	0.20	0.34	0.19

TABLE V
ABSOLUTE ERROR FOR TIME SIMULATIONS FOR F=10MHZ WITH AND WITHOUT LOAD.

According to specifications, the amplifier must be able to provide a maximum current of 25A. As such, applying the same input signals as in the previous situations, a current source is set at the wideband amplifier's output, to verify its operation behavior.

The simulations show that the wideband amplifier, at high frequencies, is bounded by an output current of 2A.

In the following Table VI the maximum absolute errors for the 2V signal with 100kHz, 1MHz and 10Mhz signals are presented.

f (Hz)		100k		1M		10M	
I_{OUT} (A)		1	25	1	25	1	2
Gain	1	0.024	0.44	0.012	0.46	0.14	0.16
Gain	2	0.014	0.048	0.090	0.55	1.18	1.17
Gain	3	0.008	0.44	0.13	0.58	2.13	2.15
Gain	4	0.029	0.43	0.16	0.61	3.09	3.11

TABLE VI
TIME SIMULATION ABSOLUTE ERROR.

As one can check in Table VI, as the output current increases, for higher gains, the output voltage attenuation increases, being more drastic for higher frequencies.

The input signal frequency increase also has another consequence, consisting on the increasing phase difference between input and output signals. However, this subject is explored in more detail in a later subsection, where the wideband amplifiers frequency response is analyzed, more specifically, its amplitude and phase.

2) Line Transient: Similar to the previous subsection, this section reports the simulation results for a step input signal with 2V amplitude, depicted in Figure 10. The goal is to check the line transient between the applied voltage maxima, assessing the line transient slew-rate as well as its stabilization time, at 1 and 5 %, depending on the used load. The settling time (t_s) is the time it takes for the system response to be bounded by a defined margin for the final value.

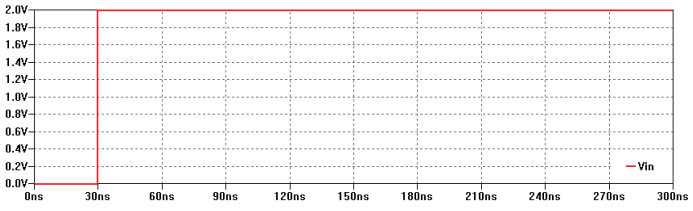

Fig. 10. Input step with 2V amplitude.

Taking the different load configurations, in Tables VII and VIII, the settling times for 1% and 5% are presented.

	Load				
	W/o	R_L=1Ω	R_L=10Ω	R_L=1Ω	R_L=10Ω
Gain	Load	C_L=1μF	C_L=1μF	C_L=10μF	C_L=10μF
1	144.12	170.71	162.73	175.63	160.37
2	208.69	210.30	222.93	220.00	243.56
3	224.19	229.12	226.01	230.83	228.14
4	221.88	231.31	240.73	228.50	241.49

TABLE VII
SETTLING TIME (NS) AT 1% FOR DIFFERENT GAINS AND LOADS.

As one can verify, the final voltage is achieved in less than 250ns, considering the 1% margin. For the 5% margin, the largest settling time is recorded for gain 4, with R_L=10Ω and C_L=1μF, with t_s=163.07ns.

	Load				
	W/o	R_L=1Ω	R_L=10Ω	R_L=1Ω	R_L=10Ω
Gain	Load	C_L=1μF	C_L=1μF	C_L=10μF	C_L=10μF
1	101.61	103.55	101.37	102.29	102.21
2	143.56	146.69	145.30	144.86	149.92
3	150.46	156.67	147.77	156.47	153.84
4	155.71	161.09	163.07	158.98	154.94

TABLE VIII
SETTLING TIME (NS) AT 5% FOR DIFFERENT GAINS AND LOADS.

Another important characteristic to take into analysis, that defines the amplifier ability to commute between voltage extremes, is the slew-rate. Measuring slew-rate, given by the maximum voltage change rate by time unit, requires a brusque change in the input voltage to occur so that the highest output voltage change rate is obtained. As such, considering the previous simulation values, Table IX presents the several slew-rate values obtain for different gains and loads.

	Load				
	W/o	R_L=1Ω	R_L=10Ω	R_L=1Ω	R_L=10Ω
Gain	Load	C_L=1μF	C_L=1μF	C_L=10μF	C_L=10μF
1	19.93	19.15	19.71	19.44	18.88
2	35.78	33.78	35.13	35.15	33.87
3	52.05	48.80	50.91	51.30	49.21
4	68.33	63.79	66.65	67.43	64.52

TABLE IX
SLEW-RATE (V/μS) FOR DIFFERENT GAINS AND LOADS..

As one can inspect in the Table IX, for the configuration without load, the amplifier has the highest slew-rate values, with its maximum for gain 4. However, with load, the same suffers a decrease, with the lowest value for unit gain and loads R_L=10Ω and C_L=10μF.

3) DC Response: This section analyses the amplifier response to a DC signal, decpited in Figure 11 to determine the possible voltage ranges, for input and output, according to gain and applied load.

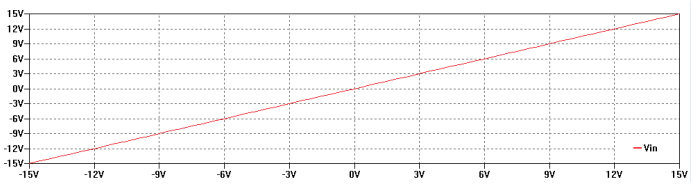

Fig. 11. Input DC signal *sweep*.

In the Table X, one can consult the several positive saturation voltage values for the different load configurations used.

4) Frequency Response: In this section, the wideband amplifier frequency domain analysis is presented, with the intent of verifying stability with resource to the frequency response diagram, by looking for the frequency amplitude and phase values.

A negative feedback system, like the one depicted in Figure 12, has a transfer function given by the equation 4.

$$\frac{V_O}{V_I} = \frac{A(j\omega)}{1 + A(j\omega)\beta(j\omega)} \tag{4}$$

	Load				
Gain	W/o Load	R_L=1Ω C_L=1μF	R_L=10Ω C_L=1μF	R_L=1Ω C_L=10μF	R_L=10Ω C_L=10μF
1	13.29	11.23	13.04	11.24	13.04
2	13.29	11.26	13.03	11.27	13.03
3	13.29	11.26	13.03	11.27	13.03
4	13.28	11.26	13.03	11.26	13.03

TABLE X
SATURATION VOLTAGE FOR THE DIFFERENT GAINS AND LOADS.

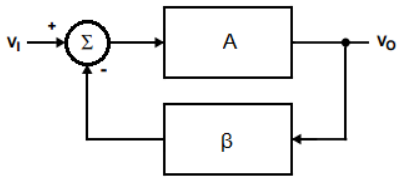

Fig. 12. Block diagram of a feedback system.

When the transfer function denominator equals zero, the system becomes unstable, meaning that the closed loop gain becomes undefined due to the division by zero [16], and in open loop it means that amplitude is unitary and phase is 180º, as one can check using equations 5, 6 and 7, and in accordance with the Barkausen criteria.

$$1 + A(j\omega)\beta(j\omega) = 0 \tag{5}$$

$$1 + |A(j\omega)\beta(j\omega)|e^{-j\phi(\omega)} = 0 \tag{6}$$

$$|A(j\omega)\beta(j\omega)| = 1 \quad \text{e} \quad \phi(\omega) = 180^{\text{o}} \tag{7}$$

So that the system can amplify in negative feedback, two conditions must be established: $|A(j\omega)\beta(j\omega)| > 1$ and $\phi(\omega) < 180^{\text{o}}$. For this, the Phase Margin is introduced, a value given by the equation 8, which translates the needed phase change for the system in open loop, for unit gain, so that the closed-loop system becomes unstable. Therefore, so that the system is stable, the phase margin must be positive [17]. On the other hand, one can also obtain the change, expressed in dB, for the transfer function gain in open loop, for the –180º phase, so that the closed-loop system becomes unstable.

$$PM = 180 - \phi(\omega) \tag{8}$$

To determine the phase and amplitude of the parameters $A(j\omega)\beta(j\omega)$, one needs to interrupt the circuit, as shown in Figure 13, set the input voltage of the system to the ground and apply an input signal of varying frequency given by V_{TI} to analyze the answer V_{TO}.

Given the amplifiers complexity, the stability circuit analysis with multiple feebacks can only be carried through assuming the existence of local feedbacks, individually stable [17], so that the architecture simulates a system of only one feedback loop, as the one decpited in Figure 12.

The amplifier's architecture has two local and stable feedbacks, so one can take the system as only one global feedback

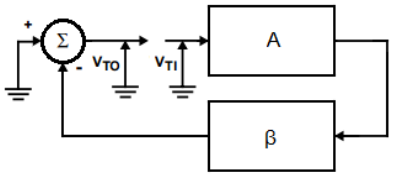

Fig. 13. Block diagram of a system with interrupted feedback.

loop. From the same circuit interruption circuit, in Figure 14 the simulation schematic is represented.

The circuit's interruption is simulated by using and indutance of value $L = 1TH$ and the input test signal is set in series with a capacitor of value $C = 1T$, with the intent to block the DC signal component.

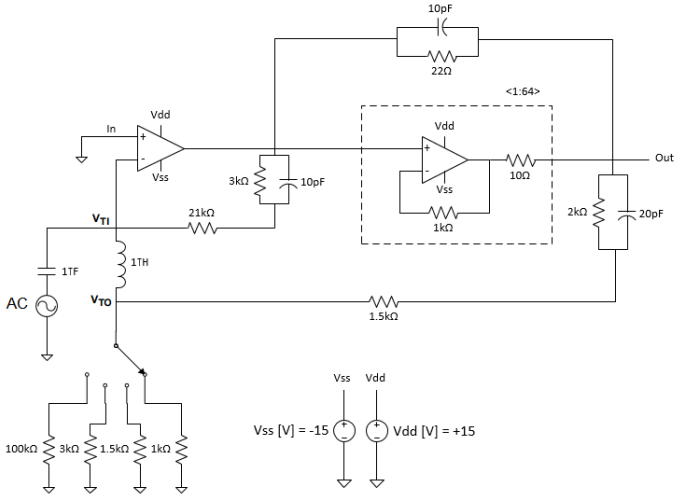

Fig. 14. Test circuit configuration for simulation in frequency domain.

Through an AC simulation with different gains without load, using the LTSpice software, a frequency response is presented in Figure 15, for amplitude and phase, with output signal V_{TO} for an input test signal V_{TI}.

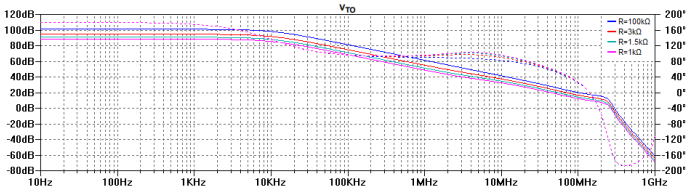

Fig. 15. System's frequency response in open-loop.

In Table XI the phase margin and gain margin are presented for the several configurations. As one can observe, the phase margin is positive and increases with amplifier gain increase, with the same being noted for the gain margin.

IV. Wideband Amplifier Implementation

A. PCB Technologies and Cooling Methods

Printed Circuit Boards, also known as PCB, can be categorized by different characteristics. Based on the number of

Gain	Phase Margin (°)	Gain Margin (dB)
1	11.69	6.26
2	20.58	9.24
3	31.87	11.74
4	38.56	13.68

TABLE XI
PHASE MARGIN FOR DIFFERENT GAINS IN OPEN LOOP WITHOUT LOAD.

Cooling Technology	Heat Flux (W/cm2)
Air Cooling	36
Indirect Water or Immersion Cooling	100
High Performance Conduction Cooling	125

TABLE XII
COOLING TECHNIQUES AND THEIR RESPECTIVE MAXIMUM HEAT FLUX REMOVAL.

copper layers, they can be classified as single, double or multi-layer [18]. Based on the substrate type, they can be classified as rigid, flexible or flex-rigid [18].

A more recent PCB technology, known as Insulated Metal Substrate (IMS), leverages the use of through hole components technology in pair with the surface-mount device technology. Figure 16 depicts PCB layers using IMS technology .

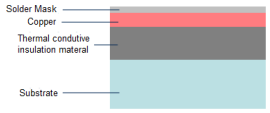

Fig. 16. Aluminium substrate PCB.

Because each THS6012 can dissipate up to 5.8W, energy dissipation as heat is a concern to be taken into consideration in this project.

Regard the experimental test comparing temperature over time of two PCB technologies. A glass fiber PCB (FR4), the most commonly used PCB manufacturing technology, and a metal substract board (IMS), more specifically, with aluminium substrate.

Implementing the same circuit with both technologies, that for this comparison purpose is a high power LED circuit, one can observe in Figure 17 that the IMS technology is able to set at a lower temperature than the FR4 technology.

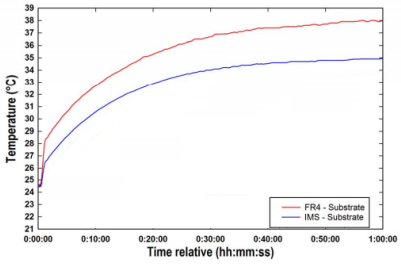

Fig. 17. Overtime temperature analysis for FR4 and IMS substrates.

Nevertheless, although the IMS technology enabling a better heat distribution over the whole substrate area, it is necessary to apply a thermal energy dissipation method to the PCB to further decrease the system's temperature.

There are three base methods for heat dissipation: conduction, convecection and radiation [20]. Convection cooling is the most used method, given its reduced cost and efficiency [21]. However, the development of systems of higher complexity renders this method inefficient, and thus demand alternative cooling methods [22]. In Table XII three possible techniques and their respective maximum heat flux removal are presented [23]:

The *High Performance Conduction Cooling* technique makes use of materials with high thermal conductivity, presenting the most satisfying results (125 W/cm2).

Thus, the IMS PCB technology allows for the best heat distribution, and the *High Performance Conduction Cooling* technique is the one presenting best heat dissipation results, making these the chosen technologies to implement a wide-band amplifier with correct operation.

B. PCB Project

1) Initial Considerations: The PCB's layout is the detailed presentation of the components placement in the board, where these are identified by their solder points (footprints), which are interconnected through copper tracks. The interconnections quality depends on the decisions taken throughout the layout process. For this reason, it is important to follow the recommendations made available by the components manufacturers, the rules difined by the PCBs manufacturer (in this case, Eurocircuits) and the norms documented in *Generic Standard on Printed Board Design* [24].

The minimum component interconnections width is determined by their respective current, using the expression 9. It is not recommended to have 90° interconnections, minimizing inductance effects, and tracks should be always spaced by 0.1mm minimum, limiting capacitive effects, and thus it is suggested to have ground tracks between different voltage tracks [24].

$$W[mils] = \frac{1}{H}\left(\frac{I}{k\Delta T^{0.44}}\right)^{1/0.725} \tag{9}$$

Considering the architecture's feedbacks, we recommend placing the feedback tracks with the shortest path possible, to avoid parasitic inductances [25]. Parasitic inductance caused by the track is given by expression 10. Copper thickness is given by H, thickness by W and track length by L. Note that parasitic inductance increases with L.

$$Ind[\mu H] = 0.0002L\left[ln\frac{2L}{(W+H)} + 0.2235\frac{W+H}{L} + 0.5\right] \tag{10}$$

Copper tracks also contribute as parasitic resistors, which can be determined using the expression 11. Copper resistivity is represented by ρ and positive temperature change rate is given by ΔT. Thus, one can limit parasitic resistors by increasing W.

$$Resistance[\Omega] = \rho\frac{L}{HW}(1 + 3.9 \times 10^{-3}\Delta T) \tag{11}$$

Before proceeding with the layout design, it is necessary to quantify the existing currents in the different branches and the components power dissipation value. Because the current depends from the selected gain and from the load value at the amplifier's output, this analysis considers the extreme case.

Imposing the maximum output current of 25A, with an input signal of 2V and 1MHz frequency, sweeping the different wideband amplifier gains, Figure 18 represents the maximum values on the circuit's branches.

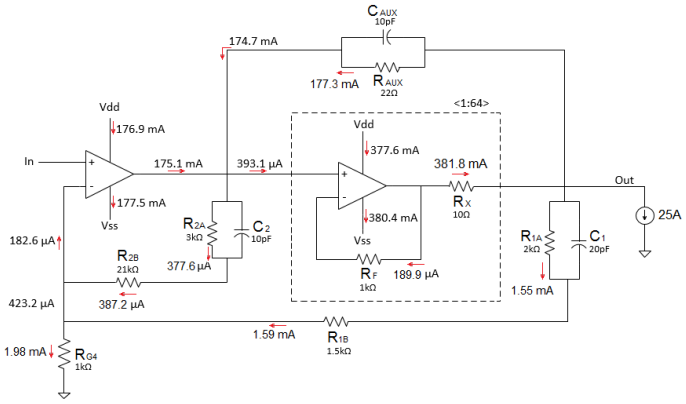

Fig. 18. Circuit configuration with maximum branch currents.

2) PCB Configuration: The PCB will rest in a conductive cooling system. Because the IMS technology only allows one copper layer, and the PCB is limited to the cooler dimensions, a choice was made to divide the amplifying circuit into three PCBs, as depicted in Figure 19, placing each PCB in the cooler's lateral surfaces.

As previously described, the integrated circuit THS6012 has two op-amps, and as such, the 64 parallel configuration in the electrical schematic map into 32 equal configurations on the PCB. Thus, these 32 blocks will be arrange by having two PCBs with 12 configurations and the third PCB with the remaining 8 configurations along with signal input and gain adjustment, as depicted in Figure 19(b).

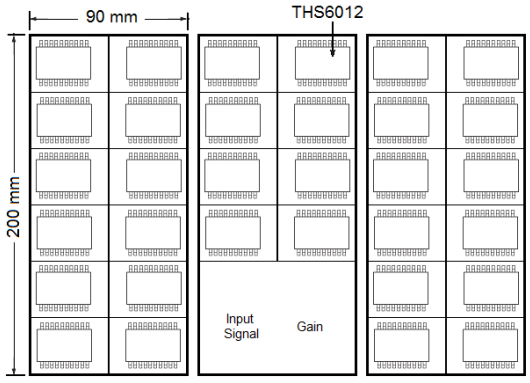

Fig. 19. Printed circuit boards configuration.

3) Component Selection: The reduced PCB dimensions and the IMS technology encourages the use of SMD technology components, by being physically smaller when compared to TH technology, which will result in a more compact layout. Besides the components depicted in Figure 18, 100nF capaciters are considered for decoupling op-amps from the power supply and a 50Ω resistor parallel to the wideband amplifier's input signal.

Tables XIII and XIV list resistors and capacitors, respectively, used in the wideband amplifer's layout. Table XIII lists the chosen resistors and their respective power heat dissipation (P_{Fab}), according to the technical documentation of each manufacturer. In choosing a resistor, a power heat value higher than the simulated was allowed.

Resistor	R (Ω)	P_{Fab} (W)
R_X	10	2
R_{AUX}	22	2
R_F	1 k	750m
R_{1B}	1.5 k	1.5
R_{1A}	2 k	63m
R_{2A}	3 k	63m
R_{2B}	21 k	63m
R_{G4}	1 k	63m
R_{G3}	1.5 k	63m
R_{G2}	3 k	63m
R_{G1}	100 k	63m
R_{50}	50	1

TABLE XIII
LIST OF RESISTORS USED FOR THE LAYOUT.

Table XIV lists the used capacitors. These allow a maximum voltage of 50V. The security margin is assured, given the wideband amplifier's operation voltage range from -15V to +15V.

Capacitor	C (F)	ΔV_{Fab}
C_{AUX}	10 pF	50
C_2	10 pF	50
C_1	20 pF	50
C	100nF	50

TABLE XIV
LIST OF CAPACITORS USED FOR THE LAYOUT.

4) PCB Components Placement: The wideband amplifier's layout was designed and optimized for high-speed signals, taken the considerations previously mentioned. For this process, the placing and disposition of components, copper tracks width, power supply voltage deviation and proper use of free areas, was carefully planned. For the layout a minimum spacing of 0.4mm between every interconnection was used, and a 1mm margin between the copper and the PCB border was applied.

Depicted in Figure 20 the wideband amplifier's main board layout is presented, where an input signal is applied and a gain adjustment is made. One can observe that the board contains 8 equal configurations, and consult it with more detail in Figure 21.

Figure 21 depicts the circuit for the two follower blocks equivalent, the 64 parallel, present in the amplifer's electric diagram.

The components $C1.1$, $C2.1$, $C3.1$ and $C4.1$ are 100nF capacitors connected to the power supply pins of the integrated circuit THS6012, the $U1.1$. Resistors $R3.1$ and $R4.1$ are the

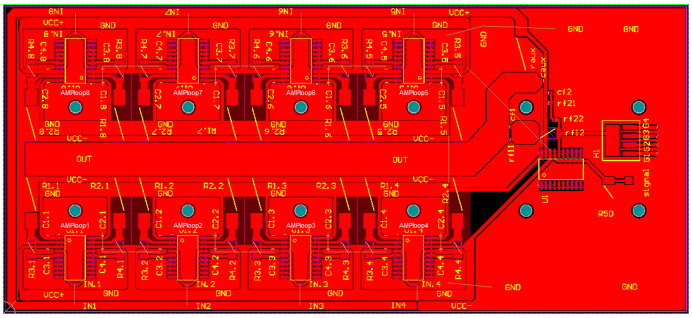

Fig. 20. Main PCB layout.

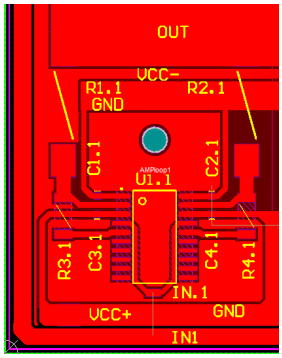

Fig. 21. Component interconnection.

feedback resistors of 1kΩ (R_F), and $R1.1$ and $R2.1$ are the compensation resistors of 10Ω (R_X). There are connected to the copper track OUT, that groups all the follower block outputs, as shown in Figure 20. Still, in the block depicted in Figure 21, one can observe that the integrated circuit THS6012 has a grounded *PowerPad*, to help heat dissipation, and that the free copper areas have GND pads, to provide a reference voltage.

As previously mentioned, the tracks width is determined by their current. Given that the branch with higher current is the op-amp output branch, with 381.8mA for the worst case, the minimum width to consider results in 0.0456mm. However, tracks with 0.8mm width were considered for component interconnections. The OUT track, being common to all the follower block's outputs, is traversed by the highest current, with a worst case of 6.11A. Using the expression that translates the track width as a function of current, results in a minumum width of 2.09mm. However, a widthness of 9.6mm was used for this track.

Horizontal tracks were also taken into consideration, for the top and bottom of the board, of $VCC+$ and $VCC-$, which will serve as the power supply tracks for the op-amps. Each of these tracks has to tolerate an aproximate current of 3A in the worst case, supplying the upper blocks 8 op-amps and the lower blocks 8 op-amps. Using the expression, the minimum width is 0.798mm, but 4mm track width were used for $VCC-$ and 3mm for $VCC+$.

The intput signal of the follower blocks, present in Figure, $IN.1$, uses external wiring to complete the interconnection. Given the IMS technology limitations, an external connection between pads $IN1$ and $IN.1$ are needed. However, given that the control voltage must come from the first amplifier stage, to ensure these provides the same voltage to the inputs of the follower blocks, this track needs to have low impedance.

The signal track IN, was of maximum width achieved of 2.4mm, given space limitations. Using expression 11, one can determine that a parisitic resistence created by the track between the first and the last follower blocks is of 0.0733 Ω. Taken into account the current traversing that branch, in the worst case it results in a voltage drop of 0.029mV, thus being this the voltage difference between the $IN5$ and $IN4$ pads.

Figure 22 depicts the first wideband amplifier stage.

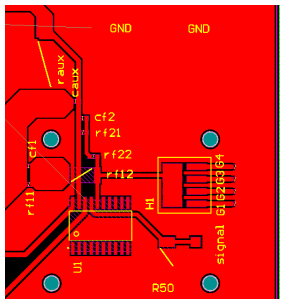

Fig. 22. Component interconnection.

The integrated circuit $U1$ is the op-amp representing this first stage, and the resistors $G1$, $G2$, $G3$ and $G4$ are the gain resistors, which enable the amplifier's gain adjustment. The remaining interconnections, depicted in Figure 22(b), correspond to the feedbacks between the two amplifier's stages.

However, as previously mentioned, the amplifier's layout was divided in three PCBs, two of them exactly the same. Figure 23 decpits this two boards layout, to be layed in the cooler's lateral surfaces. Each one is composed by 12 blocks, as the ones depicted in Figure 21, in accordance with the decisions taken for the previous layout process.

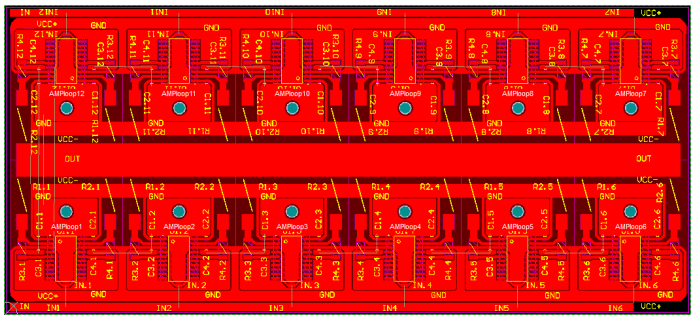

Fig. 23. Lateral PCBs layout.

Also, holes are added to the PCBs for fixing it to the cooling system. Note that Figure 24 contemplates a spacing between the hole and the copper track. This 0.4mm spacing prevents that the screw used for fixation creates a short-circuit, between the aluminium substrate and the copper track.

V. Conclusions and Future Work

A. Conclusions

Analyzing the accomplished work leads us to conclude that the initially established goals were met. The projected circuit

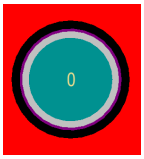

Fig. 24. Layout's footprint.

can supply capacitive and resistive loads in the disired value range, without leading to unstable operation. The variable gain amplifier can adapt to different load conditions without compromising performance and reliability.

The value range for output current and voltage are ensured, with a current constraint in high frequencies, a compromise to be taken into account when using the wideband amplifier.

The development of the layout using the IMS PCB technology was carried out with success, even though the space was limited and only one copper layer was available for placing tracks between components.

Comparing the technical specifications of the projected amplifiers with the available market amplifier models as presented in the beggining of the document, a significant advantage is highlighted relatively to the output bandwidth, which for this project is superior to 60MHz with unit gain.

Although Krohn-Hite Corporation amplifiers have higher slew-rate values, their maximum output current is of 884 mA. In contrast, Accel Instruments amplifier have higher output currents, around 6A, but much lower slew-rate values. The projected wideband amplifier can achieve output currents up to 25A and slew-rate values above 18V/μs.

B. Future Work

As future work it would be interesting to carry the following tasks:

- Manufacture and implement the projected PCBs;

- Test with the resistive and capacitive loads considered during dimensioning, with the intent of comparing simulation results with experimental results;

- Project a power supply board for the wideband amplifier

REFERENCES

[1] L. S. Pithadia Sanjay. (2009) Ldo psrr measurement simplified. [Online]. Available: http://www.ti.com/lit/an/slaa414/slaa414.pdf

[2] A. Instruments. Ts200 - modulated power. [Online]. Available: http://www.accelinstruments.com/Products/TS200/TS200-Description.html

[3] ——. Ts250 - waveform amplifier. [Online]. Available: http://www.accelinstruments.com/Products/TS250/Waveform-Amp.html

[4] ——. Ts400 - wideband power amplifier. [Online]. Available: http://www.accelinstruments.com/Products/Products.html

[5] K.-H. Corporation. Wideband power amplifiers. [Online]. Available: http://www.krohn-hite.com/htm/amps/Amplifiers.htm

[6] ——. Model 7500 - wideband power amplifier. [Online]. Available: http://www.krohn-hite.com/htm/amps/PDF/7500Data.pdf

[7] ——. Model 7600m/7602m - wideband power amplifier. [Online]. Available: http://www.krohn-hite.com/htm/amps/PDF/7600Data.pdf

[8] J. Buxton, *Careful Design Tames High Speed Op Amps*, an-257 ed. Analog Devices, 1991.

[9] "Texas Instruments Incorporated, 500-mA Dual Differental Line Driver," http://www.ti.com/lit/ds/symlink/ths6012.pdf, acedido: 13-04-2016.

[10] D. Brandenburg, *Current vs. Voltage Feedback Amplifiers*, oa-30 ed. National Semiconductor.

[11] X. Ramus, "Voltage feedback vs. current feedback amplifiers: Advantages and limitations," *IEEE presentation, Texas Instruments*, 2009.

[12] K. James. (1998) Voltage feedback vs current feedback op amps application report. [Online]. Available: http://www.ti.com.cn/cn/lit/an/slva051/slva051.pdf

[13] C. Bruce. (2000) Selecting high-speed operational amplifiers made easy. [Online]. Available: http://www.ti.com/lit/an/sloa051a/sloa051a.pdf

[14] G. King, *Op Amps Driving Capacitive Loads*, volume 31, number 2 ed. Analog Devices, 1997.

[15] G. Palumbo and S. Pennisi, "Design methodology and advances in nested-miller compensation," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 49, no. 7, pp. 893–903, Jul 2002.

[16] *Current Feedback Amplifier Theory and Applications*, An9420.1 ed. Intersil Corporation.

[17] M. Tian, V. Visvanathan, J. Hantgan, and K. Kundert, "Striving for small-signal stability," *IEEE Circuits and Devices Magazine*, vol. 17, no. 1, pp. 31–41, Jan 2001.

[18] A. Tarun. (2001) Different types of printed circuit boards. [Online]. Available: https://www.elprocus.com/different-types-printed-circuit-boards/

[19] J. Freisleben, T. Dzugan, and A. Hamacek, "Comparative study of printed circuit board substrates used for thermal management of high power leds," in *2015 38th International Spring Seminar on Electronics Technology (ISSE)*, May 2015, pp. 80–84.

[20] C. Mauney and J. Qian, "Thermal design considerations for surface mount power ics," in *APEC 07 - Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition*, Feb 2007, pp. 409–415.

[21] C. D. Jason, *An Examination of CPU Cooling Technologies*, thermal management options for engineers ed. DSI Ventures.

[22] M. B. d. S. Tiago H. Moita and A. L. N. Moreira, "Thermal design considerations for surface mount power ics," in *Advanced Intermittent Spray Cooling Systems*, Sep 2008.

[23] C. C. Richard. (2003) The perpetual challenges of electronics cooling technology for computer product applications. [Online]. Available: http://ww2.me.ntu.edu.tw/events/file/1113/Chu_University_Presentation_1.pdf

[24] *Generic Standard on Printed Board Design*, Ipc-2221a ed. Institute of Printed Circuits, 2003.

[25] J. Ardizzoni, *A Practical Guide to High-Speed PCB Layout*, analog dialogue 30-09 ed. Analog Devices, 2005.