DOCUMENT RESUME

ED 124 145 IR 003 533

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TITLE	The CGE-PLATO Electronic Laboratory Station Structure and Operation.
INSTITUTION	Illinois Univ., Urbana. Computer-Based Education Lab.
SPONS AGENCY	Advanced Research Projects Agency (DOD), Washington, D.C.
REPORT NO	MTC-R-4
PUB DATE	Jul 74
CONTRACT	DAHC-15-73-C-0077
NOTE	105p.
AVAILABLE FROM	PLATO Publications, Computer-based Education Research Lab, 252 Engineering Research Lab, University of Illinois, Urbana, Illinois 61801 ($0.50, prepayment required)
EDRS PRICE	MF-$0.83 HC-$6.01 Plus Postage.
DESCRIPTORS	Computer Assisted Instruction; *Computer Based Laboratories; Computer Programs; Computers; Computer Science; Educational Technology; *Electromechanical Technology; *Electronic Equipment; Engineering Technology; Engineers; Higher Education; Information Systems; Instructional Media; *Instrumentation; Instrumentation Technicians; Laboratory Equipment; Laboratory Training; Science Laboratories; Simulators
IDENTIFIERS	Computer Guided Experimentation; Computer Hardware; Electronic Laboratories; *PLATO IV; Programmed Logic for Automatic Teaching Operations

ABSTRACT

An electronic laboratory station was designed for student use in learning electronic instrumentation and measurement by means of the computer-guided experimentation (CGE) system. The station features rack-mounted electronic laboratory equipment on a laboratory table adjacent to a PLATO IV terminal. An integrated logic system behind the laboratory instrument panel interfaces the terminal and dial sensors within the laboratory equipment with the PLATO system. The logic interface provides PLATO with the ability to sense student-made interconnections between 30 terminals and the student-made settings of 22 dials on the laboratory equipment. PLATO guides and CGE hardware through the connection checks and stores the results for subsequent use in displays or in instructional programs. A complete record of the actual external interconnections between 30 terminals of experimentation equipment is generated in less than 5 seconds. A complete record of the settings of 22 dials of the experimentation equipment is generated in less than 4 seconds. (Author/CH)

Military Training Centers Project

MTC Report #4

THE CGE–PLATO ELECTRONIC LABORATORY STATION STRUCTURE AND OPERATION

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July, 1974

THE CGE-PLATO ELECTRONIC LABORATORY STATION STRUCTURE AND OPERATION

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ABSTRACT

This report describes the electronic laboratory station designed for student use in learning electronic instrumentation and measurements by means of the Computer-Guided Experimentation system. The station is located in Room 248 Electrical Engineering Building and features rack-mounted electronic laboratory equipment on a laboratory table adjacent to a PLATO IV terminal. An Integrated Logic System behind the laboratory instrument panel interfaces the terminal and dial sensors within the laboratory equipment with the PLATO system. The logic interface provides PLATO with the ability to sense student-made interconnections between thirty terminals and the student-made settings of twenty-two dials on the laboratory equipment. CGE-PLATO software subroutines enable instructors to program complete Connection Checks and/or Dial Checks whenever desired. For either case, PLATO guides the CGE hardware through the check and stores the result for subsequent use in displays or in instructional programs. A complete record of the actual external interconnections between thirty terminals of the experimentation equipment is generated in less than five seconds. A complete record of the settings of twenty-two dials of the experimentation equipment is generated in less than four seconds.

This work was supported in part by U.S. Army/DAHC 15-73-C-0077.

Distribution of this report is unlimited.

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CHAPTER I - INTRODUCTION

1.0 Characteristics of a CGE Station

This report describes the structure and operation of the laboratory station hardware and software designed for use in the CGE-PLATO IV Computer-Guided Experimentation (CGE) system of laboratory instruction.

There are four general requirements which may be used to characterize a CGE-PLATO station. First, the station must be capable of serving the needs of a broad class of relatively unsophisticated users, most of whom will be encountering a CAI terminal and electronic laboratory equipment for the first time. Second, the electronic instruments and the parts of the circuit boards must be commercially available general-purpose type equipment suitable for use in the variety of ways useful to introductory electronic laboratory instruction in electronic instrumentation and measurements. Third, modifications of the instruments and circuit boards which provide terminal and dial sensor connections to the interface logic system should be relatively inconspicuous and not change the external appearance or method of operation of the laboratory equipment. For new multiple installations, the internal instrument modifications should be made by their manufacturers prior to delivery. Four, the logic system interfacing the sensors of the CGE laboratory equipment with the PLATO system should be compact, accurate, reliable, and fast operating so the programmed connection and dial checking does not significantly distract from or impede the student's learning and experimentation.

1.1 The CGE Research Project

The object of this CGE research project is to demonstrate that the Computer-Guided Experimentation system will provide unique and worthwhile improvements in undergraduate or technician laboratory instruction, when properly used by competent instructors.

The CGE station consists of a PLATO IV console, Serial No. 324, Station No. 7-27, a CGE-PLATO Interface Logic System, five rack-mounted electronic instruments, and various experimentation circuit boards for student use in learning electronic instrumentation and measurements. The layout of the CGE station equipment is illustrated in Figure 1. A block diagram of the CGE-PLATO IV system is shown in Figure 2.

The CGE-PLATO Interface Logic System enables any instructor-author to program the automatic sensing of the interconnections between thirty terminals on the rack-mounted equipment or on the currently-used circuit board and/or the settings of twenty-two of the dials, knobs, or switches on the equipment. Records of the checks are stored by PLATO for subsequent use as however programmed.

The CGE station experimentation equipment is illustrated in Figure 3. The CGE rack-mounted instruments are:

1 Analab Dual-Trace Scope Type 1120 and Plug-In Type 700

1 Exact Function Generator Type 251

1 Hewlett-Packard Audio Oscillator Model 200AB

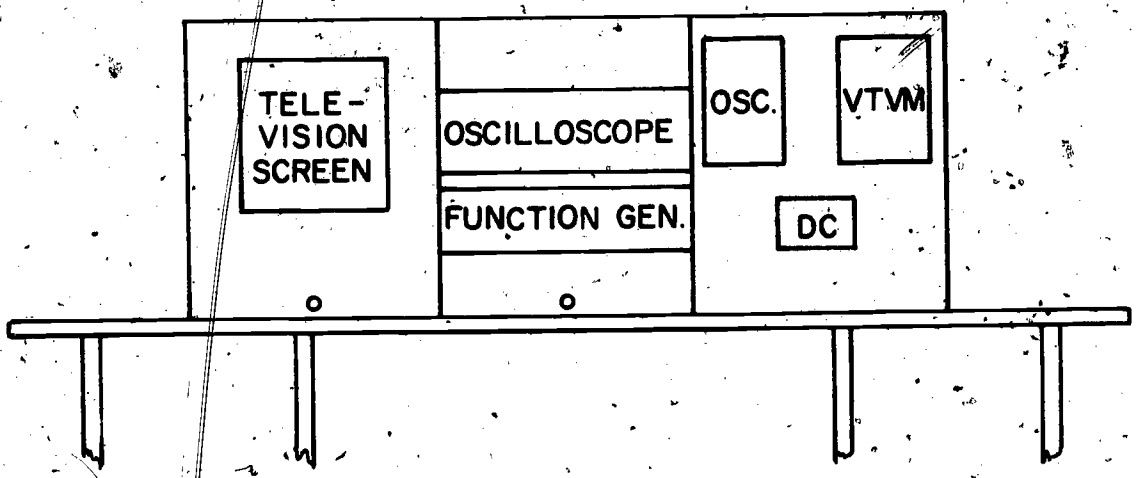
1 Hewlett-Packard Vacuum Tube Voltmeter Model 400D

1 Harrison Lab. Model 865B Power Supply.

The CGE-PLATO Interface Logic System is mounted behind the instrument rack panel, beneath the Function Generator.

The automatically sensed terminals are identified by T numbers, and the automatically sensed dials are identified by D numbers in Figure 4.

Actual laboratory experiments are programmed by knowledgeable laboratory instructors on the CAI system. The instructor writing a program provides for the automatic sensing of terminal interconnections and/or dial settings



FRONT VIEW

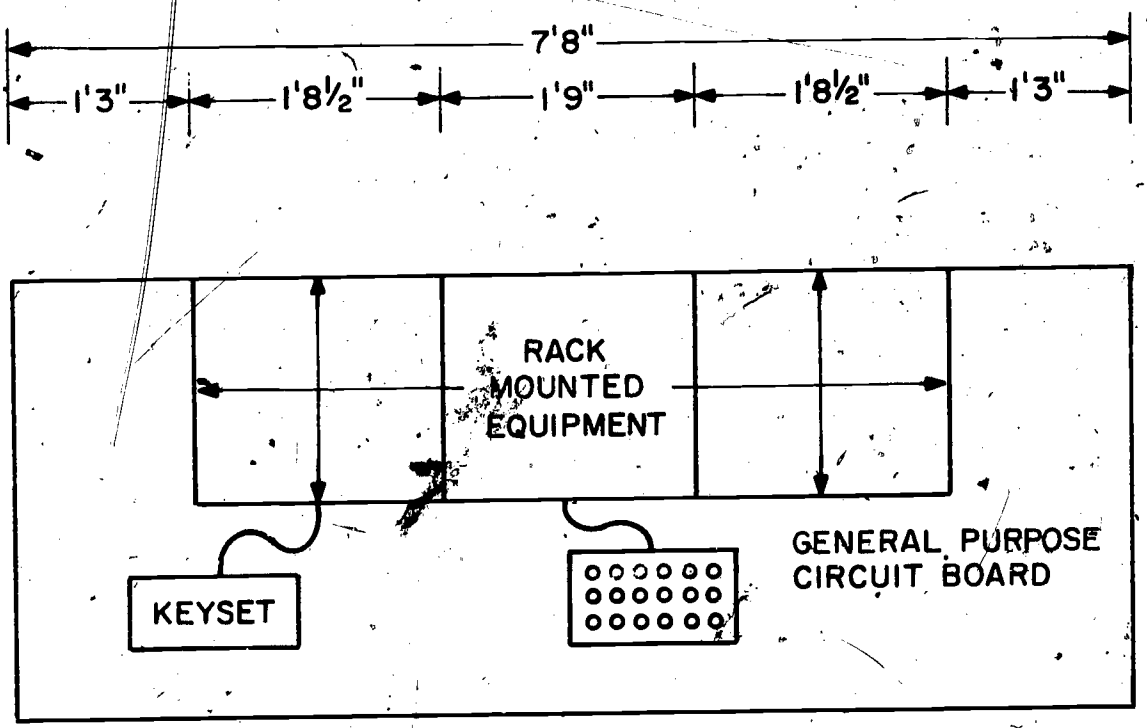


TABLE-TOP VIEW

Figure 1 The Computer-Guided Experimentation Station.

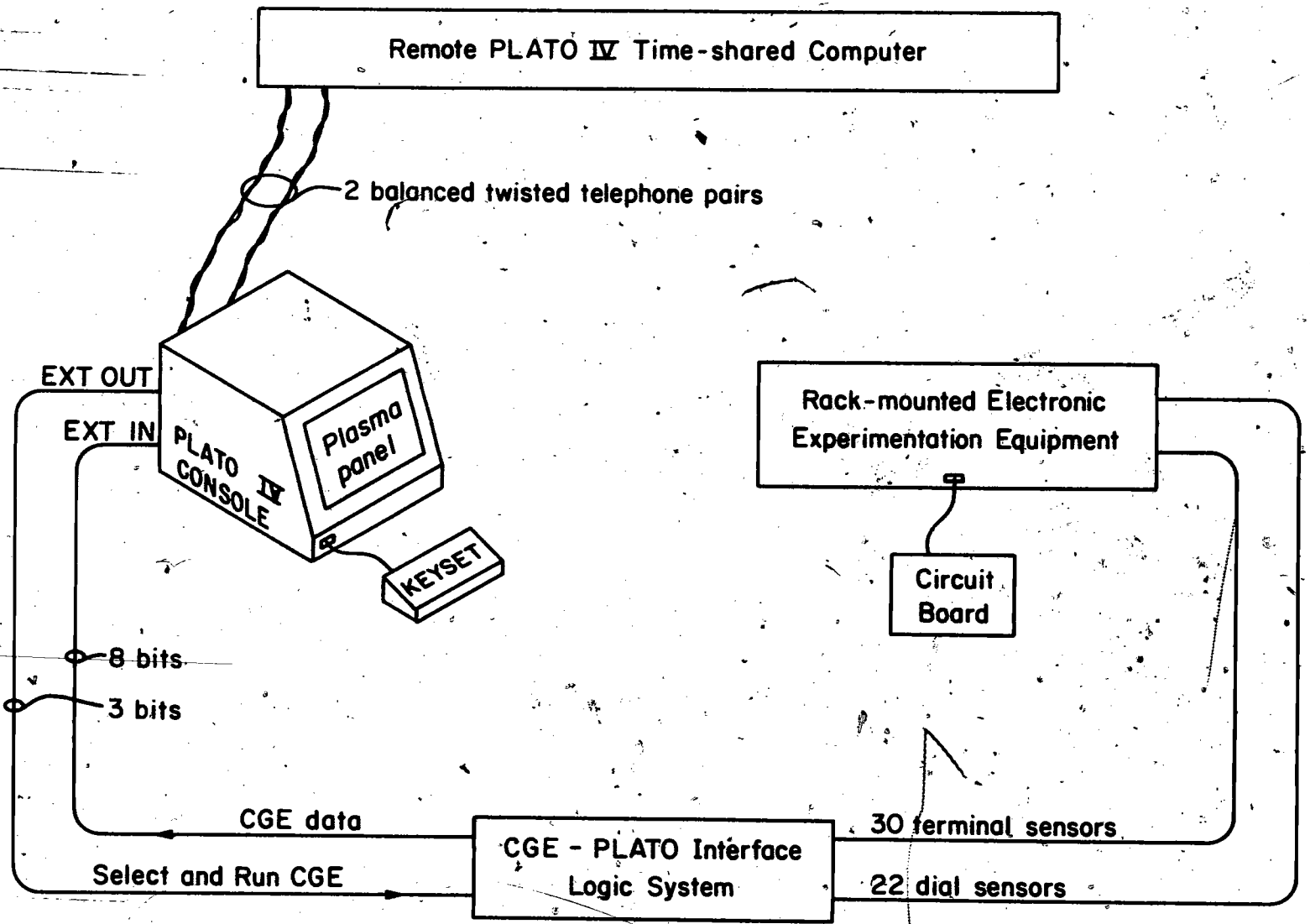


Figure 2 CGE-PLATO IV Block Diagram

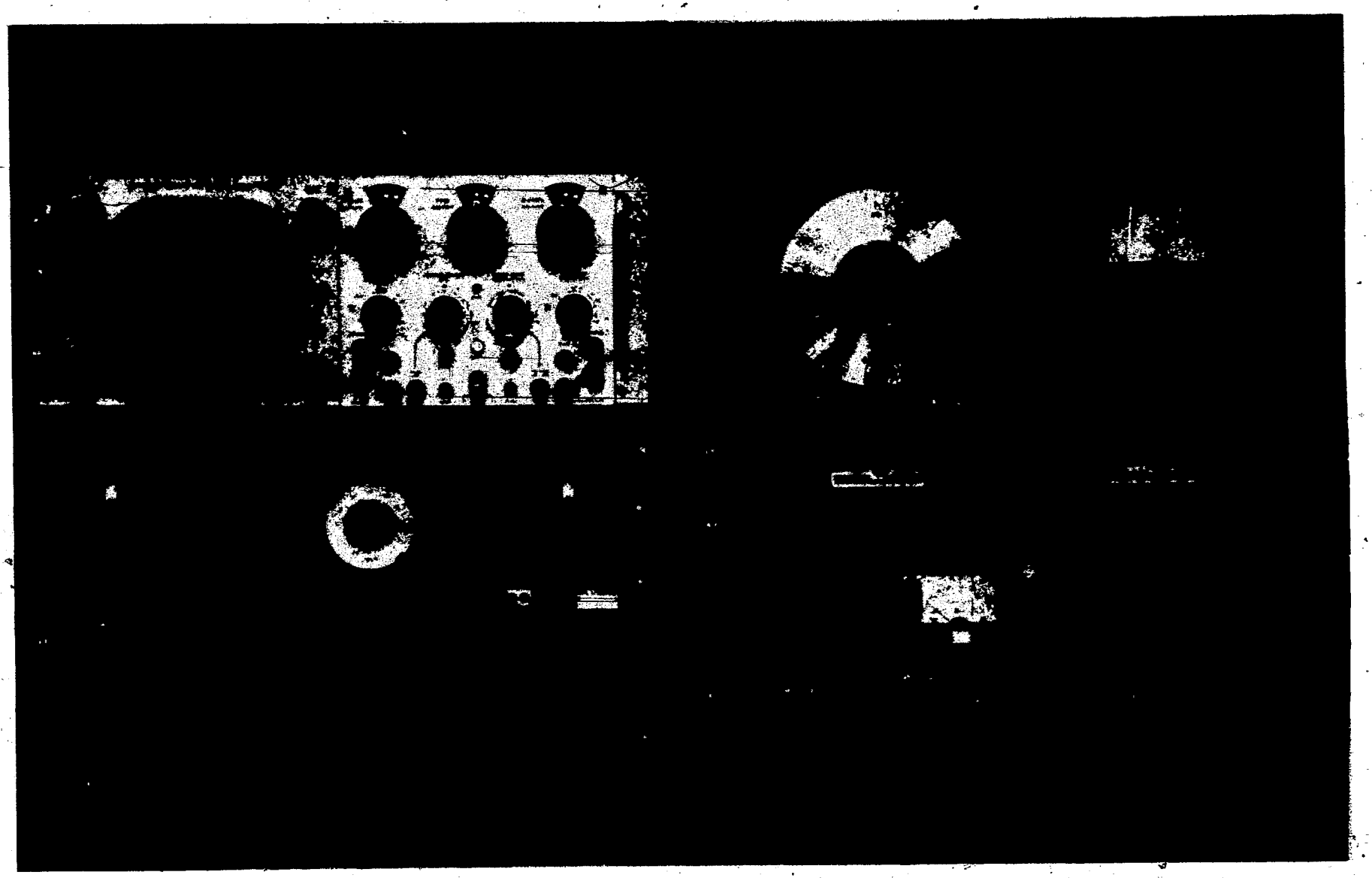
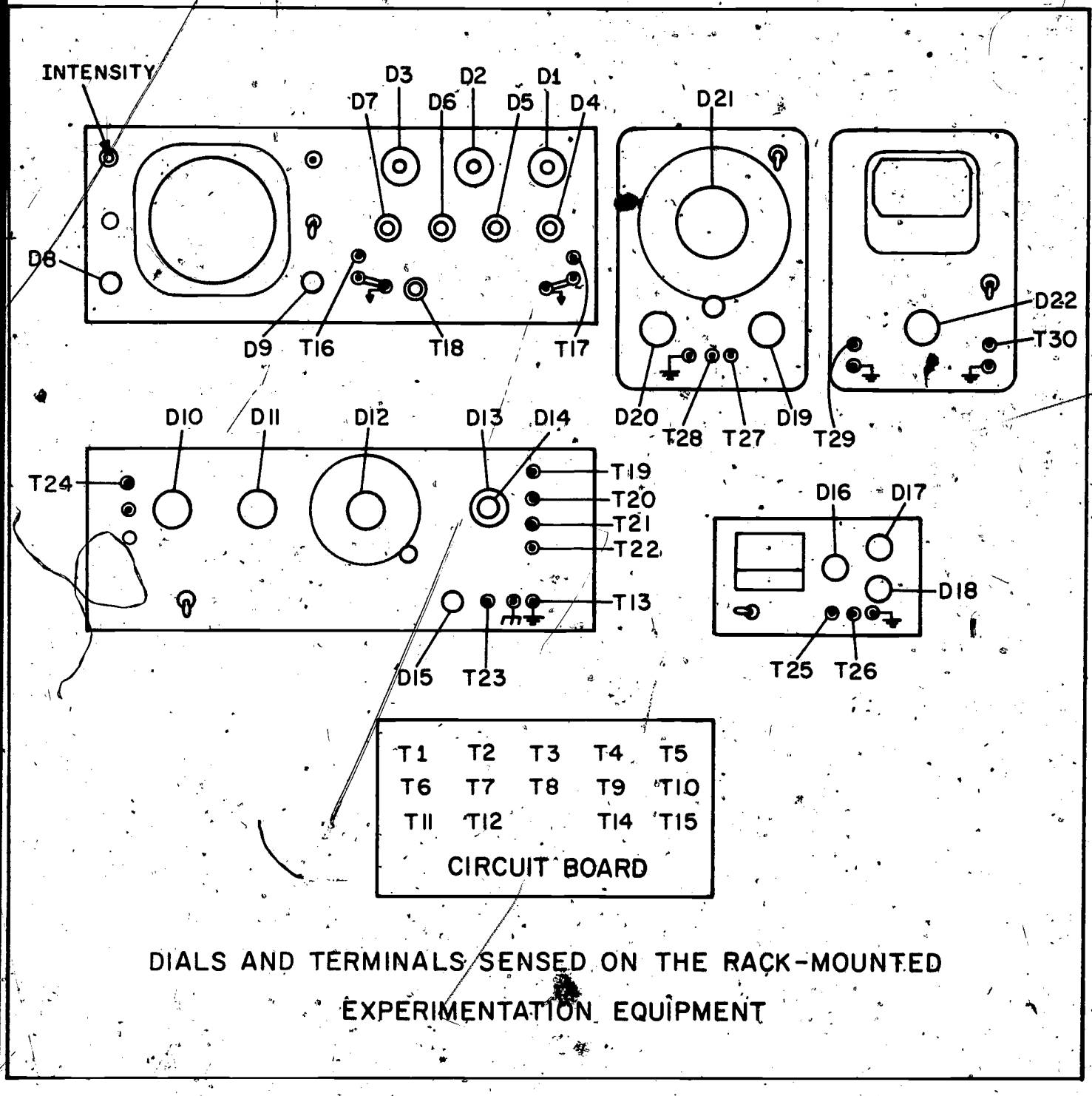


Figure 3 Introductory Electrical Engineering Laboratory Station



DIALS AND TERMINALS SENSED ON THE RACK-MOUNTED EXPERIMENTATION EQUIPMENT

Figure 4. Dials and Terminals Sensed on the Rack-Mounted Experimentation Equipment

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wherever he deems necessary. The response of the program to the fed back information of the student's physical operations can be used in any manner the instructor devises for improving the student's learning.

Each student can work independently at a CGE station and learn at his own rate how to use the equipment, and perform or devise meaningful experiments.

CGE is an entirely new instructional system, and research is required to develop its teaching capabilities and demonstrate its superiority in comparison with conventional laboratory instruction or training simulators. CGE is not simply a new teaching aid, it is a new teaching method with unexplored and unknown capabilities.

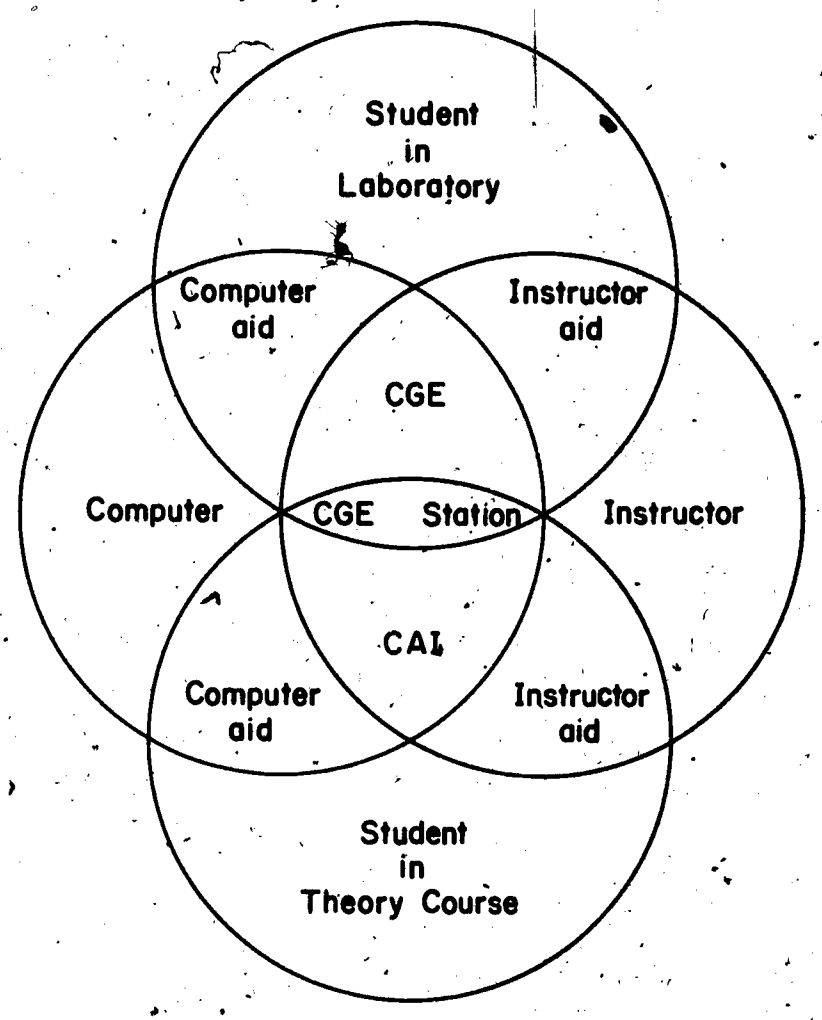
A student at a CGE station in a laboratory is provided ready access to laboratory facilities, theoretical material, computer assistance, and instructor assistance as visualized in Figure 5.

1.2 History of CGE

The concept of Computer-Guided Experimentation originated in 1968 from discussions of the capabilities of automatically monitoring the terminal interconnections and dial settings made by a student while performing an electrical laboratory experiment. These discussions were initiated by J. P. Neal with D. L. Bitzer and R. L. Johnson on 21 June 1968.

Beginning in October 1968, Larry Weber worked with R. L. Johnson to develop and demonstrate in January 1969 a system for automatically measuring and graphically displaying on a PLATO screen the interconnections between four terminals.

Also beginning in October 1968, Tony Maher and Rod Parks worked with Neal in developing means for automatically sensing the settings of dials and the terminal interconnections of the rack-mounted electrical experimentation equipment. A study of the possible positions of all the dials on the



CORRELATIONS
STUDENT - INSTRUCTOR - COMPUTER

Figure 5

AA-008-1

laboratory equipment revealed that twenty-four angular positions evenly spaced at 15° included all possible detented dial positions. Furthermore, sensing the position of any continuously variable dial shaft to within 15° would also be adequate. Therefore, a circular wafer was designed for dial position sensing so that it would provide a unique five-digit binary number for indicating each of the twenty-four different dial settings. Transmission of this five-digit binary number electrically would require five parallel sensing lines from every dial.

In a discussion on 13 December 1968, D. L. Bitzer suggested an alternate scheme, namely, the use of a shaft potentiometer which would deliver a voltage proportional to the dial shaft position via a single sensing line. Then, at a single point in the logic hardware, convert these analog voltages to five-bit binary numbers for transmission to PLATO. This scheme greatly simplified the internal wiring modifications necessary within the laboratory instruments.

During the spring of 1969, Bob Bradley joined Neal on this project and, with the assistance of the Electrical Engineering Electronics Shop, installed potentiometer units or wafers on the shafts of the twenty-two rack-mounted instrument dials whose positions should be monitored. Relays for disconnecting fifteen of the external instrument terminals from the interior instrument circuits were also installed so that the remote-sensing of interconnections would see only those connections made externally by a student during an experiment.

In June 1970, after the experimentation equipment modifications were completed, the Computer-Guided Experimentation Research Laboratory (CGERL) Station was moved to Room 261, Engineering Research Laboratory, adjacent to PLATO III, and

interfacing it with PLATO III began. In the meantime, David L. Meller and other students working with Neal developed and programmed software for the CGE system and explored ways of programming worthwhile electrical engineering laboratory experiments.

Thereafter, Robert Arthur and other students working with Neal continued to develop and construct the CGE-PLATO III Interface Logic System. This logic system was designed to respond to commands programmed in the CGE lessons and automatically measure and report to PLATO III the external interconnections between thirty terminals on the laboratory equipment, and/or automatically sense and report to PLATO III the settings of twenty-two dials on the rack-mounted laboratory instruments at the CGE station.

On 3 August 1971, the CGE-PLATO III Interface Logic System became fully operational. The sensing and report to PLATO III of the thirty terminal interconnections was reliably accomplished in three seconds, and the sensing and reporting of the twenty-two dial settings was reliably accomplished in less than one second.

The CGE-PLATO III interface hardware had grown to occupy four rows of an eighteen-inch relay rack and consisted of about sixty 4" x 6 1/2" integrated circuit boards, including eight dc power supply boards. No funds were available for the CGE project, but space and materials were furnished by the Computer-Based Educational Research Laboratory in the Engineering Research Laboratory. Student participation in the CGE project continued because of their interest and they were able to earn limited academic credit for special problems.

CGERL efforts continued towards the following goals:

1. Modifications of the logic hardware to interface with PLATO IV, soon to become operational.

2. Reduction in the size and complexity of the CGE interface hardware.

3. Improvement of the use of the CGE system in guiding students to learn laboratory work.

Modifications of the CGE-PLATO interface were made so that it could be operated with either PLATO III or PLATO IV. The interface with PLATO IV, Serial No. 118, became operational in Room 261, Engineering Research Lab, on 25 September 1972.

PLATO III was being phased-out. Therefore, on 23 October 1972, the interface was permanently modified to operate only with PLATO IV, and the IC boards necessary for PLATO III were removed.

On 24 October 1972, CGERL and the CGE-PLATO IV station was moved from Room 261 ERL to Room 248 Electrical Engineering Building, where they are now located. Communication with the central PLATO IV system was now established over a pair of telephone lines. Furthermore, the telephone lines terminated at PLATO in a site controller which communicated with the central computer over a high-speed link. The site controllers are programmed to receive signals from stations at a rate not exceeding five keys/second. This materially slowed CGE operation. Where we had previously completed a connection check requiring the equivalent of 150 keys in three seconds, a connection check now required thirty seconds. This was an untenable situation and it justified a complete review of the method of operation.

Another advantageous situation developed. In the spring of 1973, solid-state switches became commercially available. Use of these integrated circuit chips (Inselek L02) enabled Richard L. Brown, working on a Master's thesis with Neal, to replace the magnetic reed relays and multiplexing IC chips used in the dial checker and improve its simplicity and speed of operation.

A more sophisticated IC chip (Inselek L05) became available during the summer of 1973. These IC chips provided a reliably uniform low resistance in the "on" position so that it became feasible to replace the sixty magnetic reed relays and associated multiplexing chips used in the connection checker.

Consequently, with the start of the funding of the CGE project in the middle of 1973, efforts were concentrated on a complete redesign and reconstruction of the entire CGE-PLATO IV Interface hardware and software.

Douglas Dowden, Gunther Frank, Paul Thyfault and Douglas Zanter, working with Neal, accomplished this redesign and reconstruction. During this reconstruction, terminal-deactivating relays were also installed for the fifteen circuit board terminals. One breakthrough was the incorporation of a procedure for checking one terminal or dial at a time, rather than automatically reporting an entire series of checks of all dials or all terminals as a block operation. This method placed the burden on PLATO software for memory and processing, and reduced the complexity of the hardware.

Douglas C. Dowden worked out the entirely new software routines required and Gunther Frank led the hardware redesign. With this new system, only 30 equivalent keys need be sent to PLATO for a complete connection check, instead of the 150 equivalent keys previously required. Consequently, the time for a complete connection check by PLATO IV was reduced from about thirty seconds to less than five seconds. Furthermore, the more sophisticated hardware system occupied space equivalent to only four IC boards, instead of the sixty IC boards formerly used with the original system.

The reduction in volume of the CGE hardware interface permitted it to be concealed and ventilated in the rack supporting the experimentation instruments and the separate relay rack was discarded.

This entirely new CGE system interfaced with a new type PLATO IV console, Serial No. 324, became fully operational on 3 December 1973 as Station 7-27. This practically completed the hardware and software subroutines for the CGE-PLATO IV Interface Logic System. Minor improvements or repairs continue to be made as needed.

Now, the major effort of the CGERL group is directed towards testing, evaluating, and improving the instructional value of the CGE experimentation lessons.

CHAPTER 2 - CGE HARDWARE

2.0 List of CGE-PLATO Hardware Items

The electronic laboratory equipment at the CGE-PLATO station is on loan from the Electrical Engineering Department of the University of Illinois at Urbana. The major items of equipment at the CGE-PLATO station, including the CGE-PLATO interface, are:

Item No. *	Item Name
	CGE Logic System:
1	Front Interface Logic Board
2	Rear Interface Logic Board
3	Relay Driver Board
4	Connection-Check 36PDT Relay
5	DC Logic Power Supplies
	Rack-Mounted Instruments:
11	Scope (Analab Dual-Trace Scope Type 1120)
12	Plug-In (Analab Plug-In Type 700)
13	Function Generator (Exact Type 251)
14	Audio Oscillator (HP Model 200AB)
15	Vacuum Tube Voltmeter (HP Model 400D)
16	DC Supply (Harrison Lab Model 865B)
17	Circuit Board Panel-Socket
	PLATO Terminal Connectors:
25	EXT OUT Connector (PLATO console #324)
26	EXT IN Connector (PLATO console #324)
	Experimentation Circuit Boards:
31	General Purpose Board
32	Resistor Board
33	RC Board
34	RL Board
35	Impedance Board
36	Two Port Network
37	Thevenin Board
38	Superposition Board

2.1 Modifications of Laboratory Instruments and Circuit Boards for the Sensing of Terminal Interconnections

Internal to each rack-mounted electronic laboratory instrument and underneath each circuit board, a sensing lead is extended from every terminal to be sensed. Each terminal sensor lead terminates on a pole of a

* Numbers 6-10, 18-24, and 27-30 are unassigned.

62R4 terminal-deactivating relay. There is one normally open contact and one normally closed contact associated with each relay pole. The terminal-deactivating relays for each instrument are installed within that instrument. The terminal-deactivating relays for the circuit boards are on Item 3, the Relay Driver Board.

For the sensors of instrument terminals, the interior wiring to a sensed terminal is connected to the normally closed contact of a terminal-deactivating relay, and the terminal is connected to the associated relay pole. Hence, when no Connection Check is in progress, the interior circuit connection to the instrument terminal is closed and the instrument operates normally.

The circuit board terminals are also connected to poles of terminal-deactivating relays. However, the normally closed contacts of these terminal-deactivating relays are left unconnected. Therefore, when no Connection Check is in progress, the circuit boards of the experimentation system operate normally.

When an order from PLATO causes the CGE interface to initiate a Connection Check, all terminal-deactivating relays operate. First, each circuit terminal connected to a relay pole is disconnected from the normally closed terminal-deactivating relay contact, and then connected to the normally open terminal-deactivating relay contact. Each of the normally open contact of the terminal-deactivating relay poles are wired to poles of the CC 36PDT relay, which at this moment is unoperated. Each of the normally closed contacts of the CC relay are conne ted to ground through individual forty-seven ohm resistors. Hence, the operation of the terminal-deactivation relays disconnects all instrument sources and circuits from the experimentation circuit, then grounds all terminals of the experimentation circuit for the purpose of dissipating all circuit-stored energy. In other words, the student's experimentation circuit is deenergized.

The twenty-four volt supply to the CC relay coil loops serially through a pole and normally open contact on every terminal-deactivating relay. After all terminal-deactivating relays have operated, the path supplying twenty-four volts to the CC relay coil is closed and that relay operates. This disconnects all terminal sensors from ground through the normally closed contacts of the CC relay and then connects all terminal sensors through the normally open contacts of that relay to the inputs of the L05's. This situation remains until an EXT Ø or DC signal is received from PLATO, or, if CC is not reactivated by PLATO within 5.5 seconds, the CGE system will clear automatically — first releasing the CC relay, then releasing all the terminal-deactivating relays and returning the experimentation circuit to normal.

2.2 Modifications of Laboratory Instruments for the Sensing of Dial Settings

Inside each instrument, for each instrument dial whose angular position is remotely sensed by the CGE Logic System, a wafer potentiometer or twenty-four-position rotary switch has been installed and keyed to the dial shaft. This wafer provides an analog voltage proportional to the dial position. Linear potentiometers are used for sensing the positions of continuously variable dials. Single-pole rotary switches with discrete positions uniformly space at 15° angularly are used for sensing the positions of discrete-position dials, because every discrete-position dial on the rack-mounted experimentation instruments has twenty-four discrete positions or some submultiple of twenty-four discrete positions, namely, twelve, six, or three.

The rotary dial-position-sensing switches are made into potentiometers by connecting equal-resistance resistors between adjacent contacts.

All dial-position sensing potentiometers (continuously or discretely varying) have their initial end connected to the chassis ground and the

final or high end connected to + 5 volts dc through a trim resistor. The trim resistors and the intercontact resistors are designed to cause the n^{th} position of every dial to produce the same analog sensor voltage. The total resistance of each continuously variable potentiometer is about 23,000 ohms. For sensing twenty-four discrete positions evenly spaced angularly, one 1,000 ohm resistor is connected between each pair of adjacent terminals of each twenty-four position rotary switch.

The Analog-to-Digital Conversions of the Dial Sensor Voltages are listed in Figure 6. The Dial Setting Codes sensed and stored by PLATO for the various settings of the twenty-two sensed dials are tabulated in Figure 7.

Figure 6. Analog-to-Digital Conversions of Dial Sensor Voltages.

Dial Setting	Input to Pin 3, SN72741, Sheet 7*	Input to Pin 23, A/D Conv., Sheet 7*	Output of A/D Converter and Report to PLATO	
	Volts	Volts	Binary Number	Letter Code
1	Ø	.469	ØØØØ1	a
2	.238	.781	ØØØ1Ø	b
3	.476	1.Ø93	ØØØ11	c
4	.714	1.4Ø6	ØØ1ØØ	d
5	.952	1.719	ØØ1Ø1	e
6	1.191	2.Ø31	ØØ11Ø	f
7	1.429	2.348	ØØ111	g
8	1.667	2.656	Ø1ØØØ	h
9	1.9Ø5	2.969	Ø1ØØ1	i
1Ø	2.143	3.281	Ø1Ø1Ø	j
11	2.381	3.594	Ø1Ø11	k
12	2.619	3.9Ø6	Ø11ØØ	l
13	2.857	4.219	Ø11Ø1	m
14	3.Ø95	4.513	Ø1110	n
15	3.333	4.844	Ø1111	o
16	3.571	5.156	1ØØØØ	p
17	3.8Ø9	5.469	1ØØØ1	q
18	4.Ø47	5.781	1ØØ1Ø	r
19	4.286	6.Ø94	1ØØ11	s
20	4.524	6.4Ø6	1Ø1ØØ	t
21	4.762	6.719	1Ø1Ø1	u
22	5.ØØØ	7.Ø31	1Ø11Ø	v

* See page 27.

Figure 7. Dial Setting Codes.

Letter	Setting		
PLUG-IN			
D1: B VOLTS			
D3: A VOLTS			
a	1	mV	FCW*
b	2	"	
c	5	"	
d	10	"	
e	20	"	
f	50	"	
g	100	"	
h	200	"	
i	500	"	
j	1	V	
k	2	"	
l	5	"	
m	10	"	
n	20	"	
o	50	"	
p	100	"	
q	200	"	FCCW*
D2: TIME			
a	10	μs	FCW
b	20	"	
c	50	"	
d	100	"	
e	200	"	
f	500	"	
g	1	ms	
h	2	"	
i	5	"	
j	10	"	
k	20	"	
l	50	"	
m	100	"	
n	200	"	
o	500	"	
p	1	s	
q	2	"	
r	5	"	
s	10	"	
t	20	"	
u	50	"	
v	EXT C		FCCW

Letter	Setting	
D4: B PREAMP		
D7: A PREAMP		
a	-AC	FCW
b	+AC	
c	+DC	
d	-DC	
e	OFF	
f	BALSET	FCCW
D5: SWEEP MODE		
VAR. LENGTH:		
a	ARM	FCW
b	MAN	
c	AUTO	
d	DRIV	
VAR. RATE:		
e	DRIV	
f	OFF	FCCW
D6: TRIGGER SOURCE		
a	LINE	FCW
b	AC EXT/20	
c	DC EXT/20	
d	AC EXT	
e	DC EXT	
f	AC INT	
g	DC INT	
h	OFF	FCCW
SCOPE		
D8: Y DISPLAY		
a	A	FCCW
b	B	
c	A&B CHOP	
d	A&B ALT	
e	A vs. B	FCW
D9: X DISPLAY		
a	SWP x 5	FCW
b	SWP	
c	EXT	FCCW

Letter	Setting	
FUN. GEN.		
D10: TRIGGER		
a	INT	FCW
v	EXT	FCCW
D11: MULTIPLIER		
a	.001	FCCW
b	.01	
c	.1	
d	1.	
e	10.	
f	100.	
g	1000.	FCW
D12: CYCLES/SEC. (MULTIPLIER = 10)		
a	9 ± 3	FCCW
b	15 ± 3	
c	19 ± 2	
d	23 ± 3	
e	28 ± 2	
f	32 ± 2	
g	36 ± 2	
h	41 ± 3	
i	46 ± 3	
j	50 ± 2	
k	55 ± 3	
l	60 ± 3	
m	64 ± 2	
n	69 ± 3	
o	73 ± 2	
p	76 ± 3	
q	82 ± 2	
r	87 ± 3	
s	92 ± 3	
t	96 ± 2	
u	100 ± 2	
v	102 ± 2	FCW
D13: OUTPUT		
d	SQUARE	FCCW
c	TRIANGLE	
b	SINE	
a	RAMP	
b	SINE	FCW

Letter	Setting	
D14: ATTENUATOR (OC & DC FCCW) SQ. @ 1000 Hz		
a	6 ± 1 V_{pp}	FCCW
b	9 ± 2	
c	12 ± 2	
d	14 ± 1	
e	17 ± 2	
f	19 ± 2	
g	20 ± 1	
h	21 ± 1	
i	22 ± 1	
j	23 ± 1	
k	24 ± 1	
l	25 ± 1	
m	25 ± 1	
n	26 ± 1	
o	27 ± 1	
p	28 ± 1	
q	28 ± 1	
r	29 ± 1	
s	29 ± 1	
t	30 ± 1	
u	30 ± 1	
v	31 ± 1	FCW
D15: DC LEVEL (OC & D14 FCCW)		
a,b,c,d	OFF	FCCW
d	-57 ± 1 V	
e	-56 ± 1	
f	-53 ± 3	
g	-48 ± 3	
h	-44 ± 3	
i	-39 ± 3	
j	-35 ± 2	
k	-31 ± 3	
l	-27 ± 1	
m	-24 ± 2	
n	-20 ± 3	
o	-17 ± 2	
p	-14 ± 2	
q	-13 ± 1	
r	-13 ± 1	
s	-10 ± 3	
t	2 ± 11	
u	30 ± 17	
v	56 ± 11	FCW

* Fully Clock-wise
** Fully Counter-clock-wise

Figure 7. Dial Setting Codes (cont.)

Letter	Setting	
DC SUPPLY		
D16: METER		
a	VOLTS	FCCW
v	AMPS	FCW
D17: VOLTAGE (OC & D18 OFF)		
	V	
a	-.7 ± .1	FCCW
.	- - -	
.		
.		
v	-.7 ± .1	FCW
D17: VOLTAGE (OC & D18 .1A)		
	V	
a	.7 ± .7	FCCW
b	2.9 ± 1.5	
c	5.8 ± 1.4	
d	8.6 ± 1.5	
e	11.3 ± 1.3	
f	14.0 ± 1.5	
g	16.3 ± 1.3	
h	18.8 ± 1.3	
i	21.0 ± 1.0	
j	23.0 ± 1.0	
k	25.5 ± 1.5	
l	28.0 ± 1.0	
m	30.0 ± 1.0	
n	32.3 ± 1.3	
o	34.5 ± 1.0	
p	36.5 ± 1.0	
q	38.8 ± 1.3	
r	41.3 ± 1.3	
s	43.3 ± 1.3	
t	45.3 ± 1.3	
u	48.0 ± 1.5	
v	50.0 ± 1.0	FCW
D18: CURRENT (SC & D17 FCCW)		
	A	
a	-.02 ± .01	FCCW
b	-.01 ± .01	
c	.01 ± .01	
d	.03 ± .01	
.	- - -	
.		
.		
v	.03 ± .01	FCW

Letter	Setting	
D18: CURRENT (SC & D17 FCW)		
	A	
a	-.02 ± .01	FCCW
b	-.01 ± .01	
c	.02 ± .02	
d	.04 ± .02	
e	.07 ± .02	
f	.10 ± .02	
g	.12 ± .02	
h	.15 ± .02	
i	.19 ± .02	
j	.22 ± .02	
k	.25 ± .02	
l	.27 ± .02	
m	.29 ± .02	
n	.32 ± .02	
o	.35 ± .02	
p	.38 ± .02	
q	.41 ± .02	
r	.44 ± .02	
s	.46 ± .02	
t	.49 ± .02	
u	.51 ± .02	
v	.53 ± .02	FCW
AUD. OSC.		
D19: AMPLITUDE (OC & 1000 Hz)		
	Vrms	
a	1 ± 1	FCCW
b	2 ± 1	
c	4 ± 1	
d	5 ± 1	
e	7 ± 1	
f	8 ± 1	
g	10 ± 1	
h	12 ± 1	
i	13 ± 1	
j	14 ± 1	
k	16 ± 1	
l	17 ± 1	
m	19 ± 1	
n	20 ± 1	
o	21 ± 1	
p	23 ± 1	
q	24 ± 1	
r	26 ± 1	
s	27 ± 1	
t	29 ± 1	
u	30 ± 1	
v	31 ± 1	FCW

Letter	Setting	
D20: RANGE		
a	1	FCCW
b	10	
c	100	
d	200	FCW
D21: FREQUENCY (OC & RANGE x 1)		
	Hz	
a		FCW
b	19 ± 1	
c	21 ± 1	
d	22 ± 1	
e	24 ± 1	
f	25 ± 2	
g	28 ± 2	
h	31 ± 2	
i	35 ± 2	
j	40 ± 3	
k	46 ± 3	
l	53 ± 4	
m	61 ± 5	
n	71 ± 6	
o	82 ± 6	
p	94 ± 6	
q	108 ± 8	
r	122 ± 8	
s	140 ± 10	
t	160 ± 10	
u	185 ± 15	
v	210 ± 10	FCCW
VTVM		
D22: RANGE		
	Vrms-sine	
a	.001	FCCW
b	.003	
c	.01	
d	.03	
e	.1	
f	.3	
g	1	
h	3	
i	10	
j	30	
k	100	
l	300	FCW

An alternate method is used for sensing the positions of switches on circuit boards. In those cases the switches simply change circuit connections, and terminals of each switch are sensed like other circuit terminals, and the terminal interconnections sensed by the Connection Check* reveal the switch positions to PLATO.

2.3 Schematic Diagrams of the CGE-PLATO Interface Hardware

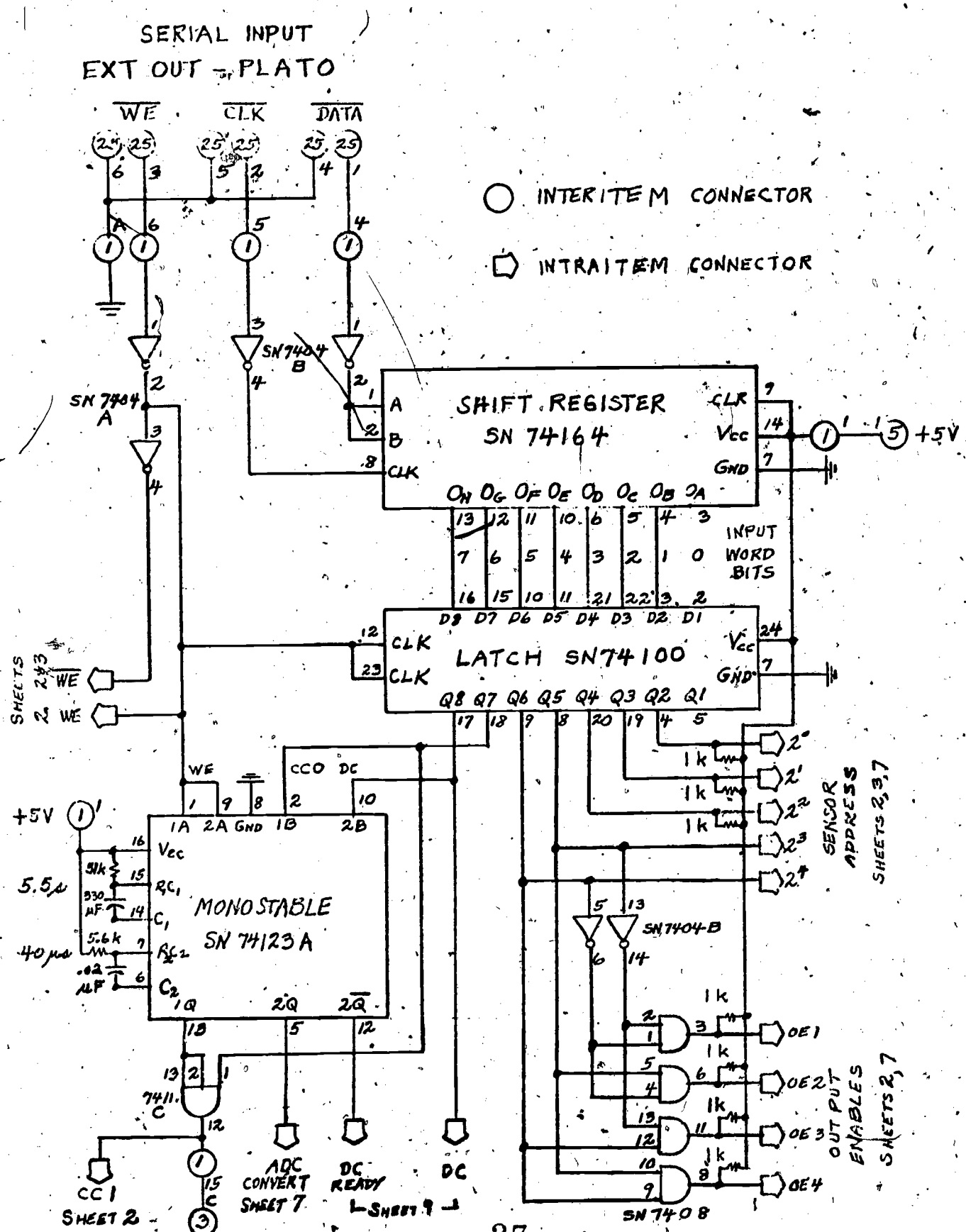
The next ten sheets of schematic diagrams cover the CGE-PLATO interface hardware and are separately indexed as follows:

Topic	Sheet No.
CGE Input from PLATO	1
The Connection Checker	2
The Connected-Terminal Selector	3
The CC Relay	4
Terminal Sensors I	5
Terminal Sensors II	6
The Dial Checker	7
Dial Setting Sensors	8
CGE Output to PLATO	9
Power Supplies	10

* For details see Chapters 3 and 4.

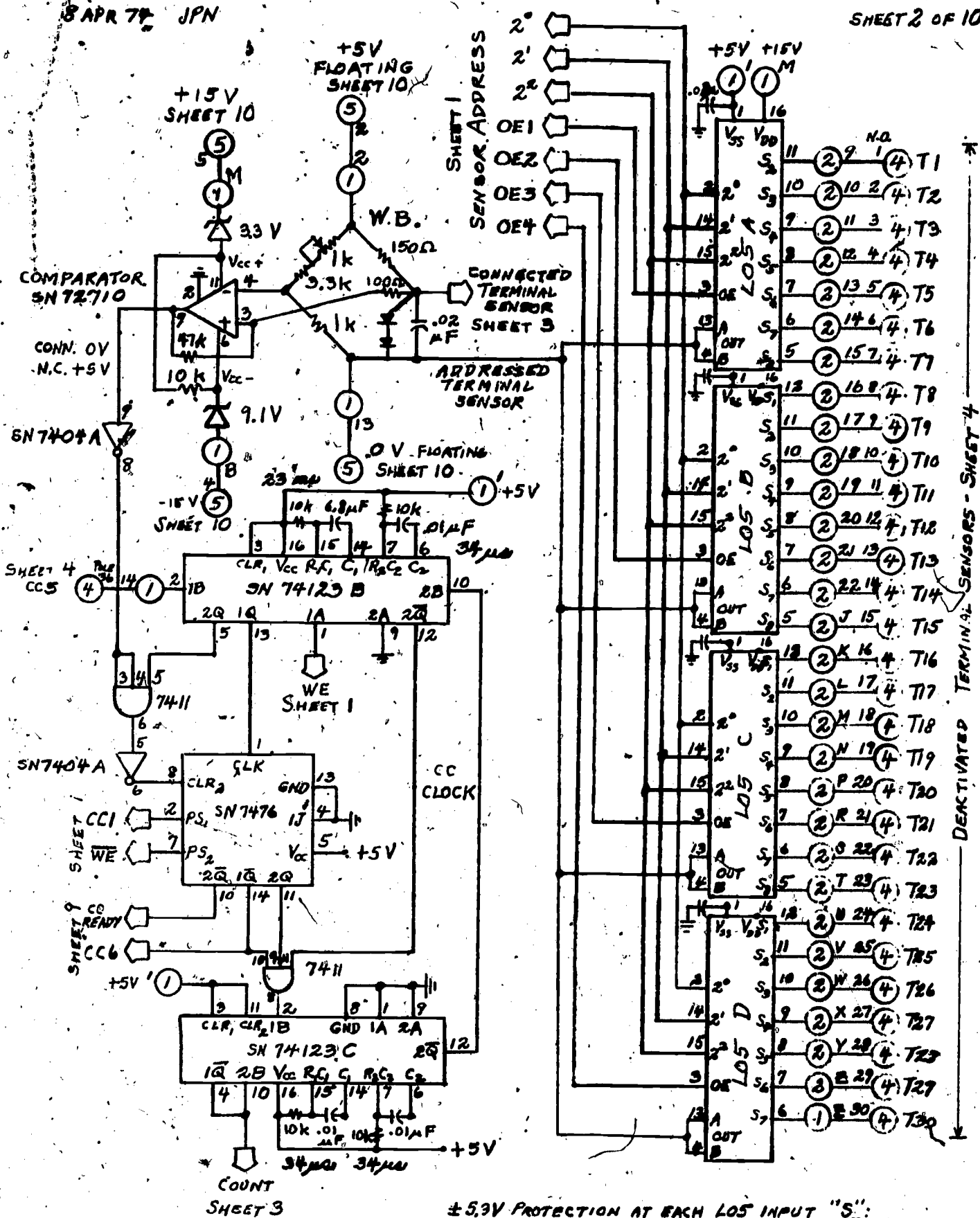
CGE INPUT FROM PLATO

8 FOR 74 JPN



THE CONNECTION CHECKER

8 APR 71 JPN

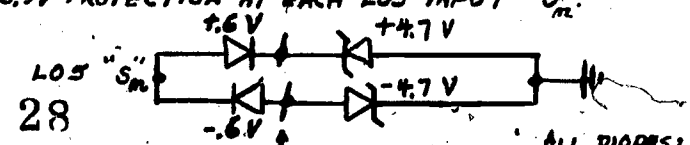


W.B. (WHEATSTONE BRIDGE) ADJUSTMENT:

INTERCONNECTION < 36Ω

NO CONNECTION > 36Ω

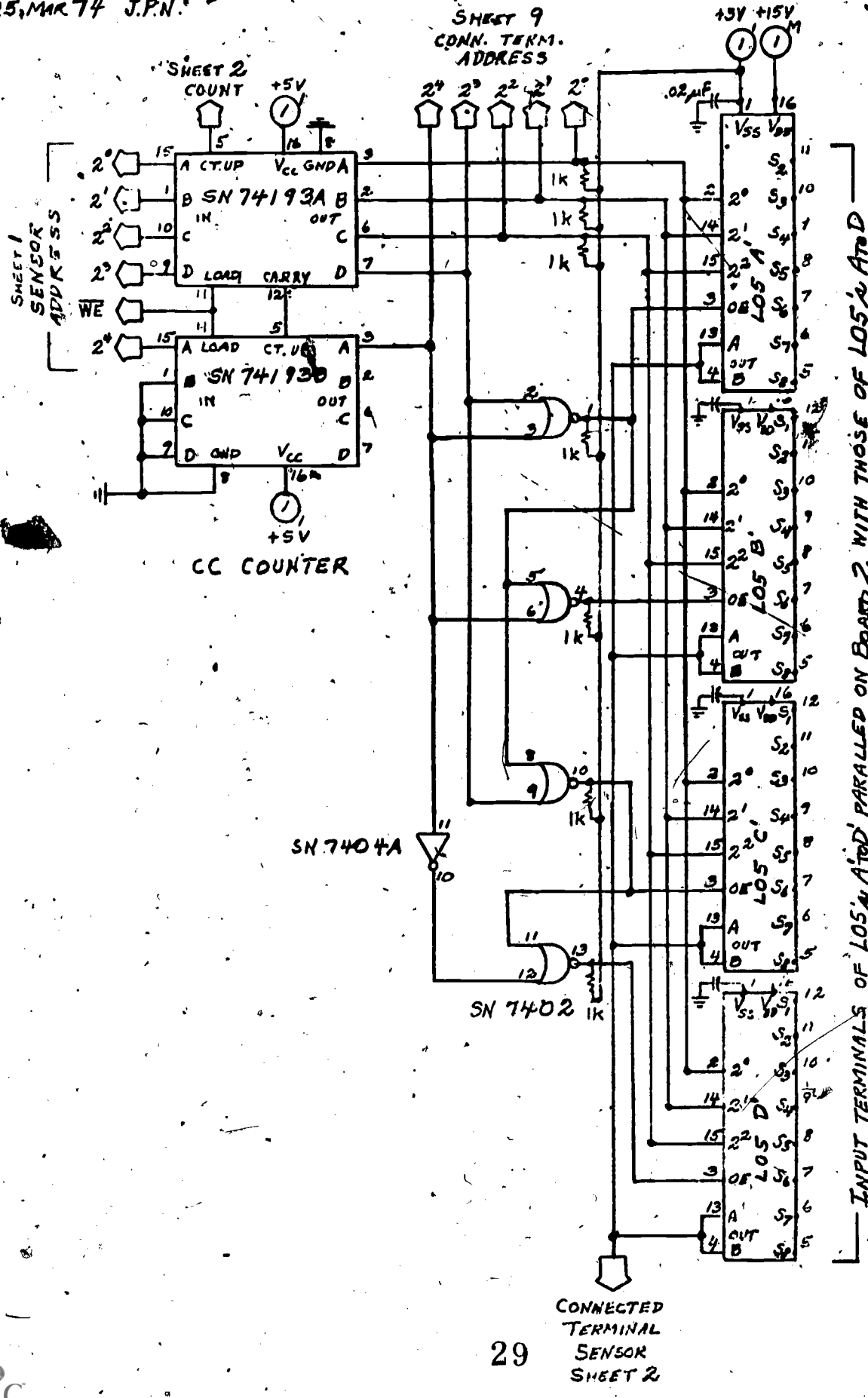
±5.3V PROTECTION AT EACH LOS INPUT "S_m":



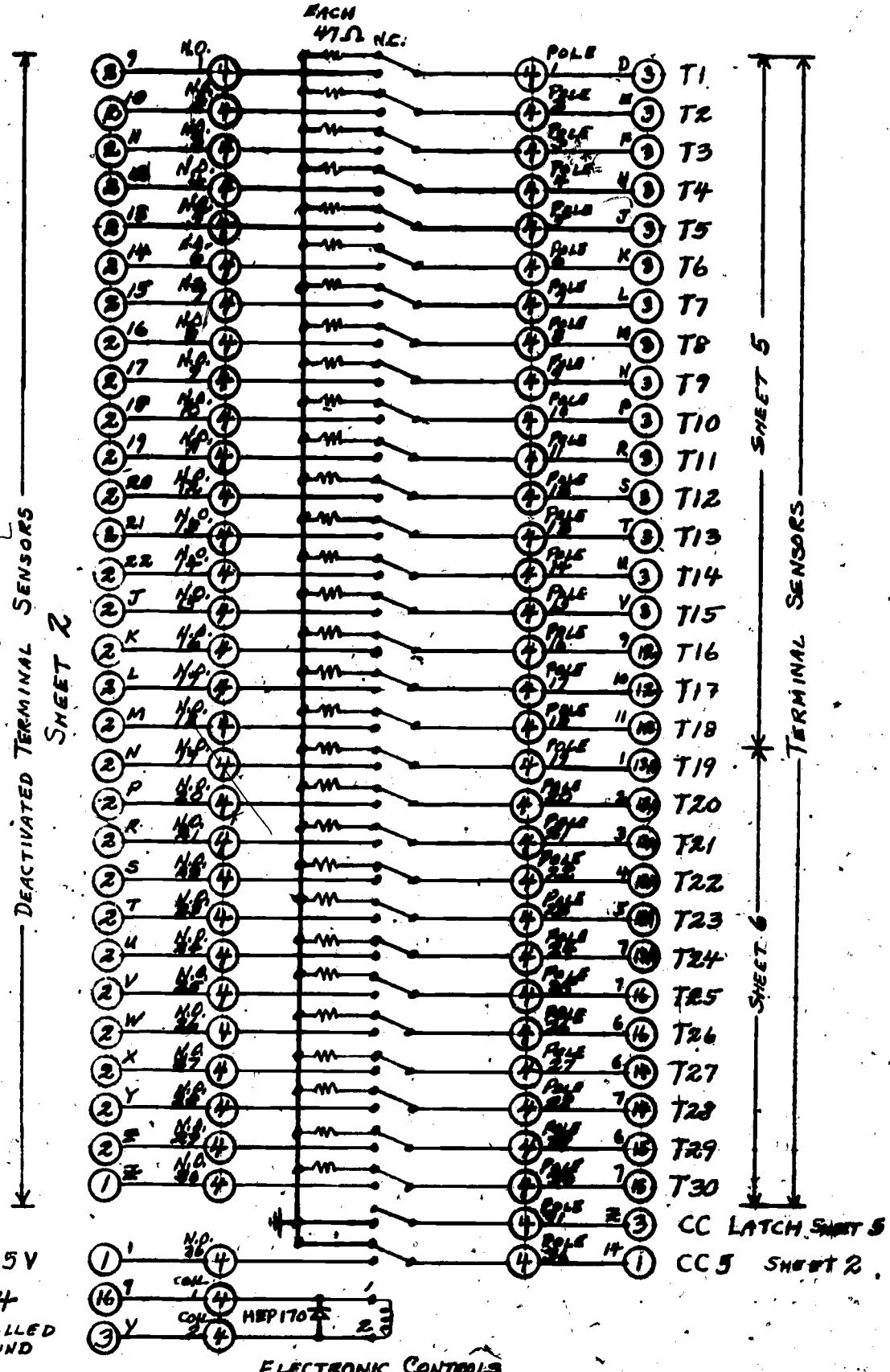
ALL DIODES: IN914.

THE CONNECTED-TERMINAL SELECTOR

25, MAR 74 J.P.N.

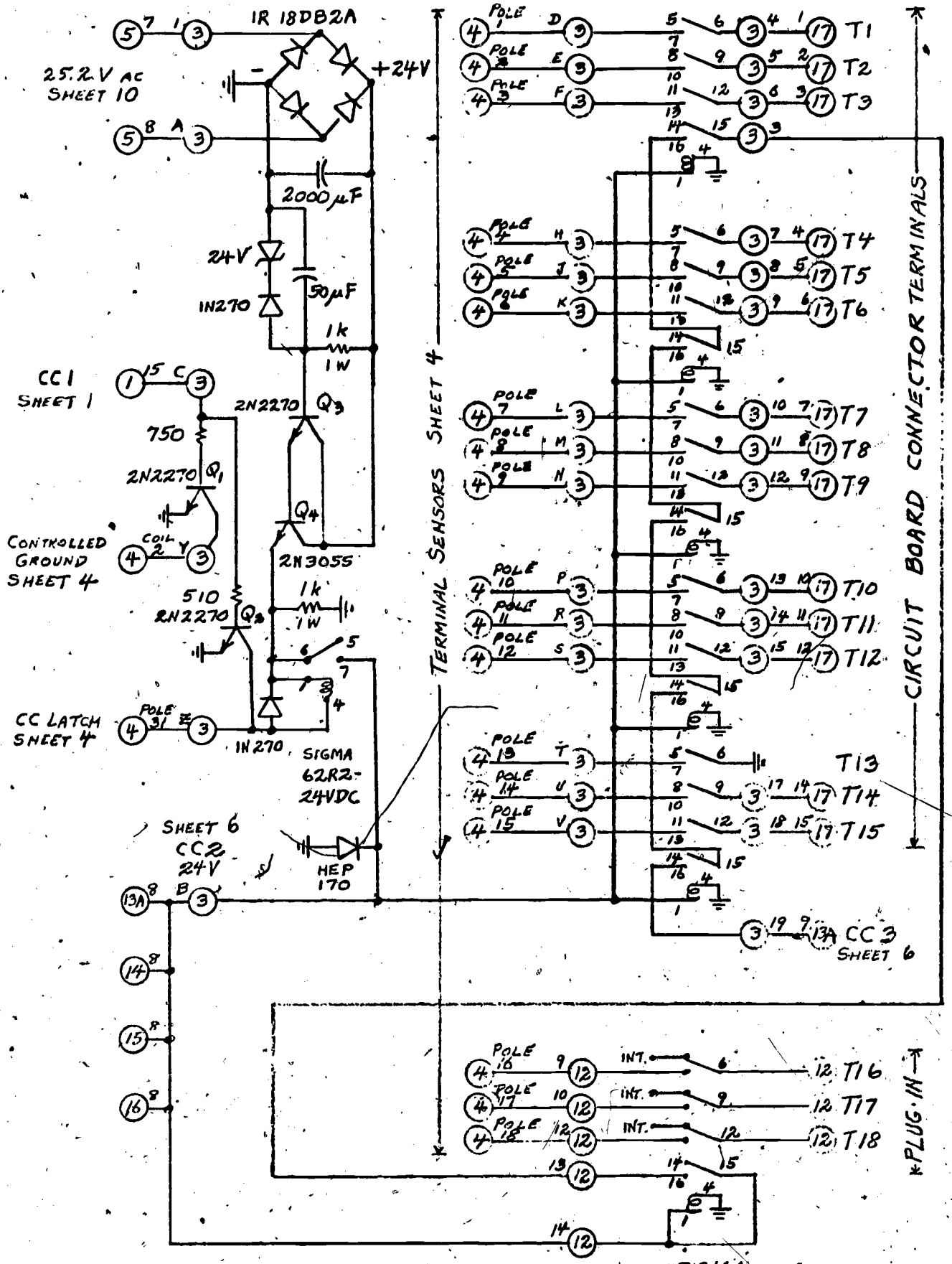


THE CC RELAY

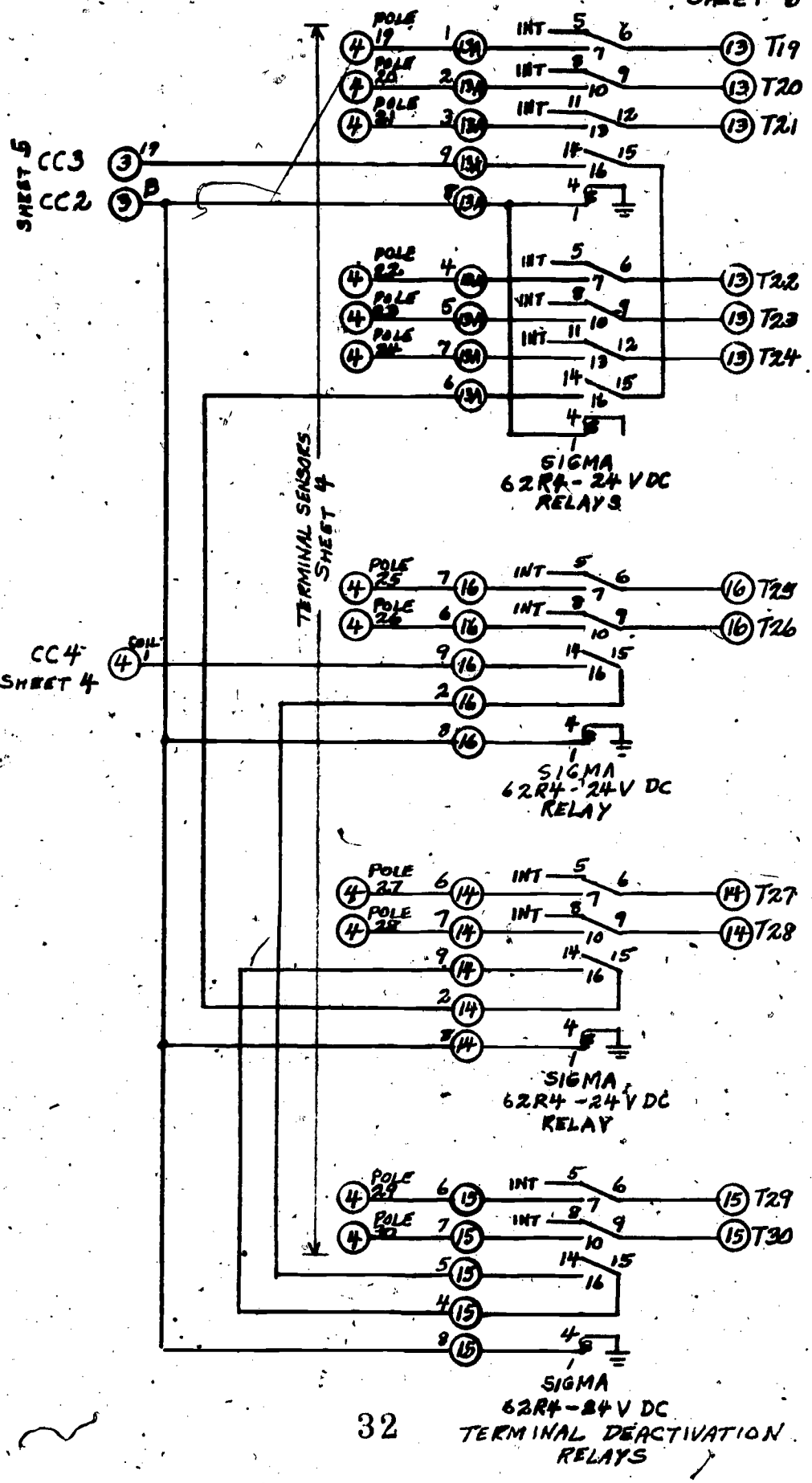


ELECTRONIC CONTROLS
36PDT CC RELAY
#36C24

TERMINAL SENSORS I

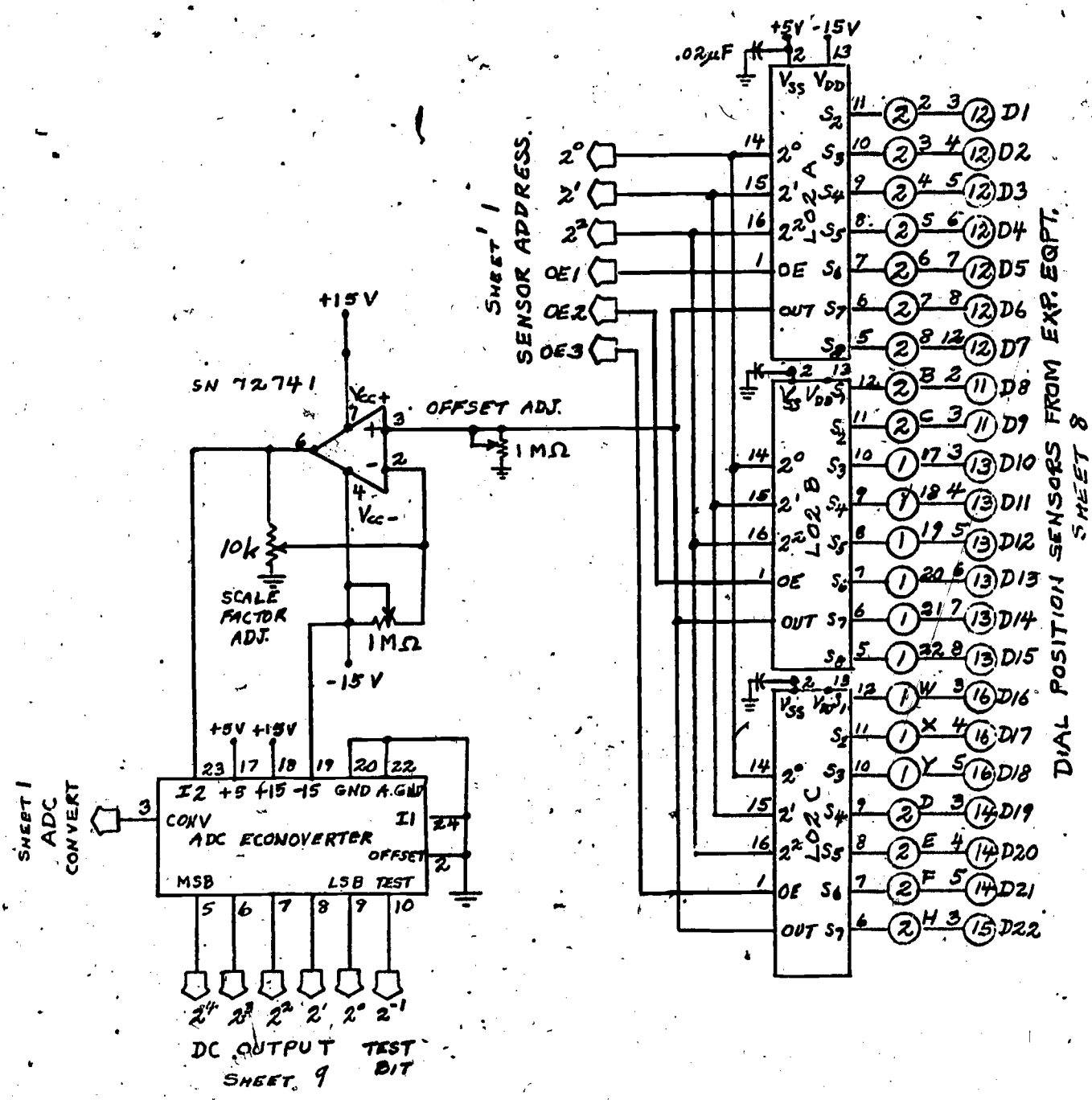


TERMINAL SENSORS II



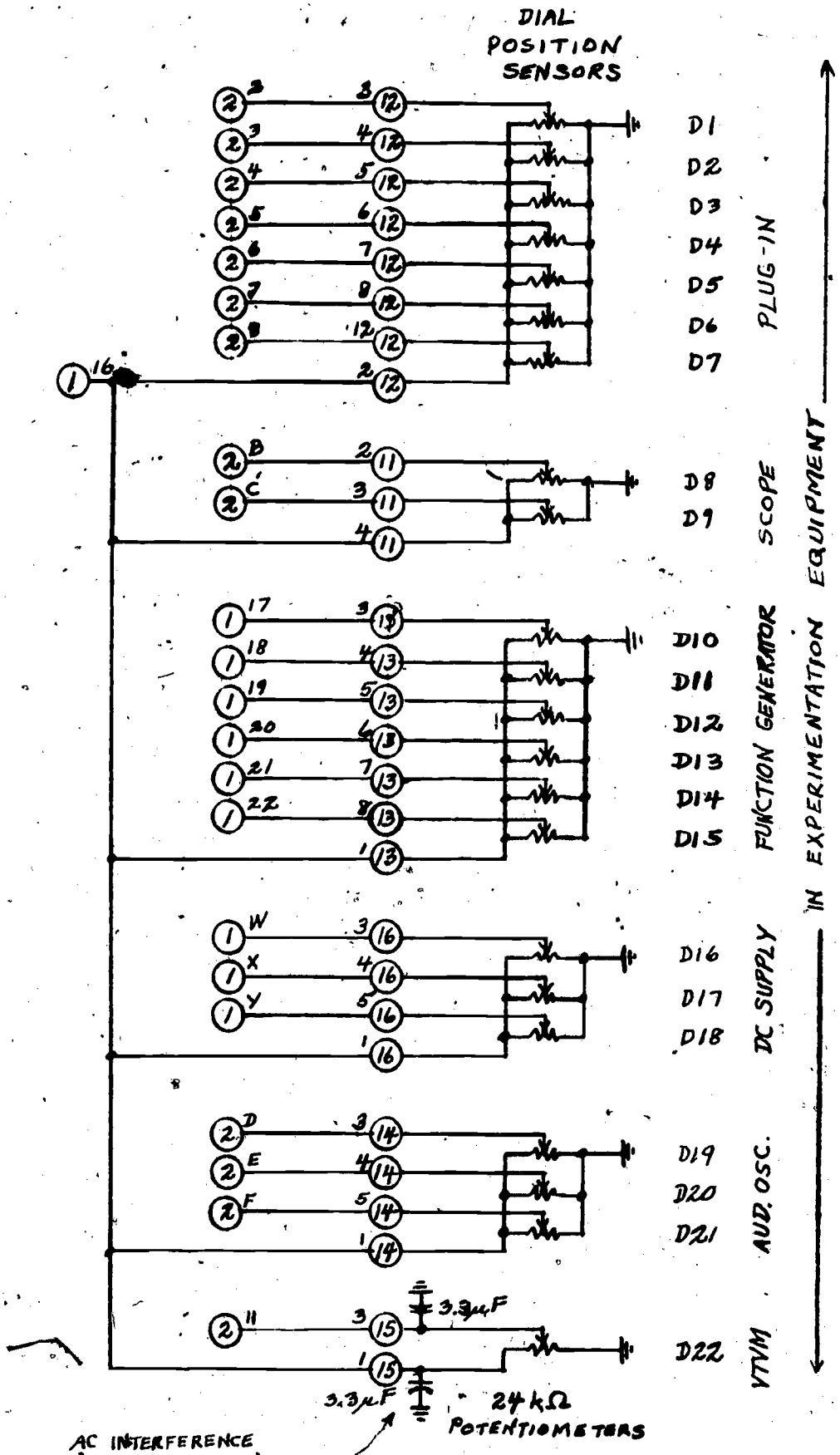
THE DIAL CHECKER

7 APR 74 JPN



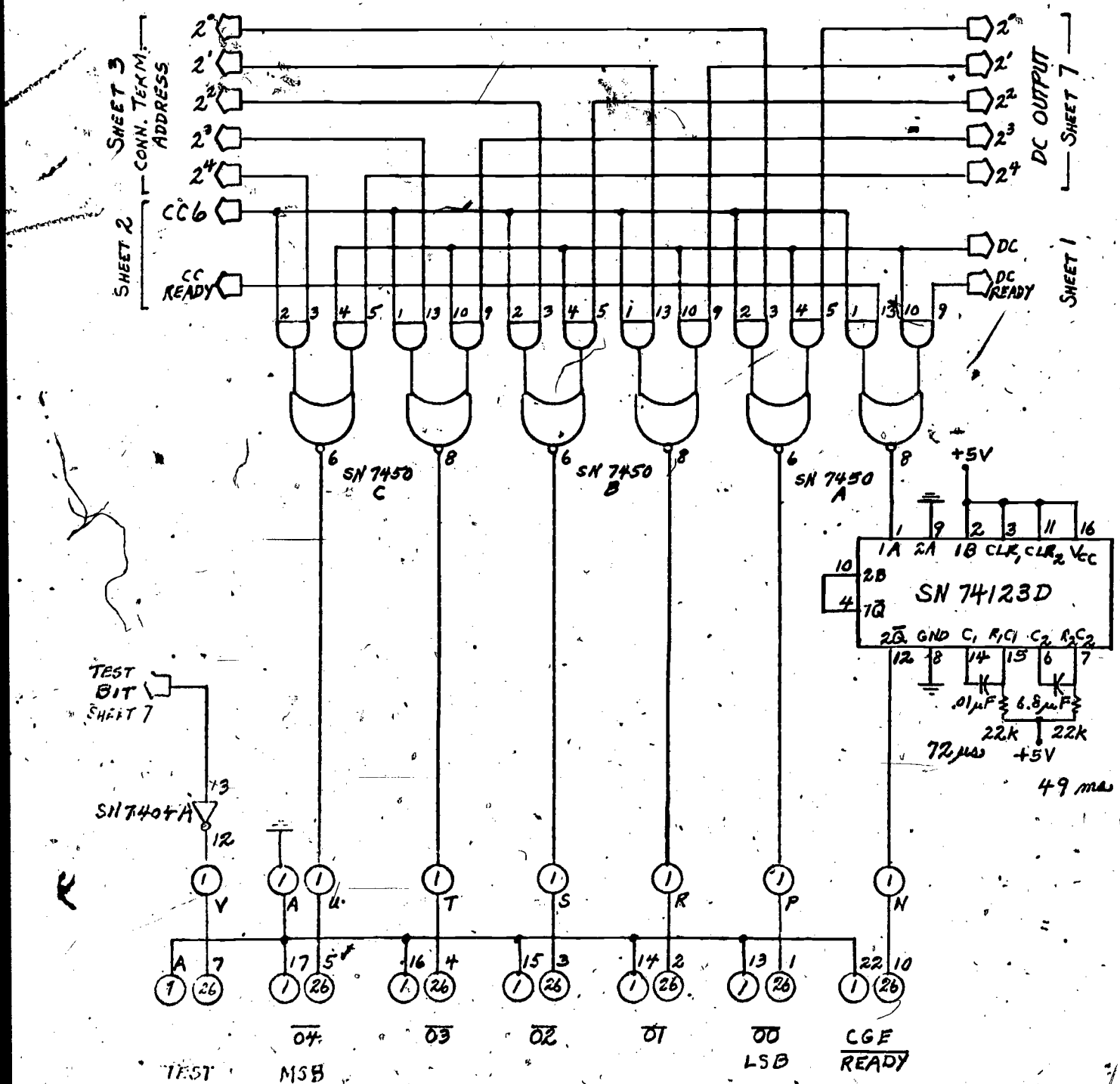
DIAL SETTING SENSORS

11 APR 74 JPN



CGE OUTPUT TO PLATO

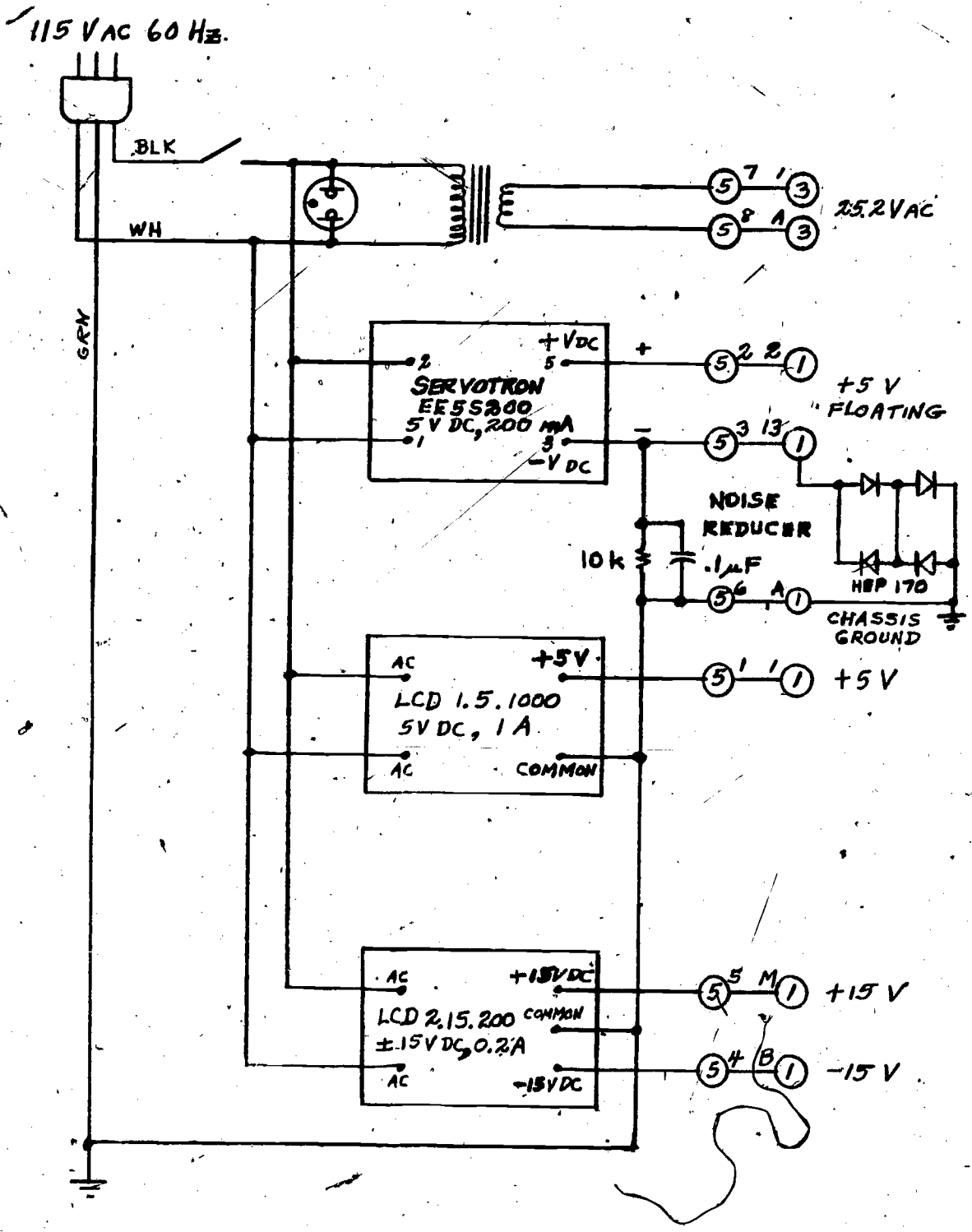
9 APR 74 JPN



PARALLEL OUTPUT
EXT IN-PLATO

POWER SUPPLIES

12 MAR 74 JPN



2.4 Descriptions of Important Hardware Components

Throughout the CGE-PLATO Interface Logic System, resistors, capacitors, and diodes have been introduced to stabilize the operation, or prevent transient effects that may damage the integrated circuit components. Every component used has been found necessary through practical experience with the system. The last modification to the hardware was made on 25 March 1974, and no significant CGE hardware failures have occurred since that time. As of 8 April 1974, complete Connection Checks and complete Dial Checks have been performed since 3 December 1973.

Certain hardware components materially contributed to increasing the speed and reliability of the interface and enabled a tremendous reduction in the number and size of its discrete components. Therefore, it seems desirable to reproduce the manufacturer's descriptions of these components in this report, as follows:

INSELEK

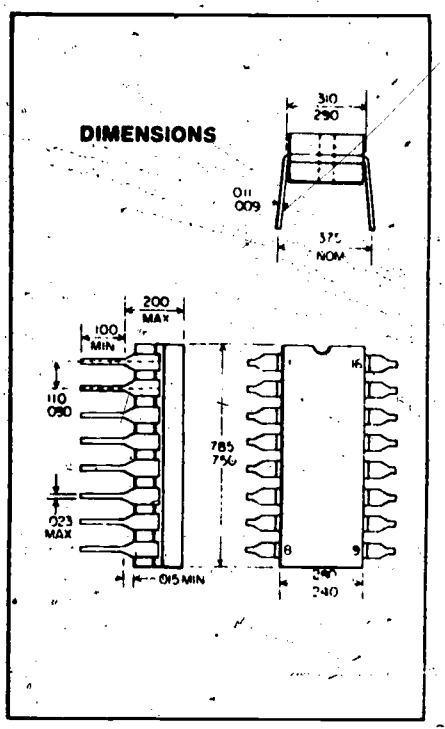
LO2

SOS/MOS 8 Channel Multiplexer

HIGH-SPEED • LOW-POWER • MOS INTEGRATED CIRCUITS ON INSULATING SUBSTRATES • LOW-POWER • HIGH-SPEED

GENERAL DESCRIPTION

The LO2 is an 8 channel multiplex switch with output enable control and 1-out-of-eight decoder included on the chip. Vastly superior characteristics are obtained through the unique process of forming SOS/MOS transistors on an insulating substrate. The logic input lines of the LO2 can be used directly with TTL logic levels with no level shifting interface required. The channel switching time is typically 20 times faster, while power dissipation is only one tenth that for conventional P-MOS multiplexers.

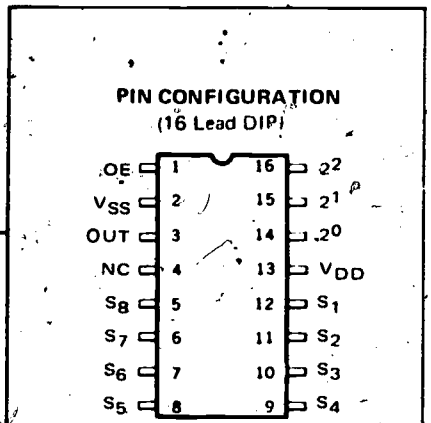


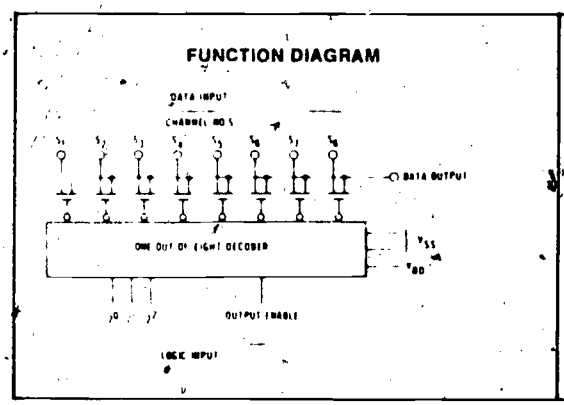
FEATURES

- TTL Compatible Input Logic Levels
- One-Out-Of-Eight Decoder on the Chip
- High On-Off Ratio
- Output Enable Control
- Fast Switching Time 50 ns
- Low Power Dissipation
- Input Gate Protection
- Low Leakage Current
- Zero Offset Voltage
- ±5 V Analog Signal Range

APPLICATIONS

- A/D Converters
- Data-Transmission Multiplexing
- Signal Selectors





TRUTH TABLE

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

C0005

1272

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{DD} with respect to most positive supply voltage V_{SS}	−22V
Control input voltages with respect to V_{SS}	−22V
Data input and output voltages with respect to V_{SS}	−22V
Storage temperature TA	−65°C to +150°C
Operating temperature TA	0°C to +75°C

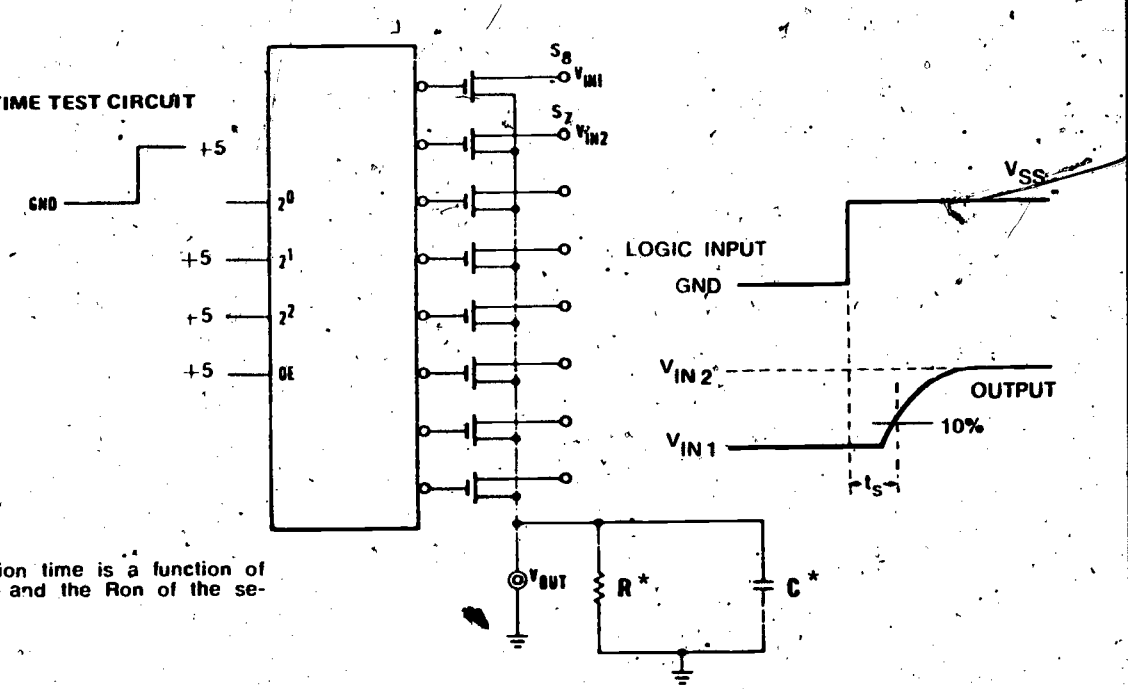
RECOMMENDED OPERATING VOLTAGES

V_{SS} = +5 V ± 5%.
V_{DD} = −15 V ± 5%.

ELECTRICAL CHARACTERISTICS (25°C) $V_{SS} = 5.0V$, $V_{DD} = -15V$, $-5.0V < V_{OUT} < 5.0V$

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
R_{ON}	Data Channel "ON" Resistance		250	400	Ω	$V_{OUT} = -5.0$ V, $I_{OUT} = -100\ \mu A$
R_{OFF}	Data Channel "OFF" Resistance	1.5	3.0		GΩ	$V_{OUT} = 0V$, OE = 0V, $V_{IN} = -5V$.
I_{LO}	Output Shunt Leakage Current		50	200	pA	$V_{OUT} = 0V$, OE = 0V, V_{IN} = N.C.
I_{LDI}	Data Input Shunt Leakage Current		100	500	pA	$V_{IN} = -5V$, OE = 0V, V_{OUT} = N.C.
V_{IL}	Logic Gate Input "Low" Level			0.8	V	
V_{IH}	Logic Gate Input "High" Level	3.2			V	
t_s	Channel Switching Time		45	70	ns	FIG. 1
C_{db}	Output Capacitance		8.5		pF	V_{OUT} = 5 V, f = 1.0 MHz
C_{is}	Data Input Capacitance		2.5		pF	VIN = 5 V, f = 1.0 MHz
P_D	Power Dissipation		50	150	mW	OE = 0 V

Fig. 1— SWITCHING TIME TEST CIRCUIT



*The output transition time is a function of external R and C and the Ron of the selected switch

University Park Plaza
743 Alexander Road
Princeton, New Jersey 08540
Phone: (609) 452-2222
Cable Inselek

INSELEK

L05

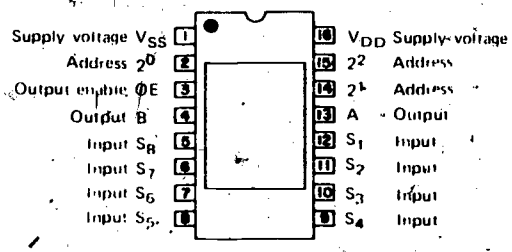
Low Resistance 8 Channel Multiplexer

INSELEK

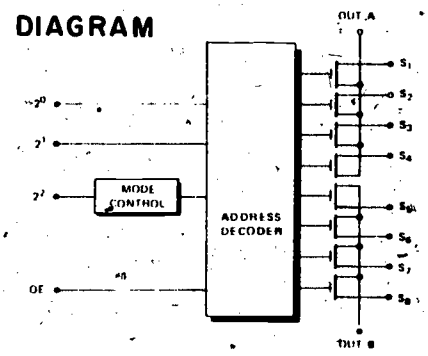
HIGH-SPEED • LOW POWER • MOS INTEGRATED CIRCUITS ON INSULATING SUBSTRATES • LOW POWER • HIGH-SPEED

- **Low On Resistance: 15 Ohms**
- **Dual Mode: Single 8/Dual 4 Channel**
- **Fast: 75 nS Channel To Channel**
- **TTL Compatible**
- **Expandable: Output Enable Provided**

PIN CONFIGURATION



FUNCTION DIAGRAM

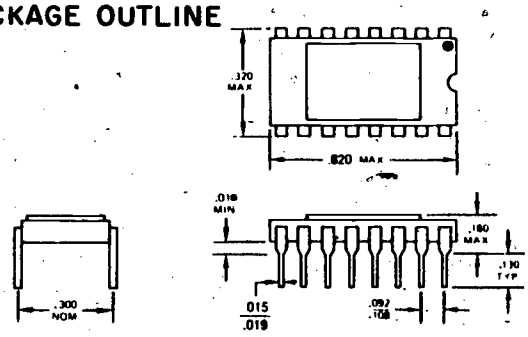


TRUTH TABLE

CONTROL INPUTS 2^2	2^1	2^0	OE	A CONNECTED TO	B CONNECTED TO
0	0	0	1	S_1	
0	0	1	1	S_2	
0	1	0	1	S_3	
0	1	1	1	S_4	
1	0	0	1		S_5
1	0	1	1		S_6
1	1	0	1		S_7
1	1	1	1		S_8
V_{DD}	0	0	1	S_1	S_5
V_{DD}	0	1	1	S_2	S_6
V_{DD}	1	0	1	S_3	S_7
V_{DD}	1	1	1	S_4	S_8
X	X	X	0	OPEN	OPEN

1 HIGH (+V)
0 LOW (0V)

PACKAGE OUTLINE



GENERAL DESCRIPTION

The LO5 is a low-resistance 8-channel multiplex switch with decoding and output-enable (chip select) controls. Three address input lines are decoded to select one of the eight channels. Alternatively, the most significant address line (2^2) may be connected to V_{DD}, thereby changing the switch mode to dual 1-out-of-4. The remaining address lines (2^1 and 2^0) then are decoded to select the desired pair of channels.

The TTL-compatible address and output-enable input buffers incorporate a unique latch feature; these input terminals retain their last logic state when the input terminal is floated.

OPERATION

1-out-of-8 Mode: Connect Output A to Output B. Apply binary address codes to the three address lines.

Dual 1-out-of-4 Mode: Connect 2^2 address line to V_{DD} supply. Apply binary codes to 2^1 and 2^0 address lines.

All switches are disconnected when Output Enable (OE) is low.

C00238

AUGUST 1973

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{DD} with respect to most positive supply voltage V_{SS}	−25V
Control input voltages with respect to V_{SS}	−25V
Data input and output voltages with respect to V_{SS}	−25V
Data (switch) current	50 mA
Storage temperature T_A	−65°C to + 150°C
Operating temperature T_A	0°C to + 75°C

RECOMMENDED OPERATING VOLTAGES

V_{SS} = +5V ± 5%.
V_{DO} = −16 ± 5%

CAUTION: Care in handling of this device is mandatory to prevent damage to the outputs due to static electricity. To retain the inherent high impedance levels of the device, no protective circuitry is used at the outputs. Recommendations include use of conductive foam or trays for out-of-circuit handling, grounding of soldering iron tips, and device removal or insertion only with power supplies turned off. Operators handling the components during test or assembly should wear grounded wrist-straps.

ELECTRICAL CHARACTERISTICS (25°C) V_{SS} = 5.0V, V_{OD} = −16V, $-5.0V < V_{OUT} < 5.0V$

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
R_{ON}	Data Channel "ON" Resistance		15	40	Ω	V_{OUT} = 0V, I_{OUT} = 1 mA
R_{OFF}	Data Channel "OFF" Resistance	10	250		MΩ	V_{OUT} = 0V, OE = 0V, V_{IN} = −5V
I_{LO}	Output Shunt Leakage Current		500		pA	V_{OUT} = 0V, OE = 0V, V_{IN} = N.C
I_{LDI}	Data Input Shunt Leakage Current		1		nA	V_{IN} = −5V, OE = 0V, V_{OUT} = N.C.
V_{CL}	Control Input "Low" Level	V_{DD}		0.8	V	
V_{CH}	Control Input "High" Level	3.2		V_{SS}	V	
I_{CF}	Control Input Load Current		10		μA	V_C = 0V
I_{CR}	Control Input Leakage Current		−20		μA	V_C = 5V
C_{db}*	Output Capacitance		32		pF	V_{OUT} = 5V, f = 1.0 MHz
C_{is}	Data Input Capacitance		8		pF	V_{IN} = 5V, f = 1.0 MHz
P_D	Power Dissipation		150	400	mW	OE = 0V

*A transient current of maximum value = 1.6 mA occurs during a one to zero transition at each input terminal.

SWITCHING CHARACTERISTICS (Fig. 1)

V_{SS} = 5V V_{OO} = −16V T_A = 25°C

	PARAMETERS	LIMITS			UNITS
		MIN.	TYP.	MAX.	
t_{CC}	Channel to channel switching time		75	150	nS
t_{EC}	Enable to channel switching time		50	150	nS
t_{DC}	Disable to channel switching time		75	150	nS

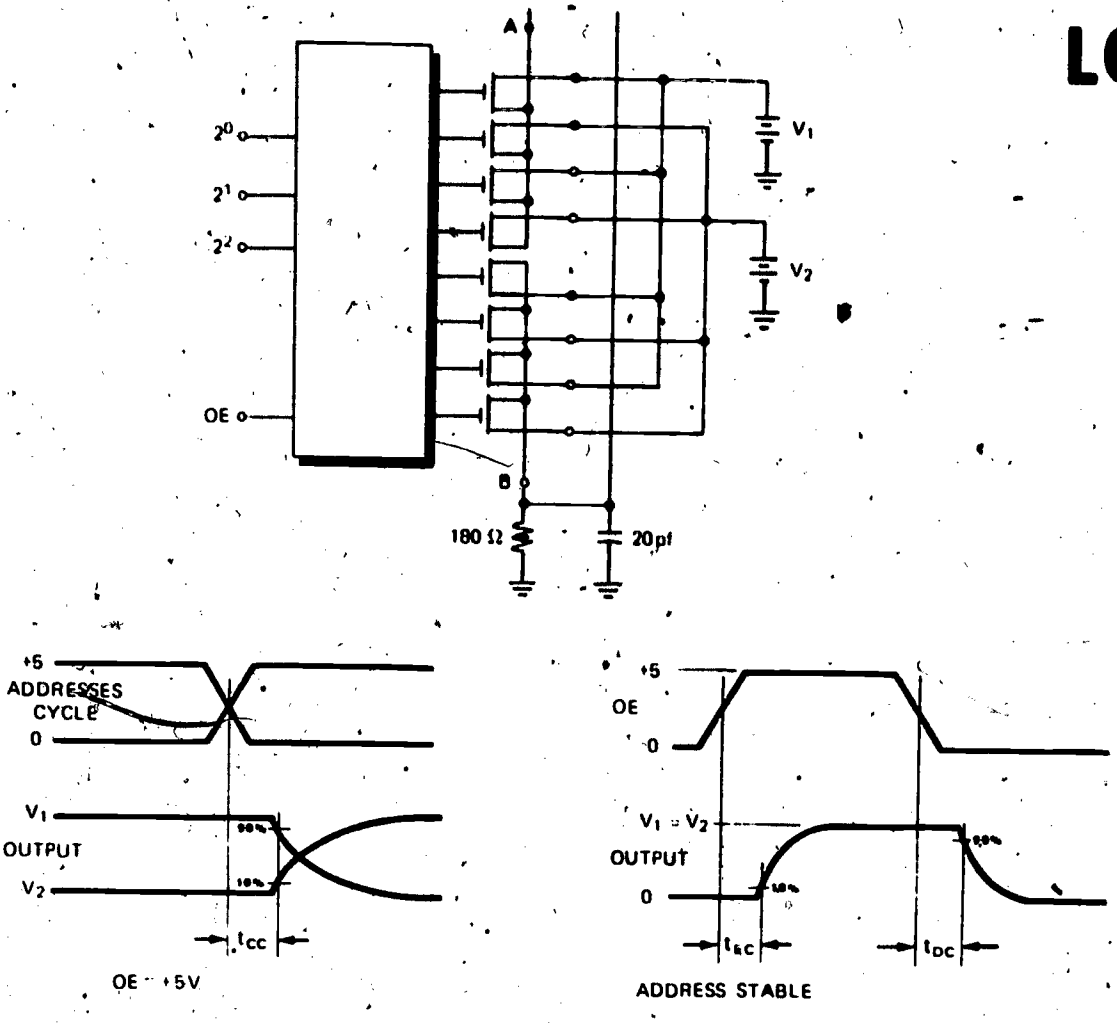


FIGURE 1
SWITCHING TESTS

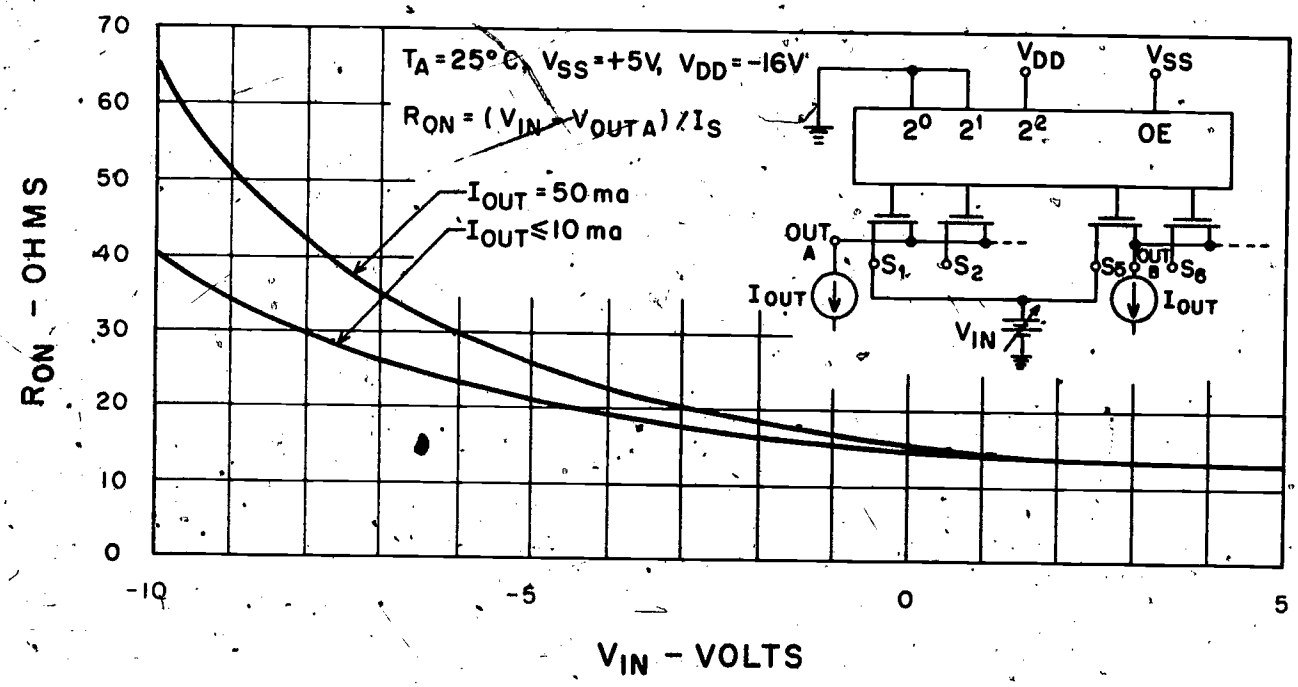
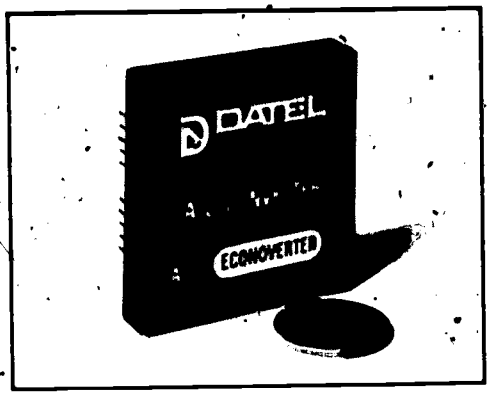


FIGURE 2
TYPICAL ON RESISTANCE VERSUS ANALOG-INPUT VOLTAGE

DATEL SYSTEMS, INC.



ANALOG -TO-DIGITAL CONVERTER

ADC ECONOVERTER

20 KHz A/D CONVERTER FOR UNDER $30.00

Datel Systems has achieved a major breakthrough in Analog to Digital converter design by use of a proprietary measurement technique and state of the art packaging fabrication. The Econoverter is completely self contained in a miniature plastic case measuring 2" x 2" x .375".

Simplified operation, small size, and low cost make this converter ideally suited to OEM applications. Market areas include avionics, automatic semiconductor test equipment, computer equipment, process control, geophysical instruments, medical electronic instruments/systems, oceanographic instruments, data transmission or any requirement where high resolution is not of prime importance.

Econoverter is available with six bit resolution with a digitizing speed of 50 µsec for a full scale input excursion and is proportionally faster for less than full scale inputs. Analog input voltage range can be either unipolar (0V to +5V or 0V to +10V) or bipolar (±2.5V or ±5V) by means of externally programming the unit via pin strapping. Overall accuracy is adjustable to ± 1/2 LSB. Output digital coding is straight binary for unipolar inputs and offset binary for bipolar inputs.

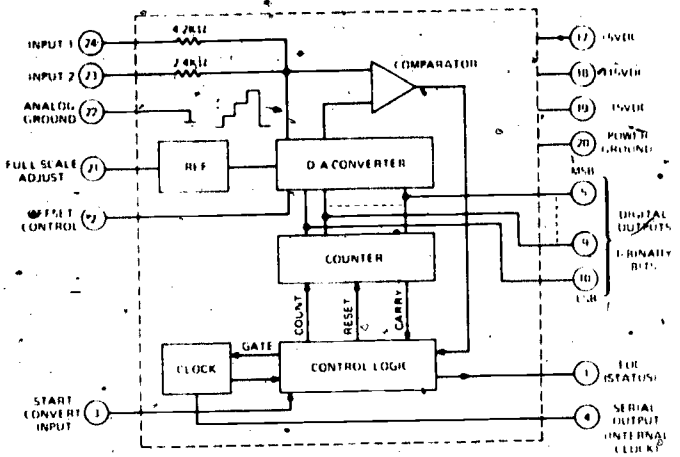
The Econoverter is adjustment free over an operating temperature range of 0° to +70°C and has a temperature coefficient of ±100 ppm/°C with long term stability of ±0.1%/year. All digital inputs and outputs are compatible with standard TTL/DTL logic levels. Input power requirements are +5VDC @ 80 ma, +15VDC @ 15 ma, and −15VDC @ 5 ma.

Econoverter is fully encapsulated and features dual-in line pinning compatibility, .100" grid pin spacing.

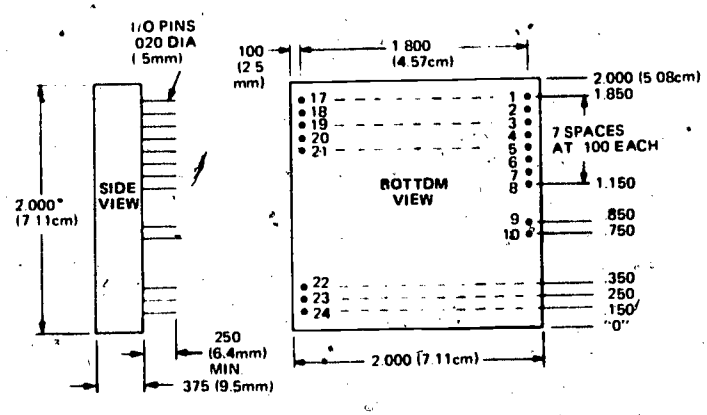
FEATURES

☐ Low cost	**$29.95** single quantity
☐ Small size	1.6 cubic inches
☐ Low power consumption	0.7 watts
☐ Programmable input	Unipolar or bipolar
☐ Fast conversion rate	20 KHz, 6 Bit resolution
☐ Self contained	Simply apply D.C. power
☐ Excellent long term stability	±0.1%/year
☐ OEM designed	Generous discounts available

BLOCK DIAGRAM - ADC ECONOVERTER



MECHANICAL DIMENSIONS, INCHES (METRIC)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	E.O.C. (STATUS)
2	OFFSET CONTROL
3	START CONVERT
4	INTERNAL CLOCK OUT (SERIAL OUTPUT)
5	BIT 1 OUT (MSB)
6	BIT 2 OUT
7	BIT 3 OUT
8	BIT 4 OUT
9	BIT 5 OUT
10	BIT 6 OUT (LSB)
17	+5V POWER INPUT
18	+15V POWER INPUT
19	−15V POWER INPUT
20	POWER GROUND
21	F.S. ADJUST
22	ANALOG GROUND
23	ANALOG INPUT 2
24	ANALOG INPUT 1

ELECTRICAL

Inputs:

Analog input voltage range . . . . . .

VOLTAGE RANGE	ANALOG INPUT PIN	JUMPER PINS
0V to +5V	23	22 to 24, 2 to 20
0V to +10V	24	22 to 23, 2 to 20
±2.5V	23	22 to 24, 2 to 17
±5V	24	22 to 23, 2 to 17

Input impedance . . . . . Input pin 23: 2.4K Ohms
Input pin 24: 4.2K Ohms

Input overvoltage . . . . . ±20V

Start of conversion . . . . 2V min. to 5.5V max.
Positive pulse with duration of 100 nsec min. Rise and fall times <500 nsec
Leading edge resets converter.
Trailing edge initiates conversion.
Loading: 2TTL loads

Outputs:

Parallel output data . . . . 6 parallel lines of data held until next conversion command.
V out ("0") ≤ +0.4V
V out ("1") ≥ +2.4V
Each output capable of driving up to 6 TTL loads.

Output coding . . . . . Straight binary (Unipolar input)
Offset binary (Bipolar input)

End of conversion . . . . . V out ("0") ≤ +0.4V during conversion
V out ("1") ≥ +2.4V conversion complete
Loading up to 6 TTL loads.
NOTE: End of conversion output will remain at logic "0" if analog input exceeds the positive full scale voltage.

Internal clock (serial output) . . . . . Pulse train, 50% duty cycle (TTL logic levels). Each negative transition indicates one count, up to 63 counts.

Performance:

Resolution . . . . . One part in 64.

Linearity . . . . . ± 1/2 LSB.

Full scale accuracy . . . . ± 1 LSB.

NOTE 1: The +15VDC power supply input is used as the reference voltage. Therefore, the F.S. voltage is directly proportional to this voltage.

NOTE 2: The full scale accuracy can be improved by external trimming.
To reduce the F.S. voltage connect a trim resistor from pin 21 to pin 18.
To increase the F.S. voltage connect a trim resistor from pin 21 to pin 22. Trim resistor range 50K to 2 Meg.

Long term stability . . . . . ±0.1%/year

Temperature coefficient . . . ±100ppm/°C

Encoding time . . . . . Min: 0.5 μsec (zero scale)
Max: 50 μsec (full scale)

Reading rate . . . . . Up to 20,000 samples/sec. for full scale, proportionally faster for less than F.S. inputs.

Input power requirements . . . . . +15VDC, ±0.5VDC @ 15 ma max
−15VDC, ±0.5VDC @ 5 ma max
+ 5VDC, ±0.25VDC @ 80 ma max

PHYSICAL—ENVIRONMENTAL

Operating temp. range . . . 0° to +70°C

Storage temp. range . . . . −55°C to +85°C

Relative humidity . . . . . Up to 100% non-condensing

Size . . . . . 2"W x 2"L x 0.375"H

Pins . . . . . 0.020" round gold plated, 0.250" long min.

Case material . . . . . Black Diallyl Phthalate, per MIL-M-14. Converters fully repairable

Weight . . . . . 4 oz. max.

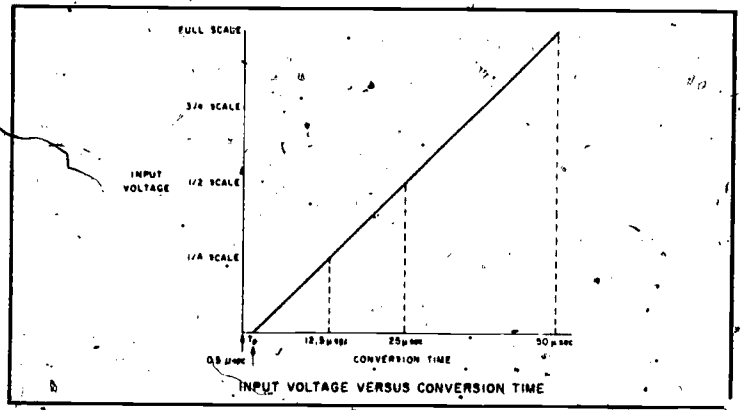
Mating Socket . . . . . DILS-2, 2 Req'd. per module, $5/pr.

ORDERING INFORMATION

MODEL — ADC ECONOVERTER
UNIT PRICE . . . $29.95 ea.

OUTPUT CODING FOR ECONOVERTER

ANALOG INPUT RANGE (±5V, FS)	OFFSET BINARY	ANALOG INPUT RANGE (0 TO +10V, FS)	STRAIGHT BINARY
+4.84	111111	+9.84	111111
+4.37	111100	+8.75	111000
+3.75	111000	+7.50	110000
+2.50	110000	+5.00	100000
0.00	100000	+2.50	010000
−2.50	010000	+1.25	001000
−3.75	001000	0.00	000000
−4.37	000100		
−4.84	000001		
−5.00	000000		



INPUT VOLTAGE VERSUS CONVERSION TIME

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

DATEL SYSTEMS, INC. 1020 TURNPIKE STREET, CANTON, MASS. 02021 TEL. (617) 828-8000 TWX: 710-348-0135 TELEX: 924461

 Bulletin AECCT15404

ECONOMY ENCAPSULATED LINE TO DC REGULATED POWER SUPPLIES

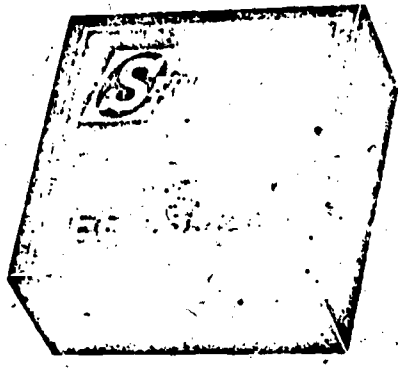
SERVOTRON CORPORATION

SERVOTRON'S EE SERIES of regulated power supplies was designed to provide the "power fit" in performance, price and packaging for the new, low cost LED, MOS, TTL, DTL, D-A Converters, Function Modules and Operational Amplifiers.

WOULD YOU BELIEVE???

Regulated (0.25%) dual and single outputs . . .
Compact (2" x 2" x .875") modular packaging . . .
Priced at $12** in unit quantities . . .

UNBELIEVABLE?. BUT TRUE!



SPECIAL FEATURES:

- $9.97** (1K quantities)
- Short Circuit Protected
- Miniature Size
- No Derating Over Specified Temperature Range

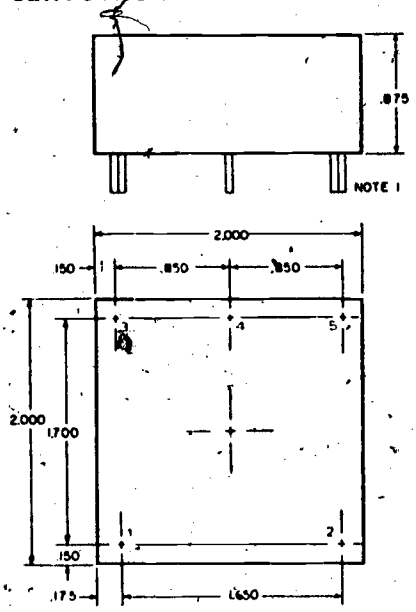
SPECIFICATIONS:

MODEL		EE5S200	EE12D25	EE15D25
Output Voltage	Vdc	5	± 12	± 15
Output Current	mA	200*	25*	25*
Regulation — Line (105-125 Vac)		.25%*		
Regulation — Load (0-100%)		.25%*		
Ripple and Noise	mV rms	2*		
Temperature Coefficient	/°C	.02%		
Warm Up Drift	mV	15		
Output Voltage Tolerance (Factory set)		± 1%		
Input Voltage and Frequency		105-125 Vac, 50-440 Hz		
Operating Temperature		–25 to + 71°C		
Storage Temperature		–25 to +85°C		
Case Dimensions (Servotron SC-3 Outline)		2" x 2" x .875"		
Connecting Instructions		SC-3A	SC-3B	SC-3B
Price	(1-99)	$14.00	$12.00	$12.00
Price	(1 K)	$11.75	$9.97	$9.97

* Indicates maximum specifications. **For Dual Output Models.

OUTLINE DIMENSIONS

SERVOTRON SC – 3 OUTLINE



BOTTOM VIEW

NOTE:

1. FIVE PINS .046 DIA. x .250 LG. MIN

CONNECTING INSTRUCTIONS

SINGLE OUTPUT MODELS

SERVOTRON SC–3A
CONNECTING INSTRUCTIONS

PIN 1. ac input
2. ac input
3. –Vdc output
4. No connection
5. +Vdc output

DUAL OUTPUT MODELS

SERVOTRON SC–3B
CONNECTING INSTRUCTIONS

PIN 1. ac input
2. ac input
3. –Vdc output
4. Common
5. +Vdc output

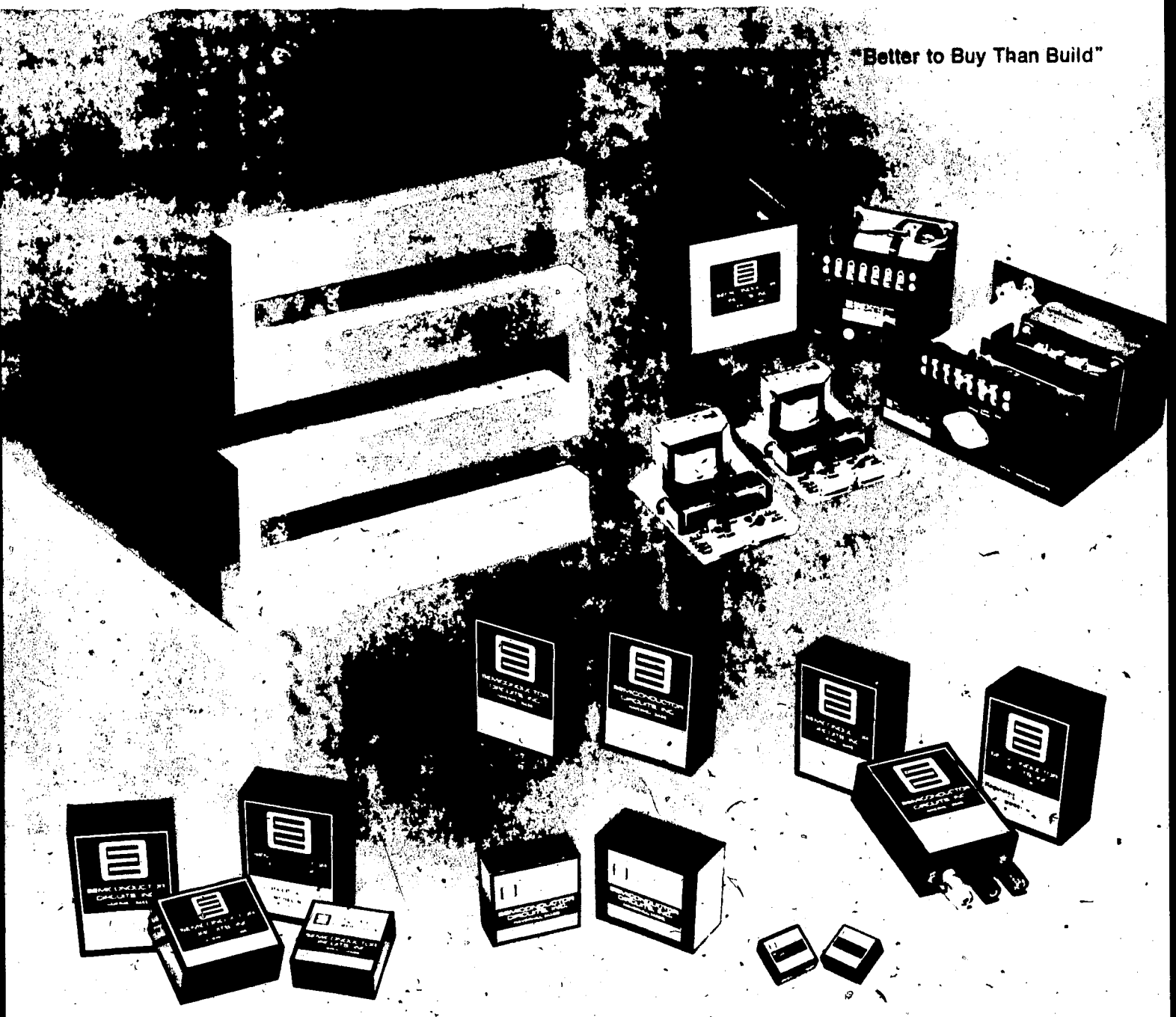
OPTIONS: (Add as suffix to part number)

E Input, 200 to 240 Vac, 50 to 440 Hz
($2.00 additional charge, 1-99)

ORDERING INFORMATION:

Prices are F.O.B. Haverhill, Mass. Terms are net 30 days to accounts that have established credit with Servotron. Orders of less than $25 with accompanying remittance must include $1.00 for transportation cost. Orders of less than $25 without accompanying remittance will be shipped C.O.D.

SERVOTRON CORPORATION
P.O. BOX 292 HAVERHILL, MASSACHUSETTS 01830 ■ TELEPHONE (617) 374-0777



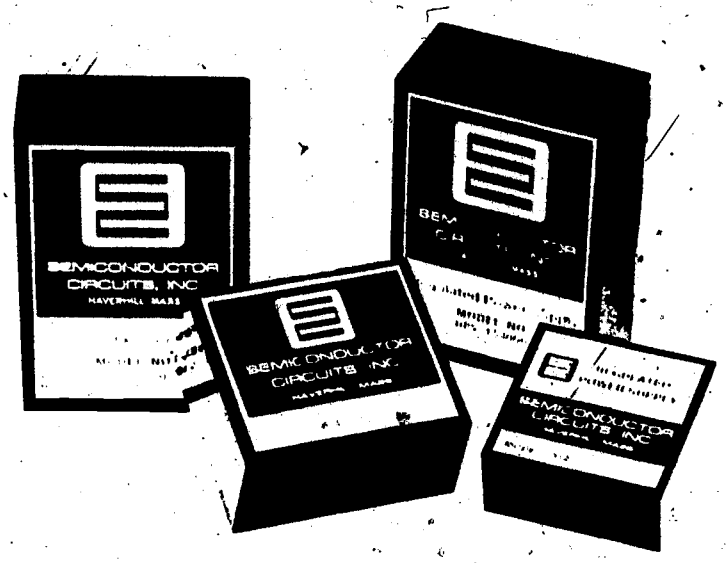
SCI CREED: *"To furnish the best possible solution. . . at a most favorable price."*

SEMICONDUCTOR CIRCUITS, INC.

HAVERHILL, MASSACHUSETTS

SQ P741 DPS LCD

Encapsulated Series



LOW COST MINIATURE POWER SUPPLY SERIES WITH BETTER THAN AVERAGE REGULATION

INPUT VOLTAGE AND FREQUENCY:
105 to 125 Vac – 50 to 440 Hz

RIPPLE AND NOISE (PARD):
1mVrms

TEMPERATURE COEFFICIENT:
0.02%/°C-typical

OUTPUT VOLTAGE TOLERANCE:
Factory set at ±1% (fixed)

OPERATING TEMPERATURE RANGE:
–25°C to +71°C

STORAGE TEMPERATURE RANGE:
–25°C to +85°C

- SHORT CIRCUIT PROTECTED
- NO DERATING UP THRU +71°C
- COMPACT SIZE
- ECONOMICALLY PRICED
- FLEXIBLE MOUNTING PINS

OUTLINE DIMENSIONS

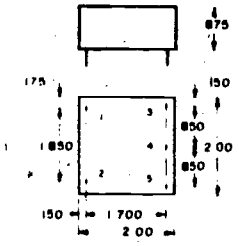


Fig. 1

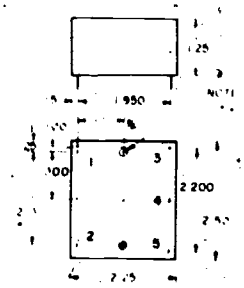


Fig. 2

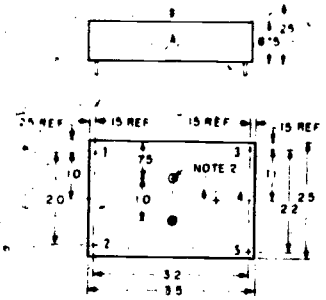


Fig. 3

CONNECTING INSTRUCTIONS

SINGLE OUTPUTS	DUAL OUTPUTS
PIN 1 ACin	PIN 1 ACin
2 ACin	2 ACin
3 Vdc out	3 -Vdc out
4 No Connection	4 Common
5 +Vdc out	5 +Vdc out
6 High Isolation 'J' Option only	

MODEL NO.	OUTPUT VOLTAGE Vdc	OUTPUT CURRENT mA	REGULATION LINE %	REGULATION LOAD %	PACKAGE SIZE fig.	UNIT PRICES 1-9
SQ1.5.200	5	200	0.25	0.25	1	$19.95
SQ2.12.30	±12	± 30	0.25	0.25	1	19.95
SQ2.12.50	±12	± 50	0.25	0.25	1	28.95
SQ2.15.30	±15	± 30	0.25	0.25	1	19.95
SQ2.15.50	±15	± 50	0.25	0.25	1	28.95
P741-5005S	5	500	0.20	0.20	2	$29.95
P741-1012	±12	±100	0.20	0.20	2	39.95
P741-1015	±15	±100	0.20	0.20	2	33.95
DPS1.5.1000	5	1000	0.50	0.50	3-B	$29.95
LCD1.5.500	5	500	0.20	0.20	3-A	$37.95
LCD1.5.1000	5	1000	0.20	0.20	3-B	49.95
LCD2.6.50	±6	± 50	0.20	0.20	3-A	43.00
LCD2.12.100	±12	±100	0.20	0.20	3-A	45.00
LCD2.12.200	±12	±200	0.20	0.20	3-B	59.95
LCD2.15.25	±15	± 25	0.20	0.20	3-A	19.95
LCD2.15.50	±15	± 50	0.20	0.20	3-A	35.00
LCD2.15.100	±15	±100	0.20	0.20	3-A	45.00
LCD2.15.200	±15	±200	0.20	0.20	3-B	59.95

OPTIONS: See Page 11 For Details

Other Models Available Upon Request.

2.5 Item Wiring Records and Parts Lists

The wiring lists and parts for the CGE-PLATO Interface Items, listed in Section 2.0 above, are reproduced on the following pages.

CGE LOGIC BRD - FRONT — 1

Item Name — Item No.

Part: 1 44-Contact Vector Plugbord Receptacle Type R-644 ($2.62)

Date 1 March 74 By J.P.Neal

Connected Item				This	Item
Use	No.	Pin	Cable Wire	Term	Chip
GRD			Chassis	A	
-15	5	4	GN (Blk)	B	72741 4
NC				C	
NC				D	
NC				E	
NC				F	
NC				H	
NC				J	
NC				K	
NC				L	
+15	5	5	Red (Blu)	M	72741 7
CGE Ready	26	10	Red (Blk)	N	74123 C/12
$\overline{2^0}$	26	1	Ora (Blk)	P	7450 A/6
$\overline{2^1}$	26	2	Yel (Blk)	R	7450 B/8
$\overline{2^2}$	26	3	Blu (Blk)	S	7450 B/6
$\overline{2^3}$	26	4	Wh (Grn)	T	7450 C/8
2^4	26	5	Wh (Blk)	U	7450 C/6
Test bit	26	7	Brn (Blk)	V	7404 A/12
D16	16	3	Red	W	LO2 C/12
D17	16	4	Ora	X	LO2 C/11
D18	16	5	Grn	Y	LO2 C/10
T30	4	N.O. 30	Red (Brn)	Z	LO5 D/6

Connected Item				This	Item
Use	No.	Pin	Cable Wire	Term	Chip
+5	5	1		1	
+5 Flt.	5	2	Red (Brn)	2	
	N.C.			3	
$\overline{DATA}$	25	1	Red (Blk)	4	7404 B/1
$\overline{CLK}$	25	2	Grn (Blk)	5	7404 B/3
$\overline{WE}$	25	3	Wh (Blk)	6	7404 A/1
NC				7	
NC				8	
NC				9	
NC				10	
NC				11	
NC				12	
OV. FLT.	5	3	Brn(Rd-Brn)	13	
CC5	4	POLE 36	Yel (Red)	14	74123 B/2
CC1	3	C	Red (Yel)	15	7411 C/12
+5				16	
D10	13	3	Blu	17	LO2 B/10
D11	13	4	Ora	18	LO2 B/9
D12	13	5	Grn	19	LO2 B/8
D13	13	6	Grey	20	LO2 B/7
D14	13	7	Blk	21	LO2 B/6
D15	13	8	Wh	22	LO2 B/5

CGE LOGIC BOARD - BACK

Item Name

2

Item No.

PART: 1 44-CONTACT VECTOR PLUGBORD RECEPTACLE TYPE R-644

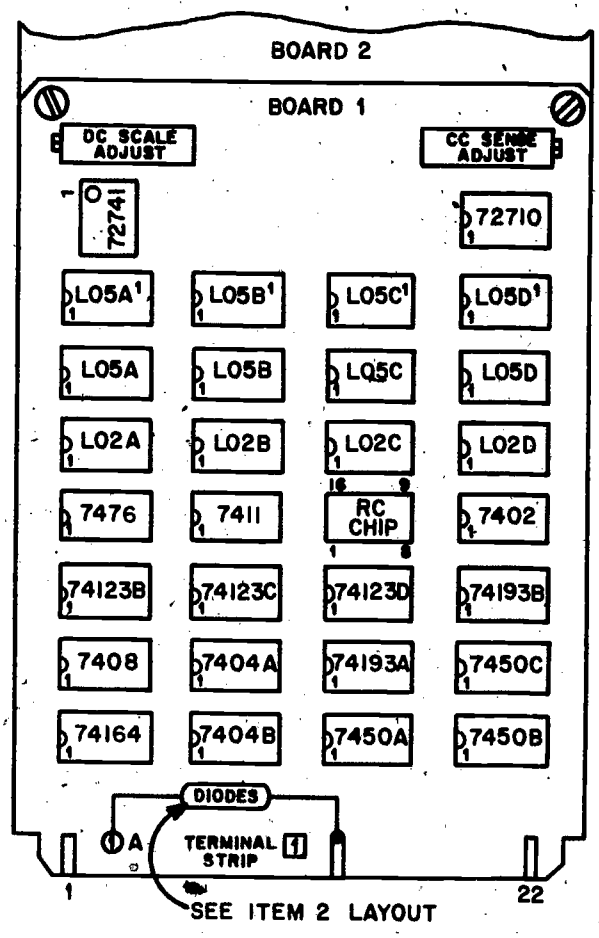
Date 4 DEC. 73 By JPN

Connected Item				This Item	
Use	No.	Pin	Cable Wire	Term	Chip
	NC			A	LO5A 12
D8	11	2	BRN	B	LO2B 12
D9	11	3	BLU	C	LO2B 11
D19	14	3	GRAY	D	LO2C 9
D20	14	4	WH	E	LO2C 8
D21	14	5	VIO	F	LO2C 7
D22	15	3	GRN	H	LO2C 6
T15	4	N.O. 15	YEL (RED)	J	LO5B 5
T16	4	N.O. 16	RED (YEL)	K	LO5C 12
T17	4	N.O. 17	RED (BLU)	L	LO5C 11
T18	4	N.O. 18	BLU (RED)	M	LO5C 10
T19	4	N.O. 19	WH (GRN)	N	LO5C 9
T20	4	N.O. 20	GRN (WH)	P	LO5C 8
T21	4	N.O. 21	RED (ORA)	R	LO5C 7
T22	4	N.O. 22	ORA (RED)	S	LO5C 6
T23	4	N.O. 23	BLU (GRN)	T	LO5C 5
T24	4	N.O. 24	GRN (XTR)	U	LO5D 12
T25	4	N.O. 25	BLU (BLK)	V	LO5D 11
T26	4	N.O. 26	BLK (BLU)	W	LO5D 10
T27	4	N.O. 27	YEL (BLK)	X	LO5D 9
T28	4	N.O. 28	BLK (YEL)	Y	LO5D 8
T29	4	N.O. 29	BRN (RED)	Z	LO5D 7

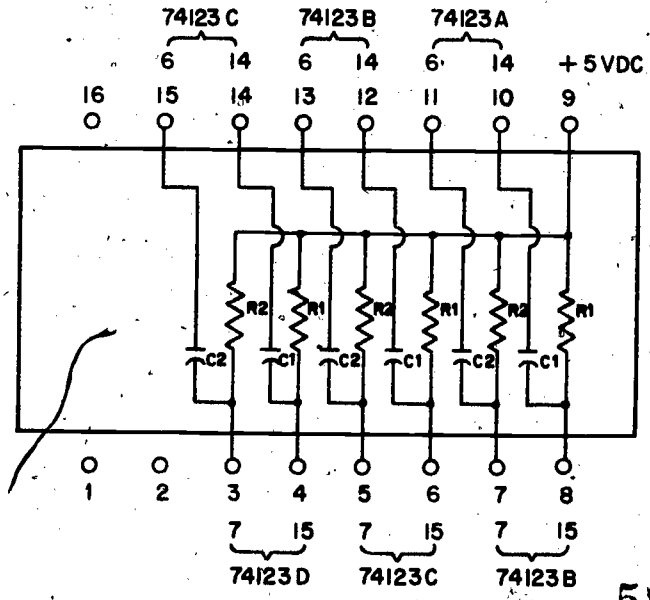
Connected Item				This Item	
Use	No.	Pin	Cable Wire	Term	Chip
	NC			1	LO5D 5
D1	12	3	WH	2	LO2A 11
D2	12	4	GRAY	3	LO2A 10
D3	12	5	RED/GN	4	LO2A 9
D4	12	6	RED/YEL	5	LO2A 8
D5	12	7	RED/BLK	6	LO2A 7
D6	12	8	TAN	7	LO2A 6
D7	12	12	YEL	8	LO2A 5
T1	4	N.O. 1	BRN (BLK)	9	LO5A 11
T2	4	N.O. 2	BLK (BRN)	10	LO5A 10
T3	4	N.O. 3	ORA (BLK)	11	LO5A 9
T4	4	N.O. 4	BLK (ORA)	12	LO5A 8
T5	4	N.O. 5	RED (WH)	13	LO5A 7
T6	4	N.O. 6	WH (RED)	14	LO5A 6
T7	4	N.O. 7	RED (BLK)	15	LO5A 5
T8	4	N.O. 8	BLK (RED)	16	LO5B 12
T9	4	N.O. 9	BLK (WH)	17	LO5B 11
T10	4	N.O. 10	WH (BLK)	18	LO5B 10
T11	4	N.O. 11	GRN (BLK)	19	LO5B 9
T12	4	N.O. 12	BLK (GRN)	20	LO5B 8
T13	4	N.O. 13	RED (GRN)	21	LO5B 7
T14	4	N.O. 14	GRN (RED)	22	LO5B 6

PARTS LAYOUT
CHIP SIDE

PART: 1 4 1/2" X 6 1/2" Vector 838 WE-IGN IC Board
30 16 pin D.I.P. sockets
2 Adjustable POT.



CHIP ELEMENTS



Chip side of RC socket

	R1	C1	R2	C2
74123B	10k	6.8μF	10k	.01μF
74123C	10k	.01μF	10k	.01μF
74123D	22k	.01μF	22k	6.8μF

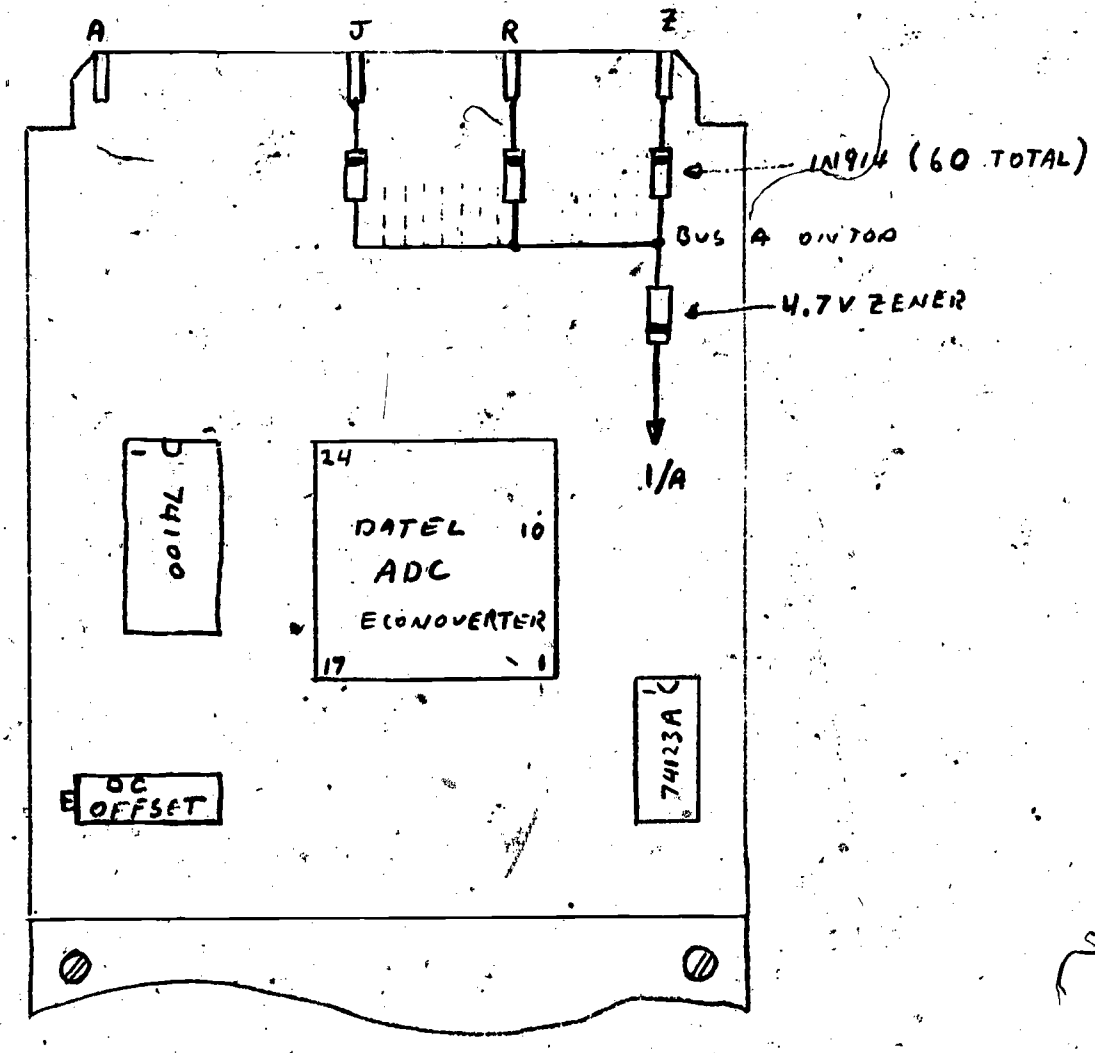
G. FRANK

PARTS LAYOUT

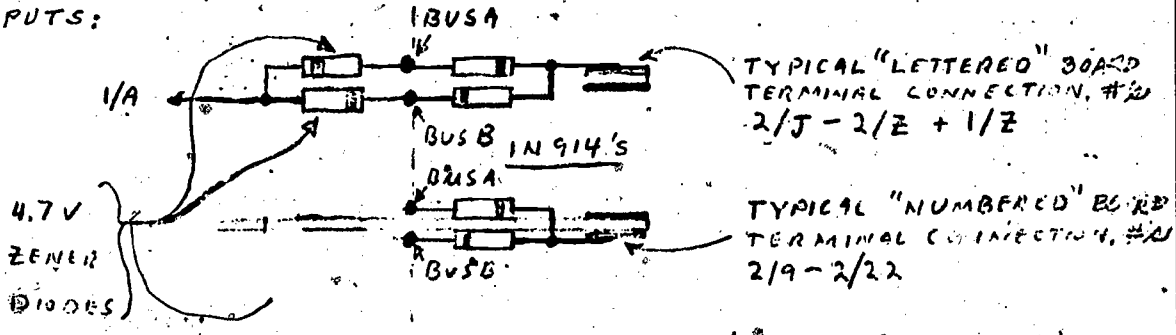
ITEM 2

29 NOV 73

CHIP SIDE



: OVERVOLTAGE PROTECTION FOR I/O INPUTS:



2 TOTAL

IN914's: 60 TOTAL (2 PER CC TERMINAL)

RELAY DRIVER BOARD — Item Name

3 — Item No.

Date 4 DEC. 73 By JPN

Connected Item				This Item	
Use	No.	Pin	Cable Wire	Term	Chip
24V AC	5	8		A	
CC2 24V	12 13A	14 8	14/8 15/8 16/8	B	
CC1 5V	1	15	RED (YEL)	C	
T1	4	POLE 1	RED	D	
T2	4	POLE 2	WH	E	
T3	4	POLE 3	BLK/WH	F	
T4	4	POLE 4	BLU/BLK	H	
T5	4	POLE 5	ORA/BLK	J	
T6	4	POLE 6	GRN/WH	K	
T7	4	POLE 7	GRN/BLK	L	
T8	4	POLE 8	RED/WH	M	
T9	4	POLE 9	BLU/WH	N	
T10	4	POLE 10	GRN	P	
T11	4	POLE 11	RED/BLK	R	
T12	4	POLE 12	WH/BLK	S	
T13	4	POLE 13	BLU	T	
T14	4	POLE 14	BLK	U	
T15	4	POLE 15	OR	V	
				W	
				X	
CONTROLLED GRD	4	COIL 2	RED (BLK)	Y	
CC LATCH	4	POLE 31	BLK (RED)	Z	

Connected Item				This Item	
Use	No.	Pin	Cable Wire	Term	Chip
24V AC	5	7		1	
GND				2	
CC1 24V	12	13	BLU	3	
T1	17	1	PINK	4	
T2	17	2	WH	5	
T3	17	3	GRAY	6	
T4	17	4	VIO	7	
T5	17	5	BLK	8	
T6	17	6	YEL	9	
T7	17	7	BRN	10	
T8	17	8	BLU	11	
T9	17	9	TAN	12	
T10	17	10	GRN	13	
T11	17	11	GRN/RED	14	
T12	17	12	YEL/RED	15	
				16	
T14	17	14	BLK/RED	17	
T15	17	15	ORA	18	
CC3 24V	13A	9	SLATE	19	
	NC			20	
	NC			21	
	NC			22	

Item 3
15 October 1973

RELAY DRIVER BOARD PARTS LIST

1 Vector No. 3662 6.5" x 4.5" Plugboard

1 Vector R644 PC Receptacle

1 RCA 2N2270 Transistor

1 Int. Rect. IR 18DB2A F.W. Rectifier

1 500 Ω, 1 watt, 5% resistor

1 Int. Rect. 1N270 Diode

1 3 mF capacitor

1 11.5/25.2 V transformer

1 Sigma 62R2-24 V Relay

5 Sigma 62R4-24 V Relay

1 Sigma AD-22 Relay Socket

5 Sigma AD-24 Relay Socket

1 ON-OFF power switch with pilot lamp

CC RELAY - POLES & COIL

Item Name

4

Item No.

SHEET 1 OF 3

Date 1 MAR 74 By JPN

Connected Item				This Item	
Use	No.	Pin	Cable Wire	Term	
T23	13A	5	BLU	23	
T24	13A	7	VIO	24	
T25	16	7	WH	25	
T26	16	6	BRN	26	
T27	14	6	RED	27	
T28	14	7	BLK	28	
T29	15	6	BLK	29	
T30	15	7	RED	30	
CC LATCH	3	Z	BLK (RED)	31	
				32	
				33	
				34	
				35	
CC5	1	14	YEL	36	

RELAY COIL					
CC4	16	9	GRN	1	HEP170
CNTRL GRD	3	Y	RED (BLK)	2	

Connected Item				This Item	
Use	No.	Pin	Cable Wire	Term	
T1	3	D	RED	1	
T2	3	E	WH	2	
T3	3	F	BLK/WH	3	
T4	3	H	BLU/BLK	4	
T5	3	J	ORA/BLK	5	
T6	3	K	GRN/WH	6	
T7	3	L	GRN/BLK	7	
T8	3	M	RED/WH	8	
T9	3	N	BLU/WH	9	
T10	3	P	GRN	10	
T11	3	R	RED/BLK	11	
T12	3	S	WH/BLK	12	
T13	3	T	BLU	13	
T14	3	U	BLK	14	
T15	3	V	OR	15	
T16	12	9	YEL	16	
T17	12	10	GRAY	17	
T18	12	11	ORA	18	
T19	13A	1	WH	19	
T20	13A	2	GRN	20	
T21	13A	3	RED	21	
T22	13A	4	ORA	22	

CC RELAY - N.C. CONTACTS

Item Name

SEE NOTE BELOW

4

Item No.

SHEET 2 OF 3

Date 1 MAR 74 By JPN

Connected Item				This Item	
Use	No.	Pin	Cable Wire	Term	
	GRD		47Ω	23	
				24	
				25	
				26	
				27	
				28	
				29	
				30	
				31	
				32	
				33	
				34	
				35	
GRD	CHASSIS GRD			36	
				—	

Connected Item				This Item	
Use	No.	Pin	Cable Wire	Term	
	GRD		47Ω	1	
				2	
				3	
				4	
				5	
				6	
				7	
				8	
				9	
				10	
				11	
				12	
				13	
				14	
				15	
				16	
				17	
				18	
				19	
				20	
				21	
				22	

Each N.C. CONTACT No. 1-30 is connected through a 47Ω, ¼W. resistor to Chassis Ground.

CC RELAY - N.O. CONTACTS

Item Name

4

Item No.

SHEET 3 OF 3

Date 1 MAR 73 By JPN

Connected Item				This Item	
Use	No.	Pin	Cable Wire	Term	
T23	2	T	BLU (GRN)	23	
T24	2	U	GRN (XTR)	24	
T25	2	V	BLU (BLK)	25	
T26	2	W	BLK (BLU)	26	
T27	2	X	YEL (BLK)	27	
T28	2	Y	BLK (YEL)	28	
T29	2	Z	BRN (RED)	29	
T30	1	Z	RED (BRN)	30	
GND	CHASSIS GND			31	
				32	
				33	
				34	
				35	
+5V	1	1	BLU	36	

Connected Item				This Item	
Use	No.	Pin	Cable Wire	Term	
T1	2	9	BRN (BLK)	1	
T2	2	10	BLK (BRN)	2	
T3	2	11	ORA (BLK)	3	
T4	2	12	BLK (ORA)	4	
T5	2	13	RED (WH)	5	
T6	2	14	WH (RED)	6	
T7	2	15	RED (BLK)	7	
T8	2	16	BLK (RED)	8	
T9	2	17	BLK (WH)	9	
T10	2	18	WH (BLK)	10	
T11	2	19	GRN (BLK)	11	
T12	2	20	BLK (GRN)	12	
T13	2	21	RED (GRN)	13	
T14	2	22	GRN (RED)	14	
T15	2	J	YEL (RED)	15	
T16	2	K	RED (YEL)	16	
T17	2	L	RED (BLU)	17	
T18	2	M	BLU (RED)	18	
T19	2	N	WH (GRN)	19	
T20	2	P	GRN (WH)	20	
T21	2	R	RED (ORA)	21	
T22	2	S	ORA (RED)	22	

CC RELAY PARTS LIST

1 36PDT T-Bar Type 801 Electronic Controls No. 36C24

65 1 kΩ, 1/4 watt, 5% resistors (36 + 29)

CGE POWER SUPPLY ASSEMBLY

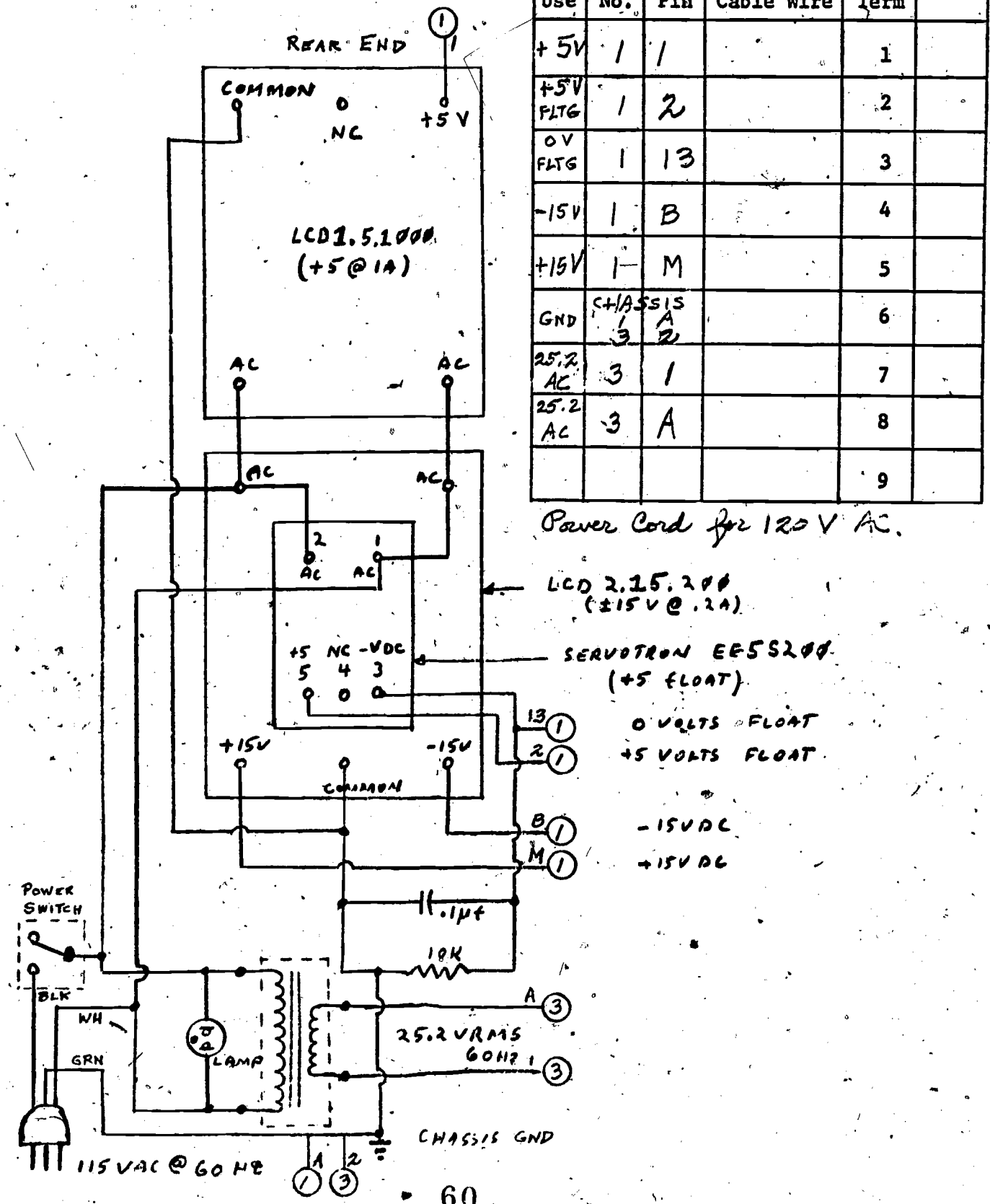
Item Name

5

Item No.

Date 10 DEC 73 By G.F.

Use	Connected Item No.	Pin	Cable Wire	This Item Term	
+ 5V	1	1		1	
+5V FLTG	1	2		2	
0V FLTG	1	13		3	
-15V	1	B		4	
+15V	1	M		5	
GND	CHASSIS 1 3	A 2		6	
25.2 AC	3	1		7	
25.2 AC	3	A		8	
				9	

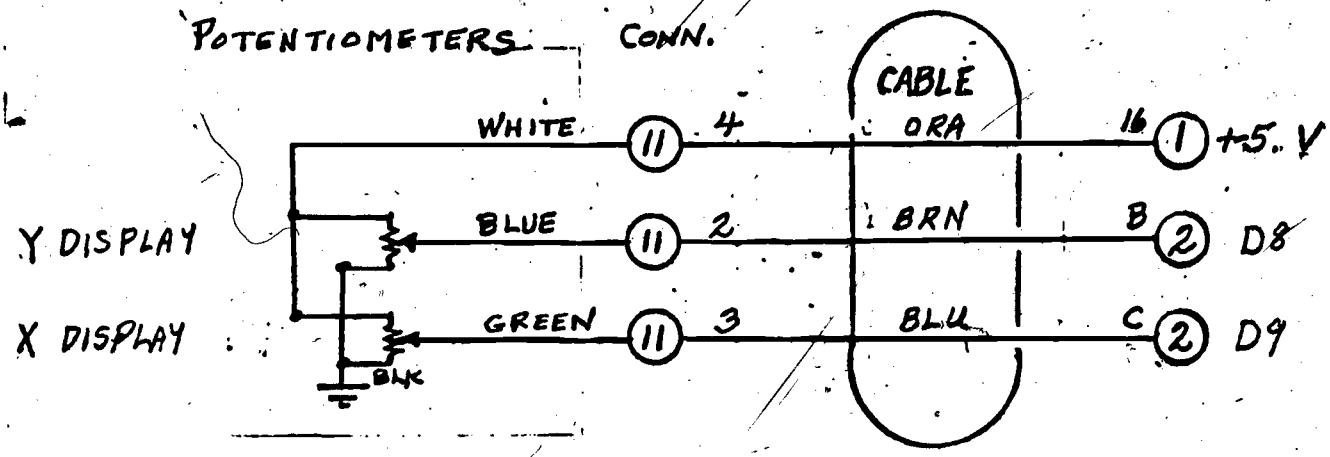


Power Cord for 120 V AC.

J.P.NEAL SCOPE - CRT ITEM 11*
7 NOV 73 (ANALAB 1120 DUAL TRACE SCOPE)

CGE MODIFICATION SCHEMATIC

DIAL SENSING:



PARTS:

1 AMPHENOL 17-20090 9-PIN PLUG
1 " 17-311-01 CABLE CLAMP

FOR SENSING "X DISPLAY FUNCTION" DIAL POSITION:

1 OAK SERIES F, 3-POSITION, 1-POLE, NONSHORTING TYPE ROTARY SWITCH WAFER:

2 1 kΩ, ½ W, 5% RESISTORS (BETWEEN CONTACTS)
1 20 kΩ, ½ W, TRIM RESISTOR (BETWEEN LAST CONTACT & +5.V)

FOR SENSING "Y DISPLAY FUNCTION" DIAL POSITION:

1 OAK SERIES F, 5-POSITION, 1-POLE, NONSHORTING TYPE ROTARY SWITCH WAFER.

4 1. kΩ ½ W, 5% RESISTORS (BETWEEN CONTACTS)
1 20 kΩ, ½ W, TRIM RESISTOR (BETWEEN LAST CONTACT & +5 V.)

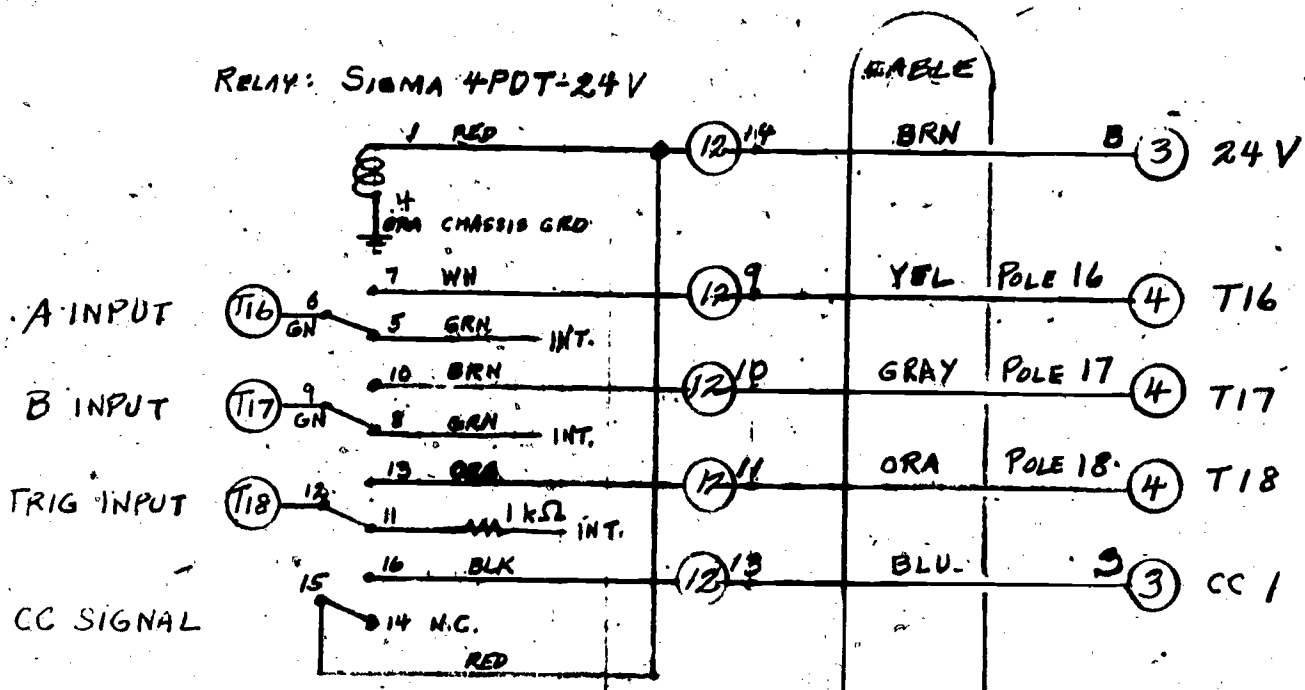
* Item Numbers 6-10 are unassigned.

JPNEAL
26 SEP 73

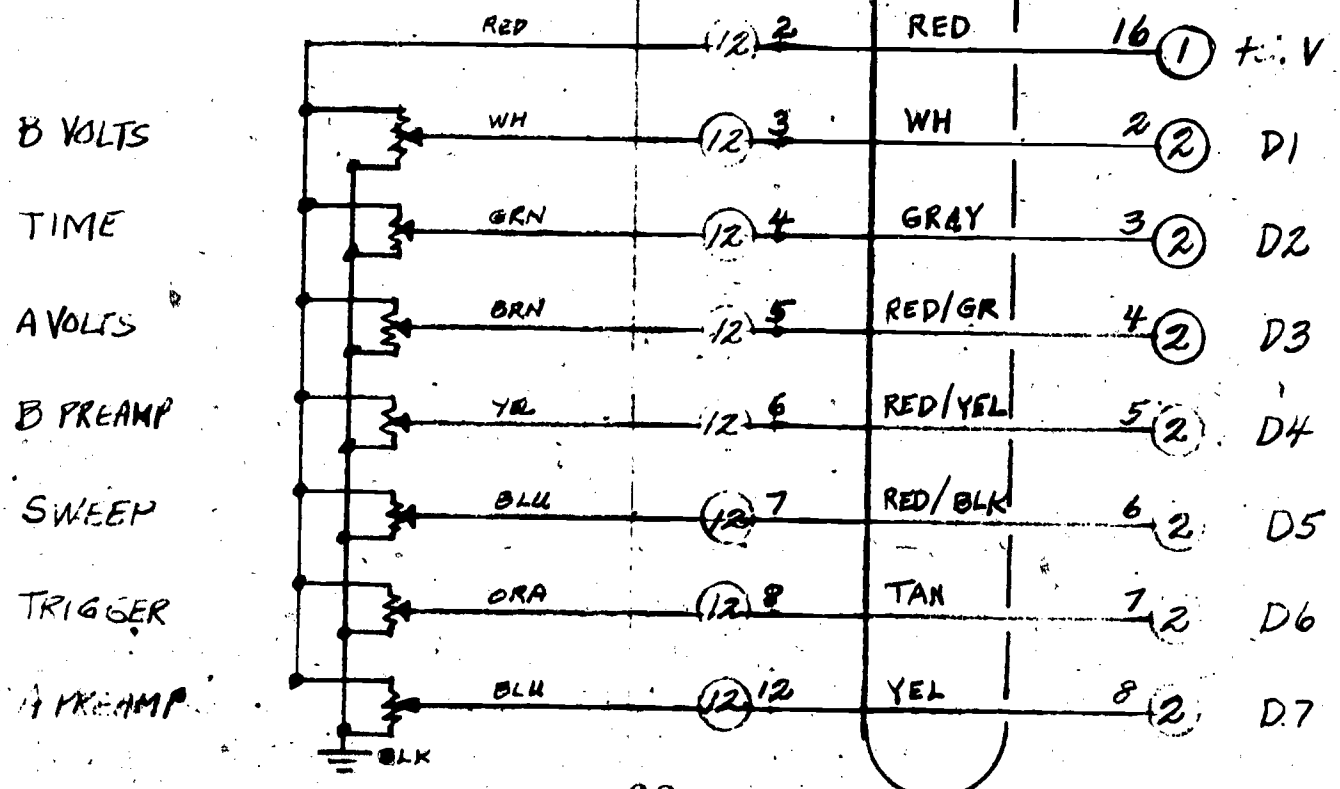
SCOPE - PLUGIN - ITEM 12
(ANALAB TYPE 700 PLUG-IN)

CGE MODIFICATION SCHEMATIC

CONNECTION SENSING:



DIAL SENSING:



ANALAB TYPE 700 PLUG-IN MODIFICATION PARTS

1 Amphenol 17-10150 15 pin Connector

Connection-Sensing Parts:

1 Cable #79 CC

1 Sigma 4PDT-24 V Relay

1 Sigma AD-24 Relay Socket

1 relay-mounting bracket

Dial-Sensing Parts:

1 Cable #79

1 Amphenol 17-10150 15 pin Connector

"B Volts" and "A Volts," each:

1 Centralab Series 4000, 17-position, 1-pole, shorting type rotary switch

16 1 kΩ, 1/4 watt, 5% resistors

1 5 kΩ, 1/4 watt trim resistor

"TIME":

1 Centralab Series 4000, 22-position, 1-pole, shorting type rotary switch

21 1 kΩ, 1/4 watt, 5% resistors

"A PREAMP" and "B PREAMP," each:

1 Oak Series F, 6-position, 1-pole, non-shorting type rotary switch

5 5.6 kΩ, 1/4 watt, 5% resistors

1 100 kΩ, 1/4 watt trim resistor

"TRIGGER SOURCE":

1 Oak Series F, 8-position, 1-pole non-shorting type rotary switch

7 5.6 kΩ, 1/4 watt, 5% resistors

1 100 kΩ, 1/4 watt trim resistor

"SWEEP MODE":

1 Oak Series F, 6-position, 1-pole non-shorting type rotary switch

5 5.6 kΩ, 1/4 watt, 5% resistors

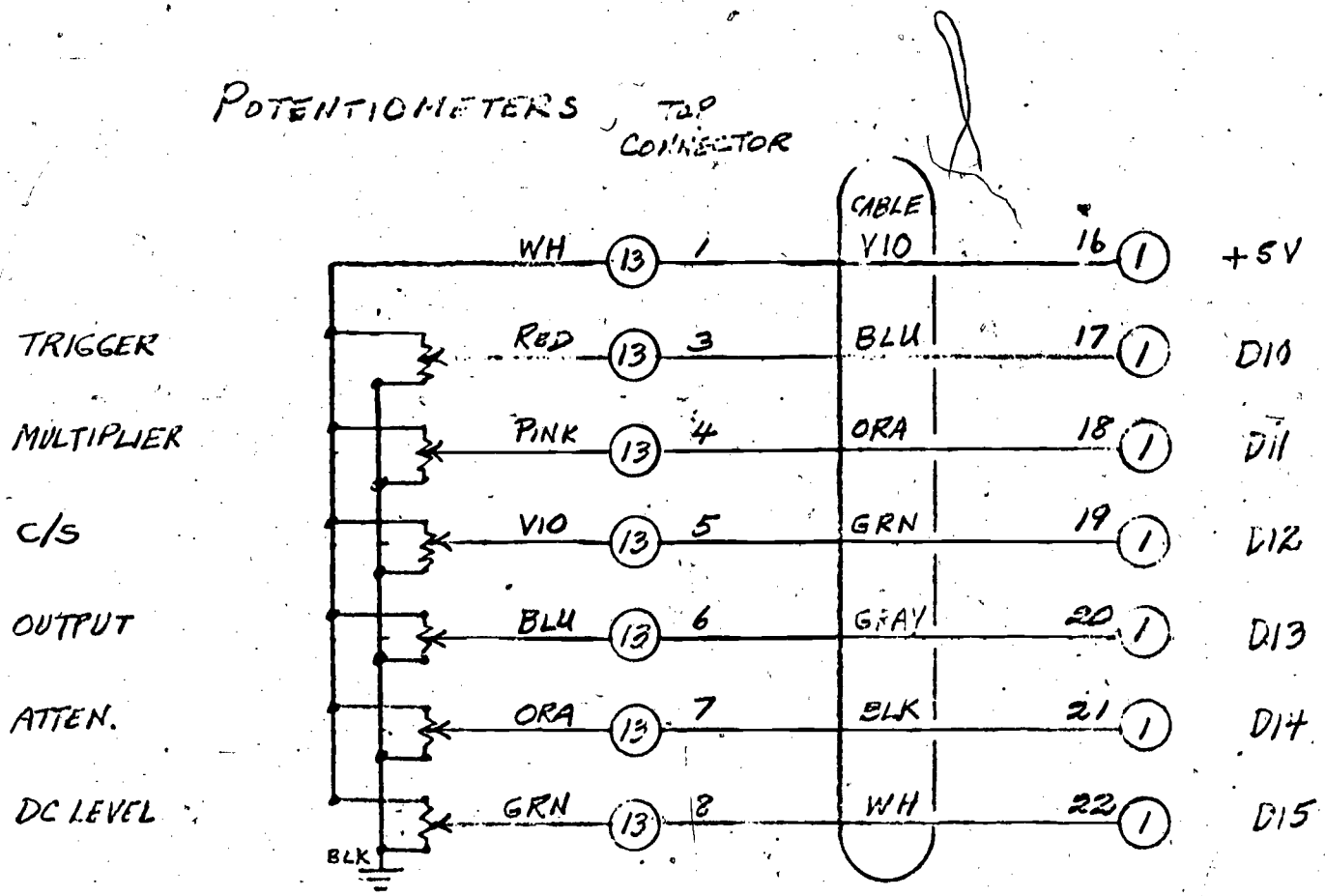
1 100 kΩ, 1/4 watt trim resistor

J.P. Neil
2 Oct 73

ITEM 13
FUNCTION GENERATOR I

CGE MODIFICATION SCHEMATIC

DIAL SENSING:



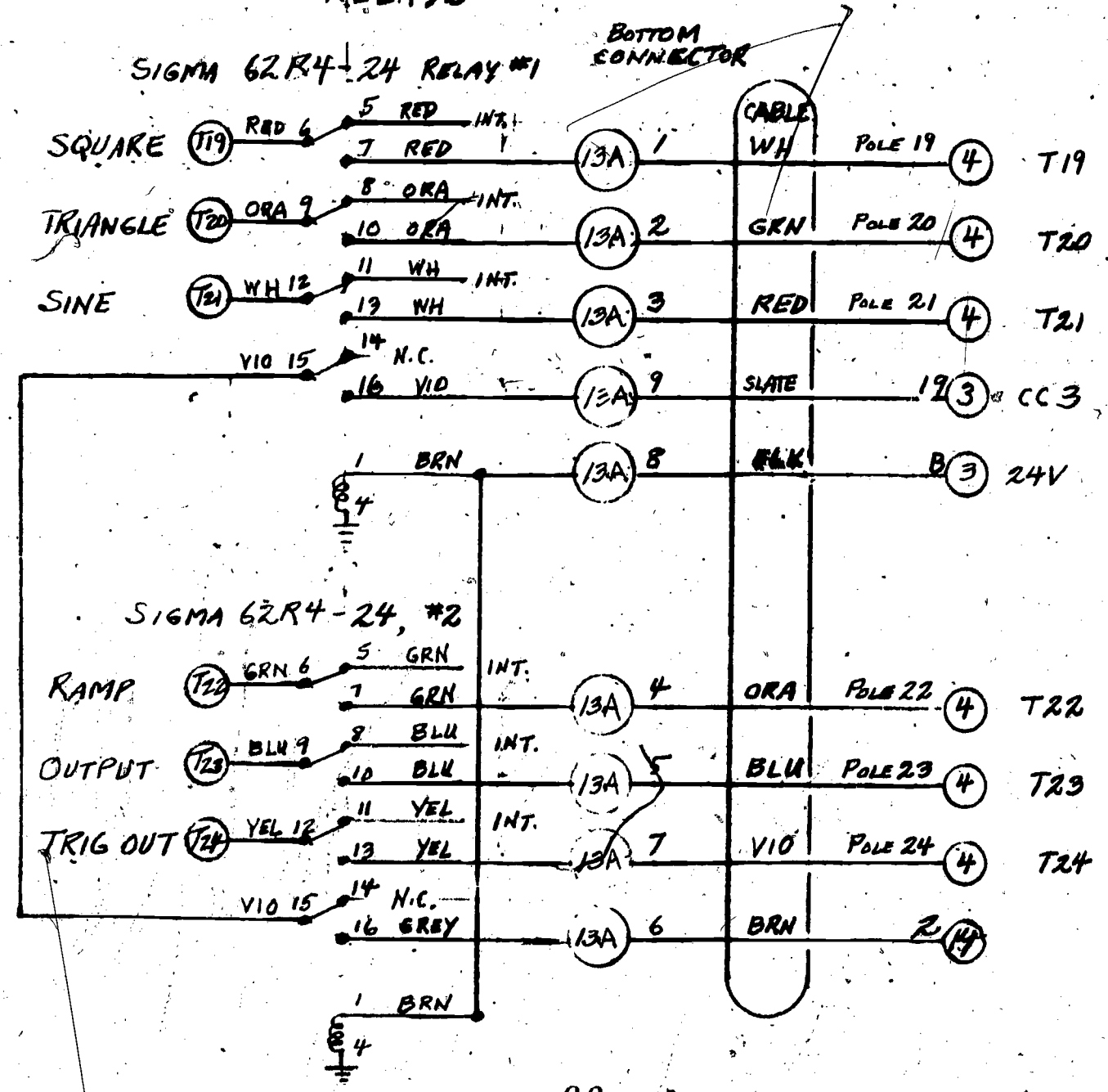
J. P. NEAL
26 SEP 73

ITEM 13A
EXACT 25/ FUNCTION GENERATOR II

CGE MODIFICATION SCHEMATIC

CONNECTION SENSING:

RELAYS



FUNCTION GENERATOR EXACT MODEL 251 MODIFICATION PARTS

Dial Sensing Parts:

1 Amphenol 17-20090 9-pin Connector (Top, Right)

For "TRIGGER":

1 PA-60 switch wafer (2 positions: ground and + 4.1 V)

For "MULTIPLIER":

1 PA-60 switch wafer

6 1 kΩ, 1/4 watt, 5% resistors

1 15 kΩ, 1/4 watt, 5% trim resistor

For "CYCLES/SEC":

1 3-sections IRS-CTC potentiometer: 30 kΩ, 20 kΩ, 25 kΩ trim resistor

For "OUTPUT":

1 PA-60 switch wafer: 3 1 kΩ and 1 18 kΩ trim resistors

For "ATTENUATOR":

1 Ohmit Dual 100 kΩ Potentiometer

For "DC LEVEL":

1 Mallory RU-54DT353 3-section Potentiometer: 1 FP14R, 1 US43, and 1 SL45

Connection-Sensing Parts:

1 Cable #81CC

1 Amphenol 17-20090 9-pin Connector (Bottom, Right)

2 Sigma 4PDT-24 V relays

2 Sigma AD-24 relay sockets

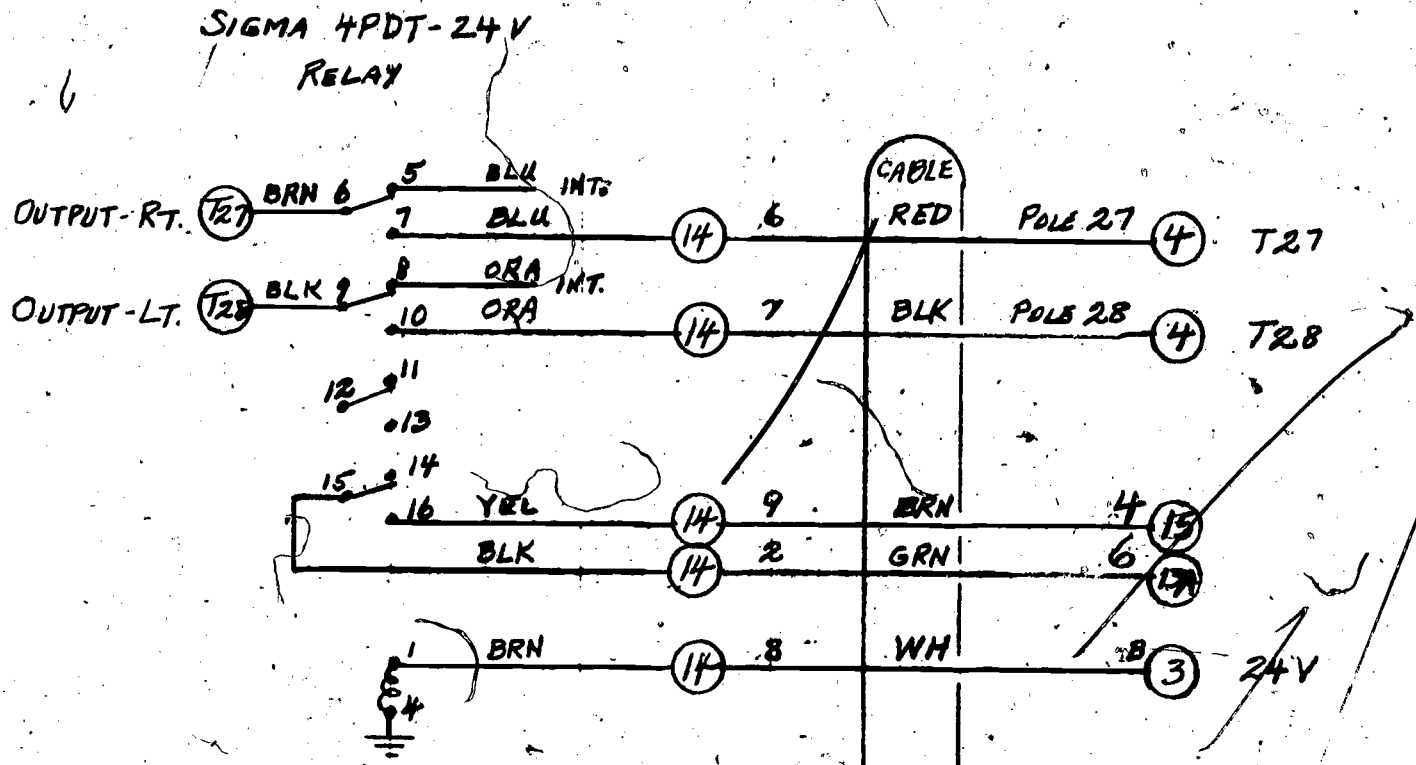
1 relay mounting bracket

ITEM 14

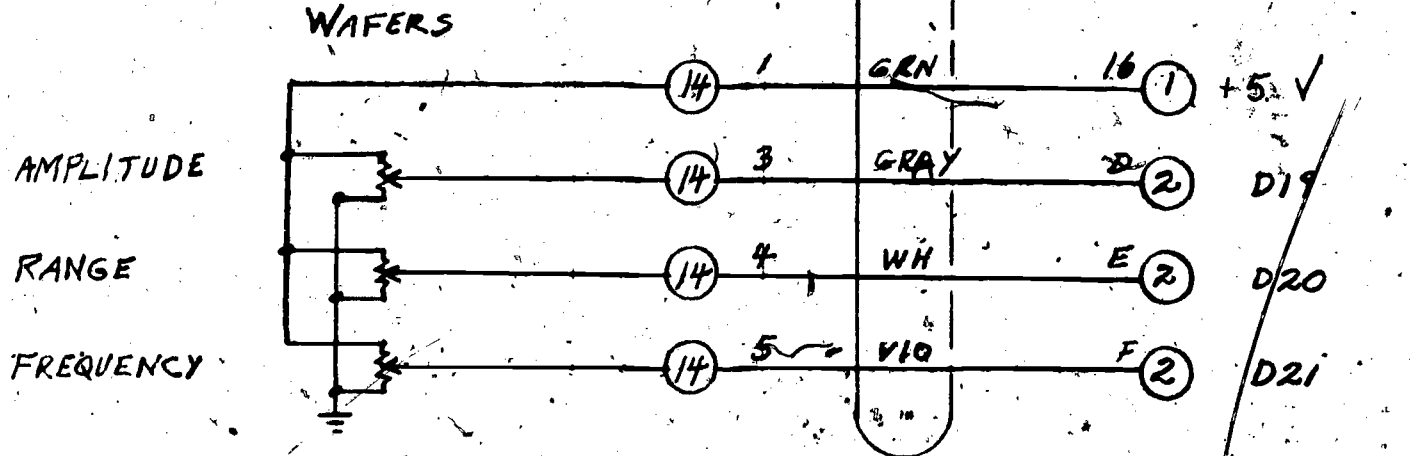
J.P. NEAL
2 OCT 73

HP 200 AB AUDIO OSCILLATOR
CGE MODIFICATION SCHEMATIC

CONNECTION SENSING:



DIAL SENSING



HP 200AB AUDIO OSCILLATOR MODIFICATION PARTS

1 Amphenol 17-20090 9-pin Connector

Connection-Sensing Parts:

1 Cable #83CC

1 Sigma 4PDT-24 V Relay

1 Sigma AD-24 Relay Socket

1 relay-mounting bracket

Dial-Position-Sensing Parts:

"AMPLITUDE," D19

1 Ohmite AB Dual 25 kΩ Potentiometer

"RANGE," D20

1 Centralab AD, 6-position, 1-pole shorting switch

3 1.5 kΩ, 1/4 watt, 5% resistors

1 100 kΩ trim resistor

"FREQUENCY," D21

1 Ohmite AB 25 kΩ Potentiometer

Dial	ID#	Equipment Pin #	Wire Color	Connector Pin
AMPLITUDE	D19	3	gray	D-19

POSITION LABEL	READING UP 0 → 100% VOLTAGE READING	READING DOWN 100 → 0% VOLTAGE READING	LETTER CODE
0.%	1.10	1.10	c
5.	1.11	1.15	c
10.	1.53	1.58	d
15.	1.92	1.99	f
20.	2.33	2.40	g
25.	2.66	2.73	h
30.	2.98	3.02	i
35.	3.26	3.38	j
40.	3.63	3.67	k
45.	3.95	4.02	l
50.	4.31	4.37	m
55.	4.67	4.78	o
60.	5.08	5.12	p
65.	5.43	5.45	q
70.	5.76	5.84	r
75.	6.10	6.12	s
80.	6.41	6.48	t
85.	6.79	6.84	u
90.	7.13	7.21	v
95.	7.44	7.53	v
100.	7.62	7.62	v

		Equipment Pin #	Wire Color	Position Label	Voltage Reading	Letter Code
RANGE	D20	4	white	x200	2.03	f
				x100	1.72	e
				x10	1.41	d
				x1	1.10	c

ITEM 15

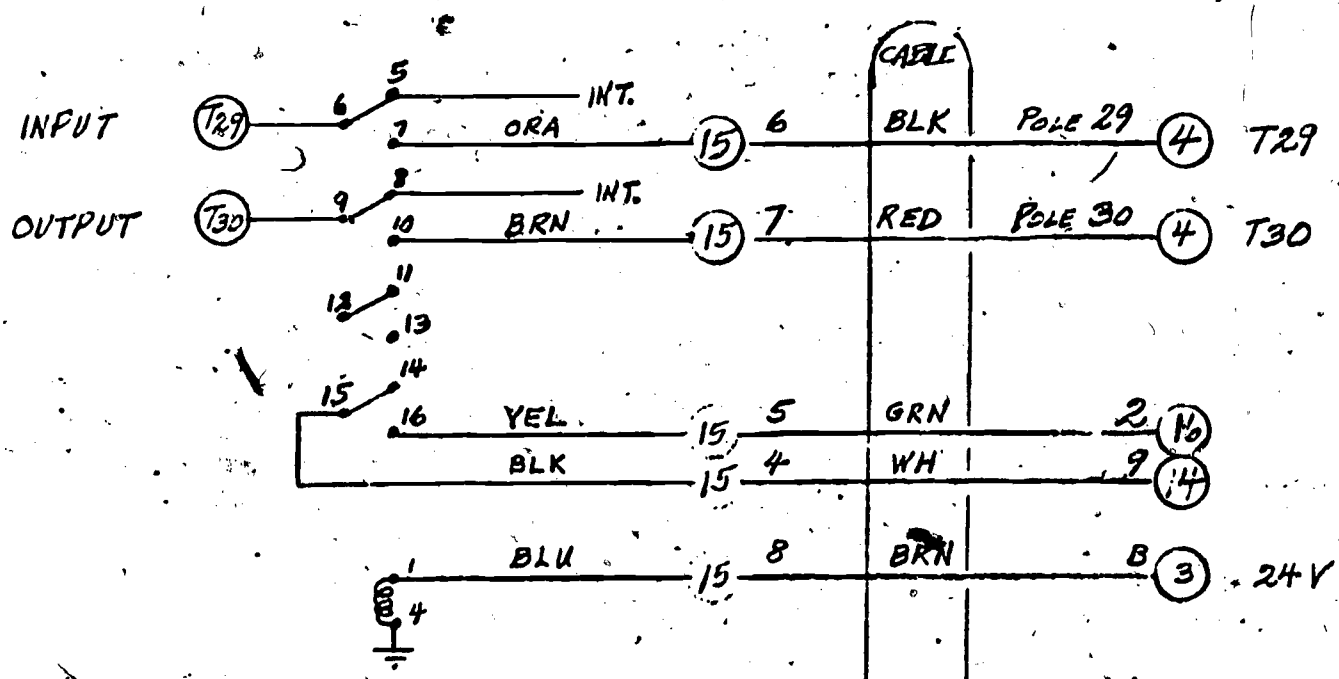
J.P. NEAL
3 OCT 73

HP400D VTVM

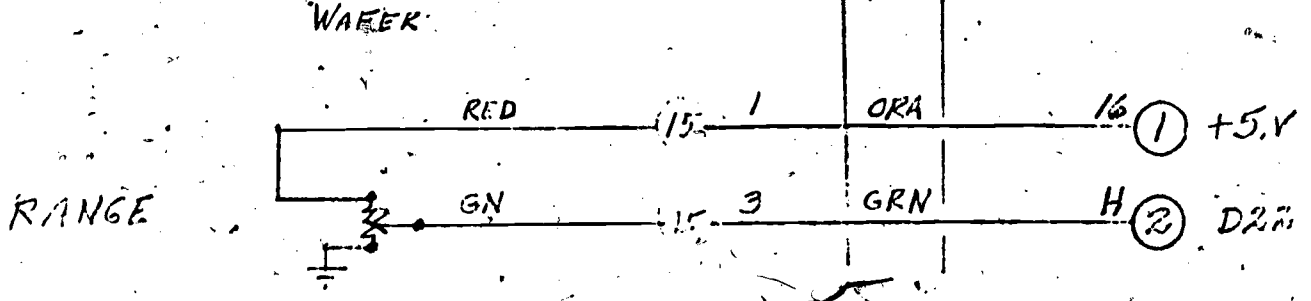
CGE MODIFICATION SCHEMATIC

CONNECTION SENSING:

SIGMA 4PDT-24V
RELAY



DIAL SENSING



VTVM HP 400D MODIFICATION PARTS.

1 Amphenol 17-20090 9-pin Connector

Connection-Sensing Parts:

1 Cable #84CC

1 Sigma 4PDT-24 Relay

1 Sigma AD-24 Relay Socket

1 relay-mounting bracket

Dial-Position-Sensing Parts:

"RANGE," D22

1 Centralab AD, 23-position, 1-pole shorting switch PA-4000

11 1 kΩ, 1/4 watt, 5% resistors

1 20 kΩ trim resistor

ITEM 16.

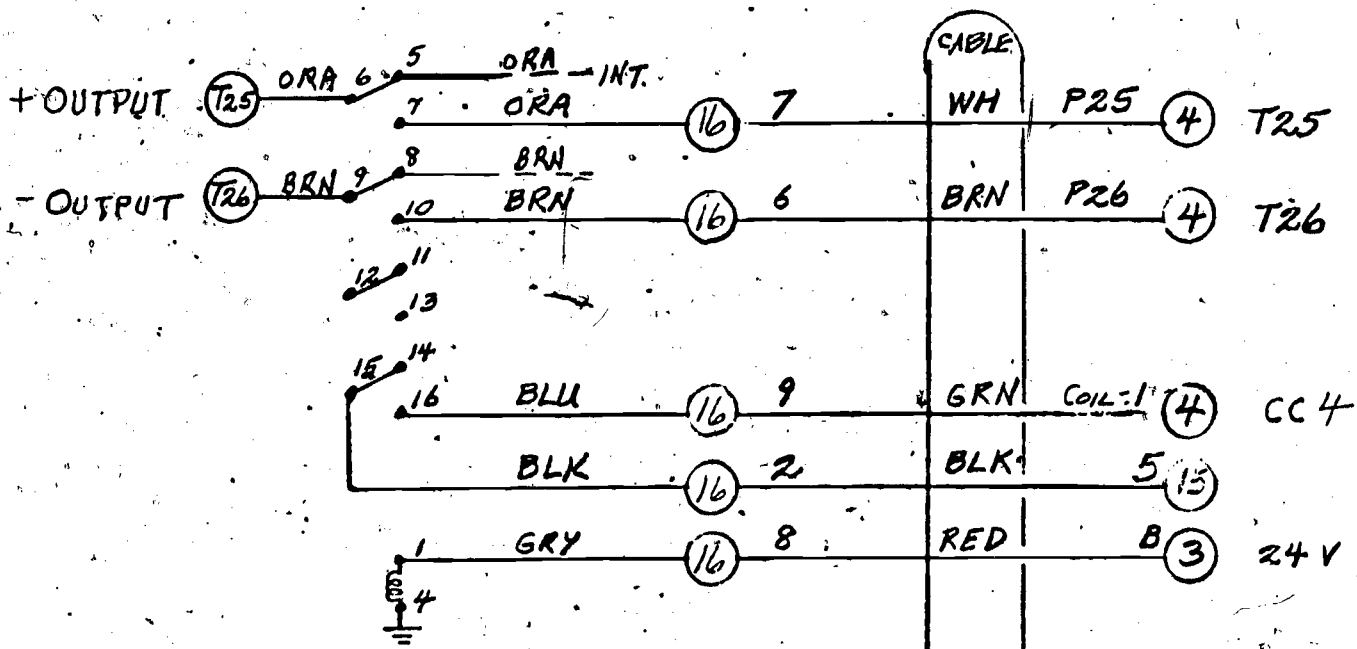
HARRISON 865B DC SUPPLY

J. P. NEAL
15 OCT 73.

CGE MODIFICATION SCHEMATIC

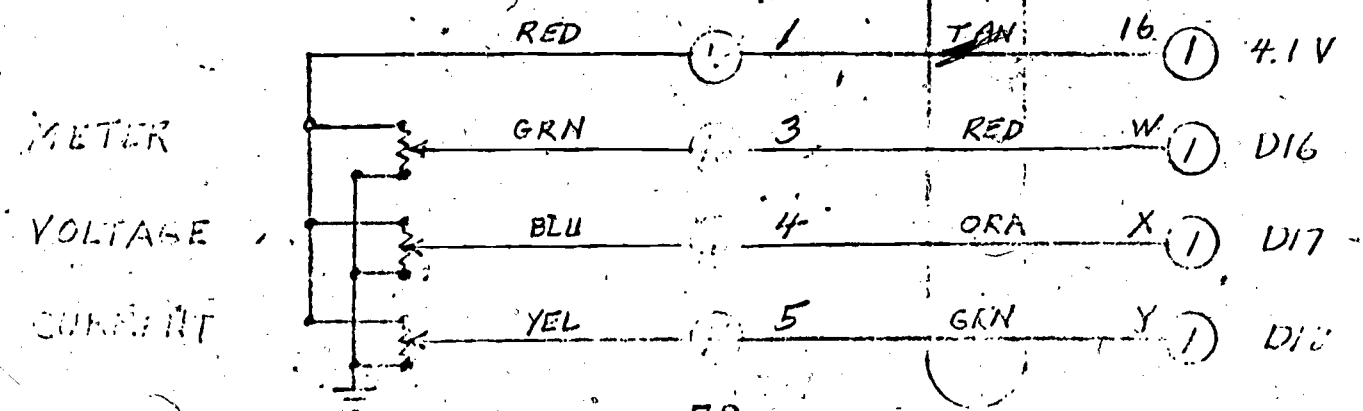
CONNECTION SENSING

SIGMA 4PDT-24
RELAY.



DIAL SENSING

WAFER



HARRISON 865B DC SUPPLY MODIFICATION PARTS

1 Amphenol 17-20090 9-pin Connector

Connection-Sensing Parts:

1 Cable #85CC

1 Sigma 4PDT-24 V Relay

1 Sigma AD-24 Relay Socket

1 relay-mounting bracket

Dial-Position-Sensing Parts:

"METER," D16

1 Centralab AD, 4-position, 1-pole shorting switch

3 1.5 kΩ, 1/4 watt, 5% resistors

1 100 kΩ trim resistor

"VOLTAGE," D17

1 Ohmite AB Dual 25 kΩ Potentiometer (1 is used for dial position sensor, the other is used for Power Supply voltage control)

"CURRENT," D18

1 Ohmite AB Dual 25 kΩ Potentiometer (1 is used for dial position sensor, the other is used for Power Supply current control)

5 NOV 73
JPN

CIRCUIT BOARD. SOCKET (ON INSTRUMENT-RACK PANEL) ITEM 17

PARTS LIST:

1 AMPHENOL # 17-10150 RECEPTACLE, #17-311-01 CABLE CLAMP, AND 17-529 LOCKING ASSEMBLY.

2' 15 #22 AWG STRANDED-WIRE CABLE.

WIRING DIAGRAM:

SENSORS	SOCKET PINS	CABLE COLOR CODE	CONNECTED ITEM
T1	(17) 1	PINK	4 (3)
T2	(17) 2	WH	5 (3)
T3	(17) 3	GRAY	6 (3)
T4	(17) 4	VIO	7 (3)
T5	(17) 5	BLK	8 (3)
T6	(17) 6	YEL	9 (3)
T7	(17) 7	BRN	10 (3)
T8	(17) 8	BLU	11 (3)
T9	(17) 9	TAN	12 (3)
T10	(17) 10	GRN	13 (3)
T11	(17) 11	GRN/RED	14 (3)
T12	(17) 12	YEL/RED	15 (3)
NOT USED	(17) 13	RED	16 (3)
T14	(17) 14	BLK/RED	17 (3)
T15	(17) 15	ORA	18 (3)

EXT OUT From PLATO

Item Name

25*

Item No.

Date 4 DEC 73 By JPN

Connected Item				This Item	
Use	No.	Pin	Cable Wire	Term	
DATA	1	4		1	
CLK	1	5		2	
WORD END	1	6		3	
GND	1	A		4	
"	1	A		5	
"	1	A		6	
				7	
				8	
				9	

PARTS:

6' of #22 AWG 3 Twisted-Pair Cable

1 Connector for J26 PLATO Console Socket

* Item Numbers 18-24 are unassigned.

EXT IN TO PLATO

Item Name

26

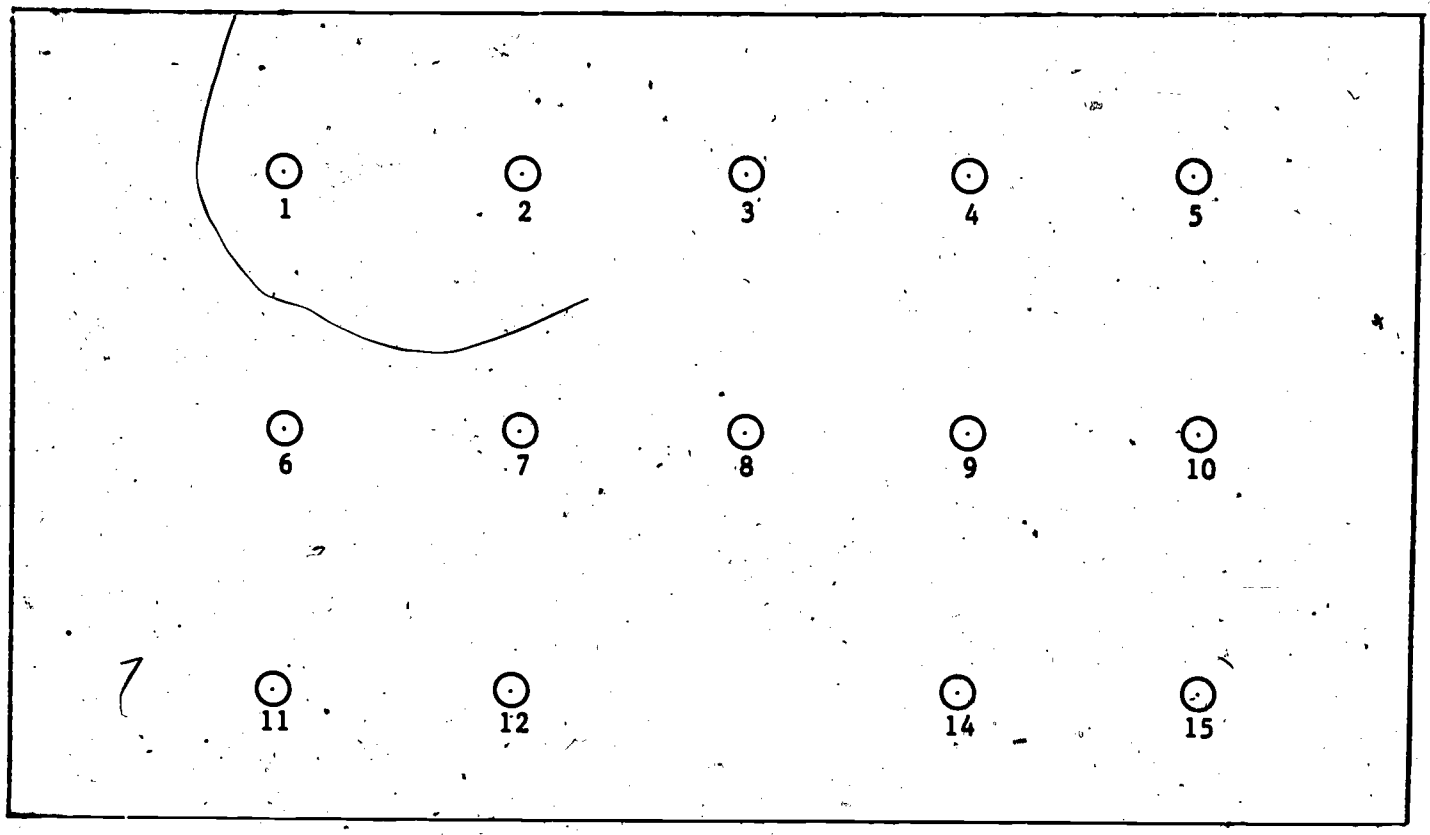
Item No.

Date 4 DEC 73 By JPN

Connected Item				This Item	
Use	No.	Pin	Cable Wire	Term	
GND	1	A	RED (BLU)	23	
	NC			24	

Connected Item				This Item	
Use	No.	Pin	Cable Wire	Term	
LSB $\overline{00}$	1	P	ORA (BLK)	1	
$\overline{01}$	1	R	YEL (BLK)	2	
$\overline{02}$	1	S	BLU (BLK)	3	
$\overline{03}$	1	T	GRN (BLK)	4	
MSB $\overline{04}$	1	U	WH (BLK)	5	
	NC			6	
TEST BIT	1	V	BRN (RED)	7	
	NC			8	
	NC			9	
CGE RDY	1	N	RED (BLK)	10	
	NC			11	
	NC			12	
GND	1	A	BLK (ORA)	13	
"	1	A	BLK (YEL)	14	
"	1	A	BLK (BLU)	15	
"	1	A	BLK (GRN)	16	
"	1	A	BLK (WH)	17	
"	1	A	RED (ORA)	18	
"	1	A	RED (BRN)	19	
"	1	A	RED (YEL)	20	
	NC			21	
GND	1	A	BLK (RED)	22	

PARTS: 6" of #22 AWG, 15 Twisted-pair cable (9 pair not used)
1 Connector for J26 PLATO Console Socket



Pin	Cable Wire Color	
1	YEL	T1
2	WH	T2
3	BLU	T3
4	RED	T4
5	BLK	T5
6	WH/GRN	T6
7	WH/BLU	T7
8	WH/BLK	T8

Pin	Cable Wire Color	
9	BRN	T9
10	TAN	T10
11	WH/RED	T11
12	WH/YEL	T12
13	--	
14	RED/BLK	T14
15	RED/GRN	T15

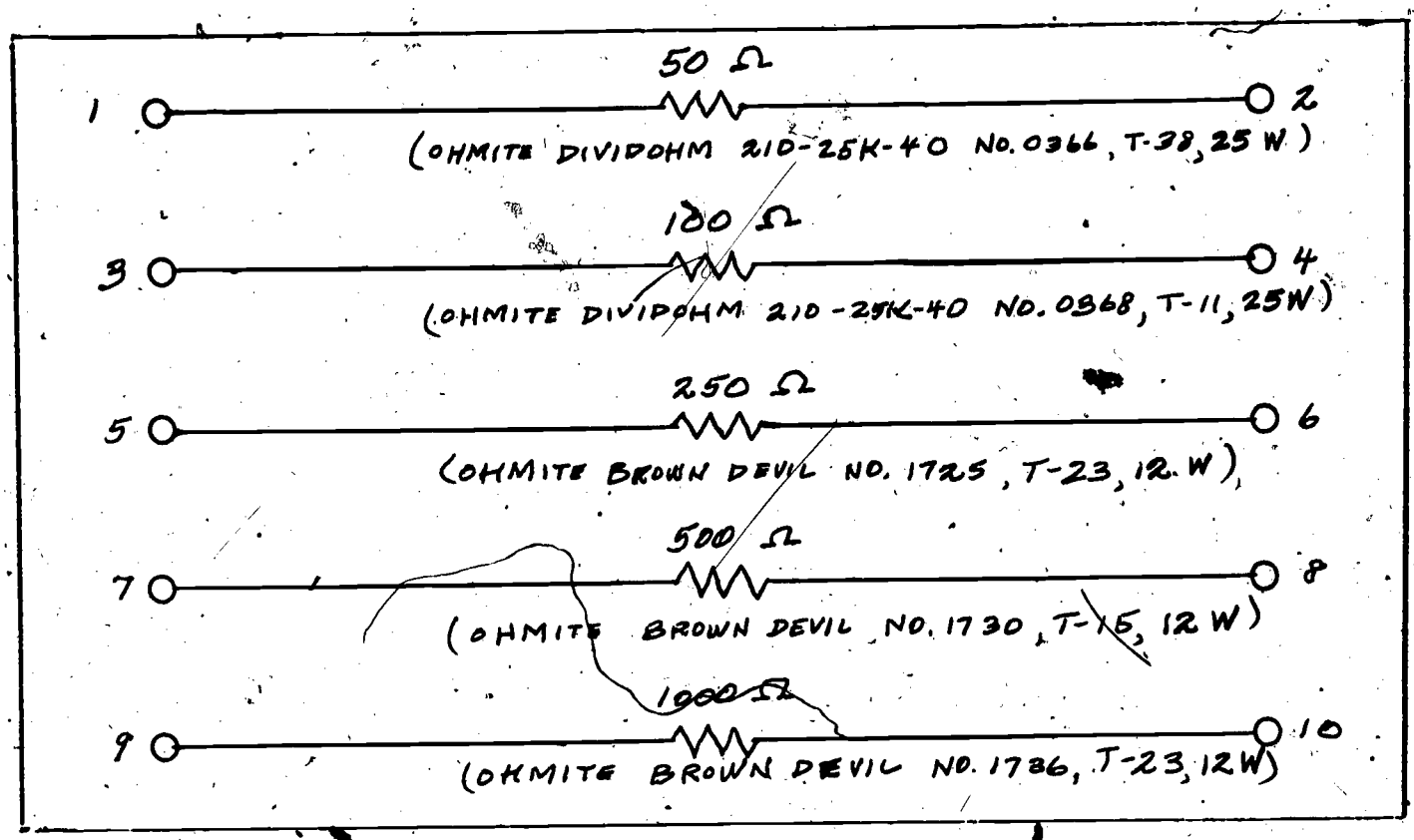
PARTS:

1 Micarta Board 8"L x 5"W x ¼"T
4 Brass spacer ¼" Dia. x 1"L with machine screw bumpers
14 Johnson 111-104 6-way green ginding posts
1 Amphenol 17-20150 Plug, 17-311-01 Calbe clamp
3'15 Pr. #22 AWG Cable

* Item Numbers 27-30 are unassigned.

By J.P. NEAL | ITEM NAME | ITEM NO. 32

Date 4 AUG 71 | RESISTOR BOARD | Sheet 1 of 1 sheets.



Cable Connector: Amphenol 17-311-01 with latches.

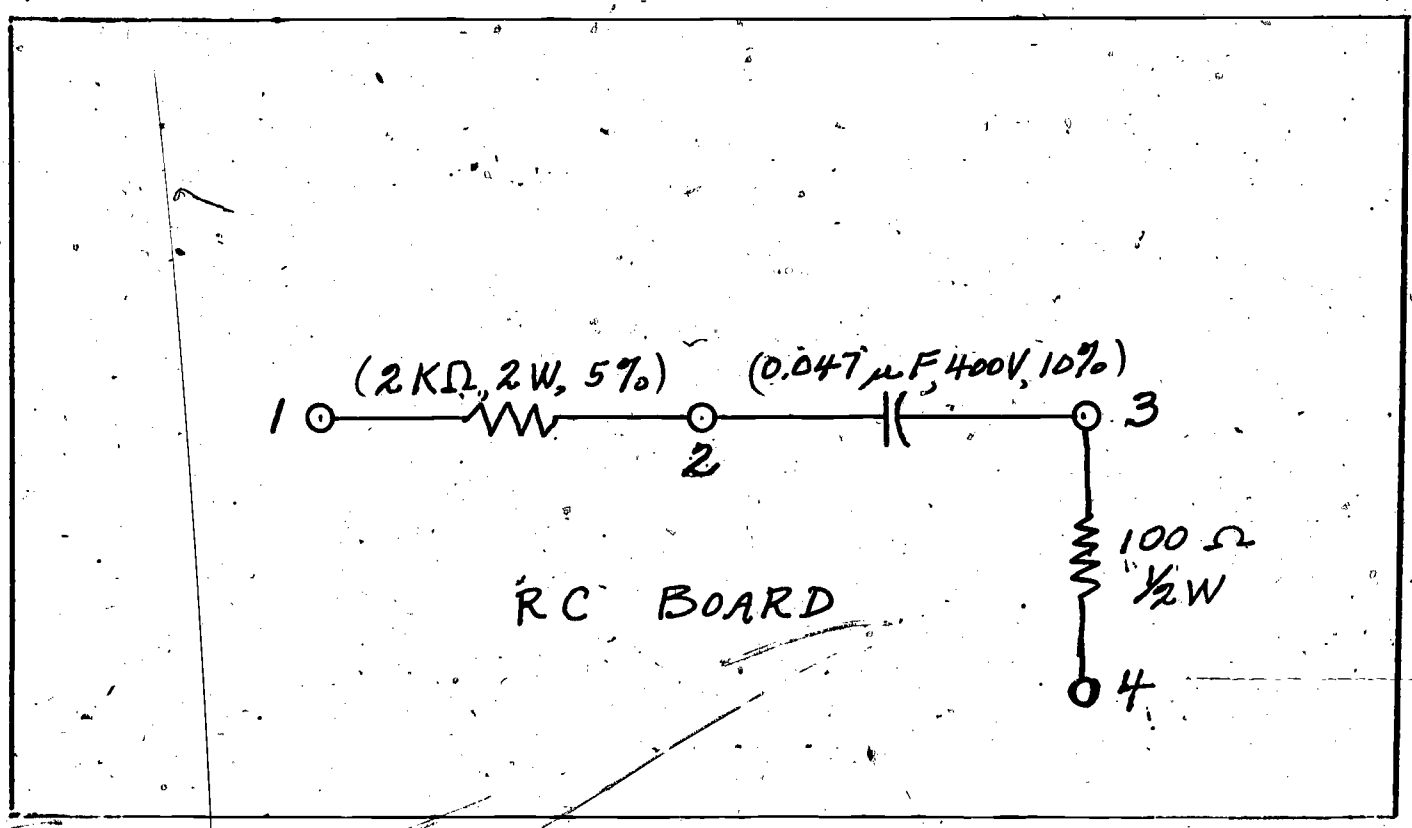
Pin	Cable Wire Color
1	BLACK / BLUE
2	BLACK / WHITE
3	BLUE
4	WHITE
5	BROWN
6	YELLOW
7	BLACK / GREEN
8	BLACK / RED

Pin	Cable Wire Color
9	GREEN
10	RED
11	
12	
13	
14	
15	

PARTS:
1 MICARTA BOARD 8"L x 5"W x ¼"T
4 BRASS SPACERS ¼" DIA. x 1"L W/BUMPERS
10 JACKS TYPE 274 J.
1 AMPHENOL 17-20150 PLUG & 17-311-01 CABLE CLAMP
3 15PR #22 AWG CABLE
5 OHMITE RESISTORS SHOWN ABOVE.

By J.P. NEAL | ITEM NAME | ITEM NO. 33

Date 2 APR 74 | RC BOARD | Sheet 1 of 1 sheets.



3' CABLE

Cable Connector: Amphenol 17-311-01 with latches: 4 TYPE 274 J JACKS

Pin	Cable Wire Color	
1	GREEN	T1
2	WHITE	T2
3	RED	T3
4	BROWN	T4
5		
6		
7		
8		

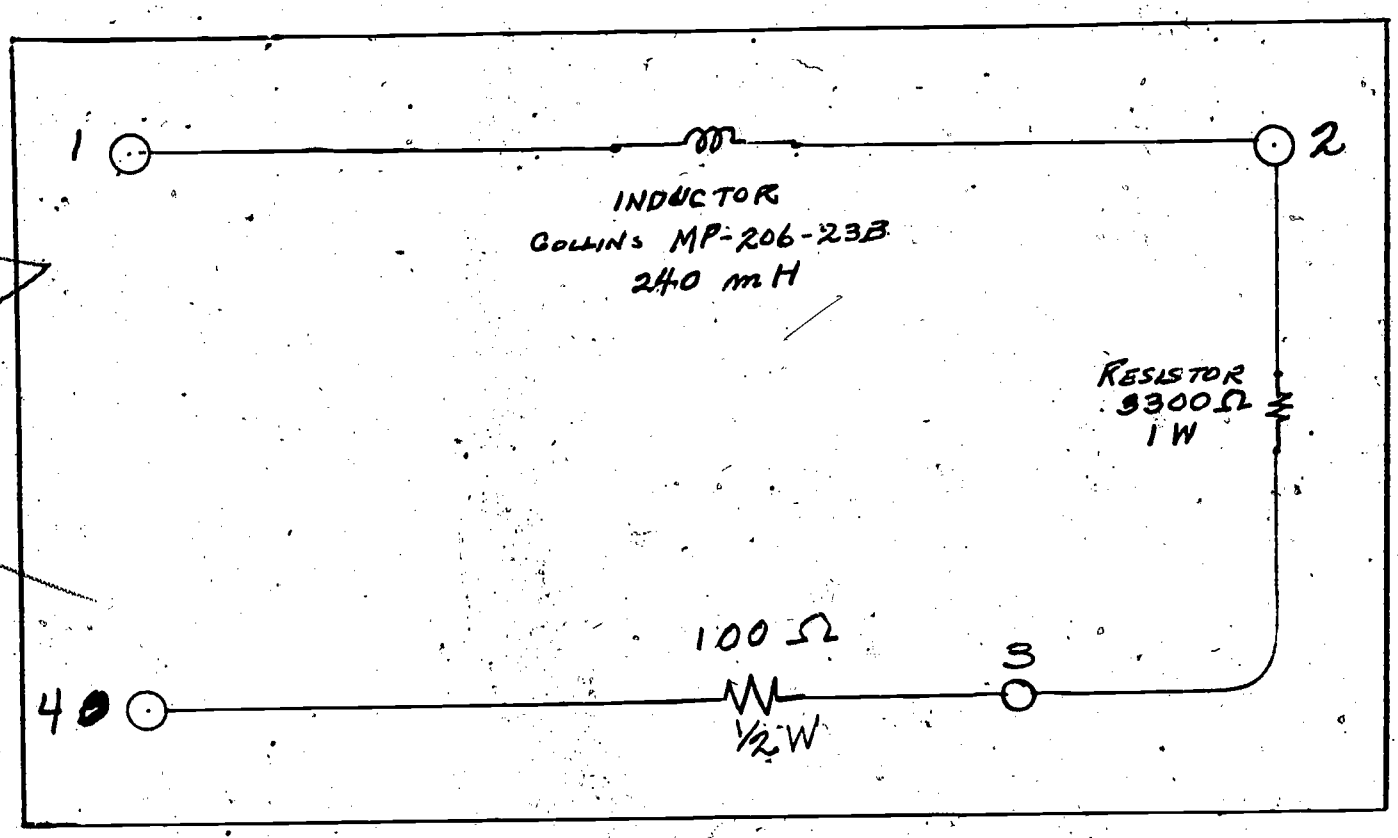
Pin	Cable Wire Color
9	
10	
11	
12	
13	
14	
15	

PARTS: SEE ABOVE.

CIRCUIT BOARD

By J.P.N. ITEM NO. 34

Date 2 APR 74 RL BOARD Sheet 1 of 1 sheets.



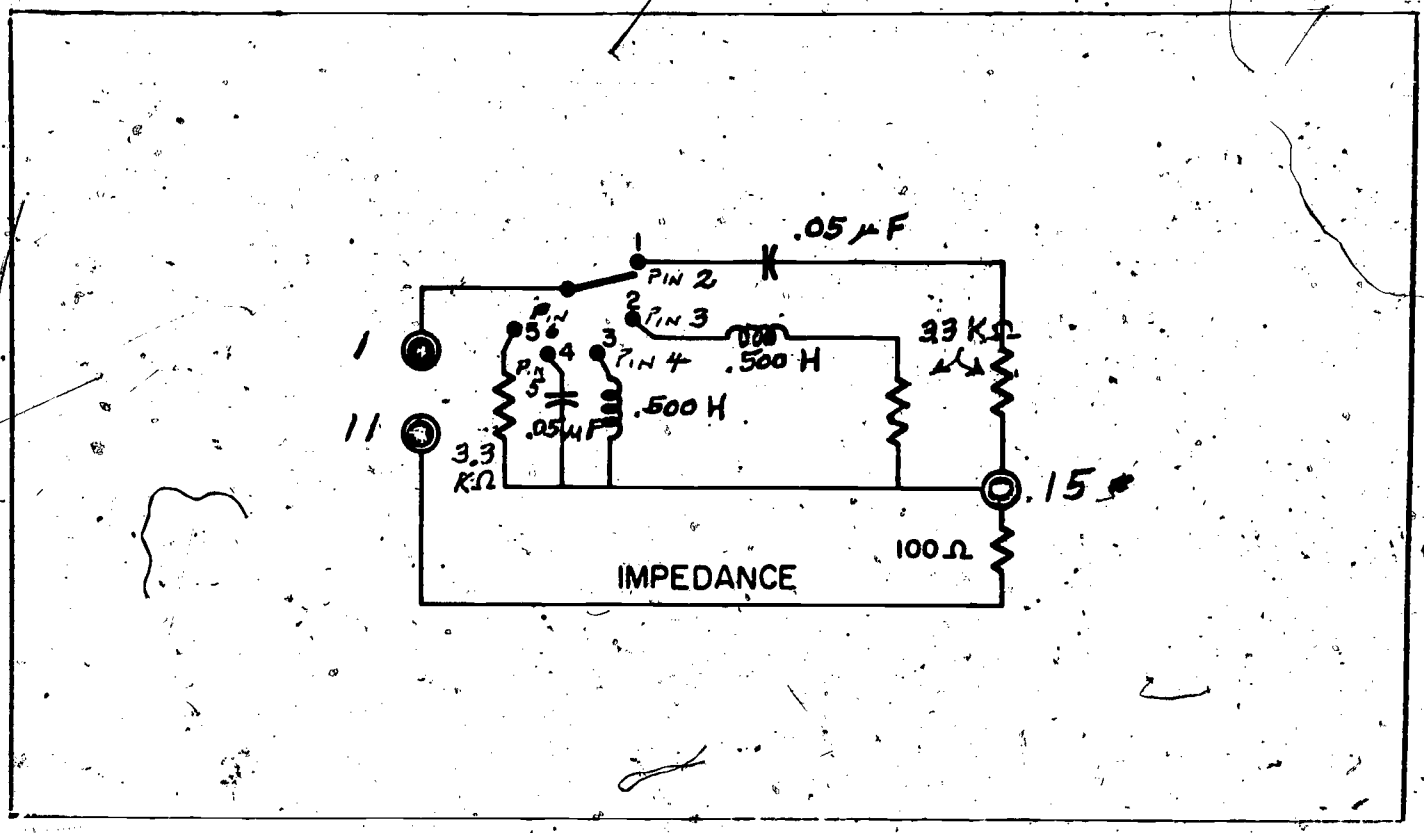
Pin	Cable Wire Color	
1	RED	T1
2	BROWN	T2
3	YELLOW	T3
4	BLUE	T4
5		
6		
7		
8		

Pin	Cable Wire Color
9	
10	
11	
12	
13	
14	
15	

PARTS: 1 MICARTA BOARD 8"L x 5"W x 1/4"T
4 MACHINE-SCREW BUMPERS AND 1/4"DIA x 1"L BRASS SPACERS
4 TYPE 274 J JACKS
1 RESISTOR, 3300Ω, 1W
1 INDUCTOR, COLLINS MP-206-23B, 0.240 H.

By V.P NEAL | ITEM NAME | ITEM NO. 35

Date 4 AUG 71 | IMPEDANCE BOARD | Sheet 1 of 1 sheets.



Cable Connector: Amphenol 17-311-01 with latches.

Pin	Cable Wire Color
1	RED
2	BROWN
3	YELLOW
4	BLUE
5	GREEN
6	WHITE
7	
8	

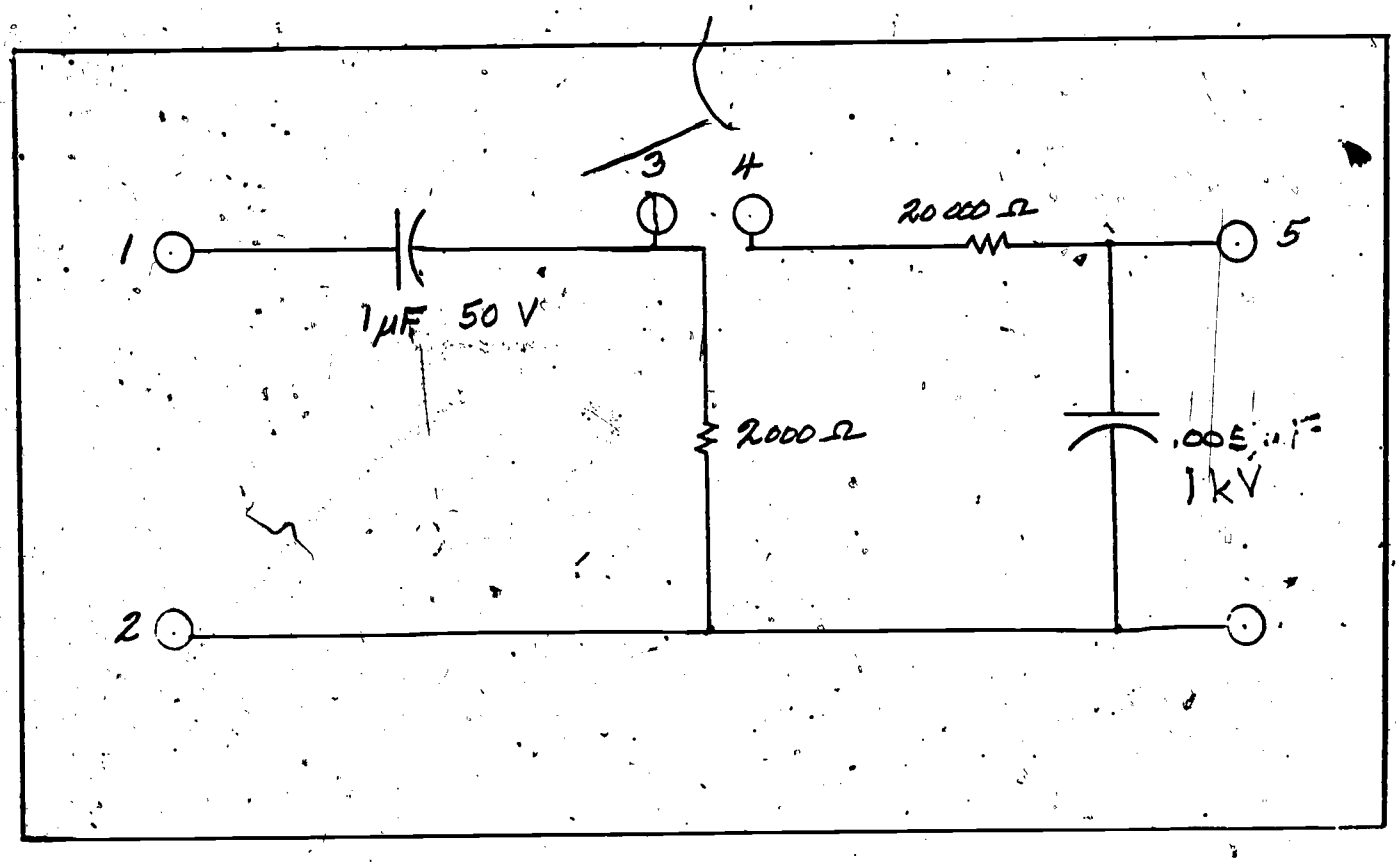
Pin	Cable Wire Color
9	
10	
11	BLACK / BROWN
12	
13	
14	
15	BLACK / RED

PARTS SEE ABOVE

CIRCUIT BOARD

By JPN ITEM NO. 36

Date 26 MAR 74 TWO PORT NETWORK Sheet 1 of 1 sheets.



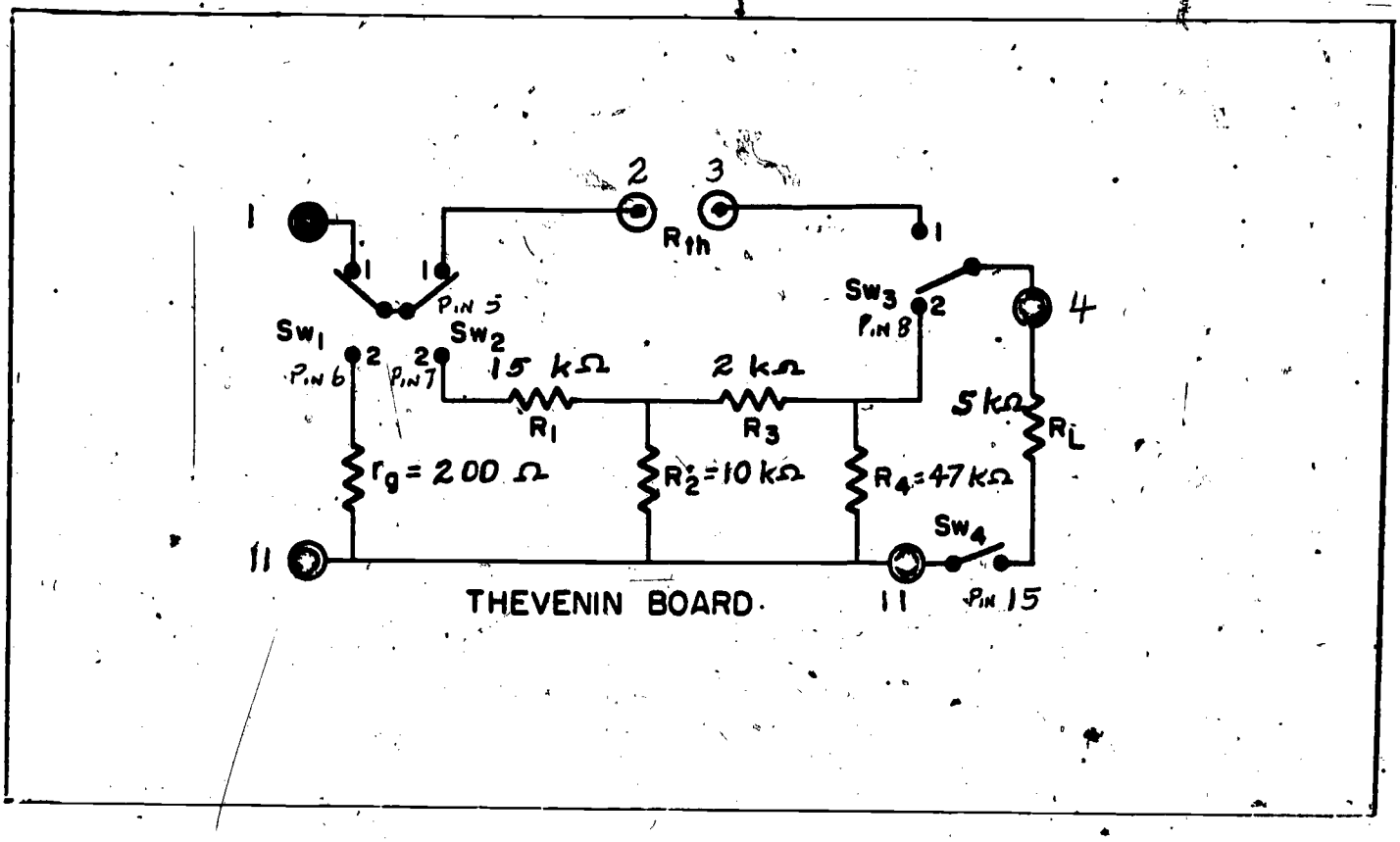
Pin	Cable Wire Color	
1	RED	T1
2	BROWN	T2
3	YELLOW	T3
4	BLUE	T4
5	GREEN	T5
6		
7		
8		

Pin	Cable Wire Color
9	
10	
11	
12	
13	
14	
15	

PARTS: 1 MICARTA BOARD 8"L x 5"W x ¼"T
4 MACHINE-SCREW BUMPERS AND ¼" DIA x 1"L BRASS SPACERS
6 TYPE 274 J JACKS
1 RESISTOR 2000 Ω, 2 W
1 RESISTOR 20,000 Ω, 1 W
1 CAPACITOR,
1 CAPACITOR,

By J. P. NEAL | ITEM NAME | ITEM NO. 37

Date 4 AUG 71 | THEVENIN BOARD | Sheet 1 of 1 sheets.



Cable Connector: Amphenol 17-311-01 with latches.

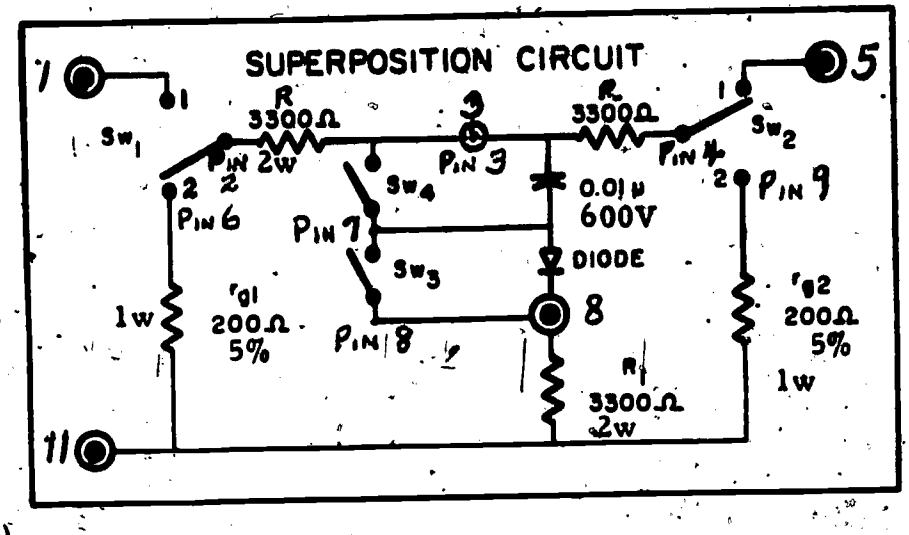
Pin	Cable Wire Color
1	RED
2	BROWN
3	YELLOW
4	BLUE
5	GREEN
6	WHITE
7	BLACK / YELLOW
8	BLACK / BLUE

Pin	Cable Wire Color
9	
10	
11	BLACK / BROWN
12	
13	
14	
15	BLACK / RED

PARTS SEE ABOVE

By J.P. Neal ITEM NAME ITEM NO. 38

Date 4 Aug 71 SUPERPOSITION BOARD Sheet 1 of 1 sheets.



Diode: IN6 47 or equivalent

Sw_3, Sw_4, SPST (2)

Sw_1, Sw_2, SPDT (2)

R, R_1, 3300Ω ±5%, 2w (3)

R_{g1}, R_{g2}, 200Ω ±5%, 1w

C, 0.01μf at 600V, tubular paper

Type 274J jacks (GR) (4)

Cable Connector: Amphenol 17-311-01 with latches.

Pin	Cable Wire Color
1	RED
2	BROWN
3	YELLOW
4	BLUE
5	GREEN
6	WHITE
7	BLACK / YELLOW
8	BLACK / BLUE

Pin	Cable Wire Color
9	BLACK / GREEN
10	
11	BLACK / BROWN
12	
13	
14	
15	

PARTS SEE ABOVE

CHAPTER 3 - OPERATION OF THE CGE-PLATO INTERFACE SYSTEM

3.0 Use of the PLATO EXT OUT Command

This operational description refers directly to the ten sheets of schematic diagrams in Section 2.3, p. 21-30. Signal flow should be followed on the schematic diagrams as the operation is described. A component number followed by a sheet number refers to one of the schematic diagram sheets.

(1) When an EXT Command is executed in a CGE-PLATO program, the EXT OUT data channel connector on the back side of the PLATO IV Console, Serial No. 324, delivers a fifteen-bit data word serially, highest-order bit first, into the shift register SN74164, Sheet 1 of the schematic diagrams. However, only the lowest-order eight bits are retained in the latch SN74100, Sheet 1.

(2) Each serial input to the shift register consists of a three-bit binary word in negative true logic as follows:

Bit #	3	2	1
Code	$\overline{WE}$	$\overline{CLK}$	$\overline{DATA}$

where WE means Word-End Bit (called EXT TRANSFER by PLATO)

CLK means Clock Bit

DATA means Data Bit

Serial signal timing is shown in Figure 8.

(a) The clock bit sequences the shift register and sets the simultaneous data bit in the lowest-order output bit position of the shift register.

(b) As illustrated in Figure 8, the Word-End Bit remains low until the 15th data bit is being sent, then its 2-μs pulse causes the latch SN74100 to store and output the highest-order seven bits of the shift register.

FOR PLATO IV CONSOLES WITH ID NO. ≥ 262

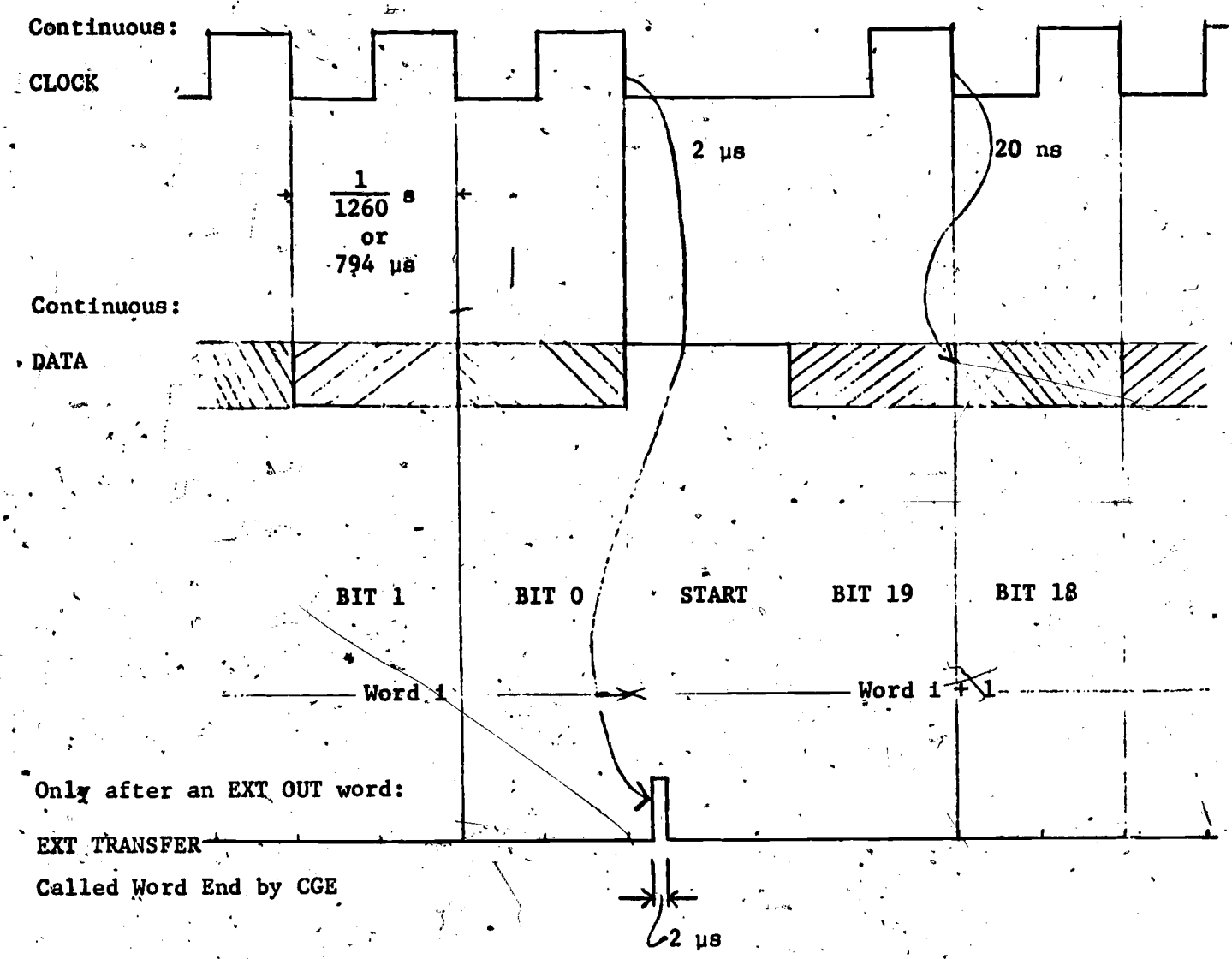


Fig. 8. PLATO EXT OUT Signal Timing.

(3). The format assigned by CGE to the eight-bit binary number output of the latch can be displayed as follows:

Bit No.:	8	7	6	5	4	3	2	1
	DC	CC	(◄	5 bit address			►)	(Parity)

(a) Bits 8 and 7 order the CGE interface to operate as follows:

ϕϕ Clear the CGE interface

ϕI Report the first terminal found connected to the addressed terminal, after checking in sequence from the addressed terminal to higher-numbered terminals

1ϕ Report the setting of the dial addressed.

(b) Consequently, Bit 7 is called CC for Connection Check and Bit 8 is called DC for Dial Check. When Bits 8 and 7 are both Ø all CGE outputs and relays are deactivated.

(c) Bits 6 through 2 form the five-bit binary address of the particular terminal or dial to be reported on by CGE.

(d) Bit 1 is a parity bit used by the PLATO terminal and is disregarded by the CGE system.

3.1 Summary of a Single Connection Check Operation

(1) An EXT CC PLATO signal Ø1xxxxx (in binary form at CGE) says, in effect: Begin with the terminal next higher in number to the address number and measure the externally-connected resistance between that (the connected) terminal and the addressed terminal.

(2) If the resistance measured by the Wheatstone Bridge (W.B. on Schematic diagram, Sheet 2) is less than 36 ohms, report to PLATO the number of the connected terminal.

(3) If the resistance measured by W.B. is greater than 36 ohms, sequence and connect to the next higher-numbered terminal and repeat the W.B. measurement.

(4) Conduct this search cyclically through the entire thirty terminals, sequencing from terminal 30 to terminal 1, until a connection to the addressed terminal is found and reported. Hence, if no other terminal is connected to the addressed terminal, the hardware will sequence through all the terminals (in about 3 ms) and simply report that the addressed terminal is connected to itself. If other terminals are externally connected to the addressed terminal, the hardware will report the number of the connected terminal next higher in number to the addressed terminal.

(5) Software routines programmed into the CGE-PLATO lessons determine what PLATO does with the report of the next connected terminal from CGE, and establish the next PLATO command.

(6) If the next EXT signal from PLATO is either ØØxxxxx or 1Øxxxxx, the connection checker system is deactivated.

(7) The step-by-step signal flow of a Connection Check command through the CGE-PLATO interface hardware is summarized on the accompanying flow chart, Figure 9.

3.2 Detailed Flow of a Single Connection Check Operation

(1) When a connection check signal is received from PLATO, the EXT TRANSFER (called WE for Word-End in CGE) pulse goes high before the CCO output of latch SN74100, Sheet 1, goes high. Timing of the EXT OUT serial-data signals is shown in Figure 7.

(2) Output 1Q of Monostable #1, SN74123A, Sheet 1, goes high with the falling edge of the 2-µs WE pulse, because the CCO signal at Input 1B is high by that time. The 5.5-second length of the 1Q output pulse is restarted at each ending of a WE pulse, in each check of a sequence of

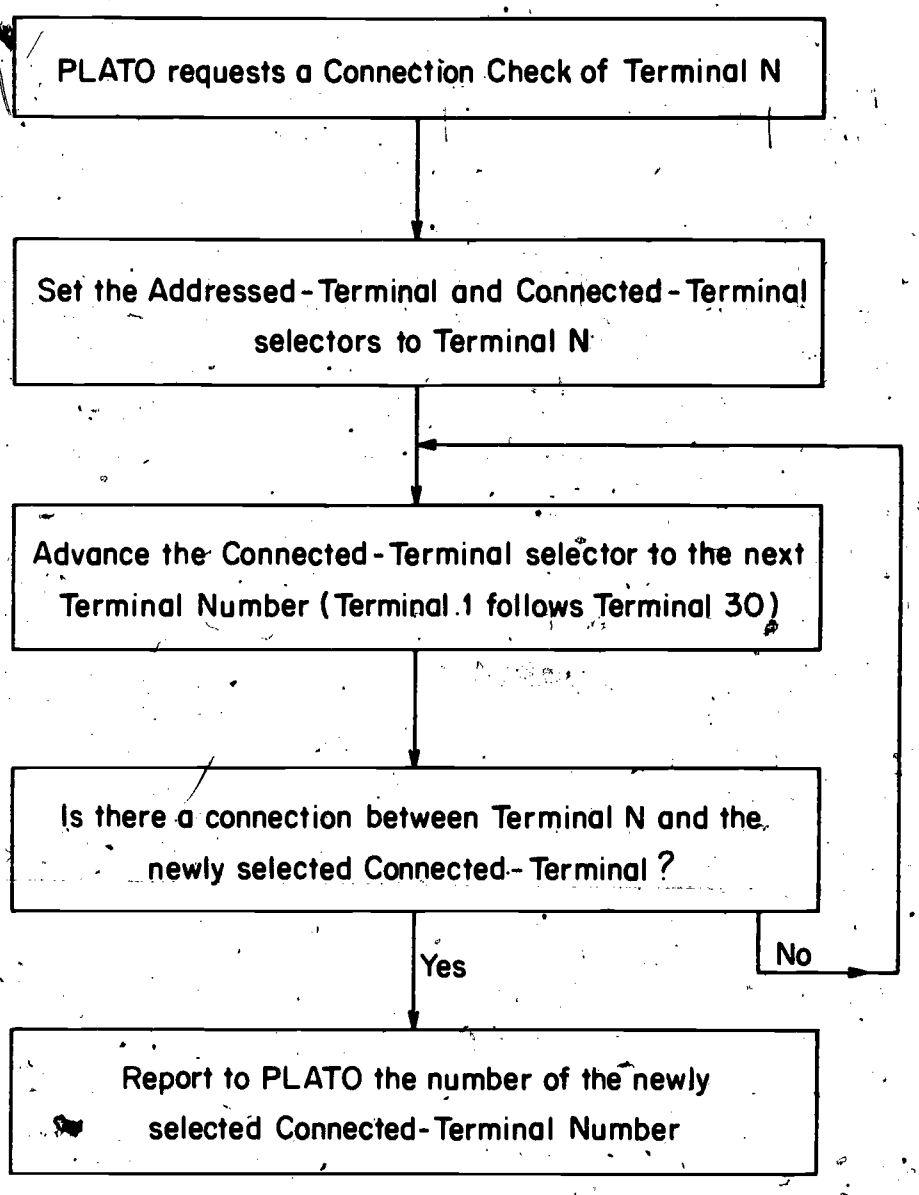


Figure 9 CGE Hardware Processing of a PLATO Connection Check Request

connection checks. If no EXT signal is received from PLATO within 5.5 seconds, the 1Q output will go low automatically and deactivate the CC system through the subsequent CC1 signal as a safety precaution, even though the CC0 signal output of latch SN74100 remains high.

(3) Output 1Q of Monostable #1, SN74123A, is added with CC0 to produce the CC1 signal. This CC1 signal controls the terminal deactivation system (Sheets 5 and 6), and the clock-counter system (Sheets 2 and 3) producing the CC connected-terminal address. In the GC clock system, the CC1 signal releases the preset of Monostable 1, SN7476, Sheet 2, so it can be clocked later by the 1Q output of SN74123B, Sheet 2.

(4) Consider the terminal deactivation system beginning on Sheet 5. The CC1 signal turns on transistors Q1 and Q2. Q1 closes the ground path to the CC relay, Sheet 4. Q2 causes the 62R2-24 V dc relay to operate and produce the 24 V CC2 signal which causes all the 62R4-24 V dc terminal deactivation relays, Sheets 5 and 6, to operate.

(5) When all 62R4 relays, Sheets 5 and 6, have operated, the 24 V CC2 signal, passing in series as the CC3 signal through one normally-opened contact on each of those relays, is sent as the CC4 signal to the CC relay coil, Sheet 4, and causes the CC relay to operate.

(6) Operation of the 36PDT CC relay, Sheet 4, connects the thirty deactivated terminals of the experimentation equipment, Sheets 5 and 6, to the inputs of the address-terminal LO2's, Sheet 2, and the connected-terminal LO2's, Sheet 3.

(7) The 62R4 terminal deactivation relays disconnect the instrument terminals from the interior circuits of the instruments and connect the thirty instrument and circuit board terminals to the normally-closed contacts of the CC relay. During the short interval between the operation of the

62R4 relays and the CC relay, the 47 ohm grounded resistors permanently connected to the normally-closed contacts of the CC relay cause any charges or currents in the experimentation circuit to be drained to zero before the CC relay operates. This is essential, because the solid-state switches, Sheets 2 and 3, will not tolerate high voltages (see ratings of Inselek L02's and L05's on pages 32-36).

(8) Operation of the CC relay, Sheet 4, also sends the + 5 V CC5 signal to Input 1B, SN74123B, Sheet 2, causing Output 1Q to deliver a 23 ms, + 5 V pulse. This pulse width is provided to allow all relay bounces to settle to zero. The falling edge of this pulse clocks Monostable 1, SN7476, Sheet 2. Subsequently, the $\overline{1Q}$ and 2Q outputs of SN7476 and the $\overline{2Q}$ output of SN74123B are all high and are added to deliver + 5 V to Input 1B of SN74123C, Sheet 2. This starts the CC clock formed by Monostable #2, SN74123B, and Monostables 1 and 2 of SN74123C, Sheet 2. The $\overline{1Q}$ output of SN7476 also sends the CC6 signal to the CGE output network, Sheet 9.

(9) Meanwhile, the SN74193A and B counters, Sheet 3, have been loaded with the terminal address received from Latch SN74100, Sheet 1, by the $\overline{WE}$ zero pulse. Consequently, at this time the addressed-terminal L05's, Sheet 3, and the connected-terminal L05's, Sheet 4, are both set to the same addressed terminal. This terminal, addressed by PLATO, is called Terminal N hereafter.

(10) The period of the CC clock consists of three distinct pulse lengths, and each pulse length is 34 μs in length. The + 5 V signal into 1B of SN74123C starts the first pulse of the CC clock period, a zero pulse at Output $\overline{1Q}$. The trailing edge of that zero pulse drives Input 2B and starts the second pulse of the CC clock, Monostable #2 of SN74123C. Also, the trailing edge of the first pulse counts the CC counter composed of SN74193A

and B, Sheet 3, advancing the connected-terminal LO5's to Terminal N + 1. The second pulse drives Input 2B of SN74123B. The trailing edge of the second pulse starts the third pulse of the CC clock at Output $\overline{2Q}$ of SN74123B. During the second pulse, Output 2Q of SN74123B is high and is added with the output of the comparator SN72710, Sheet 2, to drive the clear input of Monostable 2, SN7476, Sheet 2.

(11) If Terminal N + 1 is connected to Terminal N, Monostable 2, SN7476, will be cleared, its output 2Q will go low and stop the CC clock, as its output $\overline{2Q}$ goes high, sending the CC READY signal inverted to Input 1A of SN74123D, Sheet 9. At that time, the connected-terminal N + 1 address is set into the SN7450, Sheet 9, output system to PLATO. The leading edge of the inverted CC READY signal triggers Monostable 1 of SN74123D, Sheet 9, so the leading edge of the zero pulse of Output $\overline{1Q}$ triggers the Monostable 2, SN74123D, which sends a 49 ms zero pulse as the CGE $\overline{\text{READY}}$ signal to the PLATO console. Quite reliably, the PLATO console records the EXT IN data within 15 ms.

(12) If Terminal N + 1 is not connected to Terminal N, Monostable 2, SN7476, will not be cleared by the comparator, and the trailing edge of the third pulse during the first CC clock period will initiate the first pulse of the second CC clock period as Output $\overline{2Q}$ of SN74123B drives Input 1B of SN74123C. As described above for the first CC clock period, the CC counter again advances to make the connected-terminal N + 2. This CC clock and counter sequencing continues at the rate of about 100 μs per CC clock period until a terminal is found connected to the addressed terminal. The sequencing wraps around from Terminal 30 to Terminal 1 continuing until a terminal is found connected to Terminal N. Hence, if no terminal is found connected to Terminal N, CGE will report to PLATO within 3 ms that Terminal N is connected to Terminal N.

(13) The CGE software routines process each CC report of a terminal connection, and order checks of successive terminals as needed in the PLATO programmed lesson. As far as the CGE hardware is concerned, the complete check of thirty terminals need only require an initial 23 ms for relay bounce to dissipate plus 30 times 3 ms, or a total of about 113 ms. The actual time required for PLATO to order and receive a complete check of thirty terminals is on the order of six seconds because the round-trip transmission time of a single CC terminal report through the PLATO site controller to PLATO and return is about 200 ms per signal transmission.

3.3 Summary of a Single Dial Check Operation

(1) An EXT DC PLATO signal Ø1xxxxx (in binary form at CGE) says, in effect: Report the dial setting of the address-numbered dial. The Dial Setting Codes automatically reported by CGE to PLATO are in Figure 7.

(2) The step-by-step signal flow of a Dial Check command through the CGE-PLATO interface hardware is summarized on the accompanying flow chart, Figure 10.

(3) Software routines programmed into the CGE-PLATO lessons guide PLATO to store the reported dial setting and request the setting of the next dial. It is unnecessary to turn any hardware off after sending any dial setting.

3.4 Detailed Flow of a Dial Check

(1) When a dial check signal 1Øxxxxx is received from PLATO, the DC signal from Output Q8 of the latch SN74100, Schematic Diagrams, Sheet 1, triggers a 40 μs pulse in Monostable #2, SN74123A, Sheet 1. The leading edge of this 40 μs pulse resets the Analog-Digital Converter ADC Econoverter, Sheet 7, while the sensor address output of the latch SN74100, Sheet 1, causes the LO2's, Sheet 7, to connect the dial sensor addressed through the buffer amplifier, SN72741, Sheet 7, to Analog Input I2 of the ADC.

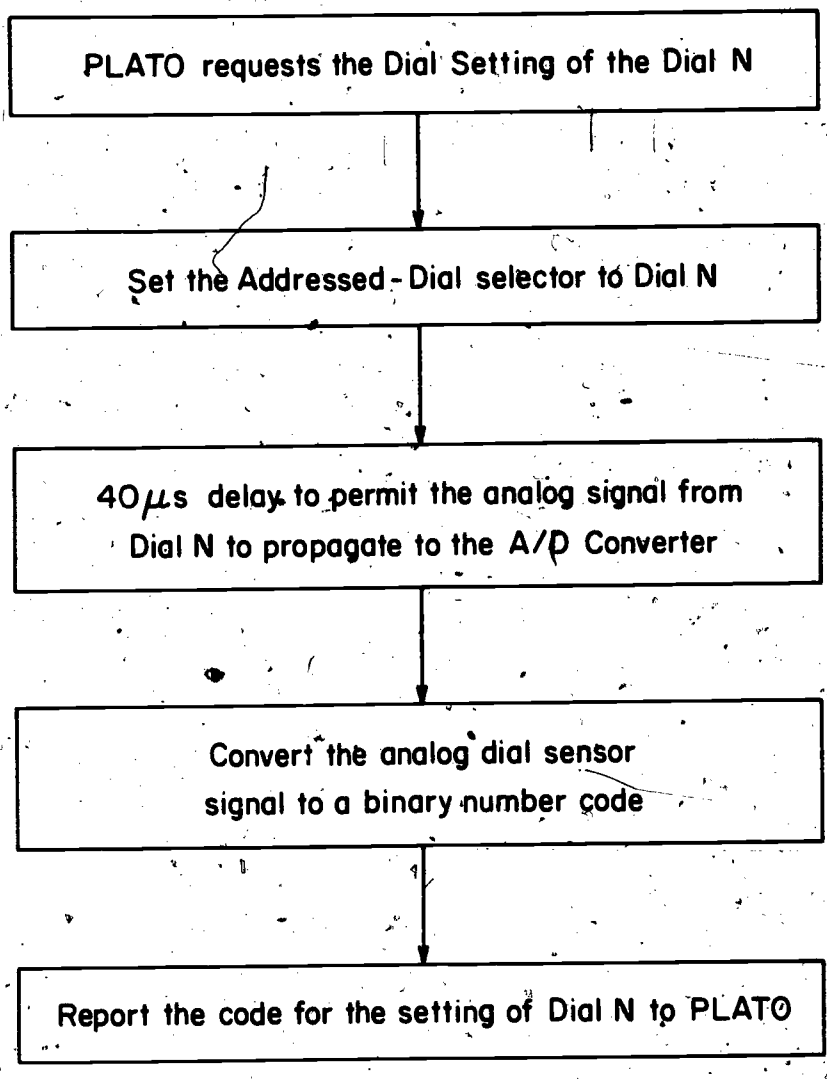


Figure 10. CGE Hardware Processing of a PLATO Dial Check Request

(2) The falling edge of the 40 μs pulse causes the ADC to convert, i.e., output the binary digital number corresponding to the input dial sensor voltage. This sensed dial setting code is set into the SN7450, Sheet 9, output system to PLATO.

(3) The leading edge of the inverted DC ready signal from Monostable SN74123A, Sheet 1, triggers #1 Monostable of SN74123D, Sheet 9, then the leading edge of the zero pulse of Output $\overline{1Q}$ triggers #2 Monostable of SN74123D which sends a 49 ms zero pulse as the CGE $\overline{\text{READY}}$ signal to the PLATO console. Quite reliably, the PLATO console records the EXT IN data within 15 ms.

(4) The CGE software routines process each DC report and order successive dial checks as needed in the PLATO programmed lesson. As far as the CGE hardware is concerned, the complete check of twenty-two dials need only require 22 times the 40 μs pulse delay or a total of about 880 μs. The actual time for PLATO to order and receive a compete check of twenty-two dial settings is on the order of four seconds because the round-trip transmission of a single dial check through the PLATO site controller is about 200 ms per signal transmission.

CHAPTER 4 - SOFTWARE OF THE CGE-PLATO SYSTEM

4.0 Control of Connection and Dial Checks by the CGE Software Subroutines

As can be seen from Figures 9 and 10 in the explanation of the operation of the CGE hardware, one command from PLATO for a connection check or a dial check elicits a single response from the hardware. Consequently, a complete check of either all the terminal interconnections or all the dial settings requires a series of commands and responses.

The original design of the CGE-PLATO interface performed and reported to PLATO a complete check of all terminal interconnections or all dial settings in response to a single command from PLATO. Though simple in concept, this report of a string of data into PLATO was found to be unreliable, because characters of the string would occasionally be lost in the transmission. High transmission reliability was achieved by reporting a single data word in response to a request from PLATO and holding this data on the line until a second PLATO request is received. So far, it has not been found necessary to have PLATO repeat back each data word as a check. Though hardware was designed to handle such a check, it was not built.

The minimum amount of hardware and the maximum reliability were achieved with the present system. The CK software subroutines organize and conduct each complete check terminal by terminal or dial by dial.

For a connection check, PLATO begins by asking the CGE station, "To what terminal is Terminal 1 connected?" The CGE hardware then tests for an external connection between Terminal 1 and each of the other terminals in a numerical and cyclical sequence in which one follows thirty. If CGE replies "Terminal 1," the hardware must have cycled through all of the terminals and found that none of them were interconnected with Terminal 1. Instead, suppose CGE replied "Terminal 11." This would mean that no terminal between 1 and 11

was interconnected with 1. In this case, PLATO would ask, "To what terminal is Terminal 11 connected?" If one other terminal is interconnected with 1 and 11, CGE would report that terminal number. If not, CGE would report "Terminal 1."

The CGE subroutines order the connection check in the above manner and flag each terminal number as it is reported. All terminals of an interconnected set are similarly flagged. Such a set is called a node in electrical circuit theory. In the above case where only Terminals 1 and 11 were found in the 1st node, PLATO would then ask, "To what terminal is Terminal 2 connected?" CGE would reply, and the queries and responses would continue until CGE reports on each of the thirty terminals. When PLATO, in sequencing through the list of thirty terminals, encounters a terminal previously flagged as having been reported on by CGE, it skips that terminal and resumes its check with the next higher numbered terminal that has not been so flagged. Thus, only thirty queries and responses establish all the possible interconnections between the thirty terminals.

Compared to a connection check, a complete dial check is quite simple. PLATO simply asks the setting of each dial and CGE reports that dial setting. PLATO continues, dial by dial, until twenty-two queries and responses have enabled PLATO to receive and store the setting of each of the twenty-two dials.

4.1 Author Usage of the CGE-PLATO Subroutines

All CGE experimentation lessons "use" the CK (checker) subroutine package contained in lesson eexØØ. The various subroutines in this package provide CGE authors with several convenient and flexible means of using the CGE-PLATO hardware interface to automatically check the terminal interconnections and the dial settings of the CGE experimentation equipment, and judge the actual setup against author-specified correct setups. Each author can use the results of the connection and dial checks in any manner he can devise for improving

student learning. Considerable experience indicates that the least instructive method is to simply display the errors in the student's setup.

The identification numbers of the terminals and dials sensed by the CGE-PLATO interface are displayed in Figure 4, Dials and Terminals Sensed on the Rack-Mounted Experimentation Equipment.

The TUTOR commands "do" or "join" are used to call a subroutine. Before the call is made to the subroutine, it is necessary to tell the subroutine what the correct setup is supposed to be. This is accomplished through the use of the TUTOR command "pack." All CK subroutines expect to find the correct setup codes starting in student variable n33. Thus the following two commands first establish the correct or author setup connection codes and then call a subroutine which directs the CGE interface to perform a connection check.

```
pack    n33,aadbbØddØØØØcØØØØØØØØØØØØØØcØØ      $$ packs conn. codes
do      ckc                                       $$ performs conn. check
```

When the subroutine "ckc" is called, it causes CGE to perform a connection check, temporarily store the result, judge the student setup against the author setup currently in n33, and then sets the number of errors in n47.

All the CK subroutines return with variable n47 = -(number of errors found in setup). There are 150 student variables. The CK subroutines use student variables n1 through n49. Therefore NO CGE experiment is allowed to use student variables n1 through n49.

A Connection Check author setup code is specified as follows:

```
pack    n33,+Ø+ØØaØabaØbØnØØnØØØØØØØØØØØØ      $$ 30 characters
```

This code specifies the following situation as the correct or author setup for the connections:

Terminals 6, 8, and 10 should be connected together as a node.
Terminals 9 and 12 should be connected together as a node.
Terminals 14 and 17 should be connected together as a node.

Terminals 1 and 3 are "don't cares" it doesn't matter what they are connected to.

Terminals 2,4,5,7,11,13,15,16,18,19,20,...,29,30 should not be connected to anything.

Note the character Ø (zero) specifies NO CONNECTIONS.
The character + (plus) specifies a "don't care."
Any other character may be used to indicate nodes, e.g., a, b, and n were used above.

The dial codes which correspond to the dial settings are listed in Figure 7, Dial Setting Codes. PLATO lesson CGERL is also useful for determining the actual settings of dials.

Dial Check Codes should be packed in variable n33 as in the following example:

```
pack        n33,d+ac+(def)+++(gh)++++++++++++
```

This code specifies the "correct setup" as being:

```
Dial  1   set to position  "d"
Dial  3   set to position  "a"
Dial  4   set to position  "c"
Dial  6   set to position  "d," "e," or "f"   judge any of these as being correct
Dial  10  set to position  "g" or "h"         judge either correct
```

and Dials 2,5,7,8,9,11,12,13,...,21,22 "don't care" judge anything correct.

Note that the group of codes within parentheses allow you to specify multiple settings on a single dial to be correct. This is particularly useful in allowing for tolerances when specifying the settings of continuously adjustable dials.

Another method of packing permits an author to specify various acceptable pairs of dial settings for any two dials which have adjacent identification numbers. For this method, two or more acceptable pairs of settings are

enclosed in angle brackets. For example, consider the Audio Oscillator. For 2100 Hertz, the RANGE and FREQUENCY dials could be set at 10 and 210, respectively (codes bv), or at 100 and 21, respectively (codes cc). To accept either of these pairs of settings, the pack for dials 20 and 21 would be: bvcc . The second letter for any pair can be shown as a multiple setting in parentheses as illustrated in the preceding paragraph. This is not true for the first letter of any pair. For example, if the code for a pair of dials is entered as c(fgh)de , then acceptable pairs would be cf, cg, ch, or de.

Two basic sets of CGE checking subroutines are available. The CKC series checks and judges a student's connections. The CKD series checks and judges a student's dial settings. Flow diagrams for the CKC series are shown in Figure 11. The CKD series flow diagrams are similar to those for the CKC series.

The following subroutines comprise the CKC series:

CKC Performs a complete connection check using the CGE interface hardware and stores the student setup data. It also judges the student setup against the current author setup in n33 and returns n47 = -(number of errors). It also initializes the "Best Match Setup" to the current author setup in n33.

CKCW Same as CKC but additionally it performs a full screen erase and generates an error display for the student. (w because it writes)

CKC1 Takes the student setup data which were stored by either CKC or CKCW and judges them against the current author setup in n33 and returns n47 as above. If the number of errors found in this setup is fewer than that found in the previous "Best Match Setup" then the "Best Match Setup" is set to the current author code in n33.

CKC1W Same as CKC1 but it does a full-screen erase and generates a display of the incorrect connections and the missing connections.

CKC2 Takes the student setup data which were stored by either CKC or CKCW and judges them against the current "Best Match Setup." It does this by automatically packing n33 with the "Best Match Setup." It returns n47 as above.

CKC2W Same as CKC2 but it does a full-screen erase and generates an error display.

Both the CKC series of subroutine entries and the CKD series of subroutine entries have the same overall structure.

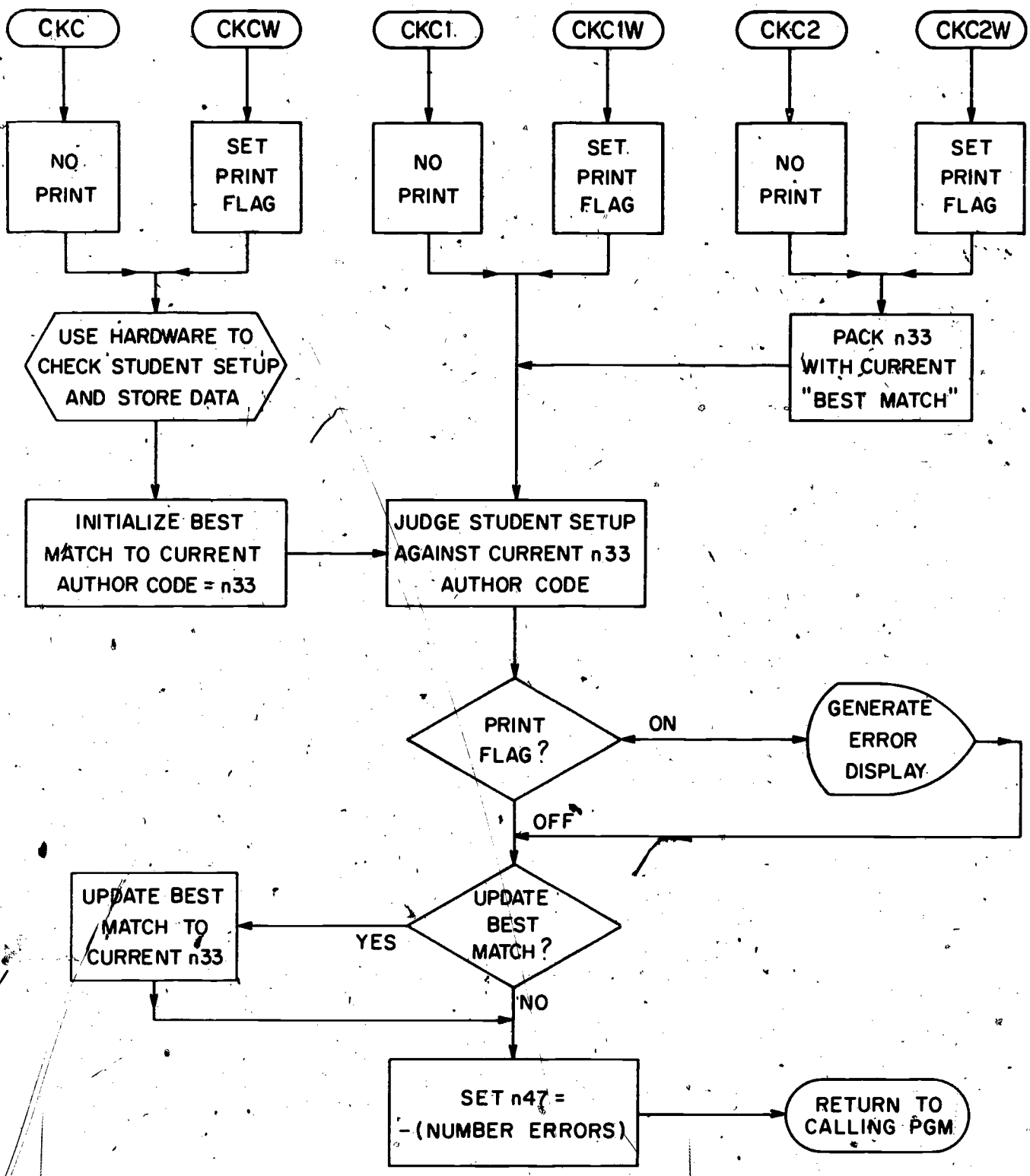


Figure 11. Basic Flow Diagram of the CKC Series of Subroutines.

The following subroutines comprise the CKD series:

CKD Performs a complete dial check using the CGE interface hardware and stores the data about the student setup in character form starting in variable n30. (It remains there after use of the subroutine. If you desire to access specific dial codes, use the TUTOR command "move" in order to move characters out individually.) It then judges the student setup against the current author setup in n33 and returns n47 = -(number of errors). It also initializes the "Best Match Setup" to the current author setup in n33.

CKDW Same as CKD but also a full-screen erase and generates a display showing only those dials which were incorrectly set, without showing the correct settings.

CKD1 Takes the student setup which is stored in n30 and judges it against the current author setup in n33 and returns n47 as above. If the number of errors found in this setup is fewer than that found in the previous "Best Match Setup," then the "Best Match Setup" is set to the current code in n33.

CKD1W Same as CKD1 but also does a full-screen erase and generates an error display.

CKD2 Takes the student setup which is stored in n30 and judges it against the current "Best Match Setup" by first packing n33 with the "Best Match." It then returns n47 = -(number of errors found).

CKD2W Same as CKD2 but also does a full-screen erase and generates an error display.

PLATO lesson CGERL allows experimentation with the various subroutines and with packing codes into n33. The following examples should be useful, in addition to other options mentioned above, in helping authors determine what the author codes should be for a particular setup:

```
unit    simplest
at      510
write   Set dials and then Press -NEXT-.
pause           $$ wait for student to press NEXT
pack    n33,/setup1/          $$ specify author code
do      ckd                   $$ perform dial check
jump    n47,wrongunit,rightunit      $$ then branch on basis of outcome of check
```

```
unit    one          $$ another example
at      510
write   Set dials and then Press -NEXT-
pause
pack    n33,/setup1/
do      ckd                  $$ perform check and judge against setup1
pack    n33,/setup2/
do      ckd1       $$ judge student setup against another setup
do      ckd2w      $$ then display errors made in the better of the two setups
next    n47,wrongunit,rightunit
```

```
unit    one
at      510
write   Set dials and then Press -NEXT-.
next    check
help    helpunit
unit    check        $$ separate unit for check useful when you don't want a
                     $$ pause in the first unit because you may want HELP or BACK etc
pack    n33,/setup/
do      ckdw
next    n47,wrongunit,rightunit
```

It is usually desirable to NOT give an error display and instead send the student to some special help unit on the basis of the type of error he made.

```
unit    one
at      510
write   Set dials and then Press -NEXT-.
inhibit erase        $$ prevent a full-screen erase from being done when student
next    two          $$ presses NEXT
unit    two
pack    n33,/setup1/     $$ setup1=dddaddddddddd+++++++++
do      ckd
pack    n33,/setup2/     $$ setup2=ddd+dd+ddddd++++++++++

jump    n47,x,allright   $$ jump if no errors in setup1
do      ckd1
jump    n47,someother,dial4or7wrong
```

In every event, the author should be sure the student is not trapped in a loop without advice on how to proceed or repeat some task.

4.2 Summary of the CGE-PLATO Lessons

Names of the TUTOR language PLATO lessons or files used by CGE are given below. The "inspect" code is cge for all these files:

cge - A summary description of the Computer-Guided Experimentation Research project for general information. This lesson is accessible to any student from lesson SAMPLE. The CGE station equipment is described in this lesson.

cgerl - This file contains CGE hardware test routines and information for CGE authors.

ee244 and eecge - These are the PLATO courses assigned to CGE.

cgeindex - This file is the router lesson for the CGE laboratory lessons in PLATO courses ee244 and eecge. All CGE experiments have PLATO names beginning with eex, and are indexed in this file and are accessed from this lesson.

cgedata - This is the student data record file for courses ee244 and eecge.

eexØØ - This is the introductory CGE lesson which assures that a student can communicate with PLATO, is oriented with the laboratory station, and learns the Safe Initial Mode in which the experimentation equipment is to be set at the beginning of each experiment. The CGE subroutines, used in all CGE experimentation lessons, are included in this file.

eexØ1 - The Oscilloscope.

eexØ2 - The Function Generator.

eexØ3 - The Audio Oscillator.

eexØ4 - The DC Supply.

eexØ5 - The Vacuum Tube Voltmeter.

eexØ6 - Transients.

eexØ7 - Impedance.

eexØ8 - Two-Port Networks.