Circuit Implementation of OOK Modulation for Low-Speed Power Line Communication Using X10 Standard

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Abstract— **This research implements a power line communication system that adopts the power line communication (PLC) [1] standard "X10" and the On Off Keying (OOK) [2] modulation technology. The OOK technology can be used to judge the demodulated results and examine the digital signal data. The circuits are divided into transmitter and receiver in the power line communication system. Power line system experiments using a realistic grid system determined the transmission signal distance between the transmitter and receiver can reach to 40~50 meters. In the case where the transmitter and receiver are not connected to the grid system, we compared the output signal with the original signal data. The signal delay time is 8.5us in one meter and 12.5us in forty nine meters. The output signals vary with the different distances. The experiment shows that the signal declined 11.116 dB in 20 meters and 15.619 dB in 50 meters. The results show that the proposed system is functional using 12 bit digital signals generated by a microprocessor.**

Keywords——**Power Line Communication, On Off Keying, Comparator, Filter, Equalizer**

I. INTRODUCTION

Transmitter is composed of a square wave generator using a CMOS astable multi-vibrator. The square wave generator is used to generate a 125 KHz pulse signal. To implement the OOK modulation technique, the 0 and 1 signal is coupled using a square wave generator circuit and a digital signal generator. The power line output signals will attenuate at different impedance with changing distance. To solve this problem, the current driving capability can be improved using a line driver circuit and an output circuit in the transmitting stage. The signal is then coupled to the power line. In the receiving stage, the transformer has a feature that can filter out the 60 Hz grid signal and receive the OOK signals. Because the power line impedance during transmission can cause signal attenuation, the gain control stage is used to fix the output signal amplitude. The receiving signal recognition can be improved. Furthermore, the OOK modulation signal will mix with the power line noise, reducing the signal accuracy. Thus, a band-pass filter is used

to catch the signals and filter out the noise. A demodulator circuit is used to distinguish the reverting signals to achieve the preliminary comparator work. The demodulator circuit consists of a full-wave rectifier and a peak detector circuit. The OOK modulated signals are restored into digital signals using the comparator circuit hysteresis characteristic.

II. PROPOSED SYSTEM DESIGN

The power line communication structure is divided into two parts. The first is a transmitter; the second is the receiver. The transmitter has three parts: OOK signal modulation, a line driver and a line coupler. The receiver has five parts: a line coupler, band-pass filter, GC, demodulator and comparator, as shown in figure 1.
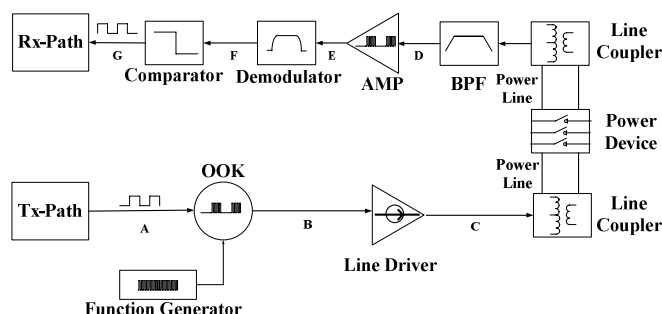
Figure1. Power Line Communication system block diagram

A. OOK Modulation Signals

The OOK modulation is composed of a square wave generator and a digital signal generator. The square wave generator is composed of a CMOS astable multi-vibrator, as shown in figure 2. The main concept is to implement the CMOS astable multi-vibrator adopting two CMOS inverter circuits to charge and discharge.
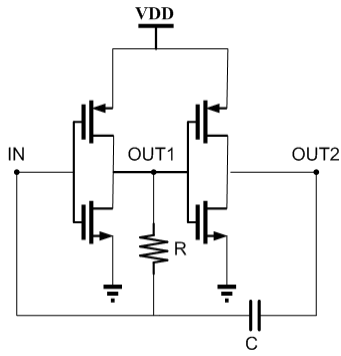
Figure 2. CMOS astable multi-vibrator circuit

1) Charge: When the input signal is high (IN=HIGH), one output signal becomes high (OUT1=HIGH) and the other becomes LOW (OUT2=LOW), as shown in figure 2. According to the output signal (OUT2) and the feedback loop composed of a capacitance C and a resistance R, the capacitance will be charged to a high level in the opposite direction. Thus, the circuit input node (IN) turns to the LOW level. The capacitance C charge formula is given as follows:

$$V_C(t1) = V_{DD} \times \left(1 - e^{\frac{-t}{RC}}\right). \qquad (1)$$

2) Discharge: When the capacitance is charging to 5V, IN= LOW, OUT1= HIGH, and OUT2= LOW. The loop is formed by OUT1, resistance R, OUT2 and capacitance C in the circuit. After the capacitance C is discharged, the current will turn the input node IN voltage down to lower than 0V. The capacitance C discharge formula is given as follows:

$$V_C(t_2) = V_{DD} \times e^{\frac{-t}{RC}}. \qquad (2)$$

$$V_C(t) = V_{th} = \frac{V_{DD}}{2}. \qquad (3)$$

We suppose that eq. (3) is established, then substituting t1 and t2 using equations (1) and (2) and adding them to get the oscillation cycle T of capacitance C.

$$T = t1 + t2 = RC \cdot \ln\left(\frac{V_{DD}}{V_{DD} - V_{th}}\right)$$
$$= RC \cdot \ln\left(\frac{V_{DD}^2}{V_{DD} \cdot V_{th} - V_{th}}\right) \qquad (4)$$

The OOK generator schematic diagram has two parts. The first is a square wave generator; the second is the digital control signal, as shown in figure 3. The OOK generator is composed of two part multiplication, generating 125 KHz OOK signals.
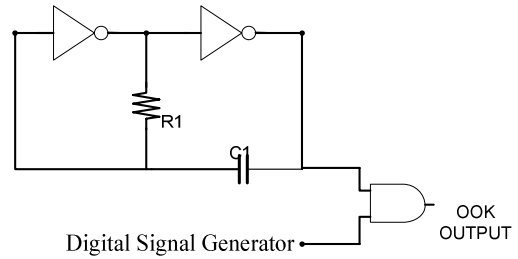

Figure 3. OOK generator circuit

B. Line Driver

The line driver has two abilities. The first is to receive signals from the OOK modulation stage. The second is to enhance the signal current driving capability. The line driver has three features:

1. Voltage gain=1

2. High input impedance

3. High output impedance

The operational amplifier (OP) generally has two features. There is only 40~80mA output current, requiring 200~300mA current promotion to deal with different loads. OOK signals can be delivered to the power line through a transformer, making a voltage to current (V-I) feedback circuit needed to achieve a stable current source. A power MOSFET IRF510 that can tolerate high voltage and high current is also needed for the driver stage. Figure 4 shows the I-V power MOSFET curve.
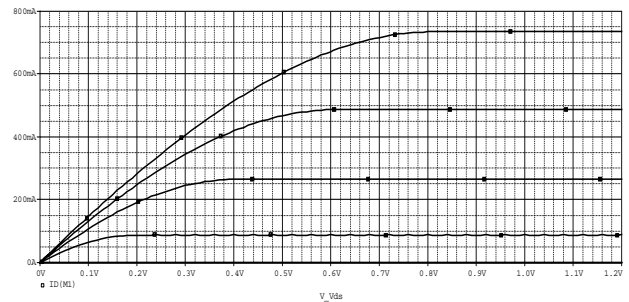

Figure 4. The I-V characteristics of power MOSFET

Figure 4 shows the different Id to Vgs characteristics of IRF510 from top to bottom at 4.5V~3.5V, respectively. In this figure, the Vgs of MOSFET is 3.9V~4.1V when the current is chosen in 200~300mA. The line driver circuit is shown in the figure 5.
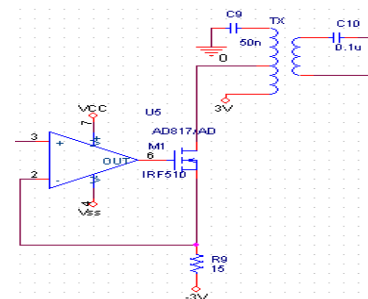

Figure 5. The line driver circuit

C. Line Coupler

When a signal is transmitted to the power line, it must be coupled with a transformer. The transformer filters the 110V 60Hz grid signals out and avoids destroying the receiver circuits. A070EK transformer coil from TOKO Company was used in this research. As shown in figure 6, the A070EK transformer coil has a primary winding and two secondary windings. The A070EK operating frequency is set to near 100 KHz to fit our OOK signal. A 1:1 ratio transformer coil winding is used to couple the signal onto the power line. A series capacitance C9 is used to form a low-pass filter at the secondary winding side. Collocating C9 with a secondary winding can form a band-pass filter (BPF) to couple the signal to the grid. The BPF can filter ambient noise and surge out to protect the receiver stage. A C10 capacitance is used to filter 110 V, 60 Hz alternating current grid out, but OOK signals will not be affected. Therefore, a special C10 capacitor with high voltage endurance is needed to protect the transformer A070EK [3].
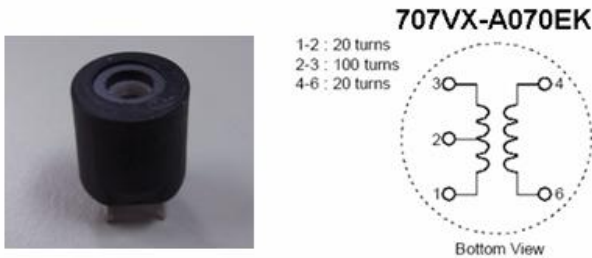

Figure6.   The A070EK transformer

D. Band Pass Filter

The filter design parameters include (a) Circuit gain. (b) Q value. (c) Load effect. (d) Circuit Complexity. A forth-order band-pass filter constructed using the Sallen-Key [4] method was used in this research. The second order filter formula is given as follows:

$$T(S) = \frac{\omega_0^2}{S^2 + S\left(\dfrac{\omega_0}{Q}\right) + \omega_0^2}. \tag{5}$$

Q is the quality factor and ω_0 is the filter operating frequency. Figures 7 and 8 show the second order filters with high, low and band-pass structure, respectively.

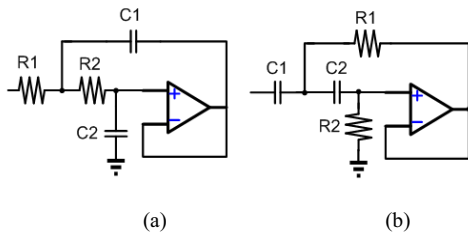(a)   (b)

Figure7.   Second order filter circuit (a) Low pass filter
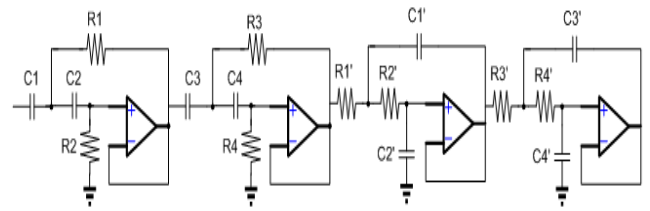(b) High pass filter

Figure8.   Band-pass filter circuit

E. Gain Control

Because the signal will be attenuated at power line distance, the gain control stage is used to generate a constant output signal using a non-inverting amplifier, as shown in figure 9.
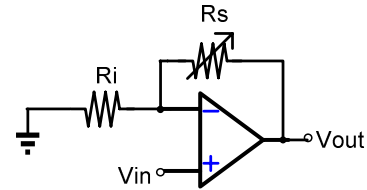

Figure9.   Gain control circuit

F. Demodulator

A demodulator circuit is used to distinguish the reverting signals to achieve the preliminary comparator work. The demodulator circuit [5] is composed of a full-wave rectifier and a peak detector circuit. The full-wave rectifier circuit and peak detector circuit are used to transform the ac signals into dc signals for data recovery.

1) Full-Wave Rectifier Circuit: Full-wave rectifier circuit is shown in figure 10, composed of a half-wave rectifier circuit. The input signal is positive and the diode (D2) is conductive. At the same time the operational amplifier A2 serves as a buffer. Because the negative input voltage of the operational amplifier A1 is positive and higher than the positive input voltage, the A1 output signal is negative. Thus, the diode (D1) is not conductive. So the conduction loop is composed of a buffer A2 and a load RL. When the input signal is positive, the output signal is positive. As the input signal is negative, the diode (D1) is conductive. The diode (D2) is not conductive. The operational amplifier A2 does not work. The conduction loop is composed of an inverting amplifier A1 and a load RL. When the input signal is negative, the output signal is positive.
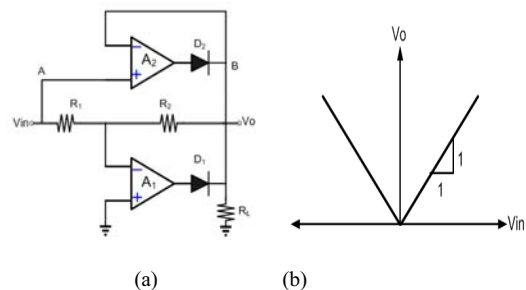

(a)   (b)

Figure10.   (a) Full-wave rectifier circuit. (b)The transform function

2) Peak Detector Circuit: when the peak detector is required to hold the value of the peak for a long time, the capacitor should be buffered, as shown in figure. 11. The circuit provides a dc voltage output equal to the peak of the input signals.
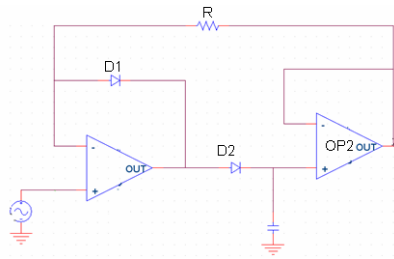

Figure 11. A buffered precision peak circuit

G. Comparator

The OOK signals are restored to digital signals by the comparator circuit [6]. The hysteresis characteristic of the comparator circuit used here is to lower the signal distortion interfered by noise, as shown in figure 12.

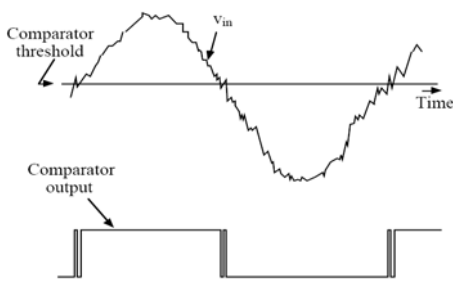Figure 12. Comparator response to a noisy input when hystersis is added

Figure 13. Comparator response to a noisy input

The normal hysteresis structure of the comparator circuit is shown in figure 14(a), and its feature curve is shown in figure 14(b).
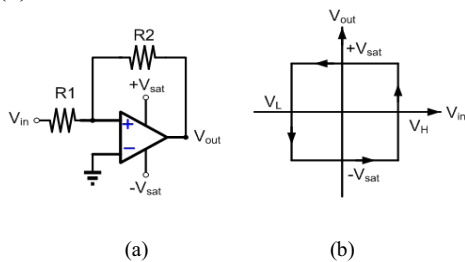

(a)   (b)

Figure 14. Noninverting bistable circuit using external positive feedback

The Formula is shown in (6)、(7)

$$V_H = \frac{R1}{R2}(-V_{sat})$$ (6)

$$V_L = \frac{R1}{R2}(+V_{sat})$$ (7)

Vsat and V-sat are supply voltages. V_H is positive trip point. V_L is negative trip point. $V_H - V_L$ represents the width of the bistable characteristic. The center point of the bistable characteristics in figure 14 can be shifted horizontally by inserting a battery, Va, as shown in figure 15 for counter-clockwise bistable circuit.
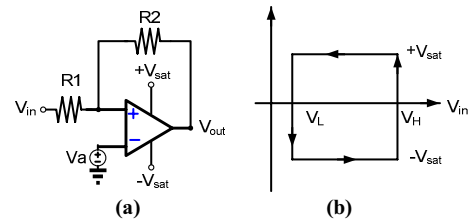

(a)   (b)

Figure 15. Horizontally shifted noninverting bistable circuit using external positive feedback

Related formulas were shown in (8), (9)

$$V_H = \frac{R1+R2}{R2}Va + \frac{R1}{R2}(-V_{sat})$$ (8)

$$V_L = \frac{R1+R2}{R2}Va - \frac{R1}{R2}(+V_{sat})$$ (9)

III. EXPERIMENT RESULTS

The experimental results are described in this section. The amplitude of input signals is 5 V. Figures 16 and 17 show the attenuated output signals received in front of the receiver stage at different distances.
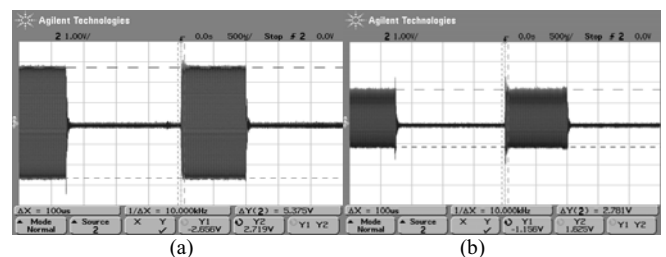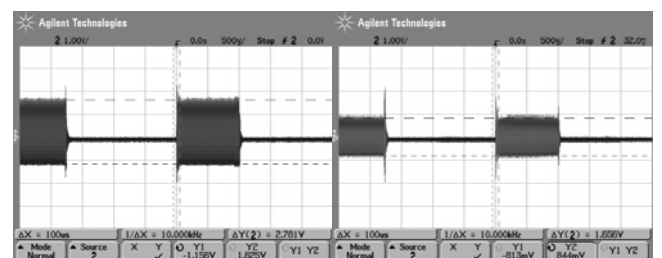

(a)   (b)

Figure 16. (a)Recevied signals 1 meters (b) Recevied signals in 10 meters

Figure17.   (a)Recevied signals in 20 meters (b) Recevied signals in 49 meters

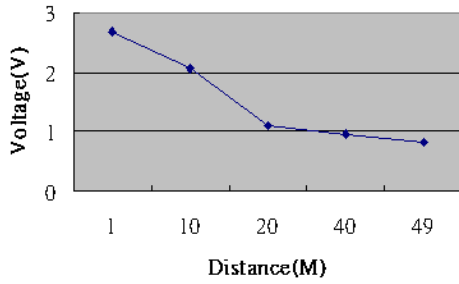Figure 18 shows the attenuated voltage varies with different distances.

Figure18.   The attenuated voltage trend

Tables I shows additional information about the distances, output voltages and attenuations of PLC system.

Table 1.   THE EXPERIMENTAL RESULTS OF DIFERENT DISTANCE

Distance（M）	Output voltage（V）	Attenuation
1（M）	2.6875 V	-5.3924 dB
10（M）	2.0625 V	-7.6915 dB
20（M）	1.0935 V	-13.2030 dB
40（M）	0.969 V	-14.2529 dB
49（M）	0.828 V	-15.6188 dB

Figure 19 illustrates the delay time between input and output signals. Figures 19(a) and 19(b) show the delay time of 8.5 us in one meter and 12.5 us in forty nine meters, respectively.
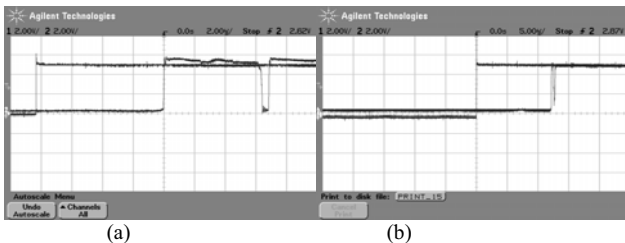

(a)   (b)

Figure19.   The results of delay time in (a) one meter (b) 49 meters

Figure 20 illustrates the proposed system is functional through verification by inputting 12 bit digital signals generated using a micro-processor.
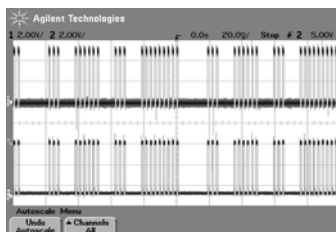

Figure20.   The verification of input/output signals generated by proposed PLC system

No fuse break (NFB) and earth leakage circuit break (ELB) are both over-loading prevention products. Figure 21 shows the attenuation after the PLC signals pass through. From the experimental results, the signal is attenuated 7.905 dB by NFB and 7.911 dB by ELB, respectively. The power device NFB NV50-MB and ELB EL350-R produced by WULING.ELECTRIC.CO.LTD was implemented in this paper.
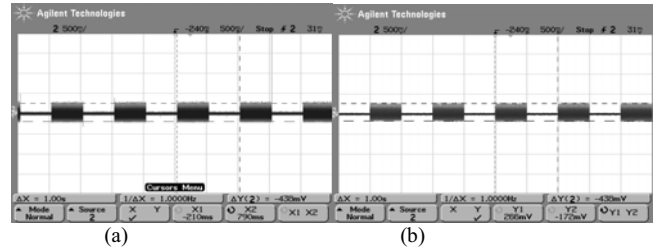

(a)   (b)

Figure21.   The output waveform of (a) NFB (b) ELB

IV. CONCLUSIONS

Power line communication systems can be applied to lighting equipment, security systems, fire suppression systems, home appliances and so on. Because all of these applications need power to work, we can lower the cost, save networks space requirements and make the networks simple. When the wireless signal is too weak, we can use power line communication systems to solve the problem. The power line communication system measures the signals at different distances 1m, 10m, 20m, 40m, and 49m shown in the experimental results, respectively. We hope to measure the attenuation signals of the power protection NFB and ELB device for linking two or more blocks together. The measurement result shows that the devices have not been cut off, but the signal is decayed. Otherwise, the receiver sensitivity is important because of the sensitivity to determine whether or not to read the signal. The proposed power line communication system implementation adopts the power line communication standard "X10" and the on-off-keying modulation technology is functional without complex micro-processor control.

V. DISCUSSION

In the situating low operation frequency, OOK incorporated with an appropriate filter can help to solve the noise problem. Moreover, this can help to determine the digital signal "1" and "0". The transformer incorporated with a series capacitance form a low pass filter at the secondary winding side. The line-driver block allows the output level of the LPF to obtain a level necessary to connect directly to the power-line medium, without the use of external amplifiers and buffers. The line driver can drive low resistive loads. In general PLC system is mainly used on transmitter massive data with high speed. Such system usually requires a computer for data transmit and receiving. By the use of OOK system, we can transmit data without the use of a computer. Moreover, the OOK system can use the power-line for data transmission in order to have a simple control system-lighting equipment and sprinkler system for example.

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