Advanced Silicon Interposer for High density and High Integration Electronic Packages

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[2] Weisti(Worldwide Electronic Integrated Substrate Technology Inc)

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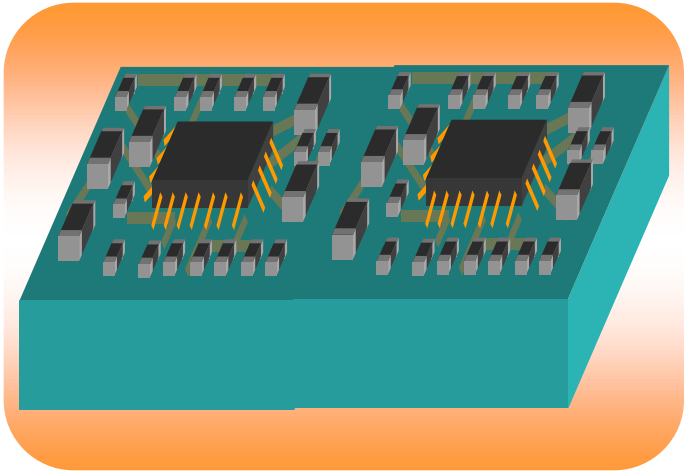
Technical Background

Electronic products:

Smaller and lighter

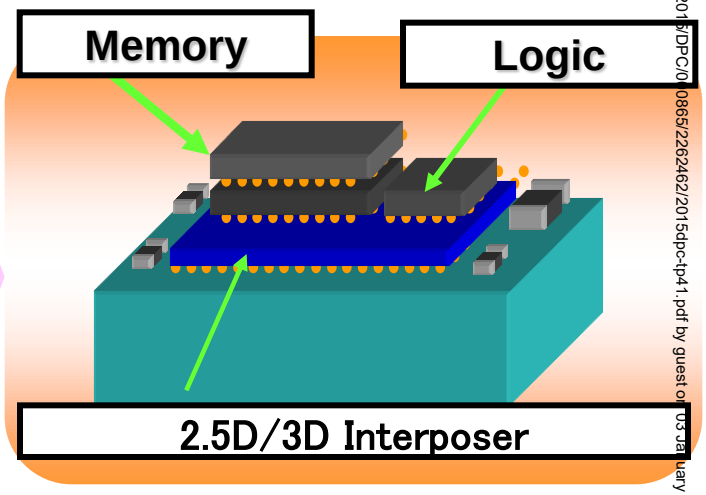
Increasing function



Lower power

Small form factor

Wide I/O



2.5D/3D vertical integration

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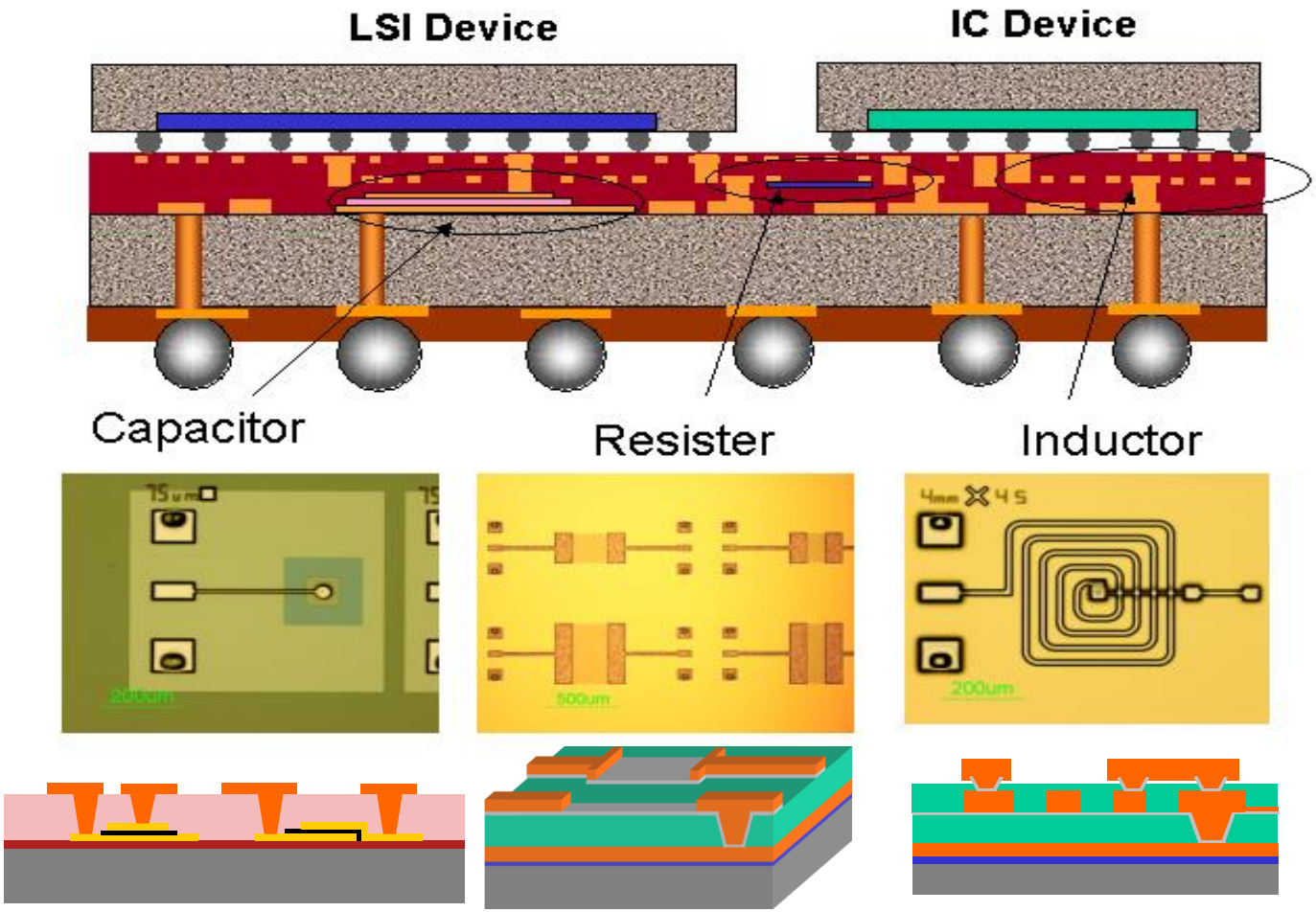
Concept of development



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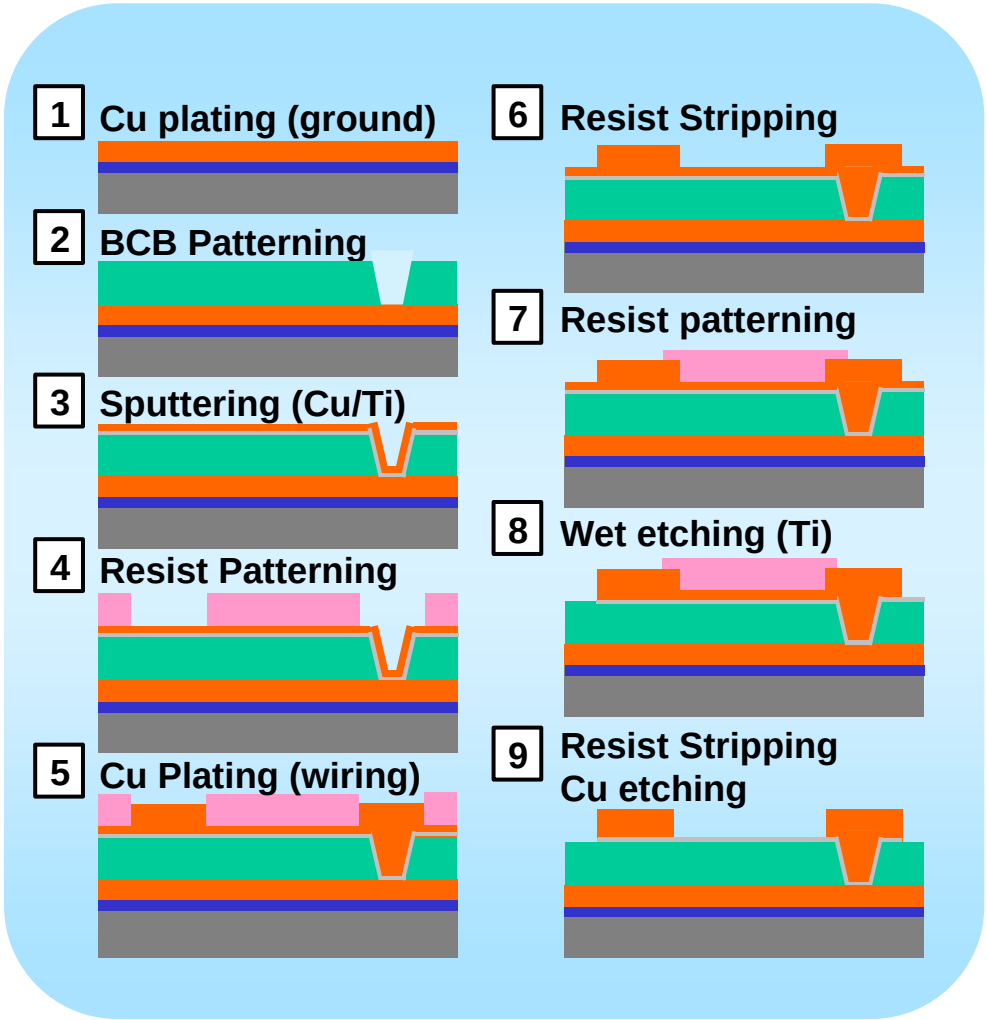
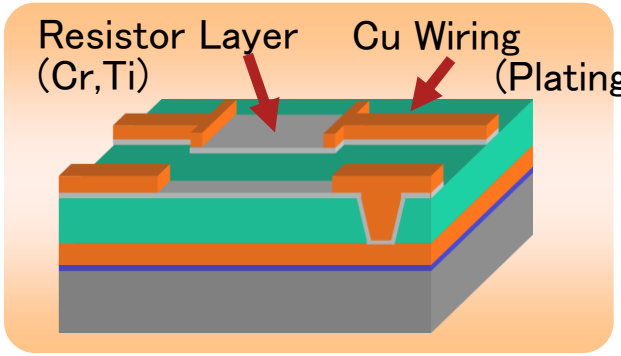
Thin film Resistor

Process flow





Adhesion and barrier layer
in sputter semi-additive process
is applied as resistor.

Both resistor and wiring
can be produced
in the same process step.

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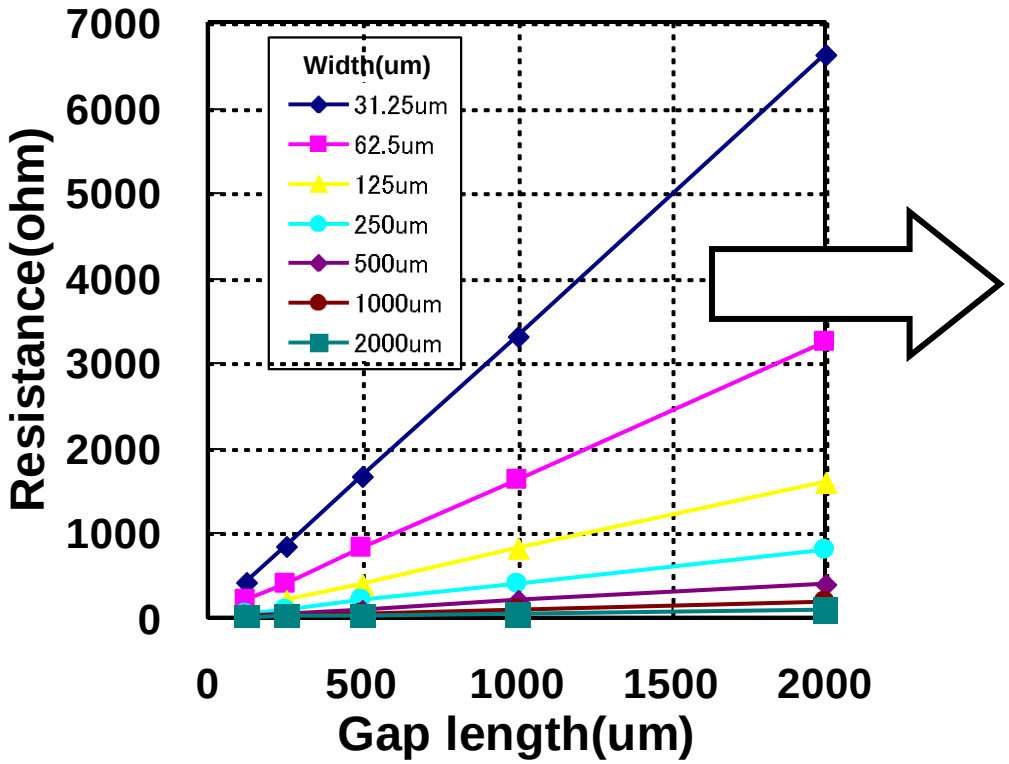
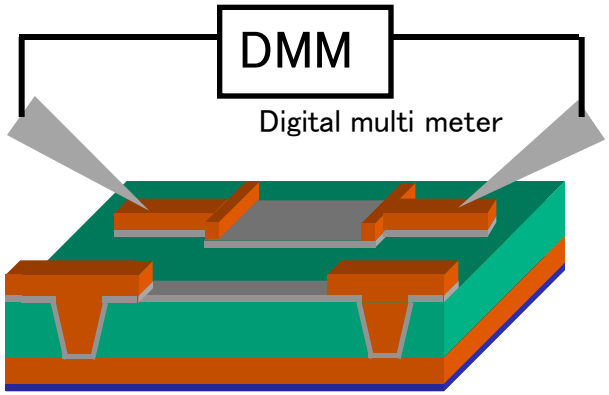
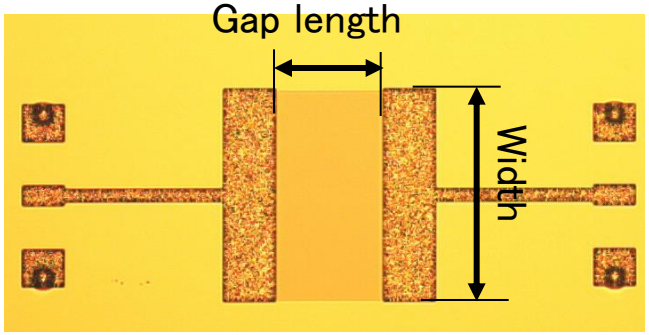
Thin film Resistor

Ti film resistor

Film thickness : 15nm







Resistance

Min : 6.3ohm
(Gap length : 125μm
width : 2000μm)

Max : 6630ohm
(Gap length : 2000μm
width : 31.25μm)

Resistivity(average)

1.5×10^{-6} [ohm・m]

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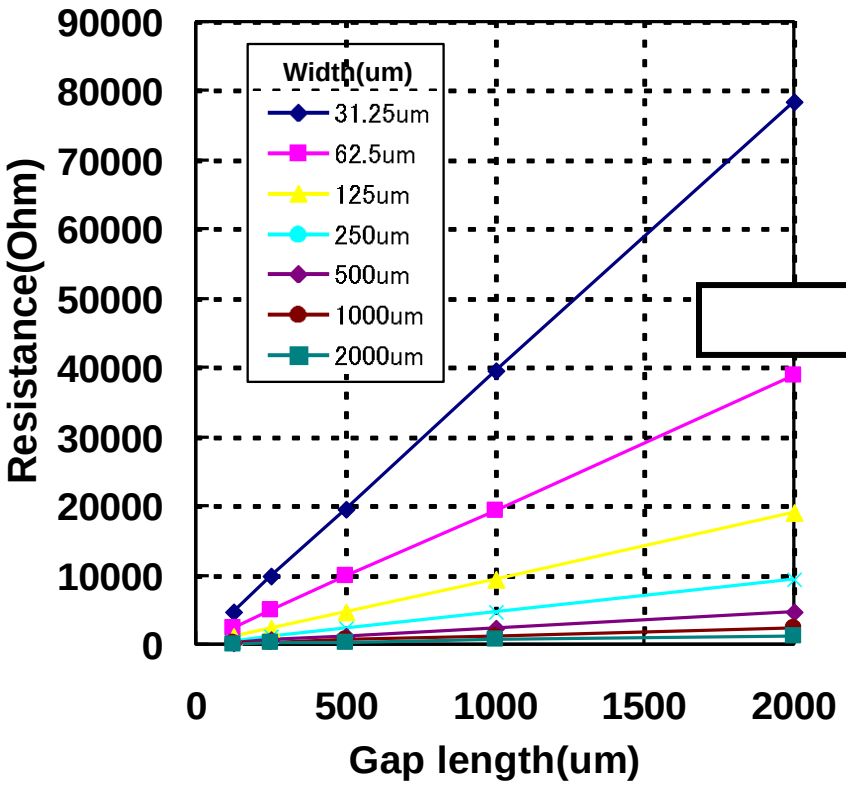
Thin film Resistor

Cr film resistor

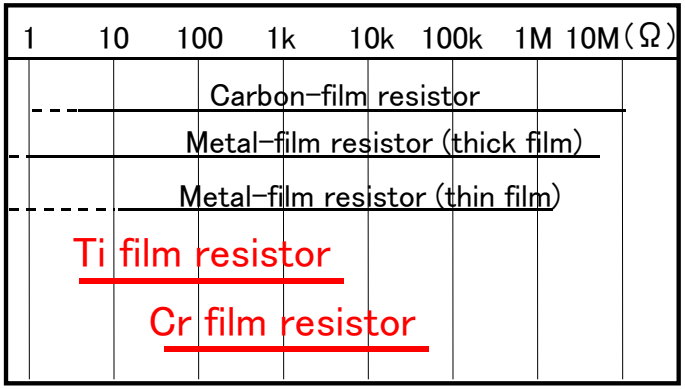
Film thickness : 20nm



Resistance

Min : 77.8ohm
(Gap length : 125μm
width : 31.25μm)

Max : 78000ohm
(Gap length : 2000μm
width : 31.25μm)



Resistivity(average)

2.3×10^{-5} [ohm·m]

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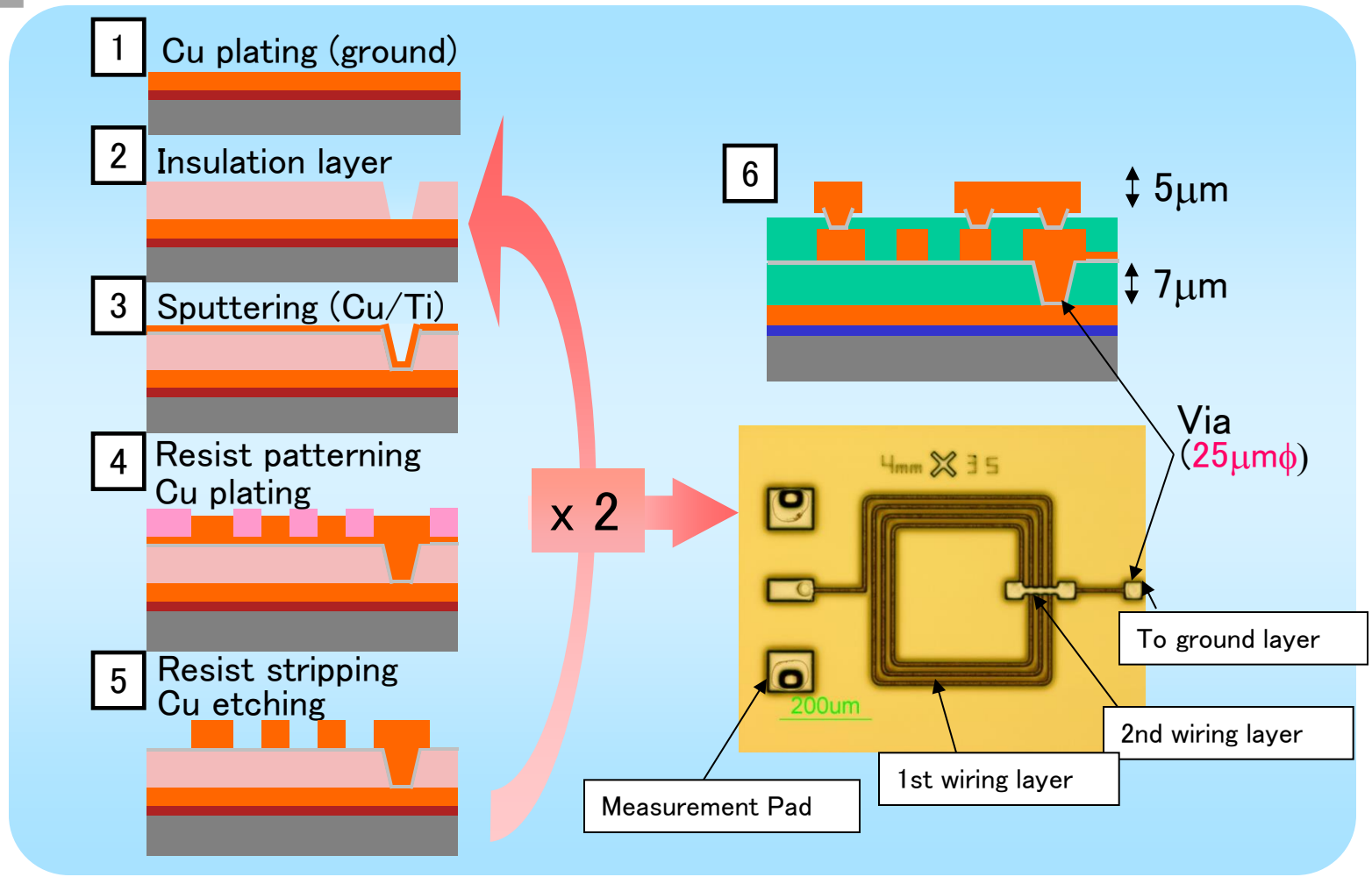
Spiral Inductor

Process flow



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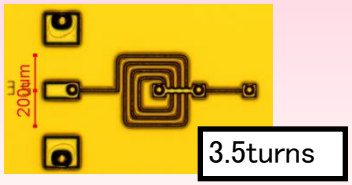
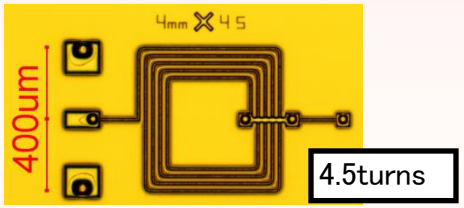
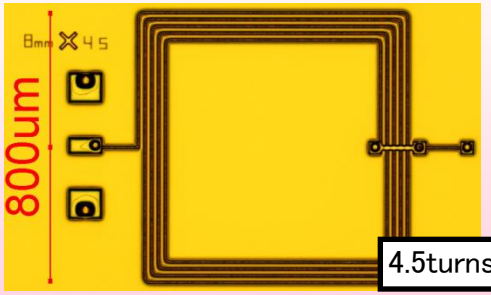
Spiral Inductor

TEG pattern

Size	Line width	Number of turns	(wiring length) (um)	Pattern (typical)
200um□	1st layer ⇒10um 2nd layer ⇒20um	1.0	974	
		2.0	1519	
		3.0	1903	
		3.5	2025	
400um□	1st layer ⇒10um 2nd layer ⇒20um	1.0	1874	
		2.0	3219	
		3.0	4403	
		3.5	4801	
		4.5	5774	
800um□	1st layer ⇒10um 2nd layer ⇒20um	1.0	3674	
		2.0	6619	
		3.0	9413	
		3.5	10410	
		4.0	12027	
		4.5	12674	

The variety of the fabricated spiral inductors are total 15 patterns with changing size ,number of turns and wiring length.

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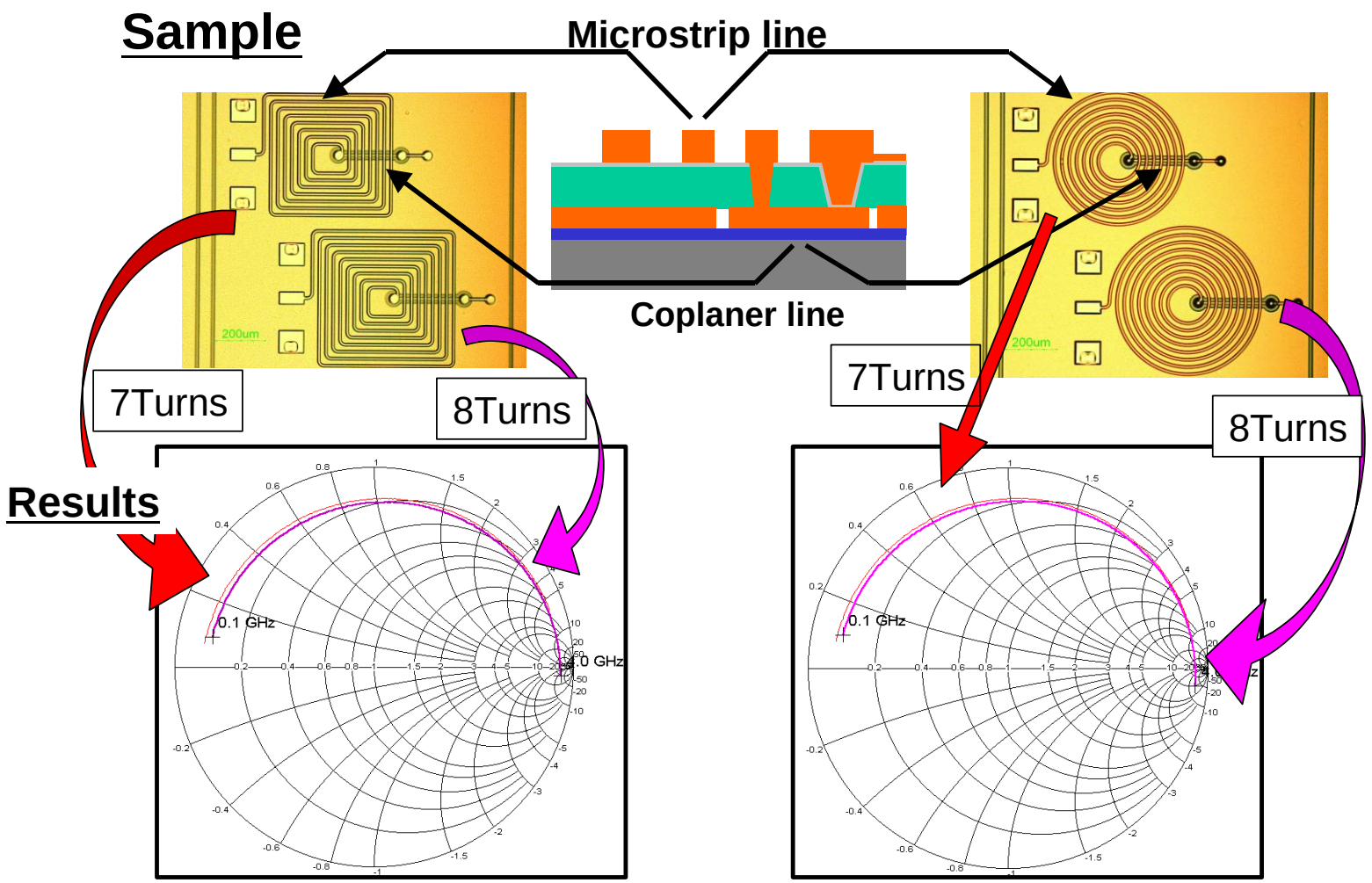
Spiral Inductor



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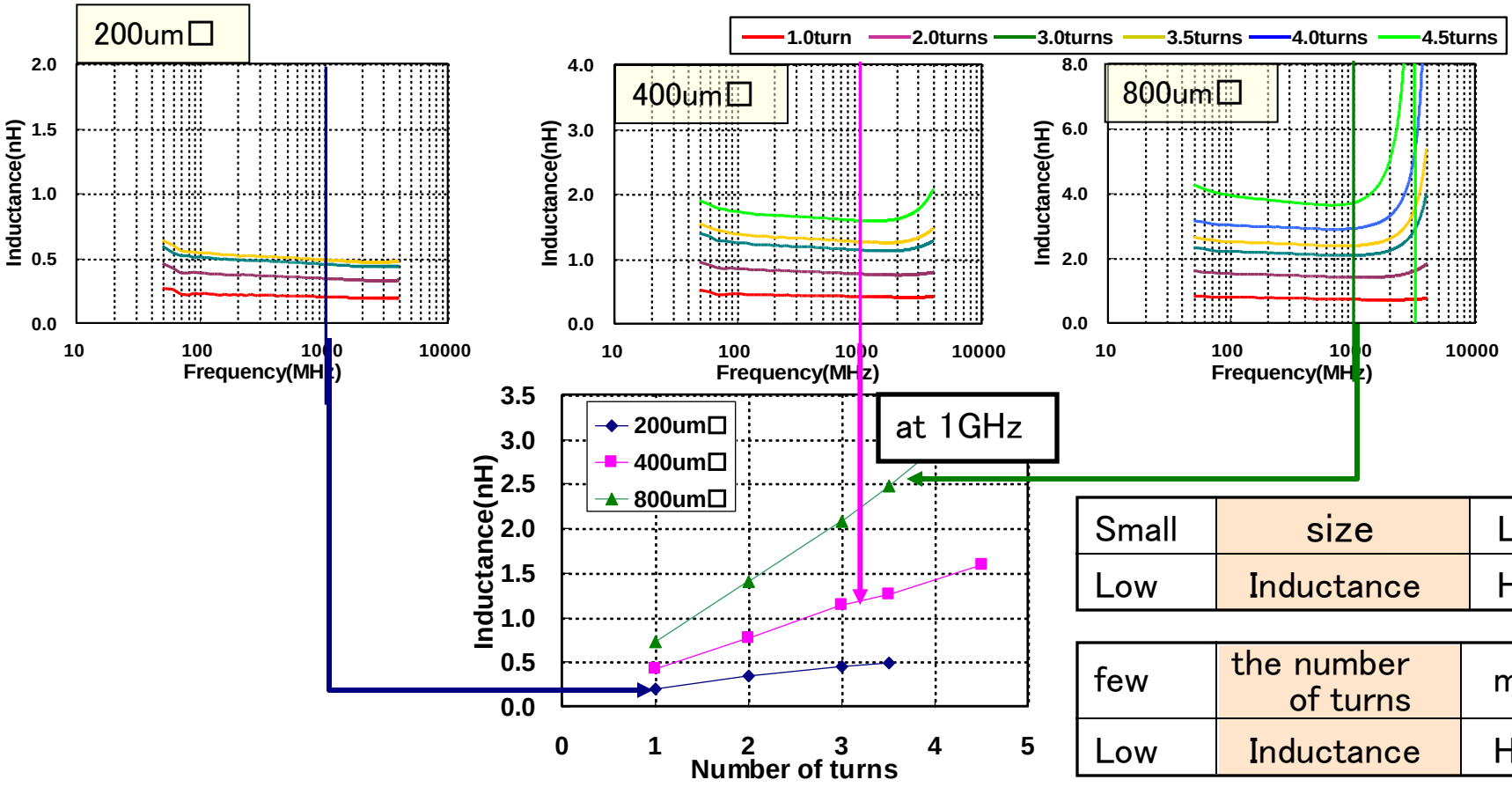
Spiral Inductor

Analysis result (1)

$Z_i = \omega L$

● Frequency vs. Inductance (calculated from S11 smith chart)



Small	size	Large
Low	Inductance	High

few	the number of turns	much
Low	Inductance	High

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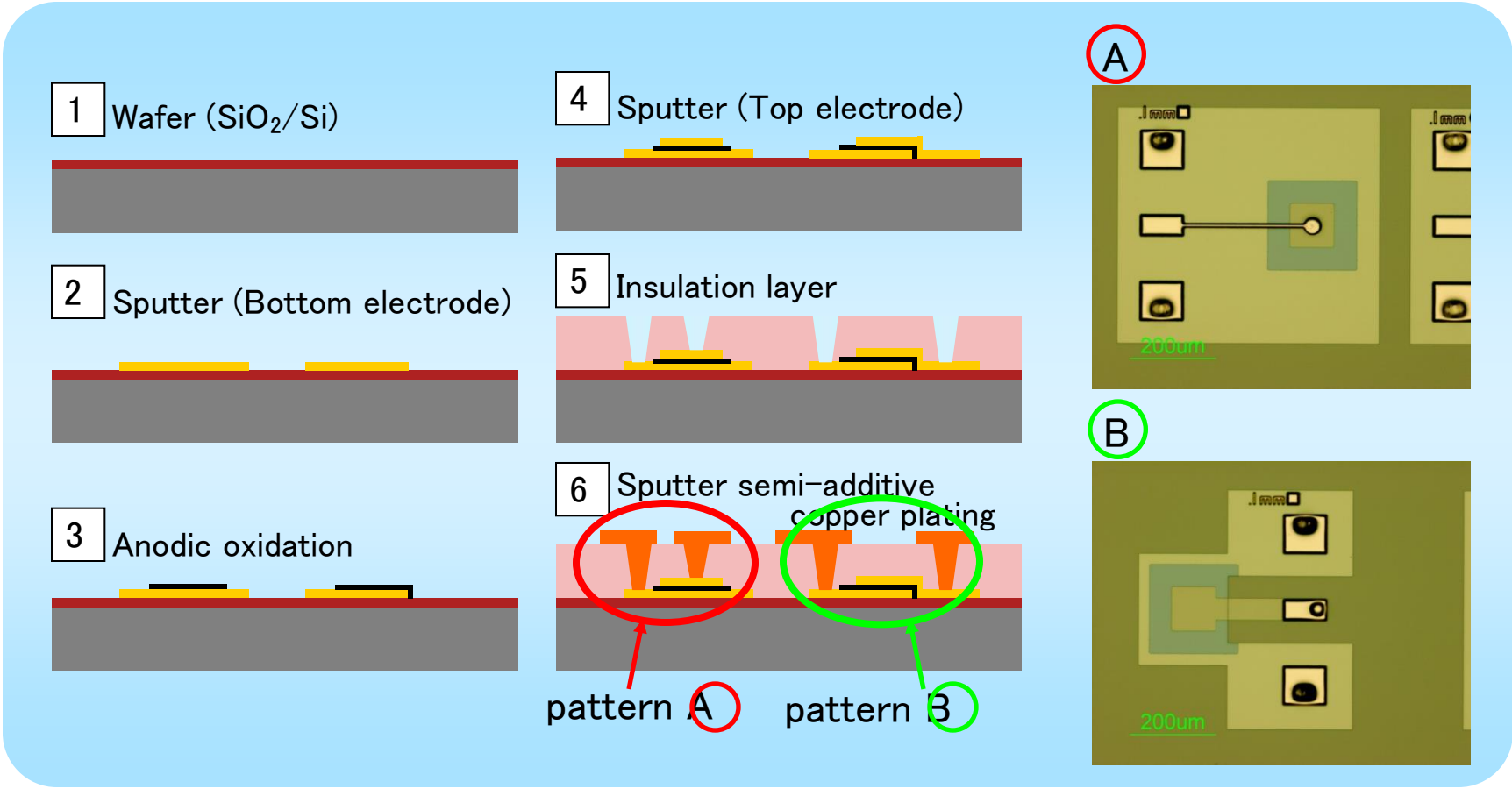
Thin Film Capacitor

Process flow



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Thin Film Capacitor

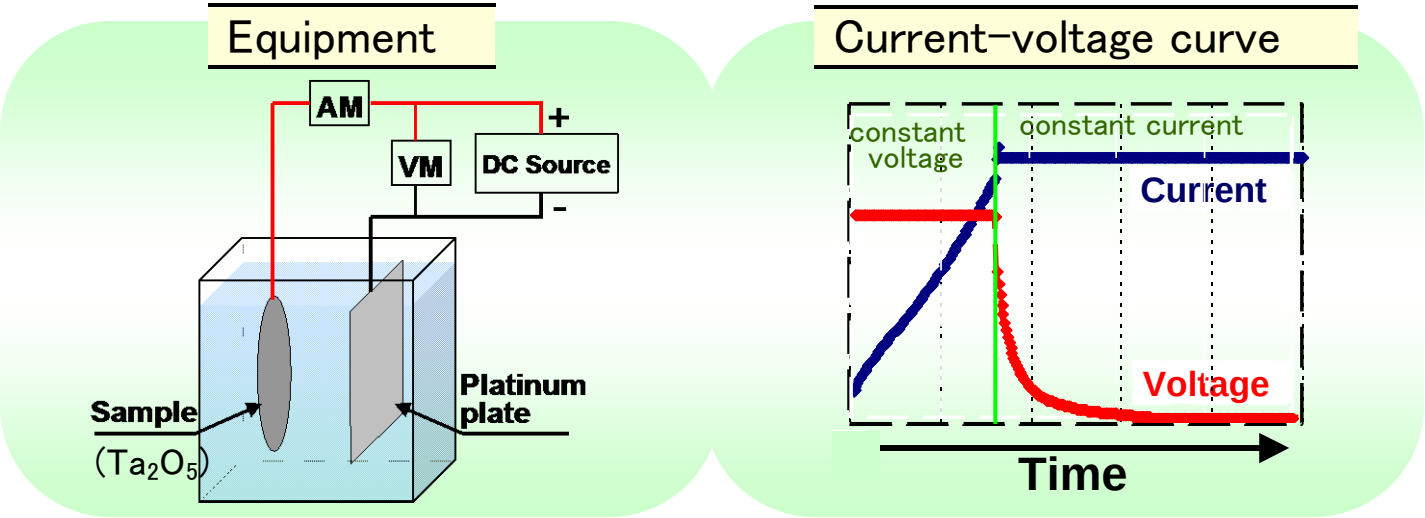
Formation process of Ta_2O_5 film

Anodic oxidation

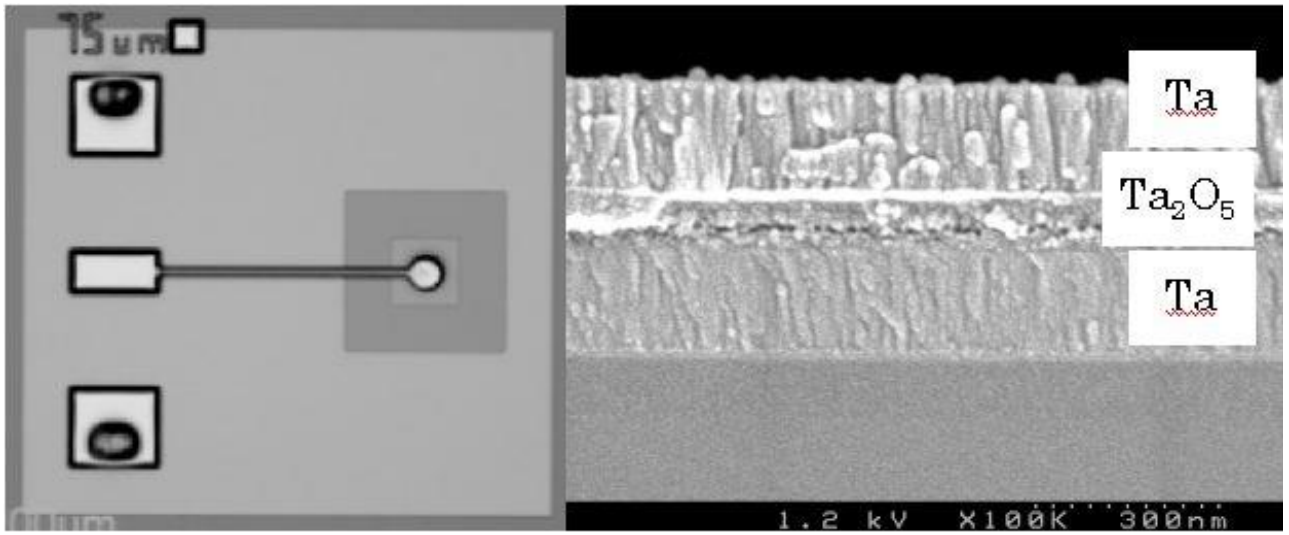
advantages: The oxidized film is stoichiometric (Ta/O=2/5)

The thickness is good repeatability
because the thickness is controlled by applied voltage

The equipment is simple and low price
because vacuum equipment is not used

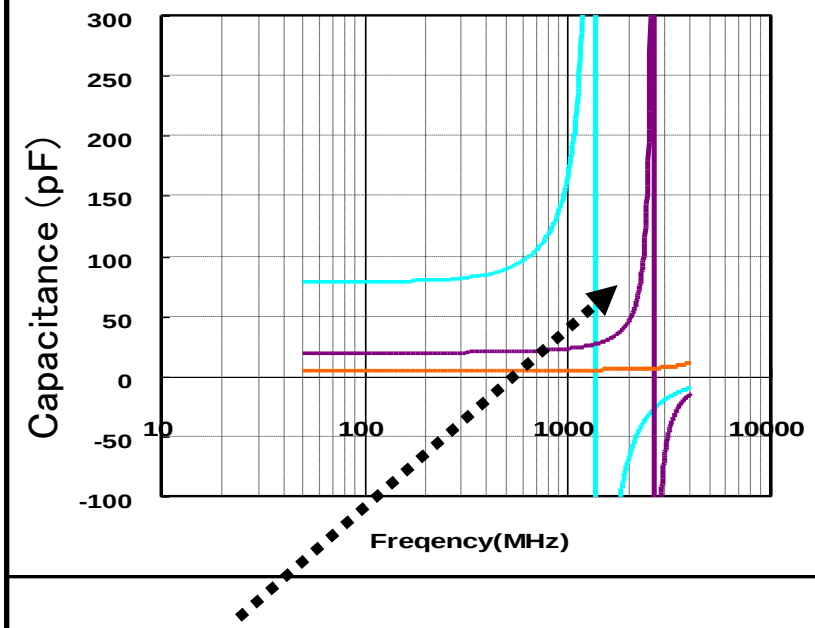
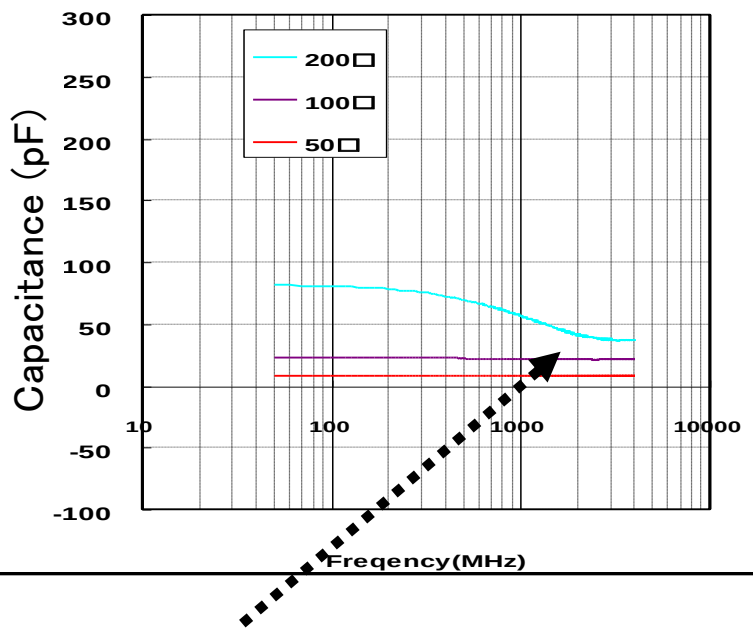


Thin Film Capacitor



Thickness[nm]	Size	Capacitance[pF] (1GHz)	Resonance Point[GHz]
110	50um^2	4.8	>4GHz
	100um^2	19.5	2.58
	200um^2	78.4	1.38
137	50um^2	3.9	>4GHz
	100um^2	15.9	2.97
	200um^2	64.0	1.45
182	50um^2	2.9	>4GHz
	100um^2	11.9	3.27
	200um^2	48.2	1.76

Thin Film Capacitor

Pattern A	Pattern B
	
	
Resonance Point Real Part of Impedance (ESR) = 4ohm	No Resonance Point Real Part of Impedance (ESR) = 30ohm

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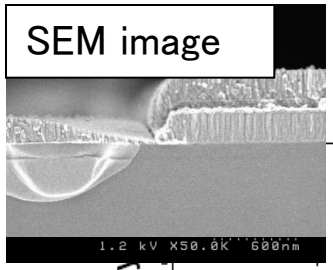
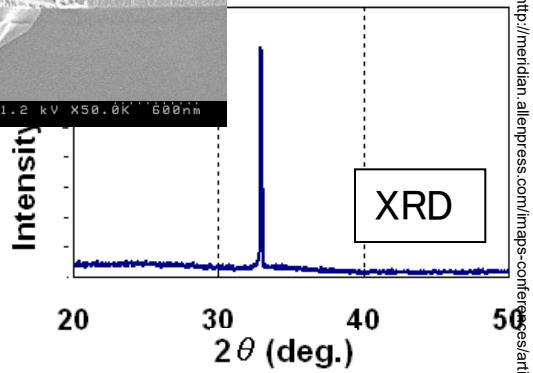
Thin Film Capacitor

The cause of parasitic resistance

1. Bad step coverage

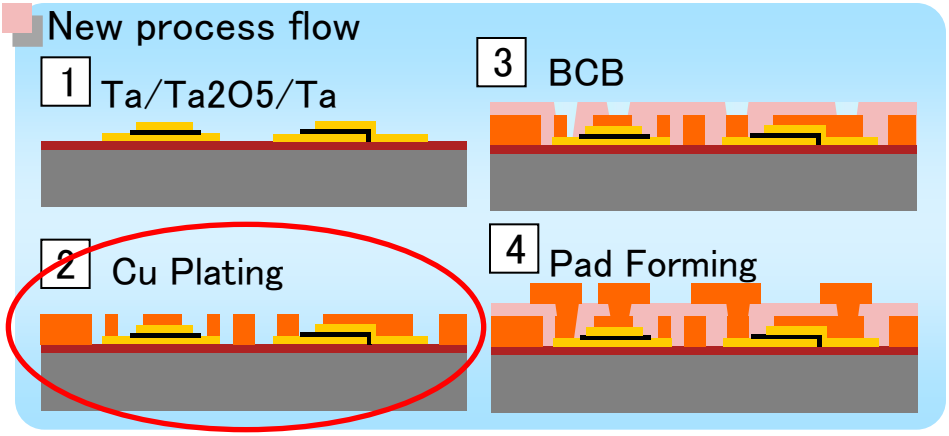
2. Crystalline structure of Ta is Tetragonal
   ->in comparison with bulk Ta(bcc)
   resistivity is more than ten times.





After capacitor forming, we take in "Cu plating" on capacitor electrode.

Apply Gnd forming process



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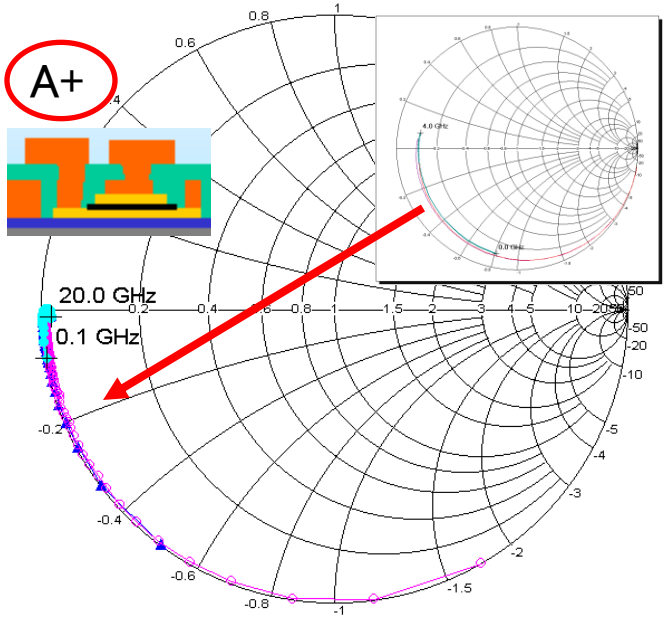
Thin Film Capacitor

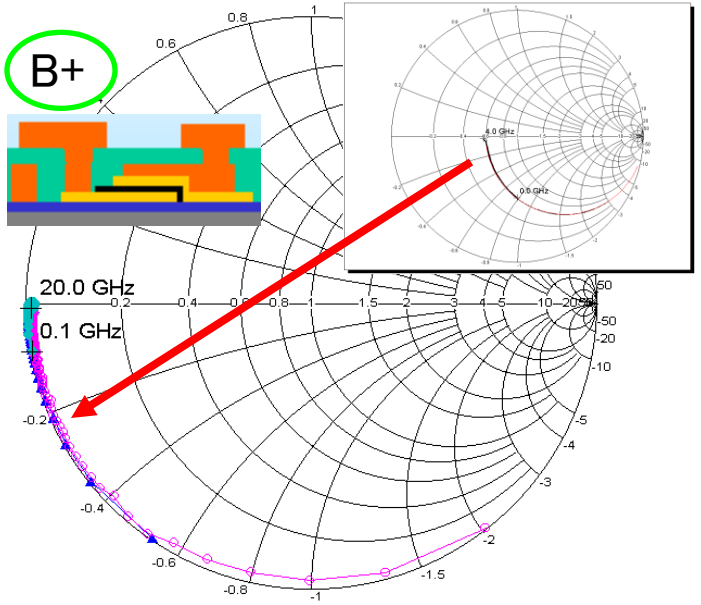
1-port S11 characteristics

Measuring Frequency:
form 0.1GHz to 20GHz

Sample:Dielectric layer thickness = 150nm

Electrode area:100um^2: 200um^2: 500um^2:





Real axis (Resistor) element is decrease
-> Capacitor Characteristics is Improvement

- Dielectric Constant : 21.8

Capacitance (at 1mm^2) = 1.93nF/mm^2 (Thickness:100nm)

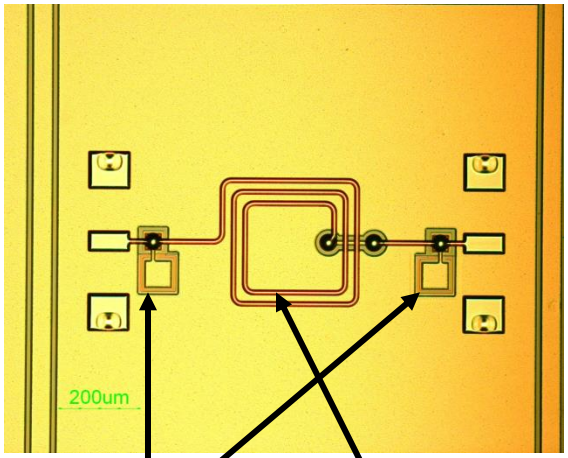
Passive devices

The Characteristic of Individual passive components could be measured.

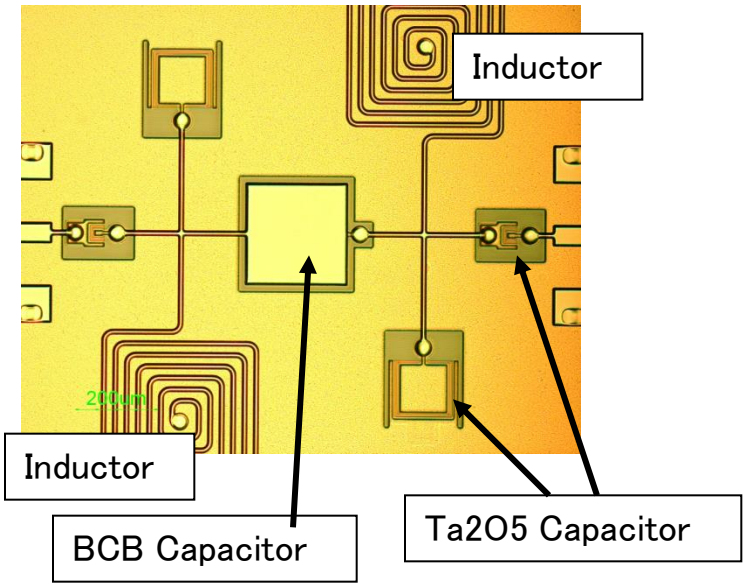
Trial production of integrated LC filter

Sample Picture

Low Pass Filter(LPF)



Band Pass Filter(BPF)



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Passive devices

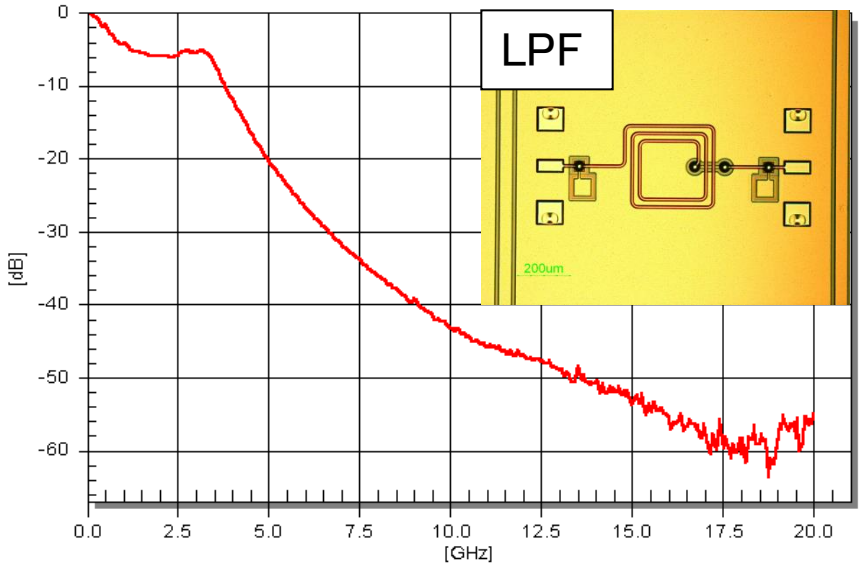
Measurement Result –S21 measurements using VNA

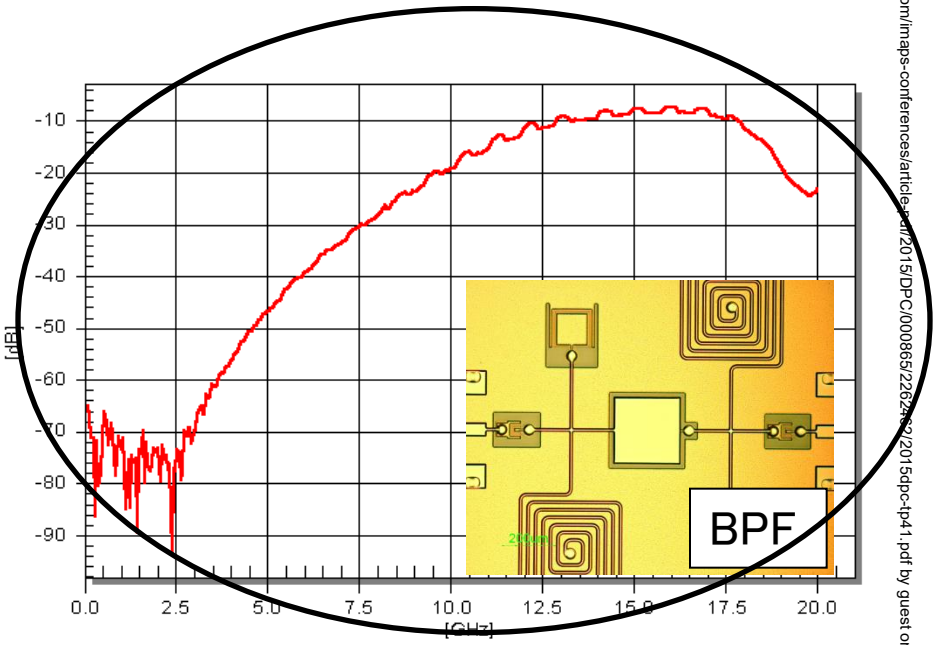
Range : 0.1 ~ 20 GHz

Measurement : S-parameter of S21

Port : 2-port

Calibration : SOLT Method (Short-Open-Load-Through)





Compare to simulation results

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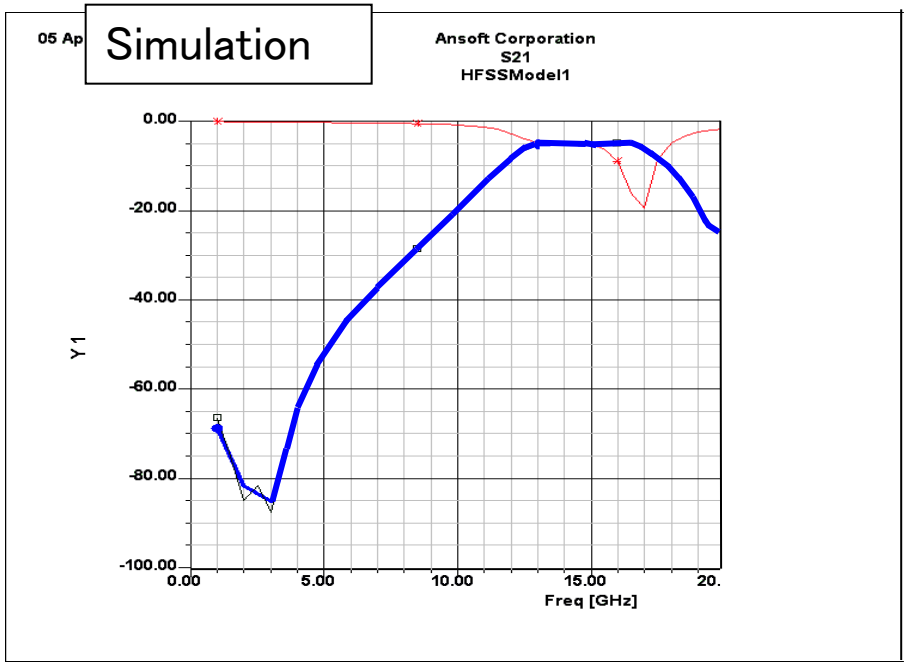
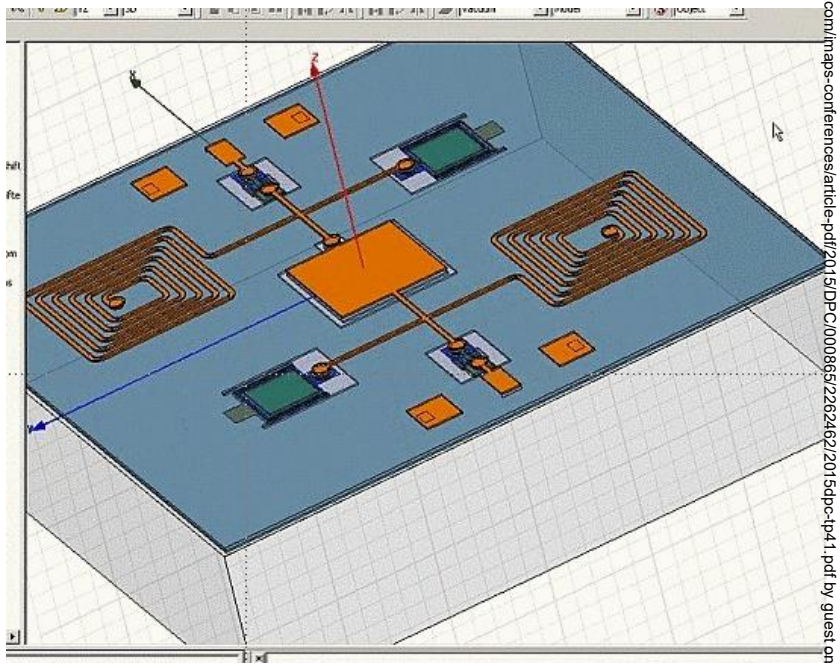
Passive devices

Simulation Result

Simulator：3D Electromagnetic-Field Simulator (FEM)
[ansoft HFSS]



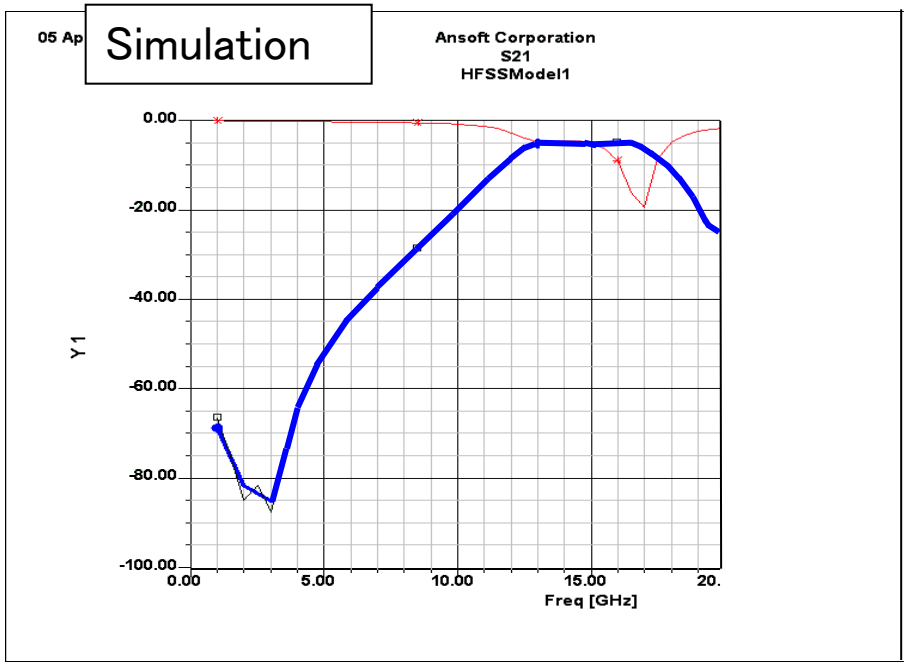


Passive devices

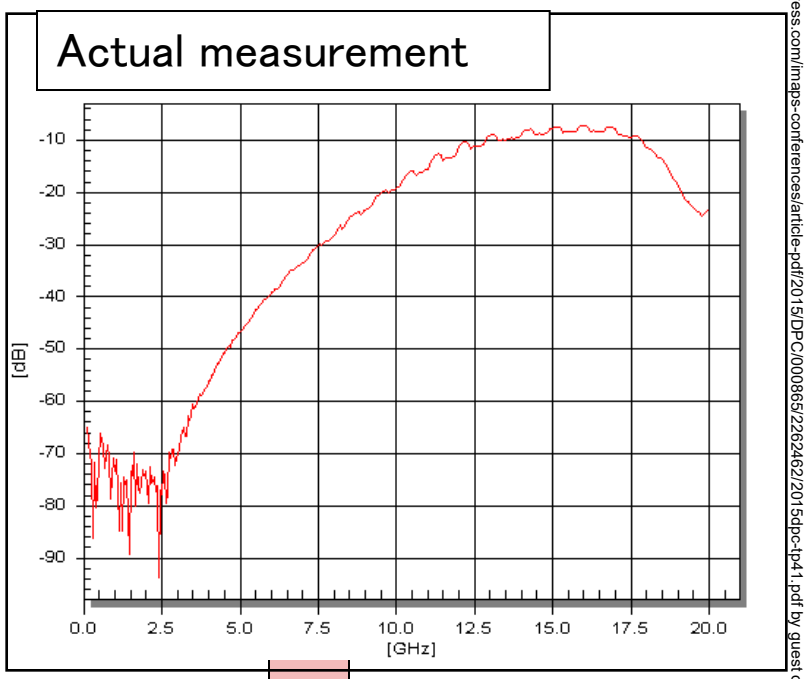
Measurement Result –S21 measurements using VNA

Range : 0.1 ~ 20 GHz
Port : 2-port
Measurement : S-parameter of S21
Calibration : SOLT Method (Short-Open-Load-Through)

Simulation



Actual measurement



Compare to simulation results

The result is in good agreement with actual measurement.

→Our simulation is able to use for filter design

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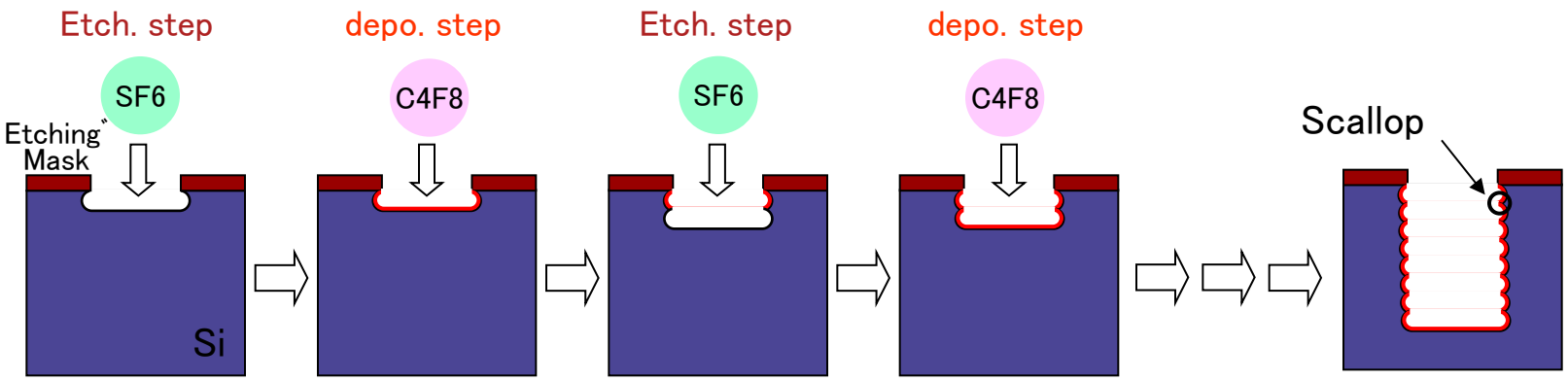
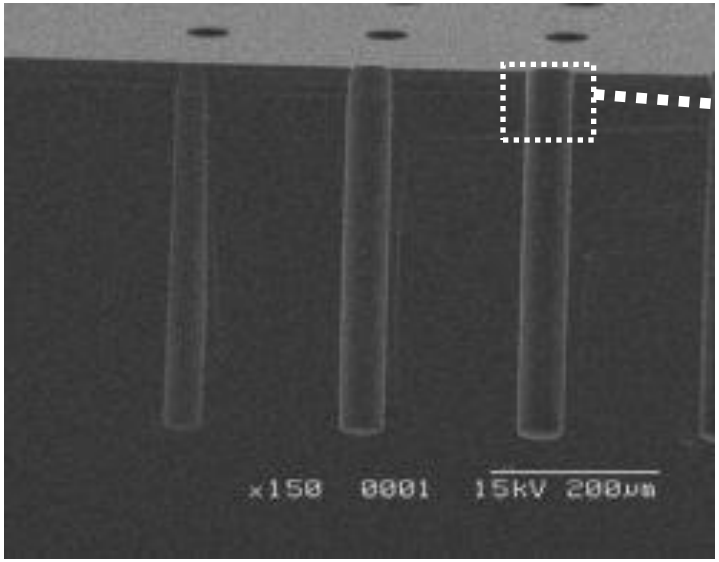
Deep-RIE Bosch Process





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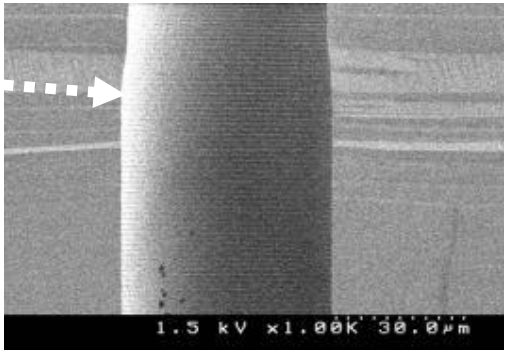
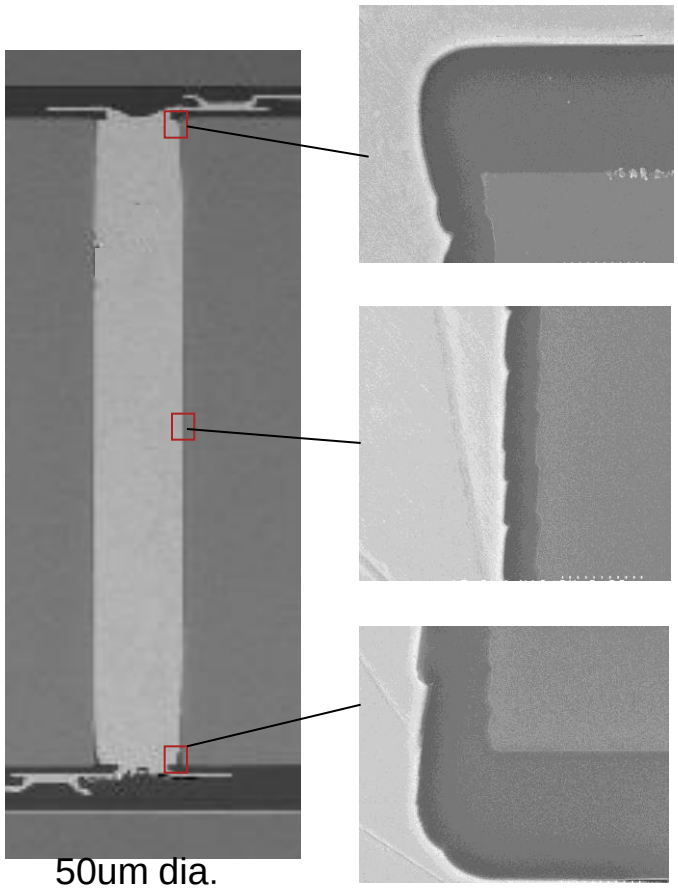


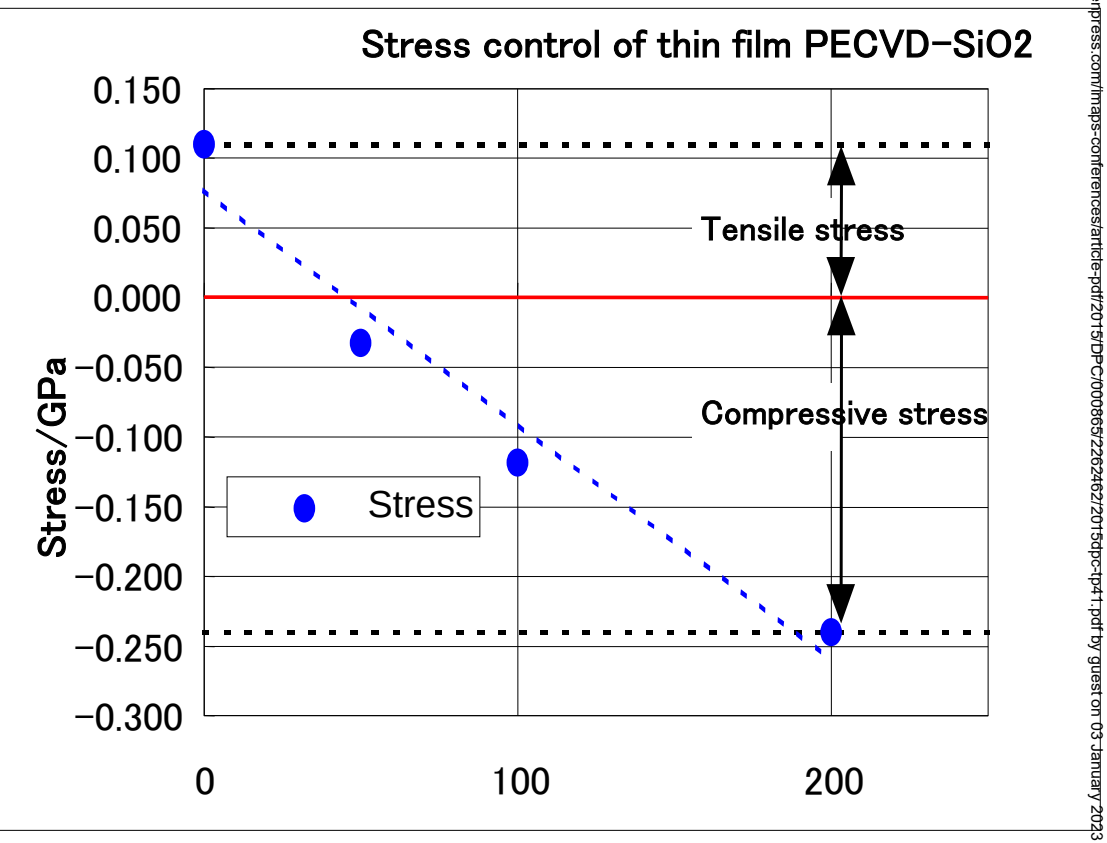
Straight and smoth surface hole

Coverage oxicide of inner holes

-Using PECVD for low stress process-



50um dia.
400um depth



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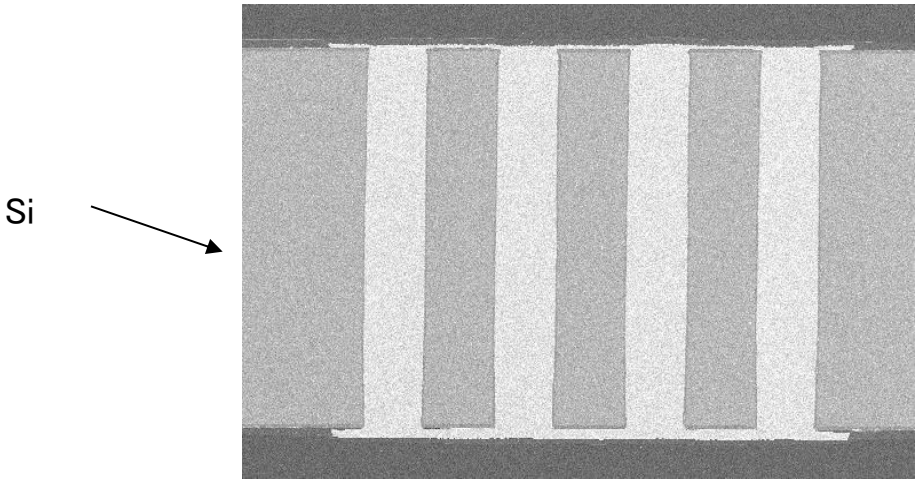
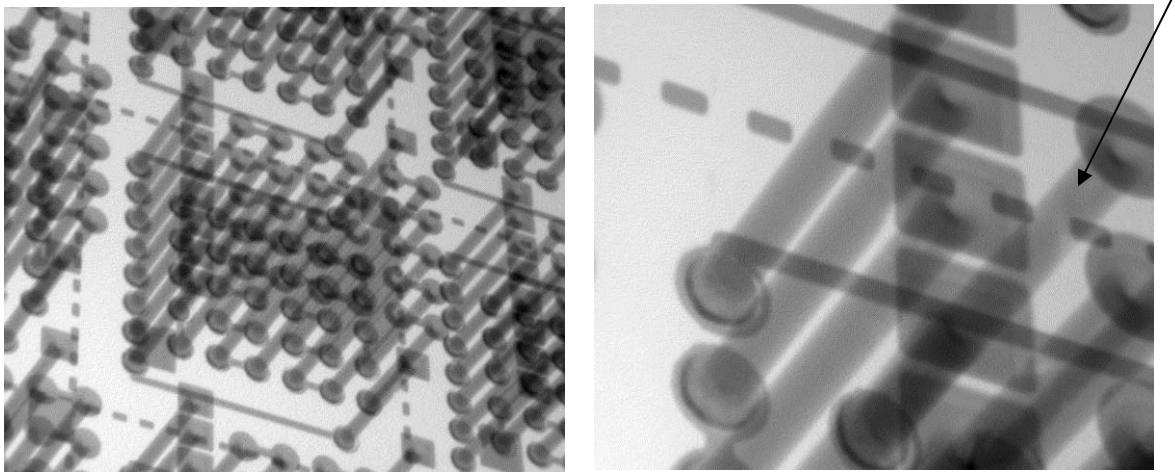
TSV filled with Cu technology

The cross section photograph and the image of X-ray transmission analysis



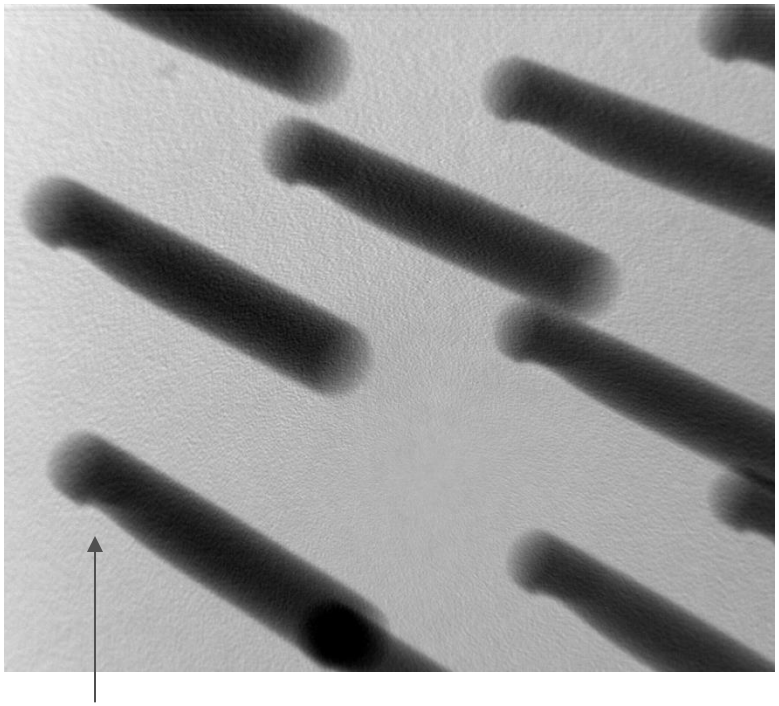
Polished Cross-Section



X-Ray CT Image

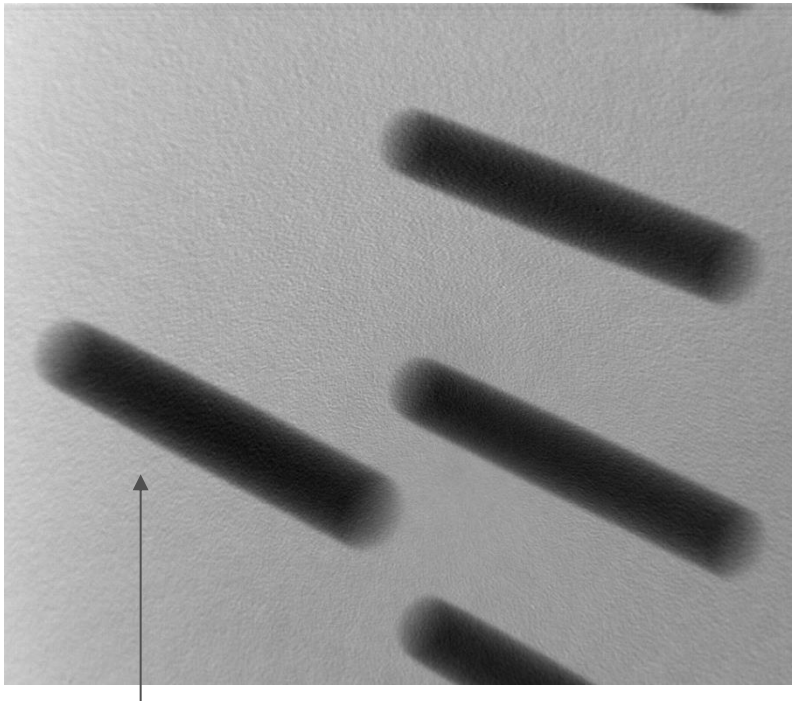
Example of optimized PPR method

Condition A



Void remain in the cupper plug.

Condition B



no voids in the cupper through plug.

Good filling characteristic is obtained by process control with liquid flow and ion delivery and current density in the hole

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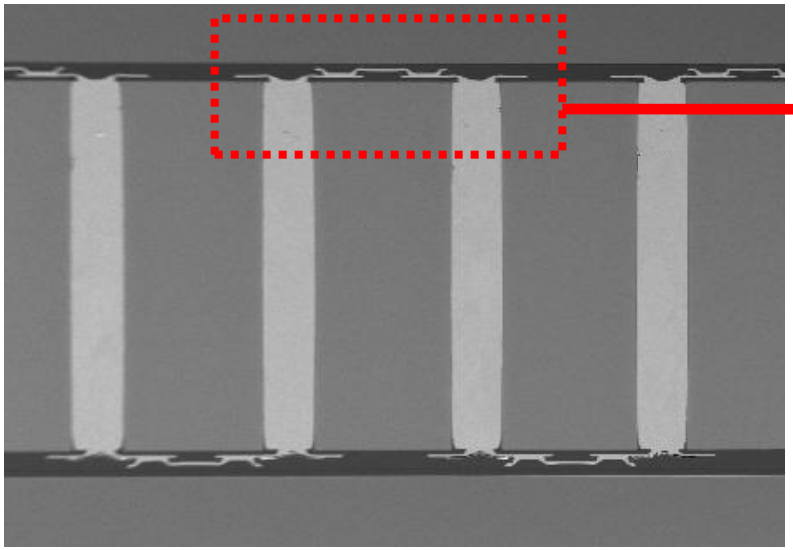
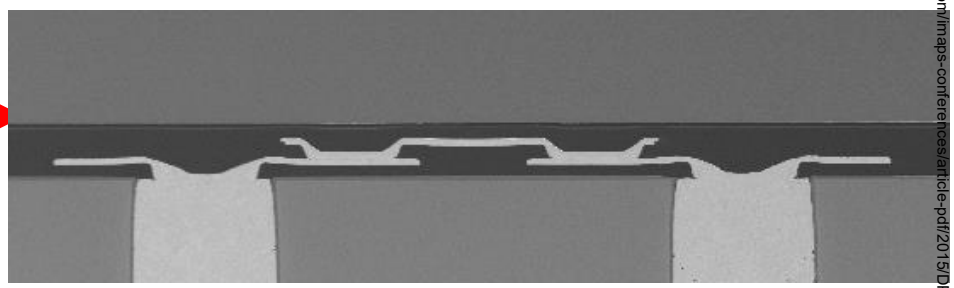
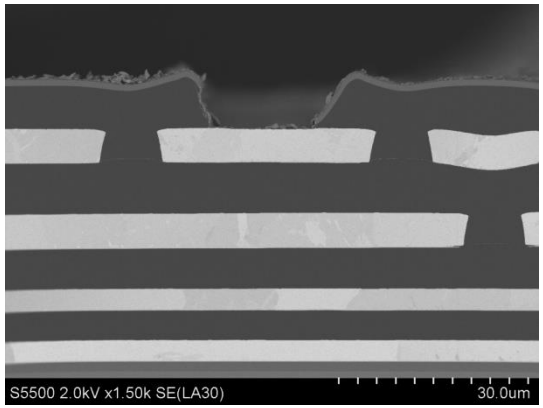
RDL (Re-Distribution Layer)

RDL consists of fine wiring layer formed by SAP(sputter semi-additive process)
Double sided dielectric layer PI formed by the photo-via process







D45 PI
L4 Metal
D34 PI
L3 Metal
D23 PI
L2 Metal
D12 PI
L1 Metal
D01 PI

Up to 4 layers for Metal/PI build up

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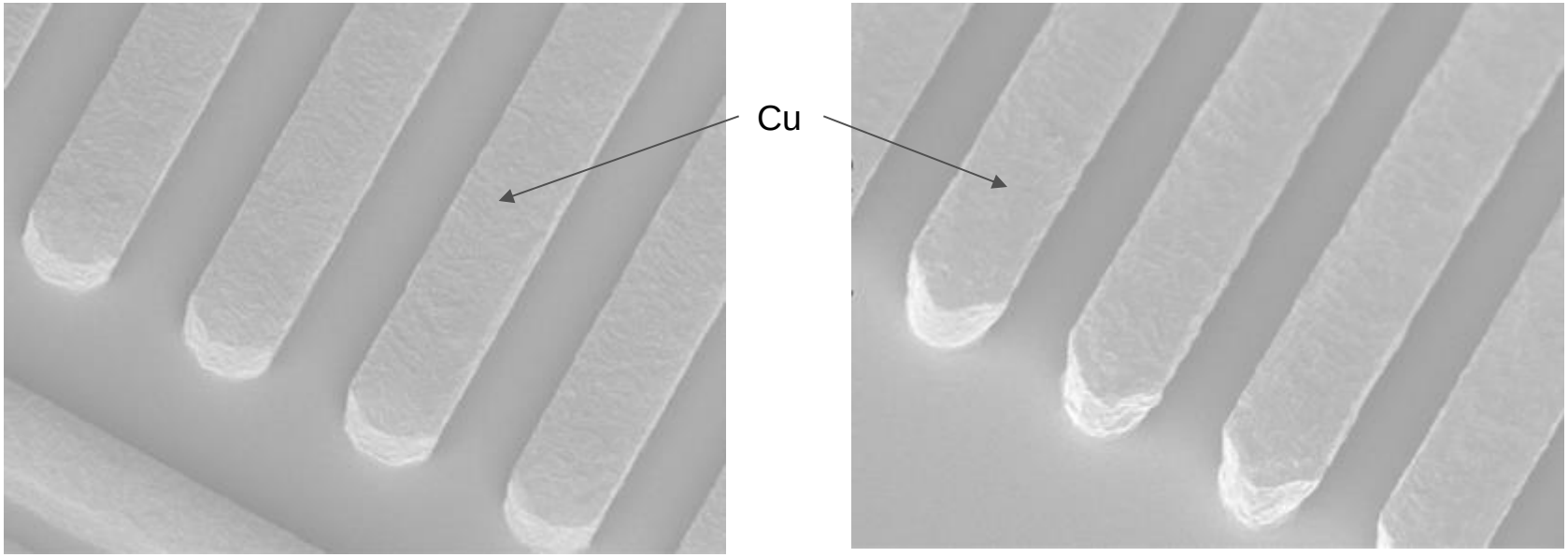
Fine Cu wiring

Fine Cu wiring fabricated by SAP(semi-additive process)



L/S=5um/5um

L/S=3um/3um

DNP

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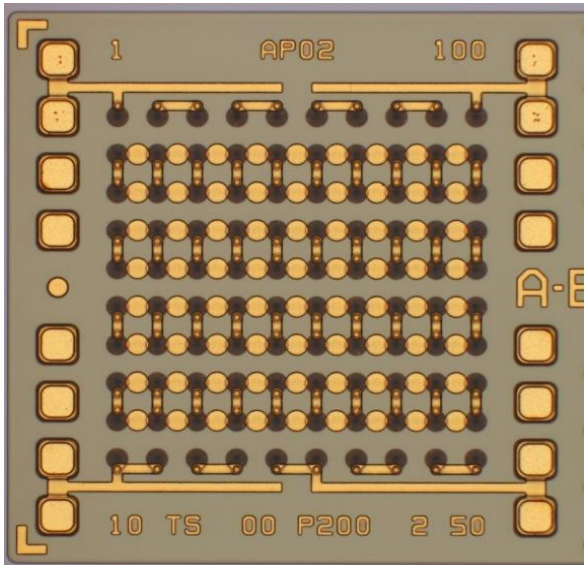
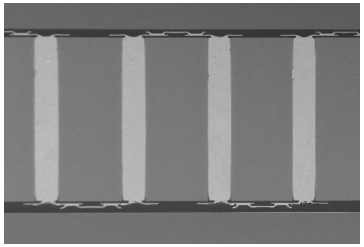
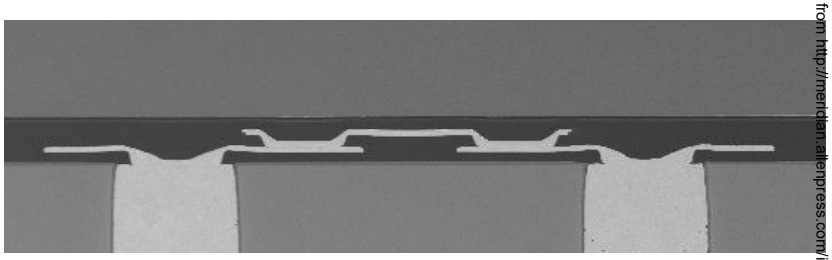
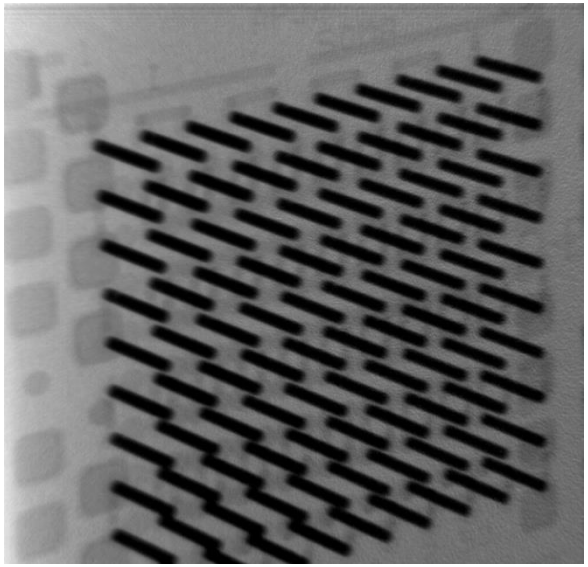
Si Interposer

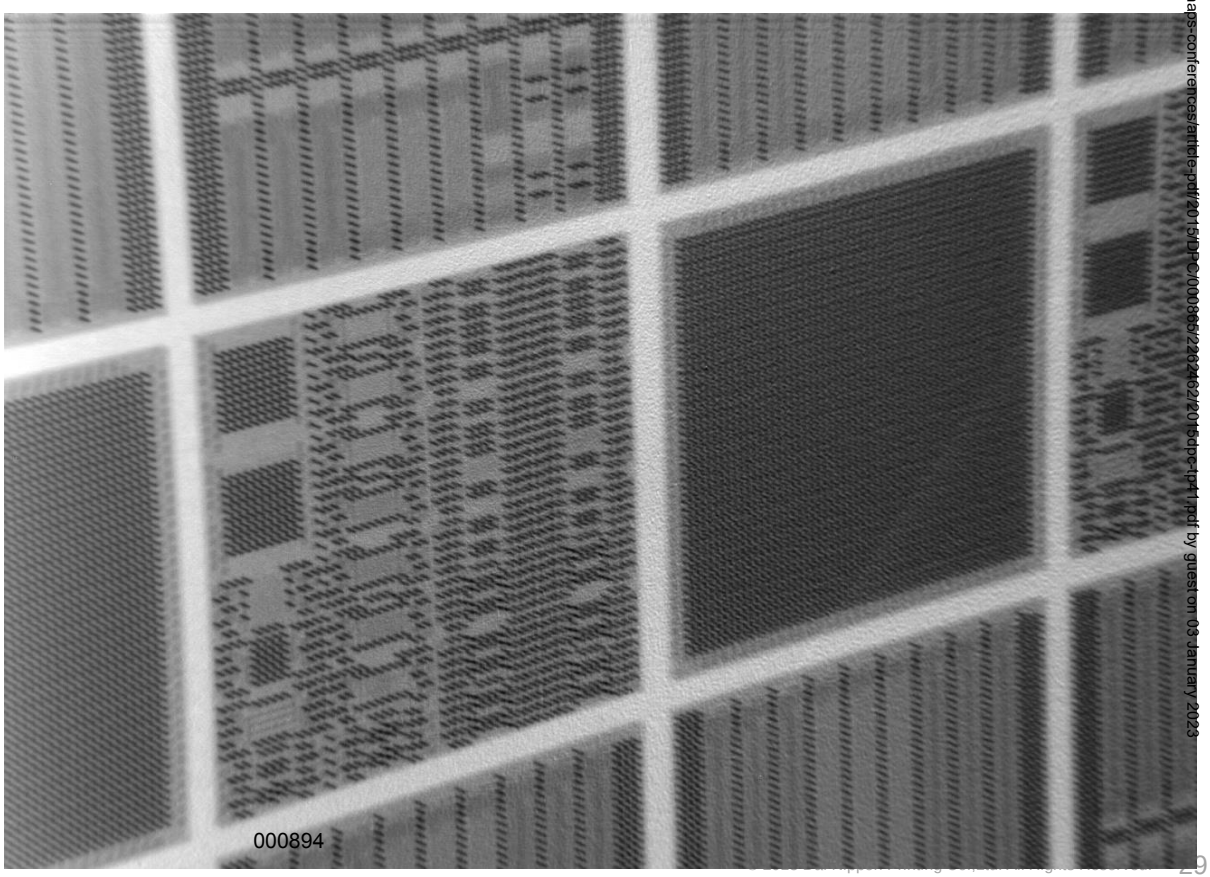
Demonstrated Test Element Group (TEG)







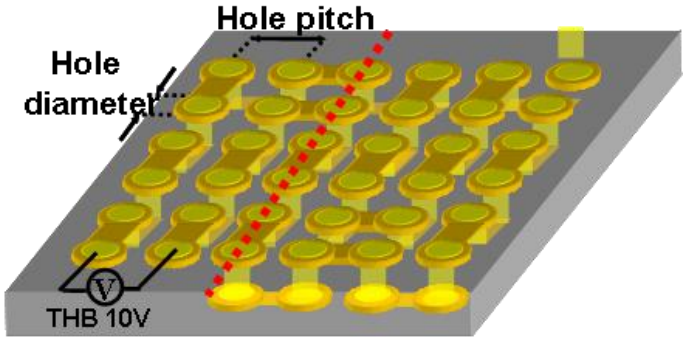


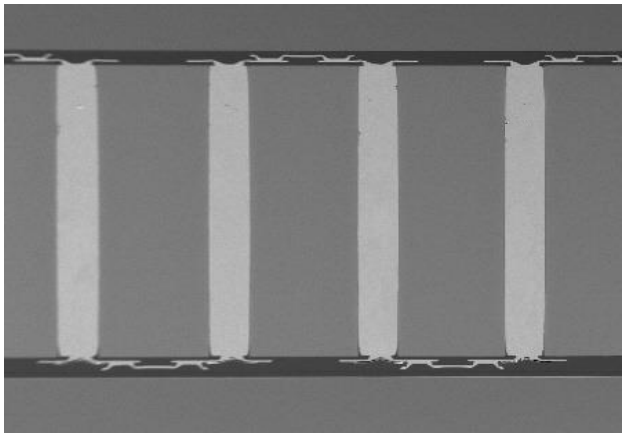


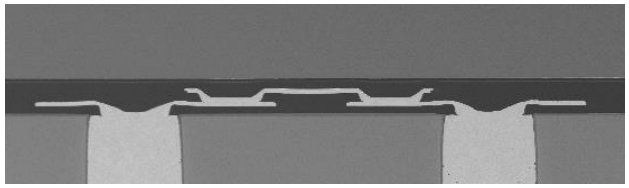
Si Interposer

Reliability test results（THB）using TEG

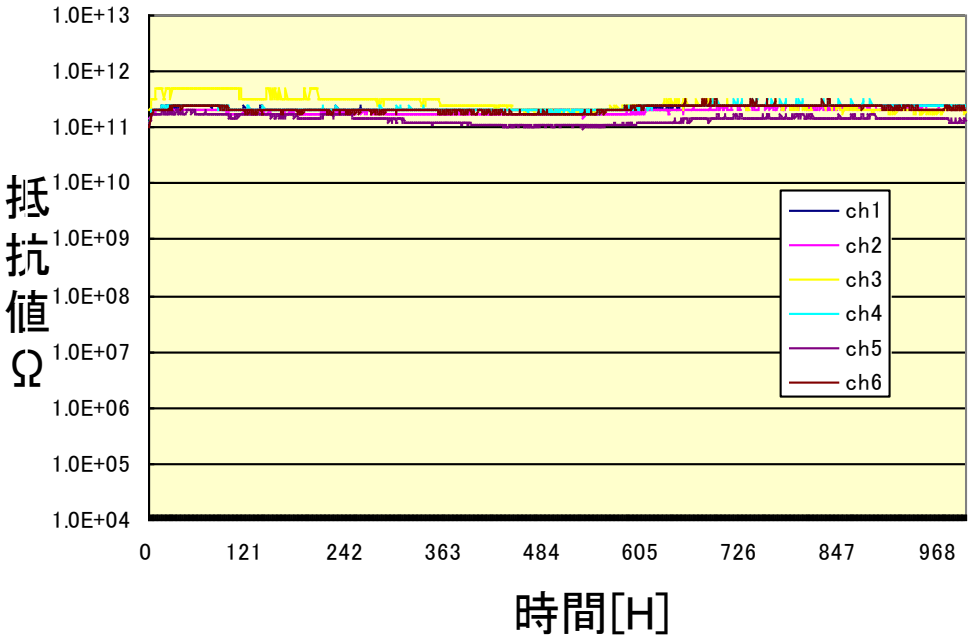
The schematic view of Sample







THB (85℃ 85% 1000hr)



Measurement condition			
Temperature	85℃	Hole diameter	50um
Humidity	85%	Hole pitch	200um
Additive V	10V	Number of Hole	100x2
Measurement V	10V	Time	1000hr

000895

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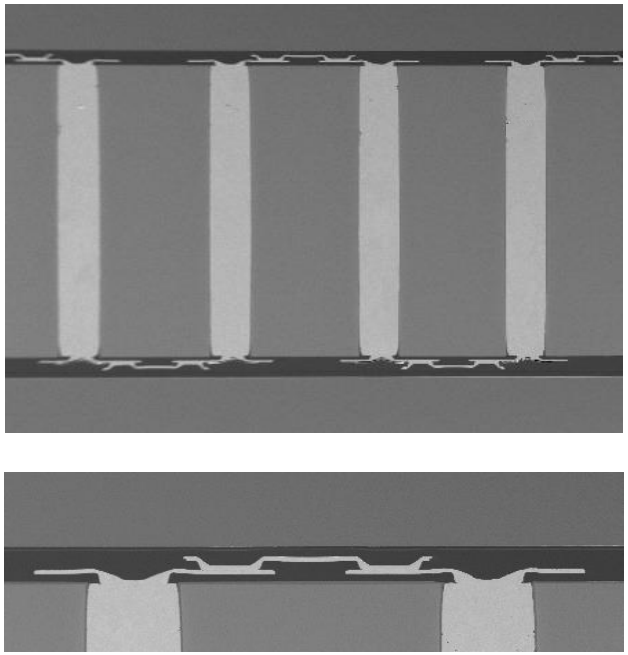
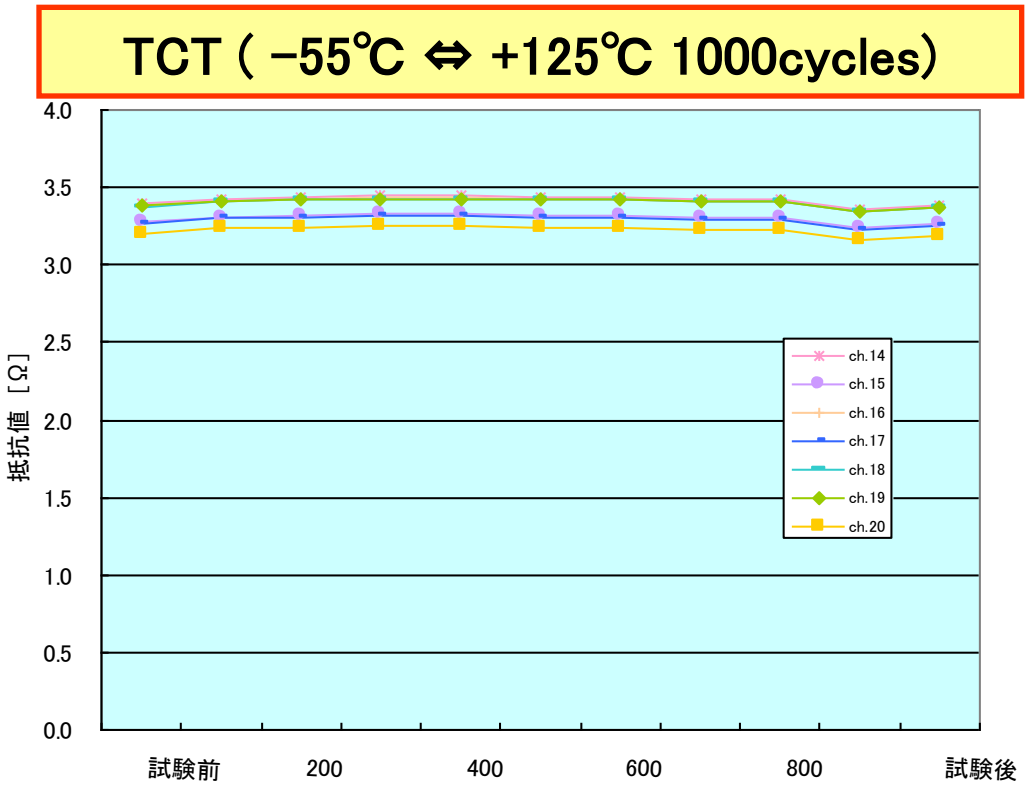
Si Interposer

Reliability test results（TCT）





Measurement condition			
Temperature	-55～125℃	Hole diameter	50um
1cycle time	15min	Hole pitch	200um
Total cycle	1000cycle	Number of Hole	100

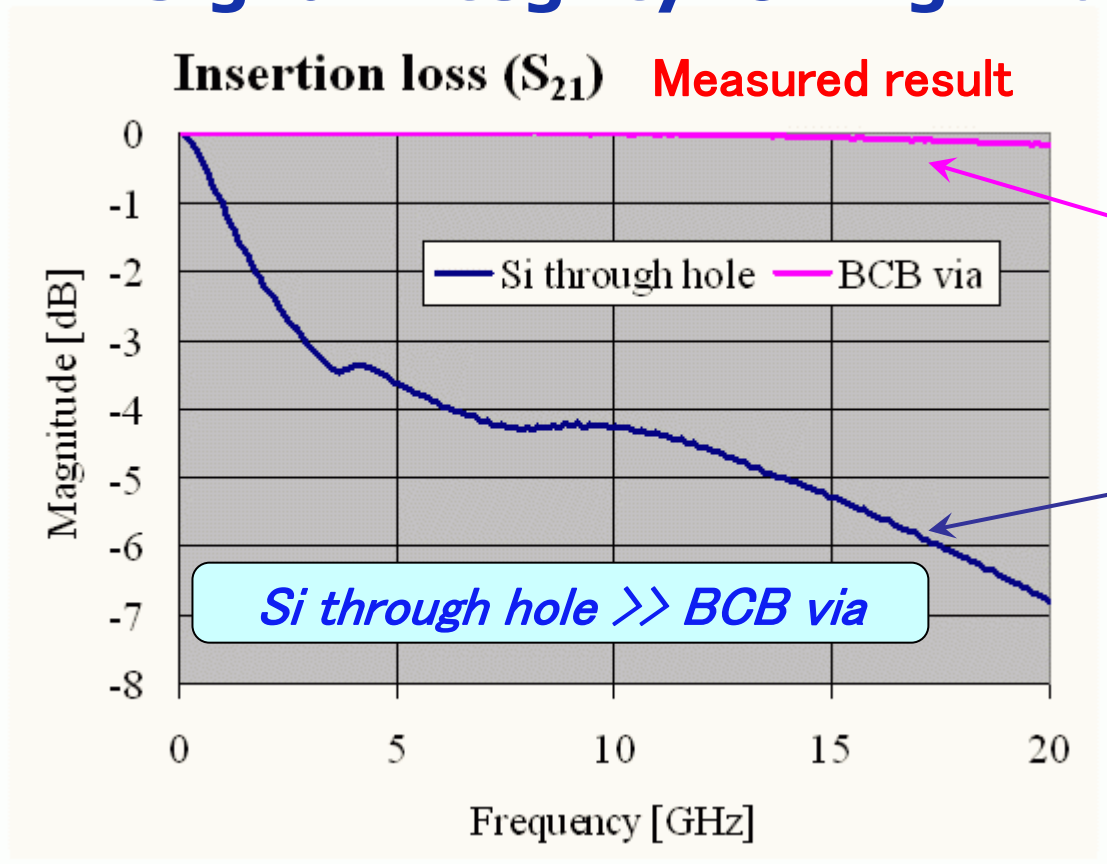
Double side thick polymer insulator that buffers the stress created by CTE mismatch

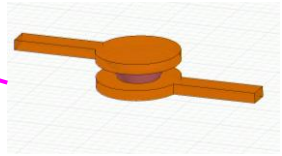
DNP

000896

Si Interposer

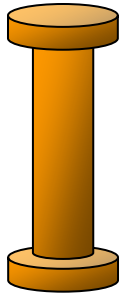
Signal integrity for high frequency





surface via

BCB 8 μ mt
Via 30 μ m



Si through hole

Si 400 μ mt
Via 70 μ m

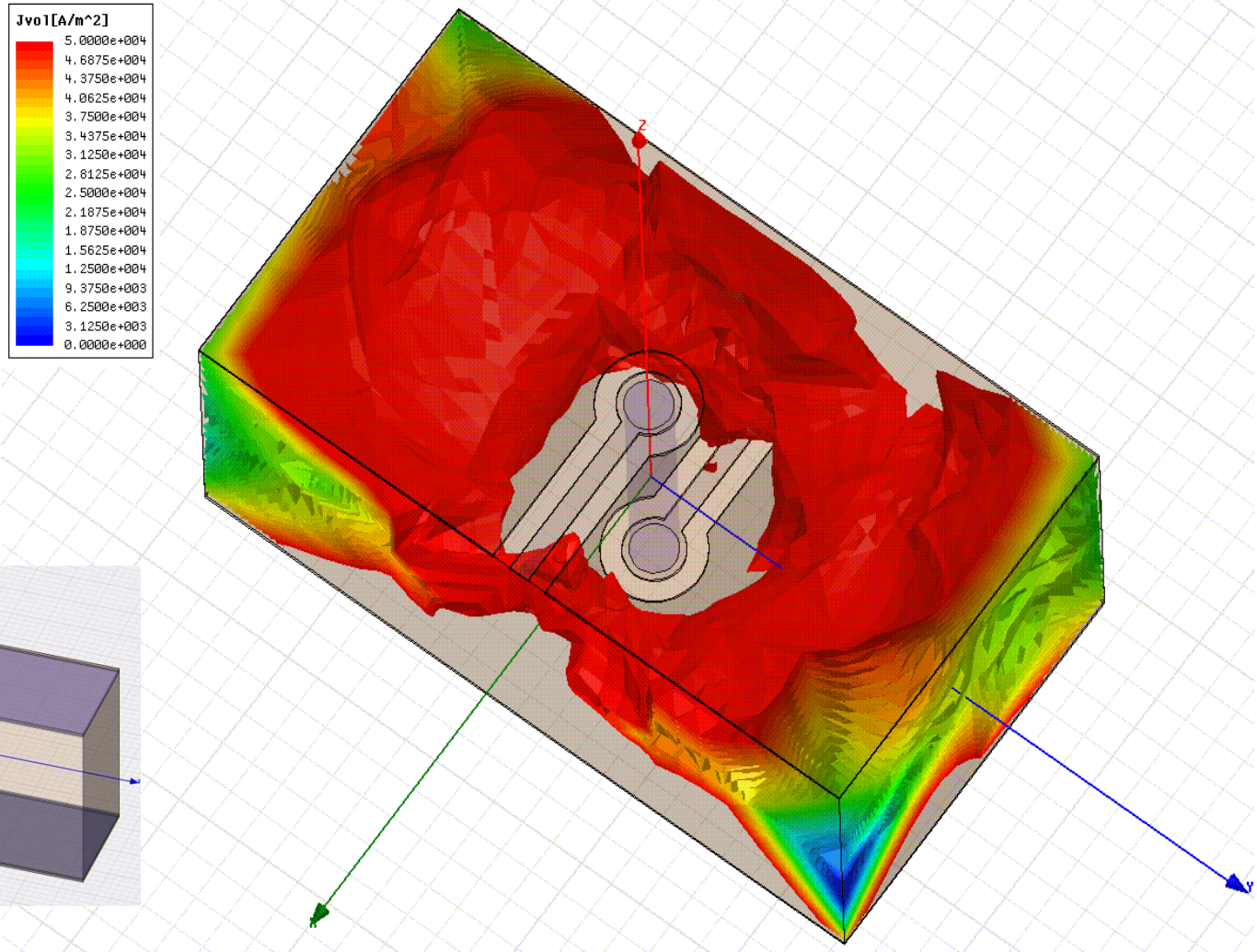
Insertion loss of Si through hole is larger than surface via

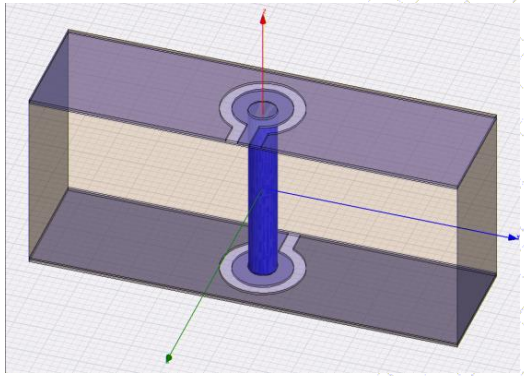
Reducing the loss of Si through hole is very important !

Si Interposer

3D-electromagnetic field simulation

low resistivity (ρ) silicon whose volume resistivity is 1.5Ω·cm



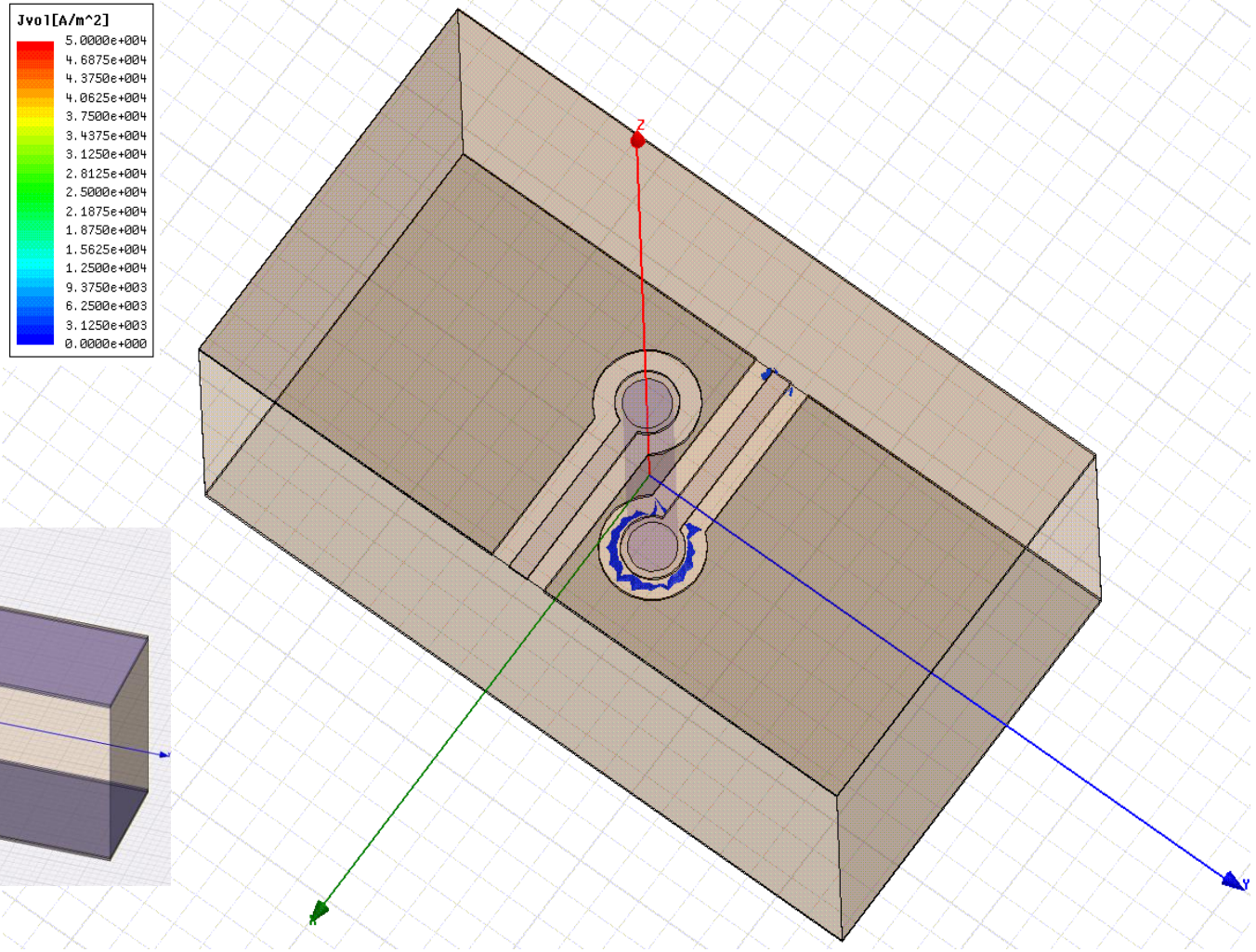


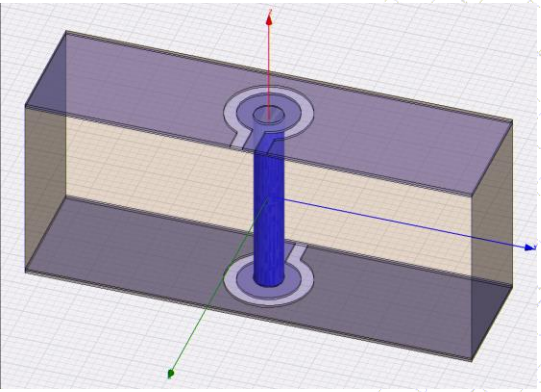
000898

Si Interposer

3D-electromagnetic field simulation

high resistivity (ρ) silicon whose volume resistivity is 4000Ω·cm





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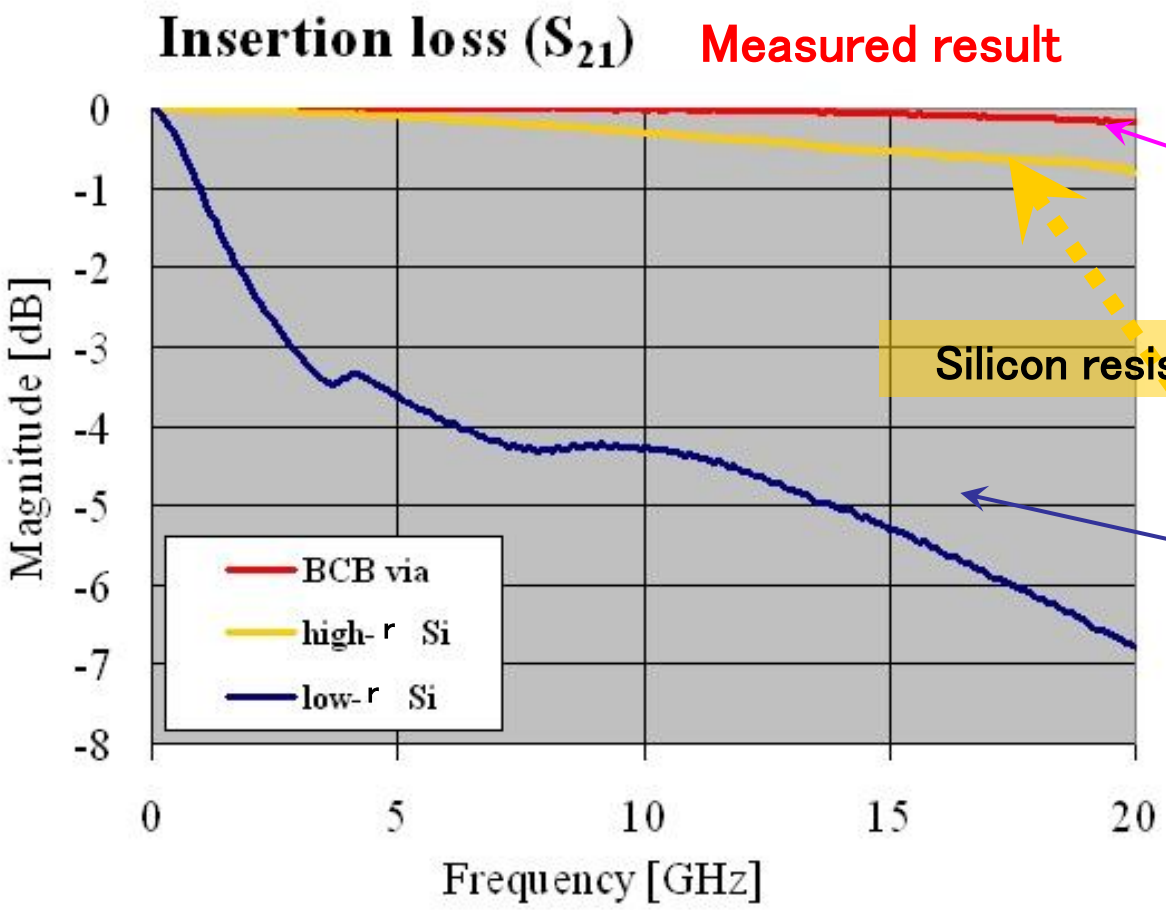
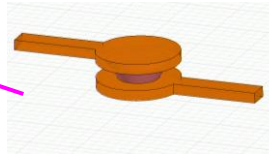
Si Interposer

Signal integrity for high frequency

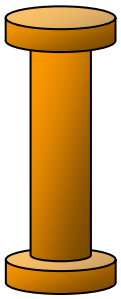
Reduced insertion loss





BCB via

Silicon resistivity higher



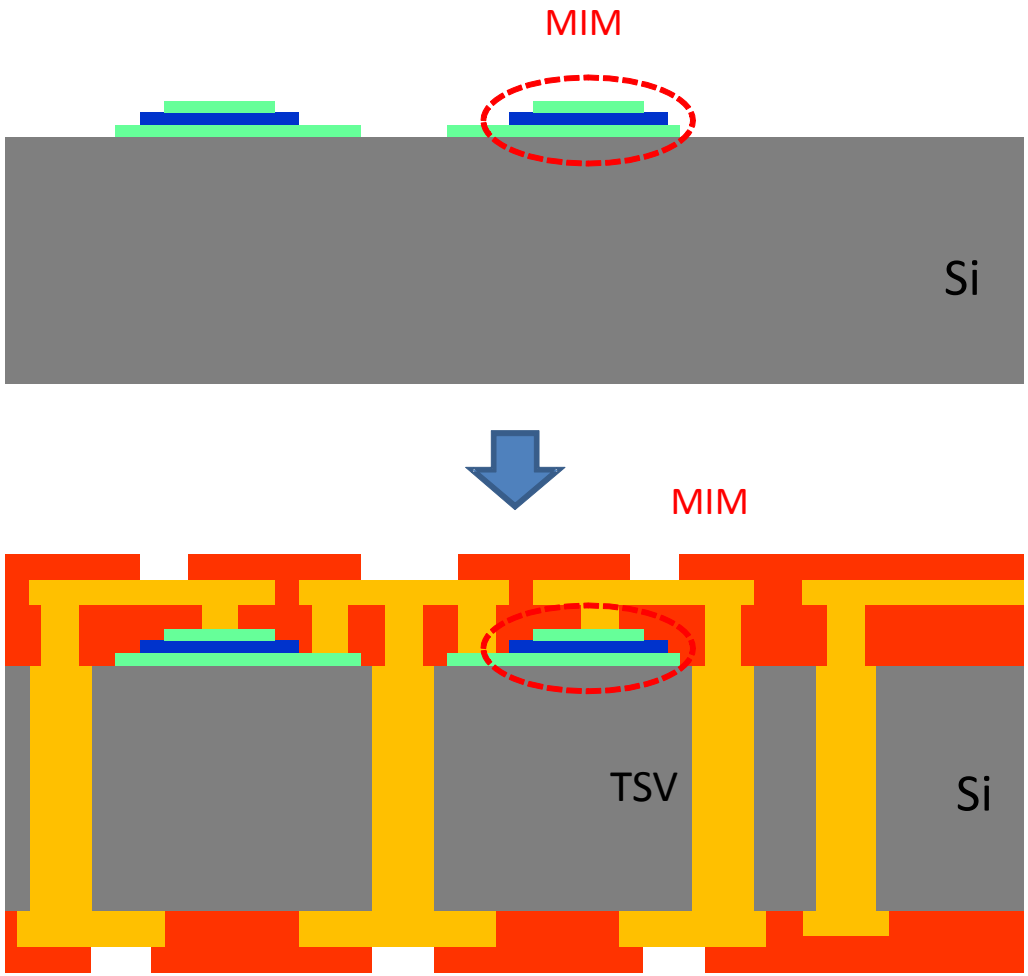
Si through hole

High reisttivity Si enable to decrease the insertion loss of Si though hole

000900

Si Interposer with passives

Via last TSV with Embedded MIM



Ⅰ MIM formation
(SiN film deposited
by PECVD 350dgeC)

Cu/Ti =200/50nm

SiN 200nm

Cu/Ti=200/50nm

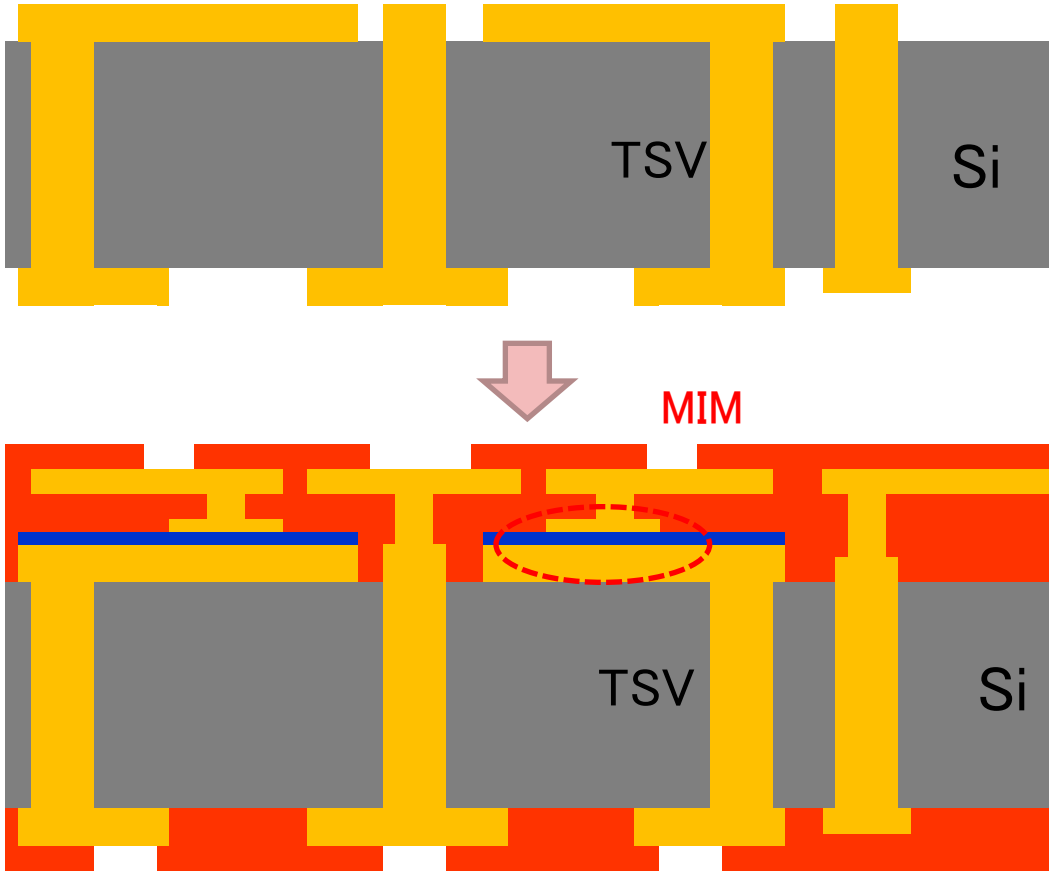
Ⅱ TSV and
RDL formation

DNP

000901

Si Interposer with passives

Via first TSV with Embedded MIM



Ⅰ TSV and
M1 metal formation

Ⅱ MIM formation
(SiN film deposited
by PECVD 250dgeC)

Cu/Ti =2000/50nm

SiN 200nm

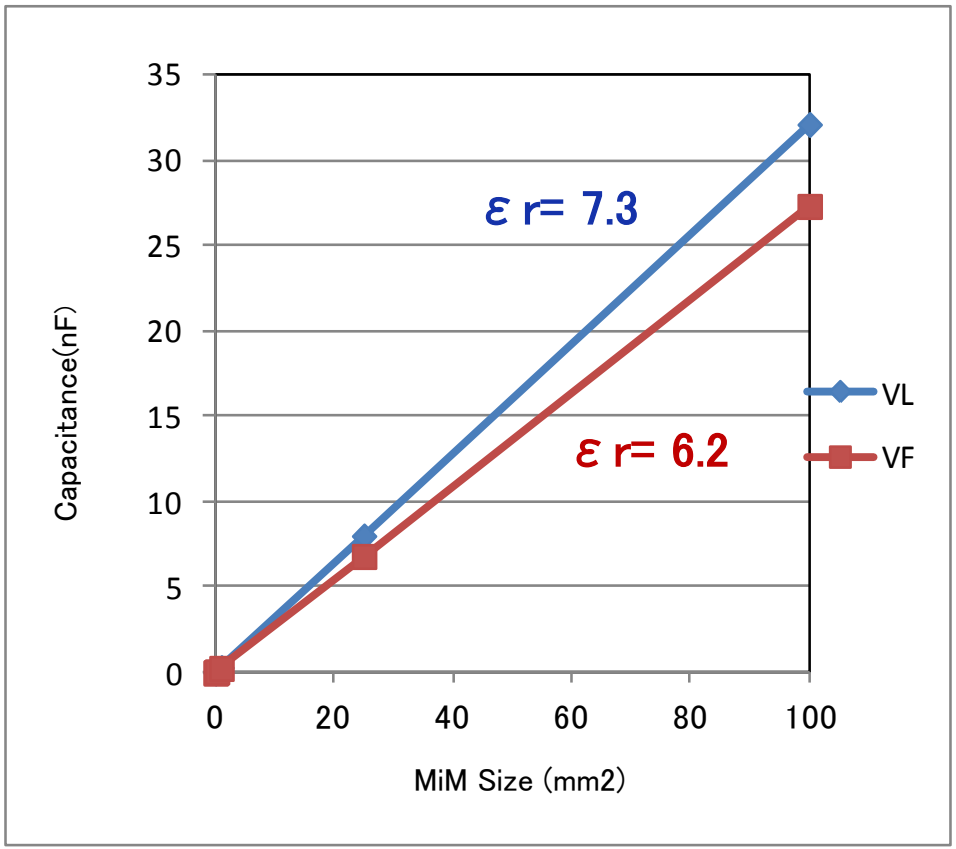
Cu/Ti=2000/50nm

Ⅲ RDL formation

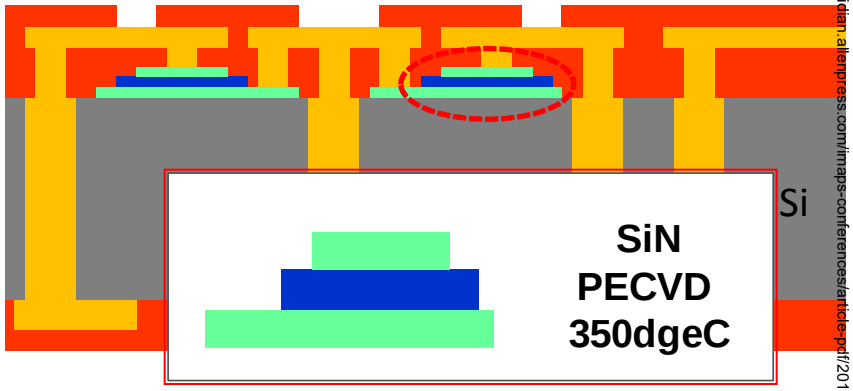
DNP

000902

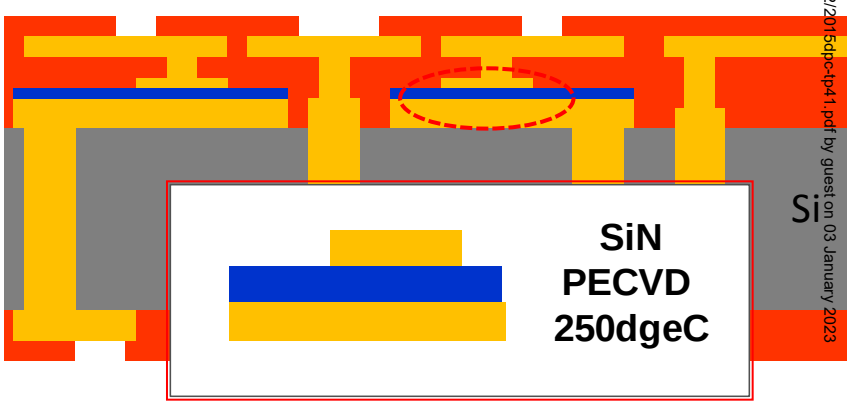
Si Interposer with passives



VL(Via last structure MIM)



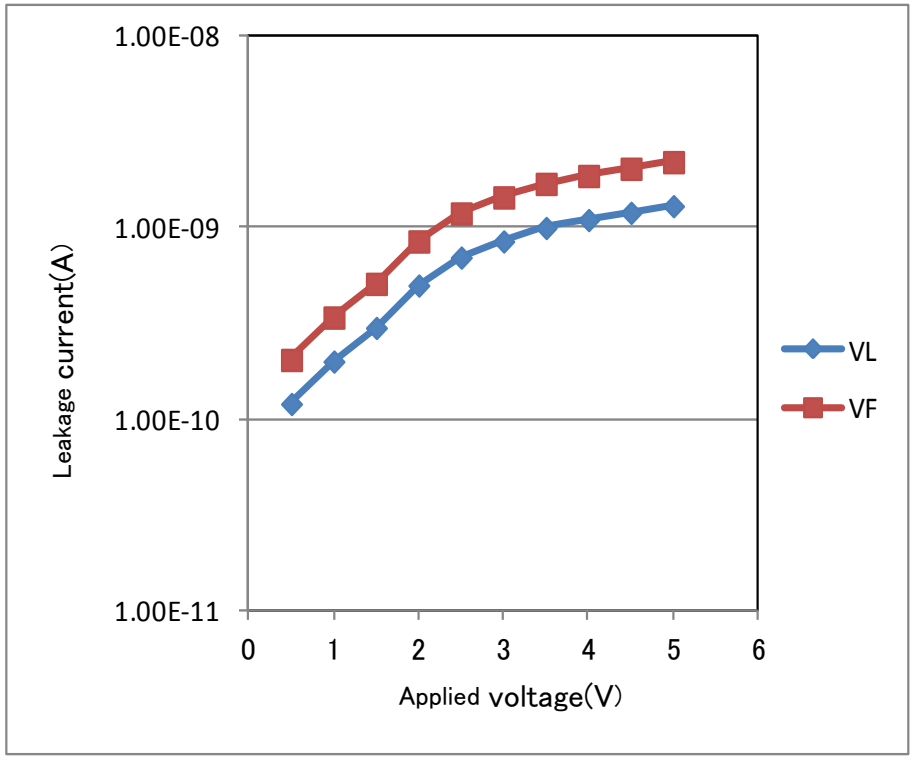
VF(Via first structure MIM)



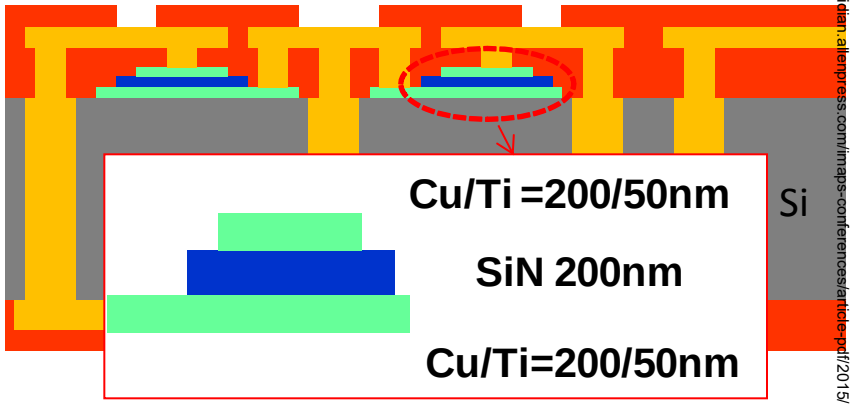
DNP

000903

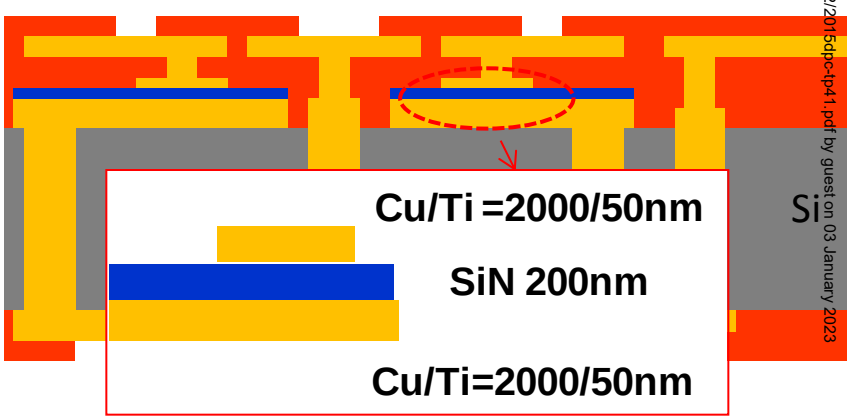
Si Interposer with passives



VL(Via last structure MIM)



VF(Via first structure MIM)



000904

Summary

- Embedded passive devices was fabricated on Si substrate by thin film method.
- The measurement result of integrataed passive device was compared with simulation result .
- Thin film SiN capacitor as embedded passive device was built in surface of TSV interposer by two types method.
- The capacitance and leakage current of capacitor was compared with two types method.
  Capacitance of Via last MIM is higher than Via first MIM .

DNP

