Technical Design Report for the ATLAS ITK - Strips Detector

Draft 0 - v0.0

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13:36h

ATLAS Collaboration

ABSTRACT:
This Technical Design Report presents the technical documentation the ATLAS Inner Tracker (ITk) to meet the challenges at the High-Luminosity LHC (HL-LHC). From 2025, the HL-LHC will provide unprecedented pp luminosities to ATLAS, resulting in an additional integrated luminosity of around 2500 fb^{-}1 over about ten years. This will present a unique opportunity to substantially extend the mass reach in searches for new phenomena beyond the Standard Model of Particle Physics.
The increased luminosity and the accumulated radiation damage will be beyond the possibilities of the the current ATLAS Inner Detector. Due to the increase in track multiplicity and the high pile-up conditions a new tracking system including new trigger capabilities is needed.

KEYWORDS: ATLAS, LHC, HL-LHC, Upgrade, CERN.

Contents

To Do List

In this chapter we will collect major issues/changes which need to be followed up.

- Implement comments from Michel on outline
- Check overlap issues in electronics (see mail Alex Grillo)

Writing Guide

Introduction

This brief document summarises the standards used in writing the Technical Design Report for the ITk strips. As well the document provides examples of call to figures, of compilations of tables, 10 citations, and LaTeX commands frequently used.
In general please follow the recommendations from the ATLAS PubCom:
https : //twiki.cern.ch/twiki/bin/viewauth/AtlasProtected/PubComHome

Comments

We implemented a package to allow the main editors detailed editing with tracking the changes. This can also be used by all people writing to leave a comment to indicate to the fellow writers if you still want to add something or if the sections is ready to be edited etc.
For example: \added{needs to be revised and updated}

will result in:
needs to be revised and updated

Conventions

This section describes the various conventions and rules that should be adopted, for quoting figures, tables or in the spelling of frequently used words.

Labels and references to Chapters and Sections

Please note that each chapter, or section, has a label positioned just at the beginning of the .tex document. The standard for the labels is as follows: **Chapter:ChapterName** that is: **Chapter:ChapterName** or, for the sections, **Section:ChapterName:SectionName** that is: **Section:ChapterName:Section**
References to chapters are as follows: if the argument to be referenced is **generic** and discussed all around a chapter, than the reference is to the Chapter [number]. If the argument to be referenced is **very specific** and discussed in a particular section, then the reference is to the Section [n.m.]

Most commonly used words

Here the spelling, adopted in the TDR, for the most commonly used world:
end-cap / pile-up / read-out / p_T / E_T/ E_T^{miss}/ 10 GeV (that is: there is a space between the digit and the unit)
physics, luminosity, supersymmetric, muons, trigger: all written with small letter
Figure at the beginning of a sentence, while Fig. in the middle of a sentence
Table, Chapter and Section: always in capital and complete word
Chapter n / Section n.n.m / Level-1 / Level-2 / Phase-I / Phase-II / Monte Carlo

Some specially defined commands for the ITk strips TDR (see /Styles/ITKtdrstuff.sty):
\ABC $\rightarrow$ ABC130
\ABCs $\rightarrow$ ABC130*

Labeling of figures

Figures may have several labels, here the rules (adopted from standard ATLAS rules):

- all figures with pp data or with pp data and Monte Carlo results shall be labeled "ATLAS"
- all figures with only Monte Carlo results shall be labeled "ATLAS simulation"
- figures without pp data or Monte Carlo results have NO labels
- figures with test beam or laboratory?s data have NO labels
- label "ATLAS preliminary" is used only in TDR draft versions

Tables and figures

Table 1.1 gives an example of style to be followed for the lay out of tables. The standard for the labels of tables is: Tab:chapterName:tablename.

Detector component	**Required resolution**	**η coverage**	
		Measurement	Trigger
Tracking	$\sigma_{p_T}/p_T = 0.05\%\ p_T \oplus 1\%$	± 2.5	
EM calorimetry	$\sigma_E/E = 10\%/\sqrt{E} \oplus 0.7\%$	± 3.2	± 2.5
Hadronic calorimetry (jets)			
barrel and end-cap	$\sigma_E/E = 50\%/\sqrt{E} \oplus 3\%$	± 3.2	± 3.2
forward	$\sigma_E/E = 100\%/\sqrt{E} \oplus 10\%$	$3.1 < \lvert\eta\rvert < 4.9$	$3.1 < \lvert\eta\rvert < 4.9$
Muon spectrometer	σ_{p_T}/p_T=10% at p_T = 1 TeV	± 2.7	± 2.4

Table 1.1. General performance goals of the ATLAS detector. Note that, for high-p_T muons, the muon-spectrometer performance is independent of the inner-detector system. The units for E and p_T are in GeV.

The following figures are from simulation data (note the label) and originally they were of different size. In the call (see the LaTeX) the figures are re-sized. Both graphs in Fig. 1.1 are in .pdf format, which is the easiest format to be used in LaTeX. The standard for the labels of figures is: Fig:chapterName:figurename.

PLEASE alway add a comment in the latex file (with a % at the beginning of the line) who is the person providing the plot so that we can quickly contact the right person if an update or different plot is needed.

References

As references tool we are using bibtex. That means, that all references should be entered in bibtex format in the file *Main_TDRStrips.bib* in the *trunk* directory. Bibtex will take care of the proper sorting of the reference, but I would recommend that people have their references all together in one area. Most of the references tools in the web provide a tool to get the bibtex formatting, i.e. INSPIRE always has a button the get the correct references. This line is here just to test that also the references are working. Here [1] few calls [2] to the references that [3] appear in the bibliography

of this script. One has to compile the bibliography separately.
If you have trouble with the references, please contact Ingrid as she has someone who volunteered to sort references.

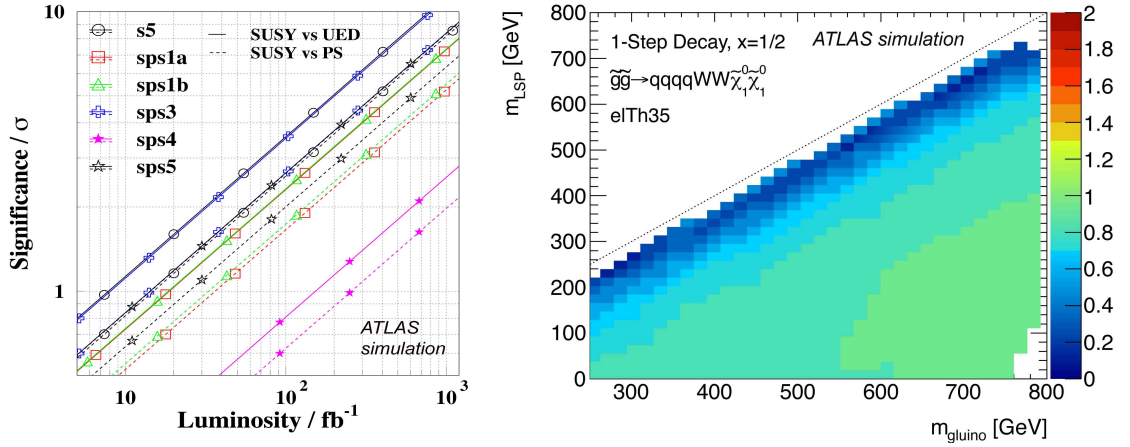

Figure 1.1. **Left**: Luminosity required to obtain significance of spin-discrimination in $q\bar{q} \to \tilde{\ell}^+\tilde{\ell}^- \to \ell^+\ell^-\tilde{\chi}_1^0\tilde{\chi}_1^0$. **Right**: The ratio of the product $A \times \varepsilon$ of acceptance and efficiency for two different offline electron p_T thresholds: 35 GeV relative to 25 GeV. The SUSY model shown is an example simplified supersymmetry model in which each of two gluinos decays to $q\bar{q} + W + \tilde{\chi}_1^0$.

Pre-Defined Macros

LaTeXMacro	Output
\degreeC	C°
\micron	μm
\itk	ITk
\ttc	TTC
\ABC	ABC130
\ABCstar	ABC130*
\HCC	HCC
\HCCstar	HCC*
\ItoC	I^2C
\AMAC	AMAC
\lpgbt	lpGBTx
\gbtx	GBTx
\vtrx	VTRx
\eos	EoS
\DCDC	DC-DC
\ninp	n^+-in-p
\neqsq	n_{eq}/cm^2

Executive Summary

Number of pages to write: 15
Chapter will be written when TDR is close to final.

1. Introduction

Editor: Phil Allport
Chaser: Ingrid-Maria Gregor
Number of pages to write: 3
General introduction to the document and explanation of document outline
This chapter will be written a little later when the overall outline is final. There is still too much movement in the chapters. (IMG May 17th 2016).

2. Motivation and Requirements of the ITk

Editor: Phil Allport
Chaser: Claudia Gemme
Number of pages to write: 20
Scope of the chapter:

- *Physics motivation for a much more granular ITK -> updated work from scoping document (reference to existing documents)*
- *Deficiencies of the existing Inner Detector*
- *- Radiation damage*
- *- Occupancy*
- *- Readout and Bandwidth*
- *Motivations for granularity of ITK including detector occupancies, pattern recognition, tracking and physics performance.*
- *Required reconstruction efficiencies for different particles special, fake rates and momentum resolution as a function of track transverse momentum.*
- *Required performance secondary Vertex Reconstruction and B-Tagging*
- *Refine the requirements compared to earlier used terms (requirements document) such as residuals etc.*
- *L1Track Trigger (physics requirements, technical requirements on strips, ?, forward reference to TDAQ TDR)*

2.1 Overview

2.2 Deficiencies of existing Detector

The current ATLAS Inner Tracking Detector (ID) was designed for 10 years of operation, at a peak instantaneous luminosity of 1×10^{34} cm^{-2} s^{-1}, 14 TeV centre-of-mass energy, 25 ns between beam crossings and $\sim$23 proton-proton interactions per crossing. The Front-End (FE) architecture was designed around a single (hardware) Level-1 trigger signal running at 100 kHz. The design of the detector (segmentation, space point precision, material content and distribution, occupancy etc.) together with the choice of detector technology in the ID is extremely well matched to these operating conditions and to meet the requirements of the ATLAS physics program. The ID has so far performed extremely well, playing a pivotal role in ATLAS physics analyses that rely on charged particle reconstruction and the identification of electrons, photons, muons, and tau-leptons produced in both proton-proton interactions and heavy ion collisions. The ID is not only used to reconstruct the trajectories of charged particles, it is also used in the identification of secondary vertices, particle identification through Transition Radiation (TR) and dE/dx, full reconstruction of exclusive decay modes and identification of primary vertices. The ID is also used to improve

the jet energy measurements, in the determination of isolation criteria and the calculation of E_T^{miss}. The detector elements of the ID were designed to comfortably withstand the radiation fluences associated with the integrated luminosities up to the 350 fb^{-1}anticipated during the running time before the Phase II upgrade.

After the upgrade of the LHC machine and ATLAS experiment with first physics around the middle of 2025 we anticipate an additional 10 years of operation of the ATLAS experiment. The HL-LHC will be able to deliver very high peak instantaneous luminosities with 25 ns between crossings, but this will be levelled down to 7 $\times 10^{34}$ cm^{-2} s^{-1} in the detector. At these levelled luminosities, there will be $\sim$200 proton-proton interactions per beam crossing. To cope with these extreme data rates , a major upgrade to the triggering capabilities of the experiment will be required. The required first level of hardware trigger is anticipated to be at 1 MHz rate (Level-0) with a minimum latency of 6 μs, but designed to handle 10 μs. A possible second hardware trigger (Level-1) at 400 kHz in under consideration which would have a minimum latency of 30 μs (but able to handle up to 60 μs). The integrated luminosity design goal for the upgraded detector is 3,000 fb^{-1}.

The existing Inner Detector was not designed to meet the requirements for the Phase II upgrade and cannot hope to meet the very stringent requirements that will be part of the physics programme that goes with it. There are several reasons why the existing Inner Detector needs to be replaced:

Radiation Damage The current pixel detector was designed using radiation hard sensors and electronics to withstand the radiation damage that is equivalent to an integrated luminosity of 400 fb^{-1}. Similarly, the Semi-Conductor Tracker (SCT) was designed and constructed to operate up to an integrated luminosity of 700 fb^{-1}, although after the insertion of the IBL, increases in fluences due to additional services reduce the luminosity ceiling to that of the pixel system. The IBL, itself was designed for fluences equivelent to roughly 850 fb^{-1}. The specifications for radiation tolerance of the detectors in the current ID are sufficient to guarantee high efficiency for the integrated luminosity expected to be collected by 2022, but they are not suitable for operation much beyond this level. Above the design fluences, the intrinsic hit efficiencies drop below the limits required by the pattern recognition algorithms and the leakage currents from the detectors will both exceed the limits of power supplies and (due to heating as a consequence of the increased leakage current) the capacity of the cooling system. The latter issues also affect on-detector power and cooling distribution.

Bandwidth Saturation The FE electronics of both the pixel and SCT detectors employ zero suppression to minimize the data volume along the optical fibres. Both detectors can accommodate events with about 50 proton-proton interactions per crossing which come with sustained instantaneous luminosity of twice the design value or about 2 $\times 10^{34}$ cm^{-2} s^{-1}. Above 3 $\times 10^{34}$ cm^{-2} s^{-1} at 25 ns bunch crossing rate, limitations in the buffering of the links between the on-detector pixel module electronics (FE chips) and the read-out driver (ROD) will lead to inefficiencies when the limit of more than 0.2 to 0.4 hits per double column per 25 ns bunch crossing is exceeded. A similar limitation occurs in the SCT at about the same value of instantaneous luminosity where the optical links between the front-end ABCD chip and the RODs will also lose data.

Limitations from Detector Occupancy With $\sim$200 proton-proton interactions inside the current detector the confusion that comes with the additional hits without the compensating increase in

granularity will compromise the efficiency of the pattern recognition and track finding efficiency. The rate of fake tracks would also increase sharply. It would be difficult to resolve nearby particles inside the SCT, while the TRT occupancy would reach 100%. The inability with the current Inner Detector to resolve nearby tracks, for example in boosted t-quark jets, would also significantly compromise the physics reach in the HL-LHC era.

These very substantial limitations, taken together with others not discussed here, necessitate the complete replacement of the Inner Detector for the Phase II upgrade of the experiment.

2.3 The Requirements of the ITk

The performance requirements that are used as input to the design of the ITk are driven by the needs of the Phase II physics programme as set out in detail in the Phase II LoI and [4, 5]. The key features of the physics programme and the reliance on tracking are sketched out in section 4. The requirements include that the ITk should. TO BE UPDATED TO THE REQUIREMENT DOCUMENT. ALSO NEED TO SAY SOMETHING FOR THE LARGE ETA REGION[CG]

1. be designed for 10 years of operation at instantaneous luminosities of $7 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$ (after levelling), 25 ns between bunch crossings and an integrated luminosity of 3,000 fb^{-1}.
2. reconstruct the tracks associated with isolated particles, such as electrons and muons, with high efficiency and low fake rate.
3. measure the electrical charge, transverse momentum and direction of isolated charged particles.
4. reconstruct the different vertices associated with the multiple proton-proton interactions and identify the vertex associated with the hard scatter interaction that fired the trigger. This information is used to compliment the calorimeter information in the determination of particle isolation and the measurements of jet and missing energy.
5. reconstruct secondary vertices including inside b-jets (even in boosted jets) with high efficiency and purity.
6. have a good two-track separation resolution to measure tracks in the core of high energy jets, with high efficiency and sufficient redundancy, and to reduce the reconstruction of fake tracks.
7. reconstruct the tracks associated with the decays of tau leptons and determine their impact parameter.
8. be able to measure the trajectories of tracks with sufficient accuracy to determine the entry point to the calorimeters to good precision.
9. allow for a luminous region that is either Gaussian in shape with a sigma of 7cm, or more complex “flat top” distributions if these can be delivered by the HL-LHC final focus system.
10. remain hermetic, for 1 GeV/c tracks, while allowing the interaction point to move ± 15 cm from the centre of the detector (0,0,0).

11. reconstruct the tracks and vertices associated with converted photons. The limiting radius for such conversion finding will depend on the final layout of the detector.

12. have an occupancy that does not compromise the pattern recognition. Experience shows that this limit is 1% in the strips and 0.1% pixels.

13. be designed such that the combination of detector layout and pattern recognition should mean that track reconstruction efficiency and rate of track mis-measurement should not be significantly deteriorated in the presence of 10% dead channels or 10% dead modules randomly distributed in the detector volume. Studies of the effects of correlated losses of acceptance (particularly phi sectors) will be made.

14. support the operation of a Level-0 trigger running at 1 MHz rate (6 μs minimum latency but designed for up to 10 μs) and a possible Level-1 running at 400 kHz (30 μs minimum latency but designed for up to 60 μs). The ITk should also be able to trigger on successive beam crossings at Level-0 and Level-1. A description of the track trigger is given in the next section.

15. have a mechanical design that is optimized for efficient pattern recognition and track reconstruction including optimized use of CPU. This is particularly important for the Higher Level Trigger (HLT)

16. have a layout that promotes both modular design and ease of access. It should be possible to remove the inner layers of the pixel detector in a long opening of the detector.

17. be assembled and commissioned on the surface and installed as a single unit into the LAr cryostat.

18. be completed with enough time to allow one full year of commissioning/testing in one of the surface buildings at point-1 before the detector is scheduled for installation in the pit.

The exact limits of the rapidity coverage of the ITk is currently under discussion inside the Layout Task force. Preliminary results on the achievable performance in the high eta region are presented in Sec. 4.

2.3.1 Reconstruction, efficiency and momentum resolution of High Transverse momentum tracks.

The resolution of a track parameter X can be expressed as a function of P_T as

$$\sigma_X(P_T) = \sigma_X(\infty)[1 \oplus \frac{P_X}{P_T}] \tag{2.1}$$

where P_X is a constant that represents the value of transverse momentum for which the intrinsic and multiple scattering terms are equal for the parameter X under consideration. A complete list of the performance requirements are given in the table 2.2 for the limited rapidity range $|\eta| < 2.5$.

The performance of the track reconstruction for muons at high transverse momentum is determined by the detector granularity in the bending and non-bending planes. In the limited rapidity

Table 2.2. Expected ITk track parameter resolutions (RMS) at large transverse momentum at a pile-up of 200.

Track Parameter $(0 < \|\eta\| < 0.5)$	Units	$\sigma_X(\infty)$
Inverse transverse momentum $\sigma_(q/P_T)(\infty)$	TeV^{-1}	< 0.2
Transverse impact parameter d_0	μm	< 8
Longitudinal impact parameter z_0	μm	< 50 (This value is η dependent)

Table 2.3. The achievable precision for reconstructing the centroid of electromagnetic clusters.

Accuracy of centroid position	$\|\eta\| = 0$	$\|\eta\| \sim 2.5$
$d\|\eta\|$	0.2×10^{-3}	0.35×10^{-3}
dϕ(rad)	0.4×10^{-3}	0.7×10^{-3}

range $|\eta| < 2.5$ the ITk must have an efficiency of around 99% for isolated high (>3 GeV) transverse momentum muons in the presence of up to 200 proton-proton interactions.

The accuracy of the reconstructed centroid of eletromagnetic calorimeter clusters is dependent on both their energy and the rapidity of the cluster. The achievable precision for high transverse energy photons is shown in table 2.3.

Also shown in the figure 2.2 [4], is the track matching resolution for high energy electrons from the decay of W and Z bosons measured in the 2010 data. The track impact precision is required to be compatible with the calorimeter precision and allow for efficient bremsstahlung recovery.

Figure 2.2. Track-cluster matching variables of electron candidates from W and Z boson decays for reconstruction with nominal geometry and after the 2010 alignment corrections have been applied.

The track reconstruction and fake rate must not be degraded at the highest pileup or within the cone of boosted t-quark jets. An indicative benchmark for the upper limit of pixel or strip occupancy in the presence of 200 pileup interactions is less than 0.1% for the pixels (barrel and disc) and < 1 % for the strip detector (barrel and discs).

As noted above, the reconstruction efficiency for high transverse momentum muons in the limited range of pseudorapidity $|\eta|$ <2.5 should be around 99%. The rate of badly mismeasured tracks that are due to shared hits or misalignments should be low. Currently this is still being studied.

Charge misidentification for the very highest momentum muons is expected to be limited by the misalignment of detector components. This is particularly true at high pseudorapidity. In the presence of 200 pile-up interactions, the number of events with tracks outside the expected 3 sigma error band due to misalignment should not exceed 1%.

The target reconstruction efficiencies for muons and pions with transverse momentum greater than 5GeV are given in table 2.4.

The track reconstruction efficiency and track mis-measurement should not be significantly deteriorated by the loss of 10% dead channels or 10% dead modules, randomly distributed within the detector volume. The effect of the loss of a correlated groups of modules should also be studied and the effects of such losses should be mitigated by design. Such correlated losses include groups of detector modules on staves or discs or losses of services as they are routed to the detector. The

Table 2.4. The target reconstruction efficiencies for different particle species in limited ranges of pseudorapidity. The target efficiency for electrons in the forward regions should not be significantly degraded with respect to the central region.

Target track reconstruction efficiency for 5GeV tracks in the presence of 200 pile up events.	
$\mu^{\pm}$	99%
$\pi^{\pm}\|\eta\| \geq 1.0$	$> 95\%$
$\pi^{\pm}\|\eta\| > 1.0$	$> 90\%$
$e^{\pm}\|\eta\| \leq 1.0$	$> 80\%$

results of these studies are used in the failure analysis that will be presented at the time of the TDRs.

The amount, location and distribution of material within the tracker is of the utmost importance to the experiment performance in the reconstruction of: pions, electrons and photons. The material influences the reconstruction efficiency, the momentum resolution and the rate of reconstruction of fake tracks. The goal is to improve the multiple scattering terms by 50% compared to the existing Inner Detector.

While the material from the active detector elements is important the dominant effects come from the services. The effect of these passive materials (services, supports, interfaces etc) are different for those inside and outside the active tracking volume. In terms of additional tracks seen by the ITk, material within the active detector volume results in conversions and interactions while material outside the detector volume causes secondaries and conversions that subsequently re-enter the active detector volume. In the both cases these tracks are not normally associated with the primary vertex. The exception will be for some tracks that originate in the inner pixel layers. In both cases, the material of the ITk compromises the performance of the electromagnetic calorimeter while material within the active volume also limit the achievable momentum and (for the innermost pixel layers) impact parameter resolution.For the ITk we target the following values:

1. $< 2\%$ X_0 per layer including services and non active support material for the pixel detector. Ie a total of 0.1 X_0 at $|\eta|$ =0 for a 5 layer system.
2. Further reduction of this value further for the two innermost layers.
3. $< 2.5\%$ X_0 per layer including services and non-active support material for the double sided micro-strip detector i.e. a total of < 0.1 X_0 at $|\eta|$ =0 for a 4 layer system.
4. In both cases the amount of inactive material seen by a track from the interaction point will tend to increase towards the end of the structure. Care should be taken in the design to minimize the material in the end of structure services.

The non-active services should be minimized where ever possible with non-active services routed to outside the detector acceptance as efficiently as possible.

2.3.2 Vertex Reconstruction and B-Tagging

As noted above, the 2 sigma limits of the z-vertex distribution are currently assumed to be +/- 150 mm. With 200 pile-up events the mean separation of primary vertex is typically less than

1mm. It is therefore not possible for all vertices of a selected event to be reconstructed. However, it is important that high transverse momentum objects (muons, electrons and tracks in high transverse energy jets) can all be associated with the vertex with good efficiency. Vertex reconstruction in such an environment poses stringent requirements on the tracking resolution close to the interaction point and imposes the need to minimize the amount of material of the inner layers of the pixel detector.

In the presence of 200 pile-up events, the requirement is to reproduce the current ATLAS ID performance for primary vertex reconstruction and identification. This means, in the case of $t\bar{t}$ events, that the probability of the $t\bar{t}$ vertex being among the reconstructed vertices must be greater than 0.97. In addition, the probability that the $t\bar{t}$ decay is associated to the correct event should also be greater than 0.97.

The ϕ and Z granularity of the innermost pixel layers must be optimized for light-jet rejection in the jet P_T range around 150GeV. The strip layout should be optimized to minimize the hit sharing in the core of dense jets. The performance of the b-tagging in the presence of 200 pile-up events, measured using tools such as IP3D and SV1, should be optimized for each layout and should match the performance of the current detector (including IBL) in the presence of 200 pile-up events. This implies that the performance metrics set out in table 2.2 are met.

2.4 L1 Track trigger for ITk

THIS WILL NEED A REWRITE TO REFLECT THE TDAQ DECSION ON A TWO LEVEL ARCHITECTURE BUT I WOULD ANTICIPATE THE MORE PROBABLE OUTCOME CURRENTLY COULD BE A 1 SINGLE LEVEL 1MHZ TRIGGER[CG]

The requirements of the ITk hardware trigger are driven by the ATLAS physics goals at the HL-LHC and the constraints imposed by the readout of the detector subsystems. From the perspective of physics, the trigger must maintain thresholds for electrons and muons at between 20-25 GeV, and should maintain sufficient flexibility to adapt to emerging physics scenarios.

At the high luminosities expected following the Phase-II upgrade, mean numbers of separate pp interactions in the range of 160-200 are expected for every bunch crossing. Event rates for single lepton candidates passing the Level 1 (L1) triggers in the ATLAS detector using the current trigger strategy with Pt thresholds for single leptons around 20 GeV are expected to be of the order of 200-400 kHz for *each* lepton species individually, with jet and other physics signatures providing some significant additional rate.

2.4.1 L1 Track trigger system requirements

A full readout of the tracker at the LHC BC frequency of 40 MHz would require bandwidth and processing capacity that exceeds available power, material and financial resources. Hence the amount of data transferred from the tracker to the trigger must be reduced. The two level trigger (L0/L1) strategy of ATLAS was introduced to allow tracking information to be used for the L1 trigger decision.

The L1 Track trigger system is divided in on-detector and off-detector parts. The on-detector part delivers with short latency tracker hits to the L1 Track trigger processors located in counting room. The implementation of the on-detector electronics is the responsibility of the ITk while the off-detector electronics is the responsibility of TDAQ. The ATLAS trigger scheme is shown in Figure 2.3. The ATLAS latency requirement (L0+L1) for the electronics to be used at HL-LHC

is 30 μs (indicated in green in Figure 2.3). This accommodates the latency of L0 accept (L0A), the time for the Central Trigger Processor to make the L1A decision and L1 Track trigger. The L1 Track trigger latency budget of around 20 μs is split into 6 μs for data readout from tracker and 14 μs for processing data in the L1 Track trigger off-detector hardware. To minimize the dead time in ATLAS the sub-systems including the ITk are required to process consecutive triggers at BC frequency. The TDAQ requirement for all new electronics designed for HL-LHC is that the L0 data should be buffered for 10 μs and L1 data for 60 μs (indicated in red in Figure 2.3).

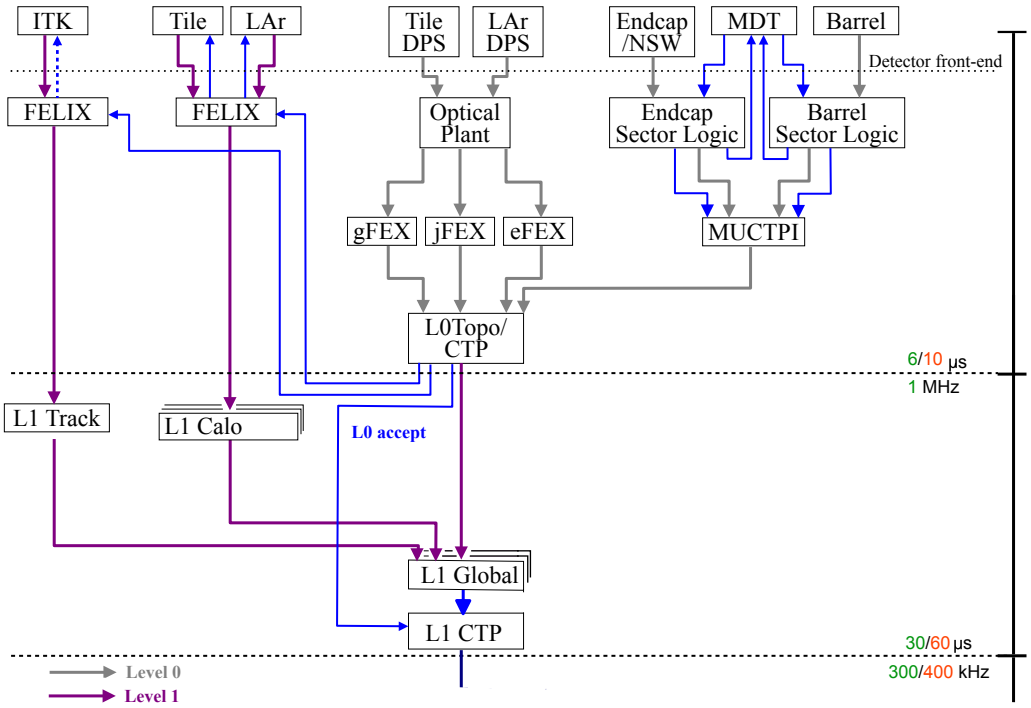

Figure 2.3. The ATLAS L0/L1 sytem overview.

The FELIX system of the tracker receives L0A and Region of Interest (RoI) from the L0Topo/CTP at maximum 1 MHz rate. FELIX request readout of the full ITk and the modules return data. However, FELIX can if running in regional readout mode send a Regional Readout Request (R3) to the detector modules. The main difference between the full readout and R3 readout is where the L1 data is buffered. In the case of full readout, all ITk data is transferred off-detector where it is buffered until L1A arrives. In the case of R3 readout, the L1 data is buffered on the front-end ASIC. The full readout of ITk data require higher readout bandwidth than the regional readout does. The full readout of L0A data at 1 MHz is however preferred by ITk because of simpler readout logic.

Only the ITk data belonging to a RoI is transferred from FELIX to the L1 Track trigger processors since the use of the full ITk information for L1 Track trigger processing would require a significant increase in L1 Track processing hardware. Unless strong physics motivations for the use of full tracker data in the trigger is found, L1 Track trigger will be RoI based. The L1 Track

off-detector hardware can if required be increase to process all ITk data as a part of regular upgrades. The output from the L1 Track processor is combined with L1 trigger information from the rest of ATLAS in L1 Global and L1 CTP which sends the L1 accept trigger at maximum 400 kHz rate.

2.4.2 ITk readout for the L1 Track trigger system

The baseline architecture is to read out the full ITk strip and pixel detectors at 1 MHz. The baseline was changed from R3 readout to full readout to facilitate simpler on-detector readout logic. Latency studies for full readout at L0A-rate are in progress.

Studies of R3 readout (old baseline) using a discrete event simulation of the complete readout chain including the distribution of the R3 and L1 accept requests, and readout of the HCC to the off-detector electronics have been performed using ITk hit occupancies expected with 200 pileup interactions per bunch crossing. The results suggest that old baseline layout with ASICS daisy chained on the hybrid gives increased latency that in parts of the tracker violates the latency budget. The studies led to a change of architecture to *star* readout where each ABC130 is connected directly to the HCC. The principle advantage of the star readout arrangement, is that the time to transfer the data along the daisy chain multiple times is not required – each data packet from each ABC130 can be transferred simultaneously to the HCC. In addition, because each chip has a dedicated link, the data packets from the chips will not need any additional header to identify from which chip they originated, therefore the size of the data packets that are transferred to the HCC is reduced. These packets can then be simply aggregated into a single, larger data packet, with a single header on the HCC, which subsequently reduces, with respect to the daisy chain scenario, the total data volume needed to be read across the GBT.

2.4.3 Trigger Processing with ITk data

A FTK-like [6] system architecture is being proposed for the L1Track, with Associative Memory (AM) devices for pattern matching and DSPs in FPGAs for track fitting. ITk data are sent to the data preprocessors of the L1Track where cluster finding is performed if needed, full resolution hits are stored and coarser resolution hits are produced for pattern recognition in the AM devices. Linear fits are performed in DSPs with the local coordinates of the full resolution hits for the patterns found, to obtain track parameters.

The very high level of pileups and the larger number of ITk detector layers and channels, compared to the current ATLAS, would inevitably require a much larger number of patterns to be stored in the AM chips in order to achieve high efficiency for real tracks and low level of fakes. Therefore, the effort to develop new generations of the AM chip, using smaller feature size and novel ASIC design technologies (e.g., 3D integration) is essential for the ATLAS Phase-II upgrade. The AM chip to be used for FTK (AMChip06) is based on 65 nm technology and can hold 128k patterns (8 layers). The AM2020 team is planning to design new chips with capacity increased at least by a factor of four by the time when the L1Track hardware construction starts.

The processing time of the L1Track is mainly contributed by the data transmission of the AM system and the tracking fitting. Where the RoI readout scheme is used, the data request rate is 5% of the total event data so that the total data I/O of the AM system and the tracking fitting load is not

significantly worse than that of FTK. In the full 1 MHz readout scheme, more parallelism is needed to comply the latency constraint.

A strategy may be untenable with pattern matching and track fitting done with all 14 silicon layers in one step. Two options could be investigated. The first one is to perform track finding using a subset of the silicon layers but employ all 14 layers in the final fitting. This scheme allows the use of relatively narrower coarse resolution hits, reducing the number of matched roads. It also breaks the power law behaviour of the number of fits because only good tracks are kept after the first step for use in the second step. The second option is the two-step architecture. Pattern matching and track fitting are first done in the SCT layers. For each track that passes the quality cut, a pseudo-hit is created for the second stage. The curvature, azimuth, and polar angle are each binned, and a single "pseudo-layer" is created with these three parameters encoded into a coarse resolution hit. The pseudo-layer and the pixel layers go through a 5-layer AM, with the matched patterns then going into full 14-layer track fitting.

3. ITk Layout

Editor: Uli Parzefall
Chaser: Ingrid-Maria Gregor
Number of pages to write: 15
Scope of the chapter:

- *High level overview of ITK Layout (Pixel overview and volume/outer radii) Layout including the motivations for the remaining layout (pixel) options and their current status*
- *Description of ITK Strip Layout (why x layers, stereo angle choice (what and why) etc.*
- *Description of cost vs performance analysis: N layers, N-disk, short-strip and long strip, stereo angle choice (what and why) etc.*
- *Envelope and other external requirements (explaining why we split etc.)*
- *Impact of the constrains from other parts of ATLAS ? calorimeter etc*
- *Justification of choice of rapidity limits*
- *Details of the material content in the detector as a function of pseudo rapidity (up to eta=5)*
- *Expected radiation levels TID and non-ionizing and impact on design (this can only come here as we first have to introduce the layout)*

Currently a collection of material from the IDR and scoping document. First additions and changes implemented.[IMG]

One of the principle conclusions of the Letter of Intent [7] was that it is possible to build an all-silicon tracker that is capable of delivering performance that is at least as good as and probably better than the current ATLAS Inner Detector. The design presented was matched to the physics program that will start at the start of the HL-LHC phase. Furthermore, it was shown that this is possible in an environment with up to 200 proton-proton interactions per beam crossing in the central region of the detector. Following the LoI, the priorities of the ITk community changed from a demonstration of proof-of-principle towards an optimal design. The optimal design of the ITk is a compromise of tracking performance, cost optimisation, ease of construction and installation, as well as the ability to maintain the detector throughout its lifetime. The requirements as outlined in Chapter 2 have spawned a range of designs, each addressing one or more particular facet of the design requirements. These designs are now under scrutinisation within the ITk simulation and performance group.

In this chapter the baseline layout for the strip detector and different concept layouts for the pixel detector are presented, together with the motivation behind them.

3.1 Overview of the ITk Layout

An all-silicon-detector tracker is proposed, with pixel sensors at the inner radii surrounded by microstrip sensors. In the central region, sensors are arranged in cylinders, with five pixel layers

followed by two short-strip layers then two long-strip layers. From current knowledge of the HL-LHC conditions the outer radius of the beam pipe will be designed to be at 32 mm Check latest number[IMG]. The forward regions will be covered by x pixel disks and 6 strip disks.

The tracker is surrounded by a polyethylene moderator to reduce the energies of neutrons, which decreases the 1 MeV neutron equivalent silicon damage fluence arising from the flux of neutrons entering from the calorimetersfind reference for the neutron moderator (which for the current ID are partially moderated by the material of the TRT).

In the optimisation process, gaps have been preserved between sub-detector parts to allow for supports, services, and insertion clearances.

In the optimisation process, gaps have been preserved between sub-detector parts to allow for supports, services, and insertion clearances. The resulting sensor areas and channel counts are shown in Table **??**. The biggest changes to the current ATLAS inner tracker are the replacement of the TRT with 48.2 mm long silicon strips; the pixel system extends out to larger radii; more pixel hits in the forward direction to improve the tracking in this dense region; and smaller pixels and 24.1 mm long inner strips to increase the granularity. The outer active radius is slightly larger, improving momentum resolution. Services have been routed out of the active area as soon as possible, minimising the effects of non- sensitive materials. The layers of silicon are more evenly spaced, especially in the forward region,

3.2 Justification of choices

need better title for this section[IMG]

- why how many staves in one layer
- why the disks where segmented into petals and why 32 petals per disks
- removal of stubs compared to LoI
- removal of one disk compared to LoI
- change of stereo angle from axial/stereo of 40 mrad to both stereo 26mrad
- z-positions of disks
- extending length of strip barrel from 13 modules to 14 modules
- pixel radius ?

3.3 Cost versus performance analysis

Maybe this should rather go into the costing chapter ? Kind of difficult here before we actually have the costs explained. [IMG]

ITk strip layers are double-sided with the sensors rotated by 26 mrad on each side, giving the second coordinate measurement.

3.4 Envelope and other external requirements

3.5 Overview on material

I think we should split this into two segments: step1.5 material description as this is what is baseline for the following studies and the difference which will be implemented for step2.0 as that will be the real material description[IMG]

3.6 Radiation environment expectations for the ITk baseline detector

taken from the IDR - to be updated to the latest plots and numbers based on the new layout - will contact Ian and Paul[IMG]

Radiation background simulations are performed for the ATLAS ITk using the FLUKA particle transport code [8] and the PYTHIA8 event generator [9]. Predictions of particle fluences and ionising doses for the LoI layout were performed and reported in the Phase II Letter of Intent [7], assuming $\sqrt{s} = 14$ TeV and an integrated luminosity of 3000 fb^{-1}. A more detailed discussion of the simulations is given in supporting note [10]. In summary, the maximum 1 MeV neutron equivalent fluences for the pixel, short-strip, long-strip and end-cap detectors were predicted to be 1.4×10^{16} cm^{-2}, 5.3×10^{14} cm^{-2}, 2.9×10^{14} cm^{-2} and 8.1×10^{14} cm^{-2}, respectively. The corresponding values for the ionising dose are 7.7 MGy, 216 kGy, 63 kGy and 317 kGy. Hadron fluences for energies > 20 MeV are also provided to allow estimates of SEU, as well as charged particle fluences for occupancy estimates. Check all numbers[IMG].

Figure 3.4. The fluence distribution for the endcap ring layout. Shown on the left is the 1 MeV neutron equivalent flux and total ionizing dose on the right. The lower plots show the ratio of the fluences with respect to the LoI layout.

Figure 3.5. The fluence distribution for the endcap ring VF layout. Shown on the left is the 1 MeV neutron equivalent flux and total ionizing dose on the right. The lower plots show the ratio of the fluences with respect to the LoI layout.

The simulations have been repeated taking into account the ITk layout as described in Section **??**. The results are shown in figure 3.4. Small increases in maximum fluence and dose, typically a few percent, are seen in the pixel and strip sensor volumes, compared to the published LoI values summarised above CHECK.

It is important to emphasise that accurate fluence and dose predictions requires an accurate modelling of the ATLAS geometry in FLUKA. In the ITk strip regions the fluences are dominated by particles coming from interactions in the calorimeter, beam-line and ITk service material. Studies have shown that routing the ITk services out radially away from the beam-line as soon as feasible is beneficial in reducing radiation backgrounds, including activation.

Comparisons between fluence and dose predictions and measurements have been made during Run 1 at $\sqrt{s} = 7$ TeV and 8 TeV [10] most updated?. Typically agreement was better than 30% and a safety factor 1.5 has been proposed for the simulation component in the predictions. Given the additional uncertainties in detector layout design a safety factor two is used on fluence predictions by the ITk strip community in irradiation testing. However, any significant addition of material

compared to the LoI layout could push up the fluence predictions beyond this safety factor. For example, preliminary simulations of the VF layout results in significant fluence and dose increases as shown in figure 3.5. Furthermore, the maximum ionising dose to pixel sensors and electronics in these high eta regions is predicted to be greater than 10 MGray (1 GRad).

4. ITk Performance

Editor: Phil Allport
Chaser: Helen Hayward
number of pages to write: 30
Scope of chapter:

- *(Similar as in IDR) Overview of the tools and results on studies with focus on the performance parameter relying on the strip system; as pixels are not completely fixed most studies will be based on the basic pixel design with 50x50um2; only in special cases the effect of different pixel choice is mentioned*
- *tracking performance in jets; momentum resolution; single track performance; physics objects as in requirements document*
- *Add physics studies (for time being in this chapter, maybe separate chapter)*

4.1 Tracking Performance Metrics

Helen: need definitions of efficiency, fake rates, resolutions. also the basic tracking track quality cuts

Among the most important performance criteria for a tracking detector are tracking efficiency, impact parameter resolution and the rate at which "fake" tracks are reconstructed. Fake tracks do not closely match any single physical particle, but are instead from multiple different particles, and/or noise hits. Significant background contributions can arise due to such fake tracks, and so understanding and minimising the number of fake tracks is very important when designing a tracking detector. The efficiency, resolution and mis-reconstructed track fraction (fake rate) are defined as follows:

- **Efficiency**: The tracking efficiency is defined as the fraction of prompt muons or pions which produce matching tracks passing a track quality selection, optimised separately for each scoping scenario. The particles considered must be a true muon or pion, and satisfy $|d_0^{\text{truth}}| < 1.0$ mm and $|z_0^{\text{truth}}| < 150$ mm. Secondary particles produced in the Geant4 simulation are excluded. When measuring the efficiency as a function of η, the muons or pions must have $p_T > 4$ GeV. For the result as a function of p_T, muons or pions must have $p_T > 1$ GeV, $|\eta| < 4.0$ for the Reference layout, and $|\eta| < 2.7$ for the Middle and Low layouts.

  In order to avoid counting fake tracks in the efficiency calculation, tracks are required to have a high probability of matching to a truth particle satisfying the above cuts. The *matching probability*, P_{match} takes into account that a track can have hits attached, that are generated by different particles and is defined as:

$$P_{\text{match}} = \frac{2N_{\text{common}}^{\text{pix}} + N_{\text{common}}^{\text{strip}}}{2N_{\text{track}}^{\text{pix}} + N_{\text{track}}^{\text{strip}}} \tag{4.1}$$

  where $N_{\text{common}}^{\text{pix/strip}}$ is the number of pixel/strip-detector hits common to both the track and the particle to which it is being matched, and $N_{\text{track}}^{\text{pix/strip}}$ is the number of pixel/strip-detector hits

assigned to the track. The factor of 2 included for N^{pix} arises due the the fact that each pixel layer provides one 2D measurement of the track whereas a double sided silicon layer provides two measurements.

The tracking efficiency, $\varepsilon_{\text{track}}$, is defined as the number of selected reconstructed tracks matched to a selected truth particle (satisfying the above cuts) with $P_{\text{match}} > 0.5$, divided by the number of selected truth particles (either muons or pions):

$$\varepsilon_{\text{track}} = \frac{N_{\text{rec}}(\text{selected, matched})}{N_{\text{truth}}(\text{selected})} \tag{4.2}$$

- **Mis-reconstruction**: There is no unique way to define the rate at which fake tracks are produced, and many of the definitions are sensitive to details of the reconstruction. For the purposes of comparison in this note, the mis-reconstructed track fraction is used, defined as:

$$f_{\text{fake}} = \frac{N_{\text{rec}}(\text{selected, unmatched})}{N_{\text{rec}}(\text{selected})} \tag{4.3}$$

  where $N_{\text{rec}}(\text{selected, unmatched})$ is the number of selected reconstructed tracks with $P_{\text{match}} < 0.5$, and the matching is to any charged truth particle.

- **Resolution**: Reconstructing tracks with a high efficiency and high purity is of limited use if the resolution in key track parameters is poor. The track parameters chosen in ATLAS are:
  - longitudinal and transverse impact parameter, z_0 and d_0;
  - transverse momentum, p_T;
  - polar and azimuthal angle, θ and ϕ.

  The resolutions for these parameters can be obtained from simulation by comparing their reconstructed values for a given particle with the MC truth value. The tracks used to calculate the resolution are required to pass the same selection as for the efficiency calculation. Tracks must be matched to a truth muon or pion with $P_{\text{match}} > 0.5$ and $p_T > 4$ GeV.

  To define the resolution, the difference between the reconstructed and generated variable is computed for each selected track. The RMS of the distribution is taken as the parameter resolution σ. In order to limit the impact of outliers, the RMS is calculated using an iterative procedure within $\pm 5\times$ RMS of the previous iteration.

4.2 Number of track hits

Figure 4.6 shows the average number of hits on tracks for the different ITk proposed layouts.

(a)

(b)

(c)

(d)

Figure 4.6. The average number of hits on muon tracks with $p_T = 100$ GeV for the (a) LoI, (b) pixel-disk layouts and (c) LoI-VF.

4.3 Tracking Efficiencies

source : Number 3 from https://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables
source : Number 4 from https://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables

4.4 Track Parameter Resolutions

source : Number 13 from https://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables
source : Number 14 from https://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables
source : Number 15 from https://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables

Figure 4.8 shows the track resolutions for (z0, d0, ϕ, θ, q and pT) vs eta + Resolution to project into Calorimeter.

4.5 Fake Rates

source : Number 17 from https://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables

fake rate vs. eta, fake rate vs. Nvtx

4.6 CP tracking performance

4.6.1 B-tagging (single plot? B-tagging eff/fake ?)

source : Number 7 from https://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables

4.6.2 primary vertex finding

reco Eff, Id Eff, z-resolution, transverse resolution, HS-PU separation *source : Number 11 from https://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables*
source : Number 12 from https://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables
source : Number 18 from https://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables

4.6.3 Electron performance

source : Number 5 from https://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables

what about brem recovery? ask Haichen/Tim ? egamma convenor?
Low pt electrons.
Does eff include brem recovery ? what is losses?

4.6.4 Photon performance

source : Number 8 from [[https://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables][List of deliverables from upgrade tracking][List of deliverables from upgrade tracking]]

4.6.5 Tau ???

4.6.6 Jet performance

source : Number 6 from [[https://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables][Lis
of deliverables from upgrade tracking][List of deliverables from upgrade tracking]]

TIDE - track separation in jets as fn of pt. - check TIDE plots? - TIDE results at strip radii

4.6.7 reconstruction of displaced particles

source : Number 9 from [[https://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables][Lis
of deliverables from upgrade tracking][List of deliverables from upgrade tracking]]

4.6.8 7.2.7 Occupancy (ours)

source : Number 16 from [[https://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables][L
of deliverables from upgrade tracking][List of deliverables from upgrade tracking]]

strip occupancy Ð density cm2, density in pile up , density jets staves a AND petals.

4.6.9 system redundancy

source : Number 20 fromhttps://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables

4.6.10 resource useage

source : Number 21 fromhttps://twiki.cern.ch/twiki/bin/view/AtlasProtected/ItkDeliverables#ListOfDeliverables

Figure 4.7. Efficiency for reconstructing prompt muons as a function of η (left) and p_T (right). MC statistical uncertainties are plotted, but are in many cases smaller than the symbol size.

Figure 4.8. Resolution of the track parameters d_0, z_0, ϕ, θ, q/p_T and p_T for reconstructed muon tracks in $Z \to \mu\mu$ events, calculated by comparing the reconstructed values for a given particle with the truth value from the Monte Carlo simulation. The true muons are required to have $p_T > 4$ GeV. The performance for the Middle layout is identical to the Reference for $2.7 < |\eta| < 3.2$. MC statistical uncertainties are plotted, but are in general much smaller than the symbol size.

5. ITk Silion Pixel Detector

This chapter is already rather advanced; it went already through one editing by Abe; now we need to see how the rest comes together for further steps[IMG]

5.1 Introduction

The Pixel detector for the ATLAS Phase-II Upgrade has been initially proposed in the Letter of Intent [7]. Updates were presented in the ITk Initial Design Report (IDR) [**?**]. Since then an intense detector R&D program and physics performance studies have resulted in converging on several general detector features as well as key technological options. Simulations are in progress to evaluate physics performance under several layout options. The final detector design will be described in the Pixel Technical Design Report that is due late in 2017. The current detector design and the on-going developments are presented in this document.

the next paragraph is repeating what will be described in the Layout Chapter earlier on - need to see if duplication is necessary or not[IMG]

One of the main changes in the Pixel layout since the IDR is the addition of a 5^{th} Pixel layer in the barrel. In order to maintain a neutral cost total for the ITk as a whole, the previously planned innermost layer of the Strip detector has been removed (see Chapter 3. Therefore the barrel tracker consists of five Pixel layers and four Strip layers. The 5-layer Pixel system will bring performance improvements such as better pattern recognition seeded in the Pixel volume, improved tracking efficiency and rejection of fake tracks and better two-particle separation. Another layout with a 6^{th} Pixel layer residing in the same Pixel volume has been proposed but the gain of a pixel hit is not sufficient to compensate the additional amount of material.

Although the final radial position of the Pixel layers is still to be optimized, the innermost layers will be located very close to the interation point and will be exposed to very large radiation which is expected for ten years of operation at an instantaneous luminosity of $5 \times 10^{34} cm^{-2} s^{-1}$. In order to prevent early loss of physics performance due to radiation damage in the silicon sensors and to anticipate a possible extension of the operations beyond the current schedule, the two innermost barrel layers will be removable and decoupled from the rest of the Pixel system.

The final layout of the Pixel detector is pending two important decisions which are being addressed by the ITk Layout Task Force: use of flat or inclined modules in the barrel layers and angle coverage with $\eta = 3.2$ or $\eta = 4.0$. In the inclined layout option tracks originating from the interaction point cross the modules at an angle close to normal. Compared to the classical layout in which the modules are postioned parallel to the beams, this option can potentially reduce the amount of modules needed, therefore the cost. The extension at high eta is motivated by better tracking and physics performance using phycics objects reconstructed in the very forward region.

Since the IDR, while intense detector R&D is still under way, major progress has been achieved in several areas and key technological options have been finalized. They are summarized in the following sections.

5.2 Modules

5.2.1 Introduction and Requirements

The basic electrical unit of the pixel detector is a module. Baseline module concept for the ITk

pixel detector is the well proven hybrid pixel detector which uses a sensor and the readout chip (ROIC) bump bonded to each other on a pixel level. In addition we also investigate other concepts like monolithic CMOS pixel detectors especially for the outer layers, see 5.2.7.

There will be two types of modules: 2-chip-modules (two chips bump bonded to a sensor, around 4×2 cm^2) for the innermost layer to accommodate the limited space, quad-modules (four chips bump bonded to a sensor, around 4×4 cm^2) for the outer layers and in the disks. For the innermost layer 3D sensors are the baseline sensor technology because of their advantages in power consumption and radiation tolerance. 3D sensors could also equip the second layer. For quad-modules the standard planar sensor technology is foreseen. Figure 5.9 shows a sketch of a quad-module based on the previous ATLAS pixel readout chip FE-I4 with 50×250 μm ^{2} pixel size. Because the new pixel readout chip is still in development the final size of this chip is not yet defined. For the time being we assume the same active size as for the FE-I4 pixel chip (16.8×20 mm^2) and a similar periphery region of 2×20 mm^2.

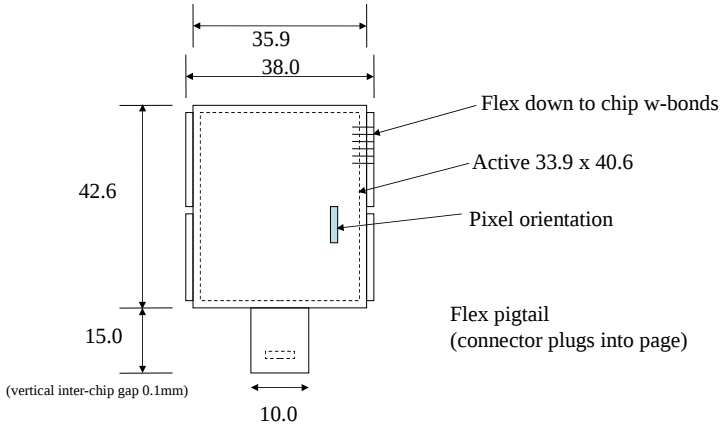

Figure 5.9. Drawing of a quad-module with four FE-I4 chips

The relevant parameters for barrel and disk modules are listed in table 5.5 assuming 25×100 μm ^{2} pixel size for the two inner layers and 50×50 μm ^{2} for the outer and disk layers. The fractions of inactive regions are kept low by having longer pixels at the edge and in the regions between chips, and by minimizing the edge region while still preventing voltage break down. Sensor and ROIC thicknesses are a compromise between material reduction and radiation tolerance improvements (which favors thinner sensors) for the inner barrel layers and rings and increased production yield and handling (which favors both thicker sensors and ROICs) for the outer layers.

All chips in the module will be controlled in parallel (shared clock and command inputs), but the module may have one or several dedicated data outputs. The multi-chip output data multiplexing functionality may be incorporated into the next generation pixel chips being developed or it could be implemented with a separate chip on the module as is done in current detectors. All connections (clock and command input, data output, low voltage and high voltage power) to the modules are done via a flexible printed circuit (flex-hybrid) which is glued to the backside of the

parameter	layer 1	layer 2	layers 3 - 5	disks
chips (ϕ x z)	RD53-FE 2x1	RD53-FE 2x2	RD53-FE 2x2	RD53-FE 2x2
pixel size (μm^2)	25 x 100	25 x 100	50 x 50	50 x 50
nb of pixels in ϕ	672	1344 +12 ganged	672 + 6 ganged	672 + 6 ganged
nb. of double columns in z	200	200	400	400
length of sensor at gap (μm)	300	300	450	450
distance to module edge (μm)	150	150	500	500
distance active to cut edge (μm)	100	100	100	100
active size (mm^2)	16.8 x 40.3	33.9 x 40.3	33.9 x 40.5	33.9 x 40.5
physical size (mm^2)	18.8 x 40.5	38.0 x 40.5	38.0 x 41.5	38.0 x 41.5
sensor thickness (μm)	100 - 150	100 - 150	200 - 250	100 - 200
ROIC thickness (μm)	100 - 150	100 - 150	200	200
power (W)	5.5	11.0	7.8	7.8

Table 5.5. Basic parameters of the pixel modules for the ITk pixel system.

sensor. The connections to the front-end chips and the sensor are done with standard wire bonds and passive components like decoupling capacitors and termination resistors are mounted on this printed circuit.

Apart from the sensor (section 5.2.2) and the front-end electronics (section 5.2.4) the key step in the classical hybrid pixel module integration is the fine pitch flip-chip bump bonding process which connects each pixel sensor with the corresponding FE readout cell. Bump bonding requirements for the Phase-II layout will be similar to those of the IBL modules, but experience with the present pixel detector and the IBL production showed the importance of multiple qualified bump vendors, see section 5.2.5 for more details.

Depending on the final layout decision of the ITk pixel detector, about 10,000 hybrid pixel modules are needed. High throughput and efficient assembly processes are mandatory. Therefore the ATLAS groups are pursuing an extensive prototype program on quad-modules [**?**], as well as high volume bump bonding using FE-I4-B wafers with several vendors. More than 100 wafers have been added to the IBL production order for such R&D efforts world-wide (the total order of 96 FE-I4B wafers contained more pixels than the present ATLAS and CMS detectors combined), as discussed further in section 5.2.6.

In many areas of the module development alternative approaches are being investigated. Among these are four side buttable dual and quad modules with Through-Silicon-Vias (when micro holes are produced after transistors and in a different factory). Such modules will relax the constraints on the mounting of the modules on the stave and potentially reduce the material budget. ATLAS pixel institutes evaluate alternative hybridization methods like capacitive coupling and industrial 3D integration processes as well as direct laser soldering to replace standard wire-bonding technology between module and flex-hybrid.

5.2.2 Planar pixel sensor technologies

A new generation of planar pixel sensors are under development for the ATLAS ITk pixel system.

The main differences with respect to the planar sensors implemented in the present detector are the different electrode arrangement (n-in-p versus the traditional n-in-n) and the reduced thickness in the range of 100-150 μm with respect to the 200 μm for the sensors used in IBL and 285 μm in the three outer ATLAS pixel layers.

The n-in-p technology allows for cost reduction given the single side processing and the reduced complexity in handling and testing. The guard ring structure is implemented on the front side, leaving the edges of the sensor at a potential close to the one of the back-side. This arrangement potentially induces the risk of electrical sparks between the sensor periphery and the chip. Isolation techniques like the deposition of a layer of Benzocyclobutene (BCB) on the sensor surface at wafer level or of parylene after module assembly have been successfully employed to prevent this problem [**?**, **?**]

Several studies have been performed to optimize the pixel cell structure in view of the smaller pitch of the read-out chip developed by the RD53 Collaboration (see 5.2.4). Two pixel cell structures are being investigated, 25×100 or 50×50 μm ^{2} cell size, the latter being the baseline option. New designs of planar sensors with 25×100 or 50×50 μm ^{2} cell size, based on beam test results obtained with the FE-I4 chip, have been implemented in prototyping productions already under process or completed.

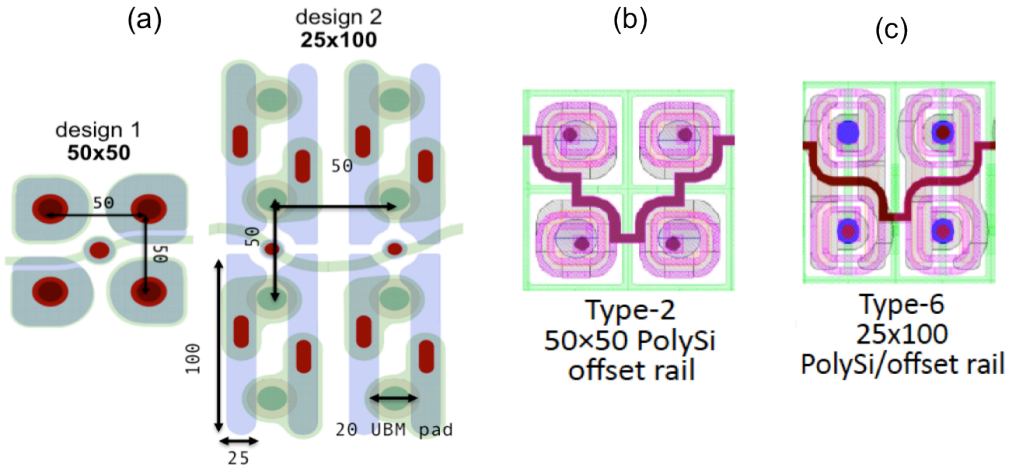

Figure 5.10. Design of 50x50 and 25x100 pixel cells implemented in (a) the MPG-HLL sensor production with a common punch-through for four pixels, and (b, c) in the HPK productions with Poly-Silicon resistor biasing, among other variants.

Preliminary results of the electrical characterization of these devices can be found in [**?**]. The cell optimization has been particularly focused on the biasing structures that induce a reduction of the efficiency after irradiation, for pixels where a punch-through dot or a poly-silicon resistor were implemented. Better performances have been demonstrated with a punch-through structure common to four cells or with a displaced bias rail in case of the poly-silicon resistors [**?**, **?**, **?**].

Thin planar sensors have been irradiated up to a fluence of 10^{16} $n_{eq}cm^{-2}$ to investigate the feasibility of employing them in the innermost pixel layers. Hit efficiency up to 97 % with FE-I4 modules have been reached with 100 μm thin sensors at a bias voltage of 350 V for a fluence of

5×10^{15} $n_{eq}cm^{-2}$ and at 500 V for a fluence of 10^{16} $n_{eq}cm^{-2}$ [**?**]. Pixel sensors with implanted sides to extend the depleted volume to the physical edges are also investigated for the innermost layer, where the maximization of active module area is particularly relevant [**?**, **?**].

Layers 2 to 5 in the new pixel system will be instrumented with quad-modules with a single sensor interconnected to four chips. Quad sensors compatible with FE-I4 chips have been produced at different vendors and good yields have been obtained also with these large area (around 4×4 cm^2) devices. Various inter-chip distances, in the range of 180-280 μm, have been used in the design of the sensors by implementing different number of ganged pixel rows in the sensor central area. The design of the inter-chip region will then have to be adapted to the finer pitch of the RD53 chip.

5.2.3 3D pixel sensor technologies

3D silicon detectors will be used for the inner most layer(s) of the barrel pixel system and some of the inner endcap rings due to their excellent radiation hardness at low operational voltages and moderate temperatures with low power dissipation compared to planar sensors. 3D silicon detectors have recently undergone a rapid development from R&D to industrialization with their first operation in the IBL. Shortly after, 3D devices have been installed in February 2016 as part of the ATLAS Forward Proton (AFP) detector, and are about to be installed in the CMS-TOTEM Precision Proton Spectrometer (PPS).

IBL-generation 3D pixel detectors have been found to have efficiencies larger than 97% at 170 V after irradiation to 10^{16} $n_{eq}cm^{-2}$, with a power dissipation of 15 $mWcm^{-2}$ at a temperature of -25C$^\circ$ [**?**], see figure 5.11.

The 3D design under development for the ITk detector builds on the successful IBL 3D sensor. Columns of 5 to 10 μm diameter are alternately n- and p-type doped into the high resistivity p-type silicon bulk, defining the pixel configuration. In the IBL 3D sensors, the columns were etched from both sides of the wafer (double sided process), which allows to produce sensors with thicknesses down to 200 μm. Moreover, the single sided approach on a support wafer is also well established at several 3D fabrication facilities, which allows for thinner sensors. Active thicknesses of 50-200 μm are currently being investigated at various production sites. The 3D sensor technology inherently allows for slim edges of 15-150 μm [**?**], or even active edges sensitive up to the physical sensor edge [**?**].

Productions of 3D devices with smaller pixel sizes of 25x100 and 50x50 μm^2 compatible with the FEI4 chip have already been carried out and the prototypes are currently being tested [**?**][**?**][**?**]. Furthermore, specific productions of 3D sensors compatible with the RD53 chip, design shown in Fig. 5.12, have also been completed.

Though performance is the decisive factor for the relatively small size of the innermost pixel layers, the 3D technology is reducing its cost and production time, while improving the yield, by optimizing the 4" production line and establishing new 6 lines [**?**], [**?**].

5.2.4 Pixel Front-end electronics

The RD53 Collaboration [**?**] is developing the pixel readout chip technology for both ATLAS and CMS in HL-LHC. This is a critical path item for both experiments. A first large format chip to demonstrate the results and allow the experiments to test sensors meeting HL-LHC requirements,

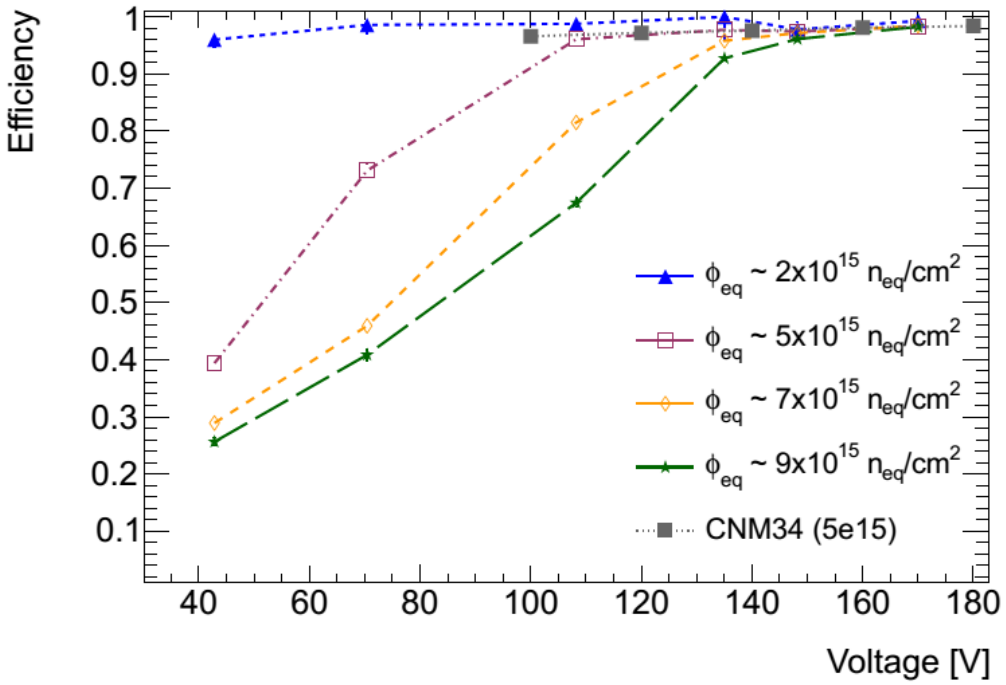

Figure 5.11. Hit efficiency as a function of bias voltage for different fluence regions on a non-uniformly irradiated 3D FEI4 detector

called RD53A, is planned to be submitted at the end of 2016. Detailed specifications for the RD53A have been approved by both experiments and released as a public document in 2015 [**?**]. The RD53A chip embodies the main deliverable of the RD53 collaboration. RD53A will be produced in wafer form, allowing developement of wafer testing on 300 mm diameter wafers. Significant testing of hybrid modules built with RD53A chips would take place in 2017/18. Design of a production chip for ATLAS will start in 2017, relying heavily on RD53A and initial test results, and using the tools, basic blocks, and design environment provided by RD53. A requirements document for the ATLAS production chip is being written in 2016.

While the plan is to use the same readout chip in the entire detector, the most critical performance requirements are driven by the innermost layer. Compared to the FE-I4 chip [**?**] used in the present inner layer (IBL [**?**]), the HL-LHC requires large improvements in several parameters at once. The new pixel size must be 20% that of FE-I4, essentially due to the 5-fold increase in particle flux (by comparison, the FE-I4 chip pixel size is only 63% that of the original pixel detector). Yet at the same time, the hit threshold must be drastically reduced to 600 electrons instead of 2000 electrons (in response to thinner sensors and heavy sensor radiation damage), all without a significant power increase. Additionally, the trigger rate will be increased by an order of magnitude. Therefore, while the readout bandwidth of one FE-I4 chip in the IBL is 160 Mbps, the new inner layer will require an estimated 5 Gbps per chip (not only is the trigger rate higher, but the events are also busier, while the chip size is assumed to the the same as FE-I4). The magnitude of these challenges was recognized early on, and the RD53 collaboration was formed to attack

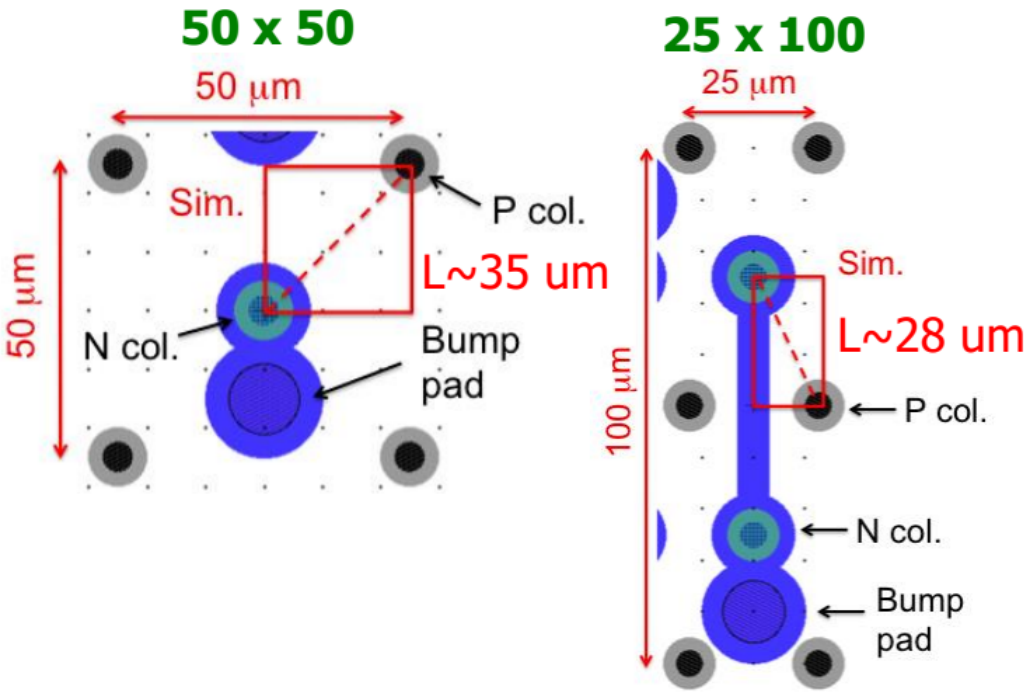

Figure 5.12. Design of 3D pixel cells with 50 × 50 and 25 × 100 μm ^{2} size.

them. A 65 nm feature size CMOS technology (through a CERN frame contract) was selected to address them. Several alternative candidate platforms were also investigated, including 3D silicon integration with 130 nm feature size as a candidate solution.

High radiation tolerance is of course a critical requirement. Following the initial studies of the chosen 65nm feature size process, more detailed and extensive studies by RD53 and the CERN Microelectronics group revealed some unexpected issues, including a previously unknown effect now called Radiation Induced Short Channel Effect or RISCE [**?**]. Like the already known Radiation Induced Narrow Channel Effect (RINCE [**?**]), this is a fundamental CMOS damage mechanism, not peculiar to any vendor or foundry. These two effects together mean that the thing that is necessary for high logic density, namely small transistors, is bad for radiation tolerance. High logic density is mandatory to have small pixels with high hit rate and long trigger latency. Fortunately, with only modest compromises on logic density (still much higher density than could be achieved in FE-I4), the RD53A design is being made to meet specifications after 500 Mrad dose. This value stems from the fact that RD53 has developed simulation models for transistors up to this dose. Simulation beyond 500 Mrad is much more difficult because degradation becomes highly dependent on voltage and temperature conditions and history. Of course, the RD53A chip will be tested beyond 500 Mrad. Nevertheless, a design with removable inner layers is prudent at this time, since performance beyond 500 Mrad is uncertain. At the same time, work on radiation damage continues. A particular focus is understanding low dose rate damage and annealing effects. For the CERN frame contract 65 nm CMOS process, annealing under power (after initial irradiation) causes additional degradation. This is not an issue for low temperature operation, but it does appear to be

a vendor-specific effect, demanding further scrutiny. It is interesting that sensor radiation damage also becomes uncertain after 10^{16} $n_{eq}cm^{-2}$ (same luminosity as 500 Mrad), and mitigation also requires cold operation, in spite of completely different damage mechanisms.

While the RD53A chip is the main prototype that the production readout chip will be based on, a small scale demonstrator called FE65-P2 [**?**] was produced in a multi-project run in late 2015, with miniature first sensors bump bonded in mid 2016. FE65-P2 has the same pixel size and same CMOS process as RD53A, and was intended to demonstrate the layout approach where digital logic completely surrounds 4-pixel amplifier blocks called "analog islands in a digital sea", together with the superb analog-digital isolation needed for 600 electron threshold stable operation. FE65-P2 results are excellent, giving significant confidence to the RD53A design. While FE65-P2 did not use the radiation hardened logic of RD53A, performance is still good after 500 Mrad.

5.2.5 Interconnection technologies

A key step in the fabrication of the hybrid pixel assembly is the flip-chip bump bonding process. There are two major challenges facing the flip-chip bonding of the ATLAS pixel system. The first is the technical challenge posed by the requirement to produce very thin pixel assemblies targeting 100 - 150 μm for the inner layers. The second challenge is the production rate and volume required for the substantially enlarged pixel system.

The specifications for the bump deposition and flip-chip process are under development based on those successfully used for the IBL production [**?**]. Additional requirements include; increased wafer sizes: 300 mm diameter readout chip wafers (increased from 200 mm), sensor wafers up to 200 mm diameter (increased from 100 mm), as well as readout chip and sensor thicknesses reduced to 100 - 150 μm. ATLAS used readout chips of 200 μm in thickness but these were only 7.4 $\times$ 10.9 mm^2 in size. While IBL was made from larger (FEI4 16.8 $\times$ 20 mm^2) readout chips of 150 μm the number of modules made was very limited and required specialized handling techniques.

Modification of the specifications take into account the larger number of pixels per chip and the five times higher bump density with a pitch of 50 μm in both directions. The increased bump number and density will impact on both the bump realisation and the flip-chip processes. The bump failure rate will remain the same as for the IBL. The details of the specifications are being developed in collaboration with the vendors that the pixel groups are working with during the R&D phase. The pixel specifications will not place a requirement on the detailed technology of how vendors produce the module but will assess the quality of the product via a qualification process. The qualification process will be based on that used for the IBL, but will additionally include a HALT (Highly Accelerated Life Test) and HASS (Highly Accelerated Stress Screen) program and will take into account the lower operational temperature of the modules. A development programme based on the FEI4 wafers are being used for the first stage of vendor engagement. A bump test structure is under development on 300 mm diameter wafers to allow process development at the final wafer diameter before the delivery of a significant number of RD53 chips in mid-2017.

As with the present ATLAS detector both Indium and solder bumps are under development. The flip-chip bump bond process is broken into five stages.

- The first is the deposition at wafer level of a solder wettable metal layer (under bump metal

UBM) on the pixel pads for both the sensor and readout chip. To reduce cost, development is taking place to allow the sensor UBM to be deposited by the sensor vendors.

- The second stage is the bump deposition on the wafers. For solder the bumps are electroplated on the readout chip wafer only. The indium process requires indium bumps to be evaporated onto both the sensor and the read-out wafers.

- Wafers are thinned to the desired thickness, before or after bump formation depending on technology, and diced after bump formation.

- For the frontend chip thickness below 400 μm require vendor specific techniques to handle chip bow during the flip-chip process to prevent disconnected pixels and these may be applied at wafer level depending on technology.

- Finally, the parts are attached via the flip-chip process. The flip-chip process requires the alignment of the two die and the application of heat and pressure to make the bond. For solder a reflow at 230 C$^\circ$ is required, while indium uses temperature from 30 to 100 C$^\circ$ during the flip-chip process.

One of the most significant technical challenges is the handling of thin readout wafers. The chip bow increases with reducing thickness, increasing die size and increasing temperature. The use of elevated temperatures causes the read-out chip to bow still further, due to the CTEExplain TLA^{MS} mismatch between the chip thick front end metal and dielectric stack and the silicon substrate, resulting in disconnected bumps.

Four different processes have been investigated to enable thin chip flip-chip by the perspective ATLAS flip-chip vendors that show the challenge has been successfully met. The first is a low temperature flip-chip processing using indium bumps; either free standing or as a cap on a nickel pillar (Selex, Ral and HPK). The chip is held flat on the vacuum tool of the flip-chip machine while the bond is performed at modest elevated temperature. The die is released only after the chip has returned close to room temperature. This process has been shown to work well, but has the disadvantage of reduced flip-chip through-put. To mitigate against this, flip-chip at various laboratories is being investigated using bumps deposited in industry. The second process developed at IZM, and successfully used for the IBL, employs a temporary glass carrier wafer bonded to the backside of the thinned readout chip wafer that prevents the chip from bowing during the solder re-flow process. The carrier wafer is removed after the flip-chip process. Again the flip-chip process is the bottle neck of this method and development to increase through-put is taking place. The last two processes aim to produce solder based flip-chip without the use of a carrier wafer to increase through-put. The third method uses a reducing atmosphere during a solder reflow stage immediately before flip-chip on the flip-chip machine (HPK), where the chip is held flat during reflow and allowed to cool before removing from the machine. The final method uses a dielectric and metal layer deposited on the backside of the readout chip wafer to balance the bow induced from the front-side stack (CEA Leti/Advacam). This layer is not removed after flip-chip. These two processes have produced a number of high yield assemblies on thin die and are under-going further development.

The ATLAS pixel community is actively working with six suppliers of flip-chip bump bonding technology. The large number of suppliers has been chosen so that we increase the likelihood of solving the challenges imposed for volume production of thin chip assemblies as well as allowing a meaningful choice of supplier at the tender stage. The vendors are given in Tab. 5.6 with their bump technology, thin chip handling option and their level of maturity in the ATLAS pixel project.

Vendor	Bump technology	bonding technology
IZM	SnAg solder	Solder reflow at 230 C°
Selex	Indium	Thermal compression 100 C°
HPK	Indium on Nickel pillar	Low temperature thermal compression
HPK	SnAg	Solder reflow on flip-chip machine
CEA LETI and Advacam	SnAg solder on copper pillar	Solder reflow at 230 C°
RTI	SnAg solder	Solder reflow at 230 C°
RAL	Indium	Room temperature compression

Vendor	thin chip bonding demonstrated
IZM	150 μm FEI4 chip demonstrated
Selex	100 μm FEI4 chip demonstrated
HPK	150 μm FEI4 chip demonstrated
HPK	150 μm FEI4 chip demonstrated
CEA LETI and Advacam	100 μm FEI4 chip under development
RTI	250 μm FEI4 chip demonstrated. Thinner under development
RAL	Thin chip not demonstrated

Vendor	thin chip handling option
IZM	Temporary handling wafer
Selex	Bonding on vacuum jig of flip-chip machine
HPK	Bonding on vacuum jig of flip-chip machine
HPK	Reducing-Reflow on flip-chip machine
CEA LETI and Advacam	Developing chip backside process to compensate bow
RTI	Under development
RAL	Bonding on vacuum jig of flip-chip machine

Vendor	Experience in Particle physics
IZM	High âĂŞ built present ATLAS pixel and IBL
Selex	High âĂŞ built present ATLAS pixel
HPK	New to particle physics
HPK	New to particle physics
CEA LETI and Advacam	Leti new to particle physics. Advacam used with ALICE pixels
RTI	Used for CMS pixels
RAL	New to flip-chip bump bonding

Table 5.6. Flip-chip bump bond vendor candidates for the ITk pixel system.

The technology at the various vendors is at different levels of development. The FEI4 chip has

been used to develop the technology to date. There are many more 200 mm diameter FEI4 wafers available to allow further process development over the coming year to allow all the identified vendors to fully demonstrate thin module processing. In addition, a bump bond test wafer processed on a 300 mm diameter wafer in being produced. This will allow the vendors to demonstrate the process with the final wafer diameter, bump density and die size. The RD53 chip will be available in the middle of 2017 by which time the vendors will be ready to produce RD53 based pixel assemblies. Some vendors will require the RD53 wafers for further optimization of thin chip processing in the second half of 2017 and early 2018. No significant flip-chip bump bonding development is expected for the ATLAS pixel chip.

The HL-LHC pixel system will have of the order of 10,000 pixel assemblies mainly consisting of 4-chip modules. This represents an increase of over five times the number of modules and approximately three times the number of front-end chips compared to the present ATLAS pixel system. The start date for module production is driven by the front-end chip development, while the completion date is dictated by the HL-LHC turn on date (see section **??**No Schedule Chapter, is this the Production one?[MS]). These constrains limit the total module production duration to at most 30 months. The rate limiting steps for module production is flip-chip bump bonding and pixel module characterisation. The bump deposition will have to be completed approximately six months before module production is finished to allow time for flip-chip and module characterisation. The 300 mm diameter wafers, produced at a high through-put fab, are estimated to produce 88 good chips per wafer. The use of larger wafers reduces the pressure on the bump deposition facility (reducing wafer count by 2.4 times compared with that required with 200 mm wafers) but reduces the number of facilities that can handle the larger wafers. Therefore, approximately 500 wafers will be required to be processed with bumps in 24 months, or an average of 20 wafers per month. A typical wafer lot is twenty wafers and takes about three months from start to finish to process. If three vendors with equal capacity are chosen they will process eight wafer lots each over two years, which is very manageable for all the vendors under investigation. The rate limiting flip-chip step may require more than three vendors. Various laboratories (e.g. RAL and Barcelona) are able to supplement commercial flip-chip vendors and this option is being investigated to guarantee supply.

A test of such a sustained high production rate is not possible during the R&D phase of the project. Several small production runs have been launched with 400 μm thick FEI4 wafer to give some evidence of a robust bump deposition process and fast flip-chip production. Lessons have been learnt from these runs and processes have been made more reliable. Further larger runs will continue through-out 2016 with the FEI4 wafers and 300 mm diameter bump bond test wafers at several vendors.

5.2.6 Module assembly and prototyping

An example of a first prototype quad-module with the FE-I4B chip is shown in Fig 5.13. Several flex PCB circuits have been developed for quad pixel modules exploiting the experience of the two chip IBL flex. The quad module flex is designed for serial powering and AC coupled communication. The flex has a single clock and command bus for the four chips but individual data outputs per chip. Presently it is assumed that the data links from the four chips of one module will be multiplexed together and transmitted electrically to PP1 (section 5.5). The concept of multiplexed data from the four FEI4 chips has been demonstrated with a module hosting a commercial

CMOS multiplexing chip. The final data multiplexing chip will be designed using IP blocks from the RD53 collaboration and mounted on the module flex. The flex also supports the PSPP chip (section 5.6) to enable the DCS functionality including module power bypassing required in case of module failure. A redesign of the quad flex to adapt it to the particular geometry of the barrel I-beam design is underway.

The FEI4 chip serial data LVDS output runs at 160 Mbps while the RD53 chip will have fast serial output with a maximum speed of 5 Gbps. While the output data rate per chip for all but the inner layer will be less than the maximum, data multiplexing of chip data results in Gbps data links on all modules. The next designs of the module flex will be produced in the coming year to handle these fast data rates. They will initially be tested in a similar fashion employed for the data links (see section 5.5) before being used to make RD53 chip based modules at the end of 2017. Many modules will be made to allow module construction and testing techniques to be developed ahead of the Pixel TDR as well as to produce a stock of modules for system tests.

The flex PCB will be produced in industry and the vendor will be responsible for guaranteeing the quality of the product, including cleanliness. The development of flex to pixel assembly techniques is starting. Presently several techniques are under investigation at different laboratories and these will be reviewed and qualified in due course. The rate limiting step for module production is module characterisation. The module testing process will be based on that used for the IBL and is presently under review. It will include a HALT and HASS program for quality assurance as well as standard tests for quality control. The development of the characterisation process is based on the FEI4 modules being produced for the bump bonding development. During the next six months more than 100 modules will be made and used to develop the module characterisation process. Parallel test facilities will be used to allow batch testing of modules such that the production schedule will be met. DAQ developments allow for the testing of many FEI4 chips in parallel at reasonable cost. Present DAQ systems include inexpensive FPGA cards, connected to a PC via USB3, (e.g USBpix3) capable of characterising a quad module and more advanced DAQ cards (HSIO-II) capable of characterising 18 front-ends (equal to 4.5 quad modules) in parallel.

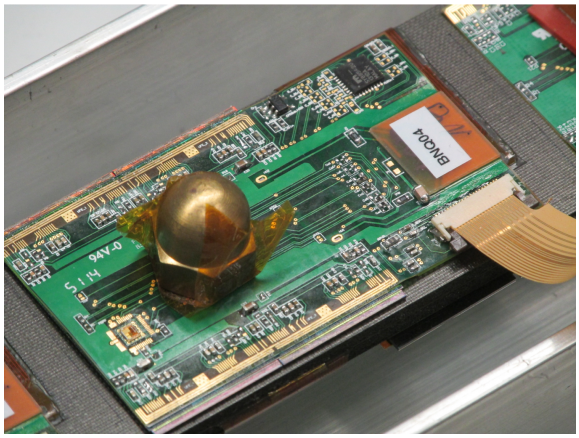

Figure 5.13. Prototype of the quad-module with four FE-I4 chips.

5.2.7 CMOS

CMOS pixel detectors with charge collection in an epitaxial layer (10-20 μm thick) have been developed since 2001 [**?**] and have become realized in the STAR pixel detector at RICH [**?**] and are also proposed for the ALICE ITS Upgrade [**?**]. For the rate and radiation environment expected at the HL-LHC new approaches have been developed [**?**, **?**, **?**, **?**, **?**] based on the following enabling technology features:

- HV add-ons that allow to use high depletion voltages (HV-MAPS).
- High resistivity wafers for large depletion depths (HR-MAPS).
- Radiation hard processed with multiple nested wells to allow CMOS electronics embedded with sufficient shielding into the sensor substrate.
- Backside processing and thinning for material minimization and backside voltage application.

A typical CMOS sensor pixel cell with sensing substrate and a CMOS electronics layer embedded in multiple cells is shown in Figure 5.14.

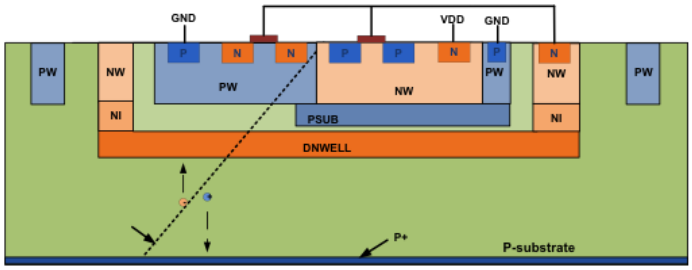

Figure 5.14. DMAPS schematic showing fully or partially depleted bulk, multiple nested wells for CMOS electronics and charge collection node.

R&D within ATLAS has started about 2010. Currently members of more than 20 groups in ATLAS are actively pursuing CMOS pixel R&D in an ATLAS Demonstrator program (sensor design and characterizations) started in 2014. The program's first goal was to demonstrate that depleted (monolithic) CMOS pixels (DMAPS) are suited for high rate and high radiation operation at LHC. For this a number of technologies have been explored and characterized: AMS 350 nm and 180 nm, Global Foundry 130 nm, ESPROS 150 nm, LFoundry 130nm, TowerJazz 180nm, Toshiba 130 nm, XFAB 130 nm (SOI), ST-M 160 nm. The designs have been characterized as stand-alone sensors as well as bonded to the FE-I4 pixel chip (as a 'hybrid') either via bump bonds or via glue bonding (capacitively coupled pixel detector, CCPD).

The results within the demonstrator program can be summarized as follows:

- Technologies complying with the above enabling technology list are principally suited to fabricate depleted monolithic sensors that can cope with the HL-LHC running condition, at least at distances larger than 20-25 cm away from the interaction point (outer layers).

- DMAPS pixel sensors detect mips with integrated efficiencies above 98% and with spatial resolutions similar to those as hybrid pixels ($50 \times 100 - 200\ \mu m^2$, possibly$50 \times 50\ \mu m^2$).
- DMAPS pixel sensors can stand radiation fluences of more than 10^{15} $n_{eq}cm^{-2}$ when properly designed. This is demonstrated in Fig. 5.15 showing the depletion depth obtained after irradiation to a neutron fluence of 5×10^{15} $n_{eq}cm^{-2}$ determined using edge TCT measurements.
- Testbeam measurements have shown high rate capability as detectors bonded to the FE-I4.
- Fully monolithic DMAPS pixel sensors have been designed incorporating readout architectures suitable to cope with the expected rates at the HL-LHC such as (column-drain architectures and direct hit transfer architectures). Such designs have been submitted for fabrication in 2016 and are currently evaluated (text to be modified depending on TDR issuing).

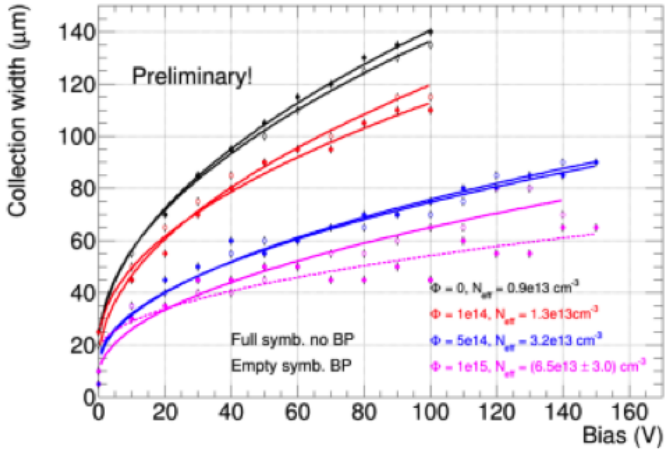

Figure 5.15. CMOS Pixel sensor (LFoundry) after 5×10^{15} $n_{eq}cm^{-2}$ demonstrating that depletion depths in the order of 50 μm can still be achieved after high irradiation.

5.3 Local Supports

5.3.1 Introduction

The design of the mechanics is deeply related to the detector layout. In general, the active elements should first be distributed in the detector volume, the mechanical structures can then be developed around them. The Layout is the input to the mechanic design.

However, as explained in section 5.1 the layout has not been finalized and two options are being evaluated for the barrel section. Different mechanic concepts have been developed so far providing solutions for both layouts. Prototypes have been produced and they are under test to verify their performances against the relevant requirements.

It is therefore mandatory to specify the requirements for the local supports and in particular those which are relevant for the current phase of the developement process. The complete description of the Pixel local support specifications are described in the following.

5.3.2 Requirements and specifications

Requirements are a set of functions that a design must guarantee. The specifications define the metric and the performance values that are needed to meet the requirements. They are numerical values that the qualification process evaluates on prototypes or via calculations.

The set of specifications (geometry, stability and thermal performance) for the local supports are described in the ATU-SYS-ES-0029. However, stabibility and thermal performance are the most relevant requirements in the current state of the detector development.

Thermal Performance Specification:

The thermal performance requirement insures that the modules will not suffer the so called thermal run-away at the end of the detector life. The metric for the requirements is given by the parameter Thermal Figure of Merit (TFM) and it is typical of any local support design.

Parameters and Safety Factors			
	Nominal	SF	Design
Nominal Luminosity			
Fluence at R=39mm at $3000 fb^{-1}$	1.33E+16	1.5	1.99E16 ($n_{eq}.cm^{-2}$)
Layer Radii			
Layer 0			39mm
Layer 1			75mm
Layer 2			160mm
Layer 3			250mm
Layer 4			345mm
Sensors			
Pixel size along Z			50 μm
Pixel size along ϕ			50 μm
Max Pixel Current			10 nAmps
Inner pipe ID			2.4mm
Evaporation Temperature	-35C	5.0	-30C
CO_2 Heat Transfer Coefficient	8000	1.3	6154 $W/K.m^2$
σ_{TFM}			16.7%
σ_{TFM} acceptance			3σ

Table 5.7. Parameters and Safety factors of the Pixel detector. Max Pixel Current: the maximum single pixel current the front-end chip can handle. Depending on the sensor technology this current can be a limiting factor even though the runaway limit is not reached. σ_{TFM} and σ_{TFM} acceptance: There will be variation of the TFM value both along the length of the local support and between local supports. The standard deviation of the TFM distribution is estimated to be 16.7%. The acceptance criteria is set to 3σ, meaning that a variation of 50% of the specified TFM value is accepted.

TFM is defined as the ratio between the temperature difference (ΔT) between the evaporation fluid and the hottest spot on the sensor and the module power per unit of area Φ_{mod}.

The unit is ${}^{o}C.cm^2.W^{-1}$ and it can be considered as the thermal impedance of the structure cross section. A low TFM corresponds to low temperature on the sensor. The total TFM (Γ_{TOT}) is made from several contributions: the Heat Transfer Coefficient (HTC) in the pipe, the interfaces in the local support cross section and the heat conduction in the materials. The total TFM can be split in two contributions: the convective part since it is related to the HTC of the boiling C02 and the conductive part that depends on the thermal conductivity coefficient of the materials and interfaces in the local support structure.

$$\Gamma_{TOT} = \Gamma_{HTC} + \Gamma_K \tag{5.1}$$

Γ_{TOT} can be measured experimentally on prototypes imposing a heat flux generated by silicon heaters and a boiling C02 flow in the cooling pipe. The temperature on the sensor is given by:

$$T_{sensor} = \Gamma_{TOT}.\Phi_{mod} + T_{evap} \tag{5.2}$$

Where Φ_{mod} is the heat flux from the module $[W.cm^{-2}]$. The heat flux from the module Φ_{mod} is the sum of two contributions:

- The Front End Chip (FE).
- The sensor power dissipation caused by its leakage current.

While the first contribution is constant and depends on the hit rate only, the sensor power depends on the radiation dose. The dependency is exponential and since the ΔT increase is, in first approximation, linear with the power. This may trigger a thermal runaway as the radiation dose increases.

Assuming a design evaporation temperature T_{evap}, Γ_{TOT} can be set as a specification for the local support such that, at the end of the detector life, there will still be a margin against the thermal runaway. The required Γ_{TOT} depends on assumptions on several detector operational parameters and onthe safety factors used in the calculations to estimate somr unknown parameters. Some of the assumptions and the most relevant safety factors are listed in Table 5.7.

The TFM specifications are determined under the assumptions made in Table 5.7. The conductive TFM [Γ_K] is more representative of the thermal performance of the structure itself. However the final temperature on the sensor is set by the total TFM (Γ_{TOT}). Disentangling the convective and conductive contribution is experimentally rather difficult and often unreliable. The tests performed on prototypes measure the total TFM. The specifications are provided in terms of both conductive and total TFM.

Figure 5.16 shows the conductive TFM_K. Given that the radiation fluence depends on the layer radius, the TFM is shown for each layer. Moreover, the requirements depend also by the type of sensors. The planar sensors dissipate more power than the 3D sensors due to the higher depletion voltage.

For 3D sensros the most limiting parameter is the single pixel current, while for planar sensors the limitation is the runaway. The grayed area below $10C.cm^2.W^{-1}$ is considered off-limits in the sense that the actual technology does not allow to reach such a low thermal impedance. It is clear that the planar sensors cannot be considered for the first two layers if the evaporation temperature is not reduced below -35C°. Developments are under way to lower the CO_2 operating temperature.

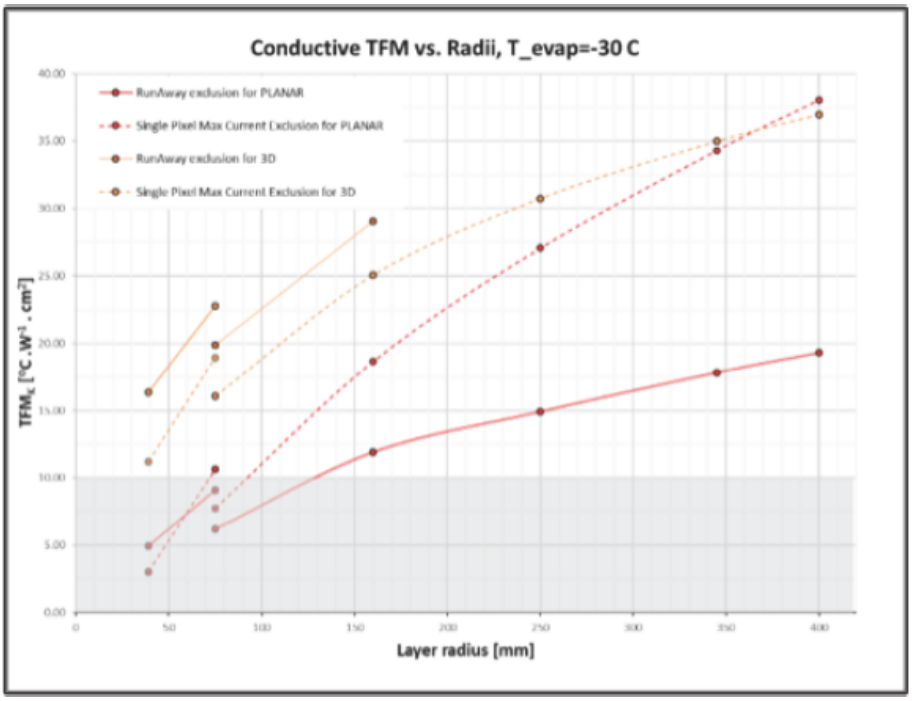

Figure 5.16. Conductive TFM. The solid lines give the conductive TFM limit required to cope with the thermal runaway in Orange for the 3D and Red for planar sensors. The dotted lines show the limit for the MAX PIXEL Current with the same color coding. Very bad quality figure - needs to be replaced; also need to know the source of this figure[IMG]

Hereafter the pixel detector is assumed to be equipped with 3D sensor in the two innermost layers (Layer 0 and Layer 1) and planar sensors for the outermost three layers. Table 5.8 summarizes the TFM specifications providing both the total and the conductive TFM for the detector configuration described above. The conductive TFM for Layer 0 and 2 is rather aggressive.

Layer	TFM_K	TFM_{HTC}	TFM_{TOT}
L0 (3D)	11.22	4.31	15.53
L0 (Planar)	2.99	4.31	7.30
L1 (3D)	16.08	8.62	24.70
L1 (Planar)	6.20	8.62	14.82
L2 (Planar)	11.91	8.62	20.53
L3 (Planar)	14.92	8.62	23.54
L4 (Planar)	17.83	8.62	26.45

Table 5.8. Specifications for the Thermal Figures of Merit.

Operational Temperature Range (OTR): The estimate of the OTR is based on the minimum evaporation temperature on the low side and on the interlock system on the high side. The interlock system will switch off the power on modules in case the temperature rises above +40C°. The nom-

inal temperature range can be therfore be set at $-35\text{C}^\circ < T < +40\text{C}^\circ$. However, a safety margin of 20C° is been added to the range specifying the OTR to be $-55\text{C}^\circ < T < +60\text{C}^\circ$.

Humidity Range (RH): The Pixel detector will be operated in a dry nitrogen environment at a constant dew-point. However, the temperature variation of a constant dew point gas produces variation of its relative humidity RH. Composite structures react to it with medium long timescale affecting the geometrical stability of the detector. For this reason, the range $0\% < RH < 80\%$ has been set for the detector volume.

Radiation Hardness: The following specification on the radiation dose applies to the structural material only and are not be used to address the radiation damage for sensors and electronics. Radiation deteriorates the mechanics characteristic of the material generally causing embrittlement and stiffness change. The requirement is calculated assuming a safety factor of two and is 1.54 Grad.

Material Budget: The specification for the mass budget of the local support is given by means of target value. The goal is to minimize the total structure mass per layer in terms of radiation length. The target value is, for the structures only with no modules, 0.5% and 0.6% X/X0 for the Innermost and Outermost layers respectively.

Stiffness: The stiffness requirement is given in terms of maximum gravity sag (Max 100 μm) and/or in terms of minimum resonance frequency. The two parameters are not independent with each other and they can be applied separately. The specifications assume that the local supports are loaded with modules and services.

Layer Hermiticity: The Hermeticity specification has two folds. The first one set the minimum number of pixel of overlap in the Φ axis once all the loads described above are applied. The goal is to guarantee at least five pixel overlaps in any operational condition. However, in the R-Z plane the minimum hermeticity per layer is set to 98.5% per layer due to the unavoidable longitudinal dead gap between modules sharing the same Local Support.

Maximum Design Pressure (MDP): The local supports house the cooling pipe in which the CO_2 evaporates to evacuate the heat generated in the services and in the modules. In general, the cooling pipe is embedded in the structure and is subjected to high pressure. The specification on the MDP of the cooling line is driven by the safety release systems that will be implemented in the cooling plant. Those are either release valves or rupture disks. In particular, the CO_2 transfer lines, running from the cooling plant to the detector, will be equipped with rupture disk at 130bar. Therefore, the pipes in the detector could experience such a pressure and the MDP for the on-detector piping necessarily needs to be set to 130 bar. So far ITk has defined the pressure code to be used for the design. The Pressure European Directive (PED) defines, among other parameters, the safety factor to be applied for the pressure test qualifying the pressurized sections of the cooling system. According to the code the pressure test must be 1.43xMDP leading to a test pressure of 186 bar.

Geometrical Stability: One of the most relevant specification refers to the position stability of the modules in the detector volume. Those are conformal to a more general specification document issued at a ITk level covering stability requirements for the whole ITk detector [G. Viehhauser et al.]. Stability requirements are given for two time ranges over which a set of load variations have been defined: Short is a timescale of 1 day, Medium in a timescale of 1 month. The loads variation be considered in order to address the stability requirement over the two time intervals are as follows:

- Short: 10% power dissipation in the FE chip and in the services; $\pm 1C$ evaporation temperature variation.

- Medium: Relative Humidity variation of the detector environmental gas from 10% to 50%; $\pm 3C$ evaporation temperature variation.

Given the loads variation above, the speciifcations for the geometrical stability are listed for both timescales in Table 5.9.

	Nominal (μm)	Safety factor	Design (μm)
Short - 1 day stability period			
δR	7	1	7
$\delta \phi$	7	1	7
δZ	14	1	14
Medium - 1 month stability period			
δR	17.4	1	17.4
$\delta \phi$	17.4	1	17.4
δZ	34.8	1	34.8

Table 5.9. Specifications of geometrical stability. Values are given by means of absolute maximum stroke in μm on each axis

5.3.3 Qualification process for barrel local supports

The final Layout will be selected on the basis of the Physics performances. However the barrel local support candidates will go through a preliminary qualification process in order to ensure that one option will meet the specifications. The qualification process will carried out on a limited but relevant subset of the requirements. The complete thermal and mechanical qualification will be performed later (by the Pixel TDR, scheduled late in 2017) and it will only apply to the candidates of the selected layout.

Preliminary qualification

- Validation of the nominal Thermal Figure of Merit. The measurement of the conductive and convective TFM requires dedicated equipment based on a C02 evaporative cooling system. The local support is loaded with 300 μm thick silicon heater mimicking the front end chip and the sensor (both assumed with $150 \mu m$ thickness. At least three silicon heaters are loaded on each structure. The prototype pipe is connected to the CO_2 cooling system and a current is run through the heaters. A number of thermal sensors are placed on the structure in order to measure the evaporation temperatures in the boiling channel and the ΔT increase profile in a few places up to the hottest point on the silicon heater.

  The test is run in a dry air environment and to subtract the effect of the heat pickup from the environment, ΔT is measured by scanning both the evaporation temperature and the power dissipated in the heaters. In all the cases the heater temperature is kept below the environment

temperature, the heat will therefore always flow from the air to the structure. This leads to systematically underestimate the effective power delivered to the structure and, consequentially, overestimate the TFM (high TFM means low thermal performance) that, in reality, will be in better or equal to what is measured .

The impact of the heat picked up from the environment decrease with increasing power dissipated in the heaters for two reasons: a) the temparaure increases in the silicon with the electrical power. The temperature gets closer to the air temperature and the heat pickup decreases linearly. b) the heat picked up is relativaly smaller at higher electrical power and its impact to the heater temperature decreases.

As long as the silicon heater is always kept below the environment temperature, the contribution to ΔT given by the heat pickup is asymptotically cancelled out by increasing the electrical power.

This is what has been experienced in the first tests on real prototype. Figure 5.17 shows the TFM as a function of the heat flux. The purple curve gives the TFM of a specific prototype. It is calculated via the value of the thermal sensor placed on the hottest place on the silicon heater. The other curves refer to other thermal sensors placed in intermediate positions. The TFM decreases with increasing of the heat flux from the silicon heater. It is the combined effect of the reduced heat pickup from the environment (due to a smaller temperaure difference between the heater and the air) and the decreased percentage of the heat picked up with respect to electrical power injected. A fit on the purple curve provides the asymptotic value. This value needs to be compared to the specs listed in Table 5.8 selecting the proper value for layer the prototype is supposed to populate.

- Consistency of the estimated TFM production performance: It is difficult to qualify a design against such a specification. It requires a large number of samples produced with the final assembly procedure. For the preliminary qualification process only, the statistical distribution of the production performance on the TFM is verified over three samples.

- Robustness Test The robustness test applies to the effect of the pressure and thermal cycling on the TFM. Once the nominal TFM has been measured, the sample undergo 100 pressure cycles (from 0 to MDP=130 bar) and 100 thermal cycles covering the whole OTR (Operational Thermal Range from -55 to +60C°). TFM is measured again and it should not show any appreciable degradation.

- Mechanic Performance Test The preliminary qualification of the mechanic performance is estimated via FEA (Finite Elements Analysis). However, the FEA needs to be validated by experimental tests on prototypes. The specifications to apply are listed ATU-SYS-ES-0029. These specifications define the maximum gravity sag (or minimum resonance frequency) of the local support design. The stability requirement is set over a period of one day by means of displacement caused by a defined load case that takes into account the expected maximum variation of the environmental loads like power and evaporation temperature.

Final Qualification

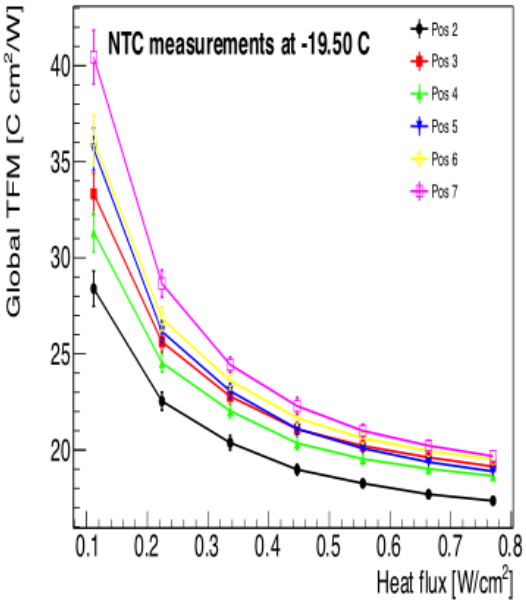

Figure 5.17. TFM as a function of the hear flux.

The full qualification of the local support will take place only after the fayout is chosen. The qualification process will therefore only apply to the relevant designs. The details of the qualification are still under development mainly for what concerns the population of the sample to test for qualifying the design against the specifications. A short description of the main aspects of the qualification is given below:

- Radiation Effects: The radiation dose is assumed flat in η and equal to 1.54×10^7 Gray. It is the value of the radiation dose expected in Layer 0 with a safety factor two applied. The TFM will be measured on irradiated samples in order to exclude degradation of the thermal compounds. Radiation could degrade the thermal coupling at the interfaces.

- TFM Production Performance: It is essential to verify the variation of the TFM measured on a preproduction samples at different module locations and from different assembly sites. The qualification will be carried out once the final design is selected on a significant number of assemblies in order to verify the production performance estimate which is equal to 1.5 the design value.

- Aging effects: Aging tests wil be performed through temperature, humidity and pressure cycles. The amplitudes of these cycles are defined in [3]REference, Citation???[MS]. A number of pre-production samples will be cycled over the OTR (Operational Temperature Range), the MDP (Max Design Pressure) and Humidity variation 100 times. The design number of cycles is defined to be less than ten per year over the detector lifetime of ten years.

- Mechanical and Stability performance The local support design must be qualified against the gravity sag (or minimum resonance frequency) on a final prototype. The stability performance within a one day and a one month period must also be verified on a final prototype. The verification of the overlap in Φ between local supports is of great importance. However this measurement can only be done once the detector is taking data. Therefore the qualification is performed simulating the displacement of the modules in a layer using as input the measured displacement of the local support under the thermal, pressure and humidity cycle.

5.3.4 Design of the local supports

Several different design options of the barrel local supports are under development. For the endcaps, a single design is under study. The design is optimized to reduce the material budget in each layer. This is achieved by using low density and low Z materials high thermal performance. The required stiffness is achieved with the use of ultra-high modules fibers.

Barrel candidates for the Extented layout

In the extended layout all the sensors are positioned on cylindrical surfaces and are parallel the beam axis. Two designs are under development: I-Beam and Carbon Stave.

I-Beam

This design achieves the low-mass requisite by coupling two layers in a single discrete structure with an I-Beam-like cross section. Modules are placed on both flanges of the I-Beam, see Figure 5.18.

The heat generated by the modules is collected by the flange whose core is low-mass thermal conductive carbon foam. The heat reaches a titanium pipe having a wall thickness of about 120 μm directly bonded to the carbon foam. There the boiling CO_2 removes the heat at low temperature. The laminates of the entire structure are bonded together by means of a process called cocuring. This process does not require extra adhesive to bond the parts together. It is the matrix of the plies itself that provides it. The uncured layups are wrapped in a mold and they are cured in one pass. The resin of the prepreg provides the adhesive.

The first thermal test conducted on non-optimized design reviled good TFM values almost meeting the specs listed in Table 5.8 for the most demanding innermost layer. Recent estimate of the radiation length shows values around 1.62 % X/X0 for the sum of the two layers leading to 0.8 % X/X0 the radiation length for a single layer.

Carbon Stave

Although the wall thickness of the pipe is slightly larger than 100 μm, the titanium density is significantly higher than for the carbon. The contribution to the radiation length from the titanium pipe is not negligible. As a consequent, the replacement of titanium with other material has recently been considered. Aluminum has been used in past detectors but it is sensitive to the galvanic corrosion and it tends to be the sacrificial anode of the galvanic couple Al-C. Severe events of galvanic corrosion have been experienced on Aluminum pipes in carbon structure that led, in the past, to lose the integrity of several cooling lines. Moreover, a metal pipe in a quasi-zero CTE carbon structure might drive to undesired deformation during cool down or thermal transient. From this point of view, a pipe made of carbon fiber is the best option in terms of mass and CTE matching.

The carbon stave is an attempt to implement the concept. The metal pipe is replaced by a carbon pipe braided dry on a mandrel and passed through an impregnating dye. Several carbon

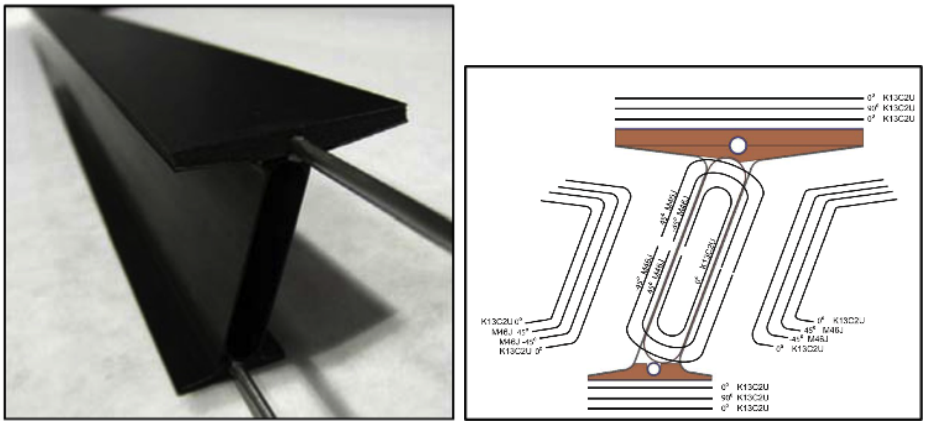

Figure 5.18. TFM as a function of the hear flux.

pipes have been produced already. They have been proven to stand the testing pressure and fulfill the tightness requirement. However, a full carbon stave has not been tested for TFM yet. The thermal performance could be extremely good since the lightness of thecarbon pipe allows to consider several pipes in the same structure without increasing its radiation length.

FEA calculations show surprising good value of TFM with a lot of room to reduce considerably the mass but simulations need to be validated by measurements.

Figure 5.19 shows a photo of a carbon stave prototype.

Barrel candidates for the Inclined layout

The mechanical implementation of the local supports for the inclined layout is more complex. The main advantage of the layout is smaller active area which leads to less services and potentially smaller radiation length. The main problem is the complexity of the design that needs to support inclined modules at different angles. At about $\eta = 1.2$ the barrel module are rotated around the Φ-axis. Assuming the cooling pipe straight, the heat generated in the modules needs to travel longer before reaching the boiling fluid. This implies a larger ΔT along the path and, consequentially, a higher temperature on the module. More mass can be added to increase the thermal coupling but with the unavoidable increase of the weight and radiation length. However, the less active area (with the consequent less services) balances the mass increase by the thermal issue making the inclined layout still competitive with respect to the Extended layout. Two mechanical options are under study: SLIM and ALPINE.

SLIM

This design groups four rows of modules supported on a longeron-like structure. Within $|\eta| < 1.2$ quad chips modules are arranged flat. For $\eta > 1.2$ modules are two chips size and inclined around Φ forming an angle between the sensor plane and the z-axis. Four titanium pipes run along the longeron corners each one cooling one row of modules (see Fig. 5.20).

A recent development foresees the replacement of the longeron laminate with a filament winding truss structure significantly lighter but with an equivalent stiffness. Prototype of SLIM have been deployed and thermal testing are ongoing in order to measure the TFM.

ALPINE

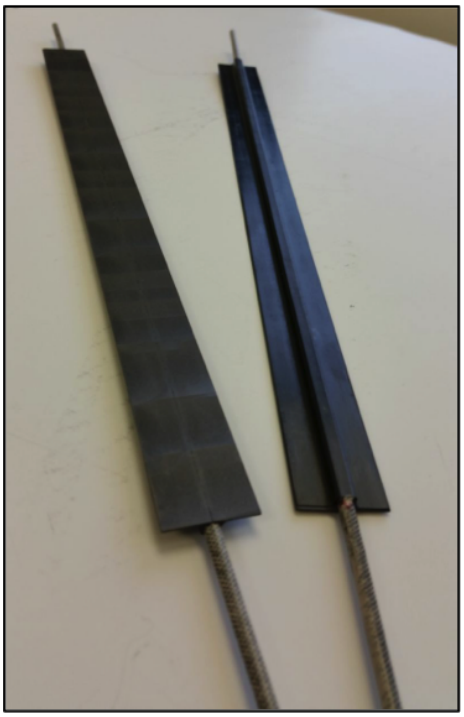

Figure 5.19. Carbon Stave prototype. The carbon pipe (in front) has been impregnated with a diamond-loaded resin in order to increase significantly the through-thickness thermal coefficient that, for the laminate, it is dominated by the resin.

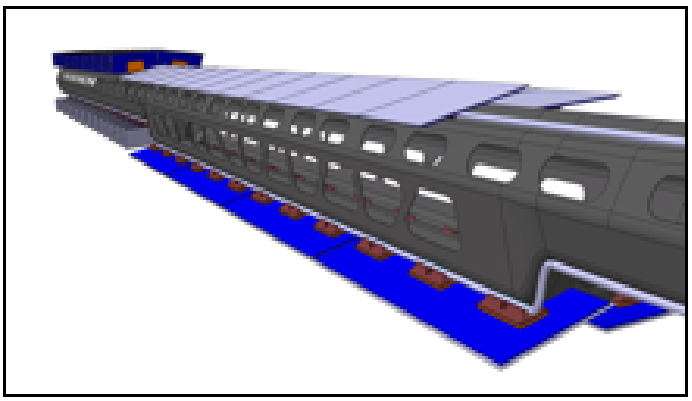

Figure 5.20. SLIM design for the inclined layout.

Alpine uses the same concept with a different design. Modules on different layers are not grouped in the same structure as for SLIM and each module has its own support. Since the stiffness is not enough to meet the sag requirement, local supports of different layers are linked together by means of radial trusses.

Local support design for the endcap

The endcap local support are developed through a novel approach. Usually the forward region

is covered by disk-like structures on which the sensors are arranged in petals. This solution is somehow rigid to any layout change. In case the radius or the z position of a disk needs to be modified, the petal geometry as well as the module size are impacted. In fact, both inner and outer radial coverage can only be matched discreetly by adding or removing one or more active elements.

This sets undesired constraints to the layout definition that benefits from flexibility in its attempt to maximize the physics performance. Ring is an elegant solution to this problem. Instead of a disk stack arranged along Z, modules are placed over a narrow round stave. Four shelvesâĂİ support the modules providing coverage up to $\eta = 4$. Each Ring in a shell can be placed independently from the sensors Z position loaded in the other shelves.

Figure 5.21 show the ring concept. Rings in different shelves line up to provide a tight disk like coverage.

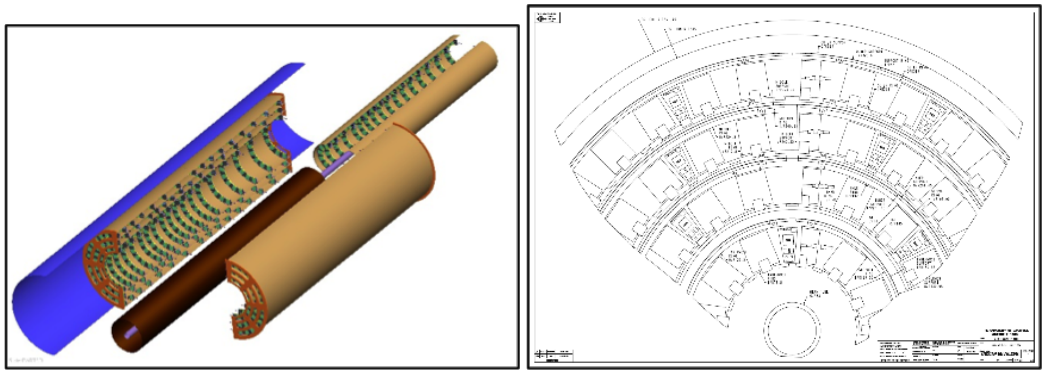

Figure 5.21. Left: Ring concept. The composite shelves inside which the Half Rings carrying the modules are shown in light brown. Right: shelvez lining up to provide coverage.

The Half-Ring is a sandwich of carbon laminates where the core is carbon foam. In its neutral plane a titanium cooling pipe and the service bus tape are placed. The heat generated by the modules is taken away by the CO_2 boiling system. The bus tape distributes the electrical services to the modules and are alternatively bonded to the two carbon faceplates allowing the adequate sensor overlap.

Figure 5.22 shows an exploded view of the assembly which is symmetric in its cross section to manage the CTE mismatch between different materials. Several prototypes have been already built but design optimization is still ongoing. Particular attention is placed to reduce the mass of the Rings system in order to minimize the particle background reaching the forward calorimeter at high η. To address this issue, it is been foreseen to implement in the assembly procedure the so called co-curing. Similar to what was successfully tested on the I-Beam, the sandwich skins are bonded to the foam without adding extra adhesive.

5.3.5 Electrical services

The cooling services will be described in section 5.7. Electrical services can be grouped under five categories: DATA to bring the data from the modules to the couting room, CLK/CMD to bring the clock and the data to configure and monitor the front-end chips, LV to power the modules, HV to bias the sensors and DCS for detector control system.

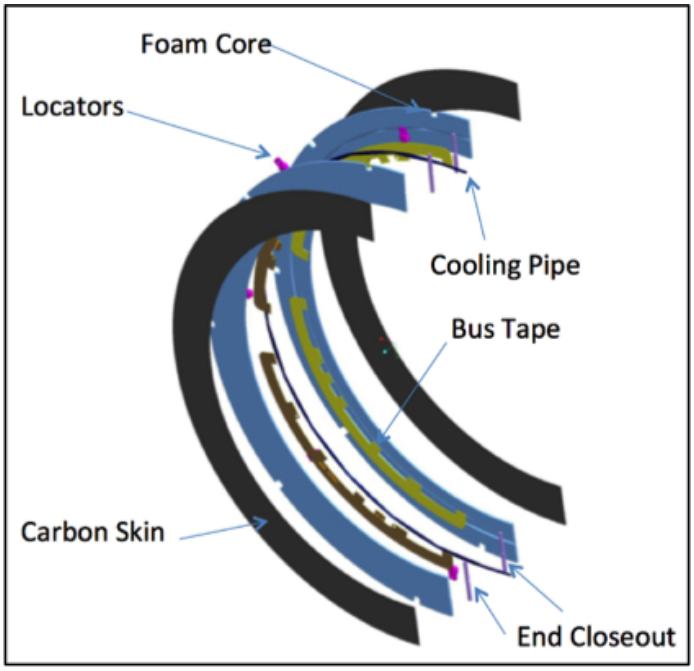

Figure 5.22. Left: Ring concept. The composite shelves inside which the Half Rings carrying the modules are shown in light brown. Right: shelvez lining up to provide coverage.

Services MODULARITIES											
Barrel	FE's per Module	Data Modularity		CMD&CLK Modularity		HV Modularity		DCS Modularity		LV Modularity	
		# Links per FE	# Links per Module	# Links per FE	# Links per Module	# Links per FE	# Links per Module	# Links per FE	# Links per Module	# Links per FE	# Links per Module
L0	2	1/1	2	1/2	1	-	1/10	1/20	1/10	1/20	1/10
L1	4	1/2	2	1/4	1	-	1/5	1/20	1/5	1/20	1/5
L2	4	1/2	2	1/4	1	-	1/6	1/24	1/6	1/24	1/6
L3	4	1/4	1	1/4	1	-	1/6	1/24	1/6	1/24	1/6
L4	4	1/4	1	1/4	1	-	1/6	1/24	1/6	1/24	1/6

Table 5.10. Summary of services modularity of the Pixel detector.

Table 5.10 shows the current understanding of the modularity of the services. Each type of services is detailled in the following.

Data

Data links connect the module to the OptoBoard that converts the electrical signal into an optical signal. OptoBoards will be located outside the detector volume and will be easily accessible. However, this feature that mitigates the risk of losing a large part of the detector in case of systematic failures on the opto-boards, implies long data links, up to 7.5m or possibly longer.

The data rate vary with the layer. This is partially taken into account with the modularity. The data links for the innermost layers are still the most demanding in terms of rate specification. Developments are under way to extend the link length while keeping the cable mass as low as possible. The optimization might require to located the optoboards inside the detector volume which would mean they would not be accessible. The most promising solution under study is

based on a micro-coaxial cable terminated with a short section of a twisted pair conductors to reduce even more the cable mass in the proximity of the modules.

Clock and Command

Clock and command lines provide the configuration and timing to the front-end chips. The required data rate is significantly lower than the data links. However, the total number of links is non-negligible and considerably contribute to the overall mass of services.

Low Voltage

Serial powering was adopted to power the front-end chip, mainly due to the large number of modules. Several modules (therefore several FE chips) are ganged in series and powered with a single line.

Hig Voltage

High Voltage services provide the bias voltage for the silicon sensor. The maximum depletion voltage dependson the sensor type (3D or Planar) and by the integrated end of life fluence. The maximum high voltage is 1200 V that corresponds to the depletion voltage required by the ;llanar sensors loaded on the innermost Layer. The distribution among sensors is done in parallel and the modularity ranges from 10 to 5.

Detector Control System

The goal of the DCS system is to monitor the module functionality and to provide automatic actions in case of risk to the detector integrity. DCS links carry the temperature information of the modules previously digitalized. In case one front end chip fails, the DCS needs to automatically bypass the affected module. The continuity of the low voltage serial line can be reestablished and the other modules on the same chain can remain powered. This is one of the most important function of the DCS system that needs to be designed to be fail-safe by means of a double failure mode. In other words, any two failures occurring in any component of the DCS system should not be sufficient to allow major damages in the detector.

5.4 Powering

The ITk pixel detector will have around 10,000 detector modules (depending on the final layout decision), which hold either two or four FE-chips. These modules need to be powered with low and high voltage. Furthermore, the finer granularity of the pixel detector sensors and its connected FE-chips together with smaller feature size technology of the electronics (65nm instead of 130 resp. 250 nm) lead to an increased current consumption inside the front-end electronics. Therefore, supplying each of the modules separately with parallel powering with a high power loss within the cables is not feasible and would introduce a tremendous amount of material with the cables to be installed. In order to save material and reduce the voltage drop on the supply services alternative power concepts are under study. Out of the two possible solutions (DC-DC conversion and serial powering) the chosen baseline for the ITk pixel detector is serial powering.

The concept of this powering scheme is to power the modules via a constant current and the current to voltage conversion is done on module or chip using shunt regulators. This way, the current being transported via the supply line is just the current for one module, while the voltage is the sum of the voltages needed by all modules: For a serial powering chain with n modules, the current is $I_{chain} = I_{mod}$ and $V_{chain} = n \cdot V_{mod}$.

The serial powering scheme foreseen for the ITk pixel detector builds the chain from the individual modules being mounted on the same support structure. This leads to different ground levels at each of the modules, which needs to be reflected by adding DCS-chips, supplying the high voltage to the modules and using AC coupled data transmission. The voltages for the individual FE-chips of the modules is distributed parallel and each FE-chip has its own shunt regulators to generate the needed voltages.

The foreseen regulator, a shunt-LDO regulator, is based on the experience gained with the FE-I4 ASIC, which has been installed in the IBL and provided a shunt-LDO already. The voltage regulation loop (LDO) delivers a constant voltage defined by an internal generated reference voltage (i.e. $V_{out} = 2V_{ref}$) and the current regulation loop keeps the current through the regulator constant, while the input characteristic is ohmic, see Fig. 5.23.

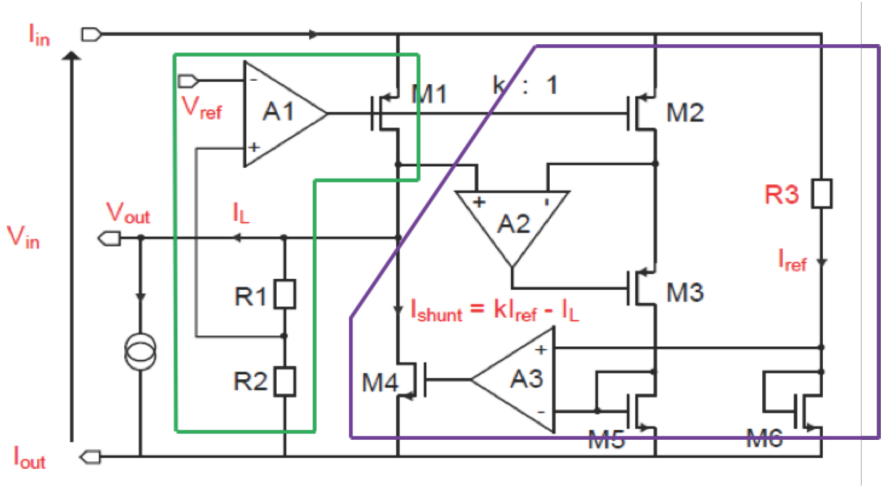

Figure 5.23. Schematic of a shunt LDO regulator. The input characteristic is ohmic: $R_{in} \approx \frac{V_{in}}{I_{in}} \approx \frac{R_3}{k}$

The main features of this regulator are:

- robust design against process variation and mismatch for safe parallel operation (i.e. sharing I_{in} and I_{out} connection, but not V_{out}!).
- Parallel operation of regulators with different output voltages possible.
- Ability to shunt extra current in case one of the regulators in parallel fails.
- Different working modes for current and voltage based power distribution.
- Shunt current for stable operation can be just 10 mA.

First prototypes of serial powering chains have been setup and the module performance is very promising and not disturbed by the different powering approach. Nevertheless, more studies are needed and several topics need to be addressed such as: module bypass in case of failures (incl. switching individual module on and off), keeping the power consumption as constant as possible and always well under the limit of the provided current, HV powering scheme (HV level depending

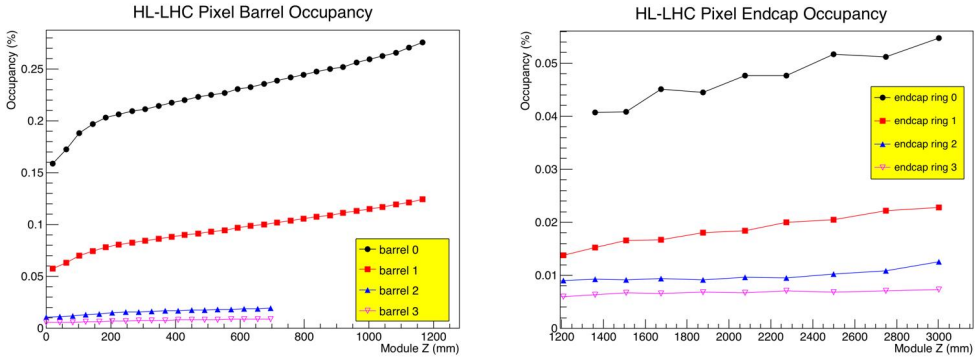

Figure 5.24. Hit occupancies in barrel and end-cap layers from a $t\bar{t}$ simulation.

on the sensor type), AC-coupled data transmission as each module has a different ground potential, constant current power supply.

5.5 Data Acquisition and Transmission

A full GEANT4-based simulation of $t\bar{t}$ events with $<\mu>=200$ was used to derive hit and cluster rates. The Pixel layout was based on an older Unity layout with four extended barrel layers and full end-cap disks. Pixel hits are derived from particle hits using the IBL digitisation modified to be compatible with the FE pixel size of 50 μm $\times$50 μm.

The resulting occupancy is shown in figure 5.24 for the four barrel and the five end-cap layers. In the barrel region, the ratio of pixel hits per particle hits rises towards the higher η region due to tracks traversing many pixels. In the end-caps, the ratio of pixel hits per particle hits is similar over all layers.

5.5.1 Bandwidth estimations

Bandwidth needs for the data transmission are driven by the trigger requirement to allow an L0 accept rate of 1 MHz with a latency of 6 μs. The pixel detector will be readout fully at L0 independently on the ROI and L1. Based on the occupancy of the simulations described above and assuming a raw hit data word size of 26 bits, the needed data rates per FE link was estimated. This used the mean occupancy over a stave and an encoding and compression overall factor 0.65 for the barrel while this is assumed to be less effective for the end-caps, thus an effective compression of one was assumed there.

Table 5.11 shows the parameters of the transmission path for the pixel modules in the barrel and end-cap layers. The bandwidth per module exceeds even for the outermost layer the input data rate of the envisaged LpGBTx chipset of 640 Mb/s. Therefore the format to be defined for the FE chip will be also used for transmission on the electrical links described below.

5.5.2 Read-out simulation studies

Based on the simulations described above, the performance of the read-out chain was simulated focussing on the innermost barrel layer which is most critical in terms of data and hit rates. In a first approach, the fraction of fully processed L0 accepts is determined over 10^6 simulated triggers,

Table 5.11. The main bandwidth parameters of the pixel readout with a 1 MHz L0 rate at a latency of 6 μs.

Detector	Number of modules per stave/ring	Module type	Rate/FE [Mb/s]
barrel 0	60	dual	4937
barrel 1	120	dual	2586
barrel 2	36	quad	1450
barrel 3	36	quad	876
barrel 4	36	quad	577
endcap 0	96	quad	3333
endcap 1	144	quad	2541
endcap 2	192	quad	1466
endcap 3	240	quad	911

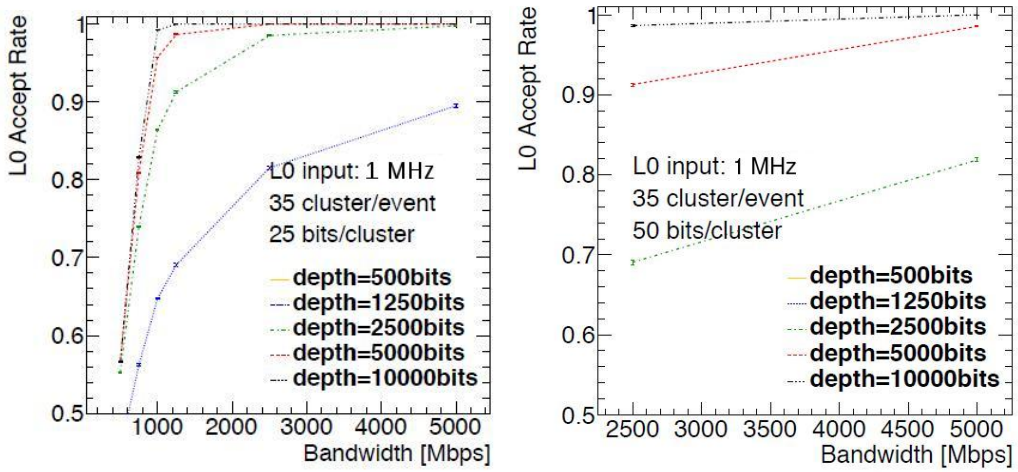

Figure 5.25. Fraction of accepted L0 requests in a simulation of the FE read-out for different data rates and FE buffer depth for the central region (left) and the end region (right) of the innermost barrel layer.

with the number of clusters per event Poisson-distributed around a mean of 35 corresponding to the number of particle hits, assumed to be identical with clusters, as obtained from the $t\bar{t}$ simulation. For a simple compression model, 25 bits per cluster is assumed for the central part of the barrel layer, while for the high-η-region a less stringent compression is assumed with 50 bits per cluster. The data is subsequently simulated to be stored in the FE buffers of variable depth. The queue is emptied with a variable data rate corresponding to the numbers discussed above. If this queue is full upon arrival of a new trigger, the corresponding L0 accept is considered as not processed.

The result is shown in Fig. 5.25. The two investigated regions in the barrel require the expected data rate of 5 Gbit/s per FE and a FE buffer depth of 10000 bits to achieve a processing of 99% L0 requests while introducing an additional latency of 1 μs or less. The assumed bit-size per cluster means that in the central barrel region, clusters can be read out but require higly optimised

compression while in the forward region clusters can be read out with more moderate compression. For more detailed simulations, a more complex implementation of data format and compression needs to be achieved.

5.5.3 Link architecture

Due to the very high radiation levels expected in the innermost detector volume, placing the opto-elements at the end of staves or rings is not feasible. Therefore, the data transmission link will be split into an optical part, running from the counting caverns down to the ID-end-plate region (final location still to be defined) and an electrical part, connecting the opto-components to the front-end electronics on the rings or staves.

The off-detector components don't need to be radiation hard and therefore can be off-the-shelf commercial components. Optical plugins and FPGA based signal processing logic will be place here. The optical signal will run via optical fibres, which need to be as radiation hard to withstand the irradiation along the routing path up to the opto-converter boards including a reasonable safety margin to guarantee an appropriate power budget for the optical link. The electrical part needs to serve the data transmission between optical converters and front-end electronics at the needed bandwidth, which depends on the location inside the detector, and must not introduce too much material into the detector not to disturb the particle flight towards the outer subdetectors. As the innermost layers will run at the highest bandwidth, this is the driving factor for the development. Very thin cables serving a bandwidth of around 5 Gbit/s are under development and study.

Electrical cable solutions

The electrical data transmission system for the pixel detector runs from the front-end readout chip to the optical transceiver box outside the ITk volume, approximately seven metres away. The point-to-point data links must operate at speeds up to 5 Gbit/s for the inner barrel layers and 2.5 Gbit/s for the outer barrel layers and endcaps. All of the components, both active and passive, must be radiation tolerant to 2×10^{16} 1-MeV neutron/cm^2 over the lifetime of the HL-LHC. Significant effort has been invested in finding data transmission solutions that satisfy these specifications with the least amount of material in the active detector region.

Long flexible 100 Ω twinaxial cables have been designed and tested for speeds up to 6 Gbit/s over distances of 7 m. This transmission rate is achievable with suitable signal conditioning (pre-emphasis, equalization, signal encoding). Bit-error rate measurements with pseudo-random bit patterns confirmed low error rates and minimal cross talk between shielded differential pairs.

Twisted-wire pairs of extremely fine gauge (AWG36 and below) have been designed, also with a characteristic impedance of 100 Ω. This design features less material than the twin-ax solution tested over longer distances. These cables successfully transmitted data over 1 m at rates up to 6 Gbit/s with no errors, but the error rate increased dramatically for transmission over longer distances. A hybrid solution composed of 1-m twisted pair plus 6-m twinax cable is attractive because of the minimal material in the central region and a robust transmission rate over long distances.

Kapton flexible printed circuit cables are also natural candidates for a radiation-hard, low-mass electrical transmission solution. These flex circuits have been irradiated to the expected neutron-equivalent fluence with no degradation in electrical 1properties. At least two solutions for data transmission inside the pixel volume using Kapton flex technology with a differential embedded microstrip arrangement and cross hatched ground plane have been developed. The Kapton flex

option can easily incorporate low voltage for serial powering, high voltage for low current detector bias, controlled impedance differential pairs for a shared chip command and clock signal, and connections for module temperature sensing in addition to the differential data transmission. For each module, the frontend chips share a clock and a control line, but each frontend has a dedicated data line. Both flex designs have demonstrated transmission over 1 m with rates above 5 Gbit/s using signal pre-emphasis and equalization in addition to 8b10b encoding. The required rate can be achieved without significant cross talk between adjacent data lines on the flex.

The data transmission lines for the pixel detector endcaps operate at up to 2.5 GBit/s. The current design uses small twin-ax cables or twisted pairs, with matched impedances. These cables, which may be the same as those used in the barrel layers, have special conductor and dielectric materials to reduce conductive losses and skin effect losses. Earlier designs used flex cables in a stripline or microstrip arrangement, with guard traces between signal lines to reduce interference. The choice of wire cable over flex circuits allows for more flexibility in the layout and for reduced material in the transmission line.

All of the data transmission options for the pixel detector depend on robust, low-mass connector options for mating at the frontend chip and optical transceiver (and possibly at the end of the pixel stave). Suitable connectors exist in miniature form and are being characterized in the different design options.

Optical components

The optical link between off-detector components and on-detector opto-converters should be array-based. This will save space needed for the connectors and driver/receiver circuitry and saves multiplicity in terms of connector front-end electronics. Two approaches are followed currently, one is based on the experience made for the run 1 pixel detector and one is based on the Versatile Link+ project developments. In general 12-channel optical transmitters and receivers will be used. The basic requirements are:

- The transmitter is optimized to operate at 5 Gbit/s per channel,
- electrical signal equalization to properly receive the signals from the electrical cables are to be added if needed,
- the transmitter and receiver connect to a 12-way fibre ribbon each,
- the receiver is optimized to operate at 2.5 Gbit/s (5 Gbit/s),
- transmitter and receiver operate within the environment of the ATLAS detector.

In the following the two concepts will be described.

Opto-board based development

Based on the experience from the run 1 and 2 pixel detector, studies for the design of optical links based on the opto-board concept, which has been successfully deployed in the two generations of optical links for the pixel detector of ATLAS, are ongoing. There will be two flavors of opto-boards, one for transmitting and the other for receiving optical signals. Each transmitter opto-board contains an ASIC with 12 channels of VCSEL (Vertical-Cavity Surface-Emitting Laser) drivers for coupling to a 12-channel VCSEL array. The ASIC will be operating at 5 Gbit/s. Each opto-board

receives the electrical signals via thin cables from the pixel modules about seven metres away. Each receiver opto-board contains up to 12 channels of receivers to amplify the signals from a PIN array. Each receiver will be operating at either 2.5 Gbit/s (if using 65 nm CMOS technology) or 5 Gbit/s (if using 130 nm CMOS technology). The received signals would then be sent to a GBTx(Gigabit Transceiver) array for de-serialization into multiple 160 Mbit/s signals for transmission via thin twisted pair cables to the pixel modules about 7 m away.

The transmitter ASIC, the VCSEL driver, has been successfully prototyped in a 4-channel version using a 65 nm CMOS technology. The corresponding transmitter opto-board has also been prototyped. The optical package for the VCSEL array is very similar to that used in the second generation opto-boards and the RXs modules (the off-detector optical receiver modules) produced for phase-0 upgrade. The optical coupling uses the commercial MTP connector which can be readily mounted and dismounted during production testing and installation. The performance at 5 Gbit/s is satisfactory [**?**]. The plan is to lay out the ASIC in 12 channels in the near future. For the receiver ASIC, the plan is to take the single channel GBTIA circuitry (IP) and lay it out in array format. Also needed is the de-serializer in the GBTxor lpGBTxwhich should also be layout in an array format.

Groups of opto-boards will be mounted inside an opto-box, a mini-crate similar to that used in the second generation optical links of the pixel detector. Due to space constraints, the opto-boxes for only two inner barrel layers and possibly the inner most end-cap rings will be located inside the ID end-plate. The remaining opto-boxes will be mounted near the LAr electronics (need a more precise description). The arrangement is similar to that of the current pixel detector. The use of array-based receiver opto-boards reduces the physical size of each opto-box by a factor of two, a much needed space saving. Overall, there are 20K data links and 10K TTC links (or 3K TTC links with the use of GBTxarray proposed above).

Versatile Link Array Driver (VLAD) development

The transmitter module proposed by the Versatile Link+ project is a prototype candidate. This optical transmitter will have the following additional features:

- The transmitter is low profile, low power and operates without a heat-sink.
- The transmitter provides channel redundancy built in and is controlled through an I2C interface.

The module consists of a VCSEL array and a connected VCSEL array driver. This array driver ASIC (VLAD or lpVLAD[1]) has been designed and prototyped in the TSMC 65 nm CMOS technology with less channels. It operates with a data rate of 10 Gbit/s per channel. The fibre connection will be done via MOI and LTP connectors. Together with the Versatile Link ATx module, this new driver can be used for test purposes in a readout system to study its behavior in a close to real detector system. With this the performance of optical transmission, power consumption, heat load and others will be tested in system testbeds once being available. A 12-channel version with built-in redundancy and an euqalizer circuit in the receiver part is foreseen for the coming year based on the testing experience using the prototype ASIC.

[1] VLAD: Versatile Link Array Drive, lpVLAD is the low power version.

5.5.4 General readout

Read-out related activities in the next years will address the compatibility of the concept of an ATLAS-wide general readout system FELIX and in addition provide test benches for module and system development needs. Apart from more stringend requirements concerning data rates, the concepts for off-detector readout of pixels are very close to that of strips and are discussed in a common chapter.

TBD: interface to L1track (might be covered by strips, also depends on trigger design desicion)

5.6 Detector Control System and Interlocks

To ensure safety, reliable control and information for debugging the ITk pixel detector control system (DCS) foresees three independent paths. These paths differ in granularity, availability, and reliability. Each has its own signal paths.

The safety path is built by a hardwired interlock system, which acts directly on power supplies or other equipment, if the safe operation of the detector cannot be guaranteed any more. This system must have the highest reliability, however, due to the required low material budget, the lowest granularity. It is always in operation. This system is built in common for both sub-detectors of the ITk and is described in more detail in Chapter 13. (I was asked by Pepe from the strips to write about the interlock system)

The control and feedback path is the interface between operator and detector and covers use cases like calibration, commissioning, and data taking. It steers all components of the detector and provides monitoring information as feedback. It is made up by the DCS network, consisting of DCS chip and DCS controller, as seen below. This path is mandatory for the detector operation and therefore requires a high reliability as well. To ensure a reliable control of individual modules its granularity must be on the module level. The main component of the control path is the DCS chip which provides the monitoring and control capabilities on module level. The graphic below shows how the DCS chip is integrated within the serial power chain. From the DCS computer the commands are sent to the DCS controller over a long term protocol. The CAN protocol is currently envisioned to be used.

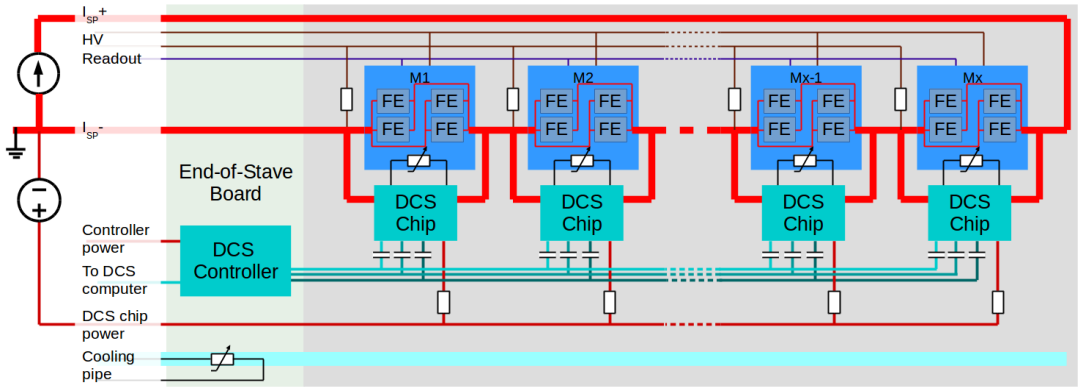

Figure 5.26. This is coming.

The DCS chip is specially designed to work in a serial power chain. It is placed on the module flex of each pixel module. It includes bypass capability for the modules, realized by a shunt transistor. The bypass can be activated or deactivated by command. Furthermore a hardwired automatic activation of the bypass transistor in case of overvoltage or over-temperature is included. The thresholds for the automatic activation are defined with external components on the flex print. This bypass is off after power-up or in case of power-loss. For feedback the DCS chip includes an ADC, which allows for monitoring of the moduleâĂŹs temperature and voltage. As the DCS chip is mounted in close vicinity to the detector modules, even in the innermost layer, it needs to fulfill the same radiation hardness as the front-end chips of the innermost pixel layer. The DCS chips are powered independently from the front end chips. The DCS chips of one serial Isp chain share the same power line (see Fig. 5.26). The power return of the DCS chips is merged with the serial supply current Isp. The DCS power line is also used as an external reference for detecting drifts of the internal reference.

There are three independent communication lines to the DCS chips of one Isp chain. The DCS chips are AC coupled to the communication lines. Currently there are up to eight modules in one Isp chain foreseen. The maximal length of the communication lines between DCS chip and DCS controller is foreseen to be 1.5m. The DCS controller realizes the communication between the DCS computer and the DCS chip. It serves as a bridge between a long range communication from the computer to the short range communication used by the DCS chip. The location is not yet fixed, but will either be on the End of Stave board, or a patch panel.

The diagnostics path provides the operator with additional monitoring values in order to debug the behavior of the detector or tune its performance. It delivers information per front end chip and so provides the most detailed information. As it is embedded into the data stream no additional lines are required.

5.7 Cooling

The development of the cooling plant and the distribution lines for the entire tracker is managed at the ITk Common Mechanics level. In the following the cooling specifications and its internal modularity are presented. The specifications for the cooling power depends on the detector layout. Hereafter estimates are given for the most demanding layout option under study that foresees five barrel layers and four EndCap Rings Layers covering up to a pseudorapidity of $\eta = 4$. This is the maximum in terms of power and number of evaporators. This layout would lead to the number of evaporators listed in Table 5.12. The evaporator is the section of the cooling pipe in which the C02 boils after passing through a restriction that produces a pressure drop required to trigger the boiling.

Due to the large number of local supports, each evaporator cannot have a dedicated cooling line up to PP1. The penetrations and the fittings would be prohibitive. The new detector must have a distribution system in its volume in order to reduce the number of fittings at PP1. This is different compared to the present Pixel detector. Evaporators can be ganged in series or in parallel. Both the options have benefits and drawbacks. These issues will addressed and shown for the inner layers. This part of the detector is the closest to the beam pipe and consists of two barrel layers and one layer of EndCap per side.

Layer	Local Supports per layer	Evaporator (one per layer)	Evaporators Total	Total In Pixel
L0	16	16	16	
L1	16	16	16	
L2	42	42	42	
L3	42	42	42	
L4	54	54	54	
			170	
Rings	Rings along Z	Evaporator/EndCap (one per half ring)	Evaporators both endcaps	
R0	17	34	68	
R1	19	38	76	
R2	16	32	64	
R3	16	32	64	
TOTAL		136	272	442

Table 5.12. Specifications for the Thermal Figures of Merit.

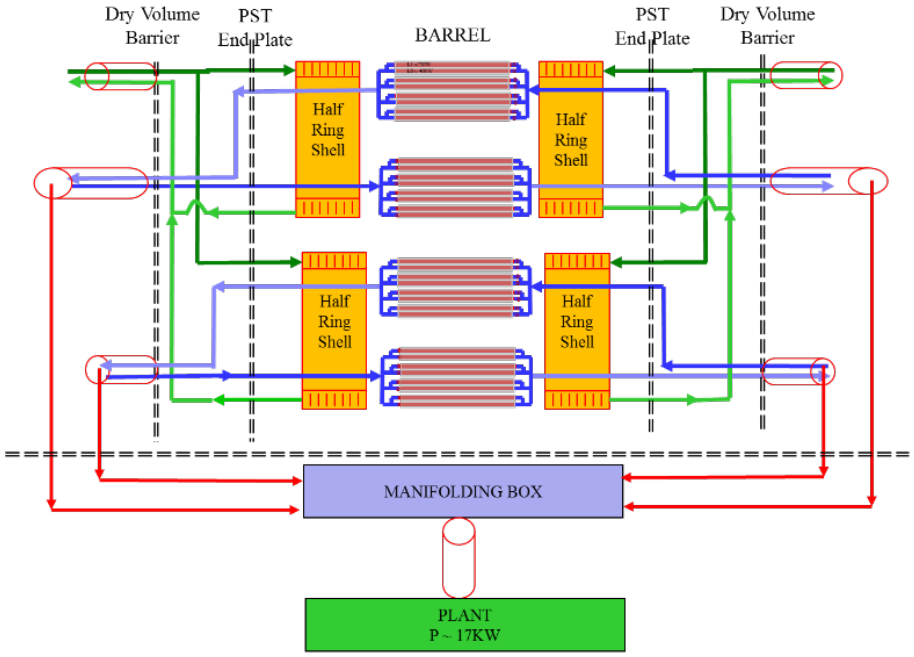

Figure 5.27. Schematic of the cooling distribution in the innermost layers.

The two innermost barrel layers are shown at the center of Figure 5.27. The cylindrical layers (see Fig. 5.28 for appreciating the geometry) are unfolded flat to better show the schematic of the distribution. Modules are arranged over 16 local supports serving both L0 and L1. Each local sup-

port houses two boiling channels in the same mechanic structure. In the picture the evaporators are indicated in red and it is where the heat dissipated by the modules is picked up by the evaporation latent heat of the CO_2.

A group of four local supports, carrying in total 8 evaporators, is supplied from a single liquid line running parallel to the beam line from PP1. At PP0 (about Z=1400 mm) the flow is split over four lines by means of a manifold serving each local support. Right after the flow is split further in two in order to feed each of the two evaporators. The evaporation process is initiated by a restriction in front of the evaporator.

At the end of the boiling channel the bi-phase flow is collected in a single exhaust pipe indicated in Figure 5.27 in light blue. This configuration requires the exhaust to be at the opposite side of the inlet. Since an exchange of heat is required between inlet and outlet lines for the cooling system to operate properly, the other group of four local supports has the feeding line flipped to the opposite side in order to arrange the inlet of the first group with the outlet of the second in a single coaxial transfer line. The third and the fourth groups of local supports are organized in the same way so that the whole barrel section of the Innermost Layers needs only four coaxial lines at PP1 arranged in a counter flow configuration.

Figure 5.28. Draft 3D model of the manifolds next to the Local Support structure.

The Rings EndCaps are two assemblies being part of the Innermost Layers (see orange blocks in Figure 5.27). Each one is made of two half shells containing 17 HalfRings. The HalfRing is cooled by a single evaporator connected in a common rail fashion to single supply line. One EndCap will therefore have two inlets and two outlets as indicated in green in the picture. However, to reduce the number of fittings at PP1 on both sides (motivation is provided in the Functional Requirement Register ATU-SYS-ES-0028) the HalfRing assembly lines are ganged in parallel after the penetration at PP1. At the end, outside the dry area barrier at PP1, one InnerMost EndCap would require a single transfer coaxial pipe.

In conclusion the InnerMost Pixel sub-assembly, that provides two barrel hits (L0 and L1) and 17 EndCap hits is cooled by only six coaxial transfer lines. On the way out those lines reach the Manifold Box (see again Figure 5.27) that will connect them all together in a single stationary coaxial vacuum insulated pipe that ends to a cooling plant unit about 100m away in the ATLAS cooling room.

Table 5.13 lists out the relevant parameters of the entire cooling distribution lines for the Pixel detector. The first column designates the layer (barrel or ring). The next two columns provide the cooling power of the loops required to cool the layer assuming the number of loops per layer indicated in the fourth column. There are two values. One gives the cooling power generated from the FE chips only while the second includes the power dissipated by the sensor at its thermal run-away. It is unrealistic to assume that all the modules in the detector reach the run-away at the same time but it is also incorrect neglecting the power from the sensors. The final cooling budget will be in between the values at the bottom of these two columns. A final budget will be issued after the layout option is chosen.

Layer	Loop Power at PP1 [W]		Number of Loops per Layer	At the Dry Barrier at PP1						Plants [W]	
				# of Feeding lines		# Exhaust Lines		# of Vacuum Insulated Fittings			
	No Senor Power	With Sensor Power= 0.25 W/cm^2		Side C	Side A	Side C	Side A	Side C	Side A	Side C	Side A
L0+L1	3447	4596	4	2	2	2	2	2	2	18386	
L2+L3	2620	3493	10	5	5	5	5				
L4	3103	4137	6	3	3	3	3	8	8	29877	29877
Ring0	4113	5484	2	1	1	1	1				
Ring1	3448	4597	4	2	2	2	2	4	4	19840	19840
Ring2	3871	5161	4	~~2~~	~~2~~	~~2~~	~~2~~				
Ring3	2419	3226	8	4	4	4	4	5	5	18065	18065
	TOTAL Modules Power			19	19	19	19	19	19	7	
	Min	Max		38		38		38			
	115462	153949	38	76							

Table 5.13. Summary of the lines and cooling power for the Pixel detector.

Last cell in the fourth column gives the total number of hydraulically independent loops penetrating the EndPlate sealing off the PST (Pixel Support Tube). The criteria followed to define the modularity are three folds:

- Keep the power of a single loop around 5KW or lower and as much as possible even over different loops.
- Inlets and Outlets lay on the same detector side. This is a general rule that is violated for the innermost barrel only. The motivation belongs to the fact that local supports in these layers are much longer than in the other layer and a u-turn configuration obtained putting two evaporators is series would lead to an excessive loop power. This has negative consequences on the pipe size, pressure drop and, finally, to the evaporation temperature that would worsen the thermal performance right where it needs to be optimized.
- The final mapping of the loops to the cooling plants array must be such that the power budget on each plant is similar to the others and lower than 30KW. A specific case is the plant serving the InnerMost barrel where it is beneficial to reduce its size in order to facilitate the decrease of the evaporation temperature.

The 38 loops, counting 38 Inlets and 38 Outlets, penetrate the PST EndPlate. The feedings and exhausts inventory per each side is given from the 7th to the 11th columns. Cell are color coded. Each color corresponds to a single cooling plant. Loops are merged again via the manifold box (see Figure 5.27). The four loops of the innermost barrel are collected to a single plant of about 18KW independently from the penetration side. For all the other layers the grouping is done over different layers.

Assuming coaxial vacuum insulate fittings at PP1, columns 12 and 13 show the fittings number in each detector side. Finally, the last two columns give the cooling power of the plants and their mapping to the loops and layers. Seven are the plants needed of abut 30 KW maximum

with a significant smaller plant for the InnerMost barrel where we aim to reduce the evaporation temperature.

The evaporation temperature which sets the temperature at which the cooling power has to be provided is addressed in the following. The evaporation temperature at the inlet of the evaporator is specified. This is the worst case due to the pressure drop built up along the evaporator. The pressure is set on the exhaust lines by the saturation point at the accumulator in the plant. The pressure drop along the exhaust lines and along the evaporator increases the absolute pressure. The effect is maximized at the inlet of the boiling channel which turns out to also be the point at the highest temperature.

The evaporation temperature must be -35C$^\circ$ or lower for any boiling channel in any local structure of the detector.

5.8 Global Mechanics

5.9 Production

The Pixel Detector production schedule is determined by two parameters: the availability of module components, fixing the start of the pre-production phase, and the date of the beginning of ITk integration at CERN, when all the modules must be ready. Practically, the only missing module component at he moment is the new FE chip.

As explained in Section 5.2.4 the FE chip for the Pixel Detector is being developed in the framework of the collaboration. A first prototype of the chip, called RD53-A will be submitted at the end of 2016. This will be the first RD53 prototype that can be bonded to a sensor and used to produce modules. Even though many important tests will be possible with RD53-A modules, this will not be sufficient to fully qualify the new pixel module design, as the chip will be too small and missing a number of crucial readout features. After a first phase of testing of RD53-A, the RD53 design team will directly proceed to the design of the final chip. It is assumed that the design phase will start mid-2017 and will take 18 months; as a consequence, the ATLAS Pixel readout chip will be submitted by the end of 2019. After initial on-wafer testing, the pre-production of modules using the final components will start in the second half of 2020. The pre-production phase (between 10% and 15% of the modules needed) will last one year, so the production of modules to be used in the ITk will start in the second half of 2021.

The end date of the module production is dictated by the beginning of the ITk detector integration at CERN. Even if the details of the integration procedure are not yet clarified, we know it will start in 2023. It is then conservatively assumed that all the modules, tested, qualified and mounted on the local supports must be available at CERN by the end of 2022. The total time available of module production and loading is 30 months, from Q3 2021 to Q4 2022. The schematic timeline of the Pixel Detector production is shown in Fig. 5.29. The detector integration is assumed to take the entire year 2023, while 2024 is reserved for extensive system test on surface. The installation in the ATLAS cavern is foreseen for mid 2025.

The layout of the Pixel detector is not yet finalized, and several options are being evaluated. In terms of number of modules, estimates are ranging, according to the layout, from 10000 to 12000, for a total active surface between 15 and 18 m^2. Most of the modules are quad, i.e. made of four FE chips arranged in a $2x2$ matrix. There are, however, single FE and $2x1$ modules, depending on

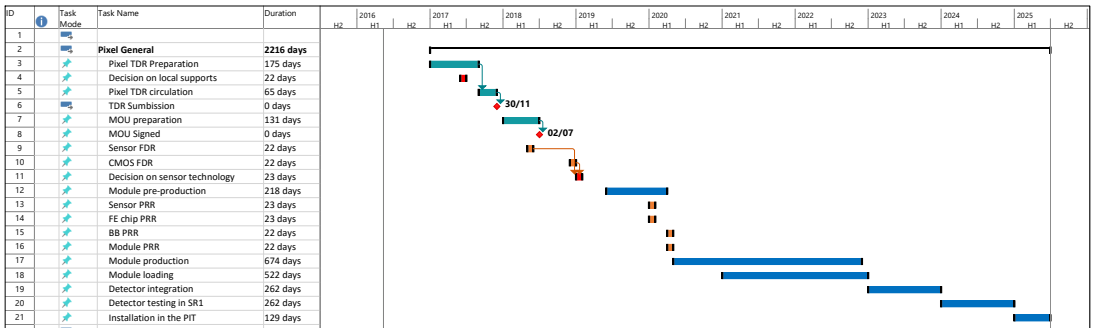

Figure 5.29. Schematic timeline of the Pixel Detector production

the exact layout and on the sensor technology. In order to complete the module production in 30 months, a flat-top production, testing and loading capacity of 24 accepted modules per day must be acheived, up to 30 if we take into account yield and failure recovery procedures. Based on the experience accumulated with the fabrication of the ATLAS Pixel detector, there is a consensus that a similar production rate is acheiveble using seven to eight production clusters operating in parallel, as it is suggested by the aspiration of the laboratories participating to the project. It is clear nonetheless that the module assembly procedure must be hghly optimized. The most time consuming phases during the assembly of an hybrid pixel module are the bump-bonding and the test.

Testing procedures can be significantly improved with respect to past productions, implementing more parallelism in the read-out and increasing the level of automatization of repetitive sequences.

Bump-bonding, on the other hand, may represent a bottleneck for the production: it's a low volume industrial production and for this reason tends to be batched and the maximum capacity available is not continually exploited. Based on prior experience, delays in bump-bonding can occur for many reasons, so excess capacity will be needed to be able to catch up and keep assembly activities properly supplied. Efforts are currently in progress to qualify five or six vendors. Besides the investigation of the technical characteristics of the different processes, a significat effort will be made to verify the maximum production rate each vendor can acheive. The aim would be to select at least three vendors with a peak capacity of 20 modules/day: this would ensure a large margin with respect to the requested average rate, hence a safe handling of fluctuations and possible problems at one vendor. At the same time, the possibility of using automatic flip-chip machines available at different institutes in the Pixel collaboration to alleviate the load on the industrial partners is being explored. Bump-bonding qualification is already on-going, using the previous generation of FE chip (the FE-I4, used in the IBL) coupled to new sensors or dummy test structures. The final step of the qualification will however be possible only at the beginning of the pre-production.

Another aspect that can have a significan input on the schedule is the decision process to select between alternative technologies at the level of sensors or module interconnection. As explained in the previous paragraphs, the Pixel TDR will not contain a complete baseline design for the different module flavours that will be used in the detector: the final decision on some aspects of the

implementation will be posponed until the FDR, i.e. at the beginning of the pre-production. One developement which is proposing a radically new module concept, hence potentially impacting the production schedule in a significan way, is the monolithic CMOS Pixel Module 5.2 proposed for the outer layers of the detector. In this case the simplification in module production and an important reduction of the load on the bump-bonding vendors may have a beneficial effect on he overall production schedule. At the same time, the effect of posponing too much the decision on the technology may generate in the end large delays. It must be clear that the selection of the baseline technology to use in each layer of the detector cannot be posponed after the beginning of the pre-production phase (i.e. the beginning of 2019) to avoid interference with the tendering and procurement procedures. Moreover, each alternative technical solution to be considered between the Pixel TDR and the beginning of 2019 must be compatible with the local support thermal and mechanical specifications listed in the TDR.

Several crucial R&D activities are still in progress, so the understanding of all the details of the production schedule will improve with time, and unfrtunately not all the answers will be available in time fro the Pixel TDR. However, it should be possible to build, in time for the TDR, a solid evidence, based on preiminary prototype work and close cooperation with the bumb-bondinf providers, that the necessary production rate can be achieved.

6. Strips Overview

Editor: Marcel Stanitzki
Chaser: Ingrid-Maria Gregor
number of pages to write: 5

6.1 Overview on Strip System

The silicon-strip detector for the new ITk is situated just outside of the pixel detector and is with a silicon area ∼165 m^2 the largest silicon tracker for ATLAS. It consists of a central barrel region between $z = \pm$ 1.4 m and two end-caps that extend the length of the strip detector to $z = \pm$ 3 m.

The strip barrel consists of four full length cylinders of 2.8 m each that surround the beam-line (see Chapter 3). The strip end-caps have six disks on each side (End-cap A and End-cap C) to provide good coverage also under shallow angles. The strip system covers ± 2.5 units of rapidity (see Fig. 6.30).

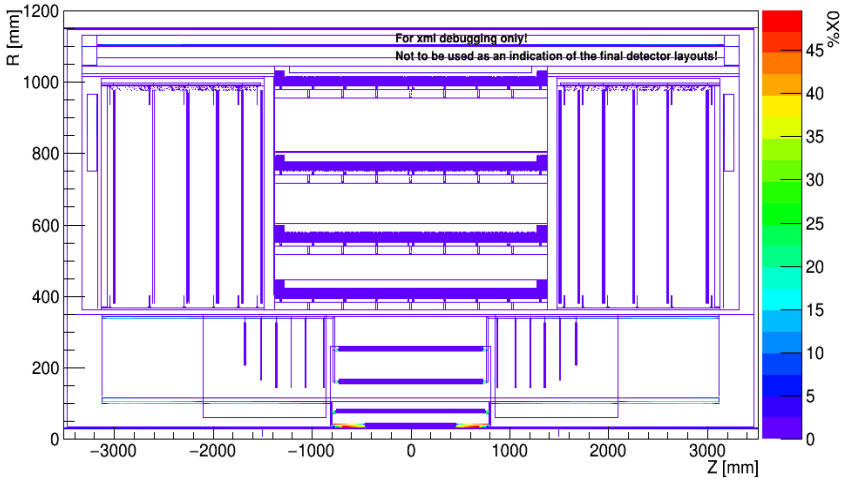

Figure 6.30. The Layout of the ITk detector. This is the upper half of the detector with Z being the beam axis and R the radius of the ATLAS detector. Only the first 31.2 m from the IP are shown.

The basic mechanical building block of the barrel is called a stave, with petals being the equivalent structure for the end-caps. This mechanical building block consists of a low mass central stave/petal core that provides mechanical rigidity, support for the modules, and houses the common electrical, optical and cooling services. All the power and data links are channeled through a end-of-substructure card, which forms the interface to the outside. The technical details and conducted R&D for the local support (stave and petal) including the on-structure electronics is described in Chapter 10.

The four barrel layers consist of 392 this number might still change[IMG] full length staves with sensors on both sides (196 staves on each side of z = 0). Each barrel stave is populated with 28 modules (14 on each stave side). The strips on the inner two cylinders are 24.1 mm long (short-strips) and those on the outer two cylinders are 48.2 mm long (long-strips). The modules in the

barrel section are placed on the stave with a angle of 26 mrad with respect to the beam axis to allow a total stereo angle of 52 mrad. See Chapter 3 for the detailed justification of these choices. In the end-caps each disk is populated with 32 identical petals. The staves and petals will be loaded into global structures (see Chapter 11) which again will be situated within a common mechanics for the ATLAS ITk (see Chapter 15).

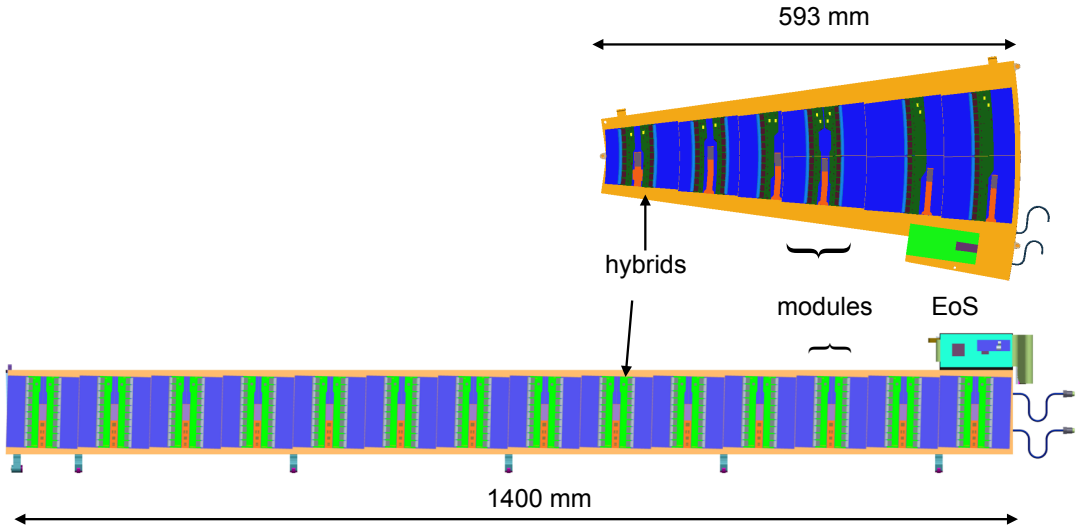

Figure 6.31. End-cap petal (upper) and barrel stave (lower) components overview.

6.2 Numbers of Staves, Petals and other Components of the Strip Detector

An overview of the overall number of staves, petals, modules, hybrids, FE-chips (ABC130*) and the silicon area is given in table 6.14. These are the numbers of items to be installed in the ITk. Spares are not included in this table. The number of parts to be produced during the production including yields and spares are summarised in Chapter 21.

6.3 Design of the Strip Modules

The smallest building blocks of the ITk Strip Detector will be a silicon-strip module. A module consists of one sensor and one to four low-mass PCB's, hosting the readout ASICs, the so-called hybrids. Due to the large number of single-sided modules required for the ITk Strip Detector, the modules have been designed with an emphasis on mass producibility and for low cost. The design is equally focused on material reduction with the elimination of a substrate between the hybrid and the sensor. This is taking advantage of the heat path through the large cross-sectional area to the underlying mechanical support with an embedded cooling. This concept differs from the current ATLAS SCT design, where heat from ASICs and detectors is conducted out laterally through lower cross-section paths leading to the module edge. An exploded view of a short strip module as example is shown in Figure 6.32.

The ITk Strip Modules are constructed by directly gluing kapton flex hybrids to silicon sensors with electronics-grade epoxy. Various different strip lengths and geometries are foreseen, depending on the planned location of the module within the detector. For the barrel two strip lengths

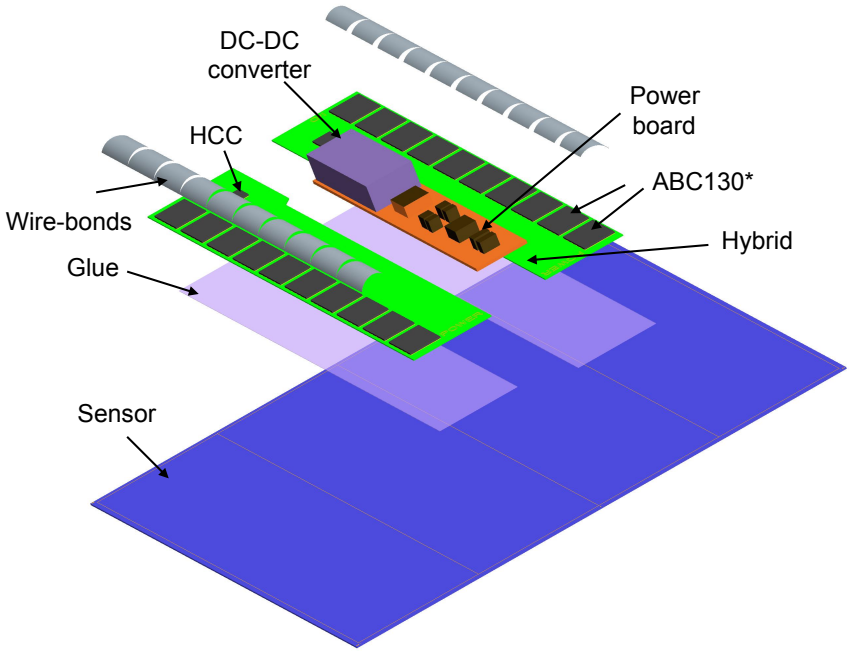

Figure 6.32. Exploded view of a short strip barrel module with all relevant components.

are being used: the long strips in the lower occupancy region at larger radii (layers L2 and L3), whereas further subdivision with shorter strips is required at lower radii (layers L0 and L1). Therefore two different module types are required for the barrel section: the so-called short and long barrel modules where "short" and "long" refers to the strip length. The short barrel modules contain two hybrids, each with ten ABC130⋆readout ASIC. The petals have each nine modules on each side organised in six rings (R0-R5) (see Fig. 6.31). The three inner rings (R0-R2) have one module each and the outer three rings (R3-R5) have two modules butted side-by-side, with the hybrid spanning over the two neighbouring modules. Covering such a complex geometry over a large area requires six different sensor geometries and 13 individual hybrids. The details of the modules for the barrel and the end-caps are described in the three following chapters: in Chapter 7 the various active components to form a silicon strip module including the silicon strip sensor and all necessary ASICs are described. The layout of the hybrids and the power boards required for the modules and the production steps to build a modules including the planned quality assurance measures are summarised in Chapter 8. In Chapter 9 a bunch of results is shown.

6.4 Overall Electronics Architecture

The main electrical components on a short-strip stave are shown as an example in Fig. 6.33 to give an overview on the main electrical components of the ITk strip detector. Charged particles passing through the sensor create an signal charge within the silicon sensor diode. The front-end chip, the ATLAS Binary Chip (ABC130⋆), bonded to the sensors, contains 256 pre-amplifiers and discriminators together with a digital pipeline, data compression, I/O and control circuitry. This signal is fed over wire bond to create a hit/no-hit information depending on the threshold settings. Details to the design of the ABC130⋆can be found in Chapter 7. On each sensor two hybrids with each ten

Barrel Layer:	**Radius [mm]**	**# of staves**	**# of modules**	**# of hybrids**	**# of of ABC130⋆**	**# of channels**	**Area [m^2]**
L0	405	28	784	1568	15680	4.01M	7.49
L1	562	40	1120	2240	22400	5.73M	10.7
L2	762	56	1568	1568	15680	4.01M	14.98
L3	1000	72	2016	2016	20160	5.16M	19.26
Total half barrel		196	5488	7392	73920	18.92M	52.43
Total barrel		392	10976	14784	147840	37.85M	104.86
End-cap Disk:	**z-pos. [mm]**	**# of petals**	**# of modules**	**# of hybrids**	**# of of ABC130⋆**	**# of channels**	**Area [m^2]**
D0	1512	32	576	832	6336	1.62M	5.03
D1	1702	32	576	832	6336	1.62M	5.03
D2	1952	32	576	832	6336	1.62M	5.03
D3	2252	32	576	832	6336	1.62M	5.03
D4	2602	32	576	832	6336	1.62M	5.03
D5	3000	32	576	832	6336	1.62M	5.03
Total one EC		192	3456	4992	43008	11.01M	30.2
Total ECs		384	6912	9984	86016	22.02M	60.4
Total		**776**	**17888**	**24768**	**233856**	**59.87M**	**165.25**

Table 6.14. Number of staves and petals for the ITK strip detector. The numbers for the barrel are for the full barrel with 2.8 m length. The numbers for the end-caps (EC) are given each for one disk in one end-cap. The total end-cap number is the total for both end-caps. UPDATED numbers from April 2016. To be checked carefully[IMG]

ABC130⋆are placed enabling the readout of 2560 strips. The ABC130⋆is planned to be produced in a 130 nm technology, which has the benefits of reduced power, improved radiation tolerance, and higher circuit density, while having a reasonable price for both prototyping and production. It has been shown to be the optimal technology choice enabling a low-noise performance for the pre-amplifier. Each hybrid has a Hybrid Controller Chip (HCC) that interfaces the stave/petal service bus (stave/petal side) and the front-end ASICs on the strip detector hybrids (hybrid side). Details of the ABC130⋆and the HCCincluding radiation tolerance studies are given in Chapter 7. The low-voltage power converter and the high-voltage switching circuit is combined in one power board which will be located on the sensor between the two hybrids. It connects to the EoSand is distributed to each hybrid via a power bus. A power interface connects each hybrid to the power bus.

Trigger, Timing, and Control (TTC) signals arriving from the off-detector systems are sent from the EoSto each HCCvia the TTC bus on the bus-tape. The TTC consists of a 40 MHz system clock, a serial command/L0 trigger, and a R3/L1 Might need update[IMG] trigger that are sent to each HCCin parallel. The TTC bus and data lines and power bus are integrated into a single copper/kapton bus tape that is co-cured onto the stave core. The EoSincludes a GigaBit Transceiver (GBTx) or low power GBT (lpGBTx) that interfaces with the HCCASICs and a Versatile link

(VTRx)) fibre optic driver [11]. here a comment where this is described later on[IMG]

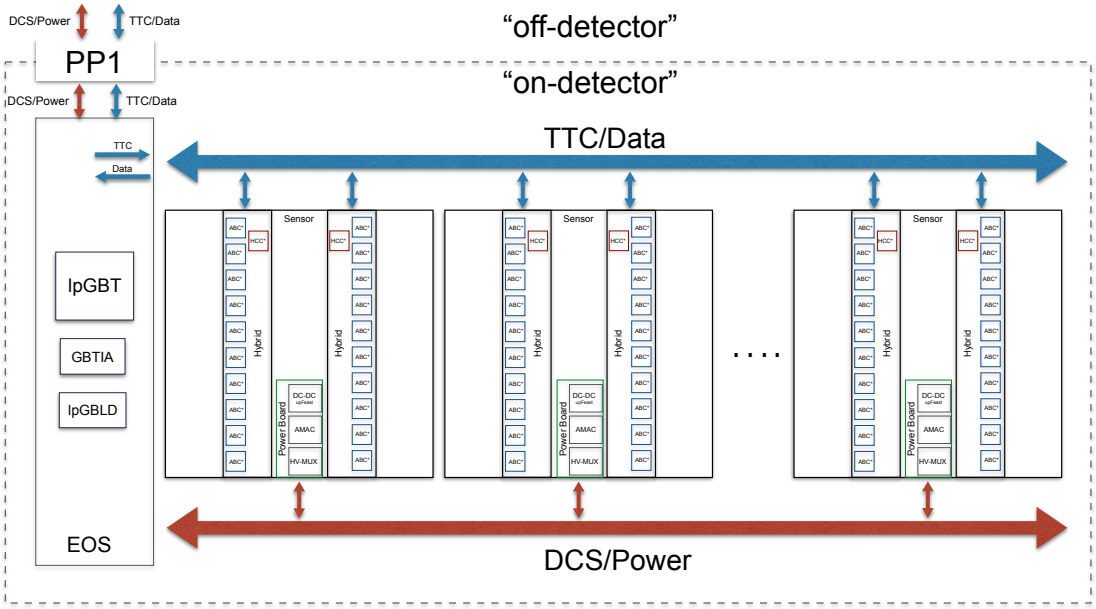

Figure 6.33. Overview of the electronics components of the ITk Strip detector located within the active area of the detector. In this document the interface between "on-detector" and "off-detector" is defined as the first patch panel (PP1).

6.5 Star Design

Since the design of the prototype ABC130, the ATLAS upgrade trigger requirement has been changed, increasing from L0/L1 of 500 kHz /200 kHz to 1 MHz/400 kHz. In addition, studies of trigger timing and latency have shown that, at most, a chain of only three ABC130devices may be used in high occupancy regions of the strip detector do we have a reference for this?. Taken together, these issues have led the project to re-evaluate the architecture of the on-detector electronics: a star architecture is now the baseline, with point-to-point connections between each ABC130⋆and the HCC. The HCCmay now build and transmit module wide events, making more efficient use of the available bandwidth. Taken together these changes permit full detector readout at 1 MHz L0, a significant simplification of the system architecture. However, to support this new topology, the hybrid will require one additional routing layer and, to maintain a safety factor of two, the HCC will require 320 Mbit down-link bandwidth back to the EoS.

Serial transfer of data to the HCC was changed to direct communication from all ABCs to the HCC hence the new ABC130⋆and HCC⋆. The "star" configuration removed a bottleneck in data transfer to the HCC, which had considerable bandwidth still available. While both ASICs required changes, the HCC⋆required nearly a complete redesign as it must now essentially build events in parallel from fragments coming from all the ABC130⋆. The specifications of the ABC130⋆and HCC⋆will be summarised in Chapter **??** and Chapter **??** respectively. As these ASICs were not

available at the prototype stage, all R&D studies presented in this TDR are based on the daisy chain ABC130and HCC. maybe I should add more details here[IMG]

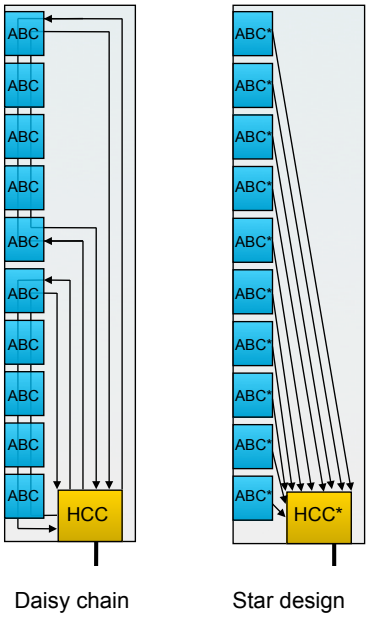

Figure 6.34. Sketch of the original daisy chain signal routing in comparison to the new star design.

6.6 LV Powering Scheme

With the increase in the total number of channels, and despite a reduction in the power consumption per channel, more total power is required for the ITk strips than for the current ATLAS ID. In addition, there is no space for extra cables from the counting rooms to the cavern, and adding more cables would lead to extra material. Therefore, a more efficient way to provide power to the modules is required for the ITk. The baseline for the strip detector is DC to DC conversion (DC-DC), with off-detector power supplies at a higher voltage, reducing the current on the cables and the ohmic losses ref to P1. On-detector, buck DC-DC converters lower the voltage to the required by the on-detector electronics. This requires the design of radiation hard DC-DC converters (see Chapter YY). The DC-DC powering scheme is explained in detail in ChapterXX.

References:

P1: Affolder,A.etal. DC-DC converters with reduced mass for trackers at the HL-LHC, JINST 6 (2008).

P2: Faccio, F. et al. FEAST2: A Radiation and Magnetic Field Tolerant Point-of-Load Buck DC/DC Converter, REDW 2014.

6.7 Working Temperature

For a safe long-term operation of the tracker it is necessary that the sensors and electronics have good contact to the cooling pipe at -35 C°. This requires a system for thermal monitoring with high

Ring	Hybrid	Row	nStrips	nChips	Inner radius	Outer radius	Length [mm]
0	R0H0	0	1026	8	384,5	403,5	19,0
		1	1026	8	403,5	427,5	24,0
	R0H1	2	1154	9	427,5	456,4	28,9
		3	1154	9	456,4	488,4	32,0
1	R1H0	0	1282	10	489,8	507,9	18,1
		1	1282	10	507,9	535,0	27,1
	R1H1	2	1410	11	535 ,0	559,1	24,1
		3	1410	11	559,1	574,2	15,1
2	R2H0	0	1538	12	575,6	606,4	30,8
		1	1538	12	606,4	637,2	30,8
3	R3H0 /	0	898	7	638,6	670,8	32,2
	R3H1	1	898	7	670,8	697,1	26,2
	R3H2 /	2	898	7	697,1	723,3	26,2
	R3H3	3	898	7	723,3	755,5	32,2
4	R4H0 /	0	1026	8	756,9	811,5	54,6
	R4H1	1	1026	8	811,5	866,1	54,6
5	R5H0 /	0	1154	9	867,5	907,6	40,2
	R5H1	1	1154	9	907,6	967,8	60,2

Table 6.15. The hybrids for the end-cap modules. Depending on the location of the module on the petal the strip length, the number of strips per module varies. Check names of hybrids[IMG]

granularity. Some of the signals in that system will be used for hardware interlock. Due to various heat sources within the thermal enclosure the average ambient temperature will be several degrees above this, but the exact amount is difficult to estimate now. if decided, somewhere we have to explain the more complex warm and cold phased required by the TID bump

6.8 Definition of Envelopes between Pixel System and Strip System

have to discuss this with Paolo and Philippe[IMG]

6.9 Interfaces with the ITk Pixel System

have to discuss this with Paolo and Philippe[IMG]

6.10 AoB

following a list of issues which should be mentioned here – or somewhere else[IMG]

- explanation that all tests are done with ABC130 and that ABC130star comes later
- latency -> here or somewhere else ?
- other overview topics like TDAQ etc. ?
- radiation levels for the various areas in the strip system

7. Silicon Strips Modules – Active Components

Editor: Marcel Stanitzki

Chaser: Ingrid-Maria Gregor

Number of pages to write: 20

In the following sections the various active ITk strip module components, from the sensor itself to the individual ASICs, are described in detail. All relevant studies demonstrating the full functionality are presented, including the performance after irradiation if available.

7.1 The Silicon Strip Sensor

The current baseline design of the ITk strips is based on 6-inch wafer technology. In the barrel region, the sensors are square, with nearly the maximum size that can be inscribed in a safe wafer area. In the end-cap, the sensors are roughly trapezoidal with two curved edges, convex and concave. The chosen strip sensors are AC-coupled with n-type implants in a p-type float-zone silicon bulk (n^+-in-p FZ). Bias resistors are implemented by polysilicon implants. Inter-strip isolation will be achieved by p-stop implants, uniform p-spray, or a combination of both. This type of sensor collects electrons and has no radiation induced type inversion. The sensors' target thickness is 300-320 μm. The radiation tolerance is a key requirement for the strip sensors; the expected maximum fluence of 8.1 $\cdot 10^{14}$ n_{eq}/cm^2, an ionizing dose of 33.3 MRad and to operate up to 700 V. To allow for uncertainties in fluence calculations, a safety factor of two is imposed for the fluence and ionizing dose (see Chapter 3). The main reason for choosing n-on-p technology over the p-on-n used in the current ATLAS SCT is the large difference in the amount of signal post-irradiation reference to ATLAS07, paper 1[IMG]. In the range of 8-10$\times 10^{14} n_{eq}/cm^2$ n^+-in-p sensors deliver than a factor of two more charge. A detailed list of specifications for the sensor before and after irradiation are given in table 7.16.

The current design of the barrel sensors foresees an active area of 96.640 $\times$ 96.669 mm^2 to maximally utilise the area of a 6-inch (150 mm) wafer. There are 1280 readout strips and a field-shaping strip at each side across a sensor, giving a strip pitch of 75.5 μm. The strips are parallel to the sides of the sensor. On a stave, the stereo angle is achieved by rotating the modules on both sides by 26 mrad. There are two variations of barrel sensors: one has four rows of short strips (24.10 mm) and the other has two rows of longer strips (48.20 mm) for the short strip and long strip modules, respectively.

The petal sensors require radial strips (i.e. pointing to the beam-axis) to give a measurement of the $r\phi$ coordinate. As a result, these sensors have a wedge shape. The dimensions of the sensors have been chosen to use as few silicon wafers as possible with 32 petals per disk and fully covering the radial range required by the layout. The 40 mrad stereo angle between strips on opposite sides of a petal is achieved by rotating the strips 20 mrad within the sensors. The strip lengths are chosen to balance the strip occupancy with the shortest strips closest to the beam region. The segmentation was also determined by the maximum latency requirement of the readout, which is closely related to the occupancy and channel count. The strip pitch was constrained to be as close as possible to the barrel pitch (75.5 μm) at the bond pad region to allow direct wire bonding between the readout ASIC and the sensor. This results in three rings (R0, R1, and R3) with four strip rows and three

Substrate Material	
Size	8-inch/200 mm or 6-inch/150 mm
Type	p-type FZ
Crystal orientation	<100>
Thickness (physical)	200-220/300-320 μm
Thickness (active)	>= 90% of physical thickness
Thickness tolerance	$\pm$ 5 %
Resistivity	$>$ 3 kΩcm
Oxygen concentration	$1{\cdot}10^{16}$ to $7{\cdot}10^{17}$cm^{-3}
Sensor specifications before irradiation	
Full depletion voltage	$<$ 330 V (preference for $<$ 150 V)
Maximum operating voltage	600 V
Poly-silicon bias resistors	1-2 MΩ
Inter-strip resistance	$>$ 10 $\times$ Rbias at 300 V at 23C$^\circ$
Inter-strip capacitance	$<$ 1 pF/cm at 300 V, measured at 100 kHz
Coupling capacitance	$>$ 20pF/cm at 1 kHz
Resistance of readout Al strips	$<$ 15 Ω/cm
Resistance of n-implant strip	$<$ 20 kΩ/cm
Onset of micro-discharge at	$>$ 600 V (preferred)
Total initial leakage current, including guard ring:	$< 0.1\ \mu A/cm^2$ at 600 V at room temperature
Number of strip defects	$<$ 1% per strip/segment and $<$ 1% per sensor
After irradiation (2$\cdot 10^{15}$ n$_{eq}$/cm^2 – 60 Mrad)	
Onset of micro-discharge at	$>$ 600 V or Vfd + 50 V after irradiation (if lower)
Inter-strip resistance:	> 10 $\times$ Rbias at 400 V and for T $= -20$C$^\circ$
Collected charge	$>$ 7500 electrons per MIP at 500V
Mechanical Specifications and Optical Inspection	
Dicing precision	$< \pm 20\mu$m or better
Sensor bow after process and dicing	$<$ 200 μm

Table 7.16. Sensor specifications.

rings (R2, R4 and R5) with two rows. In Table 7.17 the various sensor types with dimensions are summarised.

Two generations of barrel short strip sensors have been fabricated: ATLAS07 [12] and ATLAS12 [2]. With ATLAS07, the performance of the baseline sensor technology (n^+-in-p FZ) with p-stop, p-spray and mixed isolation were shown to meet all specifications. The ATLAS12 series utilised p-stop isolation only and included a number of improvements: enhanced punch-through protection structures at the end of strips; a smaller inactive edge space (450 μm in the longitudinal direction; 500 μm in the lateral direction), which reduces the dead region of the sensors; and modification to the bond pad layout to match the ABC130*readout ASIC. Miniature strip sensors (1 $\times$ 1 cm^2) have been included in the wafers of both series to enable an extensive irradiation and testing

Sensor Type	Number of Sensors	Shape	Number of Columns	Channels per Sensor	Min/Max Pitch (μm)
Short Barrel	6000	Square	4	5128	74.5
Long Barrel	8000	Square	2	2564	74.5
Ring 0	1000	Trapezoid	4	4360	73.5/84
Ring 1	1000	Trapezoid	4	5640	69/81
Ring 2	1000	Trapezoid	2	3076	73.5/84
Ring 3	2000	Trapezoid	4	3592	70.6/83.5
Ring 4	2000	Trapezoid	2	2052	73.4/83.9
Ring 5	2000	Trapezoid	2	2308	74.8/83.6

Table 7.17. Overview of the number of sensors per required shape with number of columns, channels and pitch. Phil suggested to have either the sketches of the sensors added here[IMG]

program reference to papers 1-6, see below[IMG]; these studies include a full suite of surface and bulk properties evaluation. Irradiations were conducted at six different facilities. A batch of 120 sensors with four rows of axial strips (ATLAS12A, see figure 7.35) has been delivered for detailed studies of module, stave, and petal prototyping using the 130 nm ASIC set. In addition, a batch of 45 sensors with two rows of axial and two rows of "stereo (40 mrad rotated)" strips (ATLAS12M) for prototyping a "stereo" sensor. In the following, the most relevant results are summarised. add table with specs somewhere here; a la cds.cern.ch/record/974073/files/indet-pub-2006-005.pdf [IMG]

References: ATLAS07:

1. K. Hara et al., Nucl. Instr. Meth. A636 (2011) S83-S89; J. Bohm et al., Nucl. Instr. Meth. A636 (2011) S104-S110;
2. S. Lindgren et al., Nucl. Instr. Meth. A636 (2011) S111-S117

ATLAS12:

3. K. Hara et al., Nucl. Instr. Meth. A (in press, DOI:10.1016/j.nima.2016.04.035);
4. M. Mikestikova et al., Nucl. Instr. Meth. A (in press, DOI: 10.1016/j.nima.2016.03.056;
5. L.B.A. Hommels et al., Nucl. Instr. Meth. A (in press, DOI: 10.1016/j.nima.2016.03.042;
6. R. Mori et al., Nucl. Instr. Meth. A (in press, DOI: 10.1016/j.nima.2016.04.044

7.1.1 Charge Collection Efficiency after Irradiation

The charge collection from miniature p-bulk FZ sensors of 310-320 μm thickness using penetrating beta rays from ^{90}Sr sources was extensively studied. Highly consistent results were obtained by the groups that participated in the measurements both prior to irradiation and after irradiations to fluences as expected in the strip system. After irradiation, differences in the charge collection between the ATLAS07 and ATLAS12 devices observed are due to different initial resistivity; the charge collection differences diminish with increasing irradiation fluence and bias voltage. what range of values?[PPA] The effect depends on the particles used for the irradiation. Samples irradiated with protons show a small difference in charge collection, while those irradiated with neutrons show

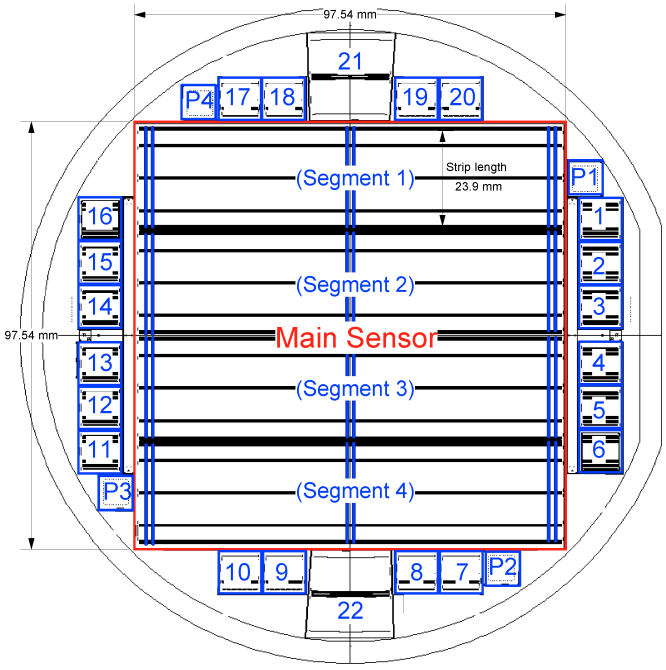

Figure 7.35. ATLAS12A 6-in. wafer layout. The main sensor in this prototype layout is 97.54 × 97.54 mm^2 with four rows of short strips.

a larger difference below $1{\cdot}10^{15}$ n_{eq}/cm^2 . The reduction in the charge collection is largest for neutron irradiation followed by that for 23 MeV proton irradiation. Damage caused by 300 MeV pions is the least for the same NIEL fluence. The results were also verified by independent measurements using an electron beam at the DESY-II Test Beam Facility.

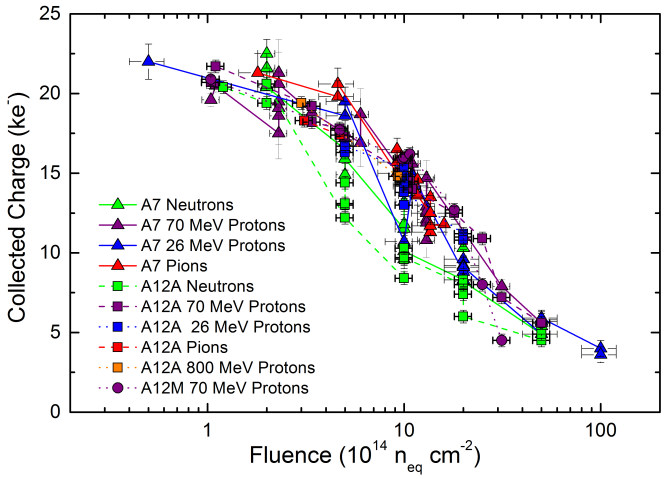

Figure 7.36. Collected signal charge at 500 V bias voltage for minimum ionising particles as a function of 1MeV n_{eq}/cm^2 fluence for various types of particles. Reference to 3. above[IMG].

The carrier velocity profiles across the depth were evaluated using an edge transient current technique (TCT) here a reference to RD50[IMG]. The profiles differ for different irradiating particles,

neutrons, protons, and pions. The field near the back-side is the largest for the pion-irradiated samples, which explains the largest charge collection observed for these samples. This is really detailed. If it is included you need to explain why. It would be good to cover a lot by referencing RD50 to avoid detailed discussions here and it seems odd not to mention RD50 in this context.[PPA]

The expected signal-to-noise ratios after the high fluence can be evaluated using the equivalent noise charge (ENC) values of the readout electronics with corresponding wire-bonded sensors. Typical ENC noise values are 550 e^- for the barrel with 48 mm connected, for the barrel with 24 mm long strips connected, 720 and 650 e^- for the end-cap module. Assuming the safety factor of two and neutron damage dominance, a conservative estimate for the lowest S/N value of 14 is derived. Reference to 3. above[IMG].

7.1.2 Surface properties after irradiation

The changes in the surface properties of the baseline sensor technology (n^+-in-p FZ) have been studied after ionising and non-ionising irradiations. Non-ionising irradiation typically displaces silicon atoms which result in point and cluster defects in the bulk. Ionising irradiation results an accumulation of positive charges and traps in the SiO_2 and Si-SiO_2 interface which cause the majority of the changes in the surface properties of silicon sensors after irradiation. Sensor properties that could change are: the inter-strip resistance and capacitance, the coupling capacitance between the readout strip's Aluminium and implant, the strip's bias resistance and the punch-through protection (PTP) structure's performance.

Miniature sensors were used to determine any changes with irradiation at multiple sites within the collaboration after irradiations by ^{60}Co gamma rays, 23 MeV and 70 MeV protons, and reactor neutrons. The inter-strip capacitance and coupling capacitance showed no measurable change over the full range of fluences expected for the strip system. The polysilicon bias resistance was shown to increase slightly with proton fluence and gamma dose (from 1.5 to 2.1 MΩ), but remains acceptable within the 3 MΩ specification. The PTP structures have been tested up to expected pixel fluences ($1{\cdot}10^{16}$ n_{eq}/cm^2) with the onset voltage of the protection increasing from 15 V to 30 V; as the coupling capacitors are specified to have a hold-off voltage of at least 100 V, these structures will work as designed for the lifetime of the strip detector.

The inter-strip resistance showed the largest changes under irradiation as shown in Fig. 7.37 and Fig. 7.38. Neutron irradiated devices show smallest changes as expected as the majority of the damage is to the bulk sensor. The proton and gamma irradiations showed similar degradation; the inter-strip resistance reaches the conservative specification at around $3{\cdot}10^{15}$ n_{eq}/cm^2 ; it is 100 MΩ at the $2{\cdot}10^{15}$ maximum strip fluence with the two times the safety factor, which is well above the 15 MΩ specification.

Reference to 4. above[IMG]. M. Mikestikova, et al., Nuclear Instruments & Methods in Physics Research A (2016), *http://dx.doi.org/10.1016/j.nima.2016.03.056*

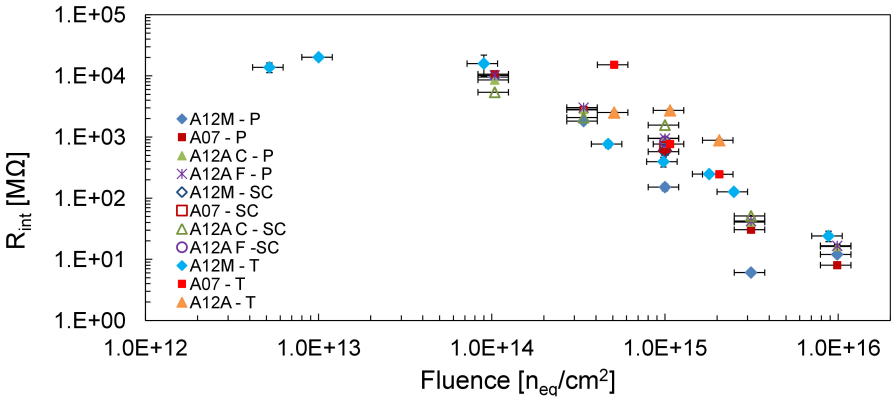

Figure 7.37. Inter-strip resistance vs. proton fluence for ATLAS12A, 12 M and 07 barrel samples irradiated in the same irradiation campaign at CYRIC and measured by various laboratories at bias voltage of 400 V. The results are normalised to temperature of -20^o C.Reference to 4. above[IMG].

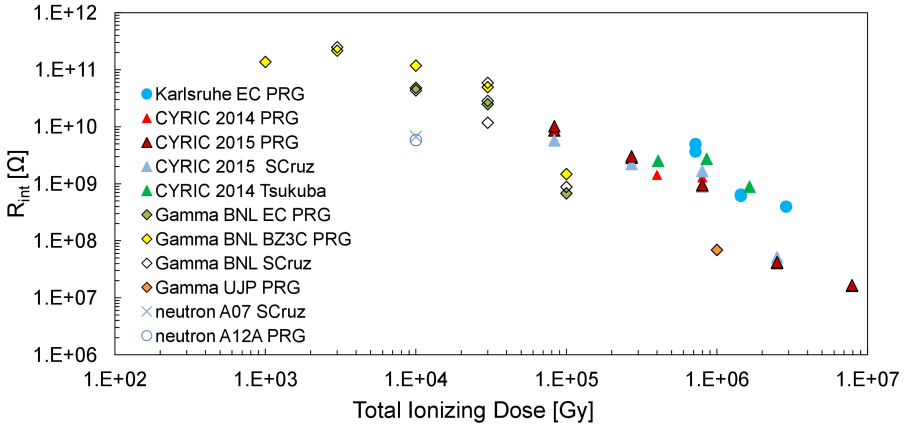

Figure 7.38. Inter-strip resistance vs. total ionizing dose for ATLAS12 sensors irradiated by protons, neutrons and gammas at different irradiation sites. Results at bias voltage -400 V are presented The results are normalised to temperature of -20^o C.

7.1.3 Lorentz Angle before and after irradiation

this has been measured with mini sensors in a 1 T magnet at the DESY test beam up to HL-LHC fluences. Results are currently being reviewed by the ITk strips collaboration.
Text will be provided by Kerstin Tackmann and Ingrid[IMG]

7.1.4 Full Size Barrel Prototype

100 of the 120 full-size (97 $\times$ 97 mm^2) ATLAS12A sensors produced at Hamamatsu have gone through the full quality assurance reception testing. The study included the measurements of the shape of the sensor (bow), a visual inspection, measurements of global electrical parameters (leakage current, depletion voltage) and measurements of individual strip parameters (leakage current, bias resistance, coupling capacitance) through the use of a multi-channel probe card.

The devices were highly uniform with only one device outside of specification due to a section

of ∼230 channels with a low coupling capacitance and a high bias resistance of up to 10 MΩ. The sensors are remarkably flat with an average bow of 51 microns corner-to-center. quantitative discussion better and need those specifications[PPA] Figure 7.39 shows the high quality of the full sensor's leakage current, in which all sensor pass the specification and most show no breakdown behaviour to maximum tested voltage (1000 V). Only 132 faulty channels (outside the faulty sensors) were found in over 0.5 million channels; the 99.97 % good strip fraction comfortably exceeds the 98 % requirement (see Chapter 2). Reference to 5. above[IMG].

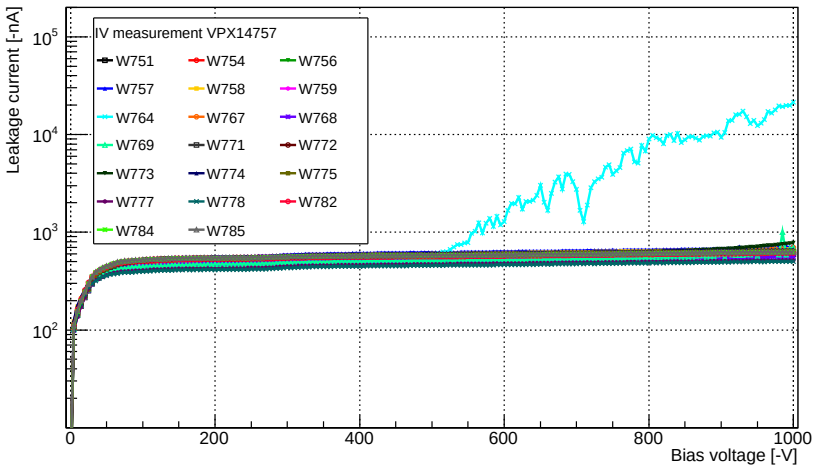

Figure 7.39. IV characteristics of large area ATLAS12 sensors at 21^{o}C exemplary for one batch.Reference to 5. above[IMG].

7.1.5 End-Cap Specific Studies

Due to the complex geometry of the end-cap, six different sensor designs are needed to cover the petal surface. It was decided to implement the strips pointing to the beam axis resulting in wedge shaped strips. Each face of a petal has nine sensors arranged in six rings named R0, R1, ... R5 from inner side to outer. R0, R1, and R2 have one sensor per petal-face; the outer three have two identical sensors per face. The two faces are identical, so in total there are six sensor designs. The sensor sizes and shapes were optimised for 6-inch wafers. Different potential layout options which may be useful for the design of end-cap sensors have been explored.

The sensor layout is chosen to cover the petal with active strips, minimising the dead space such as guard regions and physical gaps between sensors. The stereo angle is built into the sensor – as opposed to making symmetric sensors, then rotating them by the stereo angle as decided for the sensors on the barrel. Due to varying geometry of neighbouring sensors in the end-cap the physical rotation of sensors would lead to clashes.

The chosen shape for all end-cap sensor is referred to as "Stereo Annulus": the inner and outer edges are concentric arcs of circles, centred at the centre of the disk, to cover part of an annulus. The two sides are straight, but do not point to the centre of the wheel. Instead they are rotated away from the wheel centre by the stereo angle (ϕ_s = 20 mrad). Figure 7.40 shows how the sensor is designed to have the stereo angle built in. On the left side the principle geometry is explained. On

the right hand side the sensor R0 for the innermost region of the end-caps is shown as an example for the end-cap sensors.

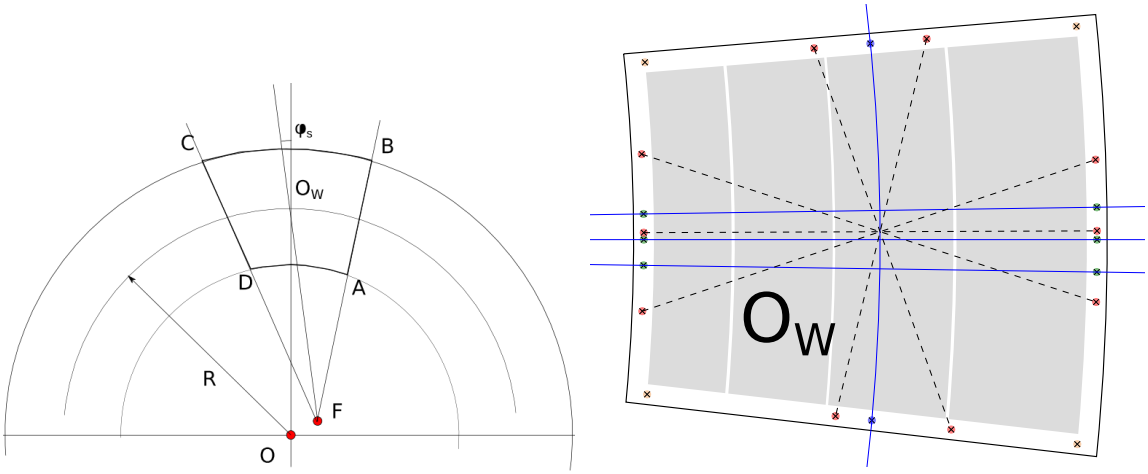

Figure 7.40. Left: Sketch showing how Stereo Annulus sensor geometry is made. The sensor is drawn connecting ABCD, the arcs CB and DA are centred at O which is the centre of the beam pipe. The strips are pointing to F which is slightly displaced from O due to the implemented stereo angle. Right: A drawing of the innermost sensor on a petal R0. Fiducials determine the centre of the sensor, the radius of the sensor in the global system and the corners of the sensitive area.

Further sensor layouts for the end-caps with implemented stereo angle and straight sensor edges were investigated. Straight edges are easier to produce and minimise the dead area between the sensors. Such a design could lead to strips at the edge of the sensor do not directly connect to the readout strip (orphan strips); if not corrected, this would result in inactive areas of the sensor for each row of channels. It was shown that this can be overcome by ganging the orphan strips to other strips that are connected to the readout chips. With special ATLAS12A end cap miniature sensors, two methods of ganging was explored: a metal strip which connects the implant of two strips (DC ganging) and a metal strip connecting the AC-coupling metal of two strips (AC ganging). It was shown that such a sensor can be designed and produced. Nevertheless, the skewed sensors were chosen as that layout does not require ganging of strips at all. reference to 6. above[IMG]

7.1.6 Preparing the Preproduction

As the process of understanding the radiation damage effects in this particular implementation is rather advanced, the ATLAS ITk strip group is initiating a sensor market survey together with the CMS outer tracker group. Both experiments chose very similar processes and therefore a combined market survey will help to understand the world wide sensor production possibilities for these large tracking systems. The process involves a three-step qualification before vendors are chosen for the delivery of the sensors. A detailed specification document was prepared which was submitted by CERN to possible vendors and posted on procurement web site of CERN. In step 1 of the qualification process the responses of various companies are collected. In step 2 free samples from previous work of the companies are collected and qualified. In the last step samples are ordered

which are produced according to the ATLAS ITk strip specification and are qualified by the ATLAS community. Only after the completion of this process a call for tender will be initiated.

7.1.7 Quality Control During Production

currently being written by Bart Hommels[IMG]

7.2 The ATLAS Binary Chip ABC130

LauraG Note: All figures will be provided in a better format in their final version. Adapted from the IDR

the following section was taken from "System Electronics for the ATLAS Upgraded Strip Detector" from Feb 2013 - number to be cross checked[IMG]

A chip set has been designed in IBM 130 nm CMOS8RF technology: the ABC130front-end (Ref. 1, 2) and the HCC(see section 7.3). Both chips are currently under evaluation. The chip set is based on a daisy-chain readout architecture, where data are serially transmitted through a group of front-end chips and then through the HCC. These new ASICs include additional capabilities aligned to the ATLAS upgrade trigger requirements.

The prototype analog binary chip (ABC130) used for most of the studies presented in this TDR provides all functions required for processing the signals from 256 strips of a silicon strip detector employing the binary readout architecture. The simplified block diagram of the hookup of the chip is shown in Figure 7.41. The main functional blocks are: front-end, input register, pipeline, derandomising buffer, data compression logic blocks, command decoder, readout logic, threshold & calibration control, power regulation.

The architecture chosen for the ABC130 allows a multi-trigger data flow control retaining the beam crossing synchronous pipeline transfer signal (L0) from previous ABC versions and a new asynchronous Regional Readout Request (R3) and a second level asynchronous data readout intended for a global readout (L1 here). The ABC130 contains 256 analogue preamplifier-shapers followed by discriminators with individual threshold trimming capabilities. The shaping time should allow 0.75 fC pulse detection separated by 75 ns. The binary outputs of the discriminators (data) are sampled at the bunch crossing clocking rate (BC) and stored for 6.4 μs in the "pipeline" or L0_Buffer memory bank. At the reception of a L0 signal, the data in the memory that were stored at some fixed latency time before the L0 signal are extracted from the pipeline and transferred to the derandomising buffer (R3L1_Buffer) and stored. The data corresponding to three consecutive time slots are transferred for each L0 and form an event. There is enough room in the R3L1_Buffer for 256 events. After 256 events are stored, new events overwrite the R3L1_Buffer content. At reception of a "R3" signal (R3s_L1 output from the HCC, see below), which carries a L0 identifier, the event that has the same L0 number is extracted from the R3L1_Buffer and processed through the R3 Data Compression Logic block that performs zero suppression and cluster identification. The same happens at the reception of a "L1" signal (R3s_L1 output from the HCC), but the event with the correct L0 number is processed through the L1 Data Compression Logic block.

the following too detailed or not detailed enough? [IMG] The R3 and L1 Data Compression Logic (DCL) differ in their algorithms to detect clusters and perform cluster identification, however, both algorithms will apply the same hit criteria as the present ATLAS-SCT chip, the ABCD. That is,

a hit channel can be defined by the time sequence X1X, 01X, or XXX where 0 is no-hit, 1 is hit and X is don?t care and the three bits represent the discriminator result for three consecutive beam crossings centred on the trigger BC. Which criteria to use is set by the configuration register. The information extracted from the 2 DCLs is different, for example the R3 unit is limited to identify four clusters at maximum and produces one data packet. The L1 unit is not limited in the number of clusters and number of packets produced. The information extracted from the DCL contains a channel number to identify each cluster and bits that represent the cluster shape. The data are stored in local FIFOs to be transferred at the proper time to the Readout block.

The Readout block contains a packet builder and a fast serialiser. The packet builder gets the data from either:

- The adjacent chip (external)
- The R3_DCL (internal)
- The L1_DCL (internal)
- The internal registers (internal)

The priority of data is set according to this order. The data from an adjacent chip is already formatted and is simply transferred to the serialiser.

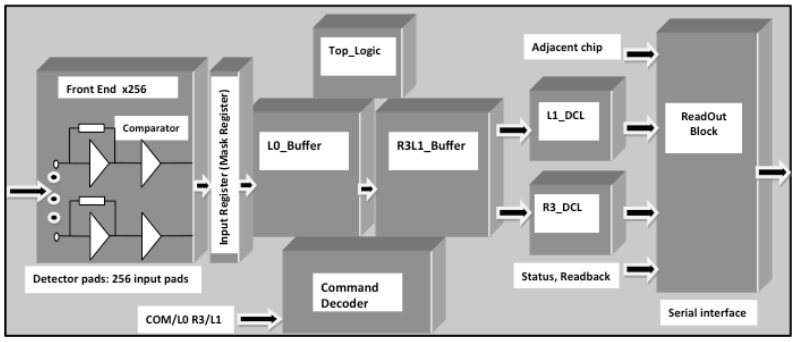

Figure 7.41. Block diagram of the ABC130 readout part with the R3 capability. All the ABC130s receive L0A and extract the corresponding data from the pipeline (L0_Buffer). These data are stored together with a L0ID in the R3L1_Buffer. Only those in the region of interest receive R3 signal and send immediately the corresponding data. L1A comes later together with the L0ID to which it refers. This L0ID is used to select data in the R3L1_Buffer and send them. The TTC system requires higher bandwidth for the R3 Scheme as some additional information is to be sent together with L0A and L1A.

The chips' geometry aids mass-production, improving the wire bonding rates and reliability. The number of channels in the ABC130has been doubled to 256 compared to the previous prototype version in 250 nm technology (the ABC250) to allow for the read out from two adjacent rows of strips. This increase in channel density reduces the overall material in the hybrids.

7.2.1 ABC130characterisation: Results before irradiation

Noise measurements

The noise measured on the bare ABC130chip is approximately 450 ENC (equivalent noise charge)how is this measured?[IMG]. This number is in disagreement with measurement on the prototype front-end, which showed a noise below 400 ENC. The prototype front-end was, however, designed and tested for positive input signals. Whilst the simulations had shown only a 5 to 8% increase in noise, depending on the model used and its accuracy, the ENC difference between positive and negative signal response measured on the FE prototype is up to 20%. Measurements of noise on an ABC130single chip with capacitive load at the input, and on modules with FIB chips[2], are in agreement with results obtained on the FE prototype with negative input signals. The reason for the difference in noise between positive and negative input signals is due to the effect of compression for negative signals, which leads to a modulation of feedback transistor gmthis was not explained...[IMG]. A resistive feedback will be used in the final chip version, the ABC130⋆(see below), to resolve this issue. Results on first, fully equipped SS and LS modules show even higher noise, respectively, around 750 ENC and 1100 ENC. Investigations of hybrid layout, grounding, and readout is ongoing to understand this effect. Noise measurements on the ABC130chip are summarised in Figure 7.42. have to update this accordingly when we know the cause of this – I hope[IMG]

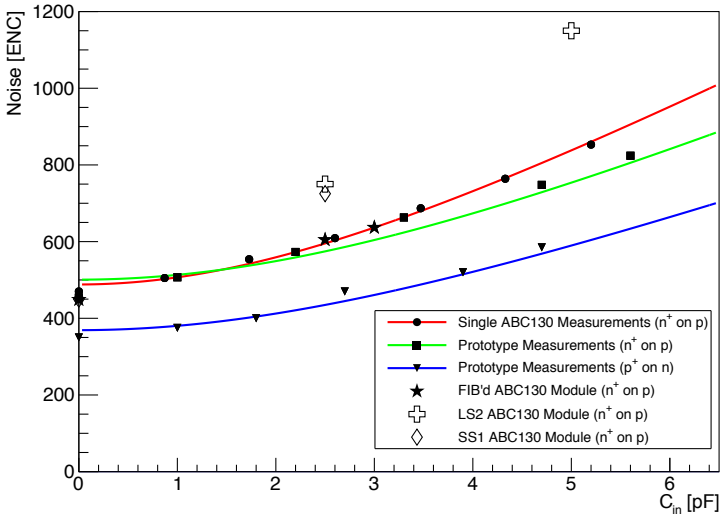

Figure 7.42. Noise measurement as a function of input capacitance for the ABC130chip, the front-end prototype (both positive and negative input signal polarity), FIB modules, short strips and long strip modules.

Input to be provided later on, in discussion with test beam groups. (Discussion is still ongoing on the method to use to get consistent results between lab measurements, source, laser, and test beam measurements. Currently multiple answers have been derived, ranging from 70mV to 100mV)[IMG]

[2]The first prototype of the ABC130 had a discrepancy between reality and functional model for the polarity of "direction" signal which was repaired for a small number of samples with a fusion ion beam (FIB) – here these prototypes are referred to as FIB chips

7.2.2 ABC130characterisation: Results after irradiation

The ABC130chip has undergone extensive x-ray and protons irradiations to test its TID tolerance. Early irradiations campaigns with x-rays at 60 krad/h and 2.25 Mrad/h at -15 C and +30 C have shown a digital current increase, peaking around 1-2 Mrad (ref 5). As shown in Figure 7.43, the increase depends on the dose rate and temperature during irradiation. This effect is well understood and typical of the 130 nm technology nodes (Ref 3, 4). The reason is the increase of the leakage current of the NMOS transistors, due to positive charge trapped in the STI define[MS] oxide. This effect is counterbalanced by the generation of interface states at higher TID, which trap negative charges in the case of NMOS transistors. No increase of the analogue current of the ABC130chip is observed as ELT transistors are used.

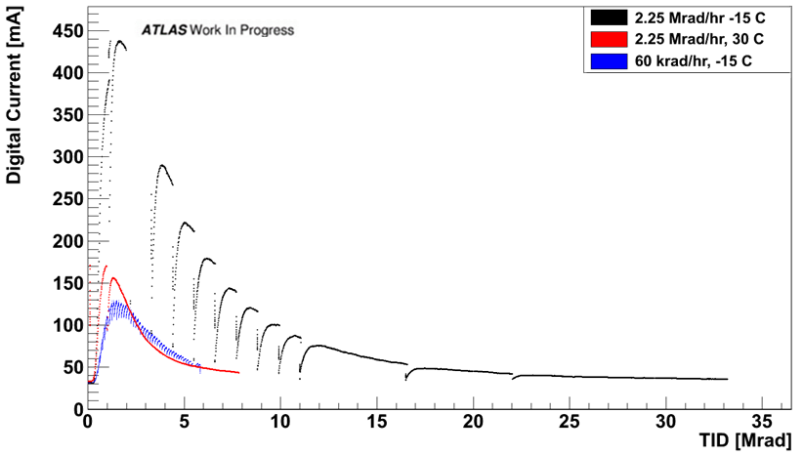

Figure 7.43. Digital current vs. TID for x-rays irradiations at different dose rates and temperatures. to be replaced by high better quality fig.[IMG]

Low dose rate irradiation campaigns have started at the ^{60}Co source at CERN to mimic the dose rates in the different part of the detector during operation. A first campaign at -25 C° and 2 krad/h (highest HL-LHC dose rate for ITk strips) gives a factor 2.5 increase on digital current (figure 7.44). More irradiations are planned at lower dose rates and higher temperature (-10C), following updated results of both fluence and TID in the detector, as well as thermal FEA simulations.

A noise increase is observed after ionising radiation. As shown in Figure 7.45 the noise increases with TID to reach a plateau after 15-20 Mrad. No recovery towards the pre-rad value is observed. The most likely reason is 1/f noise. The simulated pre-rad contribution of the 1/f noise to ENC is at the level of 3%. Some reports for 130 nm technologies (ref 6, 7 and 8) show a substantial increase of the 1/f noise for regular NMOS devices and no change for the enclosed structures. For the ABCStar all critical (for noise) NMOS devices will be in an enclosed geometry.

Gain: The gain degradation with TID shows a peak followed by a rebound, similar to what is observed for the current (Figure 7.46). Depending on dose rate and temperature during irradiation, the gain can decrease by about ˜10%, before recovering towards the pre-rad value. For realistic operating conditions the decrease is only around 2%.

SEE results: SEU test have been performed at CHARM with 24 GeV protons (Ref 9, 10, and 11). Each spill of O(5s) delivers approximately 3x10ˆ9 protons. A TID of 6 Mrad was reached

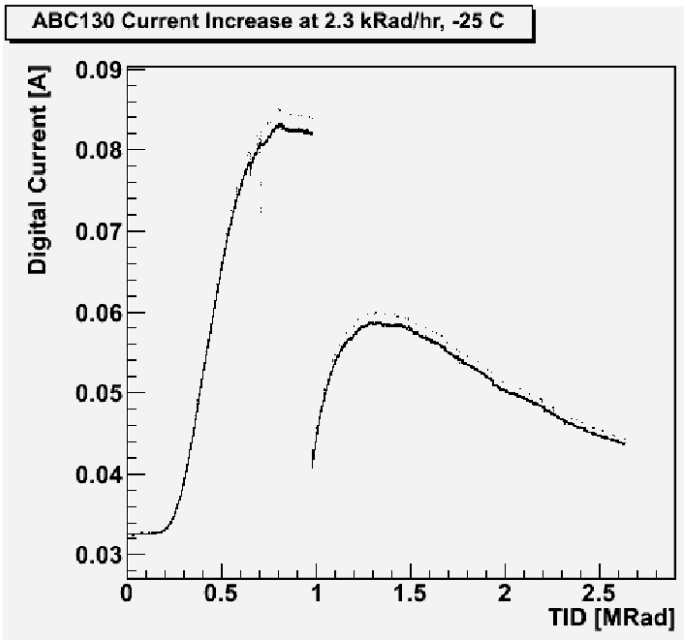

Figure 7.44. Digital current as a function of TID for an x-ray irradiation at 2.3krad/h at -25 C°. to be replaced by high better quality fig.[IMG]

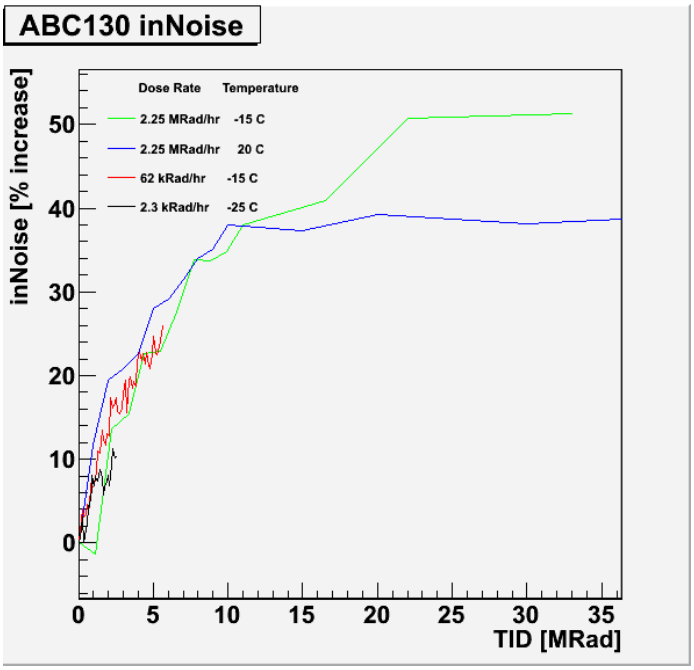

Figure 7.45. Percentage increased of input noise as a function of TID, for different dose rates and temperatures. to be replaced by high better quality fig.[IMG]

2540 over 7 days. Both ABC130single chip card and hybrids with three ABC130ASICS and a HCChave been tested. To perform the tests the chip configuration was set before the spill, data are read back by triggering on the spill, and at the end a reset was performed. The measured SEU cross

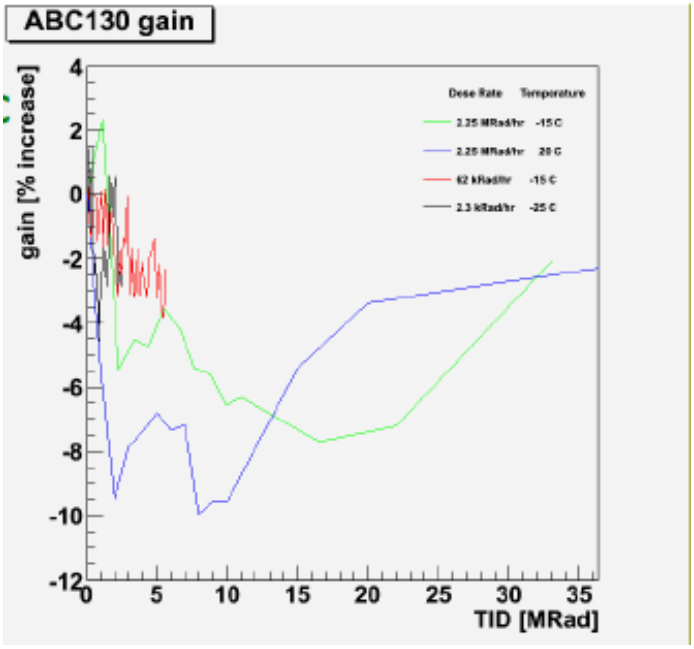

Figure 7.46. Percentage gain decrease as a function of TID, for different dose rates and temperatures. to be replaced by high better quality fig.[IMG]

section is ˜5x10ˆ-14 cm2 for memory banks (Figure 7.47a), 1 to 5x10ˆ-14 cm2 for unprotected logic (Figure 7.47b), and <5x10ˆ-16 cm2 for registers with triplicated logic (Figure 7.47c).

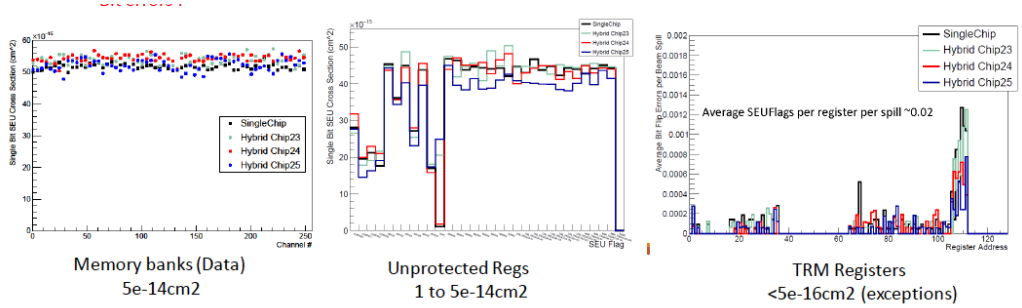

Figure 7.47. SEU cross section for (a) memory banks, (b) unprotected registers, (c) TRM registers. to be replaced by high better quality fig.[IMG]

ABC130⋆specifications

The ABC130⋆chip will be the front-end ASIC for the readout of the ITk Silicon Strips detector in the ATLAS experiment for the HL_LHC collider at CERN (ref. 12). It will be fabricated in Global Foundry (Ex-IBM foundry) in the CMOS8RF_DM 130 nm technology. The wafers are standard eight inches and will be thinned to 200-320 μm. The chip will be 7.9 mm wide to best fit the input pads to the sensor strip pitch, while keeping a reasonable gap between adjacent chips to allow the placement of decoupling capacitors. The maximum length is set to 6.8 mm.

The ABC130⋆ASIC will provide all functions required for processing of signals from 256 strips of a silicon strip detector in the ATLAS experiment employing a binary readout. The ar-

chitecture chosen for the ABCStar allows a multi-trigger data flow control retaining the Beam Crossing synchronous pipeline transfer signal (L0 here) from previous versions, an asynchronous Regional Readout Request (PR here) and a second level asynchronous data readout intended for a global readout (LP here). The design can be easily adapted to a single level readout (L0 readout mode) simply by not sending priority triggers. The simplified block diagram of the chip is shown in Figure 7.48. The main functional blocks are: front-end including threshold and calibration controls, power regulation, command decoder, Mask and Edge Detection, L0Buffer, EvtBuffer, Cluster Finder and Readout logic. The "Top_Logic" block controls the data path by interpreting the PR and LP trigger signals.

The front-end is optimised for 2.5 cm strips with 25 ns shaping time, and a noise level below 1000 electrons after full radiation effects. Resistive feedback and ELTis this ever defined somewhere ???[MS] NMOS transistors are used to improve noise performance before and after irradiation. The discriminator level should be lower than 1fC, possibly reaching 0.5 fC. After discrimination, at each bunch crossing the binary outputs of the front-end channels are sampled and stored into the L0Buffer for a duration fixed by the (programmable) latency for receiving the L0 signal.

This part will need to be changed once the L0 tag scheme is fixed.

At each L0 reception the event with the correct latency is transferred to the EvtBuffer. It is maintained for an average duration corresponding to 128 L0 (128 us at 1MHz L0 rate) and tagged with an appropriate identification number (L0ID). If a PR or LP signals are received with the corresponding L0ID number, the event is processed through the Cluster Finder (CF). The CF block acts as a data reduction circuit, creating a "cluster" byte for channels found with hits. The expected average occupancy is of 2 [4 in case of 5cm strips] clusters per event. The Readout block creates formatted packets with the event identification and the associated cluster bytes. The data are transmitted serially at 160Mb/s.

The Command Decoder block receives and distributes internally the trigger signals (L0, PR, LP). The serial command (CMD) input is used for the chip configuration instructions (including resets), the analogue bias settings, the mask and test and calibration settings, the register readback functions. Two additional signals (L0sync/BCRs) are proposed to perform real time Bunch Crossing and Event numbers resets.

The Top Logic block is the autonomous sequencer that controls the data flow path according to the arrival of the L0, PR, LP trigger signals.

References: Don't worry about the references - Daniel Rauch will sort them[IMG]

1- ABC130 specifications, version 4.6, fix URL here...

2- N. Lehman, Tracking with self-seeded Trigger for High Luminosity LHC , Master Thesis, Section of Electrical and Electronical Engineering, ÃL'cole Polytechnique FÃl'dÃl'rale de Lausanne, August 15 2014

3- F. Faccio and G. Cervelli, "Radiation induced edge effects in deep submicron CMOS technology", IEEE Trans Nucl. Science, Vol.52, Dec 2005, pp. 2413-2420

4- F. Faccio et al., "Total Ionizing dose effects in shallow trench isolation oxides", Microelectronics Reliability 48 (2008) 1000-1007

5- N. Quirk, R. Teuscher, N. Venturi, K. Cormier, "ABC130 ASIC Total Ionizing Dose Testing for the Phase-II Upgrade of the ATLAS Semiconductor Tracker", ATL-COM-UPGRADE-2016-

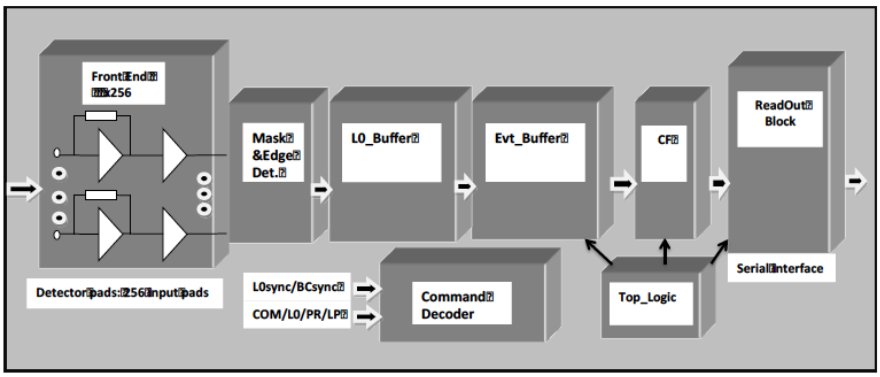

Figure 3-1 Block diagram of the ABCStar chip.

Figure 7.48. Block diagram of the ABC130⋆chip. to be replaced by high better quality fig.[IMG]

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6- Valerio Re et al., Total Ionizing Dose Effects on the Noise Performances of a 0.13um CMOS Technology, IEEE Trans Nucl. Science, Vol. 53, No. 3, June 2006

7- Valerio Re et al., Review of radiation effects leading to noise performance degradation in 100 - nm scale microelectronic technologies, 2008 NSS Conference Report

8- Xing J. Zhou et al., Radiation Effects on the 1/f Noise of Field-Oxide Field Effect Transistors, IEEE Trans Nucl. Science, Vol. 55, No. 6, December 2008

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7.3 The Hybrid Control Chip HCC130

Paul Keener working on the text[IMG]

The Hybrid Controller Chip (HCC) is the interface ASIC between the signalling on the stave and the analog front-end ASICs (the ABCs) on the hybrid. There is one HCC per hybrid, two per module.

The HCC has stave-side inputs for the bunch crossing clock and control signals. These control signals include triggering and general commands. After processing in the HCC, the control signals are sent on a hybrid-side bus to the ABCs.

Any data being returned from the ABCs is sent through the HCC, where they are queued and sent out on the data line on the stave.

The current version of the HCC is the HCC130. The data connections from the ABCs are in the form of two bidirectional loops. In the barrel, each loop has 5 ABCs. In the end-cap, the loops vary between XXX and YYY ABCs. The data handling in the HCC130 is very minimal: it adds a header to ABC data packets and sends them on.

The HCChas been fabricated in the Global Foundries 130nm process. It has three LVDS inputs for its control lines: a 40 MHz clock, a 80 Mbps line shared by the L0 trigger and Commands, and

a 80 Mbps line shared by the R3 and L1 triggers. The two 80 Mbps lines are configured so that one signal (CMD and L1) are sent with the high phase of the 40 MHz clock and the other signal (L0 and R3) are sent with the low phase of the clock.

The 40 MHz clock is used as the reference for a phase lock loop (PLL) that generates several 160 and 320 MHz clocks that are used throughout the HCC. The PLL also makes available a stabilised 40 MHz clock. One of the 160 MHz clocks is used to generate an 80 MHz clock, with deterministic phase with respect to the 40 MHz reference clock. Either the original 40 MHz clock or the PLL 40 MHz is bussed to the ABC130on the hybrid side.

On entering the HCC, the L0 and Command signals are de-multiplexed. The L0 signal is passed through the HCCwith minimal, fixed, delay and is re-multiplexed with any Command stream being sent to the ABC130. Commands to the front-end are either global, with no addressing, or specific to a given ABC130or HCC. The specific commands have the hardware address of the HCC on the addressed hybrid. The HCCwill filter out any ABC130command that does not not have its hardware address. All global commands, and those ABC130commands that are for ABC130s on this hybrid and re-multiplex with the L0 signal and sent out on the hybrid bus.

The multiplexed R3-L1 line is treated similarly to the L0-CMD line. The L1 signals are past through, while the R3 signals are processed. The R3 signal contains a 14-bit, unary encoded, value to indicate which modules are to respond to the R3 request. The HCCuses its hardware address to determinate whether its module should respond to the R3. If it determines that it should respond, a shortened form of the R3, called R3s, is generated. The R3s and L1 signals are re-multiplexed and sent out on the hybrid bus. The HCCsends a clock on the hybrid bus that is used by the ABC130s to send data back to the HCC. This clock can be selected to be either 80 or 160 MHz.

There are four inputs from the ABC130s to the HCC. Two of these are the endpoints of one loop and the other two are the endpoints of the second loop. Depending on the configuration of the ABC130s in the readout loops, data will arrive on any number of the four inputs. There are flow control signals from the HCCto the end ABC130s that indicate whether data can be sent to the HCC.

Data from the ABC130inputs have an HCCheader added to them and are combined with a data flow from HCCregister reads and the HCC high priority packet flow in a priority-based system. The HCC can output packets at 80, 160, or 320 Mbps. In one case, the data are taken from a single ABC130loop, plus the HCCdata and send out. This supports output rates of 80 and 160 Mbps. In the other case, the data from the two loops are multiplexed bit by bit on the output. This mode supports output rates of 160 and 320 Mbps. In both cases, the lower output rate corresponds to an ABC130to HCCdata rate of 80 Mbps and the high rate corresponds to an ABC to HCC data rate of 160 Mbps.

All of the hybrid side signals, both inputs and outputs, can be delayed over a range greater than one cycle time with a small step size.

The HCCalso contains blocks for monitoring the PLL and for making autonomous analog measurements of various quantities including raw and regulated voltages, on- and off- chip temperatures, and high voltage current. This monitor also has to capability to individually interlock four separate output signals.

7.3.1 HCCTesting

Functional Testing:

- Die probe tests
- Parametric tests

Radiation Tests:

- Birmingham
- PS

7.3.2 HCC⋆

A lot of the HCCStar isn't well defined because the exact requirements aren't known yet.

The HCC⋆will be fabricated in the Global Foundries 130nm process. A number of the analog blocks with be reused from the HCC, in particular the PLL and delay blocks. The drivers and receivers will be modified versions of ones in the HCC. The HCC⋆is divided into three major sections: the control path, the input channel and the packet builder/serialiser.

Control Path:
The control path takes the clock and control signals from the stave, decodes them, performs processing on them as needed and sends them on the hybrid bus to the ABCs. A lot of the details are not yet known, including incoming data rates, data encoding, protocol etc. It is likely that the clock will be 40 MHz. There probably will be two control lines, at least one of which will run at 160 Mbps with the other running at a rate of at least 80 Mbps. An encoding such as 6b/8b is under discussion.

The L0 trigger decisions for some number of bunch crossings – likely four or five – will be collected and sent together, along with a tag composed of the low order bits of the L0ID. This tag will be interpreted as the L0ID of the first L0 trigger accept. Subsequent L0 accepts will have L0IDs incremented from the first. The input channel will decode the L0 trigger information for its own bookkeeping and will forward the command stream, unmodified, to the ABCs, perhaps after multiplexing it and encoding it.

The processing of the commands – register reads and writes, specific chip resets, etc – is similar to the process in the HCC, where only commands intended for an ABC130on the hybrid where the HCC is located are forwarded intact to the hybrid bus. Because of the encoding and entanglement with the L0 trigger stream, it may be required to modify the command stream if it is not applicable rather than not forwarded it at all.

The L1 readout request stream is decoded by the HCC and enqueued as a Low Priority (LP) request in the control path. The R3 readout request is processed as in the HCC130, and if applicable, the shortened request is enqueued as a PRiority (PR) request. The HCC⋆will have an L0-only

readout mode. In this mode, an L0 accept will automatically generate an LP request and enqueue it to be sent to the ABCs.

Because there is no flow control on ABC data coming into the HCC's input channel, the HCC must control readout requests so that its input buffer to not overrun. This is achieved by a block that takes the buffer occupancies of the input channels and implements a readout request dispatch policy.

Input Channel

The HCC⋆has 11 input channels that accept data packets from ABC130⋆chips, one input channel per ABC. These data packets can contain event data, from either an LP or PR request; or register data from a register read command.

The input channel deseriallises the data coming from the ABC, performs some validity checks on that data and separates it based on its type. Event data are stored in a 64 wide by 128 deep SRAM block that is divided in two. The lower half of the memory, with most significant bit of the address being zero, is used to store the data retrieved from a PR request, while the upper half, with the most significant bit of the address being one, is used to store the data retrieved form an LP request.

Data from a register read command is stored in a small (4 deep) standard cell FIFO.

Packet builder/serialiser:

to be added later

7.4 FEAST and upFeast

Laura provided this text[IMG]

The chosen powering scheme for the ITk strip modules is based on the distribution of power through on-detector DC-DC converter modules developed by the CERN PH-ESE group reference to Ref 1. and 2 below. The module is built around a buck converter ASIC, the FEAST chip, embedding both the power switches and the control circuitry. A number of ASIC prototype DC-DC converters have been developed to reach the required performance, with particular emphasis on radiation tolerance and efficiency. The latest version of the FEAST chip, the FEAST 2.1 provides output voltages in the range of 0.6 to 5V from an input voltage between 5 and 12 V. The output current can be as high as 4 A. The switching frequency can be adjusted in the range 1-3 MHz. Operation at 1.8 MHz operation is the default configuration as it allows for reduced conductive noise. The chip proved to be radiation tolerant to TID up to $>$ 200Mrad, and displacement damage up to 5x10^{14} n_{eq}/cm^2 . SEE tests showed continuous operation during exposure to heavy ions of Linear Energy Transfer (LET) up to 64 MeVcm^{2}mg$-$1 with short transients below 20 % of the nominal V_{out} (no destructive event, no output power interruption). The FEAST2 design is being ported to a different 0.35 μm technology that can stand much higher fluence. The new chip upFEAST is expected to stand displacement damage up to 5x10^{1}5 n_{eq}/cm^2 The DC-DC converter modules features a custom toroidal air-core inductor needed to cope with the high magnetic field in the experiment. The layout of the module, as well as its SMD components, have been chosen to minimise the emitted noise (conducted and radiated).

References [1] http://project-dcdc.web.cern.ch/project-dcdc/Default.html [2] A.Affolder et al., "DC-DC converters with reduced mass for trackers at the HL-LHC", Journal of Instrumentation, Vol.6, November 2011(C11035)

7.4.1 AMAC

The following was written by Mitch - I think it needs to be slightly shortened[IMG]

The Autonomous Monitor and Control Chip (AMAC) monitors voltages, temperatures and sensor bias current on strips modules at a rate of approximately one sample per millisecond. The ADC full scale range is from 0 V to 1 V 1 mV/cnt (10 bit range). The gain in V/cnt can be adjusted by $\pm$20%. The gain for voltage values with ranges expected to be larger than 1 V will be ratioed by a resistor divider or operation amplifier (opamp) determined ratio. AMAC will be programmed and readout through the lpGBTxperipheral interface (see Chapter XX) , planned to be a standard I2C interface reference needed [IMG]. A possible noise and offset mitigation will be discussed with the lpGBTxgroup that will provide for a two line uni-directional differential ""LVDS like"" interface using most of the I^2Cprotocol.

AMAC provides a structure for interrupt servicing or direct interlock functionality through dedicated outputs with CMOS (1.2 V) logic levels. These outputs may be programmed to change state when measured values exceed programmable upper and lower limits on mask enabled sensed values. The ASIC also provides a clocked digital output to control used as a charge the gate voltage on a high voltage FET intended to ""switch"" bias potential “on” and “off” the silicon sensor. Since the logic levels for this output may be set as high as 3 V AMAC will have a separate supply rail for this clocked HV output.

AMAC Monitoring operation: Abstract description: The basic components of the AMAC monitor are: A ring oscillator clock divided down and connected to both a counter and a reference voltage ramp generator. A series of comparators (one for each sensed voltage) that send a write signal to record the counter value when the ramp voltage exceeds the sensed voltage. Detailed description: AMAC monitoring is driven by an internal ring oscillator that utilises standard gates and passive elements, a resistor and capacitor, appended to each gate output in the ring oscillator to determine the inter element delay. The combined uncertainty in the passive elements is $\pm$10% versus the inverter variation over process which can be more like a factor of two. The ring oscillator frequency is expected to vary between 35 and 40 MHz. A similar frequency to that of the BX, beam crossing clock previously used in HCC for the autonomous monitor input. This clock is divided by a factor of 48 to yield a counting rate for an integrating ramp ADC and counter of $\sim$ .75 MHz. Measurements are nearly insensitive to the clock rate since units of charge deposited on an integrating capacitor are what is counted. The integrator unit charge is determined by the reference voltage (100 mV programmable $\pm$20%) switched onto a 100 fF $\pm$10% unit charge capacitor which is then, by use of switches commuted to the input of an opamp driven integrating DAC. The 10 pF integrating capacitor sets the voltage gain of 1/100 so that one unit of charge dumped onto the integrating capacitor increases the DAC voltage by 1 mV typically. Since the unit charge capacitor and the integrating capacitor are fabricated from the same material the uncertainties in the gain are determined by the rationing accuracy of about 1 % and by the voltage on the band gap reference. One issue that may arise is that the FET based band gap is chosen for its radiation tolerance but has an uncertain absolute band gap compared to diode based band gaps that are somewhat radiation

sensitive. The clock driven integrator provides a ramp with 1024, nearly 1 mV steps. A counter keeps track of the number of charge units dumped into the integrator. The integrator provides a reference voltage ramp for comparators monitoring the various sensed voltages. There is one comparator for each sensed voltage and one storage register to hold the counter value registered when the integrator ramp exceeds the monitored voltage for two successive counts. The recorded value is compared with the programmed upper and lower limits and a flag is set if the recorded number exceeds either of these values. If enabled by a mask bit this will result in an AMAC output voltage changing state. This provides a dedicated output that may be attached directly to a supply regulator enable bit or act as an interlock or it may be attached to an input of HCC*. This approach offers a simple, low power technique to independently monitor an arbitrary number of voltages at a 1millisecond sampling rate since each channel requires only a comparator, counter, two limit registers and a mask bit.

Interrupt Functionality: Interrupt functionality offers the possibility to eliminate digital polling activity on the I2C lines by providing a CMOS logic level on a dedicated Look At Me (LAM) line to the HCC*. When enabled the LAM input to the HCCcould be used to raise a flag bit in the HCC*output packet indicating to the upstream DCS that the AMAC associated with the HCC with the flag bit high has a value out of range. With this module specific information the I2C associated with that module could be polled for out of range values on a particular module.

Monitored Quantities:

- AMAC raw input voltage 3/5 mV /cnt
- AMAC band gap voltage 1 mV/cnt
- Sensor Bias current. Range for 4 gain settings 0.01 uA to 5 mA
- NTC thermistor Temperature Off chip Resolution .5°C or higher
- Internal diode based voltage $\sim$ 1.5 cnts/°C Relative to known value. This is not an absolute precise value without calibration.
- External Sense voltages (2-3) available

The total number of monitored quantities are yet to be determined.by when ?[IMG]

8. Silicon Strips Modules – Production Steps

Editor: Marcel Stanitzki
Chaser: Ingrid-Maria Gregor, Ingo Bloch
Number of pages to write: 20

In the following sections the production steps for a full module are summarised. The chapter concludes with an overview of the planned quality assurance and quality control measures during the production.

8.1 Hybrid Design and Prototypes

provided by Ash and Kambiz[IMG]

For the short barrel module, there is a requirement for either one or two hybrids to serve a single silicon sensor with ten ABC130⋆per hybrid. The electrical design of both hybrids is identical with their only difference being geometric. Electrically, the hybrid provides:

- A single power and ground domain for all ASICs on the hybrid.
- The connection of external clock and control to the Hybrid Controller Chip (HCC).
- Distribution of on-board clock and control to the front-end readout ASICs (ABC130).
- The return of multiplexed high speed (up to 640 Mbs) module data to the EOS.

Due to the large number of circuits required and to ensure maximal yield the design of the circuits has not pushed the boundaries regarding the design rules of the manufacturer; the track and gap geometry is $\sim$ 100 μm with laser drilled vias (plated-through-hole) of 150 μm hole diameter and lands of 350 μm, to maintain uniform plating and hence reliability of the via. The circuits are constructed using 50 μm polyimide dielectrics with copper conductor thicknesses of 18 μm The current prototype ABC130 barrel hybrids utilise three copper layers which results in a circuit build thickness of 300 μm. They are laser profiled with the width coming in at 15.5 mm at the narrowest point and increasing to 17.0 mm at the widest (for approximately 20% of the overall length). The design and the layout of the hybrid has been optimised to meet the expected module noise performance whilst maintaining signal integrity of the high speed differential signals that propagate on the hybrid. Low noise performance has been achieved by the use of a single ground plane, partitioned into analogue and digital sections with no mixing of analogue and digital signals. The use of a low impedance ground plane ensures that the high frequency digital return currents will return directly underneath their signal traces and thus not corrupting the front-end analogue signals.

Furthermore, digital signals that do run close to the sensitive front-end of the readout ASICs have been routed as differential strip line (sandwiched between ground planes top and bottom) which has the benefit of shielding the digital signals and thus resulting in lower emissions and crosstalk. The ABC130hybrid topology is based on a daisy-chain readout with two groups of five ABC130⋆, with bi-directional data readout, connecting up to a Hybrid Controller Chip (HCC). This architecture results in up to four data paths into a HCC of which normally only two would be active to service the two groups of ABC130s. This topology is shown in Figure 8.49, showing

both flavours of hybrid layout, referred to as Left-Handed and Right-Handed and pictorially their readout topology.

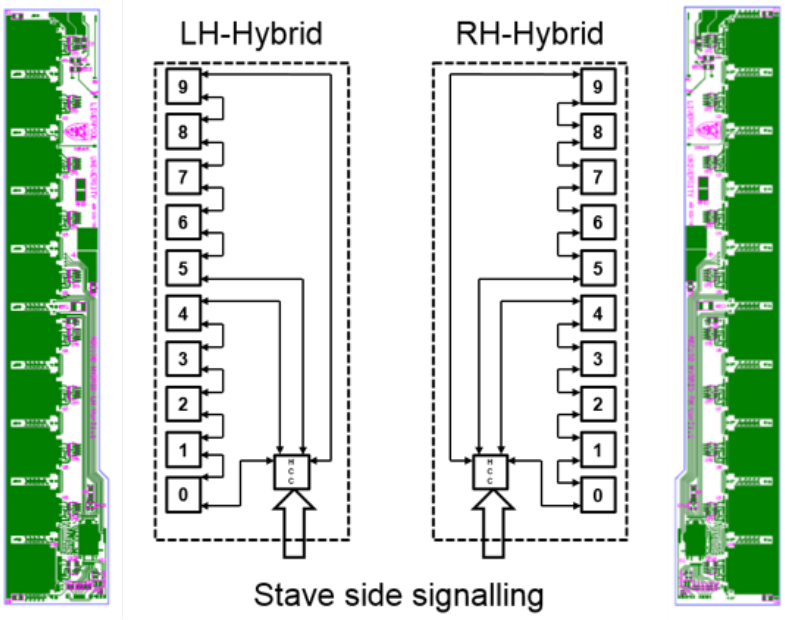


Figure 8.49. Barrel readout topology showing ten readout ASICs connected to a Hybrid Controller Chip

Hybrids come equipped with two NTC thermistors of which one will be used during its operational life to allow monitoring of the hybrid temperature and a second sacrificial thermistor. The sacrificial thermistor being used to form part of a temperature interlock system during the construction phase of both hybrids and modules. Once installed onto a stave this thermistor becomes redundant and is no longer accessible.

Due to the nature of the module construction whereby there is no substrate between the hybrid and sensor and coupled with the large number of circuits required; a panellised hybrid solution has been adopted. This is made up of two parts with the flexible hybrid circuits being selectively attached to a rigid FR4 former to provide mechanical support during their build and testing phase. The panelisation provides for:

- Eight hybrids within a panel, four of each flavour (left-handed and right-handed).
- Hybrids are assembled in-situ with both SMDs and ASICs being attached to the circuits.
- The rigid former and vacuum holes, underneath the ASICs, providing suitable mechanical support for the Al wedge wire-bonding of the bare die in-situ.
- Provision of trace routing, external to the hybrids, supplying both power and digital I/O. This enables the testing of the circuits whilst still resident on a panel. With the connections being brought to dedicated power and digital I/O connectors.

The panels also come equipped with two test coupons, one at each end of a panel. Their construction and attachment to the panel is identical to that of the hybrids, they will form an important part of the module QC with embedded test structures which will allow for the:

- Testing of vias by the use of multiple via chains and low-Ohmic resistive testing.
- Checking of trace etching quality by the use of multiple "long" traces on differing layers of minimal width (100μm), testing for their DC resistance.
- Addition of multiple bond pads, distributed longitudinally along the coupon. Providing for both visual and wire-bond pull strength evaluation.

Panel, hybrids and test coupons have provision for a Radio Frequency Identification (RFID) tag to be attached, Ref: MuRata LXMS31ACNA-010, this provides a 240-bit unique device ID and 512-bits of user accessible memory. It is foreseen that this will be integrated into the database to allow ease of tracking of the components at their differing construction phases. As mentioned previously, the hybrids and test coupons are selectively attached to the panels, they are retained by "shaped" tabs which are required to ensure that there is no geometrical distortion encountered during the high temperature solder re-flow process of the SMD attachment. Once a hybrid has been through its full construction phase of having SMDs and ASICs attached followed by wire-bonding and testing they can then be released from the panel by the cutting of these retaining tabs.

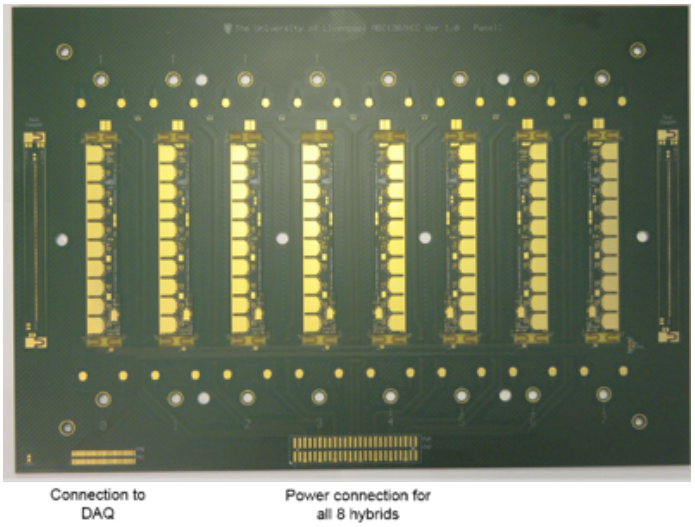


Figure 8.50. ABC130 Prototype Panel

An example of a prototype ABC130panel is shown in Figure 8.50. The eight hybrids of both flavours can be seen plus the two test coupons towards the ends of the panel. Whilst Figure, below, shows an example of both a test coupon and Left-Handed flavour hybrid. The photograph clearly showing the tabs used to retain the circuits within the panel.

8.1.1 End-cap Hybrid

The end-cap readout system is electrically identical to that of the barrel region, utilising the same front-end ASICs and infrastructures. Due to the higher multiplicity - both in sensor size and in strip pitch/length - of the end-cap modules there are more flavours of the hybrids than in the barrel. The geometrical diversity of the end-cap sensors in radial direction dictates the varying shapes and sizes of the end-cap hybrids. The number of ABC130and HCC ASICs on each hybrid varies accordingly. A tabular overview of the hybrids and the readout chip-set multiplicity is reproduced in table XY.

add table here ?? or just give reference to table in overview section[IMG]

The end-cap hybrids are four layer polyamide based flexible circuits designed and fabricated based on the industry standard HDI design rules similar to that of the barrel hybrids. These are laser cut to single pieces. Only filled and plugged laser drilled blind micro-vias are used in the design. Thru-hole vias, i.e. L1-L4 vias, are implemented utilising staggered, e.g. L1-L3 followed by L3-L4 with a short offset on L3L0 etc. is irritating as this is also used for the trigger and the barrel layers.[IMG], blind vias in order to avoid problems in the lamination phase of the manufacturing process. The overall thickness of the hybrids is about 300 μm. The hybrids are fabricated with an Al-wire bondable ENIG (Electroless Nickel Immersion Gold) surface finish. Apart from tight real estate on hybrids in some regions of the end-cap, the routing goal has been primarily the signal and power integrity. Figure **??** sketches of the R0 to R5 hybrids mounted on their corresponding sensors. R0, R1, R3, R4 and R5 hybrids are all manufactured. R2 is being designed and due production soon. The red and yellow boxes in these sketches represents the ABC130nm and the HCC ASICs respectively. Notice in the case of the R3 to R5 hybrids the segmentation across the sensor halves boundaries and the number of the HCC chips. Wire bond links provide electrical connection of the two hybrid segments. Each HCC is routed independently and readouts one half of the hybrid. The HCCs are mounted close to the left edge of the hybrids in order to avoid long stubs on the data and TTC links to and from HCCs, so as not to degrade signal integrity. As in the case of the barrel, in order to speed up testing in larger volume production phase, a panellised approach for future hybrid manufacturing is envisaged. A prototype R0 panel has already been designed to be submitted for production soon. A sketch of the final design of the flexible electrical and the rigid stiffener is shown on figure XZ.

8.2 Power Board

The baseline powering scheme adopted for the ITk strip tracker modules is DC-DC. This powering scheme has to be both radiation tolerant and provide all the necessary power to the front-end readout ASICs and auxiliary on-detector electronics used for monitoring, control and sensor HV biasing. Due to the geometrical constraints primarily associated with the barrel type modules, the power board is attached to the silicon strip sensor. This places severe limitations to the size of the board and the envelope it can accommodate whilst requiring its operation not to be detrimental to the module's expected noise performance.

The board provides the following functions:

- Power for the front-end readout ASICs, nominally 1.5 V/4.0 A (max).

- The TID contribution, could increase the current to 6.5A (max) for EndCap modules.
- Localised DCS, providing the monitoring of module front-end ASICs and DCDC converter voltages and currents and both hybrid and DC-DCconverter temperatures.
- Switchable sensor HV bias and filtering with sensor current monitoring capability.
- The power board's control, configuration and DCS monitoring will be independent of the module data links, instead utilising a multi-drop I2C link connected to LpGBTX.
- The DCS monitoring can operate in an autonomous mode providing a module level interlock in case of the risk of over temperature, voltage or current situations arising. This can operate independently of the user or can be over-ridden.
- Both DCS monitoring and sensor biasing are powered independently of the hybrid front-end ASICs. The decoupling of these powering domains allows the monitoring of both hybrid temperatures and the silicon sensor leakage currents prior to the module being fully powered. This feature allows the module to be placed into a low power mode with minimal power dissipation. When a module is configured in this mode, the hybrid temperatures will be representative of the cooling circuit embedded within the core and that of the silicon sensor. Providing a more precise measurement of the sensor leakage current and thus enhancing the monitoring of radiation damage to the sensors.

The integration of module powering, HV sensor switching and monitoring has been realised in a "stand-alone" circuit board, currently manufactured in a "thin-build" FR4 of approximately 0.5mm thickness. The future final circuit being built in flexible copper-polyamide technology. A single board is able to provide power for all types of barrel and end-cap modules prior to irradiation. The design has been optimised for low noise and attenuation of EMI emissions to ensure the necessary required noise performance of the module.

Irrespective of the module type, be it barrel or end-cap, the core functionality of the power board is identical. The difference in the boards being geometrical to enable their matching up to the differing module and bus tape geometries. The topology of the board can be segmented into four groups:

- Silicon sensor HV bias filtering circuit.
- Sensor bias HV switch. reference chapter
- Control and monitoring via the AMAC ASIC.reference chapter
- DC-DCPower Block using the radiation tolerant buck converter, upFEAST ASIC.reference chapter

A prototype barrel module type power board is shown in Figure 8.51 highlighting its functional blocks, also clearly shown are the coil, required for the DC-DCbuck converter, and prototype shield box in the background.

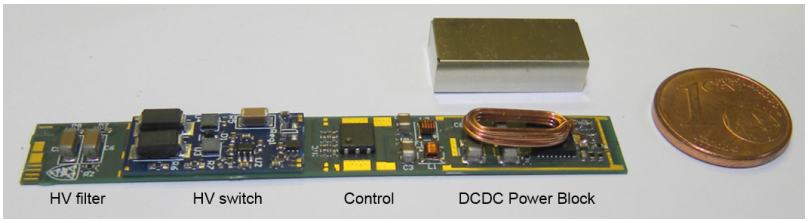


Figure 8.51. Prototype Barrel Power Board with coil and prototype shield box in the background

The use of a DC-DCbuck converter and its associated EMI emissions and given its close proximity to both the silicon strip sensor and front-end readout ASICs, makes it imperative for a shielding solution with low mass to be adopted. This is further complicated by constraints in both the height and width making it difficult to fit a toroidal coil of the nominal inductance, this type of coil would normally be the preferred choice due to its low electric and magnetic field emissions; instead a solenoidal "flat type" coil was chosen (REF 7,x). The shielding of the high EMI part of the DC-DCpower block has been achieved whilst maintain low mass by using a mixed material solution of aluminium and copper to form a shield box. The combination of the shield box and shield layer on the power board, both referenced to local Ground, provide a Faraday cage enclosure thereby mitigating electric field emissions from the DC-DCpower block. The shielding of the magnetic field is realised by eddy current cancellation; this exploits the solenoidal coil geometry whereby the time varying magnetic field, incident to the shield box, gives rise to an induced current in the shield box producing a magnetic field in opposition to the incident (aggressive) one. Although advantageous in the shielding of magnetic fields a disadvantage of this technique is that it attenuates the converters coil inductance and thereby lowering both the efficiency of the converter and increasing the conducted noise at the output (when compared to operation in free space). By maintaining a minimum coil-to-shield distance of >1.5mm the impact on the coil inductance is at the level of 5% reduction (see Chapter REF 7.x). The combination of having to maintain shield box clearance and the physical height of the electronic components plus coil within the volume determines the actual height of the shield box, this is currently 4.8 mm.

This has been shown to work very well in the attenuation of both electric and magnetic fields and thus minimising noise pick-up into the module whilst still maintaining a target efficiency of 75% at the nominal load of ˜2A.

8.3 Module Production Steps

Compared to the module production of the ATLAS SCT the number of steps in the assembly and bonding of a module were reduced and thus production throughput and time of the quality assurance chain should be manageable. Within the module, location precisions between the ASICs, bare hybrids and sensors are much more relaxed as it is set by what is wire bondable ($\sim$200 μm); the high precision action is the attachment of the modules to the stave cores (see Chapter 10). As such, all ASICs can be placed relative to their cut edges simultaneously using custom vacuum tools, which easily meet the needed precision. In addition, systems using dowel pins for module assembly can be utilised, which can be mass-produced cheaply. The detailed production steps are

discussed in the following at the example of a barrel short strip module. Differences for the end-cap module are summarised.

8.3.1 ASIC to Hybrid Gluing

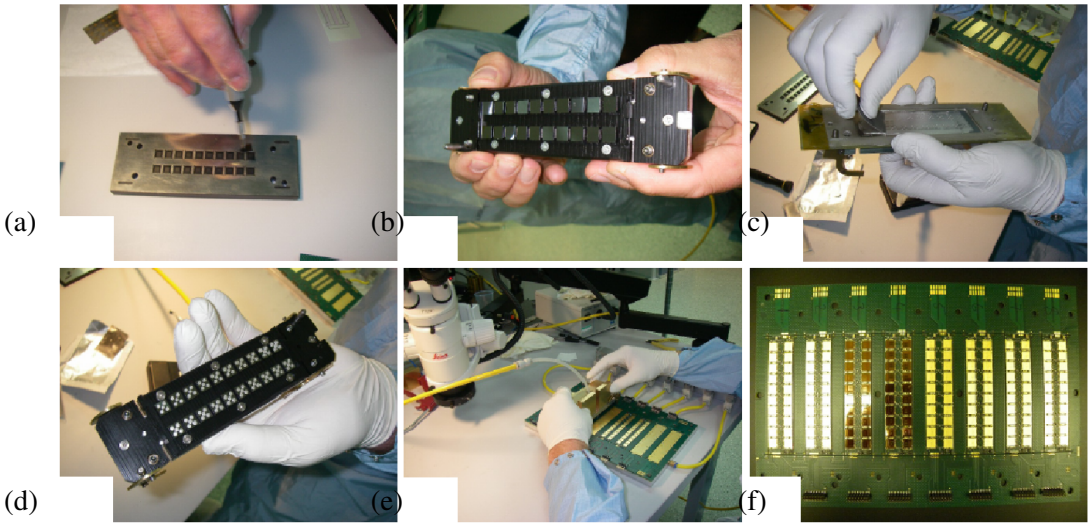


Figure 8.52. Six steps to glue ASICs to the hybrid carrier. Once wire bonded, the final hybrid is tested in the frame shown on the lower right. New photos will be made.[IMG]

The details of the ASIC to hybrid gluing process are depicted in Fig. 8.52. Several tools are used for this process. Initially chips are aligned in a mask made up of a precision, laser-cut stencil and plastic tray, as shown in Fig. 8.52 a. After being picked up with a vacuum pickup tool, as shown on Figure 8.52 b, the UV glue (Dymax 6-621 or Loctite 3535) is distributed onto the ASIC pads.with a automatic dispensing robot to dispense 2 ml of glue in a 5 dot pattern. Figure 8.52 d shows the resulting glue spots. As the last gluing step, the chips are lowered onto the hybrid. The x-y alignment is set by precision holes in the hybrid panel and pins in the pickup tool. The glue thickness of 80 μm is set by four precision jacks in the pickup tool referenced to the ASIC locations by four landing pads on the panel. A brass weight is placed on top of the bridge tool to ensure the tool is held down securely. LEDs integrated on the upper side of the tool inform that the touchdown is correct and UV LEDs within the tool are used to cure the glue. A curing time of 5 minutes is used. This procedure is repeated for each of the eight hybrids on one hybrid panel. Glue heights across the panel can be controlled using a SmartScope metrology system to check that the hybrids are within acceptable limits (see section 8.6.3). The HCC for each hybrid is placed by hand using TRADUCT silver epoxy glue and the full panel is left to cure overnight in an oven at what temperature ??. After the glue has cured, the chips are wire bonded to the hybrid, followed by a burn in and a set of electrical qualification tests of the final object (see section 8.6.6).

8.3.2 Hybrids and Power Board to Sensors

The hybrid to sensor gluing process is depicted in Figure 8.53. Several further tools are used for this process. Electronics grade epoxy (fuller Epolite 5313) is applied to the back side of the hybrids using a second 200 μm thick, laser cut glue stencil mask, shown on Figure 8.53 a. The hybrids are

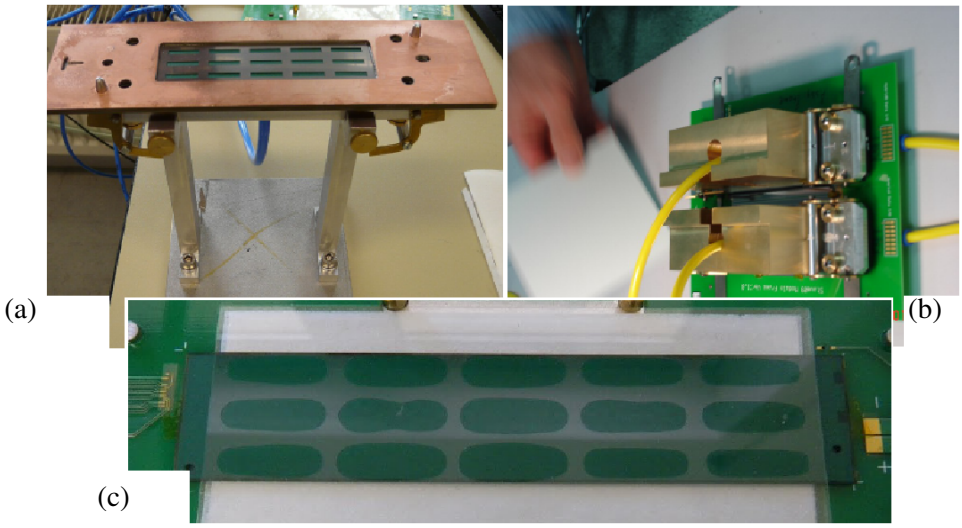


Figure 8.53. Gluing the hybrids to the sensors. New photos will be made.[IMG]

placed onto the sensor using the same vacuum pickup tools as used for the ASIC to hybrid gluing and left weighted down to set for another 6-12 hours. The hybrid placement in x-y is set by pins in the pickup tool locating into holes in the module assembly plate. The final 120 μm glue thickness is set by the four jacks in the pickup tool landing of ground pedestals on the assembly jig. The targeted glue coverage of $\sim$60% allows for the variation of the hybrid's and applied glue layer's thicknesses and of the hybrid's flatness, while still supporting the relevant areas for wire bonding and ASIC cooling. An example of the resulting glue spots is shown (using a glass sensor dummy) in Figure 8.53. After the glue has set, the power board is glued (also Epolite 5313) directly to the sensor as well. Afterwards the readout pads of the ASICs are connected to the strip pads and further electrical quality control steps are performed.

8.3.3 End-Cap Specific Details

The above steps apply generally to barrel and end-cap modules although all pictures shown are of the barrel module tools. In the case of the end-cap, the same procedure is used however tools and hybrids are arced to take into account the radial nature of the strips. One additional complication in the end-cap however is that the R4 and R5 modules are pairs of modules made up of two sensors and two hybrids which are stitched together by wire-bonds. In this case, the module with the HCCs attached is tested first and if this is successful the second module is brought in and the stitch wire-bonds added before further testing of the completed module pair.

8.4 Justification of choice of materials

currently this is only on glue. Other materials need to be mentioned as well.[IMG]

8.4.1 Selection of glues

Effort has been put into qualifying an alternative, UV-curable glue to be used instead to benefit from much faster curing times and lower costs. Figure 8.54 depicts the noise levels of hybrids

manufactured using silver-epoxy and UV-curable glue in comparison, averaging the noise over all channels of a given ASIC. Several measurements at different times, temperatures and humidity levels have been taken, leading to a few data points per chip, again overlapping within a range of ± 10 ENC. Both, silver-epoxy and UV-glue hybrids exhibit the same range of noise levels, around 370-390 ENC, for all chips investigated (Figure 8.54, left). On the right hand side of Figure 8.54, the connection between chuck temperature and hybrid temperature is shown, which can be useful to detect whether the different thermal conductivity of the UV-glue could impair the performance of the hybrid and lead to higher observed hybrid temperatures. This is however not the case: hybrids and modules with both, silver-epoxy and UV-glues, show the same relationship between hybrid and chuck temperature. This indicates, that the heat transfer between cooling chuck and the ASICs is equivalent for both glues in the tested temperature range.

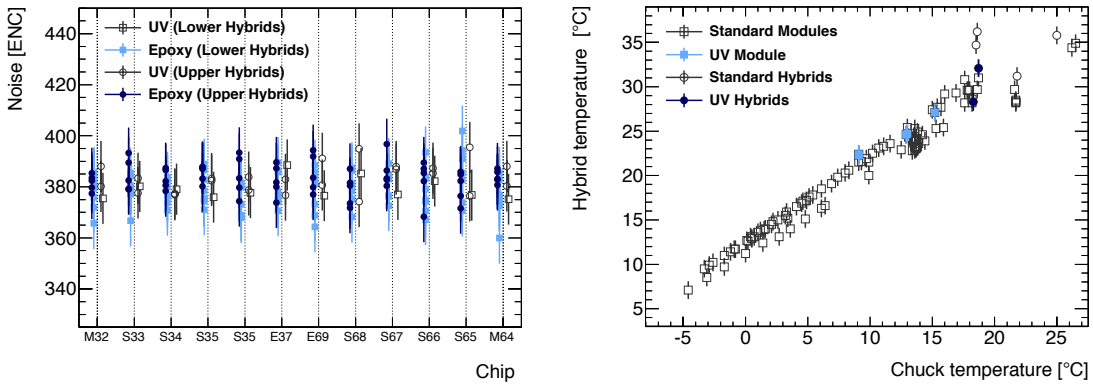


Figure 8.54. Comparison of noise levels of hybrids manufactures with silver-epoxy and UV-curable glue (left). Relationship between hybrid and chuck temperatures for a number of measurements on hybrids and modules manufactured using silver-epoxy and UV-curable glue.

here a short paragraph on the radiation hardness of the glue with one plot[IMG]

8.4.2 Material estimate

currently from the LoI, will be updated in June 2016[IMG]

Based on the module design for the ABC130⋆, a material budget estimate has been made for the barrel short strip module. End-cap modules will be similar with the differences due to the fractional coverage of the sensors by the hybrids in the various rings. Assuming a 320 μm thick sensor, this yields a predicted radiation length for short barrel and long barrel modules of 0.55% and 0.44%, respectively. Figure 8.55 shows the fractional contributions for the different materials to a module. As the sensor dominates the material, the single-sided modules has been well optimised to minimise material. Further reductions are unlikely as the second largest contributor to the radiation length is copper. Reducing the copper thickness could affect the hybrid yield. Hatching the copper area may cause unacceptable voltage drops and/or noise increases. ? The resulting hybrid is 15 mm × 98 mm and has three metal layers. Based on the prototype hybrids using the ABC250, the a bare hybrid is estimated to be 0.11% of a radiation length (X_0) and its components (ASICs, SMDs, solder, and epoxies) is 0.1% X_0 averaged over the module. The total radiation length of a stave is estimated to be under 2%, including the stave core, cooling pipes, bus tapes and modules.

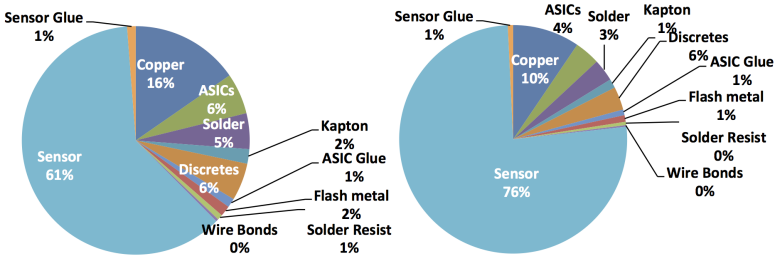


Figure 8.55. Fractional contributions for different materials to the radiation length of the barrel modules. Left: Short Barrel. Right: Long Barrel. New plots will be prepared in the next few weeks[IMG]

8.5 Finalised Module

A nearly fully bonded full barrel module is shown in Figure 8.56. The green frame in which the module rests is used for connecting the module to power and readout for qualification tests. These tests include e.g. calibrations, gain and noise measurements.

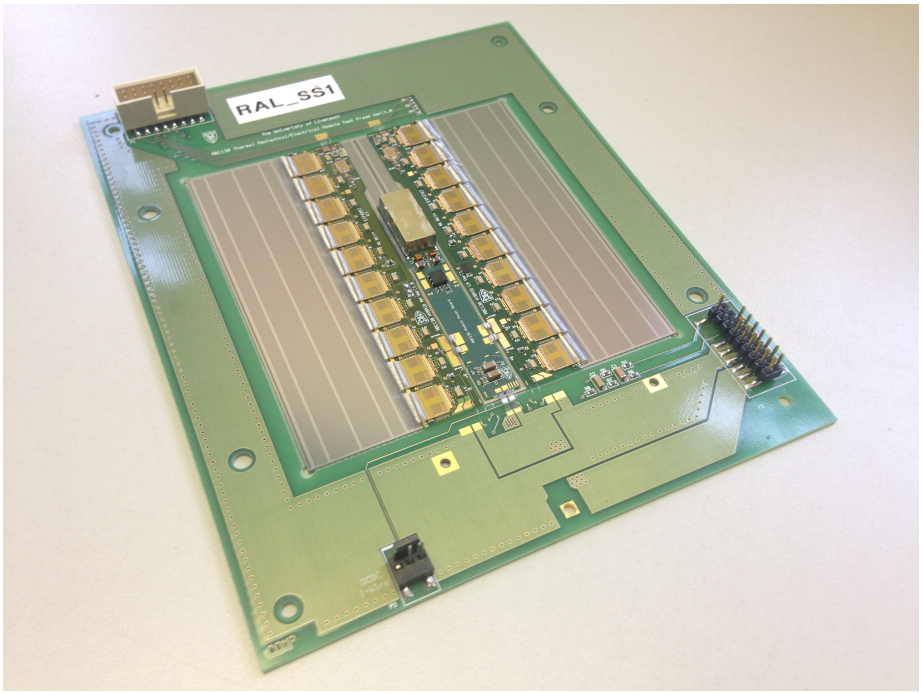


Figure 8.56. Fully assembled short strip barrel module with ATLAS12 sensor and ABC130 chips including power board.

8.6 Planned Quality Control during production

For hybrids and modules a series of tests are being designed to cover both QA (statistical studies of quality during R&D and on a batch basis in production) and QC (tests performed on every production item). These include a series of tests on their assembled structure (through metrology

surveys), their electrical functionality and their thermo mechanical properties (including ASIC burn in, thermal cycling and long term cold tests). These tests are evolving through work from several R&D programs, and the current status of these tests are explained in the following section. QA will get its own chapter later in the TDR, here we should concentrate on the QC[IMG]

8.6.1 Hybrid & Module Overview

The current plan for QC tests on each produced hybrid and module is as follows:

Hybrid QC

1. Reception and Visual inspection of components (Section 8.6.2)
2. Hybrid metrology (Section 8.6.3)
3. AISC attachement (Section 8.3.1)
4. Hybrid metrology (Section 8.6.3)
5. Wirebonding (Section 8.6.4)
6. Electrical confirmation tests of Hybrid (Section 8.6.5)
7. Thermal tests (Section 8.6.6)

Module QC

1. Reception and Visual inspection of components (Section 8.6.2)
2. Electrical confirmation tests of hybrid (Section 8.6.5)
3. Hybrid attachement (Section 8.3.2)
4. Module metrology (Section 8.6.3)
5. Wirebonding (Section 8.6.4)
6. Electrical confirmation tests of Module (Section 8.6.5)
7. I-V tests of Module (Section ??)
8. Thermal tests (Section 8.6.6)

After all QC tests, gradings will be made on the hybrids & modules: Good, Pass, Re-work and Fail. The tolerances established for each test to grade the components as 'Good' are explained in the following sections.

8.6.2 Hybrid & Module Visual Inspection

8.6.3 Hybrid & Module Metrology

After the gluing of ASICs to the hybrid, and the gluing of hybrids and power board to the module, metrology (X, Y and Z) will be carried out for grading. A range of techniques exist amongst the hybrid and module institutes for such measurements. These include

- Optical Metrology - Uses a camera optics with small depth of field, with the focussing providing a measure of the Z position
- Laser Focus Metrology - Uses a laser instead of an optical light source for a focus on the surface
- Laser Scan Metrology) Uses a laser to scan over the surface of the object, proving a visualisation of the flatness
- Touch Metrology - Use of a stylus with the object being measured after contact with the component surface

For all measurements in production, only optical and laser measurements will be used for module metrology, so to avoid potential damage of the silicon sensor by the use of a touch probe. However because of the protective passivation layer of the ASICs, touch probe measurements could used for hybrid metrology. Extensive calibration of equipment and measuring techniques have taken place since the IDR, to allow for both the comparison of data and for the qualifying of equipment for production. Fig (8.57) shows a dummy module assembled using glass pieces for metrology calibration. The blue crosses indicate the positions of the optical focussing for measuring the surface of the glass sensor. Fiducials on the hybrid give the z height of the hybrid surface, and touch down probe measurements are made on top of the glass ASICs. Using glass ASICs also allows for optical focussing on the surface of the ASIC landing pads, allowing for an additional calibration measurement.

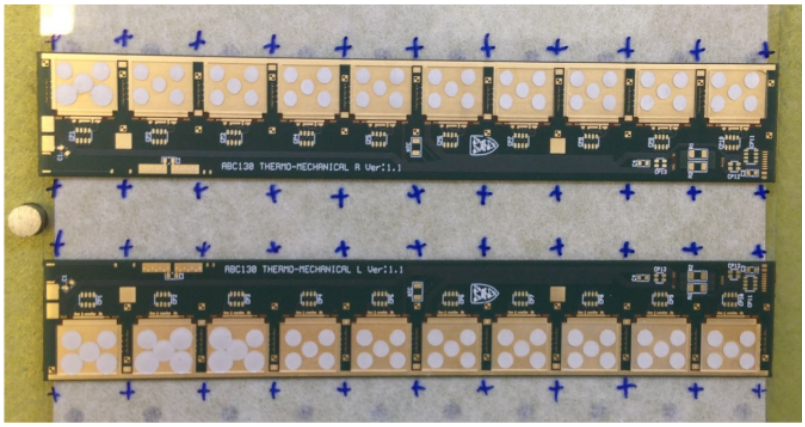


Figure 8.57. A dummy barrel module assembled using glass pieces for metrology calibration

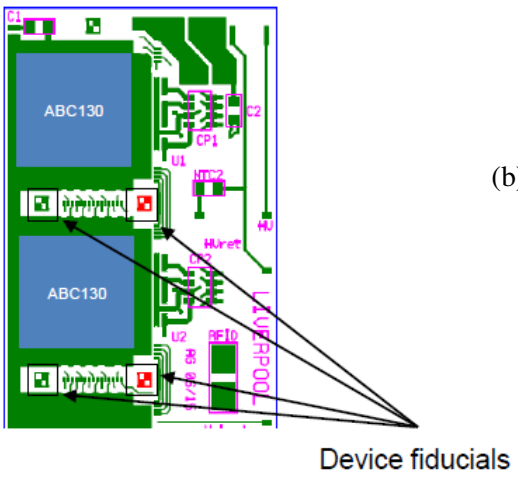
For metrology of both hybrids and modules it is envisaged the measurements will be fully automated, with pass/fails cuts introduced into custom written software. Such automation is aimed

at reducing measurement times and improving the repeatability of measurement positions on the objects under test. The constraints that are needed for X, Y and Z measurements are explained in the following subsections. At present these constraints are based on experience with barrel modules. However it is expected that most of these constraints will be largely identical for endcap modules.

X-Y Hybrid Constraints

After gluing, metrology will be carried out to investigate the positions of the ASICs relative to the hybrid. Any large displacement of the ASICs could cause issues for the wire-bonding, both in terms of the backend bonds to power the hybrid, and the front end bonds to the sensor strips. Nominally, 1.42 mm spacing between ASICs currently results in a bonding length of 400μm. Currently the the X-Y rotation of the ASICs is constrained by the pickup chip tray, and measurements have shown the max variation in position using this method to be <100 μm. As groups, chips can be misaligned to hybrid en masse but the max displacement allowed is set by hybrid panel requirements, which is currently $\pm$ 100 μm in X and Y. Placement of ASICs will be measured relative to fiducials on the hybrid. (Fig 8.58a)

(a)



(b)

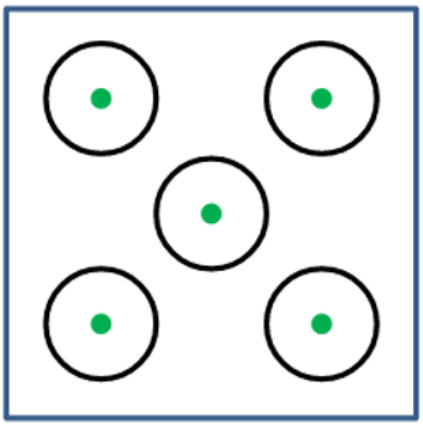


Figure 8.58. a - Fiducuals on hybrids for measuring X-Y positions of glued ASICs; b - 5 positions on each ASIC pad that are measured in Z before and after ASIC attachment for calculation of glue heights

Z Hybrid Constraints

The glue layer thickness between the ASICs and hybrid is designed to give good coverage for thermal performance, mechanical stability and to take up any variability in hybrid shape/thickness. The current 125 μm thick glue stencil is designed after compression to achieve a target glue thickness of 80 μm. The maximum glue height is set by the chip being able to stick to the hybrid, and the minimum height is set by the whether or not the glue squeezes out from under the chip (40-50 μm). Using hybrids made in the 250 nm program, a target glue thickness was found to be **80**$\pm$ **40** μm. Glue thicknesses can be measured using either optical or using a touch probe metrology. Before ASIC gluing, each ASIC placement pad is measured (in 5 locations) in Z relative to the panel surface (Fig 8.58b). After gluing measurements are made on the same X-Y locations on the top of

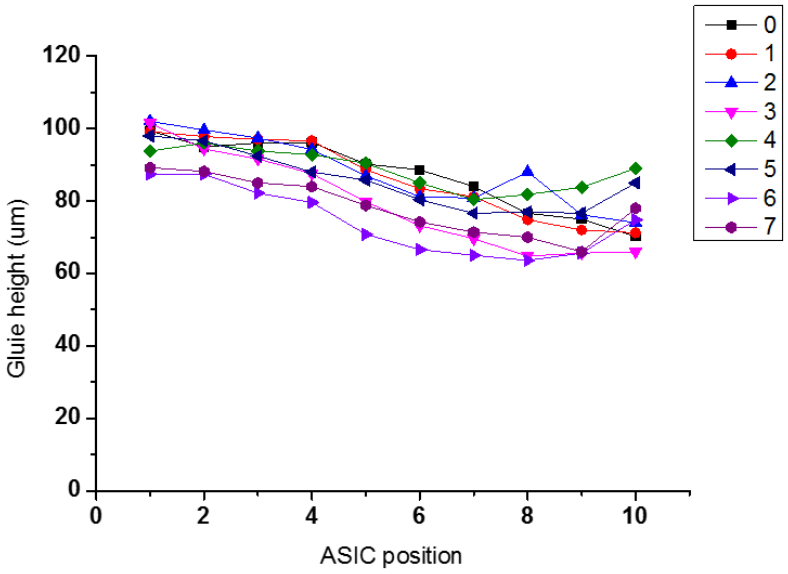


Figure 8.59. ASIC-Hybrid glue heights for a panel of 8 barrel hybrids made for the 130nm TM stave program

each ASIC. Glue heights are then calculated as the difference in Z after ASIC thickness (300 μm) is subtracted. An example of ASIC-hybrid glue heights for a full 8 hybrid panel can be seen in Fig. 8.59. [we can make and measure things to the standard needed for production]

Module co-ordinate system

For the purposes of module metrology, we will assume the following co-ordinate system (Fig. 8.60).

- X: Perpendicular to strips
- Y: Parallel to strips
- Z: Out of module

X-Y Module Constraints

As the module size is dictated by the sensor size there currently exists no module X-Y constraints in relation to the stave or petal mounting. However constraints do exist in relation to the hybrid's post gluing position on the module. Data and power bonds from the hybrid ends must be made from the bus tape, and there should be no part of the hybrid overhanging the sensor perimeter. Extreme (X-Y and angular) translations of hybrid positions on the modules will effect both the ability to wire-bond the front end channels and glue the power board to the sensor. Studies have shown that the requirements of the hybrid on sensor positions are constrained as follows

- Δ X < ? μm (Hybrid is positioned over FE wire bondpads)
- Δ Y < ? μm (Hybrid overhangs end of sensor)

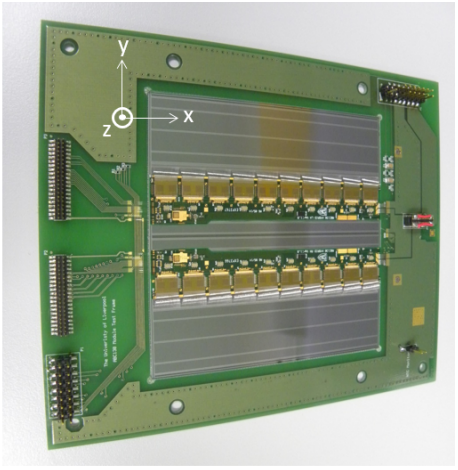


Figure 8.60. Adopted co-ordinate system for module metrology

- $\Delta\,\Theta <$? Degrees Rotation (Power board cannot be glued to sensor)

The positions of the hybrids on module will be measured using non contact (optical or laser) metrology techniques.

Z Module Constraints

The uniformity in Z is set by the hybrid-sensor gluing step. Since the LoI we have used both the 250 nm program as well as the 130 thermo-mechanical stave program to test and measure the necessary metrology constraints. Experience from the 250 nm program showed that glue thickness greater than 160-180 μm resulted in hybrids not sticking to the sensors. It also showed that thin layers (<80 μm) resulted in glue seepage, prohibiting the Front-end wire bonding. This has resulted in a target glue thickness of $\mathbf{120 \pm 40}$ μm.

Similarly to the technique for measuring glue hight measurements of ASICs on hybrids, module glue heights are determined by the subtracting the hybrid thickness (275 μm) from the difference in Z between the hybrid surface and sensor surface. Figure (8.61) shows the latest results from Z height metrology of hybrid-sensor glue heights for 130 nm thermomechanical modules over 6 module buildings sites.

It can be seen that the vast majority of hybrids glued though the different institutes can both adhere to 120$\pm$40 μm with the current generation of assembly tooling and measure glue height using the established metrology techniques.

In addition to check for sensor bowing after module assembly, Z envelope measurements of the entire assembled module will be made using non contact metrology techniques. The current thermomechnical program will be used to set the tolerance for allowed module bow. However experience from the 250nm electrical stave program showed modules with bow of up to $\sim$300 μm could be glued to the stave.

8.6.4 Hybrid & Module Wirebonding QC

- QA to be done though pull bond tests on ABC130*, HCC*, Si and hybrids

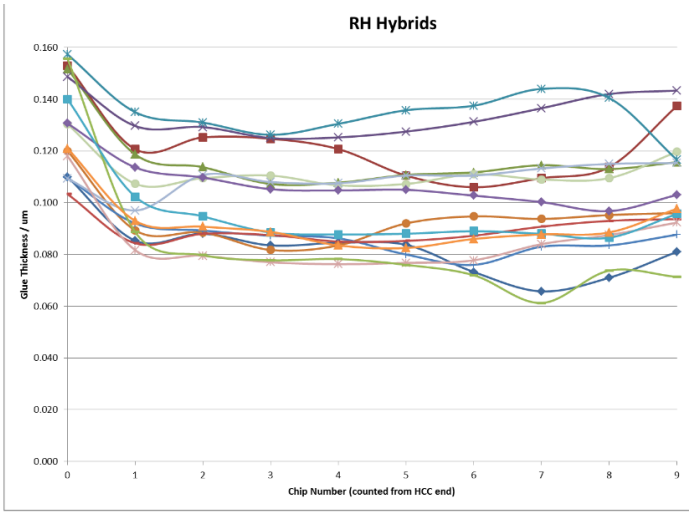


Figure 8.61. Hybrid-Sensor glue heights for a range of modules made for the 130 nm thermo-mechanical stave program

- Sampled QA to be done though pullbond tests on sacrificial bonds on each module/ hybrid test coupons
- QC of every bonded item, which has a strong inflluence on final grading

[Wire bond pull strengths, Mil spec (good enough?)]

Hybrid Bonding QC

Wire bonds are made from the ASICs to the hybrid to supply data, communication, powering and grounding connections. Additional wire bonds are made from the hybrid to the hybrid panel to allow for electrical testing. Failed bonds should be detected either by post bonding visual inspection or identified in electrical confirmation tests. The hybrid and ASIC bondpads have been designed in geometry to allow for 2nd boning/re-works if required.

Module Bonding QC

Wire bonds are made from each front end (FE) ASIC channel to a silicon strips, resulting in 2560 FE bonds for long strip modules, and 5120 for a short strip module. Additional wire bonds are made for powering and data connection to the module frame for electrical testing. Due to the 4 row bonding of modules, visual inspection is required between each row bond stage. This is due to the difficulty of removing failed bonds or re-bonding where this is an overlapping bond from a subsequent row An alternative method for wire-bond QC is also being investigated. This uses an electrical test setup integrated into the wire-bonding machine. Wire-bonds appear as channels in the software as the connections are made Fig (8.62). This allows the wire bonder to check all front end bonds are made between each row bonding stage.

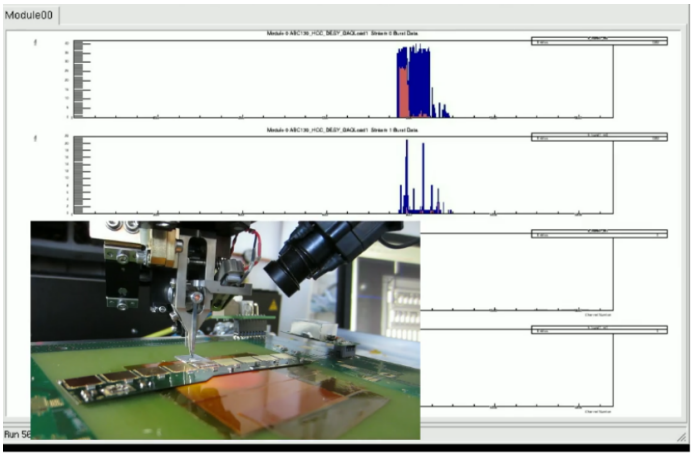


Figure 8.62. Example of electrical testing of completed front end bonds on the module during wire-bonding

Pass/Fail Grading for wire-bonded Hybrids & Modules

All bonds are required for a fully functioning hybrid. Lack of bonds will be detected though non responsive ASICs in later electrical test. For modules, all data, communication and power bonds must be functional. An element of the pass/fail grading modules will be based the number of front end channels that are not bonded, or do not respond during electrical testing. As an example, the allowed number of dead channels for end-cap SCT modules was <15 (equal to 2% of all channels) or <8 consecutive channels. For the ITk, the acceptable wire bonding failure rates is being informed by ongoing simulation studies. These studies are simulating the efficiency after a range of channels on modules are switched off to replicate failed wire bonds. Also being investigated is the effect of consecutive dead channels, dead ASICs and dead hybrids. to be checked[IMG]

8.6.5 Hybrid & Module Electrical Tests

All planned electrical testing of hybrids and modules must be scalable to match large production throughput at each build site, currently estimated to be 2-3 hybrids panels per day, and up to 4 modules per day. (see (chapter 21).

Planned Electrical tests

Hybrid Testing

- Strobe delay
- 3 Point gain
- noise occupancy

Checking for chip functionality, noise & gain. Done using single connector to panel or using multi panel crate tests

Module testing

- Strobe delay
- Tuning
- 3 Point gain
- noise occupancy
- I-C scans

Checking for chip functionality, noise & gain, as well as module response

8.6.6 Hybrid & Module Thermal Tests

It is planned that ASIC burn-in, thermal cycling and long term cooling tests will be closely based on SCT production experience, with the relevant changes made to the upper and lower temperature regimes. In addition, further QA studies based on the HALT & HASS methodology are also being investigated for their suitability.

Object	Temperature at Evap =-35°C	Temperature at Evap =-30°C
Module	-30 °C	-25°C
Silcon	-30°C	-25°C
Hybrid	°C	°C
ABC*	°C	°C
HCC*	°C	°C

Table 8.18. Estimated temperatures experienced by module components for 2 different evaporation temperatures

Thermal FEAs indicate the lowest temperature the modules and its components expect to experience during operation at the HL-LHC. The temperature of the components is strongly correlated to the expected evaporation temperature, and whether or not the pixel and strips systems share a common cooling loop. This in effects the lower temperature of any long term or thermal cycling tests. Shown in Table 8.18 are the expected temperature of components with (Evap=-35°C) and without (Evap =-30°C) a common cooling loop.

Hybrid temperature tests

A key QC test for hybrids is the ASIC burn-in tests to check for any early ASIC death. Based on SCT experiences, long term (>90hrs) tests will be carried out on hybrids at ∼37°C. For testing the thermomechanical properties of the assembled hybrids, thermal cycling will be performed 10 times through lower and upper temperatures ranges informed via further FEA studies.

Module temperature tests

Test setups are being designed to allow for both thermal cycling and long term cold tests of modules. Current prototypes allow for the testing of 4 barrel modules (to suit the required module rate through production) down to -30°C. They have been designed to allow the modules to be clocked and powered during runs if required.

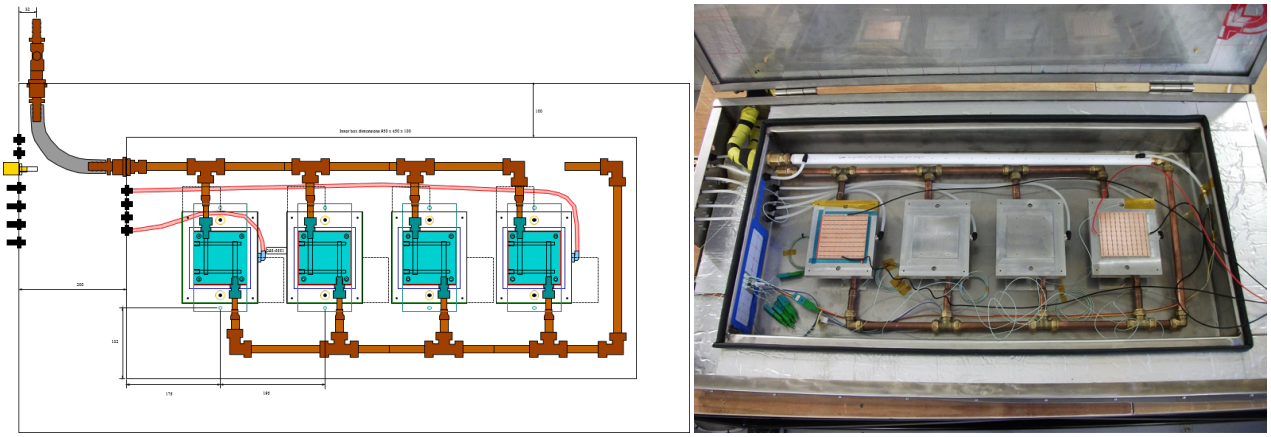


Figure 8.63. Protoype module cold box for thermal cycling and long term cooling tests

[add a part on the sensor bowing causing the cooling to be an issue]

Again, based on SCT experiences, it is envisaged that long term (>24 h) tests will be carried out for modules at ∼10°C, and thermal cycling performed 10 times through lower and upper temperatures ranges informed via further FEA studies.

Module QA - thermal shock

A planned QA test for modules is to study their effect after experiencing a large ΔT (thermal shock). The magnitude of such temperature changes are based on

- Loss of module power
- Loss of stave/petal cooling
- Temperature changes the modules experiences at installation

8.7 Review milestones, goals and purchase plans

this will most likely go into a later section[IMG]

9. Silicon Strips Modules– Hybrid and Module Test Results

Editor: Marcel Stanitzki
Chaser: Ingrid-Maria Gregor, Ingo Bloch
Number of pages to write: 20
In the following sections the various ITk strip module components,.....

9.1 Laboratory tests of hybrids and modules

During the extensive R&D programme for the ATLAS ITk strip detector a number of prototypes for the hybrids and modules were studies. In this section the most relevant results will be summarised. The parameters of interest are the Equivalent Noise Charge (ENC) and the gain. These are determined using standard threshold scans for binary readout systems.

In the threshold scans, the numbers of hits at a fixed injected charge versus the discriminator threshold voltage is recorded. This procedure is repeated for different values of the threshold voltage using 200 to be checked[IMG] iterations for each threshold value. The occupancy curves (s-curves) is recorded for each channel at a particular injected charge. The output noise is extracted as the width of the s-curve, which determines the noise amplitude at the discriminator output. The 50% occupancy point from the s-curve is plotted against the injected charge to yield the response curve. The derivative of this response curve is the gain of the channel at the discriminator. Finally, the input noise in ENC is calculated as the gain divided by the output noise. It corresponds to the noise at the input of the discriminator for every channel. The channels have been trimmed to yield as flat noise as possibleto be checked[IMG].

following itemised list is the plan currently under discussion for what to cover in the following pages

- std 3pt-gain Noise (and Gain?) results for barrel and EC, each 250(?) and 130(!) as well as with and without sensor
- 130 comparisons across labs as currently being prepared
- exemplary beta-test results for EC and Barrel 130
- exemplary laser-test results for EC and Barrel 130 (could be dropped ?)
- highlight test-beam results for EC and Barrel 130 to prove that the modules can efficiently record particles with high spacial resolution (can use 250 if we don't have the corresponding 130 results?) **already covered - see later in the chapter**

9.1.1 Results from an end-cap hybrids in 250 nm technology ASICs

Hybrids built with ABCn250 chip technology for the protoyping of the petalet structure and also the corresponding modules are characterized for their electrical performance.

The input noise in ENC and its stability for seven and eight hybrids respectively are shown in Figure 9.64. Depicted is the input noise in ENC has been determined for each of the readout chips by fitting a Gaussian to the noise distributions of each of the channels of the respective readout chip. The uncertainty on this mean noise per chip is determined by comparing a number of measurements

with the same conditions and comparing the results, some of these variations are still visible in the plot as separate data points in the same color. A variation of ± 10 ENC covers all fluctuations observed. Figure 9.64 shows an input noise of 380 ± 10 ENC per readout chip – consistently for the different readout chips on the same hybrids but also consistently for all hybrids of a specific type (lower or upper) and lastly, consistently also between hybrid types. The value of 10 ENC corresponds to about 2-3 times the widths of the Gaussian fitted to the noise of the single channels.

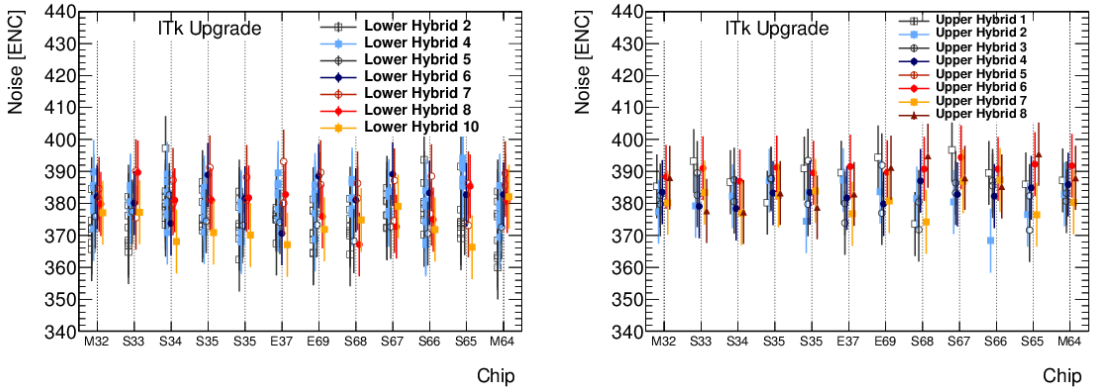


Figure 9.64. Electrical stability observed for a number of lower and upper hybrids. The measured noise in ENC has been averaged for each of the chips on the hybrid. Better quality needed without ITk Upgrade label. IMG

To further investigate the stability of the hybrid performance, the environmental conditions (i.e. temperature of the cooling chuck and the humidity) are varied. Figure 9.65 displays the results of these tests for three selected ASICs for two lower hybrids. The noise level stays within the uncertainties within a humidity range of 15 to 55% and a temperature range of 5-35°C. The temperature is inferred by the temperature of the chuck used for cooling, since these are linearly correlated (cf. Fig. 8.54).

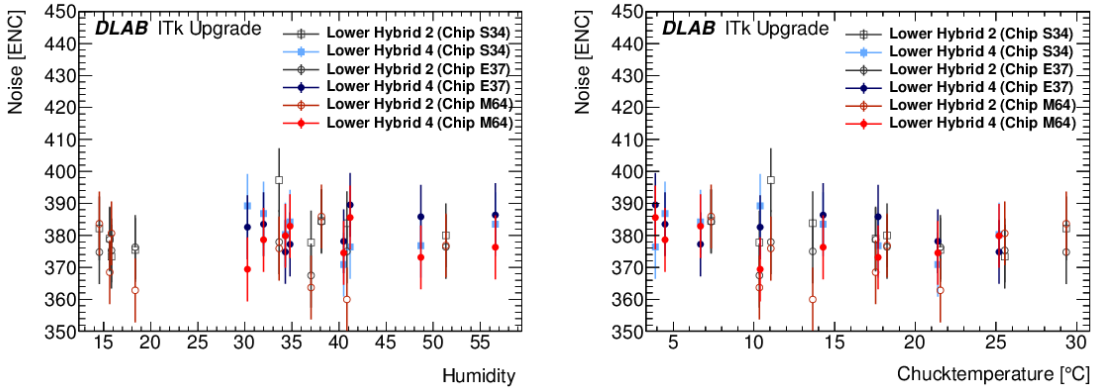


Figure 9.65. Input noise in ENC averaged over selected ASICs for two different lower hybrids as a function of humidity and chuck temperature. Better quality needed without ITk Upgrade label. IMG

The results presented up to here are obtained using silver epoxy glue to connect the 250 nm technology ASICs to the hybrids, however as described in Section 8.3

9.1.2 Comparison of hybrid-only and module performance

I am not sure if this is relevant for the TDR - keep it for the time being, but we might have to reconsider[IMG] The addition of further load to the hybrid in the form of the sensor leads inevitably to an increase in input noise. This is demonstrated in Figure 9.68 where the input noise in ENC average per ASIC (left) and in single channels is compared between hybrids and modules. Note on voltage[IMG] While the noise level of all hybrids is around the aforementioned 380±10 ENC, it rises to about 550-600 ENC for the final modules and in the case of the so-called 'embedded' modules even to 700 ENC. These 'embedded' sensors contain integrated ('embedded') pitch adapters that bridge the gaps between the varying pitch of the bonding pads on the sensor due to the geometry in the end-cap and the constant pitch of pads on the readout chip. This is realised using an additional metal layer at the back-end phase of the sensor fabrication and serves to create equidistant bonding pads, increasing reliability and bonding speed. However, the thus added additional metal-tracks also increase the interstrip resistance and thus the input noise that moreover varies depending on the geometrical position of the channel, as can be seen in the left hand side of Figure 9.68. For this reason, the embedded sensors are not further pursued for the final detector building. to be checked[IMG]

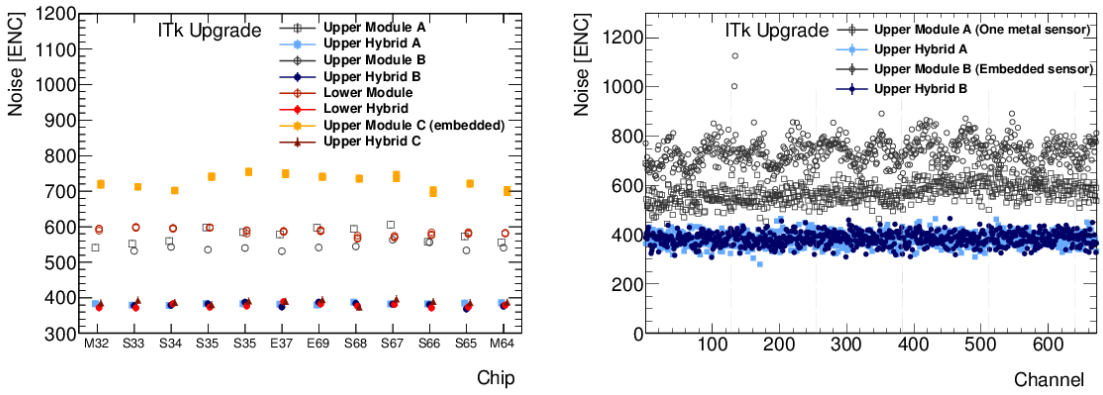


Figure 9.66. Comparison of input noise in ENC between hybrids and modules average per ASIC (left) and per channel (right). Voltage? Better quality plot needed ...

no text for the following plot ? [IMG]

no text for the following plot ? [IMG]

9.2 Test beam & Irradiations

Andy with input from many people[IMG]

writing this assuming the 2016 test beam data will be in the TDR.

Since the IDR, there have been 4 (2) test beams conducted at both DESY (3-6 GeV electrons) and CERN (140 GeV Pions) to test a range of devices. To date devices tested have included 250nm & 130nm generation end-cap and barrel modules, utilising both short and long strip strip sensors (Fig 9.69). Irradiations have also been performed on a series of objects including DAQ loads (each with an HCC, an ABC130 and a mini sensors), hybrids and modules. These devices have also been tested at test beam to measure any possible degradation in performance.

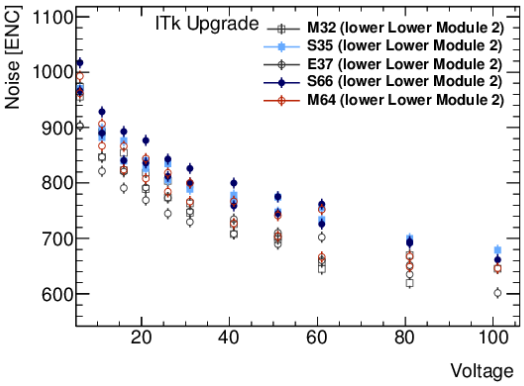


Figure 9.67. ADD: No hysteresis.... [freiburg] .

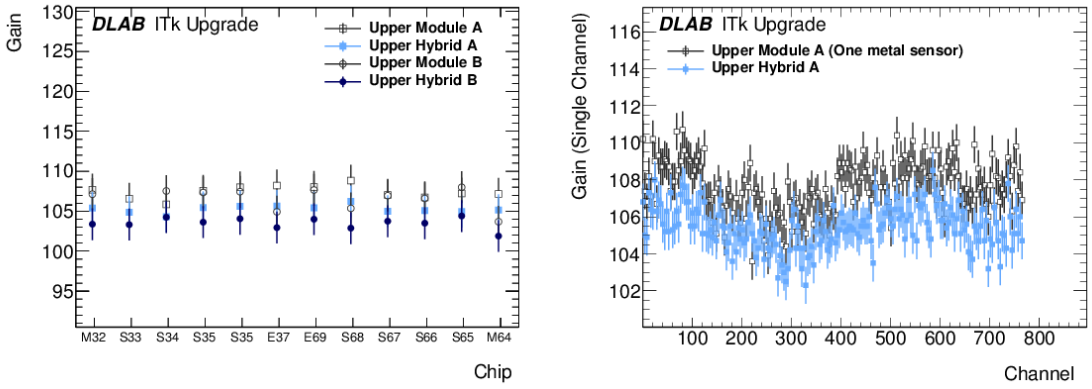


Figure 9.68. Gain .

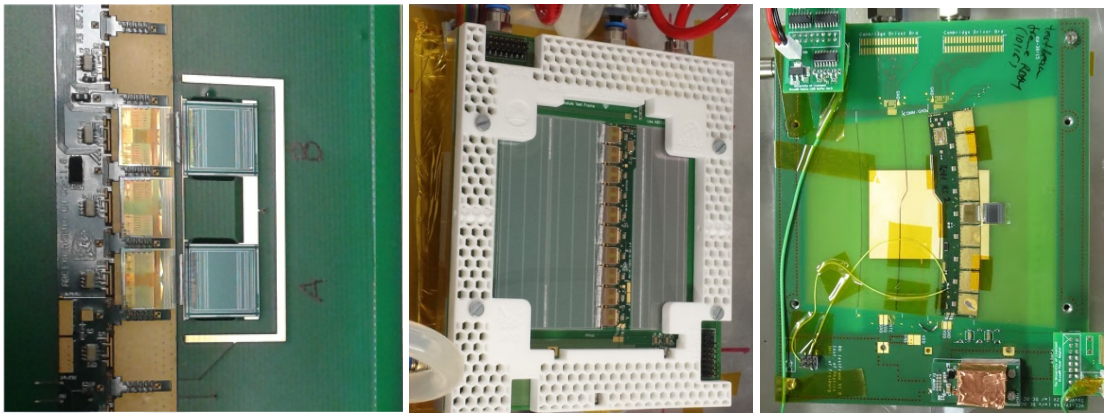


Figure 9.69. A barrel mini module, long strips module & endcap mini module under test at testbeam

In addition, it is expected that through pre production & production, a small sample of modules will be tested at test beam. Consequently, the techniques and analysis methods shown in the following section will be used for any subsequent test beam activities.

9.2.1 Test beam Setup

For both DESY and CERN test beams, the EUDET style (DURANTA, MIMOSA26 based) telescope was used (Fig9.70 [**?**]. Custom track fitting general broken lines (GBL) code was integrated into the EUTelescope reconstruction software [reference to GBL] to process strip sensor data. All DUTs were read out using the current test hardware (ATLYS FPGA development board) and software (ITSDAQ) and integrated with the telescope software (EUDAQ). Custom cold boxes were designed to regulate temperatures and test irradiated objects cold (-20°C). A pointing resolution of 4μm was measured, and a timing resolution of 25 ns was achieved with the addition of a pixel timing plane (FE-I4).

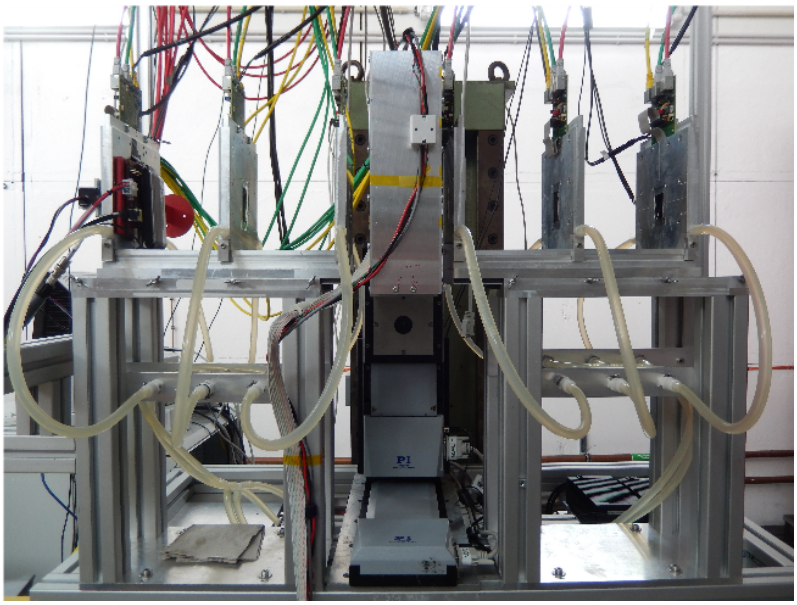


Figure 9.70. The DURANTA Telescope at DESY with a barrel mini module under test.

9.2.2 Test beam results

For each DUT threshold scans were performed with ∼10k events taken for each bias and threshold setting. The beam size (∼1cm^2) allowed for the investigation of channels attached to individual ASICs, as well as specific areas of the full size sensor (sensor edges, bias ??).

Figure 9.71 shows For both short strip & long strips devices tested, residuals of ∼31μm were achieved (Fig 9.72), allowing for the investigation of inter-strip behaviour. Fig 9.73 shows the inter-strip efficiencies for 4 consecutive strips.

- 2d efficiency plots
- gain measurements?

9.2.3 Irradiations

It is necessary to study the performance of modules after experiencing the irradiation fluences expected after 10 years of HL-LHC operation. As well as measuring any degradation in sensor per-

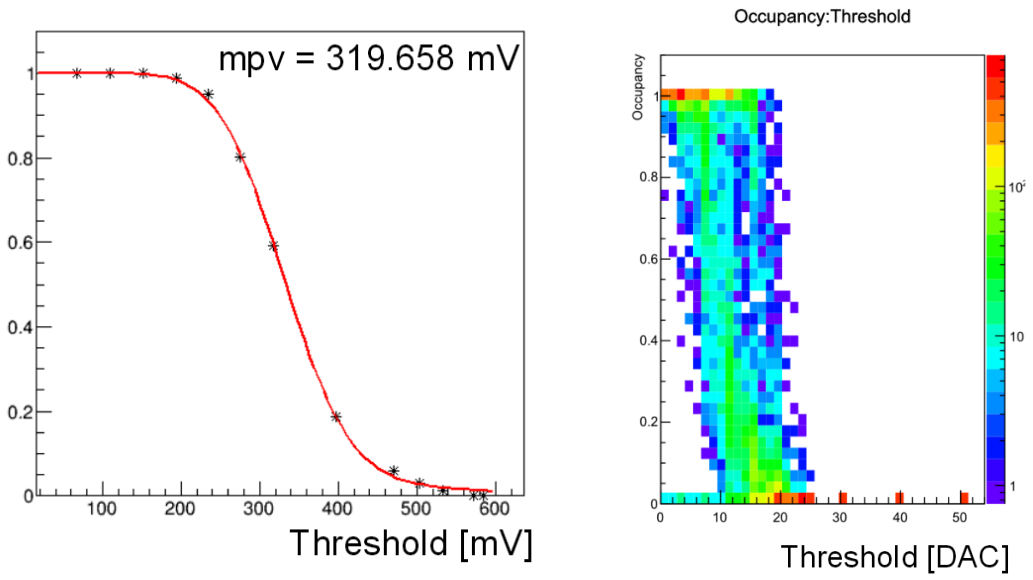


Figure 9.71. Threshold & occupancy scan data from a barrel mini module at 350V bias measured at DESY testbeam

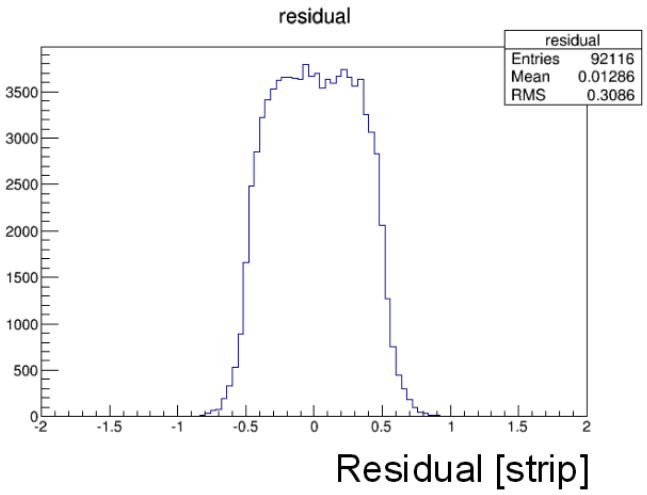


Figure 9.72. DUT residual of $\sim$31μm was achieved for the 74.5μm pitch strips, allowing for inter-strip efficiency studies

formance, it is important to study any effects on a module's electronic components such as ASICs and hybrids. FLUKA SIMULATIONS SAYS... Since the IDR, irradiation programmes have been carried out on single components such as ABC130s, hybrids, HCC's and silicon sensors. In addition, irradiations were performed on both DAQ loads and full electrical modules. The irradiations performed and subsequent tests are explained in the following sections.

X-Ray irradiations

An X-ray irradiation setup was commissioned at RAL and used to irradiate ABC130s on 2 endcap

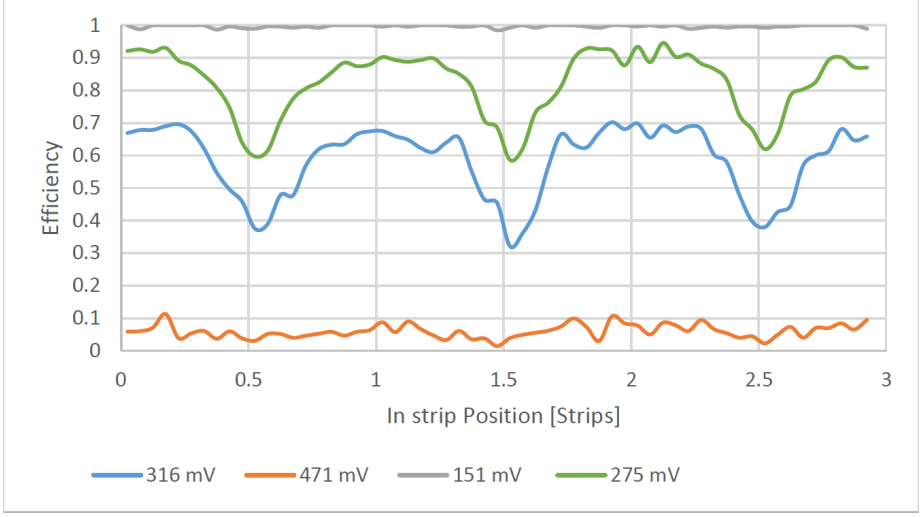


Figure 9.73. Inter-strip efficiencies for 4 strips at 4 thresholds.

DAQ loads to a dose of 1.45 MRad & 4 MRads (at 0.85 MRad/hr at -5°C)

ABC130's at Charm

Proton irradiations

Irradiation of a full 130nm barrel module and a bare barrel sensor were conducted at the PS (24 GeV protons) facility at CERN to $3x10^{15}pcm^{-2}$.

Additionally fully loaded ABCn25 hybrids were irradiated at KIT with protons to a NIEL equivalent fluence of $2x10^{15}ncm^{-2}$

9.2.4 Results

Lab tests

[none yet]

Testbeam results

The X-ray irradiated DAQ loads were tested at DESY.

[results]

However due to the activity of the irradiated module, it was tested at CERN SPS/PS

[results]

Ingrid, Ingo & Tony

10. Staves and Petals Design

Editor: Uli Parzefall
Chaser: Jens Dokpe
Number of pages to write: 30

In this chapter the engineering design of the staves (for the barrel) and petals (for the end-cap) are described. Staves and petals are simply different flavours, necessitated by geometrical considerations, of the same basic conceptual unit; a Local Support (LS). Local supports combine the mechanical support with all the required services for a completely autonomous multi-module system. The barrel and end-cap sub-detector arrays are then formed of multiple copies of the same (or at least very similar) staves and petals mounted into the barrel and two end-cap global support systems.

The general performance requirements for staves and petals concern geometric stability, cooling performance and the supply of electrical connections to and from the modules and are therefore essentially identical. Similarly they share common interfaces; mechanical (to their respective global support structures), electro-optical (via an end-of-structure (EoS) card to the Type-1 services interconnects) and their connections to the cooling system.

Given the similarities in the requirements and interfaces, the engineering designs of staves and petals are conceptually identical. Local Supports are formed from a carbon-fibre composite sandwich structure with embedded cooling and integrated electrical services. The materials used have been selected to achieve the best possible performance and reliability with minimal dead material and a reasonable cost; the carbon-fibre material combines high thermal conductivity fibres together with a radiation-hard, low moisture expansion resin; the cooling structures are made from small-diameter thin-walled titanium tubing and low-density, high thermal conductivity foam; aerospace-grade carbon-fibre honeycombs and adhesives are used.

In the remainder of this chapter the detailed design of the staves and petals is presented. The requirements for staves and petals throughout their life-cycle are presented. The elements of the Local Support Architecture are discussed before describing the detailed design of the stave and petal. Next, the thermo-mechanical performance of staves and petals is demonstrated using FEA simulations and the results of measurements on prototypes. The results of simulations of the data rates and latencies for different TDAQ architectures are presented. The assembly procedures and quality control scheme for LS assembly are summarised followed by a description of the module-mounting process and the final testing of complete staves and petals. Finally, a draft schedule for technical reviews between the TDR and start of production are presented.

10.1 Requirements and Overview

The Local Support must encompass geometric, mechanical, electrical and thermal aspects in its design. The main functional requirements are; that it supplies all the services which modules need to function and transmit the data off the detector, that it is capable of maintaining the operating temperature of all modules within acceptable limits given the constraints imposed by the cooling system, and finally, that it ensures the position of each module is maintained within acceptable limits as defined by the ability to determine the module positions using track-based alignment

procedures during data-taking. The mechanical and cooling performance of the LS is determined by employing high-stiffness, high thermal conductivity carbon-fibre for the face sheets and the sandwich geometry which gives high rigidity and allows the cooling structures to be buried within the core such that heat generated by the modules is removed directly.

Mechanically, Local Supports interface to their global support structures through a series of position locators and locking points which together define the position of each LS. The electrical services needed to power and control modules are connected to the off-stave services via an End-of-Substructure (EoS) card and distributed to each module along electrical connections on the surfaces of the LS core. Similarly, the EoS card receives the data from each module, processes it and then transmits it via optical links to the data acquisition systems. The embedded cooling loop is connected to the off-stave cooling services via orbital welding to eliminate the need for mechanical connections within the ITk volume.

The LS requirements can be summarised in three groups covering; the operation of modules within ATLAS, the integration of the strip tracker and the attachment and servicing of modules.

10.1.1 Requirements for the Operation of Modules in ATLAS

For the most part of their life-cycle Local Supports will be in operation within the ATLAS experiment. During this period, Local Supports will play a critical role in ensuring the proper functioning of the ATLAS strip tracker. Local Supports must be compatible with the environmental conditions within the tracker volume and maintain the positions of modules with sufficient stability to enable track-based alignment procedures to converge. The required electrical power and control signals for module operation need to be distributed and the data must be gathered and condensed before being transferred off. Finally, the heat generated by the modules must be absorbed in to the CO_2 cooling system whilst maintaining a safe module operating temperature.

Operating Environment The thermal condition within the ITk is dictated by the evaporation temperature of the CO_2 cooling system. During detector shut-down Local Supports will reach stable equilibrium with the environmental temperature within the ITk volume. Initially, this might be 20°C but, as the sensors become more radiation damaged, a lower temperature may be defined. During physics operation it is envisaged that the CO_2 evaporation temperature at the exit of the Local Support will be -35°C. However, in certain fault conditions it is possible for the temperature to plummet to -55°C.

Humidity within the ITk volume will be regulated by flushing it with dry N_2 gas at a rate required to keep the dew point safely below the minimum possible CO_2 evaporation temperature in any operational scenario, including system faults and catastrophic leaks. Assuming the minimum CO_2 temperature is -55°C a dew point temperature of -60°C is a reasonable requirement. The materials used to construct Local Supports are to some extent hygroscopic. Assembly will take place in an environment where the relative humidity is in the region of 50% and then operated in a dry nitrogen atmosphere. Immediately after the ITk is sealed and the dry nitrogen gas flow is started, the hygroscopic structural materials (polymers, resins & adhesives) will begin to lose moisture by diffusion towards surfaces in contact with the N2 gas. As a result, dimensional changes may occur as a result of the materials having a non-zero coefficient of moisture expansion (CME).

10.1.2 Operational Stability

The requirements for geometric stability come from the limits on deviations for track-based alignment algorithms to be able to track potential displacements. The global stability requirements are summarised in table 11.15 of the ITk IDR cite IDR (page 118). In the measurement direction (r-phi) the requirement is for displacements to be less than 2 μm over timescales of 1 day and 5 μm over 1 month. The stability requirements in lesser sensitive directions (out-of-plane) are **10x higher**Is is really higher, or are they less stringent?.

These stability requirements are global numbers and as yet there is no agreed sharing between Local Support related and global support structure related stability. Geometric instability may result from environmental changes (temperature, moisture desorption, radiation damage), or mechanical deformation (gravitational sag, external loads, vibration, material effects).

When mounted on its support structure, the geometric position of a LS can be affected by gravity and dynamic inputs from vibration sources or transients and materials effects. Gravitational effects induce a static deformation and there is a requirement that any such deformation must be less than the amount which would cause gaps in hit-coverage to open up.

There are two types of dynamic instability which need to be considered; transient phenomena and vibration. Transient phenomena, such as movements in the external services, pressure cycling of the CO_2 in the cooling tubes and thermal cycling can cause changes in the load conditions on a LS and can therefore lead to significant changes in position. It is envisaged that such thermal cycles will be relatively rare and the intervals between such transients will be considered as forming a block of data with each unique block having its own alignment constants derived from the data.

10.1.3 Power and Data Transmission

The electrical power, control signals and data transfer services required by the modules are carried by a copper/polyimide "bus tape" mounted on both faces of the LS sandwich. The design of the copper track-work is constrained by the need to achieve the correct operating voltages for the front-end ASICs, to allow the transmission of signals to and from the modules with high reliability and to respect the geometrical constraints necessary for the 500 V sensor back-plane bias connections.

10.1.4 Thermal Performance

Thermal runaway will occur if the sensor generated heat (which increases rapidly with temperature) is not balanced by its removal to the coolant. Stable operation depends on a combination of the coolant temperature, thermal path resistance and sensor power (which grows with radiation damage). Detailed FEA models of the LS have been developed to predict temperature distributions and safety margins (headroom).

Check references in the paragraphs below

Radiation in the ATLAS detector has been modelled by Dawson et al [Lancaster 2011] using FLUKA, to predict the fluence as a function of the radial and axial coordinates, expressed in terms of the equivalent flux of 1 MeV neutrons (neq). Assuming 3000 fb^{-1}, 84.5 mb and 14 TeV centre-of-mass energy, the maximum fluence within the strip detectors is predicted to be 6.0ÃŮ1014 neq/cm2, located at the extremities of the inner barrel (R ~38 cm, |Z| ~117 cm). For safety, we apply a factor 2 to this model prediction, so that in the following we assume a maximum fluence of $1.2{\cdot}10^{15}$ neq/cm^2.

The power generated in the sensor is given by the product of bias voltage and the (temperature dependent) leakage current. We assume a maximum practical value for the bias voltage of 500 V. This is insufficient to fully deplete the sensor at high fluence, so that estimation of the depleted volume (and hence leakage current) is unreliable. Instead, we use the results of extensive irradiation studies of ATLAS prototype sensors. Measurements of the annealed leakage current at 500 V bias show that, over the range of fluence of interest, the power dissipated per unit sensor area can be approximated by [Affolder 2011]:

$$q(0^{\circ}C)[mW\,mm^2] = 0.05 + 0.5 \cdot \varphi[10^{15} neqcm^2] \tag{10.1}$$

A safe estimate of the maximum sensor power (after $1.2{\cdot}10^{15}$ neq/cm^2) is 0.65mW/mm^2 at 0°C. The leakage current (and hence power dissipated, q) vary with temperature T [K] as:

$$I_{leak,q} \sim T^2 \cdot exp(-E_f/2kT), \text{ where } E_{eff} = 1.21\,eV \tag{10.2}$$

Here the difference between E_{eff} and the silicon energy band gap E_g (1.12 eV at 0°C) is due to the intrinsic temperature dependence of E_g. This is well known and commonly used in the modelling of un-irradiated silicon devices. Experimentally it is found that eq. 10.2 describes very well the temperature dependence of irradiated sensors up to and beyond the maximum fluence of interest [Chilingarov 2011, Affolder 2011].

The thermal path in the Local support depends on the geometry and is optimised by distributing the cooling pipes evenly across its width. For the stave this limits the path length to 25 mm whereas for the petal the path length increases as a function of radial position. Adequate conduction across the detector width is consequently supplied by the sensor itself, in parallel with the CFRP facing (which has a comparable thermal conductivity). The heat is coupled from the facing to the cooling pipe through a few millimetres of graphite foam insert. Approximately half of the total thermal resistance is accounted for by the glue joints between components, the integrated bus tape and the finite rate of heat transfer from the pipes into the cooling fluid.

Must have new numbers for ABC130, must have star estimates

The thermal load contributed by the readout electronics will not be known accurately until the ABC130chips and the powering scheme have been prototyped. We have assumed power dissipation based largely on estimates summarised in [Diez-Cornell 2011]. For the ABCN130 (256 channel) readout chip we take the mean of the preliminary design estimate (163 mW) and a conservative upper limit (256 mW). The power dissipation used in the FEA is then evaluated assuming:

- ABCN130 (external power conversion) = 210 mW
- HCC Hybrid Controller Chip (prelim.) = 180 mW
- DCDC Power conversion efficiency = 80%

giving a total power of $20 \cdot 210$ mW (ABCN130) + $2 \cdot 180$ mW (HCC) + 1.050 W (Converter) = 5.61 W.

10.1.5 Requirements for the Integration of the Strip Tracker

During integration, Local Supports are inserted into the global support structures, located on their position reference features and locked in place. Following insertion the connections from the LS to the cooling system, electrical power and optical data transmission systems will be made. The LS design must allow for the varying load conditions during the process of LS insertion whilst obeying all the geometric clearances and positional tolerances required.

Prior to insertion LSs are held in their transportation frames. These frames are relatively cheap components which serve as a protective enclosure for shipping and also provide dummy interfaces for various test systems. Immediately before insertion, these dummy interfaces are disconnected and removed from the transport frame and the cooling tubes are trimmed back to their final length. The transport frame is mounted onto a system of tooling which supports the frame and manipulates it into the correct position and attitude for the insertion of the LS into the correct position in the global support sub-assembly.

Local Support Flatness Local Supports will be positioned in the global support structures via a number of position locations and locking points. Local Supports need to be flat enough to allow proper engagement of all mechanical interfaces without putting too much stress on the fixation points on the global support and the local support.

LS Envelope During Insertion During Local Support insertion, the envelope of the LS needs to be such that there is no risk to the LS being installed or those already mounted. This places limitations on the heights of components (especially the DCDC convertors) and the trajectory of the LS during insertion.

10.1.6 Requirements for the Attachment of Modules

Following the construction of a Local Support core, modules will be adhesively attached to the two faces and electrical connections between the readout hybrids and the bus tape will be made via wire-bonding.

It is assumed that during this phase the LS is retained in an assembly frame which references the position of the through locators which mimic those employed on the global support structures. Modules are then positioned in the plane of the LS with reference to the nominal position of the global support structure locators. The out-of-plane position of the modules is not governed by this coordinate system and is therefore a free parameter.

Co-cured Bus Tape Geometry The precise geometry of the bus tape is defined during the co-curing of the tape to the CFRP pre-preg. With the prepreg systems currently being used the cure temperature is about 120°C. Typically the bus tape expands during heating until the temperature at which the prepreg starts to cure is reached. Experience from prototyping indicates that the bus tape expands by < 1 mm along its length due to co-curing. The cumulative positional shift of wire-bond fields must be small enough to allow the wire-bonding of any module. Currently, the design of the hybrid and bus tape wire-bonding fields is such that wire-bonding is possible up to relative shifts of 0.3 mm. Provided the part-to-part variation in the expansion is small, then a correction to the bus-tape art-work can be made to minimise the overall expansion and optimise the co-cured tape geometry for wirebonding.

Table 10.19. Stave Bus Tape Power Requirements

Supply	Minimum voltage (V)	Maximum voltage (V)	Maximum current (A)
Low voltage	10	11	16.5
High voltage	-	700	???

Table 10.20. Petal Bus Tape Power Requirements

Supply	Minimum voltage (V)	Maximum voltage (V)	Maximum current (A)
Low voltage	10	11	8.25 ???
High voltage	-	500	???

Local Support Surface Geometry The LS design and assembly processes have been developed with the intention of producing cores which are smooth (have minimal surface roughness) and flat (have minimal large-scale departures from a plane).

Modules will be positioned relative to the LS using a system with precision optical metrology and a set of vacuum pick-up tools. The pick-up tools incorporate adjustment mechanisms which allow the in-plane position of a module to be adjusted to bring it into the correct location relative to the LS coordinate system. The modules are attached to the LS via an adhesive layer. This layer has to guarantee the positional stability of modules for the lifetime of the tracker and to conduct the heat generated in the module through to the facesheet. With respect to the latter, both the area of contact and the thickness affect the efficiency of heat transfer. In thermal measures the area of the layer should be as large as possible and have minimal thickness.

10.1.7 Tape Requirements

The low voltage power will be brought to the modules at 10 V and DC-DCconverters will be used to generate the required 3.3 V and 1.5 V for each module. The current draw will increase with ionizing dose and then decrease, therefore the requirements are specified in terms of the worst case current. In order not to compromise the data transmission, the voltage drop along the low voltage return line will be limited to 200 mV. The voltage drop along the positive low voltage line should be less than 1 V to ensure that the end module is correctly powered. The widths of the power lines have been adjusted to satisfy these requirements for the worst case currents.

The high voltage requirements are based on an assumed maximum of 500 V but the tapes will be assessed for operation at higher voltages in case this is required to increase the detector signal to noise at end of life. The High Voltage Insulation Resistance (HVIR) for both HV lines to neighbouring lines should be greater than 1 GΩ.

The Timing, Trigger and Control (TTC) data are sent from the EoSto the HCCASICS using multi-drop lines. The maximum data rate required is 160 Mbps. In order to satisfy the requirement for full readout of the detector at an L1 rate of 1 MHz, the module data is transferred from the HCCs to the EoS at a rate of 640 Mbps. The data links are all point to point. The barrel staves (end-cap petals) require 28 (14) such data links. In addition slow control (monitoring data) is sent to (from) the AMAC chip using I^2C communication at a maximum rate of 400 kHz.

10.2 Details of the design

Should we have the common concepts described together, or would we rather detail the concepts in subsections? I currently assigned 4+4 pages for the stave and petal subsection, but have a feeling that we might be better off with 4+2+2, where the first 4 describe the common approach (CF+Foam+Ti tube, insulating break, EOS area, tapes co-cured ...) I would prefer that you first make a common description and then some description of the differences; a table where all the materials are collected would be great[IMG]

In this section the details of the engineering design of both barrel staves and end-cap petals is presented. Using the common set of requirements, system-level architecture and materials leads to a single conceptual design for both barrel and end-cap Local Supports from which the two geometrically different implementations are derived.

10.2.1 Stave Core Design

Tim/Dave? *4 pages*

Barrel Staves

The Barrel Local Support (Stave) is formed from two face sheets which sandwich a core formed from the cooling components and a low density honeycomb together with various edge close-outs and ancillary components which combine to form the LS-part of the mechanical interface to the global support structure. Figure 10.74 shows a schematic of the internal structure of the stave core identifying the face sheets, cooling structure, low density honeycomb, close-outs and the interfaces to the support structures and services.

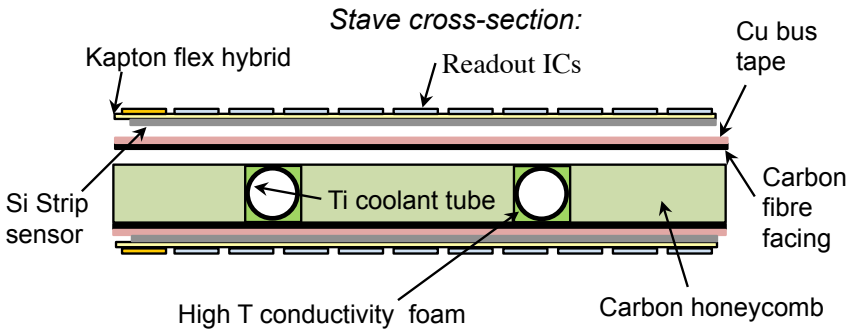


Figure 10.74. Schematic of the internal structure of the stave core.

Face sheets Face sheets are formed from layers of high-modulus unidirectional carbon-fibre material (prepreg) with radiation tolerant and low CME cyanate ester resins together with a copper/polyimide bus tape. The carbon-fibre material properties are dictated by the overall stiffness requirements for the stave and the thermal requirements for supporting the conduction of heat generated in the modules to the cooling structures embedded in the core. The copper/polyimide bus tapes are laminated together with three layers of K13C2U/EX1515 (45 gsm, 40 % RC) prepreg in a [0,90,0] lay-up (with 0 being the direction along the length of the stave) in an autoclave at high pressure and temperature (7 bar, 120 C°. Due to the high CTE of the bus-tape relative to the carbon-fibre, co-curing at high temperature stretches the tape and induces stresses in the final face sheet at temperatures below the cure temperature. These stresses can lead to curved face sheets which can

cause problems during stave core assembly. The degree to which the co-cured face sheet deforms can be reduced by performing the co-cure on a custom designed curved tool which produces a curved face sheet at 120 C° which then becomes flat at room temperature.

Cooling Structure As staves have all their services connections at the Z = 1.4 m end, the tube passes along the length of the stave and returns back again via a U-bend close to Z=0. Using both the flow and return arms maximises the area available for heat transfer into the fluid and hence the tubes are located ~25 mm from the centre-line of the stave such that heat flow from the module is divided into four sections of equal length and heat flux. In order to ensure that the structure is balanced with respect to thermally induced stresses, the cooling tubes are located in the mid-plane of the stave. The interface between the tube and the face sheet is formed using a thermally conducting carbon foam (Allcomp K9, 130 ppi, ρ_A=0.23 g cm^{-3}, K ~30 W/mK) and glue joints using an adhesive (Hysol EA9396) loaded with thermally conducting carbon particulates. To ensure electrical isolation between the stave and the external cooling services, the cooling loop incorporates two ceramic insulating breaks which are located just inside the stave core at the Z=1.4m end. Cooling loops are manufactured from three basic components; the U shape stave cooling loop and two composite inlet/outlet sub-assemblies. The joints between the three parts are all made through orbital welding. The inlet and outlet sub-assemblies each comprise a short section of the on-stave cooling tube, an insulating break and a 2.5 mm OD x 0.2 mm wall interface tube. The interface tubes follow the routing required after insertion into the global support structures but are extended by a few cm. The extension is terminated in a connector (Swagelok VCR) for all subsequent testing. Following the stave acceptance test at CERN, the extension piece is cut off and the on-stave end of the tube cleaned up ready for services connections after stave insertion.

Low-density core material Apart from the cooling structures and the close-outs, the remainder of the central portion of the stave core is filled with a low density honeycomb core material which is glued to the two face sheets. The honeycomb maintains the separation of the face sheets for good bending stiffness and ensures the stave has a sufficiently flat and robust surface to allow adhesive attachment of the modules without the need for excessively thick glue layers. Whilst the choice of honeycomb material is not critical, a high performance carbon-fibre based honeycomb with a cell size of about 6.4 mm has been selected.

Close-outs The stave edges are enclosed by end and side close-outs. End closeouts, normally made of engineering plastics, are used to mitigate against possible de-lamination of the core during handling in general and, in particular, against the effects extraneous forces applied to the cooling tubes. Meanwhile, pultruded carbon-fibre C-channel close-outs are used for the long edges of the core. The side close-outs are important in mitigating against the peel forces generated by the co-cured face sheets when the stave is cooled, form part of the mechanical interface to the global support structures and function as guide rails during stave insertion and support points during module mounting. The C-channel into which the stave locking points are glued has apertures cut into the vertical wall to allow the mounting bracket sockets to be installed during stave core assembly.

Stave Locators and Locking Points Staves are located onto the support cylinders via a minimal set of precision location features and a number of locking points. The position of a stave core on its support cylinder is defined in rφ, R and Z at the Z=0 end through a ball-and-cone arrangement with a Z-restraint from a fastener secured using a long rod with the appropriate hexagonal head for the fastener immediately after stave insertion. The angle of the stave relative to the radial direction is defined at Z=0 via a precision hole in a plastic (PEEK or LCP) locator glued into the free-edge of the stave core which slides over a tapered pin located in a bracket which is glued to the support cylinder. At Z=1.4m the free edge of the stave is located close to the EoScard to mitigate against any possible deformation of the stave as a result of stresses caused by movements in the services. Finally, the stave his held along the edge closer to the support cylinder in r*varphi* and R through 5 locking points. These bind the stave to the support cylinder and exploit the stiffness of the cylinder in maintaining the stave in a stable position. The locking points are formed from a bracket, which is mounted into the stave core, and a housing which is mounted onto the support cylinder. The position of the stave is defined by the V-shaped features in the bracket and housing are brought together through a side-ways force generated by deforming the housing through the rotation of a cam mechanism using a long circular rod terminated in a hexagonal shaft. The rod is inserted from the z=1.4m end and passes through the hexagonal holes in the five locking points. The rod is then withdrawn until the hexagonal rod sits in the corresponding hole in the cam mechanism, the rod is rotated to activate the cam. The rod is then pulled back a little further to actuate the next cam and so on.

10.2.2 Petal Core Design

Sergio

2 pages

The petal core is the equivalent to the barrel staves. It uses the same materials as stave cores. Here, the main differences are outlined. The petal core is wedge shaped, with the cooling tube approximately V-shaped as shown in Fig. 10.75. Each module in the outer three rings is cooled by a single length of tube, while the inner three modules – which have higher power densities – are cooled by two lengths of tube, similar to a stave.

Figure 10.75. Drawing of petal design showing the numerous hybrids. It is being discussed to avoid 4 hybrids in the innermost ring

A petal has fewer modules than a stave (18 cf 26) and most of these (14) have a single hybrid. This reduces the power load and servicing needs compared to a stave. Furthermore the wide-end of a petal is much wider than a stave. Placing the cable-bus under the modules adds significant unnecessary material. Instead, a cable bus will run down each outer edge of a petal, with the modules glued directly to the core face-sheets. On each side of the petal is an EoSthat connects to the cable bus on that side.

The cooling parameters are quite different between staves and petals. Gluing sensors directly to the core-facing slightly reduces the thermal impedance. The outer modules have lower power density than short-strip barrel modules, but with only one tube-section for cooling so that the heat path-length is roughly doubled. The inner most modules have higher power-density than short-strip

barrel-modules, but have two lengths of cooling pipe giving more area and shorter heat-path. Initial studies show sufficient margin to thermal runaway with CO_2 cooling at -30°C. Several prototypes have been made and measured.

Table 10.21 shows estimates for the radiation length of a single short-strip barrel stave as well as for a petal. These numbers represent best estimates based upon stave and petal prototyping and extrapolation to the use of expected lower mass components (e.g. ABC130 hybrids and titanium cooling pipes). For comparison, the current SCT radiation length excluding barrel or disk support is 2.48% for the barrels and 3.28% for the end-caps [13]. The lower expected radiation lengths are due to the high degree of sharing of support, power and services in the upgrade designs.

Barrel		End-Cap	
Element	% Radiation Length	Element	% Radiation Length
Stave Core	0.48	Petal Core	0.47
Bus Cable	0.18	Bus cables	0.03
Short-Strip Modules	1.08	Modules	1.04
Module Adhesive	0.06	module adhesive	0.06
Total	1.80	Total	1.60

Table 10.21. Radiation Length estimates for the barrel stave and end-cap petal. Power ASICs and the EOS are not included. The bus-tape for the petal has a lower value as the actual bus elements are very densely distributed at the rim of the petal while almost no tracks are underneath the sensors. These numbers have to be confirmed with a full petal design.

10.3 Electrical Concept incl. internal services and performance

In this section the details of the system-level components common to both stave and petal Local Supports are described. The detailed designs of these components differ only through geometric necessity when applied to staves and petals.

10.3.1 Optoelectronics

The optoelectronics for the readout will use the components developed by the *Versatile Link +* group and the associated lpGBT chipset (see Fig. 10.76). The optical links will use VCSELs and photodiodes operating at a wavelength of 850 nm and multimode fibre.

ASICs for optoelectronics For the data links (up-links) the lpGBT acts as a multiplexer, allowing for up to 14 input links at 640 Mbps. Therefore two lpGBTs are required per side of a barrel stave to accommodate the 28 HCCs. The data are multiplexed onto one high speed line and a Forward Error Correction (FEC) code is added. The data are scrambled to ensure DC bias. Allowing for the header and FEC, the resulting output data rate is 10.24 Gbps. The multiplexed data is sent to the laser driver lpGBLD10 which drives the VCSEL.

For the TTC links the optical to electrical conversion will be performed by the photodiode (PD). The PD signal is amplified and discriminated by the GBTIA. The lpGBTxwill receive the incoming data from the GBTIA and send out the Bunch Crossing (BC) clock, the R0 and L1 signals at maximum speeds of 160 Mbps. FEC is implemented in order to be able to correct for the

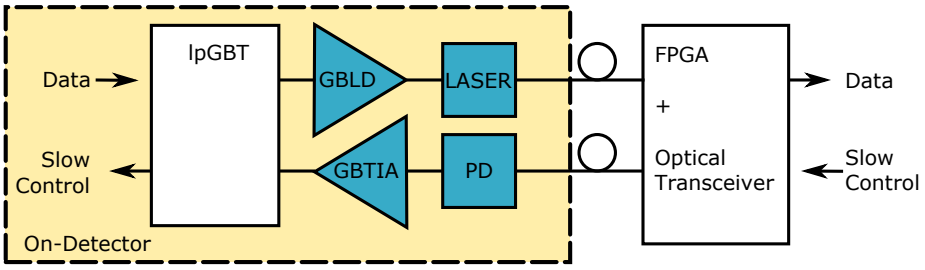


Figure 10.76. The optoelectronics readout chain. The on-detetcor items are inside the dashed yellow box. PD=photodiode. The functionality of the radiation tolerant ASICs is described in the text. The off-detector optoelectronics will use COTS components.

effects of the expected Single Event Upsets in the photodiode [14]. The lpGBTxis a development of the existing GBTxchip (ref xxx) to work at higher data rates and survive the radiation doses for the phase II upgrades. The lpGBTxis therefore being designed in 65 nm technology.

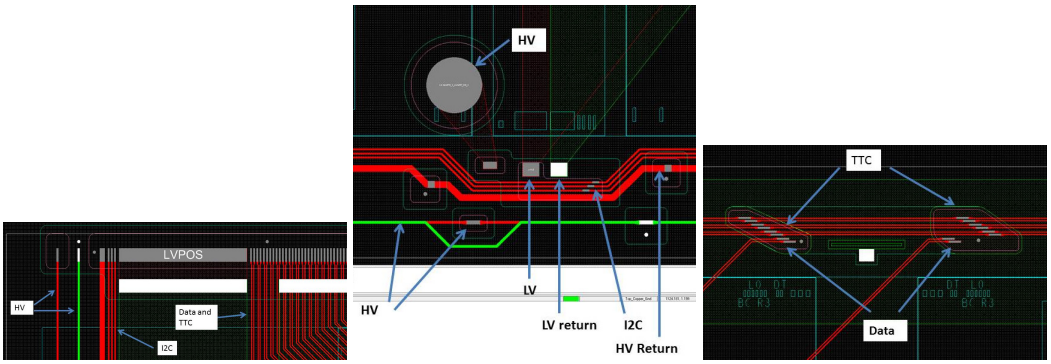
The incoming TTC signals will be received by the existing GBTIA chip. The laser will be driven by the GBLD10+ ASIC. This ASIC is under development but existing prototypes have achieved the required speeds [15]. Array drivers are being develped in 65 nm technology which will result in lower power consumption.

Optoelectronic Packaging The GBLD10, the GBTIA and the corresponding lasers and photodiode will be packaged in one transceiver module (lpVTRx) by the Versatile Link + group. The VCSELs and photodiodes will be of the same type as used in the existing VTRx modules as these have been demonstrated to be sufficiently radiation tolerant [16]. Different options for the packaging are being developed but they all very much smaller than the existing VTRx and are very low profile. The number of Rx and Tx channels can be adjusted to match the user requirements and it is currently foreseen to use two TX and one Rx channel in a package. Only prototype lpVTRx will be available at the start of ATLAS production. Therefore the lpVTRx will have an electrical connection, which will allow for the production of a simple PCB to replace the lpVTRx during stave and petal bus tape QC.

10.3.2 Bus-tape

The bus tapes provide all the low voltage and high voltage power from an End of Structure (EoS) card at the end of the stave or petal to the modules. The bus tape provides all the high speed data links to (from) the modules from (to) the EoS. The bus tape also provides I^2Ccommunication between the EoSand the AMAC chip on the power board. The modules are glued directly onto the bus tapes.

Tape Design Identical technologies will be used for the barrel stave and petal bus tapes and the differences between the two types of bus tapes will only be those dictated by the different geometry. The bus tapes are laminated from two layers of adhesiveless copper/polyimide. The tapes are designed to have very high reliability and minimum material. They therefore use adhesiveless copper/polyimide tapes and all connections to the modules and the EoSare made using standard



(a) EOS region (b) Module power connection area (c) Module data connection area

Figure 10.77. Details of the different bonding areas on the bus tape.

aluminium wire bonding. The copper thickness used is 17 μm (1/2 Oz Copper) and the polyimide and glue layers are both 25 μm thick. Openings are cut out around pads to allow standard Ni/Au plating for the exposed pads (but not the full length of the tracks). The separation between exposed HV pads and neighbouring pads is greater than 1.8 mm (0.8 mm if the tracks are underneath a cover layer) to respect the Laboratory Underwriters[3] specifications. As the same copper layer is used for high speed tracks and for power, the minimum thickness was selected in order to meet the voltage drop requirements without exceeding the available width. The voltage drop requirements for the low voltage return for the stave bus tapes is satisfied by the use of a 60 mm wide trace.

The critical issue in the tape design is to provide good quality data transmission over the full 1.4 m length of the tape, without adding too much material. A differential microstrip configuration was selected for these lines. A standard design would use wide tracks to lower the resistive loss and a thick polyimide layer to ensure the required 100 Ω differential impedance of the lines. There is insufficient space for wide lines and we require the use of thin layers of polyimide to minimise the material and the thermal impedance. The widths of the tracks is set to 100 μm and the gap between the two lines of each differential pair is also set to 100 μm. In order to minimize cross talk the gap between neighbouring pairs is set to 150 μm. These dimensions are approximately the largest that are compatible with the stave width.

The layout of a *prototype* bus tape for a 13 module stave is illustrated with three images of the design; fig. 77(a) is for the EoSregion showing the bond pads to connect from the tape to the EoS, Fig. 77(b) shows a region at the end of a module and the bond pads for the power connections and Fig. 77(c) shows the other end of a module and the bond pads for the data and TTC connections.

The quality of the data transmission was studied using FEA calculations and experimental measurements of S-parameters. The losses for the transmission lines in the relevant frequency range are dominated by the resistive loss in the lines

$$f = \exp\left(-R/2Z_0\right) \tag{10.3}$$

where R is the line resistance (taking into account the skin depth) at a given frequency and Z_0 is the characteristic impedance. Therefore we need to achieve a differential impedance of close to

[3] www.ul.com, UL 60950-1.

100 Ω both to minimize reflections and lower the resistive losses. In order to achieve acceptable resistive losses without adding any extra polyimide layers, the stackup shown in fig. 10.78 will be used.

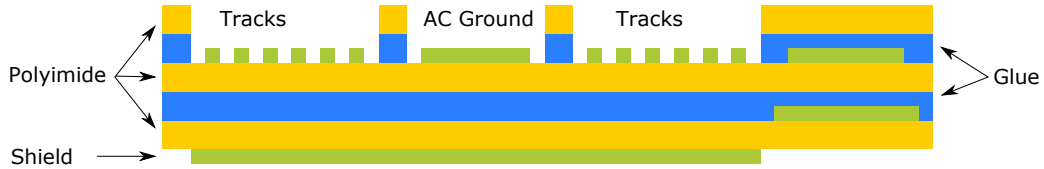


Figure 10.78. Sketch (not to scale) to illustrate the stackup of the bus tape, showing the three copper layers (green), three polyimide layers (yellow) and the glue sheets holding them together (blue).

The bottom copper layer will be in good contact with the carbon fibre skin. Copper strips will be used in the EoSregion to allow the carbon fibre to be connected to the low voltage return, thus allowing the copper strip to act as the ground for the high speed transmission lines. There will also be data and clock line for the I^2Ccommunication between the EoSand the AMAC chips.

10.3.3 Data Transmission Tests

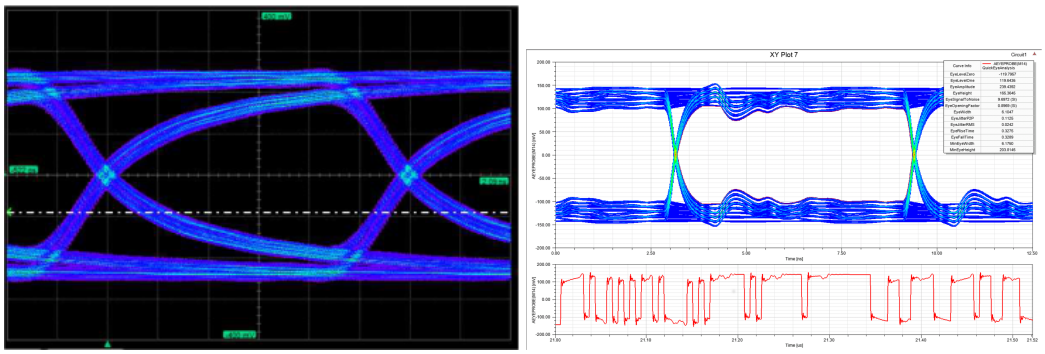
The expected performance of the data transmission on the bus tapes [4] was studied with FEA calculations [5]. The calculated S-parameters were used to simulate 'eye-diagrams' to assess the signal integrity. This indicated that clean eye-diagrams could be obtained for the point to point data links operating at 640 Mbps. Experimental measurements of S-parameters were made on a 1.4 m long test tape using a network analyser. The measured S-parameters were then used to simulate eye-diagrams for Pseudo Random Bit Stream (PRBS) data. The resulting eye-diagram for the location at the furthest end from the source (which has the maximum attenuation and dispersion) is shown in fig. 79(a).

*** still to be done *** Direct measurements of the signal integrity were performed on a test tape with test chips containing drivers and receivers of the type expected in the HCC ASIC. The directly measured eye-opening confirmed the expected clean eye and finally Bit Error Ratio (BER) measurements confirmed that the BER was lower than the required maximum value of 10^{-12}. Improvements in data quality were also demonstrated using 8b10b encoding which removes the effects of the slow tail of the rise time [17] and by using pre-emphasis. The HCC will allow for the option of using 8b10 if required and for pre-emphasis. **********

The TTC transmission uses a 40 MHz clock and 160 Mbps data lines. The critical issue here is that each of the 28 HCCs on a barrel bus tape represents a capacitive load and therefore generates unwanted reflections. This causes the transmission to fall away rapidly above a frequency of $\sim$ 500 MHz and the reflections to increase. The worst reflections were for the location nearest to the EOS. The FEA calculations suggest that the reflections could be reduced by using source and end termination of the lines. The predicted eye-diagrams for the location closest to the EOS had reasonable eye-opening at 160 Mbps as shown in fig. 79(b).

[4] The studies used barrel bus tapes as they are significantly longer than for the Endcaps.

[5] Using HFSS from ANSYS.



(a) Data eye diagram (b) TTC eye diagram

Figure 10.79. Eye diagrams resulting from a simulation based on measured S-parameters, for 640 Mbps (Data) and 160 Mbps (TTC).

The other effect of the capacitive loads was to increase the dispersion so that the rise and fall times were slowed down significantly for the furthest location from the EoS. However the edges were still sufficiently rapid to allow 160 Mbps data transmission.

The measured S-parameters confirmed the rapid decrease in the transmission and increase in reflection at frequencies above 500 MHz. *** still to be done *** The signal integrity for the TTC lines was also studied using the test driver and receiver ASICs. The measured eye-diagrams were studied and compared to the predictions. The BER measurements confirmed that a BER below 10^{-12} could be achieved. **********

10.3.4 Grounding and Screening

Need to mention GND star point on the stave, module ground referencing?[JD]

The lowest copper layer in the stack acts as the ground layer for the data transmission lines. This copper layer will be in electrical contact with the carbon fibre skin after the co-cure process. As the contact area is very large, this is expected to produce a low resistance connection. The carbon fibre skin will be connected to the low voltage return at the EoS using a wide copper strip included in the co-cure process. The carbon fibre will also be connected to the low voltage return at the opposite end of the stave ('z=0') using a copper tab included in the carbon fibre during the co-cure. This then satisfies the overall grounding and screening requirement to have all conducting surfaces grounded. There will be large currents flowing in the low voltage return on the tape. We therefore have an additional wide ground referencing track on the bus tape. This track is connected to the low voltage return near the EoS. Capacitive connections are used from this track to each hybrid, thus providing a clean AC ground.

10.3.5 End-of-Substructure Card

The End-Of-Substructure (EoS) Card is the interface between the Stave/Petals or a chain of Super-Modules with the off-detector electronics. The EoSSchematics are common, however the layout will be different according to different geometrical requirements in the barrel and end-cap sub-structures.

The EoSwill host two lpGBTxserializer/deserializer ASICS and a Versatile Link tranceiver VTRx. For the incoming TTC optical links the optical to electrical conversion is performed by the VTRx and the data is deserialised by the lpGBTxand the 40 MHz clock, the Level-1 trigger and the control data are distributed to the HCCs along the stave/chain of supermodules. The 640 Mbits/s data from the HCCchips is serialized by the two lpGBTxand converted to optical by the VTRx. If it is decided to employ redundancy, duplication of these components will be required. Part of the DCS information with be handled by the GBTSCA chip. The EoSwill also host filters for the LV/HV. Finally it will host a series of temperature, humidity , voltage and current sensors that will provide inputs to the DCS via the GBTSCA chip.

10.3.6 Interlocking Scheme

For the DCS & Interlock scheme, an entirely independent scheme isn't feasible due to cabling constraints. To ensure detector safety an independent set hardware interlocks will however be necessary. In order to minimize the number of dedicated cables required, the interlock will be based on temperature readings on the inlet and outlet of the cooling pipes for each stave/supermodule. Temperature readings from the modules will be made available in the data stream through the HCC. Additional temperature and humidity data will be fed into the GBTxso that high granularity DCS data will be available. As an additional safety feature, front-end ASICs could have a scheme in which they sense temperature and power off automatically if they detect over temperature.

10.3.7 I/O, Cables and Connectors

For the DCS we foressee to have a least three digital I/O to controls running as a bus to each module. In terms of logical cable units, we have per EoSone LV and one HV cable, the high speed fiber link plus the external DCS information.

10.3.8 DCS (on-detector)

Tony? Should we get input from Peter/Ash here or do we have everything?

Embedded NTCs, Monitoring through data stream for everything else?

There are two NTCs on the outlet pipe of every stave and petal. These are wired individually and will be used to define a hardware fail-safe interlock which will ensure that the cooling is operational before any power can be applied. Much more granular DCS data will be read out from the HCCwhich will merge DCS data with the physics stream. This will allow to read voltages, currents and one NTC per hybrid. We are also investigating the use of the AMAC chip to acquire DCS data which could be transferred out via $I^2C$to the lpGBTx, not requiring powering of the HCC. The options include an NTC on the power board, current and voltage measurements for the hybrid and power board temperature.

10.4 FEA and thermo-mechanical performance for petals and staves; deformations

Graham/Sergio?

3 pages

Detailed three dimensional thermal FEA models have been developed [**?**] that predict the temperature distributions across the sensor, readout chips and local support structures. These address

major concerns during normal operation such as thermal runaway headroom (section n ref. subsection Requirements and Overview, subsubsection Thermal Performance above), sensor leakage current (hence shot noise) and cooling requirements, that depend in turn on radiation damage to both the sensor and readout chips. They also allow temperature estimates outside normal operation, for instance during "beam off" conditions and initial detector commissioning at elevated temperature. The models concentrate on evaluating the conductive thermal paths to the cooling pipes and heat removal by the evaporating CO_2: heat exchange with ambient (by convection and radiation) has been considered, but in most situations is a negligibly small effect. The FEA predictions will be verified by comparison with stave and petal "thermo-mechanical" structures currently under construction.

FEA models of the barrel stave and end cap petal differ mainly due to their geometry and readout chip arrangements, c.f. fig 10.80.

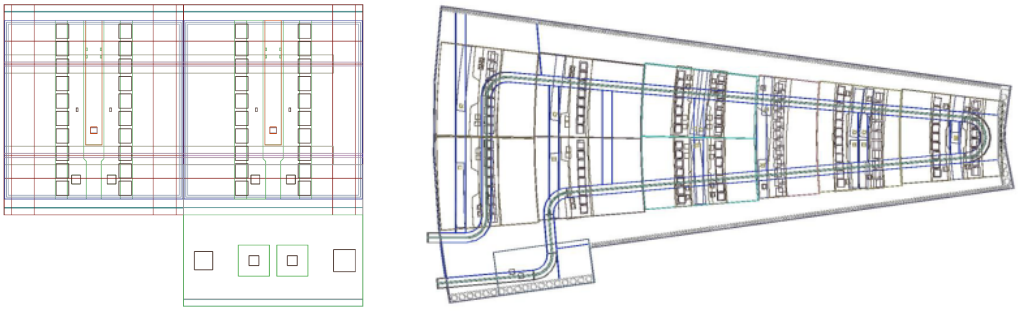


Figure 10.80. Top view of the FEA simulation models: Whilst the stave behaviour is very uniform along its length and can therefore be estimated to be better than the EoS region (simulation model on the left), the petal is a non-uniform structure and needs to be fully simulated.

Since the stave has a predominantly periodic structure, it is sufficient to model a short segment at its end, where there is a coincidence of slightly higher radiation level, thermal load from the end-of-structure chips and reduced cooling efficiency (due to the insulating break). Separate models are required for the inner radius (short strip) and outer radius (long strip) barrels. By contrast, the end cap petal spans the radial extent of the strip tracker with an irregular module geometry: here the FEA model is constructed to describe the full petal. All petals are of the same design, and the FEA is usually run for conditions expected at the end of the tracker, where the predicted radiation level is highest.

10.4.1 Thermal Conductivities

Thermal properties used as input to the FEA are summarised in Table n.

Table: Thermal Conductivity Input

Apart from minor variations they are the same for the Stave and the Petal, in particular along the conduction path between sensor and coolant as described in section ref. subsection Requirements and Overview, subsubsection Thermal Performance . Evaporative CO_2 cooling is simulated as a convective film between the pipe wall and fluid, at its evaporation temperature. The convective heat transfer coefficient (htc) varies around the cooling loop and is computed using the stand-alone

package CoBra [ ] ref. CoBra , for the appropriate stave or petal thermal loads. The cooling pipe inner diameter is currently assumed to be 2 mm, although calculations are in hand to optimise this.

Conductivity values for the foam and co-cured facing have been measured by ATLAS institutes and are so far consistent with manufacturers' specifications. Thermal conductance through the various layers, of which the most crucial is the interface between the graphitised foam and cooling pipe, have also been measured. Where thermal performance is sensitive to these they will be monitored as part of the QA/QC process. Read-out chip temperatures depend on the thermal path through the printed circuit boards. In particular, the DCDC converter (that steps down the input voltage to power the ABC and HCC chips) is a localised source of power dissipation that is particularly important at the TID peak: care is being taken to model the structure of the pcb (and compare with measurements) so as to correctly predict the DCDC chip temperature. Certain material and design variants are under study and their effect simulated in the FEA models; these include the use of UV cure glue for chip attachment (for increased assembly speed) and a reduction of the glue area between sensor and bus (in order to reduce its mass).

10.4.2 Thermal Loads - performance at the TID peak

Here we assume that the chip power dissipation is given in earlier sections. e.g. Section 8.2 "1.5 V/4.0 A (max)". Thermal loads are simulated for power dissipation by the readout electronics ref. subsection Hybrid Design and Prototypes, which is relatively independent of temperature, and for the sensor leakage power, that increases exponentially with temperature, as described in section ref. subsection Requirements and Overview, subsubsection Thermal Performance . Sensor power dissipation is simulated as Joule heating, by assigning an electric potential difference across the sensor thickness together with a specific electrical conductivity: the conductivity is input as a table (for interpolation) that describes the expected leakage power dissipation with temperature. Hence the FEA correctly accounts for temperature and power variation across the sensor area (albeit not through its thickness). At locations where radiation levels are highest, ionisation damage to the CMOS read-out electronics is expected to peak early in the life of the detector, when the sensors are relatively un-damaged and leakage currents are consequently low. However, the read-out heat itself is predicted to result in large temperature gradients and elevated chip temperatures, particularly in the regions of the DCDC converters. Figure n figure: T plots at TID peak shows predicted temperature distributions based on the present, limited understanding of the ionising dose effect: detailed studies are in progress, to quantify the irradiation damage and to understand convective corrections and design strategies that will reduce its impact.

10.4.3 End of life: Thermal Runaway

The danger of thermal runaway is greatest at the end of operation where both the leakage current and required bias voltage are a maximum. By that stage, at the locations most vulnerable to runaway the excess read-out power due to ionisation damage will have reduced to a negligible level. At the maximum expected sensor power (allowing a factor x2 on predicted fluence) the FEA finds stable temperature solutions for both the stave and the petal sensors (Fig. n) figure: Sensor T plots at 3000 fb^{-1}. Temperature variations are smaller here than at the TID peak and although localised peaks are evident, runaway will occur only if the temperature dependence of heat generated over an area comparable to the sensor exceeds the thermal conductance of the local support. FEA results

for the evaporation temperature crtitical for runaway are given in table n. ref. Thermal Performance Summary Table. The behaviour of the average temperature of a sensor can be estimated quite accurately from an analytic model in terms of just two thermal resistance parameters derived from the FEA ref. Beck&Viehhauser . This allows a simple prediction of quantities of interest, such as runaway headroom, shot noise and required cooling power. It will be further used to understand the combined effects of ionising dose and fluence as these vary with integrated luminosity and location on the detector.

10.5 Module Loading

Jens/Sergio/Susanne?

Moving Microscope/Bridge concept, referencing on Stave/Petal core and module, survey requirements post-mounting

3 pages

10.5.1 Requirements

The required outcome of the module loading is an accurate placement of modules, with particular focus on the axis perpendicular to the long stave axis (in plane). The basic requirements also include electrical functionality, in particular thinking of high voltage connection on the backside of the sensor, as well as thermal contact for cooling away the heat generated in the modules. The requirements on module alignment are derived from a requirement on hermeticity measuring 1GeV tracks. The software based alignment allows for picking up most misplacements, as long as enough overlap is given between modules from the same barrel radius, allowing to constrain the total circumference. This overlap criterion is less stringent than the aforementioned hermeticity, hence automatically fulfilled. Placement precision should be to within 100 μm (both axes) of where a module is meant to be. Post-placement, a metrology is to take place, that will give a better knowledge of the modules relative position to the stave, allowing to seed the alignment.

One of the main goals of the module loading is to provide a good cooling connection by creating close contact between the module backside and the surface of the support structure. The glue used for this process should not only withstand radiation, but also be thermally conductive. Current prototyping uses SE4445, technically speaking a two component thermal compound, based on a large Alumina filler fraction. Tests are on-going to qualify whether this glue is suitable for production.

Part of the module loading procedure is the electrical connection of the stave bus tape to modules and End-of-Substructure card by means of wirebonding. The mounting has to provide an assembly that is not too flexible, allowing to apply appropriate pressure to the wirebonds for attachment.

10.5.2 Module Loading Tooling

The setup for module loading is comprised of two major components:

- An optical table with a moving microscope that can precisely locate coordinates on the table
- Module loading bridges, which can be mounted on the table in given locations and allow for putting a module down onto a stave core in an adjustable location.

A photograph in Fig. 10.81 shows the stage system on its granite table.

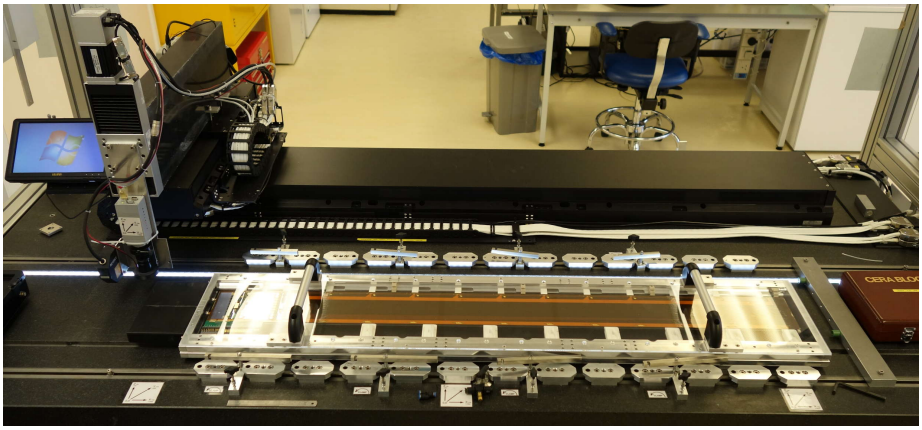


Figure 10.81. A photograph of the current barrel module mounting system, including the thermo-mechanical test stave in its assembly frame.

10.5.3 Optical Table

The microscope is currently set up to show a 2.7x2 [mm] sized area through a camera projecting 2x2 [um] fields onto each pixel of the camera. The field of view had initially been chosen smaller, but caused trouble in locating items on the table. A larger field of view allows for a much quicker approach and shrinks the apparatus significantly.

The microscope is mounted to a granite table, using X, Y and Z stages, allowing to locate any point within a region of 1500x300x150 [mm] region to O(10 um) accuracy. To deliver that accuracy, a monitoring system is needed to compensate for possible out-of-axis movements, in particular on the longest (X-) axis.

Explanation of the monitoring system (get this fixed up soon)

Explanation of the calibration

10.5.4 Module Loading Bridges

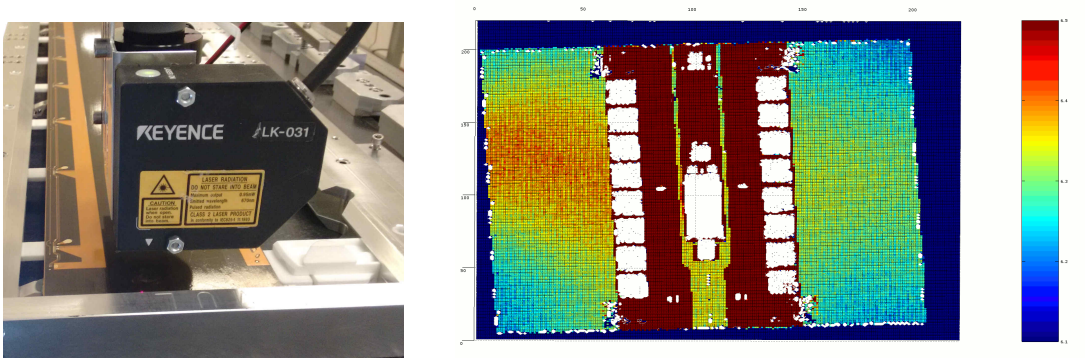
The module loading bridges are designed to move a module on the stave surface. They allow translation and rotation of the module to adjust its final position on the stave. The current design employs three fine threaded screws to do three translations, two along the staves z-axis (if screwed in opposite directions allowing an angular adjustment), one along the R·φ direction. An iteration is planned, where rotation and translation are fully decoupled, but requires testing. Each Bridge is fitted with a pickup tool that serves to hold a module underneath a Bridge. The pickup tool allows for a soft touchdown on the module (with silicone vacuum suction caps), rotational and lateral placement, whilst picking up any vertical non-conformities.

Method of Module Loading Modules are glued to their corresponding stave by applying a pattern of SE4445. A mask of film adhesive is used to apply a known thickness (~150 um). Till the glue is at least partially cured, the modules are held in position using the module loading bridges. The pickup tools on these bridges touch down on the stave surface, next to the sensor of a module, therefore defining the glue thickness.

10.5.5 Post Mounting Survey

To allow for a quick alignment, we aim to provide a survey of module locations and geometry after they have been loaded to the stave. This will incorporate re-measuring all module fiducial positions with respect to the stave/petal coordinate system. Once those are established we also intend to measure the out-of-plane geometry of all loaded modules. This will allow for alignment to run based on a fully constrained large object (one stave- or petal-side) and quickly turn around precise alignment coordinates for those.

Repeatability of the stages used for module mounting will allow for a total location accuracy of <20um in all directions. This is well below the sensors resolution and should therefore suffice for an initial alignment attempt. The out-of-plane coordinate will be measured using a laser range finder (or confocal probe, depending on availability) and should be precise to <10um.



(a) Laser range finder above a prototype stave. The red measurement dot is visibile.

(b) Exemplary measurement, colour scale in mm with an arbitrary offset. The module shows a sensor bow of about 350 μm out of plane.

Figure 10.82. Measurement system and a representative example of a measurement above a module.

10.6 Quality Control in Production

Carl/Dave/Graham?

1 pages

10.6.1 Quality Control in Production

The electrical continuity of all tracks will be measured with a robotic tape tester. The system compromises two heads on a gantry system. Each head contains a camera which can take photographs of fiducials on the tape. Image analysis software then determines the fiducial centres and after the system is calibrated this allows the tester to move to any required pad. Each head also contains a probe to allow the open and short circuit testing to be performed. A photograph of the prototype tape tester is shown in Fig. 10.83.

After checking for continuity the tape tester will check for short circuits between all neighbouring networks. In order to confirm the reliability for high voltage operation, the tape tester will also measure high voltage insulation resistance at a voltage greater than 500 V. The actual value used will be determined after tests on prototypes. The tape tester will perform simple length measurements to check that the module to module length is as expected before and after the co-cure

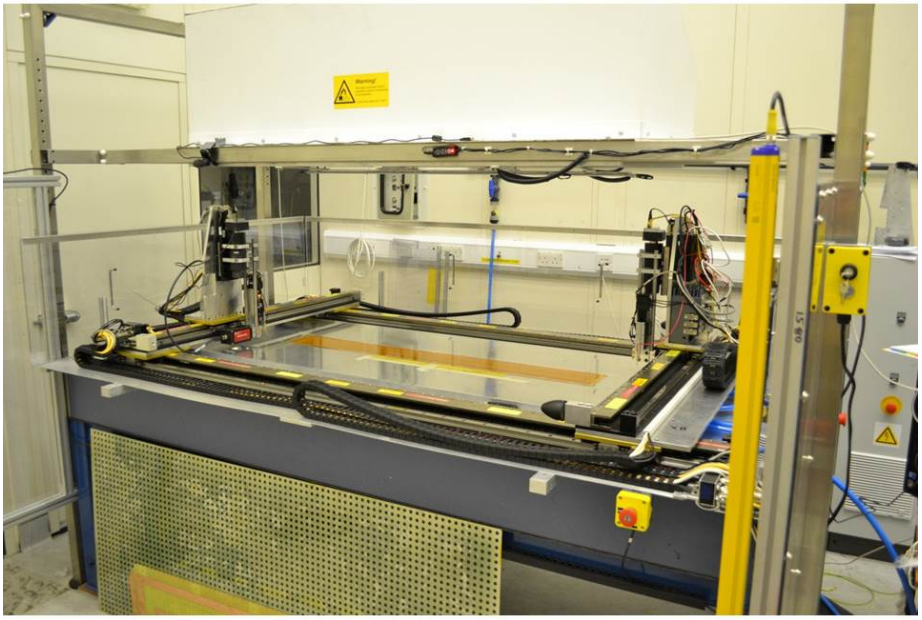


Figure 10.83. Photograph of the prototype robotic tape tester.

process. A prototype robotic tape tester has been built and used to test prototype tapes built in industry and by Oxford. The tester was able to successfully measure the electrical continuity and open circuits for these tapes.

In production an optimized version of this tape tester will be used for the Quality Control (QC) for all tapes. This QC step will be carried out at three stages of production:

1. On receipt of bus tape from industry.
2. After co-cure of tape to carbon fibre skin.
3. After the co-cured tapes are assembled into a full mechanical stave.

10.7 Timeline of reviews

Volunteers?

2 pages

10.8 Test results (incl. rad-hardness where appropriate)

This section was delivered just after electrical concept - Feeling is that people wanted this to be GBT/Opto/DC-DCconverter test results, but I am not quite sure, clarifying soon

3 pages (depending on how we plug it in)

11. Global Support

Editor: Abe Seiden
Chaser: Marcel Vreesvijk
Number of pages to write: 20
Scope of chapter:

- *Overview (Requirements and conceptual design)*
- *Details of the design Global support and on-detector services support*
- *Barrel (Stave support)*
- *End-cap (Petal support)*
- *Planned QA during production*

The text below is directly from the IDR and should be revised?[IMG6]

The Strip Structures are the structures used to locate and support the Local Supports and the inner (pixel) detector elements from the Outer Cylinder (OC), which is the large (7 m long by 2 m diameter) CFRP tube that the whole of the ATLAS ITk is built within. These structures are very closely linked with the common mechanics project; the common mechanics group is presently developing the exact form of the strip structures following is somewhat uncertain. The Strip Structures will largely be CFRP structures, in the barrel they will be formed from cylinders and in the end-cap a space frame with an inner radii tube. Where possible interfaces will be glued rather than bolted. The individual parts of the system will be made preferably from cyanite ester glues with the final assembly done with cold (room temperature) cure epoxy.

11.0.1 Barrel Structures

Since the LoI, the work on the baseline concept where tilted staves are mounted on 5 concentric cylinders has continued. These five concentric cylinders are to be connected together at the two z extremes with interlinks. The interlinks will either be ""one per stave"" or in eight discrete locations (top, bottom, left, right and mid-way points). We believe that one interlink per stave is both more compact and easier to integrate, but may not be as structurally efficient as eight discrete interlinks. ITk common mechanics works with the concept that the detector elements will be structurally independent. With this in mind, the barrel structure is designed to interface to the outer cylinder with a kinematic mounts at four points (3 and 9 o'clock at either end of the barrel). Should this concept become inadequately stiff we also have a backup where the outermost barrel can connect to the OC with individual stave interlinks interfacing to the OC around the full circumference.

Figure 11.84. Drawing of the barrel structure.

Although the design of the cylinders is incomplete we have developed a preference for single skin cylinders with reinforcement rings along the length in specific locations (up to 11 rings and

[6] IMG: April 4 2016

two end flanges). Presently, there is a reasonable theoretical understanding of the performance of the proposed cylinder and interlink designs, as we move through to the TDR, we need to understand both how well the designs can be realised in manufacture, and how performant the real parts are.

The end-cap structure starts with a central cylinder. From this cylinder at each of the disk locations two x,y planes of blades extend $\sim$ 50 mm apart in z. These provide the structure to insert petals between, which forms a ""disk"" of petals/modules. On the outside of these blades, there are rings to support the high radius ends of the blades; these rings are interconnected along the detector by more rails that also serve to support the end-cap services. As with the barrel, each end-cap sits on four kinematic mounts at 3 and 9 o'clock at either end of the sub-detector. The stiffness in the z-direction of this structure is currently not adequate for the required performance. Therefore it looks to be necessary to add a bulkhead disk between the outermost two sensor disks to improve the structural performance.

Figure 11.85. Drawing of the end-cap structure.

The end-cap structure design is not yet as mature as the barrel structure, and whilst considerable analysis has taken place, it has not yet looked at CFRP layups, manufacturability or how well a built structure would correlate with the studies.

11.0.2 Interactions with the Pixel Detector

As the pixel detector sits within the strip detector the mass of the pixel detector needs to be supported either on the strip detector or have structural fingers that reach around the strips. Our baseline is that the pixel mass will be supported by the strips. Aside from basic mass assumptions this interface has not yet been considered. We will be unable to improve these approximations until the pixel project has a more mature design. It should be noted that the strip structures need to know more than just the pixel masses. The strip structures also need to understand the integration scheme for the pixels to ensure the interfaces are adequately designed.

Open questions that are key to structure designs

1. Finalisation of alignment and stability requirements that will finalise structure specification.
2. Castellated vs tilted, although the baseline design is on tilted staves; there is some suggestion from simulation that there are some benefits from castellated, this needs to be closed one way or another.
3. Understand the pixel design, masses and integration plans.

12. Integration of the ITK Strips

Editor: Abe Seiden
Chaser: Ian Wilmut
number of pages to write: 20
Scope of chapter:

IW thoughts on structure

- Integration process stave/petals into structures
  - Barrel plans - IW, SY, GV
  - Endcap plans and process - Carlos, Marcel
- Service modules (on-detector)
  - Introduction, including description of concept and common ground - IW, probably should write this first...
  - Cable count etc. Pepe?
  - Description of barrel service module, work done and work to do - IW
  - Description of EC service module, work done and work to do - Carlos? Marcel?
- Finite element analysis
  - Barrel service module thermal performance and optimisation - IW - where does Geoff Taylor fit into this? perhaps he should do this...
  - Endcap service module thermal performance and optimisation - Carlos?
  - Thermal model of ID endplate aspirational - not started yet, may be very brief need to discuss with Georg.
- Thermo-mechanical measurements
  - TM barrel stave - stave 250 measurements, Oxford - RBN
  - TM barrel stave - stave 130 what will we have by TDR - Jens

12.1 Local support to structure and system integration

This section will describe the process of assembling the detector subsystems from the constituent parts. Generally the process is not influenced by location of the activities, but the intent is that the barrel will be integrated at CERN and the endcaps in DESY and NIKHEF.

12.1.1 Barrel Integration

Introduction and Summary of process The Barrel will have all the staves end inserted once the barrel structure is fully assembled in the Outer Cylinder. The Outer Cylinder (OC) is assumed to be sitting in a cradle (possibly the cradle that will be used to lower the tracker into ATLAS) and we assume we will have access into the bore of the OC for 2 personnel at once. We presume we will be able to populate the barrel region from both ends simultaneously. The staves will be slid into the barrel structure one at a time transferring them from a transport frame to the structure. This process will have dedicated tooling (detailed below) once at least 8 staves are in place in a keystone arrangement a barrel service module will be installed that covers at least 8 staves and routes the services up in R to R_{max} and then along in Z to Z $\approx$ 3.5m where the services will pass out of the tracker volume and be terminated in a patch panel. The staves that are now connected can be tested in situ. It remains to be decided exactly how many rounds of closing and then testing will need to happen during the build, this will be a balance of risks and schedules. Once all the staves have been inserted the ITk will be ready for the insertion of the Strip endcaps.

Assembly of structures blah blah

Insertion of staves in to barrel structures blah blah

servicing of barrel staves blah blah

12.1.2 Endcap Integration

- Carlos/Marcel

Introduction and Summary of process blah blah.

12.2 Service Modules

12.2.1 Introduction to Service Modules - how they work and why

The service design for the strip tracker has been motivated by our experiences with service installation for the ATLAS SCT. There, all services (fibres, cooling pipes and electrical cables) were installed individually either into service channels on the calorimeter wall or onto the OD of the endcap support structure. This design resulted in a sequential service installation due to the limited accessibility and the large number of individual services. It resulted in a lengthy installation and when problems were encountered led to ad-hoc modifications of the original service design. The exit of the services from the SCT barrel and endcap thermal enclosures were badly designed and resulted in a large leak rate from the ID, no overpressure has ever been possible on the SCT volume.

For the Tracker upgrade we are pursuing a model where pre-fambricated units of services (service modules) are preseneted tothe structures, these units carry all the services for a number of

staves or petals, and are intended to be pre-fabricated and pre-tested with no facility included to allow in-situ rework. The decision described in xxxxx to interface one stave/petal as the smallest detector unit has dramatically reduced the service count compared to that in the SCT. Whist this has been essential to reduce the service cross section, there is still a very considerable service count no manage.

12.2.2 Barrel Service Modules

Introduction For the Tracker Upgrade we have developed pre-fabricated, standardised and removable service modules, each of these is installed as one unit containing all services for 1/n th (n probably being 16, 24 or 32 - 24 is the present baseline, but any change in layout may change this figure) of one end (Figure 12.86). These comprise cooling pipes and associated manifolds, electrical cables, and optical fibres, at one point it was mooted that they might contain the optical converters if they need to be in a lower dose location, this looks unlikely, but remains possible. The service module would also contain well-defined internal electrical ground connection for all metallic surfaces (in particular cooling pipes) and a common ground connection to the thermal enclosure. The off-detector end of the service module is part of the thermal enclosure and contains all necessary feed-throughs. Performance of the gas and thermal seals will be fully qualified before installation. The most challenging area of the Service Module to implement reliably will be at the detector end of the complexity of weaving the services from a rotational to mirror symmetric arrangement.

Figure 12.86. Barrel service module with key elements labled

Service module body The service modules are self-supporting to facilitate installation. At the same time structural elements of the service module are low enough volume to not significantly reduce the volume available for services. The service module body is proposed to be made from folded Aluminium 0.5mm thick, if the geometry would need to be more complex the option is retained to fabricate from CFRP.

Off-detector patch panels Patch panels at the end of the ID will allow electrical connectors to exit radially in the region of the cryostat chamfer.Opto will exit longitudinally, and cooling radially in a higher Z position that the electrical services. The whole patch panel will be kept outside the endcap radii to ensure no reforming of any services are needed to install the strip endcap. All connectors will be sealed into the patch panel, with the seal qualified as part of service module production, so that just the duct needs to be sealed into the ID during ID integration.

Cooling services Our preferred joining technique for all joints inside the thermal enclosure is welding to achieve low-mass, reliable connections. All connections within the service modules are made before integration into the Outer Cylinder. Within the service module there will also be some vacuum brazed assemblies which are welded onto the rest of the tubes. It is presently expected that the electrical insulated breaks will be vacuum brazed (and will also transition pipe diameter), as will the pipe manifolds, the termination of the capillaries may also use a vacuum braze process. Service module welds could use any welding technique (EB, Laser, TIG etc.), but our preferred

option is orbital TIG. At the detector end pipes from the service module terminate short of the local supports . The connection from the detector to the service modules will be made by a short patch pipe, which will be cut to length and shaped to the actual end positions during the barrel integration. This short patch pipe will be connected using orbital TIG welding. The routing of the patch pipe, and the adjacent sections of the pipes on the service module and the local support, will prevent stress transmitted onto the staves and will allow access for the orbital weld head. The probability of a successful joint at this stage is improved if pipes of similar parameters are joined. We therefore propose that the transition from the on-detector pipe parameters to the service module pipe parameters shall be part of the on-detector cooling pipe assembly, and be qualified there.

At the off-detector end of the service modules the pipe termination is not yet finalised as it depends on the type 2 (end of the cyostart) service design that is not yet finalised - our expectation is that it will either be a bare pipe to be orbital welded or something similar to a VCR bulk-head connector.

We believe that manifolds reducing the number of cooling connections before the ID ends by about a factor 1:4 to 1:8 are a good compromise between the space needed for connectors and pipes from there to PP2, and the risk of damage that will incapacitate many modules. A 1:4 manifolding scheme could would result in the loss of 8 staves 112 module from a fault in the circuit. These manifolds will be part of the service modules.

For the barrel strip detector each service module will connect on average to 3 short strip and 5 long strip local supports (1/24th segmentation). It is believed that the difference in power load on these diferent arms of a manifold will not cause any issues as the pressure drop is dominated by the capillary. A diagram of the cooling pipe connections within a barrel strip service module is given in Figure xxx.

Power and DCS cables Cables are standardised and slightly over length at the detector end of the service modules with the surplus being lost in routing. The cables have a decoupling capacitor between each line and the system ground at PP1. A diagram of the electrical services within a barrel strip service module is given in Figure xxx.

Optical services The optical conversion of the module sdata signals will happen on stave. However, as there is a small chance the final radiation dose in the end of stave region is too high for the opto convertors space is retained in the service module that would allow the opto convertor to sit in the service module if required. The three options that have been considered are shown below with option 1 being the baseline. Option 1: Optical conversion on local support. In this case at the detector end single fibres with over length would connect to the local supports. These fibres would need appropriate protection during installation and in-situ. The single fibres would get ribbonized within the service module and terminate at MT8 or MT12 ribbon connectors at the ID end. Option 2: Optical conversion within the service module. Electrical cables (micro-coax or twisted pair) with over length would connect to the local support at the detector end. These would run to the opto-converters within the service module, where conversion takes place. The opto-converters would be located so that they are accessible form the outside of the service module, preferably at the side of the service module, which becomes the radially inner wall in the final position. Fibre ribbons would then run within the service module to MT8 or MT12 ribbon connectors at the off-

detector end. Option 3: Optical conversion outside the ID. In this case electrical cables (micro-coax or twisted pair)) would run within the service module to feed-through connectors at the off-detector end of the service modules.

figure xxx basic model of SM figure xxx welding and manifolding figgure xxx cabling cross section and mixing

12.2.3 Endcap Service Module

blah blah

IW thoughts on structure

- Integration process stave/petals into structures
  - Barrel plans - IW, SY, GV
  - Endcap plans and process - Carlos, Marcel
- Service modules (on-detector)
  - Introduction, including description of concept and common ground - IW, probably should write this first...
  - Description of barrel service module, work done and work to do - IW
  - Description of EC service module, work done and work to do - Carlos? Marcel?
- Finite element analysis
  - Barrel service module thermal performance and optimisation - IW - where does Geoff Taylor fit into this? perhaps he should do this...
  - Endcap service module thermal performance and optimisation - Carlos?
  - Thermal model of ID endplate aspirational - not started yet, may be very brief need to discuss with Georg.
- Thermo-mechanical measurements
  - TM barrel stave - stave 250 measurements, Oxford - RBN
  - TM barrel stave - stave 130 what will we have by TDR - Jens

12.3 Local support to structure and system integration

This section will describe the process of assembling the detector subsystems from the constituent parts. Generally the process is not influenced by location of the activities, but the intent is that the barrel will be integrated at CERN and the endcaps in DESY and NIKHEF.

12.3.1 Barrel Integration

Introduction and Summary of process The Barrel will have all the staves end inserted once the barrel structure is fully assembled in the Outer Cylinder. The Outer Cylinder (OC) is assumed to be sitting in a cradle (possibly the cradle that will be used to lower the tracker into ATLAS) and we assume we will have access into the bore of the OC for 2 personnel at once. We presume we will be able to populate the barrel region from both ends simultaneously. The staves will be slid into the barrel structure one at a time transferring them from a transport frame to the structure. This process will have dedicated tooling (detailed below) once at least 8 staves are in place in a keystone arrangement a barrel service module will be installed that covers at least 8 staves and routes the services up in R to R_{max} and then along in Z to Z $\approx$ 3.5m where the services will pass out of the tracker volume and be terminated in a patch panel. The staves that are now connected can be tested in situ. It remains to be decided exactly how many rounds of closing and then testing will need to happen during the build, this will be a balance of risks and schedules. Once all the staves have been inserted the ITk will be ready for the insertion of the Strip endcaps.

Assembly of structures blah blah

Insertion of staves in to barrel structures blah blah

servicing of barrel staves blah blah

12.3.2 Endcap Integration

- Carlos/Marcel

Introduction and Summary of process blah blah.

12.4 Service Modules

12.4.1 Introduction to Service Modules - how they work and why

blah blah

12.4.2 Barrel Service Modules

Introduction This service design has been motivated by our experiences with service installation for the ATLAS SCT. There, all services (fibres, cooling pipes and electrical cables) were installed individually into the ID into service channels on the calorimeter cryostat wall. This design resulted in a sequential service installation due to the limited accessibility and the large number of individual services. It resulted in a lengthy installation and let to ad-hoc modifications of the original service design, when problems were encountered. The exit of the services from the SCT barrel thermal enclosure was badly designed and resulted in a large leak rate from the ID, no overpressure has ever

been possible on the SCT volume. As an alternative we have developed pre-fabricated, standardised and removable service modules, each to be installed containing all services for 1/n th (n probably being 16, 24 or 32 - 24 is the present baseline, but any change in layout may change this figure) of one end. These comprise cooling pipes and associated manifolds, electrical cables, and optical fibres, at one point it was mooted that they might contain the optical converters if they need to be in a lower dose location, this looks unlikely, but remains possible. The service module would also contain well-defined internal electrical ground connection for all metallic surfaces (in particular cooling pipes) and a common ground connection to the thermal enclosure. The off-detector end of the service module is part of the thermal enclosure and contains all necessary feed-throughs. Performance of the gas and thermal seals will be fully qualified before installation. The most challenging area of the Service Module to implement reliably will be at the detector end of the complexity of weaving the services from a rotational to mirror symmetric arrangement.

Service module body The service modules are self-supporting to facilitate installation. At the same time structural elements of the service module should are low enough volume to not significantly reduce the volume available for services. The service module body is proposed to be made from folded Aluminium 0.5mm thick, if the geometry would need to be more complex the option is retained to fabricate from CFRP

Off-detector patch panels Patch panels at the end of the ID will allow electrical connectors to exit radially in the region of the cryostat chamfer. Cooling and opto will exit longitudinally. The whole patch panel will be kept outside the endcap radii to ensure no reforming of any services are needed to install the strip endcap. All connectors will be sealed into the patch panel, with the seal qualified as part of service module production, so that just the duct needs to be sealed into the ID during ID integration.

Cooling services Our preferred joining technique for all joints inside the thermal enclosure is welding to achieve low-mass, reliable connections. All connections within the service modules are made before integration into the Outer Cylinder. Within the service module there will also be some vacuum brazed assemblies which are welded onto the rest of the tubes. It is presently expected that the electrical insulated breaks will be vacuum brazed (and will also transition pipe diameter), as will the pipe manifolds, the termination of the capillaries may also use a vacuum braze process. Service module welds could use any welding technique (EB, Laser, TIG etc.), but our preferred option is orbital TIG. At the detector end pipes from the service module terminate short of the local supports . The connection from the detector to the service modules will be made by a short patch pipe, which will be cut to length and shaped to the actual end positions during the barrel integration. This short patch pipe will be connected using orbital TIG welding. The routing of the patch pipe, and the adjacent sections of the pipes on the service module and the local support, will prevent stress transmitted onto the staves and will allow access for the orbital weld head. The probability of a successful joint at this stage is improved if pipes of similar parameters are joined. We therefore propose that the transition from the on-detector pipe parameters to the service module pipe parameters shall be part of the on-detector cooling pipe assembly, and be qualified there.

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We believe that manifolds reducing the number of cooling connections before the ID ends by about a factor 1:4 to 1:8 are a good compromise between the space needed for connectors and pipes from there to PP2, and the risk of damage that will incapacitate many modules. A 1:4 manifolding scheme could would result in the loss of 8 staves 112 module from a fault in the circuit. These manifolds will be part of the service modules.

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figure xxx basic model of SM figure xxx welding and manifolding figgure xxx cabling cross section and mixing

12.4.3 Endcap Service Module

blah blah

Chaser: Ian Wilmut
number of pages to write: 20
Scope of chapter:

IW thoughts on structure

- Integration process stave/petals into structures
  - Barrel plans - IW, SY, GV
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  - TM barrel stave - stave 250 measurements, Oxford - RBN
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12.5 Local support to structure and system integration

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Assembly of structures blah blah

Insertion of staves in to barrel structures blah blah

servicing of barrel staves blah blah

12.5.2 Endcap Integration

- Carlos/Marcel

Introduction and Summary of process blah blah.

12.6 Service Modules

12.6.1 Introduction to Service Modules - how they work and why

blah blah

12.6.2 Barrel Service Modules

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Cooling services Our preferred joining technique for all joints inside the thermal enclosure is welding to achieve low-mass, reliable connections. All connections within the service modules are made before integration into the Outer Cylinder. Within the service module there will also be some vacuum brazed assemblies which are welded onto the rest of the tubes. It is presently expected that the electrical insulated breaks will be vacuum brazed (and will also transition pipe diameter), as will the pipe manifolds, the termination of the capillaries may also use a vacuum braze process. Service module welds could use any welding technique (EB, Laser, TIG etc.), but our preferred option is orbital TIG. At the detector end pipes from the service module terminate short of the local supports . The connection from the detector to the service modules will be made by a short patch pipe, which will be cut to length and shaped to the actual end positions during the barrel integration. This short patch pipe will be connected using orbital TIG welding. The routing of the patch pipe, and the adjacent sections of the pipes on the service module and the local support, will prevent stress transmitted onto the staves and will allow access for the orbital weld head. The probability of a successful joint at this stage is improved if pipes of similar parameters are joined. We therefore propose that the transition from the on-detector pipe parameters to the service module pipe parameters shall be part of the on-detector cooling pipe assembly, and be qualified there.

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Power and DCS cables Cables are standardised and slightly over length at the detector end of the service modules with the surplus being lost in routing. The cables have a decoupling capacitor between each line and the system ground at PP1. A diagram of the electrical services within a barrel strip service module is given in Figure xxx.

Optical services The optical conversion of the module sdata signals will happen on stave. However, as there is a small chance the final radiation dose in the end of stave region is too high for the opto convertors space is retained in the service module that would allow the opto convertor to sit in the service module if required. The three options that have been considered are shown below with option 1 being the baseline. Option 1: Optical conversion on local support. In this case at the detector end single fibres with over length would connect to the local supports. These fibres would need appropriate protection during installation and in-situ. The single fibres would get ribbonized within the service module and terminate at MT8 or MT12 ribbon connectors at the ID end. Option 2: Optical conversion within the service module. Electrical cables (micro-coax or twisted pair) with over length would connect to the local support at the detector end. These would run to the opto-converters within the service module, where conversion takes place. The opto-converters would be located so that they are accessible form the outside of the service module, preferably at the side of the service module, which becomes the radially inner wall in the final position. Fibre ribbons would then run within the service module to MT8 or MT12 ribbon connectors at the off-detector end. Option 3: Optical conversion outside the ID. In this case electrical cables (micro-coax or twisted pair)) would run within the service module to feed-through connectors at the off-detector end of the service modules.

figure xxx basic model of SM figure xxx welding and manifolding figgure xxx cabling cross section and mixing

12.6.3 Endcap Service Module

blah blah

13. Control and Readout

Editor: Marcel Stanitzki
Chaser: Pepe Bernabeu
number of pages to write: 12
Scope of chapter:

- *Introduction*
- *Off detector Readout Electronics and interface to TDAQ*
- *DCS (common and strip specific)*
- *Opto-links*
- *Planned QA during production*
- *Timeline of reviews*

13.1 Introduction

who is providing this ? maybe not so much needed, just a short intro to the chapter[IMG]

13.2 Off detector Readout Electronics and interface to TDAQ

provided by Matt Warren[IMG]

13.2.1 Scope

The off-detector readout and control electronics are responsible for communication between the on-detector electronics and the rest of the world. This covers control, monitoring, calibration and read-out of physics data, and in some cases DCS data.

ITk readout and control is closely coupled to the ATLAS TDAQ common readout and control architecture. TDAQ are providing a software framework and common hardware and interfaces that will be used where possible. This architecture is described in the TDAQ IDR, and includes the Front-End Link eXchange (FELIX), the Local Trigger Interface (LTI) and the Data Handler (DH).

All front-end (FE) data and controls flow through the FELIX. The LTI interfaces withthe ATLAS Trigger, Timing and Control (TTC) system, and the Data Handler interfaces with the data storage system.

If no better diagram, probably should make our own? Yes, I think we should make one of our own as LTI is missing[IMG]

The diagram in Fig. 13.87) from the TDAQ Phase-II IDR [**?**] shows their view of the system. This diagram is missing the LTI which is should be between LOTopo and L1 CTP and the detector FELIXs, and the Controller.

The FE-control part of the system (covering clocks, triggers, resets and configuration) operates independently of the readout part in most cases, but there are places where they converge, for example, when performing a calibration loop.

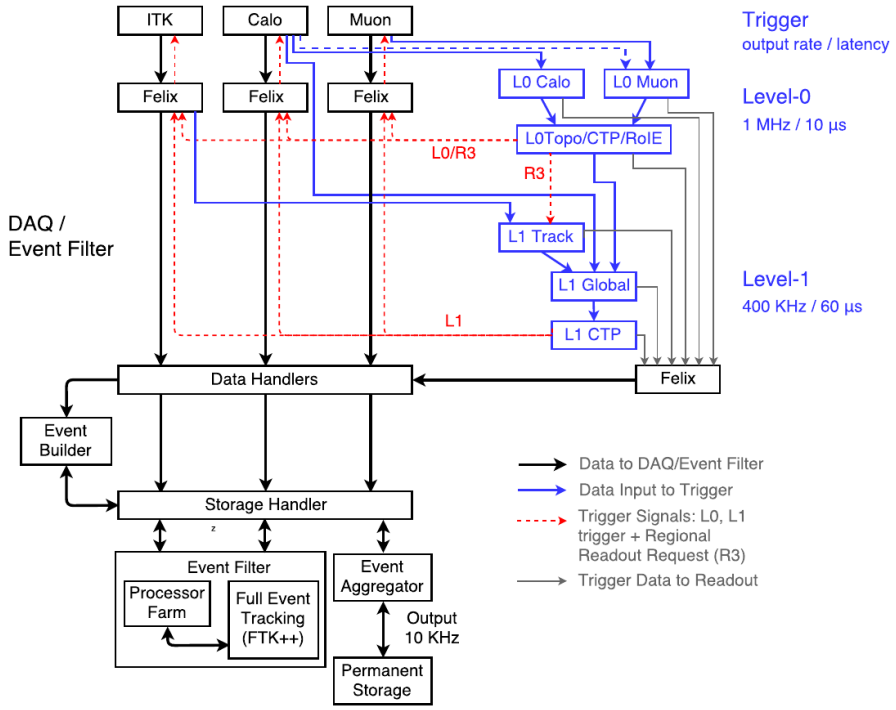

Figure 13.87. TDAQ global View of the two-level architecture. (ref TDAQ IDR fig 13) (Note: missing Controller and LTI)

Overseeing operation will be an ITk Controller PC, providing an interface and hub for ITk co-ordination of the system. This should be capable of independently controlling multiple divisions, but it is not yet known whether this could be a single shared system for all of ITk, or dedicated instances for Strips and Pixels. An operator console PC completes the system. It should be thought of as an expert terminal, located, for instance, in the satellite control room.

Readout is handled by a combination of a FELIX units and a Data Handler PCs, and FE-control will be via LTI units coupled to portions of the FELIX firmware. The Controller will be responsible for coordinating these devices, for instance when calibrating, or while starting a physics run. The bulk of the readout heavy-lifting will be performed by the FELIXs and Data Handlers, while interfaces to the ATLAS global triggers and control, and local signal generation and distribution will be provided by LTIs.

In each of the TDAQ common units - LTI, FELIX and Data Handler - ITk specific firmware/software will be needed. The Controller will run ITk software, but using TDAQ libraries to communicate with the lower-level systems. This mix of common and specific infrastructure predicates a number of interfaces that need to be carefully described.

The ITk-FELIX component will be a set of firmware for dealing with FE links, data formats and critical processing. Formatting of triggers etc. into ITk specific protocols will also take place here.

The ITk Data Handler will be a software package that resides within the TDAQ standard PC/software architecture.

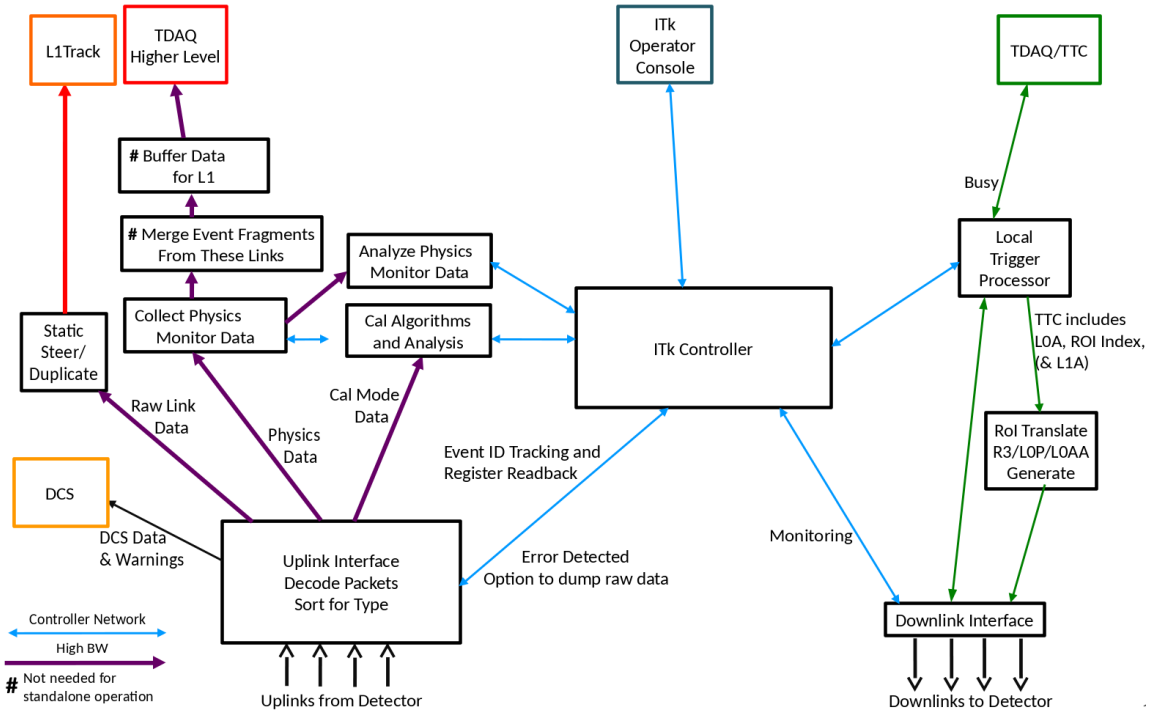

Figure 13.88. Readout Overview

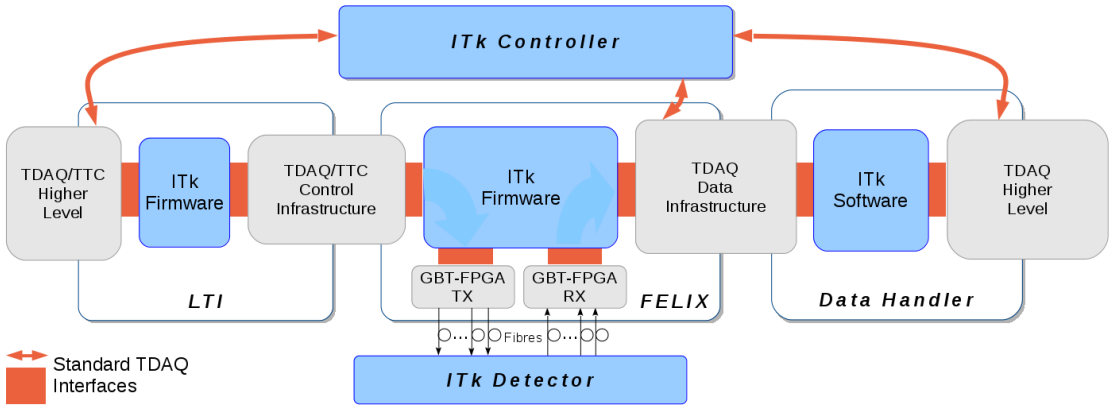

Figure 13.89. Diagram showing FELIX, Data Handler, LTI and Controller interfaces

13.2.2 FELIX

The ITk are one of the few sub-detectors that connect FELIX directly (via the versatile link) to their on-detector electronics. A high level description of the FELIX is a box that interfaces between a detector specific signalling (e.g. GBT) and Ethernet. This is a change from the current (i.e. SCT) system where all (electronic) low-level access to the detector modules is performed within one VME crate and mostly within one VME board. This alternative method is thought to be viable but

needs to be explored in more detail before it is adopted. This is only possible with ITk specific firmware built into the FELIX to provide the immediate interface to the Versatile links since the protocol on these links will be unique to ITk.

The following describes general requirements from the ITk point of view.

In the counting room, the FE fibres terminate at a FELIX. Here an FPGA will provide resources for decoding the FE-protocol. Within FELIX, the FE data frames and packets are processed by ITk specific firmware, responsible for decoding the custom data encoding/format, performing all ITk functions and interfacing to standard FELIX data-formatters and transport (for transferring the data to the Data Handlers).

13.2.3 FELIX Functions

FE-frame interface, decoding: The FE (sub-)link configuration is customisable and detector specific, As data from each module are not aligned with respect to data from other modules, and the data is transferred serially, a dedicated 8b/10b decoder/deserialiser and packet detector is needed for each (sub-)link. It is expected that the demultiplexing and 8B/10B decoding could make use of common libraries provided by CERN or TDAQ.

Data-type handling: The link from each module carries multiple data types. Firmware will separate these data into different queues as needed. In general all data will go to the Data Handler, but with a few important exceptions:

- **Error flagging/handling and monitoring:** To ensure prompt recovery from errors, it may be advantageous to deal with errors within the FELIX firmware, or to send an alert to the Controller. Any errors detected in the FE-frame or clock and data recovery (where used) will be reported. If errors become frequent on a link, the raw data may be dumped through ITk Control to the ITk Operator Console for diagnosis. Each packet will be examined for any recognisable corruption and if any is found, an error flag will be sent to ITk Control with the option of dumping the bad packet to the ITk Operator Console, discarding the packet or accepting the packet even with the corruption.

- **Calibration:** Data that is returned as part of a calibration loop may need to be dealt with on FELIX - for local histogramming and/or event counting. More details in the Calibration section (13.2.7)

Busy If any of the queues on FELIX exceed a fullness threshold, the busy needs to be asserted.

Event integrity checking (low level): Beyond checking for data corruption, event data needs to be checked for synchronisation and correlation with sent-trigger information. As this may require a prompt response, it should be performed here.

Control functions: The FELIX sends clocks (via the GBT directly) and control signals (via e-links) to the detector. Most of the control function is handled by the LTI, but some may be duplicated such that they can be applied to each downlink individually. E.g. local triggers, resets. In particular the data-link level encoding of TTC signals into the detector FE-protocol will likely be done in the FELIX. Some signals, e.g. configuration streams, will need to be delay paths to facilitated the synchronous signalling, e.g. triggers.

13.2.4 Data Handler

The Data handler implements the final detector-specific data processing layer before event data is sent to the storage handlers, e.g. formatting and/or monitoring [**?**]. The Data Handler is a TDAQ PC with a common software framework in which ITk software components are run. The infrastructure can be shared between physics and calibration running.

FE data will be parsed and decoded into hits or register data. Data is likely to be gathered by event ID, building event-fragments. These will be passed onto TDAQ components, via common software components.

Stand-alone local running: For calibration mode, histograms can be populated, and fits performed where needed (similarly for monitoring in physics mode). Results can be passed to ITk Control for other cross-checks and analysis and finally stored (this should be TDAQ provided storage).

Fragment merging: Merging event-fragments into macro-fragments [mentioned above, but needs more detail here]

Register readback: Forward any register read-back to ITk Control.

Event integrity checking (high level): Fragments checked for correct L0ID and BCID etc. This functionality will be shared with that of the FELIX firmware, although at this level there is far more detail of inter-trigger counters etc. to make use of.

13.2.5 LTI

The ATLAS-wide Trigger, Timing and Control (TTC) system connects to the ITk via Local Trigger Interfaces (LTIs). The LTI is also connected directly to the Level-0 Trigger System. The LTI forms part of the hierarchy of control signal distribution and at the lowest level will connect to multiple FELIXs. The ratio of LTI to FELIX is not yet known, but is expected to be of order 16 FELIX per LTI. This leads to about 8[?] LTIs feeding into a top-level LTI for ITk Strips, and more for Pixels.

The unit is responsible for generating local (e.g. for a subdivision of the ITk) triggers, other broadcast commands (e.g. BCR, ECR) and calibration strings [maybe in FELIX instead?].

Much of the LTI control function could be part of the FELIX, particularly more localised (e.g. link specific) signalling. This sharing will need to be optimised when details are clear - but as these are essentially control functions, they're detailed here.

The LTI is expected to provide many generic functions: Interfacing to the higher level systems, busy aggregation, monitoring and histogramming, trigger generation (and gating, when in stand-alone) etc.

Local Triggers: Generation of triggers for debug, calibration etc. of a partitions or smaller parts of the detector, e.g. a stave.

Command broadcasts (including local resets): Provides Command stream generation and sending. Interfaces to the Controller.

Register refresh: Managing the drip-feeding of automatic FE register refreshes. May need to maintain a mirror of FE registers in the LTI. This needs to respect a number of synchronising elements, e.g. Orbit or ECR.

Busy: Gating of local trigger when busy etc.

13.2.6 ITk Controller:

The Controller will manage the manage the data-flow, and form a hub for status and error flagging. The unit will likely be a PC, connected to all other systems via a dedicated control network. In most cases only commands and status updates will travel on the network, but it may be required to handle debug data dumps if other means are not present.

During data-taking, the Controller will setup the core systems to receive physics triggers (including configuring the modules), build monitoring histograms and then keep track of status and handling any errors when running.

During non-physics running, module calibration will be co-ordinated from the Controller.

13.2.7 Calibration

Calibration depends on closely coupled loops - the operation of these needs to be optimally shared between the FE ASIC, the FELIX firmware and the Data Handler software. Much of this is dependent on the deadtime (unused time between loops) of the system.

The calibration procedure will involve sending the entire chip configuration at the start and individual portions of the configuration as part of the loop structure configuring individual registers for each burst of triggers. A scan is made up of bursts of triggers, with a different configuration applied for each burst. A series of these scans is analysed and used to build a picture of the module status and performance.

The immediate result of the trigger loop will be a representation of the data acquired during this burst. This will usually include the occupancy histograms, but other data will be useful, including histograms of chip occupancy, cluster size and count. For low-level investigations, a direct map of the bits on the link might be collected.

Histograms can either be built, in the FELIX or in the Data Handler. For Strips, there is an option to histogram hits in the FE ASIC in a very low-level form (hit counter per strip). When histogramming in the Data Handler, where the data might be available only asynchronously, the loop indices to which the data belongs needs to be communicated to the process building the histogram.

Going in to more detail about how this occurs: a calibration scan is carried out using a hierarchy of loops over bursts of triggers. The different levels include the main scan parameter(s) as well as mask changes (for charge injection). For the inner loop, a trigger will be an arbitrary short command sequence sent to the FE chips in order to generate a response. This includes injecting a calibration charge, sending L1, R3, L0 triggers, as well as register readback commands. In some cases this sequence will be specified in terms of raw signals to be sent (i.e. sent without any encoding). This command will be repeated many (e.g. 100) times and in order to make the complete scan as fast as possible, an automatic adjustment of the repetition frequency depending on the amount of data being received is desired. Otherwise, delays created in this loop will be multiplied by the repetition from higher parameter loops levels.

13.2.8 Monitoring

During data taking (but not necessarily enabled all the time) the physics data will need to be monitored. This function will also be an important part of stand alone operation during integration.

The primary purpose is to look for faults in modules that may not be obvious from examining data that passes the higher-level trigger and to respond to any warnings issued by the on-detector electronics. This function must have no effect on the physics data flow.

Monitoring data will be passed from the FELIX and Data Handlers to the Controller for assessment. Potentially all data sent from the detector should be available to be monitored.

- **Collect and analyse Physics Monitor Data** Monitoring of link occupancies, how much more data can be sent down the stream. In addition to the raw event size, and the space between packets, it should be possible to keep track of how much time has passed between the transmission of the trigger and reception of the last data.
- **Triggers that are not useful for physics** Include looking for stuck cells, or high occupancy due to threshold misconfiguration (SEU).
- **Primitive operations** This may be a stream, or a single block of data triggered by user. Primitives set the output configuration, some of the options being:
  - Raw data from GBT/elink
  - Chip data (decompressed and packetized)
  - All event data
  - nth event
  - Large events (above threshold bytes)
  - All error data (as decided by error checker), including some number of events before and after
  - Matches pattern (e.g. hit in detector element)

13.2.9 L1Track Options

FELIX L1Track pre-processor: L1Track will have multiple track-finder units arranged in approximately 16 ATCA shelves. Data from the ITk (mostly Strips, but also outer-layer Pixels) will need to be routed to these shelves, and in some cases duplicated to a second shelf. There is a static correspondence between a data uplink and a shelf (or shelves). To reduce the number of links, bonding is expected to take place on the FELIX, where, for example, ten 10 Gb GBT uplinks are combined into a single 100Gb fibre.

The FELIX may also be able to duplicate links where needed.

13.3 Strips Off-detector Readout/Control Electronics and Interfaces to TDAQ

13.3.1 Scope

The Strips readout and control electronics are part of the common ITk DAQ system, shared with Pixels and detailed in the Common DAQ section 13.2. This section deals with Strip-only functionality, and finer details of the Strip system.

Strips have their own FE chipset, data transfer protocols and link archtecture. Strips also send DCS data on their readout links.

13.3.2 Strips Architecture

On the detector, within a module, a hybrid hosts 10-14 ABC ASICs connected to the silicon strips. After receiving a trigger, the ABC ASICs they pass their data to an HCC ASIC at the end of the hybrid, where it is aggregated, formatted, 8B/10B encoded and transmitted via 640Mb serial e-links to the GBTx(s) at the end of the structure (EoS). Data sent from an HCC consists of variable length packets - each containing a single data type (and a single event for the event-data type), with lengths expected to be less than 50 bytes, averaging between 15 and 30 bytes. The predominant type (by bandwidth) will be event-data, but other types include register-readback, calibration data, DCS data and warnings/alerts.

For readout purposes, each HCC operates as an independent unit, transferring data when ready, without any awareness of the other HCCs and sending data using its own e-link. This means that, because of variations in occupancy, and regional readout, events will not be transferred at the same time, and are therefore not aligned in time.

The LpGBTx aggregates up to 14 640Mb e-links onto a 10Gb optical fibre [**?**], transporting the data to the counting room using the CERN VL+ optical transmission system. The physical transmission and protocol used are internal to LpGBT/VL+ chipsets and detailed elsewhere **??**.

DCS data from the HCC and ABC ASICs is also transported over these links. Further DCS data will also travel from the modules using a different route, but ultimately by the via the GBTx and readout fibre.

During power up, power ASICs on the modules will need to be setup to apply power to the HCC and the the ABCs. This communication is via the GBTx, via the downlink fibres, but under the control of DCS. Once the HCC is up, more detailed DCS information can be obtained, allowing the ABCs to powering to be co-ordingated. [Peter really should look at this!]

Connection off-detector is via the FELIX.

13.3.3 Strips-FELIX

The the FELIX provides a generic platform for multi-function, multi-detector use. In the Strips case, it provides the only, with the exception of interlocks, path for controlling and monitoring the detector. FELIX makes provision for sub-detector specific firmware and interfaces, and will need to be able to provide a reliable path to DCS, and mechanisms for decoding Strips specific data.

As Strips will be using the GBT/VL+ physical links and protocols, the Strips-FELIX provides end-to-end GBT- to Ethernet-protocol conversion.

The GBT frames are then passed to Strips specific firmware for expansion into the component e-links, decoding of the custom data encoding/format and processing.

Strips expects 4-8k GBT uplinks, and each FELIX is expected to handle about 100 links, so we expect to have 40-80 FELIX units in the system.

13.3.4 Strips-FELIX Functions

FE-frame interface, decoding: With use of a CERN library (GBT-FPGA [**?**]) it is expected that FELIX core firmware will decode the bulk GBT frames, making the error detected/corrected

data available via a standardised interface. The first stage of the Strips-FELIX firmware will be to demultiplex the GBT frames into their component e-links.

Data-type handling: In most cases data flows through FELIX to the Data Handler, but with a few important exceptions. In addition to the data-types detailed in the common DAQ section 13.2.3, Strips have 2 more:

- **DCS data:** This is considered high priority (although not critical) for detector safety [better way of saying this DCS not DSS?]. This data will be queued separately from other data, and be passed to the DCS subsystem (external to FELIX) via a dedicated and/or prioritised connection. Data will need to be formatted for DCS handling as per the DCS spec ([**?**]) [need to check with DCS regarding (OPC-UA?) ODB?? servers etc.] More in the Monitoring section in nthe common part (13.2.8).

- **L1Track data:** When a regional trigger is used, high priority data for L1Track will arrive with its own type. This will need to make use of a DOLL (zzz) path to the L1Track formatters. This type of data can optionally be duplicated and also be sent on as standard data to the Data Handler. Once physics event-data has been separated from the other types of data coming from the on-detector electronics, the data from events and regions identified as useful to L1Track must be filtered and copied from the main data-stream and sent to the L1Track processor. This data-path has the tightest latency requirement in the readout system.

13.3.5 Calibration

As per common, but Strips calibration may be able to benifit from hit counters inside the ABC

Calibration Data Volume: Much of the time spent in calibration is in changing registers on the front-end ASICs. For Strips this is about 128 registers per chip (32 bit, but taking about 60 bits to send). So with 10 chips per barrel hybrid, 2 hybrids per module and 14 modules per stave side (similar size for petals), the configuration sent to each of the GBTs totals about 2.2Mbit.

Histogram data volume: the output of each burst can be stored in 1-4 bytes per channel, 72k per barrel stave. A calibration sequence will be made up of 100s of these bursts. It is not decided whether this raw data need be stored vs only a summarised version (fitted S-curves).

13.3.6 Bandwidth Estimations

Need to detail occupancy -> data volume, to total links etc.

13.3.7 Link Architecture and FE protocols

More on the links, including protocols.

13.3.8 L1Track Considerations

RoI readout triggers (e.g. R3) will need to be assembled and generated at more than one stage inthe system. Globally the Level-0 Trigger will broadcast RoIs, and then this list will be refined as the signalling moves closed to the physical downlink.

LTI R3 generation:

FELIX R3 generation:

13.4 DCS

Written by Susanne K. and Peter P.[IMG]

The interlock system is an ITk common safety system, which protects both the detector and the personnel against any upcoming risks. It is additionally foreseen besides the sub-detector specific interlock circuits, which control detector modules or other small detector units.

It is a completely hardwired system, which acts as last line of defence. It needs to be running at all times, but it has a coarse granularity and there is no need for a high precision. As heat-ups are one of the main risks to all silicon detectors, temperature sensors are located in the critical points of the ITk. Each cooling pipe outlet of the strip detector will be equipped with two temperature sensors for redundancy. Positioning of the temperature sensor inside the pixel volume is still under investigation. As NTCs provide large signals (delta R/delta T) and have a higher high radiation hardness, 10 kOhm NTCs are foreseen. Their large signals allow for two-wire readout and routing of signals up to the counting rooms.

All signal procession will take place in the IMCs (Interlock Matrix Crate). reads odd[MS] At first the analogue signals of the temperature sensors will be converted to digital signals by a discriminator with a predefined threshold (monitoring of the temperatures in parallel is foreseen). The interlock signals from all temperature sensors are collected by a CPLD. This is the unit, which houses the action matrix, and maps the interlock signals onto the correlated power supply units. In parallel, signals from the ATLAS wide detector safety system will be integrated into the interlock matrix. These signals provide e.g. information about the status of the cooling plant or the accelerator and typically require action on a large group of channels (e.g. all HV channels of a detector). The CPLD allows for defining any correlation between interlock protected and interlock controlled devices. For safety reasons a negative logic is foreseen. Location of the Interlock Matrix Crate is the counting room. Main advantages of this area are that no prove of radiation hardness is required and that the equipment is accessible at all times.

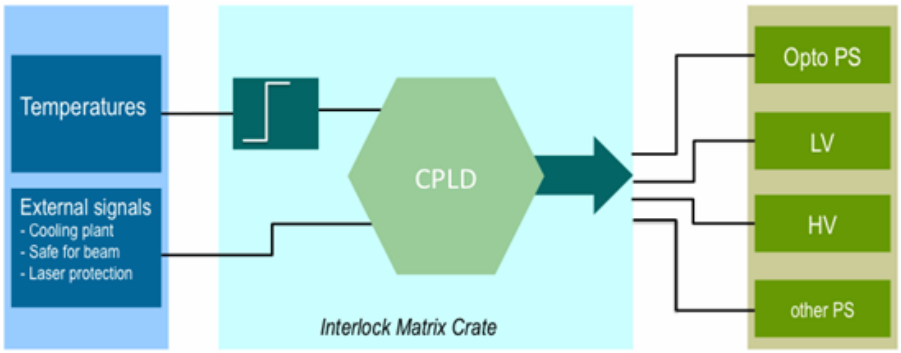

Figure 13.90. Caption. ???????

Besides the common interlock system, the environmental monitoring system will also be built in common for the pixel and strip detector. This system provides temperature and humidity monitoring in the ITk volume, e.g. the temperature of the cable bundles or other parts which are not

directly belonging to any detector elements will be supervised by this system. In order to keep the services, which are routed out of the detector volume, at a minimum local data processing is foreseen. A scheme consisting of satellite-ELMB++ and HUB-ELMB++ might be a good candidate to realise such a system.

13.5 Optoelectronics

The components of the on-detector optical links are described in section xxx. The on-detector optical transceiver, the VL+ VTRx will either use a low profile fibre connector, or contain pigtailed fibres. For each VTRx there will be a short length of fibre break out cable, terminated with LC connectors. For the barrel, this will allow a connection to the ribbon fibres in service modules, see Fig. 13.5.

Figure 13.91. Barrel service module showing individual fibres terminated with LC connectors on the left. The ribbon fibres are laid in the service module and the MT/MTP connectors are visible at the right hand end of the service module.

The fibres in the service modules will be in ribbon form and be terminated with MT/MPO connectors at PP1. All the fibres will be multimode and operated at a wavelength close to 850 nm. The fibres inside the high dose region of the detector will be qualified radiation tolerant fibres. We have verified that the radiation induced attenuation (RIA) for these fibres operating at -25 C$^\circ$ is acceptable [18]. We have also demonstrated that the mechanical reliability of these fibres is maintained with radiation [19]. We have also shown that there is no significant deterioration of bandwidth with radiation [20]. Finally we have verified the radiation hardness of the LC and MT/MPO fibre connectors [21]. In order to satisfy the bandwidth requirement, we need to use OM3 fibre. However the cost of long lengths of qualified radiation tolerant OM3 fibre is prohibitive, we will therefore use a shorter length of such fibre and splice it to a longer length of a COTs fibre which would still be sufficiently radiation tolerant.

In the counting room, commercial optoelectronics packages will be used to convert optical to/from electrical signals. Ongoing VL+ research has shown that several components are commercially available that operate at the required data rates. As this is a rapidly evolving market, new components are being continuously tested. In the counting room, the functionality of the lpGBT will be implemented in FPGAs. The I/O from the FPGAs will then be connected to the Felix system.

13.5.1 Optoelectronics Quality Control

The optoelectronic ASICs will be tested at the wafer level and only known good die will be packaged. The VCSELs and photodiodes will be packaged into the VL+ VTRx and then tests will be performed on the VTRx. The critical parameters for the VCSEL that will be measured are laser threshold and slope efficiency, rise and fall times. The minimum receiver responsivity will be measured for the photodiode. This is defined as the incoming optical power for which the Bit Error Ratio is less than a specified value. The exact tests to be performed will be defined by the VL+ group at the end of the development stage.

13.6 Timeline of reviews

13.6.1 Local monitoring and control infrastructure

I think this is partially not in the correct chapter - move to XX[IMG]

14. Powering for the Strips with Shielding and Ground Referencing for all of ITk

Editor: Uli Parzefall
Chaser: Ewa Stanecka

In this chapter the powering needs for the strip detector will be described and the possible solutions.

14.1 Estimate of the total power in the strip detector

added by IMG – numbers to be cross checked[IMG] Recent detailed estimations have shown that the maximum power consumption per channel should be of the order of 0.7? mW. Assuming a pessimistic 1 mW per channel for the strip ABC130 and a 1.2 V working Vdd, one needs to feed about 210 mA per 256-channel ABC130. Hence, one has to feed a total current (for the barrel and both end-caps) of order 61 kA to the front-end. The power dissipated in the front-end will depend on the powering scheme but will in any case include some inefficiency because of the embedded regulators or converters. 80% efficiency would lead to about 93 kW dissipated in the tracker volume, while 70% efficiency would lead to about 106 kW. These numbers show the extreme attention one has to pay to the design of the different power components so that their efficiency is maintained as high as possible.

The TID bump (see chapter XX) will lead to an increased power dissipation in the system compared to the non-irradiated. Detailed calculations showed that ....

add table here with a power estimate over time - including TID bump - see Steve's slides Oxford[IMG]

14.2 Powering the ITK Strips

Author: Alex Grillo

Power for the specific on-detector components will be provided by power boards located on the detector modules, staves and petals as already discussed in Chapter 6 ff. Power to the staves and petals will be provided by power supplies external to the ITk itself through a cable plant. These external power supplies and the associated cable plant will be described in this chapter. In order to minimise power loss in the cables, low voltage power for the ASICs will be supplied to the staves and petals at 11 V and then stepped down to the required voltages by these power boards. The high voltage required to bias the silicon sensors will be provide at the desired voltage directly to the staves and petals since the current draw on those lines is small enough to make the voltage drop a non-issue.

In the interests of minimising the cost of providing this cable plant, as much of the existing ATLAS Inner Detector (ID) cable plant as possible will be reused. Figure 14.92 gives a rough overview of the planned cable plant for the ITk Strips as a cross section of the collider and service caverns viewed from above. The figure is qualitative in nature and not at all drawn to scale. With the power supplies located in service caverns USA15 and US15, ATLAS-SCT Type IV cables will be used to reach patch panel 3 (PP3) now located in racks on either side of the ATLAS detector outside of the full Muon spectrometer. From there we will use ATLAS-SCT Type III cables which run through the Muon spectrometer area to places marked as PP2 (patch panel 2) in the figure.

Currently there are no PP2s for SCT cables but rather there is a splice of Type III cables to Type II cables at roughly the same place as PP2. We plan to cut the cables at this splice point, install new PP2s and then run new Type II cables from the PP2s to the patch panel 1s (PP1s) located just outside the ITk outer enclosure. We have decided not to use the existing Type II cables because we are unsure what their condition will be after being irradiated for the full life of the present ATLAS ID. They will likely be activated and unsafe to handle for any extended period of time. As will be described in section **??**, there is sufficient copper cross section in the Type IV and Type III cable to handle the full ITk Strips power needs. The modularity is also rather convenient in that we can assign two SCT cables to each singled-sided petal and to each single-sided half-stave for the outer two barrels with four cables assigned to each single-sided half-stave of the inner two barrels. The grouping of conductors will be rearranged at PP2 to better match the stave/petal structure of the ITk.

There are a few issues related to re-using the SCT cables that are still being worked out. One is the rating of the high voltage wires inside the SCT cables. These wires were rated for use up to 500 V. While the present operating limit of the ITk Strips sensors is also 500 V, there is a desire to have a higher voltage (600 V or 700 V) available as a possible backup for end-of-life operation if the signal-to-noise ratio drops uncomfortably low as end-of-life approaches. The procurement documents for the cables specify that the HV wire to its return line were tested up to 1500 V and the HV line to the shield and the other conductors was tested to 1000 V. Our requirements state that HV cables must be tested to twice their expected operating voltage and so we will test some spare SCT cables up from 1000 V to 1500 V in 100 V steps. Given how the cables were tested by the vendor, we are confident that we will be able to increase the operating rating of the cables from 500 V to at least 600 V if not 700 V. We expect these tests to be completed by mid-September of this year. If the cables fail these tests above 1kV such that we cannot rate them higher than 500 V, we will need to decide if the higher operating voltage is important enough to purchase new HV cables or if 500 V is sufficient. We consider this to be an unlikely needed backup plan. There will be much work occurring in these PP2 areas during LS3 with the replacement of some Muon chambers and the replacement of electronics on the remaining Muon chambers. We are working with Technical Coordination on a strategy for coordinating both the ITk and the Muon work in these areas.

Figure 14.92. Overview of Planned ITk Strips Cable Plant. Patch panels are labeled PP3, PP2, and PP1. SMs are the Service Modules that connect services from PP1 to the individual End of Structure cards for the Staves and Petals.

14.2.1 Powering for staves and petals

Author: Ewa

It will cover the powering of staves and petals starting with the modules and ending with power requirements for the two types of half-staves and the petals.

Power requirements The basic elements of ITK strip detector from power supply system point of view are the staves and petals. They are populated with ITK strips detector modules as described in add reference to chapters. The electrical power, data and control signals are distributed by kapton bus tapesadd ref installed on the mechanical supports of staves and petals. The ITK strips modules

require low voltages (LV) for front-end electronic and the power board as well as high voltage (HV) to bias silicon sensors. There are several types of strip modules: short strip barrel module, long strip barrel module and 6 types of end-cap modules. All these types have different number of FE chips, thus different power requirements. The electrical requirements of short strip barrel module, as having the highest power loads, are listed in table 14.22 for individual on-module components. The ABC and Hybrid Controller Chips are fabricated in Global Foundry (formerly IBL) 130nm process that is known to suffer from an increase in the digital current due to ionizing radiation add ref. The maximum anticipated current consumption related to TID bump is also specified in the table 14.22.

Each stave and petal is equipped with the End of Substructure card add reference to chapters which provides an interface between a chain of the detector modules and the off-detector electronics. The EoScomponents require power and the power load for its specific parts is shown in table 14.23.

Element	n	U[V]	I_{typ}[mA]	ΣI_{typ} [mA]	I_{max} [mA]	ΣI_{max} [mA]
HCC*	2	1.5	300	2400	750	4700
ABC*	20	1.5	90		160	
AMAC core	1	1.5	30	30	30	30
AMAC HV osc	1	2.5/3.5	1	1	1	1
Sensor HV	1	700??	2??	2	2	2

Table 14.22. Short strip stave module load including typical current consumption and anticipation of worst case current consumption wiht TID bump.

Element	n	U[V]	I[A]
LpGBT	2	1.2	0.625
LpGBLD	2	2.5	0.018
LpGBLD	2	1.2	0.010
GBTIA	1	2.5	0.053
UpFEAST	1	11.0	0.253
FEASTtsmc	1	2.5	0.700

Table 14.23. End of Structure elements power load ref?

Having single module and EoSpower requirements the total power load for single staves and petals can be estimated. Here a calculation for half stave for short strip module stave is summarised make table with half stave summary

The worst-case expected module operation condition for sensor bias voltage HV is 600 V or 700 V ? with a maximum module current of put a correct value here 2 mA. The LV power will be delivered to stave/petal at approximately 11 V and converted locally to the required levels.

Modularity The power will be delivered from external power supplies via cable plant down to

the service modules chapter ref which provides mechanical interface between external system and stave and petals.

The possible usage of on-module HV switch to enable/disable HV power for single module is still under investigation reference to chapter, thus the modularity of the the primary HV is not defined at the time of writing this document. Two scenarios, with 2 or 4 HV lines per stave/petal side, are considered. The LV will be supplied two groups of detector modules on one stave/petal side and one LV line per side.

Safety a few sentences about

14.2.2 Power supply options

Author: Wladek The options for delivering the power from the power supplies located in service caverns to the End of Structure cards and detector modules for the Staves and Petals is closely connected with the arrangement and parameters of the cables, which will be described in section 13.3. The are several aspects to be taken into account, namely: power losses in the cables and overall efficiency of the powering system, amount of material, cost of additional cables of type II and safety of the DC-DC converters on the Staves and Petals. These converters will be operated with a nominal input voltage of 11 V while the maximum operating voltage is 12 V. Thus, operating the power system with significant voltage drops in the cables, in an event of sudden drop of the supply current the voltage at the inputs of the DC-DC converters may exceed the limit of 12 V. The three considered options are:

- Direct powering.

  The power supplies in service caverns deliver voltages directly to the power boards located on the staves and petals. With conservative assumptions regarding the maximum currents required and cable resistances the voltage drop in the whole cable run can be as large as 4V power supply voltage of 15V. This will require the power supplies in the service caverns to provide voltage regulation according to the remote sensing, which will have to be slow given the overall impedance of cables and needs for heavy filtering of the power lines and sensing lines. Stability of such a system have to be considered very carefully and will require close interactions with the vendor(s) of the power supplies. I just note that the Wiener MARATON system used by TRT and LHCb tracker do not provide any sensing. Instead, both power systems relay heavily on the rad-hard regulators located close to the front-end electronics In addition a voltage limiter will be needed in order to prevent fast transient changes of the supply voltage at the staves and petals exciting 12 V. The voltage limiter will have to operate using a sense line for activation and its reaction time will be determined also by the length of the cables between the limiter and the sensing note. Depending on the voltage drops in the low mass power tapes, the sensing nodes can be either on the power boards on the staves and petals on the Service Modules in PP1. From this point of view location of the voltage limiters in the PP2 will be preferable.

- Additional DC-DC converter in the PP3.

  The power supplies in service caverns provide output voltage of 48 V and an DC-DC step down converter is placed in the PP3. The output voltage of this converter should cover

11 V required for the power board plus voltage drops in type III cables, type II cables, and low mass tapes. This solution will result in reduction of power dissipation and voltage drops in the type IV cables so that main power supplies could be operated without remote sensing. On the other hand regulation with remote sensing will have to be implemented in the DC-DC converter and taking a very conservative approach voltage limiters may be installed in the PP2. The radiation levels and the magnetic field in the PP3 prohibit using standard industrial electronics and custom-developed radiation tolerant DC-DC converter will be required. The radiation levels are relatively low (Craig is looking for numbers.) so that employing a COTS (Commercial of the Shelf) approach is feasible with applying a proper qualification procedures.

- Additional DC-DC converter in PP2.

  This option is similar to option (B) but it assumes DC-DC converters installed in PP2. It will allows us to eliminated the voltage limiter but the requirements regarding radiation tolerance (Craig is looking for numbers.) and sensitivity to magnetic field (Craig is looking for numbers.) will be much higher (???). Given the time and budget constraint such an option should be considered only if development of an adequate DC-DC converter using a COTS approach will become feasible.

14.2.3 Cabling options

Author: Alex Date: soon after the Oxford meeting, e.g. 27-Jun.

The cable options including the need for a voltage clamp. The cables go after the power supplies so that details of voltage drops can be covered in detail. The very brief overview in 14.2.1 will just give enough information such that details of the power supplies and the on-detector powering will make some sense to the reader without having to jump ahead to see what is going on.

14.3 Grounding and shielding across ITK and its interconnection to ATLAS

Author: Ned Spencer

Pepe sent request to Ned already.

14.4 Planned QA during production

Not sure what contet should be here

14.5 Timeline of reviews

15. Common Mechanics

Editor: Abe Seiden
Chaser: Georg Viehhauser
Number of pages to write: 20
Scope of chapter:

15.1 Decommissioning and removal of current Inner Detector (ID) (4 pages)

15.1.1 Removed items and condition of ATLAS after the removal of the ID and associated infrastructure (0.5 page)

15.1.2 Radiation environment for ID decommissioning (2 pages)

Activation of ID components (0.5 page)

Radiation environment during LS3 (1 page)

15.1.3 Decommissioning procedures and tooling (1 page)

15.1.4 Schedule for Planning, Preparation and Decommissioning (0.5 page)

A reminder to LHCC that a detailed decommissioning report will be delivered at the same time as the pixel TDR.

15.2 Common Mechanics of the ITk

The overall mechanical design of the ITk is driven by the aspiration to minimize the time needed for assembly and integration of the tracker, and in particular for the installation and service connection in the underground area. In the latter case this is to satisfy the overall schedule constraints for ATLAS within LS3 and also to minimize exposure of personnel to activated material in the experiment. The ITk will therefore be fully integrated and tested on the surface, before it is lowered down into the underground area and inserted into ATLAS.

Throughout the project we strive to achieve modularity of all components in the ITk. A modular design is a hierarchical assembly made up of well-contained sub-assemblies with simple interfaces to other parts of the project. Sub-assemblies will be thoroughly tested before integration into the next hierarchical layer, so that each integration step is simple and the risks to the integration process are small. Production and testing of sub-assemblies can be distributed. Where assemblies are needed in numbers they are designed to be identical as much as possible, which allows for interchange and reduced number of spares, and further improves schedule robustness.

The ITk is contained during the surface integration, the transport from the surface integration site to the experiment, and in the final location within ATLAS by the Outer Cylinder (OC - see section 15.4). At its ends this cylinder is closed by structural elements maintaining the hoop stiffness - the Structural Bulkheads (SBs - see section 15.4, and thermal, humidity and electrical barriers (see section 15.5), which are penetrated by the tracker service Patch Panels 1 (PP1), which also provide the necessary seals to maintain the integrity of the barriers for all service penetrations. All strip

services will terminate in a connector of some sort at this location to provide a clear envelope for the tracker during transport and allow for a fast connection of the tracker to the type II services.

The main function of the mechanical structures within the ITk is to support and place the detector modules. The positioning requirements for the ITk have been documented in ref. [**?**]. They are based on the observation that in the current ATLAS detector track-based software alignment is being used to locate the sensor elements with the required precision with no support from a hardware alignment system and little reliance on build precision and survey data. We expect that a similar strategy will be used for the alignment of the ITk.

For track-based alignment to work only moderate placement accuracies are required, mostly to maintain hermeticity and clearances (typically in the order of 100 μm). The key requirement, however, is stability of the sense element positions over periods where data for a software alignment cycle are collected. Table 15.24 lists the stability requirements relevant for the strip system with their timescales and typical loads. Similar performance has been achieved in the current ATLAS ID.

Table 15.24. Stability requirements for the ITk in $r\phi$ and expected loads. Stability requirements in the other directions are 10 times higher (from [**?**]).

Timescale	RMS stability [μm]	Comment	Load	Load level
Short ($\sim$ 1 d)	2		External vibrations	$< 10^{-7} g_N^2/\text{Hz}$
			Front-end power variations	$< 5\%$
			Temperature variations	$\pm 1^\circ$C
Medium ($\sim$ 1 m)	5	Always within sub-systems, on a global scale only between seismic events	Seismic shocks (magnet ramps, cooling system stops etc.)	
			Temperature variations	$\pm 2^\circ$C
Long (several months to years)	as assembly placement accuracy			

Ref. [**?**] also lists as desirable the provision of knowledge of the sense element position out of the detector plane to 100 μm within the strip system to support the track-based alignment in the direction where it is less powerful, but it should be noted that this is not a requirement on a par with the stability numbers above, as this constraint is not available in the current alignment of the ATLAS ID.

15.3 Support hierarchy of the ITk (1 page)

15.4 Outer cylinder and structural bulkheads (4 pages)

15.4.1 Requirements (0.5 page)

15.4.2 Conceptual design for outer cylinder and structural bulkheads (1 page)

15.4.3 Interfaces to the barrel strip system (0.5 page)

15.4.4 Interfaces to the endcap strip system (0.5 page)

15.4.5 ITk cradle (1 page)

15.5 ITk barriers (3 pages)

15.5.1 Neutron Polymoderator (0.5 page)

Reference to Background calculations
Description

15.5.2 Humidity barrier

The ITk humidity barrier has to prevent the diffusion of moisture into the tracker. We plan to re-use the current dry nitrogen supply system (3200 L/h N_2 or about half a volume exchange per hour with a dew point of -80°C, corresponding to a water content of 0.54 mm^3/L). In the current tracker we achieve a dew point of -40°C (water content of 127 mm^3/L), corresponding to a back-diffusion rate of about 25 L/h of cavern air with a dew point of 15°C. It is believed that the biggest leaks in the current system are the service feedthroughs. In the barrel SCT we cannot achieve measurable overpressure for a flow rate of 960 L/h. In the future tracker the coldest components within the ITk will be the cooling system return lines at a temperature of minimally -40°C. We therefore set a dew point requirement of -50°C in the ITk. For the given nitrogen flow this limits the maximum acceptable back-diffusion rate of cavern air to 7 L/h. We plan to achieve this more stringent requirement with more carefully designed service feedthroughs. It should be noted that this humidity barrier is integral to the ITk and is therefore already functional during the surface integration of the ITk (sub-system PP1s will be installed progressively during the integration and need to be blanked off before that).

We foresee a secondary humidity environment outside the tracker ends and extending in the gap between the calorimeters to the outer perimeter of the barrel calorimeter, similar to the current ID end plate volume. The exact dew point requirements for this volume will be defined once the designs for the PP1s and the temperatures of services outside the ITk will be better understood, but we currently expect a dew point requirement in this volume of about -25°C. This means that all cooling services in this volume need to be insulated to prevent condensation, although the performance required of this insulation will not necessarily be very demanding. Services will penetrate this enclosure in feedthroughs at the outer perimeter of the service gap, from which point the cooling services will feature high-performance thermal insulation.

Due to the sensor technology in the ITk there is no requirement that the tracker needs to be cold all the time to prevent detrimental annealing effects once radiation damage manifests itself. However, we do want to prevent the diffusion of moisture into the tracker at all times, including access to the inner or outer pixel systems, even if the tracker is warm. While we do not intend to use internal thermal barriers in the future tracker, we are planning to implement internal moisture barriers between the strips and the outer pixels, and the outer and inner pixel layers to maintain the integrity of the humidity environment during the removal of these smaller units.

The humidity barrier will be physically part of the OC and the SBs. The exact implementation of the humidity barrier will be studied when the design of these structures will be more advanced. The strip services will penetrate the ITk humidity barrier at just inside of PP1. At this location the service modules will contain a sealing block which provides the internal humidity seal (see section x). The service module will then seal to the opening in in the SBs to complete the hermetic humidity barrier.

15.5.3 Thermal barrier (1 page)

Requirements

Description

15.5.4 Faraday cage

The ITk Faraday cage needs to satisfy the grounding and shielding strategy for the ITk as discussed in section x. It will follow the outer humidity barrier, consisting of the OC, the tracker endplates and the beam pipe insulation shield just within the inner pixel layers and their services. There will be no electrical shield between the inner and outer pixel systems, or between the pixel and strip systems. This implies that the end sections of the inner pixel system would have an RF bond (continuous as possible) to the shield of the main tracker.

The electrical shield could be a thin $\sim$50 μm metal layer. We are investigating shielding properties of metal cylinders to help in determining this thickness. All system cabling will have a braid shield so that the metal shell connectors can bond well and reliably. The referencing metal for the cable shields will be the Faraday cage. Service cabinets will have a complete shield enclosure. Both, cabinets and the tracker shield skin, need particular attention to joints and seams between metal shield components, such as galvanically compatible metals or plating. The use of bare aluminium in the shielding system will be avoided. Joints and seams need detailing that provides continuous electrical contact wherever practical. One technique between stiff metal components is plated BeCu fingerstock gaskets compressed by assembly fasteners.

All conductors entering the Faraday cage will bond at the entry, or be conditioned by an EMI filter mounted on the cage (Figure 15.93). This is standard EMI shielding practice. DC connections of shields are emphasized because the shield skin can be more complete. Practices such as pigtail connections of cable shields will be avoided. Metal shell connectors with full capture of the cable shield and circumferential bonding to a service enclosure give better EMI attenuation.

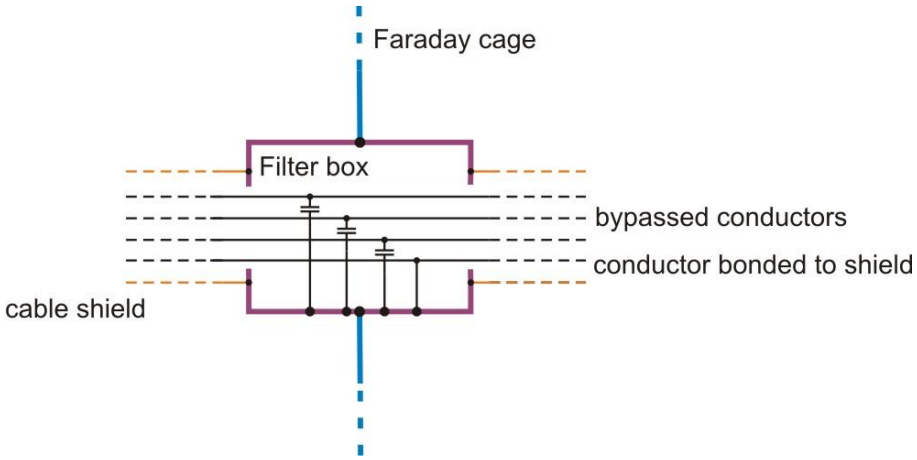

Figure 15.93. Ground connection concepts at the Faraday cage.

15.6 Envelopes (2 pages)

Definitions

15.6.1 Envelopes between barrel and endcap strips (0.5 page)

15.6.2 Envelopes and mechanical interfaces between barrel strip system and outer cylinder/structural bulkheads (0.5 page)

15.6.3 Envelopes and mechanical interfaces between endcap strip system and outer cylinder/structural bulkheads (0.5 page)

15.6.4 Envelopes and mechanical interfaces between Strips and Pixels (0.5 page)

redundant with section 6?

15.7 Schedule for development, review and delivery (1 page)

15.8 Planned QA during production (1 page)

16. Common Detector Systems

Editor: Marcel Stanitzki
Chaser: Georg Viehhauser
Number of pages to write: 20
Scope of chapter:

16.1 ITk Environment (1 page)

overlap with DCS in section 13?

16.1.1 Dry gas (including supply and pipes) (1 page)

16.1.2 Common temperature and humidity sensors (0.5 pages)

16.1.3 Radiation monitors (0.5 pages)

16.1.4 Vibration measurements (0.5 pages)

16.2 Cooling (9 pages)

16.2.1 Introduction (0.5 page)

16.2.2 Requirements (1 page)

Reference to pixel requirements

16.2.3 The 2PACL loop and operational experience with it (1 page)

16.2.4 Layout and distribution system (1 page)

16.2.5 Plant (1 page)

16.2.6 Pipework to PP2 (Type III) (0.5 page)

Including vacuum insulation

16.2.7 PP2 (0.5 page)

Including thermal insulation

16.2.8 Type II pipes and warm nosing (1 page)

Including insulation

16.2.9 Control (0.5 page

16.2.10 Timeline for Design, Prototyping and Production (1 page)

16.3 Other external services (2 pages)

16.3.1 Type III/IV electrical cables (0.5 page)

Reuse or not?
Cable cooling

16.3.2 Electrical services at PP2 (0.5 page)

16.3.3 Type II electrical cables (0.5 page)

16.3.4 Fibre Cables

The fibre cables will run from PP2 at the end of the service modules to the counting room. As explained in section 10.3.1 we will use a short length of custom radiation-hard fibre spliced to a radiation-tolerant COTs fibre. There are several options for the fibre cable itself. The fibre cables installed for the current generation of LHC experiments are based on multiple ribbons within one cable. For example the SCT fibre cables have either 6 or 8 12-way ribbons inside a cable. The radiation hardness of the cable itself has been validated, so this type of cable would be an option for the ITk. However newer multi-fibre cables are now commercially available which achieve a higher fibre density than the multiple ribbon cables. There are cables based on fibres in loose tubes and with several of these tubes inside one cable. A schematic picture of one such fibre cable is shown in fig. 16.94.

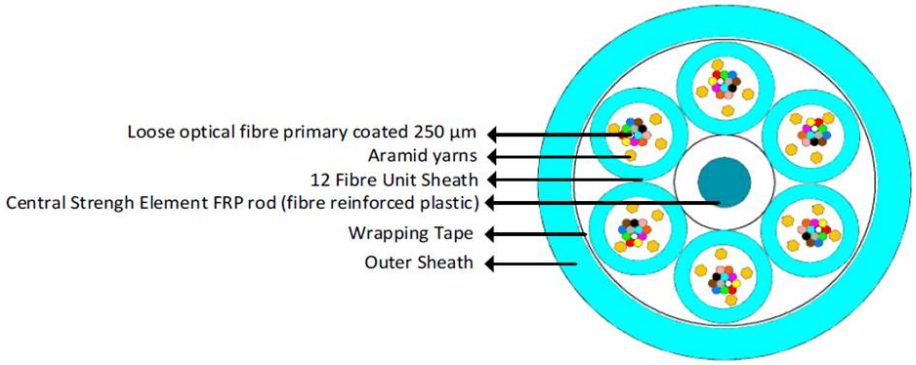

Figure 16.94. Schematic of a fibre cable with 6 loose tubes each containing 12 fibres.

The ends of the fibres will be terminated to MT/MPO connectors. These new cable types are attractive because they can achieve a higher fibre density and have smaller minimum bend radii than the multi-ribbon fibre cables. As these cables are symmetric, the minimum bend radius is identical for both directions unlike the multi-ribbon fibre cables, which would make cable routing much easier. Fibre cables are being investigated in the context of the VL+ project by the CERN-EN-EL-CF group. They will preform a market survey, test radiation hardness and install prototype cables to validate the design.

17. Integration and Commissiong

Editor: Phil Allport
Chaser: Carlos Lacasta
Number of pages to write: 15
Scope of chapter:

- *Transportation to CERN (barrel parts and full end-caps)*
- *Discussion of integration on the surface at CERN*
- *Details of strip integration*
- *Sketch of pixel integration*
- *Transportation of strip end-caps to CERN*
- *Commissioning procedure and timeline*
- *Transport from surface building to insertion position*

We plan to assemble the complete tracker, with all the sub-detectors and and internal (Type I) services installed and qualified, on the surface. The installation and commissioning time in the pit will therefore be minimized, limiting the exposure of operators to a potential harsh radiation environment, and the integration work could eventually be done in parallel to the decommissioning of the present tracker in the pit.

The Inner Tracker with all the subsystems and internal services will be delivered as a single unit into a cylinder of about 6.4 m length and an envelope diameter of about 2.25 m ready to be inserted into the LAr calorimeter bore and connected to the pre-installed Type II services.

We plan to build the tracker as a modular and hierarchical structure, where fully tested, contained components with simple interfaces (e.g. local detector supports like staves or petals, or modular service assemblies) are combined into progressively larger units. These modular components of the tracker are delivered to the surface integration site from the distributed assembly sites tested and ready for installation. The surface integration site should allocate space for the actual integration of the tracker sections, for the storage of the components, as well as infrastructure for reception testing of these components.

Pixels will be assembled in .... The strip endcaps will be assembled outside CERN (DESY and NIKHEF) and will arrive as a single unit ready to be tested and inserted. The barrel will be assembled into the OC at CERN.

Consecutively, the strip endcap and pixel systems will be inserted into the OC, thus closing all tracker barriers and a final check-out of the complete tracker can be performed on the surface.

17.1 Integration of the tracker

Integration will start with the Outer Cylinder (OC) mounted on a support frame, adequately dimensioned to maintain alignment and prevent any relevant deformation during the whole assembly

process, until the final transportation to the pit. The frame will in particular supply the necessary hoop stiffening for the OC during the times when the internal structural bulkheads cannot be present because of the installation of parts of the tracker. This frame could be the final installation cradle, in which the tracker will be lifted into UX15 and inserted into ATLAS.

Pixels will be assembled in .... The strip endcaps will be assembled outside CERN (DESY and NIKHEF) and will arrive as a single unit ready to be tested and inserted. The barrel will be assembled into the OC at CERN.

17.1.1 Barrel Strips

The barrel strip system will be populated with staves and type I services within in the OC, to allow for the installation of the final Type I services and to maximize the radius of the outermost tracking layer. Staves will be inserted from both ends into the barrel strip support structure. Once a wedge-shaped sector of about eight staves has been inserted a barrel strip service module is installed, and the staves are connected to the Type I services. On the end of the tracker the service module presents the final PP1 connector field to the outside and closes the thermal and humidity barriers in this area. During the assembly tests will be performed of individual local supports using temporary service connections to small scale detector infrastructure (cooling, readout etc.) at room temperature. Cold tests of the barrel strip system can be performed after the OC volume has been closed by temporary bulkheads.

17.1.2 Endcap Strips

The Strip endcaps will be assembledd outside CERN. One of the endcaps will be integrated at DESY and the second at NIKHEF.

A space will be needed to test each endcap as it arrives from CERN. The endcaps may stay in the transport cradle during those tests. A temporary thermal enclosure will be needed for cold tests to allow working on the barrel in parallel. After insertion cold tests will be done within the OC as with the barrel.

17.1.3 Pixel system

XXXXX

17.2 Transport of Components to CERN

Loren ipsum...

17.2.1 Barrel Strips

17.2.2 Endcap Strips

17.2.3 Pixel system

17.3 Transport to insertion position

Because of the size of the OC the insertion into the inner bore of the barrel cryostat will require ATLAS to be in the "Large Opening" configuration, which is the only one that provides a gap between the end-cap calorimeter and the toroid which is large enough for the tracker to pass. Minivans will

be installed on the ATLAS rails to provide a work platform inside the toroid, together with dedicated access tooling (rails, scaffolding, etc.). It should be noted that the transport frame for the OC needs to be added to the envelope in order to define the overall transport envelope.

The tracker will be lifted from the surface to the experimental cavern (UX15) by the surface crane (20 t capability). The shaft dimensions and the crane access zones allow the lowering and insertion on both sides. However, because of the space constraints in UX15, the lowering of the tracker is not straightforward. Two main scenarios have been identified and have to be evaluated in detail. In both of them, the tracker is lowered onto a rotating table, equipped with wheels or rollers, that will be used to carry the detector to the insertion position and align it to the cryostat inner bore. The first scenario is to lower the tracker directly onto the Minivans using the surface crane. Even if this option appears simple, the path that the hook of the crane has to follow is complicated, and the clearance to other ATLAS sub-detectors is very small in some places. The feasibility of this scenario is under study, and will mainly depend on the space available between the end-cap calorimeter and the barrel toroid.

The alternative lowering scenario has been described in the Letter of Intent [7]: The installation path for the tracker is through sector 1 on the US15 side of the cavern. The tracker is lowered down with the surface crane onto a platform above the end-cap calorimeter (position 1 in Figure 17.95). In this position the cavern crane is used to transfer the tracker from the top platform to a side platform erected on the cavern floor (position 2). The operation continues with the movement of the tracker between the calorimeter and the barrel toroid (position 3) and positioning the tracker on the rotation table (position 4). This insertion path requires careful guiding and a control of the insertion angle is necessary during this operation to avoid any damage to the tracker or surrounding objects. The operation could be done either using the cavern crane or using the rotating table as a trolley.

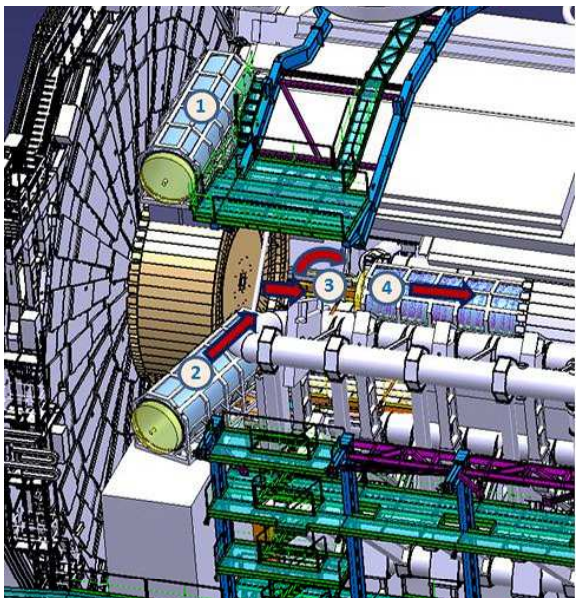

Figure 17.95. Insertion of the ITk: Lowering onto the end-cap calorimeter (1), followed by sideways insertion (2-4).

To allow for a clear assessment of both scenarios, it is mandatory to establish accurately what the clearance is in several locations. These studies are currently on-going and consist of the following steps:

- Measurement in the cavern of the critical distances: This has been done on the C side during LS1 as the components were in the appropriate position. Positions on the A side will be for now derived from these measurements and then checked during LS2.
- Construction of an 'as built' 3D CAD model of the ATLAS forward region using these measurements.
- Creation of as many cross-sections as necessary to establish the available space along the insertion path.
- Confirmation of the viability of the access paths with a dummy tracker during LS2.

It is already known that both scenarios require dismounting of some equipment (dismounting of Forward Platforms and Barrel Toroid vacuum line) in order to enlarge the space for passage for the ITk. The process above is a systematic approach that should result in the specification of the overall envelope for the Outer Cylinder plus its transport frame as well as a comparison of the two scenarios in terms of the space available.

The following was moved out of a different chapter, but still needs to find a better placement[IMG]

17.4 Full system tests

17.4.1 Barrel Test at SR1

17.4.2 End-cap Test at DESY and NIKHEF

- Electrical Interference
- trigger tests
- grounding & shielding
- operation

17.5 Preparation of labs for these tests

18. Installation

Editor: Marcel Stanitzki
Chaser: Georg Viehhauser
Number of pages to write: 20
Scope of chapter:

18.1 Radioprotection and personal safety during installation of the ITk

18.2 Preparations of cryostat before ITk insertion

18.2.1 Installation of rails

18.2.2 installation of outer polymoderator

18.3 Installation of external services (Type II/III/IV and PP2)

18.4 ITk transport

18.4.1 Transport from surface integration site to Bldg 3185

18.4.2 Lowering of ITk into insertion position

18.4.3 Insertion of ITk into cryostat

18.5 Service connection at PP1

18.6 Time and manpower estimates

19. Schedule from TDR to Installation

Editor: Ingrid-Maria Gregor
Number of pages to write: 20
Scope of chapter:

- *Gantt Chart with description of possible pit falls*
- *Gantt Chart with major construction milestones, internal (ITk) and external (ATLAS) reviews following standard review scheme*
- *Gantt Chart steps to purchase*
- *Technical risk and critical path analysis*
- *Risk mitigation in case of failure*
- *Guidelines from LHCC on the level of detail would be appreciated*

so far only some scheduling text from the ASICs section .... IMG

The submission of the full scale ABCStar chip will follow a second prototype FE submission to ensure all measures taken to control the noise are effective. The FE prototype is to be submitted in May 2016 and evaluation both before and after irradiation will take place between October 2016 and January 2017. Redesign work of the FE will start as soon as results from the prototype are available and is due for completion in Q2 2017.

Work on implementation of the ABCStar functionalities and on the verification will continue throughout 2016, followed by place and route in early 2017. Submission of the ABCStart chip is planned for end of Q2 2017.

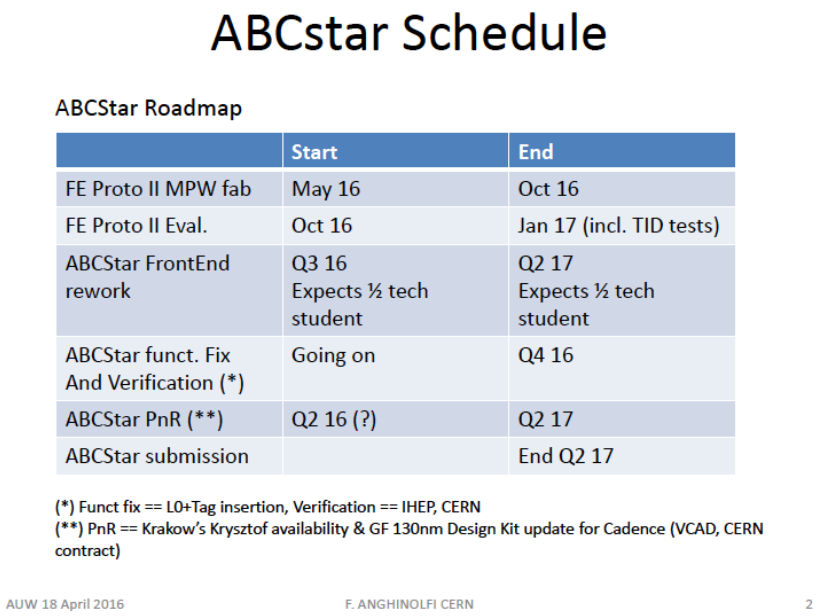

Figure 19.96. ABCStart design and submission schedule.

20. Test Beam during Production

Editor: Ingrid-Maria Gregor
Chaser: Susanne Kuehn
Number of pages to write: 10
Scope of chapter:

- *Planned future full system tests*
- *Test beam of a detector segment - to be defined*
- *Test beams for samples during production*

20.1 Overview

20.2 Test beam studies at pre-production and production phase

20.2.1 Test beam of pre-production components

Performance, efficiency, charge collection, spatial resolution, noise occupancy, pulse shape vs. HV, incident angle of beam, magnetic field, operating modes of front-end electronics

20.2.2 Cosmic ray test stand for petals and staves

20.2.3 Tests of detector segment

Electrical tests, electronics, readout, NO of full petal/stave, optimization of configuration. Tests vs. operating modes of front-end electronics, HV. Noise injection tests: from power line, from cooling pipes electrical intereference of several petal/staves.

Grounding, Shielding tests
Power consumption vs. temperature, time
HV stability

- mechanical tests, metrology
- cooling tests, different temperatures, operation, CO2 tests
- electrical intereference of several petal/staves
- trigger tests
- long-term tests
- If possible test beam of one petal, stave

21. Production Model

Editor: Uli Parzefall
Chaser: Andy Blue
Number of pages to write: 30

21.1 Overview

The build of the ITk strip tracker involves both a range and quantity of objects that far exceed the build of the current ATLAS strip tracker (SCT). For example, the number of silicon strip modules for the barrel has increased from 2,112 to 10,976, and for the endcap from 1,976 to 6,912. This is equivalent to a 388% increase in the number of modules required during the production phase of the project. Such a significant increase in the number of modules (and their associated components) has focussed efforts on improving in every way the ease of construction and affordability during the production phase.

This effort to streamline the assembly process is also what has driven the development of the local support concept. In the current SCT, large numbers of modules were mounted serially on a relatively small number of large-scale structures (four in the barrel and 18 for the endcaps). For the ITk groups of 28 barrel modules will be mounted onto the stave and groups of xx modules on to each endcap petal. These local support structures form completely independent and fully functional sub-systems and ensure that the time between the start of the assembly of a particular module to a test in its final operational environment is as small as possible. To achieve the best possible outcome, it is important to define a production model in which the rates of module assembly and local support manufacture are well matched.

The production model for the ITk strip tracker modules will be heavily based on both SCT experience and R&D developments since the IDR. Many build steps and QA / QC processes are already designed in a scalable, modular way, and production and testing rates have been estimated (and measured where possible) for all objects. Monitoring of the production process will be carried out via the ITk production database and cluster site managers who will be responsible for ensuring that all the relevant data is up-loaded in a timely manner and for reporting progress to the ITk.

In the remainder of this chapter we describe the work breakdown structure for the project and a summary of the division of responsibilities and reporting lines. We then show how the manufacture of both the barrel and endcap modules will be shared out into 'clusters' and summarise the component flow. We then discuss the manufacture of those components which are required in very large numbers (sensors, hybrids & modules), the construction database and the quality control and assurance schemes to be adopted.

21.2 Work Breakdown Structure

The WBS for the ITk strip tracker is shown in the table 21.25 below .

Table 21.25. Work Breakdown Structure for the ITk strips

21.3 Assembly Clusters

The construction of the barrel and two endcaps will be the responsibility of four assembly clusters; two for the barrel (B1 and B2) and one for each endcap (A & C). It is anticipated that some sub-components may be procured or manufactured by a single cluster on behalf of the others. Such items may include module power boards, AMAC ASICs, HV multiplexers and EoS cards.

For the barrel, each cluster will be responsible for the delivery to CERN of half the total number of staves required and will share the responsibility for the integration phase together with the ITk. For the endcaps, the two clusters will each be responsible for assembling one complete endcap sub-system and delivering it to CERN. They will then be jointly responsible for preparing the endcaps for integration with the barrel part. All clusters will share the work relating to the final testing of the ITk on the surface and the subsequent commissioning once the ITk is installed in ATLAS.

Clusters	ASIC probing	Sensor Probing	Hybrid Assembly	Module Assembly	Bus Tapes	Stave/Petal Core Production	Stave/Petal Mounting
Endcap A							
Endcap B							
Barrel 1 (UK)							
Barrel 2 (US)							

Figure 21.97. Breakdown of Production and Testing sites for all clusters.

21.4 Division of Responsibilities and Reporting Lines

During production the day-to-day management of the high-level deliverable (eg a number of staves, one endcap, etc) will be the responsibility of the management team for each cluster. Within each cluster, each top-level WBS element (eg. 1.2.1, 1.2.2, 1.2.3, etc) will have a WBS task leader who is responsible for overseeing the execution of a particular WBS task within their cluster. The Cluster WBS Task Leader will also be jointly responsible, with their colleagues in their partner clusters, for the distribution of sub-components and the monitoring of the production rate and quality control data. Each top-level WBS element will have one (or more) WBS Task Co-ordinator(s) charged with holding periodic WBS Task meetings and generating reports for the strip tracker project management team and PL. The PL will organise regular meetings of the project management team who will review progress, discuss technical issues, monitor the quality control data and pass down information to the clusters as required. The PL will report progress to the ITk PL, ATLAS management and LHCC as required.

Within each cluster, all their WBS Task Leaders will hold regular meetings to report on progress and discuss any local issues of either a technical or schedule nature. These Cluster Management Meetings will then be responsible for reporting to the relevant funding agencies.

21.5 Product flow chart and schedule

Figure 21.98 shows the parts flow involved in the manufacture of a completed stave or petal. One barrel stave will involve the assembly of 30 modules consisting of 60 hybrids and 600 ASIC purchased from industry and their mounting on a stave core. The core is made from two bus-tapes, two EoS cards and a number of small components procured from industry plus raw materials such as carbon-fibre pre-preg, honeycomb, thermally conducting foam and titanium tube which have to be processed into sub-components and then assembled into a stave core. The manufacture of modules requires the reception testing of vast numbers of sub-components, high-speed assembly and an efficient quality control regime whilst the assembly of a stave core requires relatively few parts but a large effort in processing, assembly and quality control.

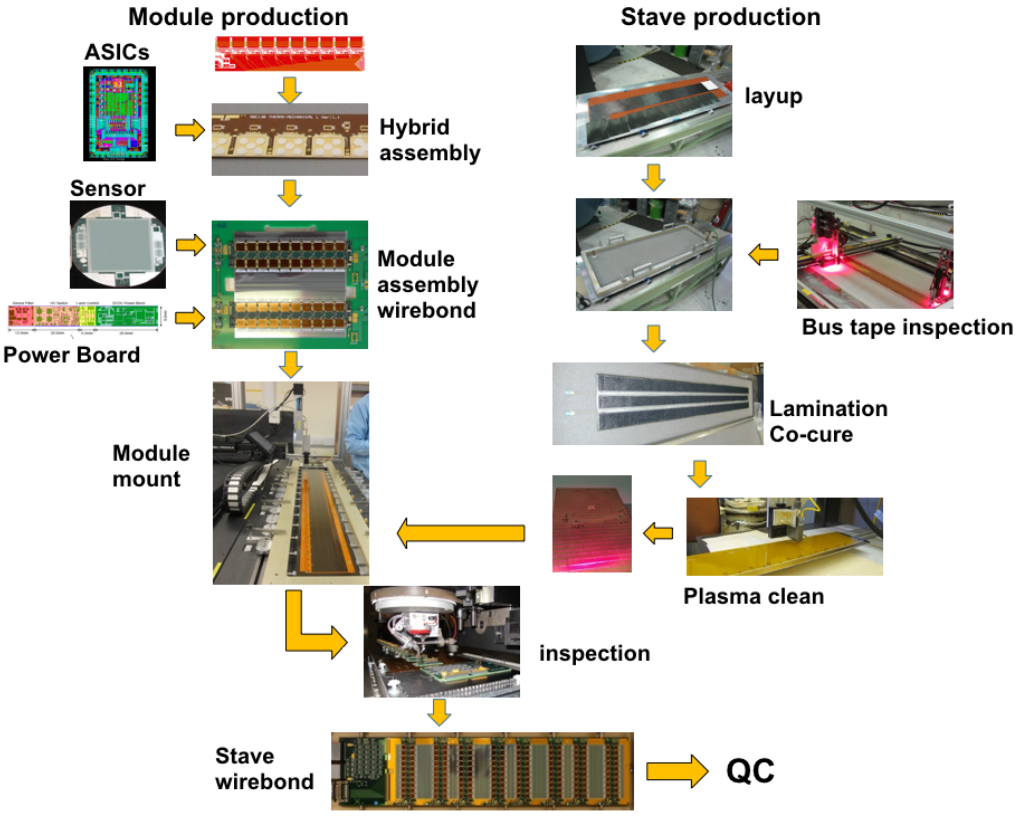

Figure 21.98. Product flow chart for a full stave or petal.

21.6 Production Database

Key to the build will be the production database, which will be used to track all components in regard to their geographic location and utilisation through the course of the build, as well as serve a vital function during operation for potential fault finding. However unlike for the current inner detector, there will be only 1 central database for the entire ITk, covering not only strip barrel and endcap components, but also all pixel and common mechanics parts.

21.6.1 Responsible Institutes

The ITk production database (PD) is being prepared in Prague with following scheme of responsibilities introduced inï£¡fig 21.99

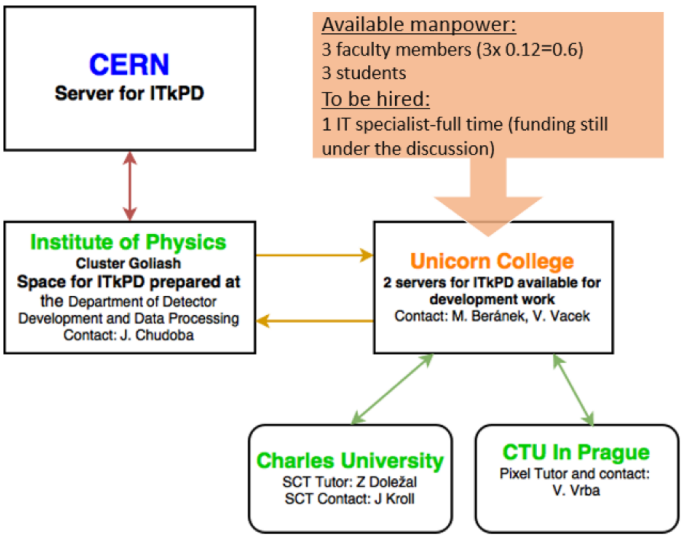

Figure 21.99. Map of the ITk PD development consortium in Prague

The group of following institutions has established a cooperation for the production database development in Prague during summer of 2015: The Institute of Physics (hosting a mirror of the PD that will be physically located at CERN), Unicorn College (the main IT developer), the Charles University and the Czech Technical University. The PD still keeps a strategy that has been layout by D. Robinson (MySQL database with Java uploaders) and has been already tested using data from Oxford University tape production. There are several modifications proposed to the original PD strategy development and they are briefly described in the following section. It is also suggested to include a responsive feature on mobile devices besides a planned standard terminals access.

21.6.2 How it will work

We have designed the ITk PD as a centralised web application with an universal API. The ITk PD will be accessible from the web application or API (see Fig 21.100) All business logic, rules and configuration will be centralised in the ITk PD. The API will be fully documented and will be accessible to the 3rd parties. The API will be designed as a RESTful and will be accessible via HTTPS.

Significant products (entities) of the ITk PD and their relations are depicted in Fig 21.101 The ITk PD will mainly store components and assemblies (Staves, Petals, Modules, Hybrids, etc.). The component is represented by an item (e.g. ASIC chip) or batch (e.g. tape). Components or other assemblies can be combined into a new assembly. The database will facilitate to track iterations of a component/assembly during a production phase.

The ITk PD will allow to store test results and related information (attachments), as well as shipments of components and/or assembly status. The database will be designed both for Strips and Pixels needs.

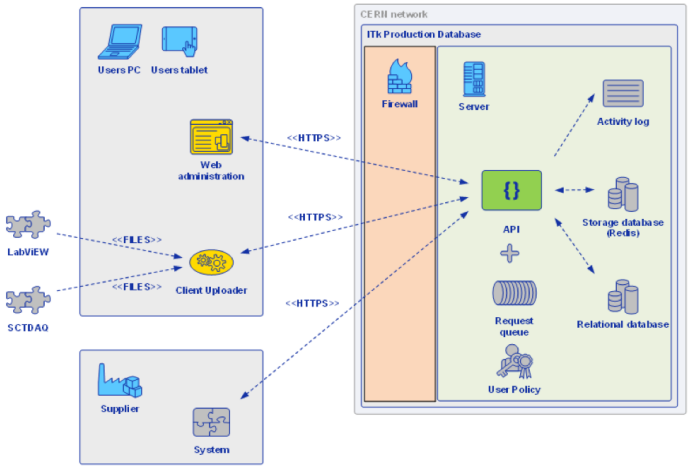

Figure 21.100. Suggested deployment diagram of the modified ITk PD

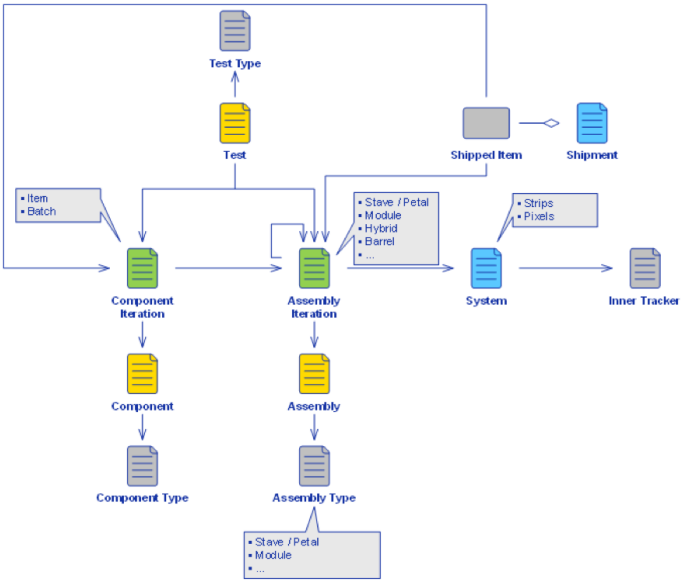

Figure 21.101. Suggested product view of the the ITk PD

21.6.3 Differences to the current SCT database

The current database design in Fig 21.102 represents a highly utilitarian design that meets the large portion of the strip community needs. It follows the same generic principles of the original SCT production database but it uses generic tables and avoids new tables for every new test. Business logic is distributed in client uploaders and web scripts but so far with no ?safety-net? for a developer. It is still lacking some functionalities (i.e. shipments and clear distinctions between basic structure components).

The main differences between the originally suggested SCT database and the modified ITk PD at present

- It will have centralised business logic. Currently, it is stored at local Java Uploaders as it is

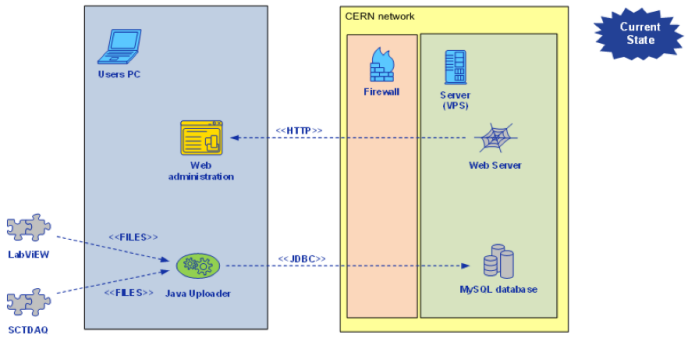

Figure 21.102. Simplified schematics of the originally suggested Strip ITk PD

depicted in Fig 21.102. In another words any update needs to distributed new version of Java Uploader.

- It will support tracking of shipments, which the current version still do not has.
- It will allow to manage access rights and user permissions.
- It will be designed as a centralised web application with standardised API accessible via HTTP (RESTful API).
- Web administration will have a responsive design that can be comfortably used on mobile devices.

21.6.4 Serial Numbers

There is a proposed new convention for the serial numbers to be used for the components parts of the ITk. The purpose of the serial number is to identify an item and relate it to a record in the construction database. Where possible the items should be labelled by a graphical code (bar, QR or similar code), which will be used to retrieve the corresponding record from the database. A serial number readable to humans is not required, although it might be convenient in some cases. Labelling by numbers will only be done where the space is easily available.

Previous Practice

The serial numbering of the ATLAS ID followed ATC-OQ-QA-2040 (Figure 21.103) The System

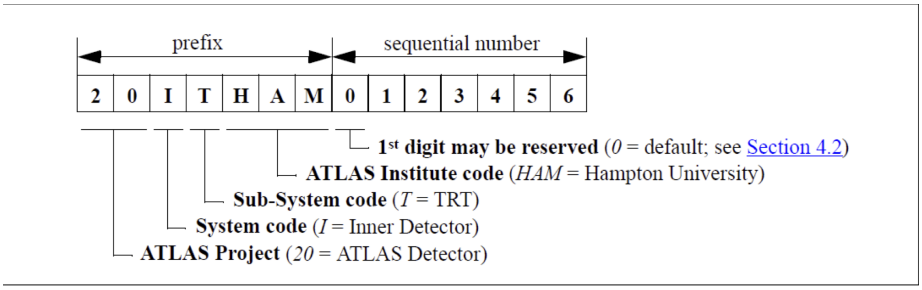

Figure 21.103. Structure of the ATLAS Part Identifier as defined in ATC-OQ-QA-2040.

and Sub-System codes listed in here have been defined in ATC-OQ-QA-2031 (Table 21.26). In the past in practice the alphanumeric code defined here have been replaced by a numeric code also listed. As this has been done throughout the project the 3rd digit has been completely used up, if only numbers are used.

Alphanumeric Code	System	Numeric Code
IP	Pixel Detector	21
IS	Semiconducter Tracker	22
IT	TRT	23
IC	Common Items	24

Table 21.26. System and Sub-system codes in ATC-OQ-QA-2031. Also listed is the numeric code used in the past.

Expected number of parts

As has been discussed earlier in this chapter, the likely number of numbered items in the ITk will be of the order of 10^6, and with high likelihood less than 10^7. Note that the intention is that all items in the ITk will be traceable, which entails that more serial numbers will be needed than in the ATLAS ID, where many integration items were not numbered. In principle the number space in the original ATLAS numbering convention with seven digits allocated for serial numbers appears sufficient for this.

Block booking vs randomly allocated serial numbers

In the past serial numbers have been allocated by block booking. The disadvantage of block booking serial numbers is that it results in inefficient usage of number space, because serial numbers are typically chosen to allow for easy human identification, and even if this is not the case, paddings need to be included to allow for an overflow of part numbers (prototypes, spares, reworks, etc.).

Random allocation of serial numbers requires a central serial number allocation server, which is reliably accessible from all construction sites at any time. In practice this would be the construction database. However, as this database is currently still under heavy development and not yet used by all aspects of the project, it seems that this service will not be available within the near future. While it would be beneficial to train users to use the database already from early on (also for prototypes) and the need to register items with the database for a serial numbers would provide such an incentive it is likely that without a real infrastructure in the database for certain items users will not use this feature and rather rely on private, more or less organized ways to keep track of items.

Therefore the current plans is to use block booking as detailed below. As a consequence we expect that the number space of 10^7. as available in the old serial number scheme will not be sufficient.

Alphanumeric vs numeric characters

The original ATLAS numbering scheme (ATC-OQ-QA-2040) does in principle allow for the use of non-numeric characters in the serial numbers. In practice this has been avoided in the ID (even system, sub-systems and institute codes have been converted into numbers). However, as has been explained above, the third digit for the 20 (ATLAS detector) serial numbers has been used in current ATLAS for the numbers 1-9. It seems therefore reasonable to start using alphanumeric characters in the more global designations of the item. However, for the actual serial number alphanumeric numbering schemes are likely to be not intuitive and could lead to misunderstandings (with the possible exception of hexadecimal numbering, although this seems to be a rather nerdy approach).

Institute identifiers

The ATLAS ID used in current ATLAS (ATC-OQ-QA-2040) uses institute identifiers. This makes sense for assemblies which are put together at one institute out of a larger group of possible production sites (typically for modules). However, in the future we want to trace more levels of assembly and integration (modules, staves, barrels/disks, etc.), which can be spread over many different sites for one assembly. We also plan to store data for assemblies which will only be produced at one site, sometimes because we only need only a small number of this assembly. In all these cases the reasoning for an institute code appears weaker. However, for assemblies where a human-readable institute identifier is deemed beneficial we should provide for the use of such an identifier as part of the serial number.

Proposed numbering scheme

The current proposal is to use a serial number with the following serial number scheme

'20 U xx yy nnnnnnn'

with

21.7 Old QA section

21.7.1 Documentation

The documentation used for the ITk strip build is strongly based on the previous SCT experience. It is planned that all production sites will have their own webpages, and this information will be aggregated into the corresponding central cluster site/database. This allows for greater control of parts and component stocks, and faster reporting of yield rates and possible build issues. Travel sheets will be used for movement of objects throughout the build, and documentation will also be written outlining in detail the assembly and testing procedures needed for production sites. As an example, it is envisaged for module production sites there shall exist;

- Module Assembly: Operator's Guide
- Module Wire bonding guide
- Mechanical survey procedures
- Electrical testing procedures
- ESD and testing specifications

20	Code ATLAS detector
U	Phase II ATLAS upgrade
xx	project/subproject code PI - inner pixels PB - outer pixel barrel PE - pixel endcapsl PC - pixel commonl SB - strip barrel SE - strip endcaps SC - strip common CM - common mechanics CE - common electronics
yy	sub-project specific block identifiers (could be MS for short-strip modules LA for A-side local supports etc.)
nnnnnnn	7-digit numerical serial number, A subset of these digits (TBD) can be used for an institute identifier (format and position to be defined)

Table 21.27. Proposed Serial numbers for ITK.

21.7.2 Storage, Transport & Tracking

During production, there will be a large number of parts being transported between institutes. It is essential that all component parts are tracked, transported and then stored in an agreed way.

Where possible all objects will be stored in line with the IPC/JEDEC J-STD-033B.1 standard for storage of components. This requires

- < 5% Room humidity sustained
- Recovery to normal conditions < 1hr
- The use of dry air, N_2 and active desiccant

Objects that will adhere to this standardisation will include ASICS, hybrids, sensors and modules. Consequently, many parts of the build will be be performed in clean rooms [specs]

Transport

During production there will be considerable movement of high value items between sites. Consequently shipping and transport strategies have been outlined for many areas of the production. Fig ((21.104a) shows the transport box designed for the barrel modules, which has successfully been used for shipping thermo-mechanical modules between US, UK and Germany.

Testing before and after transportation of a 250nm endcap module from DESY Zeuthen to DESY Hamburg showed no degradation in electrical performance Fig ((21.104b). Custom transport boxes also exist for hybrid panels, along with commercially available systems for ASIC wafers and sensors. Specifications exist for the shipment of Local Support cores along with the methodology

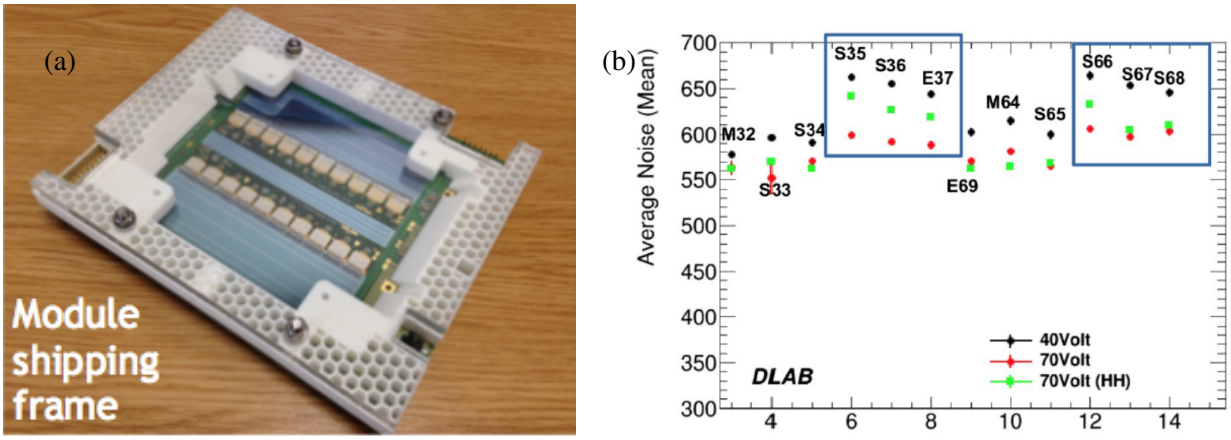

Figure 21.104. a: Example of the transport box for Barrel Modules; b: Measurement of noise performance of an endcap 250nm module before and after shipping from DESY Zuethen to DESY Hamburg.

for transportation of fully assembled stave and petals. Investigations have also been made into measuring the maximum force experienced by transport boxes using commercial shipping. An accelerometer was fitted to a module transport box and shipped from RAL to DESY Zeuthen (Fig 21.105)

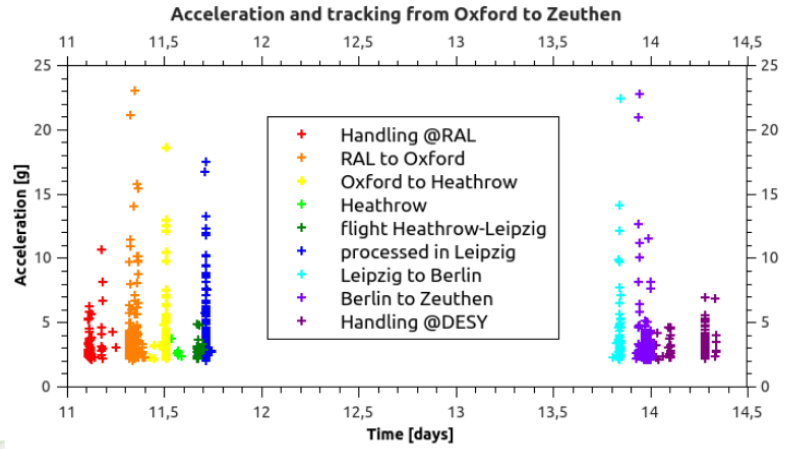

Figure 21.105. Acceleration tracking of module transport box from RAL to DESY

Tracking

To assist with tracking, all hybrids will be mounted with a LXMS31ACNA-010 RFID. It incorporates industry standards IC, and supports a frequency range of 865-955MHz, allowing to cover all globally relevant UHF frequency bands. Each RFID comes with the following memory allocation:

- EPC memory (Electronic Product Code): 240 bit unique device ID
- User memory: 512 bits
- TID: 64 bits, unique address assigned by the IC manufacturer

This then allows for a hybrid (or subsequently assembled module) to be coded with information such a serial numbers, test results or institute history. Information contained on each hybrid will then be written or read out out with a RDIF reader at the relevant institute. For larger items (such as staves & petals), barcodes will used be for item identification. For both barcodes and RFID, item identification will conform with serial number codes, which are outlined in the next section.

21.8 Production rates required for high number items

There are several steps of the build - sensor probing, hybrid and module assembly - that require a high number of parts, and consequently necessitate high production rates. For this reason an effort has been made to maximise the industrialisation and parallelisation of all the build steps. Examples include the manufacture of multi-hybrid panels [ref], use of UV cured glue to minimize assembly time [ref] and multi-module testing crates [ref].

For each component, the scope of delivery depends on the yield for that part together with the multiplicative final yield of all subsequent assembly steps which might result in a good part not making it into the final detector. For example, once a hybrid is glued onto a silicon sensor it is committed irrevocably; if the sensor gets damaged during wire bonding, module testing, module mounting, Local Support testing or integration that hybrid (possibly 2) is lost. Production rates have been calculated for those tasks of the build that will demand high production throughput and taking into account the component-to-ATLAS yields. The data is presented in term of work days, where it has been agreed to take one production year as 200 days (40 weeks). Due to the split of the build cluster sites (2 clusters for the barrel, and 1 for each endcap), rates have been calculated in relation to 50% of the barrel and 1 Endcap. Data are shown for the production length of 3 years. However numbers for 3.5 and 4 years exist too. A range of porduced parts will be shown between 100% and 115% (the latter number is based on the previous SCT module production figures.)

21.8.1 Modules

The most challenging part of the build has been thought to be the module production, due to the wire bonding time, the long curing time of the hybrid to sensor gluing, and the scalability of long-term testing. Table 21.28 and 21.29 show the module production rates needed for both 1/2 barrel and 1 endcap respectively. Work continues on methods to reduce the time for multi module assembly, including the use of UV-cure adhesive, multi module wire bonding jigs, the electrical testing of front end bond failures whilst wire bonding and the automation of module metrology.

These tables allow us to estimate number of modules that would be required to be assembled, wire bonded and tested. However, for greater clarity, rates are show as a function of number of wire bonds. This is due to the mixture of long and short strip modules for the barrel (Table 21.30), and the range of module needed for the petal. (Table 21.31)

21.8.2 Hybrids

Similarly to module production rates, hybrid build rates have been calculated in respect to half the barrel (Table 21.32) and 1 endcap (Table 21.33) over a 3 year period. The panelisation of the hybrids allows for parallelisation (up to 8 hybrids/panel) of the wire bonding and testing steps. In

Modules		No of Barrel Module Institutes				
% Made	No. made	2	3	4	5	6
100	5488	4.57	3.05	2.29	1.83	1.52
105	5762	4.8	3.2	2.4	1.92	1.6
110	6037	5.03	3.35	2.52	2.01	1.68
115	6311	5.26	3.51	2.63	2.1	1.75

Table 21.28. Production rate estimates for modules per day for 50% of the Strip barrel. Based on 3 years at 200 working days per year

Modules		No of Endcap Module Institutes				
% Made	No. made	2	3	4	5	6
100	3456	2.88	1.92	1.44	1.15	0.96
105	3629	3.02	2.02	1.51	1.21	1.01
110	3802	3.17	2.11	1.58	1.27	1.06
115	3974	3.31	2.21	1.66	1.32	1.1

Table 21.29. Production rate estimates for modules per day for 1 Endcap. Based on 3 years at 200 working days per year

Wire Bonds		No of Barrel Module Institutes				
% Wire Bonds	Bonds made	2	3	4	5	6
100	18,926,520	15773	10,515	7,887	6,309	5,258
105	19,8728,46	16,6561	11,041	8,281	6,625	5,521
110	20,819,172	17,350	11,567	8,675	6,340	5,784
115	21,765,498	18,138	12,092	9,069	7,256	6,046

Table 21.30. The humber of module wire bonds per day for the 1/2 barrel . Based on 3 years at 200 working days per year

Wire Bonds		No of Endcap Module Institutes				
% Wire Bonds	Bonds made	2	3	4	5	6
100	11,010,048	9,176	6,117	4,588	3,671	3,059
105	11,560,550	9,634	6,423	4,817	3,854	3,212
110	12,111,053	10,093	6,729	5,047	4,038	3,365
115	12,661,555	10,552	7,035	5,276	4,221	3,518

Table 21.31. The humber of module wire bonds per day for 1 endcap . Based on 3 years at 200 working days per year

addition the envisaged use of UV curing glue reduces the assembly time, as well as the necessary jigging, vacuum lines and tooling for such high throughput rates.

Hybrids		No of Barrel Hybrid Institutes				
% Made	No. made	2	3	4	5	6
100	7392	6.16	4.11	3.08	2.46	2.05
105	7762	6.47	4.31	3.23	2.59	2.16
110	8131	6.78	4.52	3.39	2.71	2.26
115	8501	7.08	4.72	3.54	2.83	2.36

Table 21.32. Production rate estimates for hybrids per day for 1/2 barrel. Based on 3 years at 200 working days per year

Hybrids		No of Endcap Hybrid Institutes				
% Made	No. made	2	3	4	5	6
100	4992	3.57	2.38	1.78	1.43	1.19
105	5242	3.74	2.5	1.87	1.5	1.25
110	5491	3.92	2.61	1.96.	1.57	1.31
115	5741	4.1	2.73	2.05	1.64	1.37

Table 21.33. Production rate estimates for hybrids per day for 1 endcap. Based on 3 years at 200 working days per year

21.8.3 Sensors

A range of sensors will have to be probed for characterisation studies before use for module production (2 variants for the barrel and 5 for the endcap). The required rates for the barrel and endcap sensors are shown in Table (21.34) . Custom probe cards used in semi-automatic probe stations will allow for high throughput of probing.

Sensors		Probed Sensors per day	
Years	Days	Barrel	Endcap
1	200	57.63	36.29
2	400	28.01	18.15
3	600	19.21	12.10
4	800	14.41	9.07

Table 21.34. Production rate estimates for sensor probing per day for the ITk strips tracker.

21.9 Site qualification

Before production starts, every construction site that is expected to build or test components will have to pass a site qualification validation. This is designed to demonstrate that the particular site has the ability to build their deliverables and measure the uniformity of test results across several clusters/sites to understand assembly yields.

The key points of site qualification will include;

- All the necessary equipment, infrastructure and personnel to execute the task exists
- All documentation, operating instructions and component build sheet check lists exists
- Procedures for tracking components, uploading test results and evaluating yield statistics exist
- A demonstration of the ability to assemble a number of pre-production pieces
- A demonstration of the ability to manufacture components which give test results compatible with other sites
- Verification that all results are in the PD ad visible to all sites.

For site qualification is it envisaged that ?? % of items shall be produced by each cluster/institute

22. ITk Strips Quality Assurance

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22.1 Introduction

All on-detector components will have to operate reliably for 10 years with little or no maintenance. Therefore ensuring high reliability of all these components is an essential part of our programme. This section gives an overview of our approach to reliability engineering and the resulting Quality Assurance programme. A brief description of some of the proposed procedures is given.

22.2 Quality Assurance & Reliability

It is important to make a distinction between Quality Assurance (QA) and Quality Control (QC) tests that will be carried out during both pre-production and production. Quality control (QC) tests are performed on every production item, validating their performance compared to agreed specifications. The tests should include stress tests to eliminate or at best reduce infant mortality (eg ASICs). Quality Assurance (QA) tests are statistical studies of quality during R&D and on a batch basis in production. They are aimed at improving product reliability during R&D. and monitoring consistency during production. This generally involves "destructive" testing. The tests generally involve more extreme stresses for devices than will be experienced during normal ATLAS operation. The functionality of the devices will be measured before and after the stress tests. These will generally involve running the QC tests. The types of stresses used are typically, elevated or reduced temperature, rapid thermal cycling (sometimes called "thermal shock") and elevated operating voltages. We are also investigating the use of vibration testing to study mechanical reliability. All on-detector components require radiation testing to validate the radiation tolerance. However the nature of the radiation testing is very device dependent and therefore these tests are described in the relevant sections of the TDR. The tests are therefore considered destructive in the sense that these parts will not be used in the final detector, even if they are fully functional after the stress tests. The tests will be used on a statistical basis to validate the quality of the parts. If there are excessive failure rates, we will perform a post-mortem of failed devices to understand the failure mode or change the device to a more reliable one or optimise the design to reduce the stress experienced in ATLAS operation. Table 22.35, below, shows examples of planned QA and QC tests for parts during the build.

22.2.1 Common Voltage & Temperature tests for all objects

Since the ITk IDR, there has been a focus to standardise the voltage and temperature ranges used for all component testing across different components. This is done to guarantee all components are tested to the required limits, to avoid unnecessary testing as a component goes through the relevant assembly stages and allow sites to plan and purchase the necessary equipment.

Voltage Ranges

In order to optimise the signal-to-noise ratio we are considering operating the detectors at a voltage of up to 700V. The silicon sensors themselves will only be tested up to this voltage but all the cables (off-detector and bus tapes) providing the high voltage will be tested to double this value.

Test	Sensor	ASICs	Hybrid	Module
QC	Probe Testing	Probe Testing	Electrical functionality Burn in	IV Electrical functionality Thermal cycling
QA	Mechanical stress	Extended temperature and voltage	Thermal cycling	Thermal cycling

Test	Bus Tape	Local Support	Optoelectronics
QC	Open / shorts HVIR Geometry	Geometry Bending stiffness Thermal performance	Power and responsivity BER and eye-diagrams
QA	Thermal cycling	Thermal cycling	Elevated temperature and humidity

Table 22.35. Examples of planned QA and QC tests for parts during the build phase. HVIR = High Voltage Insulation Resistance, BER = Bit Error Ratio.

Temperature Ranges

The coolant temperature is foreseen to be -35C$^\circ$ during normal operation. However the detector will be operated warm during integration and commissioning in order to be above the dew point. The increase in temperature from the cooling fluid to the active components is know form FEA calculations and thermal measurements. When switching the cooling on or off, the ramp rate is expected to be $\sim$ 1C$^\circ$/s. Therefore the rapid thermal cycling required for meaningful stress tests should involve significantly faster ramp rates.

22.2.2 QA for sensors

need input from Bart

22.2.3 QA for ASICs

The reliability of ASICs has not been a major concern for the current generation of experiments. However the reliability of newer deep sub-micron technologies might be worse because of the increased current density and the use of thinner gate oxides. The reliability of the current generation of GBTx will be studied using the physics of failure. The mean time to failure (MTTF) will be measured for batches of ASICs operating at different temperatures and elevated voltages. Different failure mechanisms have very different dependencies on temperature and voltage. For example hot carrier injection (HCI) is more severe at lower temperatures, while electro-migration is worse at high temperature. Therefore statistical fits will be performed on the MTTF data taken at different conditions to fit the relevant model parameters. These fits will then be used to predict the MTTF for the expected operating conditions. If these studies are successful, this methodology will be used for the production ASICs.

22.2.4 QA for hybrids

Hybrids will be produced in panels allowing for test structures to be laid out in the sacrificial area of each panel. Long lengths of narrow tracks will be used and the measurement of the resistance will monitor the quality of the etching. A Daisy chain of a large number of vias will be included. The continuity of this chain will be measured before and after rapid thermal cycling in order to

validate the reliability of the vias. Wire bond pull strengths will be measured on a batch basis. *This section needs to be checked by Ashley*

22.2.5 QA for modules

need input from Ashley/Tony

22.2.6 QA for bus tapes

TW: to be consistent the radiation tolerance should be move to the bus tape section The radiation tolerance of the acrylic epoxy used to laminate the layers was studied by irradiating short length samples of laminated tapes. Peel tests were performed on samples with and without exposure to an ionizing dose of 500 kGy(Si). A decrease in peel strength was observed after radiation but the peel strengths were still so high that this is not a significant problem. In addition the robustness of the irradiated laminated tapes was checked by repeated insertion in liquid Nitrogen which did not create any delamination.

The bus tapes contain a sacrificial area which is removed at the end of the stave mechanical assembly. Long narrow lines will be laid out in this area for QA trials. The continuity of the long lines will be measured before and after rapid thermal cycling. A large area pad will also be included that can be used for wire bond pull strength trails. The first such tests on prototype tests gave excellent results with a mean pull strength of 10.0 g and an RMS of 0.88 g. These tests will be performed on a small fraction of the production tapes. The reliability of prototype tapes is being assessed with rapid thermal cycling. A blow-off CO_2 cooling system is being used to rapidly thermally cycle a thermo-mechanical stave while the electrical resistance of all narrow lines are measured. The ramp rate is $\sim 3C^{\circ}/\mathrm{s}$. If this is successful, liquid nitrogen tests will also be used to achieve much higher ramp rates.

22.2.7 QA for local supports

QA tests will be performed on cooling pipe assemblies on a batch basis. The stresses used will involve over-pressure tests and rapid thermal cycling. *to be checked with Richard French.* The mechanical reliability of the local supports will be studied on a batch basis using rapid thermal cycling. This will be performed using a blow-off CO_2 cooling system. A small number of staves (petals) will be used for QA studies. These stress usesd will be rapid thermal cycling with a blow-off CO_2 system.The thermal performance before and after thermal cycling will be measured using the infra-red imaging used for the stave QC tests. Visual inspection will also be performed to look for evidence of delaimination. *This section needs input/corrections from Graham Beck*

22.2.8 QA for Optoelectronics

The reliability of VCSELs will be studied using accelerated ageing tests at 85°C and 85% relative humidity (RH)on a sample basis. The tests will measure the LIV (optical power, current and voltage) thorough the test. LIV scans will be performed periodically. Optical spectra will be taken before and after the test. Small changes in the widths of the spectra are sensitive to the loss of higher order modes, which has been demonstrated to be a very sensitive measure of VCSEL degradation. The tests will be run for at least 1000 hours which is sufficient to give high confidence in the long

term operation. First tests were performed with hermeticity packaged VCSELs[7] in TO cans. 19 VCSEL channels were studied and they all survived 1300 hours of the 85° and 85% RH test. There were no significant changes in the widths of the optical spectra after the test. In order to study the mechanical reliability, thermal cycling is being used. The temperature range was $-35C^{\circ}$ to $+45C^{\circ}$, however the ramp rate was very low and we are therefore considering the use of an air-jet system that could have a ramp rate of greater than 10C°/s. These tests are now being performed on a candidate small form-factor package which is not hermetically packaged. The same tests will be used to validate new VCSEL packages being developed by the VL+ group. The reliability of transceivers will also be studied. We have developed a test system to allow 11 channels of VTRx to be tested simultaneously in an environmental chamber. The performance of the VTRx under test will be determined by a loop back system. Psuedo-random Bit Sequence (PSRB) data is sent from a VTRx outside the chamber, via an optical switch to a VTRx inside the environmental chamber. An electrical loop back is used for each transceiver so that the data is then returned to the VTRx outside the chamber, such that the Bit Error Ratio (BER) can be measured. The switch allows the one VTRx outside the chamber to monitor the performance of all 11 channels under test. This system will be used to study the reliability of the VL+ VTRx prototypes as they are developed. It will also be used to study the reliability of production items on a batch basis.

[7] Finisar HFE6x92-761

23. Risk Analysis and Risk Mitigation

Editor: Phil Allport
Chaser: Ingrid-Maria Gregor
Number of pages to write: 20
Scope of chapter:

- *Technical risk analysis including financial and schedule impact of the risks*
- *Risk mitigation plans*
- *Guidelines from LHCC on the level of detail would be appreciated*

23.1 Introduction

23.2 Risk Analysis

23.2.1 Financial Impact

23.2.2 Schedule Impact

23.3 Risk Mitigation Plan

24. ITk Management

Editor: Marcel Stanitzki
Chaser: Steve McMahon
Number of pages to write: 10
some explanations on the scope of the chapter

- Division of responsibilities and reporting lines
- Organogram demonstrating organization, interactions with ATLAS and other oversight and managerial bodies
- Evolution of management in going from R&D project to production

25. Beyond Scenarios

Editor: Abe Seiden
Number of pages to write: 20
Scope of chapter:

- *Access scenarios*
- *Access scenarios at and beyond start up ? remote handling*
- *Radiation protection issues during tracker replacement and maintenance*
- *Estimates of activation levels*
- *ATLAS Radioprotection General Organization*
- *CERN general regulation for Radioprotection - Area classification*
- *ALARA strategy*

26. Costing

Editor: Marcel Stanitzki
Chaser: Tony Affolder
Number of pages to write: 10
Scope of chapter:

- *Breakdown of the component and other costs of items in the WBS*
- *Cost uncertainty for items and roadmap to improved understanding of costs (The core values of many of the cost drivers will not be updated before the time TDR.)*
- *Purchase profile including all steps in purchase and spending*

27. Glossary

27.1 Definition of objects

Below a list of objects and their definition to make sure we all mean the same throughout the TDR writing process.

- **Bare hybrid** – printed circuit board for hybrid without any active (and passive?) components.
- **Hybrid** – hybrid with x ABC130 and one HCC. x is depending on what kind of hybrid it is. It can be either a long strip hybrid (LS), a short strip hybrid (SS) or a hybrid for the end-cap (R0, R1,...)
- **Module** – object consisting of one sensor and a number of hybrids depending of what kind of module it is. Additionally a module contains a power-board for LV DCDC conversion, HV switching as well as monitoring (AMAC chip).
- **Stave** – double-sided object for half barrel with 14 modules on each side. 392 are in the detector
- **Petal** – double sided petal - equivalent of a stave for the end-cap disks. 9 modules on each side.
- **(Stave or Petal) Core** – mechanical structure of stave or petal incl. cooling pipes, honeycomb, facings, bustape, and locking points, but no modules.
- **Disk** – 32 petals are one disk.
- **Half-barrel** – All staves for one side of the barrel. There will be barrel A and barrel C depending on the side (does it make sense this way ???).

An overview of the number of staves, petals, modules, hybrids, FE-chips (ABC130) and the silicon area is given in table 27.36.

27.2 Glossary

And here a real glossary:

- **ABC** – ATLAS Binary Chip
- **HCC** – Hybrid Controller Chip

Barrel Layer:	**Radius [mm]**	**# of staves**	**# of modules**	**# of hybrids**	**# of of ABC130**	**# of channels**	**Area [m^2]**
L0	405	28	784	1568	15680	4.01M	7.49
L1	562	40	1120	2240	22400	5.73M	10.7
L2	762	56	1568	1568	15680	4.01M	14.98
L3	1000	72	2016	2016	20160	5.16M	19.26
Total half barrel		196	5488	7392	73920	18.92M	52.43
Total barrel		392	10976	14784	147840	37.85M	104.86
End-cap Disk:	**z-pos. [mm]**	**# of petals**	**# of modules**	**# of hybrids**	**# of of ABC130**	**# of channels**	**Area [m^2]**
D0	1512	32	576	832	6336	1.62M	5.03
D1	1702	32	576	832	6336	1.62M	5.03
D2	1952	32	576	832	6336	1.62M	5.03
D3	2252	32	576	832	6336	1.62M	5.03
D4	2602	32	576	832	6336	1.62M	5.03
D5	3000	32	576	832	6336	1.62M	5.03
Total one EC		192	3456	4992	43008	11.01M	30.2
Total ECs		384	6912	9984	86016	22.02M	60.4
Total		**776**	**17888**	**24768**	**233856**	**59.87M**	**165.25**

Table 27.36. Number of staves and petals for the ITK strip detector.

A. Appendix: ATLAS acronyms

ADC	Analogue-to-Digital Converter
ALFA	Absolute Luminosity for ATLAS
ASD	Amplifier/Shaper/Discriminator
ASDBLR	Amplifier/Shaper/Discriminator/BaseLine Restoration
ASIC	Application-Specific Integrated Circuit
ASM	Amplification, Sampling, (digitization) and Multiplexing
ATLAS	A Toroidal LHC ApparatuS
BC	Bunch Crossing
BCID	Bunch-Crossing IDentification
BCM	Beam Conditions Monitor
BC-mux	Bunch-Crossing MUltipleXing
BEE	Barrel End-cap Extra
BIL	Barrel Inner Large
BIR	Barrel Inner Rail
BIS	Barrel Inner Small
BM	Barrel Middle
BML	Barrel Middle Large
BMS	Barrel Middle Small
BO	Barrel Outer
BOC	Back Of Crate
BOL	Barrel Outer Large
BOS	Barrel Outer Small
BPM	BiPhase Mark
BT	Barrel Toroid
CANbus	Controller Area Network bus
CALbus	Calibration bus
CDD	CERN Drawing Directory
CERN	European Organization for Nuclear Research
CFS	Central File Server
CIC	Common Infrastructure Control
CIS	Charge Injection System
CMA	Coincidence Matrix chip
CM	Coincidence Matrix
CMM	Common Merger Module
CMOS	Complementary Metal-Oxide Semiconductor
COMbus	Common Timing and Trigger Bus
COOL	ATLAS-wide conditions database
CP	Cluster Processor
CPM	Cluster Processor Module
CRC	Cyclic Redundancy Check
CSC	Cathode Strip Chambers
CS	Central Solenoid
CSM	Chamber Service Module
CTP	Central Trigger Processor
DAC	Digital-to-Analogue Converter
DAQ	Data AcQuision system
DCS	Detector Control System
DFM	Data Flow Manager
DMILL	Durci Mixte sur Isolant Logico-Lineaire (a radiation-hard ASIC technology)
DORIC	Digital Opto-Receiver Integrated Circuit
DSP	Digital Signal Processors
DSS	Detector Safety System
EB	Extended Barrel
EC	End-Cap
ECT	End-Cap Toroid
EDMS	Engineering Data Management System
EEL	End-cap Extra Large
EES	End-cap Extra Small
EF	Event Filter

EI	End-cap Inner wheel
EIL	End-cap Inner Large
EIS	End-cap Inner Small
ELMB	Embedded Local Monitor Board
EMB	ElectroMagnetic Barrel calorimeter
EMD	Equipment Management Database
EMEC	ElectroMagnetic End-cap Calorimeter
EM	ElectroMagnetic
EM	End-cap Middle wheel
EML	End-cap Middle Large
EMS	End-cap Middle Small
ENC	Equivalent Noise Charge
EOL	End-cap Outer Large
EOS	End-cap Outer Small
EST	ElectroStatic Transformer
FADC	Flash ADC
FCal	Forward Calorimeter
FEB	Front-End Board
FECcont	Front-End Crate controller board
FEC	Front-End Crate
FE	Front-End
FIFO	First-In/First-Out
FI	Forward Inner wheel
fLVPS	finger Low Voltage Power Supply
FPGA	Field-Programmable Gate Array
FPIAA	Find Persons Inside ATLAS Area
GSEL	Gain-SELector chip
GCS	Global Control Stations
HAD	HADron calorimeter
HEC	Hadronic End-cap Calorimeter
HF	Steel structures below access shafts
HLT	High-Level Trigger
HO	Blue support structure on ends of ATLAS cavern
HS	Blue support structure on sides of ATLAS cavern
HV	High Voltage
HVPS	High Voltage Power Supply
IC	Integrated Circuit
ID	Inner Detector
IS	Information Server
ITC	Inter TileCal scintillators
IWV	Inner Warm Vessel
JEM	Jet/Energy Module
JEP	Jet/Energy-sum Processor
JTAG	Joint Task Action Group
L1A	Level-1 Accept
L1Calo	Level-1 Calorimeter trigger
L1	Level-1 trigger
L2	Level-2 trigger
L2PU	Level-2 Processing Unit
L2SV	Level-2 SuperVisor
LAr	Liquid Argon
LB	Long barrel
LCS	Local Control Stations
LFS	Local File Server
LHC	Large Hadron Collider
LUCID	LUminosity measurement using Cerenkov Integrating Detector
LVDS	Low-Voltage Differential Signalling
LV	Low Voltage
LVPS	Low Voltage Power Supply
MCC	Module Control Chip
MDT	Monitored Drift Tubes

MIP	Minimum Ionising Particle
MRS	Message Reporting Service
MTF	Manufacturing and Test Folder database
MUCTPI	MUon-to-Central-Trigger-Processor-Interface
NEF	Neutron Equivalent Fluence
NEG	Non-Evaporable Getter
NMR	Nuclear Magnetic Resonance
NRZ	Non Return to Zero
ODH	Oxygen Deficiency Hazard
OFC	Optimal Filtering Coefficients
OF	Optimal Filtering
OHS	Online Histogramming Service
OMB	Optical Multiplexer Board
OTx	Optical Transmitter
PEEK	PolyEther-Ether-Ketone
PITbus	Pattern In Time Bus
PL	Pad Logic
PMT	PhotoMultiplier Tube
PP	Patch Panel
PPM	Pre-Processor Module
PPr	Pre-Processor
PS	Presampler
PST	Pixel Support Tube
PU	Processor Unit
PVSS	Prozessvisualisierungs und Steuerungs System
QSP	Quarter Service Panel
QUAD	QUADrupole
ROBIN	ReadOut Buffer Module
ROB	ReadOut Buffer
ROC	ReadOut Crate
ROD	ReadOut Driver
RoIB	Region-of-Interest Builder
RoI	Region-of -Interest
ROL	ReadOut Link
ROS	ReadOut System
RPC	Resistive Plate Chambers
SCA	Storage Capacitor Array
SCA	Switched Capacitor Array
SCS	Sub-detector Control Stations
SCT	SemiConductor Tracker
SEU	Single Event Upset
SFI	Event building node
SFO	Event filter output node
SIC	System Interlock Card
SLB	SLave Board
SL	Sector Logic
SLC	Scientific Linux CERN
SPAC	Serial Protocol for Atlas Calorimeters
SSW	Star SWitch
TAN	Target Absorber Neutral
TAS	Target Absorber Secondaries
TBB	Tower Builder Board
TBM	Trigger and Busy Module
TC	Technical Coordination
TDAQ	Trigger and Data AcQuision
TDB	Tower Driver Board
TDC	Time-to-Digital Converter
TDR	Technical Design Report
TGC	Thin Gap Chambers
TileCal	Tile Calorimeter
TLA	Three Letter Acronym

TMB	Technical Management Board
ToT	Time over Threshold
TPG	Thermal Pyrolitic Graphite
TR	Transition Radiation
TRT	Transition Radiation Tracker
TTCR	Trigger, Timing, and Control Receiver
TTCrx	Trigger, Timing, and Control Receiver chip
TTC	Timing, Trigger, and Control
TTCvi	Timing, Trigger, and Control VME interface module
TVS	Transient Voltage Suppressor
USA	Underground Service Area
VA	Vacuum Argon end-cap
VCEL	Vertical Cavity Surface-Emitting Laser Diode
VDC	VCSEL Driver Chip
VI	Vacuum Inner detector
VJ	Vacuum forward shielding
VME	Versa Module Eurocard
VMEbus	Versa Module Euro bus
VT	Vacuum Toroid end-cap
WLS	WaveLength Shifting
ZDC	Zero Degree Calorimeter

References

[1] R. Gupta, *Probing quartic neutral gauge boson couplings using diffractive photon fusion at the LHC*, http://arxiv.org/pdf/1111.3354.

[2] Y. Unno et al., Development of n+-in-p large-area silicon microstrip sensors for very high radiation environmentsÃć {ATLAS12} design and initial results, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment (2014).

[3] Aad, G. and others, The ATLAS Experiment at the CERN Large Hadron Collider, JINST **3** (2008) S08003.

[4] Clark, A and Elsing, M and Wells, P, Performance Specifications of the Tracker Phase II Upgrade, Internal Report ATL-UPGRADE-PUB-2012-003, CERN, Geneva, Sep 2012.

[5] Clark, A and Elsing, M and Hessey, N and MÅättig, P and Styles, N and Wells, P and Burdin, S and Cornelissen, T and Todorov, T and Vankov, P and Watson, I and Wenig, S, Final Report: ATLAS Phase-2 Tracker Upgrade Layout Task Force, Internal Report ATL-UPGRADE-PUB-2012-004, CERN, Geneva, Oct 2012.

[6] Shochet, M and Tompkins, L and Cavaliere, V and Giannetti, P and Annovi, A and Volpi, G, Fast TracKer (FTK) Technical Design Report, Internal Report CERN-LHCC-2013-007. ATLAS-TDR-021, CERN, Geneva, Jun 2013, ATLAS Fast Tracker Technical Design Report.

[7] The ATLAS Collaboration, Letter of Intent for the Phase-II Upgrade for the ATLAS Experiment, CERN-LHCC-2012-022 (2012).

[8] Ferrari, Alfredo and Sala, Paola R. and Fasso, Alberto and Ranft, Johannes, FLUKA: A multi-particle transport code (Program version 2005), (2005).

[9] Sjostrand, Torbjorn and Mrenna, Stephen and Skands, Peter Z., A Brief Introduction to PYTHIA 8.1, Comput.Phys.Commun. **178** (2008) 852–867.

[10] Miyagawa, P S and Dawson, I, Radiation background studies for the Phase II inner tracker upgrade, Internal Report ATL-UPGRADE-PUB-2013-012, CERN, Geneva, Feb 2013.

[11] Amaral, Luis and others, The versatile link, a common project for super-LHC, JINST **4** (2009) P12003.

[12] Y. Unno et al.,, Development of n-in-p silicon planar pixel sensors and flip-chip modules for very high radiation environments, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment **650** (2011) 129 – 135.

[13] Aad, G. and others, The ATLAS Experiment at the CERN Large Hadron Collider, JINST **3** (2008) S08003.

[14] Troska, J. and others, Single-Event Upset Testing of the Versatile Transceiver, JINST **6** (2011) C11026.

[15] Zhang, T. and others, GBLD10+: a compact low-power 10 Gb/s VCSEL driver, JINST **11** (2016) C01015.

[16] Troska, J. and others, Radiation damage studies of lasers and photodiodes for use in multi-Gb/s optical data links, Proceedings NSREC 2011, Las Vagas, July 25-29 2011., 2011.

[17] H. Johnson and M. Graham, High-Speed Signal Propagation Advanced Black Magic, (Prentic Hall, New Jersey, 2003).

[18] Hall D. and others, The radiation induced attenuation of optical fibres below âĹŠ20 °C exposed to lifetime HL-LHC doses at a dose rate of 700 Gy(Si)/hr, JINST **7** (2012) P01047.

[19] Huffman, B. T. and others, Further studies of the effect of radiation on the mechanical strength of optical fibres, JINST **8** (2013) P12002.

[20] Achten, F. and others, A Study of the effect of a 500 kGy(Si) radiation doses on the bandwidth of a radiation hard multi-mode fibre, JINST **7** (2012) P10021.

[21] Ryder, N. and others, The radiation tolerance of MTP and LC optical fibre connectors to 500 kGy(Si) of gamma radiation, JINST **7** (2012) P04014.