Zynq Development Report

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- Development platform
  - Hardware
  - Tools
- Hardware Design
  - Zynq ARM Core
  - Infrastructure IP’s
- Software Development
  - BareMetal Software
  - Linux OS
- Future Plans
  - Zynq Development Portal
  - PTZ Forum

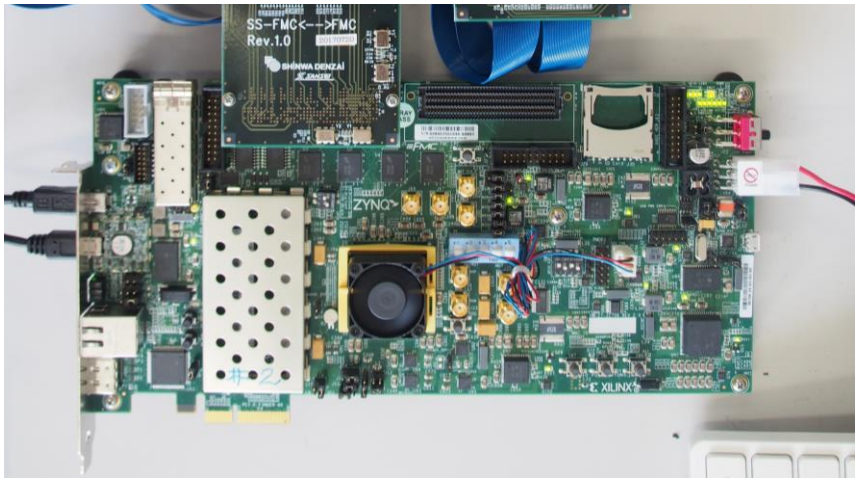
Development Platform

- Hardware
  - Two ZC706 Evaluation Boards
  - HPC-FMC <-> HPC-FMC crossing cable
- Tools
  - Vivado IDE 2018.2
    - On Windows 7
    - On CentOS 7
  - Petalinux 2018.2
    - On CentOS 7

Development Platform - Hardware

- ZC706 Evaluation Board

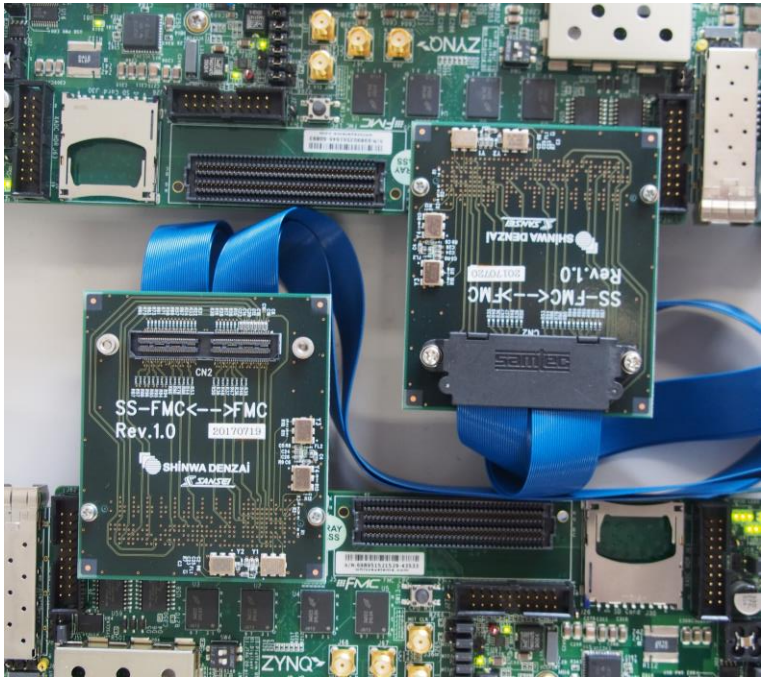
- Zynq7000 XC7Z045-2FFG900C
- 1GB DDR3 SODIMM for PL
- 1GB DDR3 Memory for PS
- Two 128Mb QSPI Flash
- SD Card Slot
- USB JTAG
- GTX on HPC and LPC FMC, SFP+, Ethernet and PCI Express
- USB UART
- …



Development Platform - Hardware

- FMC HPC – QxH A-B Board

  - Full HPC FMC Complient
  - CLK0 (H4/5) 66.66MHz
  - CLK1 (G2/3) 50.00MHz
  - GBTCLK0 (D4/5) 156.25MHz
  - GBTCLK1 (B21/22) 125.00MHz
  - QxH Connectors with cross connection



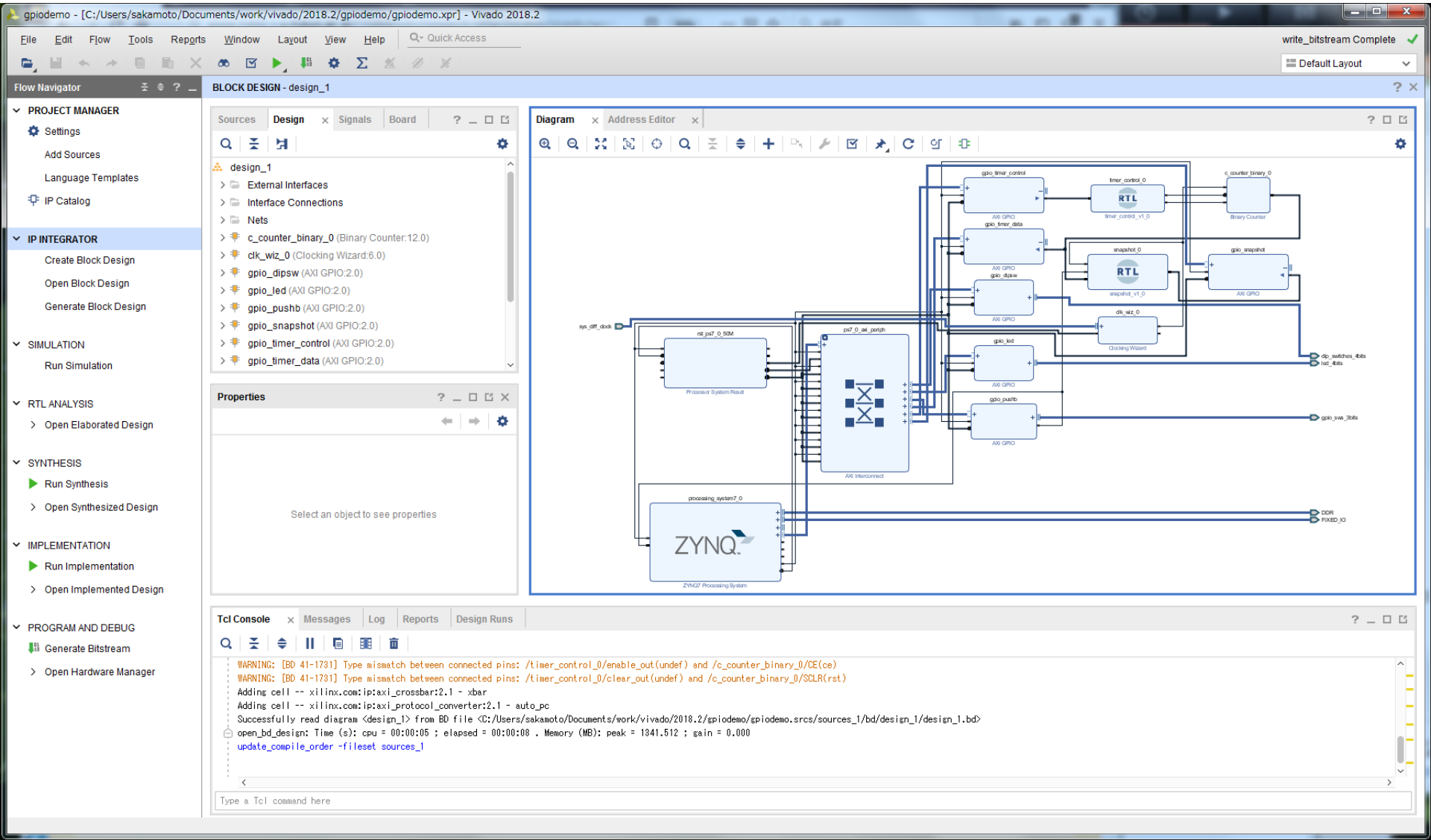
High Pin Count (HPC) FPGA Mezzanine Card (FMC)

Implemented on ZC706

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

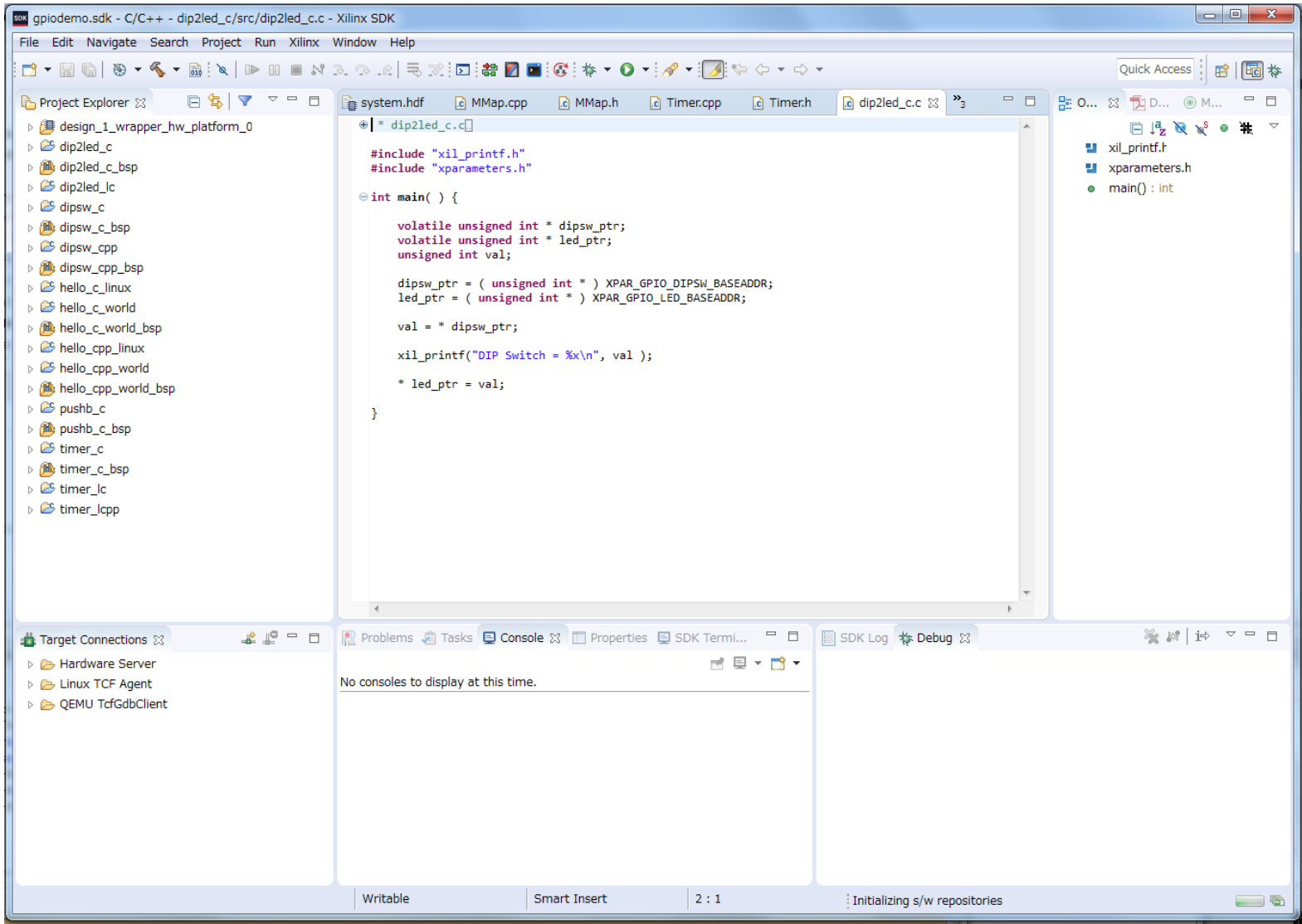
Development Platform - Tools

- Vivado 2018.2
  - Integrated Design Environment (IDE)



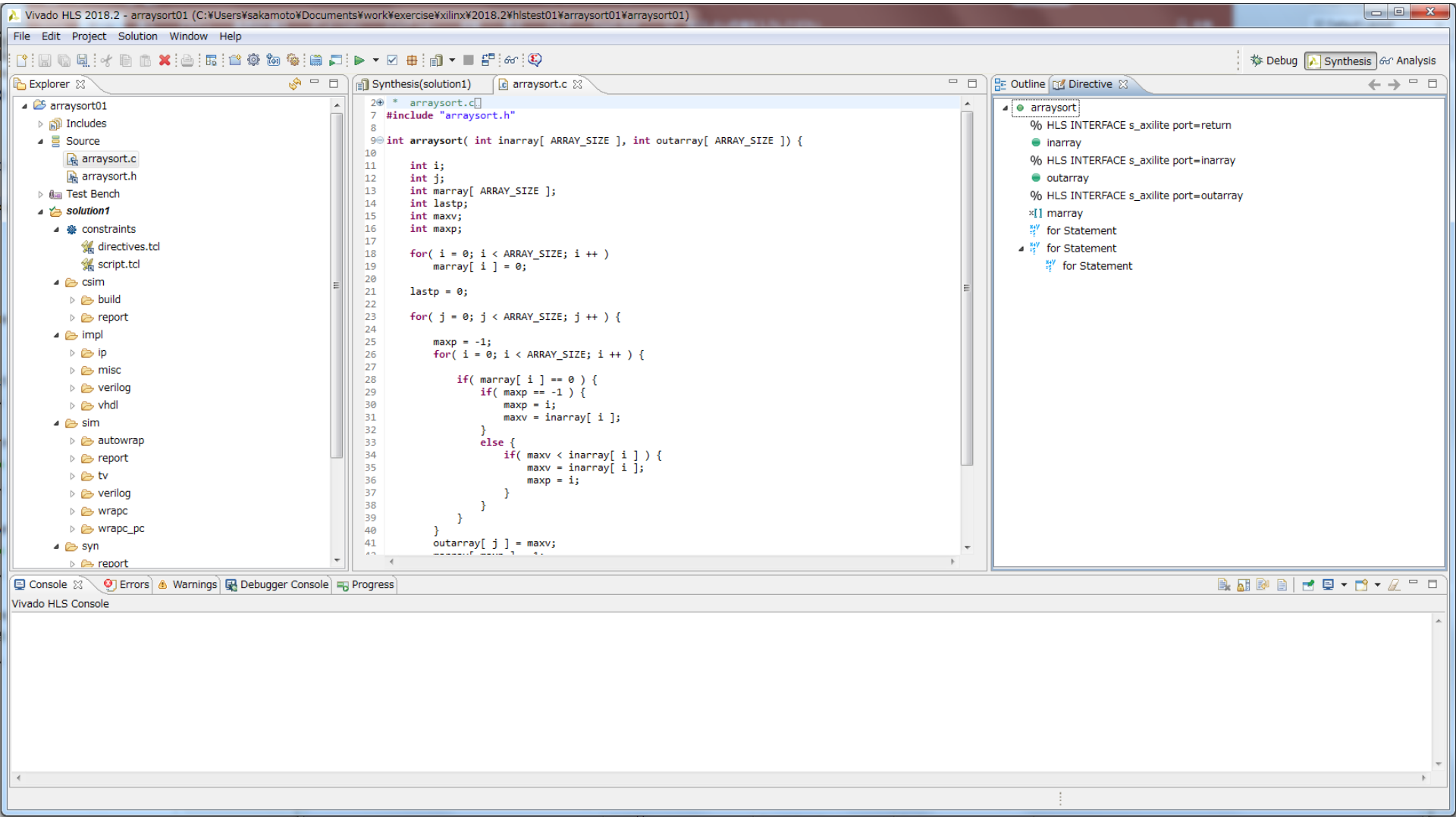
Development Platform - Tools

- Vivado SDK (Software Development Kit)



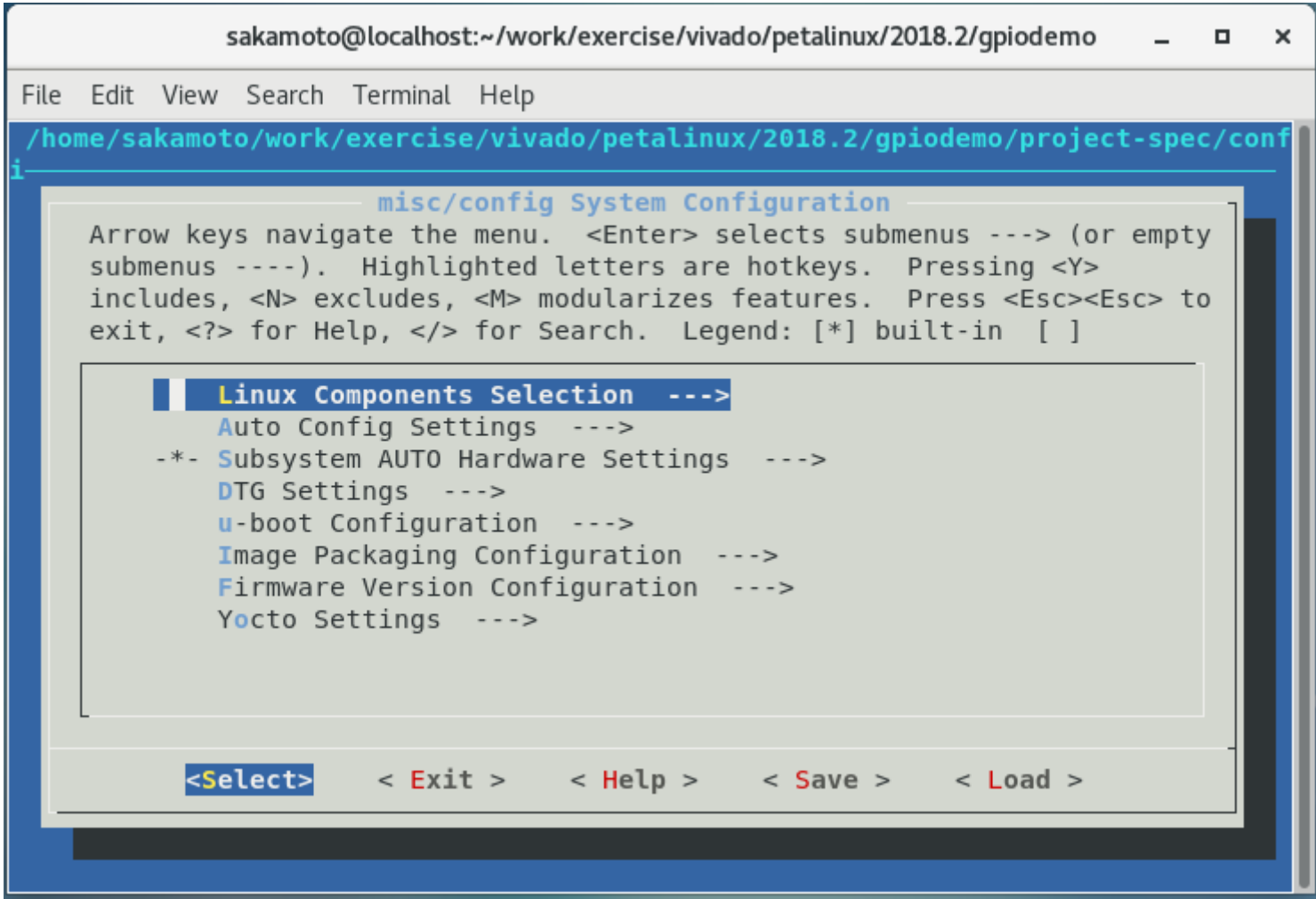
Development Platform - Tools

- Vivado HLS (High Level Synthesis)



Development Platform - Tools

- Petalinux Toolkit

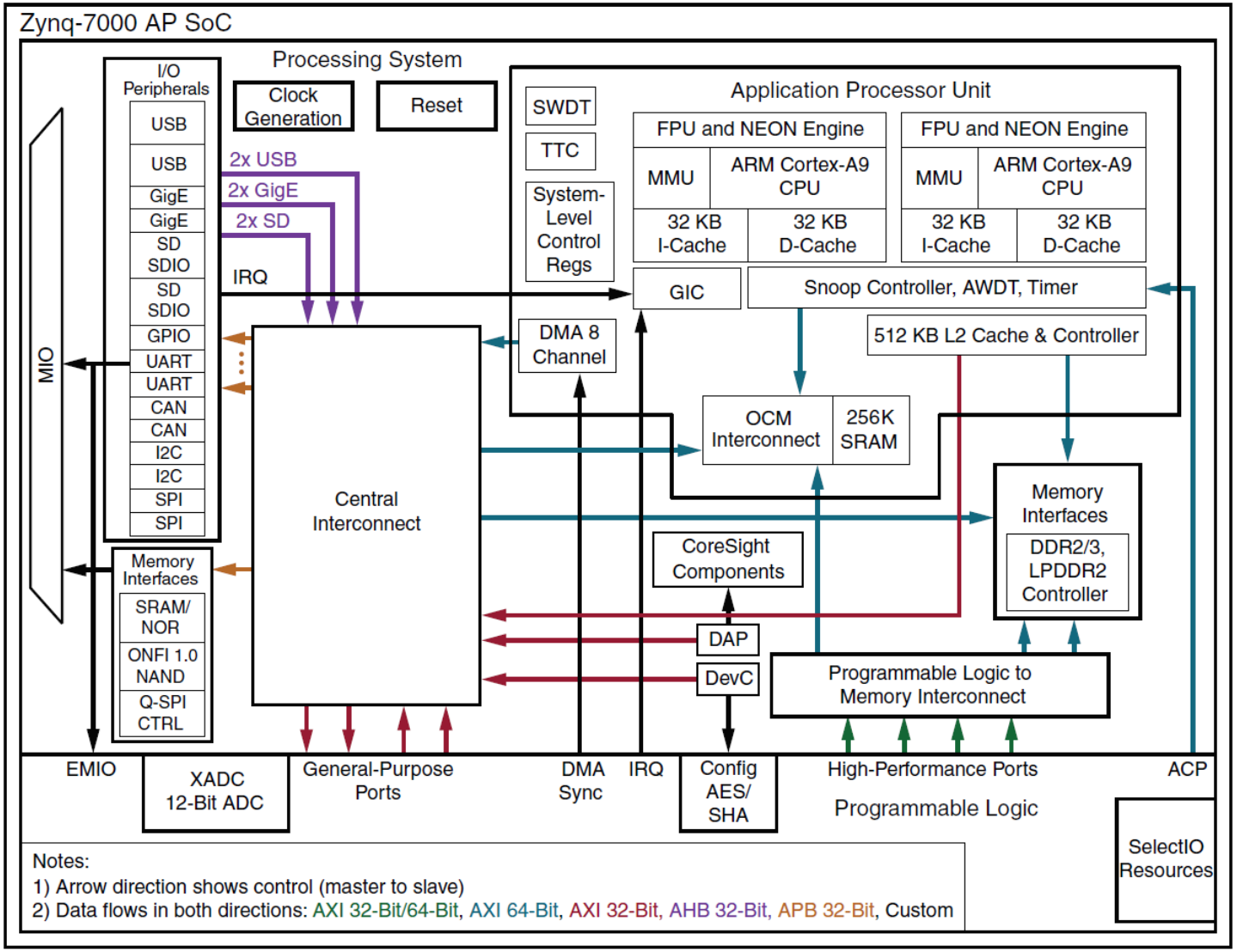


Hardware Design

- Zynq ARM Core
  - ZC706 Hardware Configuration
  - AXI Bus Interface
  - Memory Access
- Infrastructure IP’s
  - Memory Interface Generator
  - General Purpose IO (GPIO)
  - Central Direct Memory Access (CDMA)
  - Direct Memory Access (DMA)
  - AXI Chip2Chip Bridge
  - Aurora 8B/10B GTX Link Layer
- Debugging and Verification
  - Integrated Logic Analyzer
  - Integrated Bit Error Rate Tester

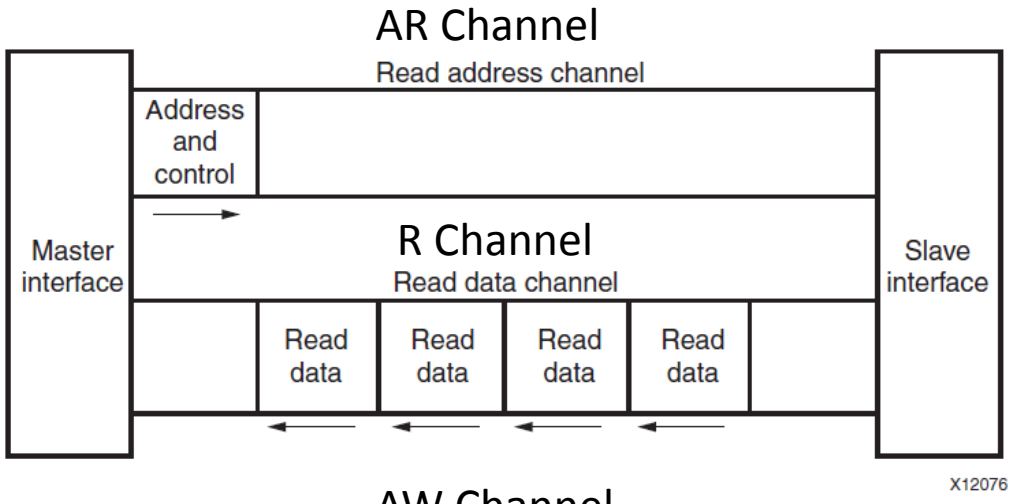
Zynq ARM Core

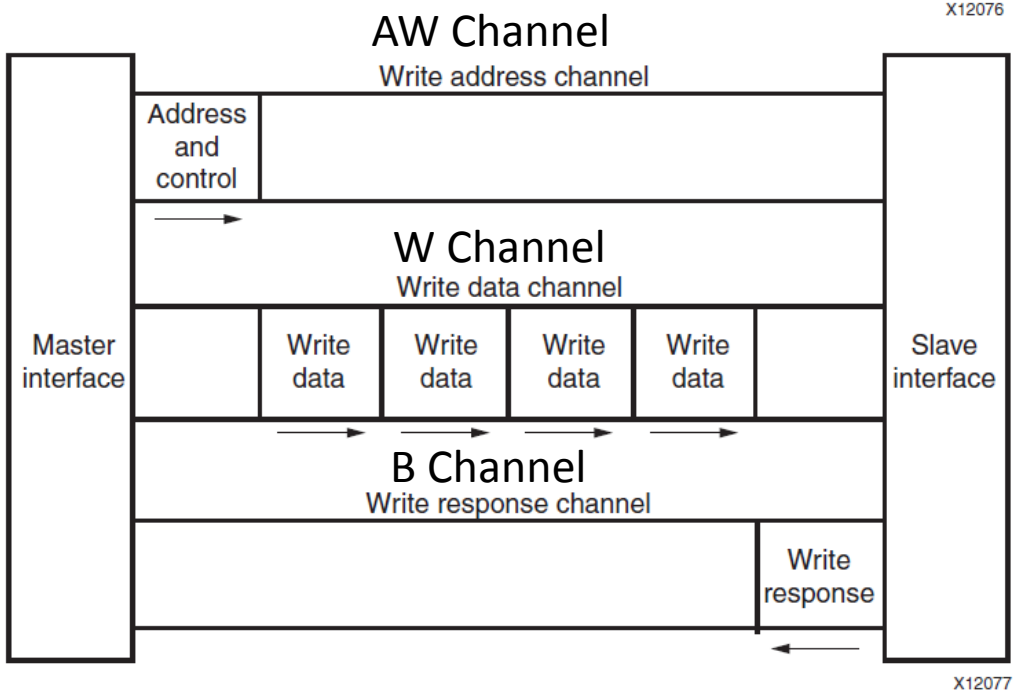
- Zynq 7000 XC7Z045



AXI4 Bus Interface

- Separate Read/Write Channels
  - AR and R channels for read ops.
  - AW, W and B channels for write.
- Synchronous to ACLK
- AXI4 capable of burst transfer up to 256
- AXI4-Lite only single transfer
- AXI4-Stream unlimited burst stream, having no addressing
  - T channel unidirectional transfer
  - Similar to W Channel





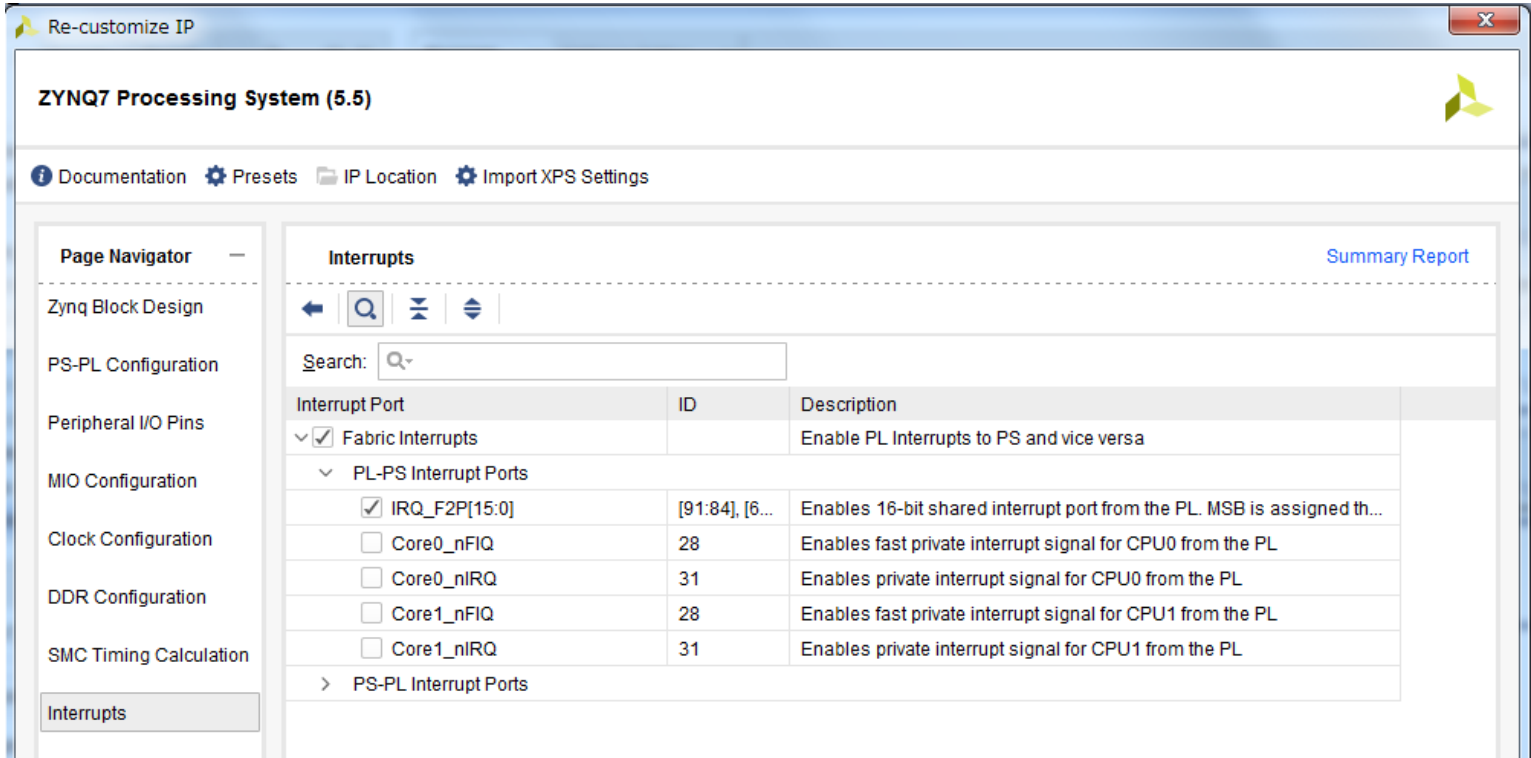
Memory Access

- PS DDR Memory
- PL DDR Memory
- Block RAM

Address Range	CPUs and ACP	AXI_HP	Other Bus Masters[1]	Notes
0000_0000 to 0003_FFFF[2]	OCM	OCM	OCM	Address not filtered by SCU and OCM is mapped low
	DDR	OCM	OCM	Address filtered by SCU and OCM is mapped low
	DDR			Address filtered by SCU and OCM is not mapped low
				Address not filtered by SCU and OCM is not mapped low
0004_0000 to 0007_FFFF	DDR			Address filtered by SCU
				Address not filtered by SCU
0008_0000 to 000F_FFFF	DDR	DDR	DDR	Address filtered by SCU
		DDR	DDR	Address not filtered by SCU[3]
0010_0000 to 3FFF_FFFF	DDR	DDR	DDR	Accessible to all interconnect masters
4000_0000 to 7FFF_FFFF	PL		PL	General Purpose Port #0 to the PL, M_AXI_GP0
8000_0000 to BFFF_FFFF	PL		PL	General Purpose Port #1 to the PL, M_AXI_GP1
E000_0000 to E02F_FFFF	IOP		IOP	I/O Peripheral registers, see Table 4-6
E100_0000 to E5FF_FFFF	SMC		SMC	SMC Memories, see Table 4-5
F800_0000 to F800_0BFF	SLCR		SLCR	SLCR registers, see Table 4-3
F800_1000 to F880_FFFF	PS		PS	PS System registers, see Table 4-7
F890_0000 to F8F0_2FFF	CPU			CPU Private registers, see Table 4-4
FC00_0000 to FDFF_FFFF[4]	Quad-SPI		Quad-SPI	Quad-SPI linear address for linear mode
FFFC_0000 to FFFF_FFFF[2]	OCM	OCM	OCM	OCM is mapped high
				OCM is not mapped high

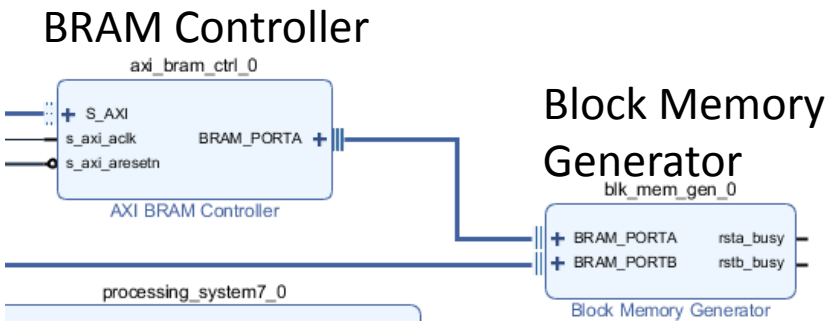
Interrupt Handling

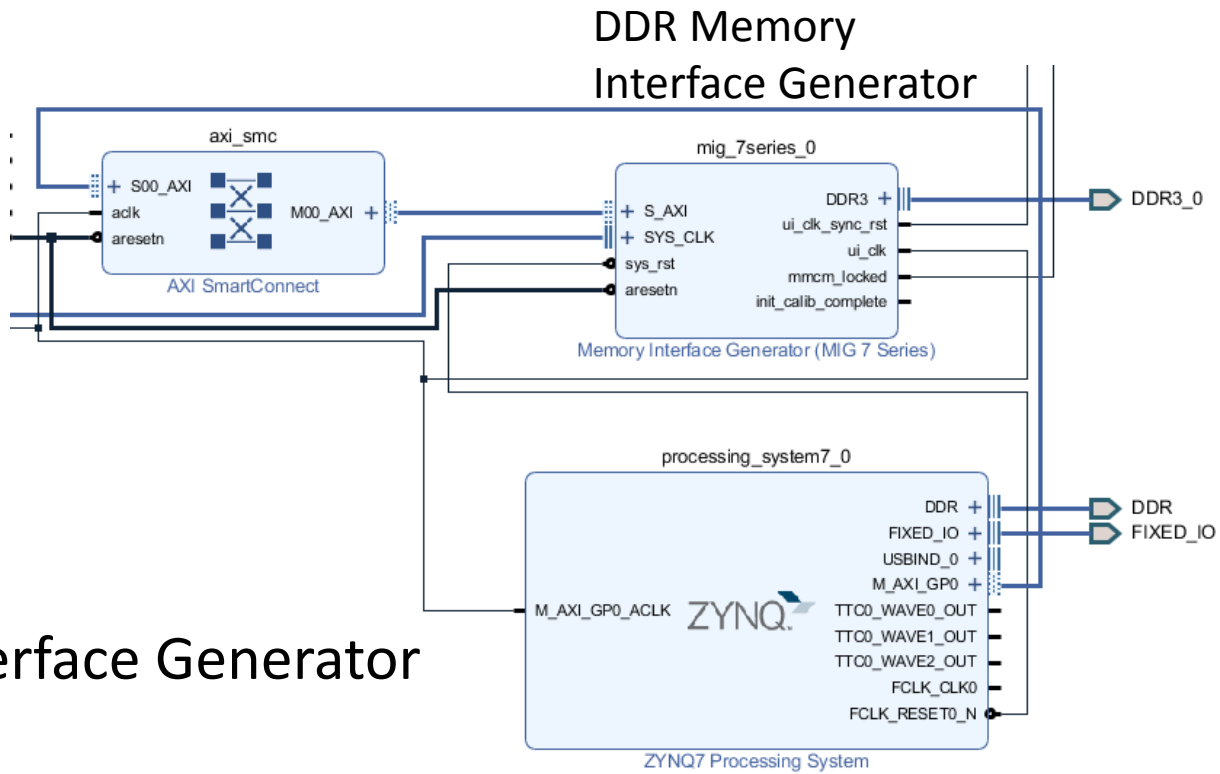
- PL to PS Interrupt



Memory Interface

- Block Memory Generator
- AXI BRAM Controller

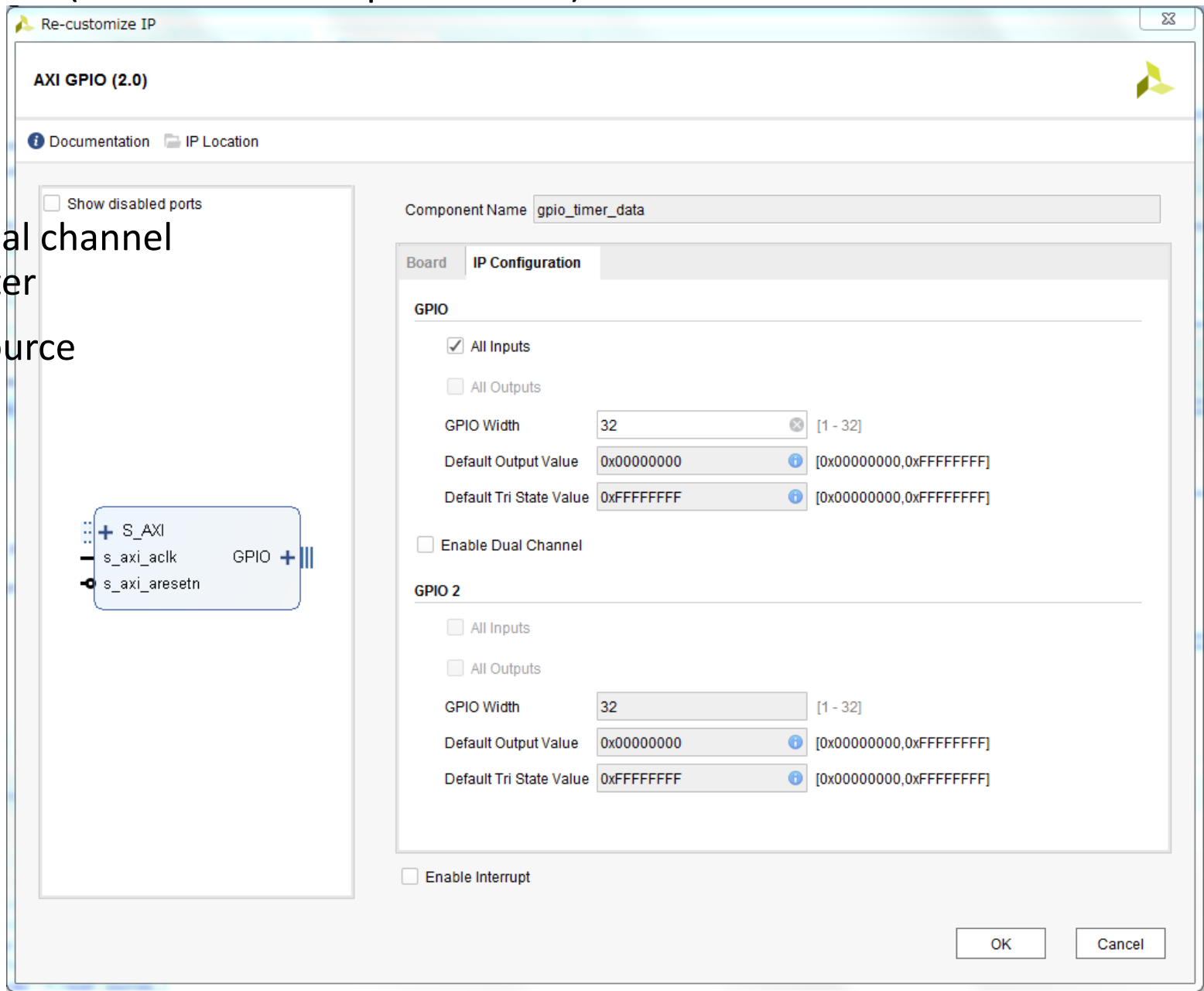




- DDR3 Memory Interface Generator

AXI GPIO (General Purpose I/O)

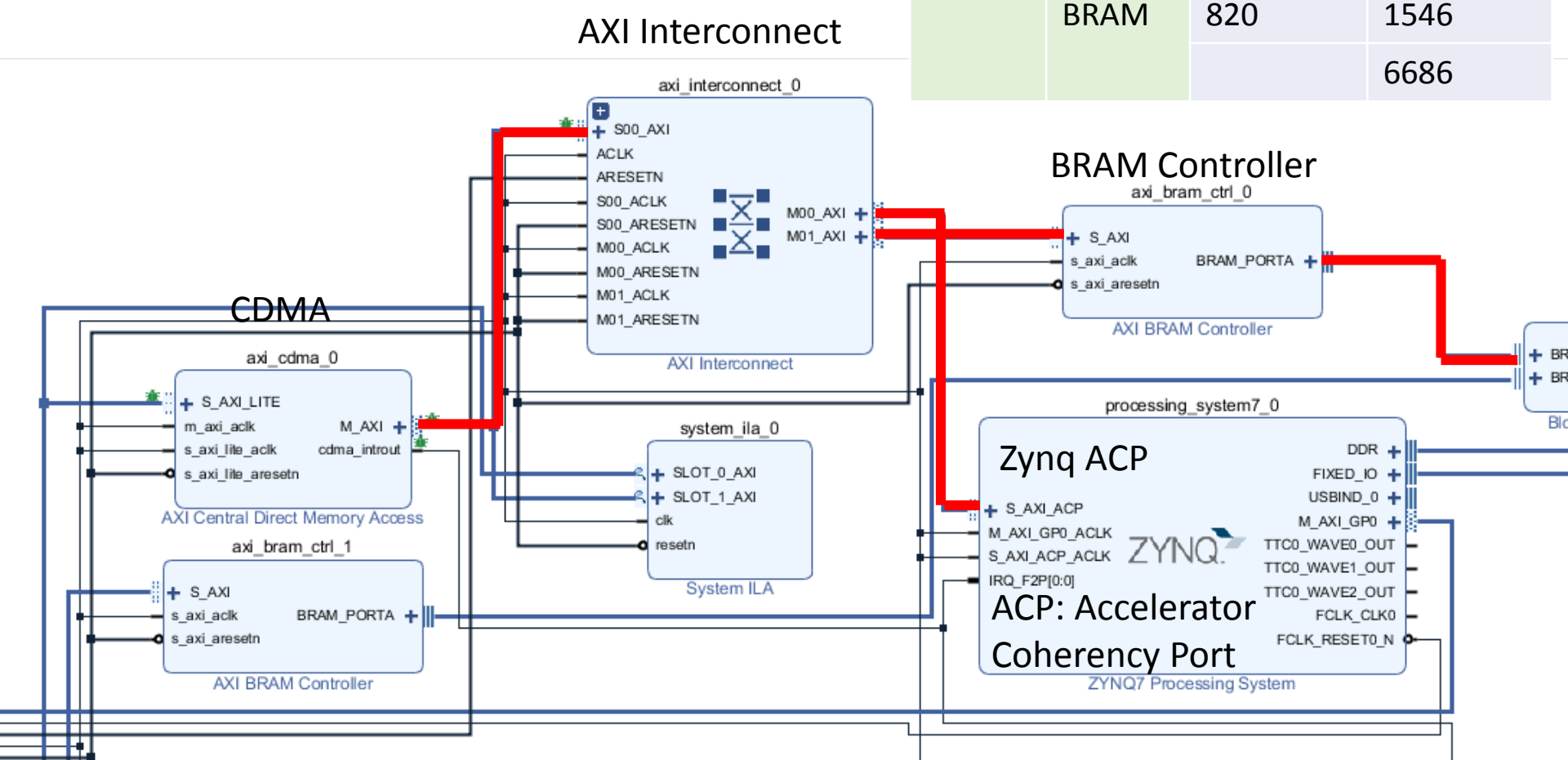
- Single or dual channel
  32 bit register
- Interrupt source



AXI CDMA (Central Direct Memory Access)

- AXI to AXI Direct Memory Access Engine
- AXI-Lite slave control port
- Interrupt source

DMA transfer		Destination	
Programmed xfer		DDR	BRAM
Source	DDR	749	1074
		270	
	BRAM	820	1546
			6686



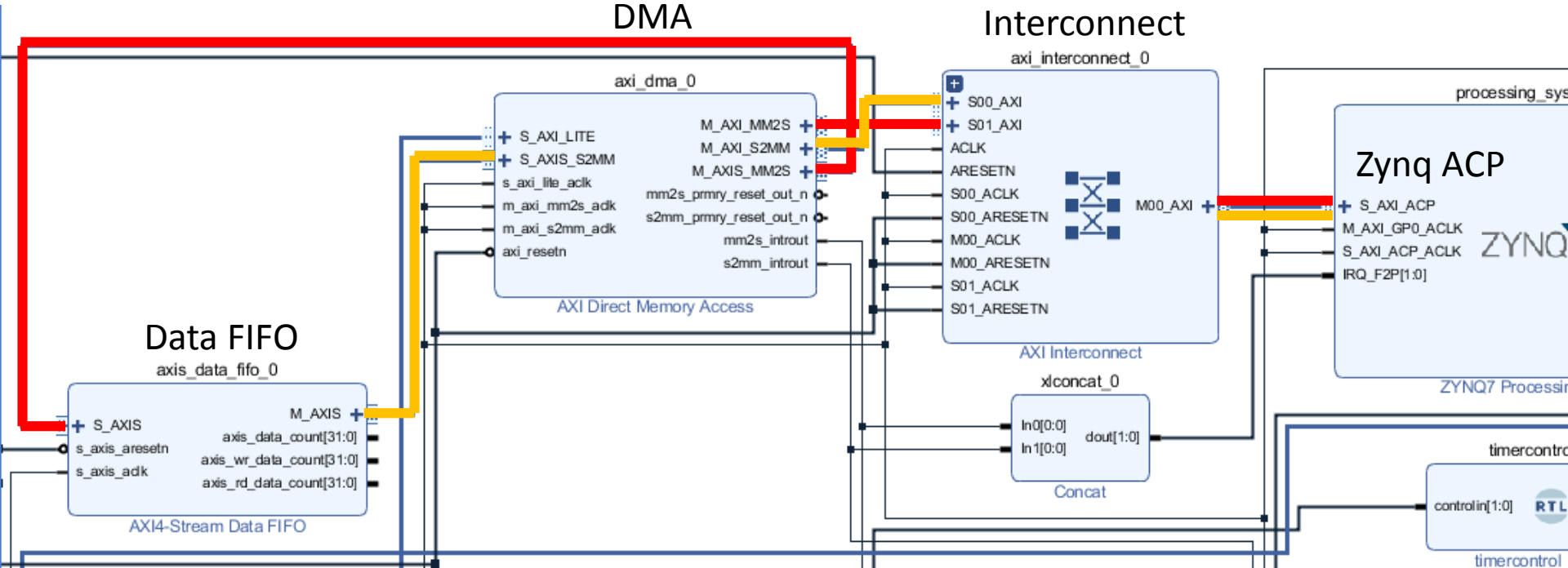
AXI DMA (Direct Memory Access)

- AXI to AXI-Stream / AXI-Stream to AXI Direct Memory Transfer Engine
- AXI-Lite slave control port
- Interrupt source

1kB Transfer	Polling	Interrupt
Send to FIFO	434	520
Received from FIFO	461	512

MM2S Path

S2MM Path

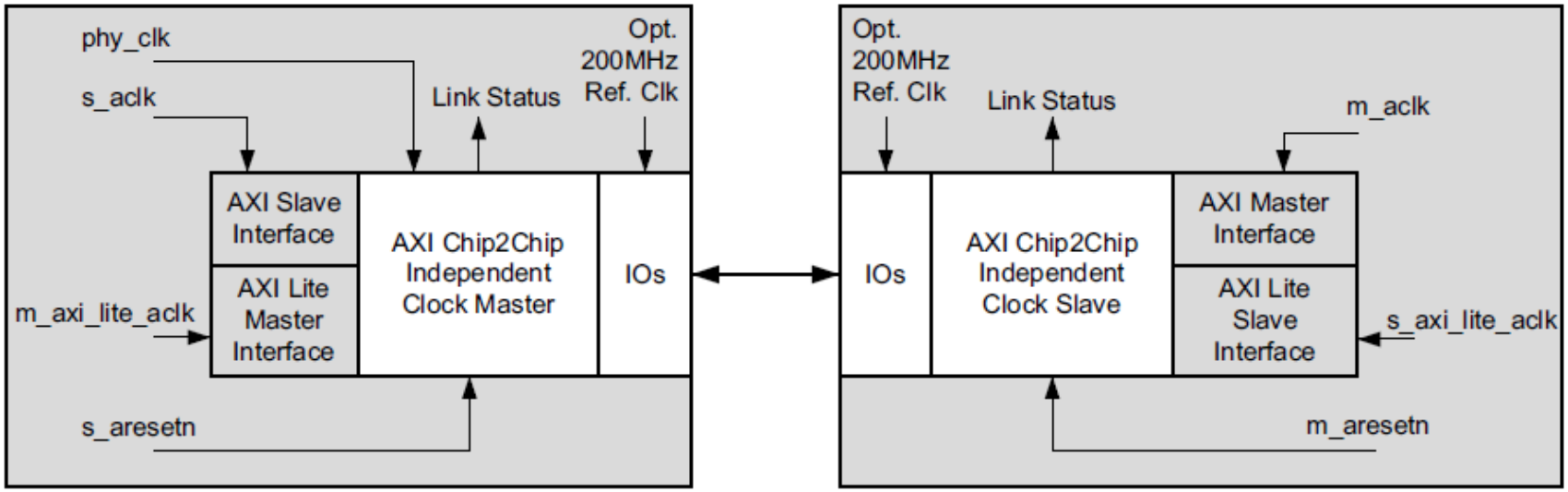


AXI Chip2Chip Bridge

Preliminary

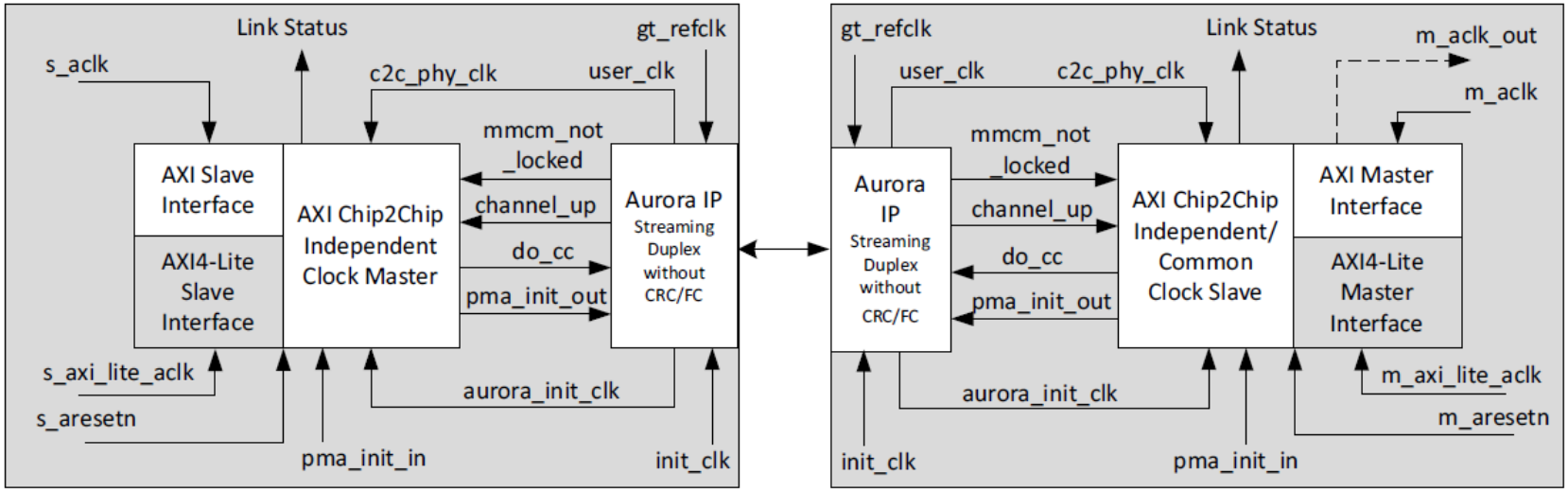
Select IO (Local 48)

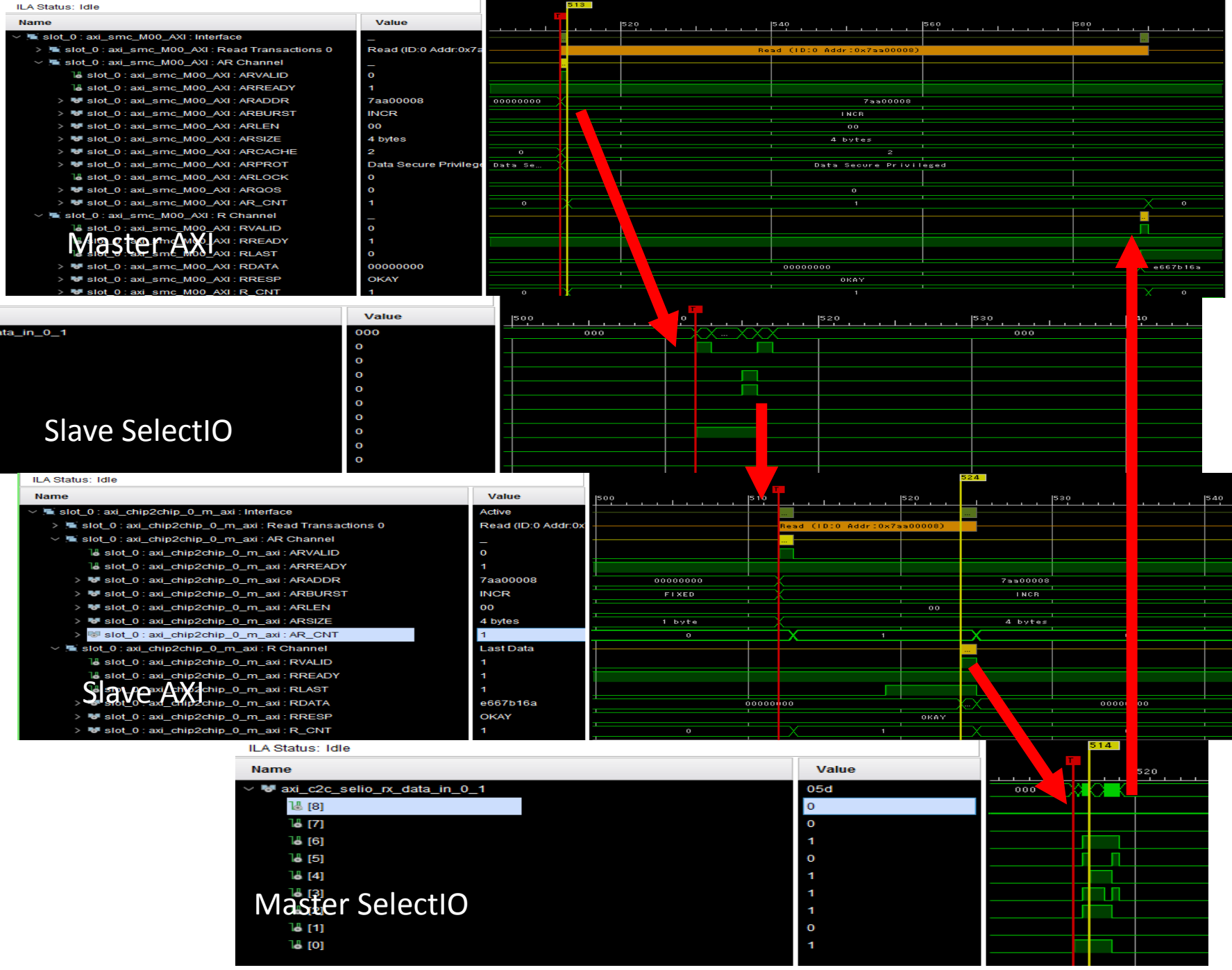
Write 108, Read 113



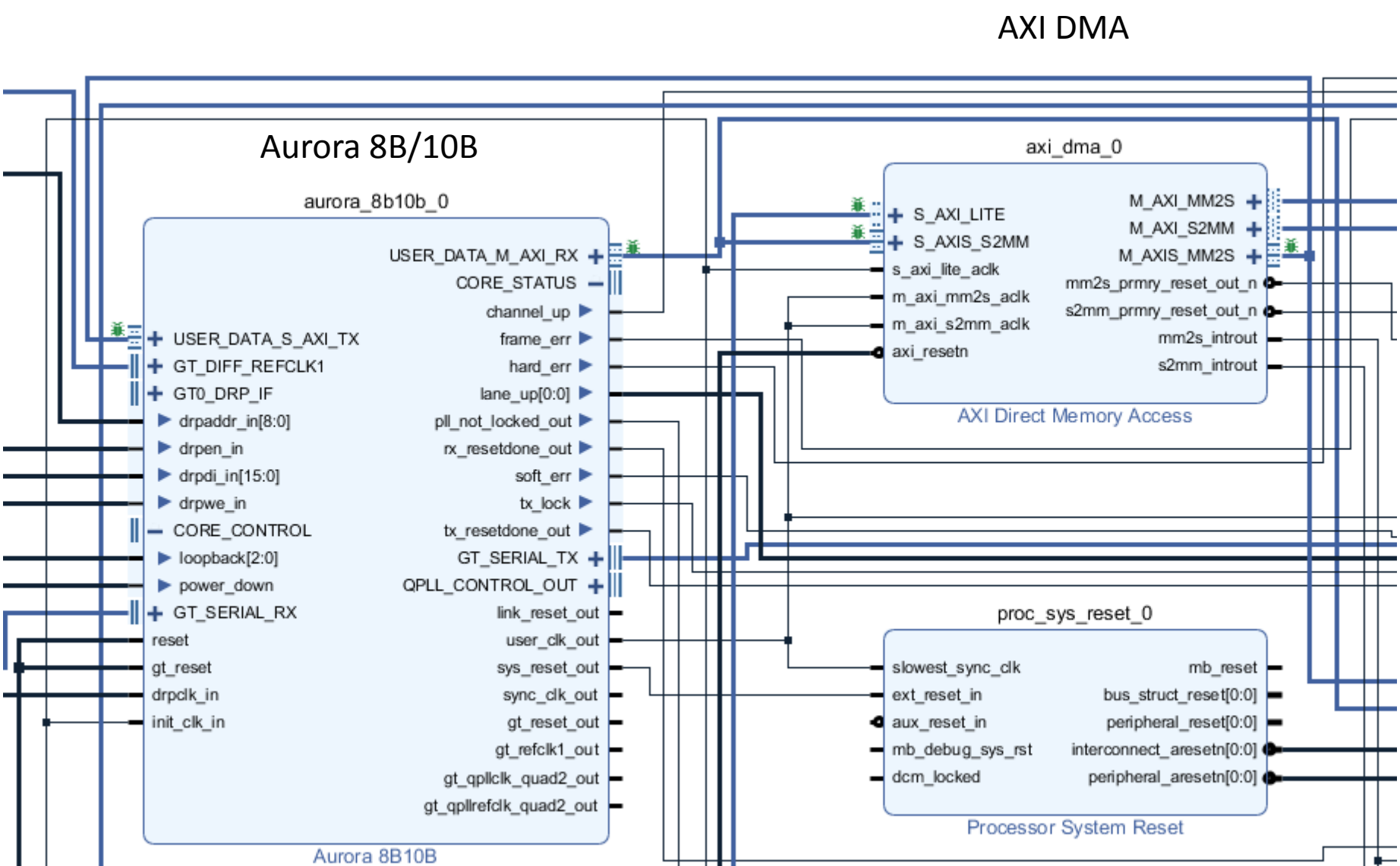
Aurora 8B/10B

Write 190, Read 192



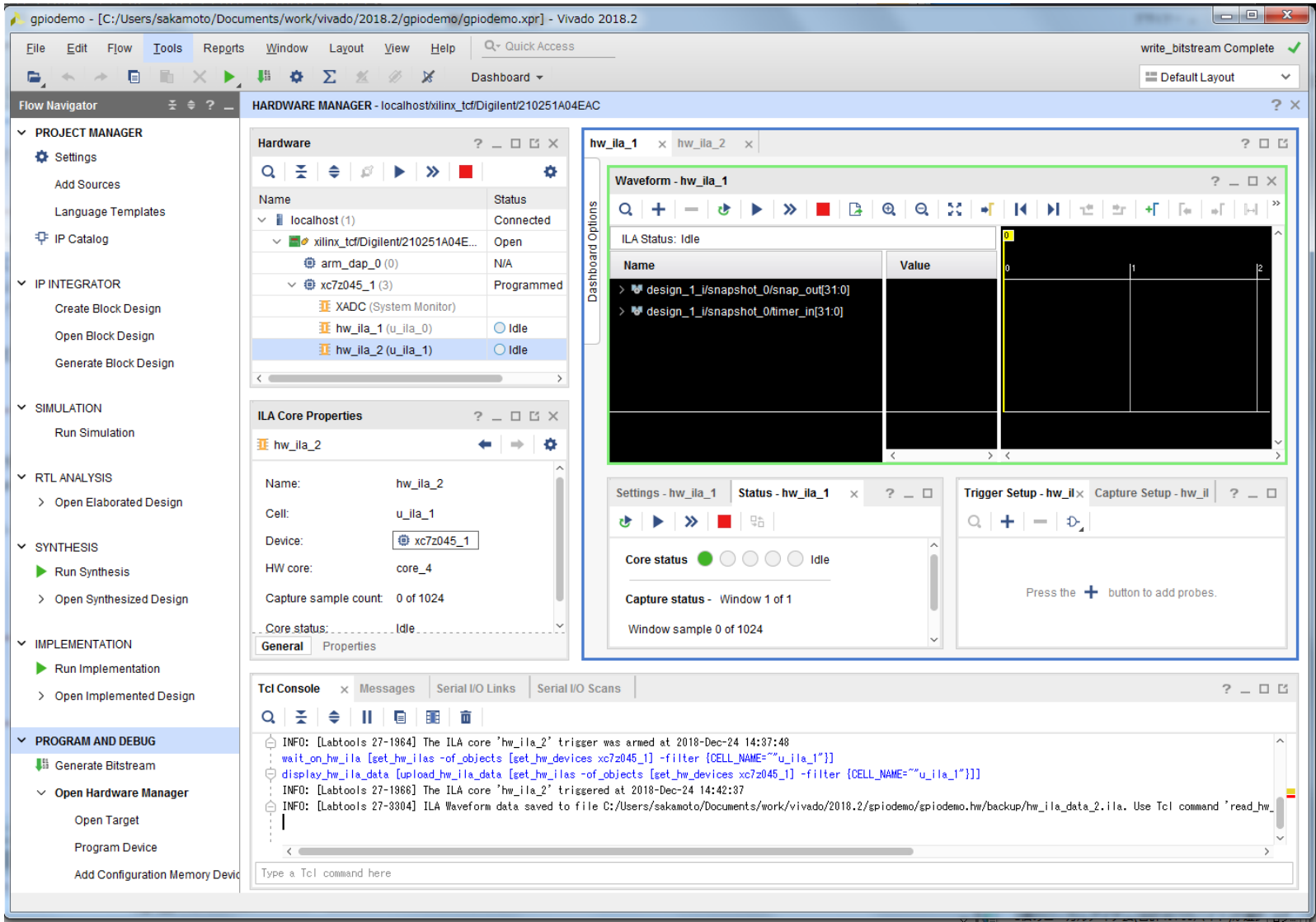

ILA Status: Idle
Name
Value
slot_0 : axi_smc_M00_AXI : Interface
slot_0 : axi_smc_M00_AXI : Read Transactions 0
slot_0 : axi_smc_M00_AXI : AR Channel
slot_0 : axi_smc_M00_AXI : ARVALID
slot_0 : axi_smc_M00_AXI : ARREADY
slot_0 : axi_smc_M00_AXI : ARADDR
slot_0 : axi_smc_M00_AXI : ARBURST
slot_0 : axi_smc_M00_AXI : ARLEN
slot_0 : axi_smc_M00_AXI : ARSIZE
slot_0 : axi_smc_M00_AXI : ARCACHE
slot_0 : axi_smc_M00_AXI : ARPROT
slot_0 : axi_smc_M00_AXI : ARLOCK
slot_0 : axi_smc_M00_AXI : AR_CNT
slot_0 : axi_smc_M00_AXI : R Channel
slot_0 : axi_smc_M00_AXI : RVALID
slot_0 : axi_smc_M00_AXI : RREADY
slot_0 : axi_smc_M00_AXI : RLAST
slot_0 : axi_smc_M00_AXI : RDATA
slot_0 : axi_smc_M00_AXI : RRESP
slot_0 : axi_smc_M00_AXI : R_CNT
Read (ID:0 Addr:0x7aa00008)
7aa00008
INCR
4 bytes
Data Secure Privileged
00000000
OKAY
Master AXI
o_rx_data_in_0_1
Slave SelectIO
slot_0 : axi_chip2chip_0_m_axi : Interface
slot_0 : axi_chip2chip_0_m_axi : Read Transactions 0
slot_0 : axi_chip2chip_0_m_axi : AR Channel
slot_0 : axi_chip2chip_0_m_axi : ARVALID
slot_0 : axi_chip2chip_0_m_axi : ARREADY
slot_0 : axi_chip2chip_0_m_axi : ARADDR
slot_0 : axi_chip2chip_0_m_axi : ARBURST
slot_0 : axi_chip2chip_0_m_axi : ARLEN
slot_0 : axi_chip2chip_0_m_axi : ARSIZE
slot_0 : axi_chip2chip_0_m_axi : AR_CNT
slot_0 : axi_chip2chip_0_m_axi : R Channel
slot_0 : axi_chip2chip_0_m_axi : RVALID
slot_0 : axi_chip2chip_0_m_axi : RREADY
slot_0 : axi_chip2chip_0_m_axi : RLAST
slot_0 : axi_chip2chip_0_m_axi : RDATA
slot_0 : axi_chip2chip_0_m_axi : RRESP
slot_0 : axi_chip2chip_0_m_axi : R_CNT
Active
Read (ID:0 Addr:0x7aa00008)
7aa00008
INCR
4 bytes
Last Data
e667b16a
OKAY
Slave AXI
axi_c2c_selio_rx_data_in_0_1
[8]
[7]
[6]
[5]
[4]
[3]
[1]
[0]
05d
Master SelectIO

Aurora 8B/10B



Debugging and Verification - ILA

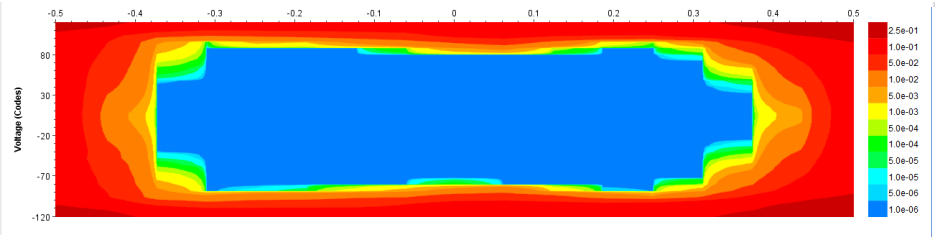
- Integrated Logic Analyzer



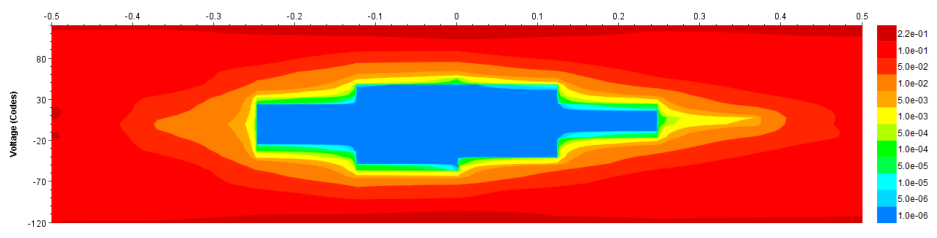
Debugging and Verification - IBERT

- Integrated Bit Error Rate Tester
- Loop back test of GTX lanes

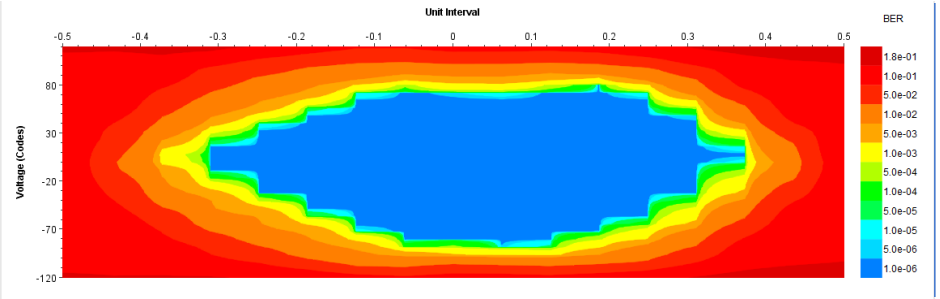
Coaxial cable 1m, 3.125GHz



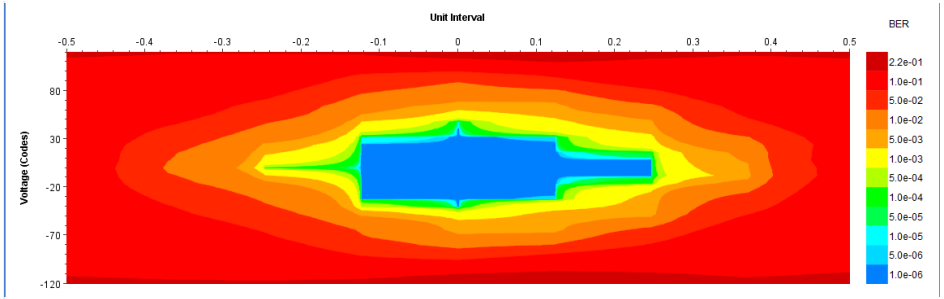
Coaxial cable 5m, 8.000GHz



Flat cable 50cm, 3.125GHz



Flat cable 50cm, 6.250GHz



Software Development

- BareMetal Software
  - Support Libraries
  - Debugging
- Linux Software
  - Linux Kernel
  - Device Drivers
  - Support Libraries
  - Sample Programs

BareMetal Software

- Vender Libraries

xgpio.h | system.hdf | MMap.cpp | MMap.h | system.mss

```
/*
 * Initialization functions in xgpio_sinit.c
 */
int XGpio_Initialize(XGpio *InstancePtr, u16 DeviceId);
XGpio_Config *XGpio_LookupConfig(u16 DeviceId);

/*
 * API Basic functions implemented in xgpio.c
 */
int XGpio_CfgInitialize(XGpio *InstancePtr, XGpio_Config * Config,
            UINTPTR EffectiveAddr);
void XGpio_SetDataDirection(XGpio *InstancePtr, unsigned Channel,
                u32 DirectionMask);
u32 XGpio_GetDataDirection(XGpio *InstancePtr, unsigned Channel);
u32 XGpio_DiscreteRead(XGpio *InstancePtr, unsigned Channel);
void XGpio_DiscreteWrite(XGpio *InstancePtr, unsigned Channel, u32 Mask);


/*
 * API Functions implemented in xgpio_extra.c
 */
void XGpio_DiscreteSet(XGpio *InstancePtr, unsigned Channel, u32 Mask);
void XGpio_DiscreteClear(XGpio *InstancePtr, unsigned Channel, u32 Mask);

/*
 * API Functions implemented in xgpio_selftest.c
 */
int XGpio_SelfTest(XGpio *InstancePtr);

/*
 * API Functions implemented in xgpio_intr.c
 */
void XGpio_InterruptGlobalEnable(XGpio *InstancePtr);
void XGpio_InterruptGlobalDisable(XGpio *InstancePtr);
void XGpio_InterruptEnable(XGpio *InstancePtr, u32 Mask);
void XGpio_InterruptDisable(XGpio *InstancePtr, u32 Mask);
void XGpio_InterruptClear(XGpio *InstancePtr, u32 Mask);
u32 XGpio_InterruptGetEnabled(XGpio *InstancePtr);
u32 XGpio_InterruptGetStatus(XGpio *InstancePtr);
```

system.hdf | MMap.cpp | MMap.h | system.mss | dip2

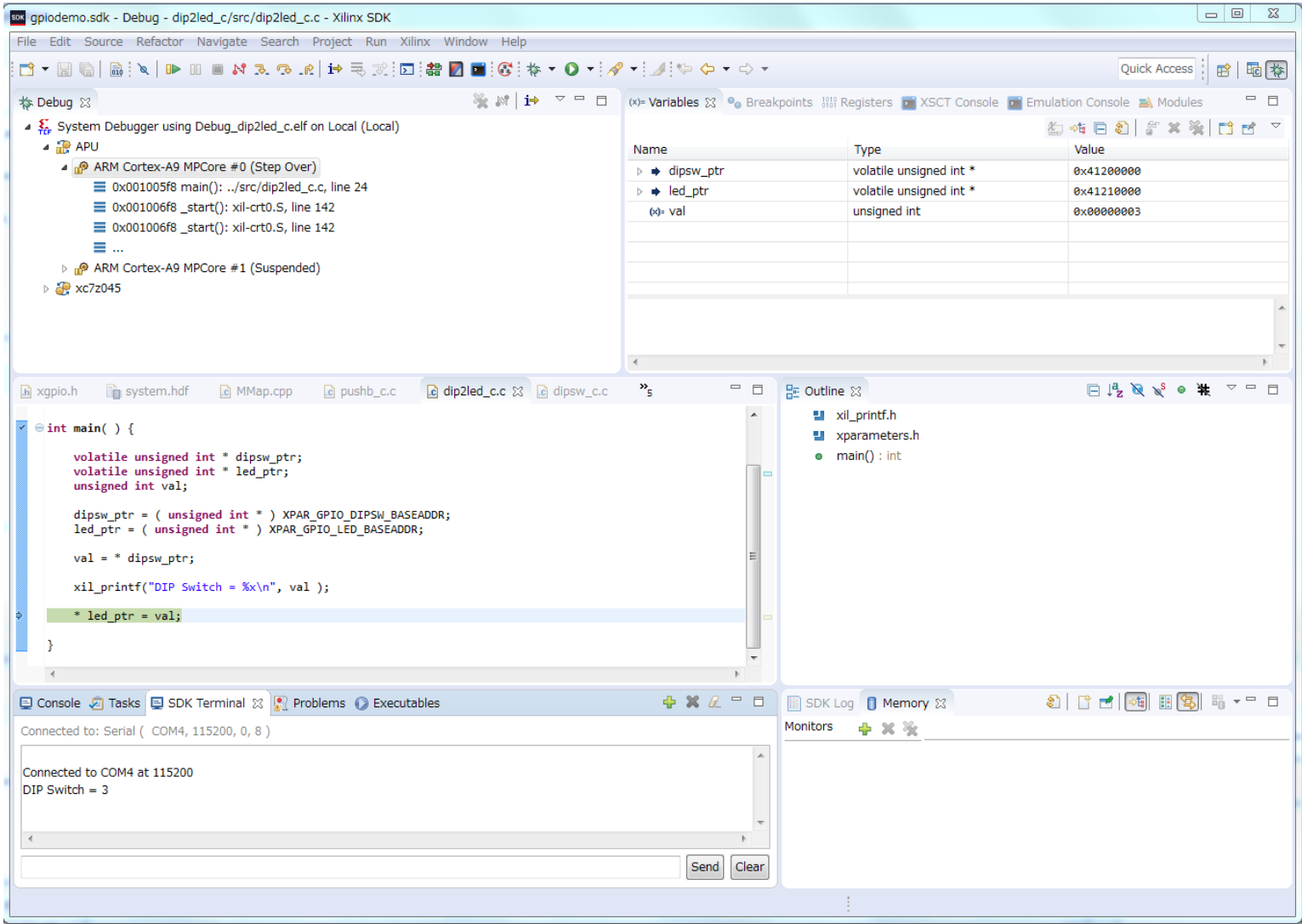
Peripheral Drivers

Drivers present in the Board Support Package.

gpio_dipsw	gpio	Documentation	Import Examples
gpio_led	gpio	Documentation	Import Examples
gpio_pushb	gpio	Documentation	Import Examples
gpio_snapshot	gpio	Documentation	Import Examples
gpio_timer_control	gpio	Documentation	Import Examples
gpio_timer_data	gpio	Documentation	Import Examples
ps7_afi_0	generic		
ps7_afi_1	generic		
ps7_afi_2	generic		
ps7_afi_3	generic		
ps7_coresight_comp_0	coresightps_dcc	Documentation	
ps7_ddr_0	ddrps	Documentation	
ps7_ddrc_0	generic		
ps7_dev_cfg_0	devcfg	Documentation	Import Examples
ps7_dma_ns	dmaps	Documentation	Import Examples
ps7_dma_s	dmaps	Documentation	Import Examples
ps7_ethernet_0	emacps	Documentation	Import Examples
ps7_globaltimer_0	generic		
ps7_gpio_0	gpiops	Documentation	Import Examples
ps7_gpv_0	generic		
ps7_i2c_0	iicps	Documentation	Import Examples
ps7_intc_dist_0	generic		
ps7_iop_bus_config_0	generic		
ps7_l2cachec_0	generic		

BareMetal Software

- System Debugger



Linux Kernel

- Petalinux Tools
- petalinux-create
  - Create a linux kernel project
  - Create a kernel module or a user application
- petalinux-config
  - Configure linux kernel parameters
  - Configure rootfs file system contents
- petalinux-build
  - Build a kernel
  - Build a kernel module or a user application
- petalinux-package
  - Generate a linux package
- petalinux-boot
  - Boot a kernel image on the system emulator
  - Boot a kernel on a remote target

Linux Device Drivers

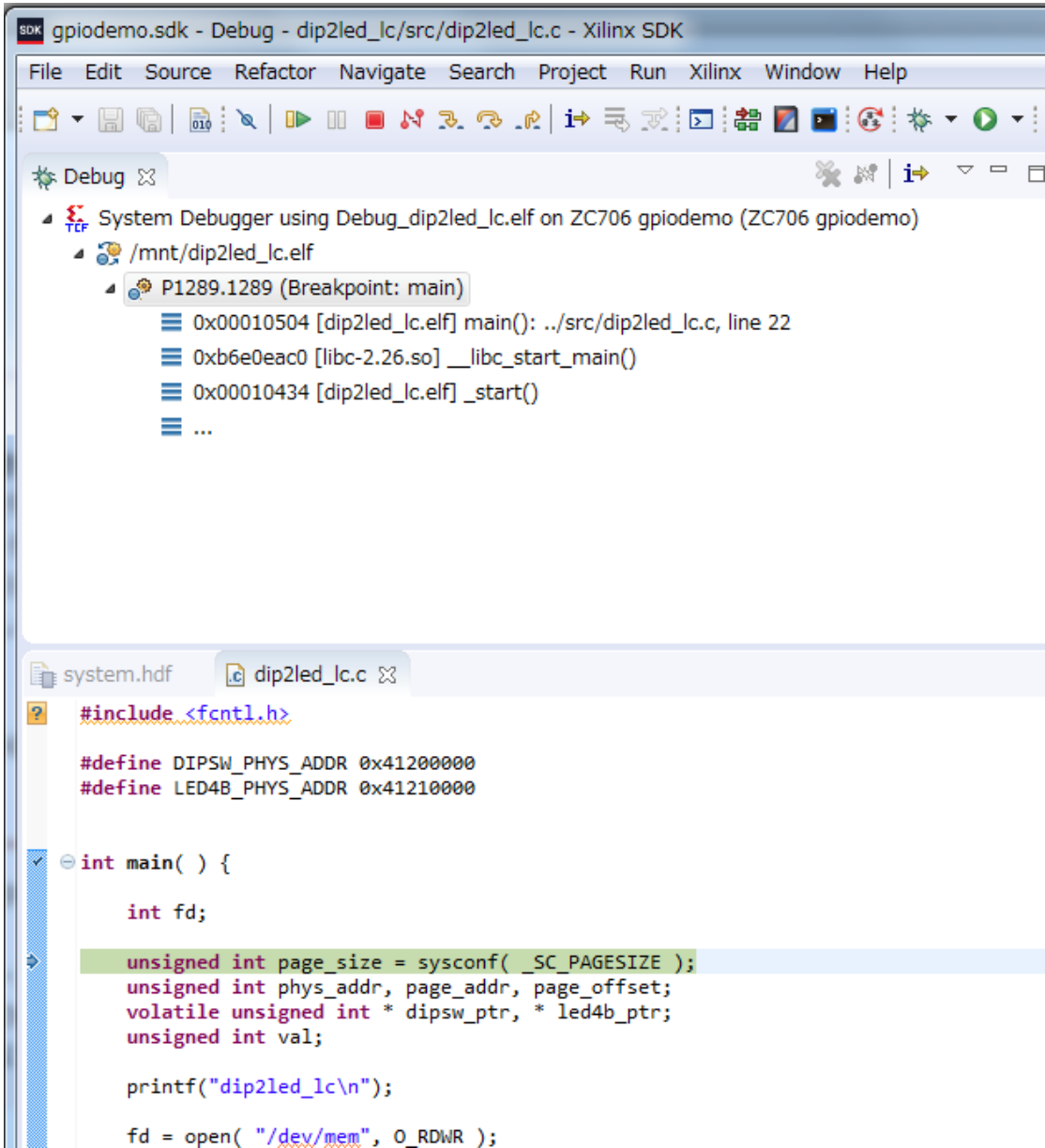
- Kernel Module
  - Running in the kernel space
  - Kernel library
  - Registered in Device Tree
  - Interrupt handler
- Character Device
  - System call from user space
  - Copy to user, copy from user
  - Sleep and wake up calls
- Hardware IP
  - Dedicated device driver if necessary
  - Application program interface
  - Implement in standard package

Linux User Application

- GNU C/C++ programming languages
  - System services
  - C and C++ standard libraries
- Python scripting
- Hardware access from user space
  - /dev/mem device
  - mmap service
- Interrupt handling – need a kernel module
  - Via a user-written character device
  - read function call

Debugging user applications

- Vivado SDK
- Debug through TCF (Target Communication Framework)Agent running on the target Linux system
- Same debugging features with BareMetal



Future Plans

- Zynq Development Portal
  - HTML Documents
  - Tutorials
  - Schematics
  - Source Code
- PTZ Forum
  - Communication
  - Information Exchange
  - Code Library - GIT

Zynq Development Portal

- My private web page

http://www.icepp.s.u-tokyo.ac.jp/~sakamoto/research/atlas/tgcelex/vivado/index.html

Topics covered

- IP usage
- Hardware design
- BareMetal software
- Building Linux OS
- Linux application

More topics

- Create user IP
- High Level Synthesis
- PTZ design

PTZ Forum

- OpenIt PTZ Project
- A User Community of PTZ
- PTZ Technical Information
  - Schematics
  - Physical constraints
  - Board support package
- Example Designs
  - Design files
  - Sample programs
  - Device driver