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THE INTERNATIONAL JOURNAL OF
ELECTROMAGNETIC COMPATIBILITY™

2013

EMC TEST & DESIGN GUIDE

SPECIAL FEATURE:
**WE ASKED,
YOU ANSWERED**
EMC EMPLOYMENT SURVEY

SALARY



CAREER SATISFACTION

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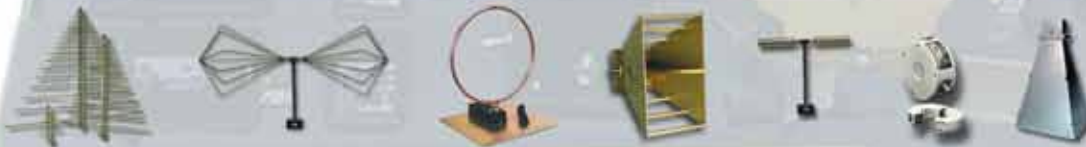
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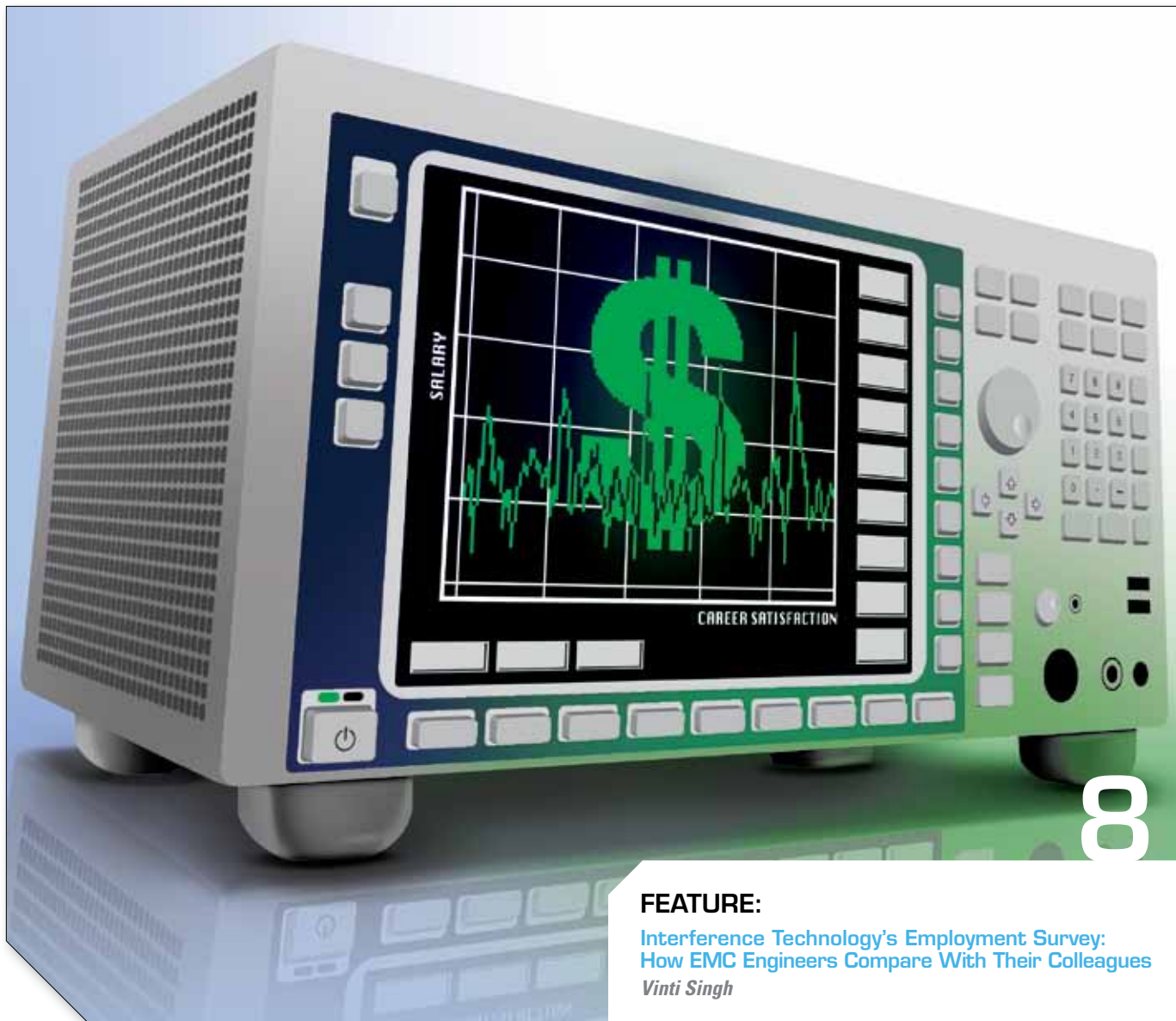
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**SPECIAL FEATURE:
2014 EMC TEST LAB DIRECTORY**

Check out our updated 2014 EMC Test Laboratory Directory, featuring more than 500 test labs around the world. The listings are arranged geographically, with details of services offered, website addresses and contact phone numbers, to provide a quick and easy reference guide to EMC testing services nearby, no matter where they are located.

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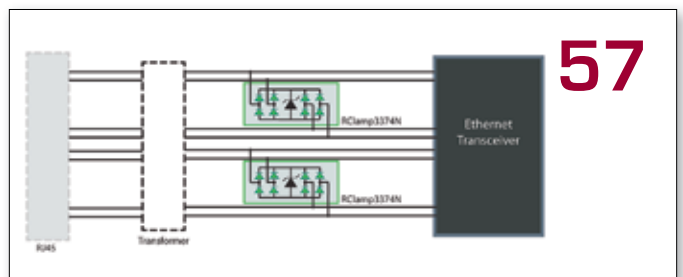
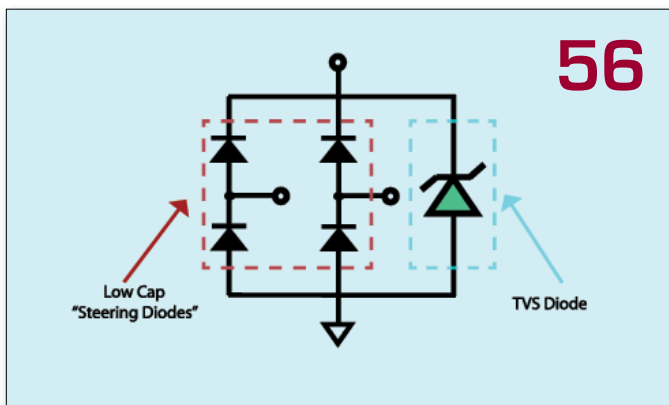
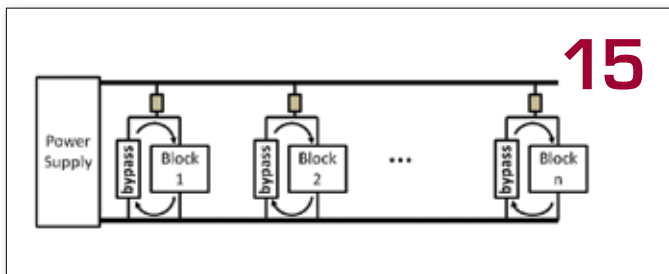
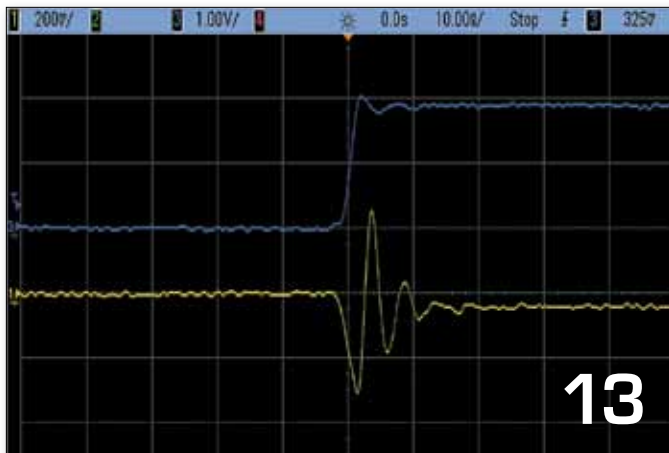
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New Ways to See EMC



WELCOME TO THE 2013 EDITION of the *Interference Technology* EMC Test & Design Guide, where you will find an updated worldwide directory of test laboratories (page 18) and articles related to all aspects of EMC testing and design.

Topics in this issue include power design for low EMI, charge generation of ESD sensitive devices, MicroTCA computing architecture and how it handles EMC, and defending Ethernet ports from electrical transient events. Also included is part one of an article on EMP protected infrastructure with shielded buildings & solar rooftops. Look for part two in our

2014 EMC Directory & Design Guide in April!

As you may have noticed, *Interference Technology* has been publishing a general interest feature article in every issue this year. We've covered a range of topics, from the challenges women face in engineering, to up-and-coming student engineers, to the feature in this issue on the current status of the EMC workforce (page 8). Our information was gathered after we sent an employment survey to our readers, and you responded! We were able to get an interesting glimpse of EMC engineer concerns, age ranges, job satisfaction, and yes, salaries. Now you can see for yourself how you rank among your colleagues.

As always, we appreciate your feedback and suggestions for future articles –either technical or general interest, or both. You can send any suggestions to me directly at bstas@item-media.net.

2013 has brought a lot of new content to *Interference Technology*, both in print and online. I hope you were able to join me during several webinars we hosted throughout the year. If not, they are archived and available to watch on our website, interferencetechnology.com – just click the “Webinar Series” link on the right-hand side. Our first collection of webinars, “EMC Basics” by Keith Armstrong, proved to be very popular for the new engineer, or someone who simply wanted to brush up on their EMC knowledge.

Another new and exciting development, starting with this issue, is the addition of exclusive content in our enhanced digital publications. You can still subscribe in print, but we encourage you to go 100 percent digital with us – if you do, you will get exclusive content not found in the digital editions available to print subscribers. You will also receive your magazine earlier, and help the environment at the same time. Still like your paper copy? No problem – you can download and print it so you have an exact copy of the magazine. Change your subscription to ‘digital only’ on our website – click the “subscribe” link at the bottom of the homepage.

I hope you continue to use us as your No. 1 EMC resource as we strive to provide new ways EMC professionals can read, watch, learn and interact.

Belinda Stasiukiewicz
Editor

SUBSCRIPTIONS

ITEM, *InterferenceTechnology*—The EMC Directory & Design Guide, EMC Symposium Guide, Europe EMC Guide and EMC Test & Design Guide are distributed annually at no charge to engineers and managers engaged in the application, selection, design, test, specification or procurement of electronic components, systems, materials, equipment, facilities or related fabrication services. Subscriptions are available through interferencetechnology.com.

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2013 EMC EMPLOYMENT SURVEY: HOW EMC ENGINEERS COMPARE WITH THEIR COLLEAGUES

BY VINTI SINGH

AS THE ELECTRONICS INDUSTRY continues to expand, employment opportunities for EMC engineers continue to grow as well. Products are becoming increasingly complex, and compatibility issues are arising ever more frequently. With each new advancement, EMC engineering jobs around the nation become more important, and more secure.

Experienced EMC engineers, especially those with specialized knowledge, are in demand, and these plum positions are not pencil-pushing desk jobs. Today's EMC engineers are getting hands-on in the lab and constantly having to stay on the cusp of rapidly progressing innovations. They told *Interference Technology* this challenging atmosphere is why their day's work is so satisfying. Interference Technology received this feedback, and more, in its first nationwide salary survey of EMC/EMI engineers.

Interference Technology sent a survey to a list of more than 15,000 EMC, design, and test engineers, from July through August 2013. Several hundred people responded to the request.

The results indicate that overall, the engineers are mostly satisfied with their career choices and current positions and value the complex problem-solving challenges of the job.

"What a wonderful time to be a part of the compliance world, with every new wave of emerging technologies comes a new wave of compliance challenges," a corporate manager from Georgia commented in the survey.

Of course, the 'compliance world' includes much more than just EMC regulations, with existing regulations on radiocommunications, telecommunications, product safety, restriction of hazardous substances, and – increasingly – sustainability (e.g. power efficiency, standby power, etc.), and in smaller companies one compliance engineer might have to deal with the lot.

Compared to just 20 years ago, a number of new industries have emerged in compliance, noted Dan Paulson, the CFO of Paulson and Clark Engineering, an engineering services provider in White Bear Lake, Minnesota.

"A lot of engineers are not even aware of all the applicable fields, and you have a lot of industries pulling from the same pool of candidates," Paulson said.

Salaries at Paulson & Clark have stayed stable in recent years.

Robert Kado, the EMC department manager and senior technical specialist for Chrysler Group, observed the same trend in the EMC segment of the automotive industry. His lab is busy with research

and development of Bluetooth technology, alternative powertrain, and wireless charging for smart devices.

"The trend is that it's hard to find the right people," Kado said. In mid-August, an opening in his department had remained unfilled for a month. The company has offered bonuses and steady salary increases to its EMC team for the last three or four years, and so far that has seemed to be the key to retention.

Hiring experienced talent is even harder in non-metropolitan areas. Therefore, Jim Teune, the lead EMC engineer at Gentex, has tried a different strategy. Gentex is a leading supplier of automatic dimming rearview mirrors and lighting assist driver features to the automotive industry, and is based in Zeeland, Mich. He finds fresh graduates with some background in radio frequency and trains and grows them into experienced team members. He keeps turnover low by giving engineers challenges that are suited to their individual skill sets.

"It works for me," Teune said. "They stick around longer. Plus they are productive and enthusiastic about their job."

Slightly more than a quarter of respondents said they have been in their current positions for more than two decades. About a quarter of survey respondents said they have been in their current position for one to two decades. Almost 20 percent have been in their

current position for five to 10 years.

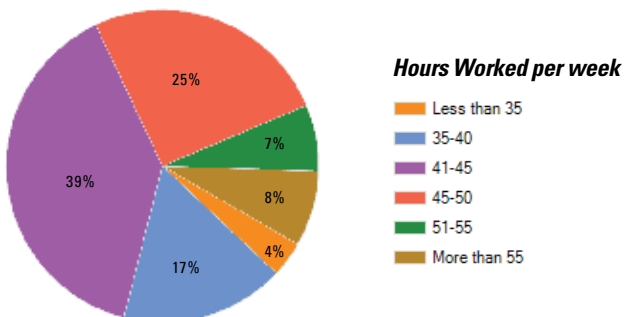
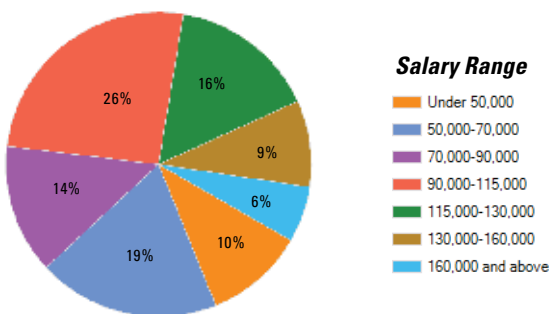
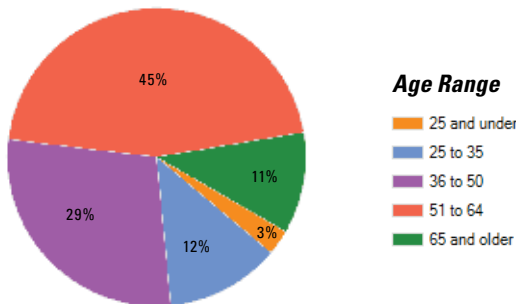
Michael Oliver is the vice president of EMC/ electrical engineering for MAJR Products Corporation, an EMC shielding manufacturer in Saegertown, Penn. He has been with MAJR for 12 years, and says his peers in the field average close to a decade, and he has witnessed very little turnover.

Companies value their EMC engineers because without them, a product or system risks not meeting the requirements of MIL-STD-461, 464, the Federal Communications Commission, and other regulatory bodies, Oliver said.

It takes three to five years to become truly proficient in the EMC field, said Daryl Gerke, an EMC consultant who is a partner at Kimmel Gerke Associates, based in St. Paul, Minn. But about 90 percent of the concepts are applicable across the electronics industry, he added, which makes for a highly portable experience. Therefore, someone in the military field could easily transition to automotive or medical or consumer electronics. The biggest learning curve is in grasping the regulations and requirements specific to that segment. When an EMC engineer is laid off, it is not unusual for them to get another job offer in a day, or even an hour, Gerke explained.

**Thirty percent of survey
respondents make more
than \$115K, while
45 percent make less than
\$90K per year**

SURVEY RESULTS



In July, more than 200 of our readers answered our employment survey. Above and on the next page are results. For more charts, view our enhanced digital edition - to receive this version, visit www.interferencetechnology.com and click 'subscribe' at the bottom of the homepage.

But a career in EMC can be very much more satisfying than just compliance, says Keith Armstrong, an EMC consultant with Cherry Clough Consultants Ltd. in the UK. He says that using good EMC engineering from the start of an electronic product design project (e.g. in circuit design, component choice and PCB layout) helps achieve good signal integrity and power integrity more quickly, meaning the product gets to market quicker, functions better, costs less to manufacture and is more reliable in the field. So EMC compliance engineers who educate their designer colleagues in good EMC design can make a huge improvement to the financial performance of their employers.

Of the electrical engineers surveyed, 32 percent identified specifically as EMC engineers. Other respondents identified as electrical engineers, compliance engineers, design engineers, test engineers or otherwise tangential to the field.

Most respondents, about 70 percent, said they felt mostly or very secure in their current positions.

Twenty-six percent of respondents said they make between \$90,000 to \$115,000. Thirty percent total of respondents total said they make more than \$115,000, while about 45 percent total said they made less than 90,000.

Different sectors of EMC enter boom times depending regulatory rollouts, Gerke said. The medical sector saw such a boom in the early 1990s when the federal Food and Drug Administration and then the European Union began taking a special interest in medical devices. After 9/11, the military sector became especially active.

In 2010, the average salary for an electrical engineer with a bachelor's degree was \$87,180, according to the Bureau of Labor Statistics Occupational Outlook Handbook. The average salary for an electronics engineer in that same year was \$90,170. The labor statistics bureau estimates a 7 percent increase in electrical engineering jobs between 2010 and 2020 and estimates job openings due to growth and replacement needs will be close to 50,000.

About half of the respondents said they were mostly or very satisfied with their salary level. A little more than 20 percent said they were not very or not at all satisfied with their income.

About 55 percent of the survey takers said their salary and benefits were a major factor contributing to their job satisfaction.

About half of the respondents reported feeling average amounts of stress, while about 40 percent said they felt a significant or very large amount of stress.

About 40 percent of respondents said they worked, on average, 41 to 45 hours a week. About 35 percent reported working 45 to 55 hours a week.

Some engineers commented stress resulted from having to coordinate with non-EMC colleagues or clients who do not understand EMC compliance needs.

"The field of compliance has changed drastically in the past few years," said an EMC engineer in Massachusetts in the comments section of the survey. "The customer base has changed where the client is no longer a compliance engineer coming to test, but in fact a program manager. They have no ideas how to fix the EMI problems and rather skirt around product issues then simply fixing them."

An EMC engineer from Colorado shared his frustration and said the business managers are the source of stress, as they don't want to fix EMI issues, but rather "just BandAid and keep shipping the product."

Stress also results from the fact that products are routinely designed and manufactured overseas, with all initial compliance checks performed there as well, he continued. Once the product reaches the States, it usually is checked again and often does not meet the standards. Design changes are hard to implement when it is hard to determine what the designer intended for the product to do.

Most respondents said they were mostly satisfied or very satisfied with their choice of engineering as a career. Less than 15 percent reported that they were somewhat or not satisfied. None of the people surveyed said they were unsatisfied.

About 40 percent of survey respondents said they felt a significant or very large amount of stress in their jobs

The biggest reason they attributed for their satisfaction was how often they were challenged and had to solve problems.

The survey takers commented the field is constantly expanding in its scope, and the variety of challenges encountered mean they are learning something new on a daily basis.

"I tell my guys, you are forever a student of EMC," Teune said. "There's always a changing standard or a new requirement. Our product evolves. Even though we might be using the same core design, we're looking for cost saving measures."

Opportunities to be creative and relationships with colleagues were other major contributing factors to job satisfaction, according to the survey.

"It's a difficult job that requires the skills of a 'rocket scientist'," said an electrical engineer from Pennsylvania.

Company size and location were a major factor for almost 40 percent of respondents.

An EMC engineer from Hawaii described his job as, "a nice, fun interesting job nearby home, which is very positive."

Similarly most respondents said they are mostly satisfied or very satisfied with their current positions. Almost 20 percent said they were somewhat satisfied and about 5 percent reported being unsatisfied.

"Private companies are so much nicer than public companies," said an electrical engineer from Colorado. "You still have to work hard and are busy, but you do things because they need to be done and not because of some ignorant corporate objective, executive metric, or political jockeying."

The majority of respondents said they were not looking for another position, but almost 40 percent of survey takers said they were passively searching for another job.

About 80 percent of respondents said they would recommend the field to a child or a friend.

"EMC is not a career for everybody, or even for every electrical engineer, but can be a very satisfying career for those with the right mind set," said an EMC/EMI engineer from Missouri.

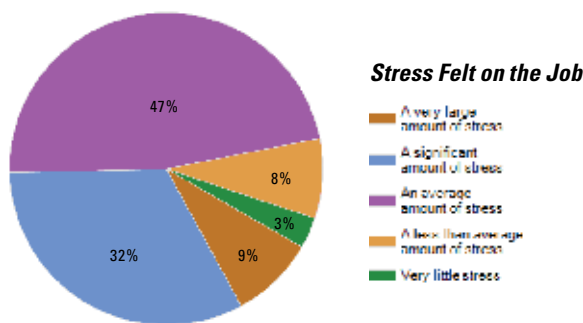
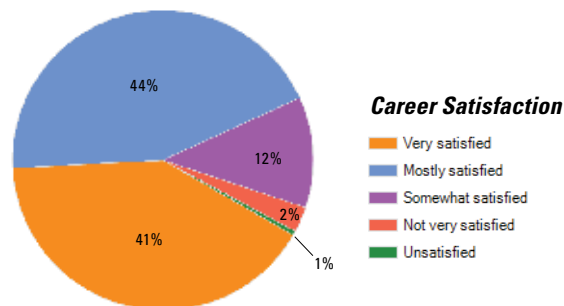
The majority (56 percent) of the respondents were 51 or older – approaching retirement age. About 40 percent were aged 25 to 50, and only about 3 percent were 25 and under.

"Five and a half years and I'm done [working]," said an engineering manager from Maryland, while an EMC engineer from Florida questioned, "Where is my replacement? Very few young folks qualify." (To see *Interference Technology's* article on up and coming student engineers, refer to the 2013 EMC Symposium Guide)

EMC consultant Daryl Gerke said he is in his 60s and his partner is on his 70s, but often feel like the "younger guys" at EMC conferences.

"I think there is a need for new fresh blood. Companies aren't good at responding to that," Gerke said.

SURVEY RESULTS



When one of Gerke's mentors was in his early 60s, he began pressing his employer to start grooming his replacement, but management didn't heed his advice. At 65, he retired, and not long after, the company asked him to return as a consultant.

The survey results suggested the industry remains a male dominated one, as only slightly more than 7 percent of the respondents identified as female.

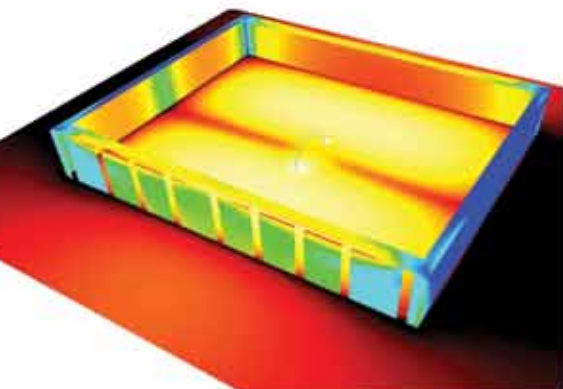
"Of the hundreds of EMC professionals I know, just three or four are women," said Michael Oliver, "And the only women I know who do go into it are from India, China or other countries. I think the U.S. is really deficient in promoting EMC to women." (*Interference Technology* has also published an article on women engineers; see the article in the 2013 EMC Directory and Design Guide.)

For more charts and additional information on our survey results, sign up for our enhanced digital versions of *Interference Technology*. Visit www.interferencetechnology.com and click the 'subscribe' link at the bottom of the homepage.



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CMOS is different: PCB design for both low noise and low EMI

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ABSTRACT

Achieving low power supply noise does not automatically assure low EMI. Fortunately a PCB layout designed for low EMI does automatically result in low noise. The techniques presented here do achieve both goals.

MUCH HAS BEEN spanning several decades, on how to design printed circuit layouts for low EMI [1] [2]. Yet, as a practicing RF engineer I repeatedly encounter boards with layouts that produce significant amounts of EMI. In this age of plentiful information, one would wonder why these problems persist. The answer is not a surprise: much of the information available is misleading and even wrong. A good survey on this is in [2]. Designers therefore choose to learn on their own, which is horribly inefficient and costly. The results presented here have been known for a long time [5]. However it appears that they are forgotten, because they are almost never

used. This article is a reminder on how easy low-EMI PC layout really is. Good EMI design for printed circuits is not that hard, but it does require attention to detail and awareness of the underlying physical processes. And there are no shortcuts. Follow the rules and success is rather easy. Cut any corners and problems rise rapidly.

Electromagnetic theory tells us that there are two conditions necessary to keep EMI at an inherently low level. These conditions are:

1. Minimize the impedance and current encounters
2. Minimize the area of each current loop

By far, EMI publications discuss well how to achieve the first requirement. Essentially nobody though discusses the second criterion. This is the loophole that allows an otherwise low noise board to still produce significant amounts of EMI. Fortunately the solution is straightforward, and easily designed into the PCB layout at the outset. Here we show both what needs to be done, along with why and how well the basic technique works.

First and foremost: know ALL your sources of dynamic currents. The most obvious source of dynamic current is from signals propagating along the signal traces. When these signals have fast edge speeds (2 nanoseconds or less) the board layout needs to have controlled impedance and accurate line source and load terminations. This is the standard fare of signal integrity, and will not be discussed more here. But, particularly when CMOS technology is used, there is another 'hidden' source of dynamic currents that, in my experience, is much more of an EMI problem than any signal current.

This additional dynamic current has several names: crowbar current, short-circuit

current, supply spike, etc. It is a natural artifact of how CMOS gates are operated inside an integrated circuit, which is shown in Figure 1. In effect, all CMOS gates are composed of switches that alternately connect the gate output directly to the power supply, or to ground, whether the output state should be a '1' or '0' respectively.

The power supply current spike follows from the chip-design criterion that it is not allowed for both switches to be OFF at the same time. Therefore when one is turning OFF and the other one is turning ON, there is a very brief and intentional moment when both switches are partially ON. During this brief instant (usually 1 nanosecond or less) there is a current path (resistance) directly across the power supply, causing current to flow that does not contribute to the output logic signal. This current, though brief, can have a very large magnitude. One small CMOS IC, measured in Figure 2, shows that this spike current magnitude is 300 mA in this instance. Reactances in the current path are excited by the current spike and respond with a damped oscillation. Everything is over in 15 nanoseconds.

Synchronous logic, extremely common in CMOS logic, makes EMI worse because it causes all output transitions to occur close to the same time. This causes all of these current spikes, one for each and every gate in the IC, to happen together. The currents add, of course, making for a very large source of dynamic current. This must be very carefully managed to avoid generating lots of EMI. And this is completely independent from signal integrity.

Electromagnetic radiation is driven by currents, not voltages. The secret to low EMI design is in managing all of the dynamic currents such that the resulting radiation is minimum, though it will never be zero. This effectively quiets any potential transmitter. To achieve this low EMI, electromagnetic theory tells us that the area of each current loop must be made small. How to do this is the trick for low EMI design.

Again, all currents are loops [3]. This we learn in beginning circuit analysis class. Afterwards it is all too easy to forget this fundamental fact when we progress to think that current comes

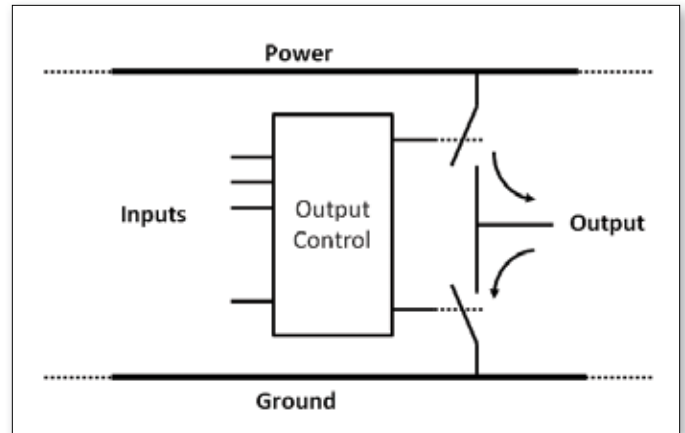


FIGURE 1: General CMOS circuit structure: controlled switches alternately connecting the output to one of the power supply rails.

from the power supply, passes through our circuit, and then disappears into 'ground'. Or worse, to simulate that all current returns are through 'Node 0'. Both of these common habits obscure reality, which we do at our peril: causing performance degradation, schedule slips from extra work that has to happen, cost increases from EMI modifications and extra testing that shouldn't be needed, and lost revenue from late product introductions.

A realistic view of current flow is shown in Figure 3. Signal current loops begin and terminate at the initiating circuit block. Power current loops originate and terminate inside the power supply. Since no practical circuit has zero impedance, Ohm's Law tells us that there must be voltage drops across all impedances the current encounters around the loop. This includes the return path! As more currents combine in their return to the power supply, the voltage drops across impedances do affect the supply voltage experienced by circuitry such as 'Block 1'. Hence, it is certainly vital to keep all power and return (this name is much preferable to the word 'ground') impedances as

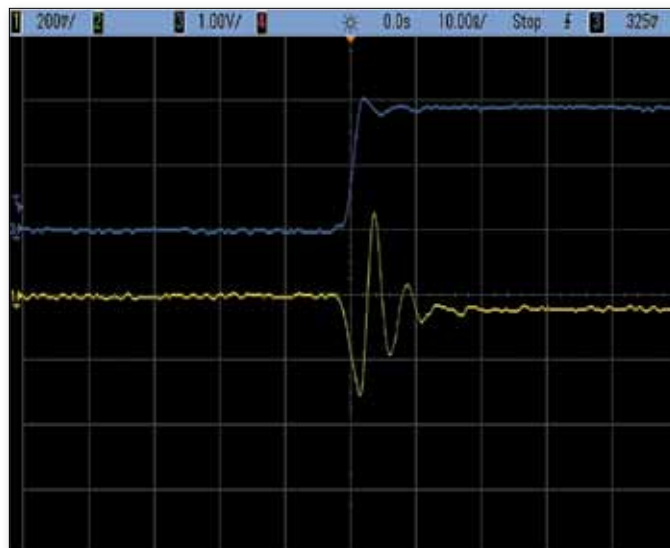


FIGURE 2: Measured typical CMOS power supply current spike at times of output transitions. Scale is 200 mA/division (bottom trace).

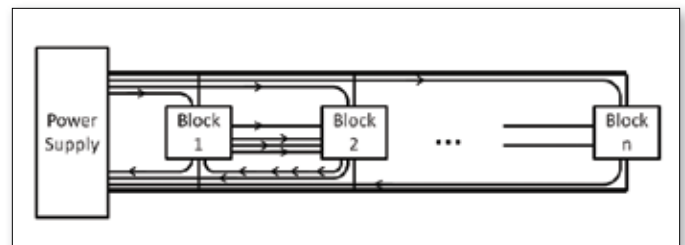


FIGURE 3: Current loops in a typical circuit

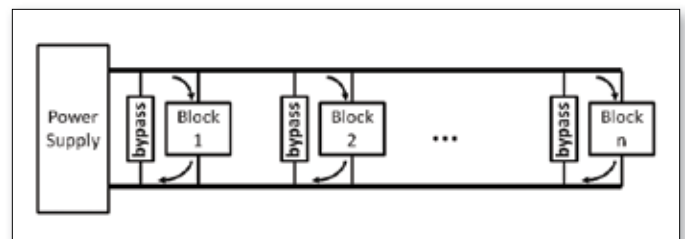


FIGURE 4: Addition of bypass paths for the power supply current loops in each circuit block.

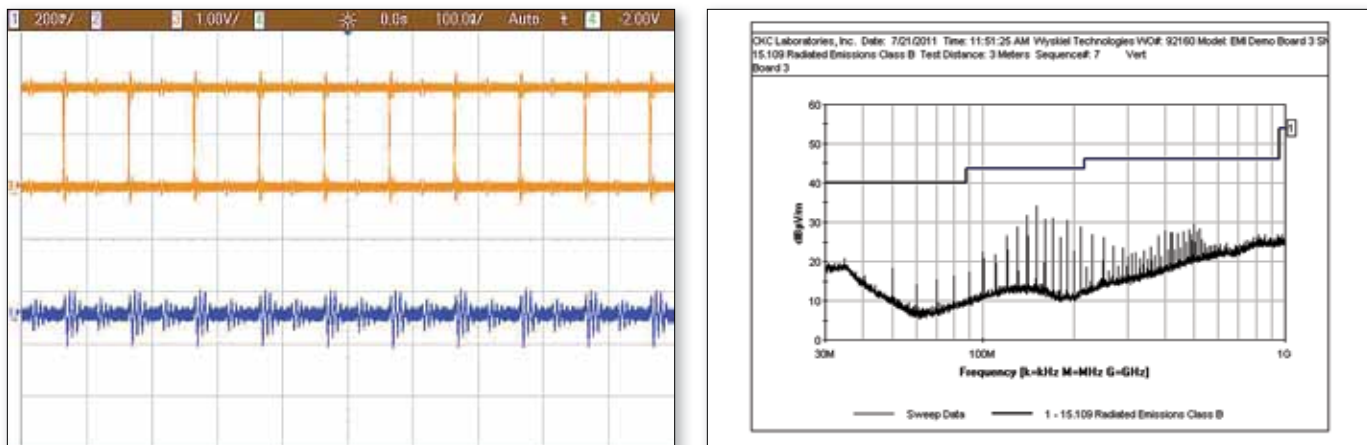


FIGURE 5: Layout with 2 sided copper, grounded pour on both sides, and bypass capacitors on each CMOS IC: **a)** power supply noise (lower trace, 200 mV / div.), **b)** formal EMI scan.

small as absolutely practical.

BYPASSING

For high frequency current spikes, which cause all of our EMI problems, it is desirable to give them a return path very close to where they are generated. This is the idea of bypassing, shown in principle in Figure 4. While the total power needed to operate the circuit block must flow from and return to the power supply,

the troublesome current spike currents only need to return to the power supply node from where they came.

Measured performance of a 2-layer PCB with bypass capacitors at each CMOS IC is shown in Figure 5. This PCB includes copper pour on both top and bottom, with both pours connected to the ground node. Including these pours has a significant beneficial effect [4] and is therefore used here to establish a performance baseline. We note from Figure 5a that the power supply noise is 200 mV peak to peak, and the EMI scan in Figure 5b shows EMI products rolling off above 500 MHz and having a peak around 150 MHz.

When originally conceived over 30 years ago, the addition of bypass capacitors (low AC impedance, high DC impedance) worked very well. This is because the impedance of power and return networks in those days was fairly high. Multi-layer PCB technology was not yet available. Today multi-layer technology is readily available, which is both a blessing and a problem.

POWER PLANES

With multi-layer PCB technology, we are able to dramatically reduce the impedance of both supply and return paths [3]. This is ideal in meeting objective (1) for achieving low EMI. It turns out that this actually makes achieving objective (2) more difficult.

Why this is true we can discern from Figure 4. Each bypass capacitor is connected directly in parallel with the power supply and the circuit block. We again remember from our first circuit analysis class that in any parallel circuit, current will predominantly flow in the path with the lowest impedance. Which path has the lowest impedance? It turns out that when power and return (ground) planes are used, the lowest imped-

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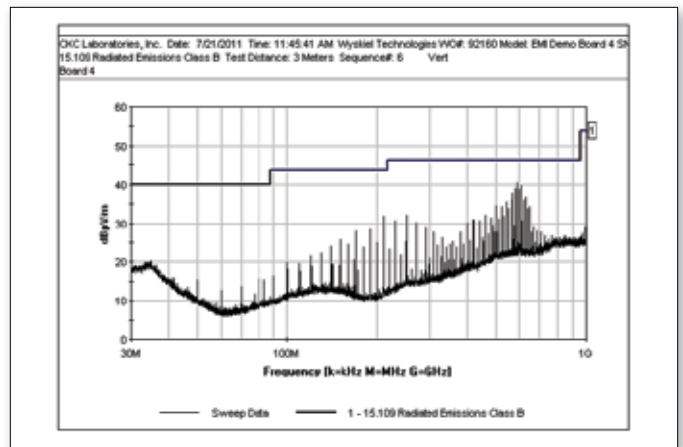
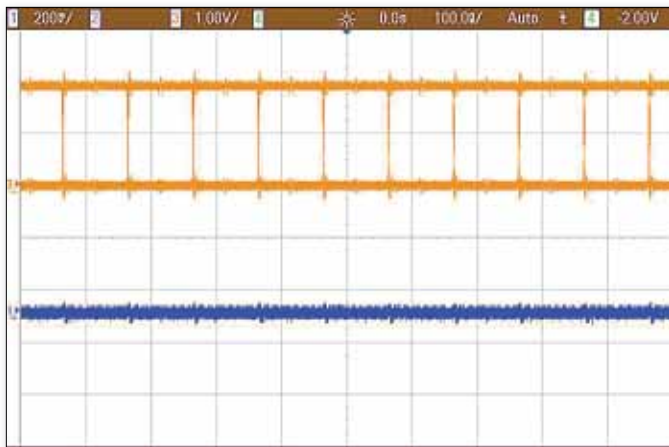


FIGURE 6: 4-layer PCB with internal power and ground planes, with bypass capacitors at each CMOS IC: **a)** power supply noise (lower trace, 200 mV / div.), **b)** formal EMI scan.

ance path is through these planes. So the electrons, being the most lazy (and therefore predictable) creatures in this universe, will flow through the planes. The bypass capacitors have almost no effect, unless the planes are shaped in such a way as they effectively have higher impedance at frequencies of interest.

I have seen many circuit boards that behaved the same whether the bypass capacitors were mounted or not. This is the reason why. As a result, we have the unexpected situation where the voltage noise is low, but the EMI is not. Our example board is one of them, as we can see in Figure 6. Taking the same circuit and part placement from the board used in Figure 5, but now using 4 layers with internal power and ground planes, we note a dramatic drop in power supply noise in Figure 6a compared to the measurement in Figure 5a.

But when we compare the EMI scans, Figure 5b shows a significant increase in the EMI radiation at UHF frequencies. The earlier peak at 150 MHz is gone, but there is now a dramatic increase in radiation above 500 MHz. This is a classic example of how we can reduce noise on the power supply, yet actually make EMI worse. The lower impedance of the power planes is definitely reducing the voltage from the CMOS currents, but the lower impedance is allowing the high frequency currents to flow over much wider area: the high frequency current loops are larger. This is proof that low impedance alone is insufficient to reduce EMI. We need to also force the current loops to be small. One more step is necessary to get what we need.

SOLUTION – LOCALIZED HIGH AC IMPEDANCE TO THE SUPPLY

The trick is to make the power planes look like they have much higher impedance at high frequencies, so that the high frequency spike currents return through the bypass caps and stay completely off of the planes. But at low frequencies we need current to flow through the low impedances that the planes are there for. Fortunately this is readily achieved by inserting an inductive element in the tap to the power plane, as shown in Figure 7.

Whenever we have both inductance and capacitance there will be resonance, which is something we do not want. This

is addressed by using a very low Q inductor, such as a ferrite bead. This part selection not only dampens out the resonance responses, it also broadens the effective bandwidth of the decoupling – both of which are very good things. The effect of adding this ferrite bead in each CMOS tap into the power plane is seen in Figure 8.

Comparing the supply noise traces of Figures 8a with 6a we see no material difference. Both boards have very low noise on the power distribution. There is a dramatic difference though between the EMI scans in these figures. Adding the ferrite beads has dropped the EMI at 600 MHz by more than 15 dB. Lower frequencies are also attenuated, though not quite as much. But this is the point: UHF EMI products can be inherently reduced in any board using CMOS circuits and power distribution planes, by simply making the bypass capacitors operate again with the insertion of ferrite beads in each tap to the power plane.

This means that both the ferrite bead inductance and the bypass capacitor on the CMOS IC side are vital. They work together in a partnership. Having only the bypass capacitors is worthless when power distribution planes are used. Having only the tap inductance without the bypass caps (I have seen this!) makes things much worse than doing nothing. But together, as we see in Figure 8b, these components are a powerful anti-EMI technique.

Including the ferrite bead into the original PCB design is extremely important. It is nearly impossible to add these later when an EMI problem arises in testing. Admittedly the addition of more components onto a tight PCB is not welcomed, but the

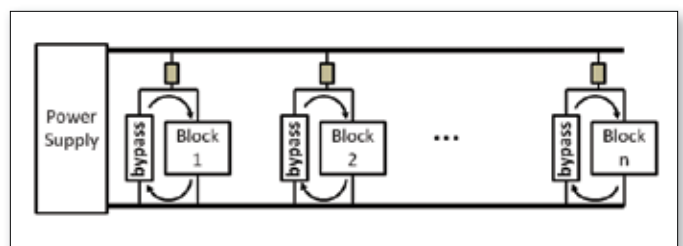


FIGURE 7: Power supply current loops are forced to flow through the local bypass capacitor when an inductive element is inserted, keeping them physically confined.

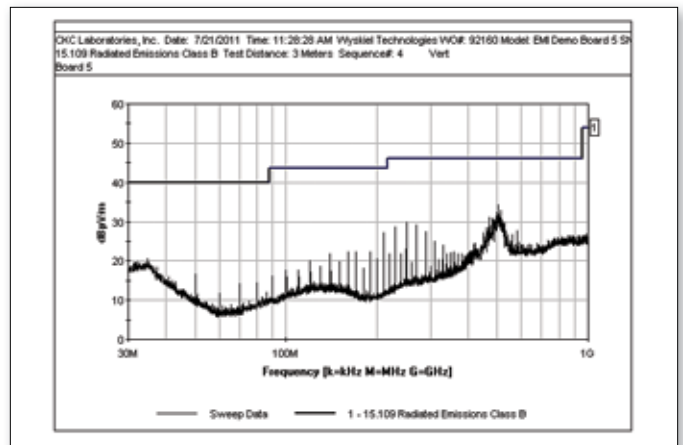
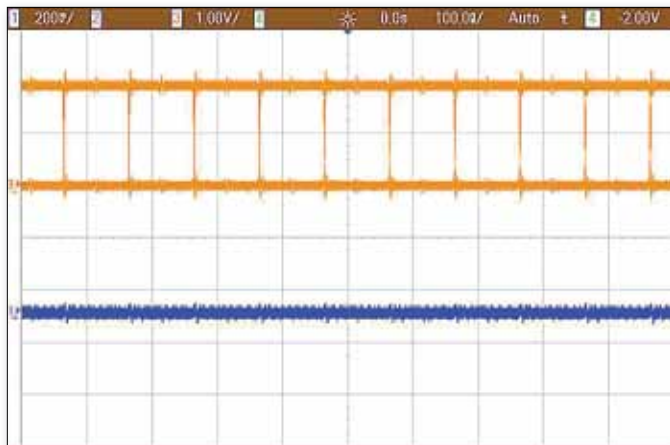


FIGURE 8: 4-layer PCB with internal power and ground planes, with bypass capacitors at each CMOS IC along with a ferrite bead in the power plane connection: **a)** power supply noise (lower trace, 200 mV / div.), **b)** formal EMI scan.

price for not doing it is later EMI problems. Compared to the cost of EMI testing and problem mitigation, along with product delays and those additional costs, the few cents and square millimeters needed for this insurance is cheap indeed.

With large CMOS IC devices, which also have multiple power and ground pins, there is one more step needed to be sure that this technique works. These large ICs usually have power on the chip partitioned into separate regions, meaning that on the chip

there is usually not a connection among all of the power supply (VDD) pins and the 'ground' return (VSS) pins. It is necessary to identify which VDD and VSS pins go together. The bypass capacitor must be connected between these matched pairs to have the desired effect. It is worthless to 'bypass' the VDD of one power region with the VSS of a different region. Though when the bypass capacitors are properly connected across each separate power region of the IC, and then with a ferrite bead in



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each tap into the power plane, the EMI from the board should look more like Figure 8b than Figure 6b.

CONCLUSION

Low noise design does not guarantee low EMI performance. The converse though is true: a low EMI design for CMOS does result in low supply noise. It is practical to simultaneously get low EMI, even at the microwave frequencies corresponding to high-order clock harmonics, and low noise voltages on power distribution networks in large digital printed circuit boards. The key is to confine signal and transient supply-current loops to physically small areas local to each CMOS integrated circuit. This is achieved with judicious choice of local bypass capacitors and adding inductive elements between the power distribution network and the IC / bypass capacitor parallel combination. It is important to assure that the bypass is connected between associated power (VDD) and ground return (VSS) pins for the particular IC.

These low EMI design techniques are very difficult to impossible to insert into an existing PC board that does not already use them. This simultaneous minimization is therefore something that must be designed in at the beginning. Doing so eliminates many of the problems encountered during EMI certification testing of the product before sale.

ACKNOWLEDGEMENT

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Earl McCune has more than 40 years of experience in radio and wireless technology, including circuit- and system-level designs. He is a graduate of UC Berkeley, Stanford, and UC Davis. He is also a serial entrepreneur in Silicon Valley, cofounding Digital RF Solutions (1986-1991) and Tropian (1996-2006). He regularly presents at international conferences and workshops, and is an instructor with Besser Associates. As an inventor and co-inventor he has 64 issued US patents. Contact him at emc2@wirelessandhighspeed.com.

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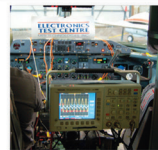
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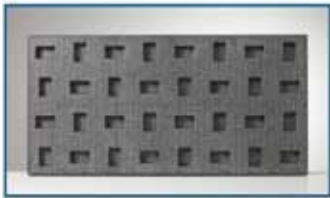
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| Liverpool | Diversified Technologies www.dttl.com | (315) 457-0245 | | | | | | | | | | | | | | | | | | | | | |
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| Melville | Underwriters Laboratories, LLC. www.ul.com | (631) 546-4346 | | | | | | | | | | | | | | | | | | | | | |
| Northport | Mohr, R.J., Assoc., Inc. www.rjm.li | (631) 754-1142 | | | | | | | | | | | | | | | | | | | | | |
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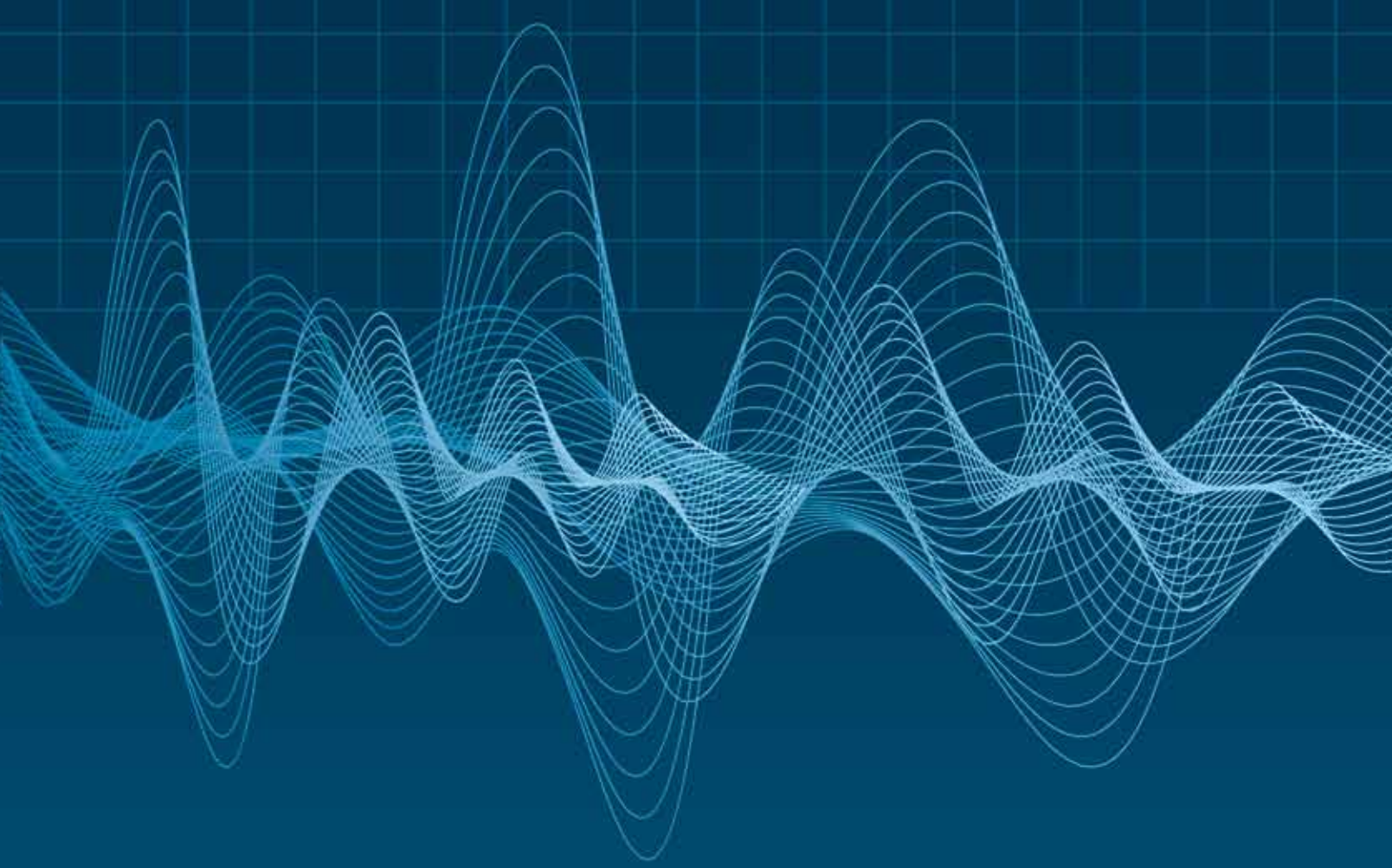
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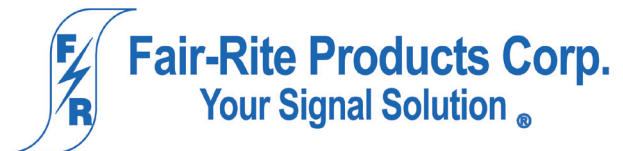
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seal with the enclosure. All AMCs have similar gasketing for consistency in EMC performance across various vendors' product lines. The side of the AMC has similar gasketing on one edge of the board. Gasketing is not required on all sides as the shape of the gasket creates enough force for a solid seal. Further, the shape of the gasket covers the top area of the top of the AMC panel block, so there is a significant area that aids in containment. See Fig 1.

EMC REQUIREMENTS FOR MICROTCA

The following is a brief excerpt of the EMC requirements from the MicroTCA.0 specification:

“All MicroTCA equipment shall meet Class A limits and should meet Class B limits of the following regulatory standards/requirements:

For ITE equipment in Europe: EN 55022 and EN 55024 (equivalent to CISPR22 and CISPR24 used in most countries)

For CO equipment in Europe: EN 300 386, Electro-Magnetic Compatibility (EMC) Requirements for Public Telecommunication Network Equipment, Electromagnetic Compatibility (EMC) Requirements (similar to EN 55022 and EN55024 combined).

For USA: FCC CFR 47 Part 15, Subpart B”*

Thus, MicroTCA utilizes established and proven Telecom and other standards for EMC, ensuring reliability.

EMC TESTING

EMC Testing of initial MicroTCA chassis are performed to IEC TS 61587-3 (2 GHz). The frequency range is 30 MHz to 3 000 MHz, with the attenuation values chosen for the definition

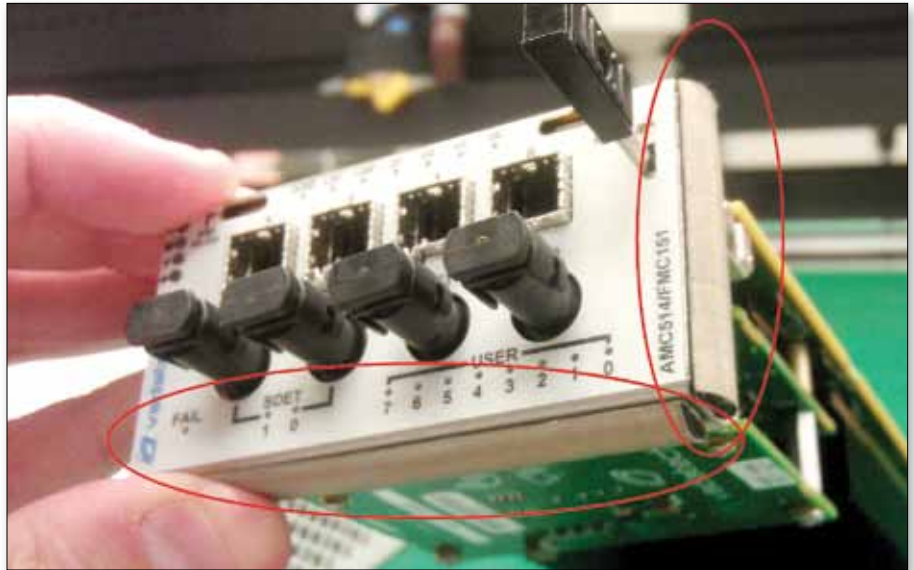


FIGURE 1: The photo shows the front of the AMC board's panel block with the gasketing on top and on one side. A close-look at the far left side of the panel illustrates the "rounded triangle" shape of the gaskets.

of the shielding performance level of cabinets and sub racks for the IEC 60297 and IEC 60917.

System-level testing is another important aspect of the specification. Regulatory EMC requirements call for compliance at the system level. Therefore, claiming conformance at the FRU (Field Replaceable Unit) level is not accepted (except for PC peripherals in some jurisdictions). Testing has to be done at the fully-loaded system level (representative worst case). The table below shows the recommended test cases based on the FRU type. See Fig 3*.

CHASSIS GASKETING

The MicroTCA chassis comes in several sizes and form factors. The most common are horizontal-mount chassis, often in 1U-3U heights. Even in a 1U height, a MicroTCA chassis can hold up to 12 AMCs, offering tremendous performance in a small space. The

enclosures also come in vertical mount orientations, typically from 4U to 8U high. These can hold standard 75mm wide (tall in this case) boards or double width sized at approximately 150mm.

Often, the AMCs provide enough shielding in those areas of the chassis. See Fig 2 of a MicroTCA chassis with very simple additional gasketing. But, additional gasketing may be required, which is easily implemented. Aside from the various types of boards that plug in, there are also Cooling Units (often redundant push-pull) that may require gasketing depending on the solution provided by the vendor.

HIGH PERFORMANCE, INHERENT EMC

MicroTCA provides a scalable, powerful, compact, and versatile platform



FIGURE 2: Additional gasketing is typically minimal for standard MicroTCA chassis, unless advanced shielding levels are required. The photo shows very standard metal gaskets easily implemented.

for all types of computing applications. Utilizing proven EMC techniques, the shielding performance of the specification is built-in to the architecture. This decreases the engineers risk and help to ensure more consistent performance. PICMG also provides an online short-form specification for those interested in the background of the technology.

**excerpt from PICMG® MTCA.0 Micro Telecommunications Computing Architecture (MicroTCA.0) specification.*

ABOUT THE AUTHOR

Justin Moll is director of marketing for VadaTech, Inc. With more than 15 years of embedded computing experience, Moll has previously worked in director and management-level positions for electronics packaging companies. He has a BS in Business Administration from the University of California, Riverside. He is active in the PICMG and VITA communities and has chaired various marketing groups. He can be reached at Justin@vadatech.com.


Table 8-2 Recommended EMC test cases based on FRU type

| EMC | Test Cases | Backplane | AC/DC Power Unit or Unit containing PUPS | Unit Containing Copper I/O | Unit With No Copper I/O | Fan Unit | Unit Containing User Interface (i.e. switch) | |
|--------------------------|--|--|--|----------------------------|-------------------------|----------|--|-----|
| | | | | | | | | |
| Emissions Specifications | Radiated Emissions | Electric Field | Shall | Should | Shall | Shall | Shall | |
| | | Magnetic Field | Should | Should | Should | Should | Should | |
| | Conducted Emissions | Signal Leads | N/A | N/A | Shall | N/A | N/A | N/A |
| | | Power Leads | N/A | Shall | N/A | N/A | N/A | N/A |
| | AC Leads Current Harmonics ^a | N/A | Shall | N/A | N/A | N/A | N/A | |
| | AC Leads Voltage Fluctuations ^a | N/A | Shall | N/A | N/A | N/A | N/A | |
| Immunity Specifications | Radiated Immunity | Electric Field | Should | Should | Should | Should | Should | |
| | | Magnetic Field ^b | N/A | N/A | N/A | N/A | N/A | |
| | Conducted Immunity | Signal Leads | N/A | N/A | Shall | N/A | N/A | |
| | | Power Leads | N/A | Shall | Should | Should | N/A | |
| | ESD | ESD | N/A | Should | Shall | Should | Should | |
| | EFT | Power Leads | N/A | Shall | Should | Should | N/A | |
| | | Signal leads | N/A | N/A | Shall | N/A | N/A | |
| | Surges | Power Leads | N/A | Shall | N/A | N/A | N/A | |
| | | Signal Leads | N/A | N/A | Shall | N/A | N/A | |
| | DIPs | AC Power Dips and interruptions ^a | N/A | N/A | N/A | N/A | N/A | |

a. Europe Only
b. H-Field Sensitive devices only

FIGURE 3: The table shows the MicroTCA.0 specification’s recommendation for EMC test cases based on Field Replaceable Unit (FRU) type.

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Defending Ethernet Ports from Electrical Transient Events

TIMOTHY PULS

Product Marketing Manager
Semtech Corporation

ETHERNET is ubiquitous. From base station backhaul, to wireless access points, to IP surveillance cameras – Ethernet is found everywhere. And, the devices enabling this Ethernet traffic – the miniature transceiver ICs driving the communications infrastructure – are more advanced than ever before. Before 2010, Ethernet physical-layer transceivers (PHYs) were based on 90-nanometer IC technology. Today, the market has strongly adopted higher performance 65-nanometer PHYs with a plan toward 45-nanometer and below. While the newer PHY platforms give system designers exciting performance advantages, there is a menacing side effect felt by the EMC community – reduced on-chip ESD protection levels.

The mantra of the IC world – smaller is better – means chip manufacturers confront new trade-offs. As IC technology leaps forward to achieve aggressive die size and

performance targets, the protection clamps at the chip I/O are often compromised. This, of course, is not without impact to the system level robustness of the transceiver interface.

While chip manufacturers are squeezed by the physical constraints of implementing protection on the chip, the system designer is likewise squeezed with the challenge of engineering an end product that will prove robust against the many electrical transient threats encountered by the end product. And, the system-level transient immunity standards are not easing. Quite the contrary – more stringent requirements are emerging.

SYSTEM LEVEL TRANSIENT THREATS

In years past, protection circuitry was something of an afterthought in the design cycle. Today, few debate the necessity of external protection arrays, and increasingly designers appreciate the value of a well-conceived circuit protection plan on the front end of the design phase.

This is especially true on Ethernet ports. The racks of twisted-pair cable within the network infrastructure need a resilient defense against a variety of transient over-voltage threats – electrostatic discharge (ESD), cable discharge (CDE), electrical fast transients (EFT) and, of course, highly destructive lightning surges.

The goal of a good protection scheme has two parts. First, the protection must safeguard the PHY from the transient threats encountered. Secondly – and maybe

more challenging – the protection circuit should be benign with respect to the signal transmission of the link. As the landscape has changed from Fast Ethernet to Gigabit Ethernet to 10Gigabit Ethernet, this is now a more challenging proposition.

A good defense must take into account the characteristics of the threats. At a most basic level, transient threats can be divided into two broad categories: *fast rise-time* threats and *slow rise-time* threats. The way in which these spikes couple into ports and onto PCB traces can be quite different, and the type of components needed to arrest them can be different.

ESD, CDE (Cable Discharge) and EFT (Electrical Fast Transients) are *fast rise-time events*; they have a rise-time on the order of 1 nanosecond (often less than 1 nanosecond). For the purposes of this discussion, we categorize these three events broadly as fast rise-time transients, but it is worth noting that these transients behave somewhat differently. The energy within a CDE strike or an EFT burst can prove more cumbersome to tame than an ESD event generated by human contact. The top row of table 1 highlights some notable differences in these pulse characteristics.

The second class of transient threat is the surge threat. Surge events are slow rise-time lightning induced pulses. These waveshapes are generally microsecond events. They have slow rise times compared to ESD, CDE and EFT, but present orders of magnitude higher power in the pulse shape.

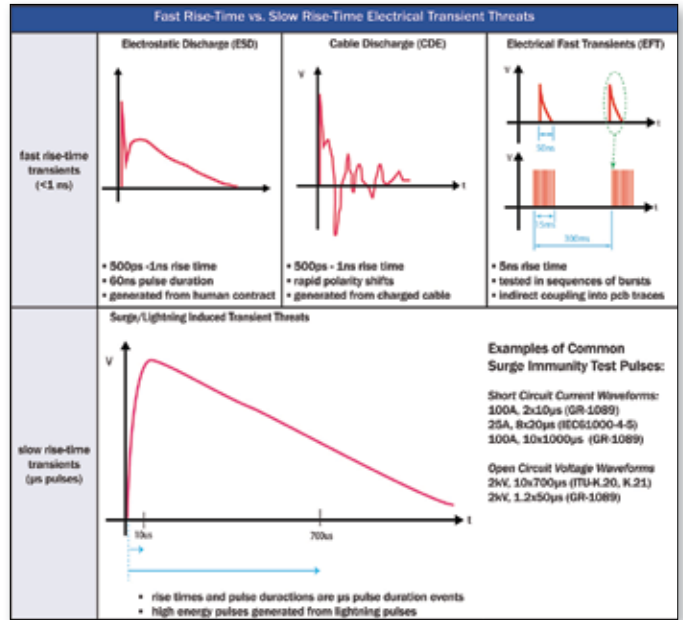


TABLE 1: Characteristics of Common Transient Threats

Experts in the Field...

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$R = 2d^2/\lambda$

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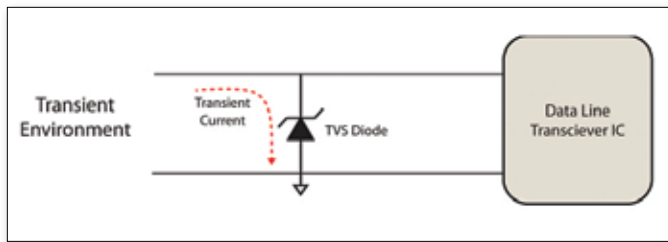


FIGURE 1: TVS Device as a Shunt Protection Element.

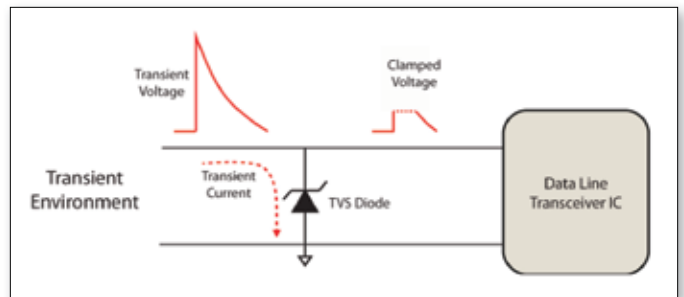


FIGURE 2: Generic Transient Clamping Response of TVS Diode.

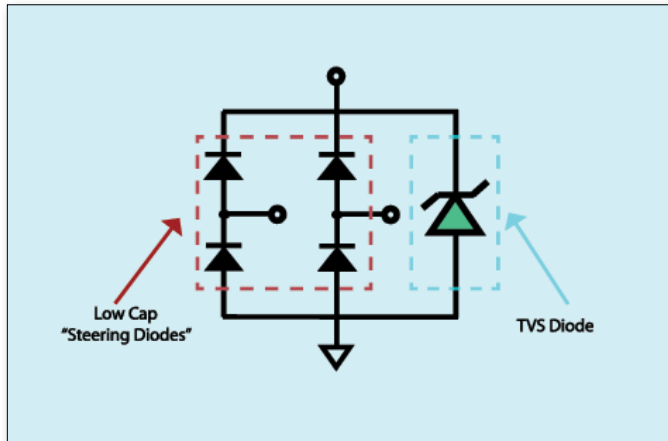


FIGURE 2: "Rail Clamp" Low-capacitance TVS Architecture.

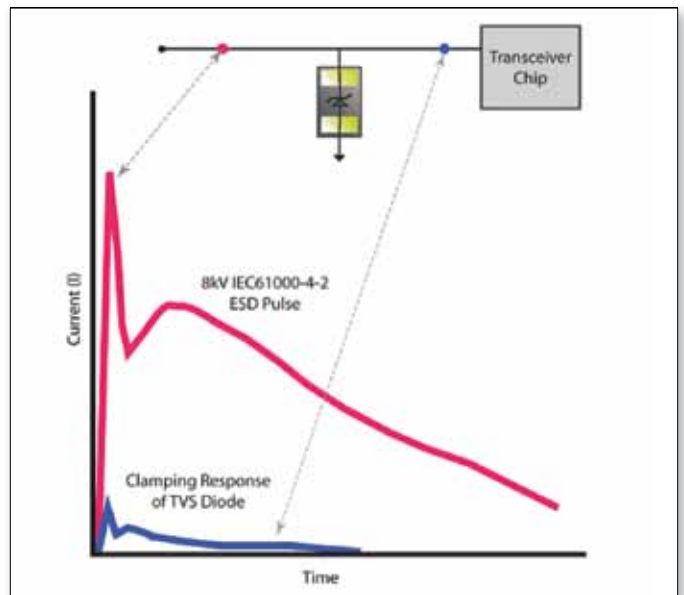


FIGURE 3: ESD Clamping Response of TVS Diode.

They can be defined as either a voltage waveform with a peak voltage or a current waveform with a peak pulse current. In segments of the telecom market, end equipment manufacturers may demand very high levels of immunity from lightning induced threats. The bottom row of table 1 shows some common test pulses used to show immunity to lightning induced surge.

TRANSIENT VOLTAGE SUPPRESSION (TVS) ARRAYS

The challenge in protecting Ethernet ports is that the end equipment may be exposed to all these different transient types. Thus, it demands versatility out of a protection structure. Where yesterday’s system designers could choose from a variety of low-end circuit protection components, today’s systems require a bit more care and attention in selecting an optimized solution.

Due to their low voltage breakdown, fast response time, and low clamping voltages, Transient Voltage Suppression (TVS) diodes offer some unique advantage for safeguarding low-voltage Ethernet lines against a range of transient threats. Other components can be used, of course, but at some level a TVS device is likely required.

HOW TVS DIODES WORK

TVS diodes are overvoltage protection elements that connect as shunt devices across a data line (Figure 1). Under normal signaling conditions a TVS diode presents high impedance. The TVS device has a rated capacitance and a rated leakage current typically measured at 0V and the device working voltage respectively. These parameters should be

chosen appropriately for the speed of the signal interface and also sufficiently minimized such that the TVS diode appears “transparent” to the circuit during normal operation.

When a transient spike hits the port the TVS diode acts like a “trap door” to ground for the transient current. The diode junction achieves breakdown and becomes a low impedance shunt path to sink dangerous current through the diode junction. An effective protection circuit diverts this transient current and clamps the transient voltage spike to a level below the failure threshold of the protected IC.

Especially for the fast rise-time events (ESD and cable discharge) the diode junction must breakdown at a low voltage threshold to engage the transient during the initial inductive spike. In the case of lightning the TVS junction must absorb the high surge currents. As such, the TVS junctions are larger for a lightning rated device.

For silicon TVS junctions, there is a trade-off between the current handling of the device and the capacitance. As a basic rule, the higher the value for the max peak pulse (Ipp) rating of a TVS part, the higher the capacitance of that device. And, conversely, a device with a low capacitance generally correlates to weaker surge absorption.

On Ethernet lines, the device must present a robust surge rating without introducing an excessive capacitance load that

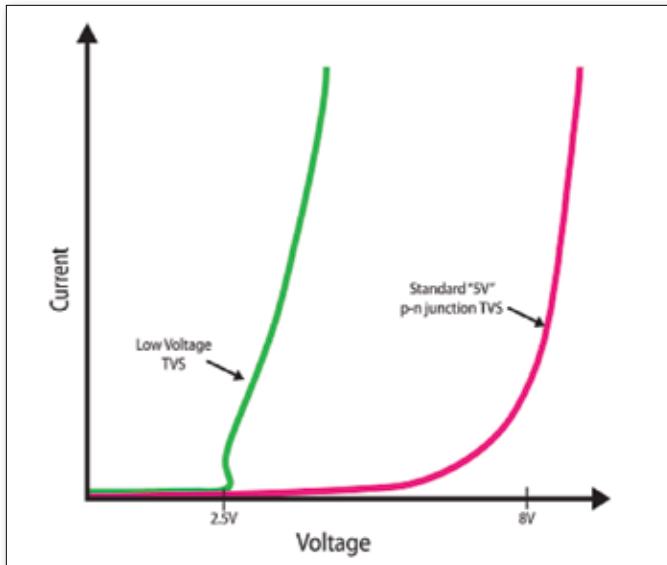


FIGURE 4: IV Curve Comparison: Low Voltage TVS & Standard “5V” TVS.

will disturb signal quality. TVS arrays can achieve such high-surge immunity and a low capacitance with a “rail clamp” diode architecture. By bridging a TVS diode with very low capacitance “steering diodes,” the effective capacitance of the TVS array can be minimized while also upholding the surge rating (Figure 2).

CLAMPING VOLTAGE

In evaluating how well a protection array is “protecting” the clamping voltage must be considered. The clamping voltage is the voltage resulting after the TVS device has clamped the incoming surge transient. (See figure 2) This “clamped voltage” will appear at the PHY input. Obviously, it should be minimized. The lower the transient voltage is clamped, the better the protection margin. It is here where the TVS selection makes all the difference.

A device with a lower working voltage can help. This is the normal dc operating voltage of the TVS. Below the working voltage the TVS device is a high impedance element. Just above the working voltage the TVS begins to conduct current. For optimal protection, it is preferable to choose devices with a low working voltage. As an example, for Gigabit Ethernet ports where the differential signal swing may be just under 2V, a TVS with a working voltage of 2.5V will typically have some clamping advantages over a device with 6V working voltage. The lower working voltage allows the TVS to arrest the voltage spike at a lower voltage threshold and in theory respond faster.

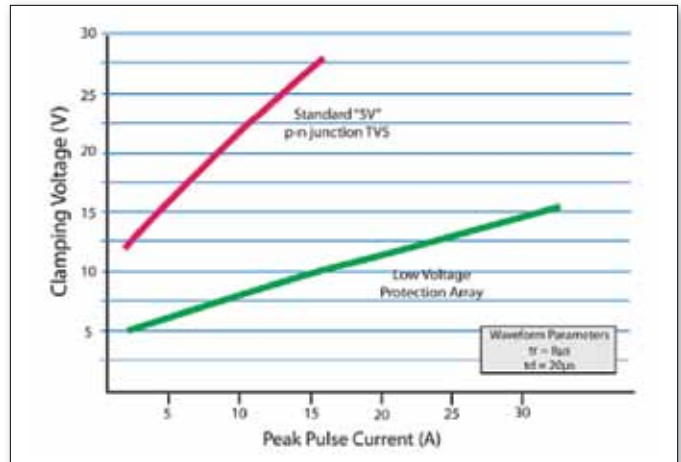


FIGURE 5: 8x20µs Surge Clamping Comparison.

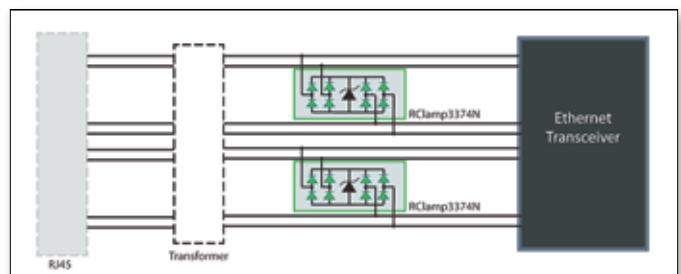


FIGURE 6: RClamp3374N Flow-through Protection for Gigabit Ethernet.

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Additionally, a TVS with a “snap back” I-V characteristic can also bring some advantage. In this case, there is a slight negative resistance in the I-V curve. This yields steeper I-V curve, which, in turn, can help lower the clamping voltage at the peak pulse current (see Figure 3).

TVS clamping voltage for a lightning condition is often benchmarked using an 8x20 μ s current pulse. The following 8x20 μ s clamping voltage curve illustrates the divergence of differing TVS devices in clamping voltage. As the silicon

PHY scaling continues leading to more sensitive IC interfaces standard 5V zener arrays are hardly suited to protect high-end Ethernet systems. Instead, low working and low clamping voltage are needed.

CIRCUIT PROTECTION IMPLEMENTATION

Finally, the question frequently arises as to where the protection devices should be implemented. Is it better to place the protection on the line side closer to the boundary of the port? Or is it better to place the protection on the PHY side behind the Ethernet magnetics? There are certainly good reasons for choosing either. Yet, for most immunity conditions, the advantages to protecting on the PHY side of the Ethernet magnetics outweigh the advantages to protecting on the line side. One of the key reasons for PHY side protection is that for most surge events, the transformer provides some level of attenuation to the surge event. Thus the pulse is reduced somewhat on the PHY side of the interface – though it is still an extremely dangerous surge. Placing TVS components on the PHY side takes advantage of whatever action the transformer core saturation is providing against the surge.

CONCLUSION

The Ethernet ports in today’s networking landscape are more sensitive than any other previous time within the industry. Power efficient, highly miniaturized Ethernet PHYs increasingly need advanced transient voltage protection circuits to safeguard against a host of transient threats. With some forethought at the outset of the design phase, TVS diodes can be effectively implemented to safeguard Ethernet-based systems from the many transient voltage threats encountered at the system level.


ABOUT THE AUTHOR

Tim Puls is a product marketing manager for protection products at Semtech. Previously, he worked as a field sales engineer with National Semiconductor and in application engineering for Texas Instruments. He holds a bachelor’s in electrical engineering from Texas A&M University. He can be reached at tpuls@semtech.com.


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A National Plan for EMP Protection

Part 1

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Future Science

1. ARTICLE OVERVIEW

T HIS ARTICLE HAS TWO PARTS.

It begins with a brief EMP historical review demonstrating the field strength threat that must be shielded against in order to assure survival of electrical and electronic items and systems, and the retention of our modern lifestyle.

Next comes planning, protection options, installation, test and certification, cost, financing and development of new products, services and markets – an ambitious scope.

In Part 1 of this article, a national program is offered in two phases to make EMP protection viable: Phase 1 is a two-year pilot design and installation of EMP protection of a few villages and towns. From lessons learned, Phase 2 is an eight-year, follow up with installation, test and certification tailored to several selected economic levels and coastal/inland locations as well as various latitudes. Structures range from individual

sheds and homes to office buildings, shopping malls, hotels, industrial parks and warehouses, public works and hospitals.

To ensure timely replenishment, products from areas outside of the EMP event are shipped to all EMP protected towns that have railroad sidings, a 4,000 foot dirt-mat runway, and/or an expanded marina, as applicable. They support the offloading and provide local distribution arrangements.

In Part 2 of this article, entitled, EMP Protection of Buildings, protection detail is addressed. This includes shielding of buildings, via shield options, shield bonding, grounding, cable surge suppression and filtering. A significant lowering in cost develops from savings in shielding a new structure vs. retrofitting existing buildings.

Solar rooftop costs are projected to achieve parity with the electric grid in kWhr cost before the end of the present decade. This encourages rapid EMP protection expansion, hopefully, before the first EMP event strikes. In addition, the existence of widespread EMP protection dramatically reduces the chances of experiencing an EMP attack in the first place.

The last section of this article presents a summary of new products and services created, their markets and the resulting millions of jobs that will be developed.

2. HISTORICAL EMP SUMMARY

This article is concerned with a particular type of electromagnetic pulse (EMP), specifically high-altitude nuclear EMP. Although much of the history of high-altitude nuclear EMP remains classified, the unique charac-

teristics of high-altitude nuclear EMP were apparently not foreseen by anyone in the scientific and engineering community.

The effects of *low*-altitude nuclear EMP, however, were foreseen by Enrico Fermi prior to the very first nuclear test in 1945. As a result of Fermi's foresight, all of the lines leading to electronic recording instruments were carefully shielded. Nevertheless, much information was lost because of the intensity of the EMP close to a nuclear explosion.

By the time of the first *high*-altitude nuclear explosions, Fermi had died and the other great physicists of the time expected the EMP from a high-altitude detonation to operate under the same basic mechanism as a low-altitude detonation.

The first openly available account of a high-altitude nuclear EMP is from the helium balloon lofted Hardtack-Yucca test of a 1.7 kiloton nuclear device over the Pacific Ocean on April 28, 1958.

The EMP from that test was a pulse that was five times the oscilloscope limits at most locations. The electric field was initially a positive-going pulse rather than the expected negative pulse. The EMP was principally horizontally polarized rather than the expected vertical polarization. Since the facts did not agree with the accepted theory of the time, the results were dismissed as possibly a wave propagation anomaly.

In July of 1962, a higher yield detonation at a much higher altitude made its effects known in a much more dramatic fashion that proved conclusively that previous theories of high-altitude nuclear EMP generation were wrong. That test was the Starfish Prime test over Johnston Island in the Pacific.

Because of its proximity to Hawaii (about 900 miles away) it was necessary to announce the time and location of the Starfish Prime test to the public. Many were watching the detonation under cloudy skies over the Pacific as 300 streetlights in Honolulu were abruptly extinguished, many burglar alarms went off and a microwave telephone link to the Hawaiian island of Kauai suddenly went dead.

Although the intensity of the EMP from Starfish Prime caught scientists completely by surprise, and resulted in very little in the way of useful EMP measurements, they were more

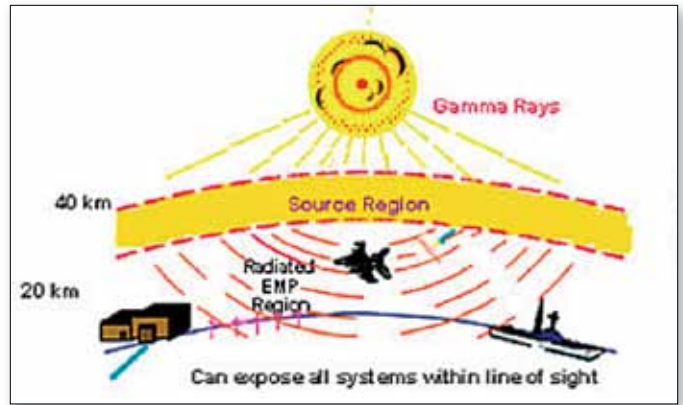


FIGURE 1: The E1 pulse, which is the first wave of high-altitude nuclear EMP energy, is generated in the mid-stratosphere when the atoms there are hit by a pulse of gamma radiation and are acted upon by the earth's magnetic field to cause a burst of extremely high-intensity electromagnetic radiation. (Illustration is from the United States Defense Threat Reduction Agency.)

prepared for the subsequent high-altitude tests of 1962.

Finally, in the Bluegill Triple Prime and Kingfish high altitude nuclear tests of October and November 1962, the scientists were ready for this previously unexpected phenomenon, and accurate EMP records were obtained.

The Soviet Union also had their share of EMP problems during their 1962 high-altitude tests over Kazakhstan (which was then a Soviet Republic). In a high-altitude test of October 22, 1962 over central Kazakhstan, and a carefully monitored 570-kilometer telephone line was shut down, a shallow buried 1000-kilometer power cable was shut down (along with a fire in the power plant feeding the line). Also, arcing across some porcelain insulators on overhead power lines caused the insulators to break, and consequently, some power lines fell to the ground.

In 1963, Los Alamos physicist Conrad Longmire was shown the EMP results of the high-altitude testing and finally figured out the mechanism that was generating the surprisingly large EMP.

There were two factors that had been largely ignored by physicists previously. One was the large effect of the interaction of the earth's magnetic field during high-altitude EMP. The other factor was the coherence of the pulse caused by enormous amounts of gamma rays hitting the upper atmosphere at almost exactly the same time. This coherence resulted in most of the first wave of EMP energy being concentrated into a very narrow pulse of very high amplitude.

3. THREAT AWARENESS AND THE FIELD STRENGTH TO SHIELD AGAINST

The blue 'pre-ionization' curve in Figure 2 applies where gamma and X-rays from the weapon's primary stage ionizes the atmosphere, making it electrically conductive before the main pulse from the thermonuclear stage. The pre-ionization can prevent the formation of part of the EMP from the secondary explosion.

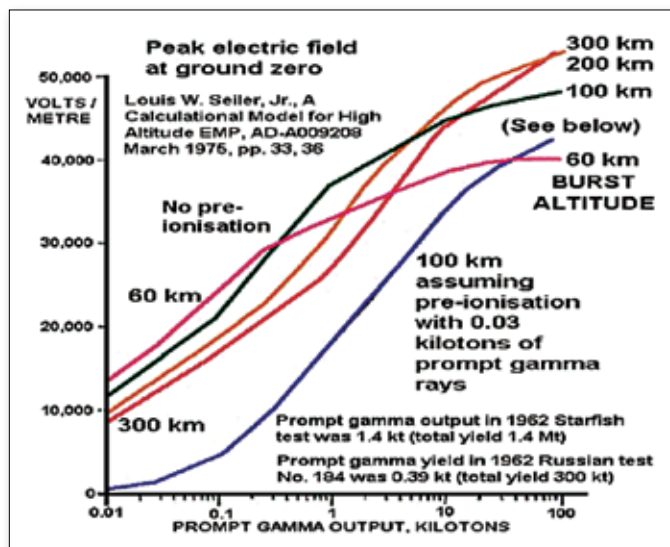


FIGURE 2: EMP Peak Electric Field

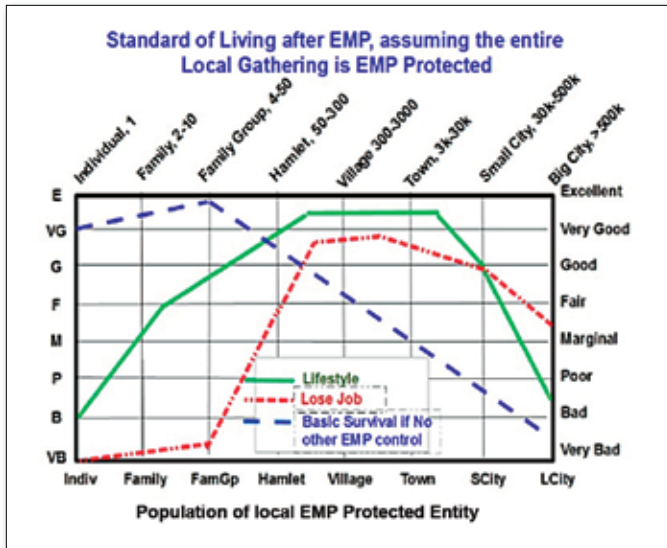


FIGURE 3: Standard of Living after an EMP burst, assuming the entire local gathering is also EMP protected.

Figure 2 shows how the peak EMP radiated field strength reaching the ground varies with the weapon yield and burst altitude. Note that the yield here is the prompt gamma ray output measured in kilotons. For known nuclear weapons, this varies from 0.1-0.5% of the total weapon yield, depend-

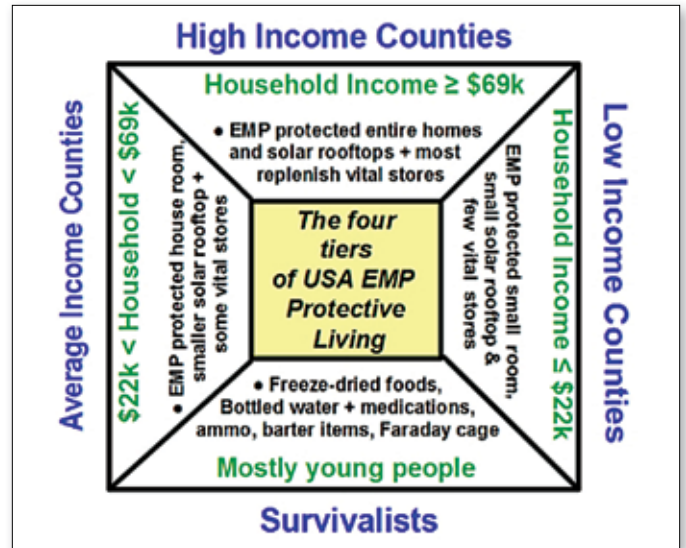


FIGURE 4: Four - Tier EMP Protection Concept

ing on weapon design. The 1.4 megaton total yield of the 1962 Starfish test had an gamma radiation output of 0.1%; therefore, 1.4 kiloton of prompt gamma rays.

Figure 2 also shows that the ground-based electric-field strength approximates 50 kV/m, a value used in MIL-STD-461E and below for calculating the 80-dB shielding effectiveness recommended for EMP protection described below. This does not mean that every shield must provide 80 dB as it may happen from two or three layers of shielding and/or partial radiation blocking from other obstacles.

One must realize that most electronic devices were tested for a field strength of 10 V/m or other specifications pursuant to MIL-STD-461 RE-105, European Union EN61000-4-3 or other international radiated susceptibility limits, to show no malfunctioning or undesirable response. Thus, an EMP threat has a 50,000 /10 volts per meter or 5,000 times more severe shielding required to comply.

One default value is that $20 \cdot \log_{10}(5,000) = 74$ dB or more shielding is generally needed for EMP compliance. Frequently, a factor of 2 (6dB) is added for safety margin. This suggests that 80 dB shielding is needed to ensure EMP immunity. Details are shown in Section 10. Again, remember that another intervening housing rack, cabinet, room or whatever else may reduce this number.

4. A NATIONAL EMP-PROTECTION PLAN

Although the U.S. government has EMP-hardened ("hardened" is military vernacular for protected) the military sector, intelligence community and other selected office buildings, essentially nothing has been done in the civil sector of residential, commercial, industrial, and public utilities. This seems ironic since employees of DOD (Department of Defense), DHS, DOE, DOT and others, nearly all live off premises, shop in malls, shop pharmacies, buy gasoline and other products from EMP unprotected facilities. Thus, the U.S. remains unprotected from an EMP burst.

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The Senate Committee on Homeland Security and other pro-EMP protection organizations are perceived by many to be frustrated from lack of timely U.S. EMP protection actions. Therefore, this section addresses a few examples of strategies, tactics, planning and implementation options. The matter of post-EMP lifestyle is a major consideration not addressed in the Internet with few exceptions.

Post-EMP lifestyle is compared and contrasted with pre-EMP lifestyle. While EMP survivalists plan to move out to the country, storing water, 25-year shelf-life freeze-dried food, medications, guns, ammo and barter items, they fail the lifestyle test. On the first day of the EMP event, they lose their job, die from failure of the dialysis machine, lack of gasoline and scores of certain provisions. Their focus, however, is surviving, defined as a bridge from a disaster to the day things are “restored.” However, after an EMP event, lifestyle may never be restored within their lifetimes.

Other interim lifestyle options may be offered at HOA (Home Owners Associations), developments, hamlet, village and town levels for EMP protection. This begins to fail at the city levels, where survival crimes increase manifold. This is due to highrise structure limitations; the starving are stalking the survivalists for their own surviving, since goods replenishment severely lags need in bigger cities.

How does all this happen?

Just how does the Survivalist score, when compared to other EMP-protection options. Figure 3 suggest three elements of many comparisons.

The surviving group size from an individual to a large city is displayed as the horizontal axis. A value judgment is shown for the vertical axis. It ranges from excellent to very bad. Of course, most value judgments are in the eyes of the beholders (like lifestyle, per se), while others are absolute, like losing your job.

Figure 3 shows that basic surviving is scored very good compared to no other EMP protection. It scores particularly bad in the big city since there is a plethora of starving people ready to break into the homes of anyone storing food. That's why survivalists prefer to move to the country when an EMP event happens.

Figure 3 also shows that one major disadvantage of the EMP survivalists is that he loses his job after an event since nothing else is working anyway. However, if a village or town were EMP protected, and almost all employment is geared to the local events of a city, job retention may approximate 90% after an event. In fact it could exceed 100% if the town is a manufacturer or it develops products or services in demand from unprotected neighboring areas struck by the same EMP event.

5. PHASE-1 SELECTION & PILOT PROTECTION OF VILLAGES AND TOWNS

5.1- The Concept of a Four-Tier, National EMP Protection Plan

Lifestyle is rarely addressed in EMP protection literature. Does it not matter? Yet, EMP survivalist will lead a very different lifestyle vs. those in a whole village or town that is nearly

| A | B | C | D |
|----------------------|--------------------|-----------------|--------------------|
| Buildings and Topics | Hi-Income Counties | Median Counties | Lo-Income Counties |
| Shopping Malls | X | X | |
| Wal-Mart | X | X | |
| Vehicles | X | X | |
| Food Stores | X | X | X |
| EMS Services | X | X | |
| Pharmacies | X | X | X |
| Adjacent Farms | X | X | X |
| Water Utilities | X | | |
| Gas Stations | X | X | |
| Airport-Trains | X | X | |
| Manufacturing | X | | |
| Hospitals | X | | |
| Clinics | X | X | X |
| Weapons-Ammo | X | | |
| Boats-Ships* | X | X | |
| Marinas* | X | | |
| Commerc. Office | X | X | |
| Home Depot, - Lowes | X | | |
| Ace Hardware | X | X | X |
| Hotels/Motels | X | | |
| Schools-College | X | X | |
| Funeral Services | X | X | |
| Churches | X | X | |
| Restaurants | X | | |
| Theaters | X | | |

FIGURE 5: Identification of Principal Resources for Survival and Living Needs

completely EMP protected. For example, following an EMP event, the EMP survivalists individual (or family) loses his job, loses access to shopping stores, hospitals, dentist, undertaker, etc. that have all become dysfunctional. Contrast this to an EMP-protected municipality in which almost nothing is lost except uncertainty of when the EMP-protected replenishment vehicles, airstrip or railroad siding may be revisited with more replenishments. Even here, a warehouse can store survivalists freeze-dried and selected canned food, principal medications, etc. These matters lead to the reason why different tiers of EMP protection are addressed as one strategy of several.

There are four tiers of EMP protection to be initiated herein in order to get things started. Except for EMP survivalists, who have started their planning and implementing years ago, the top three tiers may initially be regarded as Phase-1 pilot programs, from which a substantial pragmatic learning experience develops.

They are started at the same time and have been selected by location and economy as discussed later. Each tier advisory group has a representative of the other two tiers plus an EMP survivalist, a county Economic Development office participant, and a Chamber of Commerce person since all learn from the progress, failures and wisdom of each other. Also,

as discussed later, financing comes from issuing county and corporate bonds.

The 3,140 counties in the U.S. are divided into four quartiles of median household income (Fig. 4, data from 2010 census): (1) Tier-1, highest quartile (25% of total U.S. households earn more than \$69,000/annum), (2) Tier-2, median quartiles (2nd and 3rd quartiles earn between \$22,000 and \$69,000/annum with \$39,000/annum being their geometric midpoint), and (3) Tier-3, lower quartile, 25% of the total U.S. county households earn less than \$22,000 per year.

The master plan also provides for north and south (different latitude) locations and three geographical regions in the U.S. to be similar in the four-tier EMP protections. This allows for coastal U.S. exposures, coastal-inland and central regions in order to gain information different from each other's location.

The diagram, Fig. 4, illustrates the four tiers of EMP protection. Their assigned names are located at the outer periphery of the four-sides of the square. Just inside the square, the cor-

responding household income range is listed. As mentioned, Tier-1 counties can afford greater (full) EMP protection and Tier-3 less. Of course, there is allowance for exceptions, not discussed here. One example is that many counties will have poorer sections among the wealthier section locations within a single county.

Figure 4 also has a three-line brief (shown in black), closest to the center square, to suggest what is covered in their respective tiers. A few details of these remarks are described in the next section.

The following discussion addresses some information about the first Tier-1, High Income Homes, Commercial and Other Buildings. The others are beyond the scope of this article for space reasons.

There are 91 million homes in the U.S. and 39 million apartments to shelter it's 314 million population (year 2012). For Phase-1, two-year pilot program, a town of about 10,000 population is selected for the first tier. With an average household size of 2.6 people, this corresponds to $10,000/2.6 = 3,850$ households. Of these, 2,700 are detached homes and 1,150 are apartments. Therefore, at the end of Phase-1, about 3 locations x 3,850 = 11.6 thousand Tier-1 homes will be EMP protected. Parenthetically, assuming Phase-2 is completed eight years later, up to 23 million Tier-1 homes in all of the U.S. will be EMP protected with new jobs running into the millions.

Since average new home and new commercial building construction is estimated to be 2.5% per year, Tier-1 site, $0.025 \times$

| A | B | C | D | E | F | G | H |
|-----------------|------------|---------------|--------|---------|----------|----------------|-----------|
| Tier & Location | Population | US Population | Home # | Cost \$ | Home \$M | Commercial \$M | Total \$M |
| Tier 1, East | 10,000 | 0.0032% | 2,700 | 55,000 | 149 | 238 | 386 |
| Tier 1, Central | 10,000 | 0.0032% | 2,700 | 55,000 | 149 | 238 | 386 |
| Tier 1, West | 10,000 | 0.0032% | 2,700 | 55,000 | 149 | 238 | 386 |
| Tier 1, East | 1,000 | 0.0003% | 270 | 55,000 | 15 | 24 | 39 |
| Tier 1, Central | 1,000 | 0.0003% | 270 | 55,000 | 15 | 24 | 39 |
| Tier 1, West | 1,000 | 0.0003% | 270 | 55,000 | 15 | 24 | 39 |
| Tier 2, East | 1,000 | 0.0003% | 270 | 12,000 | 3 | 5 | 8 |
| Tier 2, Central | 1,000 | 0.0003% | 270 | 12,000 | 3 | 5 | 8 |
| Tier 2, West | 1,000 | 0.0003% | 270 | 12,000 | 3 | 5 | 8 |
| Tier 3, East | 1,000 | 0.0003% | 270 | 4,000 | 1 | 2 | 3 |
| Tier 3, Central | 1,000 | 0.0003% | 270 | 4,000 | 1 | 2 | 3 |
| Tier 3, West | 1,000 | 0.0003% | 270 | 4,000 | 1 | 2 | 3 |
| Totals: | 39,000 | 0.0124% | 10,530 | | 503 | 805 | 1,308 |

FIGURE 6: Summary of general EMP tier classification and assignment

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3,850 = 96 new Tier-1 homes per year will be added per site. This is mentioned now to inform the reader that EMP protection for new home construction is estimated to cost about 65% of that for a retrofit home, since EMP protection is more easily and economically achieved on a new home construction.

Home EMP protection in Tier-1 involves a 100% shielding of the outside skin (including the floor), some details for achievement of which are provided in later sections. The shielding is bonded and grounded to earth and any lead-in power lines and others (telephone, data) are filtered and surge suppressed as also presented in later sections.

The low end of home size in the high income counties is roughly 4,000 sq. ft. (372 sq. meters) under air. The power required for a solar rooftop is about 10 kW. This is sufficient to handle air conditioning, and hot water loads in addition to the electrical appliances, lighting, computer and peripherals, radio and TV, etc. Of course, the solar rooftop is also shielded and processed as explained in a later section.

Along with the solar rooftop is both a battery bank of about 30, 12-volt deep-cycle lead-acid batteries. They provide an energy capacity of about 30 kwh (kilowatt hours), nominally sufficient to handle all night time use and a few overcast days when solar electricity is nearly unproductive. As explained later, the number of batteries is adjusted for greater latitudes and climates having more overcast days.

The cost for a high income county, EMP protected home with protected solar rooftop will range from about \$50,000 to over \$100,000 for large homes over 10,000 sq. ft. (929 sq. m). Ignoring inflation, this will be reduced by about 30-40% in 10 years by Moore's Law for electronics and by quantity production cost reduction. (Moore's Law is the engineering dictum that, among other things, describes the cost reduction of semi-conductor products over time.)

Figure 5 wording speaks of "Larger retail replenishing stores." Focus on Column B for the present. Scan down the list of facilities that will have been EMP hardened. Note that nearly everything has been

protected so that the affluent town as a whole is nearly unaware of an EMP incident. The reason that the word "nearly" is used is that communication and transportation of delivery vehicles, delivering replenishment food, medications and other is essential to survival. This requires that some modes of communication such as satellite and fiber optics are functional. Also, all Tier-1 communities have at least a 4,000 foot metal-mat runway to help ensure vitals replenishment. Space restrictions in this article do not permit discussing the other three tiers here: (1) Column C, medium income counties, (2) Column D, low-income counties and (3) EMP survivalists .

6. PHASE 2, 8-YEAR EMP PROTECTION IMPLEMENTATION AND EXPECTATIONS

Phase 2 of the proposed National EMP Protection Plan is the follow up of Phase 1 as it is the implementation thereof. Phase 2 lasts for eight years after Phase 1. Both will be graphed later regarding expenses, growth and job generation expectations.

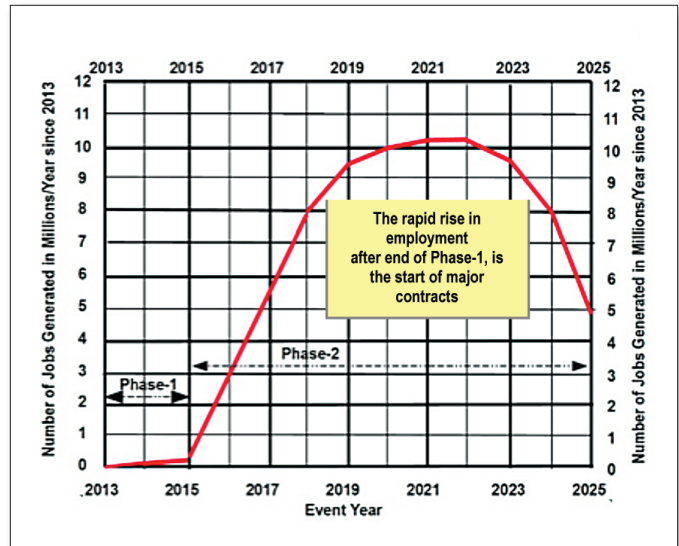


FIGURE 4: Fig. 7 – Cumulative Jobs Generated in Millions since 2013.

Remember that Phase 1 had a design and development team at each of the pilot 12 villages and towns at the county level. Near continuous feedback among all entities takes place to ensure (1) not repeating things that work poorly, plus rationale and (2) emphasizing, in a timely manner, those that work well. This is pragmatism at its best. Further, each tier can learn from a higher (or lower number) tier for possible sectors to EMP protect, along with rationale and cost.

Meanwhile a consumer EMP protection guide was under development in Phase 1 and many seminars are taught at different levels to ensure timely awareness, and how-to actions and events. Once a week a broader webinar is orchestrated for both the 12 EMP villages and towns to participate and for others looking on who may be anxious to participate during Phase 2.

Implementing Phase 2 requires significant training in all facets as the implementation involves roughly 500 times the Phase 1 cost and activities, but spread over eight years. Especially significant is the generation and refinement in mass production of the solar rooftop installation and solar panels and inverter production, all with built-in shielding and surge suppression.

Detail discussion of Phase 2 is deferred here as emphasis shifts over to physical realizability, costs, new products and services, markets and job creation.

7. A PEEK AT NEW PRODUCTS, SERVICES, MARKETS AND JOBS

This section gives the readers a peek at expectations regarding costs and jobs, first for Phase-1, EMP-Solar, Pilot Project (experiment or study). Then, when carried through Phase 2 - the entire U.S. by 2023.

Figure 6, in a spreadsheet form, gives a glimpse of the various element data and their totals on the bottom line. (Regretably, space does not permit the development of the data here.) Column B is the customer town or village population involved and Column C is the corresponding population in percent relative to the entire U.S. population of 314 million as of 2012. Column D is the approximate

number of homes involved and E is their rough cost per average home. Column F is the total home cost in units of million dollars (M) for the Tier and location shown in Column A.

The electric utility industry reports that 38% of their electricity load (users) are residential and 62% is a combination of commercial plus industrial. The latter is $6\% \div 8 = 1.6$ times the residential load. So, Column G is 1.6 times the amount of column F. Finally, Column H is a total of both Columns F and G. Remember, the numbers here are rough

since there are many expenses and variables involved and the lower cost of government participation and support has not yet been added.

Figure 7 shows that the cost for Phase-1 over the first two years is about \$1.3 billion (total at bottom right in column H). This is spread over 12 counties with the first three, each serving a town population of 10,000 which is the highest cost at about \$386 million. The average population of all 3,140 U.S. counties is (\$314 million U.S./3,140 counties) = about 100,000 people/county. Their estimated net worth (according to the U.S. census) is about \$55 trillion/3,140 counties = an average of \$17 billion/county. Highest income counties may approximate \$40 billion and the lower income about \$4B. For a high-income county of 100,000 population, \$40B net worth corresponds to \$400,000 per person.

The \$386 M of Column H, town in Fig. 7 is spread over a 100,000 county population and amounts to about \$3,800 per person. However, this is not relevant since, as mentioned earlier, the money comes from the issuance of county and corporate bonds from investors, retirement funds, and annuities. From the previous paragraph, \$3,800 is less than 1% of the county per capita wealth; so this is no financial challenge (in other words, it is readily affordable).

Regarding jobs, the \$1.3 billion pilot, Phase-1 cost (bottom line, Fig. 7, Column H) is the total direct cost exclusive of government participation. Thirty per cent (30%) is arbitrarily added to account for government participation cost, some volunteer time contributed, publicity and education costs, plus items not identified in Fig. 7. So the \$1.3 billion becomes roughly \$1.7 billion cost for Phase-1.

Since \$225,000 of money spent back into a U.S. economy corresponds to one new job created (at \$48,000 avg. annual salary), the number of jobs created from Phase-1 is $\$1.7B/\$225k = 7,600$ job-years (see Fig. 7). Because this is spread over two years, this represents 3,800 jobs lasting for two years. For the entire U.S., this will approximate the above $(7,600 \cdot 0.000124)$ or $(Jobs/Total, Col. C, Fig. 6) = 61$ million job-years, or averaged over 8 years = 7.6 million U.S. jobs.

The above financial information is admittedly rough, but adequate to get a first order evaluation of the financial doability of Phase-1 and Phase-2.

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posed National Plan for EMP Protecting the U.S. Part 2 of the article presents methods and techniques for EMP protection of buildings, solar rooftops and other structures. As such, Part 2 covers details of shielding, bonding, grounding, and cable or device surge suppression and filtering. These apply to structures from sheds and rooms to small and large homes, and to commercial and industrial buildings less than about five floors in height.

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Emanuelson is the leading EMP Internet author with scores of EMP related subjects. He is a former member of IEEE Broadcast Society, and is now part-time electronics consultant and a part-time non-fiction science writer.

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Charge Generation of ESD Sensitive Devices: Understanding Risks of Protective Packaging

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SEVERAL YEARS AGO, Ray Gompf, Ph.D., PE (Ret.), NASA, Kennedy Space Center and the author evaluated 7" x 7" ESD corrugated, Kraft and bleached B-Flute corrugated substrates for Tribocharge Generation at low relative humidity (RH). At 45% RH, all samples generated peak voltages of less than 100 volts. However, Kraft corrugated at 12%RH peaked out at 12,870 volts. The Number 3 Bleached White liner generated 16,790 volts¹.

During transport and shipping, RH conditions can reach to less than 4% representative of winter months in Colorado or Santa Ana Wind conditions in California. In flight, the relative humidity of the aircraft cabin dropped from 60%RH to 9.33% after 20 minutes (Figure 1). The 7" x 7" sheet of Kraft corrugated charged to -4,403 volts. Before takeoff, this same sheet charged to less than 10 volts.

Traditionally, the author's field measurements in electrostatic discharge (ESD) safe

areas between 30% RH to 70% RH have produced corrugated paperboard reading at less than 100 volts. However, recent on-site testing of Asia-Pacific sourced Cylinder Machine corrugated liner, produced results in excess of 100 volts.

USA grades of Kraft corrugated linerboard have moisture contents of approximately 5% to a high of about 9%; Oyster White, number 1 and 3 white liners can range from 6% to 7%. Corrugated medium can have a moisture content of 5% to 7%. Moisture insures elasticity of paper as problems can occur at <5%.

Many USA & EU Integrated paper companies that have abundant forestlands, paper mills and box conversion capabilities employ a Fourdrinier papermaking process patented in 1801 by John Gamble. Fourdrinier paperboard is a homogenous admixture of wood pulp, fiber, water and other additives with aligned moisture retaining wood fiber for strength.

Most of the Asia-Pacific forestlands have long been depleted. The Cylinder Machine papermaking process (invented by John Dickinson in 1809) produces a multi-layered corrugated liner sheet consisting of newsprint, rags, bamboo, recycled corrugated containers and other products. Therefore, lack of moisture containing virgin wood fiber can run the risk of producing charge generating paperboard.

The Fourdrinier process insures higher moisture content of paperboard enabling Kraft linerboard to be more conductive in environments ranging from about 15%RH to <30%RH. Electrical resistance of paperboard

[1] A STUDY OF ESD CORRUGATED, Bob Vermillion, CPP, Certified ESD Engineer NARTE, ARP Engineering, Larry Fromm, PE, Hewlett-Packard, ESDA Symposium, September 1999

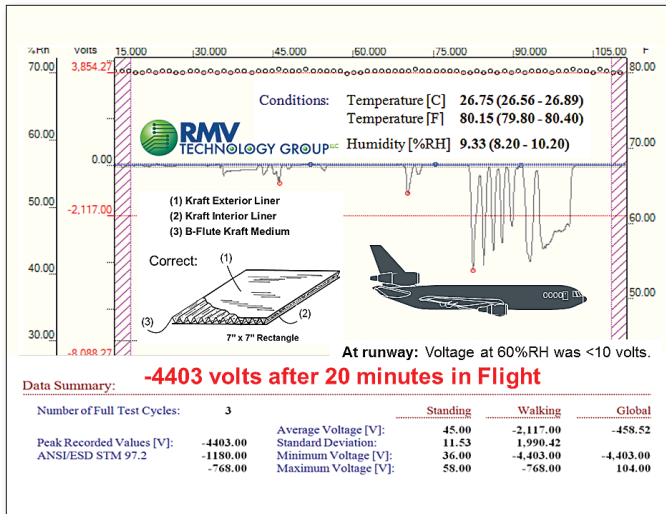


FIGURE 1: Low Humidity in Flight.



FIGURE 2: US & European Papermaking Process.

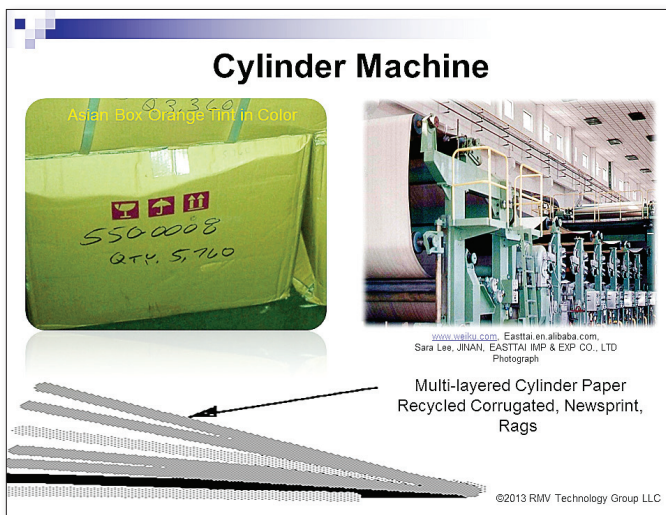


FIGURE 3: Asia Pacific Papermaking Process.

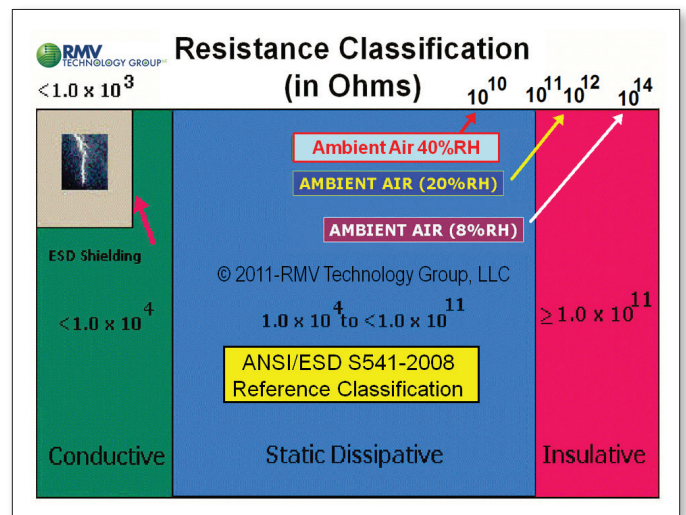


TABLE 1

using ANSI/ESD STM11.11 (surface resistance) or ANSI/ESD STM11.12 (volume resistance) will produce static dissipative readings with corrugated liner containing moisture.

At 40%RH in comparison to the same liner subjected to 12%RH conditioning, resistance testing constitutes one method in differentiating whether the paperboard contains adequate moisture. Corrugated linerboard moisture content at 5% or more insures insure a greater likelihood of being low charging. Therefore, there is a relationship between Surface Resistance and Relative Humidity as illustrated in Table 1.

According to the late John Kolyer, Ph.D. (Boeing, Retired) in his book ESD from A to Z, surface resistance of humidity dependent materials rises and falls when RH fluctuates.

Note: ANSI/ESD S541 lists [1.0 x 10¹¹ ohms] as the standard cutoff for retention of static dissipative properties. In practice, however, a lower cut-off is often desired for packaging materials since dry air may be encountered in shipping and handling. In cold and dry climactic conditions, relative humidity can reach 4% or below. In Figure 3, the reader will observe a Kraft paper



FIGURE 4: Kraft Shopping Bag Charging in Winter .

grocery bag charging to -4,970 and 2,403 volts at 13%RH.

Since the mid-1990s, the author has presented on the effects of paper charging. Moreover, recent on-site assessments by the author have identified Asia-Pacific Cylinder Machine paperboard as a significant charge source at moderate RH levels.

In Figure 5, left, the Fourdrinier liner is abundant in wood chips while the Cylinder liner (right, photograph) is layered and contains recycled paperboard, ink pigments, extraneous fiber and other unknown content.

At 20%RH, the Asia-Pacific Oyster White Cylinder paper measured in the insulative range at $[1.6 \times 10^{11}$ ohms] and 5,234 volts. At 9%RH, the voltage was 16,901 volts. In contrast, at 43%RH, the same Oyster White Lock Front Mailer measured $[1.9 \times 10^9$ ohms] and produced 99 volts (Figure 6). Another risk to an organization is the Incoming Receiving Department practice of transferring ESD sensitive devices from charge generating corrugated containers (without the use of ionization). This represents a hazard to ESD sensitive devices at a distance of less than one (1) foot.

During RFID placement (Figure 7), the tags can be incorrectly positioned representing another risk. Oftentimes, corrugated containers can travel down a conveyor in an “upside down” position so that a RFID tag ends up on the new bottom of a box. The tag then passes between two or more steel rollers at the instant when one of the rollers generates an ESD event (between its shaft and the side rail). Arguably, the thought is that corrugated containers can be placed on ESD workstations with an assumption that the packaging will not harm ESD sensitive devices above 30%RH. One must consider paperboard charging. For instance, Asia-Pacific Cylinder Machine linerboard charged to -4,450 volts at 35%RH as illustrated in Figure 8. The NASA Workmanship NASA-STD 8739.6 on page 16 sets Temperature and Relativity levels in section 6.1 18° - 30° C (65° - 85° F) and a maximum relative humidity of 70 percent. For ESD-sensitive hardware, the minimum humidity is 30%RH. For Human Body Model (HBM) Class 0 ESD sensitive devices (<250 volts), the minimum RH level is 40%.

The IC Carriers (Dip Tubes) that house ESD sensitive devices were not protected by static shielding or RFI/EMI attenuating

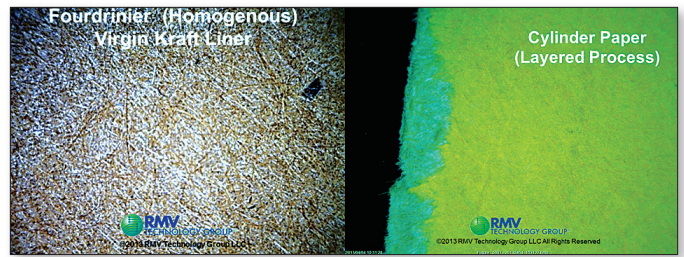


FIGURE 5: US & European Kraft Liner (Left) Asia Pacific Kraft Liner (Right).



FIGURE 6: Asia Pacific Bleached Liner Left – Room Conditions Right – Low Relative Humidity (RH).



FIGURE 7: RFID on Kraft RSC Box.

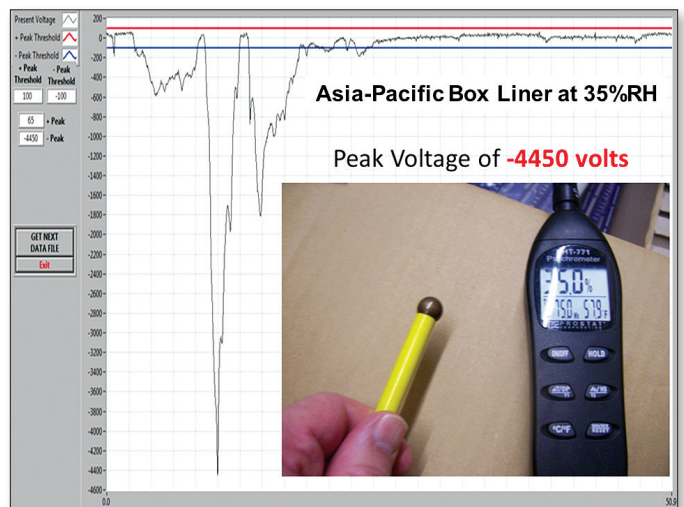
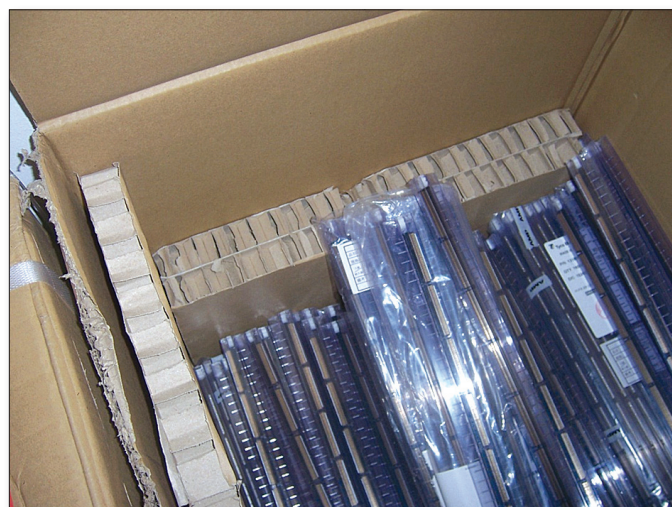


FIGURE 8: 4-ESD Sensitive Devices in Charge Generating Box.

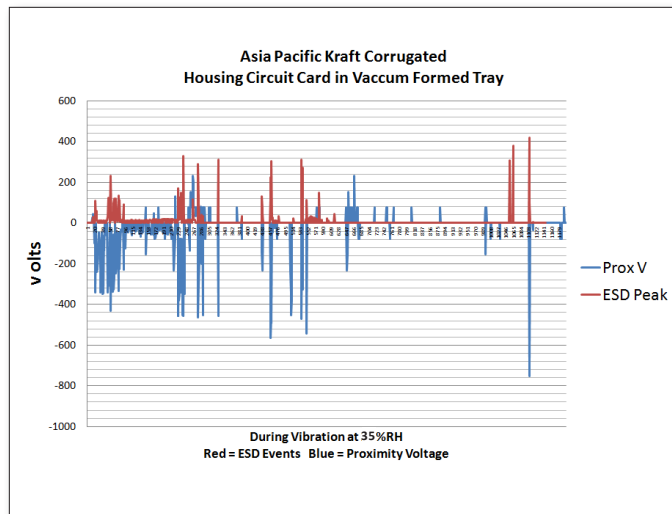


FIGURE 9: Asia Pacific Box Liner at 35%RH.

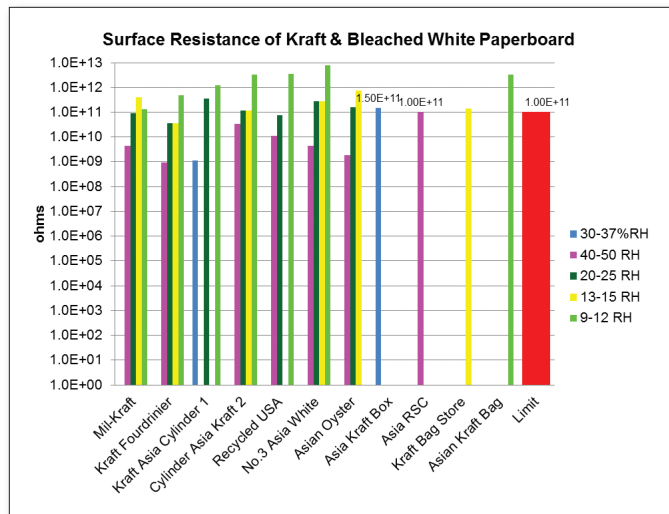


TABLE 2

Moisture Barrier Bags (MBB) in Figure 8. Consequently, for Asia Pacific Cylinder Machine paperboard, charge generation during transport causes ESD events when the relative humidity falls below 20%RH and up to 37%RH; there was one incident of charging to 667 volts at 43%RH. USA and EU Fourdrinier paperboard will charge to below 9%RH and up to 15%RH. The reader can observe simulation testing at low RH for a corrugated SIMM Module Asia Pacific box that generated numerous of electrostatic field voltages (Prox V) and discharges (ESD Peak - Voltage). The field induced model (FIM) discharges would most likely damage ESD sensitive devices if shielding precautions are not implemented.

Therefore, at first glance, Table 3 indicates that Asia-Pacific Cylinder paperboard has a tendency to generate static electricity at higher RH levels than USA and EU Kraft and bleached liner.

In short, further work in this area will be conducted to build a case history for comparison between Asia-Pacific Cylinder Machine corrugated versus EU and USA Fourdrinier grades of paperboard. Cylinder Machine paperboard from the Asia-Pacific region has a greater tendency to charge generate than Fourdrinier produced corrugated linerboard manufactured in both the US & EU.

ABOUT THE AUTHOR

Bob Vermillion is a subject matter expert in ESD mitigation of Material & Packaging and is an ESDA Standards Committee Member. He was the first to identify and present on suspect counterfeit ESD Packaging in the Supply Chain at the NASA-QLF in 2010. RMV is located on-site at NASA-Ames Research Center. He publishes numerous articles and white papers on advanced materials, packaging non-compliance and suspect counterfeiting in manufacturing, materials handling, shipping and long-term storage for the aerospace/defense, medical and electronics sectors. Speaking engagements include invitations from the DOD, DOE and NASA to present on Supplier Issues with Materials and Packaging. RMV is a NASA approved ESD Laboratory at NASA-Ames. An internationally recognized author and inventor, Vermillion developed professional level

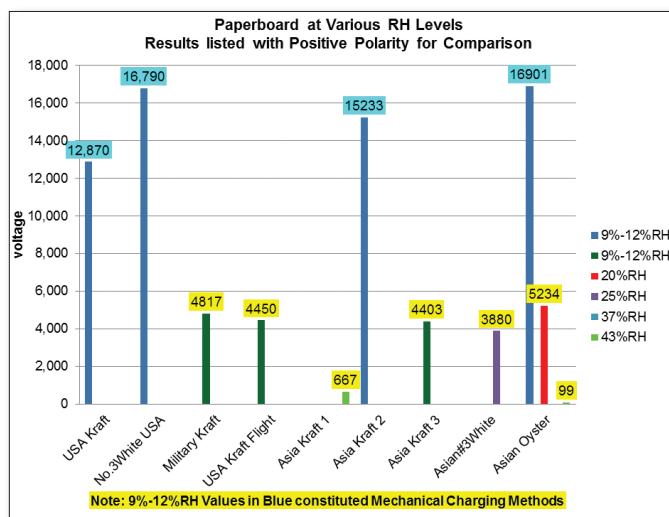


TABLE 3

ESD Packaging Seminars for Cal Poly, SJSU, UC Berkeley, Loyola Marymount, Clemson University and Oxford University. RMV is a 3rd Party ESD Material Testing, Training and Consulting Company. Vermillion is an active member of SAE G-19 Counterfeit Components and SAE G-21 Counterfeit Materiel Committees. He can be reached at bob@esdrmv.com.

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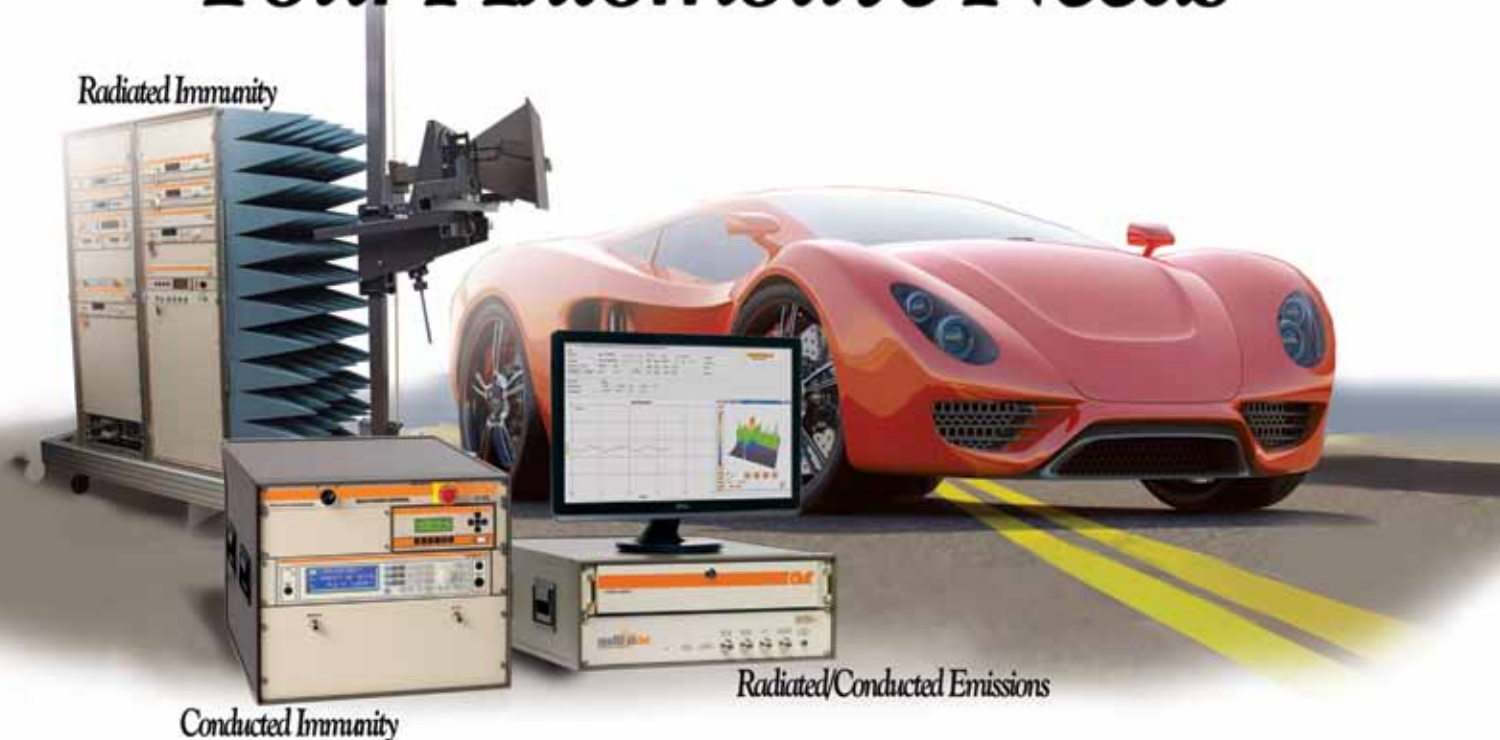
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