SerDes System CTLE Basics

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Date: March 22, 2012

Introduction

High speed digital (HSD) integrated circuits (ICs) are used in Serializer/Deserializer (SerDes) systems. In such systems, a lossy channel exists between the transmitter circuit and the receiver circuit and at high data rates the received data stream is severely distorted and requires reconstruction (equalization) before use. For system design, signal integrity (SI) engineers often convert such circuits into Input/Output Buffer Information specification (IBIS) models to achieve fast simulations for evaluation and performance prediction.

One common equalizer approach used in transmit and receive circuits is a continuous time linear equalizer (CTLE).

This article discusses CTLE characteristics in the time and frequency domain. The algorithmic point of view is presented and not the actual circuit implementation point of view. The algorithmic models discussed are based on the IBIS Algorithmic Model Interface (AMI) standard.

General SerDes System

Figure 1 shows a general SerDes system:

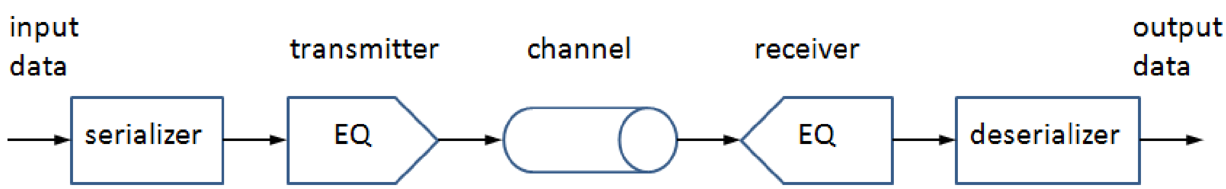

Figure 1. A general SerDes system

The typical SerDes system contains input data, serializer, transmitter (TX), channel, receiver (RX), deserializer and ouput data. The serial data bit stream is input to the transmitter. The transmitter consists of an equalizer (EQ) and a linear analog backend that includes packaging effects. The channel between the transmit backend and receiver front end consists of transmission lines (TL) that may include wiring and printed circuit board traces. The receiver front end includes packaging effects. The receiver contains signal processing with an EQ and clock and data recovery (CDR).

Though the channel in real systems has multiple input and output pins, typically with differential input and output pin pairs, the discussion in this article is as a channel with a single ended input and output.

The Problem

The typical SerDes system channel is a linear system that contains high frequency attenuation of the transmitted signal.

Figure 2 shows a typical channel frequency domain characteristic used with data with a 100 psec bit time (10 Gbps bit rate).   The y-axis is in dB units.

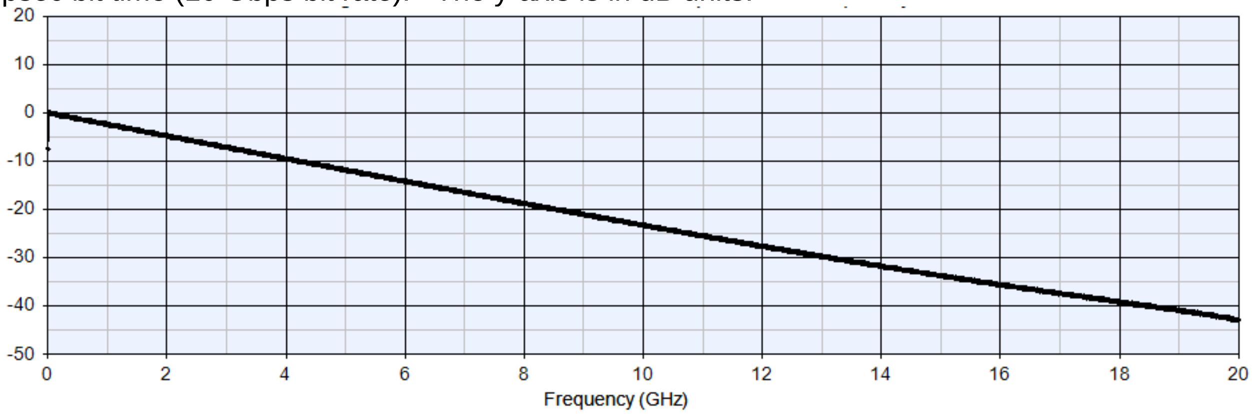

Figure 2: Channel Attenuation vs Frequency

This curve is representative of any frequency domain characteristic. Most practical systems have a channel characteristic that includes a lot of irregularity due to system mismatches and signal suck-outs. This simplified curve is for discussion purposes in this article.

The Nyquist frequency for this data stream is at 5 GHz. The channel attenuation at 5 GHz is about -12 dB. This high frequency attenuation is typical for a SerDes system channel and needs to be restored to a flat response within the Nyquist frequency band to achieve low bit error rates in the SerDes system.

This high frequency amplitude and phase distortion causes “smearing” of the data bits at the receiver side. This data smearing is called intersymbol interference (ISI). When the data bits are overlayed upon each other an “eye” diagram is formed and in this case will appear with a closed eye.

Figure 3 shows the transmit bit stream into the channel and the received bit stream out of the channel. Individual or rapidly alternating zeros and ones do not reach their full steady state value at the receiver after a lossy channel. The output data stream (red) is much distorted from the input data.

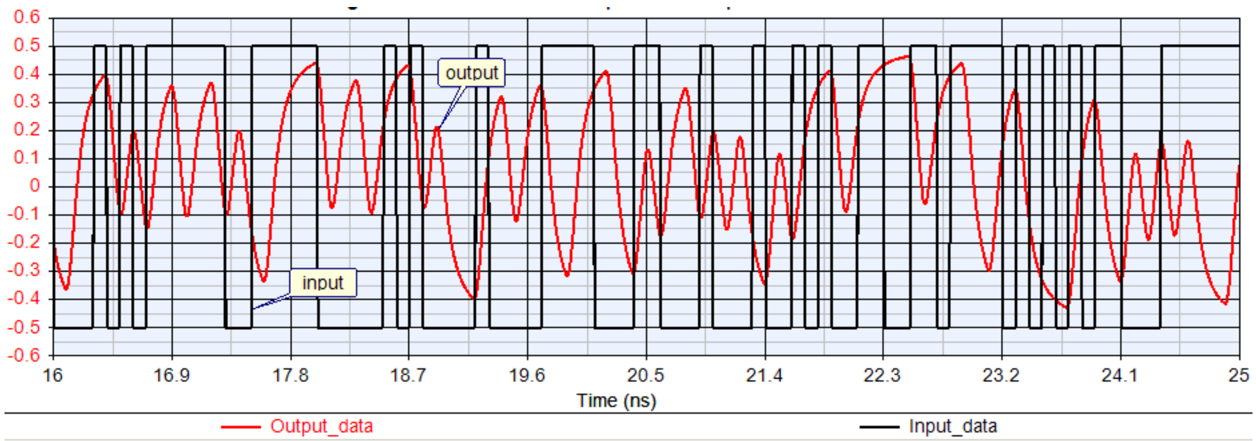

Figure 3: Channel input and output data streams

Figure 4 shows the received signal eye diagram. The output eye is very closed.

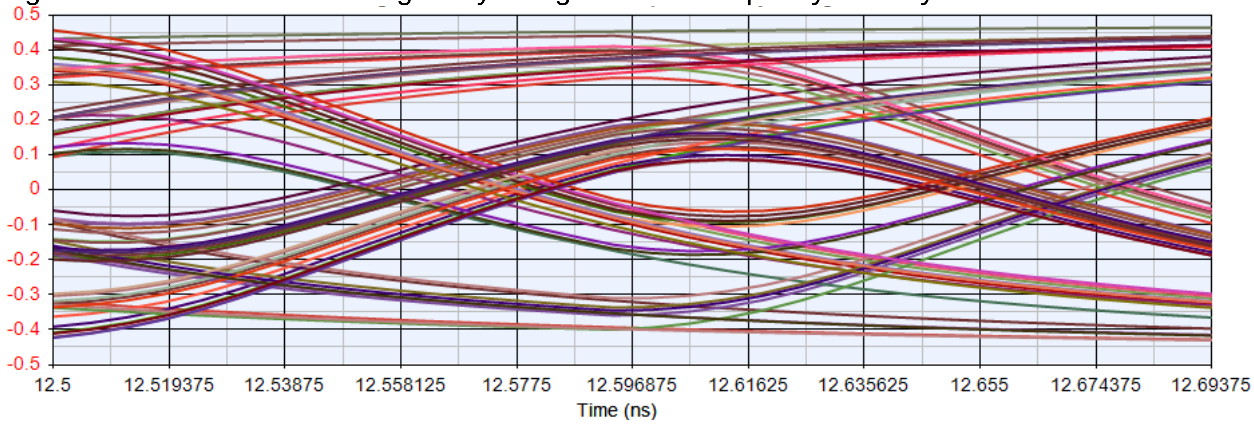

Figure 4: Channel output data eye diagram

These figures show the problem with the closed eye at the receiver. The data needs to be reconstructed (equalized) for the received data to become usable.

Equalization is typically implemented in both the transmitter and in the receiver. Before the channel, it is desirable to "peak" the transmitted high frequency content rather than do all the high frequency peaking at the receiver side. High frequency peaking at the receiver side degrades the receiver input signal to noise ratio (SNR) whereas frequency peaking at the transmit side does not. Therefore, in the transmitter, equalization is implemented to provide pre-emphasis of the high frequency leading edge of bit transitions. In the receiver, equalization is implemented to restore the combined transmitter and channel characteristic towards a reference channel that has no or reduced intersymbol interference.

CTLE in a Transmitter

In the transmitter, equalization using a CTLE is implemented to provide pre-emphasis of the high frequency leading edge of bit transitions. This can be done in several ways. Two techniques are discussed here: 1) CTLE using high pass filter (HPF) with poles and zeros; 2) CTLE using a feed-forward equalizer (FFE).

CTLE using high pass filter (HPF) with poles and zeros

A HPF CTLE can provide emphasis in its high frequency response and can be created using a single pole and zero, H(s) = K*(s-z)/(s-p), where z is the zero at 1.625 GHz and p is the pole at 6.5 GHz.

Figure 5 shows the frequency response of the HPF CTLE along with the Channel and the Channel plus HPF CTLE. The Channel alone is the black curve. The HPF CTLE response is the red curve. The combined HPF CTLE + Channel response is the green curve. The y-axis is in dB units.

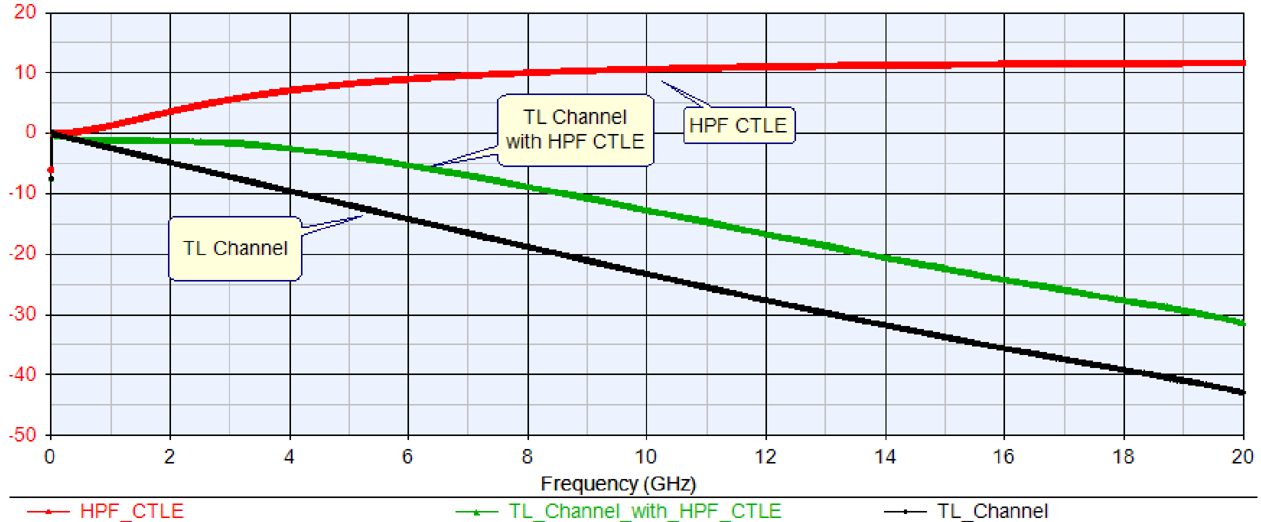

Figure 5: HPF CTLE and Response vs Frequency

As can be seen, the HPF CTLE has frequency response peaking and when combined with the channel response restores the flat frequency response (green curve) from zero Hz to frequencies approaching the data stream Nyquist frequency of 5 GHz.

Figure 6 shows that the resultant eye diagram from the combined HPF CTLE and Channel is wide open.

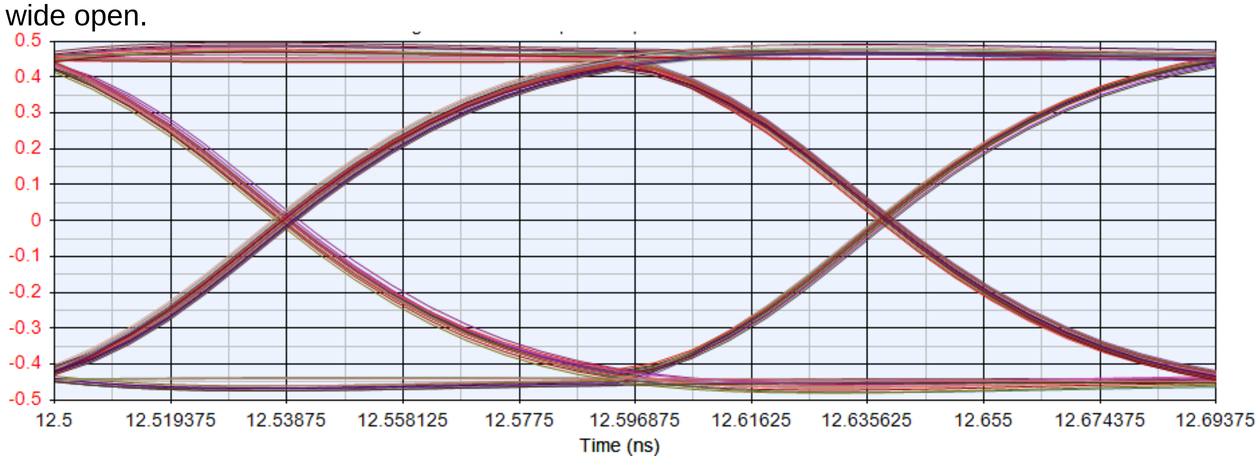

Figure 6: Channel Response equalized with a HPF CTLE

One further note on the HPF CTLE, it is often followed by high frequency poles to force attenuation of any high frequency noise so that it does not degrade the SerDes system performance.

CTLE using a feed-forward equalizer (FFE)

A FFE CTLE can provide emphasis in its high frequency response and be created using delays, gains and summer.

Figure 7 shows a FFE CTLE with four taps.

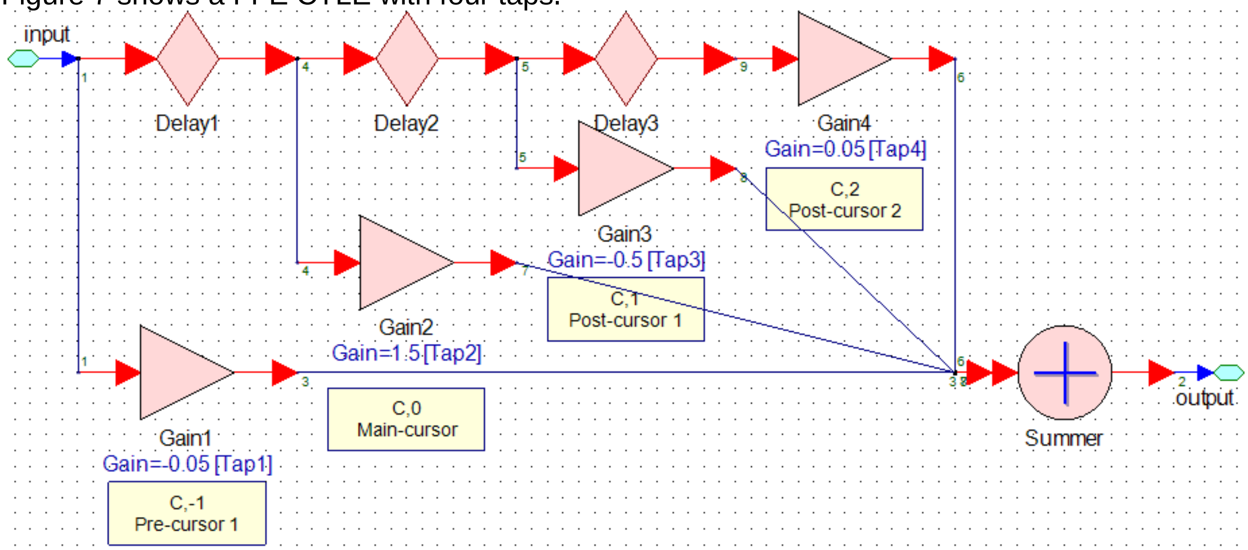

Figure 7: FFE CTLE with four taps.

The FFE CTLE is a finite impulse response (FIR) filter. The input digital data propagates through a series of delay lines. Each delay is equal to one bit unit time interval. In this example, it is 100 psec (set up with 16 samples per bit). The signal is sampled before and after each delay line and is multiplied by a FIR tap coefficients C_k. C_{-1} is the first pre-cursor tap. C_0 is the main cursor tap. C_1 and C_2 are the first and second post-cursor taps. The pre and post cursor taps compensate for the ISE before and after the main cursor respectively. The outputs from the FIR taps are summed to produce the FFE CTLE output. The number of taps depends on the length of the channel impulse response relative to one bit unit time interval.

For the Channel we have been discussing above, this FFE CTLE has its tap value set as shown in Figure 7.

Figure 8 shows the frequency response of the FFE CTLE along with the Channel and the Channel plus FFE CTLE. The Channel alone is the black curve. The FFE CTLE response is the red curve. The combined FFE CTLE + Channel response is the green curve. The y-axis is in dB units.

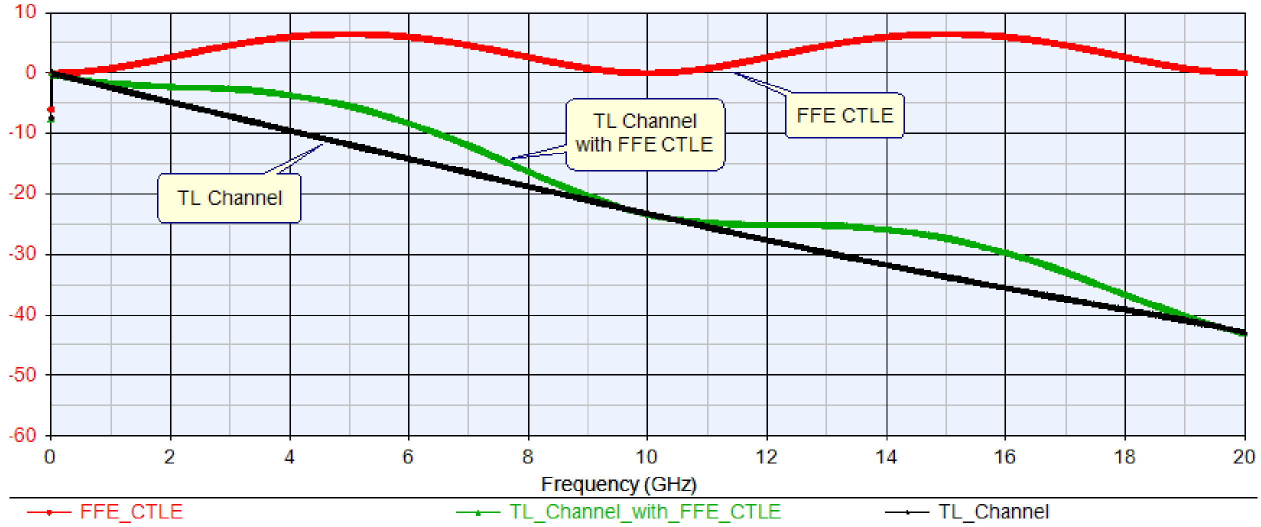

Figure 8: FFE CTLE and Channel Response vs Frequency

As can be seen, the FFE CTLE has frequency response peaking that is periodic at the bit rate (10 GHz in this example) and when combined with the channel response (green curve) the first Nyquist zone (zero Hz to 5 GHz) is restored to a more flatter frequency response.

Figure 9 shows that the resultant eye diagram from the combined FFE CTLE and Channel is wide open.

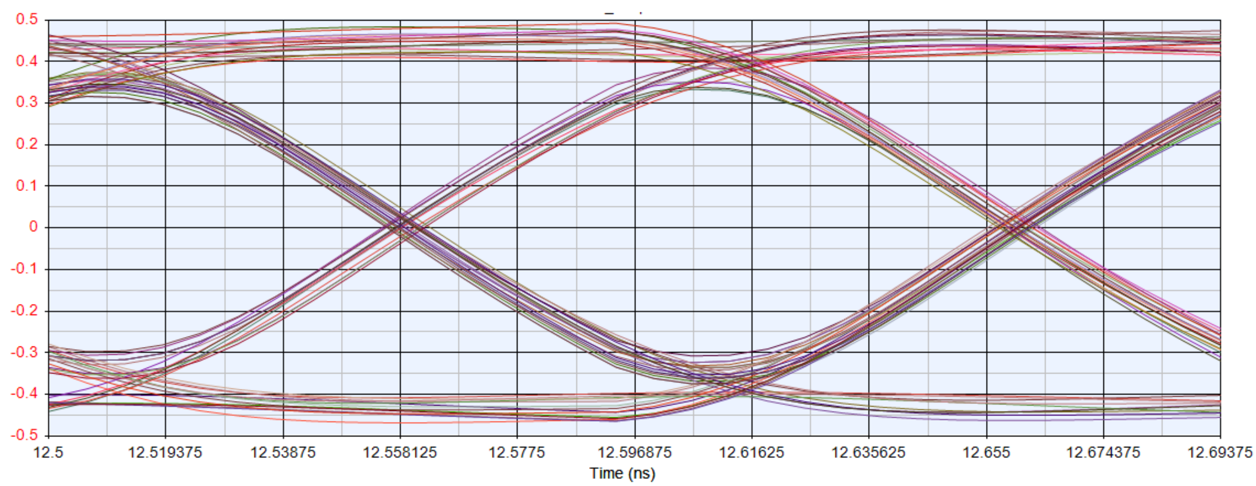

Figure 9: Channel Response equalized with a FFE CTLE.

One further note on the FFE CTLE, it is often followed by high frequency poles to force attenuation of any high frequency noise so that it does not degrade the SerDes system performance.

CTLE in a Receiver

In the receiver, use of a CTLE is intended to equalize the combined characteristic of the transmitter and channel and remove the ISI at the received signal sampling points.

The RX CTLE is similar to the TX FFE CTLE except that the input is an analog signal. The RX CTLE is often called a Discrete Time Linear Equalizer (DLE). It may also be called an FFE CTLE. In this article, it will be referred to as a DLE CTLE so as to not conflict with the FFE CTLE application in the transmitter discussed above.

As an FIR filter, the DLE CTLE operates on the analog input signal after it has been sampled by a sample-and-hold circuit. Typically, there are N samples per data time interval. The FIR taps are designed to subtract ISI effects from adjacent bits. If the DLE CTLE is designed to equalize for 3 pre-cursor pulses and 5 post-cursor pulses about the main pulse, then the CLE CTLE will have N*9 taps. The output of the DLE CTLE will further be sampled at one point per data time interval for data detection. The DLE CTLE will only cancel ISI at the data detection sample points.

A reference channel frequency response, H_ref(s), can be defined that has zero or low ISI at the data detection sample points. This is often defined to be a raised cosine characteristic or another characteristic as desired. It may also be supplemented with additional high frequency poles to reduce its high frequency response.

Figure 10 shows the eye diagram for a reference channel for a 10 Gbps signal.

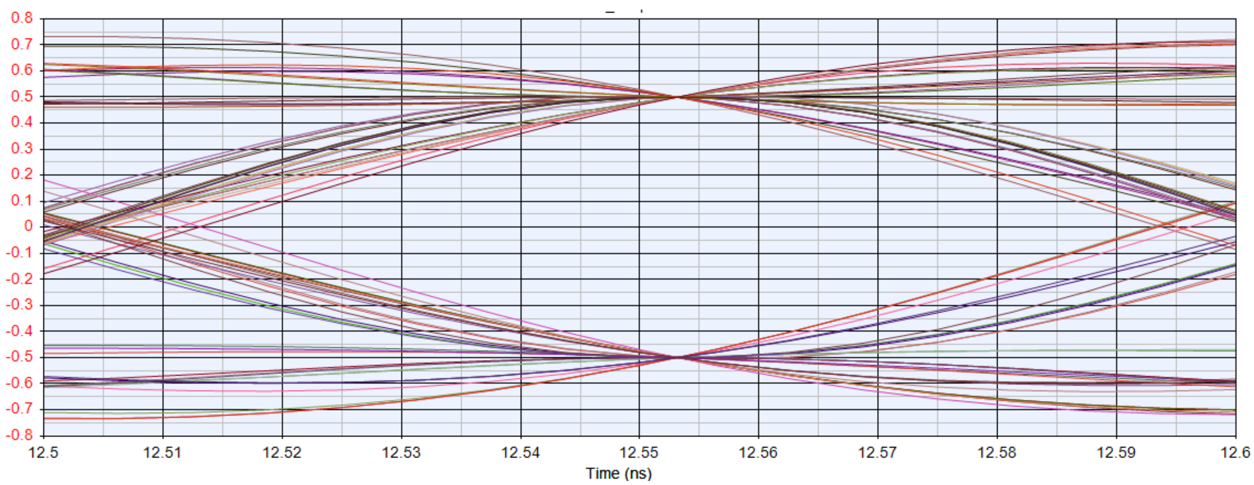

Figure 10: Eye diagram for a reference channel

By multiplying the inverse of the Channel frequency response, 1/H_TL(s), by the reference channel response, H_ref(s), the resultant response will be the desired DLE CTLE frequency response, H_dle(s).

This process discussed here presumes that the Channel frequency response does not have noise distortions in the frequency response. If it does have noise, then an averaging processes is needed to smooth out the noise to effectively results in a frequency response that has a high signal to noise ratio.

Figure 11 shows the magnitude vs frequency plots for these three functions. The y-axis is in dB units.

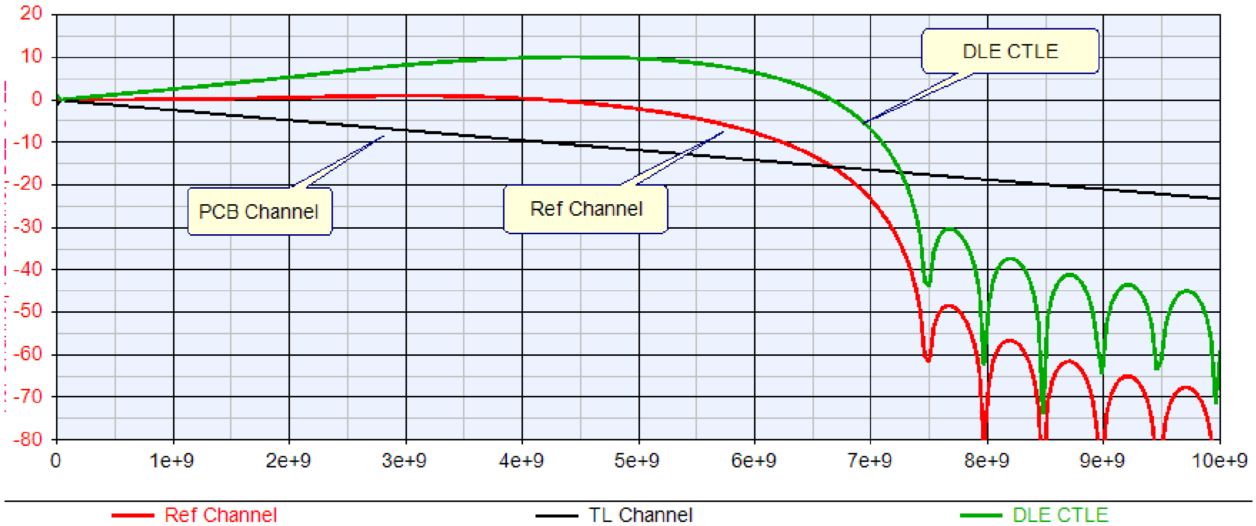

Figure 11: Magnitude (dB) vs frequency for the reference channel (red), channel (black) and DLE CTLE (green).

As can be seen, the DLE CTLE response, H_dle(s), is the ratio H_ref(s) / H_TL(s).

The inverse FFT transform of H_dle(s) will provide the desired DLE CTLE tap coefficients. Figure 12 shows the impulse response vs time for these three functions.

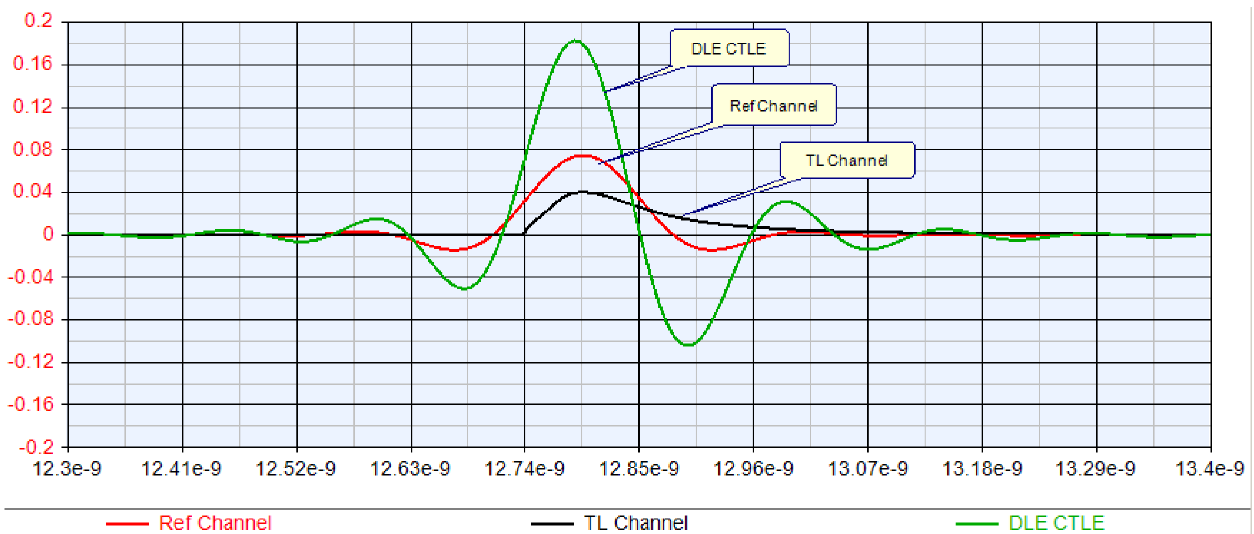

Figure 12: Impulse response vs time for the reference channel (red), channel (black) and DLE CTLE (green).

Keeping in mind that the data time interval is 0.1e9 sec, it can be seen that the DLE CTLE can be specified to provide equalization for 3 time intervals before the main response and for 5 time intervals after the main response.

Figure 12 shows the frequency response of the DLE CTLE, the Channel, and the Channel plus DLE CTLE. The Channel alone is the black curve. The DLE CTLE response is the red curve. The combined DLE CTLE + Channel response is the green curve.

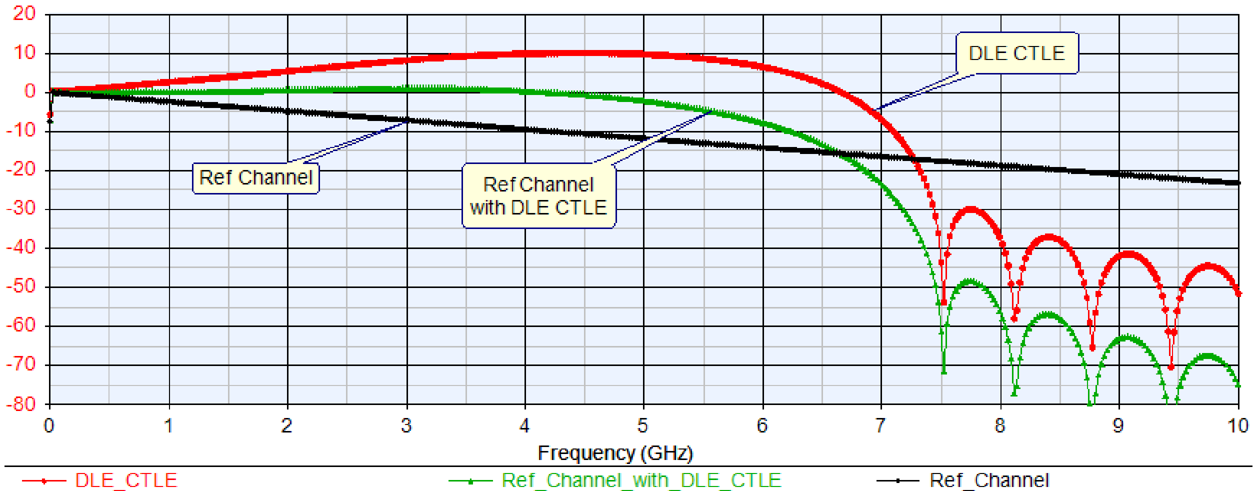

Figure 12: DLE CTLE and Channel Response vs Frequency

As can be seen, the DLE CTLE has frequency response peaking and when combined with the channel response (green curve) the first Nyquist zone (zero Hz to 5 GHz) is restored to reference channel frequency response.

Figure 13 shows that the resultant eye diagram for the combined DFE CTLE and Channel and is quite similar to that for the reference channel. The eye is wide open.

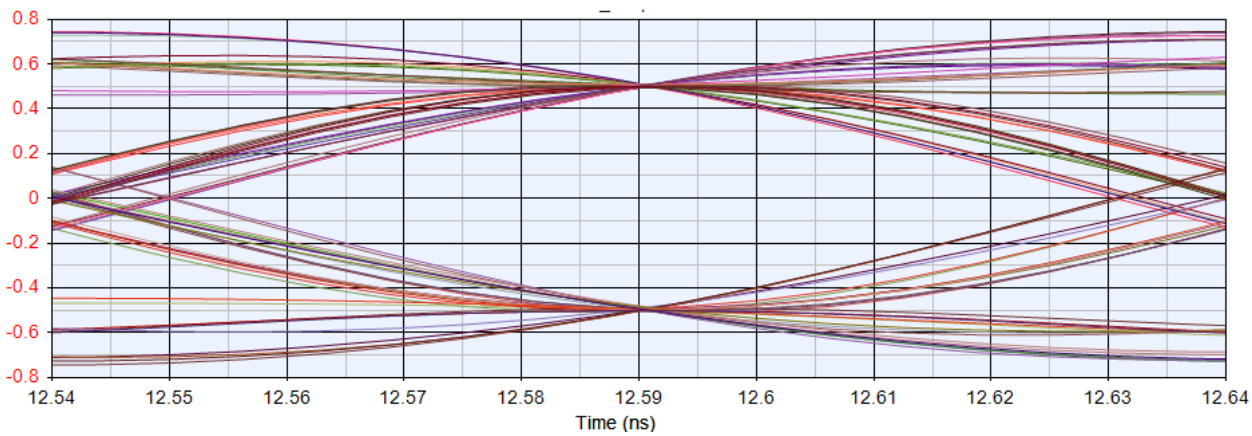

Figure 12: Channel Response equalized with a DLE CTLE.

DLE CTLE Limitations

The DLE CTLE responds to the received analog signal which includes noise. As is seen in figure 12, the high frequency noise is amplified. This is especially so when the DLE CTLE is equalizing the Channel with no pre-emphasis provided by the transmitter. To reduce the high frequency noise amplification in the receiver, the transmitter typically includes pre-emphasis using a CTLE as was discussed above.

An alternative to the receiver DLE CTLE or in addition to it, a Decision Feedback Equalizer (DFE) is often used. The DFE is discussed in a separate article from this author.

Summary

Today's high-speed digital SerDes systems require use of equalizers to ensure signal integrity in the system. Continuous time linear equalizers (CTLEs) are typically used in transmitter and receiver designs. This article provides the reader the basics for CTLE models from an algorithmic point of view. HPF CTLE and FFE CTLE models were discussed for use in transmitters. The DLE CTLE model was discussed for use in receivers. Algorithmic modeling is important for IBIS AMI modeling of SerDes systems to achieve fast simulations for evaluation and prediction of high performance networks.

Acknowledgment

Thanks to Agilent Technologies, Inc., EEsof Division for providing the SerDes signal integrity market with their fine line of EDA tools, SystemVue and Advanced Design System. These tools provide a very effective and efficient process for generating portable AMI models per the IBIS standard.

Biography

John Baprawski is Systems Engineer with over 35 years designing RF and communications systems and EDA system design products for the RF, Communications, and High Speed Digital markets. John was formerly with Agilent EEsof for 22 year as the R&D manager who led the R&D team for development of system level design tools. Currently, John is a consulting engineer for modeling high speed digital (HSD) integrated circuits (ICs) based on the industry Input/Output Buffer Information Specification (IBIS) Algorithmic Model Interface (AMI) standard (IBIS Version 5.0, August 29, 2008).

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