SRAM, DRAM and flash memories

- **Quick Overview:**

RAM - Random-access-memory: Reading and writing is possible
SRAM and DRAM need a supply voltage to hold their information while flash memories hold their information without one.

DRAM Dynamic-RAM: Dynamic stands for the periodical refresh which is needed for data integrity in difference to the Static-RAM (SRAM).

- **SRAM:**

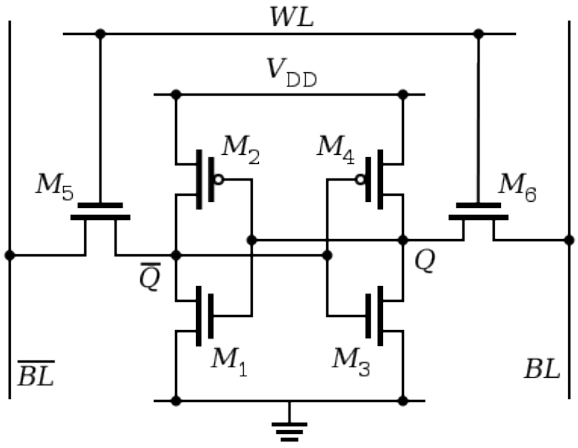
SRAM is usually built in CMOS Technology with six transistors. Two cross-coupled inverters are use to store the information like in a flip-flop. For the access control two further transistors are needed. If the Write Line is enabled then data can be read and set with the Bit-Lines.

States of an SRAM-Cell:

- Standby: Write Line is disabled, no reading and writing is possible
- Reading: Reading starts with preloading the Bitlines to 1. Now the Writline gets activated. If Q is 1 then BL gets pulled to one and $\overline{BL}$ towerds zero. A sens ampifier senses which line hast he higher voltage.
- Writing: Setting the Bitline to 1 (BL = 1, $\overline{BL}$ = 0) then enabling the write line will write a one. The input-drivers have to be much stronger than the transitors.

Advantages: Quick, easy to control, integrated in the chip -> fast because no bus is needed like in DRAM

Disadvantages: Many transistors are needed -> expensive, higher power consumption than DRAM



- **DRAM:**

Only one Mosfet with a Capacitor is needed.
The Wordline enables writing and reading with the Bitlines.

The DRAM cell hast to be refreshed periodic, since the chare gradually leaks.

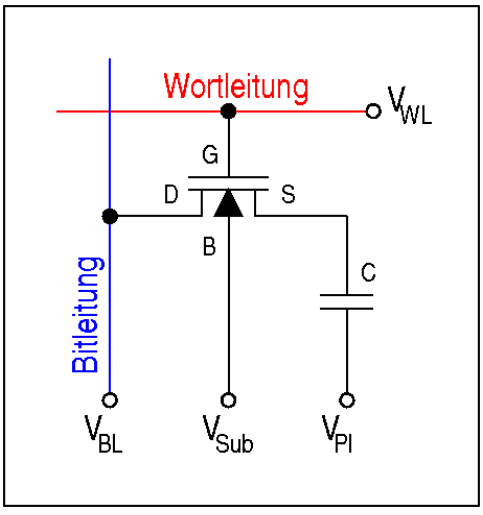
Read Operation

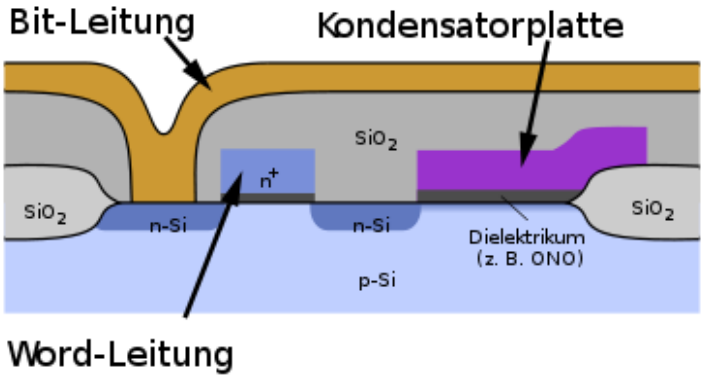
1. The two bit-lines are precharged to the same voltage that is between high and low level.
2. The Wordline gets activated. If the storage cell's capacitor is discharged, it will greatly decrease the voltage on the bit-line as the precharge is used to charge the storage capacitor. If the storage cell is charged, the bit-line's voltage only decreases very slightly.
3. The small voltage difference between the odd and even row bit-lines is getting amplified of a particular column until one bit line is fully at the lowest voltage and the other is at the maximum high voltage. Now the date is available.

Write Operation

Writing works with the Bitlines to charge or uncharge the capacitor.

Advantages: Cheap Production, lower power consumption as SRAM
Disadvantages: slower than SRAM





- **Flash**

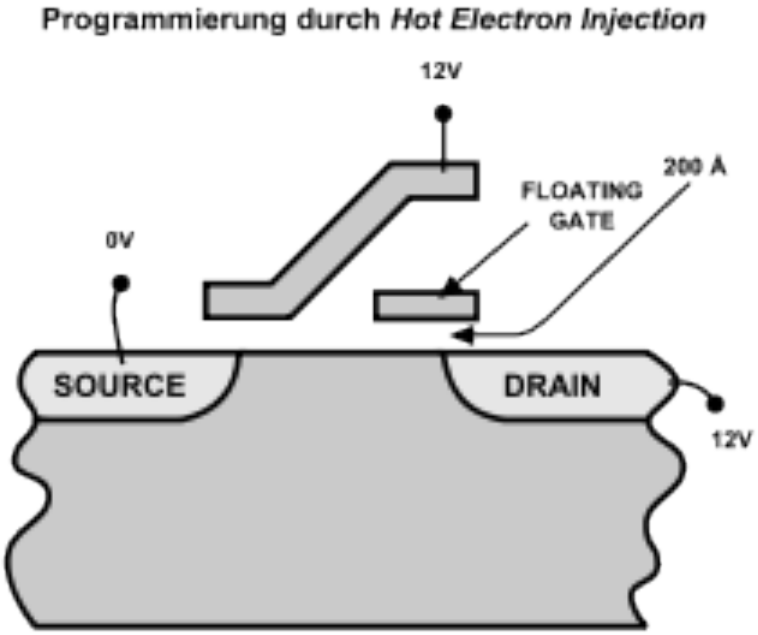
The saving works with the Floating-Gate. The Floating-Gate is between the Gate and Source-Drain Area and isolated with an Oxide-Layer.

If the Floating Gate is uncharged then the Gate can control the Source Drain current. The Floating Gate gets filled (Tunnel-Effect) with electrons when a high voltage at the Gate is supplied.

Now the negative potential on the Floating-Gate works against the Gate and no current is possible.
The Floating-Gate can be erased with a high voltage in reverse direction at the Gate.

Advantages: No power for storing needed.
Disadvantages: slower than SRAM or DRAM

Multi-Level-Cell: Floating Gate with different states (electron density). Reading and writing is slower



All Pictures are taken from Wikipedia