*Article*

# A 4 GHz Single-to-Differential Cross-Coupled Variable-Gain Transimpedance Amplifier for Optical Communication

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**Abstract:** This letter presents an inductorless transimpedance amplifier (TIA) for visible light communication, using the UMC 40 nm CMOS process. It consists of a single-to-differential input stage with a modified cross-coupled regulated cascode design, followed by a modified $f_T$-doubler mid-stage with a combined active inductor and capacitive degeneration design for bandwidth-enhancement and differential output. The mid-stage also has an attached common-mode feedback (CMFB) circuit. Both the input and mid-stages have gain-varying and peaking-varying functions. It has a measured gain range of 37.5–58.7 dBΩ and 4.15 GHz bandwidth using a 0.5 pF capacitive load. The gain range results in an input dynamic range of 33.2 µA–1.46 mA. Its input referred noise current is 10.7 pA/$\sqrt{Hz}$, core DC power consumption is 7.84 mW from a $V_{DDTIA}$ of 1.6 V and core area is 39 µm × 26 µm.

**Keywords:** active inductor; capacitive degeneration; cross-coupling; differential; $f_T$-doubler; optical receiver; regulated cascode; transimpedance amplifier; variable-gain

## 1. Introduction

The popularity of new bandwidth-intensive services such as cloud-computing and the internet of things has increased the demand for high-speed data transmission capability. The current wireless transmission (Wi-Fi) frequency for near-field communication is reaching the saturation limit. Thus, the large, unused visible light spectrum (400–800 THz) is gaining increasing research attention for near-field visible light communication (VLC) [1]. There are several key benefits of VLC. Firstly, VLC is secure as visible light is unable to pass through opaque walls, hence securing in-room data transmission. Secondly, VLC is safe to use in locations where interference of RF signals occurs, such as in hospitals and plane cabins [2]. Thirdly, as the cost of light-emitting diodes (LED) is rapidly decreasing, they are expected to become the dominant form of lighting [3]. As LEDs are able to be driven to transmit data through high-frequency modulated light signals [4,5], this makes widespread VLC adoption highly feasible in the near future.

CMOS technology is preferred for chip design as it is cheap, mature and has on-chip photodiode integrability [6,7]. The VLC architecture for the transmitter and receiver is shown in Figure 1 [4,5]. Data are transferred from the transmitter to the receiver through air via a modulated programmed high-frequency flickering light signal using properly driven LEDs. As shown in Figure 1, within the receiver module, the transimpedance amplifier (TIA) is the first chip block and it is the most crucial as it determines the bandwidth, noise and sensitivity for the receiver [7].

Thus, this paper's objective is the design of a TIA which is the most crucial component for a VLC system, which is expected to become common. The main issue for TIA designs is that the photodiode before the TIA has a capacitive load $C_{pd}$ taken as 0.5 pF [3]. $C_{pd}$ contributes greatly to the dominant pole at the input, limiting bandwidth. Thus, the key TIA trade-off is between transimpedance gain $Z_T$ and bandwidth [6]. Many TIA designs counter it by reducing the input impedance $Z_{in}$ [6–8].
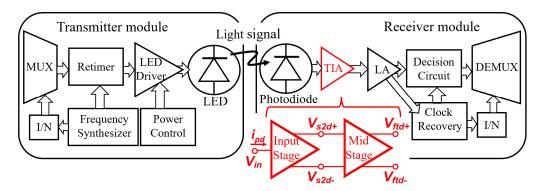
**Figure 1.** Architecture of the transmitter and receiver modules of the VLC system.

Regulated cascode (RGC) is a common TIA design to lower $Z_{in}$ [8,9]. Bandwidth-enhancing methods such as capacitive degeneration and inductive peaking are commonly used [4,8]. RGC design can also be modified to use both PMOS and NMOS configurations [10]. A single-to-differential TIA can be performed via cross-coupling [11]. When the distance between the transceiver and receiver is large, $Z_T$ needs to be large to amplify the weak input signal. Conversely, when the distance is small, $Z_T$ needs to be small to prevent saturation of the input signal. Thus, a gain-varying design with large input dynamic range is desired as $i_{pd}$ varies from 0.15 to 0.9 mA [8,12] for variable link distances [13].

This paper presents a 40 nm CMOS two-stage single-to-differential cross-coupled variable-gain TIA design with analysis of its key features, and it is taped-out and measured. The rest of the paper is organized as follows. Section 2 presents its single-to-differential cross-coupled modified-RGC input stage and Section 3 presents its $f_T$-doubler mid-stage with combined active inductor and capacitive degeneration. Section 4 presents the layout and die microphotographs, while Section 5 presents the post-layout simulation and measurement results. Section 6 is the discussion and comparison with other recent works, while Section 7 is the conclusion.

## 2. Input Stage of TIA Design

The proposed TIA design is modified from the authors' simulated fixed-gain design in [7], with no large DC-blocking capacitors at input required here. The input stage schematic is shown in Figure 2a with the input at $V_{in}$ and outputs at $V_{s2d+|-}$ and with its simplified loop diagram in Figure 2b.

### 2.1. Design Features of the TIA Input Stage

The proposed TIA input stage has some key design features. Firstly, it is differential, unlike in [14], as the component sizes for both sides are equal. The low-pass filters $R_{F1}$ and $C_{F1}$ ensure equal DC biasing of $M_{N2A|N2B}$, while current mirrors $M_{P2A|P2B}$ fix current. Hence, DC at $V_{s2d+|-}$ remain equal as the input current $i_{pd}$ varies. Secondly, it has a combined modified-RGC and cross-coupled design. $M_{N1A|N1B}$ act as both common-gate (CG) and common-source (CS) due to the cross-coupling design [8], giving it both a small CG $Z_{in}$ and large CS gain. The cascode feedbacks to $M_{N1A|N1B}$ are across $M_{P1A|P1B}$ which separate $V_{i2+|-}$ and $V_{s2d+|-}$. Thus, this prevents parasitic capacitances of the feedbacks from loading $V_{s2d+|-}$ while also allowing widths of $M_{N1A|N1B}$ to be smaller.

Thirdly, there are both variable-gain and peaking functions which increase the dynamic range upper limit. $M_{VG1}$ acts as a variable resistor. When $V_{G1}$ is low, $M_{VG1}$ is off. As $V_{G1}$ increases, $M_{VG1}$ turns on linearly, reducing gain across $V_{s2d+|-}$. The low-pass filters $R_{F1}$ and $C_{F1}$ also generate a zero that affects the frequency response. When $V_{P1}$ is increased, $M_{VP1}$ turns on and the zero shifts, preventing peaking for lower gain settings, making this TIA design suitable for variable VLC conditions.

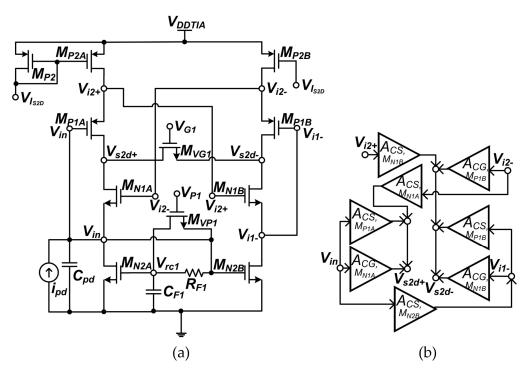**Figure 2.** (**a**) Schematic and (**b**) simplified loop diagram of the proposed TIA single-to-differential input stage.

*2.2. Input Impedance and Transimpedance Gain*

Input impedance $Z_{in}$ is estimated by taking all components connected to $V_{in}$ and is calculated as:

$$Z_{in} \approx \frac{1}{g_{mN1A}\{1 + 0.5(g_{mN2B} + g_{mP1A})r_o\}}$$

where $r_o$ is the transistor output resistance and $r_o$ of $M_{P2A|P2B}$, $M_{P1A|P1B}$, $M_{N1A|N1B}$ and $M_{N2A|N2B}$ are taken to be the same.

The single-ended transimpedance gains of the input stages $Z_{T,S2D+}$ and $Z_{T,S2D-}$ are different due to their asymmetrical design. They are estimated by finding and combining gain loop transfer functions, with the simplified diagram shown in Figure 2b. $Z_{T,S2D+}$ of loops from $V_{in}$ to $V_{s2d+}$ and $Z_{T,S2D-}$ from $V_{in}$ to $V_{s2d-}$ are calculated from their respective loop gains to be:

$$Z_{T,S2D+}(0) = Z_{in} \times \left(1 + 4g_{mN1A}g_{mN2B}r_o^2 - 2g_{mP1A}r_o\right)$$

$$Z_{T,S2D-}(0) = -Z_{in} \times \{2(g_{mN1B} + g_{mN2B}r_o) - 2g_{mP1B}r_o\}$$

The differential transimpedance gain $Z_{T,S2D,d}$ is equal to $Z_{T,S2D+} - Z_{T,S2D-}$.

## 3. Mid-Stage of TIA Design

The schematic of the modified $f_T$ (transit frequency) doubler mid-stage is shown in Figure 3.

The mid-stage has additional gain and peaking variation functions and a common-mode feedback (CMFB) circuit as compared to [7]. It makes the differential signal highly ideal while enhancing bandwidth. The inputs of the mid-stage are at $V_{s2d+|-}$ and outputs are at $V_{ftd+|-}$.
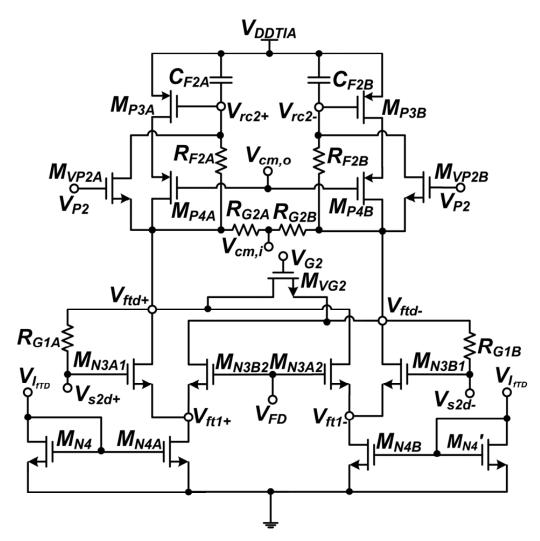
**Figure 3.** Schematic of the modified $f_T$-doubler mid-stage of the proposed TIA.

### 3.1. Design Features of the TIA Mid-Stage

The $f_T$-doubler mid-stage also has several design features. Firstly, it halves both the input and output capacitances and gives a more ideal differential signal output at $V_{ftd+|-}$ [5,7]. As in Figure 2, the CS amplifiers $M_{N3A1|N3B1}$ and $M_{N3A2|N3B2}$ drains cross with each other at the outputs $V_{ftd+}$ ($M_{N3A1}$ and $M_{N3A2}$) and $V_{ftd-}$ ($M_{N3B1}$ and $M_{N3B2}$). The transistor sources also combine at $V_{ft1+}$ and $V_{ft1-}$ with two current mirrors $M_{N4A|N4B}$. This makes the output signal highly differential.

Secondly, there is a combined active inductor and capacitive degeneration design consisting of $M_{P3A|P3B}$, $C_{F2A|F2B}$ and $R_{F2A|F2B}$. Both are bandwidth-enhancing techniques that introduce a zero in the gain transfer function, to counter the gain drop-off due to the dominant pole, and thus increase bandwidth. By combining both techniques together into a single unique structure, this reduces circuit area while giving a more prominent zero at $V_{ftd+|-}$, thus increasing the bandwidth even more. Gain and peaking are similarly adjustable and controlled by adjusting $V_{G2}/M_{VG2}$ and $V_{P2}/M_{VP2}$, respectively, preventing peaking in the frequency response at any gain setting and thus preventing instability.

Thirdly, a CMFB circuit is used for differential circuits to prevent common-mode voltage shifts from occurring, which may push transistors out of their normal DC biases [5]. The CMFB circuit in Figure 4a is biased by $V_{CM}$ and $V_{I_{cm}}$, with its input at $V_{cm,i}$ and output at $V_{cm,o}$. $V_{cm,i}$ is taken from the mid-point of the mid-stage differential outputs $V_{ftd+|-}$ while $V_{cm,o}$ controls $M_{P4A|P4B}$ in the mid-stage to complete the CMFB loop.

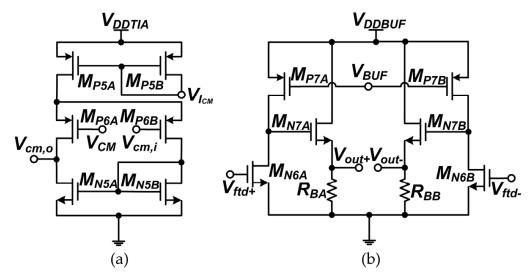**Figure 4.** (**a**) Transistor-level schematic of the CMFB circuit and (**b**) buffer stage.

The buffer after the mid-stage in Figure 4b has a common-source $M_{N6A|N6B}$ that offsets the gain loss of the common-drain $M_{N7A|N7B}$, hence making it gain neutral. Its inputs are at $V_{ftd+|-}$ and outputs are at $V_{out+|-}$.

*3.2. Voltage Gain*

In the $f_T$-doubler, $M_{N3A1|N3B1}$ are the main common sources that produce voltage gain. Hence, the voltage gain for mid-stage $A_{fTD,d}$ is:

$$A_{fTD}(0) = -Kg_{mN3A1}(r_{o,P3A} + r_{o,P4A})$$

where $K$ is the gain impact of the DC-biased $M_{N3A2|N3B2}$.

The differential transimpedance gain of the entire TIA $Z_{T,TIA}$ is equivalent to the differential input-stage transimpedance gain multiplied by the gain-stage voltage gain:

$$Z_{T,TIA}(0) = (Z_{T,S2D+} - Z_{T,S2D-}) \times A_{fTD}$$

**4. Layout**

The layout of the proposed TIA is shown in Figure 5 and the die microphotographs are shown in Figure 6. DC biasing values for the TIA are shown in Table 1, as well as the biasings for the variable-gain and peaking settings. There are six TIA gain settings for this design.

The core area (input and mid-stages) of the TIA design is 39 μm × 26 μm.

$V_{G1}$, $V_{G2}$, $V_{P1}$, and $V_{P2}$ are variables to control the variable gains and peakings at different gain settings. The measured core TIA power is 7.84 mW and the buffer power is 5.01 mW. A Keysight PNA-X N5247A Network Analyzer was used to measure the S-parameters and IP$_{1dB}$. PNA port 1 was connected to $V_{in}$ and ports 2 and 3 to $V_{out+|-}$. The $V_X$ pad was not used.
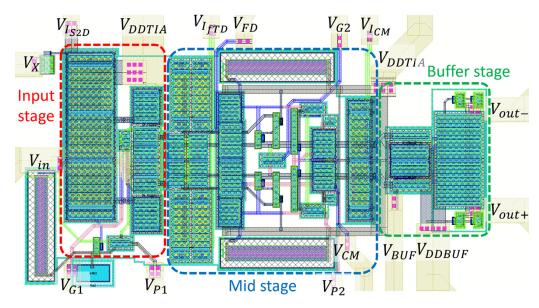
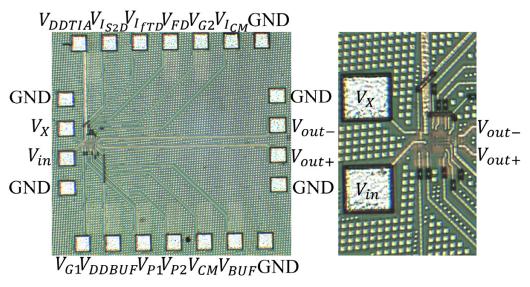**Figure 5.** Layout of the TIA input, mid and buffer stages.



**Figure 6.** Die microphotographs of different magnifications of the TIA.

**Table 1.** Bias settings for all DC pads for the TIA design and for the various gain and peaking settings.

| Bias Settings for All DC Pads | | | | | | |
|---|---|---|---|---|---|---|
| **Pad** | **DC (V)** | **Pad** | **DC (V)** | **Pad \*** | **DC (V)** | **I (mA)** |
| $V_{FD}$ | 1 | $V_{DDTIA}$ | 1.6 | $V_{I_{S2D}}$ | 0.7 | 1.4 |
| $V_{CM}$ | 0.85 | $V_{DDBUF}$ | 1 | $V_{I_{fTD}}$ | 0.9 | 2.9 [#] |
| $V_{BUF}$ | 0.2 | $V_{FD}$ | 1 | $V_{I_{CM}}$ | 1 | 0.12 |
| **Variable-gain and peaking DC biasings $V_{G1}$, $V_{P1}$, $V_{G2}$, $V_{P2}$ for different settings** | | | | | | |
| **TIA gain setting** | | $V_{G1}$ **(V)** | $V_{P1}$ **(V)** | $V_{G2}$ **(V)** | $V_{P2}$ **(V)** | |
| 1 (highest gain) | | 1 | 1 | 1 | 1 | |
| 2 | | 1.4 | 1.2 | 1 | 1 | |
| 3 | | 1.6 | 1.4 | 1 | 1 | |
| 4 | | 1.7 | 1.5 | 1 | 1.4 | |
| 5 | | 1.8 | 1.5 | 1.4 | 1.5 | |
| 6 (lowest gain) | | 1.9 | 1.5 | 1.7 | 1.6 | |

\* $V_{I_{S2D}}$, $V_{I_{fTD}}$, $V_{I_{CM}}$ are voltage-biased for equivalent $I_{S2D}$, $I_{S2D}$, $I_{S2D}$ biases. [#] $I_{fTD,A|B}$ have separate current mirror biasings, hence $I_{fTD} = I_{fTD,A} + I_{fTD,B}$.

## 5. Simulation and Measurement Results

### 5.1. Transimpedance Gain and Bandwidth

Both the post-layout simulation and measurement results of the proposed TIA differential transimpedance gain $Z_{T,d}$ frequency response are plotted in Figure 7 at settings 1–6.
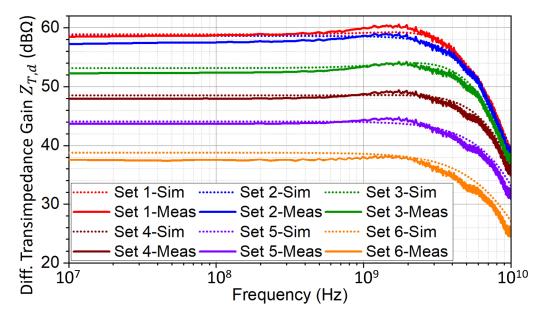


**Figure 7.** Simulated and measured differential transimpedance gain of the TIA at different gain settings.

The results of the TIA frequency response are in Table 2 below, with $Z_{T,d}$ taken at 100 MHz and bandwidth at –3 dB of $Z_{T,d}$. The measured $Z_{T,d}$ ranges from 37.5 to 58.7 dBΩ (range of 21.2 dBΩ) across settings 1–6, with bandwidth above 4.15 GHz. The TIA is also stable with limited peaking within the frequency response as shown.

**Table 2.** Simulated and measured gain, bandwidth and $IP_{1dB}$ of the TIA.

| TIA Gain Setting | Sim $Z_{T,d}$(dbΩ) | Sim BW (GHz) | Meas $Z_{T,d}$(dbΩ) | Meas BW (GHz) | Sim $IP_{1dB}$ (dBm) | Meas $IP_{1dB}$ (dBm) |
|---|---|---|---|---|---|---|
| 1 (highest gain) | 58.9 | 4.17 | 58.7 | 4.15 | −25.25 | −26.75 |
| 2 | 58.6 | 3.96 | 57.5 | 4.35 | −25.75 | −27 |
| 3 | 53.1 | 5.38 | 52.4 | 5.07 | −24 | −23.25 |
| 4 | 48.5 | 5.63 | 48.0 | 4.77 | −18.75 | −18.25 |
| 5 | 44.1 | 5.00 | 43.7 | 4.35 | −14.25 | −14 |
| 6 (lowest gain) | 38.8 | 4.23 | 37.5 | 4.04 | −9.75 | −9.75 * |

* Note that measured $IP_{1dB}$ for set 6 is extrapolated as the measured $P_{in}$ range is not wide enough; the shape of the measured curve is similar to the simulated curve.

### 5.2. $IP_{1dB}$ and Gain Compression

The input-referred 1 dB compression point ($IP_{1dB}$) is shown in Figure 8 with input power $P_{in}$ swept at 100 MHz.

The $IP_{1dB}$ ranges from –26.75 to –9.75 dBm across settings 1–6, proving that the gain variation design also greatly increases the $IP_{1dB}$. The results of the $IP_{1dB}$ are also in Table 2 below.

### 5.3. Noise and Dynamic Range

Both the input-referred noise current (IRNC) and noise figure (NF) of the TIA are simulated and plotted in Figure 9.
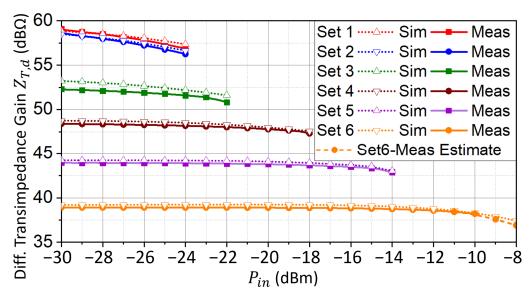
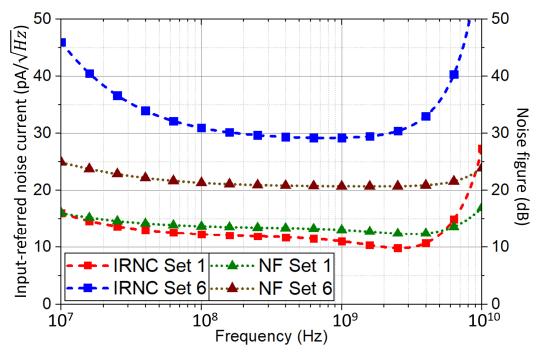**Figure 8.** Simulated and measured $IP_{1dB}$ of the TIA at different gain settings.



**Figure 9.** Simulated IRNC and NF of the TIA at maximum and minimum gain settings.

The IRNC and NF at 4 GHz for the maximum gain setting are 10.7 pA/$\sqrt{Hz}$ and 12.4 dB, respectively. The dynamic range lower limit is determined by IRNC at maximum gain and 4 GHz, as well as using a signal to noise ratio (SNR) of 49 for TIA specification [8]. This gives a minimum $I_{in}$ ($i_{pd}$) of 33.2 μA. The dynamic range upper limit is determined by the $IP_{1dB}$ at minimum gain during high $I_{in}$. Using $P_{in} = I_{in}^2 Z_{in}$ gives a maximum $I_{in}$ of 1.46 mA. Thus, using the gain range as a parameter allows for both the IRNC and the $IP_{1dB}$ of the TIA design.

*5.4. Eye Diagrams*

The simulated differential ($V_{outA} - V_{outB}$) eye diagrams of the TIA design are plotted in Figure 10 at the maximum and minimum gain settings with a 5 Gb/s 10 m$V_{pp}$ pseudo-random binary sequence (PRBS) input. The PRBS signal is used to prove that the TIA is able to function for any type of sequence of programmed signal.
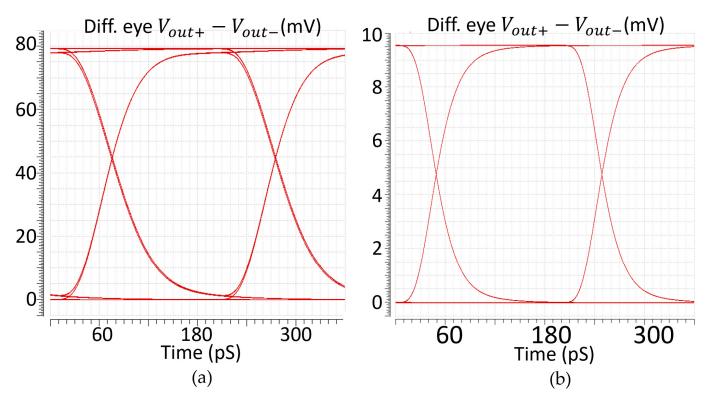
**Figure 10.** Simulated eye diagrams with 5 Gb/s 10 m$V_{pp}$ PRBS input signal at (**a**) maximum and (**b**) minimum gain settings.

As shown in Figure 10, the eye openings at both settings are large and clear with little jitter, showing no distortion of the input signal throughout the TIA and thus suitable for VLC.

*5.5. Load Capacitance Invariability*

The S-parameter differential transimpedance gain $Z_{T,d}$ measurement results can also be plotted with a range of larger $C_{pd}$ values to prove its input load shielding and load capacitance invariance ability. The frequency response when the $C_{pd}$ load is varied is shown in Figure 11.

As shown in Figure 11, when $C_{pd}$ is increased from 0.5 pF to 2.5 pF (500%), the measured bandwidth drops from 4.15 GHz to 1.54 GHz, which is only a drop of 63% for the TIA maximum gain setting. Likewise, the bandwidth drops from 4.04 GHz to 1.24 GHz (drop 69%) for the minimum gain setting. The frequency response also does not peak when $C_{pd}$ is increased, proving that it is also a more stable design, unlike [8]. A $C_{pd}$-invariance TIA design would allow a larger photodiode to be used to absorb more light signal and thus output a more detectable current to input into the TIA. Hence, this increases the range of distance between the transceiver and receiver.
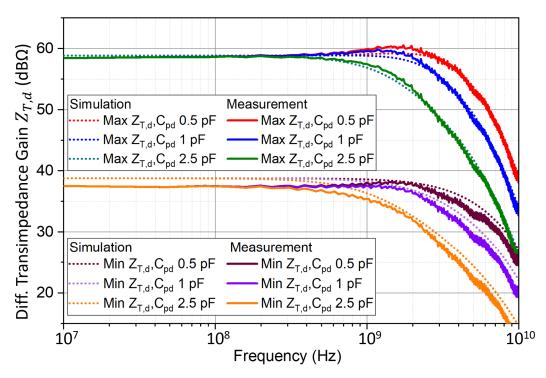
**Figure 11.** Simulated and measured transimpedance gain of the TIA with range of $C_{pd}$ values.

## 6. Discussion and Comparison

A figure of merit (FOM) is used to compare the TIA designs [8]:

$$FOM = \frac{Gain\ (\Omega) \times BW\ (GHz) \times\ C_{pd}\ (pF) \times\ Gain\ Range\ (dB\Omega)}{Core\ Power\ (mW)}$$

Table 3 compares this TIA design with other recent measured variable-gain TIAs and it has the highest FOM among all the designs.

**Table 3.** Table of comparison of this TIA design with other recent works.

| Parameter | [8] [a] | | [13] | [15] [b] | [16] | This Work |
|---|---|---|---|---|---|---|
| Technology | 0.18 μm CMOS | | 0.18 μm CMOS | 0.13 μm CMOS | 65 nm CMOS | 40 nm CMOS |
| $V_{DD}$ (V) | 1.8 | | 1.8 | 3 | 1.2 | 1.6 |
| $C_{pd}$ (pF) | 0.25 | | 0.5 | 2 | 0.45 | 0.5 |
| Max gain (dBΩ) | 60.6 | 62.8 | 69.3 | 78 | 76 | 58.7 |
| Gain range (dBΩ) | 36.1 | 35 | 13.5 | 30 | 16 | 21.2 |
| BW (GHz) | 6.42 | 5.22 | 1 | 0.64 | 0.3 | 4.15 |
| Power (mW) | 30.7 | 27.5 | 6 | 114 | 6 | 7.84 |
| Area (mm$^2$) | 0.0085 | 0.0085 | 0.0075 | 0.587 | 0.015 | 0.001 |
| IRNC $\left(\frac{pA}{\sqrt{Hz}}\right)$ | 10.3 [c] | 21.7 [c] | 9.33 | 5.6 | 2 [c] | 10.7 [c] |
| FOM | 2022 | 2293 | 3282 | 2676 | 2271 | 4831 |

[a] This paper has two different designs, [b] for the entire receiver module including TIA, [c] simulated data.

The architecture of proposed TIA design in this paper is different and improved from the various compared designs. The designs in [13,15,16] only have either a CG, CS or inverter-type input stage, making it difficult to balance the gain-bandwidth trade-off. Conversely, the input stage of the proposed design has both CG and CS in a modified cross-coupled RGC design. This, together with the unique combined active inductor with capacitive degeneration structure in its mid-stage allows it to have a significantly larger

bandwidth over [13,15,16], making it suitable for high frequency operation unlike those other designs.

Although the bandwidths of the designs in [8] are larger, their power consumption are much larger due to the multiple CS stages required to increase the gain. The designs in [8] also lack a current mirror current source and thus result in a risk of transistors being biased out of their ideal operating regions, reducing the actual input signal dynamic range. Thus, the TIA presented in this paper is the overall best design based on both its practicability for VLC applications and on the FOM used.

## 7. Conclusions

The authors present an inductorless variable-gain TIA using the UMC 40 nm CMOS process that has a unique single-to-differential cross-coupled modified RGC input stage and a modified $f_T$-doubler mid-stage with a unique combined active inductor and capacitive degeneration design for bandwidth enhancement. The measured transimpedance gain range of 37.5–58.7 dBΩ and bandwidth of 4.15 GHz show that the TIA is suitable for practical high-speed visible light communication applications.

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